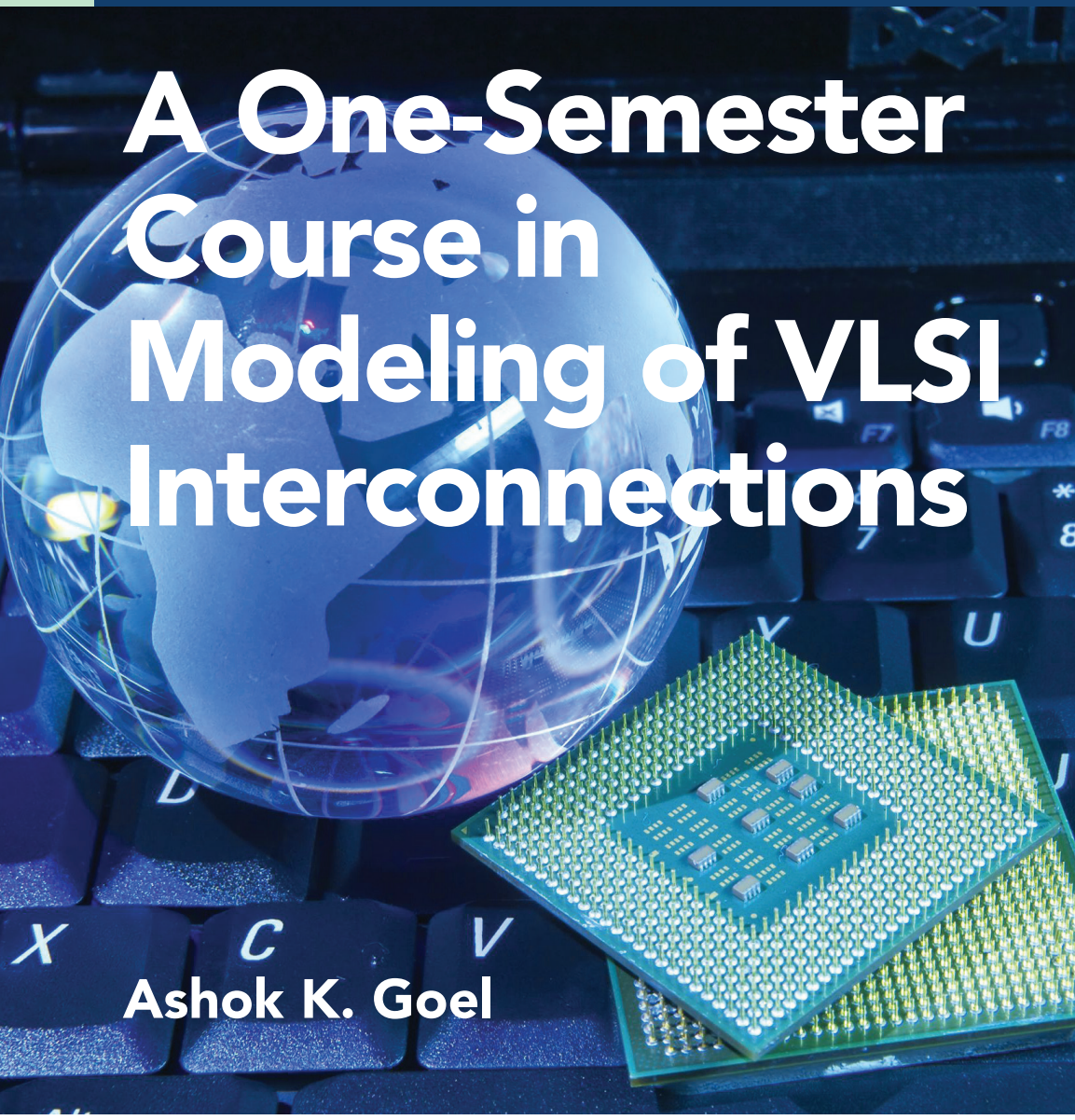
ELECTRONIC CIRCUITS AND SEMICONDUCTOR DEVICES COLLECTION

Ashok K. Goel, *Editor*

A One-Semester Course in Modeling of VLSI Interconnections



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Modeling of VLSI Interconnections

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Dedicated to

All My Students
Undergraduate and Graduate
For Giving a Purpose to My Life!

Abstract

Quantitative understanding of the parasitic capacitances and inductances and the resultant propagation delays and crosstalk phenomena associated with the metallic interconnections on the very large scale integrated (VLSI) circuits has become extremely important for the optimum design of the state-of-the-art integrated circuits. It is because more than 65 percent of the delays on the integrated circuit chip occur in the interconnections and not in the transistors on the chip. Mathematical techniques to model the parasitic capacitances, inductances, propagation delays, crosstalk noise, and electromigration-induced failure associated with the interconnections in the realistic high-density environment on a chip will be discussed. An overview of the future interconnection technologies for the nanotechnology circuits will also be presented.

This book will be the first book of its kind written for a one-semester course on the mathematical modeling of metallic interconnections on a VLSI circuit. In most institutions around the world offering BS, MS, and Ph.D. degrees in Electrical and Computer Engineering, such a course will be suitable for the first-year graduate students and it will also be appropriate as an elective course for senior level BS students. This book will also be of interest to practicing engineers in the field who are looking for a quick refresher on this subject.

Keywords

VLSI, Integrated Circuits, Interconnections, Copper Interconnections, Propagation Delays, Crosstalk, Modeling, Electromigration, Capacitances, Inductances, Nanotechnology

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Preface

Continuous advances in the very-large-scale integrated circuit (VLSI) technology have resulted in complex chips having millions of interconnections that integrate the components on IC chip. The customer demands for higher speeds and smaller chips have led to the use of interconnections in the multilevel and multilayer configurations. At present, the interconnections play the most significant role in determining the size, power consumption, and clock frequency of a digital system. Parasitic capacitances, resistances, and inductances, and their effects on the crosstalk and propagation delays associated with the interconnections in the high-density environments have become the major factors in the evolution of the very-high-speed integrated circuit technology. Furthermore, during the last decade, several developments have taken place in the field of VLSI interconnections such as the introduction of copper interconnections for VLSI applications, realization of the importance of including inductances in the delay and crosstalk models for the very-high-speed circuits, further research on optical interconnections, and the possibility of realizing nanotechnology integrated circuits using nanowires, nanotubes, and wireless interconnections.

This book is written primarily as a textbook for a one-semester course suitable for senior-level and first-year graduate students in electrical engineering. It can also be used as a reference book by a practicing professional who wants to gain a better understanding of the issues associated with the high-speed interconnections. Reader is expected to have a basic understanding of the electromagnetic wave propagation.

The chapters in this book are designed such that they can be read independently of one another while, at the same time, being parts of one coherent unit. To maintain independence among the chapters, some material has been intentionally repeated. Several appropriate exercises are provided in each chapter which are designed to be challenging as

well as helping the student gain further insight into the contents of the chapter. The six chapters contained in this book can be described briefly as follows:

Chapter 1—Introductory Concepts

In this chapter, a few basic techniques used in this book and some advanced concepts regarding wave propagation in an interconnection are presented. Various types of interconnections employed in VLSI applications including the multilevel and multilayer interconnections are discussed. Advantages of copper interconnections and their fabrication techniques are reviewed. A resistive interconnection has been modeled as a ladder network. The various modes that can exist in a microstrip interconnection are described and a quasi-TEM analysis of the slow-wave mode propagation in the interconnections is presented. The various measures of propagation delays including the delay time and rise time are defined. More introductory information is included in the appendixes presented at the end of the book. There are appendixes on the method of images used to find the Green's function matrix and the method of moments used to determine the interconnection capacitances. The even and odd mode capacitances for two and three coupled conductors are discussed and the transmission line equations are derived. The Miller's theorem which can be used to uncouple the coupled interconnections is presented. An efficient numerical inverse Laplace transformation technique is described.

Chapter 2—Modeling of Interconnection Resistances, Capacitances, and Inductances

In this chapter, numerical techniques that can be used to determine the interconnection resistances, capacitances, and inductances on a high-density VLSI chip are discussed and the dependence of these parasitic elements on the various interconnection design parameters is discussed. Approximate formulas for calculating the parasitic capacitances for a few interconnection structures are presented. An algorithm to obtain the

interconnection capacitances by the Green's function method where the Green's function is calculated by using the method of images is presented. The Green's function is also calculated by using the Fourier integral approach and a numerical technique to determine the capacitances for a multilevel interconnection structure in the Si-SiO_2 composite is presented. An improved network analog method to determine the parasitic capacitances and inductances associated with the high-density multilevel interconnections on the GaAs-based integrated circuits is presented. Simplified formulas for the interconnection capacitances and inductances on the oxide-passivated silicon and semi-insulating gallium arsenide substrates are provided. A program called FastHenry which can be used to determine the inductances associated with an interconnection structure is described. A model for understanding the resistances for copper interconnections is presented.

Chapter 3—Modeling of Interconnection Delays

In this chapter, numerical algorithms which can be used to calculate the propagation delays in the single and multilevel parallel and crossing interconnections are presented and the dependence of the interconnection delays on the various interconnection design parameters is discussed. An analysis of interconnection delays on very high-speed VLSI chips using a metal-insulator-semiconductor microstrip line model is presented. A computer-efficient model based on the transmission line analysis of the high-density single-level interconnections on the GaAs-based integrated circuits is presented. A SPICE model for the lossless parallel interconnections modeled as multiple coupled microstrips is presented and this model is extended to include lossy parallel and crossing interconnections. The high-frequency effects such as conductor loss, dielectric loss, skin-effect, and frequency-dependent effective dielectric constant are studied for a microstrip interconnection. Compact expressions of propagation delays for the single and coupled interconnections modeled as RC and RLC circuits are provided. The active interconnections driven by several mechanisms are also analyzed.

Chapter 4—Modeling of Interconnection Crosstalk

In this chapter, the mathematical algorithms which can be used to study the crosstalk effects in the single and multilevel parallel and crossing interconnections are discussed and the dependence of the crosstalk effects on the various interconnection design parameters is studied. Crosstalk among the neighboring interconnections is calculated by using a lumped-capacitance approximation. Crosstalk in very high-speed VLSICs is analyzed by using a coupled multiconductor metal-insulator-semiconductor microstrip line model for the interconnections. Single level interconnections are investigated by the frequency-domain modal analysis and a transmission line model of the crosstalk effects in the multilevel interconnections is presented. Compact expressions for studying the crosstalk effects in the interconnections modeled as RC and RLC circuits are provided.

Chapter 5—Modeling of Electromigration-Induced Interconnection Failure

In this chapter, the degradation of the reliability of an interconnection due to electromigration is discussed. First, several factors related to electromigration in the VLSI interconnections are reviewed. The basic problems that cause electromigration are outlined, the mechanisms and dependence of electromigration on several factors is discussed, testing and monitoring techniques and guidelines are presented, and the methods of reducing electromigration in the VLSI interconnections are briefly discussed. Electromigration in the copper interconnections is also studied.

Chapter 6—Other Interconnection Technologies

In this chapter, a few interconnection technologies that seem promising for the future integrated circuits are discussed. The advantages, issues, and challenges associated with the optical interconnections are discussed. The propagation characteristics and the comparison of superconducting interconnections with the normal metal interconnections are presented. Various technologies that seem promising for nanotechnology circuits including the nanowires, nanotubes, and quantum cell-based wireless

interconnections are briefly discussed. This chapter ends with an overview of the nanotube integrated circuits and a comparison of nanotubes with the copper interconnections.

It should be noted that the various computer models presented in this book may not have been validated by experimental measurements and therefore should be used in computer-aided design programs with caution. Finally, in the internet-based information age, it is necessary to give references to certain websites. Though these websites are active at the time of preparation of this manuscript yet it is possible that these may become inactive in future.

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Disclaimer

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A.K.G.
Houghton, Michigan

CHAPTER 1

Introductory Concepts

In this chapter, basic concepts regarding the metallic interconnections used in very-large-scale integration (VLSI) circuits are presented. Here are the chapter objectives:

- After going through section 1.1, students should be familiar with the various types of metallic interconnections employed in VLSI applications. They should understand the advantages and challenges posed by the copper interconnections and be familiar with the techniques used for their fabrication.
- After going through section 1.2, students should be able to model a resistive metallic interconnection as a ladder network.
- After going through section 1.3, students should be familiar with the various propagation modes that can exist in a metallic interconnection.
- After going through section 1.4, students should be able to analyze the slow-wave mode propagation in an interconnection.
- After going through section 1.5, students should be able to define different kinds of propagation delays used in the literature.

1.1 Metallic Interconnections

Continuous advances in integrated circuit (IC) technology have resulted in smaller device dimensions, larger chip sizes, and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. In the recent years, growth of GaAs on silicon (Si)

substrate has met with a great deal of interest because of its potential applications in the new hybrid technologies [1–11]. GaAs-on-Si unites the high speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from research to device and circuit development [12–15].

So far, the various IC technologies have employed metallic interconnections and there is a possibility of using optical interconnections in the near future. Recently, the possibility of using superconducting interconnections is also being explored. Optical and superconducting interconnections are discussed in chapter 6.

Multilevel and Multilayer Interconnections

VLSI chips require millions of closely spaced interconnection lines that integrate the components on a chip. As the VLSI technology advanced to meet the needs of the customers, it became necessary to use multilayer interconnections in two or more levels to achieve higher packing densities, shorter transit delays, and smaller chips. In this book, the term "level" will be used to describe conductors which are separated by an insulator and the term "layer" will be used to describe different conductors tiered together in one level of interconnection as shown in Figure 1.1.1. In most cases, because of its low resistivity and silicon compatibility as shown in Table A3 [16], aluminum has been used to form the metal interconnections. However, as the device dimensions are decreased, the current density increases resulting in decreased reliability due to electromigration and hillock formation causing electrical shorts between successive levels of Al [17–20]. Tungsten has also been used for interconnects [21–23] and, sometimes, Al/Cu is used to solve problems characteristic of pure Al [24] though this choice has not been without problems [25, 26]. There have been several studies [27–34] aimed at reducing electromigration. All these studies have used layers of two or more metals in the same level of the interconnection. Some of the multilayer structures studied so far have been Al/Ti/Cu [28], Al/Ta/Al [30], Al/Ni [31], Al/Cr [32], Al/Mg [33], and Al/Ti/Si [34]. Co-evaporation of Al–Cu–Ti, Al–Cu–Ti, Al–Cu–Co,

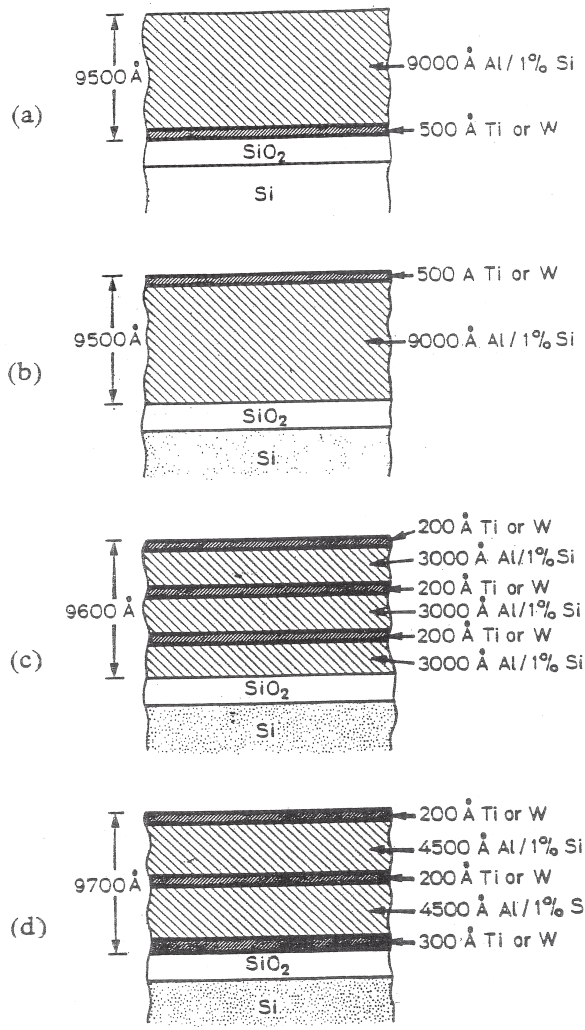

Figure 1.1.1 Schematic diagrams of layered interconnection structures using (a) Ti layer used to match the aluminum and silicon expansion coefficients; (b) Ti or W layer on top of aluminum to constrain hillocks; (c) and (d) multiple layers of Ti or W alternated with aluminum

and Al–Co has also been shown to decrease electromigration [27]. There have been many studies on the problem of hillock formation as well [16, 35–44]. One method of reducing these hillocks on the silicon-based circuits has been to deposit a film of WSi [36] or MoSi between Al and

Table A4 Resistivity and expansion coefficients [1.16] (© 1985 IEEE)

Material	Resistivity (μΩ.cm)	Thermal Expansion Coefficient (°C−1)	Melting Point (°C)
Pure aluminum (bulk)	2.65	$25.0 \cdot 10^{-6}$	660°C
Sputtered Al and Al/Si	2.9–3.4	$25.0 \cdot 10^{-6}$	660°C
Sputtered Al/2% Cu/1% Si	3.9	$25.0 \cdot 10^{-6}$	660°C
LPCVD aluminum	3.4	$25.0 \cdot 10^{-6}$	660°C
Pure tungsten (bulk)	5.65	$4.5 \cdot 10^{-6}$	3410°C
CVD tungsten	7–15	$4.5 \cdot 10^{-6}$	3410°C
Evaporated/sputtered tungsten	14–20	$4.5 \cdot 10^{-6}$	3410°C
Ti (bulk)	42.0	$8.5 \cdot 10^{-6}$	1660°C
$TiAl_3$ (bulk)	17–22	—	1340°C
$CuAl_2$ (bulk—θ phase)	5–6	—	591°C
WAl_{12}	—	—	647°C
Si	—	$3.3 \cdot 10^{-6}$	—
SiO_2	—	$0.5 \cdot 10^{-6}$	—

the silicon substrate. A complete elimination of hillocks is reported in studies where the VLSI interconnections were fabricated by layering alternately Al and a refractory metal (Ti or W) [16, 42–44].

Copper Interconnections

To be able to produce high-speed ICs, it is always desirable to use interconnections that would allow rapid transmission of information, i.e., signals among the various components on the chip. For the last forty years, aluminum has been used almost exclusively to make metallic interconnection lines on the ICs. More recently, aluminum–copper alloys have been used because they have been shown to provide better reliability than pure aluminum. In December 1997, in order to lower the resistance of the metallic interconnections, IBM announced their plans to replace aluminum with copper, a metal with lower resistivity of less than 2 μΩ.cm compared to that of about 3 μΩ.cm for aluminum. It is worth mentioning that while copper interconnections have been a hot topic in

the semiconductor industry since the IBM announcement, the race to improve the aluminum interconnect technology has not slowed down. In fact, semiconductor companies are exploring new technologies for aluminum-based interconnections. These include ionized plasma deposition, hot aluminum physical vapor deposition (PVD), and aluminum damascene structures. It is expected that while advanced microprocessors and fast memory circuits may switch to copper interconnections, aluminum-based interconnections deposited by using the latest techniques will continue to coexist at least in the near future.

While the semiconductor industry has known the potential advantages of using copper interconnects since the 1960s, it took over 30 years for it to overcome the associated challenges until it was announced in a paper on the CMOS 7S technology presented at the Institute of Electrical and Electronics Engineers' IEDM conference by IBM in December 1997. Following is a summary of the advantages of copper interconnects and the challenges in the way of implementing this technology:

Advantages of Copper Interconnections

a) An obvious advantage of the copper is its lower electrical resistivity compared with aluminum. In fact, copper interconnects offer 40 percent less resistance to electrical conduction than the corresponding aluminum interconnects which results in speed advantages of as much as 15 percent in microprocessor circuits employing copper interconnects.
b) The phenomenon of electromigration that results in the movement of atoms and molecules in the interconnects under high stress conditions of high temperatures and high current densities causing open and short-circuit failures of interconnects through the formation of voids and hillocks is known to occur much less frequently in the copper interconnects than in the aluminum interconnects. That is why aluminum–copper alloys have been preferred over pure aluminum as the interconnect material.
c) Copper interconnects can be fabricated with widths in the range of 0.2 μm while it has been difficult to reduce dimensions below 0.35 μm with aluminum interconnects. This reduction in the interconnection

dimensions allows much higher packing densities of the order of 200 million transistors per chip.

d) It has been claimed that the deposition of copper interconnects can be achieved with a potential cost saving of up to 30 percent which translates into a saving of about 10 to 15 percent for the full wafer [45].

Challenges Posed by Copper Interconnects

In the United States, a consortium of 10 leading chip-making semiconductor companies known as SEMATECH (SEmiconductor MAnufacturing TECHnology) has worked hard to overcome the challenges posed by the replacement of aluminum interconnects by the copper interconnects. Following is a list of technical challenges that must be addressed and met within acceptable standards to fabricate copper-based IC chips [46]:

a) Copper is considered poisonous for silicon-based circuits. It diffuses rapidly into the active source, drain, and gate regions of transistors built on the silicon substrate and alters their electrical properties affecting the functionality of the transistors.
b) In order to meet the above challenge alone, an entirely new fabrication process is required for implementation of the copper interconnects.
c) Fabrication of copper interconnects requires the production and use of a large amount of ultra-pure water which is rather expensive.
d) The release of waste discharges containing copper to the environment must be handled very carefully.

Fabrication Processes for Copper Interconnections

As shown in Figure 1.1.2, a conventional photolithographic process for depositing aluminum interconnects on the silicon substrate involves the following steps:

a) Deposit a layer of silicon dioxide insulator on the silicon wafer.
b) Deposit a layer of metal on the silicon dioxide layer.

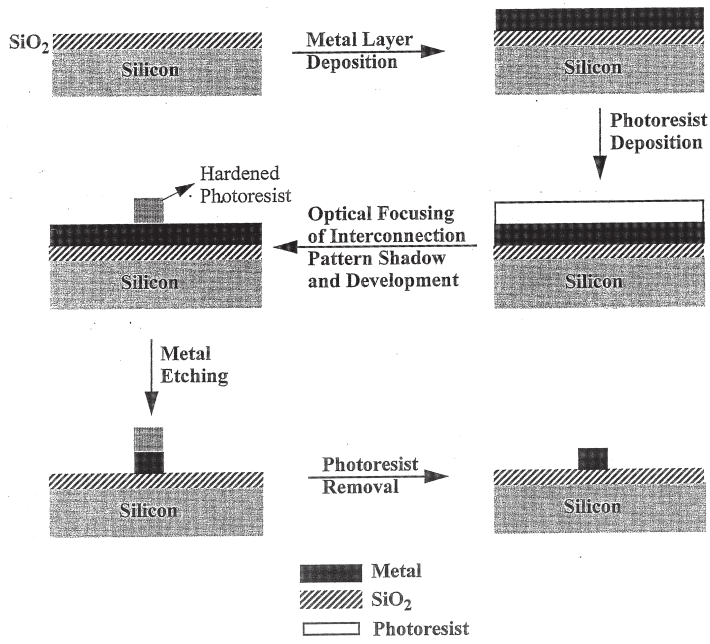

Figure 1.1.2 Conventional photolithographic process steps for depositing aluminum metallization on the silicon substrate

c) Cover the metal layer by depositing a layer of photoresist on it.
d) Project a shadow of the interconnect pattern (drawn on a reticle) on the photoresist layer by using ultraviolet rays and an optical projection system.
e) Develop the photoresist that was exposed to the ultraviolet light.
f) Using proper chemicals, etch away parts of the metal layer that are not covered by the hardened photoresist.
g) Finally, remove the hardened photoresist leaving the interconnect metal in the desired pattern on the silicon dioxide layer.

Since copper can contaminate the silicon substrate and the silicon dioxide dielectric layer of an IC resulting in increased junction leakages and threshold voltage instabilities, barrier layers are required to isolate the copper interconnects from the substrate and the dielectric layer. The barrier layer, usually made from tungsten or titanium nitride, should be as

thin as possible to minimize the resistance and to maximize the reliability of the copper interconnects. It is applied after the interconnect channels have been etched out in the dielectric layer by photolithography. The barrier layer is covered by a microscopic seed layer of copper to ease further deposition of copper on the entire wafer by electroplating. Finally, the excess copper is removed by a chemical mechanical polishing process leaving the desired pattern of copper interconnects on the wafer. The various steps are shown in Figure 1.1.3.

Various techniques have been studied for deposition of copper interconnects on the silicon-based circuits. These include chemical vapor deposition (CVD), electroless plating, and electrolytic plating [45]. In each case, the objective was to deposit very thin and even layers of copper interconnects in the horizontal direction and vias in the vertical direction for connecting interconnects in different levels. It was found that the CVD and electroless plating techniques encountered several problems during fabrication whereas electrolytic plating worked satisfactorily resulting in even copper films with a faster rate of deposition.

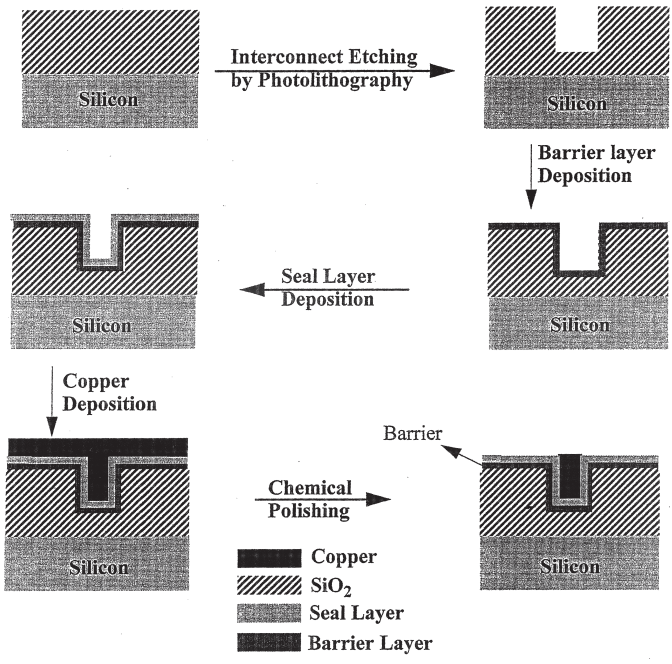

Figure 1.1.3 Various steps involved in depositing copper metallizations

Damascene Processing of Copper Interconnects

At present, damascene electroplating process is used frequently to make copper on-chip interconnects. The term "Damascene" originates from the fact that a somewhat similar technique was used by the metallurgists of old Damascus to produce sharpest polished swords in the medieval era. In the world of semiconductor processing, this technique was initially used to form vias that are used to connect interconnects at different levels of an IC.

In damascene processing, the patterns of interconnects or vias are formed first by etching the oxide on the substrate. Then the seed layer is deposited on the patterned substrate/oxide. This is followed by copper electroplating which deposits inside and outside the patterned features. Special care is taken to avoid the formation of voids and seams (shown in Figure 1.1.4) during the late stages of the copper deposition. The excess copper is finally removed by the chemical mechanical planarization process. The various steps involved in making the copper interconnects using the damascene process are shown in Figure 1.1.5. This process is repeated several times to form interconnects and vias for a multilevel interconnect structure required on an IC chip.

The process described above is called the "single" damascene process because it differs from the more widely used "dual" damascene process in which both the interconnects and the vias are first patterned by etching of the substrate/oxide before the seed layer is formed and copper is deposited. It reduces the number of processing steps by avoiding one copper deposition step and one planarization step for each level of the interconnect structure. The steps involved in making the copper interconnects using the dual damascene process are shown in Figure 1.1.6.

Figure 1.1.4 Schematic diagrams of voids and seams that may be formed during the late stages of the copper deposition

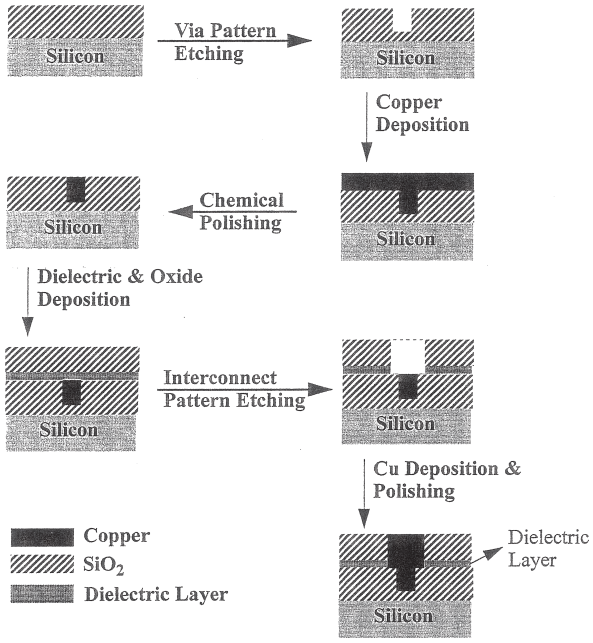

Figure 1.1.5 Steps involved in depositing the copper interconnections and vias using the single-damascene process

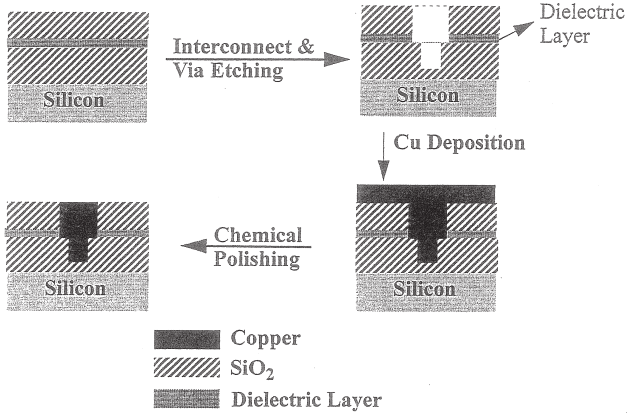

Figure 1.1.6 Steps involved in depositing the copper interconnections and vias using the dual-damascene process

1.2 Simplified Modeling of Resistive Interconnections as Ladder Networks

It is well known that interconnections made of high-resistivity materials such as polycrystalline silicon (poly-Si) result in much higher signal delays than the low-resistivity metallic interconnections. However, in the past, poly-Si has remained a principal material for the second level interconnections. In order to analyze high-speed signal propagation in resistive interconnections, it is important to understand their transmission characteristics. In this section, it has been shown that resistive interconnections can be modeled as ladder resistor–capacitor (RC) networks under open circuit, short circuit as well as capacitive loading conditions [47, 48].

Open Circuit Interconnection

From the transmission line theory [49], the open circuit voltage transfer function of a resistive transmission line is given by

$$\frac{V_2}{V_1} = \frac{1}{\cosh(\sqrt{sRC})} \tag{1.2.1}$$

where R is the total line resistance and C is the total line capacitance including the capacitance due to the fringing fields as described by Ruehli and Brennan [50]. Using infinite partial fraction expansions [51], Eqn. (1.2.1) can be written as

$$\begin{aligned}\frac{V_2}{V_1} &= \frac{1}{\cosh(\sqrt{sRC})} \\ &= \frac{4}{\pi}\sum_{k=1}^{\infty}\left[(-1)^{(k+1)}\frac{(2k-1)}{(2k-1)^2 + sRC\left(\frac{4}{\pi^2}\right)}\right]\end{aligned} \tag{1.2.2}$$

If $v_1(t)$ is a Dirac pulse, then the voltage $v_2(t)$ can be found easily by finding the inverse Laplace transforms of the terms on the right side of

Eqn. (1.2.2). If $v_1(t)$ is a unit step voltage then $V_1 = V_0/s$ (with $V_0 = 1$) and $v_2(t)$ can be obtained after a simple integration to be:

$$v_2(t) = L^{-1}\left[\frac{1/s}{\cosh(\sqrt{sRC})}\right]$$

$$= \sum_{k=1}^{\infty} (-1)^{(k+1)} \frac{4}{\pi(2k-1)}\left(1 - e^{-\frac{(2k-1)^2\pi^2 t}{4RC}}\right)$$

or

$$v_2(t) = \frac{4}{\pi}\left(1 - \frac{1}{3} + \frac{1}{5} - \frac{1}{7} + \ldots\right) - \frac{4}{\pi}\left(e^{-\frac{\pi^2 t}{4RC}} - \frac{1}{3}e^{-\frac{9\pi^2 t}{4RC}} + \ldots\right)$$

$$= 1 - 1.273e^{-\frac{\pi^2 t}{4RC}} + 0.424e^{-\frac{9\pi^2 t}{4RC}} - 0.254e^{-\frac{25\pi^2 t}{4RC}} + \ldots \quad (1.2.3)$$

It should be noted that the expression (1.2.3) differs from the corresponding approximate expression in reference [47]

$$v_{out}(t) = 1 - 1.172e^{-\frac{\pi^2 t}{4RC}} + 0.195e^{-\frac{9\pi^2 t}{4RC}} - 0.023e^{-\frac{25\pi^2 t}{4RC}} \quad (1.2.4)$$

which was obtained by a finite partial fraction expansion of an infinite expansion of Eqn. (1.2.1). It can be seen that the terms of the second and higher orders in Eqn. (1.2.4), which are particularly important at low values of time, are far from correct.

A T-network and the corresponding n-stage ladder network for an interconnection line are shown in Figure 1.2.1(a) and (b), respectively. In Figure 1.2.1(b), $r_i = R/(n+1)$ and $c_i = C/n$. Now, we need to determine the number of ladder stages required to generate the output voltage based on the transmission line model given by Eqn. (1.2.3). Assuming unit step input, a comparison of the plots of the output voltage versus time for an open circuited interconnection obtained by using Eqn. (1.2.3), obtained by a numerical simulation of the T-network, and those obtained by numerical simulations of the ladder network with different number of stages is shown in Figure 1.2.2. For the sake of comparison, the output voltage plot obtained by using the approximate expression (1.2.4) is also

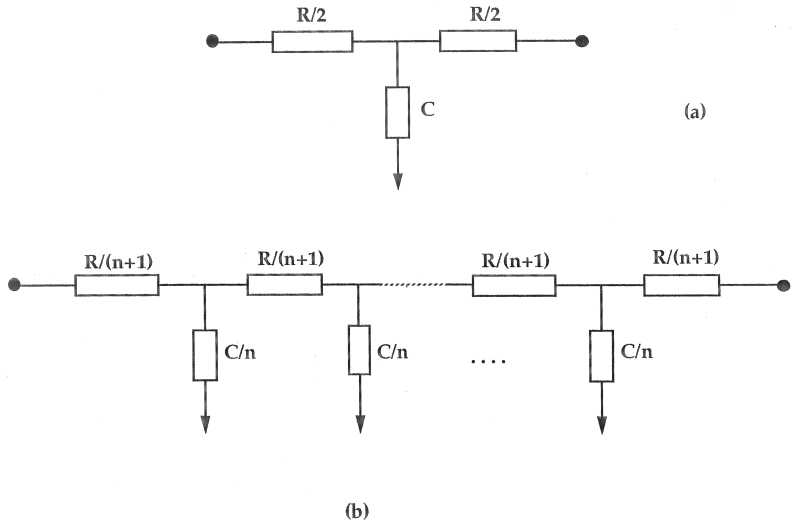

Figure 1.2.1 Representation of an interconnection line as (a) T network, and (b) n-stage ladder network [1.54]. (© 1983 IEEE)

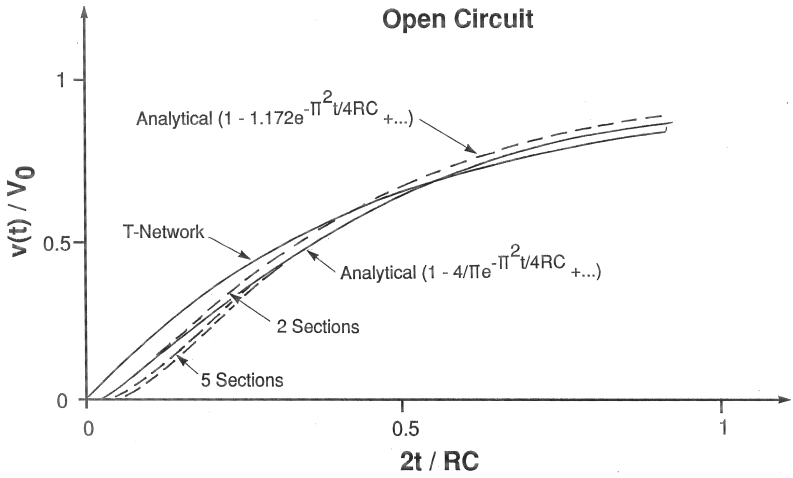

Figure 1.2.2 Output voltage versus time for an open resistive transmission line for a unit step input voltage [1.55]. (© 1983 IEEE)

included in Figure 1.2.2. It can be seen that the plot obtained by using Eqn. (1.2.3) almost coincides with that obtained for the ladder network with five stages. In fact, there is negligible difference between the results for the 5-stage and 10-stage ladder networks.

For an interconnection line loaded with a capacitance C_L, the voltage transfer function can be easily obtained in the s-domain but its analytical inverse Laplace transformation is not possible. Therefore, lumped circuit approximations have to be used. It can be shown that, for a wide range of C_L/C values, a five-stage ladder network yields sufficient accuracy. Thus, the conclusion for an open circuit interconnection also holds for a capacitively loaded interconnection.

Short-Circuited Interconnection

For a short-circuited *RC* transmission line, the output current for a step input voltage V_0/s is given by

$$I = CV_0 \frac{1}{(\sqrt{sRC})\sinh(\sqrt{sRC})} \tag{1.2.5}$$

Using infinite partial fraction expansion [51], Eqn. (1.2.5) can be written as

$$I = CV_0 \left[\frac{1}{sRC} + \frac{2}{RC} \sum_{k=1}^{\infty} (-1)^k \frac{1}{s + \left(\frac{\pi^2 k^2}{RC}\right)} \right] \tag{1.2.6}$$

The output current in the time domain can then be easily obtained by finding the inverse Laplace transforms of the terms on the right side of Eqn. (1.2.6) to be

$$i(t) = \frac{V_0}{R} \left[1 - 2e^{-\left(\frac{\pi^2 t}{RC}\right)} + 2e^{-\left(\frac{\pi^2 4t}{RC}\right)} - 2e^{-\left(\frac{\pi^2 9t}{RC}\right)} + \ldots \right] \tag{1.2.7}$$

Assuming unit step input, a comparison of the plots of the output current versus time for a short-circuited interconnection obtained by using Eqn. (1.2.7), obtained by a numerical simulation of the T-network, and those obtained by numerical simulations of the ladder network with different number of stages is shown in Figure 1.2.3. It can be seen that, for a short-circuited interconnection, at least 10 stages are required in the ladder network to obtain a good agreement with the analytical solution.

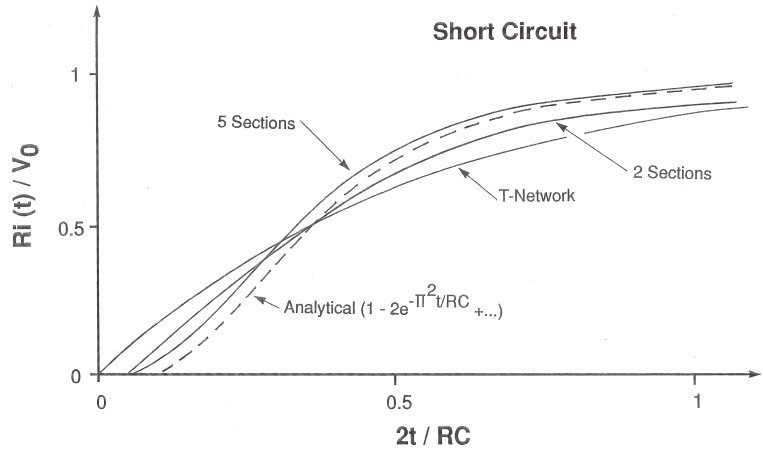

Figure 1.2.3 Output current versus time for a short circuited resistive transmission line for a unit step input voltage [1.55]. (© 1983 IEEE)

1.3 Propagation Modes in a Metallic Interconnection

A resistivity–frequency mode chart of the metal–insulator–semiconductor (MIS) microstrip line [52] is shown in Figure 1.3.1 where δ is the skin depth and ρ is the semiconductor resistivity. It can be seen from this figure that the propagation mode in the microstrip depends on the substrate resistivity and the frequency of operation. Figure 1.3.1 shows the following:

a) When the substrate resistivity is low (less than approximately 10^{-3} Ω.cm) then the substrate acts like an imperfect metal wall having a large skin effect resulting in the skin-effect mode.
b) When the substrate resistivity is high (greater than approximately 10^{4} Ω.cm) then the substrate acts like an insulator and the dielectric quasi-transverse electromagnetic (TEM) mode propagates.
c) For an MIS waveguide, the slow-wave mode propagates when the substrate is semiconducting and the frequency is low. Slow-wave mode results because, in the low frequency limit (note that this frequency limit extends into the gigahertz range at certain substrate resistivities), the electric field lines do not penetrate into the semiconductor whereas the magnetic field lines can fully penetrate into it causing spatially separated storage of electric and magnetic energies.

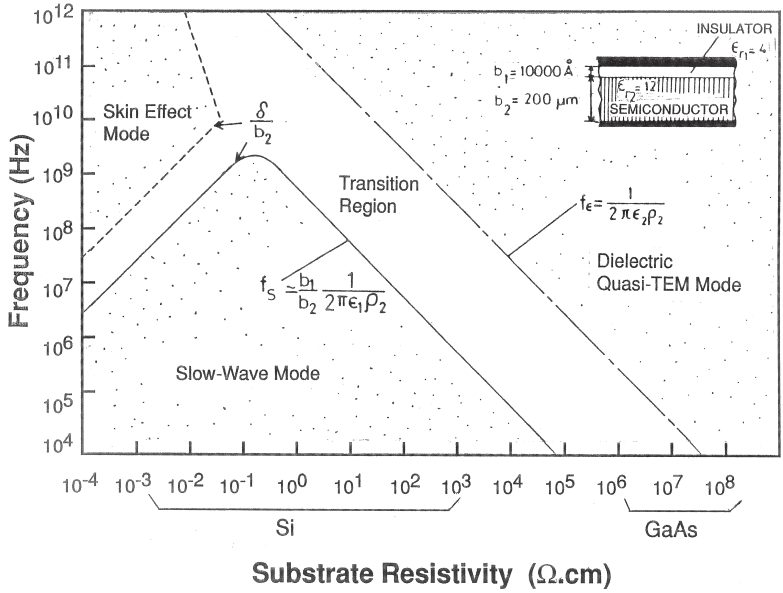

Figure 1.3.1 Resistivity-frequency mode chart of the MIS microstrip line [1.62]. (© 1984 IEEE)

1.4 Slow-Wave Mode

Now, a quasi-TEM analysis of slow-wave mode propagation in the micron-size coplanar MIS transmission lines on heavily doped semiconductors [53] will be presented. The analysis includes metal losses as well as semiconductor losses. The quantities derived from the quasi-TEM analysis are compared with those measured experimentally for a system of four micron-size coplanar MIS transmission lines fabricated on N^+ silicon.

Quasi-TEM Analysis

The geometry of the microstructure MIS transmission lines used in this analysis is shown in Figure 1.4.1. For the experimental results presented below, these structures consist of coplanar aluminum strips (fabricated by evaporating Al on SiO_2) separated from antimony-doped N^+ silicon substrate of doping density $N_d \sim 3 \times 10^{18}$ cm^{-3} and electrical conductivity 80 $\Omega.cm^{-1}$ by a thin SiO_2 layer. For the four transmission lines used in the experimental results, the wafer thickness (d) is 530 μm, the length (l) is 2,500 μm, and the metal thickness (t) is 1 μm. The values of the other

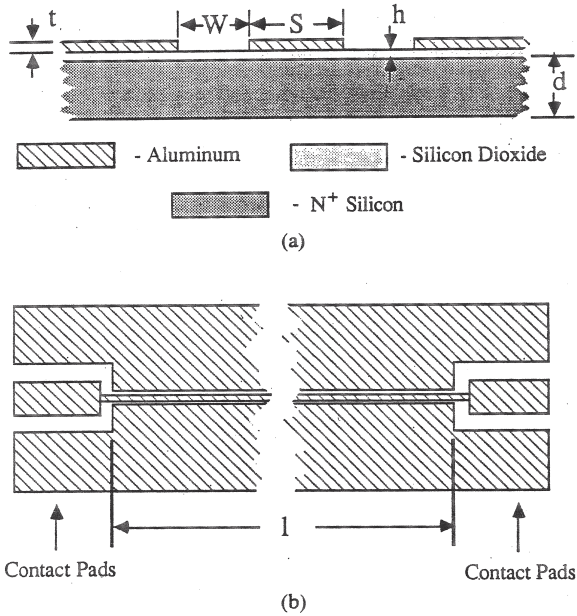

***Figure 1.4.1** (a) Cross-sectional view and (b) plan view of micron-size coplanar MIS transmission lines [1.63]. (© 1986 IEEE)*

***Table 1.4.1** Dimensions (S, W, H) and capacitance scaling factor (K) of the experimental lines [53] (© 1987 IEEE)*

Line	S	W	h	K
1	4.2	6.0	0.53	1.3
2	4.2	14.0	0.53	1.3
3	8.7	9.5	0.28	1.1
4	4.7	13.5	0.28	1.2

All dimensions are in micrometers.

dimensions shown in Figure 1.4.1 and the capacitance scaling factor used later in this analysis for each of the four lines are listed in Table 1.4.1. Because of the low impedance of the N^+ semiconductor, most of the electrical energy is confined to the insulating layer immediately below the center conductor. However, because the semiconductor is a nonmagnetic material, the magnetic field freely penetrates the N^+ substrate. This separation of the electric and magnetic energies results in the slow-wave mode propagation.

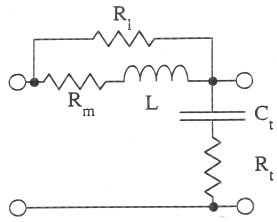

Figure 1.4.2 "Slow-wave" mode equivalent circuit of a micron-size coplanar MIS transmission line used in the quasi-TEM analysis [1.63]. (© 1986 IEEE)

For quasi-TEM propagation of the slow-wave mode of coplanar microstructure MIS transmission line, its equivalent circuit used in this analysis is shown in Figure 1.4.2. The inductance per unit length, L, is given by

$$L = \frac{1}{c^2 C_{\text{air}}} \tag{1.4.1}$$

where c is the phase velocity in vacuum and C_{air} is the capacitance per unit length of an equivalent air-filled transmission line. C_{air} can be determined by conformal mapping [54] leading to the following expression for L:

$$L = \frac{1}{4c^2 \varepsilon_0 F} \tag{1.4.2}$$

where ε_0 is the permittivity of free space and F is a geometrical factor given approximately by [54]

$$F = \frac{\ln\left[\dfrac{2(1+\sqrt{k})}{(1-\sqrt{k})}\right]}{\pi}; \quad 0.707 \le k \le 1$$

and

$$F = \frac{\pi}{\ln\left[\dfrac{2(1+\sqrt{k'})}{(1-\sqrt{k'})}\right]}; \quad 0 \le k \le 0.707 \tag{1.4.3}$$

with

$$k = \frac{S}{S+2W} \tag{1.4.4}$$

and

$$k' = \sqrt{1-k^2} \tag{1.4.5}$$

In Figure 1.4.2, the resistance R_m in series with L represents the correction due to the metal conductive losses. Its value in ohms per unit length is approximately equal to the effective resistance of the center conductor given by

$$R_m = \frac{1}{\sigma_m t S} \quad \text{for} \quad t \le \delta_m \tag{1.4.6}$$

and

$$R_m = \frac{1}{\sigma_m \delta_m S} \quad \text{for} \quad t \ge \delta_m$$

where σ_m and δ_m are the conductivity and skin depth of aluminum, respectively. The ground plane contribution to R_m can be ignored because the current densities in it are much smaller than those in the center conductor.

The resistance R_L is inserted in the equivalent circuit of Figure 1.4.2 to account for the loss caused by the longitudinal current flowing in the N^+ semiconductor parallel to the current in the center conductor. Since the longitudinal semiconductor current flows in addition to the longitudinal current in the metal, a parallel connection has been used. The value of R_L is given by

$$R_L = \frac{1}{\sigma_S \delta_S S} \tag{1.4.7}$$

where σ_s and δ_s are the conductivity and skin depth of the N^+ semiconductor, respectively. Equation (1.4.7) is based on the assumption that the longitudinal electric field under the center conductor decays exponentially in the vertical direction with decay constant δ_s.

To account for the energy storage and loss associated with the transverse electric field and current, the transverse capacitance C_t and transverse resistance R_t have been included in Figure 1.4.2. The transverse capacitance per unit length is given approximately by

$$C_t = \frac{\varepsilon_i \varepsilon_0 S K}{h} \tag{1.4.8}$$

where ε_i is the dielectric constant of SiO_2 and K is a geometrical factor listed in Table 1.4.1 introduced to account for the capacitance associated with the fringing fields. Equation (1.4.8) is based on the assumption

that most of the electric energy is stored in the dielectric layer under the center conductor. The value of the transverse resistance is given approximately by

$$R_t = \frac{1}{2\sigma_S F} \tag{1.4.9}$$

where F is the geometric factor given by Eqn. (1.4.3). In this analysis, we have ignored the finite transverse capacitance through the air because its susceptance is very small compared with that of C_t and R_t in series.

For a transmission line consisting of the circuit elements of Figure 1.4.2, the complex propagation constant γ and the complex characteristic impedance Z_0 are given by

$$\gamma = \alpha + j\beta = \sqrt{ZY} \tag{1.4.10}$$

$$Z_0 = Z'_0 + jZ''_0 = \sqrt{\frac{Z}{Y}} \tag{1.4.11}$$

where

$$Z = \frac{1}{\frac{1}{R_L} + \frac{1}{R_m + j\omega L}} \tag{1.4.12}$$

$$Y = \frac{1}{R_t + \frac{1}{j\omega C_t}} \tag{1.4.13}$$

and the quality factor Q and the "slowing factor" λ_0/λ_g are given by

$$Q = \frac{\beta}{2\alpha} \tag{1.4.14}$$

$$\frac{\lambda_0}{\lambda_g} = \frac{\beta}{\omega\sqrt{\mu_0\varepsilon_0}} \tag{1.4.15}$$

The quasi-TEM mode analysis presented above is valid only at frequencies which satisfy both $f \ll f_1$ and $f \ll f_2$ where

$$f_1 = \frac{1}{\pi\sigma_S\mu_0\left(W + \frac{S}{2}\right)^2} \tag{1.4.16}$$

and

$$f_2 = \frac{\sigma_S}{2\pi\varepsilon_0\varepsilon_S} \tag{1.4.17}$$

The contours of constant Q for the transmission line 2 are shown in Figure 1.4.3. This figure shows that, at frequencies satisfying f « f_1 and f « f_2, the mode of propagation is the "slow-wave" mode because, in this region, the magnetic field freely penetrates the substrate while the electric field does not. When $f_2 < f < f_1$, both transverse electric and magnetic fields freely penetrate the semiconductor substrate and the "dielectric quasi-TEM" is the mode of propagation. On the other hand, when $f_1 < f < f_2$, neither field penetrates the substrate and the mode of propagation is the "skin-effect mode." Using worst-case parameters for the four transmission lines studied here, we can determine that f_1 = 120 GHz and f_2 = 12,000 GHz. Therefore, all four lines satisfy the criteria for the "slow-wave" mode propagation and for validity of the quasi-TEM analysis.

Comparison with Experimental Results

The experimental results presented below are obtained by measuring the S-parameters over the frequency range 1.0 GHz to 12.4 GHz [53]. The attenuations of the four lines versus frequency are shown in

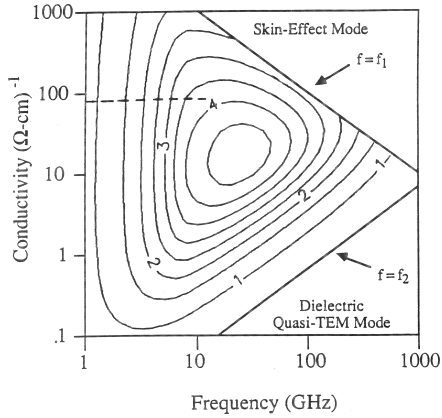

Figure 1.4.3 Contours of constant Q for the transmission line 2. Dashed line corresponds to the experiment parameters [1.63]. (© 1986 IEEE)

Figure 1.4.4(a–d). Solid lines represent theoretical values obtained from the quasi-TEM analysis presented above. The real (Z'_0) and imaginary (Z''_0) parts of the characteristic impedance as functions of frequency for the four lines are shown in Figure 1.4.5(a–d). It can be seen that the characteristic impedances of all four lines are nearly real, of the order of 50 Ω, and almost independent of frequency. The dependences of the "slowing factors" (λ_0/λ_g) on frequency for the four lines are shown in Figure 1.4.6(a–d) which also displays the quality factor Q versus frequency. It can be seen that each of the four quality factors increases with frequency reaching values in the range 3.6 to 4.3 at 12.4 GHz.

It is obvious that there is excellent agreement between theory and experiments over the full frequency range from 1.0 to 12.4 GHz for all four transmission lines. It can be concluded from this close agreement

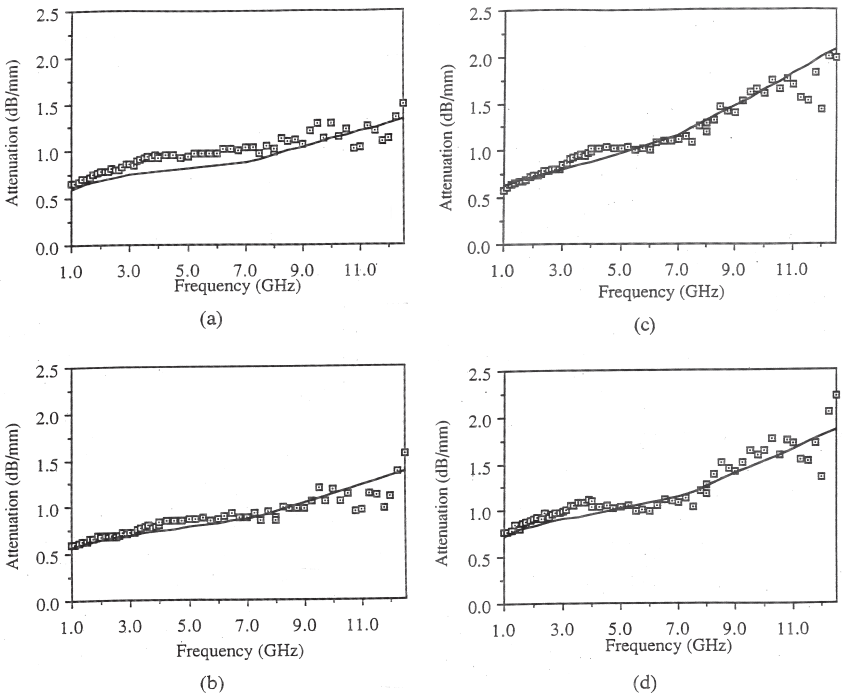

Figure 1.4.4 Dependence of attenuation on frequency for (a) line 1, (b) line 2, (c) line 3, and (d) line 4. Solid lines represent theoretical values obtained from the quasi-TEM analysis. Symbols are experimental values [1.63]. (© 1986 IEEE)

that the "slow-wave" mode propagating on these micron-size MIS transmission lines is, in fact, a quasi-TEM mode and can therefore be analyzed by elementary techniques.

In this analysis, we have included three loss mechanisms namely the metal loss, longitudinal semiconductor loss, and the transverse semiconductor loss. It can be shown that the relative contribution of each loss mechanism in the above model can be approximately (within 1 percent) calculated by keeping the corresponding resistance in the circuit of Figure 1.4.2 while setting the other two resistances to zero each. The results for the transmission line 2 are shown in Figure 1.4.7. It can be seen that the metal loss contribution is dominant at frequencies below 25 GHz and decreases with increasing frequency though, even at 100 GHz, it

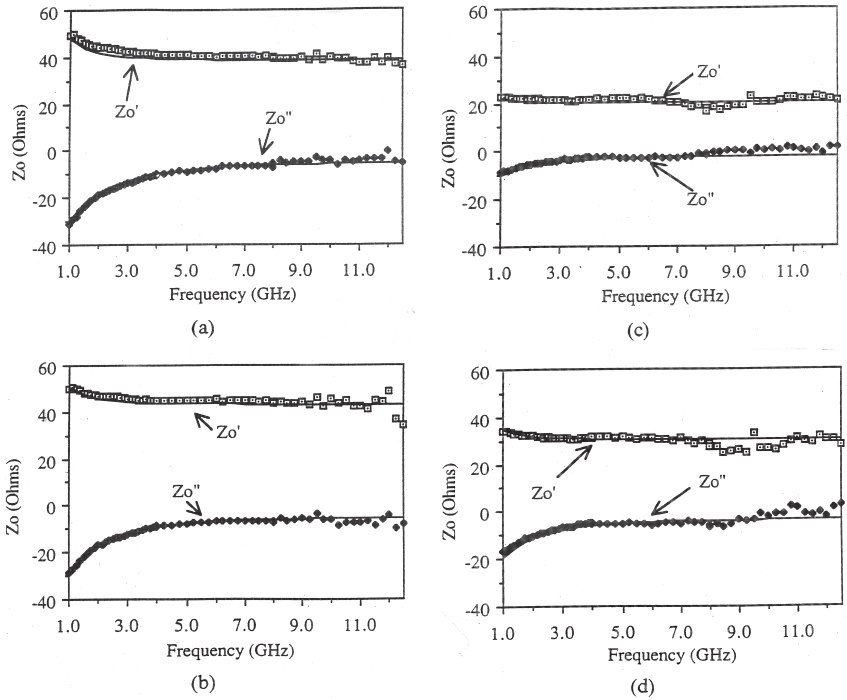

Figure 1.4.5 Dependence of real and imaginary parts of characteristic impedance on frequency for (a) line 1, (b) line 2, (c) line 3, and (d) line 4. Solid lines represent theoretical values obtained from the quasi-TEM analysis. Symbols are experimental values [1.63]. (© 1986 IEEE)

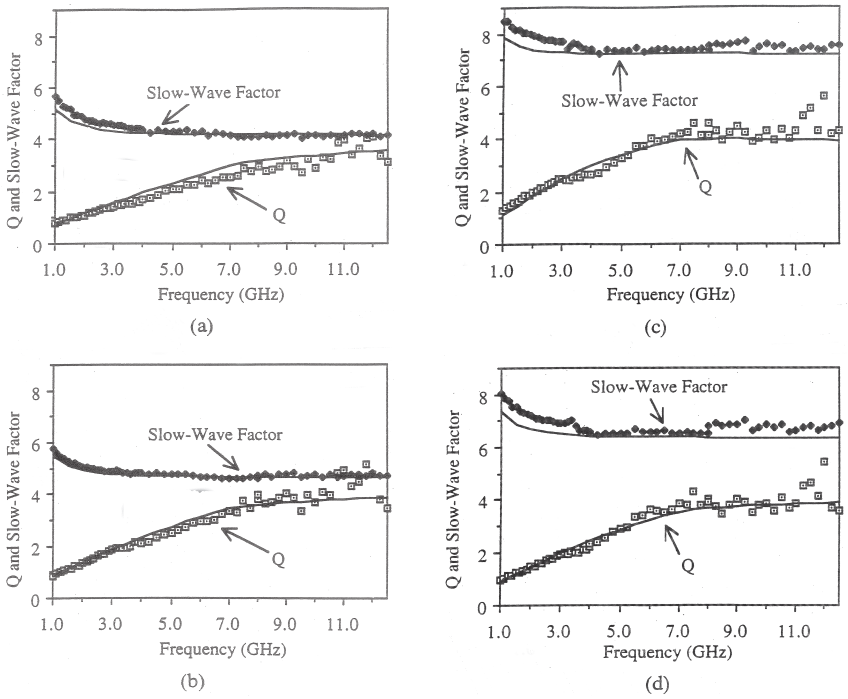

Figure 1.4.6 Dependence of quality and slow-wave factors on frequency for (a) line 1, (b) line 2, (c) line 3, and (d) line 4. Solid lines represent theoretical values obtained from the quasi-TEM analysis. Symbols are experimental values [1.63]. (© 1986 IEEE)

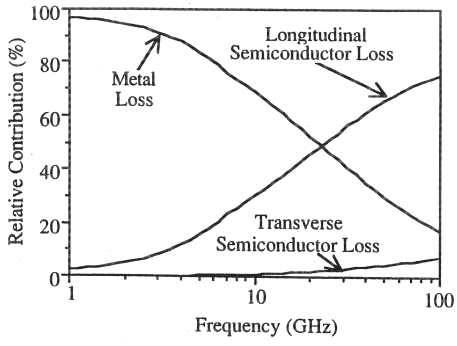

Figure 1.4.7 Relative contributions of the three loss mechanisms for transmission line 2 [1.63]. (© 1986 IEEE)

accounts for nearly 20 percent of the total loss. It can also be noted that both the transverse and the longitudinal semiconductor losses increase with frequency though the transverse loss component is very small.

1.5 Propagation Delays

In the literature, three measures of propagation delays in an electric circuit are defined [55]. These are:

Delay Time: It is defined as the time required by the output signal (current or voltage) to reach 50 percent of its steady state value.

Rise Time: It is defined as the time required by the output signal (current or voltage) to rise from 10 to 90 percent of its steady state value.

Propagation Time: It is defined as the time required by the output signal (current or voltage) to reach 90 percent of its steady state value.

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CHAPTER 2

Modeling of Interconnection Resistances, Capacitances, and Inductances

An electrical interconnection is characterized by three parameters: Resistance, capacitance, and inductance [1–40]. Series resistance is an important parameter and can be rather easily determined by the material properties and dimensions of the interconnection. On the other hand, the modeling of capacitances and inductances associated with the interconnections in the high-density environment on the high-speed integrated circuit (IC) is more complicated. Here are the chapter objectives:

- After going through section 2.1, students should be familiar with a few general considerations regarding interconnection resistances.
- After going through section 2.2, students should be familiar with certain unique factors that need to be considered for modeling the resistance of a copper interconnection.
- After going through section 2.3, students should be familiar with a few general considerations regarding interconnection capacitances.
- After going through section 2.4, students should be able to develop an algorithm to obtain the interconnection capacitances by the Green's function method which employs the method of moments in conjunction with a Green's function appropriate for the geometry of the interconnections. They will be able to calculate the Green's function by using the method of multiple images.

- After going through section 2.5, students should be able to calculate the Green's function by using the Fourier integral approach and to develop a numerical technique to determine the capacitances for a multilevel interconnection structure on the Si-SiO_2 structure.
- After going through section 2.6, students should be familiar with a few general considerations regarding interconnection inductances.
- After going through section 2.7, students should be familiar with a program called FastHenry that can be used for inductance extraction.
- After going through section 2.8, students will know that approximate equations for calculating the interconnection capacitances for a few standard structures are available.
- After going through section 2.9, students will be familiar with the approximate equations available for calculating the interconnection capacitances and inductances on oxide-passivated silicon and semi-insulating gallium arsenide substrates.

2.1 Interconnection Resistance

Resistance is a material property by which the metal resists the flow of current. It is fairly easy to predict or calculate the resistance of a material once its dimensions are known. The following formula is used for the calculation of resistance for a slab of any conducting material:

$$R = \rho\left(\frac{L}{W \cdot t}\right) = R_s\left(\frac{L}{W}\right) \tag{2.1.1}$$

where

L = Length of the slab
W = Width of the slab
t = Thickness of the slab, and
ρ = Resistivity of the slab's material

R_s is called the sheet resistance of the material and is measured in ohm per square. The sheet resistance of any metal is a function of its thickness and

the resistivity of the material. The material resistivity is a function of the chemical composition of the material and the density of impurities in that material. The process of resistance extraction may be a fairly simple task. With the prior knowledge of the interconnection layout of a circuit, any circuit simulator may be able to calculate the overall resistance with very little error. However, there are important considerations that need to be kept in mind for reducing and managing the on-chip resistances:

1. The use of copper interconnections will certainly complicate the resistance calculation process. This is because, as discussed in chapter 1 and shown in Figure 2.1.1, it is necessary for copper to have a shielding metal to prevent it from poisoning the silicon substrate. However, the shield material is not laid evenly as it is required to be thicker at some circuit locations such as at contacts and vias than at others. Accurate extraction must take this shield or seed layer into account.
2. When the frequency of operation is increased, metals display a phenomenon known as skin effect. Skin effect is a tendency for the alternating current to flow near the outer surface of a solid electrical conductor such as metal wire at frequencies above the audio range. The effect becomes more and more pronounced as the frequency is increased. The skin effect increases the effective resistance of a wire at moderate to high frequencies as shown in Figure 2.1.2. Skin effect becomes crucial only when the width and thickness of the conductor exceed twice the material's skin depth. The skin effect must be modeled into the resistance extraction tools for the high-frequency circuits.

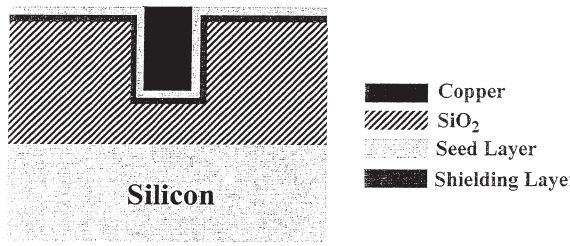

Figure 2.1.1 Shielding layer in the copper interconnection structure

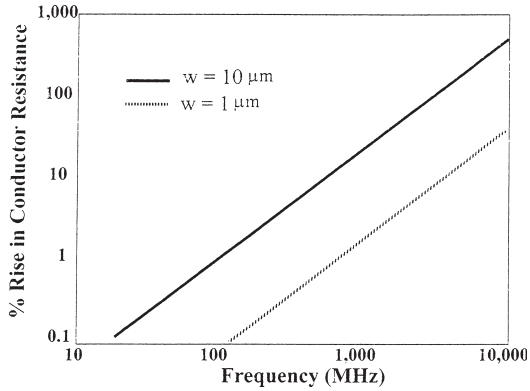

Figure 2.1.2 Approximate frequency dependence of the rise of the interconnection resistance due to skin effect

3. Full scaling, i.e., reducing all dimensions of an interconnection increases the metal's sheet resistance mainly due to the reduction in its thickness. The only solution for this is to try and use selective scaling or keep the thickness a constant. However, this makes the process of scaling more complex and would increase the fringe capacitances as well as the interwire capacitances. Another option would be to find materials with lower sheet resistance such as copper or some silicides.
4. The resistance of local interconnections grows linearly with the scaling factor. This is more so with the global interconnections which actually grow longer with the scaling process. One solution is to use multilevel interconnections which tend to reduce the wire lengths and allow straight connections between interconnections on two levels. Another important consideration is to use thicker and wider upper layers for global interconnections.
5. It is also necessary to reduce the contact resistances by avoiding the use of an excessive number of contacts and vias by making larger holes. Making holes tends to encourage current crowding around the perimeters of the holes.
6. The current densities at different points in an interconnection may be different due to a phenomenon called electromigration discussed in chapter 5. This phenomenon refers to the transport of metal

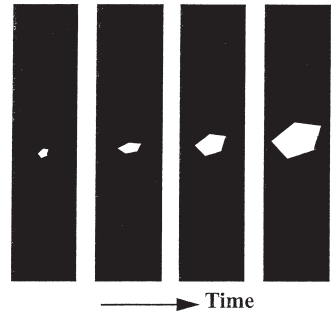

Figure 2.1.3 Growth of electromigration-induced void in an interconnection line with time

ions and molecules in a metal line due to a direct current running through it for long periods of time especially under high stress conditions such as high current densities and high temperature. Electromigration can cause the interconnection to break open or to short circuit with another neighboring interconnection. The formation of voids and hillocks due to electromigration can be observed using scanning electron microscopy of an interconnection line subjected to high currents for long periods of time. The growth of a void formed by electromigration in an interconnection line with time is shown schematically in Figure 2.1.3. The rate of electromigration in an interconnection depends on various material properties such as crystal structure in addition to the temperature and the current density. Overall, electromigration is the result of a vicious cycle in the sense that high current density speeds up the electromigration process which further increases the current density due to an effective decrease of the line width due to the formation of voids. This process also increases the overall resistance of the interconnection line.

2.2 Modeling of Resistance for a Copper Interconnection

The resistance of a relatively low frequency aluminum or another metallic interconnection of a regular shape can be determined from its dimensions (length and cross-sectional area) and the resistivity of its material.

The high-frequency effect on the resistance can be accounted for by incorporating the decrease of the effective cross section due to skin effect. However, a copper interconnection deserves a special treatment because of its unique fabrication. The effective resistivity of a copper interconnection is expected to increase due to scattering of the current carrying electrons from the interconnection surfaces and other grain boundaries [40]. Further, as the cross section of the copper interconnection is reduced, the area occupied by the highly resistive diffusion barrier around the copper line will no longer be negligibly small thereby increasing the effective resistance of the copper interconnection structure. Both the barrier effect and the surface scattering effect depend on the quality of the interface between copper and the diffusion barrier, profile of the barrier layer in the overall cross-sectional profile of the interconnection, minimum barrier thickness dictated by the reliability constraints, and the operating temperature of the interconnection line. The barrier profile is determined by the deposition technology employed for the interconnection fabrication such as atomic layer deposition (ALD), physical vapor deposition (PVD), collimated physical vapor deposition (CPVD), or ionized physical vapor deposition (IPVD).

As the interconnection dimensions are scaled down in the future, the adverse effects of diffusion barrier and surface scattering are likely to become more and more important. With reduction in the interconnection dimensions, the mean free path of electrons in the bulk of the metal can become comparable to the wire dimensions resulting in significant scattering from the copper–barrier interface. Further, the reliability constraints will not permit the barrier layer to scale down as rapidly as the copper metal dimensions thereby increasing the relative effect of the high-resistance barrier material on the interconnection resistance. It is also expected that the operating temperature of the interconnection will go up due to self-heating because of increasing chip power density due to higher current densities combined with the use of low dielectric material dielectrics with poor heat dissipation. These effects are expected to be less dominant in aluminum than in copper and it is possible that the effective resistance of the copper interconnection may exceed that of a comparable aluminum interconnection in the near future.

Effect of Surface/Interface Scattering on Interconnection Resistivity

The effects of scattering of electrons from the interconnection surface and from the barrier interface on the resistivity have been modeled by the following equation [40]:

$$\rho_s = \rho_o \left[\frac{1}{1 - \frac{3(1-P)\lambda}{2d} \int_1^\infty \left(\frac{1}{x^3} - \frac{1}{x^5} \right) \left(\frac{1 - e^{-kx}}{1 - Pe^{-kx}} \right) dx} \right] \tag{2.2.1}$$

where

ρ_s = Surface scattering dependent resistivity;
ρ_o = Bulk resistivity at the operating temperature;
λ = Mean free path of electrons in the bulk of the film at the temperature of operation;
d = Smallest thickness of the metallic film;
$k = d/\lambda$ = Ratio of the smallest film thickness to the bulk mean free path;

and P is an empirical parameter signifying the fraction of electrons undergoing elastic collisions at the interface. $P = 0$ corresponds to diffuse scattering at the interface resulting in lower mobility of electrons, whereas $P = 1$ corresponds to elastic scattering resulting in no change in the mobility of electrons. Equation (2.2.1) indicates that the surface/interface scattering dependent resistivity ρ_s is always greater than the bulk resistivity ρ_o. It also indicates that for a smaller value of k, which corresponds to a smaller film thickness and/or a higher mean free path of electrons, the surface scattering dominates the resistivity. At higher operating temperatures when the mean free path of electrons is smaller, k will be larger resulting in a smaller ρ_s/ρ_o ratio though the bulk resistivity ρ_o itself is higher at higher temperatures. It is interesting to note that the effect of surface scattering will be more pronounced in a copper interconnection than that in an aluminum interconnection. This is because copper has a lower intrinsic resistivity and a higher mean free path of electrons resulting in smaller values of the parameter k.

Effect of Diffusion Barrier on Interconnection Resistivity

The presence of the required diffusion barrier around the copper interconnection has an adverse effect on the overall effective resistivity of the interconnection. (An aluminum interconnection does not require such a barrier and hence does not suffer from this effect.) The increased interconnection effective resistivity ρ_b due to the presence of the diffusion barrier can be found from the equation [40]:

$$\rho_b = \rho_o \left[\frac{1}{1 - \frac{A_b}{hw}} \right] \tag{2.2.2}$$

where

ρ_o = Bulk resistivity of the interconnection material, i.e., copper;
A_b = Cross-sectional area occupied by the barrier material;
w = Total width of the interconnection (including copper and the barrier layer); and
h = total thickness of the interconnection (including copper and the barrier layer).

The definitions of h and w are illustrated in Figure 2.2.1 for a conformal barrier and for a nonconformal barrier where the shaded area shows the area A_b occupied by the barrier layer.

Equation (2.2.2) is based on the assumption that there is no current flowing in the barrier layer. This is a reasonable assumption because

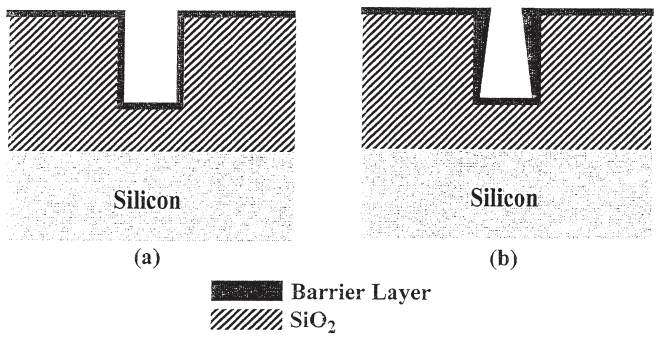

Figure 2.2.1 The barrier profiles of (a) a conformal barrier and (b) a non-conformal barrier [40]. (© 2002 IEEE)

the resistivity of the barrier material is of the order of a few hundred μΩ.cm, whereas the resistivity of copper is a few μΩ.cm. This equation shows that the effective resistivity of the interconnection increases as the barrier area A_b increases. This area depends on two factors: (a) The minimum barrier thickness required for stopping the copper diffusion into the substrate; and b) the barrier profile which is dictated by the barrier deposition technology. The barrier area is minimum when a conformal deposition technology such as ALD is employed, whereas a nonconformal deposition technology such as a PVD-based technology would require a thicker barrier at critical points resulting in a larger barrier area. It is expected that nonconformal barrier deposition technologies will become unsuitable as the interconnection dimensions are scaled down.

2.3 Interconnection Capacitances

The dynamic response of a chip is a strong function of the capacitances associated with the transistors and gates in the circuit and the parasitic resistances and capacitances associated with the interconnection lines present in the circuit layout. Until the recent past, the circuit delay was mostly due to the transistor design characteristics and for this reason, much effort has been put into the scaling of devices. At present, the propagation delays in an IC result primarily from the interconnection capacitances and the device and interconnection resistances. These are usually referred to as RC delays. An accurate model of the capacitances must include the contribution of the fringing fields as well as the shielding effects due to the presence of the neighboring conductors.

In the literature, several numerical techniques have been presented that can be used to characterize the interconnection lines though with limited applications. For example, the Schwarz–Christoffel conformal mapping technique [1] can be used to obtain exact results in terms of elliptic integrals for a symmetrical two-strip conductor; for more than two-strip conductors or for asymmetrical two-strip conductors, the method becomes very cumbersome and significant results cannot be obtained. The technique employing the Galerkin's method [2] in the spectral domain uses a Fourier series which becomes quite complicated

for mixed or inhomogenous dielectric multiconductor structures. The Green's function integral equation technique [3] is suitable for conductors of rectangular or annular shapes but becomes extremely difficult for irregular geometric shapes. The finite element method [4] and the finite difference method [5] involve determination of the charge distributions on the conductor surfaces and can be applied to several conductor geometries. The network analog method, evolved from the finite difference representation of partial differential equations [6], has been used for finite substrates in two dimensions [7], open substrates in three dimensions [8, 9], as well as for lossy, anisotropic and layered structures [10–14]. In the past, capacitance models have been developed for IC metallization wires [15–17] and the system of equations for infinite printed conductors has been solved [18–20]. There has also been reported work on systems of conductors with finite dimensions [21–27].

According to the semiconductor industry association's roadmap, the RC wiring delay will increase by over 90 percent from the 0.35 micron to the 0.l micron generation ICs. During the same time interval, gate delays are expected to drop from about 70 ps to about 20 ps while the clock period reduces by nearly 70 percent. As the interconnection is scaled with each technology generation, several trade-offs are made. In order to reduce the interconnection resistance and to improve its electromigration properties, the thickness of the metal is kept fairly constant, i.e., it is not scaled with its pitch. The increasing aspect ratio (thickness/width) results in larger coupling capacitances and more crosstalk among the interconnections (see chapter 4 for a discussion of crosstalk). This problem worsens as the number of interconnection levels is increased with almost every new generation.

It is obvious that interconnection capacitance characterization is an important aspect of current and future process development as well as circuit design. In order to give the circuit designers an accurate assessment of the speed and crosstalk issues, parasitic capacitances associated with the interconnections must be understood very well. In general, there are three types of capacitances observed in an interconnection layout and all of these are important to the overall capacitance extraction.

Parallel Plate Capacitance

It is known that most of the total interconnection capacitance is accounted for by the parallel plate capacitances though their relative contribution to the total capacitance decreases as the interconnection dimensions are scaled down. In silicon-based circuits, as shown in Figure 2.3.1, the interconnection layout usually forms a parallel plate structure with the underlying silicon substrate separated by a dielectric layer usually made of silicon dioxide and the parallel plate capacitance is given by:

$$C_{PP} = \varepsilon_{ox}\left(\frac{WL}{t_{ox}}\right) \tag{2.3.1}$$

where L and W are the length and width of the interconnection line, respectively whereas t_{ox} and ε_{ox} are the thickness and dielectric constant of the oxide layer, respectively. For circuits built on a resistive substrate such as GaAs (which is several thousand times more resistive than silicon), an oxide layer is not required and t_{ox} and ε_{ox} are replaced by the thickness and dielectric constant of the GaAs substrate itself.

Fringing Capacitances

For any parallel plate interconnection structure, there are always electric field lines that emerge from the edges of the interconnection to form the so-called fringing fields as shown in Figure 2.3.2. These fringing fields increase with the circumference and thickness of the interconnection line and add to the overall capacitance of an interconnection structure. Relative contribution of the fringing fields to the total interconnection capacitance increases as the interconnection dimensions are scaled down.

Figure 2.3.1 Electric field lines that result in parallel plate capacitance of an interconnection line on a silicon substrate (side view)

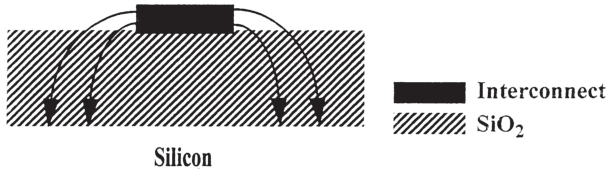

Figure 2.3.2 Fringing field lines of an interconnection line on a silicon substrate (side view)

Coupling Capacitances

In an interconnection layout consisting of two or more interconnections, there are capacitances that exist among the interconnections. These capacitances that exist between any pair of interconnections are called coupling or mutual capacitances. These coupling capacitances are the major cause of crosstalk among the interconnections due to which the signal integrity is severely distorted due to an increase in noise. An approximate closed form expression for calculating the coupling capacitances for a simple interconnection system shown in Figure 2.3.3 is given by

$$C_C = \left(\frac{\varepsilon_{ox}}{t_{di}}\right)(TL) \tag{2.3.3}$$

Even and Odd Mode Capacitances for Two Coupled Conductors

Two coupled conductors of different dimensions lying in the same plane at a distance d above the ground plane are shown in Figure 2.3.4. We are interested in finding the self and mutual (or coupling) capacitances for this system. In other words, we want to find the capacitances between each conductor and the ground (denoted by C_{11} and C_{22}) and the capacitance between the two conductors (denoted by C_{12}). To simplify the analysis, the problem can be split into the even and odd modes. In the even mode, each conductor is assumed to be at one volt potential with the same sign for each conductor. In the odd mode, the first conductor is assumed to be at a positive one volt potential while the second conductor is kept at a negative one volt potential. First, we will determine the even and odd mode capacitances for each conductor separately.

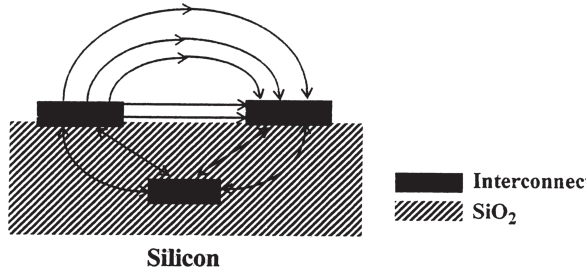

Figure 2.3.3 Electric field lines resulting in coupling capacitances among the interconnection lines on the same level or on different levels (side view)

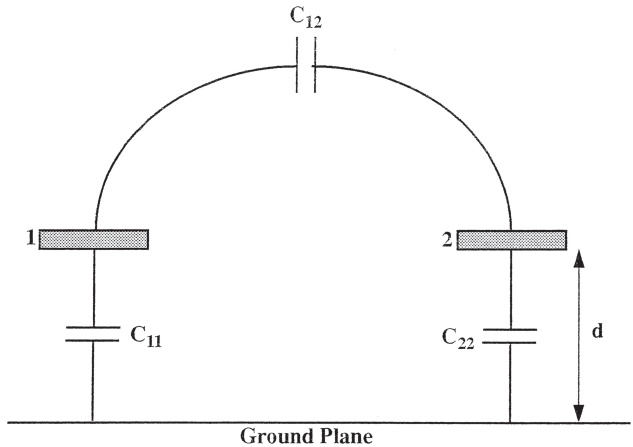

Figure 2.3.4 Two coupled conductors of different dimensions lying in the same plane at a distance d *above the ground plane*

In the even mode shown in Figure 2.3.5, there are no electric field lines at the center between the two conductors. Therefore, this plane can be treated as a magnetic wall which represents an open circuit to any mutual capacitance between the two conductors. Therefore, we can say that

$$C_1^{(e)} = C_{11} \tag{2.3.4}$$

and

$$C_2^{(e)} = C_{22} \tag{2.3.5}$$

where $C_1^{(e)}$ is the even mode capacitance for the first conductor while $C_2^{(e)}$ is that for the second conductor.

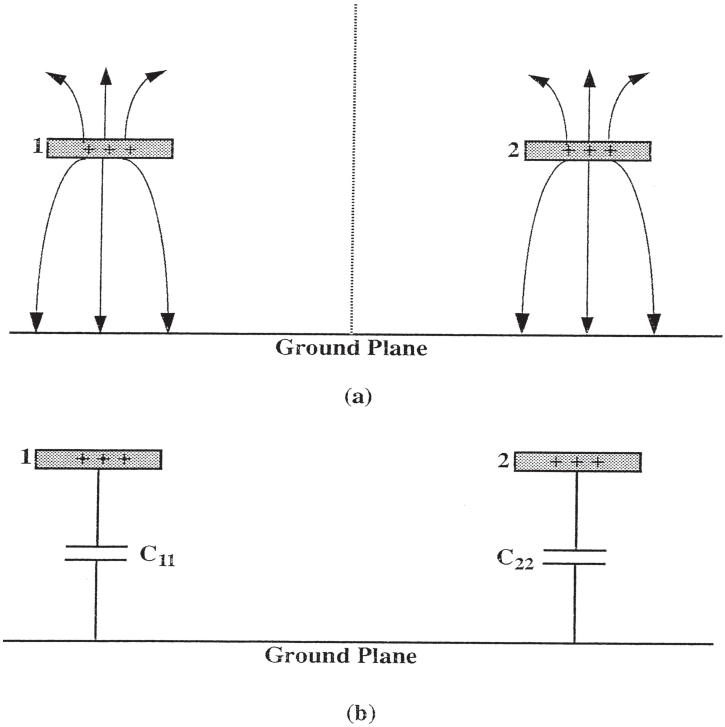

Figure 2.3.5 (a) Electric field lines for the two conductors in the even mode; (b) Equivalent circuit for the two conductors in the even mode

In the odd mode shown in Figure 2.3.6, the plane of symmetry between the two conductors can be treated as a grounded electric wall. This represents a short circuit to the mutual capacitance C_{12}. Therefore, in this case

$$C_1^{(o)} = C_{11} + 2C_{12} \tag{2.3.6}$$

and

$$C_2^{(o)} = C_{22} + 2C_{12} \tag{2.3.7}$$

where $C_1^{(o)}$ and $C_2^{(o)}$ are the odd mode capacitances for the first and second conductors, respectively. The mutual capacitance C_{12} can be expressed in terms of $C_1^{(o)}$ and $C_1^{(e)}$ by using equations (2.3.4) and (2.363) as

$$C_{12} = \frac{[C_1^{(o)} - C_1^{(e)}]}{2}$$

while the self-capacitances are given by equations (2.3.4) and (2.3.5).

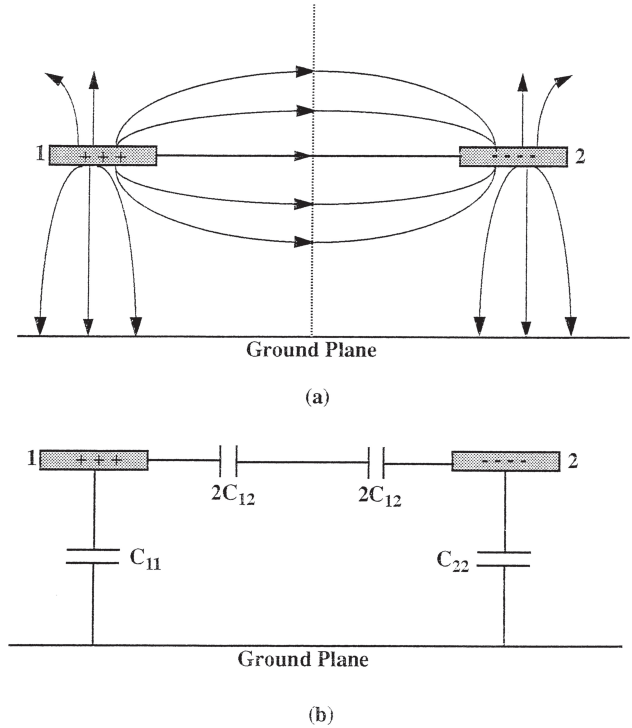

***Figure 2.3.6** (a) Electric field lines for the two conductors in the odd mode; (b) Equivalent circuit for the two conductors in the odd mode*

Even and Odd Mode Capacitances for Three Coupled Conductors

As in the case of two conductors, the three-conductor case can also be treated by splitting it into the even and odd modes. In the even mode, each conductor is again assumed to be at a positive one volt potential. In the odd mode, one conductor is kept at a positive one volt potential while the other two conductors are assumed to be at negative one volt potentials. This means that when finding the odd mode charge on the first conductor, e.g., the potentials on the second and third conductors are of the opposite sign to that on the first conductor. Figure 2.3.7 shows the self and mutual capacitances for the three conductors. These capacitances can be found in terms of the even and odd mode capacitances of the three conductors.

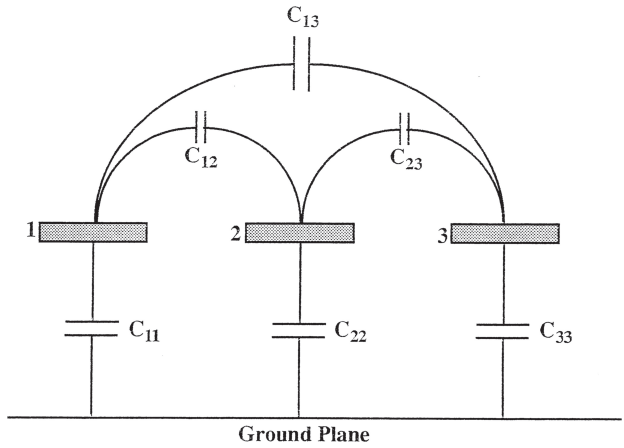

Figure 2.3.7 The self and mutual capacitances for the three conductors

In the even mode,

$$C_1^{(e)} = C_{11}$$
$$C_2^{(e)} = C_{22}$$

and

$$C_3^{(e)} = C_{33} \tag{2.3.8}$$

In the odd mode,

$$C_1^{(o)} = C_{11} + 2C_{12} + 2C_{13}$$
$$C_2^{(o)} = C_{22} + 2C_{12} + 2C_{23}$$

and

$$C_3^{(o)} = C_{33} + 2C_{13} + 2C_{23} \tag{2.3.9}$$

Solving these equations, we can find that the mutual capacitances are given by

$$C_{12} = \frac{[-C_1^{(e)} - C_2^{(e)} + C_3^{(e)} + C_1^{(o)} + C_2^{(o)} - C_3^{(o)}]}{4}$$

$$C_{13} = \frac{[-C_1^{(e)} + C_2^{(e)} - C_3^{(e)} + C_1^{(o)} - C_2^{(o)} + C_3^{(o)}]}{4}$$

$$C_{23} = \frac{[C_1^{(e)} - C_2^{(e)} - C_3^{(e)} - C_1^{(o)} + C_2^{(o)} + C_3^{(o)}]}{4} \tag{2.3.10}$$

The self-capacitances are given by Eqn. (2.3.8).

2.4 The Green's Function Method—Method of Images

Here, the parasitic capacitances for a system of closely spaced conducting interconnections lines printed on the GaAs substrate which in turn is placed on a conducting ground plane are determined by using the method of moments [34] in conjunction with a Green's function appropriate for the geometry of the interconnections. The Green's function is obtained by using the method of multiple images [3, 35]. It is assumed that the interconnections are of negligible thickness.

Green's Function Matrix for Interconnections Printed on the Substrate

The Green's function is a solution of a partial differential equation for a unit charge and with specified boundary conditions. To find the Green's function, the first step is to determine the potential due to the source charge everywhere in the region of interest. Now, the problem will be solved in two dimensions and then it will be extended to the three–dimensional (3D) case in the next subsection.

Consider the case of charged interconnections printed on a dielectric substrate which in turn is placed on a conducting ground plane as shown in Figure 2.4.1. Obviously, there are more than one interface and we need to consider the formation of image charges about the dielectric interface and about the ground plane by a process known as multiple imaging. Each image of the real charge also images across all other interfaces. For example, the real charge ρ will form an image across the dielectric interface as $[\rho(\varepsilon_1 - \varepsilon_2)/(\varepsilon_1 + \varepsilon_2)]$. This image will then form another image about the bottom ground plane as $[(-\rho)(\varepsilon_1 - \varepsilon_2)/(\varepsilon_1 + \varepsilon_2)]$. This new image will in turn image back across the dielectric interface with its magnitude changed by a factor of $[(\varepsilon_1 - \varepsilon_2)/(\varepsilon_1 + \varepsilon_2)]$, and so on. Also, the real charge will image about the bottom ground plane as $-\rho$. This image charge itself will image back across the dielectric interface modified by a factor of $[(\varepsilon_1 - \varepsilon_2)/(\varepsilon_1 + \varepsilon_2)]$. This process will continue till infinity and produce an infinite number of image charges.

For the two-dimensional (2D) case of a line charge ρ lying in a medium of dielectric constant ε_0 above a medium of dielectric constant ε

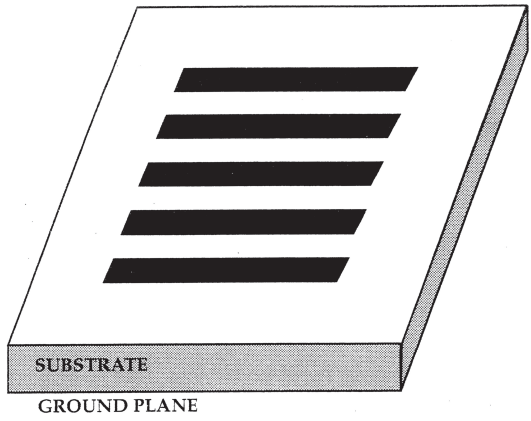

Figure 2.4.1 Schematic diagram of a few interconnections printed on top of the substrate which in turn is placed on a conducting ground plane

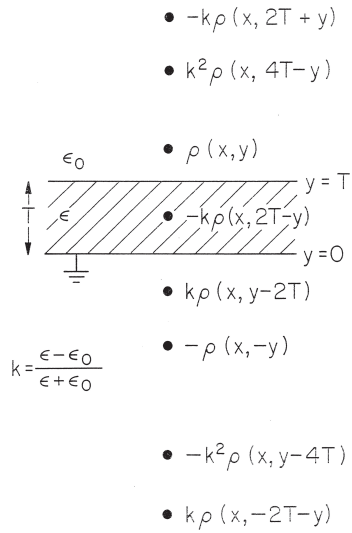

Figure 2.4.2 The magnitudes and locations of the images formed when a line charge ρ lies in a medium of dielectric constant ϵ_0 above a medium of dielectric constant ϵ with a conducting ground plane under it

with a conducting ground plane under it, the magnitudes and locations of a number of images are shown in Figure 2.4.2. First, the real charge reflects across the dielectric interface. Then both the real charge and this first image reflect across the ground plane changing in sign. These two

new images then reflect back across the dielectric interface changing by a factor of k where

$$k = \frac{(\varepsilon - \varepsilon_0)}{(\varepsilon + \varepsilon_0)}$$

and the process continues till infinity.

Now, the potential at any field point (x_i, y_i) due to a line charge ρ at the location (x_j, y_j) can be determined. In general, if r is the distance from the source charge to the field point, then

$$V(x_i, y_i) = -\frac{\rho}{4\pi\varepsilon_0} \ln(r^2)$$

However, the distance between the source charge and the field point will be different for each image, i.e., the potential due to the nth image is given by

$$V_n(x_i, y_i) = -\frac{\rho}{4\pi\varepsilon_0} \ln(r_n^2)$$

and the total potential at the field point is given by

$$V(x_i, y_i) = \sum_{n=1}^{\infty} V_n$$

Therefore, it follows from Figure 2.4.2 that for $y_i \geq T$ and $y_j \geq$ T

$$\begin{aligned} V(x_i, y_i) = \frac{\rho}{4\pi\varepsilon_0} \{ & -\ln[(x_i - x_j)^2 + (y_i - y_j)^2] \\ & + k \ln[(x_i - x_j)^2 + (y_i - y_j - 2T)^2] \\ & - k^2 \ln[(x_i - x_j)^2 + (y_i - y_j - 4T)^2] + \_\_\_\_\_ \\ & + k \ln[(x_i - x_j)^2 + (y_i + y_j - 2T)^2] \\ & - k^2 \ln[(x_i - x_j)^2 + (y_i + y_j - 4T)^2] \\ & + k^3 \ln[(x_i - x_j)^2 + (y_i + y_j - 6T)^2] + \_\_\_\_\_ \\ & - k \ln[(x_i - x_j)^2 + (y_i - y_j + 2T)^2] \\ & + k^2 \ln[(x_i - x_j)^2 + (y_i - y_j + 4T)^2] \end{aligned}$$

$$
\begin{aligned}
&- k^3 \ln[(x_i - x_j)^2 + (y_i - y_j + 6T)^2] \; + \\
&+ \ln[(x_i - x_j)^2 + (y_i + y_j)^2] \\
&- k \ln[(x_i - x_j)^2 + (y_i + y_j + 2T)^2] \\
&- k^2 \ln[(x_i - x_j)^2 + (y_i + y_j + 4T)^2] + \}
\end{aligned}
\tag{2.4.1}
$$

The Green's function $G(x_i, y_i; x_j, y_j)$ for the real charge at (x_j, y_j) and the field point at (x_i, y_i) can now be determined from Eqn. (2.4.1) by setting $\rho = 1$. Therefore

$$
\begin{aligned}
G(x_i, y_i; x_j, y_j) = \frac{1}{4\pi\varepsilon_0} \sum_{n=1}^{\infty} \{ & (-1)^n k^{n-1} \ln[(x_i - x_j)^2 \\
& + (y_i - y_j - 2(n-1)T)^2] \\
& + (-1)^{n+1} k^n \ln[(x_i - x_j)^2 + (y_i + y_j - 2nT)^2] \\
& - (-1)^{n+1} k^n \ln[(x_i - x_j)^2 + (y_i - y_j + 2nT)^2] \\
& - (-1)^n k^{n-1} \ln[(x_i - x_j)^2 \\
& + (y_i + y_j + 2(n-1)T)^2] \}
\end{aligned}
\tag{2.4.2}
$$

If all the interconnections are printed in the same plane on the substrate, then $y_i = y_j = T$. Then Eqn. (2.4.2) becomes

$$
\begin{aligned}
G(x_i, T; x_j, T) = \frac{1}{4\pi\varepsilon_0} \sum_{n=1}^{\infty} \{ & (-1)^n k^{n-1} \ln[(x_i - x_j)^2 + (2(n-1)T)^2] \\
& + (-1)^{n+1} k^n \ln[(x_i - x_j)^2 + (2(n-1)T)^2] \\
& - (-1)^{n+1} k^n \ln[(x_i - x_j)^2 + (2nT)^2] \\
& - (-1)^n k^{n-1} \ln[(x_i - x_j)^2 + (2nT)^2] \}
\end{aligned}
$$

or

$$G(x_i, T; x_j, T) = \frac{1}{4\pi\varepsilon_0} \sum_{n=1}^{\infty} \{((-1)^n k^{n-1}$$

$$+ (-1)^{n+1} k^n) \ln[(x_i - x_j)^2 + (2(n-1)T)^2]$$

$$- ((-1)^{n+1} k^n + (-1)^n k^{n-1}) \ln[(x_i - x_j)^2 + (2nT)^2]\}$$

or

$$G(x_i, T; x_j, T) = \left(-\frac{1}{4\pi\varepsilon_0}\right) \sum_{n=1}^{\infty} (1-k)((-1)^{n+1} k^{n-1})$$

$$\{\ln[(x_i - x_j)^2 + (2(n-1)T)^2]$$

$$- \ln[(x_i - x_j)^2 + (2nT)^2]\}$$

Since

$$1 - k = 1 - \frac{(\varepsilon - \varepsilon_0)}{(\varepsilon + \varepsilon_0)} = \frac{2\varepsilon_0}{(\varepsilon + \varepsilon_0)}$$

therefore

$$G(x_i, T; x_j, T) = \frac{1}{2\pi(\varepsilon + \varepsilon_0)} \sum_{n=1}^{\infty} ((-1)^{n+1} k^{n-1})$$

$$\{\ln[(x_i - x_j)^2 + (2nT)^2] - \ln[(x_i - x_j)^2 + (2(n-1)T)^2]\}$$

We can rewrite this expression for the 2D Green's function element as

$$G(x_i, T; x_j, T) = \sum_{n=1}^{\infty} A_n [g_{ijn1} - g_{ijn2}] \qquad (2.4.3)$$

where

$$A_n = \frac{1}{2\pi(\varepsilon + \varepsilon_0)} [(-1)^{n+1} k^{n-1}]$$

g_{ijn1} is the free space Green's function for the nth image at a distance of $y_j - y_i = 2nT$ from the field point and g_{ijn2} is the free space Green's function for the nth image at a distance of $y_j - y_i = 2(n-1)T$ from the field point.

Now, we can extend Eqn. (2.4.3) to the case when the charge is limited to a finite length and a finite width. First, we need to find the expression for the free space potential due to a charge in three dimensions. Consider a conductor on the surface of a dielectric which is divided into a large number of rectangular subsections. Consider a subsection of length Δx_j, width Δy_j and area Δs_j located at the source point (x_j, y_j, z_j). For this rectangular subsection in free space (i.e., without the dielectric present) the potential at a field point (x_i, y_i, z_i) can be determined by integration over the surface of the subsection, i.e., for a unit charge density,

$$V(x_i, y_i, z_i) = \frac{1}{4\pi\varepsilon_0} \int_{x_1}^{x_2}\int_{y_1}^{y_2} \frac{1}{[(x_i - x_j)^2 + (y_i - y_j)^2 + (z_i - z_j)^2]^{1/2}} dx\, dy$$

where

$$x_1 = x_j - \frac{\Delta x_j}{2}$$

$$y_1 = y_j - \frac{\Delta y_j}{2}$$

$$x_2 = x_j + \frac{\Delta x_j}{2}$$

$$y_2 = y_j + \frac{\Delta y_j}{2}$$

After the integration is performed, we get

$$V(x_i, y_i, z_i) = \frac{1}{4\pi\varepsilon_0}\left\{(x_j - x_i)\ln\left[\frac{(c + A_1)(d + B_1)}{(d + C_1)(c + D_1)}\right]\right.$$

$$\left. + \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d + B_1)(d + C_1)}{(c + D_1)(c + A_1)}\right]\right.$$

$$+ (y_j - y_i) \ln\left[\frac{(a + A_1)(b + B_1)}{(b + D_1)(a + C_1)}\right]$$

$$+ \left(\frac{\Delta y_j}{2}\right) \ln\left[\frac{(b + B_1)(b + D_1)}{(a + C_1)(a + A_1)}\right]$$

$$+ h\left[\operatorname{atan}\left(\frac{ac}{hA_1}\right) + \operatorname{atan}\left(\frac{bd}{hB_1}\right)\right]$$

$$+ h\left[\operatorname{atan}\left(\frac{ad}{hC_1}\right) + \operatorname{atan}\left(\frac{bc}{hD_1}\right)\right]\Bigg\} \qquad (2.4.4)$$

where

$$h = z_j - z_i$$

$$a = x_j - x_i - \frac{\Delta x_j}{2}$$

$$b = x_j - x_i + \frac{\Delta x_j}{2}$$

$$c = y_j - y_i - \frac{\Delta y_j}{2}$$

$$d = y_j - y_i + \frac{\Delta y_j}{2}$$

$$A_1 = \sqrt{(a^2 + c^2 + h^2)}$$

$$B_1 = \sqrt{(b^2 + d^2 + h^2)}$$

$$C_1 = \sqrt{(a^2 + d^2 + h^2)}$$

$$D_1 = \sqrt{(b^2 + c^2 + h^2)}$$

Extension of Eqn. (2.4.3) to the three dimensions is accomplished by multiplying this equation by $-4\pi\varepsilon_0$, by replacing the term g_{ijn1} by the free space Green's function for the nth image at a distance of $h = Z_j - Z_i = 2nT$

from the field point and by replacing the term g_{ijn2} by the free space Green's function for the nth image at a distance of $h = Z_j - Z_i = 2(n-1)T$ from the field point. The new expressions for g_{ijn1} and g_{ijn2} will become

$$\begin{aligned} g_{ijn1} = \frac{1}{4\pi\varepsilon_0}\Bigg\{ & (x_j - x_i)\ln\left[\frac{(c+A_2)(d+B_2)}{(d+C_2)(c+D_2)}\right] \\ & + \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d+B_2)(d+C_2)}{(c+D_2)(c+A_2)}\right] \\ & + (y_j - y_i)\ln\left[\frac{(a+A_2)(b+B_2)}{(b+D_2)(a+C_2)}\right] \\ & + \left(\frac{\Delta y_j}{2}\right)\ln\left[\frac{(b+B_2)(b+D_2)}{(a+C_2)(a+A_2)}\right] \\ & - 2nT\left[\operatorname{atan}\left(\frac{ac}{2nTA_2}\right) + \operatorname{atan}\left(\frac{bd}{2nTB_2}\right)\right] \\ & + 2nT\left[\operatorname{atan}\left(\frac{ad}{2nTC_2}\right) + \operatorname{atan}\left(\frac{bc}{2nTD_2}\right)\right]\Bigg\} \end{aligned} \qquad (2.4.5)$$

where

$$A_2 = \sqrt{(a^2 + c^2 + (2nT)^2)}$$

$$B_2 = \sqrt{(b^2 + d^2 + (2nT)^2)}$$

$$C_2 = \sqrt{(a^2 + d^2 + (2nT)^2)}$$

$$D_2 = \sqrt{(b^2 + c^2 + (2nT)^2)}$$

and

$$\begin{aligned} g_{ijn2} = \frac{1}{4\pi\varepsilon_0}\Bigg\{ & (x_j - x_i)\ln\left[\frac{(c+A_3)(d+B_3)}{(d+C_3)(c+D_3)}\right] \\ & + \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d+B_3)(d+C_3)}{(c+D_3)(c+A_3)}\right] \end{aligned}$$

$$+ (y_j - y_i)\ \ln\left[\frac{(a + A_3)(b + B_3)}{(b + D_3)(a + C_3)}\right]$$

$$+ \left(\frac{\Delta y_j}{2}\right)\ \ln\left[\frac{(b + B_3)(b + D_3)}{(a + C_3)(a + A_3)}\right]$$

$$- 2(n-1)T\left[\text{atan}\left(\frac{ac}{2(n-1)TA_3}\right) + \text{atan}\left(\frac{bd}{2(n-1)TB_3}\right)\right]$$

$$+ 2(n-1)T\left[\text{atan}\left(\frac{ad}{2(n-1)TC_3}\right) + \text{atan}\left(\frac{bc}{2(n-1)TD_3}\right)\right]\Bigg\} \tag{2.4.6}$$

where

$$A_3 = \sqrt{[a^2 + c^2 + (2(n-1)T)^2]}$$

$$B_3 = \sqrt{[b^2 + d^2 + (2(n-1)T)^2]}$$

$$C_3 = \sqrt{[a^2 + d^2 + (2(n-1)T)^2]}$$

$$D_3 = \sqrt{[b^2 + c^2 + (2(n-1)T)^2]}$$

Substituting for g_{ijn1} and g_{ijn2} from equations (2.4.5) and (2.4.6) in Eqn. (2.4.3) and multiplying by the factor $-4\pi\varepsilon_0$ and after simplifying, we get for the Green's function element in three dimensions:

$$G_{ij} = G(x_i, T; x_j, T)$$

$$= \frac{1}{2\pi(\varepsilon + \varepsilon_0)} \sum_{n=1}^{\infty} (-1)^{n+1} k^{n-1} (T_1 + T_2 + T_3 + T_4 - T_5 + T_6$$

$$+ T_7 - T_8) \tag{2.4.7}$$

where

$$T_1 = (x_j - x_i)\ln\left[\frac{(c+A_3)(d+B_3)(d+C_2)(c+D_2)}{(d+C_3)(c+D_3)(c+A_2)(d+B_2)}\right]$$

$$T_2 = \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d+B_3)(d+C_3)(c+D_2)(c+A_2)}{(c+D_3)(c+A_3)(d+B_2)(d+C_2)}\right]$$

$$T_3 = (y_j - y_i)\ln\left[\frac{(a+A_3)(b+B_3)(b+D_2)(a+C_2)}{(b+D_3)(a+C_3)(a+A_2)(b+B_2)}\right]$$

$$T_4 = \left(\frac{\Delta y_j}{2}\right)\ln\left[\frac{(b+B_3)(b+D_3)(a+C_2)(a+A_2)}{(a+C_3)(a+A_3)(b+B_2)(b+D_2)}\right]$$

$$T_5 = 2(n-1)T\left[\operatorname{atan}\left(\frac{ac}{2(n-1)TA_3}\right) + \operatorname{atan}\left(\frac{bd}{2(n-1)TB_3}\right)\right]$$

$$T_6 = 2(n-1)T\left[\operatorname{atan}\left(\frac{ad}{2(n-1)TC_3}\right) + \operatorname{atan}\left(\frac{bc}{2(n-1)TD_3}\right)\right]$$

$$T_7 = 2nT\left[\operatorname{atan}\left(\frac{ac}{2nTA_2}\right) + \operatorname{atan}\left(\frac{bd}{2nTB_2}\right)\right]$$

$$T_8 = 2nT\left[\operatorname{atan}\left(\frac{ad}{2nTC_2}\right) + \operatorname{atan}\left(\frac{bc}{2nTD_2}\right)\right]$$

and T is the substrate thickness.

Green's Function Matrix for Interconnections Embedded in the Substrate

If all the interconnections are embedded in the substrate then their heights above the bottom ground plane denoted by H will be less than the thickness of the substrate denoted by T. First, as in the previous subsection, the Green's function for a line charge ρ in two dimensions will be found by using the method of images and next, the expression for the Green's function will be extended to the 3D case. The results can be checked for accuracy by reducing them to the case when the interconnections are printed on the substrate by setting $H = T$ and ensuring that the resulting expression for the Green's function agrees with Eqn. (2.4.7).

First, we find the magnitudes and locations of the image charges when a real line charge ρ is placed at a height H ($H < T$) above the bottom ground plane. The real charge will first reflect up across the dielectric interface and give rise to an image charge equal to $k\rho$. This first image and the real charge will then both reflect across the ground plane changing in signs. These two new images will then reflect back across the dielectric interface and so on. The process will continue to infinity giving rise to the images as shown in Figure 2.4.3. To find the potential at a point (x_i, y_i)

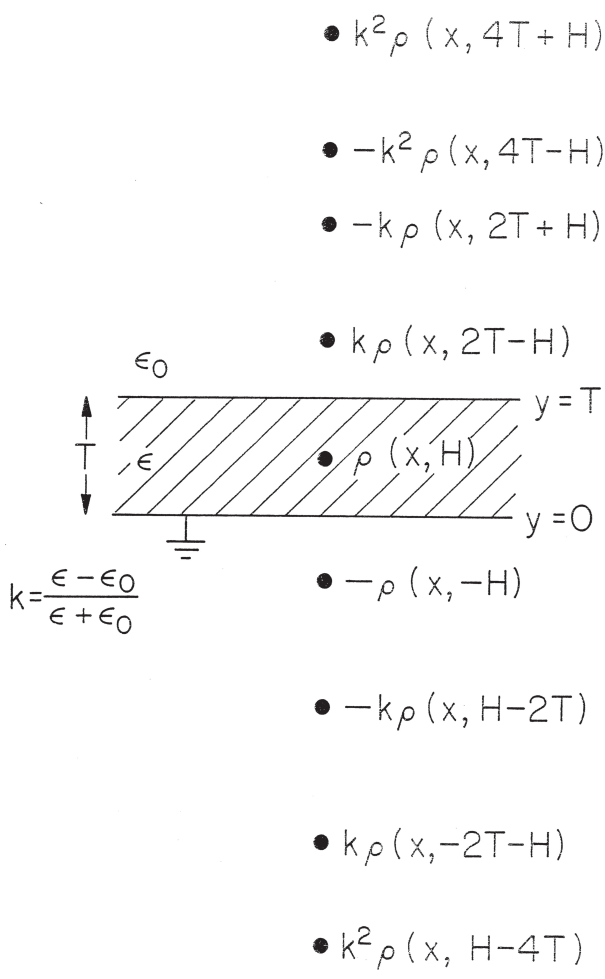

Figure 2.4.3 The magnitudes and locations of the images formed when a line charge ρ is embedded in a medium of dielectric constant . . . with a conducting ground plane under it and surrounded by another medium of dielectric constant ε_0.

inside the dielectric we need to find the sum of all the potentials at this point due to the real charge and all its image charges, i.e.,

$$V(x_i, y_i) = \sum_{n=1}^{\infty} V_n = \left(-\frac{\rho}{4\pi\varepsilon_0}\right) \ln(r_n^2)$$

where $\varepsilon = \varepsilon_0\varepsilon_r$. It follows from Figure 2.4.3 that for $y_i \leq T$ and $y_j \leq T$

$$\begin{aligned} V(x_i, y_i) = \frac{\rho}{4\pi\varepsilon}\{ & -\ln[(x_i - x_j)^2 + (y_i - H)^2] \\ & + k \ln[(x_i - x_j)^2 + (y_i - H - 2T)^2] \\ & + k^2 \ln[(x_i - x_j)^2 + (y_i - H - 4T)^2] + \_\_\_\_\_ \\ & - k \ln[(x_i - x_j)^2 + (y_i + H - 2T)^2] \\ & + k^2 \ln[(x_i - x_i)^2 + (y_i + H - 4T)^2] \\ & - k^3 \ln[(x_i - x_j)^2 + (y_i + H - 6T)^2] + \_\_\_\_\_ \\ & + \ln[(x_i - x_j)^2 + (y_i + H)^2] \\ & - k \ln[(x_i - x_j)^2 + (y_i + H + 2T)^2] \\ & + k^2 \ln[(x_i - x_j)^2 + (y_i + H + 4T)^2] + \_\_\_\_\_ \\ & + k \ln[(x_i - x_j)^2 + (y_i - H + 2T)^2] \\ & - k^2 \ln[(x_i - x_j)^2 + (y_i - H + 4T)^2] \\ & + k^3 \ln[(x_i - x_j)^2 + (y_i - H + 6T)^2] + \_\_\_\_\_ \} \end{aligned} \tag{2.4.8}$$

The Green's function $G(x_i, y_i; x_j, y_j)$ for the real charge at (x_j, y_j) and the field point at (x_i, y_i) can now be determined from Eqn. (2.4.8) by setting $\rho = 1$. Therefore

$$G(x_i, y_i; x_j, y_j) = \frac{1}{4\pi\varepsilon} \sum_{n=1}^{\infty} \{-(-1)^{n+1} k^{n-1} \ln[(x_i - x_j)^2 + (y_i - H - 2(n-1)T)^2]$$
$$+ (-1)^n k^n \ln[(x_i - x_j)^2 + (y_i + H - 2nT)^2]$$
$$- (-1)^n k^n \ln[(x_i - x_j)^2 + (y_i - H + 2nT)^2]$$
$$- (-1)^{n+1} k^{n-1} \ln[(x_i - x_j)^2 + (y_i + H + 2(n-1)T)^2]\} \quad (2.4.9)$$

If all the interconnections are in the same plane then $y_i = y_j = H$ and Eqn. (2.4.9) becomes

$$G(x_i, H; x_j, H) = \frac{1}{4\pi\varepsilon} \sum_{n=1}^{\infty} \{(-1)^n k^n \ln[(x_i - x_j)^2 + (2H - 2nT)^2]$$
$$- (-1)^n k^n \ln[(x_i - x_j)^2$$
$$+ (-1)^{n+1} k^{n-1} \ln[(x_i - x_j)^2 + \{2H + 2(n-1)T\}^2]$$
$$- (-1)^{n+1} k^{n-1} \ln[(x_i - x_j)^2 + \{2(n-1)T\}^2]\}$$

We can rewrite this expression for the 2D Green's function element as:

$$G(x_i, H; x_j, H) = \sum_{n=1}^{\infty} [A_n(g_{ijn1} - g_{ijn2}) + B_n(g_{ijn3} - g_{ijn4})] \quad (2.4.10)$$

where

$$A_n = (-1)^n k^n$$

and

$$B_n = (-1)^{n+1} k^{n-1}$$

g_{ijn1} is the free space Green's function for the *nth* image at a distance of $y_j - y_i = 2H - 2nT$ from the field point and g_{ijn2} is the free space Green's function for the nth image at a distance of $y_j - y_i = 2nT$ from the field

point, g_{ijn3} is the free space Green's function for the nth image at a distance of $y_j - y_i = 2\mathrm{H} + 2(n-1)T$ from the field point and g_{ijn4} is the free space Green's function for the nth image at a distance of $y_j - y_i = 2(n-1)T$ from the field point.

Extension of Eqn. (2.4.10) to the three dimensions is accomplished by replacing the term g_{ijn1} by the free space Green's function for the nth image at a distance of $h = z_j - z_j = 2H - 2nT$ from the field point by replacing the term g_{ijn2} by the free space Green's function for the nth image at a distance of $h = z_j - z_i = 2\mathrm{H}-2n\mathrm{T}$ from the field point, by replacing the term g_{ijn3} by the free space Green's function for the nth image at a distance of $h = z_j - z_i = -2(n-1)T$ from the field point and by replacing the term g_{ijn4} by the free space Green's function for the nth image at a distance of $h = z_j - z_i = -2(n-1)T$ from the field point. The new expressions for g_{ijn1}, g_{ijn2}, $g_{ijn3,}$ and g_{ijn4} become

$$
\begin{aligned}
g_{ijn1} = \frac{1}{4\pi\varepsilon}\Bigg\{ & (x_j - x_i)\ln\left[\frac{(c+A_4)(d+B_4)}{(d+C_4)(c+D_4)}\right] \\
& + \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d+B_4)(d+C_4)}{(c+D_4)(c+A_4)}\right] \\
& + (y_j - y_i)\ln\left[\frac{(a+A_4)(b+B_4)}{(b+D_4)(a+C_4)}\right] + \left(\frac{\Delta y_j}{2}\right)\ln\left[\frac{(b+B_4)(b+D_4)}{(a+C_4)(a+A_4)}\right] \\
& + (2H-2nT)\left[\operatorname{atan}\left(\frac{ac}{(2H-2nT)A_4}\right) + \operatorname{atan}\left(\frac{bd}{(2H-2nT)B_4}\right)\right] \\
& + (2H-2nT)\left[\operatorname{atan}\left(\frac{ad}{(2H-2nT)C_4}\right) + \operatorname{atan}\left(\frac{bc}{(2H-2nT)D_4}\right)\right]\Bigg\}
\end{aligned}
\tag{2.4.11}
$$

where

$$
\begin{aligned}
A_4 &= \sqrt{(a^2 + c^2 + (2H-2nT)^2)} \\
B_4 &= \sqrt{(b^2 + d^2 + (2H-2nT)^2)} \\
C_4 &= \sqrt{(a^2 + d^2 + (2H-2nT)^2)} \\
D_4 &= \sqrt{(b^2 + c^2 + (2H-2nT)^2)}
\end{aligned}
$$

$$g_{ijn2} = \frac{1}{4\pi\varepsilon}\left\{(x_j - x_i)\ \ln\left[\frac{(c+A_5)(d+B_5)}{(d+C_5)(c+D_5)}\right]\right.$$

$$+\left(\frac{\Delta x_j}{2}\right)\ \ln\left[\frac{(d+B_5)(d+C_5)}{(c+D_5)(c+A_5)}\right]$$

$$+(y_j - y_i)\ \ln\left[\frac{(a+A_5)(b+B_5)}{(b+D_5)(a+C_5)}\right]$$

$$+\left(\frac{\Delta y_j}{2}\right)\ \ln\left[\frac{(b+B_5)(b+D_5)}{(a+C_5)(a+A_5)}\right]$$

$$-2nT\left[\text{atan}\left(\frac{ac}{2nTA_5}\right) + \text{atan}\left(\frac{bd}{2nTB_5}\right)\right]$$

$$\left.+2nT\left[\text{atan}\left(\frac{ad}{2nTC_5}\right) + \text{atan}\left(\frac{bc}{2nTD_5}\right)\right]\right\} \quad (2.4.12)$$

where

$$A_5 = \sqrt{[a^2 + c^2 + (2nT)^2]}$$

$$B_5 = \sqrt{[b^2 + d^2 + (2nT)^2]}$$

$$C_5 = \sqrt{[a^2 + d^2 + (2nT)^2]}$$

$$D_5 = \sqrt{[b^2 + c^2 + (2nT)^2]}$$

$$g_{ijn3} = \frac{1}{4\pi\varepsilon}\left\{(x_j - x_i)\ \ln\left[\frac{(c+A_6)(d+B_6)}{(d+C_6)(c+D_6)}\right]\right.$$

$$+\left(\frac{\Delta x_j}{2}\right)\ \ln\left[\frac{(d+B_6)(d+C_6)}{(c+D_6)(c+A_6)}\right]$$

$$+(y_j - y_i)\ \ln\left[\frac{(a+A_6)(b+B_6)}{(b+D_6)(a+C_6)}\right]$$

$$+\left(\frac{\Delta y_j}{2}\right)\ln\left[\frac{(b+B_6)(b+D_6)}{(a+C_6)(a+A_6)}\right]$$

$$-(2H+2(n-1)T)\left[\operatorname{atan}\left(\frac{ac}{(2H+2(n-1)T)A_6}\right)\right.$$

$$\left.+\operatorname{atan}\left(\frac{bd}{(2H+2(n-1)T)B_6}\right)\right]$$

$$+(2H+2(n-1)T)\left[\operatorname{atan}\left(\frac{ad}{(2H+2(n-1)T)C_6}\right)\right.$$

$$\left.\left.+\operatorname{atan}\left(\frac{bc}{(2H+2(n-1)T)D_6}\right)\right]\right\} \qquad (2.4.13)$$

where

$$A_6 = \sqrt{[a^2+c^2+(2H+2(n-1)T)^2]}$$

$$B_6 = \sqrt{[b^2+d^2+(2H+2(n-1)T)^2]}$$

$$C_6 = \sqrt{[a^2+d^2+(2H+2(n-1)T)^2]}$$

$$D_6 = \sqrt{[b^2+c^2+(2H+2(n-1)T)^2]}$$

and

$$g_{ijn4} = \frac{1}{4\pi\varepsilon}\left\{(x_j-x_i)\ln\left[\frac{(c+A_7)(d+B_7)}{(d+C_7)(c+D_7)}\right]\right.$$

$$+\left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d+B_7)(d+C_7)}{(c+D_7)(c+A_7)}\right]$$

$$+(y_j-y_i)\ln\left[\frac{(a+A_7)(b+B_7)}{(b+D_7)(a+C_7)}\right]$$

$$\left.+\left(\frac{\Delta y_j}{2}\right)\ln\left[\frac{(b+B_7)(b+D_7)}{(a+C_7)(a+A_7)}\right]\right.$$

$$- 2(n-1)T\left[\operatorname{atan}\left(\frac{ac}{2(n-1)TA_7}\right) + \operatorname{atan}\left(\frac{bd}{2(n-1)TB_7}\right)\right]$$

$$+ 2(n-1)T\left[\operatorname{atan}\left(\frac{ad}{2(n-1)TC_7}\right) + \operatorname{atan}\left(\frac{bc}{2(n-1)TD_7}\right)\right]\Bigg\} \tag{2.4.14}$$

where

$$A_7 = \sqrt{[a^2 + c^2 + (2(n-1)T)^2]}$$

$$B_7 = \sqrt{[b^2 + d^2 + (2(n-1)T)^2]}$$

$$C_7 = \sqrt{[a^2 + d^2 + (2(n-1)T)^2]}$$

$$D_7 = \sqrt{[b^2 + c^2 + (2(n-1)T)^2]}$$

Substituting for g_{ijn1}, g_{ijn2}, g_{ijn3}, and g_{ijn4} from equations (2.4.11) to (2.4.14) in Eqn. (2.4.10) and after simplifying, we get for the Green's function element in three dimensions:

$$G_{ij} = G(x_i, H; x_j, H)$$

$$= \frac{1}{4\pi\varepsilon}\sum_{n=1}^{\infty}([-1]^{n-1}k^n[T_9 + T_{10} + T_{11} + T_{12} - T_{13} + T_{14} + T_{15} - T_{16}]$$

$$+ [-1]^n k^{n-1}[T_{17} + T_{18} + T_{19} + T_{20} - T_{21} + T_{22} + T_{23} - T_{24}]) \tag{2.4.7}$$

where

$$T_9 = (x_j - x_i)\ln\left[\frac{(c + A_4)(d + B_4)(d + C_5)(c + D_5)}{(d + C_4)(c + D_4)(c + A_5)(d + B_5)}\right]$$

$$T_{10} = \left(\frac{\Delta x_j}{2}\right)\ln\left[\frac{(d + B_4)(d + C_4)(c + D_5)(c + A_5)}{(c + D_4)(c + A_4)(d + B_5)(d + C_5)}\right]$$

$$T_{11} = (y_j - y_i)\ln\left[\frac{(a + A_4)(b + B_4)(b + D_5)(a + C_5)}{(b + D_4)(a + C_4)(a + A_5)(b + B_5)}\right]$$

$$T_{12} = \left(\frac{\Delta y_j}{2}\right) \ln\left[\frac{(b+B_4)(b+D_4)(a+C_5)(a+A_5)}{(a+C_4)(a+A_4)(b+B_5)(b+D_5)}\right]$$

$$T_{13} = (2H-2nT)\left[\operatorname{atan}\left(\frac{ac}{(2H-2nT)A_4}\right) + \operatorname{atan}\left(\frac{bd}{(2H-2nT)B_4}\right)\right]$$

$$T_{14} = (2H-2nT)\left[\operatorname{atan}\left(\frac{ad}{(2H-2nT)C_4}\right) + \operatorname{atan}\left(\frac{bc}{(2H-2nT)D_4}\right)\right]$$

$$T_{15} = 2nT\left[\operatorname{atan}\left(\frac{ac}{2nTA_5}\right) + \operatorname{atan}\left(\frac{bd}{2nTB_5}\right)\right]$$

$$T_{16} = 2nT\left[\operatorname{atan}\left(\frac{ad}{2nTC_5}\right) + \operatorname{atan}\left(\frac{bc}{2nTD_5}\right)\right]$$

$$T_{17} = (x_j - x_i) \ln\left[\frac{(c+A_6)(d+B_6)(d+C_7)(c+D_7)}{(d+C_6)(c+D_6)(c+A_7)(d+B_7)}\right]$$

$$T_{18} = \left(\frac{\Delta x_j}{2}\right) \ln\left[\frac{(d+B_6)(d+C_6)(c+D_7)(c+A_7)}{(c+D_6)(c+A_6)(d+B_7)(d+C_7)}\right]$$

$$T_{19} = (y_j - y_i) \ln\left[\frac{(a+A_6)(b+B_6)(b+D_7)(a+C_7)}{(b+D_6)(a+C_6)(a+A_7)(b+B_7)}\right]$$

$$T_{20} = \left(\frac{\Delta y_j}{2}\right) \ln\left[\frac{(b+B_6)(b+D_6)(a+C_7)(a+A_7)}{(a+C_6)(a+A_6)(b+B_7)(b+D_7)}\right]$$

$$T_{21} = (2H+2(n-1)T)\left[\operatorname{atan}\left(\frac{ac}{(2H+2(n-1)T)A_6}\right) + \operatorname{atan}\left(\frac{bd}{(2H+2(n-1)T)B_6}\right)\right]$$

$$T_{22} = (2H+2(n-1)T)\left[\operatorname{atan}\left(\frac{ad}{(2H+2(n-1)T)C_6}\right) + \operatorname{atan}\left(\frac{bc}{(2H+2(n-1)T)D_6}\right)\right]$$

$$T_{23} = 2(n-1)T\left[\operatorname{atan}\left(\frac{ac}{2(n-1)TA_7}\right) + \operatorname{atan}\left(\frac{bd}{2(n-1)TB_7}\right)\right]$$

$$T_{24} = 2(n-1)T\left[\operatorname{atan}\left(\frac{ad}{2(n-1)TC_7}\right) + \operatorname{atan}\left(\frac{bc}{2(n-1)TD_7}\right)\right]$$

Application of the Method of Moments

The algorithm presented below is suitable for a system of four interconnection lines and can be easily modified for a different number of lines. For a system of four conducting lines, the known potential V_i on the ith ($i = 1, 2, 3, 4$) conductor is related to the unknown surface charge density σ_j on each conductor by the following system of integral equations:

$$V_i = \sum_{j=1}^{4} \int_{S_j} G(x_i, y_i; x_j, y_j; z)\sigma_j(x_j, y_j)dx_j dy_j$$

where G is the Green's function and S_j is the area of the jth conductor. If the conductors are divided into a total of N subsections with areas ds_j then the potential V_i of the ith subsection is given by

$$V_i = \sum_{j=1}^{4} \sigma_j \, G_{ij}$$

where σ_j is now the unknown surface charge density of the jth subsection and G_{ij} is the element of the Green's function pertinent to the problem. If the subsections are made small enough so that the charge density can be assumed constant over the area of each subsection then the method of moments can be used to convert this equation into its matrix form

$$[V] = [\sigma_j][G]$$

Then, by matrix inversion, the unknown σ_j can be determined from

$$[\sigma_j] = [G]^{-1}[V]$$

where $[\sigma_j]$ and $[V]$ are two N-dimensional column matrices and $[G]$ is the N-dimensional square matrix. The total charge on the jth conductor is given by

$$Q_j = \sum_{j=1}^{N_j} \sigma_j \, ds_j; \quad j = 1, 2, 3, 4$$

where N_j is the number of subsections on the jth conductor.

Even and Odd Mode Capacitances

For the system of four interconnection lines, first, an even–odd mode excitation can be used to calculate the even and odd mode capacitances of each line separately. For the even mode excitation, each line is assumed to be +1 volt potential with respect to the conducting ground plane. For the odd mode excitation, one line is kept at +1 volt while the other three lines are kept at -1 volt potential. This means that when finding the odd mode charge on the first line, the potential on the first line is kept at $+1$ volt while the potentials on each of the second, third, and fourth lines are kept at –1 volt, and so on.

First, the four lines are divided into N_1, N_2, N_3, and N_4 number of subsections. Thus, the total number of subsections becomes

$$N = N_1 + N_2 + N_3 + N_4$$

Then, the voltage excitation for the even mode of each interconnection line is an N-row unit column matrix, i.e.,

$$[V]_{\text{even}} = \begin{bmatrix} 1 \\ \cdots \\ \cdots \\ 1 \\ 1 \\ \cdots \\ \cdots \\ 1 \\ 1 \\ \cdots \\ \cdots \\ 1 \\ 1 \\ \cdots \\ \cdots \\ 1 \end{bmatrix}$$

while the odd mode excitation for the first line is represented by the matrix

$$[V]_{\text{odd},1} = \begin{bmatrix} 1 \\ \cdots \\ \cdots \\ 1 \\ -1 \\ \cdots \\ \cdots \\ -1 \\ -1 \\ \cdots \\ \cdots \\ -1 \\ -1 \\ \cdots \\ \cdots \\ -1 \end{bmatrix}$$

and, similarly for $[V]_{\text{odd},2}$, $[V]_{\text{odd},3}$ and $[V]_{\text{odd},4}$.

If the inverse of the Green's function matrix is denoted by $[R]$ then we can define the following 16 quantities by summing the ijth elements in the 16 submatrices of the matrix $[R]$:

$$R_1 = \sum_{i=1}^{N_1} \sum_{j=1}^{N_1} R_{ij}$$

$$R_2 = \sum_{i=1}^{N_1} \sum_{j=N_1+1}^{N_1+N_2} R_{ij}$$

$$R_3 = \sum_{i=1}^{N_1} \sum_{j=N_1+N_2+1}^{N_1+N_2+N_3} R_{ij}$$

$$R_4 = \sum_{i=1}^{N_1} \sum_{j=N_1+N_2+N_3+1}^{N} R_{ij}$$

$$R_5 = \sum_{i=N_1+1}^{N_1+N_2} \sum_{j=1}^{N_1} R_{ij}$$

$$R_6 = \sum_{i=N_1+1}^{N_1+N_2} \sum_{j=N_1+1}^{N_1+N_2} R_{ij}$$

$$R_7 = \sum_{i=N_1+1}^{N_1+N_2} \sum_{j=N_1+N_2+1}^{N_1+N_2+N_3} R_{ij}$$

$$R_8 = \sum_{i=N_1+1}^{N_1+N_2} \sum_{j=N_1+N_2+N_3+1}^{N} R_{ij}$$

$$R_9 = \sum_{i=N_1+N_2+1}^{N_1+N_2+N_3} \sum_{j=1}^{N_1} R_{ij}$$

$$R_{10} = \sum_{i=N_1+N_2+1}^{N_1+N_2+N_3} \sum_{j=N_1+1}^{N_1+N_2} R_{ij}$$

$$R_{11} = \sum_{i=N_1+N_2+1}^{N_1+N_2+N_3} \sum_{j=N_1+N_2+1}^{N_1+N_2+N_3} R_{ij}$$

$$R_{12} = \sum_{i=N_1+N_2+1}^{N_1+N_2+N_3} \sum_{j=N_1+N_2+N_3+1}^{N} R_{ij}$$

$$R_{13} = \sum_{i=N-N_4+1}^{N} \sum_{j=1}^{N_1} R_{ij}$$

$$R_{14} = \sum_{i=N-N_4+1}^{N} \sum_{j=N_1+1}^{N_1+N_2} R_{ij}$$

$$R_{15} = \sum_{i=N-N_4+1}^{N} \sum_{j=N_1+N_2+1}^{N_1+N_2+N_3} R_{ij}$$

$$R_{16} = \sum_{i=N-N_4+1}^{N} \sum_{j=N-N_4+1}^{N} R_{ij}$$

The even and odd mode capacitances for each of the four lines were determined from the relations

$$C_j^{(e,o)} = \frac{Q_j^{(e,o)}}{V_j^{(e,o)}}; \quad j = 1, 2, 3, 4.$$

Since

$$[\sigma] = [G]^{-1}[V]$$

the even and odd mode capacitances for the four lines can be expressed as

$$C_1^e = (R_1 + R_2 + R_3 + R_4)\Delta s_1$$

$$C_2^e = (R_5 + R_6 + R_7 + R_8)\Delta s_2$$

$$C_3^e = (R_9 + R_{10} + R_{11} + R_{12})\Delta s_3$$

$$C_4^e = (R_{13} + R_{14} + R_{15} + R_{16})\Delta s_4$$

$$C_1^o = (R_1 - R_2 - R_3 - R_4)\Delta s_1$$

$$C_2^o = (R_6 - R_5 - R_7 - R_8)\Delta s_2$$

$$C_3^o = (R_{11} - R_9 - R_{10} - R_{12})\Delta s_3$$

$$C_4^o = (R_{16} - R_{13} - R_{14} - R_{15})\Delta s_4$$

Ground and Coupling Capacitances

The ground and coupling interconnection capacitances can be obtained by solving the following set of equations:

$$
\begin{aligned}
C_1^e &= C_{11} \\
C_2^e &= C_{22} \\
C_3^e &= C_{33} \\
C_4^e &= C_{44} \\
C_1^o &= C_{11} + 2C_{12} + 2C_{13} + 2C_{14} \\
C_2^o &= C_{22} + 2C_{12} + 2C_{23} + 2C_{24} \\
C_3^o &= C_{33} + 2C_{13} + 2C_{23} + 2C_{34} \\
C_4^o &= C_{44} + 2C_{14} + 2C_{24} + 2C_{34}
\end{aligned}
\qquad (2.4.15)
$$

Since the number of unknowns is greater than the number of equations, the Eqn. (2.4.15) cannot be solved exactly. One way is to use the method of unconstrained multivariable optimization to solve the equations.

Exercise 2.1

Consider a charge placed in air above a dielectric material of permittivity ε_1 which is deposited on another material of permittivity ε_2 which in turn is placed on a bottom ground plane.

a) Draw a diagram showing the image charges for this system.
b) Determine an expression for the Green's function matrix element G_{ij} for this system.

Exercise 2.2

Consider a charge embedded in a dielectric material of permittivity ε_1 which is deposited on another material of permittivity ε_2 which in turn is placed on a bottom ground plane.

a) Draw a diagram showing the image charges for this system;
b) Find the Green's function matrix element G_{ij} for this system.

2.5 The Green's Function Method—Fourier Integral Approach

The parasitic capacitances for a system of multilevel conducting interconnections can also be determined by the Green's function method obtained by the Fourier integral approach and by using a piecewise linear approximation for the charge density distributions [24] on the conducting interconnections. This method reduces the order of integration and the number of equations needed thereby reducing the computation time and the memory required. Here, the Green's function for the Si-SiO_2 system is derived by using the Fourier integral approach and the integral equations are solved for a multilevel interconnection structure using a piecewise linear approximation for the charge density distributions [24].

Green's Function for Multilevel Interconnections

A representation of three multilevel conducting interconnections in the Si-SiO_2 composite is shown in Figure 2.5.1. The solution of the Laplace equation governing the potentials on the conductors can be written as

$$\Phi(p) = \int_{all\ charge} G(p, q)\sigma(q)dq \qquad (2.5.1)$$

where $\sigma(q)$ is the charge density at point $q(x', y', z')$ in Figure 2.5.1 and $G(p, q)$ is the appropriate Green's function describing the potential induced at point $p(x, y, z)$ by a unit point charge at point $q(x', y', z')$. For a system of N conductors, the potential on the jth conductor is given by

$$\Phi_j(p) = \sum_{i=1}^{N} \int_{S_i} G(p, q)\sigma_i(q)ds_i(q); \quad j = 1, 2, \ldots\ldots, N \qquad (2.5.2)$$

where $\sigma_i(q)$ denotes the charge density on the surface S_i of the ith conductor.

The Green's function G(p, q) can be expressed as a Fourier integral [36] as

$$G(p, q) = \frac{1}{4\pi\varepsilon_1} \int_0^{\infty} J_0(m\rho)e^{-m|z_1|}dm \qquad (2.5.3)$$

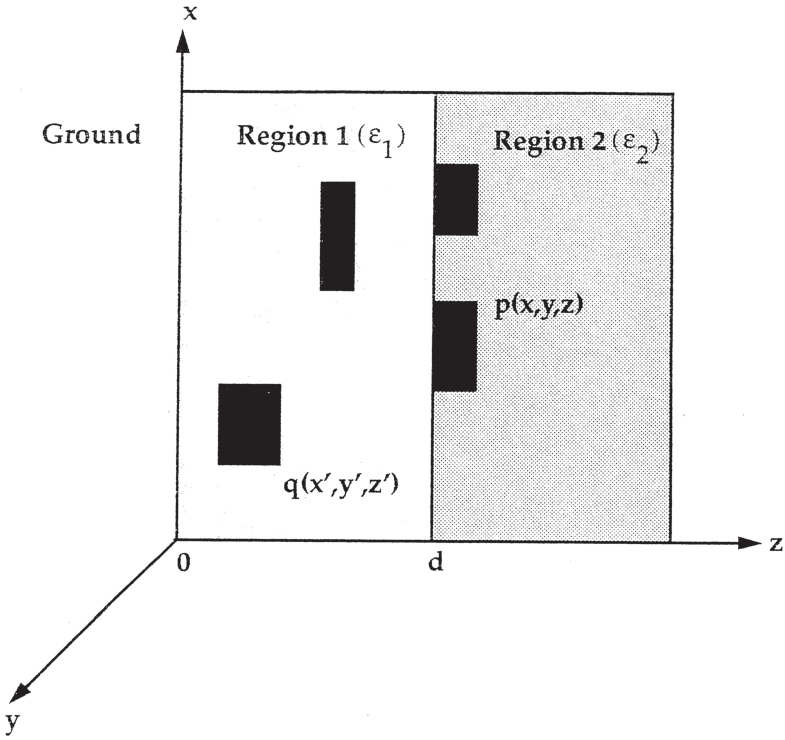

Figure 2.5.1 Representation of three multilevel interconnections in the Si-SiO_2 composite [24]. (© 1987 IEEE)

where ε_1 is the dielectric constant of SiO_2, J_0 is the Bessel function of first kind and zero order, m is the variable of integration, $z_1 = z - z'$, and

$$\rho = \sqrt{[(x-x')^2 + (y-y')^2]}$$

The Green's function in region 1 ($0 < z \leq d$) shown in Figure 2.5.1 can now be written as:

$$G_1(p, q) = \frac{1}{4\pi\varepsilon_1} \int_0^\infty J_0(m\rho)[e^{-m|z_1|} + \Theta_1(m)e^{mz_1} + \Theta_2(m)e^{-mz_1}]dm \tag{2.5.4}$$

and that in region 2 ($d \leq z < \infty$) is given by

$$G_2(p, q) = \frac{1}{4\pi\varepsilon_1} \int_0^\infty J_0(m\rho)[\Psi_1(m)e^{-mz_1} + \Psi_2(m)e^{mz_1}]dm \quad (2.5.5)$$

where the unknown functions Θ_1, Θ_2, Ψ_1 and Ψ_2 are determined by using the following boundary conditions

$$G_1(p, q) = G_2(p, q) \quad \text{at } z = d$$

$$\varepsilon_1 \frac{\partial G_1}{\partial z_1} = \varepsilon_2 \frac{\partial G_2}{\partial z_1} \quad \text{at } z = d$$

$$G_1(p, q) = 0 \quad \text{at } z = 0$$

$$G_2(p, q) = 0 \quad \text{at } z = \infty \quad (2.5.6)$$

to be given by

$$\begin{bmatrix} \Theta_1 \\ \Theta_2 \\ \Psi_1 \\ \Psi_2 \end{bmatrix} = \begin{bmatrix} \beta K(\alpha e^{2mz'} - 1) \\ (\beta K - 1)e^{-2mz'} - \beta K\alpha \\ \beta\gamma(\alpha - e^{-2mz'}) \\ 0 \end{bmatrix} \quad (2.5.7)$$

with

$$K = \frac{(\varepsilon_1 - \varepsilon_2)}{(\varepsilon_1 + \varepsilon_2)}$$

$$\alpha = e^{-m[(|d - z'|) - (d - z')]}$$

$$\beta = \frac{1}{K + e^{2md}}$$

$$\gamma = (1 + K)e^{2md}$$

Substituting Eqn. (2.5.7) into equations (2.5.4) and (2.5.5) and solving the resulting integrals, we can find that the Green's function for the case when the points p and q are both in region 1 is given by

$$G_{11}(p,q) = \left(\frac{1}{4\pi\varepsilon_1}\right)\left(\frac{1}{\sqrt{z_1^2+\rho^2}} - \frac{1}{\sqrt{(2z'+z_1)^2+\rho^2}} + \sum_{n=0}^{\infty}(-1)^n K^{(n+1)}\right.$$

$$\left[\frac{1}{\sqrt{[2(n+1)d-(2z'+z_1)]^2+\rho^2}} - \frac{1}{\sqrt{[2(n+1)d+z_1]^2+\rho^2}} + \right.$$

$$\left.\left.\frac{1}{\sqrt{[2(n+1)d+(2z'+z_1)]^2+\rho^2}} - \frac{1}{\sqrt{[2(n+1)d-z_1]^2+\rho^2}}\right]\right) \tag{2.5.8}$$

the Green's functions for the cases when the points p and q are located in different regions are given by

$$G_{12}(p,q) = \left(\frac{1}{4\pi\varepsilon_1}\right)\left(\frac{1}{\sqrt{z_1^2+\rho^2}} - \frac{1}{\sqrt{(2z'+z_1)^2+\rho^2}} + \sum_{n=0}^{\infty}(-1)^n K^{(n+1)}\right.$$

$$\left[\frac{1}{\sqrt{[2nd-z_1]^2+\rho^2}} - \frac{1}{\sqrt{[2nd+2z'+z_1]^2+\rho^2}} + \right.$$

$$\left.\left.\frac{1}{\sqrt{[2(n+1)d+2z'+z_1]^2+\rho^2}} - \frac{1}{\sqrt{[2(n+1)d-z_1]^2+\rho^2}}\right]\right) \tag{2.5.9}$$

$$G_{21}(p,q) = \left(\frac{1+K}{4\pi\varepsilon_1}\right)\left(\sum_{n=0}^{\infty}(-1)^n K^n \cdot\right.$$

$$\left.\left[\frac{1}{\sqrt{(2nd+z_1)^2+\rho^2}} - \frac{1}{\sqrt{[2nd+2z'+z_1]^2+\rho^2}}\right]\right) \tag{2.5.10}$$

and the Green's function for the case when the points p and q are both in region 2 is given by

$$G_{22}(p, q) = \left(\frac{1+K}{4\pi\varepsilon_1}\right)\left(\sum_{n=0}^{\infty}(-1)^n K^n \cdot \left[\frac{1}{\sqrt{[2(n-1)d + 2z' + z_1]^2 + \rho^2}} - \frac{1}{\sqrt{[2nd + 2z' + z_1]^2 + \rho^2}}\right]\right) \quad (2.5.11)$$

Multiconductor Interconnection Capacitances

For the three-conductor problem shown in Figure 2.5.2(a), the total charges Q_i ($i = 1, 2, 3$) on the three conductors are given in terms of the ground and coupling capacitances shown in Figure 2.5.2(b) and the potentials Φ_j ($j = 1, 2, 3$) of the three conductors by the equations:

$$\begin{aligned} Q_1 &= C_{11}\Phi_1 + C_{12}(\Phi_1 - \Phi_2) + C_{13}(\Phi_1 - \Phi_3) \\ Q_2 &= C_{21}(\Phi_2 - \Phi_1) + C_{22}\Phi_2 + C_{23}(\Phi_2 - \Phi_3) \\ Q_3 &= C_{31}(\Phi_3 - \Phi_1) + C_{32}(\Phi_3 - \Phi_2) + C_{33}\Phi_3 \end{aligned} \quad (2.5.12)$$

For a system of N conductors, the Eqn. (2.5.12) can be written as

$$Q_i = C_{ii}\Phi_i + \sum_{j=0}^{N} C_{ij}(\Phi_i - \Phi_j); \quad (i = 1, 2, \ldots\ldots, N) \quad (2.5.13)$$

which can be rewritten in terms of the short-circuit capacitances C_{sij} as

$$Q_i = \sum_{j=1}^{N} C_{sij}\Phi_j; \quad (i = 1, 2, \ldots\ldots, N) \quad (2.5.14)$$

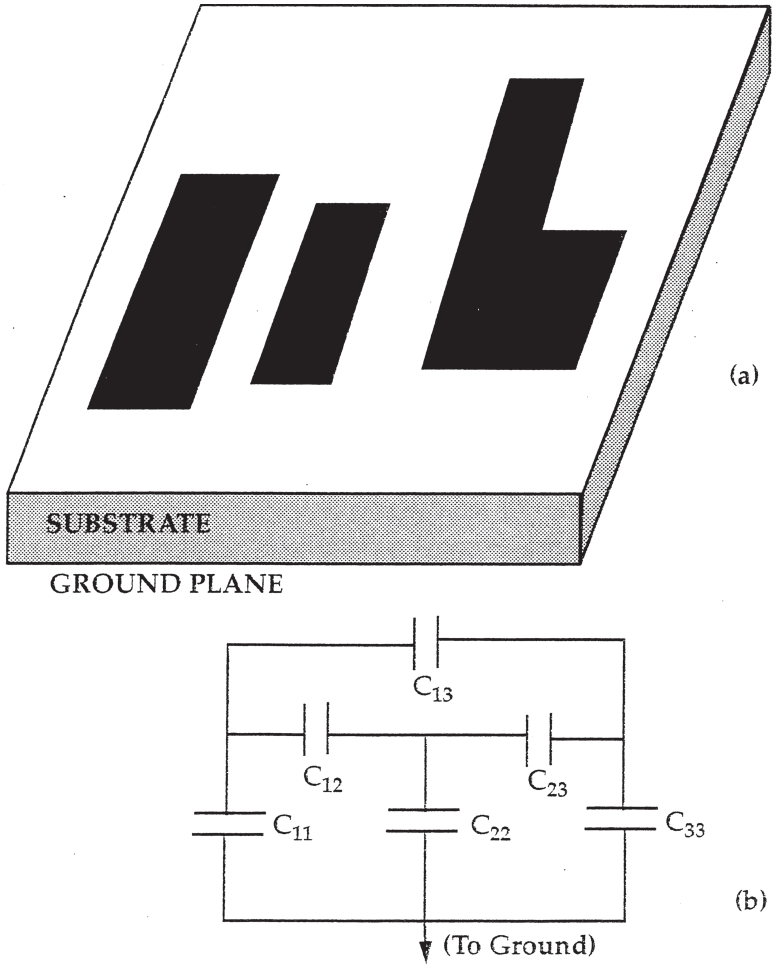

Figure 2.5.2 (a) Three finite interconnection metallization lines; (b) Equivalent circuit showing ground and coupling capacitances [24]. (© 1987 IEEE)

Comparing equations (2.5.13) and (2.5.14), the ground and coupling interconnection capacitances can be obtained from the short-circuit capacitances by using the relations

$$C_{ii} = \sum_{j=1}^{N} C_{sij}; \quad (i = 1, 2, ..., N) \quad (2.5.15)$$

$$C_{ij} = -C_{sij} \; ; \; i \neq j \quad (2.5.16)$$

which in turn require determination of the charge on each conductor for known values of the potentials Φ_j .

Piecewise Linear Charge Distribution Function

For a system of N conductors, each conductor is divided into a number of discreet elements as shown in Figure 2.5.3(a) and, on each of these elements, the charge density is approximately expressed by a linear combination of four piecewise linear functions. Thus, the charge density $\sigma(q)$ on the ith element is given by

$$\sigma_i(q) = \sum_{l=1}^{4} \alpha_{il} f_{il}(q) \tag{2.5.17}$$

where $f_{il}(q)$ is the lth of the four charge shape functions used to describe the charge distribution on the ith element and a_{il} are the unknown coefficients which need to be determined. If the ith conductor is divided into N_i elements then the total charge on this conductor is given by

$$Q_i = \sum_{j=1}^{N_i} \int_{mth\ element} \sigma_m(q) ds_m(q) \tag{2.5.18}$$

where

$$m = j + \sum_{k=2}^{i} N_{k-1}$$

For a single conductor having a rectangular cross section, the charge shape function is shown in Figure 2.5.3(b) and is given by

$$f_{qi2} = A(s - a_i) \quad ; \text{ for} \quad qi2 \le s < qi3$$

$$f_{qi2} = B(s - b_i) \quad ; \text{ for} \quad qi1 < s \le qi2$$

$$f_{qi2} = 0 \ ; \text{ for} \quad qi4 \le s \le qi1 \quad or \quad qi3 \le s \le qi4 \tag{2.5.19}$$

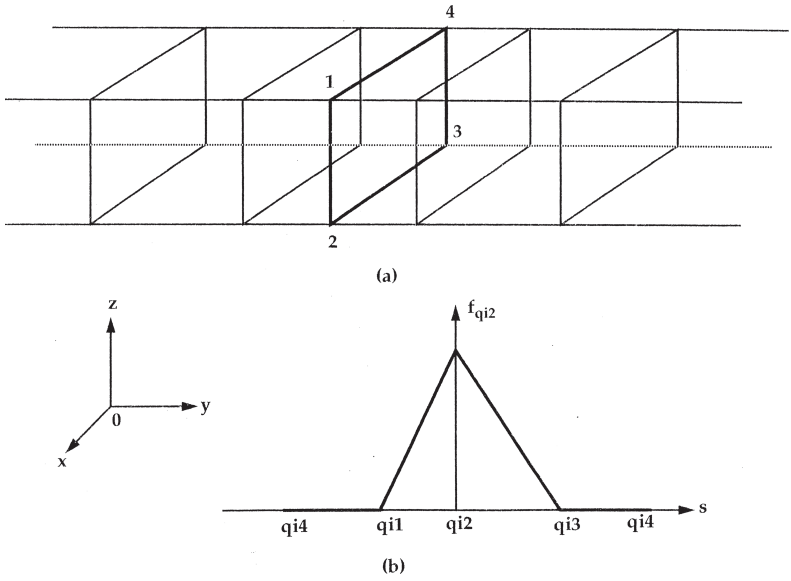

Figure 2.5.3 (a) Division of a conductor into discreet elements; (b) Shape of the piecewise linear charge function on each element [24]. (© 1987 IEEE)

where

$$A = -\frac{2}{w_i(w_i + t_i)}$$

$$B = -\frac{2}{t_i(w_i + t_i)}$$

$$a_i = s_{ix0} + w_i$$

$$b_i = s_{izo} + t_i$$

Calculation of Interconnection Capacitances

In order to determine the interconnection capacitances, we need to find the $4N$ unknown coefficients ($\alpha_{11}, \ldots, \alpha_{14}, \alpha_{21}, \ldots, \alpha_{N4}$). Substituting for charge density from Eqn. (2.5.17) in Eqn. (2.5.2), we get

$$\Phi_j(p) = \sum_{i=1}^{N} \sum_{l=1}^{4} \alpha_{il} F_{il}(p); \quad j = 1, 2, \ldots\ldots, N \qquad (2.5.20)$$

where

$$F_{il}(p) = \int_{ith\ element} G(p, q) f_{il}(q) ds_i(q) \qquad (2.5.21)$$

Following the Ritz–Rayleigh method [37], both sides of Eqn. (2.5.20) are projected onto the space spanned by the original charge shape functions. Using the following equations for the jth element:

$$(\Phi_j(p), f_{il}(p)) = 0 \quad \text{when} \quad i \neq j$$

and

$$(\Phi_j(p), f_{il}(p)) = \Phi_j \quad \text{when } i = j$$

we get from Eqn. (2.5.20)

$$\sum_{i=1}^{N} \sum_{l=1}^{4} \alpha_{il} P_{ijl} = (\Phi_j(p), f_{jl}(p)); \quad j = 1, 2, \ldots, N \qquad (2.5.22)$$

where

$$P_{ijl} = \int_{ith\ element} \int_{jth\ element} G(p, q) f_{jl}(p) f_{il}(q) ds_j(p) ds_i(q) \qquad (2.5.23)$$

Equation (2.5.22) can be written in matrix form as

$$[P][A] = [F][\Phi] \qquad (2.5.24)$$

where $A = (\alpha_{11}, \ldots, \alpha_{14}, \alpha_{21}, \ldots, \alpha_{N4})^T$ is the vector of $4N$ unknown coefficients, P is the $4N \times 4N$ matrix of the evaluated double integrals, $\Phi = (\Phi_1, \Phi_2, \ldots, \Phi_N)$ is the vector of N known potentials of the N conductors, and F is a $4N \times N$ incidence matrix of elements and conductors. Using any standard technique, the Eqn. (2.5.24) can be solved for the unknown coefficients. Then the charge densities can be obtained by using Eqn. (2.5.17) and the charges on each conductor can be found from Eqn. (2.5.18). Finally, the short-circuit capacitances required for the determination of the interconnection capacitances can be obtained by using equations (2.5.14) and (2.5.18) or can be found directly by using

$$C_s = [F]^T [P]^{-1} [F] \qquad (2.5.25)$$

2.6 Interconnection Inductances

The complementary metal-oxide semiconductor (CMOS) and other circuits consist of both active and passive devices. Active devices are the transistors while the passive devices are the interconnection structures that connect the transistors and gates in the circuit. These interconnections are mostly made of a metal such as aluminum and copper. In addition to its resistance, each interconnection has capacitances to the substrate and to the neighboring interconnections in the same level as well as to the interconnections in other levels. Furthermore, each interconnection also has self-inductance and mutual inductances caused by magnetic couplings of the interconnections.

Until a few years ago, the gate parasitics of the transistors were much larger than the interconnection parasitic impedances due to their relatively large sizes. The interconnection could be modeled as a short circuit and its impedance was ignored. Over the years, continuous scaling of the minimum gate feature sizes has increased the chip performance tremendously and reduced the cost of production. At the same time, it has reduced the gate capacitances making the interconnection capacitances more comparable. Furthermore, decreasing cross-sectional areas and increasing lengths of the interconnection wires have increased their resistances significantly. The design methodologies used to reduce the time delays on the chip have concentrated on reducing the RC time constants of the interconnection lines. More recently, this has been achieved fairly successfully by replacing aluminum with copper as the interconnection material to reduce the line resistance and breakthroughs in the use of ultra low-k dielectrics in the place of silicon dioxide have helped reduce the interconnection capacitance. So far, the on-chip inductances have largely been ignored in the interconnection models.

The present generation of ICs is designed for high clock frequencies with much faster signal rise/fall times. Considering the use of wider interconnections for power/ground buses and with faster rise times, the on-chip inductances can no longer be ignored [28–32]. These inductances lead to several undesirable effects such as increased ringing, increased crosstalk and worse power/ground bounce. In order to optimize the circuit performance, it is important to understand the dependences of these inductances on the various interconnection design parameters.

Self and Mutual Inductances

Each interconnection line has an associated self-inductance as well as a mutual inductance with respect to each of the surrounding interconnection lines. Both self and mutual inductances are loop quantities and can be determined only if the current loop is known exactly. The self-inductance of a loop is defined as the ratio of the magnetic flux passing through the loop to the value of the loop current. The mutual or the coupling inductance of a (victim) loop with respect to another (aggressor) loop is defined as the ratio of the magnetic flux passing through the victim loop caused by the current in the aggressor loop to the aggressor current. These magnetic fluxes that give rise to the self and mutual inductances are shown in Figure 2.6.1.

The magnetic interactions that take place among the current carrying conductors can be decomposed into three effects that take place concurrently:

a) Currents flowing through conductors create magnetic fields (Ampere' Law)
b) Time varying magnetic fields create induced electric fields (Faraday' Law)
c) Induced electric fields exert forces on the electrons in the conductors and cause electric voltage drops.

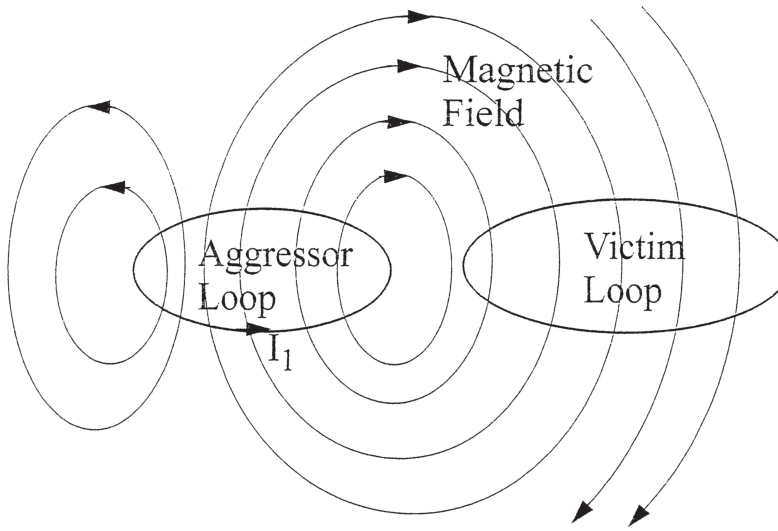

Figure 2.6.1 Magnetic fields that result in self and mutual inductances for two coupled loops

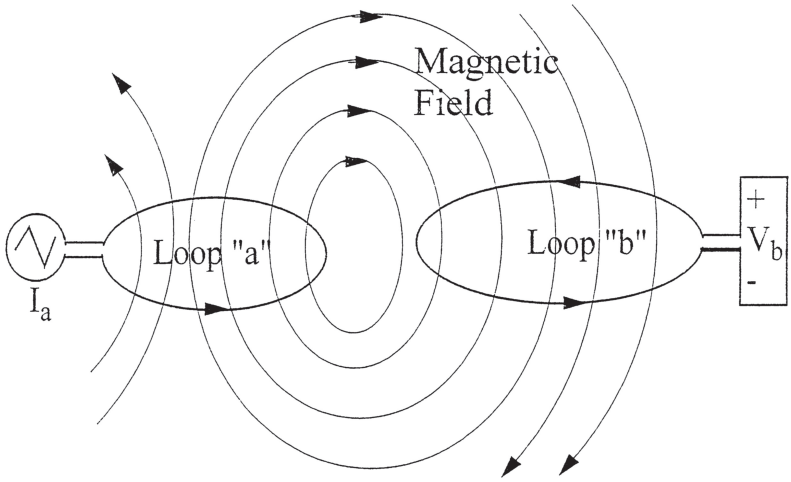

Figure 2.6.2 Voltage induced in loop "b" by the time-variant current in loop "a"

These three effects may be combined to state that a voltage drop is produced in the victim loop "b" due to a time-variant current flowing in a loop "a" as shown in Figure 2.6.2. It can be shown that the resulting induced voltage in loop "b" is given by

$$V_b = L_{ba}\left(\frac{dI_a}{dt}\right) \tag{2.6.1}$$

where L_{ba} is the mutual inductance between the loops "a" and "b" and I_a is the current flowing through the loop "a." For the special case where loops "a" and "b" are the same, the coefficient L_{aa} becomes the self-inductance of the loop "a."

Partial Inductances

Calculation of the loop inductances for large-scale ICs can prove to be cumbersome and uneconomical in several ways. Two most significant problems in the calculations are:

a) Need to know the current loops, i.e., the return paths of the currents a priori especially since these return paths have not been defined in the very-large-scale integration (VLSI) circuits
b) The fact that a current can take several return paths.

To overcome these problems, the concept of partial inductances was developed by Rosa and was introduced to the circuit modeling and analysis community by Ruehli. Since the actual current loops are not known, partial inductance is defined in terms of the magnetic flux created by the current of one aggressor segment through the virtual loop that the victim segment forms with infinity as shown in Figure 2.6.3. It can be shown that the total self and mutual loop inductances are equivalent to the sums of the partial self and mutual inductances of the segments that form all the loops in the system. In other words, the relationship between the loop and partial inductances is given by

$$L_{\text{ab, loop}} = \sum_i \sum_j s_{ij} L_{ij,\text{ partial}} \tag{2.6.2}$$

where i and j represent segments of loops "a" and "b" respectively. In Eqn. (2.6.2), the coefficient s_{ij} is -1 if one of the currents in segments i and j is flowing opposite to the direction assumed when the coupling partial inductance $L_{ij,\text{ partial}}$ was computed and is $+1$ otherwise. Thus by defining each current segment as forming its own return loop with infinity, partial inductances are used to represent the total loop interactions without prior knowledge of the actual current loops.

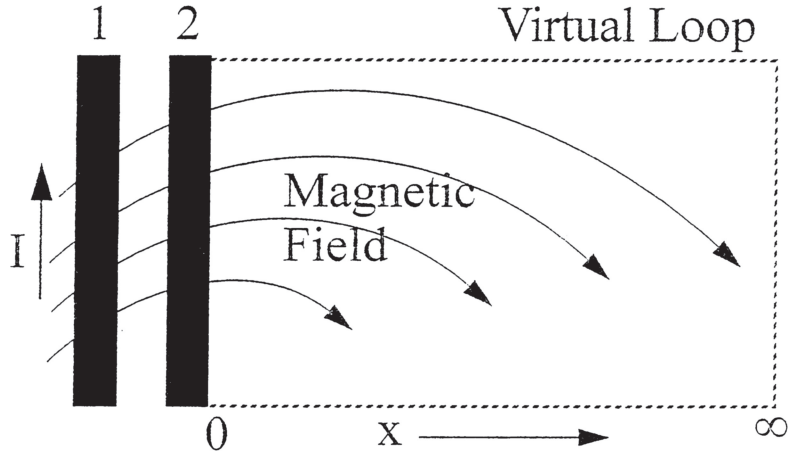

Figure 2.6.3 An illustration of partial inductances

Methods for Inductance Extraction

Over the years, several models have been developed to calculate the self and mutual inductances. All models make a trade-off between computational efficiency and accuracy and choose between specific 2D models versus the general 3D inductance models. Advocates of the 2D models insist that the return currents are equal and opposite to the interconnection currents and the inductances can therefore be extracted by using simpler 2D models which greatly limit the complexity of the problem by using several approximations and hence are more compute-efficient though less accurate. The users of the 2D models assert that the sensitivity of a signal waveform is rather low to errors in the inductance values particularly for the propagation delay and rise time analyses. It is claimed that the errors in propagation delay and rise times is below 9.4 percent and 5.9 percent, respectively, assuming a 30 percent relative error in the extracted inductance values and that this level of error may be acceptable when compared to the corresponding errors of 51 percent and 71 percent in propagation delay and rise times when using an RC model, i.e., without using the inductances at all.

On the other hand, the 3D model advocates claim that the return current paths in the ICs are fundamentally unknown and employ sophisticated analysis methods to cope with the increased complexity of these models which are more accurate though less compute-efficient. The biggest advantage of 3D modeling techniques lies in the fact that they provide a way to going around the need to know the current return paths a priori. 3D field solvers employ finite difference or finite element methods to the governing Maxwell's equations which represent one of the most elegant and concise ways to state the fundamentals of electricity and magnetism. Starting from the Maxwell's equations, one can develop the working relationships in terms of the electric and magnetic fields or the current density distributions in a complex IC interconnection layout. This approach generates a global 3D mesh for all parts of the interconnection structure and the surrounding space causing the number of unknowns to increase dramatically. There are many commercially available 3D field solvers for inductance extraction in the market. The exact analysis and extraction methods employed in these solvers may vary widely but the underlying principles are almost always based on the steps mentioned above.

Calculation of Inductance Matrix

The inductance matrix can be computed from the capacitance matrix for the corresponding 2D interconnection configuration (consisting of infinite length interconnections) in free space by the matrix inversion. The telegraphist's equations for the lossless case in the free space are

$$\frac{\partial V}{\partial x} = -L\frac{\partial I}{\partial t}$$

and

$$\frac{\partial I}{\partial x} = -C_0\frac{\partial V}{\partial t}$$

or

$$\frac{\partial^2 V}{\partial x^2} = LC_0\frac{\partial^2 V}{\partial t^2}$$

In free space, the wave should travel with the speed of light, i.e.,

$$\frac{\partial^2 V}{\partial x^2} = \frac{1}{v^2}\left(\frac{\partial^2 V}{\partial t^2}\right)$$

Therefore

$$LC_0 = \frac{1}{v^2} = \mu_0\varepsilon_0$$

This can be written in the matrix form as

$$\left[L\right] = \mu_0\varepsilon_0\left[C_0\right]^{-1} \tag{2.6.3}$$

In Eqn. (2.6.3), μ_0 and ε_0 are the permeability and permittivity for free space and $[C_0]$ is the capacitance matrix for the 2D interconnection configuration in free space.

Effect of Inductances on Interconnection Delays

The relative effects of including inductances in the interconnection delay models have been studied recently for a system of five single level interconnections [33]. Propagation delays obtained by using the RC

and RLC models have been compared as functions of the interconnection lengths, interconnection widths, and interconnection separations as shown in Figures 2.6.4 to 2.6.6, respectively. It is clear from these figures that the RLC delays exceed the RC delays significantly in all cases. These results further demonstrate the importance of including on-chip inductances in the chip design models.

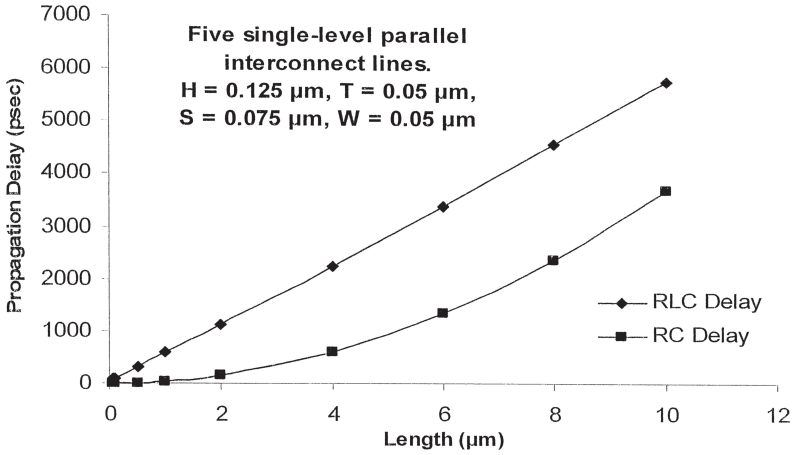

Figure 2.6.4 Dependence of propagation delays on the interconnection lengths in the range 50 nm to 10 μm using RC and RLC delay models [6].

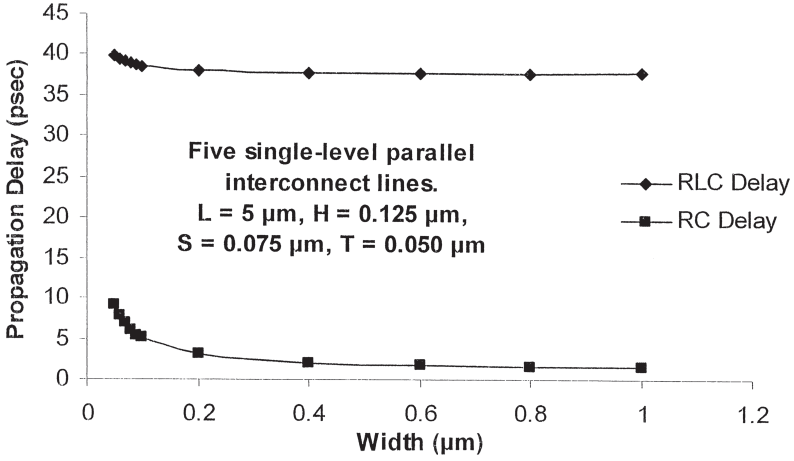

Figure 2.6.5 Dependence of propagation delays on the interconnection widths in the range 50 nm to 1 μm using RC and RLC delay models [6].

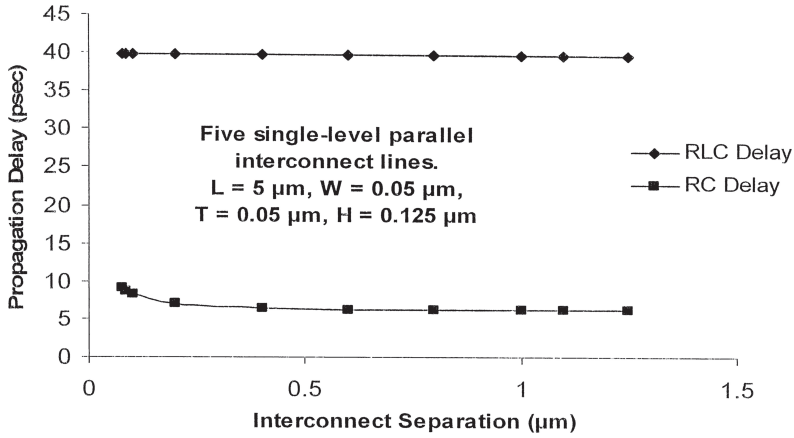

***Figure 2.6.6** Dependence of propagation delays on the interconnection separations in the range 50 nm to 1.5 µm using RC and RLC delay models [6].*

2.7 Inductance Extraction Using FastHenry

Interconnection inductances, unlike capacitances and resistances, are not material properties since they are produced by induced magnetic fields in an interconnection layout. Interconnection capacitances and resistances can be reduced by an understanding of the electrical properties of the interconnection material. On the other hand, the interconnection inductances are considered as a loop property and their values depend on the current return paths in an interconnection layout. Without prior knowledge of these current return paths or the so-called current loops, it would be very difficult to obtain the exact values of the inductances in an IC circuit. The only way out of this is to use a 3D field solver to calculate the exact current distributions in an interconnection layout and then to determine the inductive impedances present in the system. This method can prove to be extremely time consuming, computer-intensive, and uneconomical and the only alternative is to use a partial or approximate analysis technique which makes a trade-off between accuracy and compute efficiency. One such tool developed for the accelerated extraction of inductances is called FastHenry and is available under the broad title of Fast Field Solvers [38].

The Program "FastHenry"

FastHenry is a program capable of computing the frequency-dependent self and mutual inductances as well as the resistances of a 3D system of conductors. The data describing the geometry of the conductors and the frequencies of interest must be provided in an input file. This file specifies every conductor in the system as a sequence of rectilinear segments connected between nodes where a node is a point in the 3D space as shown in Figure 2.7.1. Every segment has a finite conductivity and has the shape of a parallelepiped whose height and width can be assigned. Any section of a segment can be further divided into an arbitrary number of parallel filaments, i.e., parallelepipeds with smaller cross sections than the original one. This is done to validate the assumption that every filament carries a uniform current. In fact, the current may no longer be uniformly distributed along the cross section of a conductor segment when the frequency increases due to the skin effect. However, if the section is divided into smaller filaments, the current can be reasonably approximated as uniform

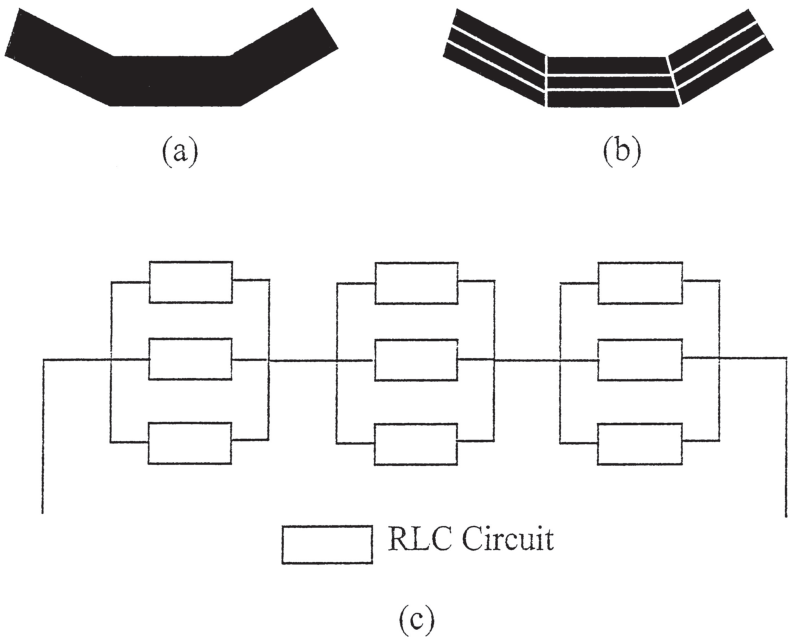

Figure 2.7.1 Splitting of conductors into segments and modeling them as RLC circuits [37].

in the filaments. In this way, it is possible to model the high-frequency effects on the segments. Ability to specify an arbitrary discretization of the volume of the conductors affects the accuracy of the results and is better as the discretization is refined. It is interesting to note that the computational complexity of the analysis technique used in FastHenry grows only linearly with the number of filaments required to discretize the conductors.

The results are provided in the form of a Maxwell impedance matrix $[Z] = [R] + j[L]$. The results can then be converted into equivalent SPICE-like lumped element circuit models with a utility called MakeLCircuit provided with FastHenry. The network thus obtained is valid only for a single frequency. Alternatively, it is possible to generate a SPICE-like circuit capable of modeling the frequency-dependent inductances and resistances. This capability is very useful because it allows the user to see how signals are degraded in the time domain by the frequency-dependent responses of the conductors [39].

FastHenry is often used with a user-interface tool called FastModel that allows the user to model and simulate the structure of conductors in a 3D editor making it possible to see the conductors described in a FastHenry input file in real time. FastModel can be integrated with FastHenry and provides features such as input file editing, unlimited number of 2D/3D views of the model, and print file capabilities. FastModel makes the inductance extraction process using FastHenry a much easier experience with the advantage that it allows the user to view the structure under analysis.

Extraction Results Using FastHenry

Now, two examples illustrating the applications of FastHenry and FastModel will be presented [33]. The first example studies inductances for a single conductor placed at a certain distance above a ground plane while the second example deals with two coupled conductors above a ground plane. Copper has been chosen as the conductor material in both the examples though the inductances unlike resistances and capacitances are not a function of the material. The thickness and the area of the ground plane are chosen randomly because these values do not affect inductances in general. The current return path for the conductor is assumed to flow

through the ground plane. Dielectrics are not included in the layouts because they are known to have no effect on the inductances.

Example 1: Single Conductor Above a Ground Plane

In this example, the layout consists of a single conducting interconnection in 3D space above a ground plane. The default values of the conductor dimensions in the layout and other parameters are as follows: Length = 100 nm; width = l0 nm; thickness = 5 nm; distance of the conductor from the ground plane = 30 nm; and frequency = 500 MHz. The screen shot of this layout in FastModel is shown in Figure 2.7.2 and the input file for FastHenry for this case is presented below:

FastHenry Input File for a Single Conductor Above a Ground Plane

```
* Setting the unit for all dimensions
.units um
* Defining the ground plane
g l x l = 0 yl = 0 zl = 0
+  x2 = 0.1 y2 = 0 z2 = 0
+  x3 = 0.l y3 = 0.1 z3 = 0
* Thickness of the ground plane
+ thick = 0.025
* Discretization
+ segl = 5 seg2 = 5
* Nodes for later reference
+ nin (0.1, 0.05, 0)
+ nout (0, 0.05, 0)
* The straight conductor
* The nodes
N1 x = 0 y = 0.05 z = 0.03
N2 x = 0.1 y = 0.05 z = 0.03
* Elements connecting the node
El N1 N2 w = 0.01 h = 0.005 nhinc = l nwinc = 2
* Shorting the end of the conductor with a corresponding
```

```
* point on the ground plane beneath it
.equiv nin N2
* Computing the loop inductance from N1 to a point directly underneath
      on the ground plane
.external N1 nout
* Computing the impedance for one frequency
.freq fmin = 5e8 fmax = 5e8 ndec = 0
* End of file
.end
```

Dependence of the inductance on the length of the conductor in the range of 20 to 100 nm is shown in Figure 2.7.3. This figure shows that the inductance increases rapidly with an increase in the conductor length and suggests that inductances for very short lines may be neglected safely. Figure 2.7.4 plots the dependence of the inductance on the width of the conductor in the range of 10 to 50 nm and shows that the inductance reduces gradually with an increase in the width.

Example 2: Two Conductors Above a Ground Plane

In this example, the system consists of two identical conducting interconnections placed above a conducting ground plane. The default values of the interconnection dimensions in the layout and other parameters are as

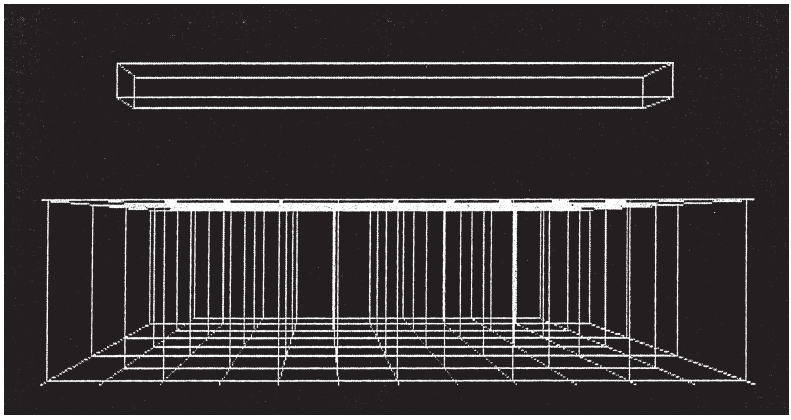

Figure 2.7.2 Screenshot of the single conducting interconnection above the ground plane [33].

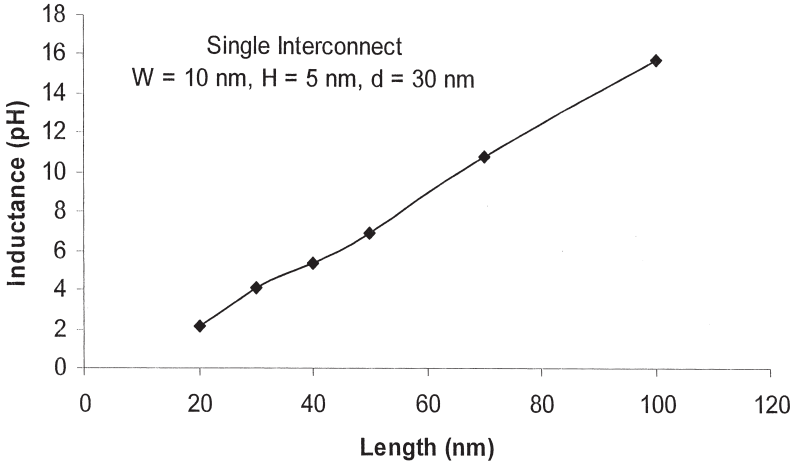

Figure 2.7.3 Dependence of inductance on the length of the conductor [33].

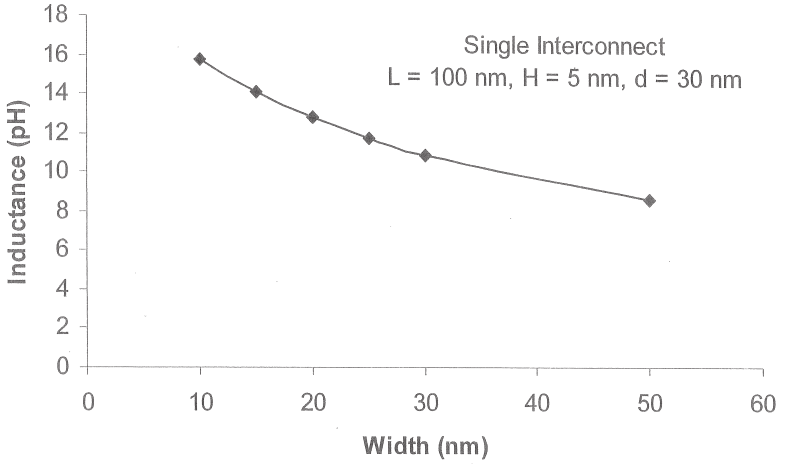

Figure 2.7.4 Dependence of inductance on the width of the conductor [33].

follows: Length = 100 nm; width = l0 nm; thickness = 5 nm; spacing between the interconnections = 30 nm; distance of the conductor from the ground plane = 30 nm; and frequency = 500 MHz. The screen shot of this layout in FastModel is shown in Figure 2.7.5.

The dependences of the self and coupling inductances for a system of two identical interconnections on the spacing between the interconnections in the range from 1 to 30 nm are shown in Figure 2.7.6.

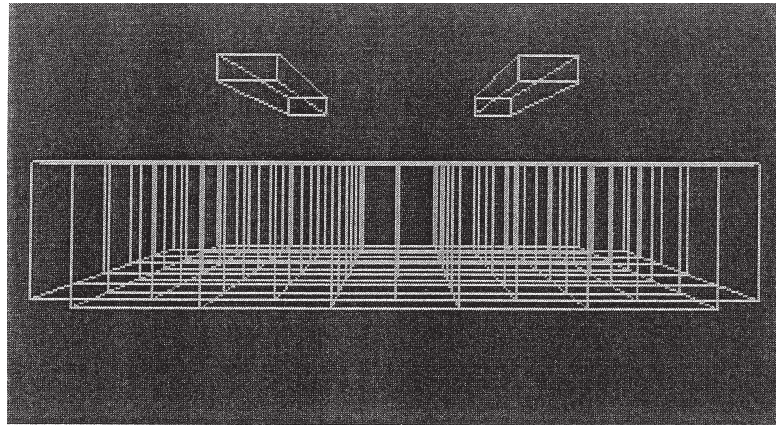

Figure 2.7.5 Screenshot of the two conducting interconnections above the ground plane [33].

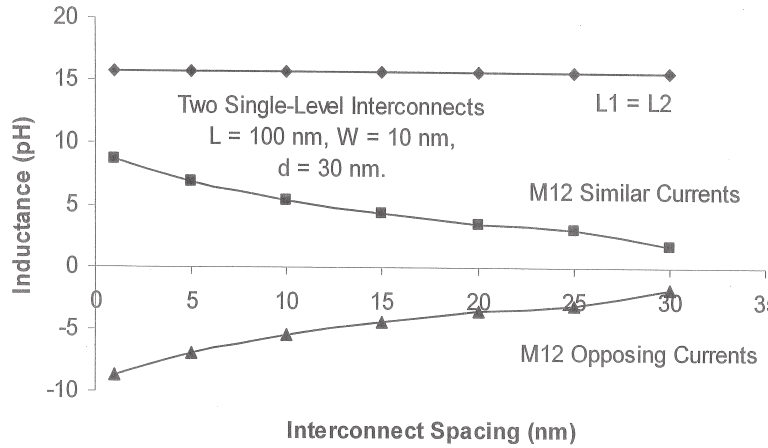

Figure 2.7.6 Dependences of the self and coupling inductances for a system of two interconnections on the spacing between the interconnections [33].

In this figure, the mutual inductances are plotted for currents in the two interconnections flowing in the same as well as opposite directions. This figure suggests that the self-inductances of the two interconnections are essentially independent of the spacing between them whereas the mutual inductances decreases with an increase in the interconnection spacing with a change of sign of the mutual inductance for the cases of similar and opposite currents.

2.8 Approximate Equations for Capacitances

In order to accurately determine the interconnection capacitances on the VLSI circuits, 2D and 3D effects must be taken into account. This requires rigorous numerical analysis which can be too time consuming when used in the computer-aided design (CAD) programs. Therefore, approximate formulas to estimate the interconnection capacitances are sometimes desirable. Here, such empirical formulas suggested by Sakurai and Tamaru [23] for a few interconnection structures are presented.

Single Line on a Ground Plane

A schematic diagram of a single interconnection line placed on bulk silicon (considered as the ground plane) is shown in Figure 2.8.1(a). The capacitance C_1 per unit length in terms of the various dimensions shown in Figure 2.8.1(a) can be estimated from the approximate formula

$$C_1 = \varepsilon_{ox}\left[1.15\left(\frac{W}{H}\right) + 2.80\left(\frac{T}{H}\right)^{0.222}\right] \qquad (2.8.1)$$

where ε_{ox} is the dielectric constant of the insulator such as SiO_2 for which $\varepsilon_{ox} = 3.9 \times 8.855 \times 10^{-14}$ F/cm. The relative error of Eqn. (2.8.1) is within 6 percent for $0.3 < (W/H) < 30$ and $0.3 < (T/H) < 30$.

Two Lines on a Ground Plane

A schematic diagram of two interconnection lines placed on bulk silicon (considered as the ground plane) is shown in Figure 2.8.1(b). In this case, the total capacitance C_2 of one line per unit length includes the ground capacitance C_{10} and the coupling capacitance C_{12} between the lines, i.e., $C_2 = C_{10} + C_{12}$. In terms of the various dimensions shown in Figure 2.8.1(b), C_2 can be estimated from the approximate formula

$$C_2 = C_1 + \varepsilon_{ox}\left[0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34} \qquad (2.8.2)$$

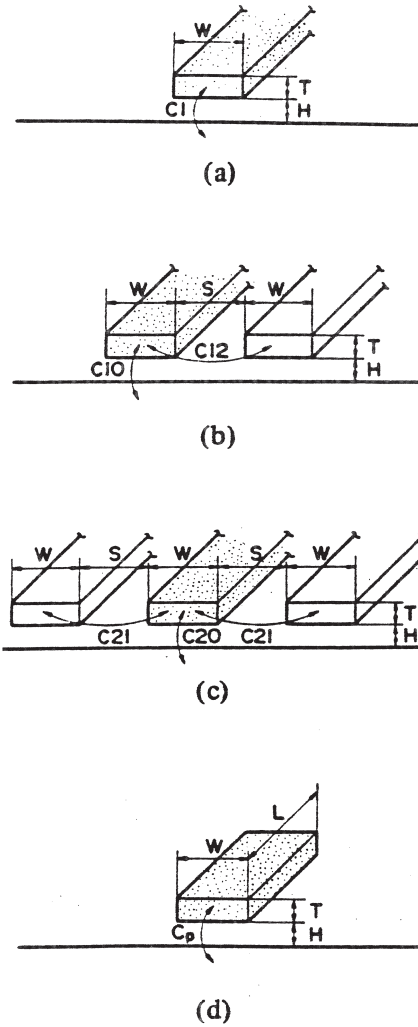

Figure 2.8.1 Schematic diagram of (a) single line on a conducting ground plane; (b) two lines on a ground plane; (c) three lines on a ground plane; and (d) single plate of finite dimensions on a ground plane [23]. (© 1983 IEEE)

The relative error of Eqn. (2.8.2) is less than 10 percent for $0.3<(W/H)<10$, $0.3<(T/H)<10$ and $0.5<(S/H)<10$. It should be noted that the Eqn. (2.8.2) tends to the single line Eqn. (2.8.1) as the line separation S approaches infinity.

Three Lines on a Ground Plane

A schematic diagram of three interconnection lines placed on bulk silicon (considered as the ground plane) is shown in Figure 2.8.1(c). In this case, the total capacitance of one line includes the ground capacitance C_{20} and the coupling capacitance C_{21} between the lines. For example, the total capacitance C_3 of the middle line per unit length is equal to $C_{20} + 2C_{21}$. In terms of the various dimensions shown in Figure 2.8.1(c), C_3 can be estimated from the approximate formula

$$C_3 = C_1 + 2\varepsilon_{ox}\left[0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222}\right]\left(\frac{S}{H}\right)^{-1.34} \tag{2.8.3}$$

The relative error of Eqn. (2.8.3) is less than 10 percent for $0.3<(W/H)<10$, $0.3<(T/H)<10$ and $0.5<(S/H)<10$. It should be noted that the Eqn. (2.8.3) tends to the single line Eqn. (2.8.1) as the line separation S approaches infinity.

Single Plate with Finite Dimensions on a Ground Plane

A schematic diagram of a single plate with finite dimensions placed on bulk silicon (considered as the ground plane) is shown in Figure 2.8.1(d). In this case, the capacitance C_p between the plate and the ground includes the 3D effects. In terms of the various dimension parameters shown in Figure 2.8.1(d), C_p can be estimated from the approximate formula

$$C_p = \varepsilon_{ox}\left[1.15\left(\frac{\textit{plate area}}{H}\right) + 1.40\left(\frac{T}{H}\right)^{0.222}(\textit{plate circumference}) + 4.12H\left(\frac{T}{H}\right)^{0.728}\right] \tag{2.8.4}$$

Compared to the data published by Ruehli and Brennan [17], the relative error of Eqn. (2.8.4) is within 10 percent for $0<(W/L)<1$, $0.5<(W/H)<40$ and $0.4<(T/H)<10$. It should be noted that Eqn. (2.8.4) tends to Eqn. (2.8.1) as the plate length approaches infinity.

2.9 Approximate Equations for Interconnection Capacitances and Inductances on Silicon and GaAs Substrates

In the recent years, insulating substrates such as Cr-doped semi-insulating gallium arsenide (GaAs) have emerged as alternatives to silicon. This is partially because of the argument that interconnections fabricated on these substrates offer considerably lower capacitances than those fabricated on silicon. Here, simplified formulas for finding the line and coupling capacitances and inductances for interconnections fabricated on the oxide-passivated silicon and semi-insulating GaAs substrates are presented [26].

Line Capacitances and Inductances

The cross section of an interconnection fabricated on an insulating substrate is shown in Figure 2.9.1 (a). It is defined by its width (w), height of the substrate (h), and the relative dielectric constant of the material of the substrate (ε_r). It is assumed that the thickness of the interconnection line is negligibly small. The approximate values of the line capacitance and inductance of the interconnection can be determined by using the formulas [26]:

$$C = \frac{2\pi\varepsilon_0\varepsilon_{eff}}{\ln\left[\frac{8h}{w} + \frac{w}{4h}\right]} \quad ; \quad w \le h$$

$$L = \frac{\mu_0}{2\pi}\ln\left[\frac{8h}{w} + \frac{w}{4h}\right] \tag{2.9.1}$$

where ε_{eff} is the effective dielectric constant of the substrate material given by

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 10\frac{h}{w}\right]^{-0.5}$$

The cross section of an interconnection fabricated on an oxide-passivated silicon substrate is shown in Figure 2.9.1 (b). In this figure, t_{ox} is the oxide thickness and t_{Si} is the thickness of the silicon substrate. For frequencies below 1 GHz, the approximate values of the line capacitance

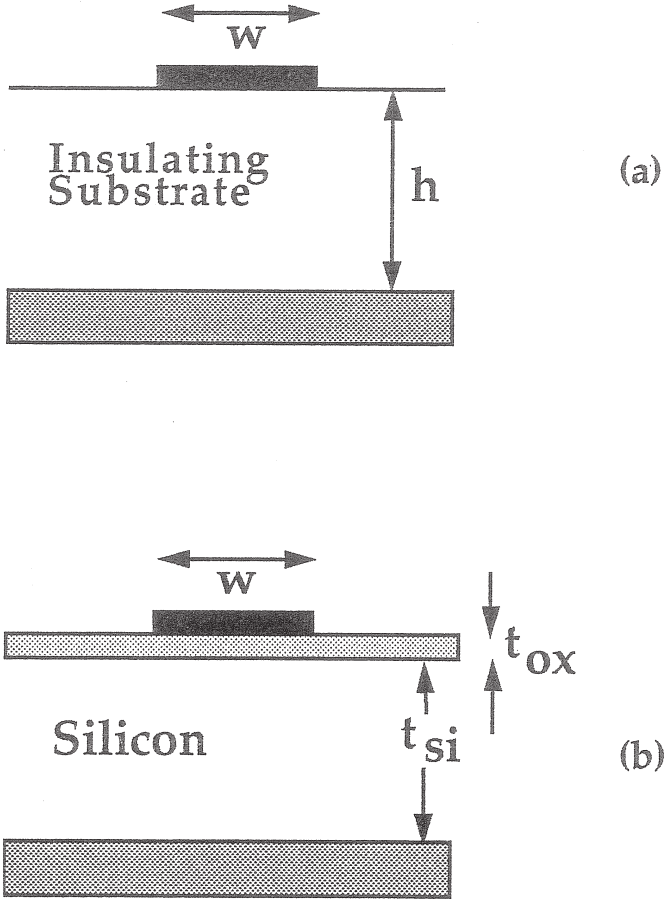

Figure 2.9.1 Schematic diagram of the cross section of a typical interconnection on an (a) insulating substrate and (b) oxide-passivated silicon substrate [26]. (© 1982 IEEE)

and inductance of the interconnection on an oxide-passivated silicon substrate can be determined by using the formulas:

$$C = \frac{2\pi\varepsilon_0\varepsilon_{eff}}{\ln\left[\frac{8h}{w} + \frac{w}{4h}\right]} \quad ; \quad w \le t_{ox}$$

$$C = \varepsilon_0\varepsilon_r\left[\frac{w}{t_{ox}} + 2.42 - 0.44\frac{t_{ox}}{w} + \left(1 - \frac{t_{ox}}{w}\right)^6\right] \quad ; \quad w \ge t_{ox}$$

$$L = \frac{\mu_0}{2\pi}\ln\left[\frac{8h}{w} + \frac{w}{4h}\right] \quad ; \quad h = t_{ox} + t_{Si} \qquad (2.9.2)$$

Maxwellian Capacitance Matrix

The Maxwellian capacitance matrix for an array of n conductors referring to a common ground plane has the following general form:

$$\begin{bmatrix} C_{11} & C_{12} & \cdots & C_{1n} \\ C_{21} & C_{22} & \cdots & C_{2n} \\ \cdots & \cdots & \cdots & \cdots \\ C_{n1} & C_{n2} & \cdots & C_{nn} \end{bmatrix}$$

The diagonal element C_{ii} is the self-capacitance of conductor i and is a measure of the capacitance of a single conductor when all other conductors are grounded. The diagonal element C_{ij} is the coefficient of induction and is a measure of the negative of mutual capacitance between conductor i and conductor j. The Maxwellian capacitance matrices for a system of five conductors with equal line widths equal to 1 μm each and equal separations equal to 1 μm each fabricated on oxide-passivated silicon and semi-insulating gallium arsenide [26] are given below:

Substrate: 1-μm SiO_2 on Si:

$$C_{ij} = \begin{bmatrix} 0.776 & -0.043 & -0.004 & -0.002 & 0 \\ -0.043 & 0.760 & -0.045 & -0.004 & -0.001 \\ -0.004 & -0.045 & 0.759 & -0.004 & -0.004 \\ -0.002 & -0.004 & -0.004 & 0.760 & -0.044 \\ 0 & -0.002 & -0.004 & -0.044 & 0.776 \end{bmatrix} \text{ pF/cm}$$

Substrate: GaAs:

$$C_{ij} = \begin{bmatrix} 1.066 & -0.520 & -0.154 & -0.092 & -0.090 \\ -0.520 & 1.315 & -0.454 & -0.124 & -0.092 \\ -0.154 & -0.454 & 1.329 & -0.454 & -0.155 \\ -0.092 & -0.124 & -0.454 & 1.315 & -0.520 \\ -0.090 & -0.092 & -0.155 & -0.520 & 1.066 \end{bmatrix} \text{ pF/cm}$$

Inductance Matrix

For a nonmagnetic and lossless substrate, the inductance matrix for the system of conductors can be derived from the Maxwellian capacitance

matrix for the same system of conductors in free space, i.e., for $\varepsilon_r = 1$. If $v_o = 1/\sqrt{LC}$ is the speed of light in free space then the inductance matrix is given by

$$\left[L_{ij}\right] = \frac{1}{v_o^2}\left[C_{ij}\right]^{-1}$$

The inductance matrix for a system of five conductors with equal line widths equal to 1 μm each and equal separations equal to 1 μm each fabricated on either of oxide-passivated silicon or gallium arsenide substrates is given below:

$$L_{ij} = \begin{bmatrix} 15.126 & 10.597 & 9.235 & 8.429 & 7.859 \\ 10.597 & 15.086 & 10.579 & 9.227 & 8.429 \\ 9.235 & 10.579 & 15.080 & 10.579 & 9.235 \\ 8.429 & 9.227 & 10.579 & 15.086 & 10.597 \\ 7.859 & 8.429 & 9.235 & 10.597 & 15.115 \end{bmatrix} \text{ nH/cm}$$

Note that the inductance matrix given above is valid for all frequencies on insulating substrates but only below 1 GHz on silicon substrates. From an examination of the capacitance and inductance matrices, it can be seen that the magnetic couplings have a longer range than the electrical couplings. For example, the mutual inductance between line 1 and line 5 is only 30 percent less than that between line 1 and line 2 whereas the mutual capacitance has decreased by almost a factor of five.

Exercise 2.3

Use equations (2.9.1) and (2.9.2) to calculate the line capacitances of an interconnection on 250-μm thick silicon (assume 1-μm SiO_2 thickness) and GaAs for line widths in the range 1 to 100 μm. Plot your values and make comments on the relative lowering of capacitance on an insulating substrate as the interconnection width increases.

Exercise 2.4

Using equations (2.9.1) and (2.9.2), calculate and plot the line inductances of an interconnection on 250-μm thick silicon (assume 1-μm SiO_2 thickness) and GaAs for line widths in the range 1 to 100 μm.

Exercise 2.5

Discuss the characteristics of a numerical model that make it suitable for inclusion in a CAD tool. Review the techniques presented in this chapter for their suitability for inclusion in the CAD tools.

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CHAPTER 3

Modeling of Interconnection Delays

The modern interconnection layout is an extremely high-density structure with millions of metallic lines running vertically and horizontally on various levels. The interconnection delays have been studied at length [1–72] and the delay models used in the industry have changed over time since the relative significance of the different interconnection parasitics (resistances, capacitances, and inductances) has changed over time. Until a few years ago, only interconnection capacitances were considered to be significant enough to contribute to the overall chip delay. With the advent of complex circuits, continuous scaling and the use of longer interconnection lines, interconnection resistance became an important factor in the delay models. The interconnection delay models could be classified as lumped capacitance models, simple RC models, lumped RC models, and distributed RC models. For the modern integrated circuits (ICs) which are much faster, it is important to include the interconnection inductances in the delay models. In fact, the inductance is becoming as important as the capacitance was a few years ago. In most cases, the interconnection delays on an IC chip account for more than 50 percent of the total delays. Clearly, a comprehensive understanding of the dependence of the interconnection delays on the various interconnection design parameters is needed for optimum chip design.

In the literature, numerous numerical techniques used to model the time- domain pulse propagation in the interconnection lines on the high-speed circuits are available [1–33]. The method of characteristics

modified to include the frequency-dependent losses has been employed [4–6] and the well-known transmission line theory has been used to analyze the high-speed interconnections [16, 17, 22–25]. Researchers have attempted to model the interconnections in terms of lumped and distributed circuit elements available in computer-aided design (CAD) programs such as SPICE [9, 13] and SPICE-like models have been developed [26, 27]. Specialized techniques to compute the time-domain responses of interconnection structures terminated in linear and nonlinear networks from their frequency domain analysis have been reported [12, 15]. In most cases, interconnections have been modeled as single lossy lines or multiple coupled lossless microstrip lines. High-frequency effects such as conductor loss, dielectric loss, skin-effect, and frequency-dependent effective dielectric constant have also been studied [18]. More recently, research has focused on developing approximate models for the transient response of distributed RLC lines [19, 20, 29–33]. Here are the chapter objectives:

- After going through section 3.1, students should be able to analyze the interconnection delays on very high-speed VLSI circuits using a metal–insulator–semiconductor microstrip line model.
- After going through section 3.2, students should be able to model single-level interconnections on a semi-insulating substrate as transmission lines.
- After going through section 3.3, students should be able to model multilevel lossless parallel interconnections.
- After going through section 3.4, students should be able to extend the model presented in section 3.3 to lossy parallel and crossing interconnections.
- After going through section 3.5, students should be familiar with the very high-frequency effects in interconnections such as conductor loss, dielectric loss, skin-effect, and frequency-dependent effective dielectric constant.

- After going through section 3.6, students should be able to write closed-form expressions for interconnection delays using the RC and RLC models for an interconnection.
- After going through section 3.7, students will be familiar with the concept of active interconnections and should be able to analyze delays in an active interconnection driven by several mechanisms.

3.1 Metal–Insulator–Semiconductor Microstrip Line Model of an Interconnection

Here, the interconnection delays on a very high-speed IC chip are investigated by using a metal–insulator–semiconductor (MIS) microstrip line model for the interconnection [11].

The Model

An MIS single microstrip line is shown in Figure 3.1.1. Note that the microstrip line is formed on a surface-passivated semiconductor substrate which in turn is placed on a metallized back. Figure 3.1.2 shows the equivalent circuit per unit length of the MIS microstrip line used

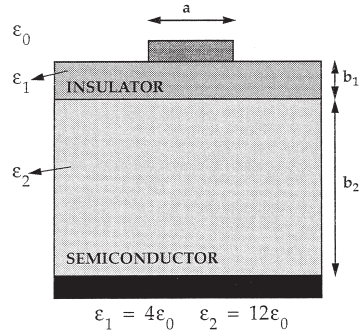


Figure 3.1.1 An MIS microstrip line model for an interconnection [11]. (© 1984 IEEE)

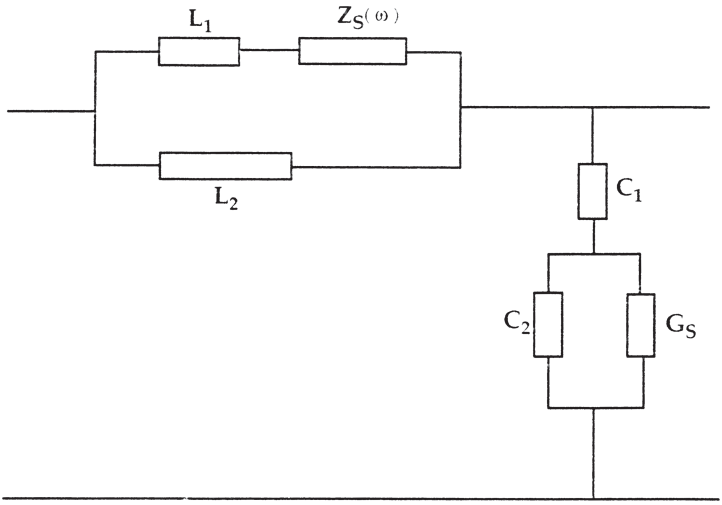


Figure 3.1.2 Equivalent circuit per unit length of the MIS microstrip line [11]. (© 1984 IEEE)

in the following analysis. The various symbols used in Figure 3.1.2 are defined as follows:

C_1 = Insulator capacitance
C_2 = Semiconductor capacitance
G_s = Transverse conductance of the semiconductor
L_1 = Inductance of the insulator
L_2 = Inductance of the air region
$Z_s(\omega)$ = Impedance of the semiconductor region including the semiconductor inductance and the longitudinal resistance.

In terms of the length parameters shown in Figure 3.1.3, which shows the inhomogenous parallel waveguide mapped from the MIS microstrip line by Schwarz–Christoffel transformation, the various circuit elements are given by the following expressions [11]:

$$C_1 = \frac{a^+}{b_1^+} = \varepsilon_1 \frac{a}{b_1}$$

$$C_2 = \varepsilon_{eff} \frac{a^+}{b_2^+}$$

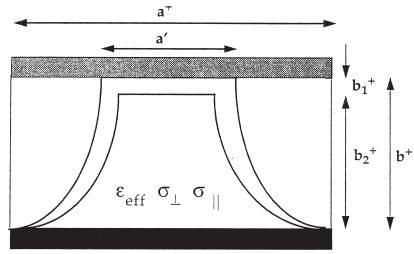


Figure 3.1.3 The inhomogenous parallel waveguide mapped from the MIS microstrip line by Schwarz–Christoffel transformation [11]. (© 1984 IEEE)

$$G_s = \sigma_{\perp}\frac{a^+}{b_2^+}$$

$$L_1 = \mu_0\frac{b_1^+}{a'}$$

$$L_2 = \mu_0\frac{b_2^+}{a^+ - a'}$$

and the impedance of the semiconductor region, $Z_s(\omega)$, is given by the expression:

$$Z_s(\omega) = j\omega\mu_0\left(\frac{b_2^+}{a'}\right)\left(\frac{1}{\gamma_m b_2^+}\right)\tanh(\gamma_m b_2^+)$$

where

$$\gamma_m = \sqrt{j\omega\mu_0\sigma_{11}}$$

$$\sigma_{11} = \sigma\bar{h}^2$$

$$\bar{h} = \sqrt{|E'(E' - K'k^2)|}$$

and, referring to Figure 3.1.3, $\bar{h}$ is the average scaling parameter between the center of the top plane and the center of the bottom plane.

The scaling parameter (h) of the Schwarz–Christoffel transformation is given by

$$h = \left| E' - K'k^2 \mathrm{sn}^2\left(\frac{\pi W^2}{2b}\right) \right|$$

where sn is the Jacobi's elliptic function and K' and E' are complete elliptic integrals of the first and second kinds with modulus k, respectively. Note that $Z_s(\omega)$ is frequency dependent because of the skin effect in the semiconductor.

For a given interconnection geometry, the transient waveforms can be calculated by the following steps: (a) Calculation of equivalent circuit parameters; (b) calculation of characteristic impedance and propagation constants based on the equivalent circuit shown in Figure 3.1.2; and (c) calculation of the transient waveforms under arbitrary excitation and termination conditions by the inverse Laplace transformation. The last step involving inverse Laplace transformation can be carried out by using the standard trigonometric function expansion method.

Simulation Results

a) *Semi-Infinite Interconnections*

For an interconnection of semi-infinite length (which is equivalent to the line of finite length terminated with a hypothetical matched load), the dependences of the propagation delay time (time to 50 percent rise) and rise time (time from 10 to 90 percent rise) of the step response on the width of the interconnection are shown in Figure 3.1.4 and Figure 3.1.5 shows these dependences on the distance z from the signal source. For a semi-infinite interconnection, the dependences of the delay and rise times on the substrate resistivity in the range 10^{-4} to 10^5 Ω.cm are shown in Figure 3.1.6. The responses are calculated at positions with distances of z = 1 mm and z = 3 mm from the signal source. The results of Figure 3.1.6 can be explained in terms of the three fundamental modes, i.e., the skin-effect mode, the slow-wave mode, and the dielectric quasi-transverse electromagnetic (TEM) mode as follows: (a) The increase of the delay

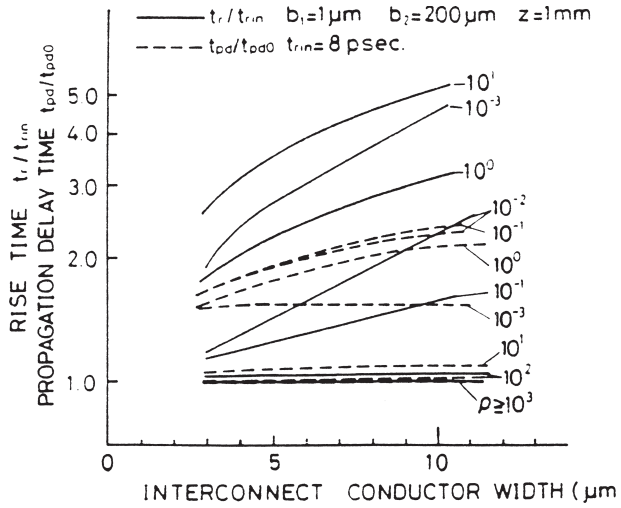


Figure 3.1.4 Dependences of the delay time and rise time on the interconnection width for a semi-infinite interconnection. The rise time of the input pulse is assumed to be 8 ps [11]. (© 1984 IEEE)

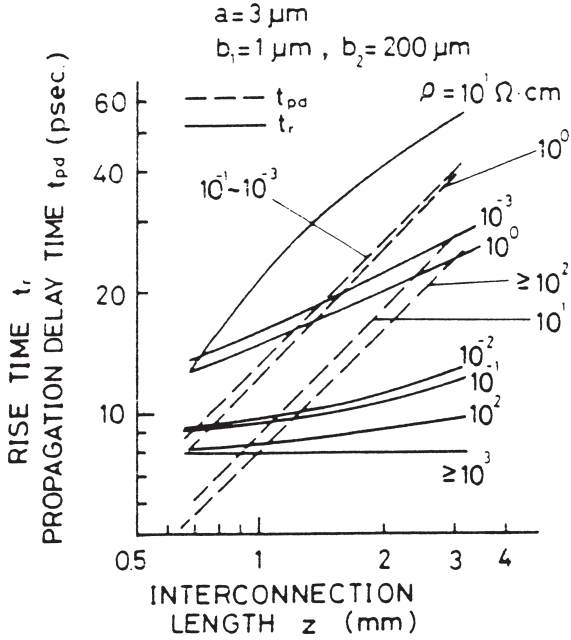


Figure 3.1.5 Dependences of the delay time and rise time on the distance z from the signal source for a semi-infinite interconnection. The rise time of the input pulse is assumed to be 8 ps [11]. (© 1984 IEEE)

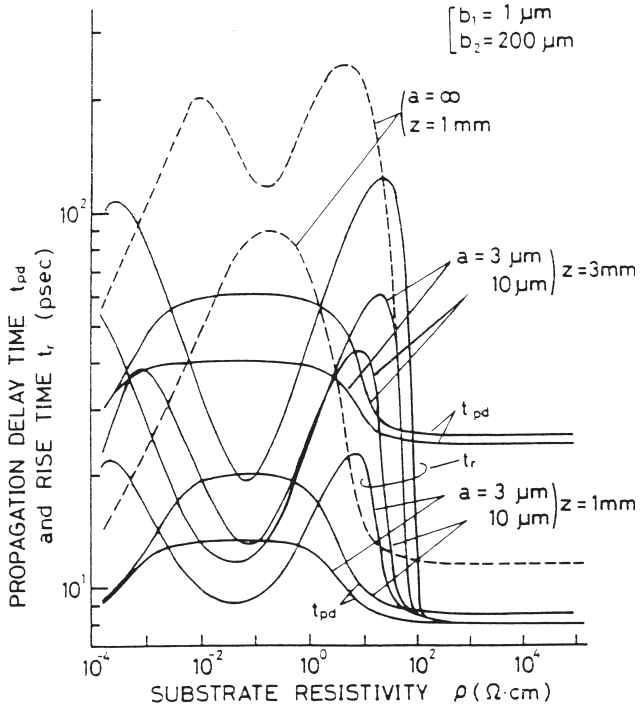


Figure 3.1.6 Calculated dependences of the delay time and rise time on the substrate resistivity for a semi-infinite interconnection. The rise time of the input pulse is assumed to be 8 ps [11]. (© 1984 IEEE)

time in the mid-resistivity range is because of the slow-wave mode; and (b) the rise time peaks on both sides of the delay time peak are due to mode transitions from the slow-wave mode either to the dielectric quasi-TEM mode or to the skin-effect mode.

b) *Interconnections Between Logic Gates*

For an interconnection connecting two logic gates shown in Figure 3.1.7(a), an equivalent model is shown in Figure 3.1.7(b) where R_s is the output resistance of the driving gate and corresponds to the resistance of the input signal source while *CL* is the input capacitance of the driven gate and corresponds to the load capacitance of the interconnection line. In gates consisting of field-effect transistor (FET)-type devices such as metal–semiconductor field-effect transistors (MESFETs),

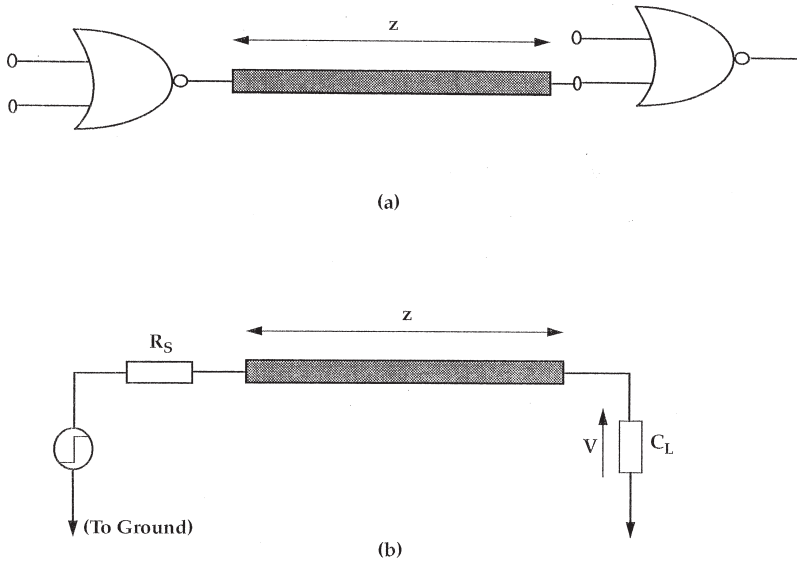


***Figure 3.1.7** (a) Schematic diagram of an interconnection between two logic gates and (b) its equivalent model [11]. (© 1984 IEEE)*

metal–oxide–semiconductor field-effect transistors (MOSFETs), and high-electron-mobility transistors (HEMTs), R_s is approximately equal to the inverse of the transconductance g_m. To determine C_L, it can be used as a rule of thumb that a standard 1-μm gate GaAs MESFET has approximately an input gate capacitance of 1 fF per 1-μm gate width. The transconductance g_m and the output resistance R_s of various FET devices each of gate length = 1 μm and gate width = 10 μm are given in Table 3.1.1.

The calculated voltage waveforms for an interconnection of width = 3 μm and length = 3 mm for two source resistances of 1 kΩ and 100 Ω

***Table 3.1.1** Transconductance g_m and R_s of Various FET Devices*

Device	g_m (mS)	Rs (Ω)
GaAs MESFET	1.4	710
Si MOSFET	0.8	1250
HEMT (77k)	2.9	350

Source: From [11]. © 1984 IEEE.
Note: Gate length. 1 μm; gate width, 10 μm.

and for various values of the substrate resistivity are given in Figures 3.1.8(a) and 3.1.8(b), respectively. For the sake of comparison, the waveforms based on the lumped capacitance approximation for $\rho = \infty$ and $\rho = 0$ are also included in Figures 3.1.8(a) and 3.1.8(b). It can be concluded that the lumped capacitance approximation yields reasonably good results when the source resistance is high and the response is slow. However, if the source resistance is low and the response is fast then the results based on the lumped capacitance approximation become rather inadequate.

The dependences of the calculated delay times on the signal source resistance for several values of the substrate resistivity are shown in Figure 3.1.9. For the sake of comparison, the values based on the lumped capacitance approximation for $\rho = \infty$ and $\rho = 0$ are also included. It can

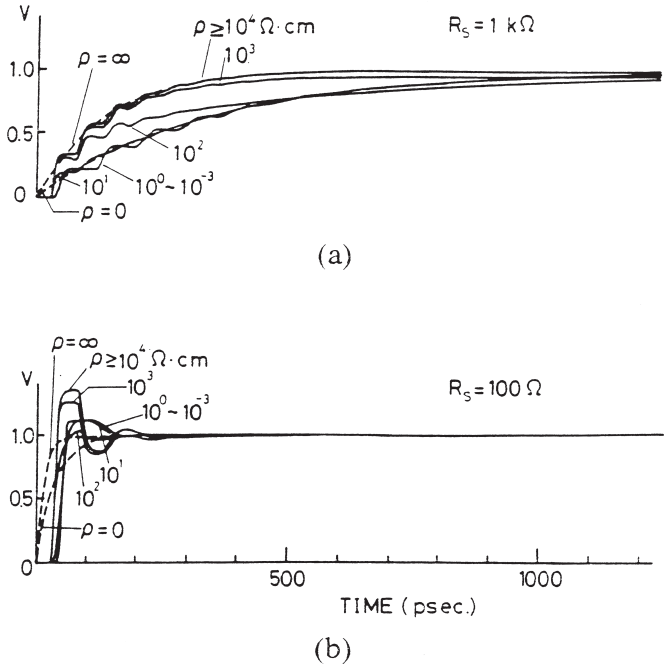


Figure 3.1.8 Calculated step response waveforms for (a) R_s 1 kΩ and (b) R_s = 100 Ω. Dimension parameters are $a = 3\ \mu m$, $z = 3$ mm, $b_1 = 1\ \mu m$, and $b_2 = 200\ \mu m$. Results based on the "lumped capacitance" approximation are shown by the dashed curves [11]. (© 1984 IEEE)

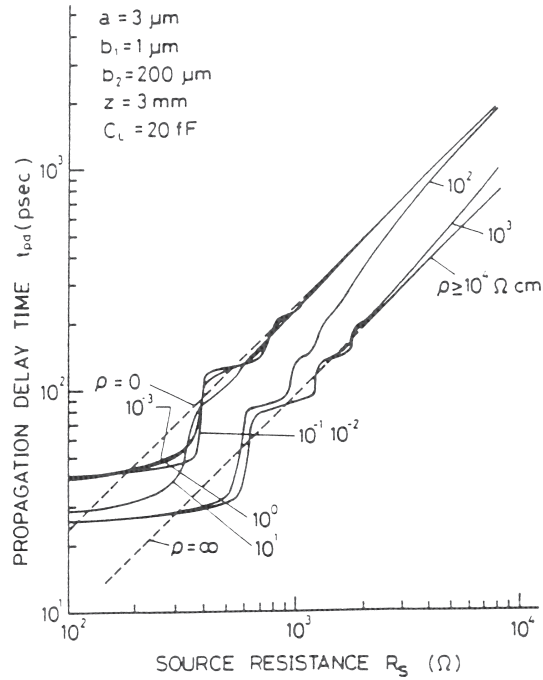


Figure 3.1.9 Dependence of the calculated delay times on the signal source resistance for several values of substrate resistivity. Results based on the "lumped capacitance" approximation are shown by the dashed curves [11]. (© 1984 IEEE)

be seen that the lumped capacitance approximation yields reasonably good results when the delay time is nearly over 200 ps. This figure also indicates that the semi-insulating substrates offer a significant advantage in delay times over semiconducting substrates.

3.2 Transmission Line Analysis of Single-Level *Interconnections*

Now, an algorithm for calculating the propagation delays in the high-density single-level interconnections on the GaAs-based high-speed ICs is presented. The interconnection has been modeled as a distributed element equivalent circuit and the effects of capacitive coupling with the neighboring interconnections have been included. The technique presented in

the model can be applied to lossy as well as the lossless lines and can be easily extended to include coupling with any number of neighboring lines. The interconnection capacitances can be determined by the method of moments in conjunction with a Green's function appropriate for the geometry of the interconnections [34]. As mentioned earlier, the capacitances thus determined include the fringing fields as well as the shielding effects due to the presence of the neighboring conductors. The model has been used to determine the dependences of the delay times and the rise times (defined as the times taken by the output voltages to rise from 0 to 50 percent and 10 to 90 percent of their steady state values, respectively [35]) on the interconnection dimensions and other parameters.

The Model

An interconnection, modeled as a transmission line driven by a unit step voltage source and terminated by a load $Z_{L,}$ is shown in Figure 3.2.1. All the elements shown in the figure are per unit length of the interconnection.

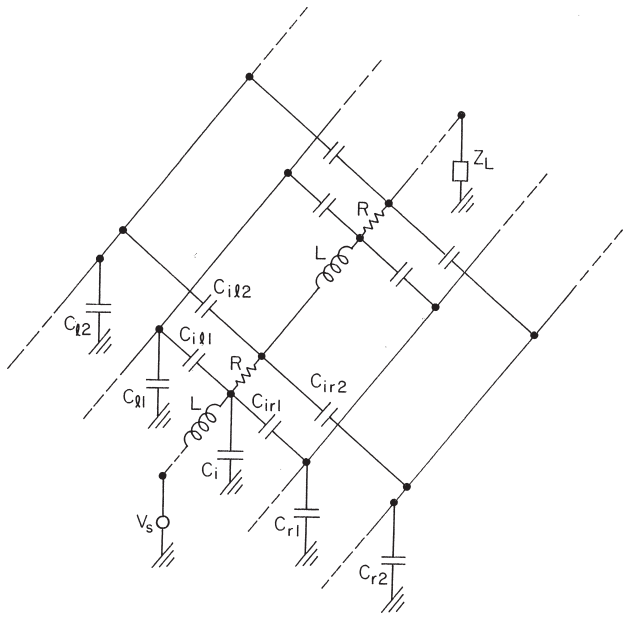


Figure 3.2.1 An interconnection modeled as a transmission line driven by a unit step voltage source and terminated by a load Z_L. Coupling of the interconnection with its nearest two neighbors on each side is also shown

Capacitive couplings of the line with its first and second neighbors are also shown in the figure. The series resistance and inductance elements for the neighboring interconnections will not affect the propagation characteristics along the interconnection in question; therefore, these are not included in the model. The various symbols used in the equivalent circuit of Figure 3.2.1 are defined as follows:

R = Resistance of the interconnection line
L = Inductance of the interconnection line
C_i = Self capacitance (i.e., the capacitance between the conductor and the ground plane) of the interconnection line
C_{il1} = Mutual capacitance between the interconnection and its first neighbor on its left
C_{ir1} = Mutual capacitance between the interconnection and its first neighbor on its right
C_{il2} = Mutual capacitance between the interconnection and its second neighbor on its left
C_{ir2} = Mutual capacitance between the interconnection and its second neighbor on its right
C_{l1} = Self capacitance of the first neighbor on the left of the interconnection
C_{l2} = Self capacitance of the second neighbor on the left of the interconnection
C_{r1} = Self capacitance of the first neighbor on the right of the interconnection
C_{r2} = Self capacitance of the second neighbor on the right of the interconnection

As far as the propagation along the interconnection is concerned, the effect of its coupling with its first right neighbor is to connect an impedance Z_1 in parallel with the capacitance Ci where

$$Z_1 = \frac{C_{ir1} + C_{r1}}{sC_{r1}C_{ir1}} \tag{3.2.1}$$

Similarly, the contributions of coupling of the interconnection with its second right neighbor, the first left neighbor, and the second left

neighbor are to connect impedances Z_2, Z_3, and Z_4 respectively in parallel with C_i where

$$Z_2 = \frac{C_{ir2} + C_{r2}}{sC_{r2}C_{ir2}} \tag{3.2.2}$$

$$Z_3 = \frac{C_{il1} + C_{l1}}{sC_{l1}C_{il1}} \tag{3.2.3}$$

and

$$Z_4 = \frac{C_{il2} + C_{l2}}{sC_{l2}C_{il2}} \tag{3.2.4}$$

Therefore, the equivalent circuit of Figure 3.2.1 reduces to that shown in Figure 3.2.2. Figure 3.2.2 shows one section of the equivalent circuit only and can be used to determine the propagation constant for the interconnection line as follows. The propagation constant γ is defined by the relationship

$$\gamma = \sqrt{\left(\frac{Z_s}{Z_p}\right)} \tag{3.2.5}$$

where the series impedance per unit length Z_s is given by

$$Z_s + R + s\,L \tag{3.2.6}$$

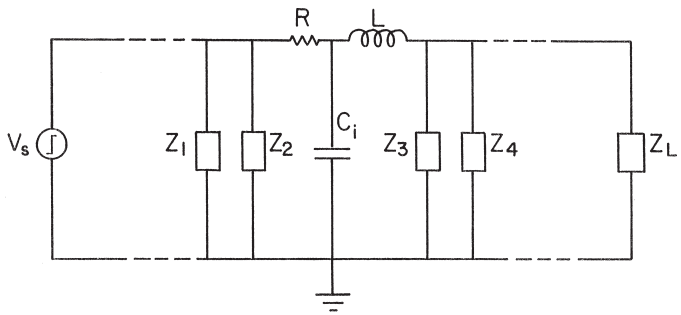


Figure 3.2.2 One section of the uncoupled interconnection line equivalent to each section of the coupled lines of Figure 3.2.1

and the parallel impedance per unit length, Z_p, is the impedance of the parallel combination of C_i, Z_1, Z_2, Z_3, and Z_4, i.e.,

$$\frac{1}{Z_p} = \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \frac{1}{Z_4} + sC_i$$

$$= (Y_1 + Y_2 + Y_3 + Y_4 + C_i)\, s \tag{3.2.7}$$

where

$$Y_1 = \frac{C_{r1} C_{ir1}}{C_{ir1} + C_{r1}} \tag{3.2.8}$$

$$Y_2 = \frac{C_{r2} C_{ir2}}{C_{ir2} + C_{r2}} \tag{3.2.9}$$

$$Y_3 = \frac{C_{l1} C_{il1}}{C_{il1} + C_{l1}} \tag{3.2.10}$$

$$Y_4 = \frac{C_{l2} C_{il2}}{C_{il2} + C_{l2}} \tag{3.2.11}$$

The propagation constant will then be given by

$$\gamma = \sqrt{\left[(R + sL)s\left\{\sum_{i=1}^{4} Y_i + C_i\right\}\right]} \tag{3.2.12}$$

and the characteristic impedance will be given by

$$Z_0 = \sqrt{\left[\frac{(R + sL)}{s\left(C_i + \sum_{i=1}^{4} Y_i\right)}\right]} \tag{3.2.13}$$

In the Laplace transform domain, the voltage and current distributions along an interconnection satisfy the following transmission line equations

$$\frac{d^2V}{dz^2} = \gamma^2 V \tag{3.2.14}$$

and

$$\frac{d^2I}{dz^2} = \gamma^2 I \tag{3.2.15}$$

The most general solutions for the voltage and current along the interconnection length (denoted by the coordinate z) are given by

$$v_z = \mathrm{A}e^{-\gamma z} + \mathrm{B}e^{-\gamma z} \tag{3.2.16}$$

$$i_z = \frac{\mathrm{A}e^{-\gamma z} - \mathrm{B}e^{-\gamma z}}{Z_0} \tag{3.2.17}$$

where the constants A and B can be determined by employing the known boundary conditions. If the interconnection is driven at the end $z = 0$ by a source of voltage V_s having an internal impedance R_s then at this end

$$v_z = V_s - i R_s \tag{3.2.18}$$

Furthermore, if the interconnection is terminated by a load Z_L at $z = l$, then at this end

$$\frac{v_z}{i_z} = Z_L \tag{3.2.19}$$

Substituting conditions (3.2.18) and (3.2.19) in equations (3.2.16) and (3.2.17), the values of A and B can be obtained to be

$$\mathrm{A} = \frac{V_s Z_0}{\left[R_s + Z_0 - \left(\frac{Z_L - Z_0}{Z_L + Z_0}\right)(R_s - Z_0)e^{-2\gamma\ell}\right]} \tag{3.2.20}$$

$$\mathrm{B} = \mathrm{A}\left(\frac{Z_L - Z_0}{Z_L + Z_0}\right)e^{-2\gamma\ell} \tag{3.2.21}$$

In order to determine the propagation delays (i.e., the delay time and the rise time) for an interconnection, one needs to know how the voltage at the load varies as a function of time in response to a unit step voltage applied at $z = 0$. In the s-space, a unit step voltage source is represented by

$$V_s = \frac{1}{S} \tag{3.2.22}$$

The voltage at the load end ($z = l$) is given by Eqn. (3.2.16) to be

$$V(s) = Ae^{-\gamma \ell} + Be^{-\gamma \ell} \tag{3.2.23}$$

where the propagation constant γ in the s-space is given by equations (3.2.5) to (3.2.12) and the constants A and B are given by equations (3.2.20) and (3.2.21), respectively. Finally, the time-domain response of the output voltage can be obtained by an inverse Laplace transformation of $V(s)$.

Simulation Results

In the results presented below, load capacitance is fixed at 100 fF and with the resistance of the unit step voltage source set equal to 700 Ω unless one of these is the chosen variable. The output voltage is normalized in the sense that it is the ratio of the voltage at the load at a given time t to its value at time $t = \infty$. Resistance and inductance of the interconnection line are kept as $R = 2 \times \rho \times 10^4$ Ω/m and $L = 10^6$ H/m where ρ is the resistivity of the interconnection material. The value of R is for 0.5 μm thickness of the interconnection. The values of the self and mutual capacitances for the system of interconnections can be determined by using the techniques presented in chapter 2.

Figure 3.2.3 shows the normalized output voltages for interconnection lengths of 100 μm and 1 cm. The insert in this figure shows that for "long" interconnections, no output voltage is expected to be observed for some time. Figure 3.2.4 shows the dependence of the delay time on the interconnection length while the dependence of the rise time on the interconnection length is shown in Figure 3.2.5. These figures indicate that for interconnection lengths above 100 μm the delay time and rise time increase significantly whereas these are almost constant below about 100 μm. As a function of the width of the interconnection, the delay time and the rise

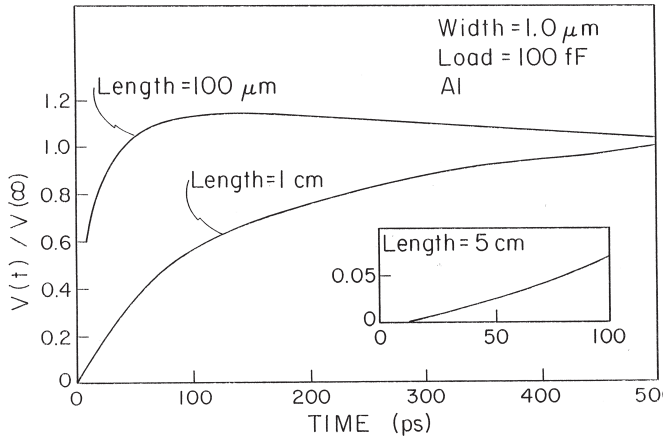


Figure 3.2.3 Normalized output voltages for the interconnection lengths of 100 μm and 1 cm. The insert shows the output voltage for interconnection length of 5 cm

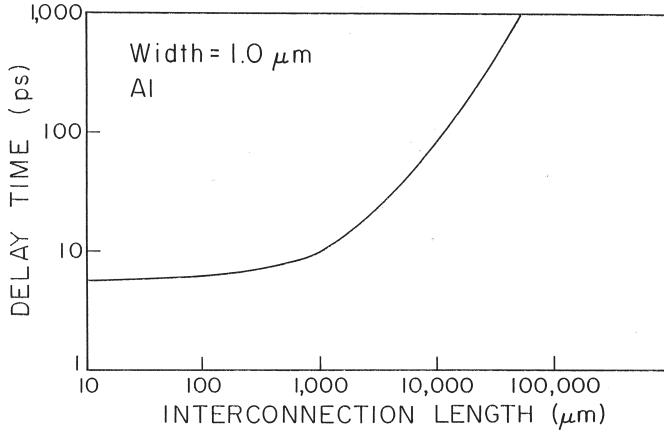


Figure 3.2.4 Dependence of the delay time on the interconnection length

time are shown in the Figures 3.2.6 and 3.2.7, respectively. Figure 3.2.8 shows the normalized output voltages for interconnection widths of 1.0 and 0.1 μm. Figures 3.2.6 and 3.2.7 indicate that the propagation delays decrease when the interconnection width is increased from 0.1 to about 1 μm. For interconnection widths above about 1 μm both the delay time and the rise time increase somewhat. The initial decrease in the transit times below about 1 μm is due to the decreasing line resistance whereas the increase observed above about 1 μm is due to the increasing interconnection

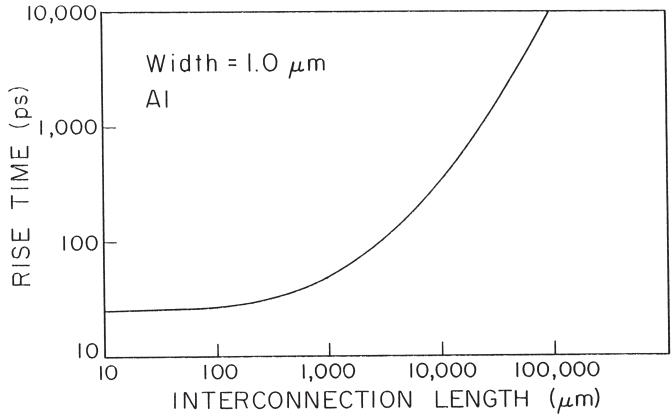


Figure 3.2.5 Dependence of the rise time on the interconnection length

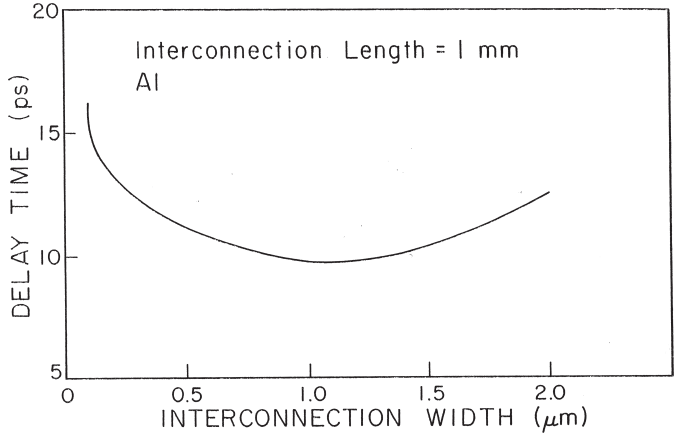


Figure 3.2.6 Dependence of the delay time on the interconnection width

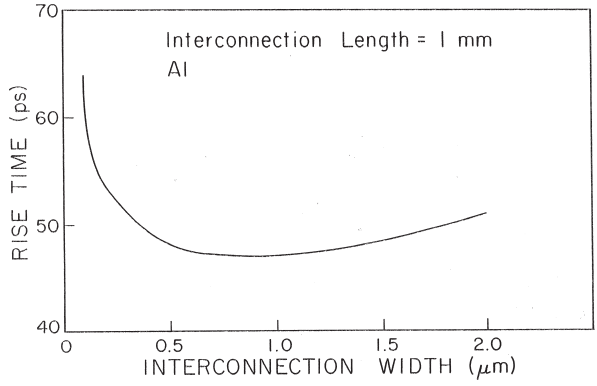


Figure 3.2.7 Dependence of the rise time on the interconnection width

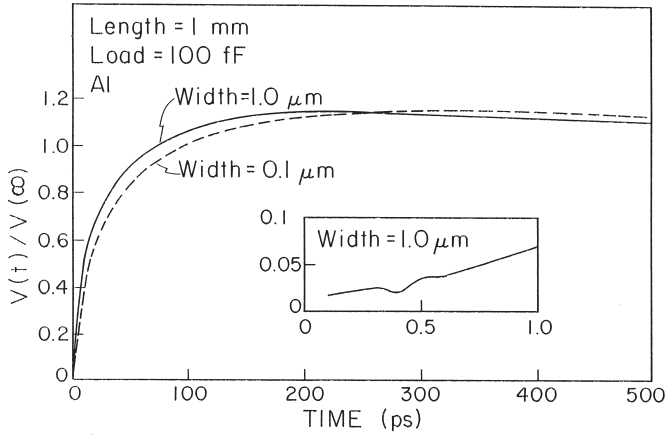


Figure 3.2.8 Normalized output voltages for the interconnection widths of 1.0 and 0.1 μm. The insert shows the output voltage for the interconnection width of 1.0 μm for times less than 1.0 ps

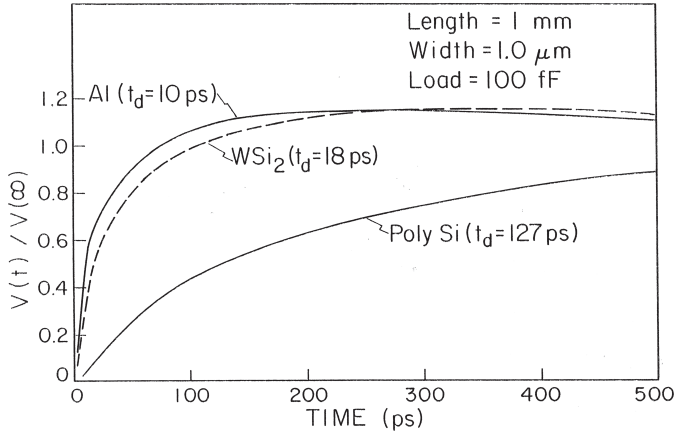


Figure 3.2.9 Normalized output voltages for the interconnection metals of A1, WSi_2, and polysilicon

capacitances. Figure 3.2.9 shows the normalized output voltages when the interconnection metal is aluminum, WSi_2, or polysilicon. These correspond to the interconnection metal resistivities of nearly 3, 30, and 500 μΩ.cm, respectively. It shows that, as the resistivity is increased, the time for the output voltage to reach its steady state value increases as well. The resulting increases in the delay time and the rise time are shown in Figure 3.2.10. Figure 3.2.11 shows the normalized output voltages for the load capacitances of 10 fF and 1 pF indicating that a higher load results in higher delay times, as expected.

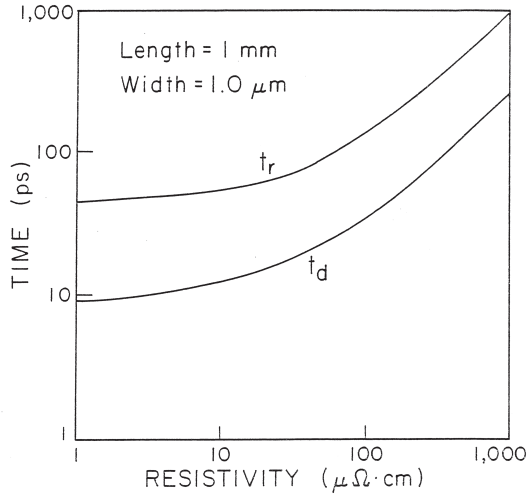


Figure 3.2.10 Dependences of the delay time and the rise time on the interconnection metal resistivity

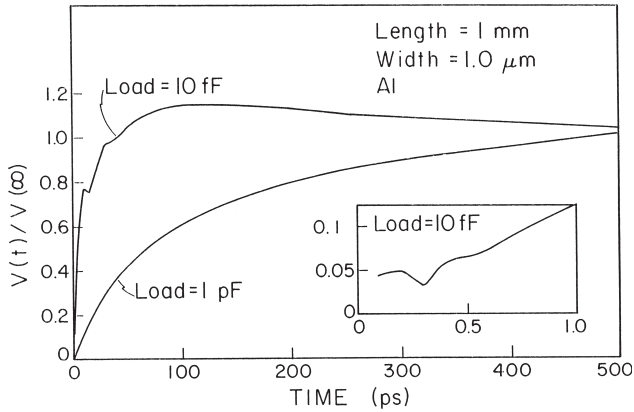


Figure 3.2.11 Normalized output voltages for the load capacitances of 10 fF and 1 pF

3.3 Transmission Line Model for Multilevel Interconnections

In the literature, multiple coupled distributed parameter systems including coupled transmission lines have been analyzed in detail. For example, the normal mode propagation constants, impedances, and eigenvectors for coupled *n*-line structures are derived in matrix form [38–45] and

these properties are available in explicit closed form for two-, three- and four-line systems [45–48]. The coupled line equations can also be used to model the propagation characteristics of interconnections in the high-speed digital circuits. Such a model [13] is presented below.

The Model

Schematic diagram of a general multiple coupled line structure is shown in Figure 3.3.1. The voltages and currents on a lossless n-line system are described by the following transmission line equations:

$$\frac{\partial}{\partial z}\vec{v} = -[L]\frac{\partial}{\partial t}\vec{i} \tag{3.3.1a}$$

$$\frac{\partial}{\partial z}\vec{i} = -[C]\frac{\partial}{\partial t}\vec{v} \tag{3.3.1b}$$

where the vectors

$$\vec{v} = [v_1, v_2, \ldots, v_n]^T$$

and

$$\vec{i} = [i_1, i_2, \ldots, i_n]^T$$

represent voltages and currents in the time domain along the n lines of the coupled structure, the superscript T denotes the transpose and the matrices $[L]$ and $[C]$ are the inductance and capacitance matrices per unit

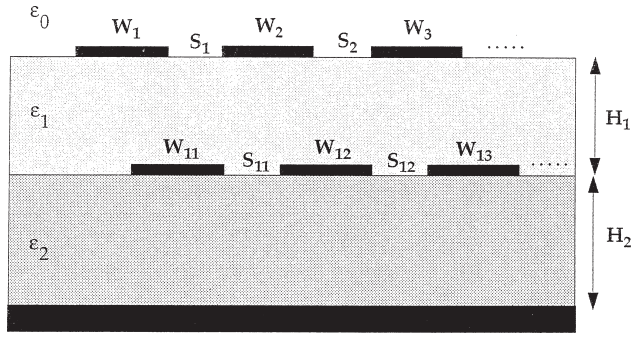


Figure 3.3.1 Cross-sectional view of a multiple coupled line structure [13]. (© 1985 IEEE)

length of the lines. As is well known, $[L]$ is a positive definite matrix while $[C]$ is a hyperdominant matrix.

Now, we can consider equations (3.3.1a) and (3.3.1b) in the frequency domain. If $\hat{V}$ and $\hat{I}$ are the voltage and current vectors in the frequency domain then, for $e^{j(\omega t-\beta z)}$ variation in the time domain, these equations can be easily decoupled to result in the following eigenvalue equations for voltages and currents in the frequency domain:

$$[[L][C]-\lambda[U]]\hat{V} = [0] \tag{3.3.2a}$$

$$[[C][L]-\lambda[U]]\hat{I} = [0] \tag{3.3.2b}$$

where $\lambda = \beta^2/\omega^2$, $[U]$ is the unit matrix and [0] is the null vector. The above equations can be rewritten as:

$$[C]\hat{V} = \lambda[L]^{-1}\hat{V} \tag{3.3.3a}$$

$$[L]\hat{I} = \lambda[C]^{-1}\hat{I} \tag{3.3.3b}$$

In most cases, the dielectric substrates used in the interconnection structures are nonmagnetic, i.e., their magnetic properties are the same as those of free space. For these cases, if $[L_0]$ and $[C_0]$ are the inductance and capacitance matrices for the interconnection structure with the dielectric removed then the inductance matrix for the interconnection structure with the dielectric is given by

$$[L] = [L_0] = \mu_0\varepsilon_0[C_0]^{-1} \tag{3.3.4}$$

Using Eqn. (3.3.4), equations (3.3.3a) and (3.3.3b) can be written in terms of the capacitance matrices only.

If $[M_V]$ and $[M_I]$ denote the voltage and current eigenvector matrices then, using the orthogonality requirement, we have

$$[M_I] = [[M_V]^T]^{-1} \tag{3.3.5}$$

Further, writing

$$\hat{v} = [M_V]\hat{e} \tag{3.3.6a}$$

and

$$\hat{i} = [M_I]\hat{j} \tag{3.3.6b}$$

we can write

$$\begin{bmatrix} \hat{v} \\ \hat{j} \end{bmatrix} = \begin{bmatrix} [M_V] & 0 \\ 0 & [M_V]^T \end{bmatrix} \begin{bmatrix} \hat{e} \\ \hat{i} \end{bmatrix} \tag{3.3.7}$$

Substituting equations (3.3.6a) and (3.3.6b), equations (3.3.1a) and (3.3.1b) can be rewritten as

$$\frac{\partial}{\partial z}\hat{e} = -diag[L_k]\frac{\partial}{\partial t}\hat{j} \tag{3.3.8a}$$

$$\frac{\partial}{\partial z}\hat{j} = -diag[C_k]\frac{\partial}{\partial t}\hat{e} \tag{3.3.8b}$$

where diag[Lk] and diag[C_k] are the diagonal matrices with elements given by

$$L_k = [M_V]^{-1}[L]\left[[M_V]^T\right]^{-1} = \frac{1}{u_k^2 C_k} \tag{3.3.9a}$$

$$C_k = [M_V]^T[C][M_V] \tag{3.3.9b}$$

where uk is the phase velocity of the kth mode. The characteristic impedance of the kth mode is given by

$$Z_k = \left[\frac{L_k}{C_k}\right]^{1/2} \tag{3.3.10}$$

For a general n-line system, equations (3.3.6) to (3.3.8) lead to an equivalent circuit model shown in Figure 3.3.2. In other words, the model shown in Figure 3.3.2 is a circuit that is the solution of the coupled transmission-line equations (3.3.1a) and (3.3.1b).

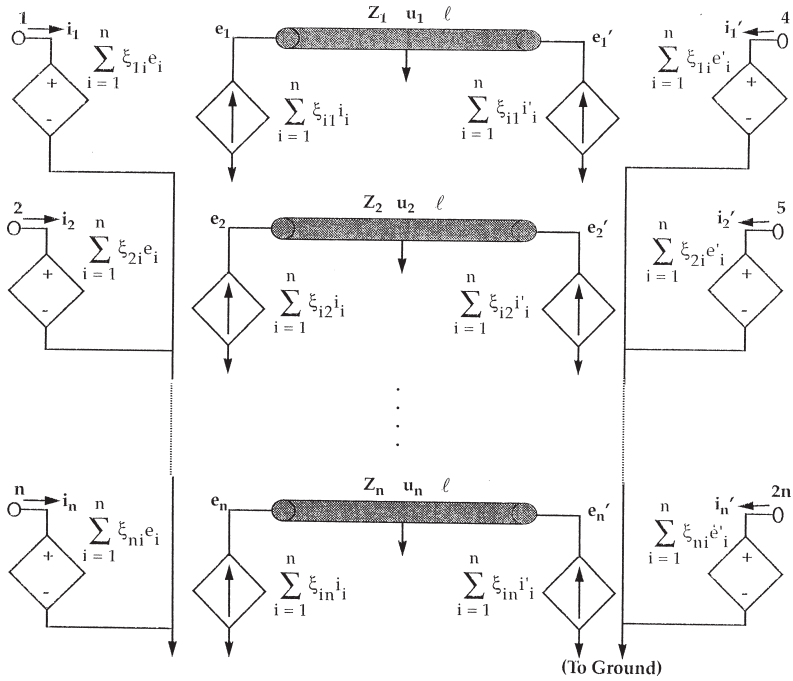


Figure 3.3.2 Equivalent circuit model for the multiple coupled lines [13]. (© 1985 IEEE)

Simulation Results

Because all the model elements shown in Figure 3.3.2 are available in the CAD program called SPICE, the simulation results given below can be obtained by using SPICE [13]. For an asymmetric coupled two-line system (also called a four-port), the SPICE model, model parameters, and its step response are shown in Figure 3.3.3(a–e). The step responses for characteristic nonmode converting terminations $Z_1 = 48.6\ \Omega$ and $Z_2 = 73.4\ \Omega$ are shown in Figure 3.3.3(c and d) and, for the sake of comparison, the step response of the same structure terminated in 50 Ω resistances is also included in Figure 3.3.3(e and f). Figure 3.3.3 shows that mismatch in normal mode phase velocities results in a finite pulse at the isolated port for both the nonmode terminations and the 50 Ω terminations.

In order to illustrate the application of the model to nonlinear terminations, it has been applied to a three-line system terminated in logic gates shown in Figure 3.3.4(a). When the input signal is applied to the

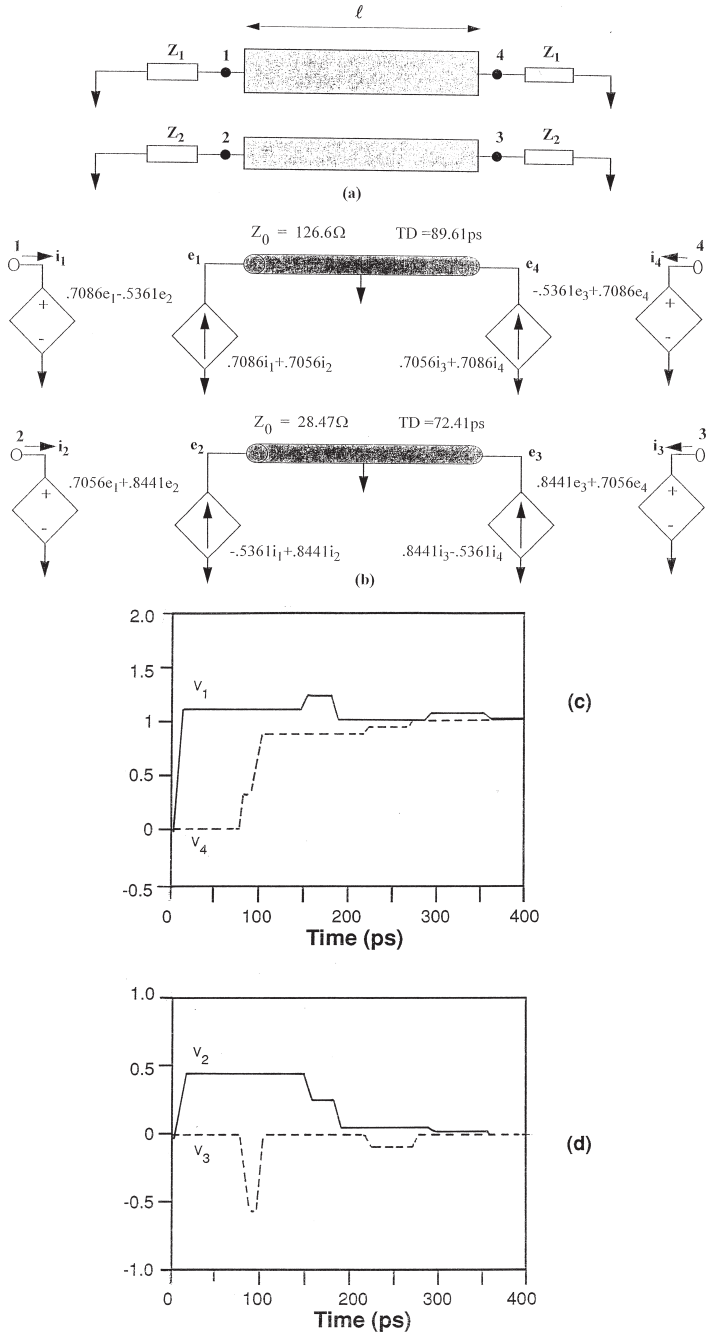


Figure 3.3.3 Step response of the asymmetric coupled microstrip four-port. (a) Schematic diagram of the coupled lines; (b) The equivalent SPICE model for $W_1/H = 2W_2/H = 0.46$, $S/H = 0.038$, and $\varepsilon_r = 9.8$; (c) and (d) Step response for characteristic nonmode converting terminations $Z_1 = 46.8\ \Omega$ and $Z_2 = 73.4\ \Omega$; (e) and (f) Step response for 50 Ω terminations [13]. (© 1985 IEEE)

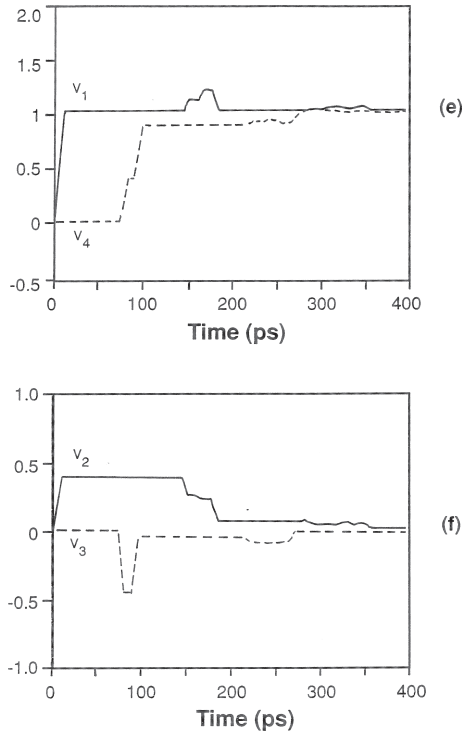


Figure 3.3.3 *(*continued*)*

gate on the outside lines, the step response results at all other ports are shown in Figure 3.3.4(b–d). The effects of interactions among the gates and the interconnections are apparent in the results. The rise time and the gate propagation delays correspond to subnanosecond performance.

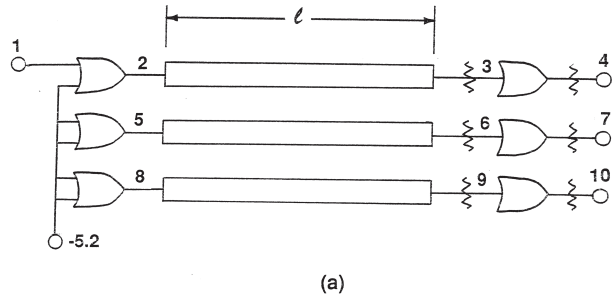


Figure 3.3.4 Step response of a three-line structure terminated in ECL-OR gates on the alumina substrate and with W/H = S/H = 1. The termination symbols denote 50 Ω consisting of two resistors in parallel—81 Ω to ground and 130 Ω to −5.2 V [13]. (© 1985 IEEE)

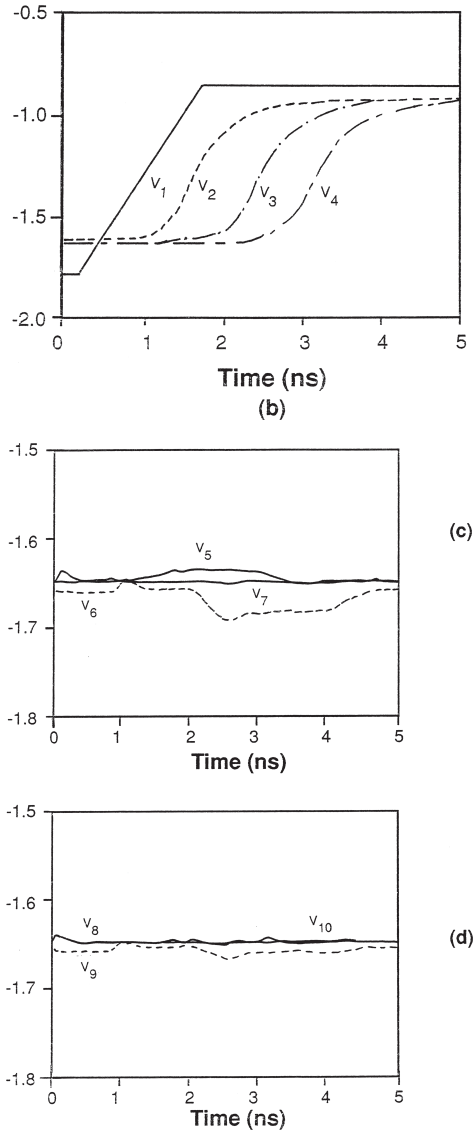


Figure 3.3.4 (continued)

3.4 Modeling of Parallel and Crossing Interconnections

Now, a model of the parallel and crossing interconnections in terms of coupled lumped distributed lossy networks [14] will be presented. This method is an extension of that presented in the last section for lossless parallel interconnections.

The Model

A schematic diagram of the interconnections analyzed here is shown in Figure 3.4.1. The interconnection lines at the same or different levels that are parallel to each other are modeled as lossy parallel coupled transmission lines. The coupling between the crossing interconnections in adjacent levels is assumed to be in the immediate vicinity of the crossover and has been modeled as a lumped element. Therefore, the crossing interconnections have been modeled as lumped distributed circuits.

In terms of the normal propagation modes, the voltages and currents in an n-line system are described by the following transmission line equations:

$$\frac{\partial}{\partial z}\vec{v} = -\left[R\right]\vec{i} - \left[L\right]\frac{\partial}{\partial t}\vec{i} \tag{3.4.1}$$

$$\frac{\partial}{\partial z}\vec{i} = -\left[G\right]\vec{v} - \left[C\right]\frac{\partial}{\partial t}\vec{v} \tag{3.4.2}$$

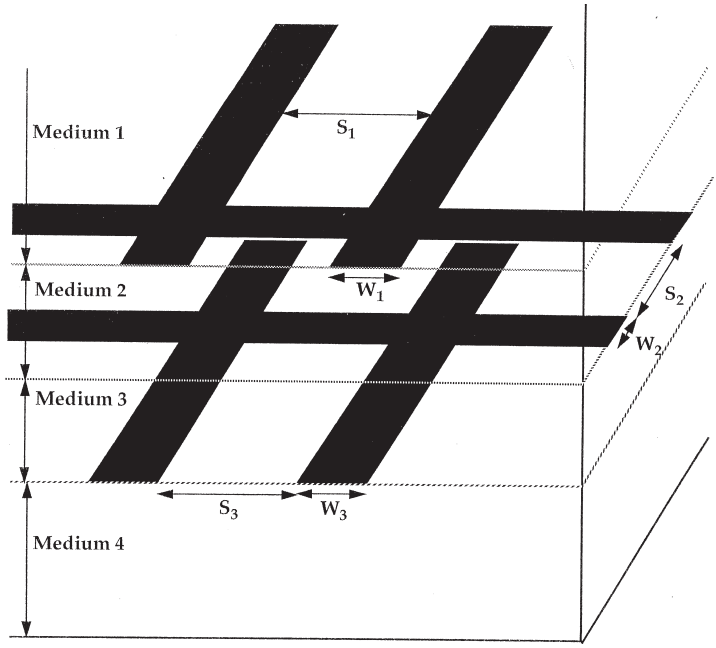


Figure 3.4.1 Schematic diagram of the parallel and crossing interconnections modeled in this section [14]. (© 1987 IEEE)

where the vectors

$$\hat{v} = [v_1, v_2, \ldots, v_n]^T$$

and

$$\hat{i} = [i_1, i_2, \ldots, i_n]^T$$

represent voltages and currents in the time domain along the n lines of the coupled structure, the superscript T denotes the transpose and the matrices $[R]$, $[L]$, $[G]$, and $[C]$ are the series resistance, series inductance, shunt conductance, and shunt capacitance matrices per unit length of the lines, respectively.

Now, we can consider equations (3.4.1) and (3.4.2) in the frequency domain. If $\hat{V}$ and $\hat{I}$ are the voltage and current vectors in the frequency domain then, for $e^{j\omega t-\gamma z}$ variation in the time domain, these equations can be easily decoupled to result in the following eigenvalue equations for voltages and currents in the frequency domain:

$$\left[\left[Z_S\right]\left[Y_{SH}\right] - \lambda\left[U\right]\right]\hat{V} = \left[0\right] \tag{3.4.3}$$

$$\left[\left[Y_{SH}\right]\left[Z_S\right] - \lambda\left[U\right]\right]\hat{I} = \left[0\right] \tag{3.4.4}$$

where $[Z_S] = [R] + j\omega[L]$, $[Y_{SH}] = [G] + j\omega[C]$, $\lambda = -\gamma^2$, $[U]$ is the unit matrix, and $[0]$ is the null vector. Equations (3.4.3) and (3.4.4) represent the generalized matrix eigenvalue and eigenvector problems. If $[M_v]$ denotes the complex eigenvector matrix associated with the characteristic matrix $[Z_S][Y_{SH}]$ then, following the same procedure as in the last section, it can be shown that the voltage eigenvector $\hat{e}$ and the current eigenvector $\hat{j}$ are solutions of the following set of decoupled equations:

$$\frac{d}{dz}\hat{e} = -diag\left[\gamma_k / y_k\right]\hat{j} \tag{3.4.5}$$

$$\frac{d}{dz}\hat{e} = -diag\left[\gamma_k / y_k\right]\hat{j} \tag{3.4.6}$$

where γ_k is the propagation constant of the kth mode equal to the square root of the kth eigenvalue of $[Z_S][Y_{SH}]$, y_k is the characteristic admittance

of the kth mode equal to the corresponding element of the diagonal matrix $[Y_k]$ given by

$$\left[Y_k\right] = \left[M_v\right]^{-1}\left[Y_{SH}\right]\left[M_v\right] \tag{3.4.7}$$

and

$$\begin{bmatrix}\hat{V}\\ \hat{I}\end{bmatrix} = \begin{bmatrix}\left[M_v\right] & \left[0\right]\\ \left[0\right] & \left[\left[M_v\right]^T\right]^{-1}\end{bmatrix}\begin{bmatrix}\hat{e}\\ \hat{j}\end{bmatrix} \tag{3.4.8}$$

For a system of n lossy parallel interconnection lines, the above equations lead to the $2n$-port circuit model shown in Figure 3.4.2 which consists of lossy uncoupled lines with a modal decoupling network at the input end and a complementary coupling network at the output end. The values of the linear real or complex dependent sources in the network are given by the elements of the voltage eigenvector matrix $[M_v]$. The model

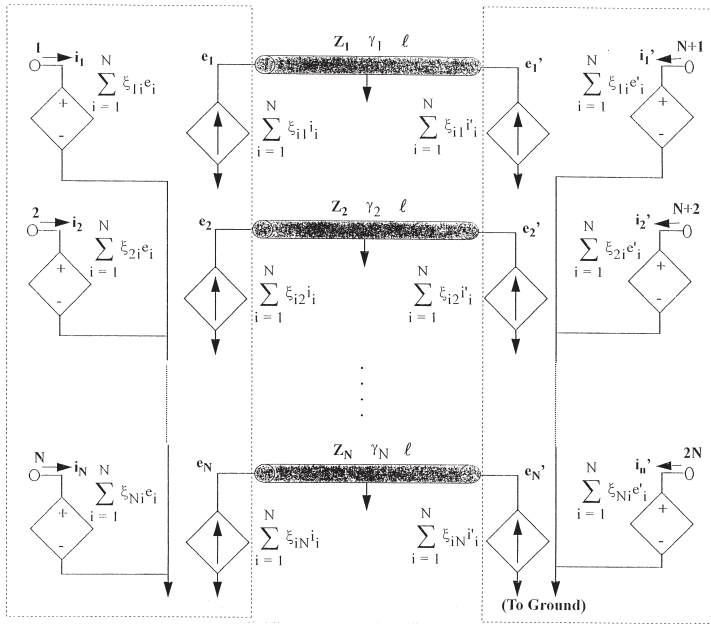


Figure 3.4.2 2n-port circuit model representing the n parallel lossy coupled interconnections [14]. (© 1987 IEEE)

presented in Figure 3.4.2 differs from that presented in the last section for the lossless lines in that, in the present case, the uncoupled lines are lossy having complex impedances and propagation constants and that the dependent sources are generally not in phase with the independent variables. It should be noted that, given the frequency-dependent behaviors of the impedances and propagation constants of these lossy lines, they can be represented as 2-ports consisting of lossless lines and lumped elements as shown in Figure 3.4.3 for the skin-effect losses. The time-domain response of the interconnection lines can be calculated directly by using the model for linear as well as nonlinear terminations.

Simulation Results

The simulation results presented below are obtained by modeling the multiple coupled lumped distributed parameter networks representing the interconnections terminated in passive or active elements on the CAD program called SPICE [14]. The parasitic elements for the interconnections have been calculated by the network analog method applied to the

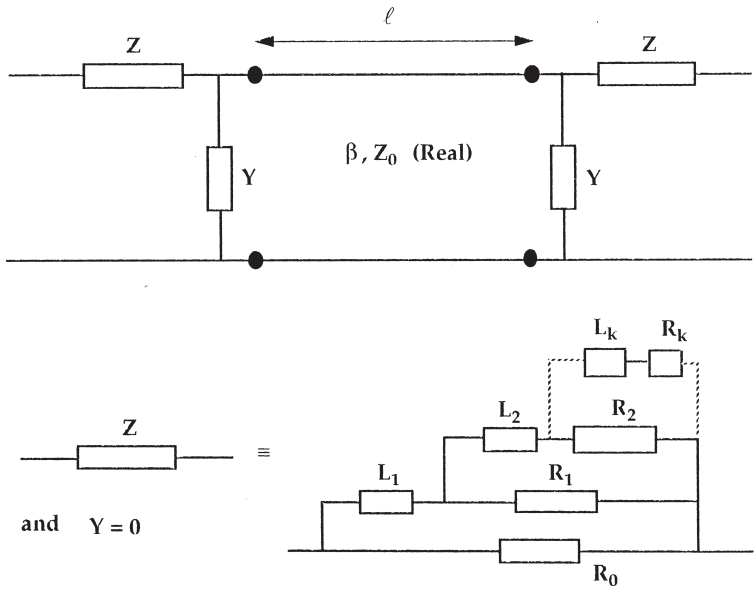


Figure 3.4.3 Model for a single lossy uncoupled line with frequency-dependent skin effect losses [14]. (© 1987 IEEE)

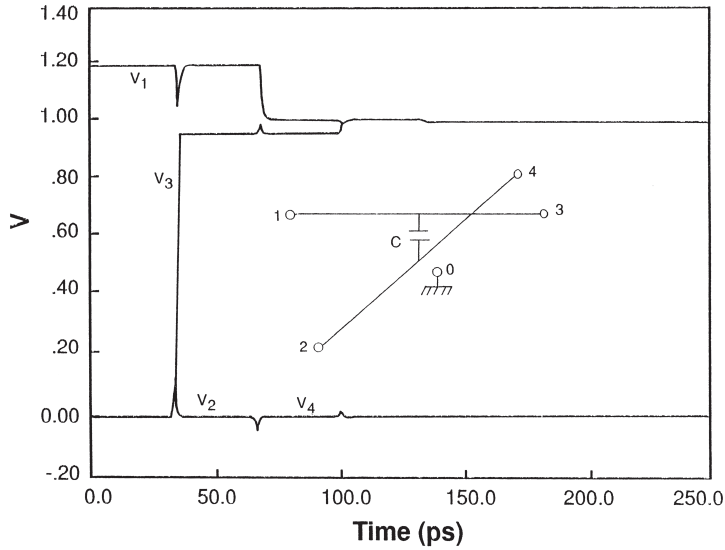


Figure 3.4.4 Step response for a pair of crossing lines in the SiO_2 medium. The schematic diagram of the interconnections is shown in the inset. The line widths and the separation are 10 μm each, length is 3 mm, and the terminations are 100 Ω each [14]. (© 1987 IEEE)

three-dimensional interconnection structures in layered lossy media including the frequency-dependent coupling between the crossing lines.

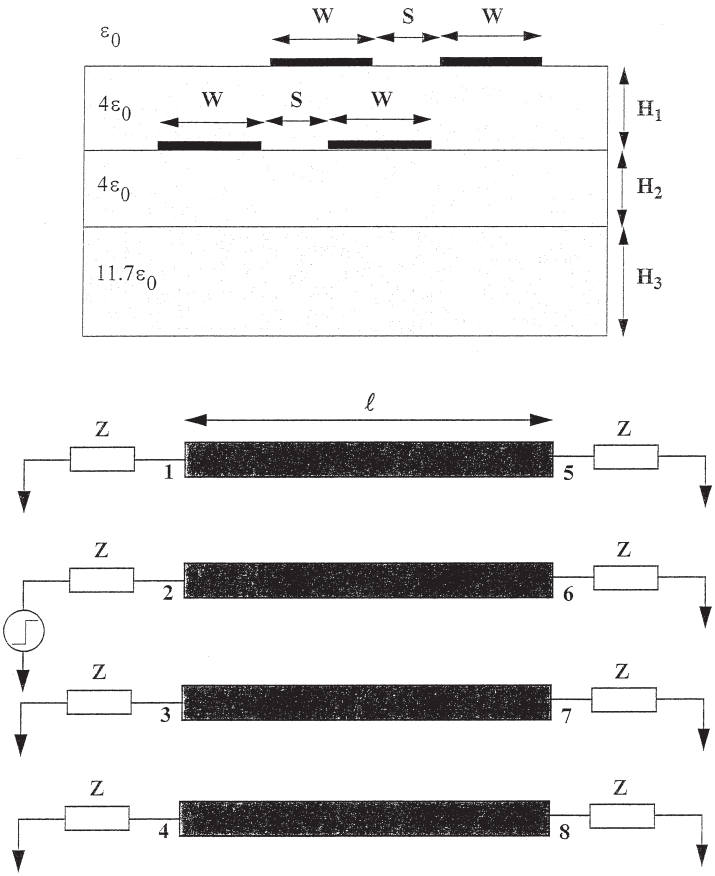
The step response for a pair of crossing lines in the SiO_2 medium is shown in Figure 3.4.4. The schematic of the interconnections is shown in the inset. The line widths and the separation are 10 μm each, length is 3 mm, and the terminations are 100 Ω each.

For a two-level interconnection structure consisting of four lines in the Si-SiO_2 system, the SPICE results for the step response are shown in Figure 3.4.5. The geometry of the interconnection structure and its schematic diagram are shown in Figure 3.4.5(a) and (b), respectively with $W = H_1 = H_2 = 2D = S/2 = 5$ μm, $H_3 = 250$ μm, $l = 10$ mm, and $Z = 100$ Ω. The SPICE model parameters for this case can be obtained from Figure 3.4.2 with $N = 4$ to be:

Normal mode line 1: Impedance $Z_1 = 11.23$ Ω; delay $T_d = 54.24$ ps;
Normal mode line 2: Impedance $Z_2 = 55.16$ Ω; delay $T_d = 59.98$ ps;
Normal mode line 3: Impedance $Z_3 = 49.79$ Ω; delay $T_d = 75.69$ ps;
Normal mode line 4: Impedance $Z_4 = 179.7$ Ω; delay $T_d = 68.79$ ps;

and the dependent sources in the SPICE subcircuit denoted by ξ_{jk} in Figure 3.4.2 are given by the elements of the following voltage eigenvector matrix:

$$\left[M_v\right] = \begin{bmatrix} 2.0 & 1.01726 & 1.02429 & 0.050117 \\ -1.86303 & 1.09345 & 0.99017 & -0.077621 \\ 0.54591 & 0.16732 & 1.40569 & 0.415290 \\ -0.43182 & 0.22045 & 1.39422 & -0.424816 \end{bmatrix}$$



(a)

***Figure 3.4.5** SPICE results for the step response for a two-level interconnection structure consisting of four lines in the Si-SiO$_2$ system. The geometry of the interconnection structure and its schematic diagram are shown in (a) with W = H$_1$ = H$_2$ = 2D = S/2 = 5 μm, H$_3$ = 250 μm, length = 10 mm, and Z = 100 Ω [14]. (© 1987 IEEE)*

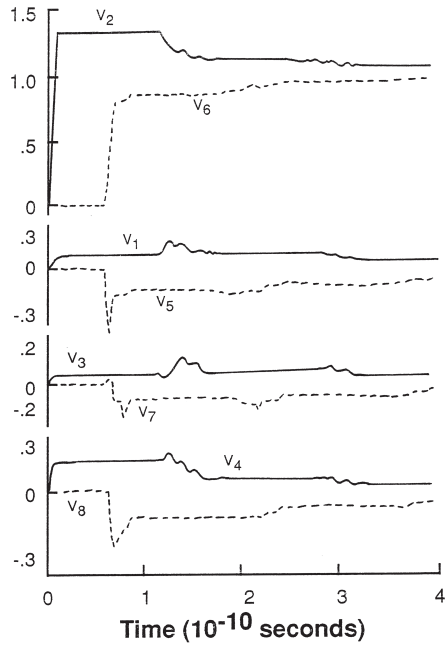


Figure 3.4.5 *(*continued*)*

The SPICE results for the step response of coupled crossing lines at adjacent levels in the SiO_2 medium, including the effects of distributed as well as lumped couplings, are shown in Figure 3.4.6. For these results, line lengths are 3 mm, separation is 10 μm, the layer thickness is 7 μm, and the terminations are 100 Ω each.

Figure 3.4.7 shows the schematic, the SPICE model, and the step response of a pair of coupled interconnections on the semi-insulating GaAs substrate including the skin-effect losses. The losses are modeled in terms of the RL circuits (see Figure 3.4.3) represented by the impedances Z_1 and Z_2 in the inset of Figure 3.4.7. Other parameters are: $W = S = 10$ μm, $T = 2$ μm, $H_1 = 2$ μm, $H_2 = 100$ μm, $l = 2$ mm, and the terminating impedances are 100 Ω each.

The results for a general lossy layered structure consisting of three interconnection lines on a GaAs system including the frequency-dependent skin-effect losses and the dielectric losses are shown in Figure 3.4.8. The interconnection structure cross section and its schematic

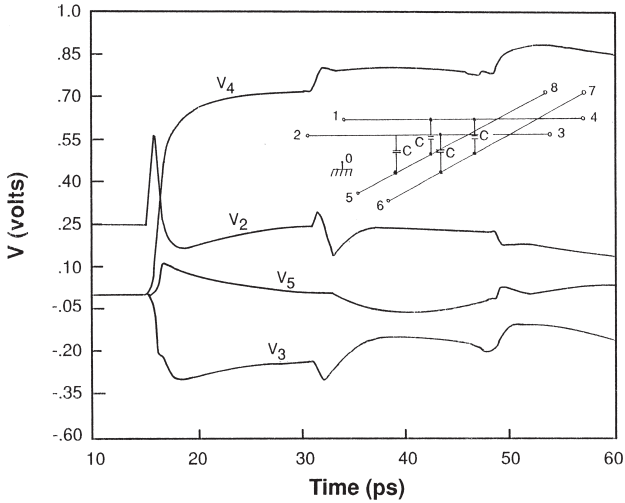


Figure 3.4.6 SPICE results for the step response of coupled crossing lines at adjacent levels in the SiO_2 medium. Line lengths are 3 mm, separation is 10 μm, the layer thickness is 7 μm, and the terminations are 100 Ω each [14]. (© 1987 IEEE)

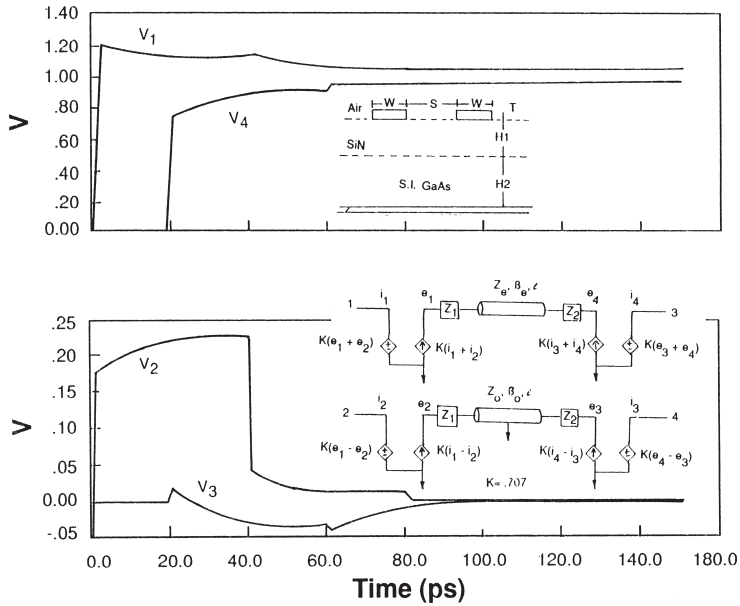


Figure 3.4.7 The schematic diagram, the SPICE model, and the step response of a pair of coupled interconnections on the semi-insulating GaAs substrate including the skin effect losses. Parameters are W = S = 10 μm, T = 2 μm, H_1 = 2 μm, H_2 = 100 μm, length = 2 mm, and the terminating impedances are 100 Ω each [14]. (© 1987 IEEE)

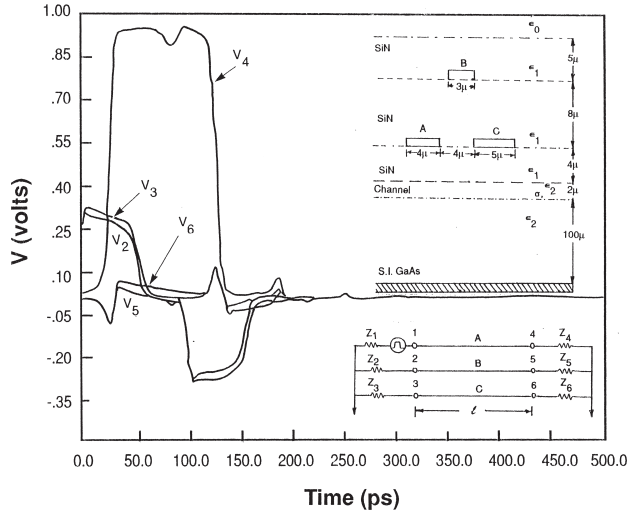


Figure 3.4.8 The step response for a general lossy layered structure consisting of three interconnection lines on a GaAs system including the frequency-dependent skin effect losses and the dielectric losses. The interconnection structure cross-section and its schematic diagram are shown in the insets. Input signal is a 100 ps pulse with $Z_1 = 0$ and all other Z's are 100 Ω each [14]. (© 1987 IEEE)

diagram are shown in the insets. Input signal is a 100 ps pulse with $Z_1 = 0$ and all other Z's are 100 Ω each.

3.5 Modeling of Very-High-Frequency Losses in an Interconnection

For very high-speed VLSI circuits, several phenomena such as reflections at discontinuities, substrate losses, conductor losses, geometric dispersion, and inductive effects become important and should be included in the interconnection delay models. The interconnection line is dispersive because the propagation factor of the corresponding transmission line varies nonlinearly with the width of the line. This is further caused by the geometric dispersion in the microstrip line reflected in the frequency dependence of the effective dielectric constant, by the finite conductivity of the silicon substrate and by the frequency dependence (due to skin effect) of the resistance of the metal conductor.

Here, a model of pulse propagation in an isolated microstrip interconnection on Si substrate including several of the high-frequency effects [34] is presented. Quasi-TEM mode propagation is assumed and the analysis is valid for frequencies up to the lowest frequency at which non-TEM modes can propagate in the microstrip interconnection. This limit corresponds to the cutoff frequency for the surface wave mode [35] which is inversely related to the substrate thickness and is 50 GHz for a silicon wafer of 450 μm thickness.

The Model

A schematic diagram of the microstrip interconnection on the Si substrate is shown in Figure 3.5.1. We assume that the dielectric constant ε_r of the substrate is real and constant which is valid in Si for frequencies up to 10^{13} Hz. Furthermore, we include the effect of the insulator (the oxide layer) by treating it as an open circuit at zero frequency and as a short circuit at all other frequencies. This assumption is valid because, even at 100 MHz, the impedance introduced by the capacitance of the oxide layer is negligible as long as its thickness (t_0) is much smaller than the substrate thickness (h). As stated above, we also assume quasi-TEM mode propagation which is justified at the substrate resistivities and frequencies used in this section. This can be further justified by finding the ratio of the

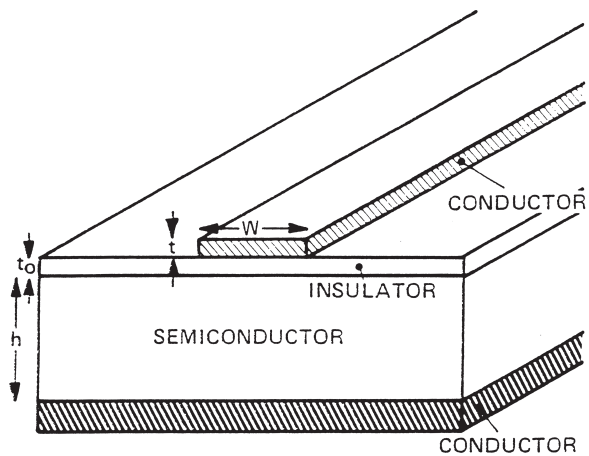


Figure 3.5.1 Schematic diagram of a microstrip interconnection line on silicon substrate [49].

longitudinal and tangential electric fields of the mode and verifying that this ratio is much smaller than one. Using the parallel-plate model, this ratio is given by

$$\frac{|E_z|}{|E_x|} = \frac{2\varepsilon_r\varepsilon_0}{\sigma\delta\mu_0} \quad ; \qquad t \gg \delta \tag{3.5.1a}$$

$$\frac{|E_z|}{|E_x|} = \frac{\varepsilon_r\varepsilon_0}{\sigma t\mu_0} \quad ; \qquad t \ll \delta \tag{3.5.1b}$$

where t is the conductor thickness, σ is the conductivity of the conductor and δ is the skin depth in the conductor. For the results presented here, this ratio is much smaller than one. In fact, it is the largest (= 0.1) for 0.5 μm thick poly-Si line (resistivity = 500 μΩ.cm) for frequencies below 10^{12} Hz.

For a given voltage waveform $v(0, t)$ at one end of the microstrip, we need to find the voltage waveform $v(z, t)$ at any point z along the microstrip line. This can be accomplished by carrying out the Fourier decomposition of $v(0,t)$, multiplying the various terms by the corresponding propagation factors and then performing the inverse Fourier transformation, i.e.,

$$v(z, t) = F^{-1}[F\{v(0, t)\} \times e^{-(\alpha + j\beta)z}] \tag{3.5.2}$$

where α is the attenuation constant, β is the propagation constant, F denotes Fourier transformation and F^{-1} represents the inverse Fourier transformation.

Using the symbols shown in Figure 3.5.1, the effective dielectric constant ε_{eff} and the characteristic impedance Z_0 at zero frequency have been calculated by Schneider [51] to be

$$\varepsilon_{eff} = 0.5\left[(\varepsilon_r + 1) + \frac{(\varepsilon_r - 1)}{\sqrt{\left(1 + 10\frac{h}{w}\right)}}\right] \tag{3.5.3}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \times ln\left[\frac{8h}{w} + \frac{w}{4h}\right]; \text{w<h}$$

$$Z_0 = \frac{120\pi}{\left[\left\{\frac{w}{h} + 2.42 - \frac{0.44h}{w} + \left(1 - \frac{h}{w}\right)^6\right\}\sqrt{\varepsilon_{eff}}\right]}; \text{w>h} \quad (3.5.4)$$

The maximum relative error in expressions (3.5.3) and (3.5.4) is less than 2 percent; however, corrections [52] are required for $(t/h) > 0.005$. The expression for ε_{eff} at high frequencies has been derived by Yamashita et al. [53] and is given by:

$$\sqrt{\varepsilon_{eff}(f)} = \sqrt{\varepsilon_{eff}(0)} + \frac{[\sqrt{\varepsilon_r} - \sqrt{\varepsilon_{eff}(0)}]}{(1 + 4F^{-1.5})} \quad (3.5.5)$$

where

$$F \equiv \frac{4fh}{c}\sqrt{(\varepsilon_r - 1)}\left[0.5 + \left\{1 + 2\log\left(1 + \frac{w}{h}\right)\right\}^2\right]$$

f is the frequency and c is the speed of light in vacuum. The error in the expression (3.5.5) is less than 1 percent.

For a lossless material, the propagation constant β_0 is given by

$$\beta_0 = \frac{2\pi f\sqrt{\varepsilon_{eff}}}{c} \quad (3.5.6)$$

However, for a conductor of finite resistivity and substrate material of finite conductivity, the attenuation should be considered. At low frequencies where the current distribution in the conductor can be considered uniform, the conductor loss factor α_c is given in nepers by

$$\alpha_c = \frac{\rho_c}{2wtZ_0} \quad (3.5.7)$$

where ρ_c is the resistivity of the metal. However, at high frequencies where the current distribution is not uniform due to the skin effect, the conductor loss is given by [54]:

$$\alpha_c = \left[\frac{R_s}{2\pi Z_0 h}\right]\left[1 - \left(\frac{w'}{4h}\right)^2\right]\left[1 + \frac{h}{w'} + \frac{h\left\{\ln\left(\frac{4\pi w}{t}\right) + \frac{t}{w}\right\}}{\pi w'}\right]; \frac{w}{h} < \frac{1}{2\pi}$$

$$\alpha_c = \left[\frac{R_s}{2\pi Z_0 h}\right]\left[1-\left(\frac{w'}{4h}\right)^2\right]\left[1+\frac{h}{w'}+\frac{h\left\{\ln\left(\frac{4h}{t}\right)-\frac{t}{h}\right\}}{\pi w'}\right]; \frac{1}{2\pi} < \frac{w}{h} < 2$$

$$\alpha_c = \frac{[R_s/(Z_0 h)]}{\left[\frac{w'}{h}+\frac{2}{\pi}ln\left\{2\pi e\left(0.94+\frac{w'}{2h}\right)\right\}\right]^2} \times \left[\frac{w'}{h}+\frac{\left(\frac{w'}{\pi h}\right)}{\left(0.94+\frac{w'}{2h}\right)}\right]$$

$$\times\left[1+\frac{h}{w'}+\frac{h\left\{ln\left(\frac{2h}{t}\right)-\frac{t}{h}\right\}}{\pi w'}\right]; \frac{w}{h} > 2 \qquad (3.5.8)$$

where μ is the permeability of the metal, $R_s \equiv \sqrt{(\pi f \mu \rho_c)}$ and

$$w' = w + \frac{t}{\pi}\left[1+ln\left(\frac{4\pi w}{t}\right)\right]; \frac{w}{h} < \frac{1}{2\pi}$$

$$w' = w + \frac{t}{\pi}\left[1+ln\left(\frac{2h}{t}\right)\right]; \frac{w}{h} < \frac{1}{2\pi}$$

The dielectric loss α_d caused by the nonzero conductivity of the substrate has been derived by Welch and Pratt [55] and is given by

$$\alpha_d = \frac{60\pi\sigma_s(\varepsilon_{eff}-1)}{(\varepsilon_r-1)\sqrt{\varepsilon_{eff}}} \qquad (3.5.9)$$

where σ_s is the conductivity of the substrate. For a 50 Ω, 0.5 μm thick aluminum microstrip line on a 450 μm thick Si wafer of resistivity 100 Ω.cm, the dependences of the conductor loss, dielectric loss, and line loss on frequency in the range 10^8 to 10^{13} Hz are shown in Figure 3.5.2.

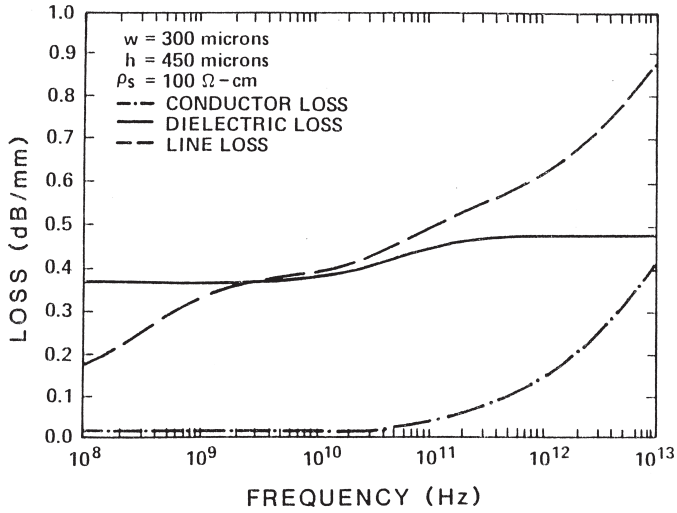
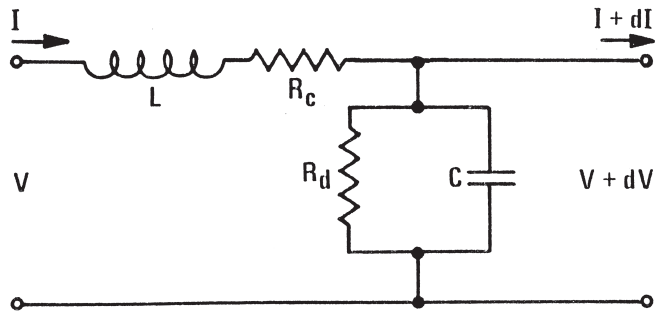


Figure 3.5.2 Dependences of the conductor loss, dielectric loss, and the line loss on frequency [49].

Circuit diagram and circuit equations for the transmission line model of the microstrip interconnection are given in Figure 3.5.3 where L and C denote the inductance and capacitance per unit length for the lossless



$$\frac{dV}{dZ} = -L\frac{dI}{dt} - R_c I$$

$$\frac{dI}{dZ} = -C\frac{dV}{dt} - \frac{V}{R_d}$$

$$V, I \propto e^{(\alpha + i\beta) Z} e^{iwt}$$

Figure 3.5.3 Circuit diagram and circuit equations for the transmission line model of the microstrip interconnection [49].

line, and R_c and R_d denote the resistances per unit length introduced by the conductor resistance and the substrate conductance. The circuit equations can be solved to yield the following expressions for the general attenuation constant α and propagation constant β:

$$\alpha = \sqrt{\frac{(-f_1 + \sqrt{f_2})}{2}} \tag{3.5.10a}$$

$$\beta = \sqrt{\frac{(f_1 + \sqrt{f_2})}{2}} \tag{3.5.10b}$$

where

$$f_1 = \omega^2 LC - \frac{R_c}{R_d}$$

$$f_2 = \left[\omega^2 LC + \left(\frac{R_c}{Z_0}\right)^2\right]\left[\omega^2 LC + \left(\frac{Z_0}{R_d}\right)^2\right] \tag{3.5.11}$$

with $Z_0 = (L/C)^{0.5}$. For low-loss conditions, the circuit model of Figure 3.5.3 yields:

$$\alpha_c = \frac{R_c}{2Z_0}$$

$$\alpha_d = \frac{Z_0}{2R_d}$$

$$\beta_0 = \omega\sqrt{LC} \tag{3.5.12}$$

Equations (3.5.11) and (3.5.12) can be combined to rewrite f_1 and f_2 in terms of β_0, α_c and α_d as:

$$f_1 = \beta_0^2 - 4\alpha_c\alpha_d$$

$$f_2 = (\beta_0^2 + 4\alpha_c^2)(\beta_0^2 + 4\alpha_d^2) \tag{3.5.13}$$

Then equations (3.5.6) to (3.5.9) can be combined with equations (3.5.10) and (3.5.13) to obtain α and β for all loss conditions. If α_c and

α_d are small as compared to β_0 as will be the case under low-loss conditions then α and β are given by

$$\alpha = \alpha_c + \alpha_d$$

$$\beta = \sqrt{(\alpha_c - \alpha_d)^2 + \beta_0^2} \tag{3.5.14}$$

Simulation Results

The simulation results are obtained for two input high-speed logic waveforms consisting of square-wave and exponential pulses. The input square-wave pulses are of 50 ps duration with 12 ps rise and fall times. The input exponential pulses are of the form

$$v(t) = e^{-(t/\tau_1)}[1 - e^{(-t/\tau_2)}] \tag{3.5.15}$$

Input pulses $v_{sw}(0, t)$ and $v_{ex}(0, t)$ with finite rise and fall times can be produced by applying ideal square-wave and exponential pulses to the circuits shown in Figure 3.5.4. By choosing the circuit parameters in Figure 3.5.4, a variety of pulses can be obtained. The Fourier transforms of the input square-wave pulses are given by

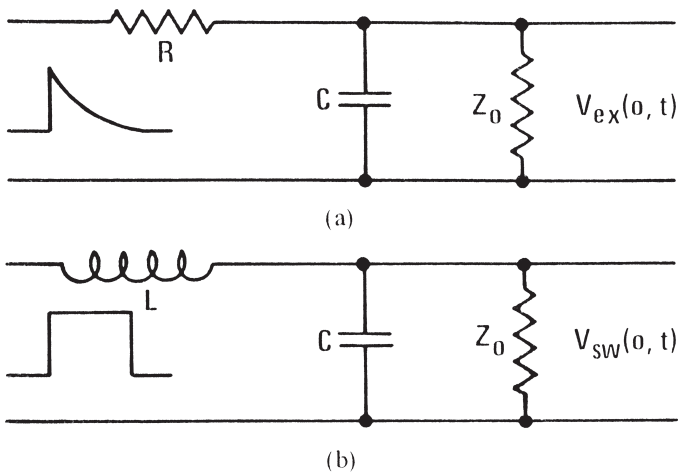


Figure 3.5.4 Circuits used to produce the (a) exponential and (b) square-wave input pulses for the simulation results presented in this section [49].

$$V_{sw}(0,f) = \left[\frac{1-e^{-(j\omega\tau_1)}}{j\omega}\right]\left[\frac{1}{\left(1+j\omega\tau_2-\dfrac{\omega^2}{\omega_1^2}\right)}\right] \tag{3.5.16}$$

where

$$\omega_1^2 = \frac{1}{LC}$$

and

$$\tau_2 = \frac{L}{Z_0}$$

The Fourier transforms of the input exponential pulses are given by

$$V_{ex}(0,f) = \left[\frac{1}{j\omega+\dfrac{1}{\tau_1}}\right]\left[\frac{1}{1+j\omega\tau_2+\dfrac{\tau_2}{\tau_1}}\right] \tag{3.5.17}$$

where

$$\tau_1 = Z_0 C$$

and

$$\tau_2 = RC$$

As stated earlier, the voltage response $v(z, t)$ at a distance z along the mi crostrip line are obtained by multiplying the Fourier transform of the input waveform (at $z = 0$) by the propagation factor $\exp[(\alpha + j\beta)z]$ and then taking the inverse Fourier transform.

The dependences of the characteristic impedance on frequency for two microstrips of widths 10 μm and 300 μm on Si wafer of thickness 450 μm are shown in Figure 3.5.5. This figure shows that the region of geometric dispersion extends from 10 GHz to 300 GHz and that this effect is more pronounced for the narrow line width of 10 μm. Figure 3.5.6 shows the line losses versus frequency for microstrip lines made of aluminum, tungsten, WSi_2, and poly-Si of widths 10 μm and 300 μm on two substrates with resistivities of 10 and 100 Ω.cm. The dependences of the

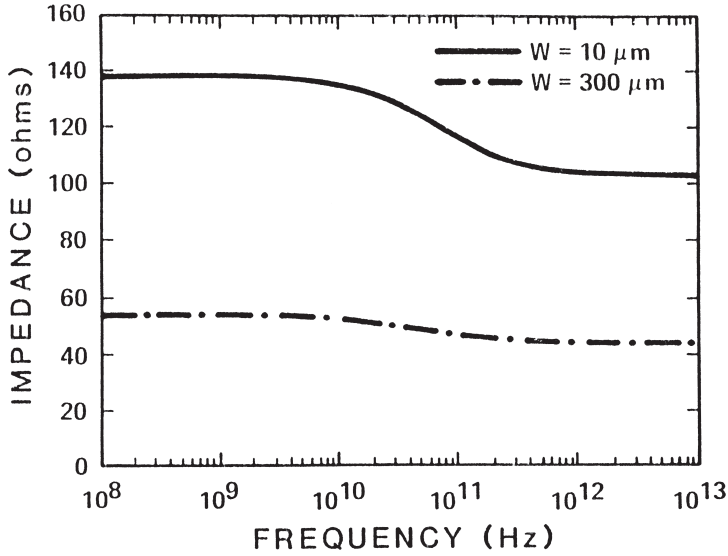


Figure 3.5.5 Characteristic impedance vs. frequency for two microstrip interconnections of widths 10 and 300 μm [49].

phase velocity on frequency for the same set of parameters as in Figure 3.5.6 are shown in Figure 3.5.7.

For exponential input pulse (with $\tau_1 = 15$ ps and $\tau_2 = 1$ ps) and square-wave input pulse (with $\tau_1 = 50$ ps, $\tau_2 = 5$ ps, and $\omega_1 = 10^{12}$ Hz), the time-domain waveforms for aluminum interconnections of widths 10 μm and 300 μm on two substrates with resistivities of 10 and 100 Ω.cm at $z = 3$ mm and 6 mm are shown in Figures 3.5.8 and 3.5.9. It should be noted that for the substrate resistivity of 10 Ω.cm, the signal is severely attenuated by 6 mm whereas, for the substrate resistivity of 100 Ω.cm, it is not affected as much. Thus, it can be concluded that high-resistivity substrates are more appropriate when designing microstrip interconnections for high-frequency ICs.

For interconnection materials of tungsten, WSi_2 and poly-Si, and for the square-wave input pulses, the time-domain waveforms at a few locations on the microstrip interconnection on two substrates with resistivities of 10 and 100 Ω.cm are shown in Figures 3.5.10 to 3.5.12. It should be noted that the conductor loss becomes increasingly significant from aluminum to tungsten to WSi_2 lines but the changes are not dramatic. Figure 3.5.12 shows that, for poly-Si lines, the loss becomes very large for very high-speed pulses though significant improvement is achieved by choosing higher resistivity substrates as is the case with other lines as well.

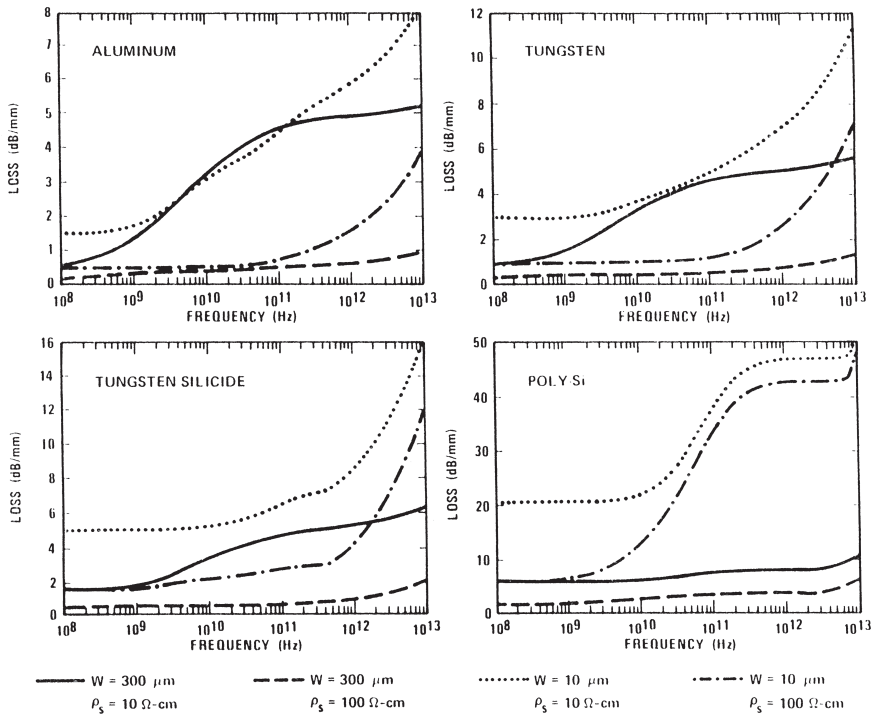


Figure 3.5.6 Plots of line loss α vs. frequency for interconnection materials of Al ($\rho = 2.7\ \mu\Omega$.cm), W ($\rho = 10\ \mu\Omega$.cm), WSi_2 ($\rho = 30\ \mu\Omega$.cm), *and poly-Si* ($\rho = 500\ \mu\Omega$.cm) *on a 450-*μ*m thick Si wafer [49].*

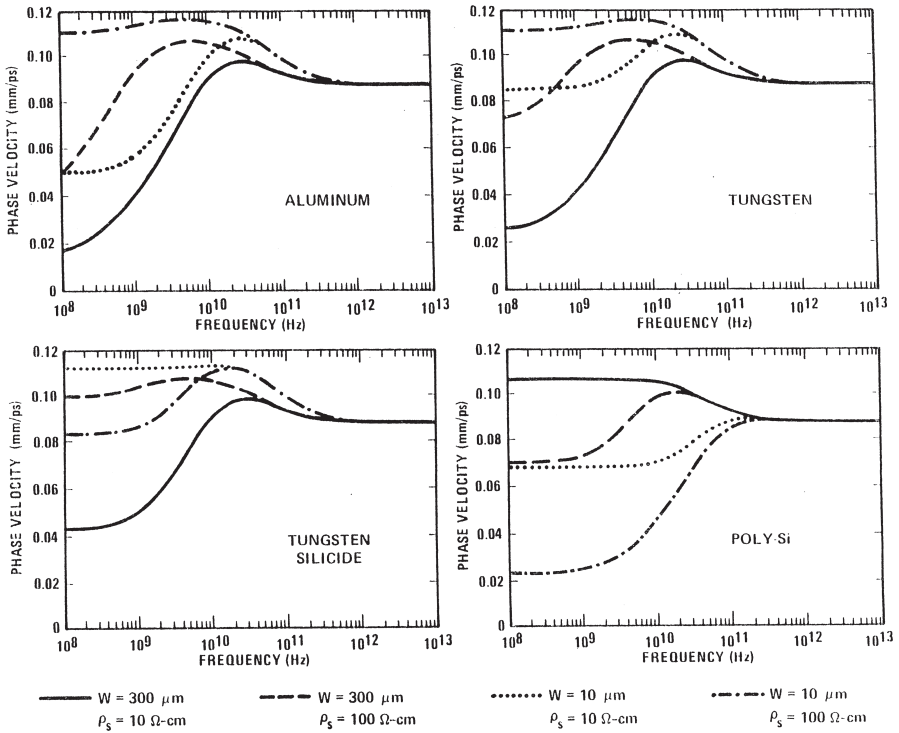


Figure 3.5.7 Plots of phase velocity vs. frequency for interconnection materials of A1 ($\rho = 2.7\ \mu\Omega$.cm), W ($\rho = 10\ \rho\Omega$.cm), WSi_2 ($\rho = 30\ \mu\Omega$.cm), and poly-Si ($\rho = 500\ \mu\Omega$.cm) on a 450-μm thick Si wafer [49].

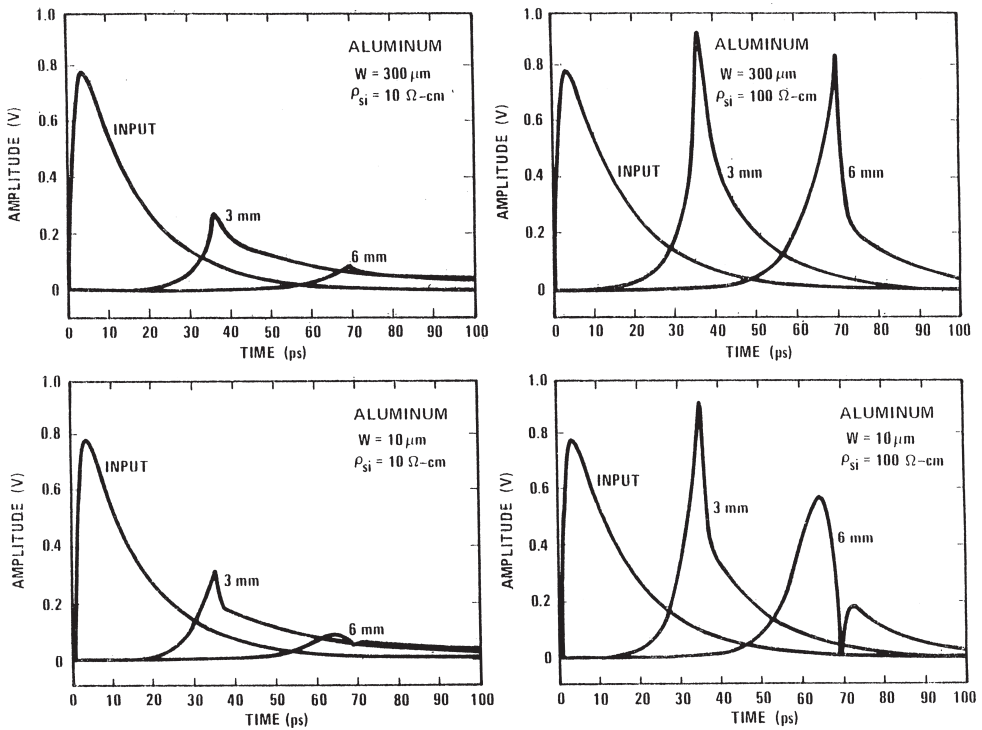


Figure 3.5.8 Plots of time-domain exponential pulses after 0, 3, and 6 mm of propagation on A1 microstrip lines on a 450-μm thick Si wafer [49].

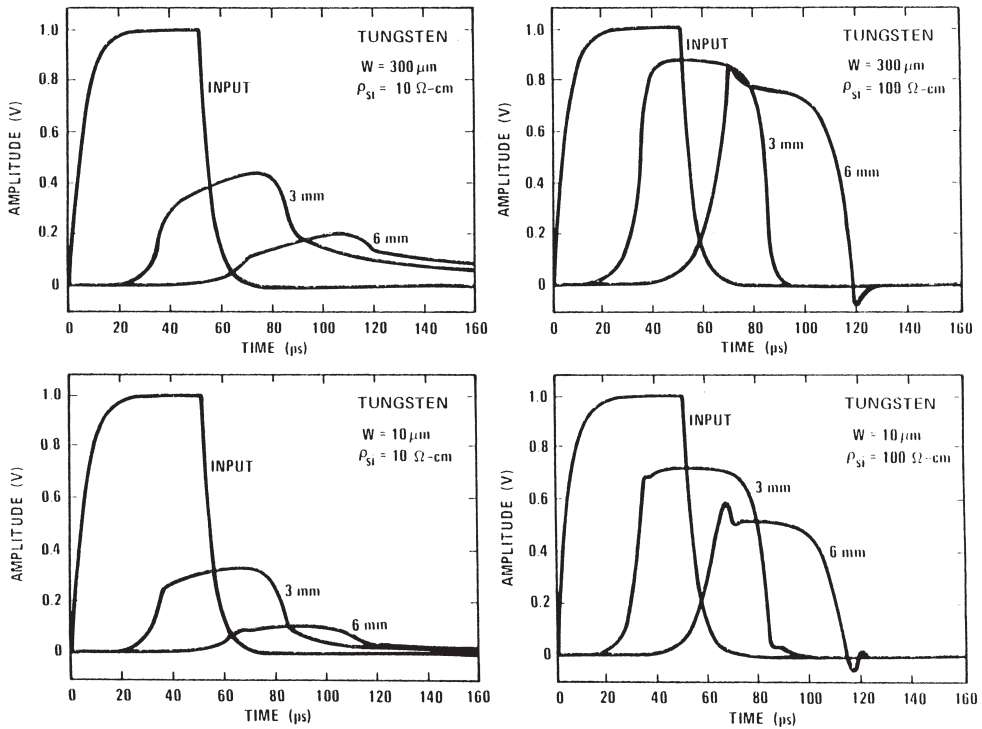


Figure 3.5.9 Plots of time-domain square-wave pulses after 0, 3, and 6 mm of propagation on A1 microstrip lines on a 450-μm thick Si wafer [49].

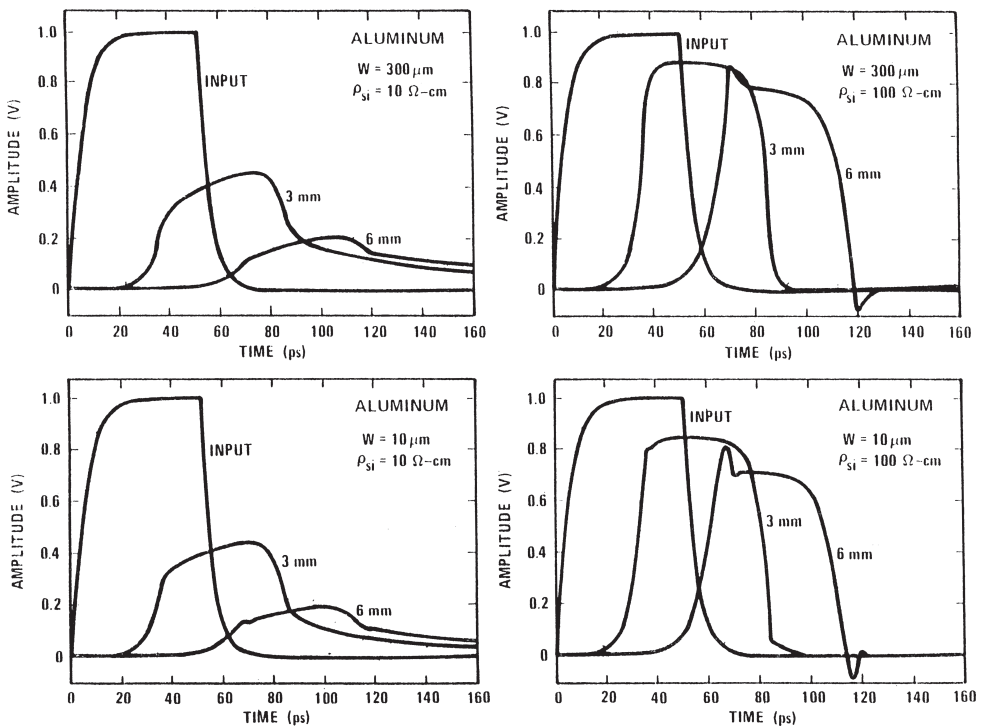


Figure 3.5.10 Plots of time-domain square-wave pulses after 0, 3, and 6 mm of propagation on W microstrip lines on a 450-μm thick Si wafer [49].

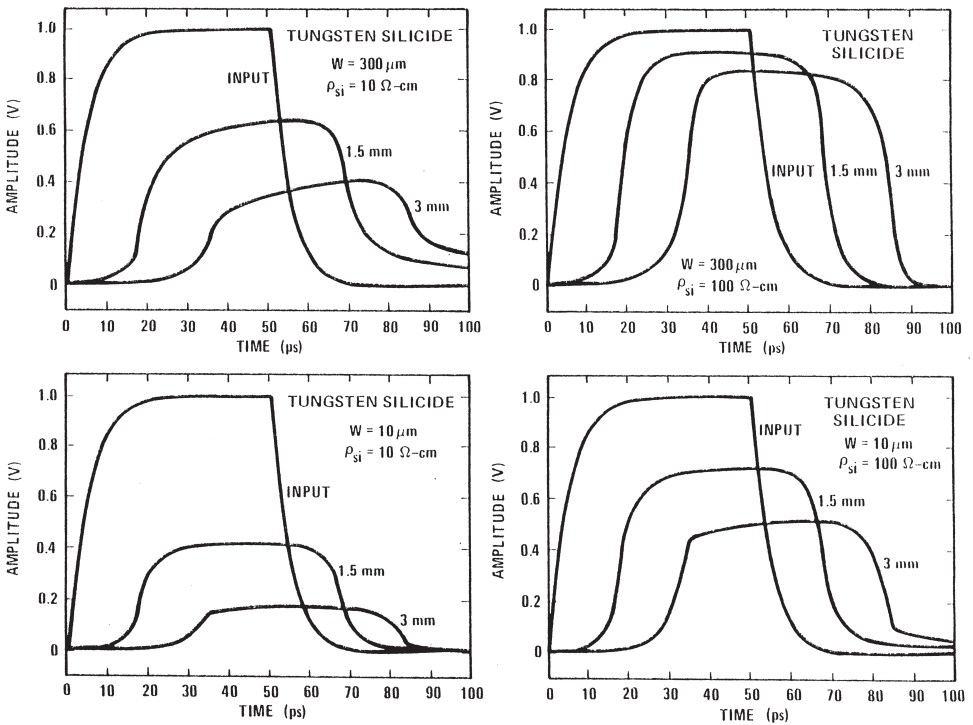


Figure 3.5.11 Plots of time-domain square-wave pulses after 0, 1.5, and 3 mm of propagation on WSi_2 microstrip lines on a 450-μm thick Si wafer [49].

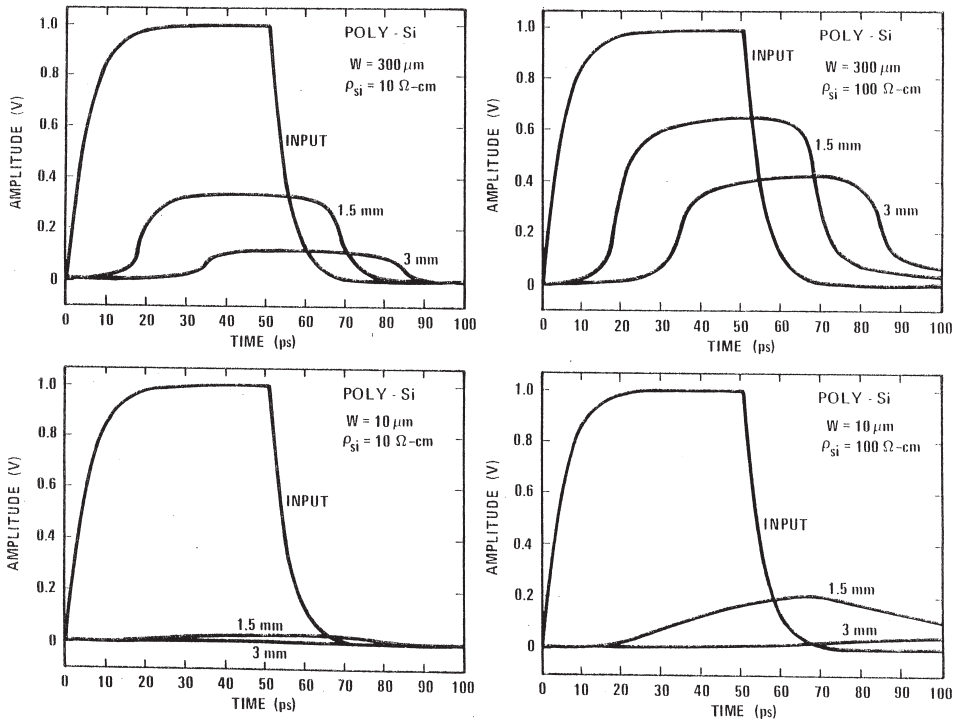


Figure 3.5.12 Plots of time-domain square-wave pulses after 0, 1.5, and 3 mm of propagation on poly-Si microstrip lines on a 450-μm thick Si wafer [49].

Exercise 3.1

Comment on the relative significance of the various high-frequency losses in an aluminum interconnection on the GaAs substrate in the following frequency ranges: (a) Below 10 MHz; (b) 10 MHz to 1 GHz; (c) 1 GHz to 10 GHz; (d) 10 GHz to 100 GHz; and (e) Above 100 GHz.

Exercise 3.2

Include the high-frequency losses in the transmission line model for single-level interconnections presented in section 3.2.

3.6 Compact Modeling of Interconnection Delays

Now, compact, i.e., closed-form expressions for the voltage waveforms and the corresponding delays at the load end of an interconnection are presented. First, the interconnection will be modeled as a distributed RC network [57] and then it will be treated as an RLC network [19]. The expressions are useful for obtaining quick estimates of the interconnection delays though at the cost of some accuracy.

The RC Interconnection Model

Consider a single-level interconnection of length l driven by a transistor or a gate and connected to another transistor or gate at its load end as shown in Figure 3.6.1. It can be modeled as an interconnection line driven by a voltage source of internal resistance R_S and loaded by a capacitor C_L.

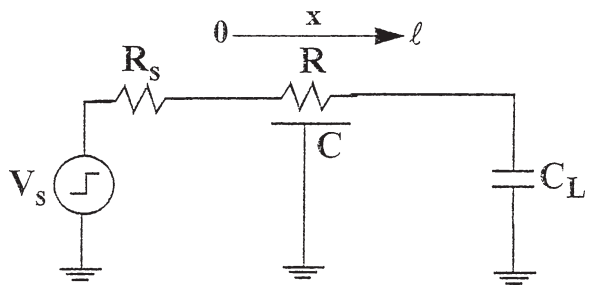


Figure 3.6.1 A single-level interconnection of length l driven by a voltage source of internal resistance $\mathbf{R_S}$ ***and loaded by a capacitor*** $\mathbf{C_L}$.

Inductive effects are neglected in this treatment. Voltage wave propagation along this line is represented by the differential equation given by

$$\frac{1}{r}\left(\frac{\partial^2 V}{\partial x^2}\right) = c\left(\frac{\partial V}{\partial t}\right) \tag{3.6.1}$$

where r and c are the resistance and capacitance of the interconnection line per unit length, respectively. The voltage waveform $V(l, t)$ at the inter connection load can be expressed as a series [58]:

$$\frac{V(\ell, t)}{V_S} = 1 + \sum_{k=1}^{\infty} K_k e^{-\sigma_k \cdot t/RC} \approx 1 + K_1 e^{-\sigma_1 \cdot t/RC} \tag{3.6.2}$$

where R and C are the total resistance and capacitance of the interconnection line, respectively, i.e., $R = (r)(l)$ and $C = (c)(l)$. σ_k's are the roots of the equation [57]:

$$\tan(\sqrt{\sigma_k}) = \frac{1 - R_T C_T \sigma_k}{(R_T + C_T)\sqrt{\sigma_k}} \tag{3.6.3}$$

subject to the condition:

$$\left(k - \frac{3}{2}\right)\pi < \sqrt{\sigma_k} < \left(k - \frac{1}{2}\right)\pi$$

where

$$R_T = \frac{R_S}{R}$$

and

$$C_T = \frac{C_L}{C}$$

The coefficients K_k can be calculated from the equation:

$$K_k = (-1)^k \frac{2}{\sqrt{\sigma_k}} \frac{\sqrt{(1 + R_T^2 \sigma_k)(1 + C_T^2 \sigma_k)}}{(1 + R_T^2 \sigma_k)(1 + C_T^2 \sigma_k) + (R_T + C_T)(1 + R_T C_T \sigma_k)} \tag{3.6.4}$$

The approximation in Eqn. (3.6.2) is excellent for $t > 0.1\ RC$ and therefore K_1 and σ_1 are the most important coefficients. The approximate values of these two coefficients are given by

$$K_1 = -1.01\left(\frac{R_T + C_T + 1}{R_T + C_T + \frac{\pi}{4}}\right) \tag{3.6.5}$$

$$\sigma_1 = \frac{1.04}{R_T C_T + R_T + C_T + \left(\frac{2}{\pi}\right)^2} \tag{3.6.6}$$

The relative errors of the above functions are less than 3 percent for K_1 and less than 4 percent for σ_1 for any values of R_T and C_T. It should be noted that the exact value of K_1 is $\frac{4}{\pi}$ and that of σ_1 is $\frac{\pi}{2}$ for $R_T = C_T = 0$. When $R_T = C_T >> 1$, the exact value of K_1 is –1 and that of σ_1 is $1/\{(R_T + 1)(C_T + 1)\}$. Both these asymptotic values are correctly produced by the expressions (3.6.5) and (3.6.6).

The voltage waveform at the load end of the interconnection can be expressed as follows:

$$\frac{V(\ell, t)}{V_S} = 1 - \exp\left(-\frac{\frac{t}{RC} - 0.1}{R_T C_T + R_T + C_T + 0.4}\right) \tag{3.6.7}$$

Equation (3.6.7) can be solved for t in terms of $V(\mathrm{l})$. The time t taken by the load voltage to reach $v = V/V_S$ is given by:

$$t = RC\left\{0.1 + \ln\left(\frac{1}{1 - v}\right)(R_T C_T + R_T + C_T + 0.4)\right\} \tag{3.6.8}$$

Equation (3.6.8) can be further solved to find the times $t_{0.5}$ and $t_{0.9}$ for $v = 0.5$ and 0.9, respectively as follows:

$$t_{0.5} = RC\{0.377 + 0.693(R_T C_T + R_T + C_T)\} \tag{3.6.9}$$

$$t_{0.9} = RC\{1.02 + 2.3(R_T C_T + R_T + C_T)\} \tag{3.6.10}$$

Comparisons of the load voltage waveforms and the corresponding delays obtained by using the compact expressions (3.6.9) and (3.6.10) with those obtained by using the exact analysis show that the error in Eqn. (3.6.8) is less than 3.5 percent of *RC* [57]. The accuracy of this equation is better than that given by the widely used Elmore's delay expression [59].

The RLC Interconnection Model—A Single Semi-Infinite Line

A single semi-infinite interconnection line modeled as a distributed RLC network driven by a step input voltage source V_S with a source resistance R_S is shown in Figure 3.6.2. The voltage $V_{inf}(x, t)$ along this line is described by the following partial differential equation:

$$\frac{\partial^2}{\partial x^2} V_{inf}(x,t) = lc\frac{\partial^2}{\partial t^2} V_{inf}(x,t) + rc\frac{\partial}{\partial t} V_{inf}(x,t) \qquad (3.6.11)$$

where r, l, and c are the distributed resistance, inductance, and capacitance per unit length of the interconnection line, respectively. Assuming

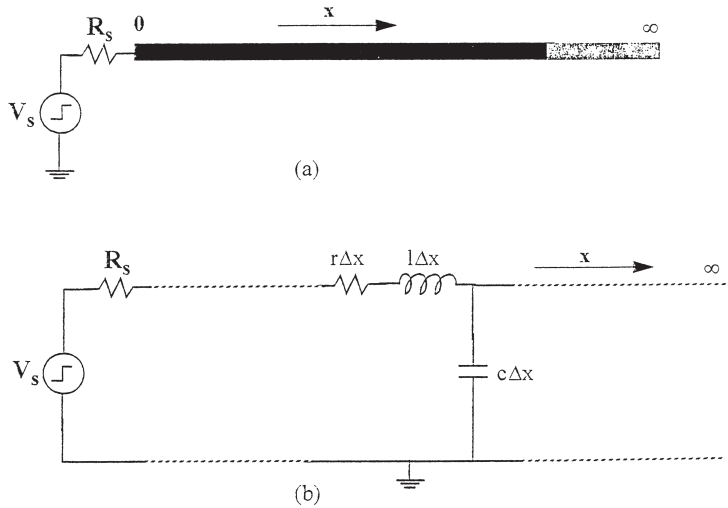


Figure 3.6.2 A single semi-infinite interconnection line shown in (a) modeled as a distributed RLC network shown in (b) driven by an input voltage source V_S with a source resistance R_S.

that the voltage and current along the line are zero at $t = 0$, Laplace transformation of Eqn. (3.6.11) yields the following differential equation:

$$\frac{\partial^2}{\partial x^2} V_{inf}(x, s) = lcs\left(s + \frac{r}{l}\right) V_{inf}(x, s) \tag{3.6.12}$$

In the Laplace domain (s-domain), a general solution of Eqn. (3.6.12) can be written as

$$V_{inf}(x, s) = A\exp\left\{-x\sqrt{lc}\sqrt{s\left(s + \frac{r}{l}\right)}\right\} + B\exp\left\{x\sqrt{lc}\sqrt{s\left(s + \frac{r}{l}\right)}\right\} \tag{3.6.13}$$

The coefficient A can be determined from applying the known boundary condition at $x = 0$ that $V_{inf}(0, s)$ is equal to the input source voltage $V_S(s)$ minus the voltage drop across the source impedance in the s-domain while B can be determined from the requirement that at $x = \infty$, the voltage must be finite and well behaved resulting in $B = 0$. Then the voltage along the line in the s-domain is given by

$$V_{inf}(x, s) = V_S(s)\frac{Z(s)}{Z(s) + R_S}\exp\left\{-x\sqrt{lc}\sqrt{s\left(s + \frac{r}{l}\right)}\right\} \tag{3.6.14}$$

where $Z(s)$ is the characteristic impedance of the lossy interconnection given by

$$Z(s) = \sqrt{\frac{r + sl}{sc}} = Z_o\sqrt{\frac{s + r/l}{s}} \tag{3.6.15}$$

where Z_o is the characteristic impedance of the lossless line given by $Z_o = \sqrt{(l/c)}$. The voltage along the semi-infinite line in the time domain can be obtained by an inverse Laplace transformation of Eqn. (3.6.14) to be [19]:

$$V_{inf}(x, t) = V_S\left(\frac{Z_o}{Z_o + R_S}\right)e^{-\left(\frac{r}{2l}\right)t}$$

$$\times \left\{ I_0\sigma\sqrt{t^2 - (x\sqrt{lc})^2} + \frac{1}{1 - \Gamma}\sum_{k=1}^{\infty} I_k(\sigma\sqrt{t^2 - (x\sqrt{lc})^2})\left(\frac{t - x\sqrt{lc}}{t + x\sqrt{lc}}\right)^{k/2}\right.$$

$$\left.(4-(1+\Gamma)^2\Gamma^{k-1})\right\}\times\ u_0(t-x\sqrt{lc}) \tag{3.6.16}$$

where $\sigma = r/(21)$, I_k is the kth-order modified Bessel function, u_0 is a unit step function and Γ is the reflection coefficient defined by

$$\Gamma\ =\ \left(\frac{R_S-Z_o}{R_S+Z_o}\right)$$

The voltage along the lossless semi-infinite line can be obtained from Eqn. (3.6.16) after substituting $r = 0$ to be

$$V_{inf}(x,\ t)\ =\ V_S\left(\frac{Z_o}{Z_o+R_S}\right)u_0(t-x\sqrt{lc}) \tag{3.6.17}$$

because the zero-order modified Bessel function has a value of unity and all higher-order modified Bessel functions become zero.

It is interesting to note from Eqn. (3.6.16) that at t = x 1c, the voltage wavefront traveling down the lossy semi-infinite line is given by

$$V_{inf}(x,\ t)\ =\ V_S\left(\frac{Z_o}{Z_o+R_S}\right)e^{-\left(\frac{r}{2Z_o}x\right)} \tag{3.6.18}$$

The RLC Interconnection Model—A Single Finite Line

A global interconnection for gigascale integration can be represented by a finite line of length l driven by a source with an arbitrary source impedance and terminated by an open circuit [60] as shown in Figure 3.6.3. The reflection diagram for a line of finite length is shown in Figure 3.6.4. In the s-domain, the voltage at the end of the line is given by

$$V_{fin}(\ell,\ s)\ =\ 2V_{inf}(\ell,\ s)+2\sum_{n\ =\ 1}^{q}\left(\frac{R_S-Z(s)}{R_S+Z(s)}\right)^n V_{inf}((2n+1)\ell,\ s) \tag{3.6.19}$$

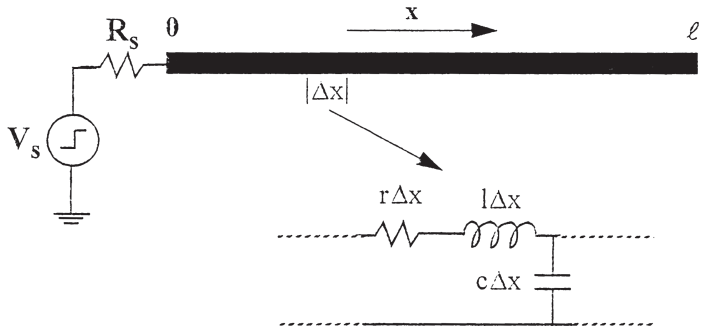


Figure 3.6.3 A single interconnection of finite length modeled as a distributed RLC network driven by an input voltage source V_S with a source resistance R_S and terminated by an open circuit.

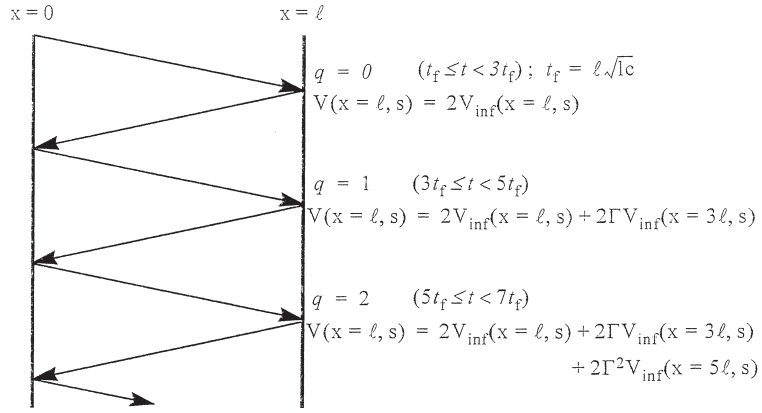


Figure 3.6.4 Reflection diagram for a single interconnection of finite length [19]. (© IEEE, 2000)

where n is the reflection number, q is the maximum reflection number shown in Figure 3.6.4 and $Z(s)$ is defined by Eq. (3.6.15). In the time domain, the voltage at the end of the finite line is given by [19]:

$$V_{fin}(\ell, t) = 2V_{inf}(\ell, t) + 2V_S\left(\frac{Z_o}{Z_o + R_S}\right)e^{-\left(\frac{r}{2l}\right)t}$$

$$\sum_{n=1}^{q}\sum_{i=0}^{n}\sum_{j=0}^{\infty}(-1)^i\Gamma^{(n-i+j)}\frac{n(n-1+j)!}{i!j!(n-i)!}$$

$$\times \left\{ \left(\frac{t-(2n+1)\ell\sqrt{lc}}{t+(2n+1)\ell\sqrt{lc}} \right)^{(i+j)/2} I_{i+j}[\sigma\sqrt{t^2-((2n+1)\ell\sqrt{lc})^2}] + \frac{1}{1-\Gamma} \right.$$

$$\left. \sum_{k=1}^{\infty} \left(\frac{t-(2n+1)\ell\sqrt{lc}}{t+(2n+1)\ell\sqrt{lc}} \right)^{(i+j+k)/2} I_{i+j+k} \right.$$

$$\left. [\sigma\sqrt{t^2-((2n+1)\ell\sqrt{lc})^2}](4-(1+\Gamma)^2\Gamma^{k-1}) \right\}$$

$$u_0(t-(2n+1)\ell\sqrt{lc}) \tag{3.6.20}$$

where q, defined earlier as the maximum reflection number for a given time can be written as a function of time as

$$q = \langle 0.5\left(\frac{t}{x\sqrt{lc}} + 1.0\right)\rangle - 1.0 \tag{3.6.21}$$

with the notation $\langle x \rangle$ representing the decimal truncation of x, i.e., $\langle 2.3 \rangle = \langle 2.8 \rangle = 2$.

For the special case when the driving source resistance *RS* is equal to the characteristic impedance of the lossless line *Zo* and the reflection coefficient Γ becomes zero, the voltage at the end of the finite line is given by

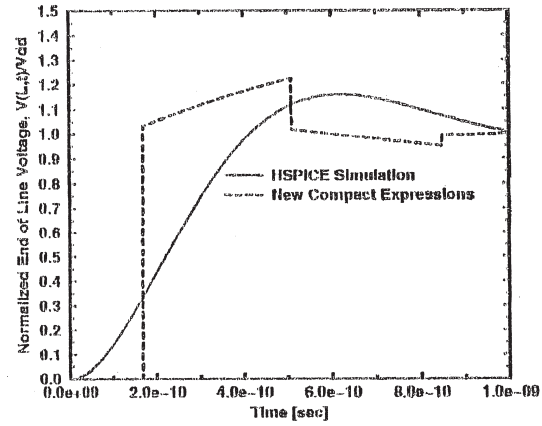
$$V_{fin}(\ell, t) = 2V_{inf}(\ell, t) + V_S e^{-\left(\frac{r}{2l}\right)t} \sum_{n=1}^{q} (-1)^n$$

$$\times \left\{ \left(\frac{t-(2n+1)\ell\sqrt{lc}}{t+(2n+1)\ell\sqrt{lc}} \right)^{n/2} I_n[\sigma\sqrt{t^2-((2n+1)\ell\sqrt{lc})^2}] \right.$$

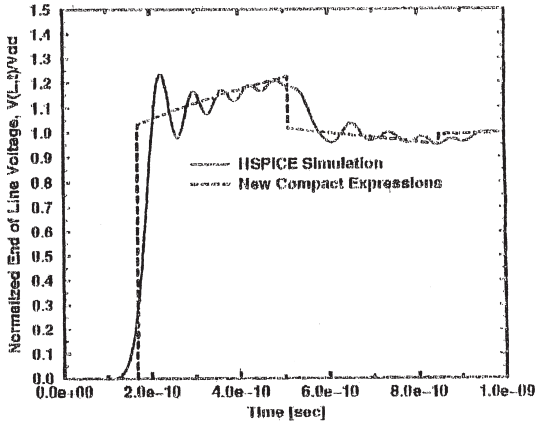
$$\left. + \sum_{k=1}^{\infty} \left(\frac{t-(2n+1)\ell\sqrt{lc}}{t+(2n+1)\ell\sqrt{lc}} \right)^{(n+k)/2} \times I_{n+k}[\sigma\sqrt{t^2-((2n+1)\ell\sqrt{lc})^2}] \right.$$

$$\left. (4-0^{k-1}) \right\} (u_0(t-(2n+1)\ell\sqrt{lc})) \tag{3.6.22}$$

Comparisons of the normalized end of line voltages obtained by the compact expression (3.6.20) with those obtained by HSPICE with 1, 10, 50, and 500 lumped RLC elements are shown in Figure 3.6.5 [19]. For these comparisons, the interconnection metal is assumed to be copper surrounded by a low-k dielectric. The various interconnection parameters are as follows:

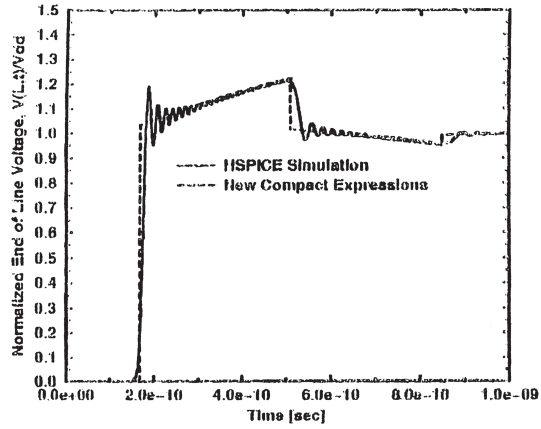


(a)

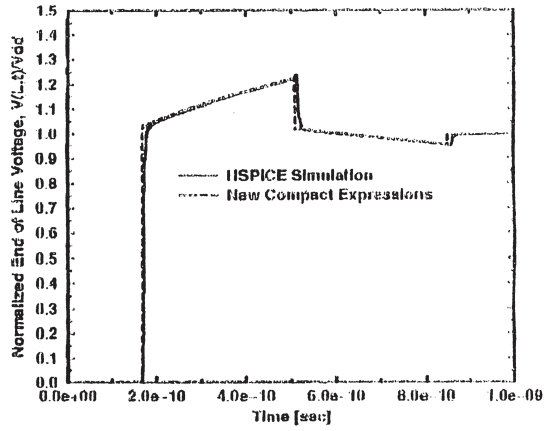


(b)

Figure 3.6.5 Comparisons of the normalized end of line voltages obtained by the compact expression (3.8.20) with those obtained by HSPICE with 1, 10, 50, and 500 lumped RLC elements [19]. (© IEEE, 2000)



(c)



(d)

Figure 3.6.5 (continued)

Interconnection length = 3.6 cm
Interconnection cross section = 2.1 μm by 2.1 μm
Resistance per unit length = 37.9 Ω/cm
Driving source resistance = 133.2 Ω
Lossless characteristic impedance = 266.5 Ω

Figure 3.6.5 shows that the HPICE waveforms approach the compact expression waveform as the number of RLC elements is increased

in the HSPICE simulation. For the typical values of the interconnection and driving source parameters chosen in these comparisons, there is virtually complete agreement between the two waveforms for 500 or more RLC elements lending excellent support to the compact expression (3.6.20).

Single RLC Interconnection—Delay Time

For a distributed RC interconnection line, Sakurai has derived the following compact expression for the delay time defined as the time taken by the load voltage to reach 50 percent of its steady state value:

$$T_{d,\,RC} = 0.693\, R_S c l + 0.377\, r c \mathrm{l}^2 \tag{3.6.23}$$

For a distributed RLC interconnection line, this expression has been extended by Davis and Meindl as follows [19]:

$$T_{d,\,RLC} = \ell/\sqrt{lc} \quad \text{for} \quad \frac{R}{Z_o} \le \ln\left[\frac{4Z_o}{R_S + Z_0}\right] \quad \text{and} \quad R_S > 3Z_o \tag{3.6.24}$$

$$T_{d,\,RLC} = 0.693\, R_S c \mathrm{l} + 0.377\, r c \mathrm{l}^2 \text{ for } \frac{R}{Z_o} \ge 2\ln\left[\frac{4Z_o}{R_S + Z_0}\right] \text{ or } R_S > 3Z_o \tag{3.6.25}$$

A comparison of the time delay obtained by the above closed-form expressions with that obtained from the compact *rlc* expression shows that the error in the simplified expression is less than 5 percent when R_S/Z_o is less than 0.2 or when R/Z_o is greater than 2.3. Outside this region, more accurate delay time can be obtained by using the compact distributed *rlc* expressions.

Two and Three Coupled RLC Interconnections—Delay Times

An analysis of two and three coupled RLC interconnections with open-circuit terminations [20] is presented in chapter 4. For a system of two coupled distributed RLC interconnects A (active) and Q (quiet) shown in Figure 3.6.6, the worst-case time delay occurs when the mutual

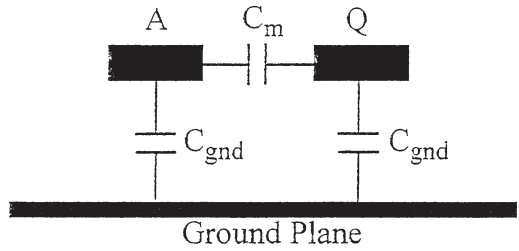


Figure 3.6.6 Two coupled distributed RLC interconnects A (active) and Q (quiet) [20]. (© IEEE, 2000)

capacitance between the lines is the highest, i.e., when the two lines are switching with opposite polarities. The solution for the voltage in this case is given by V_- which is effectively the solution for a single finite line with inductance, $l = (l_s – l_m)$ and capacitance, $c = (c_s + 2_{cm})$. It is given by

$$V_A(l, t) = V_{fin}(l, t, l = l_s – l_m, c = c_{gnd} + 2_{cm}) \qquad (3.6.26)$$

For a system of three parallel coupled interconnections, each driven by a voltage source V_S having an internal source resistance R_S, sandwiched between two virtual ground planes as shown in Figure 3.6.7, the worst-case time delay occurs when the inner interconnection is active and the two outer lines switch with an opposite polarity simultaneously. After adjusting the initial and boundary conditions (see detailed analysis in

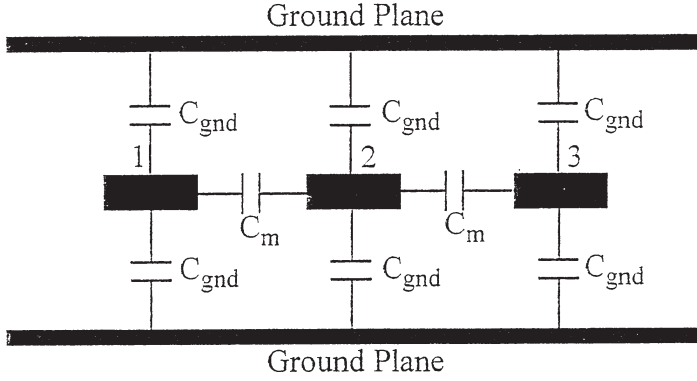


Figure 3.6.7 Three parallel coupled interconnects sandwiched between two virtual ground planes [20]. (© IEEE, 2000)

chapter 4), the load voltage waveform on the inner (active) interconnection is given by

$$V_A(\ell, t) = \frac{4}{3} V_{fin}\left(\ell, t, l=\frac{1}{(2c_{gnd}+3c_m)v^2}, c=2c_{gnd}+3c_m\right) - \frac{1}{3} V_{fin}\left(\ell, t, l=\frac{1}{2c_{gnd}v^2}, c=2c_{gnd}\right) \quad (3.6.27)$$

In equations (3.6.26) and (3.6.27), $V_{\text{fin}}(x, t)$ represents the voltage waveform along a single interconnection line given by

$$V_{fin}(l, t) = 2\, V_{inf}(x = l, t, \text{m} = 0)$$

$$+ 2\bar{e}^{\left(\frac{r}{2l}\right)t} \sum_{n=1}^{q} \sum_{i=0}^{n} \sum_{j=0}^{\infty} (-1)^i \Gamma^{(n-i+j)} \frac{n(n-1+j)!}{i!j!(n-i)!}$$

$$\times \text{V}_{inf}(\text{x} = (2\text{n} + 1)l, \text{t}, \text{m} = \text{i} + \text{j}) \quad (3.6.28)$$

where $V_{\text{inf}}(x, t, m)$ denotes the voltage waveform along the semi-infinite line given by

$$V_{inf}(x, t, m) = V_S\left(\left(\frac{Z_o}{Z_o + R_S}\right)\left(\frac{t - x\sqrt{lc}}{t + x\sqrt{lc}}\right)^{m/2} e^{-\left(\frac{r}{2l}\right)t} I_0\left(\frac{r}{2l}\sqrt{t^2 - (x\sqrt{lc})^2}\right)\right.$$

$$\left. + \frac{1}{2}\sum_{k=1}^{\infty}\left(\frac{t - x\sqrt{lc}}{t + x\sqrt{lc}}\right)^{(k+m)/2} e^{-\left(\frac{r}{2l}\right)t} (4 - (1+\Gamma)^2\Gamma^{k-1}) I_{(k+m)}\right.$$

$$\left.\left(\frac{r}{2l}\sqrt{t^2 - (x\sqrt{lc})^2}\right)\right) u(t - x\sqrt{lc}) \quad (3.6.29)$$

In the above analysis, we have assumed that the interconnects are open-circuited at the load ends and the capacitance of the driving source has been neglected. It has been shown [21] that for an interconnection driven by a large driver, neglecting the source capacitance causes about 5 percent error in the 50 percent delay time whereas neglecting both the

driver and load capacitances results in an error of about 14 percent. For a detailed treatment of capacitively terminated single and coupled distributed RLC interconnects, readers are referred to the reference [21].

3.7 Modeling of Active Interconnections

It has been known for some time that the transistors can be scaled down in size in such a way that the device propagation delay decreases in direct proportion to the device dimensions. However, if the interconnections are scaled down, it results in RC delays that begin to dominate the IC chip performance at submicron dimensions. In other words, for the high-density high-speed submicron-geometry chips, it is mostly the interconnection rather than the device performance that determines the chip performance. So far, the interconnection delays have been reduced by using higher conductivity materials such as replacing aluminum with copper to lower the interconnection resistance, replacing silicon dioxide with a low dielectric constant material to lower the interconnection capacitance and by keeping the interconnection thickness almost constant irrespective of the scaling of devices, etc. For example, in scaling from the 10 μm to the 1 μm design rules, the interconnection thicknesses were reduced by a factor of 2 or less. Now, because of the limitations of the optical lithography systems, it is essential that other approaches be developed to lower the interconnection delays. One way of solving this problem is to replace the passive interconnections on a chip by the active interconnections i.e., by inserting inverters or "repeaters" at appropriate spacings depending on the preferred driving mechanism. However, this technique does require more area on the chip and results in higher power consumption.

In the literature [69, 70], several methods have been discussed for the reduction of the transit delays in an interconnection. These include driving the interconnection using minimum size inverters, optimum size inverters, and cascaded inverters. An analysis of these driving methods for the silicon-based ICs is presented in reference [69]. Here, these methods have been examined for the GaAs-based ICs [70]. Propagation times (time taken by the output signal to go from 0 to 90 percent of its steady state value) have been calculated for each of these three methods for several

interconnection dimensions and have been compared among each other and with the case when the interconnection is driven by a single typical GaAs MESFET. Results are given for two interconnection materials: Aluminum with resistivity (ρ) = 3 $\mu\Omega$.cm and WSi_2 with ρ = 30 $\mu\Omega$.cm.

Interconnection Delay Model

An interconnection having total resistance R_i and capacitance C_i driven by a transistor of resistance R_s and driving a load capacitance C_L is shown in Figure 3.7.1. Assuming a unit step voltage source, the propagation times in distributed and lumped RC networks can be approximated as $1.0RC$ and $2.3RC$, respectively [71]. Therefore, an approximate expression for the total delay in the interconnection shown in Figure 3.7.1 will be

$$T_{90\%} = 1.0R_iC_i + 2.3(R_sC_L + R_sC_i + R_iC_L) \tag{3.7.1}$$

Ignoring the terms containing the load capacitance C_L, we have

$$T_{90\%} \approx R_iC_i + 2.3R_tC_i \tag{3.7.2}$$

This expression is in agreement with that derived by Sakurai [72]. Since both interconnection resistance and capacitance increase linearly

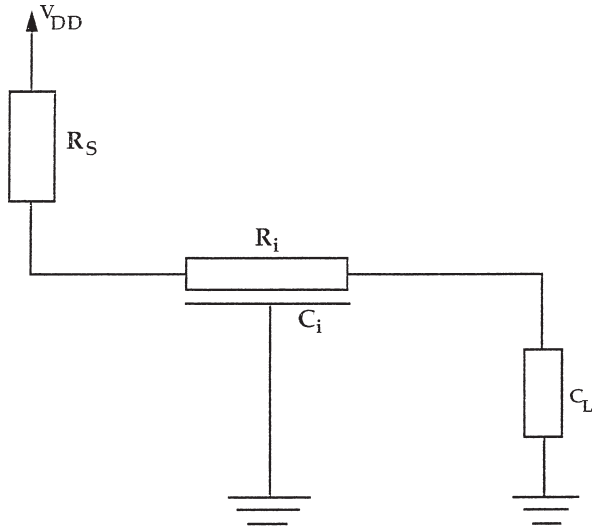


Figure 3.7.1 Interconnection delay model [69]. (© 1985 IEEE)

with length therefore the propagation time expressed by Eqn. (3.7.2) will increase nearly as the square of the interconnection length. It can be shown that this dependence can be made linear if the entire interconnection length is divided into smaller sections and each section is driven by a repeater.

Active Interconnection Driven by Minimum Size Inverters

A schematic diagram of an active interconnection driven by minimum size inverters as repeaters is shown in Figure 3.7.2. As shown in this figure, the use of inverters divides the interconnection into smaller subsections. The various symbols used in the figure are:

R_i = Total resistance of the interconnection line
C_i = Total capacitance of the interconnection line
R_r = Output resistance of the minimum size inverter
C_r = Input capacitance of the minimum size inverter
R_s = Resistance of the GaAs MESFET
C_L = Load capacitance
n = Number of inverters

To achieve the shortest total propagation time using minimum size inverters, the optimum number of inverters can be found using calculus to be [69]

$$n = \sqrt{\left\{\frac{R_i C_i}{2.3 R_r C_r}\right\}} \tag{3.7.3}$$

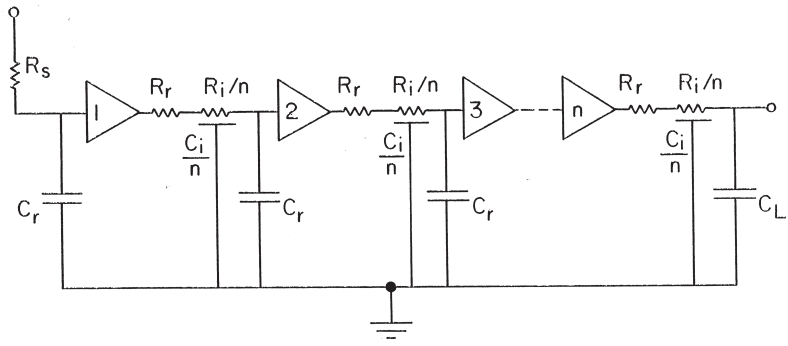


Figure 3.7.2 A schematic diagram of an interconnection driven by the minimum size inverters [69]. (© 1985 IEEE)

The propagation time for each of the subsections driven by the minimum size inverters can be determined by using the algorithm presented in section 3.2 whereas the additional delay caused by the first stage can be found by the approximate expression for lumped RC networks given by Wilnai [71] to be $2.3R_sC_r$. The results using aluminum as the interconnection material are listed in Tables 3.7.1 and 3.7.2 whereas those using WSi_2 as the interconnection material are listed in Tables 3.7.3 and 3.7.4.

Active Interconnection Driven by Optimum Size Inverters

Propagation times can be improved by increasing the size of the inverters by a factor of k, where k is given by [69]

$$k = \sqrt{\left\{\frac{R_r C_i}{R_i C_r}\right\}} \tag{3.7.4}$$

This is because the current driving capability of the inverter is directly proportional to its width/length ratio. When this ratio is increased by a factor of k, the output resistance of the inverter becomes R_r/k and the

Table 3.7.1 Comparison of the propagation times for the four methods of driving an interconnection and for several lengths of the interconnection—Propagation times for the four driving methods (All times are in nanoseconds)

Interconnect Length	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
1 mm	0.05	*	*	0.24
2 mm	0.08	*	*	0.27
5 mm	0.17	2.31	0.11	0.34
1 cm	0.33	4.16	0.20	0.46
2 cm	0.80	7.87	0.29	0.76
5 cm	3.5	18.98	0.54	2.79
10 cm	15.1	37.51	0.97	11.49

Interconnection material: Aluminum (ρ = 3 μΩ.cm)
(Interconnection width = Interconnection separation = 1 μm; Load = 100 fF; Source resistance = 700 Ω)
*For interconnect lengths below 2 mm, the method was found unsuitable because the number of repeaters as given by equation for n was less than one.

Table 3.7.2 Comparison of the propagation times for the four methods of driving an interconnection and for several interconnection widths—Propagation times for the four driving methods (All times are in nanoseconds)

Interconnect Width	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
0.1 μm	0.98	3.01	0.04	0.85
0.2 μm	0.50	3.10	0.08	0.52
0.5 μm	0.39	3.56	0.15	0.38
1.0 μm	0.33	4.03	0.20	0.46
2.0 μm	0.31	4.5	0.35	0.70
5.0 μm	0.25	*	*	1.38
10.0 μm	0.27	*	*	2.39

Interconnection material: Aluminum (ρ = 3 μΩ.cm)
(Interconnection length = 1 cm; Load = 100 fF; Source resistance = 700 Ω)
*For interconnection widths above 5.0 μm, the method was found unsuitable because the number of repeaters as given by equation for n was less than one.

Table 3.7.3 Comparison of the propagation times for the four methods of driving an interconnection and for several lengths of the interconnection—Propagation times for the four driving methods (All times are in nanoseconds)

Interconnect Length	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
1 mm	0.07	*	*	0.27
2 mm	0.14	1.11	0.13	0.34
5 mm	0.41	2.14	0.23	0.62
1 cm	1.35	3.85	0.39	1.42
2 cm	4.62	7.28	0.71	4.49
5 cm	9.6	17.55	1.67	22.3
10 cm	19.98	34.69	3.26	80.28

Interconnection material: WSi_2 (ρ = 30 μΩ.cm)
(Interconnection width = Interconnection separation = 1 μm; Load = 100 fF;
Source resistance = 700 Ω)
*For interconnect lengths below 2 mm, the method was found unsuitable because the number of repeaters as given by equation for n was less than one.

Table 3.7.4 Comparison of the propagation times for the four methods of driving an interconnection and for several interconnection widths—Propagation times for the four driving methods (All times are in nanoseconds)

Interconnect Width	GaAs MESFET	Minimum Size Repeaters	Optimum Size Repeaters	Cascaded Drivers
0.1 μm	8.9	2.79	0.05	10.6
0.2 μm	5.0	2.99	0.09	5.85
0.5 μm	2.21	3.5	0.38	2.18
1.0 μm	1.35	3.82	0.39	1.42
2.0 μm	0.8	4.34	0.42	1.19
5.0 μm	0.52	5.23	0.56	1.59
10.0 μm	0.36	6.34*	0.82*	2.48

Interconnection material: WSi2 (ρ = 30 μΩ.cm)
(Interconnection width = Interconnection separation = 1 μm; Load = 100 fF;
Source resistance = 700 Ω)
*For interconnect widths above 10 μm, the method was found unsuitable because the number of repeaters as given by equation for n was less than one.

input capacitance of the inverter becomes kC_r. A schematic diagram of an active interconnection driven by using optimum size inverters is shown in Figure 3.7.3. In this case, the additional delay caused by the first stage will be approximately $2.3kR_sC_r$. The total propagation times for this case are also listed in Tables 3.7.1 to 3.7.4.

Active Interconnection Driven by Cascaded Inverters

A schematic diagram of an active interconnection driven by the cascaded inverters is shown in Figure 3.7.4. In this case, instead of a single driver, a chain of inverters is used that increases in size until the last inverter is large enough to drive the interconnection. The optimal delay is obtained by using a sequence of n inverters that increase gradually in size (each by a factor of 2.71828 over the previous one). Optimum value of n can be found to be given by [69]

$$n = ln\left[\frac{C_i}{C_r}\right] \tag{3.7.5}$$

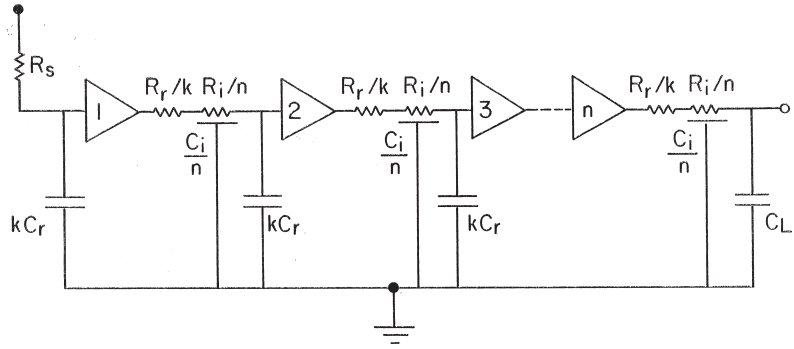


Figure 3.7.3 A schematic diagram of an interconnection driven by the optimum size inverters [69]. (© 1985 IEEE)

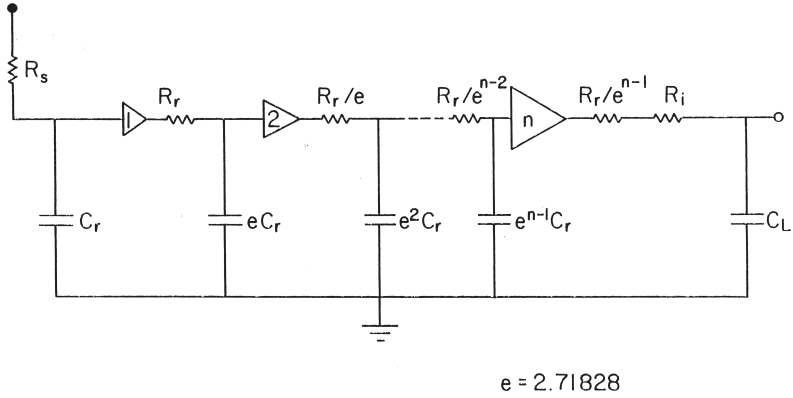


Figure 3.7.4 A schematic diagram of an interconnection driven by the cascaded drivers [69]. (© 1985 IEEE)

In this case, the additional delay caused by the first stage and the first $(n-1)$ inverters is given approximately by

$$2.3\, R_s\, C_r + 2.3(2.71828)(n-1)\, R_r\, C_r \qquad (3.7.6)$$

and the propagation time in the interconnection driven by the last inverter can be found by using the algorithm presented in section 3.2. The results for this case are listed in Tables 3.7.1 to 3.7.4.

Dependence of Propagation Time on the Interconnection Driving Mechanism

A comparison of the propagation times for each of the four methods of driving an interconnection i.e., using a single GaAs MESFET, using

minimum size inverters, using optimum size inverters, and using cascaded inverters, for several values of the interconnection lengths in the range 1 mm to 10 cm is shown in Table 3.7.1. For these results, the interconnection material is taken to be aluminum and the other parameters are shown in the table. This table shows that minimum size and optimum size inverters cannot be used to drive interconnections of lengths 2 mm and below. Otherwise, among the four methods, the method of using the optimum size inverters yields the lowest propagation times. For interconnection lengths of 1 mm and 2 mm, using a single GaAs MESFET results in lower propagation times than the method of using the cascaded inverters. Table 3.7.2 shows the propagation times for each of the four methods for several interconnection widths in the range 0.1 μm to 10.0 μm. This table shows that the methods of using minimum size and optimum size inverters are not suitable for interconnection widths of 5 μm and above. Otherwise, for the interconnection widths below about 1 μm, the method of using the optimum size inverters results in the lowest propagation times among the four methods. For the interconnection widths between 2 and 10 μm, using a single GaAs MESFET yields the lowest propagation times.

When the interconnection material is changed to WSi_2, the propagation times for the four methods of driving an interconnection for several values of the interconnection lengths and interconnection widths are shown in the Tables 3.7.3 and 3.7.4, respectively. These tables show that, in this case, minimum size and optimum size inverters cannot be used for interconnection lengths of 1 mm and below and for the interconnection widths above 10 μm. The method of using the optimum size inverters is found to result in the lowest propagation times for all values of the interconnection lengths (see Table 3.7.3) and for the interconnection widths below 5 μm (see Table 3.7.4). For interconnection widths above 5 μm, driving the interconnection with a single GaAs MESFET seems to result in the lowest propagation times.

Exercise 3.3

Show that for the shortest total propagation time using minimum size inverters, the optimum number of inverters is given by the expression (symbols are defined in section 3.7.2).

$$n = \sqrt{\left\{\frac{R_i C_i}{2.3 R_r C_r}\right\}}$$

Exercise 3.4

Show that the value of k for the optimum size inverters is given by the expression (symbols are defined in section 3.7.3).

$$k = \sqrt{\left\{\frac{R_r C_i}{R_i C_r}\right\}}$$

Exercise 3.5

Show that the optimal delay is obtained by using a sequence of n inverters that increase gradually in size (each by a factor of 2.71828 over the previous one) where n is given by the expression (symbols are defined in section 3.7.4).

$$n = ln\left[\frac{C_i}{C_r}\right]$$

Exercise 3.6

List and discuss the desirable characteristics of a numerical model that make it more suitable for inclusion in a CAD tool. Review the various techniques presented in this chapter from the point of view of their suitability for inclusion in a CAD tool.

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CHAPTER 4

Modeling of Interconnection Crosstalk

Interconnection crosstalk is defined as the voltage signal induced in the neighboring interconnections due to coupling capacitances and inductances. In the literature, modeling and analysis of crosstalk among coupled interconnections has received considerable attention [1–31]. Several authors have used the multiconductor transmission line theory [1–7]. Analysis of coupled lossy transmission lines has also been reported [8–10] and nonlinearity of the source and load networks has been addressed by several studies [6, 9, 11]. Plenty of effort has been made to get closed-form expressions for the signal waveforms on two or three coupled interconnections. For example, the analytical solutions valid for weak-coupling cases (because they ignore the second degree coupling) are reported [10, 12, 13] and the formulas for the voltage transfer functions for a two-line system without the weak-coupling assumption are presented [14]. Closed-form solutions for a system of N lossless lines using cyclic boundary conditions are developed [15] and a general crosstalk analysis technique without making the weak-coupling or the cyclic boundary condition assumption is presented [16]. Crosstalk analysis of parallel multilevel interconnections on the GaAs-based integrated circuit is presented [17, 18], and an analysis of the bilevel crossing interconnections has been carried out [19, 20]. Recently, attention has focused on developing compact models for the transient analysis of distributed RLC interconnections [21–24]. Here are the chapter objectives:

- After going through section 4.1, students should be able to calculate crosstalk voltages among the neighboring

interconnections by using an approximate lumped capacitance model.

- After going through section 4.2, students should be able to analyze crosstalk effects among interconnections on a silicon substrate by using a coupled multiconductor metal-insulator-semiconductor microstrip line model.
- After going through section 4.3, students should be able to investigate crosstalk effects among the single-level interconnections by using a frequency-domain modal.
- After going through section 4.4, students should be able to analyze the crosstalk effects among the multilevel high-density interconnections on an insulating substrate such as GaAs by using a transmission line model.
- After going through section 4.5, students will be familiar with the closed-form expressions for the crosstalk waveforms using the distributed RC and RLC interconnection models.

4.1 Lumped Capacitance Model

The lumped capacitance model of two interconnections coupled by the capacitance C_c is shown in Figure 4.1.1. C denotes the ground capacitance of each interconnection. The first interconnection is driven by the unit voltage source of resistance R_S on the left and terminated by the load capacitance C_L on the right. The second interconnection is terminated by the resistance R_S on the left and by the load capacitance C_L on the right. Crosstalk voltage is defined as the voltage $V_2(t)$ induced across the load C_L on the second interconnection. It can be shown that the amplitude of the crosstalk voltage at time t is given by

$$V_2(t) = \frac{1}{2}\left[\bar{e}^{\left(\frac{t}{\tau_1}\right)} - \bar{e}^{\left(\frac{t}{\tau_2}\right)} \right] \tag{4.1.1}$$

where

$$\tau_1 = R(C + C_L)$$

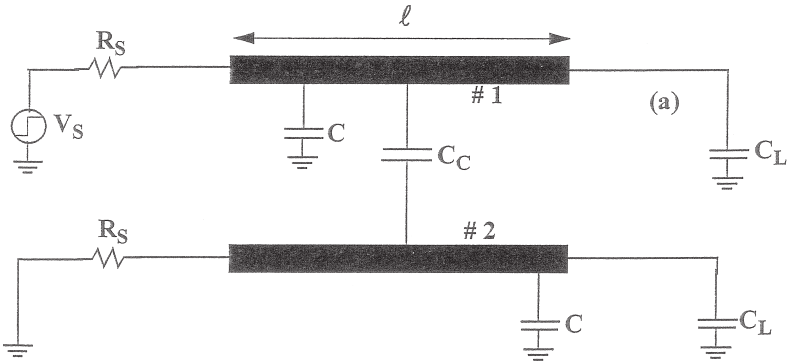

Figure 4.1.1 The lumped capacitance model of two interconnections coupled by the capacitance C_c [45]. (© 1984 IEEE)

and

$$\tau_2 = R(2C_c + C + C_L) \tag{4.1.2}$$

Using calculus, it can be shown that the maximum value of the crosstalk voltage is:

$$V_{2,\,max} = \frac{1}{2}\left[e^{\left(\frac{(n_c-1)}{2n_c}\right) ln\left(\frac{1+n_c}{1-n_c}\right)} - e^{\left(-\frac{(n_c+1)}{2n_c}\right) ln\left(\frac{1+n_c}{1-n_c}\right)} \right] \tag{4.1.3}$$

where the capacitance coupling coefficient *nc* is given by:

$$n_c = \frac{C_c}{C + C_c + C_L} \tag{4.1.4}$$

Based on the lumped capacitance model, the dependences of the crosstalk voltage V_2 on time in the range 0 to 500 ps for interconnections of widths and separation equal to 2 μm, and lengths of 1 and 3 mm are shown in Figure 4.1.2. The figure also shows the dependence of the maximum crosstalk voltage on the coupling coefficient *nc* in the range 0 to 1.

It will be shown in the next section that the "lumped capacitance" approximation becomes inadequate in high-speed circuits. In fact, it can

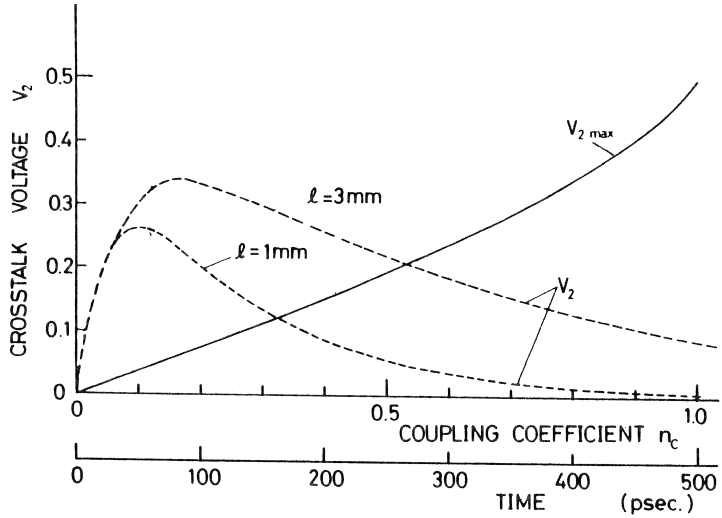

Figure 4.1.2 Crosstalk waveform and amplitude derived from the "lumped capacitance" approximation [45]. (© 1984 IEEE)

be shown that this approximation is applicable to interconnections which are at least a few millimeters long and the circuit rise time is above 200 to 300 ps.

Exercise 4.1

Referring to the lumped capacitance model of Figure 4.1.1, show that the amplitude of the crosstalk voltage at time t is given by:

$$V_2(t) = \frac{1}{2}\left[e^{-\left(\frac{t}{\tau_1}\right)} - e^{-\left(\frac{t}{\tau_2}\right)}\right]$$

where $\tau_1 = R(C + C_L)$ and $\tau_2 = R(2C_c + C + C_L)$. Further prove that the maximum value of the crosstalk voltage is given by:

$$V_{2,\,max} = \frac{1}{2}\left[e^{\left(\frac{(n_c-1)}{2n_c}\right)ln\left(\frac{1+n_c}{1-n_c}\right)} - e^{\left(-\frac{(n_c+1)}{2n_c}\right)ln\left(\frac{1+n_c}{1-n_c}\right)}\right]$$

where

$$n_c = \frac{C_c}{C + C_c + C_L}$$

4.2 Coupled Multiconductor MIS Microstrip Line Model

Here, a system of parallel single-level interconnections is modeled as a coupled multiconductor metal-insulator-semiconductor (MIS) microstrip line system having many conductors [5]. Interconnections are formed on a surface-passivated semiconductor substrate with a metallized back. This model is particularly suitable for situations where many closely spaced interconnections run parallel for a long time such as in the case of a semicustom gate array shown in Figure 4.2.1. For simplicity, losses in the semiconductor substrate are ignored, thus making the model specially applicable to interconnections on semi-insulating GaAs or InP or silicon-on-sapphire substrates.

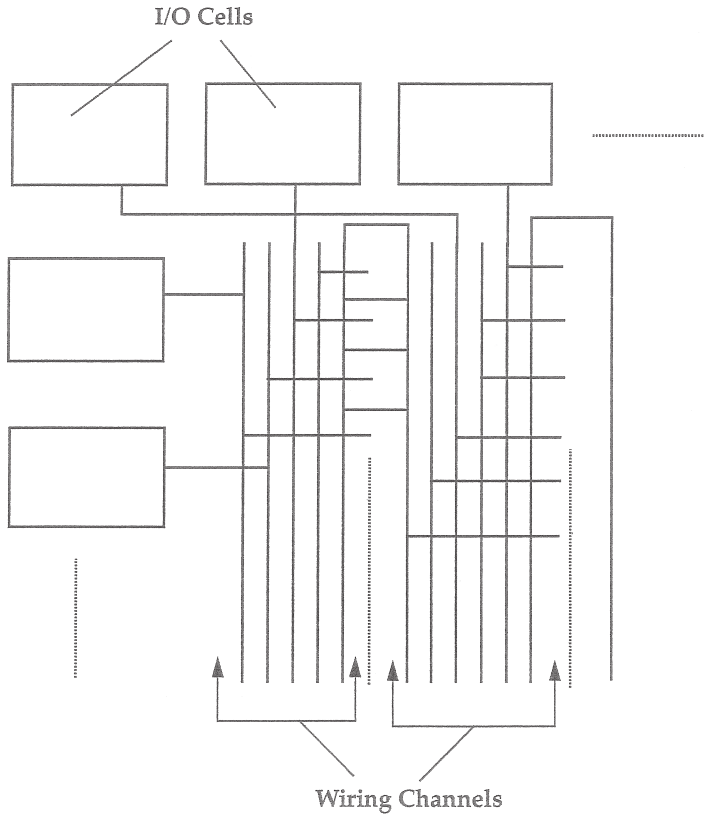

Figure 4.2.1 A schematic diagram of a semicustom gate array [45]. (© 1984 IEEE)

The Model

The MIS microstrip line model for a system of n strip conductors is shown in Figure 4.2.2(a). To incorporate the boundary conditions existing on both sides of the stripline system, a periodic boundary condition is adopted where it is assumed that the same system of n stripline conductors is repeated indefinitely as shown in Figure 4.2.2(b). This periodic boundary condition is quite useful for providing a first-order estimate of crosstalk without going into the specific layout design details.

Now, on this n-conductor stripline system, there exist n quasi-TEM modes. Consider a mode, called the "θ-mode," where the phase angle difference of voltage and current between two adjacent conductors is constant equal to θ. Possible values of θ that satisfy the periodic boundary condition are given by:

$$\theta = 0,\ 2\pi/n,\ldots..,\ 2k\pi/n,\ldots..,\ 2(n-1)\pi/n \qquad (4.2.1)$$

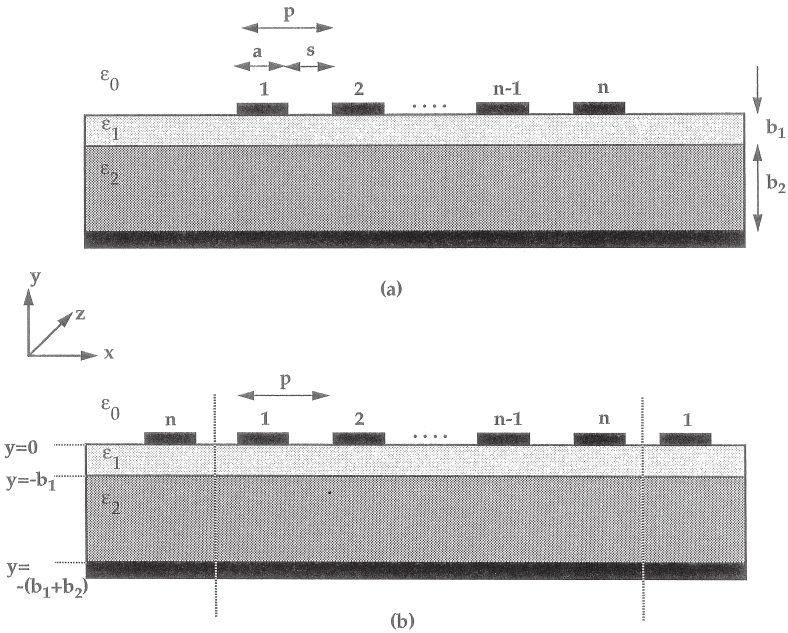

Figure 4.2.2 (a) Coupled multiconductor MIS microstrip line model having n conductors and (b) periodic boundary condition applied to the model [45]. (© 1984 IEEE)

Then the characteristic impedance $Z_{0\theta}$ and the phase velocity V_θ of the θ-mode are given by:

$$Z_{0\theta} = \frac{1}{v_\theta C_\theta} \tag{4.2.2a}$$

$$v_\theta = c_0 \left(\frac{C_{\theta 0}}{C_\theta} \right)^{1/2} \tag{4.2.2b}$$

where c_0 is the velocity of light in vacuum and C_θ and $C_{\theta 0}$ are the static capacitances of the θ-mode per conductor per unit length with and without the dielectric loadings, respectively. The static mode capacitances can be found by the Green's function method. The Green's function on the strip plane ($y = 0$ in Figure 4.2.2(b)) for the θ-mode, denoted by $G_\theta(x, x_0)$, is defined as the potential at a point x on the strip plane when a unit charge with a phase factor of $e^{-jm\theta}$ is placed at points $(x_0 + mp)$ where $m = 0, \pm 1, \pm 2, \ldots, \pm\infty$ and p is the pitch in Figure 4.2.2(b). Yamashita et al. have determined $G_\theta(x, x_0)$ by making a Fourier transformation of the two-dimensional Laplace's equation and solving the resultant equation with respect to y resulting in

$$G_\theta(x, x_0) = \sum_{m=-\infty}^{\infty} \frac{e^{-j\beta_m(x-x_0)}}{p|\beta_m|} \times$$

$$\left[\frac{\varepsilon_1 \coth(b_1\beta_m) + \varepsilon_2 \coth(b_2\beta_m)}{\{\varepsilon_2 \coth(b_2\beta_m)\}\{\varepsilon_0 + \varepsilon_1 \coth(b_1\beta_m)\} + \varepsilon_1\{\varepsilon_1 + \varepsilon_1 \coth(b_1\beta_m)\}} \right] \tag{4.2.3}$$

where

$$\beta_m = \frac{2m\pi + \theta}{p}$$

Then, the potential on the strip under consideration, denoted by V_0, can be found from the charge density function $\rho_\theta(x)$ for the θ-mode at point x on the strip conductor by solving the following equation numerically:

$$V_0 = \int_{-a/2}^{a/2} G_\theta(x, x_0)\rho_\theta(x_0)dx_0 \tag{4.2.4}$$

Then, the static capacitance of the θ-mode per conductor will be given by

$$C_\theta = \frac{1}{V_0} \int_{-a/2}^{a/2} \rho_\theta(x)\,dx \tag{4.2.5}$$

The voltage and current on the kth conductor can be expressed in terms of the normal modes defined above by the equations:

$$V_k(z) = \sum_\theta [A_{\theta f} e^{-j(k-1)\theta} e^{j\omega(t-(z/v_\theta))} + A_{\theta r} e^{-j(k-1)\theta} e^{j\omega(t+z/v_\theta)}] \tag{4.2.6}$$

$$I_k(z) = \sum_\theta \left[\frac{A_{\theta f}}{Z_{0\theta}} e^{-j(k-1)\theta} e^{j\omega(t-(z/v_\theta))} - \frac{A_{\theta r}}{Z_{0\theta}} e^{-j(k-1)\theta} e^{j\omega(t+z/v_\theta)} \right] \tag{4.2.7}$$

where z denotes the position on the conductor, ω is the angular frequency and $A_{\theta f}$ and $A_{\theta r}$ are the amplitudes of the forward and backward voltage waves in the θ-mode. The mode wave amplitudes $A_{\theta f}$ and $A_{\theta r}$ can be determined by using the known terminal conditions at both ends of each strip conductor. The values of voltage and current in the time domain can be found by an inverse Laplace transformation of the above equations.

Simulation Results

In the following results [5], unless otherwise specified, it is assumed that the interconnections are of width $a = 2$ μm, the substrate is of thickness $b_2 = 200$ μm and relative permittivity $\varepsilon_2 = 12$, the insulator is of thickness $b_1 = 1$ μm and relative permittivity $\varepsilon_1 = 4$.

First, for the case of $b_1 = 0$ and $b_2 = \infty$, the dependences of the characteristic impedance $Z_{0\theta}$ on the width to pitch ratio (a/p) for various values of θ are shown in Figure 4.2.3. It is interesting to note the high impedance nature of the interconnection system even for a typical practical case when $a = 2$ μm, $p = 4$ μm, and $b_2 = 200$ μm. This is because of the relatively small value of a/b_2 (which leads to a smaller value of the ground capacitance).

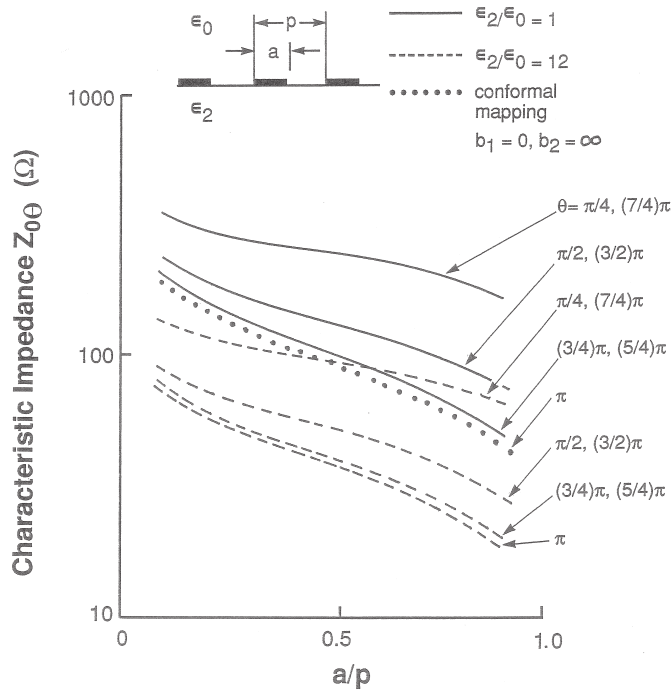

Figure 4.2.3 Calculated characteristic impedance $Z_{0\theta}$ of the various modes [45]. (© 1984 IEEE)

For a system of 10 semi-infinite interconnections with a unit step voltage applied to the input end of the first interconnection and the input ends of other interconnections open-circuited, the induced voltage V_i on the ith interconnection is plotted versus i in Figure 4.2.4. It can be seen that the voltage applied to one line tends to have its effect over a long range. This is because of the small shielding effect of the metallized back plane which in turn is due to a small value of the a/b_2 ratio. For a system of five semi-infinite interconnections, the dependence of the induced voltage at an adjacent strip on the interconnection spacing s $(= p-a)$ is shown in Figure 4.2.5. The long-range nature of the induced voltage can be again noted.

For a system of five finite length interconnections with the excitation and loading conditions shown in the inset of Figure 4.2.6, the crosstalk voltage waveform across the load capacitance of interconnection number 4 is shown in Figure 4.2.6. The waveform shows an initial time delay (due

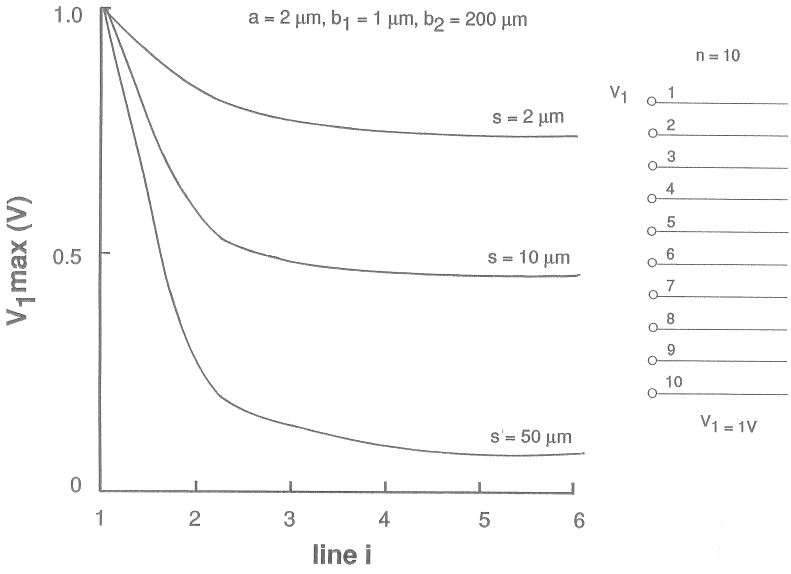

Figure 4.2.4 Calculated crosstalk amplitude at the ith interconnection for a system of 10 semi-infinite interconnections [45]. (© 1984 IEEE)

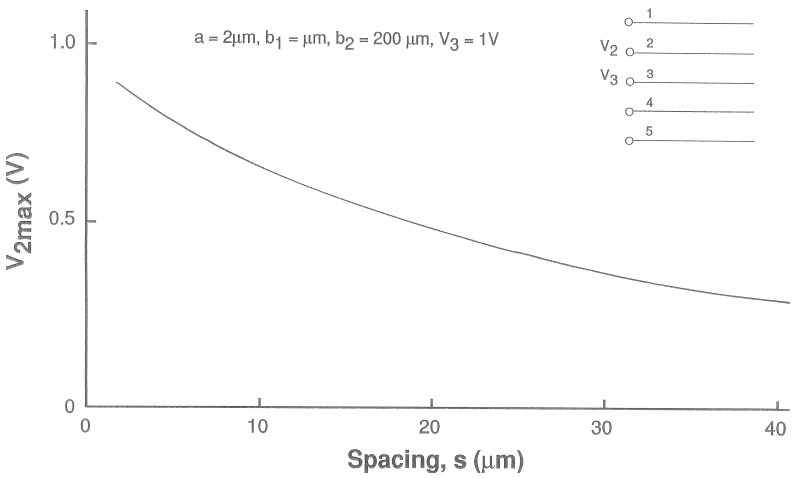

Figure 4.2.5 Crosstalk amplitude at the adjacent interconnection vs. spacing for a system of five semi-infinite interconnections [45]. (© 1984 IEEE)

to the propagation of wavefront) followed by ringing-type decaying oscillation superposed by ripple-like smaller oscillations. These small oscillations are caused by the velocity mismatches among the various modes involved. For the sake of comparison, the corresponding waveform calculated by the "lumped capacitance" approximation (using the network shown in the inset) is also included in Figure 4.2.6 which shows that, as stated earlier, this approximation is not adequate for high-speed circuits. Figure 4.2.7 shows the dependences of the amplitudes of the crosstalk waveforms on the interconnection lengths for two sets of terminal conditions shown in the insets. This figure shows that the presence of floating interconnections increases the crosstalk amplitude because it effectively increases mutual coupling by reducing the line capacitances.

For a system of five finite length interconnections, the crosstalk voltage waveforms for signal source resistance R_S of 5 kΩ, 700 Ω, and 10 Ω are shown in Figure 4.2.8(a). The dependence of the maximum crosstalk voltage on the source resistance in the range 10 to 10,000 Ω is shown in Figure 4.2.8(b). These figures show that the oscillations become more dominant and determine the crosstalk amplitude as the signal source resistance is reduced. As *Rs* is reduced down to a few tens of ohms,

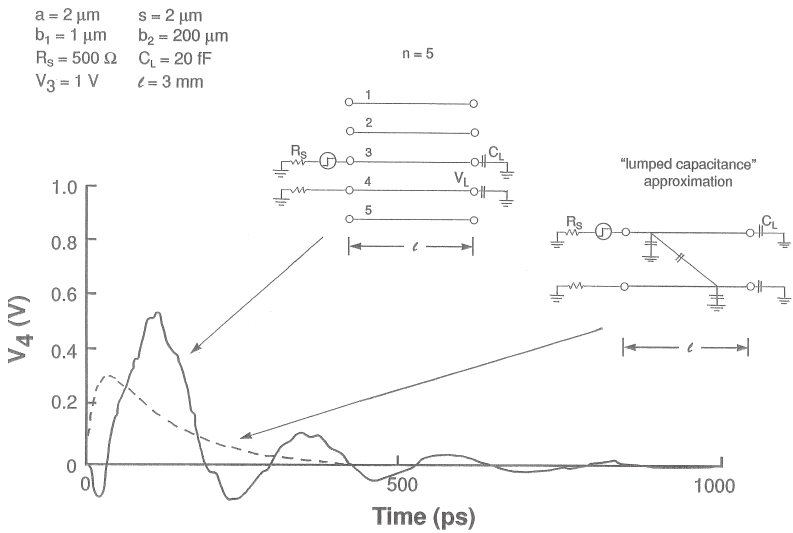

Figure 4.2.6 Calculated step-response waveforms. The dashed curve is the waveform using the "lumped capacitance" approximation [45]. (© 1984 IEEE)

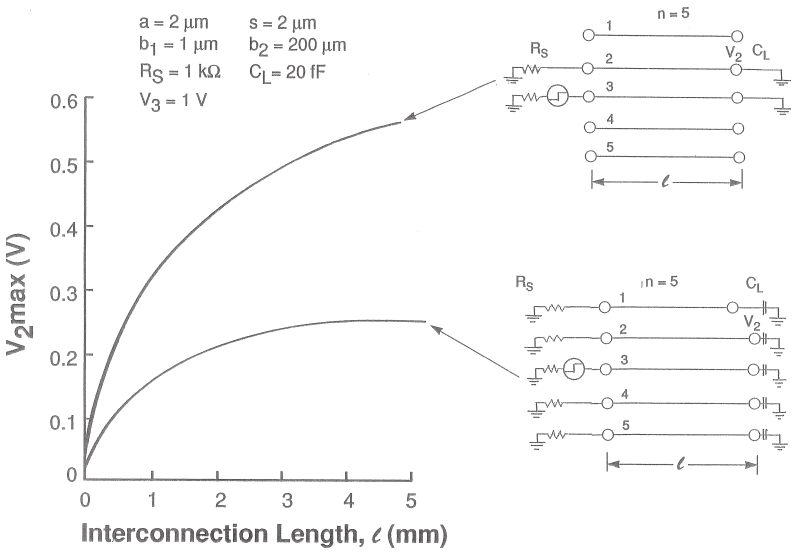

Figure 4.2.7 Crosstalk amplitude vs. the interconnection length for two systems of five interconnections with different terminal conditions [45]. (© 1984 IEEE)

multiple reflections of the wavefront appear at the initial times and the first negative peak of this transient determines the amplitude of the crosstalk waveform. The result calculated by using the "lumped capacitance" approximation is also included in Figure 4.2.8(b) which shows that this approximation is valid when *Rs* is above 2 to 3 kΩ and the response is slow.

Crosstalk Reduction

The above results suggest that for reliable operation of very high-speed very large scale integrated circuits with sufficient noise margins, it is very important to consider methods of reducing crosstalk. One method of reducing crosstalk is to reduce the substrate thickness in order to provide a solid shielding ground plane in close vicinity of the interconnections. However, this method will be effective only if the substrate thickness is reduced below 10 μm. This is clear from Figure 4.2.9 which shows the dependence of the crosstalk coupling coefficient on spacing for several values of the substrate thickness. Reducing substrate thickness below 10 μm may not be practically possible unless a new technology such as SOI is used.

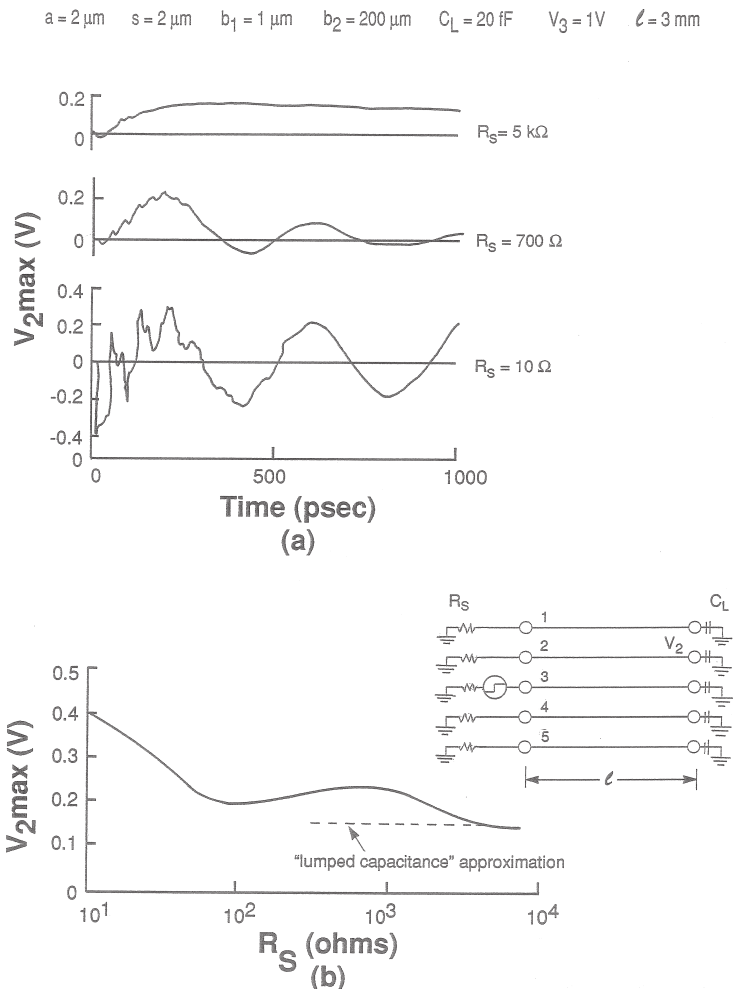

Figure 4.2.8 (a) Crosstalk waveforms for different values of the signal source resistance R_s and (b) crosstalk amplitude vs. R_s [45]. (© 1984 IEEE)

Crosstalk can also be reduced by providing shielding ground lines adjacent to the active interconnections. This is a very effective method as shown by Figure 4.2.10 which shows the dependences of the crosstalk voltage on spacing for two systems of five interconnections with and without the shielding ground lines between the interconnections. The drawback of this method is that it reduces the wiring channel capacity significantly, particularly when the availability of interconnection capacity is

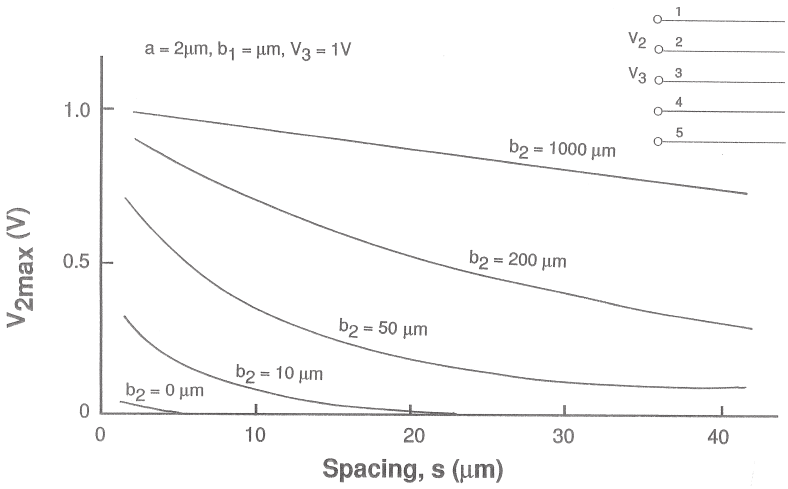

Figure 4.2.9 Crosstalk coupling coefficient vs. spacing for several values of the substrate thickness [45]. (© 1984 IEEE)

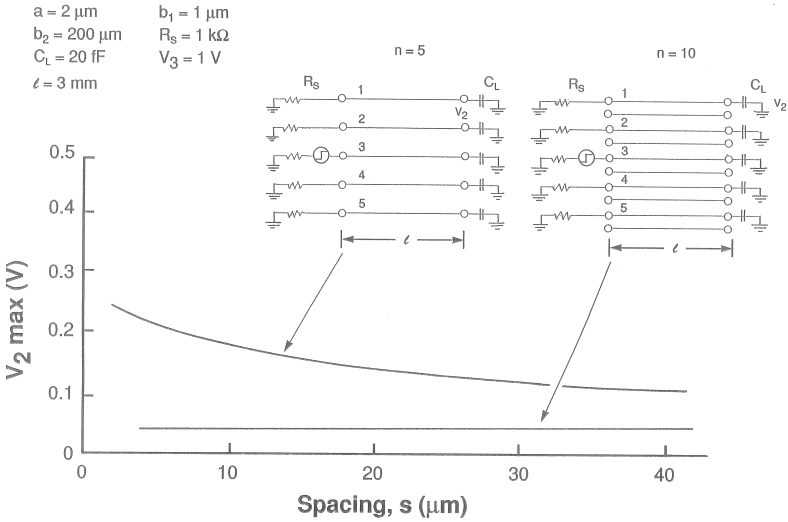

Figure 4.2.10 The effect of shielding lines on crosstalk [45]. (© 1984 IEEE)

itself a big problem in the design of very large scale integrated circuits. It is interesting to note that the potential on a narrow shielding line is not zero all along the line even if it is grounded on both ends. This is clear from Figure 4.2.11 which shows the waveforms at the centers of the adjacent line, the shielding line, and the active line.

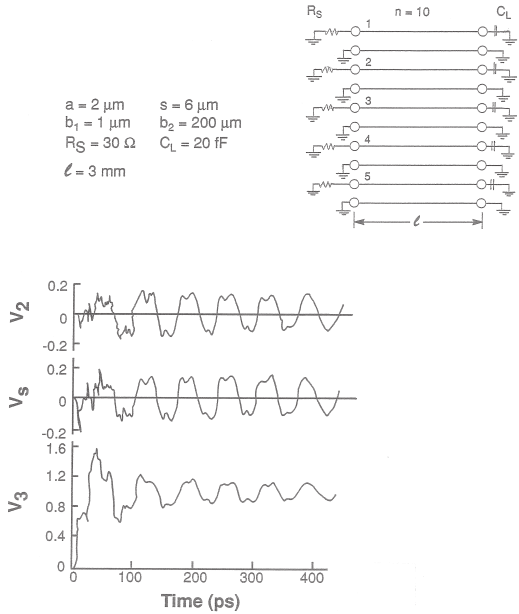

Figure 4.2.11 Waveforms at the centers of the adjacent line (V_2), the shielding line (V_S) and the active line (V_3) [4.5]. (© 1984 IEEE)

Exercise 4.2

Referring to section 4.2, show that the voltage and current on the *k*th conductor can be expressed in terms of the normal modes by the equations:

$$V_k(z) = \sum_{\theta} [A_{\theta f} e^{-j(k-1)\theta} e^{j\omega(t-(z/v_\theta))} + A_{\theta r} e^{-j(k-1)\theta} e^{j\omega(t+z/v_\theta)}]$$

$$I_k(z) = \sum_{\theta} \left[\frac{A_{\theta f}}{Z_{0\theta}} e^{-j(k-1)\theta} e^{j\omega(t-(z/v_\theta))} - \frac{A_{\theta r}}{Z_{0\theta}} e^{-j(k-1)\theta} e^{j\omega(t+z/v_\theta)} \right]$$

where z denotes the position on the conductor, ω is the angular frequency, and $A_{\theta f}$ and $A_{\theta r}$ are the amplitudes of the forward and backward voltage waves in the θ-mode.

Exercise 4.3

The mode wave amplitudes $A_{\theta f}$ and $A_{\theta r}$ in Exercise 4.2 can be determined by using the known terminal conditions at both ends of each strip conductor. Assuming a variety of terminal conditions, find these amplitudes.

4.3 Frequency-Domain Modal Analysis of Single-Level Interconnections

Now, a general technique for analyzing crosstalk in coupled single-level lossless interconnections [16] will be presented. The analysis is carried out without making the weak-coupling or cyclic boundary condition assumptions. First, modal analysis has been done in the frequency domain to obtain the closed-form expressions for the voltage and current transfer functions. Then the transfer function is expanded into its Taylor series and the inverse Fourier transformation is applied to the terms considered significant depending on the accuracy desired in the solution.

The General Technique

Consider a system of N interconnection lines shown in Figure 4.3.1. Let $[C]$, $[L]$, and $[R]$ denote the capacitance, inductance, and resistance matrices of the system. Further, let $E_n(t)$, Z_{Gn}, and Z_{Ln} denote the input signal, the source impedance, and the load impedance for the *nth* line where $n = 1, 2, \ldots, N$. Let ℓ be the length of each interconnection line. We define the series impedance matrix $[Z]$ and the parallel admittance matrix $[Y]$ as $[Z] = [R] + j^{\omega}[L]$ and $[Y] = j^{\omega}[C]$.

The N propagation modes that exist in a system of N conductors are defined by N complex modal propagation constants $\gamma_n = \alpha_n + j\omega\beta_n$ where $n = 1, 2, \ldots, N$. Then elements of the voltage eigenvector matrix $[S_v]$ are solutions of the eigenvalue equation

$$(\gamma^2[I] + [Z][Y])[S_v] = [0] \tag{4.3.1}$$

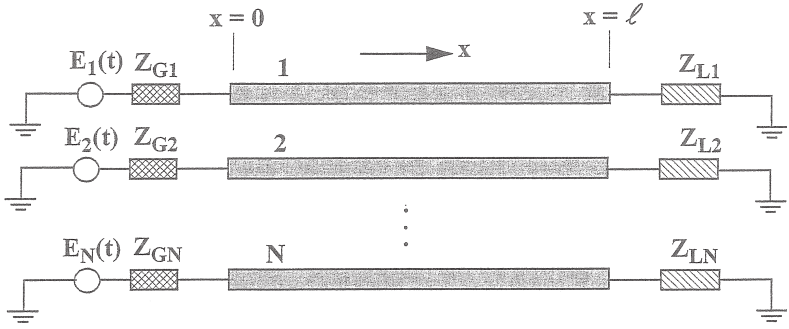

Figure 4.3.1 Schematic diagram of a system of N coupled interconnection lines [4.16]. (© 1990 IEEE)

and the current eigenvector matrix $[S_I]$ is given by

$$[S_I] = [Z]^{-1}[S_v][\Gamma] \tag{4.3.2}$$

where $[I]$ is the identity matrix and $[\Gamma] = \text{diag}\{\gamma_1, \gamma_2, \ldots, \gamma_n\}$. The characteristic impedance matrix $[Z_c]$ is given by $[S_v][S_I]^{-1}$ and the characteristic admittance matrix $[Y_c]$ is equal to $[Z_c]^{-1}$. Then the voltage and current vectors on the interconnection line can be expressed in terms of $[S_v]$ and $[S_I]$ as:

$$[V(x)] = [S_v]([W_i(x)] + [W_r(x)]) \tag{4.3.3}$$

$$[I(x)] = [Y_c][S_v]([W_i(x)] - [W_r(x)]) \tag{4.3.4}$$

where

$$[W_i(x)] = [W_{i,n}(0)(e^{-\gamma_n x})]$$

$$[W_r(x)] = [W_{r,n}(0)(e^{\gamma_n x})] \tag{4.3.5}$$

and $W_{i,n}$ and $W_{r,n}$ are the amplitudes of the incident and the reflected components of the *nth* mode. The voltage and current vectors satisfy the following boundary conditions:

$$[V(0)] = [E] - [Z_G][I(0)]$$

$$[V(\ell)] = [Z_L][I(\ell)] \tag{4.3.6}$$

where $[E] = [E_n]$, $[Z_G] = \text{diag}\{Z_{G1}, Z_{G2}, \ldots, Z_{GN}\}$, $[Z_L] = \text{diag}\{Z_{L1}, Z_{L2}, \ldots, Z_{LN}\}$, E_n is the input voltage signal applied to the *nth* line, Z_{Gn} is the internal impedance of the *nth* input signal source, and Z_{Ln} is the load impedance of the *nth* line. Substituting equations (4.3.3) and (4.3.4) into Eqn. (4.3.5), we obtain the following linear equations for $[W_i(0)]$ and $[W_r(0)]$:

$$\begin{bmatrix} [S_v] + [Z_G][S_I] & [S_v] - [Z_G][S_I] \\ ([S_v] - [Z_L][S_I])[P] & ([S_v] + [Z_L][S_I])[P]^{-1} \end{bmatrix} \begin{bmatrix} [W_i(0)] \\ [W_r(0)] \end{bmatrix} = \begin{bmatrix} [E] \\ [0] \end{bmatrix} \tag{4.3.7}$$

where $[P] = \text{diag}\{\exp(-\gamma_n 1)\}$. After solving Eqn. (4.3.6) for $[W_i(0)]$ and $[W_r(0)]$, the voltage and current transfer functions can be determined from the voltage and current spectra obtained from Eqn. (4.3.3).

In general, first, the voltage and current are calculated at a finite number of discreet frequencies and then the time domain waveforms are obtained by using the fast Fourier transform technique. If the lines can be considered lossless and are terminated at one or both ends by the line characteristic impedances, then analytical inverse Fourier transformation can be used to obtain the closed-form expressions for the time-domain waveforms as shown below for the two-, three-, and four-line systems.

Two-Line System

The capacitance and inductance matrices for a two-line system can be written as

$$[C] = \begin{bmatrix} C_{11} & -C_{12} \\ -C_{21} & C_{22} \end{bmatrix}$$

$$[L] = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \tag{4.3.8}$$

with $C_{11} = C_{22}$, $C_{12} = C_{21}$, $L_{11} = L_{22}$ and $L_{12} = L_{21}$. The propagation modes $\gamma_n = j\omega\beta_n$ ($n = 1, 2$) of the two modes can be obtained by solving equations (4.3.1) and (4.3.2) to be

$$\gamma_1 = j\omega\sqrt{(L_{11} + L_{12})(C_{11} - C_{12})}$$

$$\gamma_2 = j\omega\sqrt{(L_{11} - L_{12})(C_{11} + C_{12})} \tag{4.3.9}$$

Then, the voltage and current eigenvector matrices and the characteristic impedance matrix are given by

$$[S_V] = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$[S_I] = \begin{bmatrix} \frac{1}{Z_1} & \frac{1}{Z_2} \\ \frac{1}{Z_1} & -\frac{1}{Z_2} \end{bmatrix}$$

$$\left[Z_c\right] = \left(\frac{1}{2}\right)\begin{bmatrix} Z_1 + Z_2 & Z_1 - Z_2 \\ Z_1 - Z_2 & Z_1 + Z_2 \end{bmatrix} \tag{4.3.10}$$

where

$$Z_1 = \left[\frac{L_{11} + L_{12}}{C_{11} - C_{12}}\right]^{1/2}$$

and

$$Z_2 = \left[\frac{L_{11} - L_{12}}{C_{11} + C_{12}}\right]^{1/2} \tag{4.3.11}$$

Suppose that the load impedances of the two lines are the same, i.e., $Z_{L1} = Z_{L2} = Z_L$, the source impedances of the two lines are the same, i.e., $Z_{G1} = Z_{G2} = Z_G$ and that the signal source $E_1(t)$ is applied to line 1. Then the voltage transfer functions can be obtained to be

$$\frac{V_{1,2}(x,\omega)}{E_1(\omega)} = \frac{1}{2}\left[\frac{1}{P_1}\left(\frac{e^{-\gamma_1 x} + \rho_{L1}e^{-\gamma_1(2\ell - x)}}{1 - \rho_{L1}\rho_{G1}e^{-2\gamma_1 \ell}}\right)\right.$$
$$\left. \pm \frac{1}{P_2}\left(\frac{e^{-\gamma_2 x} + \rho_{L2}e^{-\gamma_2(2\ell - x)}}{1 - \rho_{L2}\rho_{G2}e^{-2\gamma_2 \ell'}}\right)\right] \tag{4.3.12}$$

where

$$\rho_{Ln} = \frac{Z_L - Z_n}{Z_L + Z_n};\ n = 1, 2$$

$$\rho_{Gn} = \frac{Z_G - Z_n}{Z_G + Z_n};\ n = 1, 2$$

and

$$P_n = 1 + \frac{Z_G}{Z_n};\ n = 1, 2 \tag{4.3.13}$$

If the source impedances applied to the two interconnection lines are each equal to Zcc defined as the characteristic impedance of an isolated line, i.e., $Z_G \approx Z_{cc}$, then $\rho_{Gn} \approx 0$ ($n = 1, 2$) and Eqn. (4.3.12) becomes

$$\frac{V_{1,2}(x, \omega)}{E_1(\omega)} = \frac{1}{2}\left[\frac{1}{P_1}(e^{-\gamma_1 x} + \rho_{L1} e^{-\gamma_1(2\ell - x)}) \pm \frac{1}{P_2}(e^{-\gamma_2 x} + \rho_{L2} e^{-\gamma_2(2\ell - x)})\right] \quad (4.3.14)$$

Further, if the load impedances of the two lines are each equal to Z_{cc}, then Eqn. (4.3.14) still holds but with $\rho L_n \approx 0$ ($n = 1, 2$).

The closed-form expressions in the time domain can now be determined by the inverse Fourier transformations of the voltage transfer functions given by Eqn. (4.3.14) to be

$$V_{1,2}(x, t) = \frac{1}{2}\left[\left\{\frac{1}{P_1}E_1\left(t - \frac{x}{v_1}\right) \pm \frac{1}{P_2}E_1\left(t - \frac{x}{v_2}\right)\right\} + \left\{\frac{\rho_{L1}}{P_1}E_1\left(t - \frac{2\ell - x}{v_1}\right) \pm \frac{\rho_{L2}}{P_2}E_1\left(t - \frac{2\ell - x}{v_2}\right)\right\}\right] \quad (4.3.15)$$

where $v_n = j\omega/\gamma_n = 1/\beta_n$ ($n = 1, 2$) are the two propagation velocities.

It is clear from Eqn. (4.3.15) that one source of crosstalk noise is the mismatch between the propagation velocities of different modes. In addition, Eqn. (4.3.14) indicates that the coupling of the active line with its neighbors degrades the input signal as it travels along the active line.

Three-Line System

Consider a system of three interconnection lines with matched loads having three propagation modes. If the matrix $[A]$ denotes the product of the matrices $[L]$ and $[C]$, i.e., $[A] = [L][C]$, then the propagation constants of the three modes will be given by

$$\gamma_1 = j\omega(A_{11} - A_{13})$$

$$\gamma_2 = \frac{1}{\sqrt{2}}j\omega[A_{11} + A_{13} + A_{22} + \sqrt{(A_{11} + A_{13} - A_{22})^2 + 8A_{12}A_{21}}]^{0.5}$$

$$\gamma_3 = \frac{1}{\sqrt{2}} j\omega [A_{11} + A_{13} + A_{22} - \sqrt{(A_{11} + A_{13} - A_{22})^2 + 8A_{12}A_{21}}]^{0.5} \tag{4.3.16}$$

and the voltage eigenvector matrix is given by

$$[S_v] = \begin{bmatrix} 1 & 1 & 1 \\ 0 & \eta_2 & \eta_3 \\ -1 & 1 & 1 \end{bmatrix} \tag{4.3.17}$$

where

$$\eta_2 = \frac{(A_{22} - A_{11} - A_{13}) + \sqrt{(A_{22} - A_{11} - A_{13})^2 + 8A_{12}A_{21}}}{2A_{12}}$$

and

$$\eta_3 = \frac{(A_{22} - A_{11} - A_{13}) - \sqrt{(A_{22} - A_{11} - A_{13})^2 + 8A_{12}A_{21}}}{2A_{12}} \tag{4.3.18}$$

If the input signal $E_1(t)$ is applied to line 1 (the active line), source impedances are much smaller as compared to the line characteristic impedances Z_{cc}, i.e., $Z_{Gn} = 0$ and if the load impedances are each equal to Z_{cc}, i.e., $Z_{Ln} = Z$ ($n = 1, 2, 3$), then the closed-form expressions for the line voltage waveforms can be determined by following the same steps as for the two-line system to be

$$V_1(x, t) = \frac{1}{2}\left[E_1\left(t - \frac{x}{v_1}\right) - \frac{\eta_3}{\eta_2 - \eta_3}E_1\left(t - \frac{x}{v_2}\right) + \frac{\eta_2}{\eta_2 - \eta_3}E_1\left(t - \frac{x}{v_3}\right)\right]$$

$$V_2(x, t) = \frac{1}{2}\left(\frac{\eta_2\eta_3}{\eta_2 - \eta_3}\right)\left[-E_1\left(t - \frac{x}{v_2}\right) + E_1\left(t - \frac{x}{v_3}\right)\right]$$

$$V_3(x, t) = \frac{1}{2}\left[-E_1\left(t - \frac{x}{v_1}\right) - \frac{\eta_3}{\eta_2 - \eta_3}E_1\left(t - \frac{x}{v_2}\right) + \frac{\eta_2}{\eta_2 - \eta_3}E_1\left(t - \frac{x}{v_3}\right)\right]$$

(4.3.19)

Four-Line System

Consider a system of four interconnection lines with matched loads having four propagation modes. If the matrix $[A]$ denotes the product of the matrices $[L]$ and $[C]$, i.e., $[A] = [L][C]$, then the propagation constants of the four modes will be given by

$$\gamma_1 = \frac{j\omega}{\sqrt{2}}[(A_{11}+A_{14}+A_{22}+A_{23}) + \sqrt{(A_{11}+A_{14}-A_{22}-A_{23})^2+4(A_{12}+A_{13})(A_{21}+A_{31})}]^{0.5}$$

$$\gamma_2 = \frac{j\omega}{\sqrt{2}}[(A_{11}+A_{14}+A_{22}+A_{23}) - \sqrt{(A_{11}+A_{14}-A_{22}-A_{23})^2+4(A_{12}+A_{13})(A_{21}+A_{31})}]^{0.5}$$

$$\gamma_3 = \frac{j\omega}{\sqrt{2}}[(-A_{11}+A_{14}+A_{22}-A_{23}) + \sqrt{(A_{11}-A_{14}-A_{22}+A_{23})^2+4(A_{12}-A_{13})(A_{21}-A_{31})}]^{0.5}$$

$$\gamma_4 = \frac{j\omega}{\sqrt{2}}[(-A_{11}+A_{14}+A_{22}-A_{23}) - \sqrt{(A_{11}-A_{14}-A_{22}+A_{23})^2+4(A_{12}-A_{13})(A_{21}-A_{31})}]^{0.5} \quad (4.3.20)$$

and the voltage eigenvector is given by

$$\left[S_v\right] = \begin{bmatrix} 1 & 1 & 1 & 1 \\ \eta_1 & \eta_2 & \eta_3 & \eta_4 \\ \eta_1 & \eta_2 & -\eta_3 & -\eta_4 \\ 1 & 1 & -1 & -1 \end{bmatrix} \quad (4.3.21)$$

where

$$\eta_1 = [(-A_{11} - A_{14} + A_{22} + A_{23}) + \sqrt{(A_{11} + A_{14} - A_{22} - A_{23})^2 + 4(A_{12} + A_{13})(A_{21} + A_{31})}]/[2(A_{12} + A_{13})]$$

$$\eta_2 = [(-A_{11} - A_{14} + A_{22} + A_{23}) - \sqrt{(A_{11} + A_{14} - A_{22} - A_{23})^2 + 4(A_{12} + A_{13})(A_{21} + A_{31})}]/[2(A_{12} + A_{13})]$$

$$\eta_3 = [(-A_{11} + A_{14} + A_{22} - A_{23}) + \sqrt{(A_{11} - A_{14} - A_{22} + A_{23})^2 + 4(A_{12} - A_{13})(A_{21} - A_{31})}]/[2(A_{12} - A_{13})]$$

$$\eta_4 = [(-A_{11} + A_{14} + A_{22} - A_{23}) - \sqrt{(A_{11} - A_{14} - A_{22} + A_{23})^2 + 4(A_{12} - A_{13})(A_{21} - A_{31})}]/[2(A_{12} - A_{13})] \tag{4.3.22}$$

If the input signal $E_1(t)$ is applied to line 1 (the active line), source impedances are much smaller as compared to the line characteristic impedances Z_{cc}, i.e., $Z_{Gn} = 0$ and if the load impedances are each equal to Z_{cc}, i.e., $Z_{Ln} = Z_{cc}$ ($n = 1, 2, 3, 4$), then the closed-form expressions for the line voltage waveforms can be determined by following the same steps as for the two-line system to be

$$V_1(x, t) = \frac{1}{2}\left[-\alpha_2 E_1\left(t - \frac{x}{v_1}\right) + \alpha_1 E_1\left(t - \frac{x}{v_2}\right) - \alpha_4 E_1\left(t - \frac{x}{v_3}\right) + \alpha_3 E_1\left(t - \frac{x}{v_4}\right)\right]$$

$$V_2(x, t) = \frac{1}{2}\left[\beta_1\left\{-E_1\left(t - \frac{x}{v_1}\right) + E_1\left(t - \frac{x}{v_2}\right)\right\} + \beta_2\left\{-E_1\left(t - \frac{x}{v_3}\right) + E_1\left(t - \frac{x}{v_4}\right)\right\}\right]$$

$$V_3(x,t) = \frac{1}{2}\left[\beta_1\left\{-E_1\left(t-\frac{x}{v_1}\right)+E_1\left(t-\frac{x}{v_2}\right)\right\}-\right.$$
$$\left.-\beta_2\left\{-E_1\left(t-\frac{x}{v_3}\right)+E_1\left(t-\frac{x}{v_4}\right)\right\}\right]$$

$$V_4(x,t) = \frac{1}{2}\left[-\alpha_2 E_1\left(t-\frac{x}{v_1}\right)+\alpha_1 E_1\left(t-\frac{x}{v_2}\right)\right.$$
$$\left.+\alpha_4 E_1\left(t-\frac{x}{v_3}\right)-\alpha_3 E_1\left(t-\frac{x}{v_4}\right)\right] \qquad (4.3.23)$$

where

$$v_n = \frac{j\omega}{\gamma_n};\ n = 1, 2, 3, 4$$

$$\alpha_1 = \frac{\eta_1}{\eta_1-\eta_2}$$

$$\alpha_2 = \frac{\eta_2}{\eta_1-\eta_2}$$

$$\alpha_3 = \frac{\eta_3}{\eta_3-\eta_4}$$

$$\alpha_4 = \frac{\eta_4}{\eta_3-\eta_4}$$

$$\beta_1 = \alpha_1\eta_2 = \alpha_2\eta_1$$

$$\beta_2 = \alpha_3\eta_4 = \alpha_4\eta_3 \qquad (4.3.24)$$

Simulation Results

A schematic diagram of the coupled interconnections in high-speed circuits and systems is shown in Figure 4.3.1 and the layout of the *N*

uniformly coupled 50 Ω interconnections used in the simulations given below [16] is shown in Figure 4.3.2. Referring to Figure 4.3.1, we have set $Z_{Gn} = 0$ and $Z_{Ln} = 50\ \Omega$, where $n = 1, 2, \ldots, N$. In Figure 4.3.2, unless otherwise stated, the interconnections are assumed to be of negligible thickness, the substrate is alumina with permittivity $\varepsilon_r = 10$, the width of each interconnection (W) is equal to the substrate thickness (H), the distance between any two adjacent conductors (S) is 1.5H, the length of each coupled line is 20 cm, and a ramp signal having amplitude of 1V and rise time of 100 ps is applied to line 1 (the active line).

For a system of two interconnection lines, the time-domain voltage waveforms at the load ends of the active line and the neighboring line determined by Eqn. (4.3.15) are shown in Figure 4.3.3. The capacitance and inductance matrices used in these results determined by the Green's function method are

$$[C] = \begin{bmatrix} 1.737 & -0.073 \\ -0.073 & 1.737 \end{bmatrix} \ p\text{F/cm}$$

$$[L] = \begin{bmatrix} 4.276 & 0.529 \\ 0.529 & 4.276 \end{bmatrix} \ n\text{H/cm}$$

For the sake of comparison, Figure 4.3.3 also shows the analysis results from reference [12] where weak coupling was assumed. It is clear that the weak coupling approximation can result in significant errors in crosstalk calculations. For the two-line system, the amplitude of the

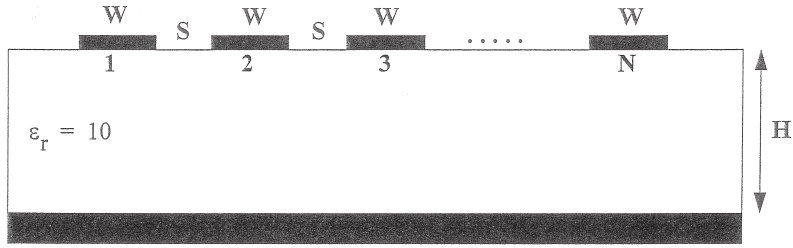

Figure 4.3.2 Layout of N uniformly coupled 50Ω interconnections on an alumina substrate [4.16]. (© 1990 IEEE)

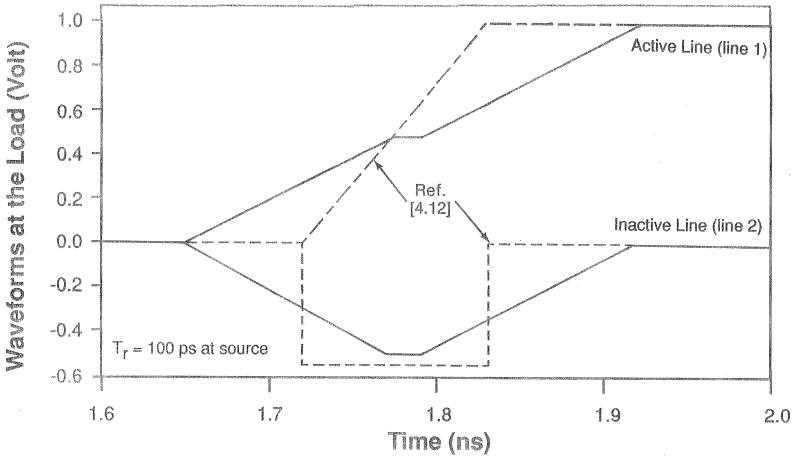

Figure 4.3.3 Signal waveforms at the load ends for the two-line system shown in Fig. 4.3.2 with N = 2 [4.16]. (© 1990 IEEE)

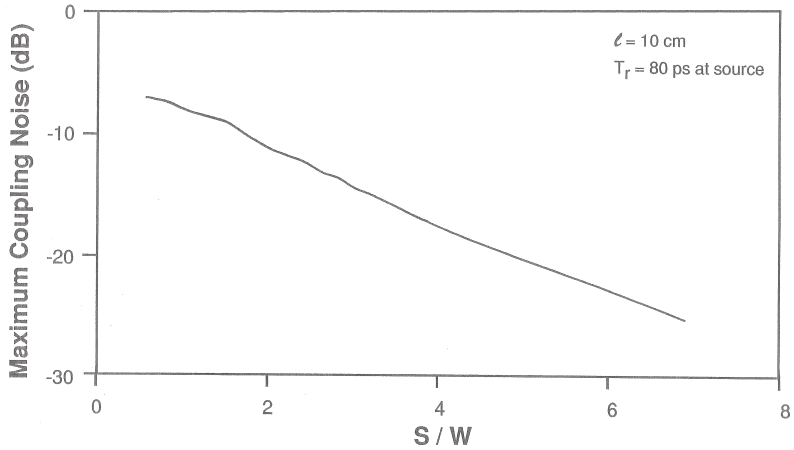

Figure 4.3.4 Amplitude of the load-end coupling noise as a function of the layout parameter S/W for the two-line system shown in Fig. 4.3.2 with N = 2 [4.16]. (© 1990 IEEE)

coupling noise at the load end as a function of the layout parameter S/W is plotted in Figure 4.3.4. Figure 4.3.5 shows the influences of the length of the coupled lines and the rise time of the input signal on the amplitude of the coupling noise.

For a system of three interconnection lines, the time-domain voltage waveforms at the load ends of the active line and the neighboring lines determined by Eqn. (4.3.19) are shown in Figure 4.3.6. The capacitance

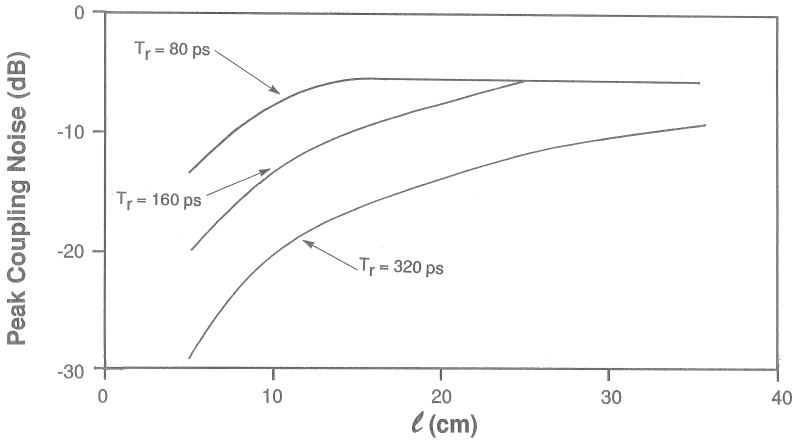

Figure 4.3.5 Dependences of the peak coupling noise on the length (ℓ) of the coupled lines of the two-line system for different values of the rise time (T_r) of the signal source [4.16]. (© 1990 IEEE)

and inductance matrices used in these results determined by the Green's function method are

$$[C] = \begin{bmatrix} 1.737 & -0.073 & -0.005 \\ -0.073 & 1.741 & -0.073 \\ -0.005 & -0.073 & 1.737 \end{bmatrix} \; p\text{F/cm}$$

$$[L] = \begin{bmatrix} 4.276 & 0.527 & 0.159 \\ 0.527 & 4.269 & 0.527 \\ 0.159 & 0.527 & 4.276 \end{bmatrix} \; n\text{H/cm}$$

The results assuming weak coupling from reference [12] are also included in Figure 4.3.6 and indicate that this approximation is not satisfactory for typical interconnection configurations.

For a system of four interconnection lines, the time-domain voltage waveforms at the load ends of the active line and the disturbed lines determined by Eqn. (4.3.23) are shown in Figure 4.3.7. The capacitance and inductance matrices used in these results determined by the Green's function method are

$$[C] = \begin{bmatrix} 1.737 & -0.073 & -0.004 & -0.002 \\ -0.073 & 1.742 & -0.073 & -0.004 \\ -0.004 & -0.073 & 1.742 & -0.073 \\ -0.002 & -0.004 & -0.073 & 1.737 \end{bmatrix} \; p\text{F/cm}$$

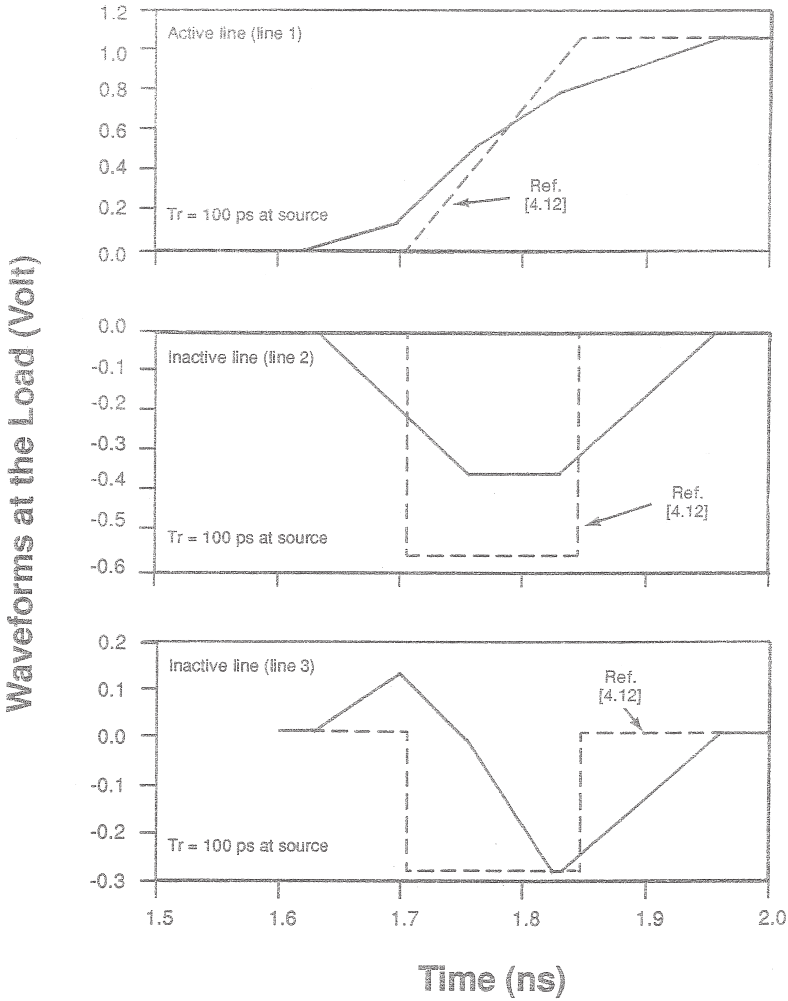

Figure 4.3.6 Signal waveforms at the load ends for the three-line system shown in Fig. 4.3.2 with N = 3 [4.16]. (© 1990 IEEE)

$$[L] = \begin{bmatrix} 4.276 & 0.527 & 0.158 & 0.072 \\ 0.527 & 4.269 & 0.526 & 0.158 \\ 0.158 & 0.526 & 4.269 & 0.527 \\ 0.072 & 0.158 & 0.527 & 4.276 \end{bmatrix} \text{ nH/cm}$$

The reduction of crosstalk by placing grounded conductors between the signal lines is demonstrated in Figure 4.3.8 which shows the load voltage waveforms on line 2 when a ramp signal having amplitude of 1 V and rise time of 80 ps is applied to line 1 for the cases of two signal lines only

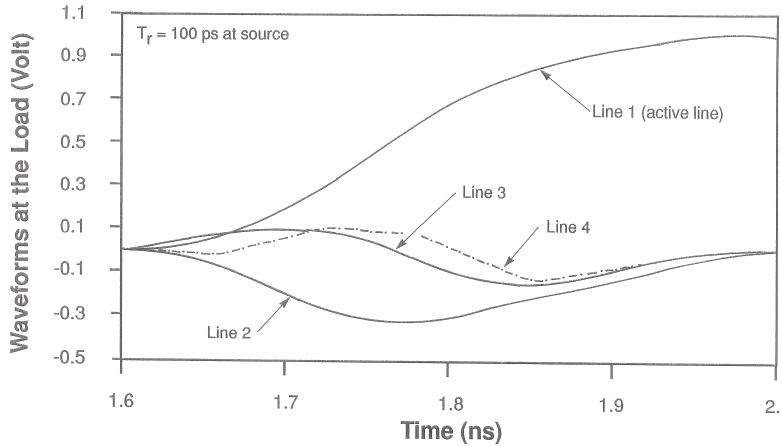

Figure 4.3.7 Signal waveforms at the load ends for the four-line system shown in Fig. 4.3.2 with N = 4 [4.16]. (© 1990 IEEE)

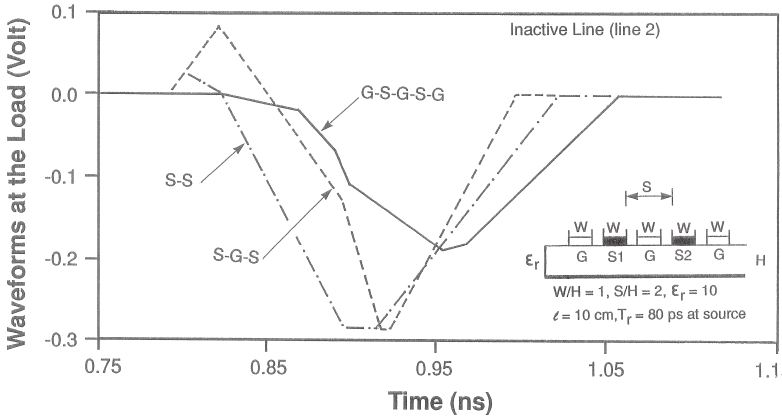

Figure 4.3.8 Load waveforms for the signal-signal (S-S), signal-ground-signal (S-G-S) and ground-signal-ground-signal-ground (G-S-G-S-G) configurations [4.16]. (© 1990 IEEE)

(S-S), for two signal lines with a grounded-shield conductor in between (G-G-S), and for two signal lines with grounded-shield conductors in between as well as on both sides (G-S-G-S-G). It is clear from the simulation results that the grounded conductors should be placed on both sides of each signal line to reduce crosstalk significantly. However, it should be noted that the insertion of ground conductors not only increases the complexity of the circuit, but also causes waveform distortion for the signal on the active line.

4.4 Transmission Line Analysis of Parallel Multilevel Interconnections

Here, the crosstalk among the parallel multilevel interconnections is studied by modeling the interconnections as transmission lines. The model has been utilized to study the dependences of the crosstalk voltage on the interconnection parameters such as their length, widths, separations, interlevel distances, driving transistor resistance, and the load capacitance.

The Model

As shown in Figure 4.4.1, the interconnection line can be modeled as a transmission line driven by a unit step voltage source having resistance R_S, loaded by the capacitance $C_{L,}$ and coupled to the neighboring interconnection lines by the mutual capacitances and inductances (not shown in the figure). The resistance R_S is determined by the dimensions of the driving transistor and the capacitance C_L is determined by the parasitic capacitances of the transistor loading the interconnection line. For the interconnection lines printed on or embedded in the semi-insulating GaAs substrate, quasi-TEM is the dominant mode of wave propagation, and the transmission line equations are given by

$$\frac{\partial}{\partial x}V(x,t) = -\left[R + L\frac{\partial}{\partial t}\right]I(x,t) \qquad (4.4.1)$$

$$\frac{\partial}{\partial x}I(x,t) = -\left[G + C\frac{\partial}{\partial t}\right]V(x,t) \qquad (4.4.2)$$

where L and C are the inductance and capacitance matrices per unit length of the interconnections, R is determined by the resistance per unit length of the interconnections and G is the conductance matrix determined by the conductivity of the substrate. For semi-insulating GaAs substrate, G can be neglected. The matrices L and C can be determined by the network analog method developed in chapter 2. In the s-domain, equations (4.4.1) and (4.4.2) can be written as

$$\frac{d}{dx}V(x,s) = -[R + sL]\ I(x,s) \qquad (4.4.3)$$

$$\frac{d}{dx}I(x,s) = -[G + s_C]\ V(x,s) \qquad (4.4.4)$$

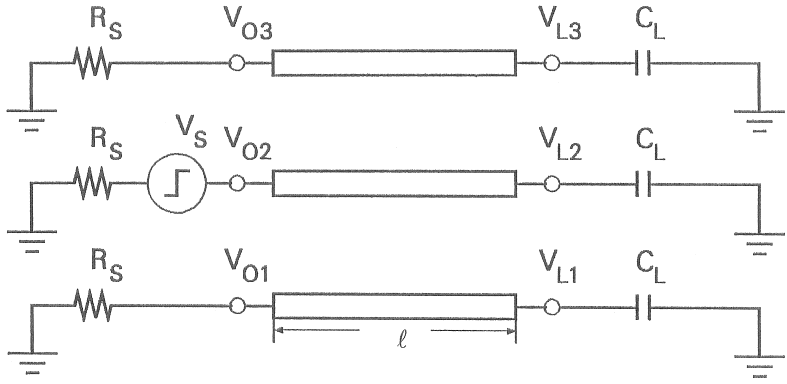

Figure 4.4.1 Interconnection driven by a unit step voltage source Vs of resistance R_S and terminated by the load capacitance C_L. The terminal ending on the neighboring interconnections are also shown. Interconnection capacitances as well as the capacitive and inductive couplings between the interconnections are not shown in the figure.

Defining

$$Z = R + sL$$

and

$$Y = G + sC$$

the equations (4.4.3) and (4.4.4) can be solved in the s-domain, yielding

$$V(x, s) = e^{-\sqrt{ZY}(x)} V_i(s) + e^{-\sqrt{ZY}(\ell - x)} V_r(s) \tag{4.4.5}$$

$$I(x, s) = \sqrt{\frac{Y}{Z}} [e^{-\sqrt{ZY}(x)} (V_i s) - e^{-\sqrt{ZY}(\ell - x)} V_r(s)] \tag{4.4.6}$$

In equations (4.4.5) and (4.4.6), ℓ is the total length of the transmission line, $V_i(s)$ is the voltage vector of the incident wave at $x = 0$ and $V_r(s)$ is that of the reflected wave at $x = \ell$. At the end points, $x = 0$ and $x = \ell$, equations (4.4.5) and (4.4.6) yield

$$V(0, s) = V_i(s) + e^{-\sqrt{ZY}\ell} V_r(s) \tag{4.4.7}$$

$$I(0, s) = \sqrt{\frac{Y}{Z}}[V_i(s) - e^{-\sqrt{ZY}\ell}V_r(s)] \tag{4.4.8}$$

$$V(\ell, s) = e^{-\sqrt{ZY}\ell}V_i(s) + V_r(s) \tag{4.4.9}$$

$$I(\ell, s) = \sqrt{\frac{Y}{Z}}[e^{-\sqrt{ZY}\ell}V_i(s) - V_r(s)] \tag{4.4.10}$$

Incorporating the boundary conditions determined by the lumped circuit elements connected to the interconnection line, i.e.,

$$V(0, s) = V_s(s) - R_S I(0, s) \tag{4.4.11}$$

and

$$V(\ell, s) = \frac{1}{sC_L} I(\ell, s), \tag{4.4.12}$$

we have

$$V_i(s) + e^{(-\sqrt{ZY})\ell}V_r(s) = (-R_s)\sqrt{\frac{Y}{Z}}[V_i(s) - e^{-\sqrt{ZY}\ell}V_r(s)] + V_s(s) \tag{4.4.13}$$

and

$$e^{-\sqrt{ZY}\ell}V_i(s) + V_r(s) = -\left(\frac{1}{sC_L}\right)\sqrt{\frac{Y}{Z}}[e^{-\sqrt{ZY}\ell}V_i(s) - V_r(s)] \tag{4.4.14}$$

which can be solved to yield for $V_i(s)$ and $V_r(s)$:

$$V_r(s) = V_s(s)\left\{-\left[I + R_s\sqrt{\frac{Y}{Z}}\right][e^{\sqrt{ZY}\ell}]\left[I - \frac{1}{sC_L}\sqrt{\frac{Y}{Z}}\right]^{-1}\left[I + \frac{1}{sC_L}\sqrt{\frac{Y}{Z}}\right] + \left[I - R_s\sqrt{\frac{Y}{Z}}\right]\left[\frac{1}{e^{\sqrt{ZY}\ell}}\right]\right\}^{-1} \tag{4.4.15}$$

$$V_i(s) = -\left[e^{-\sqrt{ZY}\ell} - \frac{1}{sC_L}\sqrt{\frac{Y}{Z}}e^{-\sqrt{ZY}\ell}\right]^{-1}\left[I + \frac{1}{sC_L}e^{-\sqrt{ZY}\ell}\right]V_r(s) \tag{4.4.16}$$

The values for $V_i(s)$ and $V_r(s)$ can be substituted in equations (4.4.7 to (4.4.10) to obtain the expressions for current and voltage at $x = 0$ and $x = \ell$ in the s-domain. The load voltage is the element of $V(\ell, s)$ that corresponds to the line on which the voltage source is applied. The other elements of $V(\ell, s)$ represent the crosstalk voltages induced on the neighboring interconnection lines. Finally, the time-domain load voltage can be obtained by an inverse Laplace transformation of $V(\ell, s)$. The reader is encouraged to use the algorithm presented above to study the crosstalk among the interconnections in the configurations shown in Figures 4.4.2(a, b, and c).

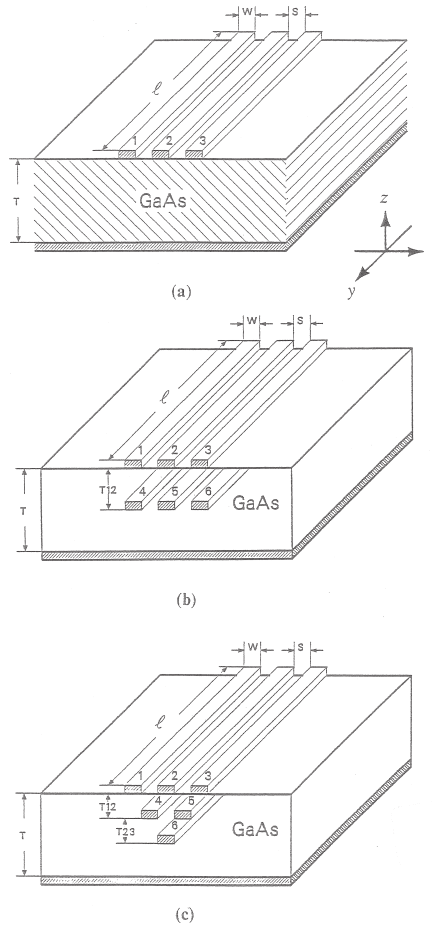

Figure 4.4.2 Schematic diagram of (a) three single-level (b) six bi-level and (c) six tri-level interconnection configurations. The various design parameters are also shown in the figure.

4.5 Compact Expressions for Crosstalk Analysis

Here, compact, i.e., closed-form expressions for the voltage waveforms under worst-case crosstalk conditions at the load end of a quiet interconnection are presented. First, two coupled interconnections are modeled as a distributed *RC* networks [27] and then these are treated as open-circuited distributed *RLC* networks [22]. Finally, the analysis is extended to three coupled open-circuited interconnections modeled as distributed as *RLC* networks [22]. An analysis of capacitively terminated single and coupled *RLC* interconnections is presented in reference [23].

Distributed RC Model for Two Coupled interconnections

Consider two interconnection lines of length ℓ each represented as distributed R_C networks as shown in Figure 4.5.1. R and C represent the total resistance and capacitance of each line, respectively, assumed equal for simplicity. C_C represents the total coupling capacitance between the two interconnections. The two interconnections are driven by two-step voltage sources V_{S1} and V_{S2} with internal resistances R_{S1} and R_{S2}, respectively. C_{L1} and C_{L2} are the capacitive loads on the two interconnections. The basic differential equations which govern the voltage waveforms V_1 and V_2 along these two coupled interconnections are described as:

$$\frac{1}{r_1}\left(\frac{\partial^2 V_1}{\partial x^2}\right) = (c_1 + c_2)\left(\frac{\partial V_1}{\partial t}\right) - c_c\left(\frac{\partial V_2}{\partial t}\right) \tag{4.5.1}$$

$$\frac{1}{r_2}\left(\frac{\partial^2 V_2}{\partial x^2}\right) = (c_1 + c_2)\left(\frac{\partial V_2}{\partial t}\right) - c_c\left(\frac{\partial V_1}{\partial t}\right) \tag{4.5.2}$$

where r_1 and r_2 denote the resistances of the two lines per unit length, c_1 and c_2 denote the capacitances of the two lines, while c_c denotes the coupling capacitance between the two lines per unit length. In other words, $R_1 = r_1(\ell)$, $R_2 = r_2(\ell)$, and $C_C = c_c(\ell)$. For simplicity, we will assume that $r_1 = r_2 = r$ and $c_1 = c_2 = c$. Equations (4.5.1) and (4.5.2) can be

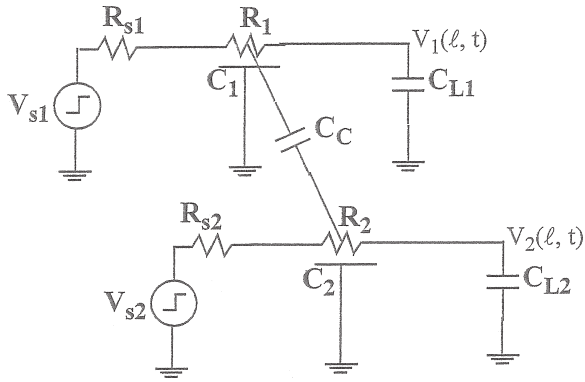

Figure 4.5.1 Two interconnection lines represented as coupled RC lines [from 4.27] (© IEEE 1993)

solved to yield the following closed-form expressions for the load voltage waveforms $V_1(\ell, t)$ and $V_2(\ell, t)$:

$$V_1(\ell, t) \approx V_{s1} + \frac{K_1}{2}\left\{(V_{S1} + V_{S2})\exp\left(-\frac{\sigma_1 \cdot t}{RC}\right)\right.$$

$$\left. + (V_{S1} - V_{S2})\exp\left(-\frac{\sigma_1 \cdot t}{RC + 2RC_C}\right)\right\} \tag{4.5.3}$$

$$V_2(\ell, t) \approx V_{s2} + \frac{K_1}{2}\left\{(V_{S1} + V_{S2})\exp\left(-\frac{\sigma_1 \cdot t}{RC}\right)\right.$$

$$\left. -(V_{S1} - V_{S2})\exp\left(-\frac{\sigma_1 \cdot t}{RC + 2RC_C}\right)\right\} \tag{4.5.4}$$

where K_1 and σ_1 are given by

$$K_1 = -1.01\left(\frac{R_T + C_T + 1}{R_T + C_T + \frac{\pi}{4}}\right) \tag{4.5.5}$$

$$\sigma_1 = \frac{1.04}{R_T C_T + R_T + C_T + \left(\frac{2}{\pi}\right)^2} \tag{4.5.6}$$

with $R_T = R_{S1}/R = R_{S2}/R$ and $C_T = C_{L1}/C = C_{L2}/C$. The relative errors of these coefficients are less than 3% for K_1 and less than 4% for σ_1 for any values of R_T and C_T. It should be noted that the exact value of K_1 is $\frac{4}{\pi}$ andvat of σ_1 is $\left(\frac{\pi}{2}\right)^2$ for $R_T = C_T = 0$. When $R_T = C_T >> 1$, the exact value of K_1 is –1 and that of σ_1 is $1/\{(R_T + 1)(C_T + 1)\}$. Both these asymptotic values are correctly produced by the expressions (4.5.5) and (4.5.6).

It is clear from expressions (4.5.3) and (4.5.4) that if $V_{S1} = V_{S2}$, i.e., the two lines are driven by in-phase source signals, each line behaves as a distributed *RC* line with a capacitance *C*. On the other hand, if the two lines are driven by out-of-phase source signals, i.e., if $V_{S2} = -V_{S1}$ then each line behaves as a distributed *RC* line with a capacitance equal to $C + 2C_C$.

The peak value of $V_2(\ell, t)$ when $V_{S2} = 0$ is the maximum crosstalk voltage induced at the load end of the second line by the coupling capacitance. It is this value that the designer needs to keep in mind to avoid malfunction of the circuit. It can be determined by differentiating Eqn. (4.5.4) to be

$$V_{2,\,max} = V_{S1}K_1\left(\frac{1}{1+2\eta}\right)^{1/2\eta}\left(\frac{\eta}{1+2\eta}\right) \approx \frac{1}{2}V_{S1}\left(\frac{\eta}{1+\eta}\right) \quad (4.5.7)$$

where

$$\eta = \frac{C_C}{C}$$

The approximation at the right end of Eqn. 4.5.7 holds when $R_T = C_T = 0$ and $\eta \leq 2$.

In a special case when R_{S1} is zero and R_{S2} is finite, the maximum crosstalk voltage is given by

$$V_{2,\,\max} \approx V_{S1}\left(\frac{0.5 + R_{T2}}{1 + R_{T2}}\right)\left(\frac{\eta}{1+\eta}\right)$$

In this case, the crosstalk becomes worse than that predicted from Eqn. (4.5.7).

A comparison between the voltage waveforms obtained by using the compact expression (4.5.7) and that obtained by using SPICE (with each interconnection modeled as a 10-step RC ladder network) shows that the maximum error in the compact expression is less than 3% of VS_1.

Simple expressions for the coupling capacitances between the interconnections can be derived from those given in section 2.4. For a system of two lines on a ground plane, the coupling capacitance C_{12} is given by [27]

$$C_{12} = \varepsilon_{ox}\left[1.82\left(\frac{T}{H}\right)^{1.08} + \left(\frac{W}{H}\right)^{0.32}\right]\left(\frac{S}{H} + 0.43\right)^{-1.38} \quad (4.5.8)$$

while for a system of three interconnections on a ground plane, the coupling capacitances are given by [27]

$$C_{12} = \varepsilon_{ox}\left[1.93\left(\frac{T}{H}\right)^{1.1} + 1.14\left(\frac{W}{H}\right)^{0.31}\right]\left(\frac{S}{H} + 0.51\right)^{-1.45} \quad (4.5.9)$$

Relative errors of these capacitance expressions are less than 15% for the values of (T/H), (W/H), and (S/H) between 0.3 and 3.0.

Distributed RLC Model for Two Coupled Interconnections

Two coupled distributed *RLC* interconnections A (active) and Q (quiet), shown in Figure 4.5.2, are described by the following partial differential equations [22]:

$$\frac{\partial^2}{\partial x^2}V_Q(x,t) = r(c_{gnd} + c_m)\frac{\partial}{\partial t}V_Q(x,t) - rc_m\frac{\partial}{\partial t}V_A(x,t) + (l_s(c + c_m)$$

$$- l_m c_m)\frac{\partial^2}{\partial t^2}V_Q(x,t) + (l_m(c_{gnd} + c_m) - l_s c_m)\frac{\partial^2}{\partial t^2}V_A(x,t) \quad (4.5.10)$$

$$\frac{\partial^2}{\partial x^2}V_A(x,t) = r(c_{gnd} + c_m)\frac{\partial}{\partial t}V_A(x,t) - rc_m\frac{\partial}{\partial t}V_Q(x,t) + (l_s(c_{gnd} + c_m)$$

$$+ (l_s(c_{gnd} + c_m) - l_m c_m)\frac{\partial^2}{\partial t^2}V_A(x,t) - l_s c_m)\frac{\partial^2}{\partial t^2}V_Q(x,t) \quad (4.5.10)$$

where V_A is the transient voltage along the active interconnection, V_Q is the transient voltage along the quiet interconnection, c_{gnd} is the ground capacitance of the interconnection, c_m is the mutual (coupling) capacitance between the interconnections, l_s is the self-inductance of each

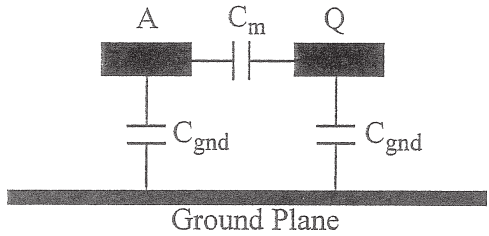

Figure 4.5.2 Two coupled distributed RLC interconnections A (active) and Q (quiet) [from 4.22] (© IEEE 2000)

interconnection, and l_m is the mutual (coupling) inductance between the two interconnections. Both lines A and Q are of finite length l and are open-circuited at the load ends; line A is driven by a voltage source V_S having a source resistance R_S, whereas line Q is not driven by a voltage source though connected to a resistance R_S at $x = 0$. The resulting boundary conditions for current and voltage along the lines A and Q are as follows:

$$V_A(x = 0, t) = V_S(t) - R_S I_A(x = 0, t) \tag{4.5.12}$$

$$V_Q(x = 0, t) = -R_S I_Q(x = 0, t) \tag{4.5.13}$$

$$I_A(x = \ell, t) = 0 \tag{4.5.14}$$

$$I_Q(x = \ell, t) = 0 \tag{4.5.15}$$

Equations (4.5.10) and (4.5.11) can be decoupled in terms of the following voltages V_+ and V_- defined as follows:

$$V_+ = V_A + V_Q$$

$$V_- = V_A - V_Q$$

The resulting set of decoupled partial differential equations is:

$$\frac{\partial^2}{\partial x^2} V_+(x, t) = rc \frac{\partial}{\partial t} V_+(x, t) + (l_s + l_m) c \frac{\partial^2}{\partial t^2} V_+(x, t) \tag{4.5.16}$$

$$\frac{\partial^2}{\partial x^2} V_-(x, t) = r(c + 2c_m) \frac{\partial}{\partial t} V_-(x, t) + (l_s - l_m)(c + 2c_m) \frac{\partial^2}{\partial t^2} V_-(x, t) \tag{4.5.17}$$

The boundary conditions for voltages V_+ and V_- and for currents $I_+ = I_A + I_Q$ and $I_- = I_A - I_Q$ can be derived from equations (4.5.12) to (4.5.15) as follows:

$$V_+(x = 0, t) = V_S(t) - R_S I_+(x = 0, t) \tag{4.5.18}$$

$$V_-(x = 0, t) = V_S(t) - R_S I_-(x = 0, t) \tag{4.5.19}$$

$$I_+(x = \ell, t) = 0 \tag{4.5.20}$$

$$I_-(x = \ell, t) = 0 \tag{4.5.21}$$

Equations (4.5.18) to (4.5.21) indicate that the boundary conditions for (V_+, I_+) and (V_-, I_-) are the same as those for an open-circuited single line driven by a voltage source V_S with an arbitrary resistance R_S.

Equation (4.5.16) suggests that $V_+(x, t)$ is the solution for the voltage along either of the two interconnection lines when both are excited simultaneously. In this case, the mutual capacitance between the lines will be zero and each line will have its ground capacitance only. In this configuration, since the currents in the two lines are in the same direction, the effective inductance of each line will be the sum of its self-inductance and the mutual inductance between the two lines. On the other hand, Eqn. (4.5.17) suggests that $V_-(x, t)$ is the solution for the voltage along the active interconnection line when the adjacent line is switching with the opposite polarity. In this case, the mutual capacitance between the lines will be twice its previous value in addition to each line having its ground capacitance. In this configuration, since the currents in the two lines are equal in magnitude but opposite in direction, the effective inductance of the line will be the difference of its self-inductance and the mutual inductance between the two lines.

The worst-case crosstalk on the quiet line occurs when both the lines are initially uncharged and the active line is connected to the voltage source. In this case, the voltage waveform induced on the quiet line is given by

$$V_Q(\ell, t) = 1/2[V_{fin}(\ell, t, \mathrm{l} = l_s + l_m, c = c_{gnd}) - V_{fin}(\ell, t, l = l_s - l_m, c = c_{gnd} + 2c_m)] \tag{4.5.22}$$

In Eqn. (4.5.22), $V_{fin}(x, t)$ represents the voltage waveform along a single interconnection line derived earlier in chapter 3. It is given by

$$V_{fin}(\ell, t) = 2V_{inf}(\mathrm{x} = \ell, t, m = 0)$$

$$+ 2e^{-\left(\frac{r}{2l}\right)t} \sum_{n=1}^{q} \sum_{i=0}^{n} \sum_{j=0}^{\infty} (-1)^i \Gamma^{(n-i+j)} \frac{n(n-1+j)!}{i!j!(n-i)!}$$

$$\times V_{inf}(x = (2n+1)\ \ell, t, m = i + j) \tag{4.5.23}$$

where $V_{inf}(x, t, m)$ denotes the voltage waveform along the semi-infinite line given by

$$V_{inf}(x, t, m) = V_S\left(\left(\frac{Z_o}{Z_o + R_S}\right)\left(\frac{t - x\sqrt{lc}}{t + x\sqrt{lc}}\right)^{m/2} e^{-\left(\frac{r}{2l}\right)t} I_0\left(\frac{r}{2l}\sqrt{t^2 - (x\sqrt{lc})^2}\right)\right.$$

$$+ \frac{1}{2}\sum_{k=1}^{\infty}\left(\frac{t - x\sqrt{lc}}{t + x\sqrt{lc}}\right)^{(k+m)/2} e^{-\left(\frac{r}{2l}\right)t} (4 - (1+\Gamma)^2\Gamma^{k-1}) I_{(k+m)}$$

$$\left.\left(\frac{r}{2l}\sqrt{t^2 - (x\sqrt{lc})^2}\right)\right) u(t - x\sqrt{lc}) \tag{4.5.24}$$

Distributed RLC Model for Three Coupled Interconnections

Three parallel coupled interconnections, each driven by a voltage source V_S having an internal source resistance R_S, sandwiched between two virtual ground planes, as shown in Figure 4.5.3, can be described by the partial differential equations as below [22]:

$$\frac{\partial^2}{\partial x^2}\begin{bmatrix} V_1(x,t) \\ V_2(x,t) \\ V_3(x,t) \end{bmatrix} = r\begin{bmatrix} C_{gnd} + c_m + c_{13} & -c_m & -c_{13} \\ -c_m & C_{gnd} + 2c_m & -c_m \\ -c_{13} & -c_m & C_{gnd} + c_m + c_{13} \end{bmatrix}\frac{\partial}{\partial t}\begin{bmatrix} V_1(x,t) \\ V_2(x,t) \\ V_3(x,t) \end{bmatrix} +$$

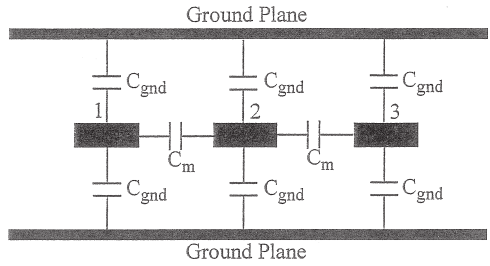

Figure 4.5.3 Three parallel coupled interconnections, each driven by a voltage source V_S having an internal source resistance R_S, sandwiched between two virtual ground planes [from 4.22](© IEEE 2000)

$$\begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{12} & l_{22} & l_{23} \\ l_{13} & l_{23} & l_{33} \end{bmatrix} \begin{bmatrix} C_{gnd}+c_m+c_{13} & -c_m & -c_{13} \\ -c_m & C_{gnd}+2c_m & -c_m \\ -c_{13} & -c_m & C_{gnd}+c_m+c_{13} \end{bmatrix} \frac{\partial}{\partial t^2} \begin{bmatrix} V_1(x,t) \\ V_2(x,t) \\ V_3(x,t) \end{bmatrix} \tag{4.5.25}$$

The inductance and capacitance matrices are connected by the following relationship:

$$\begin{bmatrix} l_{11} & l_{12} & l_{13} \\ l_{12} & l_{22} & l_{23} \\ l_{13} & l_{23} & l_{33} \end{bmatrix} \begin{bmatrix} C_{gnd}+c_m+c_{13} & -c_m & -c_{13} \\ -c_m & C_{gnd}+2c_m & -c_m \\ -c_{13} & -c_m & C_{gnd}+c_m+c_{13} \end{bmatrix} = \frac{1}{v^2} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{4.5.26}$$

where v is the speed of propagation of an electromagnetic wave in the dielectric medium where the interconnections are placed. From the symmetry of the interconnections, we will assume that the voltage waveforms on the outer interconnections 1 and 3 are the same and called them $Vo(x, t)$. For this reason, the coupling capacitance c_{13} can be taken as effectively zero. On the same lines, we will represent the voltage waveform of the inner interconnection 2 as $V_i(x, t)$. Then the matrix Eqn. (4.5.25) can be

expressed as the following two coupled partial differential equations after setting $c_{13} = 0$:

$$\frac{\partial^2}{\partial x^2}V_o(x,t) = r(c_{gnd}+c_m)\frac{\partial}{\partial t}V_o(x,t) - rc_m\frac{\partial}{\partial t}V_i(x,t) + \frac{1}{v^2}\frac{\partial^2}{\partial t^2}V_o(x,t) \tag{4.5.27}$$

$$\frac{\partial^2}{\partial x^2}V_i(x,t) = -2rc_m\frac{\partial}{\partial t}V_o(x,t) - r(c_{gnd}+2c_m)\frac{\partial}{\partial t}V_i(x,t) + \frac{1}{v^2}\frac{\partial^2}{\partial t^2}V_i(x,t) \tag{4.5.28}$$

Equations (4.5.27) and (4.5.28) can be decoupled in terms of the voltages V_{sum} and V_{diff} defined as

$$V_{\text{sum}} = 2V_o + V_i \tag{4.5.29}$$

$$V_{\text{diff}} = V_o - V_i \tag{4.5.30}$$

The resulting equations are:

$$\frac{\partial^2}{\partial x^2}V_{\text{sum}}(x,t) = rc_{gnd}\frac{\partial}{\partial t}V_{\text{sum}}(x,t) + \frac{1}{v^2}\frac{\partial^2}{\partial t^2}V_{\text{sum}}(x,t) \tag{4.5.31}$$

$$\frac{\partial^2}{\partial x^2}V_{\text{diff}}(x,t) = r(c_{gnd}+3c_m)\frac{\partial}{\partial t}V_{\text{diff}}(x,t) + \frac{1}{v^2}\frac{\partial^2}{\partial t^2}V_{\text{diff}}(x,t) \tag{4.5.32}$$

The boundary conditions for (V_{sum}, I_{sum}) and (V_{diff}, I_{diff}) can be found from those for the inner and outer interconnections to be

$$V_{\text{sum}}(x=0) = 2V_S(t) - R_S\, I_{\text{sum}}(x=0) \tag{4.5.33}$$

$$V_{\text{diff}}(x=0) = V_S(t) - RS\, I_{\text{diff}}(x=0) \tag{4.5.34}$$

$$I_{\text{sum}}(x=\ell) = 0 \tag{4.5.35}$$

$$I_{\text{diff}}(x=\ell) = 0 \tag{4.5.36}$$

According to equations (4.5.31) and (4.5.32), the voltage waveforms for $V_{sum}(x, t)$ and $V_{diff}(x, t)$ are the solutions for a single finite line though with different capacitance and inductance values. These can be used to find the voltage waveforms for the worst-case time delay and crosstalk scenarios.

The worst-case crosstalk on the inner interconnection occurs when all three lines are initially uncharged and the two outer interconnections are made simultaneously active by turning on their sources. The resulting load voltage waveform for the inner (quiet) interconnection is then given by

$$V_Q(\ell, t) = \frac{2}{3}\left\{ V_{fin}\left(\ell, t, l=\frac{1}{2c_{gnd}v^2}, c=2c_{gnd}\right) - V_{fin}\left(\ell, t, l=\frac{1}{(2c_{gnd}+3c_m)v^2}, c=2c_{gnd}+3c_m\right)\right\} \quad (4.5.37)$$

In Eqn. (4.5.37), $V_{fin}(x, t)$ represents the voltage waveform along a single interconnection line derived earlier in chapter 3. It is given by

$$V_{fin}(\ell, t) = 2V_{inf}(x = \ell, t, m = 0) + 2e^{-\left(\frac{r}{2l}\right)t} \sum_{n=1}^{q}\sum_{i=0}^{n}\sum_{j=0}^{\infty} (-1)^i \Gamma^{(n-i+j)} \frac{n(n-1+j)!}{i!j!(n-i)!} \times V_{inf}(x = (2n+1)\ell, t, m = i+j) \quad (4.5.38)$$

where $V_{inf}(x, t, m)$ denotes the voltage waveform along the semi-infinite line given by

$$V_{inf}(x, t, m) = V_S\left(\left(\frac{Z_o}{Z_o+R_S}\right)\left(\frac{t-x\sqrt{lc}}{t+x\sqrt{lc}}\right)^{m/2} e^{-\left(\frac{r}{2l}\right)t} I_0\left(\frac{r}{2l}\sqrt{t^2-(x\sqrt{lc})^2}\right) + \frac{1}{2}\sum_{k=1}^{\infty}\left(\frac{t-x\sqrt{lc}}{t+x\sqrt{lc}}\right)^{(k+m)/2} e^{-\left(\frac{r}{2l}\right)t} (4-(1+\Gamma)^2\Gamma^{k-1}) I_{(k+m)} \left(\frac{r}{2l}\sqrt{t^2-(x\sqrt{lc})^2}\right)\right) u(t-x\sqrt{lc}) \quad (4.5.39)$$

Comparisons of the normalized load voltages obtained by the compact expressions for the distributed *RLC* interconnection model with those obtained by HSPICE with 1, 10, 50, and 500 lumped *RLC* elements are shown in Figure 4.5.4 [22]. For these comparisons, the interconnection metal is assumed to be copper surrounded by a low-k dielectric. The various interconnection parameters are as follows:

Interconnection length = 3.6 cm
Interconnection cross-section = 2.1 μm by 2.1 μm
Resistance per unit length = 37.86 Ω/cm
Driving source resistance = 133.3 Ω
Lossless characteristic impedance, $Z_0^+ = 266.32\ \Omega$
Lossless characteristic impedance, $Z_0^- = 88.77\ \Omega$

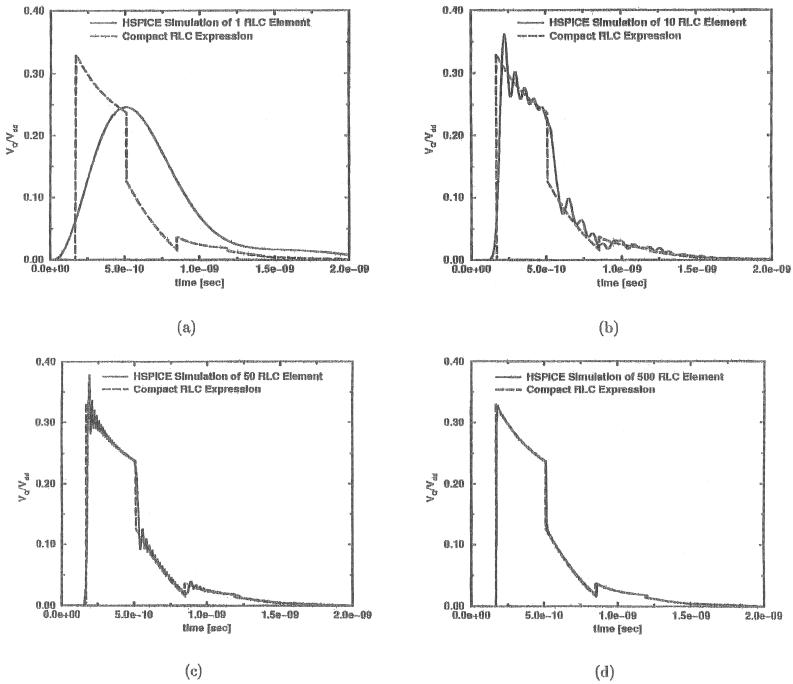

Figure 4.5.4 Comparisons of the normalized load voltages obtained by the compact expressions for the distributed rlc interconnection model with those obtained by HSPICE with 1, 10, 50 and 500 lumped RLC elements. [4.22] (© IEEE 2000)

Figure 4.5.4 shows that the HPICE waveforms approach the compact expression waveform as the number of *RLC* elements is increased in the HSPICE simulation. For the typical values of the interconnection and driving source parameters chosen in these comparisons, there is virtually complete agreement between the two waveforms for 500 or more *RLC* elements lending excellent support to the compact expressions.

Exercise 4.4

A few methods of reducing crosstalk are discussed in this chapter. Can you think of other methods? Discuss the merits and drawbacks of each method that you propose.

Exercise 4.5

List and discuss the desirable characteristics of a numerical model that make it more suitable for inclusion in a computer aided design (CAD) tool. Review the various techniques presented in this chapter from the point of view of their suitability for inclusion in a CAD tool.

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CHAPTER 5

Modeling of Electromigration-Induced Interconnection Failure

The term "electromigration" refers to mass transport in metals under high stress conditions, especially under high current densities and high temperatures. This phenomenon has been studied at length during the last several years and presents a key problem in integrated circuits since it causes open-circuit and short-circuit failures of the interconnections [1–179]. Nowadays, there is a trend to fabricate very-large-scale integration (VLSI) circuits on small chip areas to save space and to reduce propagation delays. According to the scaling theory for both bipolar and FET circuits, if the chip area is decreased by a factor k, the current density increases by at least the same factor in both cases, and this becomes one of the primary reasons for the interconnection failure due to electromigration. Here are the chapter objectives:

- After going through section 5.1, students should be familiar with the several factors responsible for electromigration in the interconnection metallizations.
- After going through section 5.2, students should be familiar with the problems caused by electromigration in the interconnection metallizations.
- After going through section 5.3, students should be familiar with the various methods of reducing electromigration in the interconnection metallizations.

- After going through section 5.4, students should be familiar with the techniques of measuring electromigration in the interconnection metallizations.
- After going through section 5.5, students should be able to model electromigration in the copper interconnections under DC and AC conditions.
- After going through section 5.6, students should be familiar with the various existing models of integrated circuit reliability.
- After going through section 5.7, students should be able to model electromigration in a metallic interconnection due to repetitive current pulses.
- After going through section 5.8, students should be familiar with the various guidelines that have been proposed for testing electromigration in an interconnection line.

5.1 Electromigration Factors and Mechanism

A lot of research has been carried out to study the electromigration pattern as well as the factors that affect electromigration [1–64, 72–135]. Some of the several known factors that induce electromigration can be classified as follows:

Current Density

Current density is the key factor that contributes to the frictional forces as well as to the flux divergence. At a high current density, the momentum exchange between the current carriers and the metallic ions becomes significantly large resulting in a very large frictional force and flux divergence along the metallization lines, resulting in mass transport that leads to the line failure. It is obvious from Table 5.1.1 that the me time to failure (MTF) decreases as the current density increases. This result has been verified by plenty of research work [1–61, 72–103, 116, 117].

Thermal Effects

Thermal gradients and the line temperature are two other important factors that cause electromigration. It has been reported that the

Table 5.1.1 Dependence of the mean time to failure on the current density for three kinds of aluminum film conductors having a cross-sectional area of 10^{-7} cm^2 and at a temperature of 160°C (Derived from the data in reference [83])

		Mean Time to Failure (h)	
Current Density (MA/cm^2)	**Small Crystallite**	**Large Crystallite**	**Glassed Large Crystallite**
0.1	15,500	120,000	—
0.2	4,000	30,000	—
0.4	960	7,800	65,000
0.6	450	3,300	29,000
0.8	250	1,900	15,000
1.0	155	1,250	11,000
2.0	40	300	2,700
4.0	10	75	700
6.0	—	33	370
8.0	—	18	—

electromigration process occurs in the direction from high temperature to low temperature and that thermal gradients are very important in the electromigration process because these can induce a thermal force that enhance further mass transport in the metallization lines [33, 94, 118, 119]. Thermal gradients are dependent on the metallization structure as well as on the processing techniques.

Line temperature is also an important factor in the electromigration process [12, 14, 120–124]. According to Eqn. (5.1.9), the MTF decreases with the increase in the line temperature. This conclusion can also be drawn from Table 5.1.2. In general, if the VLSI system is operating at room temperature under normal conditions, thermal effects can be considered insignificant.

Line Length and Line Width

Table 5.1.3 shows the relationship between the MTF and the line length. As mentioned earlier, voids, hillocks, and whiskers are formed along the interconnection line during electromigration creating a stress-related force that enhances further electromigration. The magnitude of this force is proportional to the concentration gradient. If the lines are long,

Table 5.1.2 Dependence of the mean time to failure on temperature for three kinds of aluminum film conductors having a cross-sectional area of 10^{-7} cm^2 and carrying current density of 1 MA/cm^2 (Derived from the data in reference [83])

	Mean Time to Failure (h)		
Temperature (°C)	Small Crystallite	Large Crystallite	Glassed Large Crystallite
40	23,000	—	—
60	7,700	—	—
80	3,000	—	—
100	1,280	47,000	—
120	580	12,500	—
140	300	3,800	50,000
160	155	1,250	11,000
180	90	450	2,800
200	52	180	800
220	32	80	255
240	21	37	90
260	14	18	34

Table 5.1.3 Dependence of the median time to failure on the length of the interconnection line with a width of 2 μm and a median grain size of 1.25 μm (Derived from the data in reference [93])

Length (μm)	Median Time to Failure (h)
10	530
20	380
30	325
40	315

the concentration gradient will be much larger, resulting in shorter electromigration lifetime as compared to the shorter lines [125].

A lot of work has been done to study the effects of line width on the electromigration lifetime as well [126–129]. It has been found that the electromigration lifetime is inversely proportional to the line width. This is because, for small line widths, the cross-sectional area will also be small, resulting in higher current density that may degrade the electromigration lifetime. The experimental data on this relationship is shown in Table 5.1.4.

Table 5.1.4 Dependence of the median time to failure on the width of the interconnection line with a length of 25 μm and a median grain size of 0.75 μm (Derived from the data in reference [93])

Width (μm)	Median Time to Failure (h)
0.5	165
1.0	220
1.5	270
2.0	305
2.5	335

Activation Energy and Material Structure

Activation energy of a metallization line depends on its material structure and, therefore, different metallization lines may have different values of activation energies. For VLSI interconnections, metallizations having high activation energy are desirable because they lead to enhanced stability. Material structure also affects the electromigration lifetime in many ways. Known aspects include grain orientation, grain size, and grain boundaries. Reports have shown that electromigration is related to structural inhomogeneity [33, 35, 36, 124]. An ideal metallization line is the one with uniform grain size and regular grain orientation. Unfortunately, this is not possible and there is always some degree of inhomogeneity that induces flux divergence [131, 134, 135]. As the metallization line becomes more inhomogenous in structure, this flux becomes more divergent resulting in smaller MTF. Based on the previous studies, it is known that electromigration is confined mainly in the grain boundaries [6, 33, 35, 79, 84]. Smaller grain size means that more grain boundaries are available for electromigration. Table 5.1.5 shows the experimental relationship between grain size and MTF. The fact that smaller grain size degrades the electromigration lifetime has been verified by many researchers [39, 79, 93]. If the grain size is large enough to be comparable to the stripe width, then the single grain can act as a barrier to the migrating atoms [35, 130, 133, 135].

The Electromigration Mechanism

In general, a metallization line consists of an aggregate of metallic ions. These ions are held together by a binding force and opposed by a repulsive

Table 5.1.5 Dependence of the median time to failure on the median grain size for an interconnection line with a width of 1 μm and a length of 20 μm (Derived from the data in reference [93])

Median Grain Size (μm)	Median Time to Failure (h)
1.0	245
1.5	330
2.0	405
2.5	460
3.0	515

electrostatic force. At any given temperature, some of these ions may have sufficient energy to escape from the potential well that binds them in the lattice. When they reach the saddle point of the potential well, they are free from the lattice and become "activated." The energy needed to achieve this is known as the "activation energy." Since a metallization line also contains a certain concentration of vacancies, these ions can diffuse out of the lattice into an adjacent vacancy. This process is known as "self-diffusion." In the absence of an electric current, the self-diffusion process is more or less isentropic, i.e., the probability for each nearest ion around the vacancy to exchange with the vacancy is equal. Under no concentration gradient or chemical potential [104, 105], a random rearrangement of individual ions takes place resulting in no mass transportation. Once the current is applied, the situation changes. Now, there are two external forces exerted on the metallization, namely the frictional force and the electrostatic force. The frictional force is due to the momentum exchange with the crystal and its magnitude is proportional to the current density. The electrostatic force is due to the interactions between the electric fields created by the electrons and the positively charged metallic ions. The electric field due to the electrons will attract the positively charged metallic ions toward the cathode against the electron wind and its magnitude, denoted by E, and is given by

$$E = \rho J \tag{5.1.1}$$

where

ρ = Density of ions, and
J = Current density

Because of the presence of the "shielding electrons," the frictional force is always greater than the electrostatic force.

Consider a metal strip as shown in Figure 5.1.1. The frictional force and the electrostatic force are denoted by **F1** and **F2**, respectively. The frictional force is acting in the direction of the current flow and the electrostatic force is acting against the current flow. The electric field **E** also acts against the current flow. Since **F1** is much greater than **F2**, the net force, denoted by **F**, will be in the direction of the current flow. Defining the direction of the net force being positive, we have

$$\mathbf{F} = \mathbf{F}_1 - \mathbf{F}_2 = (\mathbf{Z}^*\mathbf{e})\,\mathbf{E} \tag{5.1.2}$$

where (Z^*e) is the effective charge assigned to the migrated ion with Z^* given by [22]

$$Z^* = Z\left(\frac{\rho_d\, N\, m}{2\rho\, N_d\, m} - 1\right) \tag{5.1.3}$$

where

Z = Electron-to-atom ratio
ρ_d = Defect resistivity
N_d = Density of defects
ρ = Resistivity of metal
N = Density of metal
m^* = Effective electron mass, and
m = Free electron mass

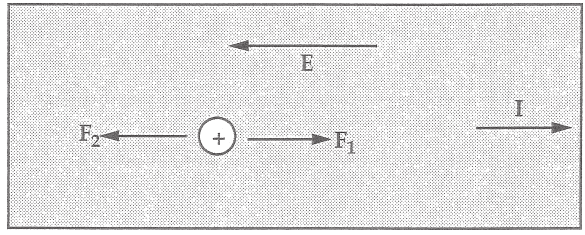

Figure 5.1.1 Frictional and electrostatic forces (F_1 and F_2, respectively) inside a current carrying metal strip.

The first and the second terms in Eqn. (5.1.3) correspond to the forces $\mathbf{F_1}$ and $\mathbf{F_2}$, respectively. According to the Nernst-Einstein equation, the average drift velocity v is given by

$$v = \mu F \tag{5.1.4}$$

where

μ = Mobility = D/fkT
D = Self-diffusion coefficient = $D_0 \exp(-E_a/kT)$
f = Correlation factor depending on the lattice structure;
In most cases, $f = 1$
k = Boltzmann's constant
E_a = Activation energy, and
T = Absolute temperature

The induced flux due to the creation of this frictional force is now given by [94]

$$\psi_A = N\mathrm{v} \tag{5.1.5}$$

Combining equations (5.1.1), (5.1.2), (5.1.4), and (5.1.5), we get

$$\psi_A = \frac{ND\rho J}{fkT}\,(Z^*\mathrm{e}) \tag{5.1.6}$$

or

$$\psi_A = \left(\frac{ND_0\rho J}{fkT}\right) \quad (\mathrm{Z}^*\mathrm{e}) \quad exp\left(-\frac{E_a}{kT}\right) \tag{5.1.7}$$

In general, ψ_A may not be the same throughout the metallization because of structural inhomogeneities. Such a divergence of flux in the metallization is more likely to occur under high current density conditions. If the divergence becomes significant, the original isentropic self-diffusion is perturbed and the ions moving along the current flow have a higher probability of exchanging positions with the vacancies. As a result, the original random process changes to a directional process in which the metallic ions move opposite to the electron wind direction while the vacancies move in the opposite direction. The metallic ions condense to

form whiskers, whereas the vacancies condense to form voids [105–108]. This process results in the change in the density of the metal ions with respect to time. The rate of this change, $\frac{dN}{dt}$, can be expressed as [33]

$$\frac{dN}{dt} = -V \operatorname{div}(\psi_A) \tag{5.1.8}$$

where V = Volume and

$$\operatorname{div}(\psi_A) = \frac{d\psi_A}{dx} + \frac{d\psi_A}{dy} + \frac{d\psi_A}{dz}$$

The formation of voids causes some of the metallization lines to fail forcing the current to go through the rest of the lines, resulting in an increase in the current density and the joule heat. This production of joule heat can increase the local temperature and cause more lines to fail [91]. Furthermore, as the whiskers and hillocks form, a concentration gradient is produced which may create a stress-related force enhancing the mass transport process and causing more lines to fail [109–111]. All these processes continue as a loop, as shown in Figure 5.1.2, until the circuit fails to work. The *MTF*, or t_{50}, is defined as the time taken for 50% of the lines to fail and is given by

$$MTF = A J^{-n} exp\left(\frac{E_a}{kT}\right) \tag{5.1.9}$$

where

E_a = Activation energy
J = Current density
T = Temperature in degrees Kelvin
A = Constant depending on geometry and material properties
k = Boltzmann's constant
n = Constant ranging from 1 to 7

The value of n is stated last because of its variance found in different reference texts and research works [112]. Some of the n values reported in different works are listed in Table 5.1.6. The deviation of n values has been explained as due to the overestimation of joule heating, resulting in low values of n and the underestimation of joule heating, resulting in an apparent very large current density dependence and hence high values of n. In general, the correct value of n should lie between 1 and 2 [124].

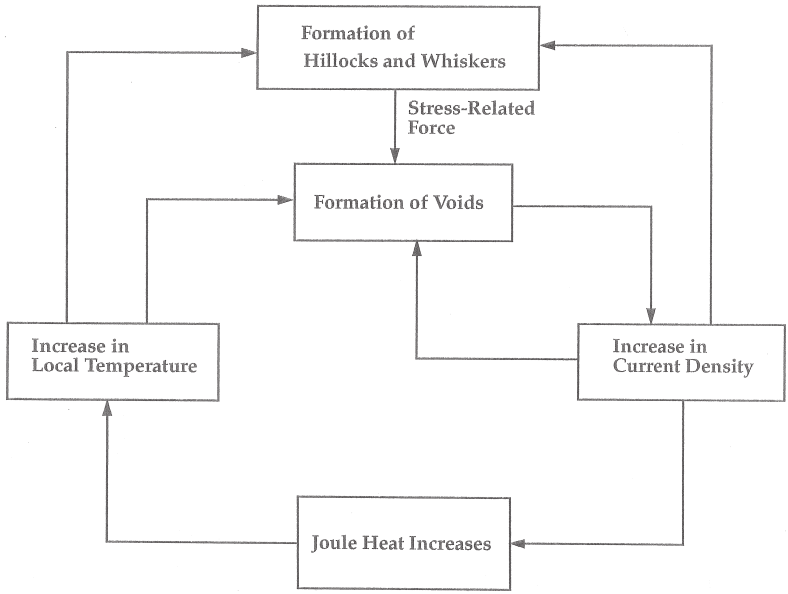

***Figure 5.1.2** Schematic diagram of the various factors that contribute to electromigration in the VLSI interconnection metallizations (modified from [591]).*

***Table 5.1.6** Values of the exponent n found in the literature*

Source [Reference]	Current Density	n
Huntington and Grone [21]	<0.5 MA/cm^2	1
Attardo [114]	0.5–1 MA/cm^2	1.5
Black [83]	0.45–2.88 MA/cm^2	2
Blair et al. [54]	1–2 MA/cm^2	6–7
Chabra and Ainslie [85]	—	1–3
Venable and Lye [90]	—	1
Sigsbee [88, 89]	$\approx$1 MA/cm^2	1
Vaidya et al. [62]	—	2
Danso and Tullos [51]	0.168–0.704 MA/cm^2	1.7
Chern et al. [41]	—	2.5 ± 0.5

If the cross-sectional area A is also taken into account [83], then Eqn. (5.1.9) is modified as

$$MTF = A\,J^{-n}\,exp\left(\frac{E_a}{kT}\right) \tag{5.1.10}$$

It is also interesting to study the speed of the metallic ions and its relationship to MTF. According to Gimpelson [115], the migration velocity v_m can be expressed as

$$v_m = G J \exp\left(-\frac{E_a}{kT}\right) \tag{5.1.11}$$

where G is a proportionality constant. Combining equations (5.1.10) and (5.1.11), MTF can be expressed as

$$\text{MTF} = \text{G}_n \frac{A}{(v_m)^n} \exp\left(-\frac{(n-1)E_a}{kT}\right) \tag{5.1.12}$$

5.2 Problems Caused by Electromigration

As mentioned earlier, smaller chip areas are desirable because device miniaturization has become a continuing trend in VLSI. To obtain a better understanding of the problems associated with electromigration, dimensional scaling and its effects on current density should be considered. Since different devices have different operational principles, scaling theories and problems may differ. For example, when the dimension of an Field effect transistor FET device is reduced by a factor k, so does the time delay per circuit while the power dissipation remains constant and the current density increases by a factor k. In bipolar devices, the scaling structure is nonlinear. Therefore, it is difficult to get a generalized picture of how scaling affects the current density. The basic scaling theories for both the FET and the bipolar devices are summarized in Table 5.2.1. Despite this problem, it is possible to classify the problems caused by electromigration into two categories, namely the geometry-related problems and the material-related problems [65–71].

Geometry-Related Problems

Geometry-related problems arise as a result of the reduction of the interconnection dimensions to a micron or a submicron range. In metal films, with grain size about the same or even larger than the film thickness, the flux generated is confined mainly along the grain boundaries.

Table 5.2.1 Scaling of device parameters

Device Parameters	FET [69]	Bipolar [70]
Device dimension	$1/k$	$1/k$
Voltage	$1/k$	~1
Current	$1/k$	$1/k$
Delay time/circuit	$1/k$	$1/k$
Power density	1	~k
Line resistance	k	k
Line current density	k	~k^2

As a consequence, the small number of grains across the line increases the importance of each individual inhomogenous site of the grain structure and its effect on the overall mass flow pattern. That makes each individual divergent site potentially more damaging since a line can fail without requiring a statistical linkage of several divergent sites. Another problem concerns the device contacts and step coverages. As the dimensions of device contacts decrease, they become comparable to those of the interconnection lines, thus subjecting them to about the same amount of current densities as the conductor lines. In some cases, the stress generated by the abrupt structural variations in contacts and steps can play an important role in causing their failure.

Material-Related Problems

Material-related problems are basically caused by the high current densities. Three associated problems in electromigration are referred to as joule heating, current crowding, and material reactions.

Joule Heating: As the chip size decreases, heat distribution becomes a serious problem. This is especially true in the case of bipolar VLSI because the power density increases by a factor k when the dimensions decrease by the same factor based on constant voltage assumption. For a metal wire that can afford a certain current density rate of about 10^5 A/m^2–s before melting, joule heat generated by current density in the interconnection line exceeding half of this limit must be completely removed through the substrate and/or some passivation layer. Cooling rate has to be faster than the heating rate due to the current density to avoid overheating the

line. Therefore, at high current density, say, above 10^6 A/cm^2, any imperfection of the substrate may result in thermal runaway and destroy the line because of inadequate space for heat dissipation. This also results in raising the strip temperature which accelerates the diffusion process, thus reducing the MTF.

Current Crowding: Current crowding refers to uneven distribution of currents along the metallization lines. It occurs especially in metallizations with structural inhomogeneities. It can alter the local electromigration driving force, thus affecting the mass transport pattern. It can also cause the atoms in the metallization lines to migrate with different velocities, resulting in the formation of voids that cause open-circuit failure.

Material Reactions: Material reactions are part of the effects caused by electromigration. As significant mass accumulation and depletion occur, the amount of mass transport is significant enough to generate enough stress to induce extrusion in the passive layer. It can also change the electrical properties of the junction contacts [71]. Furthermore, the joule heat can suppress or promote any unwanted interfacial material reactions. These problems can alter the device and interconnection characteristics and degrade the VLSI reliability [68].

5.3 Reduction of Electromigration

A lot of effort has been put in order to achieve the reduction of electromigration in the VLSI interconnections [152–170]. The most common solutions can be summarized as follows:

Substrate Overcoating

The basic reason for overcoating the substrate is to prevent the formation of vacancies needed for diffusion and to presumably fill up the broken bonds on the surface of the metallization [73, 79, 116, 152–159, 170]. This is also called "passivation." With the addition of a passivation layer, the joule heat can be dissipated more easily. In order to form a passivation layer, the substrate is basically sealed hermetically by the overcoating layer. The materials mostly used are oxides like SiO and anodic oxides as well as dielectric layers like Al_2O_3-SiO_2 and P_2O_5-SiO_2. This technique

has proven to be effective in improving electromigration lifetimes [12, 87]. It has been further shown that the increase in thickness of these layers increases the electromigration lifetime as long as the thickness does not exceed 6,000 A° [154, 160–162].

Alloying of Metallization

The addition of correct type and concentration of alloys has also been shown to improve the electromigration lifetime [163, 164, 166, 170]. For example, it has been shown that the addition of Ti-Si to Al increases the electromigration lifetime by more than an order of magnitude, whereas the addition of Cr-Si does not show any noticeable improvement [47]. Other reports have shown that the addition of 0.4% Cu to Al with or without the addition of Si results in better electromigration lifetimes than pure Al [38, 156, 158, 159]. The reason for this is that by adding the proper concentration of correct impurities into the original metallization line, the structure of the line changes substantially and this results in improvement of the electromigration lifetimes [156–159]. However, one of the major problems is the increase in the resistance after alloying. This has been demonstrated by adding manganese into the aluminum and Al-Cu metallizations [156]. In short, alloying with Cu (typical levels of 0.5%, 1%, 2%, and 4% have been widely used and reported) has been the industry standard for many years. However, Cu is very hard to etch dry for VLSI applications. This has resulted in an interest in Al/Ti and Al/Si/Ti alloys as alternatives.

Encapsulated Multilayer Interconnections

Encapsulation has the effect of preventing the formation of hillocks. It can be done by using refractory metals and a spacer technology. The refractory metal is deposited by biased sputtering and by anisotropic etching of the material. Several layers of the refractory metal are deposited to ensure reliability. Another way to achieve encapsulation is to form a native oxide layer on the interconnection [160]. In order to be effective, the native oxide has to be thick enough compared to the film thickness to ensure the removal of hillocks. This approach has also been shown to improve the electromigration lifetimes [161, 162].

Gold Metallization

It has been shown that a gold-based interconnection system has a much better MTF than the aluminum films [163]. The key reason for this is that gold has a very high activation energy. In particular, at high current densities and high temperature operations, gold interconnections have shown a better performance. In general, gold can be deposited by vacuum evaporation techniques. However, because of its inert nature, adhesion of gold to the insulating layer by chemical bonding is extremely difficult. Therefore, gold has to be used in a multilayer system where more than one layer of metallization is used to adhere to the insulator as well as to gold.

Deposition Techniques

It has been shown that the MTF of a VLSI system has a close relationship with the employed deposition technique [164, 167, 168]. For example, it is found that the MTF is smaller for the sputtered film technique than the e-beam technique [165]. One possible explanation may be that different deposition techniques may change the defect structure of a metallization and that may change the electromigration pattern.

5.4 Measurement of Electromigration

Many methods can be used for testing and measuring electromigration [143–151]. Two techniques used frequently employ resistance measurement and noise measurement though the latter is rather difficult in practice.

Resistance Measurement

In general, when an open-circuit failure occurs, the resistance goes up, whereas when a short-circuit failure occurs, the resistance goes down. Therefore, by measuring the resistance one can check whether electromigration has taken place. The MTF can be determined by finding the time during which the ratio of the change of resistance to the original resistance reaches a certain value. Rodbell and Shatynski used the ratio of 0.5 because this value corresponds to the transition from predominantly

electromigration to predominantly thermomigration [144]. A standard method of evaluation for VLSI interconnections using this approach is called "accelerated testing" in which high current density and high temperature are applied to the metallization lines [144]. The technique results in the reduction of the complicated testing work and it is widely used in studying electromigration.

Noise Measurement

Metal thin films generate thermal noise and current noise. The noise voltage spectra $S(f)$ is given by

$$S(f) = 4\,\mathrm{kT}R + \frac{k_1 V^{\beta}}{f^{\alpha}} \tag{5.4.1}$$

where

k = Boltzmann's constant
T = Temperature of the film (°K)
R = Resistance of the film (Ω)
$V = IR$ = DC voltage applied across the film
f = Frequency, and
k', α, β = Constants characterizing the current noise spectrum.

The first term corresponds to the thermal noise and the second term corresponds to the current noise. In most cases, the first term is negligible because the current noise dominates. In aluminum films, the current noise is relatively small. Therefore, the measurement of current noise may need special attention. In general, the current noise spectral density of continuous metal thin films at room temperature follows the Hooge's equation.

$$S_c(f) = \frac{\gamma V^{\beta}}{N_c f^{\alpha}} = \frac{\gamma (IR)^{\beta}}{N_c f^{\alpha}} \tag{5.4.2}$$

where N_c is the total number of free charge carriers in the film. For a uniform cross section, N_c is proportional to the volume of the film. Therefore, $S_c(f)$ is detectable only in small films. For nonuniform cross-sections, current density distribution should also be taken into account because the current crowding effect will cause the noise to increase.

Electromigration results in the formation of voids and hillocks and this also leads to a change in the noise level. Using a normal line as a reference denoted by "a" and the line under test denoted by "b," the respective noise voltage spectra can be expressed as

$$S_a(f) = K_a \frac{(IR_a)^\beta}{f^\alpha} \tag{5.4.3}$$

and

$$S_b(f) = K_b \frac{(IR_b)^\beta}{f^\alpha} \tag{5.4.4}$$

Therefore, the ratio $S_b(f)/S_a(f)$ becomes

$$\frac{S_b(f)}{S_a(f)} = \left[\frac{K_b}{K_a}\right]\left[\frac{R_b}{R_a}\right]^\beta \tag{5.4.5}$$

If this ratio is much larger or smaller than 1, then that implies that the electromigration may take place [151].

5.5 Electromigration in the Copper Interconnections

Because of its lower resistivity and potentially superior electromigration properties, copper has emerged as an alternative to aluminum or aluminum-based alloy interconnections particularly for the submicron integrated circuit technologies. Electromigration characteristics of copper interconnections with minimum interlayer barrier metal thickness have been studied by Tao et al. [174]. They have also compared the performance of copper interconnections with those made with Al-4%Cu/TiW and Al-2%Si under DC, high-frequency pulse-DC, and low-frequency bipolar current stressing conditions.

Electromigration Under DC Conditions

Figure 5.5.1 shows the Arrhenius plots of the MTF of interconnections made from electroless plated Cu, Al-2%Si, and Al-4%Cu/TiW vs. 1,000/T under a DC current density of 1.5×10^7 A/cm^2. This figure shows that the MTF for the electroless-plated Cu interconnections is about one

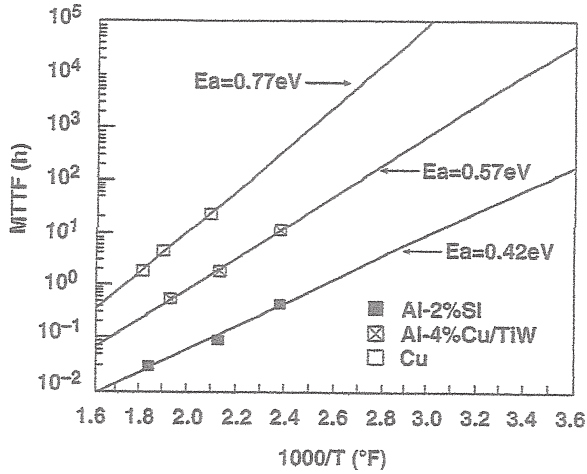

Figure 5.5.1 Arrhenius plots of MTF versus 1,000/T for Cu, Al-4%Cu/TiW, and Al-2%Si interconnections under a DC current of density = 1.5×10^7 A/cm^2 [5.174] (© IEEE 1993)

and two orders of magnitude longer than those for Al-4%Cu/TiW and Al-2%Si interconnections, respectively. Activation energies of these materials can be derived from the slopes of the Arrhenius plots. These can be determined to be 0.77 eV for electroless-plated Cu, 0.42 eV for Al-2%Si, and 0.57 eV for Al-4%Cu/TiW. Using these activation energies, it can be extrapolated that at 75°C, the Cu interconnection lifetimes are about three and five orders of magnitude higher than those of Al-4%Cu/TiW and Al-2%Si interconnections, respectively.

Electromigration Under Pulsed DC Conditions

Figure 5.5.2 shows the dependences of the MTF for Cu, Al-2%Si, and Al-4%Cu/TiW interconnections on the frequency of the pulsed DC current with a peak current density of 1.5×10^7 A/cm^2 at 275°C. This figure shows that the MTF for the Cu interconnections is about one and two orders of magnitude longer than those for the Al-4%Cu/TiW and Al-2%Si interconnections, respectively, for all frequencies. MTF values predicted by the vacancy relaxation model [175] are also included in this figure and are shown by solid lines. Defect relaxation time τ is a fitting parameter in

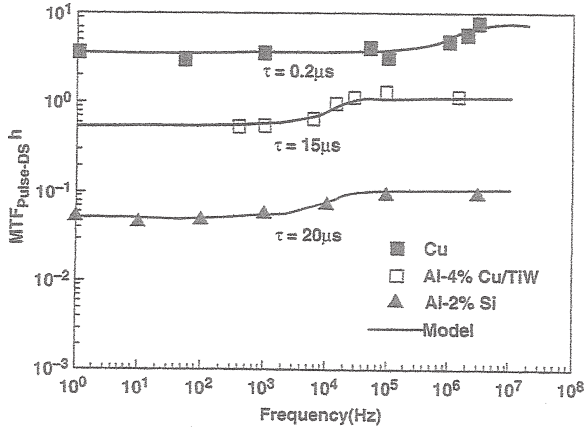

Figure 5.5.2 Dependences of MTF on frequency for Cu, Al-4%Cu/TiW and Al-2%Si interconnections under a pulsed DC current with a peak current density = 1.5×10^7 A/cm^2 at 275°C. [5. 174] (© IEEE 1993)

this model and its value can be found to be about 0.2 μ*s* for Cu interconnections, about 15 μ*s* for the Al-4%Cu/TiW interconnections, and about 20 μ*s* for the Al-2%Si interconnections [174].

Electromigration Under Bipolar AC Conditions

A comparison of the change in resistance of the Cu interconnections under a DC current density of 1.5×10^7 A/cm^2 with that under a 1 MHz bipolar symmetrical rectangular current waveform with $\pm 1.5 \times 10^7$ A/cm^2 current density at 275°C is shown in Figure 5.5.3 [174]. This figure shows that under DC conditions, the interconnection shows an open-circuit failure after about 3.4 hours, whereas no failure is detected under AC conditions for even up to about 350 hours. Similar results indicating no failure under AC conditions have also been shown for the Al-2%Si and Al-4%Cu/TiW interconnections. This has been attributed to the healing effects of electromigration-induced damage under the two opposite halves of the AC current cycle. This assertion has been further verified under low frequency AC current conditions. The change in resistance vs. time for Cu interconnections under a

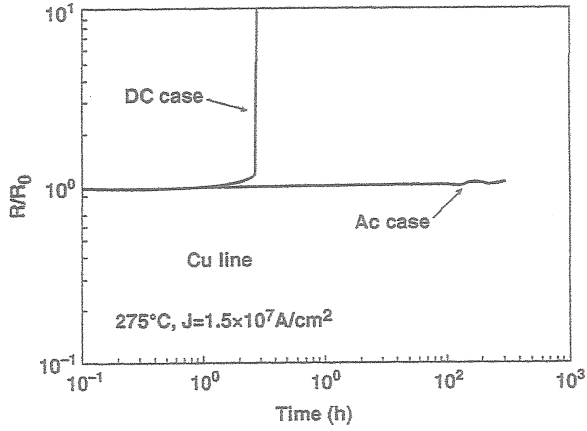

Figure 5.5.3 Normalized resistance for Cu interconnections versus time under a DC current density of 1.5×10^7 A/cm^2 and under a 1 MHz bipolar current of peak current density = 1.5 × 107 A/cm^2 at 275°C. [5.174] (© IEEE 1993)

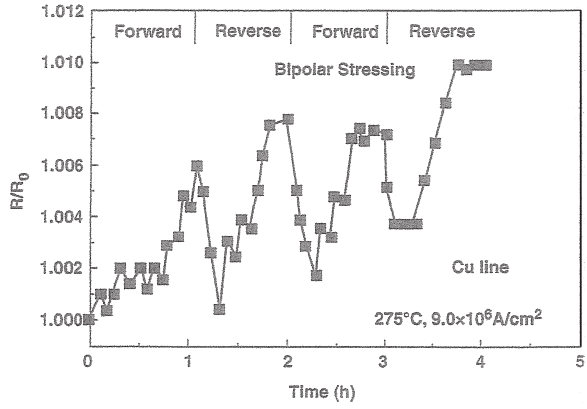

Figure 5.5.4 Normalized resistance for Cu interconnections vs. time under a low frequency bipolar current of peak current density = 9.0×10^6 A/cm^2 at 275°C. [5.174] (© IEEE 1993)

bipolar current waveform with peak current densities of $\pm 9.0 \times 10^6$ A/cm^2 of nearly 2-hour time period is shown in Figure 5.5.4. This figure clearly shows a damage recovery behavior under opposite current cycles though it shows an overall increase in resistance with successive cycles.

5.6 Models of Integrated Circuit Reliability

Reliability of an integrated circuit is a measure of the promise that it will carry out its function correctly during a given time period. Generally, it is expressed graphically by a bath-tub curve as shown in Figure 5.6.1. The portion of the curve depicting high failure rates at small times is called the infant mortality phase and accounts for the major built-in flaws in the components. The portion of the curve depicting high failure rates at large times is called the wear-out phase and accounts for the actual wear-out of the components. Rest of the curve defines the operating life of the integrated circuit. In general, the reliability of an integrated circuit can be enhanced by using better design techniques for its components, employing better manufacturing methods, using more stringent screening procedures, and providing redundancy within the integrated circuit so that it will perform its assigned function even if some of its components do actually fail. Several mathematical models to predict the reliability of an integrated circuit or components thereof have been proposed in the literature.

Arrhenius Model

Several physical mechanisms which result in the device failure can be modeled by the Arrhenius relationship, expressed as

$$\lambda(T) = \lambda(T_0)e^{\left[\frac{E_a}{k}\left(\frac{1}{T_0}-\frac{1}{T}\right)\right]} \tag{5.6.1}$$

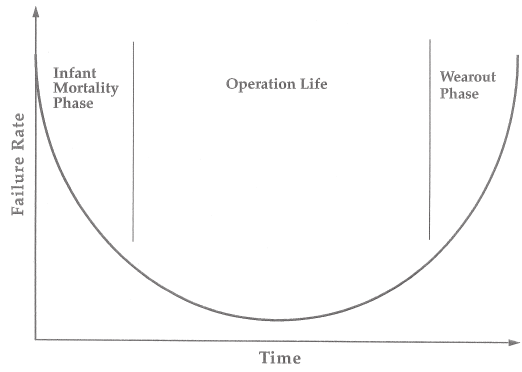

Figure 5.6.1 The bathtub curve showing failure rate as a function of time.

where

T = Temperature in ^oK
T_0 = Reference temperature in ^oK
$\lambda(T)$ = Failure rate at temperature T
E_a = Activation energy for the failure mechanism in eV
k = Boltzmann's constant in $eV/^oK$

Relationship (5.6.1) indicates that a physical mechanism having a lower activation energy results in a higher failure rate. The same is true for systems at higher operating temperatures.

Mil-Hdbk-217D Model

This is a semi-empirical model based on the measured lifetimes of a large number of devices after screening. It states that the failure rate λ in units of failures/10^6 hours can be predicted by the expression [171]

$$\lambda = \Pi_Q[C_1\Pi_T\Pi_V + (C_2 + C_3)\Pi_E]\Pi_L \tag{5.6.2}$$

where Π_Q is a quality factor dependent on the burn-in procedure used to remove devices suffering from built-in problems, Π_T is an acceleration factor dependent on the operating temperature, Π_V is a stress factor dependent on the operating voltage, Π_E is a factor dependent on the environment, Π_L is a learning factor and C_1, C_2, and C_3 are failure rates dependent on the complexity of the system expressed by the number of equivalent gates, number of pins, package type, etc. Values of C_1, C_2, and C_3 depend on the devices and their technologies and have been tabulated for several cases in reference [171]. The Mil-Hdbk-217D model is a widely used model and the data for this model has been constantly under revision to include new devices and technologies.

Series Model

A series model for calculating the reliability of an integrated circuit due to wear-out has been presented by Frost and Poole [172]. It is based on the assumptions that an integrated circuit consists of several basic elements

that are not necessarily identically distributed, the states of the various elements with respect to their being functional or failed are mutually statistically independent, the failure distribution of each element is known as priori, and the failure of any one element of the series system causes the IC to fail.

The failure rate λ_s of a system of n elements having failure rates λ_i ($i = 1, 2, 3,\ldots\ldots, n$) can be found by adding the failure rates of the elements, i.e.,

$$\lambda_s(t) = \sum_{i=1}^{n} \lambda_i(t) \tag{5.6.3}$$

If the n elements are identical, i.e.,

$$\lambda_1(t) = \lambda_2(t) = \ldots = \lambda_n(t) = \lambda(t)$$

then Eqn. (5.6.3) reduces to:

$$\lambda_s(t) = n\lambda(t) \tag{5.6.4}$$

The probability of failure function $Fs(t)$ of a series system can be determined by using the formula

$$F_s(t) = 1 - \prod_{i=1}^{n} [1 - F_i(t)] \tag{5.6.5}$$

where $F_i(t)$ is the probability of failure function for the ith element.

The series model can be used to predict the reliability of a system with respect to any of the physical processes which cause wear-out. These include interconnection metallization failure due to electromigration or corrosion, oxide shorts, threshold voltage shifts in MOS devices, and alpha-particle induced soft errors. A physical process can cause two types of defects which result in the failure of the system called the structural defects and the performance defects. A structural defect represents an abrupt change in the circuit topology such as the one caused by open-circuiting of a conductor. A performance defect represents a continuous

degradation of the system until its operation performance falls below an acceptable level. The series model treats these two defects in the same way.

Series-Parallel Model

As shown in the next section, an interconnection or a component thereof can be modeled as a series-parallel combination of several straight segments. Then, the probability of failure as a function of time, i.e., $F_{sp}(t)$ can be determined by using the expression:

$$F_{sp}(t) = [1 - \{1 - F_{11}(t)\}^{N_{11s}}\{1 - F_{12}(t)\}^{N_{12s}} \ldots \{1 - F_{1n}(t)\}^{N_{1ns}}]^{N_{1p}}$$
$$[1 - \{1 - F_{21}(t)\}^{N_{21s}}\{1 - F_{22}(t)\}^{N_{22s}} \ldots \{1 - F_{2n}(t)\}^{N_{2ns}}]^{N_{2p}} \ldots$$
$$[1 - \{1 - F_{m1}(t)\}^{N_{m1s}}\{1 - F_{m2}(t)\}^{N_{m2s}} \ldots \{1 - F_{mn}(t)\}^{N_{mns}}]^{N_{mp}} \tag{5.6.6}$$

where the total number of parallel units is equal to $N_{1p} + N_{2p} + \ldots + N_{mp}$, N_{mp} is the number of identical parallel units in the mth set and the total number of identical series units in the mth set of parallel units is equal to $N_{m1s} + N_{m2s} + \ldots + N_{mns}$. The function $F_{mn}(t)$ in Eqn. (5.6.6) is the probability of failure function for the nth unit of the mth set. For a series system of N_s identical units, Eqn. (5.6.6) reduces to:

$$F_s(t) = 1 - [1 - F(t)]^{N_s} \tag{5.6.7}$$

in agreement with Eqn. (5.6.5). For a parallel system of N_p identical units, it becomes:

$$F_p(t) = [F(t)]^{N_p} \tag{5.6.8}$$

5.7 Modeling of Electromigration Due to Current Pulses

In the past, most of the work on electromigration effects in the VLSI interconnections has been limited to steady (DC) currents and the chip design rules have been based on these DC models. However, most

VLSI devices are now digital and use unipolar or bipolar pulsed currents throughout the chip. In a few modeling efforts [138, 142] and experimental studies [136–140] concerned with pulsed or alternating currents, the pulsed current guidelines have been developed from the DC design rules by substituting the average current density of the pulsed current for the DC current density. In other words, if r denotes the duty factor of the pulsed current of density J_p (assumed constant), then the corresponding DC current density J_{dc} is given by

$$J_{dc} = r J_p \tag{5.7.1}$$

In principle, according to Eqn. (5.7.1), current density J_p can be increased in direct proportion as the duty factor r is decreased with no effect on the design rules. This is simply not true in all cases. Here, a simulation model for the major physical processes that influence the electromigration-induced damage in interconnections due to pulsed electric currents [173] is presented. It should be noted that experimental verification of the model is required before its predictions can be used in design guidelines.

Modeling of Physical Processes

An expression that adequately describes the mass flow rate due to an electrical current density is

$$J_a = \left(\frac{ND}{kT}\right)(Z^* q)E \tag{5.7.2}$$

where

J_a = Atomic flux in atoms per cm^2/second,
N = Number of metallic ions/cm^3,
D = Diffusion coefficient in cm^2/second,
k = Boltzmann's constant in joules/°K,
T = Temperature in °K,
Z^* = Effective mobile ion charge number,
q = Electronic charge = 1.6×10^{-19} C, and
E = Electric field strength in volts/cm.

In Eqn. (5.7.2), the divergence of metallic ion flux due to geometric conditions, microstructural conditions, thermal conditions, or any combination thereof, can be expressed in terms of the mass continuity equation

$$\frac{\partial N}{\partial t} + \nabla \bullet J_a = 0 \tag{5.7.3}$$

Further, the effect of local heating on the movement of metal atoms can be included in terms of the temperature dependence of the diffusion coefficient D in Eqn. (5.7.2) given by

$$D = D_0 e^{\left(-\frac{E_a}{kT}\right)} \tag{5.7.4}$$

where D_0 is a numerical factor independent of temperature and E_a is the activation energy whose value depends on the predominant manner of diffusion. It should be noted that the rate of electromigration-induced degradation of the interconnection line is also influenced by the mechanical stress generated by the difference in thermal expansion coefficients and mechanical properties such as elastic moduli of the line and its surrounding material.

To account for the several physical factors present in a complex system consisting of the interconnection line, its dielectric overcoating, its dielectric undercoating, and the substrate, the Eqn. (5.7.2) should be modified to

$$J_a = \left(\frac{ND}{kT}\right)(-\nabla U) \tag{5.7.5}$$

where U is the electrochemical potential which, as a first approximation, should be taken as

$$U = Z^* qV + kTln\left(\frac{N}{N_0}\right) + \Omega S_{nm} + \mu_0 \tag{5.7.6}$$

where

V = Electric potential in volts,
N_0 = Equilibrium metal ion concentration at reference condition in number/m^3,
Ω = Atomic volume in m^3,
S_{nm} = Mechanical stress in Newton/m^2, and
μ_0 = Reference c hemical potential in joules.

Substituting Eqn. (5.7.6) in Eqn. (5.7.5), we get

$$J_a = \left(\frac{ND}{kT}\right)\left[Z^* qE - \left(\frac{kT}{N}\right)(\nabla N) - \Omega\nabla(S_{nm})\right] \tag{5.7.7}$$

Equation (5.7.7) states that the electric force caused by the exchange of momentum between the electrons and the metallic ions is opposed by the diffusion force caused by the nonequilibrium ion concentration differences and the mechanical force caused by the longitudinal pressure differences.

Now, as done previously [90], we can define a term P called "Porosity" as the local incremental change in metal ion concentration given by the expression

$$\frac{\partial P}{\partial t} = -\left(\frac{1}{N}\right)\frac{\partial N}{\partial t} \tag{5.7.8}$$

Combining equations (5.7.3) and (5.7.5), dividing the resulting equation on both sides by N and substituting in Eqn. (5.7.8), we obtain

$$\frac{\partial P}{\partial t} = -\left(\frac{1}{N}\right)\nabla\bullet\left[\left(\frac{ND}{kT}\right)(\nabla U)\right] \tag{5.7.9}$$

First-Order Model Development

First, we assume that the grain sizes in the interconnection line follow a lognormal distribution characterized by a median value D_{50} and standard deviation s. Next, for an interconnection line of length L, we divide it into N_l segments of equal length D_{50}, i.e., $N_l = L/D_{50,}$ where N_l is taken as the nearest integer value. Further, if W is the width of the interconnection line, we partition it into N_w parallel strips of width $D_{50,}$ each with some remaining strip of width less than D_{50} such that $N_w = W/D_{50,}$ where N_w is taken as the larger nearest integer. For a line of width less than D_{50}, $N_w = 1$. Thus, each interconnection segment of length D_{50} has N_w locations or nodes where mass flux divergence is possible. The mass flux divergence factor (Df) at each node defined by the indices (k, l) with $1 \le K \le N_1$ and $1 \le 1 \le N_w$ can now be calculated from the relationship

$$D_f(k, l) = \sum_i \sin\left(\frac{\theta_i}{2}\right)\cos(\phi_i) - \sum_j \sin\left(\frac{\theta_j}{2}\right)\cos(\phi_j) \tag{5.7.10}$$

where ϕ is the random grain boundary angle with respect to the longitudinal centerline of the metallization line for each grain boundary on either side of each node and θ is another random angle selected for each grain boundary on either side of the node used to calculate a mobility factor for mass transfer along the grain boundary [135].

The divergence of the metal ion flux at the node (k, l) can now be calculated from

$$\nabla \bullet J_a(k, l) = \left[\frac{ND}{D_{50}\, kT}\, D_f(k, l)\right](-\nabla U) \tag{5.7.11}$$

where, as a first-order approximation, it is assumed that the electric field, mobile metallic ion concentration gradient, and longitudinal pressure gradient are appropriately averaged macroscopic quantities and, therefore, the forcing function terms in the factor $(-\nabla U)$ can be regarded as constants with respect to the divergence operation. The rate of porosity development at the node (k, l) is then given by

$$\frac{\partial P}{\partial t} = \left[\frac{D_0}{D_{50}\, kT}\, D_f(k, l)\right]\left[e^{\left(-\frac{E_a}{kT}\right)}\right](-\nabla U) \tag{5.7.12}$$

and the increment of porosity (ΔP) developed at node (k, l) over an increment of time (Δt) can be obtained from

$$\Delta P(k, l) = \left[\frac{\partial P}{\partial t}\right]\Delta t \tag{5.7.13}$$

The calculation of (ΔP) in Eqn. (5.7.13) needs an evaluation of every force term in $(-\nabla U)$.

The first force term in $(-\nabla U)$ is due to the electric field E and is equal to $(Z^* qE)$. Including the effect of local current crowding due to the development of porosity [2] at node (k, l), the local value of the electric field E is given in terms of the local current density J by the expression

$$E = J \cdot \rho = \left[\frac{J_0}{1 - P(k, l)}\right] \cdot \rho_0[1 + \alpha\{T(k) - T_a\}] \tag{5.7.14}$$

where

J_0 = Initial current density uniform throughout the undamaged interconnection line in amperes/cm^2,

ρ_0 = Initial electrical resistivity of the interconnection metal at temperature T_a in $\Omega \cdot$ cm,

α_a = Temperature coefficient of resistivity,
$T(k)$ = Local temperature at the boundary of kth segment, and
T_a = Ambient temperature

It should be noted that the porosity factor $1/[1 - P(k,l)]$ in Eqn. (5.7.14) is used only for $P(k,l) > 0$. Further, for a continuous train of unipolar current pulses applied to the interconnection line resulting in local current density pulses of amplitude *Jp* for a duration of δ seconds with a repetition period of Γ seconds, the duty factor "*r*" of these pulses is given by

$$r = \frac{\delta}{\Gamma} \tag{5.7.15}$$

resulting in a local power dissipation of $[r\rho(J_p)^2]$. This heat flows away from the interconnection line longitudinally by thermal conduction and transversely through a dielectric layer (such as silicon dioxide) to the substrate (such as silicon) acting as a heat sink assumed to be at the constant ambient temperature T_a. This heat flow is given in terms of the local temperature $T(k)$ by the equation

$$r\rho(J_p)^2 = \frac{K_m}{(D_{50})^2}[T(k) - T(k-l)] + \frac{K_0}{(d_0\ d_m)}[T(k) - T_a] + \frac{K_m}{(D_{50})^2}[T(k) - T(k+l)] \tag{5.7.16}$$

where

K_m = Thermal conductivity of the interconnection metal in watts/(cm.°k),
K_0 = Thermal conductivity of the dielectric layer in watts/(cm.°k),
d_0 = Thickness of the dielectric layer in cm, and
d_m = Thickness of the interconnection metal in cm.

The next force term in $(-\nabla U)$ is due to diffusion and can be considered as equivalent to the force exerted by a threshold electric field *E*th, i.e.,

$$Z^* qE_{th} = \left(\frac{kT}{L}\right) ln\left[\frac{1 - F_g}{1 - F_l}\right] \tag{5.7.17}$$

where

L = Length of the interconnection line in cm,
Fg = Average fractional mass gain along the line (corresponding to negative porosity), and
Fl = Average fractional mass loss along the line (corresponding to positive porosity).

The last force term in $(-\nabla U)$ is due to a pressure gradient along the length of the line and is caused by the transfer of mass by the electromigration and the tendency to accumulate mass at various places along the line. It can be approximated by

$$\Omega \frac{dS_{nm}}{dx} = \left(\frac{\Delta V_0}{\Delta N_0}\right)\left(\frac{1}{L}\right)\left(\frac{1}{\beta}\right)\left(\frac{\Delta N}{N_0}\right) \tag{5.7.18}$$

which has been obtained by putting the approximate expression for the bulk compressibility

$$\beta = \left(\frac{1}{V_0}\right)\frac{dV}{dS} \tag{5.7.19}$$

into its incremental form

$$\Delta S = \left(\frac{1}{\beta}\right)\left(\frac{\Delta V}{V_0}\right) \tag{5.7.20}$$

and combining it with the relation between volume increase and mass increase

$$\frac{\Delta V}{V_0} = \frac{\Delta N}{N_0} \tag{5.7.21}$$

In terms of the average fractional mass gain F_g, Eqn. (5.7.18) can be rewritten as

$$\Omega\frac{dS_{nm}}{dx} = \left(\frac{\Delta V_0}{\Delta N_0}\right)\left(-\frac{F_g}{\beta L}\right) \tag{5.7.22}$$

Substituting the force terms given by equations (5.7.14), (5.7.17), and (5.7.22) into equations (5.7.12) and (5.7.13), the increment of

porosity (ΔP) developed over an increment of time (Δt) can be obtained from

$$\Delta P(k,l) = \left[\frac{D_0 D_f(k,l)}{D_{50} kT(k)}\right] \cdot \left[e^{\left(-\frac{E_a}{kT(k)}\right)}\right] \cdot [Z^* q j_0 \rho_0 \{1 + \alpha[T(k) - T_a]\}] \cdot \left[\frac{r}{1 - P(k,l)}\right] - \left[\frac{kT(k)}{L}\right] ln\left[\frac{1 - F_g}{1 - F_l}\right] - \left(\frac{\Delta V_0}{\Delta N_0}\right)\left(-\frac{F_g}{\beta L}\right)\Bigg] \tag{5.7.23}$$

It should be noted that a factor r has been inserted in the electric force term because this force is applied for a fraction of the time only, whereas the diffusion and pressure gradient force terms are present at all times. Further, the time increment (Δt) can be larger than or equal to one pulse repetition period Γ.

In general, the failure criterion for the interconnection line can be stated in terms of the attainment of maximum tolerable fractional increase in the line resistance, elevation of the temperature at a node to the melting point of the interconnection metal, or the attainment of pressure level at any point along the line that exceeds the strength of the covering layer, if present. Here, the results are calculated using the fractional change in the line resistance (R/R_0) as an indicator of the progress of electromigration-induced damage and it is calculated by using the expression

$$\frac{R}{R_0} = \left(\frac{1}{N_l}\right)\left[\sum_k \frac{1}{\sum_l \left(\frac{N_w}{1 - P(k,l)}\right)}\right] \tag{5.7.24}$$

where only a loss of mass is considered to affect the line resistance, i.e., $P(k,l)$ is taken to be zero for those nodes where there is an accumulation of mass.

Modeling Results for DC Currents

In order to validate the physical factors included in the simulation model presented above, the simulation results obtained by using the model can

be compared with the experimental observations of various workers. In the following results, the values of the various parameters used in the model are taken as follows: constant factor in the diffusion coefficient (D_0) = 10^{-4} cm^2/sec; effective charge on the metal ion (Z^*) = −1; activation energy for diffusion (E_a) = 0.67 eV (typical of Al-Cu alloys); bulk compressibility (β) = 1.33×10^{-11} m^2/N (for Al); and thermal conductivity of the oxide layer = 0.0096 W/cm°C. In addition, the Wiedemann-Franz law is used for the thermal conductivity of the interconnection metal and the temperature dependence for the metal resistivity is taken to be given by

$$\rho = 2.42\times10^{-6}[1 + 0.00475(T - 273)] \qquad \Omega \cdot cm \quad (5.7.25)$$

The effect of an oxide coating in reducing the rate of electromigration in an interconnection line of length (L) = 50 μm, width (W) = 2 μm with D_{50} = 2 μm, s = 0.5 carrying a DC current of density (J) = 1 MA/cm^2 at temperature (T) = 200°C is shown in Figure 5.7.1. This figure shows that time at which the line resistance begins to rise very rapidly increases

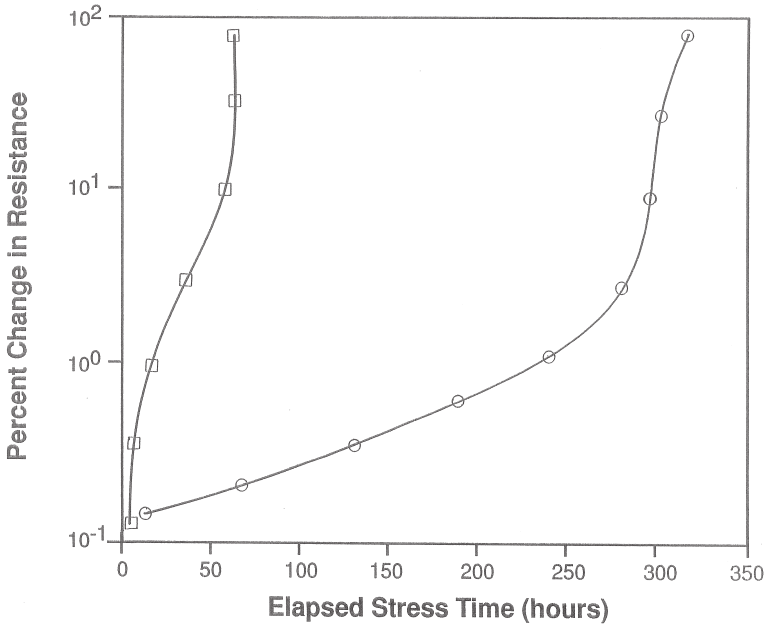

Figure 5.7.1 Simulation results showing the effect of oxide coating on the rate of development of electromigration-induced line failure [5.172]. (© 1988 IEEE)

nearly six times for the coated line (shown by circles) than with the uncoated line (shown by squares). Such a significant rise in the time to failure for coated lines has been observed experimentally by many workers.

Using a failure criterion of 10% resistance change, the effect of line length on the failure time is shown in Figure 5.7.2. The line parameters are $W = 2$ μm, $D_{50} = 2$ μm, $s = 0.5$ subjected to a DC current of $J = 1$ MA/cm^2 at $T = 200$°C. Squares indicate the results based on the present model, while the circles indicate those calculated from the statistical model presented in the reference [125]. This figure shows that lifetime increases rapidly as the line gets shorter which is in agreement with experimental observations.

The simulation results showing the dependences of the MFT on the normalized width (W/D_{50}) for 20 lines with $L = 50$ μm subjected to a DC current of $J = 1$ MA/cm^2 at T = 200°C are shown in Figure 5.7.3. For the upper curve (with squares), $D_{50} = 3$ μm and $s = 0.5$; for the middle curve (with circles), $D_{50} = 2$ μm and $s = 0.5$; and for the lower

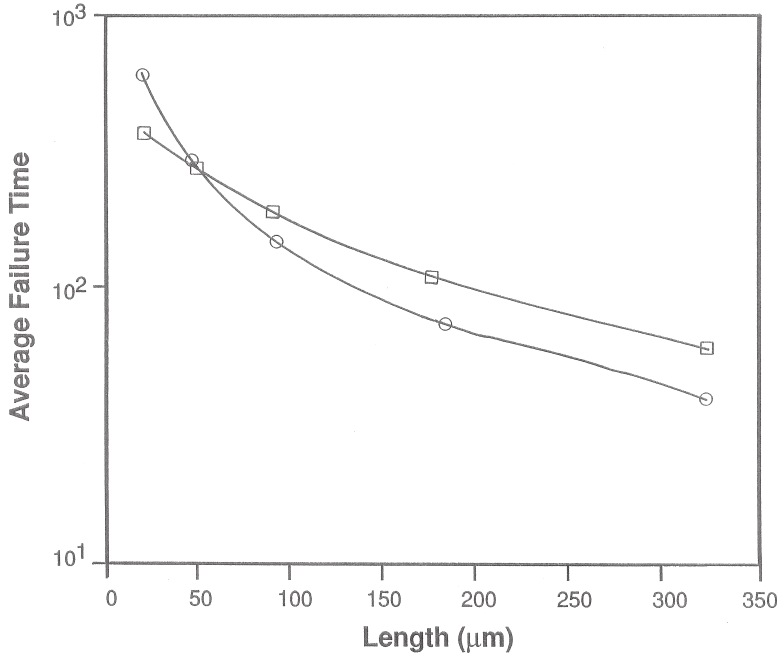

Figure 5.7.2 Simulation results showing the effect of line length on failure time [5.172]. (© 1988 IEEE)

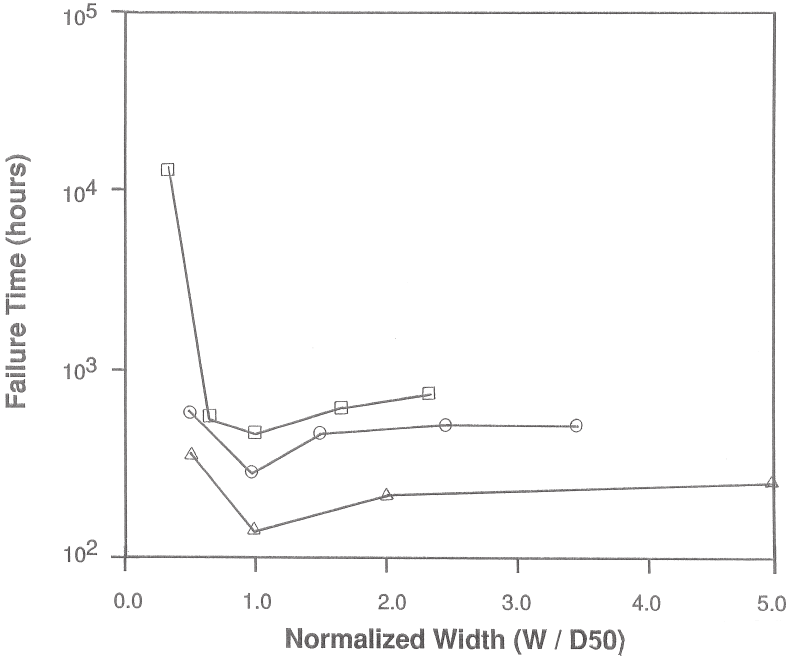

Figure 5.7.3 Simulation results showing the effect of line width on failure time [5.172]. (© 1988 IEEE)

curve (with triangles), $D_{50} = 1$ μm and $s = 0.5$. All curves indicate a minimum at about $W/D_{50} = 1$ which is in agreement with the observations of Kinsbron [126].

The effect of the DC current density on the failure time is shown in Figure 5.7.4. The upper curve (with squares) is for a line of length 50 μm and activation energy 0.67 eV (characteristic of Al-Cu alloys) with both ends kept at the ambient test temperature of 200°C and an oxide thickness of 1 μm with the substrate held at ambient temperature. The medium curve (with circles) shows the effect of allowing the ends of the line to float, i.e., adiabatic end conditions. The lower curve (with triangles) is for a 200 μm line having activation energy of 0.55 eV (characteristic of Al-Si lines) with adiabatic end conditions. The upper, middle, and lower curves correspond to −1.2, −1.5, and −1.5 power dependences upon the DC current densities, respectively. These values agree very well with experiments.

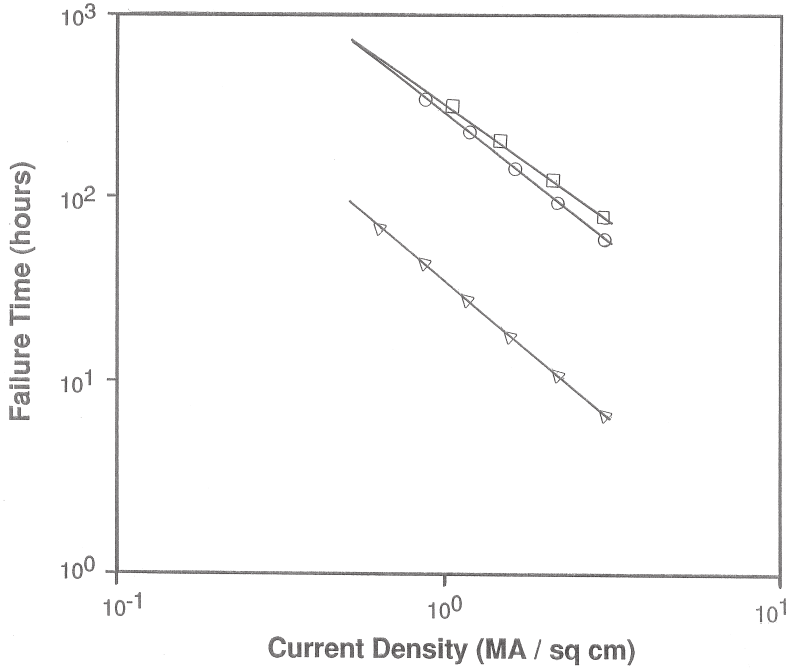

Figure 5.7.4 Simulation results showing the effect of dc current density on failure time [5.172]. (© 1988 IEEE)

Modeling Results for Pulsed Currents

For pulsed current following the relation $Jp = J_{DC}/r$ with $J_{DC} = 1$ MA/cm^2 (typical of accelerated testing of electromigration), the percent changes in the line resistance as functions of the elapsed stress time for r values of 0.03125, 0.0625, 0.125, 0.25, 0.5, and 1.0 are shown in Figure 5.7.5. The value of $r = 1.0$ corresponds to the DC case. For these results, both ends of the lines are kept at the ambient temperature of 200°C and the values of the line and other parameters are $L = 50$ μm, $W = 2$ μm, $D_{50} = 2$ μm, $s = 0.5$, and T = 200°C. Figure 5.7.5 shows that, for very short duty cycles, there is a significant decrease in the time at which the line resistance begins to increase rapidly.

Assuming a more general relationship between the DC current density and peak current density given by

$$J_p = \frac{J_{dc}}{(r)^m} \tag{5.7.26}$$

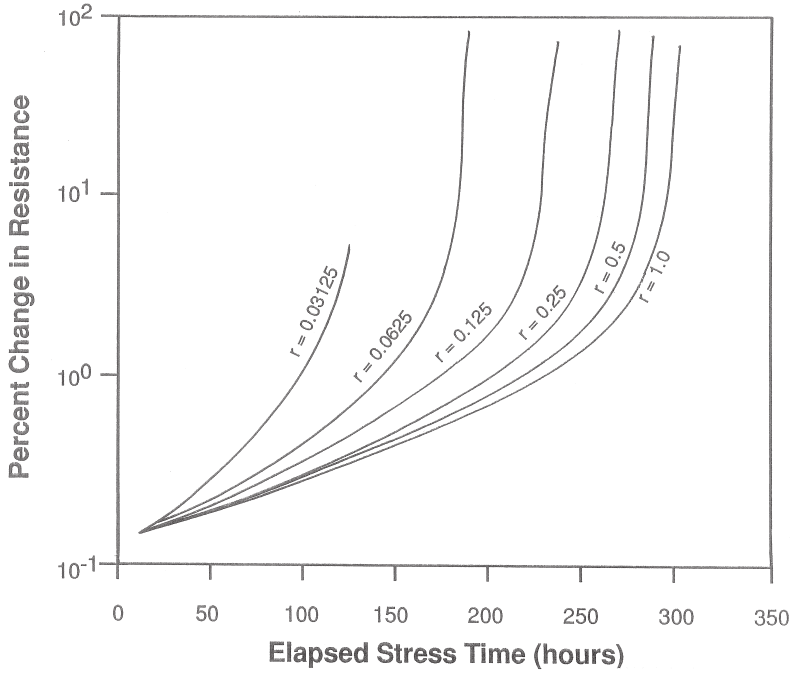

Figure 5.7.5 Simulation results showing the effect of peak current density on failure time for various values of r [5.172]. (© 1988 IEEE)

where m is a constant in the range 0 to 1, the dependences of the times required to reach 3% change in the line resistance on the duty factor r for values of $m = 0.5$, 0.666, 0.75, 0.85, and 1.0 (for curves from top to bottom) are shown in Figure 5.7.6. These results assume a 1 μm thick oxide layer with the surface below the oxide and the ends held at the ambient temperature. It should be noted that, for J_p given by Eqn. (5.7.26), the local power dissipation is given by

$$r\rho(J_p)^2 = r\rho\left(\frac{J_{dc}}{r^m}\right)^2 = \frac{\rho(J_{dc})^2}{r^{(2m-1)}} \tag{5.7.27}$$

which shows that, at a 5% duty cycle ($r = 0.05$), there is 20 times as much power dissipation as in the DC case ($m = 1.0$), but only about 11 times as much power dissipation when $m = 0.9$.

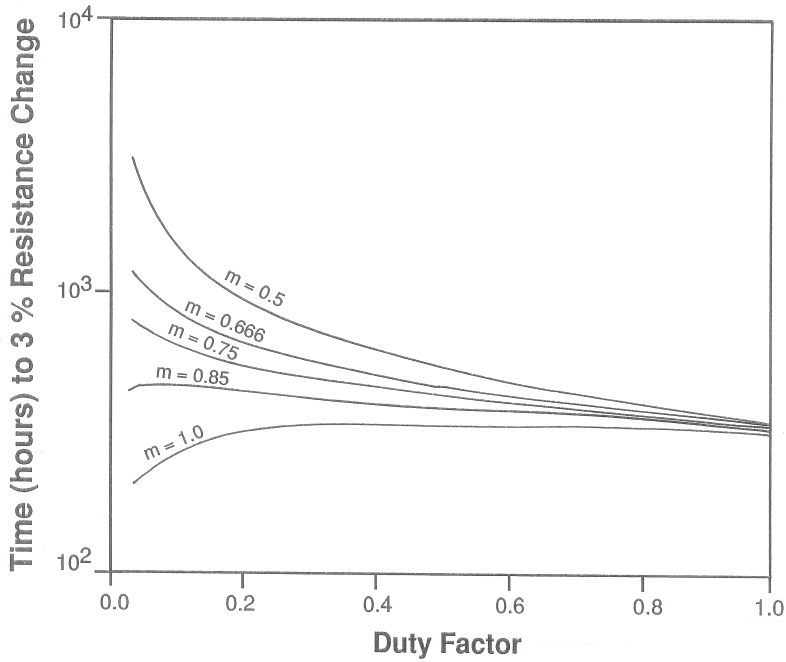

Figure 5.7.6 Simulation results showing the effect of duty factor exponent on failure time [5.172]. (© 1988 IEEE)

Exercise 5.1

According to Eqn. (5.7.16), the local power dissipation from the interconnection line is given by

$$r\rho(J_p)^2 = \frac{K_m}{(D_{50})^2}[T(k) - T(k-l)] + \frac{K_0}{(d_0 d_m)}[T(k) - T_a] + \frac{K_m}{(D_{50})^2}[T(k) - T(k+l)]$$

This equation does not account for the details of heat transfer from the substrate to the ambient environment. Comment on the significance of this missing factor and modify the equation to include this process.

Exercise 5.2

Eqn. (5.7.16) is time independent. This is valid as long as the pulse repetition rate is of the order of megahertz because the thermal time constant for a typical metal line/dielectric layer combination is usually one or more microseconds. Modify the equation so that it is also valid for lower pulse repetition rates.

5.8 Guidelines for Testing Electromigration

In the literature [92], it has been suggested that the following guidelines should be followed for the testing procedure:

Dimensions of the Test Line

a) The test line should have the minimum interconnection width used for that set of the IC family.
b) The length of the test line must be greater than 1 mm to obtain accurate results.

Test Line Preparation

a) The current to this test line should be fed by a wider lead (between two to five times the width) and leads must be greater than 0.125 mm on both sides to reach the bond pads. Long-bond pads greater than 1 mm should be avoided because it does not represent typical IC interconnections.
b) The test line fabrication process should simulate the practiced interconnection process for the IC family. For example, the test line should share the same parameters and thickness, go through an identical processing as for the other lines in the IC family, and be packaged in a standard IC package very similar to that used for the IC family.

Testing Conditions

a) The thickness data (after film deposition and/or lead patterning) coupled with the width of the line should be used to calculate the current density. If a multilayer metal such as a barrier layer/conductor is used, then the cross section of the primary conductor system should be used for the current density calculation.

b) Current density between 0.8 and 1 MA/cm^2, depending on the structure of the line, is recommended.
c) High temperature is not recommended because the microstructure properties of the film may change at high temperature and that will lead to erroneous results. Besides, thermomigration may also take place. Ambient temperature between 125 to 215°C is recommended.
d) The test temperature should be reported. If the resistance of the leads and the temperature coefficient of resistance are accurately determined, the line temperature may be reported as the test temperature.
e) For the sake of accuracy, sample sizes of 15 to 20 should be used for testing electromigration at a chosen test temperature.

Calculations and Plots

a) Lognormal probability plots are recommended to determine the MTF and standard deviation.
b) Arrhenius plot of MTF vs. (1/T°K) with at least three or four data points should be used to determine the activation energy.
c) Since electromigration-induced failures are caused by divergences of atomic fluxes and the atomic flux is directly proportional to the current density, use $n = 1$ in Eqn. (5.1.10) for the MTF at low current densities, $n = 2$ for optimistic estimates of MTF at operating temperatures and at current densities less than 1 MA/cm^2. Use $n = 1.5$ when electromigration test data is collected at 1 MA/cm^2 and has to be extrapolated to current densities in the 0.1 to 0.6 MA/cm^2 range. Three current densities in the 0.6 to 1.2 MA/cm^2 range may be used to determine the value of the exponent n.
d) Failure times are assumed to obey lognormal distribution:

$$f(t) = \frac{1}{\sigma t} \exp\left[-\frac{1}{2}\left(\frac{ln(t) - ln(t_{50})}{\sigma}\right)^2\right] \tag{5.8.1}$$

The instantaneous failure, by definition, corresponds to the decrease in the number of surviving samples at time t and is given by

$$\lambda(t) = \frac{f(t)}{1 - F(t)} \tag{5.8.2}$$

where the cumulative failure density function

$$F(t) = \int_0^t f(t)dt \tag{5.8.3}$$

corresponds to the probability of failure in total time t. From the above equations, it is obvious that the failure rate increases with time and reflects the true wear-out mechanism of the interconnection due to the electromigration-induced damage.

e) If the conductor crosses an oxide step, a thinning step for film thickness should be determined and minimum cross section of the conductor at the oxide side should be used to calculate the maximum current density.

f) If a pulsed current is used for testing then the peak current or the maximum current pulse height in a lead should be used for the current density calculation and to find the MTF. If a transient is present, similar corrections are recommended.

g) Since reliability of the film interconnections is determined by its microstructure and alloy composition, detailed test procedures should be established to characterize the as-deposited and annealed films. Routine process control procedures should be followed to verify that the film properties are reproduced.

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CHAPTER 6

Other Interconnection Technologies

In this chapter, other interconnection technologies that seem promising for the high-speed integrated circuits are presented. Here are the chapter objectives:

- After going through section 6.1, students should be familiar with the advantages, issues, and challenges associated with the optical interconnections.
- After going through section 6.2, students should be familiar with the propagation characteristics for the superconducting interconnections and their comparison with the normal metallic interconnections.
- After going through section 6.3, students should be familiar with several potential interconnection technologies for the nanotechnology circuits.

6.1 Optical Interconnections

As the integrated circuits become larger in size and faster in speed, a large fraction of the available chip area and bandwidth are used by the interconnection system. Pinout and pin capacitance limitations place severe restrictions on the size and speed realizable for the integrated circuit. Furthermore, a large amount of power is used in driving the communication lines only. For example, on a typical current steering Schottky logic chip, 80% of its power is consumed in driving its communication lines [1]. Thus, conventional interconnections are becoming a major problem in the development of the next generation VLSI systems.

The optical interconnection technology is emerging rapidly to provide relief from the problems associated with the conventional interconnections [2]. Techniques have been developed to integrate optical devices and materials with electronic circuits. It is now possible to integrate optoelectronic devices, such as photodiodes, LEDs, and laser diodes, with the high-density silicon–based electronic circuits by depositing GaAs or other heterostructure layers on top of a processed silicon wafer and building the optical devices in the layers [3]. Techniques for constructing optical waveguides and mirrors on a silicon substrate have also been developed [4-6]. Here, the advantages, challenges, and other issues associated with the optical interconnections are addressed [4].

Advantages of Optical Interconnections

On-chip as well as chip-to-chip optical interconnections offer several advantages over the conventional interconnections in that they do not suffer from the drawbacks of the latter. As stated above, the drawbacks of the conventional interconnections become more pronounced when the integrated circuit becomes more complex either by scaling down the transistor sizes or by scaling up the chip size [7].

The first drawback of the conventional interconnections results from their capacitive loading effects which increase as the chip size increases. In fact, in the present day chips, interconnection delays dominate the device delays and the chip speed is limited primarily by the delays associated with the interconnection capacitances. On the other hand, optical interconnections are free from any capacitive loading effects. The speed of propagation of a signal using an optical interconnection is determined by the speed of light and the refractive index of the optical transmission medium only. Even if the time taken to convert from electrical signal to optical signal and to convert back to electrical signal are taken into consideration, the optical interconnections turn out to be as fast as the conventional interconnections for distances as small as a millimeter and, for longer distances, an optical interconnection is much faster than a conventional metallic interconnection.

The second drawback of the conventional interconnections is the crosstalk among the nearby electrical paths which is also caused by the

stray and other coupling capacitances among the interconnections. This crosstalk increases as the interconnections are brought closer and as the bandwidth of the signals is increased. Further, as the signal frequency goes up, the self and mutual inductances of the metal interconnections go up, resulting in higher crosstalk. In contrast, the optical interconnections do not suffer from the problem of crosstalk.

The next drawback of the conventional interconnections is the limitation on the number of pinouts available for chip-to-chip connections on a chip. According to a well-known empirical relationship called the Rent's rule, which applies to random logic circuitry, the number of pins required for chip-to-chip interconnections increases approximately as the $0.61th$ power of the number of devices and other components on the chip, whereas the perimeter available for fabricating these pins increases only as the $0.5th$ power of the number of devices on the chip. (In general, fewer pins are required for memories and more are required for telecommunications circuitry). This problem can be alleviated with chip-to-chip optical interconnections because they operate at much higher speeds than conventional I/O pins allowing the multiplexing of a large number of I/O signals in a single I/O fiber. Furthermore, the optical chip-to-chip interconnections can be anchored directly to the interior of a chip rather than to a pin on its perimeter.

The next problem faced by the conventional metallic interconnections is their failure caused by electromigration. Electromigration-induced failure becomes more pronounced as the interconnections become smaller. Optical interconnections do not suffer from electromigration. However, it is interesting to note that optical interconnections can breakdown due to optical damage which occurs only in certain materials at rather high optical power densities. For example, for the optical medium called $LiNbO_3$, the threshold for optical damage is of the order of tens of kW/cm^2 and that for other optical dielectric materials, such as glass and oxides, is an order of magnitude higher.

It should be noted that when the limitations of conventional VLSI systems are alleviated by using optical interconnection technologies, several new computing architectures become available allowing much quicker handling of complex problems such as matrix operations, digital filtering, distributed symbolic connections, and other interconnection intensive algorithms. Furthermore, optical chip-to-chip interconnections offer the

promise of significantly enhancing the performance of high-throughput performance systems such as supercomputers, fifth-generation computing systems, and massively parallel SIMD and MMID machines [8].

Systems Issues and Challenges

In order to develop large systems with optical interconnections, several researchers have chosen to employ thin-film waveguides rather than free-space, holographic, or optical fiber interconnections. This is primarily because the planarity of substrates with thin-film waveguides on them allows the use of conventional processing techniques, whereas the use of optical fibers for intrachip communication may require specialized equipment and holographic techniques are less mature than the thin-film techniques. However, it should be noted that the use of thin-film waveguides poses alignment and coupling problems which can be resolved by careful process control.

The material chosen for the development of systems with optical interconnections depends on several factors. For constructing optical devices, many researchers have used epitaxial deposition on silicon substrate because silicon offers a stable base for electronic circuitry and because long-wavelength optics requires epitaxial techniques on silicon or gallium arsenide. An additional advantage of silicon-based processing is that by developing an epitaxial technique for silicon that can yield three-dimensional structures, one can still incorporate a layer of GaAs circuitry where extremely high speed, available only with GaAs, is required. For example, GaAs circuitry may be used to provide multiplexors to achieve speed matching between the electronic circuitry and the optical interconnections.

Fault tolerance is a crucial issue in the development of large systems with optical interconnections. We have seen that the greatest advantage of optical interconnections lies in the larger systems employing chip-to-chip, wafer-to-wafer, or board-to-board connections rather than in a smaller system employing the on-chip connections and these are the systems having the greatest need for fault tolerance.

Material Processing Issues and Challenges

The development of optical interconnection systems requires specialized material processing techniques. One of the processing technique that has

shown great promise in this field is called molecular beam epitaxy (MBE). Currently, MBE is used primarily as a research tool and it is important to make it widely available as a manufacturing process. MBE can be used to build three-dimensional structures needed to build optoelectronic systems. For example, it can be used to deposit layers of compound semiconductors such as GaAs, GaInAlAsP, InAlAsP, etc. to construct superlattices. The techniques to build optoelectronic components, such as photodiodes, LEDs, and laser diodes, using MBE need to be refined.

It is also important to refine the etching and material deposition techniques for constructing optical waveguides, mirrors, etc. Techniques for anchoring optical fibers onto any part of a substrate with great accuracy need to be developed. Reliable connections between the Si and GaAs layers are required. It will be extremely helpful to integrate the processes for Si and GaAs which, at present, are very different [9]. Last but not least, it is obvious that the optical interconnection technology will require many more processing steps than the electronic circuits and it may be necessary to develop techniques to decrease the number of these steps to achieve an acceptable yield.

Design Issues and Challenges

Integrating on-chip and chip-to-chip optical interconnections with the electronic circuitry requires careful designing of the various optical structures such as the optical waveguides, detectors, sources, etc. A few well-known materials for constructing optical waveguides are glass, zinc oxide, and silicon nitride. Material selection for the optical waveguide depends on several factors such as the refractive index of the material, attenuation at the wavelength of operation, ease of patterning, and ease of deposition. Channels with very smooth sidewalls are formed in the substrate such as silicon by an etching mechanism so that the light beam does not suffer significant loss due to scattering. The channels are tapered down in sizes to the size of the optical detector such that the transition from the waveguide to the detector is very gradual and does not cause any serious loss of signal.

The material in which the optical detector is fabricated depends on the wavelength of the optical signal. In the near future applications, it is expected that the optical signal will be in the near infrared and the optical detectors can be fabricated on the silicon wafer itself because silicon is

Exercise 6.1

List and discuss the problems that need to be solved before the optical interconnections can be used for on-chip and for chip-to-chip communications.

the best-known detector material at these wavelengths. However, silicon cuts off at 1.1 μm and therefore, for optical signals of wavelength greater than 1.1, μm the detectors and the sources will have to be fabricated in an InP-type compound semiconductor.

For fabricating an optical source, silicon is not a suitable substrate because it is an indirect bandgap material. On the other hand, GaAs is an excellent material for fabricating an extremely efficient and reliable light source. The best way of utilizing the silicon-based electronic circuitry with the GaAs source depends on successful heteroepitaxial techniques of depositing GaAs on silicon. This is done by first depositing a layer of germanium (Ge) on silicon because Ge and GaAs have closely matching lattice constants. The bandwidth of the structure will depend on the ability of the light source to modulate at high frequencies. Further, the power from the source should be high enough for long-distance communication.

6.2 Superconducting Interconnections

Advantages of Superconducting Interconnections

The signal propagation characteristics, including transit delays of the chip-to-chip interconnection lines, have a major effect on the total performance of an electronic system. An attempt to reduce the interconnection delays by scaling down its dimensions results in increased signal losses in the interconnection [10]. This is due to the increased series resistance and higher dispersion of the interconnection. This adverse effect can be almost eliminated by replacing normal metallic interconnections by the superconducting interconnections which have very low series resistance at frequencies up to the energy gap frequency of the material [11, 12]. In fact, in the recent years, the advent of high-critical-temperature superconductors [13–15] has opened up the possibility of realizing high-density and very fast interconnections on the silicon as well as GaAs-based high-performance integrated circuits.

The major advantages of the superconducting interconnections over the normal metal interconnections can be summarized as follows:

a) The signal propagation time on a superconducting interconnection will be much smaller as compared to that on a normal metal interconnection.
b) The packing density of the integrated circuit can be increased without suffering from high losses associated with the high-density normal metal interconnections.
c) There is virtually no signal dispersion on the superconducting interconnections for frequencies up to several tens of gigahertz.

Propagation Characteristics of Superconducting Interconnections

Now, an analysis of propagation characteristics [16] on a superconducting microstrip line with dielectric thickness t_d, strip-line thickness t_c, ground plane thickness t_g, and penetration depth λ_L, shown in Figure 6.2.1, is presented. In the structure shown in Figure 6.2.1, material #1 is air with $\varepsilon_r = 1.0$; material #2 is Ba-Y-Cu-O with critical temperature (T_c) = 92.5°K, normal state resistivity (ρ_n) = $200^{\mu\Omega}$. cm, $\lambda_L(0)$ = 1,400 A°; material #3 is SiO_2 with $\varepsilon_r = 3.9$; material #4 is Ba-Y-Cu-O with T_c = 92.5°K, $\rho_n = 200_{\mu\Omega}$, $\lambda_L(0)$ = 1,400 A°; and material #5 is SiO_2 with $\varepsilon_r = 3.9$. It is assumed that the permeability of each medium is that of free space μ^o, the loss tangent of dielectrics is negligible, the fringing field effects at the edges of the line can be neglected, and that high T_c, superconductors have standard superconducting behavior below J_c, H_{c1}, T_c, and energy gap frequency. It can be further assumed that the only nonzero component of magnetic field is H_y and that all fields are independent of "*y*." In other words, in addition to the time dependence given by $e^{j\omega}$. the nonzero field components in rectangular coordinates are $H_y(x)^{e-\omega}$, $E_x(x)^{e-\omega}$, and $E_z(x)^{e-\omega}$.

Using the two-fluid model [17, 18], the total current J_T in a superconductor consists of normal current J_n and a supercurrent J_s, i.e.,

$$\vec{J}_T = \vec{J}_n + \vec{J}_s \tag{6.2.1}$$

where the supercurrent component obeys the London's equations

$$\vec{E} = j\omega\mu_0\lambda_L^2\vec{J}_s$$

$$\vec{H} = -\lambda_L^2\nabla\times\vec{J}_s \tag{6.2.2}$$

where λ_L is the penetration depth of the superconductor. The boundary value problem presented in Figure 6.2.1 can be solved by using equations (6.2.1), (6.2.2), and the Maxwell's equations to obtain the propagation constant γ which is valid for frequencies up to several gigahertz (note that normal current component is negligible for these frequencies). γ is given by the equation

$$\gamma^2 = -\mu_0\varepsilon_3\omega^2\left[1 + \frac{\lambda_{L,2}}{t_d}\coth\left(\frac{t_c}{\lambda_{L,2}}\right) + \frac{\lambda_{L,4}}{t_d}\coth\left(\frac{t_g}{\lambda_{L,4}}\right)\right] \tag{6.2.3}$$

According to Eqn. (6.2.3), γ is purely imaginary indicating that the propagation characteristics of a superconducting microstrip line are lossless and dispersionless.

The phase velocity of propagation for the superconducting microstrip is given by

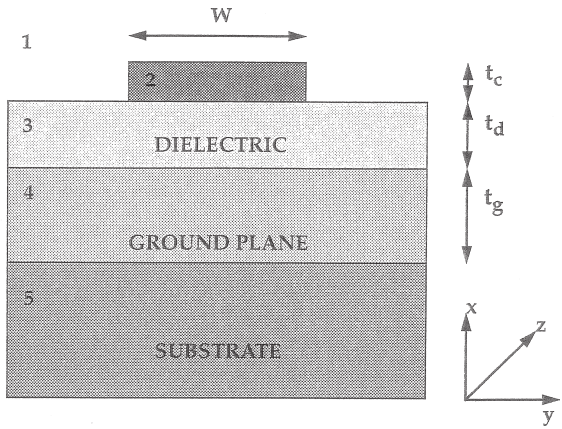

Figure 6.2.1 Schematic diagram of the superconducting microstrip structure analyzed in this section [20]. (© 1987 IEEE)

$$v_p = \frac{\omega}{Im(\gamma)} = \frac{1}{\sqrt{\mu_o \varepsilon_3 \left[1 + \frac{\lambda_{L,2}}{t_d} \coth\left(\frac{t_c}{\lambda_{L,2}}\right) + \frac{\lambda_{L,4}}{t_d} \coth\left(\frac{t_g}{\lambda_{L,4}}\right)\right]}} \quad (6.2.4)$$

Equation (6.2.4) indicates that the phase velocity depends strongly on the superconducting layer thickness, penetration depth of the superconducting layers, and the dielectric constants of the dielectric layers. Since the penetration depth is a function of temperature given by

$$\lambda_L(T) = \frac{\lambda_L(0)}{\sqrt{1 - \left(\frac{T}{T_c}\right)^4}} \quad (6.2.5)$$

the phase velocity also depends on temperature, particularly for temperatures near the critical temperature T_c. It can also be seen from Eqn. (6.2.4) that the phase velocity is a function of the dielectric constant only when the dielectric thickness and the superconducting layer thickness are much larger than the penetration depth.

Using the two-fluid model, the conductivity of a superconductor is given by [18]

$$\sigma = \sigma_{normal}\left(\frac{T}{T_c}\right)^4 - j\frac{1}{\mu_0 \omega [\lambda_{L,2}(0)]^2}\left[1 - \left(\frac{T}{T_c}\right)^4\right] \quad (6.2.6)$$

where σ_{normal} is the normal state conductivity of the superconductor at temperature just above T_c.

Comparison with Normal Metal Interconnections

Here, a comparison of the propagation characteristics of the superconducting and normal aluminum interconnections at 77°K [16] is presented. The interconnection dimensions and other transmission line parameters for the aluminum line are chosen to be the following:

Width of the microstrip line (W) = 2 μm

Thickness of the microstrip (t_c) = 0.5 μm

Interdielectric thickness (t_d) = 1 μm

Ground-plane thickness (t_g) = 1 μm

Relative dielectric constant for the interdielectric = 3.9

Relative dielectric constant for the substrate = 3.9

Conductivity of 0.5 μm thick aluminum at 77°K = 1.5×10^6 S/cm

Capacitance of the line = 1.54 pF/cm

Inductance of the line for frequencies up to 10 GHz = 2.95 nH/cm (decreasing to 2.25 nH/cm for frequencies above 100 GHz, due to skin effect).

Series resistance of the line for frequencies up to 10 GHz = 77.6 Ω/cm (increases as the frequency increases above 10 GHz, due to skin effect)

A comparison of the phase velocities at 77°K for the superconducting line and the aluminum line for frequencies up to 10^{12} Hz is shown in Figure 6.2.2 and a comparison of the attenuation for the two lines in the

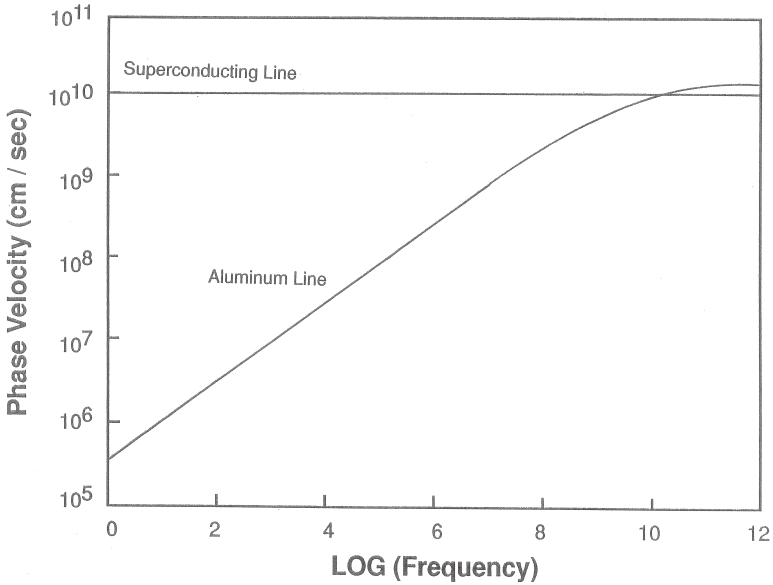

Figure 6.2.2 Comparison of the phase velocities at 77oK for superconducting and normal aluminum lines [20]. (© 1987 IEEE)

frequency range 10^6–10^{12} Hz is shown in Figure 6.2.3. First, for the normal aluminum interconnection line, it can be seen that its phase velocity is much less than that of the superconducting line for frequencies up to 100 MHz. Further, its phase velocity depends very strongly on frequency indicating that the line is very dispersive. Figure 6.2.3 indicates that, for normal aluminum line, its maximum useful length (attenuation <3 dB) is limited by attenuation to be 2 cm at 100 MHz and only 2 mm at 10 GHz.

For the superconducting interconnection line, it can be seen from Figure 6.2.2 that its phase velocity is nearly constant at frequencies up to 1 THz at 77°K, i.e., the line is virtually nondispersive. However, as shown in Figure 6.2.3, the attenuation of the superconducting line is a function of frequency and temperature; it is very small for frequencies up to 10 GHz and increases with increasing frequency. Therefore, superconducting interconnections can operate with negligible dispersion and low loss at frequencies of several GHz for lengths exceeding several meters.

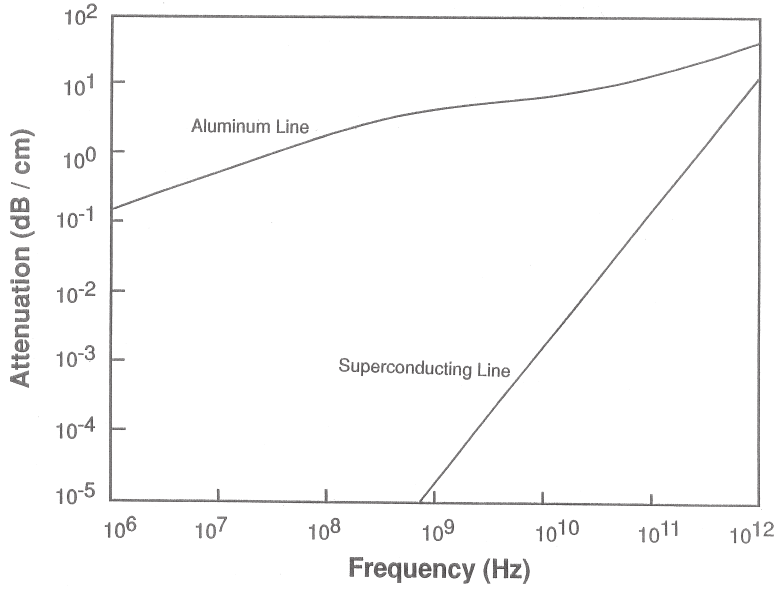

Figure 6.2.3 Comparison of the attenuations at 77oK for superconducting and normal aluminum lines [20]. (© 1987 IEEE)

Exercise 6.2

tList and discuss the problems that need to be solved before the superconducting interconnections can be used for on-chip and for chip-to-chip communications.

6.3 Nanotechnology Circuit Interconnections

As progress along the International Technology Roadmap for Semiconductors (ITRS) continues, physical and electromagnetic limitations make scaling of silicon CMOS FETs increasingly difficult. One long-term solution is to replace Si FETs by completely new structures such as nanoscale molecular, biological, or quantum devices. Before considering this changeover, an interconnection technology must be developed that is suitable for these new device concepts. To connect ultra-small devices, interconnections must be less than 10 nanometers (nm) in diameter. However, they still must be easy to fabricate, have low resistance, high maximum current carrying capacity, and be isolated by low-k dielectric materials for applications in nanotechnology circuits requiring ultra-high density of the devices and interconnections. This implies that in addition to the development of the various nano devices, interconnections that will be used to connect these devices in nanotechnology circuits should be given a very special attention. It is extremely important to gain an understanding of the parasitic elements such as capacitances and inductances and interconnection performance parameters such as propagation delays, crosstalk, and current carrying capacities for almost electromigration-free operation for the various interconnection technologies in the nanoscale regime. In the past, such models have been developed for the micro scale metallic interconnections [19].

In the future development of the nanoscale-integrated circuits, interconnections will play a crucial role. As the sizes of the active devices approach the nanometer dimensions, the wires that connect them must also be scaled down. Several IC manufacturers are in the process of commercializing 100 nm CMOS-based IC technologies and the research and development work for the 70 and 50 nm devices is well underway. Successful IC development below these feature sizes faces the fundamental challenges imposed by the basic lays of quantum physics. In addition, as the diameters of the conventional metallic interconnection

wires reach the mean free path for electrons, the surface scattering from the boundaries of ultra-narrow conductors as well as the grain boundary scattering would inhibit electronic conduction in the wires to an unacceptable level.

Nanotechnology circuits [20–26] with devices on the sub-100 nm scale will require interconnections with sizes from 50 nm down to molecular and atomic dimensions. If metallic conducting lines, such as copper, are used for the interconnections, then the miniaturization process will result in rise in the copper resistivity because the dimensions of the conducting lines will be of the same order of magnitude as the mean free path of electrons which is 39.3 nm in copper at room temperature. This rise in resistivity may dramatically slow the circuit's functioning and as a result jeopardize the ability to improve the circuit speed expected from miniaturization. Electromigration which is the result of momentum transfer from the electrons moving under the applied electric field to the ions making up the lattice structure of the interconnection material imposes another serious problem. Continuing miniaturization of the thin-film metallic interconnections results in increasingly high current densities leading to the open- and/or short-circuit electrical failures of interconnections in a relatively short time. The higher the temperature, higher the electromigration-induced failure of the metallic interconnections is. In this context, it is important to note that lots of electrons and electron scattering are required for electromigration to take place. It does not occur in semiconductors unless they are so heavily doped that they exhibit metallic conduction. In this section, the various potential interconnection technologies suitable for nanoscale-integrated circuits including metallic interconnections, nanowires, carbon nanotubes (CNTs), and quantum wires have been reviewed.

Silicon Nanowire Interconnections

A nanowire is simply a solid, cylindrical wire with a diameter on the scale of a few nanometers. These can be fabricated from a variety of materials (silicon, germanium, gallium nitride, metals, oxides, etc.) to a length of several microns. Semiconductor nanowires are one-dimensional structures with unique electrical and optical properties that are used as building blocks in nanoscale circuit design. Their low dimensionality means that they exhibit quantum confinement effects. One of the challenges lies in

understanding the electron conduction and transport properties of these nanowires and how these can be used as interconnections for integrating various nanoscale devices such as single electron transistors and quantum cellular automata (QCA). These issues are relevant to the ultimate design of a nanoscale-integrated circuit regardless of the nature of the active element. As such these issues represent a fundamental element of the road map leading toward nanoscale integration. According to CM Lieber of Harvard, nanowires represent the smallest dimension for efficient transport of electrons and excitons, and thus will be used as interconnections and critical devices in nanoelectronics and nano-optoelectronics. Silicon nanowires, a class of nanowires, are good candidates for nanoscale interconnections [27].

Metal interconnections which are used to connect transistors on an integrated circuit chip have become the major bottleneck in furthering chip miniaturization. On-chip interconnections contribute much more to the chip's overall delay than that caused by the once dominant gate capacitances in transistors. This delay in interconnections is due to the presence of parasitic impedances characteristically seen in metal lines. These impedances are seen in the form of capacitances between an interconnection line and the substrate as well as between interconnection lines in different levels, line resistances and inductances, both self and mutual, due to induced magnetic fields. Over the years, researchers have been trying to reduce this delay by reducing the interconnection's RC time constant. For the 130 nm technology chips, this has been achieved to some extent with the replacement of aluminum with copper to reduce the line's resistance and by using low-k dielectric materials in the place of the industry standard silicon dioxide to reduce the capacitances. However, with ever increasing frequencies, scaling of minimum feature sizes, the reduction of resistances and capacitances as well as larger die sizes have all led to a growing dominance of on-chip inductances. These inductances have been largely ignored in the past. However, this trend cannot continue into the future [28, 29]. Inductance effects including ringing and reflections can distort the signals severely. If not considered, further scaling of devices and the use of higher frequencies will increase these effects leading to false switching in transistors, resulting in the chip's failure. To sum up, it is crucial to understand the effects of interconnection inductances on various signal and design parameters such as the signal rise and

fall times, power dissipation, repeater insertion processes, and the signal propagation. It is particularly true for nanoscale interconnections which are expected to be used for the 65 nm technology chips and onwards.

Nanotube Interconnections

Nanotubes are tiny tubes about 10,000 times thinner than a human hair and consist of rolled-up sheets of carbon hexagons. Discovered in 1991 by researchers at NEC, they have the potential for use as minuscule wires in ultra-small electronic devices. As shown in Figure 6.3.1, there are two main types of CNTs that can have high structural perfection. Single-walled nanotubes (SWNTs) consist of a single graphite sheet seamlessly wrapped into a cylindrical tube. Multiwalled nanotubes (MWNTs) comprise an array of such nanotubes that are concentrically nested like rings of a tree trunk [30].

Multiwalled nanotubes are generally in the range of 1 to 25 nm in diameter, while single-walled nanotubes have diameters in the range of 1 to 2 nm. Both SWNTs and MWNTs are usually many microns long and hence they can fit well as components in submicrometer-scale devices and nanocomposite structures that may play an important role in emerging technologies. IBM has recently been able to manipulate the nanotubes in a controlled way. They have developed the capability of changing a nanotube's position, shape, and orientation, as well as cutting it by using an

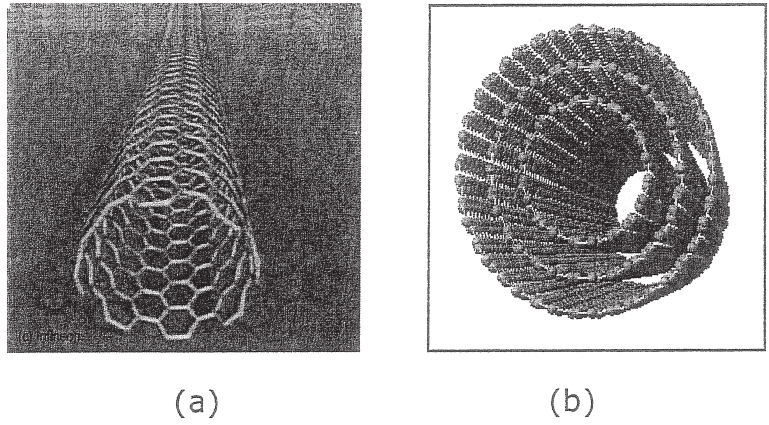

Figure 6.3.1 (a) Single-walled CNT; (b) Multiwalled CNT [39]. (© IEEE 2004)

atomic force microscope. NASA researchers have reported a new method for producing integrated circuits using CNTs instead of copper for interconnections. This technology may extend the life of the silicon chip industry by 10 years. The electrical properties of CNTs are fascinating because they can exhibit metallic or semiconducting behavior depending on their structure and dimensions. This has made CNTs a unique candidate material for potential nanotechnology applications as nanoscale electronic devices and interconnections [31–33].

To a large extent, the unique electrical properties of CNTs such as their extremely low electric resistance are derived from their one-dimensional (1-D) character and the unique electronic structure of graphite. Resistance primarily occurs due to defects in crystal structure, impurity atoms, or an atom vibrating about its position in the crystal. In the case of a CNT, the electrons are not so easily scattered. Due to the small diameter and the huge aspect ratio (length to width), nanotubes are essentially 1-D systems and therefore electrons have low chance of scattering giving rise to very low resistance. The electronic properties of perfect MWNTs are rather similar to those of perfect SWNTs because the coupling between the cylinders is weak in MWNTs.

Electrical transport in metallic SWNTs and MWNTs is ballistic, i.e., without scattering over long nanotube lengths, enabling them to carry high currents with essentially no heating. In contrast, electrons in copper travel only 40 to 50 nm before they scatter. Phonons also propagate easily along the nanotube. Superconductivity has also been observed at low temperatures with transition temperatures of nearly 0.55°K for 1.4 nm diameter SWNTs and nearly 5°K for 0.5 nm SWNTs.

The low resistance ensures that the energy dissipated in CNTs is very small, thereby solving the problem of dissipated power density that adversely affects silicon circuits. Current densities of more than 10^{10} A/cm^2 have been reported for the metallic configuration of CNTs. Since CNTs do not have any leftover bonds, there is no need to grow a film on the surface in order to tie up the free bonds and there is no need to restrict the gate insulator to silicon dioxide. This fact implies the use of other superior materials to insulate the gate terminal in a transistor which can result in a much faster device. The properties of CNTs can be summarized as follows:

a) The carrier transport is 1-D resulting in ballistic transport with no scattering and much less power dissipation. Scattering free current transport allows high current densities and improved signal delays.
b) All chemical bonds of the C-carbon atoms are satisfied and there is no need for chemical passivation of free bonds as in silicon.
c) The strong C-C covalent bonding gives the CNTs high mechanical and thermal stability and resistance to electromigration. Current densities as high as 10^{10} A/cm^2 can be sustained in metallic CNTs.
d) The diameter of a CNT is controlled by chemistry, not by fabrication.
e) Both active devices and interconnections can be made out of semiconducting and metallic nanotubes.
f) Thermal conductivity along the axis is roughly twice that of diamond.

CNTs have shown great promise for use as interconnections in nanotechnology circuit applications. This is particularly because they can conduct large currents of the order of a 10^6 A/cm^2 without any deterioration, thus avoiding the electromigration problems characteristic of metallic interconnections. The scattering-free transport of electrons possible in defect-free CNTs is a very attractive feature of CNTs for microelectronic applications. The reduction in the thickness of conventional metallic or polycrystalline interconnections leads to additional scattering at the surfaces and grain boundaries, thereby deteriorating the interconnection resistance. CNTs provide undistributed quasi-crystalline wire-like structure where pulses can travel uninterrupted by length dependent ohmic scattering. The approximate estimation of signal delays with a simple model proves that nanotubes would surpass classical wires with respect to signal delays. Plenty of work on using CNTs for building integrated circuits is in progress [34–37]. Researchers are also trying to develop complex gates and circuits by fabricating devices along the length of a single CNT.

Nanotube Vias

The ability to grow nanotubes at specific sites has helped researchers to design carbon nanotube vias [38]. Vias are defined as interconnections between wiring layers in chips and are prone to deterioration due to

current crowding and electromigration. CNTs have been proposed as an alternative for the metal plugs to overcome these problems. ULSI circuits have problems that originate from stress and electromigration of copper interconnections, particularly the vias. One proposed solution for this problem is to use the CNTs with large migration tolerance as vias. Bundles of CNTs must be used as vias to get enough current for LSI interconnections. Hot filament chemical vapor phase deposition (HF-CVD) can be used to grow carbon nanotube bundles in the via holes. Mechanical polishing with the diamond slurry can be done to control the length of the CNT vias after their growth.

Figure 6.3.2(a) suggests that the total resistance of the CNT via is about three orders of magnitude lower than that of a single CNT and that there is no visible degradation of the via current with time as shown in Figure 6.3.2(b). Such measurements show that the current flows in

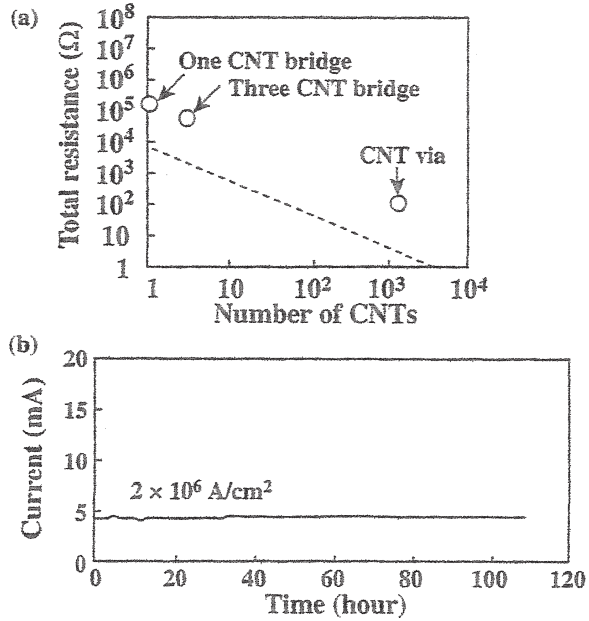

Figure 6.3.2 (a) Dependence of the resistance of a CNT bundle on the number of CNTs in the bundle. Resistances of a one-CNT bridge, three-CNT bridge, and a typical CNT via are also shown; b) Dependence of the current in a CNT via on time [41]. (© IEEE 2004)

parallel through the thousands of nanotubes used in the vias which are end bonded to the upper and lower electrodes [38]. The total resistance of a CNT via with about 5,000 nanotubes has been shown to be about 1 ohm and this resistance can be further reduced by improvements in the nanotube quality. The density of the CNTs needs to be increased and the diameters of the nanotubes need to be decreased for fabricating more effective CNT vias. It is expected that the CNT-bundle vias will prove to be effective replacements for copper vias for future ULSI interconnections.

Comparison of Nanotubes and Copper Interconnections

The potential performance of the carbon nanotube interconnections and their relative comparison to copper interconnections can be studied using physical models [39]. Nanotube bundles offer better performance than single nanotubes in which wave propagation is relatively slower. As the interconnection size decreases, the performance of copper interconnections goes down due to the increased resistivity as well as electromigration problems and CNTs have been proposed to be effective replacements due to the ballistic flow of electrons with electron mean free path of several micrometers. The latencies of the ideal carbon nanotube and copper interconnections are plotted in Figure 6.3.3. A single-walled nanotube results in a very high contact resistance and high characteristic impedance and hence a bundle of closely packed parallel CNTs is preferably used above a ground plane. The properties of the desired nanotube bundle include:

a) Good connections to all nanotubes within the bundle;
b) Distance between the nanotubes within the bundle should be as small as possible to have the largest nanotube density; and
c) Quantum coupling between the nanotubes should be nearly zero.

The ITRS predicts that the latency for carbon nanotube bundles will be given by [39]:

$$\tau_{bundle} = 0.7 R_{tr}(c_{bundle} L + C_L)$$

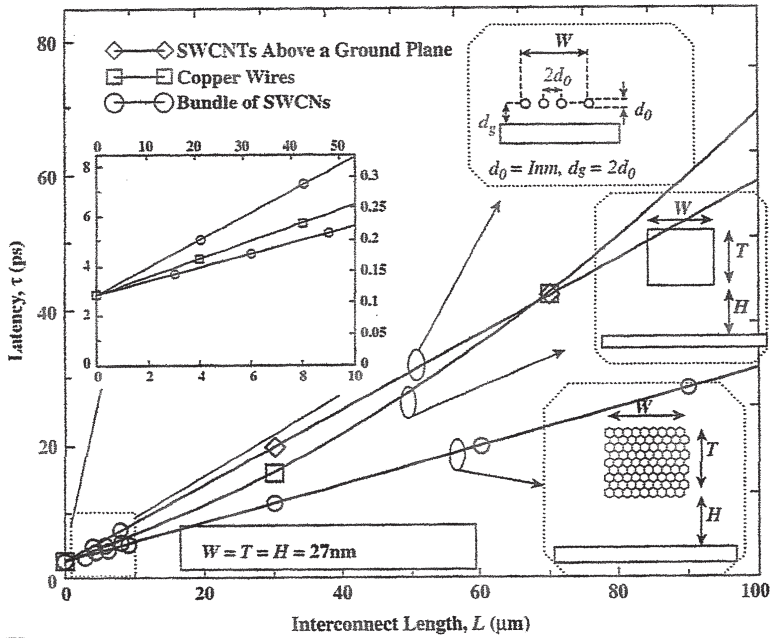

Figure 6.3.3 Dependence of latency on the interconnect length for ideal single-layered carbon nanotubes above a ground plane, 22 nm node copper wires (expected in 2016) and for bundles of ideal SWCNTs for n > 100 [42]. (© IEEE 2005)

where *Rtr* is the driver resistance, *CL* is the load capacitance, and *L* is the interconnection length. The diameters of the SWCNTs can be less than 1 nm and a bundle of, for instance, 400 SWCNTs can be as narrow as 20 nm. Assuming that the SWCNT resistance increases exponentially with length, Figure 6.3.4 shows the latencies of SWCNT bundles and copper interconnections (implemented at 22 nm node) vs. the interconnection length for electron mean free path, $L_0 = 5$ μm and for $L_0 = 10$ μm. This figure suggests that there is a length beyond which the latency of SWCNT bundles becomes larger than that of copper wires. This critical length is roughly 10 times the electron-mean free path in SWCNTs. From Figure 6.3.4, one can infer that compared to the 22 nm copper node, the bundles are about 30% faster for a mean free path of 5 μm, while they can be nearly 80% faster if a mean free path of 10 μm is achieved. Assuming that the SWCNT resistance increases linearly with length, dependences

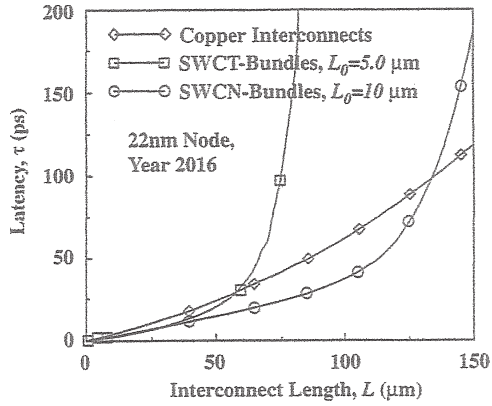

Figure 6.3.4 Dependence of latency on the interconnect length for a 22-nm node copper wire and bundles of SWCNTs with electron mean free paths of 5 and 10. It is assumed that SWCNT resistance increases exponentially with length [42]. (© IEEE 2005)

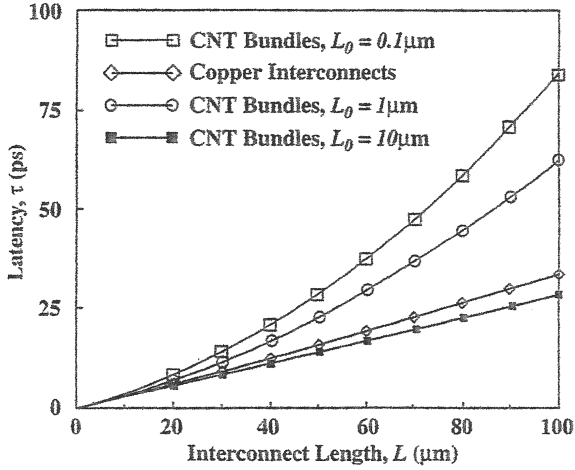

Figure 6.3.5 Dependence of latency on the interconnect length for a 22-nm node copper wire and bundles of SWCNTs with electron mean free paths of 0.1, 1, and 10. It is assumed that SWCNT resistance increases linearly with length [42]. (© IEEE 2005)

of the latency on the interconnect length for a 22 nm node copper wire and bundles of SWCNTs with electron mean free paths of 0.1, 1, and 10 μm are shown in Figure 6.3.5.

Quantum Cell-Based Wireless Interconnections

A digital signal can be propagated down a series of quantum cells by using what may be called "quantum wires." These are wireless interconnections, i.e., there is no actual contact between the cells. As shown in Figure 6.3.6, the coulomb repulsion forces the adjacent cells to align in the same "1" or "0" orientation for the low energy state, i.e., the ground state [40–44]. Hence, one can achieve wireless logic for propagation of signals. Based on this principle, quantum wires designed as a straight interconnection to achieve a 90° bend and to obtain a fanout of 2 are shown in Figure 6.3.7. In addition, quantum wires can be designed to carry crossover signals in the same plane. This kind of a wireless connection eliminates the usual electromigration problems associated with metallic interconnections in conventional integrated circuits. This also results in chip area saving and a much higher packing density.

Quantum cell-based interconnections form a part of a QCA which refers to an array of quantum cells that is fabricated at the nanometer scale and can be used to implement binary logic. These quantum cells can be arranged in principle to get all levels of circuit complexities from the basic logic gates such as inverters and adders to a complete nanocomputer. Though the current QCA-based circuit designs are limited to a single plane, it is possible that bilevel, trilevel, or even higher level circuits and interconnections will be used in future QCA designs.

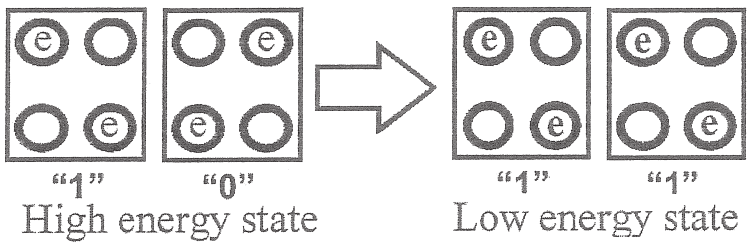

Figure 6.3.6 Ground state resulting from coulomb interaction between the two quantum cells.

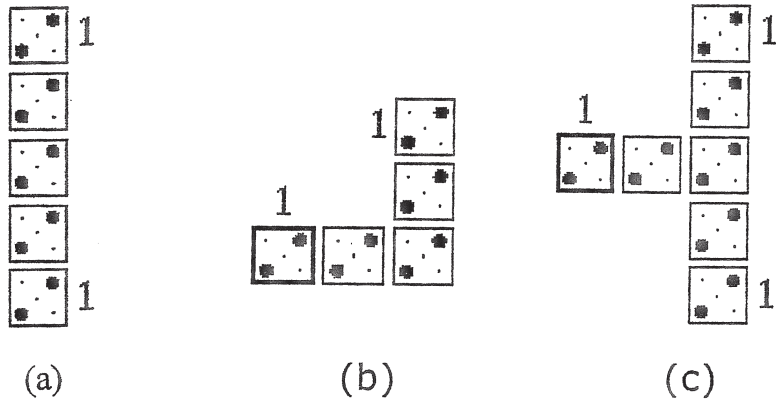

Figure 6.3.7 Layouts of quantum cells used to (a) design a straight wireless interconnection; (b) to achieve a 90o bend; and (c) to obtain a fanout of 2.

Exercise 6.3

List and discuss the problems that need to be solved before the nanotube, nanowire, and quantum cell based wireless interconnections can become a reality for nanotechnology circuits.

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APPENDIX A

Tables of Constants

Table A1 Physical constants

Boltzmann's constant	$k = 1.38 \times 10^{-23}\ J/K$
Electron's charge	$q = -1.6 \times 10^{-19}\ C$
Electron's rest mass	$m_0 = 9.11 \times 10^{-31}\ kg$
Permittivity of free space	$\varepsilon_0 = 8.85 \times 10^{-12}\ F/m$
Planck's constant	$h = 6.63 \times 10^{-34}\ J\text{-}s$
Speed of light	$c = 3 \times 10^{8}\ m/s$

Table A2 Properties of semiconductor substrates

Substrate Material	Relative Permittivity (ε_r)	Electron Mobility ($cm^2/V \cdot s$)	Melting Point (°C)
Si	11.8	1,350	1,415
Ge	16	3,900	936
GaAs	13.2	8,500	1,238
AlAs	10.9	1,200	1,740
GaP	11.1	300	1,467
ZnS	8.9	180	1,650
InP	12.4	4,000	1,070
SiC	10.2	500	2,930
InAs	14.6	22,600	943

Table A3 Properties of interconnection materials

Material	Resistivity ($\mu\Omega \cdot$ cm)	Melting Point (°C)
Pure aluminum (bulk)	2.65	660
Sputtered Al and Al/Si	2.9–3.4	660
Sputtered Al/2% Cu/1% Si	3.9	660
LPCVD aluminum	3.4	660
Pure tungsten (bulk)	5.65	3,410
CVD tungsten	7–15	3,410
Sputtered tungsten	14–20	3,410
Ti (bulk)	42.0	1,660
$TiAl_3$ (bulk)	17–22	1,340
$CuAl_2$ (bulk θ-phase)	5–6	591
WAl_2	–	647

Table A4 Resistivity and expansion coefficients [1.16] (© 1985 IEEE)

Material	Resistivity ($\mu\Omega \cdot$ cm)	Thermal Expansion Coefficient ($°C^{-1}$)	Melting Point (°C)
Pure aluminum (bulk)	2.65	$25.0 \cdot 10^{-6}$	660°C
Sputtered Al and Al/Si	2.9–3.4	$25.0 \cdot 10^{-6}$	660°C
Sputtered Al/2% Cu/1% Si	3.9	$25.0 \cdot 10^{-6}$	660°C
LPCVD aluminum	3.4	$25.0 \cdot 10^{-6}$	660°C
Pure tungsten (bulk)	5.65	$4.5 \cdot 10^{-6}$	3410°C
CVD tungsten	7–15	$4.5 \cdot 10^{-6}$	3410°C
Evaporated/sputtered tungsten	14–20	$4.5 \cdot 10^{-6}$	3410°C
Ti (bulk)	42.0	$8.5 \cdot 10^{-6}$	1660°C
$TiAl_3$ (bulk)	17–22	—	1340°C
$CuAl_2$ (bulk—θ phase)	5–6	—	591°C
WAl_{12}	—	—	647°C
Si	—	$3.3 \cdot 10^{-6}$	—
SiO_2	—	$0.5 \cdot 10^{-6}$	—

APPENDIX B

Method of Images

The method of images can be used to find the potential due to a given electric charge in the presence of conducting planes and dielectric surfaces. In other words, the presence of conducting planes and/or dielectric surfaces is represented by image charges.[1]

To illustrate this method, consider a line charge ρ lying in a medium of dielectric constant ε_1 and at a distance d above a second medium of dielectric constant ε_2, as shown in Figure A.2.1. At the interface of the two media, the following two boundary conditions must be satisfied:

a) The normal component of the electric flux density (D_n) must be the same on the two sides of the interface; and
b) The tangential component of the electric field (E_t) must also be the same across the interface.

Using the coordinate system of Figure A.2.1, it means that at $y = 0$,

$$D_{n1} = D_{n2} \qquad \text{or} \qquad \varepsilon_1 E_{y1} = \varepsilon_2 E_{y2} \tag{A.2.1}$$

and

$$E_{x1} = E_{x2} \tag{A.2.2}$$

The potential V due to an infinite line charge (ρ) in a medium of dielectric constant ε at a distance r is given by

$$V = \frac{-\rho}{4\pi\varepsilon} ln(r^2) \tag{A.2.3}$$

[1]A treatment of the method of images can be found in any standard text on Electrodynamics.

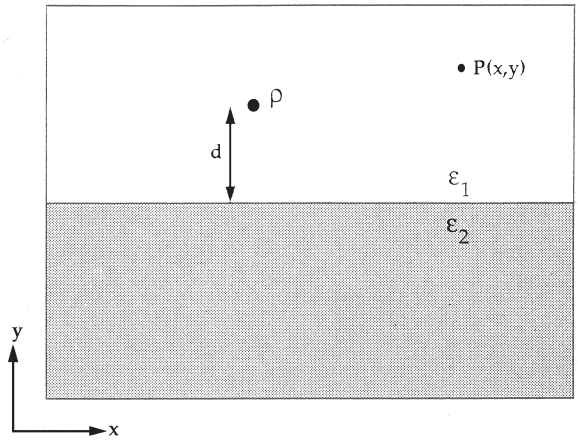

Figure A.2.1 A line charge ρ lying in a medium of dielectric constant ε_1 at a distance d above a second medium of dielectric constant ε_2.

When a second dielectric is present, the real charge ρ produces image charges across the dielectric interface. If the observation point P is above the interface, i.e., on the same side as the real line charge (see Figure A.2.2(a)), an image charge ρ_1 will be at a distance d below the interface. With the real line charge at $x = 0$ and $y = d$, the distance between the real charge and the observation point is given by

$$r = \sqrt{[x^2 + (y - d)^2]}$$

and with the image charge at $x = 0$ and $y = -d$, the distance between the image charge and the observation point is given by

$$r_i = \sqrt{[x^2 + (y + d)^2]}$$

Using Eqn. (A.2.3), the potential at all points above the interface, i.e., for $y \geq 0$ will be

$$V_1 = \frac{-1}{4\pi\varepsilon_1}[\rho\, ln(r^2) + \rho_1\, ln(r_i^2)]$$

Now since

$$E_{x1} = -\frac{\partial V_1}{\partial x}$$

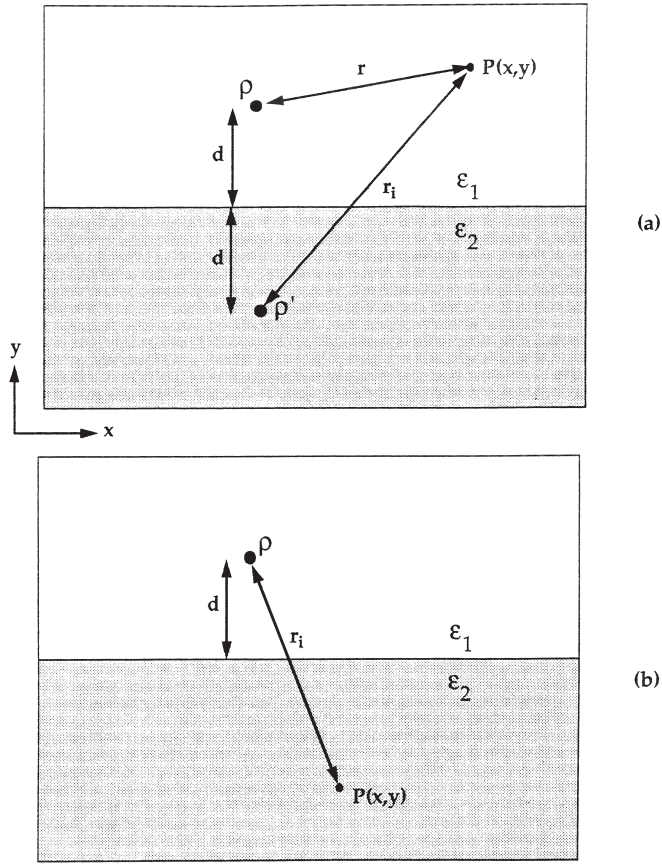

Figure A.2.2 (a) Observation point P on the same side as the real line charge; (b) Observation point P below the dielectric interface.

Therefore, for $y \geq 0$

$$E_{x1} = \frac{1}{4\pi\varepsilon_1}\frac{\partial}{\partial x}[\rho\, ln(x^2 + (y-d)^2) + \rho_1\, ln(x^2 + (y+d)^2)]$$

or

$$E_{x1} = \frac{1}{4\pi\varepsilon_1}\left[\rho\frac{2x}{[x^2 + (y-d)^2]} + \rho_1\frac{2x}{[x^2 + (y+d)^2]}\right] \qquad \text{(A.2.4)}$$

Similarly

$$E_{y1} = -\frac{\partial V_1}{\partial y}$$

Therefore, for $y \geq 0$

$$E_{y1} = \frac{1}{4\pi\varepsilon_1}\frac{\partial}{\partial y}[\rho\ ln(x^2 + (y-d)^2) + \rho_1\ ln(x^2 + (y+d)^2)]$$

or

$$E_{y1} = \frac{1}{4\pi\varepsilon_1}\left[\rho\frac{2(y-d)}{[x^2 + (y-d)^2]} + \rho_1\frac{2(y+d)}{[x^2 + (y+d)^2]}\right] \qquad \text{(A.2.5)}$$

If the observation point P lies below the dielectric interface, i.e., in the medium with dielectric constant ε_2 (see Figure A.2.2(b)) then the real line charge ρ must be modified to take care of the effect of the dielectric interface. This modified charge, say ρ_2, can be found in terms of ρ as shown below. The distance between the observation point and the charge ρ is again given by

$$r = \sqrt{[x^2 + (y-d)^2]}$$

The potential V_2 below the interface is then given by

$$V_2 = \frac{-1}{4\pi\varepsilon_2}[\rho_2\ ln(r^2)]$$

Now, since

$$E_{x2} = -\frac{\partial V_2}{\partial x}$$

Therefore, for $y \leq 0$

$$E_{x2} = \frac{1}{4\pi\varepsilon_2}\frac{\partial}{\partial x}[\rho_2\ ln(x^2 + (y-d)^2)]$$

or

$$E_{x2} = \frac{1}{4\pi\varepsilon_2}\left[\rho_2\frac{2x}{[x^2 + (y-d)^2]}\right] \qquad \text{(A.2.6)}$$

Similarly

$$E_{y2} = -\frac{\partial V_2}{\partial y}$$

Therefore, for $y \leq 0$

$$E_{y2} = \frac{1}{4\pi\varepsilon_2}\frac{\partial}{\partial y}[\rho_2 \ ln(x^2 + (y-d)^2)]$$

or

$$E_{y2} = \frac{1}{4\pi\varepsilon_2}\left[\rho_2 \frac{2(y-d)}{[x^2 + (y-d)^2]}\right] \tag{A.2.7}$$

Applying the continuity condition (A.2.2) to the equations (A.2.4) and (A.2.6), we get

$$\frac{1}{4\pi\varepsilon_1}[\rho + \rho_1]\left[\frac{2x}{x^2 + d^2}\right] = \frac{\rho_2}{4\pi\varepsilon_2}\left[\frac{2x}{x^2 + d^2}\right]$$

From this, it follows that

$$\frac{\rho + \rho_1}{\varepsilon_1} = \frac{\rho_2}{\varepsilon_2} \tag{A.2.8}$$

Applying the continuity condition (A.2.1) to the equations (A.2.5) and (A.2.6), we find that

$$\frac{\varepsilon_1}{4\pi\varepsilon_1}(-\rho + \rho_1)\left[\frac{2d}{x^2 + d^2}\right] = \frac{\varepsilon_2\rho_2}{4\pi\varepsilon_2}\left[\frac{-2d}{x^2 + d^2}\right]$$

from which, it follows that

$$-\rho + \rho_1 = -\rho_2 \tag{A.2.9}$$

Combining equations (A.2.8) and (A.2.9), we get

$$\frac{\rho + \rho_1}{\varepsilon_1} = \frac{\rho - \rho_1}{\varepsilon_2}$$

from where the image charges ρ_1 and ρ_2 can be found in terms of the real charge ρ and the dielectric constants ε_1 and ε_2 to be

$$\rho_1 = \rho\left(\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2}\right) \tag{A.2.10}$$

and

$$\rho_2 = \rho\left(\frac{2\varepsilon_2}{\varepsilon_1 + \varepsilon_2}\right) \tag{A.2.11}$$

For finding the image of a charge in a grounded conducting plane, it is well known that the image charge has the same magnitude as the real charge but an opposite sign and that it lies as much distance below the ground plane as the real charge is above it.

APPENDIX C

Method of Moments

The method of moments is a basic mathematical technique for reducing functional equations to the matrix equations [A.3.1]. To illustrate this method, consider the inhomogenous equation

$$L(f) = \mathrm{g} \tag{A.3.1}$$

where L is a linear operator, f is a field or response (the unknown function to be determined), and g is a source or excitation (a known function). We assume that the problem is deterministic, i.e., there is only one solution function f associated with a given excitation g.

Let us expand the function f in a series of basis functions $f_1, f_2, f_3, \ldots,$ f_n in the domain of L as

$$f = \sum_n \alpha_n f_n \tag{A.3.2}$$

where α_n is a constant. The functions f_n are called expansion functions or the basis functions. For exact solutions, Eqn. (A.3.2) is usually an infinite summation and the functions f_n form a complete set of basis functions. For approximate solutions, Eqn. (A.3.2) is usually a finite summation. Substituting Eqn. (A.3.2) into Eqn. (A.3.1) and using the linearity of the operator L, we have

$$\sum_n \alpha_n L(f_n) = g \tag{A.3.3}$$

Now, defining a set of weighting functions or testing functions w_1, w_2, $w_3, \ldots$ in the range of L and taking the inner product with each w_m, the result is

$$\sum_n \alpha_n \langle w_m, Lf_n \rangle = \langle w_m, g \rangle; \; \mathrm{m} = 1, 2, 3, \ldots$$

This set of equations can be written in the matrix form as

$$\left[l_{mn}\right]\left[\alpha_n\right] = \left[g_m\right]$$

where

$$\left[l_{mn}\right] = \left[\langle w_m, Lf_n\rangle\right]$$

$\left[\alpha_n\right]$ and $\left[g_m\right]$ are the column vectors. If the matrix $\left[l_{mn}\right]$ is nonsingular then the matrix $\left[l_{mn}\right]^{-1}$ exists. The constants α_n are then given by

$$\left[\alpha_n\right] = \left[l_{mn}\right]^{-1}\left[g_m\right]$$

and the solution function f is given by Eqn. (A.3.2) as

$$f = \sum_n \alpha_n f_n = \left[l_{mn}\right]^{-1}\left[g_m\right]\left[f_n\right]$$

This solution may be exact or approximate depending upon the choice of the functions f_n and the weighting functions w_n. The particular choice $w_n = f_n$ is known as the Galerkin method. If the matrix $\left[l_{mn}\right]$ is of infinite order, it can be solved only in special cases, e.g., if it is diagonal. If the sets f_n and w_n are finite then the matrix $\left[l_{mn}\right]$ is of finite order and can be inverted by known methods such as the Gauss–Jordan reduction method.

In most problems of practical interest, the integration involved in evaluating the $lmn = \langle w_m, Lf_n\rangle$ is usually difficult to perform. A simple way to obtain approximate solutions is to require that Eqn. (A.3.3) be satisfied at certain discreet points in the region of interest. This process is called a point-matching method. In terms of the method of moments, it is equivalent to using Dirac delta functions as the weighting functions. Another approximation useful for practical problems involves dividing the region of interest into several small subsections and requiring that the basis functions f_n are constant over the areas of the subsections. This procedure called the method of subsections often simplifies the evaluation of the matrix $\left[l_{mn}\right]$. Sometimes, it is more convenient to use the method of subsections in conjunction with the point-matching method.

One of the most important tasks in any particular problem is the proper choice of the functions f_n and w_n. The functions f_n should be linearly independent and chosen so that some superposition (A.3.3) can approximate the function f reasonably and accurately. The functions w_n should also be linearly independent and chosen so that the products $\langle w_n, g \rangle$ depend on the relative independent properties of g. Some additional considerations while choosing the functions f_n and w_n are the accuracy of the solution desired, ease of evaluation of the matrix elements, size of the matrix that can be inverted, and the realization of a well-conditioned matrix.

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R.F. Harrington, "Matrix Methods for Field Problems," *Proc. IEEE*, 55, no. 2, pp. 136–149, February 1967.

APPENDIX D

Transmission Line Equations

A transmission line can be treated as a repeated array of small resistors, inductors, and capacitors. In fact, the transmission line theory can be developed in terms of ac circuit analysis but the equations become extremely complicated for all but the simple cases [A.4.1]. It is more convenient to treat such lines in terms of differential equations which lead naturally to a wave equation which is of fundamental importance to electromagnetic theory in general.

We can develop the differential equations for a uniform transmission line by a simple circuit analysis of its equivalent circuit shown in Figure A.4.1 consisting of several incremental lengths and then taking the limit as the length of the increment approaches zero. The notations of voltage and current at some general points x and $(x + \Delta x)$ along the line are shown in Figure A.4.1. The parameters R, L, G, and C are the resistance, inductance, conductance, and capacitance values per unit length of the line, respectively. As Δx is changed, these values remain the same. We assume that the voltage and current are sinusoidal and that at any point x along the line, the time variation of voltage is given by

$$v_x = V_0 e^{j\omega t}$$

Now, if we apply the Kirchhoff's voltage law around the first incremental loop in Figure A.4.1, we obtain

$$\upsilon_x = i_x R\,\Delta x + i_x (j\omega L)\Delta x + \upsilon_{x+\Delta x}$$

or

$$\upsilon_{x+\Delta x} - \upsilon_x = -i_x (R + j\omega L)\Delta x \qquad \text{(A.4.1)}$$

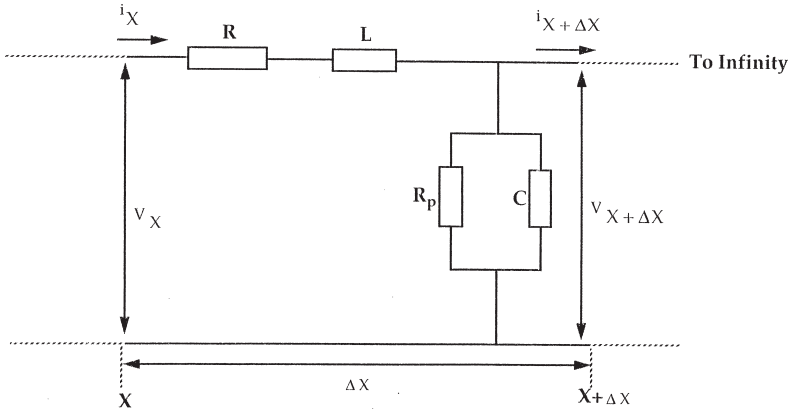

Figure A.4.1 Equivalent circuit for a uniform transmission line

In the above equations, R and L have been multiplied by Δx to get the actual values of resistance and inductance for an incremental section of length Δx. Now, the total current i_x into the first incremental section at x minus the total current $i_{x+\Delta x}$ into the next section at $x + \Delta x$ must be equal to the total current through the shunt capacitance C and the parallel resistance R_p, i.e.,

$$i_x - i_{x+\Delta x} = \frac{v_x}{[R_p/\Delta x]} + \frac{v_x}{[1/(j\omega C\Delta x)]}$$

or, setting $1/R_p = G$, the conductance per unit length, we get

$$i_{x+\Delta x} - i_x = -v_x(G + j\omega C)\Delta x \tag{A.4.2}$$

In Eqn. (A.4.1), the left hand side represents the incremental voltage drop along the line denoted by Δv_x. Dividing both sides of Eqn. (A.4.1), we get

$$\frac{\Delta v_x}{\Delta x} = -i_x(R + j\omega L)$$

Similarly, Eqn. (A.4.2) can be expressed as

$$\frac{\Delta i_x}{\Delta x} = -v_x(G + j\omega C)$$

Now, if Δx is made very small then the incremental voltage or current change per incremental distance becomes the corresponding derivative. Thus we get the two fundamental differential equations for a uniform transmission line

$$\frac{dv_x}{dx} = -(R + j\omega L)i_x \tag{A.4.3}$$

$$\frac{di_x}{dx} = -(G + j\omega C)v_x \tag{A.4.4}$$

where all line parameters are per unit distance. These equations can be solved if they can be written in terms of one unknown (v_x or i_x). An equation in terms of v_x can be written by first taking the derivative of Eqn. (A.4.3) with respect to x to yield

$$\frac{d^2 v_x}{dx^2} = -(R + j\omega L)\frac{di_x}{dx} \tag{A.4.5}$$

and then substituting Eqn. (A.4.4) in Eqn. (A.4.5) to get

$$\frac{d^2 v_x}{dx^2} = (R + j\omega L)(G + j\omega C)v_x = \gamma^2 v_x \tag{A.4.6}$$

where

$$\gamma^2 = (R + j\omega L)(G + j\omega C) \tag{A.4.7}$$

Similarly, an equation in terms of i_x can be obtained by first differentiating Eqn. (A.4.4) and then substituting Eqn. (A.4.3) to yield

$$\frac{d^2 i_x}{dx^2} = (R + j\omega L)(G + j\omega C)i_x = \gamma^2 i_x \tag{A.4.8}$$

Equations (A.4.6) and (A.4.8) are the fundamental relationships governing wave propagation along a uniform transmission line.

The symbol γ as defined by Eqn. (A.4.7) is known as the propagation constant, i.e.,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$$

In general, γ is a complex number. The real part of γ gives the reduction in voltage or current along the line. This quantity, when expressed per unit length of the line, is referred to as the attenuation constant α given by

$$\alpha = Re\sqrt{(R + j\omega L)(G + j\omega C)}$$

For a transmission line with no losses, $\alpha = 0$, i.e., a line with no losses has no attenuation. The imaginary part of γ, when expressed per unit length of the line, is known as the phase constant β given by

$$\beta = Im\sqrt{(R + j\omega L)(G + j\omega C)}$$

For a lossless line where $R = G = 0$, the phase constant becomes

$$\beta = \omega\sqrt{(LC)}$$

with dimensions of radians/meter in RMKS units. Phase shift per unit length along the line is a measure of the velocity of propagation of a wave along the line, i.e.,

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{(LC)}} \qquad \text{(A.4.5)}$$

Reference

L.V. Kantorovich and V.I. Krylov, *Approximate Methods of Higher Analysis*, 4th ed. Translated by C.D. Benster. New York, NY: John Wiley, chap. 4, 1959.

APPENDIX E

Miller's Theorem

Miller's theorem is an important theorem which can be used to uncouple nodes in an electric circuit. Consider a circuit configuration with N distinct nodes 1, 2, 3, . . . , N as shown in Figure A.5.1(a). The node voltages can be denoted by V_1, V_2, V_3, . . . , V_N where V_N is zero because N is the reference node. Nodes 1 and 2 are connected by an impedance Z_c. We assume that the ratio V_2/V_1 is known or can be determined by some means. Let us denote this ratio by K which, in general, can be a complex number.

It can be shown that the configuration shown in Figure A.5.1(a) is equivalent to that shown in Figure A.5.1(b) provided Z_1 and Z_2 have certain specific values. These values of Z_1 and Z_2 can be found by equating the currents leaving nodes 1 and 2 in the two configurations. The current I_1 leaving node 1 through the impedance Z_c in configuration (a) is given by

$$I_1 = \frac{(V_1 - V_2)}{Z_c} = V_1 \frac{(1-K)}{Z_c} = \frac{V_1}{Z_c/(1-K)}$$

while the current leaving node 1 through the impedance Z_1 in configuration (b) is given by V_1/Z_1. Therefore, we conclude that

$$Z_1 = \frac{Z_c}{1-K}$$

In a similar manner, the current I_2 leaving the node 2 through the impedance Z_c in configuration (a) is given by

$$I_2 = \frac{V_2 - V_1}{Z_c} = V_2 \frac{1-(1/K)}{Z_c} = \frac{V_2}{Z_c/(1-1/K)}$$

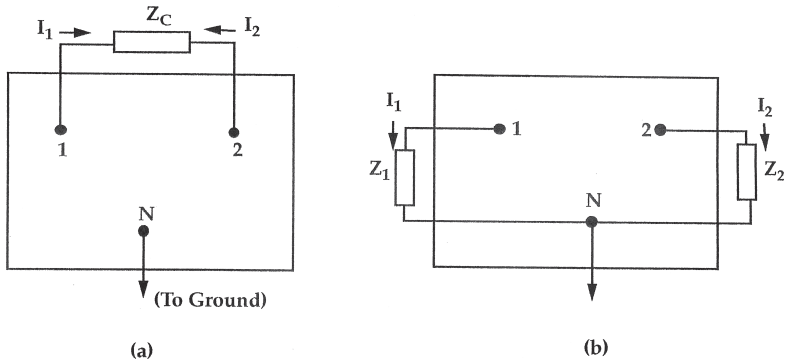

Figure A.5.1 (a) A circuit configuration with N distinct nodes; (b) Circuit configuration equivalent to that shown in Fig. A.5.1(a)

while the current leaving node 2 in configuration (b) is V_2/Z_2. Therefore, the value of the impedance Z_2 should be

$$Z_2 = \frac{Z_c}{1 - \frac{1}{K}} = Z_c \frac{K}{(K-1)}$$

Since the configurations (a) and (b) have identical nodal equations therefore these are identical. However, we note that the Miller's theorem is useful only if the value of the ratio K cab be determined by some independent means.

APPENDIX F

Inverse Laplace Transformation Technique

In several cases, it is more convenient to solve the equations in the frequency domain, i.e., the s-domain and then obtain the time domain solution by an inverse Laplace transformation of the s-domain solution. Various techniques for numerical inverse Laplace transformation are available in the literature. The technique presented here is simple yet efficient and can be easily incorporated in computer programs. It uses the Pade' approximation and does not require the computation of poles and residues [A.6.1, A.6.2].

The inverse Laplace transform of $V(s)$ is given by

$$v(t) = \frac{1}{2\pi jt} \int_{(c-j\infty)}^{(c+j\infty)} V(s)e^{st}ds \tag{A.6.1}$$

The variable t can be removed from e^{st} by the transformation

$$z = st \tag{A.6.2}$$

and then using an approximation for e^z. Substituting Eqn. (A.6.2) in Eqn. (A.6.1), we obtain

$$v(t) = \frac{1}{2\pi jt} \int_{(c'-j\infty)}^{(c'+j\infty)} V(s)e^{z}dz \tag{A.6.3}$$

According to the Pade' approximation, the function e^z can be approximated by a rational function

$$R_{N,M}(z) = \frac{P_N(z)}{Q_M(z)} \tag{A.6.4}$$

where $P_N(z)$ and $Q_M(z)$ are polynomials of order N and M, respectively. Inserting Eqn. (A.6.4) in Eqn. (A.6.3), we obtain

$$\hat{v}(t) = \frac{1}{2\pi j} \int_{(c' - j\infty)}^{(c' + j\infty)} V(z/t) R_{N,M}(z) dz \tag{A.6.5}$$

where $\hat{v}(t)$ is the approximation for $v(t)$. The integral (A.6.5) can be evaluated by using the residue calculus by choosing the path of integration along the infinite arc either to the left or to the right. To ensure that the path along the infinite arc does not contribute to the integral, M and N are chosen such that the function

$$F(z) = V(z/t) R_{N,M}(z) \tag{A.6.6}$$

has at least two more poles than zeros. This gives

$$\int_C F(z) dz = \pm 2\pi j \sum (\textit{residue} \text{ at poles inside the closed path}) \tag{A.6.7}$$

where the positive sign is used when the path C is closed in the left half plane and the negative sign is applied when C is closed in the right half plane. For $N < M$, we have

$$R_{N,M}(z) = \sum_{i=1}^{M} \frac{K_i}{z - z_i} \tag{A.6.8}$$

where z_i are the poles of $R_{N,M}(z)$ and K_i are the corresponding residues. Closing the path of integration around the poles of $R_{N,M}(z)$ in the right half plane, we get the basic inversion formula

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^{M} K_i V(z_i/t) \tag{A.6.9}$$

When M is even, we can write

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^{M'} Re[K_i' V(z_i/t)] \tag{A.6.10}$$

where $M' = M/2$ and $K_i' = 2K_i$. When M is odd, $M' = (M + 1)/2$ and $K_i' = K_i$ for the residue corresponding to the real poles.

To summarize, for a given function $V(s)$ in the s-domain, the response $v(t)$ at any time t can be obtained by the following steps:

a) Select appropriate values of N and M and take values of z_i and K_i' from the computed tables [A.6.1, A.6.2].
b) Divide each z_i by t and substitute (z_i/t) for each s in $V(s)$.
c) Multiply each $V(z_i/t)$ by the corresponding K_i' and add the products.
d) Retain only the real part of the result in step (c) and divide by $(-t)$.

Note that, because of division by t, the value of $v(t)$ at $t = 0$ cannot be calculated by the above procedure. However, this value can be obtained either by using the initial value theorem or an approximate value can be found by selecting a very small initial value of t. The technique described above is suitable for the calculation of the system response to a nonperiodic excitation such as a step or an impulse.

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Dr. Ashok K. Goel retired as an associate professor of electrical engineering at Michigan Tech. in 2014. He received his PhD degree in electrical engineering from the Johns Hopkins University in 1987. His research interests are focused in nanotechnology circuit design, high-speed semiconductor devices, and VLSI interconnections. He was sponsored by the National Science Foundation, Michigan Space Grants Consortium, U.S. Department of Defense, Michigan State Research Excellence Fund, U.S. Army Research Office, U.S. Air Force Office of Scientific Research, and the General Motors Research Laboratory.

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