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SUPERCONDUCTIVE ELECTRONICS

Task Group on Superconductive Electronics

Naval Studies Board

Commission on Physical Sciences,
Mathematics, and Resources

National Research Council

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EXECUTIVE SUMMARY

A. BACKGROUND

The two decades since the invention of the Josephson junction have seen extensive development of superconductive electronics throughout the world. The present annual worldwide expenditure is $30 million to $40 million. The Office of Naval Research (ONR) has been one of five U.S. government agencies sponsoring significant fundamental research and development in the field. The ONR investment has yielded considerable progress in ultrasensitive magnetic sensors, millimeter-wave detectors, and extremely high-speed, analog-to-digital (A/D) converters.

The decision by IBM in September 1983 to terminate its development project to make a superconductive high-speed mainframe computer and change to a research mode has raised questions about the viability and ultimate utility of superconductive electronics technology. The purposes of this Task Group on Superconductive Electronics are to (1) review the accomplishments of the IBM project and the reasons for its termination; (2) evaluate the future viability of superconductive electronics and compare its prospective utility in Navy systems with competing semiconductor technologies; and (3) make recommendations concerning present and future Navy basic and applied programs in superconductive materials, devices, and systems.

The composition of the Task Group is as follows: (1) six persons actively engaged in superconductive electronics, mainly at universities; (2) two persons working in general electronic systems; and (3) three persons engaged in semiconductor devices and systems. About 15 oral presentations were made on Navy systems needs and the status and projections of superconductor and semiconductor technology for meeting these needs. Lengthy discussions were held on extant and needed superconductive device fabrication facilities. In addition, written recommendations were received from ten key persons involved in superconductive electronics.

B. SUMMARY AND RECOMMENDATIONS

The Task Group concluded that it is definitely in the best interests of the Navy and the nation to maintain a vigorous effort in research and development in superconductive electronics. There are numerous Navy applications in which superconductive devices and circuits will give significant performance advantage.

The key characteristics that make superconductors of importance to Navy systems are (1) sensitivity of detection of magnetic and electromagnetic fields (even at millimeter wavelengths) limited only by quantum-mechanical effects, i.e., ultimate sensitivity; (2) nearly lossless transmission lines that can be incorporated into integrated circuits to achieve performance not possible with other electronic circuits; (3) lowest noise levels of any circuit, including both analog and digital types; (4) logic circuits that switch in less time by a factor of 2 than the best semiconductor devices while operating at 2-3 orders of magnitude lower power level; (5) persistent current in superconducting loops for memory applications.

The advantageous Navy systems applications include submarine detection and location, extremely-low-frequency (ELF) underwater communication, millimeter-wave and infrared imaging systems, millimeter-wave broadband communication and radar systems, and signal processors. The advantages accrue through increased sensitivity of passive detectors, greater resolution in imaging systems, receiver front ends with lower minimum detectable signal levels, and signal-processing circuits with greater bandwidths.

In most of these applications, the demonstrations of high performance of the various components (magnetometer sensors, millimeter-wave mixers, local oscillators, amplifiers, A/D converters) have been done at low levels of integration. An exception was the IBM project, where circuits with 1-kbit memory and 1000 logic gates were demonstrated. Also, system interconnections were shown to be satisfactory. (This aspect of the competing GaAs-based systems remains a problem area.) A number of institutions have developed or are developing the capability of making sufficiently large superconductive integrated circuits to permit combinations of smaller circuits in all the enumerated applications in order to achieve greatly enhanced performance. An example would be cryogenic electronic control circuits for magnetometers. Another would be the integration of a complete superconducting receiver--mixer, local oscillator, IF amplifier, and possibly an A/D converter--to achieve ultimate sensitivities.

The Task Group believes that some important applications will require levels of integration not possible with the existing and planned fabrication facilities. This perception is based on testimony given to the Task Group by those responsible for the IBM fabrication facility. One such signal-processing application is the cryogenic millimeter-wave or infrared focal-plane array. It is desired to convert two-dimensional data from a large array of detectors to digital form and process them before conducting them to room-temperature devices. This will require one A/D converter for each picture element as well as a substantial amount of digital logic and memory. Another application requiring a high level of integration is digital signal processing. New and important signal-processing techniques are becoming available through the use of digital circuits, and Navy systems will want to take advantage of this increased flexibility. These are circuit intensive. New capability for the fabrication of the required circuits should be made available in Josephson technology.

In consideration of the IBM decision the Task Group came to the following conclusions. As mentioned above, the IBM project demonstrated the feasibility of fabricating logic chips containing on the order of 1000 gates and a 1-kbit random-access cache memory chip. The IBM goal of a high-performance mainframe computer required a 4-kbit random-access cache memory chip. IBM decided that the additional 1-2 years required to develop this memory chip would put them far enough beyond the original time schedule that the projected advantage of about 2.5 over semiconductor competition (in the same time frame) would not justify their further investment. The Task Group judges that this decision does not indicate a lack of suitability of the technology for Navy special-purpose systems.

The Task Group recommends that, in addition to the continuation and encouragement of the several small ongoing fabrication efforts, one larger tightly disciplined facility be funded. It would be a source of large circuits for both its own laboratory and other U.S. organizations. The cost to establish the fabrication line is estimated to be about $2 million, with space and lithography apparatus provided by the host organization. The IBM experience indicates that a staff of 10-12 persons would be required to maintain and operate the facility, at a cost of $1 million to $1.5 million per year.

It is the opinion of the Task Group that, without this disciplined facility, the circuit technology momentum generated by the IBM project will be lost in the United States to the detriment of Navy and national interests. The Task Group also believes that any delay in funding will lead to a loss of researchers from the field, a reduction of confidence of other organizations supporting research and development in superconductive electronics, a diminution of the value of the $15 million already spent by ONR for this work, and an exacerbation of the lead already held by the Japanese in large superconductive circuits.

I. INTRODUCTION

The aim of this Task Group, as described in the Terms of Reference, given in Appendix A, is to evaluate the state of superconductive electronics and its potential in comparison with competing technologies in order to guide future Navy funding. The study was precipitated by IBM's decision to terminate its effort to develop an ultra-fast mainframe computer based on the Josephson junction. We will comment here on the reasons for the IBM decision, as well as transitions of projects in two other industrial laboratories. This is followed by a survey of the present activity in superconductive electronics in the United States, Japan, and Europe.

A. IBM

IBM decided in September 1983 to terminate its effort to develop a superconducting mainframe computer. The bases of the decision were (1) some significant technological hurdles and (2) an assessment of the future competitive potential of semiconductor technology in the late 1980s. (It should be noted that small-scale applications of Josephson technology--magnetometers and A/D converters, for example--were never among the goals of the IBM project.)

IBM had demonstrated successful operation of all the required logic circuits, power supply and regulation circuits, a packaging concept, and the essential performance of a 1-kbit cache memory. IBM established the necessary process steps to produce logic chips at an acceptable yield. The specific hurdle that they confronted on the way to producing a demonstration full-scale system was the development of a 4-K cache memory chip with appropriate yield and performance. IBM judged that this would cause a 1-2 year delay in the original schedule. They projected the development of semiconductor technologies as well as improvements in Josephson technology and estimated that the original factor of 5-6 performance advantage of a Josephson-based system would shrink to about 2.5 at the delayed time. This margin was insufficient for IBM to continue the large investment, so they chose not to develop the 4-K cache memory chip and terminated the mainframe computer development project.

B. SPERRY RESEARCH CENTER AND BELL LABORATORIES

In 1983 two other significant events occurred in industrial work on superconductive electronics. Sperry management decided to close its entire corporate research center in Sudbury, Massachusetts, and decentralize all projects to operating divisions. The superconductor group was asked to move to Minnesota, but individuals involved declined for personal reasons. The existing Josephson effort at the Sperry Corporate Technology Center (in Minnesota) inherited the mission, equipment, and technology developed at the Sudbury Research Center.

The work at Bell Laboratories had been done by a few small groups. Apparently the change in AT&T corporate structure led to a termination of projects aimed at superconductive integrated circuits, which were not perceived to lead to AT&T future products. A small research project on tunnel junction technology remains.

C. STATUS OF SUPERCONDUCTIVE ELECTRONICS

1. United States

The ten industrial laboratories engaged in research and development on superconductive electronics are AT&T Bell Laboratories, CDC, Hughes, HYPRES, IBM, Quantum Design, S.H.E. Corporation, Sperry, TRW, and Westinghouse. The total number of full-time equivalent (FTE) professionals is about 60. The IBM effort is now directed toward devising a new cryogenic millivolt transistor, the Bell work is concerned with junction technology, the present task at HYPRES is a high-speed sampler, and the remaining groups are working on or toward signal-processing applications.

Six government laboratories are involved in superconductive studies. These are the National Bureau of Standards (NBS) at Boulder and Gaithersburg; Naval Research Laboratory (NRL); Naval Surface Weapons Center (NSWC), White Oak; Naval Coastal Systems Center (NCSC), Panama City; and Laboratory for Physical Sciences, College Park, Maryland, with a total of about 20 FTE professionals.

In addition, there are several university groups working on or toward superconductive small-scale integration (SSI) or medium-scale integration (MSI) circuits: University of California, Berkeley, the Universities of Wisconsin and Utah, and MIT/Lincoln Laboratories. Materials and device studies and work on analog applications involving small circuits are in progress at the following universities: Stanford, California at Berkeley, Arizona, Minnesota, Louisiana, Vanderbilt, NYU, Columbia (Goddard), Yale, SUNY at Stony Brook and Buffalo, Case Western, Cornell, Virginia, Maryland, and Rochester, with an FTE of about 60 including graduate students.

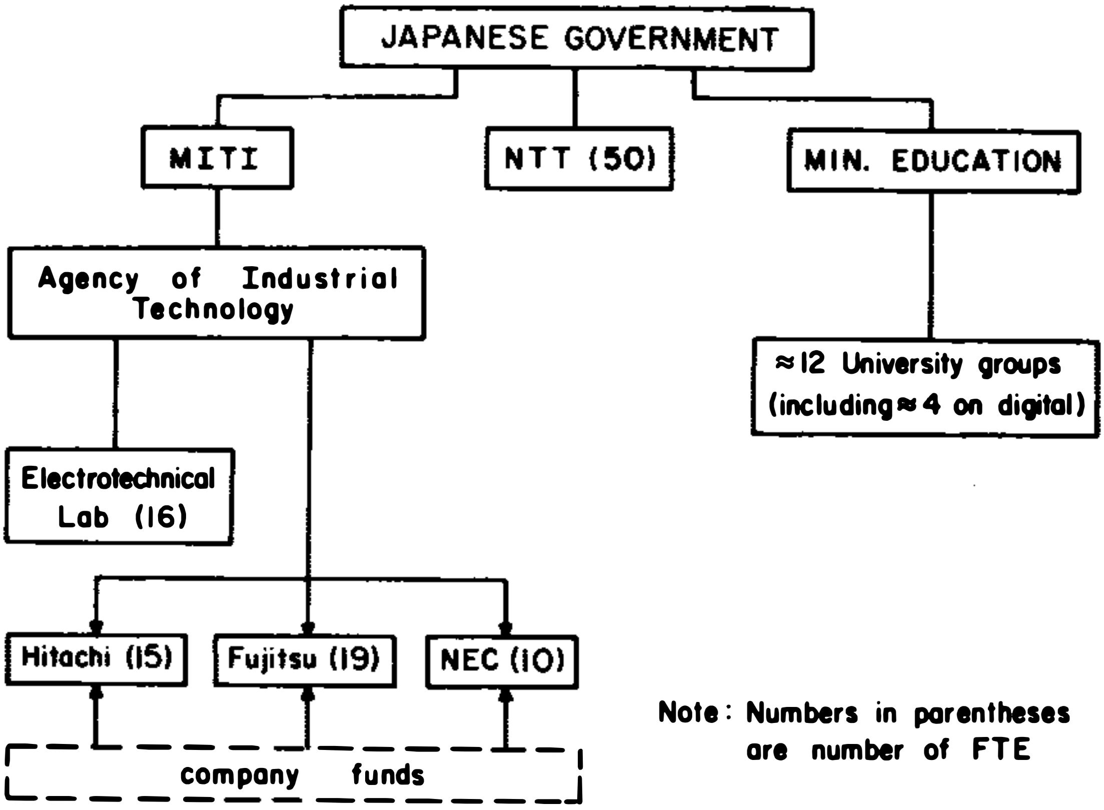

FIGURE 1 Funding of the Japanese effort in superconductive electronics.

The total effort in the United States is about 140 FTE professionals and graduate students.

2. Japan

The support structure for superconductive electronics in Japan is shown in Figure 1. The MITI-supported work is a part of the so-called "supercomputer" project. The Electrotechnical Laboratory (ETL) has the monitoring function as well as conducting research of its own. The industrial groups are supported significantly by company funds as well as by MITI. The MITI support for the eight-year project period, 1982-1990, is reported to be $100 million to $150 million. High Electron Mobility Transistor (HEMT) and Josephson technologies are to be compared until 1986, and a machine is to be demonstrated by 1990 with the chosen technology. The NTT project is aimed toward digital signal processing. The total industrial effort (including ETL) in Japan involves nearly 100 FTE professionals. They have devised several logic families, set new records for logic circuit speed, developed both Pb-alloy and Nb-based fabrication technologies, and demonstrated LSI logic and memory circuits. Their projects dwarf in accomplishments those of the industrial groups (outside of IBM) in the United States. There has been some shift of attention and considerable concern in Japan about the IBM decision, but there is no plan to reduce the projects.

There are efforts in at least two other government laboratories directed toward millimeter-wave receivers.

About 12 university groups are supported by the Ministry of Education. Of these, about four are working on various types of digital circuits, with the rest on device physics, materials, superconductive quantum interference devices (SQUIDs), and millimeter-wave detection. Most of the student participation is through undergraduate thesis projects. It is reasonable to take the FTE for universities at about 60 including professors, research associates, and students.

The total effort in Japan on superconductive electronics is about 170 FTE professionals, about 20 percent larger than the U.S. effort.

3. Western Europe

The work in Western Europe is carried out by 3 small industrial groups, 7 national laboratories, and about 20 university groups. It is estimated that there are about 100 FTE professionals. Their work includes device physics, circuit modeling, SQUIDs, magnetometers, voltage standards, millimeter-wave detection and mixing, and digital circuits. The emphasis is strongly directed toward analog applications.

4. Eastern Bloc

It is known that there are groups in Moscow, Karkhov, Kiev, Jena, Warsaw, and Sophia, but the relation of work reported in publications to work in progress is uncertain so that no accurate estimates of activity can be made.

5. Summary

It is estimated that the total worldwide effort in superconductive electronics is about 450 full-time equivalent researchers with an annual expenditure of $30 million to $40 million.

II. STATUS OF SUBSYSTEM APPLICATIONS OF SUPERCONDUCTIVE ELECTRONICS

In this section the current state of development of a number of areas of application of superconductive electronics is reviewed: magnetometry for submarine detection and localization, extremely-low-frequency underwater communications, millimeter-wave receiver front ends, analog signal processing, and digital logic and memory.

The important properties of superconductive devices that come to play in these applications are nearly zero electrical loss and dispersion in superconductive transmission lines, low noise, extremely high switching speeds of Josephson junctions, unmatched nonlinearity of the current-voltage (I-V) characteristics of the superconductor-insulator-superconductor (SIS) tunnel junction, interferometer-like behavior of superconductive loops containing Josephson junctions (SQUIDs), and persistent currents in superconductive loops. Some of these properties are superior quantitatively to semiconductor devices, and others have no counterpart outside superconductivity. At the system or subsystem level all tasks can be and have been done using other technologies so the comparisons are quantitative. The superconductive technology has clear advantages in a number of areas, as seen below; but, as complexity increases, so do the number of uncertainties and therefore the difficulty of assessing the comparisons of competing technologies as one projects future performance.

A. MAGNETOMETERS AND THEIR APPLICATIONS

SQUID magnetometers and gradiometers are examples of definite success in the development of Josephson technology. Reliable SQUID sensors have been commercially available for a number of years. They offer magnetic field sensitivity, and voltage and current sensitivity (at low input impedance), 1000 times better than that realized by existing nonsuperconductive sensors. Recent development efforts on the DC SQUID, the more advanced version of the SQUID sensor, has brought the sensitivity level in carefully designed sensors very close to the quantum noise limit. This performance is more than a factor of 100 below the energy sensitivity of commercial SQUIDs. This improvement was made possible by the availability of advanced microfabrication technology and the recent development of an improved Josephson tunnel junction fabrication process.

Realization of this performance advantage in practical systems requires attention to two problems. Much of the remaining research concern in SQUID sensors focuses on the low-frequency 1/f noise problem, in both the tunnel junction and the SQUID sensor. Recent progress suggests that the 1/f noise problem can be understood and significantly reduced. Recent work in producing practical SQUID systems with efficient thin-film input coils has been impressive.

B. MILLIMETER-WAVE DEVICES

Superconductive technology can provide voltage-tunable sources, low-noise, wide-bandwidth mixers and detectors, and amplifiers for use in the microwave and millimeter-wave frequency regions. For frequencies below about 30 GHz, GaAs technology (Schottky diodes and GaAs FET amplifiers) are extremely good, are improving with time, and have the potential to satisfy most anticipated systems needs in the foreseeable future. However, the performance of GaAs devices degrades with frequency. At higher frequencies superconductive devices can make a valuable contributions to naval communications and surveillance systems.

1. Mixers and Detectors

The extremely sharp nonlinearity of the current-versus-voltage characteristic of an SIS tunnel junction makes possible mixers and detectors with quantum-noise-limited performance at 36 GHz and higher frequencies. In this range their performance is superior to all known competing technologies. (See Figure 2 for a comparison of receiver noise temperatures.) However, since these devices require very low local oscillator power levels, their dynamic ranges are limited. The use of a series array of SIS devices is being evaluated as a means to raise the dynamic range up to a value of about 40 to 50 dB, which would be acceptable for most operational systems.

2. Low-Noise Amplifiers

A low-noise mixer and/or detector must be followed by a low-noise amplifier in order to realize low-noise operation for a receiver front end. The nonlinear-inductance behavior of Josephson junctions can be used in parametric amplifiers to provide such a function. For example, a SQUID paramp operating at 9 GHz has exhibited noise temperatures below 10 K with 17-dB gain and projected bandwidths of 1 GHz. Experimentally, bandwidths of 250 MHz have been observed in circuits whose parameters have not

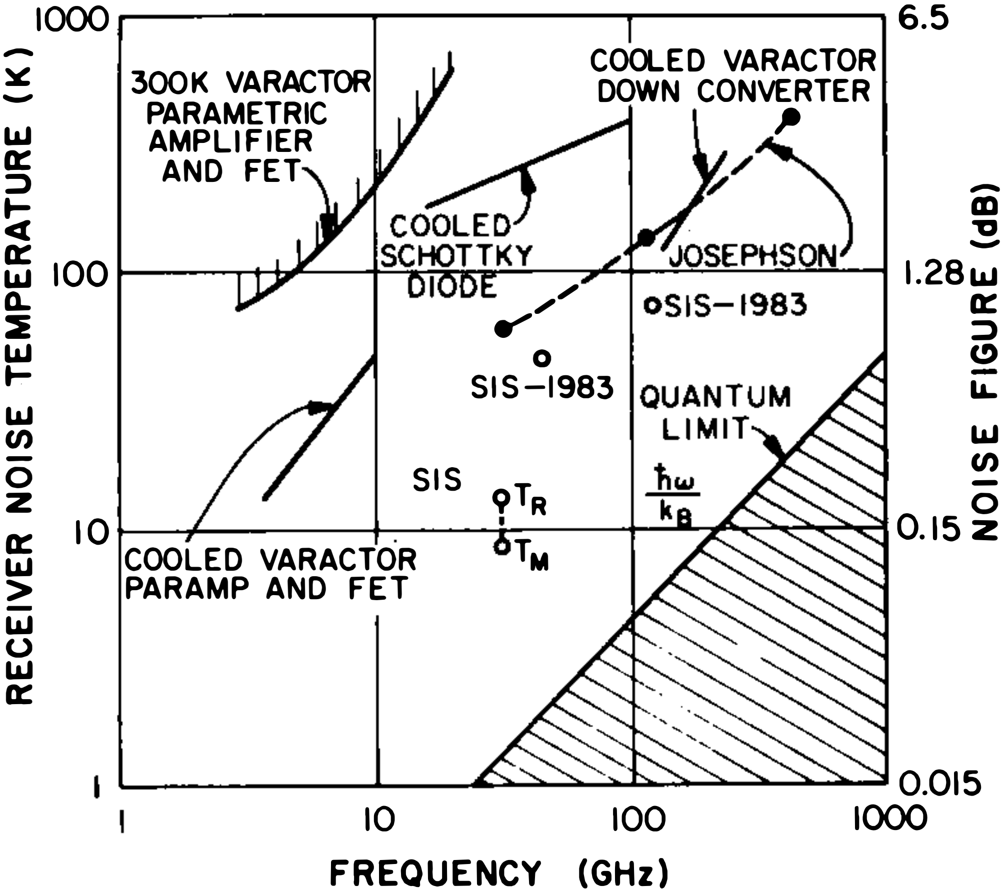

FIGURE 2 Single-sideband receiver noise temperatures and noise figures comparisons assume use of an IF amplifier with 15-K noise temperatures.

as yet been optimized. State-of-the-art GaAs amplifiers at 9 GHz have noise temperatures of about 60 K. Analysis indicates that this paramp can be scaled, without noticeable degradation of noise characteristics, to 94 GHz, where it could be employed as a wide-bandwidth preamplifier in front of the mixer elements if desired.

Another type of low-noise, wide-bandwidth amplifier has recently been demonstrated in which the circuit parameters of a DC-type SQUID magnetometer were optimized for small-signal, high-frequency operation. Noise temperatures as low as 1 K were realized up to 100 MHz. Recent theoretical work indicates that this type of amplifier, used with tuned input and output, as it would be for an IF amplifier, will give a power gain of 43 dB at 1.5 GHz. In comparing noise temperatures with other technologies, the best other amplifier at frequencies below 1.5 GHz uses a GaAs FET and has a noise temperature of 50 K at room temperature and below ~10 K when cooled to 4.2 K.

3. Passive Circuit Elements

At microwave and millimeter frequencies the surface resistance of a superconductor is finite but much smaller than that of a normal metal conductor. Therefore, passive circuit elements, such as antenna structures, transmission interconnect lines, resonant filters and couplers, can be fabricated that will have much lower attenuation factors and, in addition, exhibit near-zero dispersion characteristics. (These properties persist until the signal frequency becomes comparable with the frequency corresponding to the energy gap of the superconductor, normally about 1 THz or above.) If used alone, such passive circuit elements may not justify refrigeration but used in fabricating a monolithic integrated circuit containing mixers or IF amplifiers, for example, superconductive passive circuit elements may make a major contribution toward demonstrating the feasibility of superconductive receiver front ends in naval operational systems.

4. Voltage-Tunable Sources

If a voltage is applied to a Josephson device, an alternating current will flow through the device and, if it is embedded in a suitable circuit, energy will be transferred into the external circuit. The ratio of the applied voltage to the frequency of the radiation is h/2e, where h is Planck's constant and e is the electronic charge; this corresponds to approximately 0.5 GHz per μV. Pioneering work under ONR funding at the State University of New York-Stony Brook has demonstrated the feasibility of such a tunable source from 1 to 18 GHz. Phase-locking experiments on arrays of junctions indicate that the use of several hundred junctions in series can produce radiated power in the microwatt range. Such devices could be used as frequency-agile sources for spread-spectrum applications or as the local oscillator for a front-end subsystem in a microwave or millimeter-wave receiver.

5. Monolithic Millimeter-Wave Integrated Circuits

Since all the above components can be fabricated in compatible thin-film metallization format, they could be used to prepare monolithic circuits. Such circuits would be low cost, reliable, reproducible, and constitute a small heat load on a cryogenic subsystem.

C. ANALOG SIGNAL PROCESSORS

Work has been done on two types of analog signal-processing devices that takes advantage of their extremely wide bandwidth and low-loss properties of superconductive transmission lines. The devices are conceptually similar to the elements such as optical and surface acoustic-wave devices but with orders of magnitude greater bandwidth.

1. Transversal Filters

Miniature superconductive transmission lines are particularly well suited for transversal filters because signals with time-bandwidth products of 1000 and bandwidths of 10 GHz can be contained in compact structures that include several thousand taps with accurate phase and amplitude characteristics. Devices have been demonstrated successfully, and prototypes for system applications can be realized as early as fiscal year 1985.

2. Correlators

There are three kinds of correlators for situations where the arrival time of the signal is known only approximately and where a changing code is employed. One device that provides this function correlates a time-reversed segment of a continuously changing reference code with the incoming signal. Such devices are called convolvers. Systems where the code is changed periodically and where the arrival time of the signal is not known--as in radar and in IFF systems--require devices where successive references are stored and the incoming signal is convolved with the stored reference. These devices are called memory correlators. In both devices each reference element is multiplied at a tap with the signal, and the output of all the taps are summed simultaneously. A third version multiplies a reference directly with the incoming signal in a mixer and the output of the mixer is integrated in time to form the desired correlation. However, because the arrival time of the signal at the mixer is not known precisely, hundreds of mixers are needed, each fed with an incrementally delayed reference. After the integration interval is completed, the output of each mixer is sequentially read out. These time-integrating correlators are used in wideband emitter-location systems and in spread-spectrum communication systems requiring signal-processing gains in excess of 10^4 for low-probability-of-intercept (LPI) communications.

MIT Lincoln Laboratory has been exploring the feasibility of superconductive convolvers during the past two years. The structure consists of a transmission line that is periodically tapped. A bridge circuit of SIS mixers is located at each tap. The signal is entered at one end of the transmission line and the time-reversed reference at the other end. These incrementally delayed versions of signal and reference appear at each tap, where they are multiplied. The product signals are fed directly into a transmission line, and the combined sum of all mixers appears at the output terminal. A demonstration device with a bandwidth of 2.3 GHz and with 50 taps has been fabricated and evaluated. The device performs close to theoretical expectations, and a prototype device with the same bandwidth and a time-bandwidth product of 100 is under development. It is expected to be realized by the end of fiscal year 1984. Work has also begun at the same laboratory toward the realization of a time-integrating correlator. The device is to utilize the transmission line, tap, and mixer designs of the convolver together with resonator-integrators, Josephson junction comparators, and shift registers. The comparators and shift registers are currently under development, and the first demonstration device is expected in fiscal year 1986.

D. ANALOG-TO-DIGITAL CONVERTERS

An important device in signal-processing systems is the analog-to-digital (A/D) converter. The ever-increasing demands of radar and communication systems put a premium on an A/D technology with especially broad bandwidth. Achievements of initial experimentation on A/D devices employing Josephson technology indicate advantages over existing semiconductor devices. Predictions for A/D converters based on the HEMT device suggest performance comparable with the expectations for Josephson-based converters, but with orders of magnitude greater power dissipation. In addition, there are applications for which the low input level (≈ 2 mV full scale) of the superconducting device and/or its exceptionally low power dissipation essentially eliminates competition. Key examples are focal-plane quantizers and devices to digitize the outputs of superconducting amplifiers and millimeter-wave mixers.

There are two fast types of A/D converter, the flash type and the counting type. Work is in progress on both using Josephson technology. Flash-type converters in semiconductor technology require one input comparator circuit for each digital level, that is, $2^N - 1$ for an N-bit converter. As a result of the periodic interferometric property of SQUID circuits, only one comparator is required for each bit in Josephson technology. Circuits have been developed to provide the small aperture time handled in semiconductor technology by a sample-and-hold circuit. Initial experiments have given results of 3-4 bits of resolution for an analog signal bandwidth of 140 MHz and 3 bits of resolution for a 450 MHz analog signal. This is comparable with the best laboratory results for GaAs converters, and the power is orders of magnitude lower. In the counter-type converter, the analog signal creates a series of pulses that are counted in a binary countdown circuit. A counter for 4 bits was operated with evidence of satisfactory counting at 117 GHz. This type of A/D offers the possibility of a very large dynamic range at lower speeds. A 12-bit counter has been demonstrated to date.

E. DIGITAL LOGIC AND MEMORY

Over the past decade, a number of different Josephson logic families have been developed in the laboratories of IBM, other U.S. institutions, and in the Japanese NTT and MITI projects. Less effort has gone into the development of memories; however, in addition to the IBM work, memory cells and systems have been studied at NTT and the Electrotechnical Laboratory in Japan.

The work on logic has led to demonstrations of increasingly fast circuits. Families based on interferometers (SQUIDs) and others consisting of Josephson junctions and resistors have been demonstrated. Recently, a circuit in 1.5-μm technology with single fanout was shown to have a delay of 5.6 ps per gate. Such speeds are approximately a factor of 2 faster than the best speeds of logic gates using the HEMT based on GaAs, with 2-3 orders of magnitude lower power dissipation.

A number of circuits having a fairly large gate count have been demonstrated, including a 500-element programmed-logic array, an 8-bit ripple carry adder, a 4-bit full adder, and an 8 x 12-bit parallel multiplier.

The Task Group also discussed the results of computer studies of the effect of miniaturization. It appears that there is considerable advantage in scaling the logic families to smaller feature sizes down to about 0.5 μm. It appears that a factor of nearly 5 decrease in the average gate delay for either interferometer-type or resistor-junction-type logic families can be achieved by scaling minimum-feature sizes from 2.5 μm down to 0.5 μm. The same scaling would also increase circuit density by an order of magnitude.

In addition to logic, high-speed processors require short-access-time random-access memories (RAMs). The IBM

1-kbit Josephson RAM was nearly functional before the termination of the project. Had it been completed, it would have had a subnanosecond access time with a power dissipation of less than 2 mW including power regulation. Fujitsu reported in early 1984 a HEMT cryogenic (77 K) 1-kbit RAM with 0.9-ns access time that dissipates 360 mW. It is expected that RAM access times in the two technologies will be comparable [the GaAs FET technology (non-HEMT) is probably not in the running]. The on-chip difference will lie in power dissipation.

High-speed logic and memory must be incorporated in multichip systems; important differences could arise as this part of the effort is developed. In the case of GaAs FETs and HEMT, the translation of on-chip performance to multichip systems has yet to be demonstrated and has been acknowledged to be a problem area. On the other hand, a preliminary system-level demonstration has been made to verify the systems aspects of Josephson technology.

From what is now known about the Josephson technology, it is reasonable to expect that small to medium-size digital processors incorporating 1-kbit RAM chips could be built within 3-5 years. There are many high-performance applications that require small systems such as A/D converters, data multiplexers, digital correlators, small memories, and simple data-reduction preprocessors. For such systems, which have a small chip count, the performance features of high device speed and high system speed, coupled with low power, offer important advantages. In some cases these systems would be used to interface with already cryogenic sensors and would allow considerable reduction of data for subsequent transfer to room-temperature electronics.

III. STATUS OF FABRICATION AND DEVICE TECHNOLOGY

A. TUNNEL JUNCTIONS AND INTEGRATED CIRCUITS

Josephson junction fabrication technology for analog and digital applications centers on tunnel junctions fabricated from the higher transition temperature superconductors, Pb and its alloys, and Nb and its alloys. Early large-scale work concentrated on Pb-alloy oxide junction technology because of the relative ease of making high-quality junctions in this system. Principal drawbacks of this soft metallurgy system are the tendency for junctions to short after thermal cycling and the long-term instability of junction characteristics. Considerable effort at IBM on developing Pb-alloy electrode materials resulted in orders of magnitude improvement in cyclability; however, stability to the degree required for computer technology remained a problem. The development of high-quality Nb/Nb-oxide/Pb-alloy junction fabrication techniques solved both the stability and cyclability problems. The higher dielectric constant of the Nb oxide meant that smaller junction areas were necessary to maintain speed. Junctions grown on film edges eased the lithographic control requirements for the required small areas. In 1981 IBM switched its main development effort from the planar Pb-alloy junctions to Nb-edge junctions and chose this technology for its development line. By mid-1983 IBM had demonstrated the ability to fabricate 12-mask-level integrated circuits (ICs) with roughly ±10-15 percent control of Josephson critical currents in arrays of 1000-2000 interferometers per quarter-inch chip.

While IBM was concentrating its development efforts on demonstrating the manufacturability of the Nb/Pb-alloy edge junction technology, research at IBM and other laboratories resulted in the demonstration of several techniques for making acceptable quality all-Nb tunnel junctions. Principally, these involved either barriers of deposited amorphous silicon, Al oxidized to Al_2O_3, or an interfacial Au layer over the native Nb oxide prior to deposition of the Nb counterelectrode. Among these, the Sperry Selective Niobium Anodization Process (SNAP) employing Si barriers was developed furthest, to 10 gates per chip densities with a five-mask-level process. This process (and offshoots) starts with the fabrication of a single junction over the entire wafer. Only after the junction has been completed is the wafer exposed to any of the processing steps (such as etching and photoresist deposition and removal, etc.) which, during the conventional window-junction technology, may adversely affect the junction quality and uniformity. This may lead to uniformity advantages and rather inexpensive elimination of wafers having unfavorable current densities.

The Electrotechnical Laboratory in Japan has developed an IC process employing NbN ($T_C \sim 17$ K) junctions, and a number of other institutions are making junctions with NbN-base electrodes. Recent experiments have resulted in the demonstration of a CVD process for tunnel barriers on NbN.

Table 1 shows the existing and developing Josephson IC fabrication facilities in the United States. None of these are expected to become capable of making chips with hundreds of gates (interferometers) with viable yield.

B. NONHYSTERETIC JUNCTIONS

Some analog applications of Josephson junctions require nonhysteretic I-V characteristics. This can be obtained by resistively shunting tunnel junctions, but at the expense of reducing the device I_CR product and hence the performance of the device. This degradation can be minimized by use of high-current-density, submicrometer-area junctions.

As an alternative approach, junctions can be produced with semimetal or degenerate-semiconductor barriers. This approach can yield high I_CR products with nonhysteretic current-voltage characteristics. For most applications metal bridge junctions do not offer good performance owing to the fabrication requirement (~1000 Å bridge dimensions) and low impedance ($R \simeq 1$ ohm). Exceptions to the negative view on metal contacts is the high-temperature SNS device, which has been used to demonstrate SQUID behavior up to 16 K and granular NbN weak links. Another is the need for junctions with controlled and reduced I_CR and R to be used in series arrays for tunable millimeter-wave oscillators.

C. SUPERCONDUCTIVE TRANSISTOR

Although the applications discussed in section II successfully employ circuits with Josephson junctions, the two-terminal nature of the device and concomitant difficulty of input-output isolation and low circuit gain have made difficult the exploitation of its extremely high switching speed. Transformer coupling using interferometers has provided a kind of three-terminal operation, but at the expense of increased size and reduced performance. Circuits have also been developed using combinations of junctions and resistors in which isolation is achieved using the high resistance of a switched junction. Several

TABLE 1 Superconductive circuit fabrication facilities.

Laboratory	Existing Process	Process under Development	Circuit Complexity	Facility Resources	Personnel*		Comments
					Group Total	Fabrication	
AT&T Bell Labs (Murray Hill)	Nb-Al$_2$O$_3$-Nb (SNEP)		Single junctions (2 mask levels)		2	1	Materials and physics emphasis
Cornell University	Nb-Nb$_2$O$_5$-Pb	NbN-Al$_2$O$_3$-Nb	10s of junctions	$0.6M plus use of NRRF on submicrometer devices	6	3	Basic physics
Hughes (Carlsbad)		NbN-NbN (SNAP-like) planned	Planning 100 gates with 8 mask levels	$0.5M plus access to lithography	4 (planning 5	2)	Signal processing applications
HYPRES	Two Nb-x-Nb processes (one SNAP-like)		100s of junctions 4 logic gates 5 mask levels	$0.6M	11	5	HYPRES created August 1983; instrument product requires 4 gates; plan to develop 4-kbit cache memory
IBM (Yorktown Heights)	Nb-Nb$_2$O$_5$-Pb		Series arrays of 1000s of junctions 10s of gates 5 mask levels	$1.5M including lithography	20	9	Emphasis on basic device and materials research and scientific applications
MIT Lincoln Laboratory	Nb-Nb$_2$O$_5$-Pb		Junction arrays (24 elements with 16 junctions/element)	$1M dedicated plus access to $5M process and test equipment	13	8	Emphasis on analog signal processing

TABLE 1 *Continued*

Laboratory	Existing Process	Process under Development	Circuit Complexity	Facility Resources	Personnel*		Comments
					Group Total	Fabrication	
National Bureau of Standards (Boulder)	Pb-PbO-Pb	$Nb-Nb_2O_5-Pb$	Series arrays	\$0.7M plus dedicated optical and electron-beam lithography	11	6	Teaching and fabrication for a number of university and industry workers included
Sperry Corp. Tech. Center (St. Paul)	Nb-αSi-Nb (SNAP)	Nb-Ge-Nb planned 1985	20-junction arrays planning 7 mask-level capability 1985	\$1.5M dedicated plus access to lithography	17 (planning 29 for 1984)	6 12	Magnetometry, and millimeter-wave application (eventually digital)
State Univ. of NY (Stony Brook)	$Nb-Nb_2O_5-Pb$	Planning $Nb-Al_2O_3-Nb$	100-junction arrays 3 mask levels planning 1000-junction arrays	\$1M dedicated	5	3	Basic physics applications and millimeter-wave generator
TRW (Redondo Beach, CA)	$Nb-Nb_2O_5-Pb$	Planning Nb-x-Nb for 1985	100-junction arrays 6 gates 7 mask levels	\$0.5M	7	3	millimeter-wave and signal-processing applications
Univ. of California (Berkeley) EECS Dept.	Pb-PbO-Pb	Nb-αSi-Nb (SNAP)	32 gates 8 mask levels	\$0.4M dedicated incorporated in UCB microfabrication facility	9	4	Signal processing
Physics Dept	$Nb-Nb_2O_5-Pb$		Several SQUIDs	\$0.15M plus access to UCB microfabrication facility	4	4	Magnetometry

TABLE 1 *Continued*

Laboratory	Existing Process	Process under Development	Circuit Complexity	Facility Resources	Personnel*		Comments
					Group Total	Fabrication	
Univ. of Utah	Nb-Al_2O_3-Nb		10s of junctions	$0.15M plus access to lithography	2	2	Signal processing
Univ. of Wisconsin	Nb-Nb_2O_5-Pb	NbN-O_x-NbN Nb_3Sn-O_x-Pb	10s of junctions	$0.5M plus access to IC lithography	8	5	Junction fabrication and physics
Westinghouse (Pittsburgh)	Nb-Al_2O_3-Nb		100 junctions 5 mask levels	$5M dedicated including lithography	5	2	Materials and analysis support for high-T films (5 people)

*These numbers include persons with other responsibilities, for example, graduate students. Number of persons listed as in fabrication devote just part of their time to fabrication in most cases.

such families are being used in Japan to make medium-size circuits such as a 4-bit full adder (at NEC). The latching nature of the device also leads to the requirement of an AC power supply.

It is clear that the discovery of a device with transistor-like properties that could maintain the speed and low-power advantages of the Josephson device would be much easier to exploit for large system-level performance advantages. At present there is no suitable semiconductor transistor for high-speed, high-density circuit applications at superconducting temperatures. FETs can be made to work at these temperatures, but the power level of conventional ones is prohibitively high. Superconductive devices based on gap suppression (CLINKs, Quiterons) are fundamentally limited in performance by inelastic scattering to times of $\approx$50 ps and by the nature of the nonequilibrium effects operation, which will cause latching. Other physical principles that might be exploited for devices (e.g., superconductive hot-electron transistors or voltage-controlled tunneling devices) have not yet been developed to the point where power gain has been demonstrated.

IV. REFRIGERATION

A stable cryogenic environment is crucial for superconductive electronic system applications. A suitable cryogenic enclosure can be provided either by an open-cycle container (dewar) or by a closed-cycle refrigeration system. The choice of a cryogenic subsystem is determined by a number of factors: operating temperature, temperature stability, cooling capacity, integration with the electronic package without degradation of system performance, weight, size, or power limitations.

A. DEWAR SYSTEMS

Dewars designed for cooling of specific systems can be built with boiloff rates as low as 0.3 liter per day, which corresponds to a total heat leak into the helium reservoir of 10 mW. Heat dissipated by the electronic package and heat conduction down the I/O lines is added to this value to define the boiloff rate of the integrated system. Because the dewar has no moving parts, it can be highly reliable and produce negligible interference signals that might degrade system performance. The primary disadvantage is that helium must be periodically replenished. In some applications another disadvantage is that the vented helium gas must be removed from the environs of the dewar system in order to prevent an ambient pressure buildup.

B. CLOSED-CYCLE REFRIGERATION SYSTEMS

In a number of systems where dewar operation is not feasible, closed-cycle refrigeration is required. Closed-cycle refrigerators for 4 K have been built that can provide cooling capacities ranging from milliwatts up to 1000 W. An approximate value for the efficiency of such 4 K coolers is 10^{-3}. The disadvantages are limited reliability (associated with moving parts including sliding seals and contamination of the working fluid with condensable materials) and introduction of interfering signals generated by the refrigerator (electrical, magnetic, or mechanical, for example) which may degrade electronic system performance.

At present there are a number of ongoing programs to develop reliable systems (MTBF of the order of 6 months or more) with fractional-watt cooling capacities at temperatures below 10 K that will exhibit minimal interference signals. Such refrigeration systems suitable for many of the anticipated superconductive electronic applications will be available in the near future.

V. NAVY SYSTEM OPPORTUNITIES WITH SUPERCONDUCTIVE ELECTRONICS

In the judgment of the Task Group there are several types of Navy systems that could achieve significant performance advantages by using superconductive electronics. Figure 3 is a generalized system block diagram for an electronics system for radar, communications, or electronics countermeasures (ECM) applications. Functions toward the left of the diagram (system input end) are the most appropriate for superconductive technology because of the increased premium for low noise and wide bandwidth. Elements near the output end can be implemented with more conventional technology because of increased signal levels and lower speeds; there, greater parallelism and system complexity can be used than in elements near the input end.

Among the superconductive devices that have been demonstrated are magnetometers, mixers and detectors, amplifiers, oscillators, analog signal processors, analog-to-digital converters, and digital logic and memory. The primary advantages of these superconductive devices are quantum-limited sensitivities, lower noises, higher analog speeds and bandwidths, higher switching speeds, and lower power dissipation. In this section we describe applications where the performance advantages over room-temperature devices outweigh the disadvantage of the required refrigeration.

A. MAGNETIC ANOMALY DETECTION AND ELF COMMUNICATIONS

The Navy has a requirement for Magnetic Anomaly Detection (MAD) both for antisubmarine warfare (ASW) and antimine warfare (AMW). The Naval Coastal Systems Center (NCSC) is developing an airborne MAD system employing superconductive magnetic sensors that will provide real-time target acquisition and tracking capabilities. This could profoundly improve ASW capabilities of the fleet.

A number of serious problems that have been identified from the flight test and subsequent measurements indicate the need for a coordinated research and development effort to improve the SQUID sensors and their superconductive components. The areas that need particular attention are those associated with thermal pressure and mechanical sensitivity of the SQUID and flux transformer assembly. Research programs that should effectively deal with these problems have been initiated by NAVAIR.

There is an urgent requirement within the fleet to communicate with its submarines on station. One approach is an ELF (30-130 Hz) communications system. The existing receiving antennas are extremely long (more than 300 m in

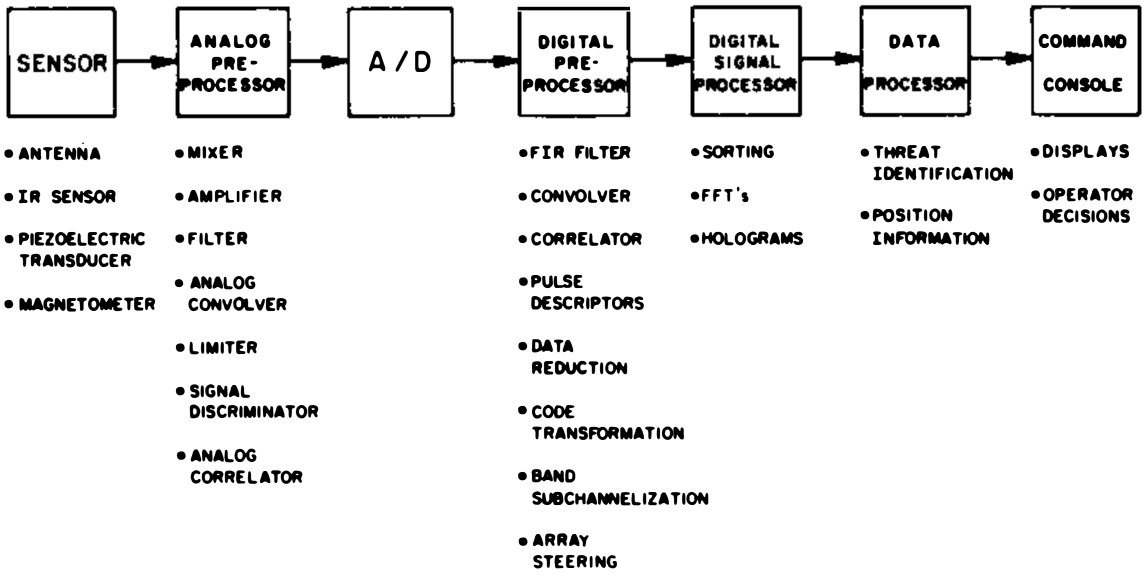

FIGURE 3 Generalized system block diagram for radar, communications, or electric countermeasures.

length) and have highly directional antenna patterns that impose stringent constraints on the maneuverability of the submarine. A SQUID-based ELF antenna for receiving these signals has been built and its performance demonstrated in stationary testing both at the surface and depths of 100 m. However, towing testing has not been performed. The availability of a SQUID system with improved dynamic range would ease the platform stability requirements for such an antenna system. A digital SQUID system employing the intrinsic quantized response of a Josephson interferometer or Josephson A/D convertors immediately behind a conventional analog SQUID sensor on the same chip in the dewar system would be useful for this application as well as for a variety of other applications.

B. RADAR AND COMMUNICATIONS SYSTEMS

Superconductive devices offer a number of opportunities for significantly improved performance of a variety of radar and communications systems through increased receiver sensitivity and bandwidth. The payoff for Navy systems of enhanced receiver sensitivity comes through lower transmitter power requirements at millimeter-wave frequencies where both sensitivity and transmitter power are hard to obtain. The advantage of large bandwidth is high information data rate. It appears possible to combine superconductive devices into a single cryogenic package to give the advantages of both high sensitivity and data rate.

1. Receiver Sensitivity

It was shown in section II, B, that the superconductor-insulator-superconductor (SIS) tunnel junction is by far the best mixer available and the only one that can give wide bandwidths with receiver noise temperatures below the ambient value at millimeter-wave frequencies. For example, measurements at the Goddard Institute showed a single-sideband receiver noise temperature of 55 K at 46 GHz and 68 K at 115 GHz, at least a factor of 2 better than has ever been done with cooled semiconductor Schottky diode mixers. It appears that another factor-of-3 improvement is possible. The SIS mixer has the unique advantage of potential conversion gain, thus minimizing the noise contributions of the IF amplifier.

Another development that may prove of great importance in making very low noise and, therefore, sensitive receivers is an amplifier that is based on a principle similar to the SQUID magnetometer. It has been demonstrated to have a noise temperature of 1 K (0.015 dB noise figure) for signal frequencies up to 100 MHz. Work is in progress to raise the bandwidth further. This amplifier could be adapted to be the IF amplifier for a very-low-noise receiver front end.

We also saw in section II, B, that the Josephson junction is a rapidly tunable voltage-controlled oscillator. The power is low unless arrays of many junctions are used, but this low power is quite adequate for its use as a local oscillator in a superconductive receiver front end.

It would be entirely feasible and highly profitable to integrate the mixer, local oscillator, and IF amplifier on a single chip to make by far the most sensitive receiver front end in existence. Sensitivity and transmitter power can be traded off unless jamming is encountered, and it is far more practical to work toward improved receiver sensitivity. Increases in transmitter power, except for applications such as electronic warfare, are not always practical because of cost, size, power requirements, source stability, and covertness of operation. It is the opinion of the Task Group that for receiver applications both in radar and communications at frequencies above 35 GHz, the superconductive front end would be of great value.

The development of refractory, high-operating-temperature SIS devices and device arrays as millimeter-wave mixers and detectors is the goal of a Navy program at NRL and under industrial contract. The SQUID parametric amplifier (see section II, B, 2) is also being done under this program, and the eventual goal is to integrate these devices and components monolithically on a single chip for evaluation as a receiver front end.

2. Broadband Signal Processing

Superconductive devices offer opportunities for high-speed signal processing both in analog and digital forms. Analog devices using superconductors are similar to the surface acoustic-wave devices currently employed in radar systems but with 1-2 orders of magnitude greater bandwidth. Digital signal-processing devices have lower bandwidth than the analog devices, but their advantage is versatility; superconductive devices offer data rates about an order of magnitude higher than is currently available. As seen in Figure 2, the analog processors would be used closer to the antenna, where the analog preprocessing could reduce the bandwidth to levels that can be handled by the A/D converter and the digital processor.

a. Analog Signal Processing

Passive transversal filters and other circuit elements are used for a wide variety of signal-processing functions in radar, communications, and electronic-intelligence systems. Such functions have been realized in charge-coupled and surface-acoustic-wave devices for the processing of signals with bandwidths as great as 1 GHz. However, transversal filters with bandwidths in the 1-10 GHz range are needed in systems for the detection and interception of millimeter-wave radar and communication signals and for the processing of high-resolution active radar imaging. Miniature superconductive transmission lines are particularly well suited for this purpose because signals with time-bandwidth products of 1000 and bandwidths to 10 GHz can be contained in compact transmission-line structures that include several thousand taps with accurate phase and amplitude characteristics. Devices have been demonstrated successfully, and prototypes could be realized for system applications in fiscal year 1985. Only optical fibers have the potential for containing such signals as well; however, it is not possible to fashion thousands of precision, phase-coherent taps in optical technology, and it is therefore not suitable for this purpose.

Perhaps the most demanding signal-processing function in radar, communications, imaging, and electronic intelligence systems is the correlation of one signal with another in real time. Often the signals change with time, or a wide variety of signals must be processed by the correlator. One of the compelling needs addressed by the national very-high-speed integrated-circuits (VHSIC) effort is to provide the defense community with correlators capable of handling signals with time-bandwidth products in the range of 10^3 and bandwidths of about 100 MHz. Such dedicated processors perform fast Fourier transform (FFT) operations, and they therefore must provide approximately 10^{10} arithmetic operations per second. The volume and power consumption of such processors fabricated with silicon technology is substantial.

In certain instances an alternate approach can be used for the direct correlation of one signal with another. For example, an ordinary diode mixer will provide the desired correlation of two inputs whenever the signals are in time synchronism. Usually the arrival time of the incoming signal is not known with adequate precision, and other analog methods have been devised for such situations. These methods are realized in silicon CCD technology for bandwidths to approximately 20 MHz, in SAW technology to 200 MHz, and in acoustooptic technology to 2 GHz. These devices afford considerable savings in power and volume over currently available digital technology, and they are employed whenever these savings are critical for a system.

In the coming decade, systems will be developed that need correlators with bandwidths to 10 GHz that are capable of handling signals with time-bandwidth products in excess of 10^3. Such systems include spaceborne imaging radars, low-probability-of-intercept (LPI) and covert spread-spectrum communication channels, LPI radar systems, and intercept receivers for the detection and identification of such signals. Optical techniques cannot be extended into this parameter range because of fundamental limits in acoustooptic materials and in semiconductor photodetectors. Therefore, a new technology is required that will provide the means to reach bandwidths to 10 GHz. The most promising approach is based on superconductive technology, particularly those in which transmission lines, SIS mixers, and Josephson junction devices are employed.

b. Digital Signal Processing

In sections II, D and E, it was shown that with superconductive devices it is possible to do A/D conversion and digital processing at gigahertz rates. There is increasing emphasis on digital systems for many kinds of signal processing because of the unique versatility provided by having the data stored and available for continued manipulation. Figure 2 shows a number of functions that can be performed, including filtering, convolving, and correlating. The availability of A/Ds, logic, and memory that can function at gigahertz rates leads to increased system bandwidth and, therefore, information-handling rates. This could be in a single-channel system or in an image processor where one A/D would be needed for each picture element (see section V, B, 4). Having the capability to do high-level processing before leaving the cryogenic environment would lower the data rate and lessen the loss of information created by going to room-temperature semiconductor electronics.

3. Applications of Sensitive, Wideband Receivers

The performance of millimeter-wave receivers based on semiconductor technologies degrades as the signal frequency is raised above 30 GHz and is noticeably inadequate for perceived applications at higher frequencies. For example, at the high end of the microwave region, semiconductor receivers operating in the 18-26 GHz frequency band can exhibit noise temperatures of about 350 K (NF = 3.4 dB). However, at 115 GHz, room-temperature semiconductor technology can produce receivers with noise temperatures in the range of 1500-2000 K. Even higher values are obtained at still higher frequencies. These values are noticeably higher than antenna noise temperatures encountered in most applications. Improved performance can be achieved by cooling these receivers to cryogenic temperatures: optimally designed receivers employing discrete components, and operating at temperatures below 15 K can have noise temperatures as low as 200 K. However, superconductive technology can yield noise temperatures below 60 K and this technology can be implemented in a monolithic configuration that will be reliable and inexpensive compared with cryogenic semiconductor equipment. These very-low-noise superconductive receivers operating in the millimeter frequency region can have an impact on a number of military systems, including 94-GHz chirped radar, millimeter-wave broadband communication links for low-noise-temperature atmospheric propagation paths such as ground-to-satellite and aircraft-to-aircraft/satellite, broadband electronic-warfare receivers, millimeter-wave imaging radars, 94-GHz antiradiation missile techniques including dual-wavelength systems (millimeter and IR), 94-GHz space-object-identification systems, and synthetic-aperture satellite radar.

A specific system that could have short-term payoff would be a low-probability-of-intercept radar. The system can be cheaply built to transmit signals whose pulse-to-pulse coherence is negligible (i.e., noise) but whose bandwidth is appreciable. Return echoes carry the transmitter spectrum modified by the target characteristics and possibly by target ECM. In order to discriminate among various target signatures, it is proposed to use correlation processing techniques. Because the transmitter spectrum varies randomly, an adaptive programmable filter is needed. To perform this function effectively requires rapid signal digitizing in real time and signal processing. To improve radar system performance will require that a modification be made to radar transmitters to give them a noise-like signal spread over about 250 MHz of bandwidth. This signal, when sampled and stored, becomes the basis of a coherent system featuring reduced probability of intercept and improved range resolution. No current room-temperature technology can provide the 6-8 bit resolution A/D conversion at 500 Msps with the 250-ps high-speed memory required to digitize and store the pulse for subsequent processing. However, this task is within the demonstrated grasp of Josephson technology.

4. Focal-Plane Arrays

Superconductive electronics can play an important role in connection with semiconductor infrared imaging arrays. The environment is already cryogenic, and the need for data processing is enormous. It is desired to convert the signal from each of the detector elements into digital form before leaving the cryogenic environment to avoid signal degradation. This requires a prodigous number of A/D converters operating in the cryogenic environment. Power dissipation would be a problem if this were done with semiconductor A/D converters, but the superconductive devices, particularly those that can give high accuracy at moderately high speeds, could be of great importance in this application. In addition to A/D conversion for each detector element, some level of digital processing would be required to reduce the number of lines between the cryogenic and room-temperature environments. One possibility would be a multiplexer; but the existence of a well-developed family of digital logic and memory circuits in superconductive electronics would also make possible more extensive processing of the image data before leaving the cryogenic environment.

Possibilities also exist for an analogous millimeter-wave focal-plane array using superconductive SIS detectors. The range limitations of current millimeter-wave imaging systems are imposed by the resolution of the system and not by the attenuation of the atmosphere. It is, therefore, possible to go to higher frequencies to improve resolution until the limiting factor is the atmosphere. This crossover occurs in the spectral region of 320-340 GHz. Research is in progress aimed at using focal-plane arrays of superconductive SIS detectors for this purpose. The same A/D converter and digital processor needs exist in this case and could be provided by superconductive devices.

VI. RECOMMENDATIONS

In this section views are given on the areas deserving of support, with an attempt to indicate which are the most promising and important. It is easier to be certain about the desirability of pushing less complex applications; the greater the complexity of a proposed system the greater the number of uncertainties involved in making comparisons between technologies. The risks become greater for more complex applications, not only because the investment is larger but also because the competition with other technologies is harder to assess accurately.

A. MAGNETIC ANOMALY DETECTION AND ELF COMMUNICATIONS

The inherent sensitivity of SQUID magnetometers and gradiometers in Navy ASW, AMW, and ELF communications systems is so great and the importance to defense so critical that the work should be continued vigorously. Emphasis should be placed on the following points:

1. Continue to improve the performance capabilities of current-generation SQUID systems with emphasis on understanding and minimizing low-frequency noise sources and implementing the use of these systems from mobile platforms.
2. Develop thin-film integrated SQUID systems, both analog and digital, employing as much superconductive circuitry as feasible to improve reliability, RFI immunity, and enhanced dynamic range.
3. Interface SQUID systems with closed-cycle cryocoolers to produce a self-contained system suitable for fleet deployment.

B. BROADBAND SIGNAL PROCESSING

Superconductive devices are available to increase the signal-processing speed of Navy systems by significant amounts either in analog or digital form. Increased sophistication of weaponry requires ever-increasing signal handling capacity of radar and communications systems. Order-of-magnitude improvements can be achieved with superconductive devices compared with present technology, in some cases. It is judged to be strongly in the national interest to pursue avenues of research and development in superconductive signal processing.

In view of the need for compact, very wideband correlators for military systems in the coming decade, it is recommended that superconductive analog correlators be strongly supported, including the development of memory correlators and alternate approaches to time-integrating correlators. The devices are likely to be quite compact and to dissipate a negligible amount of power. Their realization in high-T_C materials should permit the use of compact refrigerators, and the appropriate materials effort should be supported.

For broadband digital processing, the Josephson A/D converters and logic and memory appear to be the fastest available. The competition with HEMT at 77 K is not clear, with many problems of off-chip transmission and manufacturability for HEMT as yet not solved. It is the judgment of the Task Group that with both technologies in an early state of development (with some of the systems problems already solved for the Josephson technology), several years of research and development will be required before it is clear which roles the two technologies will play. It would be imprudent to do other than to support vigorously both the Josephson and HEMT technologies at this time. For the Josephson work this includes A/D conversion both of the highest speed flash type and the somewhat slower, more accurate, counting type, which may find its use in focal-plane arrays and magnetometers. It also includes logic and memory development, aimed at larger subsystems for specifically targeted Navy systems.

C. MILLIMETER-WAVE RECEIVER FRONT END

For a number of reasons including increased communication bandwidth, greater spatial resolution, and smaller antenna size, the range of frequencies from 30 to 300 GHz is of increasing interest to the Navy. In section V, B, we discussed the opportunities afforded by superconductive technology to make receivers with the lowest possible noise temperatures using a combination of SIS mixers and superconductive, voltage-tuned, local oscillators and IF amplifiers. It appears to be possible to make such a receiver on a single chip. Such an accomplishment would be of great importance to Navy systems working in this frequency range especially for communication links not dominated by atmospheric noise. Where such systems are to be developed, the Josephson approach should be promoted.

D. SUPERCONDUCTIVE DEVICE DEVELOPMENT

It was pointed out in section III, C, that in spite of the advantageous features of the Josephson junction, it also has disadvantages of being a two-terminal device and having low gain when used in digital circuits.

Research directed toward the development of a high-speed, millivolt-level, cryogenic transistor should be actively pursued. This is a basic research effort and should be wide ranging in scope. But it should also be sufficiently tightly directed that the effort is centered on device concepts that have some promise of delivering the very-high-performance features that a competitive cryogenic transistor must have. Research and development efforts aimed at interfacing Josephson devices and circuits with cooled semiconductor circuits should also be actively pursued.

E. REFRIGERATION

Reliable and efficient cryogenic systems are crucial if superconductive electronic systems are to be introduced into operational systems. Therefore, the development of such systems must be encouraged and aggressively pursued. Particular emphasis must also be placed on the integration of the electronic package and the cryogenic enclosure to produce an optimally designed subsystem or system.

F. RECOMMENDATION FOR A FABRICATION FACILITY

Most of the applications described above can be fabricated in existing or developing facilities at a number of institutions around the country. Various versions of the successful Pb-alloy and Nb-Pb-alloy technologies have been established in several sites and are being effectively employed at the device and small-circuit level. Attractive all-refractory materials systems have been developed and demonstrated, again at the device and small-scale circuit level. Small logic and A/D circuits are being produced and successfully tested in several laboratories, with the programs at the University of California, Berkeley, and the National Bureau of Standards (NBS) being the best examples of such efforts. The NBS program has been particularly effective in promoting interest in the Josephson technology as a result of their open-door guest-worker policy. A number of workers in the sensor area have made effective use of the NBS facility, and several electronics companies have had their interest in digital Josephson technology initiated by working visits of their staff members to NBS. The maintenance and strengthening of the ongoing efforts in superconductive electronics at the materials, device, and small-circuit level is essential.

For the purpose of demonstrating the feasibility of Josephson technology the recent IBM effort was highly successful. The capabilities of large-scale integrated

Josephson circuits (1000 gates of logic and 1 kbit RAM chips) were impressively demonstrated, and the manufacturability of stable Josephson ICs by a disciplined fabrication line has now become an established fact. This capability would have been sufficient to meet the requirements of many Navy applications. However, the development of Josephson technology has been considerably hindered by the lack of access by circuit designers outside of IBM to a stable process capable of producing circuits at the 100-gate-plus level, with a yield sufficient to test circuit designs and, eventually, to provide a systems-level demonstration of the feasibility of special-purpose Josephson circuitry (integrated sensor systems, signal processors). This problem is now critical to the survival of Josephson technology in the United States.

Therefore, the Task Group recommends that a Josephson fabrication facility be established to assure access to the hundreds-of-gates capability as soon as possible. The facility would be open to all industrial, governmental, and university researchers interested in Josephson technology. Its major role would be to produce digital circuits under a fixed set of design rules. IBM has demonstrated such rules to be suitable for very-high-performance analog applications as well. It would be open to scientists and engineers working in device development and physics experiments based on Josephson technology. These experiments would be formulated under the same set of design rules. Such a mode of operation, while appearing restrictive to scientists, has proven to be highly successful in the scientific chip projects at IBM.

It is strongly believed that such a facility would meet both a DoD and national need. It should be pointed out that several facilities of comparable capability exist in Japan.

In order to fabricate structures at the 100-gate level of complexity, a properly sized and staffed facility is required. It would require approximately 10-12 people to properly maintain and operate the equipment and to produce Josephson junction structures for use by the requestors. The equipment dedicated to the fabrication would cost approximately $2.0 million. In addition, this assumes access to the required mask making and lithography and support on the order of $1 million to $1.5 million/year would have to be supplied for a 5-year period.

APPENDIX A

TERMS OF REFERENCE

Task Group on Superconductive Electronics
(Naval Studies Board)

The Office of Naval Research has been a leading government sponsor in fundamental superconductivity research for many years, and this investment has made considerable progress in ultrasensitive magnetic sensors, millimeter-wave and IR detectors, A/D converters, and quantum-limited mixers. The recent IBM management decision to reduce its efforts to a research mode raises questions about the viability and ultimate utility of superconductive electronics technology. It is important to assess the termination of the IBM large-scale, general-purpose computer development project in terms of its implications of the Navy's continued support of research and development programs in superconductivity.

The study will:

1. Review in detail the very major accomplishments of the IBM efforts and assess the factors that caused IBM to terminate the mainframe development program.
2. Assess the future viability of superconductive electronics versus semiconductor electronics (room temperature and cooled) in terms of circuits and systems of potential future use to the fleet.
3. Recommend the directions that present and future Navy basic and applied programs in superconductive materials, devices, and systems should take.