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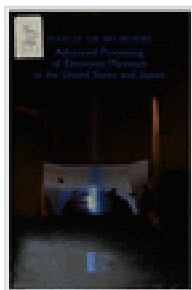

Advanced Processing of Electronic Materials in the United States and Japan (1986)

Pages
52

Size
5 x 9

ISBN
0309321220

Panel on Materials Science; National Materials Advisory Board; Commission on Engineering and Technical Systems; National Research Council

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Advanced Processing of Electronic Materials in the United States and Japan

Panel on Materials Science

National Materials Advisory Board

Commission on Engineering and Technical Systems

National Research Council

NTIS Order number:
PB 88-183 868

NATIONAL ACADEMY PRESS

Washington, D.C.

1986

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This report has been reviewed by a group other than the authors according to procedures approved by a Report Review Committee consisting of members of the National Academy of Sciences, the National Academy of Engineering, and the Institute of Medicine.

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This study by the National Materials Advisory Board was conducted under Contract No. DMS-8414639 with the National Science Foundation.

Copies available from: The National Materials Advisory Board, 2101 Constitution Avenue, N.W., Washington, D.C. 20418.

Printed in the United States of America.

Cover: A high-current oxygen beam incident on a silicon wafer during the exploratory process of fabricating a silicon-on-insulator (SOI) structure by oxygen ion implantation. The path of the incident beam is luminescent because of the excitation of residual gas atoms in the vacuum by the high-intensity oxygen beam. Courtesy of Eaton Corporation.

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PREFACE

During the summer of 1985, a group of state-of-the-art reviews was initiated by the National Research Council at the request of the National Science Foundation. The purpose of these reviews is to assess and monitor world trends and the relative strengths and competitiveness of the United States in rapidly evolving areas of science and technology. Particular emphasis is placed on developments that influence the rate at which these fields evolve. Three areas—cell biology, pure and applied mathematics, and materials science—were chosen for review.

The study on materials science was conducted by the Panel on Materials Science under the auspices of the National Materials Advisory Board (NMAB), of the Research Council's Commission on Engineering and Technical Systems. The specific topic chosen for study is surface processing of electronic materials. This is an area that is evolving rapidly, and it is of great importance. Not only are many significant scientific discoveries in semiconductor electronics continuing to emerge, but it also is the basis of a large and growing industry that has revolutionized major aspects of our lives.

Surface processing is the engine driving the advances in semiconductor electronics. Virtually all advanced processing techniques used in the production of integrated circuits depend on some form of surface modification. Although surface processing is a broad field that encompasses many other materials and applications, it is in the area of semiconductor electronics that the techniques are currently being pushed to their limits. There is great competition in this dynamic field, and recent advances in Japan have been particularly important. For these reasons we chose to assess the status of surface processing of electronic materials in the United States and Japan.

To carry out this assessment, five panel members (Drs. Appleton, Bauer, Picraux, Poate, and Rose) visited several prominent Japanese industrial and university laboratories. These included laboratories at Fujitsu Corporation, Hitachi Corporation, Mitsubishi Corporation, Nippon Electric Corporation (NEC), Nippon Telegraph and Telephone (NTT)

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Corporation, and Toshiba Corporation; the Optoelectronics Joint Research Laboratory sponsored by the Ministry of International Trade and Industry (MITI); the equipment manufacturer, Anelva Corporation; and the university laboratories at Osaka University and Tokyo Institute of Technology. We regret that time constraints kept us from visiting other laboratories and universities where there are active programs in advanced processing research.

We are indebted to our colleagues at those institutions visited for their hospitality and for their open and generous exchange of information. We are also indebted to officers of the Sharp Corporation for stimulating discussions. The panel wishes to acknowledge the support and guidance of Dr. Stanley Barkin of NMAB and the secretarial assistance of Ms. Jennifer Tilles.

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EXECUTIVE SUMMARY

The Panel on Materials Science has assessed the use and importance of advanced processing techniques in the United States and Japan for the fabrication of future electronic and optoelectronic device structures. These future devices must have patterned structures with submicrometer lateral and vertical dimensions to achieve the desired speeds and packing densities, and many will require entirely new materials, materials combinations, and device configurations. These requirements necessitate the development of new processing methods capable of controlling fabrication procedures and materials interactions with submicrometer resolution. Energetic ion, electron, plasma, and laser beam processing, as well as advanced epitaxial growth techniques, have emerged as essential technologies capable of doping, selective etching or deposition, and of controllable patterning on a submicrometer scale. It appears that these advanced processing methods will play a crucial role in the future development of the electronics industry.

Both Japan and the United States are actively involved in advanced processing research and development, but within the past few years the Japanese have entered a stage of vigorous activity that has accelerated their progress relative to that in the United States. It appears that the United States still holds the technological edge in three established areas:

- Ion implantation
- Thin film epitaxy (chemical vapor deposition, molecular beam epitaxy and metallo-organic chemical vapor deposition)
- Film deposition and etching

However, the Japanese have mounted strong programs in all three areas, and this balance could easily shift in the next few years. Within the past year the United States has lost control of

- Optical lithography

It was the assessment of the panel that there are several emerging technological areas where the Japanese are now leading that will be the

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key to future electronic and optical device development. These are the application areas of

- Microwave plasma processing
- Lithographic sources
- Electron and ion microbeams
- Laser-assisted processing
- Compound semiconductor processing
- Optoelectronic integrated circuits
- Three-dimensional device structures

The long-term Japanese commitment to the development of these critical technologies is being carried out by at least 10 major industrial companies, whereas only a few U.S. companies maintain a comparable effort. The overall competitiveness of the United States in electronics has worsened dramatically relative to Japan in the past 5 years. The Japanese are now developing the science and technology needed for the future. Unless the United States responds to this challenge, this trend is likely to continue.

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1. INTRODUCTION

PERSPECTIVES ON SURFACE PROCESSING

The invention of the transistor in 1947 has transformed the way we live, from ease of communication to availability of consumer electronics. The original transistor built by Bardeen, Brattain, and Shockley was a germanium point-contact device. The evolution from that structure to the complex silicon integrated circuits of today is a marvelous story of scientific and technological development. A crucial element of the story has been the development of new materials along with the techniques to process or fabricate those materials into working device structures.

Although the original semiconductor was germanium, it was soon realized that silicon had more advantageous electrical and materials properties. This versatile material opened the way for the development of planar device structures and integrated circuits. Planar silicon technology essentially involves the fabrication of many circuit elements in a two-dimensional fashion on a flat silicon wafer. This configuration permits remarkable control over the fabrication steps required to make and connect the many individual circuit elements.

The processing steps and materials involved can be exemplified through the field effect transistor shown in Figure 1. The goal of any electronic device is to control the flow of charge carriers—i.e., electrons or holes. In the field effect transistor the flow of carriers from the source to the drain is controlled by means of the gate electrode. How is this device fabricated? Perfect silicon crystals are cut into wafers that are then polished to give mirror-like, defect-free surfaces. To control and improve the electrical properties of the surface, an additional layer of silicon is often grown on top of the wafer—for example, by an epitaxial growth technique such as chemical vapor deposition (CVD).

Many different processing steps are required to build up the structure shown in Figure 1, and these steps must be accurately confined to specific regions of the wafer. This control is effected through pattern transfer techniques that are used to transfer geometric shapes on a mask to the surface of a silicon wafer. For example, the silicon wafers

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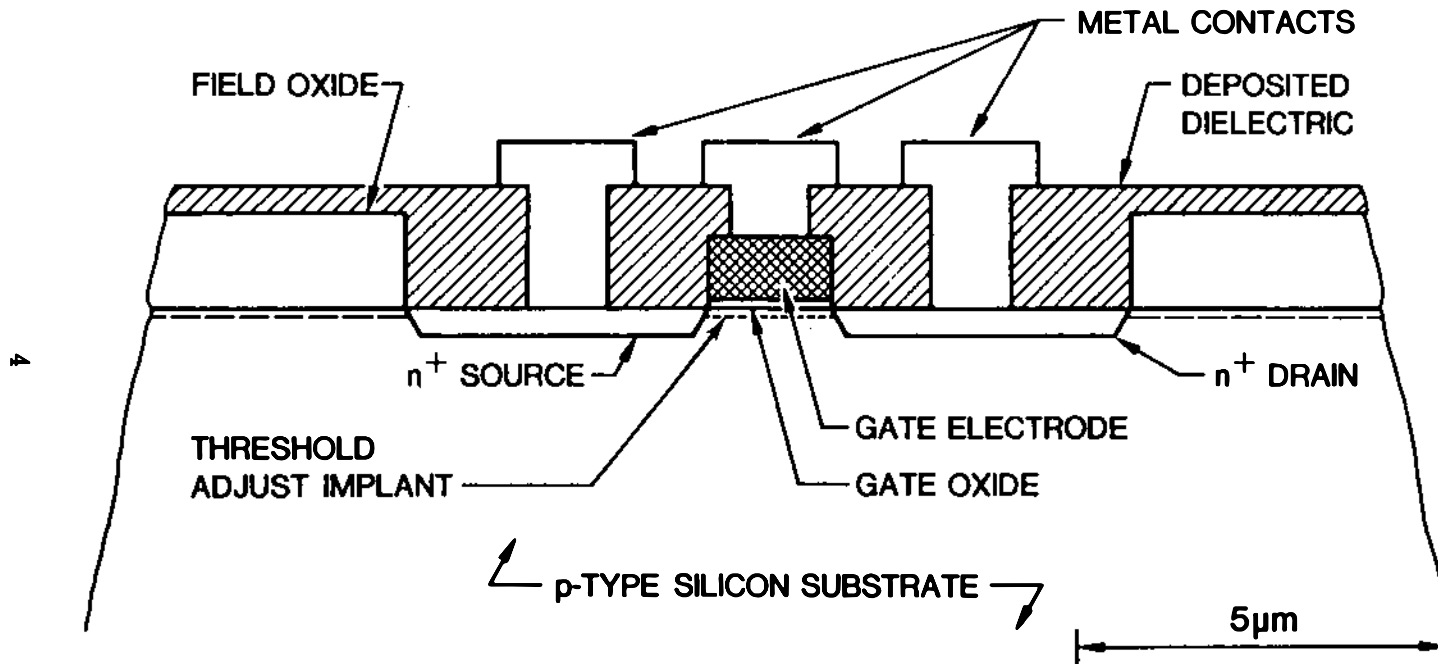

FIGURE 1. Cross-sectional view of a metal oxide semiconductor field effect transistor (MOSFET) structure showing the patterning and different components required to fabricate such a device structure.

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are heated in oxygen to form insulating SiO_2 layers for forming the field oxide. Lithographic techniques are used to transfer polymeric masks (photoresists) onto the regions that need to be protected in subsequent etching steps. The SiO_2 can be etched chemically (i.e., wet) or by plasma-assisted etching (i.e., dry). In this way, for example, the unmasked SiO_2 is removed and source-drain regions are exposed.

Pure silicon at room temperature has high resistivity, and dopants must be introduced to give the silicon its conducting properties. The dopants, such as arsenic, are injected into the silicon by means of ion implantation. The whole wafer is exposed to the energetic arsenic beam, but only the exposed or unmasked regions are implanted. The wafer must be heated after implantation to anneal the damage created in the silicon by the implanted arsenic ions.

Metal contacts are needed to make electrical connections to the source, gate, and drain areas. To provide such contacts, a metal film such as aluminum is deposited and patterned by subtractive etching or lift-off. The conductors are isolated by a deposited dielectric such as SiO_2 or Si_3N_4. In an integrated circuit there can be many thousands of such transistors and other circuit elements requiring numerous precise fabrication steps.

Entirely new surface processing technologies have evolved to fabricate the structures just described. A common theme to most of these processes is the use of energetic particles (whether photon, electron, or ion beams) to provide spatial definition at the micrometer-scale level and to initiate surface reactions such as etching and film growth. For example, masks are lithographically exposed by the irradiation of polymeric resist materials with intense photon or electron beams. Energetic ions efficiently remove material from surface layers by plasma or sputter etching. Electrical dopants are accurately and selectively introduced by ion implantation at depths ranging from near the surface to 0.5 μm.

The development of these surface processing techniques has largely been carried out in the United States and has taken place in industrial, government, and university laboratories. This has been a particularly exciting era for materials science. A classic example is the development of ion implantation. The first report came from Russell Ohl at Bell Laboratories in 1952, but the path from invention to commercial acceptance took many years. Many groups in the United States and Europe in the 1960s studied the basic physics and materials science of the process. In particular, understanding the ranges of the implanted atoms,

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the damage they produced, and the means of removing that damage by annealing were key developments. However, it was not until the early 1970s that the process gained commercial acceptance, when it was recognized that only implantation doping could be used to shift threshold voltages in field effect transistors in a reproducible and reliable fashion and to form high-precision resistors. Today, implantation has become an essential fabrication process. Every integrated circuit now made employs ion implantation. Indeed, the remarkable growth in integrated circuit technology is difficult to envision without ion implantation.

LIMITS AND TRENDS

Silicon is the most important semiconductor material at present, with a variety of functions from memory circuits in very-large-scale integration (VLSI) to high-power elements. The future of VLSI is clear. Smaller dimensions will permit faster circuits with lower power requirements and a greater number of elements. Devices and systems incorporating these faster and smaller circuits will continue to revolutionize the computer and communication industries. Societies that take a leading position in this technology will stay at the forefront of the information age.

Typical device dimensions in silicon VLSI circuits are now 1 to 3 μm. We can project that in 10 years these dimensions will be nearly an order of magnitude smaller. To achieve this shrinkage in lateral dimensions, new materials processing techniques are required. The drive to increase the density of circuit elements by shrinking lateral dimensions necessitates concomitant reductions in vertical dimensions. For example, future circuit elements will require submicrometer-wide conductor lines, insulating gate oxides a few hundredths of a micrometer thick, and junction depths of a tenth of a micrometer or less. At these dimensions the material constraints become much more critical. For example, the conductor lines must be constructed of high-conductivity material that must remain metallurgically inert while in contact with the other circuit materials and not degrade under the high current densities. Here we are discussing films that are only a few hundred atom layers in thickness. Interface reactions that normally involve many atomic layers must be controlled to within a few atomic layers if the device is to function.

Control of material fabrication and interactions on this atomic scale requires new approaches to the manufacturing process. The lithographic processes that define the circuits must be capable of high definition

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with submicrometer-scale resolution. The subsequent etching, deposition, and implantation doping techniques must be capable of performing their functions within these dimensional constraints. For example, for shallow junctions, dopants must be implanted close to the surface. But subsequent annealing steps to remove the implantation damage must be at sufficiently low temperatures (or short times) to preclude substantial dopant diffusion. In general, the trend is toward low-temperature processing to reduce unwanted motion or materials interaction in this submicrometer-scale world.

A new silicon device configuration is emerging that also relies heavily on surface processing techniques. Multiple layers of crystalline silicon separated by insulating SiO_2 layers can be built, thus allowing the construction for the first time of truly three-dimensional circuits. Immediate device advantages of one dielectrically isolated silicon layer are increased packing densities and speed of operation. In the long term, however, three-dimensional structures offer the possibility of quite new circuit functions.

The driving force to date has been planar circuits based on silicon, but other semiconductor materials and alternate device structures are becoming increasingly important. For example, optical devices permit the manipulation of photons. The ability to emit and detect light over a wide range of frequencies demands materials and structures of considerable complexity compared to silicon, which has only weak light-emitting characteristics because of its indirect bandgap. Binary compounds such as GaAs or InP and ternaries such as AlGaAs or InGaAs are used in highly complex multilayer structures to make possible, for example, lasers with a variety of frequencies. The situation here is very different from that of silicon in that these complex structures and materials require entirely new approaches to crystal growth and processing technologies. For example, thin film crystal growth techniques such as molecular beam epitaxy (MBE) and associated processing steps may have to occur in an ultrahigh vacuum (UHV) environment. Even with silicon, avoiding submicrometer-scale particulate contamination may require vacuum (or low-pressure) processing and multiple processing steps in a single chamber.

WHY JAPAN?

The past development of the U.S. semiconductor industry has been intimately coupled to advances in surface processing techniques. Most

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advances in these techniques have originated in U.S. laboratories. But what of the future? It seems certain that the future lies in smaller integrated circuits, more complex device architecture, and innovative uses of new materials. It also appears certain that new surface modification techniques must be developed to fabricate these structures. This necessity is recognized in semiconductor research laboratories in the United States and throughout the world. However, it appears that Japanese industry is ahead in making a long-term commitment to the advancement and exploitation of these techniques.

Japan has developed a systematic approach to identifying research and development priorities. Much of this is accomplished under the auspices of the Ministry of International Trade and Industry (MITI), which initiates cooperative government-industry projects targeted at specific technologies deemed crucial for future industrial development. MITI designated 12 such projects for the 1980s that were thought to require 10 years of research and development to support emerging technologies in the 1990s. The three categories for these projects were future electron devices, new materials, and biotechnology. The major emphasis in future electron devices is in the areas of superlattice devices, three-dimensional integrated circuits, and hardened integrated circuits for environmentally extreme conditions.

In conducting its study, the panel chose to visit Japan because of the strong programs there devoted to developing surface modification techniques for the processing of electronic materials. These R&D programs appear to be the most comprehensive and far-reaching of any country. This report details the panel's observations of the state of this research and development in Japan. We first present the key processing technologies that are essential to the fabrication of the next generation of electronic materials and structures. We then give two examples where the synergism between advanced processing and new materials is giving rise to new structures and concepts. The emphasis in this report is on the differences between the U.S. and Japanese positions. It appears that Japan is taking the lead in several key areas of electronic materials fabrication. This subject is rapidly evolving, and its outcome is of major importance to the U.S. scientific and industrial position.

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2. PROCESSING TECHNOLOGIES

ION IMPLANTATION

Ion implantation doping has already become one of the dominant processing techniques in the semiconductor industry. A present-day VLSI circuit may have from 6 to 12 separate implantation steps. The characteristics that have made implantation an essential process include control of lateral uniformity; control of implanted dopant profiles; accurate and reproducible control of dopant concentration and purity; low-temperature processing; and spatial definition.

In future devices these same processing characteristics will be of increasing importance. The need for shallow abrupt junctions requires better control of implantation parameters at low energies. Correspondingly, higher energy implants are finding application in the fabrication of complementary metal oxide semiconductor (CMOS) devices to replace high-temperature diffusion for forming n and p wells and for creating buried layers that act as charge traps. A new direction in ion implantation is emerging that involves implantation at doses many thousands of times higher than those used for conventional doping applications. Oxygen or nitrogen can thus be implanted beneath the silicon surface at concentrations sufficient to form buried oxide or nitride insulating layers equivalent in thickness, for example, to 0.1 μm of SiO_2. Subsequent heating can restore full crystallinity to the surface silicon layers. Moreover, the implanted oxygen combines chemically to form a layer of SiO_2 with sharp boundaries. A $Si/SiO_2/Si$ heterostructure is thus formed. There is much interest in such silicon-on-insulator (SOI) heterostructures for increased speed and higher densities. Such devices can be made to be highly resistant to transient ionizing radiation. As we discuss later, there are several competing surface modification techniques for making SOI structures. Ion implantation, although currently expensive at such high doses, offers several advantages. In particular, this solid-phase process produces high-quality silicon overlayers on wafers using techniques compatible with existing production lines.

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In addition to these extensions of conventional, broad-beam ion implantation, focused ion microbeams are being used to explore advanced circuit fabrication. For example, microbeams can be used for maskless ion implantation, for fine-line lithography, and for selective etching and sputtering. Although processes requiring direct, serial writing of the ion beam are intrinsically slow, this slow speed is not a major limitation in the fabrication of optoelectronic devices. Moreover, the exploratory use of these beams is opening up new dimensions of materials science.

Conventional ion implantation—e.g., irradiation of whole wafers at energies typically from 50 to 150 keV—is used routinely in Japan as it is in the rest of the world. There is a clear interest and need in both the United States and Japan for low-energy implantations—e.g., 10 keV—for the formation of shallow junctions. There is more activity in the United States in the area of high-energy (e.g., 1 MeV), low-dose implants. In contrast, the Japanese have a clear commitment to the use of high-dose implantations for materials synthesis such as the buried insulating layer process. Figure 2 shows the unique high-current oxygen implantation accelerator being constructed in the United States for the NTT research laboratories at Atsugi.

A significant difference observed in Japan is the degree to which all laboratories are making use of focused ion beams in advanced circuit and process development. Applications included maskless implantation, in both silicon and compound semiconductors, and ion-assisted etching and deposition. Indeed, there are about 30 commercial finely focused ion beam systems in Japanese industrial laboratories. An exemplary use of focused microbeams was seen at the Optoelectronics Joint Research Laboratory, a MITI laboratory, where focused ion beams were used in conjunction with MBE to fabricate heterostructure lasers in a UHV system that allowed for sequential processing. The microbeams were used not only for maskless implantation but for fabrication of laser cavities by reactive ion etching.

The United States leads the world in materials and physics research related to the basic understanding of implantation processes. In the area of equipment for conventional applications, the United States still commands a lead in quantity and innovation; on the other hand, the initiative for the development of equipment for ion microbeam technologies appears to lie with Japan.

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FIGURE 2. High-current ion implantation accelerator and wafer processing station used for the fabrication of buried insulating SiO_2 layers in silicon formed by O^+ implantation. Courtesy of Eaton Corporation.

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DIRECTED ENERGY SOURCES FOR ANNEALING AND RECRYSTALLIZATION

The heating of wafers in furnaces over the temperature range from 500 to 1000°C has been an intrinsic part of semiconductor manufacturing for the past 30 years. Such heating is traditionally used to anneal implantation damage and to react metal films to form contact pads to the semiconductor. These treatments are carried out in flowing gas furnaces for times and temperatures of typically 30 minutes and 1000°C. This heating cycle is not compatible with the fine dimensional control required by the next generation of silicon structures or with the special constraints such as chemical decomposition of surfaces experienced by compound semiconductors. For example, heating at 1000°C for 30 minutes can cause implanted dopants to diffuse hundreds of atomic layers. To overcome these problems, furnaces have been developed in the United States and Japan to permit high-temperature treatments with times as short as a few seconds. This technology is known as rapid thermal annealing (RTA). Historically, the first rapid heating sources used were continuous-wave and pulsed lasers; these sources showed that one could controllably melt thin surface layers of silicon. This field of "laser annealing" not only has stimulated the development of RTA but also has led to the concept of lateral epitaxy. In lateral epitaxy, melt fronts are swept across silicon films on insulating layers, resulting in device-quality silicon. Such structures are an extension of existing technology. However, the use of scanning laser or electron beams has made it possible to stack layers of crystalline silicon between dielectric films to form three-dimensional circuits.

U.S. and Japanese researchers clearly recognize the potential of RTA processing, not only for dimensional control but also for the obvious economic advantage of increased throughput. As a result they are pursuing RTA in many areas of semiconductor technology. The effort in Japan is particularly intensive. For example, at Hitachi Central Research Laboratory, RTA is being studied for the following processes: electrical activation of implanted dopants; silicide conductor film formation; annealing of high-energy implantation damage; formation of contacts to GaAs; growth of SiO_2 in an RTA reactor; and densification of phosphosilicate-glass. All these processes benefited in some fashion from RTA. We know of no comparable U.S. effort in a single laboratory addressing such a wide range of RTA applications. The focus of the

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effort appears not to be in the development of new RTA furnaces but in addressing the materials science and device processing questions. It would appear that these techniques are already in use in Japan for GaAs integrated circuit manufacturing.

The area of SOI research is extensive in the United States and is probably the most active area of silicon crystal growth research. The goal is to achieve device-worthy silicon over insulating layers on production-sized wafers. The emphasis is different in Japan. The goal there is to fabricate stacked, insulated layers of silicon for novel, three-dimensional circuits. This has involved the refinement of scanning laser and electron beam systems for lateral epitaxy. Such systems must be used to crystallize the silicon overlayers while maintaining the low substrate temperatures necessary to preserve the integrity of the underlying layers of devices. At Toshiba, researchers are forming SOI structures by the use of focused spot electron beams that are scanned and modulated to produce a linear melt front. The researchers have improved the quality and size of the recrystallized areas by careful control of the electron beam and material parameters. The subject of three-dimensional circuits, which has been targeted as a MITI goal, is now being realized in numerous laboratories. Although the complexity of such circuits implies low production yields at present, the Japanese researchers have boldly developed new scanning systems, designed mask sets, and produced working three-level silicon circuits. For example, at the LSI R&D Laboratory of Mitsubishi, researchers have produced complex circuits at the one- and two-level silicon stage, including the fabrication of a 1.1 k-gate CMOS/SOI gate array, which is the first demonstration of CMOS-LSI laser recrystallized SOI. The goal is to fabricate integrated three-dimensional circuits embodying an optical sensor on the upper layer and signal processing circuits in the four lower layers (Figure 3).

There is still concern that techniques that use thin-film melting are incompatible with the requirements of device integrity and manufacturing control. An alternative approach is to produce lateral expitaxial growth in the solid phase. Several Japanese groups are pursuing lateral solid-phase epitaxy. The main limitations of this technique are competing nucleation events leading to polycrystalline film formation, which necessitates heating at temperatures lower than 600°C for many hours to achieve 10 μm lateral growth.

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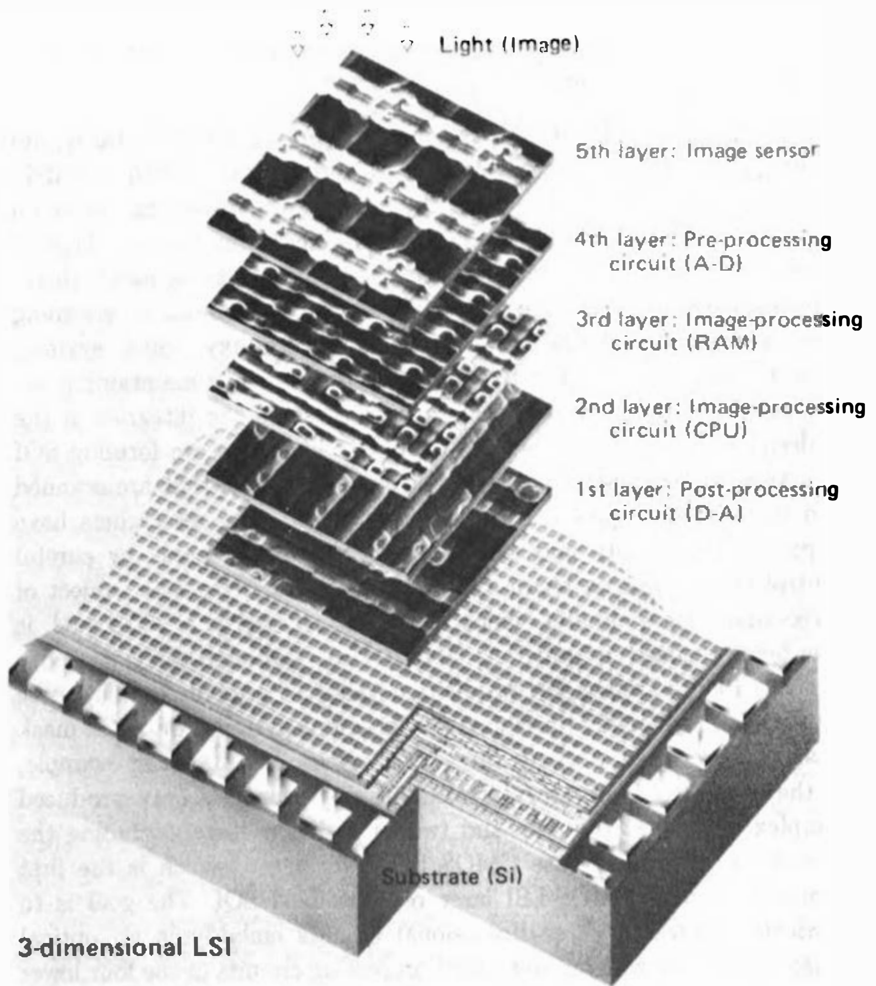

FIGURE 3. Exploded schematic view of a proposed five-layer, three-dimensional LSI device structure for image processing conceived by Mitsubishi.

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While U.S. researchers are at the forefront of the science of laser annealing with regard to basic solidification and phase transformation studies, Japanese researchers are ahead in the application of laser and electron beams and solid phase epitaxy for the fabrication of SOI structures. Furthermore, their active development of RTA will assure Japan of a leading position in this new area of semiconductor processing.

THIN FILM EPITAXY

Conventional wafer fabrication techniques for circuit processing typically involve bulk crystal growth for the production of substrate wafers on which epitaxial layers of the same material are grown by CVD or liquid-phase techniques. These epitaxial layers can be readily doped for the prescribed circuit applications. Much thinner layers with precise interface definition can be grown at lower temperatures using the newer approaches of MBE and metallo-organic chemical vapor deposition (MOCVD). The latter techniques have opened up entirely new realms of crystal growth in terms of heterostructure and superlattice fabrication. These new artificially structured materials have resulted in the discovery of new physics such as quantum well effects and new devices such as modulation doped transistors. MBE was initiated in the United States some 20 years ago, and most of the forefront research continues to originate from here. Similarly, in the area of MOCVD epitaxial growth, U.S. workers are pioneering the new developments.

The Japanese scientific community recognizes the importance of all these crystal growth techniques for their semiconductor industry. Indeed, their research in both MBE and MOCVD is accelerating rapidly, with a particular emphasis on GaAs structures. However, the production of defect-free, bulk GaAs ingots has been one of the limiting steps in the implementation of GaAs technology. One of the important current developments in Japan is the growth of high-quality, nearly dislocation-free, bulk GaAs 3-in. (7.6-cm) ingots. To achieve this end, bulk crystal growth techniques employing, for example, indium doping, arsenic overpressure, and vertical magnetic fields have been highly refined and have proved most successful.

The growth of epitaxial films on substrates necessitates not only surface cleanliness but also sufficient surface atom mobility to obtain

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layered, defect-free crystal growth. This normally requires high substrate temperatures. Japanese semiconductor scientists are intent on developing low-temperature epitaxial growth processes. They are accomplishing this by the innovative use of energetic beams to impart additional surface mobility and reactivity. Scientists at the NEC's Fundamental Research Laboratories are enhancing CVD epitaxial growth rates of silicon at low temperatures (e.g., 700 to 850°C) with excimer lasers or Hg-Xe lamps. Furthermore, the epitaxy occurs in a controllable fashion through windows etched in SiO_2 on silicon substrates. There is much emphasis in Japan on the use of microwave plasmas for film deposition and etching. Researchers at NTT's Atsugi Electrical Communication Laboratories have demonstrated that plasma-stimulated epitaxial growth of silicon from silane (reactive ion beam deposition) can take place at temperatures as low as 400°C with ion bombardment energies near 200 eV.

Epitaxial growth in microelectronic applications has conventionally involved only the deposition of semiconducting layers on semiconductor substrates with similar lattice parameters. Quite novel approaches to the growth of epitaxial structures involving dissimilar lattice parameters are being actively investigated in the United States and Japan. The area of most interest is the growth of GaAs on silicon, and competition is intense. Structures combining epitaxial metals and insulators with semiconductors are also being actively studied in the United States and Japan. For example, scientists at Tokyo Institute of Technology, Hitachi's Central Research Laboratory, and Oki Electric Industry Company laboratories are studying the growth of such semiconductors as silicon, germanium, and GaAs on crystalline insulators (CaF_2) or crystalline silicides ($NiSi_2$ or $CoSi_2$). These structures offer new device possibilities.

MBE and MOCVD technologies will play an increasingly important role in future devices. Both countries are devoting significant effort to these technologies, and the United States still appears to have the edge. Furthermore, both countries now realize that the growth of lattice mismatched structures such as GaAs on silicon could yield large rewards. Moreover, the Japanese are giving particular emphasis to beam- and plasma-stimulated low-temperature crystal growth. It should be emphasized however, that the successful effort in the growth of significantly improved GaAs bulk

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crystals puts the Japanese in a leading position in the GaAs integrated circuit area and in their effort to develop an optoelectronic technology.

FILM DEPOSITION

Thin films play an essential role in the operation of integrated circuits. They provide conductor paths between semiconductor elements and insulating layers to isolate electrical functions. The conductors are usually either highly doped polycrystalline silicon, metal films such as aluminum, or polycrystalline silicides. The drive toward smaller device structures is imposing strong constraints on these films. The resistivity of the conductor films becomes critical as they get thinner. Moreover, the metallic conductors must maintain continuous paths without cracks over abrupt circuit features. The dielectrics are usually amorphous films such as SiO_2 or Si_3N_4. To perform their insulating function, it is necessary for these thin films to be continuous and free of electrical defects.

The most critical dielectric in silicon technology is the gate oxide in MOS devices, which must be formed with a minimum of defect states at the interface and a high electrical breakdown strength. These oxides can be as thin as several hundredths of a micrometer. At present they are formed by heating wafers in a dry oxygen atmosphere at temperatures of about 1000°C. For thicker layers, wet oxidation is used at atmospheric or increased pressures. The dielectrics that are used for insulation between conducting layers or as ion implantation masks are usually deposited by chemical reaction processes (i.e., CVD) or by plasma deposition. For example, Si_3N_4 can be deposited by the CVD reaction of $SiH_4 + NH_3$ at gas pressures of 1 torr (133.3 pascals) and wafer temperatures of 700 to 900°C. For plasma deposition these gases are reacted in a gas discharge, and plasma Si_3N_4 can be formed at temperatures as low as 200 to 350°C. In a radio-frequency (RF) plasma of 13.56 MHz at pressures of 10^{-1} torr, the ion energies can be as high as 1 keV.

These CVD processes are universally used in the industry at present to produce films of good dielectric integrity and good topographical coverage because the pressures are high and the deposition is not a line-of-sight process. However, there are significant drawbacks in the

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implementation of the processes for future submicrometer-scale technologies. Temperatures are usually high for CVD processes. Temperatures are low in plasma CVD, but the high ion energies can cause radiation damage. Japanese researchers are tackling these problems by the use of microwave power for plasma generation.

Researchers at NTT are using an electron-cyclotron resonance (ECR) plasma technique to deposit SiO_2 and Si_3N_4 films on silicon for device processing. This ECR process employs microwaves at 2.45 GHz to create a plasma from oxygen or nitrogen and SiH_4. A diverging magnetic field is used to extract low-energy ions (20 to 50 eV) from the plasma at low pressures (10^{-4} torr). Very pure films of SiO_2 or Si_3N_4 were deposited over a 20-cm-diameter region. Although deposited at low temperatures (less than 150°C), the films had chemical and physical properties the equivalent of 900°C conventional CVD films, and the low-energy ion bombardment did not damage the substrate. Indeed, the interface state densities of such SiO_2 films grown on silicon appear comparable to those grown by conventional thermal oxidation at 1000°C. These microwave techniques have considerable potential for etching as will be discussed in the following section. The importance attached to these surface modification techniques for future device processing is reflected by researchers at Mitsubishi who view ECR deposition as the only technique capable of producing suitable SiO_2 films for coverage of 0.5 μm devices with step patterns having aspect ratios greater than 1.

The most active area of thin film conductor research in both the United States and Japan is that dealing with silicides. At present, for example, the gate electrode of Figure 1 can be made of heavily doped and conducting polycrystalline silicon (resistivity approximately 500 $\mu\Omega$-cm). Polycrystalline silicon is an ideal conductor on silicon circuits because it is metallurgically compatible and nonreactive. However, its resistivity is too high when channel lengths get to submicrometer dimensions. Silicides or refractory metals are then used as conductors. Silicides that are usually good metallic conductors are formed by reacting silicon with transition metals. Silicides used in current large-scale memory devices are $MoSi_2$, $TaSi_2$, and WSi_2, with resistivities of approximately 50 $\mu\Omega$-cm. This resistivity will be too high for the next generation of memory circuits, and there is intense research to find a replacement. The best candidate appears to be $TiSi_2$, with a resistivity of 15 $\mu\Omega$-cm. Research into this material both in terms of its materials

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parameters and deposition by sputter or CVD apparatus appears to be on a par in the United States and Japan.

Where Japan leads is in its novel approach in the use of silicides. For example, Fujitsu has pioneered the use of silicides on GaAs. The refractory metal silicides that are metallurgically inert on GaAs are patterned to act as electrodes and masks for implantation. This self-aligned gate technology is now widely used in GaAs fabrication throughout the world. The Optoelectronics Joint Research Laboratory has taken a novel approach to metallization on GaAs and has proposed LaB_6 for gate metallization. The concept of ion-beam mixing has been developed in U.S. laboratories in recent years; metal films can be reacted or mixed with energetic ion bombardment. However, it was a Japanese group at NEC that first applied this technique to refractory silicide formation on circuits.

There is considerable work in Japan on the use of beam techniques to enhance deposition of metals. The work appears to be concentrated on finely focused beams for mask repair (i.e., depositing metal on selective areas where there is a transparent defect in an existing metallized mask). Researchers at NEC are using Q-switched NdYAG lasers to perform selective mask repair. By using the laser to heat only the near surface of the masked device, they can deposit chromium from $Cr(CO)_6$ in areas as small as 10 μm on a side. NEC researchers are also writing fine lines of tungsten directly (without mask definition) using laser-assisted decomposition of $W(CO)_6$. The resistivity of these lines is 8 times that of bulk tungsten because of incorporated carbon contaminants. Scientists at Hitachi's Central Research Laboratory were able to circumvent this contamination problem and deposit tungsten films on SiO_2 with resistivities only twice that of bulk tungsten by shining ArF laser light parallel to the surface in the presence of the reactive gases WF_6 and hydrogen. Such resistivity values are adequate for device fabrication. Researchers at Osaka University are writing 0.5-μm lines of aluminum by 35-keV gallium ion bombardment in a $(CH_3)_3Al$ atmosphere of 3×10^{-2} torr at a rate of 20 deposited atoms per incident ion. With this same system, submicrometer-size transparent defects in lithographic masks can be repaired in a few milliseconds.

The science and technology of film deposition and growth are wide ranging. The United States would appear to be ahead of, or on a par with, Japan in most areas of present-day processing.

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However, there are obvious differences in areas that may be crucial to future technologies. The Japanese effort in low-pressure microwave plasma research for dielectric film formation surpasses anything in the United States. The Japanese effort in the use of focused beams to enhance deposition in selective areas is also extensive and appears to be surpassing similar research in the United States.

ETCHING AND MACHINING

An essential part of device fabrication is the ability to pattern planar structures in the semiconductors and overlying dielectric and conductor films. This patterning is achieved by selective etching or machining techniques through the use of organic masks. Historically, this has been achieved by wet chemical etching. This approach cannot be used for devices on any sort of fine scale because the etching is isotropic, which means that undercutting of structures becomes significant as etch depths approach the lateral feature sizes.

In present VLSI technology, etching is carried out by means of RF reactive ion etching techniques. The masked wafer is immersed in a plasma containing a reactive gas such as chlorine or fluorine at pressures typically of 10^{-2} torr. The surface is bombarded by ions from the RF plasma with energies on the order of 1 keV, and surface atoms are removed at an enhanced rate by a combination of direct physical sputtering and by the formation of volatile chemical compounds such as $SiCl_4$. This process works remarkably well at present, and the United States dominates the equipment market and research in reactive ion etching. However, problems are looming for the large-scale circuits of the future. These problems include the damage introduced by the intense ion bombardment as well as directional control over the etching. Although reactive ion etching is far more anisotropic than wet etching techniques, there are still sidewall etching problems, and undercutting in submicrometer-scale structures is crucial. These inherent problems are well recognized in the Japanese research community and are being addressed in several innovative ways.

A new approach to plasma formation widely studied in Japan at present is the use of 2.45-GHz microwaves to excite the plasma. The resonant coupling of energy to the electrons in this manner means that a plasma can be formed with characteristics very different from those

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involving gas discharges now used in reactive ion etching. Only low gas pressures (10^{-4} torr) are required in microwave plasmas, and, as a result, gas scattering is reduced. The sample surface is thus bathed with low-energy ions rather than the higher energy bombardment required for the dense high-pressure plasmas. Since the ions can be extracted from the plasma without an intervening grid electrode and directed onto the wafer by magnetic fields, the problem of sputtered contaminants from the electrode and walls is eliminated.

Both the science and technology of microwave plasma etching are being widely explored in Japan. For example, researchers at Hitachi's Central Research Laboratory are achieving high anisotropy for etching silicon with ion energies below 100 eV using SF_6 gas at 10^{-4} torr pressures. At Mitsubishi's LSI Research and Development Laboratory, the use of microwave plasma etching is considered an essential technology in plans for patterning 4- and 16-megabit dynamic random access memories (DRAMs). Researchers are developing a system in cooperation with Tokyo Electron Ltd. to produce high currents over 6-inch-diameter (15-cm) wafers with ion energies of less than 50 eV and with demonstrated feature sizes of 0.2 μm. Other major Japanese companies are developing their own systems, and the equipment manufacturer, Anelva, is marketing a commercial microwave plasma system developed in collaboration with NTT.

Another approach to etching being investigated in Japan and the United States is the use of excimer lasers to excite etchant gases and induce selective etching by photothermal and photochemical processes. For example, workers at Toshiba are investigating laser-assisted dry etching in chlorine gas. Microwave excitation of a chlorine gas stream containing organic gas additives is combined with excimer laser stimulation to enhance etch rates and improve the anisotropy of etching. Photo-assisted etching techniques are also being investigated using deep ultraviolet irradiation with Hg-Xe lamps, for example, at NEC, and high etching rates (0.1 μm/minute) have been demonstrated.

Focused ion beams have unique capabilities in the areas of machining and etching. Ion beams can be used for direct physical sputtering or can be combined with etchant gases to achieve reactive ion etching results, analogous to plasma or photo-assisted etching. What is novel here is the ability to etch structures directly without the aid of any lithographic patterning on the 0.1-μm scale. These techniques are unlikely to be used in silicon large-scale technology because serial writing processes

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are intrinsically slow. However, prototype production on a laboratory scale can be speeded up by its use. Also many optoelectronic devices do not need large-scale integration. At the Optoelectronics Joint Research Laboratory, focused ion beams were used both for maskless ion implantation and reactive ion etching in the fabrication of optical integrated circuits. Research and equipment development in focused ion beams was in progress at Optoelectronics Joint Research Laboratory, Fujitsu, Hitachi, Mitsubishi, Tokyo Institute of Technology, and Osaka University. The Osaka University group is studying the etching of GaAs, InP, and silicon with fluorine and chlorine gases as support etchants. This approach gives an etching rate an order of magnitude greater than simple physical sputtering without the etchant gases.

> The United States leads in the science and technology of conventional RF reactive ion etching, and U.S. firms dominate the manufacturing of equipment. Japanese researchers are firmly convinced that new surface modification techniques must be developed for etching and patterning future device structures. They have developed microwave etching processes that can pattern large-area wafers and are well ahead in the microwave plasma area on all accounts. Laser and ion-assisted etching techniques are being researched on a broad front in both the United States and Japan, but there is much greater emphasis in Japan on the use of focused beams.

LITHOGRAPHY

Lithography is the process of forming two-dimensional patterns. The transfer of patterns onto semiconductor chips is an essential step in the fabrication of integrated circuits. Each pattern defines the regions in which the next processing step—implantation, oxidation, film deposition, etc.—will be applied, and the patterns must be precisely registered with previous steps. Typically, about a dozen lithographic steps are involved in the fabrication of a modern integrated circuit. Achieving higher lateral resolution in the lithographic process is an essential requirement for achieving higher density and faster circuits.

Patterns can be replicated on the semiconductor surface by either the parallel process of printing with a broad area beam or by the serial process of writing with a finely focused beam. In current manufacturing processes, lithography is carried out optically by projection printing

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onto thin, photosensitive polymer films. U.S. companies dominated the optical lithography equipment business through 1985; however, in the past year Japanese companies have taken the major market share. The useful resolution of optical lithography today is around 1 μm, with possible extensions to 0.5 μm using ultraviolet light. By using X-rays, electrons, or ions, the diffraction effects are effectively eliminated and consequently there is great interest in these beams for the next generation of lithographic processes requiring high resolution. The promise of broad beam ion lithography is only being explored to a limited extent in the United States and Europe.

Focused electron beams are now the primary writing technology for mask making and can be used to directly write patterns onto polymer resists with submicrometer-scale resolution. The United States has the major market share of the mask making technology whereas the Japanese dominate the direct writing technology for circuit fabrication. Focused ion beam systems are a derivative technology, and they currently achieve resolutions below 0.1 μm. The problem with doing lithography by any direct writing on production wafers is that the time for forming the patterns is too great for economic fabrication of integrated circuits, and there is the additional problem of the proximity effect for the practical utilization of electron beams. Therefore, electron-beam direct writing is primarily used to fabricate or repair masks for optical lithography or for forming prototype circuits. Focused beams have also been demonstrated to be useful for limited operations on specialized integrated circuits, such as for altering discretionary interconnections. Even though electron-beam writing systems have increased greatly in speed, the drive to smaller dimensions and higher densities further increases the time demands on direct-writing approaches. Thus, there is great interest in the development of new lithographic techniques using X-ray or electron-beam printing while taking advantage of focused electron and ion beams wherever possible.

In all the Japanese companies visited, there was an emphasis on decreasing the size of the devices within circuits. The projected need for lithographic techniques capable of producing geometries with line widths down to 0.1 μm has forced the realization that current optical techniques will not be capable of such fine resolution. Consequently, there is active development and evaluation of e-beam, X-ray, and ion-beam lithographic systems on a scale not seen elsewhere in the world.

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In the field of X-ray lithography it appears that the United States has lost the initiative to Japan and possibly also to Europe for the development of commercial equipment. In Europe, for example, the Fraunhofer Institute for Microstructure Technology in West Berlin is developing a superconducting storage ring with microtron injection that has been licensed to a West German company for commercial sale. In Japan, the Electro Technical Laboratory is equipping itself with a synchrotron radiation source (i.e., storage ring) from Toshiba, and NTT is purchasing both a superconducting storage ring from Hitachi and a conventional magnet synchrotron from Toshiba. Sumitomo Heavy Industries, Sumitomo Electric, and Nippon Seiko have also prepared proposals to build synchrotron radiation sources for the semiconductor market. Many of the designs emphasize compact systems with diameters just over 1 m. In contrast, there is no such activity in the United States.

The advanced integrated circuits that were presented for discussion during visits in Japan were made by direct-write e-beam lithography, as would have been the case in other parts of the world. More surprising was the frequent use of ion microbeams for experimental device fabrication. In addition to direct doping or etching enhancement, focused ion beams were used to expose resists for standard lithographic applications. The high rate of energy loss, sharply defined range, and small amount of lateral scattering give remarkably well-defined submicrometer-scale patterns—i.e., 0.1 μm in size or smaller. The most significant limitation of focused ion beams is the limited throughput caused by inadequate current density (1 A/cm^2). Although several new companies are building and refining focused ion beams in the United States, the efforts in Japan in the development of commercial focused ion beams for semiconductor applications appear to be more advanced.

The Japanese have a very substantial commitment to advancing high-resolution lithography at the fastest possible pace. They are now working from a base where two companies, Nikon and Canon, command the optical lithography equipment business. Researchers at many institutions there are not only developing increasingly efficient focused ion beam systems and high-throughput electron-beam lithography systems, but they are also making a large commitment to X-ray lithography.

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ULTRAHIGH VACUUM PROCESSING

Processing technologies such as ion implantation or sputter deposition of thin films require that the particle beams move within a vacuum; otherwise, collisions with the ambient gas will stop the beam. Pressures in commercial processing apparatus are typically of the order of 10^{-6} torr where contaminants impinge on surfaces at the rate of a monolayer per second. Such pressures are compatible with economic throughput of wafers, in that large vacuum chambers can be quickly evacuated from atmospheric pressure. Vacuum seals are maintained with elastomer gaskets. A new world of physics and materials science has emerged in the past 25 years with the development of UHV science. At pressures of 10^{-9} or 10^{-10} torr, surfaces can be maintained for many hours in their pristine state without the growth of oxide or contaminant layers.

Extraordinary precautions must be taken to evacuate chambers and vessels to such low pressures. The containing walls must be baked to remove any residual gases, vacuum seals must be maintained with metal gaskets, and the vacuum pumps must have a high degree of efficiency. The scientific payoff in the development of this technology has been large. The study of pristine surfaces has revealed a wealth of new structural and electronic information. It was discovered at AT&T Bell Laboratories in the mid-1960s that molecular beams of gallium and arsenic, when impinging on clean surfaces of GaAs, would grow epitaxial layers. In this way MBE was discovered. This is one of the crucial crystal growth techniques of recent years. The growth of epitaxial structures of remarkable purity and thinness has led to the discovery of new physical properties (e.g., fractional quantized Hall effect) and devices (e.g., modulation-doped transistors).

A question of considerable importance to the device community is whether MBE techniques can be successfully wedded to processing technology. At present, UHV processing is not used in silicon technology, as it is not needed for existing device fabrication. However, MBE techniques are needed for GaAs and other compound-semiconductor technologies. The economic constraints of throughput impose formidable challenges to the vacuum engineer. We know of no MBE systems in the United States or Europe that provide realistic throughput of wafers. We learned, however, that the Anelva Corporation in Japan is constructing a GaAs MBE system with capacity for deposition on 7 wafers with 70 wafers loaded in the UHV environment. Also, as the discussion

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in the next section emphasizes, researchers at Optoelectronics Joint Research Laboratory have successfully integrated MBE, focused ion beams, annealing, and deposition processes into an experimental UHV processing line.

The importance of UHV processing for the next generation of materials and structures is still very much an open question. Research on this subject is active in both the United States and Japan. The U.S. lead in surface science and MBE should provide the edge in developing this technology.

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3. NEW STRUCTURES AND MATERIALS

The field of semiconductor materials and processing is witnessing the introduction and development of many new techniques. When the materials and techniques come together, radically new structures and devices can result. Thus far in this report we have discussed some of the crucial processing areas that are being developed and exploited in Japanese industries and universities. In this section we describe two unique examples of the synergism between processing and materials that is evident in Japan today. The two examples—SOI structures and focused ion beam implantation combined with MBE to fabricate heterostructure lasers—typify the climate for research and development in Japan. We know of no equivalent work in any U.S. industrial, government, or university laboratory that demonstrates such a concentrated intellectual and financial commitment.

The first demonstration that another dimension could be added to silicon processing came from Stanford University in the late 1970s. It was demonstrated, using laser-induced recrystallization, that device-worthy silicon could be fabricated on SiO_2, and the first three-dimensional device structure was constructed. This work at Stanford and other U.S. laboratories has stimulated much research throughout the world. There are now many competing technologies for producing SOI one-layer structures. These range from strip heaters to laser or electron beam recrystallization, solid-phase and CVD lateral epitaxial growth, ion implantation to form buried oxides, and epitaxial growth of crystalline insulators followed by conventional silicon epitaxy. The immediate or shorter term objective of this technology is the production of 4 to 6 inch wafers for one-level circuit fabrication. It would appear here that the U.S. and Japanese technologies are on an equal footing. It has been demonstrated in both countries that large-scale circuits can be fabricated. The driving forces for one-level SOI are increased speed, higher packing densities, prevention of crosstalk between devices, and resistance to transient ionizing radiation. The economics of the process, however, have not yet been established.

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What is unique in the Japanese SOI effort is the desire to construct working circuits employing many layers of silicon incorporating active areas stacked between SiO_2 layers. The only practicable approach at present appears to be recrystallization of deposited silicon using scanning laser or electron beams. In this way the temperature of the underlying silicon and dielectric layers does not rise so high as to degrade the underlying devices. This approach has been demonstrated with three-level working circuits. The realization of three-dimensional, large-scale integrated circuits is part of a MITI 10-year program.

At the Mitsubishi's LSI Research and Development Laboratory, the three-dimensional SOI process development effort is focused on achieving optical parallel processing systems (Figure 3). The concept is to detect light signals with a two-dimensional image sensor array at the top level and process the signals in parallel on subsequent levels. This would include analog-to-digital conversion, computer image processing, digital memory storage, and output functions. Mitsubishi researchers envision five-level circuitry and have already demonstrated many of the individual functions in complex circuits on one-level SOI, as well as device fabrication and operation on three levels.

The concept of parallel optical image detection, processing, and digital storage in a three-dimensional circuit architecture is an example of the revolutionary new approaches that can emerge from new materials and processing. Perhaps the most amazing aspect of this and related examples currently being pursued in Japan is the level of effort and progress on a potential product that is clearly seen to be 7 to 10 years away from the marketplace. To our knowledge, no comparable efforts on such long-term products are being carried out in the U.S. semiconductor industry.

Several trends in the semiconductor industry in Japan indicate that future device structures may depend much more heavily on UHV processing techniques than at present. The growth of heterostructures by MBE requires UHV processing. If other techniques such as implantation followed by epitaxial overgrowth are to be employed with MBE, then the processing must take place completely in the UHV environment. The Optoelectronics Joint Research Laboratory has constructed a unique UHV facility embodying MBE and focused ion beam implantation for the fabrication of optoelectronic devices.

The goal in optoelectronic devices is to create a new class of devices where optical and electrical components are integrated onto a single

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chip. Such devices cannot be made from silicon but must be fabricated from compounds of the Group III-V elements, such as GaAs. A single optoelectronic integrated circuit (OEIC) could combine lasers, photodetectors, and active electronic devices such as amplifiers and modulators onto a single GaAs chip. Although such circuits would have significant advantages, they pose serious fabrication difficulties. To circumvent some of the problems, the Optoelectronics Joint Research Laboratory has developed a novel system for fabricating OEICs that consists of several sequential UHV processing and analysis chambers connected by UHV sample transfer tubes. A schematic representation of the system is shown in Figure 4 along with the sequential steps that go into fabricating a device. The starting material is high-quality wafers of GaAs grown by a magnetic-field-applied liquid-encapsulated Czochralski method. Several UHV processing steps require epitaxial deposition in the MBE chamber shown in Figure 4. Transfer in UHV between processing steps avoids surface (interface) contamination caused by atmospheric exposure.

The second processing chamber shown in Figure 4 is a 100-keV focused ion beam implantation system connected to the MBE chamber by a UHV sample transfer module. This system is used for producing dopant concentration profiles in both horizontal and vertical directions without photolithographic resist masks of any kind. By using computer control, the finely focused ion beam can be scanned across the wafer in any desired pattern and correlated with sequential depositions in the MBE chamber to produce a variety of complex structures required for OEICs without ever exposing the wafer to the atmosphere. The focused ion beam system is capable of implanting patterns with defined regions less than 0.5 μm in width. An integrated transistor and light-emitting diode has been fabricated on an AlGaAs/GaAs double heterostructure grown using focused beams of beryllium and silicon. The intent in the future is to introduce processing steps for insulator and metal film deposition and for etching, all within the same chamber. No experimental facility like this exists in the United States.

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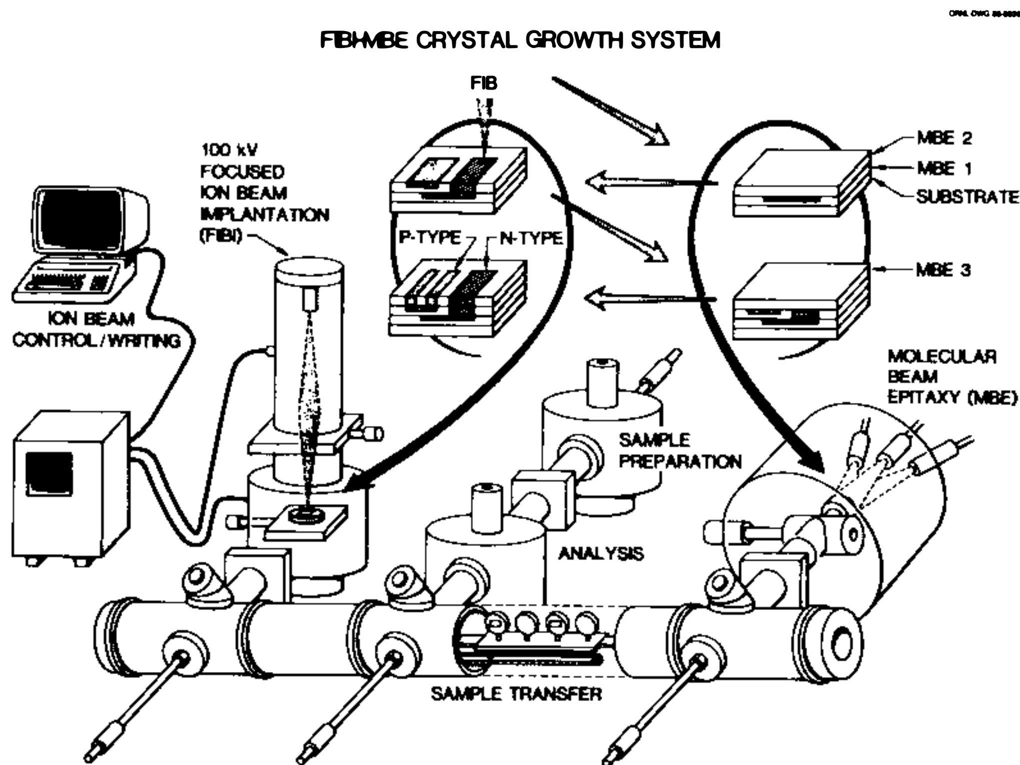

FIGURE 4. Device fabrication system at the Optoelectronics Joint Research Laboratory that integrates a focused ion beam implantation (FIBI) system, an MBE chamber, and sample preparation and analysis chambers into a common UHV processing system. Modified from an original drawing supplied by Optoelectronics Joint Research Laboratory.

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4. CONCLUSIONS

ELECTRONIC MATERIALS AND SURFACE PROCESSING

During the past 30 years the importance of electronic materials to U.S. science and commerce has become immense. Research and development in electronic materials have led to many scientific and engineering advances. In the physical sciences these range from the Nobel-prize-winning subjects of tunneling to the quantized Hall effect. Engineering and processing advances go from greatly improved vacuum technology to high-purity materials synthesis. This combination of science and engineering has led to the ability to produce devices as diverse as VLSI circuit memories used in computers and discrete heterostructure lasers used in recording and sensing. This field is large and still rapidly evolving. For semiconductor device production alone, worldwide sales exceeded $31 billion in 1984, fell to $28 billion in 1985, and is projected by market analysts to exceed $50 billion by the end of the decade. In the years from 1980 to 1985 the U.S. share of the world market has dropped from 64 to 53 percent. A loss of leadership in this area will have significant consequences for the national security and economic well-being of the United States.

We believe that the future of electronic materials and devices depends crucially on the advanced processing technologies discussed in this report. Already, surface modification is at the heart of the semiconductor processing industry. The trend for future devices is toward smaller structures embodying different combinations of electronic and optical materials. Such structures can only be fabricated with techniques that have the precision to tailor materials on the submicrometer level. This again is the regime of surface processing. It is in this increasingly important area that we believe we are losing the leadership to Japan.

THE JAPANESE POSITION

It is our observation that there are certain key ingredients to the Japanese success story.

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• *Commitment*. The Japanese have made a long-term commitment to the development of new processing technologies and the application of these to new semiconductor structures. They are convinced that novel plasma and beam processing techniques are essential for the fabrication needs of future devices. The commitment to long-range research and development in this area involves not only university and government consortia, such as the MITI large-scale projects, but also the major semiconductor industrial laboratories. MITI has designated several projects in microelectronics requiring 10 or more years of research and development to bring them to the marketplace. In microelectronics these include superlattice devices, three-dimensional integrated circuits, hardened integrated circuits for extreme conditions, and, most recently, an 8-year project to develop advanced fabrication technologies and equipment for submicrometer-scale processing. These projects center on surface processing techniques.

• *Coupling*. Within individual Japanese companies, the coupling between exploratory R&D and device fabrication is remarkably efficient. This coupling is evidenced by the extent to which materials scientists are fully cognizant of the limitations and requirements for advanced device manufacturing. The same tendency is also apparent in the interactions and collaborations between the equipment manufacturers and the semiconductor circuit manufacturers.

• *Commerce*. Japan's semiconductor industry is made up of at least ten entities that pursue long-range research and development on a scale matched by only a few U.S. companies. This arrangement gives many strengths. Each company covers the spectrum of product development from the laboratory to the marketplace, and each entity is a giant in its own right. Moreover, the commercial rivalry, both domestic and international, between these giants fosters innovative research and development, leads to new products, and forces increased efficiency.

• *Creativity*. Creativity and innovation are central to the development of any new technology, and the Japanese are demonstrating both these attributes in their R&D programs.

KEY TECHNOLOGIES

We have identified and discussed in this report the surface processing technologies required for implementation of present and future electronic structures. The competition between the United States and Japan in these areas at present is vigorous. The United States maintains its

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lead in most areas of implantation research and is the major supplier of implantation machines. On the other hand, the U.S. pre-eminence in the crucial area of lithography has been surrendered to Japan in the past year. The United States leads in the thin film deposition and etching technologies used in present-day circuit fabrication. The situation is so dynamic, however, that Japanese companies could become the major suppliers of deposition and etching equipment within the next few years. The thin film epitaxial growth techniques, MBE and MOCVD, continue to be a U.S. stronghold. But the Japanese recognize the potential of this area and are becoming major competitors.

But what of the key technologies of the future? Submicrometer-scale device structures require low-temperature depositions and machining techniques that have spatial definition approaching the atomic scale. Optoelectronic devices require novel combinations of materials and processing techniques to create new device structures. Our assessment is that Japan has within the past 2 years entered into a stage of accelerated development relative to U.S. activity. This development activity ranges from the materials scientist to the equipment manufacturer. In the following we list the areas in which we believe U.S. research and development are lagging behind Japan's.

- *Microwave Plasma Processing*. Radio-frequency (RF) plasma etching and deposition techniques are widely utilized in present-day VLSI circuit fabrication. The Japanese have developed microwave plasma systems that have significant advantages over RF techniques. These microwave systems provide low-temperature, damage-free etching and deposition capabilities, characteristics that are considered crucial for future devices. This technology is sufficiently developed so that implementation is imminent.
- *Lithography Sources*. The limit of pattern resolution for optical lithography in current large-scale silicon processing is about 0.5 μm. The resolution limits arise with present optical sources because of the wavelength limitations dictated by the shortest wavelengths allowed by refractive optics. Advances in the lithographic process require the development of higher resolution. Several Japanese companies are developing X-ray lithographic sources in the form of compact synchrotron radiation sources compatible with device processing.
- *Electron and Ion Microbeams*. Electron beams are important for the generation of optical masks and direct writing of circuits. The Japanese are now a major force in this equipment market. Finely

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focused ion beams are more versatile in that they can be used for direct writing with increased resolution, micromachining and etching, and direct implantation without a mask. Japan now leads in the development and use of this emerging technology and is the leading supplier of focused ion beam systems.

- *Laser-Assisted Processing*. Present circuit processing technologies for etching and thin film deposition do not employ laser sources to enhance reaction rates. Researchers in the United States and Japan are exploring a wide range of applications of lasers and incoherent light sources for low-temperature processing. Although this field is still in the exploratory stage, the potential for new discoveries and improvement of low-temperature CVD techniques is great.
- *Compound Semiconductor Processing*. GaAs is a potential candidate for the replacement of silicon in some applications that require increased speed and reduced power consumption. In spite of the advantages, application is held up by many processing difficulties. It would appear that Japanese laboratories already have a better understanding of the entire spectrum of processing steps for GaAs, from material growth to self-aligned gate implantations.
- *Optoelectronic Integrated Circuits*. The successful integration of electronic and optical properties in a single structure is of considerable importance. Complex compound semiconductor materials are required, and the difficult processing problems can only be solved by the most sophisticated techniques. One particularly innovative Japanese approach is the integration of sequential processing steps into one UHV processing system to fabricate complete structures.
- *Three-Dimensional Circuits*. Novel device configurations can be realized with the stacking of silicon active layers. This is being accomplished in Japan using scanned laser or electron beam sources to recrystallize silicon films on insulating layers. Although it is recognized by the Japanese researchers that this work is very exploratory, benefits are expected in terms of new processing technologies and new device architectures.

THE UNITED STATES AND THE FUTURE

Advanced processing techniques are essential for the fabrication of future devices, which are necessary for advances in electronic technology. Therefore, the United States must aggressively pursue a position of prominence in surface processing if it is to be competitive in future device

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fabrication technologies. Fundamental understanding of this technology is strong in the United States. It is not, however, sufficient to master just the underlying science; a similar competence must be sustained in the processing technology associated with advanced semiconductor manufacturing. Without such an activity, the United States could become dependent on others for the advanced electronic devices that fuel computer technology, the communications industry, and advanced defense systems.

At present the Japanese are ahead of the United States in the development and application of advanced processing technologies. At least ten of the major semiconductor companies in Japan have vigorous programs targeted for projects with an expected payoff 7 to 10 years later. There are only a few, perhaps two, U.S. firms similarly involved. Japan seems to have evolved a successful approach for identifying and implementing critical technologies within the commercial environment.

Mechanisms to encourage long-term commitment to research and development in U.S. industry need to be formulated. The Japanese long-term commitment not only has assured a competitive position in present semiconductor manufacturing technology but also appears to guarantee a competitive position in the future. The attitude and commitment of U.S. companies is determined by many complex factors, principal among which is our financial system. It is beyond the scope of this report to address these issues. A recent report on this subject has been prepared by the Presidential Commission on Industrial Competitiveness.*

One area where the United States has significant strength is in its university programs. There are at least a half dozen universities in the United States that have strong academic programs in electronic materials that are backed by equally strong research programs directly pertinent to industry needs. Some universities without strong internal programs have created or are becoming involved in research consortia directed toward research and development in electronic materials and related programs. The acceptance of this approach is reflected in the support such programs have received from government and industry in recent years in the form of joint research ventures and direct faculty

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* Report of the President's Commission on Industrial Competitiveness, January, 1985: Volume 1, Global Competition—The New Reality. Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402, Stock No. 003-009-00-438-1.

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and equipment support; such support is important to these programs. There are now at least a half dozen research consortia involving universities, government, or industries.* The net result is that the U.S. university system produces graduates who are familiar with equipment and procedures in the semiconductor industry and are qualified to take on responsible R&D positions in the industry.

In comparison, there are perhaps half as many universities similarly involved in Japan in electronic materials research. Japanese universities graduate more engineers per capita, and even on an absolute basis, than universities in the United States. However, their programs tend to be more academic, with less emphasis on laboratory training and on advanced research. The Japanese companies augment this deficiency by strong in-house continuing-education programs that train employees for the specific tasks required. Overall, U.S. universities fare very well in comparison. It is U.S. companies and government laboratories that appear to be lagging behind their Japanese counterparts.

Government-funded research in Japan has served as a potent catalyst for long-range research and development in its industries. MITI's Agency of Industrial Science and Technology has significantly influenced research and development in Japan and, as a consequence, the worldwide competitiveness of Japanese products. Industries in both Japan and the United States have a natural disincentive to pursue long-range high-risk R&D because of uncertainties of the return on the investment. MITI helps overcome these difficulties by identifying potential commercial markets, coordinating industry participation, and leveraging research with government funds. MITI also supports industrial technology through its national research laboratories like the Electro Technical Laboratory. One of the main reasons that this degree of planning and coordination is possible in Japan is the stable and competent base of technical managers in both government and industry.

Government laboratories in the United States have the potential to provide substantial support to U.S. companies in this critical technology, but this would require a change in emphasis from current policy. In

* Examples of joint research ventures involving universities include the Microelectronics and Computer Technology Corporation, the Semiconductor Research Cooperative, the National Science Foundation's Engineering Research Centers, and the Microelectronics Center of North Carolina.

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contrast to Japan, where MITI focuses government funding into areas that are considered commerically viable in 5 to 10 years, the majority of U.S. government funding for electronics research is directed toward needs in national defense and aerospace programs. Since the technological requirements of these programs are very different from the needs in consumer and communications electronics, they are not designed to contribute directly to the U.S. position in these competitive areas. At present there is little emphasis in government laboratories on advanced semiconductor processing technology or pertinent electronic materials development except in these specialized defense activities. In contrast, during the 1950s and 1960s advances in accelerator science and associated electronics developed at national laboratories and universities diffused into the private sector to help form the base of the present-day ion implantation industry. Government laboratories have the equipment and expertise to contribute to advanced processing science, but this area has not been identified as a prime mission. For increased involvement to occur, the U.S. government would need to recognize this as an area of national importance and reconcile this with the present laboratory missions. The area of most need appears to be intermediate between the truly long-range research and short-term processing R&D necessary for present device technology. To ensure success in attacking some of these intermediate processing problems, U.S. industry should be intimately involved with the government laboratories. This would allow the combined resources of government and industry to be directed toward relevant problems and to solve these problems on a set schedule in mesh with industry needs.

In this report we have attempted to assess the relative strengths of the United States and Japan in the field of advanced processing of electronic materials. The relative state of a scientific and technological subject is a complex function of a given society. To this end we have briefly compared some of the technical aspects of U.S. and Japanese companies, government laboratories, and universities. We have identified key surface processing technologies where U.S. research is lagging behind that of Japan.

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ACRONYMS

CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
DRAM	Dynamic random access memory
ECR	Electron-cyclotron resonance
FIBI	Focused ion beam implantation
LSI	Large-scale integration
MBE	Molecular beam epitaxy
MOCVD	Metallo-organic chemical vapor deposition
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
NdYAG	Neodymium yttrium aluminum garnet
OEIC	Optoelectronic integrated circuit
RF	Radio frequency
RTA	Rapid thermal annealing
SOI	Silicon-on-insulator
UHV	Ultrahigh vacuum
VLSI	Very-large-scale integration

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BIOGRAPHICAL SKETCHES OF PANEL MEMBERS

WALTER BAUER received an A.B. degree from the University of California at Berkeley and M.S. and Ph.D. degrees in physics from the University of Illinois. After working at North American Aviation, Inc., he joined the staff at Sandia National Laboratories Livermore (SNLL). He is presently head of the Physical Research Department at SNLL. His research interests include defects in metals, electron radiation effects, inert gas migration in metals, and ion implantation.

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JOHN W. COBURN received B.A.Sc. and M.A.Sc. degrees from the University of British Columbia and a Ph.D. degree in electrical engineering from the University of Minnesota. After employment at Simon Fraser University, he joined the staff at the International Business Machines Research Laboratories, San Jose. His research interests include particle diagnostics in glow discharges, thin film formation by sputtering and by plasma polymerization, and the physics and chemistry of dry etching processes.

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superlattice properties, and spectroscopies of atomic core excitation in crystals and on crystal surfaces.

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