High Performance Ultra-low Voltage Continuous-Time Delta-Sigma Modulators

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Abstract

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Submitted by **Yan CHEN**

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The scaling of the feature sizes of CMOS technologies results in a continuous reduction of supply voltage (V_{DD}) to maintain reliability and to reduce the power dissipation per unit area for increasingly denser digital integrated circuits. The V_{DD} for low-power digital circuits is predicted to drop to 0.5V in about ten years. Ultra-low voltage (ULV) operation will also be required for the analog-to-digital converter, a universal functional block in mixed-signal integrated circuits, in situations where the benefits of using a single V_{DD} out-weigh the overhead associated with multi-V_{DD} solutions.

Continuous-time (CT) Delta-Sigma Modulators (DSMs) have re-gained popularity recently for oversampling analog-to-digital conversion, because they are more suitable for low supply voltage implementation than their discrete-time (DT) counterparts, among other reasons. To the state of art at the low voltage front, a CT 0.5-V audio-band DSM with a return-to-open

feedback digital-to-analog converter has been reported. However, the 0.5-V CT DSM has a limited performance of 74-dB SNDR due to clock jitters and other factors caused by the ultra-low supply.

In this thesis, three novel ULV audio-band CT DSMs with high signal-to-noise-plus-distortion ratio (SNDR) are reported for a nominal supply of 0.5V. The first one firstly realizes a switched-capacitor-resistor (SCR) feedback at 0.5V, enabled by a fast amplifier at 0.5V, for reduced clock jitter-sensitivity. Fabricated in a 0.13μm CMOS process using only standard V_T devices, the 3rd order modulator with distributed feedback occupies an active area of 0.8mm^2. It achieves a measured SNDR of 81.2dB over a 25-*k*Hz signal bandwidth while consuming 625μW at 0.5-V. The measured modulator performance is consistent across a supply voltage range from 0.5V to 0.8V and a temperature range from -20°C to 90°C. Measurement results and thermal-noise calculation show that the peak SNDR is limited by thermal noise.

The second ULV CT DSM employs a feed-forward loop topology with SCR feedback. Designed in 0.13μm CMOS process, the modulator achieves a post-layout simulation (thermal noise included) result of 89dB SNDR over a 25-*k*Hz signal bandwidth. The 0.13μm CMOS chip consumes an active area of 0.85mm^2 and 682.5μW at 0.5-V supply. It achieves an excellent measured performance of 87.8dB SNDR over a 25-*k*Hz signal bandwidth and a102dB spurious-free dynamic range. To the best of our knowledge, this performance is the highest for DSMs in this supply voltage range. Thanks to the proposed adaptive biasing technique, the measured modulator performance is consistent across a supply voltage range from 0.4V to 0.75V and a temperature range from -20°C to 90°C.

Finally, a 0.5-V 2-1 cascaded CT DSM with SCR feedback is proposed. A new synthesis method is presented. Transistor-level simulations show that a 98dB SNDR is achieved over a

25-*k*Hz signal bandwidth with a 6.4MHz sampling frequency and 350μW power consumption under a 0.5-V supply.

摘要

隨著 CMOS 工藝特徵尺寸的不斷減小，系統供電電壓也在不斷降低，一方面確保系統工作的可靠性，另一方面降低數位電路的功耗。據預計，低功耗數位電路供電電壓在未來 10 年會降到 0.5V。在某些應用場合下單電源供電比多電源供電更佔優勢，這樣模數轉換器作爲混合信號積體電路中一個通用的模組，也必須在超低壓工作。

近幾年來，在過採樣模數轉換器中，連續時間 ΔΣ 調製器備受關注，原因之一就是他們相對離散時間 ΔΣ 調製器更適合實現低電壓下工作。據報導，到目前爲止，一個 0.5V 供電的音頻範圍的連續時間 ΔΣ 調製器已設計出來，其反饋回路的模數轉換器採用了開路回歸的方式。但該 0.5V 連續時間調製器的性能由於受到時鐘抖動和超低壓工作下其他因素的影響，其 SNDR 僅有 74dB。

在論文中，提出了三個新穎的超低壓音頻範圍的連續時間 ΔΣ 調製器，它們在 0.5V 供電電壓下工作，具有較高的信號雜訊諧波失真比。第一個 ΔΣ 調製器採用了 0.5V 供電的快速回應放大器，首次實現了 0.5V 供電時開關電容電阻回饋方式，降低了時鐘抖動的影響。該 ΔΣ 調製器採用了 0.13 微米的工藝實現，電路採用的都是標準 V_T 器件，晶片面積占了 0.8 平方毫米。調製器採用了 3 階積分器級聯回饋結構，測試結果表明，在 0.5V 供電下，在 25-*k*Hz 信號帶寬內，調製器的峰值信號雜訊諧波失真比可達 81.2dB, 功耗是 625 微瓦。從測試結果可以看出，調製器在供電電壓從 0.5V 到 0.8V 變化，溫度範圍從-20°C 到 90°C 變化的條件下工作一致性都很好。結合測試結果和熱雜訊計算結果，發現峰值信號雜訊諧波失真比受到熱雜訊的限制。

第二個 ΔΣ 調製器採用了帶 SCR 回饋的積分器級聯前饋結構，依然採用 0.13 微米的工藝實現，版圖後仿結果和熱雜訊計算結果表明，在 25-*k*Hz 信號帶寬內，調製器可以達到 89dB 的峰值信號雜訊諧波失真比。該 ΔΣ 調製器採用了 0.13 微米的工藝實現，晶片面積占了 0.85 平方毫米。在 0.5V 供電下，功耗是 682.5 微瓦。調製器的峰值信號雜訊諧波失真比可達 87.8dB，無雜散動態

範圍達到 102dB。據我們所知，這個性能是在這個低壓範圍內工作的調製器中最好的。多虧採用了自適應偏置方法，測試結果表明調製器在供電電壓從 0.4V 到 0.75V 變化，溫度範圍從-20°C 到 90°C 變化的條件下工作一致性都很好。

最後提出了一種新型的級聯連續時間 ΔΣ 調製器的綜合方法，並將該方法用於設計一個 0.5V 2-1 級聯的帶開關電阻電容回饋的連續時間 ΔΣ 調製器。電晶體級仿真表明在 25-*k*Hz 信號帶寬和 6.4M 過採樣頻率下，調製器的信號雜訊諧波失真比可以達到 98dB, 功耗僅爲 350 微瓦。

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Chapter 1

Backgrounds and Overview

1.1 Introduction

As predicated by Gordon Moore [1], semiconductor designs have benefited significantly from technology scaling in the past decades, especially for power consumption and performance. With the advancement of CMOS technologies, the feature sizes have been scaled down into the nanometer region. However, device scaling can cause breakdown and increase tunneling currents due to the high electric filed in the device. Another negative effect of technology scaling is that leakage power increases tremendously from one technology generation to next. So the supply voltage (V_{DD}) faces an inevitable downward trend for effective power consumption reduction of digital circuits and also for the reliability of the devices.

Power reduction is a major concern for almost all IC products nowadays. The rapidly increasing demands nowadays for portable electronic products or battery-powered devices like mobile phone, PDAs, portable computers, portable video gadgets, GPS facilities, wristwatch computation, hearing aids and pacemakers, particularly require low-voltage low-power circuits for longer battery times. Even for non-battery-powered products like wireless sensor networks, toxic gas sensors, microprocessors, and even spacecraft electronics [2], reduced power consumption can reduce cost due to cheaper packing or high performance because of lower operating temperature. On the other hand, environmental awareness of the public also makes low power consumption (which can be achieved effectively by using low supply voltages) a key consideration in large digital systems like data storage centers or telecommunication base stations. Another hot area of research recently is to design electronic systems which can retrieve

power from environment. For example, a single solar cell provides power to applications which only have a supply voltage of 0.5V [3]-[4]. All those facts hint that low-voltage circuit design is becoming an increasingly important topic today.

The International Roadmap for Semiconductor (ITRS) anticipates future design needs for basic research capabilities and product potentials [5]. Fig 1.1 shows the trend in supply voltage for past and future technology nodes predicted by ITRS [6]. The supply voltage for low-power digital circuits is predicted to drop to 0.5V in about ten years [5]. At the same time, the threshold voltage, V_T, scales more slowly than the supply voltage and remains in 0.15V to 0.3V to limit the sub-threshold currents.

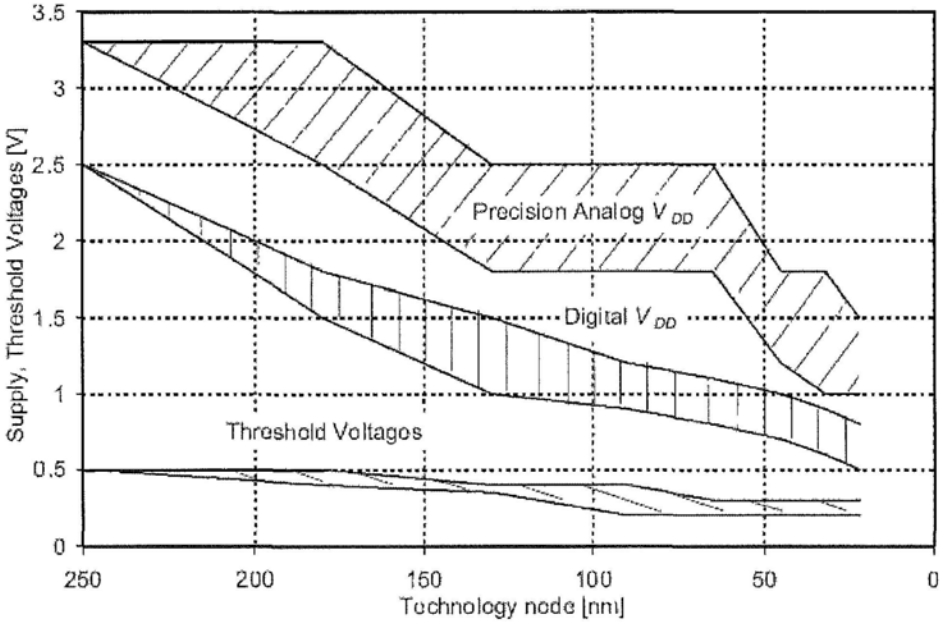


Fig 1.1 Supply voltage and threshold voltages trend s with technology scaling [6].

Nowadays, modern system-on-chip (SOC) solutions have found great benefits in consumer communications and computing products. Analog circuits take up only 5-30% of the total SOC chip area. To maintain the scaling trend of digital circuits and keep the process technology simple, the analog circuits need to operate in ultra-low-supply (ULV) voltage which

offers significant performance benefits for digital systems. On the other hand, ULV analog circuits design also provides an opportunity to push the technology limit, to explore the boundaries of the state of the arts of analog circuits design, and to develop novel circuit-level and system-level solutions.

However, there are a number of problems and challenges accompanied by this ULV analog circuits design. First, the transistor intrinsic gain is reduced. For analog circuits, the gain is an important metric of device performance. The reduced intrinsic gain limits the performance of ULV analog circuits. Second, signal-to-noise ratio (SNR) is reduced. The reduced supply voltage limits the headroom for devices, such as available voltage swing in analog circuits, and limits the achievable SNR. The input signal swing is also reduced due to the reduced supply voltage which in turn requires the reduction of noise floor to maintain the same dynamic range. Lowering the noise floor increases the chip area and power consumption for analog circuits. Third, device leakage and distortion are increased. For signal path switches in analog circuits, the ON-resistance variation introduces distortion in analog circuit at ULV operation. For a switch driven by amplifier, the drain-to-source leakage in OFF switch state can lower the output resistance of the amplifier and limit its DC gain. Fourth, analog circuits are more sensitive to process variation, voltage and temperature fluctuation at ULV operation. The circuit performance exhibits much wider variability because precise control of chip manufacturing becomes increasingly difficult and expensive in the nanometer region. In summary, design of high performance analog circuits becomes progressively harder at ULV operation.

Analog-to-digital converter (ADC) is a universal block in mixed-signal integrated circuits and systems. As an interface between analog world and digital systems as shown in Fig 1.2, an ADC is often integrated with a larger digital circuit on the same chip. Thus when the digital

portion of the chip operates from an ultra-low supply voltage, ULV operation is also required for the ADC if the benefits of using a single V_{DD} overweigh the overhead associated with multi-V_{DD} solutions.

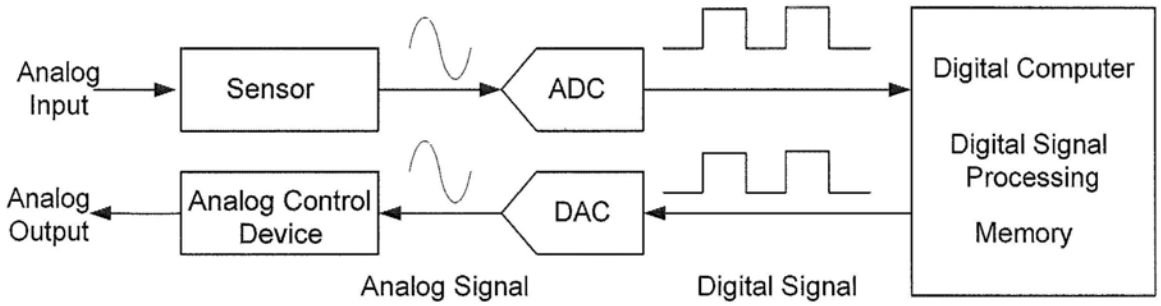


Fig 1.2 ADC behaves as the interface between analog world and digital systems.

The rapid growth of products in wireless and wire line communications is the driving force for higher specifications of ADCs. For example, for applications in wireless communications, a high dynamic range ADC is needed as the applications utilize large portions of bandwidth. It is more challenging to design high-resolution Nyquist converters due to the limited dynamic range at ULV operation. The Delta Sigma ($\Delta\Sigma$) ADC [7] is widely used for high precision applications with low to medium speed requirements, like sensor interfaces, audio interfaces, and mobile communications. However, it is challenging to design ULV high performance $\Delta\Sigma$ ADC due to some crucial problems. On one hand, the reduction of supply voltage limits the headroom for devices, such as output swing, which makes the distortion problem worse [8]. On the other hand, the non-idealities of building blocks become the bottleneck of ULV high performance $\Delta\Sigma$ ADC, such as finite gain, finite bandwidth of OTA, distortion of switches, non-linearity of feedback digital to analog converter (DAC). In a word, increasing the power consumption can solve those problems, while the low power solution of the whole mixed-signal system restricts the power consumption of the $\Delta\Sigma$ ADC. The main objective

of this research is to design high-performance ΔΣ ADCs operating under a nominal supply of 0.5V. The targeted SNDR is 90dB for an audio signal bandwidth, higher than any reported ΔΣ ADCs in this supply range.

1.2 Literature Review

A ΔΣ ADC block diagram is shown in Fig 1.3, it converts the analog input $x_{in}(t)$ to digital signal $y_{dsm}(n)$, which is further processed to obtain the final digital code $y_s(n)$ at Nyquist rate. The anti-aliasing filter is to prevent the aliasing by filtering the input signal around and beyond the sampling frequency. There are two types of ΔΣ modulator: discrete-time (DT) and continuous-time (CT). For a DT modulator, the sampling function is performed before the noise-shaping loop, while for a CT modulator, the sampling operation happens after the loop filter. The CT modulator thus has inherent anti-aliasing function [9]. After the decimation filter, the sampling rate is reduced to the Nyquist rate, and the out of band quantization noise is suppressed.

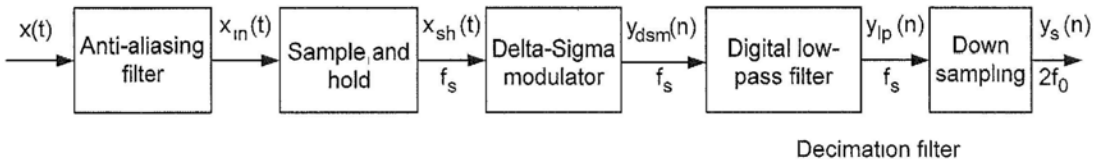


Fig 1.3 Block diagram for ΔΣ ADC.

The ΔΣ modulator is the main analog block of ΔΣ ADC, therefore design a low-voltage, low-power ΔΣ modulator is a key factor in successful design of ULV high performance ΔΣ ADC. Table 1.1 compares recently reported low voltage ΔΣ modulators. Many of these researches focuses on DT modulators, such as the switched-capacitor (SC) ones in [20]-[21] or the switched-current (SI) ones in [23]-[24]. DT ΔΣ modulators, however, have crucial limitations when operating at low voltage supply especially 0.5V or below, such as low resolution, high power consumption compared with CT modulators. For a SC integrator, the power dissipation is

higher than that of a CT integrator as the integrator's output changes faster; and the switches in the signal path are not easy to implement at ULV operation without internal voltage boosting which may harm reliability [10]. The 0.6-V SC audio-band Delta-Sigma modulator (DSM) proposed in [20] uses resistors to replace the signal-path floating switches, but a tradeoff between distortion and sampling accuracy arises. In [21], a 0.6-V SC audio-band DSM was reported with sub-threshold leakage suppression switches. However its signal-path switches remain a hurdle for lower supply operation. For SI integrators, the input current swing is limited due to the smaller overdrive voltage and the channel length modulation is severe at ULV operation. CT integrator is more suitable for ULV ΔΣ modulator design. The advantages of CT ΔΣ modulator over DT counterpart are obviously [25]. First, the restrictions on OTA bandwidths and slew rate (SR) are relaxed for CT ΔΣ modulator. Second, smaller glitches appear on OTA virtual ground nodes for CT ΔΣ modulator as the input signal is always connected to virtual ground through a resistor other than switch. Third, there is no need for extra anti-aliasing filter in CT ΔΣ modulator as it has built-in anti-aliasing filter. Finally, CT ΔΣ modulator is suitable for ULV design as there are no switches in the signal path.

However, the CT ΔΣ modulator is more sensitive to clock jitter [26]-[28] than the DT ΔΣ modulator, which in turn limits the peak signal to noise and distortion ratio (SNDR) when operating at ultra-low supply voltage. The CT ΔΣ modulator is also sensitive the absolute value of resistors and capacitors, which affect the noise transfer function, and degrades the signal to quantization noise ratio (SQNR). It is not difficult to solve the large RC product variation problem. For the cascaded CT ΔΣ modulator, digital calibration method can be used to solve the problem.

Table 1.1 Performance comparison of low supply voltage modulators

	V_{DD} [V]	$\|V_T\|$ [V]	Type	BW [kHz]	Fs [MHz]	order	SNDR [dB]	Power [uW]	CMOS [um]	FoM [pJ/conv.]
Ortmanns 2002 [11]	1.5	0.58/ 0.62	CT 1bit NRZ/ SCR	25	2.4	3	71/72	250	0.5	1.73
Samid 2003 [12]	1.5	0.58/ 0.62	CT 1bit NRZ	50	3.2	3	60	50	0.5	0.614
Dorrer 2006 [13]	1.2	NA	CT 4bit RZ	20	12	2	74	2200	0.065	13.43
Pun 2007 [14]	0.5	0.5	CT 1bit RO	25	3.2	3	74	300	0.18	1.46
Yao 2004 [15]	1	NA	SC 1bit	20	4	3	81	140	0.09	0.382
Dessouky 2001 [16]	1	0.58/ 0.6	SC 1bit	25	5	3	85	950	0.35	0.654
Keskin 2002 [17]	1	0.55	SO 1bit	20	10.24	2	77.8	5600	0.35	22.6
Peluso 1998 [18]	0.9	0.55/ 0.62	SO 1bit	16	1.538	3	62	40	0.5	1.22
Sauerbrey 2002 [19]	0.7	0.43/ 0.38	SO 1bit	8	1.024	2	67	80	0.18	2.73
Ahn 2005 [20]	0.6	0.34/ 0.31	SRC 1/1.5bit	24	3.072	2-2	77	1000	0.35	3.6
Roh 2009 [21]	0.6	0.2/ 0.15	SC	20	1.92	5	81	34	0.13	0.092
Ishida 2006 [22]	0.5	0.1	SC 1bit	8	2	1	39.6	75	0.15	60.1
Tan 1995[23]	1.2	0.84/ 0.73	SI	10	1	2	51	780	0.8	152.3
Lee 2006[24]	0.8	NA	SI	5	0.64	2	47.5	180	0.18	92.8

SO=Switched Opamp; CT=Continuous Time;
SC=Switched Capacitor; SRC=Switched-RC;
SI=Switched Current; SCR feedback=Switched-Capacitor-resistor feedback.
#: If V_{TN} and $|V_{TP}|$ are different, then two values are given as $V_{TN}/|V_{TP}|$.

The clock jitter is an important problem in ULV high performance CT ΔΣ modulator design. In [14] a continuous-time (CT) 0.5V audio-band Delta-Sigma modulator with a return-to-open feedback DAC to eliminate signal paths switches is presented, but its performance remains sensitive to clock jitters.

1.3 Major Contributions

The major contributions of this research include the new design techniques and circuits state below for achieving high-performance ΔΣ modulators under an ultra-low supply of 0.5V.

First, a new method implementing SCR feedback under 0.5-V supply is developed to reduce the modulator's sensitivity to clock jitter. A key advantage of the circuit is that it does not cause any common-mode transient disturbance.

Second, a new synthesis method for cascaded CT ΔΣ modulator is proposed. It employs only one forward signal path, and the digital cancellation logics can be easily derived as the derivation is based on DT domain analysis. This new synthesis method leads to simple implementation of circuits and the digital correction of RC product variation.

Third, new building block circuits enabling the realization of the 0.5-V modulators are developed. They include two 0.5-V amplifiers. The first one is a 0.5-V fully differential gate-input amplifier with adaptive CMFB frequency compensation. Another one is a 0.5-V fully differential gate-body-input class-AB amplifier with enhanced slew-rate performance. A RC product detection circuit is also proposed for off-chip digital correction of RC product variation.

Two modulator chips are fabricated in a 0.13μm CMOS process using these proposed circuits. The first 0.5-V audio-band CT 3rd order CIFB ΔΣ modulator is implemented with SCR feedback. Measurement results show that the modulator achieves an excellent SFDR of 93.9dB and a SNDR of 81.2dB over 25-kHz signal bandwidth while consuming only 625μW at 0.5V.

The second one is a 0.5V CT 3rd order CIFF ΔΣ modulator. The measured SFDR, SNDR and SNR are 101.9dB, 87.76dB and 87.96dB respectively over 25-kHz signal bandwidth. The chip consumes 682.5 μW at 0.5-V. To the best of our knowledge, this performance is the best compared to other modulators operating in this supply voltage range. Both modulators perform consistently over wide voltage and temperature ranges.

1.4 Thesis Outline

The outline of the thesis is as follows. Chapter 2 reviews the basic operating principle and performance parameters of ΔΣ modulators. The single loop and cascaded ΔΣ modulators are presented. The discrete-time to continuous-time conversion is also introduced. Clock jitter noise in continuous time ΔΣ modulators and the techniques to reduce the clock jitter effect are discussed. Chapter 3 presents the design, implementation and experimental results of 0.5V high performance continuous time ΔΣ modulator with a new method implementing switched-capacitor-resistor (SCR) feedback. In Chapter 4, a 0.5V 3rd order Cascaded of Integrators Feed Forward (CIFF) continuous time ΔΣ modulator is introduced, and the details of system design, circuit implementation and measurement results are described. In Chapter 5, a 0.5V 2-1 cascaded CT ΔΣ modulator with SCR feedback is proposed. A new synthesis method is presented. Finally, conclusions and future work are given in Chapter 6.

Chapter 2

Oversampling Delta-Sigma Modulators Design Overview

This chapter reviews the basic principles, synthesis methods, and circuit non-idealities reduction techniques for ΔΣ modulators.

2.1 Overview

2.1.1 Operating Principles of ΔΣ Modulators

As shown in Fig 2.1, a ΔΣ modulator is a negative feedback system composed of a loop filter H(z), a quantizer and a feedback digital-to-analog converter (DAC). At low frequencies, the loop gain |H(z)| is very high and the negative feedback forces the output signal Y(n) to track the input signal X(n) very closely. The quantization noise is greatly reduced at low frequencies. At high frequency, the loop gain |H(z)| is low and the quantization noise is not suppressed. The quantization noise is thus spectrally shaped.

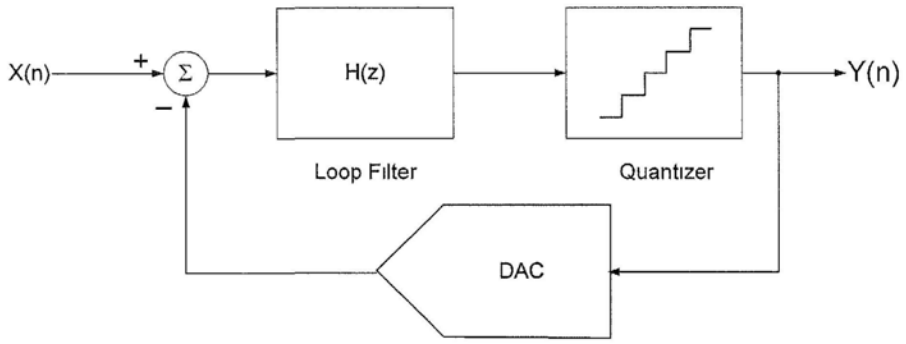


Fig 2.1 Basic diagram of ΔΣ modulator.

Fig 2.2 shows a modulator model with the quantizer replaced by a linear model. The quantization noise *E(n)* is independent of the input signal of the modulator. The output signal *Y(n)* can be written in terms of *X(n)* and *E(n)*:

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \tag{2.1}$$

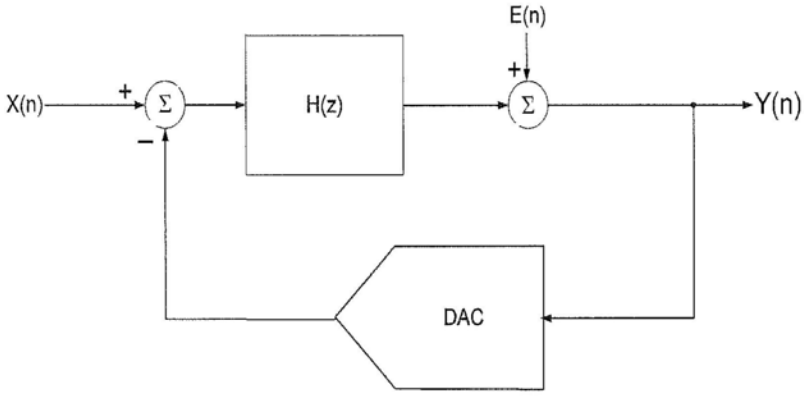


Fig 2.2 ΔΣ modulator with linearized quantizer model.

Here the signal transfer function (STF) and noise transfer function (NTF) are written as:

$$STF(z) = \frac{H(z)}{1+H(z)},\ NTF(z) = \frac{1}{1+H(z)} \tag{2.2}$$

If the H(z) is chosen such that its magnitude is large over the signal band, then STF(z)≈1 and NTF(z)≈0 over the signal band, which ensures Y(z)≈X(z) for any frequency within the signal band.

2.1.2 Oversampling

The quantizer is operates at discrete times with a sampling frequency f_s. For ΔΣ modulators, f_s is much higher than Nyquist rate, denoted as f_N here. For a signal band limited to f_B, the f_N is $2f_B$, and the oversampling ratio (OSR) is defined as:

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_B} \tag{2.3}$$

Assume the quantization error is random and has a white-noise-like behavior, it can be shown that the total quantization noise power equals to $\frac{\Delta^2}{12}$, where Δ is the quantization step size. It is interest to note that the quantization noise power is a function of Δ only, independent of the sampling frequency. For no oversampling, i.e., f_s=f_N, the quantization noise energy is evenly distributed within $\pm f_N/2$ due to aliasing, as shown in Fig 2.3. In oversampling cases (OSR>>1),

only a portion of the quantization noise power falls in the signal band as shown in Fig 2.4. The total quantization noise power in Fig 2.3 and Fig 2.4 are the same.

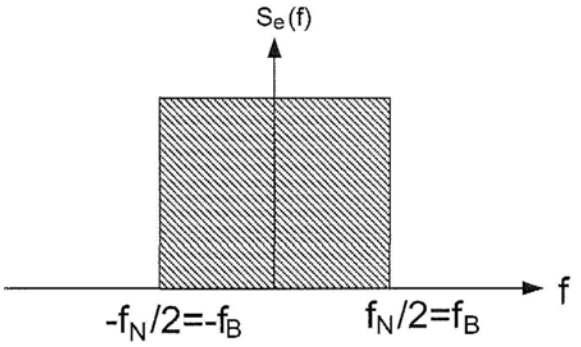


Fig 2.3 Quantization noise spectral density in a Nyquist converter.

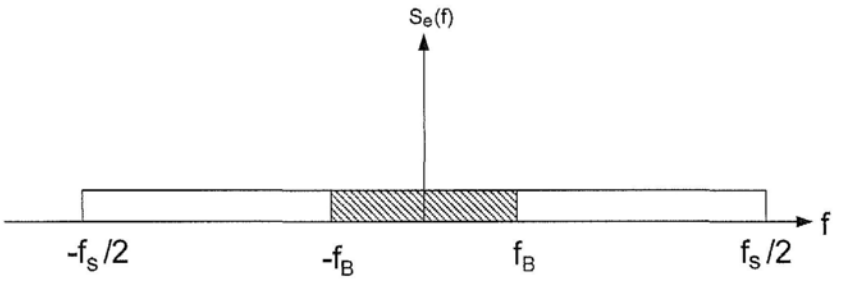


Fig 2.4 Quantization noise spectral density in an oversampling converter.

The noise power spectral density of the oversampling converter is:

$$S_e^2(f) = \frac{\Delta^2}{12}\frac{1}{f_s} \tag{2.4}$$

The high frequency quantization noise is above f_B, so the quantization noise power within signal band is reduced to:

$$P_e = \int_{-f_B}^{f_B} S_e^2(f)df = \frac{\Delta^2}{12}\frac{2f_B}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.5}$$

The oversampling operation alone reduces the quantization noise power by a factor of OSR. Doubling the OSR will result in a 3dB reduction in P_e, or equivalently, a 0.5-bit increase in resolution. This explains how a ΔΣ modulator achieves high resolution at the cost of higher speed requirement. The signal to quantization noise ratio of ΔΣ modulator, evaluated in dB, is [25]:

$$SQNR_{oversampling} = 10\log\frac{A^2/2}{P_e} = 10\log\frac{A^2/2}{(\Delta^2/12)/OSR} = SQNR_{Nyquist} 10\log(OSR) \qquad (2.6)$$

where A is the amplitude of a full-scale input sinusoidal wave.

On the other hand, the requirement of the anti-aliasing filters is relaxed due to the oversampling technique. As shown in Fig 2.5, the transition band in oversampling is much larger than in Nyquist sampling.

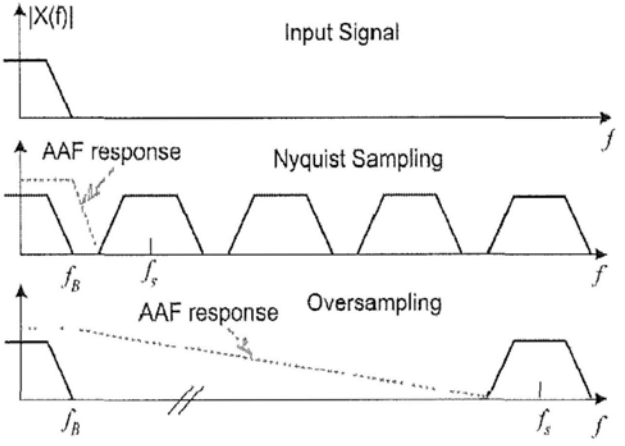


Fig 2.5 Anti-aliasing filter requirement in Nyquist converter and oversampling converter.

2.1.3 Noise shaping

Just by oversampling the SQNR improvement is quite limited. The SQNR can be further improved by further shaping the quantization noise in frequency domain.

The loop filter H(z) in Fig 2.1 is used to spectrally shape the quantization noise. From Eq. (2.2), it is obvious that the STF(z) is different from NTF(z). If H(z) is designed to have a large magnitude within the signal band and small magnitude outside the signal band, then in the signal band, the STF(z) and NTF(z) become:

$$STF(z) = 1,\ NTF(z) = \frac{1}{1+H(z)} << 1 \tag{2.7}$$

Thus, the quantization noise is greatly attenuated in the signal band; most of the noise power locates outside the signal band. The out-of-band quantization noise can be removed conveniently by a digital filter.

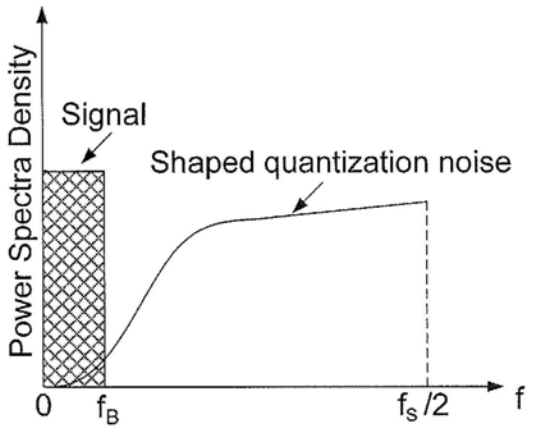


Fig 2.6 Output spectra of ΔΣ modulator.

Fig 2.6 depicts a shaped quantization noise spectrum of a ΔΣ modulator. In general, for a L^{th}-order modulation, the NTF(z) has a form of $(1-z^{-1})^L$; the in-band noise power can be readily estimated as [26]:

$$q^2_{rms} = \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)}\frac{1}{(OSR)^{2L+1}} \tag{2.8}$$

For a 1st order modulation, 9dB SQNR improvement is gained for each doubling of f_s. For a 2nd order modulation, 15dB SQNR improvement is gained for each doubling of f_s. For a Lth -order modulation, the total improvement of SQNR is (6L+3) dB, that is, (L+0.5) bit gain in resolution.

In summary, the oversampling technique is used to reduce the quantization noise in the signal band. Spectral shaping is used to further lower the in-band quantization noise power. These two techniques together improve the SQNR of ΔΣ modulator dramatically.

2.2 Performance Parameters of ΔΣ modulators

There are several performance parameters to evaluate the performance of ΔΣ modulator. These parameters characterize the dynamic performance of ΔΣ modulator.

2.2.1 Signal-to-Noise Ratio (SNR)

The noise of a practical ΔΣ modulator includes not only quantization noise, but also circuit noises like thermal noise and *1/f* noise. The SNR is calculated as:

$$SNR = 10\log(\frac{Psig}{Pnoise}) \tag{2.9}$$

For N-bit ADC, assume the quantization noise is dominated in the noise floor, the maximum SNR or SQNR can be determined. Quantization error can be viewed as being "random", and is often referred to as "noise", the total quantization noise power equals to $\frac{\Delta^2}{12}\frac{1}{OSR}$, and the maximum signal power is:

$$P_{sig} = \frac{A^2}{2} = 2^{2N-3}\Delta^2 \tag{2.10}$$

where A is the maximum amplitude of a sine wave, it equals to $2^{N-1}\Delta$.

The maximum SNR equals:

$$SNR_{\max} = SQNR_{\max} = 10\log(\frac{2^{2N-3}\Delta^2}{(\Delta^2/12)/OSR}) = 6.02N + 1.76 + 10\log(OSR) \text{ dB} \quad (2.11)$$

2.2.2 Signal-to-Noise and Distortion Ratio (SNDR)

The SNDR of ΔΣ modulator is the ratio of signal power to the noise and harmonics power, which is calculated as:

$$SNDR = 10\log(\frac{P_{sig}}{P_{noise} + P_{distortion}}) \quad (2.12)$$

SNDR includes quantization error, linearity, distortion, jitter, glitches, noise, setting time, etc. The SNDR characterizes the linear performance of the ΔΣ modulator, and is smaller than SNR when the input signal is large. It's due to the distortion effect of components.

2.2.3 Effective Number of Bits (ENOB)

The ENOB measures the real resolution of the converter. It is a metric based on the peak SNDR of the converter. ENOB is defined as:

$$ENOB = \frac{SNDR_{\max} - 1.76}{6.02} \text{ [number of bits]} \quad (2.13)$$

ENOB depends on input frequency in general.

2.2.4 Dynamic Range (DR)

The DR is the ratio between the maximum possible input signal amplitude and the minimum detectable input signal amplitude [27].

The SNR, SNDR and DR are illustrated in Fig 2.7 which is from measured results of practical ΔΣ modulator. The figure shows that the SNDR is nearly the same as SNR at small input signal amplitude. The SNR is nearly in linear relationship with the input signal amplitude.

The SNDR drops at large input signal amplitude due to the harmonics. The DR is measured from the peak SNR point to the 0dB SNR point.

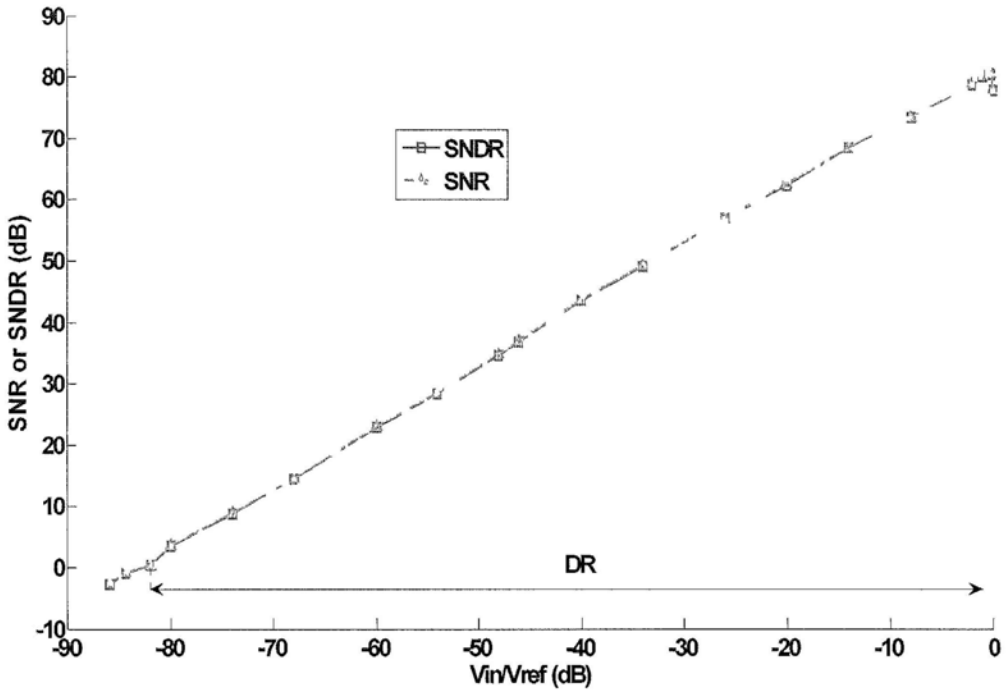


Fig 2.7 SNR and SNDR plot for a practical ΔΣ modulator.

2.2.5 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the maximum signal component and the largest distortion component. **Error! Reference source not found.** shows the frequency spectrum of practical ΔΣ modulator. The definition of performance metrics such as SNR, SFDR are clearly shown in this figure. If the converter has good linearity, the SFDR will be higher than SNR.

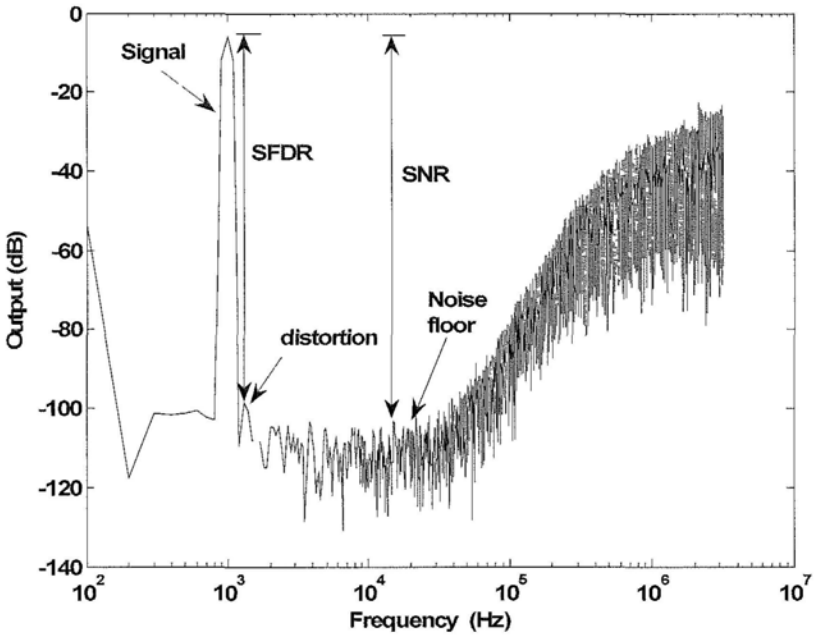


Fig 2.8 Frequency spectrum of a practical ΔΣ modulator.

2.3 Topologies of ΔΣ modulators

ΔΣ modulators can be grouped into two types of architectures, the single-loop ΔΣ modulator and the multi-stage ΔΣ modulator (also named cascaded ΔΣ modulator). These two architectures are compared in this section.

2.3.1 Single-loop ΔΣ Modulator

The single-loop ΔΣ modulator, also called single-stage ΔΣ modulator, contains only one quantizer. Fig 2.9 shows a typical single-loop ΔΣ modulator with distributed feedback.

From Fig 2.9, the loop filter transfer function can be calculated as:

$$H(z) = \sum_{i=1}^{n} k_i \prod_{j=i}^{n} k_{vj} H_j(z) \tag{2.14}$$

The noise transfer function and signal transfer function are:

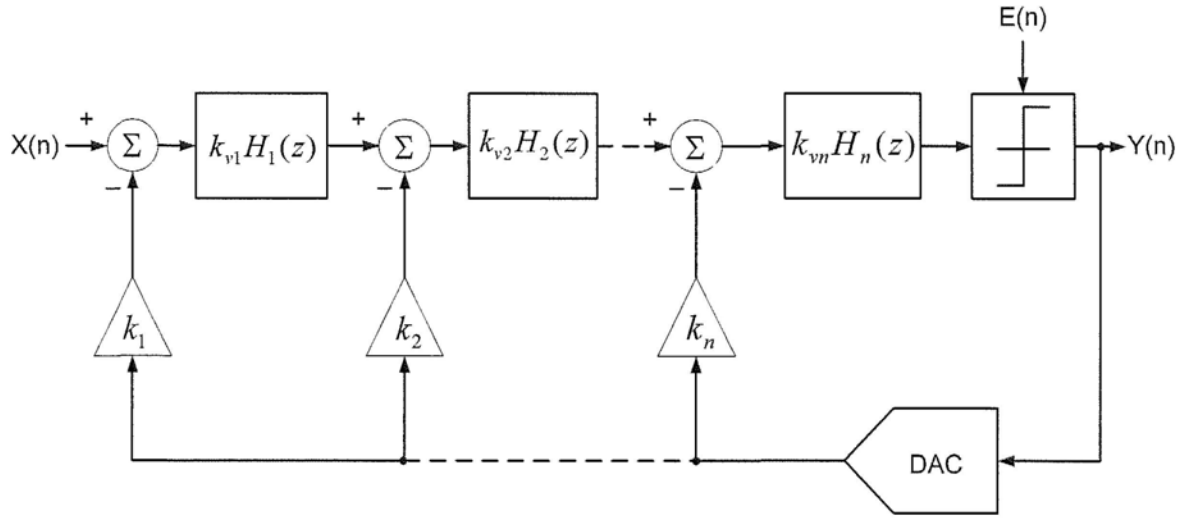


Fig 2.9 Block of distributed feedback single-loop ΔΣ modulator.

$$NTF(z) = \frac{1}{1 + \sum_{i=1}^{n} k_i \prod_{j=i}^{n} k_{vj} H_j(z)} \tag{2.15}$$

$$STF(z) = \frac{\prod_{i=1}^{n} k_{vi} H_i(z)}{1 + \sum_{i=1}^{n} k_i \prod_{j=i}^{n} k_{vj} H_j(z)} \tag{2.16}$$

The coefficient k_i is called the feedback loop coefficient, and the coefficient k_{vi} is called the signal path coefficient. Like other high order feedback systems, a high order single-stage ΔΣ modulator can be unstable. In the synthesis of single-stage high order 1-bit modulator, a general rule of thumb for stability is that the noise transfer function should satisfy the following requirement [26]:

$$H_{NTF}(e^{j\omega}) \le 1.5 \text{ for } 0 \le \omega \le \pi \tag{2.17}$$

There are several ways to increase the maximum SNR over the signal band, such as increasing the OSR, or increasing the ΔΣ modulator order, or increasing the number of

quantization levels, each with their own drawbacks. The power consumption increases when increasing the sampling frequency f_s. The stability problem arises when the modulator order is greater than two. The feedback DAC's linearity problem emerges when the number of the quantizer decision level is more than one. For 1-bit modulator, precise component matching is not required as the 1-bit DAC is inherently linear. And the analog circuitry is simple for 1-bit ΔΣ modulator. For multi-bit modulator (Fig 2.10), a highly accurate internal DAC is required as the DAC's accuracy limits the linearity of the overall ΔΣ modulator. Moreover, more analog circuitry is needed in multi-bit ΔΣ modulator.

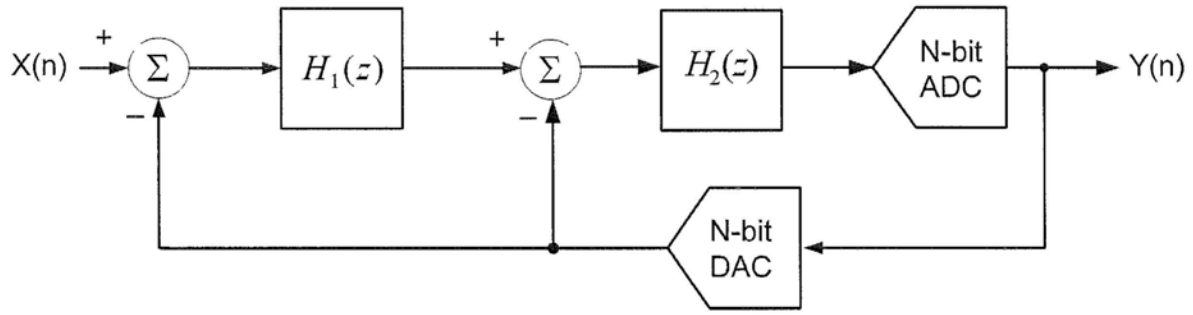


Fig 2.10 Single-loop N-bit ΔΣ modulator.

There are methods for improving the multi-bit DAC linearity, like component trimming [29]-[30], dynamic element matching (DEM) [31]-[34]. The principle of DEM is to spread out the mismatch-caused harmonic tones over the whole frequency band from DC to $f_s/2$. Digital correction methods [35]-[36] can also be used to correct the DAC nonlinearity.

2.3.2 Multi-Stage ΔΣ Modulator

The multi-stage (cascaded) ΔΣ Modulator topology was proposed in [37] to solve the stability problem of high order modulators. Fig 2.11 shows a block diagram of a two-stage ΔΣ modulator. The quantization noise of the first stage $E_1(n)$ is fed to the input of the second stage. The outputs of the two stages, $Y_1(n)$ and $Y_2(n)$, are then processed in digital circuits (including

two cancellation logics $CL_1(z)$, $CL_2(z)$) to cancel the quantization noise of first stage and to high-order shape the second stage's quantization noise.

Based on Fig 2.11, the output of first stage can be calculated:

$$Y_1(z) = \frac{H_1(z)}{1+H_1(z)} X(z) + \frac{1}{1+H_1(z)} E_1(z) \tag{2.18}$$

The output of second stage equals to:

$$Y_2(z) = \frac{H_2(z)}{1+H_2(z)} E_1(z) + \frac{1}{1+H_2(z)} E_2(z) \tag{2.19}$$

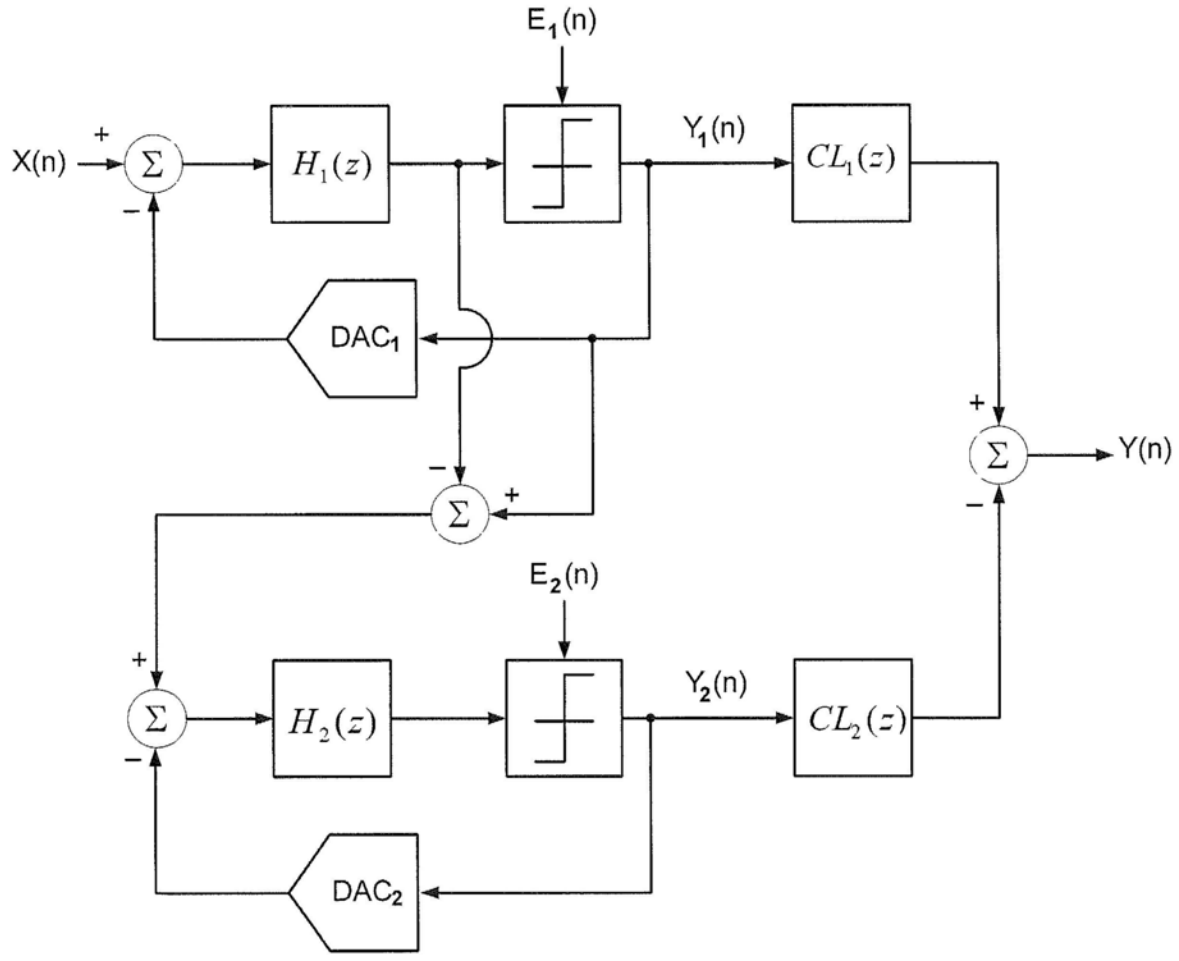


Fig 2.11 Block diagram of a two-stage cascaded ΔΣ modulator.

The final output of the cascaded ΔΣ modulator is:

$$Y(z) = Y_1(z)CL_1(z) - Y_2(z)CL_2(z) \tag{2.20}$$

The quantization noise of first stage can be completely cancelled if the following equation is satisfied:

$$\frac{CL_1(z)}{1+H_1(z)} = \frac{H_2(z)}{1+H_2(z)}CL_2(z) \tag{2.21}$$

The NTF of the second stage can be expressed as:

$$NTF(z) = -\frac{CL_2(z)}{1+H_2(z)} \tag{2.22}$$

Theoretically, the second stage quantization noise $E_2(n)$ can be high-order noise shaped when proper $H_2(z)$ and $CL_2(z)$ are chosen.

However, in practical circuit implementation, the performance of a cascaded ΔΣ modulator is limited by noise leakage. There are several factors resulting in noise leakage. The first one is mismatch between analog and digital circuitry, which results in incomplete cancellation of first stage quantization noise $E_1(n)$. The second one is imperfections of OTA, such as the finite DC gain, finite bandwidth. Digital calibration of modulator coefficients can mitigate the noise leakage problem [38].

In general, 1st order and 2nd order ΔΣ modulators are used in each stage of a multi-stage ΔΣ modulator for stability consideration. The first stage usually adopts a 2nd order sub-modulator as it can avoid the idle tone problem which happens in the 1st order ΔΣ modulator [28].

Compared to single-loop ΔΣ modulator, the loop-coefficients of cascaded ΔΣ modulator can be larger as it doesn't have the stability problem. This is a benefit when designing ULV ΔΣ modulators.

2.4 Synthesis of Continuous-Time Modulator

CT ΔΣ modulators are more suitable for ULV design than DT counterpart for several reasons, including relaxed OTA requirements, intrinsic anti-aliasing filtering, less distortion (as no switch exists in the signal path). This section presents a synthesis method to build a CT modulator from a DT prototype by impulse invariant transformation of the loop filter.

The DT to CT equivalence is achieved by ensuring the impulse responses of the DT and CT loop filters the same at the sampling moments. Fig 2.12 shows the closed-loop systems of CT and DT ΔΣ modulators. Once the loop is open at the input of DAC, an impulse input and a zero input are applied to the DAC and the modulator respectively. Then the DT and CT ΔΣ modulators are considered equivalent when their loop filter impulse responses are equal at the sampling moments. This means [39]:

$$Z^{-1}\{H(z)\} = L^{-1}\{R_D(s)H(s)\}|_{t=nTs} \tag{2.23}$$

where H(z) is the DT loop filter transfer function, *H(s)* is the CT loop filter transfer function, and $R_D(s)$ is the Laplace transform of the impulse response of the feedback DAC.

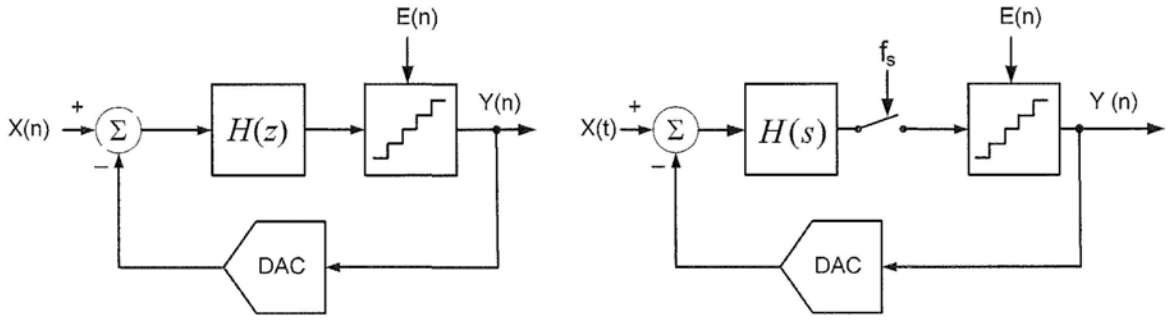


Fig 2.12 Closed-loop systems of DT and CT ΔΣ modulator.

In the time domain, this leads to the following equation [39]:

$$h(n) = [r_D(t) * h(t)]|_{t=nTs} = \int_{-\infty}^{+\infty} r_D(\tau)h(t-\tau)d\tau|_{t=nTs} \tag{2.24}$$

The steps of synthesizing a CT ΔΣ modulator from a DT ΔΣ modulator prototype are summarized below:

- First, choose a proper DT prototype NTF(z), and calculate a corresponding loop filter H(z);
- Next, get the CT loop filter H(s) by DT-to-CT impulse-invariant transformation of H(z);
- Finally, choose a proper architecture to implement H(s).

The DAC pulse shape should be chosen before the DT to CT transformation is processed. One important consideration in determining the CT DAC pulse shape is its sensitivity to clock jitter. Low jitter sensitivity DAC pulse shapes will be discussed later in this Chapter.

2.5 Jitter noise in continuous-time ΔΣ modulators

Jitter in CT modulators can be classified into pulse width jitter and pulse position jitter. The former is not shaped by the modulator loop and is directly imposed to the input signal, seriously degrading the performance of CT modulator [40]. This section analyzes the jitter noise effects in CT ΔΣ modulators and presents feedback DAC circuits to alleviate the effects.

2.5.1 Clock Jitter

Clock jitter is the uncertainty of the position or width of a pulse, it causes the variation of total amount of charge fed back in to the loop each clock cycle. This error is often called jitter noise. In a DT ΔΣ modulator, the clock jitter error at the sample-and-hold (S/H) circuit is dominant, and the total power of the jitter noise is [41]:

$$P_J|_{DT} = \frac{2\pi^2}{OSR}\left(\frac{\sigma_t}{T_s}\right)^2\left(\frac{f_{sig}}{f_s}\right)^2 A^2 \tag{2.25}$$

where A is the amplitude of sinusoid input signal, f_{sig} is the frequency of input signal, f_s is the sampling frequency of the modulator, σ_s^2 is the variance of clock jitter. The in-band-noise (IBN) induced by clock jitter is [42]:

$$IBN_J|_{DT} \approx \frac{\pi^2 A^2}{2OSR^3}\left(\frac{\sigma_t}{T_s}\right)^2 \tag{2.26}$$

However, in a CT ΔΣ modulator, the clock jitter happens at feedback DAC as well as the sampling circuit (quantizer). The clock jitter affects the total charge fed back into the loop and the quantization noise. The latter is spectrally shaped, and the former becomes dominant. CT ΔΣ modulators with rectangular feedback DAC pulse are very sensitive to clock jitter. Fig 2.13 depicts a single-loop L-th order CT ΔΣ modulator with a rectangular feedback waveform. k_l is the coefficient of each feedback branch, and k_{sig} is the input signal scaling coefficient, a_l is the coefficient of signal path. The jitter noise is induced at each feedback point, and the jitter induced IBN is found as [42]:

$$IBN_J|_{CT} = \frac{1}{k^2_{sig}}\left(\frac{N_{J,1}}{OSR} + \frac{\pi^2}{3}\frac{N_{J,2}}{OSR^3} + \ldots + \frac{\pi^{2(L-1)}}{2L-1}\frac{N_{J,L}}{OSR^{(2L-1)}}\right) \tag{2.27}$$

where $N_{J,l}$ is the equivalent jitter noise at each feedback point, it is evaluated as [42]:

$$N_{J,l} \approx \left(k_l \frac{\Delta}{2}\right)^2 \left(\frac{\sigma_t}{T_s}\right)^2 A_{DAC} \tag{2.28}$$

where Δ is step of feedback DAC, A_{DAC} is an activity factor. Obviously, the IBN of DT ΔΣ modulator is smaller than CT ΔΣ modulator as the former is rejected by cubic of OSR.

Fig 2.14 shows the clock jitter effect in a CT ΔΣ modulator with return to zero (RZ) or non-return to zero (NRZ) feedback DAC, where $0 \le \alpha < \beta \le 1$. The charge error Δq_{CT} is in proportional to the jitter error Δt.

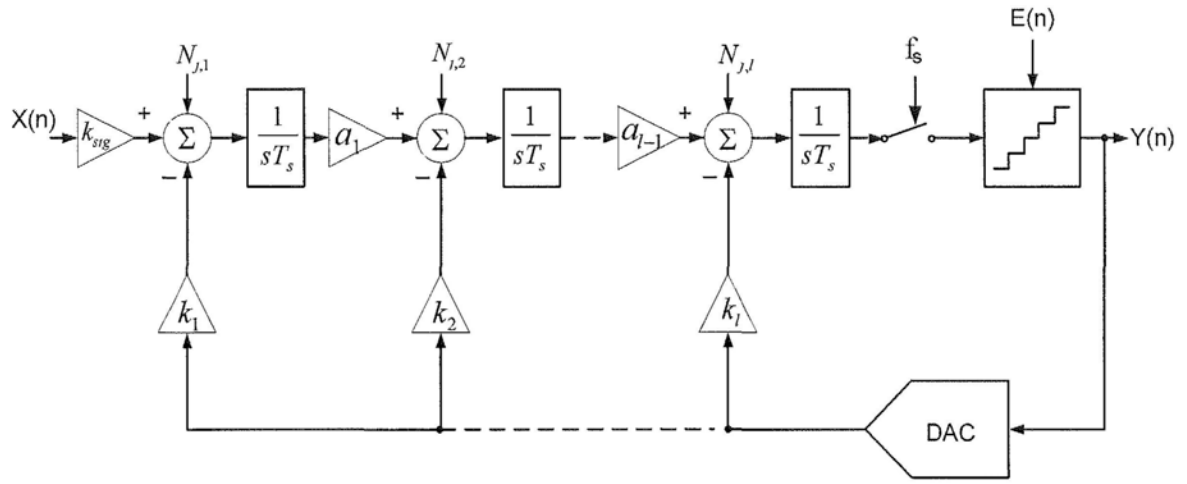


Fig 2.13 Single-loop L-th order CT ΔΣ modulator for jitter noise estimation.

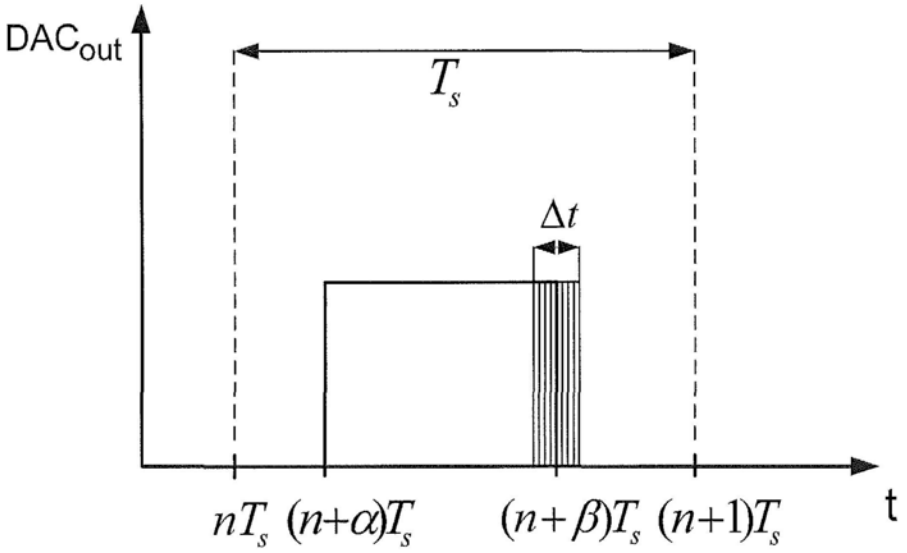


Fig 2.14 Clock jitter in CT ΔΣ modulator with rectangular feedback.

Fig 2.15 shows the jitter effect in a switched-capacitor (SC) DT ΔΣ modulator. Most charge is transferred to the loop at the beginning of each clock cycle, only little amount of charge Δq_{DT} is induced due to the clock jitter error Δt.

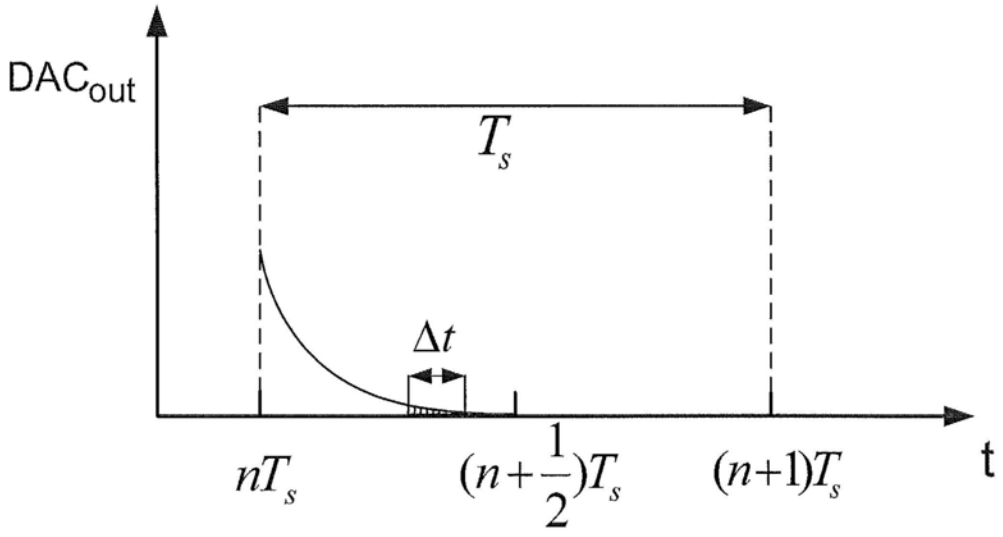


Fig 2.15 Clock jitter in SC DT ΔΣ modulator.

2.5.2 Methods to Reduce Clock Jitter in CT ΔΣ modulators

The error caused by clock jitter depends strongly on the shape of the DAC waveform. The small charge error in the SC DT ΔΣ modulator indicates that a ΔΣ modulator with exponentially decaying DAC waveform is less sensitive to clock jitter than one with rectangular DAC waveform. Several methods have been reported to tackle the jitter noise problem in CT ΔΣ modulators, including SC DAC, Sine-Shaped (SIN) DAC, Switched-Shaped-Current (SSI) DAC, and Switched-Capacitor-Resistor (SCR) DAC.

2.5.2.1 Switched-Capacitor DAC

SC feedback DAC for CT ΔΣ modulators was proposed in [43]. Fig 2.16 shows the scheme of a SC DAC. The capacitor is discharged to ground during phase ϕ_1, and charged to $+V_{ref}$ or $-V_{ref}$, depending on the output of quantizer, during phase ϕ_2. The output voltage DAC_{out} to the loop filter has an exponentially decaying shape, so the error charge injected to the modulator due to the jitter is small.

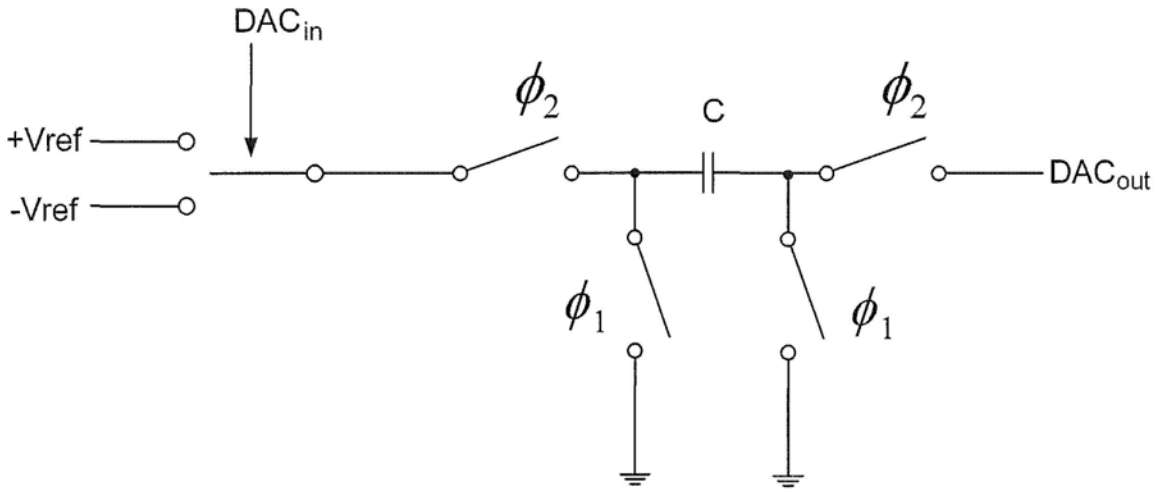


Fig 2.16 SC DAC.

Although a SC DAC can suppress the clock jitter effectively, it also has a higher peak current which results in higher requirement on the slew-rate (SR) and bandwidth for the amplifier used.

2.5.2.2 Sine-Shaped DAC

The SIN DAC waveform proposed in [44]-[45] is shown in Fig 2.17. For the SIN DAC waveform, pulse width jitter takes effect when the DAC output is at its minimum value as shown in Fig 2.18, thus the resulted error charge injected to the modulator loop is much smaller than that of the rectangular feedback DAC.

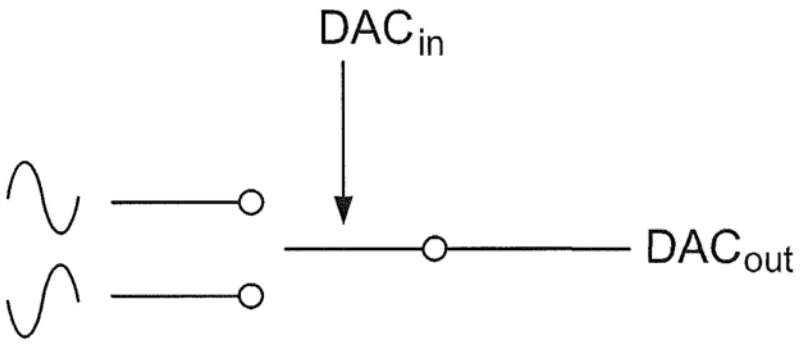


Fig 2.17 SIN DAC.

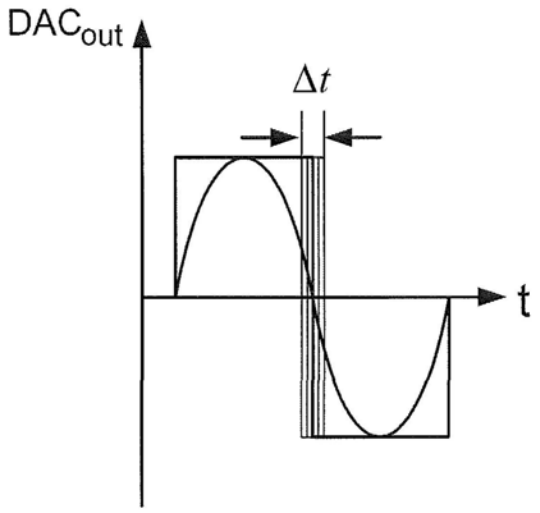


Fig 2.18 SIN DAC versus rectangular DAC in jitter reduction.

In general, jitter suppression of the SIN DAC is not as effective as the SC DAC. Besides, the SIN DAC is sensitive to pulse position jitter [46] and its circuit realization is very complicated [44].

2.5.2.3 Switched-Shaped-Current DAC

The SSI DAC is proposed in [46] to reduce the jitter noise without increasing the requirements on SR and UGB of the amplifier employed in the loop filter. The scheme of the SSI DAC is shown in Fig 2.19. The capacitor is charged to V_{ref} during phase ϕ_1, and discharged through the I_{ref1} branch during phase ϕ_2. The output current I_{SSI} is proportional to discharge current I_{ref1}. The voltage across capacitor V_C is the drain voltage of the transistor which generates I_{ref1}. With the decreasing of V_C, I_{ref1} decreases from almost constant value to zero as the transistor goes through saturation region, linear region and cutoff region.

The waveform of the output current is shown in Fig 2.20. In short, the SSI DAC generates an almost rectangular current in most time of a period and an exponentially decreased current in the end of a period. Obviously the peak current of the SSI DAC is smaller than the SC

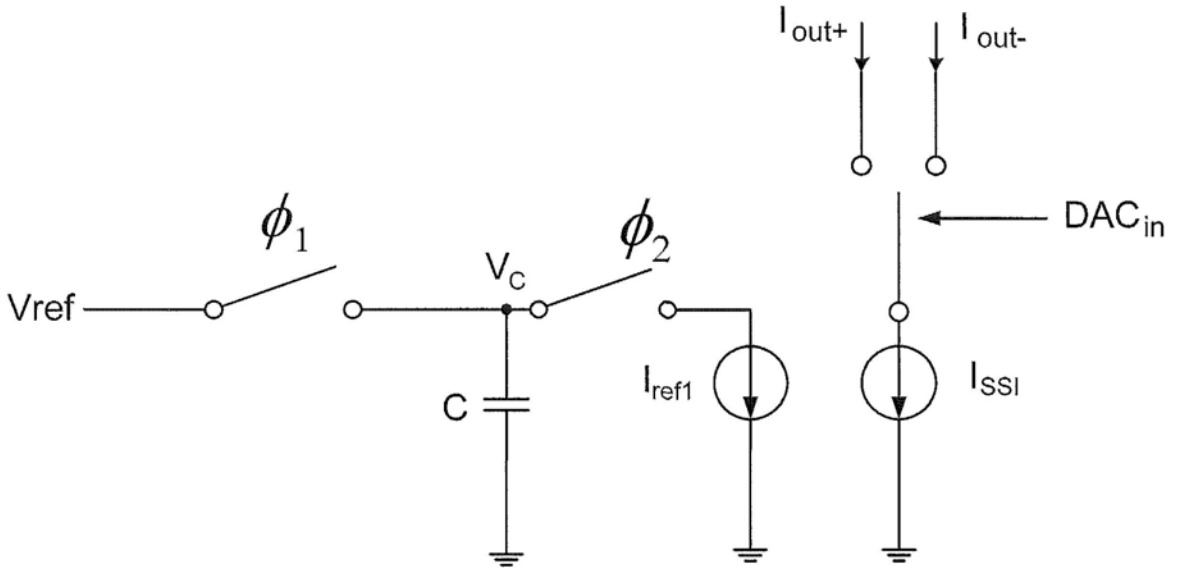


Fig 2.19 SSI DAC.

DAC. However, it is difficult to control the output current waveform depicted in Fig 2.20; tuning is needed. Moreover, the circuit implementation is more complicated than the SC DAC.

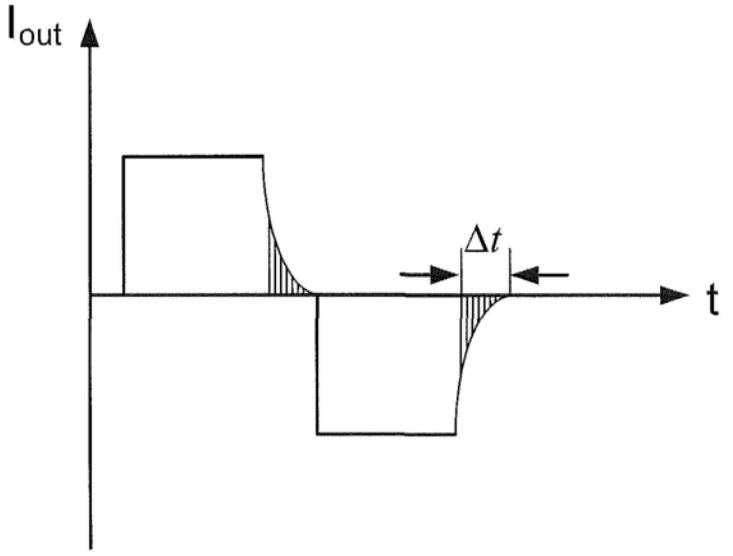


Fig 2.20 Output current waveform of SSI DAC.

2.5.2.4 Switched-Capacitor-Resistor DAC

To overcome the complexity of circuit implementation and the requirements on SR and UGB on amplifiers, the SCR DAC was proposed [47]-[48] and was further studied in [49]-[50]. Fig 2.21 shows a SCR DAC circuit. The capacitor is charged to $+V_{ref}$ or $-V_{ref}$ depending on the input of DAC during phase ϕ_1. The capacitor is discharged through resistor R during phase ϕ_2. The peak current is decreased to $V_{ref}/(R+R_{on})$, smaller than SC DAC peak current which is $V_{ref}/(2R_{on})$. R_{on} is the on-resistance of the switch controlled by ϕ_2. The discharge current is:

$$I = \frac{V_{ref}}{(R+R_{on})} e^{-\frac{t}{\tau}}, \qquad \tau = (R+R_{on}).C \tag{2.29}$$

The waveform of feedback voltage DAC_{out} is shown in Fig 2.22. The equivalent jitter noise $N_{J,i}$ of SCR DAC is approximately [42]:

$$N_{J,i}\,|_{SCR} \approx (k_i \frac{\Delta}{2} e^{-(\beta-\alpha)T_s/\tau})^2 (\frac{\sigma_t}{T_s})^2 \tag{2.30}$$

Compare (2.28) with (2.30), it's found that the SCR DAC has an exponential decreasing effect in jitter reduction. Smaller discharge time constant τ results in better jitter insensitivity and higher requirement on SR and UGB of amplifiers. So it is necessary to make compromise between

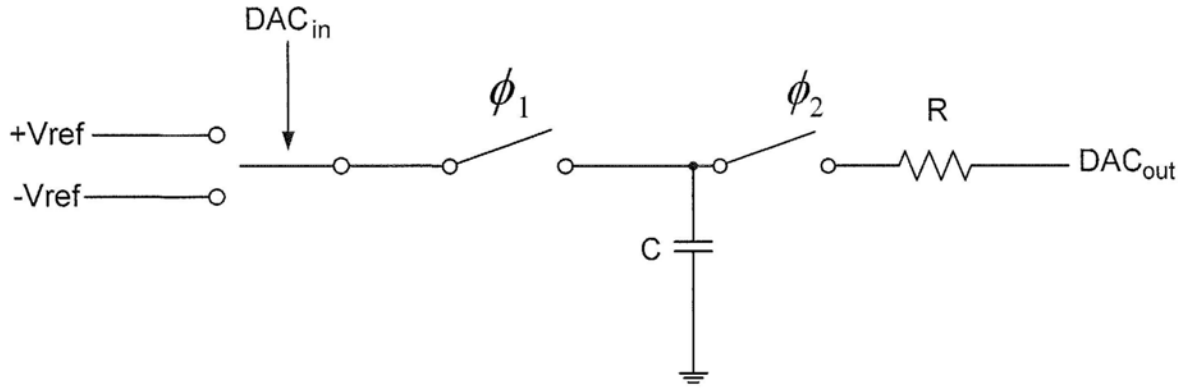


Fig 2.21 SCR DAC.

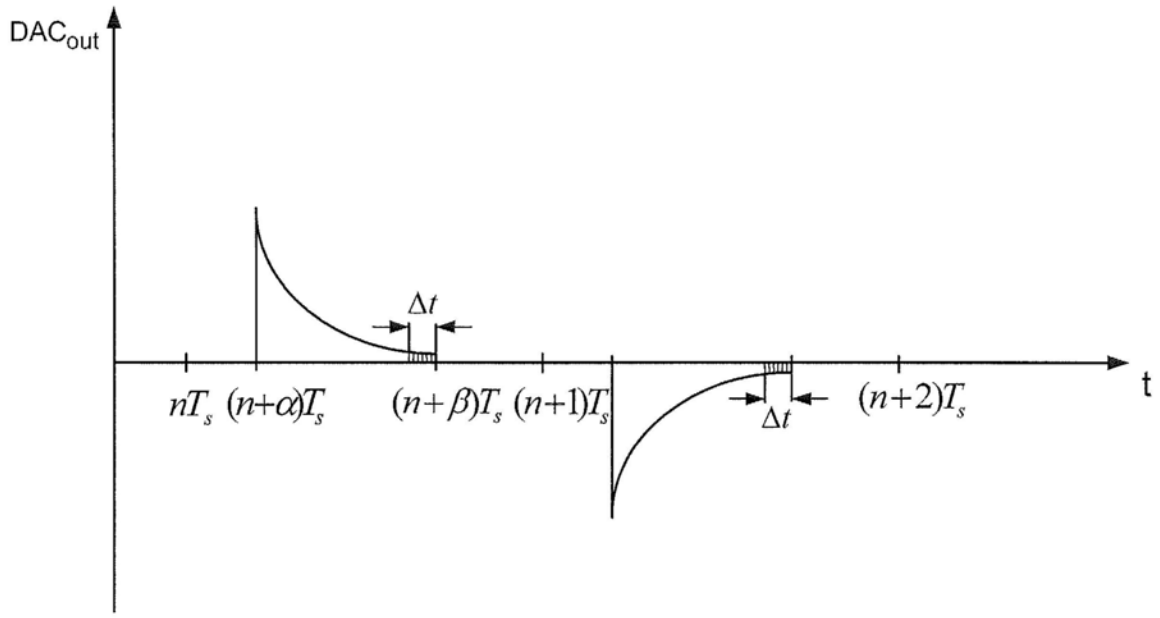


Fig 2.22 Output voltage waveform of the SCR DAC.

power consumption and the sensitivity to clock jitter when designing a low power CT ΔΣ modulator.

2.6 Summary

In this chapter, basic operating principles and important performance metrics of ΔΣ modulators are reviewed. It is discussed that the single-loop high-order ΔΣ modulator has potential stability problem while the multi-stage high-order ΔΣ modulator has quantization noise leakage problem. Synthesis of CT ΔΣ modulators through the impulse-invariant DT-to-CT transformation is presented. Ways to suppress the clock jitter effects are introduced. This chapter prepares us for the design of a high performance CT ΔΣ modulator with SCR feedback capable of ULV operation in Chapter 3.

Chapter 3

A 81.2dB SNDR Audio-Band Continuous-Time Delta-Sigma Modulator with SCR feedback at 0.5V

3.1 Introduction

As described in Chapter 1, the target performance of CT ΔΣ modulator is 90*dB* SNDR over 25*k*Hz signal bandwidth. However, CT ΔΣ modulators are sensitive to clock jitter [51]-[53], but techniques, such as SC or SCR feedback [54]-[56], are available for jitter noise reduction. In this 0.5V ΔΣ modulator architecture design, the SCR feedback DAC is adopted considering the difficulty in circuit realization, power consumption and the effectiveness in clock jitter noise reduction. The higher amplifier speed required to SCR feedback (compared to a regular CT feedback) is achieved with the wideband amplifier topology proposed in [57]. A proposed ULV comparator consisting of a body-input pre-amp and a gate-clocked latch is used in ΔΣ modulator. It's a single-bit quantizer without stringent matching requirement on linearity.

In this chapter, the system architecture and behavioral simulation results are detailed firstly. Then circuit implementation and the noise calculation are discussed. After that the details of building block circuits are illustrated. Finally measurement results are shown, followed by conclusions.

3.2 System Architecture and Behavioral Simulation

3.2.1 Architecture

To meet the target of 90*dB* SNDR over 25-*k*Hz bandwidth, the SQNR of the modulator should be larger than 90*dB* over process variation. A one-bit quantizer is chosen over a multi-bit

quantizer for the inherent linearity and simplicity of the former. Under a 0.5V supply, linearization of multi-bit DAC can be challenging and complex. The multi-bit implementation of a 0.5V modulator can be another good research topic, but is not the focus of this thesis. The sampling frequency (f_s) is chosen as 6.4*M*Hz, offering a 128x OSR. The resulted large OSR guarantees a satisfactory SQNR in the presence of large RC time-constant variations.

The synthesis of the CT modulator starts from the DT prototype in [58] with the following "optimal" third-order loop filter response:

$$H(z) = -\frac{0.5}{z-1} - \frac{0.25}{(z-1)^2} - \frac{0.05}{(z-1)^3} \tag{3.1}$$

A 3rd order distributed feedback architecture is selected for that its signal transfer function has no peaking in the high frequencies. Fig 3.1 shows the coefficients of the SCR CT modulator, synthesized by an impulse-invariant DT-to-CT transformation [42] of the DT loop filter response given in Eq. (3.1). The coefficients are derived after dynamic range scaling and input range scaling. The SCR DAC has a first-order RC decay waveform with a time constant equal to 5%T_s (T_s=1/f_s) so that the clock jitter noise is kept sufficiently below the quantization noise (detailed in sub-section 3.3.3). The SCR DAC is further designed to have a pulse width of 50%T_s and to become active 20%T_s after the sampling instant of the comparator to allow the latter to have sufficient time to settle so as to get correct output data.

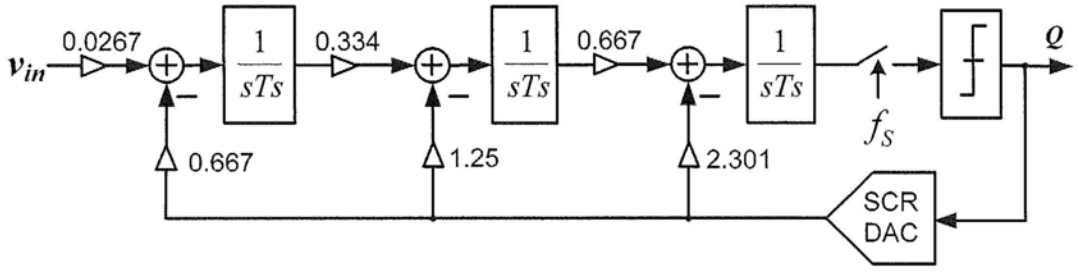


Fig 3.1 Modulator coefficients (f_s = 6.4MHz, T_s=1/f_s).

3.2.2 Behavioral Simulation

Fig 3.2 shows the Matlab Simulink^{TM} model of the synthesized CT modulator. Fig 3.3 shows the simulated power spectrum density (PSD) with V_{in} fixed at -0.35dB V_{FS} (V_{FS}=1$V_{pp,diff}$). The SQNR is 101dB under the setting of RC products having their nominal values.

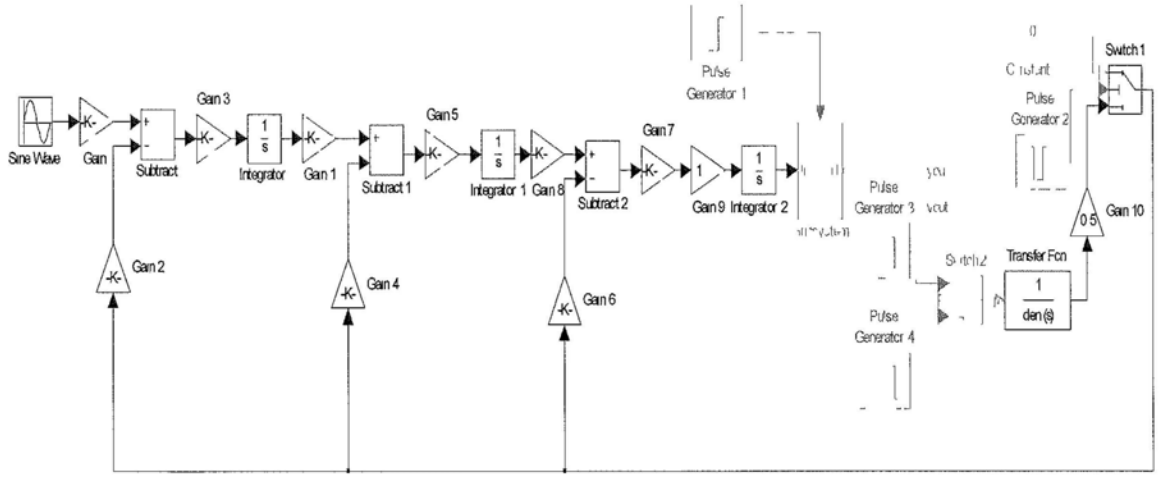


Fig 3.2 SimulinkTM model of the synthesized 3rd order CT ΔΣ modulator with SCR feedback.

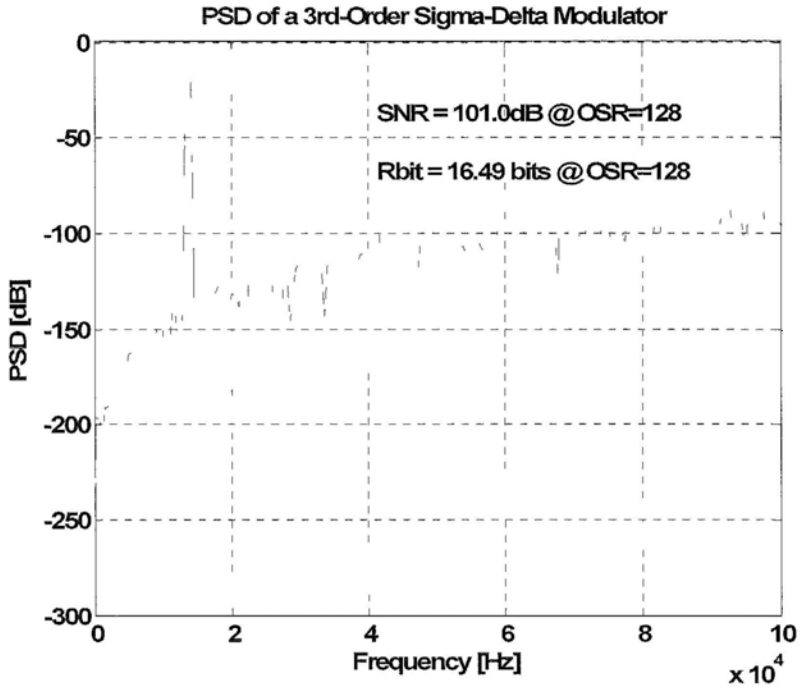


Fig 3.3 Matlab simulation result: Power Spectrum Density with V_{in} at –0.35dB V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

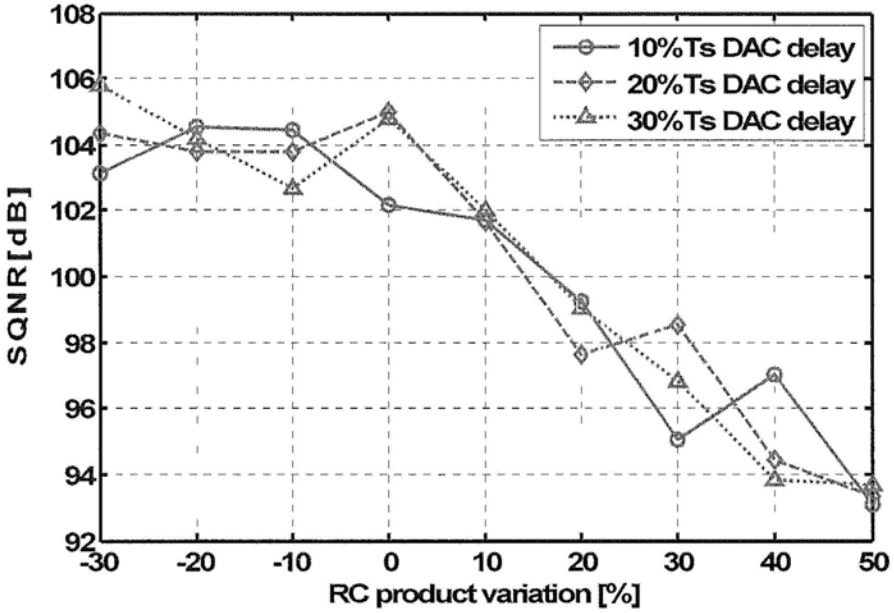


Fig 3.4 Matlab simulation results: SQNR versus RC product variation for different delay with V_{in} at -2dB V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

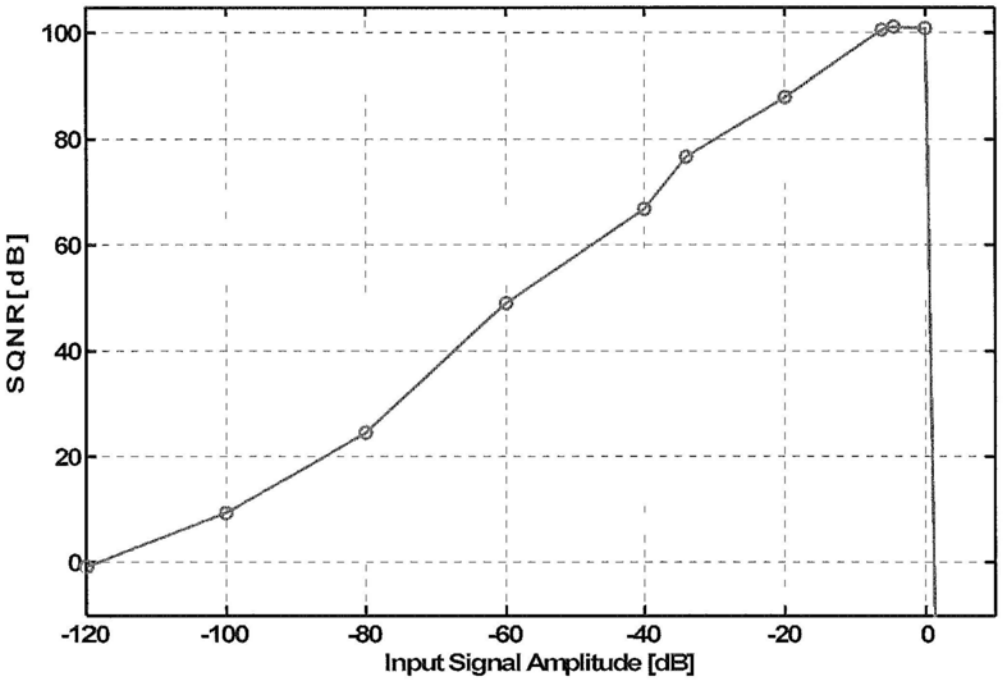


Fig 3.5 Matlab simulation results: SQNR versus V_{in}.

Fig 3.4 shows the simulated SQNR simulated with V_{in} fixed at -2dB V_{FS} as a function of RC product variation (from -70% to +150% of their nominal values). SQNR curves for different DAC delays are shown in the figure. The simulations demonstrate that the modulator maintains an SQNR better than 93dB over a large range of RC and DAC delay variations. Fig 3.5 shows the simulated SQNR as a function of input amplitude.

3.3 Circuit Implementation and Noise Analysis

3.3.1 Circuit Implementation

Fig 3.6 (a) presents a fully differential circuit of the proposed 0.5V CT ΔΣ modulator [59]. The resistors and capacitors values shown are those after dynamic range scaling and input range scaling (by varying the input resistor). The input signal can be up to $1V_{pp,diff}$ and the modulator is still stable. The smallest resistance in the modulator is 60$k\Omega$, presenting light DC load to (drawing less current from) the amplifiers. The integrating capacitors C_{1p} and C_{1n} of the first stage are relatively large to keep the thermal noise low (see section 3.3.2).

The modulator is designed in a 130nm CMOS technology with standard NMOS and PMOS V_T of 0.28V and -0.26V respectively. For these thresholds and V_{DD} = 0.5V, the normal way of setting the common-mode (CM) voltage ($V_{in,cm}$) at the amplifiers' inputs at $V_{DD}/2$ is not practical; the amplifier's input pair, constrained by reasonable W/L ratio, would not have sufficiently large g_m to obtain the speed required by the SCR feedback. Since the SCR pulse is designed to be fast, the integrator may not be able to follow. The unit-gain-bandwidth (UGB) of the amplifier is required to be $3\times f_s$ or more as not to significantly degrade the modulator performance [42].

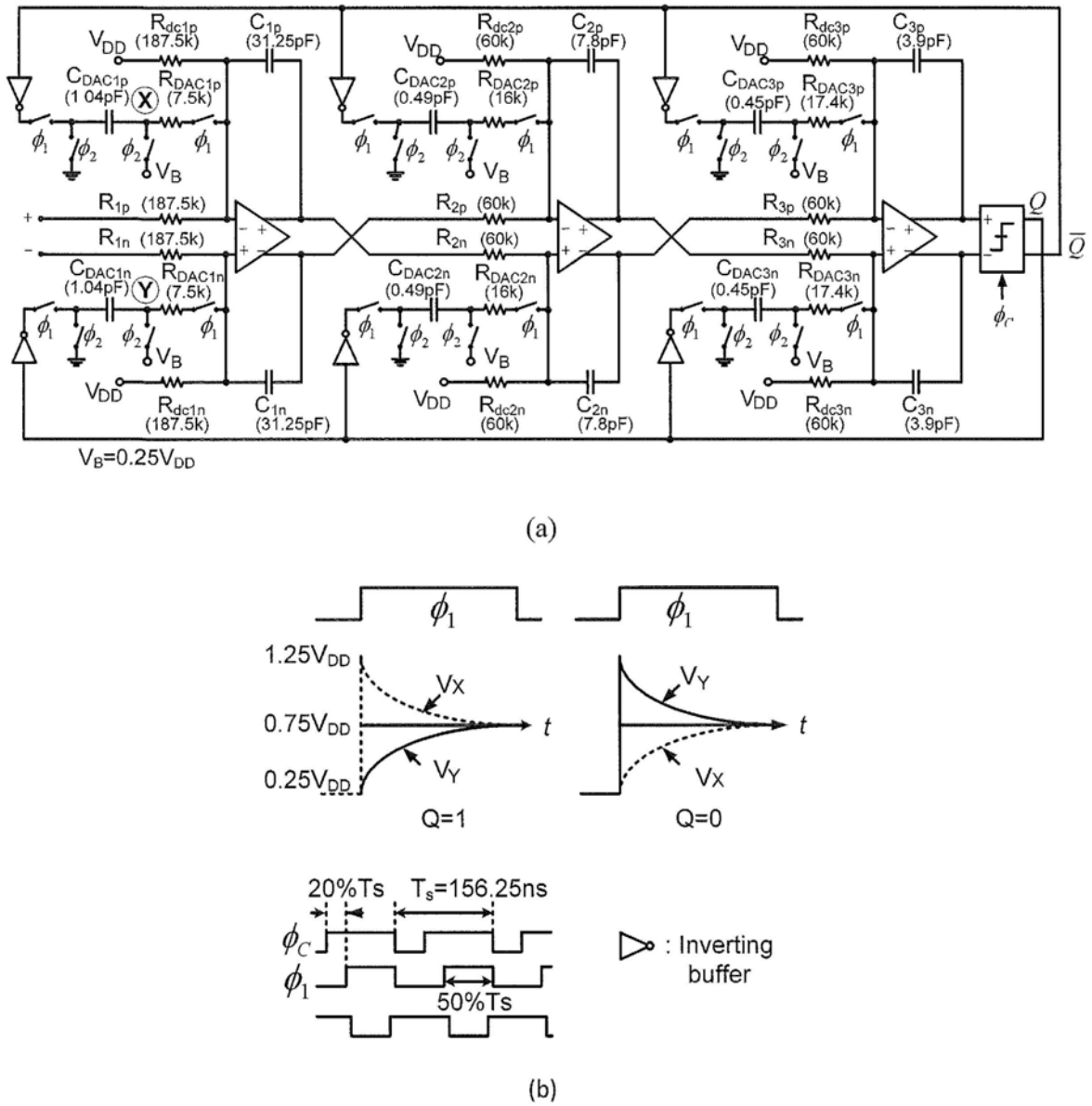


Fig 3.6 Proposed ULV 3rd order CT ΔΣ modulator with SCR feedback: (a) Schematic; (b) SCR waveform.

To overcome this problem, a new method implementing SCR feedback at 0.5-V supply is proposed. The $V_{in,cm}$ of the amplifiers is set to 0.75V_{DD} by a pair of resistors (R_{dc1p} and R_{dc1n} for the 1st stage) connected to a clean V_{DD}. The DC voltage V_B for the switches controlled by Φ_2 is set at 0.25V_{DD}. With these biasing settings, the $|V_{GS}|$ for the switches in the SCR feedback is at

least $0.75V_{DD}$ and they can be turned ON or OFF completely. The output CM voltage of the amplifiers is chosen to be $0.5V_{DD}$ to maximize the output swing.

In Fig 3.6 (b), the SCR waveforms at nodes X and Y are also shown. When Φ_2 is "high", V_X is charged to the initial value V_B ($0.25V_{DD}$). The comparator latches when Φ_C rises. After 20% T_s from the rise-edge of Φ_C, Φ_1 becomes "high" and the SCR feedback becomes active. If Q = 1, V_X jumps to $1.25V_{DD}$ and then decays towards $V_{in,cm}$ ($0.75V_{DD}$) with a time constant $\tau = R_{DAC1p}C_{DAC1p}$ (for the 1st stage). If Q = 0, V_X is charging up from V_B towards $V_{in,cm}$ with the same τ. The choice of $V_B = 0.25V_{DD}$ makes the SCR waveforms symmetrical around $V_{in,cm}$ for Q = 1 and 0 (and for the positive and negative SCR branches). There is no common-mode transient disturbance, which is another key advantage of the proposed bias settings.

3.3.2 Thermal Noise

The thermal noise associate with the switches and resistors can become the performance limiting factor of the whole modulator, if not handled properly. Due to the large loop gain, the thermal noises from the first stage dominate. Fig 3.7 shows a noise model for the first stage of the modulator in single-ended form. The opamp noise is not included in this analysis as it is of less importance here. The noise of R_1 and R_{dc} is represented by the voltage source $v_{n,1}$ and $v_{n,dc}$, the spectral density of which is

$$\overline{v_m^2} / \Delta f = 4kTR_1 \tag{3.2}$$

$$\overline{v_{n,dc}^2} / \Delta f = 4kTR_{dc1} \tag{3.3}$$

The total noise of the switches and the resistor in the SCR branch is represented by $v_{n,DAC}$. Note that the R_{DAC1p} (see Fig 3.6) is in series with the switch ON-resistance in both phases and its

noise can be absorbed in the noise model of the switches. The total noise power in the switched-capacitor branch in Fig 3.7, evenly distributed from DC to $f_s/2$ due to aliasing, is:

$$\overline{v_{n,DAC}^2} = \frac{2kT}{C_{DAC}} \tag{3.4}$$

The factor 2 in Eq. (3.4) accounts for the two clock phases. The transfer function from $v_{n,DAC}$ to v_o in Fig 3.7 is switched-capacitor integration:

$$\left|\frac{v_o}{v_{n,DAC}}\right| \cong \frac{C_{DAC}}{C_1}\frac{f_s}{2\pi f} \quad \text{for } f << f_s \tag{3.5}$$

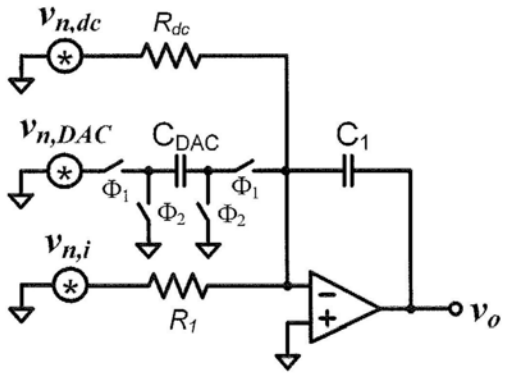


Fig 3.7 Noise model for the first integrator.

Based on the model in Fig 3.7, the total input-referred noise power within the signal bandwidth BW is found to be:

$$\begin{aligned}\overline{v_{neq}^2} &= BW \cdot \left[\frac{\overline{v_{ni}^2}}{\Delta f} + \frac{\overline{v_{n,dc}^2}}{\Delta f}\left(\frac{R_1}{R_{dc}}\right)^2 + \left(R_1 C_{DAC} f_s\right)^2 \times \frac{\overline{v_{n.DAC}^2}}{f_s/2}\right] \\ &= BW \cdot 4kTR_1 \cdot \left(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC}\right)\end{aligned} \tag{3.6}$$

The same result is obtained if the model of [60] is used. For the differential version of the circuit, the noise power is $2 \cdot \overline{v_{neq}^2}$, but note that the signal power goes up by a factor of four. Based on Eq. (3.6), a smaller value for R_1 is preferred. However, to preserve the modulator coefficients,

reducing R_1 leads to an increase in C_1 and thus the amplifier loading. In the modulator, we set C_1 to 31.25pF (see Fig 3.6), a large but still acceptable value. With the R and C values given in Fig 3.6, and for $1V_{pp}$ maximum differential signal amplitude, the thermal-noise-limited SNR of the modulator is 84dB.

The power consumption is dominated by the first integrator in ΔΣ modulator. Consider a practical integrator with a single pole operational amplifier whose frequency response $A(j\omega)$ is:

$$A(j\omega) = \frac{A_0}{1 + j\omega / \omega_p} \tag{3.7}$$

The total input-referred noise power spectral density in Fig 3.7 is:

$$S_{n\,tm}(\omega) = 4kTR_1(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC}) \tag{3.8}$$

The noise power spectral density $S_{n\,tm}(\omega)$ is filtered by the CT integrator whose frequency is:

$$H(j\omega) = -\frac{1}{\frac{1}{A_0} + (1 + \frac{1}{A_0} + \frac{\omega_0}{\omega_{top}})\frac{j\omega}{\omega_0} + \frac{(j\omega)^2}{\omega_0 \omega_{top}}} \tag{3.9}$$

where $\omega_0 = 1/(R_1C_1)$, $\omega_{top} = A_0\omega_p$ (ω_{top} is opamp UGB).

There are two poles in $H(j\omega)$:

$$\omega_{p1} \approx \omega_0 / A_0, \quad \omega_{p2} \approx \omega_{top} \tag{3.10}$$

here $\omega_0 << \omega_{top}$

The Bode diagram of the real integrator frequency response $H(j\omega)$ with the total input–referred power spectral density is shown in Fig 3.8. The noise power spectral is low-pass filtered within the cutoff frequency ω_0, which is smaller than f_s (where $1/(R_1C_1) = k_{sig} \times f_s$, k_{sig} is input coefficient), so that high frequency noise aliased down into the baseband is negligible. The output noise spectral density can be written as:

$$S_{n,o}(\omega) = S_{n,tin}(\omega) \mid H(j\omega) \mid^2 \ , \ 0 \le \omega \le 2\pi f_s \tag{3.11}$$

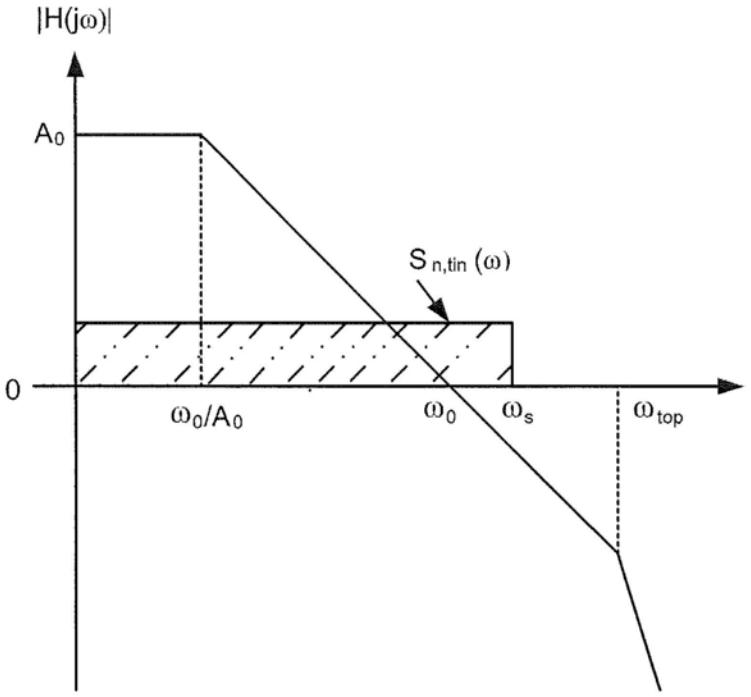


Fig 3.8 Bode diagram of practical integrator frequency response.

The differential output integrated noise power within ω_0 is:

$$P_{n,o}(\omega) = 2 \times 4kTR_1(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC}) \int_0^{\omega_0} \mid H(j\omega) \mid^2 \, d\omega$$

$$= 8kTR_1(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC})(\frac{A_0}{4R_1 C_1})$$

$$= A_0 \frac{2kT}{C_1}(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC}) \tag{3.12}$$

The signal-to-noise ratio can be calculated by the following equation:

$$SNR = \frac{V^2{}_{sig} / 2}{P_{n,o}(\omega)} \tag{3.13}$$

where V_{sig} is differential output swing. The bias current of opamp that ensure it to settle with a purely linear response is:

$$I_{bias} \geq f_{sig} \times 2\pi \times C_1 \times 0.5 \times V_{sig} \tag{3.14}$$

The minimum power consumption of this single pole operational amplifier:

$$P = I_{bias} \times Vdd = f_{sig} \times 2\pi \times C_1 \times 0.5 \times V_{sig} \times \frac{V_{sig}}{\alpha}$$

$$= f_{sig} \times \pi \times C_1 \times \frac{2 \times SNR \times P_{n,o}(\omega)}{\alpha}$$

$$= 2\pi \times f_{sig} \times SNR \times C_1 \times \frac{kT}{C_1} \times n_f \times \frac{1}{\alpha}$$

$$= 2\pi \times n_f \times \frac{1}{\alpha} \times kT \times f_{sig} \times SNR \tag{3.15}$$

where α is defined as $\alpha = \frac{V_{sig}}{V_{DD}}$, n_f is defined as excess noise factor:

$$n_f = 2A_0(1 + \frac{R_1}{R_{dc}} + R_1 f_s C_{DAC}) \tag{3.16}$$

In the proposed modulator, V_{DD}=0.5V and α=0.5. The other parameters are: A_0=65dB, C_1=31.25pF, R_1=R_{dc}=187.5$k\Omega$, C_{DAC}=1.05pF, f_{sig}=25kHz, f_s=6.4MHz. From Eq. (3.15), the calculated minimum power consumption is 504.4μW and 5044 μW when thermal-noise-limited SNR of the modulator is 80dB and 90dB separately.

3.3.3 Clock Jitter-Induced Noise

According to [42], the in-band noise (IBN) due to pulse width jitter of the SCR feedback is:

$$IBN = \frac{1}{k_{sig}^{\ 2}}\left(\frac{N_J|_1}{OSR} + \frac{\pi^2 \cdot N_J|_2}{3 \cdot OSR^3} + \frac{\pi^4 \cdot N_J|_3}{5 \cdot OSR^5}\right) \tag{3.17}$$

$$N_J|_t = \left(k_t \cdot \frac{1}{2} \cdot e^{-0.5\frac{T_s}{\tau}}\right)^2 \left(\frac{\sigma_t}{T_s}\right)^2 \tag{3.18}$$

where k_t and k_{sig} are the feedback branch and input scaling coefficients, τ is the SCR time constant, and σ_t is the standard deviation of the timing uncertainty. In this design, $k_1 = 0.667$, $k_2 = 1.25$, $k_3 = 2.3$, $k_{sig} = 0.0267$, $OSR = 128$ and $\tau = 0.05T_s$. For $\sigma_t = 0.01T_s$, the jitter-limited SNR of the modulator is $117dB$, beyond the limit set by the quantization noise (see Fig 3.4).

3.4 Circuit Design and Simulation Results

In this section, the building blocks of the modulator are presented. The amplifier is the most critical block, and is described first.

3.4.1 Amplifier

3.4.1.1 Speed Requirement of Amplifier

As mentioned earlier, the SCR feedback pulse changes more rapidly than a regular rectangular feedback pulse. The first stage amplifier needs to have a unity-gain-bandwidth (UGB) of $3\times f_s$ (19.2MHz here) or more [42]. The slew-rate (SR) requirement for the first stage amplifier is [42]:

$$SR_{max} \geq fs \cdot (k_{sig} \cdot V_{sig} + k_1 V_{ref}) = 2.22V / us \tag{3.19}$$

where V_{sig} is the maximum modulator input amplitude (0.5V), V_{ref} the reference voltage (0.5V), k_{sig} = 0.0267 and k_1 =0.667. Increasing the UGB lowers the effective time constant of the SCR pulse, and thus reduces jitter-induced noise according to Eq. (3.18). The SR and UGB requirements of second and third stage amplifiers are less demanding than for the first stage as

these stages are enclosed by the outer loop and their non-idealities are first-order or second-order high-pass shaped.

3.4.1.2 Amplifier Topology

To meet the requirement under a 0.5-V supply, a two-stage amplifier topology with a self-biased CMFB loop [57] is adopted. Fig 3.9 shows the circuit details. Table 3.1 gives the components

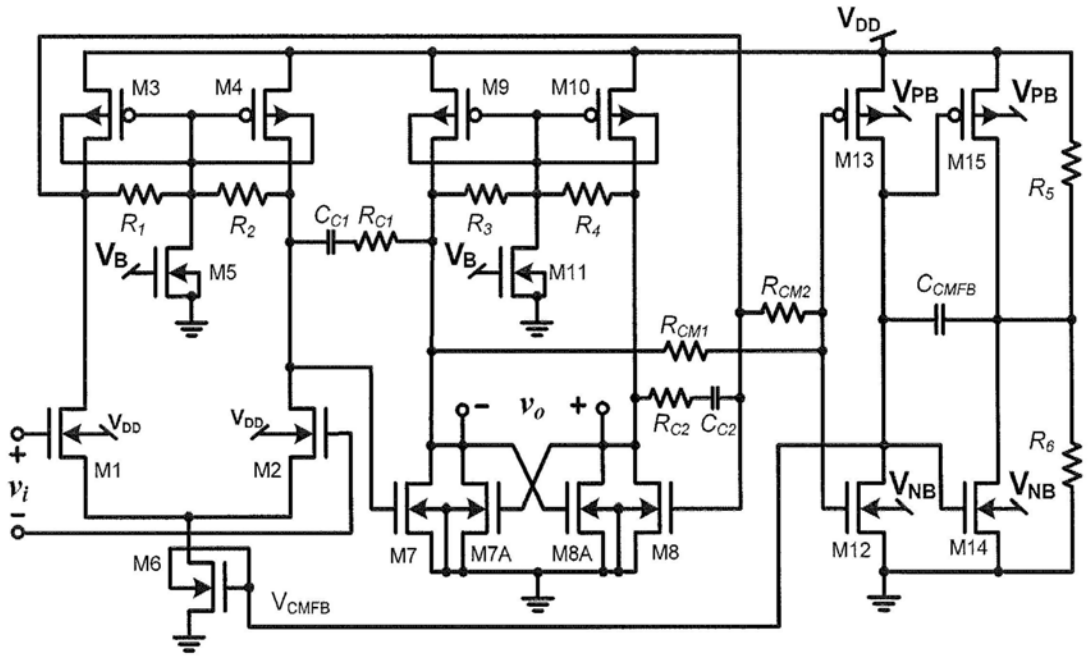


Fig 3.9 ULV two-stage amplifier with self-biased CMFB.

Table 3.1 Components values of first amplifier

R_1,R_2,R_{CM1},R_{CM2}=100K	M_6=285/1
R_3,R_4=70K	M_7,M_8=97/1
R_5,R_6=15.3K	M_{7A},M_{7B}=6/1
R_{C1},R_{C2}=1.3K	M_9,M_{10}=250/1
C_{C1},C_{C2}=9.1pF	M_{11}=5.5/2
C_{CMFB}=5.1pF	M_{12}=4/0.36
M_1,M_2=210/1	M_{13}=16.4/0.36
M_3,M_4=120/1	M_{14}=16/0.36
M_5=11/2	M_{15}=65.6/0.36

values. The amplifier consists of two stages and a DC CMFB stage. The input CM voltage is set at $0.75V_{DD}$ by external circuits (Fig 3.6) and the input pair (M_1 & M_2) of the first stage have forward-biased body-source junction to lower their thresholds. The risk for latch-up is rare when the circuit is operating under 0.5-V supply [61]. With these measures, there is voltage room to bias M_1 and M_2 towards moderate or strong inversion for the speed required without increasing their W/L ratio to impractical values. M_3, M_4, M_5, R_1 and R_2 form a local CMFB loop that assists in the CM signal rejection. The second stage of amplifier uses a gate-input differential pair without a tail current. A negative g_m pair, M_{7A} and M_{8A}, is used to reduce the differential output conductance and to enhance the voltage gain.

The amplifier forces its output CM voltage to $V_{DD}/2$ with a DC CMFB loop containing of the error amplifier formed by M_{12} and M_{13}. The error amplifier operates at $V_{in}=V_{out}=V_{DD}/2$ through proper biasing of the body terminals and acts like a differential amplifier with one input tied to $V_{DD}/2$ [62]. It compares the output CM DC voltage with $V_{DD}/2$, amplifies the difference, and applies a correction signal V_{CMFB} to the gate of M_6. A frequency-compensation capacitor larger than $200pF$ would be needed to stabilize the CMFB loop. To save the chip area, a second error amplifier (M_{14} and M_{15}) is used to multiply the equivalent capacitance of C_{CMFB} at the drain of M_{12} [57]. R_5 and R_6 are used to bias the second error amplifier in its high gain region.

The biasing voltages V_{PB}, V_{NB} and V_B are generated on chip. Fig 3.10 shows the bias circuit for V_{PB} and V_{NB} to maintain the internal reference of the error amplifiers at $V_{DD}/2$ under process/voltage/temperature (PVT) variations [62]. The bias circuit in Fig 3.11 generates V_B; the voltage at node A is set to $V_{DD}/2$ and the current in M_1 controlled by V_B is designed to be $(V_{DD}/2)/125k\Omega$. M_1 in Fig 3.11 is matched to M_5 and M_{11} in the main amplifier in Fig 3.9.

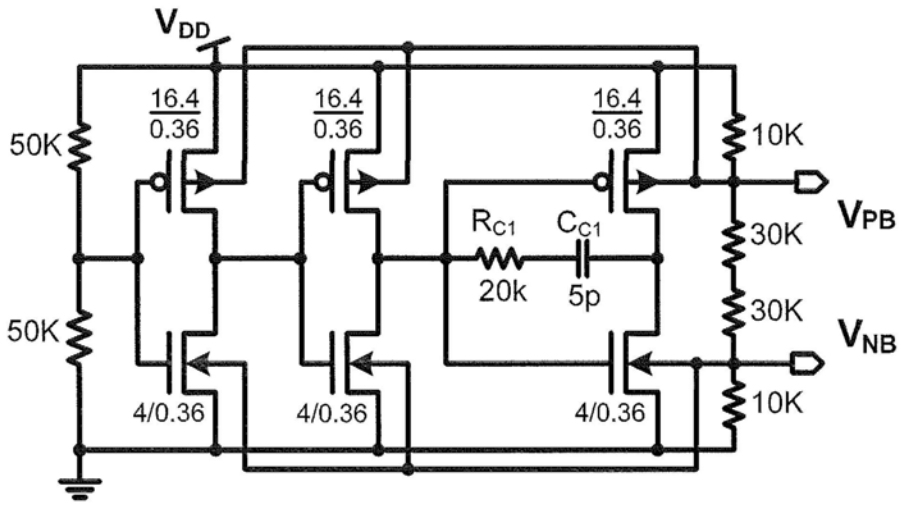


Fig 3.10 Biasing generation circuit for V_{PB} and V_{NB}.

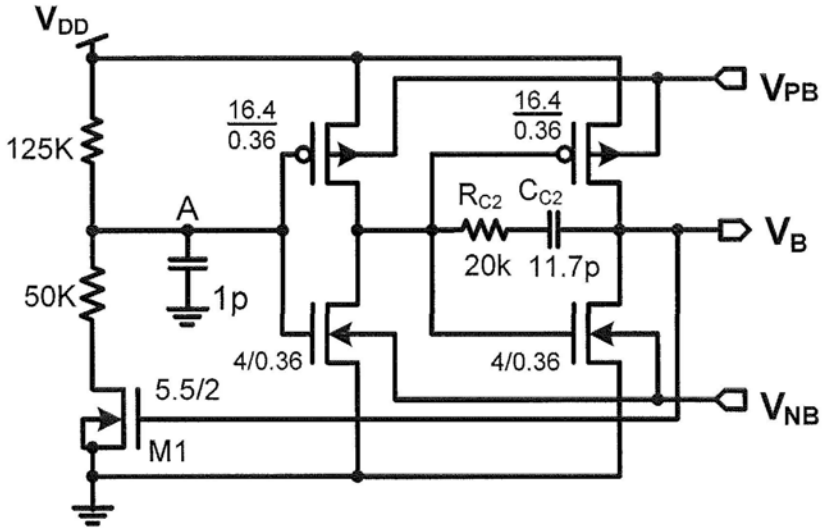


Fig 3.11 Biasing generation circuits for V_B.

3.4.1.3 Simulation Results

The amplifiers for the three ΔΣ modulator stages are scaled as 1:0.3:0.2. Fig 3.12 shows the simulated frequency responses of the first amplifier over PVT corners (-27 ℃ to 85 ℃, 0.45V to 0.55V, and slow, nominal and fast process corners). Simulations also showed that the amplifiers meet requirements over PVT corners. The simulated performance of the amplifiers is

shown in Table 3.2 . Note that the designs are conservative for high ΔΣ modulator performance and the power consumption is not optimized.

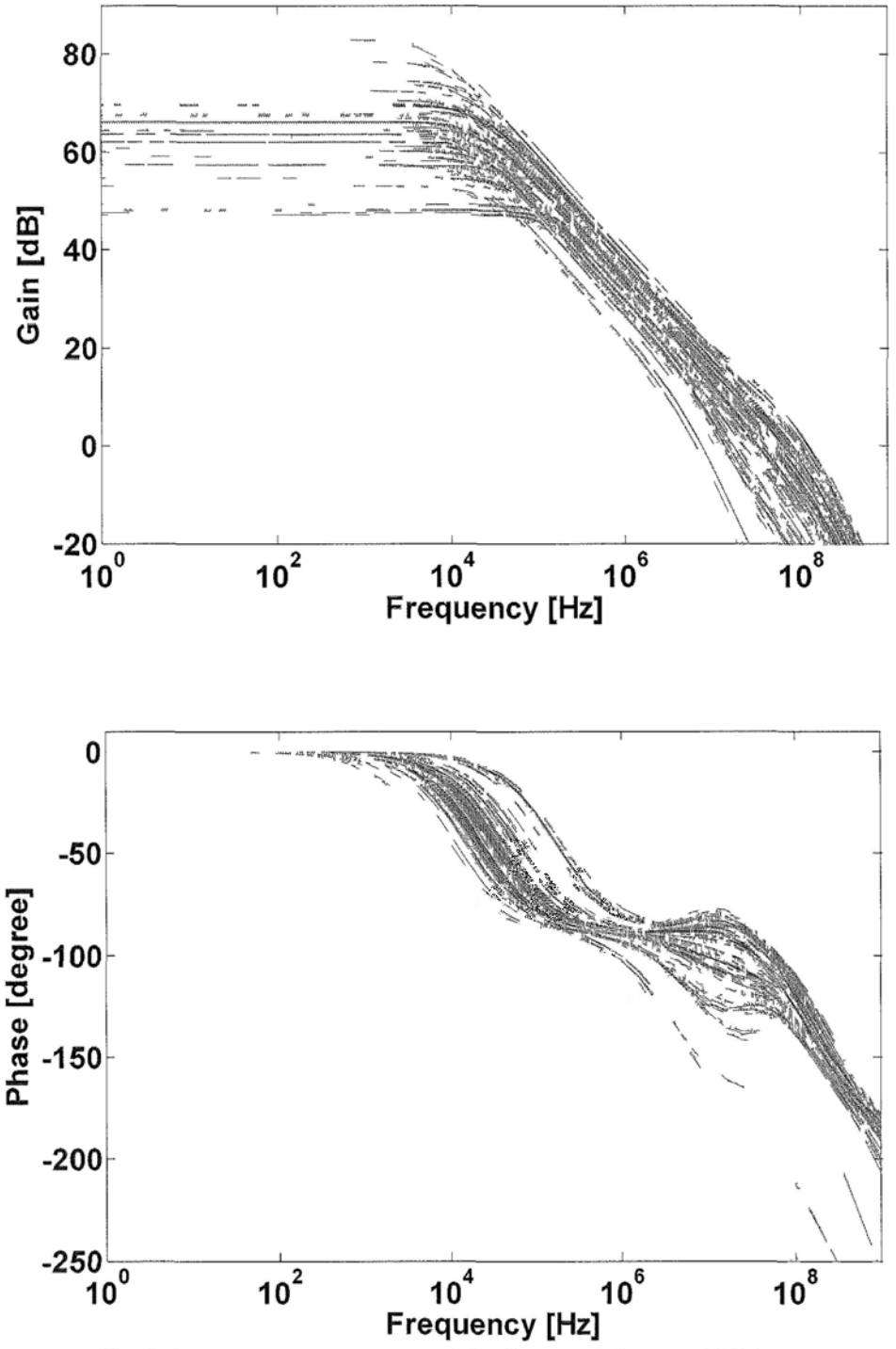


Fig 3 12 Frequency responses of the first amplifier over PVT corners

Table 3.2 Simulation performance of the amplifiers.

Parameters	AMP-1	AMP-2	AMP-3
Supply(V)	0.5	0.5	0.5
Power Consumption(μW)	442	122	78
Open loop DC Gain (dB)	65	66	59
UGB/PM (MHz / degree)	51 / 70	42 / 69	43 /60
Input ref.noise @1KHz/1MHz (nV/sqHz)	18.7 / 3	46 / 7	66 /10
CMRR@DC (dB)	132	132	124
SR+/SR- (V/μs)	7.9 / 11.7	5.5 / 7.8	8.8 / 11.9
Load(pF// kΩ)	31.25 // 60	7.8 // 60	3.9

3.4.2 Comparator

Fig 3.13 shows the proposed ULV comparator, consisting of a body-input pre-amp and a gate-clocked latch. The body-input approach is adopted since the third integrator of the modulator has an output CM level of merely 0.25V ($V_{DD}/2$), preventing the use of gate-input approach for the technology used. The latch stacks only one NMOS and one PMOS between the supply rails with the gates of PMOS used for the clocking.

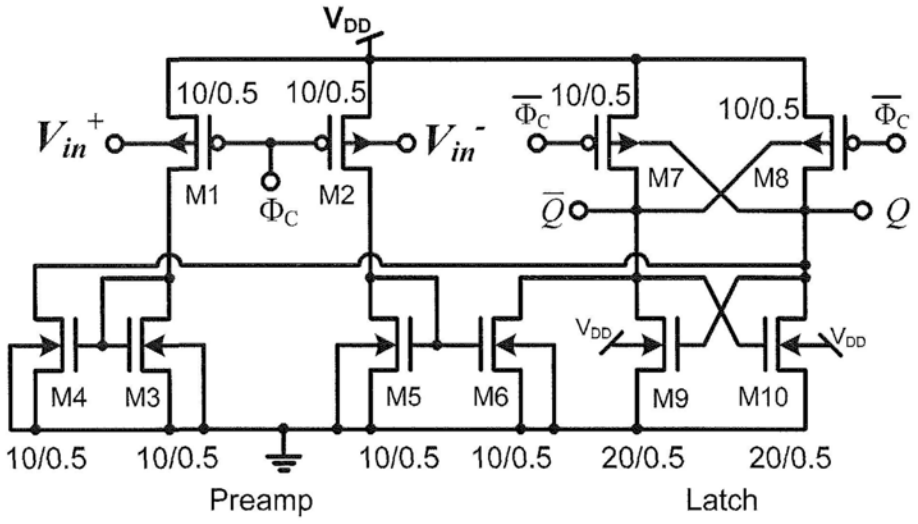


Fig 3.13 ULV body-input gate-clocked comparator.

When Φ_C is "low", the pre-amp amplifies the differential input, and the latch is turned off

and $Q = \overline{Q} = 0$. When Φ_C is "high", the latch regenerates the initial voltage difference between the gates of M_4 and M_6 to a valid logic level. This comparator has a faster settling time and is smaller compared with the body-input gate-clocked comparator in [14].

3.4.3 SCR feedback DAC

3.4.3.1 Schematic of SCR

The SCR feedback DAC is composed of an inverting buffer, a capacitor, a resistor and switches as shown in Fig 3.6. The transistor level schematic is shown in Fig 3.14. In order to keep time constant of the SCR pulse the same as the design value, the ON resistances of the switches controlled by Φ_1 should be taken into account in calculation of the resistor value. The switches in series with RC are implemented as CMOS switches to reduce their ON resistance. The switches controlled by Φ_2 are NMOS switches. A separate and clean V_{DD} is used for inverting buffer to minimize direct noise injection from the supply.

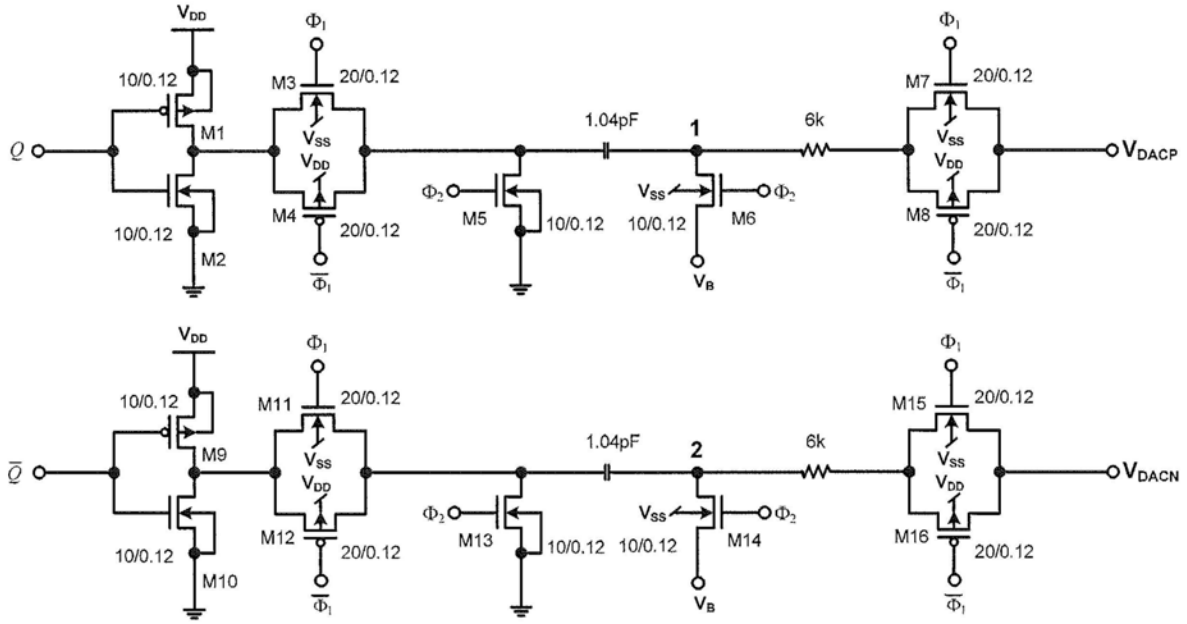


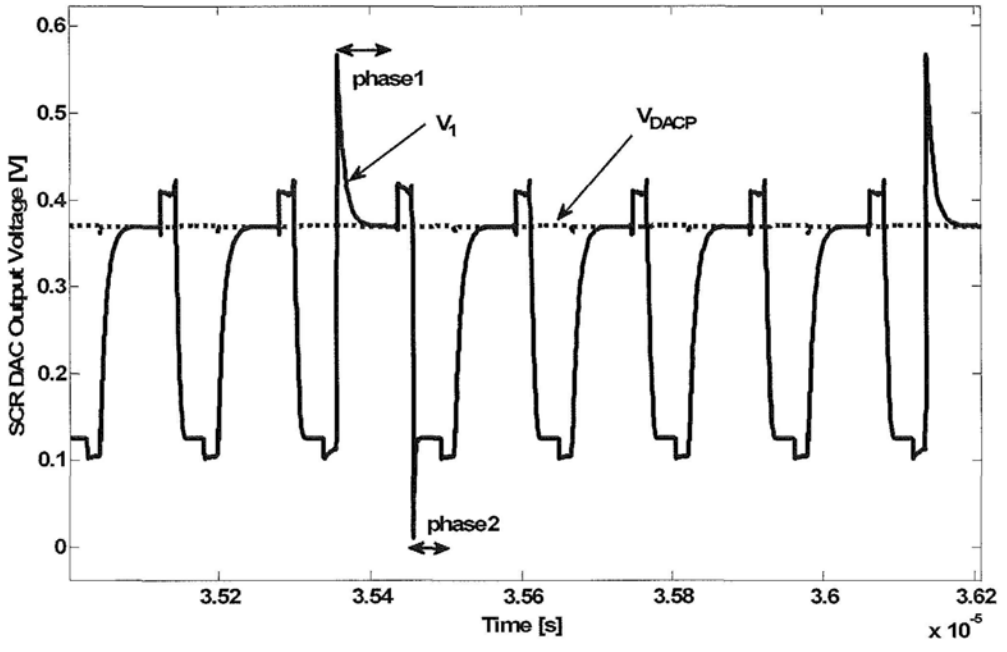
Fig 3.14 The SCR DAC circuit.

During inactive phase of SCR feedback branch, Φ_2 is "high", M_5 and M_6 are ON, M_3-M_4 and M_7-M_8 are OFF. The voltage at node 1 is charged to the initial value V_B. When Φ_C is "high", the comparator latches. After 20% T_s from the rise-edge of Φ_C, Φ_1 becomes "high" and this is the active phase of SCR feedback branch. During this phase, M_3 -M_4 and M_7-M_8 are ON, M_5 and M_6 are OFF. The voltage at node 1 either decays from $1.25V_{DD}$ towards $V_{in,cm}$ or charges up from V_B towards $V_{in,cm}$ depending on the value of Q.

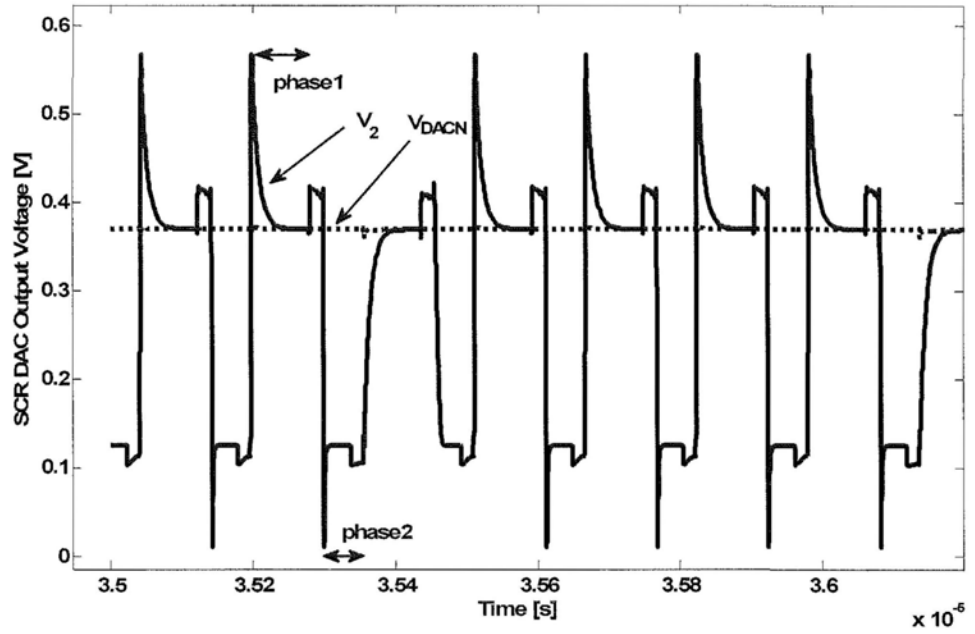
The Φ_C turns OFF later than Φ_1. When Φ_C is "low", the comparator output Q becomes invalid, and M_3-M_4 turn OFF already. The invalid Q is guaranteed not to appear at V_{DACP}.

3.4.3.2 Simulation Results of SCR DAC

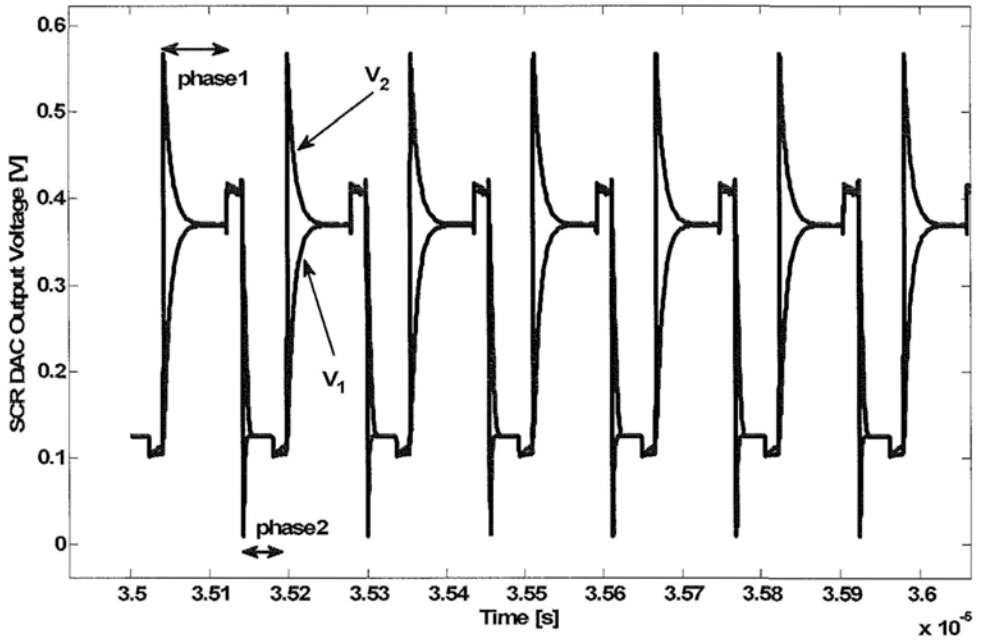
The simulated waveforms of V_1 and V_{DACP}, V_2 and V_{DACN} are shown in Fig 3.15 (a), Fig 3.15 (b) separately. As discussed earlier, V_1 and V_2 are exponentially charged or discharged to $V_{in,cm}$



(a)



(b)



(c)

Fig 3.15 (a) Simulated waveform of V_1 and V_{DACP}; (b) Simulated waveform of V_2 and V_{DACN}; (c) Simulated waveform of V_1 and V_2.

during Φ_1, and charged to initial value V_B during Φ_2. The peak value of V_1 or V_2 is less than $1.25V_{DD}$ due to the charge injection of M_3 and M_4 and the turn on resistance of M_3 and M_4. V_1 or V_2 jumps from $V_{in,cm}$ or V_B to a certain value when Φ_1 or Φ_2 changes from "high" to "low" due to charge injection. The SCR feedback DAC is a differential pair, so the charge injection can be cancelled as shown in Fig 3.15 (c).

3.4.4 Clock Generator

The clock generator circuit is shown in Fig 3.16. Input signal is an external sine-wave as its clock jitter is smaller than square-wave. The $20\%T_s$ delay from Φ_1 to Φ_C is sensitive to PVT variation as it is generated by an inverter chain. Circuit simulation shows that the delay from Φ_1 to Φ_C is up to $\pm 6\%T_s$ within the tolerance of $\pm 10\%T_s$ as shown in Matlab simulation results Fig 3.4.

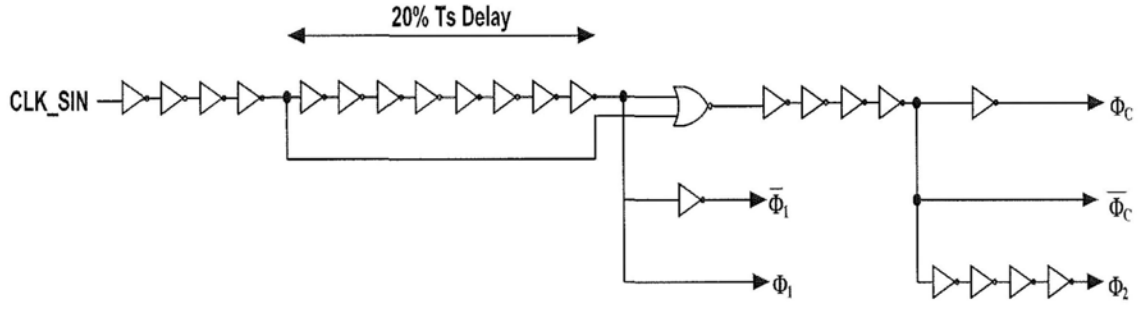


Fig 3.16 Clock generator.

3.4.5 Simulation Results of the Whole Modulator

3.4.5.1 Layout Consideration

Layout is important when designing an ULV high performance ΔΣ modulator. Special attention should be paid on the matching of the devices. As the supply voltage is 0.5V, mismatch between devices will affect the operating point of amplifier. Post-layout simulation results show that the mismatch between differential branches can degrade the DC gain and UGB of amplifier.

The common-centroid layout technique is used in minimizing the mismatch due to the process imperfection. Fig 3.17 shows the layout of a pair of transistors using common-centroid layout technique. The centroid of transistor A and B are coincident. And almost symmetrical wire-routing is used to minimize the voltage difference between differential branches.

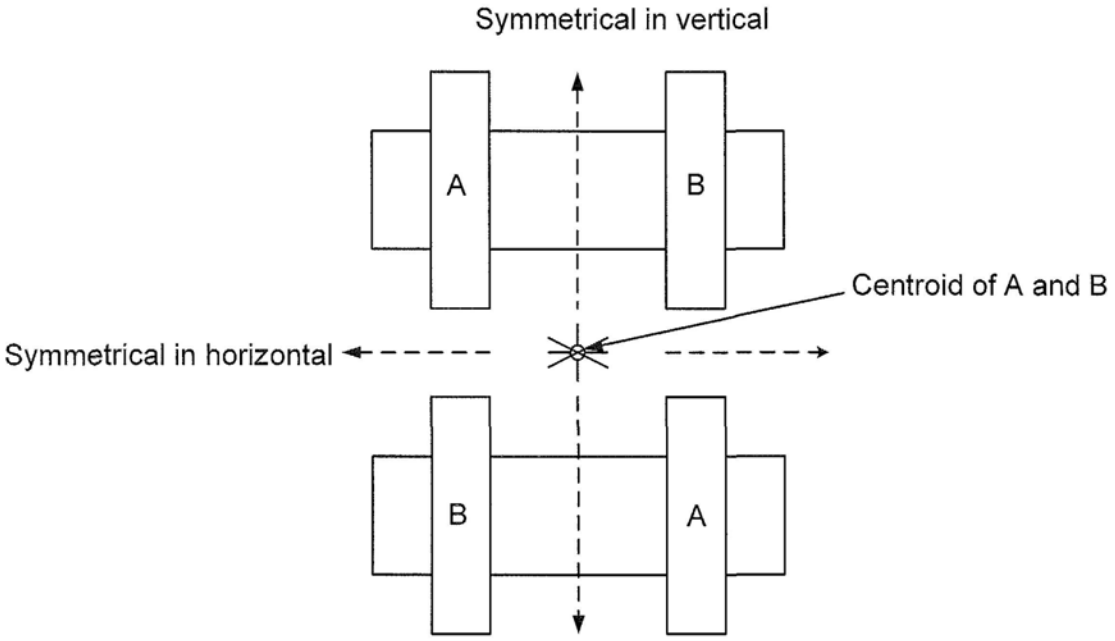


Fig 3.17 Common-centroid layout technique for a pair of transistors.

The width of analog power supply rails is 10um with two metal layers as the total current pass through it is 1.3mA, the length of the analog power suppliers is 360um, the sheet resistance of MET2 layer is 70mΩ/□, the total IR drop across the wire is 1.3mA×(360um/10um)×70mΩ, approximately 3.28mV. The IR drop effect is negligible in this prototype.

3.4.5.2 Post-Layout Simulation Result

Fig 3.18 shows the post-layout simulation result by Cadence Spectre with a 4.3-*k*Hz near full-scale sinusoidal input (V_{in}=-0.72*dB* V_{FS}, where V_{FS}=1$V_{pp,diff}$). The simulated SNR is 101*dB* over 25-*k*Hz bandwidth, and the SNDR is 1*dB* less than SNR due to the third order harmonic distortion.

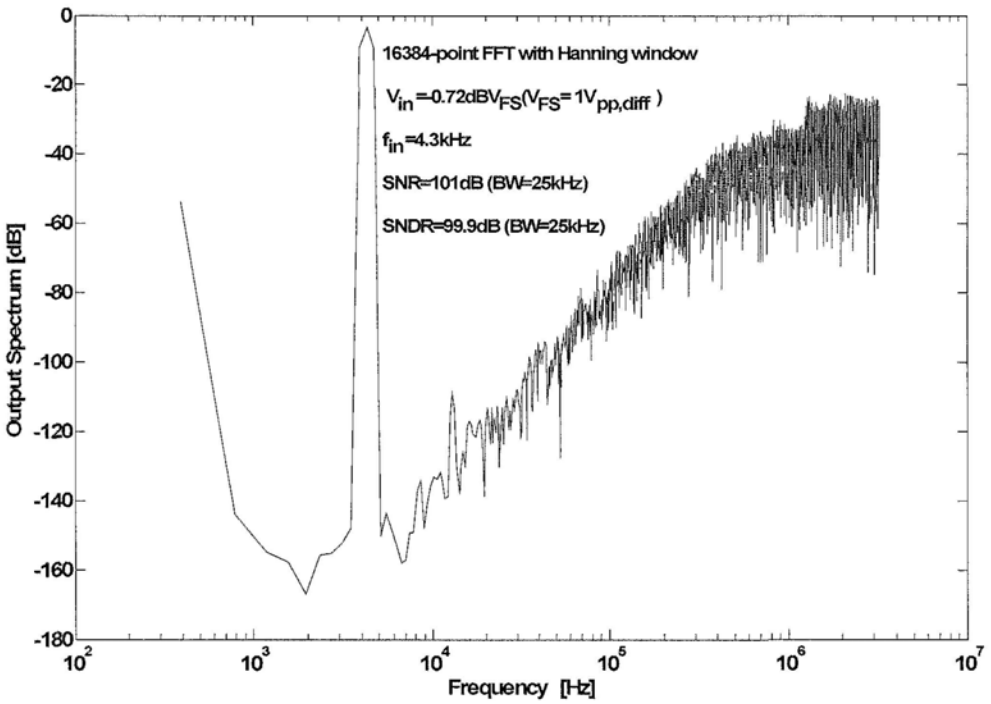


Fig 3.18 Post-layout simulation result with V_{DD}=0.5V, T=25°C.

3.5 Experimental Results

3.5.1 Chip Photograph

The modulator was fabricated in a 0.13μm CMOS triple-well process with standard V_T devices. For triple-well process, NMOS transistors can be fabricated in P-well, so that the body terminals of triple-well NMOS transistors can be used for biasing or signals. Metal-insulator-metal (MIM) capacitors and high-resistivity poly resistors were used. The high-resistivity poly resistor is chosen to save chip area as its resistivity is larger than silicon resistor. The die photo is shown in Fig 3.19. The circuit occupies an active area of is 0.8mm^2 and eight metal layers are used. Nine packaged chips have been tested and they perform consistently with results reported below.

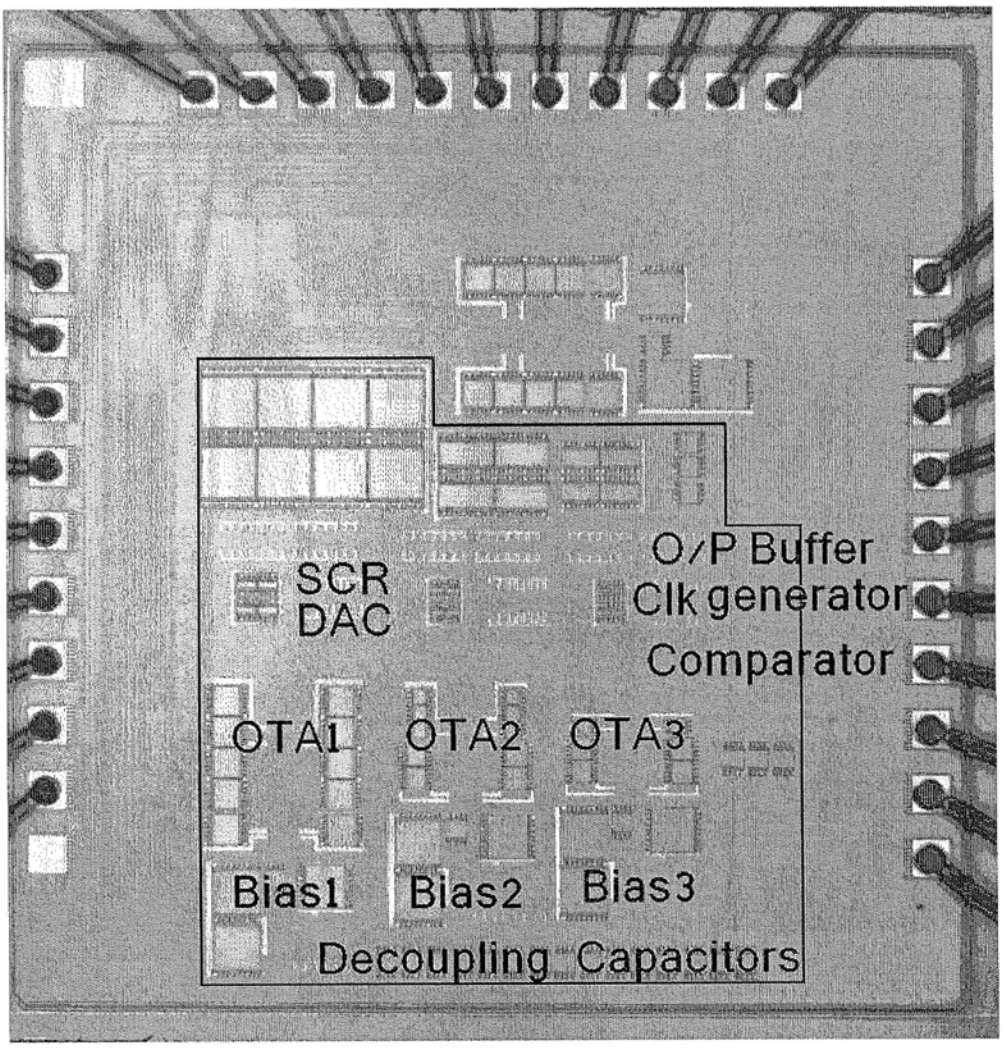


Fig 3.19 Die photograph of 0.5V CT SCR ΔΣ modulator.

3.5.2 PCB Design

Fig 3.20 shows the schematic of measurement setup. Decoupling capacitors are used in all the power suppliers and DC biasing sources. Analog power supplies, digital power supplies and output buffer supplies are separated.

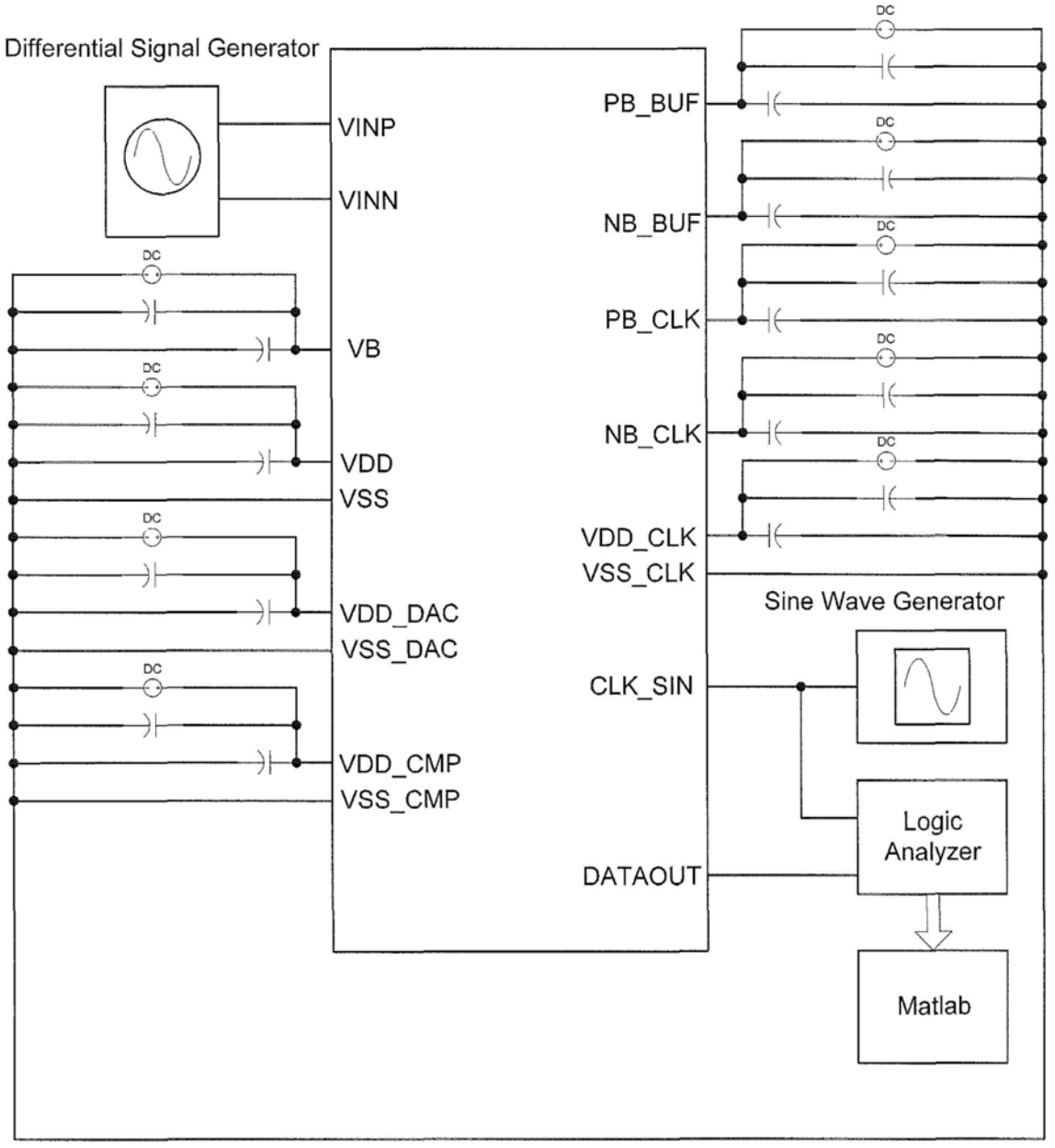


Fig 3.20 Schematic of measurement setup.

Fig 3.21 shows the complete Printed Circuit Board (PCB) for the ΔΣ modulator measurement. A 22*n*F decoupling capacitor is placed near the power supplier pins and DC biasing source pins. A 2200*u*F by-pass capacitor is placed between the power suppliers and

ground The output data is recorded by a logic analyzer and processed by Matlab™ and FFT is applied to convert the digital output to frequency spectrum

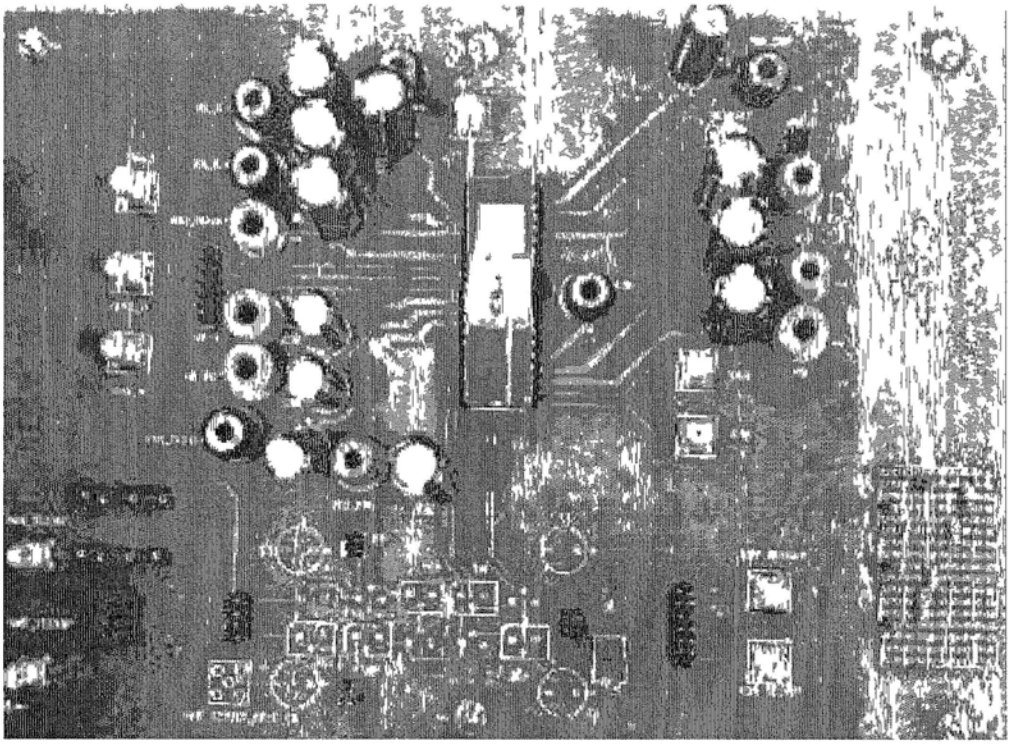


Fig 3 21 Photograph of PCB board

3.5.3 Measurement Results

Fig 3.22 shows a measured output spectrum with a 1*k*Hz near -full-scale sinusoidal input (V_{in} = –0 72*dB* V_{FS}, where V_{FS} = $1V_{pp\ diff}$) at room temperature. There are virtually no harmonic tones and the spurious-free dynamic range (SFDR) is 93.9*dB*.

Fig 3 23 shows the measured SNDR and SNR across the input range The modulator records a peak SNDR, a peak SNR and a dynamic range (DR) of 81 2*dB*, 81 3*dB* and 82*dB* respectively for 25-*k*Hz signal bandwidth At 0 5V, the modulator consumes 625μW

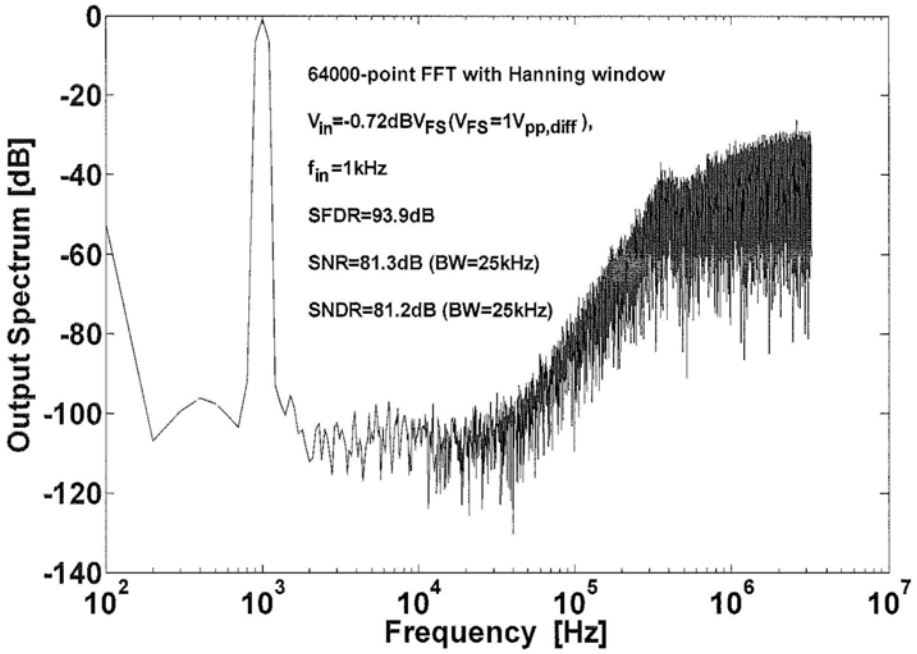


Fig 3.22 Measured output spectrum with V_{DD}=0.5V, T=25°C.

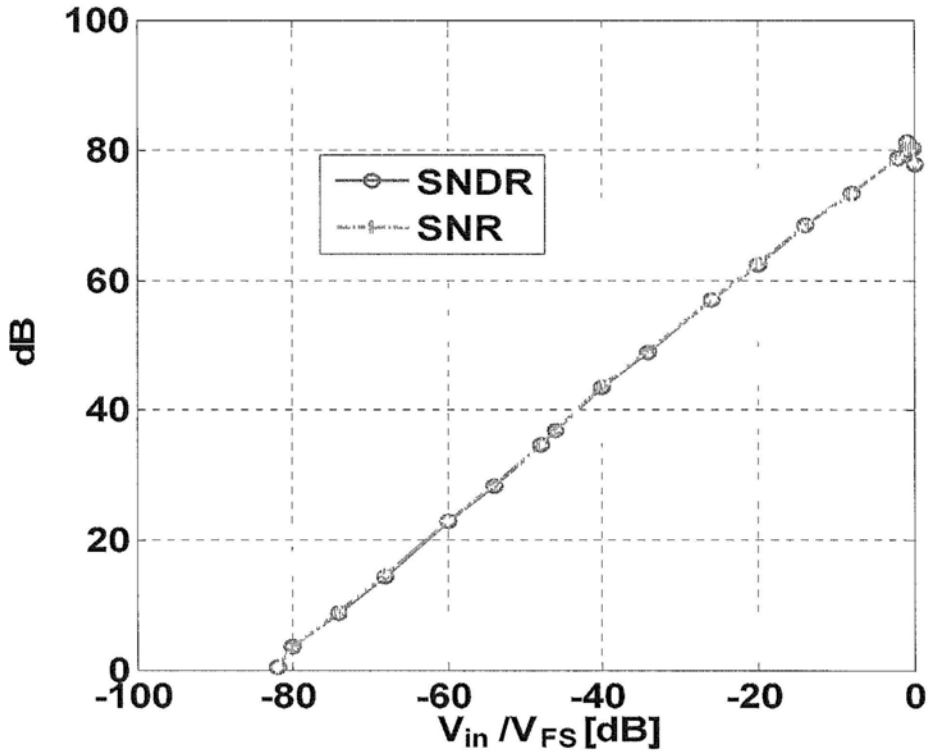


Fig 3.23 Measured SNDR and SNR versus V_{in}, V_{DD}=0.5V, T=25°C.

Table 3.3 summarizes the measured performance of the modulator at room temperature. For the nominal V_{DD} of 0.5V, a peak SNDR of 81.2*dB* is achieved in a 25*k*Hz bandwidth for a nearly full range differential input signal of $0.92V_{p\text{-}p,diff}$, and 625μW power consumed by the modulator and 67μW power by the output buffers which are used to drive the measurement equipments. For a 20-*k*Hz bandwidth, the peak SNDR and SNR are 83.4*dB* and 83.6*dB* respectively with A-weighting on the spectrum.

Table 3.3 Measured modulator performance at 25°C

Modulator type	**1-bit, 3rd order, CT**
Signal bandwidth	25kHz
Sampling frequency/OSR	6.4MHz/128
Input signal range	$1V_{ppdiff}$
Supply voltage	0.5V
Peak SNR	81.3dB@BW=25kHz 82.1dB@BW=20kHz 83.6dB@BW=20kHz, A-weighted
Peak SNDR	81.2dB@BW=25kHz 82dB@BW=20kHz 83.4dB@BW=20kHz, A-weighted
Dynamic Range	82dB@BW=25kHz 82.7dB@BW=20kHz 84.2dB@BW=20kHz, A-weighted
SFDR @ Vin=$0.92V_{ppdiff}$	93.9dB
Power consumption (total) Modulator Output buffers	692μW 625μW 67μW
Active die area	$0.8mm^2$
Technology	0.13μm CMOS, standard V_T MIM capacitors, and HiRes Poly

The input clock has a jitter of $265ps_{RMS}$, i.e., smaller than 1% T_s. Based on Eq. (3.17), the jitter-limited SNR is greater than 117*dB* and the jitter-induce noise is not limiting the performance. The measured peak SNR of 81.3*dB* is close to the 84*dB* thermal noise limit. The amplifier is likely the noise source contributing to the 2.7*dB* difference between the measured and calculated values. One way to improve the performance is to find a modulator architecture that has a larger coefficient at the input and thus a lower input resistance (see Fig 3.1).

Fig 3.24 shows the measured SNR and SNDR for a V_{DD} between 0.45V and 0.8V at the room temperature with a fixed input magnitude of 0.92 $V_{p\text{-}p,diff}$. The SNDR variation is within 2.6*dB* and an SNR variation is within 1.2*dB* when V_{DD} changes between 0.48V and 0.8V. The modulator's performance is very consistent with its nominal performance across a wide supply voltage range. According to the wafer-acceptance-test measurement results from foundry, the chip is fabricated in slow process corner, so the SNR and SNDR drops tremendously when V_{DD} is below 0.48V.

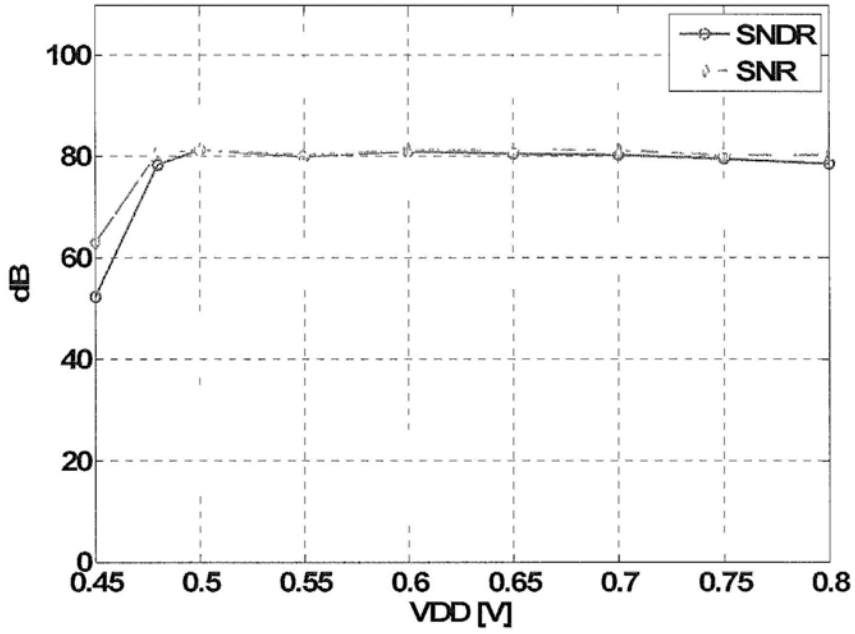


Fig 3.24 Measured SNR and SNDR versus supply voltage from 0.45V to 0.8Vwith *Vin* fixed at 0.92 $V_{p\text{-}p,diff}$, T=25°C.

Fig 3.25 shows the measured SNR and SNDR for temperature changing between -20°C and 90°C at V_{DD} =0.5V for a fixed input level of 0.92 $V_{p\text{-}p,diff}$. The lowest temperature of the temperature chamber can be set at -20°C, so the measurement result cannot go down to -27°C as in simulation. The SNDR variation is less than 6*dB* and SNR variation is less than 2*dB* for this

temperature range. The SNDR remains over 80*dB* until temperature reaches 60°C, and then gradually decreases to 77.5*dB* at 70°C. The modulator's performance is also very consistent with its nominal performance across a wide temperature range.

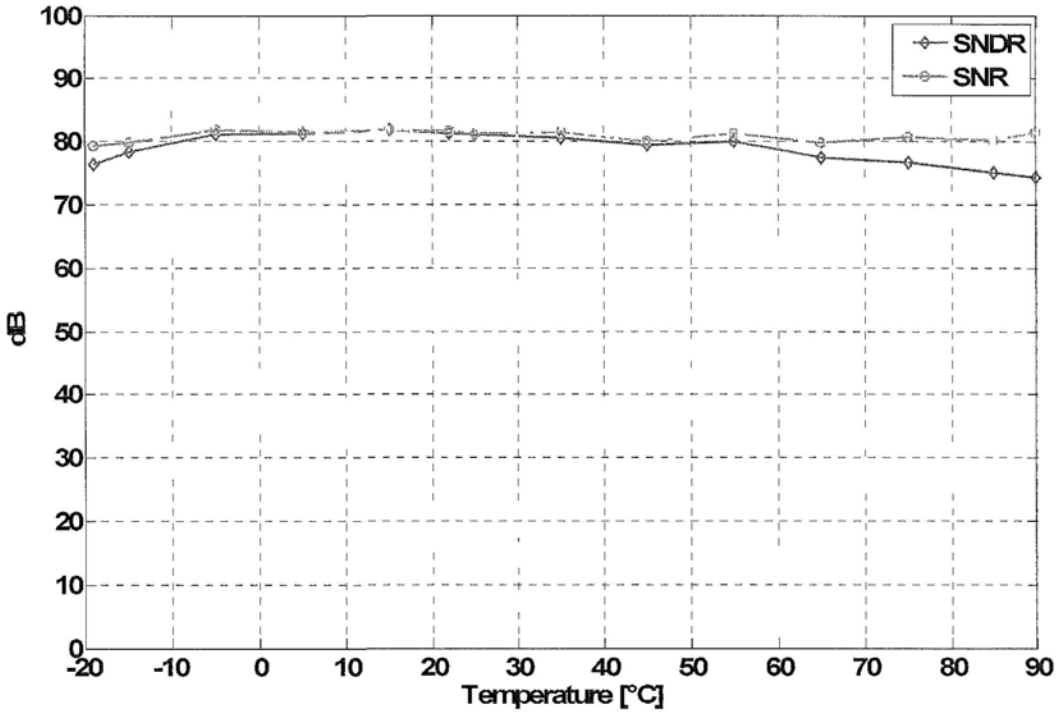


Fig 3.25 Measured SNR and SNDR versus temperature from -20°C to 90°C with *Vin* fixed at 0.92 $V_{p\text{-}p,diff}$, V_{DD}=0.5V.

The figure-of-merit (FoM), is defined as:

$$\text{FoM} = \text{Power}/\left(2^{(\text{SNDR-1.76})/6.02} \times 2 \times \text{Bandwidth}\right) \tag{3.20}$$

The FoM is 1.33*pJ*/conversion for the presented ΔΣ modulator. Comparing FoMs, the presented 0.5V ΔΣ modulator performs better than the 0.5-V and 0.6-V ΔΣ modulators in [14], [20], [22], but worse than the 0.6V ΔΣ modulator in [21]. It is important to note that with circuit architecture of [21] it is very difficult to scale to lower supply voltages. Additionally, [21] uses a process with low NMOS and PMOS thresholds (0.2V and -0.15V), while in the process for this

design the device thresholds are higher (0.28V and -0.26V). Compared to [21], this design uses a 0.1-V lower V_{DD}, which is a substantial relative change at these extremely low V_{DD} levels.

3.6 Summary

A fully-differential CT ΔΣ modulator with SCR feedback enabled by a special CM arrangement for reduced jitter sensitivity is first demonstrated with excellent noise and linearity performance for a 0.5V supply while using standard V_T. A fully differential wideband ULV amplifier and a body-input gate-clocked comparator are also key enablers for this design.

Consuming $625\mu W$ at 0.5V supply, the modulator achieves a SFDR of $93.9dB$ and a peak SNDR of $81.2dB$ over 25-kHz signal bandwidth. The measured performance is consistent across a wide supply voltage range from 0.5V to 0.8V and over the commercial temperature range. The analysis shows that the performance is limited by thermal noise, and ways to improve performance have been discussed.

Chapter 4

A 25-kHz 87.8dB SNDR 102dB SFDR CIFF Continuous-Time Delta-Sigma Modulator at 0.5V

4.1 Introduction

The performance of ΔΣ modulator presented in Chapter 3 is limited by thermal noise. In order to meet the target performance presented in Chapter 1, the thermal noise should further be reduced. The CIFF loop topology is adopted for the CT ΔΣ modulator presented in this chapter, which has large input scaling coefficient. Smaller value of input resistance results in smaller thermal noise based on Eq. (3.6). An adaptive CMFB compensation method is proposed to ensure the robust frequency compensation of amplifier against process variation. This adaptive compensation method also applies to bias circuits and ensures stable bias against process variation. Fabricated in a 0.13μm CMOS process, the modulator achieves a measured peak SNDR of 87.8dB over 25-*k*Hz signal bandwidth and 102dB SFDR, consuming 682.5μW at 0.5-V supply.

4.2 System Architecture and Behavioral Simulation

4.2.1 Architecture

The CIFF architecture is chosen for this CT ΔΣ modulator as it can increase the input scaling coefficient and lead to the decrease of input resistance. The thermal noise can be reduced by this architecture. The SCR feedback DAC is still adopted to reduce the clock jitter effect. The signal bandwidth is 25*k*Hz, sampling frequency is 6.4*M*Hz offering 128x OSR to meet the target performance specification presented in Chapter 1. The quantizer is a one-bit comparator which

has better linearity.

The DT modulator prototype designed with Matlab™ toolbox [63] is:

$$HTF(Z) = \frac{0.79974(z^2 - 1.64z + 0.6947)}{(z-1)^3} \tag{4.1}$$

The noise transfer function NTF(z) is:

$$NTF(Z) = \frac{(z-1)^3}{(z-0.6694)(z^2 - 1.531z + 0.6639)} \tag{4.2}$$

A 3rd order CIFF one-bit architecture is selected for the CT modulator. Fig 4.1 shows the modulator coefficients, which are derived from DT to CT conversion [42] and after dynamic range scaling and input range scaling. The time constant of SCR DAC is equal to 5%T_s (T_s=1/f_s). The 50% pulse width of SCR DAC waveform and 20% delay of the DAC have been taken into account of the modulator design.

The input signal coefficient is 0.12, much larger than the coefficient of 3rd order CIFB CT ΔΣ modulator in Chapter 3, which results in reduction of thermal noise (see section 4.3.2).

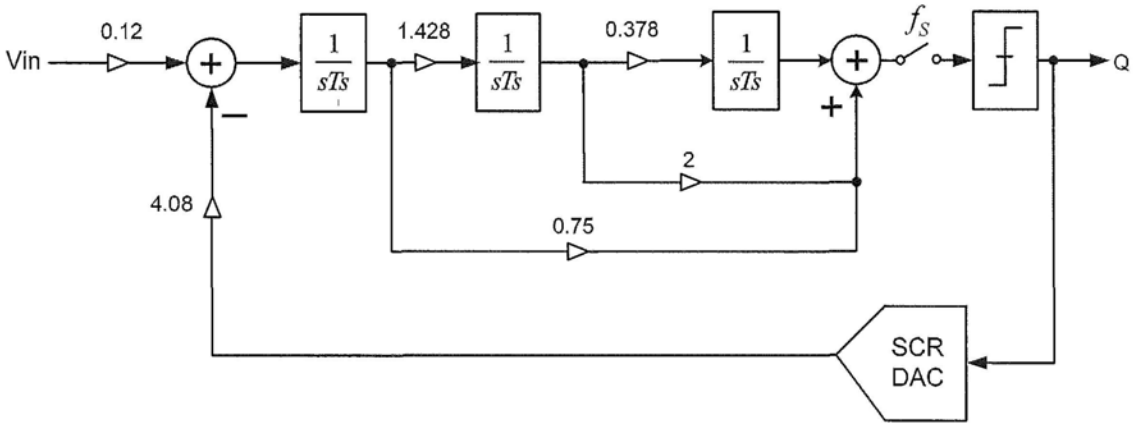


Fig 4.1 CIFF architecture modulator coefficients (f_s = 6.4MHz, T_s=1/f_s).

4.2.2 Behavioral Simulation Results

Fig 4.2 presents the Matlab™ model of the modulator. Fig 4.3 shows The PSD simulated with Matlab™ with V_{in} fixed at $0dB$ V_{FS} (V_{FS}=1$V_{pp,diff}$). The SQNR is $105dB$ under nominal RC product value.

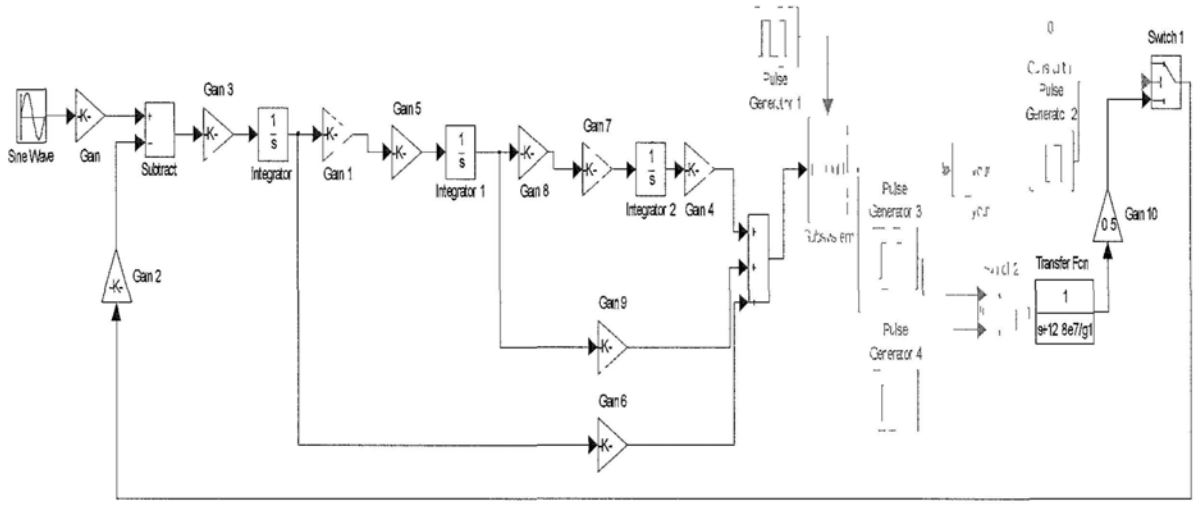


Fig 4.2 Matlab model for 3rd order CIFF architecture CT ΔΣ modulator with SCR feedback.

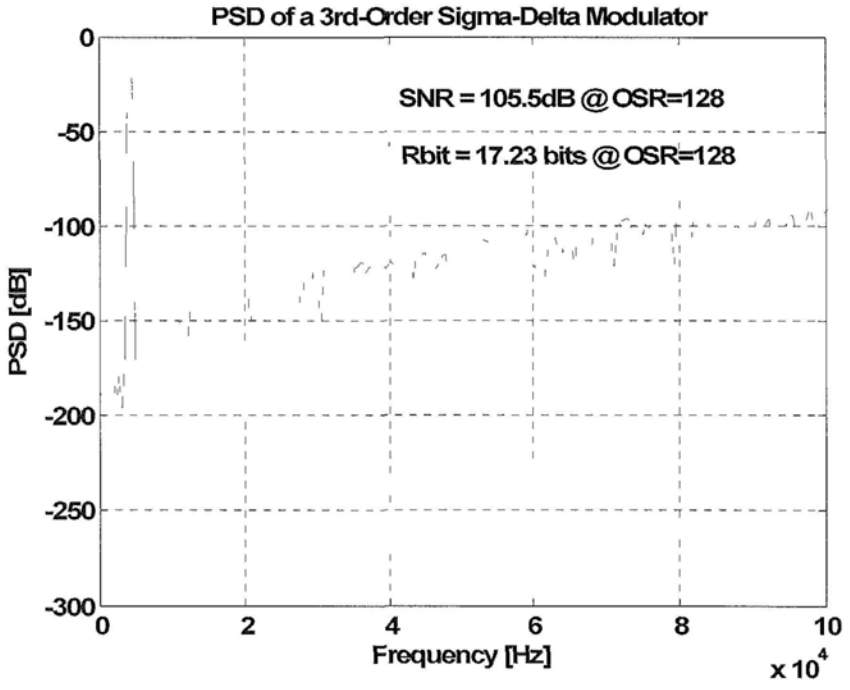


Fig 4.3 Matlab simulation result: Power Spectrum Density with V_{in} at $0dB$ V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

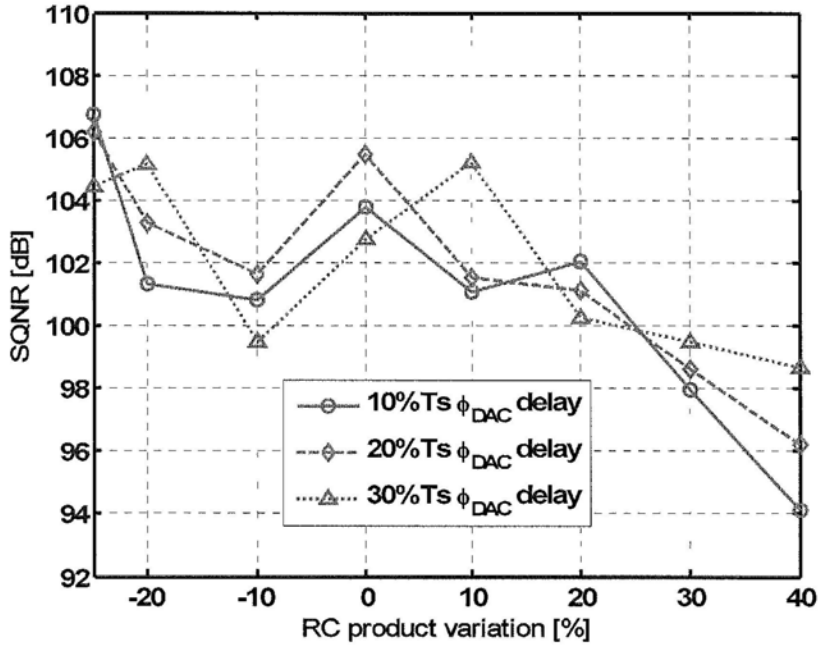


Fig 4.4 Matlab simulation results: SQNR versus RC product variation for different delay with *Vin*=0*dB* V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

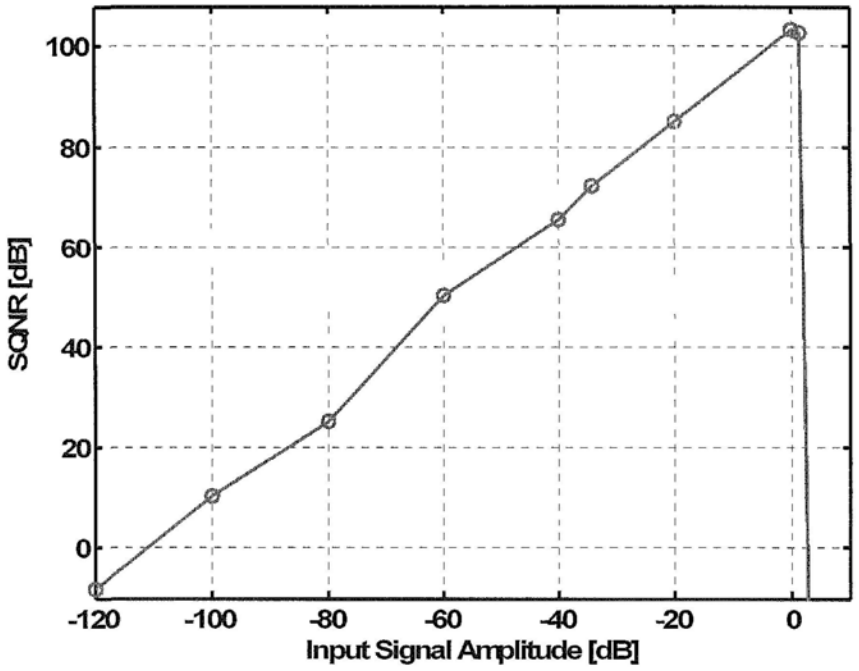


Fig 4.5 Matlab simulation results: SQNR versus V_{in}.

Fig 4.4 shows the SQNR simulated with V_{in} fixed at $0dB$ V_{FS} for an RC product variation from -25% to +40% under different DAC delay. The simulation results show that the SQNR of the modulator is better than $94dB$ over a large range of RC and DAC delay variations. The simulated SQNR across the input range is given in Fig 4.5.

4.3 Circuit Implementation and Noise Analysis

4.3.1 Circuit Implementation

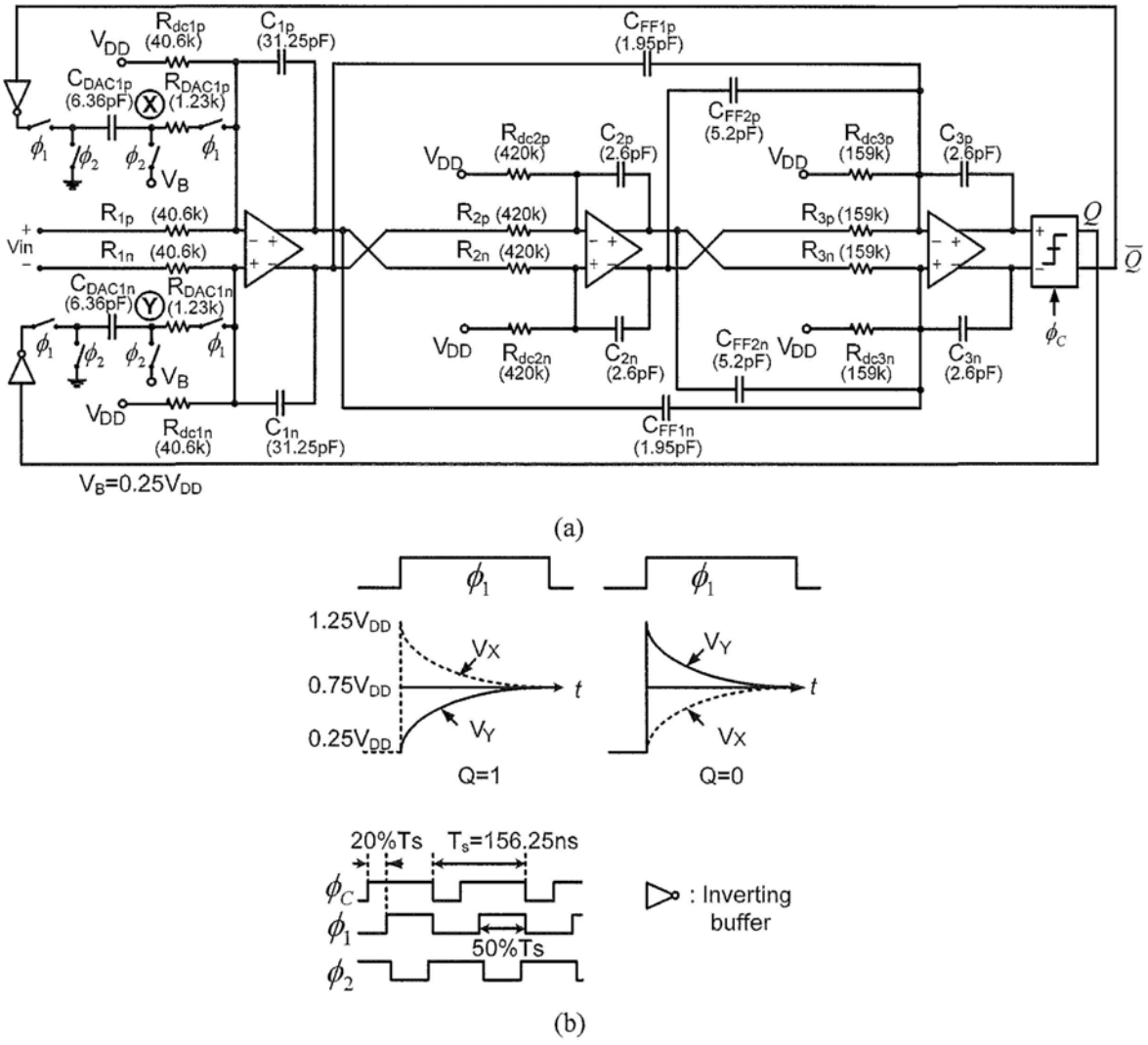


Fig 4.6 Proposed ULV 3rd order CIFF architecture CT ΔΣ modulator with SCR feedback: (a) Schematic; (b) SCR waveform.

The fully differential CIFF CT ΔΣ modulator circuit implementation for a 0.5-V supply is shown in Fig 4.6 (a). The resistors and capacitors are designed by the coefficients shown in Fig 4.1. There is only one feedback branch and power consumption can be reduced. The input signal can be up to $1V_{pp,diff}$. The input resistance of first stage is $40.6k\Omega$, which is nearly 1/5 of the resistance in 3rd order CIFB CT ΔΣ modulator discussed in Chapter 3, and thermal noise can be reduced.

The modulator is designed in a 130nm CMOS technology. The $V_{in\,cm}$ of the amplifiers is set to $0.75V_{DD}$ by the same method described in Chapter 3. The DC voltage V_B for the switches controlled by Φ_2 is set at $0.25V_{DD}$. The output CM voltage is set at $0.5V_{DD}$. The feed-forward coefficients are implemented by the ratio of capacitors, such as the ratio between C_{FF1p} and C_{3p} realizes the feed-forward coefficient 0.75 at the first stage.

4.3.2 Noise Analysis

4.3.2.1 Thermal Noise

Fig 4.7 shows a noise model including the first amplifier noise for the first stage of the modulator in single-ended form. The input referred noise including the first amplifier noise can be calculated by the following equation:

$$\overline{v_{neq}^2} = 2\times[BW\cdot 4kTR_1\cdot(1+\frac{R_1}{R_{dc}}+R_1 f_s C_{DAC})]+2\times\overline{v^2{}_{n,amp}}(\frac{R_1}{R_1 // R_{dc} // 1/f_s C_{DAC}})^2 \qquad (4.3)$$

With the R and C values given in Fig 4.6 :

$$R_1=40.6k\Omega,\ R_{dc}=40.6k\Omega,\ C_{DAC}=6.36p\text{F},\ f_s=6.4M\text{Hz}$$

and the simulated first amplifier noise is $1.4\times10^{-12}\,V^2$, we can calculate the first two terms due to R_1 and R_{dc} are $0.672\times10^{-10}\,V^2$, the third term due to the SCR feedback is $0.555\times10^{-10}\,V^2$, and the last term due to the amplifier is $0.372\times10^{-10}\,V^2$, and for $1V_{pp}$ maximum differential signal

amplitude, the thermal-noise-limited SNR of the modulator is 88.9*dB*. The thermal noise is reduced by 5*dB* than the one in Chapter 3. The total noise can be further reduced by decreasing the value of C_{DAC}, or decreasing the value of R_1. However either method will increase the UGB requirement of first amplifier and power consumption.

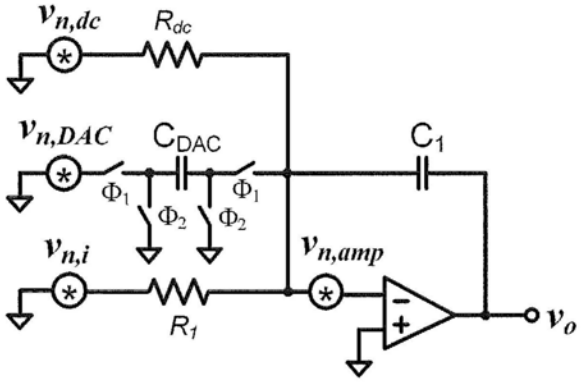


Fig 4.7 Noise model including first amplifier noise for the first integrator.

4.3.2.2 *Clock Jitter Noise*

The clock jitter noise can be calculated according to Eq. (3.17) and (3.18). In this design, there is only one SCR feedback branch, $k_1 = 4.08$, $k_{sig} = 0.12$, $OSR = 128$ and $\tau = 0.05T_S$. For $\sigma_t = 0.01T_s$, the jitter-limited SNR of the modulator is 114*dB*, beyond the limit set by the quantization noise (see Fig 4.4) and thermal noise.

4.4 Circuits Design

In this section, a 0.5V fully differential gate-input amplifier with adaptive CMFB frequency compensation is described. Bias circuits designed with this proposed adaptive compensation method are also given. Then the design details of SCR feedback branch are presented.

4.4.1 Fully Differential Amplifier with Adaptive CMFB Compensation

4.4.1.1 *Schematic of Amplifier*

Fig 4.8 shows the schematic of the proposed 0.5V amplifier with adaptive CMFB compensation [64]. Table 4.1 gives the components values.

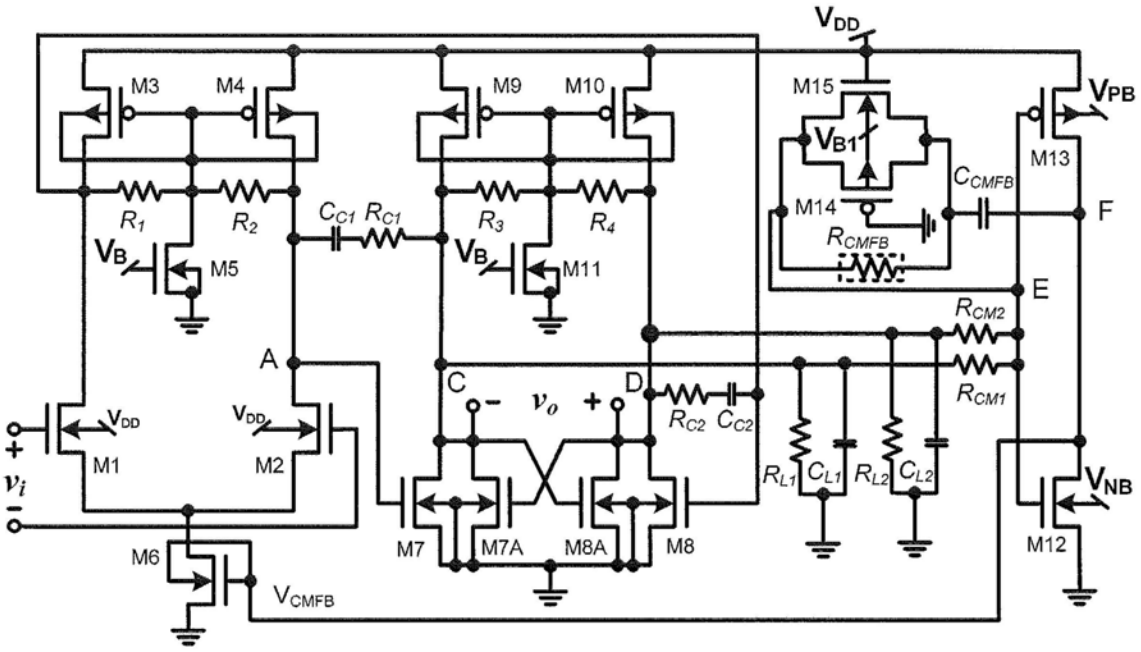


Fig 4.8 Fully differential gate-input amplifier with adaptive CMFB compensation.

Table 4.1 Components values of first amplifier

R_1,R_2,R_{CM1},R_{CM2}=100K	M_6=285/1
R_3,R_4=70K	M_7,M_8=97/1
R_{C1},R_{C2}=1.45K	M_{7A},M_{7B}=5.5/1
R_{L1},R_{L2}=420K	M_9,M_{10}=250/1
C_{L1},C_{L2}=31.25pF	M_{11}=5.5/2
C_{C1},C_{C2}=9.1pF	M_{12}=4/0.36
C_{CMFB}=7.5pF	M_{13}=16.4/0.36
M_1,M_2=420/2	M_{14}=8.2/0.36
M_3,M_4=120/1	M_{15}=2/0.36
M_5=11/2	

In this design, the input transistors size of the first amplifier is increased by 2 times to reduce the amplifier noise. It consists of two stages and an adaptive CMFB compensation stage which uses a pair of transistors to trace the g_m variation of error amplifier for robust frequency compensation against process variation. The designed values for input and output common-mode

(CM) voltage are 0.375V and 0.25V ($V_{DD}/2$) separately. The higher input CM voltage is to provide a sufficient gate voltage to get high transconductance, and also provide enough turn on/off voltage for switches which are placed in SCR feedback branch. The output CM voltage is chosen to maximize the output swing.

The first stage of amplifier uses a gate-input differential pair biased with a tail current source, which is controlled by a common-mode feedback signal, V_{CMFB}. The bodies of the input pair are tied to V_{DD} to lower its threshold voltage. M_3, M_4, M_5, R_1 and R_2 form a local CMFB loop. The second stage of amplifier uses a gate-input differential pair without a tail current. A negative g_m pair, M_{7A} and M_{8A}, is used to reduce the differential output conductance between nodes C and D to enhance its DC gain. The CMFB stage uses the error amplifier to compare the output CM voltage with $V_{DD}/2$, amplify their difference, and feed back the CM error signal to the gate of M_6 to pull the output CM voltage to $V_{DD}/2$.

Frequency compensation is needed to stabilize the CMFB loop, and it cannot affect the differential mode loop stability. In this design, a pair of transistors, M_{14} and M_{15} working in linear region are used as compensation resistor to trace the g_m variation of the error amplifier, which leads to robust frequency compensation against process and temperature variation.

For differential-mode (DM) signals, there are two poles and a left-half-plane (LHP) zero. Two poles are located at node A, C separately. At node A, there is a dominant pole P_1, which is:

$$P_1 = \frac{1}{(Av_2 \times C_{C1} + C_{out1}) \times R_{out1}})^2 \tag{4.4}$$

where A_{V2} is the DM voltage gain of the second stage and R_{out1}, C_{out1} are the DM output resistance and capacitance of the first stage. At node C, there is a second pole P_2, which is:

$$P_2 = \frac{1}{(C_{L1} + C_{out2}) \times R_{out2}} \tag{4.5}$$

where R_{out2}, C_{out2} are the DM output resistance and capacitance of the second stage. V_E is a virtual ground for DM signals and C_{cmfb} does not appear as a DM load at node C and D.

The LHP zero is given by:

$$Z_1 = \frac{-1}{C_{C1}(R_{C1} - 1/g_{m7})} \tag{4.6}$$

By properly choosing the value of C_{C1} and R_{C1}, a good phase margin can be achieved for differential mode loop.

There are three stages in the CMFB loop: the error amplifier, the first and second stages. The CM gain of the first stage $A_{V1,\,cm}$ is:

$$A_{V1,cm} = \frac{g_{m6}}{g_{m4} + g_{mb4} + g_{ds4}} \tag{4.7}$$

The CM voltage gain of the second stage $A_{V2,\,cm}$ is:

$$A_{V2,cm} = \frac{g_{m7}}{g_{m9} + g_{mb9} + g_{ds9} + g_{ds7} + g_{m7A} + g_{ds7A}} \tag{4.8}$$

which is very small.

The CM voltage gain of error amplifier $A_{V3,\,cm}$ is:

$$A_{V3,cm} = \frac{g_{m12} + g_{mb12} + g_{m13} + g_{mb13}}{g_{ds12} + g_{ds13}} \tag{4.9}$$

For the CM loop, there is a pole $P_{1,cm}$ at node A, which is:

$$P_{1,cm} = \frac{1}{(Av_{2,cm} \times C_{C1} + C_{out1}) \times R_{out1,cm}} \tag{4.10}$$

where $R_{out1,cm}$ is the CM output resistance of the first stage, it equals to $1/(gm4+gmb4+gds4)$. Note that the differential mode Miller capacitor C_{C1} is not amplified for CM signals because $A_{V2,cm}$ is very small.

The small signal model for circuit from node A to node E is shown in Fig 4.9. V_E can be expressed as a function of V_A:

$$V_E = g_{m7}V_A \times [R_{out2,cm} \parallel R_{L1} \parallel \frac{1}{S(C_{L1}+C_{out2})} \parallel (R_{CM1} + \frac{1}{SC_M})] \times \frac{\frac{1}{SC_M}}{R_{CM1} + \frac{1}{SC_M}} \tag{4.11}$$

where $R_{out2,cm}$ is the CM output resistance of the second stage, it is $1/(g_{m9}+g_{mb9}+g_{ds9}+g_{ds7}+g_{m7A}+g_{ds7A})$. $R_{out2,cm}||R_{L1}$ is smaller than R_{CM1}, so transfer function from A to E is:

$$\frac{V_E}{V_A} \approx \frac{g_{m7} \times (R_{out2,cm} \parallel R_{L1})}{(1+\frac{s}{1/[(R_{out2,cm} \parallel R_{L1}) \times (C_{L1}+C_{out2})]})(1+\frac{s}{1/(R_{CM1} \times C_M)})} \tag{4.12}$$

There are two poles, the second pole $P_{2,cm}$ is:

$$P_{2,cm} = \frac{1}{(R_{out2,cm} \parallel R_{L1}) \times (C_{L1}+C_{out2})} \tag{4.13}$$

the third pole $P_{3,cm}$ is:

$$P_{3,cm} = \frac{1}{R_{CM1} \times C_M} = \frac{1}{R_{CM1} \times C_{CMFB} \times A_{v3,cm}} \tag{4.14}$$

$P_{3,cm}$ is a dominant pole.

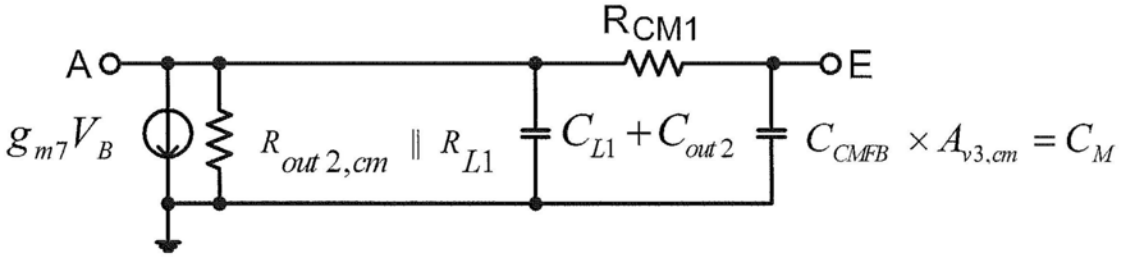


Fig 4.9 CM small signal model of second stage.

Another pole exits at node F, $P_{4,cm}$ is:

$$P_{4,cm} = \frac{g_{ds12} + g_{ds13}}{c_{gs6}} \tag{4.15}$$

$P_{3\,cm}$ is the first dominant pole, $P_{4\,cm}$ is the second dominant pole, $P_{1\,cm}$ and $P_{2\,cm}$ are far away from $P_{4\,cm}$ as g_m is much larger than g_{ds}.

A zero is formed by R_{CMFB}, C_{CMFB}, and M_{12}, M_{13}, which is expressed as:

$$Z_{1,cm} = \frac{-1}{C_{CMFB} \times [R_{CMFB} - 1/(g_{m12} + g_{m13})]} \tag{4.16}$$

g_{m12}, g_{m13} are given by:

$$g_{m12} = \mu_n C_{ox} (W/L)_{12} (V_{GS} - V_{thn}) \approx \mu_n C_{ox} (W/L)_{12} (\frac{V_{DD}}{2} - V_{thn}) \tag{4.17}$$

$$g_{m13} = \mu_p C_{ox} (W/L)_{13} (|V_{GS}| - |V_{thp}|) \approx \mu_p C_{ox} (W/L)_{13} (\frac{V_{DD}}{2} - |V_{thp}|) \tag{4.18}$$

(g_{m12}+g_{m13}) varies a lot when process corner and temperature change from slow-slow to fast-fast, from -27°C to 85°C respectively as shown in Fig 4.10. This is because of that V_{thn}, V_{thp} vary widely from 170mv to 370mv, which leads to transistors working in different region and large transconductance variation. However, R_{CMFB} cannot cover a large range to make $Z_{1\,cm}$ always in LHP, which results in poor phase margin (PM).

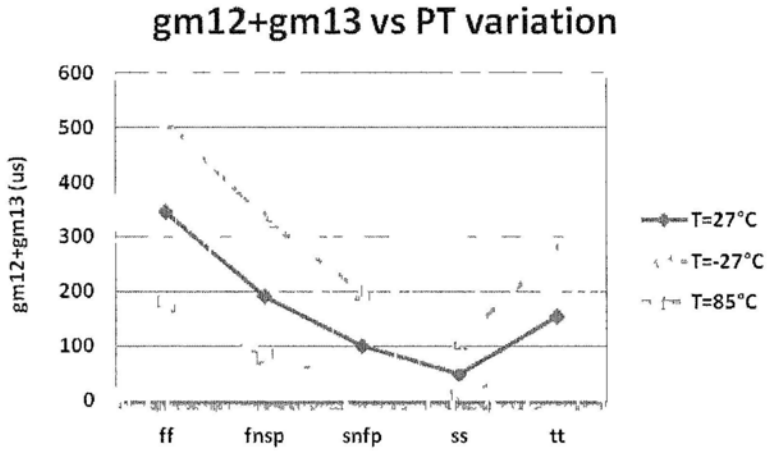


Fig 4.10 (gm_{12}+gm_{13}) variation vs PT variation.

An adaptive compensation method is proposed to solve this problem. The R_{CMFB} is replaced by a pair of transistors working in linear region to trace the g_m variation of M_{12} and M_{13}. As V_E is around $V_{DD}/2$, so the on-resistance of M_{14}, M_{15} are:

$$r_{on14} = \frac{1}{\mu_p C_{ox}(W/L)_{14}(|V_{GS}|-|V_{thp}|)} \approx \frac{1}{\mu_p C_{ox}(W/L)_{14}(\frac{V_{DD}}{2}-|V_{thp}|)} \tag{4.19}$$

$$r_{on15} = \frac{1}{\mu_n C_{ox}(W/L)_{15}(V_{GS}-V_{thn})} \approx \frac{1}{\mu_n C_{ox}(W/L)_{15}(\frac{V_{DD}}{2}-V_{thn})} \tag{4.20}$$

So the zero becomes:

$$Z_{1,cm} = \frac{-1}{C_{CMFB}\times[(r_{on14}\,||\,r_{on15})-1/(g_{m12}+g_{m13})]} \tag{4.21}$$

It's necessary to make $(W/L)_{14}<(W/L)_{13}$ and $(W/L)_{15}<(W/L)_{12}$ In this design, $(W/L)_{14}=0.5(W/L)_{13}$, $(W/L)_{15}=0.5(W/L)_{12}$, and $Z_{1,cm}$ is always in LHP. The PM of the CMFB loop is at least 45° for different process and temperature corners.

The biasing generation circuits for V_{PB}, V_{NB}, V_B and V_{B1} are adopted from the one reported in [62]. The adaptive compensation method can also be used in this circuit. Fig 4.11 shows the modified bias circuit for V_{PB}, V_{NB} and V_{B1}, where R_{C1} is replaced by a pair of transistors. The bias circuit in Fig 4.12 shows the modified bias circuit for V_B, where R_{C2} is replaced by a pair of transistors.

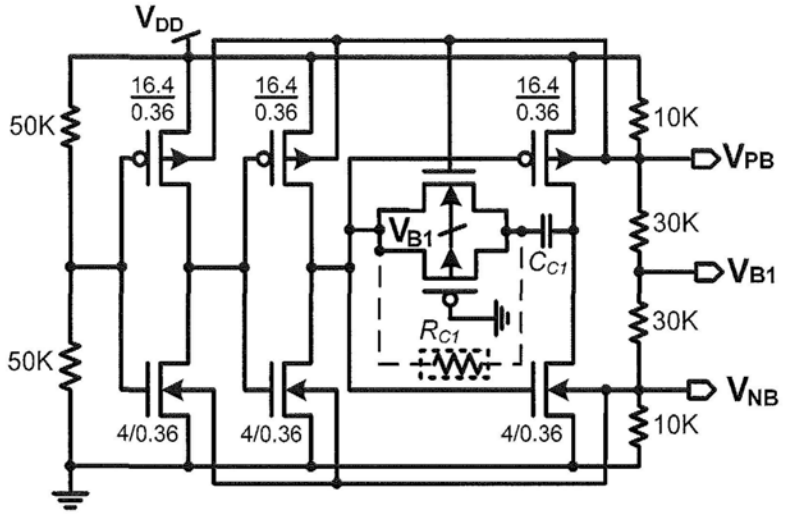


Fig 4.11 Bias circuit with adaptive compensation for V_{PB}, V_{NB} and V_{B1}.

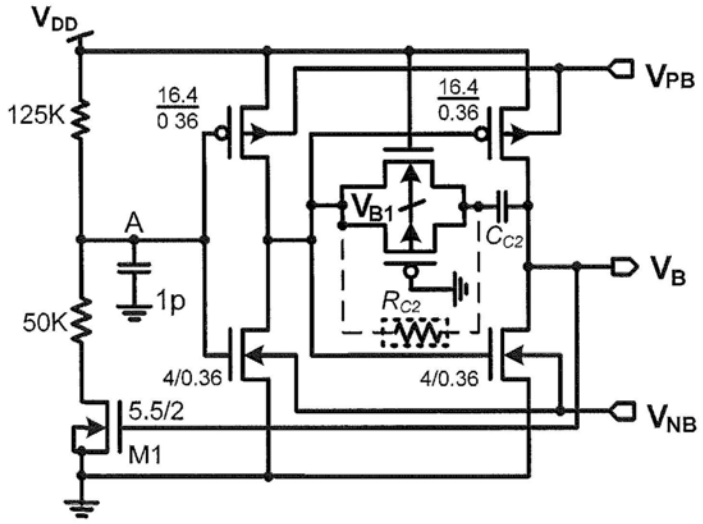


Fig 4.12 Bias circuit with adaptive compensation for V_B.

4.4.1.2 Simulation Results of Amplifier

The frequency responses of first amplifier over PVT corners (-27 °C to 85 °C, 0.45V to 0.55V, and slow, nominal and fast process corners) are shown in Fig 4.13.

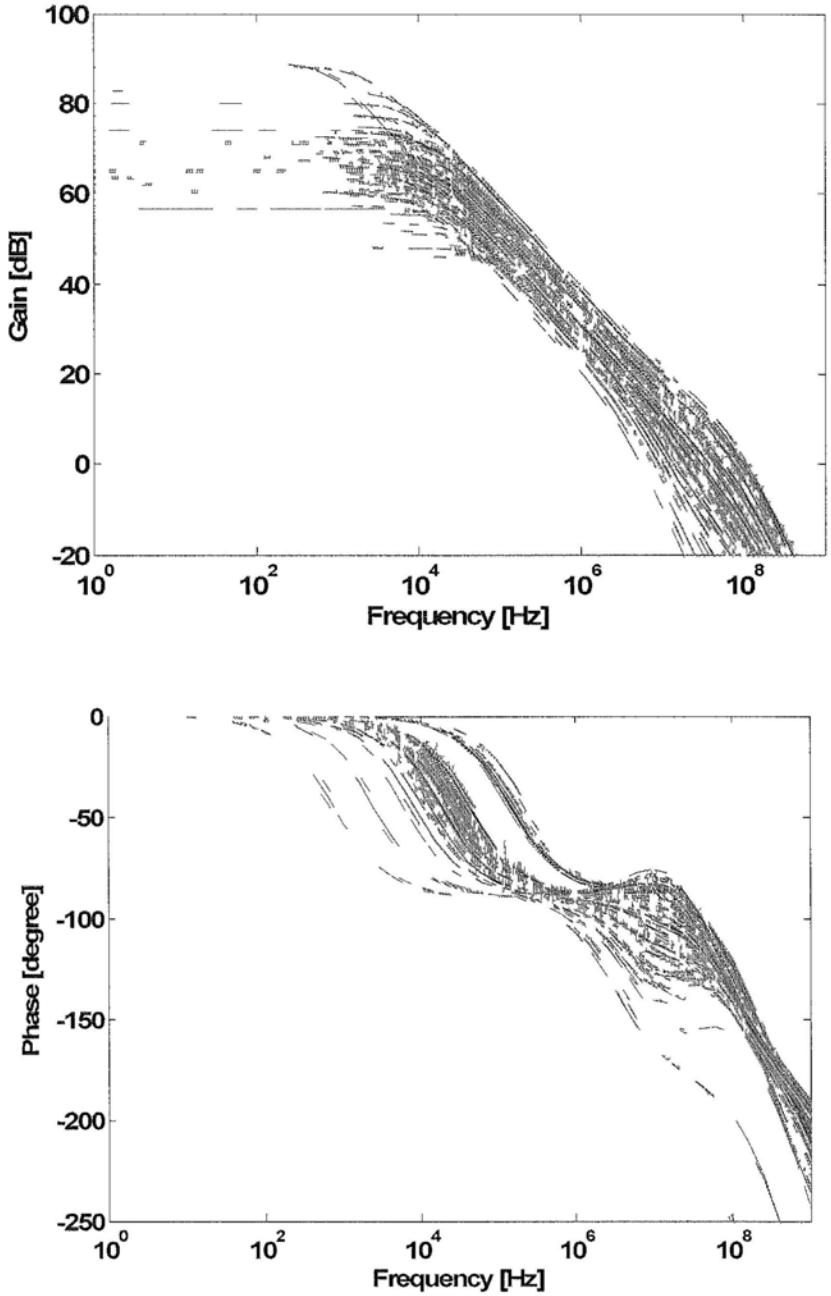


Fig 4 13 Frequency responses of the first amplifier over PVT corners

The CMFB loop frequency responses of the first amplifier over PT corners are shown in Fig 4 14 The PM of the CMFB loop is at least 45° for PT corners.

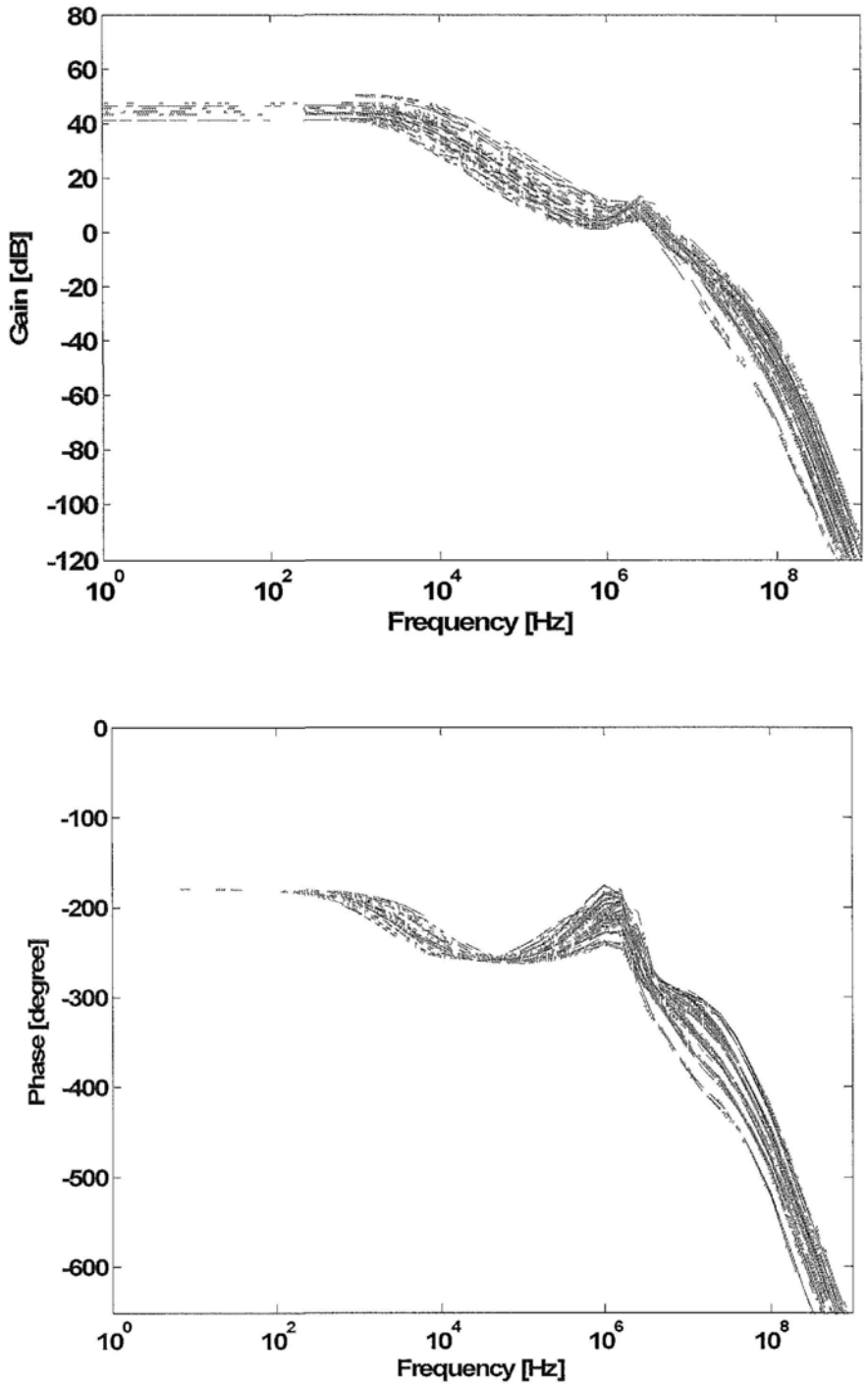


Fig 4.14 CMFB loop frequency responses of the first amplifier over PT corners.

The simulated performance of the amplifier is shown in Table 4.2. The amplifiers for the three $\Delta\Sigma$ modulator stages are scaled as 1:0.25:0.15.

Table 4.2 Simulation performance of the amplifiers.

Parameters	AMP-1	AMP-2	AMP-3
Supply(V)	0.5	0.5	0.5
Power Consumption(μW)	428	106	63.4
Open loop DC Gain (dB)	68	55	49
UGB/PM (MHz / degree)	52 / 65	41 / 70	60 /62
Input ref.noise @1KHz/1MHz (nV/sqHz)	12/ 2.9	46 / 7.2	65 /10
CMRR@DC (dB)	137	121	114
SR+/SR- (V/μs)	7.7 / 7.7	5.6 /5. 6	7.1/ 7.1
Load(pF// kΩ)	33.2 // 420	7.8 // 160	2.6

4.4.2 SCR feedback DAC

There is only one SCR DAC branch feedback to the first stage. The C_{DAC} is 6.36pF, and the R_{DAC} is 1.23$k\Omega$. In order to reduce the turn on resistances of transistor switches in series with R_{DAC}, the switches size are increased. Fig 4.15 shows the transistor level schematic of the SCR DAC.

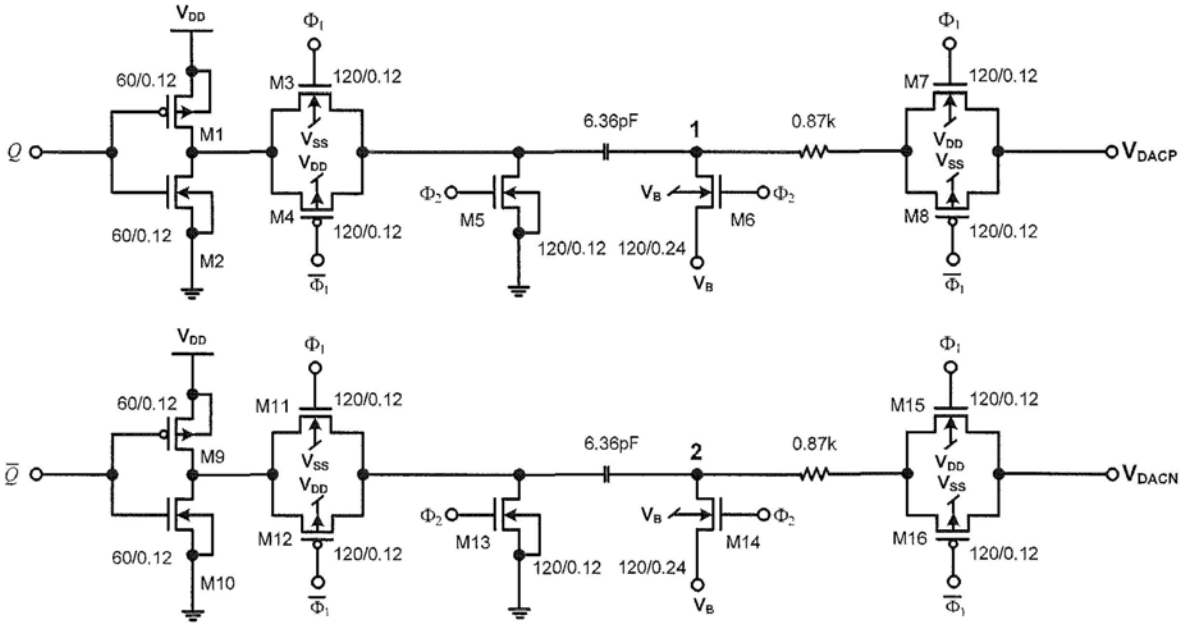


Fig 4.15 SCR DAC circuit.

In this circuit, M_7-M_8 and M_{15}-M_{16} are body-biased to reduce the turn on resistances. The minimum voltage at node 1 is V_B which is $0.25V_{DD}$, and the maximum voltage at node 1 is $1.25V_{DD}$, so the maximum forward-biased body-source junction is $0.75V_{DD}$, the risk for latch-up is rare when V_{DD} is 0.5V [61].

4.5 System Simulation Results

4.5.1 Pre-Layout Simulation Results

Fig 4.16 shows the output spectrum obtained from transistor-level simulation for the ΔΣ modulator with a 4.3*k*Hz full-scale sinusoidal input (V_{in}=0*dB* V_{FS}, where V_{FS}=$1V_{pp,diff}$). The simulated SNDR is 104*dB* over 25-*k*Hz bandwidth.

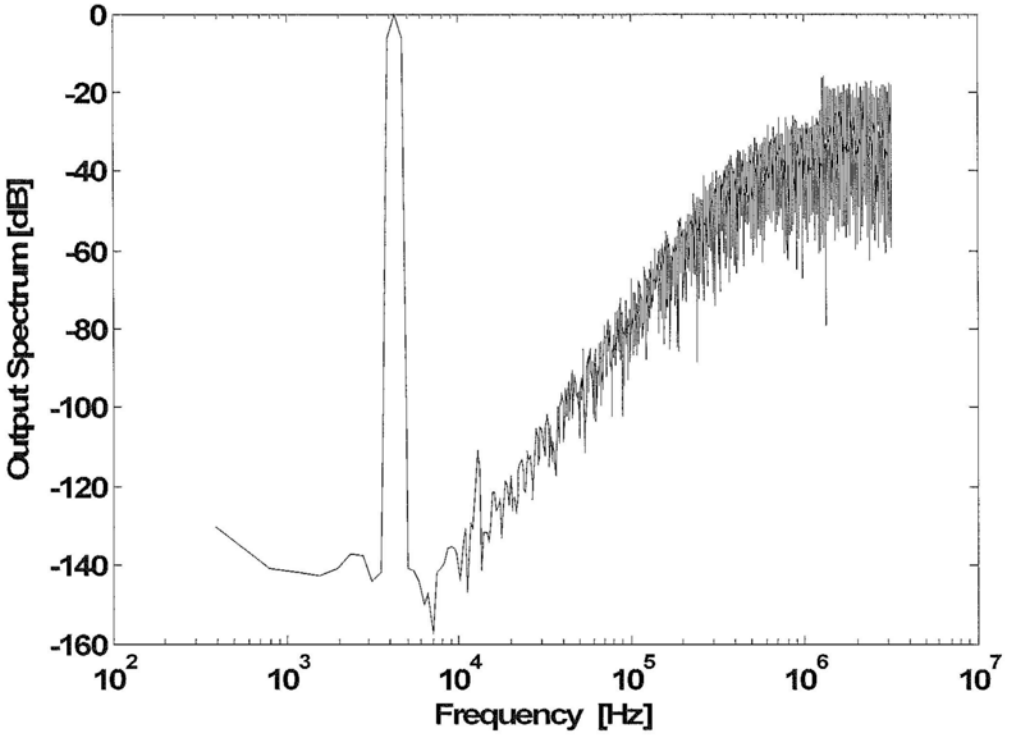


Fig 4.16 Output spectrum: transistor-level simulation CIFF architecture CT ΔΣ modulator with V_{in}=0*dB* V_{FS} (V_{FS}=$1V_{p-p,diff}$), f_{in}=4.3*k*Hz.

Table 4.3 shows the different corner simulation results for different supply voltage at

room temperature.

Table 4.3 Corner simulation results for the modulator.

Power Supply (V)	**0.45**	**0.5**	**0.55**
Temperature (°C)	27	27	27
Fin (*k*Hz)	4.3	4.3	4.3
Vin ($V_{p\text{-}p,diff}$)	0.9	1	1
SNDR@ TT (dB)	100.5	104	99.5
SNDR @ FF (dB)	101	100	102
SNDR @ SS (dB)	100.8	102.8	100
SNDR @ FNSP (dB)	98.5	99.6	103
SNDR @ SNFP (dB)	98	101	101

Fig 4.17 shows the simulated SNDR for a V_{DD} between 0.45V and 0.8V at room temperature. All the results show the performance of the modulator is consistent over a lager range of temperature as well as supply voltage.

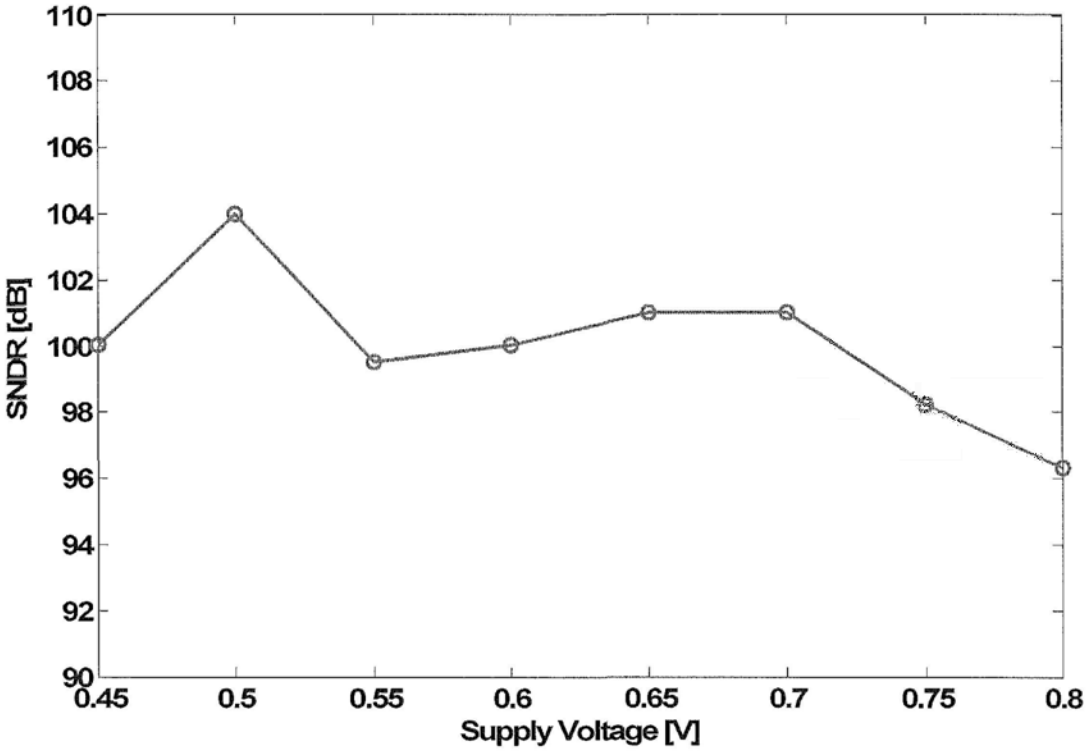


Fig 4.17 SNDR versus supply voltage at T=27°C.

4.5.2 Post-Layout Simulation Results

For layout placement consideration, the common-centroid technique and symmetrical wire-routing method are used to eliminate the mismatch effects on the performance of modulator. And the ratios between feed-forward capacitors are well controlled by placing those capacitors close to each other and using the same unit capacitor to build them.

The post-layout simulation result is shown in Fig 4.18. The input signal is a 4.3*k*Hz full-scale sinusoidal waveform (V_{in}=0*dB* V_{FS}, where V_{FS}=1$V_{pp,diff}$). The simulated SNDR is 101*dB* over 25-*k*Hz bandwidth.

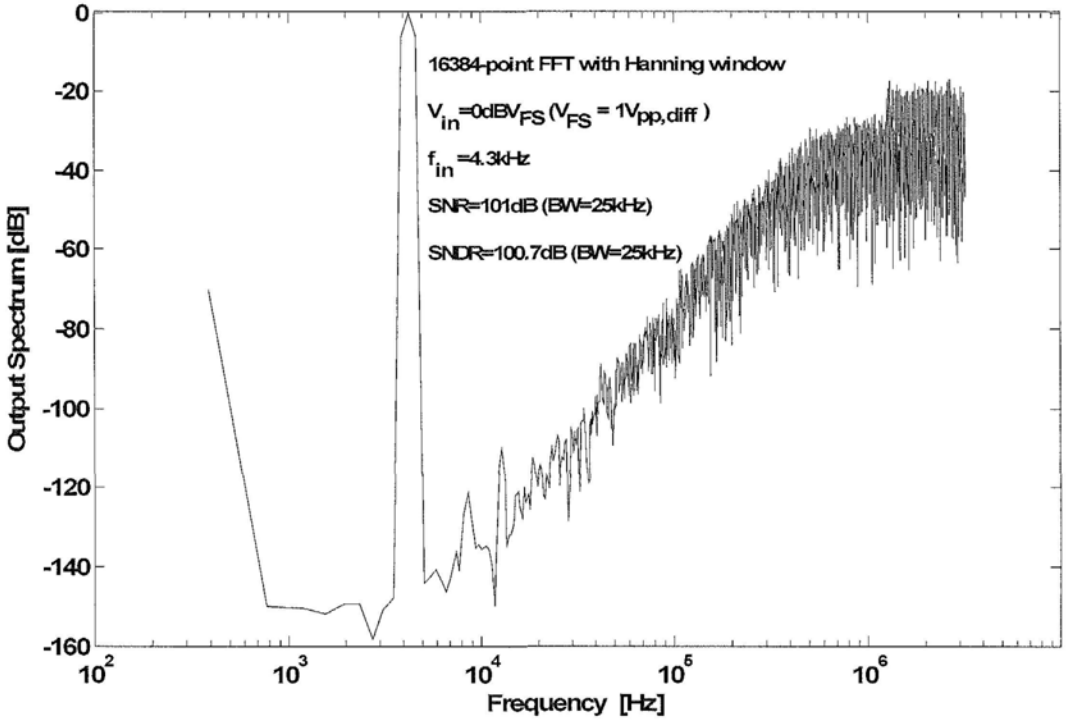


Fig 4.18 Post-layout simulation result with V_{DD}=0.5V, T=27°C.

4.6 Experimental Results

4.6.1 Chip Photograph

The die photo is shown in Fig 4.19. The circuit occupies an active area of is $0.85mm^2$. The modulator was fabricated in a 0.13μm CMOS triple-well process with standard V_T devices. Metal-insulator-metal (MIM) capacitors and high-resistivity poly resistors were used. Nine packaged chips have been tested and they perform consistently with results reported below.

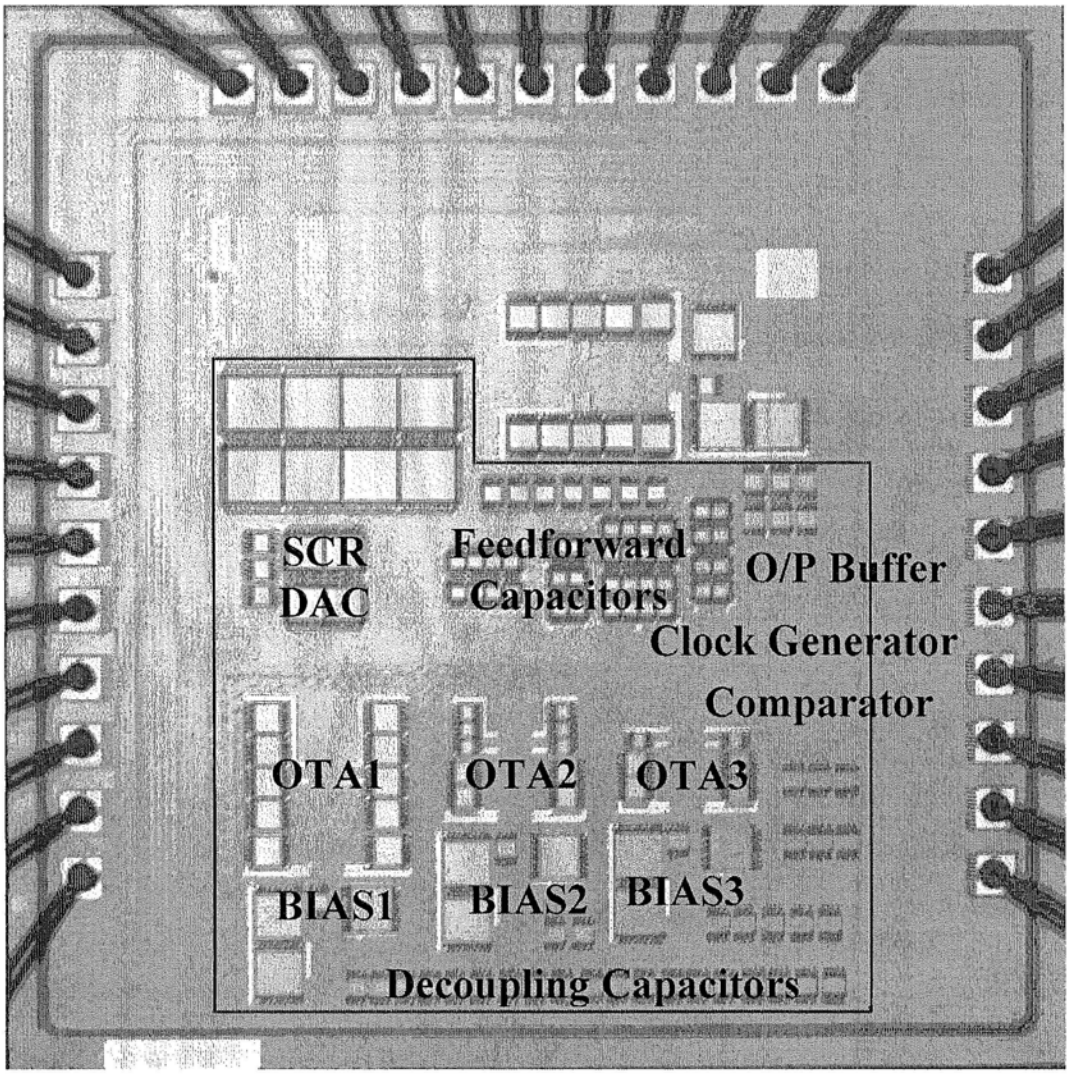


Fig 4.19 Die photograph of 0.5V CIFF architecture CT SCR ΔΣ modulator.

4.6.2 PCB Design

The measurement setup is nearly the same as the one in Fig 3.20. The complete PCB for the ΔΣ modulator measurement is shown in Fig 4.20. A 4.7*n*F and a 22*n*F decoupling capacitors

are placed near the power supplier pins and DC biasing source pins A 1000uF by-pass capacitor is placed between the power suppliers and ground The output data of $\Delta\Sigma$ modulator is recorded by a logic analyzer with Φ_2 as the synchronized clock and processed by Matlab^{TM}

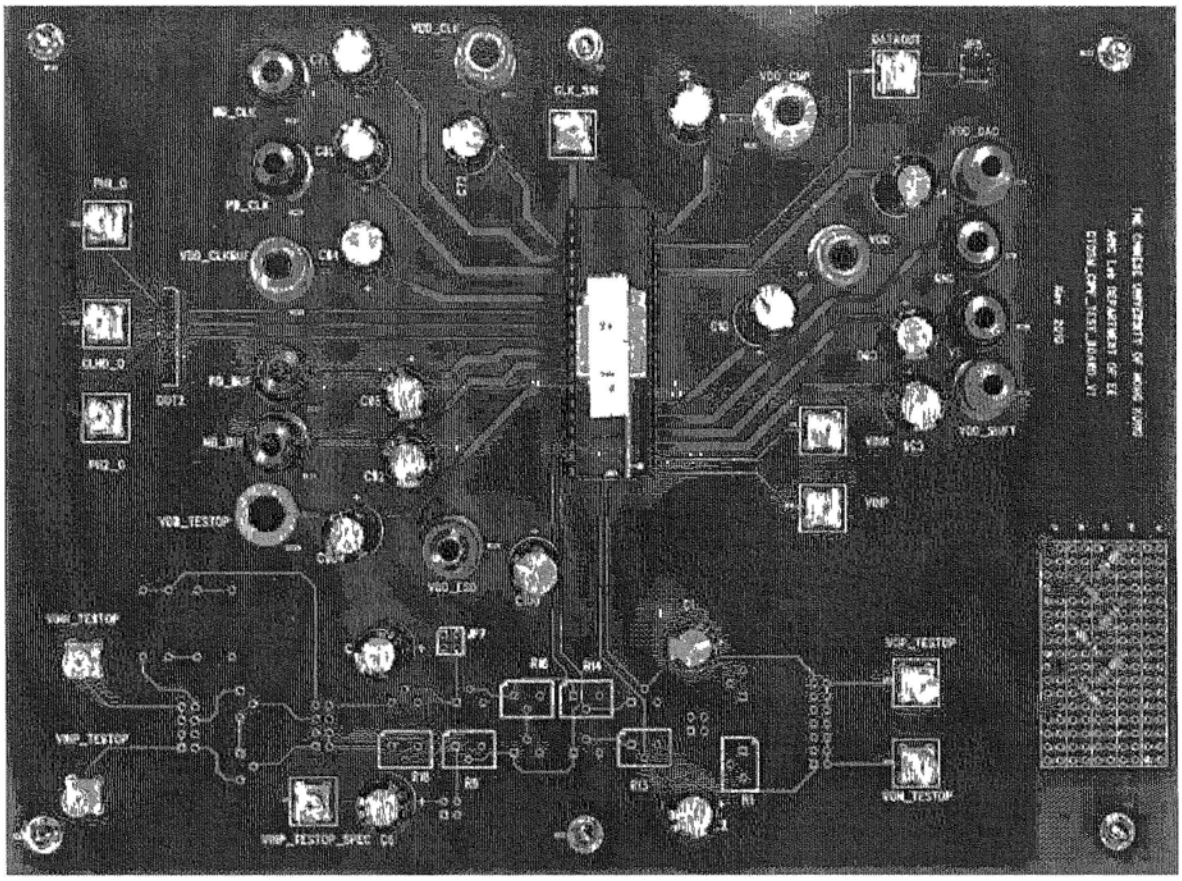


Fig 4 20 Photograph of PCB board

4.6.3 Measurement Results

Fig 4.21 shows a measured output spectrum with a 1kHz near -full-scale sinusoidal input (V_{in} = 0dB V_{FS}, where V_{FS}= 1$V_{pp,diff}$) at room temperature There are virtually no harmonic tones and the spurious-free dynamic range (SFDR) is 101 9dB

Fig 4.22 shows the measured SNDR and SNR across the input range. The modulator records a peak SNDR, a peak SNR and a dynamic range (DR) of 87 76dB, 87.96dB and 86dB respectively for 25-kHz signal bandwidth. At 0.5V, the modulator consumes 682.5μW.

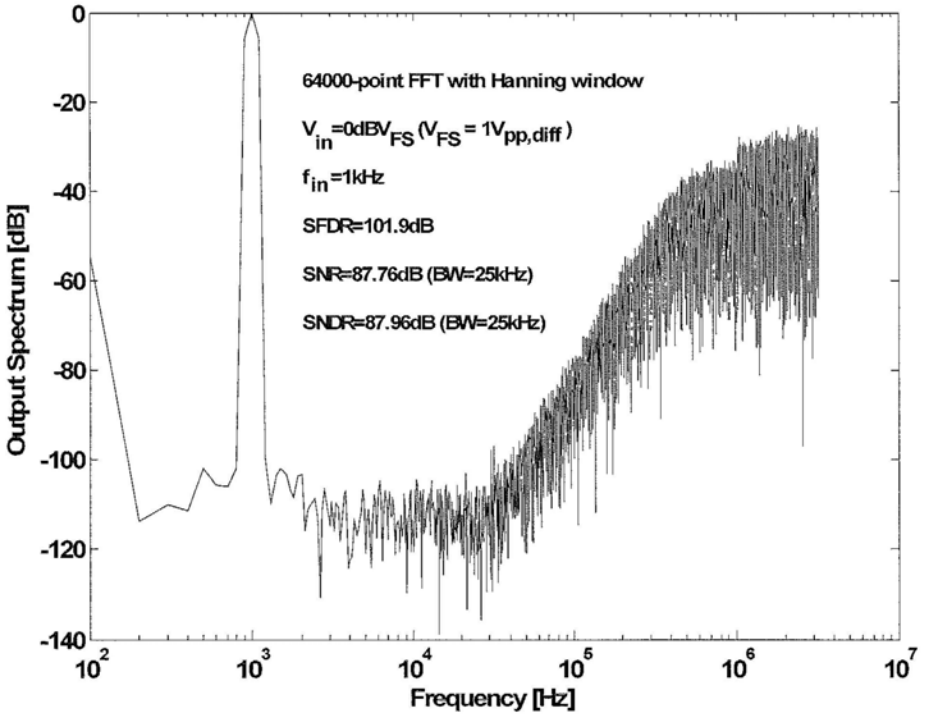


Fig 4.21 Measured output spectrum with V_{DD}=0.5V, T=25°C.

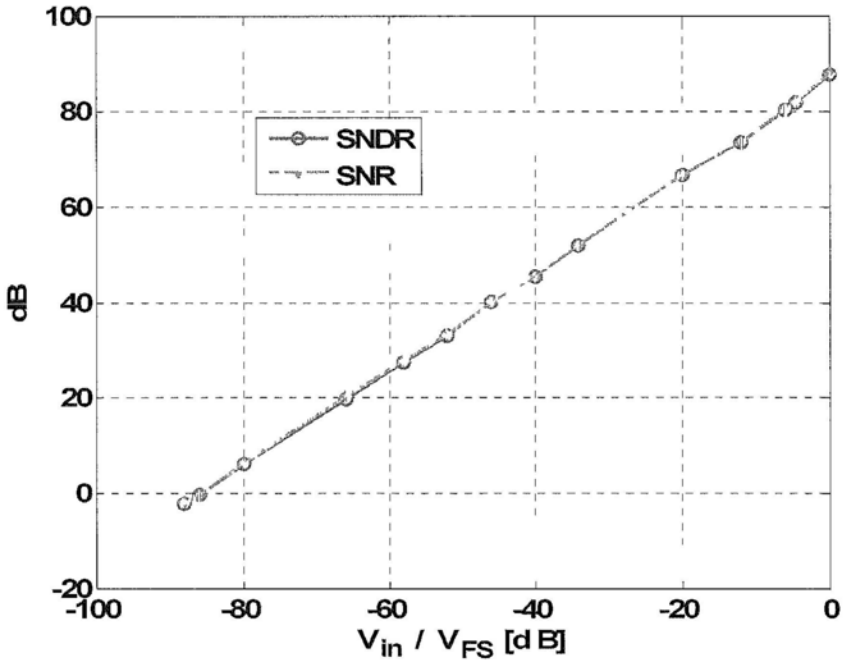


Fig 4.22 Measured SNDR and SNR versus V_{in}, V_{DD}=0.5V, T=25°C.

Table 4.4 summarizes the measured performance of the modulator at room temperature. For the nominal V_{DD} of 0.5V, a peak SNDR of 87.76*dB* is achieved in a 25-*k*Hz bandwidth for a nearly full range differential input signal of $1V_{p\text{-}p,diff}$, and 682.5μW power consumed by the modulator and 70.5μW power by the output buffers. For a 20-*k*Hz bandwidth, the peak SNDR and SNR are 90*dB* and 90.48*dB* respectively with A-weighting on the spectrum.

Table 4.4 Measured modulator performance at 25°C

Modulator type	**1-bit, 3rd order, CIFF, CT**
Signal bandwidth	25kHz
Sampling frequency/OSR	6.4MHz/128
Input signal range	$1V_{ppdiff}$
Supply voltage	0.5V
Peak SNR	87.96dB@BW=25kHz 88.77dB@BW=20kHz 90.48dB@BW=20kHz, A-weighted
Peak SNDR	87.76dB@BW=25kHz 88.5dB@BW=20kHz 90dB@BW=20kHz, A-weighted
Dynamic Range	86dB@BW=25kHz 87dB@BW=20kHz 89dB@BW=20kHz, A-weighted
SFDR @ Vin=$1V_{ppdiff}$	101.9dB
Power consumption (total) Modulator Output buffers	753µW 682.5µW 70.5µW
Active die area	$0.85mm^2$
Technology	0.13µm CMOS, standard V_T MIM capacitors, and HiRes Poly

The input clock is generated by the same equipment as the previous chip. According to input clock jitter measurement results in Chapter 3, the jitter-induce noise is not limiting the performance. The measured peak SNR of 87.96*dB* is close to the 88.9*dB* thermal noise limit. The SNR improvement is 6.66*dB* compared with the previous chip due to this CIFF architecture. And the power consumption is 57.5 μW higher than the previous chip due to the process variation. The chip size is $0.05mm^2$ larger than the previous chip due to large feed-forward capacitors.

Fig 4.23 shows the measured SNR and SNDR for a V_{DD} between 0.4V and 0.75V at the room temperature with a fixed input magnitude of 1 $V_{p\text{-}p,diff}$ except the one under 0.4V supply. When V_{DD} is 0.4V, the input magnitude is $0.8V_{p\text{-}p,diff}$. The SNDR variation is within 2.96*dB* and an SNR variation is within 3.06*dB*. Thanks to the proposed adaptive biasing technique, the modulator's performance is very consistent with its nominal performance across a wide supply voltage range.

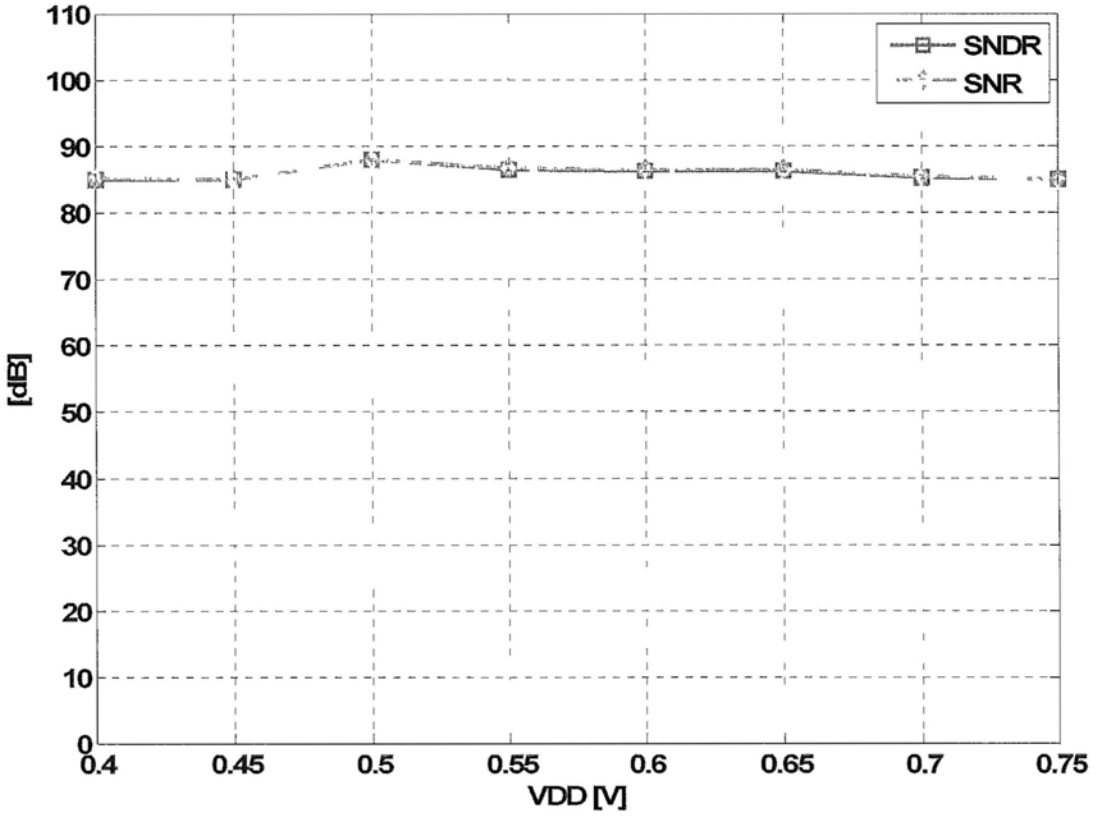


Fig 4.23 Measured SNR and SNDR versus supply voltage from 0.4V to 0.75Vwith *Vin* fixed at 1 $V_{p\text{-}p,diff}$, T=25°C.

Fig 4.24 shows the measured SNR and SNDR for temperature changing between -20°C and 90°C at V_{DD} =0.5V for a fixed input level of 1 $V_{p\text{-}p,diff}$. The SNDR variation is less than 3.7*dB* and SNR variation is less than 2*dB* for this temperature range. The SNDR remains over

84*dB* over the wide temperature range. The modulator's performance is also very consistent with its nominal performance across a wide temperature range due to the proposed adaptive biasing technique.

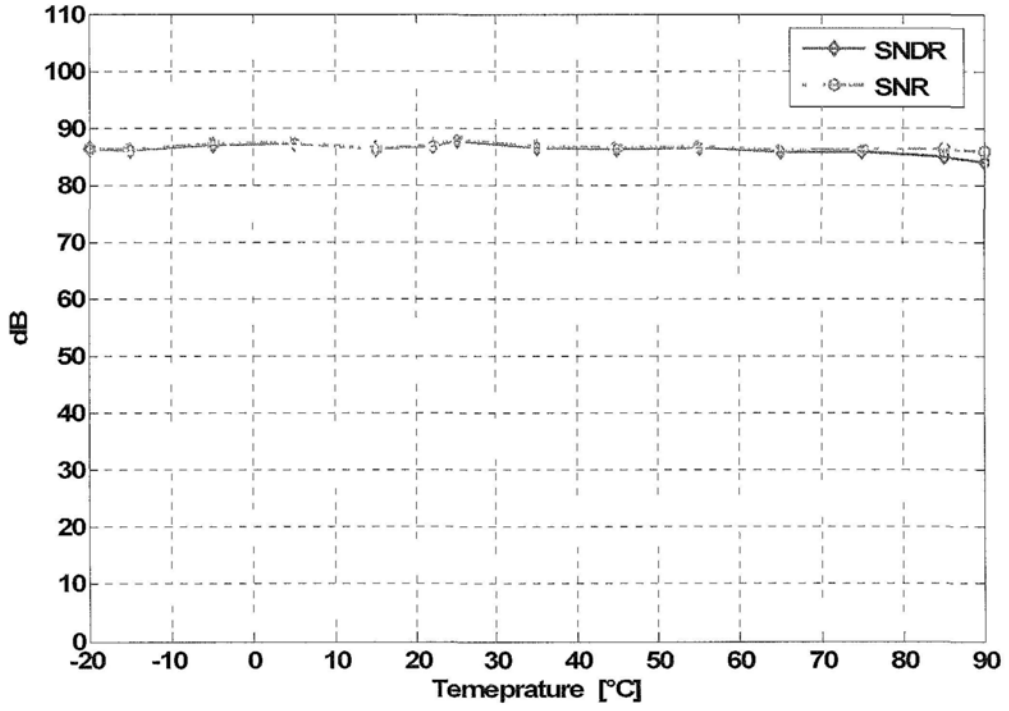


Fig 4.24 Measured SNR and SNDR versus temperature from -20°C to 90°C with *Vin* fixed at 1 $V_{p\text{-}p,diff}$, V_{DD}=0.5V.

According to Eq. (3.20), the FoM is 0.68*pJ*/conversion for the presented ΔΣ modulator. It is nearly half of the previous chip. The presented modulator has the best SNDR for modulators operating at 0.7V or below listed in Table 1.1 while not using any special process option.

4.7 Summary

This chapter presents a fully-differential CIFF architecture CT ΔΣ modulator with SCR feedback for a 0.5V supply while using standard V_T. The modulator achieves 6.66dB SNR

improvement compared with the previous chip while keep nearly the same power consumption. The 0.5V fully differential gate-input amplifier with adaptive CMFB frequency compensation and bias circuits designed with this proposed adaptive compensation method are key enablers for this design.

The 130nm CMOS modulator achieves an excellent linearity performance of 101.9dB SNDR and an excellent SNDR of 87.76dB over 25-kHz signal bandwidth while consuming 682.5μW at 0.5V supply. The measured performance is consistent across a wide supply voltage range from 0.4V to 0.75V and over the commercial temperature range.

Chapter 5

Design of a Cascaded Continuous-Time Delta-Sigma Modulator at 0.5V

5.1 Introduction

Among reported CT ΔΣ modulators, there are very few cascaded modulator [65]. The cascaded CT modulator has the potential of providing a better input coefficient because its first stage is of a low order, thus a lower thermal noise is expected. This chapter focuses on it. A new synthesis method for the cascaded CT ΔΣ modulator is proposed. The coefficients for each stage are obtained by a discrete-time to continuous-time transformation. A detailed derivation of the digital cancellation logics for modulators based on discrete-time domain analysis is presented which leads to a simple implementation of circuits and is capable of correcting the effect of *RC* value variation. The proposed synthesis method is applied to a 0.5-V 2-1 cascaded continuous-time ΔΣ modulator with SCR feedback. Transistor-level simulations show that a $98dB$ SNDR is achieved over a 25-*k*Hz signal bandwidth with a 6.4MHz sampling frequency and $350\mu W$ power consumption under a 0.5-V supply.

5.2 Review of Synthesis Methodologies for Cascaded CT ΔΣ modulators

There are two kinds of methodologies to synthesize a cascaded CT ΔΣ modulator. The first one uses the direct synthesis method [66]-[67], and the other one applies impulse-invariant loop filter equivalence method to convert a DT ΔΣ modulator to a CT one [68]-[71]. For the first method, it is difficult to achieve an optimized design [71]. The second method either employs

too many forward signal paths between stages [68]-[70], which increase the analog circuit complexity, power consumption due to the increased loading of stages, or adds analog switches between stages [71] making it difficult for ULV implementation.

5.2.1 Direct Synthesis Method

Fig 5.1 shows the scheme of the cascaded CT ΔΣ modulator with direct synthesis method.

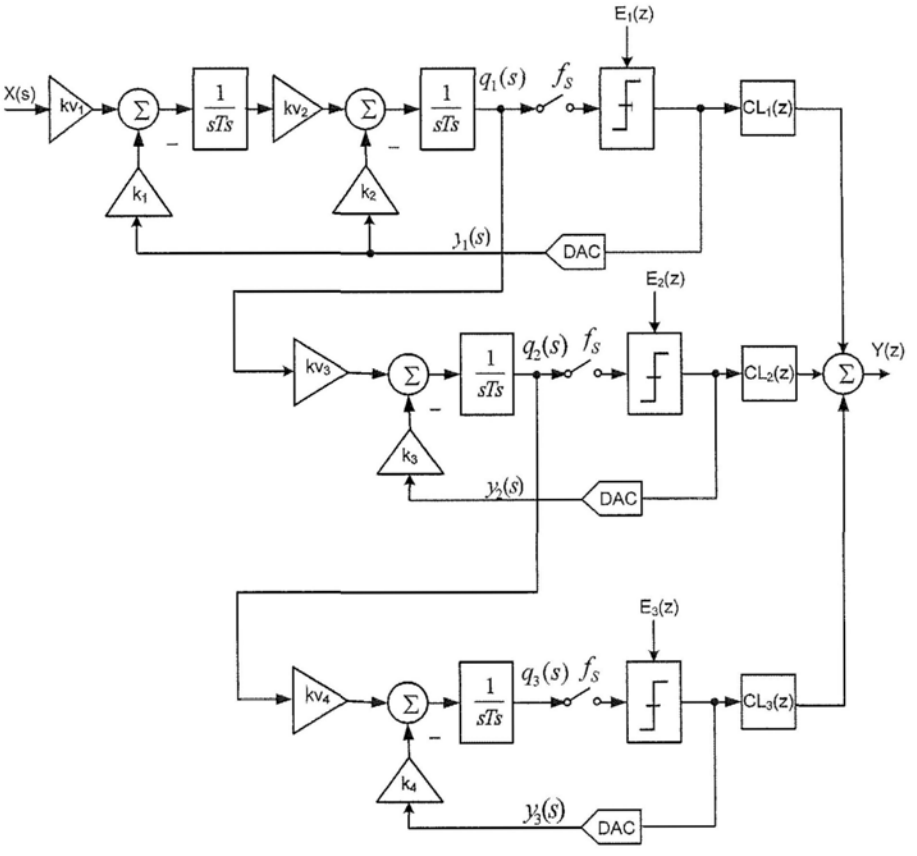


Fig 5.1 Cascaded CT ΔΣ modulator architecture with direct synthesis method proposed in [67].

The cancellation logic $CL_k(z)$ is calculated by the following equation [67]:

$$CL_k(z) = \frac{-Z\{L^{-1}[H_D F_{km}]|_{nT_s}\}CL_m(z)}{1-Z\{L^{-1}[H_D F_{mm}]|_{nT_s}\}} \tag{5.1}$$

where Z is Z-transform, L^{-1} is inverse Laplace transform, H_D is DAC transfer function, F_{ij} is defined as [67]:

$$F_{ij} = \frac{q_j(s)}{y_i(s)} \tag{5.2}$$

$CL_m(z)$ is the cancellation logic function of last stage, and is always chosen to be simplest to realize the high-pass filtered quantization noise of the last stage. The synthesis digital cancellation logic derivation is complicated as it is indicated from the expression of $CL_k(z)$.

5.2.2 Impulse-Invariant Loop Filter Equivalent Method

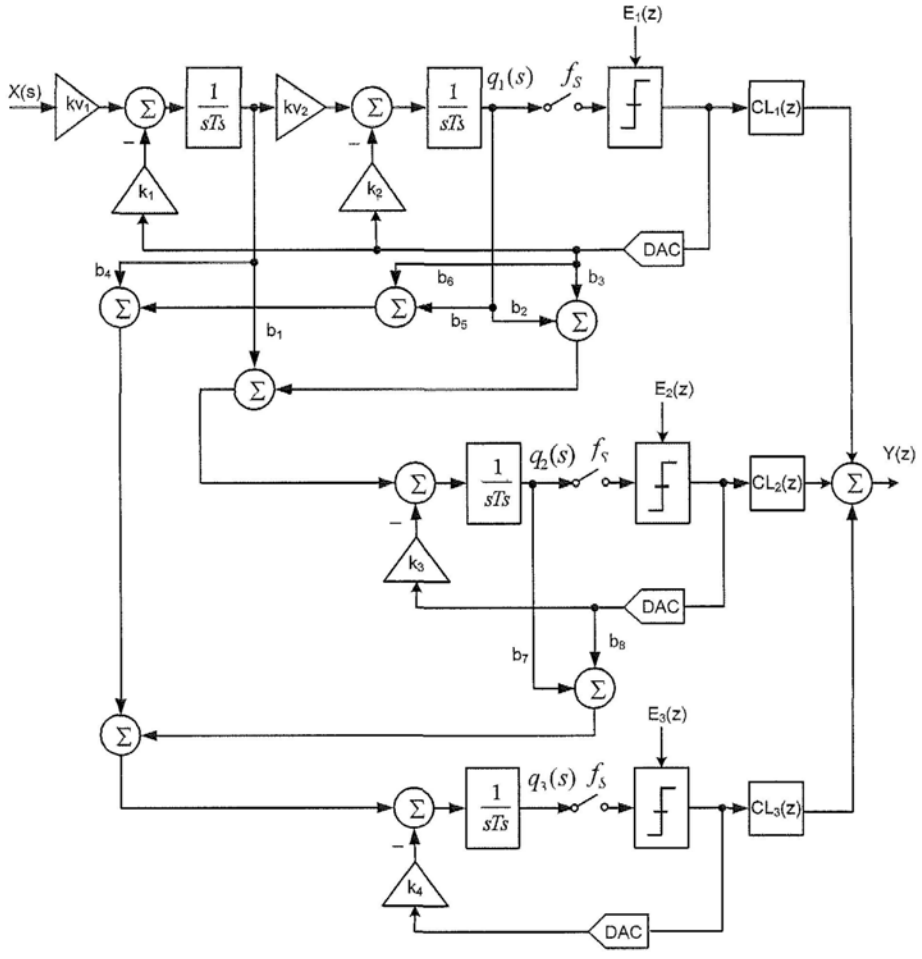


Fig 5.2 Cascaded CT ΔΣ modulator architecture from an equivalent DT ΔΣ modulator proposed in [68].

Fig 5.2 shows the scheme of cascaded CT ΔΣ modulator reported in [68], the digital cancellation logic is the same as its DT counterparts. However, it needs plenty of additional hardware to realize the forward scaling coefficients between stages.

Fig 5.3 shows the scheme of cascaded CT ΔΣ modulator reported in [71], the digital cancellation logic is the same as its DT counterparts. It uses sampling switch to sample signal and to generate error signal as the input of next stage just as its DT counterpart does. Although it can eliminate additional feed-forward path, the circuit implementation involves switch-capacitor branch between stages. It's not suitable for ULV CT ΔΣ modulator design.

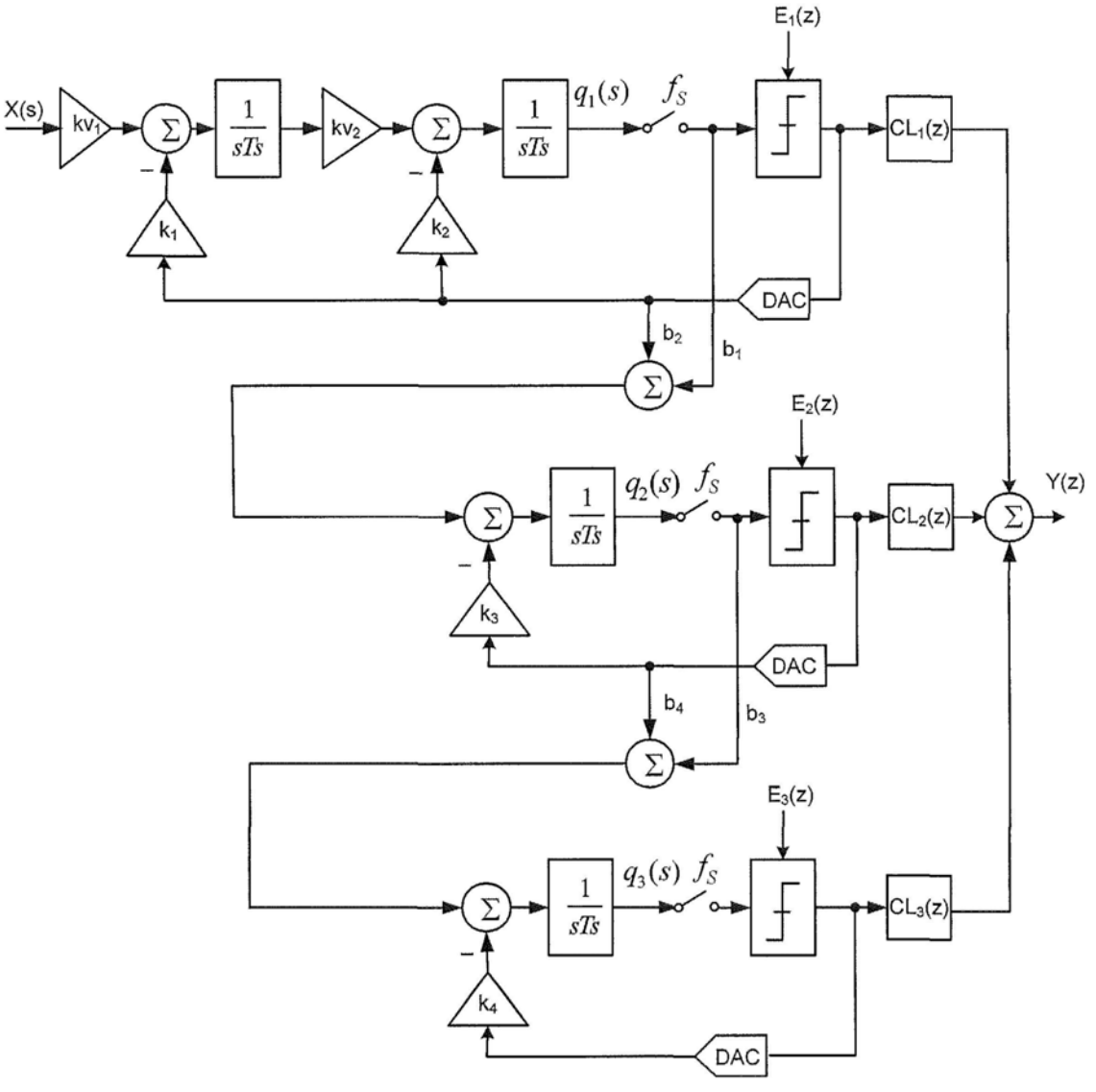


Fig 5.3 Cascaded CT ΔΣ modulator architecture proposed in [71].

5.3 Proposed Synthesis Method

This section presents a new synthesis method [72] of cascaded CT ΔΣ modulator. It employs one forward signal path like [67], but the digital cancellation logics derivation for modulators is based on discrete-time domain analysis.

In the proposed synthesis method, the coefficients for each stage of the cascaded modulator are obtained by impulse-invariant DT to CT transformation. The synthesis procedure for quantization noise cancellation logics starts with the calculation of noise transfer function (NTF) and signal transfer function (STF) of each stage. We take a 2-1 cascaded CT ΔΣ modulator as a synthesis example below, which can be extended to higher orders easily.

5.3.1 NTF and STF

Fig 5.4 shows the model of the 2-1 cascade CT ΔΣ modulator. Each stage is synthesized by DT to CT conversion, which is expressed as:

$$Z^{-1}\{H(z)\} = L^{-1}\{R_{D(s)}H(s)\}|_{t=nT_s} \tag{5.3}$$

where $H(z)$ is the DT loop filter transfer function, $H(s)$ is the CT loop filter transfer function, and $R_D(s)$ is the Laplace transform of the impulse response of the feedback DAC. The coefficients k_{v1}, k_{v2}, k_{v3} are set to 1 initially before dynamic range and input range scaling, and k_1, k_2, k_3 are calculated from $H(s)$.

The first stage here is a 2nd order one with a desired DT equivalent NTF of $(1-z^{-1})^2$. The output $Y_1(z)$ can be calculated as:

$$Y_1(z) = X(z)Z\{L^{-1}(\frac{1}{s^2})|_{t=nT_s}\} + E_1(z) + Y_1(z)Z\{L^{-1}\{-R_D(s)H_1(s)\}|_{t=nT_s}\} \tag{5.4}$$

Setting the quantization noise to zero, we obtain the $STF_1(z)$ as:

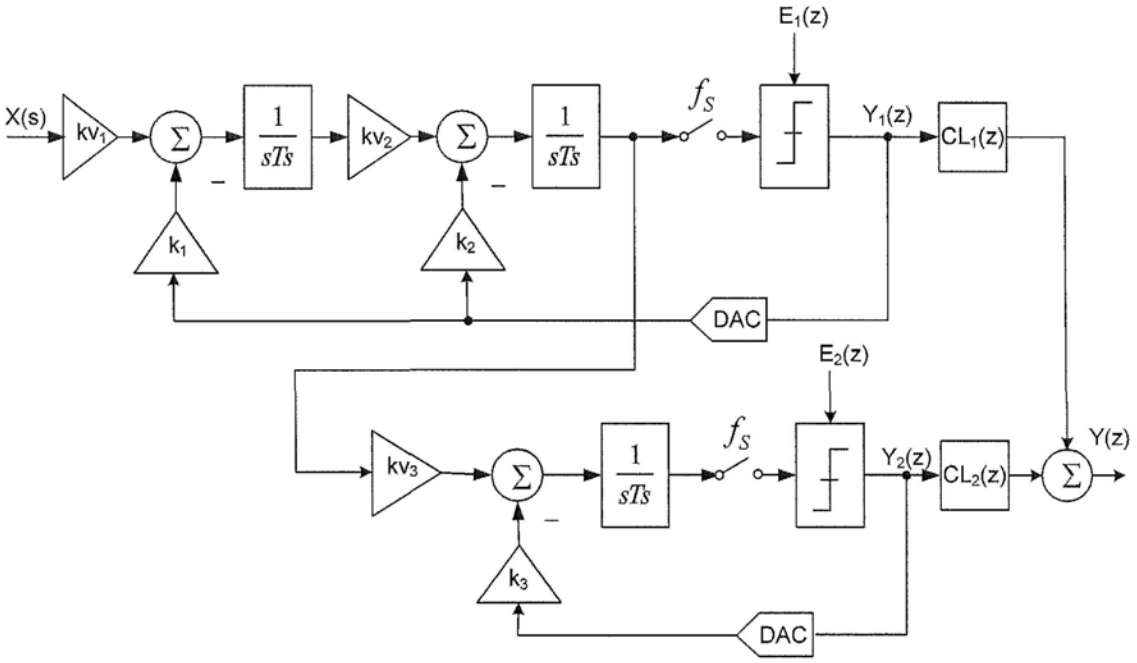


Fig 5.4 Model of a 2-1 cascaded CT ΔΣ modulator.

$$NTF_1(z) = \frac{1}{1 + Z\{L^{-1}\{R_D(s)H_1(s)\}|_{t=nT_s}\}} = (1 - z^{-1})^2 \tag{5.5}$$

Setting the quantization noise to zero, we obtain the $STF_1(z)$ as:

$$STF_1(z) = \frac{Z\{L^{-1}(\frac{1}{s^2})|_{t=nT_s}\}}{1 + Z\{L^{-1}\{R_D(s)H_1(s)\}|_{t=nT_s}\}} = (1 - z^{-1})^2 \cdot \frac{z^{-1}}{(1 - z^{-1})^2} = z^{-1} \tag{5.6}$$

The forward signal between stages can be calculated as:

$$X(z)Z\{L^{-1}(\frac{1}{s^2})|_{t=nT_s}\} + Y_1(z)Z\{L^{-1}\{-R_D(s)H_1(s)\}|_{t=nT_s}\} = Y_1(z) - E_1(z) \tag{5.7}$$

The second stage is a 1st order one with a DT equivalent NTF of $(1\text{-}z^{-1})$. The output $Y_2(z)$ can be calculated as:

$$Y_2(z) = [Y_1(z) - E_1(z)]Z\{L^{-1}(\frac{1}{s})|_{t=nTs}\} + E_2(z) + Y_2(z)Z\{L^{-1}\{-R_D(s)H_2(s)\}|_{t=nT_s}\} \tag{5.8}$$

Setting the input of second stage to zero, we get the $NTF_2(z)$:

$$NTF_2(z) = \frac{1}{1 + Z\{L^{-1}\{R_D(s)H_2(s)\}|_{t=nT_s}\}} = (1 - z^{-1}) \tag{5.9}$$

Setting the quantization noise to zero, we get the $STF_2(z)$:

$$STF_2(z) = \frac{Z\{L^{-1}(\frac{1}{s})|_{t=nT_s}\}}{1 + Z\{L^{-1}\{R_D(s)H_2(s)\}|_{t=nT_s}\}} = (1 - z^{-1}) \cdot \frac{1}{(1 - z^{-1})} = 1 \tag{5.10}$$

5.3.2 Digital Cancellation of Low-Order Quantization Noise

Since the NTF and STF have been formulated, the output $Y_1(z)$, $Y_2(z)$ and final output $Y(z)$ can be expressed as:

$$Y_1(z) = STF_1(z)X(z) + NTF_1(z)E_1(z) \tag{5.11}$$

$$Y_2(z) = STF_2(z)[Y_1(z) - E_1(z)] + NTF_2(z)E_2(z) \tag{5.12}$$

$$Y(z) = Y_1(z)CL_1(z) + Y_2(z)CL_2(z) \tag{5.13}$$

For the cascaded ΔΣ modulator, the output should contain only the high-pass filtered quantization noise of the last stage while cancel the quantization noise of all the other stages. Thus, the cancellation logics can be formulated. Substituting Eq. (5.5), (5.6), (5.9)-(5.12), into Eq. (5.13), $Y(z)$ becomes:

$$\begin{aligned} Y(z) = &[z^{-1}CL_1(z) + z^{-1}CL_2(z)]X + [(1 - z^{-1})CL_2(z)]E_2(z) \\ &+ \{(1 - z^{-1})^2 CL_1(z) + [(1 - z^{-1})^2 - 1]CL_2(z)\}E_1(z) \end{aligned} \tag{5.14}$$

For this case, $E_2(z)$ should be a 3rd high-pass function, so $CL_2(z)$ is chosen to be:

$$CL_2(z) = (1 - z^{-1})^2 \tag{5.15}$$

$E_1(z)$ should be cancelled, so $CL_1(z)$ is :

$$CL_1(z) = -z^{-2} + 2z^{-1} \tag{5.16}$$

Finally the overall output $Y(z)$ is:

$$Y(z)=z^{-1}X+(1-z^{-1})^3E_2(z) \tag{5.17}$$

The digital cancellation logics derivation is based on DT domain analysis, which is as easy as the synthesis method for cascaded DT ΔΣ modulators.

5.3.3 Digital Correction of RC Product Variation

The *RC* product variation is the main analog error contributing factor, overriding finite GBW of amplifier and the mismatch for *R* and *C* [73]. Digital correction presented in this manuscript is to suppress the negative effect of *RC* product variation on SQNR.

Let us still take the 2-1 cascaded CT ΔΣ modulator as the example. *RC* product variation alters the NTF and STF of the 1st and 2nd stages, thus digital cancellation logics should be modified to make the SQNR loss small.

Suppose the normalized *RC* product is *g*, so the *RC* product variation equals to (*g*-1)*100%. In Fig 5.4, all the coefficients can be written in terms of *g*:

$$k_{v1}'=1/g,\ k_{v2}'=1/g,\ k_{v3}'=1/g,\ k_1'=k_1/g,\ k_2'=k_2/g,\ k_3'=k_3/g$$

and the CT loop filter transfer functions of 1st and 2nd stages can be rewritten as:

$$H_1(s)=\frac{k_2}{g\cdot s}+\frac{k_1}{g^2\cdot s^2} \tag{5.18}$$

$$H_2(s)=\frac{k_3}{g\cdot s} \tag{5.19}$$

New $H_1(z)$, $H_2(z)$ can be calculated by CT to DT conversion, and new NTF and STF of stage1, stage2 can be derived by Eq. (5.5), (5.6), (5.9) and (5.10). Thus the new digital cancellation logic $CL_1(z)$, $CL_2(z)$ can be derived from the Eq. (5.14). An example to verify the digital correction method is given later in this Chapter.

5.3.4 M-Stage Cascaded CT ΔΣ Modulator

For m-stage cascaded CT ΔΣ modulator, the synthesis procedure can be summarized as followings:

Firstly, choose m-stage cascaded DT loop filter, calculate coefficients of each stage by DT to CT conversion.

Secondly, calculate the STF, NTF of each stage as described in Section **Error! Reference source not found.**. For cascaded structure, each stage is either 1st order or 2nd order loop filter, and the Eq. (5.5), (5.6), (5.9) and (5.10) can be applied to each stage in most cases.

Thirdly, get the output expression of each stage as well as the final output. Make the quantization noise of last stage mth-order noise shaped, thus get $CL_m(z)$, and obtain $CL_1(z)$ to $CL_{m-1}(z)$ by cancelling the quantization noise of all the other stages except the final stage.

Fourthly, calculate the corrected digital cancellation logics in terms of normalized *RC* product "*g*" as described in Section 5.3.3.

5.4 Synthesis Example of 0.5V 2-1 Cascaded CT ΔΣ modulator

For CT ΔΣ modulator, high sensitivity to clock jitter is the fatal disadvantage as discussed in Chapter 3. In this synthesis example, a SCR feedback DAC is adopted considering the difficulty in circuit realization, power consumption and the effectiveness in clock jitter noise reduction.

5.4.1 System Architecture

A 2-1 cascaded CT ΔΣ modulator with SCR feedback synthesized by the proposed method. The signal bandwidth is 25-*k*Hz, sampling frequency is 6.4-*M*Hz.

The loop transfer functions of DT 2-1 cascaded modulator are chosen as:

$$Y_1(z) = z^{-2}X(z) + (1-z^{-1})^2 E_1(z) \tag{5.20}$$

$$Y_2(z) = z^{-1}E_1(z) + (1-z^{-1})E_2(z) \tag{5.21}$$

The coefficients of CT ΔΣ modulator are obtained by an impulse-invariant transformation [42] of the DT modulator. The SCR DAC has a decayed pulse shaped waveform, the 70% pulse width and 20% delay of the DAC have been taken into account of the modulator design. The time constant for SCR feedback network is set to $5\%T_s$ to reduce the clock jitter noise to sufficiently lower than quantization noise. The calculated coefficients are:

$$k_{v1}=1,\ k_{v2}=1,\ k_{v3}=1,\ k_1=20,\ k_2=25,\ k_3=20$$

And the digital cancellation logics obtained by this proposed method are:

$$CL_1(z)=-z^{-2}+2z^{-1} \tag{5.22}$$

$$CL_2(z)=(1-z^{-1})^2 \tag{5.23}$$

Including the *RC* product variation, the corrected digital cancellation logics are:

$$CL_1(z) = -(\frac{1.25}{g^2} - \frac{0.25}{g^3})z^{-2} + (\frac{1.25}{g^2} + \frac{0.75}{g^3})z^{-1} \tag{5.24}$$

$$CL_2(z) = (1-z^{-1})^2 + (\frac{1}{g} - 1)(1-z^{-1})^2 z^{-1} \tag{5.25}$$

To make SQNR variation small over an *RC* variation range from -30% to 50%, *RC* product is increased by 20%. After dynamic range and input range scaling, the coefficients are:

$$k_{v1}=0.05,\ k_{v2}=0.42,\ k_{v3}=0.5,\ k_1=2.78,\ k_2=1.74,\ k_3=0.83$$

and the corresponding digital cancellation logics are:

$$CL_1(z) = -(\frac{1.25}{(1.2*g)^2} - \frac{0.25}{(1.2*g)^3})z^{-2} + (\frac{1.25}{(1.2*g)^2} + \frac{0.75}{(1.2*g)^3})z^{-1} \tag{5.26}$$

$$CL_2(z) = (1-z^{-1})^2 + (\frac{1}{1.2*g} - 1)(1-z^{-1})^2 z^{-1} \tag{5.27}$$

Fig 5.5 shows the final coefficients of the 2-1 cascaded CT ΔΣ modulator with SCR feedback.

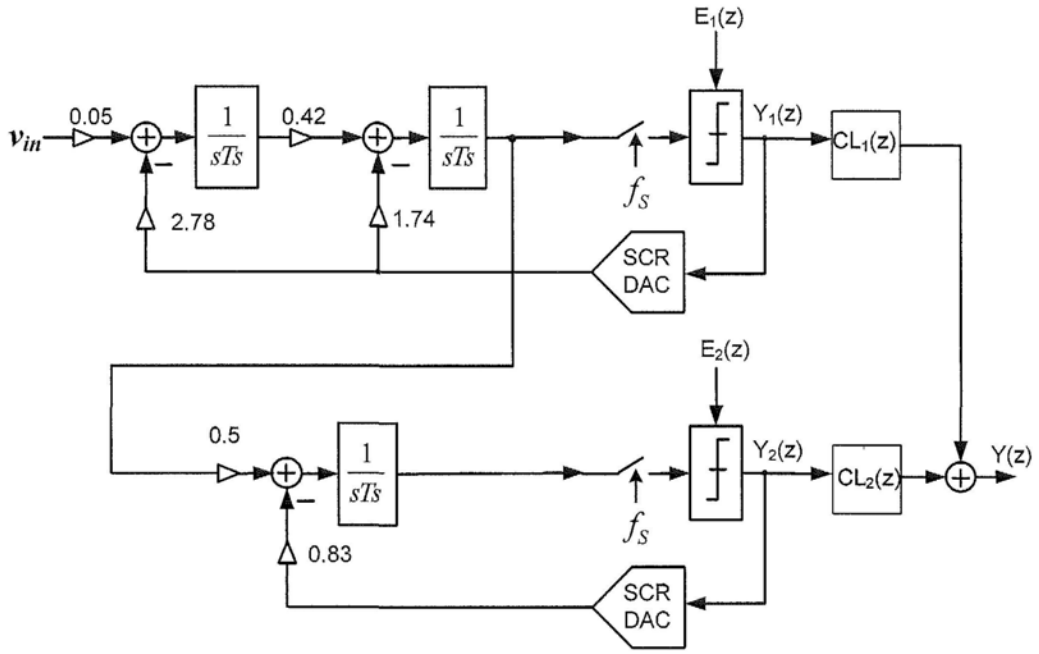


Fig 5.5 2-1 Cascaded CT ΔΣ modulator coefficients (f_s = 6.4MHz, T_s=1/f_s).

5.4.2 Behavioral Simulation

The Matlab model is shown in Fig 5.6. The power spectrum density (PSD) simulated with Matlab™ with V_{in} fixed at 0dB V_{FS} (V_{FS}=1$V_{pp,diff}$) is shown in Fig 5.7. The SQNR is 112.8dB with nominal RC product value. The Matlab simulation results for RC product variation from -30% to +50% under different delay values are shown in Fig 5.8. The Vin is fixed at 0dB V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$). SQNR is better than 101dB for a large range of RC value and a ±5%T_s variation in the DAC delay time. Fig 5.9 shows the Matlab simulation results of SQNR versus input amplitude for both the 2-1 cascaded DT ΔΣ modulator and the proposed CT ΔΣ modulator. The results verify that the proposed CT ΔΣ modulator behaves nearly the same as DT ΔΣ modulator over the whole input range. Fig 5.10 shows the Matlab simulated output spectrum for DT and CT ΔΣ modulator with a 0dB V_{FS} sinusoidal input at 4.3kHz.

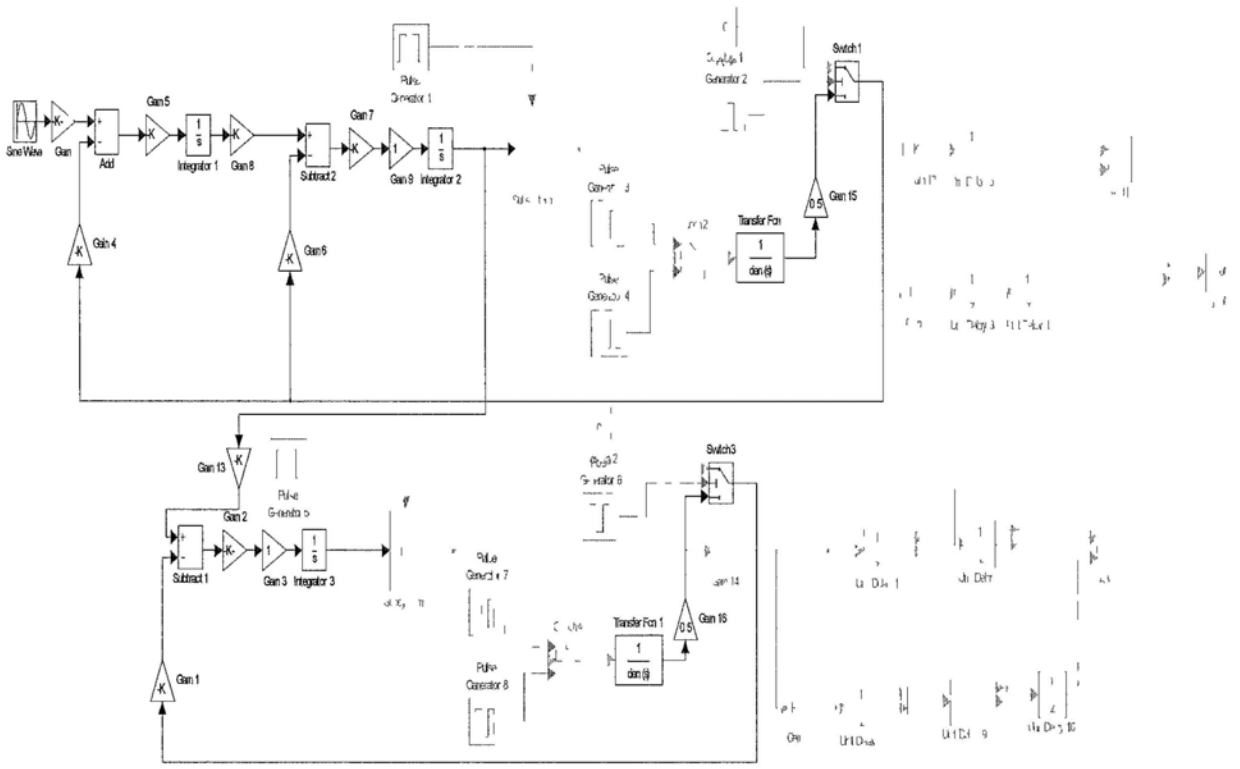


Fig 5.6 Matlab model for 2-1 casacded CT ΔΣ modulator with SCR feedback.

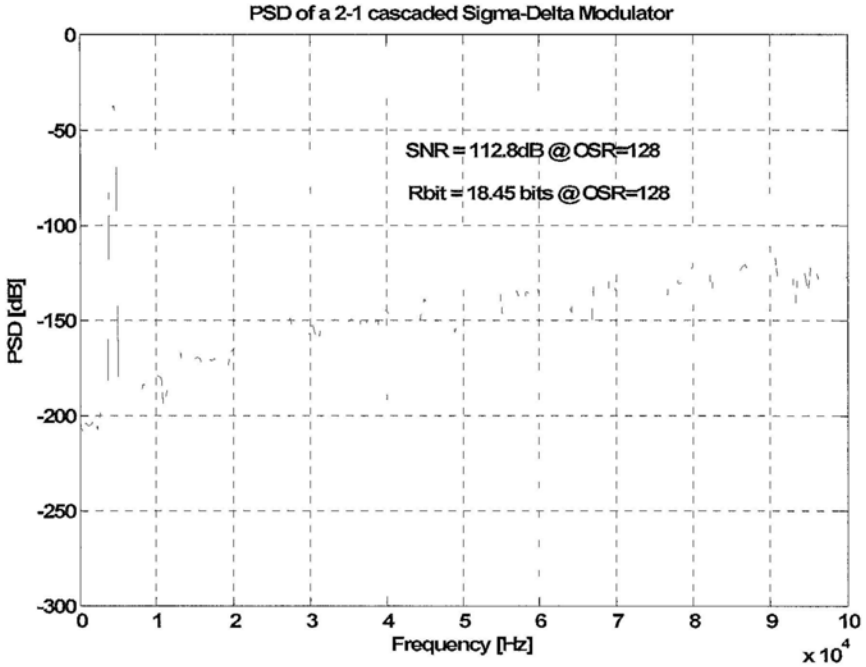


Fig 5.7 Matlab simulation result: Power Spectrum Density with V_m at $0dB$ V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

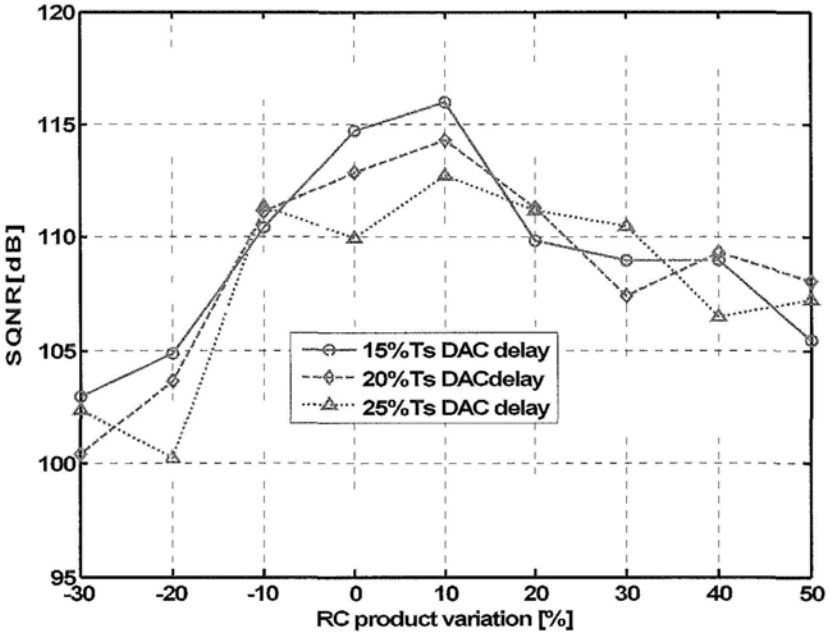


Fig 5.8 Matlab simulation results: SQNR versus *RC* product variation for different delay with *Vin*=0*dB* V_{FS} (V_{FS}=1$V_{p\text{-}p,diff}$).

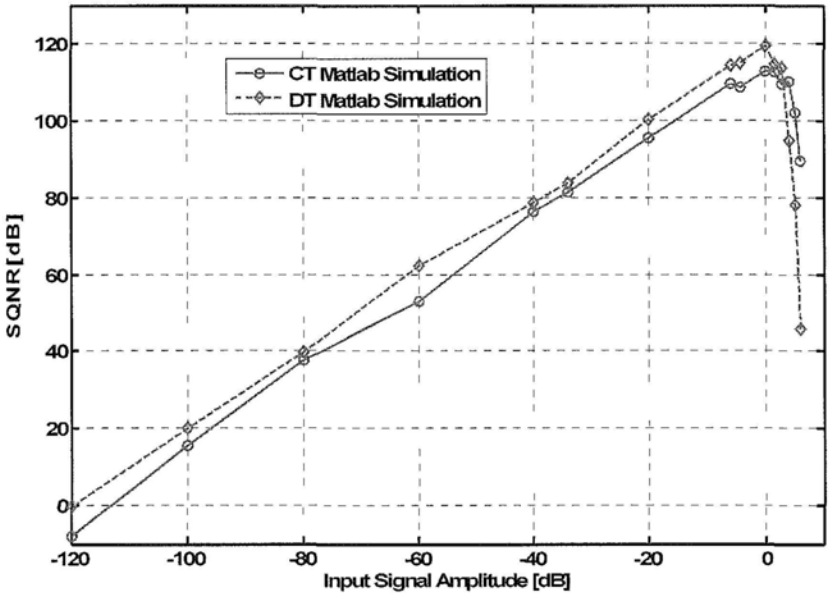


Fig 5.9 SQNR versus input amplitude of a 2-1 cascaded DT ΔΣ modulator and the proposed 2-1 cascaded CT ΔΣ modulator.

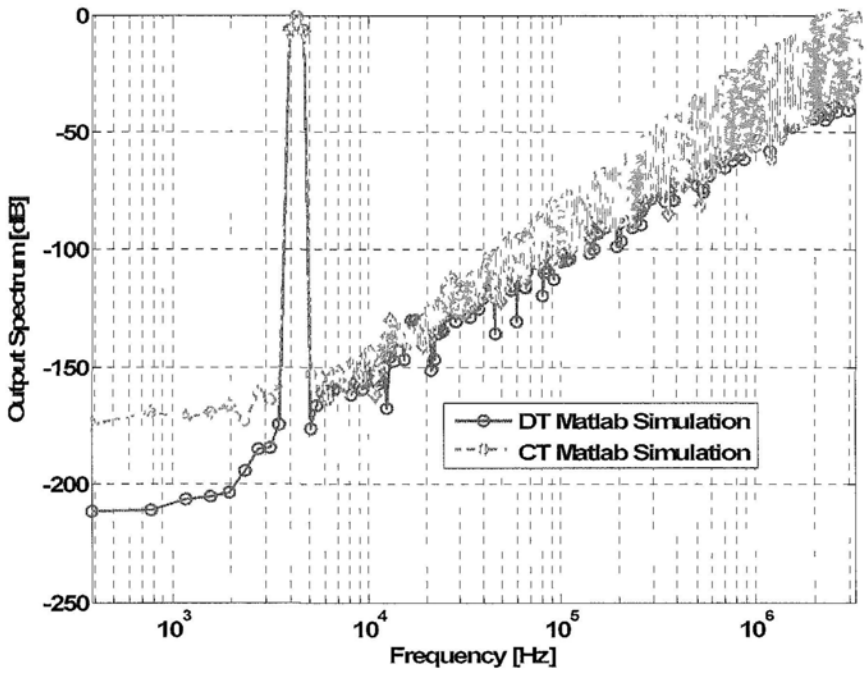


Fig 5.10 Output spectrum: Matlab simulation of the 2-1 cascaded DT ΔΣ modulator and the proposed 2-1 cascaded CT ΔΣ modulator.

5.5 Circuit Implementation

5.5.1 Architecture of 0.5V 2-1 Cascaded CT ΔΣ modulator

Fig 5.11 presents the fully differential 2-1 cascaded CT ΔΣ modulator circuit implementation for a 0.5-V supply synthesized by the proposed method. The resistors and capacitors values are designed by the final coefficients in Fig 5.5. The input signal can be up to $1V_{pp,diff}$.

The input signal coefficient is two times of 3rd order CIFB CT ΔΣ modulator discussed in Chapter 3, which results in reduction of thermal noise (see section 5.5.2).

The modulator is designed in a 130nm CMOS technology. The common-mode (CM) voltage ($V_{in,cm}$) at the amplifiers' inputs is set at $0.2V_{DD}$ by a pair of resistors (R_{dc1p} and R_{dc1n} for the 1st stage) connected to a clean V_{SS}. The DC voltage V_B for the switches controlled by Φ_2 is

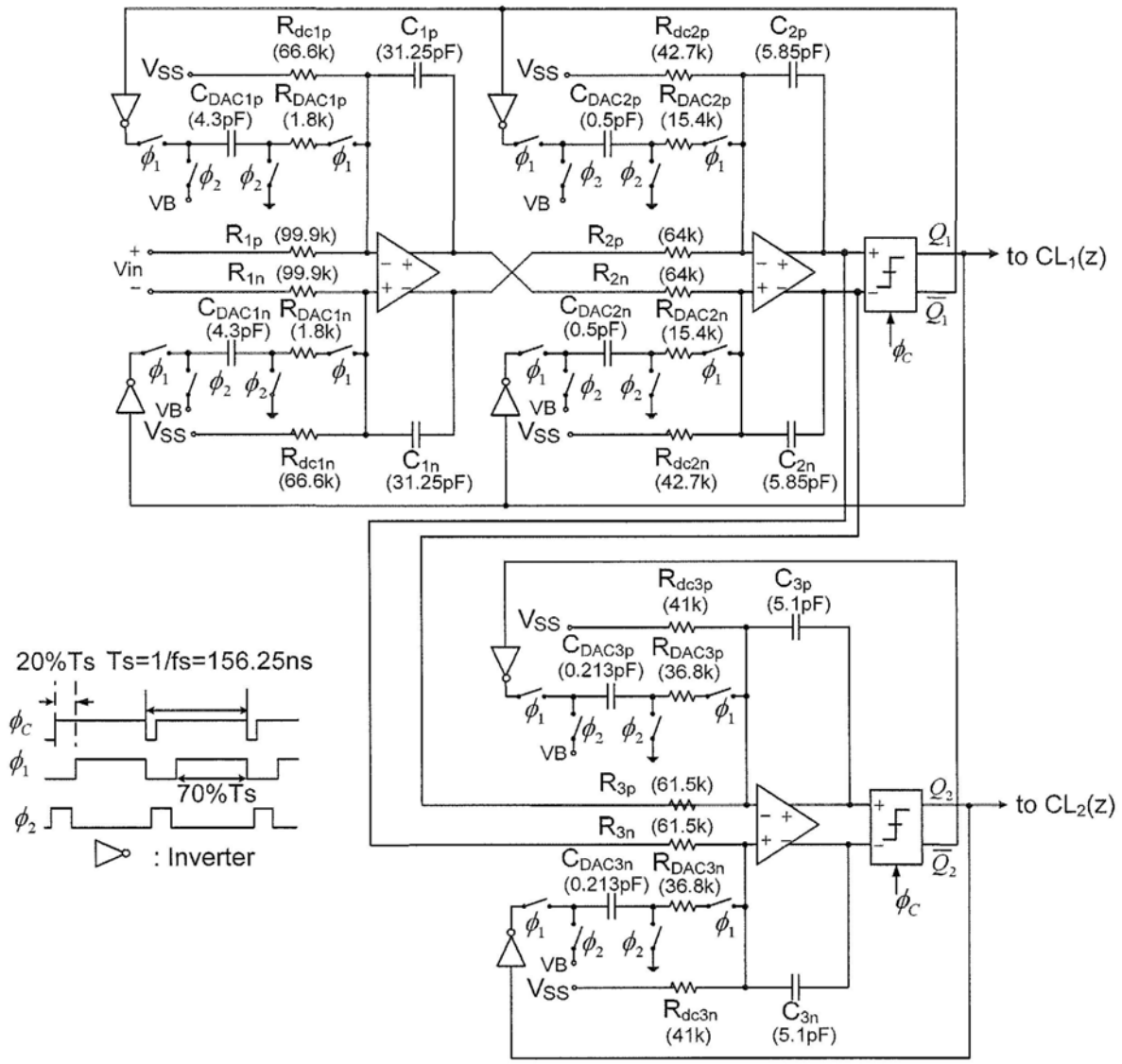


Fig 5.11 Architecture and clock waveforms of the proposed 2-1 cascaded CT ΔΣ modulator with SCR feedback.

set at $0.3V_{DD}$. The output CM voltage of the amplifiers is chosen to be $0.5V_{DD}$ to maximize the output swing. Since the $|V_{GS}|$ for the switches in the SCR feedback is $0.2V_{DD}$, the amplifier can be designed with large g_m to meet the UGB requirement set by SCR feedback DAC.

5.5.2 Noise

5.5.2.1 Thermal Noise

The input referred noise can be calculated from the Eq. (3.6), with the parameters given in Fig 5.11:

$$R_1=99.9k\Omega,\ R_{dc}=66.6k\Omega,\ C_{DAC}=4.3p\text{F},\ f_s=6.4M\text{Hz}$$

and for $1V_{pp}$ maximum differential signal amplitude, the thermal-noise-limited SNR of the modulator is $84.6dB$.

The thermal noise is reduced by $0.6dB$ than the one in Chapter 3. Although the thermal noise can be further reduced by decrease the value of C_{DAC}, which results in the decrease of SCR time constant τ, and the increase of UGB requirement of amplifier.

5.5.2.2 Clock Jitter Noise

The jitter noise of the first stage dominates the total jitter noise in cascaded ΔΣ modulator as the jitter noise of the other stages can be noise shaped by the loop filter of first stage. The jitter induced noise of the first stage can be calculated according to Eq. (3.17) and (3.18), with the parameters given in Fig 5.5:

$$k_1 = 2.78,\ k_2 = 1.74,\ k_{sig} = 0.05,\ OSR = 128,\ \tau = 0.05T_S$$

For $\sigma_t = 0.01T_s$, the jitter-limited SNR of the modulator is $144dB$, beyond the limit set by the quantization noise (see Fig 5.8).

5.6 Circuit Design

5.6.1 Fully Differential Gate-Body-Input Class AB Amplifier

As discussed in Chapter 3, the UGB and SR requirements of amplifier are:

$$UGB \geq 3\times f_s = 19.2MHz \tag{5.28}$$

$$SR_{max} \geq 6.4\times10^6 \times (0.05\times0.5 + 2.78\times0.5) = 9V/\mu s \tag{5.29}$$

The SR requirement is higher than that in Chapter 3, the amplifier proposed here is a fully differential gate-body-input class-AB topology which can alleviate power consumption problem due to the increased SR requirement.

5.6.1.1 Schematic of Amplifier

Fig 5.12 shows the schematic details of the amplifier. Table 5.1 gives the components values. This amplifier features rail to rail output swing and class-AB operation. The amplifier consists of two stages and a CMFB stage. The input CM voltage is set at $0.2V_{DD}$ by external circuits. M_1, M_2 are gate-body-input transistors to enhance the transconductance as well as to reduce threshold voltage of PMOS. R_1, R_2 and M_3, M_4 form a local CMFB which contributes to the CM rejection. M_8, M_5 and M_6 are current mirrors of M_0, and the current ratio of M_8 to M_6 is 4:1. The gain of first stage can be enhanced by this current shunt architecture as the DC current goes through M_3 and M_4 is reduced. The second stage is class-AB output stage formed by M_{10}-M_{13}. M_{10}, M_{11} are current mirrors of M_4, and the current ratio of M_{11} to M_{10} to M_4 is 3:0.5:1. The SR requirement is at least $9V/\mu s$ from Eq. (5.29), if we use the ULV two-stage amplifier discussed in Chapter 3, the second stage needs more DC bias current to meet this SR requirement.

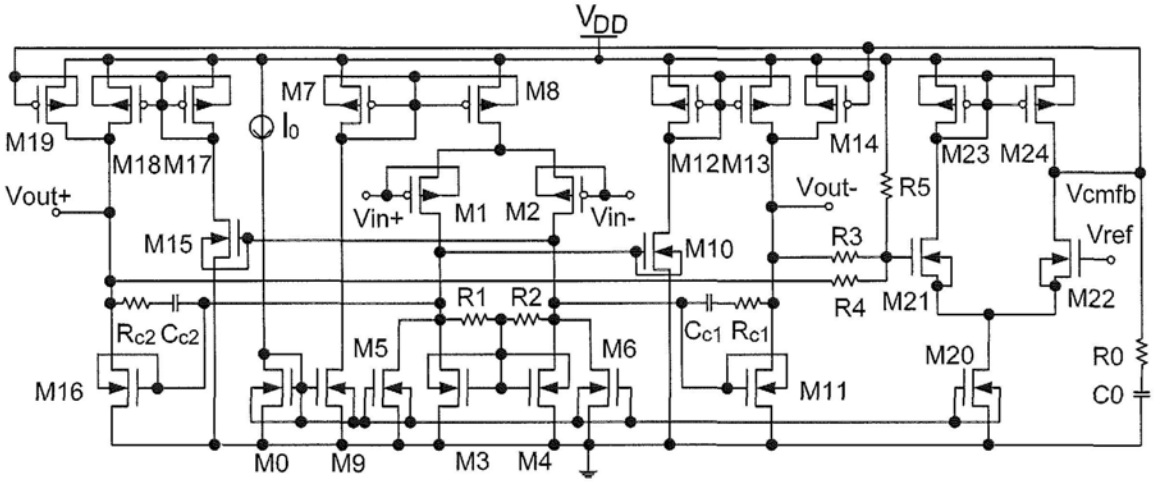


Fig 5.12 Proposed ULV fully differential gate-body-input class-AB amplifier.

Table 5.1 Components values of first amplifier

R_0=200K	M_7=30/0.5
R_1,R_2,R_3,R_4=100K	M_8=240/0.5
R_5=33.3K	M_{10},M_{15}=20/1
R_{C1},R_{C2}=2K	M_{11},M_{16}=120/1
C_0=1.6pF	M_{12},M_{17}=7.5/0.36
C_{C1},C_{C2}=9.1pF	M_{13},M_{18}=37.5/0.36
M_0,M_9=20/2	M_{14},M_{19}=30/0.36
M_1,M_2=160/1	M_{20}=20/2
M_3,M_4=40/1	M_{21},M_{22}=5/0.5
M_5,M_6=40/2	M_{23},M_{24}=15/0.36

The class-AB output stage can meet this requirement with less DC bias current. Moreover the current mirror of M_{12} and M_{13} provides extra DC gain as the ratio of M_{13} to M_{12} is 5:1.

The CMFB stage consists of R_3-R_5, M_{20}-M_{24}, the voltage of *Vref* is set at $0.8V_{DD}$ to enhance the transconductance, and M_{21}-M_{22} are triple-well NMOS transistors with body connected to its P-well to reduce its threshold voltage. R_3-R_5 is used as output CM voltage level shift to shift $V_{CM,out}$ from $0.5V_{DD}$ to $0.8V_{DD}$. The CMFB signal—V_{cmfb} controls M_{14} and M_{19} to adjust the output CM voltage to $V_{DD}/2$. R_0 and C_0 are used to compensate the CMFB loop in amplifier.

Fig 5.13 shows the small-signal equivalent circuit of first amplifier. The differential DC gain is:

$$\begin{aligned} A_{diff} = &\{(g_{m13}+g_{mb13})(g_{m10}+g_{mb10})(g_{m1}+g_{mb1})[(g_{m1}+g_{mb1})r_{ds1}r_{ds8} /\!/ r_{ds3} /\!/ R_1](r_{ds10} /\!/ 1/g_{m12}) \\ &+(g_{m2}+g_{mb2})(g_{m11}+g_{mb11})[(g_{m2}+g_{mb2})r_{ds2}r_{ds8} /\!/ r_{ds4} /\!/ R_2]\}(r_{ds13} /\!/ r_{ds14} /\!/ r_{ds11} /\!/ R_3) \end{aligned} \quad (5.30)$$

The small-signal model of CMFB loop is shown in Fig 5.14, the CMFB loop gain is:

$$\begin{aligned} A_{cmfb} = &2(g_{m14}+g_{mb14})g_{m21}g_{m24}\frac{R_5}{R_3 /\!/ R_4 + R_5}(r_{ds14} /\!/ r_{ds19})(g_{m22}r_{ds22}r_{ds20} /\!/ r_{ds24}) \\ &\times[g_{m21}r_{ds21}r_{ds20} /\!/ 1/(g_{m23}+g_{mb23})] \end{aligned} \quad (5.31)$$

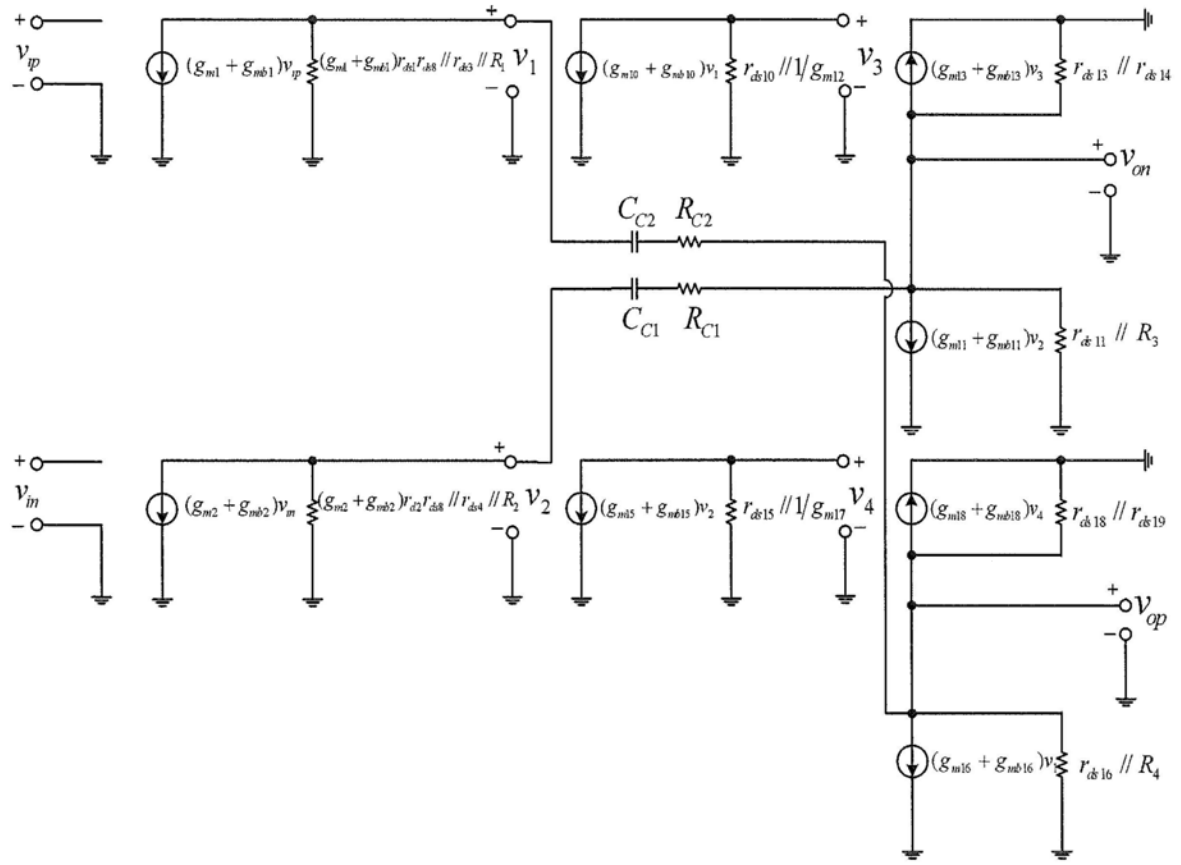


Fig 5.13 Small-signal equivalent circuit of first amplifier.

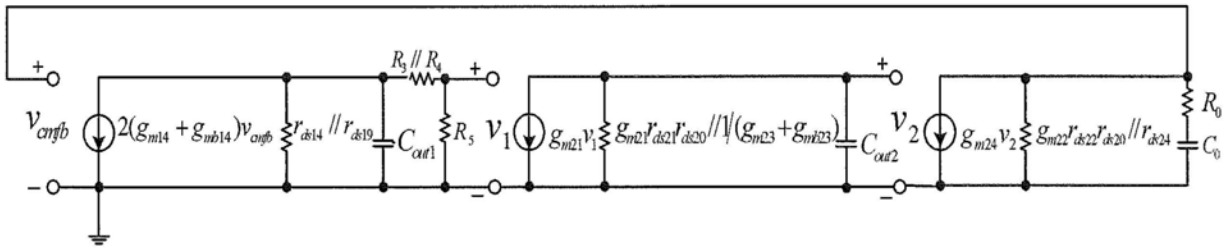


Fig 5.14 Small-signal model of CMFB loop.

Simulation Results show that the DC CMFB loop discussed in Chapter 3 consuming more power at high temperature and high supply voltage as the error amplifier is inverter architecture with no DC bias current. The CMFB loop adopted here is a single stage amplifier with constant DC bias current, and the power consumption can be consistent through PVT corner.

5.6.1.2 Simulation Results

The simulated performance of the amplifiers is shown in Table 5.2. The amplifiers for the three ΔΣ modulator stages are scaled as 1:0.22:0.2.

Table 5.2 Simulation performance of the amplifiers.

Parameters	AMP-1	AMP-2	AMP-3
Supply(V)	0.5	0.5	0.5
Power Consumption(μW)	189	42	37.5
Open loop DC Gain (dB)	63	52	60
UGB/PM (MHz / degree)	30.6 / 74	31 / 71	31 /72
Input ref.noise @1KHz/1MHz (nV/sqHz)	26/ 5.9	50 / 13	51.5 /13.5
CMRR@DC (dB)	121	96	100
SR+/SR- (V/μs)	11.25 / 11.3	18.4 / 18.4	20/ 20
Load(pF// kΩ)	31.25 // 64	5.85 // 61.5	5.1

Fig 5.15 shows the simulated frequency responses of the first amplifier over PVT corners (0 °C to 85 °C, 0.45V to 0.55V, and slow, nominal and fast process corners). Simulations also show that the amplifiers meet requirements over PVT corners. The power consumption is reduced as it adopts class-AB architecture.

Fig 5.16 shows the simulated CMFB loop frequency responses of the first amplifier over PVT corners. The PM of the CMFB loop is at least 48° for PVT corners.

Fig 5.17 shows the schematic for simulation of amplifier SR. The loading of the amplifier is $64k\Omega//31.25p$F. Note that it is a rail-to-rail amplifier, the differential-ended output full swing is $1V_{pp}$, and the amplitude of the differential input pulse is 0.5V.

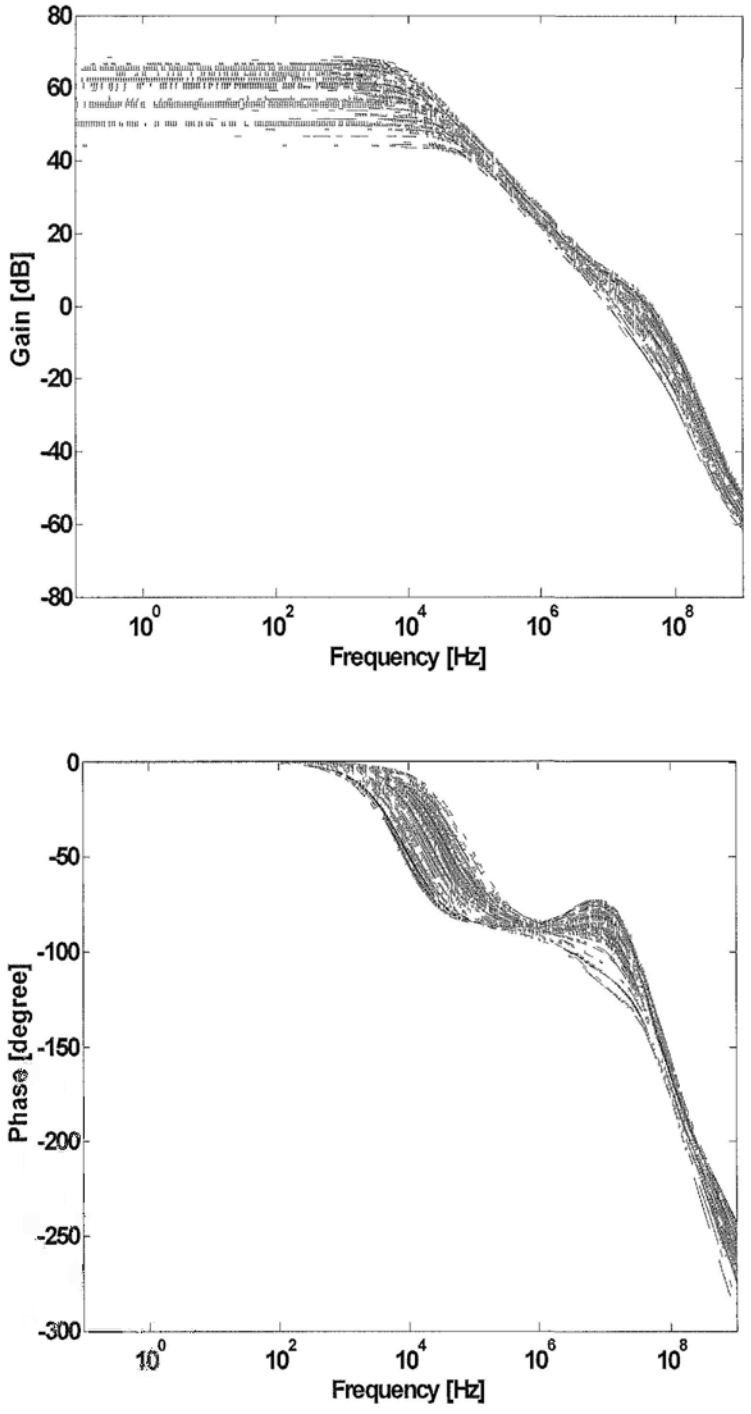


Fig 5.15 Frequency responses of the first amplifier over PVT corners.

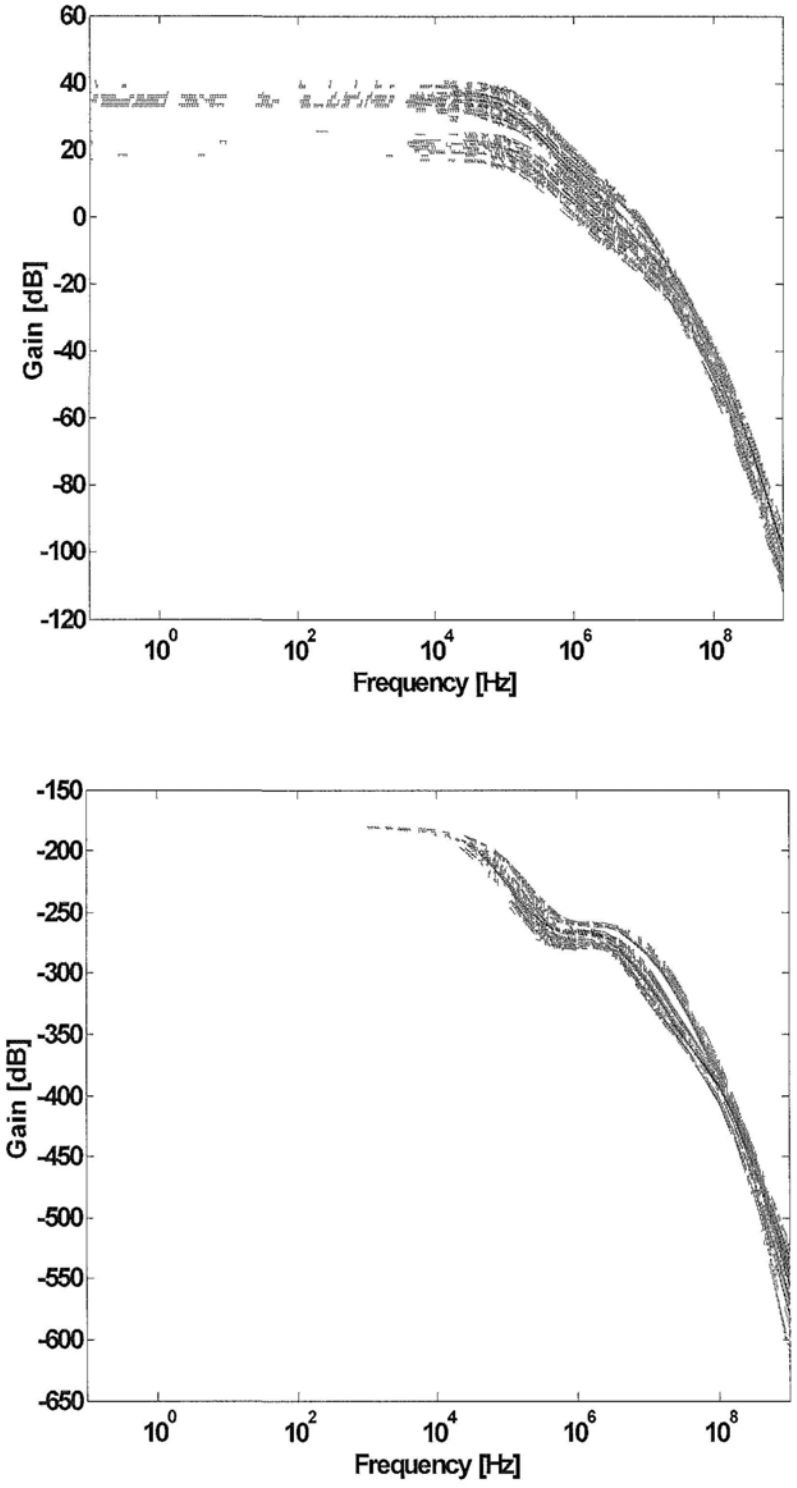


Fig 5.16 CMFB loop frequency responses of the first amplifier over PVT corners.

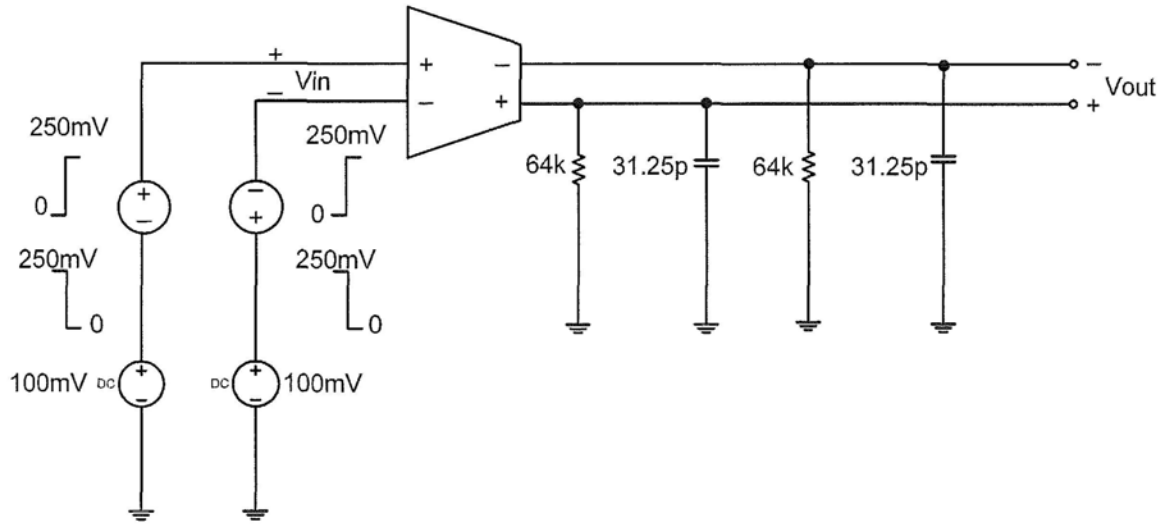
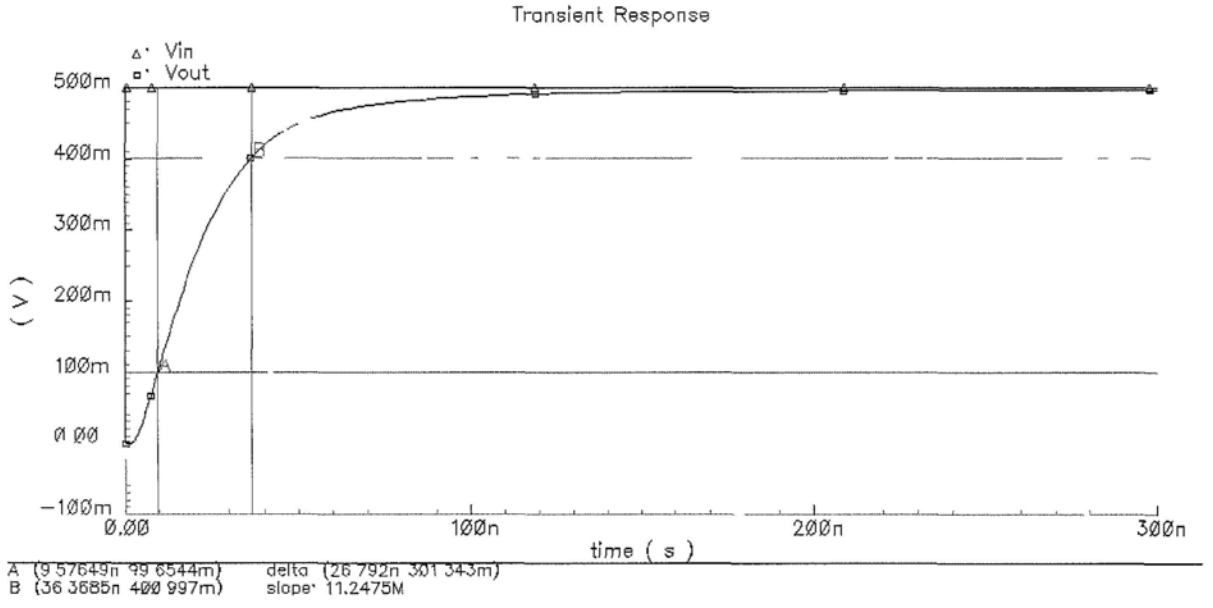
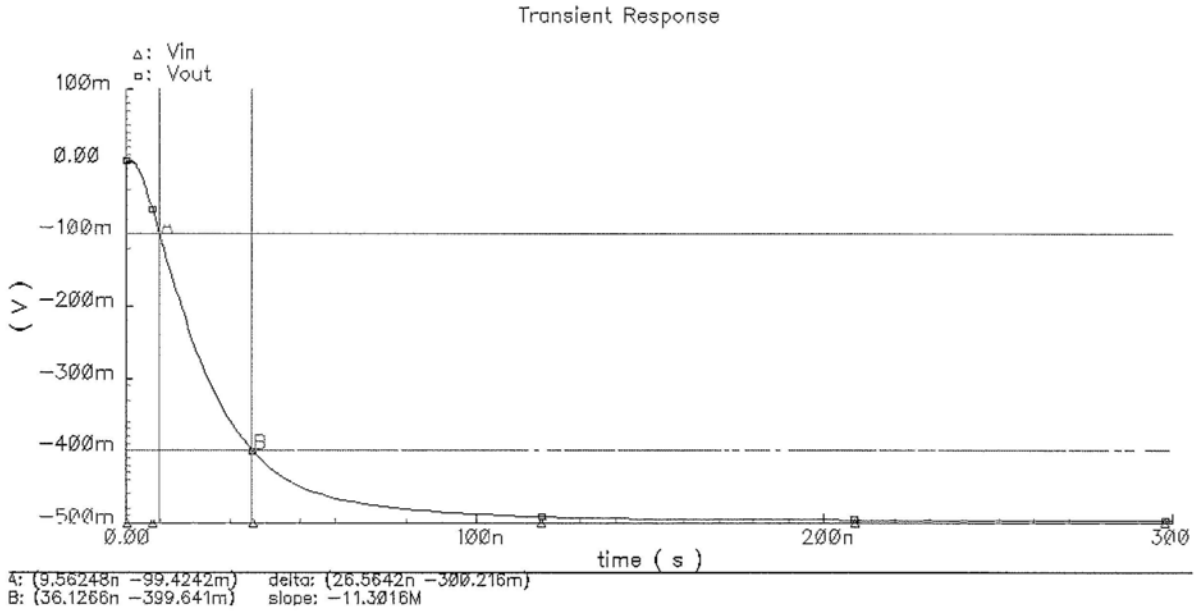


Fig 5.17 Schematic for simulation of amplifier SR.

Fig 5.18 (a) shows the simulated waveforms of differential input and output when differential input is positive 500mV pulse, while Fig 5.18 (b) shows the waveforms when differential input is negative 500mv pulse. Simulation results show that the positive and negative SR of amplifier is $11.25V/\mu s$ and $11.3V/\mu s$ separately. SR of amplifier meets the requirement set by Eq. (5.29).



(a)



(b)

Fig 5.18 Simulated differential output waveforms: (a) differential input of positive 500mV pulse; (b) differential input of negative 500mv pulse.

Fig 5.19 shows the schematic for simulation of amplifier output settling with square wave input. The amplitude of square wave is 500mV. Fig 5.20 shows the transient waveforms of differential output at typical, worst and best cases.

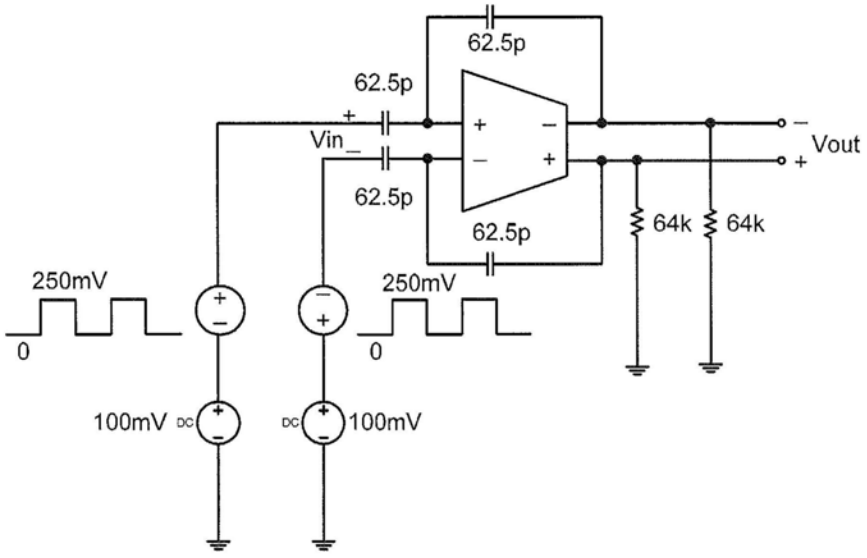


Fig 5.19 Schematic for simulation of amplifier output settling.

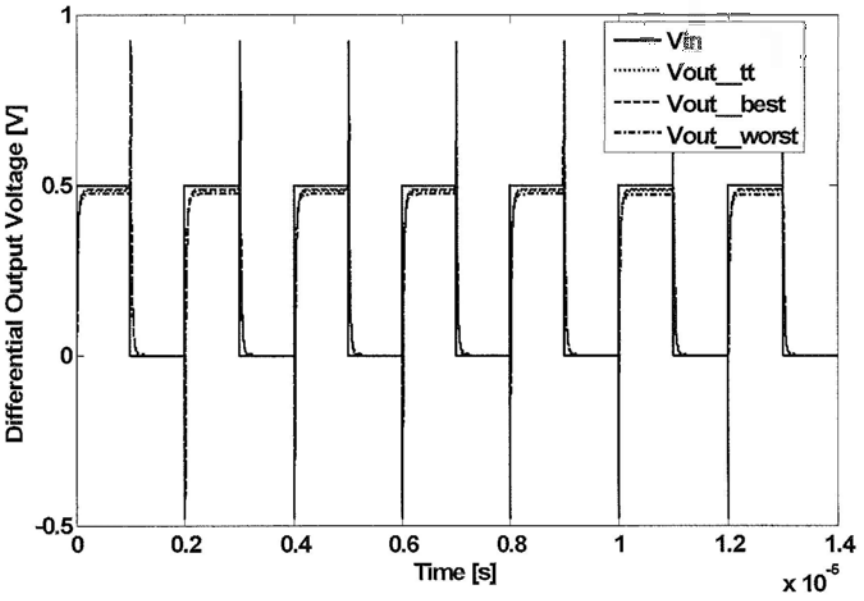


Fig 5.20 Simulated transient waveforms of differential output.

5.6.2 RC Product Variation Detection Circuit

As discussed in Chapter 2, for cascaded ΔΣ modulator, the mismatch between analog circuitry and digital circuitry can degrade the SQNR severely. *RC* product variation is the main factor resulting in noise leakage. Digital correction of *RC* product variation can eliminate the noise leakage problem once the practical *RC* product value is known. An on chip detection circuit of *RC* product is needed.

5.6.2.1 Schematic of RC Product Detection Circuit

Fig 5.21 shows the proposed *RC* product detection circuit. The ULV comparator proposed in Chapter 3 in used in this design. Table 5.3 gives the components values of this detection circuit. The error amplifiers formed by M_2 and M_3, M_4 and M_5 are biased (through the bodies of M_2-M_5) at high gain region around $V_{DD}/2$. They behave like differential amplifiers with one input fixed at $V_{DD}/2$. The biasing voltages V_{PB}, V_{NB} and V_{B1} are generated using circuits in Fig 4.11. V_A is fixed at $V_{DD}/2$ through the loop, the current goes through M_1 is:

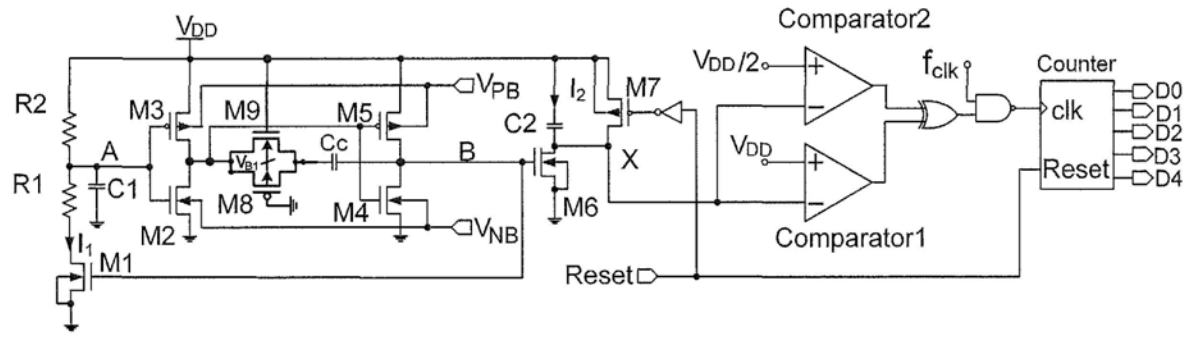


Fig 5.21 RC product variation detection circuit.

Table 5.3 Components values of RC product detection circuit

R_1=50K
R_2 =125K
C_1=1pF
C_2=25pF
C_C=11.7pF
M_1,M_6=5.5/2
M_2,M_4=4/0.36
M_3,M_5=16.4/0.36
M_7=50/0.12
M_8=12.3/0.36
M_9=3/0.36

$$I_1 = \frac{V_{DD}}{2 \times R_2} = \frac{0.5}{250k} = 2\mu A \tag{5.32}$$

and the current I_2 discharges capacitor C_2 is equal to I_1 by current mirror M_6 and M_1.

When Reset is "high", the circuit is reset, V_X is charged to V_{DD}, *and C2* is discharged quickly through M_7. When Reset is "low", the detection circuit begins to work. The V_X is discharged through M_6, and output of comparator 1 is "high", output of comparator 2 is "low", the clock signal of the counter is f_{clk}, the counter begins counting. When V_X is discharged to lower than $V_{DD}/2$, the output of comparator 2 is "high", and the clock signal of the counter is "0", the counter stops counting. The total discharged voltage through C_2 is $V_{DD}/2$ limited by these two comparators. The discharge time can be calculated by this equation:

$$t_{discharge} = \frac{C_2 \times (V_{DD} - V_{DD}/2)}{I_2} = \frac{C_2 \times V_{DD}/2}{V_{DD}/(2 \times R_2)} = R_2 C_2 \tag{5.33}$$

N is used to represent the value of counter, and the equivalent counting time is:

$$t_{counting} = \frac{N}{f_{clk}} \tag{5.34}$$

The counting time is to count the discharge time, that is:

$$R_2 C_2 = \frac{N}{f_{clk}} \tag{5.35}$$

and R_2C_2 is set to $20/f_s$ in design, here f_s is the sampling frequency of modulator. If there is RC product variation due to process variation, then the normalized RC product "g" can be expressed as:

$$g = \frac{R_2 C_2}{20/f_s} \tag{5.36}$$

Substitute Eq. (5.36) into Eq. (5.35), "g" can be calculated as:

$$g = \frac{N f_s}{20 f_{clk}} \tag{5.37}$$

The precision of this circuit depends on the ratio between f_{clk} and f_s as well as the design value of R_2C_2. The larger the ratio as well as the designed RC product value, the smaller the counting error is. Considering the power consumption as well as chip area, in this design, f_{clk} is equal to f_s, R_2C_2 is set to $20/f_s$ so for typical corner, N is 20, and g is 1. The counting error is within ±5% which is acceptable as the SQNR degradation is not too much by simulation results.

The RC product detection circuit can be shut down after the normalized RC product "g" is calculated. So the power consumption is zero during its non-active period.

5.6.2.2 Simulation Results

Fig 5.22 shows the simulation results of the detection circuit at $R_{typ}C_{typ}$ corner. The value of the counter N is 20 from the simulation result, and the g is "1" from Eq. (5.37).

Fig 5.23 shows the simulation results of the detection circuit at $R_{max}C_{max}$ corner. The value of the counter N is 27 from the simulation result, and the g is "1.35" from Eq. (5.37). For this corner, R_{max}=1.15R_{typ}, and C_{max}=1.15C_{typ}, so the actual value of g is "1.3225", so the error is 2% which is within the acceptable error value.

Fig 5.24 shows the simulation results of the detection circuit at $R_{min}C_{min}$ corner. The value of the counter N is 14 from the simulation result, and the g is "0.7" from Eq. (5.37). For this corner, R_{max}=0.85R_{typ}, and C_{max}=0.85C_{typ}, so the actual value of g is "0.7225", so the error is -3% which is within the acceptable error value.

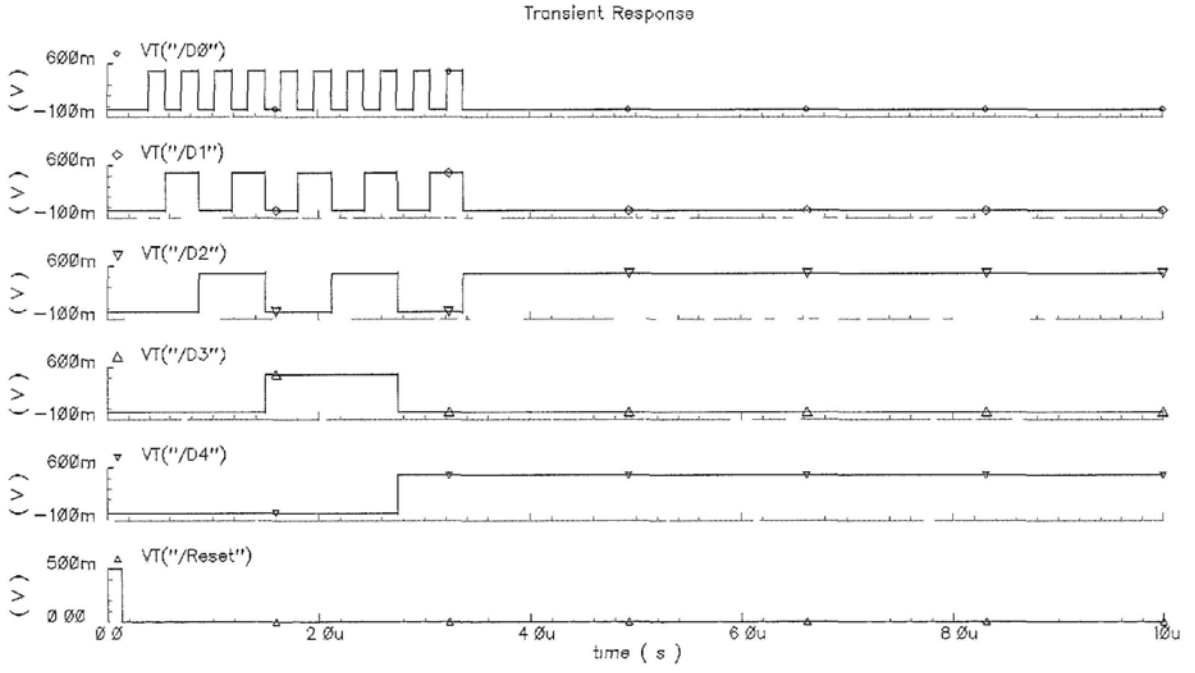


Fig 5.22 Simulated waveforms of RC product detection circuit at $R_{typ}C_{typ}$ corner.

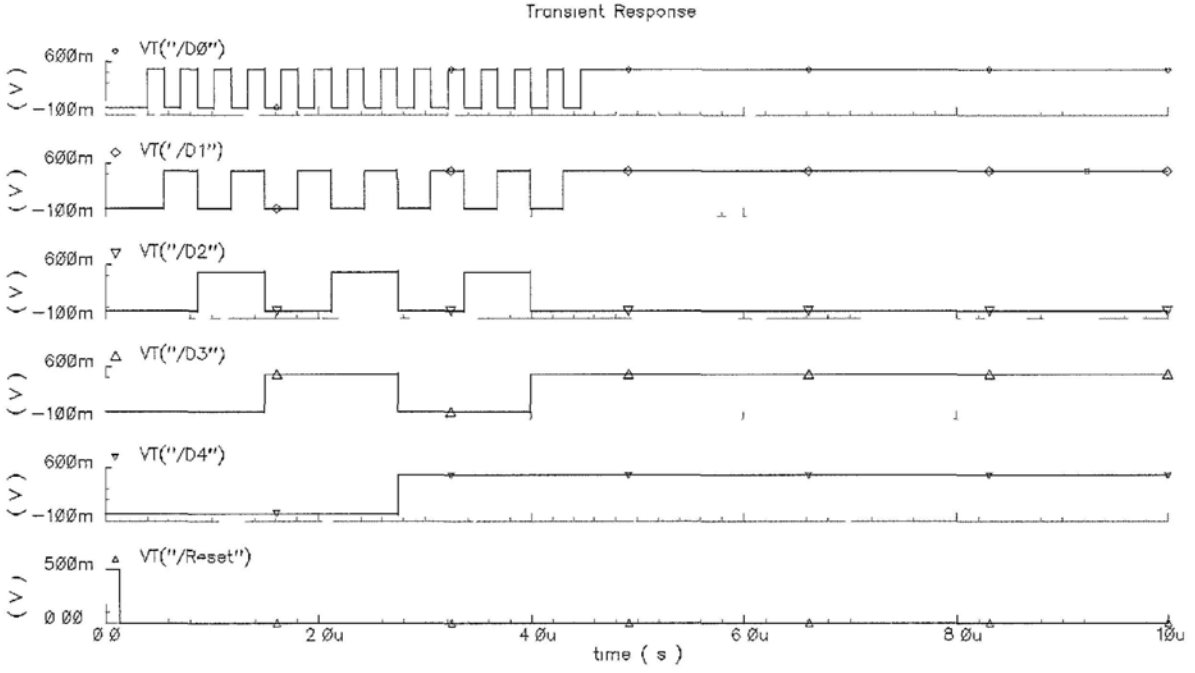


Fig 5.23 Simulated waveforms of *RC* product detection circuit at $R_{max}C_{max}$ corner.

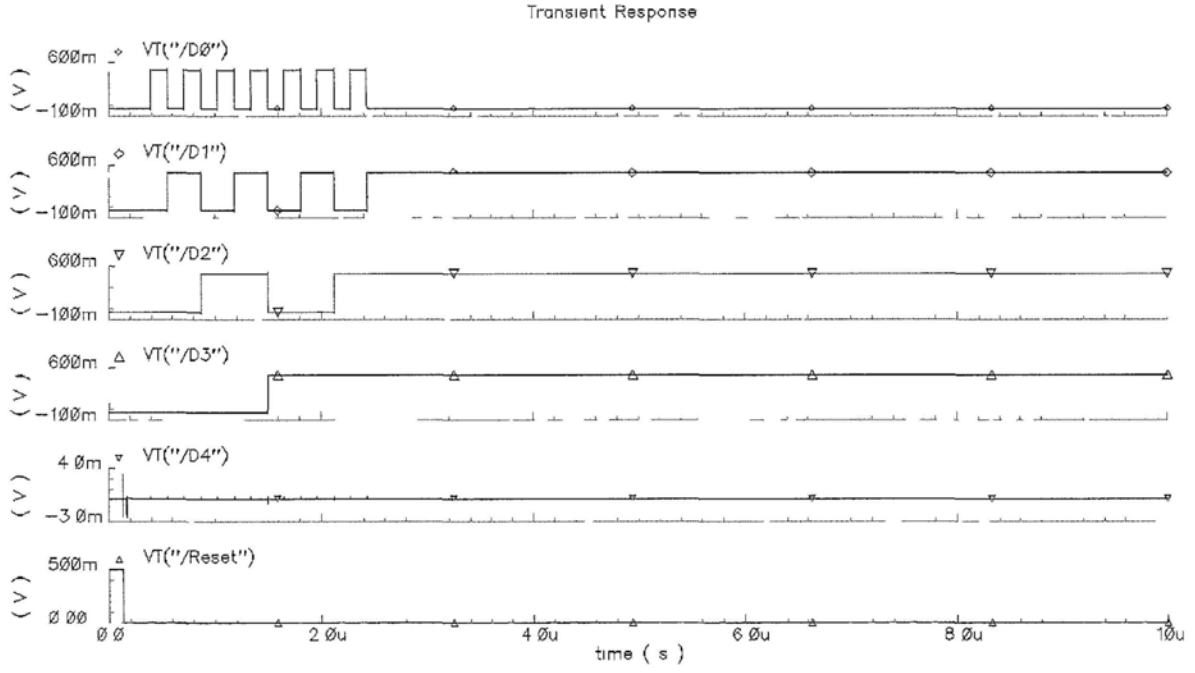


Fig 5.24 Simulated waveforms of *RC* product detection circuit at $R_{min}C_{min}$ corner.

5.6.3 Clock Generator

The compact realization of 20% T_s delay by the clock generator discussed in Chapter 3 is sensitive to PVT variation. In this section, a robust clock generator is shown to generate an accurate 20% T_s delay which is insensitive to PVT variation.

Fig 5.25 shows the clock generation circuit. The Counter1 is a counter of 10, and the Counter2 is a counter of 2. Input signal is an external 64MHz sine-wave with low clock jitter. The 20% delay from Φ_1 to Φ_C is two clock cycles of input clock, and is accurately controlled by Counter1. Fig 5.26 shows the simulation results of each clock phase.

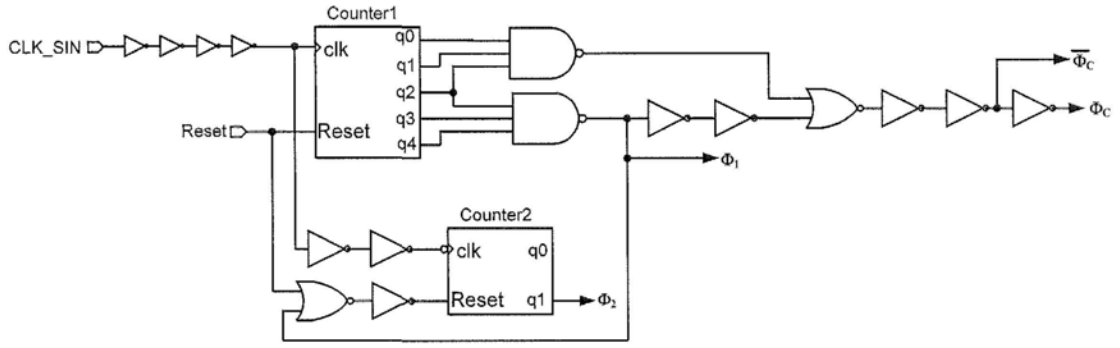


Fig 5.25 Clock generation circuit.

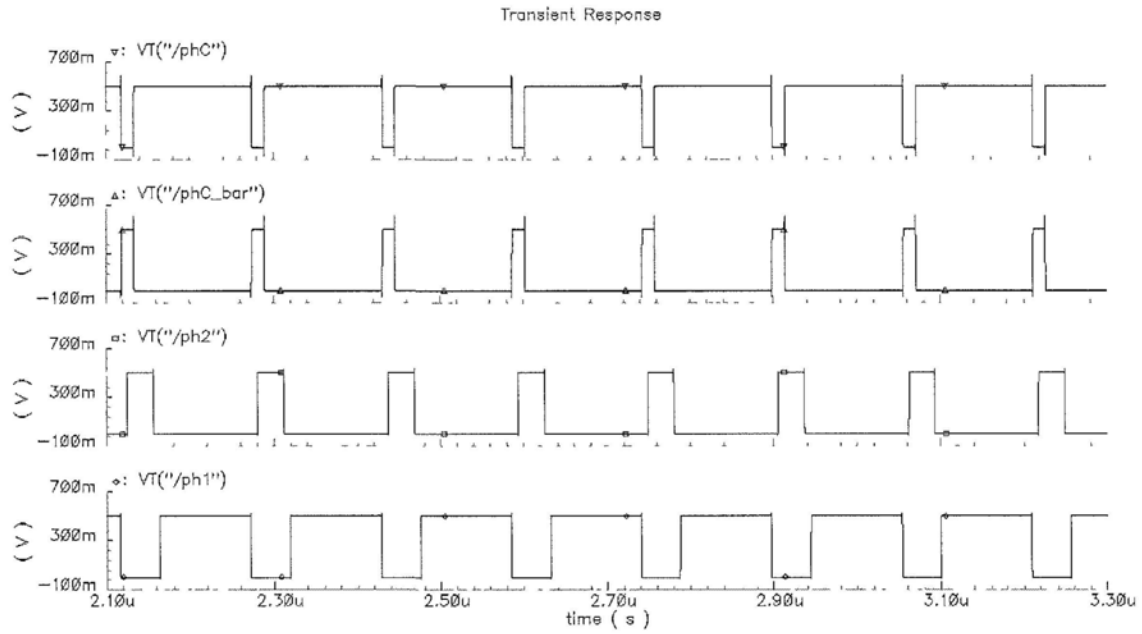


Fig 5.26 Simulated waveforms of each clock phase.

5.7 System Simulation Results

Fig 5.27 shows the output spectrum obtained from transistor-level simulations for the ΔΣ modulator in Fig 5.11 with the same input signal as Fig 5.10. The effective resolution is $98dB$ and power consumption is $350\mu W$ at 0.5V supply.

Fig 5.28 shows the simulated SNDR with a full-scale sinusoidal input at 4.3kHz for temperature between -25°C and 85°C at V_{DD}=0.5V.

Fig 5.29 shows the simulated SNDR for a V_{DD} between 0.45V and 0.8V at room temperature. All the results show the performance of the modulator is close to, or exceeds its nominal performance over a lager range of temperature as well as supply voltage. SNDR drops 2dB when V_{DD} changes from 0.6V to 0.65V due to the 3rd distortion.

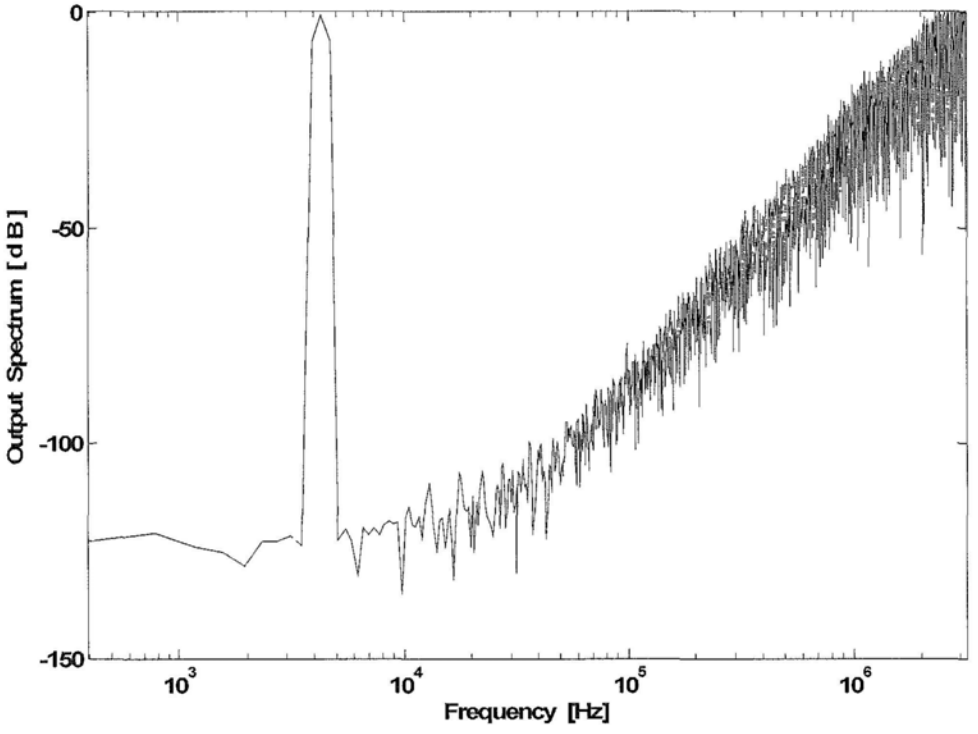


Fig 5.27 Output spectrum: transistor-level simulation of the proposed 2-1 cascaded CT ΔΣ modulator with V_{in}=0dB V_{FS} (V_{FS}=1$V_{p\text{-}p\ diff}$), f_{in}=4.3kHz.

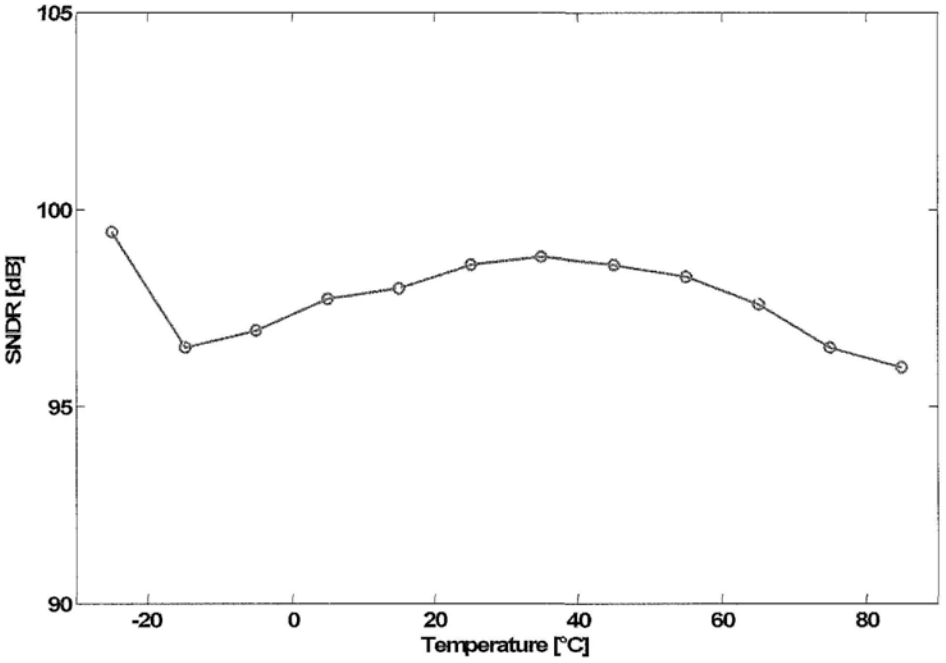


Fig 5.28 SNDR for V_m=1$V_{p\text{-}p\ diff}$ versus temperature at V_{DD}=0.5V.

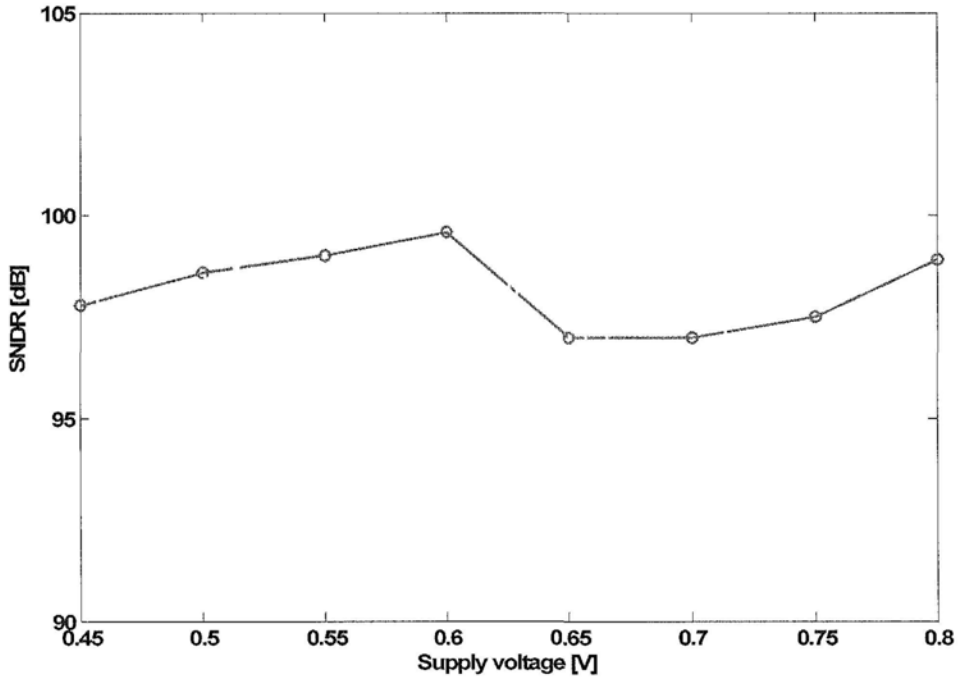


Fig 5 29 SNDR for V_m=1$V_{p\text{-}p\ diff}$ versus supply voltage at T=27°C.

5.8 Summary

A new synthesis method for cascaded CT ΔΣ modulator is presented in this chapter. It employs only one forward signal path, and the digital logics for low-order noise cancellation can be easily derived which leads to simple implementation of circuits and the digital correction of the effect of *RC* product variation.

A 0.5V 2-1 cascaded CT ΔΣ modulator has been synthesized by this method, and transistor-level simulation results show excellent performance of the modulator. A fully differential gate-body-input class-AB topology amplifier with low power consumption and *RC* product detection circuit are proposed to fulfill this design. This modulator consumes less power than the previous two chips and it may occupy more chip area than the previous two chips due to the large integrating capacitors.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

New design techniques and circuits for high-performance ΔΣ modulators under an ultra-low supply of 0.5V have been reported in this thesis.

First, a new method implementing SCR feedback under 0.5-V supply has been proposed to reduce the modulator's sensitivity to clock jitter. A key advantage of the circuit is that it does not cause any common-mode transient disturbance.

Second, a new synthesis method for cascaded CT ΔΣ modulator has been proposed. It employs only one forward signal path, and the digital cancellation logics can be easily derived as the derivation is based on DT domain analysis. This new synthesis method leads to simple implementation of circuits and the digital correction of *RC* product variation.

Third, new building block circuits enabling the realization of the 0.5-V modulators have been proposed. They include two 0.5-V amplifiers and a 0.5-V comparator. A 0.5-V fully differential gate-input amplifier with adaptive CMFB frequency compensation has been investigated to obtain a robust performance against process variation. Another 0.5-V fully differential gate-body-input class-AB amplifier features rail to rail output swing and class-AB operation has been presented to alleviate power consumption problem due to the increased slew-rate requirement by SCR feedback. A 0.5-V comparator consisting of a body-input pre-amp and a gate-clocked latch has been reported. It has a faster settling time compared with the one in [14]. A *RC* product detection circuit is also proposed in this thesis. It can realize off-chip digital correction of *RC* product variation.

Two modulator chips have been fabricated in a 0.13μm CMOS process using these proposed circuits. The first 0.5-V audio-band CT 3rd order CIFB $\Delta\Sigma$ modulator is implemented with the proposed SCR feedback circuit. Measurement results show that the modulator achieves an excellent SFDR of 93.9dB and a SNDR of 81.2dB over 25-kHz signal bandwidth while consuming only 625μW at 0.5V. The modulator also has consistent performance across a wide supply voltage range from 0.5V to 0.8V and over the commercial temperature range. The second one is a 0.5V CT 3rd order CIFF $\Delta\Sigma$ modulator implemented with the SCR feedback and the proposed 0.5V amplifier with adaptive CMFB frequency compensation. The measured SFDR, SNDR and SNR are 101.9dB, 87.76dB and 87.96dB respectively over 25-kHz signal bandwidth. The chip consumes 682.5 μW at 0.5-V. To the best of our knowledge, this performance is the best compared to other modulators operating in this supply voltage range. The modulator performs consistently over a supply voltage range from 0.4V to 0.75V and a temperature range from -20°C to 90°C.

In addition, a 0.5-V 2-1 cascaded CT $\Delta\Sigma$ modulator has been synthesized by the proposed synthesis method. Transistor-level simulation shows that a 98dB SNDR is achieved over a 25-kHz signal bandwidth with a 6.4MHz sampling frequency and 350 μW power consumption.

6.2 Future Work

There are several interesting issues remain unexplored inspired by this thesis as described below:

- Noise analysis and measurement results all demonstrate that the performance is limited by thermal noise. More research can be done to further improve the SNDR of the modulator by reducing thermal noise while keeping the power consumption low.
- To fabricate a 0.5V 2-1 cascaded CT $\Delta\Sigma$ modulator with the proposed synthesis method and the proposed 0.5V class-AB amplifier and RC product detection circuit.

- To explore high-performance ULV modulators with wider signal bandwidth.
- To explore modulators design techniques at a voltage below 0.4-V. More advanced CMOS process may be used, like a 90*nm* CMOS process.

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