A 1.5 V, 2.4 GHz Monolithic CMOS Sub-Integer-N Frequency Synthesizer for WLAN Application

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ABSTRACT

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Wireless local area networks (WLANs) are being extensively deployed since their introduction in the late 1990s. Low cost, high performance frequency synthesizers are indispensable in WLAN telecommunication systems. Meanwhile, integer-N phase-locked loop (PLL) architecture is commonly chosen due to its low circuit complexity and clean output spectrum with few spurs. However, designers have to face the tradeoffs between frequency resolution, phase noise performance and switching time. To solve the above dilemma, fractional-N PLL architecture is proposed, but fractional spurs emerge in the output spectrum, degrading the spectrum purity. Sub-integer-N PLL is thus a compromise between the integer-N and fractional-N PLL. Its structure is same as that of the integer-N while fractional division is achieved by a fractional frequency divider that is not relied on time-varying modulus control as in the fractional-N PLL.

This thesis presents the design of a 2.4 GHz sub-integer-N PLL for IEEE 802.11b/g WLAN applications. The proposed PLL not only acquires the advantages of the integer-N PLL, such as simple structure and good spurious performance, but also offers some benefits (for example, faster settling time and better phase noise performance) as in the

fractional-N PLL design. In this design, a novel quadrature-input programmable fractional frequency divider provides fractional division ratio in steps of 0.5 by the phase-switching technique. Its key building block is a dual divide-by-4 injection-locked frequency divider (ILFD), which is realized by coupling two conventional divide-by-4 ILFDs. Two different coupling schemes are introduced, namely the cross-coupling type and coherent-coupling type. In both schemes, symmetric configuration is maintained and hence does not degrade the PLL output phase quadrature accuracy. Furthermore, the generated phase pattern for phase switching is uniquely defined, which simplifies the phase-switching circuitry and suppresses the possibility of incorrect frequency division due to glitches.

To demonstrate the feasibility of the two proposed coupling methodologies, two sub-integer-N PLLs with different fractional frequency dividers have been fabricated in a 0.35 μm standard CMOS process. In design 1, the dual divide-by-4 ILFD in the fractional frequency divider is implemented with the cross-coupling scheme while the coherent-coupling scheme is used in design 2. The measured spurious tones of both designs are under -64 dBc and their measured phase noise at 1 MHz frequency offset is less than -115 dBc/Hz. The two proposed frequency synthesizers settle at approximately 32 μs and their phase mismatches of the quadrature outputs are better than 38 dB (characterized by image rejection ratio). Moreover, both designs individually occupy a chip area as small as 0.70 mm^2. At a supply of 1.5 V, the total power consumption for each design is below 24.1 mW.

摘要

自 90 年代後期提出概念起至現在，無線區域網絡 (WLAN) 的發展達到飛躍的進步，低廉且高性能的頻率合成器成爲無線區域網絡通訊系統中不可或缺的元件。在各種頻率合成器電路當中，整數分頻鎖相環因其簡潔構造和高信號純度，而被廣泛應用。不過，它受到頻率分辨度、相位噪聲和穩定速度之間折衷的限制。小數分頻鎖相環可用於解決以上難題，但衍生出來的分數雜散影響了頻譜的純度。於是，人們提出亞整數分頻鎖相環以便在兩者中取得平衡，它的好處在於擁有如整數分頻鎖相環的樸實電路結構，並以非整數除法器取代在小數分頻鎖相環中使用的時變模組控制方法來達到非整數分頻。

本論文呈獻一個依據 IEEE 802.11b/g WLAN 通訊系統考量而設計，並運行於 2.4 GHz 頻譜的亞整數分頻鎖相環。此鎖相環兼備前述兩種鎖相環的優點，如擁有像整數分頻鎖相環般的易於設計架構和高雜散性能，而穩定速度和相位噪聲也能達到一般小數分頻鎖相環所有的優勢。另一方面，在本設計中，還提出了一種嶄新的正交相位輸入、可編程非整數除法器，以相位切換技術，能獲得半步的非整數分頻步長。在此電路中，主要包含了兩個交互耦合的除四注入鎖定分頻器，而兩種不同的耦合方法將在本論文內論述，分別爲交叉耦合和同調耦合。這兩種耦合方法都保有對稱的結構，使得鎖相環輸出端的正交相位精度不受影響。此外，用於相位切換

而產生的相位順序是唯一的，所以，相位切換電路能大大簡化，也降低了因脈衝雜訊所引起的不正確分頻風險。

兩個擁有不同非整數除法器的亞整數分頻鎖相環電路經由一種標準 0.35 微米互補金屬氧化物半導體 (CMOS) 製程被製作出來，用以檢驗兩種建議的耦合方法之可行性。在一號設計內，交叉耦合方法採用在非整數除法器的雙除四注入鎖定分頻器中，而同調耦合方法則應用在二號設計內。根據實驗結果顯示，兩個鎖相環的雜散譜綫低於 -64 dBc，而離主頻 1 MHz 處的相位噪聲不多過 -115 dBc/Hz，另外，他們能在大約 32 μs 內穩定下來，輸出端的相位差也優於 38 dB (以鏡像消除比率來界定)，並且，兩個設計所佔用的芯片面積分別少於 0.7 mm^2 及總功率消耗限制在 24.1 mW 之下 (由一個 1.5 V 的電源供給)。

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LIST OF ABBREVIATIONS

ΔΣ	Delta-Sigma
BER	Bit Error Rate
BPF	Bandpass Filter
CCK	Complementary Code Keying
CMOS	Complementary Metal-Oxide Semiconductor
CORDIC	Coordinate Rotational Digital Computation
CP	Charge Pump
DAC	Digital-to-Analog Converter
DCS	Digital Cellular System
DDFS	Direct Digital Frequency Synthesizer
FCW	Frequency Control Word
FM	Frequency Modulation
FOM	Figure of Merit
GSM	Global System for Mobile Communication
IC	Integrated Circuit
ICI	Inter-Carrier Interference
IF	Intermediate Frequency
ILFD	Injection-Locked Frequency Divider
IQ	In-phase and Quadrature-phase

IRR	Image Rejection Ratio
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
LPF	Lowpass Filter
LSB	Least Significant Bit
MASH	Multi-Stage Noise Shaping
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing
MIM	Metal-Insulator-Metal
MOS	Metal-Oxide Semiconductor
MSB	Most Significant Bit
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PM	Phase Margin
ppm	Parts Per Million
QAM	Quadrature Amplitude Modulation
QVCO	Quadrature Voltage-Controlled Oscillator
ROM	Read Only Memory
SCA	Switched Capacitor Array
SCL	Source-Coupled Logic

SFDR	Spurious Free Dynamic Range
SNR	Signal-to-Noise Ratio
SoC	System-on-a-Chip
SSB	Single-Sideband
TSPC	True Single-Phase Clocking
UNII	Unlicensed National Information Infrastructure
UWB	Ultra-Wideband
VCO	Voltage-Controlled Oscillator
WLAN	Wireless Local Area Network

LIST OF SYMBOLS

ΔI_{CP}	Charge pump current mismatch
Φ_{ε}	PLL phase error in phase domain
Φ_{div}	Divider output phase in phase domain
Φ_{ref}	Reference phase in phase domain
Φ_{vco}	PLL output phase in phase domain
α	Phase shift introduced by mixing operation
β	Frequency modulation index
ϕ	Divider output phase in the dual divide-by-4 ILFD behavior model
η	Injection ratio in the dual divide-by-4 ILFD behavior model
η_{DC}	Coupling ratio in the dual divide-by-4 ILFD behavior model
φ	Phase shift introduced by the *RC* load in the dual divide-by-4 ILFD behavior model
λ_{on}	Charge pump turn-on duty cycle
τ_1	Time constant of the second pole in the PLL open loop transfer function
τ_p	Time constant of the first pole in the PLL open loop transfer function
τ_z	Time constant of the compensation zero in the PLL open loop transfer function
ω_1	Second pole in the PLL open loop transfer function

ω_c	PLL crossover frequency
ω_p	First pole in the PLL open loop transfer function
ω_z	Compensation zero in the PLL open loop transfer function
B_{CP}	Charge pump current factor
f_{ref}	Reference clock frequency
f_{vco}	VCO output frequency
$G_{loop}(s)$	PLL open loop transfer function
$H_{LF}(s)$	Loop filter transfer function
$H_{PLL}(s)$	PLL closed loop transfer function
I_{CP}	Charge pump current
I_{DC}	DC current component in the dual divide-by-4 ILFD behavior model
I_{inj}	Injection signal in the dual divide-by-4 ILFD behavior model
K_{VCO}	VCO gain
$L(\Delta f)$	Phase noise at a frequency offset Δf from the carrier
N	Division ratio
N_{frac}	Division ratio of fractional-N PLL
T_{ref}	Reference clock period
V_c	VCO control voltage

CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless local area networks (WLANs) are rapidly developed and penetrated in everyday life in the past two decades. Several generations of standards with increasing data rates and improved system performance were developed [1]. The three popular WLAN standards in use today are based on the IEEE 802.11a, 802.11b and 802.11g specifications [2]-[4]. Although the IEEE 802.11a and 802.11b standards were ratified at the same time in 1999, products based on the IEEE 802.11b standards were available in the market a couple of years earlier, making it the incumbent standard. On the other hand, to improve data throughput and to maintain backward compatibility with existing IEEE 802.11b products, the IEEE 802.11g standard was ratified in June 2003.

Table 1.1 summarizes the information of these three WLAN standards. Both IEEE 802.11b and 802.11g standards operate in the 2.4 GHz industrial, scientific and medical (ISM) band while the IEEE 802.11a standard specifies communication in the 5 GHz unlicensed national information infrastructure (UNII) band. The IEEE 802.11a standard

occupies 300 MHz bandwidth with 12 non-overlapping channels. The other two standards have an aggregate bandwidth of 83.5 MHz, where 11 channels are available in total and only three of them are non-overlapping. Besides, the IEEE 802.11a and 802.11b standards employ different modulation schemes. More sophisticated orthogonal frequency division multiplexing (OFDM) modulation with 52 sub-carriers is used in the IEEE 802.11a standard for higher data throughput while complementary code keying (CCK) modulation is employed in the IEEE 802.11b standard with maximum data rate of 11 Mbps. The IEEE 802.11g standard provides either the high data rate option as the IEEE 802.11a standard or backward compatibility with the IEEE 802.11b standards. When there is no legacy 802.11b devices in the network, 802.11g devices can operate with data rate of 6 – 54 Mbps in OFDM mode. However, in order to communicate with 802.11b devices, they can only work in CCK mode and the data rate drops to 1 – 11 Mbps.

	IEEE 802.11a	IEEE 802.11b	IEEE 802.11g
Available Spectrum (MHz)	300	83.5	83.5
Frequency (GHz)	5.15 – 5.35 5.725 – 5.825	2.4 – 2.4835	2.4 – 2.4835
Number of Non-overlapping Channels	12	3	3
Modulation Scheme	OFDM	CCK	CCK/OFDM
Data Rate (Mbps)	6 – 54	1 – 11	1 – 11, 6 – 54

Table 1.1 IEEE 802.11a/b/g WLAN standards [1]

In WLAN telecommunication systems, low cost, high performance frequency synthesizers are essential. Among them, integer-N phase-locked loop (PLL) architecture

is usually selected due to its ease in implementation and excellent spurious performance. However, the intrinsic tradeoffs between frequency resolution, phase noise performance and switching time [5] are its major drawbacks. The frequency resolution specified by the application limits the choice of reference clock frequency and loop bandwidth. The reference clock frequency cannot be larger than the required frequency resolution while the loop bandwidth is set to be less than one tenth of the reference clock frequency for PLL loop stability [6]. As such, it leads to high division ratio and narrow loop bandwidth if fine frequency resolution is recommended. The in-band phase noise contribution is also amplified by large division ratio and the phase noise specification for the reference clock becomes tough. Moreover, with narrow loop bandwidth, the PLL settling time is long and the phase noise contributed by the VCO is not suppressed sufficiently due to low cutoff frequency.

Fractional-N PLL architecture is hence used to solve the above dilemma. Since the dependence of loop bandwidth on frequency resolution is void, the frequency resolution can be set arbitrarily fine with wide loop bandwidth. Due to the loop bandwidth expansion, the VCO phase noise contribution is attenuated more and the PLL settling time becomes shorter. The in-band phase noise amplification can also be optimized with appropriate selection on frequency resolution and division ratio. Nevertheless, the spectral purity is deteriorated by fractional spurs due to the time varying division modulus control. Dithering or sigma-delta-based averaging [7] is the common practice to randomize the division modulus pattern for spur and quantization noise suppression, but residual spurs cannot be completely eliminated due to mismatches in the circuit components (for example, the charge pump current mismatch [8]).

As a compromise, sub-integer-N PLL [9] is proposed. It shares the same architecture as integer-N PLL, but provides fractional frequency resolution. This relieves the intrinsic tradeoffs in integer-N PLL. On the other hand, unlike in fractional-N PLL, fractional frequency division is accomplished by a fractional frequency divider with time-invariant modulus control. Consequently, the circuit structure is simple, the spurious performance is superior, no unexpected fractional spurs are created, the reference clock frequency and loop bandwidth can be higher, division ratio can be decreased, and phase noise can be well suppressed.

In this research, the implementation of a 2.4 GHz sub-integer-N PLL for IEEE 802.11b/g WLAN applications in a standard 0.35 μm CMOS process is demonstrated. Details of the system level design and block level circuit implementations are presented.

1.2 Thesis Organization

Besides this introductory ones, there are six additional chapters. In Chapter 2, general considerations in frequency synthesizer design are discussed. Overviews of integer-N PLL operation principle and different architectures for sub-integer frequency synthesis are also presented. The system level design of the proposed frequency synthesizer architecture is then addressed in Chapter 3.

In Chapter 4, the structure of the proposed programmable fractional frequency divider and its circuit implementation are demonstrated. The characteristics of the novel dual

divide-by-4 injection-locked frequency dividers (ILFDs) are also analyzed. Afterwards, in Chapter 5, the circuit implementation of other building blocks, including the quadrature voltage-controlled oscillator (QVCO), phase frequency detector (PFD), charge pump and loop filter, is depicted.

Experimental verifications of the proposed frequency synthesizers and the circuit components (including the QVCO, dual divide-by-4 ILFDs and programmable fractional frequency dividers) are described in Chapter 6. Finally, conclusion is drawn in Chapter 7.

CHAPTER 2

FREQUENCY SYNTHESIZER BACKGROUND

2.1 General Considerations

2.1.1 Frequency Accuracy

The frequency accuracy of frequency synthesizers is essential. For instance, frequency tolerance of less than 25 ppm is specified in the IEEE 802.11 WLAN standard. Typically, the reference frequency of frequency synthesizers is derived from a high accuracy crystal oscillator. Due to temperature variation and crystal aging effect, frequency error is inevitable and cause rotation in the signal constellation for quadrature-modulated signal. On the other hand, the orthogonal frequency division multiplexing (OFDM) modulation scheme employed in the IEEE 802.11a/g standards requires accurate frequency synchronization between the receiver and the transmitter; otherwise frequency offsets will induce inter-carrier interference (ICI), that is, crosstalk between the sub-carriers.

Frequency compensation of crystal oscillator [10] can be performed to adjust its oscillating frequency. The frequency shift is first measured in the rotated constellation diagram during the training phase at the beginning of communication. Frequency correction is then applied on the crystal oscillator. Besides, in some WLAN applications, frequency correction is performed directly on the received constellation by multiplying it with a complex exponential signal for constellation rotation [11].

2.1.2 Frequency Resolution

The frequency resolution of frequency synthesizers is the minimum frequency step that can be provided by the systems. Usually, it is determined by the required channel spacing for the intended application. Depending on the chosen frequency synthesizer architecture, the specified frequency resolution may limit the choice of system parameters and thus affect the system performance too. For example, the reference frequency of integer-N phase-locked loop (PLL) is generally equal to its frequency resolution. Its loop bandwidth is then set as one tenth of the reference frequency for stability [6]. Once the loop bandwidth is specified, the phase noise performance, spurious suppression and switching time of the PLL are determined.

2.1.3 Phase Noise

Phase noise is defined as the ratio between the total carrier power and the noise power in 1 Hz bandwidth at frequency offset Δf from the carrier f_0, which is:

$$L(\Delta f) = 10\log\left(\frac{\text{power in 1 Hz bandwidth at } f_0 + \Delta f \text{ frequency offset from the carrier}}{\text{total carrier power}}\right) \quad (2.1)$$

Frequency synthesizer phase noise will corrupt both upconverted and downconverted signals [12], degrading the signal-to-noise ratio (SNR) of the wanted signals. As shown in Figure 2.1, the phase noise sideband of a nearby strong interferer at f_1 condemns the frequency band of the weak desired signal at f_2. Even with a noiseless receiver, the desired signal cannot be discriminated from the phase noise of the nearby interferer as they are in the same frequency band. As such, in wireless communication standards, the transmitter output spectrum should obey the transmit spectrum mask, which specifies the maximum noise levels at certain frequency offsets from the carrier frequency.

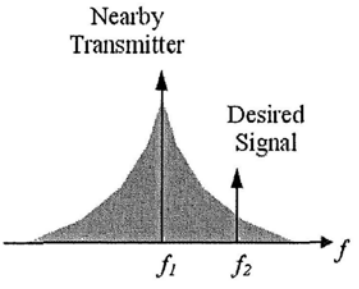


Figure 2.1 Influence of phase noise in a transmitter

Direct and reciprocal mixing effects [13] occur in downconversion, as depicted in Figure 2.2. If the LO contains phase noise and a strong interferer locates near the desired signal, two overlapping noise spectra are created at the intermediate frequency (IF) after downconversion. The LO phase noise is superposed into the wanted signal by direct mixing while the phase noise sideband of the interferer corrupts the desired signal by reciprocal mixing. The SNR of the demodulated signals hence degrades.

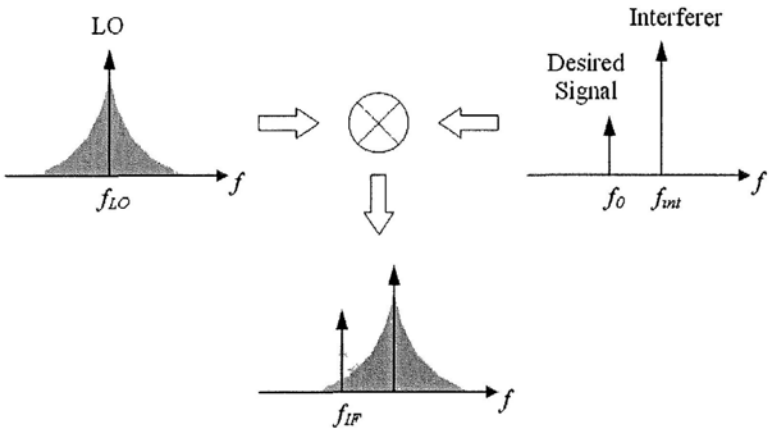


Figure 2.2 Influence of phase noise in a receiver

It can be seen that the influence of reciprocal mixing is determined by the LO phase noise at large frequency offset from the carrier, fallen into the desired signal frequency band. The phase noise at such region is usually dominated by that of voltage-controlled oscillators (VCOs). Therefore, VCO design with low phase noise has a direct impact on the reciprocal mixing effect. Moreover, the main consideration in the direct mixing effect is the in-band phase noise contribution of frequency synthesizers, which needs system optimization (for instance, decrease of loop bandwidth with sacrifice of speed).

2.1.4 Spurious Signals

In addition to phase noise, unwanted spurious signals appear in the output spectrum of frequency synthesizers. They are usually generated due to parasitic coupling of signals in the systems. For example, the reference spurs in integer-N PLL are induced by charge injection of the charge pump at a rate equal to the reference frequency. Ripples with frequency components at multiples of the reference frequency occur at the VCO control

input and modulate the VCO oscillating frequency. Spurious tones are then generated at frequency offsets equal to multiples of the reference frequency from the carrier.

In some occasions, spurious signals may mix with interference and the resulting signals fall into the desired signal frequency band, deteriorating the desired signal SNR. An example is illustrated in Figure 2.3. The frequency synthesizer output contains a main tone at f_{LO} and a spur at f_s. The desired signal at f_0 is convolved with the LO and shifted to f_{IF}, where $f_{IF} = f_0 - f_{LO}$. The interference signal is also downconverted to f_{IF} if $f_{int} - f_s = f_{IF}$. Consequently, the wanted signal is condemned.

Spurious signals can be suppressed by reducing the PLL loop bandwidth or increasing the loop filter order at the expenses of longer settling time and PLL stability.

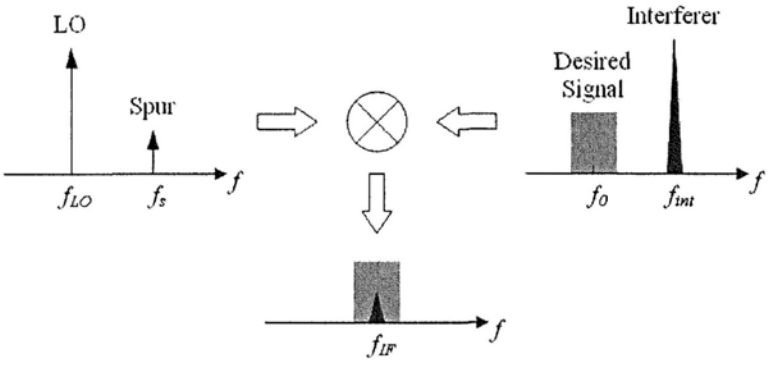


Figure 2.3 Influence of spurious signals in a receiver

2.1.5 Switching Time

In frequency hopping telecommunication systems like Bluetooth™, frequency synthesizers have to switch from one frequency to another within certain frequency

accuracy at a specified time slot. The switching time for Type-II, third-order PLL-based frequency synthesizers can be estimated as [14]:

$$t_{lock} = \frac{\ln\left(f_{step} / f_{error}\right)}{f_c \cdot \xi_e(\phi_m)} \tag{2.2}$$

where

f_c	the open loop bandwidth
f_{step}	the amplitude of frequency jump
f_{error}	the maximum frequency error at t_{lock}
ϕ_m	the phase margin
$\xi_e(\phi_m)$	the effective damping coefficient at a specified phase margin

As suggested in Equation 2.2, wide loop bandwidth is beneficial for fast switching time. However, the phase noise and spurious performance become worse as a tradeoff. PLL stability should also be considered because the loop bandwidth is limited to at least one tenth of the reference frequency, as a rule of thumb.

2.1.6 Power Dissipation

Low power consumption is a crucial aspect for portable electronic devices and products. First, it determines the battery life-time and standby-time of the portable products. Additionally, since less heat is generated, the failure due to thermal problem is alleviated and thus the product lifetime and reliability improve. To achieve low power dissipation for frequency synthesizers, current reuse [15] is one of the possible solutions.

2.1.7 Integration Level

Full integration of frequency synthesizers in the monolithic CMOS process faces two bottlenecks, namely the absence of high quality factor inductor and considerable area occupied by the loop filter capacitors. Conductor loss and substrate loss are the main causes for the high loss of on-chip inductors. Bond wires [16] can be used to replace on-chip inductors, but they lack accurate modeling and their reliability and repeatability are poor. Nowadays, the modern CMOS technology with mixed-signal RF option provides thick top metal layer and less conductive substrate to improve the quality factor of on-chip inductors.

The loop dynamic behavior and phase noise performance of frequency synthesizers determine the capacitor size of the loop filter. High capacity MIM capacitor is available in the modern CMOS process to minimize capacitor area. Moreover, the capacitance multiplier [17] and dual path loop filter topology [18] can be used to reduce the capacitor size with tradeoffs of extra power consumption and noise contribution.

2.1.8 Sensitivity to Interference

In modern telecommunication systems, the system-on-a-chip (SoC) solution acquires low cost and small form factor by implementing all functions in a single design. Nevertheless, this induces serious unwanted coupling to sensitive parts of the system and crosstalks in the substrate. Spike-like noise produced by digital baseband circuits on the supply and on the substrate may deteriorate the spectrum purity of frequency synthesizers with spurious

tones. Careful designs in layout [19] help to isolate the noise sources. Furthermore, the frequency pulling by the power amplifier (PA) in the direct conversion transmitter [20] may corrupt the synthesized signal, degrading system performance. Clever frequency planning [21], [22] has to be adopted to ensure that the PA output spectrum and LO output are sufficiently far apart.

2.2 Integer-N Phase-Locked Loop

Figure 2.4 depicts the integer-N PLL structure, which consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter, a VCO and a frequency divider. It can be used to generate a high frequency carrier with low frequency drift and superior spurious performance, from a low frequency accurate reference source (for example, crystal oscillator). The PLL output frequency f_{out} is N times greater than the reference frequency f_{ref}, where N is an integer. Additionally, it is synchronized in phase with the reference source.

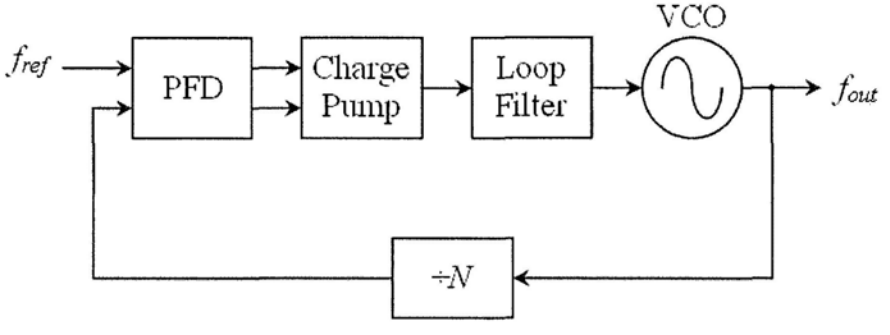


Figure 2.4 Block diagram of an integer-N phase-locked loop

Integer-N PLL is a feedback system. The PLL output frequency is scaled down N times by the frequency divider in the feedback path. It is then used for comparison with the reference source to determine if the system is in lock. Comparison is performed by the PFD, which is an error detector to detect both phase and frequency differences between the reference source and the frequency divider output. The PFD controls the charge pump to inject correction current pulses with appropriate polarity, duration and amplitude. The charge pump correction current is filtered by the loop filter to extract the desired average VCO control voltage level. Any high frequency components in the VCO control voltage are removed to assure the VCO output spectral purity. Afterwards, the VCO alters its oscillating frequency with respect to the change in its control voltage level. The frequency regulation process repeats until no phase and frequency error is detected by the PFD.

Integer-N PLL is the most commonly used frequency synthesizer architecture due to its simple structure and good spurious performance. Its building blocks are well developed and can be integrated together without great difficulty, which speeds up the implementation process. Moreover, it does not generate any unexpected spurious tones in its output spectrum and the reference spurs can be easily suppressed by the loop filter.

The main deficiency of integer-N PLL is the tradeoffs between frequency resolution, phase noise performance and switching time. The frequency divider in integer-N PLL only acquires integral division ratio. As such, the PLL output frequency should be the integer multiple of the reference frequency and the frequency resolution is limited by the reference frequency. Since the PLL loop bandwidth is generally set less than one tenth of

the reference frequency for stability, fast settling behavior is restricted with narrow loop bandwidth. On the other hand, the large division ratio due to fine frequency resolution also causes deterioration of the in-band phase noise characteristic due to high amplification factor. The considerable VCO phase noise contribution is another issue as it is not attenuated with narrow loop bandwidth.

2.3 Architectures for Fractional Frequency Synthesis

2.3.1 Direct Digital Frequency Synthesizer

The Direct digital frequency synthesizer (DDFS) was first proposed by Tierney *et al.* in 1971 [23]. Figure 2.5 shows its architecture for sine wave generation, which composes of four basic building blocks: a phase accumulator, a phase to amplitude sine function generator, a digital-to-analog converter (DAC) and a lowpass filter (LPF).

The phase accumulator consists of a L-bit full adder and a L-bit phase register, functioning as an overflowing accumulator to generate instantaneous phase argument for the sine function generator. The frequency control word (FCW) controls the rate of phase accumulator overflow, which corresponds to one sine wave output period. With the input clock frequency f_{clk}, the output frequency f_{out} and frequency resolution Δf can be expressed as:

$$f_{out} = \frac{FCW}{2^L} f_{clk} \qquad 0 \le FCW \le 2^{L-1} \tag{2.3}$$

$$\Delta f = \frac{f_{clk}}{2^L} \tag{2.4}$$

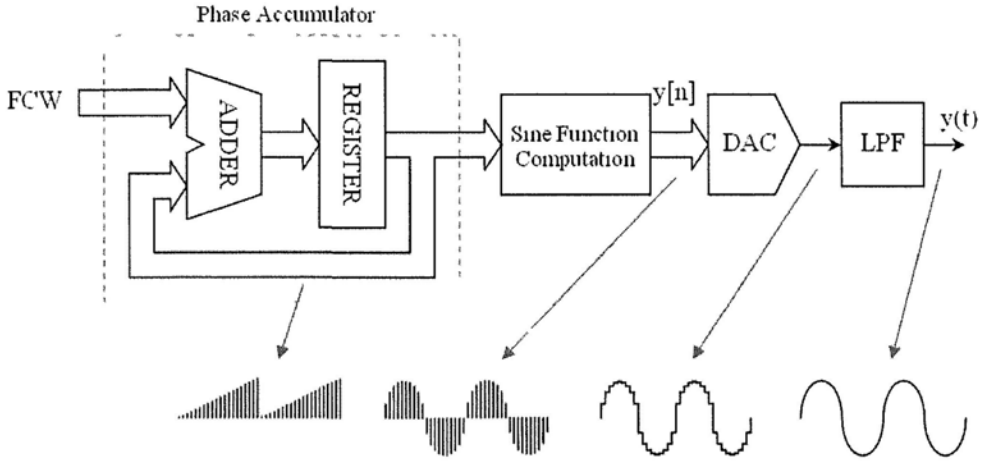


Figure 2.5 Block diagram of a sine-output direct digital frequency synthesizer

The instantaneous phase values generated by the phase accumulator are then passed to the sine function generator, which is a sine function ROM lookup table in the simplest implementation. Discrete sine output waveform is produced and converted to analog output by the DAC. To remove the harmonics and high frequency spurious signals, a lowpass filter is used.

Since the DDFS does not have a feedback loop, agile frequency switching can be acquired. Its frequency synthesis process is completely performed in digital domain, enabling transient free frequency changes with phase continuity, direct phase and frequency modulation in digital domain, and excellent temperature and aging stability.

Fine frequency resolution can also be obtained easily by increasing the number of bits in the phase accumulator. Besides, the DDFS is a synchronized system with low phase jitter as its phase noise performance is typically determined by that of the input clock source.

In spite of its many advantages, the DDFS is only suitable for manipulating IF signals of few hundreds MHz since power consumptions of both digital circuitry and DAC are huge when operating at high speed. Furthermore, the DDFS output frequency is fundamentally limited by the Nyquist criterion to bandwidth of $f_{clk}/2$. In practice, however, it is constrained to be less than $f_{clk}/3$ due to the circuit limitation and spurious problem [24].

The sine function generator is considered as the most critical block in DDFS. High frequency resolution and good spectral purity require large ROM size and it is power hungry to scan the ROM at high speed. Generally, the sine function quarter-wave symmetry property is exploited to reduce the ROM size [25]. The ROM size is also truncated to less than L-bit, but the quantization effect leads to degradation in spurious free dynamic range (SFDR) of the systems. Various optimization approaches for the sine function generator were introduced in literature and are classified into three categories: 1) CORDIC-like angle-rotation algorithms [24], [26]–[28]; 2) polynomial interpolation techniques [29]–[32]; and 3) angular decomposition ROM compression techniques [33]–[35].

In CORDIC-like angle-rotation approaches, coordinate rotation of a vector with known sine and cosine values in complex plane is performed until the error to desired angle is sufficiently small. Very small lookup memories are needed, but a complex arithmetic

circuitry is required, limiting operation speed and increasing power dissipation and tuning latency.

In polynomial interpolation techniques, trigonometric functions are approximated by using interpolation in each equal-length sub-interval. Only a small ROM is used to store the polynomial coefficients and some additional arithmetic circuitries (adders, multipliers, etc.) are built to implement the polynomial approximation.

The last method, angular decomposition ROM compression technique, divides the lookup table into smaller parts. One table stores the coarse value while others contain the fine values. The final sine/cosine values are obtained by adding up the coarse and fine values. Small lookup table and simple arithmetic circuitry are the advantages of this method.

Instead of optimizing the sine function generator, another approach was proposed in literature to eliminate the ROM completely by using a nonlinear DAC [36], [37]. The sine function generator and DAC are combined into a single nonlinear DAC to perform phase-to-amplitude transformation and digital-to-analog conversion simultaneously. Circuit complexity is reduced and considerable area and power are saved.

Due to its fast switching speed, fine frequency resolution and high precision frequency control, the DDFS plays an important role in wireless telecommunication systems (including frequency hopping and spread-spectrum systems), radar applications, electronic warfare and high precision measurement systems.

2.3.2 Fractional-N Phase-Locked Loop

For frequency synthesizer applications which demand fast switching time with narrow channel spacing, fractional-N PLL is a suitable candidate. It can synthesize fractional multiples of the reference frequency with fine resolution. High reference frequency can be used, which results in wide loop bandwidth and agile switching time.

Figure 2.6 depicts the block diagram of a fractional-N PLL [38]. The frequency divider is implemented as a dual-modulus prescaler with division ratios of N and $N + 1$, which is controlled by a k-bit digital accumulator. The digital word input K determines the accumulator overflow rate. Once the accumulator overflows, a carry bit is generated to change the dual-modulus prescaler division ratio. In each cycle, the dual-modulus prescaler divide K cycles by $N + 1$ and $2^k - K$ cycles by N and hence the average division ratio N_{frac} is evaluated as:

$$N_{frac} = \frac{(2^k - K)N + K(N+1)}{2^k} = N + \frac{K}{2^k} \tag{2.5}$$

where N is an integer and the last term belongs to the fractional part.

According to Equation 2.5, long accumulator length k results in fine frequency resolution, but this complicates the accumulator design and consumes more power. On the other hand, the choice of the reference frequency f_{ref} and the frequency resolution requirement specifies the minimum number of bits needed in the accumulator.

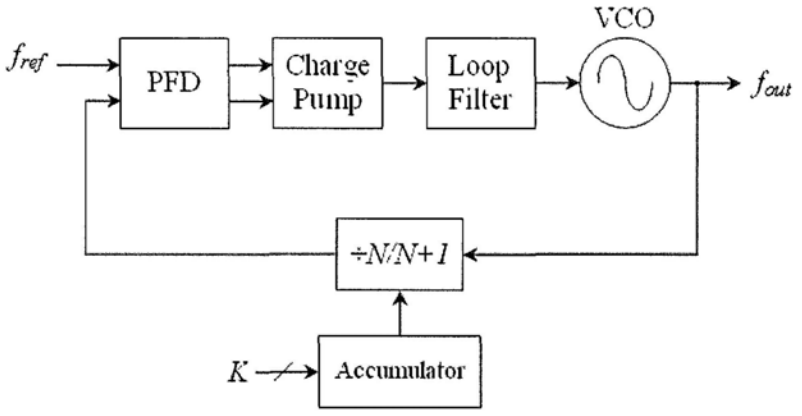


Figure 2.6 Block diagram of a fractional-N phase-locked loop

High reference frequency not only leads to wide loop bandwidth and fast settling time, but also improves system phase noise performance. With wide loop bandwidth, VCO phase noise is attenuated more by the highpass characteristic with increased cutoff frequency. Division ratio N becomes smaller and therefore the in-band phase noise is less amplified.

In spite of its various advantages, fractional-N PLL faces fractional spur problem. The accumulator overflows and changes the division modulus periodically in the fractional-N frequency synthesis. For example, to realize fractional division ratio of $N + 0.25$, the accumulator output bit pattern is N, N, N, $N + 1$, which repeats at frequency of $f_{ref}/4$. Although the overall phase error for each cycle is zero, the phase difference between the reference clock and frequency divider output is nonzero and varies repetitively. Frequency components at multiples of $\pm f_{ref}/4$ are generated at the VCO control input. Due to frequency modulation performed by the VCO, spurious tones appear next to the carrier at frequency offsets of $\pm n \cdot f_{ref}/4$, where n is an integer. Fractional spurs at large frequency

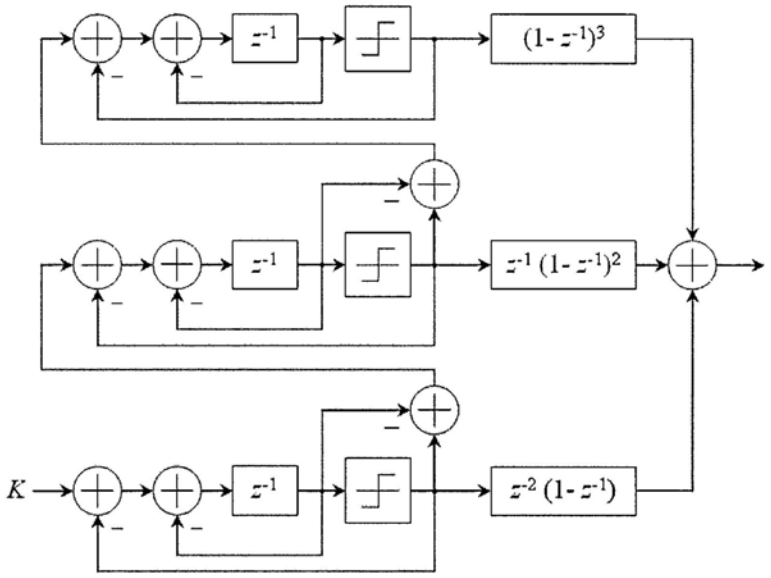
offsets can be filtered out by the loop filter, but the problem becomes severe for those fall within the loop bandwidth.

To eliminate fractional spurs, the phase error should be compensated. In the classical approach [39], the accumulator provides phase error information to control a DAC, generating opposite polarity current pulses at the charge pump output to cancel out periodicities in the phase error signal. The compensation scheme depends heavily on the precise match between the DAC output and the phase error signal, which is sensitive to temperature and process variations.

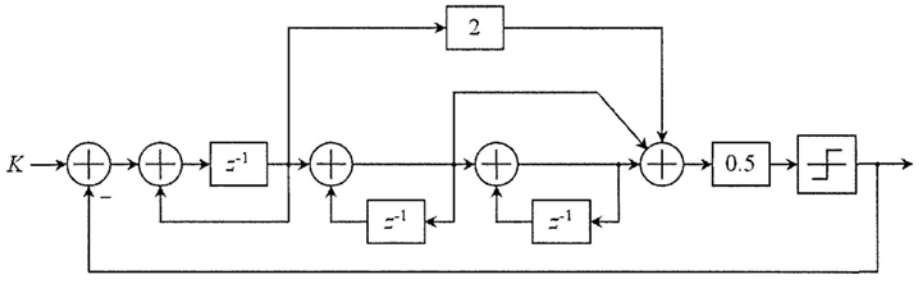
A more effective solution is to replace the accumulator by a delta-sigma ($\Delta\Sigma$) modulator [7], [40]–[45]. The $\Delta\Sigma$ modulator randomizes the division modulus to eliminate its periodicity. The resulting bit stream consists of an average value equal to the desired fractional division ratio and of shaped quantization noise. The quantization noise introduced is whitened and transposed to high frequencies, which is attenuated by the loop filter. Besides, since high order modulators are generally required to obtain sufficient noise suppression within the loop bandwidth, quantization noise at large frequency offset becomes serious and hence a higher order loop filter is implemented to counteract increased noise slope.

Another advantage of using the $\Delta\Sigma$ modulator in fractional-N PLL is the ability of indirect digital frequency modulation at RF [42], [43]. This greatly simplifies the transmitter structure. Furthermore, all-digital implementation of the $\Delta\Sigma$ modulator is favorable in CMOS technology, providing convenient approach for full chip integration.

There are two main topologies of ΔΣ modulators used in fractional-N PLLs, namely the multi-stage noise shaping (MASH) structures [42], [43] and the single loop architectures [44], [45]. Third-order examples of these two topologies are displayed in Figure 2.7.



(a)



(b)

Figure 2.7 Architectures of third-order ΔΣ modulators a) MASH [43] and b) single loop [45]

The MASH ΔΣ modulator consists of first-order modulators in cascade, where the quantization error of previous stage is the input to next stage. Quantization errors of all stages except the last one are cancelled out by summing the stage outputs in a noise-

shaping block. Since there is no feedback path between different stages and each stage is first-order, the MASH ΔΣ modulator is unconditionally stable [46]. Besides, it is simple in structure, only adders and registers are needed. Pipelining [42] can be applied to further reduce logic gate count and power dissipation. However, the MASH ΔΣ modulator tends to generate widespread fast-changing bit patterns, which transits substantial amount of quantization noise to high frequency. High order loop filter is thus needed to attenuate the high frequency quantization noise.

In contrast to the MASH counterpart, the single loop ΔΣ modulator composes of accumulators with feedforward and feedback coefficients. There is higher flexibility in constructing the noise transfer function (NTF), but stability is a concern for high order topologies. By proper pole positioning, the high frequency quantization noise can be smoothed out, which relaxes the loop filter design. The prescaler division modulus switching is less intense and its dynamic range is enhanced when compared with the MASH ΔΣ modulator. Nonetheless, there is a tradeoff between structure complexity and noise transfer function realization. The feedforward and feedback coefficients are usually approximated to values in power of two for the sake of complete removal of multipliers. As such, the stability and causality of the approximated NTF should be verified.

2.3.3 Dual-Loop Frequency Synthesizer

As the name suggested, the dual-loop frequency synthesizer composes of two PLLs. One PLL generates a fixed high frequency carrier while another produces a low frequency signal with fine frequency steps. The low frequency signal is then superposed on the high

frequency carrier to obtain the desired carrier frequency and frequency resolution. An example [47] is given in Figure 2.8. Large loop bandwidth can be chosen in the high frequency loop to attenuate the VCO1 phase noise. In the low frequency loop, the VCO2 phase noise contribution is comparatively low [48] due to low center frequency. The overall phase noise performance is therefore good. But, the single-sideband (SSB) mixer specifications are critical. Poor spurious performance results due to the phase mismatches of both PLLs quadrature outputs, and nonlinearity and mismatches of the SSB mixer.

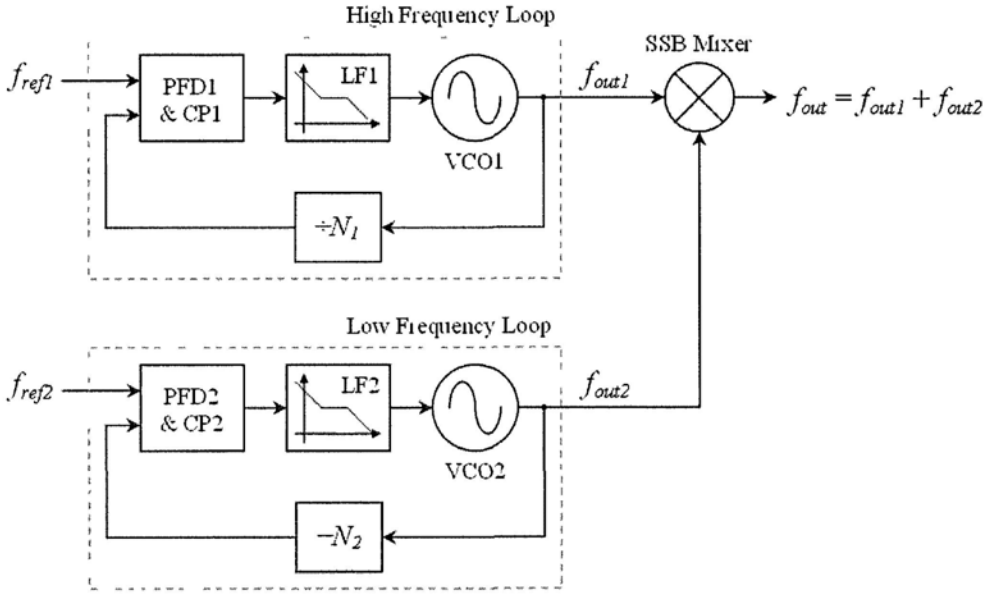


Figure 2.8 Architecture of a parallel configuration dual-loop frequency synthesizer

Another dual-loop frequency synthesizer in parallel configuration [47] is presented in Figure 2.9. The two PLLs operate at approximately half of the output frequency. Since its frequency resolution is determined only by the difference of the two reference frequencies, large values of reference frequencies can be selected to acquire wide loop bandwidth in both PLLs. Spurious performance of this frequency synthesizer type is

limited by the SSB mixer performance. On the other hand, the cross products of the two PLL outputs' harmonics may fall into the desired frequency band. This restricts the choice of the center frequency f_0 and reference frequencies f_{ref1} and f_{ref2}. Frequency pulling also occurs as both PLLs operate at almost the same center frequency.

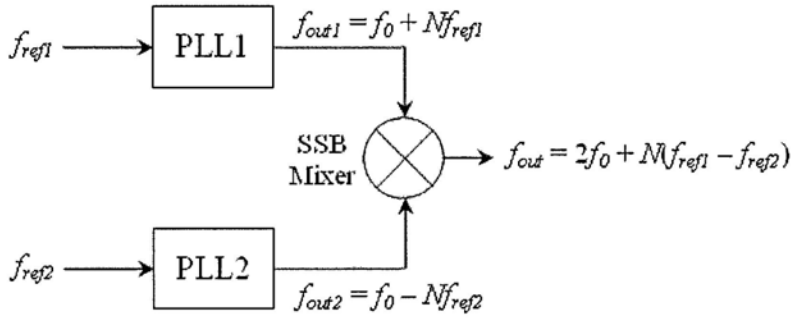


Figure 2.9 Architecture of a parallel configuration dual-loop frequency synthesizer using vernier effect

To alleviate its specifications, the SSB mixer can be placed inside the PLL feedback loop. In this way, the sidebands due to component mismatches and harmonics are attenuated by the loop filter. Two examples for GSM-900 [49] and DCS-1800 [50] applications are illustrated in Figure 2.10 and 2.11 respectively. Compared with traditional integer-N PLLs, division ratio can be greatly reduced in dual-loop frequency synthesizers. For example, the division ratio of an integer-N PLL for GSM-900 application should be 4236 – 4449 to realize channel spacing of 200 kHz while, in [49], it is just 226 – 349 (more than 10 times reduction).

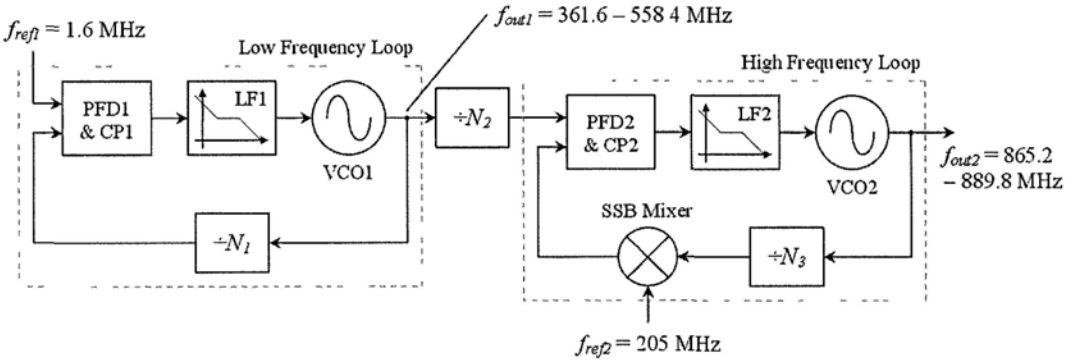


Figure 2.10 Architecture of a series configuration dual-loop frequency synthesizer at 900 MHz

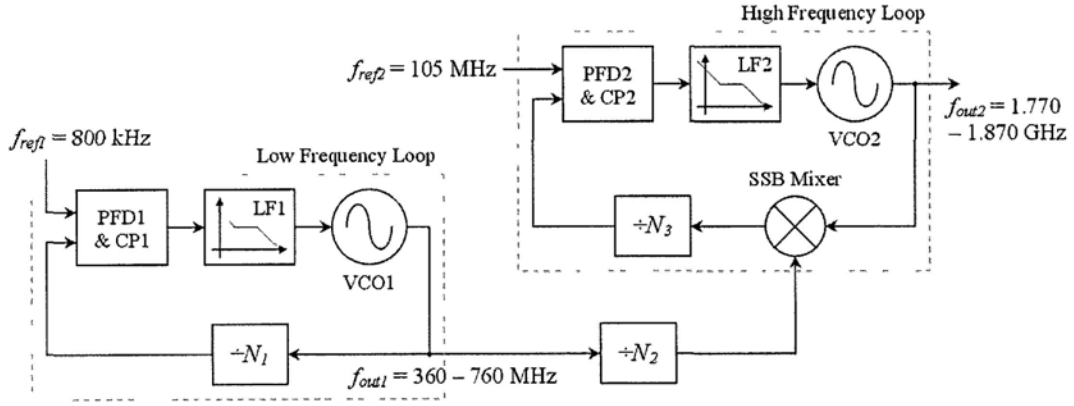


Figure 2.11 Architecture of a series configuration dual-loop frequency synthesizer at 1.8 GHz

In this dual-loop frequency synthesizer type, two PLLs are connected in series. The low frequency loop output becomes the high frequency loop input. In Figure 2.10, the divided low frequency loop output acts as the PFD2 input in the high frequency loop while it is inputted to the SSB mixer in Figure 2.11. Their noise transfer functions are different. In the first design, the low frequency loop phase noise is amplified by division ratio N_3 in the high frequency loop, but not in the second design.

Channel selection is performed in the low frequency loop with a multi-modulus frequency divider N_1 and wide loop bandwidth is preferable for fast switching time. Besides performing frequency upconversion, the high frequency loop is also intended for the suppression of phase noise and spurious tones induced by the low frequency loop.

Compared with integer-N PLLs, dual-loop frequency synthesizers acquire higher reference frequencies and lower division ratio, which are advantageous for wide loop bandwidth, fast switching time and low in-band phase noise. But their drawbacks include the need of two reference sources and more circuit components.

2.3.4 Frequency Synthesizer with Truly Modular Fractional Frequency Divider

Conventional flip-flop-based static frequency dividers act as frequency counters. The counters go through the state sequence repeatedly and advance one state in each clock cycle to provide integral division ratio. By using double-edge-triggered flip-flops instead of single-edge-triggered ones, the original divide-by-N circuits can work as divide-by-$N/2$ frequency dividers because the routine state propagation occurs at both rising and falling edges of the input clock. Examples with fixed fractional division ratio [51]–[53] and dual-modulus design [54], [55] can be found in literature.

A double-edge-triggered flip-flop [56] composes of two latches and a multiplexer. The two latches operate at different time slots, utilizing both positive and negative level of the input clock, while the multiplexer selects the output from the latch that is holding the

valid data. All of them are synchronized with the input clock and hence input clock loading increases. In order to guarantee sufficient time margin for related logic operation during both clock Hi and Lo cycles, the input clock duty cycle should be 50%. As such, a duty cycle corrector [51], [52] is needed, which consumes power and chip area.

Extra logic gates and flip-flops are required in divide-by-*N*/2 designs when compared with their divide-by-*N* counterparts. For example, a divide-by-11 frequency divider can be implemented by using four flip-flops and some combinational logic gates. If implemented using double-edge-triggered flip-flops instead, divide-by-5.5 operation results and a circuit example is shown in Figure 2.12. In addition to the four flip-flops and combinational logic gates for the state machine in the original circuit, two more D-flip-flops, one RS latch and some logic gates for output manipulation and state machine initialization are required. The extra components not only increase the input clock loading, but also prolong the critical path propagation delay, limiting the circuit operation speed.

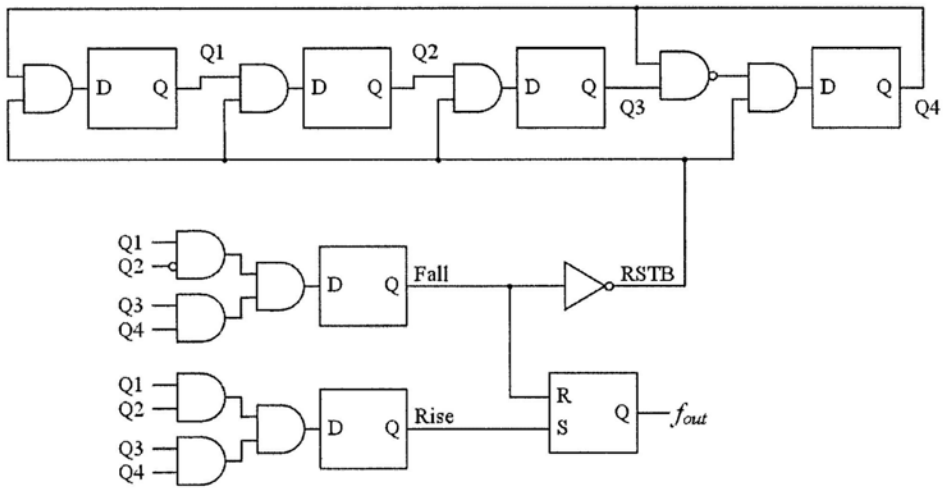


Figure 2.12 Example of a divide-by-5.5 static frequency divider [52]

A dual-modulus prescaler design with fractional division ratio [54] is presented in Figure 2.13. Its structure is similar to the divide-by-2/3 divider cell in [57] and consists of two parts: the prescaler logic to perform frequency division operation and the end-of-cycle logic to select the desired division ratio. The latches are configured as double-edge-triggered flip-flops. In the divide-by-1.5 mode (both MOD and FB_CTRL are Hi), half extra period of the input clock is swallowed by the prescaler logic to perform divide-by-1.5 operation. When either MOD or FB_CTRL is Lo, the output simply tracks the input and the circuit is in the divide-by-1 mode.

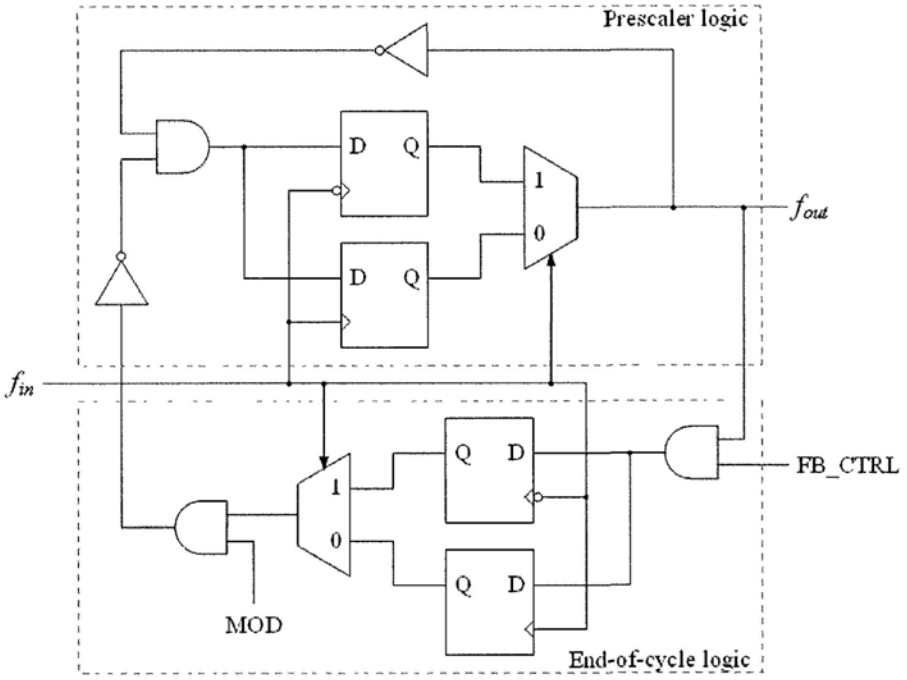


Figure 2.13 Example of a divide-by-1/1.5 dual-modulus static frequency divider [54]

2.3.5 Frequency Synthesizer with Regenerative Frequency Divider

Regenerative frequency dividers are originated from the dynamic Miller frequency divider [58]. Figure 2.14 depicts the general architecture of the regenerative frequency divider with fractional division ratio, which composes of a SSB mixer and frequency dividers. A feedback loop is formed where the divided version of the output is mixed with the input. Under proper phase and gain conditions, the desired frequency component will remain and circulate around the loop [59]. For instance, the output frequency f_{out} can be expressed as:

$$f_{in} \pm \frac{f_{out}}{N} = Mf_{out} \tag{2.6}$$

$$f_{out} = \frac{N}{MN \pm 1} f_{in} \tag{2.7}$$

where plus sign is selected if the lower sideband is chosen while minus sign corresponds to selection of the upper sideband.

The operation frequency of the regenerative frequency divider is considered higher than that of the flip-flop-based static type because the device capacitances can be tuned out by means of resonance with on-chip spiral inductors. Quadrature outputs with symmetric waveforms can also be easily acquired from the regenerative frequency divider outputs, but the SSB mixer mismatches and nonlinearity may generate spurious tones at the output.

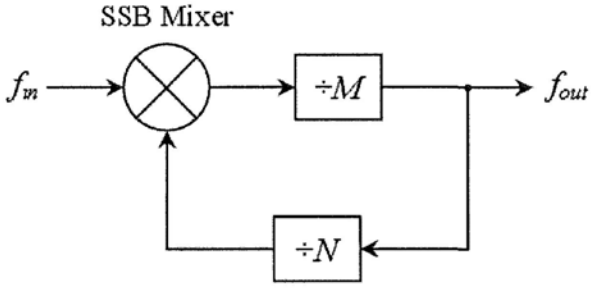


Figure 2.14 Miller frequency divider with fractional division ratio

In [60], a modified Miller frequency divider for fractional division was proposed and its structure is displayed in Figure 2.15. The major difference apart from the conventional ones is the introduction of a mixer in the feedback path, in which the output is first translated by frequency derivation Δf before mixing with the input signal. In this design, there are two possible output frequencies:

$$\begin{aligned} f_{out} &= \frac{f_{in}}{2} \pm \frac{\Delta f}{2} \\ &= \frac{N \pm 1}{2N} f_{in} \end{aligned} \tag{2.8}$$

By adjusting the bandpass filter center frequency, only the frequency component with higher loop gain is sustained in steady state. Unfortunately, the modified Miller divider is inherently suffered from the spur problem even the circuits are ideal and have no mismatches [60]. The mixer in the feedback path always produces two frequency tones at its output. They circulate around the loop and generate unexpected spurs. Those spurs also go around the loop and may sustain in regenerative operation. Therefore, the

selection of division ratio should be careful so that unexpected spurs fall outside the bandpass filter bandwidth.

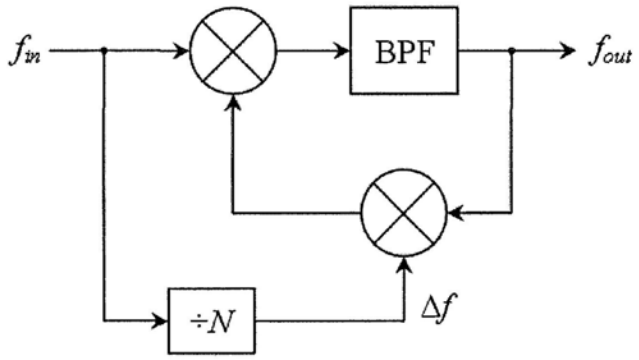


Figure 2.15 Modified Miller frequency divider

Regenerative frequency dividers can be found in various applications, such as fractional LO generation blocks for multi-band GSM [61], multi-band orthogonal frequency division multiplexing (MB-OFDM)-based ultra-wideband (UWB) frequency synthesizers [60], [62]–[64] and reconfigurable quadrature VCOs [65], [66].

2.3.6 Frequency Synthesizer with Phase-Switching Fractional Frequency Divider

Compared with the flip-flop-based static frequency divider, the division modulus control logic is replaced by the phase selection logic in the phase-switching frequency divider. The circuit complexity is relaxed as fewer components working at the full clock rate, which enhances circuitry operation frequency and reduces power consumption. The phase-switching frequency divider structure is presented in Figure. 2.16. Prescaler A, the

only circuit that operates at the full clock rate, generates equally-spaced multi-phase signals. They are then applied to the phase selection circuitry and only one of them is selected to the output for further frequency division in the subsequent stage. Moreover, the modulus control not only determines the phase selection, but also controls the phase swallow process to alter the overall division ratio.

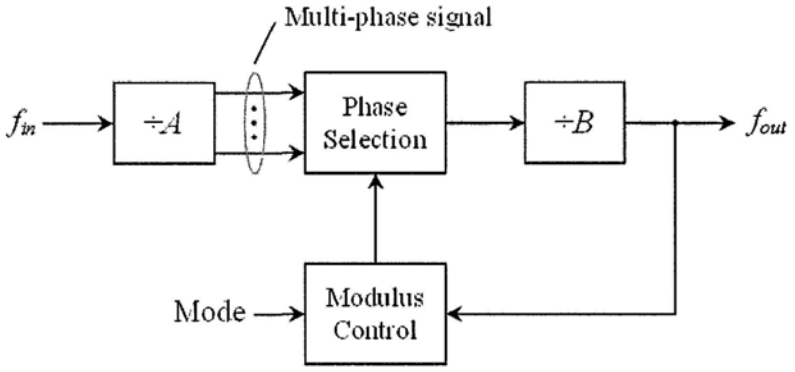


Figure 2.16 Architecture of a phase-switching frequency divider

The overall division ratio can be specified as [9]:

$$N = AB + Ak\frac{\Delta\phi}{360} \tag{2.9}$$

where $\Delta\phi$ is the phase difference between consecutive phase inputs and k is the number of times for phase switching. The minimum division ratio step depends on the prescaler division ratio A and the phase resolution $\Delta\phi$. For example, if A = 2 and $\Delta\phi$ = 90°, fractional division ratio with step size of 0.5 is obtained.

Multi-modulus frequency division is available by controlling the phase-switching occurrence k and the phase selection sequence. There are two possible schemes for phase selection, namely the forward phase selection scheme [67] and the backward phase selection scheme [68]. In the forward phase selection scheme, the rotation sequence is in clockwise direction, i.e. from the originally selected signal to the one that is phase lagging. The resulting signal period extends and thus the overall division ratio increases. On the other hand, opposite rotation direction is employed in the backward phase selection scheme. The overall division ratio decreases since the resulting signal speeds up by the amount of time swallowed in the phase switching operation. Figure 2.17 illustrates an examples of these two selection schemes for fractional resolution of 0.5 with $A = 2$ and $\Delta\phi = 90°$.

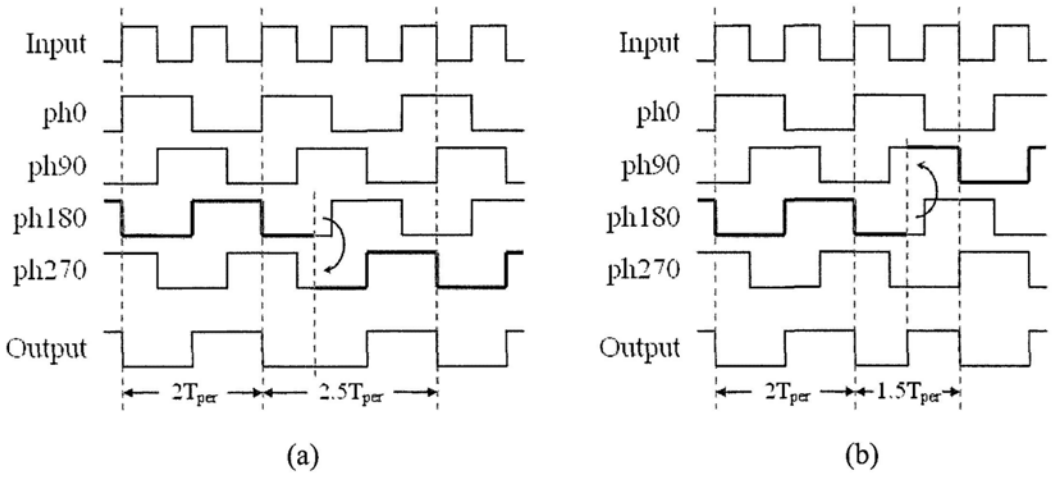


Figure 2.17 Illustration of the phase switching operation with a) forward phase selection scheme and b) backward phase selection scheme

The phase-switching frequency divider with the forward phase selection scheme may suffer from output glitches [67] due to incorrect timing control of phase switching from

one phase to the next. The propagation delay of the modulus control varies over process and temperature variations and hence the appropriate phase transition instant may fall outside the correct timing window [69]. Besides, the backward phase selection scheme does not have glitch problem, but the circuit needs to operate faster during phase transition as the signal period shrinks.

The phase-switching technique is only applicable with multi-phase signal sources. The multi-phase signals can be obtained by using symmetric static frequency dividers (usually divide-by-2 circuits) [9], [70], [71] or directly obtained from quadrature VCOs [72], [73] or ring oscillators [74], [75]. They should be equally spaced; otherwise fractional spurs will be created [76]. Fortunately, this fractional spur problem is not as severe as that in fractional-N PLLs because the divider stage after the phase selection circuit helps to suppress those spurs. Symmetrical layout also improves the phase matching of the multi-phase signals.

2.3.7 Heterodyne Phase-Locked Loop

Figure 2.18 shows the heterodyne PLL architecture [77]. It is similar to the conventional PLL structure, except that the phase frequency detector and charge pump are replaced by a group of mixers in cascade. Consequently, the heterodyne PLL behaves as a type I PLL, which has finite lock range, but fast settling behavior. As traveling along the mixer chain, the input reference frequency f_{ref} is downconverted N times, generating a DC component to control the VCO oscillating frequency while high frequency tones are removed by the lowpass filter.

Fractional division ratio can be acquired by selecting the number of mixer stages and different division ratios for various frequency dividers. The relationship between the output frequency and the reference frequency is expressed as:

$$f_{out} = \frac{M}{\frac{1}{K_1} + \cdots + \frac{1}{K_N}} f_{ref} \tag{2.10}$$

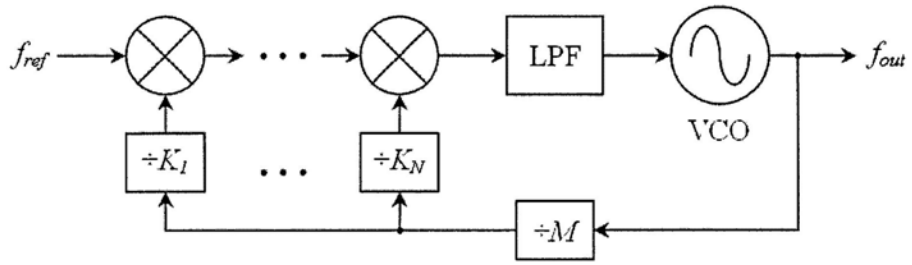


Figure 2.18 Architecture of a heterodyne phase-locked loop

Unlike static frequency dividers realized by flip-flops, no significant speed degradation is found in heterodyne PLLs to provide arbitrary division ratios. However, as the number of mixer stages increases, the loading of the feedback divider limits the tuning range and operation speed.

The spurious responses of the mixers restrict the choice of output frequency and division ratio. Unwanted sidebands produced by each mixer cannot be eliminated completely by the filtering in each mixer stage. Cross-products of harmonics and unwanted sidebands emerge at the lowpass filter input. Spurious tones will appear in the output spectrum and more seriously it may cause false lock. As such, the combinations of hazardous spurious

tones should be considered thoroughly and the VCO tuning range is adjusted to avoid those spurs fall into the desired frequency band. Nevertheless, the safe frequency range becomes narrower as the number of mixer stages increases.

Heterodyne PLLs are targeted for millimeter-wave telecommunication applications. As mentioned in [77], their operation frequency can go up to 100 GHz while static divide-by-2 circuits and Miller frequency dividers only achieve speeds up to a few tens of gigahertz and 50 GHz respectively, in 90 nm and 65 nm CMOS processes.

2.3.8 Summary

Table 2.1 summarizes the advantages and disadvantages of the various approaches for fractional frequency synthesis.

Architecture	Advantages	Disadvantages
Direct digital frequency synthesizer	Fine frequency resolution Low phase jitter Agile frequency switching Transient free frequency changes with phase continuity Availability of direct phase and frequency modulation Excellent temperature and aging stability	Low conversion speed Power hungry
Fractional-N PLL	Fine frequency resolution Fast switching time Good phase noise performance Availability of indirect digital frequency modulation at RF	Fractional spurs problem Complicated modulator structures for high performance
Dual-loop frequency synthesizer	Fine frequency resolution Fast switching time Low in-band phase noise	Two reference sources needed More circuit components
Fractional frequency division using static frequency divider	Systematic design of synchronous divider structure	High power consumption Limited operation frequency due to propagation delay of logic gates
Fractional frequency division using regenerative frequency divider	Availability of quadrature outputs with symmetric waveforms	Possibility of spur problem
Fractional frequency division using phase-switching frequency divider	Simple multi-modulus structure Fewer elements operating at the full clock rate	Demand of multi-phase input Glitch problem Possibility of fractional spur problem
Heterodyne PLL	Fast settling behavior High operation frequency for millimeter-wave applications	Finite lock range Limited operation frequency range and division ratio for spur rejection

Table 2.1 Summary of fractional frequency synthesis architectures

CHAPTER 3

FREQUENCY SYNTHESIZER SYSTEM DESIGN

3.1 Frequency Synthesizer Architecture Description

Figure 3.1 shows the proposed frequency synthesizer structure, which is implemented as a sub-integer-N phase-locked loop (PLL). It composes of a quadrature voltage-controlled oscillator (QVCO), a programmable fractional frequency divider with resolution of 0.5, a phase frequency detector (PFD), two charge pumps (CPs) and a third-order dual-path active loop filter. The proposed PLL supports quadrature-phase outputs, which is indispensable for in-phase and quadrature-phase (IQ) mixing in direct-conversion [78] and low-IF [79] wireless transceiver systems.

The programmable fractional frequency divider is employed with a quadrature-input scheme, which assists to balance the QVCO output loading to maintain good phase quadrature accuracy [80], [81]. As a result, the dummy divider for load matching [66] can

be removed. The proposed frequency divider is designed based on the phase-switching technique to obtain fractional division ratio. The division ratio N ranges from 240.5 to 248 in steps of 0.5. With reference clock frequency f_{ref} of 10 MHz, there are 16 channels covering from 2.405 GHz to 2.48 GHz with a channel spacing of 5 MHz.

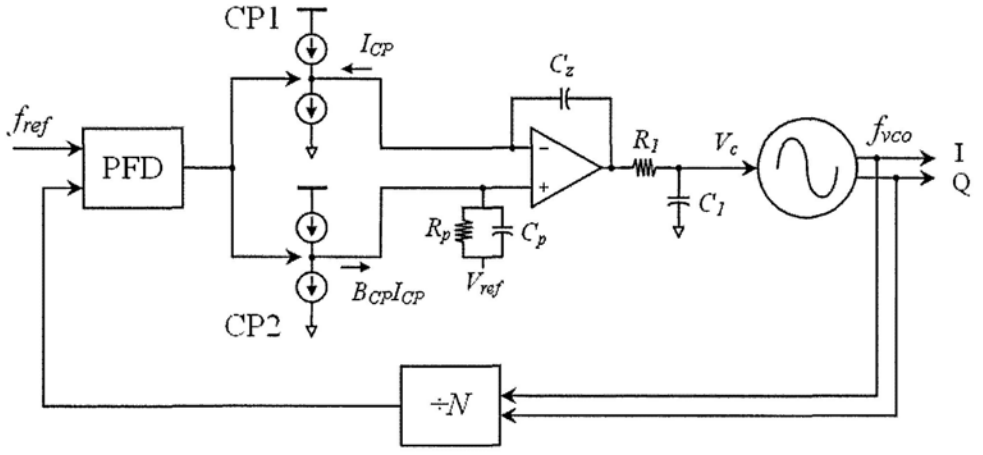


Figure 3.1 Architecture of the proposed phase-locked loop

Several advantages can be beneficial from the proposed fractional frequency synthesis scheme. Since the division ratio resolution becomes less than 1, N can be reduced to cover the same frequency band with the original channel spacing. The PLL in-band phase noise is further suppressed due to decrease of N. Furthermore, f_{ref} increases and the PLL settling time can be speeded up without degrading system stability. The reference spurs are also located further away from the carrier and are attenuated more by the loop filter. The frequency modulation index at the QVCO control voltage node becomes less sensitive due to the adoption of a higher value of f_{ref} [82], resulting in better spurious performance. No unexpected fractional spurious tones arise because the division ratio of

the proposed frequency divider is fixed in each cycle, not a time-varying number determined by delta-sigma modulators in random fashion as in fraction-N PLLs.

In order to minimize the chip area occupied by the loop filter capacitors, the dual-path loop filter [83] is introduced. Usually the capacitor used to create the compensation zero has the largest size, which is difficult for on-chip integration. By using the dual-path loop filter, the compensation zero is implemented not by an actual *RC* configuration, but by signal combination. The two charge pump current outputs are first manipulated by different transfer characteristics and finally summed up to produce the desired compensation zero. Its operation principle is illustrated in Figure 3.2.

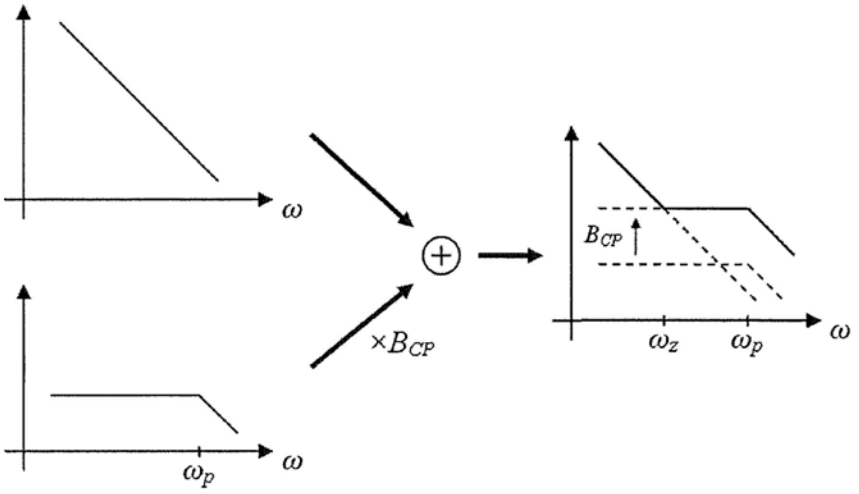


Figure 3.2 Dual-path loop filter principle

Current injected at the opamp inverted input terminal charges the feedback capacitor C_z, functioning as an integrator. It corresponds to a single-pole system with a pole at zero frequency. Moreover, current inputted to the opamp non-inverted input terminal is

lowpass filtered by the combination of R_p and C_p. The opamp acts as a summer and the resultant transfer characteristic contains a zero whose location is at the intersection of the two processed signals. Since the lowpass filtered signal amplitude can be controlled by the charge pump current factor B_{CP}, the compensation zero location is adjustable. It can be realized without a large capacitor as its time constant gains from multiplication by the factor B_{CP}. As a tradeoff, additional noise is induced by the opamp, which is the main drawback of using the active loop filter topology.

The QVCO is designed with small VCO gain, not only for low phase noise and good spurious performance, but also for size scaling of the loop filter components. For smaller VCO gain, noise contributions of the resistors in the loop filter decrease. As a result, their resistances can be increased while the capacitors in the loop filter reduce proportionally to keep the pole and zero locations unaltered for loop stability.

The proposed frequency synthesizer is designed to fulfill the IEEE 802.11b/g standards. As specified, the time to change from one operating channel frequency to another is 224 μs within frequency tolerance of ±60 kHz. The spurious components within and beyond 1 GHz frequency offset should be below -57 dBm and -47 dBm respectively. The phase noise specification is derived based on the assumptions of an adjacent interferer of 35 dBc and signal-to-noise ratio (SNR) of 26.5 dB [79] for a bit error rate (BER) of 10^{-6} in 64-QAM modulation, as:

$$L\{25MHz\} = -35 - 10\log(25M) - 26.5 = -135.5 \text{ dBc/Hz} \tag{3.1}$$

By assuming a $1/f^2$ phase noise spectrum, it corresponds to -107.5 dBc/Hz at 1 MHz frequency offset.

3.2 Frequency Synthesizer Behavior Simulations

3.2.1 Linear Model Description

Figure 3.3 depicts the linear model of the proposed PLL, which is a closed loop system with negative feedback. The transfer functions of the individual components can be found in Figure 3.3. The PFD and charge pumps are combined and represented as a gain stage with a phase-to-voltage conversion factor of $I_{CP}/2\pi$. Due to transformation from frequency to phase, the VCO acts as an integrator with conversion gain of K_{VCO}. The frequency divider, a gain stage of division by N, reduces the output phase Φ_{vco} by N times for comparison with the reference phase Φ_{ref}. In equilibrium, they should be equal. The loop filter demonstrates lowpass characteristic and contains three poles and one zero. The zero is essential for frequency compensation because the system contains two poles at zero frequency, contributed by the loop filter and the VCO respectively.

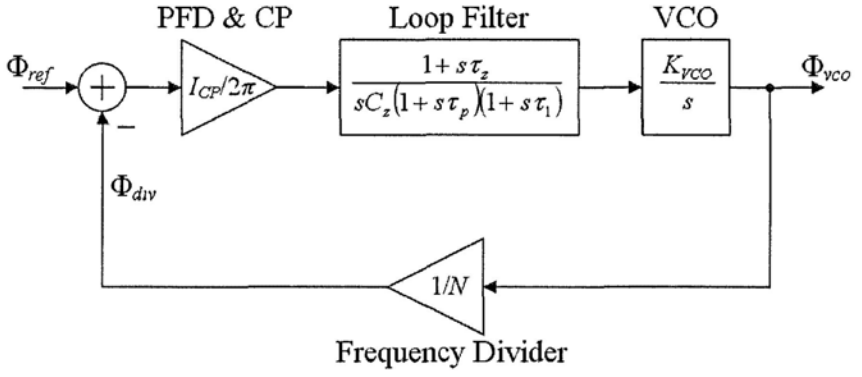


Figure 3.3 Linear model of the proposed PLL

The open loop transfer function of the PLL system is given by:

$$G_{loop}(s)=\frac{\Phi_{div}}{\Phi_{ref}}=\frac{I_{CP}K_{VCO}}{2\pi NC_z}\cdot\frac{1+s\tau_z}{s^2(1+s\tau_p)(1+s\tau_1)} \tag{3.2}$$

where $\tau_z=R_p(C_p+B_{CP}C_z)$, $\tau_p=R_pC_p$ and $\tau_1=R_1C_1$

Hence its closed loop transfer function can be derived as:

$$H_{PLL}(s)=\frac{\Phi_{vco}}{\Phi_{ref}}=\frac{NG_{loop}(s)}{1+G_{loop}(s)} \tag{3.3}$$

It can be observed that the system exhibits lowpass characteristic. At low frequency, the input signal is amplified by a factor of N while high frequency signals are attenuated as $\lim_{s\to\infty} G_{loop}(s)=0$.

Since the proposed PLL belongs to a type-II system, there is no steady-state phase error. The phase error is defined as $\Phi_\varepsilon = \Phi_{ref} - \Phi_{div}$ and its transfer function is expressed as:

$$\frac{\Phi_\varepsilon}{\Phi_{ref}} = \frac{1}{1+G_{loop}(s)} \tag{3.4}$$

With a frequency step applied to the PLL input, the input phase signal shows a linear ramp dependence $\Phi_{ref}(s) = \Delta\omega / s^2$. By using the final-value theorem of Laplace transform (i.e. $\lim_{t\to\infty} \Phi_\varepsilon(t) = \lim_{s\to 0} s\Phi_\varepsilon(s)$), the steady-state phase error turns out to be zero.

3.2.2 Stability Analysis

According to Equation 3.2, the open loop transfer function of the PLL system contains one zero and four poles, where two of them are at zero frequency. These two poles contribute 180° phase shift to the feedback signal and cause instability when there is no compensation zero. For sake of stability, the compensation zero $\omega_z = 1/\tau_z$ is placed before the other two poles ($\omega_p = 1/\tau_p$ and $\omega_1 = 1/\tau_1$) to contribute sufficient phase lead.

Figure 3.4 presents the bode plot of the PLL system with asymptotic approximation. Since the pole at ω_1 is mainly introduced for spur and noise suppression, it is usually far away from the crossover frequency ω_c and has little influence on the phase margin (PM). Eventually, the crossover frequency and phase margin of the PLL system are determined

by the locations of the pole-zero pair ω_z and ω_p. The farther the separation of ω_z and ω_p, the better the phase margin with a maximum value of 90°.

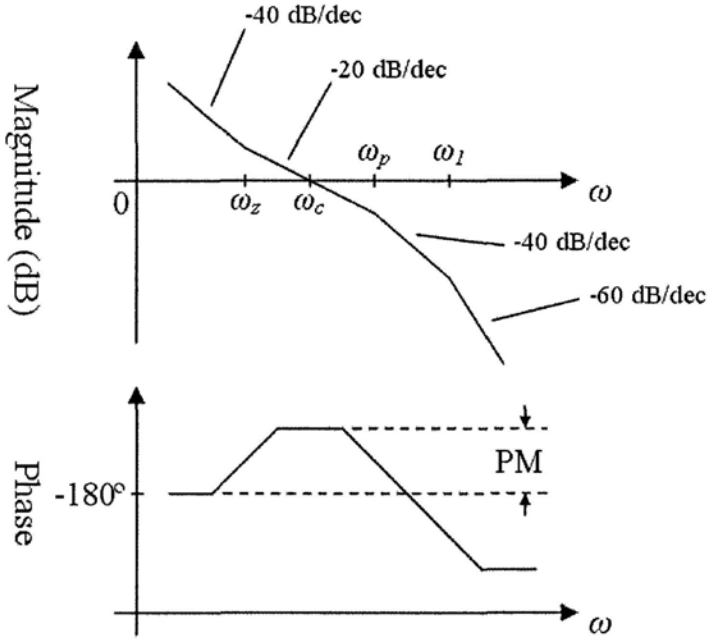


Figure 3.4 Bode plot of the PLL system with asymptotic approximation

The crossover frequency ω_c can be found from the condition $\left|G_{loop}(j\omega_c)\right|=1$, that is:

$$\left|G_{loop}(j\omega_c)\right| = \frac{I_{CP}K_{VCO}}{2\pi N\omega_c^2 C_z}\cdot\sqrt{\frac{1+\omega_c^2\tau_z^2}{(1+\omega_c^2\tau_p^2)(1+\omega_c^2\tau_1^2)}}=1 \tag{3.5}$$

Assume $\omega_c \ll \frac{1}{\tau_p} \ll \frac{1}{\tau_1}$ and $\omega_c \gg \frac{1}{\tau_z}$, Equation 3.5 can be approximated as:

$$\frac{I_{CP}K_{VCO}}{2\pi N\omega_c^2 C_z}\cdot\omega_c\tau_z \approx 1$$

Finally,
$$\omega_c \approx \frac{I_{CP}K_{VCO}R_pB_{CP}}{2\pi N} \tag{3.6}$$

The phase of the open loop transfer function $G_{loop}(s)$ is denoted as:

$$\begin{aligned}\arg\left[G_{loop}(j\omega)\right] &= -\pi + \arg(1+j\omega\tau_z) - \arg(1+j\omega\tau_p) - \arg(1+j\omega\tau_1)\\ &= -\pi + \arctan(\omega\tau_z) - \arctan(\omega\tau_p) - \arctan(\omega\tau_1)\end{aligned} \tag{3.7}$$

Generally, the crossover frequency ω_c is chosen at the frequency with respect to the maximum phase margin for specified pole-zero locations. It can be determined from the zero derivative point in the phase response. By differentiation of Equation 3.7 and equating the resulting expression to zero, it obtains:

$$\frac{d}{d\omega}\arg\left[G_{loop}(j\omega_c)\right] = \frac{\tau_z}{1+\omega_c^2\tau_z^2} - \frac{\tau_p}{1+\omega_c^2\tau_p^2} - \frac{\tau_1}{1+\omega_c^2\tau_1^2} = 0 \tag{3.8}$$

Since the pole at ω_1 has little phase shift contribution at the crossover frequency ω_c, the last term is neglected. As a result, it leads to the conclusion that the crossover frequency for optimum phase margin should be chosen as the geometrical mean of ω_z and ω_p, that is:

$$\omega_c = \frac{1}{\sqrt{\tau_z\tau_p}} \tag{3.9}$$

Defining pole-zero separation $b = \frac{\tau_z}{\tau_p} > 1$, ω_z and ω_p can be expressed as:

$$\begin{aligned} \omega_z &= \frac{\omega_c}{\sqrt{b}} \\ \omega_p &= \sqrt{b}\omega_c \end{aligned} \tag{3.10}$$

From Equation 3.6 and 3.10, the loop filter components R_p, C_z and C_p can be calculated as:

$$\begin{aligned} R_p &= \frac{2\pi N \omega_c}{I_{CP} K_{VCO} B_{CP}} \\ C_z &= \frac{I_{CP} K_{VCO} \sqrt{b}}{2\pi N \omega_c^2} \\ C_p &= \frac{I_{CP} K_{VCO} B_{CP}}{2\pi N \sqrt{b} \omega_c^2} \end{aligned} \tag{3.11}$$

Selection of component values R_1 and C_1 is less strict as long as the pole location ω_1 is not close to the crossover frequency ω_c, degrading system stability. To minimize C_1, R_1 should be maximized unless its noise contribution becomes significant.

The relationship between the phase margin and pole-zero separation exhibits parabolic characteristic, as displayed in Figure 3.5. Wide pole-zero separation does not gain much improvement on the phase margin, but requires huge component values to implement the compensation zero with a large time constant. Separation of 10 to 20 times is appropriate to obtain good phase margin of around 60°.

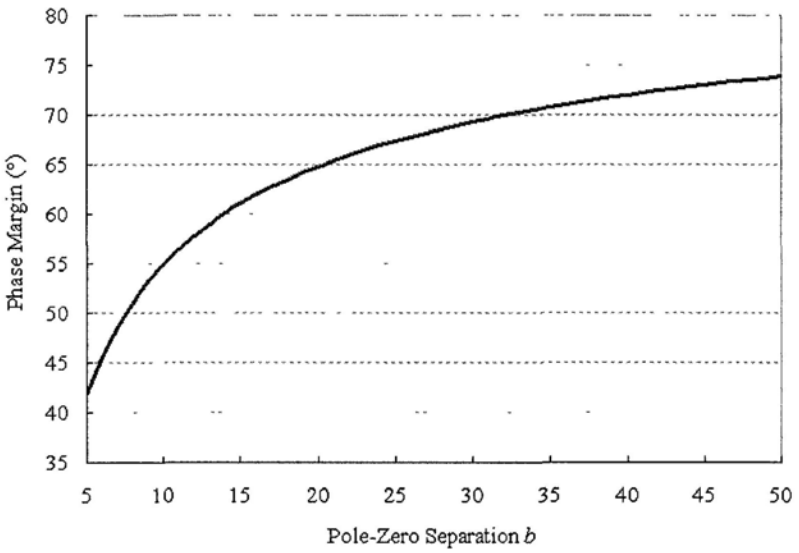


Figure 3.5 Relationship between the phase margin and pole-zero separation

For instance, with pole-zero separation of 12, the predicted phase margin is 57.8°. If the desired crossover frequency ω_c is selected as 60 kHz, the pole-zero pair at ω_z and ω_p is determined at 17.3 kHz and 207.8 kHz respectively. Additionally, the pole at ω_1 is placed two octaves away from the pole at ω_p and hence located at 831.4 kHz. Since it is more than one decade away from ω_c, it has little effect on the phase margin.

Based on the parameters K_{VCO} = 120 MHz/V, I_{CP} = 1 μA, B_{CP} = 24 and N = 248, the resistance and capacitance values of the loop filter components can be calculated, as summarized in Table 3.1. The resistance R_1 is chosen to be four times less than that of R_p and the capacitances C_p and C_1 have same size.

Component Parameter	Value
R_p	32.5 kΩ
C_p	23.6 pF
C_z	11.8 pF
R_1	8.1 kΩ
C_1	23.6 pF

Table 3.1 Component values of the loop filter elements

The open loop transfer characteristic of the PLL system is plotted in Figure 3.6. At low frequency, the trend of -40 dB/decade can be observed in the magnitude plot and the phase shift starts at -180° caused by the two poles at zero frequency, as expected. Meanwhile, the introduction of the compensation zero decreases the slope of decline in the magnitude plot and induces phase advance for stability as shown in the phase plot. The simulated crossover frequency and phase margin are 64 kHz and 54.6° respectively. The discrepancy is due to the approximations used in deriving the formulas and the influence of the additional pole at ω_1. At high frequency, the magnitude response decays at a rate of 60 dB/decade and the phase shift finally settles to 90° (or equivalently -270°).

Figure 3.7 shows the closed loop response of the PLL system, which exhibits lowpass behavior. There is a gain of 47.9 dB, corresponded to $N = 248$. The 3-dB bandwidth is around 112 kHz and the overshoot is less than 1.8 dB. Furthermore, the rolloff in the stopband acquires attenuation of 60 dB/decade.

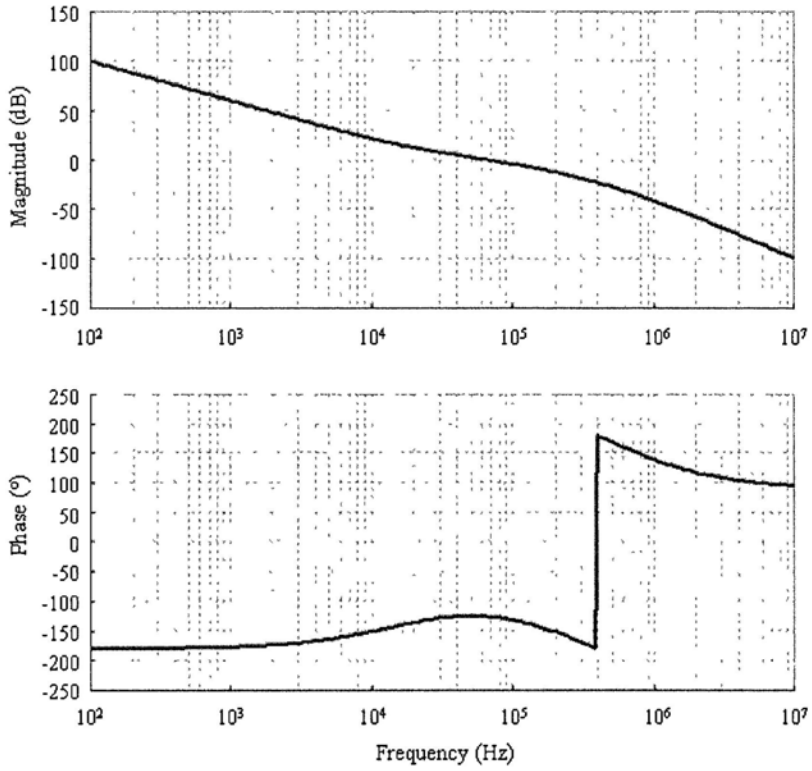


Figure 3.6 Open loop transfer characteristic of the PLL system

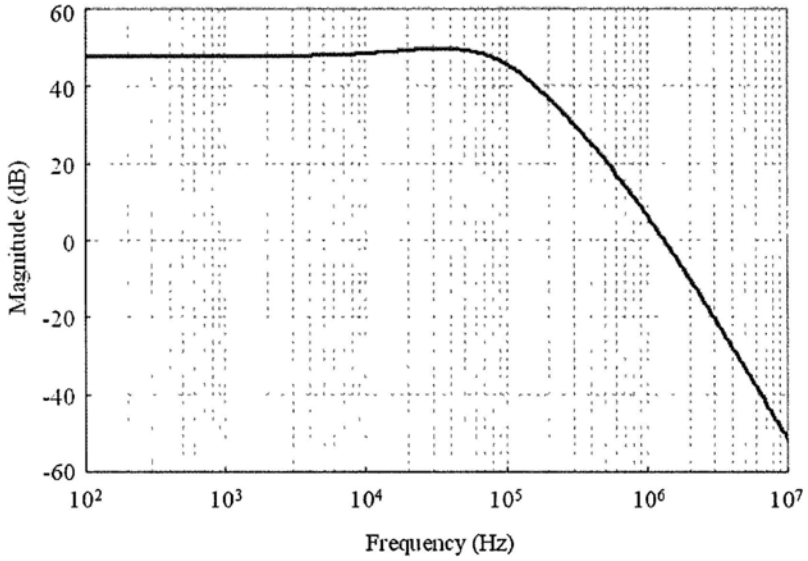


Figure 3.7 Closed loop transfer characteristic of the PLL system

3.2.3 Phase Noise Contribution

Figure 3.8 depicts the noise model of the PLL system. There are six noise sources, including the phase noise of the reference clock, PFD and frequency divider, the current noise of the charge pumps, the voltage noise of the loop filter and the phase noise of the free-running VCO. The overall phase noise of the PLL system is then the summation of all noise source contributions, modified by their individual noise transfer functions due to the feedback operation upon them.

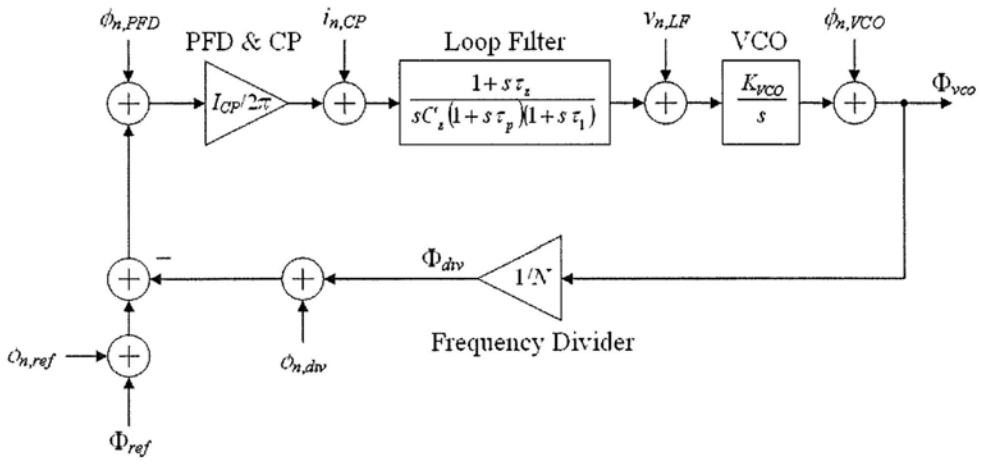


Figure 3.8 Noise model of the PLL system

The noise transfer function for the noise sources of the reference clock, PFD and frequency divider is the closed loop transfer function of the PLL system ($H_{PLL}(s)$ in Equation 3.3 and in Figure 3.7), exhibiting lowpass characteristic. Their noise contributions are dominated at low frequency offset and amplified by a factor of N^2. At high frequency offset, they are significantly suppressed. In this design, there is attenuation of 60 dB/decade in stopband. As such, narrow loop bandwidth can help to

filter out more noise with the tradeoff of slow settling time. For noise reduction, clean reference clock can be generated by using a good quality crystal while the time jitter due to logic transitions in the PFD and frequency divider can be minimized with fast transition.

In contrast, as shown in Figure 3.9, highpass behavior is observed in the noise transfer function for the VCO noise source. It is expressed as:

$$H_{n,VCO}(s)=\frac{1}{1+G_{loop}(s)} \tag{3.12}$$

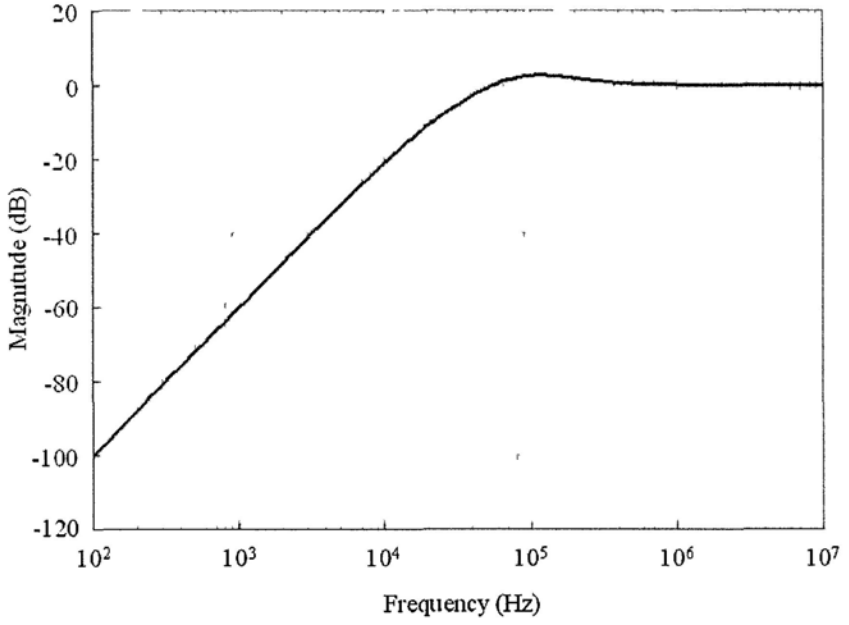


Figure 3.9 Noise transfer function for the VCO noise source

At high frequency offset, the phase noise of the free-running VCO is unfiltered as $\lim_{s\to\infty} G_{loop}(s)=0$. The phase noise contributed by $1/f$ flicker noise upconversion at low

frequency offset is greatly suppressed. According to Equation 3.12, the cutoff frequency of the VCO noise transfer function depends on the crossover frequency of the open loop transfer function $G_{loop}(s)$. High crossover frequency is desirable for better attenuation of phase noise contributed by the VCO, but wide closed loop bandwidth results and leads to degradation of the in-band phase noise performance.

In this design, the charge pump noise contribution consists of two parts because two charge pumps are used in the dual-path loop filter topology for the compensation zero formation. Current noise is generated for each charge pump and shaped by different noise transfer function. These two noise transfer functions are listed in Equation 3.13 and 3.14 respectively.

$$H_{n,CP1}(s) = \frac{1}{sC_z} \cdot \frac{1}{1+s\tau_1} \cdot \frac{K_{VCO}}{s} \frac{1}{1+G_{loop}(s)} \tag{3.13}$$

$$H_{n,CP2}(s) = \frac{R_p}{1+s\tau_p} \cdot \frac{1}{1+s\tau_1} \cdot \frac{K_{VCO}}{s} \frac{1}{1+G_{loop}(s)} \tag{3.14}$$

The pole-zero locations for these two noise transfer functions have one major difference. For the charge pump CP1, since its current is injected to an integrator, an extra pole at zero frequency is included in its noise transfer function. Moreover, it is replaced by a real pole with time constant τ_p in the noise transfer function of CP2. The noise transfer function of CP1 exhibits lowpass characteristic while that of CP2 behaves like a bandpass filter, as illustrated in Figure 3.10.

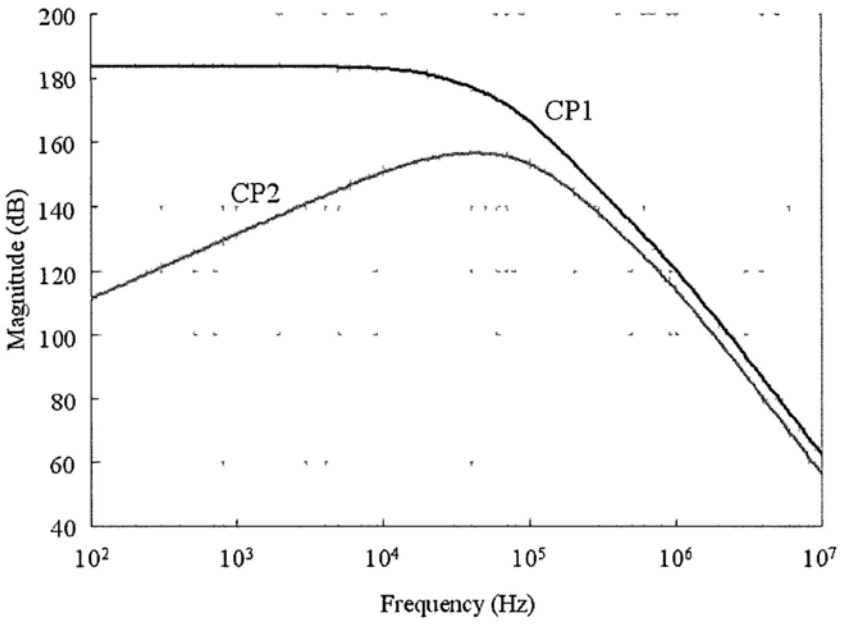


Figure 3.10 Noise transfer functions for the charge pump noise sources

At low frequency offset, the charge pump CP2 generates less noise than CP1 as its noise is filtered out. Both noise contributions at large frequency offset are greatly suppressed with rolloff of 60 dB/decade. Although the magnitude of CP1 noise transfer function is higher than that of CP2 at large frequency offset, the overall noise power contributed by CP2 is greater because the current in CP2 is amplified by a factor of B_{CP}. The charge pump noise transfer functions at large frequency offset can be approximated as:

$$H_{n,CP1}(\Delta\omega) \approx \frac{8\pi N}{I_{CP}} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^3 \tag{3.15}$$

$$H_{n,CP2}(\Delta\omega) \approx \frac{8\pi N b}{I_{CP} B_{CP}} \cdot \left(\frac{\omega_c}{\Delta\omega}\right)^3 \tag{3.16}$$

It can be seen that there is a factor of b/B_{CP} different from these two noise transfer functions. Since CP2 produces B_{CP} times more noise than CP1, the noise power contributed by CP2 is b^2/B_{CP} times greater at large frequency offset.

The current noise generated by a charge pump can be estimated as [50]

$$di_n^2 = 2\lambda_{on} \cdot 4kT \cdot g_m \cdot df \tag{3.17}$$

where k is the Boltzmann constant, T is the absolute temperature, λ_{on} is the turn-on duty cycle of the charge pump and g_m is the transconductance of the current source.

As suggested in Equation 3.17, the current noise can be reduced by decreasing λ_{on} and g_m. It should be cautious that the purpose of λ_{on} is to avoid the PFD dead zone degrading the PLL in-band performance. Therefore, for current noise suppression, it should be kept short, but long enough to ensure the dead zone removal. Increase of overdrive voltage with small aspect ratio W/L results in small transconductance and so as current noise. However, this shrinks the VCO tuning range as higher voltage headroom is needed for the current source transistors remained in saturation. On the other hand, large transistor sizes are preferable for minimizing their flicker noise contribution and current mismatches.

There are three noise sources in the loop filter, which are the equivalent output voltage noise of opamp and the thermal noise of the resistors R_p and R_1. The noise generated by

the resistor R_p has same noise transfer function as that of the charge pump CP2 (as stated in Equation 3.14) while the noise transfer function for the other two noise sources is given as:

$$H_{n,amp}(s) = \frac{1}{1+s\tau_1} \cdot \frac{K_{VCO}}{s} \frac{1}{1+G_{loop}(s)} \tag{3.18}$$

whose magnitude response is plotted in Figure 3.11.

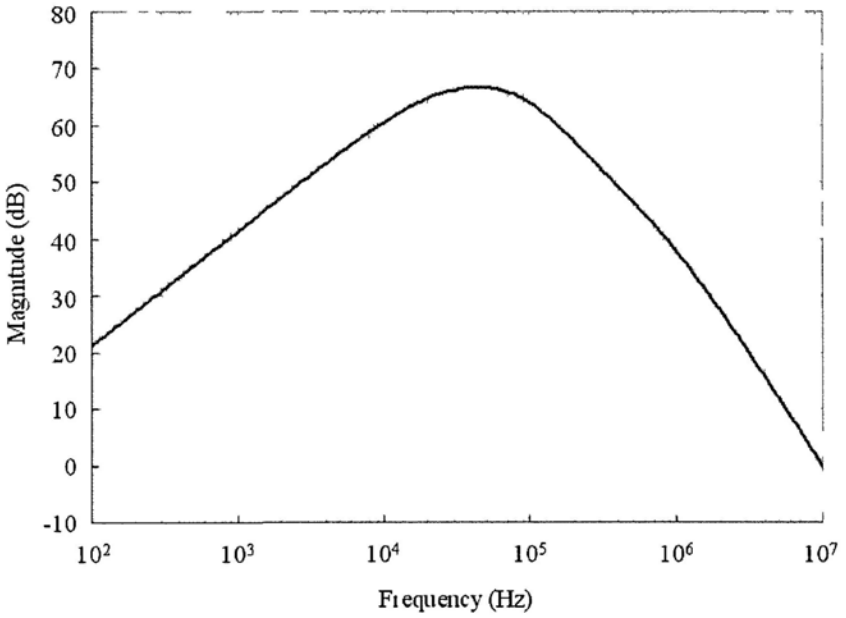


Figure 3.11 Noise transfer function for the equivalent noise source of the amplifier in the loop filter

All three noise sources of the loop filter are manipulated with bandpass filtering characteristic. Attenuation of 20 dB/decade is obtained at low frequency offset. At large frequency offset, thermal noise contributed by the resistor R_p acquires additional 20 dB suppression per decade when compared with other two noise sources. As such, the

noise specifications of the opamp and resistor R_1 are more stringent. Thermal noise contributed by the resistor R_1 can be decreased by using small resistance value, but a large capacitance size is required to keep the pole location unaltered. In general, the opamp noise can be reduced by increasing the transconductance of the differential pair with the drawback of high power consumption. The flicker noise can be effectively suppressed by using large transistor sizes.

As a summary, the estimated phase noise of the PLL system is presented in Figure 3.12, including the noise contribution of each component at the PLL output. The in-band phase noise is -70.9 dBc/Hz, which is dominated by the charge pump noise. Lowpass characteristic for noise filtering of the charge pump, reference clock, PFD and frequency divider can be observed in Figure 3.12. Besides, at large frequency offset (> 5 MHz), the overall PLL phase noise performance is solely determined by that of VCO as its phase noise is unfiltered.

At intermediate frequency offset, the phase noise contributed by the loop filter becomes significant and takes over the dominant noise contributor from the charge pump at around 300 kHz. Its bandpass behavior can be identified and provides noise suppression of 40 dB/decade at large frequency offset. At 1 MHz frequency offset, the total phase noise is -115.3 dBc/Hz, which is mainly contributed by the loop filter and VCO. There is around 10 dB margin from other noise contributors.

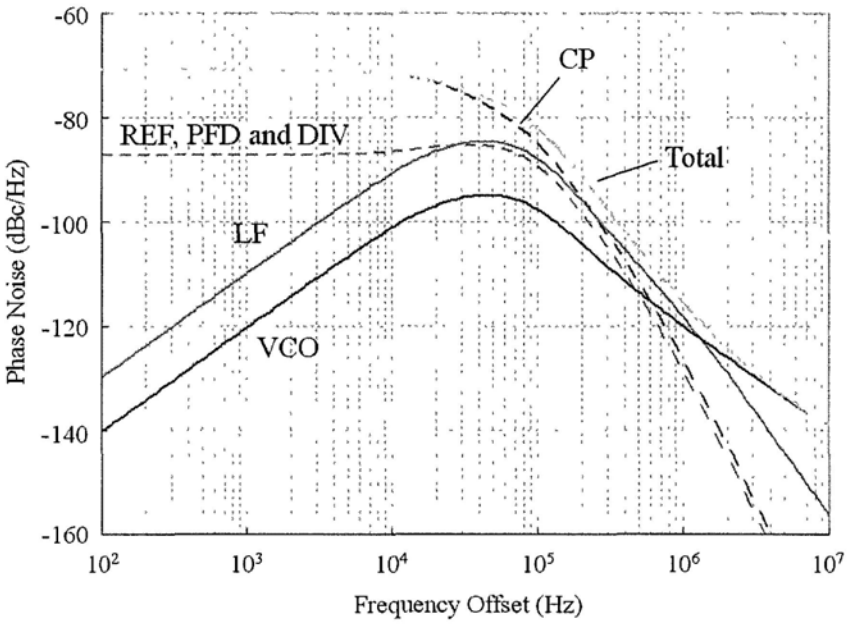


Figure 3.12 Estimated overall PLL phase noise and contribution of each component at the PLL output

3.2.4 Settling Time

As stated in [14], the settling time for Type-II, third-order PLL-based frequency synthesizers can be estimated as:

$$t_{sett} = \frac{\ln\left(f_{step} / f_{error}\right)}{f_c \cdot \xi_e(\phi_m)} \tag{3.19}$$

where

f_c	the crossover frequency
f_{step}	the amplitude of frequency jump
f_{error}	the maximum frequency error at t_{sett}
ϕ_m	the phase margin
$\xi_e(\phi_m)$	the effective damping coefficient at a specified phase margin

For defined frequency error tolerance, fast settling time depends on both crossover frequency and phase margin of the PLL system. Direct consequence of increasing crossover frequency leads to reduction of settling time. Nonetheless, the choice of phase margin affects the pole-zero locations of the PLL system. Low phase margin leads to introduction of complex conjugate poles close to the imaginary axis of *s*-plane, which results in strong oscillatory behavior when transiting to final value and hence slow settling time. Moreover, high phase margin is also not preferable. As demonstrated in [14], the settling time almost doubles when the phase margin changes from 50° to 60° and the optimum phase margin for shortest settling time is 51°.

Although the proposed PLL system is Type-II, fourth order, it can be approximated as a Type-II, third order system because the additional pole is located far from the crossover frequency. The crossover frequency and the phase margin of the proposed PLL system are 64 kHz and 54.6° respectively while the effective damping coefficient can be found in [14] as 3.5. For a frequency change of 80 MHz with maximum frequency error of ±60 kHz, the estimated settling time is calculated as 32.1 μs, which is much smaller than the specification of 224 μs for the IEEE 802.11 WLAN communication systems.

Figure 3.13 depicts the simulated settling time characteristic of the proposed PLL system. It can be seen that the settling transient shows no oscillatory behavior and the overshoot is limited to 20 MHz. The simulated settling time is 41.4 μs. The discrepancy may be concluded as the linear continuous-time approximation of the PLL discrete-time nature and the introduction of the additional pole in the transfer function.

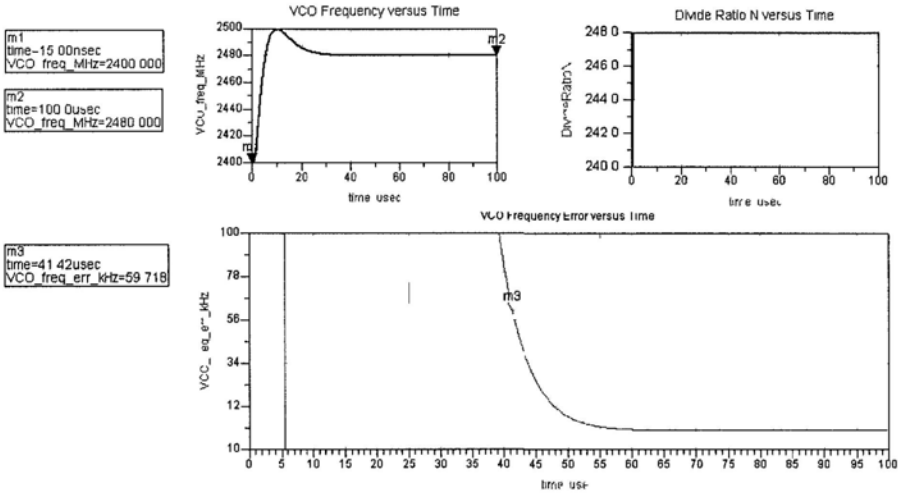


Figure 3.13 Settling time simulation result

3.2.5 Summary of Design Parameters and System Performances

The component values of the proposed PLL and its system performances are listed in Table 3.2 and Table 3.3 respectively.

Component Parameter	Value
K_{VCO}	120 MHz/V
I_{CP}	1 μA
B_{CP}	24
R_p	32.5 kΩ
C_p	23.6 pF
C_z	11.8 pF
R_1	8.1 kΩ
C_1	23.6 pF

Table 3.2 Component parameters of the proposed PLL

System Performances	Value
Crossover frequency	64 kHz
Phase margin	54.6°
Closed loop bandwidth	112 kHz
In-band phase noise	-70.9 dBc/Hz
Phase noise at 1 MHz frequency offset	-115.3 dBc/Hz
Settling time	41.4 μs

Table 3.3 Performance summary of the proposed PLL

3.3 Frequency Synthesizer Spurious Tone Analysis

3.3.1 Spur Generation Mechanism

Spurs emerged in the PLL output spectrum are caused by the frequency modulation (FM) of the VCO control signal. The VCO is an intrinsic voltage-to-frequency converter and its output signal can be expressed as:

$$V_0(t) = A\cos\left[2\pi f_0 t + 2\pi K_{VCO}\int_{-\infty} s(\lambda)d\lambda\right] \tag{3.20}$$

where f_0 is the center frequency of the carrier, K_{VCO} is the VCO gain and $s(t)$ is the input signal at the VCO control node.

For instance, suppose that $s(t)$ is a sinusoid signal with amplitude of ΔV_{peak} and frequency of f_m, the VCO output signal $V_0(t)$ becomes:

$$\begin{aligned} V_0(t) &= A\cos[2\pi f_0 t + \beta\sin(2\pi f_m t)] \\ &= A\cos(2\pi f_0 t)\cos[\beta\sin(2\pi f_m t)] - A\sin(2\pi f_0 t)\sin[\beta\sin(2\pi f_m t)] \end{aligned} \tag{3.21}$$

where $\beta = \dfrac{K_{VCO}\Delta V_{peak}}{f_m} = \dfrac{\Delta f_{peak}}{f_m}$ is the frequency modulation index

Assuming narrowband FM (β « 1), it can be simplified as:

$$V_0(t) \approx A\cos(2\pi f_0 t) - \frac{\beta A}{2}\cos[2\pi(f_0 - f_m)t] - \frac{\beta A}{2}\cos[2\pi(f_0 + f_m)t] \tag{3.22}$$

As observed in Equation 3.22, in addition to the main carrier tone at f_0, there are two spurious tones located at frequency offsets of $\pm f_m$ apart from the carrier. Hence, the single sideband-to-carrier ratio can be defined as:

$$\text{Single sideband-to-carrier ratio (dBc)} = 20\log\frac{\beta}{2} = 20\log\left(\frac{K_{VCO}\Delta V_{peak}}{2f_m}\right) \tag{3.23}$$

Equation 3.23 implies that the spur magnitude can be attenuated by decreasing K_{VCO} or by increasing f_m.

3.3.2 Spurs due to Reference Feedthrough

For integer-N PLLs, phase comparison operates at a rate equal to the reference frequency f_{ref}. When locked, the rising edges of the two input clock signals at the PFD are synchronous and therefore the net current supplied by the charge pump to the loop filter is zero, leading to a constant VCO control voltage. However, in real world, mismatches exist and cause net charge to be injected into the loop filter, changing the VCO control voltage. As a result, reference spurs appear at frequency offsets equal to integer multiples of $\pm f_{ref}$ from the carrier. There are three main sources that induce reference spurs [84], namely:

- Leakage current, including those caused by the charge pump itself, varactors and any leakage in the substrate
- Mismatch between the charge pump up and down current sources
- Timing mismatch in the PFD

Among them, the current mismatch in the charge pump is usually the most important factor. Figure 3.14 demonstrates the effect of charge pump current mismatch when the PLL stays in lock. In order to ensure zero net charge inputted to the loop filter, the frequency divider output signal f_{div} is shifted by time Δt_s and no longer aligned with the reference clock signal f_{ref} in steady state. Not only phase error exists, but also current pulses at rate of f_{ref} are injected into the loop filter, causing periodic disturbance on the VCO control voltage. It is then frequency modulated and appears as spurious tones in the PLL output spectrum.

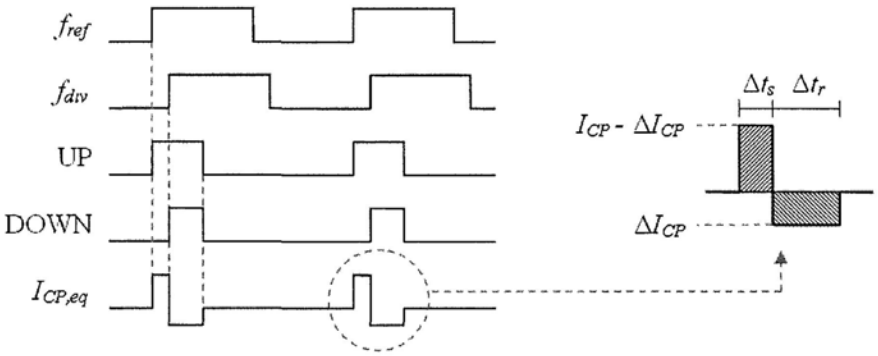


Figure 3.14 Effect of charge pump current mismatch in PLL steady state condition

The amplitude of the frequency component at f_{ref} for the net charge pump current $I_{CP,eq}$ can be yielded by finding the corresponding Fourier series coefficient:

$$\begin{aligned}\Delta i_{peak} &= \frac{2}{T_{ref}}\left|\int_0^{T_{ref}} I_{CP,eq}(t)e^{-j2\pi f_{ref}t}dt\right| \\ &= \frac{2}{T_{ref}}\left|\left[\int_0^{\Delta t_s}(I_{CP}-\Delta I_{CP})e^{-j2\pi f_{ref}t}dt - \int_{\Delta t_s}^{\Delta t_s+\Delta t_r}\Delta I_{CP}e^{-j2\pi f_{ref}t}dt\right]\right|\end{aligned} \tag{3.24}$$

For zero net charge injection, the following condition $(I_{CP}-\Delta I_{CP})\Delta t_s = \Delta I_{CP}\Delta t_r$ holds for equal amount of positive and negative charges. Δt_r is the charge pump minimum turn-on time and the charge pump turn-on duty cycle λ_{on} is equal to $\frac{\Delta t_r}{T_{ref}}$. For small charge pump current mismatch and short charge pump turn-on duty cycle, Equation 3.24 can be simplified as:

$$\Delta i_{peak} \approx 2\pi \cdot \Delta I_{CP} \cdot \lambda_{on}^2 \tag{3.25}$$

Equation 3.25 implies that, as well as minimizing the charge pump current mismatch, reducing the charge pump turn-on duty cycle is more effective for diminishing the spurious signal magnitude. As recalled, shortening the turn-on duty cycle is also beneficial for suppressing charge pump noise contribution at the PLL output, but elimination of the PFD dead zone must be guaranteed.

The signal amplitude ΔV_{peak} that disturbs the VCO control voltage can be found by multiplying the current mismatch amplitude Δi_{peak} by the loop filter transfer function $H_{LF}(s)$, which is given as:

$$H_{LF}(s)=\frac{1+s\tau_z}{sC_z(1+s\tau_p)(1+s\tau_1)} \tag{3.26}$$

Since the spurious components at f_{ref} are at much higher frequency than the poles and zero in the loop filter transfer function, the magnitude of loop filter transfer function at f_{ref} can be approximated as:

$$\begin{aligned}\left|H_{LF}(j2\pi f_{ref})\right| &\approx \frac{f_{ref}/f_z}{2\pi f_{ref}C_z \cdot f_{ref}/f_p \cdot f_{ref}/f_1} \\ &\approx B_{CP}R_p \cdot \frac{f_p}{f_{ref}} \cdot \frac{f_1}{f_{ref}}\end{aligned} \tag{3.27}$$

Finally, the spur suppression is expressed as:

$$\begin{aligned}\text{Spur suppression} &= -20\log\left(\frac{K_{VCO}\Delta i_{peak}\left|H_{LF}\left(j2\pi f_{ref}\right)\right|}{2f_{ref}}\right) \\ &= -20\log\left(\frac{\pi\Delta I_{CP}\lambda_{on}^2 K_{VCO}B_{CP}R_p}{f_{ref}}\right) - 20\log\left(\frac{f_p}{f_{ref}}\cdot\frac{f_1}{f_{ref}}\right)\end{aligned} \tag{3.28}$$

It can be observed that decreasing the VCO gain K_{VCO}, charge pump current mismatch ΔI_{CP} and charge pump turn-on duty cycle λ_{on} are the rules of thumb in optimizing the spurious tone performance. Increasing the reference frequency f_{ref} is also a possible way, but it is limited by the channel spacing requirement in the integer-N PLL structure. Furthermore, both poles at f_p and f_1 provide additional improvement on spur suppression, which is over 55 dB in the proposed design.

Introduction of the dual-path loop filter is advantageous in size reduction of loop filter capacitance, but the spurious tone performance degrades by the same factor B_{CP}. Contradiction in performance optimization also occurs in determination of resistance R_p. Small resistance value results in better spurious tone performance with the tradeoff of higher noise contribution and larger capacitance size.

The spurious tone performance of the proposed design under different charge pump current mismatches and turn-on duty cycles is displayed in Figure 3.15. There is better than 70 dB attenuation even the charge pump current mismatch and turn-on duty cycle

are as large as 10% and 20% respectively. Around 12 dB improvement can be obtained when decreasing the charge pump turn-on duty cycle by half.

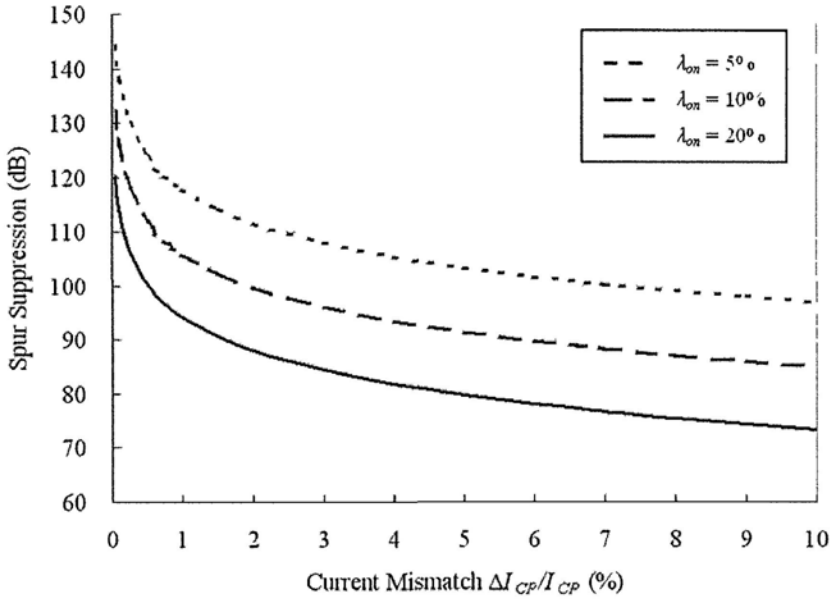


Figure 3.15 Spurious tone performance under the influences of charge pump current mismatch and turn-on duty cycle

3.3.3 Spurs due to Phase Mismatch in Phase Switching

In the phase-switching frequency divider, pulse swallowing for changing its division ratio is accomplished by switching between different inputs from a multi-phase clock source. It is recommended that the phase difference between consecutive phases of the clock source should be equal; otherwise phase error is induced in each phase switching. Due to phase mismatch, the overall division ratio will be varied by a small amount for each period in a periodic pattern. This small change has zero mean on average and the overall division ratio is still the expected constant value. However, it is equivalent to the situation of

indirect frequency modulation using PLL and consequently spurious tones emerge in the PLL output spectrum [85].

In the proposed programmable fractional frequency divider, the multi-phase clock generator composes of two conventional divide-by-4 injection-locked frequency dividers (ILFDs), which are cross-coupled together to generate eight equally-spaced outputs for phase switching. Phase mismatches between consecutive phases are inevitable due to manufacturing tolerances and other variations. Since the phase relationship between the two ILFD outputs is enforced by the coupling network, the sensitivity of inducing phase mismatch between the outputs of different ILFDs is higher than that between the outputs within the ILFD. As such, phase mismatch between the outputs of different ILFDs is the dominant factor of spur generation by phase switching.

To obtain fractional division ratio, the occurrence of phase switching in each period is an odd number. The phase selection is hence toggled between the outputs of the divide-by-4 ILFDs in alternate period. When phase mismatch exists, the frequency divider output period is varied between two values, as illustrated in Figure 3.16. Because the average period is still T_{ref}, the PLL functions normally as an integer-N PLL. Nevertheless, a phase offset of $\pm\pi\cdot\frac{\Delta t_d}{T_{ref}}$ occurs in alternate period with positive and negative current pulses pumped to the loop filter. According to Figure 3.16, since the current pulse train repeats with a period of $2T_{ref}$, spurious tones are generated at frequency offsets equal to multiples of $\pm f_{ref}/2$.

On the other hand, for integral division case, the number of phase switching activity in each period is even and hence the final phase selection will always occur in the same divide-by-4 ILFD as the first phase selection. Even there is phase mismatch between the divide-by-4 ILFDs, the period of the frequency divider output is not affected because there is no output switching between different divide-by-4 ILFDs in consecutive period as in the fractional division case. Consequently, the spur performance for integral division case will be better than that for fractional division case.

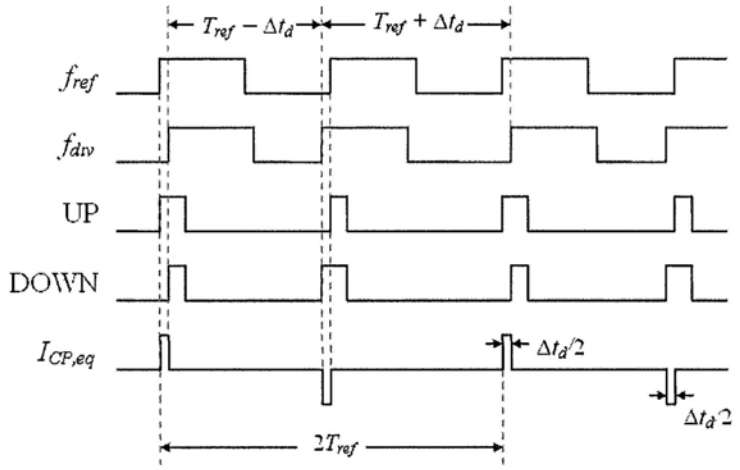


Figure 3.16 Effect of phase mismatch in phase switching of the frequency divider

The net charge pump current $I_{CP,eq}$ contains frequency components at multiples of $\pm f_{ref}/2$. Due to odd-mode symmetry of the waveform, it can be represented by Fourier sine series as:

$$I_{CP,eq}(t) = \sum_{k=1}^{\infty} b_k \sin\left(k\pi f_{ref} t\right) \tag{3.29}$$

and $$b_k = \frac{2}{T_{ref}} \int_0^{T_{ref}} I_{CP,eq}(t) \sin(k\pi f_{ref} t) dt \tag{3.30}$$

Evaluation of Equation 3.30 yields:

$$b_k = \begin{cases} \frac{2I_{CP}}{k\pi}(-1)^{k+1} \sin\left(\frac{k\pi}{2} \cdot \frac{\Delta t_d}{T_{ref}}\right) & k \text{ is odd} \\ \frac{4I_{CP}}{k\pi}(-1)^{k} \sin^2\left(\frac{k\pi}{4} \cdot \frac{\Delta t_d}{T_{ref}}\right) & k \text{ is even} \end{cases} \tag{3.31}$$

For small $\Delta t_d / T_{ref}$, the approximated magnitudes of the spurious components are given as:

$$|b_k| \approx \begin{cases} I_{CP} \cdot \frac{\Delta t_d}{T_{ref}} & k \text{ is odd} \\ \frac{k\pi}{4} \cdot I_{CP} \cdot \left(\frac{\Delta t_d}{T_{ref}}\right)^2 & k \text{ is even} \end{cases} \tag{3.32}$$

which implies that the spurious components can be suppressed with low charge pump current, as well as small phase offset. On the other hand, one may be confused that the contributions of high-order even-multiple spurious components increase with the factor k, which leads to infinite total power. For large k, the approximation $\sin\theta \approx \theta$ is no longer valid and therefore the magnitudes of the high-order even-multiple spurious components are limited to $\frac{4I_{CP}}{k\pi}$, which diminishes with increasing k. Same argument is also applicable for odd values of k.

Figure 3.17 shows the relative magnitudes of the second to seventh spurious components in respect to the first spurious component. It can be verified that, for small phase offset, all odd-multiple spurious components have roughly the same magnitude (the derivation is less than 0.5 dB for $\Delta t_d/T_{ref} \leq 5\%$) while the even-multiple spurious components are much weaker in few orders of magnitude. For $\Delta t_d/T_{ref} = 1\%$, the difference in magnitude is more than 25 dB. Among the even-multiple spurious components, higher order ones acquire larger amplitudes. Nevertheless, they are attenuated more by the loop filter and hence the spurious tones induced by them can be ignored. Similarly the influences of those high-order odd-multiple spurious components are minor even though their amplitudes are approximately the same as that of the first spurious component.

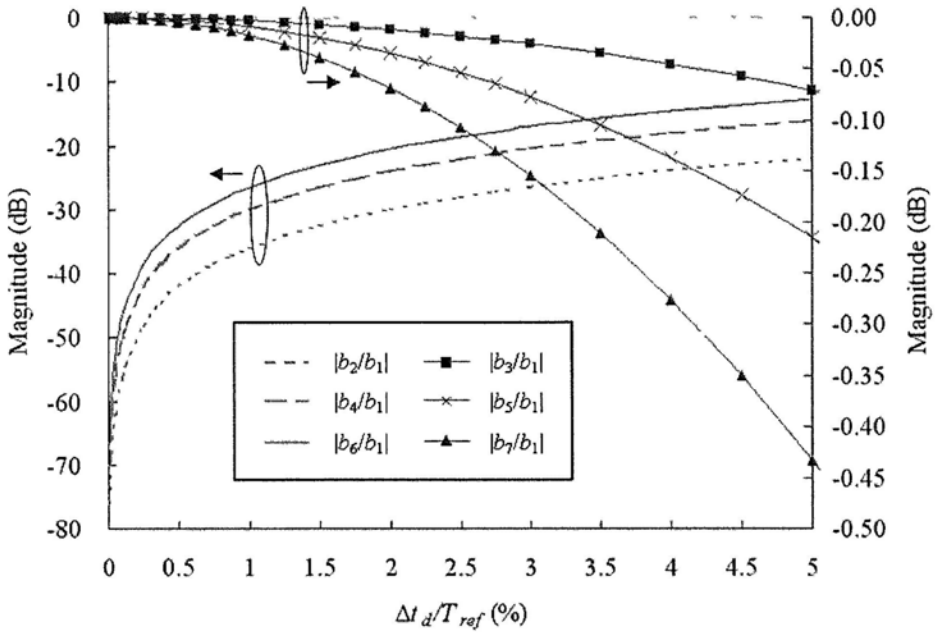


Figure 3.17 Influence of phase offset in spurious component magnitudes

The spur suppression expression for reference feedthrough mentioned in Equation 3.28 can be adopted to calculate the spurious tone performance due to the phase mismatch in phase switching. The expression is modified as:

$$\begin{aligned}&\text{Spur suppression at } \pm\frac{kf_{ref}}{2}\\&=-20\log\left(\frac{K_{VCO}\Delta i_{peak}\left|H_{LF}\left(j2\pi\left(kf_{ref}/2\right)\right)\right|}{2\left(kf_{ref}/2\right)}\right)\\&\approx-20\log\left(\frac{|b_k|K_{VCO}B_{CP}R_p}{kf_{ref}}\right)-20\log\left(\frac{2f_p}{kf_{ref}}\cdot\frac{2f_1}{kf_{ref}}\right)\end{aligned}\tag{3.33}$$

Figure 3.18 presents the suppression performance for the first four spurious components. The spurs induced by the even-multiple spurious components are less severe than those induced by the odd-multiple ones, as expected. There is more than 40 dB improvement when compared with the spurs at $\pm f_{ref}/2$. Moreover, the high-order spurious components are attenuated more by a factor of $60\log(k)$. Even the spurious component b_4 is larger than that of b_2, the suppression for spurs at $\pm 2f_{ref}$ is better than that at $\pm f_{ref}$ due to the additional attenuation of the loop filter. As seen in Figure 3.18, the dominant spurious tones occur at $\pm f_{ref}/2$ and the suppression is more than 70 dB for $\Delta t_d/T_{ref} < 0.5\%$

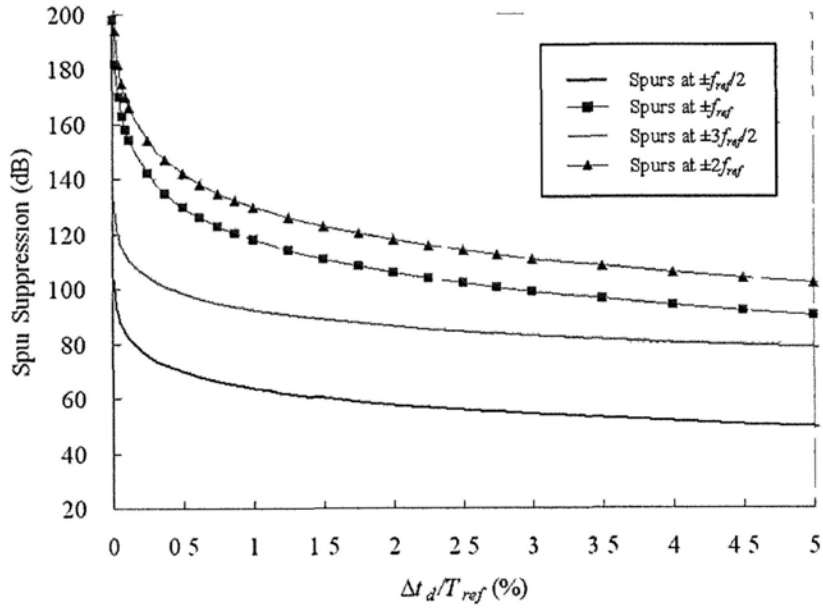


Figure 3 18 Spurious tone performance under the influence of phase mismatch in phase switching

CHAPTER 4

PROPOSED PROGRAMMABLE FRACTIONAL FREQUENCY DIVIDER

4.1 Architecture Description

Figure 4.1 shows the programmable fractional frequency divider architecture, which belongs to the phase-switching type. Compared with the flip-flop based static type [51], [53], [55], the proposed frequency divider can operate with fewer elements running at the full speed, leading to lower power dissipation and less capacitive loading burden.

The input stage of the proposed frequency divider is a dual divide-by-4 injection-locked frequency divider (ILFD), in which two conventional divide-by-4 ILFDs are cross-coupled together. Eight equally-spaced outputs at frequency equal to a quarter of input frequency are generated for phase switching. The backward-phase selection scheme [68] is employed in order to avoid glitch problem. Unlike in [73], the dual divide-by-4 ILFD

isolates the multiplexer from the quadrature input source, decreasing the operation frequency of the subsequent circuitry, reducing capacitive loading at the input ports and eliminating the possibility of quadrature phase deviation due to phase transition. No power-hungry buffer or interpolator [75] ran at the input clock rate is needed in the proposed design, but its division ratio resolution is limited to 0.5, as a tradeoff.

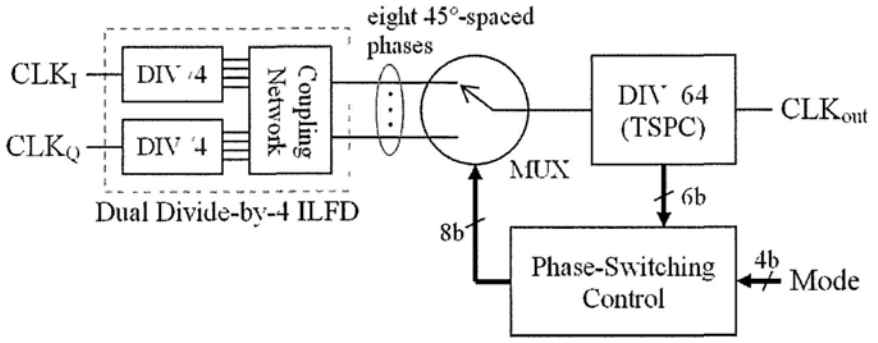


Figure 4.1 Architecture of the programmable fractional frequency divider

A single-stage 8-to-1 multiplexer is used to minimize the propagation delay. A control circuitry is also implemented to assure that the multiplexer selects only one of the input phases from the dual divide-by-4 ILFD, eliminating glitches during transition.

To reduce power consumption, the divide-by-64 frequency divider is implemented as a ripple-counter with 6-stage divide-by-2 frequency dividers in TSPC logic. Size scaling is applied to successive divide-by-2 stages. The 4-bit mode control determines the number of times to perform phase switching in each cycle for different division ratios. The phase-switching control circuitry consists of an 8-bit shift register to select the correct output phase and combinational logic to trigger the shift register to next state during phase switching.

The proposed frequency divider attains programmable division ratios from 240.5 to 248, with step size of 0.5. Figure 4.2 illustrates its fractional division principle. The multi-phase outputs of the dual divide-by-4 ILFD $\phi_0 - \phi_{315}$ have a period equal to 4 times that of the input clock $CLK_{I/Q}$ while the delay between consecutive outputs is half input clock period (0.5 T_{per}). Supposing that ϕ_{135} is initially selected to the multiplexer output MUX_{out}, and when there is no phase-switching operation, the period of MUX_{out} is 4 times that of the input clock, resulting in divide-by-4 operation. When phase switching occurs, the multiplexer swaps its output from ϕ_{135} to ϕ_{90}. MUX_{out} is shortened by $0.5T_{per}$ for each phase switching and hence the overall division ratio diminishes in step of 0.5.

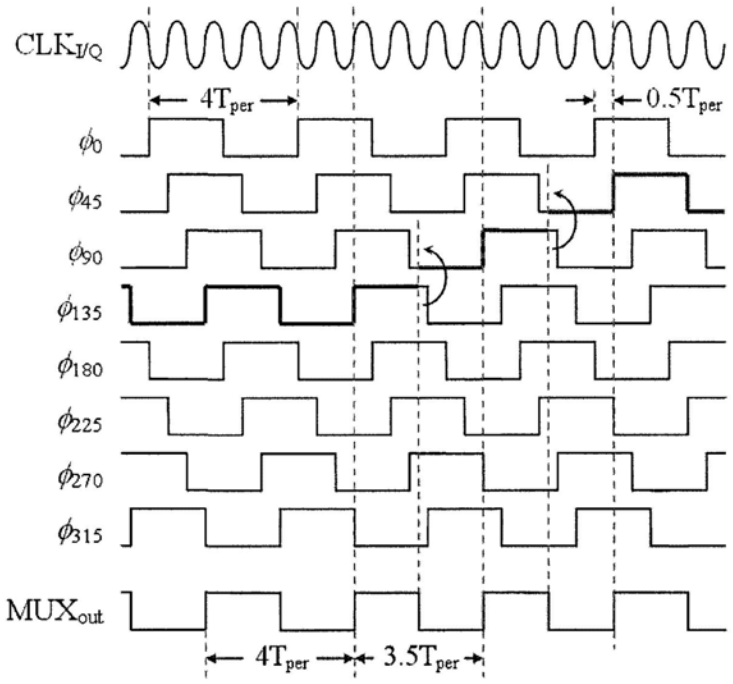


Figure 4.2 Illustration of fractional division by the phase-switching operation

4.2 Dual Divide-by-4 Injection-Locked Frequency Divider

The dual divide-by-4 ILFD composes of two standard divide-by-4 ILFDs and a coupling network, as depicted in Figure 4.3. The I- and Q-phases of the input clock are used to drive the two divide-by-4 ILFDs individually. Since the input clock loading is the same, its quadrature accuracy is maintained. Because single divide-by-4 ILFD produces quadrature phase outputs with one input clock period delay between consecutive outputs, only division ratio with integer values can be obtained in the phase-switching frequency divider. Intuitively, a coupling network is added to lock two divide-by-4 ILFDs with 45° offset. The resultant multi-phase signal resolution halves and fractional division becomes feasible.

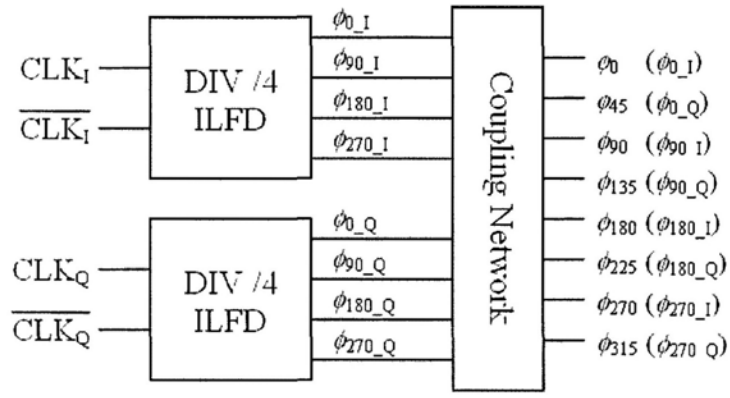


Figure 4.3 Block diagram of the dual divide-by-4 ILFD

The coupling network is realized in two different approaches, namely the cross-coupling and coherent-coupling designs. Based on the generalized behavior modeling in Appendix

B, the cross-coupling approach has the advantage of wide locking range while the coherent-coupling design can operate at higher frequency.

4.2.1 Cross-Coupling Design

Figure 4.4 shows the schematic of the quadrature-input cross-coupling dual divide-by-4 ILFD. Two identical divide-by-4 ILFDs are cross-coupled together to generate eight 45°-spaced outputs for phase switching in the subsequent stage. For instance, Latch 1 and 2 form a ring oscillator, in which both are triggered by the same clocking signals (I-phases of the input clock). Four input clock cycles are needed for their output signals to return to the original state, thus resulting in divide-by-4 operation [86]. Moreover, the outputs are in quadrature and their phase sequence is unique. Likewise, another divide-by-4 ILFD, which are clocked by the Q-phases, composes of Latch 3 and 4. Since each input clock phase drives equal size clock transistor with same biasing condition, the loading is well matched and so it does not deteriorate the quadrature accuracy of the input clock source (the quadrature VCO, in this case).

A source-coupled logic (SCL) latch with PMOS active load is used as the basic building block of the latches in the proposed cross-coupling dual divide-by-4 ILFD. In contrast to conventional designs, the source nodes of the sensing transistor pairs are connected together in each divide-by-4 ILFD. The same applies to the source nodes of the hold transistor pairs and those of the coupling transistor pairs too. By doing so, the bias current can be adaptively supplied to the devices that demand more current for toggling while less current is flowing through those that preserve their present state. The circuit can then

operates at higher frequency with same power consumption when compared with the conventional design with separate bias current for each latch.

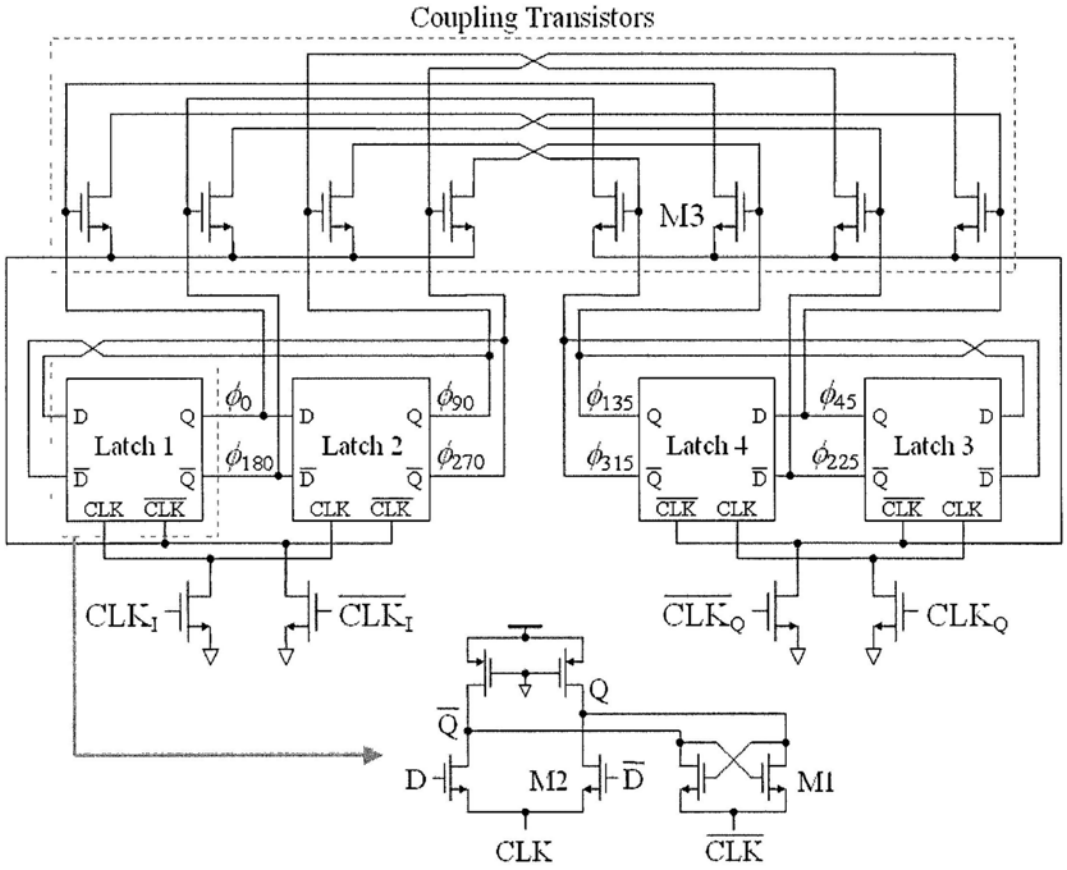


Figure 4.4 Schematic of the quadrature-input cross-coupling dual divide-by-4 ILFD

The coupling network of the quadrature-input cross-coupling dual divide-by-4 ILFD is implemented with eight NMOS transistors, as outlined on top of Figure 4.4. Each coupling transistor injects current to the corresponding phase output node so as to introduce additional phase derivation to the output phase, enforcing the desired phase offset of 45° between the outputs of the two divide-by-4 ILFDs. Besides, the coupling relationship of the coupling transistors forms a cyclic symmetrical structure. The input

and output phases for each coupling transistor differ by 225°. As an example, ϕ_0 couples with ϕ_{225} while the coupling transistor controlled by ϕ_{135} induces current injection to ϕ_0. The complete coupling sequence for the proposed design is $\phi_0 \rightarrow \phi_{225} \rightarrow \phi_{90} \rightarrow \phi_{315} \rightarrow \phi_{180} \rightarrow \phi_{45} \rightarrow \phi_{270} \rightarrow \phi_{135} \rightarrow \phi_0$, as displayed in Figure 4.5.

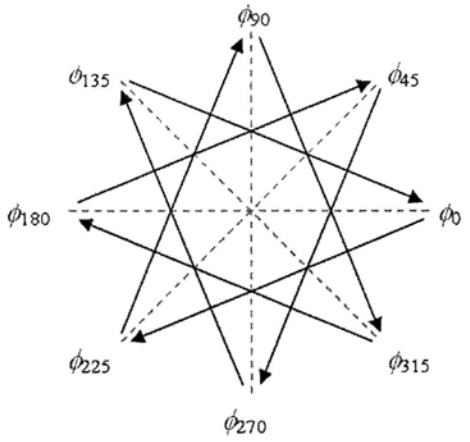


Figure 4.5 Coupling sequence of the quadrature-input cross-coupling dual divide-by-4 ILFD

Focusing on the output node ϕ_0, the behavior model of the quadrature-input cross-coupling dual divide-by-4 ILFD is derived, as presented in Figure 4.6. The proposed circuit is modeled as a regenerative frequency divider [58]. The hold transistor M1, sensing transistor M2 and coupling transistor M3 behave as hard switching mixers driven by the corresponding output voltages. The injection signals i_{in_1}, i_{in_2} and i_{in_3}, composed of DC bias current and AC component at input frequency, are provided by the input clock transistors. They are inputted to the source terminals of M1, M2 and M3 accordingly. Current components i_1, i_2 and i_3 are then generated by mixing operation, flowing into the PMOS load, whose impedance can be expressed as:

$$Z(j\omega)=\frac{R}{1+j\dfrac{\omega}{\omega_0}}=|Z(j\omega)|e^{j\varphi(\omega)} \tag{4.1}$$

where $\varphi(\omega)=-\arctan\left(\dfrac{\omega}{\omega_0}\right)$ and $\omega_0=\dfrac{1}{RC}$

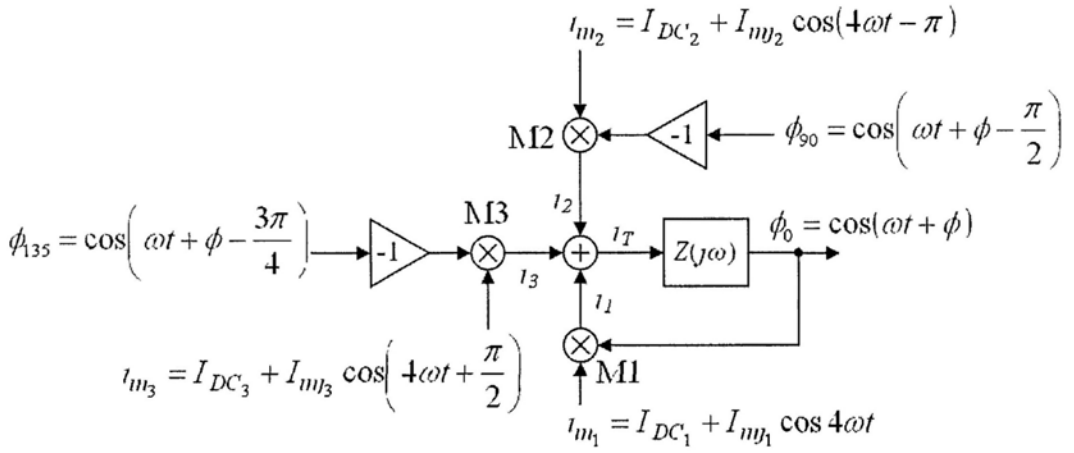


Figure 4.6 Behavior model of the quadrature-input cross-coupling dual divide-by-4 ILFD

To sustain steady-state oscillation in the loop with incident signals, the Barkhausen criteria on gain and phase must be satisfied, i.e. the loop gain at the operation frequency should be greater than unity and the total phase shift around the loop must be zero. Generally, the gain condition is met because the DC component in the mixer input current causes the loop self-oscillation [87]. Nonetheless, this DC term reduces the maximum achievable phase shift of the mixer output current and thus limits the locking range [88].

The *RC* load introduces a phase shift $\varphi(\omega)$ between the input current and the output voltage, within a range from 0 to -π/2 dependent on the operation frequency ω. To satisfy

the criterion of zero total phase shift around the loop, the resultant mixer current i_T is required to induce a phase shift of α_T to compensate that introduced by the *RC* load (that is, $\alpha_T + \varphi(\omega) = 0$).

Consider the occasion for mixer operation when a driving sinusoidal signal at frequency of ω is multiplied by a DC signal plus an AC signal at frequency of 4ω, as depicted in Figure 4.7. Due to the hard-limiting characteristic of the transconductor, the driving signal is considered not a pure sine wave, but rather a square wave with fundamental peak of $4/\pi$ [89]. The fundamental component of the mixer output current I_0 is then evaluated as:

$$\begin{aligned} I_0 &= \left[I_{DC} + I_{inj}\cos(4\omega t)\right]\cdot\left[\frac{4}{\pi}\cos(\omega t+\phi) - \frac{4}{3\pi}\cos(3\omega t+3\phi)\right. \\ &\quad \left. + \frac{4}{5\pi}\cos(5\omega t+5\phi) + \cdots\right] \\ &= \frac{4}{\pi}I_{DC}\cos(\omega t+\phi) - \frac{2}{3\pi}I_{inj}\cos(\omega t-3\phi) + \frac{2}{5\pi}I_{inj}\cos(\omega t+5\phi) \\ &\quad + \text{higher harmonics} \end{aligned} \tag{4.2}$$

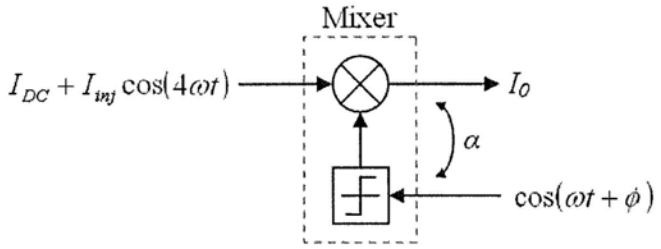


Figure 4.7 Mixer operation with a DC and a quadruple frequency sinusoidal input current

Because of the lowpass nature of the *RC* load, higher harmonics in I_0 are filtered out. Equation 4.2 is simplified and written in complex notation as:

$$\begin{aligned} I_0 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj} e^{j\omega t} e^{j\phi}\left[\frac{I_{DC}}{I_{inj}} - \frac{1}{6} e^{-j4\phi} + \frac{1}{10} e^{j4\phi}\right]\right\} \\ &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj} e^{j\omega t} e^{j\phi}\left[\frac{I_{DC}}{I_{inj}} - \frac{1}{15}\cos(4\phi) + j\frac{4}{15}\sin(4\phi)\right]\right\} \\ &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj} e^{j\omega t} e^{j\phi} \cdot K e^{j\alpha}\right\} \\ &= \frac{4}{\pi} I_{inj} K \cos(\omega t + \phi + \alpha) \end{aligned} \tag{4.3}$$

The extra phase shift α is determined as:

$$\alpha = \arctan\left[\frac{4\eta \sin(4\phi)}{15 - \eta\cos(4\phi)}\right] \tag{4.4}$$

where $\eta = \dfrac{I_{inj}}{I_{DC}}$ is the injection ratio.

In this case, it demonstrates that the mixer adds a phase lead α in the output current, which can be used to balance the phase lag $\varphi(\omega)$ introduced by the *RC* load. For stronger injection strength, the possible range of phase shift α increases and therefore the locking range extends.

Practically, since $\eta\cos(4\phi) \ll 15$, the phase shift α and magnitude change K can be approximated as:

$$\begin{aligned} \alpha &\approx \arctan\left[\frac{4}{15}\eta\sin(4\phi)\right] \\ K &\approx \frac{1}{\eta}\left|\sec\alpha\right| \end{aligned} \tag{4.5}$$

Returned to the proposed cross-coupling dual divide-by-4 ILFD, the resultant mixer output current i_T consists of three components that are generated by different mixing processes, as shown in Figure 4.6. Their fundamental components can be expressed as:

$$\begin{aligned} i_1 &= \mathrm{Re}\left\{\frac{4}{\pi}I_{inj_1}e^{j\omega t}e^{j\phi}\cdot K_1 e^{j\alpha_1}\right\} \\ i_2 &= \mathrm{Re}\left\{\frac{4}{\pi}I_{inj_2}e^{j\omega t}e^{j\phi}e^{j\pi/2}\cdot K_2 e^{j\alpha_2}\right\} \\ i_3 &= \mathrm{Re}\left\{\frac{4}{\pi}I_{inj_3}e^{j\omega t}e^{j\phi}e^{j\pi/4}\cdot K_3 e^{j\alpha_3}\right\} \end{aligned} \tag{4.6}$$

where

$$K_n = \frac{1}{\eta_n}\left|\sec\alpha_n\right| \qquad \text{for } n = 1, 2 \text{ and } 3 \tag{4.7}$$

and

$$\begin{aligned} \alpha_1 &= \arctan\left[\frac{4}{15}\eta_1\sin(4\phi)\right] \\ \alpha_2 &= -\arctan\left[\frac{4}{15}\eta_2\sin(4\phi)\right] \\ \alpha_3 &= \arctan\left[\frac{4}{15}\eta_3\cos(4\phi)\right] \end{aligned} \tag{4.8}$$

To derive the phase of the resultant mixer output current, its expression is manipulated in complex form as:

$$\begin{aligned} i_T &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left[I_{inj_1}K_1e^{j\alpha_1}+I_{inj_2}K_2e^{j\pi/2}e^{j\alpha_2}+I_{inj_3}K_3e^{j\pi/4}e^{j\alpha_3}\right]\right\} \\ &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left\{\left[I_{DC_1}+\frac{4}{15}I_{DC_2}\eta_2\sin(4\phi)+\frac{1}{\sqrt{2}}I_{DC_3}\left(1-\frac{4}{15}\eta_3\cos(4\phi)\right)\right]\right.\right. \\ &\quad \left.\left.+j\left[\frac{4}{15}I_{DC_1}\eta_1\sin(4\phi)+I_{DC_2}+\frac{1}{\sqrt{2}}I_{DC_3}\left(1+\frac{4}{15}\eta_3\cos(4\phi)\right)\right]\right\}\right\} \\ &= |i_T|\cos(\omega t+\phi+\alpha_T) \end{aligned} \tag{4.9}$$

where the overall mixer output phase α_T is

$$\alpha_T = \arctan\left[\frac{15\left(\sqrt{2}I_{DC_2}+I_{DC_3}\right)+4\left[\sqrt{2}I_{DC_1}\eta_1\sin(4\phi)+I_{DC_3}\eta_3\cos(4\phi)\right]}{15\left(\sqrt{2}I_{DC_1}+I_{DC_3}\right)+4\left[\sqrt{2}I_{DC_2}\eta_2\sin(4\phi)-I_{DC_3}\eta_3\cos(4\phi)\right]}\right] \tag{4.10}$$

For stable oscillation, the phase condition $\varphi(\omega)+\alpha_T=0$ should be fulfilled at operation frequency ω, which leads to

$$\frac{\omega}{\omega_0} = \frac{15\left(\sqrt{2}I_{DC_2}+I_{DC_3}\right)+4\left[\sqrt{2}I_{DC_1}\eta_1\sin(4\phi)+I_{DC_3}\eta_3\cos(4\phi)\right]}{15\left(\sqrt{2}I_{DC_1}+I_{DC_3}\right)+4\left[\sqrt{2}I_{DC_2}\eta_2\sin(4\phi)-I_{DC_3}\eta_3\cos(4\phi)\right]} \tag{4.11}$$

In the proposed cross-coupling dual divide-by-4 ILFD displayed in Figure 4.4, the hold and coupling transistors share the same bias current and injection signal and so the following conditions hold:

$$\begin{aligned} I_{DC_2} &= I_{DC_1} + I_{DC_3} \\ I_{inj_2} &= I_{inj_1} + I_{inj_3} \end{aligned} \tag{4.12}$$

Assuming equal partition of the bias current and injection signal among the hold and coupling transistors, all injection strengths are the same, that is $\eta_1 = \eta_2 = \eta_3 = \eta$. The total mixer output phase shift α_T becomes:

$$\alpha_T = \arctan\left[\frac{15\left(2\sqrt{2}+1\right)+4\eta\left(\sqrt{2}\sin(4\phi)+\cos(4\phi)\right)}{15\left(\sqrt{2}+1\right)+4\eta\left(2\sqrt{2}\sin(4\phi)-\cos(4\phi)\right)}\right] \tag{4.13}$$

Figure 4.8 plots the resultant mixer output phase response α_T against the divider output phase ϕ for different injection ratios. Strong injection leads to a broader range of α_T, which allows a wider divider locking range. For instance, the maximum phase shift range is less than 4° for η = 0.25 while it increases to around 14.6° for η = 1. The divider locking range extends from 14% to 57%, as illustrated in Figure 4.9.

From Equation 4.11, the operation frequency of the cross-coupling dual divide-by-4 ILFD should obey:

$$\frac{\omega}{\omega_0} = \frac{15\left(2\sqrt{2}+1\right)+4\eta\left[\sqrt{2}\sin(4\phi)+\cos(4\phi)\right]}{15\left(\sqrt{2}+1\right)+4\eta\left[2\sqrt{2}\sin(4\phi)-\cos(4\phi)\right]} \tag{4.14}$$

The locking range is then the frequency set that satisfies Equation 4.14. This analysis is further validated by circuit simulations, as presented in Fig. 4.9. The result agrees well

for small η. The discrepancy with increasing η is due to the reduction of effective injection signal strength caused by nonlinearity of the input clock transistors at large signal operation.

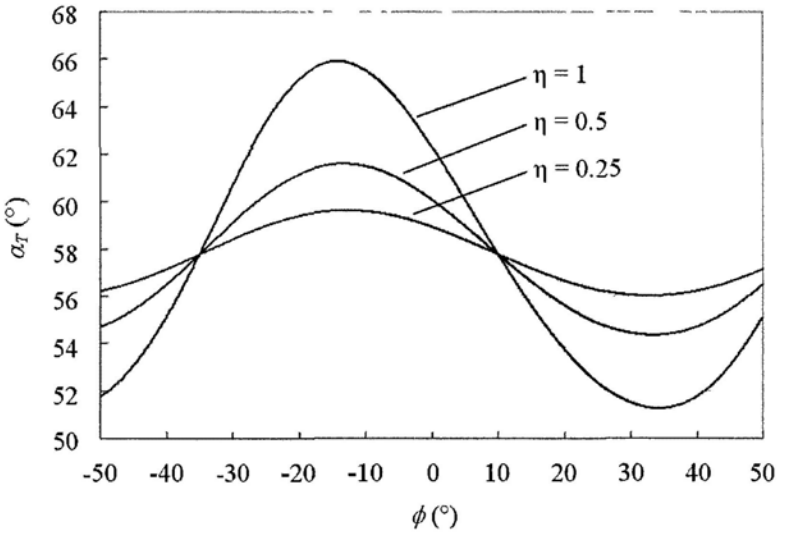


Figure 4.8 Resultant mixer output phase response versus divider output phase for various injection ratios

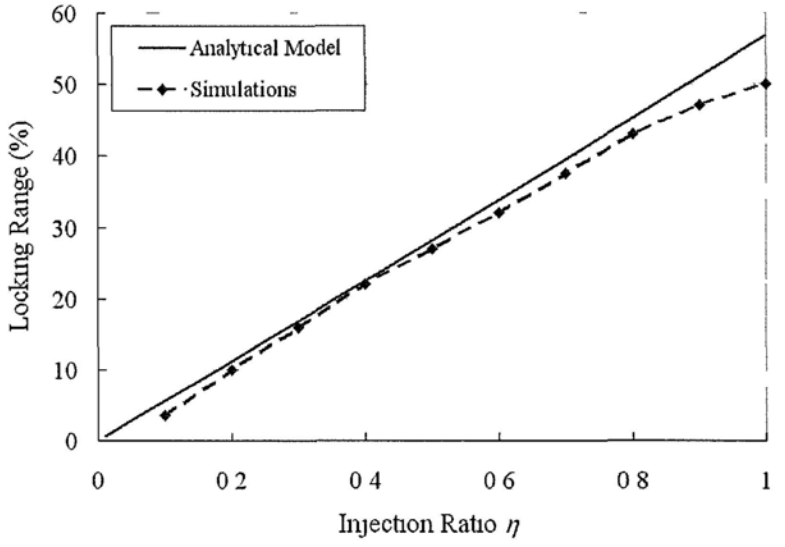


Figure 4.9 Calculated and simulated locking range of the cross-coupling dual divide-by-4 ILFD

The bias current distribution between the hold and coupling transistors affects the divider operation frequency and locking range. By defining the coupling ratio $\eta_{DC} = \frac{I_{DC_3}}{I_{DC_2}}$ and assuming all injection ratios $\eta_1 = \eta_2 = \eta_3 = \eta$, Equation 4.11 is transformed as:

$$\frac{\omega}{\omega_0} = \frac{15\left(\sqrt{2}+\eta_{DC}\right)+4\eta\left\{\sqrt{2}\sin(4\phi)-\eta_{DC}\left[\sqrt{2}\sin(4\phi)-\cos(4\phi)\right]\right\}}{15\left[\sqrt{2}+\left(1-\sqrt{2}\right)\eta_{DC}\right]+4\eta\left[\sqrt{2}\sin(4\phi)-\eta_{DC}\cos(4\phi)\right]} \tag{4.15}$$

With increasing coupling ratio η_{DC}, both the divider center frequency and locking range increase, as shown in Figure 4.10. The shift in center frequency by the injection ratio η is not as significant as that of η_{DC}, but the locking range increases twice for every doubling of η. However, due to the lowpass characteristic of the *RC* load, the divider output voltage decreases when operating at higher frequency.

Till now, the discussions of the cross-coupling dual divide-by-4 ILFD properties are based on the phase sequence mentioned in Figure 4.5, where ϕ_0 leads ϕ_{45} by 45°. The existence of reverse phase pattern (ϕ_0 lags ϕ_{45} by 45°) is destructive because incorrect phase switching occurs. For the reverse phase pattern, the outputs of the second divide-by-4 ILFD (ϕ_{45}, ϕ_{135}, ϕ_{225} and ϕ_{315}) are advanced by 90° and mapped to ϕ_{315}, ϕ_{45}, ϕ_{135} and ϕ_{225} respectively. Its coupling sequence becomes $\phi_0 \rightarrow \phi_{135} \rightarrow \phi_{90} \rightarrow \phi_{225} \rightarrow \phi_{180} \rightarrow \phi_{315} \rightarrow \phi_{270} \rightarrow \phi_{45} \rightarrow \phi_0$, in which the phase shift between consecutive stages becomes uneven. As a result, the two divide-by-4 ILFDs may operate at different frequencies and this degrades the phase sequence matching with phase offsets.

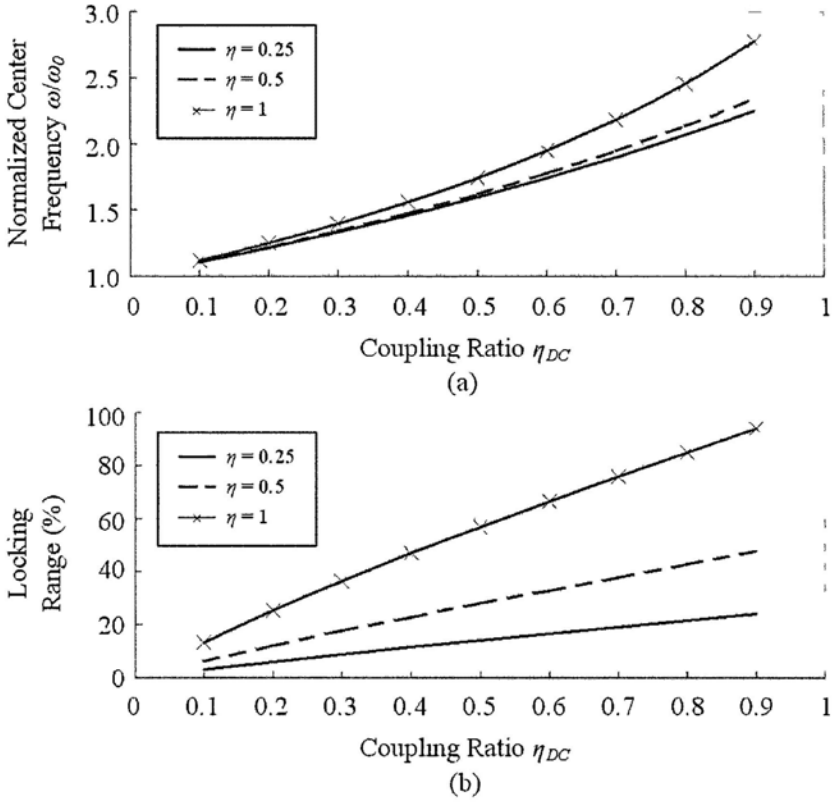


Figure 4.10 Influence of coupling strength on (a) divider output center frequency (normalized) and (b) locking range, for different injection ratios

Moreover, the output amplitude for the desired phase pattern is greater than that for the reverse one, as depicted in Figure 4.11. Because the current component generated by the coupling transistor is in the same direction as the resultant one produced by the sensing and hold transistors, the output amplitude is enhanced in the desired phase pattern. In contrast, they are almost orthogonal in the reverse phase pattern. Smaller output amplitude therefore results. As the mode with higher amplitude is stable [90], the reverse phase pattern cannot sustain and only the desired phase pattern is feasible.

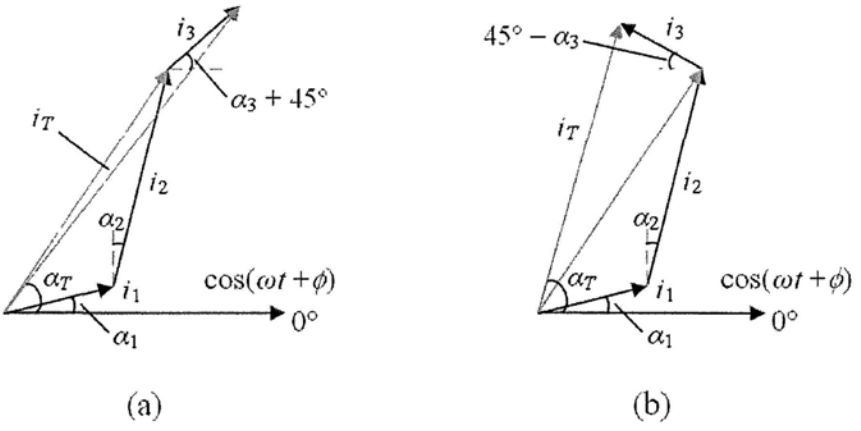


Figure 4.11 Phasor diagram of the resultant mixer output current and output voltage for (a) the desired phase pattern and (b) the reverse phase pattern

4.2.2 Coherent-Coupling Design

The quadrature-input coherent-coupling dual divide-by-4 ILFD, whose schematic is shown in Figure 4.12, composes of two divide-by-4 ILFDs and a coupling network. The divide-by-4 ILFD is implemented as a ring oscillator built with two latches. Its outputs are in quadrature and the output phase sequence is unique. In the proposed design, Latch 1 and 2, both triggered by the I-phases of the input clock, constitutes a divide-by-4 ILFD. Another is formed by Latch 3 and 4, which are clocked by the Q-phases. Because the loading for each input clock phase is identical (equal size clock transistor at same biasing condition), the quadrature accuracy of the input clock source (i.e. QVCO) is maintained.

The latch used in the proposed coherent-coupling dual divide-by-4 ILFD is constructed as a SCL latch with PMOS active load. To enhance the circuit operation frequency, the bias transistors for the sensing transistor pairs and hold transistor pairs for each latch are grouped together in each divide-by-4 ILFD. For the coupling transistor, their source

nodes are also joined. The proposed scheme does not affect the circuit functionality, instead the bias current can be adjusted autonomously so as to supply more current to the devices toggling their outputs while less current is flowing through those that hold their present state. As a result, the overall power consumption does not increase at higher operation frequency when compared with the standard design with separate bias current for each latch.

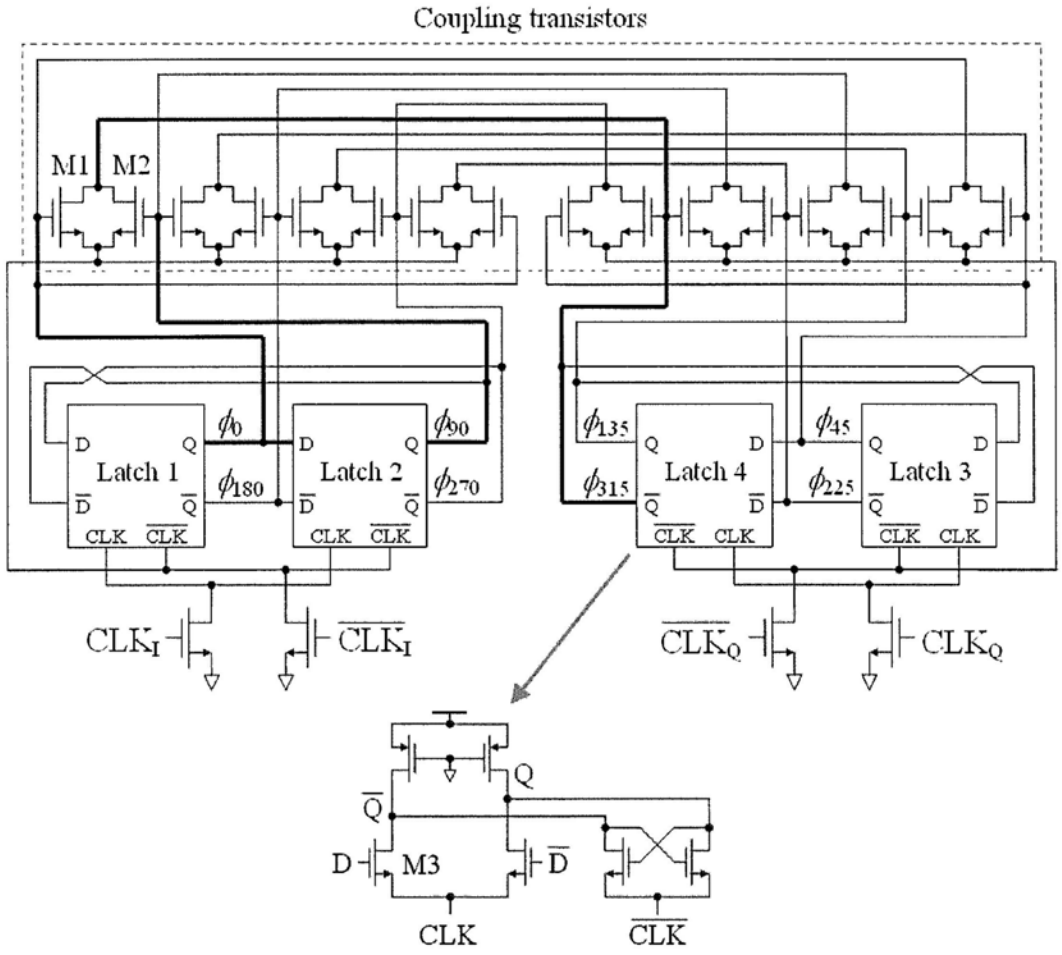


Figure 4.12 Schematic of the quadrature-input coherent-coupling dual divide-by-4 ILFD

The cross coupling between two divide-by-4 ILFDs is realized by a coupling transistor pair for each phase. For example, as depicted in Figure 4.12, ϕ_0 and ϕ_{90} control the coupling transistors M1 and M2, whose drains are connected to ϕ_{315}. When either ϕ_0 or ϕ_{90} is Hi, ϕ_{315} will be discharged. Originally when there are no coupling transistors, ϕ_{315} is only controlled by ϕ_{45} through the sensing transistor M3. When ϕ_{45} is Lo, ϕ_{315} is charged up through the PMOS active load and then grows up till hitting the rail. Long discharge time is needed to toggle ϕ_{315} form Hi to Lo and thus the operation speed is limited.

With introduction of the coupling transistors, signal growth at ϕ_{315} is restricted and discharge time is also shortened. Consequently, the circuit can work at higher frequency. As presented in Figure 4.13, for 2.4 GHz divide-by-4 ILFDs, their operation frequency can be increased to 3.7 GHz (over 50% improvement) when coupling transistors are implemented. In this way, the circuit can be scaled down to operate at 2.4 GHz with lower power dissipation. Compared with two stand-alone divide-by-4 ILFDs, simulation results reveal that the proposed coherent-coupling dual divide-by-4 ILFD achieves about 23% power saving when operating at 2.4 GHz.

Figure 4.14 illustrates the operation principle of the proposed coherent-coupling dual divide-by-4 ILFD with the coupling transistors. Before time t_1, ϕ_{315} is rising since ϕ_{45} is Lo. The coupling transistors M1 and M2 have little contribution to pull down ϕ_{315} because both ϕ_0 and ϕ_{90} are Lo. At time t_1, when both $\overline{CLK_I}$ and ϕ_0 are Hi, the coupling transistor M1 is activated and discharges ϕ_{315}, limiting it raised to the rail. A quarter cycle later when CLK_Q is Hi at time t_2, the sensing transistor M3 starts discharging ϕ_{315},

toggling it from Hi to Lo. At time t_3, another coupling transistor M2 takes effect as ϕ_{90} becomes Hi. The voltage swift of ϕ_{315} is reduced to less than 1V, which enables fast charging and discharging of the node.

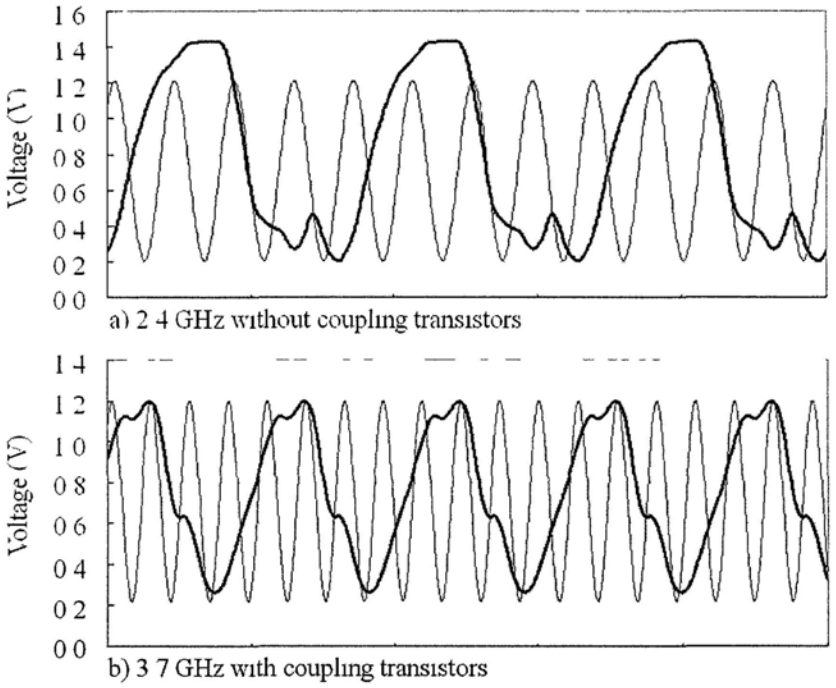


Figure 4.13 Simulation result comparison of the divide-by-4 ILFD output with and without coupling transistors

As mentioned, the stand-alone divide-by-4 ILFD has uniquely defined phase sequence. Nevertheless, there are two possible phase patterns for the overall eight output phases of the coupled ILFDs, that is, ϕ_0 lags or leads ϕ_{315} by 45°. The desired phase pattern is shown in Figure 4.14, where ϕ_0 lags ϕ_{315} by 45°. The undesired phase pattern is hard to be a stable state because the coupling transistor will oppose the change induced by the sensing transistor if ϕ_0 leads ϕ_{315} by 45°. In this case, ϕ_{315} becomes undetermined. The desired phase pattern is therefore the only feasible pattern. Unlike [68], the proposed

design requires no additional circuitry to detect the correct phase-switching sequence. The control circuitry is simpler in structure and more power efficient. Furthermore, the glitch problem is solved without a power-hungry synchronizing circuit as in [91].

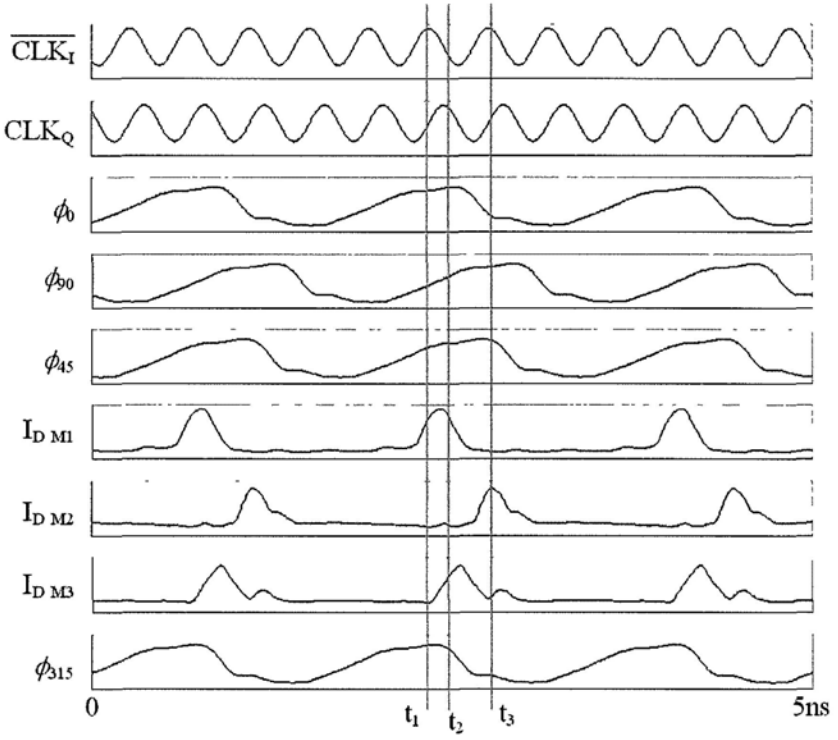


Figure 4.14 Simulation result of the operation principle of the quadrature-input coherent-coupling dual divide-by-4 ILFD

Figure 4.15 depicts the simulated maximum and minimum operation frequencies in relation to the coupling transistor size. The coupling transistor size is compared with the sensing transistor size as plotted in the x-axis. In Figure 4.15, the maximum operation frequency locates roughly at width ratio of 1. As the coupling transistor size increases, the increased capacitive load dominates the charge and discharge time constant of the output nodes. As such, there is a decrease of operation frequency. On the other hand, if

the coupling transistor size is too small, it is not sufficient to limit the signal growth at the output nodes and hence the operation frequency reduces too. The simulated operation frequency range is about 550 MHz when the coupling and sensing transistors have equal size.

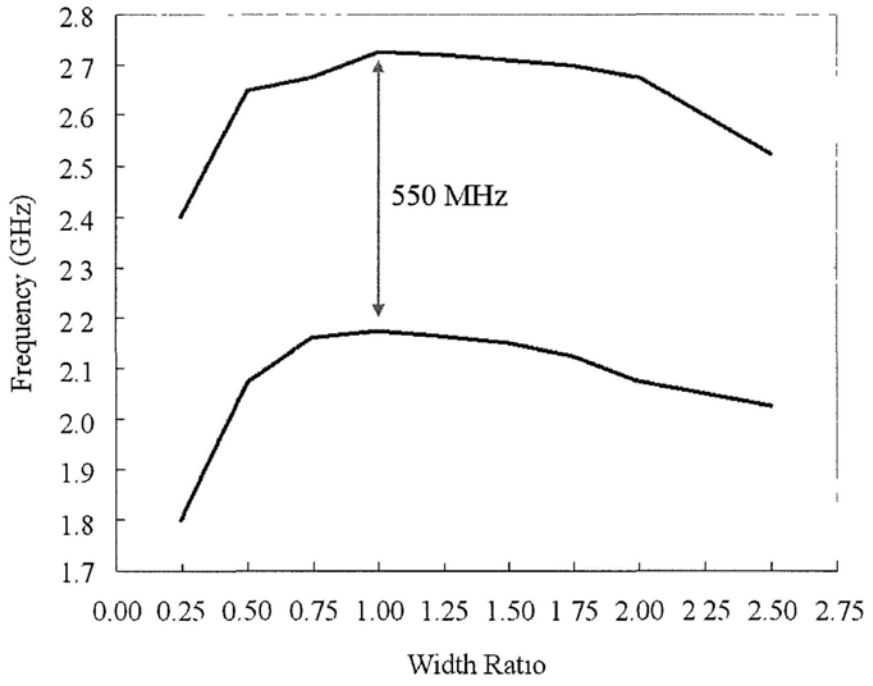


Figure 4.15 Simulation result of the operation frequency range of the quadrature-input coherent-coupling dual divide-by-4 ILFD versus coupling transistor size

The behavior model of the quadrature-input coherent-coupling dual divide-by-4 ILFD, which is shown in Figure 4.16, is developed in the same manner as that of the cross-coupling counterpart. Compared with that of the cross-coupling type, there is an additional contribution from the coupling transistor driven by ϕ_{45}. The fundamental components of the four branches can be expressed as:

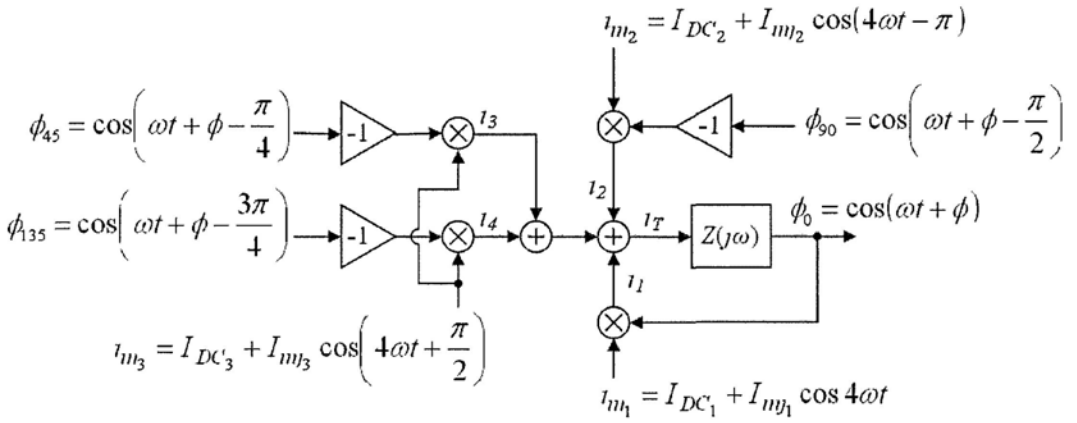


Figure 4.16 Behavior model of the quadrature-input coherent-coupling dual divide-by-4 ILFD

$$
\begin{aligned}
i_1 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_1} e^{j\omega t} e^{j\phi} \cdot K_1 e^{j\alpha_1}\right\} \\
i_2 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_2} e^{j\omega t} e^{j\phi} e^{j\pi/2} \cdot K_2 e^{j\alpha_2}\right\} \\
i_3 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_3} e^{j\omega t} e^{j\phi} e^{j3\pi/4} \cdot \frac{1}{2} K_3 e^{j\alpha_3}\right\} \\
i_4 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_3} e^{j\omega t} e^{j\phi} e^{j\pi/4} \cdot \frac{1}{2} K_3 e^{j\alpha_4}\right\}
\end{aligned}
\tag{4.16}
$$

where

$$
K_n = \frac{1}{\eta_n}\left|\sec\alpha_n\right| \qquad \text{for } n = 1, 2 \text{ and } 3 \tag{4.17}
$$

and

$$
\begin{aligned}
\alpha_1 &= \arctan\left[\frac{4}{15}\eta_1 \sin(4\phi)\right] \\
\alpha_2 &= -\arctan\left[\frac{4}{15}\eta_2 \sin(4\phi)\right] \\
\alpha_3 &= \alpha_4 = \arctan\left[\frac{4}{15}\eta_3 \cos(4\phi)\right]
\end{aligned}
\tag{4.18}
$$

The factor $\frac{1}{2}$ in the expressions for i_3 and i_4 in Equation 4.16 is due to the fact that input current i_{in_3} is distributed to two coupling transistors. The resultant mixer output current can be derived in complex form as:

$$\begin{aligned} i_T &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left[I_{inj_1}K_1e^{j\alpha_1}+I_{inj_2}K_2e^{j\pi/2}e^{j\alpha_2}+I_{inj_3}\frac{K_3}{2}\left(e^{j3\pi/4}e^{j\alpha_3}+e^{j\pi/4}e^{j\alpha_4}\right)\right]\right\} \\ &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left\{\left[I_{DC_1}+\frac{4}{15}I_{DC_2}\eta_2\sin(4\phi)-\frac{4}{15\sqrt{2}}I_{DC_3}\eta_3\cos(4\phi)\right]\right.\right. \\ &\quad \left.\left.+j\left[\frac{4}{15}I_{DC_1}\eta_1\sin(4\phi)+I_{DC_2}+\frac{1}{\sqrt{2}}I_{DC_3}\right]\right\}\right\} \\ &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\cdot K_Te^{j\alpha_T}\right\} \\ &= |i_T|\cos(\omega t+\phi+\alpha_T) \end{aligned} \tag{4.19}$$

where the overall mixer output phase α_T is

$$\alpha_T = \arctan\left[\frac{15\left(\sqrt{2}I_{DC_2}+I_{DC_3}\right)+4\sqrt{2}I_{DC_1}\eta_1\sin(4\phi)}{15\sqrt{2}I_{DC_1}+4\left[\sqrt{2}I_{DC_2}\eta_2\sin(4\phi)-I_{DC_3}\eta_3\cos(4\phi)\right]}\right] \tag{4.20}$$

For the phase condition $\varphi(\omega)+\alpha_T=0$ with stable oscillation, it implies that:

$$\frac{\omega}{\omega_0} = \frac{15\left(\sqrt{2}I_{DC_2}+I_{DC_3}\right)+4\sqrt{2}I_{DC_1}\eta_1\sin(4\phi)}{15\sqrt{2}I_{DC_1}+4\left[\sqrt{2}I_{DC_2}\eta_2\sin(4\phi)-I_{DC_3}\eta_3\cos(4\phi)\right]} \tag{4.21}$$

Assuming equal partition of the bias current and injection signal among the hold and coupling transistors, it leads to:

$$\begin{aligned} &I_{DC_1} : I_{DC_2} : I_{DC_3} = I_{inj_1} : I_{inj_2} : I_{inj_3} = 1:3:2 \\ &\eta_1 = \eta_2 = \eta_3 = \eta \end{aligned} \tag{4.22}$$

Equation 4.21 becomes

$$\frac{\omega}{\omega_0} = \frac{15\left(3+\sqrt{2}\right)+4\eta\sin(4\phi)}{15+4\eta\left[3\sin(4\phi)-\sqrt{2}\cos(4\phi)\right]} \tag{4.23}$$

Figure 4.17 displays the relationships of the normalized center frequency and locking range with injection ratio η, based on Equation 4.23. A dramatic increase in the normalized center frequency is observed for large injection ratio. However, due to the lowpass characteristic of the *RC* load, the output amplitude will decrease significantly and the implication of gain condition fulfillment may be violated.

The output amplitude is the product of the resultant mixer output current magnitude and the transfer characteristic of the *RC* load, that is:

$$\begin{aligned} \left|i_T\right| \cdot \left|Z(j\omega)\right| &= \frac{4}{\pi} K_T \cdot \frac{R}{\sqrt{1+\left(\omega/\omega_0\right)^2}} \\ &= \frac{4}{\pi} I_{DC_1} R\left\{1+\frac{4}{15}\eta\left[3\sin(4\phi)-\sqrt{2}\cos(4\phi)\right]\right\} \end{aligned} \tag{4.24}$$

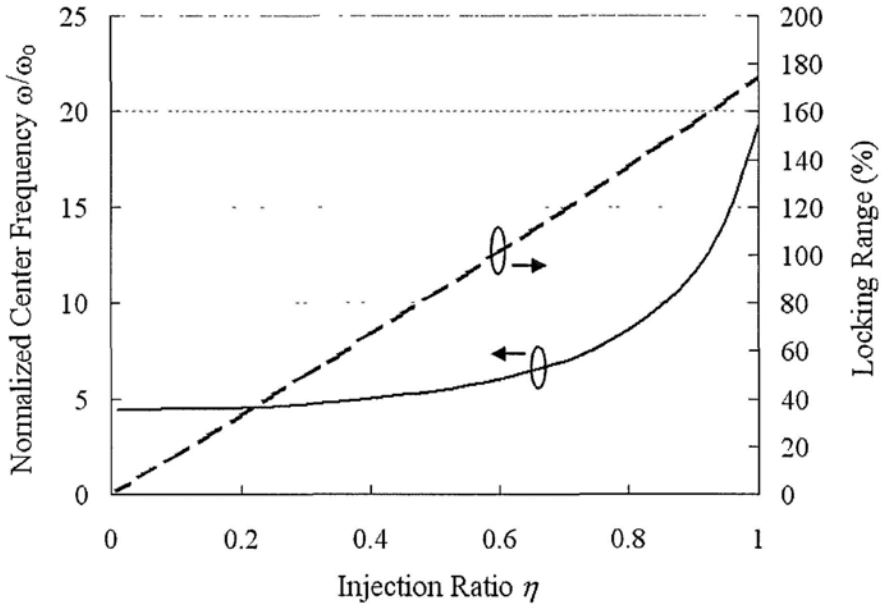


Figure 4.17 Normalized center frequency and locking range for various injection ratios

The term $\frac{4}{\pi} I_{DC_1} R$ represents the output amplitude at free running. In order to satisfy the gain condition, the following inequality holds:

$$1+\frac{4}{15}\eta\left[3\sin(4\phi)-\sqrt{2}\cos(4\phi)\right]\geq 1 \quad or \quad 3\sin(4\phi)-\sqrt{2}\cos(4\phi)\geq 0 \tag{4.25}$$

From Equation 4.25, the possible values of ϕ for stable oscillation can be found and so as the corresponding valid operation frequencies. Figure 4.18 depicts the corrected normalized center frequency and locking range with respect to different injection ratios. Simulation verification is also shown for comparison and good agreement can be seen. Since the maximum operation frequency is limited by the gain condition, the center frequency drifts to lower frequency as injection ratio increases.

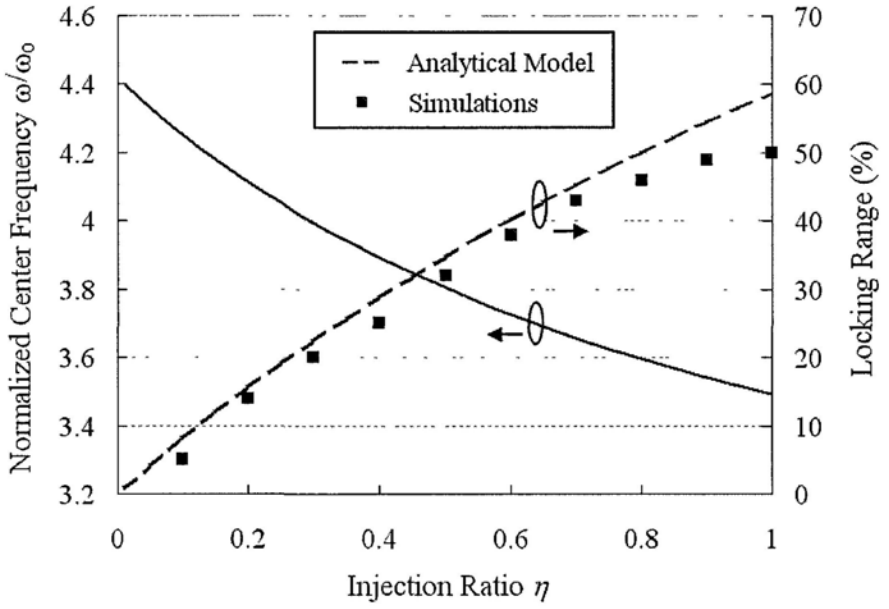


Figure 4.18 Normalized center frequency and locking range versus injection ratio with simulation result comparison for the quadrature-input coherent-coupling dual divide-by-4 ILFD

4.3 Multiplexer

The main functionality of the multiplexer is to select the appropriate phase correctly and promptly without producing output glitches; otherwise wrong division ratio results. Figure 4.19 presents the multiplexer architecture. In addition to an 8-to-1 multiplexer, a phase-selection control circuitry [92] is introduced to assure that only one of the input phases from the dual divide-by-4 ILFD is selected and no glitches happen during phase switching.

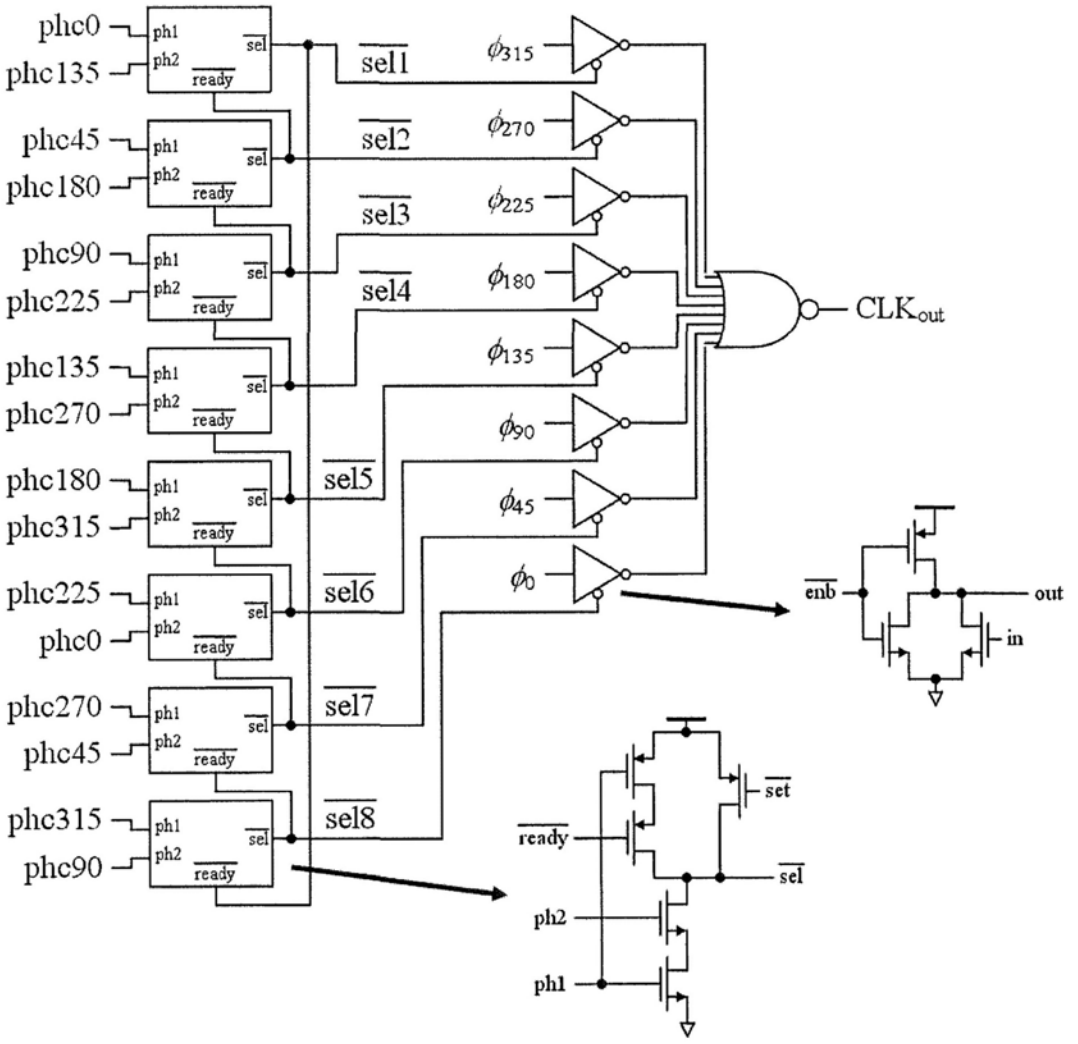


Figure 4.19 Schematic of the multiplexer

The 8-to-1 multiplexer consists of an 8-input NOR gate for signal summation and eight inverters for buffering and selecting the input phases (i.e. $\phi_0 - \phi_{315}$) from the dual divide-by-4 ILFD. To enhance speed under low supply voltage, pseudo logic design is employed. Although pseudo logic gates consume static power, they response faster and their gate delay is smaller. Furthermore, the proposed multiplexer structure is much simpler and effective than the conventional multiplexer implemented by NAND gates in tree structure.

In the conventional design, the input signal needs to propagate through six NAND gates to the output while it just passes two logic gates in the proposed design. Fewer logic gates are involved and consequently the total power consumption and gate delays are less when pseudo logic gates are used.

The phase-selection control circuitry composes of eight inverter stages, forming a ring structure. Inputs from the phase-switching control circuitry (i.e. phc0 – phc315) are used to determine the logic level of the enable signals (i.e. $\overline{\text{sel1}}$ – $\overline{\text{sel8}}$). Only one of the enable signals is Lo, which indicates the associated input phase is selected. An additional "ready" signal is introduced in each stage to identify whether the transition to next stage is completed before disabling the selection of previous stage. This avoids glitches happened during phase transition even when there is timing mismatch in the inputs from the phase-switching control circuitry. The employed scheme also provides high tolerance to variations of gate delay and transition time in digital logic circuits.

A smooth transition example for phase selection is illustrated in Figure 4.20. When both phc0 and phc135 are Hi, $\overline{\text{sel1}}$ is Lo and ϕ_{315} is selected to the multiplexer output. Afterwards, phase switching occurs when phc180 becomes Hi. Finite time is required for $\overline{\text{sel2}}$ toggles from Hi to Lo. As long as $\overline{\text{sel2}}$ is changing to Lo, $\overline{\text{sel1}}$ remains Lo even phc0 changes to Lo. $\overline{\text{sel1}}$ cannot charge up to Hi because the PMOS connected to $\overline{\text{ready}}$ is turned off by $\overline{\text{sel2}}$. This ensures $\overline{\text{sel1}}$ is not disabled too early if phc0 accidentally changes to Lo earlier than the arrival of phc180 becoming Hi. Once $\overline{\text{sel2}}$ is identified as Lo, ϕ_{270} is selected to the multiplexer output and $\overline{\text{sel1}}$ can be transited to Hi to deactivate

the phase selection of ϕ_{315}. It can be observed that the employed scheme guarantees the phase-switching process is smooth and any abrupt change of multiplexer output due to de-selection of all phases is completely avoided.

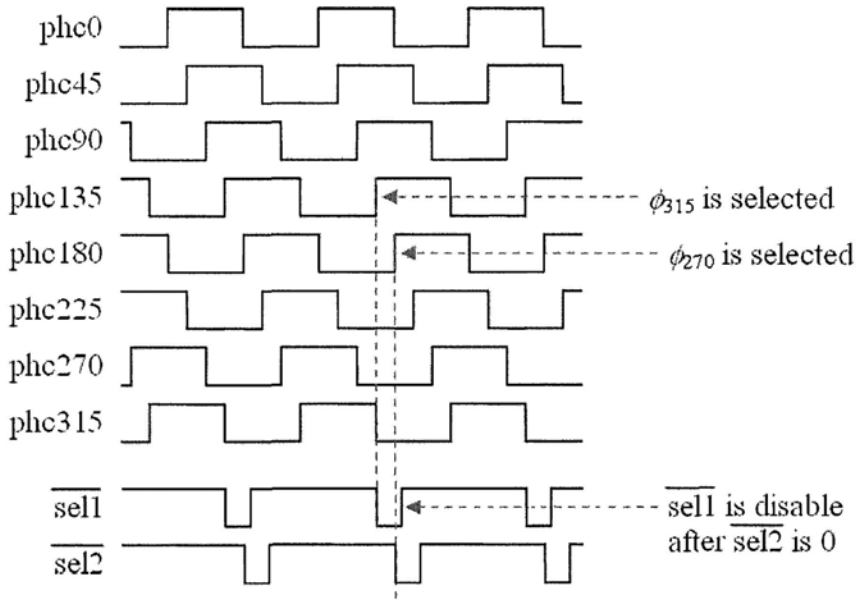


Figure 4.20 Timing diagram of phase selection

4.4 Phase-Switching Control Circuitry

The phase-switching control circuitry consists of two parts: an 8-bit shift register and a combinational logic circuitry. The shift register, whose schematic is shown in Figure 4.21, is constructed with eight D-latches in cascade and the last stage outputs are twisted and fed back to the first stage inputs to form a closed loop. The eight D-latches are grouped into four master-slave D-flip-flops, forming a 4-bit synchronous counter. The D-flip-flop differential outputs are then used to control the phase selection in the multiplexer. The

shift register clock input comes from the combinational logic circuitry. When a clock pulse is generated by the combinational logic circuitry, the shift register toggles to next state and the multiplexer selects the corresponding phase to the output. Conventional D-latch structure with regenerative load is used in the shift register because it has no static power consumption, but fast transition time.

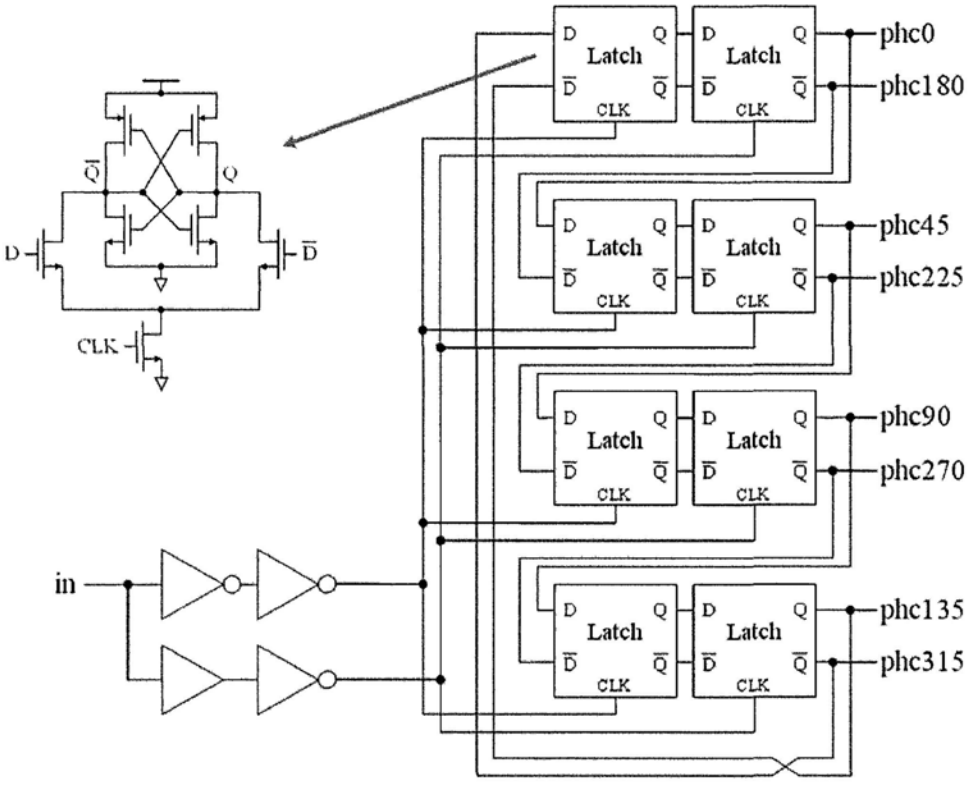


Figure 4.21 Schematic of the shift register in the phase-switching control circuitry

The combinational logic circuitry is used to control state propagation in the shift register when performing phase switching operation. It is implemented in two-level tree structure of NOR gates and its schematic is displayed in Figure 4.22. The mode control bits (b0 – b3) enable/disable the associated NOR gates to specify the phase-switching occurrence in

each cycle for corresponding division ratios. The outputs of the six divide-by-2 stages in the TSPC divide-by-64 ripple counter (i.e. /8, /16, /32, /64, /128, /256 and their complements) are fed to the combinational logic circuitry to determine the proper timing for triggering the shift register advancing to next state. In circuit implementation, the NOR gates are realized as pseudo logic to enhance their operation speed. The PMOS transistor stacking in multi-input NOR gates is thus removed. The parasitic capacitance decreases significantly and the output rise time is not limited by the long stack of PMOS transistors. As a tradeoff, static power consumption increases.

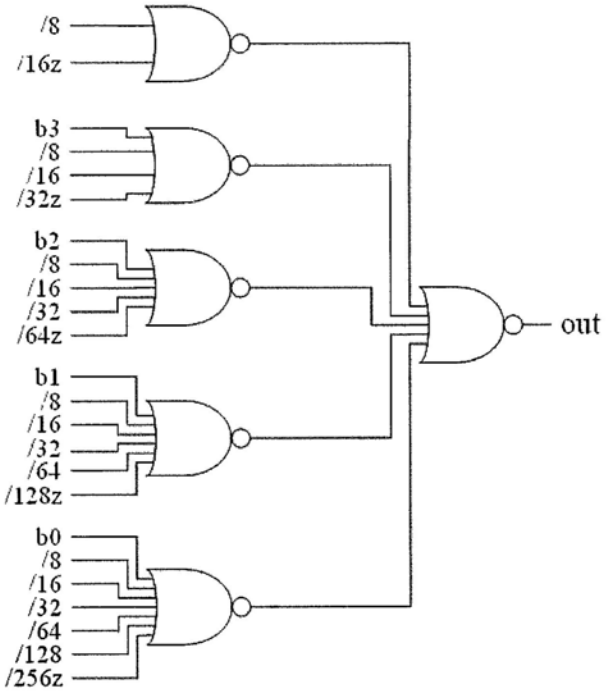


Figure 4.22 Schematic of the combinational logic in the phase-switching control circuitry

4.5 TSPC Divide-by-64 Ripple Counter

The schematic of the divide-by-64 ripple counter is presented in Figure 4.23. Six divide-by-2 frequency dividers are connected in a chain to obtain the overall division ratio of 64. Each divide-by-2 stage can be easily implemented by a D-flip-flop with its complement output fed to its data input. Since the output of the previous stage becomes the clock input of the next stage, the operation frequency deduces by half in next stage. Size scaling is then applied to successive divide-by-2 stages to reduce power consumption. When compared with the synchronous counter with same division ratio, the input clock loading of this ripple counter is minimized as the input clock only drives the first divide-by-2 stage (i.e. DFF1).

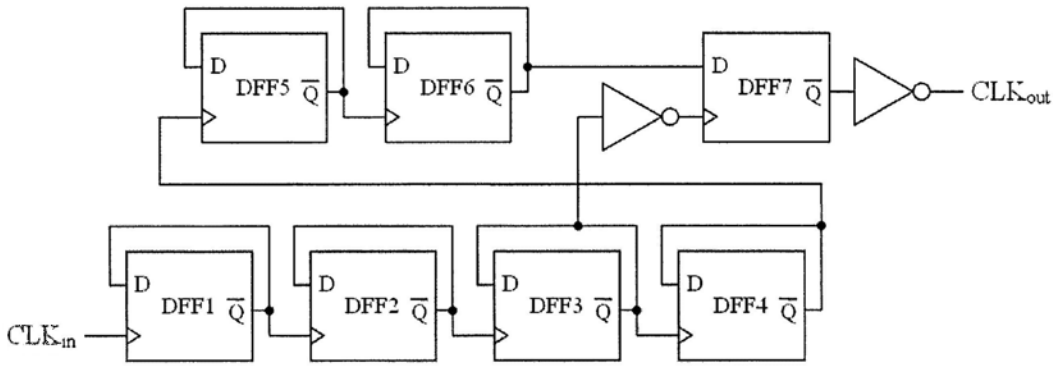


Figure 4.23 Schematic of the TSPC divide-by-64 ripple counter

The major drawback of ripple counters is jitter accumulation [93]. Because of the asynchronous nature, jitters contributed by all divide-by-2 stages are accumulated through the whole circuit. In order to suppress jitter accumulation, resynchronization technique is employed. DFF7 in the ripple counter is used to resample the divide-by-64

output. For the best jitter suppression, the input clock of the ripple counter should be used to trigger DFF7. In this way, the overall jitter will be contributed by the input clock and DFF7 only. Nevertheless, it is practically impossible to guarantee proper sampling of the divide-by-64 output by DFF7 when driven by the input clock. Since their frequency difference are large (64 times in this design) and each stage delay is affected by variations of power supply, temperature and process etc, the timing relationship between the divide-by-64 output and the input clock is rather difficult to control. As a compromise, DFF7 is driven by the third divide-by-2 stage output, whose frequency is 8 times higher than that of the divide-by-64 output. The jitters contributed by the last three divide-by-2 stages are hence eliminated.

The D-flip-flops used in the ripple counter is constructed in TSPC logic, which is advantageous to alleviate the clock skew problem and provide a rail-to-rail output for logic operation. Figure 4.24 shows its schematic, which belongs to Yuan-Svensson D-flip-flop [94]. Since only a single clock is needed, no clock skew exists and higher operation frequency can be achieved. On the other hand, for operation speed optimization, parasitic junction capacitances should be minimized in the layout. For the transistor stack, the transistors can be laid out in parallel strips and the drain/source areas are shared without contacts [95].

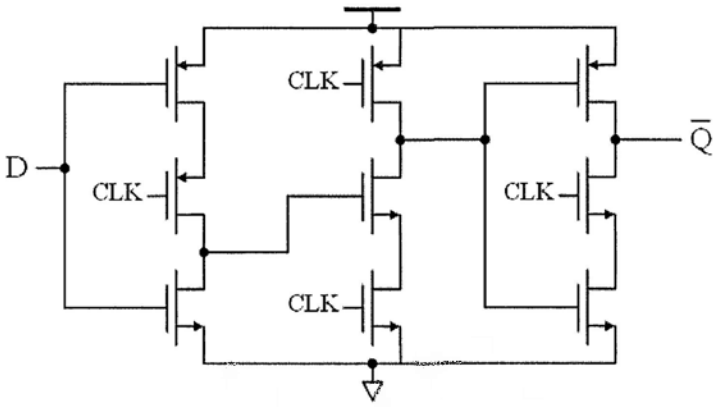


Figure 4.24 Schematic of the TSPC D-flip-flop used in the divide-by-64 ripple counter

CHAPTER 5

CIRCUIT IMPLEMENTATION OF OTHER BUILDING BLOCKS

5.1 Quadrature *LC* Voltage-Controlled Oscillator

Figure 5.1 depicts the schematic of the quadrature voltage-controlled oscillator (QVCO), which belongs to the parallel-coupled type [96]. There are two identical *LC* VCOs with negative transconductance cells to compensate the *LC* tank loss. The coupling transistors are connected in parallel with the negative transconductance cells for generating quadrature output phases. The left VCO core is cross coupled to the right one, and the right VCO core is directly coupled back to the left one. Besides, instead of using a NMOS bias transistor, a PMOS one is chosen in order to suppress its $1/f^3$ phase noise contribution by the flicker noise up-conversion. For the chosen 0.35 μm CMOS process, the PMOS transistor flicker noise is around 3 times less than that of the NMOS transistor.

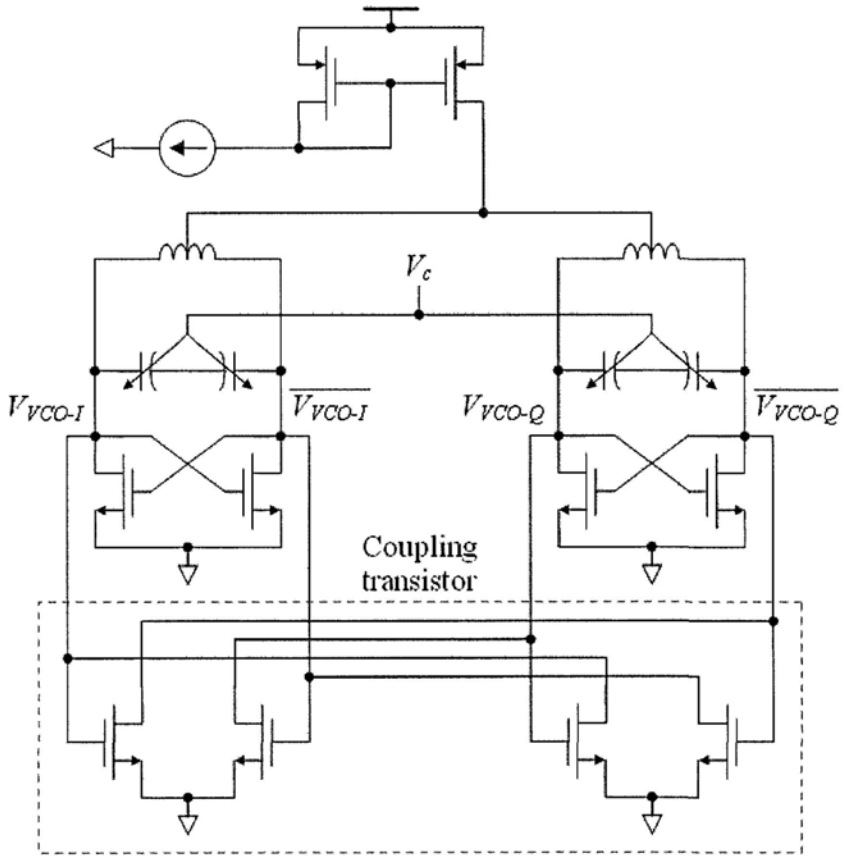


Figure 5.1 Schematic of the quadrature VCO

The bias transistors of the two *LC* VCOs are merged in this design. This modification does not alter the functionality and the small-signal circuit model of the QVCO, but its large-signal behavior is considerably different [97], [98]. Oscillation is enhanced with higher output amplitude at same current consumption due to the supply of excess current from the other core. Phase noise is thus improved [99] without increasing power dissipation. Furthermore, the quadrature accuracy of the proposed QVCO is also less immune to the component mismatches. For the traditional parallel-coupled QVCO, there is a tradeoff between its quadrature accuracy and phase noise [100]. Large coupling transistor size is advantageous for good quadrature phase matching at the expense of

increased power consumption and phase noise. Due to the improvement of component mismatches immunity introduced by the bias transistor combination, the size of the coupling transistors can be reduced to minimize their phase noise contribution and to increase the QVCO frequency tuning range.

To achieve low phase noise, a *LC* tank with high quality factor is desirable, but the lossy monolithic spiral inductor in CMOS technology is usually the bottleneck. The differential inductor [101] is one of the approaches to improve the quality factor of the monolithic spiral inductor in silicon. Compared with two single spiral inductors, it offers better quality factor, higher self-resonance frequency and smaller chip area. Since the differential inductor is used in a balanced configuration, the parasitic capacitance at the center tap is cancelled out, leading to higher differential self-resonance frequency and differential quality factor. The mutual coupling between the coils increases too, which increases the inductance with reduced chip area. As mentioned in [99], high *L/C* ratio is beneficial because the *LC* tank can reject stronger any phase deviation, resulting in less phase noise. But, the required QVCO frequency tuning range limits the maximum value of *L/C* ratio. On the other hand, the top metal thickness for the chosen 0.35 μm CMOS technology is less than 1 μm and the achievable quality factor is around 5.

The frequency tuning scheme of the proposed QVCO consists of coarse and fine tuning to achieve wide frequency tuning range and low VCO gain for good spurious and phase noise performance. The coarse frequency tuning is employed by using a three-bit binary-weighted switched capacitor array (SCA) [102], whose schematic is shown in Figure 5.2. Each branch consists of a poly1-poly2 capacitor and a NMOS switch transistor. To

improve matching, equal size unit capacitor is used. The most significant bit (MSB) contains 4 units while the second MSB and the least significant bit (LSB) have 2 units and 1 unit respectively. The total capacitance value can then be varied digitally by turning on/off the MOS switches, but the finite turn on resistance of the NMOS switch transistor limits the SCA quality factor. High quality factor can only be acquired by increasing the transistor width, which reduces the turn on resistance, but increases the parasitic capacitances simultaneously. The drain-to-bulk and drain-to-gate capacitances are connected in series with the unit capacitance and affect the achievable minimum capacitance of the SCA when all NMOS switch transistors are off. For increasing the transistor width to obtain higher quality factor of the SCA, the QVCO frequency tuning range is sacrificed as the increased parasitic capacitance diminishes the achievable maximum to minimum capacitance ratio of the SCA.

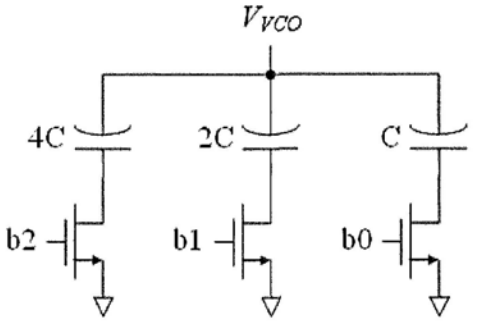


Figure 5.2 Schematic of the switched capacitor array

The NMOS switch transistors are drawn as donut transistors [103] to further reduce their drain-to-bulk capacitance in order to enlarge the achievable maximum to minimum capacitance ratio without sacrificing the SCA quality factor. An example of donut

transistor is presented in Figure 5.3. The drain area of the donut transistor is surrounded by the circular gate while the source area is at the outer side. Although the source area is larger than that in the normal transistor layout, the increase in the source junction capacitance will not affect the QVCO frequency tuning range because the source is connected to ground.

Figure 5 3 Layout of donut transistor

A MOS varactor [104] is used for fine frequency tuning in the QVCO. Compared with a diode varactor, the MOS varactor achieves higher capacitance control range and better quality factor. Furthermore, the quality factor of a diode varactor drops rapidly when it is forward biased, but it will not happen in the MOS varactor case. Nonlinear capacitance characteristic, which is the main cause for flicker noise up-conversion in the $1/f^3$ phase noise region [105], is the major drawback of using the MOS varactor. Introduction of the SCA for coarse frequency tuning decreases the sensitivity of the capacitance change due to the MOS varactor. Eventually, the VCO gain is lower and the flicker noise up-conversion is less severe.

5.2 Phase Frequency Detector

The phase frequency detector (PFD), whose schematic is depicted in Figure 5.4, consists of two TSPC D-latches, a delayed reset path (AND gate) and inverter chains. The TSPC D-latches and the delayed reset path generate the UP and DOWN signals with variable pulse widths according to the phase error between the input reference clock (CLK_{ref}) and the frequency divider output (CLK_{div}). Three states, i.e. pull-up, pull-down and Hi-Z, are produced to control the current sourcing/sinking of the charge pumps.

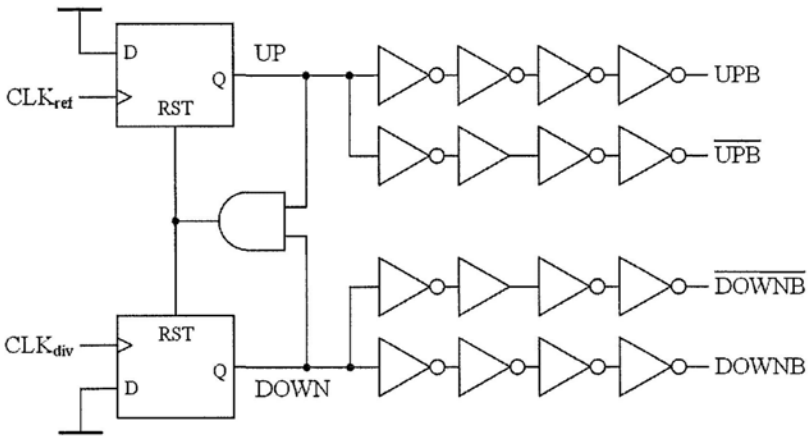


Figure 5.4 Schematic of the phase frequency detector

The chosen PFD architecture is dead zone free. The cause of dead zone in a PFD is due to delay and finite rise/fall time of the digital logic circuit. When the phase error between CLK_{ref} and CLK_{div} is very small, an infinitely short pulse should be generated to control the charge pump. It is impossible to generate such pulse and the charge pump cannot response so rapidly too. As a result, the PFD outputs fail to reflect the true phase error for correction in the phase-locked loop (PLL) operation. The PLL loop seems to be broken

and the in-band phase noise cannot be suppressed and degrades significantly. For the PFD used, as illustrated in Figure 5.5 (case 1), even when CLK_{ref} and CLK_{div} are in-phase, the PFD generates short pulses of finite width for UP and DOWN signals. Since the pulse widths for both signals are the same, the net current outcome of the charge pumps is zero, which corresponds to no phase error. The PFD succeeds in comparing small phase error and so the in-band phase noise does not become worse.

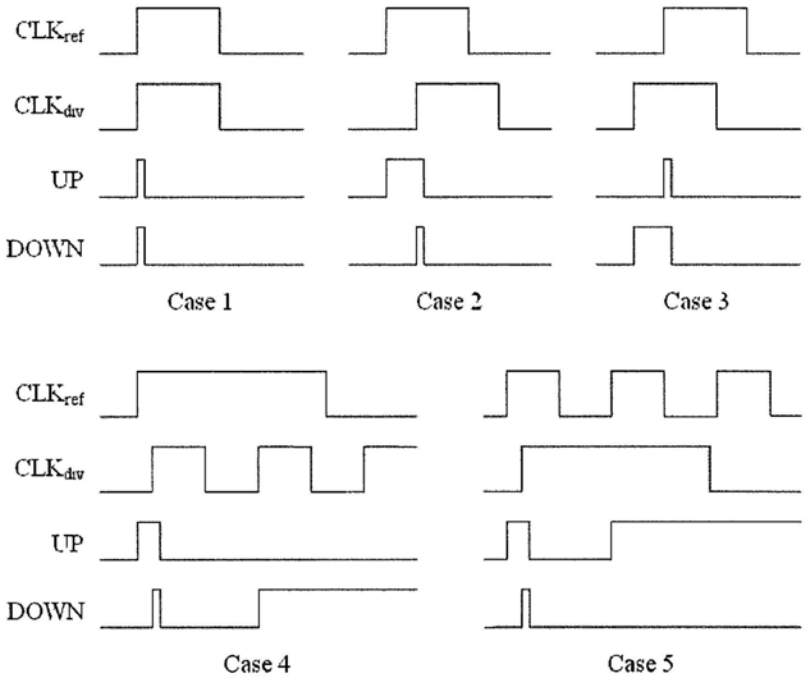


Figure 5.5 Timing diagram of the PFD operation

In contrast to a XOR phase detector, the chosen PFD architecture can detect both phase and frequency errors. Case 2 and 3 in Figure 5.5 present the PFD responses when there are positive (CLK_{ref} leads CLK_{div}) and negative (CLK_{ref} lags CLK_{div}) phase errors respectively. For example, when CLK_{ref} leads CLK_{div}, the PFD controls the charge pumps

to source current to the loop filter to increase the QVCO control voltage. This causes the QVCO to oscillate at higher frequency and hence minimizes the phase difference between CLK_{ref} and CLK_{div}.

Examples of the PFD responses for frequency errors are shown in case 4 and 5 of Figure 5.5. For instance, the frequency of CLK_{div} is higher than that of CLK_{ref} in case 4. At the first rising edge of CLK_{div}, the PFD reacts as if there is positive phase error and longer UP pulse is generated. Afterwards, because the frequency of CLK_{div} is higher, the positive edge of CLK_{div} comes first and triggers a DOWN pulse. Since the positive edge of CLK_{ref} is missing, DOWN signal remains Hi. The QVCO control voltage is thus continuously discharged to decrease the oscillating frequency to minimize the frequency error.

Figure 5.6 depicts the schematic of the TSPC D-latch [106] used in the PFD. Compared with the conventional ones [107], the first stage is omitted since the D-latch input is always Hi. The chosen D-latch is positive-edge triggering and half-transparent. When both input clock (CLK) and reset signal (RST) are Lo, node A is charged to Hi while node B is unaltered (the PMOS is off as node A is Hi and the NMOS controlled by CLK is off too). Until CLK changes to Hi, node B is discharged and output Q toggles to Hi. On the other hand, the reset operation is asynchronous. Once RST switches to Hi, node A is shorted to ground, node B is pull-up to Hi and output Q resets to Lo. The discharge time of node A determines the reset time of the D-latch.

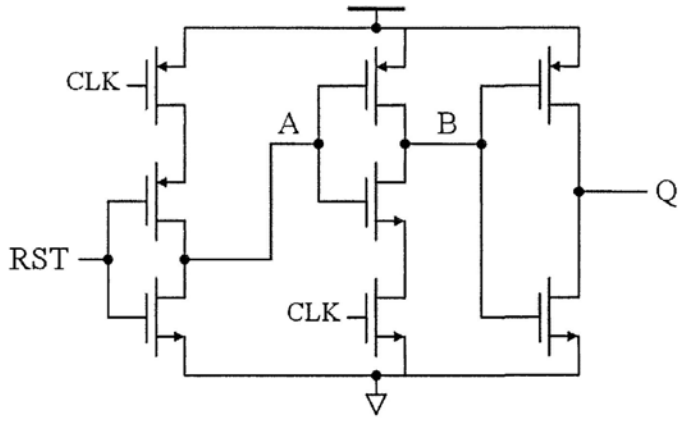


Figure 5.6 Schematic of the D-latch in the PFD

5.3 Charge Pump

Figure 5.7 shows the schematic of the charge pumps and their bias circuit. Unlike in the standard design, there are two charge pumps, which are driven by the same UP and DOWN signals and their complements from the PFD. Their current flow directions are complementary and their current levels are different by B_{CP} times, which are used to control the compensation zero location for PLL loop stability.

In order to acquire fast switching time, current steering technique [108] is employed in the charge pump design. During normal operation, currents are sourced to/sunk from the loop filter through the charge pump outputs (i.e. I_{CPz} and I_{CPp}), depending on the UP and DOWN signal control from the PFD. When both UP and DOWN signals are Lo, the charge pump currents flow through the dummy branches instead. This keeps the PMOS and NMOS current source transistors always in saturation. The high current spike

problem occurred at rise edges of the UP and DOWN signals for the conventional charge pump with drain switching is thus significantly suppressed as the current source transistors do not operate in triode region when switching on. Moreover, since the DC voltage levels at I_{CPz} and I_{CPp} are clamped to V_{ref} by the loop filter, The drain-source voltage of the PMOS and NMOS current source transistors remain unchanged when switching between the main and dummy branches, minimizing current mismatch due to the channel length modulation effect.

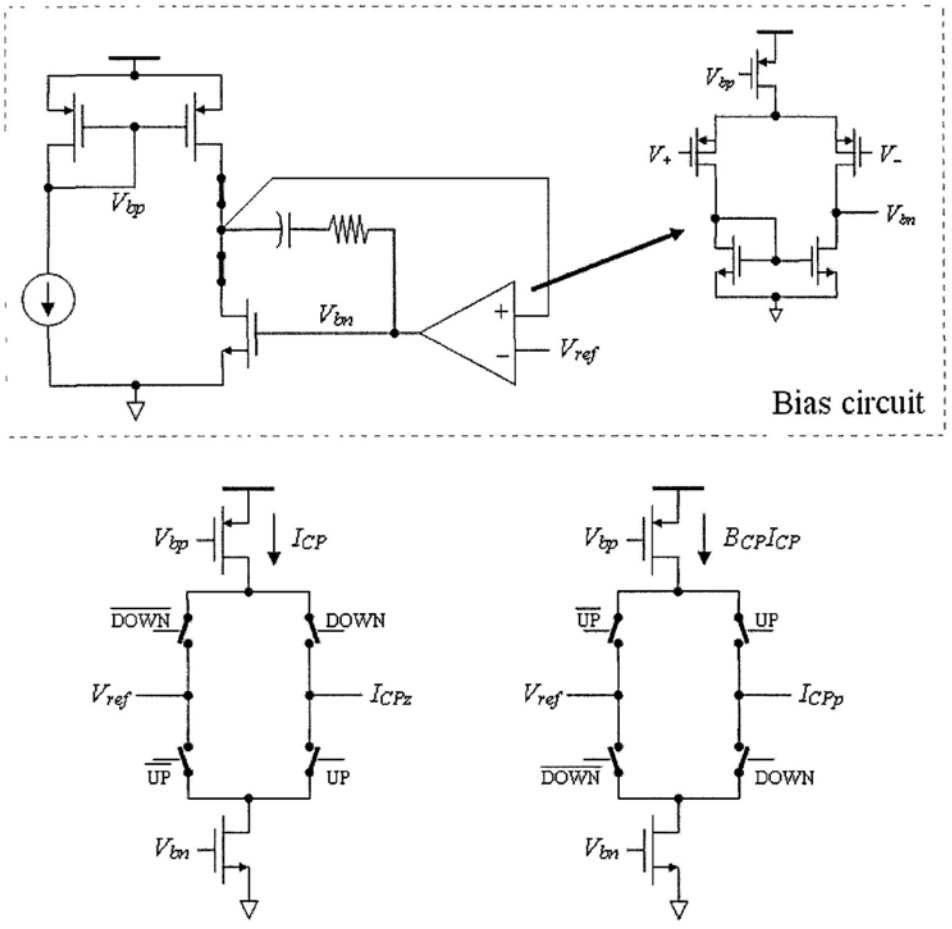


Figure 5.7 Schematic of the charge pumps

To minimize the charge injection and clock feedthrough phenomenon, all switches are implemented as a CMOS transmission gate [109]. Their complementary control signals are adjusted so as to turn on the transistors at the same time. Holes and electrons injected from PMOS and NMOS transistors respectively can then be partially cancelled with each other. Additionally, small switch transistor sizes are preferable to reduce the influences.

To improve the current matching between the PMOS and NMOS current source transistors, the NMOS current source transistor gate bias V_{bn} is generated by using error amplifier [110], as depicted in Figure 5.7. The error amplifier is a single-stage differential amplifier with a PMOS differential pair. The gate bias V_{bn} is regulated autonomously so that V_{DS} of the NMOS bias transistor is roughly equal to V_{ref}. Dummy switches are also inserted to estimate the voltage drop of the switches in the charge pumps.

The proposed error amplifier approach achieves good current matching over a wide range of V_{ref}, as illustrated in Figure 5.8. Due to the channel length modulation effect, the PMOS transistor current decreases as V_{ref} increases. Nevertheless, the NMOS transistor tracks the change well for V_{ref} = 0.2 V to 1.1 V. At the lower end (V_{ref} < 0.2 V), the NMOS current source transistor falls into triode region and thus the current matching is deteriorated. High input common mode voltage (V_{ref} > 1.1 V) is not acceptable for the error amplifier with a PMOS differential pair, degrading its common mode rejection performance. As shown in the inset of Figure 5.8, the simulated current mismatch is less than 0.3 nA (several order of magnitude less than the charge pump current level) for V_{ref} = 0.2 V to 1.1 V.

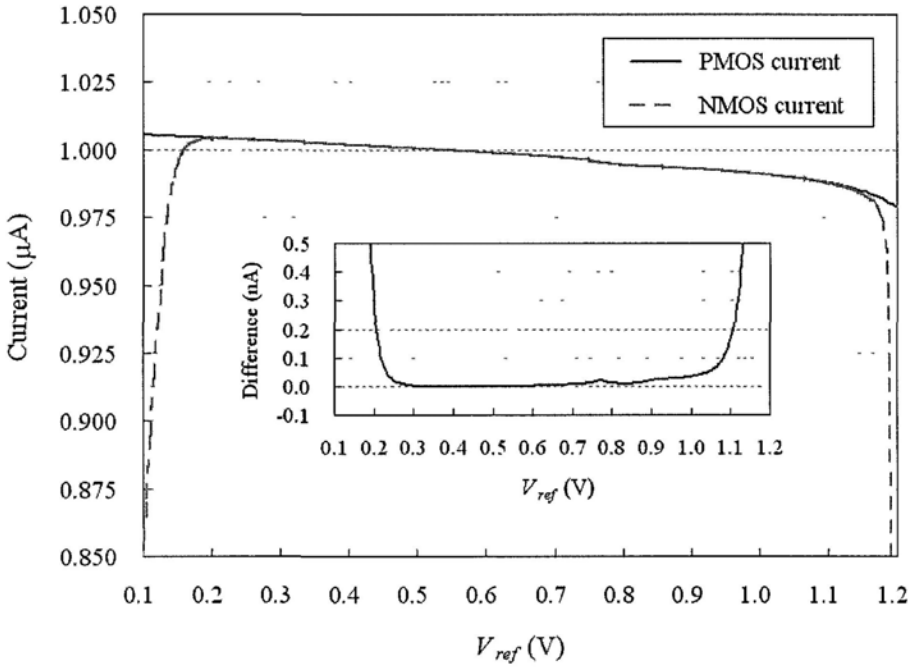


Figure 5.8 Simulated current matching characteristic of the charge pump

5.4 Loop Filter

The loop filter is constructed as a third-order dual-path active loop filter [83], as depicted in Figure 5.9. The two charge pump outputs (i.e. I_{CPz} and I_{CPp}) are connected to the opamp differential inputs in the loop filter. The current pulse I_{CPz} with a nominal value of I_{CP} charges/discharges the feedback capacitor C_z, functioning as an integrator. Another current pulse I_{CPp}, whose typical value is B times larger than that of I_{CPz} and having opposite flowing direction, is supplied to a first-order lowpass filter formed by the combination of R_p and C_p. The opamp is used to perform signal substitution. An additional pole implemented by R_1 and C_1 is inserted at the opamp output for reference

spur rejection and opamp noise suppression. Table 5.1 lists the component values of the loop filter.

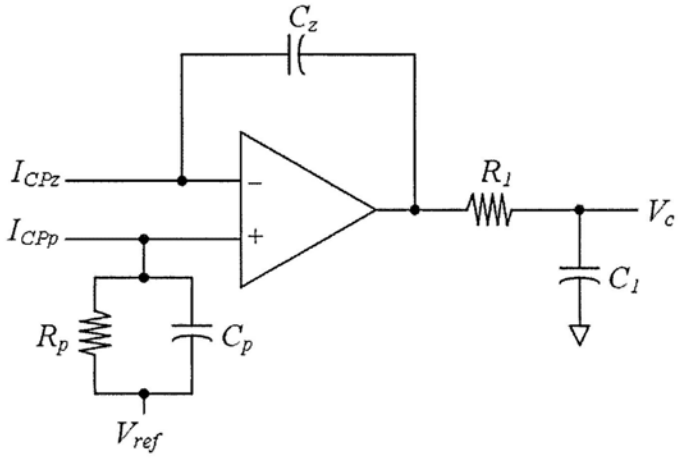


Figure 5.9 Schematic of the loop filter

Component Parameter	R_p	C_p	C_z	R_1	C_1
Value	32.5 kΩ	23.6 pF	11.8 pF	8.1 kΩ	23.6 pF

Table 5.1 Component parameters of the loop filter

The loop filter transfer function is derived as:

$$V_c = \frac{sR_pC_zI_{CPp} - (1+sR_pC_p)I_{CPz}}{sC_z(1+sR_pC_p)(1+sR_1C_1)} \tag{5.1}$$

Since the charge pump outputs follows the relationships:

$$\begin{cases} I_{CPp} = B_{CP} I_{CP} \\ I_{CPz} = -I_{CP} \end{cases} \tag{5.2}$$

Equation 5.1 can be simplified as:

$$V_c = \frac{1 + sR_p\left(C_p + B_{CP}C_z\right)}{sC_z\left(1 + sR_pC_p\right)\left(1 + sR_1C_1\right)} I_{CP} \tag{5.3}$$

According to Equation 5.3, the loop filter transfer function contains three poles (one poles at zero and the other two poles at $\tau_p = R_pC_p$ and $\tau_1 = R_1C_1$ respectively). Its compensation zero location is at $\tau_z = R_p\left(C_p + B_{CP}C_z\right)$, which is not only depend on the RC component values, but also on the charge pump current factor B_{CP}. In this way, the compensation zero location is adjustable and its capacitor size can be reduced approximately by B_{CP} times. In this design, the total capacitor size is less than 60 pF, which is feasible to implement on-chip. For a unit capacitance of 0.86 fF/μm^2 in the chosen 0.35 μm CMOS process, the active area of the capacitors used in the loop filter is less than 0.07 mm^2.

As shown in Figure 5.10, the opamp integrated in the loop filter is a two-stage Miller-compensated operational amplifier. The two bias voltages V_{bp1} and V_{bp2} are generated internally by draining current out of diode-connected transistors, which are not drawn for clarity. The first stage of the opamp is a single-ended differential amplifier with a PMOS differential pair while a common source amplifier is implemented in the second stage. Since the second stage is a gain stage, the overall opamp noise is dominated by the first

stage. Large transconductance is feasible to suppress the thermal noise with the tradeoff of higher power consumption. To minimize the flicker noise, the transistor sizes should be maximized and using a PMOS differential pair is also advantageous.

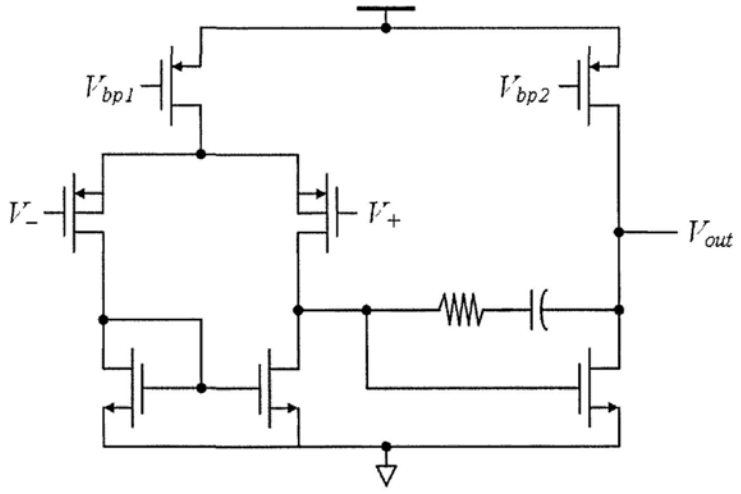


Figure 5.10 Schematic of the opamp in the loop filter

CHAPTER 6

EXPERIMENTAL RESULTS

6.1 IC Fabrication and Measurement Setup

Figure 6.1 shows the overall architecture of the frequency synthesizer for IC fabrication. Two identical pairs of the quadrature voltage-controlled oscillator (QVCO) and frequency divider are implemented. QVCO1 and DIV1 are used to measure the proposed frequency synthesizer performances (such as spurious tones, phase noise and settling time) while QVCO2 and DIV2 are included to verify the phase quadrature accuracy of the QVCO outputs. They can be power-down when not in use. In this way, influence between the two measurement setups is eliminated, the layout is simpler and the QVCO loading is reduced to widen its frequency tuning range. The phase frequency detector (PFD), charge pump (CP) and loop filter are shared to save chip area. The outputs of the frequency dividers are selected through a multiplexer to complete the phase-locked loop (PLL). Additionally, the PFD, charge pump and loop filter can be disabled so as to measure the performances of the QVCO and frequency divider individually in open loop. The on-chip QVCO also serves as a quadrature-input signal source for the frequency divider.

The phase accuracy of the QVCO quadrature outputs is verified by using the conventional image band rejection technique [111]. An on-chip passive single-sideband (SSB) mixer [112] is included in the measurement setup for frequency up-conversion. The IQ baseband signals at 19 MHz are generated by an on-chip four-stage *RC* polyphase filter [113].

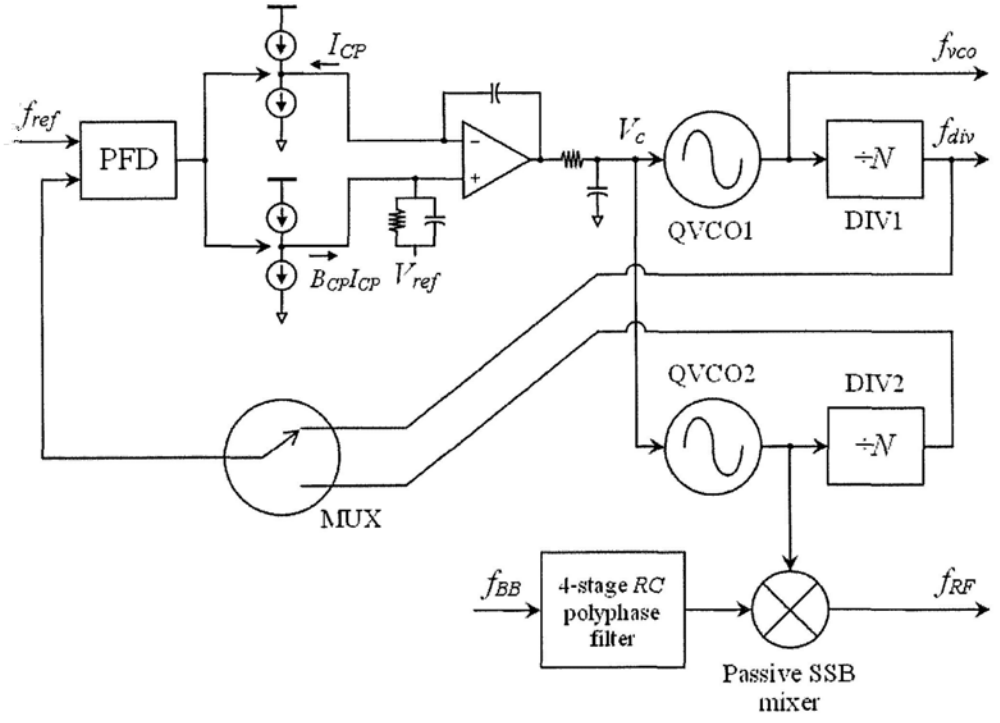


Figure 6.1 Overall architecture of the frequency synthesizer for IC fabrication

Two frequency synthesizer prototypes have been fabricated in a 0.35 μm standard 2P4M CMOS process without the thick top metal option. Their only difference is the design of the dual divide-by-4 injection-locked frequency divider (ILFD) in the programmable fractional frequency divider. In design 1, it is the cross-coupling type while the coherent-coupling dual divide-by-4 ILFD is implemented in design 2. Their microphotographs are

depicted in Figure 6.2 and 6.3 respectively. The core area of both PLL designs occupies 0.70 mm^2.

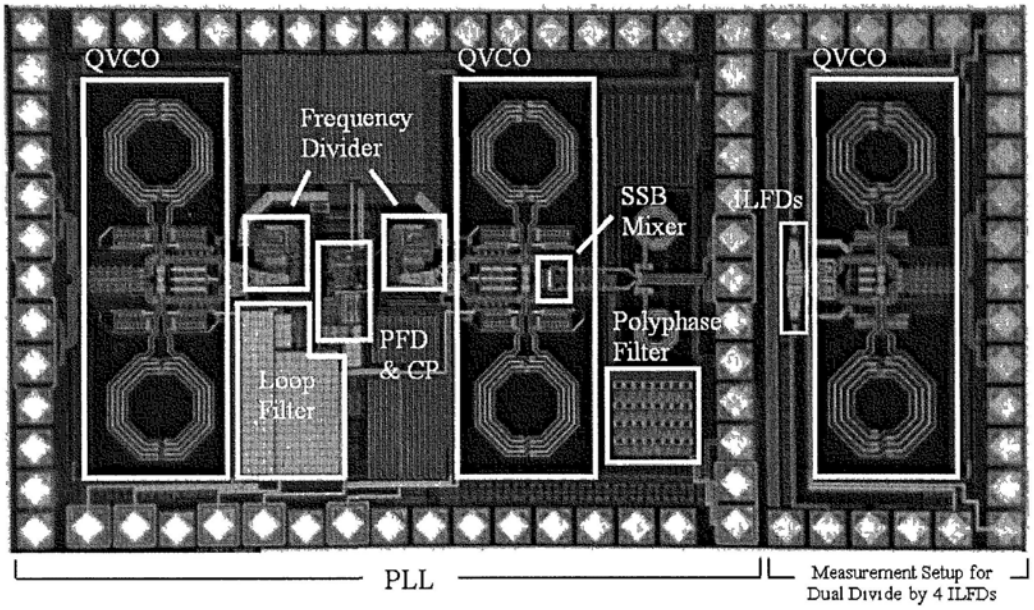


Figure 6 2 Die photo of the proposed frequency synthesizer (Design 1) and the measurement setup for the dual divide-by-4 ILFDs

Circuitries for measuring the cross-coupling and coherent-coupling dual divide-by-4 ILFDs are also fabricated, as shown in Figure 6.2. These two dual divide-by-4 ILFDs are connected to an on-chip QVCO as their input signal source. For each dual divide-by-4 ILFD, their eight outputs are properly loaded in order not to deteriorate their phase matching.

All measurements were performed on standard FR4 gold-plated printed circuit boards (PCBs) and the chips were wire-bonded on them.

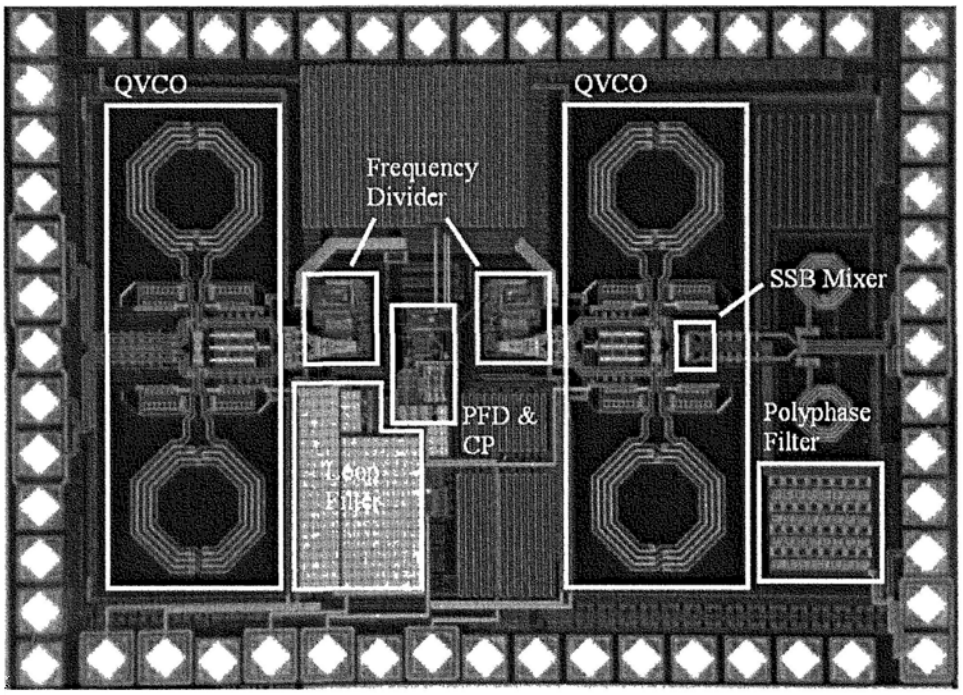


Figure 6.3 Die photo of the proposed frequency synthesizer (Design 2)

6.2 Quadrature *LC* Voltage-Controlled Oscillator

The QVCO characterization was performed by using a HP 4352B VCO/PLL signal analyzer. The PLL is left open loop with the PFD, charge pump and loop filter disabled. The image band rejection measurement setup is also power off to minimize the VCO frequency pulling effect. Only the QVCO (QVCO1) and the frequency divider (DIV1) are switched on. The QVCO control voltage V_c is driven externally by a low noise voltage source provided by the VCO/PLL signal analyzer.

6.2.1 Frequency Tuning Range

Figure 6.4 and 6.5 present the measured frequency tuning range and VCO gain K_{VCO} of the QVCO respectively. The QVCO covers a frequency range from 2.26 GHz to 2.80 GHz. For the three-bit switched capacitor array (SCA) coarse frequency tuning, there are eight tuning curves. Each tuning curve has a frequency coverage range of less than 200 MHz and overlaps with the neighboring ones by approximately 100 MHz. This guarantees no dead zone in frequency tuning over the entire coverage range.

In the 2.4 GHz industrial, scientific and medical (ISM) band, the VCO gain variation is from 90 MHz/V to 140 MHz/V. The deviation is within -25% and 17% of the design value (i.e. 120 MHz/V).

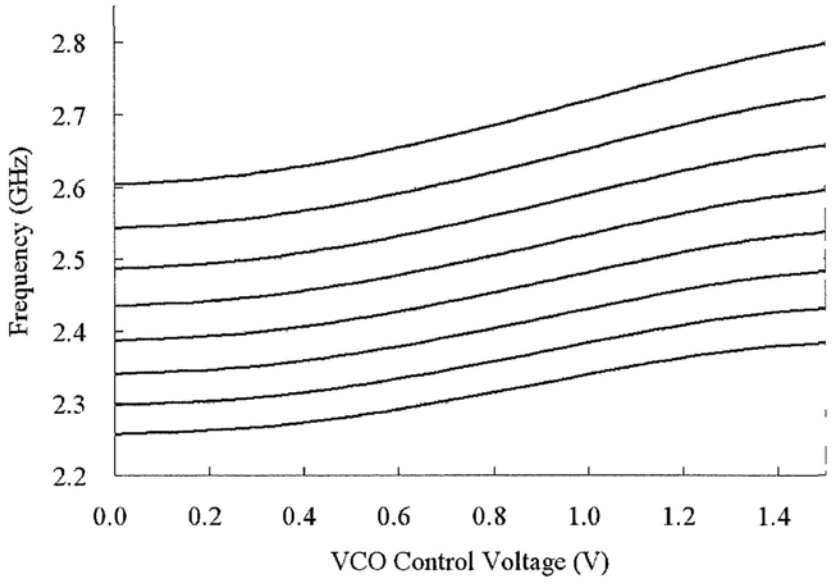


Figure 6.4 Measured frequency tuning range of the quadrature VCO

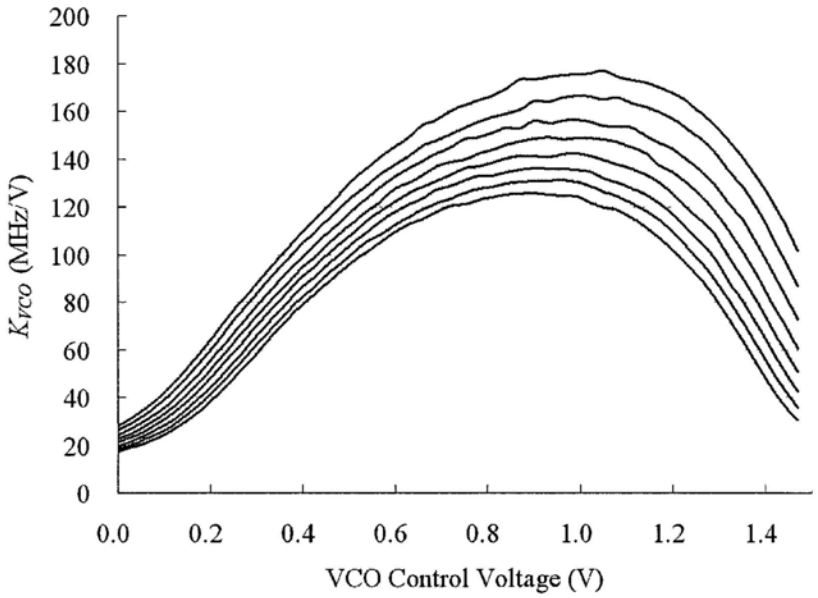


Figure 6.5 Measured VCO gain of the quadrature VCO

Figure 6.6 shows the measured QVCO output spectrum at 2.4 GHz, captured through an Agilent E4470B ESA spectrum analyzer. The output power is -9.6 dBm and no spurious tones are observed.

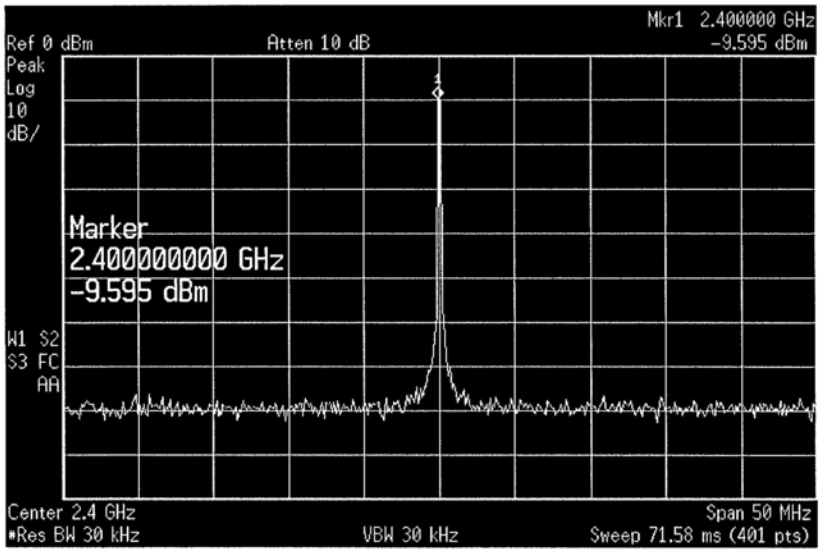


Figure 6.6 Measured output spectrum of the quadrature VCO

6.2.2 Phase Noise

The measured phase noise performance of the QVCO at 2.4 GHz is depicted in Figure 6.7. The $1/f^3$ region due to the $1/f$ flicker noise up-conversion can be identified at low frequency offset, which shows a trend of -30 dB/decade. At around 1 MHz frequency offset, the plot roughly follows the trend of $1/f^2$ region. The measured phase noise at 1 MHz frequency offset is -125.4 dBc/Hz. The measured noise spectrum flattens to noise floor of -140 dBc/Hz at 10 MHz frequency offset. Figure 6.8 shows the measured phase noise at 1 MHz frequency offset for various output frequencies. The variation is within 2 dB.

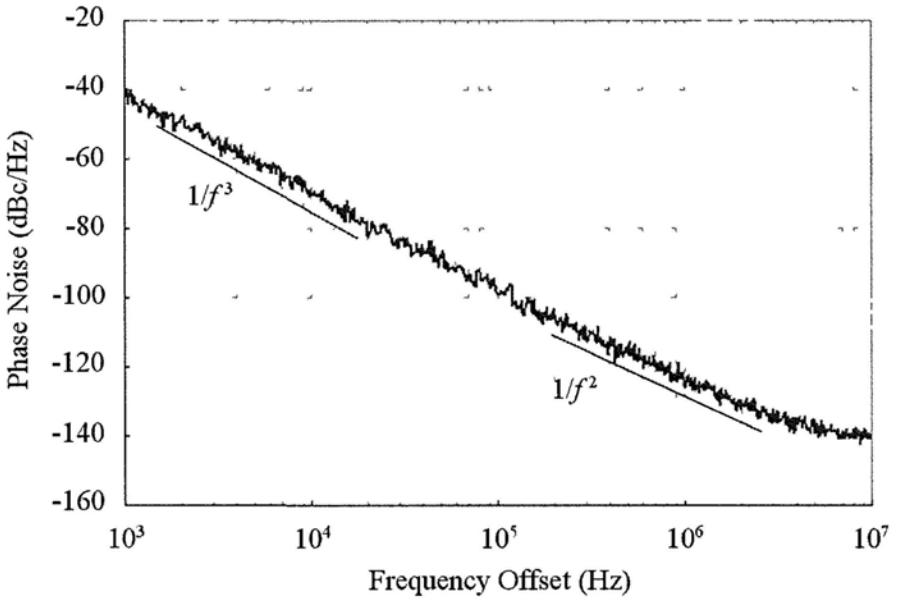


Figure 6 7 Phase noise measurement of the quadrature VCO

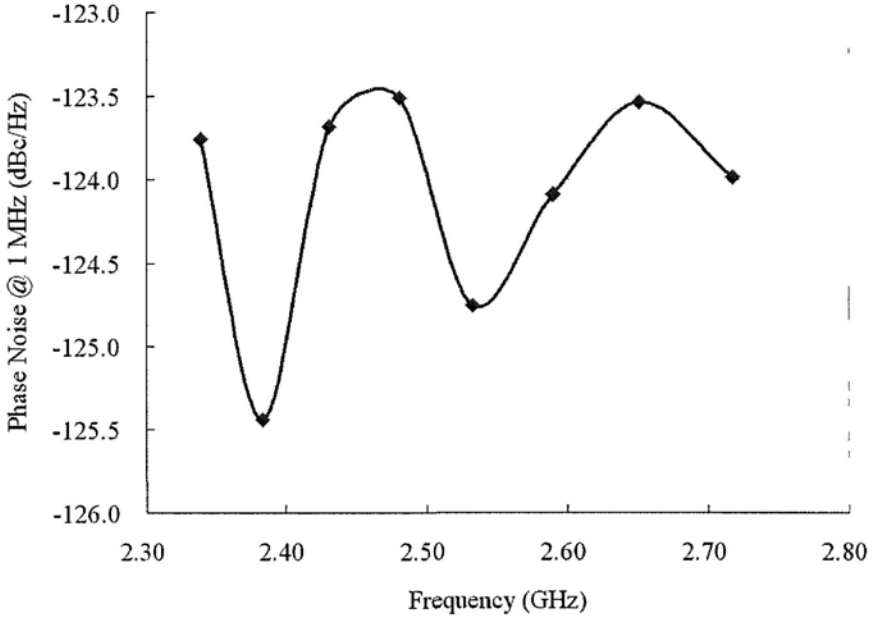


Figure 6.8 Measured phase noise at 1 MHz frequency offset of the quadrature VCO

6.3 Dual Divide-by-4 Injection-Locked Frequency Dividers

For comparison, the cross-coupling and coherent-coupling dual divide-by-4 ILFDs are both connected to an on-chip QVCO as their quadrature-input source. To suppress the frequency pulling phenomenon, the two dual divide-by-4 ILFDs are measured separately (When one of the ILFDs is measured, another is turned off). Their phase noise characteristics were measured through a HP 4352B VCO/PLL signal analyzer. Since the HP 4352B VCO/PLL signal analyzer can only show spectrum with a span of 10 MHz around the center frequency, the output spectra of the dual divide-by-4 ILFDs were measured through an Agilent E4470B ESA spectrum analyzer.

6.3.1 Locking Range

Both cross-coupling and coherent-coupling dual divide-by-4 ILFDs have comparable locking range. At QVCO output power of -8 dBm, the locking range of the cross-coupling dual divide-by-4 ILFD covers from 2.16 GHz to 2.79 GHz while that of the coherent-coupling counterpart is from 2.18 GHz to 2.79 GHz. They are slightly less than the simulated values (around 30% for $\eta \approx 0.5$) because the upper bound of the locking range is limited by the QVCO frequency tuning range, which ranges from 1.91 GHz to 2.79 GHz.

Figure 6.9 and 6.10 show the measured output spectra of the cross-coupling and coherent-coupling dual divide-by-4 ILFDs respectively. At the QVCO output frequency of 2.4 GHz, a frequency tone at 600 MHz is observed at both ILFD outputs, which validates the functionality of frequency division by four.

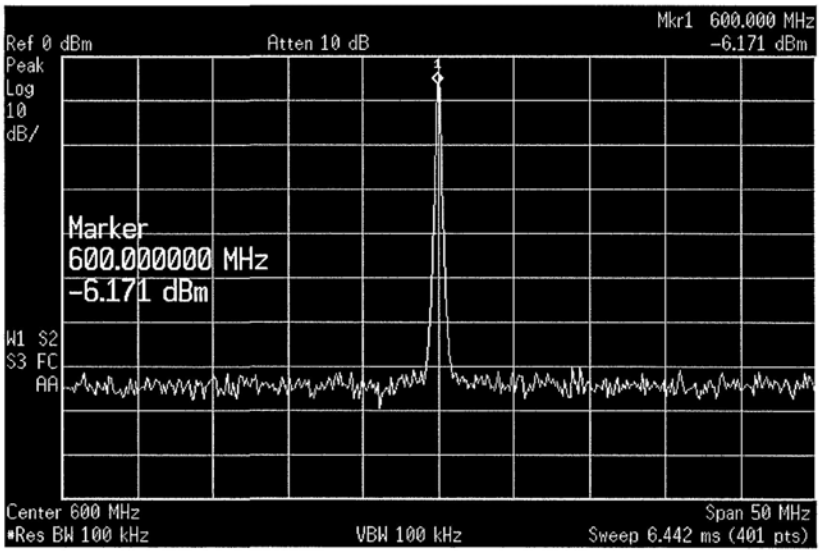


Figure 6.9 Measured output spectrum of the cross-coupling dual divider-by-4 ILFD

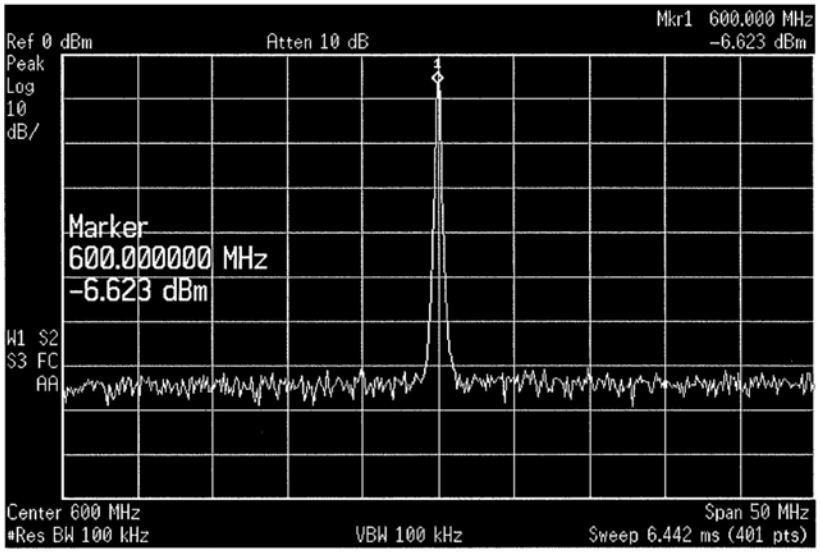


Figure 6.10 Measured output spectrum of the coherent-coupling dual divider-by-4 ILFD

6.3.2 Phase Noise

The phase noise performance of the cross-coupling and coherent-coupling dual divide-by-4 ILFDs are illustrated in Figure 6.11 and 6.12 respectively. The QVCO phase noise characteristic is also included in both figures as reference. The phase noise at 1 MHz frequency offset for the free-running cross-coupling dual divide-by-4 ILFD is -82.30 dBc/Hz. On the other hand, the free-running coherent-coupling dual divide-by-4 ILFD achieves the phase noise of -99.81 dBc/Hz at 1 MHz frequency offset, which has over 17 dB improvement when compared with that of the cross-coupling counterpart. When locked, there is approximately 12 dB reduction in the phase noise between the QVCO output and the dual divide-by-4 ILFD outputs in both designs, as expected due to frequency division by four.

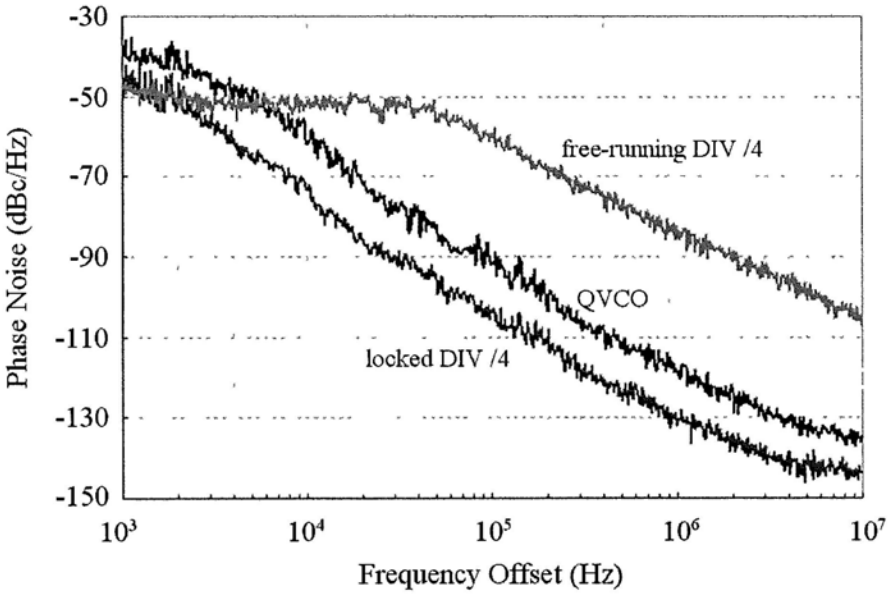


Figure 6.11 Phase noise performances of the QVCO and the cross-coupling dual divider-by-4 ILFD

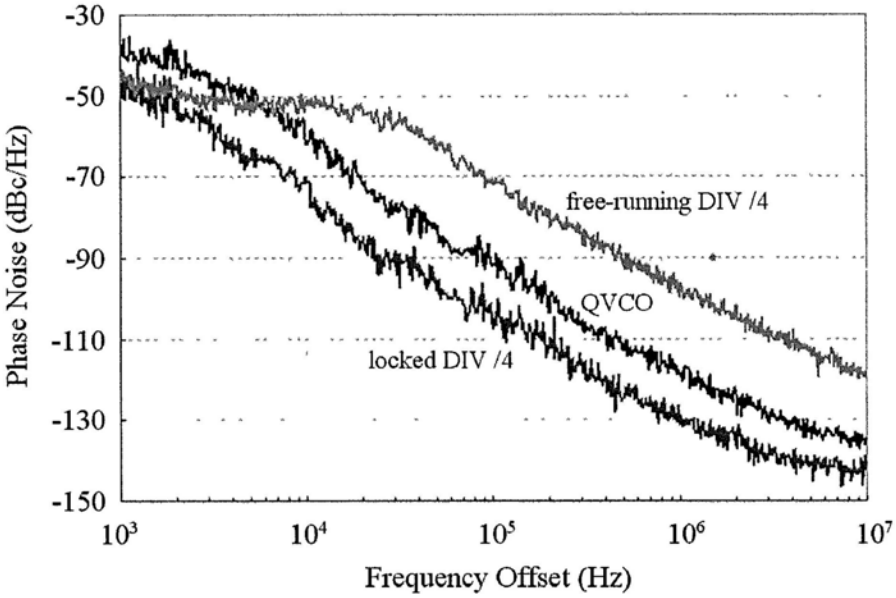


Figure 6.12 Phase noise performances of the QVCO and the coherent-coupling dual divider-by-4 ILFD

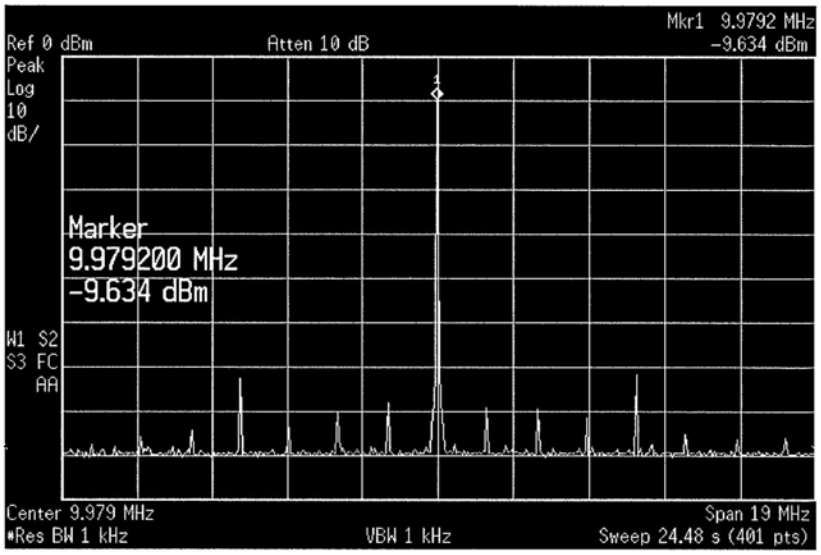
6.4 Programmable Fractional Frequency Dividers

The measurement setup for the programmable fractional frequency dividers is the same as that for the QVCO. All circuit components except the QVCO and the frequency divider are turned off to minimize their influences. The on-chip QVCO serves as a quadrature-input source for the frequency divider and its coarse and fine tuning circuitries are used to vary its oscillating frequency. The output spectrums of the frequency dividers were captured through an Agilent E4470B ESA spectrum analyzer while their phase noise performances were measured through a HP 4352B VCO/PLL signal analyzer.

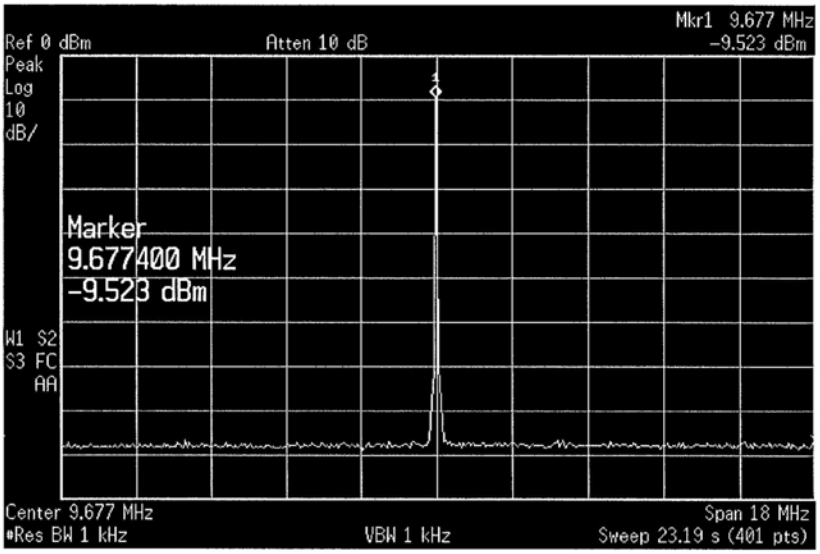
6.4.1 Locking Range

At the QVCO output power of -10 dBm, the proposed frequency dividers with the cross-coupling dual divide-by-4 ILFD acquires an operation range from 2.24 GHz to 2.70 GHz while that with the coherent-coupling counterpart is from 2.26 GHz to 2.67 GHz. Both frequency dividers feature programmable division ratios from 240.5 to 248. At the input frequency of 2.4 GHz, the divider output frequencies f_{div}, as shown in Figure 6.13 and 6.14, match the expected values for division ratios of 240.5 (9.9792 MHz) and 248 (9.6774 MHz) respectively in both designs. Spurious tones at multiples of $f_{div}/8$ frequency offsets are observed for the fractional division cases in Figure 6.13(a) and 6.14(a) due to the phase mismatches [85] of the multi-phase signals of the dual divide-by-4 ILFDs. The highest spurious tone is less than -65 dBc at $\pm f_{div}/2$ frequency offset in both designs.

Besides, for the integral division cases in Figure 6.13(b) and 6.14(b), no spurious tones are observed because the influence of the phase mismatch between the divide-by-4 ILFDs is cancelled out due to even number of phase switching occurrence.

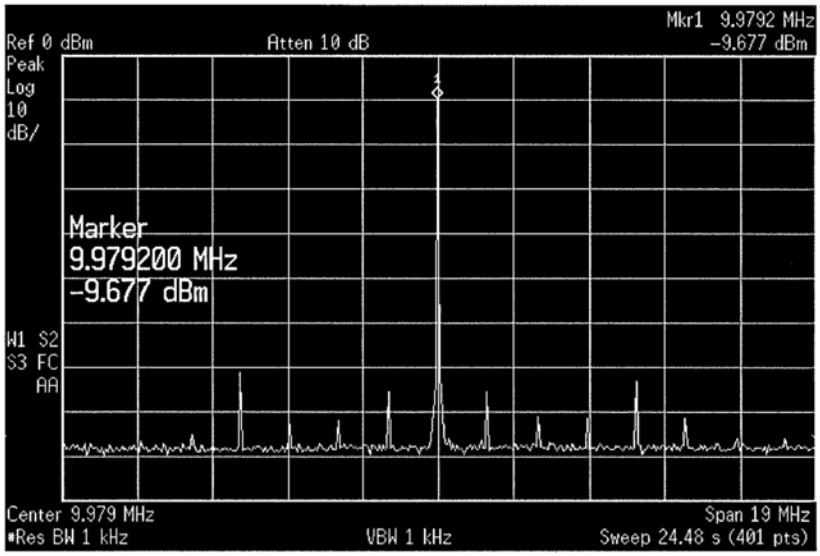


(a)

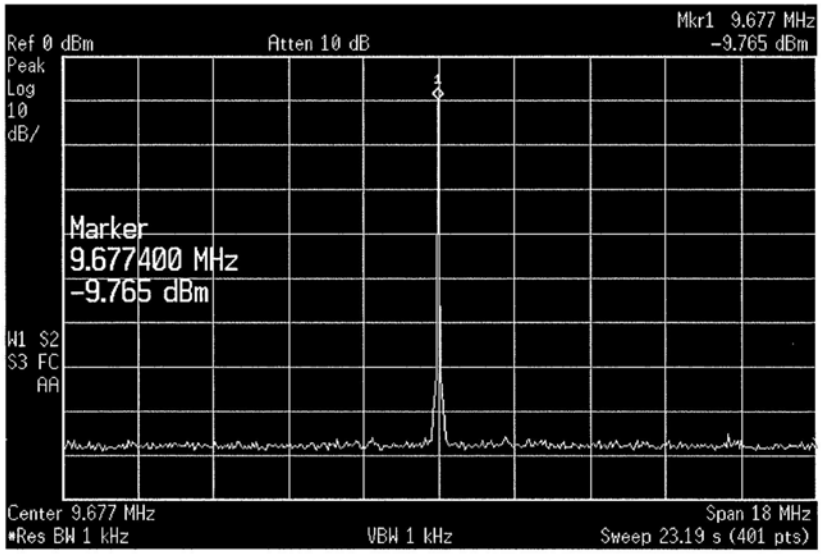


(b)

Figure 6.13 Measured output spectrum of the frequency divider with the cross-coupling dual divide-by-4 ILFD for division ratios of (a) 240.5 and (b) 248



(a)



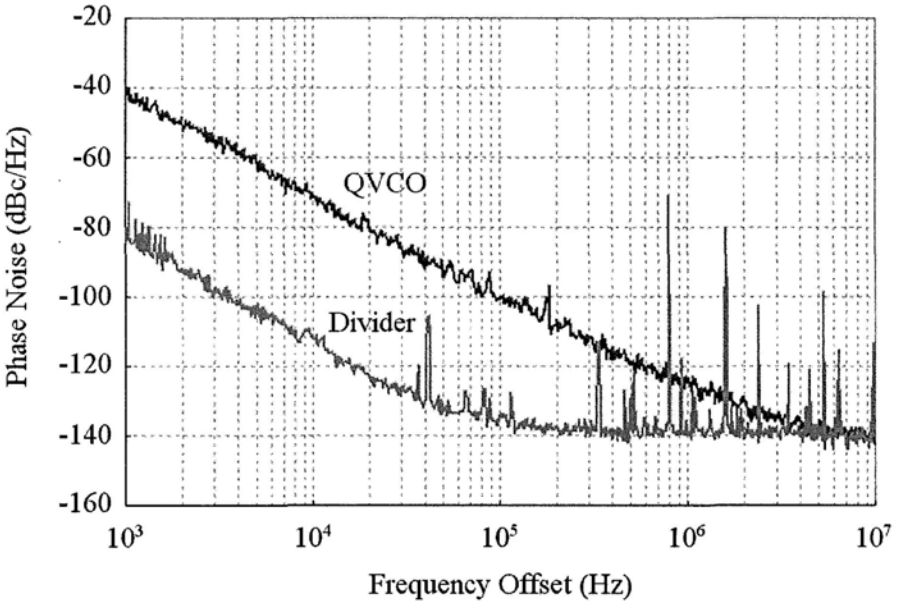
(b)

Figure 6.14 Measured output spectrum of the frequency divider with the coherent-coupling dual divide-by-4 ILFD for division ratios of (a) 240.5 and (b) 248

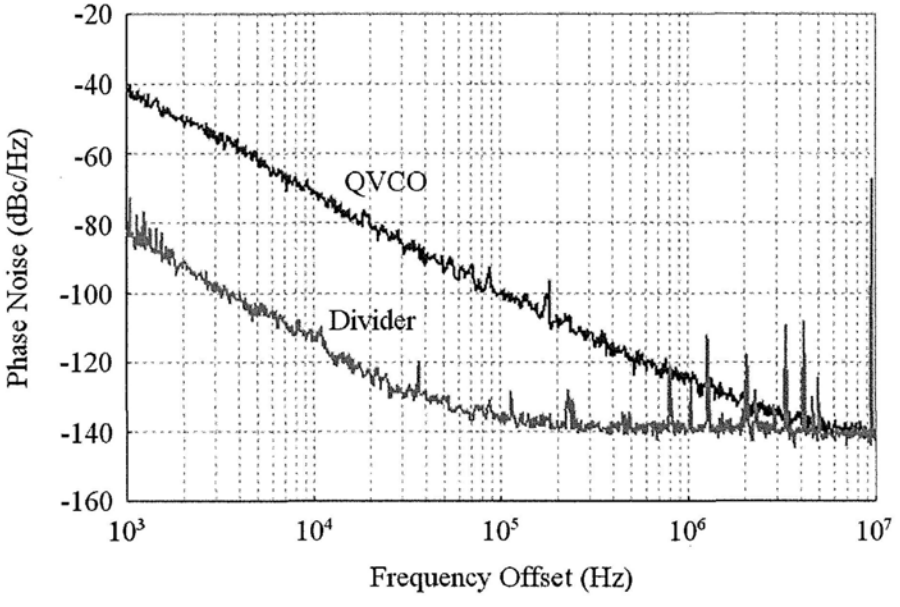
6.4.2 Phase Noise

The phase noise performances of the proposed frequency dividers with the cross-coupling and coherent-coupling dual divide-by-4 ILFDs are presented in Figure 6.15 and 6.16 respectively. The QVCO phase noise characteristic is also displayed. At low frequency offset, the phase noise improvement between the QVCO output and the frequency divider outputs is approximately 43 dB, which is slightly different from the theoretical values of 47.6 dB and 47.9 dB for division ratios of 240.5 and 248 respectively. The discrepancy is mainly due to the noise contributed by the frequency dividers. Besides, the thermal noise contributed by the frequency dividers starts to dominate at around 100 kHz frequency offset and hence the phase noise spectra flatten to the noise floor of -140 dBc/Hz.

In both designs, when compared between the phase noise spectra for different division ratios, there are fewer spurious tones in the case for the division ratio of 248. Since the divide-by-64 TSPC frequency divider, phase-switching multiplexer and control circuitry in the proposed frequency divider are single-ended, they are more susceptible for switching noise. Furthermore, the number of times for phase switching to achieve division ratio of 248 is less than that for division ratio of 240.5 in the backward phase-switching scheme. Consequently, less switching noise is induced to the frequency divider output.

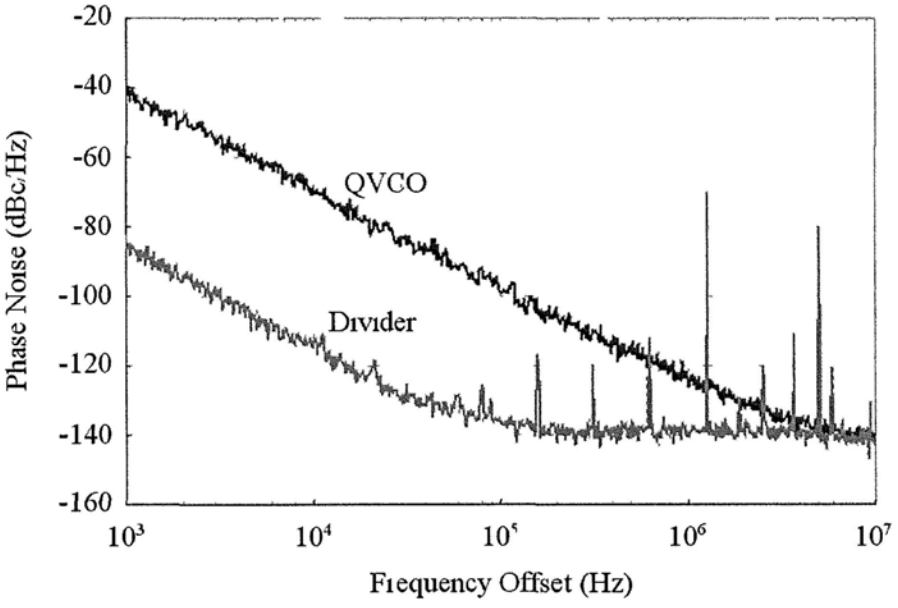


(a)

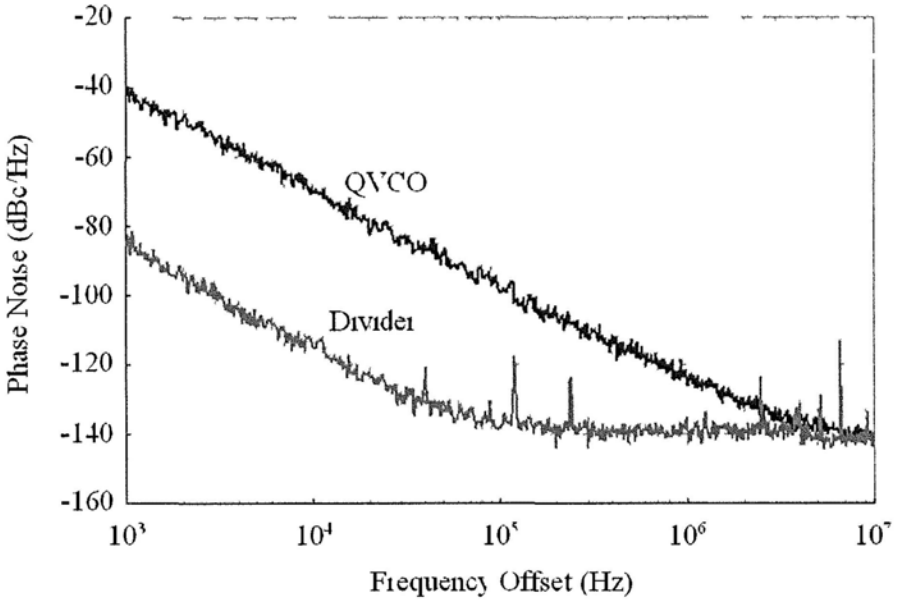


(b)

Figure 6.15 Phase noise performances of the QVCO and the frequency divider with the cross-coupling dual divide-by-4 ILFD for division ratios of (a) 240.5 and (b) 248



(a)



(b)

Figure 6 16 Phase noise performances of the QVCO and the frequency divider with the coherent-coupling dual divide-by-4 ILFD for division ratios of (a) 240 5 and (b) 248

6.5 Proposed Frequency Synthesizer – Design 1

In the first design of the frequency synthesizer, the cross-coupling dual divide-by-4 ILFD is implemented in the programmable fractional frequency divider. The spurious tone performance and phase noise characteristic of the proposed frequency synthesizer were measured through an Agilent E4440A PSA spectrum analyzer. To measure the settling time, the QVCO control voltage was monitored through an Agilent DSO8104A Infiniium oscilloscope. Moreover, the phase accuracy of the proposed frequency synthesizer quadrature outputs was verified by using the conventional image band rejection technique [111]. The up-converted output spectrum was then captured through an Agilent E4470B ESA spectrum analyzer.

6.5.1 Spurious Tone Performance

Figure 6.17 depicts the proposed frequency synthesizer output spectrum. The functionality of sub-integer division is illustrated. With the reference clock frequency of 10 MHz and divider division ratio of 241.5, the proposed frequency synthesizer generates a main frequency tone at 2.415 GHz. The reference spur at 10 MHz frequency offset from the carrier is -64.37 dBc, which is the worst case for all channels, as shown in Figure 6.18. Spurious tones at ±5 MHz frequency offset from the carrier are also observed and are better than -73 dBc. This is due to the spurious tones at the frequency divider output. Reduction of the PLL loop bandwidth and improvement in the phase matching between

the dual divide-by-4 ILFD outputs in the frequency divider help to suppress those spurious tones.

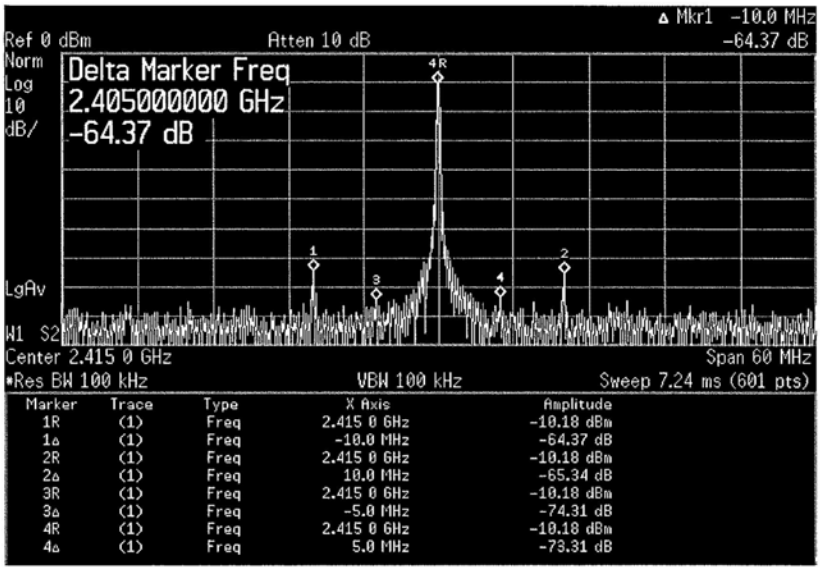


Figure 6.17 Measured output spectrum of the proposed frequency synthesizer – design 1

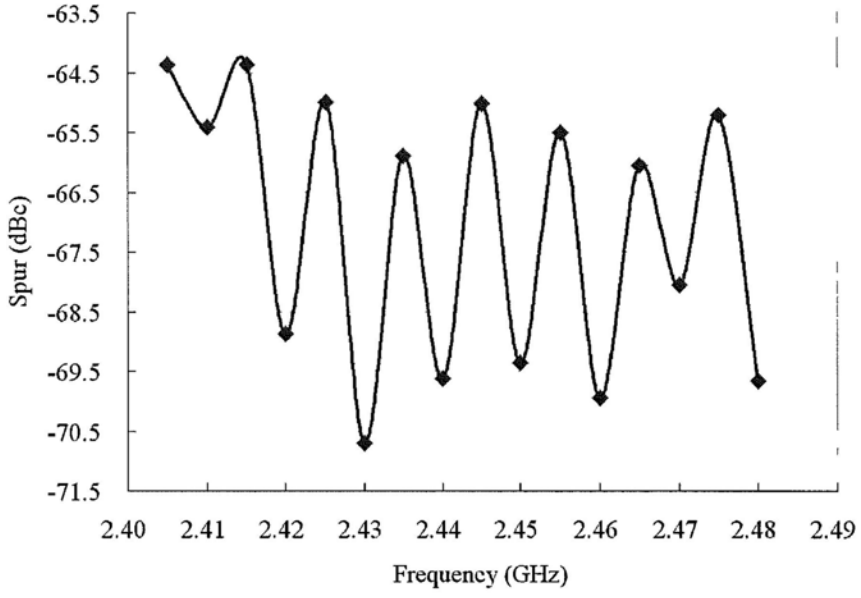


Figure 6.18 Measured reference spur performance of the proposed frequency synthesizer – design 1

6.5.2 Phase Noise

The worst case phase noise performance of the proposed frequency synthesizer is presented in Figure 6.19. At 1 MHz frequency offset, the measured phase noise is -115.18 dBc/Hz, which matches with the analytical value[1]. Its variation is less than 4 dB for all channels, as shown in Figure 6.20. The in-band phase noise is around -70 dBc/Hz. At above 10 MHz frequency offset, the phase noise spectrum is limited to the noise floor of around -144 dBc/Hz.

6.5.3 Settling Time

The settling behaviors when switching the proposed frequency synthesizer between the first (2.405 GHz) and last channel (2.48 GHz) are displayed in Figure. 6.21. The proposed frequency synthesizer needs 16.55 μs to settle when migrating from the first to last channel. In contrast, the settling time in reverse order is 29.27 μs. The asymmetric behavior is due to the nonlinearity of the VCO gain. In both cases, the QVCO control voltage settles to the final state fast with slight damping, which reflects good stability characteristic of the PLL loop dynamics.

[1] Although the measured QVCO phase noise has 5 dB improvement, it will only decrease the overall PLL phase noise by around 1.5 dB in the analytical modeling. In this case, the loop filter noise contribution, mainly due to the opamp noise, becomes dominant. As such, in order to suppress its noise contribution, the transconductance of the differential pair in the opamp should be increased with the tradeoff of higher power consumption.

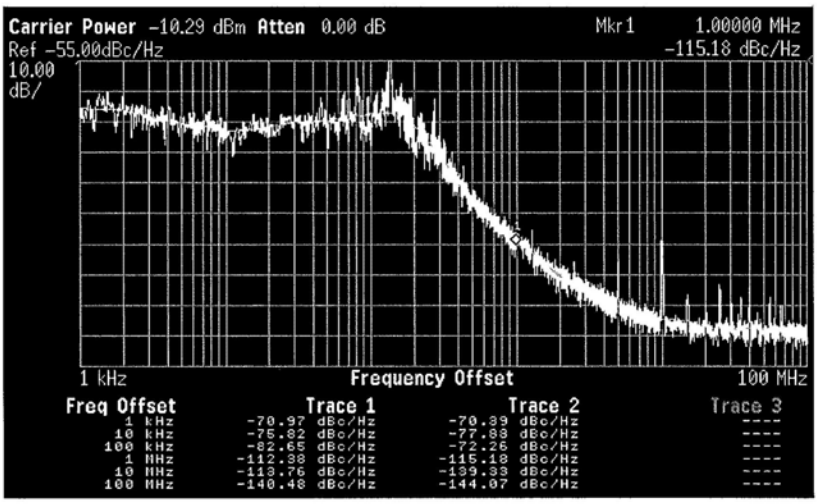


Figure 6.19 Phase noise measurement of the proposed frequency synthesizer – design 1

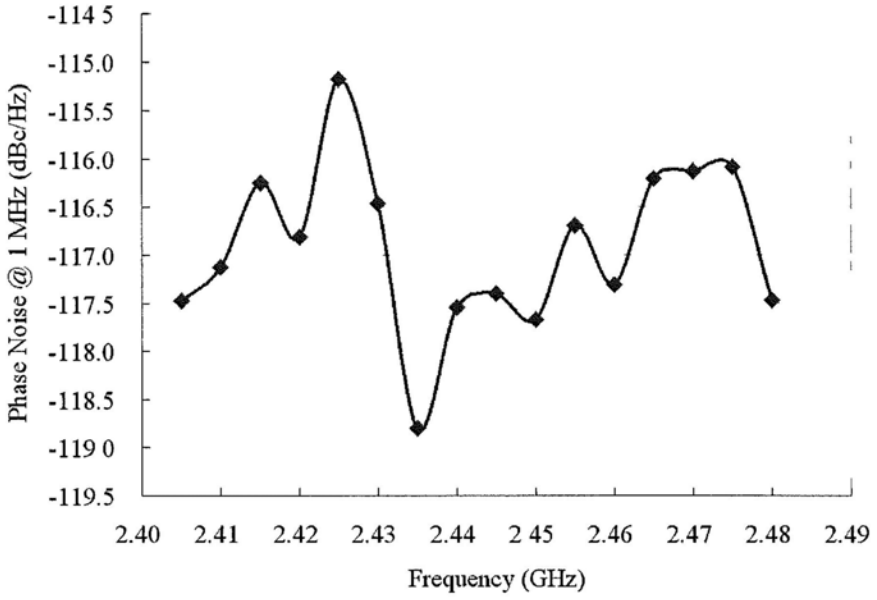
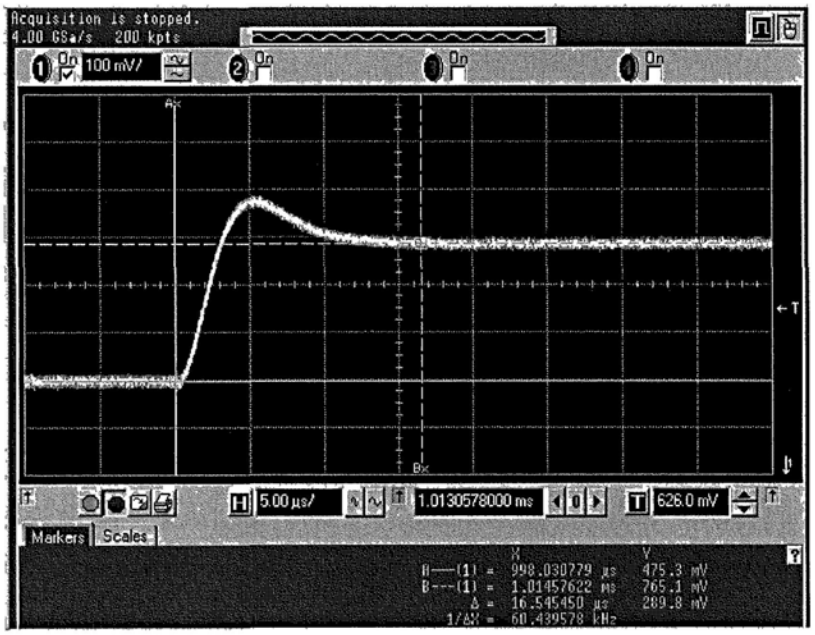
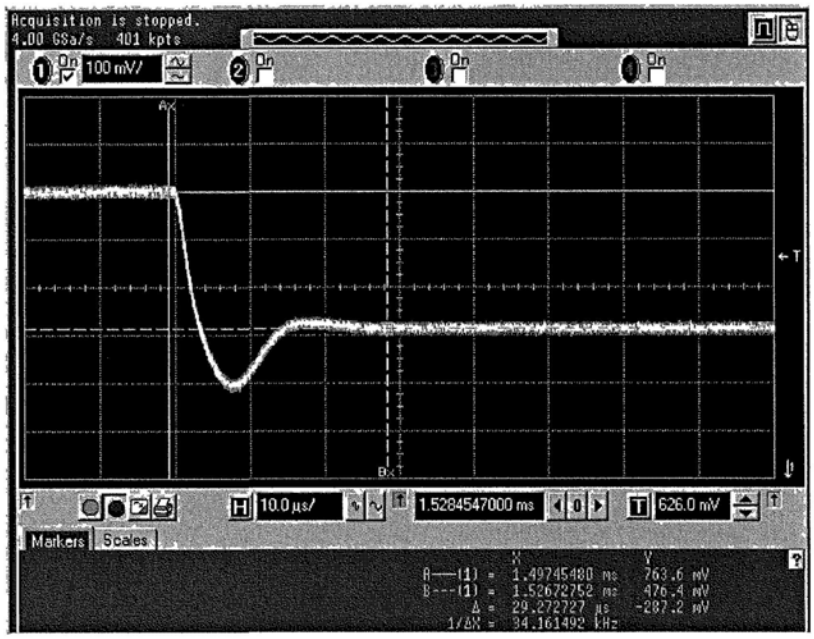


Figure 6.20 Measured phase noise at 1 MHz frequency offset of the proposed frequency synthesizer – design 1



(a)



(b)

Figure 6 21 Settling time measurement of the proposed frequency synthesizer – design 1
(a) from 2 405 GHz to 2 48 GHz and (b) from 2 48 GHz to 2 405 GHz

6.5.4 Quadrature Accuracy

The measured up-converted output spectrum of the passive SSB mixer is depicted in Figure 6.22. Due to the device mismatches of the circuit components (not only from the QVCO, but also from the passive SSB mixer and polyphase filter as well), a spurious tone at lower sideband is generated. At a LO frequency of 2.425 GHz, the measured image rejection ratio (IRR) is -40.71 dB, which is the worst case for all channels, as shown in Figure. 6.23.

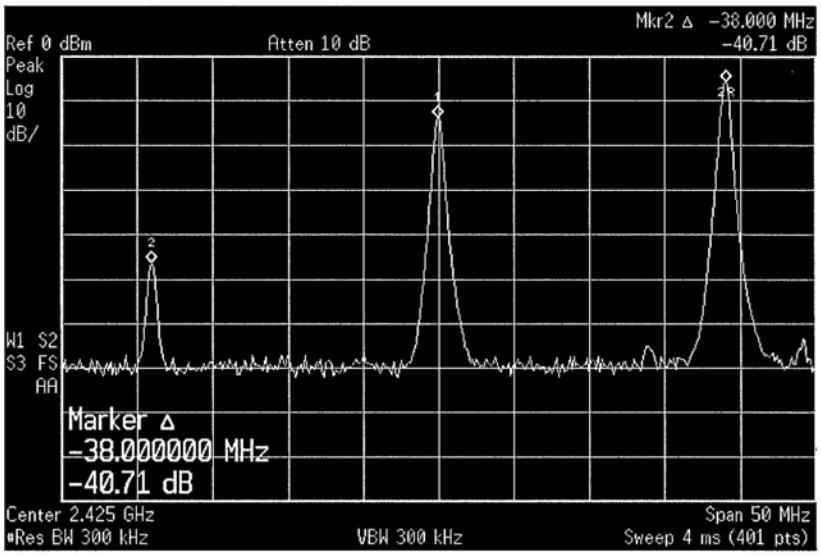


Figure 6.22 Measured sideband rejection of the proposed frequency synthesizer – design 1

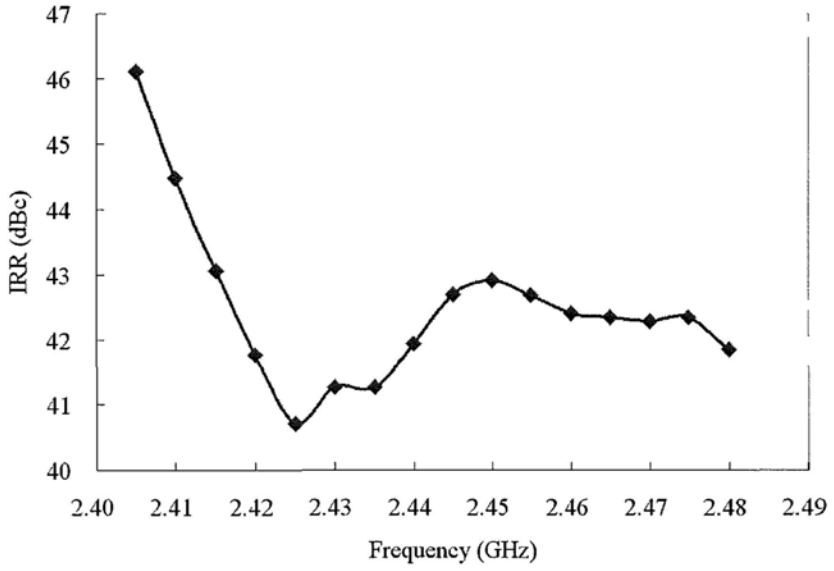


Figure 6.23 Image rejection measurement of the proposed frequency synthesizer – design 1

6.6 Proposed Frequency Synthesizer – Design 2

The measurement procedures for characterizing the first design of the proposed frequency synthesizer in the previous section are completely adopted in measuring the second design performances. In this design, the first stage of the programmable fractional frequency divider is replaced by the coherent-coupling dual divide-by-4 ILFD. Other circuit components are identical in both designs.

6.6.1 Spurious Tone Performance

The output spectrum of the proposed frequency synthesizer at 2.435 GHz is shown in Figure 6.24. Fractional division ratio of 243.5 is selected and a main frequency tone at 2.435 GHz is then generated with the reference clock frequency of 10 MHz. The reference spur at 10 MHz frequency offset from the carrier is measured as -65.86 dBc. Additionally, due to the spurious tones induced at the frequency divider output, spurs at ±5 MHz frequency offset from the carrier are observed and are less than -71 dBc. Figure 6.25 presents the measured reference spur performance for all channels. It can be seen that the reference spur is suppressed better when there is no fractional division occurred.

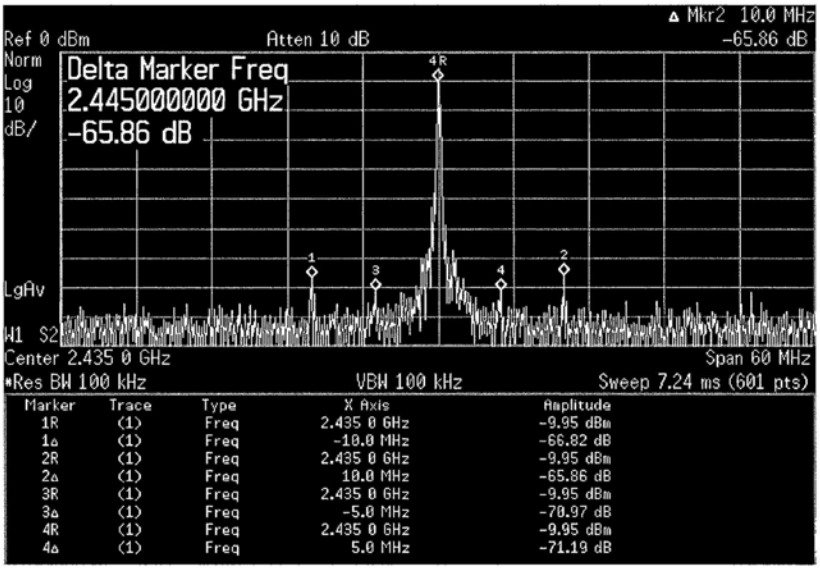


Figure 6.24 Measured output spectrum of the proposed frequency synthesizer – design 2

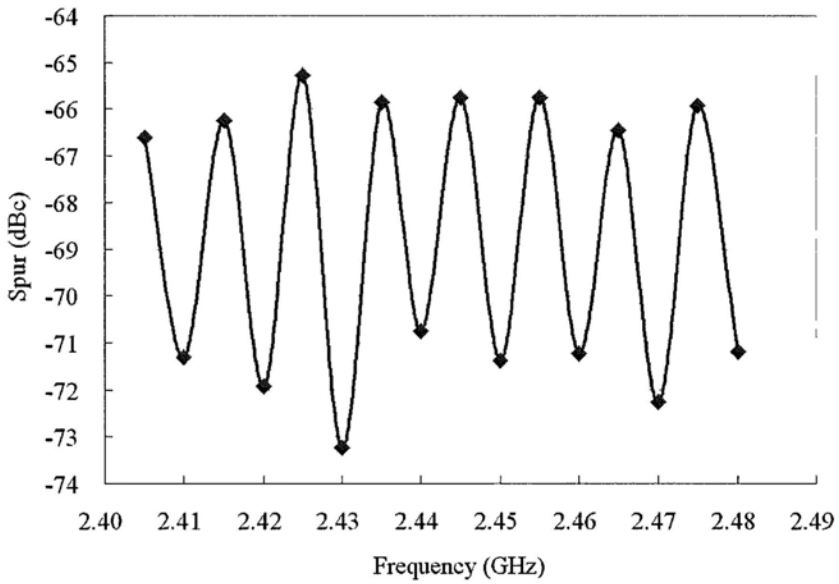


Figure 6.25 Measured reference spur performance of the proposed frequency synthesizer – design 2

6.6.2 Phase Noise

Figure 6.26 presents the phase noise characteristic of the proposed frequency synthesizer at the center frequency of 2.44 GHz. The measured phase noise at 1 MHz frequency offset and the in-band phase noise are -115.44 dBc/Hz[2] and -68.06 dBc/Hz respectively. It is the worst case for all channels, as depicted in Figure 6.27. The best case occurs at the center frequency of 2.41 GHz, with the phase noise of -118.88 dBc/Hz at 1 MHz frequency offset. Besides, it is observed that the noise floor is approximately -145 dBc/Hz at 100 MHz frequency offset.

[2] In the measurement, the QVCO phase noise has 5 dB improvement, which will only decrease the overall PLL phase noise by around 1.5 dB in the analytical modeling. In this case, the loop filter noise contribution, mainly due to the opamp noise, becomes dominant. As such, in order to suppress its noise contribution, the transconductance of the differential pair in the opamp should be increased with the tradeoff of higher power consumption.

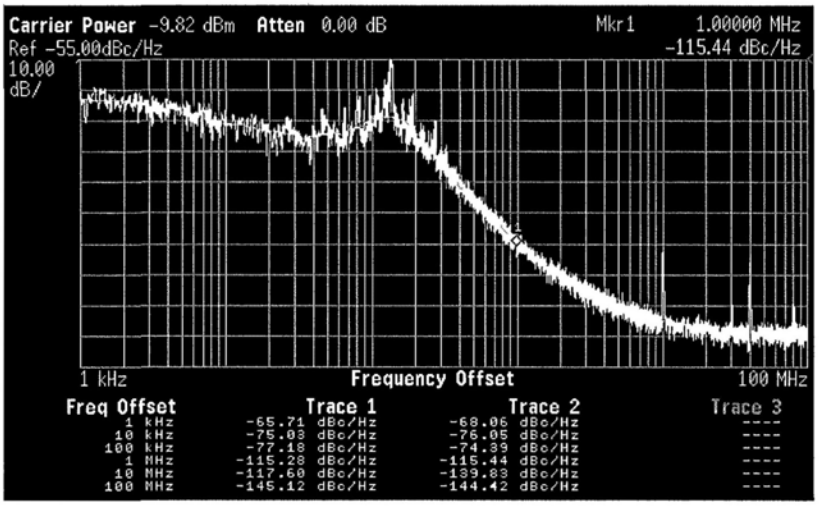


Figure 6.26 Phase noise measurement of the proposed frequency synthesizer – design 2

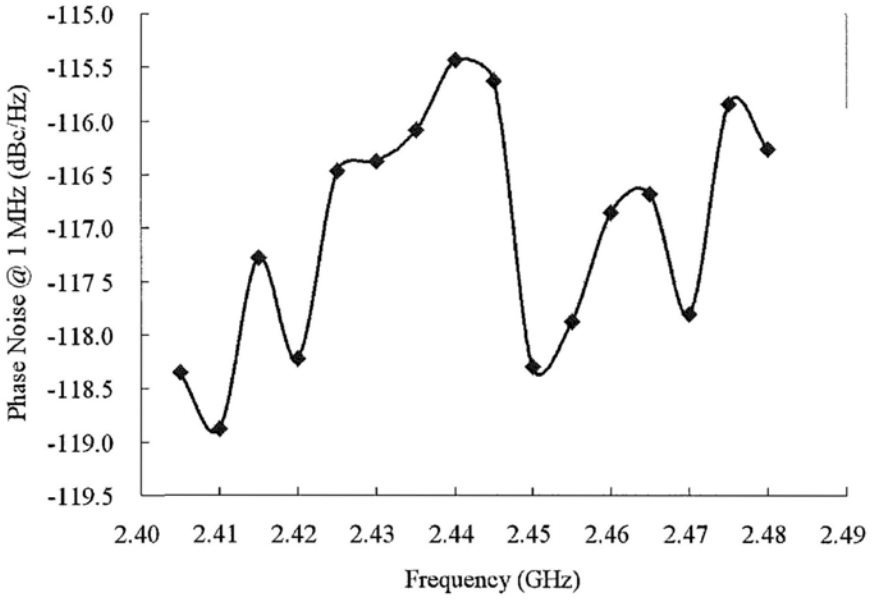


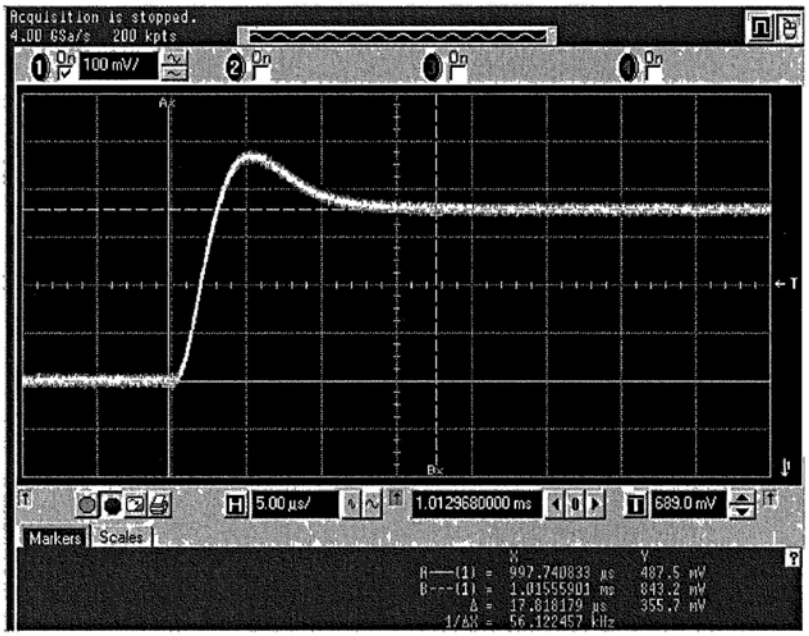
Figure 6.27 Measured phase noise at 1 MHz frequency offset of the proposed frequency synthesizer – design 2

6.6.3 Settling Time

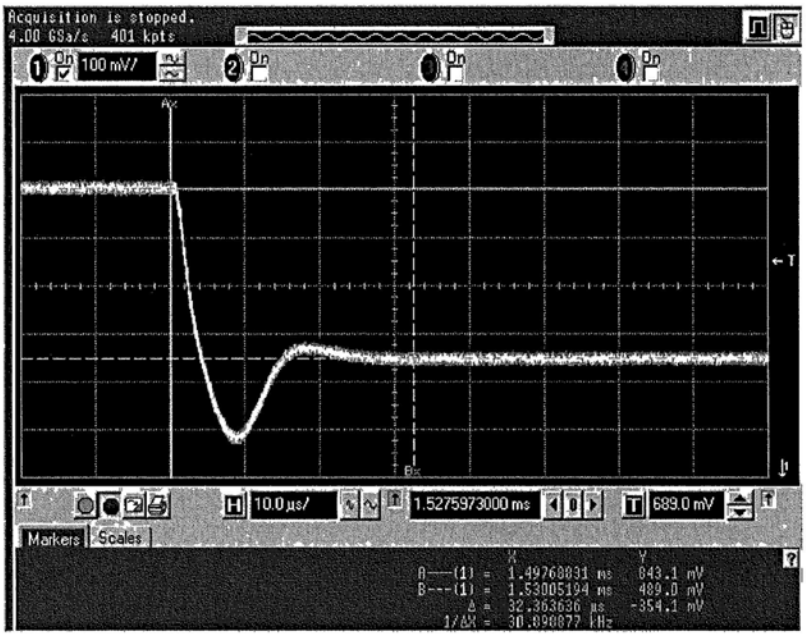
The settling time measurement results are shown in Figure 6.28. When toggling between the first and last channel, the proposed frequency synthesizer takes 17.82 μs (from 2.405 GHz to 2.48 GHz) and 32.36 μs (from 2.48 GHz to 2.405 GHz) respectively to settle. The VCO gain nonlinearity of the QVCO causes this asymmetric behavior. Good stability performance of the PLL loop dynamics is demonstrated as the QVCO control voltage changes to its final state fast with little damping in both cases.

6.6.4 Quadrature Accuracy

Figure 6.29 depicts the measured up-converted output spectrum of the passive SSB mixer at a LO frequency of 2.43 GHz. The measure image rejection ratio is -38.13 dB, which is the worst case for all channels. As presented in Figure 6.30, the measured image rejection ratio for all channels has an average of around 40.5 dB with a deviation of ±2.5 dB.



(a)



(b)

Figure 6 28 Settling time measurement of the proposed frequency synthesizer – design 2
(a) from 2 405 GHz to 2 48 GHz and (b) from 2 48 GHz to 2 405 GHz

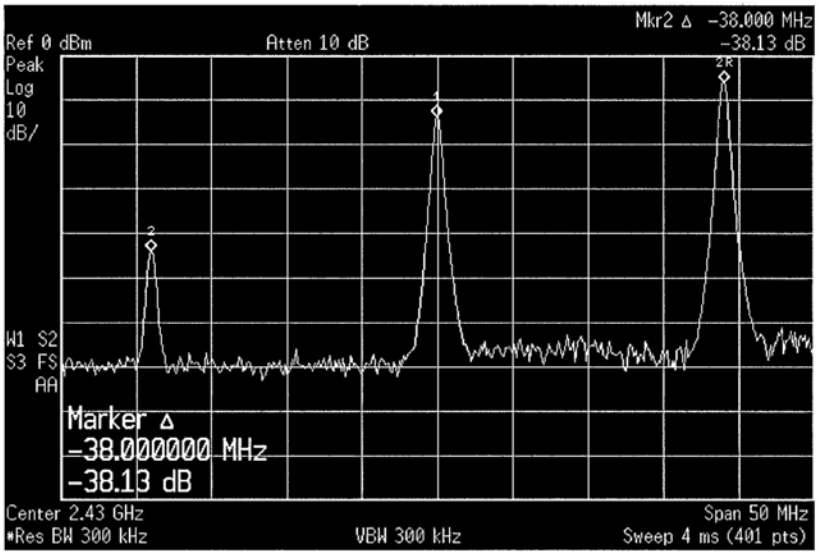


Figure 6.29 Measured sideband rejection of the proposed frequency synthesizer – design 2

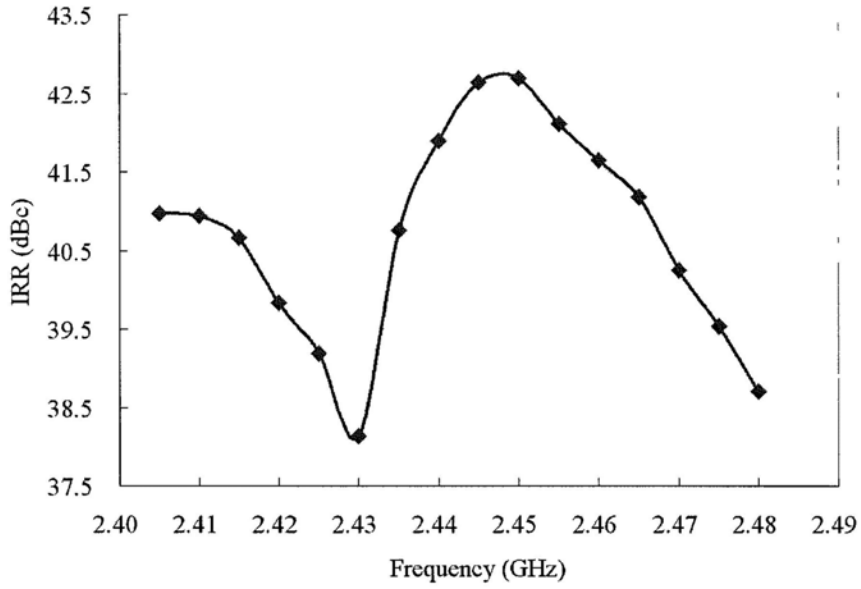


Figure 6.30 Image rejection measurement of the proposed frequency synthesizer – design 2

6.7 Measurement Result Summary and Performance Comparison

A comparison between the proposed fractional frequency dividers and other published works is shown in Table 6 1 Design A is the fractional frequency divider with the cross-coupling dual divide-by-4 ILFD while the coherent-coupling dual divide-by-4 ILFD is represented as Design B

Design	[51]	[55]	[73]	Design A	Design B
CMOS Process	0 13 μm	0 18 μm	0 25 μm	0 35 μm	0 35 μm
Frequency (GHz)	5 15625	2 5 – 3 2	1 2	2 24 – 2 70	2 26 – 2 67
Division Ratio	16/16 5	32 – 511 5	6 25 – 9 75	240 5 – 248	240 5 – 248
Step Size	0 5	0 5	0 25	0 5	0 5
Area (mm^2)	0 0075	0 15[+]	0 29[+]	0 0276	0 0276
Supply Voltage (V)	1 2	2	2	1 5	1 5
Power (mW)	18	22	3	5 13	3 63
FOM[*] (GHz/mW)	0 29	0 13	0 4	0 48	0 68

Table 6 1 Performance comparison of the fractional frequency dividers

[+] Divider area is estimated from the overall frequency synthesizer area
[*] FOM is defined as the ratio of center operation frequency to power consumption

Table 6 2 depicts the summary of the proposed frequency synthesizers' measured performances and a comparison with other published works

Design	[114]	[115]	[116]	[117]	[118]	Design 1	Design 2
Architecture	Integer-N	Dual PLL	Fractional-N	Fractional-N	Integer-N	Sub-Integer-N	Sub-Integer-N
CMOS Process	0 18 μm	0 35 μm	0 18 μm	0 18 μm	0 18 μm	0 35 μm	0 35 μm
Chip Area (mm^2)	1 10	3 70	4 84 [#1]	4 84 [#1]	1 68 [#2]	0 70	0 70
Quadrature Output	Yes	No	No	No	Yes	Yes	Yes
Phase Noise (dBc/Hz)	-125 @3 MHz	-97 @1 MHz	-124 @3 MHz	-121 @3 MHz	-104 2 @1 MHz	-115 18 @1 MHz [#3]	-115 44 @1 MHz [#3]
Spurious Level (dBc)	-30	-55	-47	-64	-36 5	-64 37	-65 86
IRR (dB)	30	N A	N A	N A	32 75 [#4]	40 71	38 13
Switching Time (μs)	120	N A	35	N A	N A	29 27	32 36
Supply Voltage (V)	1 8	3 3	1 8	1 8	0 6	1 5	1 5
Power (mW)	15	49 5	37 6	48 8	14 4	24 03	22 53

Table 6 2 Measurement result summary of the proposed frequency synthesizers and comparison with other published works

[#1] Area includes ESD devices and pads
[#2] Area includes pads, but loop filter is off-chip
[#3] Phase noise at 3 MHz frequency offset is about -130 dBc/Hz
[#4] Measured phase error is 2 64° Assuming IRR is entirely caused by phase deviation [111], it is equivalent to an IRR of 32 75 dB

CHAPTER 7

CONCLUSION

7.1 Concluding Remark

In this thesis, the implementation of a 2.4 GHz sub-integer-N phase-locked loop (PLL) has been demonstrated and fabricated in a standard 0.35 μm CMOS process. The proposed sub-integer-N PLL architecture offers a simple structure and good spurious performance as in the integer-N PLL design. With fractional division ratio, the reference clock frequency and loop bandwidth can be increased, which leads to agile switching time. Furthermore, the phase noise performance is improved. No unexpected fractional spurs are created as in the fractional-N PLL design.

Design considerations and techniques are discussed to obtain small chip area and robust performance under low supply voltage. For instance, by using the dual-path loop filter topology, the total loop filter capacitance diminishes to less than 60 pF in the proposed design, ensuring on-chip implementation feasibility. The current steering technique and bias regulation by an error amplifier employed in the charge pump design improve the charge pump current matching and switching time, reducing noise contribution and spurious tone generation. Moreover, the parallel-coupled *LC* quadrature voltage-

controlled oscillator (QVCO) is designed with wide tuning range, low VCO gain and good phase noise performance.

A novel quadrature-input programmable fractional frequency divider is proposed. Since the quadrature-input scheme provides equal loading to the QVCO outputs, good phase quadrature accuracy is maintained without dummy divider as in conventional designs. The phase-switching frequency divider architecture is chosen due to low power dissipation and high operation speed when compared with the static frequency divider counterparts. The structure of the phase-switching circuitry is also considered to minimize logic propagation delay, reduce output glitches and achieve low power consumption.

The generation of equally-spaced signals for phase switching is realized by cross-coupling two divide-by-4 injection-locked frequency dividers (ILFDs) in the fractional frequency divider. Two different coupling schemes for the dual divide-by-4 ILFD are introduced, namely the cross-coupling and coherent-coupling types. In both schemes, a symmetric architecture is preserved to balance the QVCO output loading. The unique phase switching sequence also simplifies the phase-switching circuitry and suppresses the possibility of incorrect frequency division due to glitches.

Two sub-integer-N PLLs with different fractional frequency dividers are experimentally verified. The measured phase noise is approximately -115 dBc/Hz at 1 MHz frequency offset and the spurious tones are below -64 dBc. The measured switching time is around 32 μs and the mismatches between the quadrature outputs are better than 38 dB

(characterized by image rejection ratio). Additionally, each proposed design occupies a chip area of 0.70 mm^2 and consumes less than 24.1 mW from a single supply of 1.5 V.

7.2 Recommendation for Future Work

The extension of the present work may be continued in two directions:

- Elimination of the spurious tones induced by the phase mismatch in the phase-switching frequency divider. Suppression of those spurious tones can be achieved in two possible ways. A direct solution is minimization of the phase imbalance of the multi-phase signals in the phase-switching frequency divider by introduction of a self-calibration circuit to adjust the mismatches autonomously [74]. Another approach is attenuation of spurious components in the VCO control signal by charge averaging [119] or charge redistribution [120], [121]. As a tradeoff, PLL loop stability is concerned for the suggested methodologies. Since the self-calibration circuit operates when the PLL is locked, the locking behavior of the main loop may be disturbed and even becomes unstable. Besides, the charge averaging and charge redistribution techniques induce additional time delay in the loop characteristic, degrading the loop stability.

- Generalization of the coupling scheme in dual frequency divider structure. The proposed coupling scheme is not limited to its implementation on the divide-by-4 ILFD as presented in this work. It is also feasible to apply on frequency dividers of

non-injection-locked type, for example, divide-by-2 static frequency dividers. In this case, the division ratio resolution decreases to 0.25. Further investigation can be performed on different frequency divider structures to illustrate the impact of different coupling schemes on locking range and operation frequency, in order to obtain an optimal solution for individual structure.

APPENDIX A

PROCESS PARAMETERS OF THE CHOSEN 0.35 μM CMOS PROCESS

A.1 Key Features

- 0.35-micron double poly, quadruple metal N-well CMOS process
- Double poly capacitor module with high capacity per area
- High-resistive poly resistor module
- Thin metal 4 module
- Minimum feature size: 0.35 um gates
- Supply voltage: CMOS 3.3V; periphery up to 5.5V
- High density CMOS standard cell library available
- Gate delay: 0.10ns (NAND2 typical)
- Applications: mixed signal analog designs, large digital designs and system on chip

A.2 Wafer Cross-Section

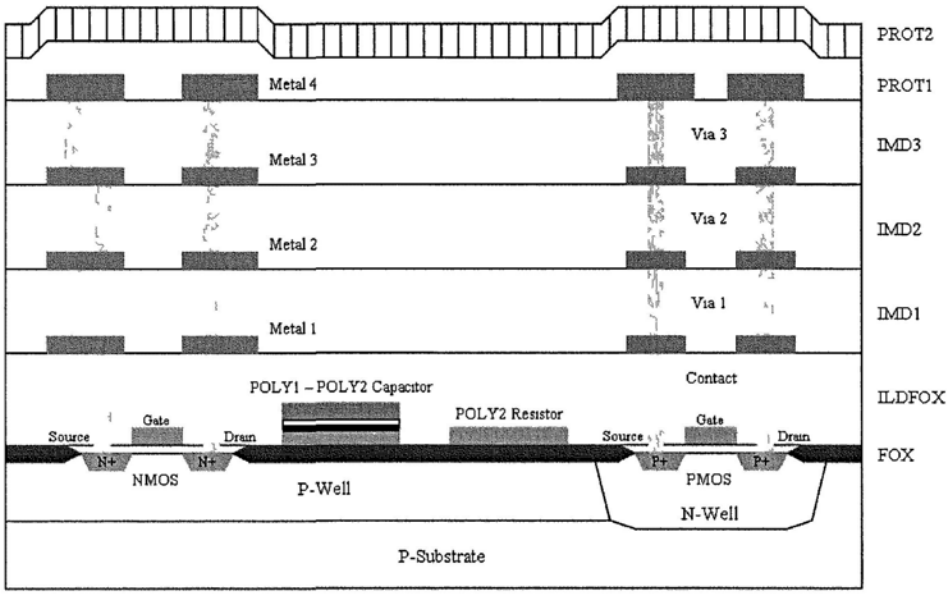


Figure A.1 Wafer cross-section of the chosen 0.35 µm CMOS process [122]

A.3 Basic Design Rules

Mask	Width (µm)	Spacing (µm)
N-well	1 7	1 0
Active Areas	0 3	0 6
Poly-Silicon Gate	0 35	0 45
Poly-Silicon Resistor	0 65	0 5
Contact	0 4	0 4
Metal 1	0 5	0 45
Via 1	0 5	0 45
Metal 2	0 6	0 5
Via 2	0 5	0 45
Metal 3	0 6	0 5
Via 3	0 5	0 45
Metal 4	0 6	0 6

Table A 1 Basic design rules of the chosen 0 35 µm CMOS process [123]

A.4 Device Parameters

A.4.1 Active Devices

MOS Transistors						
Device	Device name	VT (V)	IDS (µA/µm)	BVDS (V)	max. VDS (V)	max. VGB (V)
3.3 V NMOS	NMOS	0.50	540	> 8	3.6	3.6
3.3 V PMOS	PMOS	-0.65	-240	< -8	3.6	3.6
5 V NMOS	NMOSM	0.70	470	> 9	5.5	5.5
5 V PMOS	PMOSM	-0.97	-200	< -8	5.5	5.5
HV NMOS (gate oxide)	NMOSH	0.44	200	19	15	3.6
HV NMOS (mid-oxide)	NMOSMH	0.67	220	22	15	5.5

Table A.2 Device parameters of MOS transistors [122]

Bipolar Transistors					
Device	Device name	BETA	VA (V)	BVCEO (V)	max. VCE (V)
Vertical PNP	VERT10	5.0	> 80	5	3.6
Lateral PNP	LAT2	140	15	5	3.6

Table A.3 Device parameters of bipolar transistors [122]

A.4.2 Passive Devices

Capacitor						
Device	Device name	Area Cap ($fF/\mu m^2$)	Linearity (ppm/V)	Temp. Coeff. ($10^{-3}/K$)	BV (V)	max. VCC (V)
Poly1-Poly2	CPOLY	0.86	85	0.03	30	5.5

Table A.4 Device parameters of poly capacitor [122]

Resistors						
Device		Device name	Sheet resistance ($\Omega/\square$)	Temp. Coeff. ($10^{-3}/K$)	Max. J/W (mA/μm)	max. VTB (V)
Poly Silicon	Poly1	RPOLY1	8	0.9	0.5	20
	Poly2	RPOLY2	50	0.59	0.3	20
	HR Poly2	RPOLYH	1200	-0.75	0.1	20
Diffusion	P+ diffusion	RDIFFP	140	1.5		5.5
	N+ diffusion	RDIFFN	75	1.5		5.5
Well	N-Well	RNWELL	1000	6.2		13
Metal	Metal1	RMET	0.07	3.3	1.0	
	Metal2	RMET2	0.07	3.4	1.0	
	Metal3	RMET3	0.07	3.4	1.0	
	Metal4	RMET4	0.04	3.5	1.6	

Table A.5 Device parameters of resistors [122]

Varactor						
Device	Device name	Capacitance @ +1 V ($fF/\mu m^2$)	Capacitance @ -1 V ($fF/\mu m^2$)	Q factor W/L = 317/0.65, 2.4 GHz	BV (V)	max. VCC (V)
MOS varactor	CVAR	4.88	1.33	43	30	5.5

Table A.6 Device parameters of MOS varactor [122]

Spiral Inductors						
Device name	Outer diameter (μm)	Inductance (nH)		Q factor		f_{RES} (GHz)
		@ 2.4 GHz	@ 5.0 GHz	@ 2.4 GHz	@ 5.0 GHz	
SP014S300D	300	1.34	1.38	6.1	6.2	> 6
SP020S180D	180	1.99	2.04	4.5	5.7	> 6
SP026S200D	200	2.64	2.83	4.7	5.3	> 6
SP037S180D	180	3.87	4.30	3.9	4.9	> 6
SP047S180D	180	5.01	5.81	4.1	4.1	> 6
SP050S155D	155	5.62	6.47	3.4	4.1	> 6
SP090S155D	155	9.98	12.7	3.3	2.5	> 6

Table A.7 Device parameters of spiral inductors [124]

APPENDIX B

GENERALIZED DUAL DIVIDE-BY-4 INJECTION-LOCKED FREQUENCY DIVIDER BEHAVIOR MODEL

Figure B.1 shows the generalized dual divide-by-4 injection-locked frequency divider behavior model. The hold and sensing branches generate i_1 and i_2 respectively and the coupling branch are driven by the output with an arbitrary coupling angle γ ($-180° < \gamma \leq 180°$) to produce i_3.

The fundamental components of i_1, i_2 and i_3 are expressed as:

$$\begin{aligned} i_1 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_1} e^{j\omega t} e^{j\phi} \cdot K_1 e^{j\alpha_1}\right\} \\ i_2 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_2} e^{j\omega t} e^{j\phi} e^{j\pi/2} \cdot K_2 e^{j\alpha_2}\right\} \\ i_3 &= \mathrm{Re}\left\{\frac{4}{\pi} I_{inj_3} e^{j\omega t} e^{j\phi} e^{j\gamma} \cdot K_3 e^{j\alpha_3}\right\} \end{aligned} \tag{B.1}$$

where

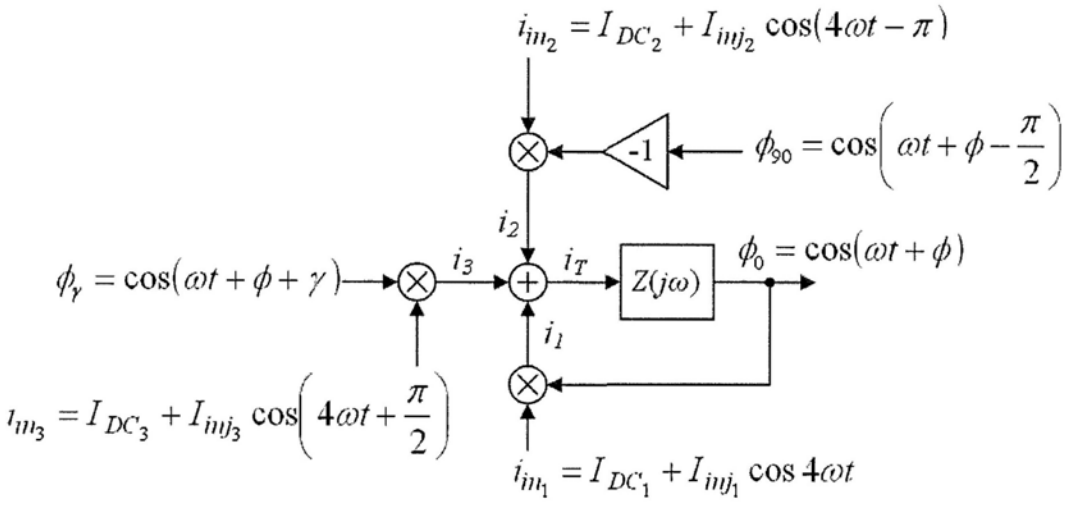


Figure B.1 Generalized dual divide-by-4 injection-locked frequency divider behavior model

$$K_n = \frac{1}{\eta_n}\left|\sec\alpha_n\right| \qquad \text{for } n = 1, 2 \text{ and } 3 \tag{B.2}$$

and

$$\begin{aligned}
\alpha_1 &= \arctan\left[\frac{4}{15}\eta_1\sin(4\phi)\right] \\
\alpha_2 &= -\arctan\left[\frac{4}{15}\eta_2\sin(4\phi)\right] \\
\alpha_3 &= -\arctan\left[\frac{4}{15}\eta_3\cos(4\phi + 4\gamma)\right]
\end{aligned} \tag{B.3}$$

The resultant mixer output current i_T is then manipulated in complex form as:

$$
\begin{aligned}
i_T &= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left[I_{inj_1}K_1e^{j\alpha_1}+I_{inj_2}K_2e^{j\pi/2}e^{j\alpha_2}+I_{inj_3}K_3e^{j\gamma}e^{j\alpha_3}\right]\right\} \\
&= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\left\{\left[I_{DC_1}+\frac{4}{15}I_{DC_2}\eta_2\sin(4\phi)+I_{DC_3}\left(\cos\gamma+\frac{4}{15}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right)\right]\right.\right. \\
&\qquad \left.\left.+j\left[\frac{4}{15}I_{DC_1}\eta_1\sin(4\phi)+I_{DC_2}+I_{DC_3}\left(\sin\gamma-\frac{4}{15}\eta_3\cos\gamma\cos(4\phi+4\gamma)\right)\right]\right\}\right\} \qquad \text{(B.4)} \\
&= \mathrm{Re}\left\{\frac{4}{\pi}e^{j\omega t}e^{j\phi}\cdot K_Te^{j\alpha_T}\right\} \\
&= |i_T|\cos(\omega t+\phi+\alpha_T)
\end{aligned}
$$

where the overall mixer output phase α_T is

$$
\alpha_T = \arctan\left[\frac{I_{DC_2}+I_{DC_3}\sin\gamma+\frac{4}{15}\left[I_{DC_1}\eta_1\sin(4\phi)-I_{DC_3}\eta_3\cos\gamma\cos(4\phi+4\gamma)\right]}{I_{DC_1}+I_{DC_3}\cos\gamma+\frac{4}{15}\left[I_{DC_2}\eta_2\sin(4\phi)+I_{DC_3}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right]}\right] \qquad \text{(B.5)}
$$

To satisfy the phase condition $\varphi(\omega)+\alpha_T=0$ (where $\varphi(\omega)=-\arctan\left(\frac{\omega}{\omega_0}\right)$) at the operation frequency ω, it leads to

$$
\frac{\omega}{\omega_0} = \frac{I_{DC_2}+I_{DC_3}\sin\gamma+\frac{4}{15}\left[I_{DC_1}\eta_1\sin(4\phi)-I_{DC_3}\eta_3\cos\gamma\cos(4\phi+4\gamma)\right]}{I_{DC_1}+I_{DC_3}\cos\gamma+\frac{4}{15}\left[I_{DC_2}\eta_2\sin(4\phi)+I_{DC_3}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right]} \qquad \text{(B.6)}
$$

with $I_{DC_1}+I_{DC_3}\cos\gamma+\frac{4}{15}\left[I_{DC_2}\eta_2\sin(4\phi)+I_{DC_3}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right]>0$ for $|\alpha_T|<90°$

On the other hand, the output amplitude is derived as:

$$\begin{aligned}|i_T|\cdot|Z(j\omega)| &= \frac{4}{\pi}K_T\cdot\frac{R}{\sqrt{1+\left(\omega/\omega_0\right)^2}} \\ &= \frac{4}{\pi}I_{DC_1}R\cdot\left|1+\frac{I_{DC_3}}{I_{DC_1}}\cos\gamma+\frac{4}{15}\left[\frac{I_{DC_2}}{I_{DC_1}}\eta_2\sin(4\phi)+\frac{I_{DC_3}}{I_{DC_1}}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right]\right|\end{aligned} \tag{B.7}$$

To fulfill the gain condition of loop gain greater than 1, it should obey:

$$\left|1+\frac{I_{DC_3}}{I_{DC_1}}\cos\gamma+\frac{4}{15}\left[\frac{I_{DC_2}}{I_{DC_1}}\eta_2\sin(4\phi)+\frac{I_{DC_3}}{I_{DC_1}}\eta_3\sin\gamma\cos(4\phi+4\gamma)\right]\right|\geq 1 \tag{B.8}$$

In actual circuit implementation, the hold and coupling branches share the same bias current and injection source while the sensing branch has its own. Assuming equal partition,

$$\begin{aligned}&I_{DC_1}:I_{DC_2}:I_{DC_3}=I_{inj_1}:I_{inj_2}:I_{inj_3}=1:2:1 \\ &\eta_1=\eta_2=\eta_3=\eta\end{aligned} \tag{B.9}$$

From Equation B.6, B.8 and B.9, the necessary conditions to satisfy the Barkhausen gain and phase conditions at the operation frequency ω are:

$$\begin{cases}1+\cos\gamma+\dfrac{4}{15}\eta[2\sin(4\phi)+\sin\gamma\cos(4\phi+4\gamma)]\geq 1 \\ \dfrac{\omega}{\omega_0}=\dfrac{2+\sin\gamma+\dfrac{4}{15}\eta[\sin(4\phi)-\cos\gamma\cos(4\phi+4\gamma)]}{1+\cos\gamma+\dfrac{4}{15}\eta[2\sin(4\phi)+\sin\gamma\cos(4\phi+4\gamma)]}\end{cases} \tag{B.10}$$

Figure B.2 and B.3 depicts the normalized center frequency and locking range of the proposed model with various injection ratios η and coupling angles γ. The proposed model obtains stable oscillation for $|\gamma| < 135°$. The operation frequency range extends outward with increasing η because larger output amplitude is obtained. Refer to the gain condition in Equation B.10, since $\cos\gamma < 1$ for $90° < |\gamma| < 180°$, greater contribution for the last term with dependence on η should be involved in order to compensate the gain reduction by $\cos\gamma$.

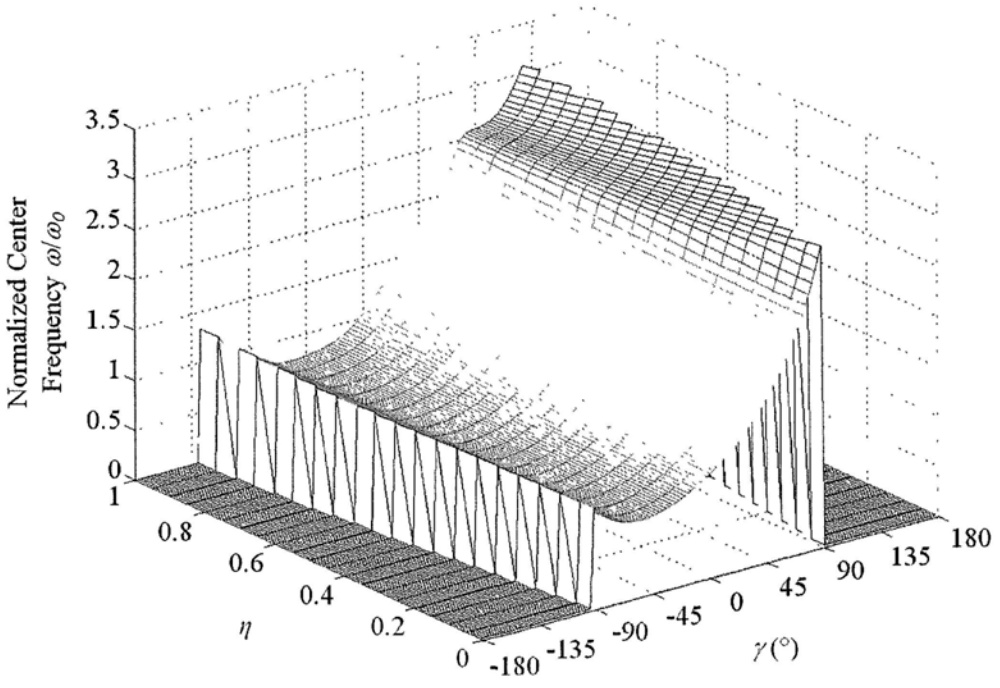


Figure B.2 Normalized center frequency with respect to η and γ

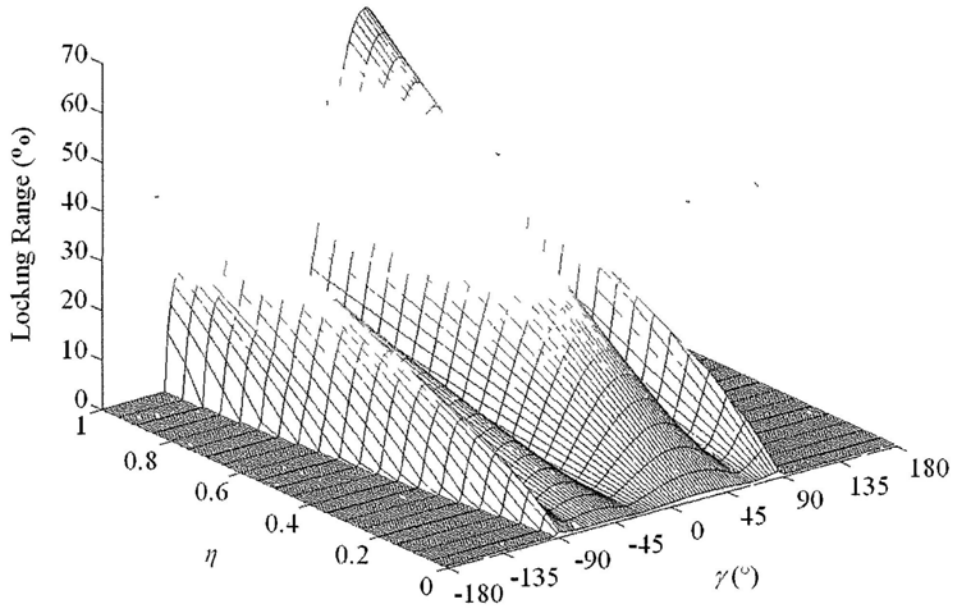


Figure B.3 Locking range with respect to η and γ

Higher center frequency occurs at around $\gamma = 90°$. In this case, the coupling branch current component is almost in phase with that of the sensing branch. These two components add up and increase the transconductance for sensing operation. Faster switching occurs due to stronger sensing strength. This explains the operation frequency enhancement in the coherent-coupling design[1], which has the coupling angle $\gamma$of 90°.

The asymmetry of the operation frequency between the positive and negative values of γ is illustrated by the phasor diagram in Figure B.4. Since larger phase shift of α_T is acquired with positive values of γ, higher operation frequency results.

As presented in Figure B.3, the locking range of the proposed model varies with different values of γ. It expands with stronger injection and has the maximum located close to $\gamma = 45°$, which corresponds to the cross-coupling design. By viewing Figure B.3 in parallel with the axis for η as in Figure B.5, the maxima and minima can be clearly

[1] Current distribution in the coherent-coupling design does not follow Equation B.9, but similar conclusion can be drawn if actual one is used. It operation frequency, shown in Figure 4.18, is even higher.

identified. It can be seen that not only higher operation frequency can be selected with positive γ, but also larger locking range can be obtained.

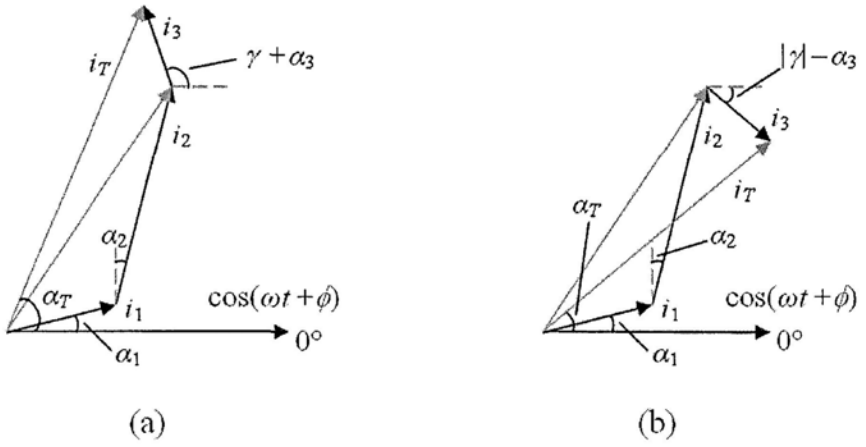


Figure B.4 Phasor diagram of the resultant mixer output current and output voltage for (a) positive $\gamma$and (b) negative γ

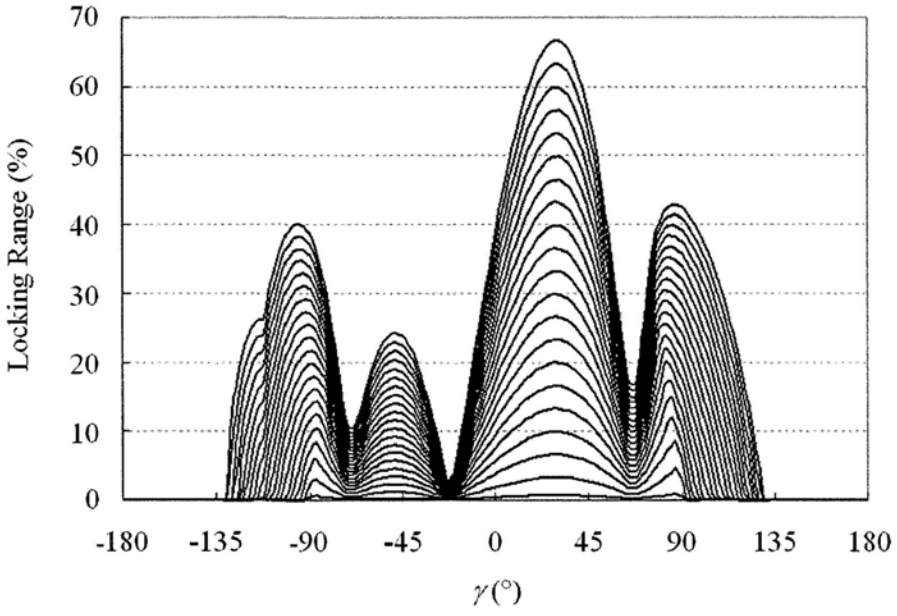


Figure B.5 Locking range versus γunder the influence of η

The proposed model has the narrowest locking range at γ = -22.5°. As illustrated in Figure B.6, the phase shifts of i_1 and i_3 are equal, but they rotate in opposite direction. The resultant component of i_1 and i_3 has a fixed phase offset and its amplitude change is minor (< 9%) because α varies less than 15° even for η = 1. As a result, mainly the phase shift of i_2 contributes to the overall phase shift α_T. This limits the possible range of α_T and so as the locking range.

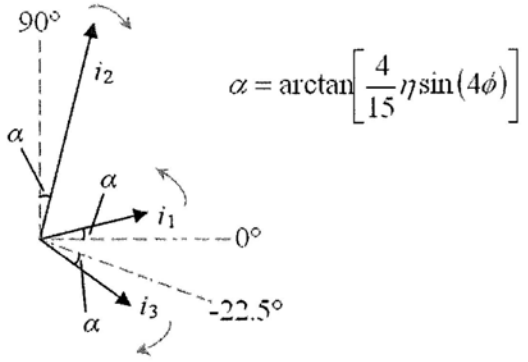


Figure B.6 Phasor diagram of the current components for γ= -22.5°

Comparison between cross-coupling (γ= 45°) and coherent-coupling (γ= 90°) designs reveals that the first approach is advantageous of wide locking range while the second one results in faster operation speed. For the phase noise performance, the coherent-coupling design has better measurement result (Fig. 6.11 and Fig. 6.12). This may be explained by the phasor relationship between the sensing and coupling current components. As in [125], [126], the phasors of different current components should be aligned in same direction so as to improve the phase noise performance. Although more circuitries (corresponding to more noise sources) are needed to implement the required phase shift, the overall phase noise performance does not degrade, but improves. Resemble to the above case, in the coherent-coupling design, the sensing and coupling current components are almost in phase. Phase noise improvement is therefore expected.

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