Design of On-Chip Low-Dropout Regulators for Energy-Aware Wireless SoC in Nano-Scale CMOS Technologies

GUO, Jianping

A Thesis Submitted in Partial Fulfillment of the Requirements for the

Degree of Doctor of Philosophy

in

Electronic Engineering

The Chinese University of Hong Kong

June 2011

Abstracts of thesis entitled:

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for the degree of **Doctor of Philosophy**

in **Electronic Engineering**

at **The Chinese University of Hong Kong**

in **April 2011**

Remotely- or battery-powered wireless system-on-a-chip (SoC) needs energy-efficient and high-integration power-management solutions due to their energy-aware characteristics. Low-dropout regulator (LDO) is a good solution because of its excellent performances such as low power consumption, fast load-transient response and high power-supply ripple rejection (PSRR). Moreover, it is easy to be fully integrated since no inductor is needed to be the energy-storage element. Recent development of output-capacitorless LDO (OCL-LDO) realizes on-chip, local voltage regulation to enable more effective integrated power management for SoC. In this thesis, OCL-LDOs with low power consumption and fast load-transient response are investigated and presented in this thesis. LDO with output capacitor for high-PSRR operation to provide clean power supply to RF circuits is also reported. Three LDOs are developed and fabricated to verify the proposed ideas.

The first design is an ultra low-power voltage regulator for remotely powered energy-autonomous devices. It has been fabricated in a commercial 0.18-μm CMOS technology and applied to a passive UHF RFID tag IC. With the low-power voltage reference circuit and sub-threshold operations, the total quiescent current is 700 nA under a 1.8-V power supply. The output voltage of the regulator is 1.45 V with load capability of 50 μA. The temperature coefficients of the voltage reference and the

output voltage are only 9 and 43 ppm/°C, respectively. A POR signal with 150-ns-width pulse is also generated to reset the digital processing part in the tag IC.

The second design is a fast-transient OCL-LDO, which has been implemented in a commercial 90-nm CMOS technology. Experimental result verifies that it is stable for a capacitive load from 0 to 50 pF and with load capability of 100 mA. Moreover, the gain-enhanced structure provides sufficient loop gain to improve line regulation to 3.78 mV/V and load regulation to 0.1 mV/mA, respectively. The embedded voltage-spike detection circuit enables pseudo Class-AB operation to drive the power transistor promptly. The maximum overshoot and undershoot under a 1.2-V supply are less than 66 mV for full load current changes within 100-ns edge time, and the recovery time is less than 5 μs. While the measured power consumption is only 6 μW under a 0.75-V supply.

Finally, the PSRR performance of LDO is studied. An energy-efficient embedded ripple feed-forward path is proposed to improve the PSRR of LDO. Comparing with some state-of-the-art techniques for PSRR improvement, the proposed LDO features very simple structure thus low-power consumption. A LDO implemented in 0.18-μm CMOS technology with 0.042-mm^2 active area has been designed to verify the idea. With an external 4.7-μF output capacitor, in the maximum load condition (i.e. at 25 mA), the PSRR is -77 dB at 1 MHz, -85 dB at 2.5 MHz and -55 dB at 5 MHz, respectively. The quiescent current is 15 μA only, while the transient voltage overshoot or undershoot is less than 40 mV when load current changes between 1 mA and 25 mA with 40-ns step time. The LDO achieves good line and load regulations of 3 mV/V and 50 μV/mA, respectively.

摘 要

遠程或電池供電的無線系統級芯片（SoC）需要極低功耗和高集成度的電源管理解決方案。低壓差線性穩壓器（LDO）因具備低功耗、快速負載瞬態響應和高電源紋波抑制比（PSRR）等出色之性能，實為上佳之選。此外，由於無需電感器作為能量存儲元件，其易于完全集成。無需外部電容的 LDO 可有效減小封裝引線引起的各種寄生效應并節省了 I/O Pad 的數量，減小了芯片面積。因此，本論文對低功耗及具備快速響應能力之 LDO 進行研究。此外，為獲得高 PSRR 性能而向 RF 電路供電，本文對需要外部電容的高 PSRR LDO 也進行探討。為此，我們設計了三個 LDO 芯片用於驗證所提出之設計思路。

第一個 LDO 具備 700-nA 超低靜態電流及低電壓操作之特徵，極適合於無線供電系統。該 LDO 已在某商用 0.18-μm CMOS 工藝下流片驗證，並已完全集成於某無源超高頻射頻識別標籤芯片（UHF RFID tag IC）中，無需任何外圍元件即可為負載電路提供穩定電源、高精度基準電壓及上電復位（POR）信號。

第二個 LDO 基於 90-nm CMOS 工藝，能在 0–50 pF 負載電容下提供 100 mA 帶載能力。增益加強技術使之能夠獲得良好的穩壓性能，線性調整率及負載調整率分別低至 3.78 mV/V 及 0.1 mV/mA。 嵌入式的輸出電壓尖峰檢測電路使該 LDO 在 8 μA 低靜態電流下獲得超快效應能力及極低毛刺電壓。負載電流于 100 ns 內在 3 mA 至 100 mA 間跳變時，該 LDO 能在 5 μs 內完全恢復且輸出電壓毛刺小於 66 mV，較之傳統電路降低 7 倍之多。上述特性表明該 LDO 極適合於向電池供電的 SoC 供電。

第三個 LDO 致力於不通過增加電路功耗而提升其 PSRR 性能並為 RF 負載電路提供低紋波電源電壓。我們提出了一種嵌入式的電源紋波前饋通路用於提高 LDO 之 PSRR 性能。由於其簡單結構及不消耗靜態功耗之優良特性，在 0.18 μm CMOS 工藝下流片實現的該 LDO 僅佔有 0.042 mm^2 芯片面積及消耗 15 μA 靜態電流。在單個 4.7 μF 輸出電容及最大 25 mA 帶載情況下，該 LDO 在 2.5 MHz 處可獲最高達-85 dB 之 PSRR，並且在 5 MHz 處也可達-55 dB。

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1. **J. Guo** and K. N. Leung, "A 6-μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Vol. 45, No. 9, pp. 1896-1905, Sept. 2010.
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Acknowledgement

I wish to express my deepest gratitude to my supervisor, Prof. LEUNG Ka Nang, who provided me with an excellent research environment. I feel greatly honored to have worked under his guidance. I benefited from his extensive knowledge in circuit design, invaluable teaching and research skills, and so many supports in technical and personal matters. I thank him for his kindness and for being a source of inspiration at every level.

I would like to thank Prof. CHOY Chiu Sing, Prof. PUN Kong Pang and Prof. KI Wing-Hung for serving in my graduate committee.

I am also pleased to express my thanks to laboratory technician, Mr. YEUNG Wing Yee, who has helped me a lot for CAD tools and computer software.

I am grateful to all members in the ASIC Lab for discussions and friendship. With them, the life in CUHK becomes enjoyable, easy and interesting.

Thanks my many friends at CUHK and outside. I have had many memorable moments besides my work. Special thanks to LIU Hongqing for more than 10 years' true friendship. I would not be in CUHK without his help.

Finally, and most importantly, I would like to thank my wife XIE Fangying, my father, brother, sisters and every one in my family, for all their endless love and support.

It's Qingming Festival when I wrote this acknowledgement. This thesis is dedicated to my mother XIE Linlin for the love of her lifetime. Each one of my family misses her so much.

CHAPTER 1. Introduction

1.1 Motivation

In the past 50 years, to improve integration density and processing speed, digital integrated circuits were fabricated in more and more advanced technologies following Moore's Law. The minimal channel length of MOS transistors in today's high-speed memory or processors can be down to 28 nm or even 24 nm [1], [2]. Moreover, they integrate some of the biggest and most important components of the system, such as the CPU, GPU, memory controllers, and channel controllers [3], [4], but there are other system components also on the leading edge of monolithic integration.

Analog parts, including power-management units (PMU), are also needed to be integrated with digital circuits in the same chip to minimize external components, and reduce PCB area and cost of electronic device [5]–[12]. Moreover, all parasitic effects such as bond-wire inductance and resistance due to the external connections with passive components existing in the classical monolithic voltage regulators can be eliminated. In addition, the chip area occupied by many I/O pads for connecting with the different chips is no longer required so that the function-to-area ratio of the system-on-a-chip (SoC) with integrated power management can be significantly improved.

In modern wireless SoC, especially remotely- or battery-powered wireless SoC, there are more restrict requirements for PMU. Ultra low-power fully integrated

voltage regulator is preferred in remotely powered energy-autonomous devices such as passive RFID tag. Low-power fast-transient voltage regulator is needed for digital processing and mixed-signal part in battery-powered systems. For noise sensitive RF or analog parts, high power-supply ripple rejection (PSRR) is an additional requirement.

Linear voltage regulator has smaller output ripples or noise, lower quiescent current (I_q) and faster transient response comparing with the switching DC-DC counterparts. Moreover, it is easier to be fully integrated since no inductor is needed to play as energy-storage element. Low-dropout regulator (LDO) is a kind of linear voltage regulators features with low input-output difference and high efficiency. In this case, LDO is a good choice for wireless SoC for its many advantages mentioned above.

A remotely powered wireless cortical implant system through inductive power link is shown in Fig. 1.1 [13]. Since no battery is available to provide the power supply, the voltage regulator should feature with the low-power and high-efficiency characteristics to maximize the performance of load circuits.

The block diagram of a battery-powered cellular handset chip with integrated power management units is shown in Fig. 1.2 [14]. Several on-chip LDOs are used as post regulators to provide voltage supply to digital, analog and RF parts with different demands. Output capacitors are needed for stability and transient issues. Since the cellular phone works in standby mode in most time, the PMU should have low static power consumption to prolong the battery life. Longer battery life in modern portable

electronic devices is a key factor to win a large market share.

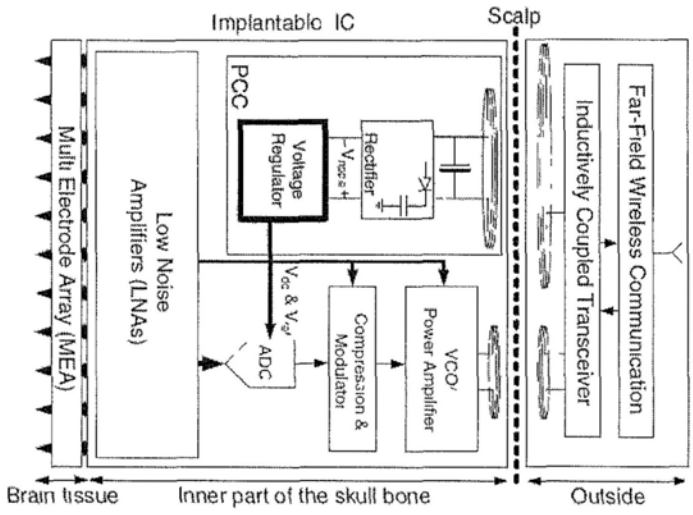

Fig. 1.1 A wireless-powered energy-autonomous system for brain implant application [13]

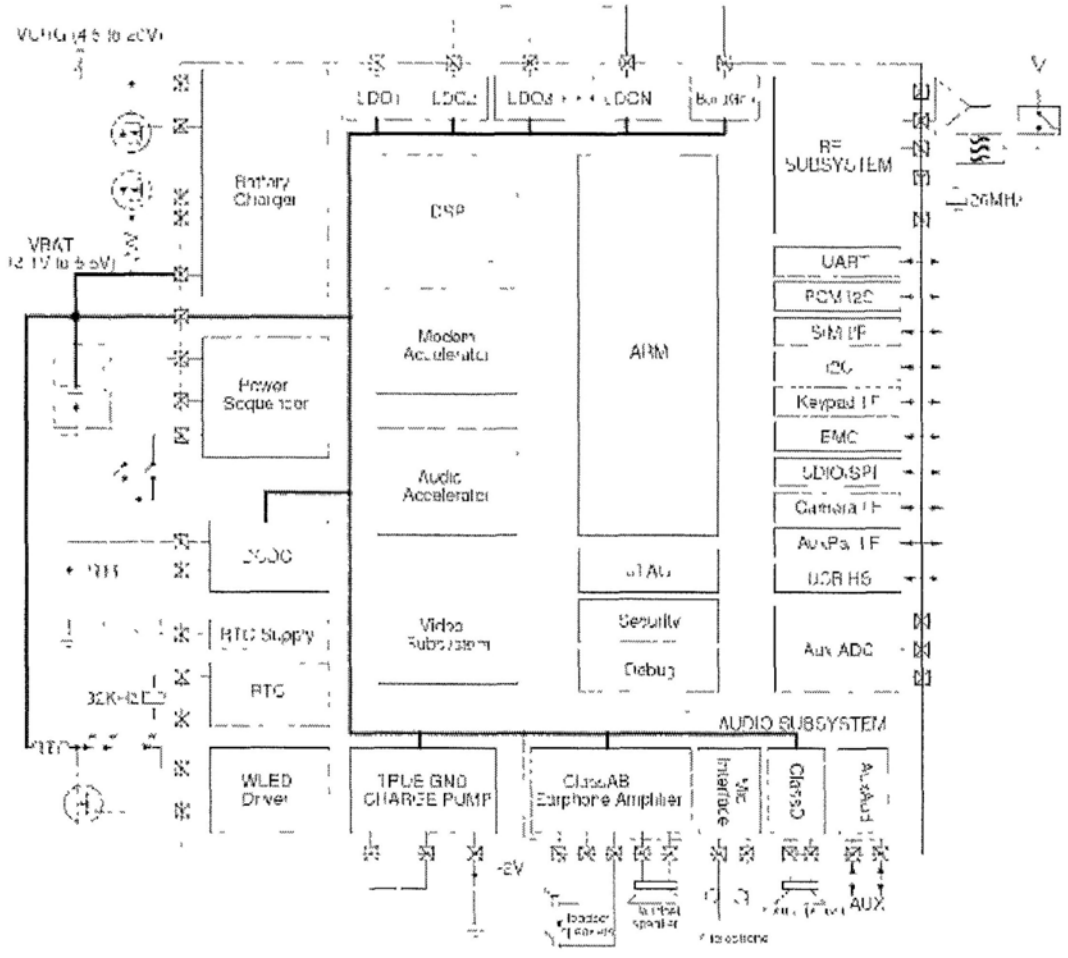

Fig. 1.2 Block diagram of a cellular handset chip with integrated PMU [14]

1.2 Basic understanding of the operation principle and power efficiency of LDO

The LDO circuit can be partitioned into four functional blocks: the reference, the pass element, the sampling resistor, and the error amplifier [15], [16]. The pass elements can be PNP bipolar transistor, NMOS transistor, PMOS transistors, etc. LDO with PNP pass element has a high quiescent current and low efficiency, which are not ideal in applications where maximizing efficiency is a priority. Moreover, the bipolar transistors cannot be implemented in standard CMOS technology. The NMOS pass element is most advantageous due to its low on resistance. Unfortunately, the gate drive difficulties make it less than ideal in applications and, as a result, there are few NMOS LDOs available. PMOS devices have been significantly developed and now have performance exceeding most bipolar devices. Typical LDO topology with PMOS as pass element is shown in Fig. 1.3. The basic operation can be understood easily through Fig. 1.4. In the saturation region (regulation region), the series pass element acts like a constant current source, in terms of the gate-to-source voltage. Under different load conditions, V_{SG} of power transistor controls the LDO to supply the demand output load and keep the LDO output regulated. As the input voltage nears the output voltage, a critical point exists at which the voltage regulator cannot maintain a regulated output. The point at which the LDO circuit begins to lose loop control is called the minimum input voltage (V_{IN_MIN}). The input/output difference at this point is defined as the dropout voltage (V_{DO}) at this particular load condition. Below V_{IN_MIN}, LDO can no longer regulate the output. In the dropout region, the series pass element

limits the load current like a resistor. Moreover, V_{SG} of power transistor is not a function of the control loop, but is a function of the input voltage. In other words, the regulator control loop cuts off and V_{SG} begins to depend on the decreasing input voltage. Thus, when the input voltage decreases further, the control voltage (V_{SG}) also decreases in proportion to the decreasing input voltage. In dropout region, the magnitude of the dropout voltage depends on the load current and the on resistance (R_{ON}) of the series pass element. It is given by

$$V_{DO} = I_{OUT} R_{ON} . \tag{1.1}$$

Throughout the dropout region, the output voltage cannot be maintained any more by the control loop since the control loop is electrically disconnected at the output of the controller and then the pass device acts like a resistor. Therefore, the output voltage can be pulled down to the ground by the load.

Typical measurement method of V_{DO} is to measure the input/output differential voltage when V_{OUT} decreases to below 100 mV of its nominal value [17].

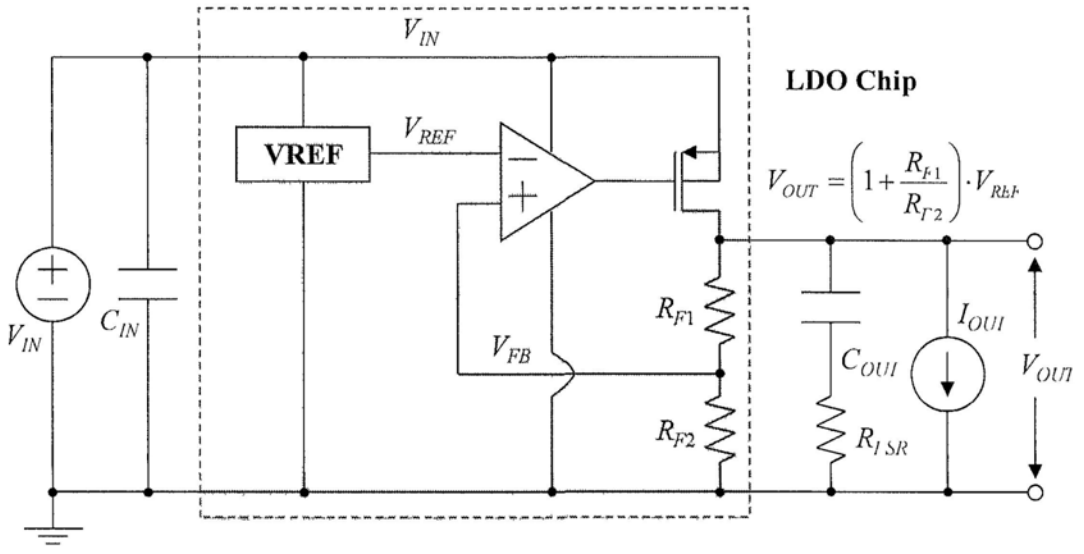

Fig. 1.3 Typical LDO topology with PMOS as pass element

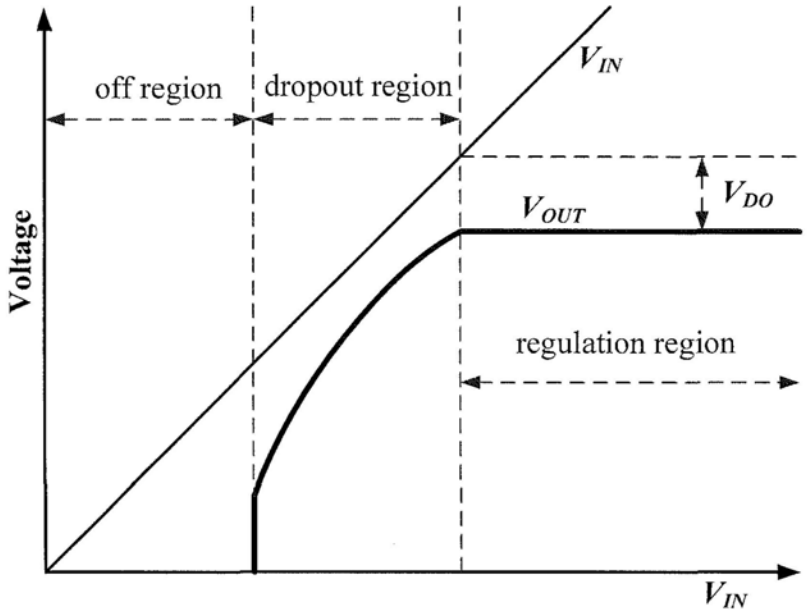

Fig. 1.4 Typical input/output voltage characteristics of a LDO

Since the load current is provided through the pass element, the power efficiency is highly dependent on input/output difference. While dropout voltage decides the minimum input/output difference, a smaller dropout voltage means higher efficiency.

Another issue related to power efficiency of LDO is its quiescent current I_q, which is consumed by LDO itself and the value equals the currents difference between input and output. Obviously, less I_q consumed leads to higher efficiency.

Based on above analysis, it can be noted that the efficiency of a LDO is limited by the quiescent current and dropout voltage as follows:

$$\eta = \frac{V_{OUT} I_{OUT}}{V_{IN} I_{IN}} = \frac{V_{OUT} I_{OUT}}{V_{IN}(I_{OUT} + I_q)} < \frac{V_{OUT}}{V_{IN}} < 1 - \frac{V_{DO}}{V_{OUT} + V_{DO}} . \quad (1.2)$$

To have a high efficiency LDO, dropout voltage should be minimized. In addition, the input/output voltage difference must be minimized since the power dissipation of LDOs accounts for the efficiency (power dissipation = $V_{DO} \bullet I_{OUT}$). The input/output voltage difference is an intrinsic factor in determining the efficiency regardless of the

load condition.

Quiescent current influences the efficiency not too much, especially in heavy-load condition. However, many circuits only consume high power in active mode, and work in standby mode with very small power consumption in most of time. Lower quiescent current is also very important to save power consumption to prolong the battery life, especially in today's portable electronic equipments. Fig. 1.5 shows an example of LDO power efficiency changing with I_q in different load conditions (V_{IN} - V_{OUT} = V_{DO} = 200mV in this example). For typical CMOS LDOs with I_q around 100 μA [18], the efficiency is less sensitive to I_q in heavy-load conditions, e.g., I_{OUT}= 25 mA. However, the efficiency can be improved around 10% when I_{OUT} decreases to 1 mA. If the standby current is only 100 μA, power efficiency can be improved around 81.8% (45% to 81.8%) when I_q changes from 100 μA to 10μA. Obviously, power efficiency is more sensitive to I_q with the decrease of standby current of load circuits.

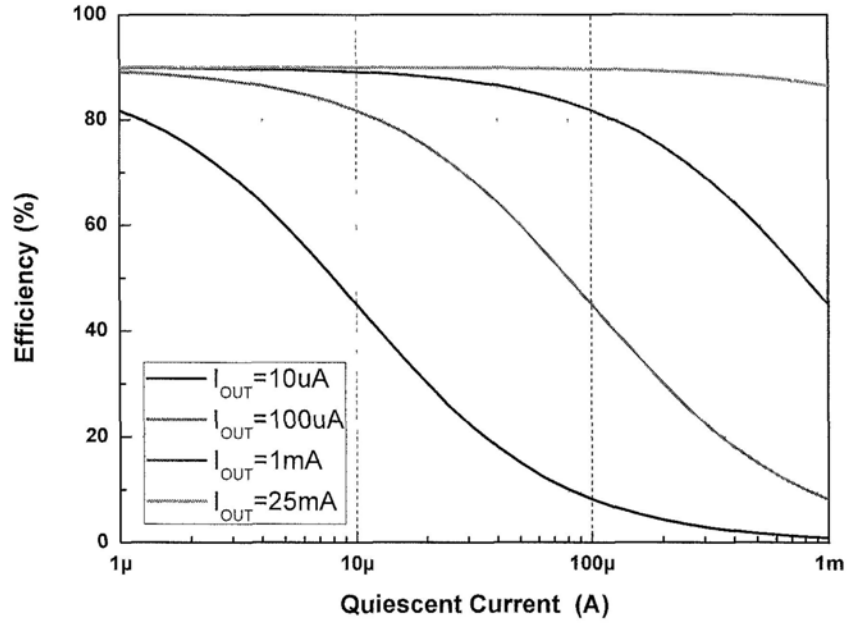

Fig. 1.5 LDO power efficiency changing with I_q in different load conditions

1.3 Challenges in design of LDO in nano-scale CMOS technologies

With the CMOS technology moving towards to nano-scale even deep nano-scale level, there are more challenges in LDO design.

(1) Voltage scaling

Operation voltage is down with the scale of the minimal channel length of MOS transistors. For example, the maximum operation voltage is only 1 V in standard 90-nm CMOS technology. Moreover, low-voltage operation is very important in the systems in nano-scale technologies to save the power. Many circuits work below 1 V (which is below the bandgap voltage of about 1.25V) or even under 0.5-V supply [19], [20]. In this case, new circuit structure is needed to replace the traditional bandgap voltage reference to meet the low-voltage operation.

(2) Channel-length modulation effect

Short channel-length effect increases the g_{ds} of the MOS transistors thus decreases the output resistance, which leads to the degradation of system's loop gain. This means worse line/load regulations and PSRR for LDOs are resulted. Moreover, the decrease of on resistance of power transistors degrades the isolation between input and output of a LDO, and this further degrades the PSRR performance.

1.4 Research goal and thesis outline

The research goal of this thesis is to design some LDOs in nano-scale CMOS technologies for energy-aware wireless SoC, especially remotely- and battery-powered

systems, with the solutions for the challenges mentioned above. More specifically, fully integrated voltage regulators with low-voltage operations for remotely powered energy-autonomous devices, fully integrated LDO with fast transient and good DC regulations for battery-powered SoC, and high-PSRR LDO for RF circuits. All of them are implemented in nano-scale CMOS technologies and feature with low-power performances comparing with some state-of-the-art works with same applications.

This thesis is the integration of three low-power LDOs with the features mentioned above. In Chapter 2, a fully integrated CMOS LDO with only 700-nA quiescent current is presented. It was fabricated in 0.18-μm CMOS technology and has been applied in a passive Radio-Frequency Identification (RFID) tag IC. A CMOS voltage reference with sub-1-V operation and a reliable POR circuits are also designed and analyzed. Then, an output-capacitorless fast-transient LDO fabricated in 90-nm CMOS technology is proposed in Chapter 3. The LDO features minimal 6-μW power consumption and 100-mA load capability. While the transient overshoot and undershoot voltages are decreased by 7 times with the direct capacitor-coupling technique. Moreover, the gain-enhanced structure provides sufficient loop gain to improve line regulation to 3.78 mV/V and load regulation to 0.1 mV/mA, respectively. The low-I_q, high-I_{OUT}, fast-transient and excellent-regulation characteristics make it be a good solution to the digital or mixed-signal circuits in battery-powered energy-aware wireless SoC. To provide a very clean voltage supply to RF or high-performance analog circuits, a 0.18-μm CMOS LDO with best PSRR of -85 dB at 2.5 MHz is presented in Chapter 4. With a single 4.7-μF ceramic output capacitor and under

25-mA load condition, it can achieve PSRR better than -55 dB up to 5 MHz. This LDO also features 15-μA low I_q due to the proposed embedded ripple feed-forward path for improving PSRR and saving power consumption at the same time. Finally, the conclusions of this thesis are given, and the future work is summarized.

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CHAPTER 2. Design of Fully Integrated CMOS Voltage Regulator for Passive RFID Tag ICs♣

Radio-Frequency Identification (RFID) is one of the widely used techniques in wireless sensor nodes, supply-chain management, security, movement tracking, environment monitoring, medical care, etc. [1]–[3]. An RFID system contains readers and tags. There are three types of RFID tags including active, semi-active and passive RFID tags [4]. The passive RFID tag, due to its low cost and small chip area, is preferred when its performance can meet the requirements of application.

Fig. 2.1 shows a typical diagram of the passive UHF RFID tag consisting of an antenna and a tag IC. There are three parts in the tag IC, which are the power-management front-end (rectifier & multiplier and voltage regulator), the signal front-end (demodulator, modulator and clock generator) and the digital part (baseband processor). The brief principle of RFID tag can be described as follows. The rectifier and multiplier convert the received RF signal power from the antenna into a sufficiently high DC voltage V_M, which is then further regulated by low-dropout linear voltage regulator (LDO) to provide a stable voltage supply V_{REG} to other blocks. The demodulator detects ASK-modulated signal and send it to be processed by the baseband processor. After received the signal from baseband processor, the modulator

♣ The material presented in this chapter is extracted from two published papers:
"A CMOS Voltage Regulator for Passive RFID Tag ICs," International Journal of Circuit Theory and Applications, published online, Oct. 2011.
"Power-On-Reset Circuit with Power-Off Auto-Discharging Path for Passive RFID Tag ICs," IEEE International Midwest Symposium on Circuits and Systems, Aug. 2010.

changes the effective impedance of the antenna to achieve ASK modulation for backscattering signals back to the RFID tag reader.

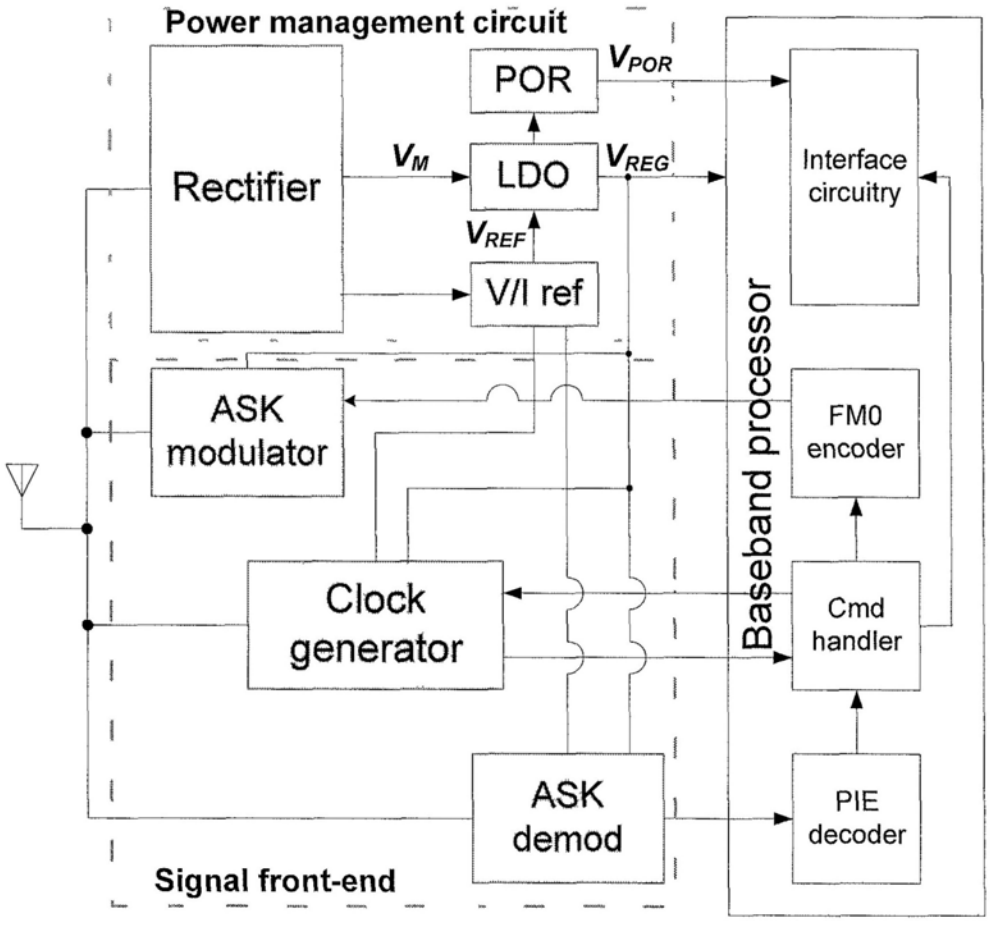


Fig. 2.1 Diagram of a typical passive RFID tag

The main design challenges are to design a high-efficiency rectifier and achieving ultra low-power consumption in each part of the tag IC [5], [7], [8]. Moreover, the voltage regulator is very important as it provides the regulated supply to the RF front-end and digital blocks in the passive RFID tag.

A low-voltage low-power voltage regulator [9] is proposed firstly in this chapter. The design demonstrates the tradeoff considerations among the chip area, the precision of the output voltage, the power consumption of the voltage regulator and its

transient response. Then an improved power-on-reset (POR) circuit target for more reliable operation is proposed [10]. Both of them have been fabricated and the measurement results will be shown.

This chapter is organized as follows. Section 2.1 includes the analysis of the design considerations of a voltage regulator for passive RFID tag IC. The circuit implementation of the proposed regulator is presented in Section 2.2. The measurement results are given in Section 2.3. Then an improved POR circuit fabricated in 90-nm CMOS technology is introduced in Section 2.4 for more stable operation. Finally, conclusions and discussions are given in Section 2.5.

2.1 Design Considerations

Voltage regulator is responsible to provide stable power supply to the front-end and other circuits in the tag. Meanwhile, the tag has to function properly when there is little or even no RF power available during backscattering, attributed to the large on-chip capacitors of the voltage regulator [8]. Generally, a voltage regulator in a passive RFID tag usually includes a voltage reference, a voltage regulation circuit and a POR circuit.

2.1.1 Voltage Reference

The main challenge for the voltage reference design in passive RFID tag IC is to achieve low-power and low-voltage operation at the same time. Many low-power low-voltage reference circuits have been proposed [11], [12], but all of them need large diodes or parasitic BJTs which have a large turn-on voltage. Moreover, the on-chip

resistance is large in ultra-low-power design. All-MOS nano-power reference circuits have been proposed in [13] and [14], but the requirement of high-voltage devices increases the mask cost and no trimming procedure can be done, which may lead to a low production yield. The voltage reference circuit reported in [15] can solve these problems, but a clock signal is required, which makes the circuit and its applications become complicated. Moreover, switching noise degrades circuit performance, and the clock generator for the switching signal increases the overall power consumption of the reference circuit. As a result, both approaches are not preferred in passive RFID tag IC design. Based on the above analysis, it reveals that a low-voltage low-power voltage reference with small chip area is needed to meet the strict requirements of passive RFID tag IC. This reference circuit should allow for easy trimming to achieve a high production yield.

2.1.2 Voltage Regulation

The regulation circuit should have a simple structure for low-power operation. It should also consist of a large output capacitor for energy storage, which can also minimize the voltage ripples and improve the immunity to the variations of the load or the power supply. Due to such ultra-low power condition, any internal high-impedance node is not favorable due to the long charging and discharging times. A typical structure is a series regulator based on negative feedback since it is more power efficient than the shunt regulator counterpart [17].

2.1.3 Power-on Reset

The POR circuit is very important for the RFID tag design due to its two major functions: 1) generating the whole chip reset signal when the tag is powered up by the electromagnetic field provided by the reader, and 2) protecting the chip circuit from malfunctioning when the power supply voltage drops to a certain level [4]. A very low-power and simple solution has been proposed in [18], but the power-on threshold has not been considered carefully to provide accurate operation.

Based on the above considerations, a low-power voltage regulator is proposed, and its structure is shown in Fig. 2.2. A self-biased mutually compensated voltage reference is developed to provide a stable voltage reference with a low temperature coefficient (TC) under low-supply operation. A single-stage low-dropout regulator is used as voltage-regulation circuit. The large output capacitor achieves the functions of both the energy storage and the dominate-pole compensation. Moreover, a POR circuit with hysteretic comparator is adopted to provide the POR pulse signal for the digital circuit. Undoubtedly, the POR threshold is accurate due to the comparator structure.

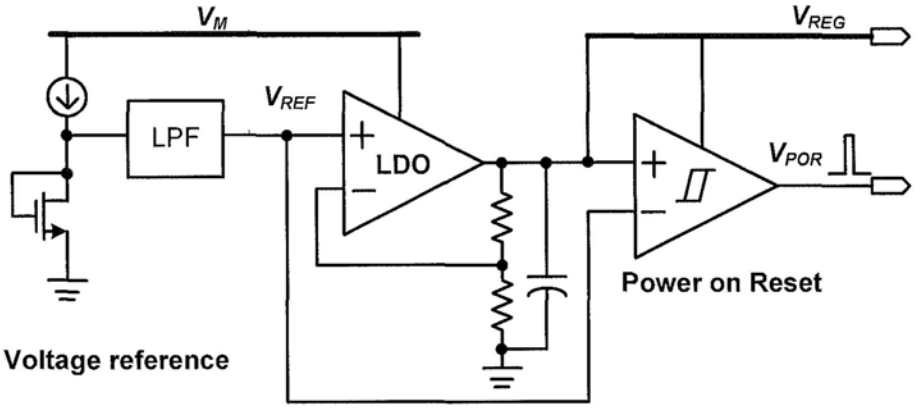


Fig 2 2 Structure of the proposed voltage regulator

2.2 Circuit Implementation

In this section, the circuit design of the proposed voltage reference, voltage regulation and POR circuit will be described individually.

2.2.1 Sub-1-V nano-power voltage reference

Achievability of zero temperature coefficient (ZTC) has been confirmed in CMOS technologies [18]. In this design, a low-voltage low-power temperature-insensitive voltage reference is obtained by biasing a diode-connected NMOS transistor at the ZTC point with an internal current source. The schematic of the proposed voltage reference is shown in Fig. 2.3. It consists of a start-up circuit, a *V*-to-*I* converter, a core reference generator and an *RC* low-pass filter.

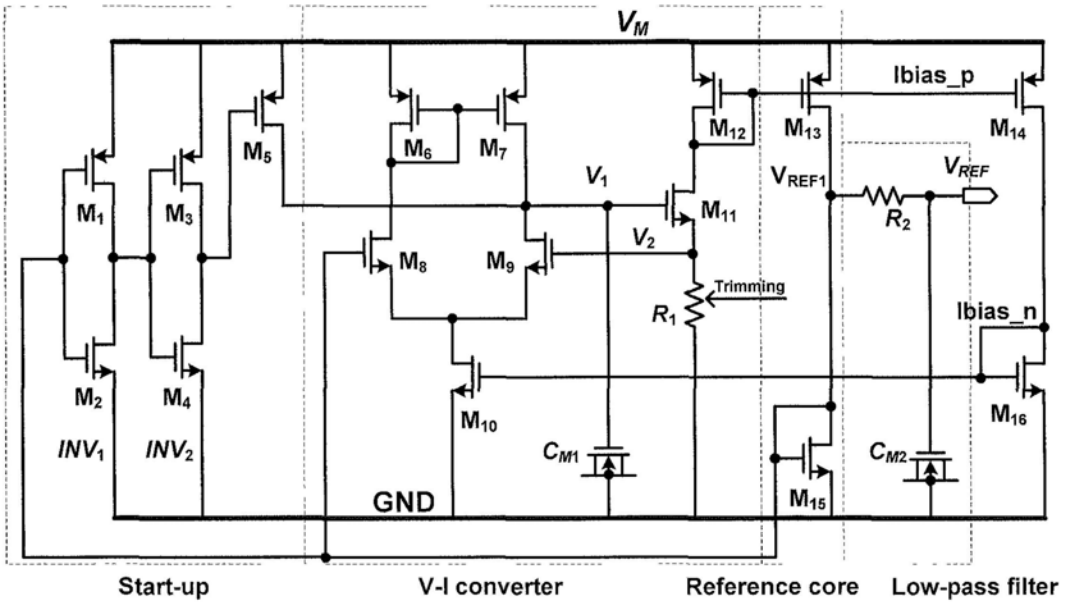


Fig. 2.3 Schematic of the voltage reference

It can be found easily that the circuit has two operation points. One is the zero bias point, which means that all branch currents are zero, and another is the targeted

operation point [19]. The start-up circuit, consisting of INV_1, INV_2 and M_5, is adopted to avoid working at the zero bias point. Initially, if the circuit works at its zero bias point when V_M is being powered on, V_M reaches the threshold voltage of M_5 to turn on M_5 and V_1 is charged. Then, a current is generated and it is mirrored from M_{12} to M_{13} and M_{14}. With continuously charging at V_1, both the drain-source current and voltage of M_{15} increase at the same time. When V_{REF1} increases to the threshold voltage of INV_1, the gate voltage of M_5 is high and M_5 will be off. Then, V_{REF1} reaches the designed value and the circuit works at the targeted operation point. To improve the power-supply ripple rejection (PSRR) and noise performance, an RC low-pass filter, composing of R_2 and C_{M2}, is introduced. Both C_{M1} and C_{M2} are MOS capacitors which are used to decrease the chip area.

Based on the analysis in [18], the reference voltage equals to:

$$V_{REF} = V_{THN} + \sqrt{2I_{D15} \Big/ \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_{15} \right]}. \tag{2.1}$$

Since the bias current I_{D15} is generated by V_{REF} through the V-to-I converter, (2.1) can be rewritten to

$$V_{REF} = V_{THN} + \sqrt{2V_{REF} \Big/ \left[\mu_n C_{ox} \left(\frac{W}{L} \right)_{15} R_1 \right]}. \tag{2.2}$$

The temperature dependence of the reference voltage can be obtained by differentiating (2.2) with respect to temperature. Setting the result to zero, the following relationship can be obtained.

$$\frac{\partial V_{THN}}{\partial T} = \sqrt{\frac{I_{D15}}{2\mu_n C_{OX}\left(\frac{W}{L}\right)_{15}}}\cdot\left(\frac{1}{\mu_n}\cdot\frac{\partial \mu_n}{\partial T}+\frac{1}{R_1}\cdot\frac{\partial R_1}{\partial T}\right). \tag{2.3}$$

The threshold voltage V_{THN} has a negative TC equal to α and the mobility μ_n has negative TC equal to α_μ. To achieve low-power performance and small chip area, non-salicide high-resistive poly resistors (about 1 kΩ/sq.) are used. Their TCs equal to

$$TC_{HR} = 1.0 + t_{c1}(T-25) + t_{c2}(T-25)^2, \tag{2.4}$$

where $t_{c1} = -8.34\times10^{-4}$ and $t_{c2} = 1.3\times10^{-6}$. t_{c2} can be ignored in the temperature range concerned. In this case, (2.3) can be simplified to

$$\left(\frac{W}{L}\right)_{15} = \frac{I_{D15}}{2\mu_n C_{OX}\alpha^2}\cdot\left(\frac{\alpha_\mu}{\mu_n}+\frac{t_{c1}}{R_1}\right)^2. \tag{2.5}$$

Once the values of I_{D15} and R_1 are designed, the ZTC can be achieved by setting proper $(W/L)_{15}$ based on the above equation.

To improve the yield, a trimming circuit has been adopted to change R_1, so that a proper I_D can be provided to generate a ZTC voltage reference. The trimming circuit is shown in Fig. 2.4. *TxN* (x = 1, 2, 4 and 8) means the top metal connection and the resistance can be decreased by x% through cutting this connection. On the contrary, *TxP* (x = 1, 2, 4 and 8) means the resistance can be increased by x% by cutting this top-metal connection. In this case, the total resistance can be easily trimmed within ±15% by doing the laser cut on the top metal, with trimming step of 1%. The trimming strategy is to compare the measured V_{REF} with the simulated value based on different R_1. It can be

optimized further through TC measurements after the preliminary trimming. The bias current for the trimming circuit should be as small as possible to save the total power consumption.

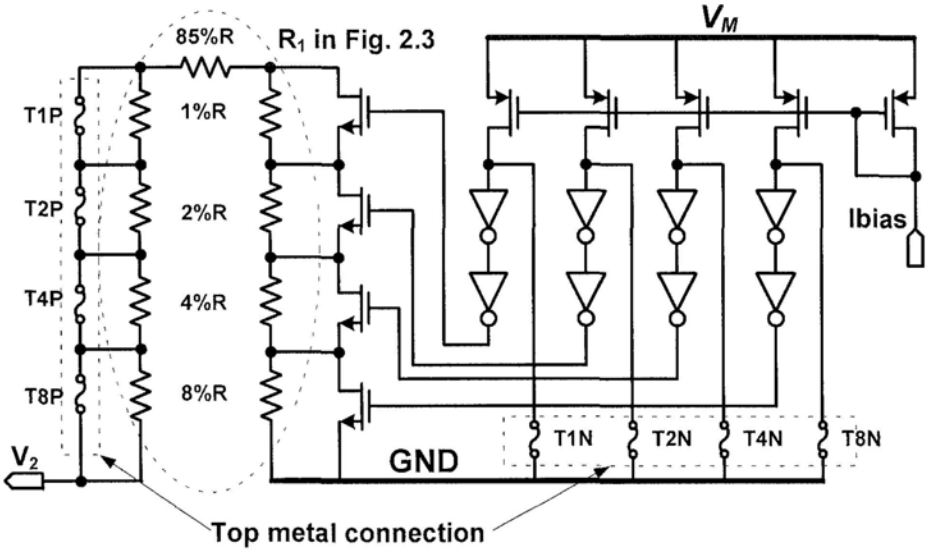


Fig. 2.4 Schematic of the trimming circuit

Comparing with the existing methods, the proposed reference circuit requires less resistance and no BJT devices, thus less chip area is consumed. Moreover, it can be trimmed easily while there is no clock needed. These features make it a suitable solution for the passive RFID tag ICs.

2.2.2 Low-Dropout Voltage Regulation Circuit

To save power and simplify the compensation of the voltage regulator, a single-stage amplifier is adopted to drive the power PMOS transistor directly. The schematic is shown in Fig. 2.5. The input NMOS transistors of the differential pair work in the sub-threshold region for low-power operation, which also makes low-voltage operation possible (the minimum supply can be as low as 1 V if V_{REG} is set to less than 1

V). A large storage capacitor is added at the output of the regulator, and this makes the circuit more stable since other parts can work properly due to the charges stored in this capacitor, even when the supply voltage V_M is discharged to be smaller than V_{REG} in the backscattering stage. Assume that the load current (I_{OUT}) of the regulator is a constant value, the required capacitance ($C_{on\text{-}chip}$) to maintain proper function of the circuits can be calculated when there is little or even no RF power available to the chip during backscattering. It equals to

$$C_{on-chip} = \frac{I_{OUT}\, T}{\Delta V_{REG}}, \tag{2.6}$$

where T is the period when no RF power available. Assume that I_{OUT} of 1 to 3 μA is consumed and it can be acceptable for 20% of V_{REG} decrease, it will not trigger the POR threshold which will be presented later in the next sub-section. A 1.2-nF capacitor is adopted to meet the requirement of the EPC Class-1 Generation-2 standard (T = 12.5 μs) [20].

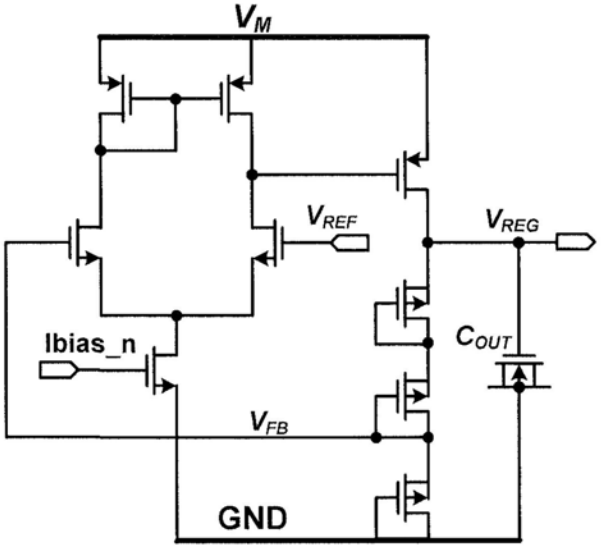


Fig. 2.5 Schematic of the low-dropout voltage regulation circuit

In addition to the energy storage, this capacitor generates a low-frequency dominant pole, which makes the circuit simple and sufficiently stable. In this case, no large compensation capacitor is needed in the internal node of LDO, and this provides the circuit with faster response. The NMOS transistor with shorted drain and source terminals is used to be active capacitor to save the chip area effectively. The unit capacitance of an NMOS transistor in UMC 0.18-μm CMOS technology is about 8 times more than that of a metal-metal capacitor. The short-term and long-term reliabilities of the MOS capacitors used in this design is same as the MOS devices in the circuit since the output voltage of LDO is within the breakdown voltage of the devices in the technology.

The diode-connected PMOS transistors are used to implement the feedback network. This decreases the chip area effectively comparing with resistive feedback network. Moreover, no body-effect issue would exist, which makes all the transistors to have the same performance and the potential division to be more accurate.

The open-loop transform function of this LDO circuit can be expressed as

$$H(s) = \frac{\beta A_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}, \tag{2.6}$$

where β is the feedback ratio (1/3 in this circuit) and A_0 is the DC open loop gain. The dominant pole ω_{p1} and first non-dominant pole ω_{p2} are decided by $\omega_{p1} = \frac{1}{R_o C_{OUT}}$, $\omega_{p2} = \frac{1}{R_{o\_ea} C_{pg}}$, where R_{o_ea} is the output impedance of error amplifier and C_{pg} is the equivalent gate capacitance of power transistor. The simulated bode plots with

1.8-V V_M and under different load conditions are shown in Fig. 2.6. The information on gain, dominant pole (-3dB frequency, f_{-3dB}), phase margin and unity-gain frequency are summarized in Table 2.1. The phase margin is no less than 46° even under 50-μA load current.

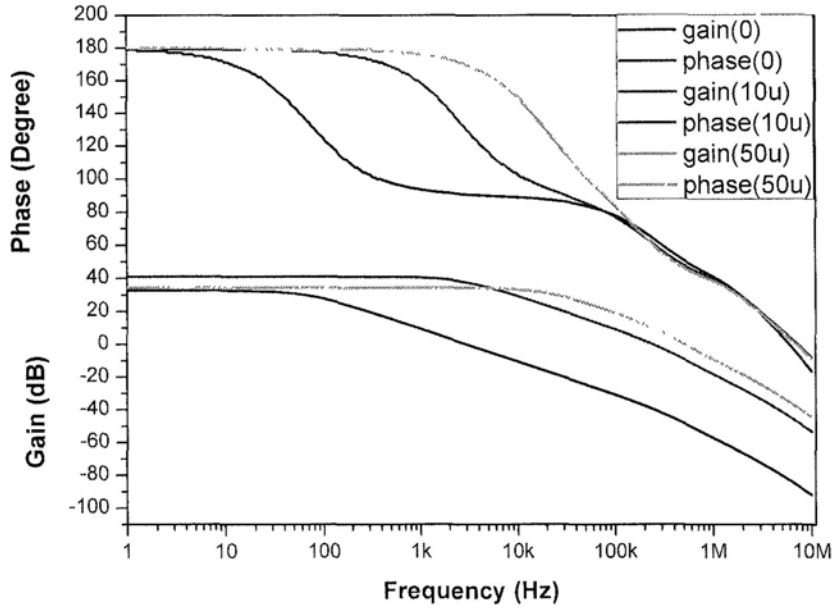


Fig. 2.6 Bode plots of LDO circuit under 0-, 10- and 50-μA load current

Table 2.1 AC simulation results of LDO circuit under different load conditions

Load current (μA)	DC gain (dB)	Phase margin (degree)	f_{-3dB} (kHz)	UGF (kHz)
0	32.5	90	0.069	2.8
10	41	61	2.63	240
50	34.3	46	18.5	520

2.2.3 POR Circuit

In this design, the POR mechanism is designed to reset the digital synchronous baseband processor when the POR signal is high and to release the control of the

baseband processor when the POR signal is low. Therefore, a pulse is needed to reset the baseband circuit.

As the baseband circuit is based on EPC C1G2 protocol, it will only control the tag to backscatter signal with a valid encoded sequence when

1) certain sequential cells in the processor have a valid output status (e.g., some output vectors of the state machine and some parameters over 15 bits), and

2) the output status is kept or changed correctly for a long period when backscattering data back to the reader.

In addition, the reader neglects any correct or wrong response from tag when it is powering up the tags. In that case, correct operation of whole RFID system can be ensured when V_{REG} is rising and POR keeps at low level.

The proposed POR circuit is shown in Fig. 2.7. It provides the reset signal by detecting the output voltage of the regulator accurately due to the precise voltage reference and the comparator structure.

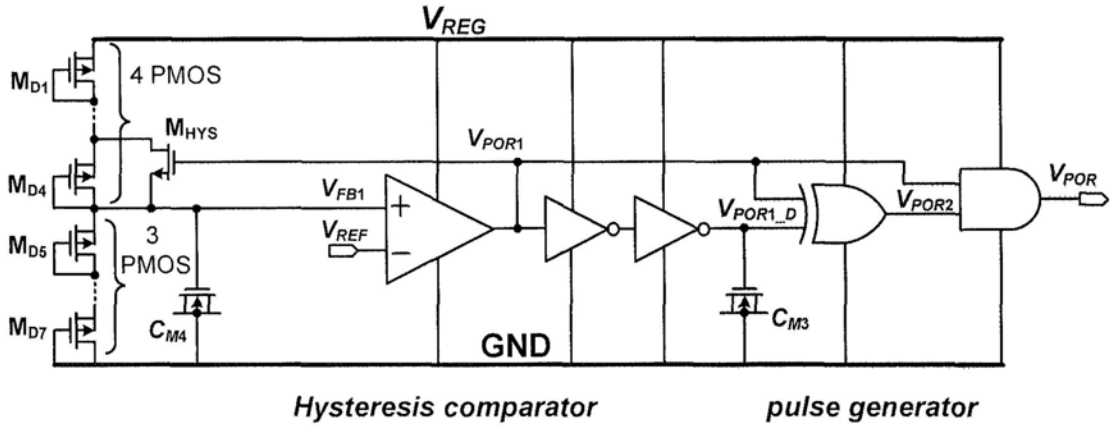


Fig. 2.7 Schematic of the proposed POR circuit

As shown in Fig. 2.7, the proposed POR circuit provides the reset signal by

comparing V_{REF} with V_{FB1}, which is the scaled V_{REG} obtained from a low-power voltage divider formed by series-connected M_{D1}–M_{D7}. When V_{REG} is low, V_{POR} remains low. Once V_{REG} is sufficiently high, a low-to-high transition is generated at the output of the voltage comparator (i.e. V_{POR1}). The switch M_{HYS} is turned on momentarily, and then the threshold of the comparator is changed to a lower value, which will enhance its noise-rejection ability to avoid any possible wrong operation.

The ideal time sequence of the POR circuit is shown in Fig. 2.8. With the XOR operation between V_{POR1} and its delayed signal V_{POR1_D}, a pulse signal can be generated in each power-on and power-off periods. To eliminate unwanted pulses during the power-off period, an AND gate with V_{POR1} and V_{POR2} as two input terminals are introduced. In this case, the pulse is generated only during power-on period, and this guarantees the correct operation of the baseband circuit.

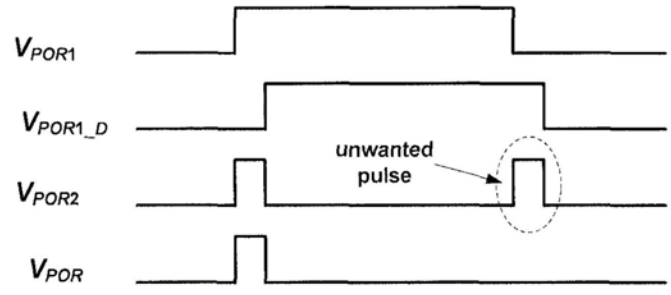


Fig. 2.8 Ideal time sequence of POR circuit

In this design, the power-on threshold is set to be 89% of the nominal output voltage, and the hysteresis is 12% of the nominal output, which is about 180 mV. The pulse period is 150 ns, which ensures the proper operation of the designed baseband circuit. This POR circuit also features low-power performance, with only 150-nA quiescent current (simulated) consumed in typical condition.

2.3 Experimental Results

The proposed voltage regulator has been fabricated in UMC 0.18-μm mixed-mode RF CMOS technology. The chip micrograph is shown in Fig. 2.9. The chip area, including a 1.2-nF storage capacitor and a buffer for POR testing, is 0.2236 mm^2.

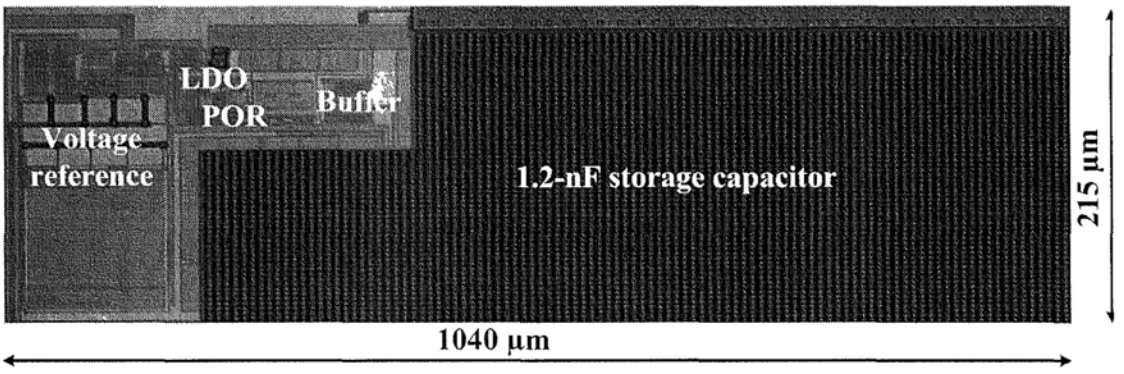
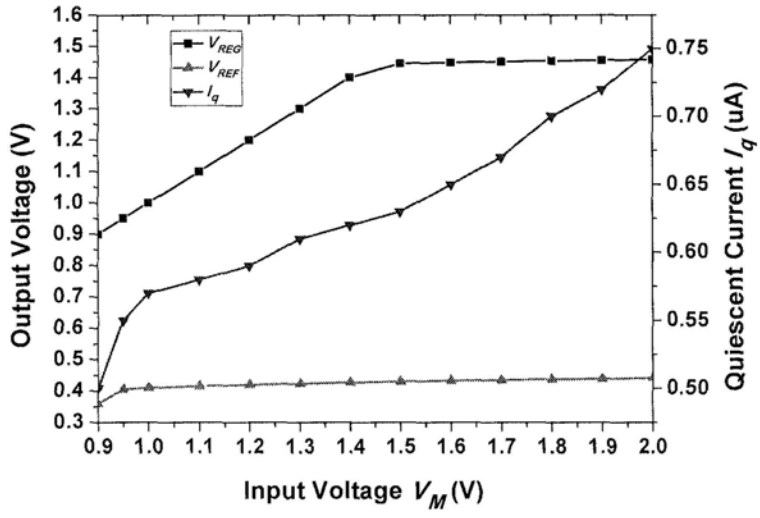
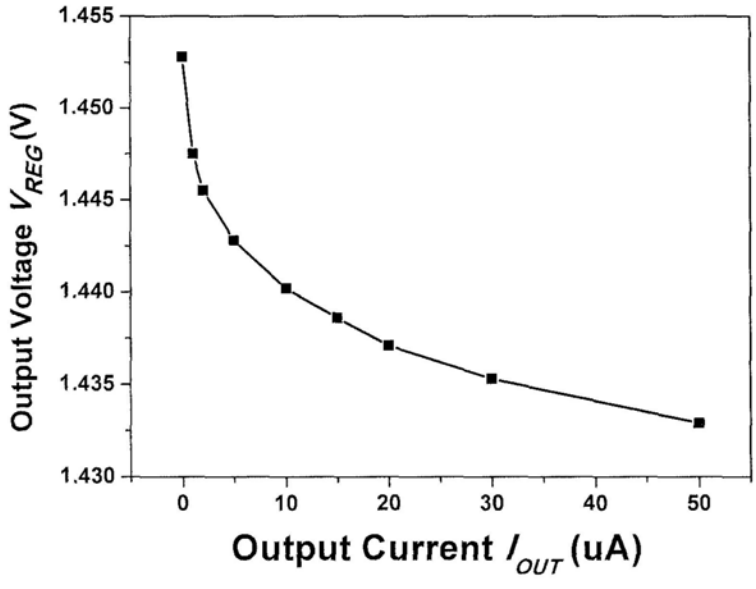


Fig. 2.9 Chip micrograph

The typical DC performance is shown in Fig. 2.10. The reference voltage varies from 500 mV to 508 mV when input voltage V_M changes from 1 to 2 V, and the output voltage V_{REG} varies from 1.445 to 1.456 V when V_M changes from 1.5 to 2 V. The regulator achieves a quiescent current (I_q) of 570 nA and 750 nA under a 1-V and 2-V supply, respectively. Moreover, the regulator can provide output current up to 50 μA and V_{REG} has 20-mV variation from no load to 50 μA.



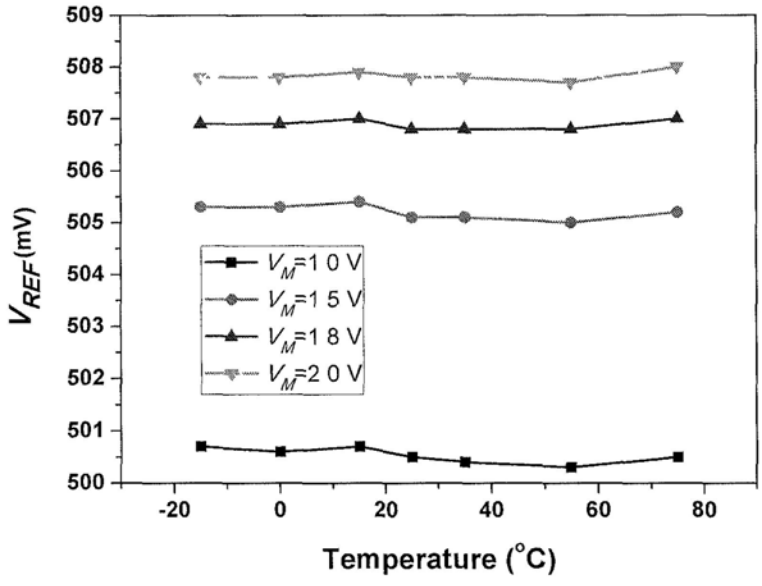
(a)



(b)

Fig. 2.10 Measured DC performance (a) V_{REG}, V_{REF} & I_q vs. V_M and (b) V_{REG} vs. I_{OUT}

Measured TC characteristics of temperature changing from -15°C to 75°C are shown in Fig. 2.11. Under the supply voltage V_M between 1 V and 2 V, the best and the worst TCs of the voltage reference are 5 and 9 ppm/°C, respectively. Under V_M of 1.8 V, V_{REG} has variation of 5.7 mV, and the achieved TC is 43 ppm/°C. I_q is proportional to the absolute temperature, changing from 0.67 to 0.79 μA.



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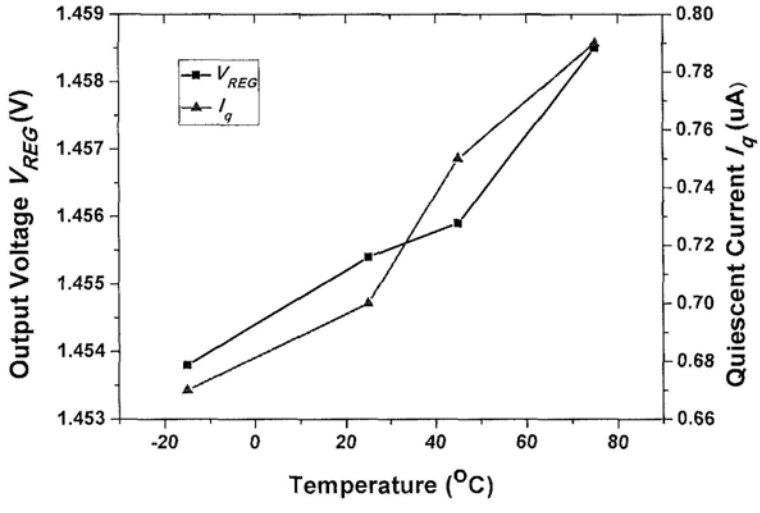
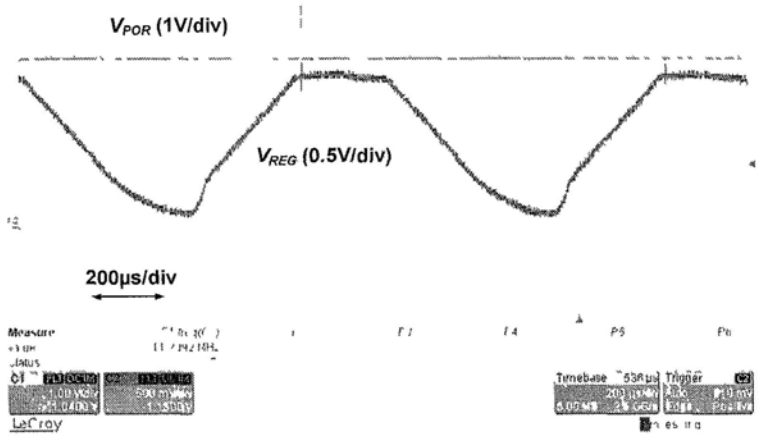


(b)

Fig. 2.11 Measured TC performance

(a) V_{REF} vs. temperature under different V_M and (b) V_{REG} & I_q vs. temperature

Fig. 2.12(a) shows the periodic power-on and power-off waveforms of V_{REG}. The regulator can be started up without overshoot during 400 μs, and the POR signal can be generated at each cycle of power on. The pulse width of the POR signal is about 150 ns, which can be shown in Fig. 2.12(b). It is guaranteed to meet the requirements of the designed baseband processor.



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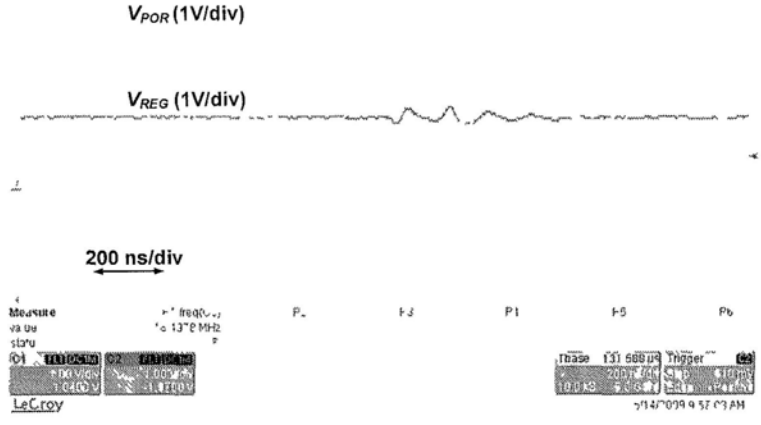
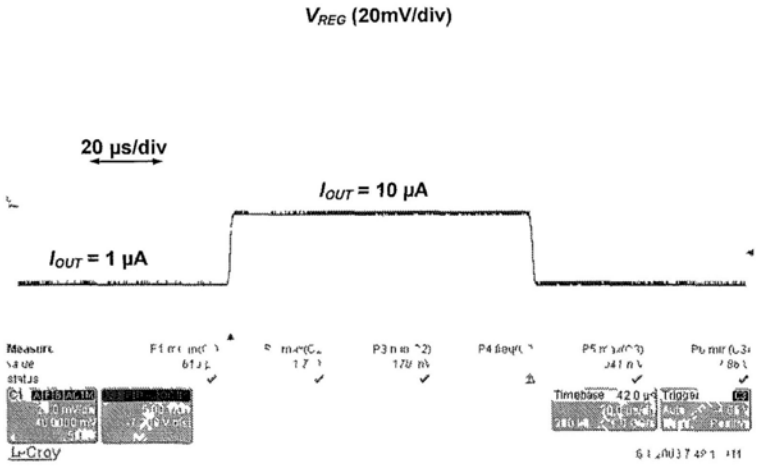


(b)

Fig. 2.12 (a) Power-on and power-off response of the voltage regulator and (b) zoom-in of (a)

Load transient responses, shown in Fig. 2.13, prove the stability of the regulator and show that the maximum voltage spike is less than 5 mV when load current changes from 1 µA to 10 µA, or even from 10 µA to 50 µA. Moreover, the recovery time is less than 20 µs.



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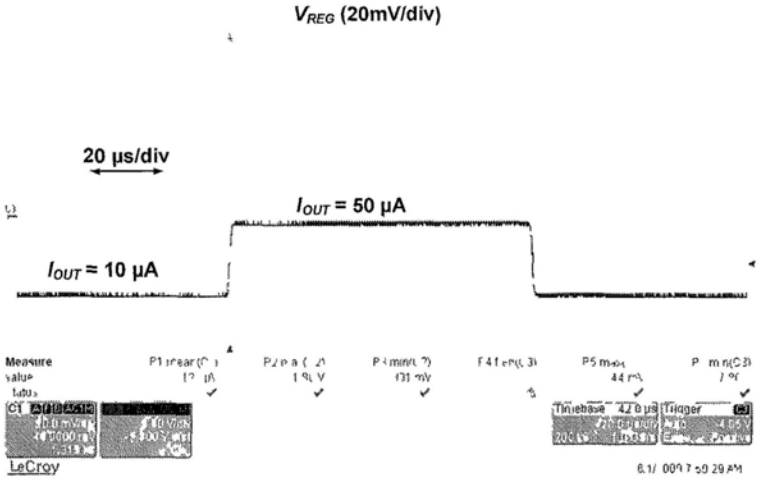
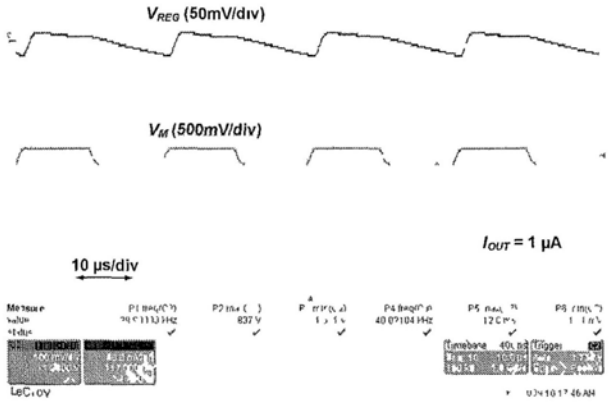


(b)

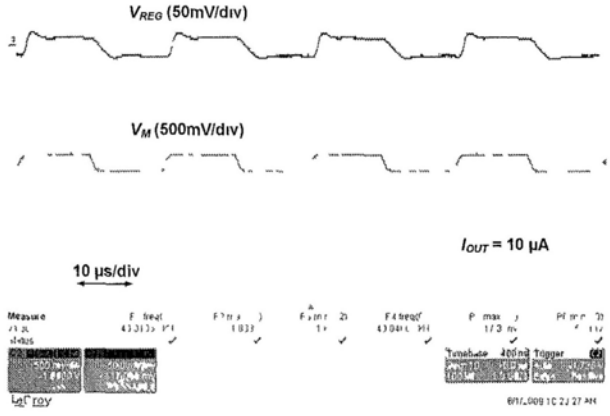
Fig. 2.13 Load transient response

(a) I_{OUT} from 1 µA to 10 µA and (b) I_{OUT} from 10 µA to 50 µA

The line transient responses are measured by applying an EPC Class-1 Generation-2 compatible input pulse (40-kHz frequency) [20], which are shown in Fig. 2.14. In this measurement, the V_{REG} has about 25-mV variation with less than 10-mV spike when V_M changes from 1.8 to 1.6 V.



(a)



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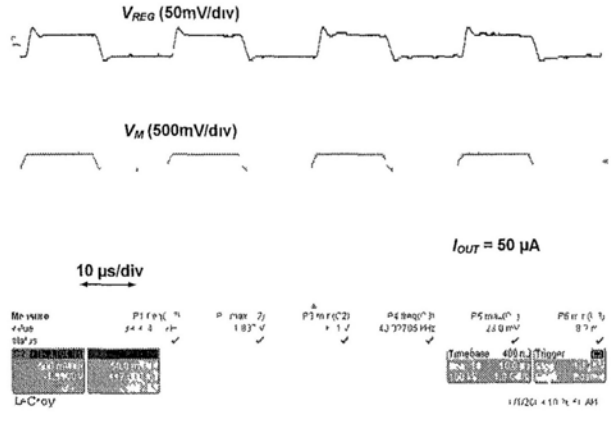


(c)

Fig. 2.14 Line transient response under

(a) 1-µA, (b) 10-µA and (c) 50-µA output current

Finally, a performance comparison with recently published works targeted for passive RFID applications and fabricated in CMOS technologies is shown in Table 2.2. It shows that the proposed voltage regulator has balanced performance among the power consumption, the output voltage precision, the load capability and the chip area. Moreover, the proposed trimming strategy ensures the production yield.

Table 2.2 Performance comparison with recently published works

	[15]	[21]	[6]	This work
Year	2008	2009	2009	2010
Features	Switched-capacitor CMOS voltage reference, digital clock is needed	Fully on-chip LDO with bandgap voltage reference	Multi-output power management unit with bandgap voltage reference	Low-power voltage regulator with POR and CMOS voltage reference
Technology (μm)	0.35	0.18	0.18	0.18
Chip area (mm^2)	0.0490	0.1044	0.5668	0.2236
Input voltage (V)	1 – 4	> 2.1	N/A	1 – 2 for V_{REF} 1.6 – 2 for V_{REG}
Output voltage (V)	V_{REF}: 0.1901	V_{REF}: N/A V_{REG}: 1.8	V_{REF}: N/A V_{REG}: 0.5, 1 & 1.7	V_{REF}: 0.505 V_{REG}:1.45
Load capability	N/A	4 mA	35.6 μW	50 μA
Quiescent current (μA)	0.25 – 0.56	28	~2.4	0.7
Line regulation (mV/V)	V_{REF}: 1.44	V_{REF}: N/A V_{REG}: 0.24	V_{REF}: N/A V_{REG}: N/A	V_{REF}: 7.2 V_{REG}: 22
Load regulation	N/A	0.7 mV/4mA	N/A	20 mV/50μA
TC (ppm/°C)	V_{REF}: 16.9	V_{REF}: N/A V_{REG}: N/A	V_{REF}: N/A V_{REG}: N/A	V_{REF}: 9 V_{REG}: 43
Trimming strategy	Capacitance (0.3 – 2.8 pF adjustable)	N/A	N/A	Resistance (±15% adjustable)

2.4 Improved POR Circuit in 90-nm CMOS Technology

As mentioned before, POR circuit is always required in passive RFID tag ICs to achieve whole-chip reset when the tag is powered up by electromagnetic field and to avoid malfunction of the tag IC when the supply voltage drops to a certain level. Some solutions for passive RFID applications have been proposed [22]–[24], but the accuracy of the power-on threshold and the reliability during the switch between power on and power off are not considered carefully. In this section, a low-power POR circuit with hysteresis-comparator structure and power-off auto-discharging path is proposed for passive RFID tag ICs. It features with accurate threshold voltage and reliable pulse signal. The circuit design with detailed analysis and simulation results will be described first, and the experimental results are then given.

2.4.1 Circuit Design

The proposed POR circuit, which consists of a hysteretic voltage comparator and a pulse generator, is shown in the bottom of Fig. 2.15. The reference circuit is also included (top of Fig. 2.15) for helping to describe the principle of operation of the proposed POR circuit.

Reference circuit

The reference circuit provides a stable reference voltage (V_{REF}) and the bias current with small temperature coefficient to other blocks. Both the reference voltage and the bias current are generated by M_{10} based on the mutual temperature compensation

between the threshold voltage and the electron mobility [18]. The start-up circuit, which is formed by three cascade inverters (INV_1–INV_3), has hysteresis. It generates a signal V_{DIS} which is high when the reference circuit cannot start up completely. M_6 is introduced to achieve the hysteresis operation to guarantee the reference circuit is noise-free during the start-up period.

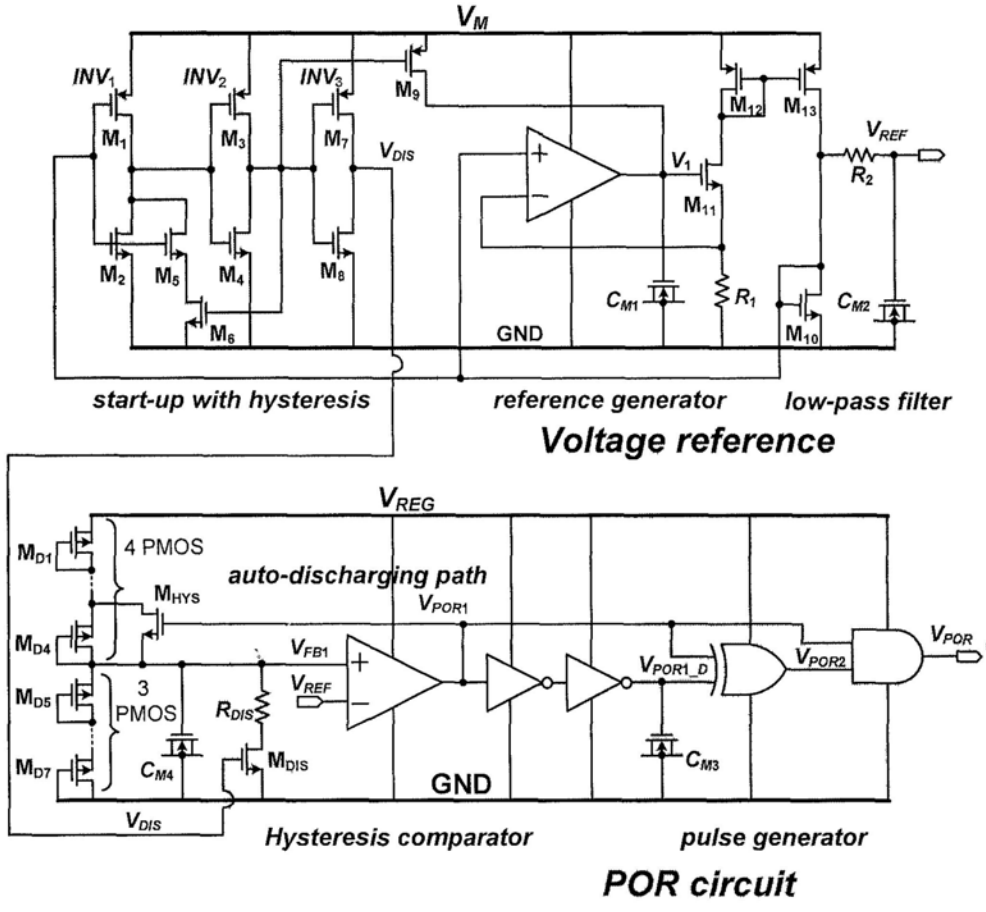
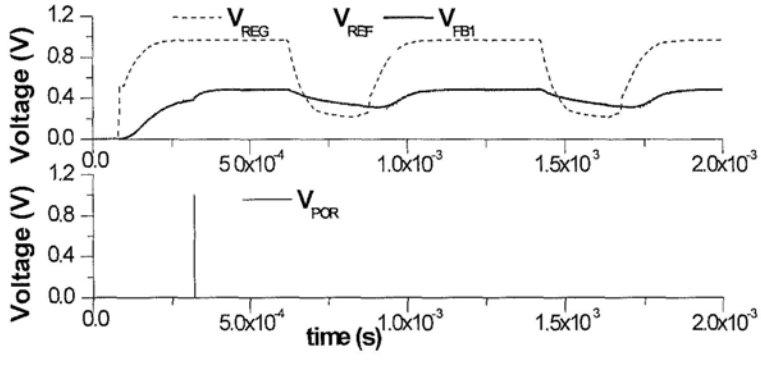


Fig. 2.15 Proposed voltage reference and POR circuit in 90-nm CMOS technology

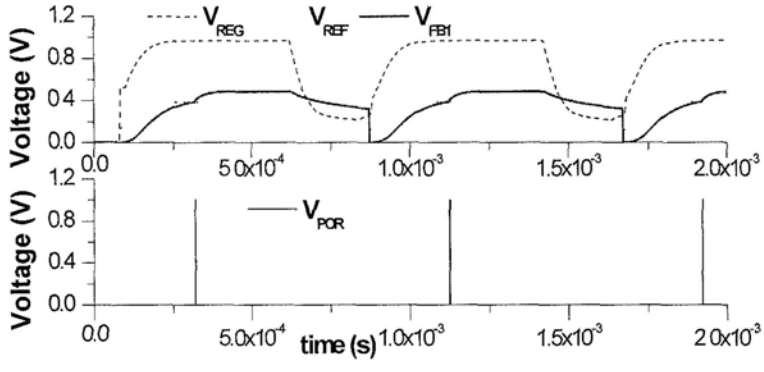
Power-off auto-discharging path for reliable operation

One important design issue of this structure is the large turn-on resistances of M_{D1}–M_{D7} due to its low-power characteristic. This causes the ultra slow discharging speed of V_{FB1}. As a result, when V_{REG} is powered off or becomes very small, V_{REF} is

discharged, but V_{FB1} may retain at a relative high voltage. Then, when tag IC is powered on again, the POR pulse signal cannot be generated again since V_{FB1} is always larger than V_{REF}. To avoid this condition, a power-off auto-discharging path formed by M_{DIS} and R_{DIS} is added. V_{FB1} will be discharged through this path when V_{REF} is decreased to be less than its start-up threshold (i.e. when V_{DIS} is high). The simulated waveforms without and with the proposed power-off auto-discharging path for the power-on and power-off responses are shown in Fig. 2.16(1) and (2), respectively. It proves that the malfunction due to fast turn-on and turn-off can be avoided due to the proposed auto-discharging path.



(1)



(2)

Fig. 2.16 Simulation results of power-on and power-off responses

(1) without and (2) with the proposed power-off auto-discharging path

Leakage current in the 90-nm technology

In order to save chip area, MOS capacitors are often preferred to replace metal-metal (MIM) capacitors. In UMC 90-nm CMOS technology, the unit capacitance of a standard NMOS capacitor (NCAP_10) is about 15 fF/μm^2, which is about 10 times of that of a MIM capacitor. However, the gate leakage of nano-scale devices cannot be ignored especially when they are used in ultra-low-power circuits such as the passive RFID tag. In order to evaluate whether the gate leakage is an important issue for this design, a test circuit with setup shown in Fig. 2.17 is used to simulate the gate leakage current. The simulation results are shown in Fig. 2.18. It can be found that the leakage current is proportional to the gate area of the MOS capacitor. When the terminal voltage V_{DC} is 1 V, the gate leakage current of a 1-pF NCAP_10 capacitor is about 1 μA, which is even larger than the quiescent current of the POR circuit. This situation will cause the POR circuit malfunction.

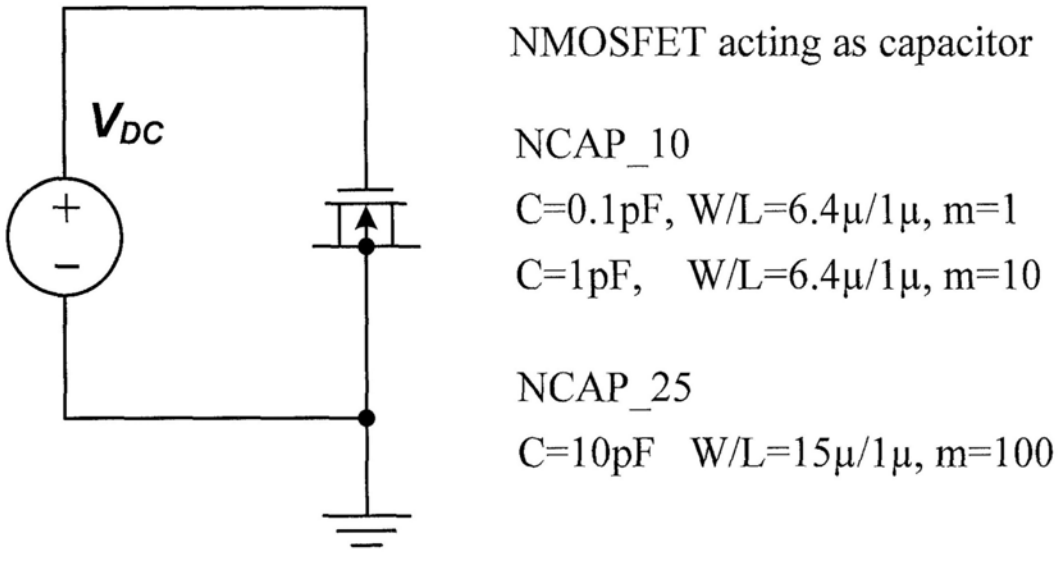


Fig. 2.17 Test setup for the gate leakage simulation

One method to delink the tradeoffs between the area and the total capacitance is to use MOS transistors with thicker oxide to decrease leakage. In this paper, the 2.5-V NMOS transistor is used to act as a capacitor (NCAP_25) to save area. It can avoid wrong operation of the POR circuit due to gate leakage. The unit capacitance of NCAP_25 is about 6 fF/μm^2, which is about four times of that of a MIM capacitor. The gate leakage performance of NCAP_25 is also shown in Fig. 2.18. From the result, it shows that even though it is a 10-pF capacitor, the gate leakage is still small and can be neglected. This small leakage current has been confirmed by the measurements

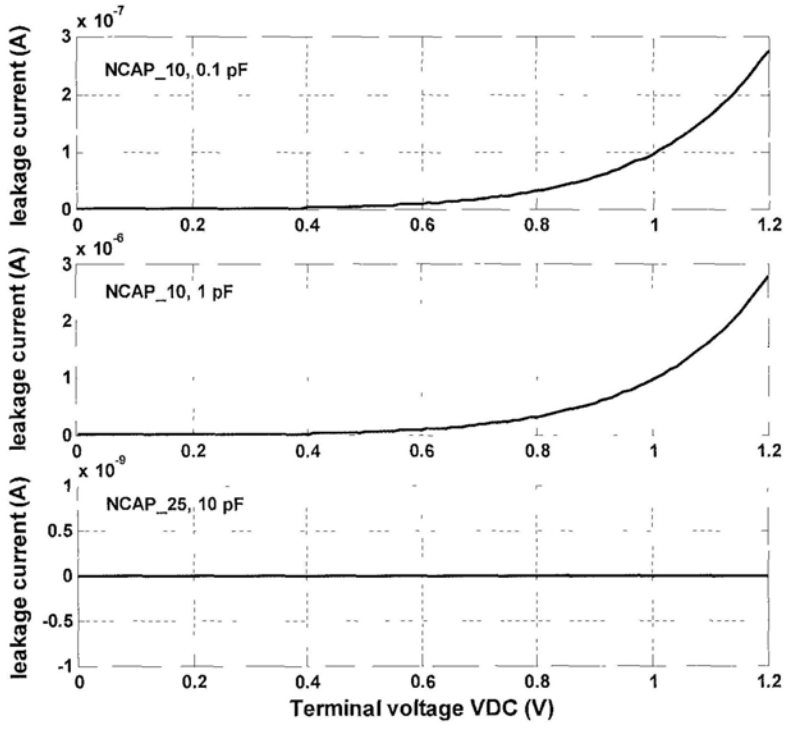


Fig. 2.18 Simulation results of gate leakage current

2.4.2 Experimental Results of 90-nm POR circuit

The proposed POR circuit is implemented in UMC 90-nm CMOS technology. The chip micrograph of the proposed POR and the reference circuit, which is a part of a

fully-integrated passive RFID tag IC, is shown in Fig. 2 19. The POR circuit occupies an area of 0.08835 mm^2. A digital buffer, also shown in Fig. 2.19, is integrated in the chip for testing purpose.

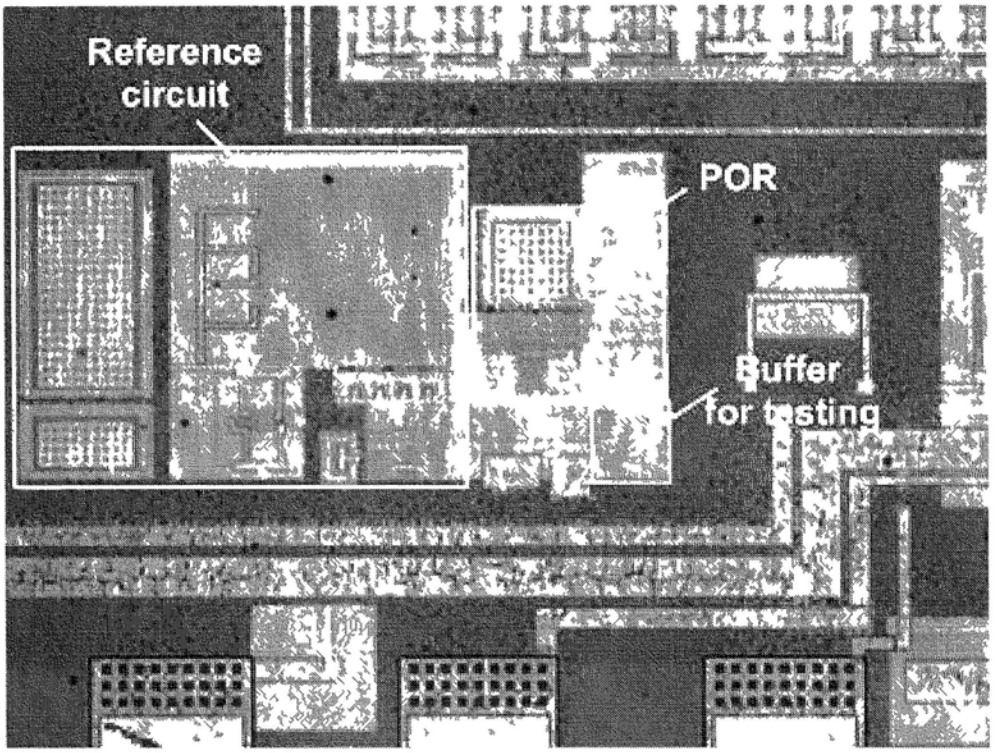


Fig. 2.19 Chip micrograph

The measurement results of the whole tag operation are shown in Fig. 2.20. The LDO can provide a stable output even V_M has large variations in the backscattering stage. The demodulated signal can be processed properly by the baseband processor, and then it sends data back to the reader through backscattering. The results indicate that the tag IC, including POR circuit, functions properly. The measured power-on and power-off responses of the proposed POR is shown in Fig. 2.21. It is consistent with the simulation results previously shown in Fig. 2.16. The POR pulse signal can be generated each time after power on. The effectiveness of the proposed POR circuit is verified.

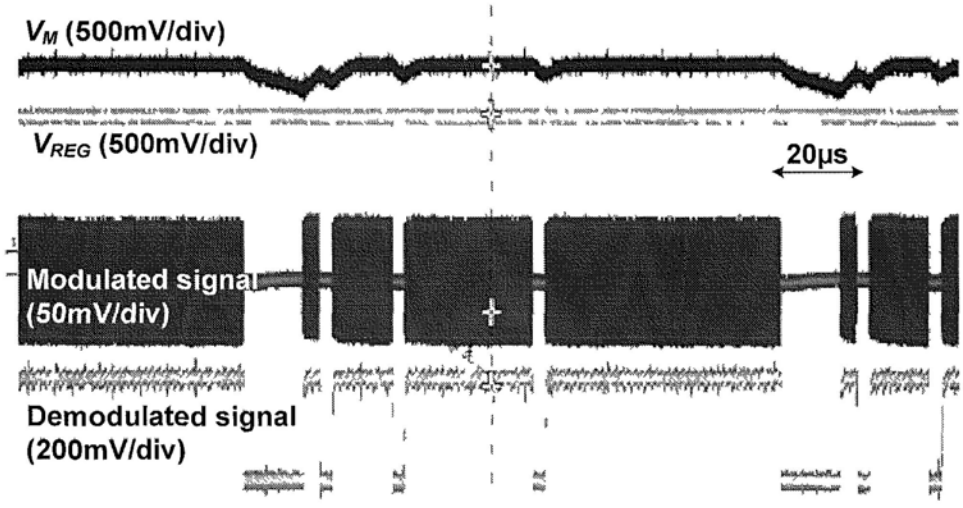


Fig. 2.20 Measurement results of the whole-tag operation

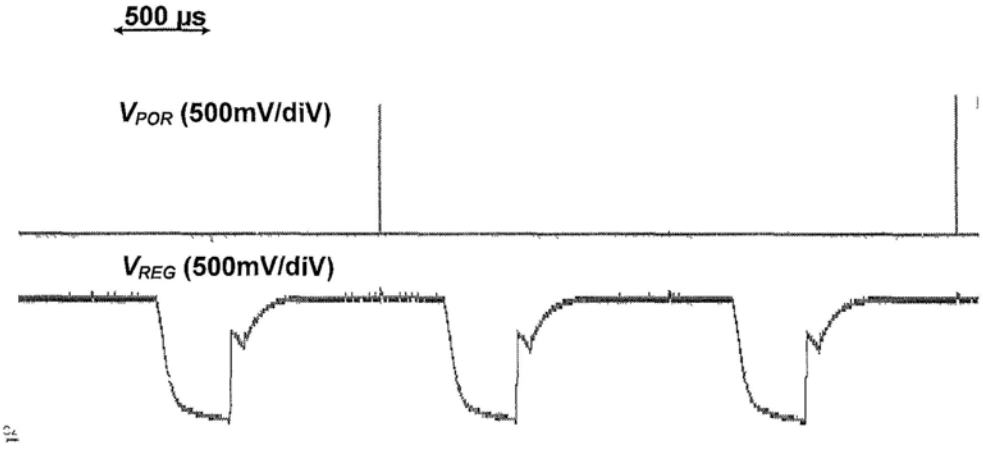


Fig. 2.21 Measured power-on and power-off responses of the POR circuit with the proposed power-off auto-discharging path

2.5 Summary

A low-power voltage regulator for passive UHF RFID tag IC has been presented in this chapter. A 9-ppm/°C voltage reference working under a sub-1-V supply voltage and

a 150-ns-pulse POR circuit are included in this regulator. The measurement results of the proposed regulator implemented in a 0.18-μm CMOS technology verify the design and prove that this 700-nA regulator is very suitable for passive tag ICs. This regulator structure can achieve 1-V operation by changing the feedback factor based on the power supply requirements of the signal front-end and the digital processing part. Moreover, it can be easily implemented in other advanced technologies and the supply voltage can be further decreased. Besides that, a POR circuit fabricated in 90-nm CMOS technology is also presented to improve the reliability.

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CHAPTER 3. Design of Fully-Integrated Energy-Efficient CMOS LDO with Fast Transient Response[♣]

LDOs are commonly used to provide power to low-voltage digital circuits [1]. In these applications, it is common for the digital circuit to have several different modes of operation. Similarly, the analog parts or whole SoC powered by LDO may work in different modes too, such as standby and active modes [2]–[4].When the load current changes quickly due to the mode switch, the LDO output has a temporary glitch. This glitch should not affect the normal operation of the load circuits. It indicates that most two important factors to evaluate the load transient response are recovery time and voltage spike amplitude of LDO output.

This chapter is organized as follow. The basic analysis on LDO load transient response is first introduced in Section 3.1. A low-power fast-transient LDO based on capacitor coupling and fabricated in 90-nm CMOS technology is proposed in Section 3.2, where the theory analysis, circuit implementation and experimental/simulation results are given. Finally, the conclusions and discussions are given at the end of this chapter.

[♣] The material presented in this chapter has been published in IEEE Journal of Solid-State Circuits in Sep. 2010 with the title of "A 6-μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology".

3.1 Load transient response of LDO: a basic review

The typical load transient response of LDO is shown in Fig. 3.1 [5]. The maximum output voltage spike $\Delta V_{tr\text{-}max}$ is approximately by

$$\Delta V_{tr-\max} \approx \frac{I_{OUT-\max}}{C_{OUT}} \Delta t_1 + \Delta V_{esr} \quad , \tag{3.1}$$

where $I_{OUT\text{-}\max}$ is the maximum load current, C_{OUT} is the output capacitance, and ΔV_{esr} is the voltage variation resulting from the equivalent series resistance (ESR) of output capacitor ($\Delta V_{esr} \propto R_{esr}$). The response time can be approximated to be

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{pg} \frac{\Delta V}{I_{sr}} \quad , \tag{3.2}$$

where BW_{cl} is the close-loop bandwidth of the system, t_{sr} is the slew-rate time associate with C_{pg}, the parasitic gate capacitance of power transistor, ΔV is the voltage difference at the gate of power transistor between different load conditions, and I_{sr} is the slew-rate limited current.

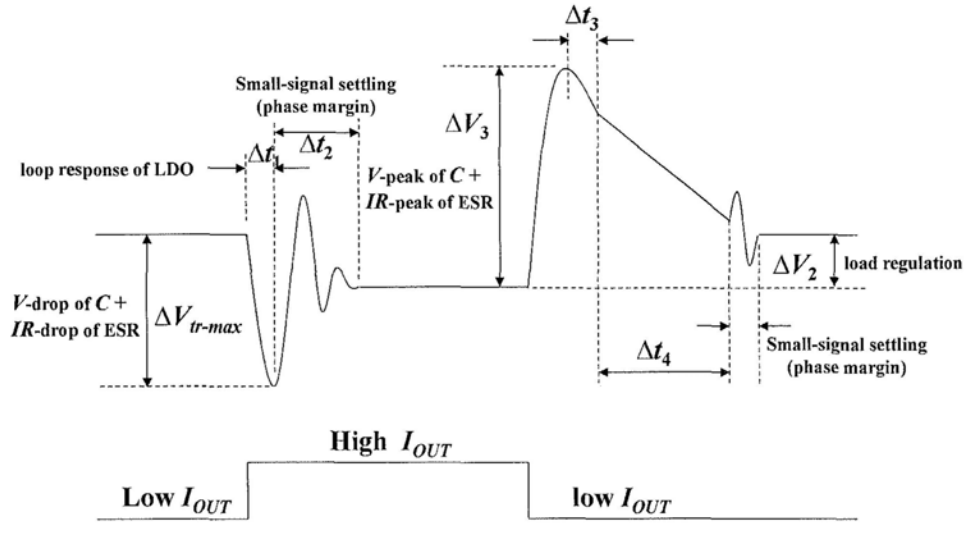


Fig. 3.1 Typical load transient response of LDO

Equations (3.1) and (3.2) indicate that to achieve small voltage spike and response,

(1) large C_{OUT} is preferred, which means high cost and bulk PCB area;

(2) small ESR is preferred, which means ESR compensation is not a good selection to make the LDO stable;

(3) High BW_{cl} is preferred, which means high power consumption is needed and it is a tradeoff with the LDO stability;

(4) Small C_{pg} is preferred, which is a tradeoff with the dropout voltage. It is also indicated that the load transient performance in advanced technology, such as nano-scale CMOS technology, can be better;

(5) Higher I_{sr} is preferred, which means more quiescent current, and thus more static power is consumed by LDO itself. Thus the total efficiency, especially in standby mode, is decreased.

As analyzed in [6], there are many methods to increase the transient response of LDO, which are shown in Fig. 3.2 again. High I_q is used to achieve high BW_{cl} and increase the slew rate in Fig. 3.2(a). However, the static power consumption of LDO itself is increased and the total power efficiency is degraded, especially in the standby mode where the load current is very small. Adaptive biasing is used to improved load transient response through sensing the output current [5], [7], [8]. However, it is only effect when output current changes from low to high, and it is not helpful to improve line transient response. The dynamic-biasing method [6], [9], [10] shown in Fig. 3.2(c), is the most energy-efficient way to improve the load transient response, which is very

important for low-power applications especially in wireless powered systems.

Based on the above analysis, smaller ESR and larger charging/discharging current for the gate of power transistor are needed to improve the transient response of LDO. In the next section of this chapter, a low-power LDO with capacitor-coupling techniques are reported to improve the load transient response by providing dynamic biasing current.

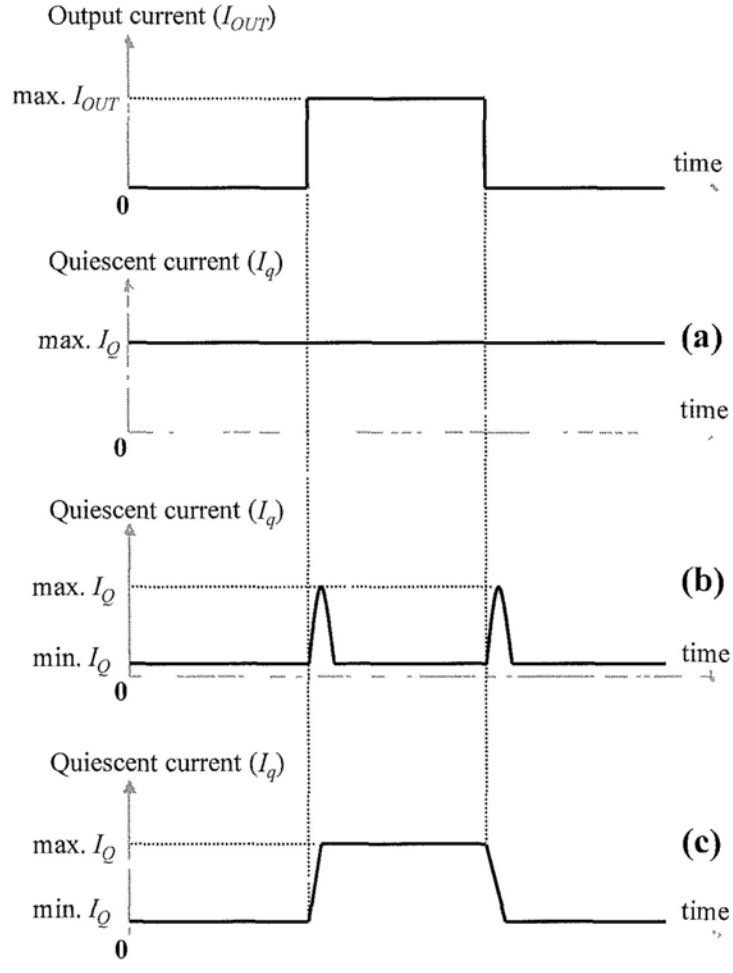


Fig. 3.2 Different methods to improve load transient response

3.2 A 6-μW chip-area-efficient output-capacitorless LDO with direct output voltage detection in 90-nm CMOS technology

In this section, an output-capacitorless LDO (OCL-LDO) compensated by a single Miller capacitor is implemented in a commercial 90-nm CMOS technology [11]. The proposed LDO makes use of the small transistors realized in nano-scale technology to achieve high stability, fast transient performance and small voltage spikes under rapid load-current changes without the need of an off-chip capacitor connected at the LDO output. Experimental result verifies that the proposed LDO is stable for a capacitive load from 0 to 50 pF (estimated equivalent parasitic capacitance from load circuits) and with load capability of 100 mA. Moreover, the gain-enhanced structure provides sufficient loop gain to improve line regulation to 3.78 mV/V and load regulation to 0.1 mV/mA, respectively. The embedded voltage-spike detection circuit enables pseudo Class-AB operation to drive the embedded power transistor promptly. The measured power consumption is only 6 μW under a 0.75-V supply. The maximum overshoot and undershoot under a 1.2-V supply are less than 66 mV for full load current changes within 100-ns edge time, and the recovery time is less than 5 μs.

3.2.1 Introduction

Recent development of OCL-LDO realizes on-chip, local voltage regulation [12] to enable more effective integrated power management for SoC. Parasitic effects such as bond-wire inductance and resistance due to the external connections with passive

components existing in the classical non-OCL-LDO can all be eliminated. In addition, the chip area occupied by the I/O pads for connecting with external passive components is no longer required so that the function-to-area ratio of the SoC with integrated power management can be significantly improved. Due to these reasons, many OCL-LDOs were proposed [13]–[20]. In the prior works, loop stability and load-transient response of the OCL-LDOs are regarded as important design issues. Frequency-compensation approaches for enhancing the loop bandwidth, as well as the closed-loop stability, and dynamic-biasing methods for solving the serious slew-rate limit problem at the gate of the integrated power transistor are two key aspects currently under extensive investigation.

With forecasting that more SoC will be implemented by ultra-small-scale technologies in the next decade, the impacts, either positive or negative, of the nano-scale technology on the OCL-LDO design cannot be overlooked anymore. Unfortunately, most of the foregoing OCL-LDO designs are not implemented in nano-scale technologies, except one fully-integrated 50-mA LDO design implemented in 90-nm CMOS technology reported in 2005 [14]. This design consumes a quiescent current (I_q) of 6 mA and is stabilized by a 0.6-nF on-chip capacitor. The load regulation under voltage positioning is 90 mV/50 mA. The performance of this LDO design reveals that the design challenges of OCL-LDO in nano-scale technology are (1) enhancement of loop gain for better load regulation, (2) optimization of quiescent current for power saving, and (3) minimization of on-chip capacitance for chip-area reduction.

The recently reported OCL-LDO structures are based on a LDO reported in [14], as shown in Fig. 3.3. The core is a flipped voltage follower (FVF) [21]. The stability of this LDO structure has been proven stable under the absence of an off-chip capacitor. However, the large-signal response under the low-I_q condition limits the transient response, and thus dynamic biasing was proposed in [6] and [9]. When the LDO is implemented in nano-scale technology, both the small-signal and large-signal responses are expected to be significantly improved due to the much smaller parasitic capacitance associated with nano-devices. However, the FVF-based LDO structure itself does not have a high loop gain due to its simple folded circuit structure, even though it is implemented in a sub-micron CMOS technology. As a result, the reported load regulation is not outstanding. It can be easily predicted that when the FVF-based LDO is implemented in nano-scale technology, the load regulation should be worse due to the more serious channel-length modulation in the nano-devices.

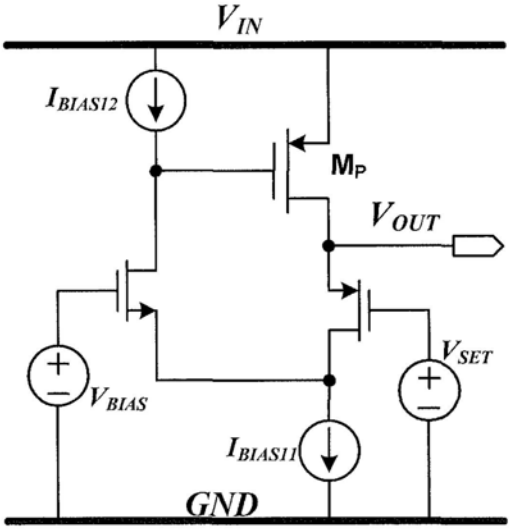


Fig. 3.3 Prior work: LDO structure based on FVF

With regard to the above issues, a 90-nm CMOS OCL-LDO, based on FVF and

compensated by a single Miller capacitor, is proposed in this paper. The proposed LDO makes use of the small transistors realized in nano-scale technology to achieve high stability, fast transient performance and small voltage spikes without the need of an off-chip capacitor connected at the LDO output. In Section 3.2.2, the proposed OCL-LDO structure, implementation and principle of operation will be presented. Detailed measurement results will be reported in Section 3.2.3. A comparison of the proposed design with the reported OCL-LDOs will be given in Section 3.2.4. Finally, the conclusion of this paper is given.

3.2.2 Proposed LDO Structure and Circuit Implementation

In this section, the structure and circuit implementation of proposed OCL-LDO will be presented. Performance improvement on regulation, stability and transient response will be addressed.

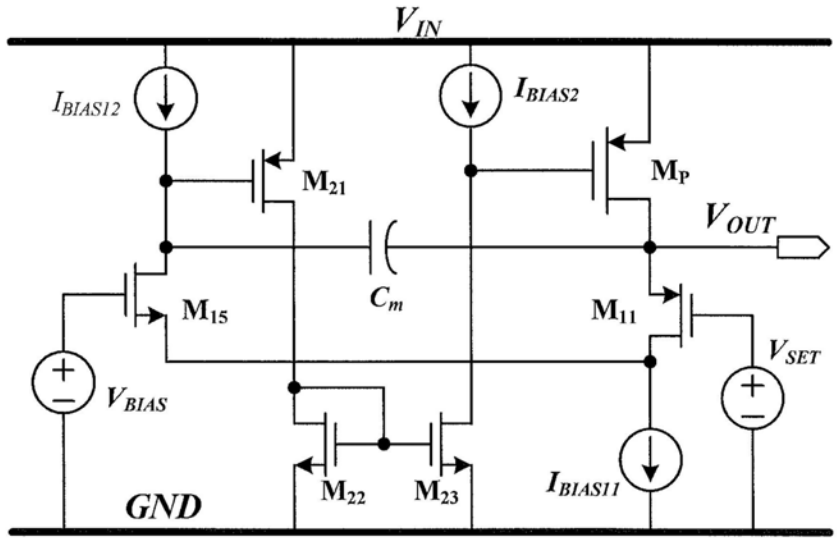


Fig. 3.4 Proposed OCL-LDO structure (core part, without slew-rate enhancement)

A. Proposed LDO structure with regulation improvement

The proposed OCL-LDO structure is shown in Fig. 3.4, which originates from the FVF-based LDO structure. M_P is the power PMOS transistor. The input voltage and output voltage are V_{IN} and V_{OUT}, respectively, whereas V_{SET} is a control voltage generated by a voltage reference circuit and a V_{SG}-shifting circuit, which have been previously presented in [6]. Comparing with the structure shown in Fig. 3.3, an additional non-inverting gain stage, formed by M_{21}, M_{22}, M_{23} and I_{BIAS2}, could boost the loop gain to improve both line and load regulations. Another important advantage of the added gain stage is that the dynamic range of the gate voltage of M_P in the proposed structure is also extended, which is just one saturation voltage of M_{23} above the ground. This enables a larger achievable V_{SG} of M_P, so that the W/L aspect ratio of M_P can be smaller under the condition that the metal routing of M_P is sufficiently wide or thick to sustain the maximum output current with sufficiently low IR drop. A compensation capacitor, C_m, is inserted between V_{OUT} and the drain of M_{15} to stabilize the LDO. Detailed analysis of the loop stability will be given later in Part B of this section.

Circuit simulation is conducted to compare the load regulation of the LDO structures shown in Figure 3.3 (denoted as LDO_1) and Figure 3.4 (denoted as LDO_2). Both LDOs are simulated using the BSIM3v3 models provided by the foundry of UMC 90-nm CMOS technology. The sizes of M_P used in both LDOs are 1500 μm / 0.08 μm[†]. The test conditions are V_{IN} = 0.75 V and I_{OUT} = 1 to 100 mA, where I_{OUT} is the load current. The results are consolidated and shown in Fig. 3.5. Obviously, the proposed OCL-LDO has better load regulation due to enhanced loop gain.

[†] The drawn channel length is 80 nm which is the adjustment defined by the foundry and stated in the design rules

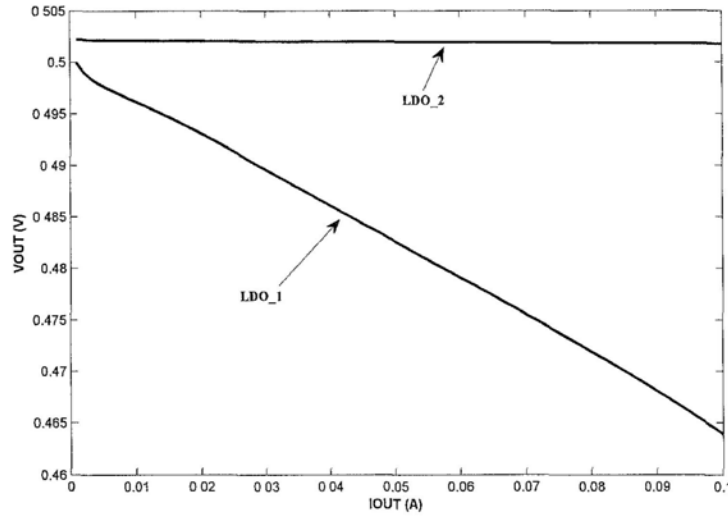


Fig. 3.5 Simulated load regulations of the LDOs shown in Fig. 3.3 (LDO_1) and Fig. 3.4 (LDO_2) designed in CMOS 90-nm technology and operated at $V_{IN} = 0.75$ V

B. Frequency compensation strategy

The proposed LDO shown in Fig. 3.4 is suspected of closed-loop stability if no compensation strategy is applied, since there is no low-frequency dominant pole due to the small parasitic capacitance and drain resistance in the 90-nm technology. The poles at the output of the LDO, the gate of M_P and the input of the non-inverting gain stage are all not at very low frequency. To solve this problem, pole-splitting technique is adopted. A compensation capacitor, C_m, is inserted between V_{OUT} and the input of the added gain stage. Since the parasitic gate-to-drain capacitance of M_P (C_{gd}) is very small in the 90-nm technology and the gain of M_P under different load current conditions is not large, the Miller effect of C_{gd} of M_P is negligible. Thus, the compensation topology, in fact, is not nested Miller compensation (NMC) [22]. The structure is similar to single Miller compensation reported in [23]. Fig. 3.6 shows the small-signal modeling of the proposed LDO, where R_{Oi} and C_{Pi} are the equivalent output resistance and lumped

output parasitic capacitance of the i-th gain stage, respectively. R_{OUT} is the output resistance including the loading resistance, and C_{OUT} is the sum of the parasitic capacitance from the LDO itself, power lines and load circuits. With the assumption of $g_{mp} >> g_{m1}$, $C_m >> C_{p1}$, and $C_{p2}R_{o2} >> C_{OUT}R_{OUT}$ (C_{p2} is about 1.3 pF and R_{o2} is about 300 kΩ, their product is much larger than $C_{OUT}R_{OUT}$ since C_{OUT} is up to 50 pF and R_{OUT} is less than 500 Ω) which are all valid in this OCL-LDO design, the transfer function of the LDO modelling shown in Fig. 3.6 is given by

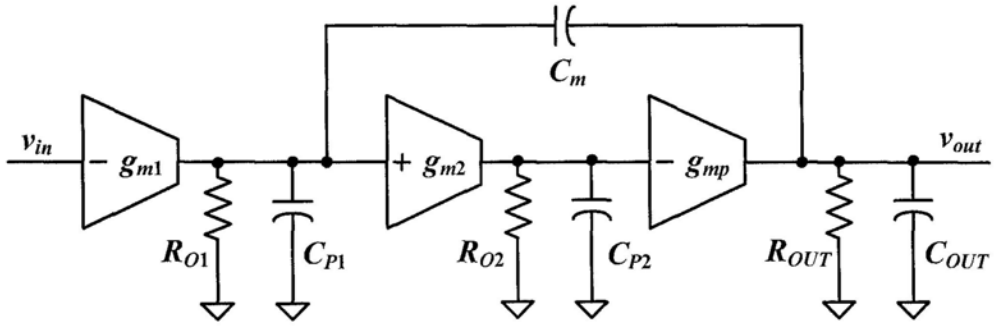


Fig. 3.6 Small-signal modelling of the proposed LDO

$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)}$$
$$\approx \frac{A_{dc}\left(1 - s\frac{C_m}{g_{m2}R_{o2}g_{mp}} - s^2\frac{C_mC_{p2}}{g_{m2}g_{mp}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_{p2}}{g_{m2}g_{mp}R_{OUT}} + s^2\frac{C_{p2}C_{OUT}}{g_{m2}g_{mp}}\right)}$$
$$\approx \frac{\left(1 - s\frac{C_m}{g_{m2}R_{o2}g_{mp}} - s^2\frac{C_mC_{p2}}{g_{m2}g_{mp}}\right)}{\frac{s}{GBW}\left(1 + s\frac{C_{p2}}{g_{m2}g_{mp}R_{OUT}} + s^2\frac{C_{p2}C_{OUT}}{g_{m2}g_{mp}}\right)} \quad (3.3)$$

where $A_{dc} = g_{m1}g_{m2}g_{mp}R_{o1}R_{o2}R_{OUT}$ is the low-frequency open-loop gain, $p_{-3dB} = 1/(C_mR_{o1}g_{m2}g_{mp}R_{o2}R_{OUT})$ is the dominant pole, and $GBW = A_{dc} \cdot p_{-3dB} = g_{m1}/C_m$ is the gain-bandwidth product of the loop gain. There are two non-dominant poles and two

zeros. It is highlighted here that C_m does control the GBW of the loop gain but it does not affect the location of the non-dominant poles. When the chosen C_m is small and g_{mp} is large, the zeros are located at high frequencies and are negligible. Thus, (3.3) can be simplified to

$$A_v(s) = \frac{v_{in}(s)}{v_{out}(s)} \approx \frac{A_{dc}}{(1+\frac{s}{p_{-3dB}})(1+s\frac{C_{p2}}{g_{m2}g_{mp}R_{OUT}}+s^2\frac{C_{p2}C_{OUT}}{g_{m2}g_{mp}})} \tag{3.4}$$

To avoid frequency peaking due to complex poles, the relationship shown below should be met.

$$C_{OUT} \le \frac{C_{p2}}{4g_{m2}g_{mp}R_{OUT}^2} \tag{3.5}$$

With an approximation of $R_{OUT} \approx 1/(\lambda I_{OUT})$, (3.5) can be rewritten to

$$C_{OUT} \le \frac{\lambda^2 I_{OUT}^2 C_{p2}}{4g_{m2}\sqrt{2\mu_p C_{OX}(W/L)_{M_p} I_{OUT}[1+\lambda(V_{IN}-V_{OUT})]}} \tag{3.6}$$

Based on the above condition, (3.4) can be further simplified to

$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{A_{dc}}{(1+\frac{s}{p_{-3dB}})(1+\frac{s}{p_2})(1+\frac{s}{p_3})} \tag{3.7}$$

where

$$p_2 = \frac{1}{2C_{OUT}R_{OUT}} - \sqrt{\frac{1}{4C_{OUT}^2R_{OUT}^2} - \frac{g_{m2}g_{mp}}{C_{p2}C_{OUT}}} \tag{3.8}$$

$$p_3 = \frac{1}{2C_{OUT}R_{OUT}} + \sqrt{\frac{1}{4C_{OUT}^2R_{OUT}^2} - \frac{g_{m2}g_{mp}}{C_{p2}C_{OUT}}} \tag{3.9}$$

To make the LDO stable, p_2 and p_3 should satisfy the condition: $GBW \le (1/2)p_2 \le (1/4)p_3$ [24]. In this design, a condition of $p_2 \ge 10GBW$ is set to maintain high stability. The relationship between C_{OUT}, V_{IN} and I_{OUT} can be found from (3.6). It indicates that a

smaller C_{OUT} is needed for a smaller I_{OUT} or a higher V_{IN}. Thus, the condition stated in (3.6) actually specifies the maximal restriction of C_{OUT} to maintain stability. Since a larger I_{OUT} is needed for a larger C_{OUT} or V_{IN}, the minimum requirement of I_{OUT} can be found from (3.6) and is given by

$$I_{OUT} \geq \sqrt[3]{\frac{32 g_{m2}^2 C_{OUT}^2 \mu_p C_{OX} (W/L)_{M_p} [1+\lambda(V_{IN}-V_{OUT})]}{\lambda^4 C_{p2}^2}} \tag{3.10}$$

Similar to the LDOs compensated by NMC or some advanced compensation methods [13], [16], [17], (3.10) reveals that there is a minimum load current requirement to maintain the overall stability of the proposed LDO design. However, since the leakage current of 90-nm CMOS technology is significant and is up to several milliamperes in some designs [14], the proposed LDO is always stable in these applications. The reduction of the minimum load current requirement is not performed in this design although some methods reported in [16], [17], and [19] can lessen this problem.

The simulated loop gains of the proposed LDO at different V_{IN} and I_{OUT} are shown in Fig. 3.7. The highest low-frequency loop gain is 75 dB, whereas the lowest value is 50 dB when V_{IN} is 0.75 V and I_{OUT} is 100 mA (the power transistor operates in linear region when V_{IN} is 0.75 V and I_{OUT} is 100 mA, operation regions of power transistor under different V_{IN} and I_{OUT} are summarized in Table 3.1). The phase margins in all conditions are more than 80°. Both the sufficient loop gain and large phase margin show that the proposed LDO has good voltage regulation and high closed-loop stability.

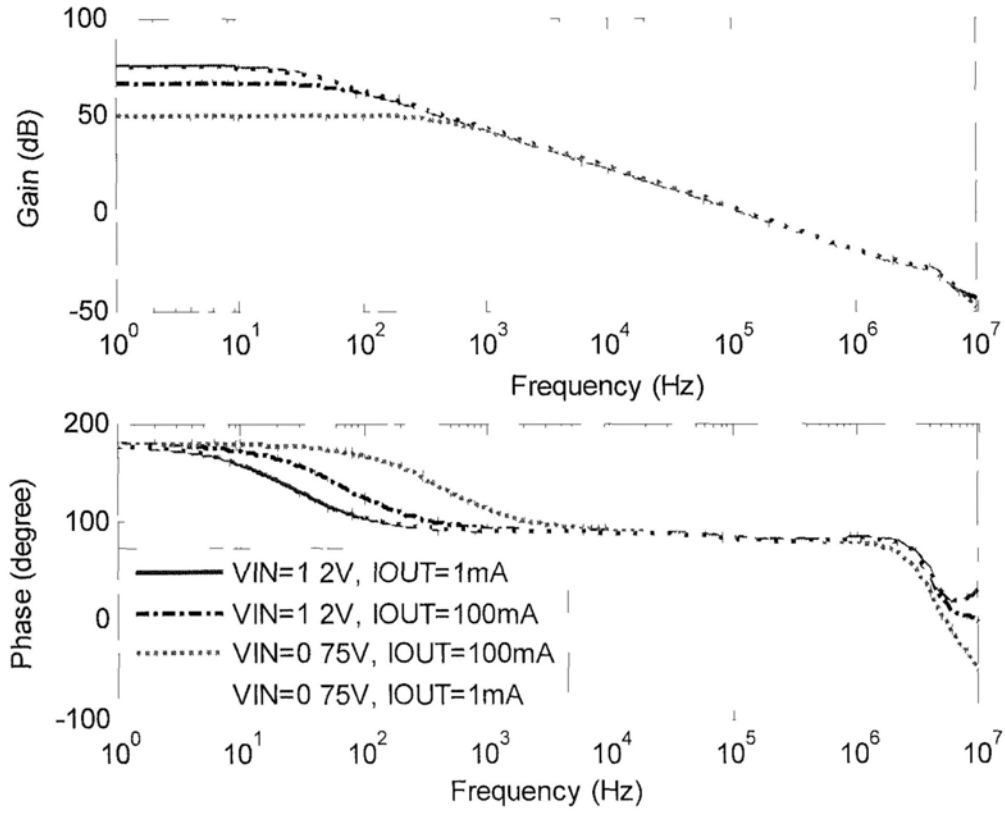


Fig. 3.7 Simulated bode plots of proposed LDO with different V_{IN} and V_{OUT} (C_{OUT} = 10 pF).

Table 3.1 Operation regions of power transistor under different V_{IN} and I_{OUT}

V_{IN} (V)	I_{OUT} =1 mA	I_{OUT} =10 mA	I_{OUT} =50 mA	I_{OUT} =100 mA
0.75	Sub-threshold	Saturation	Saturation	Linear
1.2	Sub-threshold	Saturation	Saturation	Saturation

C. *Circuit implementation with slew-rate enhancement*

The error amplifier in Fig. 3.4, formed by M_{11}, M_{15}, I_{BIAS11}, I_{BIAS12}, M_{21}, M_{22}, M_{23} and I_{BIAS2}, features a Class-A output stage to drive the gate capacitance of M_P (C_g, which is equivalent to C_{p2} in Fig. 3.6). The charging current of C_g is defined by I_{BIAS2}, whereas

the discharging current of C_g is from M_{23}. When V_{OUT} drops due to rapid increase of the load current, the source terminal of M_{11} senses the changes and then propagates to the gate of M_{21} via M_{15}. The voltage change at the gate of M_{21} is between $\{V_{IN} - \min[V_{(I\_BIAS12)}]\}$ and $(V_{BIAS} - V_{GS15} + V_{DS15(sat)})$, where $\min[V_{(I\_BIAS12)}]$ is the minimum operational voltage of I_{BIAS12}. As a result, the discharging current from M_{23} is not small and this enhances the discharge of C_g. However, when an overshoot of V_{OUT} happens, the static charging current provided by I_{BIAS2} is not sufficiently large to charge C_g in the low quiescent-current LDO design. In that case, a direct voltage-spike detection technique is adopted to suppress this large overshoot. The detailed operation will be introduced using the full schematic of the proposed LDO.

The complete schematic of the proposed LDO is shown in Fig. 3.8. The error amplifier is formed by a common-gate differential pair consisting of M_{11}–M_{16} and a non-inverting gain stage consisting of M_{21}–M_{24}, whereas the function of the non-inverting gain stage is to enhance the loop gain and increase the signal swing at the gate of M_P. The aforementioned voltage-spike detection circuit is formed by M_{B1}, M_{B2}, R_1 and C_1 [6]. C_1 is used to detect the output voltage spikes, and the detected changes of V_{OUT} activate the dynamic-biasing circuit to improve the slew rate at the gate of M_P. For example, when V_{OUT} increases suddenly, C_1 couples the effect to the gate of M_{B2} and hence the gate voltage of M_{B2} is increased to make the drain current of M_{B2} increase simultaneously. As a result, more charging current from M_{24} to C_g helps to suppress the output voltage spike. With the added output-detection high-pass network, consisting of R_1 and C_1, the error amplifier features a pseudo Class-AB output stage, which improves

the slew rate effectively and thus improves the transient performance. Comparing with the spike-detection circuit in [6], only one pair of *RC* is needed and so the chip area for another pair of *RC* component can be saved (R_1 is 500 kΩ and C_1 is 1 pF in this design).

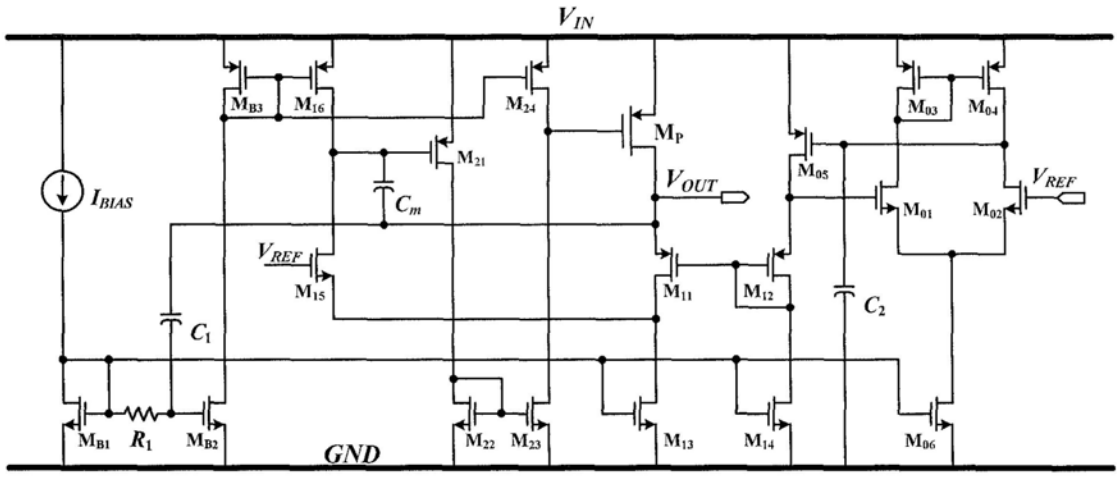


Fig. 3.8 Full schematic of the proposed LDO (with slew-rate enhancement)

The simulated load transient results of the LDO shown in Fig. 3.3 (LDO_1), the proposed LDO without voltage-spike detection circuit shown in Fig. 3.4 (LDO_2) and the proposed LDO with voltage-spike detection circuit (denoted as LDO_proposed) are given in Fig. 3.9. Under a 0.75-V supply, when the output current switches between 1 mA and 100 mA within 100-ns edge time (i.e. the rise and fall times taken for the change of I_{OUT}), the overshoots of LDO_proposed, LDO_2 and LDO_1 are 97 mV, 242 mV and 230 mV respectively. The overshoots of the last two cases are close to the supply, and they are larger at a higher supply. Moreover, the simulated undershoots of LDO_proposed, LDO_2 and LDO_1 are 54 mV, 65 mV and 359 mV respectively. The output voltage spike is much reduced due to the enhanced loop-gain structure with a pseudo Class-AB output stage of the error amplifier. In other words, the proposed LDO shown in Fig. 3.8 has much improved steady-state and transient accuracies.

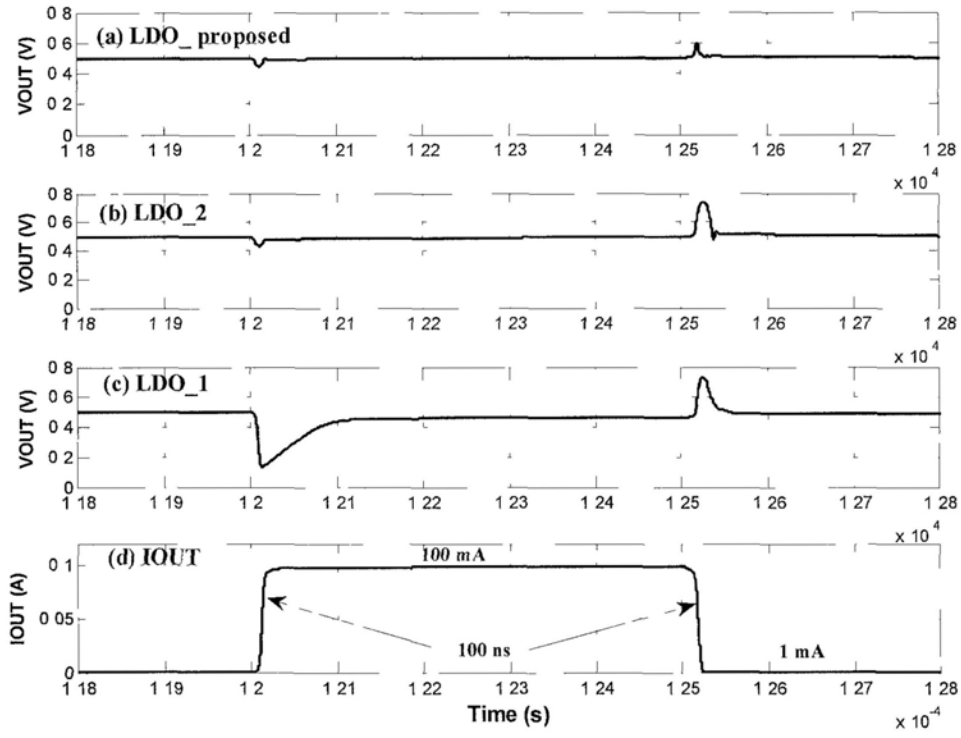


Fig. 3.9 Simulated load transient responses of different LDO topologies

(a) V_{OUT} of LDO_proposed (b) V_{OUT} of LDO_2 (c) V_{OUT} of LDO_1 (d) I_{OUT}

3.2.3 Experimental results

The proposed LDO has been realized in UMC 90-nm CMOS technology. The Chip micrograph is shown in Fig. 3.10. It occupied 0.019 mm^2 (163 μm × 117 μm) of the chip area. The input supply range is 0.75 – 1.2 V, and the dropout voltage is 200 mV at 100-mA of I_{OUT}. The quiescent current is only 8 μA. The minimum output voltage can be down to 0.5 V, which can meet the requirements of some ultra low-voltage advanced circuits [25].

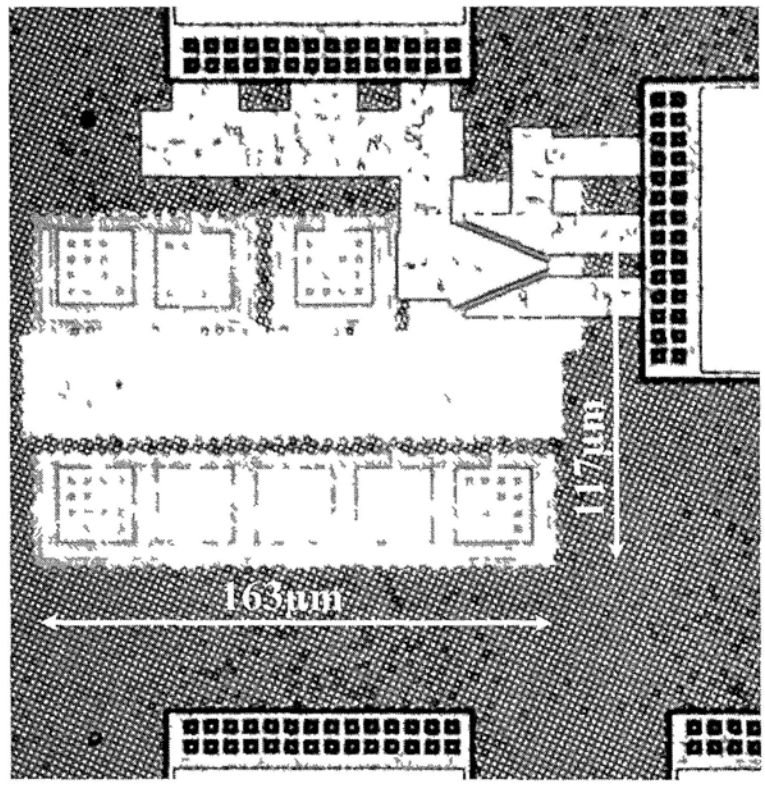
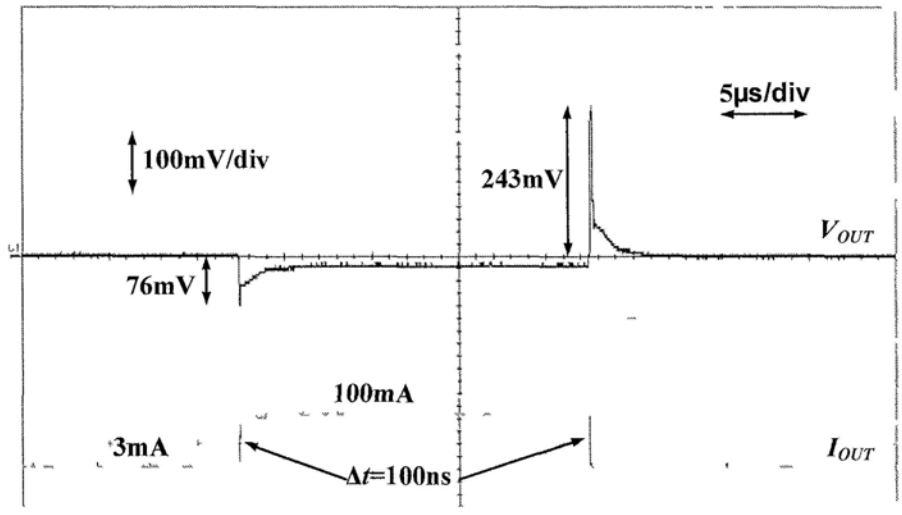


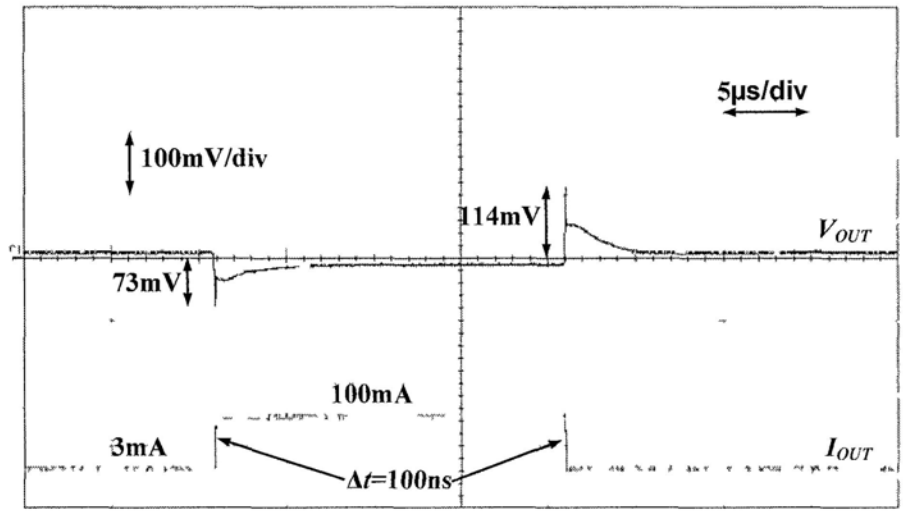
Fig 3 10 Micrograph of the proposed LDO

The proposed LDO is stable in full input supply range with equivalent capacitive load of no more than 50 pF and I_{OUT} of larger than 3 mA. Load transient measurements have been done to prove the stability and the improved transient performance of the proposed LDO structure. The measured load transient waveforms under different supply voltages and edge times are shown in Fig. 3.11 to Fig. 3.13. Both the LDOs (with and without the voltage-spike detection circuit, i.e., the slew-rate enhancement circuit) have been measured. As shown in Fig. 3.11, when the output current is switched between 3 mA and 100 mA within 100 ns, the overshoot of V_{OUT} with the slew-rate enhancement is about 114 mV, while it is about 243 mV (nearly reach the supply rail of 0.75 V) when without the slew-rate enhancement circuit. In Fig. 3.12, the measurement condition is changed to V_{IN} = 1.2 V. The overshoot for the case with slew-rate

enhancement is only 66 mV, while the overshoot for the case without slew-rate enhancement is about 413 mV. The reduction of the overshoot by the slew-rate enhancement circuit is over 6 times. As shown in Fig. 3.13, both the overshoot and undershoot are within 30 mV when the load current changes with 1-μs edge time. The voltage spikes are much smaller when the load current change is slower.

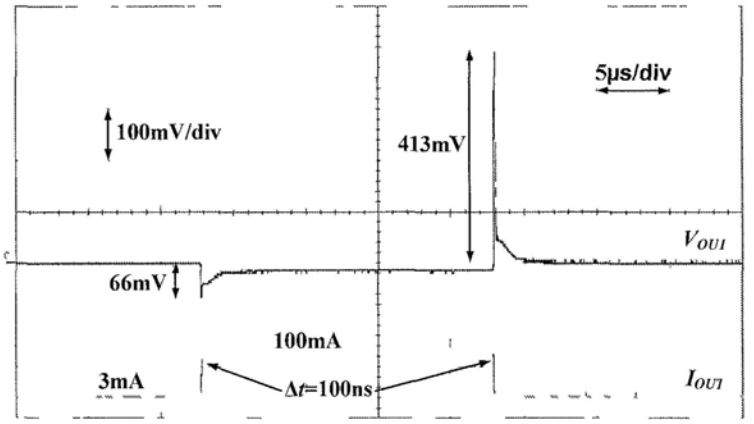


(a)

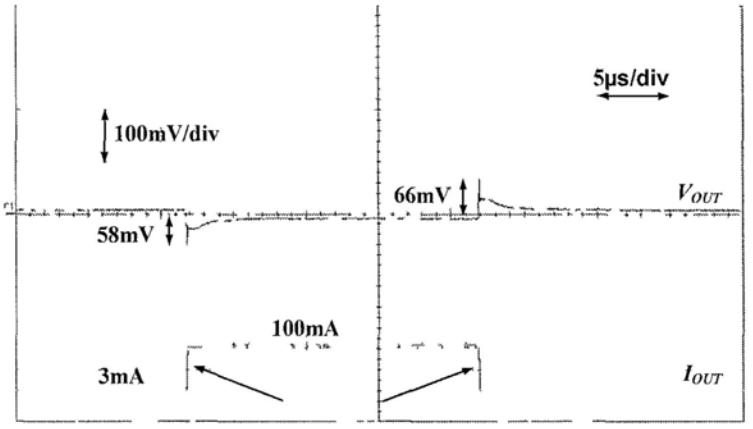


(b)

Fig. 3.11 Measured load transient response at V_{IN} = 0.75 V, V_{OUT} = 0.5 V, C_{OUT} = 50 pF and 100-ns edge time (a) without slew-rate enhancement (b) with slew-rate enhancement



(a)



(b)

Fig. 3.12 Measured load transient response at V_{IN} = 1.2 V, V_{OUT} = 0.5 V, C_{OUT} = 50 pF and 100-ns edge time (a) without slew-rate enhancement (b) with slew-rate enhancement

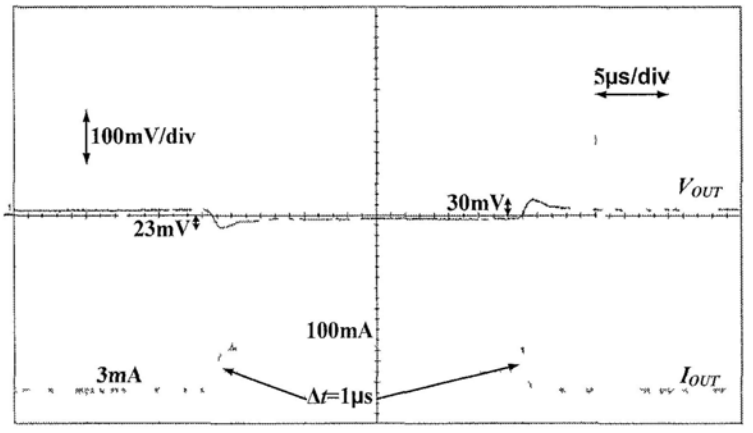


Fig. 3.13 Measured load transient response at V_{IN} = 1.2 V, V_{OUT} = 0.5 V, C_{OUT} = 50 pF and 1-μs edge time

From Section 3.2.2 and (3.10), the minimum load current requirement is a function of the input voltage and the equivalent load capacitance of the LDO. It is verified experimentally that the minimum load current can be reduced when V_{IN} and C_{OUT} are smaller. Table I summarizes the measurement results of the minimum load current requirement under different input voltages and output capacitances when V_{OUT} is set to 0.5 V. It shows the minimum load current is 1 mA for V_{IN} = 0.75 to 1.2V when C_{OUT} = 10 pF. The corresponding transient response is shown in Fig. 3.14 (top: full view; bottom: zoom-in view). This measured result verifies the foregoing analysis that the minimum load current can be smaller when C_{OUT} is smaller. When C_{OUT} is increased to 50 pF, the minimum load current is 1.5 mA with V_{IN} = 0.75 V. This transient response is shown in Fig. 3.15 (top: full view; bottom: zoom-in view). This measured result verifies that the minimum load current can be smaller when V_{IN} is smaller. Finally, when V_{IN} = 1.2 V and C_{OUT} = 50 pF, it becomes 3 mA, which have been verified in Fig. 3.12 and Fig. 3.13.

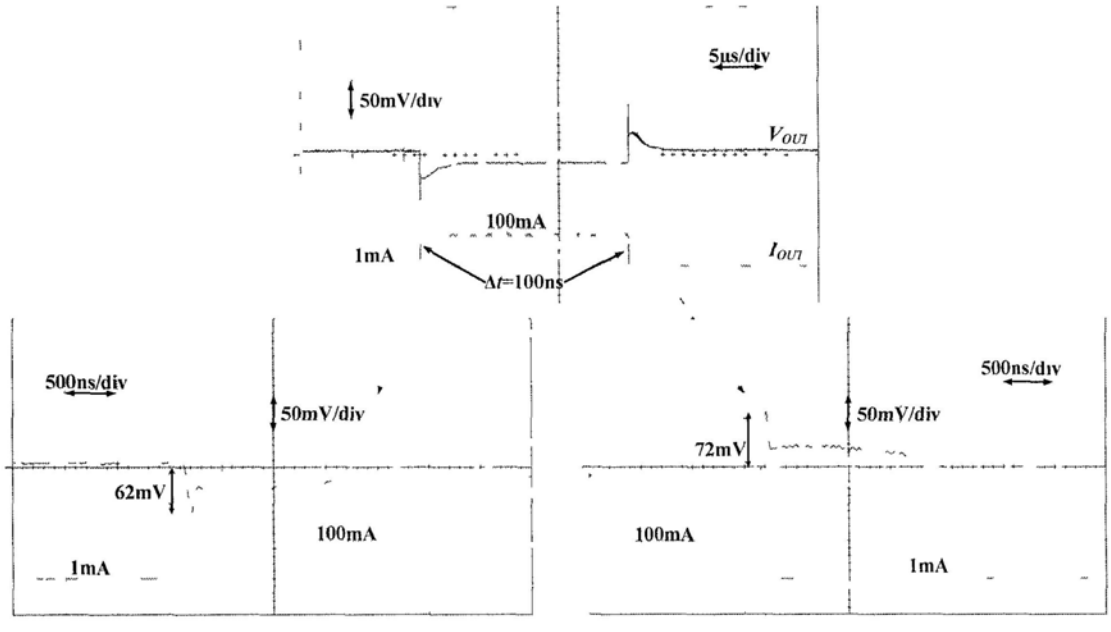


Fig. 3.14 Measured load transient response at V_{IN} = 1.2 V, V_{OUT} = 0.5 V, C_{OUT} = 10 pF and 100-ns edge time.

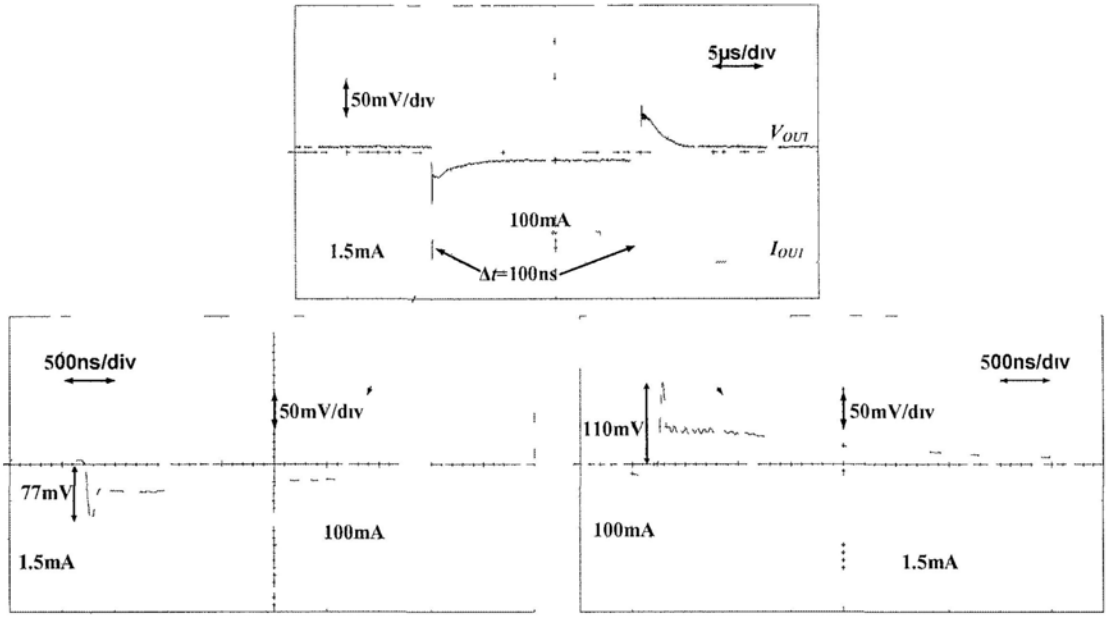


Fig. 3.15 Measured load transient response when V_{IN} = 0.75 V, V_{OUT} = 0.5 V, C_{OUT} = 50 pF and 100-ns edge time

Table 3.2 Measured minimum load current requirement under different V_{IN} and C_{OUT}

	C_{OUT} = 10 pF	C_{OUT} = 50 pF
V_{IN} = 0.75 V	I_{OUT} (min) = 1 mA	I_{OUT} (min) = 1.5 mA
V_{IN} = 1.2 V	I_{OUT} (min) = 1 mA	I_{OUT} (min) = 3 mA

Fig. 3.16 shows the line transient response. The voltage spikes are within 40 mV when supply voltage changes between 0.78 V and 1.2 V within 10 μs.

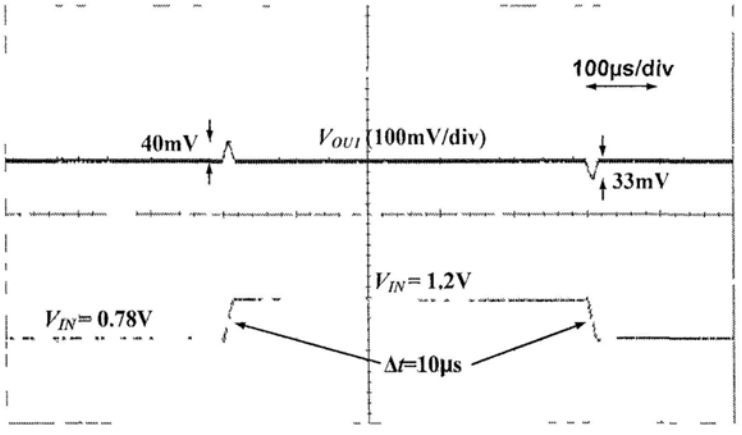


Fig. 3.16 Measured line transient waveform when V_{OUT} = 0.5V, I_{OUT} = 1 mA and C_{OUT} = 10 pF

In addition of the transient measurements, both the DC and AC measurements are also performed.

The measured line and load regulations are shown in Fig. 3.17 and Fig. 3.18, respectively. From the results, it shows that V_{OUT} varies 1.7 mV and 3 mV, respectively, when V_{IN} changes from 0.75 V to 1.2 V for I_{OUT} = 1 mA and I_{OUT} = 100 mA. When V_{IN} = 0.8 V, V_{OUT} varies about 10 mV when load current changes from 1 mA to 100 mA. Fig. 3.19 shows the relationship between the dropout voltage and the load current at V_{REF} = 1 V.

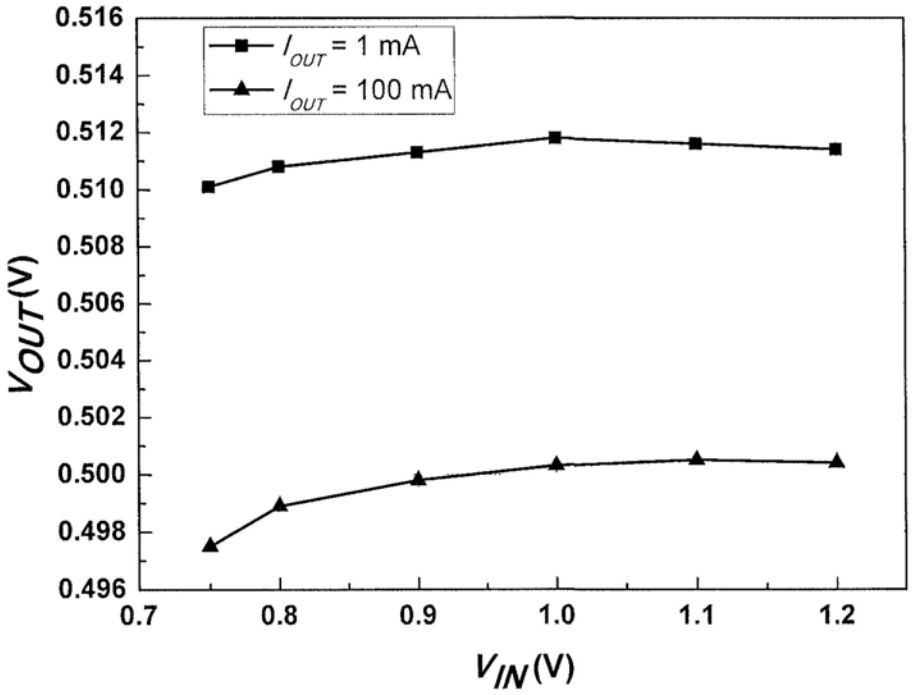


Fig. 3.17 Measured line regulation for I_{OUT} = 1 mA and I_{OUT} = 100 mA when V_{REF} = 0.5 V (no external C_{OUT} is added)

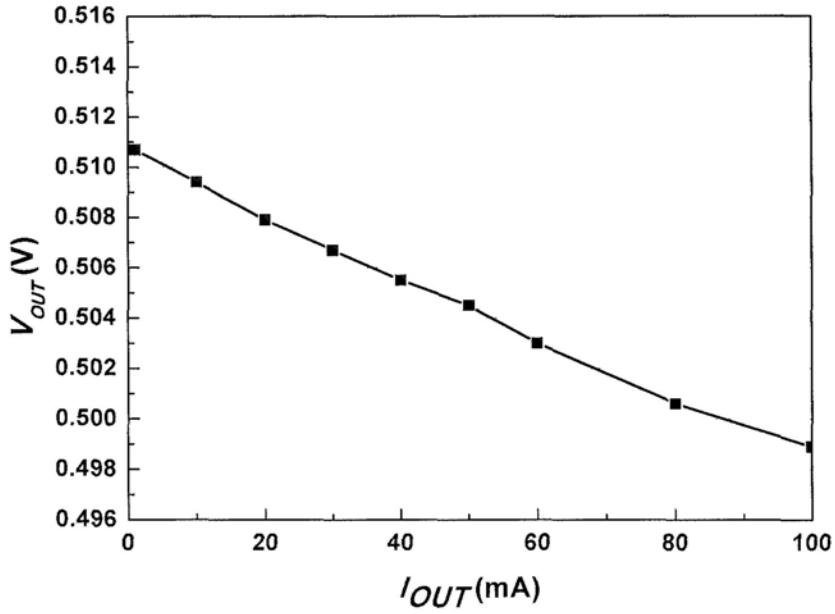


Fig. 3.18 Measured load regulation when V_{IN} = 0.8 V, V_{REF}= 0.5 V (no external C_{OUT} is added)

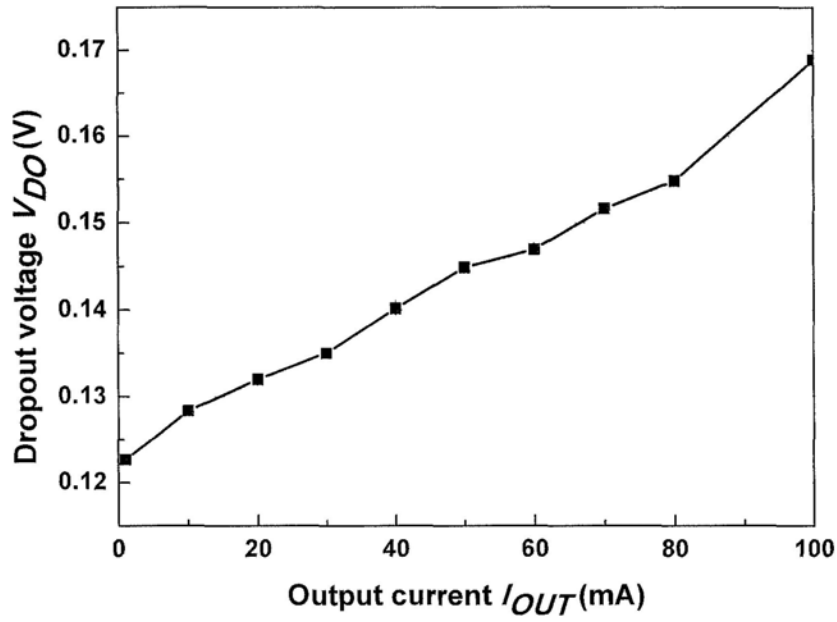


Fig. 3.19 Measured dropout voltage vs. I_{OUT} when V_{REF} = 1 V (no external C_{OUT} is added)

Finally, PSRR performance is measured. The input ripples are injected to LDO input through a voltage follower based on OPA2674 [26], which can provide 500-mA driving capability and has 250-MHz unity-gain bandwidth. The LDO input DC voltage

is 1 V and the amplitude of the input ripple is 400 mV. Both the input and output amplitudes are measured through oscilloscope. Detailed measurement setup is shown in Fig. 3.20. PSRR against different load currents is shown in Fig. 3.21. The proposed LDO can achieve about -44-dB PSRR at 1 kHz when I_{OUT} = 100 mA.

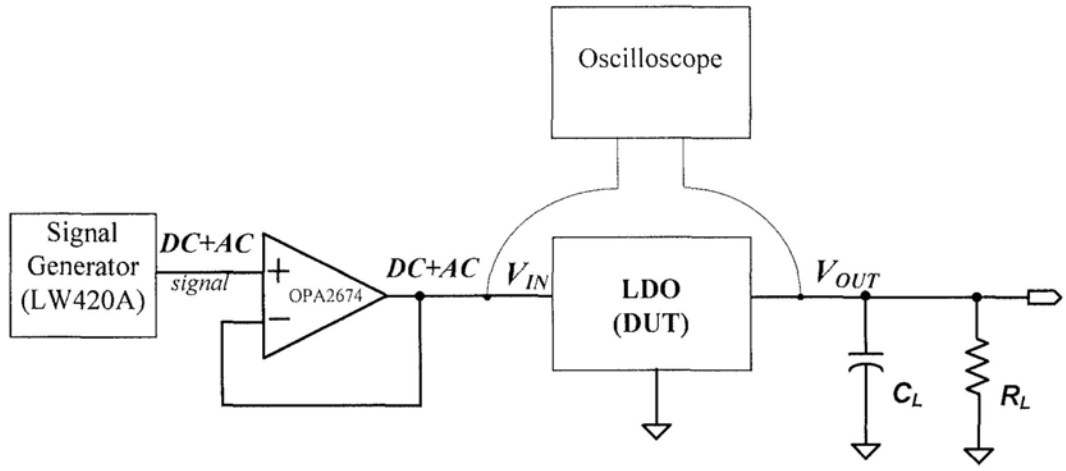


Fig. 3.20 PSRR setup through voltage buffer and oscilloscope

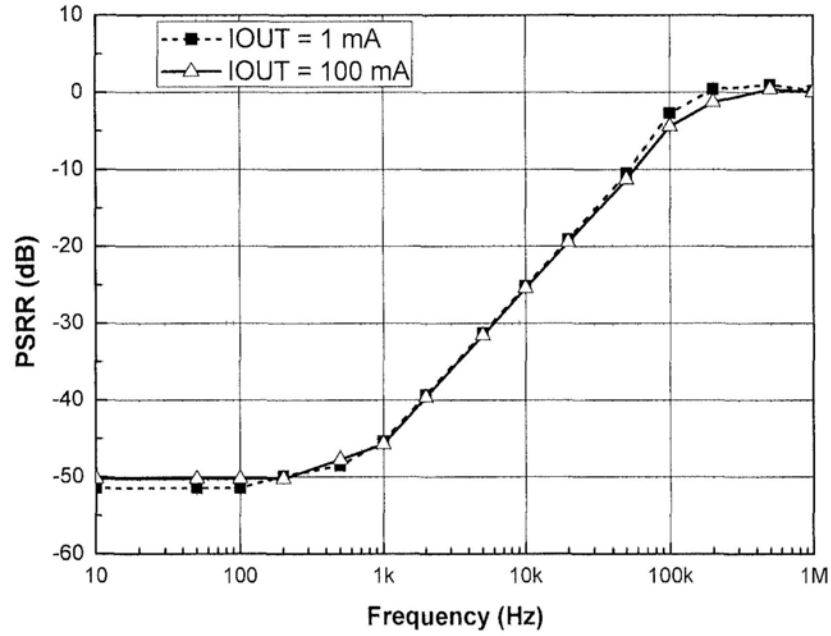


Fig. 3.21 Measured PSRR vs. frequency for I_{OUT} = 1 mA and I_{OUT} = 100 mA when $V_{OUT} = V_{REF}$ = 0.5 V, V_{IN} = 1 V and C_{OUT} = 10 pF

3.2.4 Performance comparison

Performance comparison between the proposed OCL-LDO and some selected recently-published OCL-LDOs is shown in Table 3.3. Due to the implementation in the 90-nm CMOS technology, the proposed LDO has the smallest chip area. More importantly, the proposed LDO does not need a large on-chip output capacitor as in [14], and thus the proposed LDO shows more suitable for high-density SoC applications. Moreover, the proposed LDO can operate in an ultra-low-voltage supply of 0.75 V, and it achieves the lowest quiescent current of 8 μA among other designs. Both the line and load regulations are good as well. The measured transient performance shown in Section 3.2.3 reflects the design has good small-signal and large-signal responses under a low-I_q level.

When comparing the load transient performance, both the output voltage variation (ΔV_{OUT}) and the edge time taken for the change of the output current (Δt) relate to each other closely. In typical LDO design with an output capacitor, when the load current change is faster than the loop response of a LDO, the output capacitor will be charged or discharged until the LDO can respond the change. In that case, the voltage spike is directly related to the output capacitance. However, in OCL-LDO design, there is no output capacitor. The equivalent lumped capacitance at the output of an OCL-LDO is a few tens of pF and is not helpful to the transient response. In fact, the equivalent output capacitance is a big problem to the OCL-LDO stability [13], [15] –[20]. As a result, the figure of merit (FOM) proposed in [14], which includes the dependence of the output capacitance, is not suitable for the comparison of different

OCL-LDOs. In addition, the edge time is another key factor affecting the response speed of an OCL-LDO. This effect can be proved by the experimental results shown in Fig. 3.12 and Fig. 3.13. Based on these considerations, a new FOM for comparison of different OCL-LDOs, which takes ΔV_{OUT}, ΔI_{OUT}, I_q, and Δt into account, is proposed in this section. It is given by

$$\text{FOM} = K\left(\frac{\Delta V_{OUT} \cdot I_q}{\Delta I_{OUT}}\right)$$

where K is edge-time ratio which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}}$$

It is noted that the unit of this FOM is volt. The K-factor does include a mutual comparison of the edge time used in the measurement of the OCL-LDOs. Since the edge time used in [14] is the smallest in the comparison, it becomes the reference of other designs and its K-factor equals to 1. A smaller FOM of an OCL-LDO design implies that the transient response of this design is better. From Table 3.3, it shows that the proposed LDO has the smallest FOM.

3.2.5 Conclusion

In this chapter, a 0.75-V output-capacitorless LDO implemented in 90-nm CMOS technology is presented. Closed-loop stability under output-capacitorless condition is maintained by a single Miller capacitor. Even though the quiescent current is as low as 8 μA, the voltage spike generated during transient change of the load current is small due to the proposed pseudo Class-AB error amplifier. Both line and load regulations are also improved due to the added non-inverting gain stage. Moreover, the required on-chip

capacitor is small, and so the chip area of this design is much smaller than one published design implemented in 90-nm CMOS technology. The achieved specifications of the proposed LDO (i.e. 100-mA load capability and 0.5-V minimum output) are suitable for modern low-voltage mixed-signal SoC applications.

Table 3.3 Performance comparison with recent published OCL-LDOs

	[13]	[14]	[15]	[18]	[19]	[6]	**This work**
Year	2003	2005	2006	2007	2008	2010	**2010**
Technology (μm)	0.6	0.09	0.18	0.35	0.35	0.35	**0.09**
Chip area (mm^2)	0.307	0.098	0.122	0.120	0.342	0.155	**0.019**
V_{IN} (V)	1.5–4.5	1.2	0.65–0.95	3–4.2	3–5	0.95–1.4	**0.75 – 1.2**
V_{OUT} (V)	1.3	0.9	0.5	2.8	2.8	0.7 – 1.2	**0.5 – 1**
I_q (μA)	38	6000	12.72	65	170	43	**8**
I_{OUT} (max) (mA)	100	50	50	50	100	100	**100**
I_{OUT} (min) (mA)[1]	10	0	0	0	0.05	≤ 0.58	**1**
Dropout voltage (mV)	200	300	150	200	200	200	**200**
Line regulation (mV/V)	±0.25%	N/A	~ 30	~ 23	3.3	N/A	**3.78**
Load regulation (mV/mA)		1.8	~ 0.19	~ 0.56	0.02	~ 0.4	**0.1**
On-chip capacitance (pF)	~ 12	600	N/A	23	6.5	6	**7**
ΔV_{OUT} (mV)	~ 120	90	300	~90	~ 80	~ 70	**114**
ΔI_{OUT} (mA)	90	50	50	50	~ 100	99	**97**
Edge time Δt (μs)	0.5	0.0001	~ 4	1	5	1	**0.1**
Edge time ratio K	5000	**1**	40000	10000	50000	10000	**1000**
FOM $= K\left(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}\right)$ (V)	0.253	0.011	3.053	1.170	6.800	0.304	**0.009**

Note 1: I_{OUT} (min) is the minimal output current requirement when there is no off-chip capacitor.

3.3 Summary

Design factors related to transient response of LDO are concluded in this chapter. Some transient improvement methods are analyzed. Then a transient-enhanced OCL-LDO fabricated in 90-nm CMOS technology is proposed to achieve fast transient and excellent regulation performances at the same time with minimum 6-μW power consumed.

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CHAPTER 4. Design of Low-Power High-PSRR CMOS LDO for High-Performance Analog and RF Circuits♣

4.1 Introduction

Ripple-free power supply is essential for many noise-sensitive analogue and RF circuits. While highly efficient switching power supplies are commonly used to prolong battery life in portable end equipment such as mobile phones and PDAs, the internal circuitry of some of these devices is sensitive to noise and therefore does not operate properly when powered from a switching power supply with output ripple. Audio circuitry, PLLs, RF transceivers, and ADCs/DACs are just a few examples of such circuits [1]. For example, in the noise system environment, the power-supply ripple rejection (PSRR) limits the dynamic performance of the ADC [2] and affects the jitter performance of clock generation circuits, [3], [4]. LDO with high PSRR is an ideal choice as a post regulator of switching DC-DC converter to provide clean voltage source. With the increase of switching frequency to several MHz even several tens of MHz to reduce PCB area and component cost [5], [6], LDO with high PSRR under wide bandwidth is required. On the other hand, modern wireless communication standards feature wider signal bandwidth. For example, signal bandwidth in WiMAX systems

♣ The material presented in this chapter has been presented in the Student Research Preview Session of ISSCC 2011 with the title of "High PSRR LDO with Embedded Ripple Feed-Forward Path".

ranges from 1.25 MHz to 28 MHz [7]. To meet the more strict requirement of transmit mask, LDO should has small noise including output ripple caused by the supply rail under wide bandwidth [8].

The PSRR is a measure of a circuit's power-supply rejection (PSR) expressed as a ratio of output noise to noise at the power-supply input. It provides a measure of how well a circuit rejects ripple at various frequencies injected from its input power supply [9]. In the case of linear regulators, PSRR is a measure of the regulated output-voltage ripple compared to the input voltage ripple over a wide frequency range and is expressed in decibels (dB), i.e.,

$$PSRR = 20\lg\frac{v_{out}}{v_{in}}. \tag{4.1}$$

More specifically, PSRR for an LDO can be written as

$$PSRR = 20\lg\frac{A_{VO}}{A_V}. \tag{4.2}$$

where A_V is the open-loop gain of the regulator feedback loop, and A_{VO} is the gain from V_{IN} to V_{OUT} with the regulator feedback loop open. From this equation, it can be seen that to improve the PSRR it is beneficial to increase the open-loop gain and decrease the gain from V_{IN} to V_{OUT}.

The remaining parts of this chapter are organized as follow. A series of measurement methods for LDO PSRR are concluded in Section 4.2, where many design tips are given. The basic analysis of PSRR in traditional LDOs is given in Section 4.3, and then some popular methods to improve LDO PSRR performance are

discussed in Section 4.4. In Section 4.5, a LDO fabricated in 0.18-μm CMOS technology is reported to achieve high PSRR under wide bandwidth based on proposed embedded ripple feed-forward cancellation technique. Finally, conclusions and discussions are given in Section 4.6.

4.2 LDO PSRR Measurement Methods

The measurement of PSRR of LDO is not trivial as the signal from the supply is attenuated much and appears at output. In order to achieve accurate measurement results, in this chapter, a series of measurement methods for LDO PSRR are given.

The basic method of measuring PSRR is shown in Fig. 4.1. The input supply generator provides input voltage, where DC information and AC ripples at different frequencies are included, to the device under test (DUT), i.e., LDO in this thesis. The ripples, i.e., AC voltages, appearing at the input and output terminals are measured and the PSRR can be gotten through their ratios automatically by machine or calculated by hand. At the same time, the DC voltages of LDO input and output should be monitored through oscilloscope to make sure that V_{IN} and V_{OUT} are in their respective normal ranges.

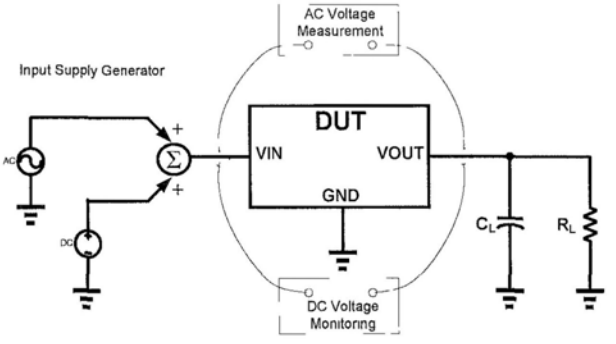


Fig. 4.1 LDO PSRR measurement setup

Many PSRR measurement methods have been mentioned in [10]. However, it is still necessary to summarize them for a systematic study. The PSRR measurement methods are summarized in this chapter based on different input supply generators and ripple voltages measurement strategies.

4.2.1 Methods of input ripple injection

There are many kinds of input supply generator, and each has its advantages and drawbacks or limitations, just like analog IC design.

(1) Direct input ripple injection

The most direct way to provide input power for LDO is using a signal generator with DC bias ability and driving capability. However, many signal generators cannot provide DC bias. Moreover, most signal generators have very poor driving capability. This is often occurred when the load current is low. For example, arbitrary waveform generator LeCroy LW420A can provide at least 1-mA driving capability with DC bias ability in our measurement, which makes the PSRR test become very simple in low-power design like passive RFID.

(2) Input ripple through capacitor coupling

The more popular way to inject AC signal to LDO input is using capacitor-coupling technique. *RC* and *LC* summing node methods are two examples, which are shown in Fig. 4.2. In this method, DC voltage and AC voltages are summed together and applied at the input of the LDO. V_{DC} is the operating point bias voltage and V_{AC} is the noise source used in the test. *R* (or *L*) and *C* are used for isolating both

the sources, V_{DC} and V_{AC}, from each other.

The R (or L) and C create a high pass filter for V_{AC} which will limit how low in frequency we can measure the PSRR. The 3-dB point of this filter, $f_{\min}$, is determined by

$$f_{\min} = \frac{1}{2\pi RC} \text{ or } f_{\min} = \frac{1}{2\pi\sqrt{LC}} \tag{4.3}$$

Frequencies below $f_{\min}$ will start to be attenuated which will make measurements more difficult. The highest frequency that can be measured is determined by the self-resonant frequencies of the L and C components.

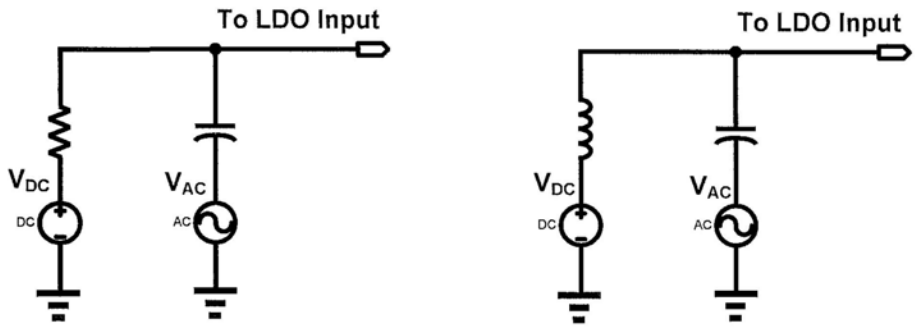


Fig. 4.2 AC signal injection through capacitor coupling

The 3-dB point can be extended by increasing the values of R (or L) and C. However, large R will increase the IR drop across the resistor, which is more serious in heavy-load conditions. In this case, V_{DC} is under very high level. Engineers should be very careful since many wrong operations may make this high voltage transform to LDO input directly and damage the LDO chip.

The more convenient way to use LC summing node method is to replace the discrete LC by an integrated device, named Bias Tee, like shown in Fig. 4.3 [11]. The main specification for LDO PSRR measurement is its minimum operation frequency and load capability. The maximum operation frequency of typical Bias Tee often

exceeds the requirement in LDO PSRR measurement. For example, Bias Tee with model name 5546, manufactured by Picosecond Pulse Labs., features 3.5-kHz to 7-GHz bandwidth and 500-mA load capability.

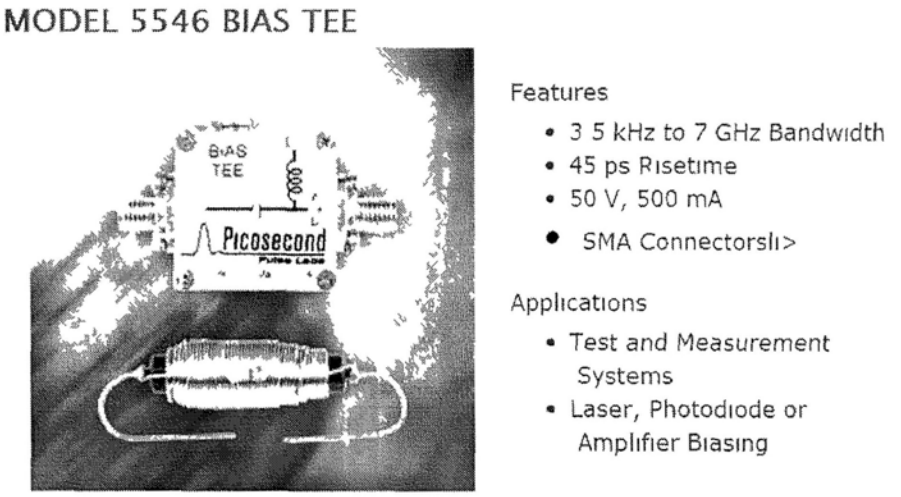


Fig. 4.3 A commercial Bias Tee and its main specifications and applications [11]

(3) Transformer

A different way is to use a transformer to inject the AC signal. A transformer is placed in series with the power supply. This transformer must be able to handle the DC current drawn by the DUT. A capacitor is placed in parallel with the power supply to give an AC-signal path to GND. The AC signal is then injected into the supply line via the transformer. The test setup for ripple injection is shown in Fig. 4.4.

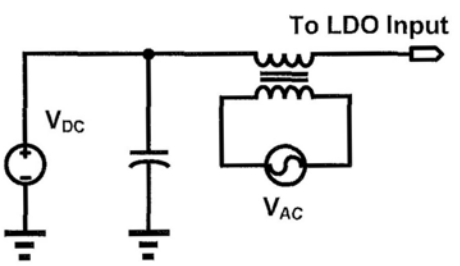


Fig. 4.4 AC signal injection through a transformer

(4) Voltage follower based on operational amplifier (Op Amp)

As mentioned before, signal injection through capacitor coupling suffers a

problem caused by minimum 3-dB frequency. This can be solved by introducing an Op Amp function as voltage follower to transform both DC bias and AC ripples to LDO input if the signal generator can provide both DC bias and AC signal. An additional Op Amp is needed when signal generator cannot provide DC bias voltage. A solution for this problem is shown in Fig. 4.5 [12]. DC bias voltage and AC signal (through a voltage buffer) are summed through a summing amplifier to provide power supply to LDO input.

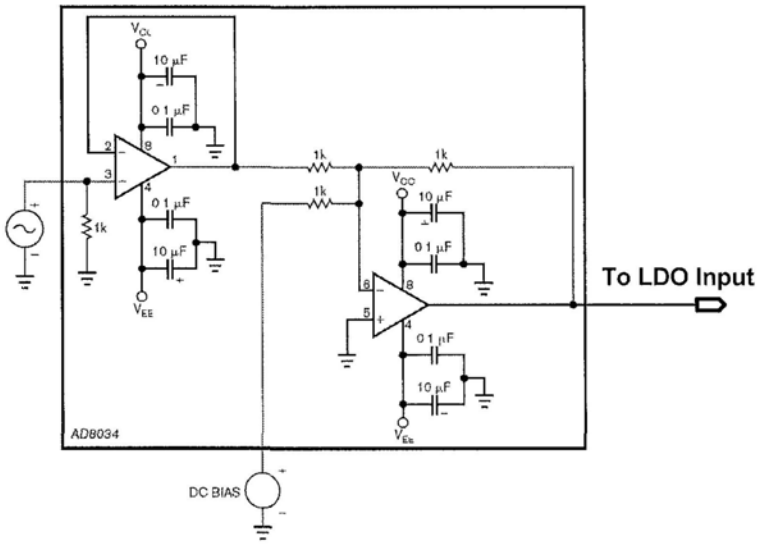


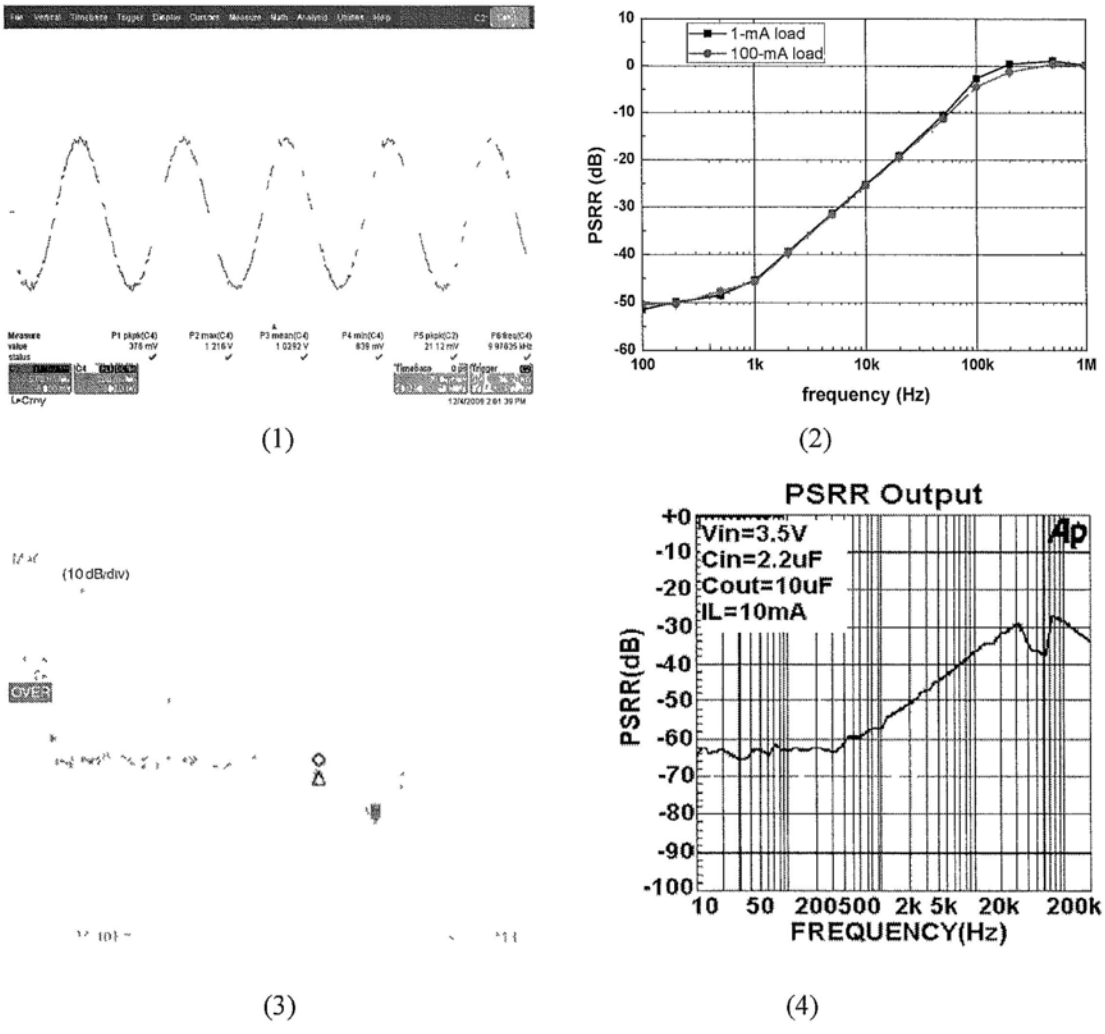
Fig. 4.5 A input supply solution for signal generator without DC bias ability by using AD8034 [12]

4.2.2 Methods of ripple voltage measurement

The input voltage ripples can be measured easily by oscilloscope directly since its amplitude is often higher than 100 mV. However, the output ripples are very small with the rejection of LDO circuit. In general, the output ripples cannot be measured precisely if the LDO's PSRR is better than -50 dB. Spectrum analyzer is preferred to measure the power or magnitudes of voltage ripples in both input and output, and

PSRR can be calculated by the amplitude ratio between the LDO output and input at different frequencies. Network analyzer provides a more convenient method. Both the input and output ripples can be measured at the same time. The PSRR curves can be plotted by the equipment directly. If either of spectrum and network analyzer is not available, LDO PSRR can also be measured by AP analyzer through a similar way in [13]. The frequency range is limited by the equipments. For example, the effective frequency range of AP analyzer is about 20 Hz – 200 kHz.

Fig. 4.6 shows some PSRR curves measured through different equipments.



(1) (2)

(3) (4)

Fig. 4.6 PSRR plots measured by different equipments

(1) Oscilloscope (2) Spectrum analyzer (3) Network analyzer [14] (4) AP analyzer [15]

4.3 Basic analysis of PSRR in traditional LDOs

The LDO PSRR transfer function can be viewed as the effect of a voltage divider caused by the impedance between the input supply and the regulator output and the impedance between the output and ground [16]. The intuitive and insightful model is presented in Fig. 4.7.

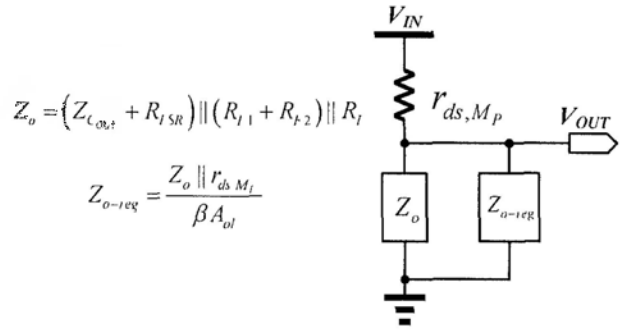


Fig. 4.7 A simple modeling to investigate the PSRR of LDO

The PSRR transform function can be found from the above model:

$$PSRR = \frac{v_{out}}{v_{in}} = \frac{z_o \| z_{o-reg}}{r_{ds,M_P} + (z_o \| z_{o-reg})} \tag{4.4}$$

Some conclusions can be found from the above modeling.

(1) At low frequencies, since the high loop gain ($\beta A_{ol\text{-}dc}$) allows $z_{o\text{-}reg}$ to shunt z_o, the PSRR of the regulator is intimately related to the open-loop gain of the system. The most direct way to improve LDO PSRR at low-frequency range is to increase the open-loop gain, while stability is hard to fulfill in that case.

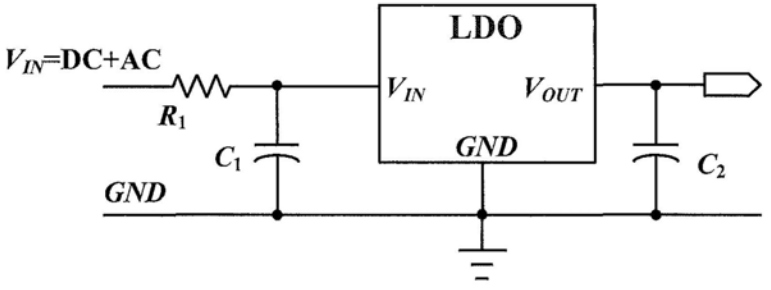
(2) At moderate frequencies, the shunting effect of the feedback loop deteriorates at the frequency beyond the bandwidth of error amplifier, this leads to the degradation of PSRR. However, the output capacitor also starts to shunt the LDO output ripples to

ground, which will improve the PSRR. Whether the PSRR is improved or degraded first is decided by the frequency of output pole and the bandwidth of the error amplifier.

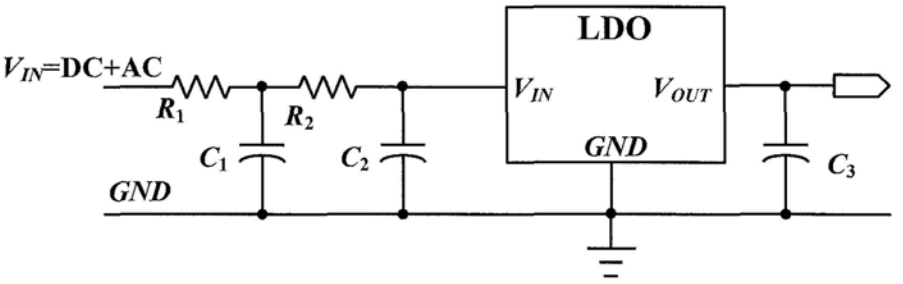
(3) At high frequencies, the PSRR is dominated by the ESR and ESL of output capacitor. The best PSRR often happens at the resonate frequency of output capacitor since the shunt effect is best in that point. After that, PSRR is degraded due to the existence of ESL. An effective way to improve the PSRR in high frequency range is to allocate more small decoupling capacitors to decrease the total equivalent ESR and ESL.

4.4 Methods to improve LDO PSRR

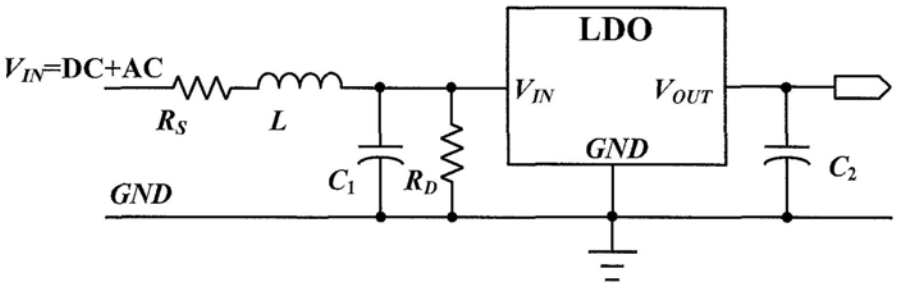
The most direct way to modify the basic rejection response of the regulator is to add an external network at the input of the regulator. Single order or second-order *RC* network, *LC* filter, or additional LDO is effective to improve PSRR performance [17], the diagrams of which are shown in Fig. 4.8. Actually, the isolation between input power supply and LDO output is enhanced effectively in these configurations.



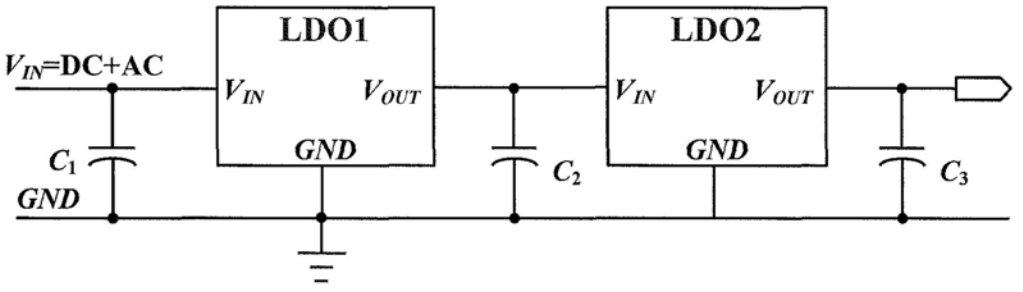
(1) Single *RC* ripple filter



(2) Second-order cascade *RC* ripple filter



(3) *LC* filter



(4) Series cascade of LDOs for input ripple isolation.

Fig. 4.8 Some PSRR improvement methods by adding external filters

The drawbacks of the PSRR improvement methods mentioned above are low power efficiency, large PCB size and high components costs.

Application engineers may have no other choices when some LDOs are designated. For IC designer, there are some better choices. As analyzed in Section 4.2, the most direct way to improve PSRR, both the magnitude and bandwidth, is designing a high-gain high-bandwidth error amplifier. For example, an integrated LDO for VCO's supply, reported in [18], has a dc loop gain higher than 90 dB and a

wide unity-gain bandwidth of 176 MHz, and it achieves a simulated –97 dB at DC, –80 dB at 100 kHz frequency and –60 dB at 1 MHz frequency. High quiescent current is obviously needed in that case, which is not suitable for energy-efficient portable wireless systems. Stacking more power transistors to enhance the isolation between input supply and LDO output is also an effective way to improve PSRR [19]–[21]. However, the equivalent dropout voltage is increased and then minimum input requirement is increased too, which leads to the degradation of power efficiency obviously. Moreover, stacked power transistors occupy much more chip area.

The main idea behind some other existing methods of achieving high PSRR is to provide a signal path to duplicate the input supply ripples to the gate of power transistor to achieve ripple cancellation. Voltage subtractor with a diode-connected transistor between the supply and the gate of power transistor was adopted to improve PSRR in low-frequency range [22], [23]. Current-mode LDO was proposed to enhance the PSRR at high frequency with the cost of more than 180-pF on-chip capacitance needed, which leads to 1.2-mm^2 chip area in 1.5-μm bipolar technology [24]. A recently reported CMOS LDO by using a feed-forward path can achieve high PSRR better than -56 dB up to 10 MHz [25]. Its block diagram is shown in Fig. 4.9. Although the high-bandwidth error amplifier is not needed there, the feed-forward amplifier and summing amplifier consume more power to achieve high-bandwidth operation for regenerating the high-frequency ripples at the gate of power transistor.

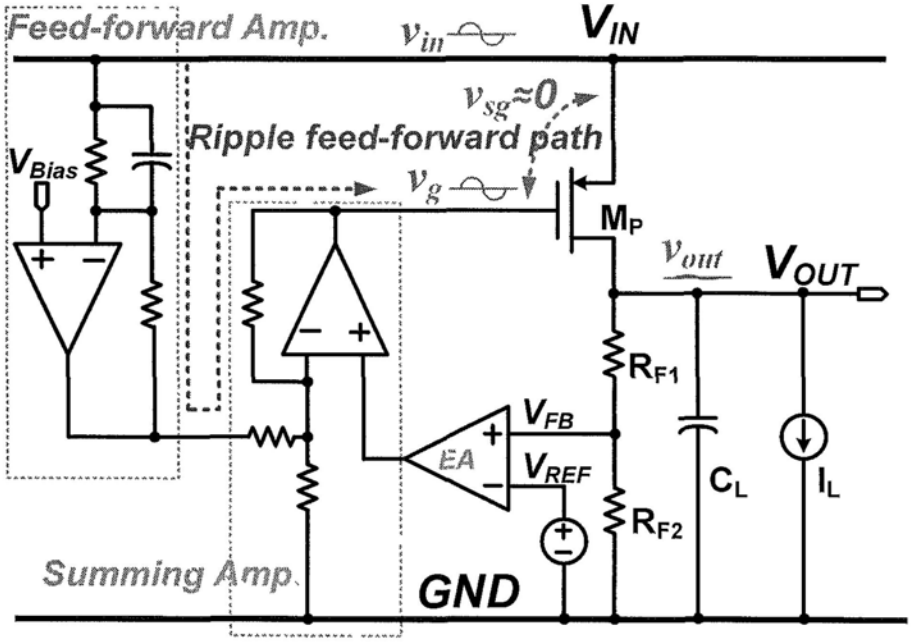


Fig. 4.9 A high-PSRR LDO with ripple cancellation by feed-forward and summing amplification

4.5 High PSRR LDO with embedded ripple feed-forward path

Based on above considerations, an embedded feed-forward path (EFFP) is proposed to extract ripples from the supply rail to the gate of power transistor to improve PSRR. It reuses the buffer stage which is commonly adopted in the traditional LDO and no additional static power is consumed. Only two low-pass filters (LPFs) are added comparing with the typical design. The LDO's PSRR can be improved effectively up to several MHz.

4.4.1 Proposed idea

The block diagram of proposed LDO is shown in Fig. 4.10. Only two transistors, M_2 and M_1, in the same single current branch, are used to conduct similar function of the

feed-forward amplifier and summing amplifier reported in [25]. Considering M_2 as a common-gate amplifier, the input supply ripple is feed-forwarded to the gate of power transistor M_P with a gain of g_{m2}/g_{m1} since its output terminates the source of M_1. A low-pass filter (LPF) is introduced to shunt the gate of M_2 to the AC ground to make it operate as a common-gate amplifier after the corner frequency of the LPF. Ignoring the supply ripple from the EA, which will be discussed later, the ripple voltage appearing at the gate of M_P can be set to close to supply ripple by setting the proper size ratio of M_2 to M_1, so the source-gate voltage of M_P is free of ripples and the LDO's PSRR can be improved.

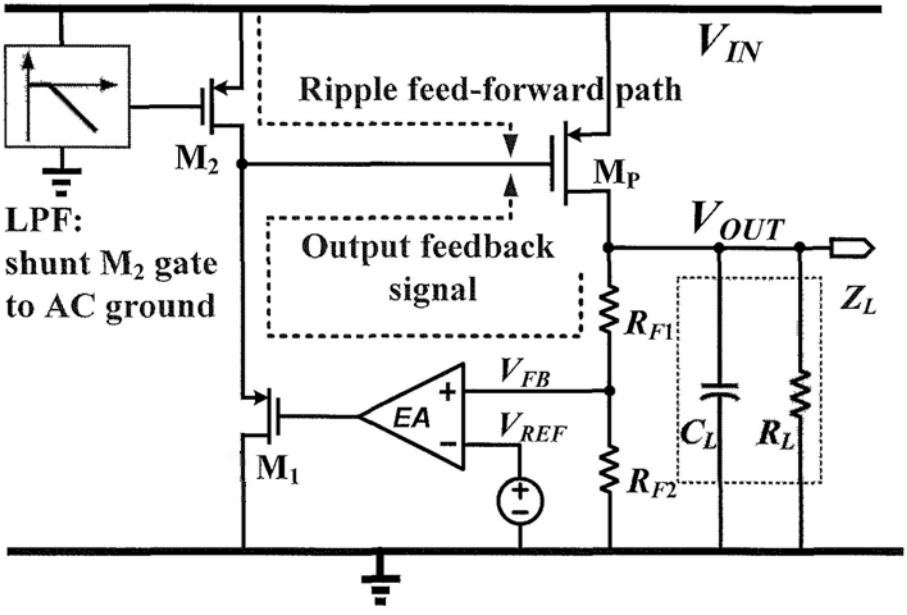


Fig. 4.10 Block diagram of proposed LDO

In fact, the equivalent feed-forward and summing amplifiers acted by M_2 and M_1 are also the typical buffer stage in traditional LDO design. It indicates the feed-forward path is embedded into the buffer stage and no additional static power is needed for EFFP. As a result, this simple single-transistor structure consumes much less power to achieve high PSRR over a wide range of frequency.

In [25], the feed-forward and summing amplifications are designed step by step, and the gain is decided by the resistance ratio. While in the proposed LDO, the feed-forward and summing amplifications are combined together in current form through a traditional buffer stage, and the gain is decided by the size ratio of M_1 and M_2. M_2 provides DC bias current to buffer as a current source and feeds-forward supply ripples to the gate of M_P as a common-gate amplifier at the same time.

The supply ripples from the voltage reference and EA can be removed by a LPF. The details will be discussed in the next section. Based on this, the signal flow chain from input supply to LDO output of the proposed LDO is shown in Fig. 4.11. Since both M_1 and M_2 can have higher bandwidth operation than the EA, the gain of common-gate amplifier formed by M_2 and the source follower formed by M_1 are approximated to g_{m2}/g_{m1} and 1, respectively. In that case, PSRR can be calculated by

$$PSRR|_{EFFP} = \frac{v_{out}(s)}{v_{in}(s)}$$

$$= \frac{1 + g_{m,M_P} \cdot r_{ds,M_P} \cdot (1 - \frac{g_{m2}}{g_{m1}})}{1 + \frac{r_{ds,M_P}}{Z_L(s)} + \frac{r_{ds,M_P}}{R_{F1} + R_{F2}} + \frac{R_{F2} \cdot g_{m,M_P} \cdot r_{ds,M_P} \cdot A_{eo}}{(R_{F1} + R_{F2})(1 + \frac{s}{\omega_e})}} \tag{4.5}$$

where A_{eo} is the gain of error amplifier, ω_e is the internal pole and $Z_L(s)$ is the equivalent impedance at the LDO output.

The optimum relationship between g_{m1} and g_{m2} can be found by setting the numerator of (4.5) to be zero by

$$g_{m1} = g_{m2} \cdot \frac{g_{m,M_P} \cdot r_{ds,M_P}}{1 + g_{m,M_P} \cdot r_{ds,M_P}}, \tag{4.6}$$

and the LDO has infinite PSRR in ideal case. The relationship between g_{m1} and g_{m2} is not fixed. The value of g_{m1}/g_{m2} should be considered carefully to make PSRR to be improved effectively in the whole load range.

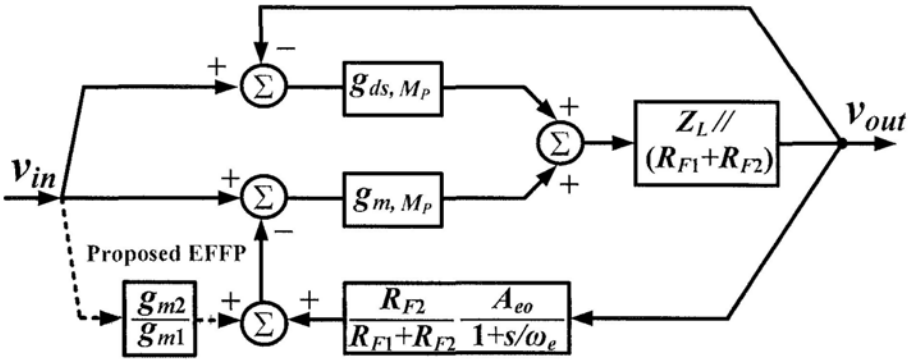


Fig. 4.11 Signal flow chain of proposed EFFP-LDO

Without the feed-forward path, it is the PSRR of a traditional LDO. It can be found easily from Fig. 4.11 by removing the g_{m2}/g_{m1} block and it is expressed as

$$PSRR|_{Trad} = \frac{v_{out}(s)}{v_{in}(s)} = \frac{1+g_{m,M_P}\cdot r_{ds,M_P}}{1+\frac{r_{ds,M_P}}{Z_L(s)}+\frac{r_{ds,M_1}}{R_{L1}+R_{L2}}+\frac{R_{L2}\cdot g_{m,M_P}\cdot r_{ds,M_P}\cdot A_{eo}}{(R_{L1}+R_{L2})(1+\frac{s}{\omega_e})}} \tag{4.7}$$

The theoretical PSRR improvement due to proposed EFFP is

$$\frac{PSRR|_{LLFP}}{PSRR|_{Trad}} = \frac{1+g_{m\,M_P}\cdot r_{ds\,M_P}\cdot(1-\frac{g_{m2}}{g_{m1}})}{1+g_{m\,M_P}\cdot r_{ds\,M_P}} \tag{4.8}$$

From (4.8), the PSRR improvement level is dependent on the output current due to different $g_{m\ MP}$ and $r_{ds\ MP}$. It indicates that the PSRR improvement in different load conditions is different. In this case, the output current range may be limited to keep high-PSRR performance.

The PSRR simulation results without and with EFFP under different load conditions are shown in Fig. 4.12. With EFFP, the PSRR can be improved up to 6 MHz and the maximum improvement is about 40 dB.

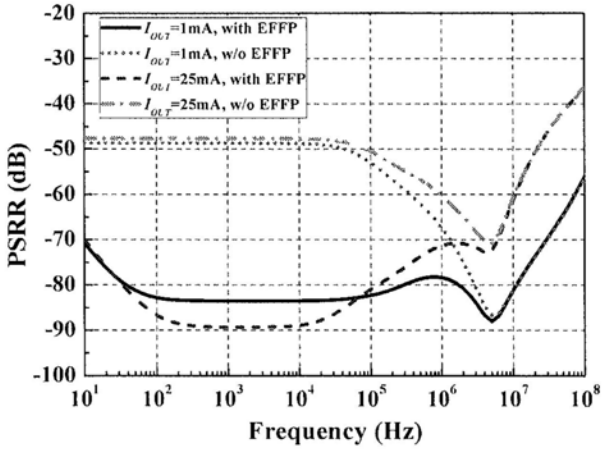


Fig. 4.12 PSRR simulation results with and without EFFP

4.4.2 Circuit Implementation

The complete schematic of the proposed LDO is shown in Fig. 4.13. It consists of EA, buffer stage and power stage with feedback network.

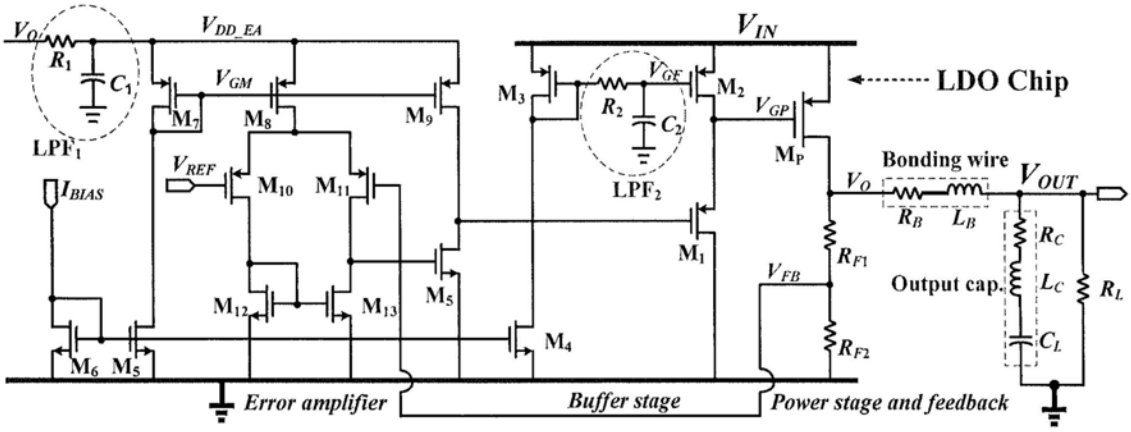


Fig. 4.13 Schematic of proposed EFFP-LDO

As mentioned before, EA should feature with high PSRR. The PMOS input stages are selected for better matching [9]. The power supply of EA is provided by the LDO

output through LPF_1, thus all ripples beyond the bandwidth of LPF_1 (i.e., f_{LPF1}) can be suppressed. Since large capacitance occupies large chip area and the *IR* drop of R_1 is limited, f_{LPF1} cannot be very low. To filter low-frequency ripple more effectively, the drain voltage of M_8 should be insensitive to V_{DD_EA} in the frequency range from DC up to f_{LPF1}. This can be achieved by setting V_{GM} to be similar to V_{DD_EA} to make source-gate voltage of M_8 is free of supply ripples. In that case, M_5 is set to have a very long channel length, and $v_{GM}/v_{DD\_EA} = r_{ds5}/(r_{ds5} + 1/g_{m7})$ is close to 1 in the low-frequency range. The ideal frequency responses from V_O to V_{GM} are shown in Fig. 4.14. f_{LPF1} is designed to be lower than f_{PD} (-3-dB bandwidth of the potential-division network consisting of M_5 and M_7) for better noise filtering.

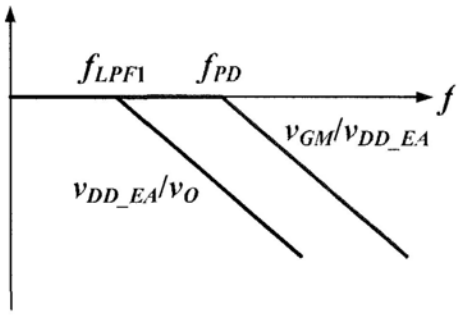


Fig. 4.14 Frequency response of LPF_2 and voltage divider.

A buffer stage is often used in typical LDO design to enhance the drive capability and move the pole located at the gate of power transistor to a higher frequency. In the proposed LDO, a supply ripple feed-forward amplifier and summing amplifier are combined together and embedded into a typical voltage buffer. This innovative structure reduces the power consumption and makes the LDO design become simpler.

As shown in Fig. 4.13, LPF_2 made by R_2 and C_2 are inserted between the gates of

M_3 and M_2. LPF_2 is used to bias the gate of M_2 and to shunt its gate to the AC ground. In this case, supply ripples are feed-forwarded to M_P gate directly with a gain approximate to g_{m2}/g_{m1}, which can be adjusted easily by setting the size ratio of M_2 to M_1.

The small-signal modeling of the proposed feed-forward amplifier is shown in Fig. 4.15. The feed-forward voltage gain can be calculated by

$$A_{ff} = \frac{v_{gp}}{v_{in}} \approx \frac{g_{m2} + sC_{gp}}{g_{m1} + sC_{gp}} \cdot \frac{sC_2R_2}{1 + sC_2R_2} \tag{4.9}$$

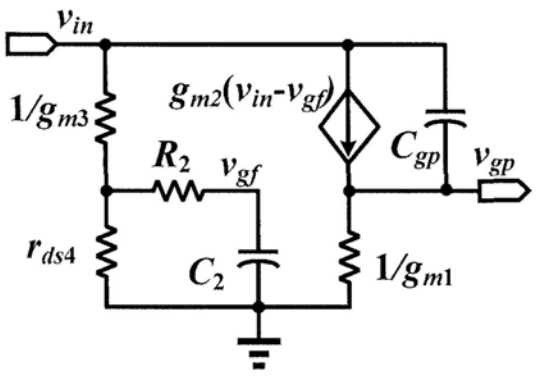


Fig. 4.15 Small signal modeling of embedded feed-forward amplifier

Large time constant of C_2R_2 is required to improve the PSRR in both low and medium frequency ranges to eliminate the requirement of high-gain EA. To save the chip area at the same time, a diode-connected PMOS transistor is used to implement the huge resistance of R_2 while C_2 is a MOS capacitor.

The Components' parameters of LPF_1 and LPF_2 are listed in Table 4.1.

Table 4.1 Components' parameters of LPF_1 and LPF_2

R_1 (Ω)	C_1 (pF)	R_2 (diode-connected PMOS)	C_2 (pF)
1 k	10	W / L: 240 nm / 400 nm	10

Based on (4.9), (4.5) can be expressed more accurately by

$$PSRR|_{EFFP} = \frac{v_{out}(s)}{v_{in}(s)}$$
$$= \frac{1 + g_{m,M_P} \cdot r_{ds,M_P} \cdot (1 - \frac{g_{m2} + sC_{gp}}{g_{m1} + sC_{gp}} \cdot \frac{sC_2R_2}{1 + sC_2R_2})}{1 + \frac{r_{ds,M_P}}{Z_L(s)} + \frac{r_{ds,M_P}}{R_{F1} + R_{F2}} + \frac{R_{F2} \cdot g_{m,M_P} \cdot r_{ds,M_P} \cdot A_{eo}}{(R_{F1} + R_{F2})(1 + \frac{s}{\omega_e})}} \quad (4.10)$$

The detailed analysis of PSRR presented in (4.10) will be given below with the considerations of parasitic effects from the bonding wire and from the output capacitor.

4.4.3 Design Considerations

Traditional modeling on the LDO output stage includes the load resistance and output capacitance with equivalent series resistance (ESR), and the bonding wire resistance is only used to evaluate V_{DO}. This modeling provides reasonable accuracy when loop bandwidth is much less than 1 MHz in typical conditions. However, the parasitic inductance of bonding wire and output capacitor cannot be ignored again in today's nano-scale CMOS technologies, especially when designing a LDO with loop bandwidth higher than 1 MHz.

Output stage with parasitic modeling on the bonding wire and the output capacitor is also shown in Fig. 4.13. The total equivalent output impedance can be approximated by

$$Z_O(s) \approx (r_{ds,M_P} // R_L) \cdot \frac{1 + \frac{s}{Q_z\omega_{zo}} + \frac{s^2}{\omega_{zo}^2}}{1 + \frac{s}{\omega_{po1}}} \quad (4.11)$$

where $Q_z = \frac{\sqrt{C_L(L_C + L_B)}}{C_L(R_C + R_B)}, \omega_{zo} = \frac{1}{\sqrt{C_L(L_C + L_B)}}, \omega_{po1} = \frac{1}{C_L(r_{ds,M_P} // R_L)}$.

Due to the parasitic effects of bonding wire and the output capacitor, the LDO is stable without any additional compensation circuits with the help of the zeros (i.e., ω_{zo}). The open-loop transform function can be expressed as

$$H(s) \approx A_o \frac{1 + \frac{s}{Q_z w_{zo}} + \frac{s^2}{w_{zo}^2}}{\left(1 + \frac{s}{w_{po1}}\right)\left(1 + \frac{s}{w_{po2}}\right)} \tag{4.12}$$

where $w_{po2} = \frac{1}{C_{pg} R_{o\_buffer}}$ is the first non-dominant pole and is decided by gate capacitance of power transistor (C_{pg}) and output impedance of the voltage buffer (R_{o_buffer}). The simulated loop gains with 1.5-V V_{IN} and under 1-mA and 25-mA load conditions are shown in Fig. 4.16. The DC open-loop gains are around 80 dB and the phase margin are larger than 90°. The UGF are 200 kHz and 3.5 MHz, respectively. The power transistor operates in sub-threshold region and saturation region, respectively.

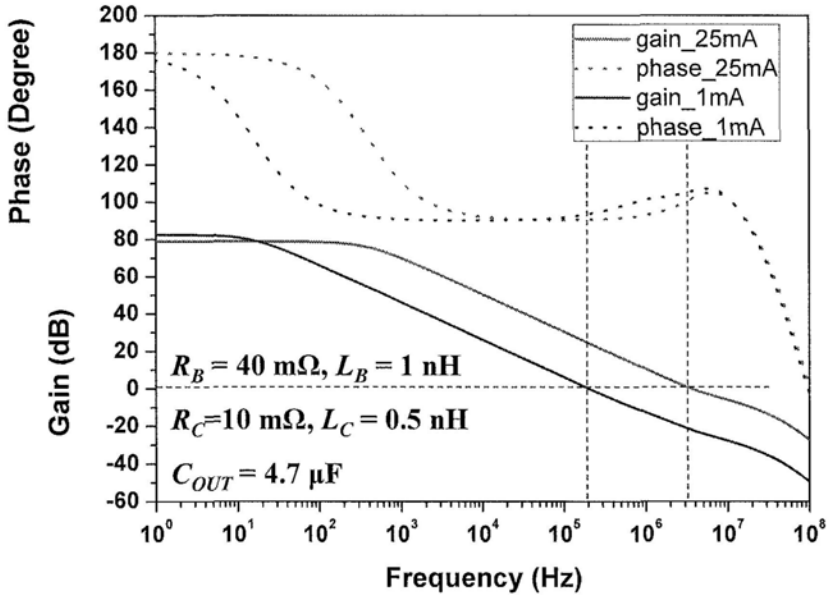


Fig. 4.16 AC simulation results of loop gain under different load conditions

In fact, the PSRR performance should be measured at V_{OUT} node instead of V_O node. The relationship between V_{OUT} and V_O is given by

$$\frac{v_{out}(s)}{v_o(s)} \approx \frac{s^2 C_L L_C + sC_L R_C + 1}{s^2 C_L (L_C + L_B) + sC_L (R_B + R_C) + 1} \tag{4.13}$$

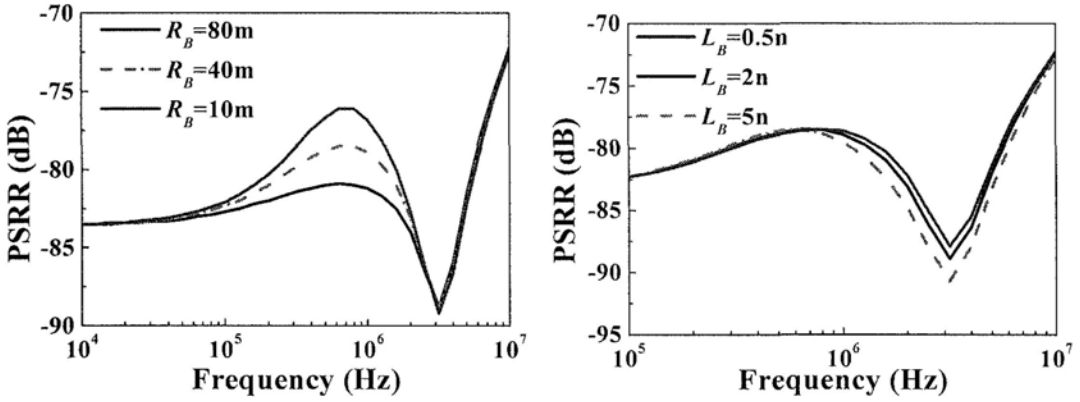
The influence of the bonding wire effect and the parasitic of the output capacitor can be investigated based on (4.10)–(4.13).

(A) The PSRR can be improved in the medium frequency range with larger R_B and L_B. This can be understood directly since the isolation between V_{IN} and V_{OUT} is enhanced. Simulation results with different values of R_B and L_B are shown in Fig. 4.17. This is a tradeoff with V_{DO}. Larger R_B increases V_{DO} and reduces the efficiency.

(B) The PSRR can be improved with smaller R_C in medium frequency range since a smaller R_C shunts the ripples to the ground more effectively when the PSRR is dominated by the output capacitance before resonant frequency.

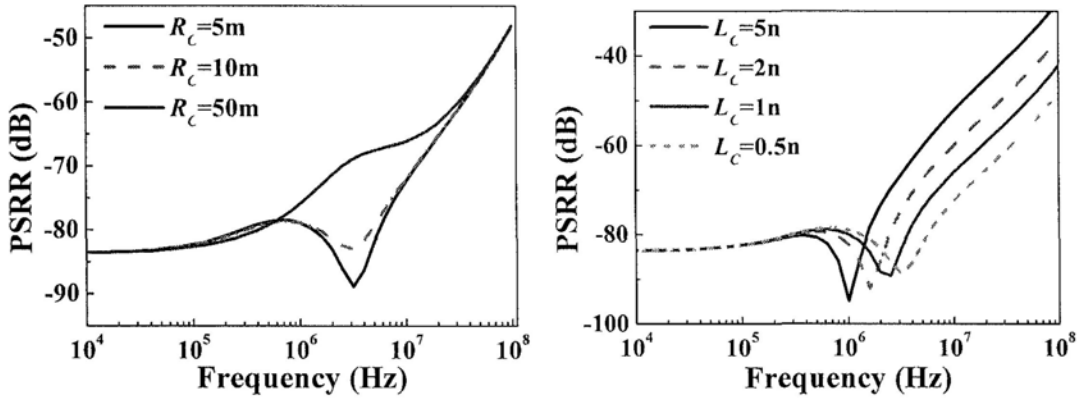
(C) The PSRR can be improved with smaller L_C in high frequency range. After the resonant frequency of the output capacitor, the PSRR is determined by its equivalent series inductance (ESL) L_C. Smaller L_C means better shunt performance and thus better PSRR in the high frequency range.

The PSRR simulation results with different values of R_C and L_C are shown in Fig. 4.18. They agree with the analysis well.



(a) (b)

Fig. 4.17 PSRR simulation results with different bonding wire (a) resistance and (b) inductance



(a) (b)

Fig. 4.18 PSRR simulation results with different (a) ESR and (b) ESL of C_l

Based on above analysis, the PSRR performance with proposed EFFP can be concluded here. At very low frequency, PSRR is dominated by the open-loop gain of LDO, and then it is improved when frequency beyond f_{LPF1}. After that, PSRR is mainly decided by the ripple feed-forward cancellation and is kept until the feed-forward effect starts to degrade when the ripple frequency is high and it reaches to the internal pole frequency (ω_e). With the further increase of frequency, C_L starts to shunt the ripples to the ground and the PSRR can be improved. The best PSRR is

achieved at the resonant frequency of C_L, i.e., $1/2\pi\sqrt{L_C C_L}$. After the resonant frequency, the PSRR is dominated by the ESR and ESL of the output capacitor and it is then degraded at higher frequencies.

In this situation, other than the design of high-PSRR LDO itself, the selection of output capacitor is very important. A single ceramic capacitor (C1632X5R0J475K from TDK Corporation) with small ESR and ESL is selected to conduct the measurement. To further improve PSRR in high frequency range, some capacitors may be needed to be parallel to decrease the effective ESR and ESL [25], or some additional decoupling capacitors are needed and located close the load circuits.

4.4.4 Experimental Results

The proposed EFFP-LDO has been fabricated in UMC 0.18-μm CMOS technology. The active chip area is 0.042 mm^2 and the chip photo is shown in Fig. 4.19.

PSRR measurement setup is shown in Fig. 4.20. The input ripples are injected to LDO input through a voltage follower based on OPA2674 [26], which can provide 500-mA driving capability and has 250-MHz unity-gain bandwidth. The amplitude of the input ripple is 200 mV. Both the input and output amplitudes are measured through spectrum analyzer (Agilent E4440A) and observed by oscilloscope (Lecroy 6100A) at the same time. Measured PSRR performances under different load conditions are shown in Fig. 4.21. With a 4.7-μF ceramic capacitor, the low-frequency PSRR are better than -60 dB and the best PSRR performance is achieved at 2.5 MHz, where the

PSRRs are -89 dB at 1 mA and -85 dB at 25 mA, respectively. Moreover, the wide-bandwidth high PSRR are achieved, the -55 dB lowest PSRR performance up to 5 MHz is measured under the 25-mA load condition. The measured PSRR in the low frequency range is not as good as the simulation values, possibly, due to the process variation and mismatch between g_{m1} and g_{m2}.

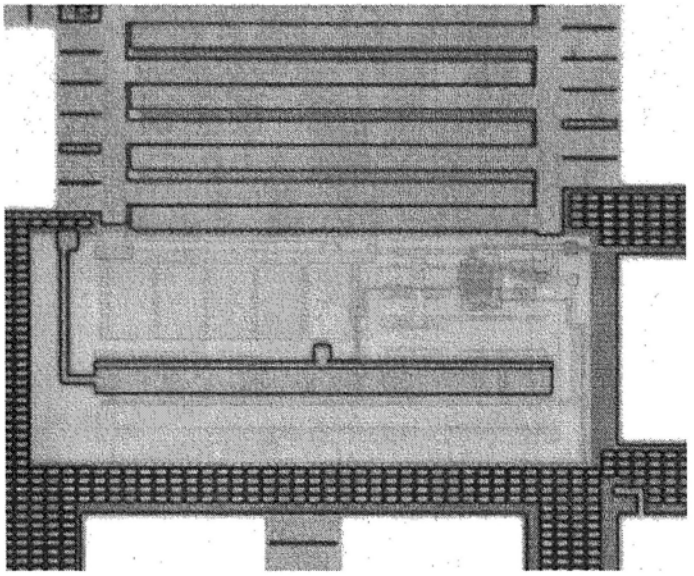


Fig. 4.19 Die photo of the proposed LDO

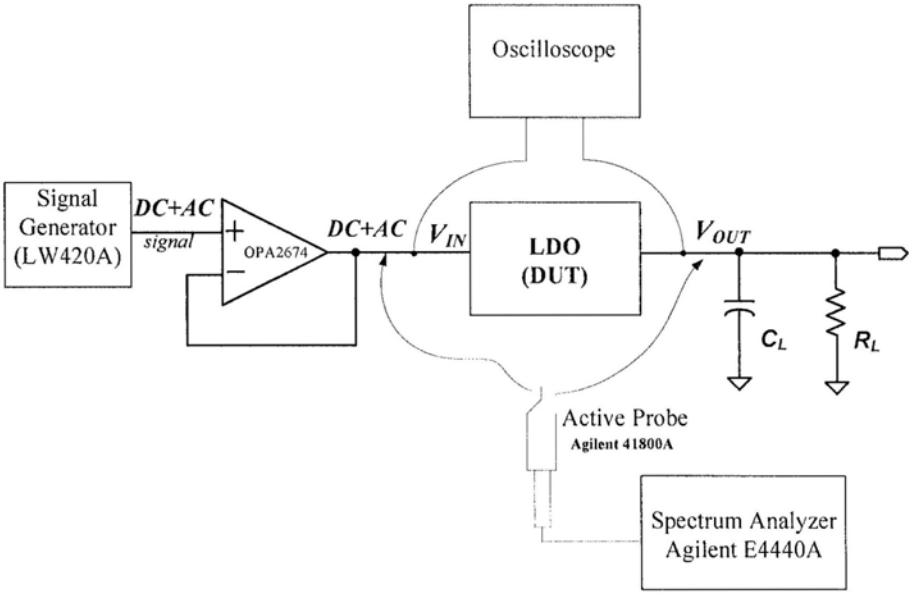


Fig. 4.20 PSRR measurement setup

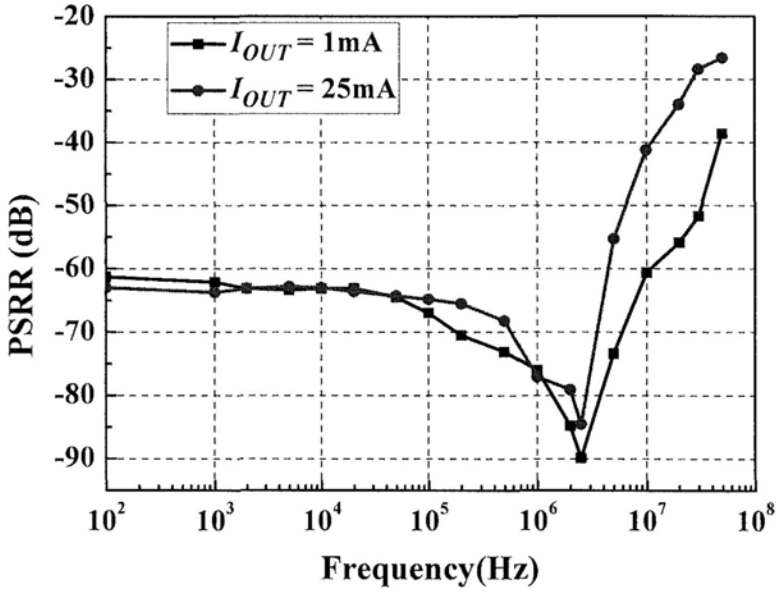


Fig. 4.21 Measured PSRR performance under different load conditions

The load transient response is shown in Fig. 4.22. The LDO is stable over the whole loading range and it responds fast under rapid load changes. Both the overshoot and undershoot are less than 40 mV when load current changes between 1 mA and 25 mA within 40 ns.

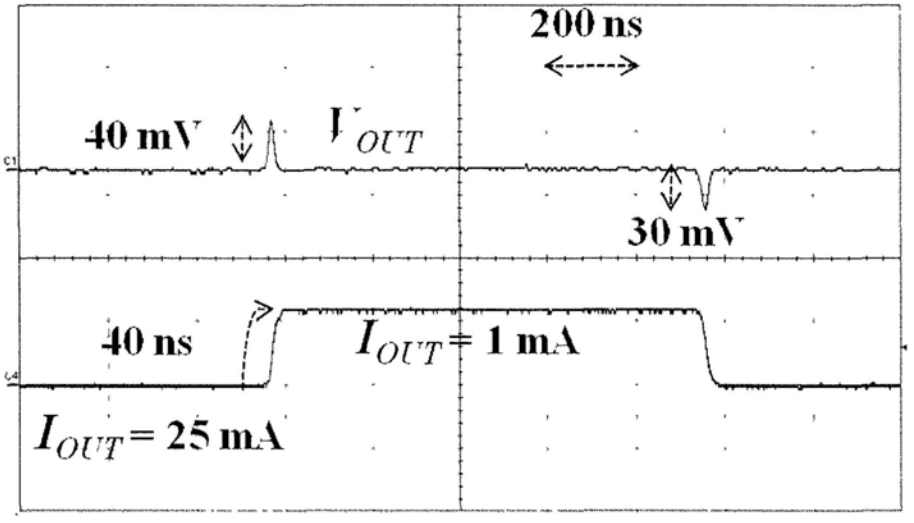


Fig. 4.22 Measured load transient response

Table 4.2 shows the performance comparison between the proposed LDO and a recently reported high-PSRR LDO [25]. Both of them have 25-mA load capability and are measured with around 4-μF output capacitance for a fair comparison of PSRR. It is well known that high V_{DO} can enhance the isolation between supply rail and LDO output to improve PSRR effectively in low-frequency range, and high I_q can widen the loop bandwidth to improve PSRR in medium-frequency range. However, even with a lower V_{DO} and consumed lower I_q, the proposed LDO can achieve better PSRR performance up to 2.5 MHz, and only a bit lower PSRR performance at 5 MHz due to more serious parasitic effects in the used 0.18-μm technology than the 0.13-μm technology used in the design reported in [25]. Moreover, a single output capacitor (i.e., relatively higher ESR and ESL effect) is used in this work.

Table 4.2 Performance Comparison

Parameters	[25]	**This work**
CMOS technology (μm)	0.13	**0.18**
Area (mm^2)	0.049	**0.042**
Dropout voltage V_{DO} (mV)	150	**100**
Maximum load current (mA)	25	**25**
Quiescent current I_q (μA)	50	**15**
Line regulation (mV/V)	N/A	**3**
Load regulation (μV/mA)	48	**50**
Output capacitance C_L	2 μF x 2	**4.7 μF**
PSRR (dB) @ max. loading		
100 kHz	-60	**-65**
2.5MHz	-80	**-85**
5 MHz	-62	**-55**

4.4.5 Conclusion

A ripple feed-forward path is proposed to improve the PSRR of CMOS LDO by ripple-cancellation technique. Principle validity has been verified through measurement results. Energy-efficient operation can also be achieved due to the simple structure and embedded characteristic. Moreover, the propose structure can be applied in most LDO topologies.

4.6 Summary

In this chapter, PSRR test and improvement methods are presented. Based on the detailed analysis on PSRR in traditional LDOs and some state-of-the-art methods for improving PSRR, an energy-efficient embedded ripple feed-forward path is proposed to improve the LDO's PSRR with simple structure and low power consumption. A LDO protocol fabricated in 0.18-μm CMOS technology verifies the validity.

In the future, OCL-LDO with high PSRR under wide bandwidth is preferred to further decrease the external components and chip area due to I/O pads. The main challenge is that smaller output capacitance decrease the shunt ability in high frequency range. One possible solution is to design a very high-gain high-bandwidth error amplifier and try to make LDO stable enough with internal compensation. High quiescent current is obviously needed in that case. An energy-efficient solution is required for many energy-aware systems. This will be our next research goal in the future work.

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CHAPTER 5. Conclusions and future works

5.1 Conclusions

Several topics on on-chip voltage regulation for energy-aware wireless SoC with low-power, fast-transient and high-PSRR performances have been discussed in this thesis. Three LDOs are designed and fabricated in nano-scale CMOS technologies to achieve the above performances for remotely- and battery-powered Wireless SoC. The contributions of the thesis are concluded as follow.

(1) CMOS voltage regulator with only 700-nA quiescent current is proposed to achieve ultra low-power low-voltage on-chip voltage regulation for remotely powered energy-autonomous devices. A self-biased mutually compensated CMOS voltage reference with sub-1-V operation is proposed to fit the voltage scaling trends. Moreover, it can save chip area effectively without the need of bipolar transistors and ultra large resistance for low-power issue.

(2) Direct voltage detection through capacitor coupling is applied to improve transient response for a 90-nm capacitor-free CMOS LDO. Multi-stage error amplifier with flipped voltage follower is adopted to improve DC regulations and achieve capacitor-free operations at the same time.

(3) PSRR measurement methods are summarized. Design and test engineers can select the most suitable method under their practical conditions to do the measurement.

(4) An energy-efficient embedded ripple feed-forward path is proposed to

improve the LDO's PSRR without additional static power consumption.

5.2 Future works

There are many interesting topics for further research inspired by the work described in this thesis.

(1) Low-power low-voltage CMOS reference circuit with high PSRR is preferred in energy-autonomous systems. Comparing with the state-of-the-art voltage references, pure CMOS voltage reference without the need of any bipolar transistor and resistor is the future design interest. The reference should also feature with the low-power, low-voltage and high-PSRR operations.

(2) High-PSRR CMOS LDO with capacitor-less operation is really challenging. Small output capacitance decreases the shunt effect in high-frequency range. In the future, we will try to decrease the output capacitance and achieve high PSRR simultaneously.