

Simo Hietakangas

DESIGN METHODS AND
CONSIDERATIONS OF
SUPPLY MODULATED
SWITCHED RF POWER
AMPLIFIERS

UNIVERSITY OF OULU GRADUATE SCHOOL;
UNIVERSITY OF OULU, FACULTY OF TECHNOLOGY,
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INFOTECH OULU



ACTA UNIVERSITATIS OULUENSIS
C Technica 419

SIMO HIETAKANGAS

**DESIGN METHODS AND
CONSIDERATIONS OF SUPPLY
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Academic dissertation to be presented with the assent of
the Doctoral Training Committee of Technology and
Natural Sciences of the University of Oulu for public
defence in Auditorium TS101, Linnanmaa, on 8 June 2012,
at 12 noon

UNIVERSITY OF OULU, OULU 2012

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Acta Univ. Oul. C 419, 2012

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ISBN 978-951-42-9835-6 (Paperback)
ISBN 978-951-42-9836-3 (PDF)

ISSN 0355-3213 (Printed)
ISSN 1796-2226 (Online)

Cover Design
Raimo Ahonen

JUVENES PRINT
TAMPERE 2012

Hietakangas, Simo, Design methods and considerations of supply modulated switched RF power amplifiers.

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Acta Univ. Oul. C 419, 2012

Oulu, Finland

Abstract

This thesis studies the design methods and properties of supply-modulated switch-mode radio frequency power amplifiers. Besides simulation based studies and theory review, two amplifiers were designed: a discrete MESFET class E amplifier (0.5 W at 1 GHz), and an integrated pHEMT class E⁻¹ amplifier (2.0 W at 1.6 GHz) with an on-chip resonator.

The existing design methods of the resonant output network of switching amplifiers were reviewed and some extensions on the handling of nonlinear capacitances were proposed. The effects of varying supply voltage were studied and suggestions were given to minimize V_{dd} / AM and V_{dd} / PM distortion in supply modulated amplifiers. The implementation of the bias feed was also discussed resulting in proposing a combination of a short transmission line and a small inductor, which provides both fast supply modulation and little effect on harmonic impedances.

The main contributions are related to the study of the input impedance of a class E power amplifier, where the effects of supply dependent input impedance and timing skew generated by injected harmonic distortion were analyzed. The stabilization of the amplifier was also discussed.

Based on the findings, a push-pull class E amplifier with extra cross-coupled feedback capacitors and second harmonic traps at the gates appears to be a very good starting point for a further study.

Keywords: high-efficiency amplifiers, modulation, radio frequency amplifiers, supply modulation, switching circuits, switching power amplifiers

Hietakangas, Simo, Käyttöjännitemoduloitujen kytkintyyppisten RF-tehovahvistimien suunnittelumenetelmistä.

Oulun yliopiston tutkijakoulu; Oulun yliopisto, Teknillinen tiedekunta, Sähkötekniikan osasto, PL 4500, 90014 Oulun yliopisto; Oulun yliopisto, Infotech Oulu, PL 4500, 90014 Oulun yliopisto

Acta Univ. Oul. C 419, 2012

Oulu

Tiivistelmä

Tämä väitöstyö käsittelee radiotaajuuksilla toimivien käyttöjännitemoduloitujen kytkintehovahvistimien ominaisuuksia ja suunnittelumenetelmiä. Suunnittelumenetelmiin liittyvän katsauksen ja simulaatioihin perustuvan tutkimusten lisäksi kaksi vahvistinta toteutettiin väitöstutkimuksen aikana: diskreettikomponentein toteutettu E-luokan vahvistin (MESFET, 0.5 W ja 1 GHz) ja integroituna piirinä toteutettu käänteinen E-luokan vahvistin (pHEMT, 2.0 W ja 1.6 GHz), jonka lähdön resonanssipiiri sisällytettiin integroituun piiriin.

Kytkinvahvistimien suunnittelumenetelmiä verrattiin ja kehitettiin edelleen siten, että suunnitteluvaiheessa voidaan ottaa huomioon esim. transistoripiirin takaisinkytkennässä olevan kapasitanssin epälineaarisuus. Työssä tutkittiin myös käyttöjännitemodulaation vaikutusta kytkinvahvistimien toimintaan, ja tutkimuksen tuloksena annettiin muutamia ehdotuksia käyttöjänniteriippuvan amplitudi- (V_{dd} / AM) ja vaihemodulaation (V_{dd} / PM) vähentämiseksi. Lähdön biasointipiiriin toteutukseen suositeltiin pienen kelan ja siirtolinjan yhdistelmää. Yhdistelmän avulla pyritään maksimoimaan modulaationopeus ja minimoimaan vaikutukset harmonisiin impedansseihin.

Pääkohtina väitöksessä ovat E-luokan kytkinvahvistimesta saadut tutkimus- ja mittaushavainnot käyttöjännitteen funktiona muuttuvasta transistorin tuloimpedanssista sekä suurikokoisen transistorin tuloissa tapahtuvan, säröytymisen aiheuttaman tulosignaalien ajoitusvirheen analyysi. Näiden lisäksi vahvistimen stabiilisuuteen kiinnitettiin huomiota.

Saatujen havaintojen perusteella voimme todeta, että push-pull -tyyppinen E-luokan vahvistin olisi mielenkiintoinen valinta jatkotutkimuksille.

Asiasanat: korkean hyötysuhteen vahvistimet, kytkinpiirit, kytkinvahvistimet, käyttöjännitemodulaatio, modulaatio, radiotaajuiset vahvistimet

Acknowledgements

This thesis is based on research work carried out at the Electronics Laboratory of the Department of Electrical Engineering and Infotech Oulu, University of Oulu, during the years 2004-2011.

First, I would like express my gratitude to my supervisor, Professor Timo Rahkonen for his brilliant guidance, support and patience during these years. Who could have known that the 'blessed moment' when I came to ask for a job in 2004, would lead to such a challenging and interesting research project. I wish to thank Professor Torben Larsen and Associate Professor Anne-Johan Annema for reviewing this thesis and BA Janne Rissanen for revising the English of the manuscript. I would also like to thank both Dr. Jukka Typpö and Lic.Tech. Timo Rautio for their comments and support as co-authors of two publications. A special thanks to Dr. Janne Aikio for his advice and comments how to improve this thesis. Also colleagues in the Electronics laboratory deserve my gratitude for the friendly and supportive working atmosphere.

I would like to thank the following foundations and institutions for financial support: The Academy of Finland, Infotech Oulu Graduate School, TEKES (the Finnish Funding Agency for Technology and Innovation), Nokia Foundation, Foundation of Tauno Tönning, Foundation of Ulla Tuominen, Foundation of Finnish Electronics Engineers and The Foundation of Riitta and Jorma J. Takanen. Also, I would like to show my gratefulness to the following companies for their support: TriQuint Semiconductor Inc., National Semiconductor Finland Oy, Elektrobit Oyj, AWR-APLAC Corp., and Esju Oy. My special thanks go to the personnel of the Department of Electronics and Telecommunications in the Norwegian University of Science and Technology (NTNU) and to the personnel of the Micro- and Nanotechnology Centre in the University of Oulu.

I would like to express my deepest gratitude to my wife, Virpi, for the unlimited love, support and understanding during these years. Benjamin, I want to thank you for your attention and all the ways of distracting me from my work and thus, for teaching me how to unwind. Mum and dad, thank you for the endless support and care. I would like to thank Sari, Sami and their families for caring and staying in touch regardless of the long distance in between. Also friends and relatives deserve my thanks for motivating me in my work. Finally, I would like to show my humble gratitude to God for giving me wisdom and strength to carry on and for keeping me under His protection.

Abbreviations

AC	<i>Alternating current</i>
ACPR	<i>Adjacent channel power ratio</i>
AM	<i>Amplitude modulation</i>
AM/AM	<i>Amplitude-to-amplitude modulation</i>
AM/PM	<i>Amplitude-to-phase modulation</i>
CMCD	<i>Current mode class D amplifier</i>
DAC	<i>Digital-to-analog converter</i>
DSP	<i>Digital signal processor</i>
EM	<i>Electromagnetic</i>
ET	<i>Envelope tracking</i>
EER	<i>Envelope elimination and restoration</i>
ESR	<i>Equivalent series resistance</i>
EVM	<i>Error vector magnitude</i>
FET	<i>Field-effect transistor</i>
GaAs	<i>Gallium arsenide</i>
HB	<i>Harmonic balance</i>
IC	<i>Integrated circuit</i>
Im	<i>Imaginary part of complex value</i>
IMD	<i>Intermodulation distortion</i>
LINC	<i>Linear amplification using nonlinear components</i>
LO	<i>Local oscillator</i>
LP	<i>Low pass (filter)</i>
MMIC	<i>Monolithic microwave integrated circuit</i>
PA	<i>Power amplifier</i>
PAE	<i>Power added efficiency</i>
PAR	<i>Peak to average ratio</i>
PCB	<i>Printed circuit board</i>
pHEMT	<i>Pseudomorphic high electron mobility transistor</i>
PM	<i>Phase modulation</i>
Re	<i>Real part of complex value</i>
RF	<i>Radio frequency</i>

SwPA	<i>Switching power amplifier</i>
UK	<i>United Kingdom</i>
US	<i>United States of America</i>
VMCD	<i>Voltage mode class D amplifier</i>
ZCS	<i>Zero current switching</i>
ZCDS	<i>Zero current derivative switching</i>
ZVS	<i>Zero voltage switching</i>
ZVDS	<i>Zero voltage derivative switching</i>
A	<i>Envelope information of radio frequency signal</i>
A_u	<i>Device gain in terms of supply</i>
B_{RF}	<i>Radio frequency bandwidth</i>
C	<i>Parallel tuning capacitance in class E⁻¹</i>
$C_{1,2\dots n}$	<i>Capacitance 1,2...n</i>
C_{DC}	<i>DC blocking capacitance</i>
C_{DE}	<i>Decoupling capacitor</i>
C_{ds}	<i>Drain-to-source capacitance</i>
C_{fb}	<i>Additional feedback capacitance</i>
C_{gd}	<i>Gate-to-drain capacitance</i>
C_{gs}	<i>Gate-to-source capacitance</i>
C_{in}	<i>Device input capacitance</i>
C_{j0}	<i>Zero bias capacitance</i>
C_o	<i>Parallel output capacitance</i>
C_p	<i>Resonant parallel capacitance in class E⁻¹</i>
C_r	<i>Resonant series capacitance</i>
C_s	<i>DC-block/series capacitance</i>
C_{tot}	<i>Total capacitance</i>
C_X	<i>Parallel tuning capacitance</i>
D	<i>Duty cycle</i>
f	<i>Frequency of operation</i>
f_o	<i>Fundamental frequency</i>
f_{max}	<i>Maximum achievable frequency</i>
$G_{1,2\dots n}$	<i>Gate node of transistor 1,2...n</i>
H_{2T}	<i>Second harmonic trap</i>
I	<i>In-phase term of radio frequency signal</i>
I_{dc}	<i>DC current from supply</i>

I_{ds}	<i>Drain current</i>
$I_{ds1,ds2\dots dsn}$	<i>Drain current of transistor 1,2...n</i>
I_{gd}	<i>Gate-to-drain current</i>
I_o	<i>Output current</i>
I_{res}	<i>Resonance current</i>
i_s	<i>Switch current</i>
j	<i>Imaginary term</i>
k	<i>Transistor off time</i>
K	<i>Rollet's stability factor</i>
L	<i>Series inductance in class E⁻¹</i>
$L_{1,2\dots n}$	<i>Inductance 1,2...n</i>
L_{bondw}	<i>Bondwire inductance</i>
L_p	<i>Resonant parallel inductance</i>
L_r	<i>Resonant series inductance</i>
L_{RFC}	<i>Bias inductance, RF choke</i>
L_{tot}	<i>Total amount of inductance, L_r+L_x</i>
L_x	<i>Series tuning inductance</i>
M	<i>Grading coefficient of pn-junction</i>
N_d	<i>Drain efficiency</i>
p	<i>Load normalized admittance of parallel output capacitance</i>
P_{diss}	<i>Device power dissipation</i>
P_o	<i>Output power</i>
q	<i>Load normalized resonator series impedance</i>
Q	<i>Phase quadrature term of radion frequency signal</i>
Q	<i>Quality factor</i>
Q_l	<i>Loaded quality factor</i>
R	<i>Resistive load</i>
R_1	<i>Fundamental tone resistance</i>
R_{on}	<i>On-state resistance of the transistor</i>
R_{paras}	<i>Parasitic resistance</i>
S_{11}	<i>Input port term of S-parameters</i>
S_{21}	<i>Gain term of S-parameters</i>
t	<i>Time</i>
T	<i>One wave period</i>
$T_{1,2\dots n}$	<i>Transistor 1,2...n</i>

V_{bi}	<i>Built-in potential</i>
V_{dd}	<i>Supply voltage</i>
V_{dd}/AM	<i>Supply-to-amplitude modulation</i>
V_{dd}/PM	<i>Supply-to-phase modulation</i>
V_{ds}	<i>Drain to source voltage</i>
$V_{ds1,ds2\dots dsn}$	<i>Switch voltage of transistor 1,2...n</i>
V_{gs}	<i>Voltage between gate and source</i>
V_{in}	<i>Input voltage</i>
V_o, V_{out}	<i>Output voltage</i>
v_s	<i>Switch voltage</i>
X	<i>Tuning term, tuning reactance</i>
X_2	<i>Tuning term, tuning reactance of second harmonic tone</i>
X_{ds}	<i>Drain-to-source reactance</i>
Y_{in}	<i>Device input admittance</i>
Z	<i>Impedance</i>
Z_1, Z_{fo}	<i>Fundamental tone impedance</i>
Z_{2fo}	<i>Second harmonic tone impedance</i>
Z_{Co}	<i>Impedance of parallel output capacitance</i>
γ	<i>Phase shift</i>
λ	<i>Wavelength</i>
ω	<i>Angular frequency</i>
ϕ	<i>Amplitude limited phase information of radio frequency signal</i>

List of original articles

This thesis is based on the following original articles, which are referred to in the text by their Roman numerals [I-VII]:

- I Hietakangas S, Rautio T & Rahkonen T (2007) Feedthrough cancellation in a class E amplified polar transmitter. 18th European Conference on Circuit Theory and Design (ECCTD) Sevilla, Spain 27-30 August 2007: 591-594.
- II Hietakangas S, Typpö J & Rahkonen T (2008) Effects of input routing in switched RF amplifiers. Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC) Malaga, Spain 24-25 November 2008.
- III Hietakangas S, Rautio T & Rahkonen T (2008) One GHz class E RF power amplifier for a polar transmitter. Analog Integrated Circuits and Signal Processing 54(2): 85-94.
- IV Hietakangas S & Rahkonen T (2010) Dimensioning space of a parallel tuned amplifier. NORCHIP 2010 Tampere, Finland 15-16 November 2010.
- V Hietakangas S, Typpö J & Rahkonen T (2010) Design of integrated 1.6 GHz, 2 W tuned RF power amplifier. Analog Integrated Circuits and Signal Processing 64(3): 261-270.
- VI Hietakangas S & Rahkonen T (2011) Input impedance of class E switching amplifiers. Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC) Vienna, Austria 18-19 April 2011.
- VII Hietakangas S & Rahkonen T (2012) Analysis of Class E amplifier with both Linear and Nonlinear Shunt Capacitance at Any Duty Cycle, Grading Coefficient and Supply Modulation. Analog Integrated Circuits and Signal Processing 71(2): 245-253.

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1 Introduction

1.1 Motivation and aim of the thesis

Although radio frequency (RF) power amplifiers (PA) are rather well known and thoroughly studied, there is an increasing interest towards high-efficiency switched mode PAs such as class D, E and F. These amplifiers respond to the requirement of more 'green' solutions by providing a theoretical drain efficiency of 100%, which makes all the fuss understandable, since traditional linear amplifiers achieve a maximum theoretical drain efficiency of only 50% in class A and 78% in class B. Regardless of the obvious efficiency advantage, the commercial RF amplifier products utilising switched modes seem to be missing. This eventually leads to a question: Are there some problems in designing switched mode RF amplifiers that have not been solved yet?

The aim of this thesis is to study this question by designing and implementing two amplifiers, where the main focus will be on the class E and inverse class E (E^{-1}) topologies. The design of class E amplifiers requires the analysis of drain voltage and current in the time domain. Finding the correct waveforms in analytical form is challenging and often impossible. Another complication to the analysis are the necessary conditions that ensure optimum switching and the theoretical 100% efficiency. Finally, in the third phase, one would like to calculate the proper component values for the class E amplifier. It is often this phase that moves a designer from the analytical approach to a supporter of a numerical one. And so far, we have not taken any nonidealities, the effect of feedback or even the effect of input signal into account.

Attention is also given to the stability of the amplifiers, to the modulation speed of the supply voltage and to the minimization of nonlinearities inherent to switching amplifiers. Due to the fact that high-power amplifiers require large periphery devices, a carefully designed signal routing and overall input design are important issues that are discussed. The difficulties, special features and lessons learned are written into this thesis. Hopefully, this will give some insight what a designer should and should not do.

1.2 Organisation of the thesis

The thesis is organized so that Chapter 2 reviews three switched mode amplifiers class D, E and F and takes a look at other harmonic tunings in between the traditional classes. A separate section about the supply modulation of these amplifiers is provided. Chapter 3 of the thesis takes a look at class E design principles by discussing the different analysis methods and by taking a quick glimpse to special features necessary for accurate simulations. Chapter 4 provides information about the nonlinear properties of the output circuit of class E in the presence of supply modulation. The main focus in this chapter is on the efficiency degradation due to nonlinear output capacitance, on the optimization of supply bias route and on the distortion caused by feedthrough of input signal at low supply levels. In addition, some specific design choices are considered. Chapter 5 discusses empirical findings discovered from the input side of the implemented amplifiers and gives advice how to avoid some problems found. Finally, everything is summarized and further discussed in Chapter 6.

1.3 Main contributions

The main contributions are divided into four parts. The first part is related to the design of the input of a class E power amplifier, discussed in Chapter 5 and in [II,V,VI]. It is shown that the input impedance of a switching amplifier has a heavy dependency on supply voltage caused by the Miller effect, including a strongly varying input capacitance and negative input resistance. Means for stabilization are discussed in [V] and in Section 5.3.

The second part of contributions is related to the literature review of different class E load design principles and to a small contribution to the analysis and synthesis of class E, where the nonlinear feedback capacitance has been added to the analysis in combination of both linear and nonlinear parallel output capacitance. Specific device grading can be used in the nonlinear capacitors. In addition, the tradeoff of drain voltage to drain current and back as a function duty cycle and the effect of device junction grading on peak voltage is discussed in Chapter 3. The detailed descriptions of these are found in [VII]. The design procedure and properties of a switched amplifier with an integrated parallel resonator are discussed in [V].

The third part of contributions deals with the changes of optimum class E tuning as a function of supply modulation, which are discussed in Chapter 4 and in [VII]. It will be

shown that it is possible to design the class E amplifier with different set design values for optimizing the low supply level efficiency.

The fourth part of contributions provides an improvement to the supply bias line design by introducing a combined structure of transmission line together with a small discrete inductor. The combined bias line is used in the implemented amplifier in [III] and discussed in Chapter 4.

Also other small notes will be made. These are the feedthrough of a wideband constant amplitude input signal to the output of the amplifier, discussed in Chapter 4 and the effect of device modeling uncertainties in a switch use (Chapter 6).

All the included publications are joint publications. The author of this thesis is the main author and also main researcher in all the publications. Lic.Tech. Timo Rautio was responsible for the polar transmitter measuring setup and helped in the measurements of [I] and [III]. Dr. Jukka Typpö was at that time in the Department of Electronics and Telecommunications in the Norwegian University of Science and Technology (NTNU), and helped with the Gallium arsenide (GaAs) integrated circuit (IC) design tools - he for example made a layout generator for a high- Q capacitor structure. Professor Timo Rahkonen as a supervisor gave suggestions related to circuit analysis, especially in papers [IV] and [VII].

2 High-efficiency power amplifiers

2.1 Efficiency enhancement in power amplifiers

A common goal for all high-efficiency amplifiers is to minimize the device power dissipation due to simultaneous drain (or collector) voltage and current while maintaining the wanted output power level. For a field-effect transistor (FET) this means the minimization of

$$P_{diss} = \frac{1}{T} \int_0^T I_{ds} \cdot V_{ds} dt, \quad (1)$$

while output power P_o is held constant. In switching amplifiers this is achieved by utilising the used transistor as a switch instead of as a high-impedance current source. Ideally, if a transistor is used as a switch, the output current is fully determined by the properties of the load network [1, 2]. This approach is different from other high-efficiency amplifiers such as class F [2] and class J [3], which utilise harmonic resonators or some harmonic tuning to reduce the power dissipation of a transistor that is still being used as a high-impedance current source. Thus, in classes F and J the output current is determined by the input signal, not by the load network [1, 2]. Confusingly, in reference [4] class F is considered an example of switchmode RF power amplifiers, but the reason for this is probably dependent on the viewpoint how we look at things: from the input or from the output. This is clarified more in Section 2.3.1, and in this dissertation we will use the classical categorization [1, 2].

What is essential in all high-efficiency amplifiers is the harmonic tuning of the output load. To minimize power dissipation, the second and higher harmonic terminations are dominantly made reactive, while the fundamental impedance is resistive or a combination of resistance and reactance. In some papers [5, 6], the design begins from harmonic waveforms and the required optimal harmonic impedances are given, but the actual implementation is left open. More often [7–10] the circuit topology is fixed and the high-efficiency analysis and synthesis is based on the proposed topology. Examples of these different approaches can be found in Section 2.3.3.

2.2 Switching power amplifiers

In switching amplifiers, the transistor is driven with a large input drive and this is why the device is assumed to behave as a switch. Switching amplifier topologies are often divided into two subclasses: the traditional class and the dual circuit. The difference between the two is that the voltages and currents are duals. This means that the waveforms have the same shape, but the voltage of the traditional class has the shape of a current waveform in the inverse class and vice versa. This swap from voltage to current and back is often made by changing a series resonator in the load to a parallel resonator. The dual class is sometimes denoted with extra letter I, e.g. class EI [5]. In this work, the use of mathematical inverse $^{-1}$ is adopted so that inverse class E is class E^{-1} .

A common feature to all switching circuits is the need for a good and low-ohmic, large periphery device that is capable of high output current with a decent amount of input drive and drain voltage. This is illustrated in Fig. 1, in which a transistor on-state current curve nearing the ideal shape is provided together with regions where voltage switching and current switching occur. In an ideal case the rising slope would be straight up until some very high current level and thus, the current should not be limited by the device to some low level, as shown in three lines in the figure. And, of course, switching from on to off and vice versa should happen very quickly.

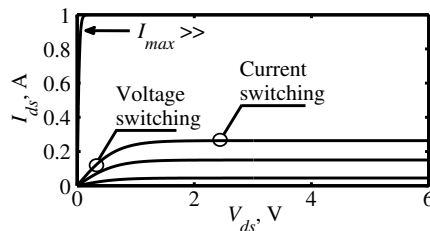


Fig 1. Voltage and current switching in the I_{ds}'/V_{ds}' curves.

2.2.1 Class D, D^{-1}

According to [2], class D amplifiers (sometimes referred to as voltage-mode class D, VMCD [11]) were first studied by Baxandall in 1959 [7]. In class D a pair of transistors is used as switches, where the on-time between the transistors is phase shifted by 180 degrees. The resulting output is a square wave voltage, also referred to as a

voltage-switching class D [2], where the output current is a series of half-sinewave pulses. The waveforms in a dual structure, referred to as the current-switching class D [2], current-mode class D (CMCD) [11, 12] or D^{-1} [13], are duals to the voltage-switching class D. The output is a square wave current, whereas the output voltage is a series of half sinewave pulses [2]. The voltage waveforms of both class D and D^{-1} are shown in Figs. 2(a) and 2(b), and the currents are plotted in Figs. 2(c) and 2(d), respectively. Note that the waves in class D are normalised to a supply and load of unity [2], whereas in class D^{-1} the levels are for the ideal theory [4, 12]. The waves are for illustration only and not for magnitude comparison purposes. The output resonator in class D is a series

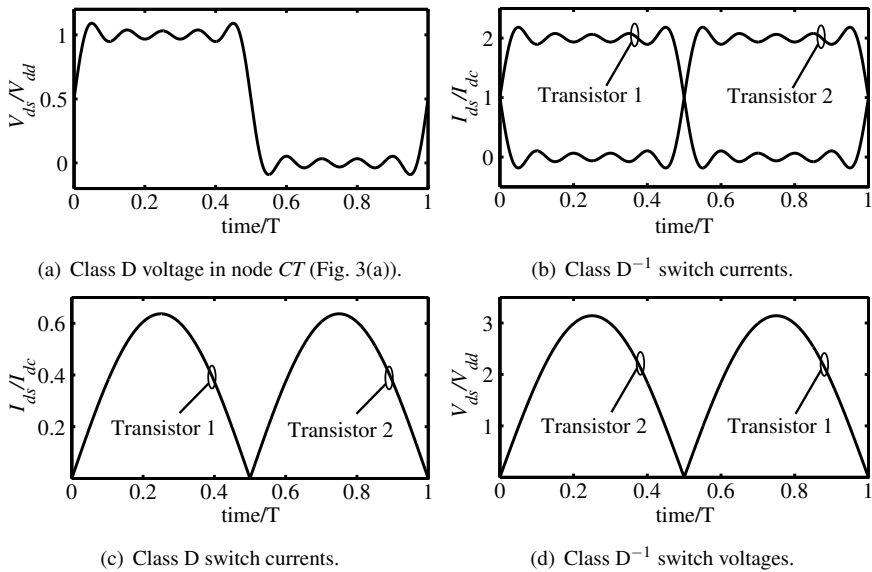


Fig 2. Class D and D^{-1} voltage and current waveforms.

resonator, whereas the dual topology uses a parallel resonator. The output resonator response to the train of output pulses defines the output current and the resonator is tuned properly to the fundamental frequency to make the output ideally a pure sinusoid [2]. The schematics of class D and D^{-1} are shown in Fig. 3(a) and 3(b), respectively.

The efficiency of the class D amplifier is reduced in high operating frequencies due to device output parasitic capacitances [8]. The parasitic capacitances store energy during device off-phase and dissipate the charge during the next on-phase [4]. This power dissipation can be minimized by taking the output capacitances into account

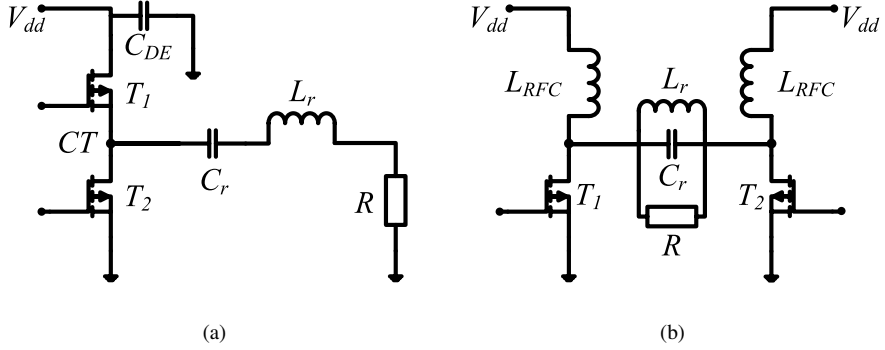


Fig 3. High-efficiency a) class D amplifier, revised from [2] and b) class D^{-1} amplifier (symmetrical), revised from [12].

when designing the load of the class D amplifier. Such an amplifier is called class DE amplifier, which is introduced in Section 2.2.3.

2.2.2 Class E, E^{-1}

The large scale introduction of the class E amplifier happened in 1975 by Sokals [1] and analytical design equations were provided by Raab [9] in 1977. The idea behind class E is that the passive output load is tuned to achieve an optimal transient response to the switching operation of the transistor [1], thus ideally reducing the voltage-current product to zero.

The class E load network transient response should in an optimum case prevent drain voltage when the transistor is on, decrease it to zero before the transistor turns on and provide a zero slope when the transistor turns on [9]. Mathematically the same is stated for class E with duty cycle

$$V_{ds}(0 \rightarrow D2\pi) = 0, \quad (2)$$

$$V_{ds}(2\pi) = 0, \quad (3)$$

$$\frac{\partial V_{ds}}{\partial \theta}(2\pi) = 0, \quad (4)$$

where the transistor is on from 0 to $D2\pi$ and off from $D2\pi$ to 2π ($0 < D < 1$). If one or several of the requirements (2), (3) and (4) are not met, then the class E amplifier is called suboptimum class E [9] amplifier. Suboptimum drain voltage waveform is shown in Fig. 4 together with the effect of load component variations. Load components are R , C_o , C_r , L_r and L_X , that are resistive load, parallel output capacitance, series resonant

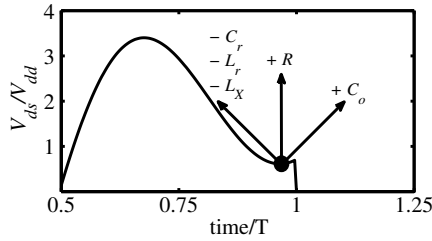


Fig 4. Suboptimum drain voltage waveform and the effect of component tuning. Revised from [14].

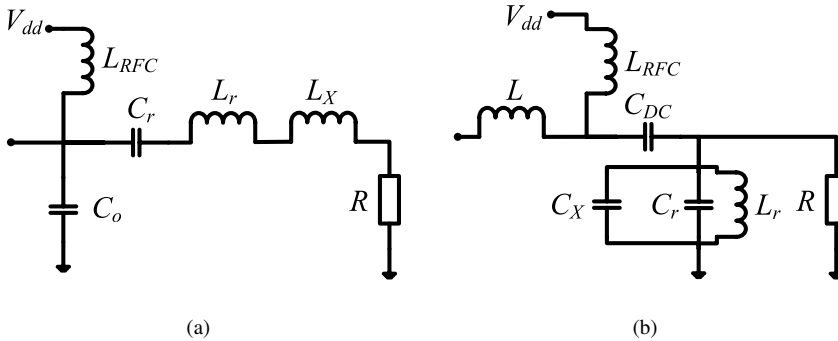


Fig 5. High-efficiency a) class E topology, revised from [9] and b) class E⁻¹ topology, revised from [10].

capacitor, series resonant inductor and series tuning inductor, respectively. The class E circuit topology is shown in Fig. 5(a).

The first requirement, (2) is in practice difficult to achieve, since transistors do have a nonzero on-state resistance R_{on} . This resistance causes the drain voltage to rise during the on-period and violate requirement (2). In many papers, only requirements (3) and (4) are used. These are optimum waveform requirements for class E and they are sometimes called zero voltage switching (ZVS) or zero derivative switching (ZDS) as in [15]. These class E optimum waveforms are shown in Fig. 6(a). The meaning of (3) and (4) is to minimize the voltage-current product during off-period and to eliminate off-to-on transistor power loss [16]. In addition, requirement (4) makes the amplifier more tolerant against component variations and timing errors [17]. However, here we will use a more accurate definition due to the otherwise overlapping description of ZDS between class E and inverse class E (from now on E and E⁻¹). Accurate definitions for class E and E⁻¹ are: zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) in classical class E, shown in Fig. 6(a) and zero current switching (ZCS) and

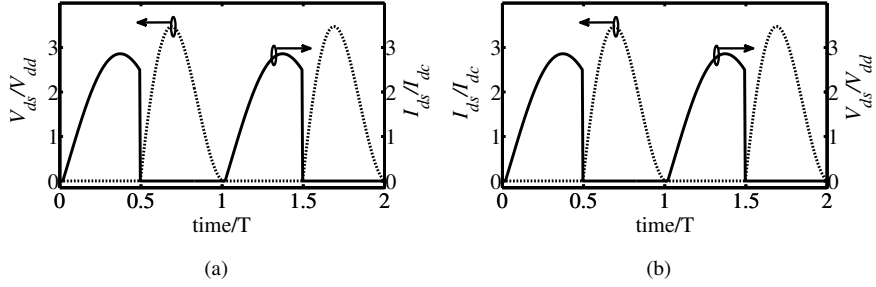


Fig 6. a) Series tuned class E drain current and voltage and b) parallel tuned class E drain current and voltage.

zero current derivative switching (ZCDS) in the case of E^{-1} in Fig. 6(b) [18]. These two different requirements and resulting waveforms are again duals to each other. Both switching requirements lead to a situation, where the voltage-current product is zero, according to (1). ZVDS in (4) and ZCDS require that the drain voltage or current comes smoothly down to zero before the transistor starts to conduct (ZVDS) or opens. The ZVS/ZVDS requirement has been the goal in [III] and the ZCS/ZCDS in the design of the amplifier in [V].

The requirement of ZVDS and ZVCS leads to different topological structures. The classic class E is realized with an optimally tuned series resonator [9], whereas one example of E^{-1} utilises a parallel resonator accompanied with a series inductive component [10]. There are also other realizations of E^{-1} [9] and a further developed circuit of parallel resonator topology that actually utilises ZVS and ZVDS instead of ZCS and ZCDS [18]. The class E and E^{-1} topologies were shown in Fig. 5(a) and 5(b), respectively.

The choice of class E topology depends mainly on the device drain (collector) voltage limits. The class E^{-1} swaps the output waveforms from voltage to current and vice versa, which results in a considerably lower drain peak voltage ($2.86 \cdot V_{dd}$, ideal circuit, high- Q , 50%/50% duty cycle calculated from [10]) than in classic class E, where the drain peak voltage rises to $3.56 \cdot V_{dd}$ [1]. On the other hand, the peak currents through the device class E^{-1} are $3.56 \cdot I_{dc}$ [10] compared to class E peak current, $2.86 \cdot I_{dc}$ [1]. The increase of the peak current in class E^{-1} requires higher maximum drain current and larger device size. The increase in the device periphery is somewhat problematic since the output capacitance of the device increases and this is not taken into account by the traditional analysis [10]. It is, however, suggested that this is not a major problem if the device output capacitance remains below 0.7 pF in an amplifier operating at 2.5 GHz

and delivering 0.5 W [10]. This gives a small indication about the achievable power levels, since the device size and device technology is directly limited by the output capacitance. However, in [18] the output capacitance and bondwire inductance have been taken into account using ZVS and ZVDS. According to the same reference, the peak drain voltage is higher and current is lower than in the traditional class E case, at $3.63 \cdot V_{dd}$ and $2.697 \cdot I_{dc}$, respectively.

The choice of class E topology also depends on the purpose and implementation strategy. The class E^{-1} is better suited for low power monolithic microwave integrated circuits (MMIC) since the inductors in the design are considerably smaller than in an equivalent class E implementation [10]. This helps to reduce both the necessary area of the MMIC design and the equivalent series resistance (ESR).

Classic class E utilises the transistor output capacitance as part of the load transient network, which is a considerable benefit when compared with the situation in class D, where the transistor output capacitance causes power losses in the switching operation [4]. However, there is a new approach where the class E load principles are used in class D [8]. This issue will be discussed in Section 2.2.3.

After the first introduction of class E in 1975, the analyses have experienced a series of different additions, improvements and approximations. For example, the improvements may be the approximations of power losses due to parasitics such as saturation voltage or saturation resistance, current transition time and device series inductance [19]. There are other nuances that have been discussed as well, such as circuit variations [20], the additions of nonlinear components [21], transmission line approaches [22], the inclusions of non-infinite RF-bias choke [23, 24], the effects of collector fall time [16, 25], losses as a function of duty cycle [26] and discussion about harmonics in the output [27]. Further, there are studies about design variables such as duty cycle D [9], loaded quality factor Q_l [28] and the combined effect of nonlinear feedback capacitance and nonlinear parallel capacitance [VII]. The closer review on different analysis methods is found in Section 3.1.

2.2.3 Class DE

When compared to class E at lower frequencies, the class D amplifier provides lower conduction losses and higher power output capability [29]. However, at higher operating frequencies, the device output parasitic capacitances of class D reduce the efficiency by causing power dissipation [2, 8, 29]. This dissipation can be minimized by the use of

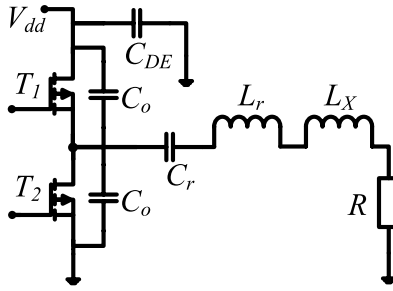
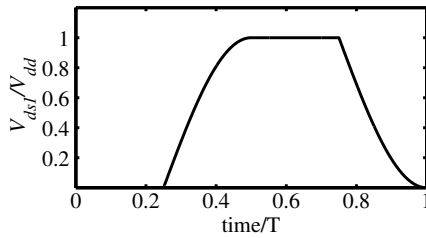


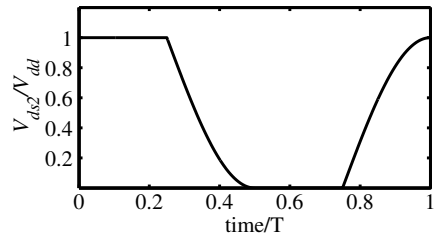
Fig 7. High-efficiency class DE amplifier. Revised from [8].

Table 1. Class DE drive sequence [8].

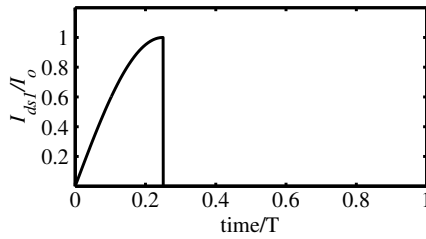
Transistor	$0-\frac{\pi}{2}$	$\frac{\pi}{2}-\pi$	$\pi-\frac{3\pi}{2}$	2π
$T1$	ON	OFF	OFF	OFF
$T2$	OFF	OFF	ON	OFF



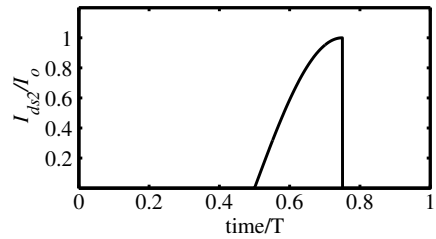
(a) Class DE transistor 1 voltage.



(b) Class DE transistor 2 voltage.



(c) Class DE transistor 1 current.



(d) Class DE transistor 2 currents.

Fig 8. Class DE voltage and current waveforms. Revised from [8].

'dead time', where the switches are turned on and off with a slight delay in between [8, 29], meaning that the duty cycle of each switch is less than 0.5 [29]. This class DE amplifier attempts to minimize the power dissipation by utilising a class E type load network, where output capacitances are part of the output load. Similarly, the class DE load has an additional offset reactance in the series resonant filter, shown in Fig. 7, similar to class E amplifier [8, 29].

A special case of Class DE is driven with a duty ratio of 25%, where the on-off sequence is written in Table 1, showing the use of dead time between conductive periods [8]. The output is roughly a combination of class D voltage waveforms and class E current waveforms, as shown in Fig. 8. The class DE amplifier utilises ZVS and ZVDS [8, 29], which is evident from the drain current and voltage waveforms. Albulut [29] extends the class DE analysis to accompany finite output Q and provides curves explaining the dependence on Q and duty cycle D .

2.3 Other high-efficiency power amplifiers

Other modes of high-efficiency operation rely similarly on a specific tuning of output loads, but differ in the sense that the transistor is operating as a high-impedance current source instead of a switch.

2.3.1 Class F, F^{-1}

In class F (see Fig. 9) the transistor is operated as a distorting high-impedance current source, but on the drain side the amplifier is ideally producing a train of squarewave type of voltage pulses or as in class F^{-1} , a train of half sinusoid pulses. This series of output pulses is typical of switching amplifiers. Therefore, referring to class F/ F^{-1} as one example of switch mode amplifiers is not exactly wrong [4], although the device itself is not used as a switch.

The reduction in P_{diss} (1) is achieved in two ways: First, the classical Class F utilises near square wave drain voltage, while the drain current is a half sine wave, as shown in Fig. 10(a). The second approach is inverse class F (F^{-1}), where the drain current has almost square wave shape, while the collector voltage resembles a half sinusoid, as shown in Fig. 10(b). To shape the drain voltage closer to square wave and current pulse towards a half sine wave in class F, the load reactances at odd harmonics have to be high, whereas the reactances at even harmonics are low. In the inverse class F, the requirement

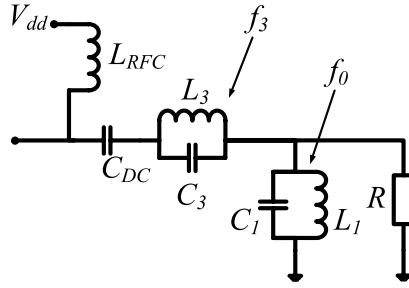


Fig 9. High-efficiency class F amplifier. Revised from [30].

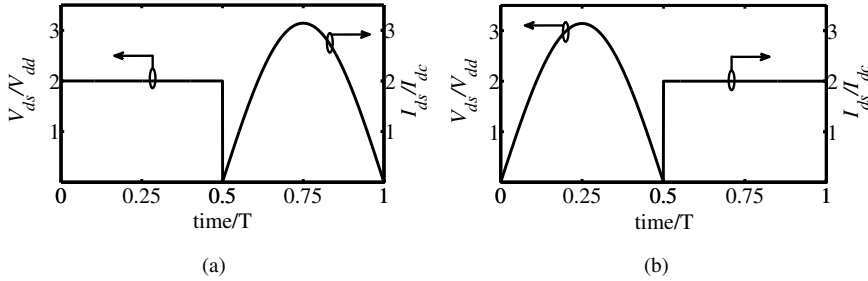


Fig 10. a) Class F drain voltage and current and b) Class F⁻¹ drain voltage and current waveforms.

for load reactances at odd and even harmonics is reversed: at odd harmonics reactances have to be low while at even harmonics they have to be high [4, 5, 30]. These reactances are achieved by tuning resonators to one or several harmonic frequencies. Ideally, odd harmonic series tank resonators are used to shape the drain voltage waveform towards square wave in class F and even harmonic series tank resonators in class F⁻¹ to shape the drain current towards square wave [4]. Other topologies are also possible, as shown in reference [31], where class F interstage topologies with a simplified synthesis approach are discussed.

It must be noted that it is necessary to drive the device out of linear region so that the necessary harmonic components are generated at the drain in order to achieve the wanted drain waveforms [5]. In addition, filtering at the fundamental frequency is used to make the output a pure sinusoid [2, 30].

2.3.2 Classes E/F and FE

Class E/F [32] amplifier attempts to combine the ability of class E to incorporate the device parasitic output capacitance as part of the wanted load network with inverse class F's lower peak currents and voltages. In other words, it is a combination of class E and class F^{-1} tunings, fulfilling ZVS as in class E. The tuning is done by a similar inductive fundamental load as in class E. Table 2 shows some harmonic impedance combinations in order to achieve the wanted operation, where the Z_{Co} is the impedance of the parallel output capacitance.

Table 2. Class E/F harmonic tunings [32].

Class	fund.	2nd harm.	3rd harm.	4th harm.	5th harm.
E/F ₃	$Z_{Co} \parallel (jX + R)$	Z_{Co}	short	Z_{Co}	Z_{Co}
E/F _{2,3}	$Z_{Co} \parallel (jX + R)$	open	short	Z_{Co}	Z_{Co}
E/F _{2,4}	$Z_{Co} \parallel (jX + R)$	open	Z_{Co}	open	Z_{Co}
E/F _{3,4}	$Z_{Co} \parallel (jX + R)$	Z_{Co}	short	open	Z_{Co}

These tuning combinations generally provide somewhat lower peak voltages and currents, which helps in reducing the losses of the amplifier. Further, a properly tuned class E/F amplifier can tolerate higher values of parallel device output capacitance than class E, but the gain of these amplifiers is usually lower [32].

A similar approach called class FE is discussed by Grebennikov [33]. The basis of the amplifier is in principle the same: Class E switching conditions are combined with the class F amplifier. However, the direction of the tuning principle is different, from class F towards class E, not Class E added with class F^{-1} . The idea behind class FE is the same as that of E/F: to provide ZVS with lower peak voltages. The implementation in [33] is done with the help of a quarter-wave transmission line and dead time in switching, somewhat like in the class DE amplifier (see Table 1). The use of dead time leads directly to duty cycles less than 0.5. The optimum load for the class FE amplifier is shown in Table 3.

Table 3. Class FE harmonic tuning with a quarter-wave transmission line [33].

Class	fund.	2nd harm.	3rd harm.	4th harm.	5th harm.
FE	$Z_{Co} \parallel (jX + R)$	short	Z_{Co}	short	Z_{Co}

The actual implementations of class FE are with parallel or series quarter-wave transmission lines. The first one is topologically close to class E amplifier with a $\lambda/4$ transmission line connected to supply, while the latter is topologically close to the inverse class E amplifier with a $\lambda/4$ series transmission line added between the drain and load. Further, a combination of class F discrete component resonating supply line and class E load may be used in creating a class FE amplifier [33].

2.3.3 Harmonic tuning

The class E, F and other tuned amplifiers can be designed with a finite number of known harmonic load impedances. This is useful, for example, when the amplifier is designed with transmission lines with a limited amount of traps [5] or if one does not want to be limited to only one circuit realization. One of the key findings in [5] was that the maximum efficiency and the power output capability of a tuned amplifier are directly dependent on the used amount of harmonics in the design process. As a special example from [5] we can take the second harmonic tuned class E amplifier, which uses the fundamental load of

$$Z_1 = R_1 + jR_1. \quad (5)$$

This 45° phase shift in the fundamental frequency is the first requirement since the second-harmonic components have to be at 90° phase shift (in phase quadrature) in order to eliminate power generation in the second harmonic [5]. The phase quadrature requirement causes peaking in the drain voltage waveform, which is an issue that can be found also in class J drain waveforms in Fig. 11(b). For comparison, almost optimal class B waveforms are shown in Fig. 11(a).

Second, to keep the same relative levels of second harmonic-to-fundamental in the current waveform as in the voltage waveform, it is required according to [5], that

$$X_2 = -j1.414R_1. \quad (6)$$

These two requirements ideally guarantee efficiency of over 70% by shifting the phase between the voltage and current waveforms and thus by reducing the voltage-current product in (1). It has to be noted that [5] does not give any comment on the realization of the loads but merely gives harmonic impedances to approach.

With a similar harmonic impedance approach as previously, a specific example of second harmonic tuned amplifier called Class J is reviewed in [6]. Class J is essentially

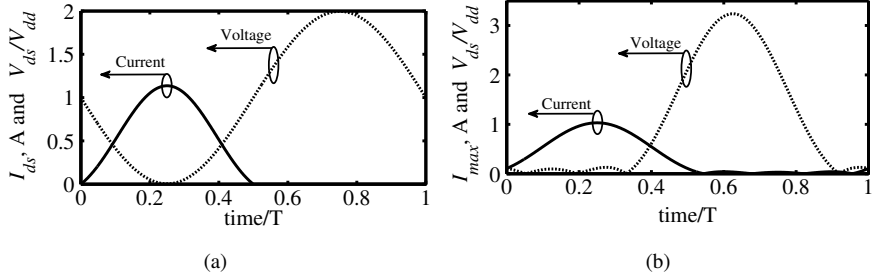


Fig 11. a) Class B drain voltage and current and b) Class J drain voltage and current waveforms.

a well-tuned class AB or B amplifier, which utilises a transistor with a specific output capacitance when compared with the fundamental frequency loadline resistance [6, 34]. The drain capacitance acts as specific reactive harmonic termination at the second harmonic, which according to [6] is ideally

$$Z_{2f_o} = 0 - j\frac{3\pi}{8}R_L \sim -j1.178 \cdot R_L \quad (7)$$

and the fundamental load is

$$Z_{f_o} = R_L + jR_L. \quad (8)$$

This turns the drain voltage into a non-sinusoidal pulse with considerable second harmonic content, as shown in Fig. 11(b). Higher harmonics than the second are considered zero because of the large output capacitance of the devices [34]. Further, the proposed low pass matching circuit is tuned to be reactive at the fundamental frequency, as shown in (8). A conflicting statement to the previous is made in [35], where the optimal low pass tuned class B topology is claimed to be the actual class J amplifier topology, rather than some specially defined harmonic impedance tuning.

The main points of class J are to avoid the use of harmonic traps and to reach a capacitive harmonic tuning, where the second harmonic output current and voltage are in phase quadrature [3]. The resultant voltage waveform overlaps with the current wave only partially and thus decreases the dissipated power [6]. The wanted target impedances for class J are shown in (7), (8) and in reference [6], although some third harmonic load-pull tuning, together with class C biasing was applied in [6] into the design process for the optimization of efficiency. The extra benefit of this approach is the extended operation bandwidth of the amplifier [3, 6], due to the lack of narrowband harmonic traps.

According to [36] class J has been extended to multiple sets of different drain waveforms, which are all capable of reaching class B efficiency level with differently tuned reactive load circuits. In addition, a new class notation seems to be introduced in [36], class J^* , which utilises conjugate reactances when compared to class J at the fundamental and at the second harmonic. In [37], a new approach by Cripps [36] is utilised and thus, improvement is achieved to the work previously done by the same authors [6].

The increased interest for classes J and J^* is due to the relatively large operating bandwidths available (over 50%) while maintaining efficiency levels above 60% [6, 37]. Recently, the class J analysis has been experimentally extended to cover the effects of nonlinear output capacitance to the load network design in [34], where it was noted that even higher output powers and efficiencies are available due to the capacitance nonlinearity. The nonlinear capacitance can replace the necessary series fundamental inductive tuning by producing the extra second harmonic necessary for modifying the drain voltage waveform and thus, improves efficiency and available output power [34]. In the same reference, the partial resemblance of class J with class F^{-1} became more obvious due to the second harmonic peaking of the drain waveform.

There has been discussion about the similarity of class E [5] and class JJ^* [3, 6, 37] because the approach and impedance tuning of the output network are very close to each other. The class J idea of reactive fundamental load [6] is close to the requirement in series tuned class E [5, 9], which is by no means a key difference between other classes, as stated in [6]. Further, the requirement of the second harmonic current and voltage being in phase quadrature at the drain of class J, while the fundamental impedance is phase shifted by 45° , are both actually the same as stated in [5] for the second harmonic tuned class E. In an ideal sense it is true, that there is a difference in the input signal between classes J and E (high-impedance current source vs. switch) and therefore in the power control between the two. Hence, class J falls into the category of a well-tuned second harmonic tuned class B amplifier. Regardless of the similarity of class E, the class J concept has received interest also by other researchers [34, 35].

Due to the same fundamental loading, the class E and class J amplifiers have similar impedance gyration applied to the input of the amplifiers. In [VI] it was noted that due to the phase shift in device gain, the input impedance experiences a considerable negative resistance, which can be detrimental to the stability of the amplifier. In a class E amplifier, this negative resistance varies with the supply level and causes an additional

concern in the design of supply modulated transmitters, such as envelope elimination and restoration systems. This issue is discussed in Section 5.1 and [VI].

2.3.4 Class C-E

The class C-E amplifier is between class C and class E operation in a class E topology, shown in Fig. 5(a). The analysis of class C-E originates from class E topology, but the output circuit is tuned somewhat differently. Also, the operation of the transistor is partially different, where the transistor operates part time as a switch and the other part as high impedance current source. The output tuning is chosen delicately by

$$q = \frac{\omega(L_r + L_X)}{R} - \frac{1}{\omega C_r R}, \quad (9)$$

$$p = \omega C_o R, \quad (10)$$

where L_r , L_X and C_r are the components of the class E series resonant filter [38]. R is the resistive load and C_o is the parallel output capacitance. When the impedance of the output network at the fundamental frequency is purely resistive ($Z_1 = \text{real}$) and the value of q is three or larger, the amplifier is a class C amplifier, as illustrated in Fig. 12. However, if q is lower than three and both q and p differ from the values of the optimum class E case ($q = 1.204$, $p = 0.1971$ and $Q = 10$), the amplifier is then a class C-E amplifier [38]. The optimum class E tuning depends on the Q value and in Fig. 12, the optimum class E line is plotted where the Q value is varied from 1 [38] to infinity [5, 9]. The class C-E amplifier trades some of the peak efficiency to the capability to

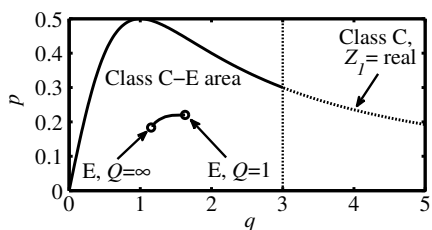


Fig 12. Normalized output loads of class C, C-E and E. Revised from [38].

operate at higher frequencies. The maximum frequency of operation can be as high as 16 times the maximum frequency of a class E amplifier while the maximum efficiency lies between 77 and 95% [38]. A similar study for parallel tuned output network can be found in [IV], where the amplifier implemented in [V] was analysed.

2.4 Supply modulation (EER/ET)

Envelope elimination and restoration (EER) was first introduced by Kahn in 1952 [39] as one solution for single-sideband transmission. This technique is adopted by high-efficiency amplifier community both as a solution to restore amplitude variations in the output of a switching amplifier and as a possibility to use highly nonlinear amplifiers to produce linear amplification with amplifiers such as class C, D, E and F [40]. The basic signal flow is shown in Fig. 13(a), where the phase and amplitude information are combined in a switching PA [40, 41]. The modern addition to this is digitally controlled signal generation, which allows the user to accompany digital predistortion for correcting the nonlinearities generating in the amplifier itself [42]. This computer controlled EER is called polar modulation [43, 44], and the block diagram of such a transmitter is in Fig. 13(c) [42, 43].

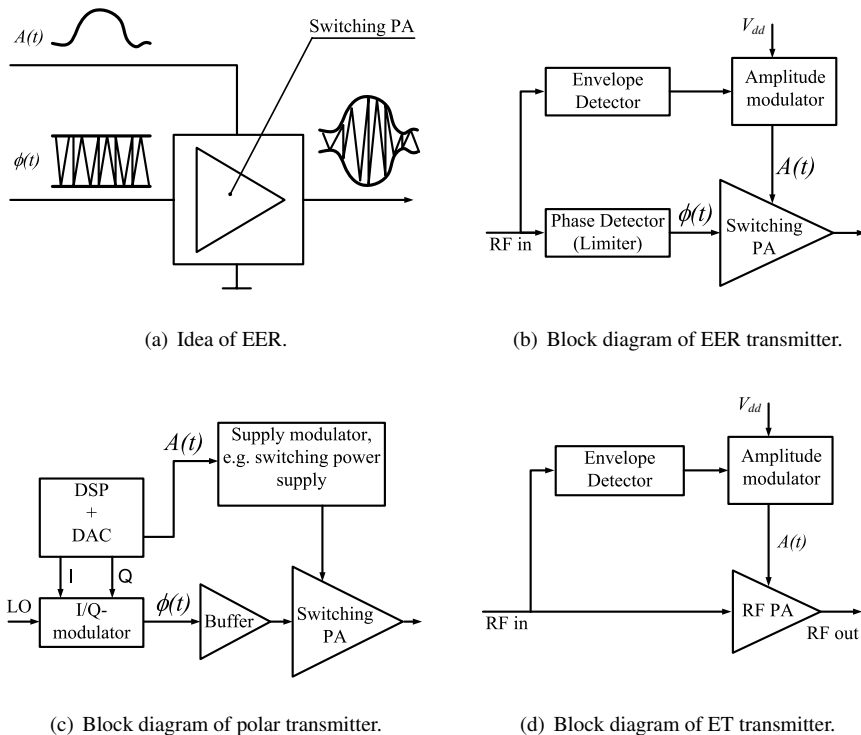


Fig 13. High-efficiency power amplifiers.

The basic principle of EER is shown in Fig. 13(b), where first the amplitude and phase information are extracted with an envelope detector and a limiter, respectively [41, 44]. Then the amplitude limited phase signal is passed to the gate of a switching class E amplifier, for example. Further, the amplitude information of the original signal is passed on to an amplitude modulator that modulates the supply voltage of the switching PA. If the phase and amplitude information is combined with correct timing in the PA, the result in the output is an amplified replica of the original signal.

In EER, the linearity of the output signal is not dependent on the linearity of the device itself if the device is capable of delivering the necessary current. Instead, the linearity is dependent on the bandwidth of the modulator (and thus the envelope path) and the differential delay between the envelope and phase paths [40]. The correct timing of phase and amplitude routes is important in EER, since timing errors lead immediately to increased intermodulation distortion (IMD) levels [41], which makes the detection of the correct transmitted signal difficult. According to [40], the envelope and phase path bandwidths have to be at least the width of RF bandwidth (B_{RF}) and $3.5 \cdot B_{RF}$, respectively. It is also suggested in [43] that for 16.6 MHz signal bandwidth it is required to have at least 45 MHz bandwidth both in envelope and phase paths to achieve less than 2% error vector magnitude (EVM). In addition, the modulation speed of the supply line is dependent on the size of drain bias inductor, which is an issue that is discussed by comparing two different class E topologies in [45], by deriving equations to the calculation of IMD products due to the bias inductor with a single pole low pass (LP) filter in [46] and by deriving the bias frequency response with a second order LP filter in [47]. A special compromise bias topology is used in [III] in order to improve modulation speed, which is discussed further in Section 4.2.2.

If the device used is unable to deliver enough current, the supply to amplitude modulation, V_{dd}/AM , is a curved line in the highest supply levels, and this nonlinearity appears as distortion in the output of the amplifier. This issue is discussed in [III]. An additional distortion product comes from the feedthrough of the strong and constant envelope input signal to the output of the amplifier, which is discussed in [48, 49], in [I] and in [III]. When the supply voltage is low in EER or polar transmitter, the feedthrough of the amplitude limited input signal causes a wideband distortion in the output of the amplifier [42]. Feedthrough can be minimized by driver bias modulation [49] and by predistortion [42, 50]. The issue of feedthrough is explained at transistor level in Chapter 4 and in [I]. There is still one possible source of nonlinearity, which is the input impedance variation according to supply voltage discussed in [VI]. The impedance

variations can change the input swing, which in the worst case can change the transistor to behave as a high impedance current source rather than a switch. This can lead to insufficient output current, distorting the V_{dd}/AM behaviour of the amplifier.

Envelope tracking (ET, Fig. 13(d)) differs from EER in a sense that the gate signal includes both the amplitude modulation as well as phase modulation [42, 50]. In ET the input signal envelope information is also extracted and passed onto the supply modulator, which in turn will keep the linear PA (e.g. class A, AB or B) near or at a compression point. This approach will ensure that the linear PA is operating with good efficiency at all signal levels [51].

The input and supply line timing is not so critical in special cases of ET that do not exactly follow the envelope of the input signal. The supply modulation may be changing rather slowly and thus, only making a crude approximation by leaving some space between the inserted supply voltage and voltage where the transistor would be in compression. Further, the ET can be used at the highest voltage levels only by leaving a bias voltage minimum [3, 50]. However, the efficiency of these two systems is degraded in high peak-to-average ratio modulations (PAR) when compared to fast following ET systems [42, 50]. ET systems that precisely follow the chosen compression point causes the design requirements of the supply modulator to be more stringent than in slowly following ET systems. The supply dependent gain will also cause considerable variations in amplitude-to-amplitude modulation (AM/AM) and amplitude-to-phase modulation (AM/PM) in a fast following ET system [50]. In ET the input signal contains both phase and amplitude information, and the feedthrough of the input signal is not an issue here as it is in the EER system, since the input drive goes low when the output is low [42]. Due to the lack of input limiter and thus, the narrower bandwidth in the input signal, the design requirements of the input path are more relaxed than in EER.

There are also digitally controlled modulation approaches [52, 53], which utilise either a combination of digitally controlled supply modulation and digitally controlled array of tail current sources [52] or only a digitally controlled array of gain cells [53]. The advantage is that when amplitude modulation in the output can be done with the help of the gain cells or current sources, this avoids the use of bandwidth limited supply modulators and improves power control dynamic range [52, 53]. The additional supply modulation in [52] is used to improve low output level efficiency and in the digitally controlled case, the power control rate is a few kilohertz and more approximate (5-bit) than in envelope modulation, making the use of a highly efficient switching regulator possible [52].

3 Design principles of class E amplifiers

3.1 Objectives and categorizations

The class E analysis attempts to fulfil time domain ZVS in (3) and ZVDS in (4) simultaneously. Essentially, this means that the switch voltage v_s and switch current i_s waveforms have to be found somehow before we can utilise the optimum conditions of class E. Finding the appropriate expression for v_s and i_s proves to be one of the most difficult processes in the analysis [17]. The second part of the class E problem is the synthesis; how can we choose a combination of correct circuit components, whose transient response fulfils the wanted waveforms and thus, the requirement of equations (3) and (4)? Sometimes the analysis leads to fully analytic design equations that can be used to solve optimum class E component values. More often this is not the case and we have to rely on numerical calculation in order to find the correct component values or even v_s/i_s waveforms for that matter. One example of class E analysis and synthesis using the numerical approach is found in [VII].

The main methods for finding v_s and i_s in the case of classical class E with series resonator and parallel output capacitor can be divided roughly to two categories: High- Q and low- Q (finite Q) analyses. Although the division of analyses seems simple, a great deal of effort has been used in deriving class E design equations that accommodate device nonidealities, finite RF-choke, parasitic resistances, etc. This makes the separation of approaches somewhat difficult since some approaches cannot include some nonidealities while another approach can.

A totally different separator could be used to categorize the main methods for finding v_s and i_s ; the use of linear or nonlinear parallel capacitance C_o in the output circuit. This is due to the fact that the parallel capacitance nonlinearity affects the drain voltage. Finding waveforms and component values to the case with linear capacitance are relatively straightforward in a high- Q case, since the drain waveforms and component equations have an analytic solution [9]. The only case when analytic solution is found in the nonlinear case is when the output capacitance is nonlinear with device pn grading coefficient of abrupt junction (M is 0.5) according to the capacitance nonlinearity model

$$C_o = \frac{C_{j0}}{\left(1 + \frac{v_s}{V_{bi}}\right)^M}, \quad (11)$$

where v_s is the voltage over the capacitance, V_{bi} is built-in potential, C_{j0} is capacitance at zero bias voltage and M is the grading coefficient of the pn-junction. Otherwise, if M differs from 0.5 or output capacitance is a combination of linear and nonlinear capacitances, the solution of the drain voltage waveform becomes numerical.

3.2 Obtaining design equations

Time domain analyses contain roughly four different approaches: classic high- Q equations [1, 2, 9, 21, 23, 24, 54, 55], Laplace analysis [28, 56], other low- Q equations [5, 14, 57, 58] and State-Space analyses [17, 59, 60]. As stated before, the first thing to do is to solve the drain voltage and current waveforms and then solve output components with the requirement of ZVS in (3) and ZVDS in (4). When waveforms are found, the equations to find optimum circuit components are to be solved.

3.2.1 Classical class E design equations

The classic case of the time domain analysis of a class E load network relies on the assumption that the filter Q value is sufficiently high [1, 2, 9, 21, 23, 24, 54, 55] so that the only spectral component appearing in the output is the fundamental tone or wanted harmonic tone if class E is used as a frequency multiplier [23]. The approaches proposed in [1, 2, 9, 23, 24] consider linear output capacitance. In the first analysis and synthesis in [9], the equations for waveforms and component calculations remain analytical. However, even the introduction of a finite bias inductor [23] leads to lengthy, yet still analytical waveform equations and in the end, an iterative component calculation process is needed.

High- Q analysis is used to derive optimum class E design values in the case of nonlinear output capacitance in e.g. [21, 54, 55], where Chudobiak [21] was the first one to derive equations to a case where output capacitance has an abrupt pn junction grading ($M = 0.5$) according to (11). This leads to an analytical solution both in terms of waveforms and component values, with the limitation of 50%/50% pulse width. Alinikula [54] extended the analysis to cases when M was 0.5/0.67/0.75, but this leads to the use of numerical methods in order to calculate the DC drain voltage. Suetsugu [55] derived class E design equations for a combination of linear and nonlinear output capacitance when the nonlinear part has an abrupt pn junction grading. Further, the combination of linear and nonlinear capacitance forces the calculation of drain DC

value to be numerical in nature. As it seems, it is difficult or even impossible to achieve analytical high- Q design equations to any other case than fully linear output capacitance or fully nonlinear output capacitance with an abrupt pn junction.

Many of the above analyses [1, 2, 9, 21, 54, 55] assume the DC feed to be a large inductor so that the inductor behaves as a current source. In practice, a large choke or 10 times larger impedance than the parallel capacitance [61] is difficult to implement and it reduces the modulation bandwidth of the supply route. Zulinski and Steadman [23] extended the high- Q class E equations to both amplifiers and frequency multipliers with linear output capacitance by taking into account the finite DC feed inductance L_{RFC} . They also found out that class E designs can be done with higher values of parallel capacitance (larger than twice the original size) due to the compensating effect of the parallel finite bias inductor. Further, the output power capability can be increased from the values achievable with a large DC feed inductor [23]. Acar [24] takes the finite DC-feed inductance and class E parallel capacitance into account as one design parameter. Interestingly, with a certain combination of duty cycle and DC-feed inductor or parallel capacitor, the size of the parallel capacitor could be increased up to 4.2 times larger than in the traditional case with a decreased peak drain voltage. These enable wider transistors with lower breakdown voltages to be used in class E [24].

3.2.2 Laplace analysis

There is a rising demand for higher operating bandwidths, which is in conflict with the classic high loaded Q class E analysis. Lower output circuit loaded Q offers lower power losses in the passive circuitry together with the wider operation bandwidth [16, 61]. Further, low loaded Q ensures that optimum operation does not easily change with frequency [16]. It is shown that by designing a class E amplifier with a loaded Q value below 10, over 10% design value differences can occur [28] when the high- Q equations are utilised and some references [62] imply that it is necessary to have loaded Q value of over to 20 keep design errors small.

Laplace transformation offers an easy possibility to avoid the single-tone analysis and the necessity of infinite Q . In addition, a fixed value of D can be avoided in the analysis and therefore, the Laplace approach has been used e.g. by Kazimierczuk [28] and Smith [56]. Kazimierczuk [28] uses Laplace transform to achieve analytical design equations to any Q , any duty cycle and large L_{RFC} , while Smith's analysis [56] extends to cover finite L_{RFC} .

While the transformation from s-domain to the time domain can help us solve the low loaded Q class E operation, it is seen at Table 4, that in [28] and [56] losses in the class E load network have not been considered. Indeed, it is also mentioned in [17] that analytical inverse Laplace transformation becomes difficult when the series resistances of coils are introduced, and therefore numerical analysis is the only option. The numerical approach has been used in two occasions by Avratoglou [62, 63], but he did not include any other parasitic resistances except the device on resistance in [63]. It should be stated that the addition of resistances should not pose a problem in Laplace analysis, but rather, the problems arise from the synthesis part. The use of Laplace transformation results in a linear set of equations for solving the waveforms. Yet, solving the component values from the ZVS and ZVDS conditions results in a group of nonlinear equations that needs to be solved numerically, as stated in [63].

Another issue is the simplifying fact of Laplace: linear lumped components. It is therefore not possible to accompany any device or component nonlinearity in the analysis and thus, in the synthesis. As a result, the fact is that no output capacitance nonlinearity or other nonlinearity is discussed in the papers that have used the Laplace method, which is evident from Table 4. Further, Laplace analyses of class E amplifiers utilising transmission lines seem to be missing.

3.2.3 Other low- Q methods and cases

Since the series output resonator loaded Q is a value chosen by the designer to accommodate bandwidth requirements, the value of Q is never infinite. The minimum can be as low as 1.79 according to Sokal [61] and Kazimierczuk [28] and thus, the high- Q design assumption is no longer valid or accurate [57]. Therefore to enable the design of the class E amplifier *a priori*, it is necessary to derive component values also for low- Q operation. According to [57] the output power depends mainly on supply voltage and the used load resistance, but also to some extent on the chosen Q . This dependency on Q can be taken into account by calculating numerically the relationship between output power and necessary optimum component values in terms of Q . Then a new set of design equations can be fitted to the numerical data as it has been done by a second order fit in [57] and by a third order fit in [14]. In the reference [57] the parasitic resistances are compensated in the resistive load in order to achieve the wanted output power level. The reference [57] takes the effect of a finite size of L_{RFC} into account.

Kazimierczuk analysed in [58], with the help of Laplace methods, the special case

when the capacitor in the series resonant circuit becomes a DC-block and does not resonate with the series inductor anymore. This is the limiting case where loaded Q becomes 1.79 at a duty cycle of 50%/50% [28], for example. In [58] the changes in circuit values, voltages, currents and output power were determined when the duty cycle was varied.

Raab [5] analysed class C, E and F through a frequency domain analysis, where the Fourier series of drain voltage and current were studied. By finding the appropriate Fourier coefficients we can alter and phase shift the voltage and current waveforms to achieve, for example class E operation, where only a limited number of harmonics are taken into account [5]. This helps in the choice of the load topology since there does not have to be an infinite amount of traps or resonators. The reference [5] did not and does not have to take any comment on the realization of the output circuit. As long as the necessary load impedances are met, the load circuitry can be chosen freely.

3.2.4 State-Space analysis

The State-Space analysis defines the differential equations in the on- and off- states and then makes the circuit voltages and currents continuous at the switching moments. The latter ensures that energy is maintained in the periodical operation. This leads to a linear set of equations which avoids the solving of the first defined differential equations in order to improve numerical calculation speed. [17] The State-Space method allows a considerable freedom in several design variables, such as finite bias inductor, finite resonator Q , any duty cycle. [17, 60] Furthermore, both the on- and off-resistance together with other resistive parasitic components in the circuit can be added to the equations. [17] Also, the effect of nonlinear output capacitance in State-Space analysis was taken into account by Sekiya [60]. Even though the State-Space analysis covers all necessary design variables, the iterations needed to achieve the class E switching conditions together with proper component values for the parallel capacitor, and series tuning inductor requires a careful minimization process [17], which may be time-consuming. The analysis and synthesis are fully numerical, and if the optimum efficiency requirements are discarded, the state equations in [17] may be used to evaluate other types of amplifiers with the same output circuit topology as class E.

3.3 Comparison of analyses and common design choices

The load network design of class E amplifiers has had several evolutions over the years. The usual addition to equations is the inclusion of some kind of nonlinearity in the output, such as a replacing the linear capacitance with a nonlinear one [21, 54] or combining the linear and the nonlinear output capacitance [55, 64] into the calculations. The effect of feedback capacitance on the size of total output capacitance [65] has also been discussed. Table 4 shows the changes in chronological order.

Table 4. Class E load network analyses over the years.

Author	Q/D	C_o	R_{paras} / R_{on}	L_{RFC}	Analysis type	Comp. calculation	M
[1]	Any / 0.5	Linear	No / No	Large	HQ+EX	AN	-
[9]	High / Any	Linear	No / No	Large	HQ	AN	-
[28]	Any / Any	Linear	No / No	Large	LA	NU	-
[62]	Any / Any	Linear	No / No	Large	LA	NU	-
[23]	High / Any	Linear	No / No	Finite	HQ	NU	-
[63]	Any / Any	Linear	No / Yes	Finite	LA	NU	-
[56]	Any / Any	Linear	No / No	Finite	LA	NU	-
[21]	High / 0.5	Nonlin.	No / No	Large	HQ	AN	0.5
[54]	High / 0.5	Nonlin.	No / No	Large	HQ	NU	$\frac{1}{2}, \frac{2}{3}, \frac{3}{4}$
[57]	Any / 0.5	Linear	Yes / Yes	Finite	DSF	AN	-
[66]	High / 0.5	Linear	No / No	Finite	HQ	AN	-
[17]	Any / Any	Linear	Yes / Yes	Finite	SS	NU	-
[65]	High / Any	Linear+ Lin. FB	No / No	Large	HQ	AN	-
[55]	High / 0.5	Combo	No / No	Large	HQ	NU	0.5
[60]	Any / Any	Combo	No / Yes	Finite	SS	NU	Any
[64]	Any / Any	Eqv. Cap.	Yes / Yes	Large	SS+LA	NU	Any
[24]	High / Any	Linear	No / No	Finite	HQ+DSF	AN	-
[VII]	High / Any	Combo+ Nonlin. FB	No / No	Large	HQ	NU	Any
High- Q = HQ	Laplace = LA	State-Sp. = SS	Dataset fit = DSF	Experim. = EX	Numerical = NU	Analytical = AN	Feedback = FB

Table 4 gives as a quick overview of the used analysis methods. If the output Q is assumed to be high, it seems that in many cases either the duty cycle of the device is fixed to 0.5 for nonlinear (or combination of linear and nonlinear) output capacitance. If the duty cycle is freely chosen, the output capacitance in the analysis is usually linear. In the original paper [VII], the duty cycle can be arbitrarily chosen for high- Q load component calculation while enabling any combination of nonlinear and linear output capacitance, nonlinear feedback capacitance and pn junction grading. The equations were kept simple to allow the easy numerical calculation of device drain voltage and load components. Numerical calculation makes it possible to know the drain peak voltage during the calculations of load components, and this is something that is not possible to do analytically in high- Q assumption equations, if the C_{ds} grading coefficient M differs from the value of an abrupt junction.

Indeed, [VII] shows another tendency which can be found in class E papers. Either the design equations become lengthy and analytical as in [23] or the numerical results are brought down to a set of figures, graphs and tables as in [VII]. The results in [VII] are all aiming to give some insight to the design choices that a designer can make.

Useful parameters in class E analysis are, for example, the peak drain voltage and current, duty cycle and quality factor. Peak drain voltage and current give necessary insight about stresses that the device has to face and thus, the designer has to choose an appropriate supply voltage and device size accordingly, so that reliable and efficient operation is reached. These issues are revisited for example in [VII], where the drain peak voltage increased when nonlinear output capacitance was included in the class E equations.

The peak drain voltage and output load are functions of the duty cycle. The duty cycle gives us some freedom to modulate the drain peak voltage and current levels with each other. The higher device off time increases the peak current and lowers peak voltage and vice versa. Alternatively, the load can be adjusted to a wanted level to avoid the use of an impedance transformation network. If the designed load is close to a wanted load, such as 50Ω , it is possible to tune the duty cycle parameter in the design phase of the circuit to achieve the wanted load match. The most interesting finding in [VII] was that the supply normalised peak voltage can be brought to under four even with the hyperabrupt device grading M of 0.8. The requirement was that the off time, k , had to be increased from 1 (50%/50% duty cycle) to about 1.35 (67.5% off, 32.5% on). The downside is that the peak current increases, which actually creates a minimum for the device size.

The quality factor Q in class E can be lowered until the minimum value of about 1.79 is reached [28, 61], in order to widen the operation bandwidth. At that Q level, the series capacitor in the output circuit becomes very large, in other words, the capacitor is an ideal DC-block. Since the Q has a minimum, the maximum value for operation bandwidth in a class E amplifier is reached at that Q level. In theory, if a 3 dB limit is used, a roughly 56% operation bandwidth can be achieved.

The finite bias inductor has been added into the class E analysis in [63]. It is found out that the class E component values are rather strongly affected by the low values of the bias inductor. Also, the dependency of the parallel capacitor on quality factor Q becomes stronger when the bias inductor is low. The benefits of the low bias inductor are that the output power is increased, the size of series inductor is reduced and by suitably choosing the size of the bias inductor, a larger output capacitance can be tolerated [63]. The most tempting benefit is the ability to apply a larger output capacitor or by tradeoff, increase the maximum operating frequency due to a smaller output capacitor [66]. However, there is a normalized ($R = 1$, $V_{dd} = 1$, $\omega = 1$) lower limit to the bias inductor value and it is found to be 0.6 [63]. Indeed, and as stated in [17], the bias inductor cannot be decreased to zero since the series tuning inductor will decrease to zero at some point. The direct design equations for the high- Q class E amplifier with a low bias inductor as part of output wave shaping was done by Grebennikov and Jaeger [66]. Zulinski [23] has done the same analysis for any duty cycle and thus, achieved a more general result, but his approach did not have any easily applicable design equations.

The previously mentioned parameters are not all that affect the optimum class E operation. The transistor feedback capacitance plays a part in the output load by increasing the total parallel capacitance seen at the drain, as shown in [65] and [VII]. Furthermore, if feedback is not taken into account in the design, there is a substantial amount of second harmonic current from drain to gate [VI]. The second harmonic feedback modulates the input signal by varying the duty cycle and input impedance. The effect of feedback on class E has been studied in [VI] and discussed in this work in Sections 4.3 and 5.1.

3.4 Simulation considerations

The design of class E amplifiers requires care in the simulation phase. Class E amplifiers are designed for higher and higher output powers and often with a harmonic balance (HB) simulator. The combination of high output power together with a HB simulator

may lead to the use of an electromagnetic (EM) field simulator. This way the designer can ensure that the current capability of the output wiring is sufficient for the currents, and S-parameters can be obtained for easy reuse in the HB simulator. Therefore, the use of a field simulator together with HB simulator is justified.

3.4.1 Harmonic Balance

Since harmonic balance is based on *a priori* knowledge of the used frequency spectrum, this may lead the designer to a faulty result if the amount of used harmonics is small. As an example, a simple class E circuit simulation set with different amount of harmonics is shown in Fig. 14(a). The simulations were carried out by using an ideal switch and all components except parallel output capacitance C_o were linear. It is clearly seen that both the normalized drain efficiency and output power saturate to a fixed level with a higher amount of harmonics than eight. As a rule of thumb, nine or more harmonics should be used in harmonic balance simulations of switching amplifiers. The relatively simple simulation circuit is also analysed in terms of the used simulation time in Fig. 14(b). It is seen that in this simple case there is not much difference if we use eight or 13 harmonics in the simulations. However, it should be emphasized that the circuit has only one nonlinear component, the C_o . When circuit complexity and the number of nonlinear components increase, the simulation time will increase accordingly.

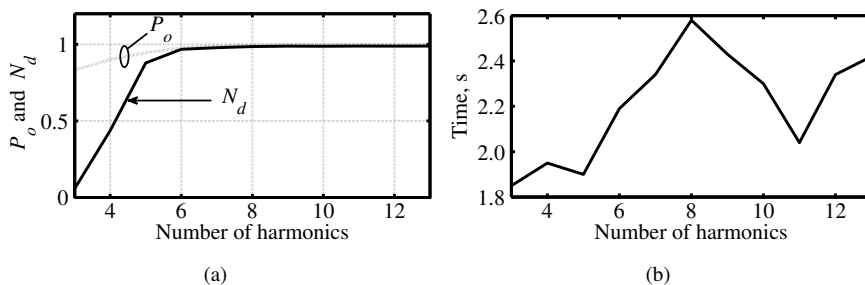


Fig 14. a) Normalized output power and drain efficiency and b) simulation time as a function of used harmonics.

3.4.2 EM field simulations

In paper [V] it was found out that currents flowing in the parallel resonant circuit of a tuned amplifier were so high that special care had to be taken in the design of the integrated circuit. The current capability of both the wiring on the integrated circuit and the capacitors had to be high, which meant that the wire width had to be over $200\ \mu\text{m}$ and the capacitors had to be divided into several fingers in order to increase the current capability and to lower the ESR. This involved the use of a 2.5-D EM field simulator. The original lumped circuit schematic together with peak currents in the circuit are shown in Fig. 15(a). The lumped circuit had to be converted into a distributed element manually while constantly comparing the S-parameters between the two circuits. The final simulated S-parameter file of the distributed resonator was brought back to the HB simulator for further evaluation of the resonator operation. The designed distributed resonator resulted in a lower Q than in the original lumped resonator. This was due to the $3/4$ -turn inductor line, which could not be made physically any smaller. The implemented distributed resonator, in Fig. 15(b) is clearly seen in the actual implementation of the whole amplifier chip.

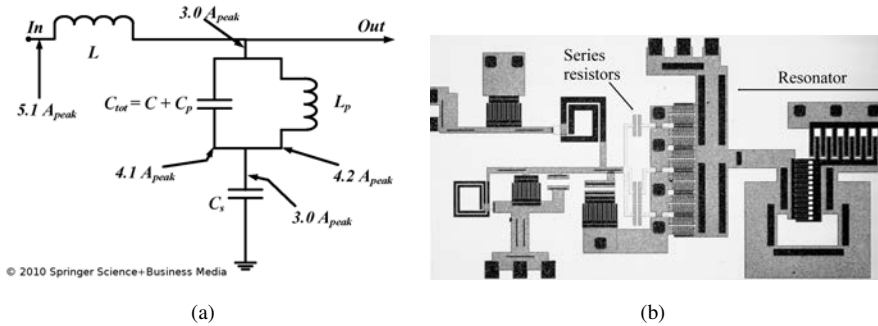


Fig 15. a) Simulated lumped resonator circuit [V, with kind permission from Springer Science+Business Media] and b) the implemented Class E⁻¹ amplifier.

4 Implemented circuits and simulation studies

I - Output circuit

This chapter introduces circuit implementations together with the simulation studies of several tuned power amplifiers. The focus is on the output circuit, what are the effects of matching on the operation of a low- Q resonator, how do the nonlinear properties of the output circuit behave in the presence of supply modulation, what is the effect of feedback (or feedforward) and parasitics on efficient output circuit operation.

4.1 Low- Q output network

In [V] the implemented amplifier uses a modified and tuned class E⁻¹ parallel resonator, which utilises wide inductor lines to ensure reliability due to high currents in the resonator. Depending on the current, the line has a minimum width, which also restricts the length of a 3/4-turn inductor. This resulted in [V] as a lower Q value of the parallel resonator than originally designed. The load network's Q value is of importance when the designer is considering the bandwidth of the amplifier and the sensitivity issues of the network.

In [IV], the low- Q resonator of [V] was also considered by taking into account the common single stage L-type matching circuit. It was shown that the Q value of the external matching circuit was higher, which had an effect on output load tuning as well. In an ideal case in [IV], the optimum design value of the parallel output capacitance, designed to operate with a specific parallel resonator, was decreased down to a half of the original size if the external circuit was a single stage L-type match. This change was not seen with a broadband resistive match. The decrease of the size of an optimum parallel capacitor restricts the size of a usable device or changes the maximum achievable frequency of operation. If the parallel capacitance of the device is taken into account in class E⁻¹ design [18], the maximum operating frequency is

$$f_{max} = 0.0728 \frac{P_o}{C_o V_{dd}^2}, \quad (12)$$

which is 1.3 to 1.4 times larger than the value for the traditional class E amplifier [18]. Just for reference, the maximum operating frequency for the traditional class E can be

approximated for a 50/50-duty cycle from Eq. (13) [38],

$$f_{max} = 0.057 \frac{P_o}{C_o V_{dd}^2}. \quad (13)$$

In both class E topologies, the decrease in output parallel capacitance gives some additional freedom in the design of a suitable output resistive load [67] and supply voltage level [68]. Furthermore, the parallel tuned resonator discussed in [IV] contained parasitic resistances and inductive reactances that caused the resonator to perform only modestly. While knowing the high currents in the resonator and the reality that the output resistive load in [IV] was only about 5 Ω , these underline the difficulty of designing a well-performing, high current resonator and matching, since small variations e.g. in ESR contribute quickly to the overall performance.

4.2 Effects of varying supply voltage

In this section, an extended view on supply modulation is taken by discussing the nonidealities of the output circuit and the transistor itself. The focus is mainly on the class E amplifier. Later, in Section 4.3 the effects due to the input signal feedthrough in class E amplifiers are studied.

4.2.1 Efficiency degradations due to nonlinear output capacitance

The supply dependent output amplitude and phase variations are a point of interest since it is our aim to use class E amplifiers with some kind of supply voltage modulation. One of the changing parameters in terms of supply voltage is the nonlinear C_o . There are also other variations, such as the output signal variations in terms of the series output filter properties [48] and feedthrough [48], but they do not vary with supply. Instead, the Miller effect due to gate-to-drain capacitance does vary with supply.

Suetsugu *et al.* [69, 70] have discussed the influence of voltage dependent C_o , but only to a case where junction grading M was 0.5. In [VII] the influence of nonlinear output capacitance on amplifier performance was further investigated by allowing the grading to vary from 0.3 to 0.8. The increase in M degrades the drain efficiency at low supply voltages, which is shown in Fig. 16(a). Below 5 V supply (max. being 20 V), all device gradings show a decrease in drain efficiency due to non-optimum switching (no

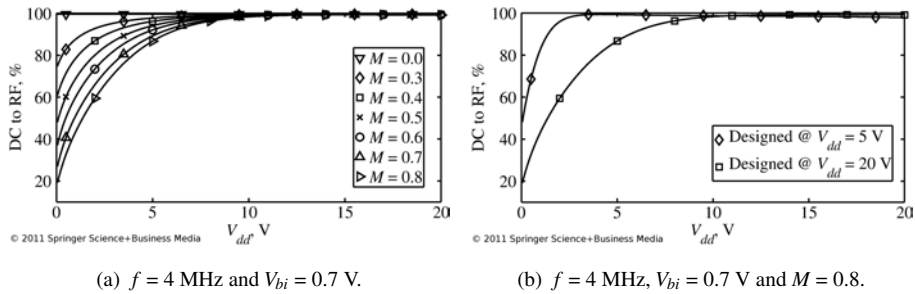


Fig 16. Simulated drain efficiencies when supply voltage is varied [VII, with kind permission from Springer Science+Business Media].

ZVS and ZVDS), where hyperabrupt case is the most lossy of all. This detuning is caused by the nonlinear output capacitance because it appears as a larger capacitor in the low supply levels and changes the time constant of the output circuit. The change in time constant can be circumvented partially by designing the amplifier to supply level of 5 V instead of the original 20 V. In practice, the implemented amplifier will be used with the same levels of supply as the original design (up to 20 V) and thus, it has to be ensured that the modified amplifier can produce the same amount of power as the original to the 20 V supply. With the changed design and by providing in actual operation a maximum supply level of 20 V, we can achieve significant improvements in low voltage drain efficiency while losing it slightly at higher supply levels. The comparison between the suggested 5 V, lower resistive load design and original 20 V design is shown in Fig. 16(b). This design strategy is of great importance when the signal levels are low most of the time and the device output capacitance nonlinearity is high.

Gaudó *et al.* [71] extend the study of nonlinear output capacitance to include frequency limitation caused by the output capacitance as a function of duty cycle. It was found out that optimum duty cycle in terms of maximizing the operation frequency is $D = 0.35$ [71]. This is a favourable value, since the peak voltages in the output decrease while the peak currents increase, as shown for example in [9, 28, 71] and in [VII]. Unfortunately, the increase in peak currents requires the device to have greater ability to withstand high peak currents, and thus, the device has to be larger in physical size.

4.2.2 *The effect of bias impedance on supply modulation speed*

It has been noted in one of the first analyses [9], that the voltages and currents in the output circuit depend directly on the supply voltage. Therefore the V_{dd}/AM characteristic should in theory be very linear. One of the earliest studies about supply modulated class E amplifiers was done by Kazimierczuk [48], where special attention was given to the effect of the output circuit during *AM* modulation. Kazimierczuk suggests that the upper and lower sidebands are transmitted through the output network with non-equal amplitudes and phases. According to [48], output harmonic distortion increases with the increase of *AM* amplitudes, with the increase of load network loaded Q and with the increase in the ratios of modulation frequency to carrier frequency. Reference [48] does not take into account in the analysis the effect of DC-bias inductor, but only gives some approximations of the minimum value of a usable bias inductor.

Raab [41] considered the bandwidth of the supply modulator and the delay differences of phase and amplitude signals in terms of IMD levels in a Kahn-technique (EER) transmitter. The RF power amplifier that Raab used in the implementation was class D. What Raab found out was the requirement for envelope bandwidth in terms of IMD level and he calculated the relationship between envelope bandwidth and the differential time delay of the two signal paths. Further, the effects of differential time delay onto the IMD products in a two-tone case was analysed and requirements for the maximum value for the delay to achieve a certain IMD level were shown [41]. Milosevic *et al.* [46] studied also the intermodulation products in an EER transmitter. In the analysis approach, he considered a class E amplifier, where the envelope path was modelled with a single LP-filter. The focus in [46] was in the relationship of envelope path transfer function and IMD levels. It is evident from [46] that the envelope path has to have a bandwidth of 4 or more times the bandwidth of the envelope signal in order to keep the IMD to sideband ratio above 35 dB.

Kimber [47] has extended the analysis to approximate the whole output network with a two-pole low pass filter. One pole comes from the series resonant capacitor-inductor combined with the load resistance. The second pole is formed by the bias inductor and the effective DC-resistance seen by the supply, where the latter varies with the frequency of operation. One of the most interesting points in Kimber's investigation was the fact that a low valued DC bias inductor causes the amplifier to dissipate more power (about 20% of DC power) when high frequency *AM* modulation is applied to

supply voltage. This is a disappointing finding, since the lower valued bias inductor can increase modulation speed and improve, in certain inductor values, the output power capability of the class E amplifier [23]. Additionally, Kimber [47] discusses the dynamic losses, where the memory of the series resonant circuit causes the voltage of the parallel output capacitor (or C_o) to remain non-zero just before the switch starts to conduct and thus, result in power dissipation.

Heiskanen [45] compared two class E amplifiers with a different bias line design. The first one was the classical class E with a relatively high impedance bias line and the other was class E where the bias inductor is relatively low and partially resonates out the parallel output capacitance of the device. The latter topology showed increased modulation bandwidth and 1.4 times higher centre frequency compared with the classical class E. Further, the modulation bandwidth could in theory be as wide as the value of centre frequency while the classical topology with a large bias inductor showed modulation bandwidth under 1% of the value of centre frequency (-3 dB level). The tuned class E topology also presented improved IMD characteristics, where two-tone output IMD levels were reduced by 40 dB when compared with the classical class E [45].

It is clear that a large bias inductor slows down the modulation speed, causes IMD and has a notable amount of equivalent series resistance (ESR). The high value bias inductor can be replaced by a $\lambda/4$ length transmission line, which does not slow down the supply modulation and is a rather low-ohmic route. This solution is, however, relatively narrowband and consumes a lot of printed circuit board (PCB) space. As an example of this, a $53 \Omega \lambda/4$ at 1 GHz in a Rogers TMM 6 PCB takes around 37 mm long line. In some cases this is impossible to implement.

As a compromise, a combination of reduced length line and small bias inductor can be used. To compare the effects between the large bias inductor, the inductor/line combination and $\lambda/4$ transmission line, an ideal inductor of 150 nH, an ideal inductor of 15 nH + $\lambda/12$ transmission line and $\lambda/4$ transmission line is chosen in a TMM 6 laminate. The simulated results of bias line impedance and imaginary part of S_{11} are shown in Fig. 17(a) and 17(b), respectively. It is immediately clear that the combination of the inductor and line can reach the same or higher impedance at the designed frequency of 1 GHz. Further, the impedance of the combined bias is slightly more wideband than the $\lambda/4$ line, which is also clear from S_{11} plot in Fig. 17(b). This all can be implemented with 1/3 of the original line length and 1/10 of the size of original bias inductor. The combination is not as wideband as the ideal inductor and does not

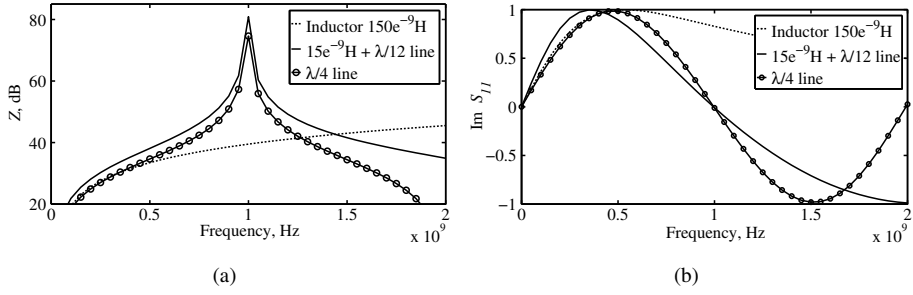


Fig 17. The change of a) bias line impedance and b) the imaginary part of S_{11} .

have the low-ohmic high speed properties of the single $\lambda/4$ line, but it is still a good compromise of size and ESR for narrowband use. The $\lambda/12$ transmission line alone additionally has a natural low impedance resonant frequency at the fourth harmonic, which eliminates the second harmonic trap effect that the $\lambda/4$ transmission line has. The $\lambda/4$ trap effect at the second harmonic is detrimental to amplifiers such as class E, F^{-1} or J, since the high-efficiency operation inherent to these amplifiers requires a high second harmonic voltage component in the drain. In other words, due to the shift in high impedance resonant frequency, the bias line can be connected directly to the drain pin of class E, F^{-1} or J amplifiers without the fear of losing the tuning of the second and third harmonic. The added small inductor to the $\lambda/12$ transmission shifts the resonant frequencies even more and causes them to be non-integer multiples of each other. This is a considerable benefit since now the low impedance trap frequencies do not occur at any harmonic frequencies of the amplifier and thus, give a total freedom in the design of the harmonic impedances of an amplifier.

4.3 Input - output feedthrough

Feedthrough effects in class E amplifiers can be divided into two parts: First, the effect of input signal feedthrough (or feedforward) on the linearity of a low amplitude output signal, and second, the effect of both current feedback and Miller effect onto the input of the amplifier. The latter is discussed later in Section 5.1. The directions of effects are shown in Fig. 18, where a) is the direction of input signal feedthrough to the output and b) represents the direction of both Miller effect and second harmonic current injection. It is demonstrated by measurements in [I], that both V_{dd}/AM and V_{dd}/PM are dominantly caused by the heavy feedthrough from input to output. The input signal

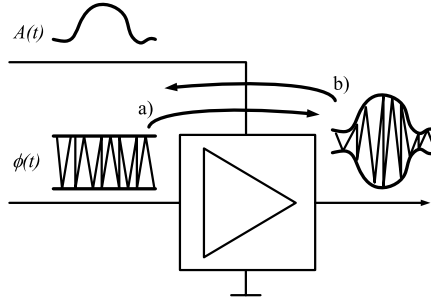
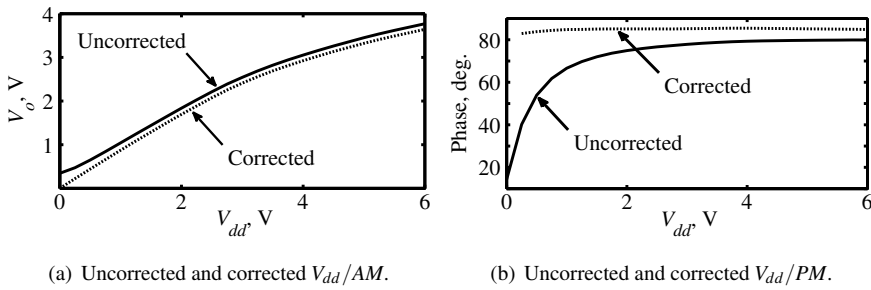


Fig 18. Directions of effects of feedback: a) feedthrough of the input signal and b) Miller effect and current feedback.



(a) Uncorrected and corrected V_{dd}/AM .

(b) Uncorrected and corrected V_{dd}/PM .

Fig 19. 1-tone V_{dd}/AM and V_{dd}/PM before and after computational feedthrough tone removal. Revised from [III].

is fed to the output of the class E amplifier slightly attenuated and phase shifted. This feedthrough of an attenuated and phase shifted input signal creates variations in the output by shifting both the phase and amplitude of the output signal. These phase and amplitude changes are also evident from the single tone measurement results of an actual class E amplifier in Fig. 19(a), where the feedthrough shows as a non-zero output voltage level when the supply is zero [I]. Similarly, the measured phase behaviour in Fig. 19(b) experiences a heavy phase shift in the region of low supply voltages.

However, there is more to this feedthrough, since in EER the input signal of a class E amplifier is an amplitude limited phase signal, which is a very wideband one due to the nonlinear signal processing. The wideband input signal appears as a wideband distortion in the output of the amplifier as demonstrated in Fig. 20. From the design point of view, the feedback capacitance appears as an additional capacitance in parallel to the device output capacitance [65] that should be accounted for [VII].

Feedthrough effect is discussed in original article [I], where the supply voltage of a

class E amplifier was modulated to find out how large an error tone vector was created to the output of the amplifier. It was found out that by subtracting the feedthrough vector from the output signal in a mathematics program, the phase behaviour of the amplifier was almost linear throughout supply levels. This is illustrated in the phase graph with correction in Fig. 19(b). The V_{dd}/AM behaviour is also linearised especially in low supply voltages, which is clearly seen when comparing uncorrected and corrected V_{dd}/AM in Fig. 19(a). After the elimination of feedthrough signal, the correction of both the phase and amplitude behaviour needs less effort and is easier to implement.

Fig. 20 illustrates the situation in EER, where the input signal is a modern wideband communications signal. The signal is first divided into amplitude and phase information, which are led to the amplifier through supply and input (gate), respectively. Now the high amplitude wideband input signal is fed to the output due to feedthrough with attenuation. Therefore, the reconstructed and amplified output has an increased amount of distortion right next to the wanted output signal. The dotted line in the output shows the shape of the original signal. The feedthrough causes in this case a wideband distortion that decreases the adjacent channel power ratio (ACPR) of the output signal. This example emphasizes the importance of feedthrough attenuation, and next we will take a look at five possible ways of eliminating the feedthrough.

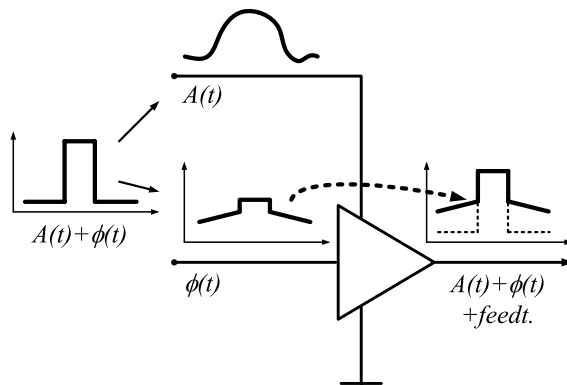


Fig 20. Distortion due to feedthrough of a wideband input signal.

4.3.1 Minimizing the feedthrough

One correction to the feedthrough is to lower the input signal level when the supply is low. This is already discussed in [49] and applied by lowering the supply voltage and therefore the gain of a driver buffer stage. This results in a decrease in intermodulation distortion (IMD) and in an increase in amplifier total efficiency [49]. A suitable drive signal reduction function in a digital signal processor (DSP) can be used as well to lower the applied input drive according to the drain voltage of the class E amplifier. A sample implementation of this is demonstrated in [42] and the reduction function is also discussed in [III].

The second solution is to apply an AC-coupled inductor in parallel with the feedback path or to use a device technology with low feedback coupling. In [I] it was suggested to use a series RLC-resonant circuit in parallel with feedback capacitance. In simulations it was found out that about 5 dB feedthrough attenuation can be achieved at the centre frequency of 1 GHz with 0.8 dB loss of gain. The simulated attenuation of feedthrough is shown in Fig. 21, where the supply voltage is kept at zero. The reduction in feedthrough is also evident in V_{dd}/AM behaviour [I]. Unfortunately, the feedback resonator approach shifts the V_{dd}/PM more in the low supply region [I], which is likely due to a phase reversal when supply dependent C_{gd} varies.

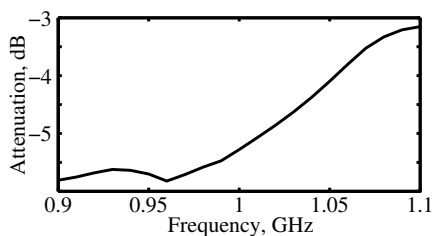


Fig 21. Attenuation of feedthrough due to feedback resonator. Revised from [I].

The third way to eliminate feedthrough is using push-pull class E topology, where the inputs are cross-coupled to the output with capacitors. The capacitors have to be equally sized when compared with feedback capacitors. This topology is discussed later in Section 5.1 and in Fig. 27, where the topology is able to correct also input impedance changes due to variations in device gain.

The fourth way to tackle the feedthrough signal is to apply a tone with exactly the same frequency and amplitude and sum it up with appropriate phasing to the output

signal. The generation of this tone can be done with DSP as in Fig. 22(a) or alternatively with a secondary parallel switching power amplifier (SwPa) with no supply voltage and the same input applied as the original amplifier (see Fig. 22(b)). The latter choice has been patented in the UK by Chen [72].

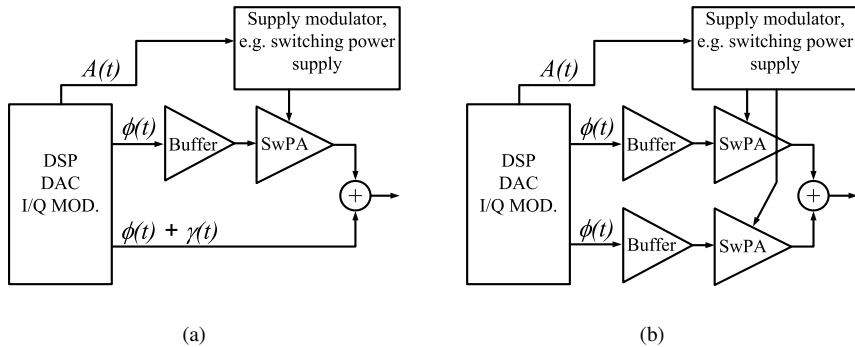


Fig 22. a) Polar transmitter with feedforwarded feedthrough correction and b) with combined feedthrough correction and peak amplifier.

As a fifth suggestion, the implementation in Fig. 22(b) can be extended to combine both the low supply feedthrough cancellation and peak amplitude power boost. When supply voltage is high enough in the primary amplifier, the supply of auxiliary SwPA might be increased from zero and by changing the input phasing, the two amplified signals can be combined into one high-power signal in the output. This way two SwPAs could be designed to have a smaller output power instead of one large amplifier, which helps in extending the operation frequency of a class E amplifier and increases the value of resistive load in the output circuit. The latter relaxes the sensitivity requirements of output matching. Furthermore, the switching power supply does rarely have to apply high currents if the PAR of the signal is high. Therefore, it is beneficial to use accurately optimized twin switching power supplies or a combination of switching power supply and a linear regulator to deliver the necessary amplitude information. A very similar topology as in Fig. 22(b) is patented by Rosnell in the US [73], but it utilises a different power control scheme by combining linear amplification using nonlinear components (LINC) and envelope tracking (ET) together. However, the power control in [73] may be used differently to implement the amplifier in Fig. 22(b) and to eliminate the feedthrough of the main amplifier.

4.4 Effects of transistor size

The most beneficial feature of a polar transmitter is the ability to correct device nonlinearities and delays through baseband DSP predistortion. This gives the ability to correct the feedthrough seen in Section 4.3 and to predistort the remaining V_{dd}/AM and V_{dd}/PM . There is one situation where the predistortion through supply modulation and thus, the correction of V_{dd}/AM does not achieve the wanted function.

This happens when the device becomes unable to deliver the necessary output current. This issue is discussed in [III], where it is shown by simulations that when current is saturated, it is no use to correct the V_{dd}/AM behaviour by increasing the supply voltage. It will only lead to unnecessary instantaneous power dissipation in the device, shown in Fig. 23, where the instantaneous power dissipation is plotted at different supply voltage levels. The power dissipation is due to the fact that at a certain supply voltage level the current of the device saturates and even when extra supply voltage is applied, the output does not increase accordingly. Instead, the drain voltage starts to rise during the on-period, indicating an increase in on-resistance R_{on} . Thus, the extra power applied with predistortion is dissipated in the device itself.

There are at least two obvious ways to minimize this current saturation: to manipulate the device current saturation point higher either by increasing the drive level or by increasing the transistor effective periphery. The drive increase may result, in the worst case scenario, in a damaged device and the large periphery device limits the achievable operating frequency according to Eq. (13). A further option is to accept the current limitation corner and linearize the V_{dd}/AM to lower supply voltages below the seen compression point.

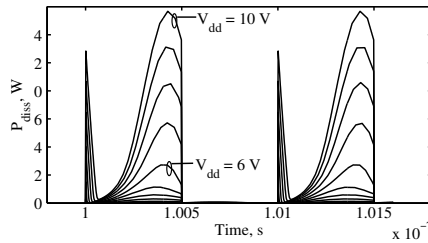


Fig 23. Instantaneous power dissipation waveforms when supply is modulated. Revised from [III].

4.5 Multiple resonances

Transistor package parasitics may cause unwanted current resonances that ruin the optimal waveforms and cause power dissipation. One source of such a detrimental effect is the bondwire inductance, which is connected in between the drain to source capacitor and external linear output capacitance, as shown in Fig.24(b). Together with the bondwire inductance, the capacitors form a pi-network which has very low damping. The resonance shows as sinusoidal current resonance, I_{res} , in the device off-state where the external output capacitor and drain to source capacitor are pushing and pulling energy from each other, as shown in one simulated off-period in Fig.24(a). If the transistor is switching on and off, as in class E amplifiers, the steady on-state drain current pulses excite the off-state resonance through bondwire. The worst case is when two capacitors are of the same size and thus, have the same energy storage capability. For example, the external load circuit does not damp this resonance since the bias inductor and the series inductor toward resistive load appear as high impedance at the frequency of the resonance. The situation is roughly the same in all inductively tuned amplifiers, where the fundamental load has a considerable inductive reactance. It is disturbing to notice that this type of resonance can easily go unnoticed in a case where the amplifier is designed only by fulfilling certain harmonic impedances. In that situation the designer is looking only at the harmonic tones, and not at some unwanted tone somewhere in between the harmonics.

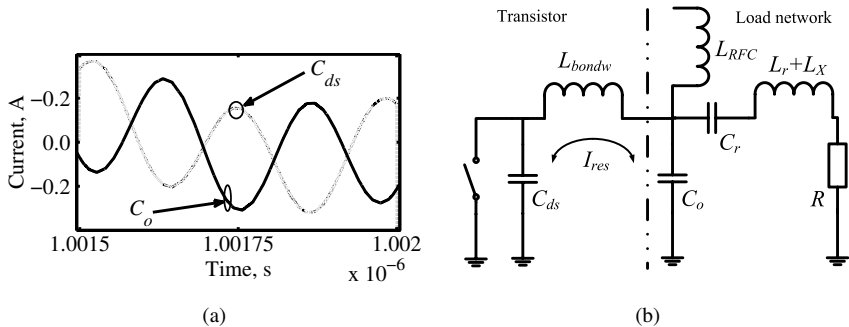


Fig 24. a) Current resonance in between parallel capacitances during off-state (0.5 ns) and b) schematic of the resonant pi-network. Revised from [III].

We can quickly notice that either we have to eliminate one component in the pi-network or to find some kind of circuit solution that takes all components into account.

As a solution, the circuit should be implemented totally in the integrated circuit avoiding the bondwire inductance, or the device used should be sized so that all of the parallel capacitance comes from the drain to source capacitance, thus avoiding the external capacitance. The circuit in the latter choice can be synthesized with the help of [VII]. If a class E⁻¹ topology is to be designed with bondwire and device parasitic capacitance, one solution is found in [18], where both parasitics are accounted in the output load in order to achieve ZVS and ZVDS.

5 Implemented circuits and simulation studies II - Input circuit

In this chapter, we will take a look at different nonidealities of the input circuit, and particularly the nonlinear capacitors of feedback and gate node are of interest. Further, some discussion about improving the device operation by minimizing the seen nonlinearities and timing mismatches is presented. Also, the amplifier's stability will be looked at. The emphasis in the first section will be on class E, while the second and third focus mainly on class E⁻¹.

5.1 Input - output feedthrough and input impedance nonlinearity

In Section 4.3 the feedthrough from input to output was studied and now we will take a look at the effect of the reverse direction, the Miller effect. The Miller effect causes both a time and drain supply dependent feedback capacitance that varies the capacitive input impedance of the amplifier. The Miller effect can be written in a simple form in equation (14)

$$C_{in}(t, V_{dd}) = (1 - A_u(t, V_{dd}))C_{gd}, \quad (14)$$

where $A_u(t, V_{dd}) = -\partial V_{ds}(t, V_{dd})/\partial V_{gs}(t)$. The Miller capacitance has several effects on the input impedance. The value of gain term $A_u(t, V_{dd})$ is changing during one period due to drain voltage pulses and also according to supply level, which both make the apparent input capacitance vary heavily in a switching power amplifier, e.g. class E. This leads to the fact that when a class E amplifier is applied with EER, the input capacitance will vary accordingly with the modulated supply and thus, the input impedance varies considerably. These variations make the matching of the input more difficult and may result in some amplifier gain variation due to improper matching. Also, due to inductive output tuning, the gain has a phase shift of about -150 degrees, which makes the feedback capacitance appear partially as a negative resistance at the gate. Further, the feedback capacitance provides a path for large second harmonic current injection from output to input, which causes duty cycle variations that degrade the drain efficiency of a class E amplifier.

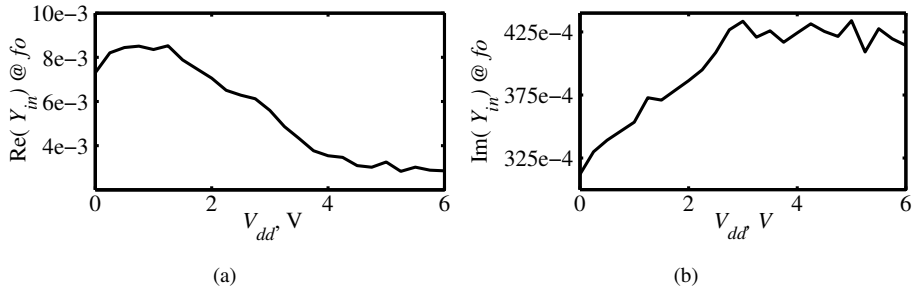


Fig 25. a) Measured real and b) imaginary part of fundamental input admittance of implemented class E amplifier. Revised from [VI].

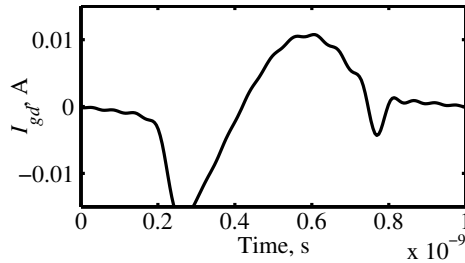


Fig 26. Drain-to-gate feedback current. Revised from [VI].

These issues are discussed in [VI] where simulations and measurements of varying class E input impedance are presented. The Miller effect is shown clearly in Figs. 25(a) and 25(b), where the real and imaginary parts of measured input admittance are plotted, respectively. The measurements show a clear reduction in the resistive component, indicating the gyration of feedback capacitance. The same reduction is shown in a Smith chart in [VI], where the input impedance is strongly closing the edge of a Smith chart. Luckily, there is enough resistive damping to keep the amplifier stable. Similarly, the imaginary admittance increases with supply, confirming the increase in input capacitance [VI].

The second harmonic current feedback from the output of a class E amplifier has a rather high amplitude even when coupling between input and output is modest. This is shown in the simulation result in Fig. 26, where the gate-to-drain capacitance is 0.15 pF at 1 GHz . The generation of the second harmonic can be explained by the drain pulse shape, or alternatively by considering C_{gd} a strongly time varying Miller capacitance. Either way, C_{gd} injects to the gate a strong second harmonic current that alters the duty

cycle of the input signal and thus causes efficiency losses due to nonoptimum timing [VI].

These effects cannot be eliminated through the decrease of input drive in low supply values or similar, because the increase in Miller capacitance and feedback current occur mainly when the switch is off. Therefore, the solution is to somehow eliminate the coupling between output and input. This can be done with an AC-coupled resonant inductor in parallel with C_{gd} . However, as C_{gd} injects current on several harmonics, the designer has to choose whether to minimize the fundamental impedance change by tuning the resonance of inductor and C_{gd} to the fundamental frequency or to minimize the second harmonic injection by tuning the resonance to the second harmonic. In short, by resonating the C_{gd} we can achieve either cancellation of fundamental impedance change or feedback current, but not both. As a suggestion, a designer should tune the circuit to minimize fundamental effects and use separate traps in the input for minimizing the second harmonic. In addition, this solution attenuates the second harmonic generated by nonlinear C_{gs} [VI].

As a topology solution to fundamental impedance change, a push-pull class E can be used with two extra cross-coupled feedback capacitors that are of the same size as feedback capacitors. The cross-coupled push-pull class E circuit is shown in Fig. 27. The push-pull configuration eliminates the fundamental feedback but unfortunately doubles the second harmonic current injection. Therefore the extra traps are still necessary at the gate. However, as an extra benefit of the topology, the input signal feedthrough from input to output is cancelled accurately and thus, the low supply level linearity is improved.

The gate to source C_{gs} capacitance is also one significant nonlinear capacitance in a transistor device. It was suggested in [17] to use a supply bias inductor of a driving circuit to resonate the C_{gs} out. The idea was not only to minimize impedance variations and ensure matching, but to help the driving circuit by minimizing the capacitive load and thus, to increase PAE. Further, the inductor used to resonate the C_{gs} out can be used in delivering the gate bias to the final PA. Even with these two approaches, push-pull class E and resonated C_{gs} , the second harmonic current injection from feedback remains. The elimination of the second harmonic requires a separate trap at the gate.

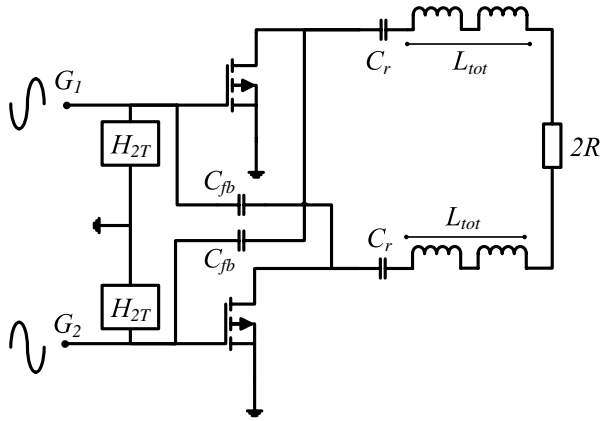


Fig 27. Push-pull class E amplifier with second harmonic traps (H_{2T}) at the gates. Revised from [VI].

5.2 Effects of input routing

In a high-power RF amplifier the device periphery increases to significant in terms of the wiring lengths of the device. By applying a simple microstrip ladder-input network, it is possible that the non-equal input wiring can cause severe timing mismatch and thus, losses in switched power amplifiers. This issue was simulated and studied in a class E^{-1} case in [II], where it was found out that the matching of the input lengths is much more critical in switching PAs than in linear PAs. The input design of a large periphery transistor can lead to a situation, where a simple ladder-type input routing made the input voltage waveforms severely mismatch from each other and the non-optimum timing of the switches led directly to efficiency losses. The microstrip input structure used in simulations is shown in Fig. 28.

However, the simulated mismatch in the gate waveforms of different fingers in [II] was so large in time domain that the timing error due to input routing lengths could not fully explain the differences observed. The simulated waveforms are shown in Fig. 29, where the gate voltages of extreme ends of the transistor in a class E^{-1} amplifier are plotted in the time domain. The floor of Fig. 29 is selected to be the transistor threshold voltage -0.8 V. The timing difference in the rising edge is around 80 ps, which is considerably larger than the calculated line delay of around 20 ps. The seen amplitude and timing differences in the simulated class E^{-1} amplifier are caused largely by distortion produced from the voltage dependent gate to source capacitance

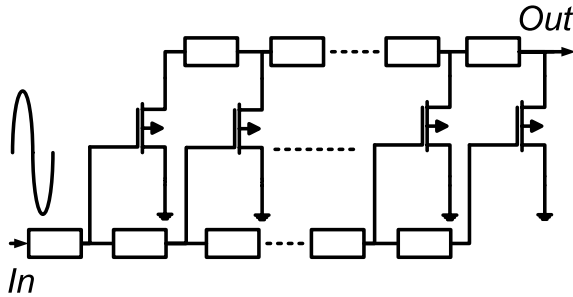


Fig 28. Input routing used in simulations of class E^{-1} in [II]. Revised from [II].

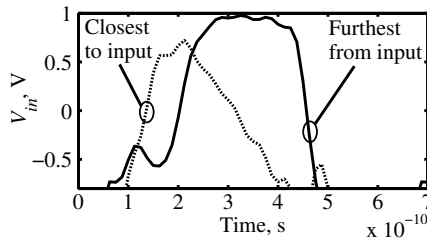


Fig 29. Timing differences between extreme ends of transistor in class E^{-1} during on period. Revised from [II].

C_{gs} of a pseudomorphic high electron mobility transistor (pHEMT). The simulation model is discussed in [II], where the modelled C_{gs} increases to very high values when gate voltage is high and supply voltage is low. Note that here the second harmonic generated by this mechanism was dominant, also compensating the second harmonic delivered in via C_{gd} . Just for reference, the same indication of the C_{gs} being dominant at the second harmonic was also found in [VI], where the second harmonic admittance of a GaAs-based class E amplifier was measured.

The heavily varying C_{gs} due to high amplitude drive and the mismatch of the input lines cause a total of 80 ps differential delay. This level of delay is detrimental to the efficiency of any switching amplifier. In [II], the decrease of simulated efficiency due to delay was 11 % units. The obvious solutions are to eliminate the uneven lines, to minimize generated distortion, or both. As a solution, a tree-like input was implemented in [II] to a class E^{-1} amplifier, where the input lines have the same lengths. With this

solution, the simulated timing difference decreased considerably and the drain efficiency was increased to its original level [III]. The implemented wiring is shown in Fig. 15(b).

Further, the original article [II] discussed another solution for the timing mismatch. The suggestion was to use a well-tuned and physically well-placed second harmonic trap in the ladder input that would eliminate the distortion caused by the gate capacitance. However, if the transistor itself is large, positioning a trap to every gate of parallel divided transistors would consume a lot of chip area. It was found out that a single trap in the furthest end of the ladder (last transistor) reasonably eliminates the timing shifts. Still, the amplitudes seen at the gates remain uneven and need equalization [III].

5.3 Need for stabilization

It is necessary for a RF designer to evaluate the stability of PA by sweeping the frequency. Often, there are one or two frequencies, where the amplifier is not unconditionally stable. Then we have to rely on stability circles to further evaluate the possibility of oscillation. In the original article [V] the stability of a class E^{-1} PA was evaluated with stability circles obtained from large-signal S-parameters, and a small amount of series resistance had to be added to ensure stable operation. The implemented three series resistors in the input lines are shown in Fig. 15(b). Further, the designed output resonator structure in Section 3.4.2 provided the possibility to attenuate instability just below the operation frequency. The resonator structure was a modified class E^{-1} load, shown already in Fig. 15(a), where the original DC-block was taken away and replaced with a single capacitor C_S under the parallel resonator. The capacitor C_S causes a notch in the frequency response and the ability to tune this notch with the value of C_S helps in eliminating possible unstable frequencies, which can appear just below fundamental frequency. This tuning of C_S was used in [V], where a persistent instability at 1.3 GHz was stabilized. The simulated stability factor after the implementation of the stabilizing notch is shown in Fig. 30(a). The tunability of notch with C_S is shown in Fig. 30(b).

The designed class E^{-1} amplifier needed small series resistors at the input to further stabilize the operation, and this was done with the help of stability circles. Further, too much resistance attenuates the gain of the amplifier and therefore, a careful examination of the stability circles had to be done in order to maintain as high a gain as possible.

To further improve the stability of the designed class E^{-1} amplifier, a wideband RC-sink was implemented in [V] to be in parallel with the gate in order to reduce gain in higher frequencies. The RC-sink provided a substantial improvement in amplifier

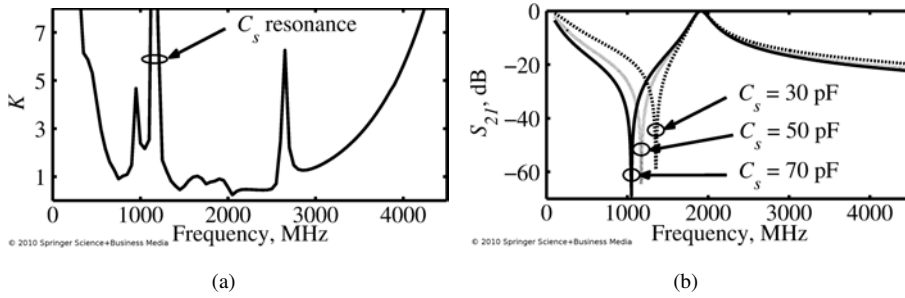


Fig 30. a) Simulated stability factor with 30 pF C_s and b) the effect of C_s variation [V, with kind permission from Springer Science+Business Media].

stability, as can be seen from the measured load-pull instability points of Figs. 31(a) and 31(b), where the measured points come from an amplifier without and with the RC-sink, respectively. The instability recorded at the measurements was caused by the supply bias line and seen as spurious tones at the output, ± 33 MHz away from the fundamental tone [V]. Surprisingly, the unstable behaviour can be stabilised considerably by the wideband RC-sink. With the RC-sink, the drain bias oscillations could be seen in only a few load impedances, as shown in Fig. 31(b). The instability caused by the supply bias line can also be eliminated by providing very low impedance bias supply through a supply modulator or by increasing the size of decoupling capacitors, if a static supply is used.

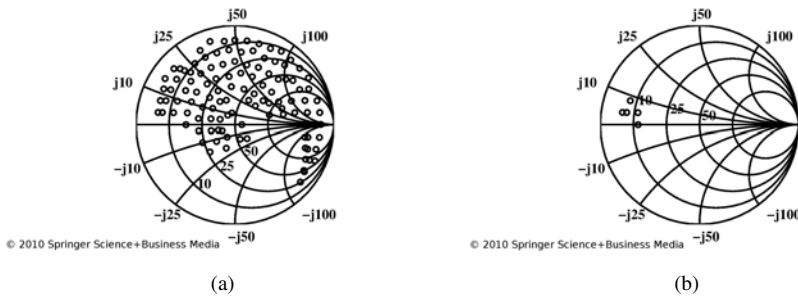


Fig 31. a) Measured load instability points without and b) with RC-sink [V, with kind permission from Springer Science+Business Media].

6 Summary

Now we will summarize the main points found out about supply modulated switching amplifiers. The focus will be on different design choices and circuit variations, which might affect the optimum operation of supply modulated switching amplifiers. First we will discuss the input side of the amplifier and then the output. Then some summary about the effects due to supply modulation and the bias line design will be made. In the end, some interesting notes and remarks will be made.

6.1 Changing nature of the input

The changes in input impedance in supply modulated switching amplifiers are considerably larger and more difficult to predict than in linear amplifiers. This is shown especially when a high input drive, necessary for a switching power amplifier, is applied at the gate of the device. The nonlinear input capacitance C_{gs} experiences high changes in effective value, which in turn generates distortion. Distortion changes the pulse width of the input signal and thus, changes the input signal phasing between transistor fingers in large periphery devices. The latter is shown to decrease the amplifier efficiency due to nonsimultaneous switching [II,V].

The changing nature of capacitors highlights both the necessity to model the devices in the most nonlinear regions so that we can simulate the correct operation of the switching amplifier and the importance of correct input signal timing. Although the majority of capacitance change in the pHEMT design in [II,V] was generated by nonlinear C_{gs} , there is another capacitance to take into account: the gate to drain capacitance that has a strong, supply dependent Miller effect as discussed in [VI]. It affects the device operation by causing a large and varying capacitive input impedance change and by gyrating the apparent capacitance at the gate to show partially as negative resistance. Further, the feedback capacitor provides a path for a strong second harmonic current injection from output to input. All variations send their own negative impact on the operation of the class E amplifier. The second harmonic modulates the duty cycle of the input signal, negative resistance exposes the amplifier to instability and input impedance change causes gain variations due to drive mismatch. The amount of negative resistance and impedance variation can be decreased by applying an AC-coupled

inductor in parallel to the feedback capacitor or by choosing a push-pull class E topology with cross-coupled feedback capacitors. The latter has the extra benefit of accurately cancelling out the input signal feedthrough from input to output. The remaining problem in both cases is the heavy second harmonic injection through feedback, which has to be eliminated with a separate second harmonic trap at the input [VI].

To improve stability at high frequencies, a wideband RC-sink was implemented in [V] to the gate of the tuned power amplifier. The RC-sink provided an improvement in amplifier stability, not only to the high frequencies but also close to carrier frequencies. In [V], the instability seen at the load-pull measurements was caused by the supply bias line and appeared as close to fundamental spurious tones. Surprisingly enough, when the load side was load-pulled, a more stable operation occurred when the RC-sink on the gate side was operational. This leads to the conclusion that the RC-sink has a considerable stabilizing effect also to the supply bias induced instability.

6.2 Different variations of tuned output circuit

The high-efficiency RF PAs have many times originated from cut-and-try type of designs that have been reanalysed to find the optimum tuning of the load network. This optimum design has then evolved, as in the case of class E amplifiers, to accompany several nonidealities which are, for example, the additions of different parasitics, nonlinearities and design value choices, such as low- Q . All of the added nuances have made the analysis difficult, more or less. Sometimes the analytical solutions of the analysis itself or solving the circuit component values may be impossible. Luckily, numerical solutions are still possible while it might require some patience from the designer to get them coded [VII].

In class E analyses, the nonlinear output capacitance and the combination of linear and nonlinear output capacitance have been in the interest of several researchers. Somewhat less has been said about the effect of feedback capacitance on the operation of class E. Further, the synthesis method of nonlinear feedback capacitance together with combined linear and nonlinear parallel capacitance in class E amplifiers [VII] is rather rare. Even though the analyses combining several nonidealities are at times awkward, some guidelines and rules of thumb can be laid out, as discussed next.

6.2.1 Continuum of different tuned output loads versus classes of operation

The output tuning is many times focused on a specific topology that delivers some level of harmonic tuning for high efficiency. It seems to be necessary that at least the second harmonic is somehow tuned, as shown in the cases of class E [5] and class J [6]. The further a designer goes into different of harmonic tunings, the more vague are the borders between different classes. Examples of amplifier turning from one case to another is the path from class C to class E (C-CE-E) [38], from class F via class E to class F^{-1} [5] and class F to class C [5].

It is true that the requirements of ideal operation of a certain class are many times difficult to achieve, because there are always some parasitics that affect the operation [IV, V]. As an example, one might mention the requirement of perfect open or short circuits in class F amplifiers. It is thus easier to say that ideal versions of different classes provide a reasonable starting point for the eventual tuning of the amplifier, as was the case in article [V].

6.2.2 Duty cycle in class E amplifiers

The choice of duty cycle plays an important role in the design of tuned and switching power amplifiers. Especially in the design of class E amplifiers, the duty cycle alters e.g. peak voltages, peak currents [VII] and maximum achievable operation frequency [71]. When the device reliability is considered, the peak voltages over the device are of great importance and a considerable reduction in peak voltage can be achieved by choosing D less than 0.5. According to [71], the optimum on-time ratio in terms of operation frequency is $D = 0.35$. By choosing this value, the normalized peak drain voltage over the device is decreased below $5 \cdot V_{dd}$ regardless of junction grading [VII]. The downside is that peak currents are increased, which means that larger periphery transistors are necessary and the required resistive load is decreased. The latter increases the importance of low parasitics in the output circuit and correct matching in order to maintain the wanted output power. These issues are discussed in the next section.

6.2.3 Low resistive load, Q and output design

Since the class E amplifier is not very sensitive to component variations [20], we are tempted to make the quick conclusion that the input design is a bigger problem than output load design. This is not exactly the case. The output load may withstand $\pm 10\%$ changes [20], for example, but this becomes a problem if the resistive output load has to be in the region of, say $4\ \Omega$. The $\pm 0.4\ \Omega$ margin for changes is small and requires a careful design of not only the resonator itself but of the output matching as well. The latter is an issue that has been mentioned briefly e.g. in [24]. Further, the parasitic resistances in the matching circuits can become a problem since they can be considerable when the resistive load is low. These low resistive loads are mainly met in high output power or low supply voltage devices.

Today's communication systems require large bandwidths which in turn reflect the necessity to create amplifiers with similar operation bandwidths. This affects the design of resonators and filters often by lowering their Q value. The lowest Q value in class E is around 1.7, which produces a limit to consider when designing the amplifier for wideband use. If the Q of 1.7 is enough and the design of the resonator is done, the design of output matching still remains. Quickly done, the output matching is designed to be a single stage L-match, which in the end can have a higher Q than the already designed resonator. In other words, the output matching should meet the bandwidth specification and thus, the resonator Q . Otherwise the matching can affect the tuning of the resonator and decrease the optimum size of output capacitance C_o in a class E amplifier. Too high C_o increases the power dissipation due to non-optimum switching [IV].

6.2.4 The design of high current resonator

In [V], the design of the parallel resonator in the case of class E⁻¹ led to wide line widths due to large flowing currents. This meant that the design had to be carefully evaluated with a EM field simulator in order to maintain correct operation and to minimize losses in the resonator. The large amplitude currents were also a reason why the capacitors in the resonator had to be divided into several fingers so that the ESR was decreased and the current capability was increased. The design of the resonator was not only physically unusual, but the placing of the DC-block was redesigned as well. By placing the DC-block under the parallel resonator, the block could be made smaller both in

value and size. Further, the currents flowing in the DC-block are smaller and the new positioning creates a trap circuit with the parallel resonator that can be used to improve close to carrier stability. Also, the DC-block is no longer in between the device and load, which reduces the ESR in the signal path. Additionally, the restrictions in the minimum size of $3/4$ turn inductor in the resonator meant that the inductor could not be made physically any smaller in [V], which in turn meant that the resonator Q was lowered.

6.3 Output tuning vs. supply modulation

The nonlinear output capacitance affects amplifier linearity and efficiency when supply is modulated. Considerable variations in V_{dd}/AM and V_{dd}/PM are found [VII] when supply voltage is lowered. The simulations show that parallel output capacitance varies not only V_{dd}/AM and V_{dd}/PM , but the efficiency of the amplifier varies as well [VII]. The higher the value of the grading coefficient, the larger are the changes in time constant while the supply is low. This results in higher losses at the drain.

However, to increase the low supply level efficiency [VII], it is possible to design the class E amplifier by lowering the design values of the supply level, the power level and resistive load in the design equations. While the efficiency of the amplifier can be increased with proper design value choices, the linearity is not improved by this [VII]. In devices with a hyperabrupt junction, the efficiency in low supply levels can be significantly improved by a specific choice of design values [VII]. Still, the supply modulated class E amplifier requires some additional linearization scheme or predistortion system to meet the linearity requirements of modern communication systems.

6.4 Supply bias line design

The supply bias inductor has a direct impact on bias modulation speed and therefore the optimal design of the bias line is important. In linear PAs the large bias inductor can be replaced by a $\lambda/4$ line, especially in high-power amplifiers, to reduce the loss caused by the ESR and to improve modulation speed. In some cases, it is impossible to implement the long transmission line due to layout size constraints or because the designed amplifier utilises second harmonic tuning, which is ruined by the second harmonic trap effect of a $\lambda/4$ line. Luckily, there is a possibility to make a decent compromise between a large inductor and long line by applying a combination of the two [III], as shown in

Section 4.2.2. With a combination structure, the high impedance bias line is achievable with a fraction of the original bias inductance and with a considerable reduction in bias line length. The bandwidth of combination structure is slightly larger than that of a $\lambda/4$ line while the size, ESR and modulation speed are something in between a large bias inductor and a $\lambda/4$ line.

One important benefit of a short bias line and attached inductor is the shift of both high impedance resonance and the second harmonic trap effect on higher frequency. If only a $\lambda/12$ line is used, the high impedance frequency is the third harmonic of the amplifier, while the natural trap effect falls into the fourth harmonic of the amplifier. This alone allows the combination bias line to be connected directly to the drain pin and the harmonic tuning necessary in classes E, F and J is possible without any fear of trap resonance. Further, the applied small inductor shifts the resonant frequencies to be noninteger multiples of each other, which helps even more in the design of a general type harmonic tuned amplifier.

6.5 Notes and remarks

6.5.1 Feedthrough and device modelling issues

The feedthrough from input to output has a significant effect on amplifier linearity at low supply levels. Variations in amplitude (V_{dd}/AM) and phase (V_{dd}/PM) when supply is low are largely caused by the input signal having a direct route through gate-drain capacitance C_{gd} [I]. This is a severe problem in EER, where the variations limit the dynamics of the transmitter and the wideband amplitude limited input signal shows as wideband distortion in the output [III]. Further, the signal feedthrough causes uncertainty in single tone efficiency measurements even when computationally eliminated from the efficiency calculations [I]. There are several approaches how to minimize the unwanted output tone, such as AC-coupled inductor in parallel with feedback, special DSP controlled drive attenuation function, feedforwarding the cancelling tone to the output, push-pull topology with cross-connected feedback capacitors and two DSP controlled parallel amplifiers that combine both feedthrough cancellation and peak amplifier operation.

Most of the device models are more or less directed to the design of linear amplifiers, where the modelling of input capacitance in large input swings [II, V], on-resistance in the linear region and knee effect are not so critical. If there is uncertainty in the modelling

of saturation current or the linear region, these can lead to unreliable simulation results where both the simulated output power and drain efficiency of switching power amplifiers are affected. The modelling of the dispersive output conductance of the devices can also have detrimental effects on the simulated efficiency and output power of a switching amplifier [III]. This conductance modelling can, in the worst case, be done with a fixed parallel RC-sink circuit at the output. This RC-sink may have a high time constant which in some models does not depend on the gate bias and thus, has a very low impedance in the off-state. The high time constant causes a considerable leakage in the off-state of the transistor and thus, ruins the simulated efficiency [III].

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ISBN 978-951-42-9835-6 (Paperback)

ISBN 978-951-42-9836-3 (PDF)

ISSN 0355-3213 (Print)

ISSN 1796-2226 (Online)

