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Jussi-Pekka Jansson

A STABILIZED MULTI-CHANNEL CMOS TIME-TO-DIGITAL CONVERTER BASED ON A LOW FREQUENCY REFERENCE

UNIVERSITY OF OULU GRADUATE SCHOOL;
UNIVERSITY OF OULU, FACULTY OF TECHNOLOGY,
DEPARTMENT OF ELECTRICAL ENGINEERING;
INFOTECH OULU

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A STABILIZED MULTI-CHANNEL CMOS TIME-TO-DIGITAL CONVERTER BASED ON A LOW FREQUENCY REFERENCE

Academic dissertation to be presented with the assent of the Doctoral Training Committee of Technology and Natural Sciences of the University of Oulu for public defence in OP-Pohjola-sali (Auditorium L6), Linnanmaa, on 9 November 2012, at 12 noon

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Abstract

The aim of this work was to improve the performance and usability of a digital time-to-digital converter (TDC) in CMOS technology. The characteristics of the TDC were improved especially for the needs of pulsed laser time-of-flight (TOF) distance measurement, where picosecond-level precision with a long µs-level measurement range is needed in order to approach mm-level measurement accuracy. Stability in the face of process, voltage and temperature variations, multiple measurement channels, alternative measurement modes, a high integration level, standard interfaces and simple usage were the main features for development.

The measurement architecture is based on counter and timing signal interpolation on two levels. The counter counts the full reference clock cycles between the timing signals, while a new recycling delay line developed in this thesis interpolates within the reference clock cycle. This technique utilizes a short delay line several times per reference clock cycle, which minimizes the interpolation nonlinearity. The same structure also makes the use of a low, MHz-level reference frequency possible, and thus only a crystal is needed as an external oscillator component. The parallel load capacitor-scaled delay line structure acts as the second, sub-gate-delay interpolation level. The INL does not accumulate in elements connected in parallel, and the load capacitance differences enable high, ps-level resolution to be achieved.

Four TDC circuits in 0.35 µm CMOS technology were designed and tested in the course of this work, of which the latest, a 7-channel TDC, is able to measure the time intervals between the start pulse and three separate stop pulses in one measurement and to resolve the pulse widths or rise times at the same time. In laser TOF distance measurement this functionality can be used when several echoes arrive at the receiver, and also to compensate for the detection threshold problem known as timing walk error. The TDC achieves 8.9 ps interpolation resolution within the cycle time of a 20 MHz reference clock using only 8 delay elements on the first interpolation level and 14 delay elements on the second. A measurement precision better than 9 ps was achieved without using result post-processing or look-up tables. This work shows that versatile, high performance TDCs can be created in standard CMOS technology.

Keywords: delay line interpolation, laser radar, reference recycling, time interval measurement, time-to-digital converter (TDC), walk-error compensation

Jansson, Jussi-Pekka, Stabiloitu, monikanavainen, matalataajuiseen referenssikelloon perustuva CMOS aika-digitaalimuunnin.
Oulun yliopiston tutkijakoulu; Oulun yliopisto, Teknillinen tiedekunta, Sähkötekniikan osasto; Infotech Oulu, PL 4500, 90014 Oulun yliopisto
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Tiivistelmä

Väitöskirjatyön tavoitteena oli parantaa CMOS-aika-digitaalimuuntimien suorituskykyä ja käytettävyyttä. Muuntimen ominaisuuksia kehitettiin erityisesti laseretäisyysmittauksen tarpeita ajatellen, missä millimetritason mittaustarkkuus laajalla mittausaluella edellyttää aika-digitaalimuuntimelta pikosekuntitason tarkkuutta mikrosekuntien mittausalueella. Stabiilius prosessiparametri-, jännite- ja lämpötilavaihteluita vastaan, useat mittauskanavat, useat mittausmoodit, korkea integraatioaste, standardoidut liitäntäväylät ja helppo käytettävyys olivat erityisesti kehityksen kohteina.

Suunniteltu mittausarkkitehtuuri koostuu laskurista ja kaksitasoisesta ajoitussignaali-interpolaattorista. Laskuri laskee kokonaiset referenssikellojaksot ajoitussignaalien välillä ja työssä kehitetty referenssiä kierrättävä viivelinjarakenne rekistereineen interpoloi ajoitussignaalien paikat referenssikellojaksojen sisältä. Referenssinkierrätystekniikka hyödyntää lyhyttä viivelinjaa useampaan kertaan kellojakson aikana, mikä minimoi epälineaarisuuden interpoloinnissa. Sama rakenne mahdollistaa myös MHz-tason referenssitaajuuden, jolloin matalataajuista kidettä voidaan käyttää referenssilähteenä. Toinen interpolointitaso koostuu rinnakkaisista kapasitanssiskaalatuista viive-elementeistä, mitkä mahdollistavat alle porttiviiveen mittausresoluution. Rinnakkaisessa rakenteessa elementtien epälineaarisuudet eivät summaudu, mikä mahdollistaa pikosekuntitason mittaustarkkuuden.

Väitöskirjatyössä suunniteltiin ja toteutettiin neljä aikavälinmittauspiiriä käyttäen 0,35 µm CMOS-teknologiaa, joista viimeisin, 7-kanavainen muunnin kykenee mittaamaan aikavälin useampaan pulssiin yhdellä kertaa sekä voi selvittää samalla pulssien leveydet tai nousuajat. Laseretäisyysmittauksessa monikanavaisuutta voidaan käyttää kun useita kaikuja lähetetystä pulssista saapuu vastaanottimeen sekä kompensoimaan mittauksessa esiintyviä muita virhelähteitä. Käytettäessä 20 MHz:n kidettä referenssilähteenä muunnin saavuttaa alle 9 ps:n interpolointiresoluution ja tarkkuuden ilman epälineaarisuudenkorjaustaulukoita. Työ osoittaa, että edullisella CMOS-teknologialla voidaan toteuttaa monipuolinen ja erittäin suorituskykyinen aika-digitaalimuunnin.

Asiasanat: Aika-digitaalimuunnin, aikavälinmittaus, laseretäisyysmittaus, referenssinkierrätys, viivelinjainterpolointi

Acknowledgements

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List of terms, symbols and abbreviations

The terms describing the performance of the measurement equipment are defined according to the IEEE Standard Dictionary of Electrical and Electronics Terms (IEEE 1996):

Accuracy is the degree of correctness with which a measured value agrees with the true value

Differential nonlinearity is the difference between a specified code bin width and the average code bin width

Integral nonlinearity is the maximum nonlinearity (deviation) over the specified operating range of a system

Jitter refers to the short-term deviations of the significant instants of a signal from their ideal positions in time

Precision is the quality of coherence or repeatability of measurement data, customarily expressed in terms of the standard deviation of the extended set of measurement results from a well-defined (adequately specified) measurement process in a state of statistical control

Random error has unknown magnitudes and direction and varies with each measurement

Resolution is the least value of the measured quantity that can be distinguished

Systematic error remains constant in magnitude and direction throughout the calibration process

ADAS	advanced driver assistance systems
ADC	analogue-to-digital converter
ALU	arithmetic logic unit
AWG	arbitrary waveform generator
BiCMOS	bipolar-CMOS, a semiconductor technology containing both bipolar and CMOS transistors
BIST	built-in self-test
CLK	clock
CMOS	complementary MOS, a semiconductor technology containing both NMOS and PMOS transistors
CP	charge pump
CSN	chip select negative
CTR	counter

DAC	digital-to-analogue converter
DLL	delay-locked loop
DNL	differential nonlinearity
EN	enable
FPGA	field-programmable gate array
GaAs	gallium arsenide
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	integral nonlinearity
INT1	first interpolation level result
INT2	second interpolation level result
LSB	least significant bit
LUT	look-up table
MDLL	multiplying delay-locked loop
MISO	master in, slave out
MOSI	master out, slave in
NRE	nonrecurring engineering
PD	phase detector
PET	positron emission tomography
PVT	process, voltage, temperature
QFN	quad flat no-leads package
REFCLK	reference clock
rms	root mean square
SPI	serial peripheral interface
SYNC	synchronization block
TAC	time-to-amplitude converter
TCXO	temperature compensated crystal oscillator
TDC	time-to-digital converter
TEKES	Finnish Funding Agency for Technology and Innovation
TOF	time-of-flight
XTAL	crystal

c	velocity of light
C	capacitance
I	current
M	recycling factor
Q_e	quantization error

$R\Phi n$	register value of time sample n
ST_{int}	result of start interpolator
SP_{int}	result of stop interpolator
T	actual input time
T_{INT}	interpolation time interval
T_m	measurement result of TDC
T_{SPn}	time interval between start and stop pulse n
T_w	pulse width
T_r	rise time
V_{ctrl}	control voltage

σ	standard deviation
σ_{clk}	rms jitter of reference clock
σ_{inl}	standard deviation of integral nonlinearity
σ_{start}	rms jitter of start signal
σ_{stop}	rms jitter of stop signal
σ_{tdc}	rms TDC internal jitter
σ_q	rms quantization error
σ_{rms}	rms standard deviation of the single-shot precision of a TDC
μ	average value
τ_1	resolution of the first interpolation level
τ_2	resolution of the second interpolation level
τ_{clk}	period of the internal clock
τ_e	delay element basic delay
τ_{int}	interpolation resolution
τ_{ref}	period of the reference clock
τ_{tot}	delay element total propagation delay
Φn	interpolation time sample n

List of original publications

I Jansson J-P, Mäntyniemi A & Kostamovaara J (2005) A Delay Line Based CMOS Time Digitizer IC with 13 ps Single-shot Precision. Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'2005). Kobe, Japan, 23–26 May 2005, 5: 4269–4272.

II Jansson J-P, Mäntyniemi A & Kostamovaara J (2006) A CMOS Time-to-Digital Converter with better than 10 ps Single-Shot Precision. IEEE Journal of Solid-State Circuits, 41(6): 1286–1296.

III Jansson J-P, Mäntyniemi A & Kostamovaara J (2009) Synchronization in a Multi-level CMOS Time-to-Digital Converter. IEEE Transactions on Circuits and Systems I: Regular Papers. 56(8): 1622–1634.

IV Jansson J-P, Mäntyniemi A & Kostamovaara J (2009) Multiplying Delay Locked Loop (MDLL) in Time-to-Digital Conversion. Proceedings of International Instrumentation and Measurement Technology Conference (I2MTC'2009). Singapore, 5–7 May 2009: 1226–1231.

V Jansson J-P, Koskinen V, Mäntyniemi A & Kostamovaara J (2012) A Multichannel High-Precision CMOS Time-to-Digital Converter for Laser-Scanner-Based Perception Systems. IEEE Transactions on Instrumentation and Measurement. 61(9): 2581–2590.

The author wrote the above papers and was responsible for the practical work lying behind them. The work was supervised by Prof. Juha Kostamovaara, whose ideas, comments and hints helped in the completion of the whole work.

Contents

1 Introduction

1.1 Background

A time-to-digital converter (TDC) measures the time interval between two or more timing signals and presents the result in a digital form. The main inputs, the electrical timing signals, define the beginning and end of the measurement and are thus often called the start and stop signals, respectively. The measurement result, a digital word, is the main output of the TDC.

High resolution time-to-digital conversion is used in many applications. Measurement devices such as oscilloscopes and logic analysers commonly utilize TDCs (Park & Park 1999), and experiments in high energy physics, such as those concerned with particle lifetimes, flight times and identification, are largely based on high precision time interval measurements (Porat 1973, Myllylä 1976, Brockhaus & Glasmachers 1992). The TDC is a basic block in laser time-of-flight (TOF) rangefinders (Goldstein & Dalrymble 1967, Kostamovaara 1986, Määttä 1995) and can be used to characterize the timing and performance parameters of high speed circuits, i.e. jitter, skew, clock-to-output, setup times, hold times, ageing and clock control (Wilstrup 1998, Rivoir 2006, Abas *et al.* 2007, Chen *et al.* 2011, Bowman *et al.* 2011). TDCs are used in telecommunications for clock recovery (Park & Kim 1999), phase and frequency demodulation (Chu 1988, Rahkonen & Kostamovaara 1994) and all-digital frequency synthesis (Staszewski *et al.* 2006, Tonietto *et al.* 2006), for example. Medical imaging techniques such as time-of-flight positron emission tomography (TOF-PET) also make use of TDCs (Moses 2003, Conti *et al.* 2005). Analogue-to-digital conversion (ADC) can be performed over the time domain with analogue-to-time and time-to-digital converters (Huang & Sechen 2009, Daniels *et al.* 2010, Townsend *et al.* 2010). Other new applications to have emerged recently are single photon counting (Niclass *et al.* 2008) and fluorescence measurements (Schwartz *et al.* 2008).

Interest in TDCs is increasing, for a number of reasons. Picosecond-level measurement performance with standard, cheap technologies has made new applications possible and profitable. New small line width circuit technologies with a low operating voltage weaken the characteristics of traditional analogue signal processing but improve the performance of the signal processing in the time domain. The analogue circuit blocks used in frequency synthesis, for example, can in many cases be replaced with digital blocks including a TDC.

The numbers of TDC-related articles contained in the IEEE (Institute of Electrical and Electronics Engineers) *Xplore* digital library in given years are shown in Fig. 1, the identification criterion being the occurrence of one of the search terms listed in the insert in either the title, abstract or index. It should be mentioned in this connection that one of the articles included in this thesis (Paper II) is the second most referenced TDC architecture publication of all time, having a total of 67 citations in the IEEE library and totally 111 citations according to the Google Scholar (August 2012).

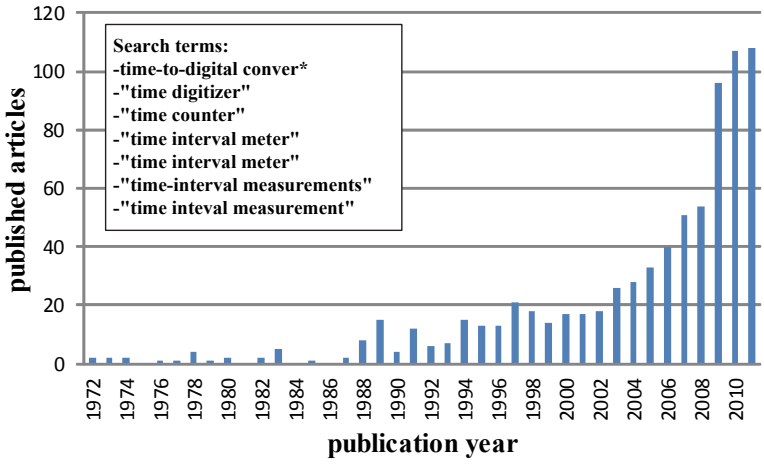

Fig. 1. TDC-related articles in the IEEE *Xplore* digital library.

Electronic time interval measurement has been studied at the Electronics Laboratory of the University of Oulu since the late 1970s. Many measurement architectures have been developed and a large number of master's, licentiate's and doctoral theses have been published concerning time interval digitization. Nuclear science and laser distance measurement have been the main applications for the TDCs designed in the laboratory (Myllylä 1976, Kostamovaara 1986, Rahkonen 1993, Määttä 1995, Räisänen-Ruotsalainen 1998, Mäntyniemi 2004, Nissinen 2011).

The aim of this work is to continue the laboratory's TDC development work by improving the performance of time-to-digital conversion. Measurement precision is perhaps the main performance parameter, but calibration-free operation, operation with several timing signals, suitability for serial production,

user-friendliness, versatility, integration of auxiliary functions, size and power consumption have also been taken into account in this work.

1.2 Contributions and structure of the thesis

The first mission in this work was to reach a better than 10 ps time interval measurement precision within a long measurement range. The goal was achieved with a TDC that included a counter and a two-level interpolation architecture in 0.35 μm CMOS technology. The counter is responsible for the measurement range, the first interpolation level creates even-sized time samples with a new developed delay line structure which makes low integral nonlinearity (INL) possible, and the second interpolation level continues the interpolation with a parallel load capacitor scaled delay line structure which is able to create linear time samples with better than 10 ps resolution.

The second contribution is the proposal for a means of utilizing a low-frequency reference source. TDCs usually require higher reference frequencies, from several tens of MHz up to the GHz level. With a high reference frequency the interpolation region becomes smaller, in which case linear high resolution interpolation is easier and the TDC can be small in size. The power consumption of a high frequency oscillator can be high, however, and its costs can be much greater than those of the actual TDC. It is shown here that the reference frequency does not need to be high in order to achieve high precision and stable operation in varying environmental circumstances. The reference recycling technique developed here employs a short delay line several times per reference clock cycle and the resulting TDCs are able to use reference sources of only few megahertz. Finally, the oscillator was also integrated into the circuit, so that only a crystal is needed as an external component, which further reduces the costs and size of the device.

The third contribution is the designing of a TDC especially for the needs of pulsed laser TOF radar, within the Minifaros Project, part of the 7th Framework Programme funded by the European Commission (www.minifaros.eu), The aim of this project was to develop a low cost, lightweight and miniature laser scanner sensor (prototype shown in Fig. 2) for vehicular environmental perception (Fürstenberg & Ahlers 2011). The resulting TDC circuit, presented in detail in Chapter VI, measures the time interval between transmitted and received laser pulses, and uses this information to determine the distance from the target. The application demands several parallel measurement channels in order to locate a

number of adjacent echo-pulses, and also for walk-error compensation, as will be explained later. The 7-channel TDC designed here can provide the time intervals between the start and three successive stop pulses and the widths or rise times of the stop pulses. There are also several new structures that improve the usability of the circuit. The circuit can be tested at the wafer level without precise external time delays by means of a built-in self-test (BIST), a serial peripheral interface (SPI) provides a standard data link for the user, and the final measurement results are calculated within the TDC, which reduces the data flow out of the circuit and minimizes external data processing. The TDC is also able to handle situations in which the stop signals arrive before the start.

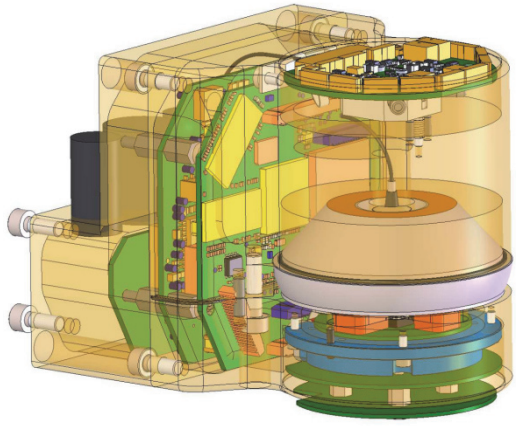

Fig. 2. The prototype laser scanner produced in the Minifaros Project.

The fourth mission was to improve synchronization in the two-level interpolation architecture. As explained in Chapter V, the two-level interpolation architecture requires synchronization delays between the operations of the different resolution interpolators in order to render the results received from the levels compatible, and this delay needs to be compensated for in the asynchronous timing signal path. Non-ideal silicon wafers and circuit fabrication, however, will create mismatched propagation delays even in identical structures. Mismatch in the synchronization delays will shift the interpolation signals out of the interpolation region, creating error in the measurements. The delay offset can be cancelled out with external delay adjusting structures, which need to be calibrated externally for each circuit. The solution proposed here is a widening of the region covered by the second interpolation level. With only a few extra delay elements and registers

the second interpolation level can have an offset in its interpolation signals which does not detract from the performance of the device.

The thesis is composed of a summary part comprising 8 chapters and a publication part consisting of a total of 5 internationally peer-reviewed original publications. The summary part is organized as follows. Chapter 2 goes through the general TDC-related terms and factors affecting the measurement performance, Chapter 3 presents the most common time interval digitization methods and structures introduced in the literature, and Chapter 4 gives a short review of the original publications included in the thesis. Chapter 5 presents the structures developed during this work in order to make high-performance measurement possible, Chapter 6 presents the architecture and measurement results of the multi-channel TDC developed here especially for the needs of laser TOF distance measurement, including all the ideas and structures developed for it, Chapter 7 discusses and compares different TDC realizations, and finally Chapter 8 summarizes the findings of the thesis.

2 Time interval measurement uncertainty

The result (output) of an *ideal* time-to-digital converter should be exactly correct with any input time interval. The number of bits in the measurement result will be enormous due to the infinite resolution and unlimited maximum measurement time interval. External variables such as temperature changes, supply voltage variation and noise should have no influence on the result. *Real* time interval measurement devices have always weaknesses which introduce error into the measurement result and detract from measurement performance. This chapter presents the main terms which are used when describing TDCs and are needed in order to understand why the measured result is always an approximation of the true value.

Resolution and the equivalent term LSB (least significant bit) are used to describe the smallest time interval that the TDC can fractionate. The result given by the TDC (as a digital word) must be multiplied by the LSB value in order to reconstitute the measured time interval T_m.

When the same time interval T is measured many times with a real TDC, several adjacent results usually turn up, as in Fig. 3, for example. The measured values T_m tend to vary around the mean value with a certain statistical variation that can be described with the standard deviation value σ, usually called the precision of the measurement. The precision usually depends on the time interval to be measured, and the maximum and root-mean-square (rms) values of the precision within a certain measurement range should be indicated when describing a TDC. Precision is very good performance parameter when comparing TDCs, because it includes the effects of all the *random* error sources. It should already be noted at this point that a small measurement LSB (high resolution) does not automatically mean good measurement precision.

The deviation of the mean measured value from the correct value can be called the averaged accuracy, or simply the accuracy, as in Fig. 3. Accuracy error results from *systematic* error sources, which can create a constant offset, or linearity error in the resulting measurement, which can fluctuate with the time interval. This constant offset can be easily subtracted from the result, because it is always the same, but a varying linearity error can be removed from the result only by means of look-up tables (LUT). The sources of error responsible for measurement uncertainty are presented in the following sections.

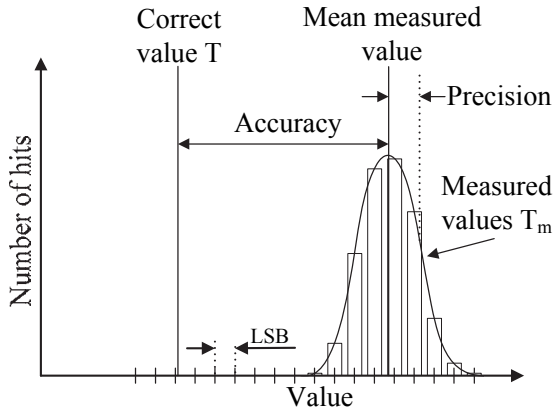

Fig. 3. Measurement uncertainty.

2.1 Quantization error

As in all analogue-to-digital converters (ADC), quantization error is a result of finite measurement resolution. The manner in which quantization creates measurement error and the variation in the amount of this error with the time interval are shown in Fig. 4. The asynchronous timing signal (start or stop) can arrive in any moment within the LSB, which causes the quantization error, Q_e, to be in the region $(0 \leq Q_e < 1) \times$LSB with an rms error value of σ_q = LSB/$\sqrt{12}$. In TDCs based on a single conversion, Fig. 4 a), this is the final effect of the quantization noise. The start signal, for example, can propagate in a delay line and the stop signal will record the state of the delay line (Staszewski *et al.* 2006, Henzler *et al.* 2008, Lee *et al.* 2008). Fig. 4 b) shows the quantization error in a situation where both the timing signals, start and stop, are asynchronous with respect to the resolution of the measurement. The error region will now be $(-1 < Q_e < 1) \times$LSB with a rms value of σ_q = LSB/$\sqrt{6}$ (Hewlett Packard).

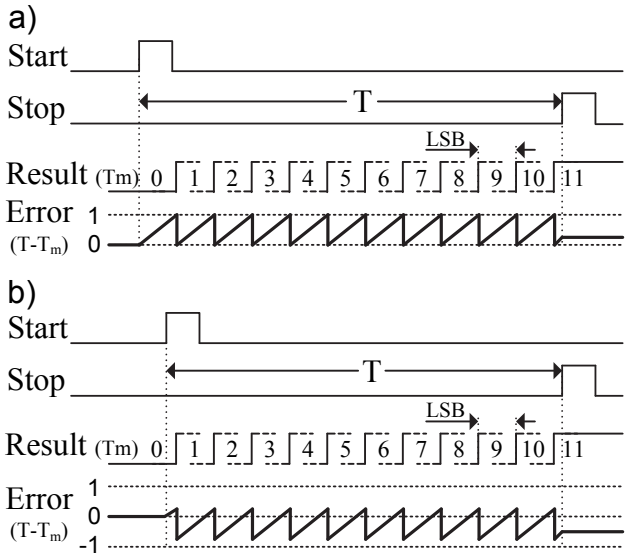

Fig. 4. Quantization error with a) one, b) two asynchronous timing signal(s).

2.2 Nonlinearity

Linearity error describes the deviation of the output value (measurement result) from the input value (time interval). In a linear device the output changes in direct proportion to the input value, yielding a straight line as the output-versus-input graph.

Measurement nonlinearity results from mismatch in the measurement resolution. A nonlinear current or capacitor in analogue measurement structures, nonhomogeneity in silicon process parameters and processed layout and systematic noise sources, for example, can create static differences with respect to the measurement LSBs, which interfere with the smooth growth of the measurement result with the time interval. The manner in which variation in the resolution of the measurement creates nonlinearity error is illustrated in Fig. 5. The differential nonlinearity (DNL) is the deviation of a single quantization step from the ideal value of 1 LSB. The LSBs and the errors within them are usually interconnected and interdependent, which means that the nonlinearity accumulates as the time interval becomes longer. The accumulated linearity error is called the integral nonlinearity (INL). The maximum INL defines the maximum

measurement error due to nonlinearity. As presented later on, the standard deviation of the INL, σ_{inl}, can be used to describe the effect of INL on the rms precision.

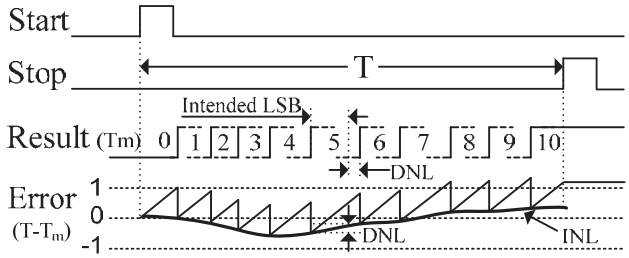

Fig. 5. Differential and integral nonlinearity.

2.3 Stability

The stability of a measuring instrument describes how its metrological properties vary with changes in the environment and with time. Instability in TDC measurement results can occur due to changes in temperature, operating voltages and/or reference clock frequency, for example. An example of measurement error occurring when environmental changes lead to a change in measurement resolution is shown in Fig. 6. The measurement error usually increases smoothly with the time interval, and nonstability is often described as gain error.

A TDC needs a stabilization system in order to find out and adjust to the LSB in different circumstances. The measurement resolution has to be known in order that the measured digital output word should correlate with the true time interval. Usually an external reference clock, e.g. a temperature-compensated crystal oscillator (TCXO), is used for stabilization, i.e. to minimize the effects of PVT (process, voltage, temperature) variations. The propagation delay of adjustable delay elements can be locked to a reference clock cycle time (Rahkonen & Kostamovaara 1993), or else the prevailing resolution can be assessed by processing the result using a period estimation technique (Staszewski *et. al* 2006) or a separate calibration cycle (Nissinen *et al.* 2003).

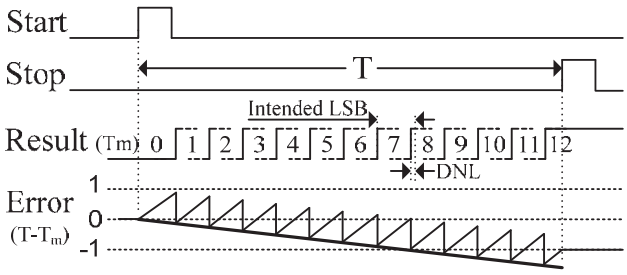

Fig. 6. Stability error.

2.4 Jitter sources

Random jitter sources worsen the statistical variation in the measurements obtained (precision). Noise in the supply and bias voltages and thermal noise in the TDC measurement structure create random time error in the signals participating in the measurement. Jitter can also accumulate in the time samples during measurement, as shown in Fig. 7. The rms effect of this inherent jitter on measurement precision can be denoted with σ_{tdc}.

The main input signals entering the TDC, the reference clock and the start and stop signals also contain jitter. The rms jitter from the reference clock, σ_{clk}, can be estimated from its phase noise spectrum (Hajimiri & Lee 1999). At short measurement time intervals the effect of clock jitter is low, usually below 1 ps with good oscillators, but at longer time intervals (>1 ms) the reference clock jitter starts to affect the measurement precision dramatically (Keränen *et al.* 2011). Jitter in the start and stop timing signals (σ_{start} and σ_{stop}) is not actually a characteristic of the TDC, but is present in the precision value when the same time interval is measured many times over.

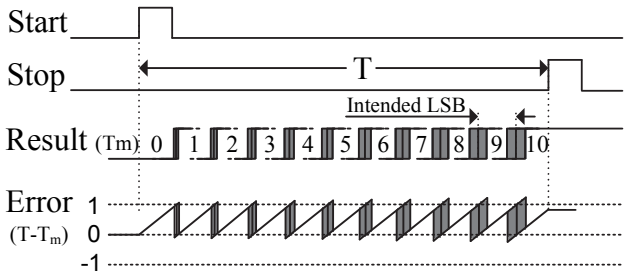

Fig. 7. Accumulating jitter in measurement time samples.

3 Time-to-digital conversion methods

Many time interval measurement methods and variations within them have been presented in the literature, and they can also be categorized in various ways. Analogue measurement methods make use of charges, currents and voltage differences, while digital methods are based on fast, discrete state changes. The design platform/technology can be FPGA, CMOS or BiCMOS, or else the TDC can be constructed from discrete components. Some TDCs use just a counter to digitize the interval between the timing signals (start and stop), which easily provides long measurement range. Some TDCs use only a single high resolution conversion structure, which allows high precision but lacks the necessary dynamic measurement range. The third solution is to use both of the above, a combination of a counter and high resolution timing signal interpolators, which is also known as the Nutt method (Nutt 1968).

In the Nutt method, as presented in Fig. 8, a counter, CTR, counts the reference clock edges between the timing signals and is responsible for the measurement range. Counting is enabled by the start signal and disabled by the stop signal. Usually two interpolators, one for each timing signal, locate the timing signals within the reference clock cycle time τ_{ref} with much higher resolution τ_{int}. The interpolators indicate the time delay of the timing signals relative to the reference clock edges, so that their maximum measurement range is τ_{ref}. The actual reference edge used for the interpolation depends on the architecture and can also be the next edge after the timing signal. An estimate, T_m, of the real time interval T consists of the counter result CTR and the digitized interpolation results of the start and stop signals, ST_{int} and SP_{int} respectively:

$$T_m = CTR \times \tau_{ref} + (SP_{int} - ST_{int}) \times \tau_{int}. \quad (1)$$

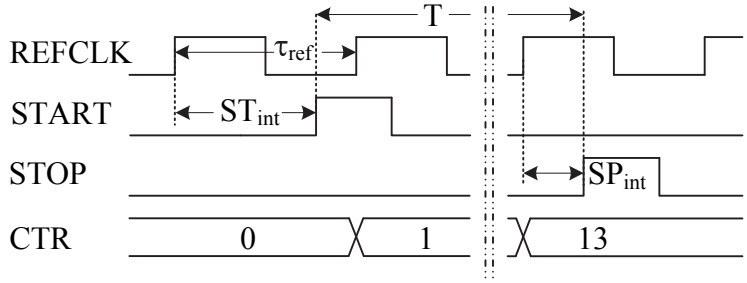

Fig. 8. Timing diagram of the Nutt method.

The Nutt method is usually used in time digitizers because it entails several benefits. The binary counting method of the counter provides an effective way of measuring long time intervals, and the measurement range can be extended simply by adding more bits to the counter. The measurement precision of a Nutt-based TDC worsens at time intervals longer than the reference clock cycle time, but only due to the reference source jitter, which can be very small. The measurement range of the interpolator (high resolution measurement unit) is only the reference clock cycle time, and it needs to be linear only in that region.

The Nutt-based TDCs are linear by nature. When the same time interval is measured many times and the timing signals are asynchronous with respect to the reference clock, these signals will also hit upon different locations within the reference clock period. The effects of static error sources, quantization error and measurement nonlinearity differ in every measurement and average out in the result if the same time interval is measured many times. In other words, the nature of the quantization and nonlinearity error sources changes from that of an accuracy problem to that of a precision problem. Only the static offset in the result persists when averaging, and that can easily be subtracted from the result.

In a Nutt-based measurement architecture the rms precision of the TDC, σ_{rms}, is a compound of the error sources presented in Chapter 2: the rms quantization error σ_q, the standard deviations of the integral nonlinearities in the start and stop interpolation channels, $\sigma_{inl\text{-}st}$ and $\sigma_{inl\text{-}sp}$ respectively, the rms value of the random inherent TDC jitter, σ_{tdc}, the rms reference clock jitter, σ_{clk}, and the rms jitter in the input timing signals, σ_{start} and σ_{stop}. When the error sources are not correlated their effects can be summed:

$$\sigma_{rms} = \sqrt{\sigma_q{}^2 + \sigma_{inl-st}{}^2 + \sigma_{inl-sp}{}^2 + \sigma_{tdc}{}^2 + \sigma_{clk}{}^2 + \sigma_{start}{}^2 + \sigma_{stop}{}^2}. \quad (3)$$

When using averaging, the number of measurements needed per time interval depends on the desired precision, the improvement in precision being inversely proportional to the square root of the number of averaged results. The precision without averaging may be 10 ps, for example, but it can be reduced to 0.1 ps by measuring the same time interval 10 000 times.

Several measurement blocks, a counter and two interpolators are needed in the Nutt method, unless the same interpolator can measure both of the timing signals. The measurement architecture, which includes several measurement levels, such as the counter and an interpolator, always needs a synchronization structure as well in order to achieve the correct overall result. The synchronization issue will be discussed in Chapter 5.

This chapter presents the mainstream time digitizing architectures. These can be used as stand-alone converters which directly digitize the time interval between the start and stop signals, but more often the high resolution structures (other than in the counter method) are used as interpolators in the Nutt method, and then they actually measure the interval between the timing signal (start or stop) and the reference signal, as presented in Fig 8. The referenced TDC related to the measurement method is marked with (N) if the Nutt method is used. Precision-based comparisons between architectures would be convenient and highly meaningful, but often this parameter is not reported at all in the literature. The performance and characteristics of the TDCs implemented here are discussed in Chapter 7.

3.1 The counter method

The easiest way to measure time digitally is probably to use a reference clock of known frequency and a counter. The counter result states how many reference clock periods fit within the measurement time interval when the counting is enabled between the start and stop signals. The counter method provides a large linear dynamic range and good stability (Porat 1973), the structure of a counter-based TDC is straightforward and the measurement range can be extended easily by adding a few logic gates and registers.

The measurement resolution in the counter method depends on the counter frequency. One nanosecond resolution has been achieved with a 0.5 μm CMOS operating at a frequency of 1 GHz (Veneziano 1998), and 417 ps resolution with a 2.4 GHz reference clock in GaAs technology (Gao & Partridge 1991). The power consumption of a pure counter method is high because the capacitive loads in the

counter are driven with a high frequency. Averaging can also be used to improve the precision.

3.2 Time-to-amplitude converter (TAC)

A time-to-amplitude converter (TAC) converts the measurement time interval first to a corresponding analogue voltage, which can then be digitized with an analogue-to-digital converter (ADC) (Henebry & Rasiel 1966, Porat 1973) or time stretching method (Nutt 1968). The analogue voltage can be created by (dis)charging a capacitor (C1 in Fig. 9) during the time interval with a constant current (I1 in Fig. 9). In the time stretching method, as presented in Fig. 9, the analogue voltage is discharged with a much smaller current (I2) after the stop signal and the stretched time interval is measured by enabling a counter during this time.

A 0.8 µm BiCMOS dual-slope time stretching converter (N) interpolates the cycle time of a 100 MHz reference clock with 32 ps resolution and better than 30 ps precision (Räisänen-Ruotsalainen *et al.* 2000). A resolution of 1 ps with a 100 MHz clock and 1 ms measurement range was obtained using a two-stage stretching method (Kalisz *et al.* 1987) with discrete components and a microprocessor (N), but the jitter level was about 5 ps and the linearity error 10 ps, so that the benefit gained from the high resolution was only minor. A pulse stretching-based 0.35 µm CMOS TAC (N) was shown to measure time intervals of up to 250 ns with 50 ps resolution (Chen *et al.* 2006) using a 80 MHz reference clock, while an integrated 1.2 µm CMOS TAC-ADC combination achieved a resolution of 107 ps within a measurement range of 8–24 ns (Gerds *et al.* 1994). A TAC-ADC combination constructed with discrete components and FPGA (N) was even able to achieve 0.1 ps resolution and 1.8 ps precision with a 200 MHz reference clock and had a wide, programmable measurement range (Keränen *et al.* 2011).

Digital measurement methods are usually preferred because analogue converters are more sensitive to the ambient temperature, are more susceptible to external disturbances, consume more power and are more difficult to realize in modern technologies. The time stretching method has also a long conversion time. The primary reason why analogue converters are still considered, however, lies in their superb resolution capability.

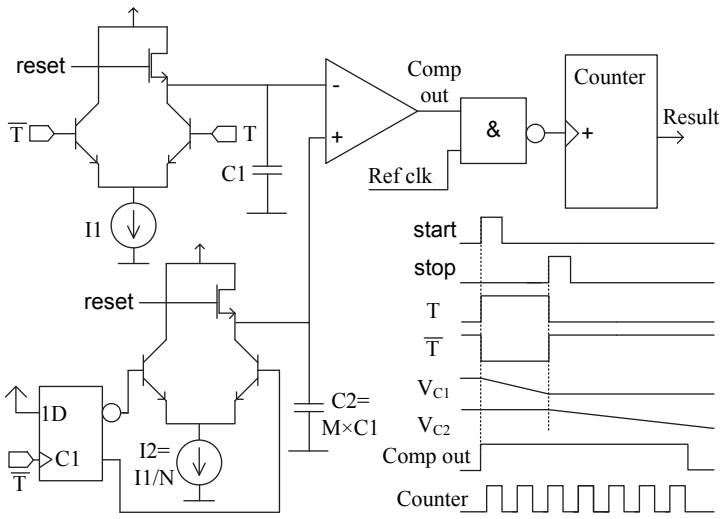

Fig. 9. An analogue dual-slope time stretching-based time-to-digital converter.

3.3 Delay line-based measurement methods

The basic construction block in a digital time digitizer is usually called a delay element. It is a digital gate in which the propagation delay is controlled or measurable. Delay elements can be connected in several ways to form delay lines for time digitizing (Rahkonen & Kostamovaara 1993).

3.3.1 Delay line with successive elements

The simplest delay line consists of identical delay elements, e.g. buffer-type gates, placed one after another, as presented in Fig. 10. The signal which propagates through the delay line generates time samples for the delay element outputs with an even time delay. The start signal can propagate in the delay line and the stop signal can register the state of the delay line, which reveals how many element delays there were between the timing signals. In timing signal interpolation the reference signal usually propagates in the delay line and both timing signals (start and stop) record the state of the delay line.

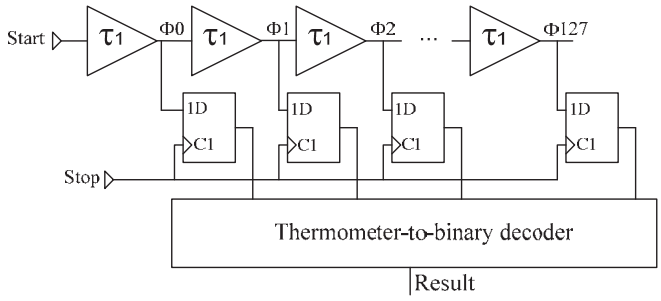

Fig. 10. A delay line with successive elements.

The measurement resolution with successive elements depends mainly on the circuit technology and the structure of the delay elements. The buffer delay is about 250 ps in 0.35 µm CMOS technology and around 40 ps in 90 nm CMOS. The propagation delay increases if the element contains functions such as delay adjustability, for example, to stabilize the delay at different temperatures. Then about 500 ps resolution can be achieved in 1.2 µm CMOS over a wide temperature range (Rahkonen & Kostamovaara 1993). When the delay elements in a 0.8 µm BiCMOS technology were connected to form a ring oscillator 125 ps resolution was obtained with a 500 MHz reference clock (N) (Herve & Torki 2002).

Since an inverter is the simplest logic component, the best resolution can probably be achieved when inverter-type elements are used. One disadvantage is that the delay line forms successive rising and falling edges, which makes the resolution inconstant, in addition to which the delay difference fluctuates with temperature. The problem can be solved by using a differential delay line in which two parallel inverters form rising and falling edges at every step and only the rising edges are used for time sample generation, for example. This structure has been used in the present work and also in other high resolution TDCs (Staszewski *et al.* 2006, Henzler *et al.* 2008). The cross-coupled inverters between the differential outputs in Fig. 11 maintain the opposite polarity of the signals in long delay chains. A differential inverter-based delay line in 90 nm CMOS technology creates time samples with ~20 ps resolution and can cover a 640 ps measurement range (Staszewski *et al.* 2006).

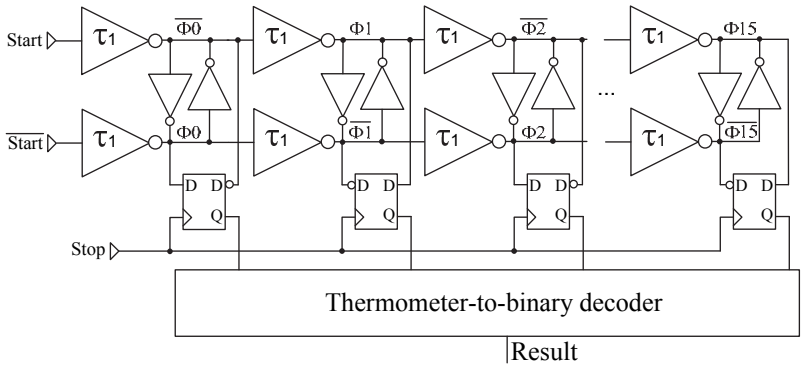

Fig. 11. Differential successive delay line.

Several methods have been presented for improving the LSB below the unit delay of a delay element. An on-chip RC delay line creates 4 time samples from the timing signal as well and records the state of the delay line, allowing 24.5 ps resolution and 22.4 ps precision to be achieved in 0.25 µm CMOS with a 320 MHz reference clock (N) (Mota *et al.* 2000). Resistors were used in the delay line, as shown in Fig. 12, to divide the differential inverter-based delay so that 4.7 ps resolution and 3.3 ps precision could be achieved in 90 nm CMOS when measuring over a 600 ps range (Henzler *et al.* 2008). The measurement method with successive elements is used as the first level in multi-level measurement structures in many TDCs, and was also used for this purpose here.

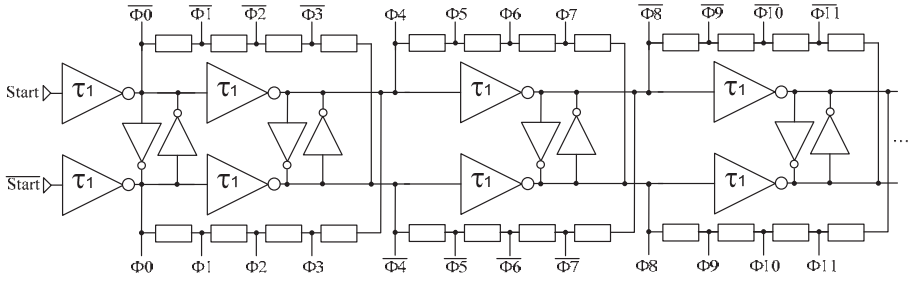

Fig. 12. A successive delay line with resistors.

Measurement with a successive delay line can be fast (flash-type), because the result is ready as soon as the measurement signals have arrived and the raw measurement data in the thermometer code are decoded to binary format. The size

of the digitizer increases with the measurement range and resolution, however, and a delay element and register are needed for every time sample. For example, if a high performance technology with 10 ps resolution were to interpolate the 10 ns period of a 100 MHz reference clock, 1000 delay elements and registering flip-flops would be needed. Another problem arises from the nonlinearity in the delay line. The delay mismatch of individual elements accumulates as the elements are placed one after another. Thus the measurement error can be large, especially in long delay lines (Toifl *et al.* 1999).

3.3.2 The Vernier-based measurement method

The Vernier time measuring technique (Baron 1957) utilizes two delay generators having a small time difference, which corresponds to the resolution (LSB). At first the Vernier principle was realized with two startable oscillators having a slightly different oscillation frequency, the slower-frequency oscillator being enabled by the start signal and the faster one by the stop signal. The time samples of the faster oscillator caught those of the slower one up in every oscillation period. Measurement was complete when the oscillators produced time samples at the same time and the number of oscillations up to this point revealed the measurement time interval. A resolution of 1 ps with a 1 µs range was achieved with an integrated bipolar gate array and two external oscillators with a clock rate of up to 700 MHz (Otsuji 1993).

In integrated circuits the Vernier principle is usually realized as presented in Fig. 13, with two separate delay lines having slightly different delays (Hoppe 1982). When the start signal propagates in the slower delay line and the stop signal in the faster delay line, the stop signal catches up with the start signal after a certain number of propagation steps. The number of propagated delay elements before the coincidence is multiplied by the delay difference between the elements (resolution) to obtain the measurement time interval. A Vernier TDC with delay lines in 0.7 µm CMOS can reach a resolution of 30 ps and a precision of 20 ps over a dynamic range of less than 4 ns (Dudek *et al.* 2000), while an integrated Vernier-based TDC in 0.35 µm CMOS with a counter and two ring oscillators (N) having a slightly different oscillation frequency has 37.5 ps resolution and 39 ps precision within an input range of over 50 ns with a 55 MHz reference clock (Chen *et al.* 2007). A Vernier-based interpolation architecture made with FPGA (N) was shown to measure a long 45 s range with 100 ps resolution using a 100

MHz reference clock (N). The TDC concerned achieved 70 ps precision using INL look-up tables (Szplet *et al.* 2000).

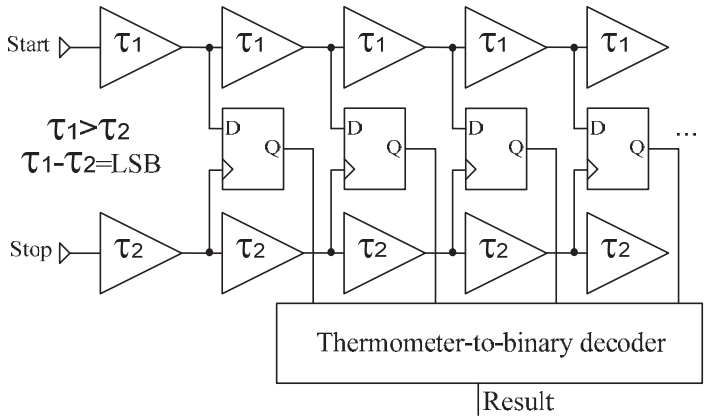

Fig. 13. A converter based on the Vernier principle.

In the Vernier method the faster time sample generator catches up with the slower one with a certain resolution at every propagation step, which can lead to a long conversion time. The amount of jitter increases in such delay lines, especially in long conversions, which detracts from the measurement precision. The nonlinearity in delay line-based Vernier TDCs can also be large because it now accumulates in two separate delay lines. Without these factors, the measurement resolution and precision could be very good.

3.3.3 Pulse-shrinking delay line

The measurement time interval can be converted to a pulse of a width equal to the time interval. The pulse width can then be measured with a pulse-shrinking delay line (Rahkonen & Kostamovaara 1990). The delay elements in the pulse-shrinking delay line, two inverters in Fig. 14, shorten the pulse by an amount which corresponds to the LSB. After a certain number of delay elements the pulse vanishes totally, and this number reveals the pulse width. 50 ps resolution was obtained with 0.8 μm CMOS within a range of 100 ns (Karadamoglou *et al.* 2004).

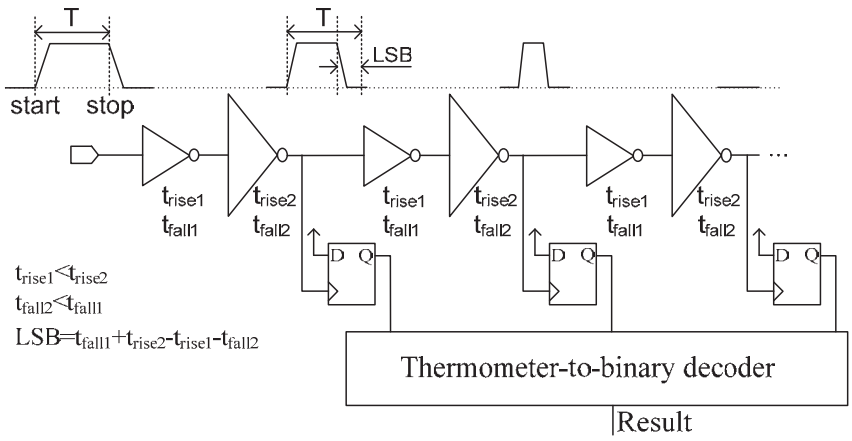

Fig. 14. A TDC based on pulse shrinking in a delay line.

Another similar approach, the cyclic pulse-shrinking technique, uses a single shrinking element in the delay line and circulates the pulse in this delay line until it vanishes (Chen *et al.* 1997). A counter counts the rounds of circulation and indicates the result. Only one element is responsible for the shrinking, which improves the nonlinearity. A dynamic range of 18 ns was measured with 20 ps resolution and 76 ps precision (Tisa *et al.* 2003).

Size, nonlinearity and accumulating jitter are the biggest problems affecting pulse-shrinking delay lines. Their nonlinearity and size can be improved by adopting the cyclic version, although this multiplies the measurement time and the effect of jitter at the same time.

3.4 Technological issues

Size, power consumption, production volume and unit price are the main parameters affecting the selection of a suitable technology. Discrete components offer a good platform for high resolution analogue-based TDCs in low volume production, especially because modern integrated circuit technologies concentrate on digital performance, but the other parameters mentioned above do not fit in well with discrete component implementation. FPGAs offer fast implementation and reconfiguration, but their measurement performance and unit price are usually no more than moderate with high production volumes. ASIC implementation is good where size, power consumption and high production

volumes are concerned. All the supporting blocks can be integrated into the same circuit and the measurement performance also approaches that of realizations designed with discrete components. Analogue signal processing, amplification, current sources etc. can be implemented quite easily in BiCMOS technology, whereas CMOS technology is the natural choice with pure digital TDCs.

Technology scaling in integrated circuits affects their delay generation. When the delay of a buffer in 0.35 µm CMOS technology is about 250 ps, a similar gate in 65 nm CMOS technology, according to the simulations, requires a time of only about 30 ps. When the technology is scaled down, high resolution TDCs are possible with simpler measurement structures and circuit size and power consumption are also reduced.

Not all the negative factors are scaled down with the technology, however. The influence of process variations becomes more clearly visible as the transistors shrink in size, which increases the percentage variation in transistor characteristics. Where the maximum DNL of a differential inverter-type delay element in 0.35 µm CMOS (Paper III) was 15 ps (5% of the propagation delay), the maximum DNL in a similar delay element in 90 nm technology was 12 ps (60% of the propagation delay) (Staszewski *et al.* 2006). If the cycle time of a 100 MHz reference clock (10 ns) is interpolated with a successive delay line, 500 delay elements with a 20 ps propagation delay are needed in a highly developed technology, for example. The INL in this long delay line is higher than in a shorter delay line with longer delays but a smaller relative delay mismatch. The improvement in precision achieved with smaller quantization noise, as in (3), is thus at least partly cancelled out due to the higher nonlinearity.

Noise in the supply and control voltages is also proportionally larger when the operating voltage decreases, which creates more jitter in the delay elements. Although the circuit size becomes smaller with scaled technology, the price of the circuit can be higher, especially in low volume production, due to the higher NRE (non-recurring engineering) costs.

3.5 Conclusions

Most of the TDCs published in the literature are based on the structures presented in this chapter. Several variations on these have been presented, but the original characteristics of the techniques usually remain. The goal is always the same, to obtain an accurate estimate of the measurement time interval with high resolution, low nonlinearity and low jitter. The measurement performance should also remain

within the overall measurement range. The Nutt method relaxes the accuracy requirements within the region of the reference clock cycle time, and for this reason it has been preferred for the present work.

Discrete component realization of the time-to-analogue converter together with an ADC can achieve very high resolution and precision, but interest in this alternative is usually limited by the large size, power consumption and costs. Integration of the analogue parts into a single chip is more or less possible with BiCMOS technologies, but it is difficult to achieve stable operation and low power consumption in combination with high measurement performance. Use was made of standard CMOS technologies and digital measurement architectures in the present work because they offer lot of possibilities at moderate cost, especially when the most modern technologies are avoided.

Delay elements can be combined in several ways for time digitization. Placing the elements one after another causes accumulation of the delay errors of the individual elements and the INL begins to detract from the measurement performance. The resolution is also low, especially in former integrated technologies, but it can be improved by using two parallel delay lines with different delays, as in the Vernier principle. Again long delay lines are needed and the measurement time increases, which begins to increase the jitter as well. The INL can be limited by using the same delay elements several times in cyclic measurement structures, but a feedback logic is usually needed for this, which increases the measurement time and jitter levels further. The measurement or conversion time is also important, because it is this that defines the measurement rate of the TDC.

Previous studies and structures were consulted for guidance on the design of the time interval measurement architecture for the present work, and it is evident that an accurate, high precision TDC can be created by combining the basic structures presented here. The successive delay line is a simple method for covering the measurement region, but long chains must be avoided because of the INL. Cyclic structures help with the INL but cannot be used excessively due to the increase in jitter. A delay difference in parallel delay elements, as in the Vernier principle, provides an effective method for attaining high resolution. Other desired features in a TDC may be a high measurement rate, calibration-free operation, no need for post-processing of the results, full system integration in a small-sized circuit, standard, cheap technology, low power consumption and flexibility of the timing signals and measurement intervals. These characteristics formed a basis for the TDC development work carried out here.

4 Overview of the original publications

The five original publications included in this thesis describe the developmental work carried out with respect to time-to-digital converters. Four TDC circuits were designed, and the papers present the structure, operation, measurement results and the elements behind their performance. This chapter presents an overview and the main messages of all five publications.

4.1 Paper I (2005), A Delay Line Based CMOS Time Digitizer IC with 13 ps Single-shot Precision

Paper I, originally presented at the IEEE International Symposium on Circuits and Systems in Kobe, Japan, in 2005, describes the first TDC circuit designed for this work. Like all the others, it was realized with 0.35 μm CMOS technology, which was quite modern at that time. The Nutt-based measurement core was composed of a counter and stabilized two-level interpolators. Many structures were adopted from previous high precision TDCs designed in the same laboratory, especially those of Mäntyniemi *et al.* (2002). A successive delay line was used for the first level of interpolation within the cycle time of a 145 MHz reference clock. A differential inverter-based delay line structure was presented, which improved the resolution and nonlinearity as compared with a one-sided realization. The second interpolation level was composed of parallel load capacitor scaled delay elements and provided an LSB width of 13.5 ps. The rms precision was 12.4 ps and the maximum measurement range up to 226 μs. The measurement precision was the best published up to that time, and the architecture seemed promising for further development. The main weaknesses were the dependence on a high reference clock frequency and the external calibration, which had to be performed for each circuit separately.

4.2 Paper II (2006), A CMOS Time-to-Digital Converter with better than 10 ps Single-Shot Precision

Paper II, published in the IEEE Journal of Solid-State Circuits, presents the second TDC circuit. The paper goes through the factors affecting measurement precision in Nutt-based converters and presents a new delay line structure for timing signal interpolation. The reference recycling method reduces the number

of delay elements in the successive delay line, which improves the INL. The reference frequency can also be a fraction of the internal delay line frequency.

The TDC measures time intervals up to 204 μs with 12.2 ps resolution. The frequency of the reference source can be chosen freely and a 5 MHz signal generator was used in the measurements. The interpolation factor, τ_{ref}/LSB, was hence 16384 and was achieved using only 20 effective delay elements. The TDC achieved 13.0 ps rms precision alone and 8.1 ps with an INL look-up table (INL-LUT). External calibration was still needed for every circuit in order to compensate for the synchronization delay mismatches. This publication is still the second most cited TDC article of all time in the IEEE *Xplore* digital library.

4.3 Paper III (2009), Synchronization in a Multi-level CMOS Time-to-Digital Converter

Paper III, published in IEEE Transactions on Circuits and Systems I: Regular Papers, presents the third TDC circuit to be designed in the present connection. It is primarily concerned with synchronization problems and the structures required in converters based on multiple measurement blocks. The results obtained at the counter and interpolation levels can be inconsistent, if the operations of these levels are not reliably synchronized. The paper presents a technique for avoiding the synchronization delay mismatch problem. The measurement range at the second interpolation level can be widened in both directions over the effective range, which secures the operation of the second interpolation level in the case of a mismatch.

The TDC contained only 6 differential delay elements at the first interpolation level. The measurement resolution was 9.6 ps and the maximum measurement range 1 ms. The rms precision of the TDC was 10.6 ps, but a precision of 6.0 ps was achieved when the static interpolation nonlinearity was removed with an INL-LUT. A 6 MHz reference source was used in the measurements. The performance in terms of precision was again the best among the known long-range digital TDCs. The main needs for further development concerned usability. The programming and result readout were nonstandard and difficult to use.

4.4 Paper IV (2009), Multiplying Delay Locked Loop (MDLL) in Time-to-Digital Conversion

Paper IV was published in the proceedings of the International Instrumentation and Measurement Technology Conference, Singapore, 2009. It deals with the reference recycling technique, its properties and capabilities as a single interpolation level in modern technologies. The reference recycling delay line, or synonymously, the multiplying delay locked loop (MDLL), can form a compact, efficient time digitizer unit as a stand-alone component with the counter in a small line width technology where the propagation delay of the delay element (LSB) can be few tens of picoseconds. The size of the device can be small and nonlinearity good, because the delay line is short and the counter is responsible for the long range. Jitter and area calculations were performed for the MDLL. The measurement results were based on the TDC presented in Paper III.

4.5 Paper V (2012), A Multi-Channel High Precision CMOS Time-to-Digital Converter for Laser Scanner-Based Perception Systems

Paper V was published in IEEE Transactions on Instrumentation and Measurement. It presents a TDC that was especially suited for the needs of laser time-of-flight (TOF) distance measurement. The characteristics, architecture and measurement results of this latest circuit are also presented in Chapter 6.

The TDC has 7 measurement channels, so that it can detect the start and 6 successive stop signals in one measurement. Several new structures and functions were integrated into the circuit, which improve its usability, reduce the number of external components and are needed for serial production. The internal oscillator makes possible to use a crystal as a reference. The programming and data readout interface is a standard serial peripheral interface (SPI), and the integrated arithmetic logic unit (ALU) calculates the results inside the TDC. A build-in self-test (BIST) can be used for circuit testing at the wafer level. The TDC can also handle situations in which stops arrive before the start, which creates negative measurement results.

The TDC measures time intervals up to ±74 µs with 8.9 ps resolution. The rms precision was 8.6 ps without an INL-LUT and 8.0 ps with an INL-LUT. The measurements were carried out using a 20 MHz reference clock.

5 Structures for a high performance time-to-digital converter

This chapter goes through the principles and structures developed and improved during the work on this thesis in order to make high performance time-to-digital conversion possible. The whole TDC was constructed from the parts presented in Chapter 6.

5.1 Two-level (coarse-fine) measurement architecture

Recent high precision TDCs have usually used a two-level architecture to digitize the interval between the timing signals (Huang *et al.* 2007, Lee & Abidi 2008) or between the timing and reference signals in the Nutt method (Mäntyniemi *et al.* 1997, Chen *et al.* 2007, Mäntyniemi *et al.* 2009, Papers I–V). The two-level measurement principle adopted in the interpolation is presented in Fig. 15. The first interpolation level, also known as the coarse interpolator, locates the timing signal within the reference clock cycle with moderate resolution. This interpolation is often based on a successive delay line in which the resolution is determined by the propagation delay of a digital gate. The second interpolation level, also known as the fine interpolator, locates the timing signal within the result of the first level, i.e. with higher resolution. In other words, sub-gate delay measurement techniques are employed to perform another measurement within the resolution of the first level, which also represents the dynamic range of the second measurement level.

The two-level architecture entails several benefits as far as high resolution measurement is concerned. The number of delay elements and registers is reduced, because the second, high resolution measurement is performed only within a small range, as in Fig. 15. A 100 ns reference clock cycle, for example, can be interpolated with 10 ps resolution by means of 10000 delay elements and registers on one interpolation level, but the same task requires only 100 delay elements and registers for both the coarse and fine interpolations in a two-level setup. The fact that less delay elements participate in the measurement also means that the INL and power consumption can be lower.

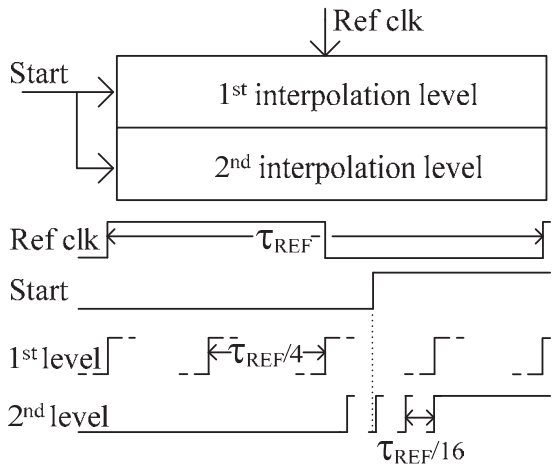

Fig. 15. Interpolation on two levels. Revised from [II] © 2006 IEEE.

5.2 Coarse interpolation

5.2.1 Basic successive delay line structure

The coarse interpolation in the circuits designed here is based on continuous and uniform reference signal propagation in a delay element chain. The external reference signal creates time samples with an even time delay, τ_1 in Fig. 16, in a delay line with identical cascaded delay elements. The timing signals, start and stop, define the prevailing time sample, and the register outputs, $R_{\Phi 0}$–$R_{\Phi 7}$ in Fig. 16, reveal the coarse location of the timing signal within the reference clock cycle. The counter is connected to count the reference clock edges occurring between the timing signals.

Stabilization in the face of process, voltage and temperature (PVT) variations is handled with a delay locked loop (DLL) structure, also shown in Fig. 16. The beginning and end of the delay line are connected to a phase detector, which controls a charge pump that adjusts the delay control voltage V_{ctrl} in the delay line. The control voltage is adjusted until the phase detector receives both signals, the signal which has gone through the delay line and the new reference edge, at the same time, which means that the delay corresponds to the reference clock

cycle time τ_{ref}. The DLL stabilizes the delay in the delay line automatically and continuously when the reference signal is propagated in the delay line.

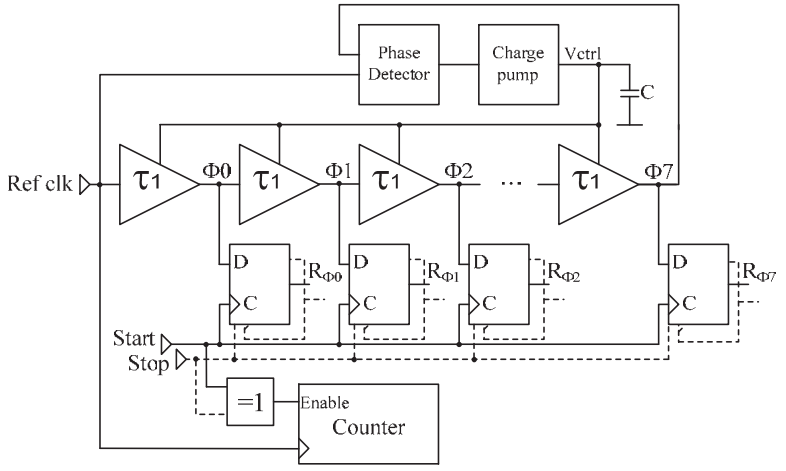

Fig. 16. Basic DLL-stabilized delay line interpolation structure with counter. Revised from [II] © 2006 IEEE.

The delay line structure presented in Fig. 16 has certain drawbacks which had to be considered here. The interpolation signals Φ0… Φ7 have to be identical, e.g. rising edges, so that the time samples will be uniform in every situation. If both rising and falling edges were used, the interpolation LSBs would vary in length with PVT changes. The delay elements in the present structure have to be of the buffer type rather than the inverter type, which would increase the delay in the delay elements and detract from the achievable resolution and precision.

Another drawback is that the total delay in the delay line has to cover the reference clock cycle time. This forces us to use a high frequency reference source and long delay lines, especially as the delay in modern delay element technologies is short. A high frequency external oscillator nevertheless increases the cost and power consumption of the TDC. Operation with a low cost, low frequency external crystal would be the most desirable case.

The third issue is that the length of the delay line, i.e. the number of delay elements in it, affects the linearity of the interpolation time samples (Toifl *et al.* 1999). The DLL stabilization structure matches the beginning and end of the delay line, but time samples taken between these points are not controlled (Paper II). Delay variation (DNL) between the elements accumulates to yield INL, as

discussed earlier, and this time error in the interpolation time samples is also transferred to the measurement result and detracts from the precision. The delay in the delay line should be reduced, but this would further increase the reference clock frequency.

5.2.2 Reference recycling delay line

To relieve the problems presented above, a new delay line structure for timing signal interpolation was designed here (Paper II). This structure is based on a multiplying delay-locked loop (MDLL), which was originally designed to prevent excessive jitter accumulation in frequency synthesis (Waizman 1994). The idea is to recycle the reference signal several times in the delay line before the next jitter-free reference edge is passed to that delay line. A suitable MDLL delay line structure for timing signal interpolation is shown in Fig. 17. The delay elements, as in the transistor-level diagram in Fig. 18, are differential delay-adjustable multiplexers with two input channels. The two input channels are needed only in the first element, but all the elements are identical in order to maintain even-sized time samples. Note that the end of the delay line in Fig. 17 is cross-coupled back to the second channel of the first element. This is necessary in order to achieve pulse propagation.

The delay line operates as follows. The external reference signal rising edge is first converted to a differential and then passed to the delay line. After this the input channel of the first element is changed and the reference begins to circulate in the closed loop. After a certain number of rounds (counted by the recycling counter) the first element lets the next jitter-free reference edge enter the loop. A phase detector and charge pump control the delay so that the delay in the recycled delay line becomes equal to the reference clock cycle time.

When the reference signal is recycled in the coarse interpolator the delay line can be short, which reduces the size of the device and improves the INL. The inverting differential delay element structure, presented in Paper I, makes its propagation delay smaller than that of a buffer-type delay element, which improves the interpolation resolution. As in Fig. 11, opposite signal phases are cross-coupled with inverters, which improves the DNL and the effect of jitter compared with a one-sided element. The propagation delay in an element depends on both the rising and the falling edge, which balance each other out in the case of an extra load or supply noise in the other line, for example.

The reference recycling in a closed loop increases the inherent delay line jitter if the reference frequency is reduced, because the thermal noise and the noise in the supply and bias voltages have more time to create random error in the interpolation time samples. The effects of quantization noise and INL in the delay line nevertheless still dominated in terms of the precision of the designed circuits when a 10 MHz crystal was used as the reference source. Thus the recycling delay line structure also makes use of as low frequency a reference as possible, which will reduce power consumption.

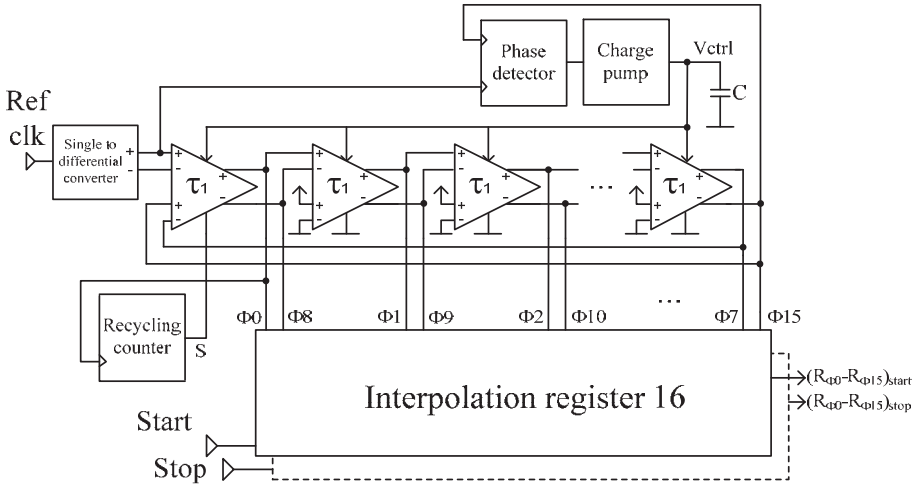

Fig. 17. A reference recycling delay line for timing signal interpolation. Revised from [II] © 2006 IEEE.

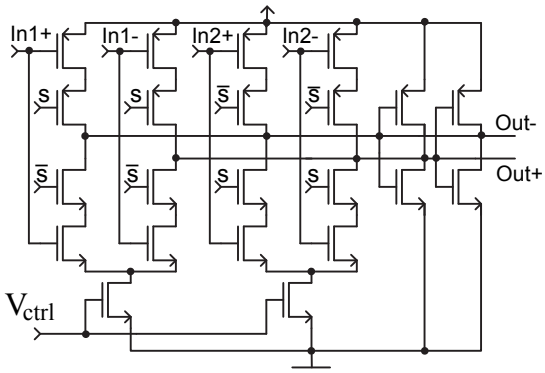

Fig. 18. A differential delay-adjustable delay element with two input channels. Revised from [I] © 2005 IEEE.

5.3 Fine interpolation

5.3.1 Load capacitor-scaled delay lines

The second interpolation level in the TDCs designed here was based on load capacitor scaling in delay elements connected in parallel (Mäntyniemi *et al.* 1997). The propagation delay of a buffer-type delay element, as presented in Fig. 19, can be increased by adding extra capacitance inside the element. When a rising edge propagates through the element the extra charge needs to be discharged, which creates an additional delay. Changes in the propagation delay resulting from the placement of different numbers of unit capacitors of the same size within the elements are shown in Fig. 19. The total propagation delay τ_{tot} consists of basic delay τ_e in a delay element and the delay from a single unit capacitor τ_2 multiplied by the number of unit loads n.

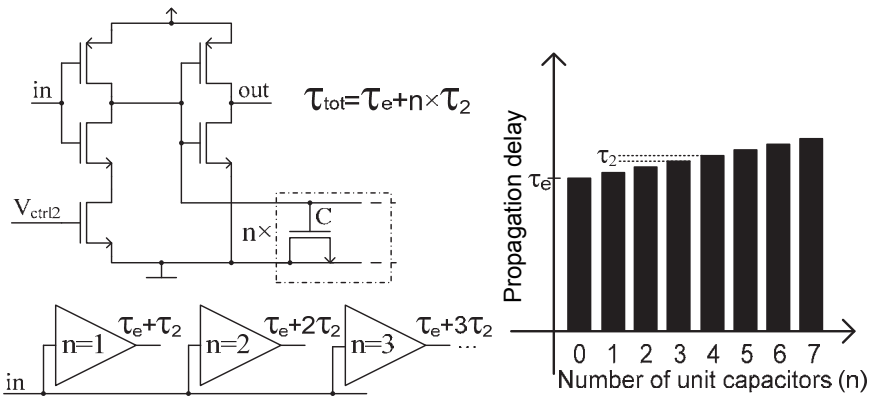

Fig. 19. A load capacitor-scaled delay element. Revised from [I] © 2005 IEEE.

Actual high resolution interpolation can be performed by using two capacitor-scaled delay lines and a register bank, which form a two-dimensional array as shown in Fig. 20, a setup in which the structure digitizes the time interval between the synchronous reference edge (signal sync in Fig. 20) and an asynchronous timing signal (async), as is the case in Nutt-based interpolation. The creation of the synchronous reference signal for the second interpolation level will be discussed in Section 5.4.2 below. The signal async creates 4 time samples, A0–A3 in Fig. 20, with an $8\tau_2$ time difference, while the signal sync creates 8 time samples S0–S7 with a $1\tau_2$ time difference. The delay lines are connected to an arbiter register bank where each arbiter records which out of the two time samples arrived earlier. The register data change as the timing signal moves in the interpolation region, and the interpolation result can be decoded from the register result. Note that the effect of the basic delay in the delay element, τ_e, is cancelled out within the limits of mismatch, because the same delay is used in all the elements of both delay lines.

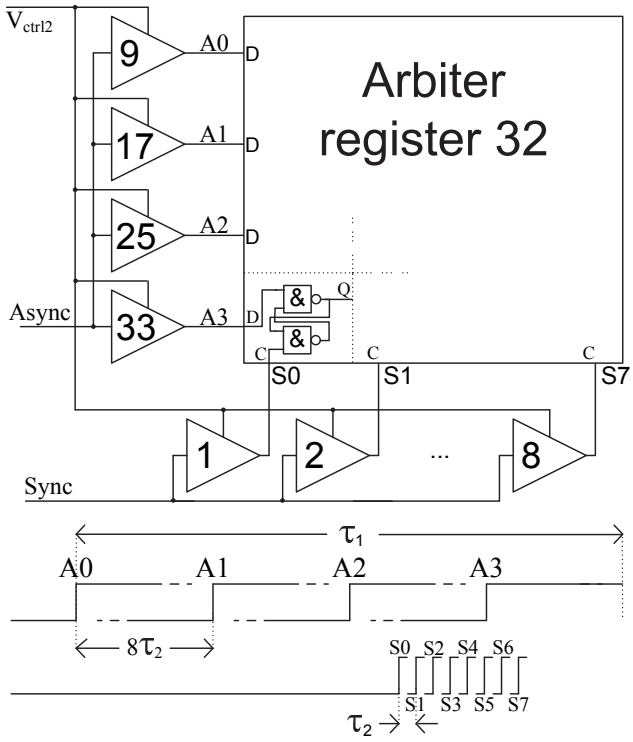

Fig. 20. Fine interpolation with load capacitor-scaled delay elements. Revised from [I] © 2005 IEEE.

Parallel load capacitor scaling is a straightforward and effective interpolation method. High interpolation resolution can be achieved with only a few simple delay elements. When one delay line contains 4 delay elements and the other 8, as in Fig. 20, 4 × 8 = 32 interpolation slots can be created with only 12 delay elements. The parallel structure makes the interpolation fast (flash-type, as used in coarse interpolation) and linear. The DNLs of the individual parallel delay elements do not accumulate to create a high INL as is the case with a successive delay line, because the elements are connected together only on their input side. Each measurement time sample is affected by only one delay element, so that INL = DNL. The capacitors are well-matched components in integrated technologies, so that the extra unit loads do not greatly increase the DNL. All the parallel delay elements change state at the same time, which creates a spike in current consumption (charge and discharge of the unit capacitors), but as the fine

interpolator operates only when the timing signal arrives, the power consumption is almost zero for the rest of the time. The actual interpolation also discharges the unit capacitors, which reduces interference with the supply (the ground is usually a lower impedance path out of the circuit than the supply).

5.3.2 Stabilization of load capacitor-scaled delay elements

In a two-level interpolation architecture the second level interpolates within the result of the first interpolation level. The interpolation range of the fine interpolator is thus $\tau_1 = 32\tau_2$, as presented in Fig. 20. The delay τ_1 was stabilized with a DLL structure on the first interpolation level, but the delay in the fine interpolator delay element must also be stabilized so that τ_2 will be equal to $\tau_1/32$ in all PVT circumstances.

This stabilization can be carried out using the DLL structure presented in Fig. 21. The time difference τ_1 (between time samples Φ2 and Φ3 in Fig. 17, for example) is fed to two parallel fine interpolator delay elements, the unit capacitor difference between which is 32, equalling the delay of the fine interpolator measurement range. The phase detector (PD) and charge pump (CP) adjust the control voltage V_{ctrl2} until the two input signals to the phase detector arrive at the same time. The two delay elements with a unit capacitor difference of 32 compensate for the delay of τ_1 at a certain control voltage V_{ctrl2}, which leads to a situation in which one unit capacitor is equal to a delay of $\tau_1/32 = \tau_2$.

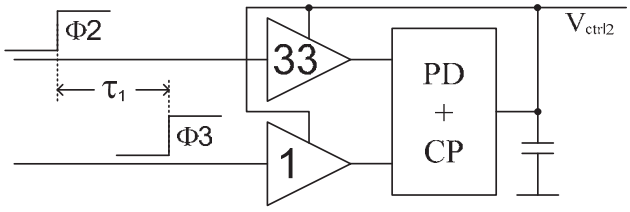

Fig. 21. A DLL structure for capacitor-scaled delay element stabilization. Revised from [I] © 2005 IEEE.

5.4 Synchronization structures

Long range, high resolution TDCs are composed of a counter and one or two interpolation levels. Each measurement unit changes its state as a function of time

and the registers store the final result. A multi-level measurement architecture demands synchronization structures between the measurement blocks so that the measurements made by individual blocks will be compatible and the total measurement result will be correct and unambiguous. The synchronization problem will be discussed here briefly, as a more thorough discussion is available in Paper III.

The timing signals (start and stop) are asynchronous with respect to the operation of the counter and interpolators. In other words they can arrive at any moment during the counter clock cycle or an interpolator time sample. This creates difficulties for the registers, because their reliable, synchronous operation presupposes that the input data are ready and settled before the moment of registering. If the change in register value (data input) comes too close to the moment of registering (clock input), the final result will be uncertain and the propagation delay (decision time) of the register will grow longer (Paper III). This metastable operation of the registers is especially common in delay line-based measurement architectures, which try to locate timing signals by generating time samples with high resolution.

An example of the synchronization problem is depicted in Fig. 22. The asynchronous timing signal stop arrives at the same time as the counter is changing state and the two interpolation levels INT1 and INT2 are naturally also starting new cycles from the beginning of their interpolation regions. All the individual measurement blocks register one or other of the two possible states around the dashed line. The decisions depend on several factors; setup time, threshold voltage, slew rate, wiring, supply voltage, or noise, for example, which are individual to each register. If the decisions made by the counter and interpolator registers in Fig. 22 are on different sides of the dashed line, the total TDC measurement will be wrong. If the counter result is 3, the result in INT1 should be 7 and that in INT2 should be 3. If, for example, CTR = 4, INT1 = 7 and INT2 = 3, the total measurement result will contain an error of one counter clock cycle.

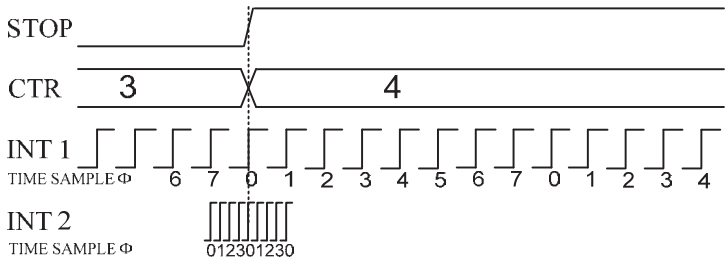

Fig. 22. The synchronization problem with asynchronous timing signals. Revised from [III] © 2009 IEEE.

Synchronization structures between the measurement blocks prevent incompatible operations and measurement results. One solution to the synchronization problem is to allow enough settling time for the registers in one measurement block and steer the other blocks in accordance with these settled register data to achieve compatible operation. For example, the final result of interpolator INT1 in Fig. 22 can be clarified first by giving it enough settling time. The counter and INT2 make their decisions only after this extra delay, also known as synchronization delay, and their measurements are steered to the same side of the dashed line in Fig. 22 as the result of INT1. If, for example, after an adequate synchronization delay the registers in INT1 decide that the timing signal arrived in time sample 0, the counter and second interpolation level will be forced to choose the latter (CTR = 4, INT2 = 0) out of the two possible results.

5.4.1 Counter synchronization

Counter synchronization can be handled with a dual edge synchronization method (Mäntyniemi *et al.* 1997), as presented in Fig. 23, where counting is delayed by one reference clock cycle and the counter control (enabling/disabling) is steered into the correct, safe position by the settled register result from the first interpolation level INT1.

In the counter synchronization structure two parallel flip-flops, A and B in Fig. 23, in the start and stop channels record the arrival of the timing signal together with the falling and rising edges of the reference signal (the rising edge also changes the state of the counter). This dual edge method ensures reliable recording of the timing signal, because one of the two flip-flops always has enough delay between the data change and the clock edge. The selection of which

flip-flop is used for counter control depends on the register results at the first interpolation level. The time sample Φ0 on the first interpolation level, INT1, always begins a new cycle of interpolation and counting by the counter, so its state $R_{\Phi 0}$ (see Fig. 16) can be used to control the counting. If Φ0 was high when the timing signal arrived (to the right of the dashed line in Fig. 23) the result $R_{\Phi 0}$ will also be high, but if Φ0 was low (to the left of the dashed line in Fig. 23), $R_{\Phi 0}$ will also be low. The register result $R_{\Phi 0}$ controls a multiplexer which chooses which of the two flip-flops is used to enable/disable the counter. If $R_{\Phi 0}$ was low (to the left in Fig. 23), the next falling edge of the reference after the timing signal (flip-flop A) will enable/disable the counter, but if $R_{\Phi 0}$ was high (to the right in Fig. 23), the next rising edge of the reference after the timing signal (flip-flop B) will enable/disable the counter. As shown in the timing diagram, the counter is enabled/disabled one clock cycle later in the latter case than in the first case, because the counter is also clocked in conjunction with the rising edge.

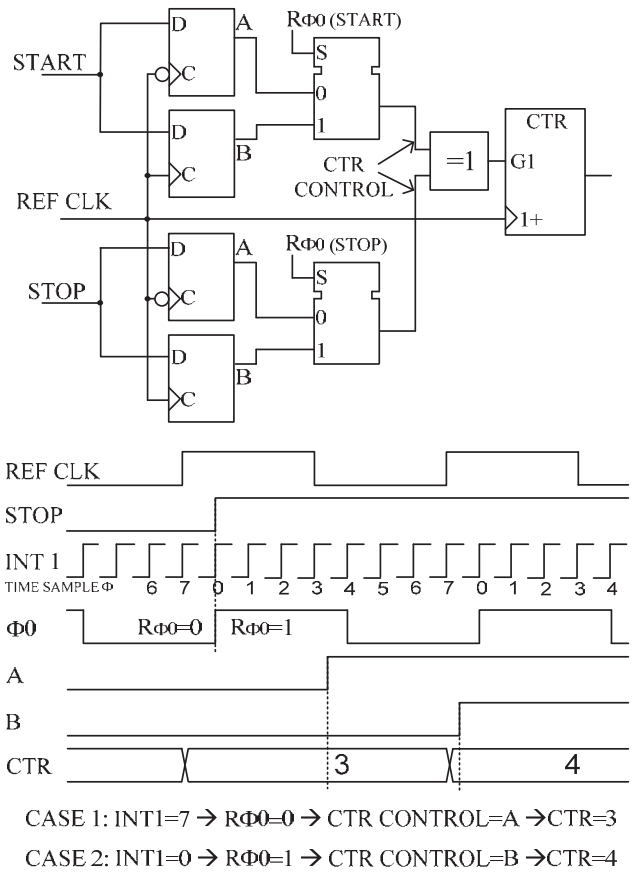

Fig. 23. Counter dual edge synchronizer structure and timing diagram. Revised from [III] © 2009 IEEE.

5.4.2 Synchronization of the second interpolation level

The second interpolation level (fine interpolator) locates the timing signal with higher resolution within the time sample registered on the first interpolation level. In other words, the second level resolves the time interval between the asynchronous timing signal (async) and the synchronous time sample (virtual clock edge) from the first interpolation level (sync). Metastable registration (variation in the decision time of the register) is to be expected on the first level, because the signals are very close to each other (less than or equal to the delay in

one first level delay element). A proper synchronizer between the interpolation levels is needed to deal with two issues. Since the total result of the two levels must be unambiguous, the operation of the second level must be steered by the final, settled result of the first level. The varying decision time of the register on one level due to metastable operation cannot be allowed to influence (shift) the measurement signals on the other level.

A suitable synchronization structure for two-level interpolation in which the first level uses successive delay elements (Mäntyniemi *et al.* 1997) is shown in Fig. 24. The measurement signals on the second interpolation level, sync and async, are delayed by a synchronization delay $\Delta t_S = \Delta t_A = 4\tau_1$, which provides compatible and correct results in the event of metastable register operation at the first interpolation level. The timing diagram and the numbers (0 or 1) next to the flip-flops describe the signal states in one possible situation after the timing signal. The upper flip-flops in Fig. 24 describe the register bank of the first interpolation level, INT1, from where the result can then be decoded to a binary word. It can be seen from the recorded values and the timing diagram that the timing signal arrived after the time sample Φ1. The complementary outputs of these flip-flops are connected to data inputs to flip-flops in the second row in Fig. 24, the second row being clocked with first interpolation level time samples having a phase shift of four time samples. In other words the first interpolation level registers have a settling time of $4\tau_1$ before the data are used for the generation of a synchronous measurement signal for the second level. The OR gate with 8 input lines in Fig. 24 finds the first settled flip-flop after the synchronization delay and generates the sync signal. The total delay due to synchronization, Δt_S, must be compensated for in the asynchronous timing signal path by delaying it respectively by Δt_A.

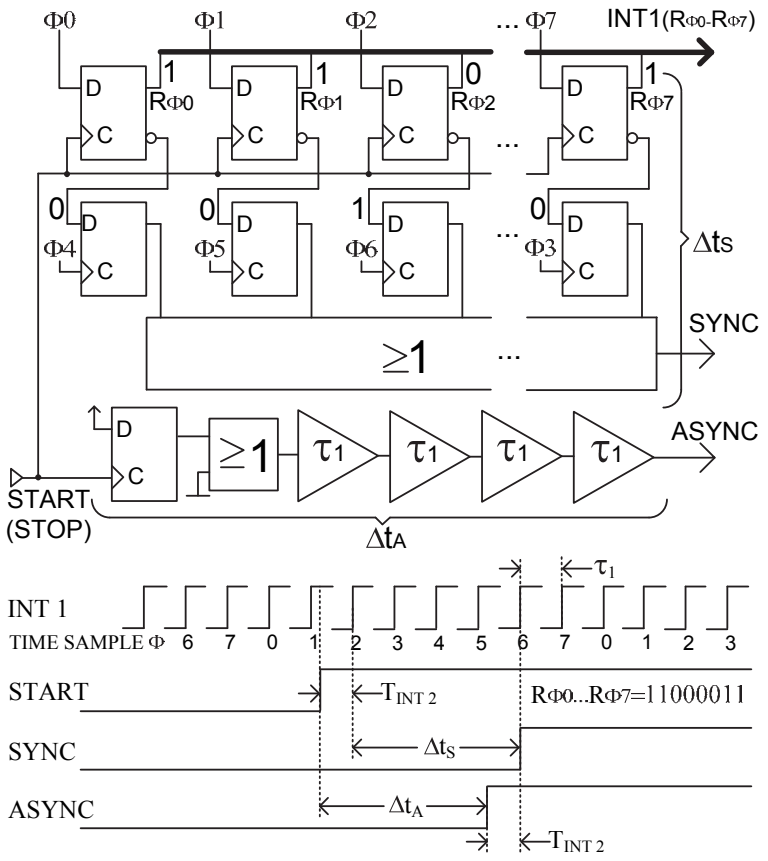

Fig. 24. Synchronization in two-level interpolation. Revised from [III] © 2009 IEEE.

Another problem arises due to differences between the synchronization delays Δt_S and Δt_A. In real circuits the propagation delays of logic gates and registers vary due to process and layout variations, as discussed earlier, and delay mismatch can also be expected between the delays Δt_S and Δt_A in Fig. 24. This delay difference varies between circuits and causes an offset between the measurement signals (sync and async) at the second interpolation level. As shown in more detail in Paper III, the second interpolation level is totally useless if the mismatch is more than $1\tau_1$, because the range of the second interpolation level is the resolution of the first interpolation level ($1\tau_1$). An even smaller mismatch will in any case weaken the performance of the second interpolation level.

The mismatch can be compensated for by introducing extra adjustable delay elements into the measurement signal paths, but these have to be adjusted externally for every interpolator in every circuit. The problem was solved in the present work (Paper III) by widening the measurement region of the fine interpolator. If extra delay elements are used on both sides of the original interpolation region (e.g. one extra element on each side of the parallel delay line, creating time samples with a $8\tau_2$ time difference in Fig. 20), the measurement region of the fine interpolator will be widened to cover the mismatch in the synchronization delays. By this method the mismatch in the synchronization delays can be shifted to the static offset in the final measurement result, which is in any case subtracted in real usage of the TDC.

6 A multi-channel TDC for TOF distance measurements

The development of time-to-digital converters in the present context culminated in the multi-channel TDC presented in this chapter and described in detail in Paper V. This TDC includes all the structures developed from the previously designed TDCs, which is why the other circuits designed in this connection are not presented here in detail. This TDC succeeds for the first time in combining high measurement precision (millimetre-level in laser distance measurement) with multi-channel operation, which can be used to improve the distance measurement performance. Usability and testability are important properties in circuits designed for real applications, and these factors were also considered in the designing of the TDC.

The TDC was realized in the Minifaros Project (part of the 7th Framework Programme funded by the European Commission) (www.minifaros.eu). The project was aimed at developing a low cost, lightweight miniature laser scanner sensor for environmental perception in order to significantly increase the penetration of advanced driver assistance systems, ADAS, in the automotive market (Fürstenberg & Ahlers 2011). The project vision was to create an accident-free traffic environment by means of effective environment perception systems.

6.1 TDC requirements in laser TOF distance measurement

Pulsed laser time-of-flight (TOF) distance measurement is perhaps the most challenging application for a time-to-digital converter. The laser transmitter in Fig. 25 sends a short laser pulse, usually of width 3–5 ns, to the measurement object, which is then reflected back to the receiver block of the radar. The receiver amplifies the weak echo pulse and creates logic-level timing signals from both the transmitted and the received optical pulse. The TDC then resolves the time interval between the timing signals T_m, which corresponds to the distance from the target R, given that the velocity of light, c, is constant.

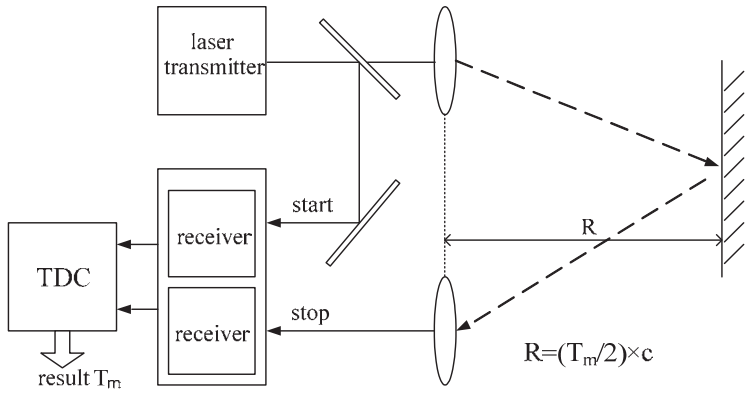

Fig. 25. Concept of pulsed laser time-of-flight measurement. Revised from [V] © 2012 IEEE.

The application is a demanding one for several reasons. Measurement of a long distance to the target requires a high measurement range in the TDC as well. A distance of 100 m from the target corresponds to a time interval of about 670 ns in TOF distance measurement, and the TDC needs to maintain its precision within such a large measurement range. Automatic cruise control is one example of ADAS in which a TOF measurement range of 200 m is needed. At the same time, millimetre-level distance measurement precision calls for a precision better than 10 ps in the TDC.

In difficult circumstances, e.g. in traffic perception, the receiver channel and the TDC can receive several successive echo pulses from one laser shot, as parts of the transmitted pulse may reflect from several objects such as fog, rain or a dirty cover lens, for example, before the actual target is reached. The TDC should be able to handle several successive stop pulses close to each other in order to measure the actual target.

The start signal for time interval measurement in a pulsed laser radar device can be created optically through the receiver channel, as in Fig. 25, or directly from the laser control electronics, which is a much easier way. The propagation delay of an electronic start signal to the TDC input is usually slower than for an optical one, however, which creates a problem when the measured target is very close to the laser radar, as it may mean that stop signals begin to arrive at the TDC before the start signal (negative time intervals). The TDC should be able to handle situations of this kind, too.

The amplitude of the received laser pulse varies with the distance and reflectivity of the target (Kostamovaara *et al.* 1991). The receiver channel amplifies the signal for the TDC, but the varying pulse amplitude may create a timing signal detection error, also known as walk error. The effect of a difference in pulse amplitude in changing the moment of detection and creating error in the measurement result is shown in Fig. 26. The magnitude of this walk error depends on the slew rate of the laser pulse and can be several nanoseconds, which dramatically limits the attainable measurement accuracy. As can be seen in Fig. 26, both the width and slew rate of the received echo pulse change with the amount of walk error. If the TDC is able to measure these as well, the information can be used for walk error compensation.

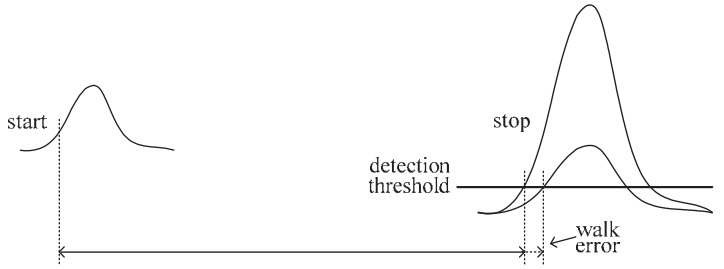

Fig. 26. Walk error in pulsed laser TOF distance measurement. Revised from [V] © 2012 IEEE.

6.2 Operation

The multi-channel TDC designed here has 7 parallel interpolation channels which can detect and register 7 time instants per measurement. It has three input paths (input pins) for the timing signals, one for the start signal and two for stop signals (stop0 and stop1) and can operate in two modes, as presented in Fig. 27. Mode 0 is suitable for pulse width measurements and can resolve time intervals between the start signal and three successive stop pulses in the input path stop0, T_{SP1}–T_{SP3} in Fig. 27. In addition it can measure the widths of the stop pulses, T_{w1}–T_{w3} in Fig. 27. The second operation mode (Mode 1) is indicated for slew rate measurements. It measures the time intervals between the start and stop pulses, T_{SP1}–T_{SP3} in Fig. 27, but it also uses the third timing signal input path stop1. The previous stage before the TDC (the receiver channel, for example) can detect pulse echoes at two threshold levels. The first path, with a lower detection threshold, is connected to stop0 inputs to the TDC and the second, with a higher

detection threshold, to stop1. Now the slew rates of three successive stop pulses can be measured with the TDC, T_{r1}–T_{r3} in Fig. 27.

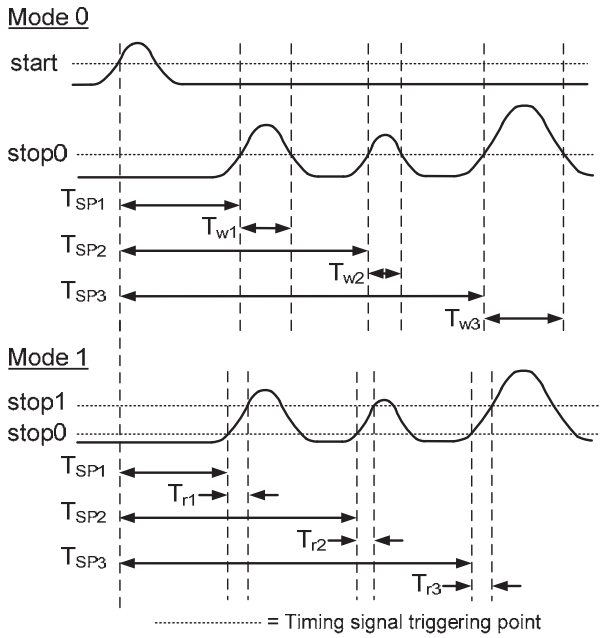

Fig. 27. Pulse width and slew rate measurement modes (V, published by permission of IEEE).

6.3 Architecture

The TDC circuit, composed of the blocks depicted in Fig. 28, includes an on-chip oscillator which uses a crystal as a time reference and is provided with a second input for an external oscillator (a temperature-compensated crystal oscillator, TCXO, for example) for use if the jitter or temperature drift of the crystal is too large for the application. The reference signal continues from the internal oscillator to the measurement core, including the DLLs and time digitizers. The measurement core will be presented in detail later. The ALU (arithmetic logic unit) decodes the raw measurement data and calculates the time intervals, pulse widths or slew rates in the corresponding measurement modes. The output is in a binary two's complement presentation format, which can handle cases in which

stop signals arrive before the start signal. The data interface to and from the TDC is a standard 100 MHz SPI (serial peripheral interface). In addition, two extra interface signals Ready (measurement ready) and Init (initialize the registers) can be used to improve the measurement rate. The circuit can be tested without external timing signals by means of a BIST (built-in self-test) in which timing signals are created by the corresponding control words at the SPI interface. Defined measurement results are expected because the time interval between the control words is stable (a known multiple of the SPI cycle time). The Input Control block transmits the correct timing signals for digitization, the rising and falling edges of the stop0 input in Mode 0 and the rising edges of the stop0 and stop1 inputs in Mode 1.

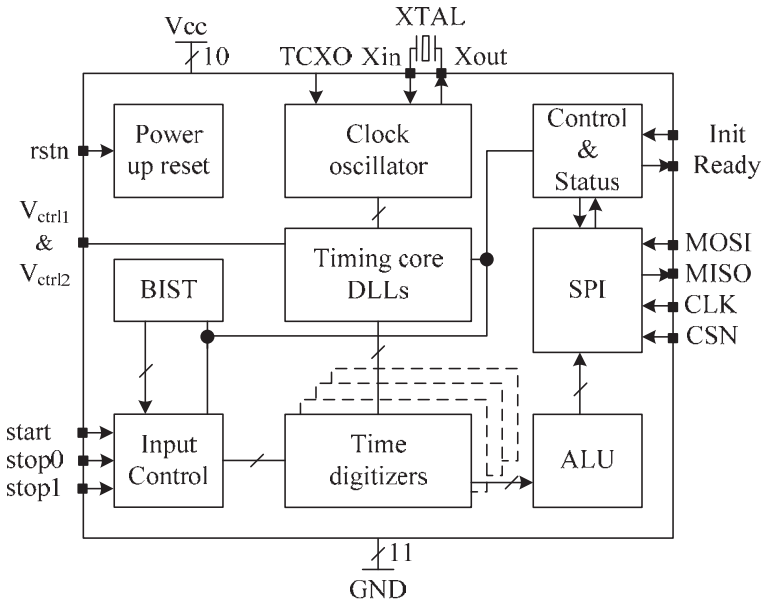

Fig. 28. Block diagram of the TDC. Revised from [V] © 2012 IEEE.

6.4 Measurement core

The measurement core, shown in Fig. 29, is based on the techniques and structures presented in chapter 5. The reference signal REFCLK is first converted to a differential and then passed to the reference recycling delay line. This delay line is composed of 8 differential delay elements which create a total of 16 time

samples Φ0… Φ15 as the reference signal first propagates through the delay line and then does so again in the opposite phase due to cross-coupling in the first element. The 0.35 µm CMOS technology provides a ~280 ps propagation delay τ_1 for the adjustable delay elements over a large temperature range. With a 20 MHz reference crystal and a recycling factor M = 11, the internal delay line frequency $1/\tau_{clk}$ becomes 220 MHz.

The second delay-locked loop above the recycling delay line adjusts the control voltage V_{ctrl2} and stabilizes the second interpolation level delays against PVT variations. The 14-bit counter with counter synchronization at the top of Fig. 29 counts the rounds of the recycling delay line between the timing signals and provides a ±74 µs measurement range between the timing signals. The first timing signal (start or stop) enables the counter and all the arriving timing signals register the current state of the counter.

The interpolator block at the bottom of Fig. 29 is replicated 7 times, because it is necessary to interpolate 7 successive timing signals for each measurement. The register and synchronization block, also presented in Fig. 24, composes the first interpolation level result INT1 and also provides the synchronous reference signal, sync, for higher resolution interpolation at the second level. Each asynchronous timing signal is delayed by the synchronization delay Δt_A, after which the signal async creates 6 parallel time samples with a time difference of $8\tau_2$ by means of the parallel capacitor-scaled delay line, also presented in Fig. 20. Actually four such delay lines are needed to cover the interpolation region of $32\tau_2$, but one extra element is inserted on each side of the targeted interpolation region to allow for a mismatch between the synchronization delays Δt_A and Δt_S, as explained in Section 5.4.2. The sync signal creates eight parallel time samples with a resolution of τ_2 = 8.8 ps. The synchronous and asynchronous high resolution time samples confront each other in the register bank presented in Fig. 20, and the second interpolation level result, INT2, can be determined from their degree of coincidence. One timing signal registers the counter state, CTR, first interpolation level result, INT1, and the second interpolation level result, INT2. The time intervals between the start and stop signals, stop pulse widths or slew rates can be counted by subtracting the corresponding timing signal results. The subtraction for the time interval between the start and stop pulses, for example, is of the form:

$$T_m = \left(CTR_{stop} - CTR_{start}\right) \times \tau_{clk} + \left(INT1_{stop} - INT1_{start}\right) \times \tau_1 + \left(INT2_{stop} - INT2_{start}\right) \times \tau_2. \quad (4)$$

The subtraction (stop – start) applied to the counter result makes it possible to express a negative overall result when the stop pulse arrives before the start pulse.

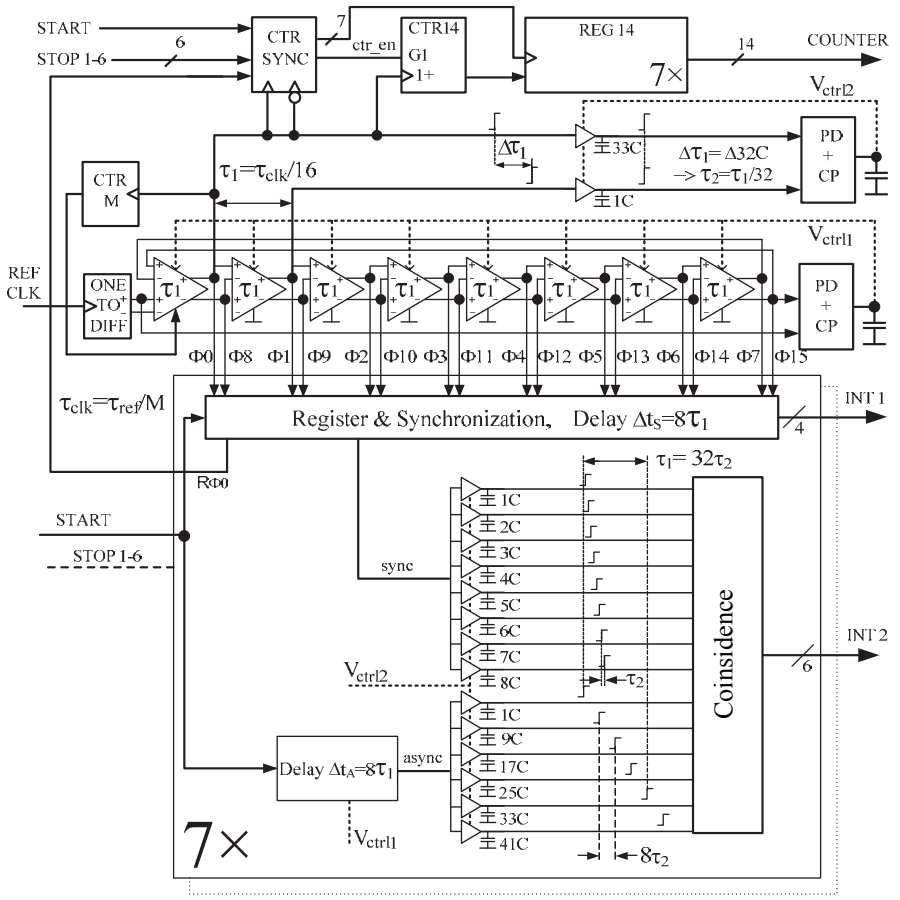

Fig. 29. TDC measurement core. Revised from [V] © 2012 IEEE.

6.5 Measurement results

The circuit dimensions of the multi-channel TDC are 2.4 mm x 3.7 mm, and the power consumption at an operating voltage of 3.3 V and an internal frequency of 220 MHz is 85 mW. The following measurement results were collected from 5 circuits using a 20 MHz crystal as a reference. A photograph of the circuit is presented in Fig. 30.

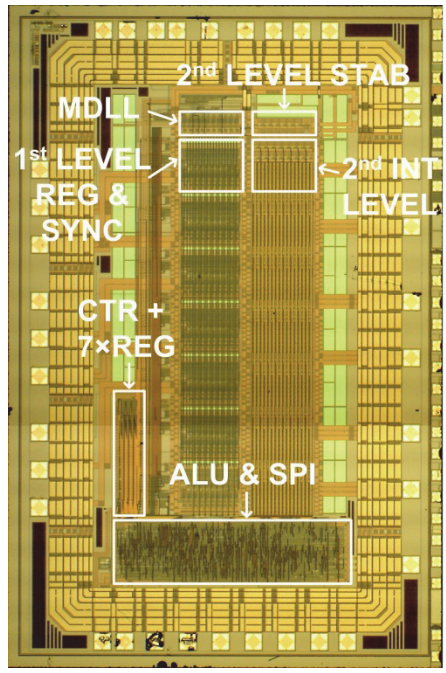

Fig. 30. Photograph of the TDC circuit. Revised from [V] © 2012 IEEE.

6.5.1 Interpolation nonlinearity

As discussed in Chapter 3, the effect of interpolation nonlinearity on the averaged linearity of the measurement result is small when the Nutt method is used, because the asynchronous timing signals hit the nonlinear interpolation region in a random manner. Nonlinearity is important, however, because it affects the measurement precision (3).

DNL, the time deviation of the interpolation LSBs from the intended value of 8.878 ps, was estimated by making 10 000 000 asynchronous measurements and collecting the distribution of the timing signal hits among the interpolation slots. In the ideal case every slot should receive an equal number of hits, but when the slot has a positive DNL, for example, its number of hits will be higher.

The differential and integral nonlinearities (DNL and INL) presented for one interpolator in one circuit in Fig. 31 cover the whole ~4.5 ns interpolation region with 512 interpolation slots. The same nonlinearity of the 32 interpolation slots

from the second interpolation level repeats itself 16 times in both the DNL and INL diagrams, because the same second level operates within all the 16 time samples from the first interpolation level. As can be seen from the INL diagram, the second interpolation level causes an INL of less than 12 ps and the maximum difference in INL, ~30 ps, is caused by the first interpolation level. The delay elements, wirings and interpolation registers in the first level are not fully identical, and the accumulation of error in the successive delay line also increases the INL. The standard deviations of the INLs in the different interpolators and circuits, $\sigma_{inl\text{-}st}$ and $\sigma_{inl\text{-}sp}$ in (3), were found to vary in the range 4.0 ps–6.3 ps.

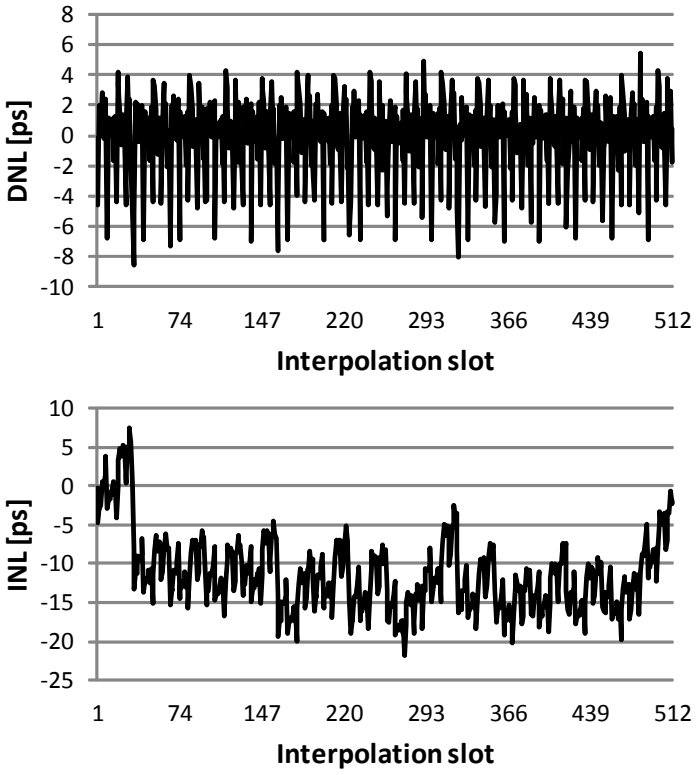

Fig. 31. Interpolator differential and integral nonlinearity (V, published by permission of IEEE).

6.5.2 Temperature drift

Several techniques may be used to compensate for the drift in measurement results caused by temperature. The delay cells in the TDC are delay-locked to the reference clock cycle time, which minimizes the temperature drift in the interpolators, while the temperature drift in the nonstabilized gates and structures mostly cancels out, because all the measurement channels are identical. A threshold voltage change in register at a low temperature, for example, will cancel out in the overall measurement result, because all the registers experience almost the same effect and the total measurement result is always a subtraction between two interpolations (4). The small delay variations due to layout and process parameter differences in nonstabilized structures, e.g. the timing signal paths from input pads to measurement blocks, can nevertheless drift with temperature.

The temperature drift in Fig. 32 was determined by measuring a constant time interval while the circuit was in a heating chamber. The reference signal was created with an external signal generator at room temperature in order to remove the effect of crystal temperature drift. The measurement results drifted by less than 0.5 ps/°C, when the temperature was altered from -35 °C to +65 °C.

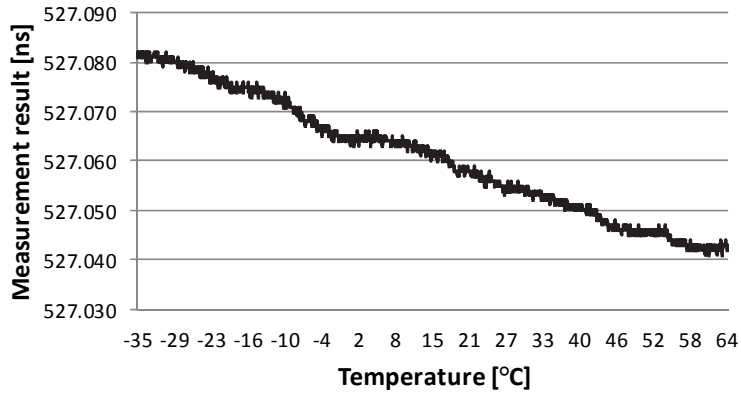

Fig. 32. Temperature drift.

6.5.3 Measurement linearity

The linearity of the TDC, i.e. the deviation in the straight line on the output-versus-input graph when measuring different time intervals, was determined by creating the time intervals with a delay generator and measuring them with this TDC and another in which the linearity error had been calculated separately. Each time interval was measured 10 000 times and subtraction of the averaged results obtained from both TDCs was used to reveal the measurement linearity. The TDC nonlinearity when the time interval was swept from -100 ns to 100 ns is shown in Fig. 33. Cross-talk effects begin when the edges of ~5 ns start and stop pulses are in close proximity to each other. The maximum nonlinearity spikes, about ±22 ps, occur when the edges, rising or falling, arrive at the same time, whereas nonlinearity is below ±2 ps when the timing signals and interpolators do not interfere with each other. The offset error of about 8 ps between the positive and negative measurement values seem to depend on the slightly different slew rates for the timing signals in the measurement setup but the reason is mostly unclear.

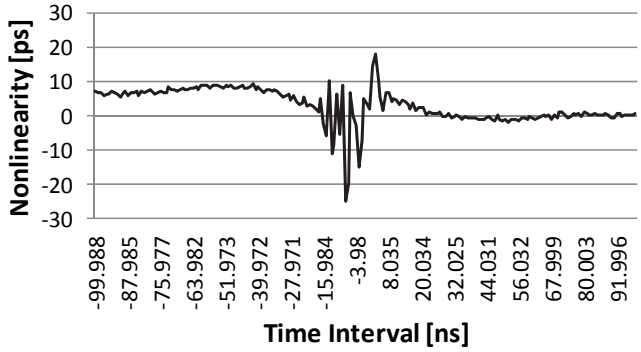

Fig. 33. Measurement nonlinearity with different time intervals.

6.5.4 Precision

Several time intervals of around 400 ns were generated with coaxial cables and each was measured 30 000 times in order to resolve the precision. Precisions obtained with 5 TDCs over the whole interpolation range (~4.5 ns) are presented in Fig. 34. The precision achieved for different time intervals varied from 6.1 ps

to 9.8 ps, mainly due to interpolation nonlinearity. Post-processing of the results with an INL look-up table removed the effect of INL from the measurement results, and the precision improved further by 0.5–1.0 ps with different measurement time intervals and in different circuits. The rms value σ_{rms} for the precision without post-processing of the results varied in the range 8.0 ps–8.6 ps between the circuits measured. When only the rms quantization error σ_q = 3.6 ps and average measured standard deviations of interpolator nonlinearities $\sigma_{inl\text{-}st}$ = $\sigma_{inl\text{-}sp}$ = 5.2 ps are used in (3), the equation gives 8.2 ps as the calculated rms precision. The rms effect of all the jitter sources can be approximated as being very small, maybe less than 3 ps.

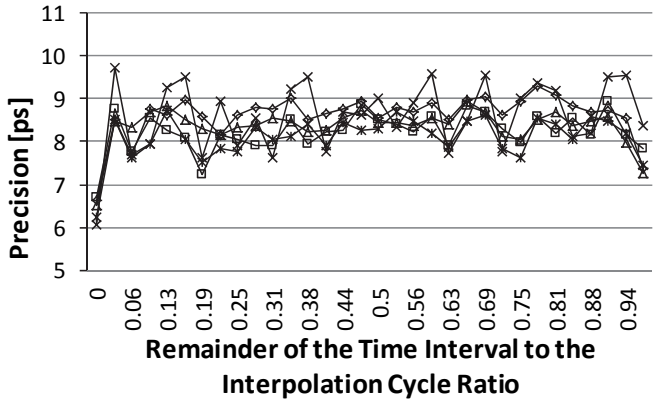

Fig. 34. Single-shot precision at an internal frequency of 220MHz. Precision is shown as a function of the remainder Q, where ΔT = N*(1/220MHz) + Q (V, published by permission of IEEE).

6.5.5 Multi-channel measurement

One start and three successive stop-pulses with different pulse widths and time intervals over several microseconds were generated with the Tektronix AWG 2021 signal generator. The stop-pulse cable was divided between the two stop input channels of the TDC in such a way that the stop1 input path contained a longer coaxial cable than the stop0 input path, as shown in Fig. 35. The TDC was first operated in Mode 0, to measure the time intervals from the start pulse to the rising edges of the three stop pulses and also the stop pulse widths, and then Mode 1 was used to determine the delay between the pulses in the stop0 and

stop1 input channels due to the difference in cable length. The measurements were repeated 100 000 times in both measurement modes, yielding the distributions of results with average values (μ) and standard deviations (σ) presented in Fig. 36.

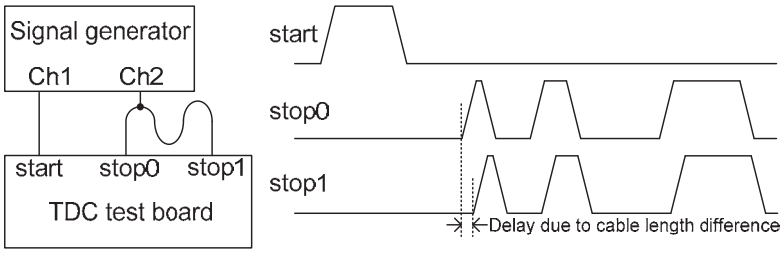

Fig. 35. Multi-channel measurement setup.

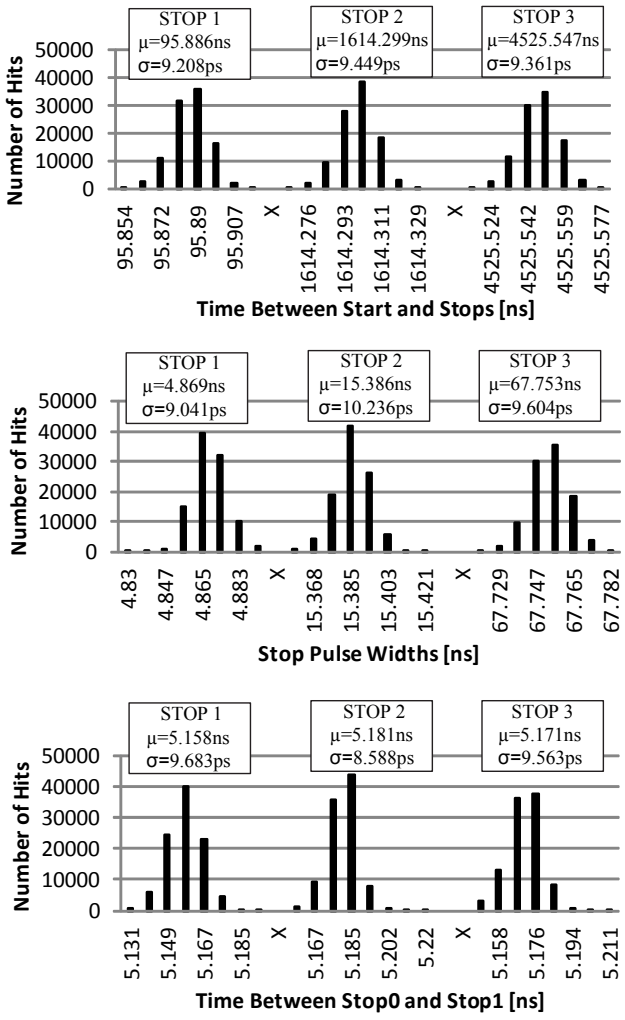

Fig. 36. Measurements with 3 successive stop-pulses (V, published by permission of IEEE).

The diagram at the top of Fig. 36 shows the measured time intervals between the start and three successive pulses in the stop0 input channel, the results being similar in both measurement modes. The data for the next diagram were collected in Mode 0 and show the stop pulse widths. The last diagram describes operation in Mode 1 and shows the propagation time difference between the two stop input

channels with coaxial cables of different lengths. Note that the small offsets in the averaged values in the last diagram result from differences in the timing signal detection moments of the interpolators, whereas the offsets remained constant when the delay between the stop0 and stop1 input channels was altered. Jitter from the signal generator is also present in the results.

7 Discussion

The aim of this work was to improve the measurement performance of integrated TDCs, the main performance parameters of which are accuracy and precision. Demanding applications need the reliable, high precision information on the time interval even over a long measurement range. Pulsed laser TOF distance measurement, for example, can achieve millimetre-level measurement performance only if the time interval measurement unit is capable of picosecond precision over a long µs-level linear dynamic range. On the other hand, there are several other characteristics that are also important for the real use of TDCs, depending on the specific applications. These include automatic stabilization against temperature and supply voltage variations, elimination of the need for post-processing (look-up tables), full integration in a standard moderate line width CMOS technology (economy), high-speed operation, low power consumption (mobility) and flexibility in terms of timing signals and measurement intervals (different measurement modes).

It is pointed out here that achieving low measurement uncertainty demands a balance between the contributing factors shown in equation (3), quantization error, integral nonlinearity and jitter. Minimizing one of these does not help to improve the precision, because then the others become dominant. It is the dominant factor that should be minimized in every case, even if it increases the others. For example, the level of jitter can be allowed to increase if this helps to minimize the INL, which was probably the main reason for the performance improvement in the present case.

A small quantization error in time interval digitization can be achieved only by using high measurement resolution. Highly developed digital circuit technologies offer this easily, because the propagation delays of digital gates in most modern technologies can be just a few tens of picoseconds (Staszewski *et al.* 2006, Henzler *et al.* 2008, Lee & Abidi 2008). Use of the latest technologies for low-volume production is expensive, however, as here, too, sub-gate delay interpolation techniques are needed in order to attain picosecond-level measurement performance. The higher relative delay mismatch in shrunken delay elements can also become a problem.

High resolution can be achieved with less aggressive technologies by means of sub-gate delay measurement techniques. The Vernier principle applied to integrated circuits employs two delay lines, which makes the INL even higher than with a successive delay line. The delay lines can be shorter and the INL

smaller in the cyclic Vernier method, but the jitter level is still a problem, as the signals propagate in the delay lines for a long time in order to reach high resolution (Chen *et al.* 2007). Jitter also accumulates to a high level in the cyclic pulse shrinking method, because the long time intervals at high resolution require thousands of circulations (Chen *et al.* 2000).

The INL in digital measurement architectures can be minimized by preventing the excessive accumulation of DNL from the individual elements. The reference frequency can be increased in the Nutt method in order to reduce the interpolation time cycle and render the interpolator more linear. TDC architectures usually use reference frequencies ranging from several tens of MHz up to the GHz level, but the power consumption of the high frequency oscillator can then be high and the costs of the oscillator can be much greater than those of the actual TDC. The best situation could be when only a low frequency crystal is needed as a reference source.

The INL affecting the measurement resolution can be also measured and the data gathered into a look-up table (LUT), which can be used after every measurement to remove the effect of nonlinearity. The result post-processing will reduce the measurement rate, however, and demand extra electronics, as every chip has to be measured individually and the look-up table is only applicable when the measurement circumstances (temperature, supply voltage etc.) are the same as when the table was compiled. It is not reasonable to present a very small, integrated, high performance TDC if this actually needs an external microcontroller, a memory chip and a lot of look-up tables in order to work well.

External reference sources, oscillators or simple crystals, can have rms jitter levels below 1 ps, and the effect of clock jitter on measurement precision is not usually relevant. Random jitter in measurement signals due to thermal noise, for example, can accumulate to become a dominant factor, so that the measurement or interpolation time, i.e. the conversion time, should be minimized in order to prevent excessive jitter.

The possibility for using the TDC at varying temperatures and when the supply voltage is liable to change slightly, as in a mobile application, for example, should be a natural advantage, but the topic is often ignored in publications. With adjustable delay elements the measurement resolution can be locked to a certain portion of the reference clock cycle time, which will remain the same under different conditions. Stabilization can be made automatic, as explained in Chapter 5. When the resolution varies with temperature and supply voltage, the prevailing resolution has to be measured constantly in order to prevent accuracy error in the

measurement results. Digital calibration methods have been presented in which the TDC is used from time to time to measure the cycle time of a known reference clock, from which the actual measurement resolution can be deduced (Nissinen *et al.* 2003, Staszewski *et al.* 2006, Lee & Abidi 2008). This fully digital stabilization method can be difficult to use with TDCs having a long measurement range, however. The prevailing resolution must be resolved with extremely good accuracy for the error in the total result to be acceptable at long time intervals. If, for example, a time interval of 1 μs is to be measured with a digitally calibrated TDC having an approximate resolution of 10 ps (LSB), a 0.1 fs offset in the deduced prevailing resolution will produce an error of one LSB in the total result. The cycle time of the reference needs to be averaged many times in order to ascertain the prevailing resolution with this accuracy, and a temperature change of 0.003 °C, for example, would alter the resolution this much (Rahkonen & Kostamovaara 1993).

The work completed here has proved that the measurement technology does not have to be the most modern and the reference frequency does not need to be high in order to achieve high measurement performance and stable operation in varying environmental circumstances. The reference recycling technique developed here combines a short delay line with a wide interpolation region and fully automatic timing stabilization. The short delay line provides for a low INL and the interpolation range can be extended by using it several times. This increases the jitter, but the jitter level remains moderate even at reference frequencies of less than 10 MHz.

The second interpolation level continues the interpolation with a parallel load capacitor-scaled delay line structure. Capacitors are well matched components in CMOS technologies and adding them as extra loads to the parallel delay line, in which element mismatches do not accumulate, keeps the INL low. Capacitor scaling is perhaps the only method for achieving a resolution better than 10 ps with better than 10 ps linearity in 0.35 μm CMOS technology.

7.1 Comparison with other TDCs

The main parameters of previously published high precision TDCs, their architecture, design technology, reference clock frequency, measurement resolution (LSB), precision (usually rms value, if reported), maximum measurement range, measurement/conversion channels and power consumption, have been collected together and are presented in three tables below. The number

of measurement/conversion channels describes how many time-to-digital conversions the architecture performs or is able to perform per measurement. Nutt-based TDCs digitize the time intervals of timing signals (at least the start signal and one stop signal) with respect to the reference clock edge, and at least two conversions are always included. Some TDCs need to digitize only the time interval of one asynchronous timing signal relative to the reference edge or measure the time between timing signals directly without using a reference signal (single conversion structures), and then the number of channels is one.

Table 1 applies to converters in which the high resolution measurement unit is realized with discrete components: resistors, capacitors, operational amplifiers and analogue-to-digital converters (ADC), for example. The best published measurement resolution, and also the best precision, can be found among these (Keränen *et al.* 2010). The Nutt-based converter interpolates within the cycle time of a 200 MHz reference source by means of time-to-amplitude conversion (TAC), a high resolution (16-bit) analogue-to-digital converter (ADC) and FPGA counts of the full reference cycles elapsing between the timing signals. The analogue measurement method with discrete components can provide high performance when size, price and power consumption are not the main priorities.

Table 1. TDCs with discrete components.

Reference	Architecture	Technology [µm]	Reference frequency [MHz]	LSB [ps]	Precision RMS [ps]	Range [µs]	Channels	Power [mW]
Kalisz *et al.* 1994	Counter and TAC	Discrete components	100	3	20	2.15E+07	2	NA
Määttä & Kostamovaara 1998	Counter and TAC	Discrete components	100	10	10	2.55	2	2000
Keränen *et al.* 2010	Counter and TAC	Discrete components	200	0.1	1.8 (1.0)[a]	Program-mable	2	5800

[a] with look-up tables or result post-processing

Table 2 presents recent integrated TDCs that are suitable for applications in which a long measurement range is not needed. In frequency synthesis, for example, a TDC can be used to digitize the cycle time of a GHz-level output signal or its phase difference with respect to a reference signal.

The successive delay line measurement method provides inverter delays of about 20 ps in 90 nm CMOS technology (Staszewski *et al.* 2006). This gate delay

was divided by four thanks to the interesting idea of using four passive resistors between the delay elements (Henzler *et al.* 2008). Another sub-gate delay measurement method (Lee & Abidi 2008) amplifies the residue between the timing signal and delay line time sample and achieves almost 1 ps measurement precision by means of complicated linearization methods and look-up tables.

The architecture is simpler (a single conversion structure), when the measurement range needs to be linear for a few nanoseconds or even less, as the synchronized counter and the second high resolution measurement unit are not needed. This together with small line width technology can also reduce the power consumption, and can similarly improve the measurement precision, because there is only one conversion to create quantization error in the digitized result. The delay elements in the first 5 TDCs in Table 2 do not have an adjustable delay. The simpler element structure makes for better resolution, but it also means that the resolution varies with temperature or operating voltage and from one circuit to another. Digital stabilization methods employing a GHz-level reference clock need to be used alongside the actual measurements in order to assess the prevailing resolution.

Table 2. Integrated TDCs with a low measurement range.

Reference	Architecture	Technology [µm]	Reference frequency [MHz]	LSB [ps]	Precision RMS [ps]	Range [µs]	Channels	Power [mW]
Tisa *et al.* 2003	Cyclic pulse shrinking	0.8 CMOS	NA	20	76	0.018	1	NA
Staszewski *et al.* 2006	Delay line	0.09 CMOS	1800	17-21	NA	0.0006	1	6.9
Henzler *et al.* 2008	Delay line with resistors	0.09 CMOS	NA	4.7	3.3	0.0006	1	3.6
Lee & Abidi 2008	Time amplification	0.09 CMOS	NA	1.25	<1.25[a]	0.0006	1	3
Straayer & Perrot 2008	Gated ring oscillator	0.13 CMOS	NA	6	NA	0.012	1	2.2-21
Yu *et al.* 2010	Counter and Vernier ring	0.13 CMOS	NA	8	NA	0.03	1	7.5

[a] with look-up tables or result post-processing

Table 3 presents the integrated long range TDCs suitable for laser radar applications, for example. Various interpolation methods, usually based on the delay line principle, have been realized and all the architectures utilize the Nutt method. The measurement precision fluctuates, but is usually near or above the measurement resolution, which shows that the interpolation nonlinearity or jitter predominates when the precision is evaluated. In these cases the measurement resolution could even have been reduced without any significant effect on the precision.

Perhaps the most interesting TDC in Table 3 is the cyclic time domain successive approximation method (CTDSA) (Mäntyniemi *et al.* 2009), in which the measurement signals are recycled in the delay lines several times and come closer to each other by a different known amount in each cycle. The amount can be defined by a delay element in which the number of load capacitors can be changed. The INL remains low, because the same delay lines are used every time, and jitter levels also remain low because only a few rounds are needed, i.e. the conversion time is moderate.

The TDCs designed here have very good performance in almost every aspect by comparison with other published TDCs. The 0.35 µm standard CMOS technology used here reduces fabrication costs, especially by comparison with the most modern technologies listed in Table 2. The reference frequency required is

low, which makes it possible to use a low frequency crystal as a reference, while the automatic DLL-based stabilization system keeps the resolution constant under varying PVT conditions. The two-level interpolation architecture improves the resolution to below 10 ps without an inconvenient number of delay elements and registers. The precision of the latest TDC is better than 10 ps without result post-processing, due to the short, linear delay line architecture and good matching between the load capacitors on the second interpolation level. The measurement range can easily be extended in the Nutt method without detracting from the performance. Precision deteriorates at higher time intervals only on account of the jitter in the reference clock. Multiple measurement channels can be combined in the architecture, as was done in the latest TDC (Paper V). Power consumption remains moderate, as only the first interpolation level operates between the actual interpolations.

Table 3. TDCs with a long measurement range.

Reference	Architecture	Technology [µm]	Reference frequency [MHz]	LSB [ps]	Precision RMS [ps]	Range [µs]	Channels	Power [mW]
Gorbics *et al.* 1997	Counter and vernier	0.8 CMOS	166.66	46.9	40	10	2	NA
Mota *et al.* 2000	Counter and RC-delay lines	0.25 CMOS	320	24.4	22.4	12.8	8	NA
Räisänen-Ru. *et al.* 2000	Counter and TAC	0.8 Bi-CMOS	100	32	<25	2.5	2	350
Szplet *et al.* 2000	Counter and vernier	FPGA	100	110	70a	4.3E+07	2	140
Mäntyniemi *et al.* 2000	Counter and delay lines	0.6 CMOS	66	29.6	28 (16)a	496	10	50
Nissinen *et al.* 2003	Counter and ring oscillator	0.35 CMOS	10	156	79	0.985	2	72
Chen *et al.* 2006	Counter and TAC	0.35 CMOS	80	50	NA	0.25	2	0.75
Chen *et al.* 2007	Counter and vernier	0.35 CMOS	55.56	37.5	40	>0.05	2	150
Copani *et al.* 2008	Counter and TAC	0.18 Bi-CMOS	350	NA	12	188	4	518
Nissinen *et al.* 2009	Counter and ring oscillator	0.13 CMOS	6.7	15.9	20	0.1	3	15.9
Mäntyniemi *et al.* 2009	Counter and CTDSA	0.35 CMOS	100	1.2	11 3.2a	327	2	36
Jansson *et al.* 2005	Counter and delay lines	0.35 CMOS	145	13.5	13	226	2	55
Jansson *et al.* 2006	Counter and delay lines	0.35 CMOS	5	12.2	13 8.1a	202	2	40
Jansson *et al.* 2009	Counter and delay lines	0.35 CMOS	6	9.6	12 6a	1000	2	35
Jansson *et al.* 2011	Counter and delay lines	0.35 CMOS	20	8.88	8.6 8.0a	74	7	85

[a] with look-up tables or result post-processing

8 Summary

The aim of this work was to improve the performance of integrated digital time-to-digital converters. One goal was to be able to measure long µs-level time intervals with better than 10 ps measurement precision, as required in laser TOF distance measurement, for example. Delay line interpolation methods with a counter seemed to be the key to achieving such a performance. It is usually INL that limits the precision attainable in delay line-based architectures.

A new delay line structure for timing signal interpolation was developed in which the number of delay elements in the successive delay line interpolation method was minimized by using the same delay line several times per reference clock cycle. INL does not accumulate to any high degree in the reference recycling architecture developed here, but repeats itself during each recycling period. The same structure also makes it possible to use a low MHz-level reference frequency, so that only a crystal is needed as a external oscillator component. A delay element structure based on a differential inverting multiplexer was developed which makes the propagation delay shorter than in the buffer-type elements used previously. The differential nature of the structure also reduces the effects of random noise sources, which create jitter in the propagating signals.

A parallel load capacitor-scaled delay line structure was chosen for the second, sub-gate delay interpolation level. INL does not accumulate in elements connected in parallel, and the delay difference between the elements was based on capacitors, which have a very low mismatch in CMOS technologies. The issue of mismatch between the synchronization delays on the second interpolation level was resolved by widening the interpolation range.

The versatility of the TDC was improved by integrating several measurement channels into the same circuit. The 7-channel TDC presented here is able to measure the time intervals from the start pulse to three separate stop pulses in one measurement and can also resolve the pulse widths or rise times at the same time. The main application for the circuit was laser distance measurement, where it can be used when several echoes arrive at the receiver and in order to compensate for the detection threshold problem known as walk error. Several new functions were developed and integrated into the circuit, including a Built-In Self-Test (BIST) in order to be able to test the circuit without external timing signals, a standard communication protocol Serial Peripheral Interface (SPI), calculation of the final result within the circuit by means of an Arithmetic Logic Unit (ALU), and the

two’s complement presentation format, which makes negative measurement values possible.

Measurements performed with the 7-channel TDC realized here in 0.35 µm CMOS describe the level of performance achieved. The TDC can achieve 8.88 ps interpolation resolution within the cycle time of a 20 MHz reference clock using only 8 delay elements on the first level and 14 on the second. The INL within the interpolator is less than 30 ps and the temperature drift in the results less than 0.5 ps/ºC. When the timing signals arrive at the TDC very close together a measurement error of ±20 ps due to cross-talk can be observed, but the linearity is better than ±2 ps provided the arriving timing signals do not interfere with each other. Rms precisions between several measured circuits fluctuate around 8 ps without result post-processing. To the author’s knowledge, the most precise to date, digital, fully integrated CMOS, long range time-to-digital converters have been designed in this work.

References

Abas MA, Russell G & Kinniment DJ (2007) Built-in measurement circuits – a comparative design study. IET Computers & Digital Techniques, 1(2): 87–97.

Baron RG (1957) The Vernier time-measuring technique. Proceedings of the IRE 45(1): 21–30.

Bowman KA, Tokunaga C, Tschanz JW, Raychowdhury A, Khellah MM, Geuskens BM, Lu SLL, Aseron PA, Karnik T & De VK (2011) All-digital circuit-level dynamic variation monitor for silicon debug and adaptive clock control. IEEE Transactions of Circuits and Systems-I:Regular papers, 58(9): 2017–2025.

Brockhaus H & Glasmachers A (1992) Single particle detector system for high resolution time measurements. IEEE Transactions on Nuclear Science, 39(4): 707–711.

Chen M, Reddy V, Carulli J, Krishnan S, Rentala V & Srinivasan V (2011) A TDC-based test platform for dynamic circuit aging characterization. Proc IEEE International Reliability Physics Symposium, Monterey, CA, USA, 36–40.

Chen P, Chen C & Shen Y (2006) A low-cost low-power CMOS time-to-digital converter based on pulse stretching. IEEE Transactions on Nuclear Science 53(4): 2215–2220.

Chen P, Chen C, Zheng J & Shen Y (2007) A PVT insensitive Vernier-based time-to-digital converter with extended input range and high accuracy. IEEE Transactions on Nuclear Science 54(2): 294–302.

Chen P, Liu S & Wu J (1997) Highly accurate cyclic CMOS time-to-digital converter with extremely low power consumption. IET Electronics letters 33(10): 858–860.

Chen P, Liu SI & Wu J (2000) A CMOS pulse-shrinking delay element for time interval measurement. IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 47(9): 954–958.

Chu D (1988) Phase digitizing sharpens timing measurements. IEEE Spectrum, 25(7): 28–32.

Conti M, Bendriem B, Casey M, Chen M, Kehren F, Michel C & Panin V (2005) First experimental results of time-of-flight reconstruction on an LSO PET scanner. Physics in Medicine and Biology, 50(19): 4507–4526.

Copani T, Vermeire B, Jain A, Karaki H, Chandrashekar K, Goswami S, Kitchen J, Chung HH, Deligoz I, Bakkaloglu B, Barnaby H & Kiaei S (2008) A fully integrated pulsed-LASER time-of-flight measurement system with 12ps single-shot precision. Proc IEEE Custom Integrated Circuits Conference, San Jose, California, USA: 359–362.

Daniels J, Dehaene W, Steyaert MSJ & Wiesbauer A (2010) A/D conversion using asynchronous delta-sigma modulation and time-to-digital conversion. IEEE Transactions of Circuits and Systems-I: Regular papers, 57(9): 2404–2412.

Dudek P, Szczepański S & Hatfield JV (2000) A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line. IEEE Journal of Solid-State Circuits 35(2): 240–247.

Fürstenberg K & Ahlers F (2011) Development of a low-cost automotive laser scanner – the EC project Minifaros. Advanced Microsystems for Automotive Applications 2011 – Smart Systems for Electric, Safe and Networked Mobility (G. Meyer and J. Valldorf, Eds.). Berlin: Springer: 149–158.

Gao GS & Partridge R (1991) High speed digital TDC for DØ vertex reconstruction. IEEE Transactions on Nuclear Science 38(2): 286–289.

Gerds EJ, Van der Spiegel J, Van Berg R, Williams HH, Callewaert L, Eyckmans W & Sansen W (1994) A CMOS time to digital converter IC with 2 level analog CAM. IEEE Journal of Solid-State Circuits 29(9): 1068–1076.

Goldstein BS & Dalrymble GF (1967) Gallium arsenide injection laser radar. Proc IEEE 55(2): 181–188.

Gorbics MS, Kelly J, Roberts KM & Sumner RL (1997) A high resolution multihit time to digital converter integrated circuit. IEEE Transactions on Nuclear Science, 44(3): 379–384.

Hajimiri A & Lee TH (1999) The design of low noise oscillators. Boston, Kluwer Academic Publishers.

Henebry WM & Rasiel A (1966) Design features of a start-stop time-to-amplitude converter. IEEE Transactions on Nuclear Science 13(2): 64–68.

Henzler S, Koeppe S, Lorenz D, Kamp W, Kuenemund R & Schmitt-Landsiedel D (2008) A local passive time interpolation concept for variation-tolerant high-resolution time-to-digital conversion. IEEE Journal of Solid-State Circuits 43(7): 1666–1676.

Hervé C & Torki K (2002) A 75 ps rms time resolution BiCMOS time to digital converter optimized for high rate imaging detectors. Nuclear Instruments and Methods in Physics Research A481: 566–574.

Hewlett Packard Inc. Time interval averaging. Application Note 162–1.

Hoppe DR (1982) Differential time interpolator. US patent 4,433,919, priority: 7.

Huang H & Sechen C (2009) A 22mW 227Msps 11b self-tuning ADC based on time-to-digital conversion. Proc Circuits and Systems Workshop, Dallas, USA, 1–4.

Huang H-Y, Wu S-D, Tsai Y-J (2007) A new cycle-time-to-digital converter with two level conversion scheme. Proc IEEE International Symposium on Circuits and Systems (ISCAS 2007), New Orleans, USA, 2160–2163.

Kalisz J, Pawlowski M & Pelka R (1987) Error analysis and design of the Nutt time interval digitizer with picosecond resolution. Journal of Physics E: Scientific Instruments 20(11): 163–169.

Kalisz J, Pelka R & Poniecki A (1994) Precision time counter for laser ranging to satellites. The Review of Scientific Instruments 65(3): 736–741.

Karadamoglou K, Paschalidis NP, Sarris E, Stamatopoulos N, Kottaras G & Paschalidis V (2004) An 11-bit high-resolution and adjustable-range CMOS time-to-digital converter for space science instruments. IEEE Journal of Solid-State Circuits, 39(1): 214–222.

Keränen P, Määtta K & Kostamovaara J (2011) Wide-range time-to-digital converter with 1-ps single-shot precision. IEEE Transactions on Instrumentation and Measurement, 60(9): 3162–3172.

Kostamovaara J (1986) Techniques and devices for positron lifetime measurement and time-of flight laser rangefinding. Acta Univ Oul C 37.

Kostamovaara J, Määttä K & Myllylä R (1991) Pulsed time-of-flight laser rangefinding techniques for industrial applications. Proc SPIE Conference on Intelligent Robotic Systems, 1614: 283–295.

Lee M & Abidi AA (2008) A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that Amplifies a Time Residue. IEEE Journal of Solid-State Circuits 43(4): 769–777.

Moses WW (2003) Time of flight in PET revisited. IEEE Transactions on Nuclear Science, 50(5): 1325–1330.

Mota M, Christiansen J, Débieux S, Ryjov V, Moreira P & Marchioro A (2000) A flexible multi-channel high-resolution time-to-digital converter ASIC. Proc IEEE Nuclear Science Symposium, Lyon, France, 2: 155–159.

Mota M, Christiansen J, Débieux S, Ryjov V, Moreira P & Marchioro A (2000) A flexible multi-channel high-resolution time-to-digital converter ASIC. Proc IEEE Nuclear Science Symposium, Lyon, France, 2: 155–159.

Myllylä R (1976) On the measurement technique of positron lifetimes. Acta Univ Oul C 10.

Mäntyniemi A (2004) An integrated CMOS high precision time-to-digital converter based on stabilized three-stage delay line interpolation. Acta Univ Oulu C 210.

Mäntyniemi A, Rahkonen T & Kostamovaara J (1997) A 9-channel integrated time-to-digital converter with sub-nanosecond resolution. Proc 40th Midwest Symposium on Circuits and Systems (MWSCAS'97). Sacramento, California, USA, 1: 189–192.

Mäntyniemi A, Rahkonen T & Kostamovaara J (2000) An integrated digital CMOS time-to-digital converter with sub-gate-delay resolution. Journal of Analog Integrated Circuits and Signal Processing 22(1): 61–70.

Mäntyniemi A, Rahkonen T & Kostamovaara J (2002) An integrated 9-channel time digitizer with 30ps resolution. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, CA, USA: 1: 266–267, 465.

Mäntyniemi A, Rahkonen T & Kostamovaara J (2009) A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method. IEEE Journal of Solid-State Circuits 44(11): 3067–3078.

Määttä K & Kostamovaara J (1998) A high-precision time-to-digital converter for pulsed time-of-flight laser radar applications. IEEE Transactions on Instrumentation and Measurement, 47(2): 521–536.

Määttä K (1995) Pulsed time-of-flight laser rangefinding techniques and devices for hot surface profiling and other industrial applications. Acta Univ Oul C 81.

Niclass C, Favi C, Kluter T, Gersbach M & Charbon E (2008) A 128×128 single-photon image sensor with column-level 10-bit time-to-digital converter array. IEEE Journal of Solid-State Circuits, 43(12): 2977–2989.

Nissinen I (2011) CMOS time-to-digital converter structures for the integrated receiver of a pulsed time-of-flight laser rangefinder. Acta Univ Oul C 390.

Nissinen I & Kostamovaara J (2009) A 2-channel CMOS time-to-digital converter for time-of-flight laser rangefinding. Proc IEEE International Instrumentation and Measurement Technology Conference (I2MTC'2009). Singapore, 1647–1651.

Nissinen I, Mäntyniemi A & Kostamovaara J (2003) A CMOS time-to-digital converter based on a ring oscillator for a Laser Radar. Proc IEEE European Solid-State Circuits Conference (ESSCIRC'2003). Estoril, Portugal, 469–472.

Nutt R (1968) Digital time intervalometer. The Review of Scientific Instruments 39(9):1342–1345.

Otsuji T (1993) A picosecond-accuracy, 700-MHz range, Si-bipolar time interval counter LSI. IEEE Journal of Solid-State Circuits 28(9): 941–947.

Park J & Kim W (1999) An auto-ranging 50-210Mb/s clock recovery circuit with a time-to-digital converter. IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco, CA, USA, 350–351.

Porat DI (1973) Review of sub-nanosecond time-interval measurements. IEEE Transactions on Nuclear Science ns-20(5): 36–51.

Rahkonen T & Kostamovaara J (1990) Pulsewidth measurements using an integrated pulse shrinking delay line. Proc. IEEE International Symposium on Circuits and Systems, New Orleans, LA, USA, 1: 578–581.

Rahkonen T (1993) Circuit techniques and integrated CMOS implementations for measuring short time intervals. Acta Univ Oul C 73.

Rahkonen T & Kostamovaara J (1994) Low-power time-to-digital and digital-to-time converters for novel implementations of telecommunication building blocks. Proc IEEE International Symposium on Circuits and Systems, London, UK, 3: 141–144.

Rahkonen TE & Kostamovaara J (1993) The use of stabilized CMOS delay lines for the digitization of short time intervals. IEEE Journal of Solid-State Circuits 28(8): 887–894.

Rivoir J (2006) Fully-digital time-to-digital converter for ATE with autonomous calibration. Proc IEEE International Test Conference, 1–10.

Räisänen-Ruotsalainen E (1998) Integrated time-to-digital converter implementations. Acta Univ Oulu C 122.

Räisänen-Ruotsalainen E, Rahkonen T & Kostamovaara J (2000) An integrated time-to digital converter with 30-ps single-shot precision. IEEE Journal of Solid-State Circuits 35(10): 1507–1510.

Schwartz DE, Charbon E & Shepard KL (2008) A single-photon avalanche diode array for fluorescence lifetime imaging microscopy. IEEE Journal of Solid-State Circuits, 43(11): 2546–2557.

Staszewski RB, Vemulapalli S, Vallur P, Wallberg J & Balsara PT (2006) 1.3 V 20 ps Time-to-digital converter for frequency synthesis in 90-nm CMOS. IEEE Transactions on Circuits and Systems-II: Express Briefs 53(3): 220–224.

Straayer MZ & Perrott MH (2008) An efficient high-resolution 11-bit noise-shaping multipath gated ring oscillator TDC. Proc IEEE Symposium on VLSI Circuits, Honolulu (HI), USA, 82–83.

Szplet R, Kalisz J & Szymanowski R (2000) Interpolating time counter with 100 ps resolution on a single FPGA device. IEEE Transactions on Instrumentation and Measurement, 49(4): 879–883.

Tisa S, Lotito A, Giudice A & Zappa F (2003) Monolithic time-to-digital converter with 20ps resolution. Proc. European Solid-State Circuits Conference (ESSCIRC'03), Estoril, Portugal, 465–468.

Toifl T, Vari P, Moreira P & Marchioro (1999) 4-channel rad-hard delay generation ASIC with 1 ns timing resolution for LHC. IEEE Transactions on Nuclear Science 46(3): 139–143.

Tonietto R, Zuffetti E, Castello R & Bietti I (2006) A 3MHz bandwidth low noise RF all digital PLL with 12ps resolution time to digital converter. Proc IEEE Solid-State Circuits Conference, Montreux, Switzerland, 150–153.

Townsend KA, Macpherson AR & Haslett JW (2010) A fine-resolution time-to-digital converter for a 5Gs/s ADC. Proc IEEE International Symposium on Circuits and Systems, Paris, France, 3024–3027.

Waizman A (1994) A delay line loop for frequency synthesis of de-skewed clock. Proc IEEE International Solid-State Circuits Conference, Digest of Technical Papers, San Francisco (CA), USA, 289–299.

Veneziano S (1998) Performances of a multichannel 1 GHz TDC ASIC for the KLOE tracking chamber. Nuclear Instruments and Methods in Physics Research A 409: 363–368.

Wilstrup J (1998) A method of serial data jitter analysis using one-shot time interval measurements. Proc International Test Conference, Washington, DC, USA, 819–823.

Yu J, Dai FF & Jaeger RC (2010) A 12-bit Vernier ring time-to-digital converter in 0.13 μm CMOS Technology. IEEE Journal of Solid-State Circuits, 45 (4): 830–842.

Original publications

I Jansson J-P, Mäntyniemi A & Kostamovaara J (2005) A Delay Line Based CMOS Time Digitizer IC with 13 ps Single-shot Precision. Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'2005). Kobe, Japan, 23–26 May 2005, 5: 4269–4272.

II Jansson J-P, Mäntyniemi A & Kostamovaara J (2006) A CMOS Time-to-Digital Converter with better than 10 ps Single-Shot Precision. IEEE Journal of Solid-State Circuits, 41(6): 1286–1296.

III Jansson J-P, Mäntyniemi A & Kostamovaara J (2009) Synchronization in a Multi-level CMOS Time-to-Digital Converter. IEEE Transactions on Circuits and Systems I: Regular Papers. 56(8): 1622–1634.

IV Jansson J-P, Mäntyniemi A & Kostamovaara J (2009) Multiplying Delay Locked Loop (MDLL) in Time-to-Digital Conversion. Proceedings of International Instrumentation and Measurement Technology Conference (I2MTC'2009). Singapore, 5–7 May 2009: 1226–1231.

V Jansson J-P, Koskinen V, Mäntyniemi A & Kostamovaara J (2012) A Multichannel High-Precision CMOS Time-to-Digital Converter for Laser-Scanner-Based Perception Systems. IEEE Transactions on Instrumentation and Measurement. 61(9): 2581–2590.

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