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SÄHKÖTIETOTEKNIIKAN KOULUTUSOHJELMA

DESIGN OF A LOW-NOISE OPTOELECTRONIC AMPLIFIER CHANNEL FOR A LASER RADAR

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ABSTRACT

The goal of this Master's thesis is to find and develop the best topologies and circuit structures for a low-noise amplifier channel for a laser radar application. In this work different topologies, their strengths, weaknesses and challenges are studied. Low-noise optoelectronic amplifier channels have been used extensively in a variety of applications such as wireless communication, optical receivers and laser radar. The common constraint for all the mentioned applications is the noise. The optical input signal for optoelectronic receivers can be very weak. In order to detect the signal reliably and accurately, the receiver must not add significant noise to the input signal.

Therefore, this thesis concentrates on improving the signal to noise ratio (SNR) by minimizing the noise sources, filtering the high frequency noise and amplifying the signal. In addition, the delay of the whole channel should be constant with respect to signal strength, supply voltage etc. variations. This low-noise optoelectronic amplifier channel can be employed in a laser radar to detect the distance of several kilometers.

Key words: laser radar, low-noise amplifier, optoelectronic receiver, long distance detection.

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TIIVISTELMÄ

Tämän diplomityön tavoitteena on etsiä ja kehittää sopivia piiriratkaisuja ja –rakenteita lasertutkan pienikohinaiseen vahvistinkanavaan. Työssä tutkittiin eri rakenteita, niiden vahvuuksia, heikkouksia ja haasteita. Pienikohinaisia optoelektronisia vahvistinkanavia on käytetty paljon useissa sovelluksissa kuten langattomassa viestinnässä, optisissa vastaanottimissa ja lasertutkissa. Näissä sovelluksissa yhteisenä haasteena on kohina. Optoelektronisen vastaanottimen tulosignaali voi olla hyvin heikko, joten tarkan ja luotettavan vastaanoton varmistamiseksi vastaanottimen itsessään tulee olla hyvin pienikohinainen.

Tässä työssä keskityttiinkin signaalikohinasuhteen (SNR) optimointiin minimoimalla itse kohinalähteet, suodattamalla korkeataajuista kohinaa ja vahvistamalla signaalia. Lisäksi koko kanavan viive oli pidettävä mahdollisimman vakiona eri signaalitasoilla, eri lämpötiloissa, eri käyttöjännitteillä jne. Työssä kehitettyä optoelektronista vahvistinkanavaa voidaan käyttää lasertutkissa mittaamaan etäisyyksiä kilometrien päässä oleviin kohteisiin.

Avainsanat: lasertutka, pienikohinainen vahvistin, optoelektroninen vastaanotin, etäisyyden mittaus kaukaisiin kohteisiin

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FOREWORDS

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- My lovely father who is my first teacher and hero; the first person who has taught me to think, to question, to be ambitious and hardworking.
- My invaluable mother who taught me love and generosity.
- My kind sisters and brother who have been always supportive.
- To my gorgeous homeland, Iran.

Oulu, September. 2014
Agheleh Yaghoobi

LIST OF ABBREVIATIONS AND SYMBOLS

A	Voltage gain
AC	Alternating current
APD	Avalanche photodiode
BW	Closed-loop bandwidth
CG	Common-gate
CMOS	Complementary metal-oxide-semiconductor field-effect transistor
CS	Common-source
DC	Direct current
Ge	Germanium
IC	Integrated circuit
InGaAs	Indium-Gallium-Arsenide
LNA	Low noise amplifier
NMOS	N-type metal-oxide-semiconductor field-effect transistor
MC	Monte Carlo simulation
MOSFET	Metal-oxide-semiconductor field-effect transistor
PM	Phase margin
PMOS	P-type metal-oxide-semiconductor field-effect transistor
RC	Resistor-capacitor
Si	Silicon
SiO_2	Silicon-oxide
SNR	Signal to noise ratio
TIA	Transimpedance amplifier
TDC	Time-to-digital converter
TOF	Time-of-flight
V	Volt, unit of voltage
A_{OL}	Open loop gain
C_c	Coupling capacitance
C_d	Diode capacitance
C_f	Feedback capacitance
C_{gs}	Gate to source capacitance
C_{gd}	Gate to source capacitance
C_I	Input capacitance
C_{PD}	Photodiode capacitance
C_T	Total capacitance
C_{ox}	Gate capacitance per unit area
fc	Corner frequency
f_p	Pole frequency
f_T	Unity-gain frequency
f_{Zf}	Zero frequency
g_m	Transconductance
gnd	Ground
$H(f)$	Transfer function
I_D	Drain current
I_{do}	Dark current
$I^2_{n,amp}$	Input-referred noise power spectrum
I_{po}	photocurrent
$i_{n,G}$	Shot noise of transistor gate

inn	Negative input voltage
$i_{n.MOS}$	Noise of MOS input transistor (here)
$i_{n,Rf}$	Feedback resistor thermal noise
i_{ovl}^{PP}	Input overload current
$i_{n.PD}$	Noise of a photodiode
$i_{n.TIA}$	Equivalent noise current source
inp	Positive input voltage
K_{ox}	Relative permittivity of SiO_2 (≈ 3.9)
L	Length of the channel in field-effect transistors
k	Boltzmann constant
q	Electronics charge (1.6×10^{-19} C)
R_D	Drain resistors
R_f	Feedback resistance
R_{in}	Input resistance
rms	Root mean square
R_L	Load resistance
Rs	Resistance of the current amplifier (here)
T	Temperature
t_{ox}	Thickness of the thin oxide under the gate
V_{dd}	Supply voltage
$V_{n,amp}^2(f)$	Noise power spectrum
$v_{I,ovl}^{PP}$	Input voltage swing
$voutn$	Negative output voltage
voutp	Positive output voltage
W	Width of the channel in field-effect transistors
Z_T	Transimpedance
β	Feedback factor
η	Quantum efficiency
Γ	Channel-noise factor

1. INTRODUCTION

Laser radar is a device to measure distance to a visible target by transmitting a laser pulse and receiving the reflected pulse, and measuring the time between the transmission and reception of the pulse. The most common lasers work within a wavelength range from 600nm to 1000nm, but they should have limited output power because eyes absorb those wavelengths. Alternatively, one may use a wavelength of 1550nm, which is eye safe.

The main task for the analog circuitry is to convert the received optical signal to an electrical one. The obtained electrical signal from the input transducer, in this case photo-detector, is current, which is directly proportional to the incident optical power. Photo-detectors are fabricated from different semiconductor materials and compounds such as Si, Ge and InGaAs. An avalanche photodiode (APD) is used in this work because of its high quantum efficiency (η), fast response, low-noise and its built-in gain stage [1]-[4].

In optical measurement, one popular method is time-of-flight (TOF). It includes variety of techniques, and e.g. pulsed TOF [5] - [8] laser distance measurement is based on using short laser pulses. A pulsed TOF often consists of a pulsed laser transmitter, optics, an APD, which receives the optical signal, an amplifier channel, timing detector and a time-to-digital converter (TDC), which measures the time interval between the original pulse and the reflected pulse.

When the distance is increased, the received pulse becomes weaker and can eventually be buried under the noise, i.e. the signal to noise ratio becomes low. Thus, the time interval measurement technique should be enhanced with sampling and averaging techniques. The principle hypothesis is that one is able to detect the signal after enough samples are taken and averaged as the noise will be attenuated in averaging because of its random characteristics. This method, like any other, requires a sensitive receiver. It is expected that such a receiver is capable of sensing a signal with 0.1 SNR after a few thousand samples.

This study investigates the design of a low-noise optoelectronic amplifier channel suitable for a TOF laser radar application. To optimize the noise performance, the best preamplifier topology is selected and carefully optimized. The noise is also limited in the postamplifier stage by rejecting out-of-band signal, and an optimum noise point where the receiver is stable in all conditions, including different temperatures and process corners parameters, is selected.

This thesis consists of the study of known topologies, their strengths, weaknesses, constraints and enhancements in chapter 2. It is followed by a proposal for a suitable topology for the receiver. Chapter 4 describes the design of the receiver using a 0.35μm CMOS technology. Chapter 5 assesses the performance of the receiver by means of simulation and reports the results. Eventually, a discussion and conclusion is provided.

2. OVERVIEW OF SAMPLING RECEIVER TECHNIQUES

2.1. Foundation of a low SNR pulsed receiver

The signal to noise ratio (SNR) is one of the key factors for any receiver and often specifies the accuracy of a receiver, and obviously having lower noise means that the receiver is more sensitive. The noise performance of the overall receiver is usually determined by the front-end (i.e. input) stage. In other words, the noise which is introduced in the input stage is added to the signal and travels through the receiver stages.

In this thesis work, the input transducer of the receiver is an APD, which like all real components, is non-ideal and inherently adds some noise to the receiver. The environment typically contains different light sources and wandering beams which are considered as noise. Therefore, the reflected light level may become too low compared to the noise level. A low SNR receiver, which aims to work under these circumstances, should be able to sense the changes of the photodiode current magnitude and resolve it.

One of the helpful techniques which increases the performance of a low SNR receiver is using a pulsed signal in the transmitter. Pulsed signal input is commonly used when the process is non-continued. In pulsed systems it is possible to concentrate the available energy to a short pulse with high peak power (amplitude), which improves the accuracy in the timing detection. Also, it is possible to modulate the transmitted signal in order to make the receiver more immune to random input signals. Nonetheless, the ability of demodulating the signal depends on the SNR level.

2.2. Basics of sampling and averaging technique

In order to convert the output of analog receivers to digital events, generally, comparators are employed. The data is recovered by comparing the signal with a threshold level and signals which are higher than the threshold pass through the comparator and weaker ones are blocked. To detect the signal with this technique, the signal to noise ratio needs to be high enough. Several approaches can be used to improve the SNR. The first one is to amplify the signal by means of a low noise amplifier (LNA), and the second one is to add extra poles in the post amplifier to filter out-of-band noise. The comparator can be clocked or asynchronous (free running) one, and in this work the latter one is used. An example of a differential optoelectronic receiver is shown in Figure 1.

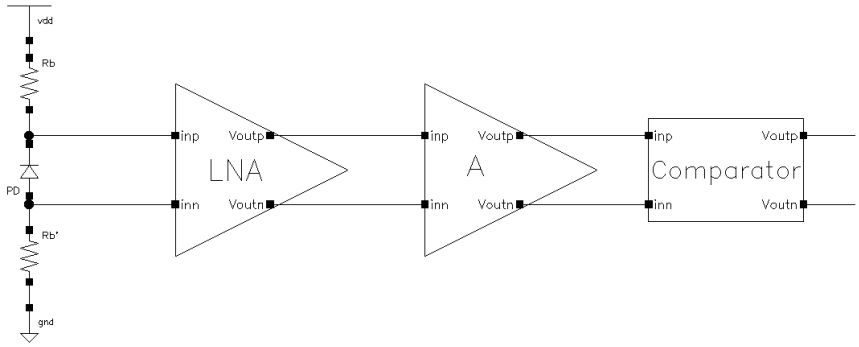

Figure 1. Optoelectronic receiver with a photodiode input.

Figure 2 tires to visualize the operation of a receiver when the SNR is low. It shows the original signal without noise (red), the channel input with the signal and noise (green), the sampling clock (blue) and the channel output (pink). The channel input is a sum of the input current pulse and a hypothetical white noise source which presents the noise at the input of the receiver channel. The output of the proposed receiver shows that when the SNR is low the receiver detects many false signals. Hence, so called sampling technique is employed to process the result and recover the original data.

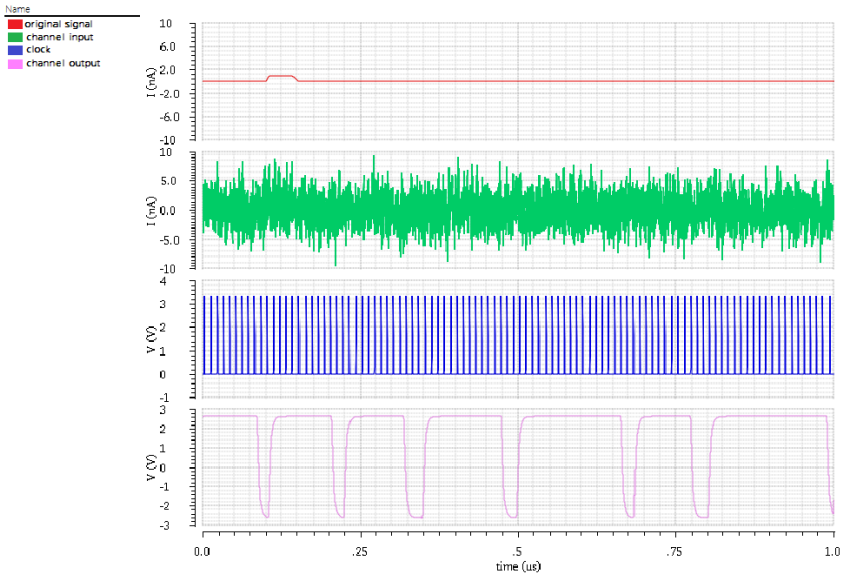

Figure 2. Input current of the receiver without noise, input current signal with noise, and the output voltage signal of a low SNR receiver channel.

In the sampling technique a number of the outputs are averaged. In this technique the signal (deterministic) amplitude adds up directly, i.e. with n samples the amplitude is increased to n times the original one. Due to the random nature of noise, the rms value of the summed noise is increased to only $\sqrt{n}$ times the original value. As the averaging improves the signal by factor of n, and rms value of the noise only increases by factor of $\sqrt{n}$, the SNR grows by $\frac{n}{\sqrt{n}} = \sqrt{n}$. Eventually the random characteristic of noise helps the sampling technique to detect the original pulse.

Figure 3 shows the block diagram of a sampling receiver channel with the analog receiver channel followed by a digital signal processing part, and in which the #n

defines the number of samples taken with a sampler from the output of the comparator. The digital processor takes care of the sampling and averaging, as well as the final distance calculation.

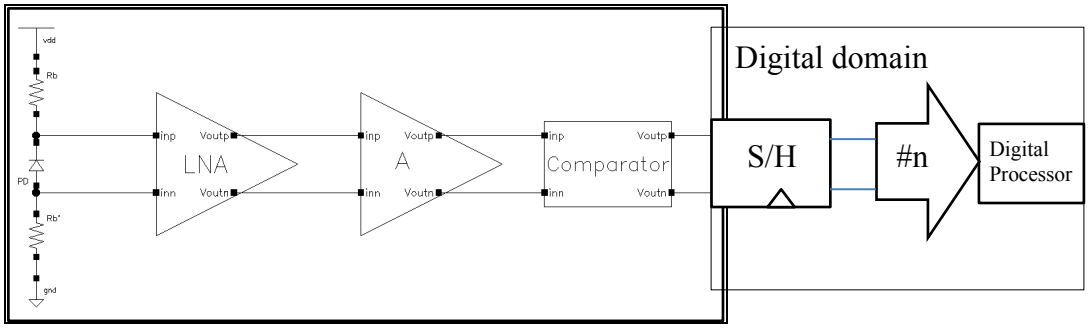

Figure 3. Sampling technique in an optical receiver.

2.3. Requirements for the pulsed receiver

The first task for a low SNR pulsed receiver is to convert the low-level photo-detector current to a voltage. The easiest type of a current to voltage (I-V) convertor is using a single RC circuit as shown in Figure 4. A voltage amplifier can then be used to amplify the resulting voltage V1.

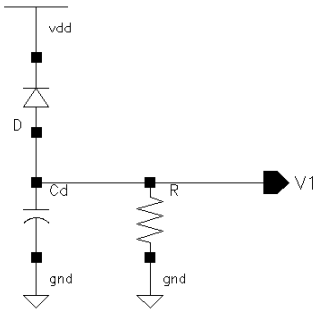

Figure 4. Simple I-V convertor.

The problem with using a front-end resistor (R) is that the bandwidth will be limited by the R and C_d composed of the diode capacitance and all the parasitic capacitances. The other disadvantage of this topology is the dependency of the bandwidth and signal to noise ratio on each other, i.e. lower R increases the bandwidth but reduces the SNR. To override this effect one can substitute the RC circuit with a transimpedance amplifier (TIA) as shown in Figure 5.

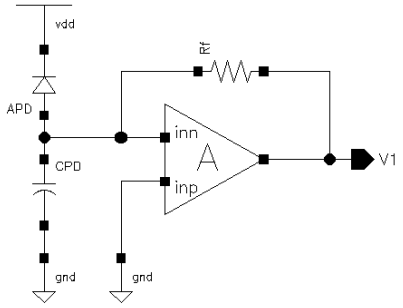

Figure 5. I-V convertor by means of a transimpedance amplifier.

A transimpedance amplifier is composed of a voltage amplifier and a feedback resistor, and benefits from having low input impedance (ideally zero). Ideally a high-gain, high bandwidth op amp is needed for good performance.

At high frequencies the bandwidth is limited due the op amp bandwidth. The bandwidth of a first order feedback transimpedance amplifier is defined as

$$\mathrm{BW} = \frac{1 + \mathrm{A}}{2\pi R_f \mathrm{C}_{PD}}, \tag{1}$$

where R_f is the feedback resistor and C_{PD} is the total capacitance of the photodiode plus all the stray capacitances. The transimpedance amplifier suffers from high power consumption and area, because according to [9] and [10], the transimpedance amplifier achieves the best noise performance when

$$C_I = C_{PD}\,, \tag{2}$$

where C_I is the total input capacitance and is given by

$$C_I = C_{gs} + C_{gd}\,, \tag{3}$$

where C_{gs} is the gate to source capacitance and C_{gd} is the gate to drain capacitance. In other words, a photodiode with large capacitor necessitates the transimpedance amplifier to have a large input transistor which results in large area and power consumption to have minimum noise value.

The transimpedance amplifier is designed to minimize the input channel noise, while the following stages are allocated to achieve the gain. Thus in the second stage, postamplifier, the noise is not so critical factor, but the stability, gain and bandwidth are the main focus. Moreover an offset compensation is included in this level.

The third stage, comparator, is a wideband amplifier chain for amplifying and converting the signal to digital domain. Depending on the digital circuit input, a latch may be added at the end of the comparator. A latch is a stage using positive feedback to amplify the signal level to zero or supply voltage. Figure 6 shows the block diagram of the designed receiver. The details of each block are discussed in the next chapters.

In this work an avalanche photodiode is used because of its high gain, fast response and low noise which make it a good choice for distance measurement technique. The avalanche photodiode needs a high biasing voltage in the range of a few tens to a few hundreds of volts, thus AC coupling capacitances (C_{c1} and C_{c2}) are used to block the DC signal.

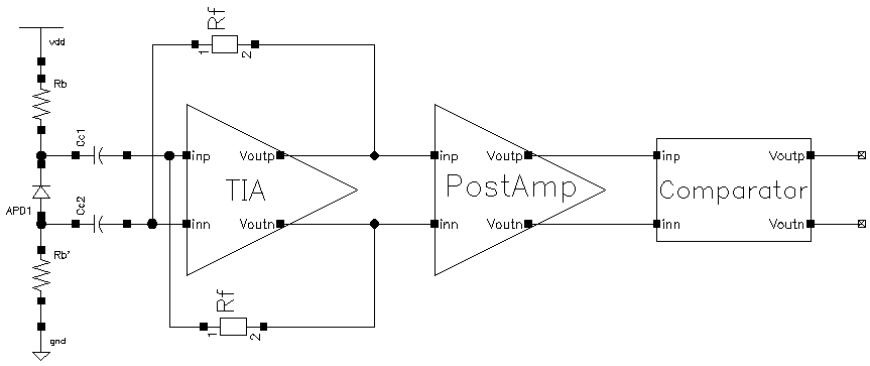

Figure 6. Designed low SNR pulsed receiver with an APD input.

3. PREAMPLIFIER CHALLENGES

This chapter discusses the main challenges of designing a preamplifier. Here, the preamplifier is a differential transimpedance amplifier as shown in Figure 7.

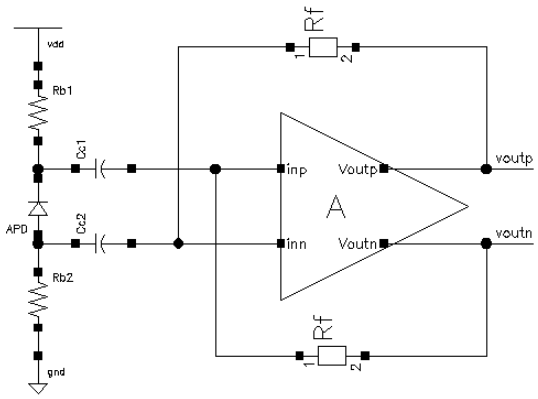

Figure 7. Differential transimpedance amplifier.

3.1. Different topologies

Transimpedance amplifier is a current to voltage convertor, and the most common way to implement it is using an operational amplifier and a feedback resistor. In designing a transimpedance amplifier, one can apply a few different topologies. The input stage of the TIA can be common-gate (CG) stage (it is also called open-loop TIA) or common-source (CS) stage (it is normally called feedback TIA). The TIA can be single-ended or differential one. Furthermore, the feedback resistor can be a fixed resistor, a variable resistor or an active load. Current-mode TIA and burst-mode TIA are other types of transimpedance amplifiers [10].

3.1.1. Common gate and common source amplifier

The common-gate (CG) amplifier, which is transimpedance amplifier by its nature is often used in high-frequency applications and has a very high bandwidth due to its low input impedance. As Figure 8 illustrates, the input current is applied to the source of the input transistors and it generates voltage in the drains where the transimpedance gain is equal to the drain resistors. The main drawback of using common-gate is that both the noise of input transistors and the drain resistors have direct effect on the noise level, and therefore it may be difficult to have as low noise level as with the common source amplifier.

The common-source (CS) amplifier is a voltage-to-voltage amplifier. In order to make a transimpedance amplifier with a common-source stage amplifier, feedback resistors are implemented to work similar as the drain resistors in the common gate amplifier. The feedback resistors convert the input current to the output voltage, hence, a voltage-to-voltage amplifier changes to current-to-voltage amplifier. Figure 9 shows a differential common-source CMOS transimpedance amplifier where R_{f1} and R_{f2} are the feedback resistors.

The feedback resistors define the gain and bandwidth, and as it will be explained later, higher R_f can improves the SNR. Nevertheless, as with any feedback system, the phase shift resulting from the feedback resistors and the input capacitance (C_I) of the amplifier can cause oscillations. To mitigate this effect, often a small compensation capacitor, so called feedback capacitor (C_f), is added across the R_f to make the amplifier stable. If the R_f is much larger than input resistor (R_{in}), the C_f can be estimated by [11]

$$C_f = \frac{C_I}{2(\frac{R_f}{R_{in}} + 1)}. \tag{4}$$

Comparing the CG and CS transimpedance amplifiers, one drawback of the CG stage is that the noise of the CG stage is higher than the CS stage because the noise of the input transistors, drain resistors (R_D) and source resistor directly impacts the input-referred current noise. Moreover if the current gain of the CG stage is less than one, the input-referred current noise caused by the drain resistor increases and the transimpedance decreases. Eventually the power consumption is higher in the CG stage than in the CS [10]. All in all a common-gate stage seems to be more useful in integrated high bandwidth TIA where the input signal is large enough and the noise is not critical factor, such as in optical communication circuits.

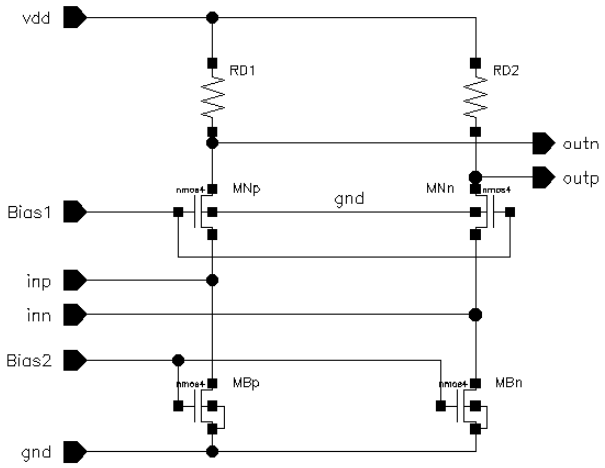

Figure 8. Basic differential CG amplifier.

In a CS stage transimpedance amplifier it is easier to reduce the input-referred current noise, which is a crucial factor in low SNR application, by increasing the size of the input transistor and feedback resistor. In addition, the gain of a CS amplifier is higher because it has low output impedance.

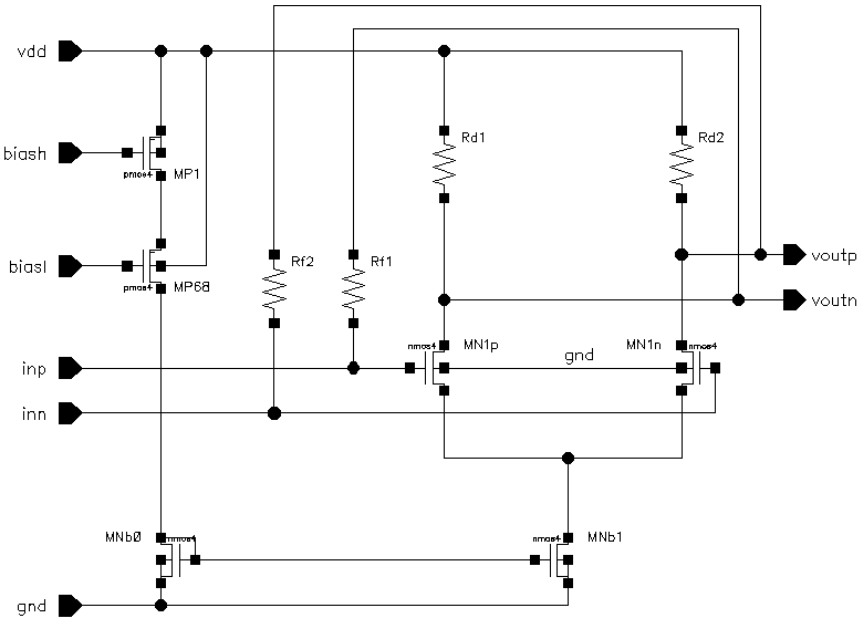

Figure 9. Basic differential CS amplifier.

3.1.2. Differential transimpedance amplifier

The transimpedance preamplifier can be single-ended or differential on. Sometimes the benefits of differential TIA over a single-ended TIA are significant. One of the most important one is the better immunity towards power supply and substrate noise, and bigger voltage swing. So the differential TIA is more applicable in integrated low SNR receivers. Also, a differential stage doesn't need a reference voltage if it is connected to differential circuit. The disadvantages of a differential TIA can in some applications be higher power consumption and larger input-referred current noise.

A fully differential TIA needs a differential photodiode, and therefore the avalanche photodiode used in this work is connected in balanced configuration as shown in Figure 7. All formulations which have been presented for a single-ended TIA are valid in differential TIA if the input voltage is replaced by the subtraction of the positive and negative input voltages (inp,inn) and the output voltage by the subtraction of the positive and negative output voltages (voutp, voutn).

3.1.3. Variable feedback resistor and active-feedback

The input current amplitude for a transimpedance amplifier in optical receivers may vary in a wide range due to varying power of the transmitted pulse, the distance, the reflectance of the target and the environment. Nonetheless, in a transimpedance amplifier with voltage amplifier with a gain of A and a feedback resistor of R_f, there is a limit for the dynamic input range which is defined by the input overload current and the sensitivity of the TIA. The input overload current (i_{ovl}^{PP}) is directly proportional to the gain (A) and the input voltage swing ($v_{I,ovl}^{PP}$), and inversely proportional to the R_f:

$$i_{ovl}^{PP} = (A+1)\frac{v_{I,ovl}^{PP}}{R_f}. \quad (5)$$

In addition, the sensitivity also turns out to be inversely proportional to the feedback resistor, so that with an adaptive feedback resistor the dynamic range could be enhanced. As the sensitivity is related to $1/\sqrt{R_f}$ for a weak signal and almost independent of the feedback resistor for a strong signal, the dynamic range is extended if the feedback resistor reduces for strong input signals and increases for weak ones.

To implement the variable feedback, a MOS transistor which is working in the linear region can be used in parallel with a fixed feedback resistor (R_f). A comparator output which compares the output signal with a threshold level can control the gate voltage of the MOS. The drawback of a variable R_f is the risk of instability which can happen when the feedback resistance is decreased while the other elements are fixed [10]. Hence, in practice the implementation of the adaptive resistor is challenging.

Another replacement of a fixed feedback resistor is a voltage-controlled current source or a trans-conductance, e.g. a transistor. If the g_m of a transistor is chosen to be $1/R_f$, the TIA is working the same way as a fixed feedback resistor TIA. The advantage of using active-feedback is that the voltage output amplifier is not loaded by a resistive load, while the disadvantages are that the input capacitance and noise are increased and the linearity is decreased [10].

3.1.4. Current-mode transimpedance amplifier

A current-mode TIA, as shown in Figure 10, has a current mirror instead of a common-gate or common-source stage at its input. If the input resistance of the current amplifier (R_s) is considered to be small and the width of the output transistor of the current mirror is A times bigger than the input transistor width, the input resistance (R_{in}) of the current-mode TIA at low frequency is

$$R_{in} = \frac{R_s}{A+1}, \quad (6)$$

whereas at high frequency $R_{in}=R_s$. An advantage of a current-mode TIA is the independency of its performance on the photodiode capacitance due to the small R_s, and as a result small R_{in}. However, similar to a common-gate stage, its main drawback is that there are more noise sources than in a common-source TIA.

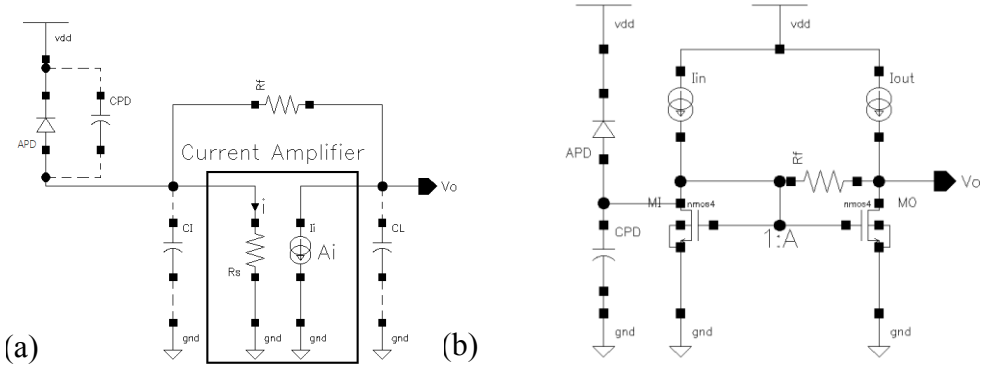

Figure 10. (a) current-mode TIA, (b) current-mode TIA with a current mirror.

Another approach to implement a nonlinear TIA is to replace the feedback resistor with a resistor (R_1) in parallel with a series combination of a diode and a resistor (R_2). For small input signals the diode is turned off and the transimpedance is defined by R_1. For large input signals the feedback resistance is equal to parallel resistance of R_1 and R_2, and as a result the lower feedback resistance prevents the TIA from overloading.

3.1.5. Transimpedance amplifier used in this work

The aforementioned types of TIA can be further modified by a variation of techniques such as gain boosting, transfer function peaking etc. for specific applications. There seems not to be one topology with superior performance fitting all applications, so the topology must be chosen based on the work constraints and modified to achieve the best result.

In the case of laser radar, usually the amplitude of the input signal is unpredictable and most of the time it is very small. So the key requirement for this type of receiver is low noise TIA which is working reliably and stably in different temperatures, with different supply voltages and in different silicon process corners. For all the mentioned reasons a CS TIA with a large shunt feedback resistor has been employed for this work.

3.2. Transimpedance amplifier specifications

The main specifications for a TIA are transimpedance (Z_T), bandwidth, overload response and input-referred rms noise current. The transimpedance has a limit based on the required bandwidth and technology [13]. Thus, the transimpedance of the presented differential TIA is two times the shunt feedback resistor.

$$Z_T = \frac{\Delta(V_{outp} - V_{outn})}{\Delta i_{APD}} = 2R_f\,, \tag{7}$$

where $\Delta(V_{outp} - V_{outn})$ is the output voltage change and Δi_{APD} is the APD current change.

The transimpedance bandwidth (BW) of a transimpedance amplifier is usually presented by the -3dB bandwidth. If we consider that the TIA has a large op amp gain of A, and an input capacitance of C_I then

$$BW_{-3dB} = \frac{1 + A}{2\pi\, R_f C_T}, \tag{8}$$

where

$$C_T = C_I + C_{PD}. \tag{9}$$

As presented in section 3.1.3, there is an upper limit to the amplitude of the input signal, input overload current (i_{ovl}^{PP}), which can be handled in linear manner. The low input resistance of the feedback TIA improves the input overload current.

The input-referred noise current is usually the most important parameter of a TIA and is defined as the equivalent noise current source ($i_{n.TIA}$) at the input of a noiseless TIA producing the same noise at the output as all the real noise sources together [2]. To ease working with the TIA, input-referred root mean square (rms) noise current, which is the rms output noise voltage divided by the TIA transimpedance, is used in this work. The input-referred rms noise current that relates directly to the sensitivity of the TIA and can be expressed by a single number in the range of nanoamperes is given by [10]

$$i_{n.rms} = \frac{1}{R_T}\sqrt{\int_0^{2BW} |Z_T(f)|^2 \; . {I_n}^2(f)\, df}\,, \tag{10}$$

where R_T is the transimpedance limit defined as (11), and $Z_T(f)$ is the frequency response of the transimpedance and $I_n^2(f)$ is the input-referred noise spectrum.

$$R_T = \frac{2A}{A + 1}\, R_f\,. \tag{11}$$

3.3. Noise

In electronics any unwanted or random signal which interferes the target signal is called noise. The output voltage of any non-ideal linear channel consists of two parts, signal voltage and noise voltage. The noise voltage is generated by the transimpedance amplifier and the photodiode. For an amplifier with input-referred noise power spectrum $I_{n,amp}^2$ and transfer function of H(f), the noise power spectrum at the output is calculated as

$$V_{n,amp}^2(f) = |H(f)|^2\, I_{n,amp}^2(f). \tag{12}$$

The noise of a photodiode is inherently shot-noise [2] and is given by

$$i_{n.PD} = [2e(I_{do} + I_{pho})M^2FB]^{1/2}, \tag{13}$$

where I_{do} is the dark current, I_{pho} is photocurrent, M is multiplication factor, F is called excess noise factor which is a function of M and B is the frequency bandwidth of the photodiode. In this work, the noise of the noise of the avalanche is quite small compared to the channel noise, so it can be ignored.

As mentioned, the noise is usually the most important parameter of a receiver channel as it defines the receiver sensitivity. In order to minimize the input-referred noise current, first the main noise sources should be identified. In Figure 11 the noise sources of a single-ended TIA with a feedback resistor are illustrated. $i_{n,Rf}$ models the feedback resistor thermal noise, $i_{n,G}$ models the shot noise generated by the gate current of the input transistor, $i_{n,D}$ models the MOS channel noise and $i_{n,TIA}$ is the equivalent input noise source modeling the effect of all the noise sources.

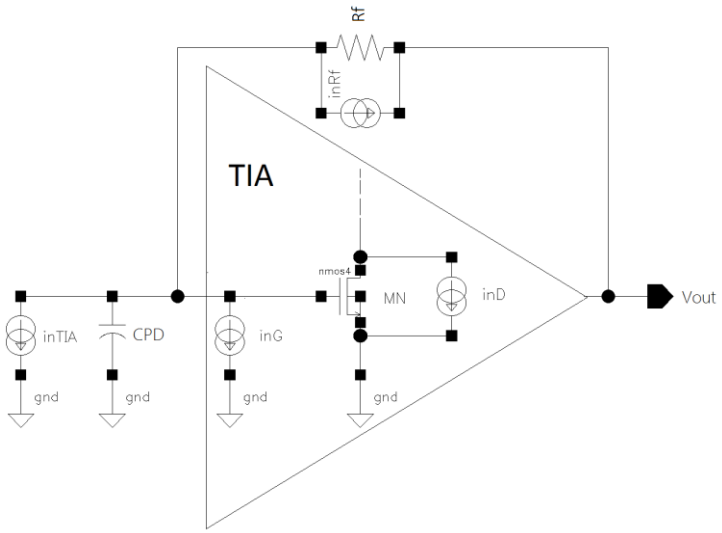

Figure 11. Noise source model in a TIA with MOSFET input transistor. [10]

From Figure 11 one can see that the input-referred noise current spectrum of a TIA ($i_{n.TIA}$) consists of two main components, the noise of the feedback resistor ($i_{n,Rf}$) and the input referred noise of the amplifier which in a properly designed amplifier is practically the noise of the input transistor ($i_{n.MOS}$), and it is calculated from

$$i_{n,TIA}^2(f) = i_{n,Rf}^2(f) + i_{n,MOS}^2(f). \tag{14}$$

The thermal noise of the feedback resistor caused by the random motion of charge carriers is a significant noise source. In T degree Kelvin, the noise current spectrum of the feedback resistor R_f can be written as

$$i_{n,Rf}^2(f) = \frac{4kT}{R_f}, \tag{15}$$

where k is Boltzmann constant.

The input transistor noise spectrum can be broken to two types of noise, shot noise ($i_{G,n}$) and channel noise ($i_{n,D}$). The shot noise of the transistor gate current, which is negligible in low speed receivers due to low gate current, contributes directly to the input-referred noise but the thermal noise of the channel needs to be

transformed to the input-referred noise current. As a result, the noise spectrum of input transistor is written as

$$i_{n,MOS}^2(f) = i_{n,G}^2 + i_{n,D}^2(f). \quad (16)$$

The spectrum of the shot noise of the front-end transistor due to its gate current i_G, caused by the random statistical fluctuations of the discrete charge carriers, is written as

$$i_{n,G}^2 = 2qi_G \quad (17)$$

where q is one electronics charge (1.6×10^{-19} C). As said, this current is negligible in the amplifier used in this work.
The channel noise of the input MOS transistor is thermal noise due to the channel resistance and its spectrum is calculated from

$$i_{n,D}^2(f) = 4kT\Gamma.\frac{1}{g_m R_f^2} + 4kT\Gamma\,.\frac{(2\pi C_T)^2}{g_m}\,.f^2, \quad (18)$$

where Γ is the channel-noise factor (between 0.7 to 3.0 for MOSFET), C_T (Equation (9)) is the total capacitance, g_m is the transconductance of the transistor and f is frequency [10]. The first term is negligible when $g_m R_f >> \Gamma$, which is the case here due to the large feedback resistor and input wide transistor.

Apart from the noise sources which are mentioned there are other noises such as 1/f noise at low frequencies, f noise at high frequencies, load resistor noise and the noise of the subsequent gain stage. However, if the first gain stage has high enough gain, the load resistor noise and noise of the subsequent gain stage can be neglected. Therefore, the input-referred noise current of TIA which is presented in Equation (14) can be simplified

$$i_{n,TIA}^2(f) = \frac{4kT}{R_f} + \ 4kT\Gamma\,.\frac{(2\pi C_T)^2}{g_m}\,.f^2. \quad (19)$$

3.4. Stability

In a real non-ideal differential TIA with feedback resistors (R_f), the feedback system may become unstable if at frequency f_1 the phase shift in the loop is so high that it changes the negative feedback to positive and at the same frequency the open loop gain is higher than 1 so that signal can buildup. [14] Two main approaches are suggested to achieve stability; the first is to decrease the phase shift and the second is to decrease the gain.

The instability limits the achievable bandwidth. The effect of the parasitic capacitances, the limited bandwidth of the amplifier and the frequency response of the photodiode are the main factors limiting the bandwidth. In addition, the internal poles of the amplifier, the delay in the large feedback resistor (in effect a distributed RC network), the bonding wire inductances and other non-ideality factors make the ac response of feedback TIA complex.

Any current-to-voltage amplifier is subject to an inherent response limit caused by the parasitic capacitances and the limited amplifier bandwidth. However, their limitation usually reside at higher frequencies than the feedback resistor bandwidth limit. The high feedback resistor and the equivalent input capacitance dominates the response at high frequencies and set the bandwidth of the TIA.

Figure 12 shows the bode diagram (logarithmic gain vs. logarithmic frequency) of the transimpedance amplifier of Figure 5 (here voltage amplifier is assumed to be a one-stage amplifier). The A_{OL} is the open loop gain, I-to-V gain is the frequency response of the TIA and the inverse of the feedback factor is 1/β. The R_f and C_T (the equivalent capacitance at the TIA input) define the feedback factor:

$$\beta = \frac{1}{1 + R_f C_T s}. \tag{20}$$

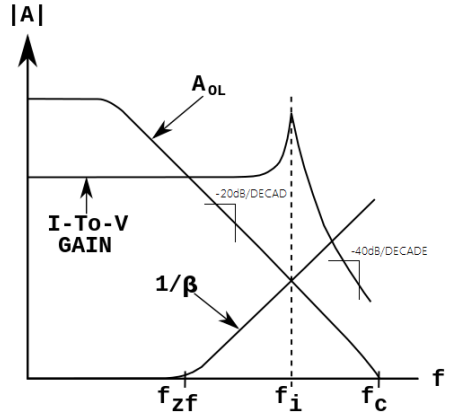

Figure 12. Bode diagram of an uncompensated one-stage TIA. [15]

The dominant pole in the A_{OL} curve generates a -20dB slope. The frequency of the zero (f_{zf}) which generates a +20dB slope in the 1/β curve is given by

$$f_{zf} = \frac{1}{2\pi R_f C_T} \tag{21}$$

and thus the intersection point (at frequency f_i) receives a 360 degree phase shift. As a result, oscillation occurs at a frequency f_i given by

$$f_i = \sqrt{f_{zf} f_c}\,, \tag{22}$$

where fc is the unity-gain crossover frequency at which the gain of voltage amplifier is one (0dB).

To compensate for the phase shift, as presented in Equation (5), a feedback capacitor (C_f) is employed, which bypasses the feedback resistor at high frequencies. As a result, a zero is generated at a frequency of

$$f_C = \frac{1}{2\pi R_f C_f} \tag{23}$$

and this adds phase lead so that the phase shift is reduced and the compensated feedback factor changes to

$$\beta = \frac{1 + R_f C_f s}{1 + R_f (C_T + C_f) s}. \tag{24}$$

It also reciprocates a pole generated at the frequency of f_{zf} which is given by

$$f_{zf} = \frac{1}{2\pi R_f (C_T + C_f)}. \tag{25}$$

The Bode diagram in Figure 13 shows the frequency response of the feedback TIA compensated by means of a feedback capacitance, and where the oscillation is almost eliminated.

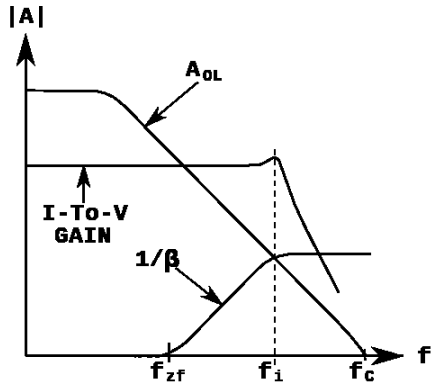

Figure 13. Bode diagram of a compensated one-stage TIA. [15]

In this thesis work, to achieve high enough gain bandwidth the internal amplifier has three stages. Improving the stability, when using a three-stage amplifier is more challenging than with a one pole amplifier because, the three-stage amplifier contains many poles which interfere with the dominant pole. Thus, poles should not be placed near the same frequency, and especially not in the same frequency with the dominant pole. Also, extra capacitance may be applied to filter the high frequency noise and enhance the signal to noise ratio.

There is a tradeoff between noise reduction and stability. Lowering the pole frequencies of the amplifier stages reduces noise significantly but causes instability which results in overshoot in the AC response, ringing in the transient respond and lack of phase margin.

Also, the delay in the feedback resistor R_f (distributed RC filter in a real layout) increases the phase shift in the loop and therefore worsens the stability. In this case increasing the gain or phase-margin in the open-loop circuit can compensate for the delay of the feedback path. Another way to enhance the phase margin is to add a feedback capacitor in parallel with the feedback resistor.

4. DESIGN OF THE RECEIVER

4.1. Block diagram

The main requirements for this thesis work are input-referred rms noise current, the bandwidth of the analog signal path, the preamplifier phase margin and the effective transimpedance (see Table 1).

Table 1. Design requirments

Design specification	Goal
Input-referred rms noise current after the preamplifier	<3nA
Minimum channel bandwidth after the postamplifier	>10MHz
Preamplifier phase margin	>60
Effective transimpedance	5-10MΩ

The proposed receiver core includes a differential TIA with shunt feedback resistor and capacitor, a post amplifier, a comparator, a buffer and two bias generators as shown in Figure 14.

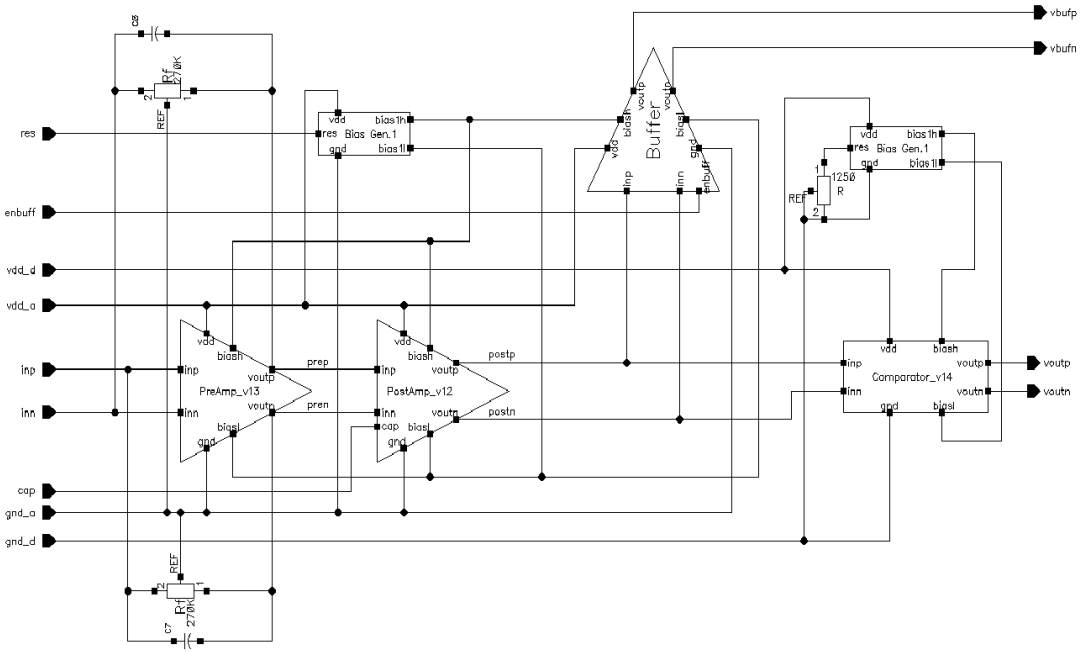

Figure 14. Block diagram of the receiver.

As shown in Figure 14 the amplifier chain has its own bias generator, positive supply voltage (vdd_a = 3.3V) and ground (gnd_a), and the comparator has its own bias generator, positive supply voltage (vdd_d = 3.3V) and ground (gnd_d). The reason is that the comparator bias line, supply voltage and ground connection could be very noisy due to its speed and digital nature. Therefore usually these connections have separate IOs on the chip. Labels res and cap IOs are dedicated to an external resistor of the bias generator and an external capacitor of the offset-cancellation

circuit respectively. The last groups of IOs are the positive and negative input signals (inp and inn) and the positive and negative output signals (voutp and voutn).

4.2. Preamplifier

The designed preamplifier shown in Figure 15 has three stages (PreAmp_L1, L2 and L3), two feedback resistors and capacitors (R_f, C_{f1} and C_{f2}) and one filtering capacitor which is divided to two parts (C_1 and C_2).

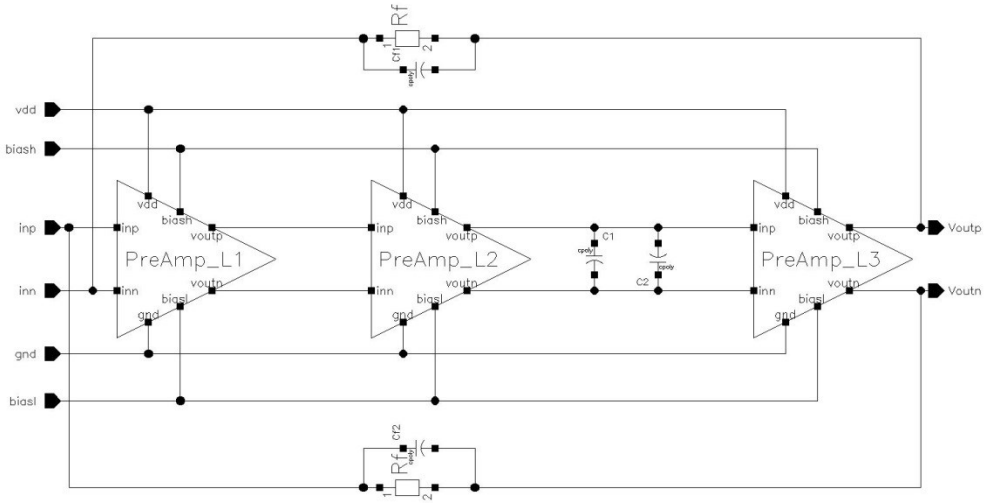

Figure 15. Preamplifier block diagram.

The most challenging part of the preamplifier design is the input stage (PreAmp_L1) because of its dominant effect on the input-referred current noise. To implement this stage, a common-source amplifier has been chosen (see chapter 3), i.e. a voltage-to-voltage amplifier stage. Hence, the sizing of transistors is the primary consideration in designing the front-end amplifier stage.

In Chapter 2 it is studied that the optimum noise is achieved when the input capacitances (C_I) size follows Equation (2). Thus, the capacitive load of the input transistor which is dictated by the photodiode capacitor is the starting point. The avalanche diode which has been selected for this project has 1.5pF capacitive load. Employing Equation (3), if C_I is equal to 1.5pF, the noise performance is the best. Using Equation (26) and selecting minimum value for the length of the transistor, the width can be solved.

$$C_{gs} = \frac{2}{3} WLC_{ox} + L_{ov}W, \tag{26}$$

where W is the width, L is the length, L_{ov} is the gate to source overlap and C_{ox} is the gate capacitor per unit area is given by

$$C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}}, \tag{27}$$

where K_{ox} is the relative permittivity of SiO_2 (≈ 3.9) and t_{ox} is the thickness of the thin oxide under the gate. The gate-drain capacitance ($C_{gd)}$ is given by

$$C_{gd} = C_{ox} W L_{ov} \tag{28}$$

and is non-negligible for large transistors.

As a result of the optimization the W/L ratio of the input transistors is 1000 µm/ 0.35 µm and the input capacitance (C_I) is about 1.26 pF. Further increasing the transistors width has no significant effect on the noise optimization. Figure 16 illustrates the front-end stage of the preamplifier.

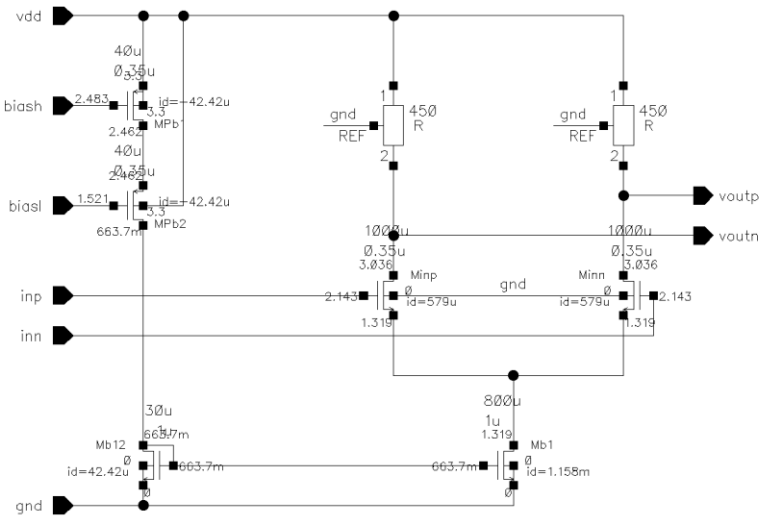

Figure 16. Preamplifier input stage.

g_m-constant bias technique, which is explained in detailed in section 4.5 is used to bias the amplifier. In the g_m-constant biasing technique the transconductance of a transistor is kept constant by properly changing the current in different circumstances, e.g., temperatures or process corners. Consequently, as the current can vary in a wide range, a transistor which is working in saturation region in normal temperature and typical process corner may not work in the same region in another situation. Thus, it is important to predict the extreme situations.

In order to secure proper operation points with the changing bias current, which can push transistors to triode region, the voltage headroom of transistors is designed high enough. To this end, the drain resistor (R_D) is selected to be as small as 450 Ω to provide the necessary voltage headroom. As a result, the circuit is less sensitive to the changes in the temperature and/or fabrication.

Although the drain resistor is selected to be very small, the gain of the first stage should be as large as possible in order to improve the signal to noise ratio. Therefore, the bias current of the input stage of preamplifier is chosen to be as large as 5 mA. Increasing the bias current, the g_m of the input transistor is enhanced and according to the formulation of the open-loop gain for a CS amplifier (29), the gain of the input stage increases to 13. Obviously, the other gain stages are needed to enhance the internal gain of the preamplifier.

$$A_v = g_m\left(\frac{1}{g_{ds}} \,||\, R_D\right). \tag{29}$$

In order to increase the voltage gain of the preamplifier, two more stages are employed. The designs of the 2nd and 3rd stages are similar except that the 3rd stage has a buffer at its end. The source follower stage, which works as a buffer, is used to drive the input of the postamplifier and to set the output DC voltage of the preamplifier. Figure 17 shows the schematic of the preamplifier 3rd stage with the buffer output (see preamplifier 2nd stage in Appendix 1).

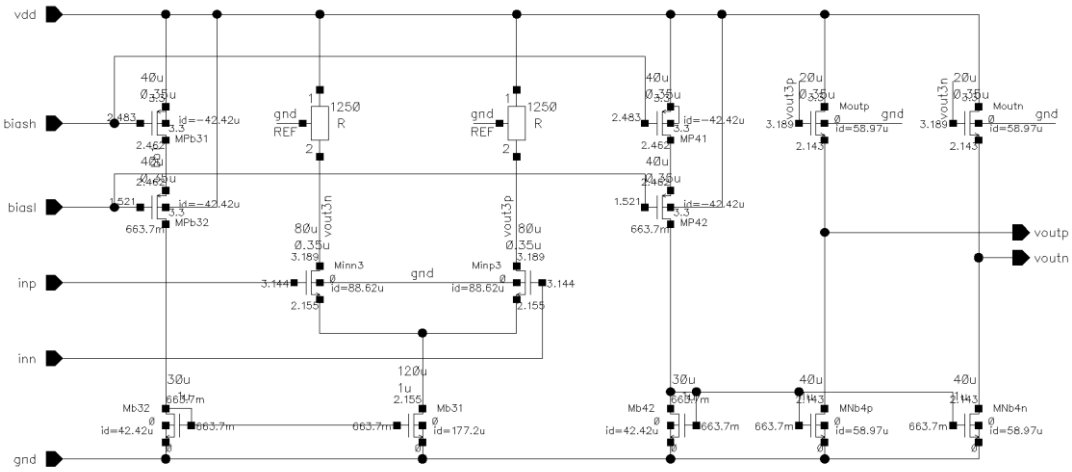

Figure 17. Third stage of the preamplifier.

The total gain of the preamplifier is given by

$$A = A_{v1} * A_{v2} * A_{v3}, \tag{30}$$

where A_{v1}, A_{v2} and A_{v3} are the voltage gains of the 1st, 2nd and 3rd stage of the preamplifier and are equal to 13, 6 and 5. Thus, the total voltage gain is about 390. Figure 18 shows the closed-loop gain of preamplifier. The V(dB) represents the closed loop magnitude frequency response of the preamplifier and M2 is the -3dB bandwidth frequency.

The internal voltage gain should be high enough to minimize the internal gain error signal e_0/A_v and to push the bandwidth limit to higher frequency (see section 2.3). The gain of the transimpedance amplifier is defined by the feedback resistor, which is $2*R_f$ in the differential case. The feedback resistor is in this design 270kΩ, so the transimpedance gain of the TIA is 540kΩ.

Knowing the gain, the bandwidth of the preamplifier can in principle be calculated, but in practice the bandwidth calculation of a three-stage feedback TIA is complicated. So, the bandwidth is simulated with a circuit simulator. The preamplifier bandwidth interacts with some factors including stability, noise and channel bandwidth. Therefore, setting the stability by adding feedback capacitance or decreasing the noise by adding extra capacitance, changes the bandwidth.

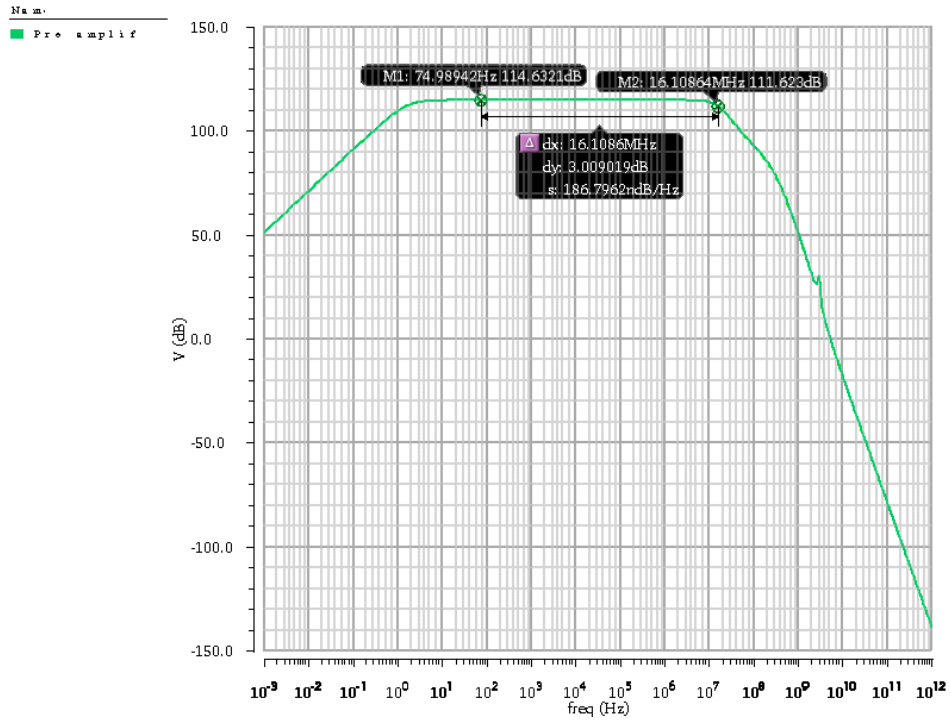

Figure 18. Closed loop magnitude response of preamplifier.

In the low-noise receiver of this design work, the bandwidth is not limited in the receiver channel because the digital circuitry facilitates a digital filter which sets the final bandwidth. Hence, it is enough that the bandwidth of the preamplifier, and accordingly the bandwidth of the whole channel, is high enough, whereas the priorities are the maximum stability and minimum noise.

The stability, as well as the bandwidth, are designed and verified using the circuit simulator. With a careful design, the circuit will stay stable in all circumstances. To investigate the stability, corner simulations are run in extreme temperatures and process corners. Then, Monte Carlo simulations (200 runs) in different temperatures are run to check the stability.

The stability can be checked by means of other techniques, such as transient simulation, where the circuit is excited with a fast spike. In a stable amplifier the ringing made by a fast spike damps fast, however, an unstable amplifier oscillates forever. The drawback of this approach is that like every transient analysis, it is time consuming. Nonetheless the visual aspect of transient analysis is an advantage.

As stated before, the stability trades off with the noise optimization. It means that improving the stability increases the noise and decreasing the noise of the system increases the risk of instability. For this reason, during the noise optimization the stability is always taken into account.

In the noise simulation of the preamplifier of Figure 15, the output noise is taken from voutp and voutn, the positive and negative output respectively, while the input is excited by a white noise current source model. The model of the input circuit which is used in noise simulation is shown in Figure 19, where inp and inn are the negative and positive inputs of the preamplifier. The full test bench is shown in Appendix 4.

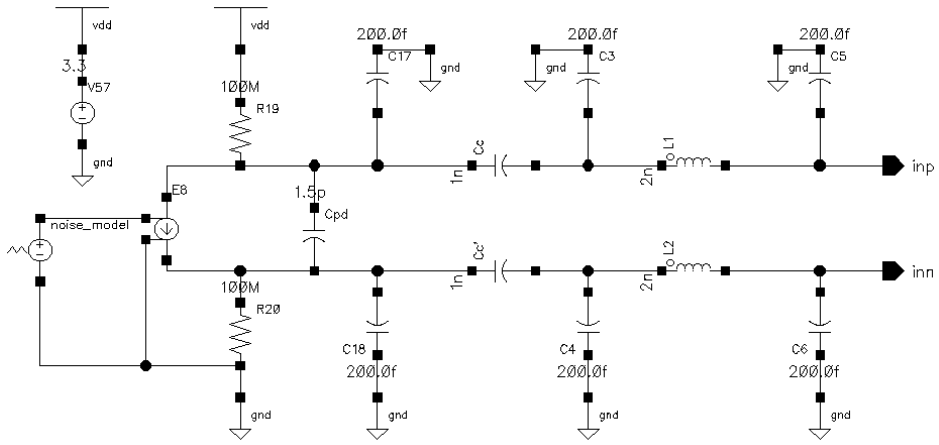

Figure 19. Model of the input for the noise simulation test bench.

The noise of the preamplifier output is shown in Figure 20. The noise is almost constant except at around the frequency of 16.5MHz in which a small peak occurs. A closer look to the output noise graph and its comparison with the AC response reveals that the peak happens in the upper cutoff frequency of the TIA. Considering the noise point of view, the TIA is working like a pass-band filter. The low frequency noise is filtered in the AC coupling in the input and by the offset compensation circuit, and the high pass noise by the poles of the preamplifier and postamplifier. This new view emphasizes the importance of the pole locations which is a challenge in the noise optimization.

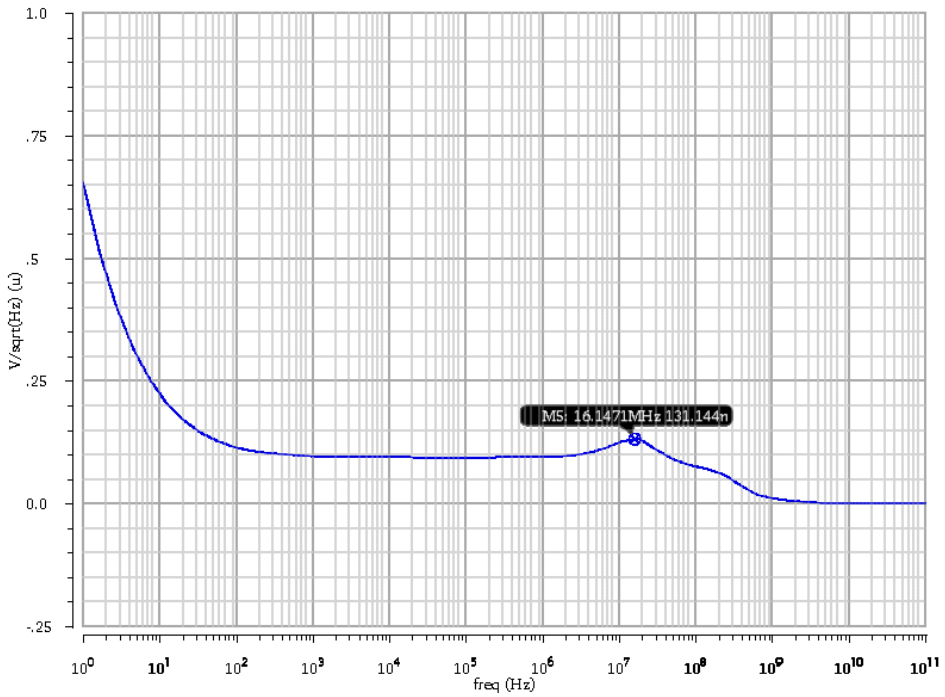

Figure 20. Output noise of the preamplifier.

The noise performance is partly optimized by adding extra poles in the preamplifier using extra capacitances. These poles help the circuit to filter out the high-frequency noise. Capacitances C1 and C2 (see Figure 15) are employed between the 2nd and 3rd stage of the preamplifier. The capacitor is divided into two parts in order to have symmetric load to the ground. Figure 21 illustrates the difference of the output noise with and without the extra capacitances.

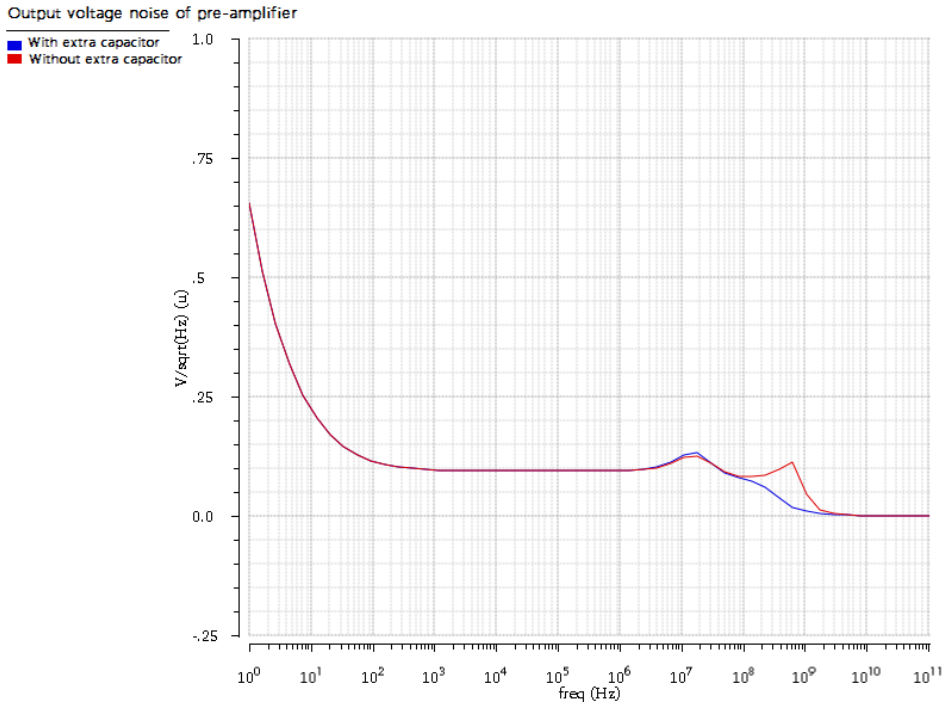

Figure 21. Output noise of the preamplifier with and without the extra capacitances.

Figure 22 shows the closed loop magnitude response of the preamplifier with and without extra capacitances. Akin to Figure 21, the effect of the extra poles, i.e. having extra capacitances, is more visible in the voltage gain of the TIA. Figure 22 reveals that the TIA without the extra capacitances has slower slope in the high-frequencies. Such a characteristic allows more noise passing through the TIA. The extra capacitances in the preamplifier cut out-of-band noise.

Eventually, the input-referred rms noise current provides the numerical proof for the noise optimization. By adding the capacitors, the preamplifier rms noise is decreased from 4.3nA to 2.6nA, which is a significant improvement. It is also good to note that the capacitances at the output of the 2nd stage add a pole in the high frequency which does not affect the bandwidth. Thus, the values for the input-referred rms noise current provide comparable data for both with and without extra capacitances situations.

Further noise optimization is investigated by increasing the value of the capacitive load and adding other capacitances at the output of the 1st stage but none of them enhance the SNR. The problem with larger capacitive load is that it decreases the phase margin and stability. Besides increasing the risk of instability, adding another capacitive load stage is also limiting the bandwidth of the whole channel. As a result, 2×500 fF capacitance at the output of the 2nd stage is the optimized way for filtering out high-frequency noise.

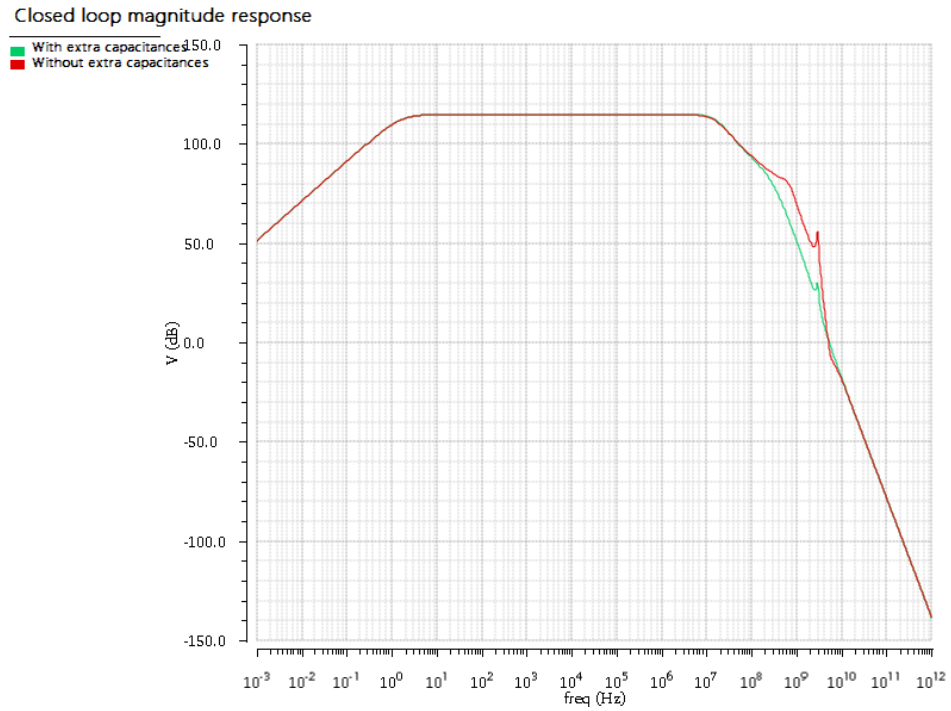

Figure 22. AC response of preamplifier with and without the extra capacitances.

4.3. Postamplifier

The post amplifier is shown in Figure 23. The signal is amplified with the two voltage amplifiers, PostAmp_L1 and PostAmp_L2, while the Offset Cancellation block, a g_m-c filter, reduces the voltage offset between the positive and negative output of the postamplifier (voutp and voutn).

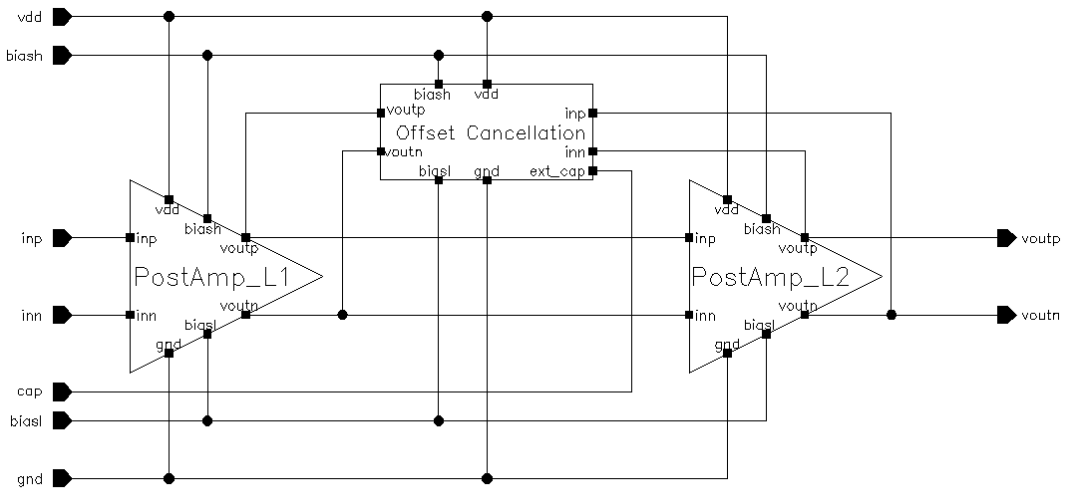

Figure 23. Postamplifier block diagram.

The amplifier stages of the post amplifier are typical wideband voltage amplifiers shown in Figure 24, and the gain is defined by resistor ratio given by

$$A_v = \frac{2R_D}{R_S + \frac{2}{g_m}}. \tag{31}$$

The second gain stage is using the same approach with different gain values and a common drain stage at the output (see Appendix 2). The post amplifier is employed to enhance the signal for the comparator. Therefore the gain of the postamplifier needs to be high enough that comparator can reliably detect the signal.

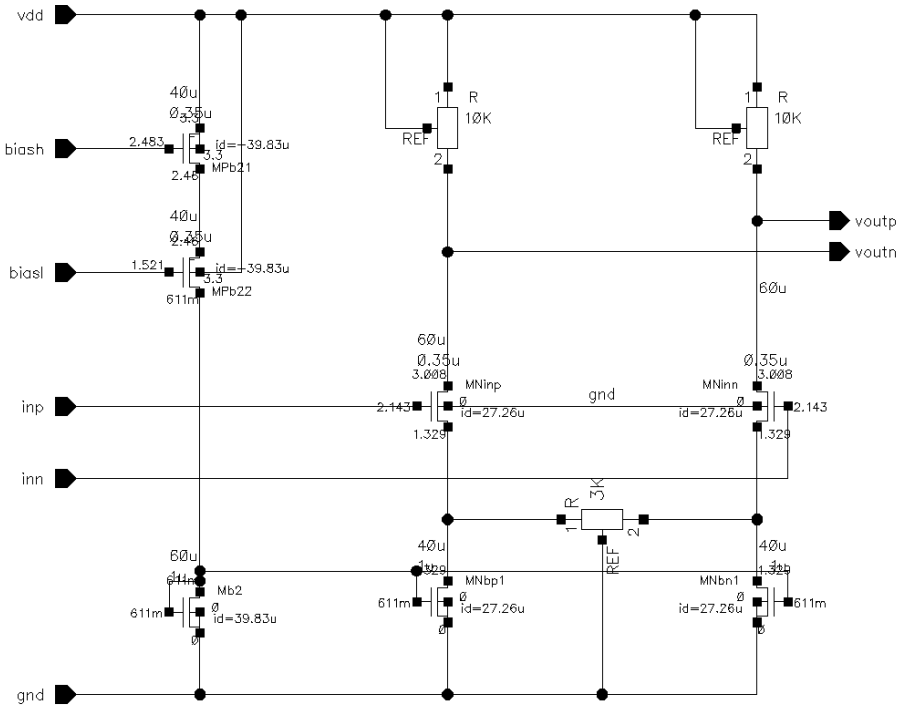

Figure 24. Postamplifier, gain stage L1.

The voltage gains of the postamplifier stages are shown in Figure 25 where the green, red and blue colors mark the input, the output of the 1st stage and the output of the postamplifier. The graphs shows that as the gain is increased along the channels, the bandwidth is decreased. The postamplifier filters the peak of the noise of the preamplifier output by adding high frequency poles.

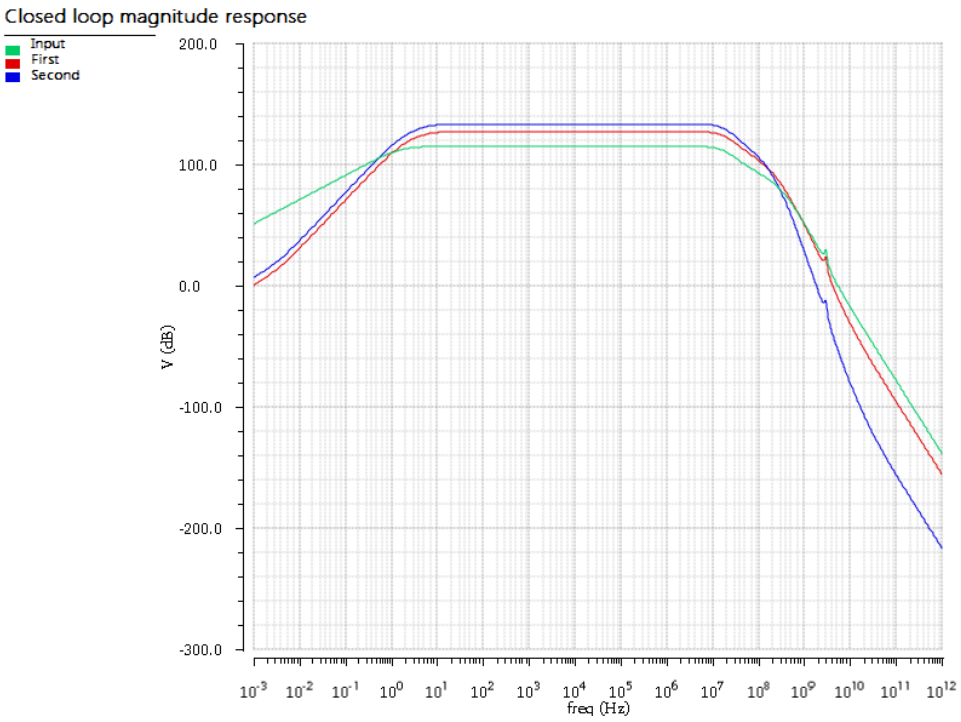

Figure 25. Closed loop magnitude response of postamplifier stages.

Offset cancellation circuit is added to the postamplifier to minimize the offset created by mismatches in e.g. the input transistors and feedback resistors of the preamplifier. The risk of amplifying the offset voltage along with the original signal is that the offset can easily destroy the linearity of the circuit.

The offset cancellation system (see Figure 26) takes the postamplifier output voltage to a Gm block, which integrates an error voltage at its output. This voltage drives a differential pair which sinks current from the postamplifier input stage for positive offset or sources current to the postamplifier input stage for negative offset to compensate for the voltage difference and correspondingly decreases the offset.

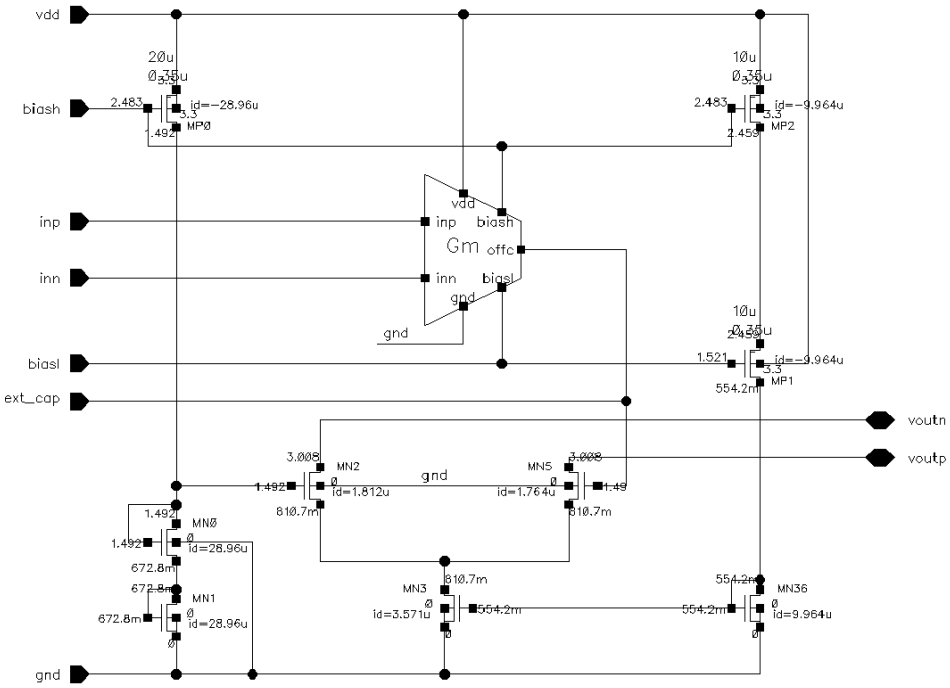

Figure 26. Offset-cancellation circuit.

The Gm block, which is a transconductor shown in Figure 28, and an external capacitor work as a g_m-C integrator as shown in Figure 27. The open drain amplifier (differential pair composed of MN2 and MN6, and biased with current mirror composed of MN3 and MN36) is a single-ended to differential amplifier which is driven by the integrator output (ext_cap) from one side and a fixed bias voltage from the other side.

The advantage of an integrator over an RC filter is that the DC gain of an integrator is quite high (infinity in ideal case) which decreases the voltage error.

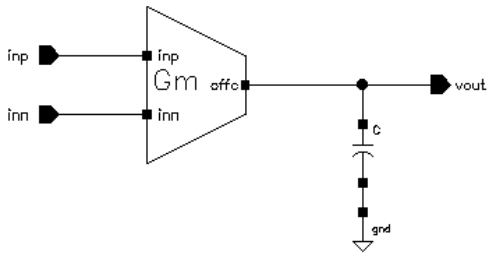

Figure 27. An example of an integrator in G_m-C technology.

One of the most important features of the g_m-C integrator is the relation of the output current and input voltage as given by

$$i_{out} = G_m V(inp - inn) \tag{32}$$

where G_m is the transconductance, inp is the positive input voltage and inn is the negative input voltage of the g_m-C integrator. In addition, another important factor of the filter is the unity-gain frequency which is given by

$$\omega_T = \frac{G_m}{C} \tag{33}$$

where C is the capacitive load of the g_m-C integrator and is in this work chosen to be a 1µF external capacitor. The benefit of an external capacitance over the internal one is the ability of tuning it after fabrication. The designed Gm cell is shown in Figure 28.

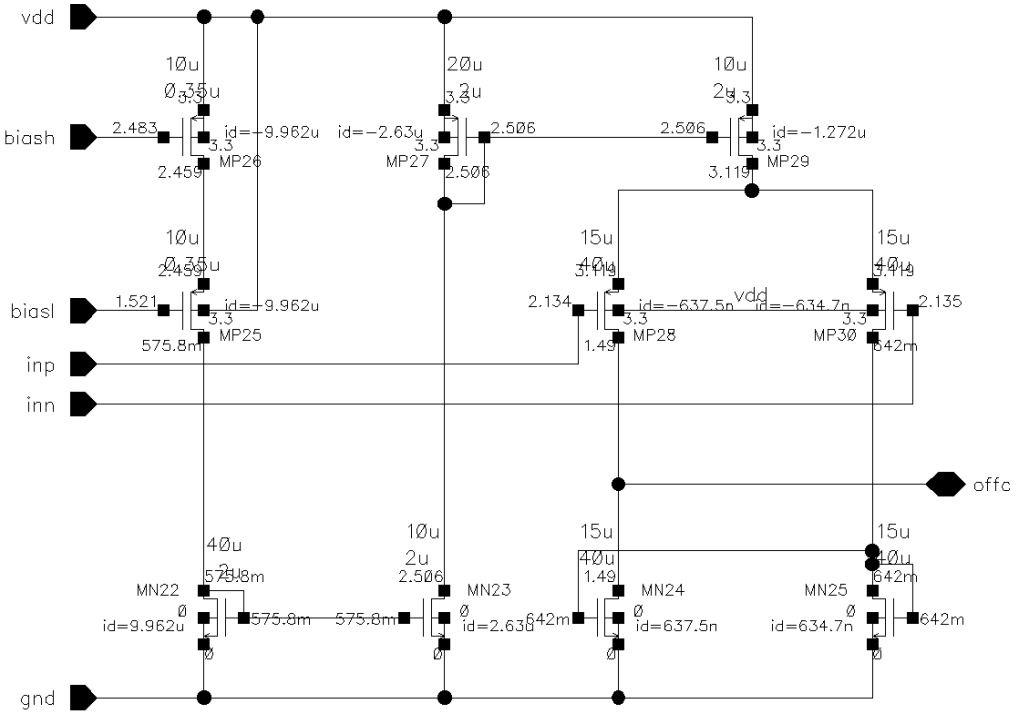

Figure 28. Differential to single-ended transconductor (G_m cell).

4.4. Comparator

Theoretically, a comparator is a device that compares the magnitude of two currents or voltages by means of a high-gain differential amplifier chain and produces a clear indication as e.g. a logic level signal. For example, a standard open-loop op-amp is a low-performance comparator. Comparators are commonly used in analog-to-digital interfaces so that the output of the analog part is converted to value which can easily be handled with digital circuitry.

Figure 29 represents the comparator of this design which consists of five differential amplifier stages and a latch. Any comparator design has two fundamental concerns, the gain and the speed. In order to reach high enough speed, every amplifier stage should be wideband. Then several amplifier stages are needed to amplify the input signal to saturation level and finally the latch stage saturates the output to the supply rails (vdd and gnd) by means of positive feedback.

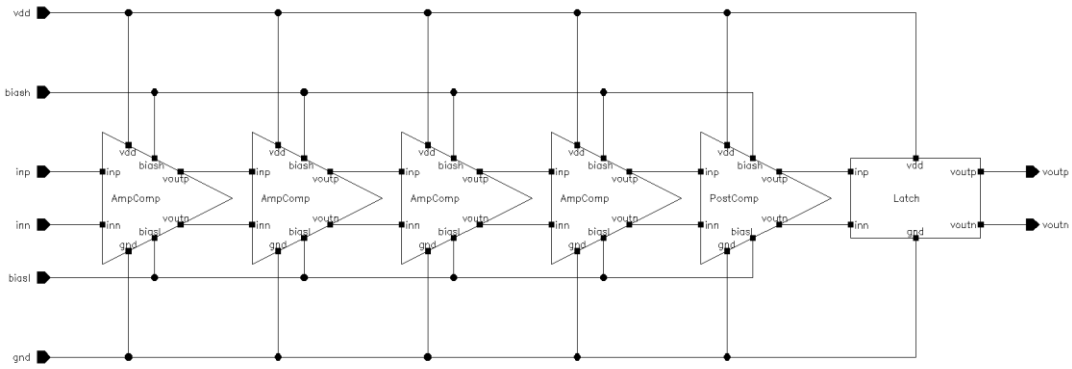

Figure 29. Comparator block diagram.

To implement an amplifier chain with those qualifications, four similar voltage amplifier stages (AmpComp) are designed with the same structure as the 2nd stage of the postamplifier (see Appendix 3). The gain of each stage is 3.3 and the bandwidth is high enough so that it doesn't limit the channel bandwidth. The voltage gain of each stage is presented in Figure 30 where the lower graph is the input and the higher one is the output of amplifier chain respectively.

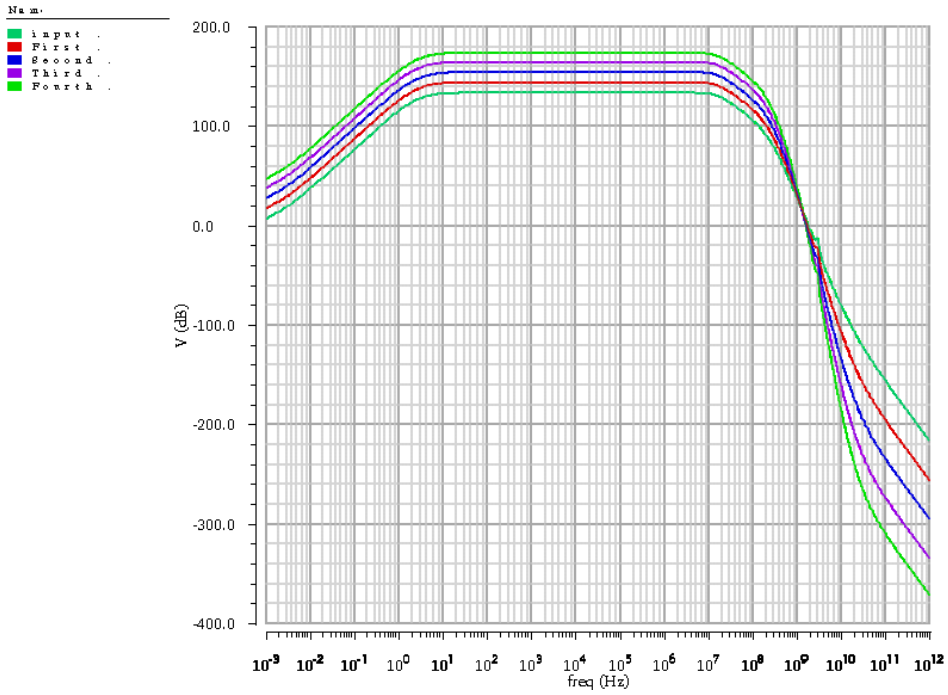

Figure 30. Closed loop magnitude response of the comparator amplifiers (Comp_Amp).

The combination of a unique amplifier stage (PostComp) and a latch is employed to form a square shape pulse which is able to drive the digital circuit. The last amplifier is designed differently because it must drive the latch stage.

As Figure 31 shows, the last amplifier stage is equipped by PMOS transistors which drive current to the output. In addition, NMOS transistors work as pulsed

current sources to enhance the switching from 0 to 1. The NMOS transistors work as DC current sources at low frequencies, but for pulsed input signals the NMOSses work as signal dependent drivers. This is arranged by DC biasing the gates through big resistances and feeding the signal to the gates capacitively.

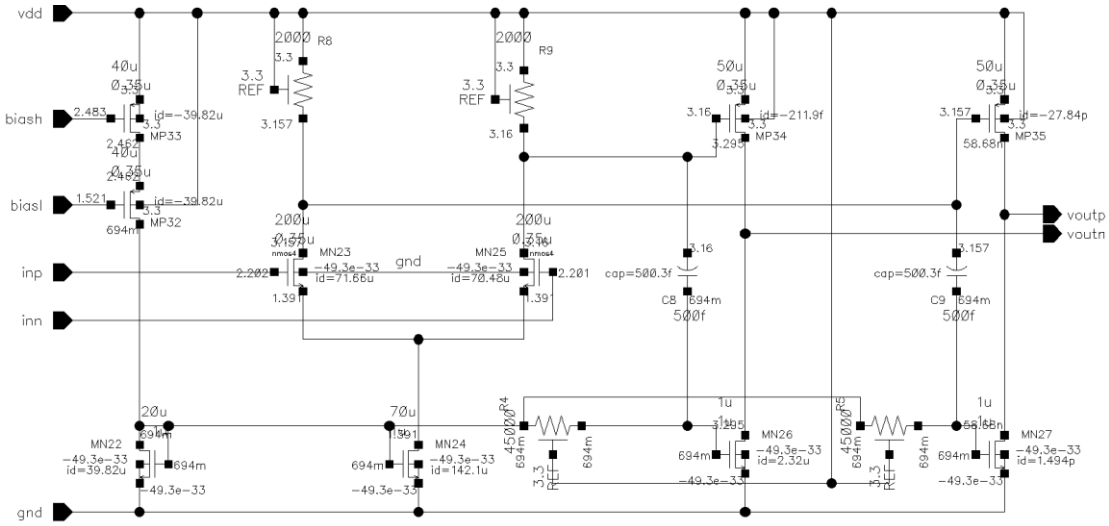

Figure 31. Last amplifier stage of the comparator (PostComp).

The last stage of the comparator is a latch which is composed of two inverters which are cross-connected to each other. The transistors need to be small enough so that the previous stage can drive them but strong enough to drive all the output load. As the latch is a digital non-linear block its functionality is most readily analyzed by transient analysis.

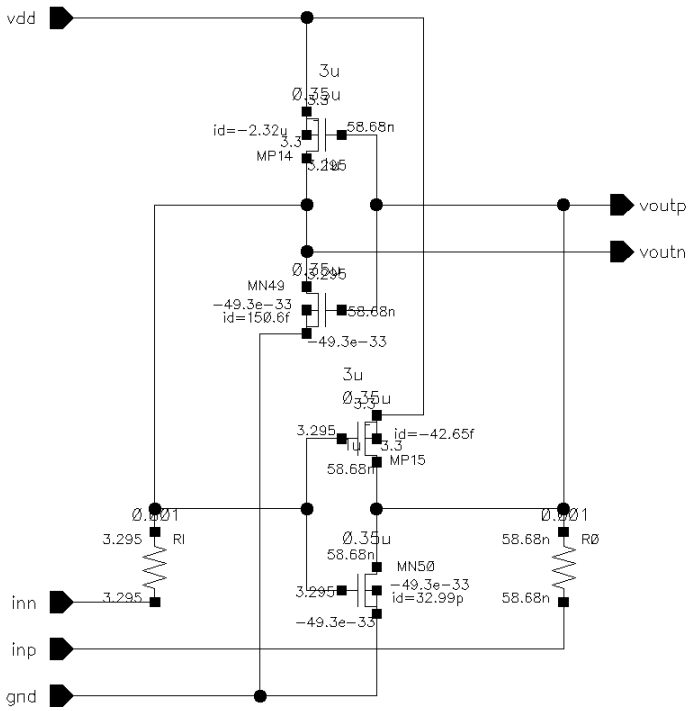

Figure 32. Latch stage.

The comparator, which is a limiting amplifier here, is responsible to boost the signal level and swing from the output of the postamplifier stage. At the end of the postamplifier the signal level is around few tens of millivolts while the logic needs a signal level in the order of e.g. 500mV. Therefore, the amplifier stages in the comparator block enhance the output voltage so that it is saturated. Figure 33 shows the transient response of each stage. The first amplifier stage has a smooth response while the last amplifier stage has the sharpest slope. The digital square shape pulse which is 0-3.3V is the latch transient response.

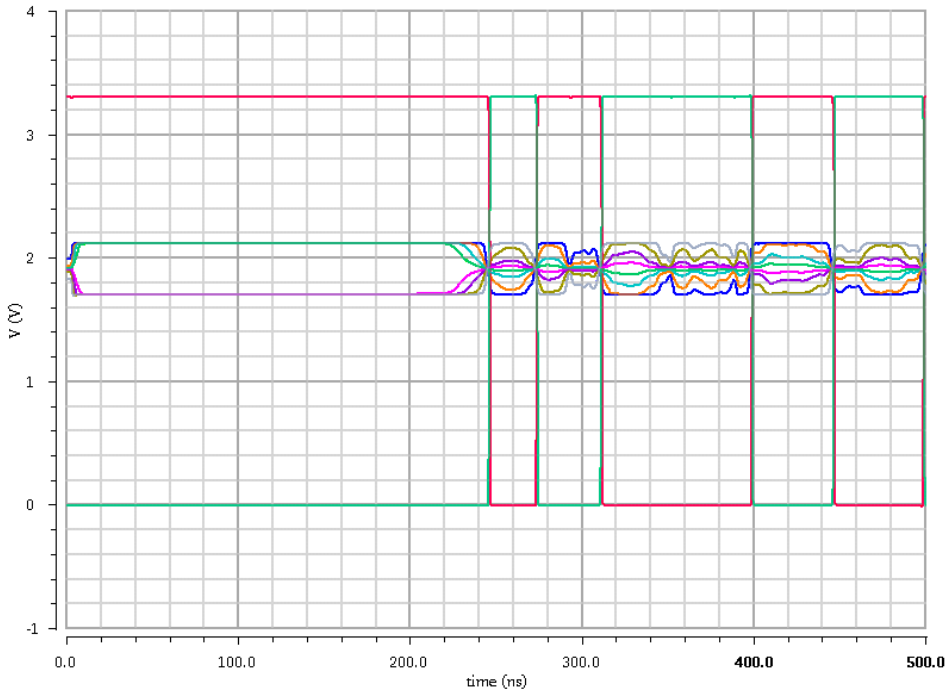

Figure 33. Transient response of the comparator stages.

4.5. Buffer

The objective of the buffer cell is to enable measuring and testing the noise, bandwidth and offset of the signal in the input of the comparator. Figure 34 shows the designed buffer. The buffer works only if the enable buffer input is active. The buffer stage is designed to be fast, wideband and linear enough so that it doesn't distort the amplifier channel output.

The measuring system is considered to have capacitive load in the order of 10pF (see Appendix 4). The buffer gain is a bit less than one and its bandwidth is 62MHz which is not limiting the receiver channel bandwidth. The output linear range is about $1V_{p\text{-}p}$ while the maximum noise is less than 50mV.

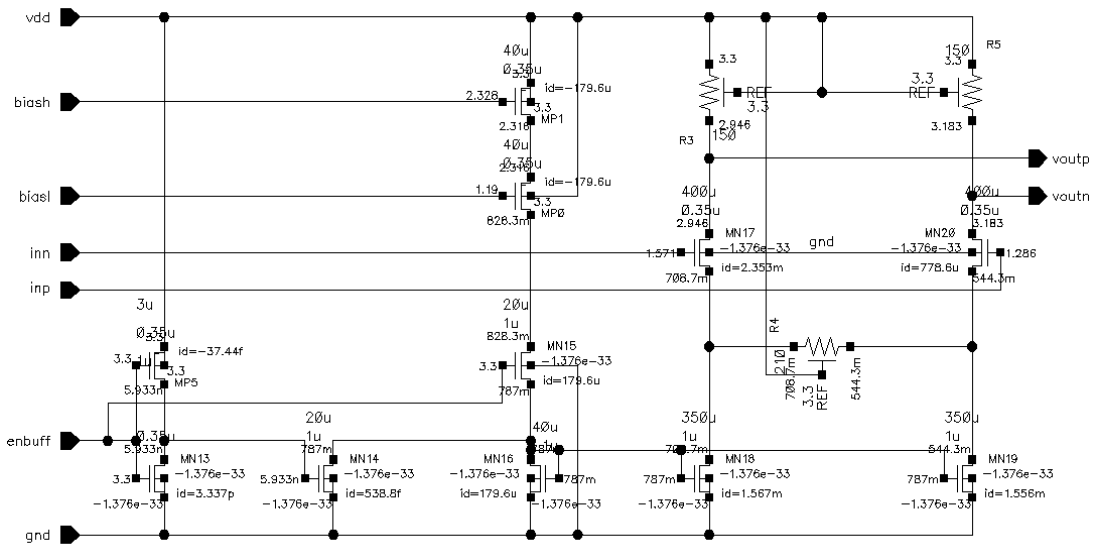

Figure 34. Buffer schematic.

4.6. Biasing scheme

Analog circuits require current and voltage references. The references define the dependency of the operating point and circuit performance on the supply voltage, process parameters and temperature. For example, in a differential pair, the bias current affects the voltage gain and noise. To produce reference current or voltage, reference generators are designed with different techniques such as supply-independent, temperature-independent and constant-gm.

In general, the main idea of the reference generators is to produce a voltage or current which is independent from the supply voltage and has the desired dependency on the process parameters and temperature. In this specific receiver, a constant-Gm reference generator has used so that the bandwidth is stailized in different working temperatures or process corners.

In a MOS differential pair, the transconductance (g_m) has a strong inverse variation with temperature. Nonetheless the g_m is determining some performance parameters such as noise, voltage gain and speed which raise the need of a constant-g_m reference generator. The circuit for constant-gm biases a transistor so that it has a temperature-independent g_m [16]. Then with a proper matched current mirror, the current of this transistor is transferred to the bias transistor of the differential pair. Eventually the g_m of the differential pair is also stabilized (see Figure 35).

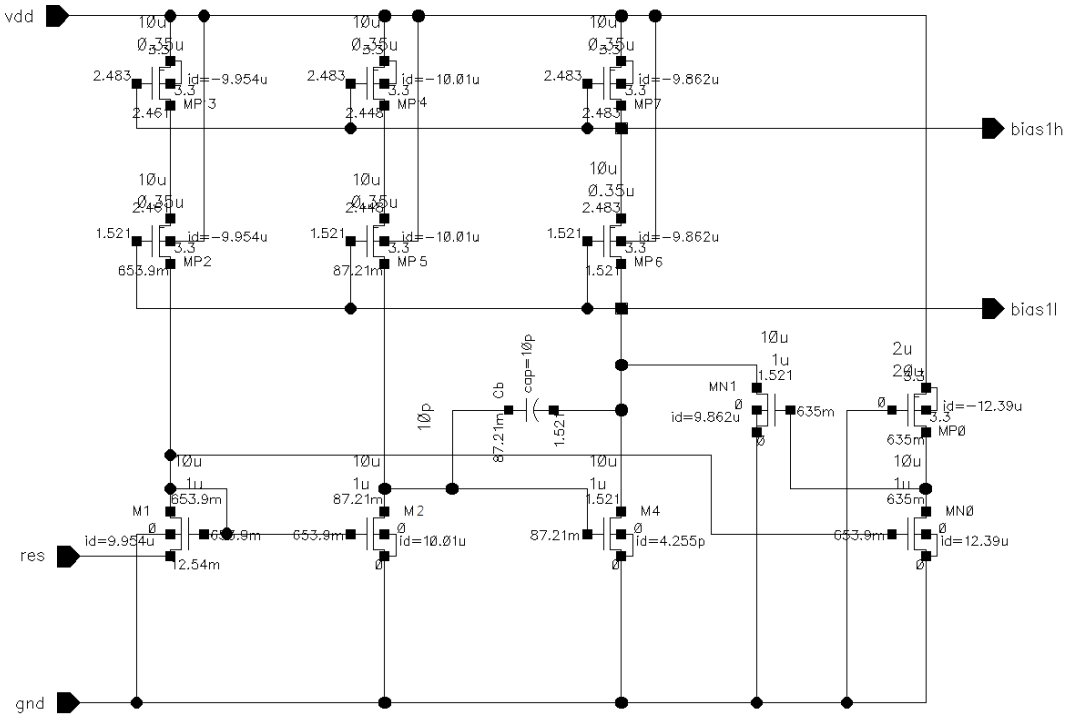

Figure 35. Constant-Gm generator circuit.

In the constant–G_m generator circuit of Figure 35, the transconductance of transistor M2 is stabilized by means of an external resistor which is connected to pin "res". If the size of the resistor is considered to be R_1, transistors M1 and M2 have equal drain current, and

$$\frac{W_1 L_2}{W_2 L_1} = N \tag{34}$$

then

$$g_{m2} = \frac{\sqrt{2}(1 - \sqrt{1/N})}{R_1} \tag{35}$$

The circuit requires a startup circuitry to ensure proper and reliable operation. The group of three transistors, MN0, MN1 and MP0 are working in the very first moment of the start to force the circuit to exit the zero current state, and with proper sizing of the devices the startup circuitry turns off right after the startup.

Also, stability must be ensured because this reference generator contains both positive and negative feedback. To that end, capacitor C_b is used as the compensation capacitor.

To improve the accuracy of the mirror currents cascade PMOS mirrors have been used, and thus two bias voltages (biash and biasl) have been used in every single design block.

5. SYSTEM LEVEL PERFORMANCE

To demonstrate the system level performance of the proposed receiver, the critical parameters, such as noise, bandwidth and phase margin are simulated for each design block and in different temperatures and process corners. Moreover, Monte Carlo simulations verify the operation taking into account mismatches.

5.1. Bandwidth and phase margin of the channel

The bandwidth is accessible directly from the simulator, while simulating the preamplifier phase margin requires a specific test bench where an element so called diffstbprob is used to cut the connection between the feedback resistors and the preamplifier output. The preamplifier is excited by a differential AC current source and the phase margin is read at the output of the diffstbprob (see Appendix 5).

Table 2 illustrates the bandwidth and phase margin of the channel after each block in three different process corners, i.e. typical corner in +27 ºC, worst case and best case.

Table 2. Bandwidth and phase margin after each designed block

Design cell	Bandwidth			Phase margin		
	Typical corner (MHz)	Best case (MHz)	Worst case (MHz)	Typical corner (degree)	Best case (degree)	Worst case (degree)
preamplifier	16.1	17.4	10.6	112.2	112.2	82.8
postamplifier	15.7	17.1	10.3	NA[1]	NA	NA
buffer	15.1	16.3	10.2	NA	NA	NA

[1)] NA stands for Not Applicable, as the phase margin is not relevant for non-feedback circuit.

As table above illustrates, in this design the bandwidth of the signal is limited after each design block. However, the inevitable bandwidth limitation is very small because the bandwidths of the postamplifier and buffer are large. Furthermore, the result shows that the bandwidth after the postamplifier is over 10MHz for each and every process and temperature corner, which is sufficient for the digital filtering. In addition to the bandwidth, the phase margin as an indication of stability shows a reliable margin so that even the internal feedback, such as the offset-cancellation, can't make the system unstable. After stability, the most important factor in designing a low-noise amplifier channel is its noise.

5.2. Noise of the channel

The noise simulation is done by using of a white noise source model at the input of the receiver channel (see Figure 19). The input rms current of the noise is set to 20 nA to represent the real circumstances. The voltage noise and input referred rms noise current are shown in Table 3.

Table 3. Noise summary

Design cell	Voltage noise (mV)			Input referred rms noise current (nA)		
	Typical corner	Best case	Worst case	Typical corner	Best case	Worst case
preamplifier	--	--	--	2.77	1.81	4.93
postamplifier	7.84	1.05	4.60	--	--	--

Furthermore, the effect of the bandwidth as well as the stability is observable on both the noise voltage and input referred current noise, i.e. wherever the bandwidth is lower the noise is smaller.

5.3. Delay variation of the channel

The delay stability of the channel is an important factor for range finding application as any variation is directly seen in the measured distance. The result of the transient simulation in Table 4 shows the delay variation in the amplifier channel (preamplifier and postamplifier), and reveals that the delay of each block increases with pulse amplitude, which is typical for linear amplifiers.

Table 4. Delay of the design blocks

Signal amplitude (nA)	Delay (ns)	
	Preamplifier	Postamplifier
5	0.95	3.10
10	1	3.30
20	1.30	3.24
30	1.93	3.24
40	2.47	3.27
50	2.84	3.41

The delay variation of the comparator is visible in the Figure 36, where each graph represents the delay versus amplitude of the comparator for a specific offset value. It can be seen that the delay is shortest for high signal amplitudes, which is quite typical for nonlinear comparators.

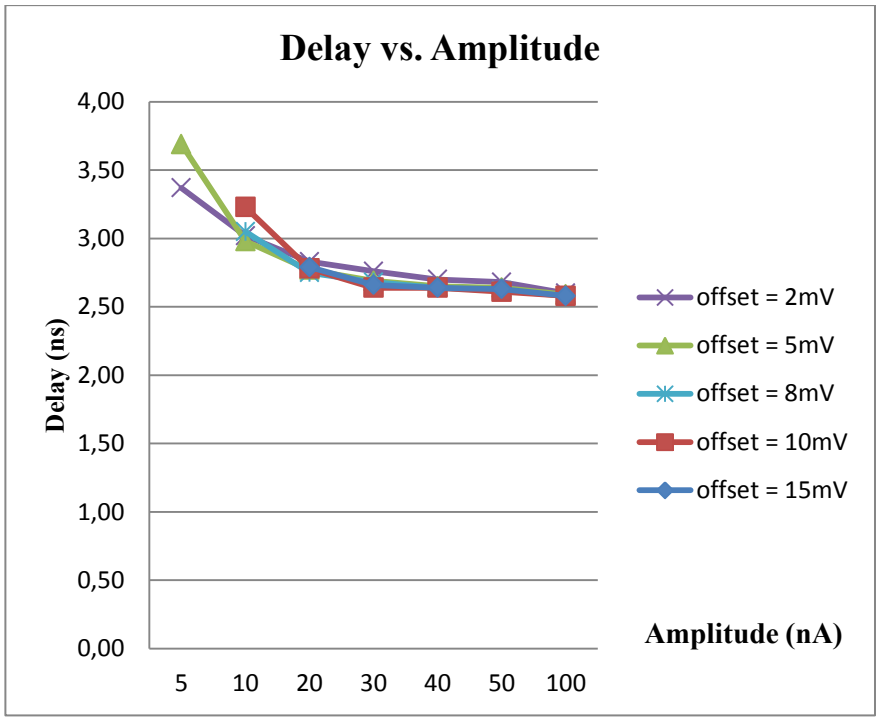

Figure 36. Comparator delay vs. signal amplitude for different offset value

The total delay variation for the receiver channel from the input of the preamplifier to the output of the comparator for signal amplitude variation from 5nA to 100nA is around 2ns, which corresponds to 303mm in distance measurement result. This sets one limit to the achievable distance measurement accuracy.

5.4. Monte Carlo simulation

Monte Carlo (MC) simulations are used to check how the circuit behaves when mismatches are taken into account. The silicon foundry provides simulation models containing the mismatch data for each component type, i.e. the type of the distribution and the corresponding parameters, and the simulator varies randomly the device parameters accordingly.

To get some insight on the behavior of the receiver taking into account mismatches 200 runs are applied for typical corner in minimum, normal and maximum temperatures which are -30, 27 and 60 degrees centigrade. The result is gathered in Table 5.

Table 5. Monte Carlo simulation result over typical corner

Name	Bandwidth (MHz)		
	Min	Max	Mean
Preamplifier	14.9	16.65	15.89
Postamplifier	14.41	16.14	15.39
Buffer	13.97	15.45	14.81

5.5. Power consumption

The input stage of the preamplifier consumes large amount of the whole receiver channel budget due to the wide transistor needed to optimize the noise performance. Also, the comparator blocks need high bias current in order to have wide bandwidth. Table 6 exhibits the current consumption of the design blocks.

Table 6. Total current consumption

Design cell	Total current consumption (mA)
Preamplifier	7.91
Postamplifier	1.64
Buffer	0.18
Comparator	6.21
Bias generators	2.17

Summing up the current consumption of all stages, the receiver channel consumes 18.11mA which is about 60mW power in a system with 3.3V power supply.

6. DISCUSSION

In this thesis work, a low-noise optoelectronics amplifier channel is designed. The channel consists of a preamplifier, postamplifier, comparator, buffer and bias generator. The design focus is on suppressing the channel noise and keeping the total bandwidth over 10MHz.

Following the study on the different preamplifier topologies a differential common-source feedback transimpedance amplifier was chosen for the preamplifier. Differential topology was chosen as it is less sensitivity to power supply and substrate noise.

The main challenge in the preamplifier design is the minimization of noise. To that end wide input transistors with high bias currents were used. Furthermore, the bandwidth and gain of the internal voltage amplifier were designed just high enough to give the desired total bandwidth with good stability.

One of the challenges in the preamplifier design is the selection of the number of stages in the internal voltage amplifier, and finding the optimal gain and bandwidth for each stage. Preamplifier with three and four internal stages was investigated. The three stage preamplifier had just enough internal gain and less noise, so it was selected. To minimize the noise bandwidth extra capacitance between the 2nd and 3rd stages was added.

The noise bandwidth is further limited by adding a feedback capacitance in parallel with the feedback resistor. Furthermore, the feedback capacitance improves the stability of the transimpedance amplifier.

The gain of the preamplifier stage alone is not enough for signal amplification, thus a differential common-source voltage amplifier is employed as postamplifier.. The bandwidth of the designed amplifier channel should be defined by the preamplifier and not limited by the following stages, and therefore the post amplifier stage is designed to be wideband enough. At the end of the postamplifier the signal is in the range of a few tens of mV, therefore it is a good point for offset-cancellation. In order to cancel the offset a trans-conductance (G_m) block is used in which a differential to single-ended slow amplifier reads the output of postamplifier and feeds back the difference to the input of the postamplifier.

Designing the comparator cell, the signal should be amplified enough to drive the latch stage, the latch. At the same time the comparator should be fast to be able to produce sharp, accurately timed logic level output signal for the following digital signal processing part. Therefore, the amplifier stages are high bandwidth common-source voltage amplifiers.

According to the simulations the proposed receiver fulfills all of the design goals, such as input-referred rms noise current, delay and bandwidth. Table 7 shoes the goals and obtained results from designed receiver.

Table 7. Design specifications

Design specification	Goal	Proposed receiver (worse case)
Input-referred rms noise current after preamplifier	<3nA	2.6nA
Minimum channel bandwidth after postamplifier	>10MHz	10.3MHz
Phase margin of preamplifier	>60degree	82.8degree
Effective transimpedance	6.5MΩ	2.8MΩ

It is not easy to compare this work with other available works because the design specifications such as technology, bandwidth, photodiode capacitor, application area are different. However, the result of some comparison is presented in the Table 8.

Table 8. Comparison of the performance of low-noise amplifiers and this work

Design	[17]	[18]	[19]	[20]	[21]	This work
Technology	1.2 µm BICMOS	0.18µm BICMOS	0.18µm BICMOS	0.18µm CMOS	0.18µm RF-CMOS	0.35µm CMOS
Power supply (V)	5	5	5	3.3	1.8	3.3
Input-referred noise (pA/√Hz)	0.9	8	6	7.2	17.5	0.8
Bandwidth (MHz)	10	4000	170	1900	7000	16
Photodiode capacitance (pF)	1	0.2	1.6	1	0.2	1.5
maximum trans-impedance (kΩ)	2700	11	260	---	---	6500
Power consumption (mW)	---	60	270	112	18.6	60

7. CONCLUSION

The objective of this thesis work is to study and find the best topologies for a low-noise optoelectronics amplifier channel for laser radar. Therefore, low SNR pulsed receivers, their requirements and basics of detecting techniques (sampling technique in here) were studied. Then the receiver channel consisting of four main blocks, i.e. the preamplifier, postamplifier, buffer and comparator was designed. A detailed study on the preamplifier stage, which is the most critical element of the design, was carried out.

To achieve the best signal to noise ratio, a common-source feedback transimpedance amplifier with three internal gain stages was opted. The noise performance of the transimpedance preamplifier was optimized by using large input transistors and carefully optimizing the pole locations of the amplifier stages to filter out high frequency noise. The signal was further amplified by employing a postamplifier stage. In the postamplifier stage the offset was cancelled and out-of-range signal was further filtered out. Finally, a fast comparator was designed to generate the logic level output signal.

The simulations indicated that designed channel fulfills the goals for the design. The amplifiers were reliably stable, the input referred rms noise current was less than 3nA and the bandwidth was in excess of 10MHz in the extreme temperatures and process corners. Moreover, a Monte Carlo simulation showed that the designed channel works even taking into account mismatches. The receiver has been designed using a 0.35µm CMOS technology in Cadence design environment with AMS kit.

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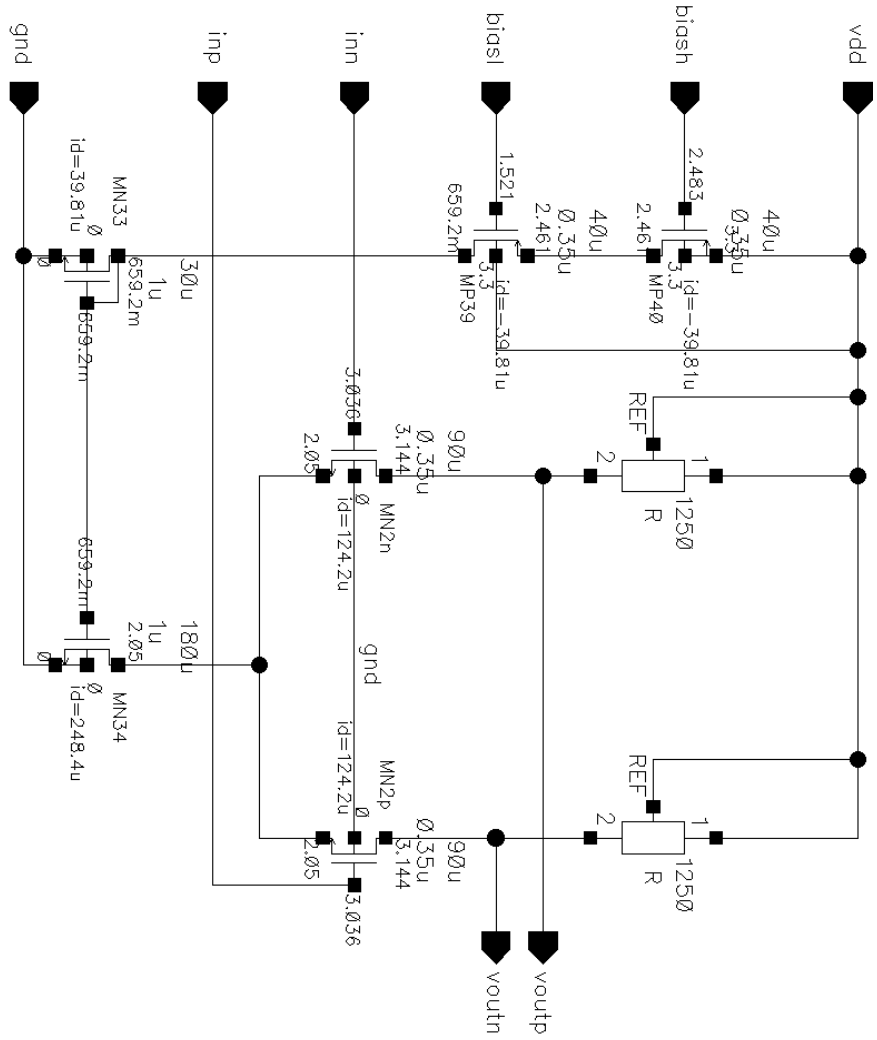
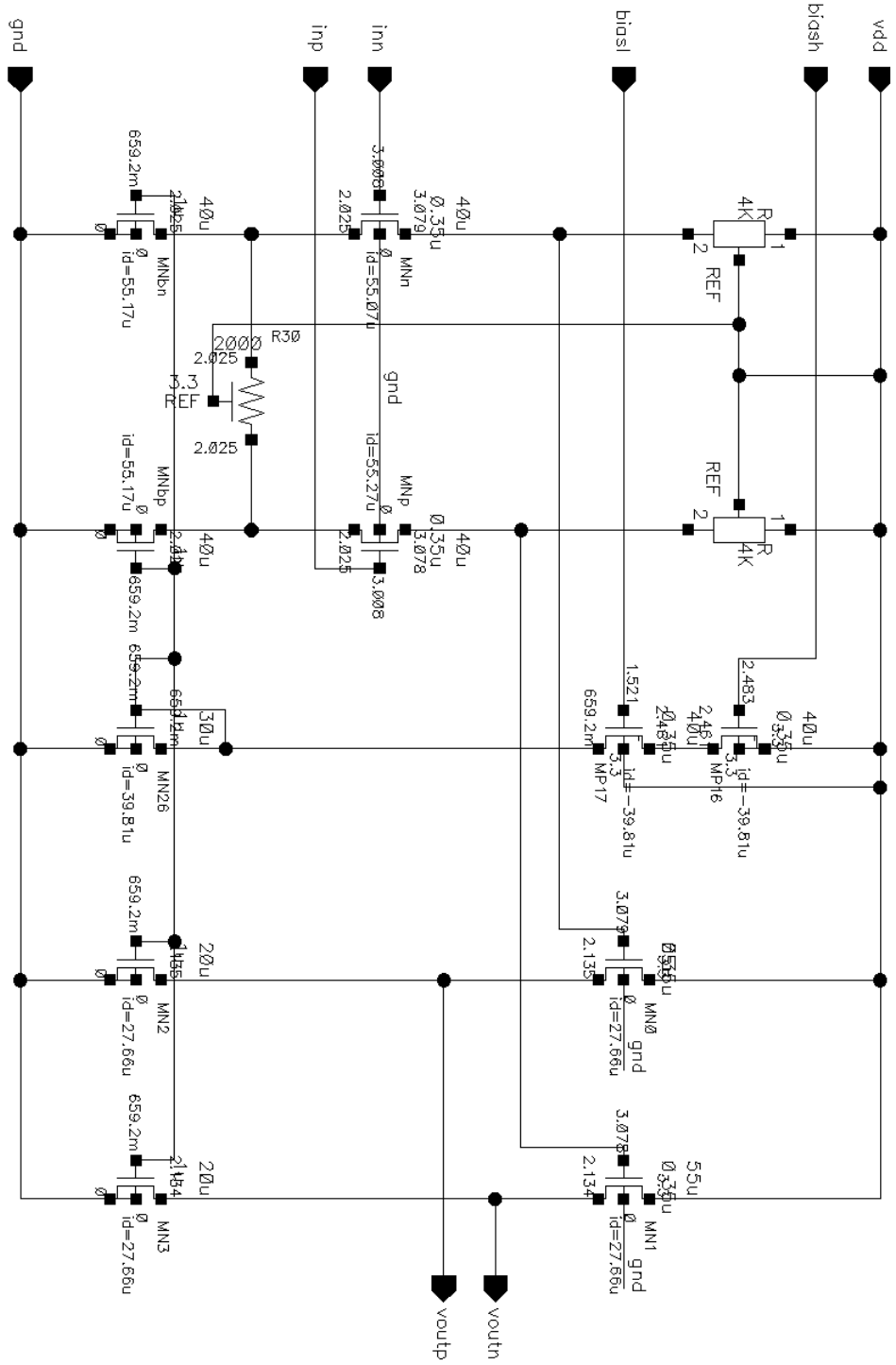
9. APPENDIX

Appendix 1. Schematic of preamplifier
Appendix 2. Schematic of postamplifier 2nd stage
Appendix 3. Schematic of comparator amplifier (Amp Comp)
Appendix 4. Schematic of simulation test bench
Appendix 5. Schematic of preamplifier phase margin simulation test bench

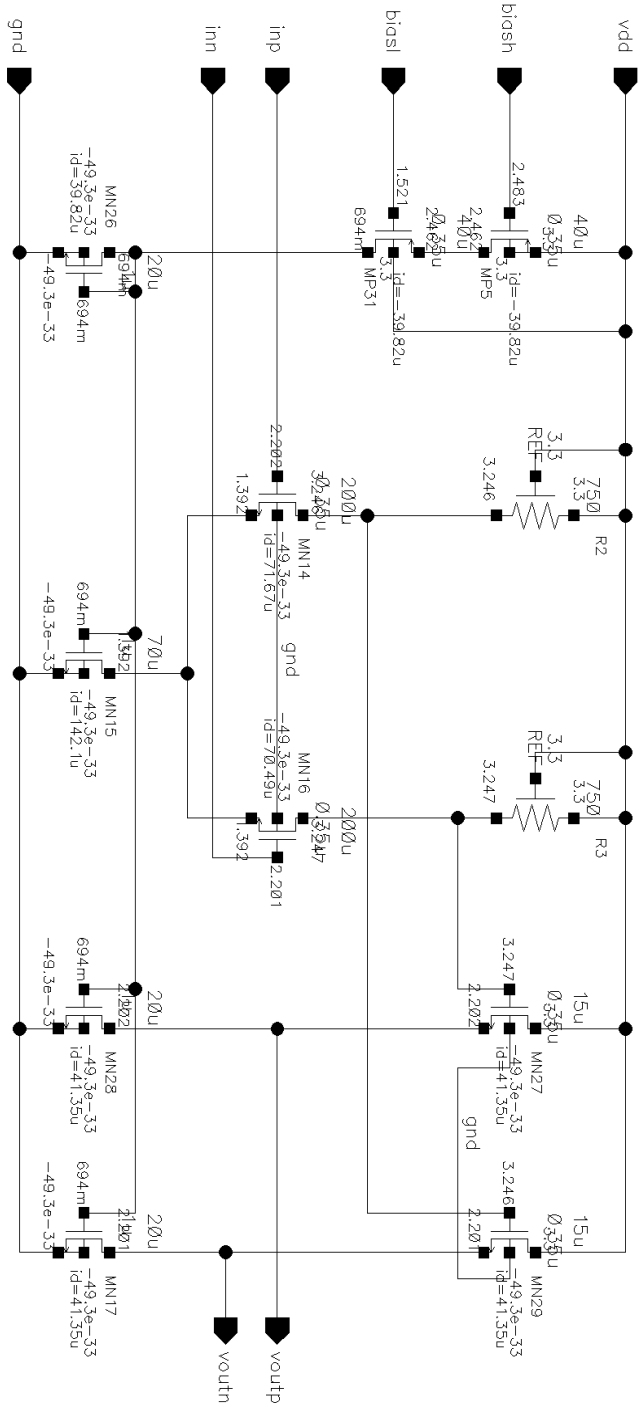
Appendix 1. Schematic of preamplifier 2nd stage



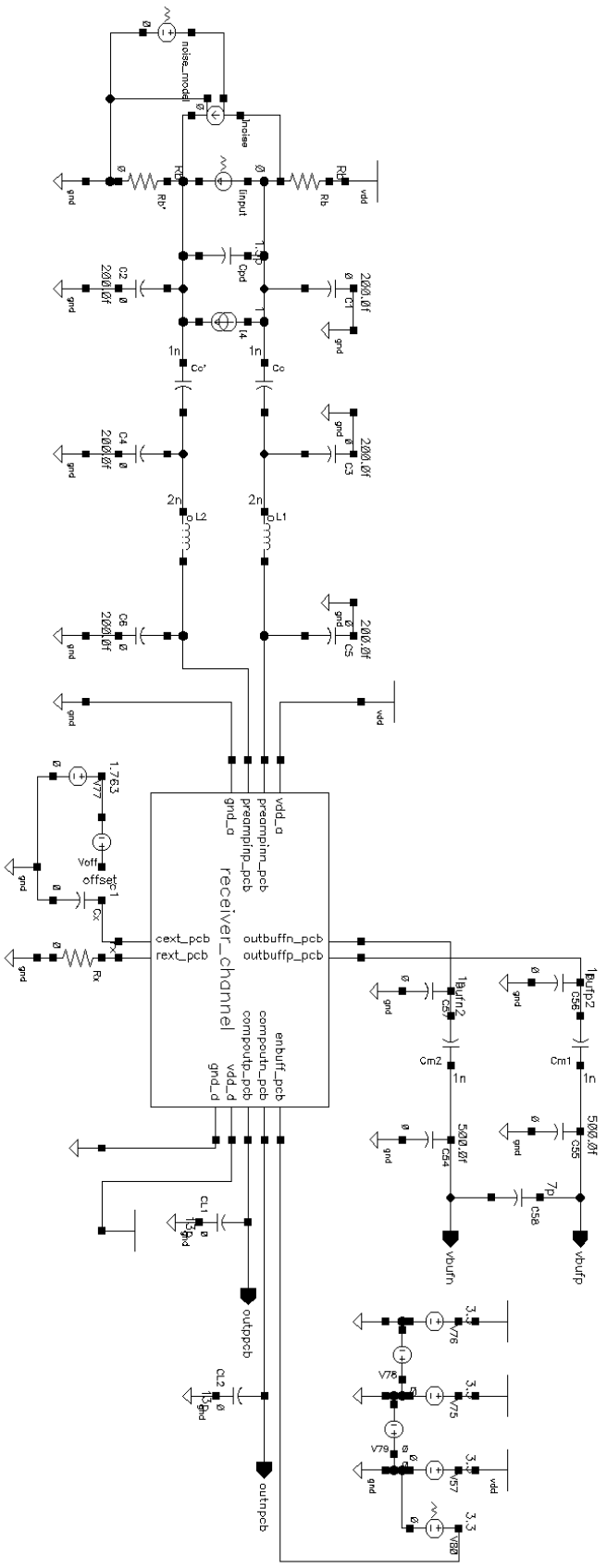
Appendix 2. Schematic of postamplifier 2nd stage



Appendix 3. Schematic of comparator amplifier (Amp Comp)



Appendix 4. Schematic of simulation test bench



Appendix 5. Schematic of preamplifier phase margin simulation test bench