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SÄHKÖTEKNIIKAN OSASTO
ELEKTRONIIKAN KOULUTUSOHJELMA

DESIGN AND VERIFICATION OF A LOGIC INPUT BUFFER

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ABSTRACT

Two low-power logic input buffer topologies are designed, simulated and compared. The most important parameters of the buffers are input threshold voltage level stability and minimal current consumption. Topologies have been implemented earlier for a wider line width process, and now the intention is to move them to a narrower line width process without losing performance. Based on the simulations, a topology with the better performance and smaller area is chosen and layout for particular topology is designed. Layout parasitics effect to the performance is also verified by simulations.

In this thesis are also discussed common buffer structures and I/O structures shielding against outside of a circuit disturbances. Finally there is a measurement plan how an input buffer functionality could be measured and verified on a chip.

Key words: input buffer, control input buffer, fixed threshold input buffer, low current input buffer

Niemelä J. S. (2013) Logiikkatasoisen tulopuskurin suunnittelu ja varmennus. Oulun yliopisto, sähkötekniikan osasto. Diplomityö, 42 s.

TIIVISTELMÄ

Työssä suunnitellaan, simuloidaan ja verrataan kahta eri topologialla toteutettua kontrollitulopuskuria, joiden tärkeimmät parametrit ovat tulon kynnystason stabiilisuus ja minimaalinen virrankulutus. Topologiat ovat aiemmin toteutettuja leveämmällä viivanleveydellä, ja ne on tarkoitus siirtää kapeamman viivanleveyden prosessiin suorituskyky säilyttäen. Simulointien perusteella valitaan suorituskyvyltään parempi ja pinta-alaltaan pienempi tulopuskuri, ja sille piirretään piirikuvio ja varmennetaan parasiittisten komponenttien vaikutus toimintaan.

Diplomityössä käsitellään myös yleisesti puskureita ja I/O-rakenteiden suojausta. Puskurit ovat yhteydessä piirin ulkopuoliseen maailmaan ja niiden täytyy kestää piirin ulkopuoliset häiriötekijät. Lopuksi esitetään mittaussuunnitelma, jolla tulopuskurin toiminta voitaisiin mitata ja varmentaa valmistetusta komponentista.

Avainsanat: tulopuskuri, kontrollitulopuskuri, kiinteän kynnysarvon tulopuskuri, pienivirtainen tulopuskuri

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FOREWORD

This master's thesis intent was to design and implement control input buffer from a wider line width process to a narrower line width process. There were two different topologies for an input buffer and the idea was to find the better in terms of performance and area. Both topologies were designed to meet given specifications and the better design was selected. Layout for the chosen topology was drawn and measurement plan is proposed.

I would like to thank Fairchild Semiconductor Finland Oy about my master's thesis position, especially design manager Panu Jalas and my design engineer colleagues Juha-Matti Kujala, Jani Kauppinen and Jouni Vuorinen helping with circuit design and Francisco Castro helping with layout design.

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Jari Niemelä

LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATION	explanation
IC	integrated circuit
MOSFET	metal oxide semiconductor field effect transistor
NMOS	n-channel metal oxide semiconductor field effect transistor
PMOS	p-channel metal oxide semiconductor field effect transistor
ESD	electrostatic discharge
PTAT	proportional to absolute temperature
I/O	input / output
SPICE	Simulation Program with Integrated Circuit Emphasis
ggNMOS	Grounded-gate NMOS
SCR	Silicon Controlled Rectifier
IP	intellectual property
ATE	Automated Test Equipment
SMU	source meter unit
AWG	arbitrary wave generator
SMPS	switched mode power supply

1. INTRODUCTION

Almost every integrated circuit product has some kind of I/O buffers inside. Especially products which have digital inputs and outputs for receiving and transmitting information and control signals have buffers. Input buffers are typically used for signal conditioning and level recognition and output buffers are used to make outgoing signals strong enough to drive external loads that typically are orders of magnitude higher than on-chip loads. From the beginning of the integrated circuits development design requirements and targets has been tightened all the time and it has set the need to develop buffers which have some special features as hysteresis and fixed trigging levels.

This master's thesis purpose is to design, implement and verify a logic input buffer for a new tighter line width process. An input buffer with this topology has been designed earlier to a 350 nm process and its functionality has been verified by simulations to meet Jedec standard JESD76 for 1.8 voltage CMOS logic devices [1]. The intention is to move this topology to the 180 nm silicon process and verify its functionality by simulations and measurements.

The most important parameter of this kind a control input buffer is recognising the input signal level and send information forward is the input signal over or under the specified triggering levels. The second important parameter in the aimed applications is current consumption. The circuit must not consume more than 500 nA shutdown current, because the usable amount of energy is very restricted on battery powered mobile products. The third important parameter is silicon area. Less area means lower price and that is very important when competing place on the market. Other parameters like propagation delay and speed are not critical in this application; it just has to be fast enough to react to control signals slower than 500 kHz and - contrary to most high-speed input buffers - filter higher frequency noise.

From application point of view the input buffer has to have robust functionality in all conditions. The main problem in the design of the input buffer is to find a topology which can handle supply voltage fluctuations, consume minimal amount of power and needs the least silicon area. The input buffer has to also tolerate a wide temperature and process variations range and it still has to be able to surely recognise an input signal level and control an output signal to other circuits inside an IC-circuit. Despite the varying of these parameters the input buffer has to be capable to operate in a narrow window where lower and upper thresholds are fixed for certain voltage levels. In all operating conditions when the input signal rises the input buffer has to set the output signal high before the input reaches the upper threshold 1.07 V and when the input signal falls the input buffer has to set the output signal low before the input reaches the lower threshold 0.68 V. In addition to these parameters the input buffer has to have enough hysteresis to avoid problems which can be caused by noisy input signals. Without hysteresis a noisy input signal could trigger the input buffer many times before the output signal settles to right state. Combining all of these functionalities in one input buffer is a challenge which is tried to be solved in this master's thesis.

The first input buffer topology is very simple which contains traditional CMOS inverters and has the resistor as pull-up at first stage to act like a current source for NMOS transistor to minimize effects of a supply voltage variation and setting input

buffer threshold voltage. It can be easily understood that this is not the most accurate way to set the threshold voltage of the input buffer but if it is designed well it will apparently fulfil the functionality of the input buffer.

There is also an other topology for an input buffer which has a current source for driving first stage of a buffer and thereby it should minimize the dependence to the supply voltage. This buffer has been simulated with the wider line width process and it seems to provide improved performance. It is also possible that the first input buffer topology cannot achieve the required threshold specifications in the narrower line width process and this cause the need to use current-biased topology for the input buffer.

2. LOGIC INPUT BUFFERS

This chapter familiarizes to the state of the art of input buffers and buffers generally. Basic requirements and topologies are presented as well as their pros and cons. The important thing regarding I/O buffers and I/O pins generally, the shielding against ESD, is also discussed and basic ESD structures are presented.

2.1. State of the art of input buffers

Semiconductor technology runs to tighter line width processes all the time and voltage levels have also decreased down to 1.2 V and even lower [2][3]. This contest is driven by integration of new functionalities to less and less area especially in mobile technology now-a-days. To integrate more functionality to same or less area has to shrunk the line width and tighter line widths tolerate less voltage and thereby supply voltage levels also decrease. This voltage reduction causes a need to design new topologies for lower voltage levels and power consumptions [4].

Many buffers are used for transferring data and one of the key requirements is to transfer signals as fast as possible. Fast signals require short delay times and noise immunity from buffer. One way to transfer fast signals is differential. Differential signal consist of two signals which levels are referred to each other and signal information is the difference between signals [5]. Differential topology has almost independent delay of supply voltage and input signal amplitudes. The output signal pulse shape is highly symmetric and this mitigates skew related errors.

An other way to transfer high speed signals is current-mode logic (CML).The advantages of the current mode logic are speed and noise immunity for crosstalk and power/ground noise. Speed advantage compared to traditional CMOS inverter is achieved due shorter propagation delay time, because basic CMOS inverter suffers from a larger threshold voltage and lower drift velocity of PMOS transistor.[6]

2.2. Basic requirements and topologies

There are almost as many topologies for buffers as there are inventors. Inventors have had some special target or specification which they have optimized their designs. Output buffers have tight specifications for driving capability and rise and fall time. Input buffers major aspects are switching level and propagation delay. Buffer can also be a combination of both input and output buffer and have some special features like fixed switching level. There is a lot of different optimizations to decide, buffer can be designed for a low voltage or an optimized accuracy or area, which is very expensive in silicon wafer. Usually a design is a combination of all these specifications and designer have to decide which is the most important property which steers the design. It is also possible that some known topology has good performance for some application but it is patented by some company and using a straight copy of the topology is illegal and violates the patent. In this case the designer has to modify the circuit topology for the particular design in order not to violating patents.

One of the simplest input buffers is shown in Figure 1. a) where two transistor are connected in series between supply voltages. The upper MOSFET is P-type which source is connected to the high supply voltage and lower MOSFET is N-type which source is connected to the low supply voltage. Transistors drains are connected together. This component consisting of two transistors in series between supply voltage is also known as CMOS inverter and it is one of the basic logic components.

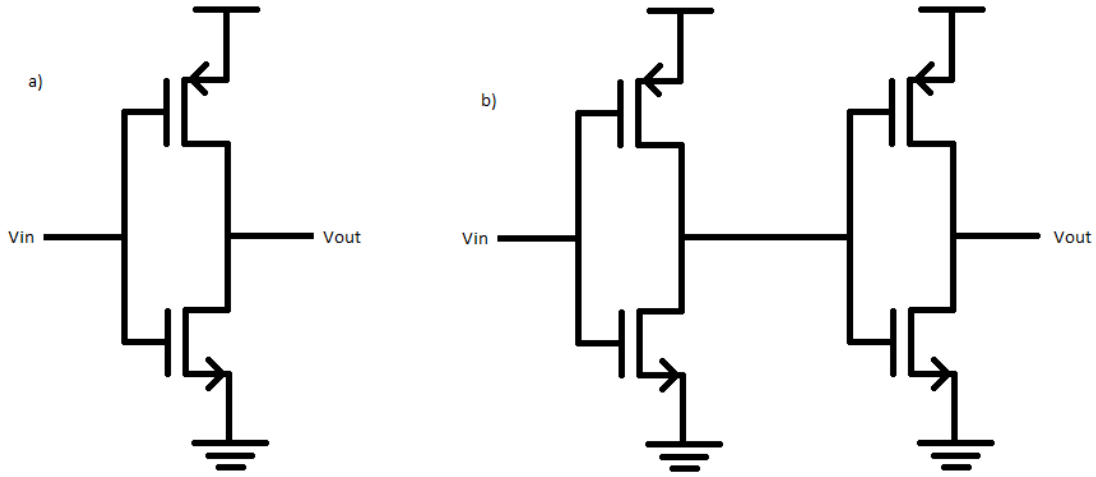

Figure 1. a) CMOS inverter and b) CMOS buffer, two inverter combined in series.

Drawback of the basic inverter is that the input signal is inverted but by combining two inverter in cascade the output signal can be restored. Although this topology is very simple it lacks features. First, the input voltage threshold voltage can be fixed for certain level of supply voltage by choosing transistors widths and lengths but the switching threshold has strong dependency to supply voltage: if the supply voltage varies the threshold will vary too. Second, this topology does not have any hysteresis which is very important when input buffer has to handle real signals with noise. Noisy signal can cause wrong detections on signal edge and forwarded signal from input buffer to next circuits is distorted and exact information is lost.

Hysteresis can be added by adding a positive feedback transistors to the buffer as shown in Figure 2. These transistors sinks and sources a little amount of current and hence cause hysteresis to the buffer and buffer action is more robust. Although this is the solution for hysteresis problem the topology still suffers from the variation of the supply voltage and variation of the supply voltage affects also to the threshold voltage of the buffer.

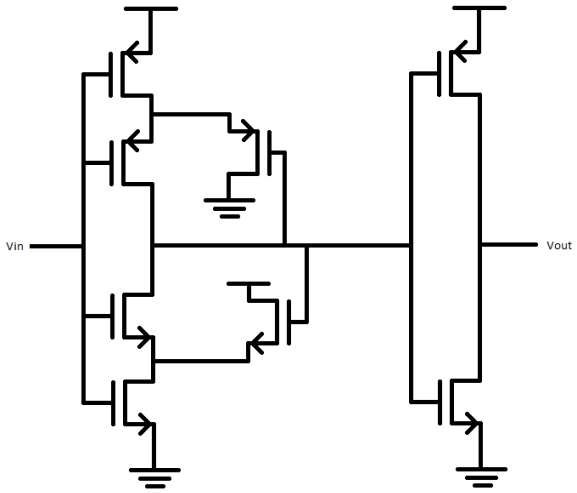

Figure 2. Buffer with hysteresis (Schmitt-trigger).

2.3. Advanced requirements and topologies

In advanced buffer designs some methods are used to handle the varying supply voltage effects. One of the ideas is to control the current which flows through the first stage transistor and by controlling the current it is possible to minimize effects of varying supply voltage.

The first method is to use some kind of current source to drive the input transistor current at a constant level and this allows setting threshold point with less dependence to the supply voltage. This method is shown in Figure 3. Assuming that we have an ideal current source which sets the branch current to the certain level it is possible to implement an input buffer which has good immunity against supply voltage variation.

One of the biggest challenges in this topology is the current source. Because the current source has to be accurate over the temperature, voltage and process corners, it is not easy to design, and it needs a bunch of transistors to implement and will occupy a lot of silicon area. Other drawback is a low level transition time because when the NMOS transistor is turned off the current source drives the same current despite of the supply voltage level and if the supply voltage is higher it will take a longer time to charge inverter gates and change the inverter output off.

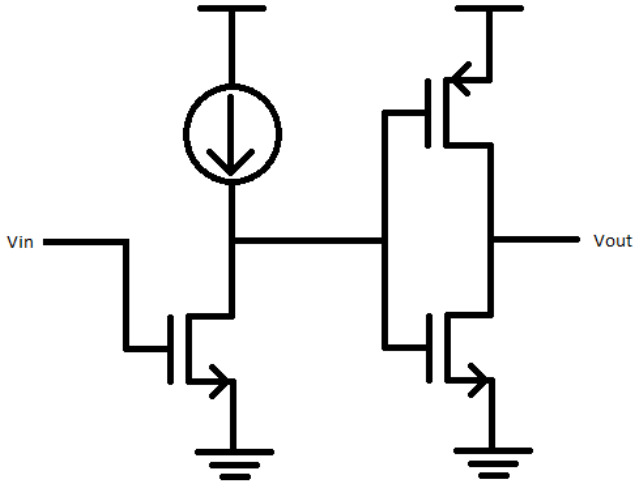

Figure 3. Input buffer with current source for varying supply voltage.

The second, simpler method is to use a resistor from higher supply voltage to the drain of the NMOS transistor, as shown in Figure 4. In this topology the resistor from the high supply voltage to the drain of the first NMOS sets the maximum current level in the branch and by choosing the first transistor width and length correctly it is possible to define a wanted threshold point. Although with this topology the triggering point dependence to the supply voltage is decreased a lot it still exist but it is possible to keep it at acceptable level.

One of the problems in this topology is the size of the resistor, it will have a value usually in a range of couple of hundreds kilo-ohms to mega ohm to keep current consumption as low as possible. Implementing a big value resistor in silicon process is not very area effective and it will cost a lot of silicon area.

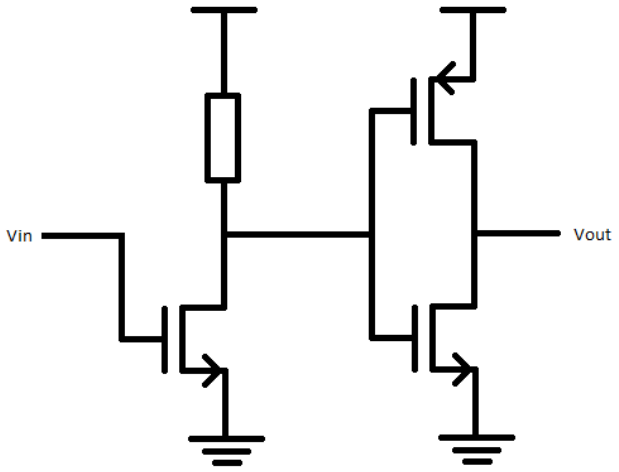

Figure 4. Input buffer with resistor for varying supply voltage.

Both above topologies (Figs 3&4) provide a way to withstand supply voltage variation but they still are missing the hysteresis functionality which helps to prevent unwanted switching due to noise. Both topologies can be improved with hysteresis functionality to make them more robustness. The challenge is to design an input buffer which combines all functionalities sufficiently together and is still

manufacturable in a modern silicon process. The other challenges are to make circuit which needs the smallest area and which has the least current consumption, especially in “off”-state when input signal is low.

2.4. Input buffer specifications

Every electrical circuit are designed to fulfil some boundary conditions wherein they should be able to function. These boundary conditions come straight from applications and environments where electronic circuits are planned to be used and usually they are obeying some known standard. That is why a product is suitable for as many applications as possible. Of course these boundary conditions can be application driven and can have very specific and tight design rules such as military and medical applications usually have.

Input buffer circuits have to be designed to achieve specified requirements so, that the variation of the supply voltage and the temperature and also a used silicon process variations are taken in account, because all of these parameters affect a lots to the operation of the circuit. The design boundary conditions for this particular design case are shown in Table 1.

Table 1. Input buffer boundary conditions

Symbol	Parameter	Limits		Unit
		Min	Max	
V_{DD}	DC supply voltage	2.0	5.5	V
V_{IN}	Input voltage	0	Vdd	V
V_{OUT}	Output voltage	0	Vdd	V
T_{AMB}	Operating free-air temperature	-40	+85	V
V_{IH_MAX}	Input high voltage	1.07	Vdd	V
V_{IL_MIN}	Input low voltage	0	0.68	V
V_{HYS}	Hysteresis	20		mV
$I_{Q\_MAX\ (OFF)}$	Quiescent current, input low state		500	nA
t_{DELAY}	Rising and falling edge delay time at worst case		1	µs

As mentioned earlier this master's thesis purpose is to design, implement and verify input buffers with different topologies. After schematic simulations the best topology will be chosen and the layout will be drawn related to the chosen topology. After the layout has been drawn post layout simulations will be run to verify the proper operation and to avoid effects of excessive parasitic components. The topology choice is based on schematic simulation results and other important parameters such as a area of a topology and a power consumption. These both have to be minimized to be as low as possible without losing the correct operation.

2.5. I/O devices and ESD

2.5.1. ESD and IC-designing

Since semiconductor industry has been developed from the middle of the 1900-century there has been challenges with the fact how to protect sensitive integrated circuits from electrical shocks which are being generated either intentionally or unintentionally outside of a chip. Integrated circuit's voltage and current levels are usually very low compared to levels which can occur during electrostatic discharge (ESD) and caused damage to internal circuits is destructive [7]. ESD has been one of the major failure mechanism during semiconductor lifetime and it is getting more and more attention on today's integrated circuits. Now-a-days circuits are even more sensitive for ESD based failures because technologies shrink all the time, transistors are smaller and gate oxides also shrink and can withstand less over-voltage stress caused by ESD.

ESD in semiconductor level is divided in three different type of occurrence depending on how ESD pulse is generated and conducted to a chip. These three types are human body model (HBM), machine model (MM) and charged-device model (CDM). The charged-device model describes a chip self-charging and self-discharging due electric field or triboelectric, the human body model represents a charged human body which discharges to a chip, and machine model shows charging due machine handling. The most destructive of the models is the CDM which has fastest transient and maximum peak current during ESD discharge. Basic phenomena to ESD failure in CMOS processes are oxide and junction breakdown in transistors and capacitors and overheating in metals and vias due excessive voltage and power. Table 2 presents ESD models electrical characteristics. [7]

Table 2. ESD models and electrical characteristics [8].

Model	I_{peak} (A)	Rise Time Leading Edge (ns)	Bandwidth (MHz)
HBM	1.33	10-30	2.1
MM	3.7-7	15-30	12
CDM	10	1	1100

2.5.2. Common ESD structures

Protecting semiconductor circuits is very important part of a design flow and it should be taken in account in early phase of the design process. In semiconductor technology there is usually specialist designers for ESD structures whose responsibility is to design protecting structures and solve problems caused by ESD.

Early days the most common ESD protection structure was reverse-connected diodes from I/O pad to high and low supply voltages (Figure 5). Although this method is simple, can handle large surge currents and is possible to simulate with SPICE, it suffers from low fixed turn-on voltage which limits its utilization in high and varying voltage cases. Other disadvantage is high power dissipation when ESD pulse occurs and it can be destructive for the diode. Despite of these diode method

still works well for low voltage and I/O lines not sensitive for parasitic components caused by diodes. [9]

More advanced method for ESD protection is to use snapback behaving devices. Snapback means the behavior of the current versus ESD voltage after ESD protection structure has triggered. Snapback devices once triggered, lower their conduction voltage while discharge current increases (Figure 5). This means lower power consumption in ESD device and lower clamping voltage to protect internal I/O structures. Snapback behaving devices are active, this means that they consist of one or more transistor and the ESD pulse triggers a transistor and actively protects circuits.

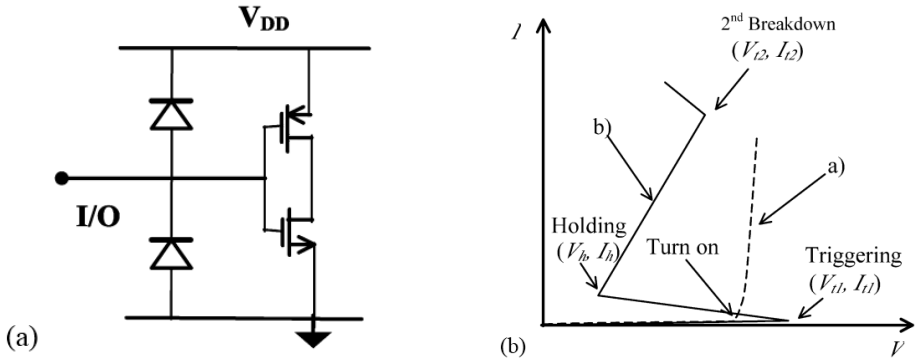

Figure 5. (a) Reverse-connected diodes to supply voltages and (b) typical I-V characteristics of a) simple turn-on and b) snapback device [9].

First snapback acting device is a grounded-gate NMOS (ggNMOS). Grounded-gate means that NMOS gate is tied to ground and drain to I/O pin. Figure 6 cross-section presents how positive ESD pulse breaks down reverse biased drain-body junction and generates hole current flow into ground via body. Since body and source are grounded current builds up positive voltage between body and source which turns on the lateral NPN transistor and forms low-impedance discharging path for ESD current. Negative ESD pulse is shunted via NMOS parasitic diode. Advantages of the ggNMOS is active protection which can be optimized via physical design. Disadvantages of the ggNMOS are non-SPICE compatible snapback simulation, high holding point, low area efficiency and parasitic effects.[9]

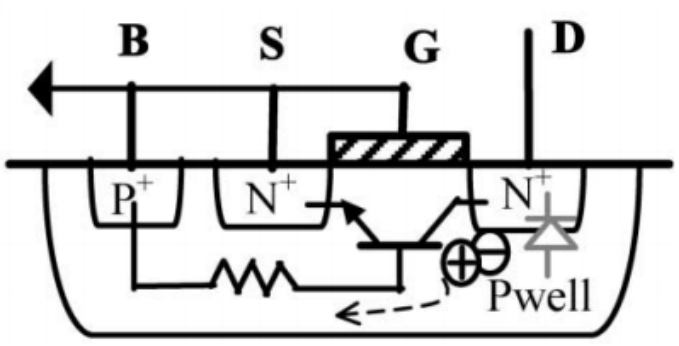

Figure 6. Grounded-gate NMOS (ggNMOS) cross-section view and triggering mechanism current flow through substrate [9].

Another snapback acting device is a silicon-controlled rectifier (SCR). Its advantage is deep snapback behavior and high current handling capacity in small silicon area. Figure 7 shows the schematic and the cross-section view of the SCR ESD structure. The SCR operates so that when a positive ESD pulse occurs at the anode (A), it breaks down the base-collector junction of vertical PNP Q1 and generates hole current flow through parasitic substrate-R which turns on the lateral NPN Q2 and SCR triggers. A disadvantage of the SCR is that it is sensitive for latch-up effect. Holding current must be designed higher than any other currents on the chip and proper isolation using double guard rings must be used. Other problem is negative direction ESD pulse because it is discharged via parasitic diode of the SCR which restricts its usage in high voltage mixed-signal ICs. [9]

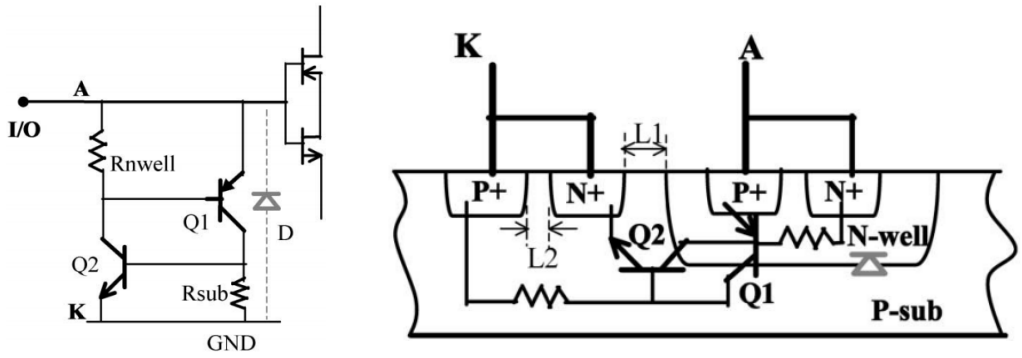

Figure 7. SCR ESD structure schematic and cross-section view illustrating how current paths and parasitic transistors are formed [9].

Integrated circuits need ESD protection for every input, output and power lines. The perfect ESD protection structure should be able to be low-impedance, low-holding, non-destructive discharging path for all ESD pulses and act in active device mode to be suitable for SPICE modeling and have negligible leakage in off-state. Combining all of these properties together is the big challenge which has been tried to solve by ESD designers to achieve full chip ESD protection.

3. DESIGN OF THE INPUT BUFFERS

In this chapter both input buffer topologies and design flow including simulation results are presented and explained. Especially the topology in Section 3.2 is discussed with more details how the input buffer is designed and verification is performed for this particular design. And what are the most important parameters where to focus on during the design flow and what was needed to do to achieve specification limits.

Both input buffers have a passive RC-filter in input line. The filter -3 dB bandwidth is 2MHz and its purpose is to filter a high frequency noise away from the input signal. Designed input buffers are slow control input buffers and high frequency noise would be harmful for they operation and it has been stated that filtering input noise is beneficial for operation of a input buffer. Also because buffers are slow, input signal filtering is not violating control signal itself. In a case of fast input buffer, any filtering will slow down signal and cause extra delay to transmission.

3.1. Circuit 1, PTAT biased input buffer

3.1.1. Theory and designing

As mentioned earlier there are couple of ways to implement an input buffer with a constant threshold voltage. One of the key issues is to find a way to control a current through a first stage transistor on which gate an input signal is applied. The solution is not to make a current flow at certain level over temperature range. The current should preferably dynamically change when temperature changes because the 1st stage NMOS threshold level changes also.

In this PTAT topology the first stage current is fed through PMOS transistor which acts like a current source. The PMOS current is controlled by a PTAT bias circuit which forces the PMOS to source the current proportional to a temperature. The idea behind the PTAT sourced first stage is that the NMOS transistor threshold voltage decreases with negative slope when temperature rises. Another idea is to minimize effects of a supply voltage variation to the first stage current and thereby minimize input buffer threshold variation.

The input buffer consists of two main parts which are the PTAT bias circuit and the input buffer itself which recognize the level of the input signal. The topology of the input buffer is presented in Figure 8 and the PTAT bias circuit in Figure 9. More detailed figures about schematics are presented in Appendix 1 and 2.

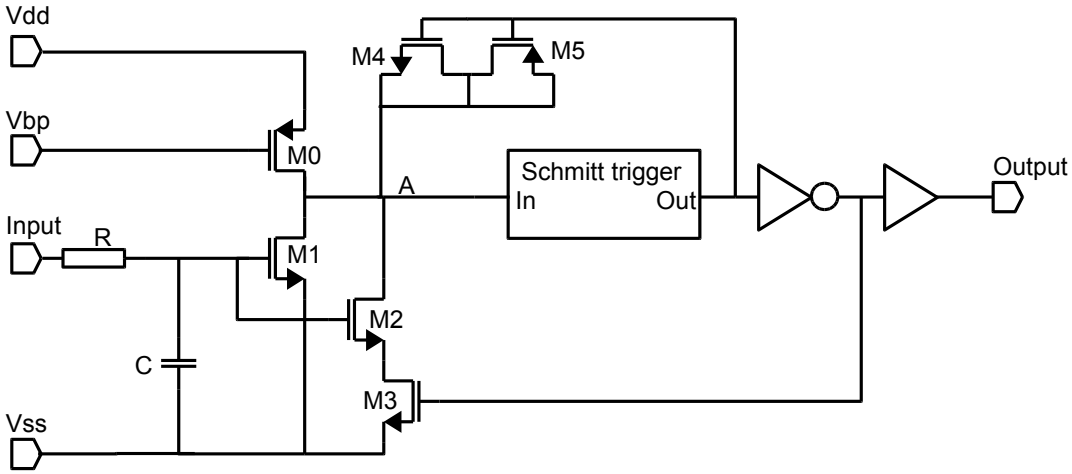

Figure 8. The input buffer topology.

The PMOS transistor M0 is the current source which is biased by the PTAT bias circuit. The transistor feeds the current to node A and thus when the first stage NMOS transistor M1 gate voltage, the input pin, is low raises the node A voltage up to a supply voltage. Now if the input pin voltage is raised above the M1 threshold voltage it begins to conduct current and there is a threshold voltage level in a Schmitt trigger when the node A voltage has lowered enough the Schmitt trigger changes its state from high to low and this point the input pin the Vih threshold is detected and transferred forward. And vice versa when input pin is lowered there is the threshold voltage Vil when the buffer changes state from high to low.

There are also additional transistors M2 to M5 in the schematic in Figure 8. Transistor M2 is connected in parallel with M1 and M3 function as a switch. When the input signal is low and node A is high the transistors M2 and M3 are closed. After input signal has risen up transistors M1, M2 and M3 are open and sinking all the current which transistor M0 can source. Now when input signal falls transistors M1 and M2 in parallel are stronger to sink M0's current and as a result the input signal has to fall lower on falling edge than rising edge before the node A is low enough to get the Schmitt trigger to change its state. So the purpose of transistors M2 and M3 is to add DC hysteresis to the input threshold voltage to avoid oscillation of the output signal. The purpose of the transistors M4 and M5 is to add AC hysteresis over Schmitt trigger. In simulations it was seen that in some corners the node A is very weak and glitches to the node A when the node A was changing state caused too many state transition at a time. This AC hysteresis causes capacitive kickback to the node A and prevents erratic state changes. In this kind of applications the hysteresis is usually necessary to get buffer function properly because even a small amount of a noise signal added to the input signal could get the input buffer triggering more than one time on both input signal edges and it would cause erroneous function in other blocks.

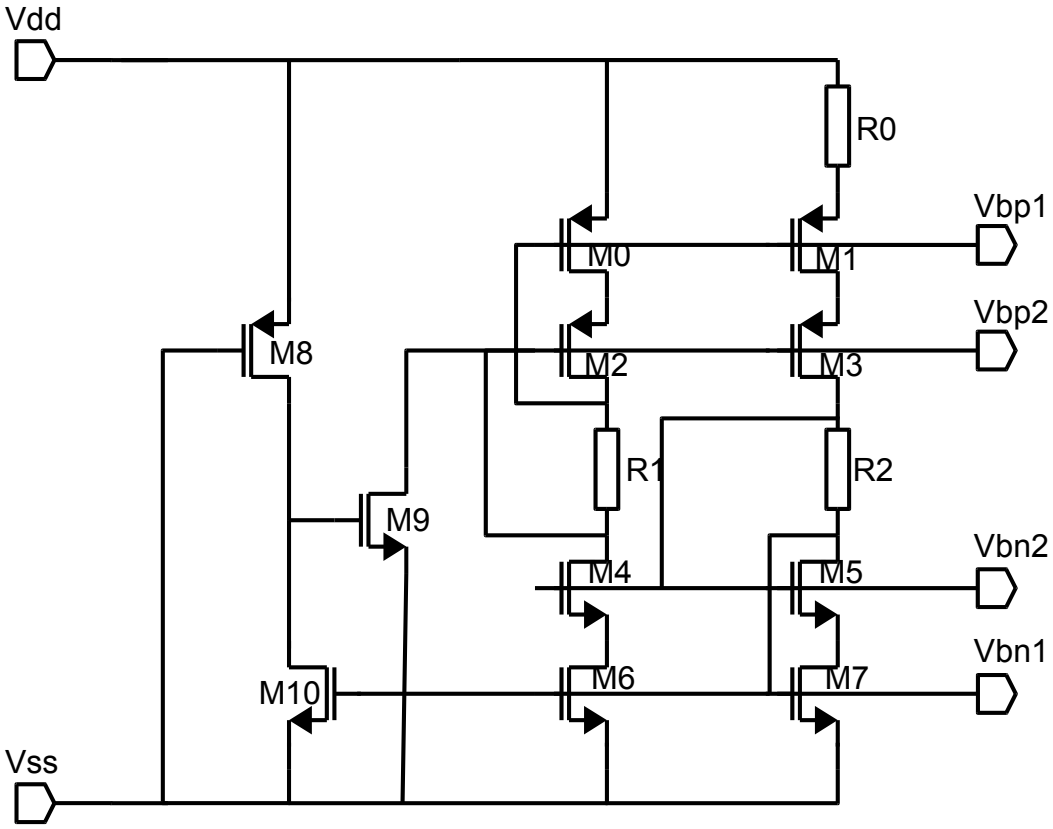

Figure 9. The PTAT circuit topology.

The design phase was started with porting the schematics in Cadence IC-circuit design environment from earlier process to the thinner line width process. After that the PTAT and the input buffer topologies were modified to achieve design specifications listed in Table 1. The main modification was to get the shutdown current consumption of the PTAT bias circuit under specification limit[10][11]. And because the bias current was changed had to the input buffer transistors M0 and M1 be modified to meet specified threshold levels in all conditions over process, voltage and temperature (=PVT) variations.

3.1.2. Simulations

After porting the design to the 180nm process a simulation test bench in Cadence IC design environment was accomplished and it was used for simulating behaviour and functionalities of the input buffer in different conditions. The input buffer simulation test bench is shown in Figure 10. It consists of the input buffer itself, PTAT bias current circuit and also there is strong buffer after the input buffer output which drives the estimated capacitive load. There are also voltage sources which are used to generate the needed high and low power supply voltage levels and the input signal waveform. There is also a pull down resistor in the input pin and couple of capacitors in PTAT circuit outputs but those purpose is only prevent floating node errors in simulation environment.

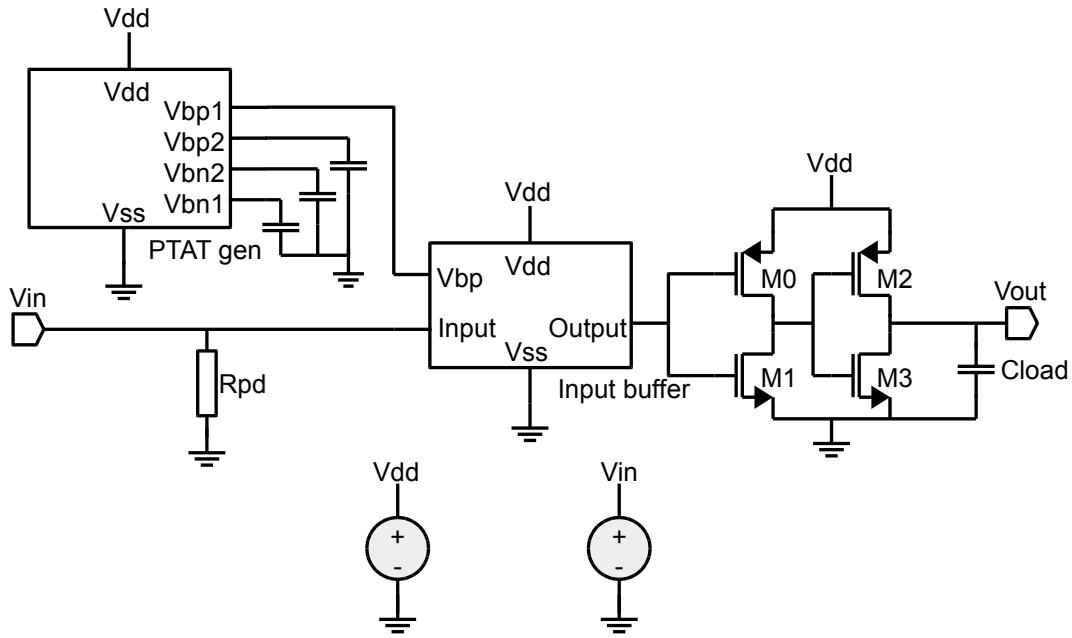

Figure 10. The input buffer simulation test bench.

Simulated input signal waveform is presented in Figure 11. This waveform includes first slow rising and falling edge to find out threshold voltage Vih and Vil triggering points. The input voltage is first swept from 0.6 V to 1.15 V and back. Threshold limits are defined so that the input buffer output must be set to a high state before the input signal reaches 1.07 V on rising edge and output must be set to a low state before the input signal reaches 0.68 V on falling edge. Both rising and falling edges lasts one second. After the slow edges the input voltage level is driven from 0 V to 1.8 V (3 ms pulse, 10 ns edges) to verify current consumption in ON-state. After that there is a level change from the lower threshold limit 0.68 V to the higher voltage limit 1.07 V and vice versa. This extreme worst case is used to measure maximum turn-on and turn-off times. Maximum time results are presented in Figure 12 and 13. The fourth part of the waveform is narrow 1.8 V pulse (50 ns, edges 1 ns) which is used to test the input buffer and its RC-filter robustness to suppress voltage spikes and a noise in input signal. All results in Figures 11.-13. were simulated over PVT corners and simulations were performed for the final PTAT input buffer version where all the simulated parameters fulfil specifications.

Simulations results are presented in Table 3. Process variations impact is about ±14 % to switching level and temperature variation from -40°C to +85°C causes M0 current change from -70% to 275 % compared to typical process corner and nominal temperature +25°C and supply voltage 3.7 V.

Table 3. The PTAT input buffer simulation results

Description	Vih (V)	Vil (V)	Vhys (V)	Time delay on worst (s)	Time delay off worst (s)	Iq_sd (A)
Minimum	761.5m	713.4m	29.6m	61.95n	64.89n	72.45n
Typical	894m	852.2m	41.7m	160.3n	186.6n	174.1n
Maximum	1.034	998.8m	61.8m	502.2n	501.9n	384.6n

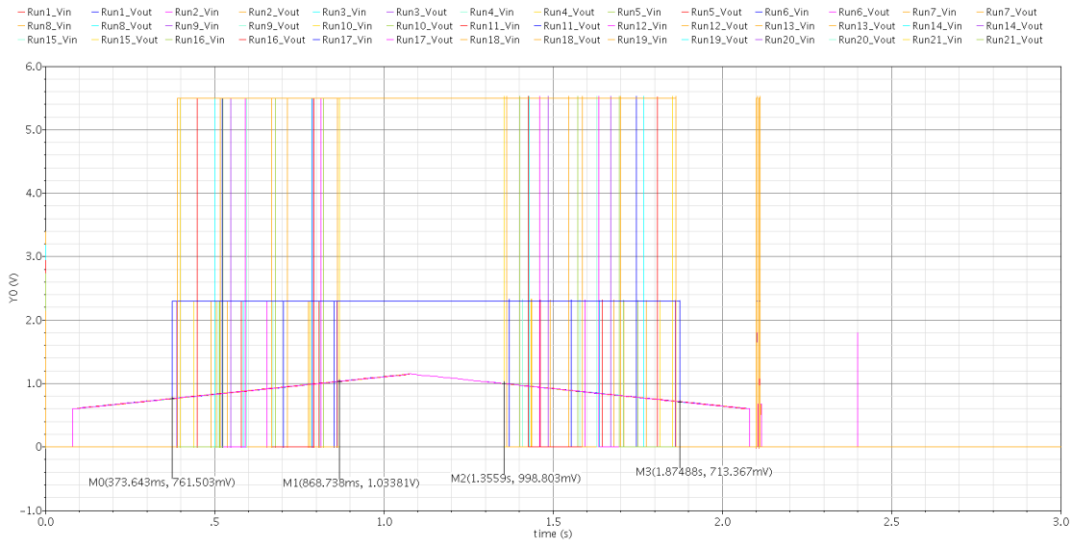

Figure 11. Input signal threshold voltages over PVT corners.

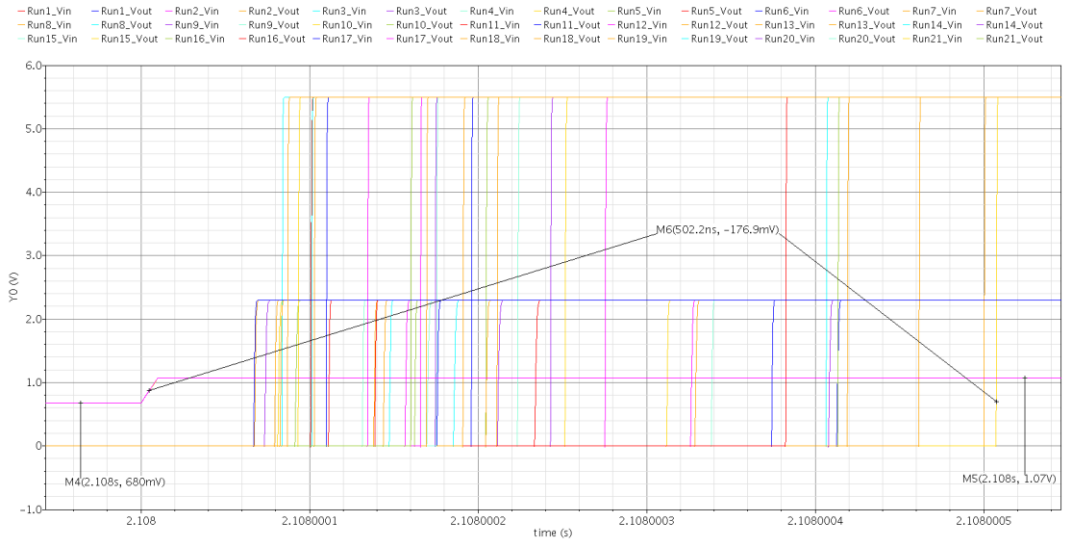

Figure 12. Input signal turn-on delay over PVT corners.

Figure 13. Input signal turn-off delay over PVT corners.

3.2. Circuit 2, resistor biased input buffer

3.2.1. Theory and designing

The resistor biased input buffer topology differs from the PTAT topology so that there is no active component sourcing the current to the first stage NMOS. This active source has been replaced with pull up resistors and M0 and M1 transistors are designed to sink all the current when the input is at high state. The topology is presented in Figure 14. More detailed figure is presented in Appendix 3.

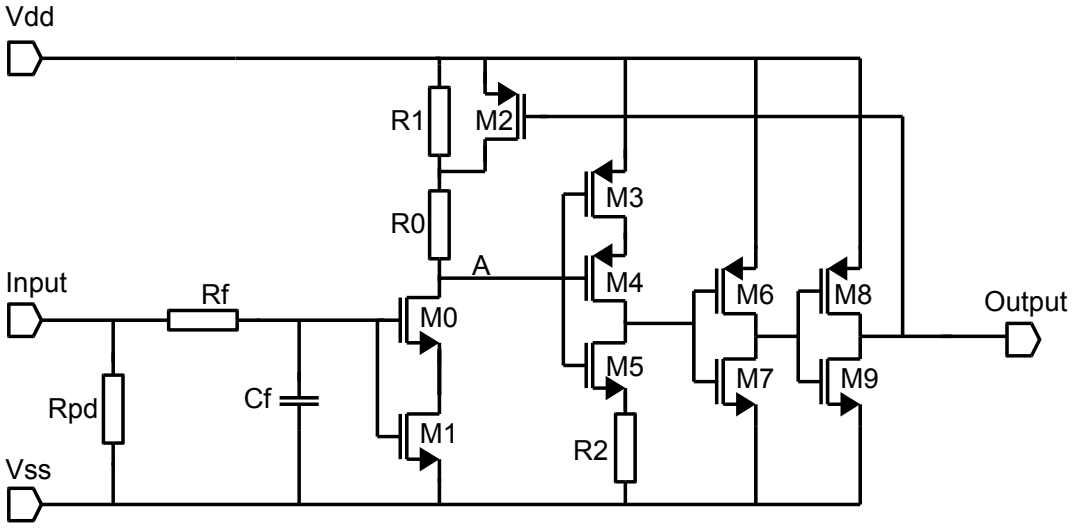

Figure 14. The resistor biased input buffer topology.

The pull-up resistor consists of two resistor in series and the purpose of this division is to add hysteresis to the threshold voltage. When the input is at low state the transistor M2 is open and the upper pull-up resistor, resistor R1, is bypassed with low-impedance trace compared to the resistor R1. This effectively causes that pull-up is stronger and the input signal has to rise higher to sink current enough and to get the 1st node voltage low enough to get the 2nd stage change its state. Right after the input signal has risen high the transistor M2 is closed and the resistors R0 and R1 are in series and the input signal has to fall lower level to get node A to rise enough to change the 2nd stage. As mentioned in the PTAT chapter this hysteresis is needed for increase robustness against noisy input signal which could cause oscillation of the input buffer and cause erratic state recognition. The hysteresis generation in the proposed signal direction helps also to reduce on-state current consumption.

In this topology the 2nd stage is like the inverse of the 1st stage. The purpose of the special 2nd stage is to minimize a variation of the threshold voltage caused by the supply voltage variation. The threshold voltage variation is tried to minimize by connecting resistor R2 between the NMOS M5 and the Vss voltage and this effectively gets the 2nd stage tracking the Vdd variation to cancel out the input buffer dependency about the Vdd voltage. The 3rd stage is like a basic inverter although it has been dimensioned to have a higher triggering point than a half of the supply voltage range. To scale triggering point upwards PMOS M6 has to be made stronger than NMOS M7. 4th stage is a basic strong inverter and its triggering point is in the

middle of the supply voltages. The 4th stage also feeds feedback for the hysteresis transistor M2.

The threshold voltage calculation of this kind of input buffer is done in a similar way as for a basic inverter. The threshold voltage of the each stage is resolved when incoming and outgoing current to a output node are equal. More complexity for the threshold point calculation cames from the 1st and the 2nd stages where there are resistor in series with transistors.

The input buffer threshold voltage calculation begins from the 1st stage which consist of the pull-up resistors R0 and R1 and the transistors M0 and M1. To simplify the current equations transistors M0 and M1 are treated as a single transistor M0 and the transistor M2 Rds_{ON} is negligible so it is not taken in account. The threshold voltage calculation is done to a rising input signal direction when signal rises from low to high, it can also be examined to a falling direction same way as for rising direction. Constituted current equations for the 1st stage are presented in Equation (1) and (2). Equation (2) shows the NMOS transistor drain current in saturation region [12]. In equations the V_I is the input voltage and the V_A is the first node voltage. The K_N and K_P includes process related parameters about mobility and gate oxide capacitance. The K_N and K_P are represented in Equation 3.

$$I_1 = \frac{V_{DD} - V_A}{R_0} \tag{1}$$

$$I_1 = K_n \frac{W_{M0}}{L_{M0}} (V_I - V_{tn})^2 \tag{2}$$

$$K_N = \frac{\mu_N C_{OX,N}}{2} \; and \; K_P = \frac{\mu_P C_{OX,P}}{2} \tag{3}$$

Combined Equation (4) presents the relationship between the V_{DD} and the V_I. In the Equation (4) is shown that if the V_{DD} changes will the V_I change too. To mitigate the V_{DD} voltage impact to the threshold voltage V_I the special 2nd stage was designed. It can be thought that the 1st stage transistor M0 should be acting as a current sink with a fixed V_{GS} voltage from the gate (V_I) to the source (Vss) and when the V_{DD} voltage fluctuates will the node V_A voltage follow this change linearly. In the PTAT biased input buffer version the first stage current level is fixed and this attach the threshold voltage. The idea behind the 2nd stage is to get the stage threshold voltage tracking the V_{DD} voltage as the 1st stage tracks. This tracking is implemented by the resistor R2 which raises the threshold voltage of the 2nd stage and gets it to track the V_{DD} voltage.

$$V_I = \frac{\sqrt[2]{(K_n L_{M0} V_{DD} - K_n L_{M0} V_A) W_{M0} R_0} + K_n V_{tn} W_{M0} R_0}{K_n W_{M0} R_0} \tag{4}$$

The 2nd stage consist of the transistors M3 and M4 which are combined to the one transistor M3 to simplify equations. In addition the 2nd stage has NMOS M5 and the resistor R2. The 2nd stage current equations are represented in Equations (5) and (6). To form analytically solvable equation the Equation (6) current had to be approximated to be linear because if the value of the resistor R2 is high enough, in

the order of hundreds of kilo-ohms, the current I_2 is almost linear and the transistor M5 effect is negligible. The approximated current I_2 is presented in Equation (7).

$$I_2 = K_p \frac{W_{M3}}{L_{M3}} \left(V_{DD} - V_A - V_{tp}\right)^2 \tag{5}$$

$$I_2 = K_n \frac{W_{M5}}{L_{M5}} (V_A - R_2 I_2 - V_{tn})^2 \tag{6}$$

$$I_2 = \frac{V_A - V_{tn}}{R_2} \tag{7}$$

By solving the Equations (5) and (7) the 2nd stage threshold voltage is presented in the Equation (8).

$$V_A = -\frac{\sqrt[2]{\left(-4K_pL_{M1}V_{tp} - 4K_pL_{M1}V_{tn} + 4K_pL_{M1}V_{DD}\right)W_{M1}R_2 + L_{M1}^2}}{2K_pW_{M1}R_2} + \frac{\left(2K_pV_{tp} - 2K_pV_{DD}\right)W_{M1}R_2 - L_{M1}}{2K_pW_{M1}2} \tag{8}$$

By placing Equation (8) to Equation (4) the threshold voltage V_I was resolved. In Figure 15 is plotted the resolved Equation (4) and Equation (8) as the function of the V_{DD}. In this plot is shown that even though the V_{DD} voltage fluctuates the V_I voltage remains at a same level and the 2nd stage threshold voltage V_A tracks the V_{DD} voltage as wanted. The V_I voltage stability was the one of the main design goals of the input buffer.

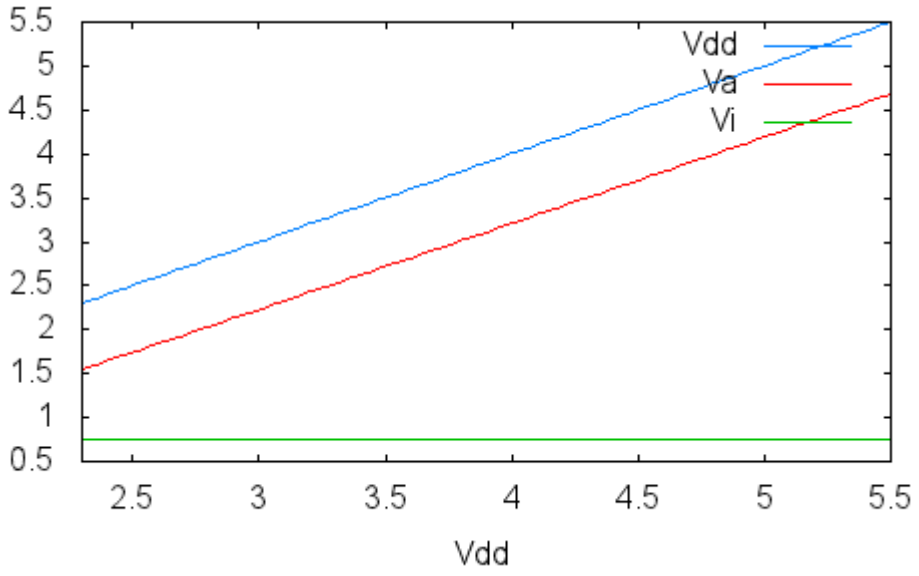

Figure 15. Equations (4) and (8) plotted as the function of the V_{DD}.

The threshold voltage V_I is a calculated approximation of a real simulated threshold voltage. One of the reasons why the threshold voltage calculation is only directional is the fact that square law of the transistor current is not the exact power of 2. When a channel length of a silicon process is decreasing under 1µm the transistor current equation is behaving more like between power of 1.2...2 [12][13]. Also channel length modulation is excluded from these equations to simplify calculation. Other reason why the threshold voltage is approximated even more is the rejection of the 3rd and 4th stage influence to the threshold voltage. The error what was done by excluding 3rd and 4th stage is very minimal because 1st and 2nd stage together has enough gain to change the input buffer state and 3rd and 4th stage will only amplify that change more and thereby cause negligible error to the threshold voltage [14].

3.2.2. Simulations

The resistor biased input buffer schematic was drawn with the same tighter line width process as the PTAT version of the input buffer so they are comparable to each other. Both designs were simulated with same test bench and waveforms to eliminate mistakes caused by different test setup and to ensure comparability of the simulation results. Simulation test bench is presented in Figure 16. It includes supply voltage sources and input signal waveform sources as well as a load capacitance.

Simulations were started with same widths and lengths as in earlier process, of course first runs were not close to the specified values so the design have to be modified to meet given specifications. Main changes for the design were in the 1st stage and hysteresis generation.

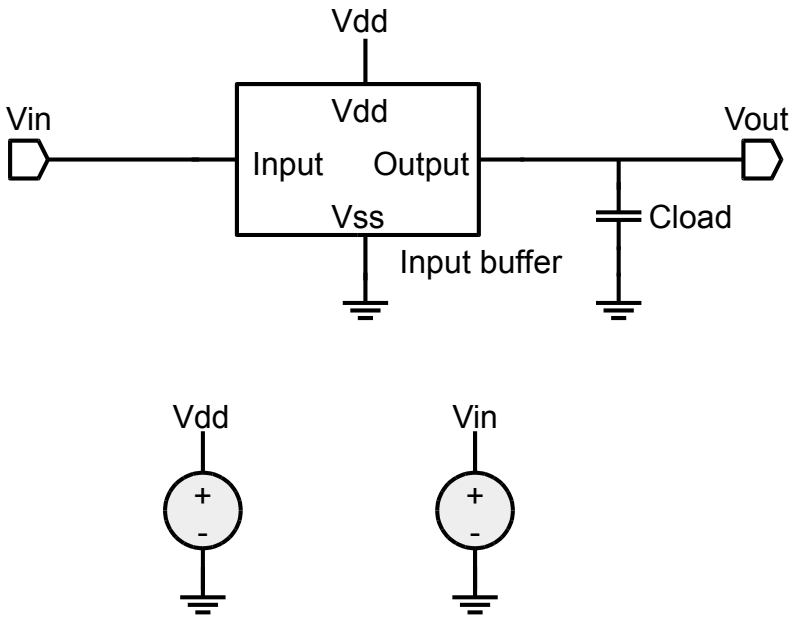

Figure 16. Resistor biased input buffer test bench.

This topology were able to be designed to meet required specifications. Simulation results for the Vih and the Vil thresholds of the final version over PVT-

variations are presented in Figure 17. There is also presented the input signal waveform in the same Figure 17. Figure 18 and Figure 19 shows the worst case turn-on and turn-off times over PVT-variations. Especially the worst case turn-off time is double as long as in PTAT version. This is limitation which derives from the resistor biased input buffer topology and hysteresis generation. When the input signal rises there are the NMOS M0 and M1 which are quite strong to pull-down current through the resistor R0 and the node A voltage falls quickly. In the other direction when input signal falls there are both resistors R0 and R1 in series to source current to the node A and this current is much smaller to raise the node A voltage as quickly as it falls.

Results of the resistor biased input buffer over PVT-variations are presented in Table 4. Process variations' impact is about ±11 % to switching level and temperature variation from -40°C to +85°C causes on-state current change from -60% to 200 % compared to typical process corner and nominal temperature +25°C and supply voltage 3.7 V.

Table 4. The resistor biased input buffer simulation results

Description	Vih (V)	Vil (V)	Vhys (V)	Time delay on worst (s)	Time delay off worst (s)	Iq_sd (A)
Minimum	736m	694m	30m	67n	221n	19f
Typical	899m	858m	40m	170n	432n	1p
Maximum	1.055	1.017	55m	560n	1028n	173p

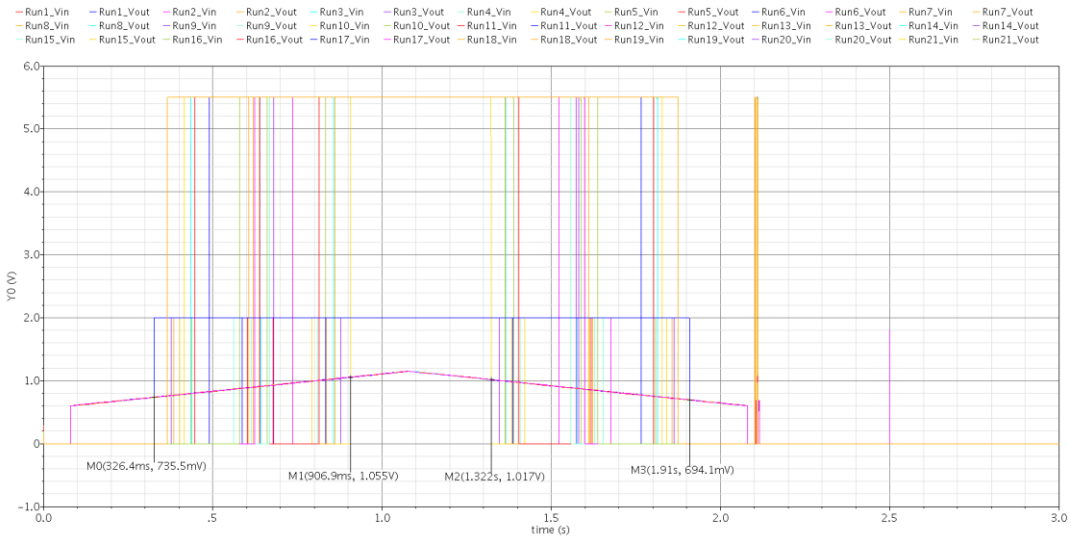

Figure 17. Input signal threshold voltages over PVT corners.

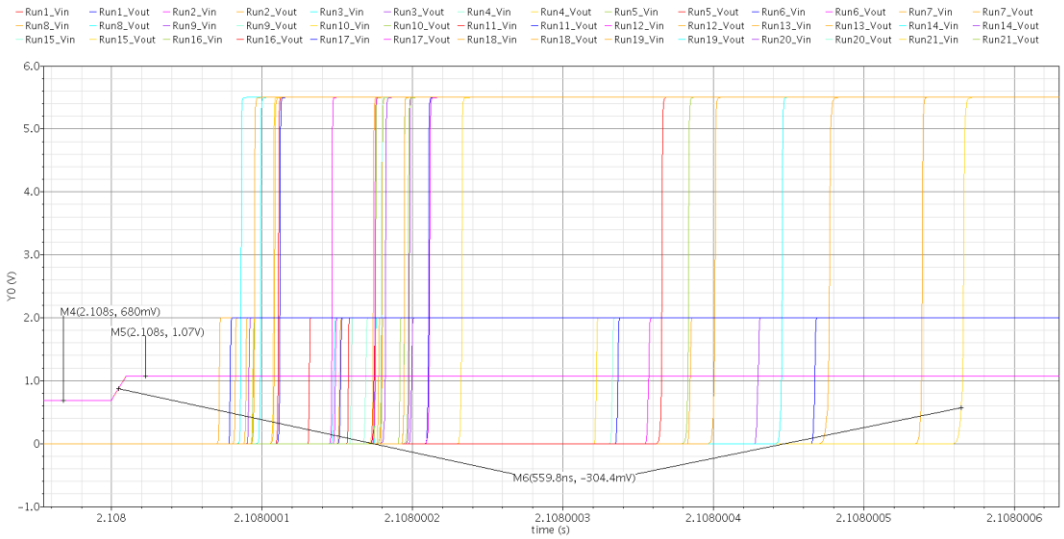

Figure 18. Input signal turn-on delay over PVT corners.

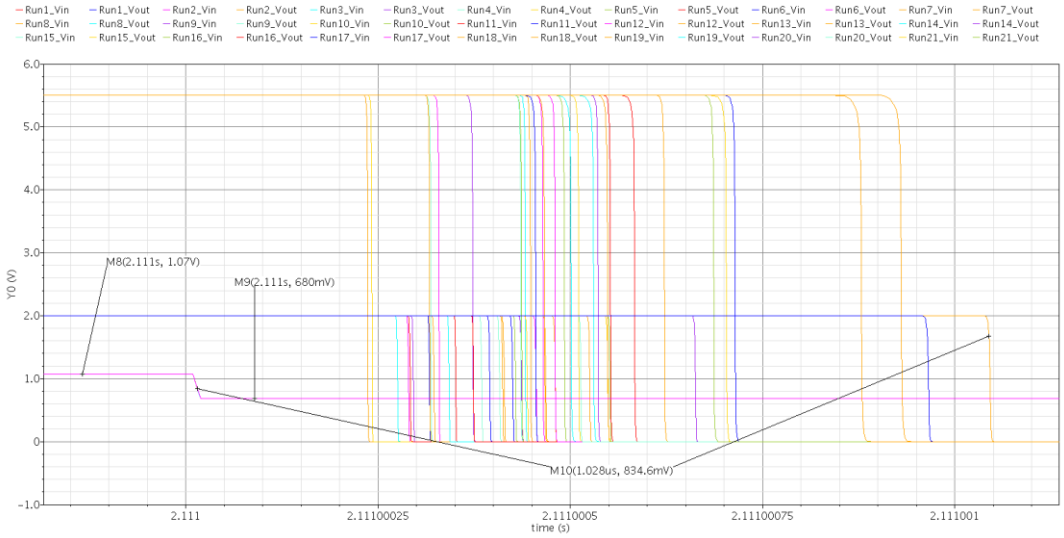

Figure 19. Input signal turn-off delay over PVT corners.

3.3. The topology choice of input buffer

Before layout phase was started the decision of which one of the topologies gets drawn has to conclude. Based on the simulation results with schematic both seem to provide almost similar performance in terms of threshold voltages and hysteresis. Comparison of a required silicon area was made by importing components to Virtuoso IC layout design environment and making quick draft layout by combining components beside each other. The PTAT biased version area is about 0.0345 mm^2 and the resistor biased version area is about 0.0059 mm^2. This leads to the conclusion that size of the resistor biased version is about 20 percent of the PTAT biased version. As the result the resistor biased input buffer was chosen because it is much more area efficient and provides same performance compared to the PTAT biased topology.

3.4. Layout design

3.4.1. IC-layout designing and its challenges

IC layout design is a challenging design work to do. Usually in IC-companies there are specialized designers for layout design. Layout designers have to be familiarized with components physical implementation and electrical and placement design rules. These rules include minimum spacing between components and wires as well as guard ring insertion rules to isolate block from other blocks and attach substrate tight to a desired potential to avoid latch-up phenomenon and noise via substrate. Good layout designer also has knowledge about which transistors must be laid out symmetrically and matched and should capacitors have common-centroid structure and is there possibility to achieve better matching by using dummy components.

Based on the area comparison and conformity of other parameters the resistor biased input buffer was chosen and layout was designed to finalize IP block for use in the future. Designed layout for resistor biased input buffer is presented in Appendix 1. Layout design process was pretty straightforward. This input buffer design is simple and it doesn't have many critical points in the physical implementation. Despite of the simple design in first time the layout was failed by drawing hysteresis feedback signal overlaying with the first node A wire too much which is the weakest point of the design. In some corners, feedback signal capacitively pulled the node A down too much and caused extra glitch to the output signal. The problem was solved by rearranging wires and transistors. Designed layout has also dummy pull-up resistors to add possibility to fine tune threshold voltage by modifying the metal mask.

In IC design projects usually the first round of silicon is not fully meeting all of its specifications. IC designs are usually designed the way that it is possible to make only metal mask change to fine tune functionalities, centralize trimmable parameters and speed up testing times using spare dummy components. First round silicon achieving specifications completely are limited by modelling accuracy of components to simulation software's and in case of a new process which is not modelled good enough or modelling is missing some parameters.

3.4.2. Post layout simulations

Every simulations which had been ran for schematic view were simulated for a RC-extracted layout view. The RC-extraction means that design software calculates resistive and capacitive parasitic components formed by adjacent and overlapping wires of the physical design. This is very important design phase, because by implementing physical layout it is possible to mess up good design by inadvertently making parasitic components which affects to a functionality.

After correcting the first layout design every simulations where ran again for the RC-extracted view. Results are shown in the Table 5.

Table 5. Post layout simulation results for resistor biased input buffer.

Description	**Vih (V)**	**Vil (V)**	**Vhys (V)**	**Time delay on worst (s)**	**Time delay off worst (s)**	**Iq_sd (A)**
Minimum	736m	694m	30m	74n	258n	178f
Typical	900m	858m	41m	187n	493n	1.38p
Maximum	1.057	1.017	57m	616n	1.16u	174p

Results shows that RC-extracted view performance remain at same level as the schematic view performance. Based on the simulation results, layout is functional and IP-block is ready for use in the future.

4. MEASUREMENT PLAN

In this chapter a measurement plan for testing the performance of a input buffer is presented. Typical verification plan is described although the test chip for the designed input buffer was never manufactured.

4.1. Application validation of an IC-design

Application validation of a manufactured chip is a required phase of a IC-design process. Its purpose is to ensure that system is functional also in real silicon, catch up design bugs and in the other hand it provides feedback information about process to designers which can this way avoid process related design problems in the future projects. Validation can also reveal design problems which are caused by insufficient or missing modelling.

Input buffer can be processed as separated test chip or it can part of the bigger test chip design or actual project design which is straight going to be sampled. Basically control type of input buffer designs are so simple that they are processed straight to an actual design project. In this case, a project application validation plan includes part to the input buffer testing in test mode.

To cover process corners variation and derive more statistical data, production testing with ATE (Automated Test Equipment) tester for a chip should be taken. The ATE tester runs test sequences for whole silicon wafer chip by chip and collects data for test engineer which plots statistical distribution of test parameters. The ATE tester also performs trimming for chips if the chips have trimmable parameters.

4.2. Bench measurement plan

Application validation, which ensures that chip is functional in its final application environment, are only done for some chips. In a case of a input buffer, bench measurement plan consists of shutdown current, DC switching point, delay and noise immunity measurements in a function of temperature and supply voltage. Measurement plan could also include ESD related test at with Human Body Model (HBM) and Charged Device Model (CDM).

4.2.1. DC switching point and shutdown current

DC switching point and shutdown current measurements are the easiest to implement. Test bench has either variable voltage source (SMU = source meter unit) or AWG (arbitrary wave generator) in the input line to make slow voltage ramp up and down and SMU or similar as the supply voltage source. Oscilloscope is needed for measuring signal levels and to identify the switching point. Figure 20 represents the test bench setup for DC measurements. Measurements variables for all bench measurements are shown in the Table 6. If a input buffer is a block inside a chip, in test mode chip has output buffers to drive input signal state to output, but if input buffer is standalone test chip it would definitely need a strong buffer between output of a input buffer and oscilloscope probe to drive capacitive load with sufficient

speed. Delays of the buffers are not causing error in DC switching point measurements, because the sweep is slow. Rising and falling times of the sweep is 1 second on both edges. Sweep voltage levels are from 0 V to 1.2 V and back to 0 V.

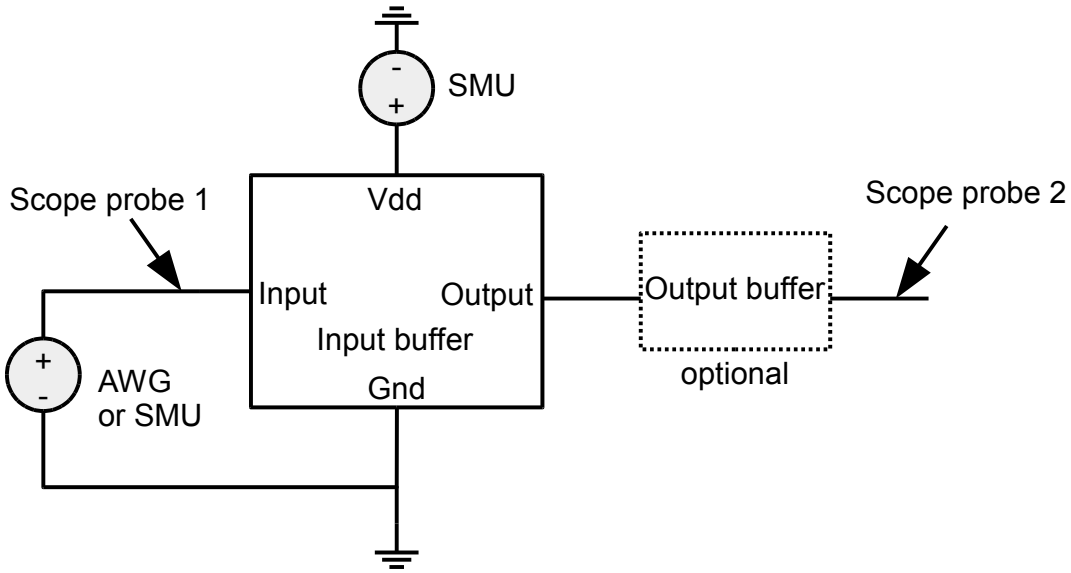

Figure 20. DC switching point test bench.

Shutdown current is observed either keeping input at 0 V or by disconnecting source from the input when internal pull-down resistance keeps input at ground and shutdown current can be measured from sourcing SMU.

Table 6. Measurement variables for all bench tests.

Description	Min.	Typ.	Max.	Unit
Voltage (Vdd)	2.0	3.7	5.5	V
Temperature (T)	-40	+25	+85	°C

4.2.2. Delay measurement

Delay measurement is much harder to implement. Problem is not with setup because actual test bench is the same as in Figure 20 and fast signal edges will be used to find output signal propagation delay self-inflicted by input buffer. The tricky thing with measurement is the delay which is either caused by chip internal output buffer in a case when input buffer is part of a product or when the input buffer is manufactured as a test chip and strong buffer is needed for driving capacitive load caused by probes. If the input buffer is part of the product, then there is no way to avoid output buffer delay because internal signals are anyway buffered to output. In a case of separated test chip it is possible to figure out delay caused strong buffer by driving buffer with AWG and measuring delay with oscilloscope for all measurement corner. Buffer delay can be measured by buffer manufacturer and written in a datasheet but to ensure buffer delay in the specified corners it could be better to measure it again. Proposed buffer could be some "74xx" logic series buffer and should have as small input capacitance as possible to avoid extra propagation delay.

AWG sources the input signal level from 0.68 V to 1.07 V and back to 0.68 V with 10 ns edge times. These voltage levels are the minimum and maximum level between which the input buffer changes state from low to high and vice versa depending on a signal direction. Since delays of input buffer with strong buffer and strong buffer are measured, calculation of the input buffer delay can be done by subtracting the strong buffer delay from total delay.

4.2.3. Noise immunity

Noise immunity test is conducted with same test setup as earlier tests. Only the AWG signal is modified to pulse between 0 V and Vdd with 1 ns edge times and pulse width is varied between from 10 ns to 100 ns.

A better way to find out noise immunity could be achieved by driving the input with signal levels 0.68 V and 1.07 V separately and for both signals add negative and positive pulse sequentially after every 250 ns period. Pulses should have 1 V peak-to-peak voltage and edge times 1 ns per edge and 1ns hold time. If noise filtering works correctly it should filter this noise away and with DC signal level of 0.68 V output stays at low state and with 1.07 signal level output stays at high state all the time.

4.2.4. ESD testing

ESD testing is very straight forward implemented test. The chip is just shot by ESD gun and chip functionality is tested after every third shot. ESD testing should include both HBM and CDM testing because chips are handled by assembling devices in factory.

5. DISCUSSION

Designed input buffers worked as specified and the resistor biased input buffer was chosen to be implemented because its size was overwhelming smaller compared to PTAT biased input buffer. Silicon area on today's IC designs focusing to mobile applications is very restricted and saving area is usually the most important thing. The implemented input buffer is a ready IP-block which can be used in future projects.

Although both buffers fulfilled design specifications in terms of performance, by designing the PTAT version more carefully it could be possible to tighten it thresholds window where the buffer triggers to a low or a high state. This could be achievable by carefully matching the PTAT current slope to compensate NMOS transistor threshold voltage so that when the threshold voltage lowers towards hot temperatures the PTAT current increases with a right amount of current to keep input buffer triggering level at constant level. This could be a cure for temperature related triggering point shifting. Also the PTAT circuit occupies a lot of silicon area. Redesigning the PTAT circuit smaller by using active resistors, more area efficient start-up circuit and minimizing process variables related errors it would be possible to make the PTAT biased buffer with tight threshold voltage window.

The PTAT biased input buffer would be more interesting in case when an application has more than one or two input lines. Multiple input buffers can share the same bias voltage from one PTAT block and only input buffer blocks needs to be multiplied.

One of the lesson what was learned during thesis is that although the MOS transistors Vth voltage has negative dependency to temperature the MOS drain current still decreases towards hot. This is caused by the reduction in mobility in channel because if MOSFET is biased over its Vth voltage and temperature rises the mobility reduction in channel is dominating the drain current and drain current decreases. This leads to the conclusion that the first stage biasing current should be more like inverse of the PTAT current which increases towards hot. Inverse PTAT current is called CTAT which means a complementary to absolute temperature. However this mobility parameter is process related and finding it out would help the design of this kind of input buffers.

In the resistor biased input buffer next improvement step could be decreasing ON-state current consumption. Current consumption decreasing would be achieved by adding a PMOS transistor in series with biasing resistor and controlling it with the input signal. A problem which could arise is the turn-off delay increasing of the input buffer because when the input is high the PMOS is closed and when the input goes down, must the PMOS turn-on to conduct current. By designing the PMOS big enough this should not be the problem. The resistor biased input buffer area might also be shrinkable by replacing the passive pull-up resistor by an active pull-up. Big resistors occupy a lot of silicon area and replacing them by active transistor, or transistor in triode region, the input circuit would be more area efficient.

Because of slow control type of a input buffer the input has the passive RC-filtering to filter input line voltage. Input voltage can capture every kind of noise outside from chip. The main noise source in this application is supposed to be a switched mode power supply (=SMPS) chip wherein the input buffer is controlling

the operation of the SMPS and the noise from SMPS would disturb the input buffer state accidentally without filtering. In addition to the passive filtering the input buffer has a hysteresis. Hysteresis where designed to have as much as possible and together with passive filtering them should prevent unwanted state changes of the input buffer. Hysteresis and filtering can be modified, increased or reduced, only making a metal mask change. This is allowed by adding dummy resistors to the design and those can be taken in use only by making routing changes into layout and processing chip again.

Although the IP-block design porting from one process to other is a straightforward process, the designer needs to understand which process parameters change and how much. And maybe the most important thing, if a design has special components like isolated transistors that is the design possible to working without those special components and how its performance can suffer. Figuring out how much process parameters and temperature changing causes variation to the threshold voltage helps the design process and leads to better performance of the input buffer.

6. CONCLUSIONS

Integrated circuits have input and output specified pins which are used to communicate and control chip. These I/O-pins can have specified functionalities as communication with some protocol or control pins can have some special threshold voltage levels or driving capabilities.

The purpose of this master's thesis were to be designed fixed threshold voltage input buffer for a slow control input. The circumstances which makes fixed threshold voltage point keeping challenging are varying supply voltage, temperature and process variations. An input buffer topology should be capable to tolerate and overcome these circumstances and try to keep triggering point as fixed as possible. Triggering point specifications comes from the Jedec standard for low voltage applications which ensures chip compatibility with other chips and controlling of the chip is well specified. The designed and implemented topology fulfilled specifications and is functional based on the simulations. Also the layout for the input buffer were drawn and this way the input buffer IP-block were finalized.

The measurement plan for fixed triggering voltage input buffer was introduced. Measurement plan was examined although the designed input buffer were not measured in a real silicon. Measurement plan goes through basic measurements how this type of input buffers should be verified in real application and what things should be taken in account with input buffers measurements.

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8. APPENDICES

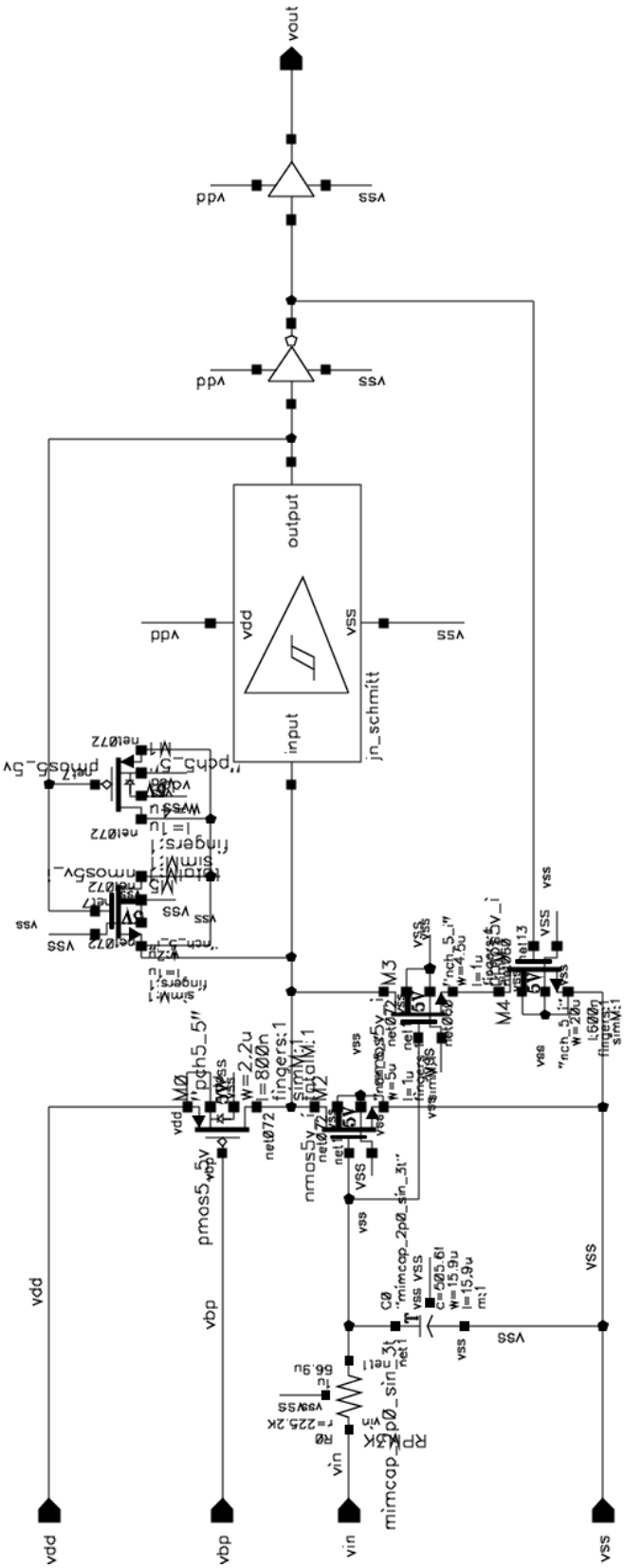
Appendix 1. PTAT biased input buffer schematic

Appendix 2. PTAT bias circuit schematic

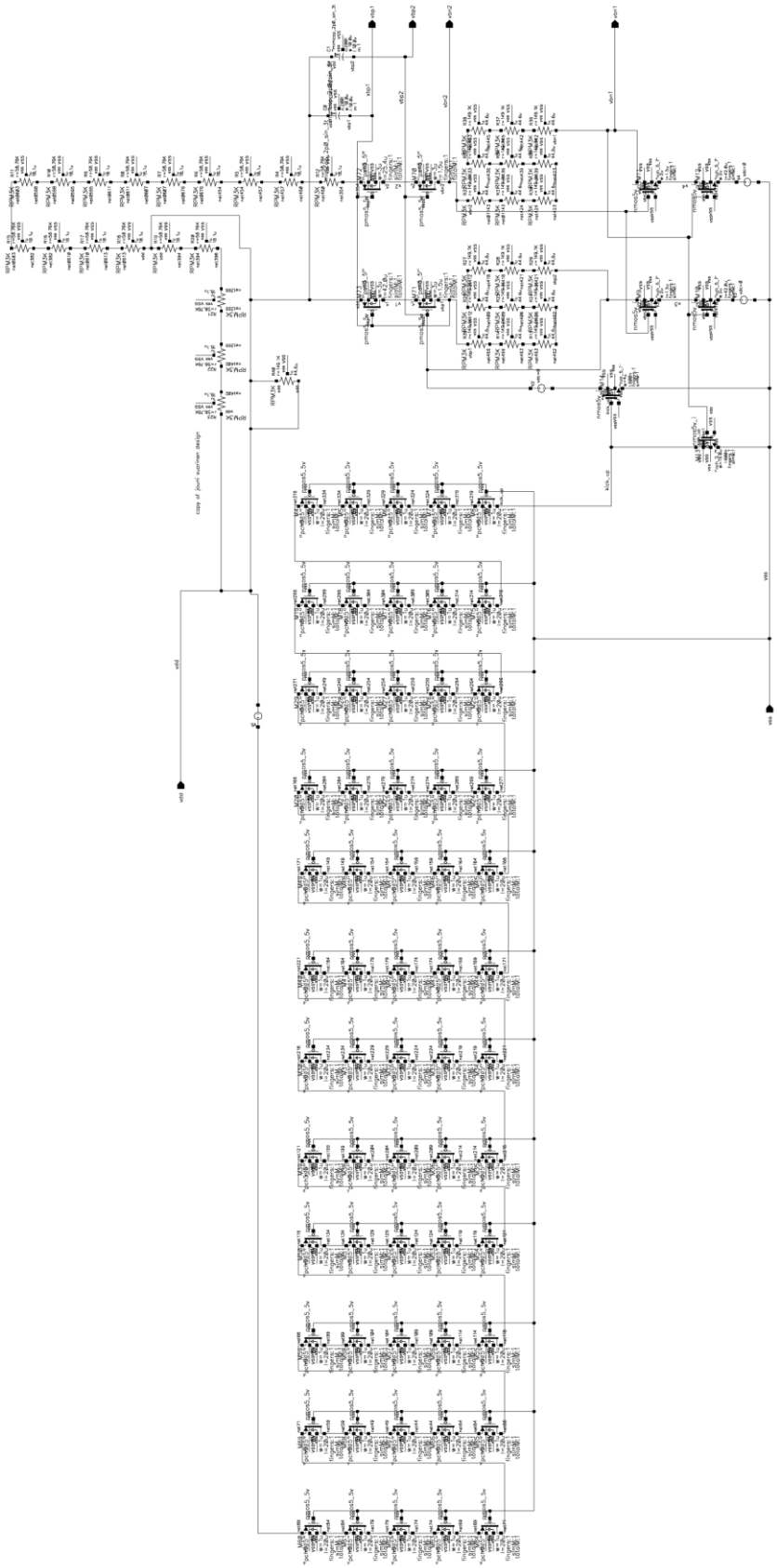
Appendix 3. Resistor biased input buffer schematic

Appendix 4. Resistor biased input buffer layout

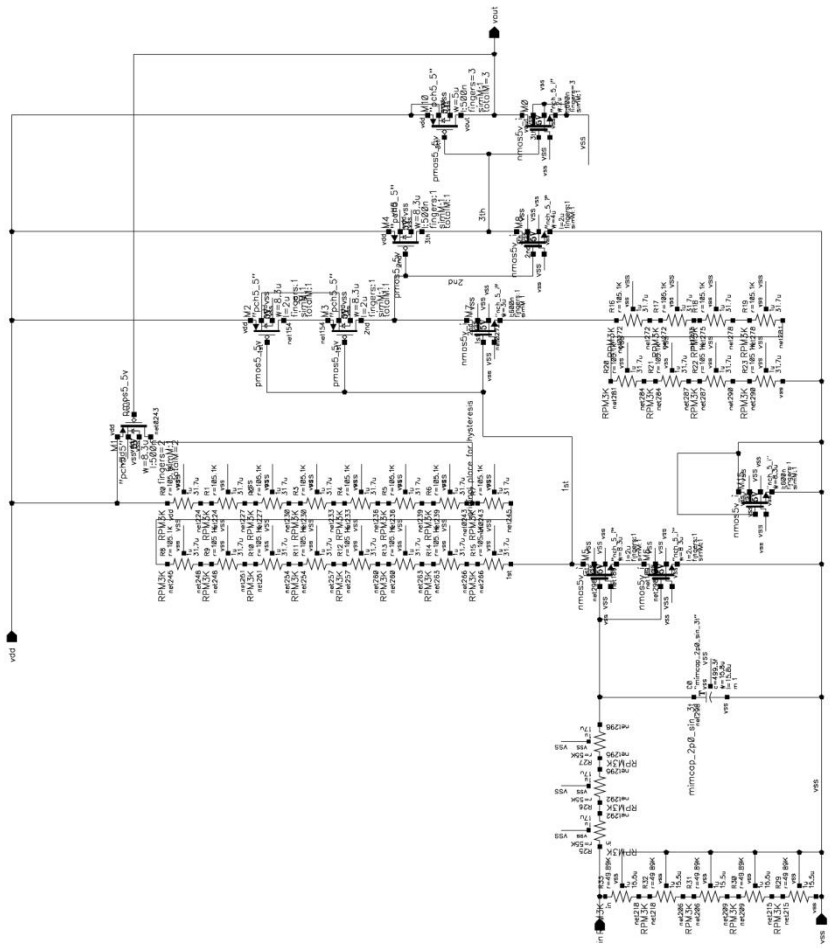
Appendix 1. PTAT biased input buffer schematic



Appendix 2. PTAT bias circuit schematic



Appendix 3. Resistor biased input buffer schematic



Appendix 4. Resistor biased input buffer layout