ON THE EFFECTS OF TOTAL IONIZING DOSE IN SILICON-GERMANIUM BICMOS PLATFORMS

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Master's Thesis in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2014

ON THE EFFECTS OF TOTAL IONIZING DOSE IN SILICON-GERMANIUM BICMOS PLATFORMS

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ACKNOWLEDGEMENTS

I would first like to thank my research advisor Dr. Cressler. His endless support and encouragement has made me a better researcher and has provided me with the perfect environment to continue my education. I would also like to thank the members of my reading committee: Dr. Papapolymerou and Dr. Yoder. I appreciate their taking the time to provide me with helpful feedback on this thesis in addition to being my teachers at Georgia Tech.

I would also like to thank my Mom, Dad, and brothers: Aaron and Nathan. Your support and love over the years means everything to me. I would especially like to thank my father for taking the time to help provide me with feedback on my technical work — you have taught me so much.

And I would also like to thank all my friends. Thank you to my Vandy friends Dylan McQuaide and Zac Diggins — I don't know where I would be right now without you guys. A big thank you to all the members of the SiGe team at GaTech — past and present. I am especially thankful to all the guys who have worked on radiation effects work with me: Nelson, Troy, Rajan, Adilson, Ickyhun, Jung, Farzad, Stan, and Adrian — you guys are the best.

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SUMMARY

The research presented in this thesis focuses on total ionizing dose (TID) radiation effects in Complementary Metal Oxide Semiconductor (CMOS) and Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technologies. This work includes the first ever investigation of low dose rate effects in 4^{th}-generation SiGe HBTs. In addition, it evaluates the contention of an advanced BiCMOS technology for space missions to Jupiter's moon, Europa.

Chapter 1 provides the motivation and scope of this work.

Chapters 2, 3, and 4 provide background material for this thesis. Chapter 2 presents an introduction to BiCMOS technologies and shows the benefit of Silicon-Germanium devices. Chapter 3 highlights the origins of radiation and presents a brief analysis of various radiation environments. And Chapter 4 discusses the most prominent radiation concerns for electronic engineers and highlights underlying mechanisms.

Chapters 5 and 6 include two studies of the author. Those studies include 1) the TID response of a 180 nm bulk BiCMOS process and 2) a generational study of dose rate effects in SiGe HBTs.

The article in Section 5.2 is published in *IEEE Transactions on Device and Materials Reliability* and is reference [24] in this thesis:

"Fleetwood, Z.E.; Kenyon, E.W.; Lourenco, N.E.; Jain, S.; En Xia Zhang; England, T.D.; Cressler, J.D.; Schrimpf, R.D.; Fleetwood, D.M., "Advanced SiGe BiCMOS Technology for Multi-Mrad Electronic Systems," Device and Materials Reliability, IEEE Transactions on , vol.14, no.3, pp.844,848, Sept. 2014"

The article in Chapter 6 is set to be published (Dec. 2014) in *IEEE Transactions*

on Nuclear Science and is reference [23] in this thesis:

"Fleetwood, Z.E.; Cardoso, A.S.; Song, I.; Wilcox, E.; Lourenco, N.E.; Phillips, S.D.; Arora, R.; Paki-Amouzou, P.; Cressler, J.D., "Evaluation of Enhanced Low Dose Rate Sensitivity in Fourth-Generation SiGe HBTs," Nuclear Science, IEEE Transactions on , vol.PP, no.99, pp.1,8"

Finally, Chapter 7 provides a conclusion for the work. The contributions of the author are discussed as well as possible avenues of future work.

CHAPTER I

MOTIVATION

Space is unquestionably an extreme environment. Temperature variations are drastic, air is absent, and intense radiation is ubiquitous. These conditions are not conducive to life and make it extremely difficult to operate microelectronics. Ever since the first satellite launches, it has been apparent that space radiation would be particularly difficult to handle. Particle strikes continually bombard semiconductor devices and cause an accumulation of charge to build up at sensitive interfaces. This charge accumulation due to radiation is known as total ionizing dose (TID) damage. The particles consist of highly energetic protons, electrons, heavy ions, and Galactic Cosmic Rays (GCRs). These particles are caused by solar events on the Sun, background radiation, and even nuclear weapons testing.

Modern semiconductor technologies have benefited over time from scaling — seeing an overall increase in hardness to TID damage effects as technology nodes have become smaller and smaller. One such modern technology is Bipolar and Complementary Metal Oxide Semiconductor (BiCMOS) platforms, which merge modern-day CMOS devices with the Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT). BiCMOS platforms are well suited for space electronics as SiGe HBTs are able to handle analog and radio frequency (RF) circuitry while CMOS devices are able to handle digital circuits and memory.

Due to differences in device structure, SiGe HBTs are generally multi-Mrad tolerant to TID damage whereas CMOS devices are much more susceptible. As such, it is accepted that the TID response of a BiCMOS platform will be limited by the CMOS on board and it is expected that SiGe HBT damage will be much less severe.

CHAPTER II

INTRODUCTION

Having electronics that are robust to the deleterious effects of radiation is absolutely vital to the success of all space-based missions. This includes the proper design of satellite systems and exploratory rovers which cost multiple millions of dollars and must operate correctly in any circumstance. Every mission is different and will carry its own temperature and radiation requirements. This makes electronic design for extreme environments especially challenging as engineers are forced to make trade-offs between robust operation and performance. At times it is possible to use maximum shielding, redundant designs, and custom radiation-hardened semiconductor processes. However, such an approach can significantly constrain the size, weight, and power (SWaP) of a system. These metrics are at a premium and impact the overall capabilities and cost of a system.

This work primarily focuses on the radiation response of Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) technologies, which merge the most popular semiconductor devices, n and p-type field effect transistors (FETs), with the Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT). SiGe HBTs are extremely robust to temperature and radiation effects. As built, SiGe HBTs are able to handle cryogenic temperatures below 4 K and have multi-Mrad total ionizing dose (TID) hardness [14], [13]. As such, SiGe HBTs are an intriguing option for many space missions. One such example is NASA's Europa mission, in which satellites must orbit around Jupiter's moon Europa and be capable of withstanding at least 6 Mrad(SiO_2) of TID damage. Most commercial CMOS technologies could not meet such a requirement; however, having a CMOS platform which could meet such a

requirement is very desirable.

This work covers an analysis of a 180 nm BiCMOS platform which was specifically targeted for the Europa space mission. This includes an analysis of the TID response in addition to simulation work in this technology in order to help to try and understand the technology and the TID response better.

This thesis also covers a generational study of SiGe BiCMOS platforms in the context of low dose rate response. As most terrestrial testing is undertaken at high dose rates, it is relatively unknown what the response of SiGe HBTs will be in a more realistic, low dose rate environment. This discussion helps shed light on an issue that has not been well documented in the field. Such a study helps demonstrate and prove the robust TID response of SiGe HBTs.

However, before any in depth discussion of those studies is conducted, a background and introduction into the basics of radiation effects is discussed. This begins with the basics of SiGe technology and the radiation environment.

2.1 Background of SiGe BiCMOS Technology

Complementary Metal Oxide Semiconductor (CMOS) devices dominate the semiconductor industry. They are extremely small (commercial technology is currently at 22 nm), operate extremely fast, and are relatively cheap compared to III-V technologies. However, III-V devices are still important as they are able to outperform CMOS for many radio-frequency (RF) and analog circuit applications. The advanced materials and improved device structure of III-V devices allow for lower noise figure (NF), higher output conductance, higher operating frequencies, and improvements in many key RF parameters (OIP3, IRR, etc.). As such, many technologies, like cell phones, that require top-notch RF performance will utilize III-V devices, off chip, in conjunction with CMOS devices which are still necessary to handle digital signal processing. This creates a multi-billion dollar industry for III-V RF circuitry, but

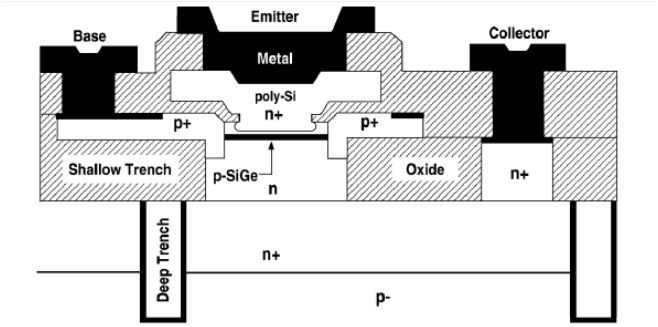

Figure 1: 2D Cross-Section of a First Generation SiGe HBT (after [31]).

requires for multiple chips to be implemented in a given design.

A more elegant solution would be to use a technology that implements both the RF circuitry and the digital circuitry together on chip. If done correctly, this would greatly reduce the cost and size restrictions of having to implement different technologies together.

One such implementation could be conceived using Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology (cross-section shown in Fig. 1). SiGe HBTs are vertically structured Silicon Bipolar Junction Transistors (Si BJTs) with the addition of a grading of Germanium (Ge) in the base region of the device. The addition of Germanium allows for bandgap engineering of the device and improves device operation in a number of ways (discussed further in Section 1.2) to make the transistor performance comparable to that of III-V devices.

SiGe HBTs are merely an add-on to existing CMOS technologies and create a combined BiCMOS (Bipolar and Complementary Oxide Semiconductor) technology. The addition of SiGe HBTs incurs minimal price increases (normally no more than 10-15%) on the original CMOS technology and allows for circuit implementation that can handle RF, analog and digital signal processing, all on the same chip.

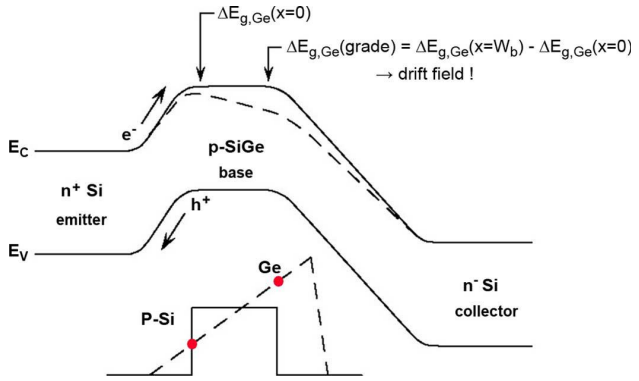

Figure 2: Band diagram of SiGe HBT (after [14]).

2.2 SiGe HBT Device Structure

Bandgap engineering enables semiconductor devices to incorporate new materials to physically alter the bandgap of the material(s) in the device. This is extremely challenging to do in semiconductor processing but, if done correctly, will greatly improve device performance. In the case of Silicon-Germanium technology, the introduction of Germanium in the Silicon lattice causes an effective shrinking of the "bandgap" in the base of the device. This shrinking, when graded over a distance, causes a slope in the band diagram which is physically realized as an electric-field which has been intentionally engineered into the device. In the case of the Silicon-Germanium Heterojunction Transistor (SiGe HBT), the additional electric-field across the base allows for the base to be much more heavily doped. This causes the base resistance to be much smaller and consequently the operating frequency of the transistor to be much higher. This allows SiGe HBTs to operate at much higher frequencies, which makes them very well suited for high-performance analog and radio frequency (RF) applications.

Fig. 2 shows the result of the Germanium grading to the band diagram of the device (compared to a standard Si BJT). The dashed line in the figure highlights the contribution of the Germanium, which can also be seen in a doping profile (Fig. 3).

To fully grasp the impact of Germanium on the device operation, it is important

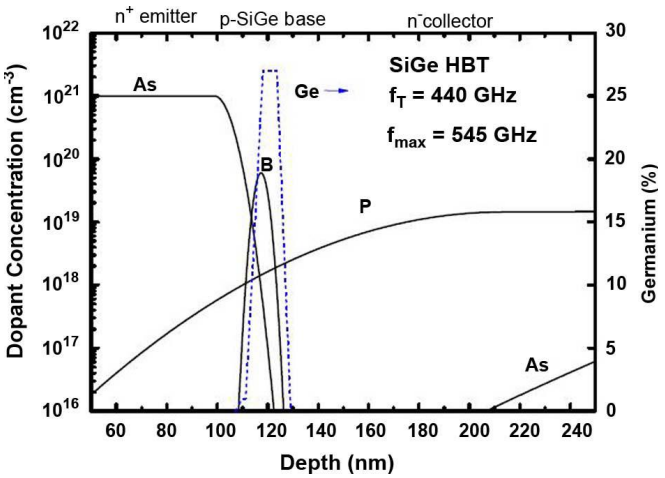

Figure 3: Doping profile of a SiGe HBT (after [14]).

to look at its impact on key figures of merit (compared to a traditional Si BJT). The first parameter to consider is the Beta (β) of the device which denotes the current gain of the transistor (collector current divided by the base current). The β of the device improves based on the amount of band-bending due the Germanium right at the emitter-base (EB) junction of the device.

$$\beta \propto e^{\Delta \mathrm{Eg}(0)/(\mathrm{kT})} \tag{1}$$

Where k is the Boltzmann factor and T is the temperature. For a value of 20% Ge at the EB junction, the DC gain improves immediately by a factor of 6 at room temperature. Clearly an encouraging result for circuit designers — amplifiers with more gain allow for greater design flexibility and better performance. An interesting result of the equation is that the effect of Germanium also gets amplified at lower temperatures.

Another important relationship is how Germanium impacts the maximum oscillation frequency of the device (f_T) and the maximum unity-gain power frequency (f_{MAX}). It is first important to look at the equation for f_T.

$$f_T = \frac{1}{2\pi}\left\{\frac{kT}{qIc}(C_{te}+C_{tc})+\tau_b+\tau_e+\frac{W_{CB}}{2V_{sat}}+r_cC_{tc}\right\}^{-1} \tag{2}$$

The equation is primarily dominated by capacitances and resistances (parasitics) in addition to transit times τ_b and τ_e. Improvements in lithography and scaling naturally lessen the impact of parasitics on f_T and the limitations are instead the transit times. In many cases, it is appropriate to approximate the equation to the following form [13]:

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{3}$$

In this form, it is clear to see that the limiting factor is τ_{ec} — the total delay time from the emitter to the collector, which defines the switching speed of the transistor [13]. For standard *npn* devices, one of most limiting transit times will be the minority carrier transit time in the base: τ_b. This is where the Ge grading will come into play. The steeper the Ge grading in the base, the greater the improvement in the base transit time. This relationship can be seen in the following equation:

$$\tau_b \propto \frac{kT}{\Delta Eg, Ge(grade)} \tag{4}$$

The reduction in the base transit time, τ_b, allows electrons to travel much more quickly through the base region of the device. Improving the f_T of the device will greatly improve the operating speed.

Improved current gain (β) allows processing engineers to make a further improvement to the device. Some of the gain can essentially be given back by doping the base region more heavily. At its core, current gain is a function of the emitter doping divided by the base doping. Increasing the base doping causes the base resistance to drop. This improves the f_{MAX} of the device through the following relationship:

$$f_{MAX} \simeq \sqrt{\frac{f_T}{8\pi\ r_b\ C_{CB}}} \tag{5}$$

Having high f_{MAX} and f_T is critical to devices designed for high-quality RF and analog circuitry. It is the bandgap engineering of the Ge within the SiGe HBT which gives it performance capabilities that rival that of some III-V technologies.

Now that a brief background of SiGe HBTs has been provided, the next focus in this work will be on the basics of radiation effects. This discussion will include an in-depth look at various causes of radiation and the radiation environment. Afterwards, the discussion will shift toward the contributions of the author.

CHAPTER III

THE RADIATION ENVIRONMENT

The Radiation Environment is dynamic and can be influenced by a large number of factors — some of which, little is known about. Highly energized particles continually bombard the Earth's atmosphere and are comprised of electrons, proton, neutrons, heavy ions, gamma rays and x-rays. A significant portion of these particles actually originate from the Sun (see Fig. 4). Solar events, such as solar flares and Coronal Mass Ejections (CMEs), occur hundreds of times a year and, in the process, release protons, electrons, and heavy ions that are accelerated towards the Earth near the speed of light [6]. These events are cyclical in nature and follow an 11-year cycle of the Sun, one 7-year period of solar maximum followed by a 4-year period of solar minimum [53]. Protons and electrons can become trapped in the Earth's magnetosphere and form what is known as the Van Allen Belts. These bands of radiation can pose significant hardness assurance concerns for satellites orbiting the Earth as they pass through the Van Allen belts many times a day and are exposed to large amounts of total ionizing dose (TID).

Outside of solar events, the most significant contribution to the radiation environment in space is Galactic Cosmic Rays (GCRs). GCRs are extraordinarily high-energized particles that exist at low fluxes in space. These particles do not originate from the Sun and are rather believed to originate outside of our galaxy. Theories to explain the existence of these particles vary. However, most people believe these particles are a result of two contributing factors: 1) the death of stars resulting in a supernova and 2) the beginning of the universe and the Big Bang. GCRs, although low in number, have a significant impact on electronic design for space radiation.

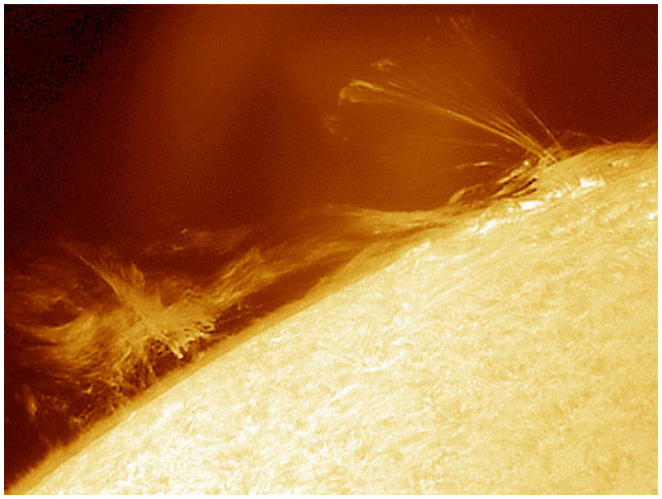

Figure 4: NASA — a solar prominence which materializes over the surface of the Sun, this prominence may erupt — emitting large quantities of solar debris (after [48]).

Particles at extremely high energies cannot easily be stopped by traditional shielding techniques and can cause upsets to occur in electronics. GCRs also cause a serious problem for terrestrial electronics as well. When colliding into the Earth's atmosphere, GCRs create atmospheric neutrons, which can in turn, damage sensitive electronics.

A lot of consideration goes into designing electronics for radiation. The environment can vary drastically depending on whether the electronics are being operated terrestrially, at a given orbit around the Earth, or at some other location — such as another planet or moon. In addition, engineers must be mindful that those environments are quite dynamic and significant design margin must be built in. Many space missions can involve multi-million dollar projects, which must succeed under any circumstance. Even with strict requirements, though, significant care must be taken in order to weigh the trade-offs of designing parts that are overly hardened to radiation. Sometimes minimal damage or risk is acceptable when over-design results in significant increases to size, weight, and power (SWaP) of the electronics.

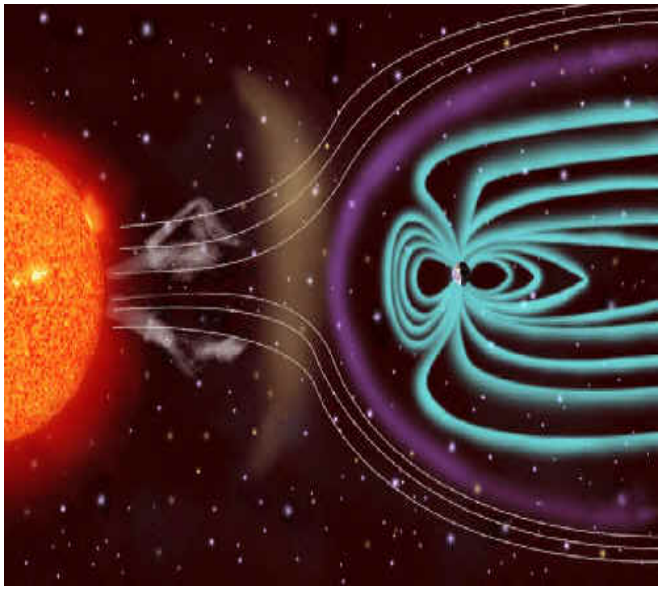

Figure 5: Illustration of particles emitted from the Sun interacting with the Earth's magnetosphere (after [16]).

3.1 Solar Events and Cycles

As mentioned earlier, the Sun roughly follows an 11-year solar cycle. Seven years of this is spent at solar maximum — seeing roughly three coronal mass ejections (CMEs) a day, while four years are spent at solar minimum — seeing roughly one CME every five days (see Fig. 4 to view a solar prominence, the precursor to a CME) [25]. The frequency of coronal mass ejections (CMEs) has an impact on both the Earth's magnetosphere and also the flux of galactic cosmic rays (GCRs) observed near the Earth. At periods of solar minimum the flux of GCRs is at a maximum as the magnetic polarity of the Sun modulates the resulting GCR flux density [7]. During periods of solar maximum, particles from the Sun are frequently being emitted in massive quantities toward the Earth. The effect of particles colliding into the Earth's magnetosphere can be seen, on Earth, as the aurora borealis — also known as the northern lights. The particles effectively compress the Earth's magnetosphere facing towards the Earth and create solar winds (trapped particles) which may be seen at various latitudes in the night sky. An illustration depicting this effect may be seen

Figure 6: The Northern Lights — caused by trapped particles in the Earth's magnetosphere (after [43]).

in Fig. 5 and an image of the aurora borealis, as seen from Quebec, may be seen in Fig. 6.

3.2 Van Allen Belts

Coronal mass ejections effectively charge the Earth's magnetosphere with a large influx of electrons and protons, creating bands of highly energized particles: the Van Allen Belts. There are normally two primary Van Allen Belts (see Fig. 7); however during highly active solar periods (solar storms), the bands can connect together, posing a significant risk to a number of satellite systems. The Earth's geomagnetic field is approximately dipolar up to an altitude of roughly 4-5 Earth radii [53]. As charged particle trapping coincides with the Earth's geomagnetic field lines, this confines the Van Allen Belts to within approximately 30,000 km of the Earth's surface.

3.3 Orbit Dependency

As Geo-Synchronous Orbit (GEO) occurs at altitudes of 35,786 km, the Van Allen Belts are not a primary concern for satellites orbiting at GEO. They are however, major concerns for satellites operating at Mid-Earth Orbit (MEO) or Highly Elliptical

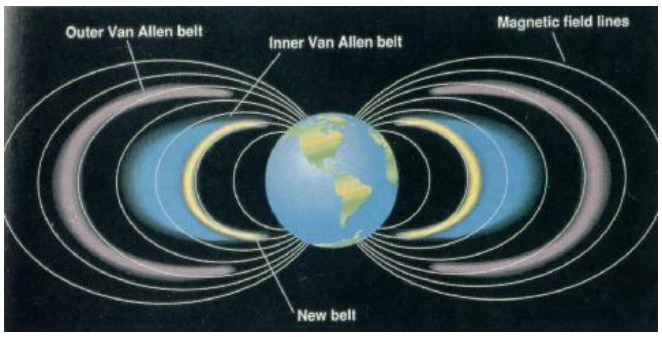

Figure 7: The Van Allen Belts (after [5]).

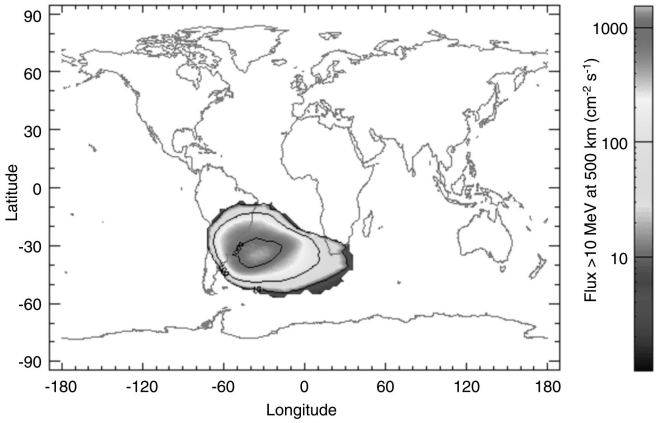

Figure 8: The South Atlantic Anomaly (after [2]).

Orbit (HEO) [6]. At these orbits, the satellites will regularly pass through the Van Allen Belts and, consequently, high amounts of ionizing radiation. These satellites must be robust to high fluences of highly energized protons — whereas other satellites (such as those at GEO), may have looser requirements for total ionizing dose damage.

3.4 South Atlantic Anomaly

Satellites that operate at Low Earth Orbit (LEO), at altitudes of 160 km to 200 km, do not usually experience high fluences of protons. However, there is one region, known as the South Atlantic Anomaly (SAA), where this is not the case. The SAA is created by the offset and tilt of the magnetic dipole of the Earth with respect to the Earths axis of rotation [15]. This region may be seen in Fig. 8. Although confined to a relatively small space, the SAA will cause mission interruptions for nearly all satellites that pass through it [6].

3.5 Mitigation Approaches

3.5.1 Radiation Hardening by Design

Radiation hardening by design (RHBD) involves using specialized layout techniques in order to account for radiation induced damage. One example is the use of triple modular redundancy (TMR), which involves using three instances of a sensitive circuit or block. The redundancy accounts for upsets due to single event effects in any one circuit while allowing a majority voting scheme to allow for consistent operation even through such an event. Other approaches involve the creation of "edgeless" transistors [29]. These transistors have a more robust TID response; however, this improvement comes at a cost to device area (larger layout footprints).

3.5.2 Radiation Hardening by Process

Radiation hardening by process (RHBP) involves hardening at the processing level. This can be as simple as reducing oxide thicknesses or completely revamping device

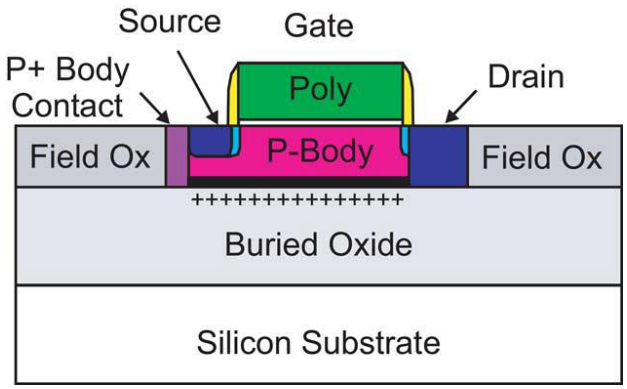

Figure 9: Cross section of a BUSFET (after [46]). The shallow source implant prevents a back channel from forming at the BOX.

structures. One such example is a Body Under Source Field Effect Transistor (BUSFET shown in Fig. 9) [46]. This transistor is intentionally engineered such that the source implant does not fully extend to the buried "BOX" oxide of a Silicon-on-insulator (SOI) CMOS transistor. This device modification prevents a "back-channel" from forming in the transistor as a result of TID damage. In a sense, the BUSFET prevents a parasitic back gate from conducting current — which can be an issue in some CMOS devices as the BOX is a very thick oxide and trapped carriers cannot easily tunnel out.

3.5.3 Shielding

Most space missions involve radiation shielding of some sort on board. Although shielding will not be able to stop all highly energized GCRs, it is quite effective at preventing a substantial amount of total ionizing dose damage. As such, electronics are normally contained within a "warm box" where parts are shielded and kept at an ambient temperature to ensure proper operation. However, warm boxes are bulky and limit where electronics can be placed on board a spacecraft. Nonetheless, studies have proven that even modest amounts of Aluminum shielding can drastically reduce the amount of TID for a given mission lifetime. For example, Bhat in [8], showed that 7 mm of Al results in less than 1 krad of dose over 500 days, whereas the

accumulated dose with 2 mm of Al results in about 60 krad over the same time period. This is a substantial difference and shows how the addition of shielding can be used to meet mission specifications for radiation without having to compromise designs with radiation hardening by design or process techniques.

CHAPTER IV

INTRODUCTION TO RADIATION EFFECTS

There are three primary types of radiation damage that concern radiation effects engineers: total ionizing dose (TID) damage, single event effects (SEE), and displacement damage (DD). The focus of this work is on total ionizing dose effects; however, a brief background is still fundamental to understanding the scope of this work. The two most critical types of radiation damage, at present, are total ionizing dose effects and single event effects. Displacement damage can still result from radiation; however, the benefits of scaling and improved fabrication techniques make it often an afterthought to other radiation concerns.

4.1 Total Ionizing Dose

Total ionizing dose (TID) damage results from charge accumulation at sensitive interfaces in a device (primarily at Si-SiO_2 interfaces). Charge accumulation can adversely affect the operation of the device. In the case of an n-type metal oxide semiconductor field effect transistor (MOSFET), charge accumulation at the sensitive gate oxide (where the channel forms) will result in a shift to the threshold voltage of the device. The charge accumulation is a result of chemical bonds being broken at the Si-SiO_2 interface. The following process is taking place: 1) a charged particle (with energy exceeding than the bandgap of the semiconductor material) passes through a device creating large quantities of electron-hole pairs (EHP). Electron-hole pairs normally recombine very quickly; however, at times (often being aided by drift fields in the device), free carriers can reach sensitive interfaces. There is an Oxygen deficiency at the Si-SiO_2 interface that results in a number of strained Si-Si bonds — instead of normal Si-O-Si bonds [36]. A hole encountering such a bond may break the bond

(because it is weakly bound) and then recombine with one of the bonding electrons. This process is known as hole trapping. The resulting positively charged structure relaxes to the E' (E prime) configuration with one of the Si atoms retaining the remaining electron from the broken bond and the positive charge residing on the other "trivalent" Si atom [36]. These trapped holes are not necessarily permanent and may dissipate with time — annealing processes can result in the removal of the trapped holes as well.

4.2 Single Event Effects

Single event effects (SEE) come into play in a number of different ways. The term SEE is a catch-all term used in order to describe a number of effects such as: single event latchup (SEL), single event transients (SET), single event gate rupture (SEGR), single event functional interrupt (SEFI), and more. Single event effects result from a single, incident particle which imparts energy into the device. The generated electron-hole pairs induce a photocurrent which in turn may damage the device or have adverse effects on the circuit application for the device. In the extreme case a SEE may induce a bit flip and put a digital circuit in an undesirable and possibly unrecoverable state of operation. Further, in the case of single event latchup (SEL), a parasitic feedback channel is formed which shorts V_{DD} to GND causing an overcurrent condition, which may in turn completely destroy metal traces in an attempt to dissipate the energy.

4.3 Displacement Damage

Displacement damage (DD) is a result of radiation physically damaging the lattice of the semiconductor device. Dopant deactivation can result from DD; however, most lattice damage seen, is quickly recovered. Displacement damage is primarily a concern from particles with a lot of mass such as protons and heavy ions. Electrons will rarely cause DD. Displacement damage is very rarely the limiting radiation response for a given technology. As such, more emphasis is given on TID and SEE effects.

CHAPTER V

TOTAL IONIZING DOSE EFFECTS IN A 180 NM BICMOS TECHNOLOGY

The results in section 5.2: "CMOS Radiation Response," have been previously reported in the following article:

"Fleetwood, Z.E.; Kenyon, E.W.; Lourenco, N.E.; Jain, S.; En Xia Zhang; England, T.D.; Cressler, J.D.; Schrimpf, R.D.; Fleetwood, D.M., "Advanced SiGe BiCMOS Technology for Multi-Mrad Electronic Systems," Device and Materials Reliability, IEEE Transactions on , vol.14, no.3, pp.844,848, Sept. 2014"

It is important to note that the data in Section 5.2 was a result of experiments conducted by Eleazar Kenyon. In addition, the plots in the section were also a result of his endeavors. The resulting explanation and interpretation of the results involved a joint effort between the author of this thesis (Fleetwood) and Kenyon. The follow-up simulation work, reported in Section 5.3, is not a part of the original article and is an addition of this author and thesis document.

5.1 Introduction

Total ionizing dose (TID) damage was first identified as an issue for MOSFETs by Hughes and Giroux in 1964 [30]. Ever since that time, significant work has gone

into the mitigation of TID effects in MOS devices. In a MOSFET, TID degradation is marked by shifts in key device parameters such as threshold voltage (V_{TH}) and off-state leakage current. Shifts in V_{TH} cause circuit bias points to shift — this can consequently cause the circuit to no longer function. Off-state leakage current increases (in general) with increasing levels of TID. Eventually these devices, even when biased in the off-state, leak so much current that they are permanently turned on (ruining any possible circuit functionality). The basic mechanisms underlying TID damage in MOSFETs is well-documented in the field and further background may be found in [36].

The focus of this thesis on CMOS TID effects will be on the 180nm CMOS node, specifically in Jazz Semiconductor's 180 nm SiGe BiCMOS platform (SBC18-HXL, with 150 GHz peak f_T). Minimum length CMOS devices (nFETs and pFETs at 180 nm channel length) were irradiated at TID testing facilities at Vanderbilt University and the University of California Davis.

The experiments at Vanderbilt University were conducted using a 10 keV X-ray source (ARACOR) at a dose rate of 31.25 krad(SiO_2)/min. CMOS devices with varying widths were irradiated up to a accumulated dose of 6 Mrad(SiO_2) and were measured at intermediate dose points along the way (immediately after irradiation to limit annealing effects). Another set of nFETs were irradiated at UC Davis using a 63-MeV proton source (described in [10]) at a dose rate of 1 krad(SiO_2)/s. These nFETs were irradiated up to a total dose of 3 Mrad(SiO_2) and were also measured at intermediate dose points immediately following irradiation. For both experiments, all FETs were biased with maximum rated gate voltage applied — which is, for these devices, the worst case bias condition.

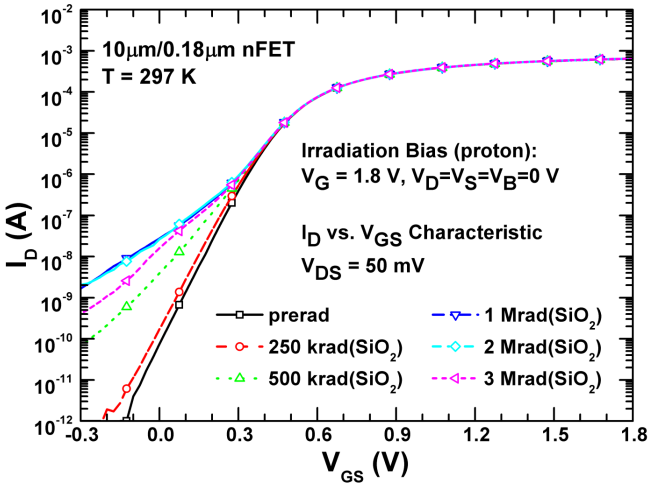

Figure 10: Proton-induced degradation of nFET subthreshold characteristics at low V_{DS}.

5.2 CMOS Radiation Response [24]

Fig. 10 shows the total dose response of the drain current of a wide (10 μm/0.18 μm) nFET at low V_{DS} as the gate source voltage is swept. The X-ray and proton responses of all FETs were similar, with the proton exposure resulting in slightly greater degradation. The lack of threshold voltage shift (see Fig. 11) for large devices, even at these very high doses, indicates that there is very little net charge trapping in the gate oxide. The observed degradation is therefore caused primarily by charge in the shallow trench isolation (STI) oxide and its interface with the channel region. For comparison, the response of an identically-sized nFET from a comparable 180 nm SiGe BiCMOS platform (published in [34]) is shown in Fig. 12. The change in off-state leakage current for the given technology can also be seen in Fig. 13.

The two devices show significantly different degradation characteristics, with the leakage of the nFET from the present technology showing a much stronger V_{GS} dependence. The previously published device response also shows a more classical off-state leakage characteristic independent of V_{GS}, consistent with charge trapping deep along the STI edge, which creates a parasitic inversion channel far removed from the upper

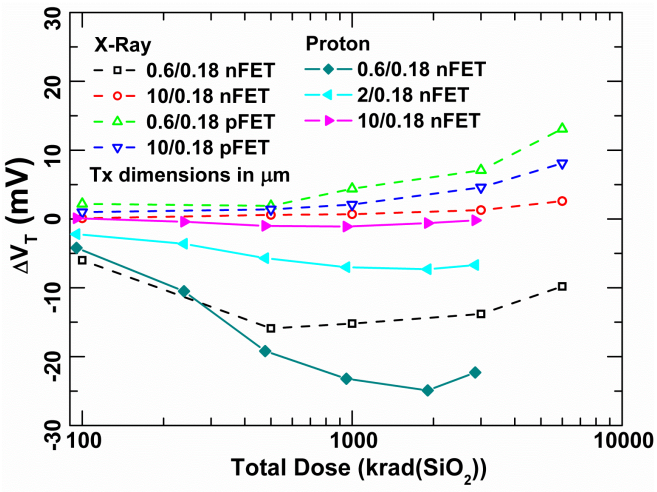

Figure 11: Radiation-induced threshold voltage shifts in CMOS transistors.

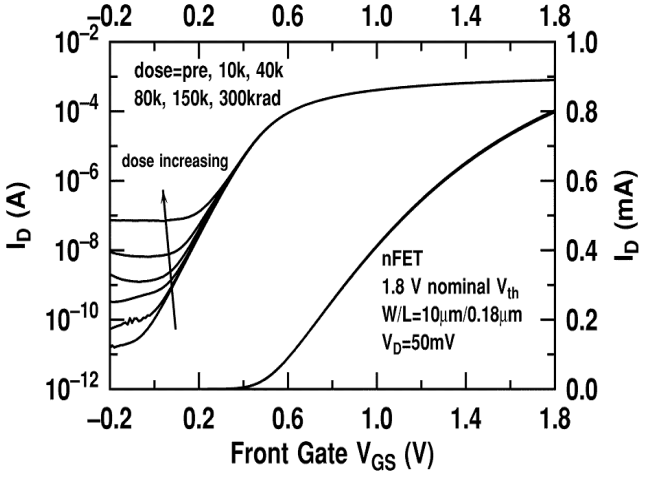

Figure 12: Previously-published TID response of nFETs implemented in a different 180 nm SiGe BiCMOS platform (after [34])

STI corner, inducing a shunt leakage path between source and drain. Previous studies have also shown that STI corner leakage causes a sub-threshold "hump" in the I_D-V_{GS} characteristics, while "deep" STI leakage results in a flat, constant leakage current [37, 50]. In [50], a strong dependence of the leakage characteristics on the spatial distribution of the charge in the STI and at the STI/bulk Si interface was reported, potentially offering insight into the differences between the two technologies.

The factors responsible for the different responses of the nFETs from two different SiGe BiCMOS technologies with comparable lithography (180 nm) and performance may include both doping and structural differences. Higher doping concentrations reduce the susceptibility of the well-to-STI edge inversion, and as a triple well process, the present technology will have a uniquely defined doping profile. The pwells used for the nFET devices are intended to provide device isolation and individual control over body potentials, but the doping control also provides a benefit to the TID response.

The physical structure of the STI dictates the electric field contours and gate-STI interactions and will also dictate the TID response. One known difference between the two BiCMOS platforms is the shape of the STI oxide. In the present BiCMOS technology, the STI exhibits both a slightly recessed top surface (the gate dips down as it crosses the STI channel edge) and a retrograded, or inward-sloped, shallow trench edge. Other STI profiles like those found in [34] feature a nearly vertical profile. This difference in STI structure is likely to influence the mechanical stress on the STI oxide, which may affect charge trapping and TID response [42].

Figs. 14-15 show the leakage characteristics for a narrow and wide nFET, respectively, at high V_{DS}, and Fig. 11 shows the threshold response (extracted by extrapolating to zero from the linear region of the I_D-V_{GS} curve) of all irradiated CMOS devices. Additionally, Fig. 16 shows the X-ray response of a narrow nFET, which, contrasted with Fig. 14 highlights the two major differences between the proton and X-ray exposures. The first difference is the increased degradation seen in the proton

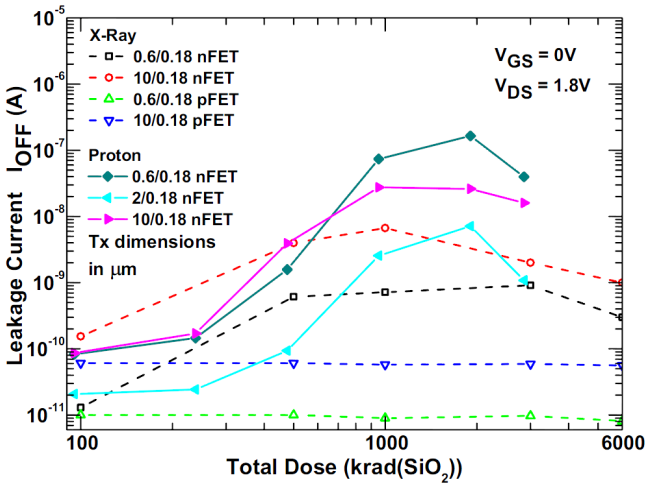

Figure 13: Radiation-induced off-state leakage current at high V_{DS}.

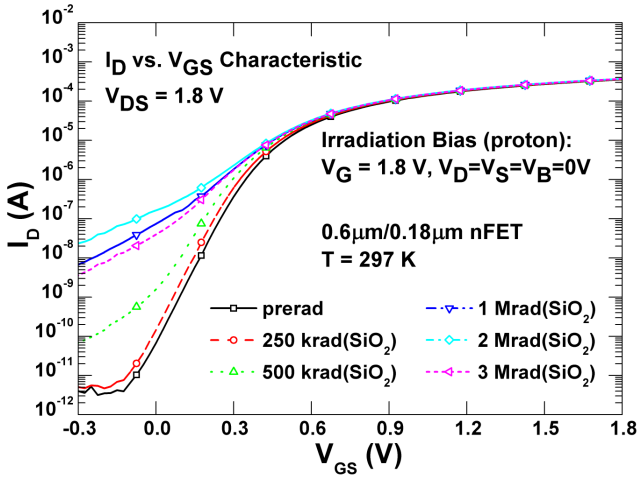

Figure 14: Proton induced degradation in narrow nFET at high V_{DS}=1.8 V.

exposure, and the second is the "turn-around" effect that is seen in both exposures. Unlike X-ray exposure, the proton exposure results in noticeable lattice damage which leads to the slightly increased degradation [47]. This result is not unexpected and as such will not be discussed further and more attention and analysis will instead be put on the other difference.

This other difference, a key feature of this device's TID response, is the apparent "turn-around" effect seen in both irradiations (around 2 Mrad in the proton case and 1 Mrad for the X-ray case). This effect is marked by an initial increase in the

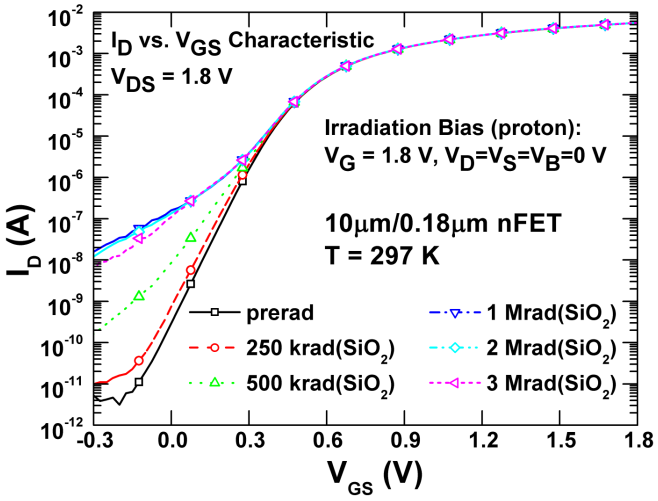

Figure 15: Proton induced degradation in wide nFET for V_{GS}=1.8 V.

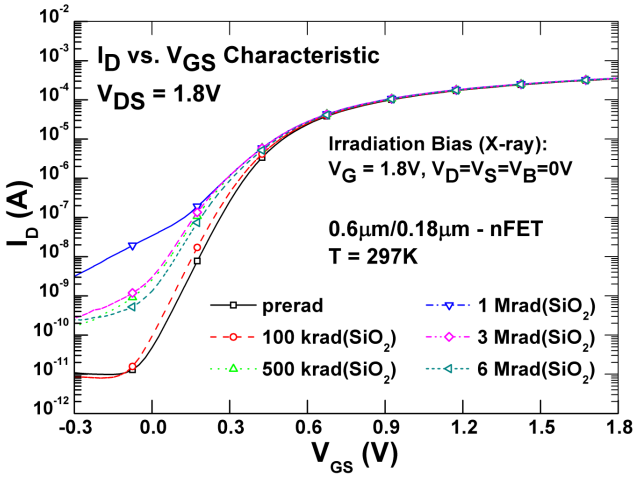

Figure 16: X-ray induced degradation in narrow nFET at V_{DS}=1.8 V.

degradation up to a certain "saturation" point and the subsequent reversal of the degradation past this point. This "turn-around" effect is observed at different levels of total dose due to the sources used. The difference in dose rates and the particles themselves will contribute to a difference in the charge yield in the devices and thus a varying TID response. The device irradiated with the low energy X-rays (10-keV) may also experience some level of "dose enhancement" [47]. This effect is seen in thin oxides irradiated by low-energy X-rays and is marked by an increased oxide dose. This "dose enhancement" along with the source differences causes the apparent acceleration of the "turn-around" effect in the X-ray irradiated device.

The STI leakage effects cause an apparent threshold voltage shift in the small devices, a result of radiation-induced narrow channel effects, as described in [20], since the edge structure and hence magnitude of the leakage current is roughly the same regardless of transistor width. The previously mentioned "saturation" or "turn-around" effect observed in the nFETs at high dose levels results from charge building up at the oxide/Si interfaces. The radiation-induced interface charges are negative for a p-substrate (nFET) and positive for an n-type substrate or well (pFET) and form at a different rate than bulk STI oxide charges, which are responsible for the degradation at low values of total dose. In the pFETs, the positive interface charge reinforces the effect of the positive bulk STI charge, resulting in a slight increase in threshold voltage, the only observed degradation seen in the pFETs at high total dose. In the nFETs, however, the interface charges are negative and counteract the positive bulk oxide charges at high total dose values [26], improving the total dose tolerance of the nFETs under these irradiation conditions. An additional buildup of interface traps at lower dose rates would decrease the leakage further [22].

Other circuit-relevant FET parameters, such as transconductance and on-state current, did not show any appreciable degradation or shift above threshold even up to 6 Mrad(SiO_2) dose, and the output characteristics of a wide nFET and pFET (Fig.

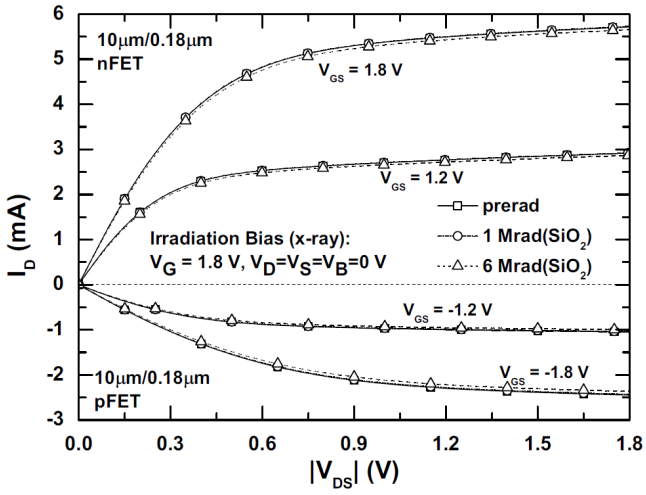

Figure 17: Output characteristics of wide nFET and pFET after X-ray exposure

17) also show very little degradation up to 6 Mrad(SiO_2), again a favorable result.

5.3 CMOS TCAD Modeling

In order to investigate the "turn-around" effect seen in the 180 nm Jazz nFETs, 3D NanoTCAD models were created. NanoTCAD is part of a software suite designed by CFDRC that can be used to investigate radiation effects. Further information on NanoTCAD can be found at [1].

These models tried to attack first a basic question: "How does the STI profile affect TID response?" It is known that Jazz's 180 nm process has an angled STI edge whereas comparable technologies, such as IBM's 180 nm technology, has an STI profile with an extremely anisotropic (vertical) edge. The difference in these two concepts in depicted in Fig. 18.

This difference in STI structure is likely to influence the mechanical stress on the STI oxide, which may affect charge trapping and TID response [42]. In addition, the STI profile for the Jazz process has a recessed gate oxide. This means that the gate oxide physically dips down (looking at a 2D cross-section) to connect to the STI oxide. The oxide corner, where the gate oxide meets the STI, greatly dictates the resulting electric field across the oxides when a gate potential is applied [50]. This electrical

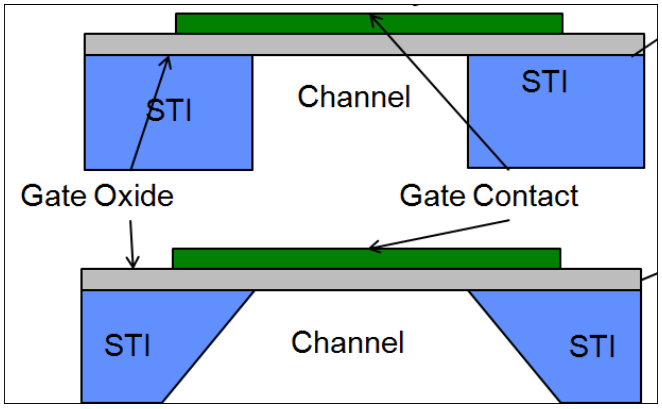

Figure 18: Depiction of an STI sidewall with a vertical profile (top) and a slanted profile (bottom).

field, consequently, will then affect the charge trapping mechanisms seen along the STI sidewall. Modeling work, conducted by Turowski *et al.*, has shown that charge trapping will not occur right at the corner of the STI but it will rather occur further down the STI sidewall. This buildup of charge causes a parasitic conduction path between the source and drain of an nFET. The parasitic conduction path, like charge buildup at the gate oxide, will result in increased leakage current and shifts to the threshold voltage of the device. Since gate oxides are thin in modern MOSFETs (gate oxides $\leq$ 7 nm), it is this parasitic conduction that is a primary cause for concern in modern FETs. The oxides at the STI are substantial in size (possibly hundreds of nm thick) and tunneling of trapped carriers is much less likely to occur than in thin gate oxides.

Three different 3D 180 nm nFET structures were created in order to analyze the effects of STI angle on the TID response (see Fig. 19). The initial goal was to investigate whether or not the STI angle had an effect on the TID response. The first model was a control device with a completely vertical STI sidewall — like that of IBM's comparable technology, the second had a sidewall with a slight angle to the STI, and the third device had an STI sidewall with a drastic angle — like that of Jazz's technology. Each profile was modeled to contain a sheet charge along the

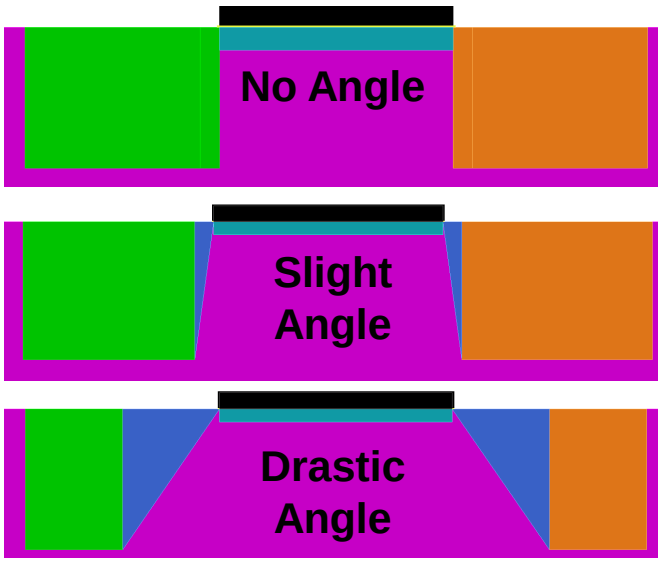

Figure 19: Sideview of 3D nFET models. Top model has a vertical STI sidewall, the middle model has a slightly slanted STI sidewall, and the bottom model has a larger, more gradual slant to the STI sidewall.

sidewall and the effects of the sheet charge were analyzed. The charge along the sidewall is an investigation of whether or not an equivalent sheet charge will cause the resulting transfer characteristics of the device to shift. Another approach would be to remove the charge away from the STI corner and then apply a non-uniform sheet charge (as described by [50]).

The transfer characteristics for all three models are plotted in Fig. 20-22. The figures show that the overall leakage current (from TID) slightly decrease due to the slant of the STI sidewall. However, there is not a drastic shift in the TID response as was expected (comparing the Jazz results to the STI), there is not a leveling off of leakage current in the case of the vertical sidewall (IBM). There is also no turn-around effect seen in the Jazz case; however, this is not at all surprising as a sheet charge was applied to the Si-SiO_2 interface of the STI sidewall. There was no mechanism in place to describe how the equivalent sheet charge should change at different levels of total dose. Design improvements, some of which are currently being investigated, are discussed in the "future work" section of the thesis conclusion.

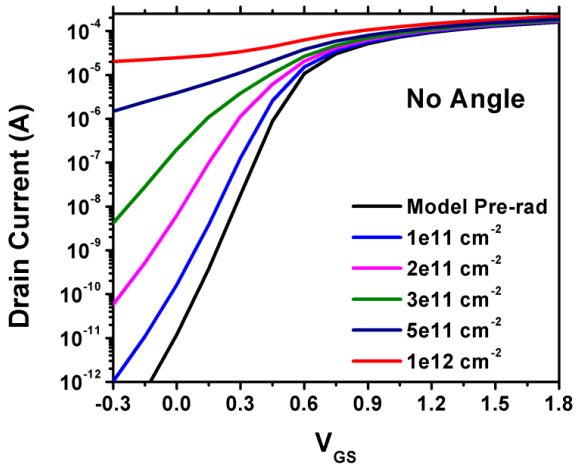

Figure 20: Transfer characteristics of the model with the a vertical STI sidewall.

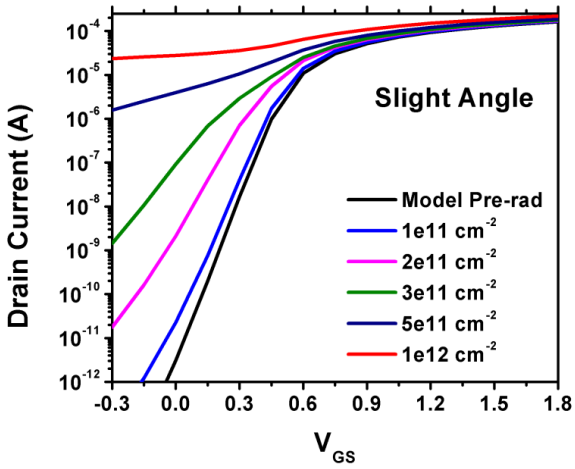

Figure 21: Transfer characteristics of the model with the a slightly slanted STI sidewall.

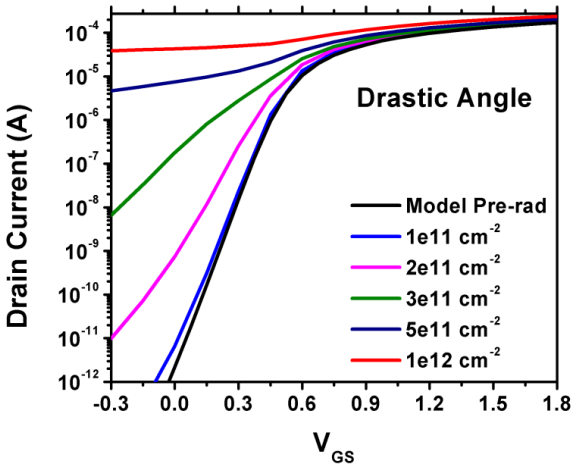

Figure 22: Transfer characteristics of the model with the a larger slant to the STI sidewall.

CHAPTER VI

GENERATIONAL STUDY OF DOSE RATE EFFECTS IN SILICON-GERMANIUM HBTS [23]

The results in Chapter 6: "Generational Study of Dose Rate Effects in Silicon-Germanium HBTs," is slated to be published in the following article:

"Fleetwood, Z.E.; Cardoso, A.S.; Song, I.; Wilcox, E.; Lourenco, N.E.; Phillips, S.D.; Arora, R.; Paki-Amouzou, P.; Cressler, J.D., "Evaluation of Enhanced Low Dose Rate Sensitivity in Fourth-Generation SiGe HBTs," Nuclear Science, IEEE Transactions on , vol.PP, no.99, pp.1,8"

It is important to note that the low dose rate and high dose rate irradiation experiments were conducted by Edward Wilcox at NASA Goddard. The data analysis, plotting, and interpretation of the results were contributed by the author of this thesis.

6.1 Introduction

Radiation testing facilities permit electronics to be rapidly analyzed for radiation hardness assurance to total ionizing dose (TID) and single event effects (SEE). Most TID studies involve irradiation at dose rates > 50 rad(SiO_2)/s, which is much higher than would be expected in space or many extreme environments [45]. Using higher

dose rates for testing saves valuable time and resources. Some integrated circuits (ICs) require low dose rate (LDR) ≤ 10 mrad(SiO_2)/s radiation testing to ensure that latent dose-rate dependent degradation mechanisms are not masked by high dose rate (HDR) irradiation. Most ICs show good agreement between high and low dose rate accumulated TID damage, and as such, radiation effects engineers are justified in their use of high dose rate sources. Unfortunately, some ICs are susceptible to enhanced low dose rate sensitivity (ELDRS). Simply stated, an ELDRS-sensitive device (normally a bipolar transistor) appears to experience significantly more degradation at a LDR than the same device experiences at the HDR, for an equivalent total dose. Numerous studies have been conducted in regards to this occurrence. The community consensus is that the devices are not experiencing increased degradation at the low dose rate but are rather experiencing a suppression of damage in the higher dose rate irradiation [21, 28, 41]. This scenario is clearly a major concern for ICs intended for extreme environments such as space, since the radiation tolerance of susceptible devices can be drastically overestimated, potentially resulting in circuit failure much sooner than expected.

Over the past twenty years, Silicon-Germanium Heterojunction Bipolar Transistors (SiGe HBTs) have emerged as a serious contender for many analog and RF applications. However, very few studies have been conducted to determine whether dose rate has a major impact on degradation mechanisms in this relatively new type of bipolar device [11, 51, 49]. It is widely believed that the underlying reasons behind the TID robustness of the SiGe HBT (vertical transport with thin spacer oxides) also lead to a robustness to ELDRS effects [14]; however, no prior study has thoroughly investigated the topic.

No state-of-the-art SiGe HBT (4^{th}-generation with peak $f_T > 300$ GHz) has undergone ELDRS hardness assurance testing. Discernible changes in fabrication have been made for 4^{th}-generation SiGe HBTs in order to improve performance. Those

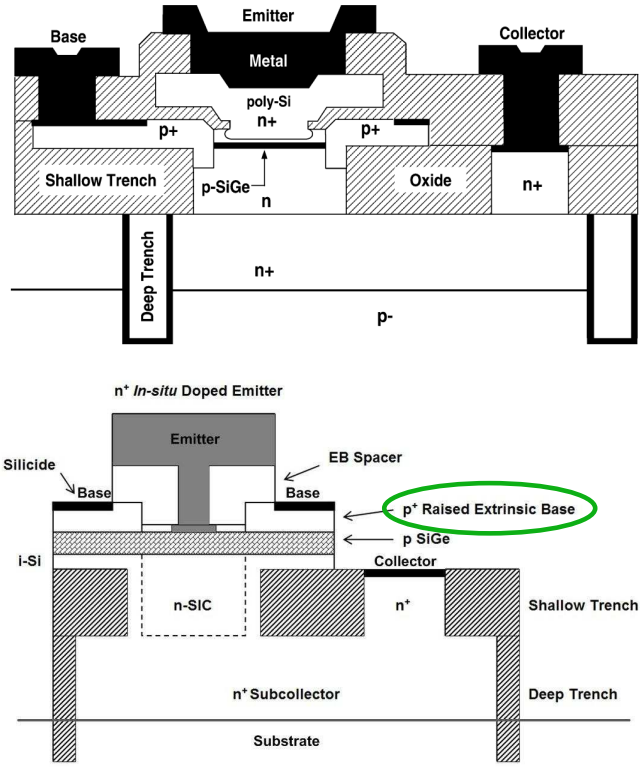

Figure 23: Schematic cross-sections of a 1st-generation SiGe HBT (top) [12] and a 4th-generation SiGe HBT (bottom) (after [31]). A key difference (circled on the bottom figure) is the raised extrinsic base in the newer device structure.

changes include: thinner base and collector profiles, changes to vertical and lateral profiles, and an improved device structure that minimize parasitics associated with the collector-base (CB) junction [35]. In addition, the technology uses rotated wafers, novel emitter contact technology, and reduced thermal cycles [35]. A 2D cross-section of this new structure is compared to a 1st-generation device in Fig. 23. Key parameter changes across generations, along with the corresponding lithography node, is also provided in Table. 1. It is uncertain whether changes in fabrication will lead to changes in damage mechanisms at low dose rates. SiGe HBTs are well known for having an impressive inherent tolerance to TID damage (multi-Mrad) — making them prime candidates for many space applications [14]. Any deviation from this trend of TID robustness would be extremely detrimental to their contention for use in extreme environments.

Table 1: Parameter Scaling by Generation

Parameter	**Units**	**1st**	**2nd**	**3rd**	**4th**
Lith Node	nm	500	180	130	90
WE,eff	μm	0.42	0.18	0.12	0.09
Peak β	-	100	200	400	550
BV_{CEO}	V	3.3	2.5	1.7	1.4
BV_{CBO}	V	10.5	7.5	5.5	5
Peak f_T	GHz	47	120	207	300
Peak f_{MAX}	GHz	65	100	285	350

The aim of the present investigation is to analyze the effects of dose rate on state-of-the-art, 4th-generation, SiGe HBTs at both the device and circuit level, and determine whether or not the newest SiGe BiCMOS (Bipolar and Complementary Metal Oxide Semiconductor) technologies are susceptible to deleterious dose rate effects such as ELDRS. The data presented in this paper, to the authors' knowledge, contains the first circuit study of ELDRS in SiGe HBTs. In addition, this work provides the first investigation of low dose rate effects in 4th-generation SiGe HBTs. Measurements from previous devices generations (1st and 3rd) have also been conducted to expand the analysis across multiple device generations. A discussion is provided that includes past findings on 2nd-generation SiGe HBTs [27] that only not only covers all major technology generations but also provides insight into the future of low dose rate effects for the SiGe HBT.

6.2 ELDRS

Enhanced low dose rate sensitivity (ELDRS) was first identified as a hardware assurance concern for bipolar devices by Enlow *et al.* in 1991 [17]. Since the discovery of the effect, many studies have been conducted to identify ELDRS sensitive parts and to understand the phenomenon. Initial findings by Johnston *et al.* showed that the

relative damage of ELDRS parts could be as much as 6 times larger than parts irradiated at higher dose rates of ≥ 50 rad(SiO_2)/s [33]. The ratio of relative damage for ELDRS parts is known as the "enhancement factor" (EF). This term describes how much more sensitive the part is to damage at low dose rates when compared to higher dose rate damage [40, 33]. ELDRS is most commonly a *pnp* device issue; however, *npn* devices may also experience ELDRS. A compendium of ELDRS sensitive parts through 2008 may be found in [39].

ELDRS is a "true" dose rate effect (TDRE) and is different from time dependent effects (TDE) traditionally seen in metal oxide semiconductor (MOS) devices irradiated at low dose rates. When comparing circuits irradiated at high and low dose rates, time dependent effects are identified by following a high dose rate irradiation with a room temperature anneal up to the (longer) irradiation time for the low dose rate experiment. In the case of a TDE, the degradation between the low dose rate irradiation and the high dose rate irradiation with the subsequent anneal will be very similar. However, in the case of a TDRE, a disparity in the degradation between the high and low dose rate irradiations will exist even when accounting for annealing [41]. Due to the long time period associated with low dose rate testing, it is not always feasible to increase testing time to account for annealing effects, and because of this, the enhancement factor used in ELDRS testing is based off of measurements taken immediately after irradiation for both the high and low dose rate experiments. The enhancement factor used to compare high and low dose rate degradation will include time dependent effects in addition to possible true dose rate effects such as ELDRS [38]. However, previous studies have shown the calculation of the enhancement factor to be an effective method to determine ELDRS sensitive parts [38].

Enhanced low dose rate sensitivity is a major concern for oxides with high defect densities [22]. These defects can be introduced during oxide growth or may be introduced during passivation in the form of hydrogen as a contaminant [22, 41].The

amount of hydrogen introduced to the device and the subsequent interactions of hydrogen can impact the buildup of interface traps at sensitive regions of the device [18, 44]. Additionally, the type of packaging used for a given part may have trace amounts of hydrogen and impact the resulting dose rate response [4].

ELDRS is a potential issue in oxides irradiated at low electric fields [22]. For this reason, bipolar devices irradiated with terminals grounded may be ELDRS sensitive. MOS devices normally experience maximum degradation from TID when irradiation occurs with rated voltage across the gate. This bias condition creates a much stronger electric field and prevents the presence of ELDRS in the vast majority of MOS devices [38]. However, recent studies have shown that low electric fields within MOS devices, particulary within the shallow trench isolation, may exhibit enhanced degradation at low dose rate irradiation [19, 52, 32]. Such studies show that ELDRS is not only a bipolar device concern.

6.3 ELDRS in SiGe HBTs

Total ionizing dose damage in SiGe HBTs is well documented and understood [14]. The radiation-induced damage is marked by an excess leakage base current that results from a build-up of radiation-induced traps in the emitter-base (EB) spacer region. Increased base leakage current degrades current gain at low injection [14]. The result of this damage can be seen in the Gummel characteristics from Lourenco *et. al.* shown in Fig. 24 for 4^{th}-generation SiGe HBTs [35]. Due to the vertical profile and the thin EB spacer oxide, SiGe HBTs are, in general, inherently multi-Mrad TID tolerant as built.

Nearly all TID studies on SiGe HBTs are conducted using high dose rates, as dose rate effects are not considered a major hardware assurance concern [14]. In 2009, however, SiGe HBT hardness assurance testing was re-evaluated by Cheng *et al.* in [11] for first-generation SiGe HBTs (IBM 5AM). Some unexpected results were

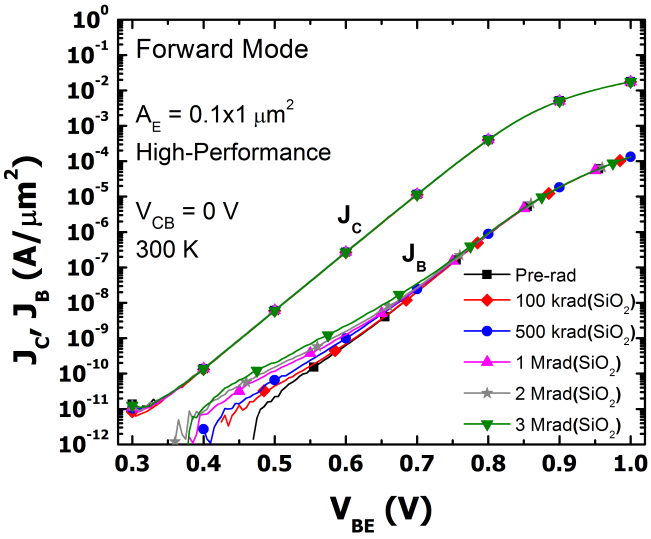

Figure 24: Gummel characteristic of 9HP SiGe HBT up to 3 Mrad(SiO_2) [35].

observed in the irradiated hardware. The results in this study suggest that some first-generation *npn* SiGe HBTs could in fact experience shifts in collector current as high as 12% under LDR irradiation. Collector current shifts are an unexpected TID result and could indicate a real effect that is masked by high dose rate irradiation. Changes in collector current can drastically impact operation of both analog and RF circuits and would indicate an overlooked and quite serious hardware assurance concern for SiGe HBTs, thus making it important to investigate further.

6.4 Experimental Details

One of the major challenges in conducting low dose rate experiments is the time involved in accumulating a significant amount of total ionizing dose. An accumulated dose of 100 krad(SiO_2) takes only minutes using a high dose rate X-ray or proton source. However, reaching the same equivalent dose using a low dose rate source $\leq$ 10 mrad(SiO_2)/s takes months. For the present study, both low and high dose rate experiments were conducted at the NASA Goddard Spaceflight Center (GSFC) Radiation Effects Facility (REF). The exposures were made using a gamma source at a dose rate of 50 rad(SiO_2)/s and 10 mrad(SiO_2)/s for the high and low dose rates,

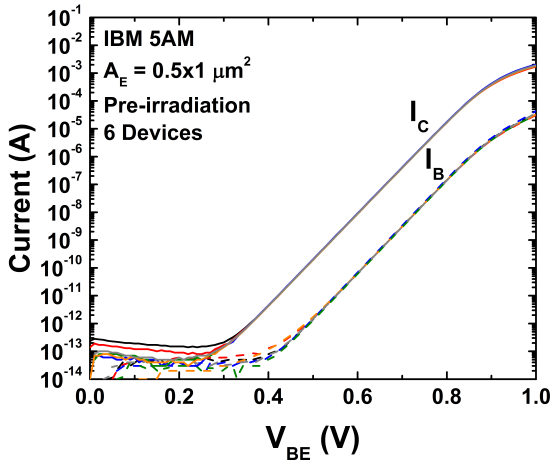

Figure 25: Forward Gummel 1st-generation SiGe HBT.

respectively.

Individual devices were selected from 1st, 3rd, and 4th-generation Silicon-Germanium HBTs. These devices were all manufactured by IBM and correspond to the 5AM, 8HP, and 9HP BiCMOS technologies, respectively. The devices were irradiated up to a total dose of 80 krad(SiO_2), with all terminals grounded. Pre-irradiation measurements were conducted as well as measurements at 50 krad(SiO_2) and 80 krad(SiO_2). Forward Gummel measurements were taken with $V_{CB} = 0$ V. Irradiation was briefly halted to take the 50 krad(SiO_2) measurements and then quickly resumed. Pre-irradiation forward Gummels ($V_{CB} = 0$ V) for all devices, along with the device geometries used, may be seen in Fig. 25, 26, and 27.

The circuit chosen for the present study is the Brokaw bandgap reference (BGR) [9]. Bandgap references are ubiquitous circuits for setting a bias voltage (or current) to an exact value regardless of temperature, loading effects, and power supply variations. A BGR functions by operating two transistors at different current densities in order to produce a voltage proportional to absolute temperature (PTAT) across a sense resistor [9]. This PTAT voltage is then used to drive the output voltage (V_{OUT}) to a value of V_{BE} and the temperature compensated value that is now constant across

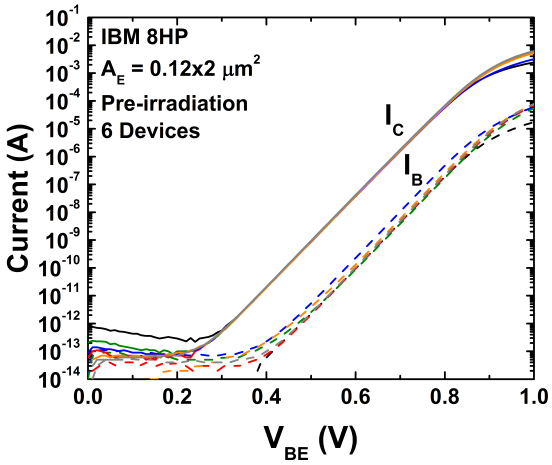

Figure 26: Forward Gummel 3rd-generation SiGe HBT.

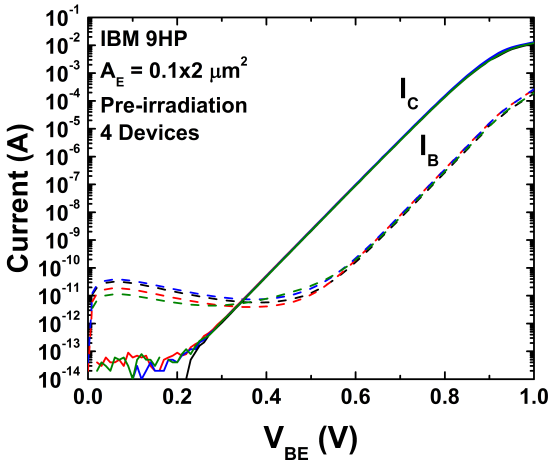

Figure 27: Forward Gummel 4th-generation SiGe HBT.

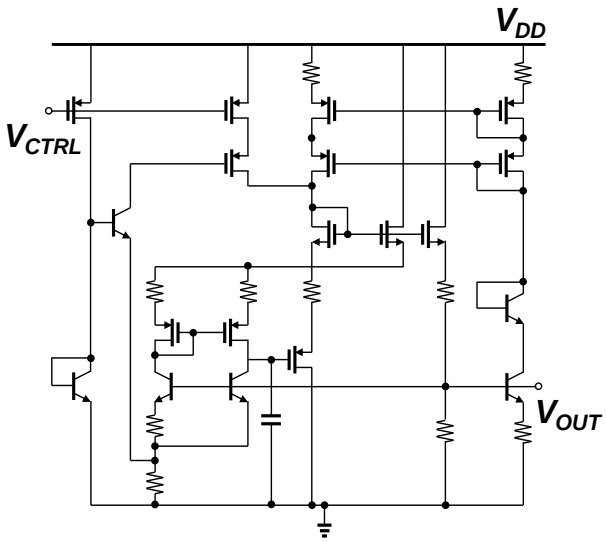

Figure 28: Schematic diagram of Brokaw BGR circuit. All devices (SiGe HBTs, nFETs and pFETs) are on die and simultaneously exposed during irradiation.

temperature [9]. The BGR used in this study (schematic diagram shown in Fig. 28) is a unique topology that exhibits an especially good power supply rejection ratio (PSRR). Higher PSRR prevents harmful variations at the voltage rails from effecting the output voltage of the circuit. The circuit includes pFETs, nFETs (both 90 nm) and *npn* SiGe HBTs from IBMs 9HP SiGe BiCMOS platform. The circuit utilizes a 3.0 V supply rail, a 0 V ground, and an input bias (V_{CTRL}) of approximately 1.7 V used to set the output voltage (V_{OUT}) to 1.2 V.

The BGRs underwent ELDRS testing at room temperature at nominal bias conditions, with V_{DD} = 3 V and V_{CTRL} = 1.7 to 1.8 V (V_{CTRL} varied to set V_{OUT} = 1.2 V). Five BGRs (one BGR per die) were exposed up to a total dose of 100 krad(SiO_2) two at the high dose rate and three at the low dose rate. At each accumulated dose point, the samples were briefly removed from the test chamber to be measured using a Keithley 4200 SCS Parameter Analyzer. All significant bias voltages and currents were tracked at each dose point. No measurements across temperature were performed.

6.5 Device Damage Results

A total of 16 SiGe HBTs underwent gamma irradiation up to a total dose of 80 krad(SiO_2). Half of the devices were irradiated at 50 rad(SiO_2)/s, while the other half underwent low dose rate testing at 0.01 rad(SiO_2)/s. Six of the devices were 1^{st}-generation SiGe HBTs, six were 3^{rd}-generation, and four were 4^{th}-generation. Gummel characteristics are provided for representative devices (one at LDR and one at HDR) from each technology. In addition, normalized base currents are provided for every irradiated device in the generation. The device results are presented in ascending order of generation, followed by a comparison of the device generations.

Of all the generations tested, the 1^{st}-generation SiGe HBTs experienced the smallest overall increase to base leakage current due to TID exposure. This leakage can be seen in Fig. 29. The base leakage current appears to be slightly larger in the low dose rate irradiation case. However, it can be shown that any given device has some variability and that the devices follow the same overall trend in TID degradation. By normalizing the base current to the "least leaky" device and selecting a reasonable operating voltage ($V_{BE} = 0.6$ V), we can more clearly see that the devices are degrading in roughly the same fashion regardless of dose rate. The current normalization is based off of the least leaky device's base current pre-irradiation value (subsequent current values are divided by this normalization factor). The voltage $V_{BE} = 0.6$ V is chosen to look at the relative increase in base current for circuit applications. Although the magnitude of the increased leakage is larger at smaller values of V_{BE}, the trends between LDR and HDR are the same. The result of normalizing the base current in 1^{st}-generation SiGe HBTs is shown in Fig. 30. Notice that two of the devices, one at LDR and one at HDR, actually improve in terms of leakage from 50 krad(SiO_2) to 80 krad(SiO_2). This occurs because the SiGe HBTs are quite robust to TID damage and minor annealing can occur in between irradiation and measurement. This effect would be much less pronounced at higher levels of accumulated dose; however,

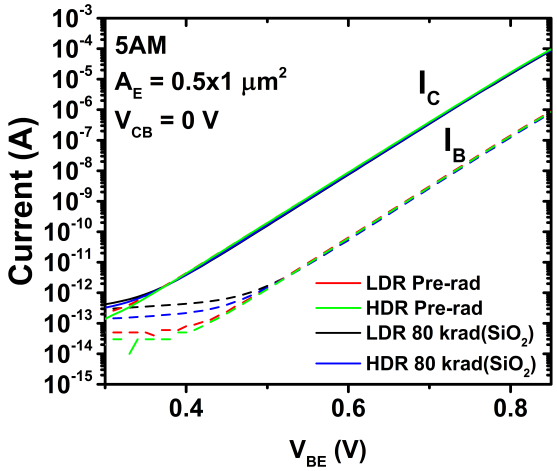

Figure 29: Forward Gummel characteristics at LDR and HDR for 1st-generation SiGe HBTs.

reaching higher levels of TID is challenging using a low dose rate irradiation source.

In a similar fashion, base current degradation is also seen for 3rd-generation SiGe HBTs. Fig. 31 shows the Gummel characteristics of devices after low and high dose rate irradiation, and Fig. 32 shows normalized base leakage current for all devices in this technology generation. As in the previous case, degradation appears to be similar for both the HDR and LDR devices. Some of the devices have more base leakage current before any irradiation occurs. The best device starts at a base current roughly three times smaller than the leakiest device, but subsequent increases in base current due to irradiation are consistent.

Finally, the 4th-generation SiGe HBT device results may be seen in Fig. 33 and Fig. 34. As shown in Fig. 33, the devices in this new technology generation have the most overall base leakage current. However, they, too, do not suffer from ELDRS. If anything, it appears in Fig. 34 that the HDR devices actually experience worse degradation than the LDR devices. This disparity is likely due to time dependent effects and the test setup rather than a true dose rate effect. Given a larger sample size with irradiations to a larger total dose, it is expected that these curves will better match.

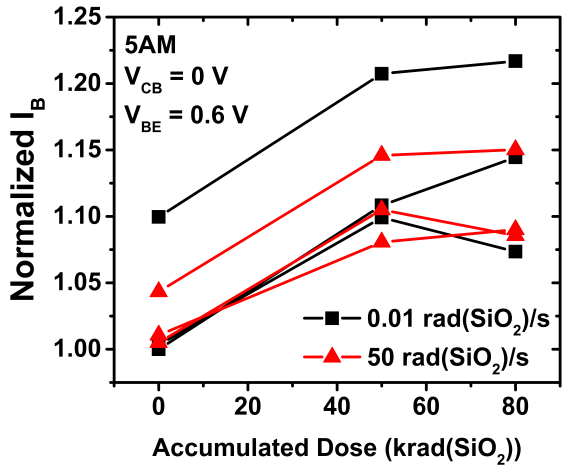

Figure 30: Normalized base leakage current of the 1st-generation SiGe HBTs.

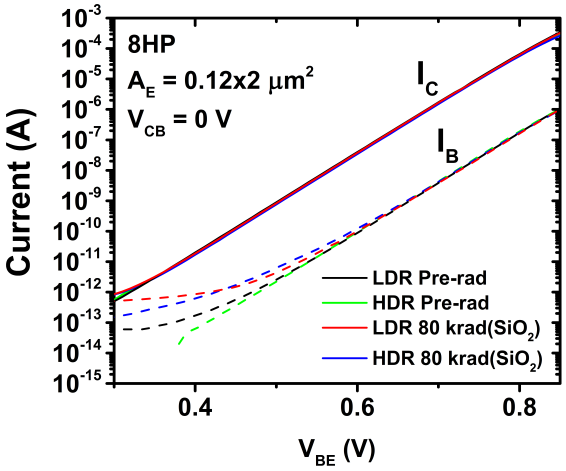

Figure 31: Forward Gummel characteristics at LDR and HDR for 3rd-generation SiGe HBTs.

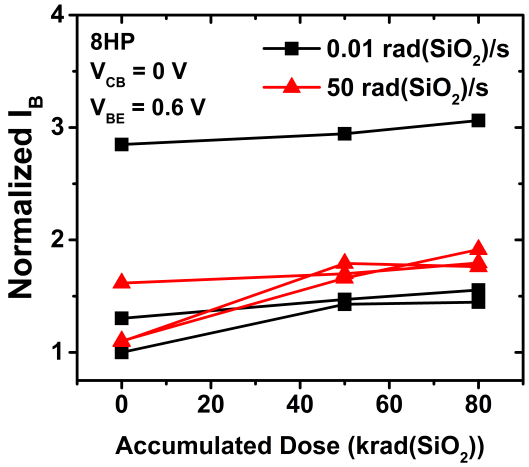

Figure 32: Normalized base leakage current of the 3rd-generation SiGe HBTs.

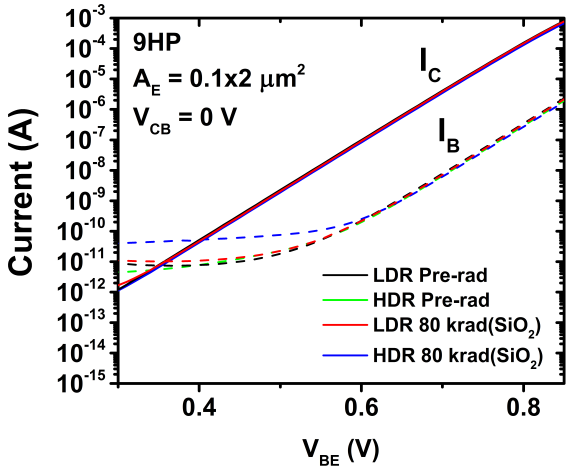

Figure 33: Forward Gummel characteristics at LDR and HDR for 4th-generation SiGe HBTs.

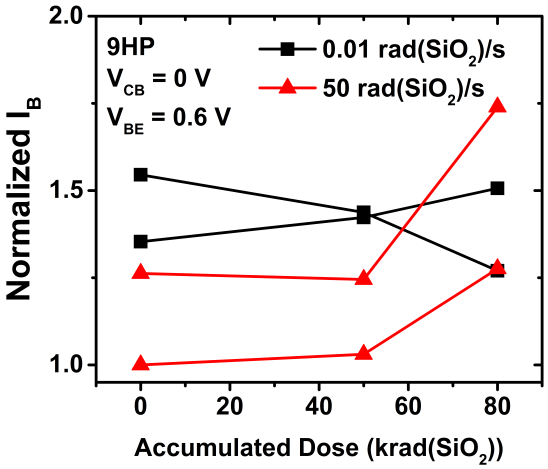

Figure 34: Normalized base leakage current of the 4th-generation SiGe HBTs.

None of the devices under low or high dose rate irradiation experienced any collector current degradation. This result is a good indication that circuits designed with SiGe HBTs will not behave any differently in a low dose rate environment than a high dose rate environment. The TID response between the three generations is quite consistent. However, 3rd and 4th-generation devices are much more sensitive to experimentation in general and tend to have more leakage after device packaging (before irradiation) than 1st-generation devices. In general, looking at the change in base current for all the devices, at $V_{BE} = 0.6$ V, the majority of devices experience less than a 15% change to base current up to 80 krad(SiO_2).

For SiGe HBTs to be ELDRS sensitive there should be a discernible increase to base current leakage at a low dose rate when compared to high dose rate irradiation. However, this increase is not seen. By averaging the change in base current for the devices by generation and dose rate, it can be shown that the LDR devices do not experience a marked increase to base current leakage when compared to the HDR devices. This is shown in Fig. 35. SiGe HBTs remain multi-Mrad TID hardened by process regardless of dose rate, clearly an important benchmark for use in space environments.

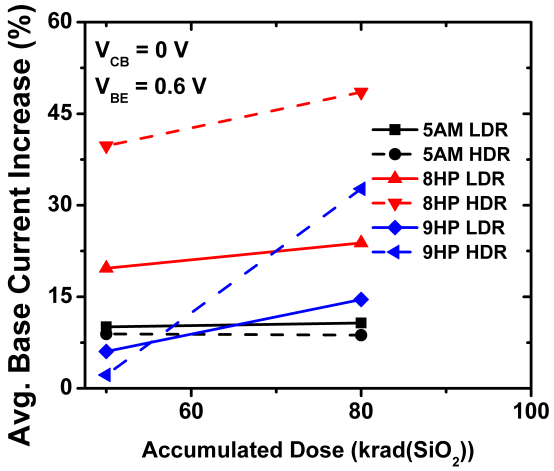

Figure 35: Average percent change in base current for all devices investigated.

6.6 Circuit Damage Results

The bandgap reference (BGR) used in this investigation is an excellent test vehicle to monitor for changes in collector current due to low dose rate irradiation. Any potential collector current shifts due to irradiation would be clearly detectable by monitoring the bias of the BGR. This circuit topology also may help identify large changes in leakage current between LDR and HDR irradiations by monitoring shifts in the supply current. However, results from the single device data show that the leakage difference between high and low dose rate irradiation is very small, and as such, it would be difficult to separate the increased base current leakage from the nFET leakage current using this circuit.

Fig. 36 shows the normalized output voltage for the BGR versus total dose, for dose rates of 50 and 0.01 rad(SiO_2)/s. Both dose rates exhibit an increase in V_{OUT} at increasing TID; however, this increase is reasonably consistent between both dose rates. The slight degradation is driven predominately by two factors: 1) the charge accumulation at the EB spacer in the SiGe HBTs and 2) the charge accumulation at the gate oxide and shallow trench isolation (STI) in the nFETs (field effect transistor). The pFETs in the BGR will not contribute to the TID response, as they do not suffer

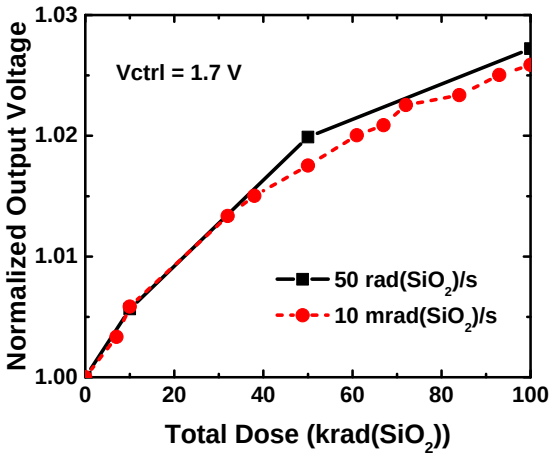

Figure 36: Normalized V_{OUT} versus accumulated dose. Normalized values are given for representative circuits and are calculated by dividing the value of V_{OUT} for a given dose by its pre-irradiation output voltage value.

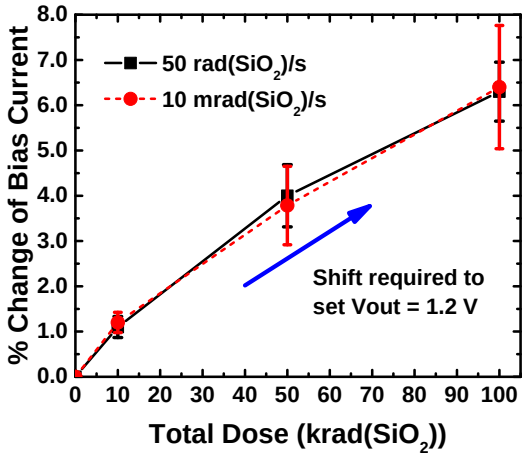

Figure 37: Change in input bias versus accumulated dose. Error bars represent one standard deviation of the measured data.

from TID-induced leakage [14]. For the BGR, the nFET radiation response will likely dominate the circuit response. The SiGe HBT damage results in very minor base leakage current and current gain degradation. The increase to base leakage current will not contribute substantially to the increase in V_{OUT}. When compared to the high dose rate, the low dose rate irradiation does not result in a pronounced increase to base or collector leakage current, and as such, this circuit is not sensitive to ELDRS effects, clearly an encouraging result.

To further address this point, V_{CTRL} was tuned at each accumulation point to see what change in supply current was necessary to return the V_{OUT} to 1.2 V. In this case, both dose rates again give results that are nearly identical. The changes in the supply current, shown in Fig. 37, vary by less than 80 μA (7%) at the highest dose of 100 krad(SiO_2). This change is attributed to the increased leakage current and the resulting shift in the bias operation of the nFET devices. The radiation response for the nFETS is more sensitive to total ionizing dose in this technology. The resulting radiation induced damage will be marked by threshold voltage shifts which cause V_{OUT} and operating points to drift at higher values of TID; the impact of which is much more pronounced than the SiGe HBT response.

6.7 Discussion

SiGe HBTs are not sensitive to ELDRS, a result due primarily to the device structure. The strict processing requirements needed to incorporate a strained SiGe alloy in an epitaxially grown base yield multiple benefits to the total ionizing dose response, and consequently, the dose rate response. The emitter-base (EB) spacer oxide is thin and contained within the heavily doped base region — effectively suppressing much of the leakage that results from interface traps at the Si/SiO_2 interface as a result of TID exposure [14]. In ELDRS, many effected devices are lateral or substrate *pnp* devices [38]. These devices differ from the vertical structure of the SiGe HBT,

where carrier transport is removed from many sensitive structures (e.g., shallow trench isolation). This is true of all SiGe HBTs, not just the technology examined in the present investigation.

SiGe HBTs, like many Si BJTs, do experience worst case degradation with all device terminals grounded. This could be conceived as an indicator for an ELDRS sensitive device. However, SiGe HBTs are strictly controlled during processing to ensure that hydrogen contaminants are eliminated. Epitaxial Si growth generally involves hydrogen passivation and special care is taken to remove any remaining hydrogen, which would otherwise severely impact device operation. Part of this process involves creating oxides and oxide interfaces that are as defect free as possible. The special processing considerations needed to create a robust, well-functioning SiGe HBT also brings about an immunity to ELDRS effects.

6.8 Summary

The three SiGe BiCMOS technology generations (1^{st}, 3^{rd}, 4^{th}) evaluated in this paper, combined with previous work in [27] on 2^{nd}-generation SiGe HBTs, provide a broad evaluation of ELDRS in SiGe HBTs, up through state-of-the-art devices. Based on both device and circuit results, there is no evidence of ELDRS in any generation for this foundry provider. Although this study is limited to only one manufacturer, the same conclusion can be readily inferred for other advanced BiCMOS platforms as well. The strict processing control required to make SiGe HBTs (high quality oxides, low defect densities and epitaxially grown Si), combined with the lack of traditional characteristics of ELDRS-sensitive devices, make this statement likely to remain valid for future generations of the SiGe HBT.

CHAPTER VII

CONCLUSION

7.1 Contributions

The results of the discussions from Chapter 5 on the effects of TID on a 180 nm CMOS technology show the efficacy of such a platform for space missions with extremely high (multi-Mrad) TID hardness requirements such as missions to Jupiter's moon, Europa. Standard, commercial CMOS platforms are unable to meet such a requirement. The saturation effect seen in the TID platform is quite unique and allows a BiCMOS implementation to be feasible for such a mission. The results from this work have been published in the September (2014) issue of IEEE Transactions on Device and Materials Reliability [24].

The results from Chapter 6 on the effects of low dose rate irradiation across multiple SiGe HBT generations (all the way from the initial 1^{st}-generation to state-of-the-art 4^{th}-generation devices) has been evaluated. The results from this study include the first ever evaulation of low dose rate effects in 4^{th}-generation SiGe HBTs, and the first SiGe HBT circuit study for ELDRS effects. This work shows that SiGe HBTs are indeed multi-Mrad TID hard as manufactured. In addition, devices only see a small increase to base current at low injection increases in collector current are not observed. The results from this work are slated to be published in the December (2014) issue of IEEE Transactions on Nuclear Science [23].

7.2 Future Work

7.2.1 Improved 3D 180 nm CMOS Models

In order to better understand the TID effects seen in the 180 nm Jazz nFETs, improved TCAD models are needed. The present models do a good job at analyzing a

sheet charge; however, NanoTCAD has limitations in TID simulations. As such, 3D 180 nm NMOS models have been designed in Synopsis TCAD [3]. The new models are currently undergoing calibration to device data and will be better equipped for future alterations. One necessary modification will be designing a non-uniform sheet charge as opposed to a constant sheet charge. This approach will likely be able to distinguish the disparity between the IBM (vertical STI sidewall) and the Jazz (slanted STI sidewall). As mentioned previously, the electric field contours at the STI corner dictate where charge accumulation occurs on the STI sidewall, and a non-uniform sheet charge will be able to account for this effect.

It will be much more challenging to distinguish the underlying cause of the turn-around effect. There will need to be a software-based feedback system in place that is able to adaptively take-in information about the current state of the transistor in order to determine how and where charge accumulation is occurring or being removed. No such simulation technique is currently used today, and such a system could help better explain TID effects in advanced CMOS technologies.

7.2.2 Generational Study of SET Effects in SiGe HBTs

Now that a generational study of TID (dose-rate effects) in SiGe HBTs has been conducted, it would be helpful to do a similar type study for SET effects. It is known that SiGe HBTs are quite susceptible to SET effects — being upset at LETs (linear energy transfer) as low as 1 to 2 MeV-cm^2/mg. However, some systems (like the laser two-photon absorption system at the Naval Research Laboratory) do not have the capability of correlating laser testing to an equivalent LET (which is necessary to know for a real radiation environment). Test structures have been designed in regards to this issue so that an equivalent LET can be correlated to a laser strike at such a facility. Each technology may have different response, so it is necessary to look at multiple generations in order to better understand the underlying physics of charge

collection and transient effects in SiGe HBTs.

7.2.3 Analysis of SETs in Highly Scaled CMOS Circuit Primitives

An on-going area of research is trying to better understand how RF circuits respond to current transients. It is very challenging to create a system that is able to completely track a current or voltage spike all the way down a transceiver chain. Thus it makes sense to begin looking at RF circuit primitives such as multiple transistor structures and amplifier cores. Plans are underway to start testing the transient response of differential pairs (a circuit primitive) in a 32 nm technology. Such a study will allow for differences in 32 nm transients to be investigated in addition to seeing how a basic circuit functions in response to a transient.

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