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Low Frequency Sinusoidal Oscillator for Impedance Spectroscopy

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Low Frequency Sinusoidal Oscillator for Impedance Spectroscopy

by

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Dedication

This work is dedicated to my mother and father, whose constant motivation and support through the years has been indispensable.

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I would like to express gratitude to my advisor, Dr. TR Viswanathan for his support and guidance throughout my graduate education. His vast experience and insight has proven to be invaluable.

I am indebted to my parents, Leelavathi BR and Revanna Siddappa. It is only their encouragement, co-operation and support that has led to all my accomplishments.

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Abstract

Low Frequency Sinusoidal Oscillator for Impedance Spectroscopy

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The University of Texas at Austin, 2014

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Impedance measurement as a function of frequency is being increasingly used for the detection of organic molecules. The main building block required for this is a sinusoidal oscillator whose frequency can be varied in the range of a few kHz to tens of MHz. The thesis describes the design of Integrated CMOS Oscillator Circuits. There are 2 designs presented in the thesis, one of which is based on the Wien Bridge and the other, on an *LC* architecture. They provide both in-phase and quadrature outputs needed for the determination of the real and imaginary parts of complex impedances.

The inductor in the *LC* tank is realized by gyration of a capacitor. This needs two variable transconductance elements. Linear transconductance elements with decoupled transconductance g_m and output conductance g_o is presented. A novel circuit for detecting and controlling the amplitude of oscillation is described. A current mode technique to scale the capacitance is also discussed.

Since this oscillator is used in an inexpensive hand-held instrument, both power consumption and chip area must be minimized. A comparison between the Wien Bridge

and the *LC* tank based oscillator is presented. Simulation results pertaining to the design of the different blocks of the circuit are made available.

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Chapter 1: Introduction

1.1 Overview

Oscillators have been an integral part of analog circuit design from the days when Howard Armstrong designed the first electronic oscillator with vacuum tubes. Even digital circuits require a timing reference, which is produced by an oscillator. The use of oscillators has extended vastly even in the field of Biomedical Engineering in applications like Impedance Spectroscopy.

This thesis discusses the design of an integrated CMOS oscillator circuit specifically meant for the application Impedance Spectroscopy. Low-frequency impedance measurement is becoming popular for the detection and analysis of molecules encountered in biological systems. This requires an integrated oscillator tunable over a wide low frequency range, i.e. from *1kHz* to *10MHz* [1]. Impedance spectroscopy has man bio-medical applications such as blood glucometers and is meant to be a single use throwaway chip. For this reason, both cost and power consumption must be minimized.

The design of a low frequency sinusoidal oscillator is not a trivial problem. We need large values of resistance (*R*), inductance (*L*) and capacitance (*C*), which will need more area in an integrated circuit (*IC*). Filtering low frequency sinusoids also require large time constants. The design of an integrated circuit that meets these challenges of lower cost, power with acceptable low levels of distortion is discussed in this thesis.

We investigate two architectures of oscillators in this thesis, namely the conventional Wien-Bridge Oscillator and the LC Oscillator. Design techniques to implement linear inductors / resistances for realizing the oscillator is described. Novel circuits for the detection and control of the amplitude of oscillation are described. Simulation results pertaining to the same are presented.

1.2 IMPEDANCE SPECTROSCOPY

Impedance spectroscopy is a technique used for the characterization or detection of biological molecules. Currently, integrated circuits are being designed for a variety of applications that employ impedance spectroscopy. In this technique, traditionally known as cyclic voltametry, the complex impedance measurement of a solution is used to detect the presence and estimate the quantity of a specific substance.

Electrodes are placed in an aqueous solution containing the substances/analytes to be analyzed. These analytes in the solution bind to the electrodes and changes the electrical characteristics of the electrode-electrolyte interface. Typically, the electrode - electrolyte interface is modeled as a parallel combination of a resistor and capacitor (R_d and C_d), in series with a solution resistance (R_b). The presence of R_d and C_d inherently gives rise to a frequency response, which is characteristic to the analytes present in the solution. The modeling of electrodes is dealt in great detail in [2].

Impedance is purely an electrical quantity. A key component for impedance spectroscopy is an oscillator that generates pure Sine waves. A sinusoidal voltage is applied to an electrolyte and the resulting current is measured. The complex ratio of the two gives the impedance. A generic block diagram of the technique is given in Figure 1.

The architecture resembles a typical quadrature mixer. A sinusoidal voltage input of amplitude A and frequency ω, $V_{in} = A\ Sin(\omega t)$ is applied to the electrolyte. The current, $I_{in} = A_1\ Sin(\omega t - \Theta)$ is sensed. The magnitude of A_1/A gives the magnitude of the impedance of the solution. This impedance has a reactive component, which manifests as a phase change Θ in the measured current. The mixer multiplies I_{in} with in-phase and quadrature sinusoids of amplitude B as shown in the figure. The product yields a second order term. The DC components are extracted by Low Pass Filters (LPF). This contains the amplitude information (A_1) and phase information (Θ). From the outputs of the mixer,

the magnitude of the impedance is obtained by taking the square root of the sum of the squares of the LPF outputs. An arc-tangent of the ratio will give the phase of the complex impedance. This procedure is repeated for different frequencies by sweeping ω and measuring the impedances for all frequencies of interest. This way, the complex impedance as a function of frequency is obtained for the solution under test. This information is used to determine the nature and the quantity of a specific molecule in the test solution.

The reference [1] provides the design of the mixer, electrode and the low pass filter. The scope of this thesis is limited to the design of the sinusoidal excitation V_{in}, the in-phase and quadrature signals for the mixer.

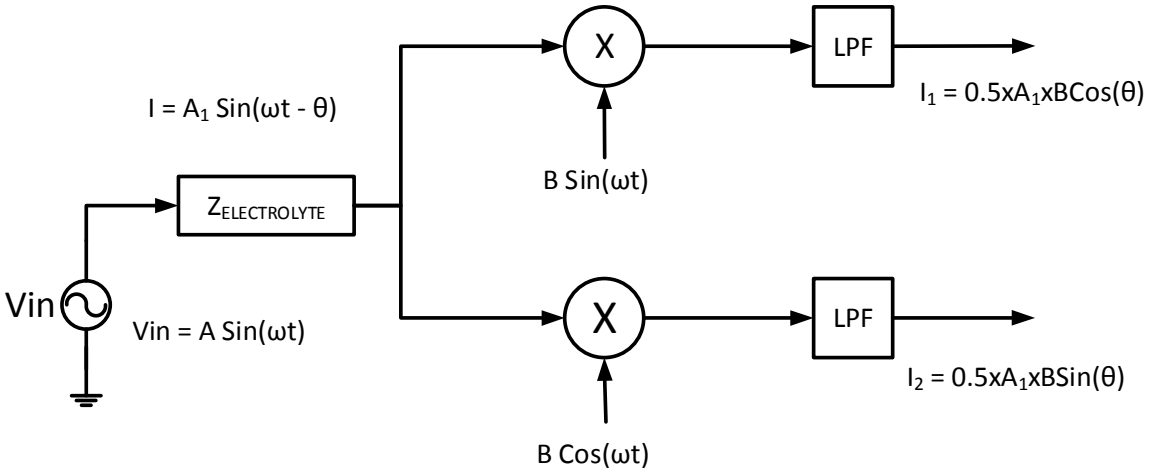

Figure 1: Block Diagram of Impedance Spectroscopy.

1.3 SPECIFICATIONS

A high purity, low frequency, integrated sinusoidal oscillator can find an application in many fields of engineering. Once a sinusoid is obtained, generating a

square wave or a ramp would be trivial tasks of squaring, integration etc. Traditional low frequency signal generators inherently have a very large power consumption. This prevents the utility of such devices in portable applications where the available power is limited. An application such as impedance spectroscopy is used in blood glucose monitoring. With the cost of integrated circuits going down, the development of a single use portable blood glucometer chip is indeed economical. Such a portable application demands low power consumption. These are meant to be single use throw-away chips and hence, the cost of the *IC* must be minimal.

In the context of impedance spectroscopy, the oscillator is required to generate frequencies spanning from *1kHz* to *10MHz*. Linearity of the frequency sweep with respect to the control variable is not essential. The frequency of the oscillations can always be measured by on-chip digital counters.

The purity of the sine wave, which is characterized by the Total Harmonic Distortion (THD) must be better than *-25dB* [1]. This ensures that the impedance profile obtained from a solution is within the accuracy limits of the system. As the distortion increases, the impedance resolution will not be adequate for molecular identification. So, it is very important to focus the design on reducing distortion. A voltage output is desired. For impedance spectroscopy, it is sufficient that the amplitude of excitation is around *1mV* to *10mV* [5]. But, the amplitude of the output can always be adjusted with a variable gain amplifier depending on the application requirement. It must be ensured that there is no DC component in the output. This is only to ensure that there is no polarization of the molecules in the electrolyte, which inherently degrades the electrode - electrolyte interface.

1.4 ORGANIZATION OF THE THESIS

Chapter 1 provided a motivation for having a portable low frequency sinusoidal oscillator. With reference to Impedance Spectroscopy, a set of specifications are established. We investigate two different circuit choices, namely the Wien-Bridge oscillator and the *LC* Oscillator. Chapter 2 discusses the former and Chapter 3 discusses the latter part. Chapter 4 compares the two topologies. Chapter 5 provides the conclusion and scope for future research in the design of low frequency sinusoidal oscillators.

Chapter 2: Wien Bridge Oscillator

2.1 INTRODUCTION

This chapter discusses the design of a Wien bridge Oscillator for applications like impedance spectroscopy. The design of an integrated circuit that meets the challenges of low frequency, low cost, power and low levels of distortion is presented here. Design choices which makes the performance of the oscillator temperature and process independent are discussed. The chapter concludes with simulation results in a 180nm CMOS process.

The well-known Wien-Bridge driven by a sinusoidal voltage source is shown in Figure 2a. It consists of two impedances, namely R_1 in series with C_1 and R_2 in parallel with C_2. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the output voltage, V_{out} becomes maximum when the frequency f of the sinusoidal excitation (V_{in}) is equal to $1/2\pi RC$. Furthermore, at this frequency, the output is in phase with the input and is attenuated by a factor of three. Thus, to design an oscillator with this network, the output voltage is sensed and fed back to its input with a voltage amplifier of gain greater than 3 to start the oscillations [3].

The gain of *3* can indeed be altered by changing the value of the capacitors/resistors in the design. The gain expression at the resonant frequency is given below.

$$I3 = \frac{Iin}{\frac{C1}{C2} + (1 + \frac{R2}{R1})}$$

To keep the resonant frequency the same, the product $C_1C_2R_1R_2$ must be the same. So, if $C_1 = nC_2$, then $R_2 = nR_1$. Thus, the gain expression will have a minimum when either $n = +1$ or $n = -1$. The case of $n = -1$ requires the use of -ve resistance and capacitance. The design of these units will consume more power. So, we choose $n = +1$ and make $C_1 = C_2$ and $R_1 = R_2$.

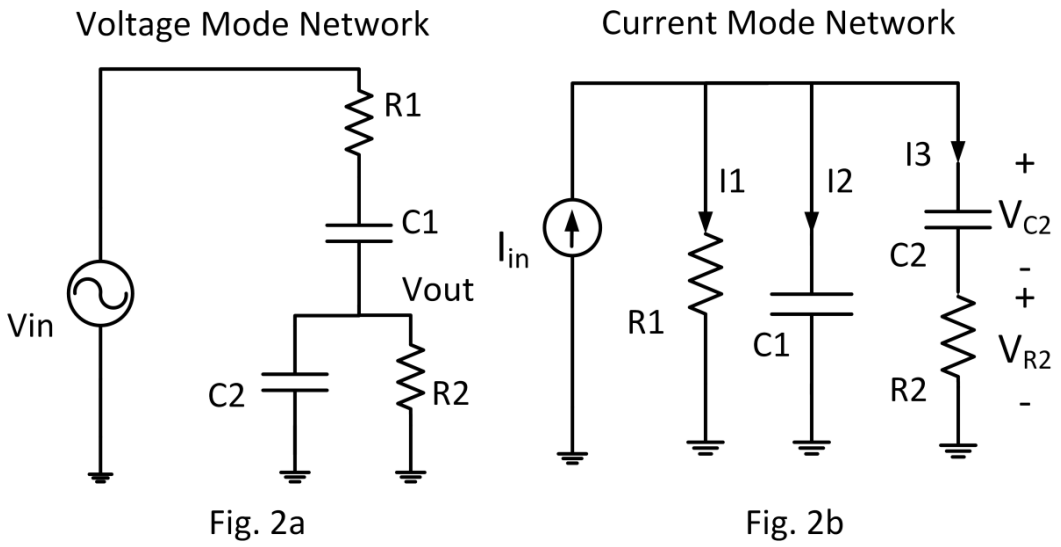

Figure 2: Voltage and Current Mode Wien Bridge Networks

We use a current mode approach to enable the use of a current-gain element instead of a voltage-gain element keeping in mind the fact that the well known current-mirror circuit is translinear, temperature insensitive and immune to process variations. Thus, we transform a Wien Bridge network using its dual network as shown in Figure 2b.

The transfer functions of the currents I_1, I_2, I_3 in the three branches of Figure 2b are given in Table 1. The time constant RC is represented by symbol τ. Note that at $\omega=1/\tau$, the currents I_1 and I_2 as well as the voltages V_{C2} and V_{R2} are in quadrature. A current gain of three is required to configure an oscillator using this transformed network.

T(s)	Transfer Function	*For $s=j\omega$ and $\omega\tau=1$*
$I_1(s)/Iin(s)$	$(1+s\tau)/(s^2\tau^2+3s\tau+1)$	$T(j\omega)=(1-j)/3$
$I_2(s)/Iin(s)$	$s\tau(1+s\tau)/(s^2\tau^2+3s\tau+1)$	$T(j\omega)=(1+j)/3$
$I_3(s)/Iin(s)$	$s\tau/(s^2\tau^2+3s\tau+1)$	$T(j\omega)=1/3$

Table 1: Transfer functions for I_1, I_2, I_3

2.2 DESIGN CONSIDERATIONS

The frequency of oscillation, $f = 1/2\pi RC$ is a function of resistance and capacitance. Since the frequency of the oscillator is to be varied over a wide range of *1kHz* to *10MHz*, either *R* or *C* must be variable. In this design, the value of the capacitance is fixed and the resistors are chosen to be "incremental resistances" of CMOS transistors ($R=1/g_m$, where g_m is the Transconductance of a CMOS transistor) so that their values can be varied by the DC quiescent currents flowing through them.

The key issues in the design are to get a wide range of low frequencies, low power, cost and acceptable levels of distortion. Temperature and process-independent current-gain, obtained by a current-mirror maintains oscillations over a wide temperature range. The following sections will explain the design of a linear resistor, biasing circuit, current-gain blocks, amplitude detector etc.

2.3 LINEAR RESISTOR AND CURRENT MIRROR

There are many circuit choices for obtaining variable resistance. The current-biased MOSFET or a differential pair with a current mirror active load etc., are examples of commonly used circuits. Here, we use the well-known class-AB CMOS inverter as a variable transconductance element [4]. When the output of the inverter is connected to its input (called diode-connection), the quiescent voltage at the node will be at the "Logical Threshold", V_{LT} of the inverter. We use the CMOS-inverter shown in Figure 3a because it provides a linear transconductance when operating into a voltage source that maintains a bias voltage equal to V_{LT} at its output as shown in Figure 3b. The advantage of using the CMOS inverter is that the transconductance obtained is doubled for a given current in contrast to a differential amplifier since both the PMOS and NMOS share the same bias current. Hence, the power consumed is halved, which is critical for this application.

An inverter provides a linear incremental transconductance around V_{LT} and for an incremental input voltage V_{in} applied around this operating point, it behaves like a linear resistor so long as its magnitude is less than the over-drive voltage V_{GS}-V_{TH}. Its value is varied by controlling the quiescent current through the inverter. A diode connected inverter acts as a grounded resistor $R = 1/g_m$, as shown in Figure 3c. This would be used as a substitute for the resistors in the design. The transconductance, g_m of the inverter is the sum of the transconductances of the NMOS and PMOS transistors g_{mn} and g_{mp} respectively. (i.e. $g_m = g_{mn}+g_{mp}$).

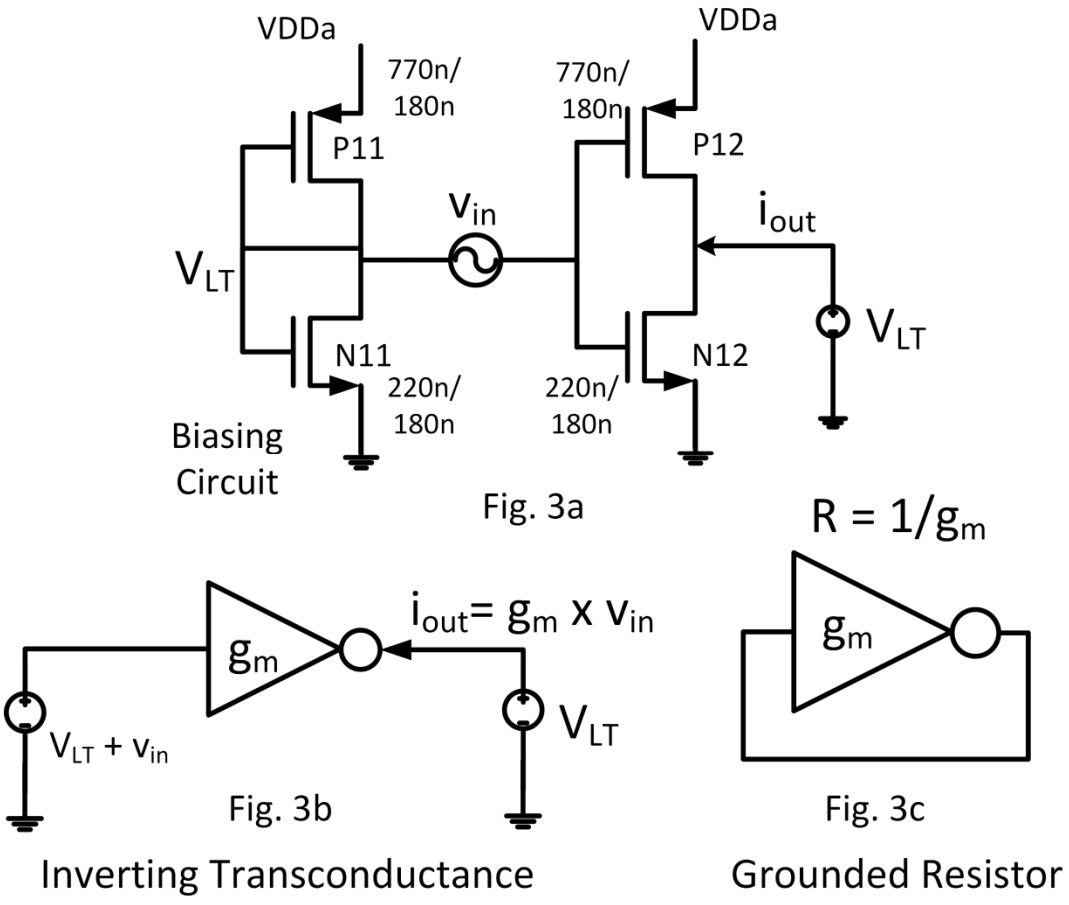

Figure 3: CMOS Class AB Inverting Transconductance

The device sizes chosen for this implementation are annotated in the figure. The V_{LT} bias is obtained by diode connecting an inverter circuit (formed by *P11* and *N11*) as shown. It is a known fact that both mobility and threshold voltage differ between a PMOS transistor and NMOS transistor. This means that the two devices have different transconductances for the same bias current if sized similar. By scaling the width of the PMOS to be 3.5 times larger than the width of the NMOS, it is ensured that the derivative of g_m around V_{LT} is 0, so that the inverter is linear around V_{LT}.

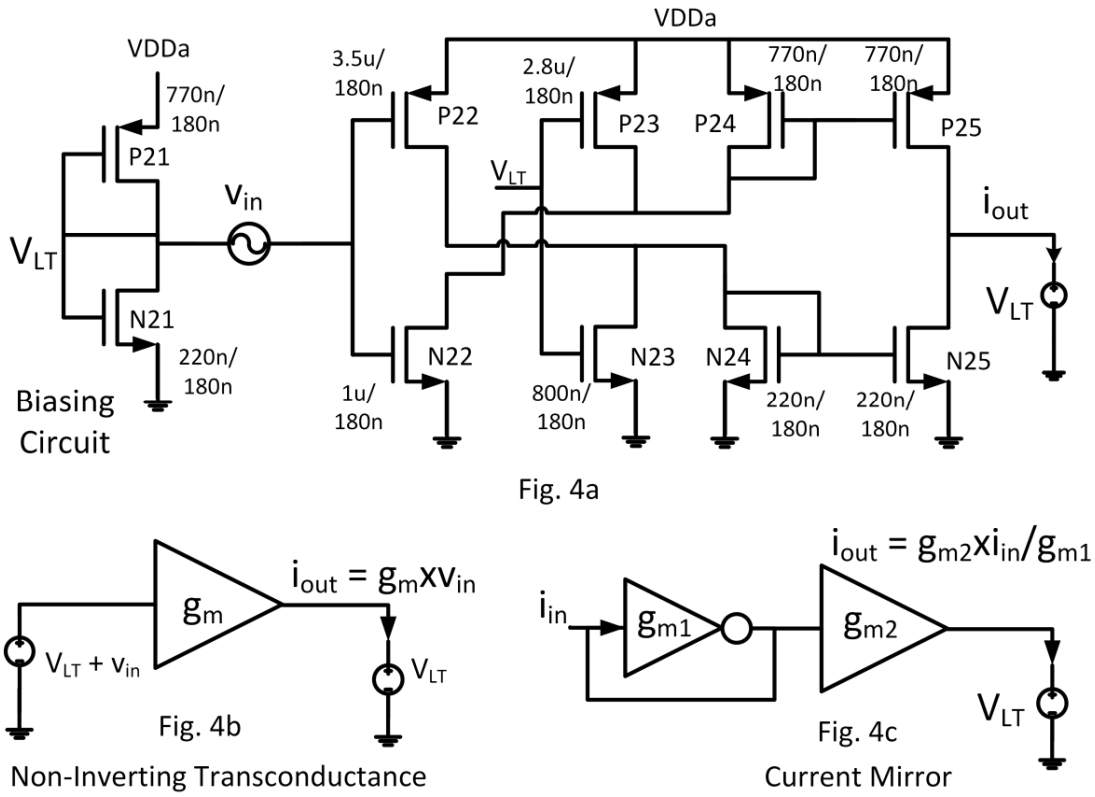

Figure 4: Non Inverting Transconductance.

Let $i = f(v)$ represent the transfer characteristics of a MOSFET, where $f(v) = f_{odd}(v) + f_{even}(v)$. In a CMOS inverter, if a voltage $V_{LT}+v$ drives the NMOS, the PMOS

receives a voltage V_{LT}-v. It is customary to make the strengths of the two devices equal by appropriate sizing and make them identical. Thus, their currents will have magnitudes represented by $f(V_{LT}+v)$ and $f(V_{LT}-v)$ respectively. If the PMOS output is considered as a current source, the output of the NMOS is a current sink. If we invert the two currents using current mirrors and subtract them, we get a purely odd output that is linear for signals less than the overdrive voltage, V_{ov}.

A non-inverting transconductance element based on this idea is shown in Figure 4a. It can also be implemented with 3 inverters, where the first inverter will feed a diode-connected inverter load, the output of which will drive another inverter operating as a g_m element. Such a circuit will have lower linearity and bandwidth than the arrangement shown in Figure 4a because of the use of current mirrors for obtaining the inversion. The diode connected transistors of the current mirror, *P24* and *N24* provides larger bandwidth because it reduces the capacitance and the resistive impedance seen at the output node of *N22* and *P22*.

In the inverter shown in Figure 3, both the transconductance g_m and the output conductance g_o were coupled because the same quiescent current flowed through the transistors *P12* and *N12* which is responsible for both g_m and g_o. In the non-inverting g_m structure of Figure 4, the coupling is isolated. The transistors *P22* and *N22* are the transistors responsible for determining the g_m of the circuit, whereas transistors *P25* and *N25* determine the output conductance g_o. The quiescent currents of *P22* and *N22* are removed before entering the current mirrors to minimize the output conductance of the circuit. This is done using *P23* and *N23* as shown. Only the signal current flows into the diode-connected transistors *P24* and *N24* of the current mirror. Thus, the V_{GS} of *P24*, *P25* will be V_{tp} and the V_{GS} of *N24* and *N25* will be V_{tn} due to almost zero quiescent current. The behavior will now be Class B. Since there is no quiescent current in *P25* and *N25*,

the output resistance is very large for the non-inverting g_m element. Thus, we can have independent control of g_m and g_o in the circuit.

From the device sizes, it is quite evident that the quiescence is not completely canceled. If the quiescence is completely canceled, it can be noticed that the diode connected transistors of the PMOS and NMOS current mirrors sit at V_{tp} and V_{tn} respectively. This may give rise to problems of cross-over distortion as the signal swings, which will further degrade the harmonic distortion of the sine wave. So, there is a fraction of the quiescence being allowed to flow at the output to avoid the problems of cross-over distortion. We still benefit from having large g_m and low g_o due to the decoupling offered by the circuit.

Note the conventions used for inverting and non-inverting transconductance elements, shown in Figure 3b and 4b. In a non-inverting transconductance, the output current is sourced into the voltage source when $V_{in}>V_{LT}$. In an inverting transconductance, the output is a current–sink.

Consider a diode connected inverter fed by an input current as shown in Figure 4c. The input current i_{in} sees a load of $1/g_{m1}$ and produces a voltage, $v = i_{in}/g_{m1}$. When this voltage is fed to another logic-inverter operating with the output at V_{LT} and a transconductance equal to g_{m2}, we get a current mirror with the output current, i_{out} being $i_{out} = g_{m2} \times i_{in} / g_{m1}$. The current gain i_{out}/i_{in} is g_{m2}/g_{m1}. This relation is very useful because it is temperature and process invariant. The g_m is varied by scaling the aspect ratio (W/L) of the devices. Here, the current gain g_{m2}/g_{m1} is greater than 3 for sustaining oscillations. We use this structure to get the required current gain to start the oscillations.

2.3 BIAS ARRANGEMENT

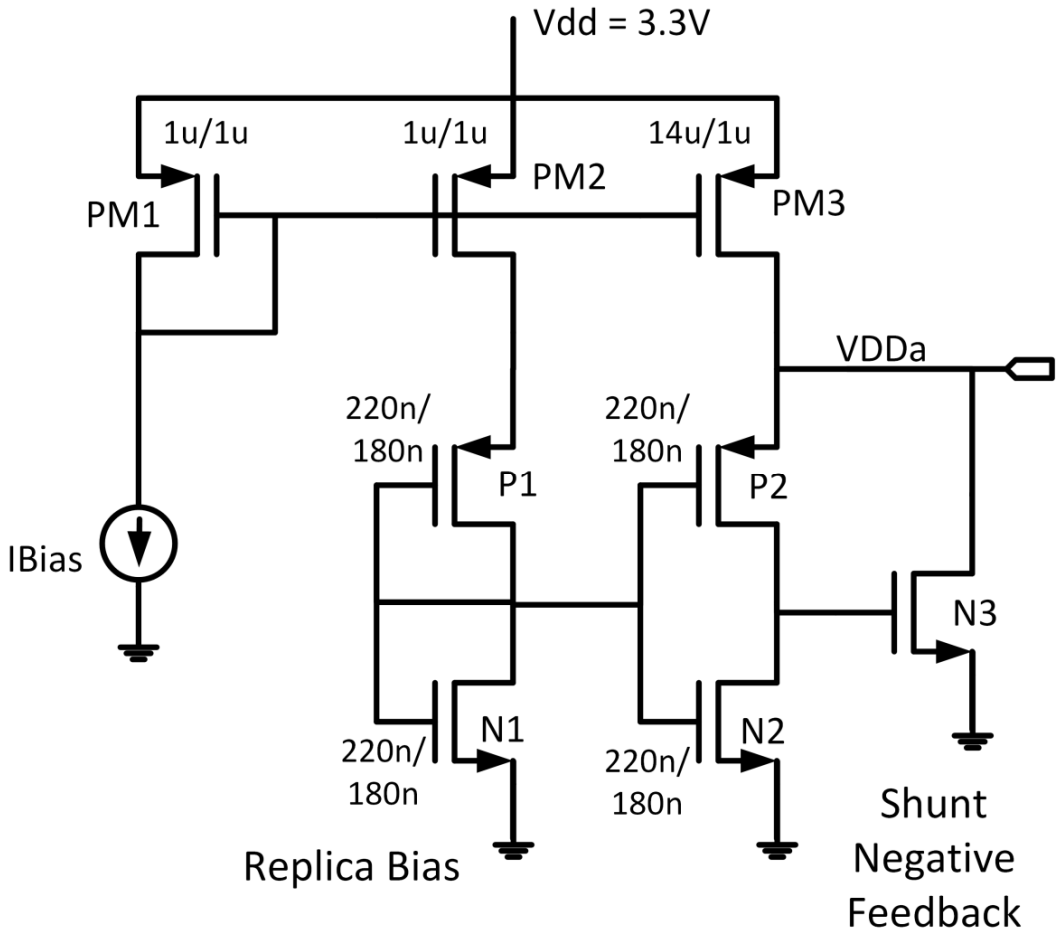

Figure 5: Current Control using Replica Biasing Technique

Since FET's are square-law devices, a constant voltage biasing can result in large variations in the bias current with respect to both process and temperature variations. Thus, a better biasing technique is necessary to keep the current through the inverters at a controlled reference value. The idea here is to use a replica arrangement shown in Figure 5. The input current is made to flow in a replica-inverter (formed by *P1* and *N1*) and the voltage across it (*VDDa*) becomes a regulated power supply voltage for all the inverters

used in the oscillator circuit. So, with process and temperature variations, the voltage, *VDDa* scales appropriately. This is a well known super-source follower circuit with shunt negative feedback (achieved by *P2*, *N2* and *N3*). It helps achieve very low output-impedance at *VDDa*. Without *N3*, the small signal impedance seen at *VDDa* is $1/g_{m2}$, the g_m of *P2*. The shunt negative feedback configuration changes this factor to $1/(g_{m2}+A_2 g_{m3})$, where A_2 and g_{m3} are the open loop gain of *P2* and g_m of *N3* respectively, thereby reducing the output impedance of the power supply. By changing the bias current, *VDDa* and V_{LT} changes and hence the g_m of all the inverters.

2.4 OSCILLATOR SCHEMATIC

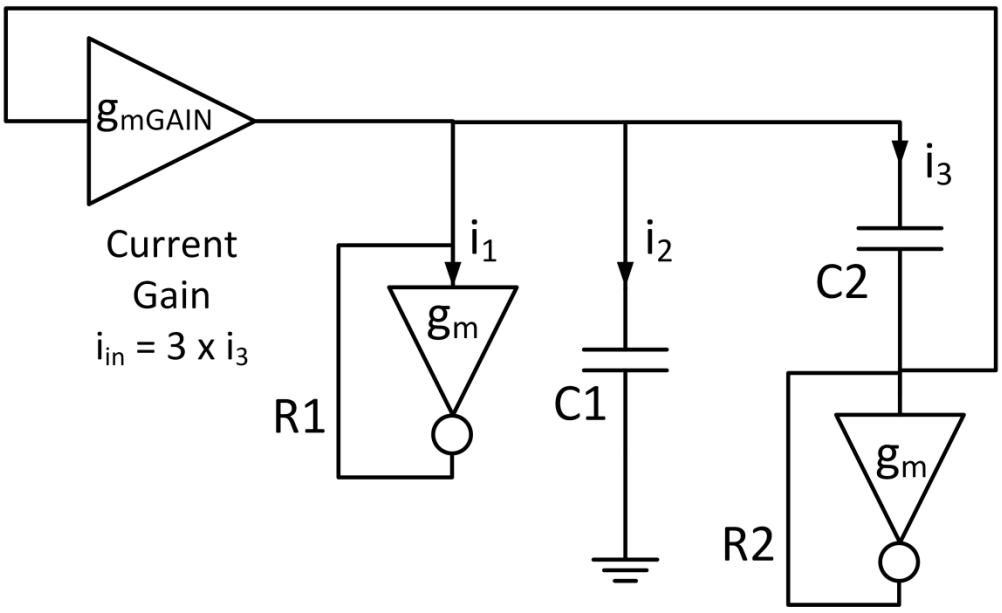

Figure 6: Oscillator Schematic

The schematic of the oscillator is shown in Figure 6. The design requires a current gain greater than 3 between i_3 and i_{in}. Comparing this to Figure 4c, the g_m block,

indicated as *R2* acts as both current sensing block and a resistor. This prevents unnecessary loading of the third branch for current sensing. We limit *C1* and *C2* to *10pF* due to area constraints. So, to achieve the frequency range, the g_m (*=1/R*) has to sweep from *60nS* to *0.6mS* because $f = g_m/2\pi C$.

2.5 AMPLITUDE CONTROL

Historically, the very first Wien Bridge audio oscillators manufactured by HP used vacuum tubes for active elements and light bulbs for amplitude control. There are also other structures that use diodes, high temperature coefficient resistors etc., limiting the amplitude of oscillation.

We present a novel circuit for detecting the amplitude of oscillation in Figure 7. The circuit uses the well known trigonometric identity $Sin^2\theta+Cos^2\theta = 1$. Thus, if we square and add the I and Q components, we get a DC output proportional to the amplitude of oscillation without any need for filtering which is difficult at low frequencies [5].

Consider the circuit shown in Figure 7. The orthogonal voltages across the capacitor *C2* and resistor *R2* are applied as inputs to this circuit and are represented as sine and cosine signals. The circuit implements the following simple but general idea. When we add *f(v)* and *f(-v)*, the odd terms cancel and thus, we can isolate the even-component. We use long-channel transistors to maximize the square-law content in the even component. The PMOS output is inverted using a current mirror and added to the NMOS output to get a square law output. In the circuit of Figure 7, the Sine and Cosine squaring paths share the current mirror. The quiescent current at the output is removed by

P33. This circuit always sinks a current for positive and negative values of *v* due to its square-law behavior.

When the sine and cosine components are squared and summed, the output current I_{OUT} which has the amplitude information is still in the square form. To obtain the square root of I_{OUT}, a diode-connected complementary circuit that sources a square-law current is required. It is obtained by rebuilding the circuit with PMOS mirrors instead of NMOS mirrors. Such a diode-connected circuit (input and output being shorted) is shown in Figure 8. When not diode-connected, the circuit will always source a current for both positive and negative values of the input voltage *v*, depicting the complementary behavior to the circuit in Figure 7. Similar to *P33* of Figure 7, *N42* removes the DC quiescent current at the output. The diode connection ensures that the output voltage is proportional to the square-root of the current i_{in} fed into the circuit.

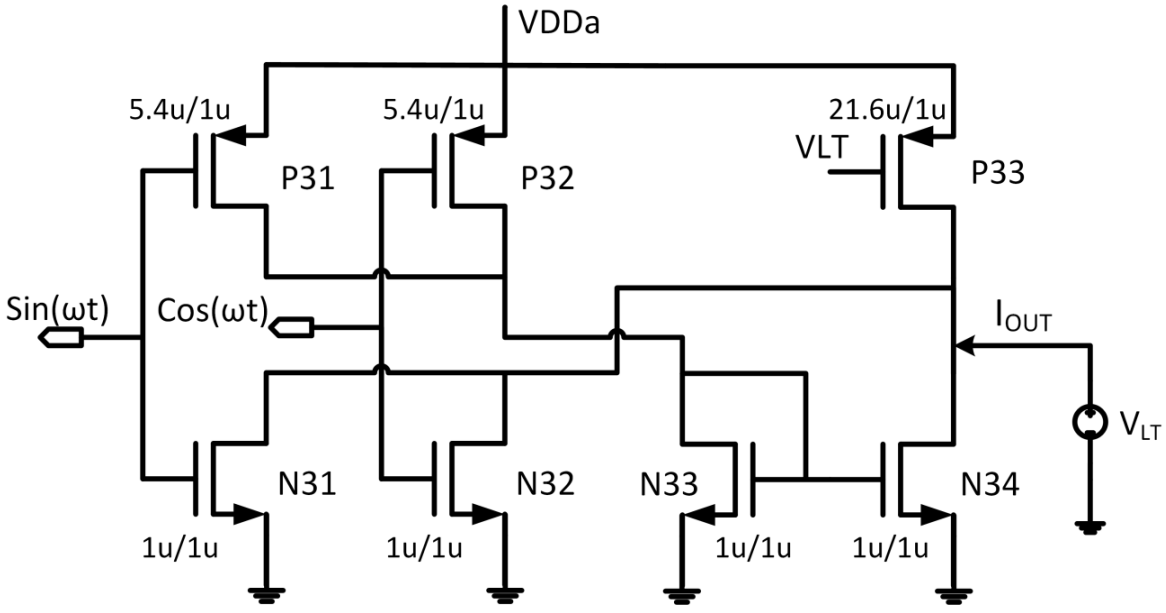

Figure 7: A Novel CMOS Squaring Circuit

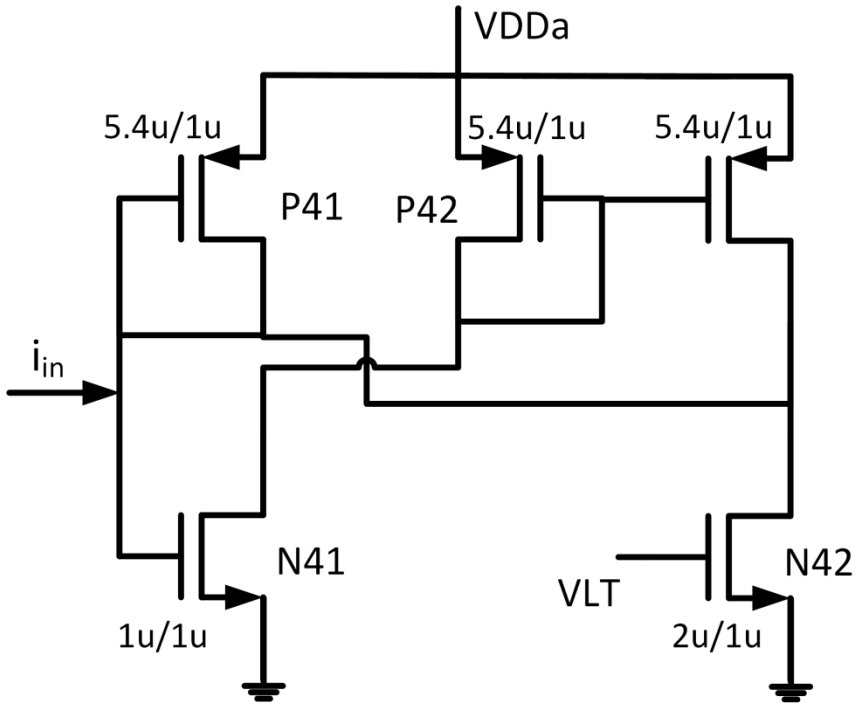

Figure 8: Complementary diode connected Squarer circuit.

Since the current gain of three is set by a ratio g_{m2}/g_{m1} (Figure 4c) and the g_m values in turn set by the quiescent currents, by decreasing the quiescent current in g_{m2}, the gain is reduced as the amplitude tends to grow. The inherent non-linearity of the current gain block could also be used to limit the amplitude of oscillation [6]. As the amplitude grows, g_{m2} decreases, reducing the incremental gain. This will stabilize the oscillation amplitude and prevent it from growing further.

2.6 SIMULATION RESULTS

The simulations were done in a *180nm* CMOS process. Few important simulation results are presented in this section.

Figure 9 shows the output current, i_{out} for both the inverting and non-inverting transconductance elements. The application requires an output signal swing of *10mV* - *50mV* peak-peak. As we can see, the currents are linear for a swing of +/- *100mV* around the V_{LT}. This ensures that the resistor is linear when the signal changes around the V_{LT}. The plots are obtained for a bias current of *10uA*. The solid line is the output current of the inverting transconductance and the dotted line is that of the non-inverting transconductance.

The Wien Bridge network produces both in-phase and quadrature components (Sine and Cosine) as required by the application [1]. The voltages, V_{R2} and V_{C2} are taken across *R2* and *C2* of Figure 6 respectively. The corresponding plots are shown in Figure 10. V_{R2} and V_{C2} are in perfect quadrature because they are taken across a resistor *R2* and a capacitor *C2* having the same current i_3 flowing through them.

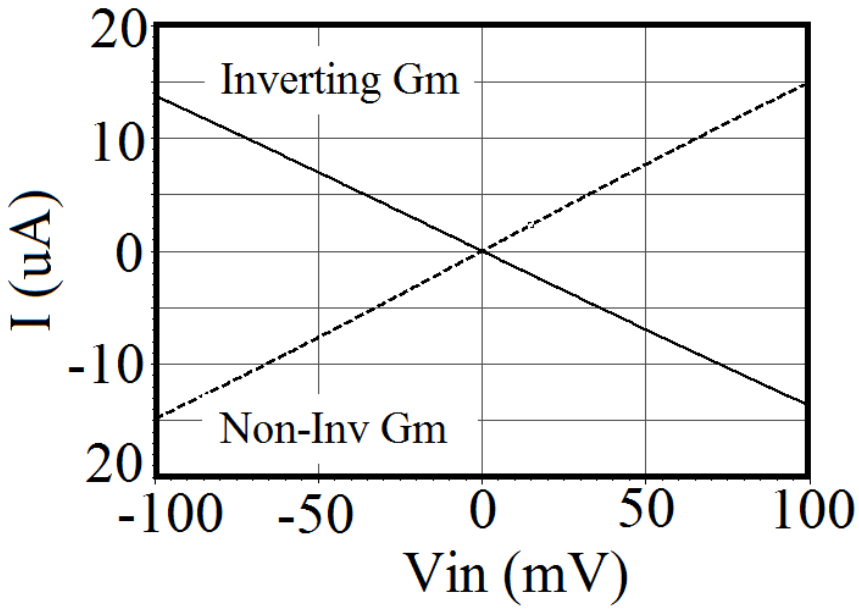

Figure 9: Output Current plots for the inverting and Non-inverting transconductance.

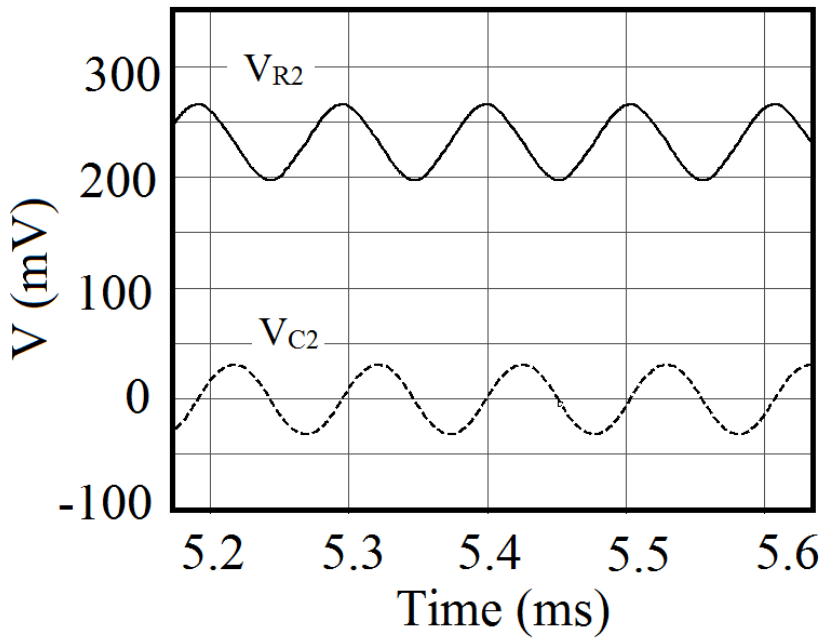

Figure 10: Sine and Cosine waves across *C2* and *R2* at 10kHz.

The transfer characteristics of the squarer circuit is shown in Figure 11. The output current is shown as a solid line. The *i-v* relationship is square-law with respect to the input voltage *v*. The output voltage of a diode-connected complementary circuit (dotted line) driven by a square law current is linear with respect to *v*.

In our application, frequency sweep across the entire range of *1kHz* to *10MHz* is very important. The linearity of the sweep is not necessary [1] as the digital circuits incorporated in the spectroscopy chip will measure the frequency of oscillations. Figure 12 shows Frequency v/s Control current. The current sweeps from *1nA* to *25uA* to get the required frequency range. Note that the frequency is proportional to current at low bias currents. This suggests that the transistors are operating in their sub threshold region where the device characteristics are exponential. In this region, the transconductances are proportional to the bias current.

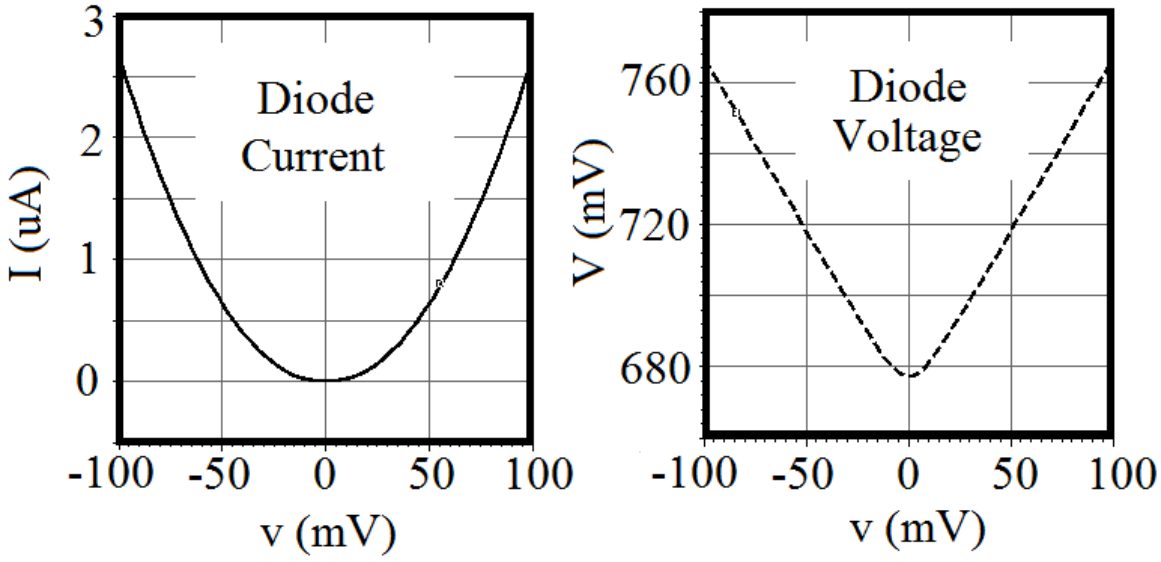

Figure 11: Transfer Characteristics of the Squaring Circuit.

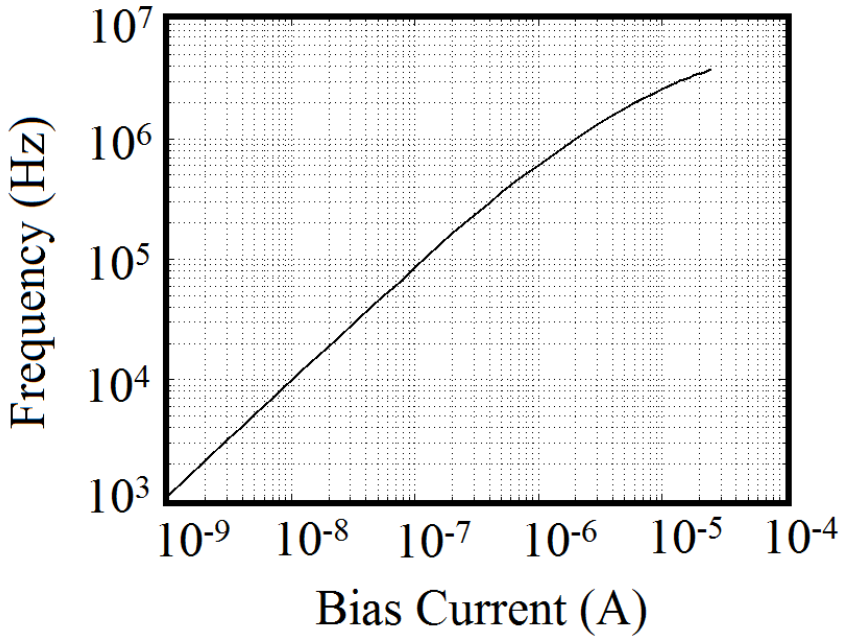

Figure 12: Frequency Sweep of the Wien Bridge Oscillator.

The purity of the sine wave output is very important for many applications. The application requires a sine wave with a THD better than *-25dB* [1]. Several simulations results across process corners and temperatures yielded a THD below *-32dB*. This meets the requirement for impedance spectroscopy.

2.7 CONCLUSION

A novel technique of using CMOS inverter-based transconductances having a wide tuning range has been presented. A new non-inverting transconductance element with high output impedance and wide bandwidth has been discussed. A new circuit that provides an output current proportional to the square of an input signal voltage is explained. Simulation results show that THD below *-32dB* across process and temperature variations can be achieved meeting the requirements of the target-application. The simulated power consumption is *0.5mW* and the estimated area is *150um* x *100um* in a typical *180nm* process.

Chapter 3 : LC Oscillator

3.1 ARCHITECTURE:

The problem statement of this thesis requires a tunable sinusoidal oscillator with very low levels of distortion. This chapter deals with the LC oscillator architecture for the realization of the sinusoidal oscillator. Creating inductors on chip is expensive in terms of chip area costs. In order to realize large inductance values on chip, a capacitor is gyrated to obtain an inductor, and is tuned with another capacitor to make an LC resonant circuit. The chapter discusses the design of the gyrator and techniques used to improve the harmonic distortion of the sine wave.

3.2 GYRATOR:

A gyrator is a two terminal network, whose basic operation is that of an impedance inverter. Figure 13 shows the generic circuit of a gyrator. The impedance to be inverted, Z_{LOAD} is connected as shown. For the sake of the simplicity of analysis, the transconductance elements (g_m blocks) are assumed to be ideal for now. g_{m1} is a non-inverting transconductance element and g_{m2} is an inverting transconductance element. An ideal g_m block has zero output conductance and infinite input impedance. With these idealizations, it is clear that the current through the load Z_{LOAD} is given by $i_{load} = g_{m1} v_{in}$. This creates a voltage on the load, $v_{load} = g_{m1} v_{in} Z_{LOAD}$. The inverting transconductance element g_{m2} converts this voltage to a current i_{in}, which is given by $i_{in} = g_{m2} v_{load}$. Hence, the impedance seen looking into the input of the gyrator is $Z_{in} = 1/(g_{m1} g_{m2} Z_{LOAD})$.

Clearly, the gyrator inverts the impedance Z_{LOAD} and scales it with the product of g_{m1} and g_{m2}. So, when a capacitor ($Z_{LOAD} = 1/s*C_{LOAD}$) is connected as the load, it transforms into an inductor at the input ($L = s*C_{LOAD} / g_{m1}\, g_{m2}$).

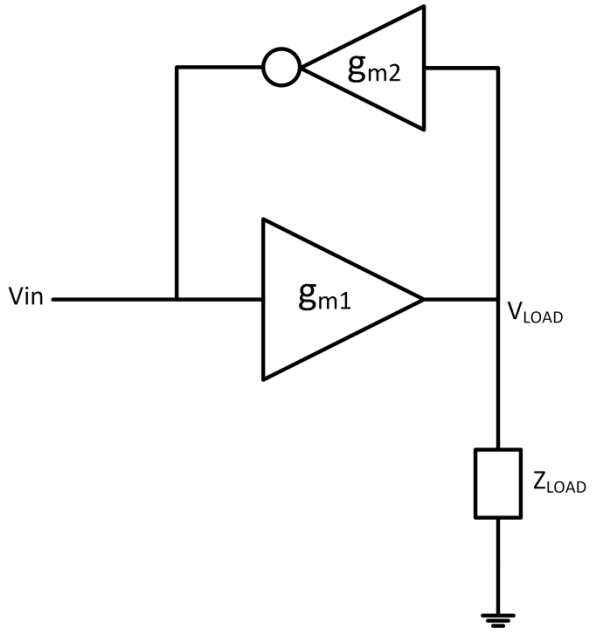

Figure 13: Gyrator - A basic understanding

In a conventional LC tank oscillator, the frequency of oscillations is varied by varying the capacitance *C*. A varactor, which is generally a MOS capacitor, changes its capacitance when the biasing voltage changes, thereby allowing a change in the frequency of oscillations. The capacitor always needs a bias voltage. and must be biased in strong inversion or accumulation region of the MOSFET to get a large value of capacitance.

The advantage in using a gyrated inductor is that the obtained inductance is a function of g_m, which can be varied by changing the bias currents through the it. The circuits used to realize the g_m for the LC oscillator will be discussed later in the chapter.

Figure 14 shows realization of an inductor with a gyrator. The load Z_{LOAD} is replaced with a capacitor. The equivalent inductance obtained is $L = C_2 / g_{m1} g_{m2}$. Clearly, the inductance can be changed by changing g_m.

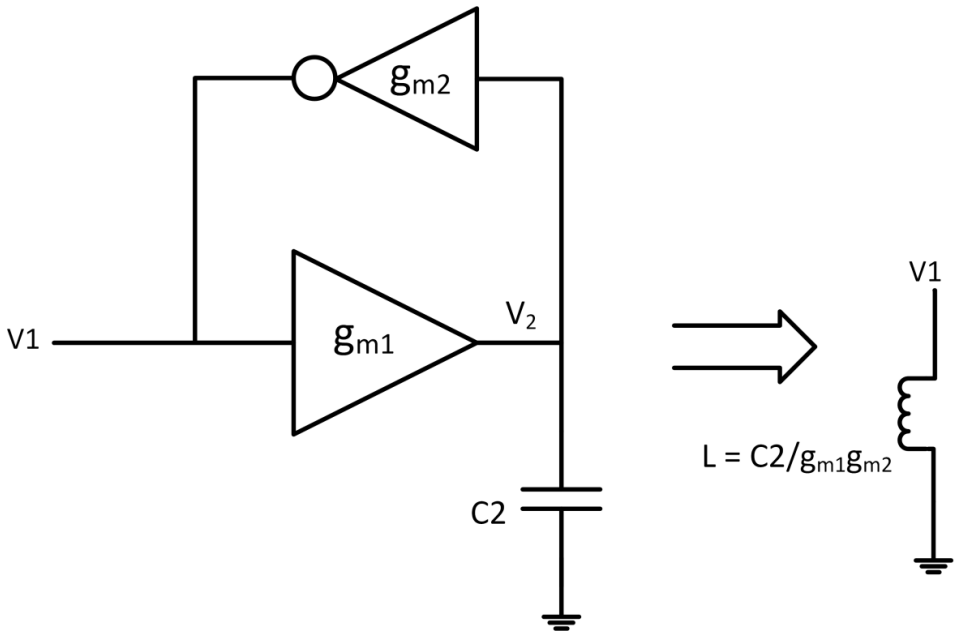

Figure 14: Gyrating a capacitor to obtain an inductor.

In this analysis, the transconductance elements were assumed to be ideal, which is far from reality. In the later part of the thesis, non-idealities like finite output conductance, bandwidth limitation of the g_m blocks, inherent delays in routing the wires connecting the capacitors/transconductance blocks etc will be modeled and included. The *Q* factor of an inductor is defined as $(2\pi fL)/R$, where *R* is the resistance in the inductor and *"f"* is the operating frequency. It should be noted that the *Q* of the obtained inductor is infinite as $R = 0$. Once non-idealities of g_m and *C* are included, a change in the *Q* factor of the inductor will become evident.

Once the inductor is realized, an LC tank can be constructed as shown in Figure 15. The frequency of the oscillations will be $w = gm/C$ (assuming $g_{m1} = g_{m2} = g_m$ and C_1

$= C_2 = C$). This is annotated in the figure. g_m is designed to be a function of the control current (bias current). So, by changing the bias current, the g_m and hence, the frequency of oscillation can be changed.

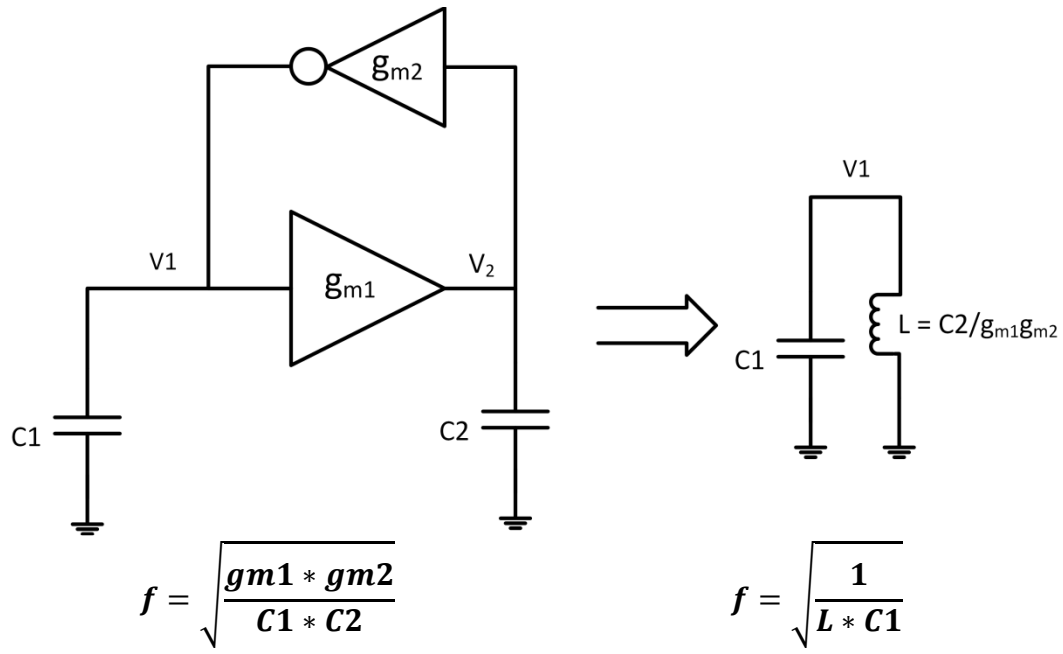

Figure 15: Illustration of a gyrated LC Tank.

To start the oscillations, a small negative resistance is needed in parallel to the LC tank circuit. Due to the negative resistance, it can be easily shown from network theoretical analysis that the poles of the circuit is in the right half plane (RHP) of the s-plane. It is well known that RHP poles makes the oscillations grow exponentially. The negative resistance is killed when sufficient amplitude is reached. At this point, the poles fall back to the *jw* axis. Poles on the *jw* axis maintains steady oscillations.

3.3 NON-IDEALITIES IN A GYRATOR

In the previous analysis, the transconductance blocks were assumed to be ideal, being independent of frequency of operation and with infinite output conductance. This gave us an infinite-Q inductor. In this section, we analyze the behavior of the gyrator and the quality of the inductor produced when non-idealities like finite output conductance and finite bandwidth effects of g_m is brought in the picture. This allows a designer to get a perspective of how critical the elements like output conductance / bandwidth etc are for determining the quality factor of the inductor.

Figure 16 shows the output conductance g_{o1} of the transconductance block g_{m1} being considered for analysis. This comes in parallel with the capacitor C_2 as shown, where $R_{01} = 1/g_{01}$ and $R_{02} = 1/g_{02}$. The inductor obtained by gyration will now have a series resistance whose value is given by $1/g_{m1}g_{m2}R_{01}$, degrading the Q of the inductor. The Q of the inductor (assuming $g_{m1} = g_{m2} = g_m$ and $C_1 = C_2 = C$) will be given by $Q = g_m/g_{o1}$ at the frequency of oscillation $w = g_m/C$. The output conductance g_{02} of the inverting transconductance block g_{m2} will occur in parallel to C_1. In order to get the circuit to oscillate, a negative resistance is always needed to cancel both R_{01} and R_{02}. This negative resistance (R_{neg}) is added in parallel to C_1. Simple analysis would show that for the oscillations to start, the condition $C_1R_2 + C_2R_{01} < 0$, (where R_2 is a parallel combination of R_{02} and R_{neg}) must be satisfied so that the poles move to the right half plane. Once the oscillations start, to maintain a steady amplitude, $C_1R_2 + C_2R_{01} = 0$. Note that the DC loop gain is negative and its magnitude $|g_{m1}R_{01}g_{m2}R_2| > 1$ must be true. The -ve resistance needed for sustaining oscillations is easily computed.

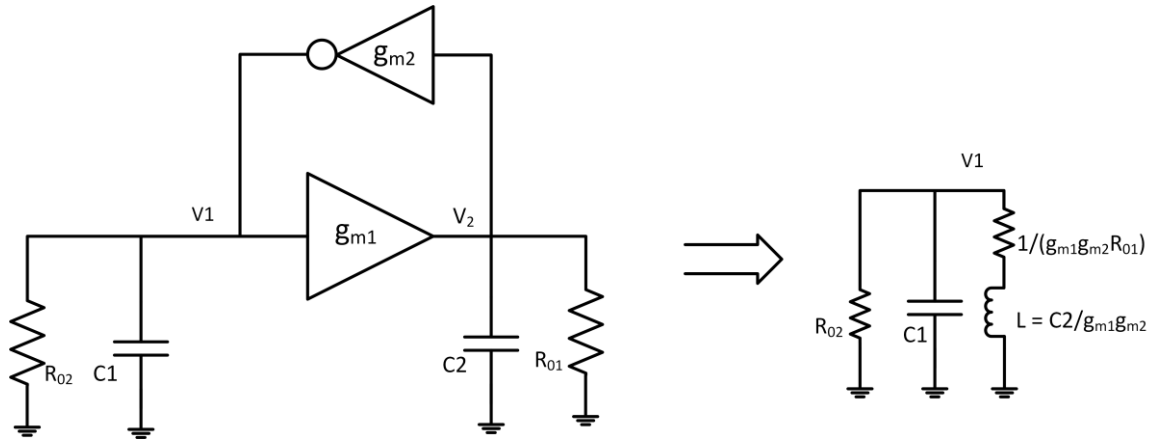

Figure 16: Effects of Output Conductance

We now consider the effects of finite bandwidth with finite output conductance of the transconductance blocks. Let the non-inverting transconductance block, g_{m1} be modeled as $g_{mBW} = g_{m1}/(1+s/\omega_p)$. Figure 17 shows the inductor L, realized by gyrating C_2 when a bandwidth-limited transconductance element with finite output conductance is used.

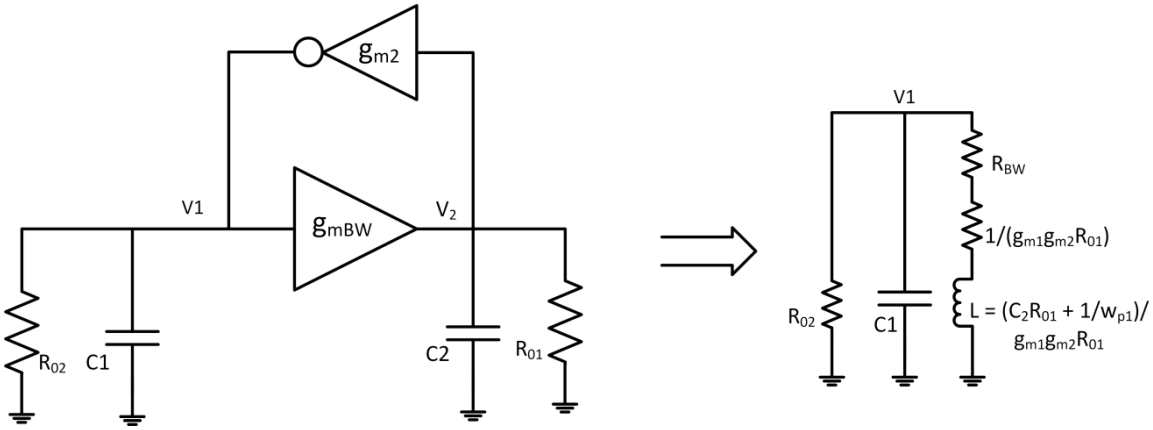

Figure 17: Effects of finite bandwidth of g_m

Bandwidth limitations of the g_m element introduces an additional resistor, R_{BW} which is a Frequency Dependent Negative Resistance (FDNR) whose value is given by

$R_{BW} = -\omega^2 C_2 / g_{m1} g_{m2} \omega_{p1}$. It also changes the value of the inductance slightly but considering the product of C_2 and R_{01} which is practically very large compared to $1/\omega_{p1}$.

From this analysis, we see that to get a high Q inductor, the design effort must focus to reduce g_{01}. A discussion on the design of such transconductance block will be discussed in the next section.

3.4 TRANSCONDUCTANCE ELEMENTS:

The gyrator is built with two transconductance elements. The important factors to consider while designing the g_m elements is the output conductance and the bandwidth of the g_m blocks as explained before. The architectures for realizing a transconductance block has been explained in Chapter 2, Section 3. The same circuit will be used in the design of the LC Oscillator. The inverting transconductance (g_{m2}) of Figure 15 is implemented as shown in Figure 3a and the non-inverting transconductance (g_{m1}) is implemented as shown in Figure 4a. The biasing circuits, based on varying the supply voltage of an inverter by changing the bias current still remains the same as in Figure 5.

Quiescence cancellation in g_{m1} allows us to have very low g_{01} and hence, the Q of the inductor obtained by gyration will be very large (because $Q = g_m/g_{01}$ at the frequency of oscillation). The use of minimum sized mirrors helps to keep the bandwidth as high as possible.

3.5 SHUNT SCALING

To achieve low frequencies of oscillation, we need large capacitances. In this section, we present a new technique of scaling the capacitance using shunt feedback. In the well known Miller multiplication shown in Figure 18, the capacitor C across a gain

block of gain *-A* will look like *(1+A)C* at the input of the gain block. This structure provides a grounded capacitance of value *(1+A)C*. This scaling is brought about because the voltage swing around the capacitor is boosted up by a factor *(1+A)*. From the figure, $Vx = -AV_{in}$ making the voltage across the capacitor to be $(1+A)V_{in}$. This makes Miller multiplication of capacitance a voltage-mode operation.

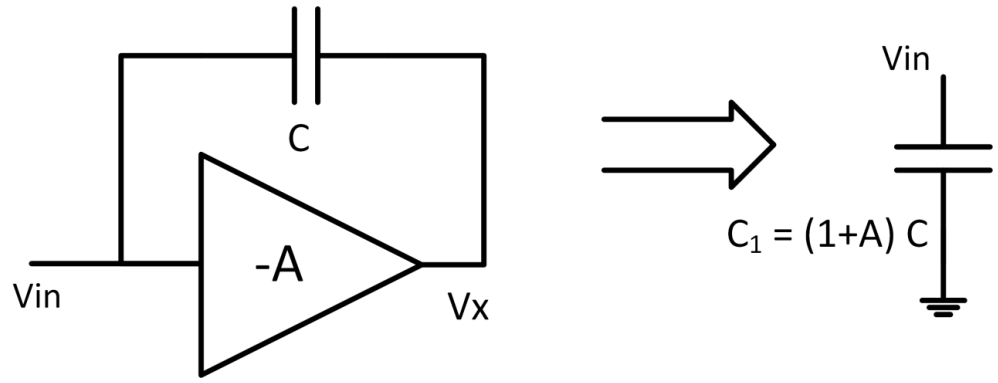

Figure 18: Miller Multiplication to scale capacitance

In modern CMOS processes, PVT variations causes significant change in parameters of a transistor and hence, the gain *A*. Negative feedback around a large gain OPAMP to realize a finite scale factor *A* would consume a large amount of power. Figure 19 shows a technique of obtaining a finite, PVT tolerant gain. The obtained scaled capacitance, C_1 is given by $C_1 = (1+g_{m1}/g_{m2})C$. The gain/scaling factor $(1+g_{m1}/g_{m2})$ is a ratio of the transconductances g_{m1} and g_{m2}, both of which will scale with PVT, improving the PVT tolerance of the circuit. The value of C_1 is purely capacitive as long as the gain *A* is large. V_x is required to be at virtual ground for all practical purposes, so that the output conductance of g_{m1} and g_{m2} blocks wouldn't affect the gain much. This is possible when

A is large. From the figure, basic analysis yields the following results. $V_x = -(g_{m1}/Ag_{m2})V_{in}$ and $V_y = -(g_{m1}/g_{m2})V_{in}$.

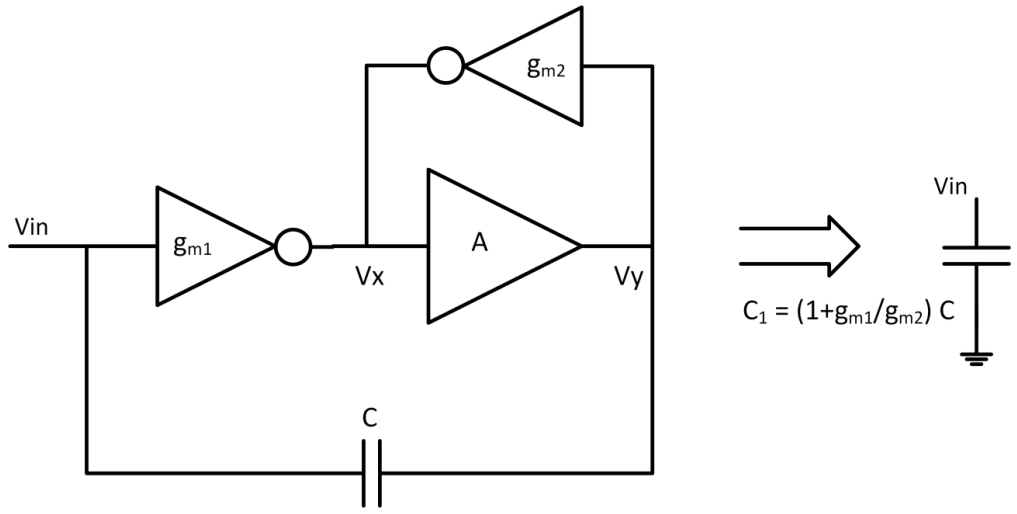

Figure 19: Miller Multiplication with a PVT tolerant gain.

As the supply voltage scales down, it would be difficult to support large signal swings at the output of the gain elements, making Miller multiplication to scale the capacitance becomes difficult in a low supply voltage technology. In Figure 20 we present a technique which uses current mode techniques to scale the capacitance. The current through the capacitor *C* is sensed. For a sufficiently large gain *A*, *Vx* can be assumed to be at virtual ground. The current I_C through the capacitor *C* flows through g_{m2}. If *Vx* is at virtual ground, it wouldn't load the capacitor to sense the current. This generates a voltage, $Vy = I_C / g_{m2}$. Thus, the total current drawn from the input V_{in} would be $I_{in} = I_C + g_{m1}Vy$. Hence, the effective capacitance gets scaled by a factor $(1+g_{m1}/g_{m2})$.

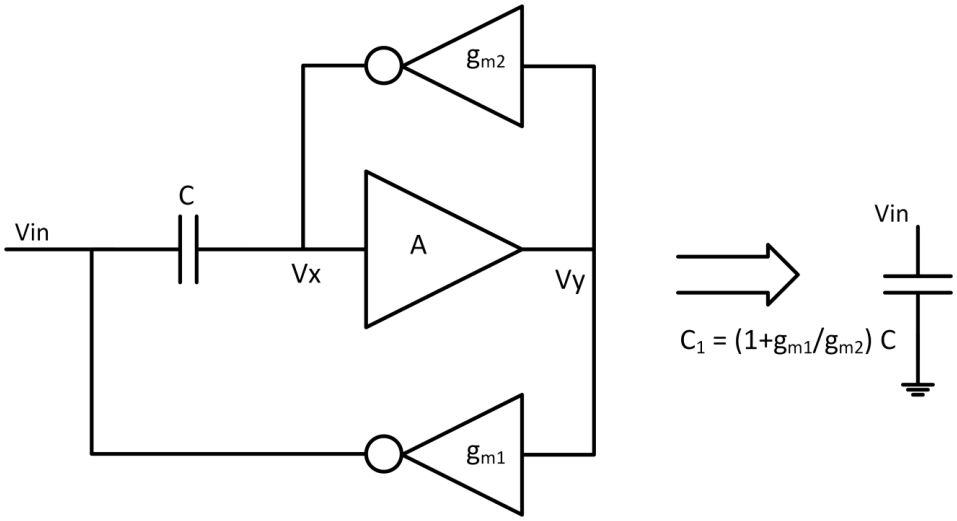

Figure 20: Shunt Scaling for boosting Capacitance.

The key feature of this circuit is the use of current-mode operation for scaling the capacitance. In the analysis, it was assumed that *Vx* is at virtual ground by considering a large gain *A*, which made the loading effect on the capacitor to be 0. In reality, the capacitor will be loaded when the current is sensed because of finite impedance seen at *Vx*. The impedance seen by the capacitor is $1/Ag_{m2}$. In the final expression of the impedance seen at the input, this shows up as a resistor, $R = 1/A(g_{m1}+g_{m2})$ in series with the scaled capacitance C_1, degrading the *Q* of the capacitor. So, the choice of *A* depends on the application and available error tolerance for this block. If a high Q capacitor is needed, *A* should to be increased. If the amplitude of interest is small, scaling the capacitance by Miller multiplication would yield a high Q capacitor than shunt scaling.

3.6 OSCILLATOR STRUCTURE

In this section, the dynamics of the oscillator is explained. For the oscillations to start and be sustained, we already saw the need of a negative resistance. This is obtained by applying a feedback on a non-inverting g_m element. The value of the negative

resistance thus obtained would be $R_{NEG} = -1/g_{m3}$ and is as show in Figure 21. The final oscillator block diagram is also shown.

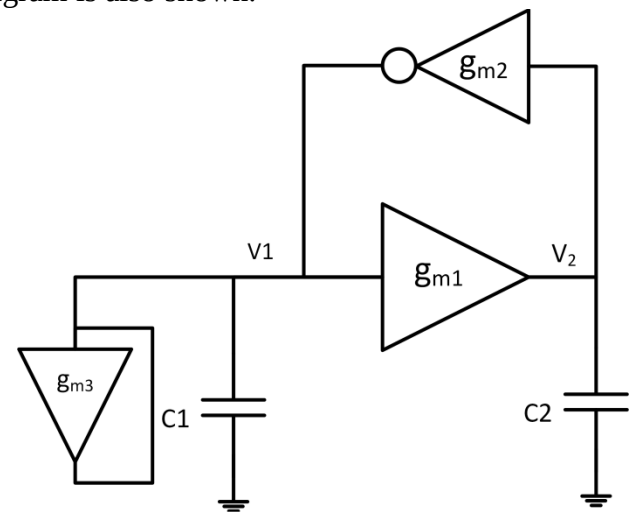

Figure 21: LC Oscillator Block Diagram

When the oscillator circuit is powered on, the output conductance g_{01} and g_{02} are small compared to g_{m3}. Hence, the negative resistance R_{NEG}, ($R_{NEG} = 1/g_{m3}$) is small compared to R_{02}. The effective negative resistance, R_2 is a parallel combination of R_{NEG}, R_{02} and R_{03} ($R_{03} = 1/g_{03}$) which is the output impedance of g_{m3}. This value turns out to be a negative number as long as $R_{NEG} < R_{02}||R_{03}$. From Section 3.4, we saw that for the oscillations to start, $C_1R_2 + C_2R_{01} < 0$. This condition can be easily met when the magnitude of R_2 is sufficiently large since R_2 is negative.

As the amplitude of oscillation starts to grow, the output conductances g_{01}, g_{02} and g_{03} increases because of the signal induced DC component. Hence, R_2 changes to a point where the condition $C_1R_2 + C_2R_{01} = 0$ becomes true. At this point, the poles are on the jw axis. If the amplitude changes further, then $C_1R_2 + C_2R_{01} > 0$ making the poles to move to the left half plane. Thus, the amplitude stabilizes and remains constant. In summary, we use the direct dependence of output conductance on the quiescent current to stabilize

the amplitude of oscillation. The quiescent current increases with the amplitude of oscillation due to the nonlinearity of the FET namely the square law. This technique has been well described in [6]. In essence, the amplitude of oscillation is proportional to the negative conductance ($1/R_{NEG}$).

Figure 22 shows the circuit schematic of the oscillator. V_{LT} and *VDDa* are generated from the biasing circuit discussed in Chapter 2. The non-inverting transconductance element g_{m1} is implemented with the transistors *P1- P4* and *N1 - N4* as shown. Transistors *P2* and *N2* remove the quiescence and makes the output conductance at V_{out2} very small. This was explained in great detail in Chapter 2. Transistors *P5* and *N5* form the inverting transconductance element g_{m2}. The capacitance chosen is 10pF due to area limitations.

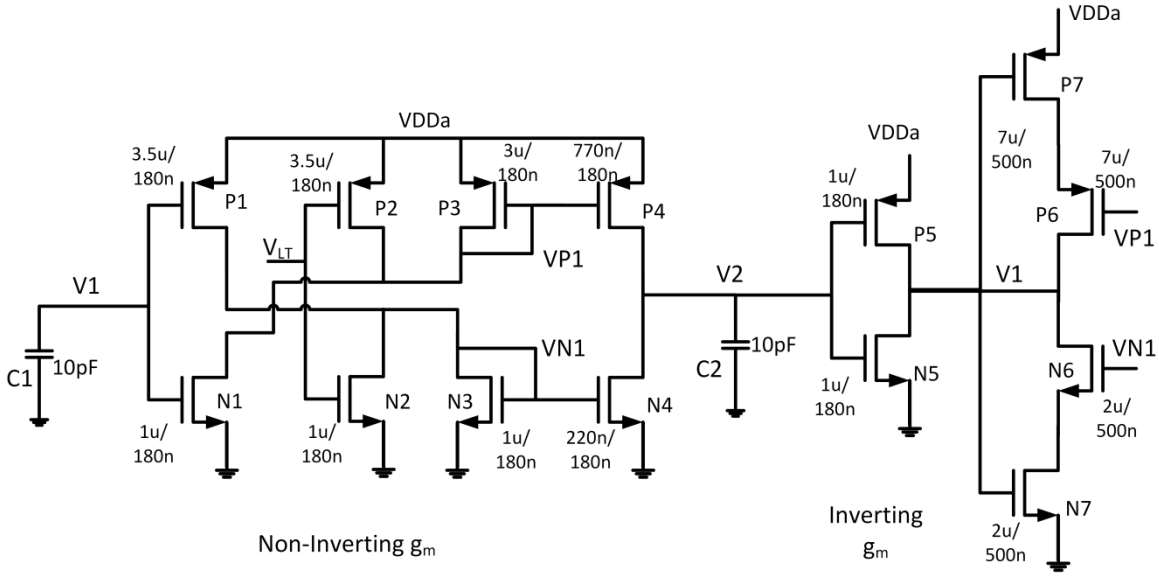

Figure 22: Circuit Diagram of the LC Oscillator.

From Figure 21, we saw that a feedback around a g_m element realizes a negative resistance of value $R_{NEG}=1/g_{m3}$. We notice that both g_{m1} and g_{m3} share the same input and since both are non-inverting transconductance elements, the transistors *P1*, *P2*, *P3*, *N1*,

N2, *N3* can be shared. Thus, g_{m1} is formed by the transistors *P1* - *P4* and *N1* - *N4* and g_{m3} is formed by *P1* - *P3*, *P6*, *P7* and *N1* - *N3*, *N6*, *N7*. This reduces the area requirement and power significantly. The nets V_{P1} connects the gate of both *P4* and *P6*, V_{N1} connects the gate of both *N4* and *N6*.

The negative resistance element is degenerated. This degeneration is provided by *P7* and *N7* as shown, in order to limit the amplitude of oscillation. The degeneration is not achieved with a constant gate bias to *P7* and *N7*, but rather making them signal dependent to make the degeneration more effective. When V_1 increases, V_{P1} reduces. So, for effective degeneration, the gate voltage of *P7* has to increase, making *P7* less conductive. So, by tying up the gate of *P7* to V_1, we achieve the task of pulling the gate high. By degenerating, we reduce g_{m3}. This means that R_{NEG} is very large. So, when the effective -ve resistance R_2 is considered, the condition $C_1R_2 + C_2R_{01} = 0$ can be achieved at a smaller amplitude. The amplitude of oscillation is proportional to the negative conductance g_{m3}. By degenerating the negative resistance, i.e. decreasing the value of g_{m3}, the amplitude of oscillation is reduced, in turn reducing the distortion.

3.6 SIMULATION RESULTS

An important factor in the design of a gyrated inductor is the Q of the inductor. Figure 23 shows the plot of the Q of the inductor obtained by gyration when tuned with a capacitor. The circuit setup is as shown in Figure 15. This Q is plotted against the bias current used to vary the transconductance of the gyrator. It can be clearly noticed that the Q degrades for low currents and as the bias currents increases, the Q of the inductor improves. This is an indicative that the distortion at higher frequencies is less than that at lower frequencies.

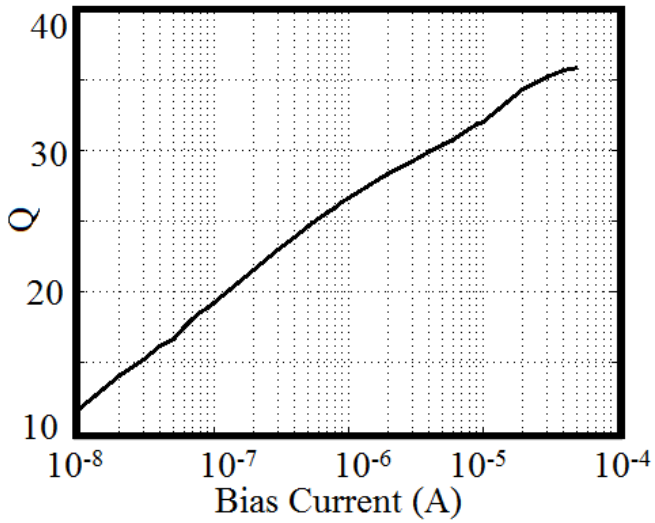

Figure 23: Q of the tuned circuit v/s Bias Current.

Figure 24 shows the I-V characteristics of the negative resistance block. It is clear that due to degeneration, the I-V relation becomes non-linear and the gain reduces as the voltage increases. This is a key factor limiting the amplitude of oscillation.

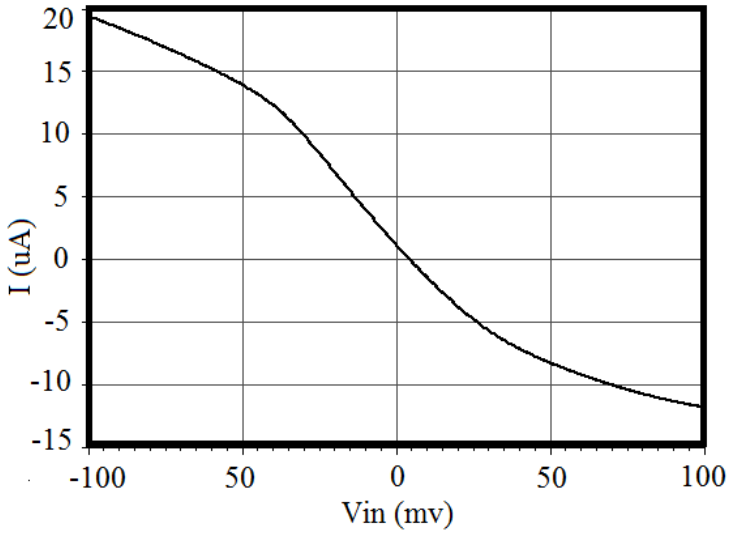

Figure 24: I-V Characteristics of negative Resistance

The obtained sine waves (V_1) is shown in Figure 25. The sine waves are at a frequency of 5MHz. The Total Harmonic Distortion (THD) of the obtained sine wave was found to be -32dB.

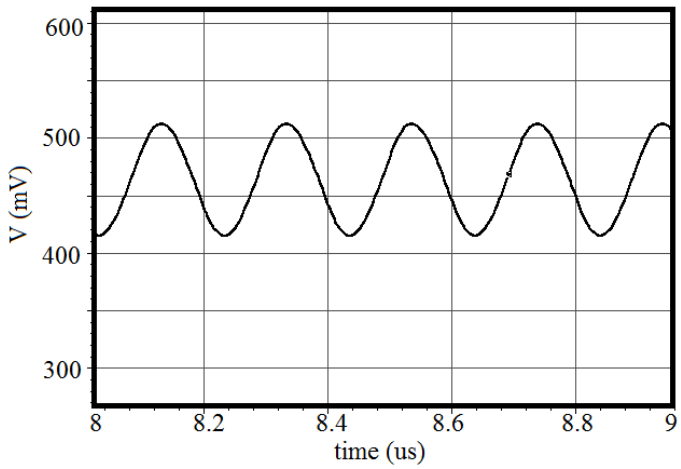

Figure 25: Sine wave output of the LC Oscillator

To obtain different frequencies, the bias current is changed from 10nA to 40uA. The Frequency-Bias current relation is plotted in Figure 26. It is clear that the relation is linear (the plots are in log-log scale). The frequency of oscillation in the gyrator is given by $f = g_m/2\pi C$. g_m is a linear function of the input bias current in sub-threshold region and varies as square-root of the bias current in strong inversion. The plot clearly specifies that a wide range of low-frequencies are obtained by operating the transistors in sub-threshold region where the transconductance is proportional to the bias current. As the bias current increases, the devices move to strong inversion and the frequency is no longer a linear function of the bias current.

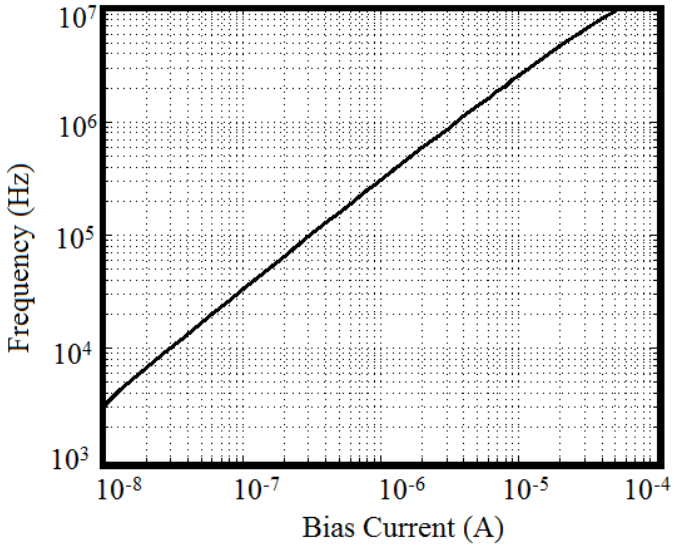

Figure 26: Frequency of Oscillation v/s Bias Current

From extensive simulations, it was observed that the Total Harmonic Distortion of the sine wave is better than -30dB across the entire dynamic range.

Chapter 4: Future Work and Conclusion

Few directions for future work to improve the performance of the oscillator will be illustrated in this chapter.

4.1 Cascaded Wien Bridge Network

From Table 1, we saw that the transfer function of I_3/I_{in} is a bandpass response with 2 poles. The Q of this response can be improved by having fractal stages as shown in Figure 27. A single stage response has a -20dB per decade roll off from the center frequency. By cascading multiple stages as shown, the roll off gets scaled by the number of stages. In other words, I_{33}/Iin will be a 6 pole bandpass response with a sharp roll off of -60dB per decade from the center frequency.

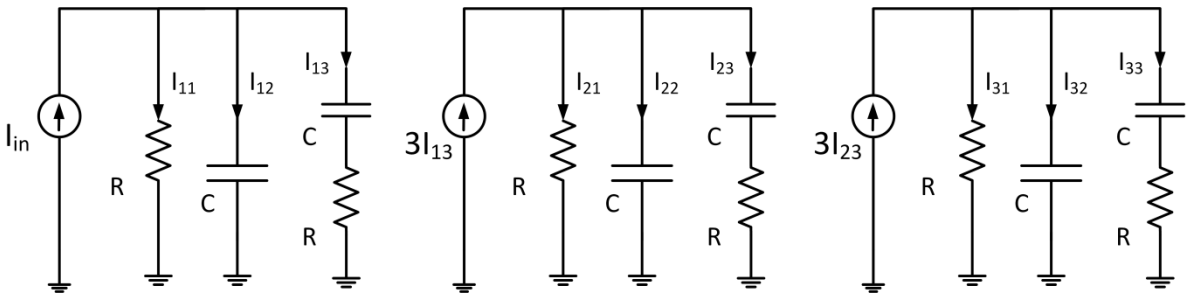

Figure 27: Cascaded Wien Bridge Network

This architecture can have a better distortion specification compared to the single stage counterpart. It manifests as a direct trade-off between power and distortion. Having 3 stages will triple the power consumption. This is something which future designers can look forward to and try to improve the power/performance metrics.

As stated in Chapter 2, the gain relation which is given by $I3 = \frac{Iin}{\frac{C1}{C2}+\left(1+\frac{R2}{R1}\right)}$ can have an alternate solution where $I_3 = -I_{in}$ when $C_1 = -C_2$ and $R_2 = -R_1$. The implementation

of a negative *R* and *C* consumes more power than gaining the signal by a factor of 3. If new techniques to implement a negative *R* and *C* which consume less power is designed, it could substitute the requirement for a gain of 3 in the Wien Network.

4.2 LINEAR TRANSCONDUCTANCE ELEMENTS

Linear transconductance elements, which can maintain its linearity across a wide input range is required in order to get a very low distortion oscillator. An NMOS or a PMOS transistor as such will have poor linearity compared to the inverter used in this design. The problem with the inverter is the inherent mismatch between the PMOS and NMOS transistor, which makes it hard to match them and maintain a linear g_m across a wide range of inputs.

Figure 28 shows the design of a linear transconductor, which makes use of just NMOS devices to obtain higher linearity. The idea behind this circuit is the following. Following the convention introduced in Chapter 2 Section 3, when *f(v)* and *f(-v)* are subtracted, the even components disappear. Here $f(v) = f_{even}(v) + f_{odd}(v)$. In an inverter, the NMOS generates *f(v)* and PMOS generates *f(-v)*. The problem with this is getting *f(v)* due to PMOS the same as *f(v)* due to NMOS. In the circuit of Figure 28, we make sure that both *f(v)* and *f(-v)* is being generated by a NMOS, so that we do not have a problem of matching the NMOS and PMOS.

A current $i_1 = f(v)$ is generated by the transistor *N2*. Transistors *P2* and *PN3* are used to generate *-v,* which is a unity-gain inversion. The connection forms a gain stage whose gain is given by g_{mP2} / g_{mPN3} ignoring channel length modulation. We need to make sure that the gain is unity across a large range of input signals. This inverted signal is then applied to *N4*, which generates $i_2 = f(-v)$. Note that the DC gate bias of *N2* is at

V_{LT}. So, the source of *PN3* (which is connected to the gate of *N4*) must be at a DC potential equal to V_{LT}. This is possible when *P2* and *PN3* are sized the same and when $VDDa = 2xV_{LT}$. Current i_1 is inverted using the current mirrors *P3* and *P4*. i_{out} is then given by i_2-i_1. Hence, the even components are canceled out, making the circuit more linear.

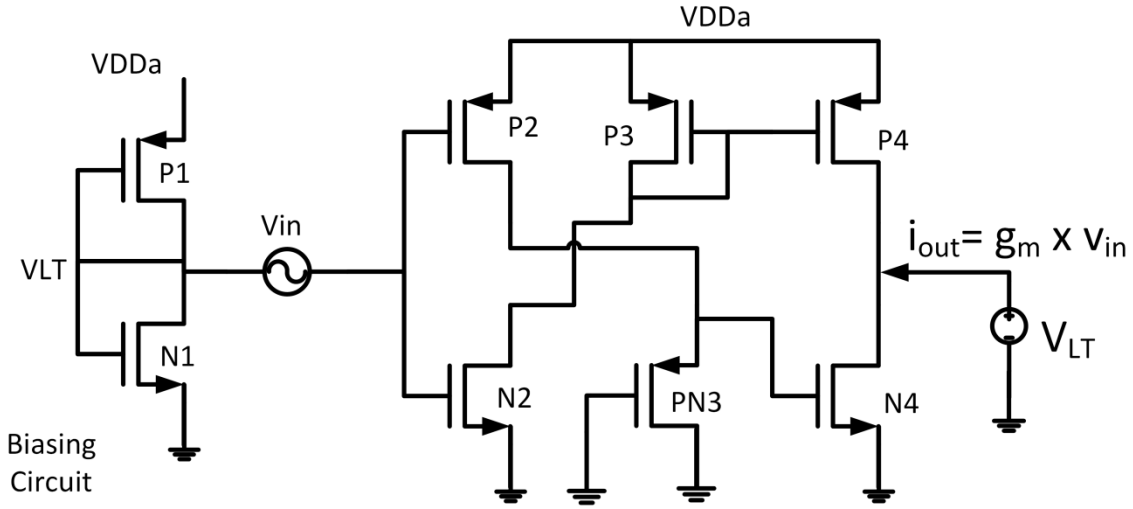

Figure 28: Inverting Transconductance Element

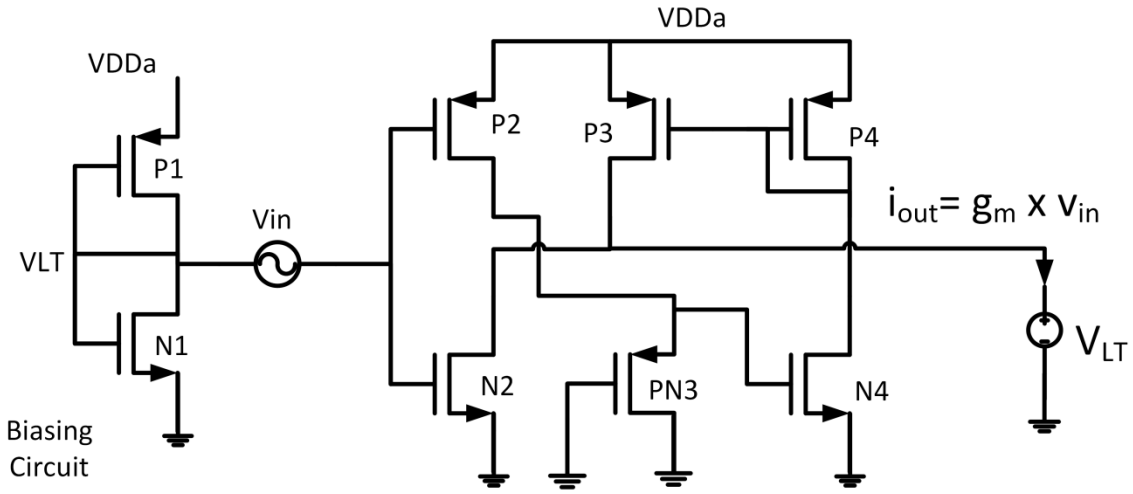

Figure 29: Non-Inverting Transconductance Element

Figure 29 shows a non-inverting transconductance element based on the same principles. Here, instead of inverting i_1 using the mirrors, i_2 is inverted. Hence, $i_{out} = i_2 - i_1$, making the circuit a non-inverting transconductance block.

The squarer circuit described in Chapter 2 can be further improved using the above idea. To obtain a transconductance element, the 2 currents, i_1 and i_2 are subtracted, which cancels the even component. To make a squarer, the two currents are to be added. The addition can be done by just tying the outputs of *N2* and *N4*. Techniques of removing the DC component, taking the square root etc has already been described in Chapter 2. The problem with designing a complementary circuit for taking the square root is the following. The circuit will use PMOS transistors to create *f(v)* and *f(-v)*. Generating *-v* with NMOS transistors using a g_m/g_m technique faces problems of back gate bias unless an expensive triple well process or an SOI process is used. This is something which future designers can explore further.

4.3 LC Oscillator Improvements

The Q of the obtained inductor is highly dependent on the output conductance of gm1 as seen in Chapter 3. This can be canceled using a negative resistance $R=1/g_{m4}$ as shown in Figure 30**.** Lower distortion levels can be obtained by the cancelation. This would be a trade-off with power because of the additional non-inverting g_m block.

To achieve low frequencies of oscillation, we go to very low currents (tens of nano-Amperes). In short channel technologies, the transconductance of devices to start with are very large and leakage issues dominate at low currents, making the problems of generating low frequencies even harder. So, degeneration techniques should be used to limit the g_m of a circuit. Also, in the non-inverting transconductance block discussed in

Chapter 2, the mirror gain can also be used to control the g_m. The mirroring ratio decides what fraction of the signal current reaches the output.

Well known cascoding techniques can be used to reduce the output conductance of the g_m block. Cascoding g_{m1} would be highly important as the g_{01} of this blocks determines the Q of the inductor. The extent of complexities in the circuit entirely depends entirely on the application.

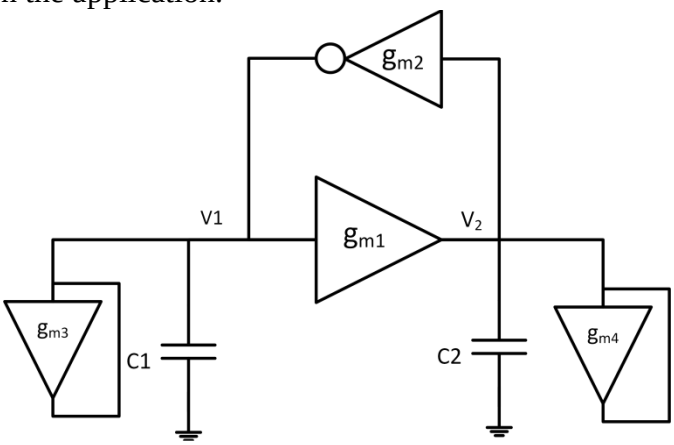

Figure 30: Improvements in LC Oscillator

4.4 CONCLUSION

This thesis focused on designing a low frequency sinusoidal oscillator, with a tuning range of *1kHz* to *10MHz*. Two architectures of oscillators, namely the Wien Bridge and the LC architecture were realized in a *180nm* CMOS process. Novel circuits for linear transconductance elements, squaring circuits, amplitude detection circuits etc has been implemented and explained. Simulation results shows that the Total Harmonic Distortion (THD) was better than -30dB across process and corners, which meets the specifications of the target application.

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Vita

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