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Design of Wide Tuning Range Current-Controlled Oscillator

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Design of Wide Tuning Range Current-Controlled Oscillator

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Dedicated to my parents, F. Mao and all my friends for their support and help.

Abstract

Design of Wide Tuning Range Current-Controlled Oscillator

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This thesis presents a novel current-controlled oscillator (CCO). It charges and discharges a source-coupled capacitor periodically with well-controlled current sources. Its current-to-frequency conversion relies on passive components, which are insensitive to the temperature and process variations. The proposed CCO is compact and area-efficient. Moreover, compared to ring-oscillator and LC-tank oscillator, it exhibits much wider tuning range and better linearity. Therefore, it suits the modern system-on-chip (SoC) design.

This linear CCO can be used for data conversion. Following the oscillator with a digital counter, it is equivalent to an analog-to-digital converter (ADC). This architecture becomes attractive because of its simplicity and digital-intensive nature. For obtaining N-bit resolution, 2^N-1 cycles are counted. By increasing the oscillating frequency, more bits are resolved within certain sampling period. Oscillator-based ADCs are good candidates for high-speed, low-resolution applications, such as serial link and hard-disk drive.

In this thesis, the well-known source-coupled multivibrator is introduced first. We then replace the resistive loads with PMOS transistors operating in saturation region and

its channel length modulation effect makes their output resistance independent of the input current. This enables a constant voltage swing across the integrating capacitor. As a result, the oscillating frequency becomes linearly proportional to the input current.

Quantitative equations are derived to obtain the current-to-frequency conversion gain. We use small-signal model to analyze the conditions for oscillation. Sources of nonlinear current-to-frequency conversion are discussed as well. To address these problems, we propose several analog/mixed-signal techniques including cancellation of effects that cause nonlinearity in the transfer characteristics and replica biasing.

A design prototype is implemented in $130nm$ CMOS technology. Simulation results indicate that this circuit can oscillate up to 2 GHz with 8-bit dynamic range. Furthermore, the current-to-frequency characteristic is insensitive to process and temperature variations. The measured data are in accordance with the simulation results and prove the effectiveness of this novel CCO.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 OVERVIEW

Oscillators are widely used in applications such as phase-locked loops (PLLs), frequency synthesis and clock data recovery (CDR). They generate periodic waveforms that are used as timing references. The voltage/current-controlled oscillators (VCOs/CCOs) are oscillators whose output frequency is controllable by input voltage or current.

In this thesis, we focus on the analysis and design of a linear current-controller oscillator with wide tuning range. First, we revisit the well-known oscillator structure, namely the emitter/source-coupled multivibrator. By replacing the resistive loads with active transistors, we can control the oscillating frequency linearly by changing the input current.

The theoretical equations describing the current-to-frequency conversion are obtained first. Meanwhile, we derive the conditions for oscillation based on small-signal model. The linearity of the CCO is degraded by the circuit non-idealities. Especially at high frequency, it behaves differently from what is predicted by the simple model we used for analysis. To address these problems, we propose several circuit techniques such as nonlinear cancellation, replica biasing and feedback. These techniques are suitable for different applications. For example, the nonlinear cancellation is necessary for high frequency application.

A CCO prototype using nonlinear cancellation is implemented in $130nm$ CMOS technology. Simulation results indicate that it can run up to $2GHz$. The measured results show that this oscillator maintains very good linearity in the frequency range up to $550MHz$. Beyond $550MHz$, its performance degrades due to parasitic and other nonlinear sources.

1.2 MOTIVATION

Recent publications [1]-[10] have revealed that, the VCOs/CCOs can be used in high-performance ADC. In [1]-[8], ring-oscillator replaces the conventional comparator-based multi-bit quantizer in the continuous-time delta-sigma modulator. The architecture presented in [9], [10] digitizes the phase output with a digital counter. This structure is concise and simple because only one precision analog building block, namely a VCO/CCO is required. The resolution of ADC depends solely on the linear tuning range of the VCO/CCO. For an N-bit resolution data converter, the oscillator has to run $2^N - 1$ clock cycles. As an example, for video application, a 20MS/s ADC with 10-bit resolution is required. Therefore, the peak oscillating frequency goes up to $20GHz$.

To design an oscillator for data conversion is quite different from for frequency generation in communication system. The latter one needs an oscillator with very low phase noise. However, for data conversion, wide tuning range and high linearity are more important.

In all categories of oscillator, the ring-oscillator can work over wide tuning range, but is prone to process, voltage and temperature (PVT) variations. The LC-tank oscillator exhibits excellent phase noise performance, but is poor in tuning range and area efficiency. Therefore, we investigate the relaxation oscillator in this thesis. While the phase noise of the relaxation oscillator is inferior to the phase noise of the LC-tank oscillator, it is robust, insensitive to PVT variations and able to operate over wide tuning range with good power/area efficiency.

1.3 THESIS ORGANIZATION

Chapter 2: The history of the emitter/source-coupled multivibrator is revisited. The oscillating frequency is analyzed and discussed.

Chapter 3: The novel current-controlled oscillator is presented. The current-to-frequency conversion gain is derived. Based on the small-signal model, we obtain the conditions for oscillation. We also examine the sources of circuit nonlinear behavior to figure out the trade-offs between tuning range and linearity. To improve the linearity, several circuit techniques are discussed.

Chapter 4: The circuit implementations and layout details are presented.

Chapter 5: Simulation and silicon-measured results are shown. We discuss the reasons for the discrepancies.

Chapter 6: We conclude and summarize our work in this chapter.

Chapter 2: Multivibrator

2.1 INTRODUCTION

Multivibrator is simple and popular. Fig. 2.1(a) shows the block diagram of a classic multivibrator. It consists of a bidirectional current source (I_{in}), an integrating capacitor (C_{int}) and a comparator. The constant current source charges/discharges C_{int} between two well-defined voltages, V_H and V_L. The block diagram shows the two threshold voltages as inputs to the comparator, which is assumed to act instantaneously. The waveforms of the charging current and voltage on C_{int} are plotted in Fig. 2.1(b). The voltage exhibits a triangular shape waveform bounded by V_H and V_L.

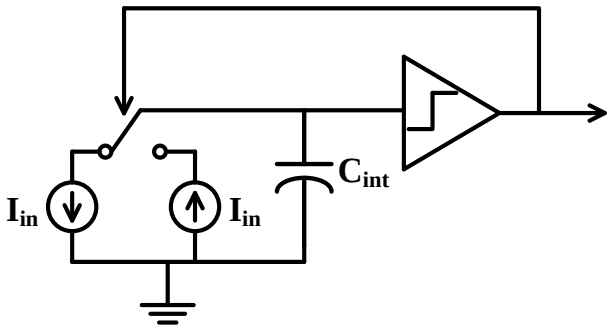


Fig. 2.1(a) Block diagram of a classical multivibrator.

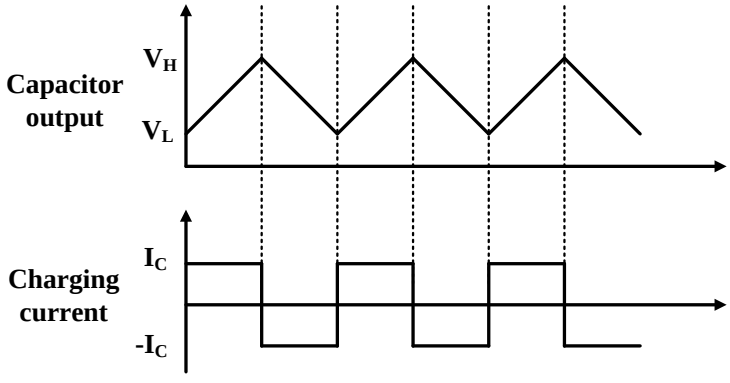


Fig. 2.1(b) Waveforms of the output voltage and charging current.

2.2 EMITTER-COUPLED MULTIVIBRATOR

The emitter-coupled multivibrator was proposed in 1950s and first implemented based on bipolar-junction-transistors (BJTs) [11]. Fig. 2.2 shows the schematic of a fully differential emitter-coupled multivibrator. It consists of two load resistors R, a BJT cross-coupled pair $Q_1$and Q_2, an emitter-coupled integrating capacitor C, two current sources (implemented with BJTs) and two voltage level shifters. To calculate the period of oscillation, we assume that the circuit is fully symmetrical. Initially, Q_1 is off and Q_2 is on. Since no current go through Q_1, the base and the emitter of Q_2 are $V_{DD} - V_{LS}$ and $V_{DD} - V_{LS} - V_{BE}$ (V_{LS} is the voltage drop of the level shifter), respectively. Meanwhile, the base of Q_1 is $V_{DD} - V_{LS} - 2I_1R$. One copy of current I_1 charges C and this causes the emitter of Q_1 to become more negative. When the emitter of Q_1 is one V_{BE} below its own base voltage, it starts to conduct current. As a result, the multivibrator switches to the other state (Q_1 is on and Q_2 is off). As long as the cross-coupled pair provides enough loop gain, this circuit will toggle between two different states by charging and discharging the capacitor C.

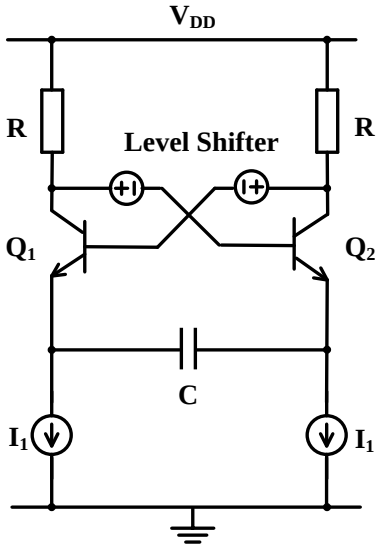


Fig. 2.2 Circuit diagram of an emitter-coupled multivibrator.

In oscillation mode, the voltage swing of the bases of Q_1 or Q_2 is $2I_1R$. Since the voltage drop across the base and emitter stays constant in oscillation, the voltage swing across C also equals to $2I_1R$. Therefore, we can express the oscillating frequency as following:

$$\frac{T}{2} = \frac{2C \cdot \Delta V}{I_1} = \frac{4CI_1R}{I_1} \tag{2.1}$$

$$f = \frac{1}{8RC} \tag{2.2}$$

According to (2.2), the product of the resistance and capacitance defines the oscillating frequency. Therefore, it is insensitive to the temperature variations since passive devices are more temperature-independent compared to active counterparts.

2.3 SOURCE-COUPLED MULTIVIBRATOR

The source-coupled multivibrator, replacing the BJTs in Fig. 2.2 with the CMOS transistors, was proposed in late 80s. The schematic of a source-coupled multivibrator is shown in Fig. 2.3. It is composed of two load resistor R, a CMOS cross-coupled pair M_1 and M_2, an integrating capacitor C and two current sinks. This circuit works in a similar way to the emitter-coupled multivibrator. However, the gate-source voltage drop of M_1 and M_2 is not constant as the input current varies. Therefore, the voltage swing across C is not $2I_1R$ anymore, which complicates the analysis.

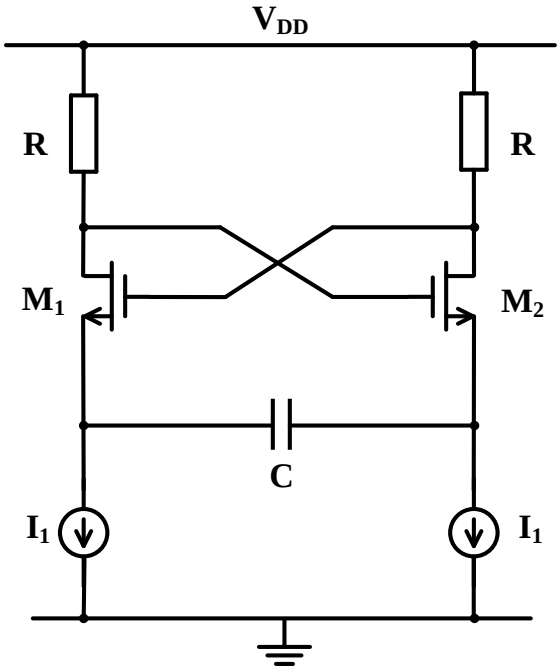


Fig. 2.3 Circuit diagram of source-coupled multivibrator.

In [12]-[14], analytical equations are derived to calculate the oscillating frequency. According to [14], at low frequency, the oscillator behaves similar to what we modeled in Fig. 2.1(a). However, at high frequency, it becomes a sinusoidal (resonance) oscillator. The analytical equation at high frequency is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{g_m}{2RC(C_{gs}+4C_{gd})}} \tag{2.3}$$

Where g_m is the small-signal transconductance of the cross-coupled pair, C_{gs} and C_{gd} are the gate-source and gate-drain capacitance of the cross-coupled pair. According to (2.3), the oscillating frequency is not only dependent on passive components, but also related to the device parameters of M_1 and M_2.

Fig. 2.4(a) and (b) plot the two operation modes (relaxation and resonance) running at $70MHz$ and $900MHz$, respectively. In Fig. 2.4(a), the differential voltage on C ($1pF$) exhibits clear triangular shape and the charging current stays reasonable constant across the period. In Fig. 2.4(b), we use much smaller C ($50fF$). The waveform becomes smooth since the high frequency harmonics are attenuated by the resonance network. The constant charging assumption is not valid here.

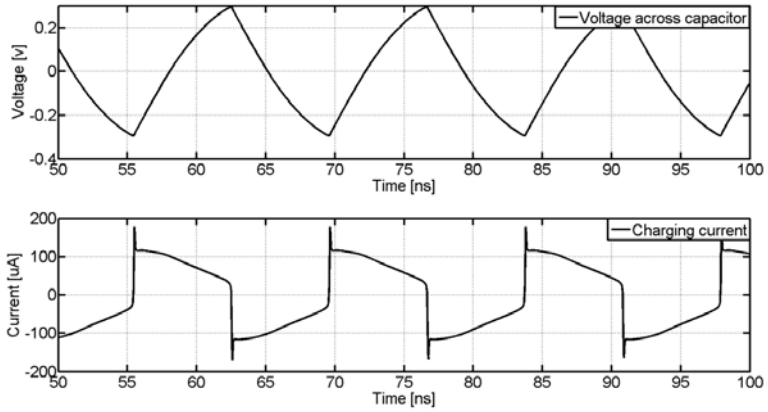


Fig. 2.4(a) Waveform of a source-coupled multivibrator in relaxation mode.

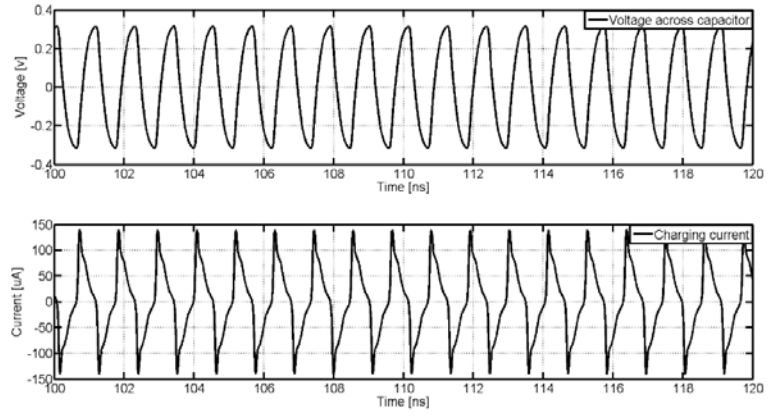


Fig. 2.4(b) Waveform of a source-coupled multivibrator in resonance mode.

Chapter 3: Current-Controlled Oscillator

3.1 INTRODUCTION

The emitter/source-coupled multivibrator discussed in the previous chapter is compact and insensitive to PVT variations. Unfortunately, the oscillating frequency is fixed and defined by the device parameters such as resistance and capacitance. To design a linear current-controlled oscillator, we need the oscillating frequency to vary with the input current.

Let us revisit the operation of multivibrator briefly. Essentially, two current sources charge and discharge an integrating capacitor periodically. If the voltage on the integrating capacitor exceeds the thresholds, the control logic reconfigures the switches and changes the charging direction. The oscillation period/frequency can be derived based on the operation and given by :

$$\int_{t=0}^{t=T/2} I_{in} \cdot dt = C(V_H - V_L) \tag{3.1}$$

Here I_{in} is the input charging current, C is the coupling capacitor connected between the sources, $V_H \; and \; V_L$ are the two reference voltages. To simplify the analysis, we assume that I_{in} is constant during the half period. Therefore, (3.1) reduces to:

$$I_{in} \cdot \frac{T}{2} = C(V_H - V_L) \tag{3.2}$$

$$f = \frac{I_{in}}{2C(V_H - V_L)} = \frac{I_{in}}{2CV_{SW}(I_{in})} \tag{3.3}$$

Where V_{SW} stands for the peak-to-peak voltage swing on C set by the voltage drop across the resistive loads in Fig. 2.2. However, the voltage drop is proportional to the input current for an emitter/source-coupled multivibrator. As a result, the oscillating frequency is not tunable. The basic idea of the proposed current-controlled oscillator is to decouple I_{in} from V_{SW}.

In the following sections, we first go through several existing techniques. Based on the pre-arts, a new current-controlled oscillator replacing the resistive loads with PMOS active loads is presented. Conditions for oscillation and circuit nonlinear behaviors are also analyzed. In last part, we discuss several circuit techniques that can improve the tuning range and/or the linearity.

3.2 PRE-ART OF CURRENT-CONTROLLED OSCILLATOR

In order to obtain current-control of the frequency, the first modification is to keep the load voltage drop constant for different input current. The buffered emitter-coupled multivibrator is proposed. Here a diode is connected in parallel with the load resistor as shown in Fig. 3.1.

The circuit works as follows: we assume that the voltage of the resistive load is large enough to turn on the bypass diode D_1 and D_2. Then the base and emitter of Q_4 are $(V_{DD} - V_{BE})$ and $(V_{DD} - 2V_{BE})$, respectively. Since the base of Q_3 equals to the supply voltage, the base and emitter of Q_2 are $(V_{DD} - V_{BE})$ and $(V_{DD} - 2V_{BE})$, respectively. Since Q_2 is off, one copy of current I_{in} charges the capacitor C and its emitter becomes more negative. Q_1 will eventually turn on when the voltage of emitter becomes smaller than $(V_{DD} - 3V_{BE})$. Q_1 starts to conduct current from the resistor and pulls down

the base and emitter voltage of Q_3. The base voltage of Q_2 moves to more negative value accordingly, causing Q_2 to cut-off. This circuit switches to the other state.

The voltage swing is $2V_{BE}$, therefore, we can calculate the oscillating frequency as follows:

$$\frac{T}{2} = \frac{Q}{I_{in}} = \frac{2CV_{BE}}{I_{in}} \tag{3.4}$$

$$f = \frac{I_{in}}{4CV_{BE}} \tag{3.5}$$

Since the denominator in (3.5) is constant (~0.7v), the oscillating frequency is linearly proportional to the input current. However, this structure shows strong temperature dependence because V_{BE} is complementary-to-absolute-temperature (CTAT). The slope is roughly $-2mV/℃$, therefore, extra temperature compensation circuitry are required for high performance current-controlled oscillator.

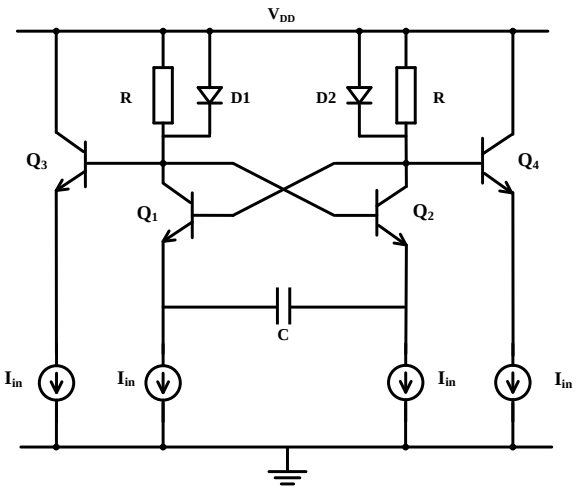


Fig. 3.1 Circuit diagram of a buffered emitter-coupled multivibrator.

Reference [15] solved the temperature dependence problem by using another differential pair to switch a fixed bias current I_B though a resistor R_B. Therefore, the voltage swing V_{SW} becomes $2I_BR_B$, which can be controlled precisely. As a result, the oscillating frequency becomes (3.6). It is proportional to the input current and able to achieve a tuning ratio of 1:1000 with very good linearity.

$$f = \frac{I_{in}}{4CI_BR_B} \tag{3.6}$$

3.3 PROPOSED CURRENT-CONTROLLED OSCILLATOR

The innovation in this thesis is to replace the resistive loads in Fig. 2.3 with PMOS active transistors. Here the channel length modulation provides a conductance proportional to the input current. Thus, the voltage drop across them becomes independent of current. This property translates into linear tuning characteristics.

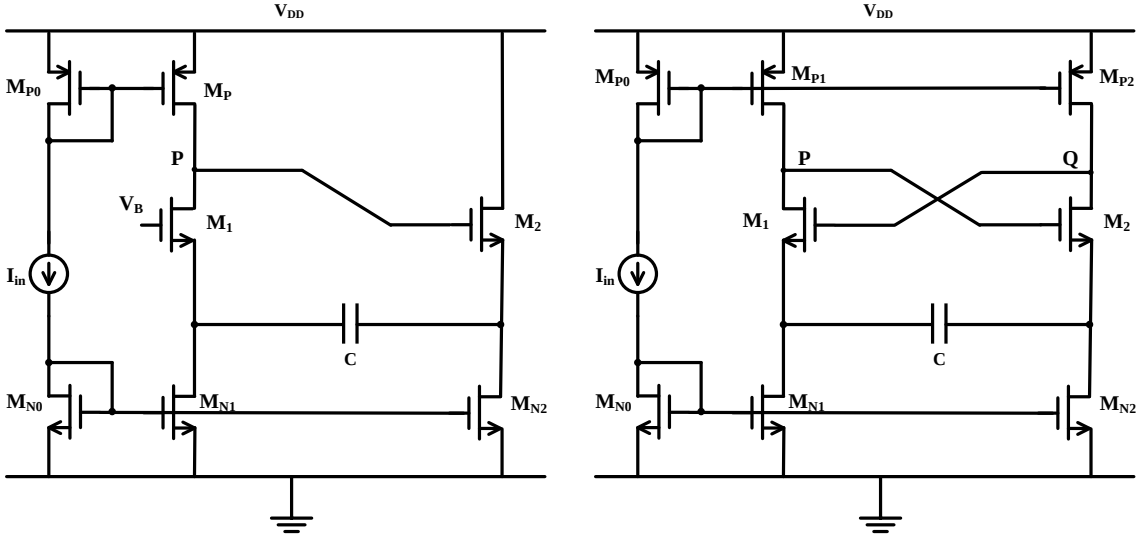
The circuit diagrams of single-ended and fully differential version are depicted in Fig. 3.2, respectively. Let us examine Fig. 3.2(a) for simplicity. We assume that all transistors operate in saturation. The ratio of PMOS and NMOS current mirror is 1:2 and 1:1, respectively.

Initially, M_1 is on and M_2 is off. The gate and drain voltage of M_1 is V_B and $(V_{DD} - V_{DSP})$, respectively. The gate voltage of M_2 is $(V_{DD} - V_{DSP})$. V_{DSP} is the drain-source voltage drop of M_P. The load current from M_P flows through M_1, splitting into two paths. One goes into the NMOS current sink and another copy charges C. The

source of M_2 goes negative as the charging goes on until the gate-source voltage of M_2 exceeds the threshold. As a result, M_2 turns on and the circuit enters into the other state.

The fully differential current-controlled oscillator depicted Fig. 3.2(b) works in a similar fashion. The gate of M_1 is connected to the drain of M_2 to form a cross-coupled pair, producing positive feedback. Another PMOS transistor M_{P2} is loaded between M_2 and the voltage supply to make it fully symmetrical.

The fully differential current-controlled oscillator doubles the effective voltage swing and improves the noise immunity and common-mode rejection. However, the oscillating frequency halves because of the wider voltage swing. Therefore, the singled-ended structure in Fig. 3.2(a) is better for high-speed application that requires wider oscillating range, while the fully differential structure is more suitable for high-resolution application.



(a) (b)

Fig. 3.2 Proposed single-ended (a) and fully differential (b) CCO.

Fig. 3.3 shows the I-V characteristic curves with the resistive loads and active loads. In the resistive loads case, the intersect points (square) are pushed towards zero as the current increases. On the other hand, the intersect points with PMOS active loads (circle) are restricted in certain range with proper sizing. This modification greatly reduces the load variation and preserves the constant V_{SW}. Fig. 3.4 plots the peak load voltage drop on M_1 (V_{DSP1}) and V_{SW}. We sweep the input current from $100\,uA$ to $700\,uA$, the corresponding variations of V_{DSP1} and V_{SW} are $54\,mV$ and $23\,mV$, respectively. The residual fluctuation is smaller than 5% of the nominal value, which is caused by other circuit non-idealities discussed in next section. In summary, by replacing the resistive loads with PMOS active transistors, we are able to control the oscillating frequency in a much more linear way.

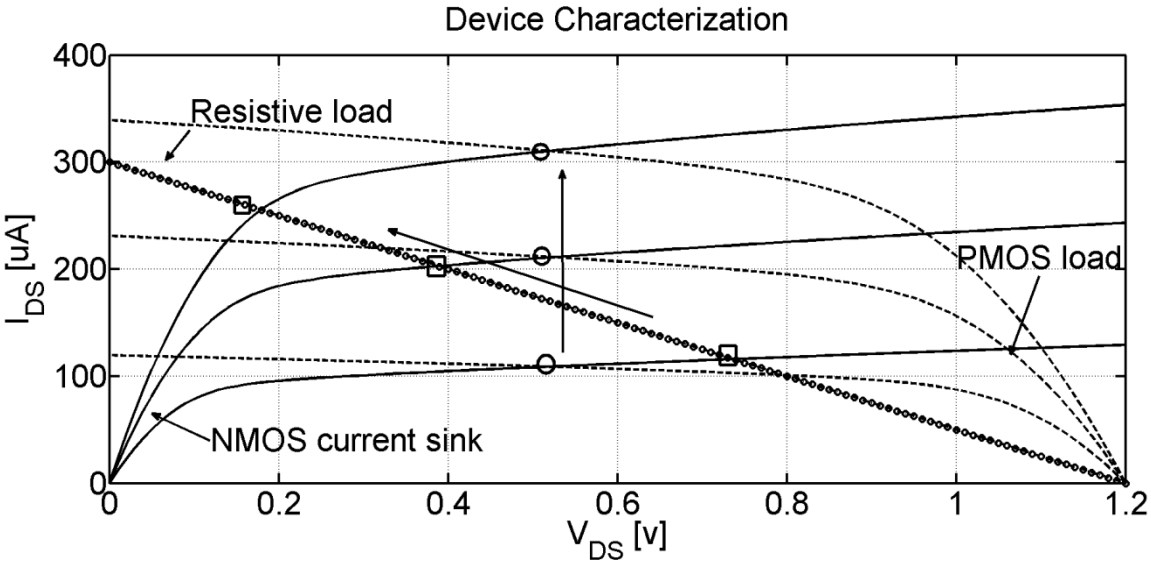


Fig. 3.3 Device characteristic curve with resistive and active load.

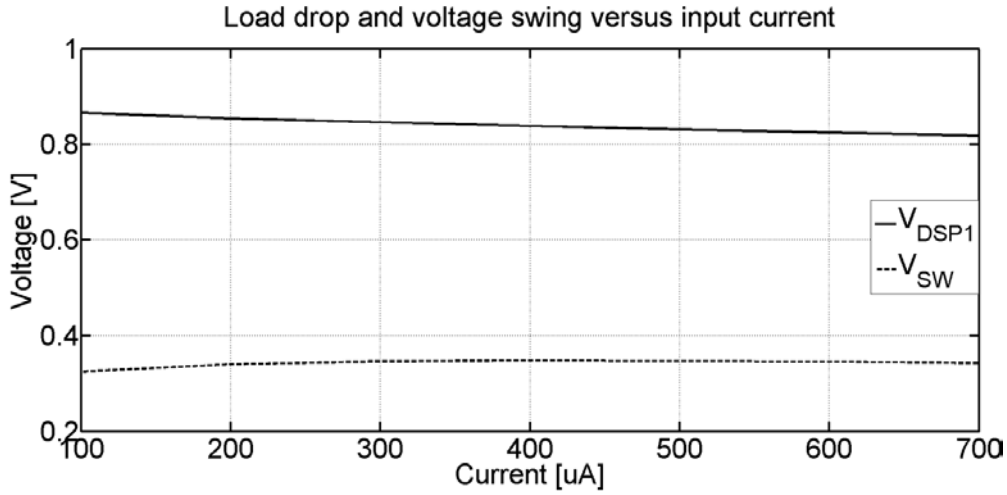


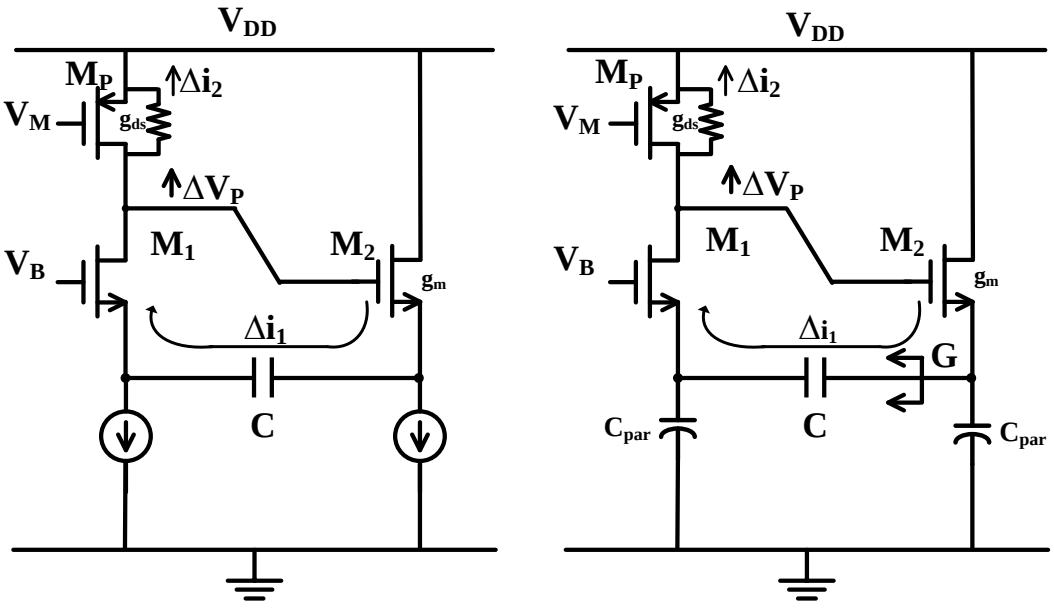
Fig. 3.4 Load voltage drop and peak voltage swing on C against input current.

3.4 CONDITIONS FOR OSCILLATION

In this session, the conditions for oscillation of the proposed current-controlled oscillator are derived. At low frequency, we use the very basic small-signal model with the assumption that all transistors are in saturation. Even though it is not valid for large signal transient operation, it still offers a good starting point for circuit design. As the input current and oscillating frequency increase, parasitic capacitances compromise the loop gain of the positive feedback. As a result, at some point, the oscillator does not operate properly.

3.4.1 Low Frequency

To obtain the analytical expression, we start from the small-signal single-ended model in Fig. 3.5(a) for simplicity. Assuming that all transistors are in saturation and the NMOS current sinks behave like ideal current sources.



(a) (b)

Fig. 3.5 Small-signal model at low frequency (a) and high frequency (b).

Let us assume that there is a small incremental voltage change (ΔV_P) at the gate of M_2. It generates a small current i_1 through M_2. At low frequency, the small current goes through the source-coupled capacitor and flows back in to the source of M_1. Meanwhile, a small current i_2 is generated by the V_{DS} change of M_P. If $i_1 > i_2$, then ΔV_P is magnified. Therefore, the positive feedback provides enough loop gain, making the circuit oscillate. The condition for oscillation at low frequency is given by:

$$g_m \cdot \Delta V_P > g_{ds} \cdot \Delta V_P \tag{3.8}$$

$$\frac{g_m}{g_{ds}} > 1 \tag{3.9}$$

Where g_m is the transconductance of M_2 and g_{ds} is the output conductance of M_P. Assuming that the oscillator is in equilibrium, which means the DC current I_{in} of M_2 and M_P are the same, we can express g_m and g_{ds} as follows:

$$g_m = \frac{I_{in}}{V_{ov}} \tag{3.10}$$

$$g_{ds} = \lambda_P I_{in} \tag{3.11}$$

Here $\lambda_P$is the channel length modulation factor of M_P and V_{ov} is the overdrive voltage of M_2. Combing (3.9)-(3.11), we obtain:

$$\frac{1}{\lambda_P V_{ov}} > 1 \tag{3.12}$$

To make the oscillator regenerate, we need to keep the denominator far below two for enough design margins. Therefore, long-channel PMOS devices are preferred since λ_P is inverse proportional to the channel length. For M_2, it is desirable to bias the transistor with low overdrive voltage. However, small overdrive voltage means large device size and parasitic capacitance. These undesired parasitic capacitances limit the highest oscillating frequency and the linearity of CCO.

3.4.2 High Frequency

However, equation (3.12) ignores other high frequency effects. As the oscillating frequency increases, the parasitic capacitances steal the charging current and reduce the loop gain. Moreover, the overdrive voltage of cross-couple devices increases with the

input current. As a result, the loop gain falls below one. Fig. 3.5(b) represents the simplified model at high frequency, which includes the parasitic signal paths. The effective current flowing through the loop is given by:

$$I_{eff} = \frac{g_m}{g_m + j\omega C_{par}} \cdot \frac{G}{G + j\omega C_{par}} \cdot (g_m \cdot \Delta V_P) \tag{3.13}$$

$$G = \left(\frac{1}{j\omega C} + \frac{1}{g_m + j\omega C_{par}} \right)^{-1} \tag{3.14}$$

$$I_{eff} > g_{ds} \cdot \Delta V_P \tag{3.15}$$

Where C_{par} is the parasitic capacitance at the source of the cross-coupled pair. By substituting (3.13) and (3.14) into (3.15), we got the condition for oscillation as follows:

$$\left\| \frac{1}{\left(1 + \frac{j\omega}{\omega_C}\right)(1+\alpha) + \frac{j\omega}{\omega_C}} \cdot \frac{g_m}{g_{ds}} \right\| > 1 \tag{3.16}$$

Where $\omega_C = \frac{g_m}{C_{par}}$ and $\alpha = \frac{C_{par}}{C}$. With proper design and layout, parameter α should be smaller than 0.05 so that the overall performance is not limited by the parasitic capacitance. Therefore, we can further reduce (3.16) and obtain:

$$\left\| \frac{1}{1 + \frac{2j\omega}{\omega_C}} \cdot \frac{g_m}{g_{ds}} \right\| > 1 \tag{3.17}$$

$$\left\| \frac{1}{1+\frac{2j\omega}{\omega_c}} \cdot \frac{1}{\lambda_P V_{ov}} \right\| > 1 \tag{3.18}$$

The magnitude of left term in (3.18) rolls off 20dB/dec after it hits the first pole at $\frac{g_m}{2C_{par}}$. It is reasonable to conclude that the pole is 10~15 times smaller than the ω_T of M_2.

$$\omega_p = \frac{1}{2}\omega_c = \frac{g_m}{2C_{par}} \cong 0.1\omega_T \tag{3.19}$$

$$\omega_T = \frac{\mu C_{ox}(\frac{W}{L})V_{ov}}{\frac{2}{3}C_{ox}WL} = 3\mu V_{ov}/2L^2 \tag{3.20}$$

Here μ is the carrier-mobility of M_1 and M_2. Therefore, for oscillation, long-channel PMOS load and short-channel NMOS cross-coupled devices are desirable. The overdrive voltage of cross-coupled pair becomes a design nob for optimization. It should be small to ensure oscillation, meanwhile, ω_T should be large enough to extend the oscillating range.

3.5 NONLINEARITIES

Several nonlinear sources make the proposed CCO behave differently from what we modeled in (3.3). In this session, we discuss the fundamental mechanisms behind and the effects on the transfer characteristics.

3.5.1 Gate-Source Voltage of Cross-Coupled Pair

Let us examine the circuit shown in Fig. 3.6. At the moment that M_1 turns off and M_2 is about to turn on, the source voltage of M_1 and M_2 are at their peak and valley, V_H and V_L, respectively. We can derive the value of V_H and V_L and get the analytical expression of V_{SW}:

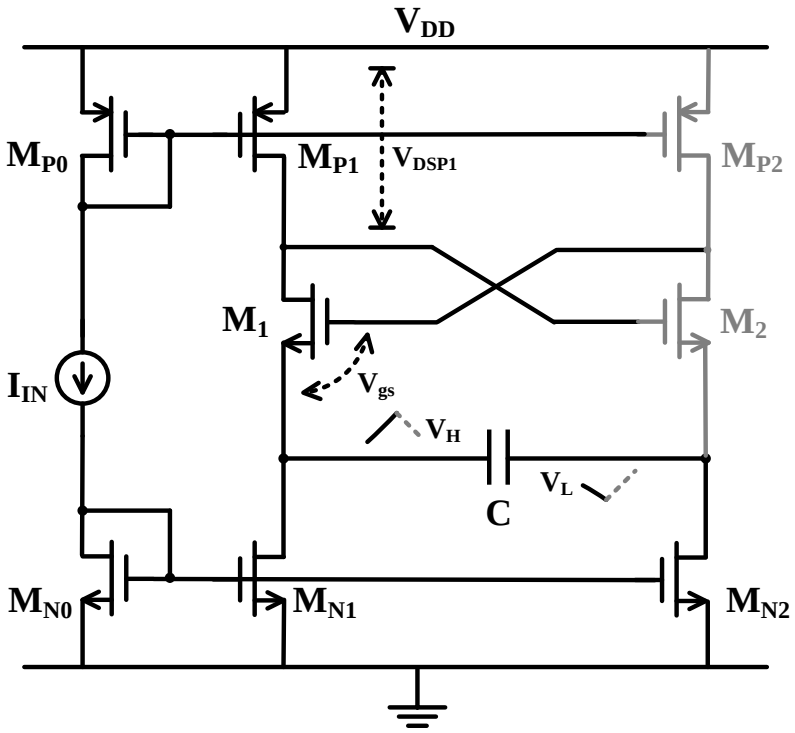


Fig. 3.6 Circuit operation in state transition.

$$V_H = V_{DD} - V_{gs} \tag{3.21}$$

$$V_L = V_{DD} - V_{DSP1} - V_{th} \tag{3.22}$$

$$V_{SW} = V_H - V_L = V_{DSP1} - V_{ov} \tag{3.23}$$

V_{DSP1} is the load voltage drop of the PMOS active device (M_{P1}) and V_{ov} is the overdrive voltage of cross-coupled pair ($M_1\ and\ M_2$). Assuming that $M_1\ and\ M_2$ operate in saturation region in oscillation, we can simplify (3.23) with the square law model and obtain:

$$V_{SW} = V_{DSP} - \sqrt{\frac{4I_{in}}{\mu C_{ox}\frac{W}{L}}} \tag{3.24}$$

The second term in (3.24) is proportional to the square root of input current causing nonlinear conversion gain. As the input current increases, the cross-coupled pair behaves as switches steering the current. As a result, $M_1\ and\ M_2$ operate in linear region rather than saturation region. The corresponding voltage swing expression becomes:

$$V_{SW} = V_{DSP} - \frac{2I_{in}}{uC_{ox}\frac{W}{L}V_{DSN}} \tag{3.25}$$

As show in (3.25), the second term is proportional to the input current. Therefore, the nonlinear effect is stronger compared to (3.24). V_{DSN} is the drain-source voltage drop of $M_1\ and\ M_2$. With large input current, we assume that V_{DSN} is small and constant.

To reduce the nonlinear effects, we need to maximize the denominator of the nonlinear terms in (3.24) and (3.25). Therefore, we choose NMOS cross-coupled pair with large geometric ratio. However, large devices contribute huge parasitic capacitance compromising high frequency performance and oscillating range.

3.5.2 Charging Current

Fig. 3.2 depicts a conceptual current source for simplicity. In actual design, a current mirror circuitry shown in Fig. 3.7(a) is required. It matches the current between the active loads and the current sinks to 2:1. However, the finite output impedance of the current mirrors causes mismatch errors on the net charging current. The errors are dependent on the input current and generate harmonic distortions.

Fig. 3.7(a) is a static replica of the oscillator emulating the charging/discharging processing when M_{P1} is conducting $2I_{in}$ and the gate of M_1 is connected to supply voltage. We sweep the input current from $5uA$ to $400uA$. The actual current of M_{P1} and its ideal value are compared in Fig. 3.7(b)

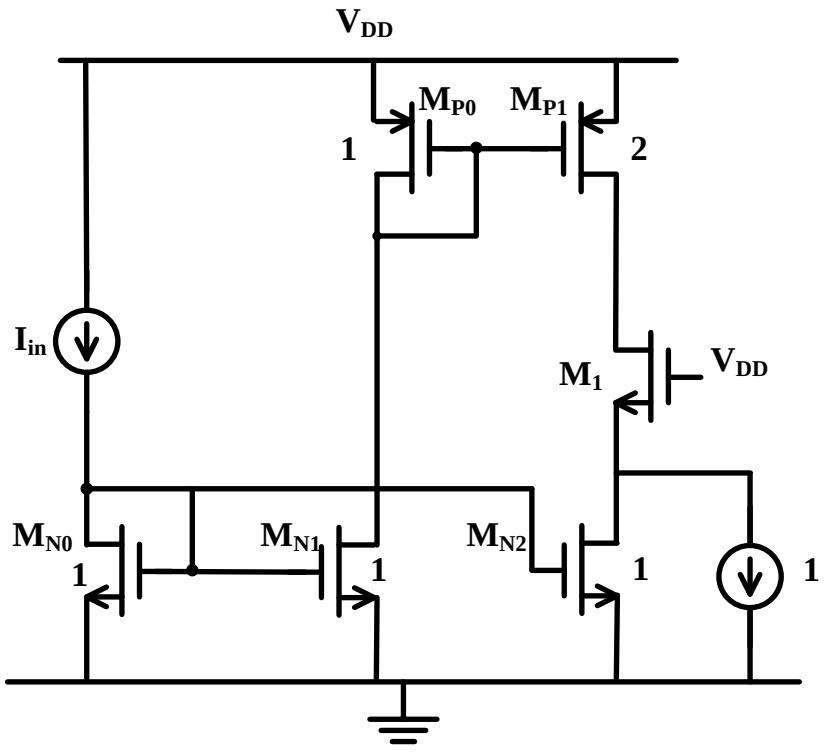


Fig. 3.7(a) Input current mirror circuitry

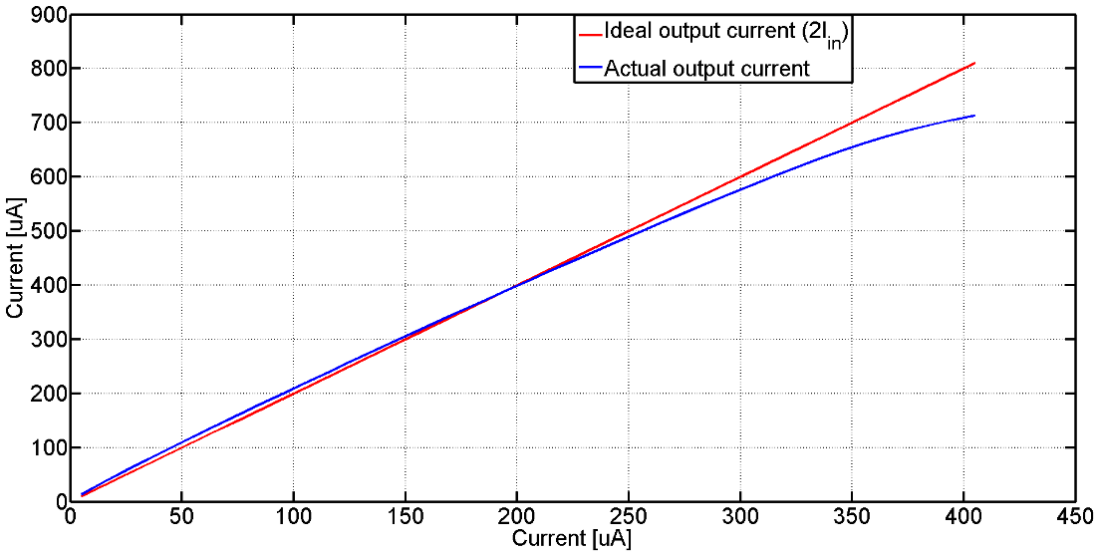


Fig. 3.7(b) Ideal charging current versus actual current

It is clear that the actual charging current is slightly larger than the ideal value when the input is small. However, as increasing current, the PMOS loads and the NMOS current sinks are fighting with each other because of their finite output impedance. As a result, the actual current falls below the ideal one at some point ($I_{in} \cong 200uA$). The discrepancy becomes larger as the input current increases. The error is about 12% of the ideal value when $I_{in} = 400uA$.

The bending shape of the transfer curve mainly contributes 2nd order harmonic distortion. Pseudo-differential structure using two CCOs cancels the even-order harmonics with 2x power and area penalty. Another effective way to resolve the current mismatch problem is to use cascode. It improves the output impedance of the current sources by sacrificing the output swing. Nevertheless, extra parasitic nodes slow down

the oscillator. Therefore, to design a CCO oscillating above $1GHz$, we avoid using the cascode technique.

In summary, the current mismatch is a big error source for the wide tuning range CCO. For high-speed design whose resolution or linearity is of less concern, we use long channel devices to make good current sources. For low-speed high-resolution design, cascode is preferred to improve the quality of current sources.

3.5.3 Finite Switching Speed

In the previous discussion, we assume that the switching speed is infinite and the transition time between two states is zero. However, it takes time and its value is relative constant in actual design. As the input current and oscillating frequency increase, the transition time becomes a larger portion of the overall period. As a result, at high frequency, the oscillating frequency is smaller than the value we predicted and its transfer curve becomes saturated. This bending shape of the current-to-frequency transfer curve also contributes 2^{nd} order harmonic distortion.

It is effective to improve the switching speed by increasing the bandwidth of the cross-coupled pair. As we move into advanced technology nodes, device scaling will help and mitigate this problem.

3.6 PERFORMANCE IMPROVING TECHNIQUES

According to the analysis in previous sessions, there are four major error sources contributing to the CCO nonlinearity:

1) Voltage variations of the active loads.

2) Gate-source/overdrive voltage variations of the cross-coupled pair.

3) Matching error of the current sources.

4) Finite switching speed of the cross-coupled pair.

3.6.1 Nonlinear Cancellation

For high frequency application, it is desirable to use simple structure. Therefore, it would be instructive to design and bias the oscillator in a certain way so that the nonlinearities cancel with each other.

Fig. 3.8 shows three transfer curves dominated by different nonlinear sources. Curve 1 indicates that the decreasing voltage swing on the source-coupled capacitor leads to up-tilt. Curve 2 shows that the input current matching error and the finite switching speed causes bend-down at high frequency. Therefore, we can linearize the transfer characteristics by cancelling the two nonlinear effects properly as curve 3.

Unfortunately, the cancellation relies on different physical mechanisms that are uncorrelated. Therefore, the cancellation effect is sensitive to the process and temperature variations. We implemented a CCO based on this technique. Details of the chip design and simulation results are explained in Chapter 4 and Chapter 5, respectively.

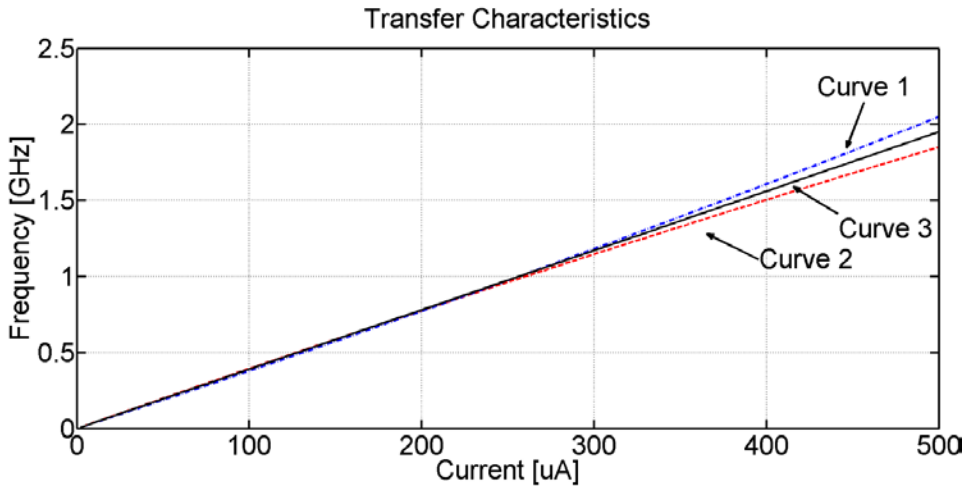


Fig. 3.8 Nonlinear cancellation.

3.6.2 Replica Biasing

The load voltage variation depends on the strength of PMOS loads and NMOS current sinks. It is sensitive to the process and temperature variations. Even with optimal design, it is very hard to keep the variation below 2% in all corners. To obtain high accuracy, we need extra circuit techniques to improve the quality of the load voltage.

Here the replica biasing technique is used. In addition to the core circuit for oscillation, another slave copy is added to provide information correlated with the master/core oscillator. By sensing the circuit parameters of the slave part, we can compare them with voltage/current references and tune the master/core part adaptively.

The circuit diagram is shown in Fig. 3.9. We degenerate the PMOS loads with tunable MOS resistors operating in linear region. It provides a nob to adjust the current density so that the load voltage drop remains constant over the full input range. The strength of the degenerated MOS resistor should be designed properly to cover a wide dynamic range.

The load voltage drop increases due to the degeneration. As a result, the current-to-frequency conversion gain decreases. Essentially, it trades speed for accuracy. In summary, it is a powerful technique to improve the linearity of the transfer characteristics with small hardware overhead.

3.6.3 Gate-Source Voltage Control

As discussed in Section 3.5, the gate-source voltage variation of the cross-coupled pair is a major nonlinear source. When we sweep the input current from $2uA$ to $512uA$, the equivalent overdrive voltage is nearly doubled, causing big nonlinearity on the transfer characteristics.

In Fig. 3.10, the gray dashed boxes with NMOS device in feedback replace the purely NMOS cross-coupled pair. The inputs of the amplifier become the new gate and source terminals. Therefore, the gate-source voltage variation is suppressed by the amplifier's gain. As a result, we can restrict it to a small value. Here an amplifier with gain of 20-30 dB is good enough. Therefore, we can apply this technique even in 20nm technology. Similar to all feedback systems, at high frequency, the loop gain drops. Therefore, it is only useful for low frequency application such as biomedical and audio system.

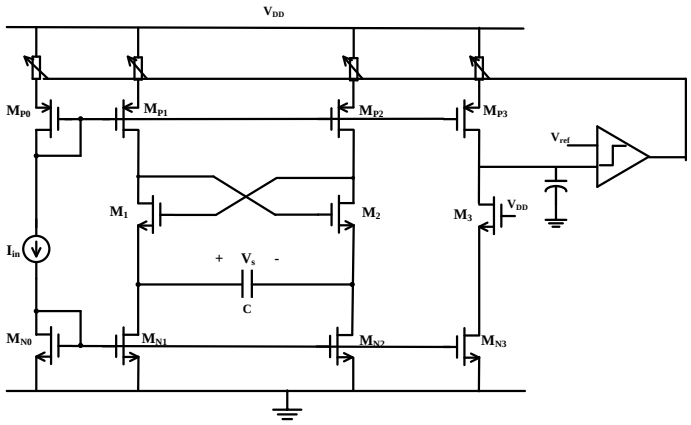


Fig. 3.9 Replica biasing circuitry

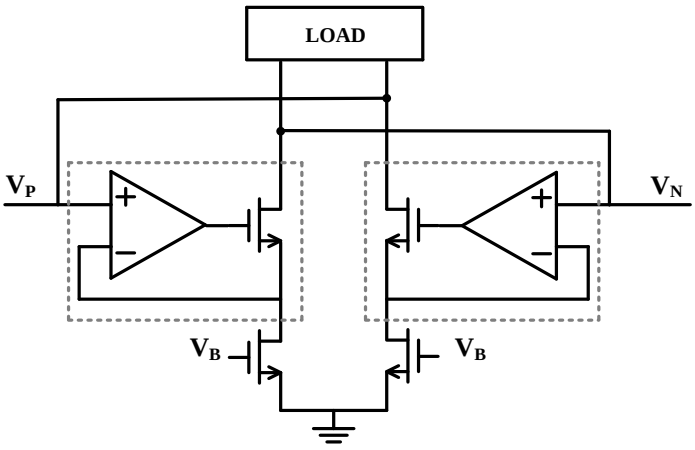


Fig. 3.10 Cross-coupled pair in feedback.

Chapter 4: Circuit Implementation

4.1 CIRCUIT DESIGN

In this chapter, the circuit design and optimization of the CCO are presented. Fig. 4.1 shows the top-level diagram. The input current is injected into the core oscillator through current mirror as shown in Fig. 3.7(a). The oscillator generates differential output. A buffer is inserted to convert the differential signal into full-swing single-ended output. It follows by a frequency divider to count down the high frequency output.

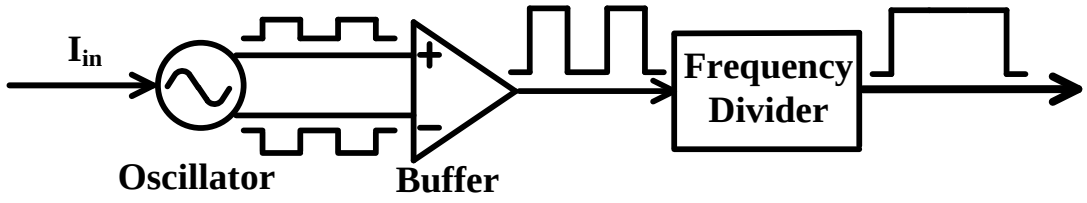


Fig. 4.1 Block diagram of the current-controlled oscillator prototype.

4.1.1 Core Oscillator

The full schematic of the core oscillator is shown in Fig. 4.2. The device sizing is provided in Table-1. In this prototype, we use low V_T devices since they provide low threshold voltage and high transconductance. To improve the output impedance, we choose long channel devices for the current sources. On the load side, the channel length is set to $150nm$ to reduce input dependent load voltage variation.

For the cross-coupled pair, we prefer to use minimal channel length because it delivers the high speed and wide bandwidth. According to (3.3), small source-coupled capacitance produces high oscillating frequency; however, the nonlinear junction capacitances (C_{SB1}, C_{DB2}) will degrade the linearity of the transfer characteristics at high

frequency. We choose a $50fF$ Metal-Oxide-Metal (MoM) capacitor and make sure that the lumped parasitic capacitance on each terminal is less than $10fF$.

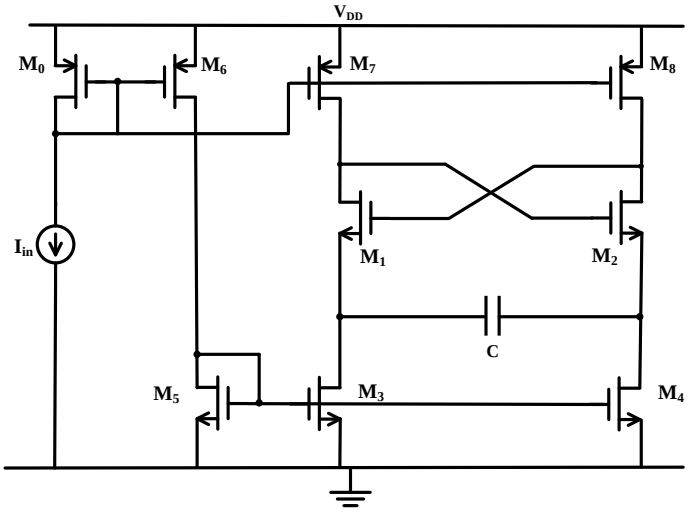


Fig. 4.2 Full schematic of the CCO.

	Device type	$W/L\ (um)$
M_1/M_2	NMOS lvt	12/0.12
M_3/M_4	NMOS lvt	12/0.24
M_5	NMOS lvt	12/0.24
M_0	PMOS lvt	12/0.15
M_6	PMOS lvt	9/0.15
M_7/M_8	PMOS lvt	12/0.15
C	MoM Cap	12.28/11.9 (x4)

Table 1. Device sizing of the core oscillator.

4.1.2 Differential to Single-Ended Buffer

The oscillator output is differential with limited swing ($\sim 400mV$). Therefore, a buffer is required to convert it into full-swing single-ended signal. Moreover, the buffer provides gain to block the kick-back switching noise from the digital side. The schematic and device sizing of the buffer are shown in Fig. 4.3 and Table-2, respectively.

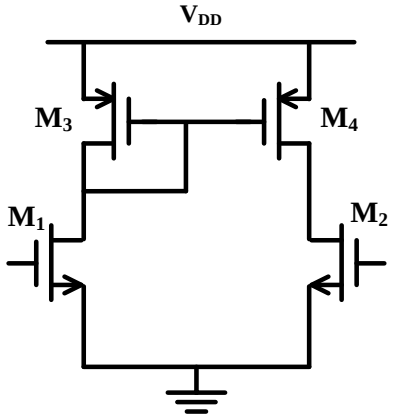


Fig. 4.3 Schematic of the differential to single-ended buffer.

	Device type	$W/L\ (um)$
M_1/M_2	NMOS lvt	4/0.12
M_3/M_4	PMOS lvt	16/0.12

Table 2. Device sizing of differential to single-ended buffer.

4.1.3 Frequency Divider

The frequency divider is implemented on-chip to facilitate the measurement. It is composed of seven divide-by-2 D-flip-flops (DFFs) in cascade as depicted in Fig. 4.4(a).

The maximal division ratio is 128 in our design. We adopt the true single-phase-clock (TSPC) structure in Fig. 4.4(b) to implement the DFFs.

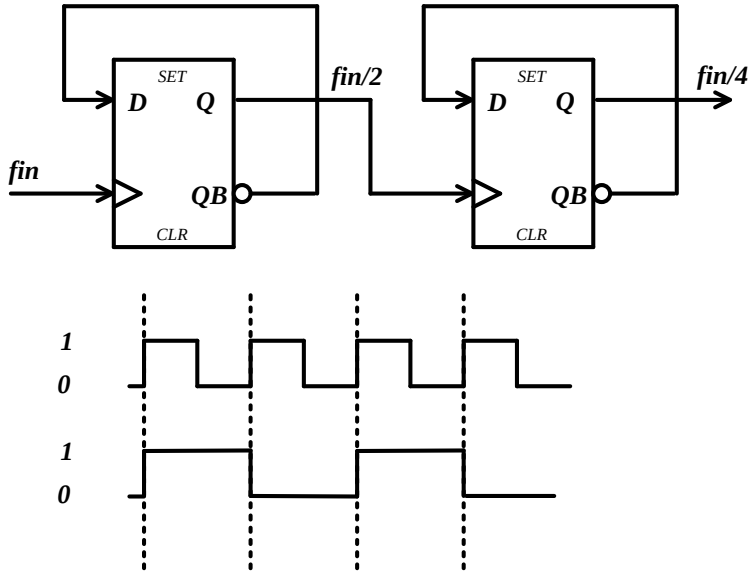


Fig. 4.4(a) Asynchronous frequency divider.

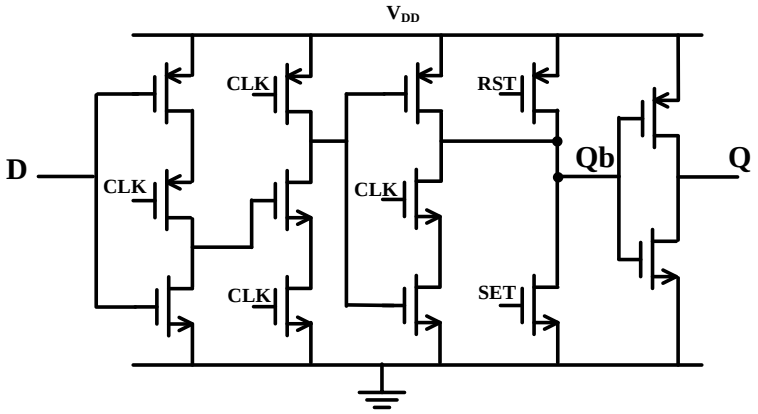


Fig. 4.4(b) Schematic of the TSPC DFFs.

4.2 LAYOUT IMPLEMENTATION

4.2.1 Core Oscillator

Essentially, the core oscillator is the most critical part in our design. The layout of this block was done with great care to reduce the parasitic capacitance. Symmetrical layout also improves the common-mode rejection and noise immunity.

Fig. 4.5 shows the layout of the core circuits (source-coupled capacitor is not shown). We use multi-finger structure extensively to reduce the gate resistance. In addition, the active regions of cross-coupled pair are shared with the NMOS current source. It reduces the parasitic capacitances at the source terminals by a factor of two. This arrangement improves the linearity performance at high frequency.

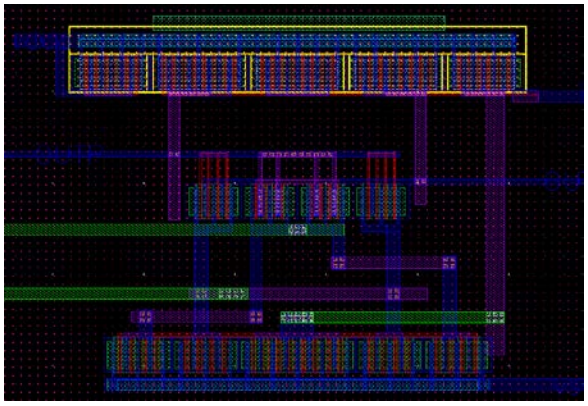


Fig. 4.5 Layout of the core oscillator

4.2.2 Buffers and Frequency Divider

Fig. 4.6 shows the digital circuits including the differential to single-ended buffer and the frequency divider. These building blocks were implemented manually and optimized for low power.

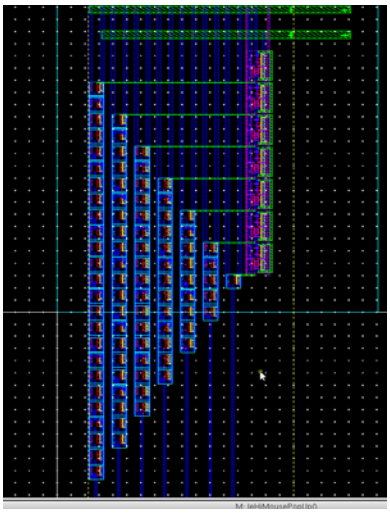


Fig. 4.6 Layout of the digital parts

4.2.3 Floorplan

The overall layout is shown in Fig. 4.7. The most critical analog blocks are placed at the top-right corner so that the input analog signals are well protected. The digital building blocks are arranged at the right side of the chip. All the gigantic output buffers are located at the bottom-left corner far away from the analog part.

The chip includes 20 pads dividing into three different domains: analog, digital and I/O. The analog pads are located in top-right corners as well. The digital pads are placed close to the digital building blocks. The I/O pads contain all the supply and ground, driving $2\,pF$ capacitive loading. We separate them intentionally from the top-right corner so that the large switching currents do not affect the analog performance.

Large de-coupling capacitors are also added all around the chip (red parts) to attenuate the high frequency noise. The core area including the core oscillator and digital

circuits is about $150\ um \times 100um$. The total chip area is about $700um \times 700um$.The compact layout is attractive for the modern system-on-chip (SoC) design.

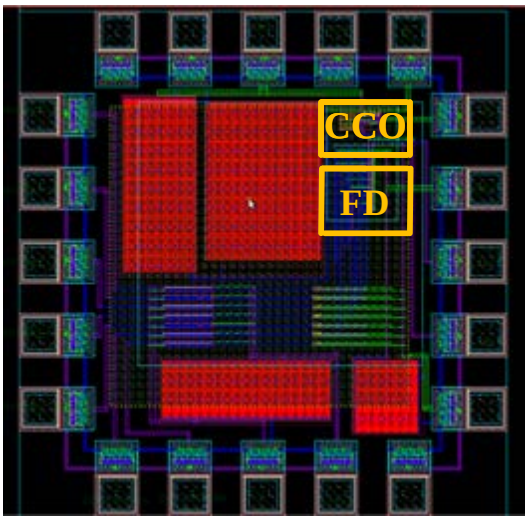


Fig. 4.7 Chip layout

Chapter 5: Simulation and Measurement Results

A current-controlled oscillator prototype is implemented in $130nm$ CMOS technology as a proof of concept. Careful layout and extraction reduce the impact from parasitic to minimum. The performance across different process and temperature corners are evaluated. The simulation and measurement results prove the effectiveness of our proposed CCO.

For linearity analysis, we measure the current-to-frequency transfer curve statically by sweeping the input current from $2uA$ to $512uA$ for 8-bit dynamic range. Matlab provides a polynomial curve fitting function, converting the transfer curve into the following polynomial equation:

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \cdots \quad (5.1)$$

By analyzing the nonlinear terms (a_2, a_3 ...), we obtain the harmonic distortion power of the CCO. We also calculate the differential nonlinearity (DNL) and integral nonlinearity (INL) of the CCO based on the simulation and measured data.

5.1 Simulation Results

5.1.1 Current-to-Frequency Transfer Curve

Fig. 5.1 exhibits the block diagram of simulation setup. DC current is fed into the CCO. It charges/discharges the source-coupled capacitor and generates differential output. The differential output is converted to single-ended signal and processed in Matlab.

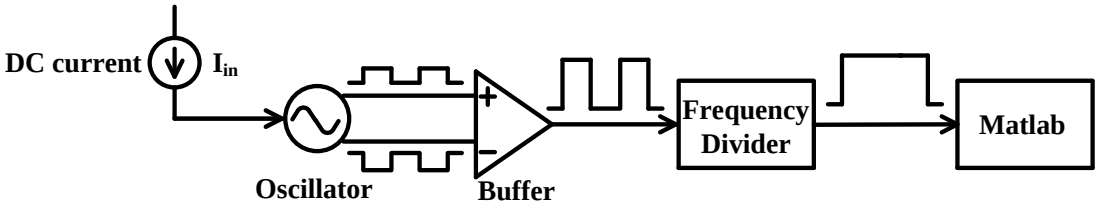


Fig. 5.1 Simulation setup of current-to-frequency transfer curve

Fig. 5.2(a) plots the current-to-frequency transfer curves in different temperatures. The slope (conversion gain) of the transfer curve increases slightly with temperature. The peak oscillating frequency is about $2GHz$. In Fig. 5.2(b), we simulate the CCO in different process corners at room temperature. As expected, the oscillating frequency is insensitive to the process variations since it relies more on passive devices. The variation of the conversion gain is less than 3% of the nominal value, which is much smaller than the ring-oscillator.

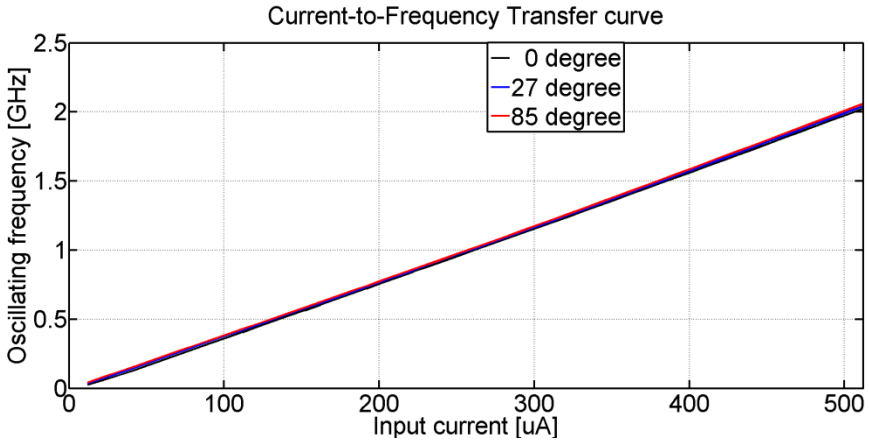


Fig. 5.2(a) Current-to-frequency transfer curve with different temperature.

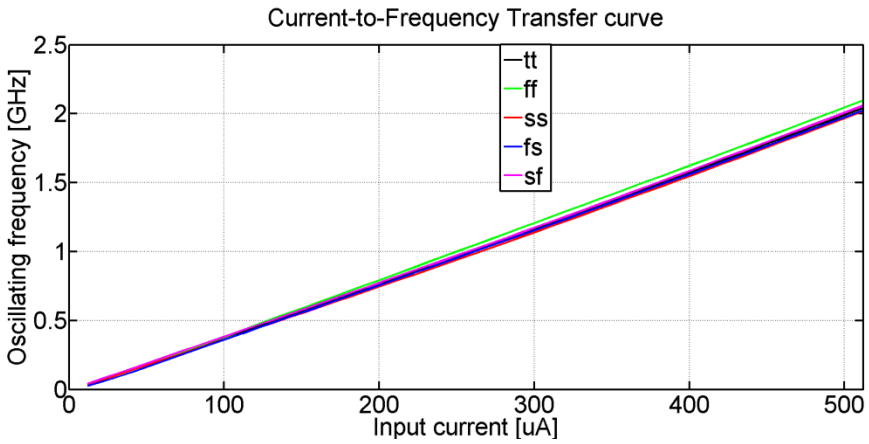


Fig. 5.2(b) Current-to-frequency transfer curve with different process corners.

5.1.2 DNL and INL

DNL and INL are the most cited specifications describing the performance of a data conversion system. Fig. 5.3 shows the DNL and INL with full scale input current of $512uA$. The DNL is +0.31/-0.32 LSB and INL is +2.0/-2.2 LSB, respectively. The discontinuous jump points on the DNL plot are caused by the segmentation we use to speed up the simulation. The shape of the INL curve proves again that even order (2^{nd}) harmonic distortions are the main nonlinear sources. Therefore, we can improve the CCO linearity by using pseudo-differential structure. Fig. 5.4 shows the DNL and INL curve of a pseudo-differential CCO. The DNL is improved to +0.17/-0.17 LSB and INL is improved to +0.75/-0.75 LSB. In summary, the proposed CCO exhibits excellent linearity up to $2GHz$. Much higher frequencies should be possible as we migrate to more advanced process node.

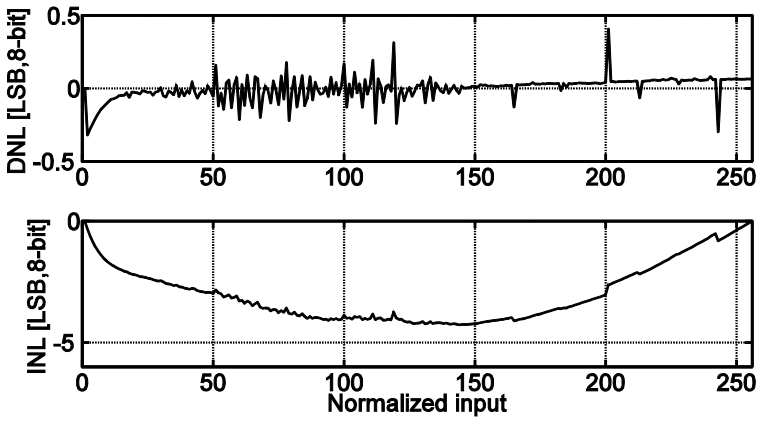


Fig. 5.3 Simulated DNL and INL of the CCO.

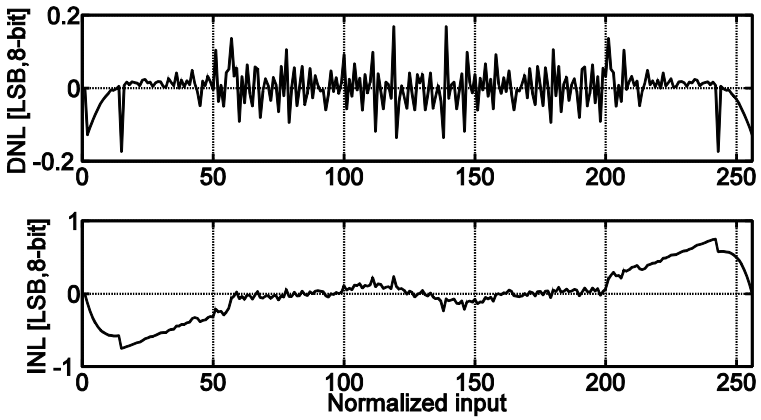


Fig. 5.4 Simulated DNL and INL of the pseudo-differential CCO.

5.1.3 Phase Noise

For conventional oscillator design, noise performance, especially phase noise, is the most important specification. Local oscillator (LO) with poor phase noise degrades the SNR of a receiver system. Fortunately, for application like data conversion, the effect of the phase noise is minor compared to the nonlinearity. In high-speed low-resolution system, quantization noise is the dominant noise source. For high-resolution data

conversion system, the oscillator is placed inside a loop. Therefore, the phase noise is suppressed.

Fig. 5.5 shows the phase noise result in “pnoise” analysis when the CCO runs at 1 GHz. At $1MHz$ offset frequency, the phase noise is about -75 dBc/Hz. The flicker noise from the cross-coupled pair contributes to the -30 dB/dec slope. The noise performance is inferior to the LC-tank oscillator, but it is good enough for data conversion with medium resolution.

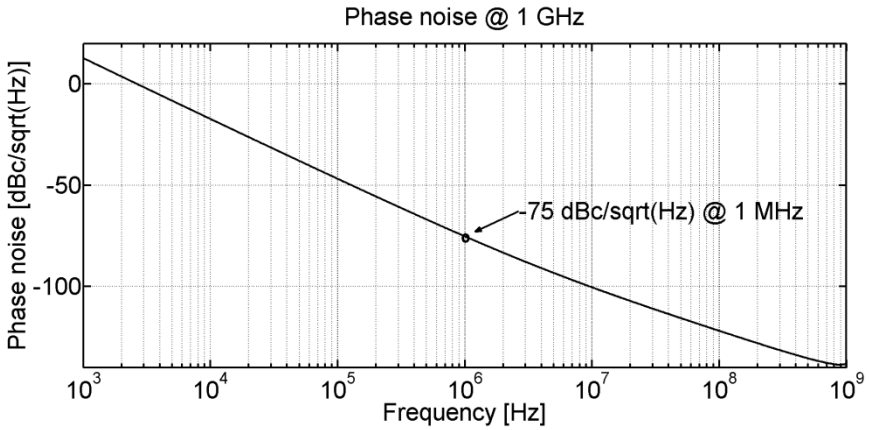


Fig. 5.5 Phase noise of the CCO at 1GHz.

5.2 MEASUREMENT RESULTS

The CCO was fabricated in standard CMOS 130nm technology. Fig. 5.6 shows the chip photograph. The core area is $150um \times 100\ um$. The measurement setup is shown in Fig. 5.7. A 12-bit DAC feeds the input current into the CCO. The output frequency is divided by 128 times. A digital frequency counter counts the divided frequency output.

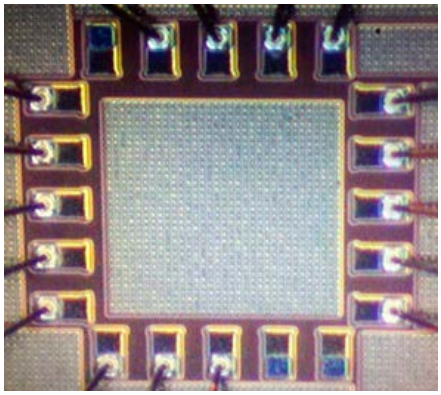


Fig. 5.6 Die photo.

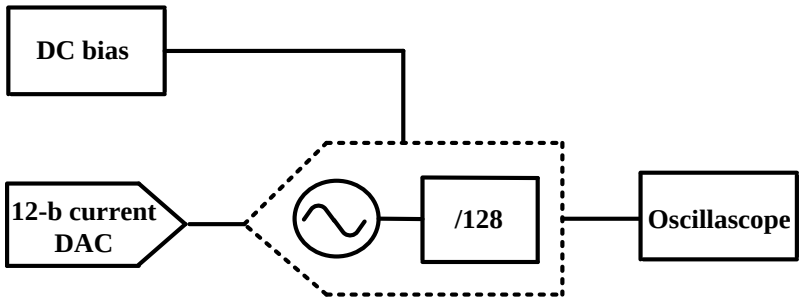


Fig. 5.7 Measurement setup.

Fig. 5.8 shows the measured transfer characteristics with 1v supply. The CCO operates properly when the input current varies from $20uA$ to $420uA$. The peak measured oscillating frequency is $550MHz$. The operation at low current/frequency range matches the simulation results. Extra higher-than-expected parasitic capacitance slows down the oscillation and stops the circuit from regenerating at high frequency.

In summary, the measured data exhibits smaller dynamic range due to implementation imperfections. Nevertheless, in the frequency range up to $550MHz$, it still shows very linear transfer characteristics.

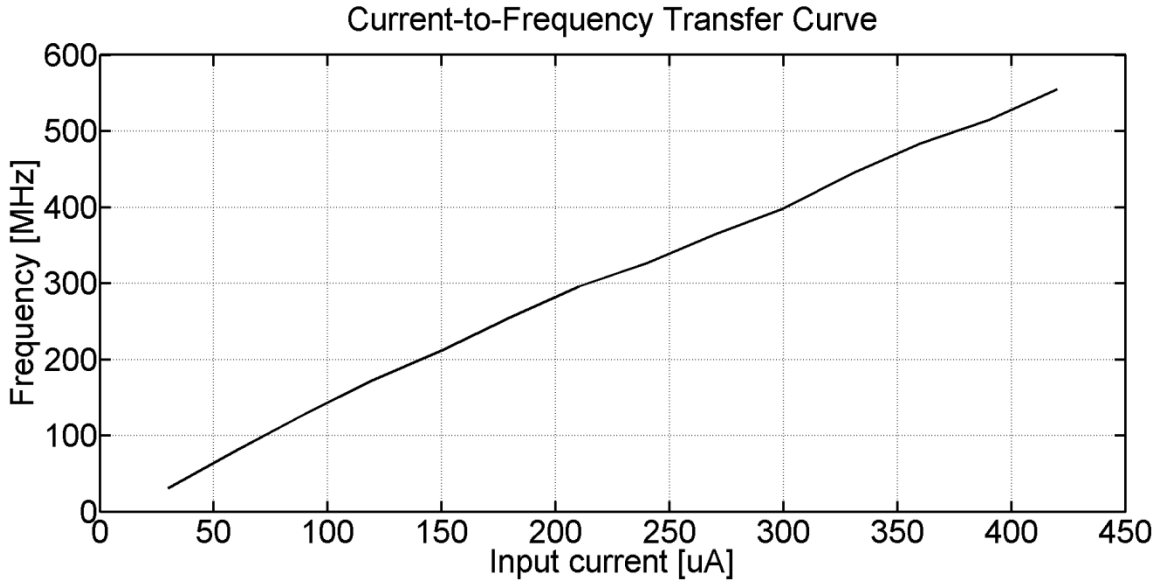


Fig. 5.8 Measured transfer characteristics.

Chapter 6: Conclusion and Future Work

6.1 Conclusion

In this thesis, a novel current-controlled oscillator based on the source-coupled multivibrator is presented. By replacing the resistive loads with active loads, the voltage swing on the source-coupled capacitor becomes independent of the input current. As a result, the oscillating frequency varies linearly with the input current. Mathematical equations describing the conversion gain and the conditions for oscillation are derived.

However, the tuning range and linearity of the CCO are limited by the circuit non-idealities such as residual load voltage variation, gate-source voltage change of the cross-coupled pair and the input current mismatch. At high frequency, the operation of the CCO deviates from our model. As explained, the net charging current and the voltage swing reduce as the input current increases. These input-dependent errors lead to the nonlinear behavior of the CCO.

To address these problems, several circuit techniques are proposed. By cancelling the nonlinear effects from different sources, we obtain good linearity across wide tuning range. The implemented prototype incorporates this idea and shows good static performance. Other circuit techniques such as the replica biasing and feedback are also effective to mitigate the nonlinearities at low speed.

A CCO prototype with nonlinear cancellation is implemented in CMOS $130nm$ technology. The simulation results indicate that this CCO is able to oscillate up to $2GHz$ with wide dynamic range (8-bit). Furthermore, since the oscillating frequency is defined by the capacitor, it shows very small temperature and/or process variations compared to the ring-oscillator. The current-to-frequency conversion gain varies less than 3% across different process corners.

The physical layout of the CCO is very compact and area efficient. The core circuit only occupies $150\ um \times 100um$. Therefore, it is possible to integrate several of them onto one SoC.

The measured results prove the effectiveness of the CCO. It is able to run up to $550MHz$. It quits oscillating at high frequency because of the parasitic capacitance and the layout imperfections. The main nonlinearity of the transfer characteristics are the even order harmonics. Therefore, we are able to improve the linearity substantially by using the pseudo-differential structure. In summary, the proposed linear current-controlled oscillator exhibits wide tuning range. Its compact structure and low PVT sensitivity is very attractive.

6.2 FUTURE WORK

Based on the current work in this thesis, we can explore the opportunities in the three following directions:

1) Pseudo-differential structure: As discussed in Chapter 5, the main nonlinear components are even order harmonics. Thus, we can improve the CCO linearity by using the pseudo-differential structure.
2) Other linearity improving techniques: It is meaningful to design CCOs for different frequency range/linearity requirement with different techniques discussed in Chapter 3.
3) Low voltage CCO design: The CCO is able to operate properly even with 0.5v supply voltage. Therefore, it is very interesting to design it in ultra-low voltage environment for low power biomedical applications.

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