The Thesis Committee for Li Ji
Certifies that this is the approved version of the following thesis:

SiO_x-Based Resistive Switching Memory Integrated in a Nanopillar Structure Fabricated by Nanosphere Lithography

APPROVED BY

SUPERVISING COMMITTEE:

Supervisor:

Edward T. Yu

John G. Ekerdt

SiO_x-Based Resistive Switching Memory Integrated in a Nanopillar Structure Fabricated by Nanosphere Lithography

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Li Ji, B. E.

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Dedication

To my parents and my wife

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The work described herein would not have been possible without the help from my roommate, Yao-Feng Chang. He has extended my vision to the field of RRAM and has helped me on the measurements and analysis of data. Special thanks go to Dr. Ping-Chun Li for valuable advice and suggestions.

Finally, I would like to appreciate my parents, Liji Wu and Jian Li, for their love and support throughout my education. I am also grateful for my wife, Lufang Zhang, for her love, trust and understanding.

Abstract

SiO_x-Based Resistive Switching Memory Integrated in a Nanopillar Structure Fabricated by Nanosphere Lithography

Li Ji, M.S.E.

The University of Texas at Austin, 2014

Supervisor: Edward T. Yu, John G. Ekerdt

A highly compact, one diode-one resistor (1D-1R) SiOx-based resistive switching memory device with nano-pillar architecture has been achieved for the first time using nano-sphere lithography. The average nano-pillar height and diameter are 1.3 μm and 130 nm, respectively. Low-voltage electroforming using DC bias and AC pulse response in the 50ns regime demonstrate good potential for high-speed, low-energy nonvolatile memory. Nano-sphere deposition, oxygen-plasma isolation, and nano-pillar formation by deep-Si-etching are studied and optimized for the 1D-1R configurations. Excellent electrical performance, data retention and the potential for wafer-scale integration are promising for future non-volatile memory applications.

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Chapter 1: Introduction

1.1 Reemergence of Memristor

The capacitor, resistor, and inductor, were considered as the three basic electrical circuit elements for a long time. In 1971, Leon Chua postulated the fourth basic circuit element naming in the *memristor* (memory + resistor), in which the nonlinear resistance can be memorized indefinitely by controlling the flow of the electrical charge or the magnetic flux, as shown in Figure 1[1].

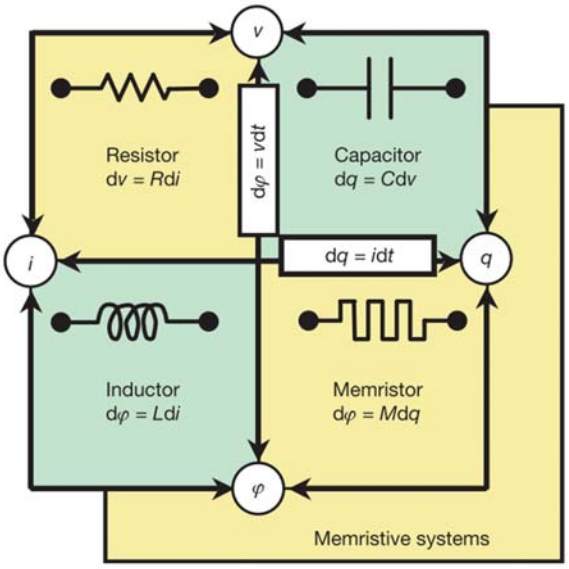


Figure 1. The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor [2].

The observations of such behavior, mainly in oxides insulators, have been reported for over 40 years [3-6]. The early observations of resistance switching were not robust enough for real applications and remain only for scientific studies. Through there were

initial attempts to validate Chua's theory for practical design, the complexity involved in implementing memristors made them impractical for commercial products. The recent revival of interest in such resistive switching started in late 1990s, with perovskite oxides such a $SrTiO_3$ and $SrZrO_3$. In 2004 *International Electron Devices Meeting* (IEDM), Samsung presented a paper demonstrating NiO cells integrated with conventional complementary metal-oxide-semiconductor (CMOS) in a one-transistor-one-resistor (1T1R) device architecture [7]. This work suggested a memory technology based on resistive switching may be feasible. Particularly in 2008, a paper in *Nature* by a group from Hewlett Packard (HP) demonstrated memristive behavior in crossbar memory arrays based on TiO_2 and credited the work of Leon Chua in 1970s to the phenomenon they observed[2]. Since the reemergence of this missing memristor, the research output has grown exponentially with publications in conferences and journals.

Within the semiconductor industry, it is considered that the transistor based flash memory technologies are approaching the end of scaling, because the building block of current CMOS technology will be difficult to scale below 10 nm regime due to increasing tunneling current, loss of gate control and increased threshold fluctuations. In addition, for a charge-storage memory, it becomes difficult to control or retain electrons with continuing shrinking of dimensions. Hence, to meet markets' fast growing demand for portable electronic devices, many concepts and studies for non-field-effect-transistor (non-FET) based memories have been pursued as potential alternatives for Flash memory, such as carbon memory[8], Mott memory[9], Ferroelectric-RAM (FeRAM)[10-14], Organic-RAM (ORAM)[15-17], Resistive-RAM (RRAM)[16, 18-39], as shown in Figure 2, which illustrates the taxonomy of emerging memory devices cited from *The 2013 International Technology Roadmap for Semiconductors* (the 2013 ITRS) [40].

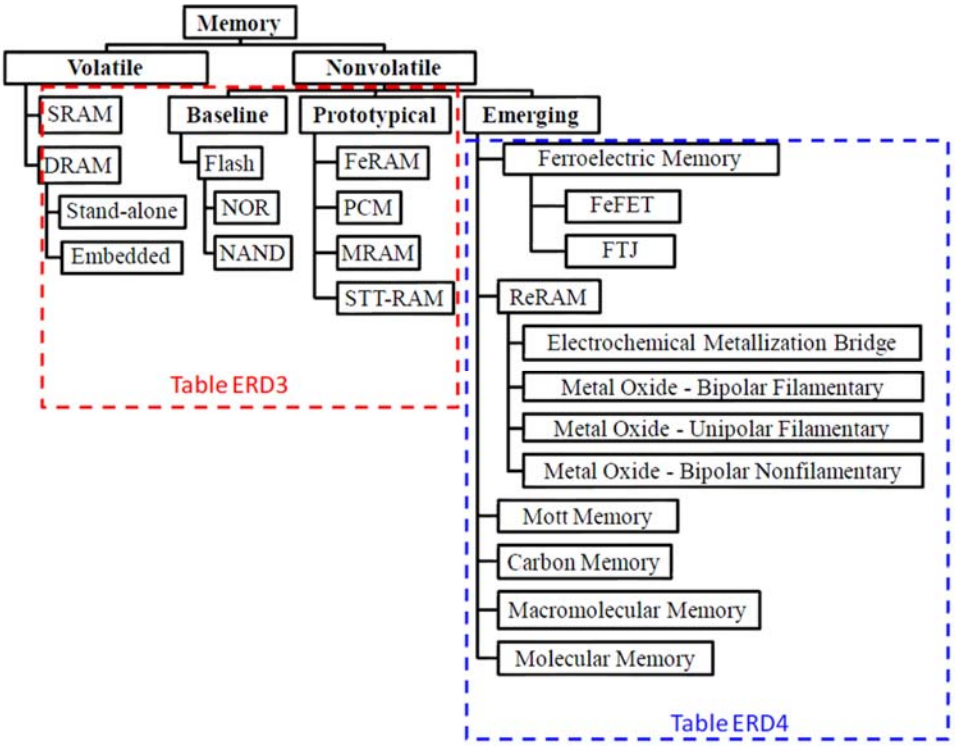
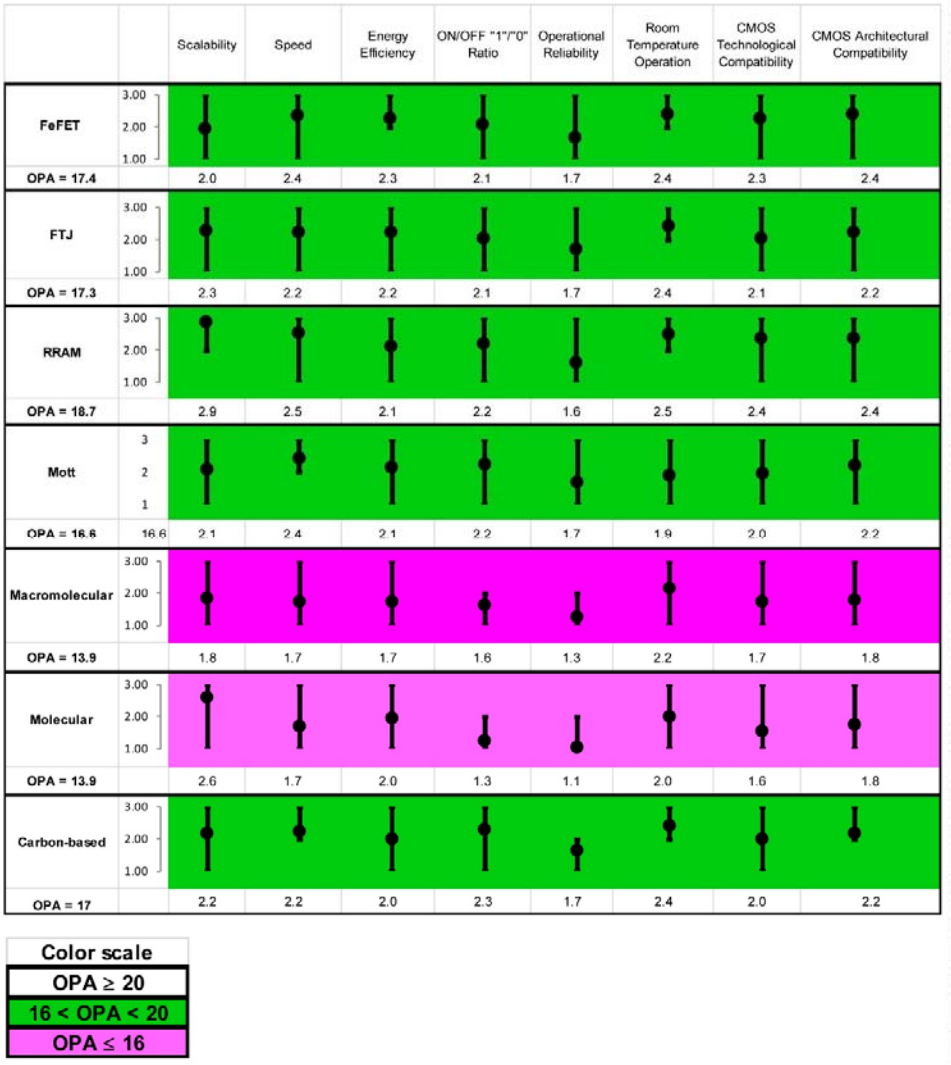


Figure 2: Taxonomy of emerging memory devices. Cited from *The 2013 International Technology Roadmap for Semiconductors* (ITRS).

A new memory will ideally combine the best features of current memories including the high density of DRAM, fast speed of SRAM and nonvolatile property of flash memory with a CMOS compatible fabrication technology. Table 1 is the list of the Overall Potential Assessment (OPA) for all emerging memory devices of becoming a viable, manufacturable memory. Among all of them, RRAM stands out with a highest OPA score. Overall RRAM assessment is similar to or better than existing CMOS-based nonvolatile memories (Flash). A clear advantage of RRAM is scalability owing to the filamentary conduction and switching mechanisms. The smallest feature can be scaled down to 5 nm [41]. The simple device structure, metal-insulator-metal stack, and fab-friendly materials also contribute to high raging in CMOS compatibility. For FeRAM and Ferroelectric

Tunnel Junction (FTJ) memory, the major challenge is the control of ferroelectric-semiconductor interface. The scalability of both beyond 22 nm generation is uncertain. Mott memory is considered to have fast speed but suffers from the operation temperature and reliability. Organic-based RAM, Macromolecular Memory and Molecular Memory, face severe reliability challenges [40].

Table 1: Potential Evaluation for Emerging Research Memory Devices. Cited from *The 2013 International Technology Roadmap for Semiconductors* (ITRS).



1.1 Classification of RRAM by Switching Modes

The architecture of RRAM is simple. The resistive switching element is a two-terminal devices with an active resistive switching layer sandwiched between two metal electrodes. The switching event from High Resistance State (HRS) to Low Resistance State (LRS) is called the *set* process. Conversely, the switch from LRS to HRS is named the *reset* process. For a fresh sample, a sufficiently large voltage (> set voltage) is usually applied to remove the initial resistance state for the subsequent cycles. This process is called *forming* process. It is worth noting that an enforced compliance current is usually applied during set process to avoid a permanent dielectric breakdown. This can be done by a semiconductor parameter analyzer (for individual device tests) or by a memory cell selection transistor/diode or a series resistor (in more realistic circuit implememtations) [42]. Based on the different phenomenological behavior, the switching modes of RRAM can be generally classified into two switching modes: unipolar and bipolar.

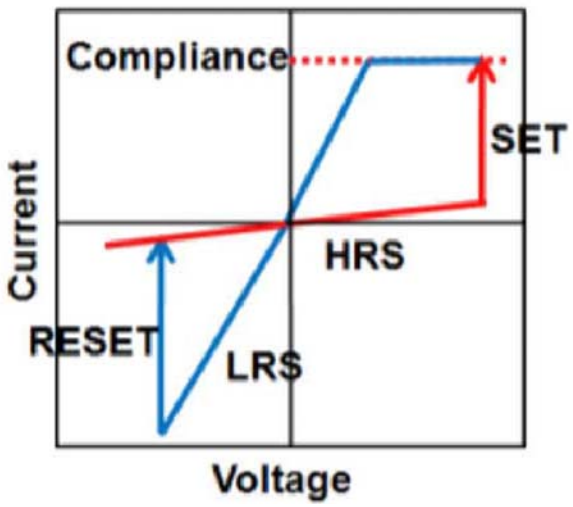


Figure 3. I-V characteristics in a bipolar type RRAM. The arrows indicate the voltage sweep directions. Compliance current is applied during set process. Graphics are reproductions from Ref. [42].

Figure 3 is the I-V characteristic of a typical bipolar type RRAM. The change of resistance is dependent on voltage sweeping polarity. Set occurs at one polarity while reset occurs only at the other polarity. This type of switching behavior can be observed in many metal oxides, such as perovskite oxides, TiO_2, HfO_2 or metal-doped SiO_2.

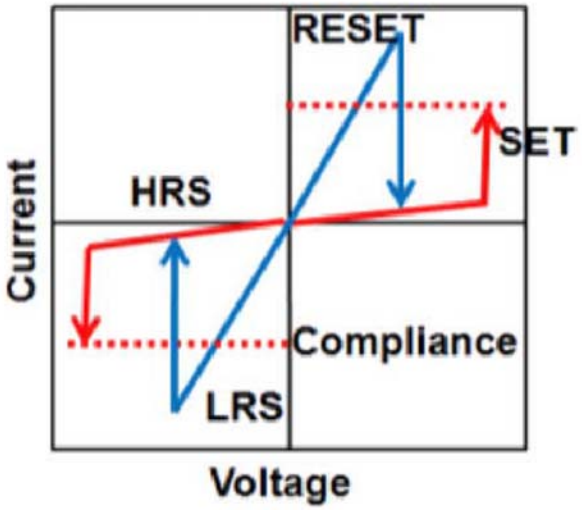


Figure 4. I-V characteristics in a unipolar type RRAM. The arrows indicate the voltage sweep directions. Compliance current is applied during set process. Graphics are reproductions from Ref. [42].

Figure 4 is a representative I-V characteristic for unipolar type RRAM. The resistance switching depends only on the amplitude of voltage but not on the polarity, whether it is positively or negatively biased. As shown in Figure 4, the change from HRS to LRS is the set voltage. The reset process, from LRS to HRS, doesn't require a compliance current. This type of behavior is usually observed in highly insulating oxides, such as nickel oxide [24, 43-51], aluminum oxide [19, 52, 53], zinc oxide [23, 32, 54-56] and silicon oxide [57-82].

1.2 Classification of RRAM by Switching Mechanisms

Based on the switching mechanism, RRAM can be categorized as (i) 1D filamentary type, including thermochemical fuse/antifuse, oxygen vacancy migration and electrochemical switching or (ii) 2D interfacial type, based on the change of Schottky barrier height between oxide/metal interfaces, as illustrated in Figure 5.

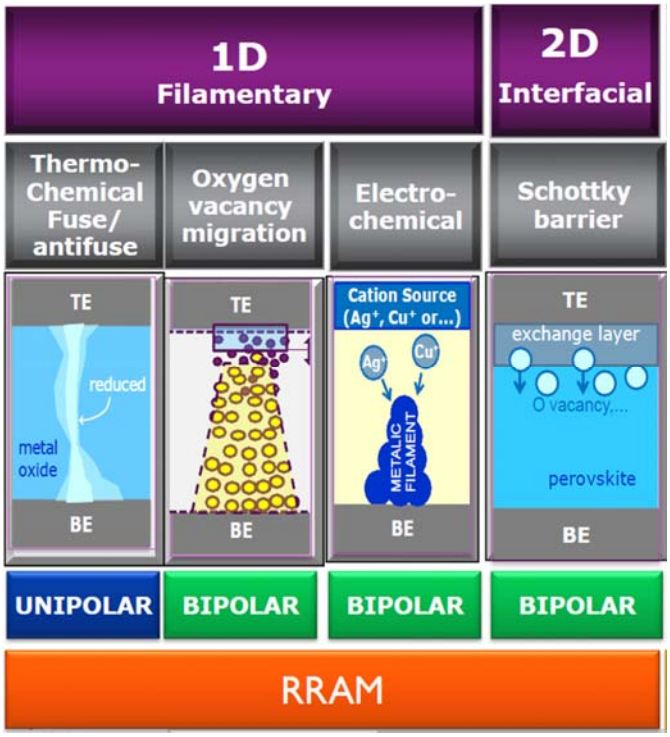


Figure 5. Resistance Modulation Geometry. Cited from tutorial of *43rd IEEE Semiconductor Interface Specialist Conference* (SISC), by Dirk Wouters from IMEC.

For a unipolar type thermochemical fuse/antifuse RRAM, a conducting filament is formed during the forming process. During the reset process, the conducting filament is antifused or ruptured due to the Joule heating effects when a high current flowing through

it. During the set process, the filament is fused when a sufficiently applied with high electric filed.is applied

Oxygen vacancies are considered to be the origin of resistive switching phenomena in various transition metal oxides, such as NiO [24, 49, 50, 83-85], $SrTiO_3$ [86-90] and TiO_2 [91]. For example, the movement of oxygen vacancies, particularly at the boundary of metal electrode and oxide interface, changes the valence of transition-metal ions (*e.g.,* between Ti^{3+} and Ti^{4+} in TiO_2) and thus changes the conducting state [92].

Electrochemical RRAM or Redox type RAM (ReRAM) is based on mobil metal anions or cations embedded in a solid state electrolyte. The reduction-oxidization (redox) electrochemical process will create or annihilate of a metallic conducting path (metal filament), resulting in the switching between HRS and LRS. This type is intrinsically bipolar due owing to the polarity dependence of the electrochemical redox process. The ReRAM are usually metal doped systems, such as CuS [93] and metal doped SiO_2 [94-97].

1.3 Advantages of intrinsic SiO_x based unipolar type RRAM.

Owing to its low cost, high quality Si/SiO_x interface and excellent insulating properties, SiO_2 has been used as MOSFET gate oxide for many decades. The compatibility with CMOS technology makes SiO_x an excellent candidate for RRAM applications. In addition, the resistive switching behavior has been observed as early as 1962 by Hickmott [3] and has been modeled by Dearnaley in 1970s [5]. They observed that a simple device with $Au/SiO_x/Al$ structure can form an active device based on its repeatable negative resistance phenomenon. Recently, Tour's group from Rice University reported resistive switching behaviors based on SiO_x, indicating that this traditionally passive material can be converted to an active memory element by external electrical activation [60, 62, 63, 65, 77, 80, 81, 98].

In addition, intrinsic SiO_x shows unipolar type behavior and this property allows its integration into one-diode-one-resistor architecture, which yields the high density and reduced complexity. The purpose of many memory systems is to store massive amounts of data, and therefore memory capacity (or memory density) is one of the most important system parameters. A functional memory cell usually comprises two components: the 'storage node' and the 'select device', the latter of which allows a given memory cell in an array to be addressed for read or write. Both components impact scaling limits for memory. In a two-dimensional layout using planar select transistors the cell layout area is Acell = (6-8) F^2 (F is the smallest feature size in a technology node). In order to reach the highest possible memory density for 2D structure, a vertical selector can be used. As discussed above, for a bipolar type RRAM, the set and reset process have opposite voltage polarity. So it cannot be integrated into simple 1D-1R architecture. For a unipolar type, set and reset process have same polarity so opposite voltage is not required during operation and it is applicable for 1D-1R architecture. Since no transistors are involved, the scale down problem for transistors will not be a limiting factor in RRAM application. This provides the highest density attainable in a 2D planar structure ($4F^2$). Furthermore, this planar structure is conductive to multi-layer integration (3D stacking) and multi-level operation, further increasing the storage capacity.

1.4 Purpose of this work

Due to the simple MIM structure, RRAM can be easily incorporated into a cross bar structure, as shown in Figure 6.

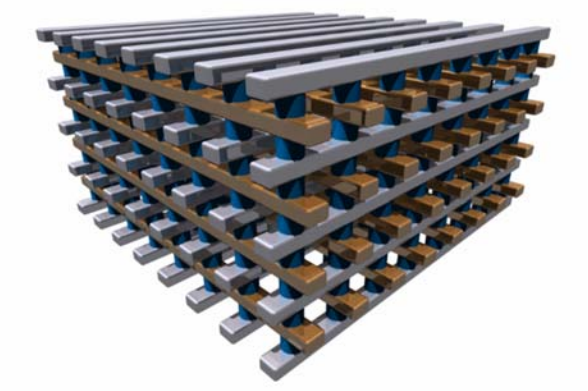


Figure 6. Schematic of a typical crossbar structure. Cited from Crossbar Inc. (https://www.crossbar-inc.com/)

However, the crossbar structure can lead to undesirable misreading of the state within a memory cell due to the *sneak path* issue between adjacent cells. The purpose of embedded diode elements is essentially to minimize leakage current through unselected paths (sneak paths). In this work, we fabricated 1D-1R nanopillar devices consisting of a SiO_x resistive switching element and p-n diode integrated in nanopillar structure. Nanosphere lithography was used because of its low cost, wafer-scale fabrication capability and high throughout in deep sub-micrometer region.

Chapter 2: Fabrication Processes

2.1 Substrate preparation

(100) n-type silicon wafers were purchased from a commercial vendor (University Wafer Inc.) with resistivity of 0.001-0.005 ohm-cm. 3 nm Ti and 100 nm Au were successively deposited onto the backside of the wafer as bottom contact via e-beam evaporation (PVD, CHA Industries). 60 nm thick SiO_x was deposited on the front side of wafer using the same method. Prior to each deposition, samples were dipped into buffered oxide etch solution (6:1) to remove the native oxide.

2.2 Hard mask fabrication

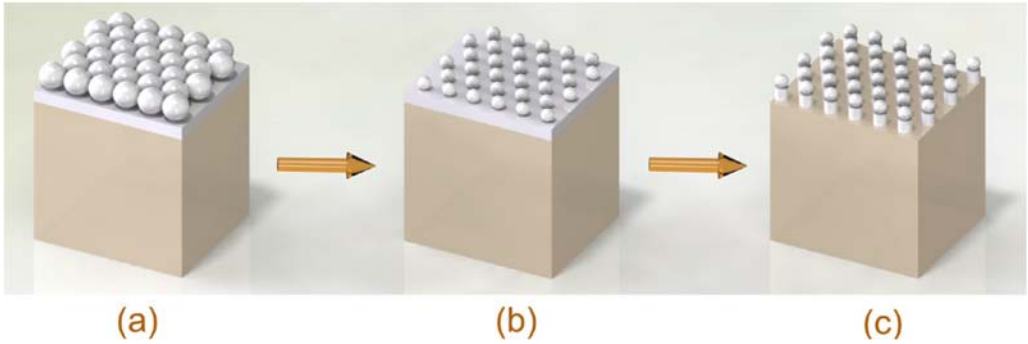


Figure 7. The process flow for hard mask fabrication with Nanosphere Lithography technique. The brown cubic box represents silicon substrate. The white thin film represents SiO_x. The white spheres represent for polystyrene nanospheres. (a) Nanosphere deposition on 60 nm SiO_x. (b) Reactive-ion etching (RIE) oxygen plasma shrinks the diameter of nanospheres. (c) RIE plasma for SiO_x dry etching to transfer the pattern into SiO_x layer.

18MΩ deionized water and 200nm polystyrene nanospheres (Polysciences Inc.) were used for nanosphere mask preparation. 200nm nanospheres were chosen due to a trade-off between minimum feature size and larger-scale uniformity. Polystyrene

nanosphere solution was dropped on top of microscope coverslips. This was then introduced to air-water interface in petri dish filled with 18MΩ DI water. The polystyrene solution spread out at the air-water interface forming monolayer. Prior to monolayer formation, a prepared silicon substrate with SiO_x coating was immersed at the bottom of petridish. The monolayer was then transferred to immersed substrate by slightly lifting the substrate. Then the sample was dried in air. The diameter of each NS in the monolayer was reduced by reactive ion etching (Oxford 80 RIE) in oxygen-plasma (80 sccm O2; power 60 W; pressure 100 mTorr; 1 minute). The power, partial pressure, and time of etching were optimized to obtain the desired size. The 1R array is formed by RIE (5 sccm Ar + 5 sccm O2 + 80 sccm CF4; Power 100 W; pressure: 200 mTorr) to transfer the treated NS pattern into the SiOx layer (Figure 7c, with average diameter of 130 nm). The NS layer was removed by sonication in toluene for 15 min.

2.3 Nanopillars fabrication

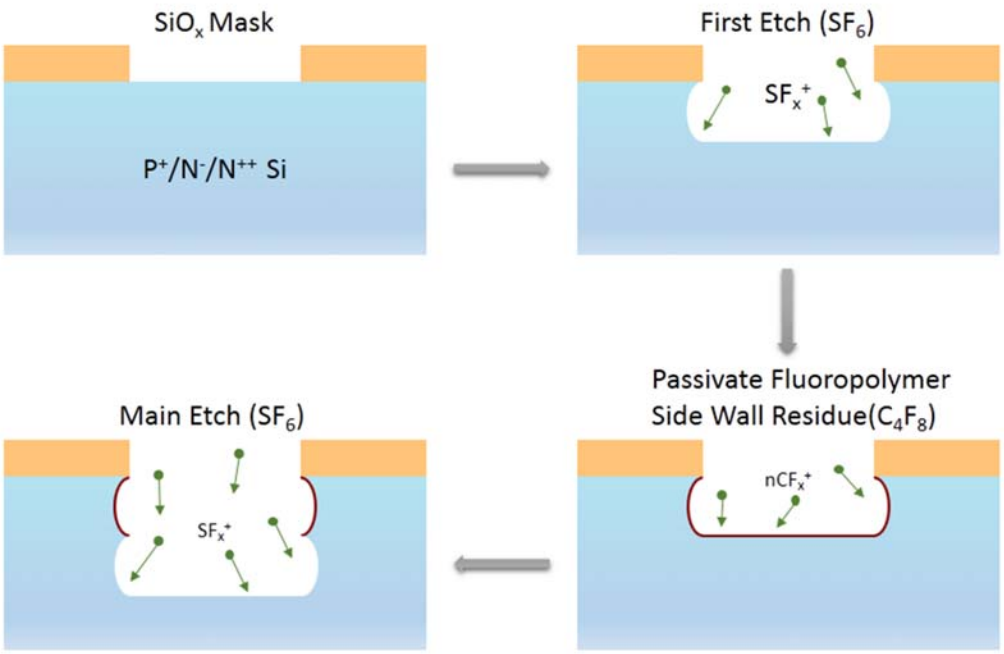


Figure 8. Schematic of Deep Silicon Etch (DSE) process.

For high aspect ratio nanopillar fabrication, the Deep Si Etching (DSE) process was utilized as illustrated in Figure 8. The first etching process is aimed to expose the Si surface by Ar ion-bombardment (physical reaction) with SF_6 chemical reaction). The exposed Si surface is then passivated isotropically by C_4F_8-induced fluoro-carbon polymer deposition to limit isotropic etching in the next cycle. The main etch process is used to anisotropically bombard the bottom fluoropolymer and re-expose the Si surface to SF_6 chemical reactions. Then, repeating cycling of deposition and main etching.

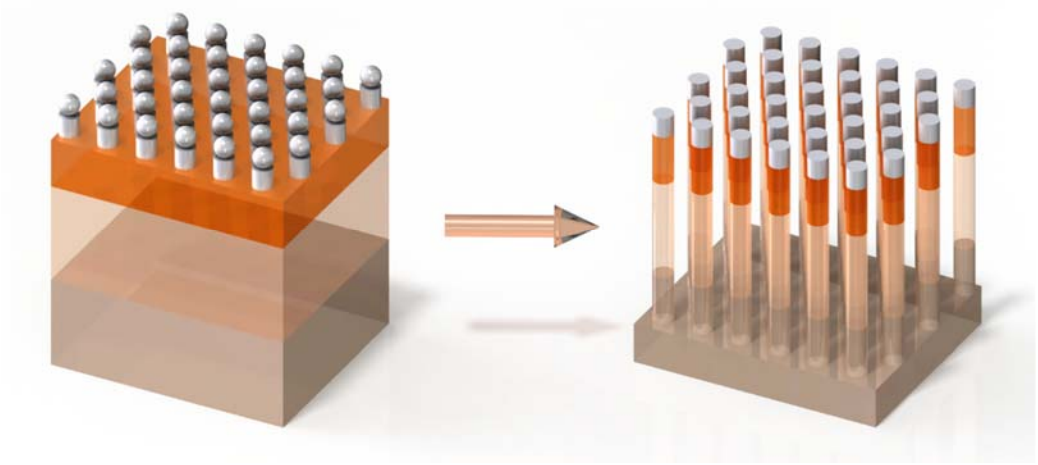


Figure 9. Schematic of 1D-1R pillar fabrication via deep silicon etch process. The different colors in substrate represents different doping concentration. Nanospheres were removed by ultrasonic bath in toluene.

Figure 9 is the schematic for 1D-1R fabrication process flow via deep silicon etch process. The only difference between 1R and 1D-1R is the difference of substrate doping level. For 1R, the substrate is (100) N^{++} Si wafer with resistivity of 0.001-0.005 ohm-cm. For 1D-1R, a $P^{++}/N^{+}/N^{++}$ epitaxial Si wafer is used as substrate (P^{++}: thickness 0.3 um, Boron (B), concentration 5×10^{19} cm^{-3}/ N^{+}: thickness 0.6 um, Arsenic (As), concentration 5×10^{16} cm^{-3}/ N^{++}: substrate, Phosphorus (P), concentration $1\text{-}7\times10^{19}$ cm^{-3}).

2.4 SEM Characterizations

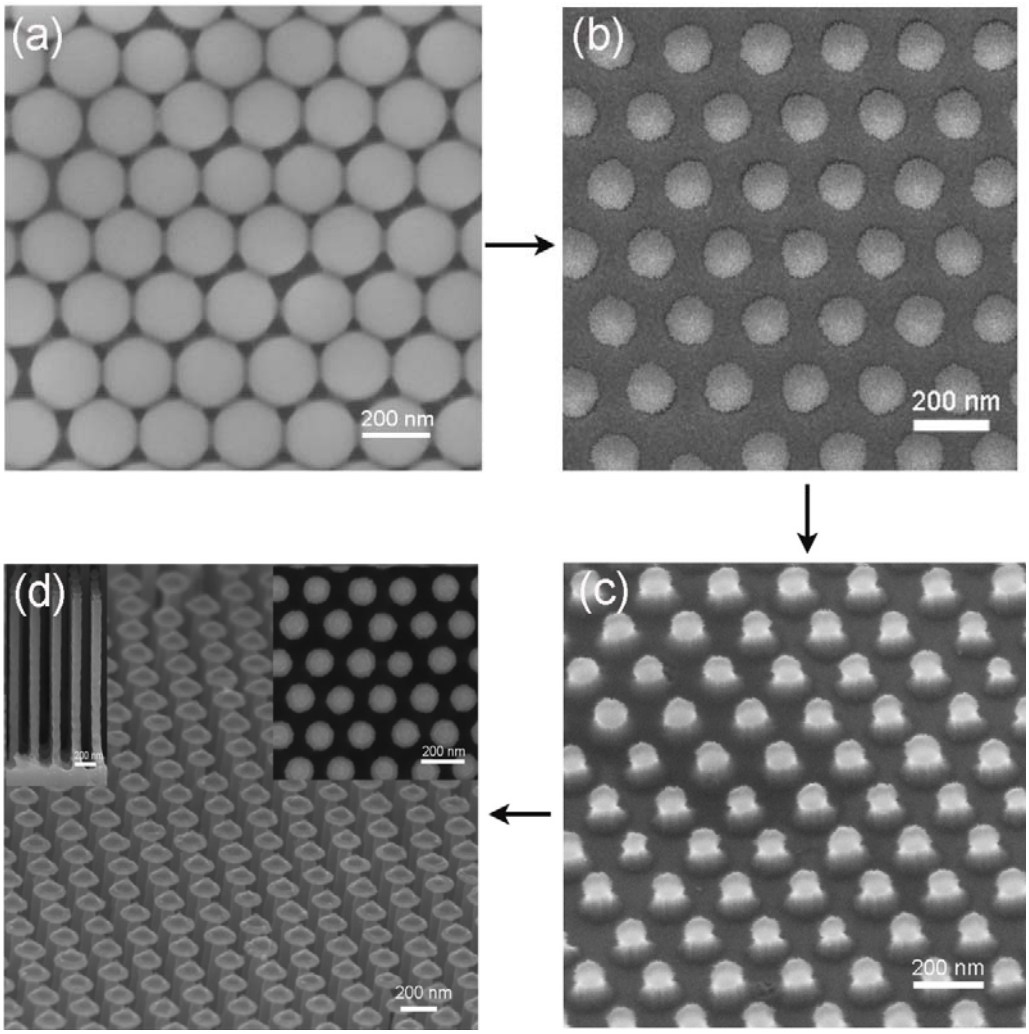


Figure 10. SEM characterization for each process. (a) nanosphere deposition, (b) RIE oxygen plasma shrinks the diameter of nanospheres, (c) RIE plasma for SiO_x dry etching to transfer the pattern into SiO_x layer and (d) top view, cross section view and tilted view of nanopillars after deep silicon etch process. The scale bars in every images are 200nm in length.

Figure 10 shows the SEM images after several key process steps. We could see compact hexagonal pattern of nanospheres with perfect arrangement in Figure 10 (a). After the oxygen plasma treatment, the diameter of nanosphere is reduces while the good

uniformity is preserved, as shown in Figure 10 (b). In Figure 10 (c), we can clearly observe the patterned SiO_x dots underneath nanospheres with a sharp contrast. Figure 10 (d) is the final nanopillar structure. The cross section view shows the nanopillars are straight and smooth. No scallops are observed, indicating a good optimization in etch recipe.

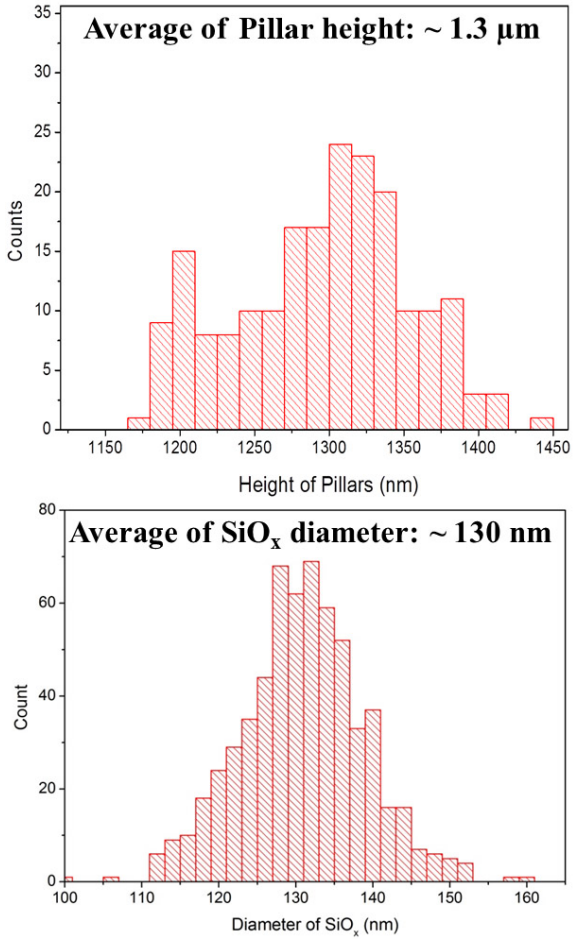


Figure 11. Statistics of average height and diameter of fabricated nanopillars. The average pillar height is around 1300 nm and the average pillar diameter is around 130 nm.

Figure 11 shows the average height and diameter of nanopillars are 1300 nm and 130 nm, respectively, with an aspect ratio ~ 10:1.

Chapter 3: Results and Discussion

3.1 Measurement setups

The electrical measurement was performed by Agilent B1500 Semiconductor Device Analyzer (Agilent Inc.). Samples were kept in a Lakeshore Cryotronics vacuum chamber with pressure lower than 1 mTorr. Bottom contact of the samples were connected to the chuck of chamber. A tungsten (W) probe tip (~10 μm radius) was used as a top electrode, directly contacting with SiO_x active layer. Voltage was applied to the top electrode with the bottom electrode grounded.

3.2 Results of 1R architecture

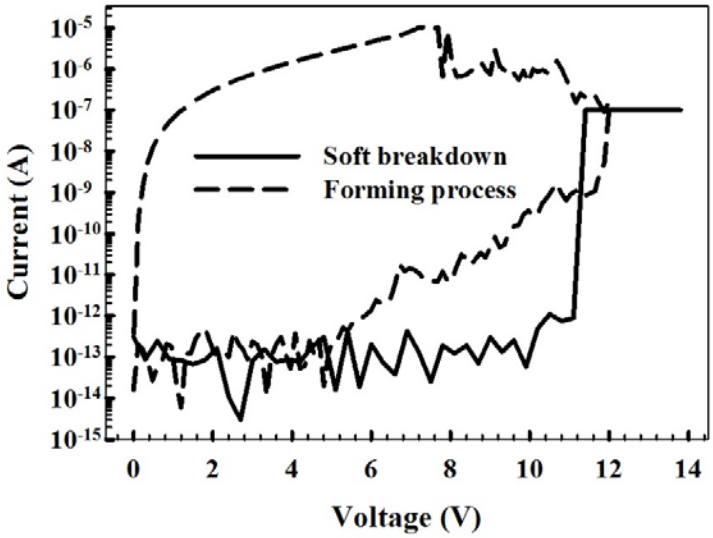


Figure 12. Double sweep forming process. The first run is soft breakdown, with compliance current fixed at 100 nA (solid line). The second run is forming process without any compliance current (dash line).

Figure 12 shows the results of an electroforming process. Here we utilized a double sweep method, with 1st sweep under fixed 100 nA compliance current and 2nd sweep without any compliance current. The purpose of soft breakdown is to avoid hard

breakdown and increase forming yield. A second forming sweep was done using forward/backward sweep, where current fluctuations are observed. During the backward sweep, the current keeps increasing and fluctuations are still present until hits a point after which the I-V curve becomes smooth, indicating a stable LRS is reached.

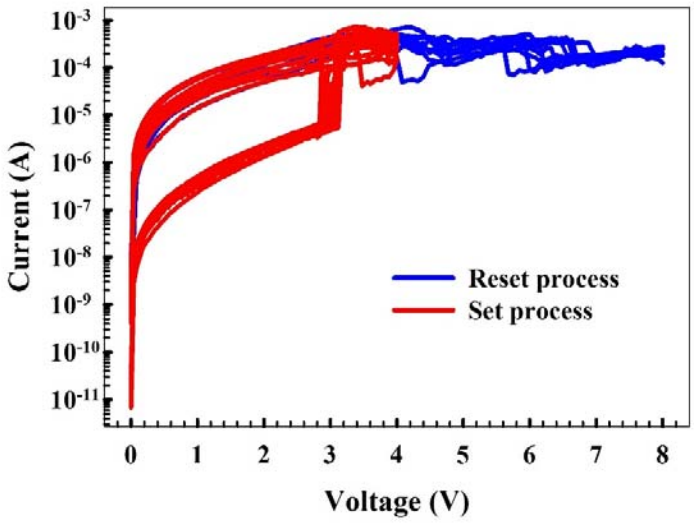


Figure 13. I-V characteristics for set and reset process for 1R structure samples.

The set process is a forward/backward scan without any compliance current. The current level has an abrupt change at 3 V during the forward scan. So the set voltage is around 3 V. For reset process, it is a forward scan from 0 V to 8 V. The current decrease as the voltage increases in range of 5 V to 8 V, during which the device is changed to HRS. Choosing 1 V as the reading voltage, the HRS/LRS ratio is around 50, satisfying the requirement of programming.

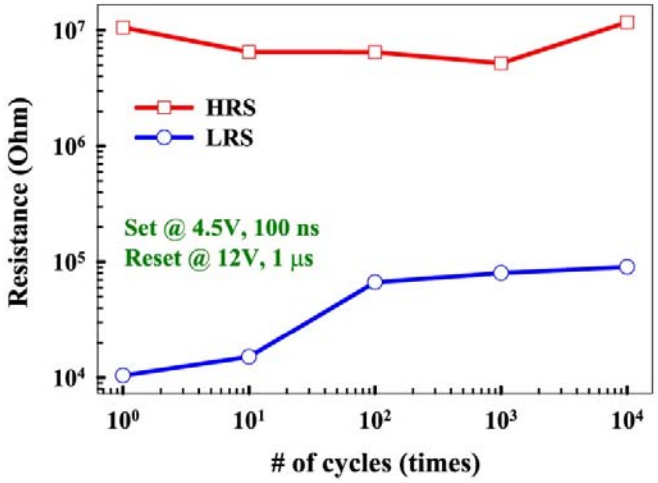


Figure 14. Endurance tests of 1R structure samples.

Endurance of HRS and LRS for 1R structure sample is shown in Figure 14. One order of magnitude difference in resistance between the HRS and LRS is maintained after 10^4 cycles. For endurance measurement, the devices were programed by applying a pulse, which is used in real-world circuit operation. For the set process, the pulse height and width are 4.5 V and 100ns. For the reset process, the height and width are 12 V and 1 μs, respectively.

3.3 Results of 1D-1R architecture

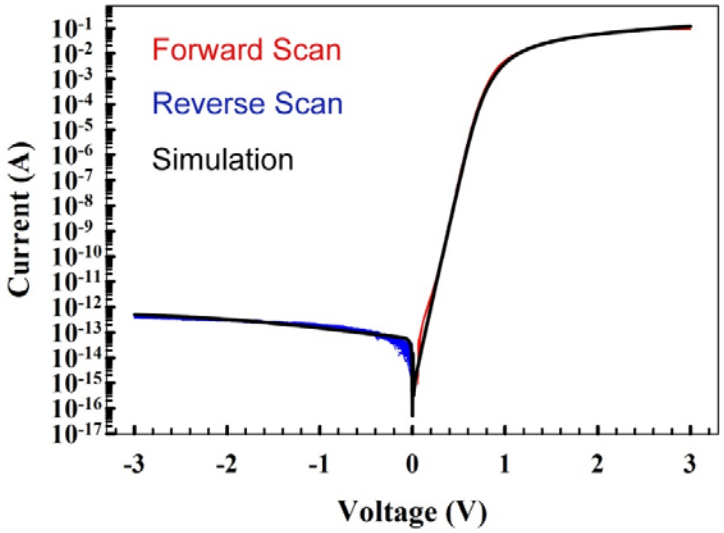


Figure 15. Characterizations and simulation of p-n Si diode used as 1D element in 1D-1R structure. Red line, blue line and black line are forward scan, reverse scan and simulation results, respectively.

For the characterizations of 1D-1R devices, the quality of diode should be checked first. Figure 15 shows the 100 cycles of nanopillars diode. The maximum current reaches 100 mA, high enough for the requirement of reset process. The reverse current is suppressed below pA regime, indicating the high quality of the diodes. The simulation was performed in standard TCAD software and the results fit well with experimental results.

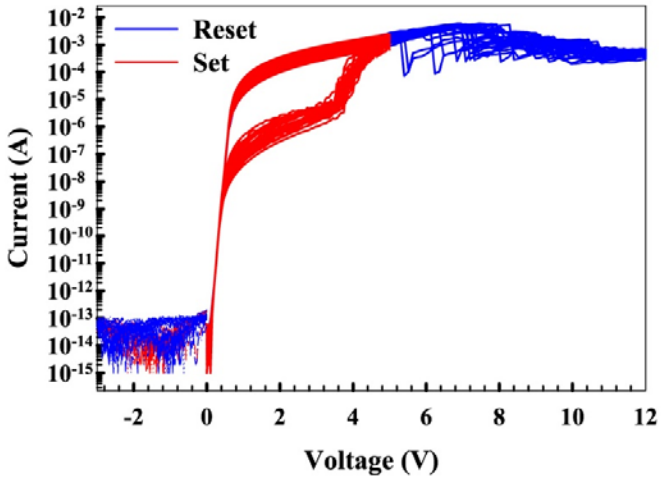


Figure 16. I-V results of set and reset process for 1D-1R structure samples.

50 switching cycles for 1D-1R devices are shown in Figure 16. The set voltage is around 4 V and the reset voltage is in range of 6 – 8 V, both of which are slightly larger than those observed in 1R devices. In addition, the current change during set process is more gradual. All these may be due to the series resistance involved with insertion of diode. It is worth noting that the reverse current level is smaller than 1 pA, attributed to the integrated p-n diode.

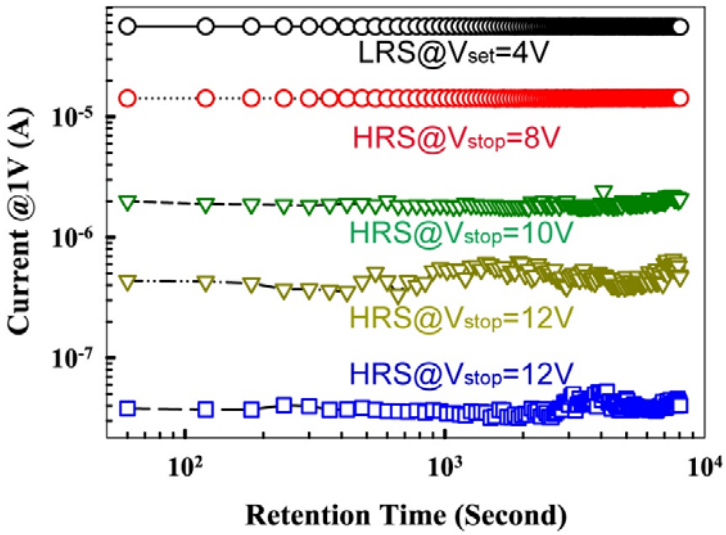


Figure 17. Retention measurement results of multi-level operation by controlling the reset stop voltage.

As shown in Figure 17, by controlling the reset stop voltage, the HRS level can be well controlled, confirming the potential for multi-level operation. When increasing the reset stop voltage, the current level of HRS is reduced. This is attributed the length of filaments can be modulated by the reset stop voltage. For all states, no obvious degradation are observed after 10^4 switching cycles.

Chapter 4: Conclusion and Future Work

4.1 Conclusion

We have demonstrated high density nanopillar shaped RRAM based on SiO_x. Nanosphere lithography technique was used for the fabrication of nanopillars structures. SiO_x served both as active memory layer and self-aligned hard mask. To solve the sneak path issue, epitaxial silicon p-n diodes were integrated vertically into nanopillars. Good resistive switching characteristics and reliability are obtained.

4.2 Future work

As described in measurement setups section, all data were obtained under vacuum (< 1 mTorr). Under ambient condition, the devices would become inactive after several switching cycles. The reason is still unknown. On possible mechanism is that the resistive switching behavior comes from the mobile proton in SiO_x, when exposed in an oxygen rich environment, proton will be oxidized, resulting in the loss of capability of switching. A similar phenomena has been observed as early as in 1997, in *Nature [57]*.

The future work will focus on how to efficiently protect the active device area from the oxidation environment. One possible way is to use high quality Si_3N_4, grown by plasma-enhanced-atomic-layer-deposition (PEALD), as the protection layer.

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Vita

Li Ji received the B.S. degree in Microelectronics from Xiamen University in China, in 2011. He entered the University of Texas at Austin in 2011 as a graduate research assistant in *Nanoscale Characterization and Devices Laboratory*, supervised by Prof. Edward T. Yu.

Permanent email address: nmgjili@utexas.edu & nmgjili@gmail.com

This thesis was typed by Li Ji.