On the Electronic-Photonic Integrated Circuit Design Automation: Modelling, Design, Analysis, and Simulation

by

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Abstract

Photonic networks form the backbone of the data communication infrastructure. In particular, in current and future wireless communication systems, photonic networks are becoming increasingly popular for data distribution between the central office and the remote antenna units at base stations. As wireless-photonic systems become increasingly more popular, not only low-cost implementation of such systems is desirable, but also a reliable electronic-photonic design automation (EPDA) framework supporting such complex circuits and systems is crucial. This work investigates the foundation and presents implementation of various aspects of such EPDA framework.

Various building blocks of silicon-photonic systems are reviewed in the first chapter of the thesis. The review discusses an example of a 60-GHz wireless system based on photonic technology, which could be suitable for the emerging 5th-generation (5G) cellular networks, and also provides design use cases that need to be supported by the EPDA framework.

Integrated photonic circuits, which are the building blocks of wireless-photonic systems, will achieve their potential only if designers can efficiently and reliably design, model, simulate, and tune the performance of electro-optical components. The developed EPDA framework supports an integrated optical solver, INTERCONNECT, to provide optical time and frequency domain simulations so that a designer would be able to simulate electrical, optical, and electro-optical circuits using two developed and implemented methodologies: sequential electro-optical simulation and co-simulation. We propose an algorithm to enhance the performance of electronic simulation engines that can be integrated into the EPDA simulation methods such as Harmonic Balance. It will be shown that body-biasing of CMOS transistors can be used as an effective method for tuning the performance of the electronic section of an electro-optical design. This can help designers adjusting the performance of their designs after fabrication. Modelling of electro-optical components is discussed in this thesis; It is shown that some traditional passive components such as inductors, which take a large amount of space in CMOS processes, could be fabricated in the much

lower cost photonic process and consequently the overall cost of silicon-photonic systems can be reduced significantly.

Preface

Except Chapter 2 which is the result of collaboration with my colleagues whose contributions are as follows:

- Section 2.2.1, 2.2.2, 2.5.1, 2.5.2, and 2.5.3 → Yun Wang, Hasitha Jayatilleka, Michael Caverley, and Lukas Chrostowski1
- Section 2.5.8, 2.5.9 , and 2.5.10 → Mohammad Beikahmadi , Amir Hossein Masnadi Shirazi, Reza Molavi, and ShahriarMirababsi

I, Ahmadreza Farsaei, am the principal contributor of all chapters. Dr. Shahriar Mirabbasi who is the research supervisor has provided technical support and editing assistance on the manuscript. Dr. Jackson Klein and Dr. James Pond, from Lumerical Inc., guided me through industry specifications needed for the development of the Integrated Photonic-Electronic Environment.

As mentioned below, some of the content of this thesis is written based on the following published works:

1. A. Farsaei, Y. Wang, R. Molavi, H. Jayatilleka, M. Caverley, M. Beikahmadi, A. H. M. Shirazi, N. Jaeger, L. Chrostowski, and S. Mirabbasi, "A Review of Wireless-Photonic Systems: Design Methodologies and Topologies, Constraints, Challenges, and Innovations in Electronics and Photonics," in Optics Communication, 2016 → Chapter 2
2. A. Farsaei, J. Klein, J.Pond, J. Flueckiger, X. Wang, G. Lamant, L. Chrostowski, and S. Mirabbasi, "A Novel and Scalable Design Methodology for the Simulation of Photonic Integrated Circuits," Photonic Networks and Devices. Optical Society of America, 2016. → Chapter 3 and 4
3. G. Lamant, J. Flueckiger, F. Villa, A. Farsaei, B. Wang, R. Stoffer, X. Wang, J. Pond, and T. Korthorsti, "Schematic Driven Simulation and Layout of complex Photonic IC's," accepted at 13th International Conference on Group IV Photonics. → Chapter 3 and 4

4. A. Farsaei, R. Molavi, and S. Mirabbasi, "On the Modelling and implementation of inductors in a photonic process," Photonic Networks and Devices, Optical Society of America, 2016. → Chapter 6

5. A. Farsaei and R. Safian, "An effective method for generating initial condition in harmonic balance analysis using method of nonlinear currents," Microwave Conference, 2009, APMC 2009, Asia Pacific, IEEE, 2009. → Chapter 7

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I am grateful to the professors who served on my Ph.D. examination committee and provided valuable feedbackand guidance on my research and thesis.

Dedication

This thesis is dedicated to my parents and my wife.
For their endless love, support and encouragement.

Chapter 1

Introduction

The idea of using light for transferring data has rapidly evolved since the invention of optical fibre and semiconductor laser in 1960s. Not only optical fibre's low loss makes it a suitable medium for transferring electromagnetic waves over long hauls but also its wide bandwidth allows for broadband communication. Furthermore, Wavelength Division Multiplexing (WDM) has made broadband optical communication more pervasive. Continuous advances in photonics technology along with the decrease in its deployment cost have made optical communication more popular for both long- and short-distance broadband communication applications. For example, in Local Area Networks (LANs), conventional copper wires are being replaced by optical fibres because of their cost-effectiveness and broadband nature [1, 2]. Moreover, Photonic devices, which are using light instead of electron to transfer information, demonstrate many advantages such data rate enhancement and a more energy efficient communication method.

One of the emerging applications of photonics technology is in the area of wireless communication where optical and wireless communication technologies are combined. In such wireless-photonics systems, the communication between the access point and the central router is established using optical fibre as is shown in Fig. 1.1. Furthermore, wireless-photonics systems are suitable candidates for emerging network architectures, such as small-cell cloud radio networks, and thus they offer a promising approach for signal distribution in many current and future applications such as the next-generation cellular systems [3]. The advantages of photonic systems, especially silicon-photonic systems, have provided us with many research opportunities related to the modelling, simulation, and analysis of these systems. As discussed in the next section, in this thesis, we focus on a few of these aspects.

1.1 Research Contributions

Chapter 2: Given the potential impacts of wireless-photonics systems, we will overview such systems as one of the emerging and representative appli-

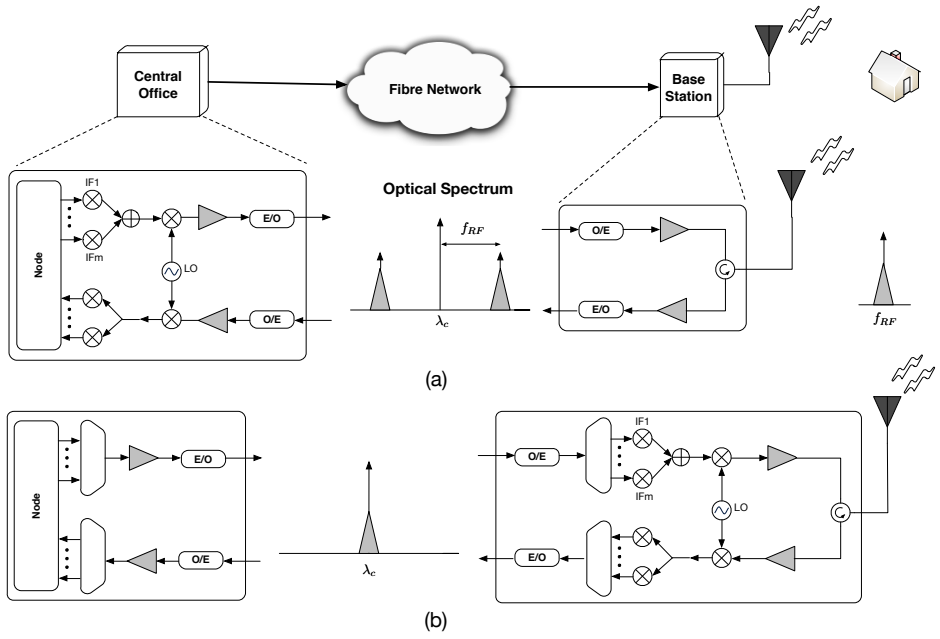


Figure 1.1: Radio signal transport schemes for optical-wireless links : (a) RF-over-fiber (b) Baseband-over-fiber. [1]

cations of silicon-photonics. In this context, we review the design methodology and topologies of different building blocks of the system, and present the challenges and constraints relevant to these building blocks. We will also discuss alternative ideas and techniques that offer benefits for silicon-photonics systems.

Chapter 3, 4, and 5: We discuss the development of an integrated design tool/flow as a software prototype/package, namely, an Integrated Design Environment (IDE) that facilitates the design in both optical and electrical domains, and therefore, the designer can use the IDE for an end-to-end design of silicon-photonic systems. Using the developed tool, we envision that the designer will be able to use optical components in the electrical environment, create an optical netlist (using the developed IDE), convert the netlist to a format readable for the engine of the optical tool, simulate the optical netlist (using optical engine), bring the results back to the electrical tool and properly show them to the designer. In the development of the IDE, a new technique and methodology for simulation of electro-optical systems having feedback is implemented and demonstrated. This IDE will provide

the foundation for a natural and efficient Electronic photonic design flow (EPDA) in the emerging field of silicon-electronics-photonics systems.

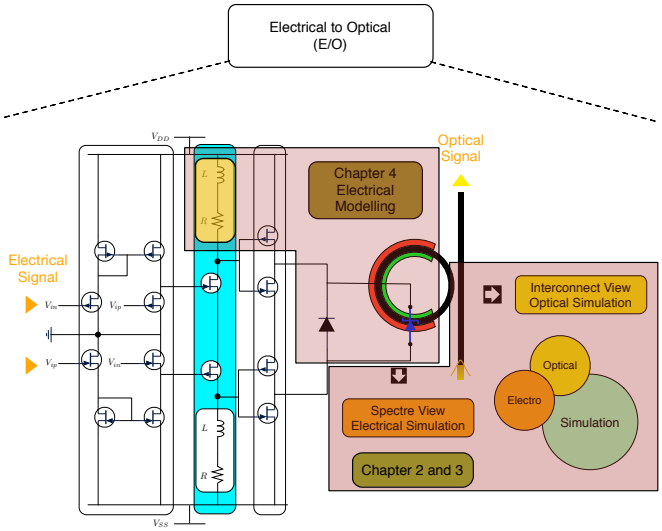
Chapter 6: As one of the main challenges in the above mentioned EPDA flow, We then present and demonstrate a few techniques and methodologies to model electro-optical components. It is shown that by accurate modelling and measurement techniques, it is possible to fabricate one of the most area consuming elements in a CMOS design, namely, an inductor, onto a photonic process. This not only decreases the total cost of fabrication for an electro-optical system but also offers efficient integration of photonic components, e.g., photodetector, and their corresponding electronic circuitry that typically employs a bandwidth enhancement techniques using inductors.

Chapter 7: Considering the nonlinear elements used in the design of a silicon-electronics-photonics systems and in the context of circuit simulation, we present a new method that enhances the convergence of nonlinear simulators such as Harmonic Balance and Period Steady State that could be used in the above EPDA flow. It is shown that this method could provide a nonlinear simulator with an initial condition that not only reduces the convergence time but also helps the diverging solution to converge. In Chapter 7, we will overview the fact that the response of a nonlinear circuit can be modelled by Volterra kernels. These kernels can be derived analytically and can be used for approximating the nonlinear response of the circuit. The Volterra based method is similar to the approach when a value of a function is approximated by its Taylor series expansion. We advocate that the approximate response can be used as an initial condition for other simulation methods such as Harmonic Balance and we show that such a choice offers improvements in the convergence of those simulation methods.

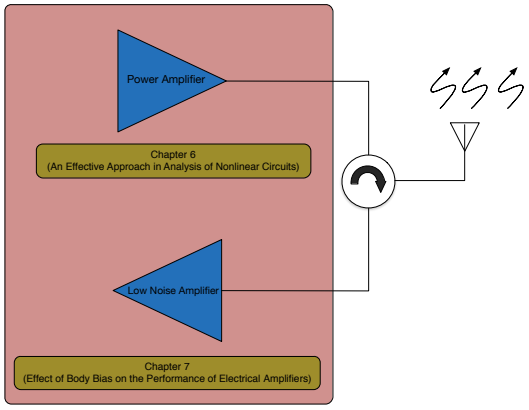
Chapter 8: Body effect in CMOS circuits is examined as an effective tuning method in the above mentioned EPDA flow both for electronic designs and electro-optical designs. It is shown that body biasing can be used as an efficient tuning mechanism to adjust and/or improve different performance areas. Such tuning could be beneficial not only in the design phase of a project but also as a post-fabrication tuning tool.

1.2 Thesis Structure

In different chapters of this thesis, different sub-systems of the an optical-wireless link is discussed as shown in Fig. 1.2 In Chapter 2, an overview of wireless-photonic systems is provided. Different topologies for building blocks of the system are discussed and their design approaches are exam-



(a)



(b)

Figure 1.2: Different chapters are dedicated to discuss an wireless-optical link's sub-systems 1.1 including design, modelling, simulation, and analysis

ined. The building blocks that are reviewed include: laser sources, optical modulator, CMOS drivers, optical couplers, optical filters, optical detectors, transimpedance Amplifiers (TIAs), low-noise amplifiers (LNAs), mixers, and voltage-controlled oscillators (VCOs).

In Chapter 3 and 4, development of a process design kit (PDK) for optical components in an electrical tool is demonstrated. The PDK is im-

plemented using a SKILL language provided by Cadence. Moreover, we will develop an efficient method to export electrical voltages and currents from the electrical tool (Cadence) and efficiently import them into the optical tool (INTERCONNECT); an efficient algorithm to read the data generated in the optical tool (i.e., INTERCONNECT) and properly show them to the designer in the electrical tool (Cadence). Data modelling of the simulation results is discussed and Parametric Storage Format is used as the data format of the generated simulation results. A calculator function is developed to extract the information of different optical modes from the simulation results and bundle them as a parametric waveform. co-simulation of a pulse amplitude modulation (PAM-4) is demonstrated using the developed IDE. A new technique and methodology are implemented and demonstrated that could be used to simulate electro-optical systems having feedback. All the above implemented functionalities are included in an IDE. The developed software package is the fundamental part of an electronic-photonic design automation (EPDA) flow. In Chapter 6 , a modelling methodology for an optical ring modulator is discussed and a compact electrical model based on the measurement results are proposed. Modelling of an inductor in a photonic process is also discussed in this chapter and inducor performance values such as quality factor, self resonant frequency (SRF), and inductance value are extracted from the measurement results. Furthermore, the benefits of its implementation in a photonic process is discussed. Chapter 7 is dedicated to a new algorithm proposed for efficiently solving nonlinear electrical circuits. It is demonstrated that typical algorithms for nonlinear circuits such as harmonic balance will not necessarily converge; and it is shown that he proposed technique not only t could enhance the convergence time and capability of Harmonic Balance but also most of nonlinear solvers, such as periodic steady state (PSS), can benefit from it. In Chapter 8 the effect of body biasing on different performance areas of the circuit are examined. This examination is done both using measurement results and theoretical calculations using Volterra series.

In Appendix A, the design, simulation, and measurement results of an assymettic Mach-Zehender Interferometer are discussed and the its temperature performance is evaluated based on measurement results. In Appendix B, some UML diagrams of the above mentioned IDE are shown.

Chapter 2

Wireless-Photonic Systems Review and Design Challenges

2.1 Introduction to Wireless-Photonic Systems

In wireless-photonics systems two popular communication approaches are [1, 4]: Radio-over-Fibre (RoF) and digital baseband optical communication (Fig. 2.1). It should be noted that in this classification, RoF includes both Radio-Frequency (RF) and Intermediate-Frequency (IF) over fibre. The overall structure of typical links using these two approaches are shown in Fig. 2.1; As it can be seen from the figure, the digital baseband approach does not require the RF up- and down-converters and thus its design is typically simpler. It should be noted that the modulation scheme commonly used in the digital baseband approach is On-Off Keying (OOK) which is significantly simpler as compared to the one used in RoF. In RoF, often, Quadrature Amplitude Modulation (QAM) or Orthogonal Frequency Division Multiplexing (OFDM) are used [4]. Although RoF uses more complex modulation schemes, it typically requires a lower bandwidth for the same data rate; it is likely the most straightforward radio signal distribution scheme because the wireless signals are transported directly over the fibre at the radio carrier transmission frequency and does not require frequency up- or down-conversion at the Base Station (BS) [1]. The key optical and RF components required at the Central Office (CO) and BS are shown in Fig. 1.1. As it can been seen from the figure, using RoF approach enables centralized control scheme and simpler BS implementation. As it is shown in Fig. 1.1(a), the wireless data that is to be transmitted is first modulated (for example, as shown in the figure the signal may be modulated onto a number of lower IF carriers and then multiplexes and up-converted to the desired RF carrier). Such RoF signal achieved results in an optical double side band with carrier that will be recovered using a photodetector in the BS

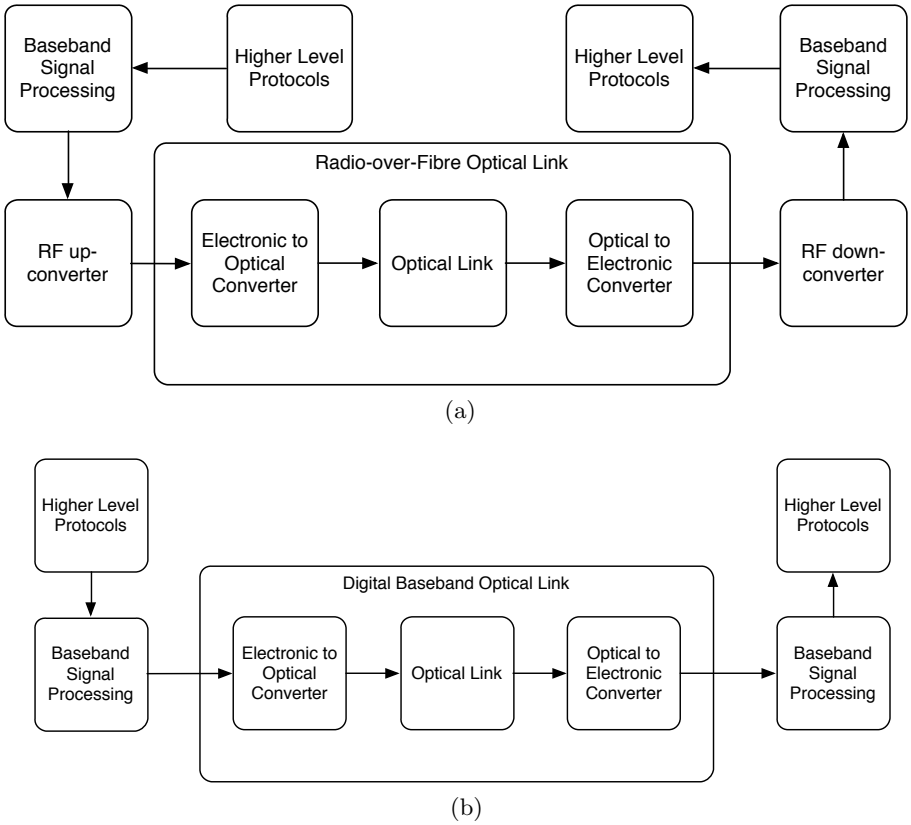


Figure 2.1: Overall structure of two general topologies for optical communication (a) Radio-over-Fibre, (b) digital baseband optical fibre communication [4]

and is then directly applied to the antenna. In the baseband approach, as is shown in Fig. 1.1(b), the digital baseband data is transferred to the BS and at the BS several data channels may be multiplexed and then up-converted using a Local Oscillator (LO); this approach can use existing mature and reliable RF and digital components at CO and BS as well as low cost opto-electronic components. In RoF technique the wireless signal in the system is already deteriorated by both the RoF optical link as well as the nonlinearities of the electrical to optical signal conversion process [1, 4]; this bring us to the key advantages of the baseband approach that are reduction in the number of errors in the data transmission and higher dynamic range [1]. These advantages can be attributed to the digital nature of the baseband approach.

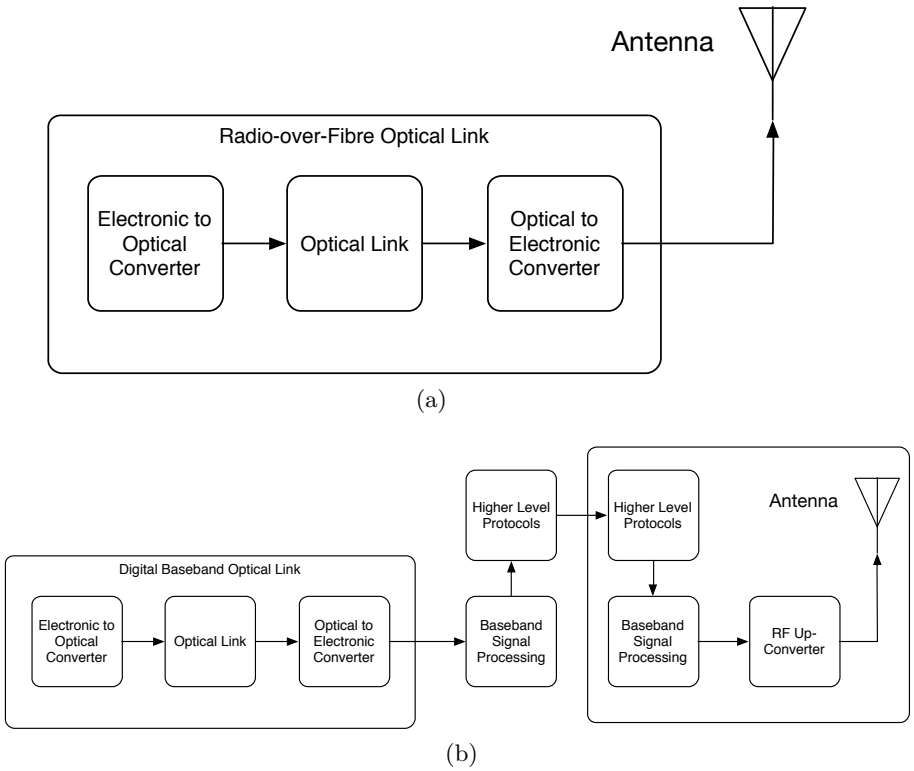


Figure 2.2: Including output stage for wireless communication in the overall structure of two general topologies for optical communication (a) Radio-over-Fibre, (b) digital baseband optical fibre communication [4]

From another point of view, the difference between the two approaches is related to a design trade-off between electronics and photonics. Namely, the RoF approach places much more stringent and challenging requirements on the optical side (e.g., linearity of the modulators), whereas the baseband digital approach places the challenge on the electronics, e.g., linearity of the mixers, high frequency amplifiers, Analog-to-Digital Converters (ADCs), and Digital-to-Analog Converters (DACs); a summary of advantages of each approach is mentioned in Table 2.1. In this paper, we focus on the baseband approach, where the biggest challenges are related to the electronics side. The photonics components can be implemented either using discrete, albeit expensive components, or in an integrated platform with potential lower cost (Fig. 2.3). Regarding such integrated platform, we focus on an implementation of electronic components using silicon Complementary Metal Oxide

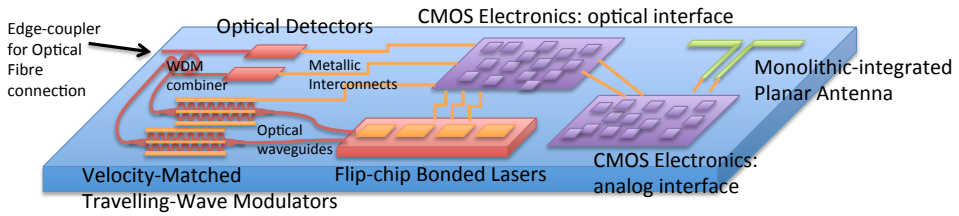


Figure 2.3: Proposed structure of an Access Point (AP) implemented as an integrated optical-wireless communication subsystem

Table 2.1: Comparison between RoF and Baseband Technique [1, 4]

RoF Advantages	**Digital Baseband Advantages**
Lower Bandwidth Requiremnt	Lower Cost
Transparency to Modulation	Digital Technique
Centralization	Lower Bit Error Rate

Semiconductor (CMOS) technologies. The optics may be implemented in a Silicon-on-Insulator (SOI) or silicon photonics technology [5, 6]. Such integrated platform has the potential for large volume production. In principle, the electronics and the photonics can be integrated on the same chip which reduces the footprint of the system as well as possibly the packaging costs [7, 8].

2.2 Optical Transmitter

2.2.1 Laser Source

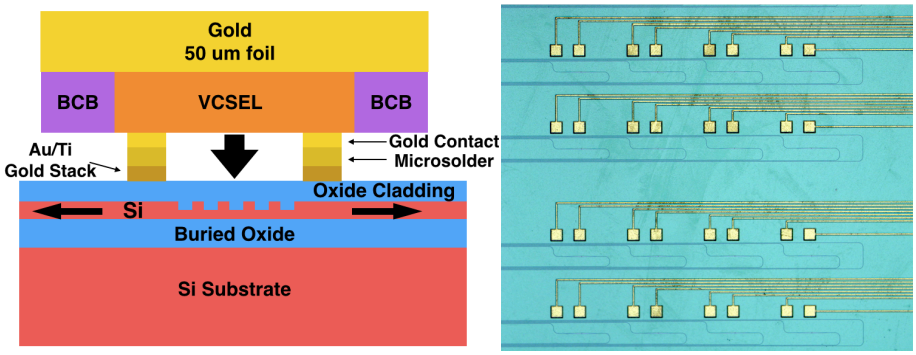
One of the most challenging issues faced by the silicon photonics community is the integration of the laser source. The solutions to address this issue mainly fall into three categories: 1) the monolithic on-chip solution achieved by epitaxial growth of III-V materials [9] or germanium [10] on silicon; 2) the hybrid on-chip solution achieved by heterogenous integration approach of bonding III-V materials onto the silicon photonics platform using wafer bonding [11, 12] or die-bonding [13–15] techniques; and 3) external laser or co-packaged lasers. The monolithic solution has challenges related to crystal properties and fabrication processes, whereas the hybrid solution takes advantage of separately fabricated III-V optical materials attached to silicon chips with potential bonding yield challenges. The third approach uses external lasers. The simplest method is to use a separately packaged

laser (e.g., butterfly package), and connect it to the silicon photonic chip via an optical fibre. Although it is the simplest to implement, it is costly and limited to low volume applications or those requiring exceptionally high performance lasers. For high volume applications, the laser can be integrated with silicon photonics via flip-chip bonding [7].

In this section, we focus on this latter approach that has already been commercialized, namely testing the external laser first, then aligning and bonding it to silicon photonics chips [7]. However, we discuss the integration of Vertical-Cavity Surface-Emitting Lasers (VCSELs) with silicon photonics [16]. VCSELs are a mature technology used data centre and high-performance computing, with the advantages of low cost, low power consumption, wafer-scale testing, fabrication in 2D arrays, and wavelength tuneability [17–19]. VCSELs can also be directly modulated, hence VCSEL-based communication links use VCSELs that are directly coupled to optical fibres. VCSELs have been integrated with CMOS electronics, for the purpose of integration with electronics drivers, using the flip-chip bonding technique [20, 21]; in this case, the alignment accuracy need only be tens of microns to ensure an electrical connection. However, to integrate the VCSEL as a light source for silicon photonics, the alignment accuracy requirement is much more stringent. Specifically, the output from the VCSEL needs to be precisely aligned to the optical coupler on the silicon chip. Here, we describe the approach using vertical grating coupler (Section 2.5.1) on the silicon photonics chip, which requires sub-micron alignment accuracy for the flip-chip bonding. This is at the limit of what commercial flip-chip bonders can achieve.

We integrated a 1550 nm VCSEL [19] with a silicon photonics chip using the flip-chip bonding technique [16]. The light from the VCSEL was coupled into the silicon photonic chip using grating couplers [22], in this case designed to couple light that is perpendicular to the chip, instead of the typical off-axis used in fibre grating couplers. The schematic of the bonding structure is shown in Fig. 2.4a. The output beam from the VCSEL is diffracted at the centre of the grating and couples the light equally into the waveguides on both sides of the grating. Adiabatic tapers were used on both sides of the vertical grating coupler to couple the mode from a 6-μm slab mode into a sub-micron silicon-wire waveguide mode. Detuned output grating couplers were connected to both arms of the vertical grating coupler. Detuned grating coupler is the grating coupler that couples light at an angle to the normal of the chip surface, therefore the second order reflection can be mitigated and the coupling efficiency can be improved. Fabrication of the silicon photonics chip was perforomed using electron beam lithography

[23]. Bond pads were designed for the silicon photonics chip matching the dimensions of the VCSEL pads, Fig. 2.4b. Therefore, when the VCSEL is flip-bonded to the silicon photonics chip, the pads on the silicon photonics chip can drive the VCSEL. In this example, the VCSEL had a threshold current of 1.3 mA with an output power of 1.4 mW with an applied current of 10 mA. Due to the polarization uncertainty of the VCSEL and the insertion loss from the input and output grating couplers, the measured power from the output grating coupler after bonding was much lower (by 13.5 dB) than before bonding. One challenge that has been identified is the requirement for the VCSEL polarization to match the polarization of the grating coupler; a polarization mismatch can significantly degrade the coupling efficiency. Further improvement can be made using optical feedback from the grating to control the polarization of the VCSEL [24] or using asymmetric oxide-aperture VCSELs and aligning to the polarization of the grating coupler. Further research is required to improve upon the coupling efficiency between the VCSEL and the silicon photonics.



(a) (b)

Figure 2.4: (a) Schematic diagram of the proposed strategy for integrating Vertical-Cavity Surface-Emitting Lasers with silicon photonics, using flip-chip bonding. (b) Top-view image of the silicon photonic chip, including an array of bidirectional vertical grating couplers and electrical bond pads. Ref. [16]

2.2.2 Optical Modulators

High-speed and efficient Si modulators are key components in the Si photonic links [25]. Silicon modulators based on ring resonator and Mach-Zehnder

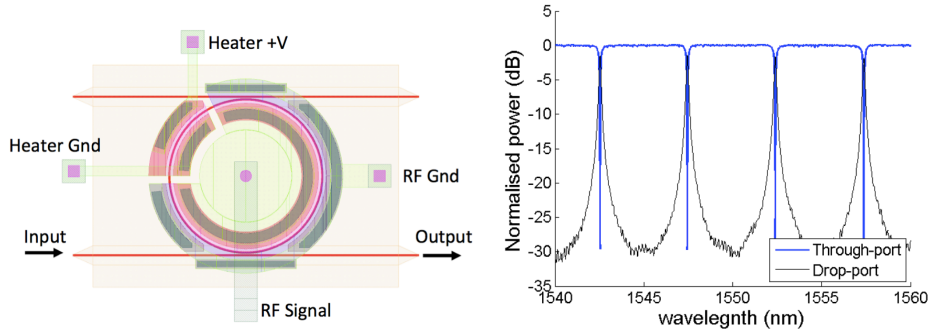
Interferometer (MZI) have been intensively explored [26–29]. In this section, we will focus on a reverse biased carrier depletion ring modulator for our application.

Ring Modulator

Microring resonator based modulators have the advantages of compact size, low driving voltage and low power consumption. One issue with optical resonators, however, is their temperature sensitivity [30], where thermal tuning is required for the ring resonator modulator. The device used in our system is an add/drop ring modulator, which has an integrated heater to allow wavelength tuning for the ring. The layout of our add-drop ring modulator is shown in Fig. 2.5(a). The modulator has a ring radius of 20 µm with a through-port coupling gap of 328 nm and drop-port coupling gap of 360 nm. The spectral response of the fabricated ring modulator is shown in Fig. 2.5(b). The ring resonator has a Q factor of 12500, with a FSR of 4.98 nm. The spectral response of the modulator near resonance, with DC voltage applied across the PN junction, is shown in Fig. 2.6(a). Fig. 2.6(b) shows the heater measurement, where various voltage was applied to the heater of the ring resonator so the resonance frequency can be shifted accordingly. The modulators electrooptic S21 response was measured using a 67 GHz vector network analyzer. The measured result in Fig. 2.7 indicates a 3dB bandwidth of 9.2 GHz with a -0.5 V bias voltage at operation wavelength of 1552.4 nm. By fitting the model to measure the reflection coefficient (S11) at 0V bias, we extracted that the capacitance of the PN junction we use was 42.7 fF. The modulation bandwidth of the device is subject to both the RC limit and the photon lifetime limit [6]. Large signal modulation has also been demonstrated. The signal generator was set to swing from -1.5 V to 0.5 V, in order to obtain 2 Vpp driving voltage. The resulted optical eye is wide open with 7.3 dB extinction ratio, as shown in Fig. 2.7(b).

2.2.3 CMOS Driver for Optical Modulators

The main role of a CMOS driver of an optical modulator is to properly condition the electrical signal and apply it to the the optical modulator for the electrical signal to be modulated onto the light. To get a better understanding of the properly conditioning of an electrical signal, a typical electro-optical modulator using a ring modulator is shown in Fig. 2.8 [31]. In this figure, the ring modulator is modelled using its effective index [32]. Schematic in Fig. 2.8 was simulated in frequency domain using Optical Net-

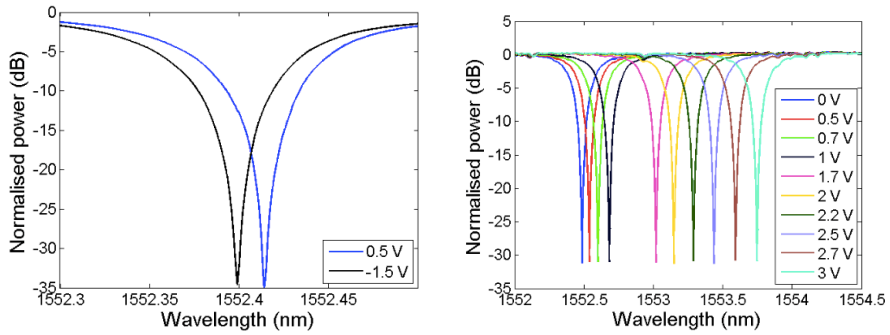


(a) (b)

Figure 2.5: (a) layout of a reverse biased ring modulator. (b) spectral response of the ring modulator

work Analysis (ONA) method; the DC source, modulation voltage, was also swept from 0 to 1.2. Simulation results are shown in Fig. 2.9. In case of designing a Wavelength Division Multiplexing (WDM) using multiple ring modulator, Fig. 2.9a could be used to specify the division between channels. A CMOS designer who is designing the driver for this ring modulator could use Fig. 2.9b to properly condition the electrical signal. As it can be inferred from Fig. 2.9b the voltage that is generated by the CMOS driver should be between the 0.5 and 1.1 to get a reasonable Extinction Ratio (ER). This means that the CMOS driver needs to provide a swing of $0.3V$ around $0.8V$. As it can be seen from Fig. 2.9b, increasing the swing of electrical signal will cause a bigger difference in the value of Transmission for 0 and 1 symbols which means a better Extinction Ratio and easier signal detection.

A standard implementation of a ring modulator can be divided into two categories: carrier-injection and carrier-depletion. Carrier-depletion type modulator has a higher modulation speed relative to carrier-injection duo to its ability to rapidly sweep the carries out of the junction. Considering the fact that carrier-injection ring modulators can provide larger change in the refractive index, these types of modulators can provide higher modulation depth; however, they are limited by relatively slow carrier dynamics of the forward p-i-n junction [33]. Having said that, electrical driver can be used to enhance the performance of the carrier-injection ring modulator by shaping the electrical signal. Increasing the optical rising transition by simply applying a high modulation swing not only leads to a slow optical falling transition but also causes the inter-symbol interference (ISI) [33]. A

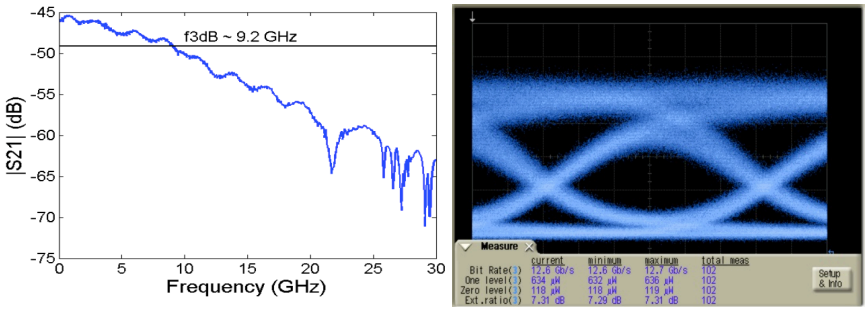


(a) (b)

Figure 2.6: (a)Spectral response of the modulator near resonance showing the resonance frequency shift as the applied voltage across the PN junction is varied. (b) Thermal tuning measurement of the ring modulator

useful technique is to use pre-emphasis modulation scheme to enhance the dynamic behavior of the ring modulator. In this technique, during the rise-edge transition a positive overshoot for a fraction of a bit period is applied to allow for high initial charge before settling to a lower level voltage which correspond to a lower charge density. Similarly, a negative overdrive voltage on the falling-edge is used to draw the junction carriers faster. Based on the optical modulator type, e.g., MZI or ring modulator, the topology of the driver would vary. Significant progress has been made in the past few years towards the design and fabrication of high-speed modulators [34–37]. One key step in the design of a CMOS driver for an optical modulator is to properly model the optical modulator in the electrical domain. For example, a ring modulator needs to be modelled electrically by measuring its scattering parameter (i.e., S_{11}); then creating its equivalent electrical model and find the respective parameters (for example, by adjusting the parameters such that the model's S_{11} is matched to the measured S_{11}). Such model can be used in the design of the CMOS driver. A schematic of a typical optical ring modulator with its equivalent electrical model is shown in Fig. 2.10.

An important and challenging task in the design of any electro-optical system is the modelling of electro-optical components such that the designer is able to model both the electrical and optical behaviour and use the models with the Computer Aided Design (CAD) tools. As an example, accurate modelling of a high-speed injection ring modulators requires inclusion of both electrical and optical dynamics; these electrical and optical dynamics can be modelled using an analog behavioural language, e.g., Verilog-A [38].



(a) (b)

Figure 2.7: RF characteristics of the ring modulator(The bit rate was 12.5 Gbps). (a) Electrooptic (EO) S21 parameters. (b)Large signal modulation. Wavelength = 1552.4 nm, bias voltage = -0.5 V, Vpp = 2 V (swing from -1.5 V to 0.5 V)

2.3 Driver Topology for a 10 Gbps Optical Modulator

One of the main tasks of the driver is to apply a proper voltage level to the modulator. Typically, the larger the voltage swing of the driver output the better the modulator will perform. There are different methods to maximize the voltage swing of the signal that is applied to the optical ring modulator. In some topologies two power supplies are used in the driver's implementation [37, 39] which may not be an optimal solution due to the use of multiple supplies. The overall structure of an optical ring modulator is shown in Fig. 2.11; the implementation of the driver section of the diagram in Fig. 2.11, which is fabricated in a 130-nm CMOS technology, is depicted in Fig. 2.12.

2.4 Driver Topology for a 25 Gbps Optical Modulator

Some techniques that are used for increasing the operational bandwidth of a Trans-Impedance Amplifier (TIA) can also be used to extend the bandwidth of an optical modulator driver. One of these techniques is shunt-peaking that

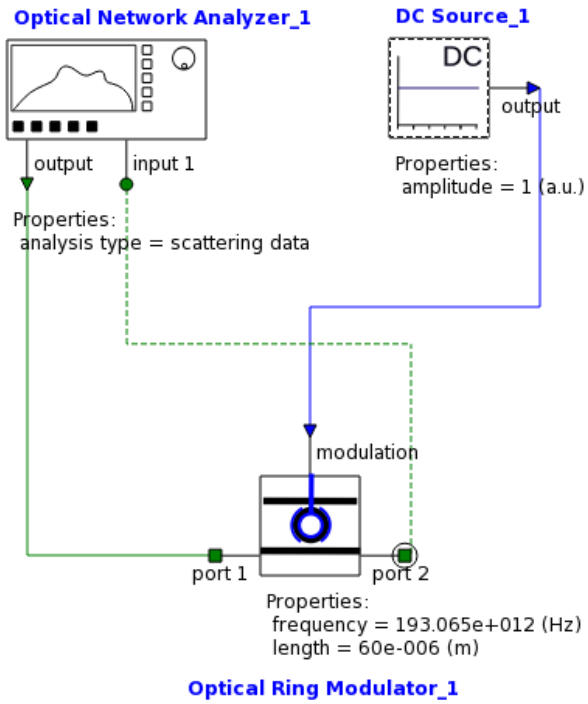
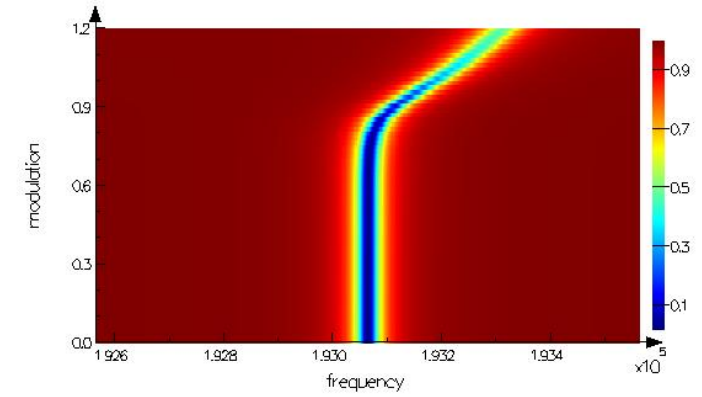
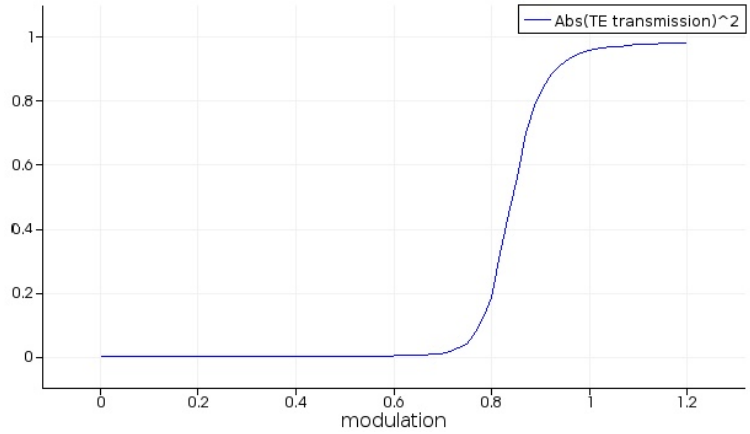


Figure 2.8: A typical electro-optical modulator drawn in INTERCONNECT [31]

is used in the design of the 25 Gbps driver [40] shown in Fig. 2.13. The basic concept of this technique is the fact that an inductor will resist any change in its current and therefore having an inductor in parallel with a capacitor will charge the capacitor faster (most of the excess current of the switched current source will charge the capacitor). In this specific case, the parallel capacitor is the gate-source capacitance of the next stage input transistor. The driver structure in Fig. 2.13 is an inverter type driver; to increase the voltage swing across the optical modulator the push-pull structure is used at the output stage, i.e., the cathode node swings between V_{DD} and GND and the anode node swings between V_{SS}, which is a negative voltage source, and GND. The first stage provides the correct voltage levels for the pre-amplifier section which is the second stage before the output push-pull structure.



(a)



(b)

Figure 2.9: Optical frequency analysis of Schematic 2.8 (a) Transmission over frequency and modulation, (b) Transmission at modulation frequency,193.065THz, for different values of modulation voltage [31]

2.5 Optical Receiver

2.5.1 Optical Fibre Connections to Silicon Photonics

High-speed optical links for distance over 2 km use single-mode fibre (SMF) as the medium of transmission. The THz-scale, low loss bandwidth of SMF in the optical C-band centered at 1550 nm has made it one of the most viable transmission medium for long distances, broadband communication

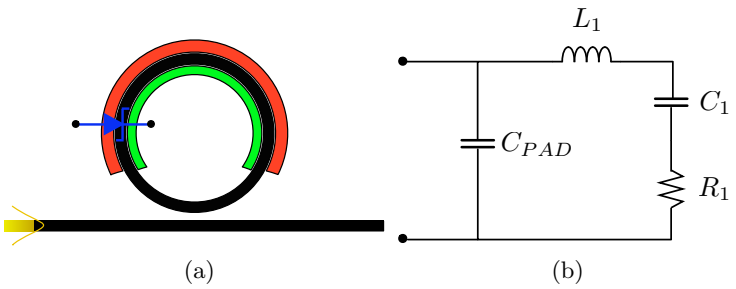


Figure 2.10: A typical optical ring modulator (a) Schematic, (b) Electrical model of the optical ring modulator [35]

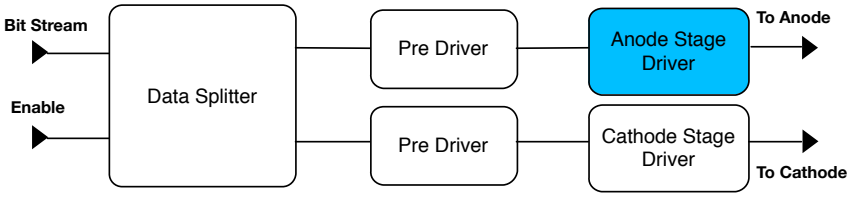


Figure 2.11: Overall Diagram of a CMOS driver for and optical ring modulator [37]

networks. Advantages of optical links over copper links such as 1) scalability of SMF to higher bandwidth using optical techniques such as wavelength division multiplexing (WDM) 2) limited capacity of copper links, suggests that fibre is replacing copper even for shorter links [41]. There are different techniques to couple light from a fibre to a silicon photonic chip. The silicon photonics is based on the silicon-on-insulator (SOI) platform. The high index contrast of SOI facilitates highly confined optical modes in the waveguides, thereby enabling dense on-chip integration of photonics systems. However, the highly confined optical mode also brings the mode mismatch issue between an optical fibre and the sub-micron silicon wire waveguide. To address the mode mismatch issue, two light coupling techniques, namely edge coupling or grating coupling techniques have been widely adopted.

Edge Coupler

Edge coupling using lensed fibres is a popular coupling technique to address the mode mismatch issue [42, 43]. The edge coupler has the advantages of broad coupling bandwidth and polarization insensitivity. Edge coupling

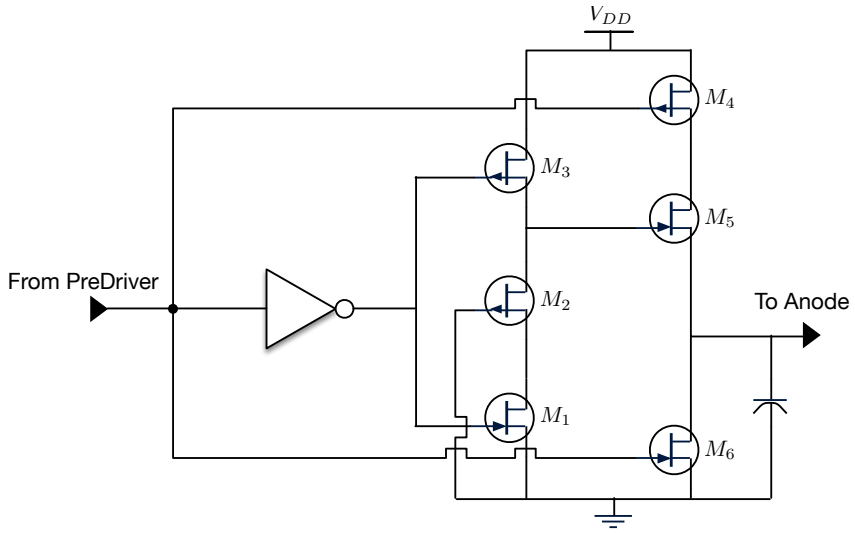


Figure 2.12: Implementation of the driver section fabricated in 130nm CMOS process [37]

is the standard technique for coupling to and from a single-mode fibre for most photonic devices such as DFB lasers, modulators, and high-speed detectors; packaging solution based on the edge coupling technique are well established. The challenges with edge coupling are related to the need for precision alignment which is typically done using active alignment, polishing/etching the facet, beam astigmatism, and the need for anti-reflection coatings.

An improved approach demonstrated by IBM uses evanescent coupling to the silicon waveguides, rather than coupling to their edges. It uses a polymer chip with mode-matching waveguides to transition from a fibre mode to evanescently couple to silicon waveguides [44]. The configuration is similar to an edge coupler spot-size converter except that the polymer chip is placed on top of the silicon chip instead of on the side. The structure offers improved coupling efficiency and a reduced alignment tolerance.

Grating Coupler

Compared with the edge coupling technique, grating coupler has the advantages of lower cost (e.g., no lensed fibres), reduced alignment accuracy requirements, small footprint, position flexibility, etc. Grating couplers also enable wafer-scale automated measurements, without the need

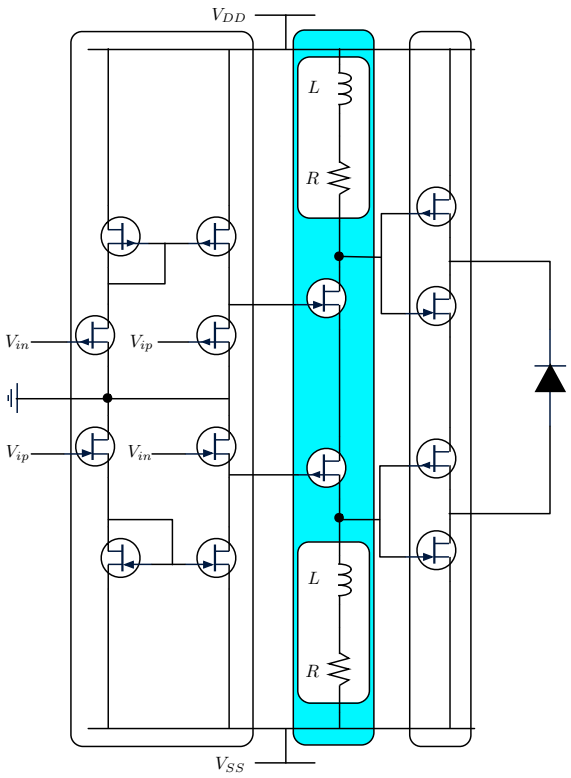


Figure 2.13: A 25 Gbps driver for an optical modulator: shunt-peaking technique is used to increase the operational bandwidth [40]

to dice the wafer. High-efficiency, shallow-etched grating couplers have been achieved though Multi-Project Wafer (MPW) foundries [45–47]. Compared with fabrication through MPW foundries with long turn-around times and time-consuming design rule checking, rapid prototyping using electron beam lithography provides a low-cost and rapid proof-of-concept alternative. When combining fundamental building blocks that can be fabricated in a single, fully-etched step, having fully-etched grating couplers provides an efficient and economical solution. Subwavelength grating couplers have been demonstrated [48–51]. We used a newly designed focusing subwavelength grating coupler for rapid prototyping of various photonics components [52] . With our automated measurement setup [6], thousands of devices can be designed, fabricated and measured within a week.

Fibre arrays can be packaged to grating couplers on silicon photonic chips [7]. This is achieved by glueing an array of fibres perpendicular to a

silicon photonic chip.

2.5.2 Wavelength-Division Multiplexing Filters

In order to increase the transmission capacity of an optical fibre, wavelength-division multiplexing (WDM) is typically used. WDM offers the potential of reduced optical packaging costs as a single fibre can be used to couple multiple optical channels into and out of the SOI chip. Add-drop filters are essential components for WDM systems, which have been extensively developed for the SOI platform [53–55]. We discuss two types of structures that can be used to implement the required wavelength filtering functionality, namely ring-resonator filters and the contra-directional coupler.

Add-drop Ring Resonator Filters

Ring resonator filters are attractive for add-drop filters in on-chip WDM systems because of their small footprint sizes and low tuning power requirements [56]. Fig. 2.14 shows how an array of ring resonator filters can be used to de-multiplex the channels of a WDM signal at the receive-end. The resonant wavelength of each ring is tuned to the carrier wavelength of the desired channel to extract the signal at this wavelength. Ring resonators on SOI platforms can support GHz linewidths making them suitable candidates for filtering of channels with multi Gbps data capacities. The filter response of a single ring resonator is approximately Lorentzian. Where necessary, several resonators can be cascaded to achieve a box-like higher-order filter response [57]. A single ring resonator can support multiple resonances, and the spacing between these resonances, the free spectral range (FSR), depends on the path length of the ring resonator. Hence, to avoid the filtering of multiple channels from the same resonator, all of the WDM channels should be constrained within one FSR the ring resonator filter. Typically, on SOI platforms, the FSR of a ring resonator cannot be increased beyond a few THz, thereby limiting the number of WDM channels [58]. To overcome this limitation, the Vernier effect is often exploited to create filters with an extended FSR [59] and to enable tuning of the filter across wide wavelength range [60]. Similar to ring modulators, the resonance wavelengths of ring resonator filters are highly sensitive to temperature and fabrication variations, which requires compensation using various electronic feedback control methods [61–63].

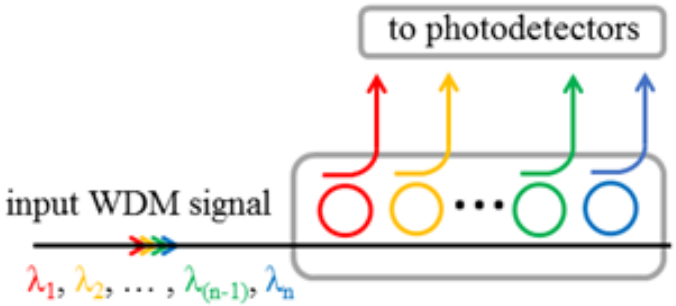


Figure 2.14: Array of ring resonator filters at the receive end for demultiplexing the WDM signal

Contra-directional Couplers

Ring-resonator based optical filters are limited by their comparatively narrow free spectral range (FSR). Contra-directional couplers (CDC), on the other hand, are based on Bragg gratings in which the bandwidth can be adjusted by design. A CDC is a four port device, and has advantages of wide bandwidth, single band operation, a flat-top channel feature, which make them suitable to be used as add-drop filters [54, 55], as illustrated in Fig. 2.15. The advantage of the contra directional configuration is that unlike the Bragg grating it is not a two port device, but rather a four port device. What was previously the reflection signal in the Bragg grating, is routed to the drop port in the CDC, which eliminates the need for optical circulators and isolators when used for optical filtering. It is also provides a fourth port which is used as the "add" port, hence the device can be cascaded to be used as an add-drop multiplexer. In order to obtain a large bandwidth, it is necessary to use an "anti-reflection" design in the waveguides, which eliminate the conventional Bragg reflection [64]. The CDC approach is very promising for both conventional WDM, as well as coarse WDM, applications.

2.5.3 Detector

The front-end of a typical optical receiver consists of a grating coupler, which is generally a periodic structure (periodic etch in SOI), used to couple light in and out of an optical chip, similar to electrical Input/Output(I/O) in an electronic chip; after light is coupled to the optical silicon waveguide from

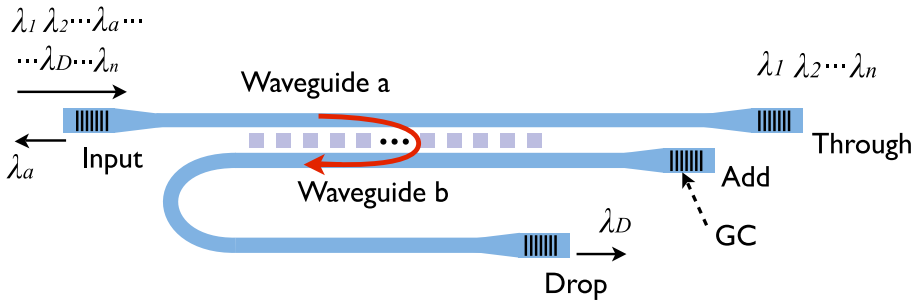


Figure 2.15: Diagram of an optical add-drop multiplexer based on a contra-directional grating-assisted coupler. Ref. [55]

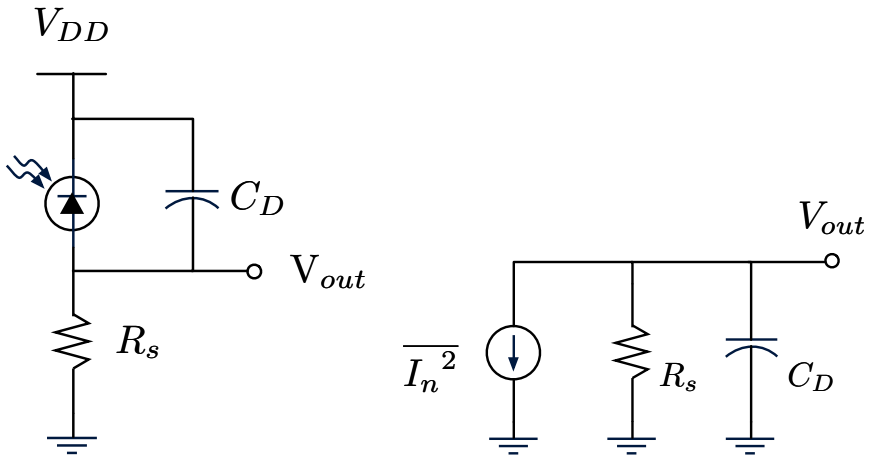
fibre, typically there is a an on-chip Germanium (Ge) photodetector with low parasitic capacitance.

Photodetector is a critical component of monolithically integrated silicon photonics, which is used to convert an optical signal to an electrical signal. One bottleneck that emerges during the design of silicon-photonics-based data links is the constraint on link power budget, and a photodetector with high responsivity could compensate for some of the channel insertion loss, and help satisfy the required link power budget. However, silicon is not an effecient light absorber at standard telecommunication wavelengths (1310 nm and 1550 nm). A number of techniques have been developed to build photodetectors on silicon including epitaxial germanium growth [65], III-V bonding [66], plasmonic absorption [67] and sub-bandgap silicon detection [68].

A few design criteria that a CMOS designer should consider while designing the amplifier, which is used to amplify the current of this photodetector, are: 1) parasitic capacitance of the photodetector that has a significant effect on the speed of the optical receiver, less parasitic means potentially higher speed performance 2) noise performance of the photodetector, since the current noise is amplified with the signal, has direct effect on (S/N) performance of the receiver and consequently Bit Error Rate 3) high responsitivity (η) of a photodetector needs a mechanism to protect the amplifier, which is used to convert current to voltage, from being overdriven [69].

Ge Detectors

The epitaxially-grown germanium optical detector has emerged as the most practical detector technology due to its CMOS compatibility, relatively high



(a) (b)

Figure 2.16: A simple structure of a TIA (a) Schematic, (b) Small signal model for noise calculation [69]

responsivity, low size requirements and high speed [6]. For our application, we use a germanium detector fabricated via a multi-project wafer (MPW) run offered by CMC Microsystem, fabricated at IME. The device has a responsivity of 1.14 A/W at −4 V reverse bias, at 1550 nm wavelength. Dark current is less than 1 µA under both bias conditions. 40 Gbps, with an open eye diagrams, has been demonstrated [70].

2.5.4 TransimpedanceAmplifier (TIA)

In a photonic system, light incurs loss in its transmission through either a fibre or a silicon waveguide; therefore the extracted electrical signal from photodiode, which is in the form of electrical current, incurs loss too. To be able to process this extracted electrical signal, the electrical current needs to be amplified and also converted to electrical voltage. Transimpedance Amplifier (TIA), as its name suggests, coenverts electrical current to voltage. Design criteria for a TIA includes parameters, such as noise, bandwidth, gain, linearity, supply voltage and power dissipation. A simple structure for a TIA is show in Fig. 2.16 to demonstrate the trade-offs between different design criteria [69]. Assuming that bandwidth of $R_b = (2\pi R_L C_D)^{-1}$ is enough to support bit rate equal to R_b, then total input-referred current

noise, can be derived as in (2.1).

$$\overline{I_{n,in}^2} = \frac{kT}{R_L^2 \cdot C_D} = 4\pi^2 \cdot k \cdot T \cdot C_D \cdot R_b^2 \tag{2.1}$$

As it can be seen from (2.1) designing for a higher data rate infers more input-referred current noise. Therefore, this topology is not suitable for high performance applications.

2.5.5 TIA Topoliges

Common Gate Open-Loop TIA

Common Gate (CG) topology of a TIA is shown in Fig. 2.17. The challenges for this topology can be explained as follow:

- The current noise of the transistor M_2 and the resistor R_D are added directly to the input-referred current noise of this topology.
- Assuming that $g_m \cdot r_{o2}^2 \gg \gamma \cdot R_D$, the contribution of M_1's current noise is negligible.
- Reduction in the input-referred current noise needs reduction in the current noise contribution from either M_2 or R_D. Based on 2.1 and a fixed bias current, the contribution of M_2 will be reduced by decreasing g_{m2} which means increasing overdrive voltage of M_2, $V_{GS_2} - V_{th}$. Similarly to reduce the contribution of R_D to input-referred current noise, the value of R_D needs to be increased.
- $V_{DD} \geq V_{RD} + V_{M_1} + V_{M_2}$

The above limitations leads to the conclusion that this topology is not suitable for a low-noise TIA particularly in low-voltage technologies.

$$\overline{I_{n,in}^2} = \overline{I_{n,M_2}^2} + \overline{I_{n,R_D}^2} = 4kT(\gamma g_{m2} + \frac{1}{R_D}) \tag{2.2}$$

2.5.6 Feedback TIAs

The general topology and a particular implementation for a feedback TIA is shown in Fig. 2.18. The benefits of this structure compared to a simple resistor can be mentioned as follow:

- using shunt feedback reduces the input impedance and therefore will increase the bandwidth of operation for this type of TIA.

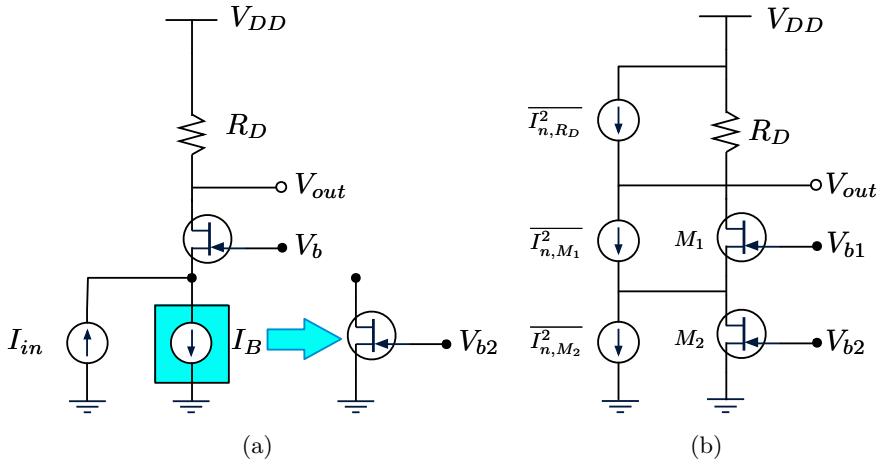
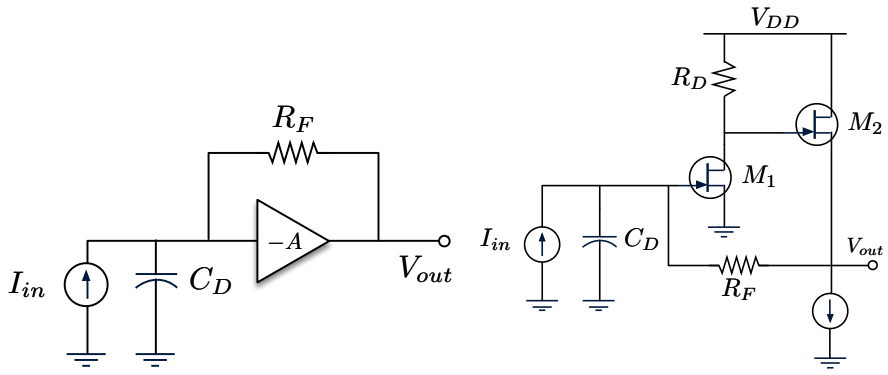


Figure 2.17: Common gate topology for a TIA(a) Schematic, (b) Small signal model for noise calculation [69]

- Although the current noise generated by R_F contributes directly to the input-referred current noise, its contribution can be decreased without any trade-off for voltage headroom (V_{DD}), i.e., by increasing the value of R_F, its contribution will decrease and a bigger supply voltage is not needed. (refer to (2.1)).
- For a given supply voltage, $V_{DD} = V_{RD} + V_{GS_1} + V_{GS_2}$, there is a constraint on how far open loop gain, $g_m \cdot R_D$, can be increased by means of increasing R_D.
- It should be mentioned that the feedback can also be used over a multi-stage amplifier [71].

The above sections talked about the fundamentals of a TIA and also explained about the different trade-offs in a TIA design. There are different techniques to improve the performance of a TIA such as inductive peaking, Automatic Gain Control (AGC) [72], gain boosting and using capacitive coupling to alleviate the voltage headroom constraint in case there is a need for a source follower, acting a buffer, at the last stage of the TIA.



(a) (b)

Figure 2.18: A feedback TIA (a) Overall topology, (b) A particular implementation [69]

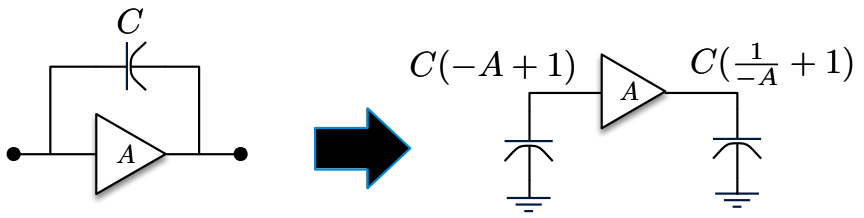


Figure 2.19: Miller effect and inductive behaviour of a capacitance [73]

2.5.7 Bandwidth Extension Using Capacitance in a 12.5 Gbps TIA in 130 nm CMOS Process

Because inductors will consume a lot of space on chip, designer has come up with different ideas to substitute them with other elements. Exploiting Miller effect a capacitance can show an inductive behaviour [73] as it is shown in Fig. 2.19; this technique can be used to cancel the effect of transistors' capacitances and increase the bandwidth of a TIA as is shown in Fig. 2.20. Performance parameters of the TIA in Fig.2.20 is shown in Table 2.2. Cancellation of parasitic capacitance of transistors using the above mentioned Miller effect should be used cautiously because using big capacitance and having a relatively large peak in the frequency response of the TIA will deteriorate the group delay variations and will have a negative effect on the waveform of the received signal in the time domain.

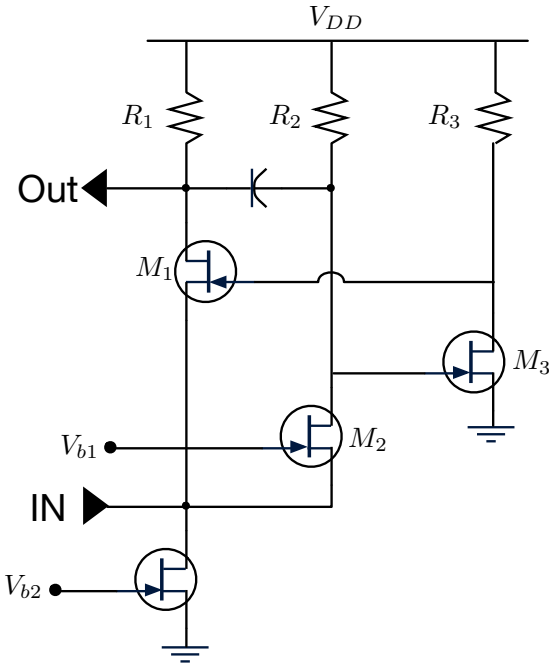


Figure 2.20: 12.5 Gbps TIA using Miller effect to increase its operational bandwidth [73]

Table 2.2: Performance Parameters of the TIA shown in Fig.2.20

Performance Summary	
Gain	53 dBΩ
Bandwidth	14.3 GHz
Input-referred noise	30 pA/$\sqrt{Hz}$
Input cap	400 fF
Power	2.7 mW

2.5.8 Low Noise Amplifier (LNA)

The available large unlicensed bandwidth around 60 GHz has led to significant increase in demand for low-cost mm-wave CMOS receivers [74–76]. A low-noise amplifier (LNA) is the first and most critical block of a receiver which provides signal amplification with minimum additive noise and distortion. Stability, gain, noise figure, and linearity are the important design parameters for LNAs.

Stability of the amplifier can be a big issue specially at high operating frequencies. At these frequencies even the smallest parasitic capacitors can provide undesired signal paths between the input and output ports of the LNA. Any reverse signal path may potentially cause the amplifier to oscillate and cause instability. To prevent this, the amplifier must have a good reverse isolation. Unilateralization is a common technique that is used for this purpose [74].

The LNA must provide a relatively constant gain across the frequency band of operation. When the input signal is weak, the LNA provides a high gain while the gain must be reduced for stronger signals to prevent saturation. Therefore, a gain control mechanism is often needs to be implemented [76, 77].

The noise performance of the LNA is usually expressed in terms of noise figure (NF). It is desired to maximize the signal to noise ratio by minimizing the NF. The noise performance of the LNA is directly related to the choice of the architecture. For example, a common-source amplifier has a fewer number of transistors and consequently fewer noise sources than a cascode and therefore exhibits better noise performance [76].

The LNA must be sufficiently linear in order to suppress interference and maintain a good sensitivity. The linearity of the amplifier is often expressed in terms of third-order input intercept point (IIP3). By definition, IIP3 is the input power level at which the power of the desired tone and the third-order intermodulation product intersect. Several linearization techniques

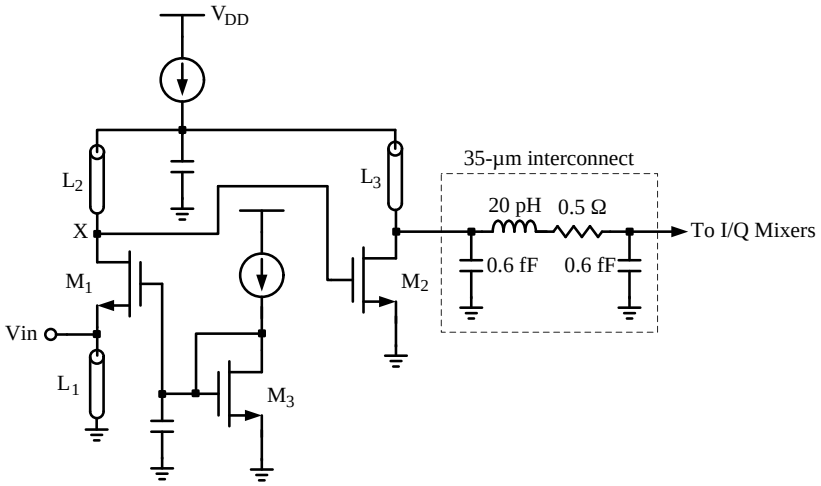


Figure 2.21: Circuit schematic of a 60 GHz LNA. The circuit is taken from [81]

exist in the literature in order to improve the linearity of the LNAs [78–80]. Common-gate (CG) LNAs generally provide better linearity than common-source LNAs. Transconductance (g_m) and output conductance (g_{ds}) nonlinearities are two important distortion sources for LNAs. Preserving linearity of the LNA has become more challenging with the scale of CMOS technology. Shorter channel length makes the g_{ds} of the transistors more nonlinear. Furthermore, reduction of supply voltage has reduced the available voltage headroom for transistors. Therefore, the devices are biased closer to the triode-saturation boundary which further worsens the g_{ds} nonlinearity.

Fig. 2.21 shows the circuit schematic of a 60 GHz LNA taken from [81]. The design is carried out in a 0.13 μm CMOS process. A CG topology is chosen for the implementation of the LNA. The circuit draws 4 mA from the supply voltage [81]. L_1 resonates with the parasitic capacitances of the LNA and the pad. The resonance cancels the capacitances seen at the source node of M_1. Without resonance, the parasitic capacitances degrade the input matching and NF of the LNA [81]. Similarly, L_2 resonates with the capacitances seen at node X. Transistor M_2 increases the overall gain of the LNA and also is used to drive the mixers. The signal from the LNA output needs to travel 35 μm to reach the mixers due to layout constraints. The interconnect is modeled by a network which consists of an inductor, a resistor and two capacitors. The inductive source degeneration configuration is another attractive solution to implement 60GHz LNA in

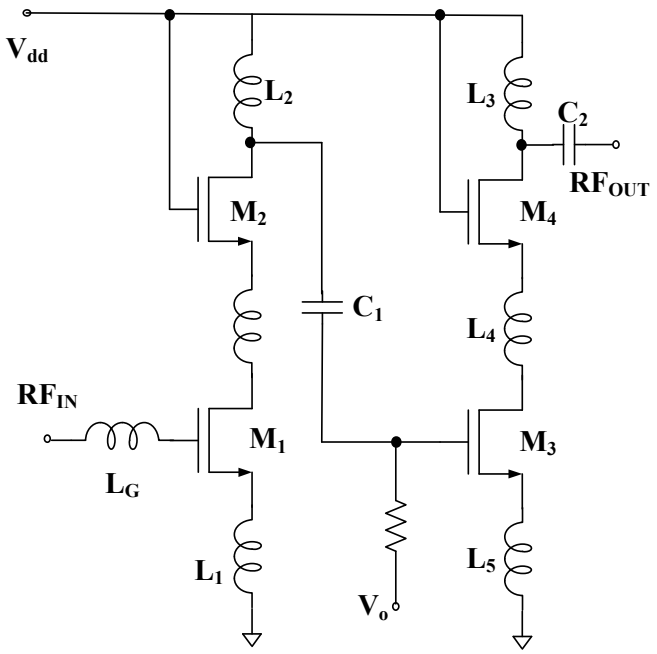


Figure 2.22: Schematics of a cascode architecture [84]

CMOS technology. This topology provides simultaneous noise and input matching at the input port even when employed for wideband applications [82, 83]. The schematics of cascode architecture proposed in [84] is illustrated in Fig. 2.22. Cascode architecture exhibits better isolation between the input and output ports while featuring similar input linearity and simultaneous noise and input impedance when compared to the common-gate (CG) or common-source (CS) topologies. In this work, two cascode stages are used to boost the gain at 60 GHz. The role of series inductors (LM1, LM2) between the cascode devices in each stage is to nullify the impact of parasitic capacitance at middle node and increase the bandwidth [85, 86]. This LNA achieves a maximum gain of 14.6dB at 58GHz and isolation of better than 32dB. The 1dB compression point measurement exhibits a value of -0.5dBm and an IIP3 of 6.8dBm at 58GHz. The LNA noise figure was measured at lower rates and the extrapolated value at 60GHz is between 2.8dB and 3.6dB.

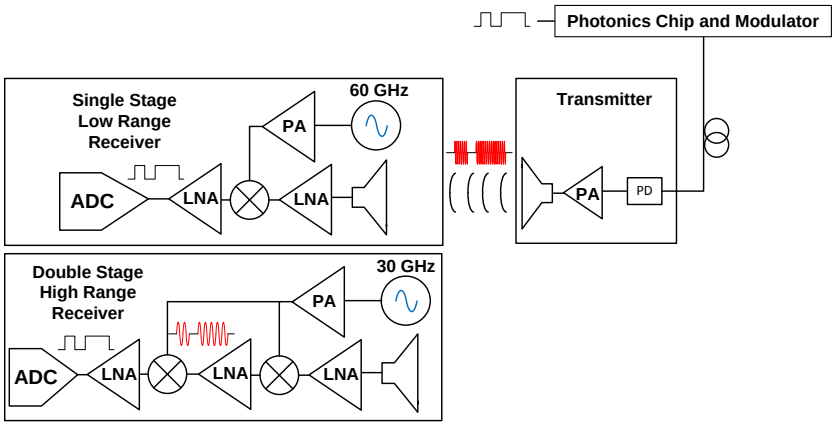


Figure 2.23: Overall diagram of a receiver chain

2.5.9 Mixer

As shown in Fig. 2.23, down converter mixer plays important role in receiver chain of a radio over fibre link. After modulating the input signal using the photonic parts, the unconverted 60 GHz modulated signal is transmitted using a high gain power amplifier. In the receiver chain, after getting and amplifying the weak received signal using LNA, it should be down converted and be passed to ADC for further base band process. Generally mixer acts as a switch where the switching frequency is equal to the carrier (e.g. in this case it is 60 GHz). Generally as the switching frequency increases, performance of the mixer degrades significantly and implementation of mixer chain becomes challenging. As shown in Fig. 2.23, to relax the switching frequency, down conversion can be done in two stages using a half clock rate. This will significantly improves conversion gain and NF performance of mixer, in addition, it improves sensitivity of the receiver which in turn is an effective solution for high range transmission. For the mixer architecture, different active structures can be used such as Gilbert-type mixers [87, 88] or switched-transconductance method [89, 90]. Here we briefly discuss a general problem of mm-wave mixers as well as a general solution which is application in any type of mixers. Fig. 2.24 presents a generic down conversion mixer, known as Gilbert current commutating mixer. First the input 60 GHz signal which is in voltage mode, should be converted to current using M1 transistor and then generated 60 GHz current at the drain of M1 should be switched and down converted between two branches using M2 and M3 transistors [91]. Although switching can be done efficiently

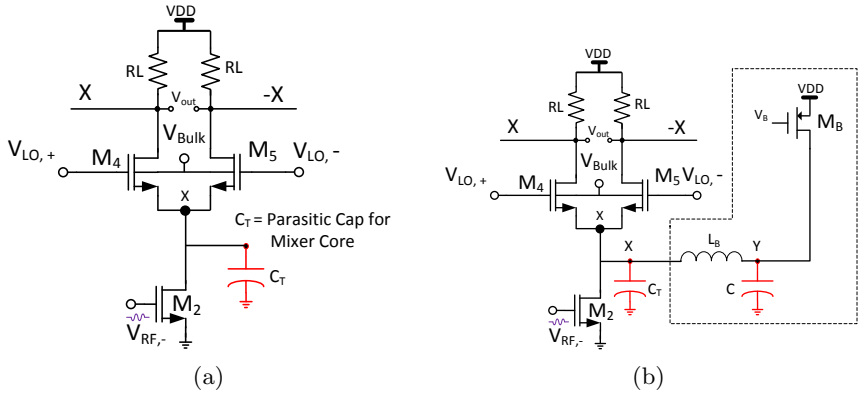


Figure 2.24: Mixer structure (a) Conventional Mixer, (b) High gain and lowe noise figure for mm-wave application

at low frequencies, in mm-wave frequency range it becomes a challenging task. To briefly understand this challenge, consider the parasitic cap at the drain of M1 transistor, CT, which includes total parasitic capacitance of node X. As frequency increases, CT shows smaller impedance and part of 60GHz current splits between CT and switching stage and thus NF and conversion gain of mixer degrades significantly. For example, as discussed in [6], conventional Gilbert-mixer cannot provide enough gain and proper NF at 60 GHz range. As a general solution, it is desired to properly cancel out parasitic capacitances. For example as shown in Fig. 2.24a , by using LB inductor which is ac-grounded with a large capacitor(CBIAS), the parasitic capacitance CT can be managed to cancel out and have parallel resonance with LB . Although this technique is in cost of area, performance of mixer improves significantly and in comparison to the conventional mixer it can improve NF by 13.5 dB and conversion gain by 28dB [81].

2.5.10 Voltage Controlled Oscillator (VCO)

The on-chip synthesis of high quality oscillatory signal is one of the major challenges in the design of communication systems operating at 60 GHz and beyond. The proper design of high frequency oscillators mandates a delicate balance among several requirements such as the phase noise, frequency tuning range, power consumption and silicon area. Traditionally, The integration of high-performance mm-wave Local-Oscillators (LOs) into the low-cost digital CMOS technologies had to overcome the bottleneck of the low value of ft for CMOS process (compared to BiCMOS, SiGe, or

GaAs counterparts). However, advanced CMOS process (with ft of 200+ GHz) and alternative design techniques have lately emerged to tackle the historical shortcomings [92–94].

To better demonstrate the design techniques for 60 GHz signal synthesis, it is worthwhile to review the LO design from a system-level perspective. Fig. 2.25 demonstrate the block diagram of a phase-locked loops (PLLs) which has predominantly been employed to generate the on-chip oscillatory signal [95, 96].

The negative feedback in the loop guarantees that the frequency of the feedback clock generated by the local oscillator (LO), $f_{LO,FB}$ follows the expression $f_{LO,FB} = N \cdot f_{ref}$, where N is the divide ratio of the feedback divider block and fref is the frequency of the reference clock (typically, a low-noise crystal oscillator). The PLL operation satisfies this relationship by constantly monitoring the phase difference between the reference clock and the output of the feedback divider and correcting any deviations between the two ($\Delta\phi$). The combination of the phase-frequency detector (PFD) and the charge-pump (CP) inject current signals with pulse width proportional to $\Delta\phi$ into the loop filter [97]. This current alters the output voltage of the low-pass filter which, in turn, adjusts the frequency of a Voltage-Controlled Oscillator (VCO), the source of both $f_{LO,FB}$ and $f_{LO,OUT}$. Traditionally, the output of VCO would directly produce both $f_{LO,FB}$ and$f_{LO,FB}$ hence $f_{LO,FB} = f_{LO,FB}$. The generic LC-VCO shown in Fig. 2.25 (inset) is a simplified model of cross-coupled LC-VCO [98] widely used for this type of synthesis known as direct or fundamental LO synthesis.

Direct LO Synthesis Techniques

In [99], a variation of cross-coupled pair structure, with only NMOS cross-coupled pair and a PMOS current source is used to achieve oscillation at 60 GHz. The use of PMOS at the center-tap of the inductor allows to bias V_{drain} node (as depicted in Fig. 2.26) at approximately half the supply value, i.e. $V_{dd}/2$. Therefore, as the control voltage of VCO, V_{tune}, varies from 0 to V_{dd} the entire C-V tuning curve of varactor is swept and a large tuning range is achieved, a challenging requirement for mm-wave design. This work has paid a particular attention to the design, and layout of varactor and its impact on the overall tank quality. This is an important issue given the continuous drop in the quality factor of varactors, as frequency increases to 60 GHz and above. The fabricated VCO achieves a tuning range of 5.8 GHz at 59 GHz with a phase noise of -89 dBc/Hz at 1 MHz offset. The current drawn from a 1.5 V supply is 16.5 mA.

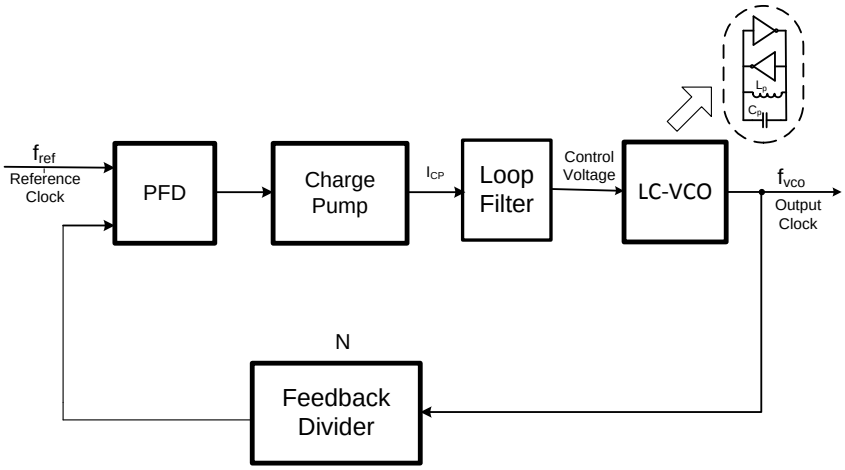


Figure 2.25: Block diagram of a phased-locked loop [95, 96]

In another recent work the VCO tuning is realized using the intrinsic capacitance of the core transistors to avoid the use of low quality varactors [100]. This work takes advantage of the voltage-dependent junction capacitors of a MOS device as an alternative for tank varactors. A triple-well NMOS device possess several junction capacitances which can be modulated by an external voltage to serve the purpose. In particular, the application of a voltage to the bulk node of this configuration allows one to change the drain-bulk capacitance. In this work it has been shown that, the depletion capacitance of the structure may vary from 8.9 fF to 12.1 fF which is equivalent to an overall capacitance change of 10% for the tank. Employing a low-loss spiral inductor ($QL \approx 20$), this VCO oscillates at a centre frequency of 69.8 GHz. The measured tuning range of 4.5% (66.7 GHz to 69.8 GHz) is reported for this VCO.

In [101] an inductive divider, as shown in Fig. 2.27, is implemented to facilitate a capacitance-splitting and a gatedrain impedance-balancing techniques. This technique ameliorates the drop of transistor gm at high frequencies hence lowering the required size of active devices for proper startup, hence the power consumption. Also, the resulting balance between the transistor terminal resistive impedances improves the loaded quality factor and the noise factor is reduced. The implemented VCO achieves a tuning range of 8.3%, with an output power of 6 dBm, and a phase noise of 124.5 dBc/Hz at 10-MHz offset.

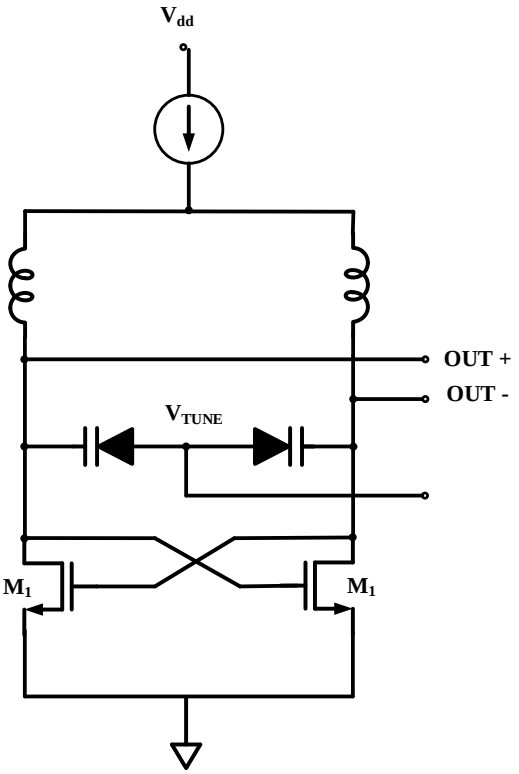


Figure 2.26: Simplified model of a cross-coupled LC-VCO [98]

Indirect LO synthesis techniques

Despite the inherent simplicity, direct LO synthesis techniques, as observed in previous section design examples, suffer from several shortcomings which limit their performance at mm-wave frequencies. In particular, the gm of devices drops as the frequency of operation f0 approaches the maximum oscillation frequency (f_{max}) of the transistors. Therefore, larger devices in the cross-coupled pairs are required to compensate the tank loss, which come at the cost of excess power consumption and noise of the VCO. The quality factor (Q) degradation of passive devices (varactors and inductors) at 60 GHz is also a known effect that deteriorates the phase noise performance of LO. Also, the required tank capacitance to resonate with the integrated coil, i.e., the tank inductance, is relatively small at 60 GHz band. Therefore, the voltage-dependant capacitance of the oscillator core devices, wires, and the drivers connected to tank output severely limit the amount of varactor

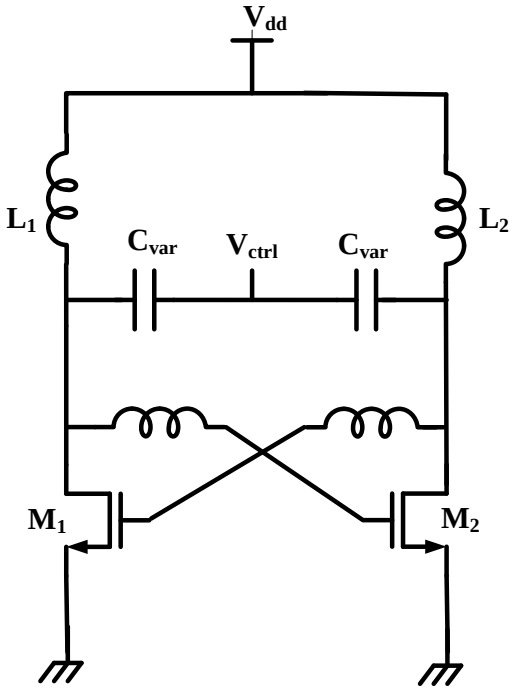


Figure 2.27: Inductive divider implementation is used to facilitate a capacitance-splitting and a gatedrain impedance-balancing [101]

capacitance and the achievable frequency tuning range. Furthermore, the use of switched-capacitor coarse tuning to reduce KVCO and improve the phase noise, is nearly impractical due to loss and parasitic capacitance of the switches.

To alleviate the above-mentioned issues, alternative approaches, generally regarded as Indirect LO synthesis techniques have gained popularity over the recent years. Fig. 2.28(a) depicts the PLL block diagram for indirect synthesis using several variants (Fig. 2.28(b)-(d)). Fig. 2.28(b) illustrate higher-order harmonics generation as one of variant of indirect synthesis techniques. In this technique, an N-push VCO is used in the LO block of PLL (instead of a fundamental-mode VCO in the PLL) to improve the frequency tuning range [102]. Therefore, for f_{LO},out of 60 GHz, VCO core only needs to operate at 30 GHz for a push-push architecture and at 20 GHz for a triple-push design. One immediate advantage of this architecture is that the first-stage of feedback divider only requires to function up to the fundamental frequency of the VCO and not at its N-push output which

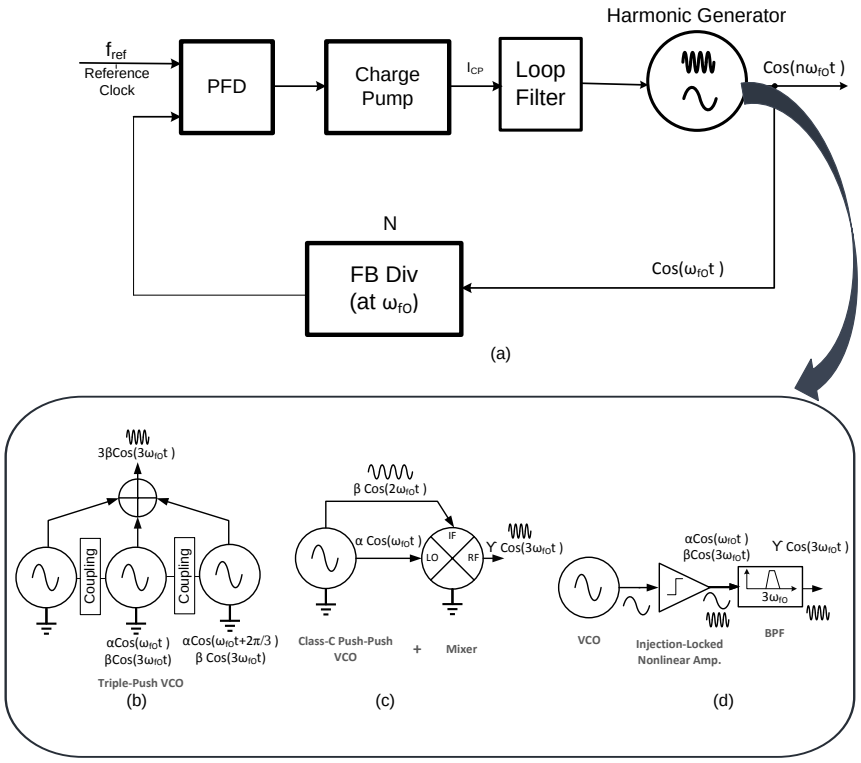


Figure 2.28: Several proposed indirect LO synthesis

greatly reduces the power dissipation of the divider chain. Another advantage is that the core of VCO operates at a much lower frequency where the transistors have larger gain and the varactors constitute a larger portion of total tank capacitance. However, N-push VCOs suffer from low output power because their output power relies on the nonlinearity of the devices, particularly transistors and varactors. Therefore, proper buffering of LO output and other design techniques to improve the output power of multi-giga-hertz N-push VCOs play an important role in adopting these technique into mm-range synthesiser design [103].

In [104] a source degeneration technique (as shown in Fig. 2.29(b)) is proposed that allows the extraction of the 2nd harmonic content of the fundamental oscillation. It is analytically shown that the squaring function of M1-M2 pair provides a frequency doubling effect. This effect, in turn, generates two in-phase 2^{nd} harmonic signals at the source node of the differential pair which is then extracted at the common-mode connection of the two de-

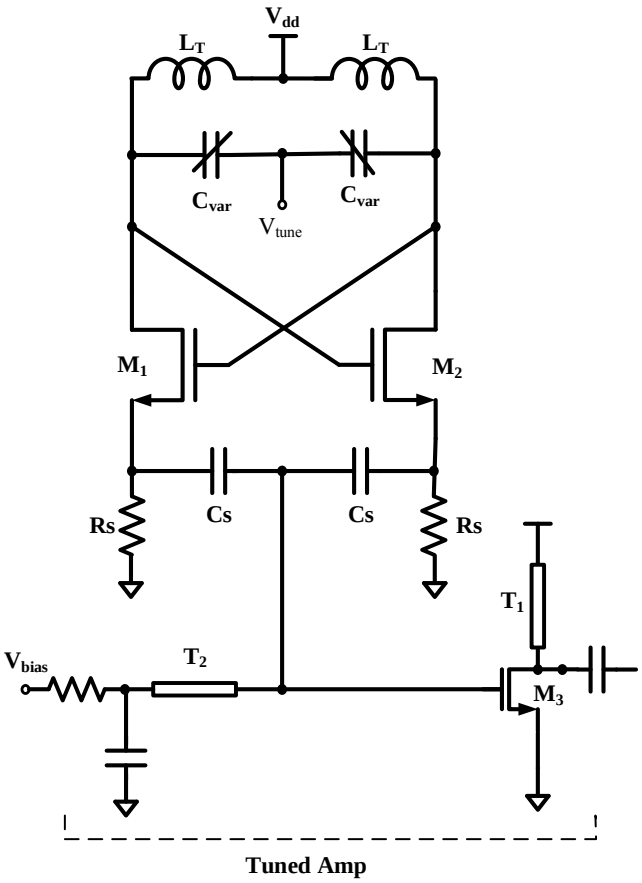


Figure 2.29: Proposed technique to extract the 2^{nd} harmonic [104]

generation capacitors, CS, and is amplified through the use of a single-ended tuned amplifier. Therefore, to generate 60 GHz output signal, the LC tank circuit is required to operate only up to 30 GHz resulting in an improved quality factor. The VCO consumes 30 mW (including the VCO core and the following amplifier at $2f_o$) from a 1.2 V supply and the measured phase noise at 1 MHz offset is -89 dBc/Hz. In [105], a triple push VCO design in 130-nm CMOS technologies achieves a frequency tuning range of 13.6% at centre frequency of 67 GHz while consuming 18 mW from a 1.4 V supply.

Fig. 2.28(c), depicts another variation of harmonics generation which employs self-mixing of two harmonics of VCO to generate the high frequency $f_{LO,out}4$ [106]. This technique exhibits similar benefits as N-push design

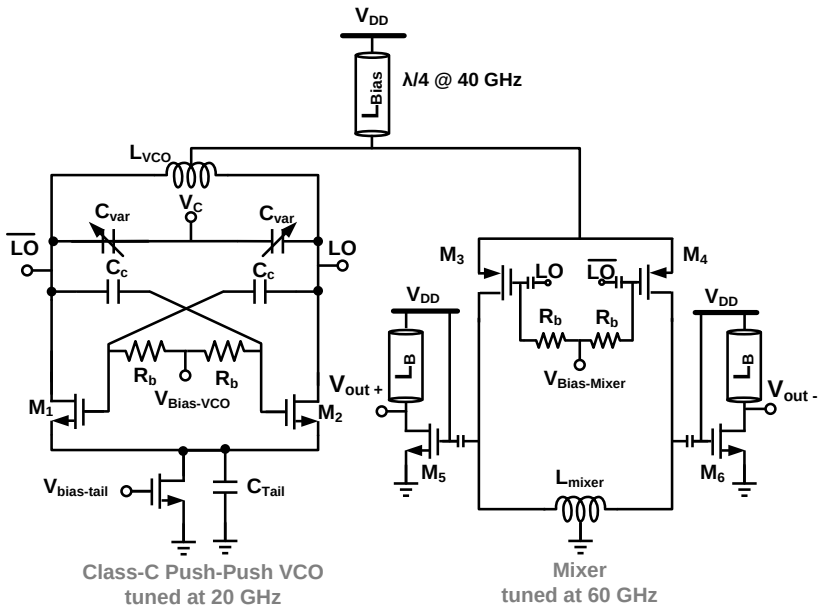


Figure 2.30: Class-C self-mixing VCO is used to achieve a wide tuning range [107]

mentioned above (the mixing of two harmonics allows generating even larger output frequency from a fundamental signal). One drawback of this architecture is the existence of large harmonic contents at the output of VCO due to the parasitic capacitance as well as mixer feed through. In [107], as shown in Fig. 2.30, a class-C self-mixing VCO is employed to achieve a wide tuning range of 10 GHz at 60 GHz band while burning only 7.6 mW from a 1.2 V supply. The reported phase noise is -100.5 dBc/Hz at 1 MHz offset for a 53 GHz output signal. Another variant of indirect synthesis is illustrated in Fig. 2.28(d) where a low-frequency PLL and an a subsequent frequency multiplier generate the mm-wave output [108]. This frequency multiplier can be implemented as either oscillating or non-oscillating architecture. An injection-locked oscillator, at the output of low-frequency PLL is an attractive realization of the former [109, 110]. However, process, voltage and temperature variations typically put stringent requirements on the pulling and locking range of these oscillators. The use of a harmonic generator may well serve as an implementation of the latter[111]. However, the gain of these multiplier drastically drops with increasing multiplication ratio and mandates use of high power low-frequency VCO to generate ac-

ceptable output powers. In addition, the strong fundamental tone of the VCO can leak through the multiplier and affect the system performance so the unwanted tones should be properly filtered out. On the other hand, one considerable advantage of this architecture.

2.6 On the Capacity of a 60 GHz Wireless Communication

The United States Federal Communication Commission (FCC) assigned 7 GHz of continuous spectrum that can be used for transferring high definition media ($2-3$ Gbit/s) even using simple modulation such as PAM and PSK. Due to higher path loss in 60 GHz, higher transmit power, 10W, is permitted. There are several challenges in the design and implementation of a 60 GHz communication link [112–114]. These challenges are twofold. One category is related to wave propagation challenges and the other one is related to circuit design challenges in this frequency band. Wave propagation challenges come from the facts that 60 GHz channel has the free path loss of 20 to 40 dB that is significantly higher compared to low frequency bands, atmospheric absorption contribute 15 to 30 dB/km depending on the condition and fading effect, related to non-line-of-sight (NLOS) communication, is more significant. On the other side circuit design in 60 GHz is challenging because of lower gain in this frequency band, need for millimeter-wave modelling of transmission lines due to distributed nature of circuitry in this frequency band, higher phase noise and etc. [112–115]

2.7 Simple Modelling of a 60GHz Communication Link

In the simplest form, Friis equation models the communication between two antennas; based on Friis equation the received power at the received antenna can be calculated as in (2.3).

$$P_r = P_t + G_t + G_r + 20 \cdot log_{10}\left(\frac{\lambda}{4\pi R}\right) \tag{2.3}$$

G_t and G_r are the antenna gains of the transmitting and receiving antennas; λ is the wavelength of the transmitted signal; and R is the distance between transmitting and receiving antennas. Empirical adjustment is needed to make the Friis equation more suitable for situations where there is not a

clear line of sight communication and strong multi-path effects exists; in these situations the Friis equation can be written as in (2.4). In (2.4), n is experimentally determined and is approximately 1.5 for LOS communication and 2.44 for NLOS [116].

$$P_r = P_t + G_t + G_r + 10 \cdot log_{10}\left[\left(\frac{\lambda}{4\pi R}\right)^n\right] \tag{2.4}$$

To calculate the channel capacity for a 60 GHz communication link, Shannon equation (2.5) can be used. Considering the fact that FCC limited the isotropic radiated power of 60 GHz transmission band, 57 GHz to 64 GHz, to a maximum power density of $9\mu W/cm^2$ at 3 meter from the radiating source [117].

$$\text{Link Capacity} = W \cdot log\,(1 + \text{SNR}) \tag{2.5}$$

Assuming that the main source of noise is thermal noise, the required sensitivity of the receiver can be calculated as in (2.6). Sensitivity in a receiver is normally taken as the minimum input signal required to produce a specified output signal having a specified signal-to-noise (S/N) ratio. Term $k \cdot T_0 \cdot B$ in (2.6) is the noise floor and it can be calculated as -76 dBm for a 60 GHz communication link.

$$(S_r)_{min} = (\frac{S}{N})_{min} \cdot k \cdot T_0 \cdot B \cdot NF \tag{2.6}$$

$$NF = Noise\ Factor \tag{2.7}$$

Using all the above equations, it can be shown that channel capacity falls rapidly with distance especially in NLOS channel where ideal communication distance is less than 20m for NLOS communication channel. In LOS channels, Contrary to NLOS, this capacity loss is not as sharp as NLOS. For example the normalized channel capacity falls from 16 to 6 (bit/s/Hz) while distance from the transmitter to the receiver is increasing from 1 meter to 45 in LOS channels (NLOS channel capacity falls sharply from 16 to 1.6 (bit/s/Hz) in similar situation) [118, 119]. Summary of the above calculation is shown in Table 2.3. An advantage of using digital baseband approach, as mentioned in Section 2.1, is its digital nature compared to RoF, which is analogue in nature. Being digital in nature, the noise properties of the optical link do not enter into the 60 GHz RF Link. In the RoF approach, the RF link gain of the optical link is critical and any RoF impairments have a direct impact on the channel capacity; in contrast, in the digital approach, ensuring a zero bit error rate is the necessary condition, as is typical in digital optical fibre links.

Table 2.3: Comparison Between Channel Capacity for LOS and NLOS 60 GHz Wireless Communication[119]

Communication Type (Distance = 45 meters)	**LOS**	**NLOS**
Normalized Channel Capacity(bit/s/Hz)	6	1.6
Approximate Channel Capacity (Gbit/s)	42	11

2.8 Photonic Integrated Circuit Design Challenges

As discussed in the previous sections, a typical photonic integrated circuit consists of photonic, electronic, and electro-optical devices. Consequently, a photonic-electronic design framework should be able to support electro-optical designs at both schematic and layout levels. Furthermore, the framework should provide electro-optical device models through a well calibrated/modelled process design kit (PDK). Given that electronic design automation (EDA) frameworks are already well established, it is logical to incorporate them in the electronic-photonic design framework.

Although using EDA framework as the foundation of an electronic-photonic design automation (EPDA) framework could benefit the design community by using well-established methodologies, it has its own challenges. These challenges include:

- The layout shape of photonic component are curvilinear. The EPDA should be able to support such shapes not only at the application level but also at the database level.
- The EPDA framework should be able to support optical, electrical, and electro-optical simulations.
- The EDA framework should improve its existing verification methodologies, such as layout versus schematic (LVS) and design rule check (DRC) to include photonics components.
- A well calibrated/modelled PDK that supports both electrical and optical devices should be provided by foundries.
- The framework should be able to support photonic technology computer-aided design (TCAD) tools inherently or through an interface to extract a compact model for a photonic device.

In Chapter 3, we will discuss different methodologies that have been developed to address some of the above challenges and also introduce our proposed method to address them.

Chapter 3

A Novel and Scalable Design Automation Framework for the Simulation of Photonic Integrated Circuits

Silicon photonics is a promising platform for photonic integrated circuits (PICs) because it is compatible with highly mature silicon integrated circuit (IC) fabrication processes. Although there has been significant progress in the modelling and simulation of silicon-photonic systems, none of the existing PIC design flows support a complete and efficient scalable electro-optical ecosystem. Some of the silicon-photonic electro-optical design flows are discussed in[120–127]. These design flows can be categorized into two groups: those based on Verilog-A modelling and those based on data exchange. Some of the challenges of the photonic design automation (PDA) with regards to the layout of a photonic circuit are discussed in [128].

In the first category, Verilog-A is used to describe the analog behaviour of photonic components. This technique has been discussed both in research [126, 127] and in the commercial tools [129, 130]. Verilog-A modelling in this type of design flow, as shown in [127], is based on a signal-flow system description. These signal-flow techniques suffer fundamentally from some restrictions with regards to their modelling (refer to the Verilog-A reference manual): (1) typically, it is not possible to directly interface signal-flow and conservative components, (2) because the signals are potential-like, it is difficult to represent float-like signals, and (3) component descriptions can only be written in terms of ground-reference signals, which makes it challenging to have behavioural modelling using floating or differential signals. In addition, most examples in the Verilog-A modelling category are based on a single-mode optical signal. This could be explained by observing that: (1) increasing the number of channels and modes increases the number of Verilog-A module's terminals significantly, and (2) including higher order

propagating modes in Verilog-A requires conservative modelling including both potential-like and flow-like signals causing significant modelling challenges and convergence issues [131]. For example, a waveguide modelled using Verilog-A and supporting one propagating mode has 4 ports for its optical input and 4 ports for its optical output [127]; consequently, modelling a multi-mode interferometer (MMI) having 4 optical connections, and only considering 4 optical modes, requires 64 ports (4 ports per mode per optical connection $\times$ 4 modes $\times$ 4 optical connections). This not only puts constraints on the routing in the schematic in large systems but also creates challenges when routing these pins in the layout view and performing layout versus schematic (LVS) tests. Another issue that is of great concern in the industry is the intellectual property (IP) of the developed compact models. For example, if a Verilog-A model for a transverse electric (TE) mode of an optical coupler is implemented, encrypted and provided to a designer, the designer can only make modifications, such as including another mode in the coupler, if they have access to the Verilog-A source code, and recompile it. In contrast, the frequency dependence and number of modes for INTERCONNECT compact models can be set by external files, which is scalable and also protects the IP of the compact model. Another challenge of Verilog-A is that the models must be described in the time domain and it is challenging to model a multi-mode photonic component described by frequency-domain S parameters.

The second category of electro-optical design flows is based on exchanging the data between electrical and optical [122, 123] simulators. In [122, 123], an electro-optical design flow is presented that is based on data exchange between INTERCONNECT and Mentor Graphics' Eldo Spice. The most critical challenge of this design methodology is its inability to simulate systems having electro-optical feedback.

The purpose of this chapter and Chapter 4 is to come up with a novel approach and implementation in the form of an integrated development environment (IDE) to resolve the above mentioned challenges. Our implemented approach uses Cadence Spectre communicating with INTERCONNECT through three mechanisms simultaneously as follows:

- Using Open Analog Simulator Interface Socket(OASIS) framework to generate INTERCONNECT compatible netlist
- Generate optical simulation results in Parametric Storage Format (PSF) that could be recognized by Cadence framework
- Use an Interface provided by INTERCONNECT's Dynamic Link Li-

braries, which are wrapper in a Verilog-A module, so Spectre and INTERCONNECT can communicate seamlessly

The Cadence/INTERCONNECT interface for the implemented electro-optical design flow is shown in Fig. 3.1. In the proposed methodology, a

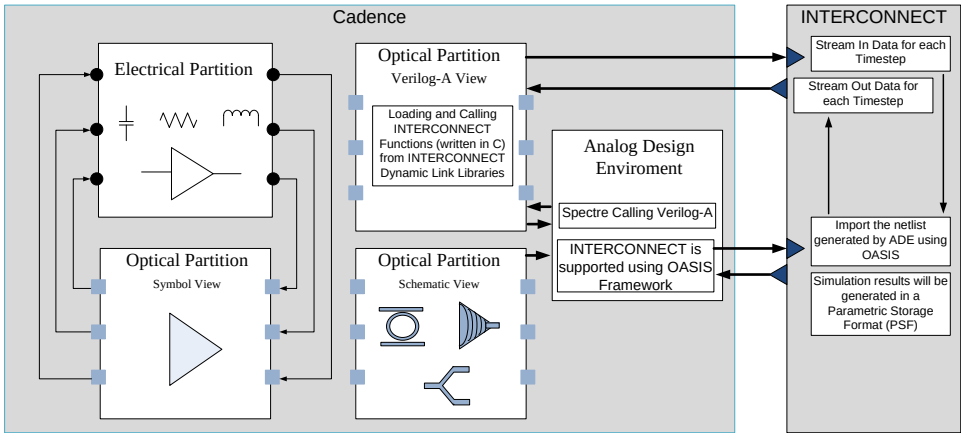


Figure 3.1: Cadence/INTERCONNECT electro-optical interface supporting complete design flow for silicon photonic integrated circuits

PIC is naturally divided into electrical and optical partitions. An optical partition is represented using a subcircuit having only electrical terminals. The electrical signals to an optical subcircuit are conveyed by electrical nets connecting to the electrical nodes of the electrical partition. As can be seen from Fig 3.1, Verilog-A is used as a wrapper to call the interface functions provided by INTERCONNECT dynamic link libraries. Considering that INTERCONNECT is used as the optical solver engine, a natural design flow for time- and frequency-domain simulations of photonic integrated circuits can be implemented because INTERCONNECT can simulate compact models, such as those defined by S parameters, in both the time and frequency domains.

INTERCONNECT as the optical solver engine can resolve most of the restrictions of using Verilog-A as follows: (1) the number of modes can be changed without any revision and recompiling of the code while maintaining IP protection of the underlying compact models, (2) Since Spectre, as the main solver, only needs to consider electrical connections and the optical simulation is performed by a dedicated optical circuit solver, the electro-optical simulation will converge more reliably, (3) because the optical simulation is performed in INTERCONNECT, it does not suffer from restrictions

of signal-flow Verilog-A modelling, and (4) because optical simulation and modelling are performed in INTERCONNECT, there is no restriction on the use of photonic component compact models defined in the frequency domain.

In the proposed methodology the optical schematics developed inside Virtuoso and INTERCONNECT are connected using the OASIS framework. Electrical input and output signals of the optical subcircuit are updated at each electrical time-step set by Spectre. The INTERCONNECT simulation engine sets the optical time-step, which is not necessarily similar to the electrical time-step, and generates optical simulation results using time interpolation if necessary. The generated optical results are fed back to the Cadence framework at each time-step using parametric storage format (PSF) so they can be used for post-processing in Cadence tools such as ViVA. Separating electrical and optical time-steps and updating electrical and optical signals at their relevant time-steps makes our approach a true co-simulation methodology supporting electro-optical designs having electrical feedbacks.

3.1 Electro-Optical Integrated Development Environment Challenges

It was shown, in chapter 2, that modelling of electro-optical components such as a ring modulator is necessary for the design of the relevant electronic circuitry (e.g. CMOS driver). The electrical model proposed for the ring modulator was implemented and shown by electrical components such as resistors, capacitors, and inductors. This modelling type infers that for electro-optical co-simulation the electronic circuitry with its load, which is the electrical model of the ring modulator in this case, needs to be simulated first and the required electrical time-domain signals (for optical simulation) need to be extracted. These time-domain signals are then imported into the optical simulator for optical simulation. Moreover, the results of optical simulation may need to be imported back into the electrical simulator. For example, if there is a photo-detector in the electro-optical schematic and its output drives a Trans-Impedance Amplifier (TIA), then the output of the photo-detector, considering the loading effect of the TIA, needs to be imported into the electrical simulator. This cycle is demonstrated in Fig. 3.2. As can be deducted from Fig. 3.2, there are some challenges that could be enumerated as follows:

- Two schematics need to be drawn: one schematic needs to be drawn in the optical simulator for the optical part, and another schematic

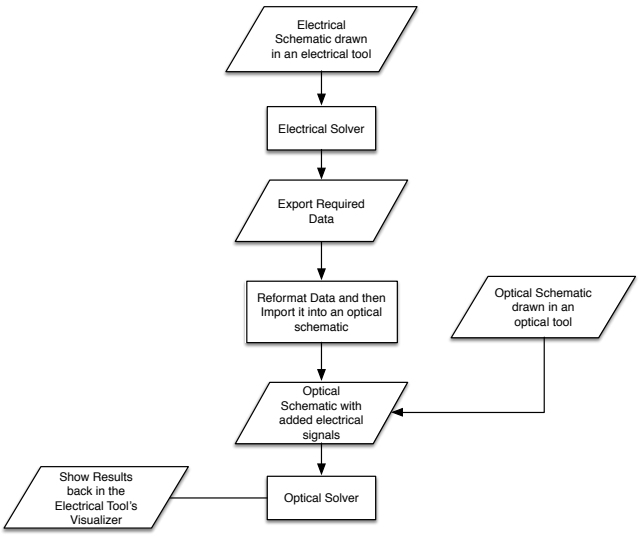


Figure 3.2: The cycle of electro-optical co-simulation using separate electrical and optical tools

needs to be drawn in the electrical simulator for the electrical part.

- The generated results of an electrical simulator are not necessarily compatible with the importing format of the optical simulator and vice versa.

- If an electro-optical design needs to be fabricated in a monolithic electro-optical process (e.g. Luxtera [132]), the layout of optical and electrical components need to be drawn in separate Computer Aided Design (CAD) tools. This means not only does a separate Process Design Kit(PDK) needs to be developed for each of tools but also merging of two separately generated Graphical Database System (GDS) for an electro-optical design needs to be resolved; furthermore, a different Design Rule Check (DRC) needs to be developed for each tool separately, which makes the DRC of an electro-optical design challenging.

. All of the mentioned issues make the design, simulation, and fabrication of electro-optical designs very challenging. An efficient methodology addressing these challenges should provide designers with an integrated design environment (IDE) so that they can design and co-simulate electro-optical systems; consequently, there needs to be a transparent mechanism

to partition electro-optical schematics into electrical and optical partitions and simulate electrical partitions based on an equivalent electrical model of electro-optical components and simulate optical partition by extracting required electrical waveforms from precedent electrical simulation. This IDE should also have the capability of supporting both electrical and optical PDKs. As will be shown, the Cadence suite not only can be used as an IDE but it can also provide the developer with platform/framework to address the above challenges.

Two of the industry leading software packages used for simulating electrical circuits and optical designs are Cadence Spectre and Lumerical INTERCONNECT respectively. INTERCONNECT is a photonic integrated circuit software package that provides designers with design, simulation, and analysis of complex photonic integrated circuits, and Cadence is an electronic software package mainly used for integrated circuit design, simulation (the main simulator of Cadence is Spectre), analysis, and layout.

In both of these simulators, the schematic, which is the graphical representation of the design, needs to be converted to a textual format called netlist showing the connectivity of the components used in the schematic. This generated netlist from Cadence needs to be imported into INTERCONNECT for an optical simulation. The netlist format that INTERCONNECT accepts is not compatible with netlists that are generated by analog simulators such as Spectre and Spice; consequently, a separate netlister, a program that creates the netlist, needs to be developed. This program needs to be developed in Cadence because INTERCONNECT is going to be implemented as an optical solver inside the Cadence design environment. The main programming language inside Cadence for integrating new solvers is SKILL/SKILL++. SKILL is a scripting language based on LISP and is used in many software packages provided by Cadence such as Cadence Virtuoso and Cadence Allegro. SKILL++, which is based on Common Lisp Object System, adds new features to the core of SKILL so it can support object oriented programming features such as class, inheritance, method overloading, and etc. Most of the software developed in this chapter is done using either SKILL or SKILL++ based on features needed at the time of the development. In a few parts of the implemented code, Linux Bash commands have been used to reformat text files by regular expressions.

To provide a modular development environment for new solvers (in this case INTERCONNECT) that need to be integrated into Cadence, a framework called Open Analog Simulator Interface Socket(OASIS) is provided by Cadence. This framework provides an interface to the internal Analog Design Environment (ADE) code, so a developer can benefit from most of

the code already written for analog/mixed-signal simulations. Using OASIS, we can exploit the inheritance feature of SKILL++ to access most of the functionality that has been already developed in ADE such as verification, optimization, and simulation of analog/mixed-signal designs. Fig. 3.3 shows two sub-packages of the Virtuoso design environment, which are used in this chapter, and their relationship to INTERCONNECT. The integra-

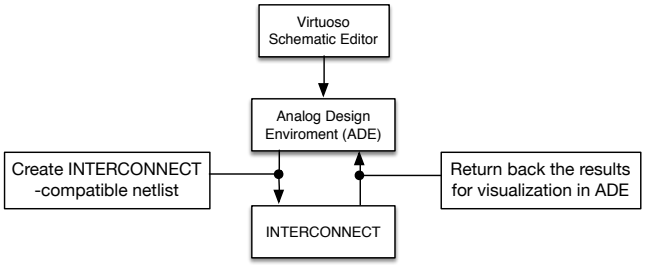


Figure 3.3: Two cadence sub-packages, ADE and VSE, used in conjunction with INTERCONNECT for an electro-optical simulation

tion of INTERCONNECT engine, using OASIS, into Cadence has been done based on the following steps for two classes of analysis in INTERCONNECT: the frequency domain, Optical Network Analysis (ONA); and time domain, Optical Transient Analysis (OTRAN).

- Create a library for electro-optical components, called INTERCONNECTLib, in Cadence
- Initialize INTERCONNECT as a new simulator inside ADE
- Use inheritance functionality of SKILL++ to overload netlister, which is the procedure that generates netlists, to generate netlists whose formats are compatible with the format that INTERCONNECT can import/simulate
- Generate smart simulation forms acting as a Graphical User Interface (GUI) for a designer so that simulation options can be set up in ADE for analysis that are supported in INTERCONNECT
- Use inheritance functionality of SKILL++ to overload the procedure that generates simulation statements and options that are compatible with INTERCONNECT

- Create/Modify configuration files in Cadence Design Framework II (DFII) such as "*.cdsenv*" and "*.cdsinit*" that are used to set up default values of simulator (INTERCONNECT) and load contexts at the launch of Cadence respectively
- Test simulation environment

In the above list, loading context basically means loading code and data that have been already written and packaged. The benefit of using context compared to loading SKILL files directly are faster loading time and code encryption for commercial products.

3.2 Create INTERCONNECTLib in Cadence

Every electro-optical schematic consists of electro-optical components; as a result, before being able to draw a schematic we need a library of components. This library is used as a placeholder to contain information of different component views. Different views basically specify different use of a component. For example, a transistor can have a symbol view that can be used in the schematic editor and can have a layout view that is used in the layout editor. To support both electrical and optical components in INTERCONNECTLib, some of the them only have optical views such as optical waveguides, waveguide bends, and grating couplers and some of them only have electrical views such as resistors, capacitors, and electrical sources. There are components that have both electrical and optical views such as phase shifters, optical modulators, photodetectors, and INTERCONNECT-Export. To be consistent with the simulators' names, the electrical view is called Spectre and the optical view is called INTERCONNECT. Each component also has a symbol view that is used in the Virtuoso schematic editor to represent it. There are two ways to generate these symbols: they can be generated using SKILL language or drawn using basic drawing objects such as lines, arcs, and rectangles in the Cadence symbol editor tool. The basic version of SKILL code that is used in this development to generate grating coupler symbol, is shown in code snippet Code 3.1.

Code 3.1: SKILL code to generate a grating coupler symbol

```
1 procedure(GratingCoupler(GratingHeight GratingSteps)
2        let((x stepsize EllipseBox EllipseArc)
3                cv=geGetEditCellView()
4                x=0
5                stepsize=1.2
```

```
6                 for(x 0 GratingSteps
7                         EllipseBox=list(list(0+stepsize*x -(
                              GratingHeight/2)+x) list(4+stepsize
                              *x  GratingHeight/2-x))
8                         EllipseArc=list(list(2+stepsize*x+1 -(
                              GratingHeight/2)+x) list(4+stepsize
                              *x  GratingHeight/2-x))
9                         dbCreateArc(cv '("device" "drawing")
                              EllipseBox EllipseArc)
10                        )
11                )
12                CornerBox=list(list(2 -(GratingHeight/2))
13                                            list(2*GratingSteps
                                                  GratingHeight/2)
14                                            )
15                dbCreateRect(cv '("device" "drawing") CornerBox
                      )
16 )
```

One of important reasons to use the SKILL language to generate symbols is to be able to use Cadence Parameterized Cell (PCell) functionality to create symbols that could change their shapes based on parameters defined by a designer; for example, a designer can specify the magnification of a symbol and it will change its size automatically or a designer can specify the number of inputs for a logic gate and the symbol will redraw itself to comply with the updated number of inputs.

Each component in INTERCONNECTLib could have parameters assigned to it; these parameters could be specified using either the Graphical User Interface (GUI) provided by Cadence as shown in Fig. 3.4 or the SKILL language as shown in code snippet 3.2. In both cases, Cadence uses Component Description Format (CDF) to describe parameters of new components. In the latter case, the user needs to use "*almBuildLibrary*" procedure, which is provided by Cadence, to associate parameters to components; it should be mentioned that this method (using SKILL) is more time-efficient when many components need to be defined in a library. We used this method to generate most of components inside INTERCONNECTLib library.

Code 3.2: SKILL code to define wg_width parameter and set it as a parameter for Waveguide component in INTERCONNECTLib

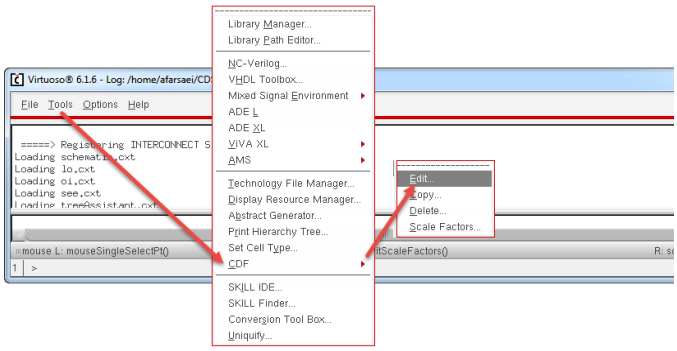
```
1 ;;;;;;The following code snippet is located in params.il file
      ;;;;;;;;;;
2 procedure( almDefineParam_wg_width(_cellName)
3     '( nil
4        name          "wg_width"
5        prompt        "Width of the waveguide"
```

```
        type           "string"
        defValue       ""
        storeDefault   "no"
        parseAsNumber  "yes"
        parseAsCEL     "yes")
)
;;;;;;The following code snippet is located in simInfo.il file
    ;;;;;;;;;;
procedure( almCreateSimInfo_Waveguide_INTERCONNECT()
    '( nil
        otherParameters          ()
        instParameters           ( wg_length )
        termOrder                ( opt_a1 opt_b1 )
        termMapping              ()
        componentName            wg
     )
)
```

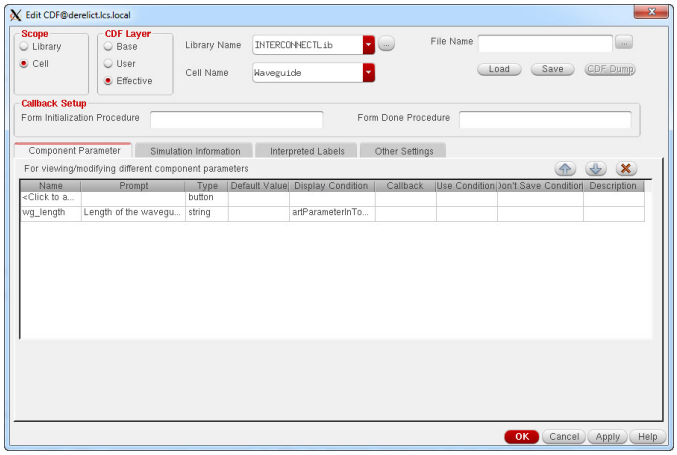
3.3 Initialize INTERCONNECT as a New Simulator

The first step in INTERCONNECT integration, which is called initialization, is to introduce INTERCONNECT as a new simulator to ADE. As has already been mentioned in the previous section, one of the benefits of using OASIS is that we can exploit the code that has already been written and moreover by using the inheritance feature of SKILL++, just add the extra functionalities that we need to the initialization process. The procedure for the initialization process of a simulator is called "*asiInitialize*". This procedure can be overloaded for a new simulator, so that a developer can change its behaviour. The input argument for this procedure should be an object (in our case this object is of type INTERCONNECT). It should be mentioned that since INTERCONNECT class isn't defined in Cadence/ADE, it needs to be defined first. This is done in a separate file "*classes.il*"; this file is going to be the main file that contains the definition of new classes in our development process. The classes that have been defined for our development are listed below.

- INTERCONNECT: This class is used to represent the INTERCONNECT tool and is derived from *asiAnalog*
- INTERCONNECT_session: This class is used to represent the INTERCONNECT simulation session and is derived from *asiAnalog_session*



(a)



(b)

Figure 3.4: Define components' parameters using Graphical User Interface (GUI) in Cadence: Here the parameter used is *wg_length* which is the length of the Waveguide component

- INTERCONNECT_ONA_analysis: This class is used to represent ONA analysis in INTERCONNECT and is derived from *asiAnalog_analysis*
- INTERCONNECT_OTRAN_analysis: This class is used to represent OTRAN analysis in INTERCONNECT and is derived from *asiAnalog_analysis*
- INTERCONNECTFormatter: This class is used to represent the INTERCONNECT formatter object that is used to format the design, which is in the form of a schematic, to netlist and is derived from

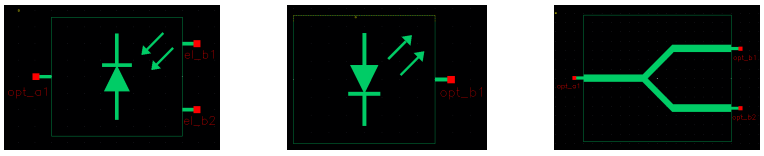
nlAnalogFormatter

The first step in the initialization process is to register INTERCONNECT as a new simulator. This is done by using the "*asiRegisterTool*" procedure. After the registration of INTERCONNECT, the initialization procedures are called; the purpose of this initialization procedures are to initialize environment options, simulation options and analysis options; the procedures for the initialization of these options are: "*asiInitEnvOption*", "*asiInitSimOption,*" and "*asiInitAnalysis*" respectively.

As it has already been mentioned, to load the initialization code faster, there are two things that need to be done: a context file from the source code (initialization code) needs to be generated and this context file needs to be loaded into memory automatically. The reason that a context file is loaded faster into memory is related to the difference between a context file and its relevant SKILL source file. A SKILL source file needs to be parsed first and then an evaluator, a program to convert the expression to a machine-executable code, is called for each expression; however, in a SKILL context file, the loading files already contains binary data that is loaded into memory directly without parsing and evaluation. To load the context file into memory automatically (when Cadence is being launched), we need to add a line in "*cds.ini*" file to load the context using "*loadContext*" procedure.

3.4 INTERCONNECTLib Components

As it has been mentioned in Section 3.2, creating a library of electro-optical components (INTERCONNECTLib) is a key step of INTERCONNECT integration into Cadence. A few of these components are shown in Fig. 3.5. Fig. 3.6 shows properties of a CWLaser that has already been defined in its CDF.



(a) (b) (c)

Figure 3.5: A few components from INTERCONNECTLib: (A) Photodiode, (B) CWLaser, and (C) Splitter

Figure 3.6: Properties of a CWLaser component that have already been defined in its CDF

3.5 Generate an INTERCONNECT-Compatible Netlist

A textual netlist, which contains components' connectivity, is partially created by the "*asiNetlist*" procedure. A textual netlist has three sections: a netlist header, a netlist body, and a netlist footer. The "*asiNetlist*" method, which is a method of a netlist object, basically acts as the main agent to convert a schematic into a textual netlist. in this process, it uses a formatter object to print a formatted text from properties of schematic components. This format needs to be compatible with formats that INTERCONNECT can import. A code snippet of netlister is show in Code 3.3.

Code 3.3: SKILL code snippet showing "nlPrintInst "procedure overloaded

```
1 defmethod( nlPrintInst ((formatter INTERCONNECTFormatter) inst)
2         let(( (netlister nlGetNetlister(formatter)) tool
              Origin_x Origin_y RotationString (RotationDegree
              "0") (FlipStatus "F")
3                       Transform Cellname AppendString
                            FileName (Scale 3)
                            FileNameExportedSpectre
                            FileImportedINTERCONNECT
                            ImportedNetName)
4                   nlPrintInstComments( formatter inst)
5                   nlPrintIndentString( nlGetNetlister( formatter
                        ))
6                   nlPrintInstName( formatter inst)
7                                   ....................
```

The INTERCONNECT netlist formatting style for every component is shown below; in the following example the number in the parentheses represents the sequential order of parameters.

INTERCONNECT Netlist Formatting Style
InstanceName(1) ConnectedNets(2) InstanceModelName(3) InstanceParameters(4) X_Postion(5) Y_Position(6) RotationStatus(7) FlipStatus(8) Example: I20(1) net05(2) net03(2) nrz_pulse_generator(3) amplitude=4(4) bias=0(4) sch_x=-2.435417(5) sch_y=2.493750(6) sch_r=0(7) sch_f=Y(8)

As you can see from the above formatting style, there are parameters related to position, rotation, and flip status of components inside the schematic that needs to be included in the netlist. Using these parameters, Cadence netlist not only can be imported into INTERCONNECT but also can be recreated, as is in the Cadence schematic, in INTERCONNECT schematic editor. There are a few features that are included in the generated textual netlist; these features are included to make the generated netlist compatible with the importing format of INTERCONNECT; they are listed in the following.

- The main functionality that is the generation of the textual netlist's body is done by the "*nlPrintInst*" procedure, and then this procedure is overloaded to create an INTERCONNECT-compatible textual netlist.
- While nelister is printing components, it will not print electrical components such as resistors, capacitors, and etc. in the generated textual netlist.
- To support electro-optical simulation, there is a component called INTERCONNECTExport in INTERCONNECTLib that provides the netlister with the option of recognizing the electro-optical schematic and also provides INTERCONNECT solver with the required electrical signals extracted from Spectre's time-domain simulation.
- To be compatible with INTERCONNECT netlist, the comment character is changed from # to *
- The netlist header is mainly used to include comments and is generated by overloading the "*nlPrintHeader*" procedure

3.6 Generate Analysis Statements

Each INTERCONNECT analysis needs to have an associated procedure to format its analysis statement. The generated analysis statement needs to be compatible with INTERCONNECT analysis statement. This means that for each analysis we need to overload the "*asiFormatAnalysis*" procedure. A code snippet is shown in Code 3.4 for both INTERCONNECT analyses: ONA and OTRAN

Code 3.4: SKILL Code Showing nlPrintInst Procedure Overloaded

```
1 defmethod( asiFormatAnalysis ((analysis
    INTERCONNECT_ONA_analysis) fp)
2         printf("\n ====> Generating Netlist (Formatting ONA
              Analysis) \n")
3         ..................
4
5 defmethod( asiFormatAnalysis ((analysis
    INTERCONNECT_OTRAN_analysis) fp)
6         printf("\n ====> Generating Netlist (Formatting ONA
              Analysis) \n")
7         ..................
```

3.6.1 OTRAN Analysis Statement

OTRAN analysis is used for optical time-domain/transient analysis. The analysis statement formatting style, which needs to be generated by Cadence, should comply with the following format.

OTRAN Analysis Formatting Style
.otran AnalysisParameters Example: .otran bitrate=25e9 simulation_input=time_window time_window=5e-9 num_of_samples=2048 monitor_data=save_to_memory multithreading=automatic check_disconnected_ports=false check_internal_monitors=true check_analyzer_sensitivity=false source_connections=resolve

A feature that is added in the "*asiFormatAnalysis*" procedure for this analysis is that the user can interactively specify a component's pin to get its time-domain waveform from the simulation results, and the "*asiFormatAnalysis*" procedure will convert it to an ".omonitor" analysis statement that can be recognized by INTERCONNECT netlist importer.

3.6.2 ONA Analysis Statement

ONA analysis, which is an optical frequency domain analysis, is similar to an AC analysis in Spectre. The analysis statement formatting style, which needs to be generated by Cadence, should comply with the following format.

OTRAN Analysis Formatting Style
.ona AnalysisParameters Example: .ona input_unit=wavelength input_parameter=center_and_range center=1550e-9 range=100e-9 peak_analysis=disable analysis_type=scattering_data multithreading=automatic output=I5,opt_a1 input(1)=I13,opt_a1 input(2)=I7,opt_a1 input(3)=I14,opt_b2

3.7 Testing Simulation Environment

3.7.1 OTRAN Analysis

In this section, we demonstrate INTERCONNECT integration in ADE for OTRAN analysis. The schematic in Fig. 3.7 is an optical modulator that is used as an example. Components that have been used in this design are from INTERCONNECTLib that has been created as part of the integration process. These components can be enumarated as: a CWLaser, a GratingCoupler, Waveguides, Splitters, a PhaseShifter, a DCSource, a NRZPulseGenerator, a PseudoBitGenerator, and a Photodiode. In Fig. 3.8 properties of two components: CWLaser and NRZPulseGenerator are shown. These properties were defined using CDF, as has already been mentioned in Section 3.4. The simulation form is shown in Fig. 3.9. This form is designed to be a graphical user interface in which a user can insert simulation parameters. As you can see from Fig. 3.9, analysis form is designed to support two analyses: ONA and OTRAN. It should be mentioned that this form is implemented to be an interactive form. In other words, if you change the "Simulation Input" drop-down menu from "time_window" to "sequence_length", subsequently "Time Window" and "Number of Samples' text boxes will be disabled and "Sample per Bit" and "Sequence Length" text boxes will be enabled.

As has been mentioned in Section 3.6, the user can select a specific terminal of a component to see its time-domain simulation result. This process is shown in Fig. 3.10a and Fig. 3.10b. The generated netlist from the schematic in Fig. 3.7 is shown in Fig. 3.10c. The pins where selected inside schematic

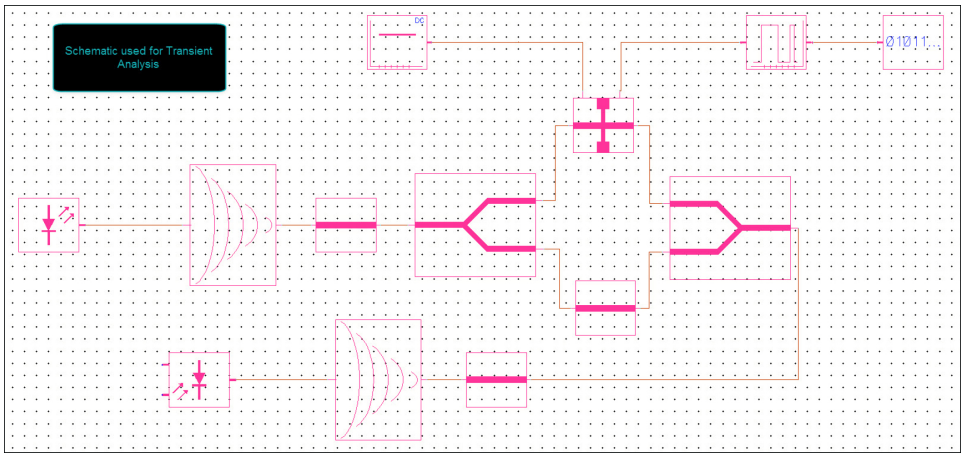
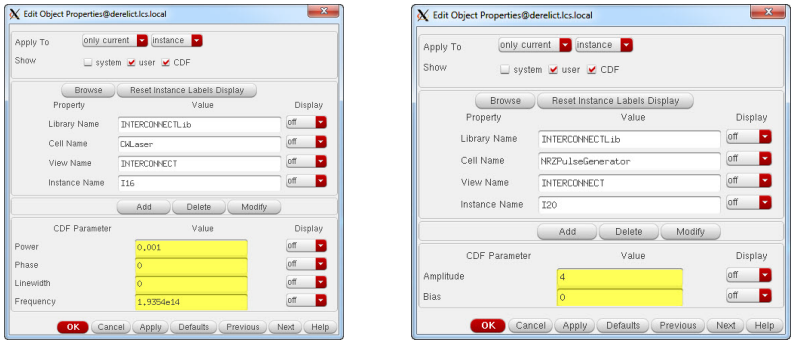


Figure 3.7: Schematic of an optical modulator, which is used as an example, to demonstrate INTERCONNECT integration in Cadence for OTRAN analysis



(a) (b)

Figure 3.8: Properties of two components used in schematic of Fig. 3.7: (A) CWLaser and (B) NRZPulseGenerator

editor are converted to an ".omonitor" analysis statement recognizable by INTERCONNECT. Fig. 3.11a shows ADE before running the simulation. Fig. 3.11b shows INTERCONNECT simulation result visualized in Cadence.

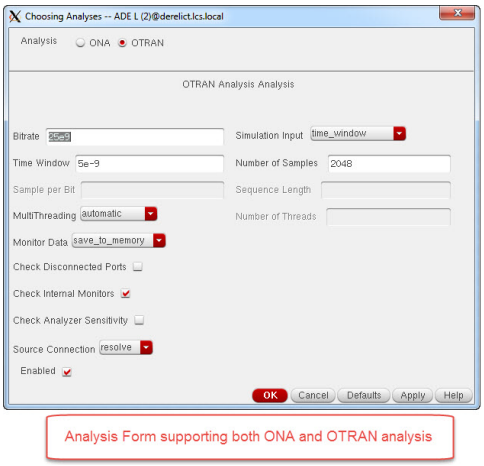
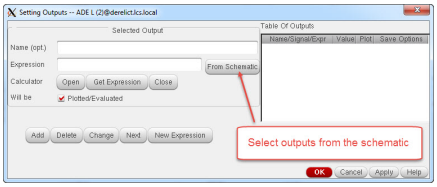
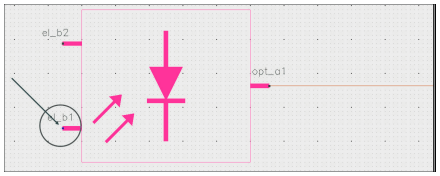


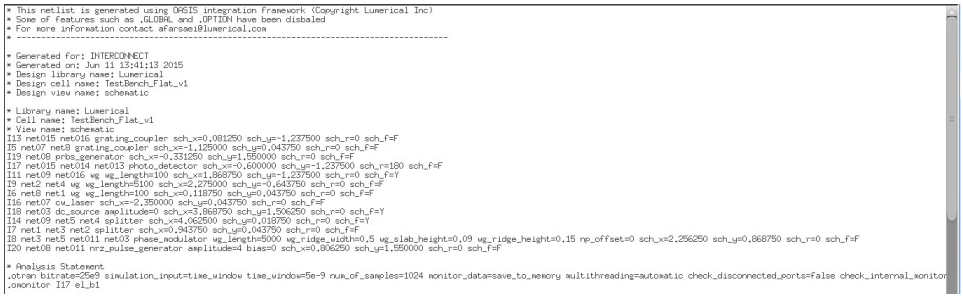
Figure 3.9: Analysis form for OTRAN analysis. User will insert simulation parameters here



(a)

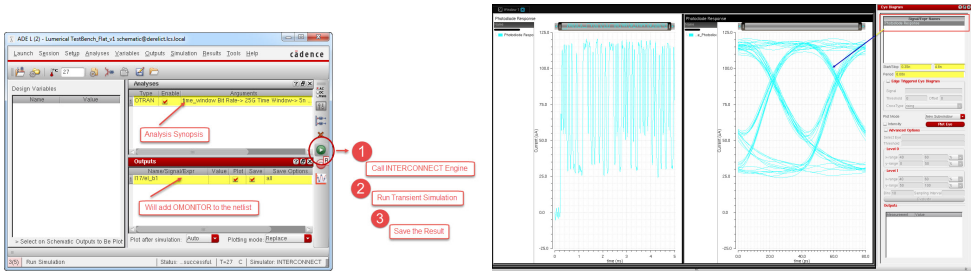


(b)



(c)

Figure 3.10: Specify outputs that to be plotted (A) Selecting output in ADE, (B) Select the terminal, and (C) Final generated netlist of the schematic including the selected pins shown as ".omonitor" analysis statements



(a) (b)

Figure 3.11: Running INTERCONNECT simulation: (A) ADE before running the simulation and (B) Visualize INTERCONNECT simulation results in Cadence

3.7.2 ONA Analysis

In this section, we demonstrate INTERCONNECT integration in ADE for ONA analysis. The schematic in Fig. 3.12 is an asymmetrical Mach-Zehneder that is used as an example. Components that have been used in this design are from INTERCONNECTLib that has been created as part of the integration process. These components can be enumerated as: Grating-Couplers, Waveguides, and Splitters.

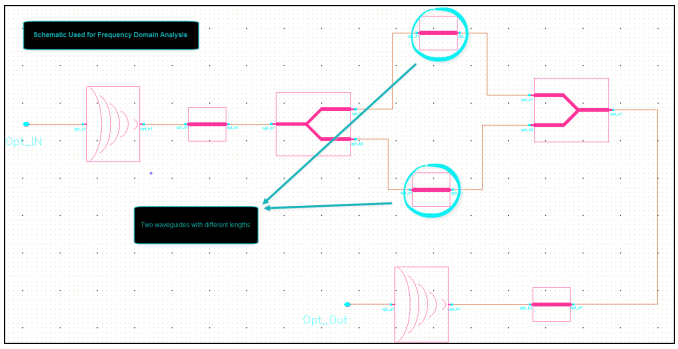
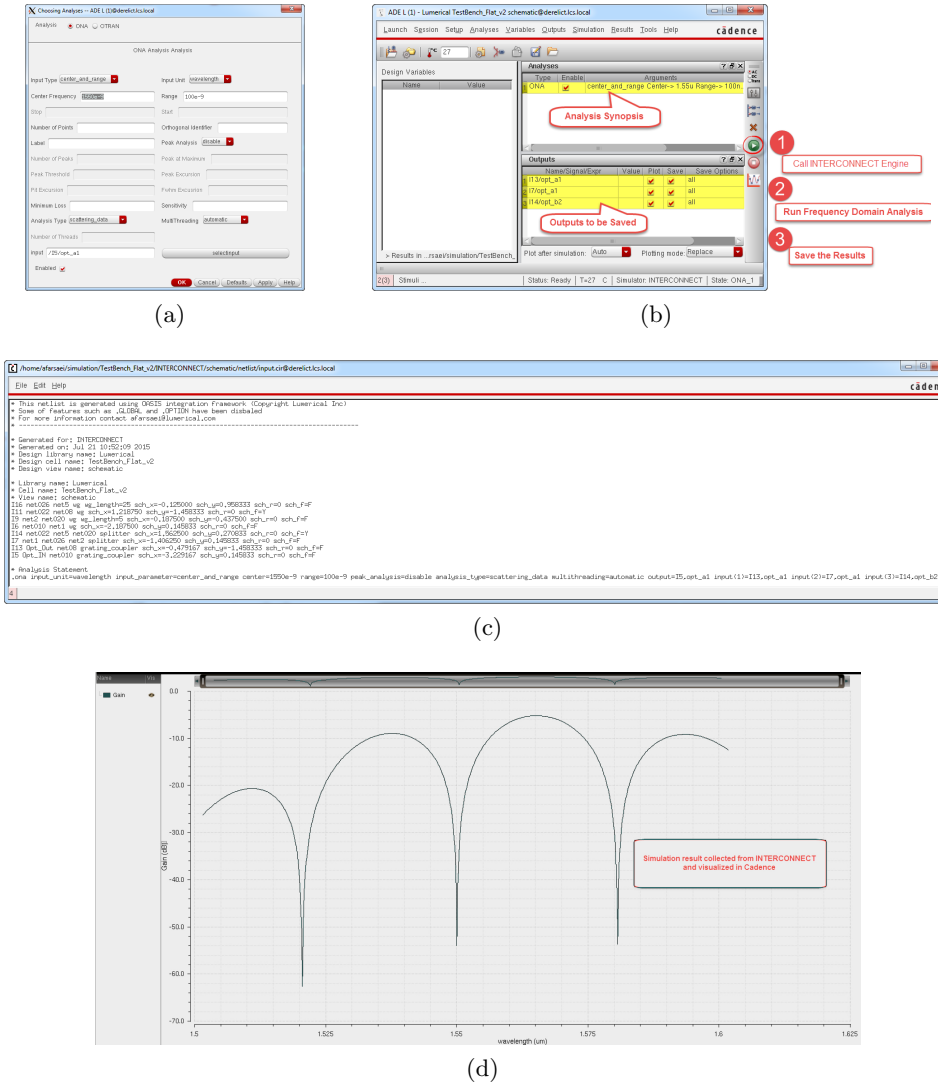


Figure 3.12: Schematic of an assymetrical Mach-Zehneder, which is used as an example, to demonstrate INTERCONNECT integration in Cadence for ONA analysis

Fig. 3.13 shows the process of using ADE to run an ONA analysis. The simulation form, which is implemented for ONA analysis, is shown in Fig. 3.13a. As mentioned before, this form is designed to be interactive



(a) (b)

(c)

(d)

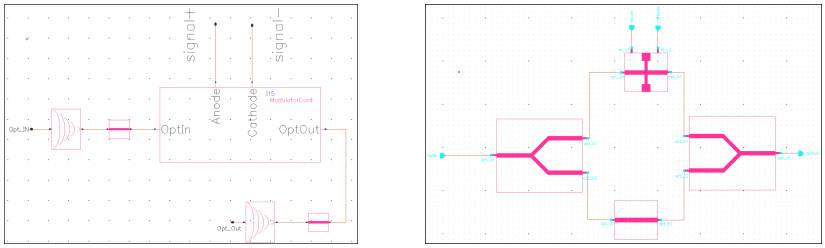
Figure 3.13: Steps for setting up ONA analysis inside ADE: (A) ONA analysis form, (B) ADE window before running the simulation, (C) Final generated netlist of the schematic, and (D) Simulation results collected from INTERCONNECT and visualized in Cadence

which means when user select “star_and_stop” from the drop-down menu instead of “center_and_range”, subsequently the “Center Frequency” and “Range” text boxes will be disabled and the “Stop” and “Start” text boxed

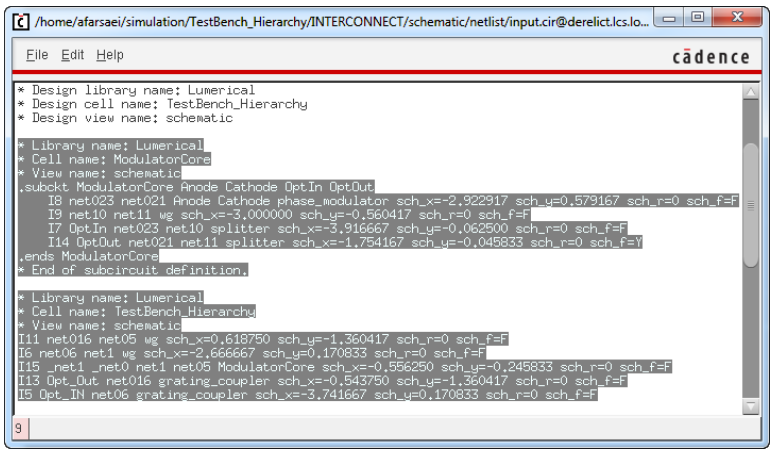
will be enabled. The ADE window is shown in Fig. 3.13b and the generated netlist is shown in Fig. 3.13c. As is shown in Fig. 3.13b, the user can select the outputs that need to be saved interactively and our code will include it in the ONA analysis statement with the appropriate formatting style. Fig. 3.13d shows simulation results visualized inside Cadence.

3.7.3 Hierarchy Support in Netlist

Our code supports hierarchical structures and it will generate the appropriate formatting style that is compatible with INTERCONNECT hierarchical netlist format. An example of a hierarchical schematic and the generated netlist from the schematic is shown in Fig. 3.14.



(a) (b)

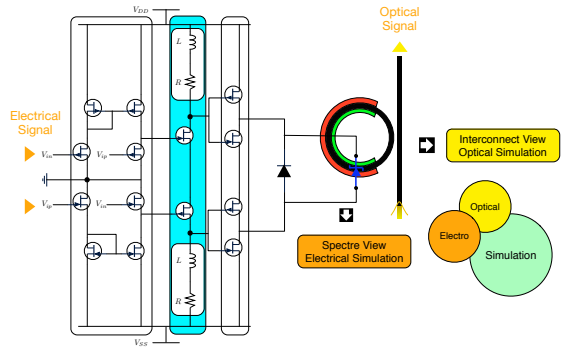


(c)

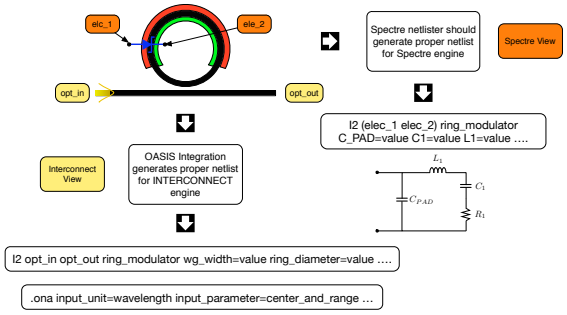
Figure 3.14: The Integration package developed supports hierarchical schematics and converts them to correct formatting style: (A) Hierarchical schematic, (B) Hierarchical cell, and (C) Generated netlist showing support of netlisting hierarchical schematics

3.8 Electro-Optical Co-simulation

In two previous sections the simulation environment test for ONA and OTRAN analyses was presented. It was shown that optical schematics can be simulated in Cadence using INTERCONNECT as an integrated engine in ADE. To be able to co-simulate electro-optical schematics, there should be an element connecting simulation results in electrical domain to proper electrical nodes in the optical domain. This connection could be understood by a simple diagram showing the concept of co-simulation as is shown in Fig. 3.15. In this figure, a CMOS driver and an optical ring modulator are



(a)



(b)

Figure 3.15: Electro-Optical co-simulation concept using INTERCONNECT integration as the optical solver and Spectre as the electrical solver

used to show the concept of co-simulation. The ring modulator has two electrical ports, elc_1 and elc_2, and two optical ports, opt_in and opt_out. To be able to simulate a schematic that contains this element, the electrical sub-section needs to be simulated first using Spectre as an electrical solver

and electrical signals related to nodes elc_1 and elc_2 should be saved for further use in optical analyses. The optical sub-section of the schematic needs to be simulated with the required extracted signals from the electrical domain; eventually the final results should be able to be shown in Cadence visualizer. As you can see from Fig. 3.15, an important step in this process is to include the loading effect of the electro-optical element, , which is the optical ring modulator, in the electrical domain. This could be done using lumped elements as shown in Fig. 3.15.

3.8.1 Testing Electro-Optical Co-simulation Environment

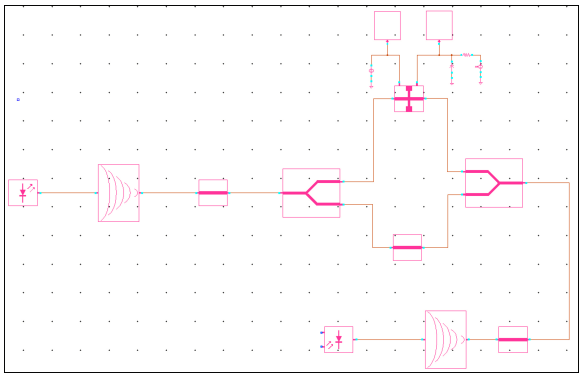
In this section an electro-optical schematic will be used as an example to test the co-simulation environment. The schematic is shown in Fig. 3.16.

In this schematic, the electro-optical element is the PhaseModulator and its equivalent model is shown in Fig. 3.17b. As you can see from Fig. 3.17a, electrical properties of this component are included in its CDF and can be set by the designer.

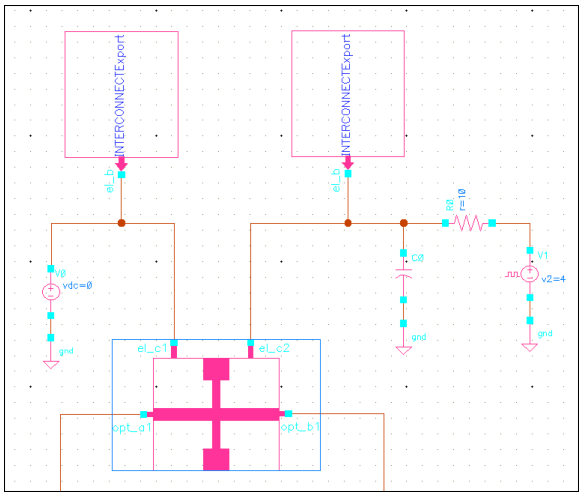
The steps to do co-simulation are shown in Fig. 3.18. As you can see from the figure, the simulation is run in the electrical domain using Spectre as the simulation engine and then optical simulation is run by changing the simulator to INTERCONNECT; the INTERCONNECT engine will extract electrical results generated by the precedent Spectre simulation and then will do optical simulation and results can be seen in Cadence visualizer as shown in Fig. 3.19.

3.8.2 Using Cadence Open Command Enviroment in Co-simulation

Cadence Open Command Environment for Analysis (OCEAN), which is part of Cadence suite, can be used to set up, simulate and analyse circuit data. In our code, it is used to access simulation results generated by Cadence Spectre. A key element in the electro-optical co-simulation that uses OCEAN functionality is INTERCONNECTExport. As is shown in Fig. 3.16b, when INTERCONNECT netlister is launched to netlist electro-optical schematics, this element will indicate that signals needs to be extracted from Cadence Spectre analysis. As a result, netlister will use OCEAN skill procedures to access Spectre simulation results and extract required signals; these extracted signals are stored as text files and the name of text files are the same as the name of nets attached to INTERCONNECTExport components. It should be mentioned that extracted signals from Spectre are not compati-



(a)

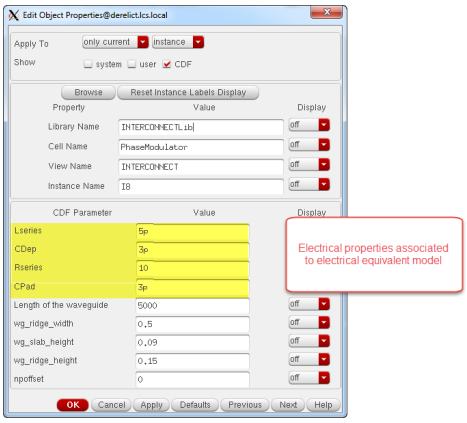


(b)

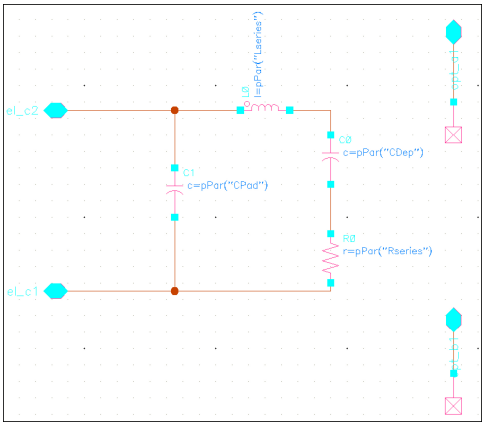
Figure 3.16: Electro-optical schematic: PhaseModulator acts as an electro-optical element that needs to be modelled both in electrical and optical domains

ble with the required format for importing signals, so a conversion needs to happen. This conversion is coded as a regular expression substitution in our integration package.

The other important issue that needs to be considered is a referring method(a relative or absolute path) to the generated text files from Spectre. To make it easier to access these files, they should be stored in the same directory that contains the generated netlist for INTERCONNECT engine. This needs to be done because when INTERCONNECT engine



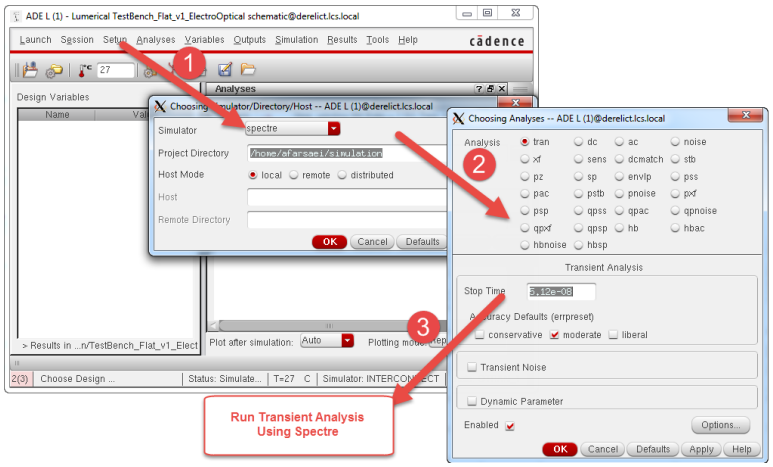
(a)



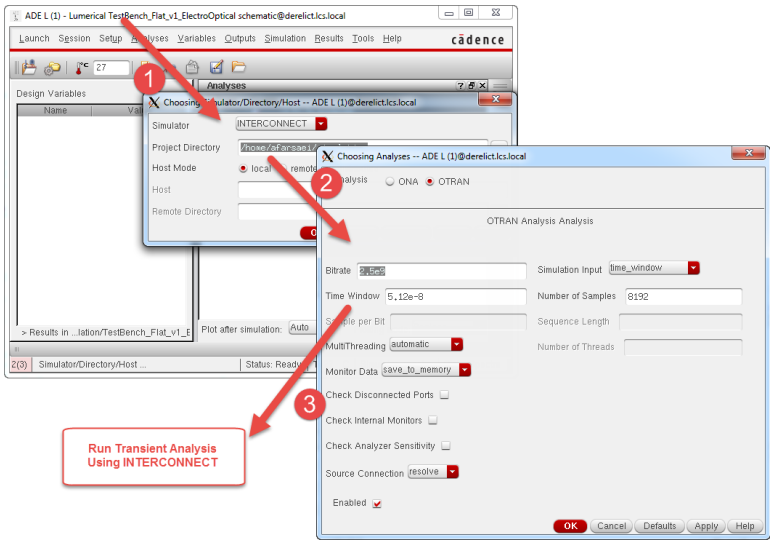
(b)

Figure 3.17: CDF parameters of a PhaseModulator showing the inclusion of electrical properties associated to the electrical equivalent model

reads the generated netlist, it generates components equivalent to INTERCONNECTExport in its environment whose "filename" property specifies name of the file that has the extracted signal (from Spectre); and INTERCONNECT assumption is that this file is located in the directory of the previously generated netlist. The generated netlist of Fig. 3.16 is imported into INTERCONNECT and the result is shown in Fig. 3.20. As can be seen, the INTERCONNECTExport components in Cadence are substituted by equivalent components, cdnimport, inside INTERCONNECT environment.



(a)



(b)

Figure 3.18: Steps that needs to be done in Cadence ADE for the co-simulation of an electro-optical schematic

3.8.3 Data Structure of the Simulation Results

one important stage, which is also the final stage, in the integration of an optical engine solver in an electrical engine solver is the capability of showing and post-processing simulation results, which is already generated by the optical solver. Because the data model/format used in optical engine

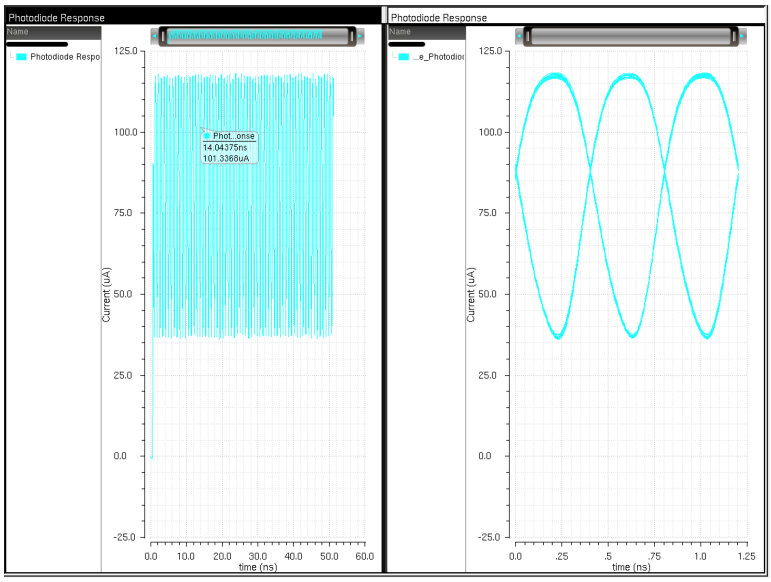


Figure 3.19: Electro-optical co-simulation results of Fig. 3.16

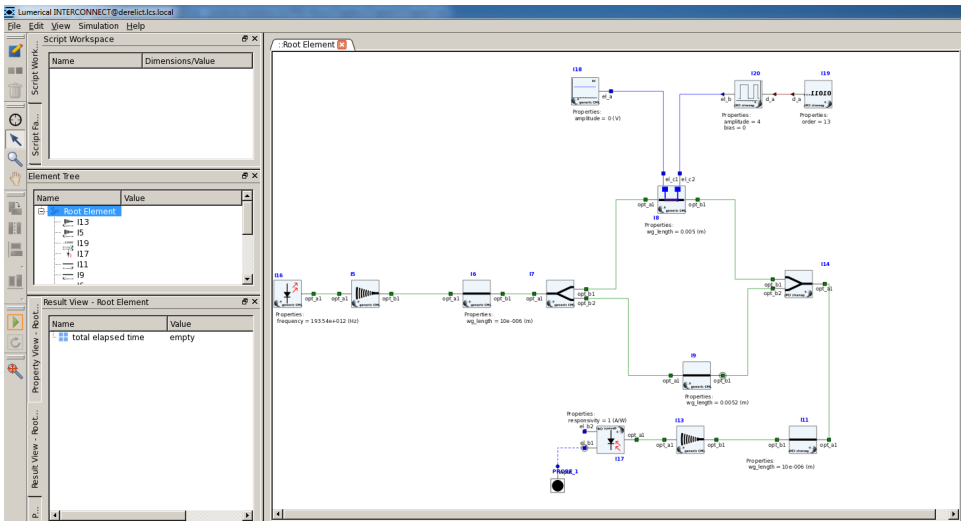


Figure 3.20: INTERCONNECT representation of the generated netlist from Cadence schematic of Fig. 3.16

solvers, to generate simulation results, is different from the data model/format that electrical visualizers, which are used to show the results in the form

of graphs, can read/analyze; consequently research should be done to find an efficient and suitable algorithm/method to solve this inconsistency. The results shown in previous sections, which is shown in Cadence visualizer, are based on Virtuoso Comma Separated Value (VCSV) data structure. This data structure is similar to Comma separated Value(CSV), where data is separated using comma, and is one of the data structures that is compatible with Cadence visualizer. CSV is the data structure that is used by INTERCONNECT for its generated simulation results. Although CSV and VCSV are quite similar in their data structure, there still some conversion that needs to be done on CSV so that it can be displayed in Cadence visualizer (this is what we have done to show the simulation results in this chapter). Because this conversion hasn't been accounted in the OASIS integration framework, the simulation results will not pop up automatically after they are generated by INTERCONNECT; and moreover modes associated to different ports of an optical component cannot be categorized as a family easily in this format , and consequently post-processing of the simulation results is quite challenging. To circumvent these issue, Parametric Storage Format(PSF) is used as the data structure of generated simulation results by INTERCONNECT. In the next chapter, this data structure and its use in the integration of electrical and optical simulators are discussed in details.

3.9 Conclusions

In this chapter, we have discussed the simulation core of the EPDA framework. We have demonstrated that the developed EPDA framework supports both optical and electro-optical simulations. We have shown that electro-optical simulations can be categorized into two groups: electro-optical sequential simulations and electro-optical co-simulation, and we have proposed a new methodology to resolve the challenges related to electro-optical co-simulation using Verilog-A Direct Programming Interface (DPI). Our main contributions in this chapter can be listed as follows:

- Developed a photonic library using SKILL language to evaluate the EPDA framework. This library can be used as the foundation for further developments of photonic Parameterized Cells (PCell).
- Presented a new scalable methodology to resolve electro-optical co-simulation based on Verilog-A DPI. This methodology will be demonstrated in 5.

- Developed and implemented the functionality to generate an INTERCONNECT compatible netlist using Open Analog Simulator Interface Socket (OASIS) from schematics captured in Virtuoso.
- Developed the functionality to generated analysis statements for ONA and OTRAN analyses that are compatible with INTERCONNECT netlist importer.
- Developed and implemented the functionality to support hierarchical photonic designs in the generated netlist that is also compatible with INTERCONNECT netlist importer.
- Developed and implemented the functionality to do a sequential simulation using INTERCONNECT Export components.

Chapter 4

Data Structure in Electro-optical Co-simulation

AS was already discussed in Chapter 3, the simulator for the electrical section of an electro-optical design is set to be Spectre and the simulator for the optical section of an electro-optical design is set to be INTERCONNECT. Both of these simulators should generate a data structure which is compatible with a data structure that the Cadence data viewer and analyzer (ViVA) can read. Since the Spectre engine is already designed to generate the simulation result in a data format acceptable to ViVA, the challenge that needs to be addressed is the consistency/compatibility with the INTERCONNECT-generated results and their compatibility with ViVA-supported data structures.

Spectre generates its results in a format called Parametric Simulation Format (PSF), which is one of the formats supported by ViVA. To be consistent with the Spectre-generated simulation results and also because of availability of the C/C++ package, by Cadence to support this format in the OASIS framework, PSF is chosen to be the data structure that INTERCONNECT needs to support. There are different ways to support PSF format when INTERCONNECT simulation results are being generated: either convert the INTERCONNECT-generated data structure to a data structure that is readable by ViVA (which is PSF in this case) or use OASIS integration library, which is provided by Cadence and use Parametric Storage Library (PSL). In the latter case, appropriate function calls from PSL Library needs to be inserted in the INTERCONNECT source code to support the PSF data structure. Each of the mentioned methods has its own advantages and constraints in terms of speed, multi-threading support, support of advanced analysis such as parametric and statistical analysis (Monte Carlo), post-processing of the simulation results using Cadence Calculator, etc. These advantages and constraints need to be researched and analyzed to choose an efficient method to support PSF data structure so that INTERCONNECT-generated results are compatible with this format. All of the above functionality, which is explained in more details in the following

sections, is delivered as a new software package coded in SKILL/SKILL++ and C/C++ languages.

Inherent inconsistency between the generated simulation results in the electrical domain and optical domain makes developing a proper data structure for storing optical simulation results a crucial stage. For example, in the electrical domain, two terminals attached to a resistor can store their voltages and currents and these values are a single-value floating point numerical data; however, an optical component such as an optical waveguide (if it is modeled as a two port device) can have multiple modes associated to each of its ports. Developing a data structure to store these modes in a PSF format, which are readable in ViVA, is crucial for post-processing of the generated results using the Cadence calculator. This could be understood by the fact that if the generated results are stored as separate entities (called Traces in PSF format), then the Cadence calculator will not recognize them as a family and their post-processing as a group will be challenging for a designer.

A few of the features provided to a designer by this new software package developed using SKILL/SKILL++ and C/C++ are as follow:

- Support of advance analysis such as parametric sweep
- Designer will be provided by two data formats for the generation of simulation results in INTERCONNECT: Comma Separated Value(CSV) that is already supported by INTERCONNECT and a new data format, PSF, which is aimed to support integration with Cadence
- Automatic plotting feature and family creation in ViVA based on the generated results by INTERCONNECT
- Detection of electrical and optical results in PSF file and automatic family creation using different modes of each optical components' terminal
- Support and detection of distributed simulation results: one simulation result for each probe added to schematic (in PSF format) for OTRAN analysis

4.1 Introduction to Parametric Sotrage Format

Parametric Storage Format (PSF) is a format for storing complex (real and imaginary part) structured data. PSF can support both non-sweep mode

and sweep mode. In the non-sweep mode the data generated are a collection of objects having identifiers and values and in the sweep mode the data can be modelled as objects acting as dependent variables vs some objects acting as independent variables.

PSF files can also be created in two forms: textual and binary. Binary PSF files are more compact and they can be processed more efficiently using application programs. In PSF files, the data is structured into different tables. Every PSF file could consist of five to seven tables depending on the mode (sweep or non-sweep mode); these tables are as follows:

- Headear Table: contains the header properties such as "simulation start frequency"
- Type Table: contains the definition of data that is going to be used in the Sweep and Trace tables
- Sweep Table: it specifies the independent variables that are swept in this PSF file such as "frequency" in the ONA analysis or "time" in the OTRAN analysis
- Trace Table: specifies the dependent variables (used only in the sweep mode). This could be transmission (gain or loss) of an optical mode
- Value Table: specifies the values related to the independent (swept variable) and dependent objects
- Trailer Table: similar to the header table, this table contains trailer properties that are represented as "property name" "property value"
- End Table: this table doesn't contain anything; it just specifies the end of PSF file

Basically each table starts with the table name, followed by the entries for that table except the end table, which doesn't have any entries. The PSF structure is designed in a way that if a PSF file is in the sweep mode, for each sweep point, each signal should be printed in the PSF file. In the following sections, a few examples of textual PSF files are discussed to get not only a better understanding of this format but also the generality of this data structure in representing data.

4.1.1 Schematic Representation Using PSF

In the following example, the schematic is represented by nodes ("net") to which components are connected. Each node is given a name and its type

is set as a variable- length array containing connected element's names that is connected to the relevant node (for example "I1" could be a laser source that is connected to "net01"). As mentioned before the header and trailer tables could be used to specify header and trailer properties in the format of "Property Name" "Property Value" as shown in Code 4.1. It should be mentioned that "PSF Version" is a mandatory property that needs to be specified in every PSF file.

Code 4.1: Circuit representation using PSF data structure

```
HEADER
        "PSF Version" "1.00"
        "Simulator" "INTERCONNECT"
        "Design" "MZI"
TYPE
        "componentList" ARRAY (*) STRING 4
VALUE
        "net01" "componentList" ("I1" "I2" "I3")
        "net02" "componentList" ("I4" "I5" "I6")
        ...
        ...
        ...
TRAILER
        "Number of Modes" 3
END
```

The entries in the value table are called objects; each object has name, type and its value. Like other data structures the type of the object should be consistent with its value. For example, in Code 4.1 "net01" is an object of type "componentList" and component "I1", "I2", and "I3" are connected to this specific node.

4.1.2 Using a Structure Type inside PSF

A simple schematic is shown in Fig. 4.1, this schematic can be represented by a PSF file if each component is self-contained, i.e., has all information related to attached nets to a component's ports; this is where a structure type can be useful. Structures could be used inside a PSF file to group list of parameters under one name; for example the schematic shown in Fig. 4.1 can be represented by a PSF file as shown in 4.2.

Code 4.2: Circuit representation using PSF and structure data type

```
HEADER
        "PSF Version" "1.00"
        "Simulator" "INTERCONNECT"
        "Design" "MZI"
```

```
TYPE
        "netName" STRING *
        "3port" STRUCT(
                "opt_a1" USER "netName"
                "opt_b1" USER "netName"
                "opt_b2" USER "netName"
        )
        "Waveguide" STRUCT (
                "opt_a1" USER "netName"
                "opt_a2" USER "netName"
        )
VALUE
        "Waveguide1" "Waveguide" ("0" "1")
        "PowerSplitter" "3port" ("1" "2" "3")
TRAILER
        "Number of Components" 2
END
```

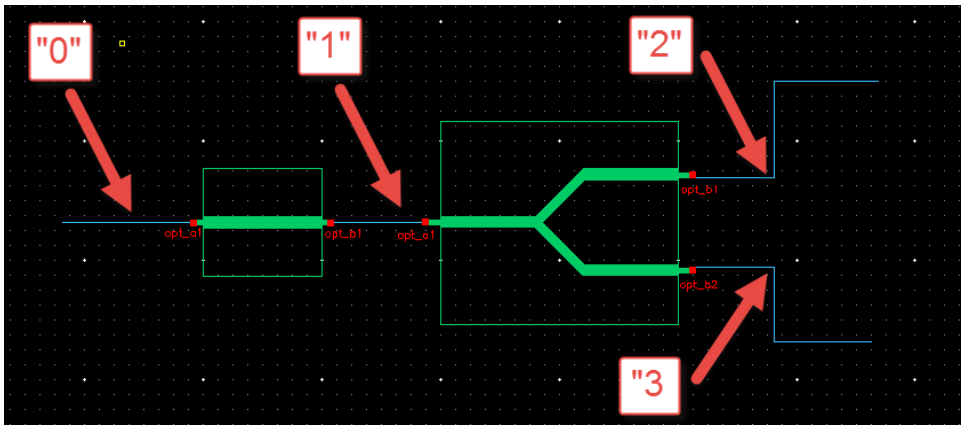


Figure 4.1: A schematic representation of the PSF Code 4.2

Using structures in a PSF file is basically similar to the use of a structure data type in other high-level languages such as C. In Code 4.2, the structure data type is used to define a "3-port" data that is defined such that it contains three other use-defined data types "netNames" specifying names of connected nets to its ports. Code 4.2 shows the use of this data type to define an object named "PowerSplitter".

4.1.3 Sweep-Mode PSF File

In a sweep-mode PSF file, there is another table called "SWEEP"; the independent variables' declaration are written in this table. For example, in

frequency domain analysis such as ONA, “frequency” is swept and act as an independent variable and in time-domain analysis such as OTRAN, “time” is used as an independent variable. Signals which are acting as independent variables are specified in the “TRACE” table. In the sweep-mode, the value of each signals needs to be specified for each value of sweep variable, which is a frequency value for a frequency domain analysis and a time value for a time-domain analysis.Code 4.3 shows a part of a PSF file generated by ONA analysis using INTERCONNECT.

Code 4.3: PSF file generated by INTERCONNECT for an ONA analysis

```
1  HEADER
2  "PSFversion" "1.00"
3  "BINPSF creation time" "1442528571"
4  "simulator" "INTERCONNECT"
5  "version" "5.1.588"
6  "date" "Thu Sep 17 15:22:51 2015"
7  "design" "// Generated for: INTERCONNECT"
8  "analysis type" "ona"
9  "analysis name" "ona"
10 "analysis description" "Optical Network Analysis ‘ona’: freq =
       (1.5016094723uHz -> 1.6017201108uHz)"
11 TYPE
12         "sweep" FLOAT DOUBLE
13         "V" COMPLEX DOUBLE
14 SWEEP
15         "freq" "sweep"
16 TRACE
17         "I13:opt_a1:mode 1" "V"
18 VALUE
19         "freq" 1.601720111e-06
20         "I13:opt_a1:mode 1" (-0.1740746734 0.06227359059)
21         "freq" 1.601613226e-06
22         "I13:opt_a1:mode 1" (-0.05103597787 0.1723881217)
23         "freq" 1.601506356e-06
24         "I13:opt_a1:mode 1" (0.1058248655 0.1380045451)
25         "freq" 1.6013995e-06
26         "I13:opt_a1:mode 1" (0.1671349037 -0.003930848825)
27         "freq" 1.601292658e-06
28         "I13:opt_a1:mode 1" (0.09160033176 -0.1315646699)
29         "freq" 1.60118583e-06
30         "I13:opt_a1:mode 1" (-0.05002219102 -0.1445591218)
31         "freq" 1.601079017e-06
32         "I13:opt_a1:mode 1" (-0.1385093756 -0.04235248669)
33         "freq" 1.600972218e-06
34         "I13:opt_a1:mode 1" (-0.1091799838 0.08174434085)
35         "freq" 1.600865433e-06
36         "I13:opt_a1:mode 1" (0.001606037555 0.1276116108)
```

```
37          ...
38          ...
39          ...
40 END
```

As you can see from Code 4.3, the new "SWEEP" table declared the "freq" as the sweep variable's name and it is of "sweep" data type that is a floating-point data type with double precision. In the "VALUE" table "freq" is swept and for each value of "freq", the signal needs to be specified. In Code 4.3, signal is defined in the TRACE table as "I13:opt_a1:mode 1" and it is of data type "V", which is a floating-point complex number with double precision. Complex data type and its value needs to be specified using the following format: "(Complex Value Real Part Complex Value Imaginary Part)".

4.1.4 Using Group and Nested Sweep

In 4.2, "freq" is the only variable that is swept; however, multiple variables can also be swept. In Code 4.3, if there are many signals in the "TRACE" table, then each signal's name and value should be specified in the "VALUE" table for each value of swept variables. This could increase the length of the file, especially when there are nested(multiple) sweeps. To circumvent this issue, a "GROUP" specifier can be used inside a PSF file. A sample PSF file generated by INTERCONNECT for an ONA analysis containing both the grouping and nested(multiple) sweep features is shown in 4.4.

Code 4.4: PSF File generated by INTERCONNECT for an ONA analysis showing "GROUP" feature and nested sweep

```
1  HEADER
2  "PSFversion" "1.00"
3  "BINPSF creation time" "1442528571"
4  "simulator" "INTERCONNECT"
5  "version" "5.1.588"
6  "date" "Thu Sep 17 15:22:51 2015"
7  "design" "// Generated for: INTERCONNECT"
8  "analysis type" "ona"
9  "analysis name" "ona"
10 "analysis description" "Optical Network Analysis 'ona': freq =
       (1.5016094723uHz -> 1.6017201108uHz)"
11 TYPE
12          "sweep" FLOAT DOUBLE
13          "V" COMPLEX DOUBLE
14 SWEEP
15          "freq" "sweep"
16          "waveguidelength" "sweep"
17 TRACE
```

```
18          "DATA" GROUP 2
19          "I13:opt_a1:mode 1" "V"
20          "I13:opt_a1:mode 2" "V"
21  VALUE
22          "waveguidelength" 1e-6
23                  "freq" 1.601720111e-06
24                          "DATA"
25                          (-0.1740746734 0.06227359059)
26                          (-0.1740746734 0.06227359059)
27                  "freq" 1.601613226e-06
28                          "DATA"
29                          (-0.05103597787 0.1723881217)
30                          (-0.05103597787 0.1723881217)
31                  ....
32                  ....
33                  ....
34          "waveguidelength" 1.5e-6
35                  "freq" 1.601720111e-06
36                          "DATA"
37                          (-0.1740746734 0.06227359059)
38                          (-0.1740746734 0.06227359059)
39                  "freq" 1.601613226e-06
40                          "DATA"
41                          (-0.05103597787 0.1723881217)
42                          (-0.05103597787 0.1723881217)
43                  ....
44                  ....
45                  ....
46          ....
47          ....
48          ....
49  END
```

In Code 4.4, there are two variables defined as sweep variables and they will be swept in a nested manner; moreover, "DATA" is going to act as a group and in the "VALUE" table, there is no need to repeat signals' names, i.e., "I13 opt_a1 mode 1" and "I13 opt_a1 mode 2".

4.2 Supporting Data Types in PSF Data Structure

PSF supports the following data types:

- Integer data type: PSF supports both integer data types (INT) and unsigned integer (UNSIGNED), and the precision of the data type could be BYTE, SHORT, LONG, or HYPER

- Floating point data type: keyword for the floating point is FLOAT, and its precision can be either DOUBLE or SINGLE
- Complex number data type: its keyword is COMPLEX, and its precision could be one of the floating point data type's precision
- Text data type: this data type specifies a single character or a string data. There is no precision for this data type; instead the user can specify the length of the text data as a fixed number (unsigned integer) or a variable-length string
- Array data type: its keyword is ARRAY, and it should be followed by the size of the array
- Structure data type: structures can be declared using STRUCT keyword and should have one or more parameters (refer to Code 4.2); each parameter should have a name and a data type

4.3 Parametric Storage Format Log Files

As is shown in the previous sections, simulation data can be stored in PSF format. Unless simulation data is readable by Cadence tools such as Analog Design Environment and Result Browser, there is not much use for it in INTERCONNECT-Cadence integration. For this purpose, there should be a file describing the relationship between generated simulation results and different types of simulations such as ONA, OTRAN, parametric analysis, etc. In PSF data structure, this file is called a log file. This log file includes the following information and describe the structure of the data generated by the simulator.

- A unique name for the analysis which is of type "analysisInst"
- Type of the analysis: this could be an already defined analysis such as ac, tran, and noise or it could be a custom analysis such as ONA or OTRAN.
- "dataFile": This is the file where simulation results are stored in PSF format.
- "format": specifies the format of the data file, which is PSF in our case.

- Name of the parent analysis: this is useful if we want to model our simulation results such that there is a parent analysis and there are some subsequent child analyses based on the change in the some parent analysis's parameters.
- Name of the sweep variables
- Description of the analysis
- Data type generated by the analysis, which is ONA or OTRAN analysis in our case. Data type could be either of scalar, swept_scalar, struct or swept struct. The data type used for ONA and OTRAN analysis is swept_scalar.
  - Scalar data type: this data type is used for an analysis that create data in a numeric format. For example, this data type could describe data type generated by a DC analysis.
  - swept_scalar: this data type is used for an analysis that creates a scalar value which is swept over an independent variable. This could be used for example to describe the data generated by INTERCONNECT for an ONA analysis.

The content of log files related to ONA and OTRAN analysis will be discussed in the following sections. The log files for these analyses not only are different in their nature (because one of them is frequency domain analysis and the other one is time-domain analysis), but also the structure of files associated with simulation results for these two analyses are also different. In ONA analysis there is only one file that keeps the simulation results; however, in OTRAN analysis every selected output will have its own PSF file; consequently, OTRAN analysis will have different "analysisInst" entries for each selected output while ONA has just one "analysisInst".

4.4 Parametric Storage Format and ONA/OTRAN Analysis in ADE

Parametric Storage Format(PSF) is a data format/model that Analog Design Environment (ADE) can read and susequently plot, back annotate, and display its simulation results. PSF is designed to be able to support different kinds of data generated by different types of analysis such as DC, AC, transient. Cadence provides two general techniques to write simulation data in a PSF format:

- Using the Cadence SPICE PSF writer
- Using the Parametric Storage Library (PSL) functions

Because SPICE PSF write functions are designed to support Cadence SPICE data, they are not efficient for the simulation results' data generated by ONA or OTRAN analysis. Having said that, separate PSF writer functions based on PSL functions have been developed to convert the data generated by ONA and OTRAN analysis to their PSF equivalent. The developed code is included in the INTERCONNECT source code and a new INTERCONNECT build is generated to support the new added feature.

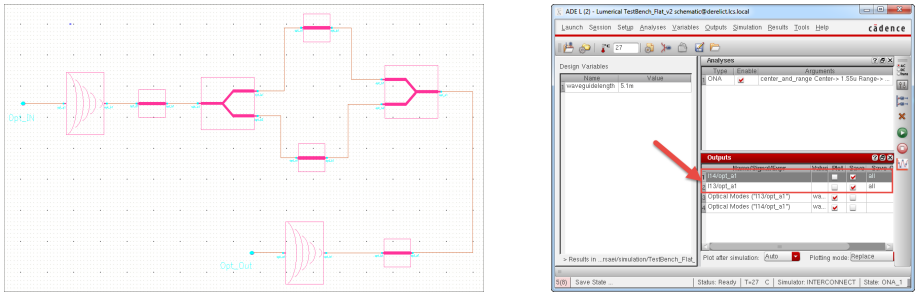
4.4.1 PSF for ONA Analysis inside ADE

As was shown in the previous chapter, the user needs to specify the ports whose simulation results needs to be stored; these stored simulation results subsequently could be used for post-processing. These outputs selected inside the Cadence schematic editor are going to be inputs to a component named "Optical Network Analyzer" in INTERCONNECT. A schematic and its ADE environment is shown in Fig. 4.2. A part of generated simulation results, which is in PSF, is shown in Code 4.5.

Code 4.5: PSF file generated by INTERCONNECT for an ONA analysis

```
1  HEADER
2  "PSFversion" "1.00"
3  "BINPSF creation time" "1442879609"
4  "simulator" "INTERCONNECT"
5  "design" "// Generated for: INTERCONNECT"
6  "analysis type" "ona"
7  "analysis name" "ona"
8  "analysis description" "Optical Network Analysis 'ona': freq =
       (1.5016094723uHz -> 1.6017201108uHz)"
9  "start" 1.50161e-06
10 "stop" 1.60172e-06
11 "operating point producer" "ona"
12 "modes" "I13:opt_a1;TE/I14:opt_a1;TE"
13 TYPE
14         "sweep" FLOAT DOUBLE
15         "V" COMPLEX DOUBLE
16 SWEEP
17         "freq" "sweep"
18 TRACE
19         "I13:opt_a1:mode 1" "V"
20         "I14:opt_a1:mode 1" "V"
21 VALUE
```

```
22          "freq" 1.601720111e-06
23                  "I13:opt_a1:mode 1" (-0.1740746734
                        0.06227359059)
24                  "I14:opt_a1:mode 1" (0.2104890468
                        -0.2633380311)
25          "freq" 1.601613226e-06
26                  "I13:opt_a1:mode 1" (-0.05103597787
                        0.1723881217)
27                  "I14:opt_a1:mode 1" (-0.09440551909
                        -0.3133204356)
28          "freq" 1.601506356e-06
29                  "I13:opt_a1:mode 1" (0.1058248655 0.1380045451)
30                  "I14:opt_a1:mode 1" (-0.3010378069
                        -0.09595434149)
31          ...
32          ...
33  END
```



(a) (b)

Figure 4.2: Generated PSF by INTERCONNECT for an ONA analysis: (A) Schematic, (B) ADE Environment

As you can see from Code 4.5, the generated results have different modes associated to each port. These modes need to be modelled as a family so that they can be post-processed efficiently by a designer. Having said that, we developed a function to parse the PSF file and not only create a family for modes associated to an optical port but also resolve the name of each mode based on the information given in the "HEADER" table of the PSF file. This can be better understood by inspecting the value of "modes" property in the "HEADER" table in Code 4.5. Function "MakeModeTable", shown in Code 4.6, gets the value of "modes" property and creates an association table based on that. For example, "mode 1" of port "opt_a1" of component "I13" refers to TE mode in 4.5. Parts of the developed code for ONA analysis

are shown in 4.6 and 4.7. The simulation results, which are generated in PSF format, will be automatically extracted after running the simulation and the results are shown in Fig. 4.3.

Code 4.6: "MakeModeTable" function: make an associate table using the value of "modes" property in the "HEADER" table

```
procedure(MakeModeTable(Mode)
        let((Output Outupts ModelTable)
                ModeTable=makeTable("ModeTable" nil)
                Outputs=parseString(Mode "/")
                foreach(Output Outputs
                        OutputModeSperated=parseString(Output
                            ";")
        ....
        ....
        ....
        )
```

Code 4.7: "Mode" function: extracts different modes associated to each selected port in ADE creates a family from them and plot them

```
procedure(Modes(specifier)
        let((WaveNameList WaveID (WaveNumber 1) FamStr Fam Wave
             WaveList Signal
                SignalwithMode ModeNames ModeTable Result
                    TimeDomainType (ModeNumber 1) (Session
                                    asiGetCurrentSession()))
                        Signal=buildString(parseString(
                            specifier "/") ":")
                        if(nth(0 results())=="ona-ona"
                                then
                                        Result="ona-ona"
                                        ModeTable=MakeModeTable
                                            (resultParam("modes
                                            " ?result Result))
                                else
                                        Result=Signal
                                        if(resultParam("modes"
                                            ?result Result)==
                                            nil
                                ...
                                ...
                                ...
```

As it was mentioned before, Cadence tools such as ADE and Result Browser cannot access the result unless there is a log file specifying the structure of the data generated and the relationship between the generated data and simulation types. This log file is generated using Design Result Log (DRL)

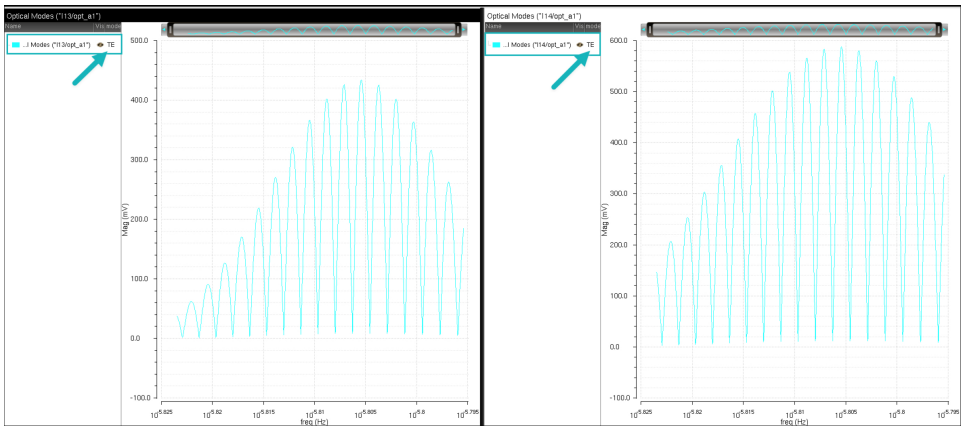


Figure 4.3: Simulation result of an ONA Analysis inside Cadence: simulation results are generated in PSF format

functions provided by Cadence. A part of this log file for ONA analysis is shown in Code 4.8. As you can see from Code 4.8, the format of a log file is also PSF.

Code 4.8: Log file generated by INTERCONNECT using Design Result Log (DRL) functions for an ONA analysis

```
1  HEADER
2  "PSFversion" "1.00"
3  "Log Generator" "drlLog rev. 1.0"
4  "simulator" "INTERCONNECT"
5  "version" "5.1.588"
6  "design" "// Generated for: INTERCONNECT"
7  "signalNameType" "INTERCONNECT"
8  "measdgt" 0
9  "ingold" 2
10 "sst2usecolon" 0
11 TYPE
12 "analysisInst" STRUCT(
13         "analysisType" STRING *
14         "dataFile" STRING *
15         "format" STRING *
16         "parent" STRING *
17         "sweepVariable" ARRAY ( * ) STRING *
18         "description" STRING *
19         )
20 VALUE
21         "ona-ona" "analysisInst" (
22         "ona"
```

```
23          "ona.ona"
24          ...
25          ...
26          ...
```

A few DRL functions that have been used for log file generation are mentioned in Table 4.1.

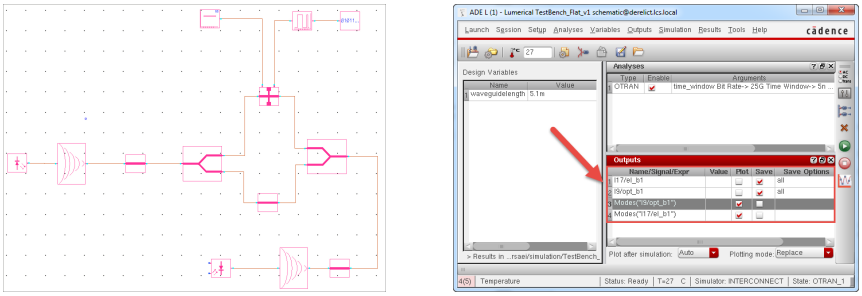
Table 4.1: A few DRL functions that are used to generate ONA log file

Function Name	Function Purpose
drLogEntry	Adds an entry to the log file (there need to be an entry for every data file created)
drLogAddPropFd	Adds a floating-point property (precision double)
drLogAddPropFd	Adds a floating-point property (precision long)

4.4.2 PSF for OTRAN Analysis inside ADE

Similar to an ONA analysis, a designer needs to specify elements whose simulation results needs to be saved by selecting elements' ports before running OTRAN analysis. The difference in OTRAN analysis is that for each selected port, INTERCONNECT generates a separate PSF file and the relation between these files is resolved using a log file. The reason that there are multiple PSF simulation files in OTRAN analysis is that when INTERCONNECT reads Cadence-generated netlist, it creates a separate component named "Probe" in the INTERCONNECT environment for each selected output in Cadence; INTERCONNECT then saves the time-domain simulation results for each probe in a separate file; subsequently, it would be also easier to generate separate PSF files for each selected output. Using the mentioned log file relationship between the generated simulation files and selected outputs can be resolved. Another difference between OTRAN and ONA, in terms of signal types, is that in OTRAN analysis there could be time-domain electrical signals that don't have any mode associated to them; subsequently, our software package should be smart enough to be able to distinguish between an electrical and optical simulation result/signal and only create a family from the optical results based on the modes associated to selected optical ports. The function "Mode", shown in Code 4.7, was developed to be able to handle both ONA and OTRAN analysis results and also distinguish between electrical and optical simulation results generated by INTERCONNECT for an OTRAN analysis. A schematic and its ADE

environment are shown in Fig. 4.4. Parts of the generated simulation results in PSF format are shown in Code 4.9 and Code 4.10.



(a) (b)

Figure 4.4: Cadence is set up for an OTRAN analysis: (A) Schematic, (B) ADE Environment

As you can see from 4.4b, two ports have been selected: one electrical and the other optical and also "Mode" function is used to make a family from different modes associated to an optical port and also to distinguish an electrical signal from an optical one. By running the simulation "Simulation → Netlist and Run ", simulation plots will automatically pop up as is shown in Fig. 4.5. As you can see from Fig. 4.5, "Mode" function automatically detected the optical port and creates a family from the associated modes of that port (in this case there is only one mode which is TE), and also it recognizes that the port "el_b1" of component "I17" is an electrical port and it doesn't need to create a family for that port. As mentioned before the simulation results are generated in separate files. A part of each file is shown in 4.9 and 4.10. Contrary to an optical port, there is no "modes" property for an electrical port as you can see in Code 4.9.

Code 4.9: PSF file i17_el_b1.tran generated for port "el_b1" of component "I17"

```
1 HEADER
2 "PSFversion" "1.00"
3 "BINPSF creation time" "1442948487"
4 "simulator" "INTERCONNECT"
5 "version" "5.1.588"
6 "design" "// Generated for: INTERCONNECT"
7 "analysis type" "tran"
8 "analysis name" "tran"
9 "analysis description" "Transient Analysis `tran': time = (0s
    -> 5ns)"
```

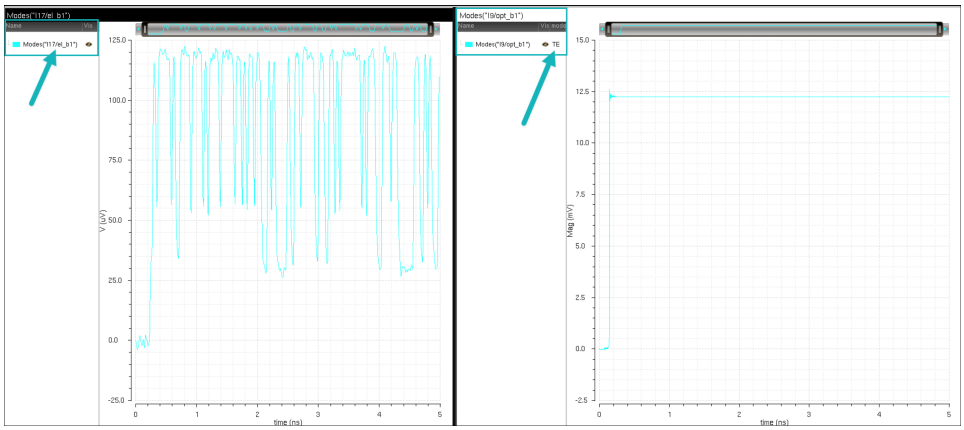


Figure 4.5: Simulation result of an OTRAN Analysis: simulation results are generated in PSF format

```
"start" 0
"stop" 5e-09
TYPE
        "sweep" FLOAT DOUBLE
        "V" FLOAT DOUBLE
SWEEP
        "time" "sweep"
TRACE
        "I17:el_b1" "V"
VALUE
        "time" 0
                "I17:el_b1" -7.056890792766487e-09
        "time" 2.44140625e-12
                "I17:el_b1" -4.899364141510132e-08
        "time" 4.8828125e-12
                "I17:el_b1" -1.583951856602623e-07
        "time" 7.324218750000001e-12
                "I17:el_b1" -3.244943643395414e-07
        "time" 9.765625e-12
        ...
        ...
        ...
```

Code 4.10: PSF file i9_opt_b1.tran generated for port "opt_b1" of component "I9"

```
HEADER
"PSFversion" "1.00"
"BINPSF creation time" "1442948487"
```

```
"simulator" "INTERCONNECT"
"version" "5.1.588"
"design" "// Generated for: INTERCONNECT"
"analysis type" "tran"
"analysis name" "tran"
"analysis description" "Transient Analysis `tran': time = (0s
    -> 5ns)"
"start" 0
"stop" 5e-09
TYPE
        "sweep" FLOAT DOUBLE
        "V" FLOAT DOUBLE
SWEEP
        "time" "sweep"
TRACE
        "I9:opt_b1:mode 1" "V"
VALUE
        "time" 0
                "I9:opt_b1:mode 1" (0 0)
        "time" 2.44140625e-12
                "I9:opt_b1:mode 1" (0 0)
        "time" 4.8828125e-12
                "I9:opt_b1:mode 1" (0 0)
        "time" 7.3242187500000001e-12
                "I9:opt_b1:mode 1" (0 0)
        "time" 9.765625e-12
                "I9:opt_b1:mode 1" (0 0)
        ...
        ...
        ...
```

Similar to an ONA analysis, Cadence tools such as ADE and Result Browser need a log file to be able to read the structure of simulation results. A part of the log file generated by INTERCONNECT using DRL for the OTRAN analysis is shown in Code 4.11. As you can see from 4.11, two "analysisInst" have been generated: one for port "el_b1" of component "I17" and one for port "opt_a1" of component "I9"; the reason for the creation of multiple PSF simulation files is explained in the first paragraph of this section.

Code 4.11: Log file created by using Design Result Log (DRL) functions for an OTRAN analysis

```
HEADER
"PSFversion" "1.00"
"Log Generator" "drlLog rev. 1.0"
"Log Time Stamp" "Tue Sep 22 12:1:27 2015"
"simulator" "INTERCONNECT"
```

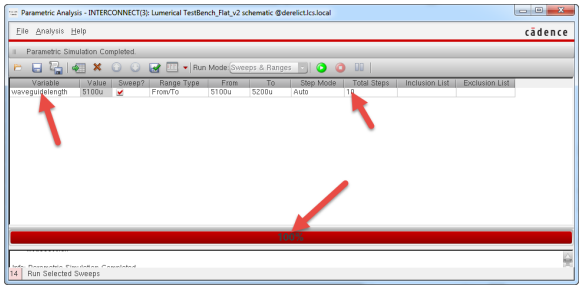
```
"version" "5.1.588"
"design" "// Generated for: INTERCONNECT"
"signalNameType" "INTERCONNECT"
TYPE
        "analysisInst" STRUCT(
        "analysisType" STRING *
        "dataFile" STRING *
        "format" STRING *
        "parent" STRING *
        "sweepVariable" ARRAY ( * ) STRING *
        "description" STRING *
        )
VALUE
        "I17:el_b1" "analysisInst" (
        "tran"
        "i17_el_b1.tran"
        ...
        ...
        ...

        "I9:opt_b1" "analysisInst" (
        "tran"
        "i9_opt_b1.tran"
        "PSF"
        ...
        ...
        ...
END
```

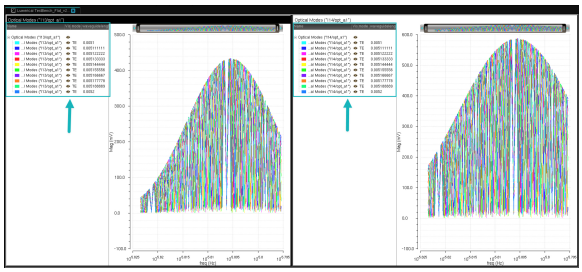
4.5 Advanced Analysis: Parametric Sweep

The data structure on which our software package is based gives us the capability of not only setting up parametric analysis efficiently (because the amount of coding to support it is minimum) but also all of the previously developed code/functions can be used without any change. The data structure that is used to store parametric simulation analysis results is based on distribution of simulation results in different directories, i.e., ADE will generate a separate netlist for any change in parameters that are being swept and simulation results will be stored under a unique directory named appropriately based on the value of the parameter. For example, assuming that we are changing the length of a waveguide and the number of parametric analysis is 10, then 10 separate directories will be created and each of the directories contains the simulation results for a specific value of that parameter. Parametric analysis setup of Fig. 4.2a and Fig. 4.4a is shown in

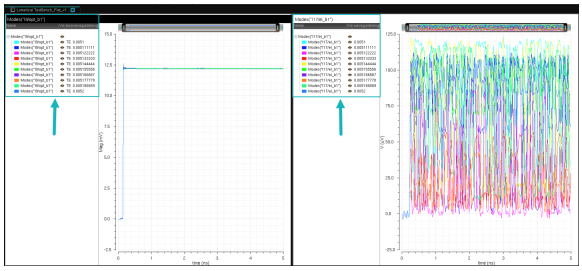
Fig. 4.6a. The simulation results of the ONA parametric analysis are shown in Fig. 4.6b and the simulation results of OTRAN analysis are shown in Fig. 4.6c.



(a)



(b)



(c)

Figure 4.6: Cadence setup for parametric analysis: (A) Parametric analysis setup, (B) Simulation results of ONA analysis, and (C) Simulation results of OTRAN analysis

Simulation results will pop up automatically after running the simulation ("Simulation→Netlist and Run"). As you can see from Fig. 4.6, the "Mode" function still make a family from the available modes of each selected port, and moreover ADE adds another parameter to this family called

waveguidelength which is the name of the parameter that is swept. This is exactly the structure we need to do post processing on the simulation results, i.e., see the change in the simulation results of an optical port by changing a design parameter. As an example, the eye diagram measurements of "Modes("I17/el_b1")" for different values of "waveguidelength" are done using parametric analysis and the results are shown in Fig. 4.7. It should be mentioned that if the selected port has different optical modes, the eye diagram will be plotted for each mode separately, but because the selected port is an electrical port, it doesn't have any mode associated to it and the only parameter that is swept is the "waveguidelength". The basic

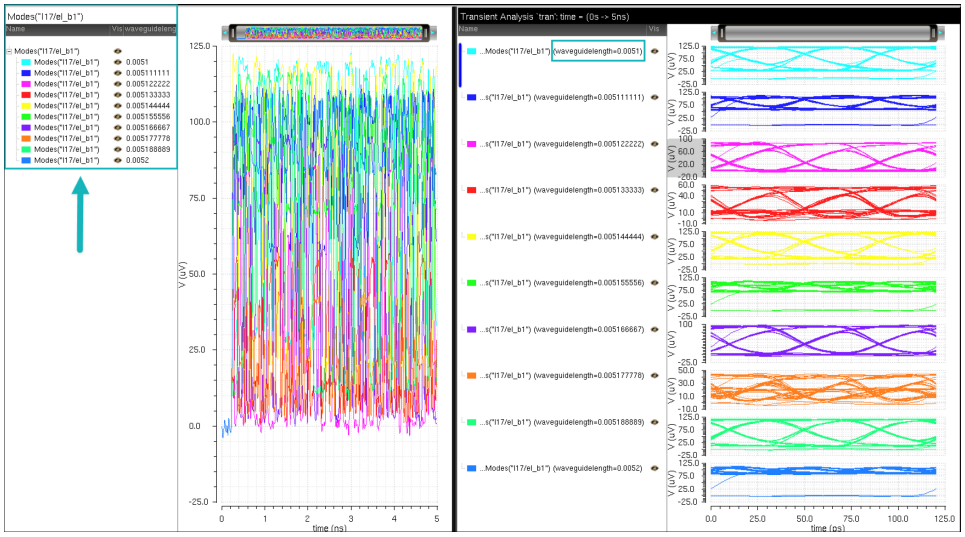


Figure 4.7: Eye digram measurements on the electrical port "el_b1" of component "I17"

framework that has been established using our software package provides the foundation for more advanced analysis such as Monte Carlo.

4.6 Conclusion

In this chapter, we discussed the data structure that is used in the generation of the optical simulation results from ONA and OTRAN analyses. The generated simulation results are formatted to be compatible with Virtuoso Visualization and Analysis (ViVA). Thus, a designer can visualize both electrical and optical results in ViVA. The main contributions of this chapter

are as follows:

- Presented an efficient methodology to format the simulation results generated from the INTERCONNECT ONA and OTRAN analyses, so they are seamlessly imported into ViVA (without any additional user interference).
- Developed and implemented the functionality to extract optical information such as optical modes (TE, TM, etc.) from the ONA and OTRAN simulation results.
- Developed and implemented the functionality to visualize the optical modes of an optical signal as a single family of graphs associated with that optical signal.
- Proposed and implemented a flow to support parametric analysis in the EPDA framework.

Chapter 5

Electro-Optical Sequential and Co-Simulation Evaluation

In the previous two chapters the implementation of the EPDA fromework in regards to the front-end design (schematic and simulation) has been discussed with many examples. This chapter is separated from the previous two chapters to evaluate the developed EPDA framework with respect to two classes of electro-optical simulation: sequential simulation and co-simulation.

Sequential simulation is used when an electro-optical circuit can be partitioned into electrical section and optical section without any feedback between these two sections. These circuits can be simulated sequentially by first simulating in the electrical domain and extract the required electrical signal, which are driving the optical section, and subsequently simulate the optical section with the extracted electrical signal as the electrical source. Using this method, the electrical loading effect of the optical section can be modelled and included in the electrical simulation as shown in Fig. 3.17.

Sequential simulation cannot address the shortcomings in the electro-optical simulation methodology when it comes to electro-optical circuits having electro-optical feedback. A simulation methodology needs to be developed that can simulate both electrical and optical partitions of an electro-optical circuits at each time step including the feedback effect. The solution, electro-optical co-simulation, that is proposed discussed at the beginning of Chapter 3 and is shown in Fig. 3.1.

In the rest of this chapter, both simulation methodologies, sequential and co-simulation that already developed and implemented in the previous two chapters, are examined and evaluated by examples.

5.1 Sequential Electro-Optical Simulation: A 5 Gbaud Pulse Amplitude Modulation (PAM4)

In this section, an optical PAM-4 is used to demonstrate the interoperability of Cadence and INTERCONNECT with respect to electro-optical simulation. Using the interface developed in the previous two chapter, two simulation engines, Spectre from Cadence and optical engine solver from INTERCONNECT, could communicate with each other. The design of optical section of the PAM-2 modulator is based on [133], and the design of the electrical section is based on a 45 nm CMOS 11M/2P Generic Process Design Kit (GPDK) provided by Cadence. The schematic of the electro-optical design is shown in Fig. 5.1. This electro-optical design could be simulated in a single run using OCEAN scripting; however, for clarification the co-simulation of this design is divided into three sequential simulation steps as follow:

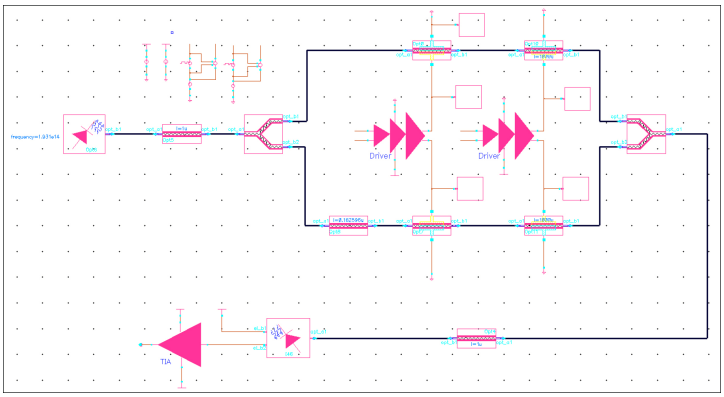
1. The electo-optical design will be simulated using Spectre. Spectre will only simulated the electrical aspect of the the design and the required results for the subsequent optical simulation will be save.

2. OTRAN analysis will be launched and simulated the optical aspect of the design by extracting the required signals from the Spectre simulation (as mentioned before these required electrical signal is specified using INTERCONNECTExport element inside schematic.IT should be mentioned that at this stage the electrical signal that are needed for the subsequent Spectre analysis such as the output current of the photodetector component will be extracted and saved.

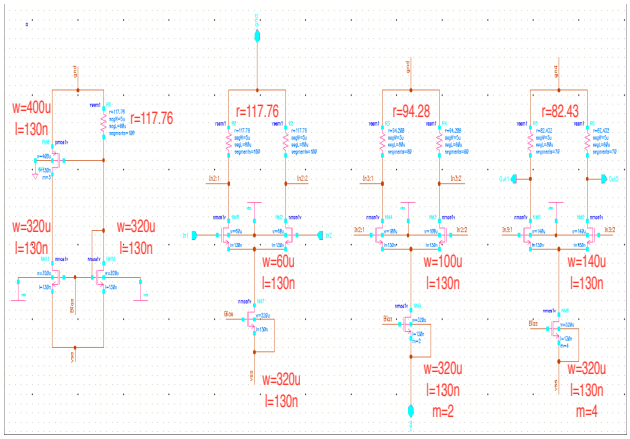
3. Spectre simulator will be launched and the final electrical simulation will be done including the output current of the photodetector. At this step, the output voltage of the TIA could be visualized and the required post-processing could be done.

5.1.1 (1) Electrical Simulation Using Spectre

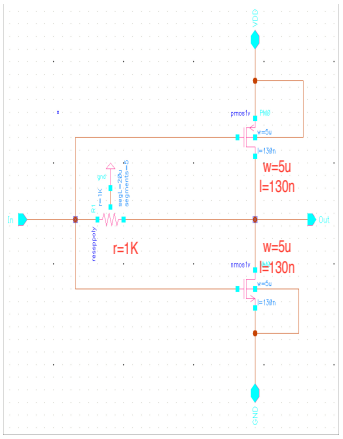
The ADE set-up of the first step and its simulation result are shown in Fig. 5.2. The result shown are the outputs of the first driver. The driver is design to provide differntial outputs swinging between 0 and -1. It should be considered that the biasing technique used in the design of the driver is a self bias design based on threshold voltage a PMOS transistor.



(a)



(b)

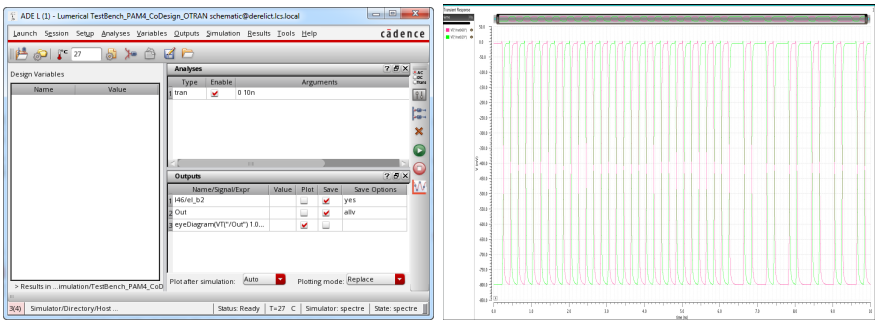


(c)

Figure 5.1: Cadence setup for parametric analysis: (A) Schematic of the electro-optical design, (B) Schematic of the CMOS driver, and (C) Schematic of the TIA

5.1.2 (2) Optical Simulation Using INTERCONNECT

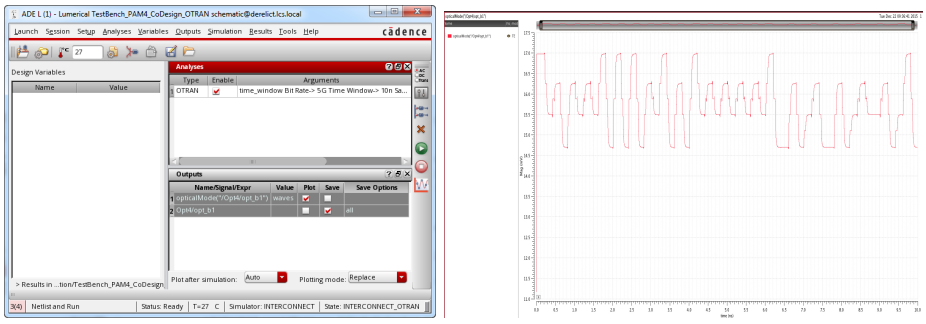
After the Spectre simulation, the electrical signals of CMOS drivers are saved and can be extracted by INTERCONNECT. It should be mentioned that the electrical simulation has been done considering the loading effect of the phase shifter components as demonstrated in the previous chapter. The INTERCONNECTExport components will guide INTERCONNECT engine to extract only the minimum number of electrical signals required for the optical simulation. In this design, at least 4 INTERCONNECTExport



(a) (b)

Figure 5.2: Spectre simulation result for the first step of Spectre → INTERCONNECT → Spectre sequence: (A) ADE set-up for a transient analysis, (B) Simulation result of the first driver's output

element is used to extract 4 output signals of two CMOS drivers and 1 INTERCONNECTExport element is used to specify the analog ground. The ADE set-up of this step and its simulation result are shown in Fig. 5.3. The waveform shown in Fig. 5.3 is the optical signal driving the photodetector, which is the optical signal coming out of the last waveguide element; as you can see this optical signal has a mode, TE, associated to it.

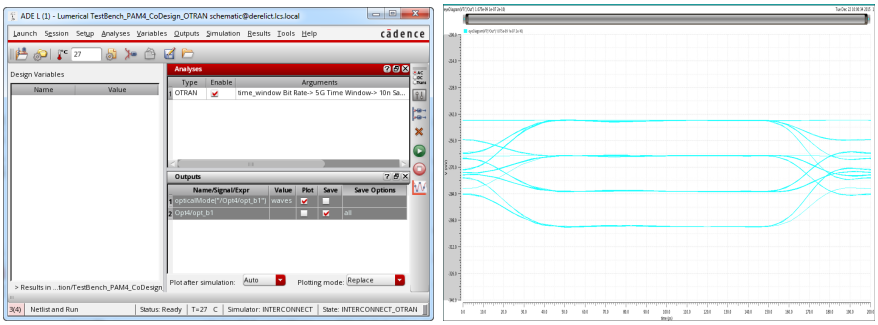


(a) (b)

Figure 5.3: INTERCONNECT simulation result for the second step of Spectre → INTERCONNECT → Spectre sequence: (A) ADE set-up for an OTRAN analysis, (B) OTRAN simulation result showing the TE mode of the optical signal driving the photodetector

5.1.3 (3) Electrical Simulation Using Spectre

The last step is to extract the photodetector's current, simulated using INTERCONNECT, and simulate the rest of the electrical section of the design, which is the TIA. The ADE set-up of the last step and its simulation result are shown in Fig. 5.4. It should be mentioned that the inherent bandwidth limitation of the photodetector could be modelled either in INTERCONNECT or as a subcircuit in Cadence; in this design, it is modelled in INTERCONNECT. The TIA is an inverting TIA that is designed to provide approximately $1K$ transconductance.



(a) (b)

Figure 5.4: Spectre simulation result for the last step of Spectre → INTERCONNECT → Spectre sequence: (A) ADE set-up for a transient analysis, (B) Simulation result showing the eye diagram of the TIA's output

5.2 Electro-Optical Co-Simulation Evaluation

The developed integration package from the previous two chapters is used at this stage to evaluate the electro-optical co-simulation. As shown in Fig. 3.1 and discussed at the beginning of Chapter 3, this methodology is based on communication between Cadence Spectre (electrical solver) and INTERCONNECT (optical solver) at each simulation time step. Spectre uses the recent Cadence Verilog-A feature to call and communicate with INTERCONNECT using Dynamic Link Libraries (DLL). It should be mentioned that sequential simulation is a subset of co-simulation. Having said that, two examples will be provided to demonstrate co-simulation methodology used for electro-optical circuits with and without feedback.

5.2.1 Electro-Optical Co-simulation: Opto-Electronic Oscillator (OEO)

The example that is used in this section is based on [134]. Electro-optical oscillators offer an improved spectral purity compared to their electronic counterparts.These oscillators benefit from the high quality factor provided by optical domain components to reduce the phase noise of the oscillator. The typical topology of this class of oscillators is shown in Fig. 5.5. In Fig. 5.5, the electro-optical feedback is shown using a red wire. The same topology

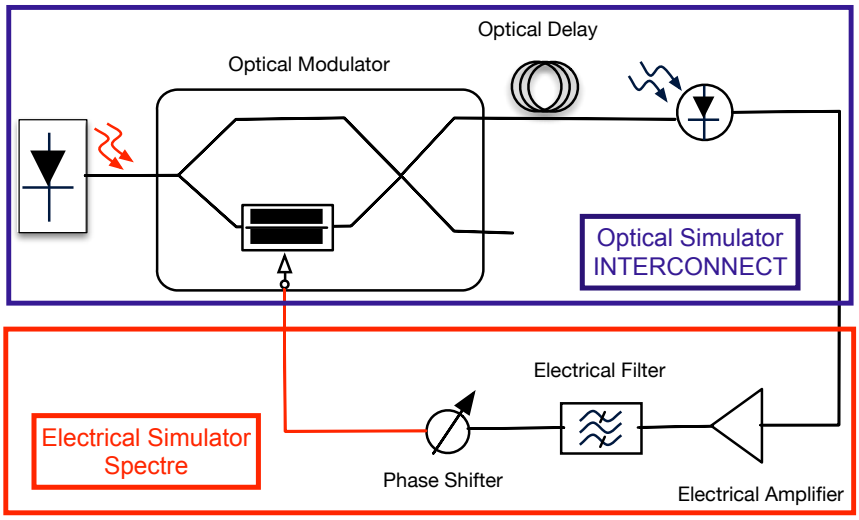
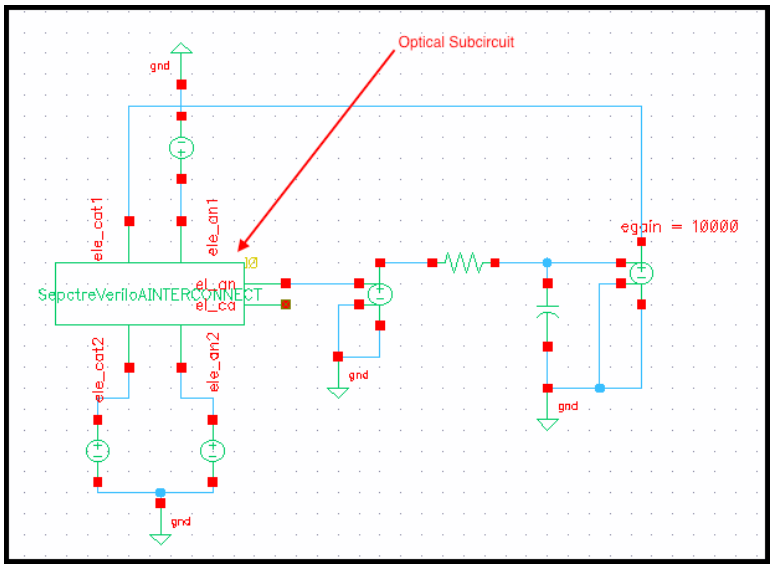


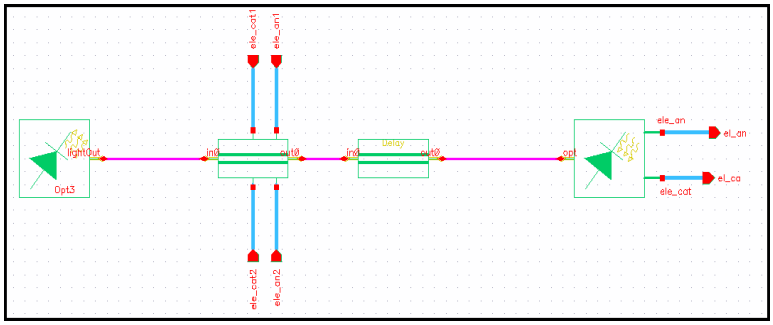
Figure 5.5: Structure of a typical optoelectronic oscillator [134]

has been implemented in Cadence as shown in Fig. 5.6. For the purpose of co-simulation using the proposed methodology discussed in Chapter 3, the following steps need to be performed:

1. As shown in Fig. 5.6, the electro-optical circuit needs to be partitioned into electrical section and optical subcircuits
2. A new property, named “INTERCONNECT”, needs to be added to the optical subcircuits. This will help INTERCONNECT netlister to distinguish between optical subcircuits and electrical sections
3. An OTRAN analysis needs to be specified in ADE for the top-level electro-optical schematic, Fig. 5.6a (Refer to Chapters 3 and 4)



(a)



(b)

Figure 5.6: A similar optoelectronic oscillator topology 5.5 has been implemented in Cadence to evaluate the electro-optical co-simulation: (A) Top-level schematic, (B) Optical subcircuit schematic

4. The top-level schematic needs to be netlisted by the integrated INTERCONNECT simulator. This will generate two files: an INTERCONNECT compatible netlist and a Verilog-A view of the optical subcircuit (Refer to Chapter 3 and 4)

5. A Spectre transient analysis needs to be specified in ADE for the top-level electro-optical schematic

6. The top-level electro-optical schematic can be simulated in the time domain using Spectre as the master solver and INTERCONNECT as the slave optical solver

5.2.2 Netlisting Top-Level Electro-Optical Schematic Using INTERCONNECT Netlister

In this section, the results of netlisting top-level electro-optical schematic using the proposed integrated INTERCONNECT netlister is discussed. The role of integrated INTERCONNECT netlister in this stage is to generate two files: (1) a textual netlist representation of the optical subcircuits that is compatible with INTERCONNECT netlist importer, and (2) a Verilog-A representation of the optical subcircuit.

The textual netlist representation is shown in Code 5.1 and its imported representation is shown in Fig. 5.7. As you can see from the textual netlist the OTRAN analysis statement has also been added in the generated netlist to specify the optical transient analysis' details.

Code 5.1: Generated Netlist by the integrated INTERCONNECT netlister

```
1 ............
2 .subckt SepctreVeriloAINTERCONNECT el_an el_ca ele_an1 ele_an2
      ele_cat1 ele_cat2
3     I2 ele_an1 ele_an2 ele_cat1 ele_cat2 net17 net05
          lcml_mod_mzi_1550 sch_x=0.041667 sch_y=-0.125000 sch_r
          =0 sch_f=F
4     Opt0 net05 net16 opticaldelay timedelay=2e-9 sch_x=0.479167
           sch_y=-0.041667 sch_r=0 sch_f=F
5     Opt3 net17 cw_laser power=1m phase=0 linewidth=0 frequency
          =193T sch_x=-0.895833 sch_y=0.041667 sch_r=0 sch_f=F
6     I0 net16 el_an el_ca lcml_pd_1550 sch_x=1.520833 sch_y
          =-0.145833 sch_r=0 sch_f=F
7 .ends SepctreVeriloAINTERCONNECT
8 * End of subcircuit definition.
9
10 * Library name: PhotonicsDesigns
11 * Cell name: SepctreVeriloAINTERCONNECTTestBench
12 * View name: schematic
13 XI0 net1 net2 net01 net02 net04 net03
      SepctreVeriloAINTERCONNECT sch_x=0.104167 sch_y=0.041667
      sch_r=0 sch_f=F
14
15 * Analysis Statement
16 * ------------------
17 .otran bitrate=2.5e10 simulation_input=time_window time_window
      =1.5e-8 num_of_samples=12000 monitor_data=save_to_memory
```

```
    multithreading=automatic .......
18 ......................
```

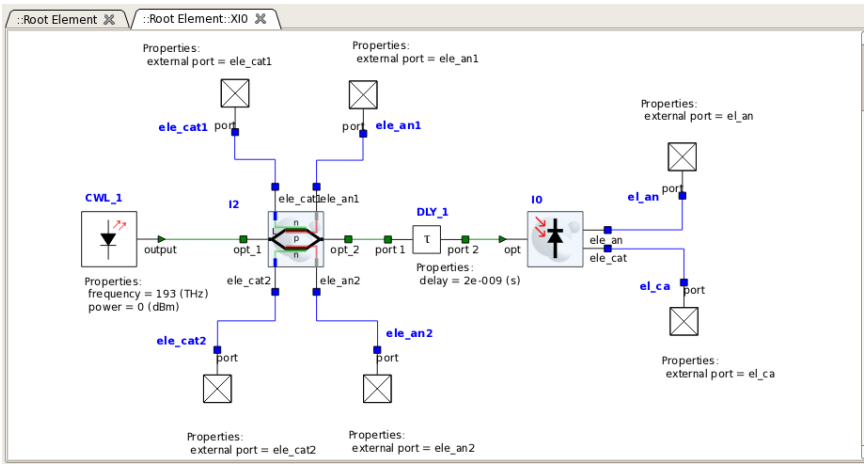


Figure 5.7: Importing the netlist generated in Code 5.1 showing the compatibility of the generated netlist with INTERCONNECT

While the optical subcircuits of the top-level electro-optical schematic is being netlisted, INTERCONNECT netlister will also generated their associated Verilog-A model automatically. The generated Verilog-A code for the optical subcircuit of the OEO oscillator shown in Code 5.2.

Code 5.2: Generated Verilog-A View for the optical subcircuit of the top-level electro-optical circuit

```
1 //VerilogA  PhotonicsDesigns, SepctreVeriloAINTERCONNECT
2 `include "constants.vams"
3 `include "disciplines.vams"
4
5 module SepctreVeriloAINTERCONNECT(el_an, el_ca, ele_an1,
      ele_an2, ele_cat1, ele_cat2);
6 input ele_an1, ele_an2, ele_cat2, ele_cat1;
7 output el_an, el_ca;
8 voltage el_an, el_ca, ele_an1, ele_an2, ele_cat1, ele_cat2;
9 integer PIC_ID;
10 import "CDS_VA_DPI" function integer PIC_INIT(integer
      Netlist_ID);
11 import "CDS_VA_DPI" function integer PIC_PUSH(integer PIC_ID,
      integer Port_Number, real Time, real Value);
12 import "CDS_VA_DPI" function real PIC_PULL(integer PIC_ID,
      integer Port_Number);
```

```
13 import "CDS_VA_DPI" function real PIC_RUN(integer PIC_ID, real
       Time);
14 analog begin
15          @(initial_step) begin
16                  PIC_ID=PIC_INIT(825031445);
17          end
18          PIC_PUSH(PIC_ID, 3, $abstime, V(ele_an1));
19          PIC_PUSH(PIC_ID, 4, $abstime, V(ele_an2));
20          PIC_PUSH(PIC_ID, 6, $abstime, V(ele_cat2));
21          PIC_PUSH(PIC_ID, 5, $abstime, V(ele_cat1));
22          PIC_RUN(PIC_ID, $abstime);
23          V(el_an) <+ PIC_PULL(PIC_ID, 1);
24          V(el_ca) <+ PIC_PULL(PIC_ID, 2);
25 end
26 endmodule
```

In the above Code 5.2, the DLL functions that are used to communicate with INTERCONNECT optical solver for each time step are PIC_PUSH, PIC_RUN, PIC_PULL, and PIC_INIT.

5.2.3 Running Time-Domain Analysis on the Top-Level Electro-Optical Circuit Using Spectre

Having both the netlist that can be recognized by INTERCONNECT and the Verilog-A model communicating with INTERCONNECT, it is now possible to run Spectre transient analysis on the top-level electro-optical circuit shown in Fig. 5.6a .

Fig. 5.8 shows INTERCONNECT environment in co-simulation mode while spectre pushing data into the optical solver and extract the optical simulation results. The simulation result is shown in Fig. 5.9.

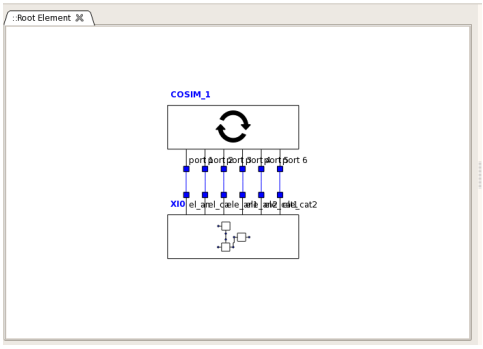


Figure 5.8: INTERCONNECT environment in co-simulation mode

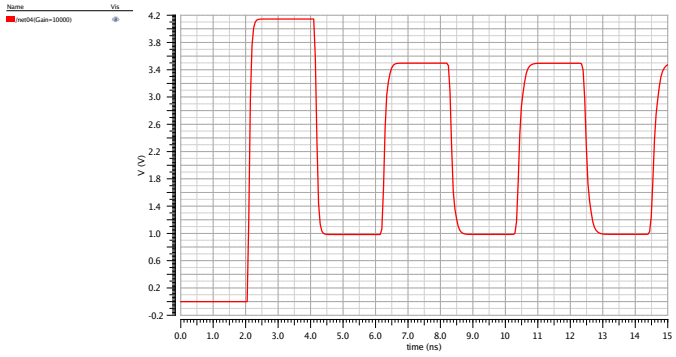


Figure 5.9: Co-simulation of the electro-optical top-level circuit shown in Fig. 5.6a (Gain of the electrical amplifier is set to $10,000$) for sustainable oscillation

5.2.4 Parametric Analysis and Co-simulation

Supporting parametric analysis is not only necessary in a complete EPDA methodology but also is required more advanced analyses such as statistical analysis. The developed co-simulation methodology and framework supports parametric analysis not only for the sequential simulation shown in previous chapter but also for co-simulation. To demonstrate that our EPDA framework supports parametric analysis, the gain of the electrical amplifier used in the electrical section of the electro-optical circuit (Fig. 5.6a) is defined as a design variable and is varied $1000 \rightarrow 10,000$. Changing electrical amplifier's gain will change the oscillator's loop gain and consequently if electrical amplifier's gain goes below a threshold, there wouldn't be a sustainable oscillation. Parametric simulation results shown in Fig. 5.10 demonstrate the same behaviour.

5.2.5 Validation of Simulation Result

In this section, the co-simulations results are validated (using Verilog-A to model the behaviour of the optical subcircuit). As shown in Fig. 5.7, if we can model the behaviour of the the laser source, mzi, and photo-detector using Verilog-A, then by just modelling a time delay, $2ns$, in Verilog-A the complete subcircuit can be modelled. Fig. 5.11a demonstrates how the laser source, mzi, and photo-detector are modelled in INTERCONNECT. Considering that in the Optoelectronic oscillator the feedback is applied to the "el_cat1", as shown in Fig. 5.6a, a ramp function is applied to the same

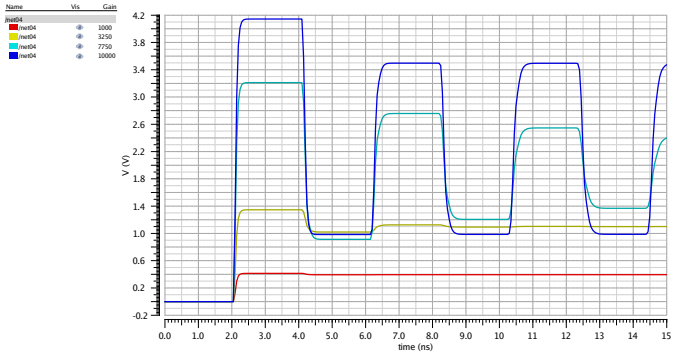
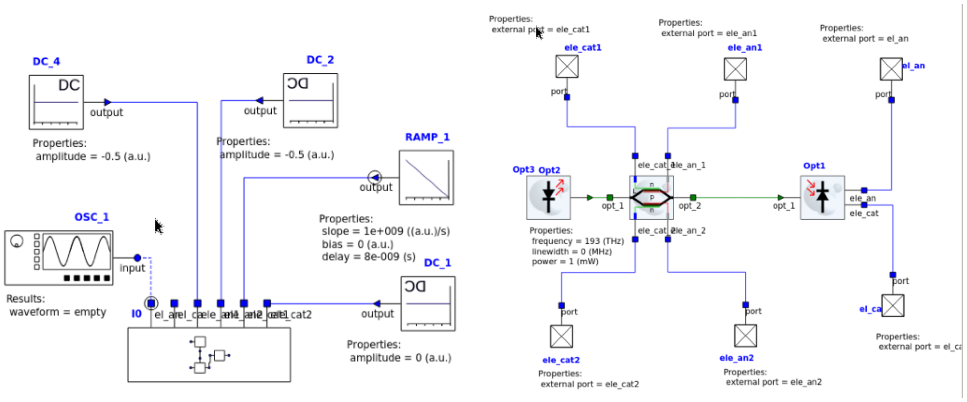


Figure 5.10: Co-simulation parametric analysis of the top-level electro-optical circuit shown in Fig. 5.6a (gain of the electrical amplifier is varied $1000 \rightarrow 10,000$)

port to evaluate the variation of photo-detector's output with respect to the change in "el_cat1". This is done in the INTERCONNECT simulator as shown in Fig. 5.11a. The simulation result is shown in Fig. 5.12. Using



(a) (b)

Figure 5.11: Evaluate the effect of change in the value of "el_cat1" on photo-detector's output: (A) Top-level schematic, (B) Expanded subcircuit

the simulation results, it is possible to come up with a simple behavioural model to relate the change in the voltage value of the "el_cat1" on the photo-detector's output as shown in Code 5.3.

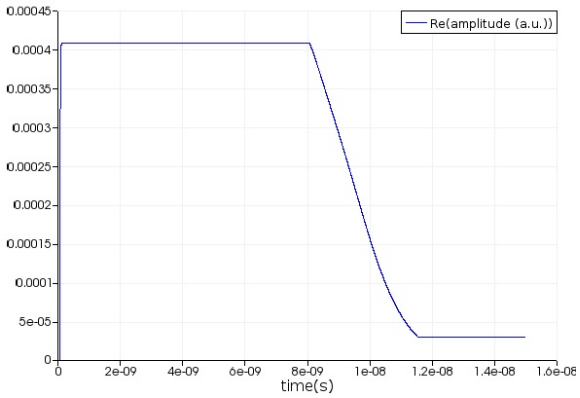


Figure 5.12: IINTERCONNECT Simulation results of the schematic shown in Fig.5.11a

Code 5.3: Behavioural Verilog-A mode to relate the change in the voltage value of "el_cat1" on the photo-detector's output

```
1  //VerilogA  OptoElectronicOscillator, MZI, veriloga
2  `include "constants.vams"
3  `include "disciplines.vams"
4
5  module MZI(in,out);
6  input in;
7  output out;
8  electrical in,out;
9  analog begin
10         if(V(in) <= 0)
11                 V(out) <+ 409.04e-6
12         else if(V(in) >= 3.4)
13                 V(out) <+ 2.96464e-5
14         else
15                 V(out) <+ -(409.04e-6 - 2.96464e-5)/3.535*V(in)
                       + 409.04e-6
16 end
17 endmodule
```

It should be mention the above Verilog-A model does not include the time delay between the change in the voltage of "el_cat1" and the photo-detector's output. This delay can be added to the delay value of the delay component. To get an approximate value for this delay, instead of applying a ramp function, one can apply a dc voltage to the same schematic (Fig. 5.11a) and then measure the delay in the change of the photo-detector's output. Fig. 5.13 demonstrates such simulation results. The approximate value of

delay is $0.06ns$.

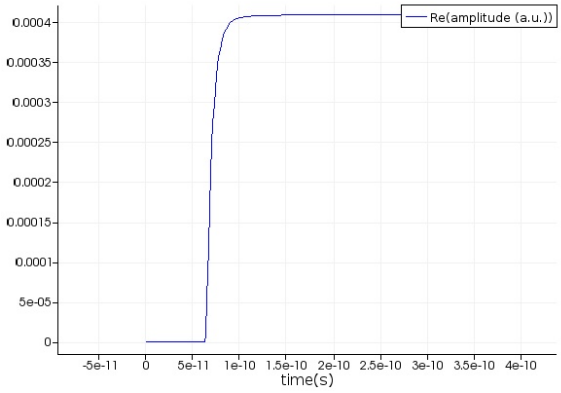


Figure 5.13: INTERCONNECT Simulation results of the schematic shown in Fig.5.11a: In this schematic, the ramp component is substituted with a $4V$ DC source

Code 5.4 shows the Verilog-A model for the delay line. As can be seen, the delay from "el_cat1" to the photo-detector's output is added to the original delay time of $2ns$; consequently, the total delay will be the addition of these two delays.

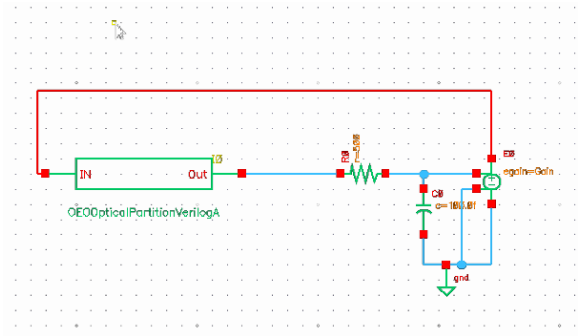
Code 5.4: Behavioural Verilog-A mode of the delay line including the delay associated with the change in the photo-detector's output with the change in the voltage value of "el_cat1"

```
1 //VerilogA  OptoElectronicOscillator, Delay, veriloga
2 `include "constants.vams"
3 `include "disciplines.vams"
4
5 module MZI(in,out);
6 input in;
7 output out;
8 electrical in,out;
9 analog begin
10                 V(out) <+ absdelay(V(in), 2.06e-9)
11 end
12 endmodule
```

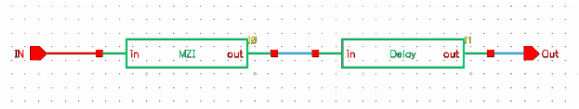
Comparison of Co-simulation and Verilog-A Simulation Results

To validate the co-simulation methodology with regards to the OEO oscillator, the simulation results of the co-simulation methodology is compared

with the simulation results where Verilog-A is used to model the optical subcircuit. The schematic and testbench for the simulation of OEO based on the Verilog-A modelling of optical subcircuits are shown in Fig. 5.14. Simu-



(a)



(b)

Figure 5.14: Simulate OEO using Verilog-A model of the optical subcircuit: (A) Top-level schematic, (B) Expanded subcircuit

lation results of two methodologies are shown in Fig. 5.15. The above figure

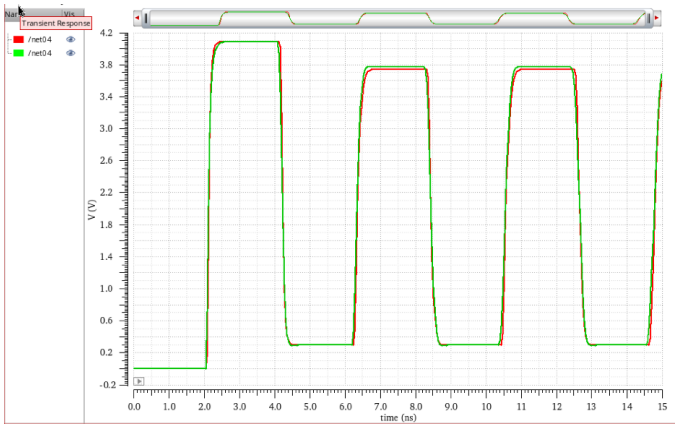


Figure 5.15: Comparison of the simulation results using co-simulation methodology and Verilog-A modelling.

demonstrates the validity of our co-simulation methodology for simulating a typical OEO oscillator.

5.2.6 Simulation Time Profile of the Co-Simulation Methodology

As shown in Code 5.2, the Verilog-A view of an electro-optical subcircuit does not model the behaviour of the subcircuit; it only provides an interface between the electrical simulator, namely, Spectre, and the optical simulator, INTERCONNECT. Verilog-A does not have a build-in mechanism to examine the execution time of different parts of the code. There is a $simparam("systime") function that returns the current system time. This system time's value is based on the number of seconds elapsed since the Epoch (1, Jan,1970) and it does not return the CPU clock cycle associated with the process which is needed to calculate the execution time.

To overcome the above mentioned limitation, a C function based on "clock_gettime()' is defined,"GetCurrentCpuTime()", that returns the CPU clock cycle for a process. This function is linked to Verilog-A using Direct Programming Interface (DPI) and is called as shown in Code 5.5.

Code 5.5: Verilog-A View for the optical subcircuit (Code 5.2) with added functionality to track the execution times. The added lines are indicated by "ADDED"

```
1  //VerilogA  PhotonicsDesigns, SepctreVeriloAINTERCONNECT
2  `include "constants.vams"
3  `include "disciplines.vams"
4
5  module SepctreVeriloAINTERCONNECT(el_an, el_ca, ele_an1,
       ele_an2, ele_cat1, ele_cat2);
6  input ele_an1, ele_an2, ele_cat2, ele_cat1;
7  output el_an, el_ca;
8  voltage el_an, el_ca, ele_an1, ele_an2, ele_cat1, ele_cat2;
9  integer PIC_ID;
10 real CpuTime1Run, CpuTime2Run, CpuTime1, CpuTime2,
       CpuTotalTimeRun, CputTotalTime; ADDED
11 import "CDS_VA_DPI" function integer PIC_INIT(integer
       Netlist_ID);
12 import "CDS_VA_DPI" function integer PIC_PUSH(integer PIC_ID,
       integer Port_Number, real Time, real Value);
13 import "CDS_VA_DPI" function real PIC_PULL(integer PIC_ID,
       integer Port_Number);
14 import "CDS_VA_DPI" function real PIC_RUN(integer PIC_ID, real
       Time);
15 import "CDS_VA_DPI" function real GetCurrentCpuTime(); ADDED
```

```
16 analog begin
17          @(initial_step) begin
18                  PIC_ID=PIC_INIT(825031445);
19          end
20          CpuTime1 = GetCurrentCpuTime();
21          PIC_PUSH(PIC_ID, 3, $abstime, V(ele_an1));
22          PIC_PUSH(PIC_ID, 4, $abstime, V(ele_an2));
23          PIC_PUSH(PIC_ID, 6, $abstime, V(ele_cat2));
24          PIC_PUSH(PIC_ID, 5, $abstime, V(ele_cat1));
25          CpuTime1Run = GetCurrentCpuTime(); ADDED
26          PIC_RUN(PIC_ID, $abstime);
27          CpuTime2Run = GetCurrentCpuTime(); ADDED
28          V(el_an) <+ PIC_PULL(PIC_ID, 1);
29          V(el_ca) <+ PIC_PULL(PIC_ID, 2);
30          CpuTime2 = GetCurrentCpuTime(); ADDED
31          CpuTotalTimeRun = CpuTime2Run - CpuTime1Run; ADDED
32          CputTotalTime = CpuTime2 - CpuTime1; ADDED
33          @(final_step) begin
34                 $debug("\n************\n Total CPU Time for
                       PICPUSH and PICPULL = %.6f \t Total CPU
                       time for PICRUN = .6f \n ************",
                       CputTotalTime-CputTotalTimeRun,
                       CputTotalTimeRun);ADDED
35          end
36 end
37 endmodule
```

As shown in Code 5.5, at the last time step of the time-domain simulation (@final_step), a debug message is printed in the simulation output window showing the execution times. The simulation output window is shown in Fig. 5.16. Fig. 5.17 shows the execution time of Verilog-A interface compared to Spectre's execution time. As can be seen, the bottleneck of the interface are the "PICPUSH" and "PICPULL" functions that are used to push data into and pull data off the optical simulator, INTERCONNECT.

5.2.7 Using Co-Simulation Methodology to Run Sequential Simulation

As mentioned, sequential simulation is a subset of co-simulation. This means that co-simulation could be used as the ultimate solution to simulate electro-optical circuits. However, considering that there are data exchange happening between two solvers, electrical and optical, at each time step, co-simulation shows performance degradation compared to sequential simulation for circuits without feedback. This is an area that needs further research not only to quantify this degradation but also to find methods to

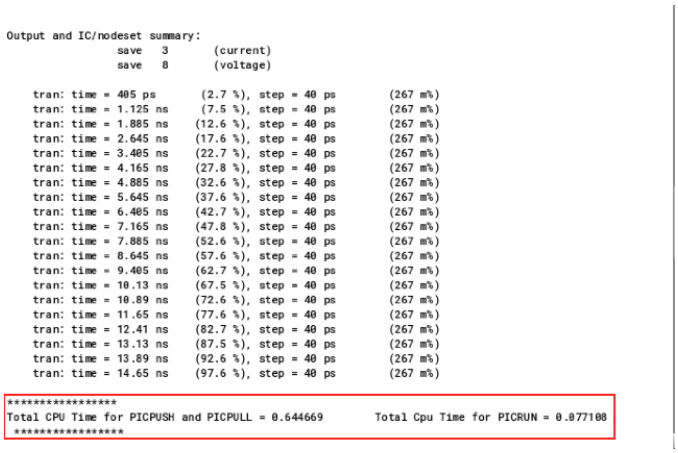


Figure 5.16: Simulation output window showing the total execution times of Verilog-A interface

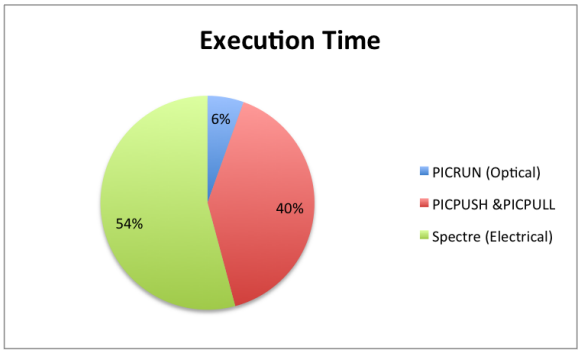


Figure 5.17: Execution time of different parts of Verilog-A interface compared to the Spectre's execution time

enhance the performance of the co-simulation as a substitute for sequential simulation.

The top-level electro-optical circuit for evaluating the use of co-simulation methodology to run sequential simulation is shown in Fig. 5.18. The optical subcircuit and its generated Verilog-A view are shown in Fig. 5.19a and 5.19b respectively. As mentioned previously, this view will be automatically generated by the integrated INTERCONNECT netlister. In the previous section, it was shown that the developed EPDA support parametric analysis for Co-simulation. As shown in Fig. 5.19c, co-simulation methodology used in place of sequential simulation also support parametric analysis.

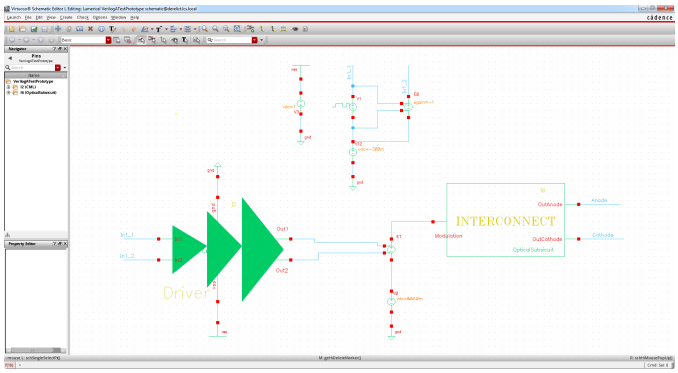
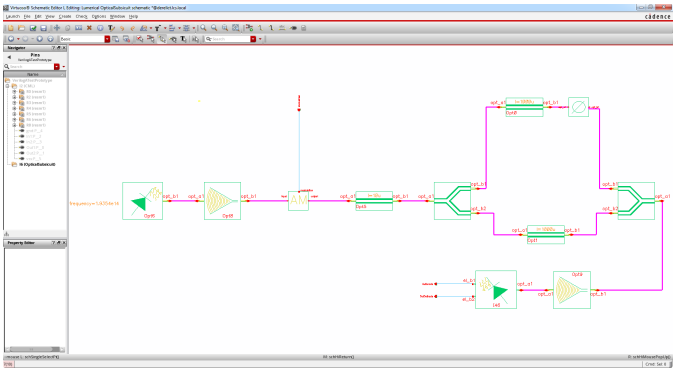


Figure 5.18: Electro-optical top-level circuit used to demonstrate that co-simulation can be used to do sequential simulation

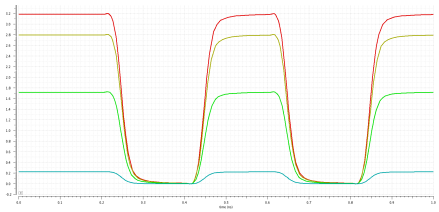


(a)

```
//Verilog-A for Lumerical, OpticalSubsicuit
 include "constants.vams"
 include "disciplines.vams"

module OpticalSubsicuit(Modulation, OutAnode, OutCathode);
parameter PhaseShift = 0;
input Modulation;
output OutAnode, OutCathode;
voltage Modulation, OutAnode, OutCathode;
integer PIC_ID;
import "CDS_VA_DPI" function integer PIC_Init(integer Netlist_ID);
import "CDS_VA_DPI" function integer PIC_PUSH(integer PIC_ID, integer Port_Number, real Time, real Value);
import "CDS_VA_DPI" function real PIC_PULL(integer PIC_ID, integer Port_Number);
import "CDS_VA_DPI" function real PIC_Run(integer PIC_ID, real ModulationValue, real PhaseShiftValue);
analog begin
    @(initial_step) begin
        PIC_ID=PIC_Init(276047788);
```

(b)



(c)

Figure 5.19: Co-simulation methodology used in a sequential electro-optical simulation: (A) Schematic view of the optical subcircuit , (B) Verilog-A view of optical subcircuit, and (C) Co-simulation parametric simulation's results (Phase shift of top branch in Fig. 5.19a is varied as a parameter)

5.3 Conclusion

The proposed PIC design flow provides designers with a unified and reliable integrated development environment inside Cadence, so they can design and simulate electro-optical systems. It supports parametric analysis, optimization, and statistical analysis. Electro-optical systems having feedback can also be designed and simulated inside this environment. It naturally resolve the challenges related to scalability of Verilog-A modelling by assigning an optical multi-mode port to each port of a photonic component and exploiting Parametrized Cells (PCell) capabilities to represent photonic components in layout and schematic.

Chapter 6

High Frequency Modelling and Design for a Photonic Process

The ever-growing demand for higher data rates has been driving the industry to come up with new ideas and technologies. Silicon photonics is one of the promising technologies that not only is compatible with already mature CMOS Very Large Scale Integration (VLSI), but also provide the required bandwidth for the higher data rates. Supporting higher data rates cannot be satisfied without accurate modelling of both active and passive devices. The modelling should be accurate both in the electrical and optical domains. As an example, an optical phase shifter that could be categorized as an electro-optical component should be modelled accurately both in electrical domain and also in the optical domain. In the electrical domain this modelling could be done by different modelling techniques such lumped components, S-parameter, Verilog-A, and in the optical domain Verilog-A and S-parameter could be used.

6.1 Inductor Modelling and Performance Enhancement Techniques in a Silicon Photonic Process

6.1.1 A Review on Performance Entrancement Techniques

Inductors are key components in many high-frequency and radio-frequency (RF) circuit blocks such as trans-impedance amplifiers (TIAs) voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), and mixers. Consequently, not only their proper modelling is crucial but also enhancing their performance such as increasing their self-resonant frequency (SRF) and quality factor (Q) is always desired. For example, as mentioned in [135], the phase noise and power consumption of LC-type oscillators are directly proportional

to the Q of the LC tank. Considering the fact that the Q of an LC tank is limited by the that of the lowest-Q component, on-chip inductors are the limiting factor in this regard. Thus, increasing the Q of the inductor is a key to a better performance.

Using micro-electro-mechanical system (MEMS) technologies, it is possible to enhance the Q and SRF of an inductor by reducing its parasitic capacitance to substrate as well as the substrate loss [136, 137]. However, most of these techniques are not compatible with a standard complementary metal-oxide semiconductor (CMOS) process. In [138], an inductor is implemented using micromachining, which is compatible with CMOS materials, and then the silicon below the inductor is removed and the inductor is suspended over the substrate; this will increase the Q factor of the inductor. Moreover, the dielectric between inter-turns also is removed to enhance the SRF. The implemented inductor is used in a VCO showing improvement in the VCO's performance [135]. In [139], the modelling of CMOS-compatible surface-micromachined suspended spiral inductors is discussed. It should be noted that most of the above techniques modify the structure around the inductor; however, the changing the physical properties of the inductor such as the metal thickness of its paths could also be exploited to enhance its performance [140]. Although physical modification is an effective technique to enhance the performance of an inductor, the way an inductor is excited, single-ended or differential excitation, can also change its performance. It is shown that at higher frequencies the substrate can favourably enhance both the Q factor and SRF [141].

Silicon photonics can also benefit from the inductor-based bandwidth enhancement techniques, e.g., nullifying the photodetector's capacitance and enhancing its operating bandwidth [142, 143]. 3-dimensional (3-D) integration of photonic and CMOS chips has introduced flexible integration solutions using these two technologies. Considering the fact that the cost per unit area of advanced CMOS processes used for high data rate communication is significantly higher than that of photonic processes, moving the inductors from the CMOS process to the photonic process not only can considerably reduce the cost of the overall photonic integrated circuit but also could lead to a tighter integration for more high-performance components. Inductors fabricated in a photonic process could also potentially benefit from the abovementioned micromachining techniques, such as substrate etching. Although these techniques have been used in CMOS process and their advantages have been demonstrated, their effectiveness in photonic processes has not been fully investigated. In this paper, we investigate the effect of similar enhancement techniques on the performance of inductors that are

fabricated in a photonic process.

6.1.2 Inductor Modelling in a Silicon Photonic Process

As is mentioned in the introduction chapter, the front end of a receiver has a grating coupler to couple the light into a chip and after that there is a photo detector to convert the light to current. A few design criteria that a CMOS designer should consider while designing the amplifier, which is used to amplify the current of this photodetector, are: 1) parasitic capacitance of the photodetector that has a significant effect on the speed of the optical receiver, less parasitic means potentially higher speed performance 2) noise performance of the photodetector, since the current noise is amplified with the signal, has direct effect on (S/N) performance of the receiver and consequently Bit Error Rate 3) high responsivity (η) of a photodetector needs a mechanism to protect the amplifier, which is used to convert current to voltage, from being overdriven [69].

The parasitic capacitance of a photodetector is the main cause of bandwidth limitation. Several bandwidth enhancement techniques have been proposed to compensate for the bandwidth limitation behaviour of a capacitance. The idea behind these techniques is to cancel a capacitive behaviour by an inductive behaviour. For instance, in the shunt-peaking technique an inductor is used in series with the load of a transistor; considering the fact that a transistor could be modelled as a voltage controlled current source, the output current of the transistor will charge the input capacitance of the next stage faster because of the inductive behaviour of the inductance in the series with the load. A similar idea is used in the design of a distributed amplifiers that the capacitances are included in the model of the transmission line and the inductive behaviour of a transmission line will compensate for the capacitive behaviour of capacitances. Having said that, the modelling of an inductor is a critical stage in the bandwidth enhancement techniques.

In particular, passive components, including inductors and transformers, are extensively used in communication circuits for both wireless and wireline applications. The main application of inductors (and their variants such as coupled-rings and transformers) is to improve the gain, and extend the operation bandwidth of the underlying circuit [144–146]. However, integrated inductors, generally being lossy components, can significantly deteriorate the performance of the system. In CMOS technology, the trend toward higher levels of integration tends to accelerate the degradation of inductor performance due to the top metal layers (where inductors are typically implemented) being located closer to the substrate. A recent deep-sub-micron

(DSM) CMOS option, the ultra-thick-metal (UTM) with low resistivity, ameliorates these effects, but this option calls for an extra cost, and also does not scale with the DSM technology. Given the available technology options and trade-offs between inductance (L), area, quality factor (Q), and self-resonance frequency (SRF) of the inductor, an accurate EM modelling technique to design and model all DSM effects for various 3-D structures, becomes an essential ingredient for todays integrated circuit design.

Traditionally, the modeling of integrated inductors to obtain their respective L and Q has been relatively time-consuming and required specific custom-developed tools, such as ASITIC or ADS Momentum, with various degrees of accuracy versus speed trade-off [147, 148]. The accuracy of these tools would also depend on the type and complexity of the subject structures. For example, ADS Momentum, as a "2.5-dimensional" (2.5D) electromagnetic (EM) simulation tool, employs pre-computed functions to simplify the EM simulation from 3D to 2D, which could pose modeling constraints if employed on a 3D inductor structure with multiple metal layers. Recently, a number of commercial tools, such as Helic, SONNET and Integrand EMX, have emerged that offer inductor PCells (parameterized custom-made layout and schematic cells) and are conveniently built into the mainstream IC design tools such as Cadence Virtuoso [149]. However, the relatively high cost, licensing restrictions, significant simulation time (required to model custom structures) and lack of analytical model limits their usage. Furthermore, due to the specific requirements of substrate files in CMOS technology, the majority of available tools are not suitable for inductor modelling in non-conventional process, e.g. photonic process.

As is mentioned above an inductor could be used to compensate the capacitive behaviour of photodetector. This inductor is fabricated in the CMOS process and consequently the photodetector whether wire-bonded or flip-chipped to the CMOS chip. Considering the fact that the cost per area of advanced CMOS processes used for high data rate communication is significant, moving the inductor from a CMOS process to a photonic process could significantly reduce the cost of overall electro-optical system. For example the academic cost of fabrication in a TSMC $65-nm$ CMOS process per mm^2 is 10 times that of an IME Silicon Photonics General-Purpose Fabrication Process [150]. Because photonic processes have been engineered for the fabrication of photonic components such as photodetectors, electro-optical modulators, waveguides, and etc. the fabricated inductor should be modelled accurately including the effect of substrate loss on the quality factor of the inductor.

In the following sections, the effect of the inductor on the bandwidth en-

hancement of a photodetector will be analysed. Two different fabrications of an inductor in a photonic process (IME) will be shown: one having silicon below and the other with silicon etched to reduce the loss and see the effect on the quality factor of the inductor. We leverage the extraction techniques developed for CMOS technology to accurately model the performance metrics of spiral inductors such as L, Q and SRF when implemented in the photonic process. The rest of the paper is organized as follows: In Section 6.1.3, the inductor structure is drawn, modelled, and analyzed inside HFSS; consequently, simulation results extracted from HFSS will be compared with the measurement results in Section 6.1.4. The extraction of inductor parameters such as inductance value, quality factor is discussed in Section 6.1.5; the effect of silicon removal on the performance of the inductor is covered.

6.1.3 Inductor Modelling in HFSS

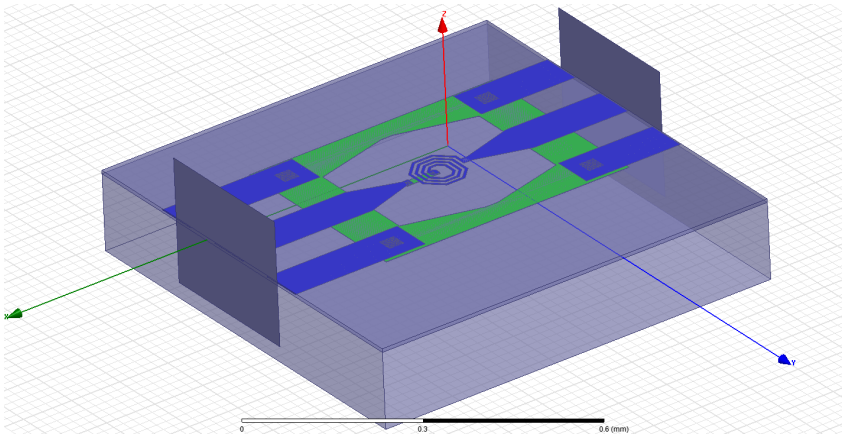
The structure of the inductor intended to be fabricated in a photonic process, IME (Silicon-on-insulator, $220 - nm$ top Si film, $2000 - nm$ buried oxide), is drawn in HFSS as shown in Fig. 6.1a. The inductor's shape and dimensions conform to the shape and dimensions of similar component from a $130nm$ CMOS fabrication process by IBM. Two wave ports are used to excite the proper mode of propagation on the GSG Coplanar Waveguide (CPW). Because of the boundary conditions associated to a wave port, its dimensions should be selected properly then the correct mode of the CPW could be excited. To make sure that the correct mode is propagating, the modal field distribution of the port is shown in Fig. 6.1b.

6.1.4 S-Parameters Simulation and Measurement Results

The fabricated inductor structure is shown in Fig. 6.2.

Two versions of the same inductor are fabricated in the IME photonic process: (a) In this version Fig. 6.2b, the silicon below the inductor isn't removed, (b) In this version Fig. 6.2c, the silicon below inductor is removed to see its effect on the performance of the inductor, especially the quality factor.

The measurement results saved directly from the VNA are shown in Fig. 6.3a. To be able to compare the simulation and measurement results, the measured S-parameters are saved and plotted in Matlab with simulation results from HFSS as shown in Fig. 6.3b.



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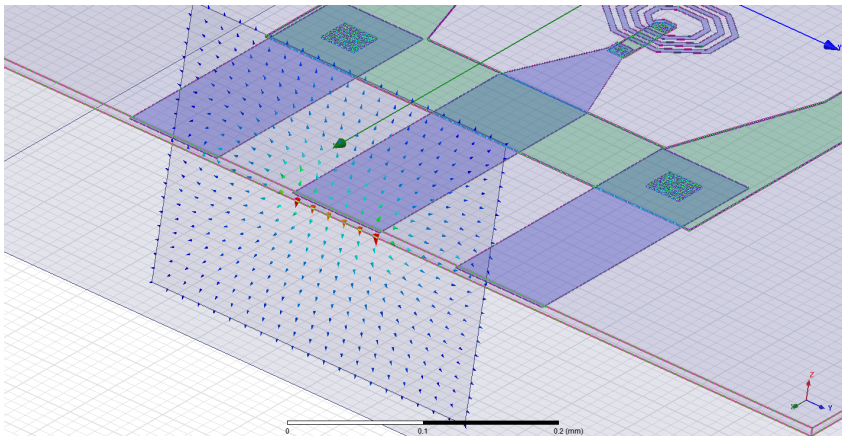
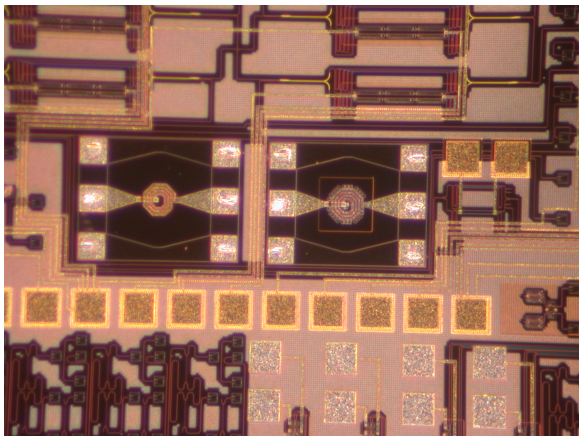
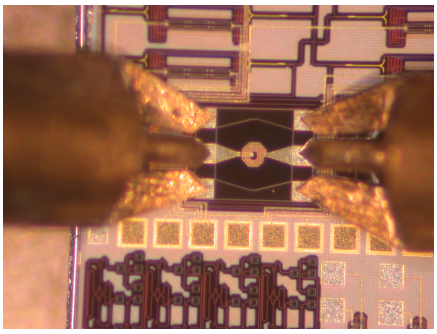


(b)

Figure 6.1: Indcutor modelling inside HFSS: (A) 3D structure, (B) Modal field distribution on a port



(a)



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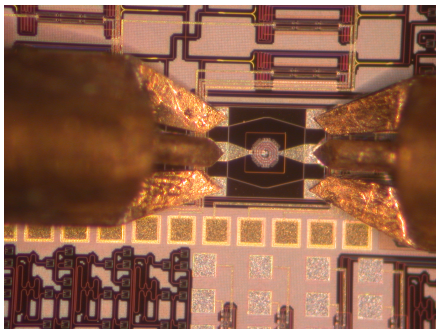


(c)

Figure 6.2: Fabricated inductors in the IME photonic process: (A) Two versions of inductor fabricated to see the effect of silicon removal on the their performance (B) Fabricated inductor that its below silicon isn't removed, (C) Fabricated inductor that its below silicon is removed

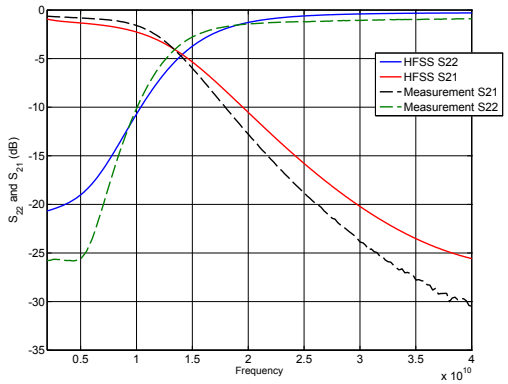
6.1.5 Extraction of The Inductor Parameters

Inductance value and quality factor of the inductor could be extracted using the Y-parameters [151]. The extraction equations are shown in 6.1.

$$L = Im(\frac{1/Y_{11}}{2\pi f}) \tag{6.1}$$

$$Q = \frac{Im(1/Y_{11})}{Re(1/Y_{11})} \tag{6.2}$$

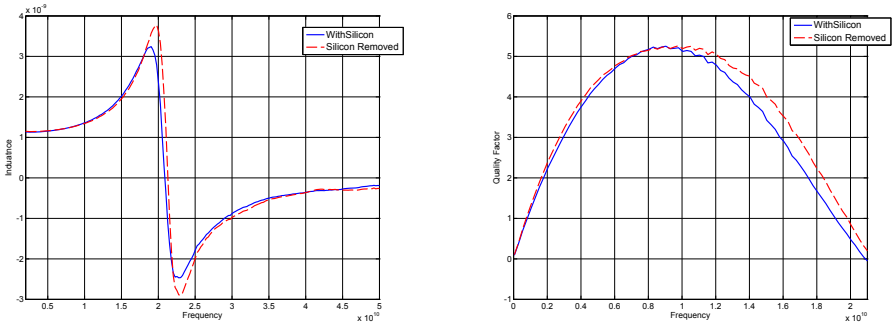
(a)



(b)

Figure 6.3: Comparison of the simulation and measurement results of the fabricated inductor in the photonics process : (A) Saved directly from VNA, (B) Measured results extracted from VNA and plotted with HFSS simulation results for comparison

Using Matlab RF toolbox, the above equations are implemented and the extracted inductance value and quality factor of the fabricated inductors are shown in Fig. 6.4. As can be seen from Fig.6.4a, the silicon removal doesn't have a significant effect on the inductance value, which is approximately $1.15nH$, and self-resonant frequency (SRF) of the inductors; however, it has



(a) (b)

Figure 6.4: Extracted value of inductance and quality factor for the fabricated inductors: (A) Inductance value, (B) Quality factor calculated in the frequency range where the component shows inductive behaviour ($freq \leq 22GHz$)

Table 6.1: The Effect of Silicon Removal on The Quality Factor of The Fabricated Inductors

Inductor	Quality Factor	Comment
With Silicon	2.9 @16 GHz	Loss increases due to eddy currents
Silicon Removed	3.52 @16 GHz	Increase of quality factor by 22%

a meaningful effect on the quality factor of the inductor especially in higher frequencies. This could be related to the fact that silicon removal reduces eddy currents and consequently the loss related to these currents which show themselves as reduction in the quality factor of the inductor. As is shown in Table 6.1, it could increase the quality factor by 22%.

It should be mentioned that in the above calculations, the effect of bonding pads have been eliminated by subtracting their Y-parameters from the Y-parameters of the device under test, the inductor. The bonding pads are fabricated separately in the same process and their Y-parameters are measured.

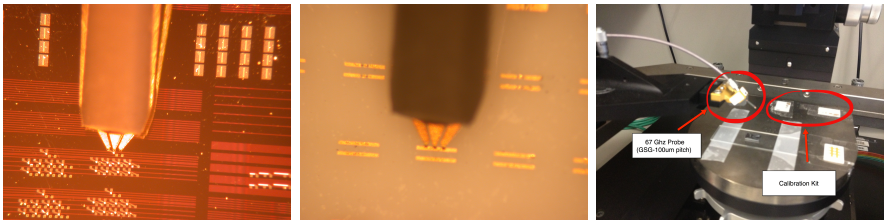
6.2 Electrical Modelling of a Ring Modulator

A ring modulator can be categorized as an electro-optical component in the design of telecommunication links. Not only do its optical properties need

to be simulated and modelled for the required performance of the communication link but also its electrical properties such as capacitance, resistance, and its inductance need to be modelled accurately, so its associated electrical driver can be designed based on the value of these components. In the coming sections the modelling methodology for a ring modulator is discussed. This methodology is based on measuring the scattering parameters of a ring modulator and changing value of hypothetical model parameters such that the measured scattering parameters are in good agreement with the simulated scattering parameters of the proposed model.

6.2.1 Measurement Set-up

The measurement set-up to measure S_{11} is shown in Fig. 6.5. parameter for the performance of a ring modulator. Some of the designed ring modulators



(a) (b) (c)

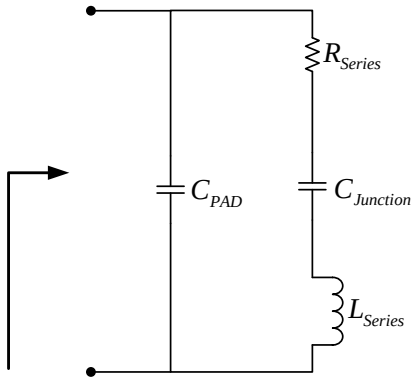
Figure 6.5: Measurement set-up for a ring modulator to measure S_{11}

have buried metals to change the temperature value of the structure and use temperature as a tuning The calibration process of measuring probes is crucial in accurate modelling of components that are required to model Radio Frequency (RF) and Microwave frequencies. One of the calibration steps, measuring short, for our GSG probes is shown in Fig. 6.5b. The measured S_{11} is saved using Touchstone format so that it could be imported into an EDA tool, in this case ADS, for further analysis.

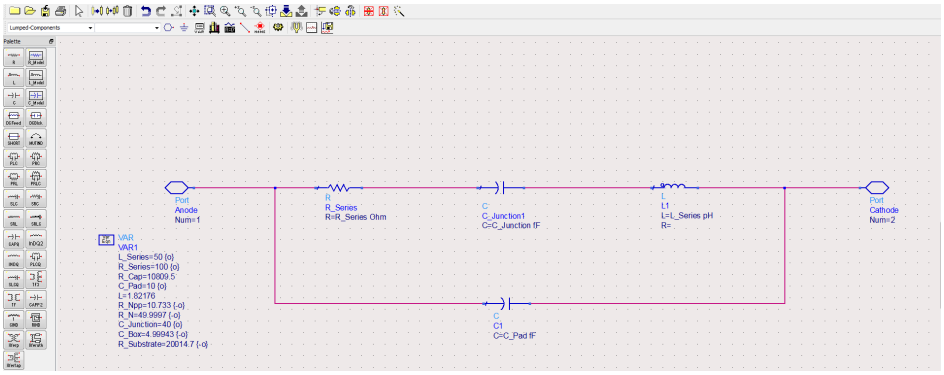
6.2.2 Modelling and Curve Fitting Using Advanced Design System (ADS)

After measuring the scattering parameter, a physical model should be proposed for the measured ring modulator. Based on the structure of the ring modulator, a hypothetical model is proposed as shown in Fig. 6.6. The validity of this model could be verified after curve fitting of the measured

results with the simulated results and evaluation of the value of the physical components proposed in the model. The ADS set-up is shown in Fig. 6.7.



(a)



(b)

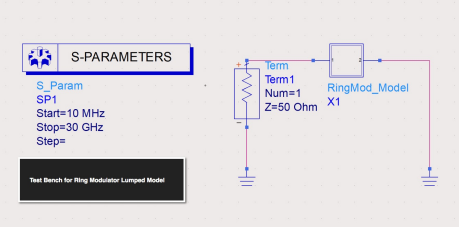
Figure 6.6: Proposed physical model and its equivalent schematic inside Advanced Design Systems (ADS)

As can be seen from Fig. 6.7, the lumped model shown in Fig. 6.6b is used to generate the simulation results. The simulation and measurement results are two inputs to two goal functions for optimization engine. These goal functions are the difference between the imaginary and real parts of the

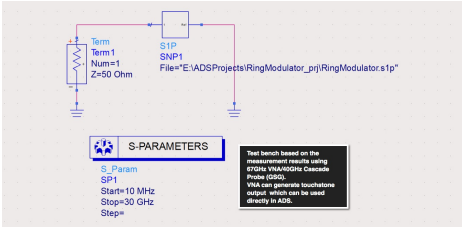
simulation and measurement results, as can be seen in Fig. 6.7c and (6.3).

$$real(TB2.S11 - TB1.S11) \longrightarrow TB2 : Measurement, TB1 : Simulation \tag{6.3}$$

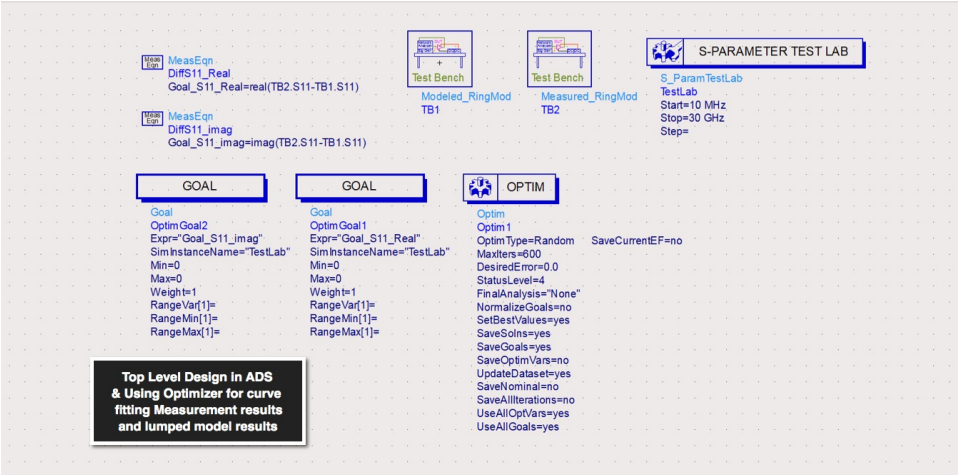
$$imag(TB2.S11 - TB1.S11) \longrightarrow TB2 : Measurement, TB1 : Simulation \tag{6.4}$$



(a) Ring modulator testbench



(b) Testnech based on the measurement results using 67 GHz VNA and 40 GHz cascade probe (GSG)



(c) Top-level design in ADS and using optimizer for curve-fitting of simulation and measurement results

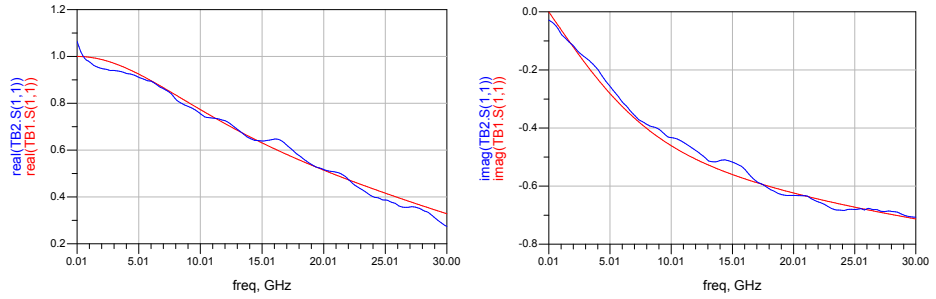
Figure 6.7: ADS set-up for curve-fitting simulation and measurement results using ADS optimization engine

Table 6.2: Extracted Value for Model Parameters

Model Parameter	Value
C_{PAD}	56 fF
$C_{Junction}$	41 fF
R_{Series}	225 Ω
L_{Series}	12 pH

6.2.3 Curve-Fitting Results and Component Value Extraction

The values of C_{PAD}, $C_{Junction}$, R_{Series}, and L_{Series} have been swept by the optimization engine and their final values that minimize the goal function will be extracted by the optimization engine. The final results of the optimization are shown in Fig. 6.8. The extracted value for the model parameters are shown in Table 6.2.



(a) Real value of S_{11}, $TB1$ is simulation results and $TB2$ is measurement results

(b) Imaginary value of S_{11}, $TB1$ is simulation results and $TB2$ is measurement results

Figure 6.8: Optimization results based on the defined goal functions (6.3).

6.3 25 Gbps CMOS Driver designed in 130-nm IBM Process

As mentioned in Section 2.2.3, the electrical driver has a significant role in the design of the overall optical communication link. In this section, a topology of a CMOS driver designed to driver an optical ring modulator with $3V_{pp}$ differential signal is discussed. Four of these driver could be used for a $100Gbps$ Wavelength Division Multiplexing (WDM) communication

link.

6.3.1 Topology of The CMOS Driver

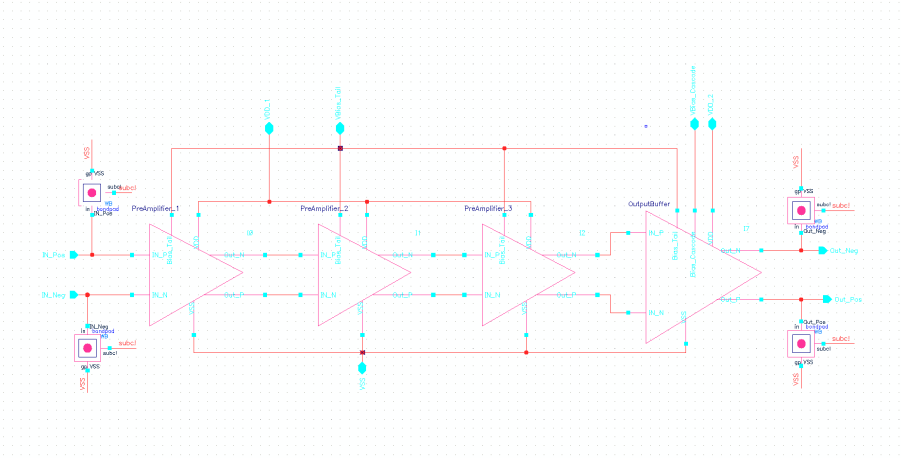
The schematic of one of the drivers is shown in Fig. 6.9. As shown in Fig. 6.9a, there are a few pre-amplifier stages, Fig. 6.9b, and there is a final output buffer, 6.9c. The pre-amplifier stages are used to gradually build enough driving voltage to switch the last output stage of the driver. Because the voltage variation of the output buffer is more than the withstanding voltage of a single NMOS transistor then a cascode structure is used with the top transistors having thick oxide to protect them from breaking. It should be mentioned that inductive peaking has been used in all of the pre-amplifiers and also output buffer.

6.3.2 Post-Layout Simulation Results

The layout of the final design is shown in Fig. 6.10 having 4 of the designed CMOS drivers. The Post-Layout simulation results for 20 Gbps and 23 Gbps are shown in Fig. 6.11a and Fig. 6.11b; the simulation results show only one of the outputs of the output buffer and the differential signal will be the same waveform multiplied by 2.

6.4 Conclusion

In this chapter, electrical modelling of passive electrical and electro-optical components are discussed. It is shown that to be able to model the performance of passive electrical components such as capacitors and inductor, EM simulation is necessary. A methodology for modelling the electrical performance of a fabricated ring modulator is proposed. Another important conclusion of this chapter is about the feasibility of fabricating an inductor in a photonic process and reducing the overall fabrication cost of an electro-optical system. Fabrication measurements show that the performance of the inductor could be enhanced by silicon-etching techniques aiming to reduce the loss relevant to eddy currents.



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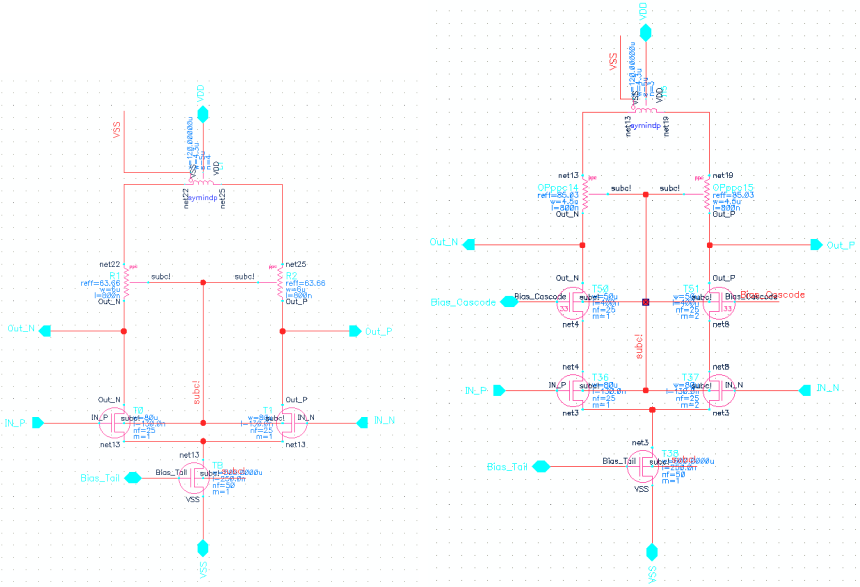


(b) (c)

Figure 6.9: Topology of a 25 Gbps CMOS driver, $3V_{pp}$, designed in a $130-nm$ IBM RF CMOS process: (A) Overall topology , (B) a Pre-amplifier topology, (C) Output buffer topology

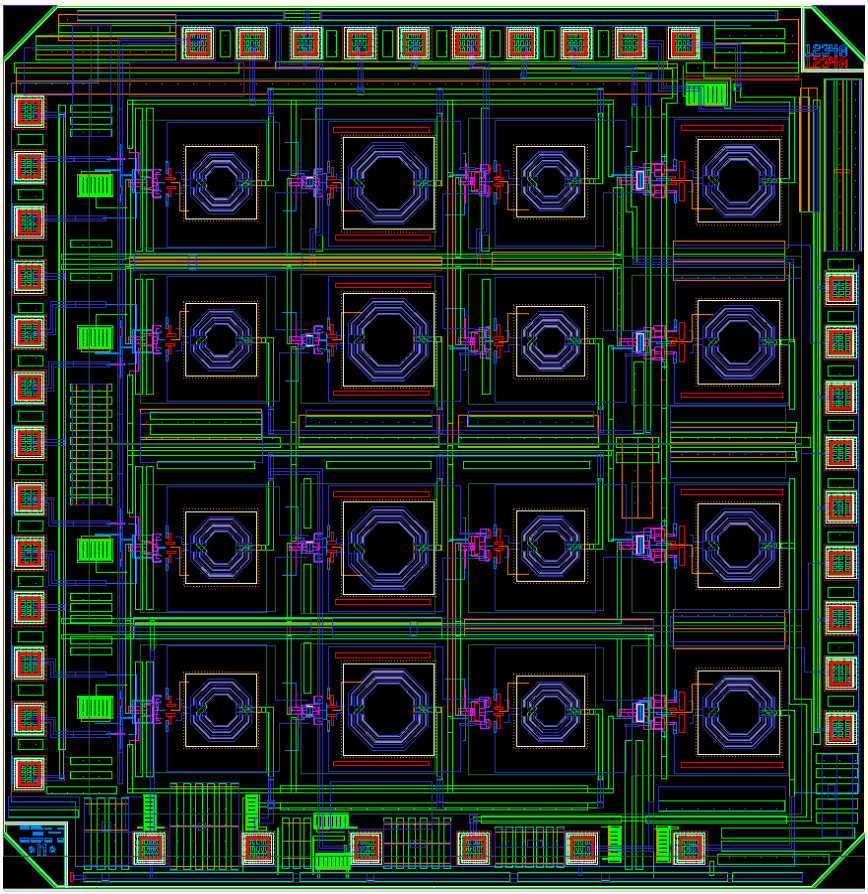
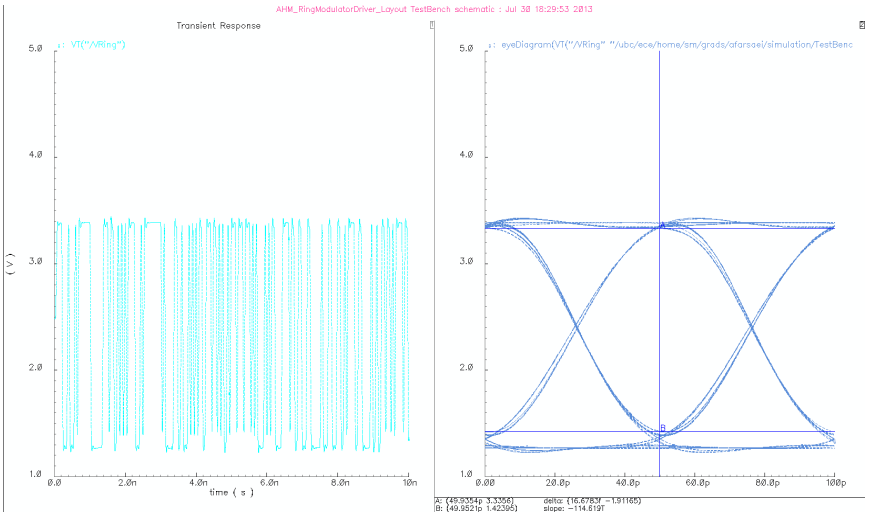


Figure 6.10: Final layout of 25 Gbps $3V_{pp}$ CMOS drivers. There are four of them for a 100 Gbps WDM system



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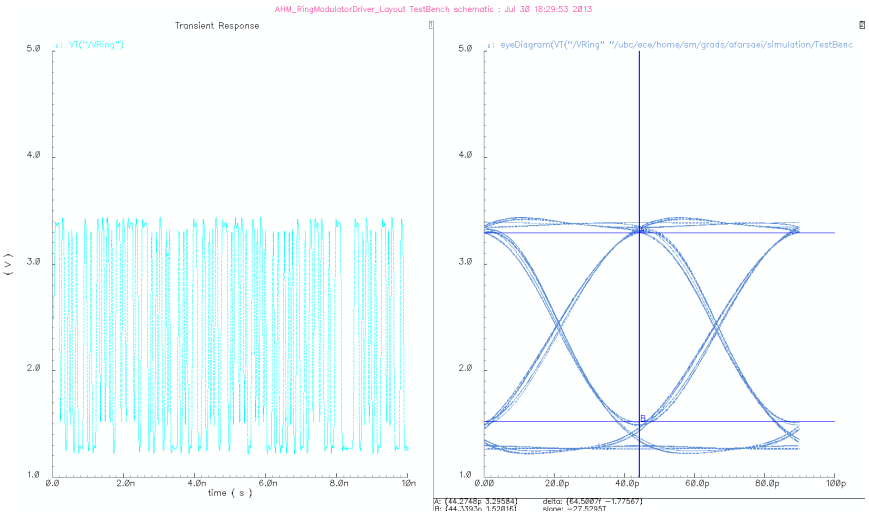


(b)

Figure 6.11: Post-layout simulation showing approximately 3.4 V_{pp}: (A)20 Gbps, (B)23 Gbps

Chapter 7

An Effective Approach in the Analysis of Nonlinear Circuits

In practice, communication systems consist of many building blocks that are nonlinear in nature, including low-noise amplifiers (LNAs), mixers, and power amplifiers (PAs). Thus, the simulation techniques that are used for analysis and design of such circuits should be able to predict the behaviour of the system in the presence of these nonlinearities. One of the well-established methods for simulating nonlinear circuits is harmonic balance analysis (HBA). Although this is a fairly robust and fast technique and is incorporated in many computer-aided design (CAD) tools, its convergence is not guaranteed if the starting value is not properly chosen. In this paper, we present an approach based on the harmonic input method of Volterra series for calculating the starting value for HBA. To show the effectiveness of the proposed method, an example circuit is considered and it is shown that by applying this method an otherwise non-convergent HBA simulation can converge. Also, effectiveness of different Volterra kernels is examined, and it is shown that in the proposed method evaluation of all Volterra kernels is not required and thus, the memory usage and simulation time of the proposed technique can be optimized.

7.1 Introduction to Analysis Methods of Nonlinear Circuits

There are different analysis methods that can be applied to nonlinear circuits such as Large-Signal Scattering Parameters, Volterra Series and Transient Analysis. These analyses can be categorized into two broader groups: Time-Domain Analysis and Frequency Domain Analysis. The Large-signal scattering parameters and harmonic balance methods are frequency domain analyses. Large-signal scattering parameters method is based on measuring

a set of two-port parameters of a nonlinear circuit, usually S-parameter, considering the fact that the excitation levels are large-signal, and consequently by changing the excitation level the two-port parameters will be changed. This technique could be useful in circuits that are not strongly nonlinear. Transient analysis is included in the time-domain analysis technique. This is a technique that could be used for low frequency and digital analyses; however, it is not suitable for microwave circuits on one hand since these circuits have both small and large time constants that make finding their steady-state response very time consuming; and on the other hand, it is not well suited for the components that are characterized in a frequency domain such as transmission lines with dispersion. Harmonic balance and Volterra series methods are frequency domain methods that are used for different types of nonlinear circuits. Harmonic balance is mostly used for strongly nonlinear circuits and Volterra series is used for weakly nonlinear circuits. Both of these methods could be applied to nonlinear circuits with non-commensurate frequencies. The assumption in the rest of this chapter is the quasistatic assumption, i.e., the charge of a capacitor only depends on the value of the instant voltage across it and the same concepts apply to the value of flux and voltage for an inductor and a resistor.

It should be mentioned that Volterra series analysis is not limited to electrical circuits and it can also be used in optical circuits. For example, Volterra series is used in [152] to derived a closed form expression for harmonic and intermodulation distortions. In [153], Volterra series is used to to derive distortion and cross modulations in erbium-doped fiber amplifiers.

7.2 Nonlinear Modeling of Lumped Elements Under Quasistatic Assumption [154]

Nonlinear lumped elements broadly can be divided into voltage controlled and current controlled elements. Having said that, each nonlinear element can be characterized either by its large signal nonlinear performance or by its incremental small signal performance. For example, in Fig. 7.1, the nonlinear characterization of a nonlinear resistor is shown. The large signal characterization is the relationship between the voltage across the resistor with respect to the current passing through it, and the incremental small signal model is the first order term of the Taylor series expansion of the large signal characterization around a specific current point. Using multi-index notation, a Taylor series expansion of a multi-variable function could be defined based on the following theorem.

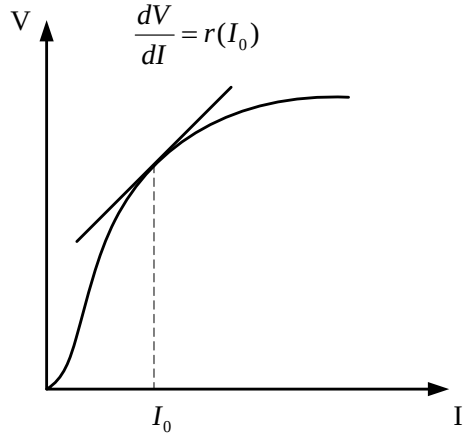


Figure 7.1: Nonlinear characterization of a nonlinear resistor with its first order approximation around its bias point

Theorem 1 *Suppose* $f : \mathbb{R}^n \longrightarrow \mathbb{R}$ *is of class* C^{k+1} *on a convex open set* S*. The Taylor series expansion around a point* $a \in S$ *and* $a + h \in S$ *can be written as:*

$$f(a+h) = \sum_{|\alpha| \leq k} \frac{\partial^\alpha f(a)}{\alpha!} h^\alpha + R_{a,k}(h) \tag{7.1}$$

and the remainder could be derived either using integral form or Lagrange's form, its Lagrange's form is as follow:

$$R_{a,k}(h) = \sum_{|\alpha|=k+1} \partial^\alpha f(a+ch) \frac{h^\alpha}{\alpha!} \quad for\ some\ c \in (0,1) \tag{7.2}$$

Based on Theorem 1, if the large signal nonlinear characterization of a nonlinear element is smooth enough, which is the case for a broad range of electronic elements, then it could be linearized around its bias point. For example, a nonlinear conductance, I as a function of V, can be modelled around its bias point by its Taylor expansion and consequently it can be represented by voltage controlled current sources as shown in Fig. 7.2. Because the incremental modelling of a nonlinear element is important in the Volterra series modelling and simulation, an example is shown in Fig. 7.3

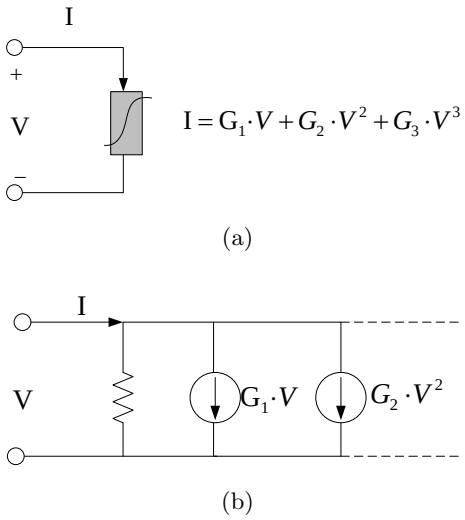


Figure 7.2: Using substitution theorem to replace the voltage controlled nonlinearities with nonlinear current sources

and Equation 7.6.

$$Large\ Signal\ Modelling : I = f(V) = G_1 V + G_2 V^2 + G_3 V^3 + \cdots \quad (7.3)$$

$$Taylor\ expansion : f(V_0 + v) = f(V_0) + \frac{\partial f}{\partial V}|_{V=V_0} \cdot v + \frac{1}{2!}\frac{\partial^2 f}{\partial V^2}|_{V=V_0} \cdot v^2 + \frac{1}{2!}\frac{\partial^3 f}{\partial V^3}|_{V=V_0} \cdot v^3 + \cdots \quad (7.4)$$

$$Incremental\ Current : i = f(V_0 + v) - f(V_0) = \frac{\partial f}{\partial V}|_{V=V_0} \cdot v + \frac{1}{2!}\frac{\partial^2 f}{\partial V^2}|_{V=V_0} \cdot v^2 + \frac{1}{3!}\frac{\partial^3 f}{\partial V^3}|_{V=V_0} \cdot v^3 + \cdots \quad (7.5)$$

$$Incremental\ Small\ Signal\ Modelling : i = g_1 v + g_2 v^2 + g_3 v^3 + \cdots \quad (7.6)$$

It should be mentioned that it is possible for the nonlinear element to be controlled by different voltages, e.g. drain current of a CMOS transistor; this also can be modelled by a multi-dimensional Taylor series expansion.

Large signal nonlinear modelling of a capacitance is also similar to a resistor; the only difference is that in the capacitance case the charge, instead of current, is controlled by voltage. Both the large signal and incremental modelling of a capacitance is derived in 7.10. It should be mentioned that

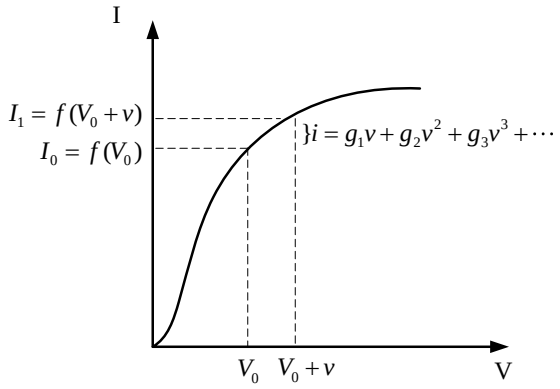


Figure 7.3: Incremental modelling of a nonlinear conductance that is used in Volterra series modelling and simulation

similar theory could be used for nonlinear inductors

$$Large\ Signal\ Modelling : Q = f(V) = Q_1 V + Q_2 V^2 + Q_3 V^3 + \cdots \quad (7.7)$$

$$Taylor\ expansion : f(V_0 + v) = f(V_0) + \frac{\partial f}{\partial V}|_{V=V_0} \cdot v + \frac{1}{2!}\frac{\partial^2 f}{\partial V^2}|_{V=V_0} \cdot v^2 + \frac{1}{3!}\frac{\partial^3 f}{\partial V^3}|_{V=V_0} \cdot v^3 + \cdots \quad (7.8)$$

$$Incremental\ Charge : q = f(V_0 + v) - f(V_0) = \frac{\partial f}{\partial V}|_{V=V_0} \cdot v + \frac{1}{2!}\frac{\partial^2 f}{\partial V^2}|_{V=V_0} \cdot v^2 + \frac{1}{2!}\frac{\partial^3 f}{\partial V^3}|_{V=V_0} \cdot v^3 + \cdots \quad (7.9)$$

$$Incremental\ Small\ Signal\ Modelling : i = \frac{dq}{dt} = q_1 \cdot \frac{dv}{dt} + q_2 \cdot v\frac{dv}{dt} + q_3 \cdot v^2\frac{dv}{dt} + \cdots \quad (7.10)$$

Coefficients of Taylor series expansion of Large signal modelling can be related to the coefficients of Taylor series expansion of small signal incremental

modelling as shown in Equations 7.11 and 7.12.

$$\textit{Nonlinear Resistors} \tag{7.11}$$
$$f(V_0+v) = f(V_0) + g_1 v + g_2 v^2 + g_3 v^3 + \cdots$$
$$G(V_0+v) = G(V_0) + \zeta_1 v + \zeta_2 v^2 + \zeta_3 v^3 + \cdots$$
$$g_1 = \zeta_0 \quad g_2 = \frac{\zeta_1}{2} \quad g_3 = \frac{\zeta_2}{3} \qquad \cdots$$
$$\textit{Nonlinear Capacitance} \tag{7.12}$$
$$f(V_0+v) = f(V_0) + q_1 v + q_2 v^2 + q_3 v^3 + \cdots$$
$$C(V_0+v) = C(V_0) + \gamma_1 v + \gamma_2 v^2 + \gamma_3 v^3 + \cdots$$
$$q_1 = \gamma_0 \quad q_2 = \frac{\gamma_1}{2} \quad q_3 = \frac{\gamma_2}{3} \qquad \cdots$$

7.3 Harmonic Balance Analysis

Harmonic balance analysis (HBA), also referred to as harmonic balance method (HBM), is one of the powerful techniques that not only can be used to find the steady-state response of a nonlinear circuit [154] but also can assist other simulation techniques to solve for a nonlinear phenomena [154],[155]. To calculate the solution of a nonlinear circuit using HBA, we need to solve a system of nonlinear equations having several variables; the engine for solving the HBA's nonlinear system of equations usually uses the Newton method for its convergence routine [154, 156]; In the Newton method a starting point is chosen, and then the solution is found by using an iterative procedure. Numerically this method converges quadratically provided that a sufficiently accurate starting value is chosen; otherwise, the solution may not converge [156, 157].

7.3.1 Harmonic Balance Method's Algorithm

The Harmonic Balance Algorithm is based on partitioning a circuit into linear and nonlinear sections as shown in Fig. 7.4. Linear circuit theory, such as multiport Z, Y, or S parameter, can be applied to the linear section, and the nonlinear section can be characterized by the large signal modelling of nonlinear elements as discussed in previous section (I/V or Q/V). Basically the assumption in Harmonic Balance Analysis is that the response of the circuit has reached a steady-state response and it could be represented by a finite number of harmonics of the input source; for simplicity we assumed that there is just one sinusoidal source in the circuit. Mathematically, the

voltage and currents at each port, which connects nonlinear and linear sections, can be expressed in the frequency domain. It should be mentioned that nonlinear elements have caused these voltages and currents to have harmonics of the input excitation. Generally speaking in nonlinear circuits having feedback, an infinite number of harmonics could be generated, but to be able to implement this method we need to truncate the number of harmonics to a specific number K. Partitioning the linear and nonlinear parts of a circuit and writing Kirchhoff's Current Law (KCL) for the connecting port between linear and nonlinear, a solution can be reached if the following Equation 7.13 is satisfied. In this equation, I refers to the current related to the linear partition of the circuit and $\widehat{I}$ refers to the current related to the nonlinear partition. The subscripts in Equation 7.13 refers to the port number and harmonic number. For example, $I_{1,1}$ is referring to the first harmonic of the current going through the linear part of port 1.

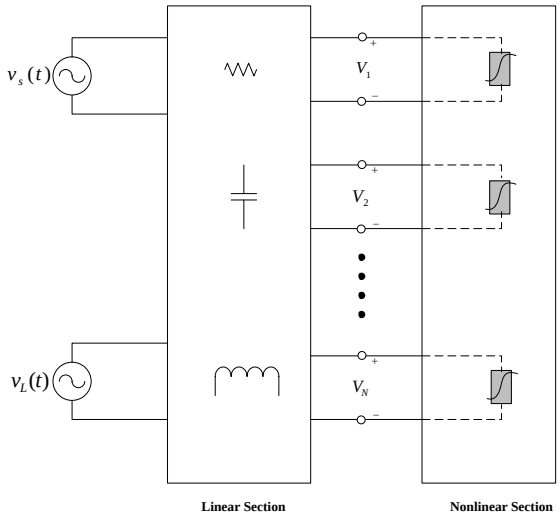


Figure 7.4: Partitioning of a nonlinear circuit into a linear and nonlinear sections for Harmonic Balance Analysis

$$\begin{bmatrix}[I_1]\\[I_2]\\[I_3]\\\cdots\\[I_N]\end{bmatrix} + \begin{bmatrix}\left[\widehat{I_1}\right]\\\left[\widehat{I_2}\right]\\\left[\widehat{I_3}\right]\\\cdots\\\left[\widehat{I_N}\right]\end{bmatrix} = 0 \qquad [I_1] = \begin{bmatrix}I_{1,0}\\I_{1,2}\\I_{1,3}\\\cdots\\I_{1,K}\end{bmatrix} \tag{7.13}$$

The equation for the linear section of the circuit can be written in a matrix form as shown in the following Equations (7.14).

$$\begin{bmatrix}[I_1]\\[I_2]\\\cdots\\[I_{N+1}]\\[I_{N+2}]\end{bmatrix} = \begin{bmatrix}[Y_{1,1}] & [Y_{1,2}] & \cdots & [Y_{1,N+1}] & [Y_{1,N+2}]\\[Y_{2,1}] & [Y_{2,2}] & \cdots & [Y_{2,N+1}] & [Y_{2,N+2}]\\[Y_{3,1}] & [Y_{3,2}] & \cdots & [Y_{3,N+1}] & [Y_{3,N+2}]\\\cdots & \cdots & \cdots & \cdots & \cdots\\[Y_{N,1}] & [Y_{N,2}] & \cdots & [Y_{N,N+1}] & [N_{1,N+2}]\\[Y_{N+1,1}] & [Y_{N+1,2}] & \cdots & [Y_{N+1,N+1}] & [Y_{N+1,N+2}]\\[Y_{N+2,1}] & [Y_{N+2,2}] & \cdots & [Y_{N+2,N+1}] & [Y_{N+2,N+2}]\end{bmatrix} \begin{bmatrix}[V_1]\\[V_2]\\\cdots\\[V_{N+1}]\\[V_{N+2}]\end{bmatrix} \tag{7.14}$$

In the Equation 7.14, $Y_{m,n}$ is a diagonal matrix whose elements relates harmonic of V_n to harmonics of I_n.

Nonlinear partition cannot be modelled using multiport parameters. Instead, by inverse Fourier transformation of V_n, $v_n(t)$ can be derived using: $F^{-1}\{V_n\} \longrightarrow v_n(t)$, and it could be used to calculate the current of the nonlinear elements connected to port n both in the time domain and frequency

domain as shown in Equation 7.15.

$$\begin{aligned} &Nonlinear\ Capacitance\ Contorlled\ by\ Voltage\ of\ Node\ n\ (V_n) \\ &q_n(t) = f_{q_n(t)}(v_n(t)) \\ &q_n(t) \xrightarrow{Fourier} Q_n \\ &i_{c,n}(t) = \frac{dq_n(t)}{dt} \xrightarrow{Fourier} I_{c,n} = j\Omega Q_n \\ &\Omega = diag(0, w_p, 2 \cdot w_p, \cdots, K \cdot w_p) \end{aligned} \tag{7.15}$$

$$\begin{aligned} &Nonlinear\ Resistance\ Contorlled\ by\ Voltage\ of\ Node\ n\ (V_n) \\ &i_{g,n}(t) = f_n(v_n(t)) \\ &i_{g,n}(t) \xrightarrow{Fourier} I_{G,n} \end{aligned} \tag{7.16}$$

Substituting the currents of linear and nonlinear sections into Equation 7.13, will give us the criteria to validate whether the selected voltages for the ports are the correct ones as shown in Equation 7.17.

$$F(V) = I_{linear} + j\Omega Q + I_G = 0 \tag{7.17}$$

7.3.2 Harmonic Balance Solution Algorithms

There are different methods that could be used to solve Equation 7.17. Between all of these methods, Newton's method is the preferred one for harmonic-balance analysis. Newton's method is an iterative method. These methods mostly are based on contraction theorem as discussed in Theorem 2. It should also be mentioned that considering the space X is a normed space that has finite dimension, then convergence to the fixed point is satisfied for all norms defined on the vector space as shown in Theorem 3.

It should be mentioned that theorems and definitions in this section are derived from [158].

Theorem 2 *Suppose there is a complete metric space X=(X,d), where $X \neq \emptyset$. If there is a contraction transform $T : X \longrightarrow X$, then T has precisely one fixed point. T is a contraction if there is an $\alpha < 1$ such that for all $x, y \in X$*

$$d(Tx, Ty) \leqslant \alpha \cdot d(x, y) \tag{7.18}$$

Theorem 3 *In a finite dimensional vector space, all norms are equivalent to each other, i.e., if $||x||_1$ and $||x||_2$ are different norms defined on a finite dimensional vector space, then there are positive number a and b such that:*

$$a||x||_1 \leqslant ||x||_2 \leqslant b||x||_1 \tag{7.19}$$

Applying Newton's method to Equation 7.17 results in an iterational method for the Harmonic Balance Analysis as shown in Equation 7.20.

$$V^{p+1} = V^p - (\frac{dF(V)}{dV})^{-1} F(V^p) \qquad J_F = \frac{dF(V)}{dV}|_{V=V^p} \tag{7.20}$$

The correct formulation of Newton's method for the Harmonic Balance method is discussed in Theorem 4.

Theorem 4 *Let X be a closed, bounded, and convex set in X. Let α be a fixed point of Equation 7.20 and assuming that the components of the Jackobian matrix J_F are continuously differentiated at some neighborhood and furthermore*

$$\lambda \equiv Max||J_F||_\infty < 1 \tag{7.21}$$

Then by choosing initial condition sufficiently close to α the iteration V^{P+1} will converge to α and this also is the unique fixed point for Equation 7.20

The Equation 7.21, which is related to convergence criterion, can become weaker by substitution it by the criterion shown in Equation 7.22.

$$Spectral\ Radius \equiv r_\sigma(J_F) < 1 \Rightarrow \lim_{m\to\infty} (J_F)^m = 0 \tag{7.22}$$

Spectral radius is defined in Definition 6 which is based on Definition 5.

Definition 5 *Assume X is a complex normed space and $T : D(T) \longrightarrow X$ is a linear operator. A regular value λ of T is a complex number such that*

$$\begin{aligned} &R_\lambda(T) = (t - \lambda I)^{-1} \quad exists, \\ &R_\lambda(T) = (t - \lambda I)^{-1} \quad is\ bounded, \\ &R_\lambda(T) = (t - \lambda I)^{-1} \quad is\ defined\ on\ a\ set\ which\ is\ dense\ in\ X \end{aligned}$$

The resolvent set ρ (T) of T is the set of all regular values λ of T

Definition 6 *The spectral radius $r_\sigma(T)$ of an operator $T \in B(X, X)$ on a complex Banach space X is:*

$$r_\sigma(T) = \sup_{\lambda\in\sigma(T)} |\lambda| \tag{7.23}$$

$$\sigma(T) = \mathbb{C} - \rho(T) \tag{7.24}$$

As mentioned in Theorem 4, the success of the Newton method is primarily based on the proper choice of its starting point; there are a few methods for generating this initial guess, e.g., using linear solution (linear estimation) of the nonlinear circuit as an initial guess and using DC solution and using transient analysis to find quasi steady-state response that can be used as an initial guess (transient-assisted harmonic balance (TAHB)) [154]. There is no guarantee that these methods always provide the proper initial guess and in many cases where the nonlinear circuit has multiple excitations, the initial guess derived from these methods can be inaccurate and far away from the actual solution[156].

Another possible technique is to calculate the circuit response with the assumption that the circuit is weakly nonlinear, and then use the response of this weakly nonlinear circuit as an initial guess for calculating the general response of the circuit. One of the popular methods for calculating the response of a weakly nonlinear circuit is based on the Volterra series analysis [154, 159, 160]. This method does not rely on the initial guess and the response can be found analytically. More importantly, this technique can be used to accommodate large nonlinear circuits with nonlinearities up to degree of 5[161], and it also can be used for the circuits with multi-tone inputs with commensurate and non-commensurate frequencies[160]. Therefore, it is a reasonable choice for finding initial guess of a strong or moderate nonlinear circuit.

7.4 Volterra Series Method

There are two general methods that use Volterra series analysis: the first is harmonic input method, and the second is the method of nonlinear currents. The latter is not as general as the former, because effectively the latter can only be used to calculate the nonlinear response at specific frequencies, but the former can be used to extract a general nonlinear transfer function that can be used to find the nonlinear response of a weakly nonlinear circuit at any frequency[160, 162]. These methods are discussed in the following sections.

There are some restriction in regards to the Volterra series application that should be considered when this method is used to find the solution of a nonlinear circuit [154]. The main restriction is based on the fact that the nonlinear elements should be categorized as weakly nonlinear. Although there is not an exact mathematical definition and distinction between weakly and strongly nonlinear circuits, weekly nonlinear circuits can be described

and modelled with adequate accuracy by their Taylor expansion of their nonlinear characteristic function. The other factor that restricts the application of this method to weakly nonlinear circuits is that the input excitations should be small and non-commensurate.

7.4.1 Introduction

Most of nonlinear circuits can be modelled using nonlinear components that are controlled by voltages. It could be shown that nodal analysis could be used for the solution of these circuits after finding state space representation of them. Based of the type of nonlinearity in the circuit, state variables could be chosen from the charge of capacitors and flux of inductors. This will lead to a representation similar to Equation 7.25

$$\begin{aligned} \xi_i'(t) = f_i(t, x(t)), \qquad \xi_i(t_0) = \eta_{i0}, \qquad i = 1, \cdots, n \\ x(t) = (\xi_1(t), \cdot, \xi_n(t)) \\ \xi_i = \xi_i(t_0) + \int_{t_0}^{t} f_i(s, x(s))ds \end{aligned} \tag{7.25}$$

Before getting into details of Volterra Series method, there are a few theorems that should be discussed first. Theorem 7 explains the completeness of function space $C[a, b]$ as follow:

Theorem 7 *The function space $C[a, b]$ is complete with the following metric:*

$$d(x_m, x_n) = \max_{t \in [a,b]} |x_m(t) - x_n(t)| \tag{7.26}$$

Using Equation 7, it can be proved that the space $C[a, b]$ is a Banach space with $||x(t)|| = \max_{t \in [a,b]} |x(t)|$ norm. This could help us to define a compact operator based on 7.25 on this space based on Theorem 8. It should be mentioned that this operator is defined on a infinite-dimensional space $C[a, b]$.

Theorem 8 *Suppose we have a continuous function*

$$f : [a, b] \times [-R, R] \longrightarrow \mathbb{R} \tag{7.27}$$

where $-\inf < a < b < \inf$, $0 < R < \inf$. Set $M = \{x \in C([a, b], \mathbb{R} : ||x|| \leqslant R\}$ then the integral operator

$$(Tx)(t) = \int_{t_0}^{t} f_i(s, x(s))ds \tag{7.28}$$

defined in Equation 7.25 is a compact operator.

Using the compactness property of the integral operator (Equation 8), it could be approximated with an operator with finite dimension range as is shown in Theorem 9

Theorem 9 *Let X and Y be Banach spaces and $T : M \subseteq X \longrightarrow Y$ be a compact operator. then for every $n \in \mathbb{N}$ there exists a compact operator $P_n : M \longrightarrow Y$ such that*

$$\sup_{x \in M} ||T(x) - P_n(x)|| \leq \frac{1}{n}, \qquad and \qquad dim(span\ P_n(M)) < \infty \tag{7.29}$$

The definition of a compact operator is shown in Definition 10.

Definition 10 *Assume X and Y are Banach Spaces, and $T : D(T) \subseteq X \longrightarrow Y$ is an operator such that*

1)T is continuous

2)T maps bounded sets into relatively compact sets, that is, $\overline{T(M)}$ is compact

then T is a compact operator

Using the above theorems and StoneWeierstrass Theorem (see Theorem 11), which are the modern basis of Volterra Theorem, Norbert Weiner showed that the response of a weakly nonlinear circuit having small excitations could be expressed in the time domain as shown in Equation 7.30.

Theorem 11 *Assume that K is a compact metric space and $A \subset C(K, \mathbb{R})$ a unital sub-algebra which separates points of K; consequently, A is dense in $C(K, \mathbb{R})$*

$$\begin{aligned} w(t) = &\int_{-\infty}^{\infty} h_1(\tau) s(t - \tau_1) d\tau_1 \\ &+ \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} h_2(\tau_1, \tau_2) s(t - \tau_1) s(t - \tau_2) d\tau_1 d\tau_2 \\ &+ \cdots \end{aligned} \tag{7.30}$$

$$w(t) = \sum_{n=1}^{N} w_n(t)$$

$$w_n(t) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \cdots, \tau_n) s(t - \tau_1) \cdots s(t - \tau_n) d\tau_1 \cdots d\tau_n$$

Equation 7.30 could also be represented in the frequency domain form as shown in Equation 7.31.

$$w_n(t) = \frac{1}{2^n} \sum_{q1=-Q}^{q1=+Q} \cdots \sum_{qn=-Q}^{qn=+Q} V_{s,q1} \cdots V_{s,qn} \cdot exp[j(w_{q1} + \cdots + w_{qn})t].H_n(w_{q1} + \cdots + w_{qn}) \tag{7.31}$$

$$H_n(w_{q1} + \cdots + w_{qn}) = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \cdots, \tau_n) \cdot exp[-j(w_{q1} + \cdots + w_{qn})t] \cdot d\tau_1 \cdots d\tau_n$$

The $H_n(w_{q1}+\cdots+w_{qn})$ in Equation 7.31 is called the nonlinear transfer function. To calculate this nonlinear transfer function there are two well-known methods called the Harmonic Input Method and the Method of Nonlinear Current. Because we used the Harmonic Input Method in this chapter, we will explain this method in more detail in the following section.

7.4.2 Harmonic Input Method

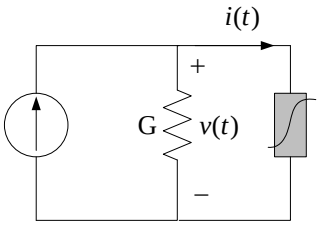
The assumption in reaching Equation 7.31 was that the input excitations are in the form of multi-tone sinusoidal waveforms, $\frac{1}{2}\sum_{q=-Q}^{q=+Q} V_{s,q} exp(j \cdot w_q t)$. Similar to finding the linear transfer function where a single tone is used to calculate the linear transfer function, in this method multi-tone excitation is used to find nonlinear transfer functions. For example, if we want to find the n_{th} order transfer function, $h_n(\tau_1, \cdots, \tau_n) \cdot exp[-j(w_{q1} + \cdots + w_{qn})t]$, there needs to be a n multi-tone excitation and the transfer function could be found based on Equation 7.32.

$$Input\ Excitation = \sum_{n=1}^{n=N} exp(j \cdot w_n t) \tag{7.32}$$

$$n_{th}\ order\ Output|_{w=w_1+w_2+\cdots+w_n} = n! \cdot H_n(w_1 + w_2 + \cdots + w_n) \cdot exp[-j(w_1 + w_2 + \cdots + w_n)t]$$

Based on the above equation, the circuit will be solved considering the fact that only the terms of order n_{th} will be retained because other terms cannot contribute to the n_{th} order response.

In this chapter, we use the harmonic input method for calculating the initial guess of the response which is used as the initial guess for HBA. This technique is more accurate than DC and linear estimation because in addition to linear terms, the effects of of nonlinear terms are also included. Since



$$i(t) = g_1 \cdot v(t) + g_2 \cdot v^2(t) + g_3 \cdot v^3(t) + g_4 \cdot v^4(t) + g_5 \cdot v^5(t)$$

Figure 7.5: Schematic of the nonlinear circuit used in the simulations

other methods that improve HB convergence usually are susceptible to numerical error [163], the proposed technique can complement them to improve their speed and performance. To show the efficiency of the proposed method, a simple circuit is evaluated to compare the proposed method with TAHB and linear estimation. It is demonstrated that while none of these conventional methods can converge to the solution, the presented method will resolve the convergence issue. Then, the effectiveness of different Volterra kernels are examined and it is shown that one can improve the speed of initial guess calculation by choosing a fewer number of Volterra kernels instead of including all of them.

7.5 Derivation of Volterra Kernels by Using Harmonic Input Method

The Volterra series method is a well-known technique in the simulation of weakly nonlinear circuits. For implementation of this method and calculating the behaviour of the weakly nonlinear circuit, Taylor series expansion of the nonlinearities around their bias points is used. [154, 159, 160, 164]

To extract the nonlinear transfer function of the sample nonlinear circuit, typically the harmonic input method is used, and by using these nonlinear transfer functions (Volterra kernels), one can find the nonlinear response of the circuit. The results obtained from the harmonic input method can create a good initial guess for the actual nonlinear circuit. This response will be used as an initial guess in HBA; therefore, the complete analysis of the circuit is not necessary at this point. To show applicability of the proposed procedure, we will demonstrate the analysis of a simple circuit in the following sections. This circuit is composed of a current source, a nonlinear conductance which is controlled by the voltage across it and a load. The schematic diagram of the circuit is shown in Fig. 7.5. Although

simple, this circuit can be used for modeling an amplifier where the nonlinear conductance models the output resistance of the amplifier which is nonlinear in deep sub-micron technologies [165].

7.5.1 Nodal Analysis Based on Harmonic Input Method

For the circuit of Fig. 7.5, to derive different kernels, one can write Kirchhoff's current law (KCL) for the only node of the circuit (7.33); this KCL is the fundamental equation used in derivation of each nonlinear transfer function.

$$I_s(t) = G_L \cdot v(t) + g_1 \cdot v(t) + g_2 \cdot v^2(t) + g_3 \cdot v^3(t) \tag{7.33}$$

First-Order Kernel

The first step is to calculate the linear transfer function of the system. It should be noted that in this step, as mentioned in the previous section, the input to the nonlinear circuit (i.e., the current source in Fig. 7.5), is assumed to be in the form of $exp(j2\pi f_1 t)$.The procedure for deriving the linear transfer function of the circuit is shown in (7.35).

$$v(t) = \sum_{n=1}^{N} v_n(t) = \sum_{n=1}^{N} A_n(f_1, \cdots, f_1) exp[j2\pi(nf_1)t] \tag{7.34}$$

putting (7.34) in (7.33), we will have (7.35)

$$\begin{aligned}(G_L + g_1) \times \sum_{n=1}^{N} A_n(f_1, \cdots, f_1) exp[j2\pi(nf_1)t] \qquad (7.35)\\ = exp(j2\pi f_1 t) - g_2 \times \{\sum_{n=1}^{N} A_n(f_1, \cdots, f_1) exp[j2\pi(nf_1)t]\}^2\\ - g_3 \times \{\sum_{n=1}^{N} A_n(f_1, \cdots, f_1) exp[j2\pi(nf_1)t]\}^3\end{aligned}$$

Because the $exp(j2\pi f_i)(i = 1, \cdots, n)$ functions are linearly independent, then we will have (7.36).

$$(G_1 + g_1) \times A_1(f_1) \times exp(j2\pi f_1 t) = exp(j2\pi f_1 t) \tag{7.36a}$$

$$\Longrightarrow A_1(f_1) = \frac{1}{G_1 + g_1} \tag{7.36b}$$

Second-Order Kernel

The second step is to calculate the second-order transfer function of the system. In this step, the input to the nonlinear circuit, which is the current source in Fig. 7.5, is assumed to be in the form of $exp(j2\pi f_1 t)+exp(j2\pi f_2 t)$. The procedure for deriving the second-order transfer function of the system is shown in (7.37).

$$v_n(t) = \sum_{q_1=1}^{2} \cdots \sum_{q_n=1}^{2} A_n(f_{q_1}, \cdots, f_{q_n}) \times exp[j2\pi(f_{q_1} + \cdots + f_{q_n})t] \tag{7.37}$$

Because in (7.33) only $v_2(t)$ and $v_1^2(t)$ contain second-order terms, then in calculating the second-order nonlinear transfer function, we can neglect the other terms in (7.33), and the result is shown in (7.38).

$$(G_L + g_1) \times v_2(t) = -g_2(t) \times v_1^2(t) \tag{7.38a}$$

$$v_2(t) = \sum_{q_1=1}^{2} \sum_{q_2=1}^{2} A_2(f_{q_1}, f_{q_2}) \times exp[j2\pi(f_{q_1} + f_{q_2})t] \tag{7.38b}$$

By substituting (7.38b) in (7.38a), the Second Order Transfer Function can be found (7.39)

$$A_2(f_1, f_2) = \frac{-g_2 \times A_1(f_1) \times A_1(f_2)}{(G_L + g_1)} \tag{7.39}$$

Third-Order Kernel

The procedure for finding the third-order kernel is the same as the other lower orders; the subtle difference is in finding the terms that can produce third-order components in Equation 7.33. The process for deriving the third-order kernel is shown in Equation 7.40.

$$(G_L + g_1) \times v_3(t) = -g_2(t) \times (2v_1(t)v_2(t)) - g_3 \times v_1^3(t) \tag{7.40a}$$

$$v_3(t) = \sum_{q_1=1}^{3} \sum_{q_1=1}^{3} \sum_{q_2=1}^{3} A_3(f_{q_1}, f_{q_2}, f_{q_3}) \times exp[j2\pi(f_{q_1} + f_{q_2} + f_{q_3})t] \tag{7.40b}$$

Table 7.1: ADS HBA and Custom HBA results for the magnitude of harmonics of the output voltage

Frequency (Hz)	Magnitude (Commercial HBA)	Magnitude (Custom HBA)
0	1.1070	1.1073
1	11.904	11.9041
2	0.0470	0.0469
3	2.7880	2.7881
4	0.0280	0.0283
5	1.2760	1.2760

By substituting (7.40b) and (7.38b) in (7.40a), the third-order nonlinear transfer function can be found as (7.41).

$$A_3(f_1,f_2,f_3) = \frac{-12\times g_2}{6\times(G_L+g_1)}\overline{A_1(f_1)A_2(f_2,f_3)} - \frac{g_3}{(G_L+g_1)}A_1(f_1)A_1(f_2)A_1(f_3) \tag{7.41}$$

In (7.41), the overbar denotes the arithmetic average of the permuted terms.

7.6 Numerical Analysis of the Proposed Algorithm

To implement the proposed technique we use a custom HBA code developed in [162]. The obtained results from this custom HBA tool with its initial guess generated by the harmonic input method is compared with those of Agilent Advanced Design System (ADS) with an arbitrary initial guess. In this analysis, for the nonlinear circuit in Fig. 7.5 nonlinear coefficients $g_1 = 1e-3$, $g_2 = 0.5e-3$, $g_3 = 1e-4$, $g_4 = 0.5e-4$, and $g_5 = 1e-5$ are used. The amplitude of the current source is $1A$, and the resistance of the load is $1k\Omega$. The results are shown in Table 7.1. It can be seen that the output of both simulators, commercially available ADS and our proposed HBA, produce the same results. These matched results are also verified for other circuit examples and thus the fidelity of the custom HBA code is verified. To demonstrate the effectiveness of the proposed method, we first change the coefficients of the nonlinearities so that our custom HBA and

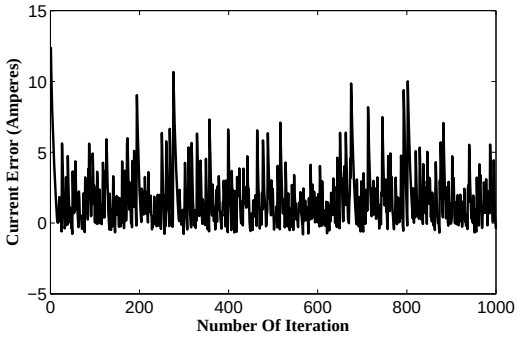


Figure 7.6: Current error of the output node without using Volterra initial condition (logarithmic vertical-axis scale, $10 \cdot log(x)$)

ADS HBA simulations fail to converge. The selected nonlinear coefficients are $g_1 = 1e-3$, $g_2 = 2$, $g_3 = 2e-3$, $g_4 = 0$, $g_5 = 0$. The amplitude of the current source and the value for the load resistance are the same as before. The error in calculated current of the custom HBA is shown in Fig. 7.6. As can be seen from the figure, the numerical algorithm is trapped, and is not able to converge to the right solution. It should be noted that with these nonlinear coefficients, transient analysis of ADS also does not converge. Next, we obtain the initial guess generated by harmonic input method using the equations derived in Section 7.5 ((7.36b), (7.39), and (7.41)). The results of using custom HBA simulator with the initial guess generated by harmonic input method are shown in Figs. 7.7(a) and (b). Figure 7.7(a) demonstrates improvement of the final response and decreasing trend of the error in the calculated current versus number of iterations in the underlying Newton algorithm. To assist the ADS simulator to converge, the results of harmonic input method are used to calculate the initial voltage; this initial voltage is used as the initial node set in ADS transient-assisted harmonic balance, and the final results, Table 7.2, are very similar to the results obtained by the custom HBA.

7.7 Effect of Each Volterra Term in the Convergence

In our previous analysis, we used several Volterra terms. These terms include first, second and third harmonics in addition to DC components. These components can be obtained by using (7.36b), (7.39), and (7.41). In this

Table 7.2: ADS TAHB and custom HBA using harmonic input method (HIM) results for the logarithmic scale magnitude of harmonics in output voltage.

Frequency (Hz)	Log (V_{out}) (Commercial HB using TAHB)	Log (V_{out}) (Custom HB using HIM)
0	+3.260	+3.30
1	-3.501	-3.6021
2	-9.602	-10.1
3	-13.493	-13.34

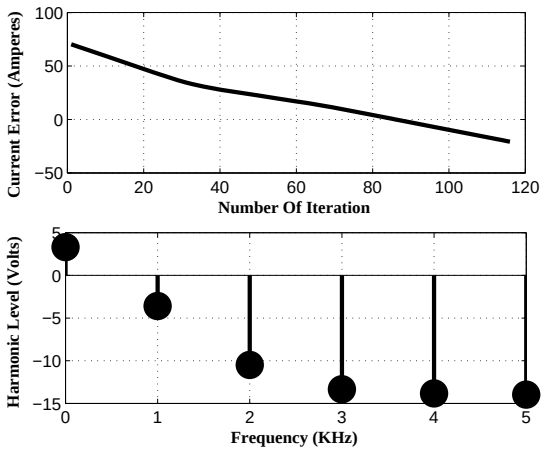


Figure 7.7: (a) Error in calculated current (logarithmic scale on vertical axis) (b) Magnitude of the voltage harmonics (logarithmic scale)

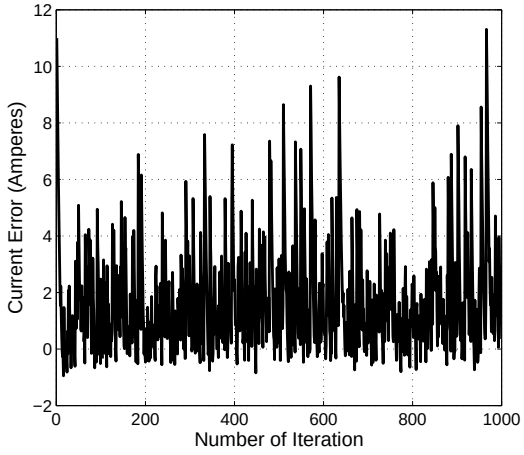


Figure 7.8: Logarithmic scale of current error of the output node with including just one term of Volterra initial condition (linear term)

section, we show that it is not necessary to use all of these terms to achieve a good estimate for the initial guess. By proper choice of harmonic input terms, one can obtain the same results by using fewer Volterra terms.

The choice of harmonic input terms that should be included in initial guess calculations depends on the magnitude of the Taylor series expansion coefficients around the bias point. For demonstrating this idea, the nonlinear coefficients, amplitude of the current source and the resistance of the load are chosen as $g_1 = 1e-3$, $g_2 = 2$, $g_3 = 2e-3$, $g_4 = 0$, $g_5 = 0$), $1A$ and $1k\Omega$, respectively. As can be inferred from nonlinear coefficients, the linear part of the nonlinearity is the weakest component among its nonlinear coefficients; then, it can be predicted that including just this term, in other words just (7.36b), in the initial guess approximation process may not be sufficient for the convergence of the Newton algorithm. By using custom HBA and including only (7.36b) in the initial guess approximation, Fig. 7.8 is obtained. Fig. 7.8 shows that by including only the linear term (7.36b) in the initial guess approximation our algorithm will not converge. To solve this problem we have to include another term from the harmonic input analysis. To show this, we will include the effect of the nonlinear coefficient of degree 3 by (7.41) in producing an initial guess approximation in our Custom HBA. Fig. 7.9 shows the result of including the effects of both first- and third-degree terms. As can be seen from the figure, by using these two nonlinear coefficients, the algorithm converges to the correct solution. Finally, because

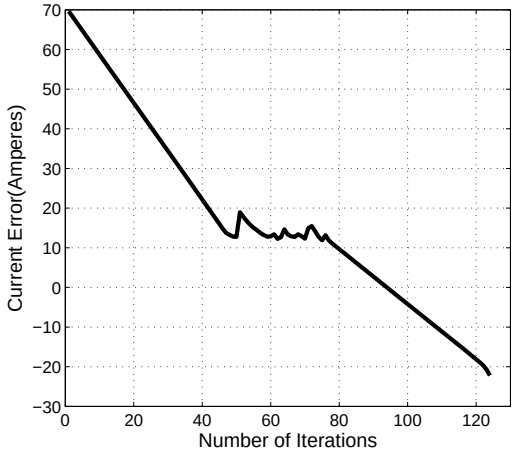


Figure 7.9: Logarithmic scale of current error of the output node with including the effects of first and third degree terms of Volterra initial condition

the nonlinear coefficient of degree 2 is the largest coefficient between all of the nonlinear coefficients, it can be predicted that by including just the effect of this nonlinearity, we can produce a good approximation of the initial condition. This statement can be shown by Fig. 7.10 which is obtained by only including the effect of nonlinear coefficient of degree 2. When fewer Volterra terms are used less memory is required for implementation of the technique and also due to the decrease in the required computations, the speed of calculations is also improved.

7.8 Conclusions

In this chapter, a method to estimate the initial guess in the harmonic balance method is proposed. The technique uses the harmonic input method and is based on Volterra kernels. It is shown that selecting initial point inappropriately can make the analysis non-convergent, and by using an initial guess generated by the harmonic input method, the convergence of the Newton algorithm is substantially improved. The proposed method does not need an initial guess, and the solution of it can be derived analytically. It is also shown that by choosing appropriate Volterra terms, we can achieve improvement in simulation time and also memory required for calculating an initial guess. Some rules of thumb, about the effectiveness of each Volterra

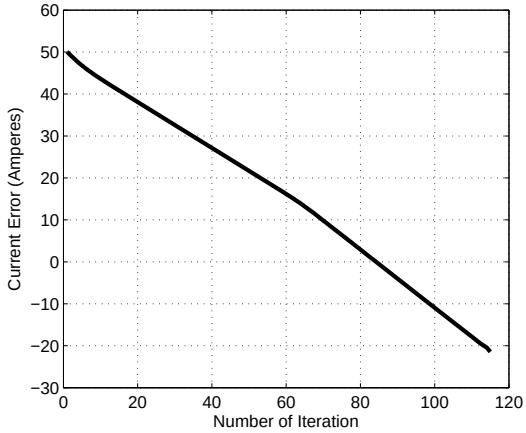


Figure 7.10: Logarithmic scale of current error of the output node with including the effects of second degree term of Volterra initial condition

term, and the proper choice of Volterra terms are also presented.

Chapter 8

Effect of Body Bias on the Performance of Electrical Amplifiers

Volttera theory with its application in the nonlinear circuit simulation has been discussed in the previous chapter. In this chapter, the effect of body biasing on the nonlinear behaviour of MOS transistors operating at radio frequency (RF) band is analyzed and modelled based on the previously discussed Volterra theory. To verify the analysis, intermodulation distortion of a single-stage MOS amplifier is modelled and is experimentally characterized. The I-V characteristic of a transistor is modelled using a multi-dimensional Taylor series expansion and the nonlinearity coefficients of the characteristic curve are extracted using curve fitting by the method of least square error (LSE). The nonlinearity coefficients are then used to find the optimum third-order intercept point (IP3), which can be calculated by the Volterra method. As a result, different Volterra kernels up to the third-order are derived and used to find the input-referred IP3 (IIP3) sweet spot. The IIP3 sweet spot calculated using the Volterra method compares favourably with the simulation results based on the periodic steady-state (PSS) analysis as well as experimental results. The derived theory and experimental results show that body bias could be used as an effective tuning tool in the design of a typical electronic amplifier which has been discussed at the end of chapter. A typical Low Noise Amplifier (LNA) has been designed and fabricated in $130nm$ IBM process, and the effect of body bias on its design criteria such as Gain, Noise Figure, and IP3 is examined.

8.1 Introduction

In the design of radio-frequency (RF) integrated circuits, special attention should be paid to different nonlinear phenomena such as harmonic generation, intermodulation distortion, saturation and desensitization. Different

figures of merit used to evaluate and compare the nonlinear effects of RF circuits include total harmonic distortion (THD), 1-dB compression point, and third-order intercept point (IP3).

IP3 is commonly used to represent the nonlinearity of amplifiers. Ideally, in a given design IP3 should be maximized subject to design trade-offs such as the required noise performance and power consumption. Finding the operating point that optimizes such design criteria is typically challenging, and thus the process of finding the sweet spot for linearity performance is usually based on heuristic simulations [166]. Relying only on the simulation results, the designer cannot capture the effect of different circuit parameters on the linearity performance on the circuit.

In [167] the effect of V_{GS} on the linearity performance of a 90-nm RF CMOS transistor has been examined; however, in this analysis a simplified model for calculating IP3 has been used. Using a more realistic model and accounting for different nonlinearity coefficients, in [168] the effect of V_{GS} on t linearity performance of the same 90-nm RF CMOS technology has been elaborated more accurately. In [169] different configurations for low-noise amplifiers (LNAs) have been used to simultaneously optimize the input matching, power consumption and noise figure; however, the linearity hasn't been taken into account in this approach. An RF synthesis tool has been proposed in [170]; however, in this tool the linearity performance is optimized based on only three nonlinear coefficients and furthermore body effect is not taken into consideration. The effect of body biasing has been studied in literature, in particular, in the context of designing variable gain amplifiers [166, 171] and low-power and low-noise circuits [172–174].

This chapter presents an alternative approach for analytical modelling and characterization of body biasing and its effects on nonlinear behaviour of a MOS transistor. Using Volterra theory as an analytical tool for this modelling, a procedure for finding the sweet spot for IP3 is presented. The organization of the paper is as follows: Section 8.2 is focused on deriving different Volterra kernels that are used in calculating sweet IP3 spot; Harmonic Input Method (HIM) is used in order to calculate the analytical expression for these kernels. Then, using the LSE technique, curve fitting of a multi-dimensional Taylor series to a characteristic curve of an RF transistor is presented in Section 8.3, and the required nonlinearity coefficients for calculating the sweet IP3 spot are extracted. Based on these coefficients and nonlinear kernels in 8.2, the sweet IP3 spot is calculated in 8.4, and then the results are compared with PSS analysis as well as experimental measurements of a single-stage MOS amplifier. Concluding remarks are provided in Section 8.7.

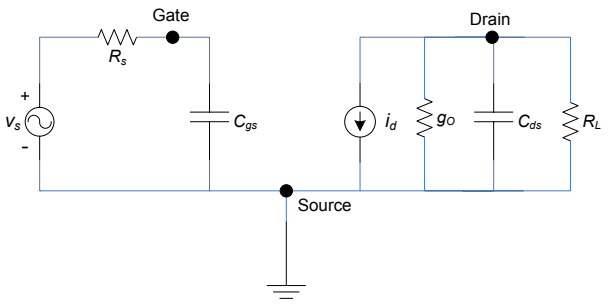


Figure 8.1: The main simplified model for calculating different Volterra Kernels

8.2 Volterra Theory and Kernel Calculation

Volterra theory is a useful method for analyzing the nonlinear phenomena in weakly nonlinear circuits [159, 160] as mentioned in the previous chapter. Different Volterra kernels (nonlinear kernels) can be derived analytically by using the Harmonic Input Method (HIM) [154, 160]. the HIM needs all nonlinear characteristic of each nonlinear elements to be expanded around their bias point by a Taylor series; as a result, the drain current of the transistor should be expanded to its Taylor series (8.1).

$$\begin{aligned} i_d = {} & g_m\, v_{gs} + K_{2GM}\, v_{gs}^2 + K_{3GM}\, v_{gs}^3 \\ & + g_o\, v_{ds} + K_{2GO}\, v_{ds}^2 + K_{3GO}\, v_{ds}^3 \\ & + K_{2GMGO}\, v_{gs}\, v_{ds} + K_{3GM2GO}\, v_{ds}\, v_{gs}^2 \\ & + K_{3GMGO2}\, v_{gs}\, v_{ds}^2 \end{aligned} \tag{8.1}$$

The simplified model for extracting nonlinear kernels is shown in Fig. 8.1. The general equation for using in the Volterra method and deriving nonlinear kernels can be obtained by writing KCL at the drain node in Fig. 8.1 as in (8.2). Extracted using HIM, different Volterra kernels can be derived by this basic equation (8.2). Although the procedure to extract Volterra kernels needs some algebra,it is straight forward [160]. It should be mentioned that in the following equations, subscript for voltages and currents means the component of that voltage or current having the same order as subscript.

$$i_d + \frac{v_{ds}}{R_L} + g_o\, v_{ds} + C_{ds}\, \frac{dv_{ds}}{dt} = 0 \tag{8.2}$$

8.2.1 First Order Kernel

To show the process of extracting nonlinear kernels, first order kernel derivation is elaborated as follow: first assume that the input to the circuit is $e^{(j2\pi f_1 t)}$, then it is now possible to calculate the First Order Volterra Kernel based on (8.2):

$$\begin{aligned}
&\text{Based on Volterra Theory: } (v_{ds})_1 = H_1(f_1) \times e^{(j2\pi f_1 t)} \\
&\rightarrow (i_d)_1 + \frac{(v_{ds})_1}{R_L} + g_o\,(v_{ds})_1 + C_{ds}\,\frac{(dv_{ds})_1}{dt} = 0 \\
&\rightarrow g_m\, v_{gs} = -(g_o + g_L + j2\pi f_1\, C_{ds})\, H_1(f_1) \\
&\Rightarrow H_1(f_1) = \frac{-g_m}{R_s}\, Z_s(f_1) Z_L(f_1)
\end{aligned} \tag{8.3}$$

8.2.2 Second Order Kernel

Calculating the second order kernel is similar to the first order one in essence; however, the assumption about the input to the circuit should be changed. Using HIM, the input should be in the form $e^{(j2\pi f_1 t)} + e^{(j2\pi f_2 t)}$. It is now possible to calculate the second order Volterra kernel based on (8.2). From the different terms in (8.1) only the following terms can produce second order currents:

$$\begin{aligned}
(i_d)_2 &= K_{2GM}\,(v_{gs}^2)_2 + K_{2GO}\,(v_{ds}^2)_2 + K_{2GMGO}\,(v_{gs}\, v_{ds})_2 \\
&= K_{2GM}\,(v_{gs})_1^2 + K_{2GO}\,(v_{ds})_1^2 \\
&+ K_{2GMGO}\,(v_{gs})_1\,(v_{ds})_1
\end{aligned} \tag{8.4}$$

Using the first order Volterra kernel (8.3), Volterra theory [160], and (8.4), the second order kernel can be computed after doing some algebra (8.4)

$$\begin{aligned}
H_2(f_1, f_2) &= -\frac{K_{2GM}}{R_s^2} Z_s(f_1) Z_s(f_2) Z_L(f_1 + f_2) \\
&- K_{2GO} H_1(f_1) H_1(f_2) Z_L(f_1 + f_2) \\
&- \frac{K_{2GMGO}}{Rs} \overline{H_1(f_1) Z_s(f_2)} Z_L(f_1 + f_2) \\
\overline{H_1(f_1) Z_s(f_2)} &= \frac{1}{2!}\,(H_1(f_1) Z_s(f_2) + H_1(f_2) Z_s(f_1))
\end{aligned} \tag{8.5}$$

8.2.3 Third Order Kernel

The process for extracting the third order Volterra kernel is actually the same as other kernels. Similar to the second order kernel, the assumption

for the input should be changed. Using HIM, the input should be in the form $e^{(j2\pi f_1 t)} + e^{(j2\pi f_2 t)} + e^{(j2\pi f_3 t)}$. Using Volterra theory [160], first and second order kernels(8.3,8.5), and the terms in (8.1) producing third order components, third order kernel can be obtained as (8.6).

$$\begin{aligned} H_3(f_1,f_2,f_3) = Z_L(f_1+f_2+f_3)\times \\ \big[\, & K_{3GO}\, H_1(f_1)H_1(f_2)H_1(f_3) \\ & + 2K_{2GO}\, \overline{H_1(f_1)H_2(f_2,f_3)} \\ & + \frac{K_{3GMGO2}}{R_s}\, \overline{Z_s(f_1)H_1(f_2)H_1(f_3)} \\ & + \frac{K_{3GM}}{R_s^3}\, Z_s(f_1)Z_s(f_2)Z_s(f_3) \\ & + \frac{K_{2GMGO}}{R_s}\, \overline{Z_s(f_1)H_2(f_2,f_3)} \\ & + \frac{K_{3GM2GO}}{R_s^2}\, \overline{Z_s(f_1)Z_s(f_2)H_1(f_3)} \,\big] \end{aligned} \tag{8.6}$$

It should be mentioned that similar to (8.5), overbar means the arithmetic average of the permuted terms in (8.6).

8.3 Nonlinear Coefficients Calculation

In using Volterra Theory for this problem, the current of the drain should be expanded by Taylor series according to (8.1). In this specific case, because we want to expand the drain current with respect to two variables (V_{ds} and V_{gs}), then assuming up to third degree terms in the Taylor series expansion, the number of coefficients for the multi-variable Taylor series expansion will be nine (8.1). In (8.1), variables i_d, v_{gs}, v_{ds} and v_{bs} are incremental variables; this means that:

$$\begin{aligned} v_{gs} &= v_{GS} - V_{GSQ} \\ v_{ds} &= v_{DS} - V_{DSQ} \\ v_{bs} &= v_{BS} - V_{BSQ} \\ i_d &= i_D - I_{DQ} \end{aligned} \tag{8.7}$$

The configuration for measuring the characteristic curve of the RF transistor is shown in Fig. 8.2. Running the simulations and importing the data to the Matlab, now it is possible to use LSE to fit these data to a multi-dimensional Taylor series (8.1). The imported results to Matlab and also the results of

using LSE to find nonlinear coefficients are shown in Fig. 8.3 and Fig. 8.4 respectively. We need many data points (at least 9) to do curve fitting using LSE; the mesh for getting these data points are shown in Fig. 8.5, the LSE equation that also needs to be solved is shown in Equation 8.8. This mesh can be imagined as a perpendicular plane to the plane which V_{BS} and V_{DS} axes create in Fig. 8.3.

$$AX = B$$

$$A = \begin{bmatrix} (v_{gs})_1 & (v_{gs}^2)_1 & \cdots & (v_{ds})_1\,(v_{gs}^2)_1 & (v_{gs})_1\,(v_{ds}^2)_1 \\ (v_{gs})_2 & (v_{gs}^2)_2 & \cdots & (v_{ds})_2\,(v_{gs}^2)_2 & (v_{gs})_2\,(v_{ds}^2)_2 \\ (v_{gs})_2 & (v_{gs}^2)_2 & \cdots & (v_{ds})_2\,(v_{gs}^2)_2 & (v_{gs})_2\,(v_{ds}^2)_2 \\ \vdots & & & & \\ (v_{gs})_i & (v_{gs}^2)_i & \cdots & (v_{ds})_i\,(v_{bs}^2)_i & (v_{gs})_i\,(v_{ds})_i\,(v_{bs})_i \end{bmatrix}$$

$$i = (2 \cdot Temp1 + 1) \times (2 \cdot Temp2 + 1)$$

$$i = (\text{Number of Measurements} \equiv \text{Number of Equations})$$

$$X = \begin{bmatrix} g_m \\ K_{2GM} \\ K_{3GM} \\ g_o \\ K_{2GO} \\ \vdots \\ K_{2GMGO} \\ K_{3GM2GO} \\ K_{3GMGO2} \end{bmatrix} \quad B = \begin{bmatrix} (i_d)_1 \\ (i_d)_2 \\ (i_d)_3 \\ (i_d)_4 \\ \vdots \\ (i_d)_i \end{bmatrix} \tag{8.8}$$

8.4 Simulation Results

The process for calculating the $IIP3$ is as follows: first the amplitude of the intermodulation distortion, which is amplitude at frequency $2f_2 - f_1$, should be calculated; it is called $A_{(2f_2-f_1)}$; after that, the amplitude at frequency of one of the input frequencies should be calculated, it is called A_{f_1}. Based on these amplitudes, it is now possible to calculate $IIP3$, which is the amplitude of one of the input waveforms where $A_{(2f_2-f_1)} = A_{f_1}$.

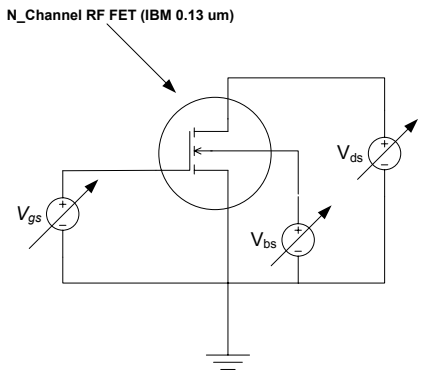


Figure 8.2: Schematic for measuring the drain current (The analysis type is DC-Sweep and the sweep variables are V_{GSQ}, V_{DSQ}, and V_{BSQ})

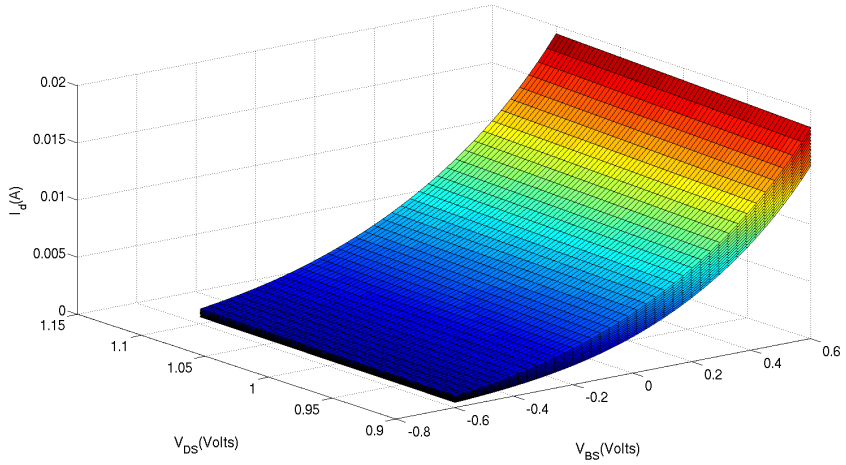


Figure 8.3: Drain Current with respect to $V_{BSQ}, V_{GSQ}, V_{DSQ}$

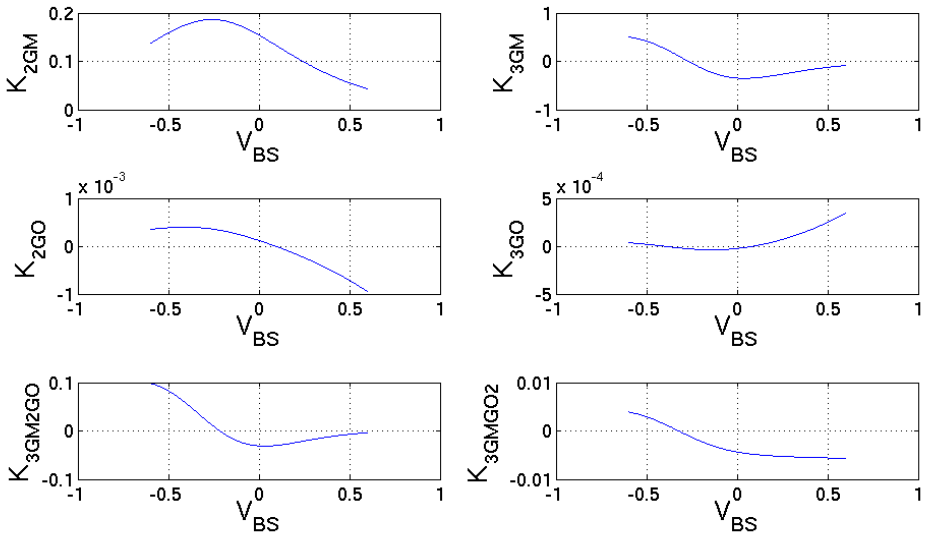


Figure 8.4: Multi-Dimensional Taylor Coefficients, refer to (8.1)

all the above process can be done analytically by using the Volterra method; in (8.9), the equation for IIP3 is given; this equation can be derived by using Volterra theory and doing some algebra.

$$IIP3 = \frac{4\,|H_1(f_1)|}{3\,|H_3(-f_1, f_2, f_2)| \times (8 \times 50 \times 10^{-3})} \tag{8.9}$$

As you can see from (8.9) and Fig. 8.6, since $H_1(f_1)$ has increasing trend with the change in body bias voltage, then the sweet point for IIP3 can be found by minimizing the $|H_3(-f_1, f_2, f_2)|$. Fig. 8.7 shows $|H_3(-f_1, f_2, f_2)|$ based on plugin in all of our data from section 8.3 into equations in section 8.2 and using 8.9. For comparison and verification of our results, the same circuit has been simulated with SpectreRF PSS analysis of Cadence. The result of the simulation is shown in Fig. 8.8. As you can see from the Fig. 8.7 and Fig. 8.8, our result is in good agreement with PSS result. To summarize our result, and for better comparison and verification of our method with respect to PSS analysis, the value of sweet point for each of the analyses is shown in Table 8.1.

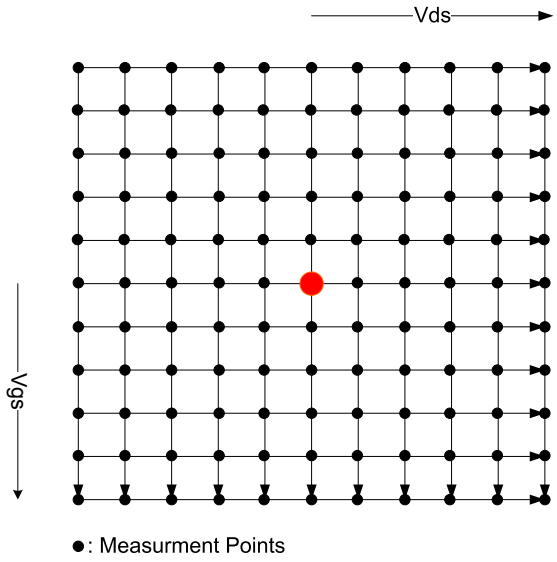


Figure 8.5: Sample web of nodes that have active role in solving Least Square Equation

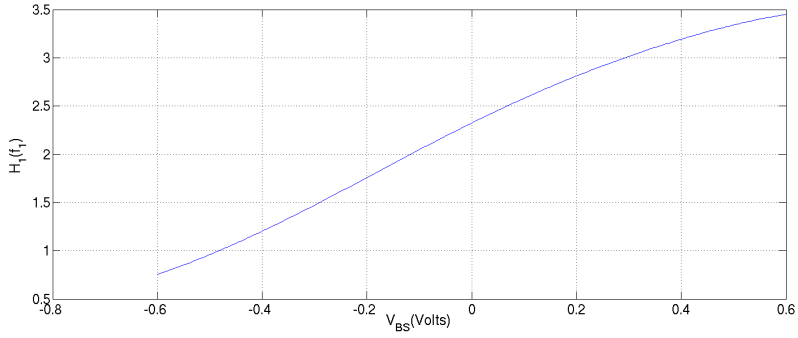


Figure 8.6: Variation of first order kernel with change in bias voltage ($f_1 = 2\,GHz, V_{DS} = 1,$ and $V_{GS} = 0.5$)

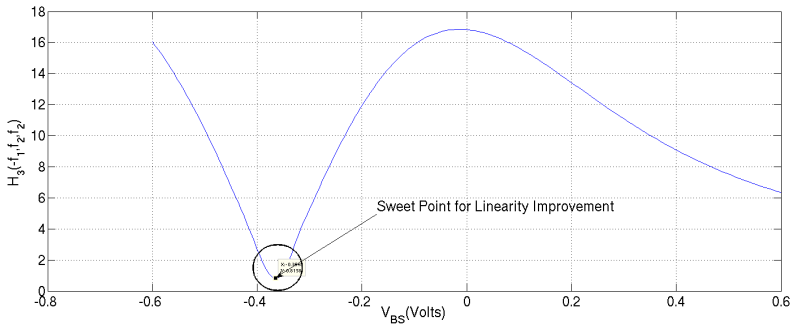


Figure 8.7: Variation of first order kernel with change in the body bias voltage ($f_1 = 2\,GHz, f_2 = 2.02\,GHz, V_{DS} = 1,$ and $V_{GS} = 0.5$)

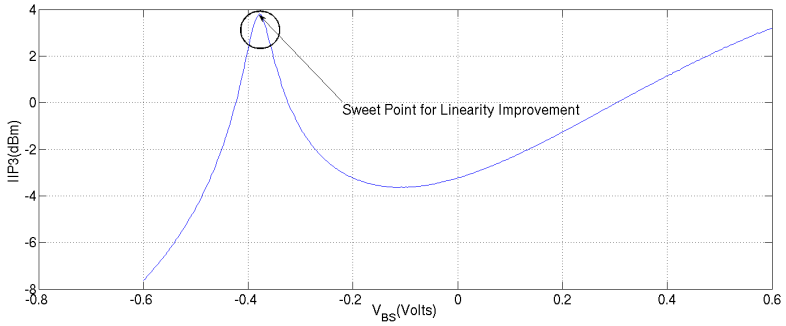


Figure 8.8: Variation of first order kernel with change in the body bias voltage using SpectreRF PSS analysis ($f_1 = 2\,GHz, f_2 = 2.02\,GHz, V_{DS} = 1,$ and $V_{GS} = 0.5$)

Table 8.1: Comparison of sweet points obtained by Volterra Method and PSS analysis

Method	IIP3 sweet point with respect to V_{BS}
Voletrra	-0.365
PSS using SpectreRF	-0.375

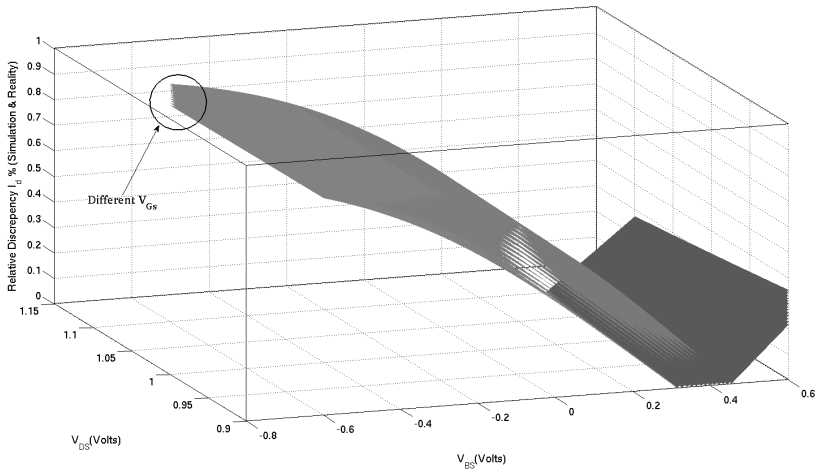


Figure 8.9: Comparison between Experimental drain current and Simulation drain current for different bias conditions using HP 4155A Semiconductor Parameter Analyzer

8.5 Experimental Results

Fig. 8.9 shows the difference between the simulation results and experimental result for the drain current. To measure the drain current for different bias conditions, HP 4155A Semiconductor Parameter Analyzer were used. As you can see there are some discrepancies in the simulation and practical results for the drain current, which can be justified by considering well proximity effect, isolation-induced stress, and process variation. As you can see from Fig. 8.9 the maximum relative difference for drain current between the experimental results and simulation results is approximately 0.9%. Based on Fig. 8.9 and since we expect that sweet bias point to be in the reverse bias region of the body, approximately between -0.4 to -0.2, then some discrepancy between simulation results and experimental results can be predicted. Experimental results for the effect of body bias on IIP3 is shown in Fig. 8.10. As you can see from Fig. 8.8 and Fig. 8.10 the trend of change in IIP3 is the same in both of them, and also the experimental sweet point is in good agreement with simulation sweet point.The IIP3 obtained by different methods are compared in Table 8.2 for clarification.

Table 8.2: Comparison of points obtained by Volterra Method and PSS analysis

Method	IIP3 sweet point with respect to V_{BS}
Voletrra	-0.365
PSS using SpectreRF	-0.375
Experimental Result	-0.26

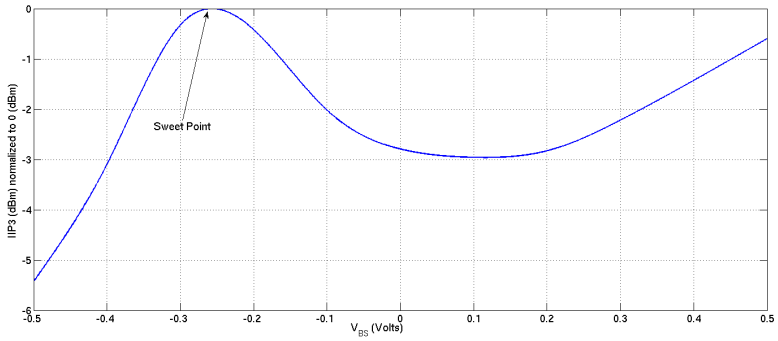


Figure 8.10: Effect of body bias in linearity performance ($f_1 = 2\,GHz, f_2 = 2.02\,GHz, V_{DS} = 1,$ and $V_{GS} = 0.5$)

8.6 Extraction Proof of Volterra Nonlinear Kernels

To get the general idea behind deriving Volterra kernels of the order higher than one the derivation behind second order Volterra kernels are shown in the following subsection:

8.6.1 Second Order Volterra Kernel

Based on (8.4) :

$$\begin{aligned}(i_d)_2 &= K_{2GM}\,(v_{gs}^2)_2 + K_{2GO}\,(v_{ds}^2)_2 + K_{2GMGO}\,(v_{gs}\,v_{ds})_2 \\ &= K_{2GM}\,(v_{gs})_1^2 + K_{2GO}\,(v_{ds})_1^2 + \\ &+ K_{2GMGO}\,(v_{gs})_1\,(v_{ds})_1 \end{aligned} \tag{8.10}$$

By using the First Order Volterra Kernel (8.3) we will have:

$$(v_{gs})_1^2 = \left(\sum_{i=1}^{2} \frac{Z_s(f_i)}{R_s} e^{(j2\pi f_i t)}\right)^2$$
$$= \sum_{i=1}^{2}\sum_{j=1}^{2} \frac{Z_s(f_i)Z_s(f_j)}{R_s^2} e^{(j2\pi(f_i+f_j)t)} \tag{8.11}$$

$$(v_{ds})_1^2 = \left(\sum_{i=1}^{2} H_1(f_i) e^{(j2\pi f_i t)}\right)^2$$
$$= \sum_{i=1}^{2}\sum_{j=1}^{2} H_1(f_i)H_1(f_j) e^{(j2\pi(f_i+f_j)t)} \tag{8.12}$$

$$(v_{gs})_1(v_{ds})_1 = \left(\sum_{i=1}^{2} \frac{Z_s(f_i)}{R_s} e^{(j2\pi f_i t)}\right)\left(\sum_{j=1}^{2} H_1(f_i) e^{(j2\pi f_j t)}\right)$$
$$= \sum_{i=1}^{2}\sum_{j=1}^{2} \frac{H_1(f_i)Z_s(f_j)}{R_s} e^{(j2\pi(f_i+f_j)t)} \tag{8.13}$$

The equation which should be solved to extract the Second Order Volterra Kernel is as follows:

$$(i_d)_2 + \frac{(v_{ds})_2}{R_L} + g_o\,(v_{ds})_2 + C_{ds}\,\frac{(dv_{ds})_2}{dt} = 0 \tag{8.14}$$

For solving the above equation we need $(v_{ds})_2$ which can be obtained by Volterra Theory as follows:

$$\underline{\textit{Based on Volterra Theory}}:$$
$$(v_{ds})_2 = \sum_{i=1}^{2}\sum_{j=1}^{2} H_2(f_i, f_j) e^{(j2\pi(f_i+f_j)t)} \tag{8.15}$$

By using the above equation we can derive $H_2(f_i, f_j)$ as follow:

$$H_2(f_i, f_j) = -\frac{K_{2GM}}{R_s^2} Z_s(f_1)Z_s(f_2)Z_L(f_1+f_2)$$
$$- K_{2GO} H_1(f_1)H_1(f_2)Z_L(f_1+f_2)$$
$$- \frac{K_{2GMGO}}{Rs}\overline{H_1(f_1)Z_s(f_2)}Z_L(f_1+f_2)$$
$$\overline{H_1(f_1)Y_s(f_2)} = \frac{1}{2!}\left(H_1(f_1)Z_s(f_2) + H_1(f_2)Z_s(f_1)\right) \tag{8.16}$$

8.7 Effect of Body Biasing on the Performance of a Radio Frequency Low Noise Amplifier

The modeling and characterization of 130-nm RF Technology was examined analytically using Voletrra theory in previous sections. It was shown that by changing the bias of the body, it is possible to get an optimum point for linearity performance. The idea was verified by both an analytic method (Volterra Method), a numerical method (PSS analysis), and experimental results. It should be mentioned that because changing the body bias could also potentially change the first term of the multi-dimensional Taylor series, which is g_m, in Equation 8.1; consequently, it can change the gain of an amplifier. Moreover, the body of a transistor acts like a back gate, so changing body voltage could potentially change the transistor's operating region, i.e., the moving transistor from an active region to a linear region or vice versa. This change in the operating region directly affects the noise performance of an amplifier. In the following sections, the effect of body bias on the noise and gain of a typical RF amplifier is discussed.

8.7.1 Schematic of a typical 2.4 GHz Low Noise Amplifier with Access to its Body

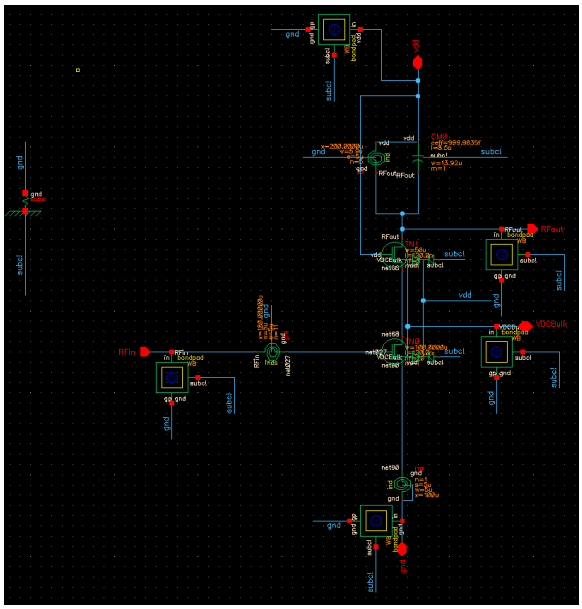
In Fig. 8.11 you can see the schematic and layout of a 2.4GHz LNA that is designed to evaluate how the change in the body bias could change the performance of the amplifier.

8.7.2 Measurement Set-Up

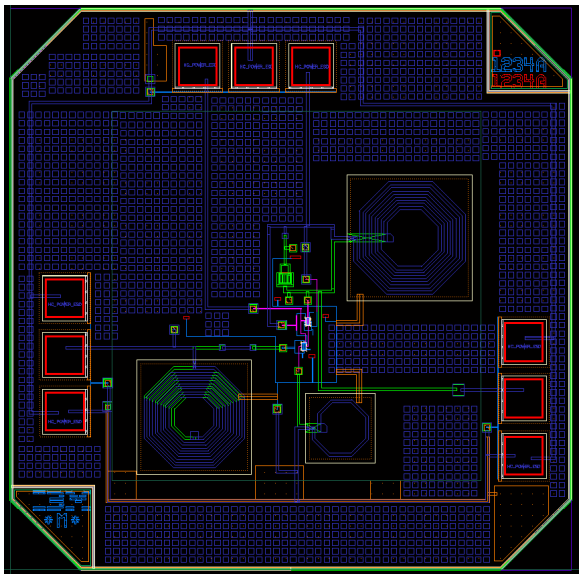
The measurement set-up for the above LNA is shown in Fig. 8.12

8.7.3 Measuring Third Order Intermodulation Distortion

For measuring the third order intermodulation distortion, two tones have been fed to the amplifier and the power of the linear product and third-order intermodulation product are measured as shown in Fig. 8.13. Fig. 8.13 shows third-order intermodulation measurement for $V_{BS} = -0.6$, and V_{BS} was changed to see the effect of body bias on the nonlinear performance of the amplifier. The change in the power value of the first harmonic and third-order intermodulation distortion is shown in Table 8.3. Using the data provided in Table 8.3, the third-order intercept point can be calculated, which is plotted in Fig. 8.14.



(a)



(b)

Figure 8.11: Schematic and layout of a typical 2.4GHz LNA designed in 130nm technology node

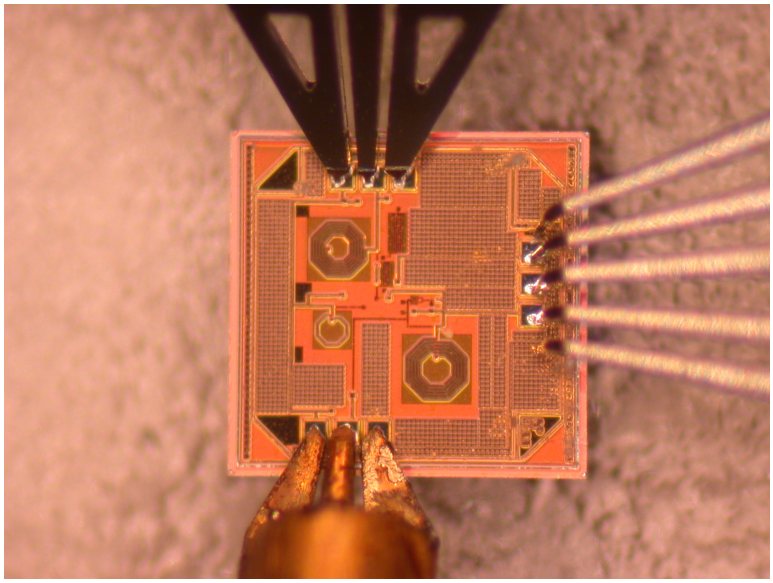


Figure 8.12: Measurement set-up to measure the performance of the designed LNA with respect to change in its body bias

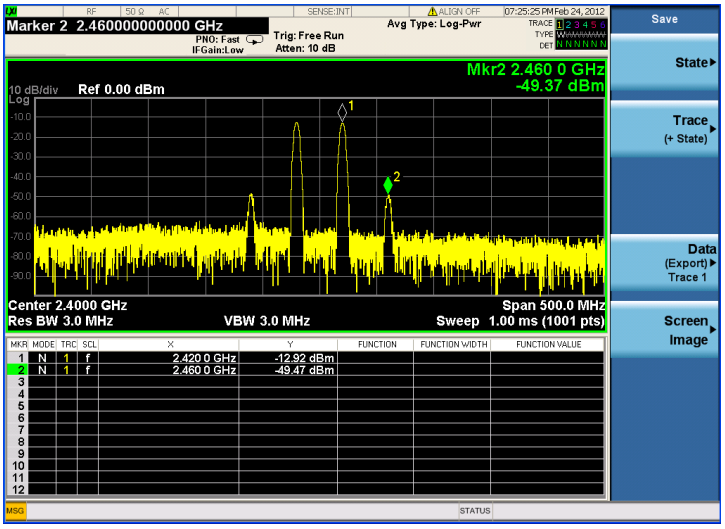


Figure 8.13: Measurement of third-order intermodulation distortion using two-tone measurement for $V_{BS} = -0.6$

Table 8.3: Change in the value of power in the first harmonic and third-order intermodulation distortion components because of change in the body bias voltage

Body bias (Voltage)	Fundamental component (First Order)	Intermodulation distortion (Third-order)
-0.6	-12.9	-50.2
-0.5	-12.5	-49.8
-0.4	-12.2	-49.6
-0.3	-11.8	-49.7
-0.2	-11.55	50
-0.1	-11.35	50.3
0	-11.1	50.5
0.1	-11	50.6
0.2	-10.9	50.6
0.3	-10.95	50.3
0.4	-11	50.1

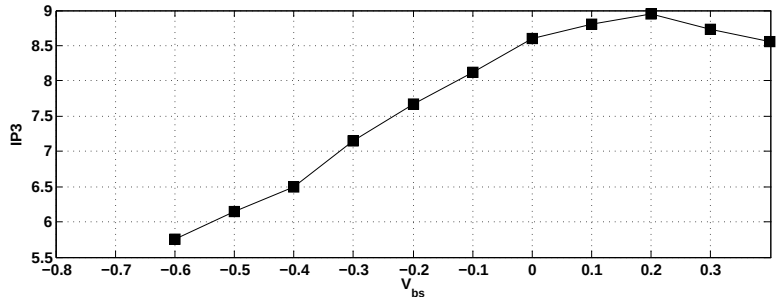
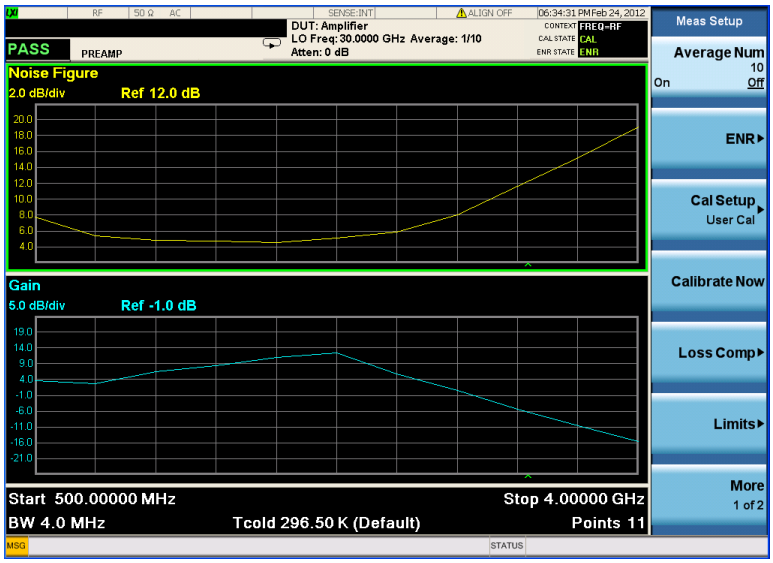


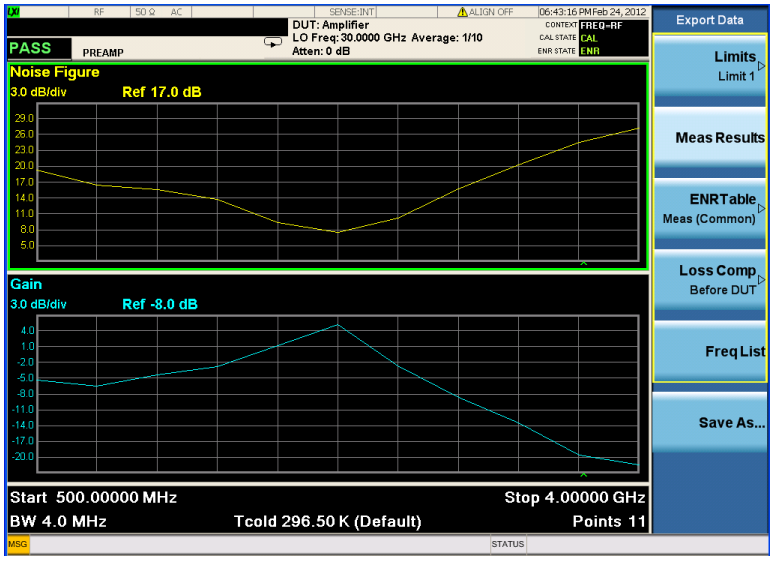
Figure 8.14: Third-order intercept point calculated using the measured data provided in Table8.3 showing the dependency on the value of body bias

8.7.4 Measuring Gain and Noise Figure of the LNA

Fig. 8.15 shows the variation of the gain and noise figure of the LNA with respect to change in the value of V_{BS}. As you can see from this figure, by increasing the value of V_{BS}, gain of the amplifier is reduced and its noise figure increases significantly. The change in the value of gain by changes in the body bias is shown in Table 8.4.



(a)



(b)

Figure 8.15: Effect of body bias on the performance of the designed LNA (a) $V_{BS} = -0.5$, (b) $V_{BS} = 0.1$

Table 8.4: Change in the value of gain because of change in the body bias voltage

Body bias voltage	Gain (dB)
-0.6	11.61
-0.5	11.63
-0.4	11.45
-0.3	10.89
-0.2	9.75
-0.1	9.04
0	7.12
0.1	6.45
0.2	4.95
0.3	3.5
0.4	0.6

8.8 Conclusion

In this chapter, we characterized the effect of changing the body-bias of a CMOS transistor on its nonlinear performance. The characterization is based on the Volterra theory. The main contributions of this work are:

- Calculated the first-, second-, and third-order Volterra kernel of a simple CMOS amplifier.
- Compared the measured and simulated I_d and extracted the variations of nonlinear conductance coefficients of I_d of a CMOS transistor with respect to changes in its body bias using the LSE method.
- Derived an analytical formula for IP_3 of the simple CMOS amplifier and compared it with the measurement results.
- Designed, fabricated, and measured the performance of an LNA to show the effects of changing the body-bias of the core transistor on the LNA performance (i.e., gain, linearity, and noise figure).

Chapter 9

Conclusion and Future Work

9.1 Research Contributions

In this thesis, we have described the structure of a radio-over-fibre link using silicon photonics and CMOS electronics. This approach is promising in delivering high performance and low cost systems using few physical parts. By using a digital baseband optical transmission approach, the optical links can be implemented using well established silicon photonics technology. Silicon photonic links in excess of 40 Gbps have already been commercialized, and the optical part of the system takes advantage of these developments. We talked about about challenges and constraints of an electro-optical design not only in the areas such as modelling and analysis but also in the areas of Computer Aided Designed (CAD) tools aimed for the integration of electrical and optical simulation tools. An efficient and reliable CAD tool that could support both electronic and photonic components with regards to simulation, layout, design rule check (DRC), Layout Versus Schematic (LVS), and statistical analysis is a crucial step to move from a few hundred photonic components in a Photonic Integrated Circuit (PIC) to millions of them in a PIC. This work paves the way for implementing complete wireless-photonic systems based on integrated silicon photonics and CMOS electronics.

In Chapter 3 and 4, an integrated electronic/photonic design automation (EPDA) environment is developed. This EPDA is designed and developed to support Photonic Integrated Circuit (PIC) designers to work on their electro-optical design in a single/central environment. The environment is developed around Cadence Virtuoso custom design platform. Different algorithms and data structures used in the development of the environment are discussed in these chapters.

In Chapter 6, the high frequency modelling of electro-optical elements are discussed. The electrical modelling of an optical ring modulator, which is fabricated in a photonic process, is derived. A methodology to extract compact electrical model for this component is discussed and measurement results are used to extract the electrical compact model and to validate the proposed methodology. It is shown that the inductor, as a passive elements

that could be used to enhance bandwidth, could be directly implemented in the photonic process and its performance could be enhanced by silicon-etching techniques. The design, implementation and post-layout simulation of a $25Gbps$ CMOS driver is shown that is used to drive the derived electrical compact model of the fabricated optical ring modulator.

In Chapter 7, harmonic balance method, as a main analysis tool for nonlinear electronic circuits, is examined. The convergence of this method is discussed and a new method based on Volterra kernels is proposed to improve the convergence of harmonic balance method. It is shown that the initial condition provided by this method can be derived based on analytical equations.

In Chapter 8, the effect of body bias on the overall performance of an electronic circuit is examined. This examination is based on modelling and characterizing of $130nm$ RF technology using Volterra theory. It is shown that body bias could be an effect tool to tune the performance of an electronic circuit, such as a Low Noise Amplifier (LNA). Analytical, simulation and measurement results are provided to support the idea.

9.2 Future Work

The EPDA developed in Chapter 3 and 4 is the building block of a complete EPDA tool. This complete EPDA could support schematic or layout-driven design flows for PICs; it could be used to extract photonic component parameters and generate compact model for them. This EPDA could support photonic mask layout implementation for PICs. Further collaboration with companies supporting photonic integrated circuit fabrication is required to create a Process Design Kit (PDK) for each relevant photonic process.

As mentioned in Chapter 6 the operating bandwidth of a TIA detector could be enhanced by using an indcutor to compensate the capacitive behaviour of the photo detector. Based on developed methodology in this chapter, an inductor could be implemented near the photodetecotr for the front-end of an optical receiver to enhance the operating bandwidth of the receiver.

As discussed in Chapter 7, Volterra kernels could be used to generate an initial starting point for harmonic balance analysis. This technique could be also be used in Periodic Steady State (PSS) analysis to evaluate its effectiveness and to develop faster solution algorithms for analysis of string nonlinear circuits.

As shown in Chapter 8, body bias could be used an effective tool to

tune the performance of electronic circuits. This needs to be investigated further for each CMOS circuit and topology. For instance, body bias could be used to tune the tail current of CML drivers in each stage of the designed CMOS driver in this chapter and by tuning the tail current, we can make sure that the transistors are bias in the right region for proper operation of the driver.

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Appendix A

On the Design and Temperature Performance of Mach-Zehender Interferometer

In this section, a methodology to design an asymmetric Mach-Zehnder interferometer (MZI) is discussed, its measurement results is presented and its performance with respect to temperature variation is analyzed. The design methodology contains three sub-sections in which each sub-section is a separate component that is designed and simulated on its own. The sub-sections includes the design and simulations of: waveguide by using effective-index-method (EIM), power splitter, coupler, and phase shifter; these components are simulated using 2-D finite-difference time-domain (FDTD) method and are used to make the final MZI. Final design is analyzed and simulated by full 3-D FDTD method for verification purpose and final tuning. The fabrication is done using IMEC photonic process: silicon-on-insulator, 220-nm top Silicon film, 2000-nm buried oxide.

A.1 Introduction

Mach-Zehnder Interferometer (MZI), a typical external modulator, is the building block in most of the electro-optic modulators (EOM); considering the deficiencies in internal modulators such as: turn-on delay, frequency chirping, and relaxation oscillation; making an integrated silicon photonics links working beyond 50Gbps [175] wouldn't be feasible without using external modulators such as Mach-Zehnder interferometer. Mach-Zehnder interferometer not only can be used as the building block of an optical modulator but also it could be used as the building block of optical filters [176]. Assumptions in the design of an integrated optical filter that has Finite Impulse Response (FIR) or all-zero type optical filters is that Asymmetric

Mach-Zehender interferometers are used as the building blocks to generate variable phase shifts and there is no feedback in the structure of the integrated optical filter; otherwise, the designed filter will be categorized as an Infinite Impulse Response (IIR); these filter are mainly designed using ring resonators [176].

Having said that, There are many challenges moving from discrete optics to integrated silicon photonics such as modelling, simulation, and verification of different basic optical blocks such as light source block, guiding block, modulator block, detection block. The final design also needs tuning methods to compensate the uncertainties in the fabrication such as dimension of the optical components. One efficient method for tuning photonic devices is temperature, then evaluating photonic component's behaviour under temperature variation, both as a tuning tool and performance indicator, is crucial.

Asymmetric MZI not only is used in the design of an integrated optical filter but also is used in applications such as Wavelength division multiplexing (WDM) switching [177, 178], networking [179], and experiments on the light speed [180]. The role of an assymetric MZI as the building block of a Photonic Integrated Circuit (PIC), specially integrated optical filters, makes its modelling, simulation, and verification of its behaviour crucial. The first part of this paper is devoted to explain the role of an asymmetric MZI as the building block of a multi-stage integrated optical filter having finite impulse response; subsequently, methodology used to design an asymmetric MZI will be explained. The proposed methodology is divided into three sections: (a) using effective-index-method to calculate the effective propagation constant and consequently the length of the asymmetric section [181, 182], (b)the final structure including waveguides, power splitter, coupler and phase shifter are designed and simulated using 2-D FDTD [183] (the design is tuned to get an optimum result) (c)the final structure is simulated using 3-D FDTD to compare with the results of 2-D FDTD. In the second part of the paper the measurement results is presented, and the effect of temperature variation on the performance of the device is depicted.

A.2 Asymmetric MZI as the Bulding Block of FIR Optical Filters

Fig. A.1 shows the structure of an stage of a multi-stage FIR optical filter. As you can see the asymmetric MZI play the main role shaping the response of the multi-stage filter. Considering the transfer matrix representation of

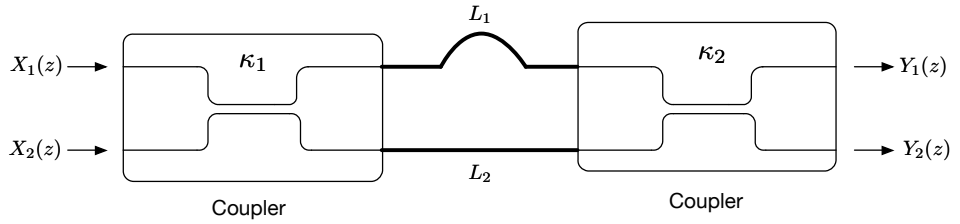


Figure A.1: Single stage of a multiple-stage integrated optical filter having finite impulse response

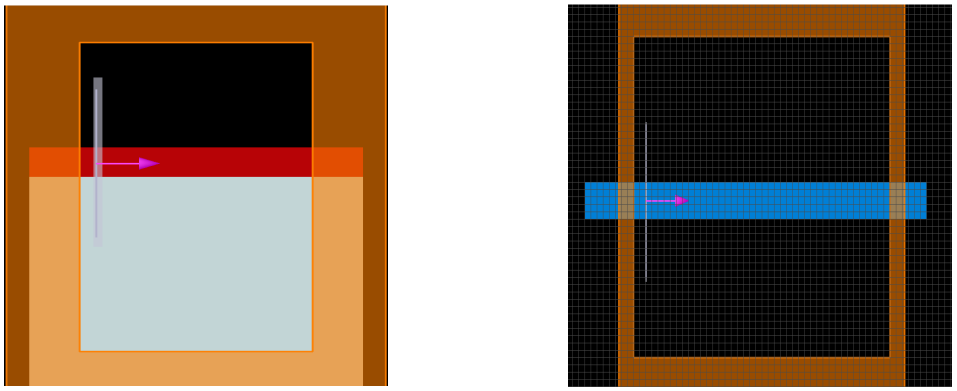
the input and output coupler and the asymmetric optical waveguides in the structure, the overall transfer matrix could be derived as in A.1. In A.1, s and$c$ represent cross- and through-port transmission coefficient of the directional coupler receptively. In the next section the first directional couple is substituted by an optical splitter; this could be represented in the transfer matrix representation by assuming $X_2(z) = 0$ and $s = c = \frac{1}{2}$. As mentioned before the structure in Fig.A.1 is a single stage of a multiple-stage FIR filter. Adding more stages will increase the degree of the filter and its overall transfer matrix could be modelled by multiplying the transfer matrix representation of each stage.

$$\begin{bmatrix} Y_1 \\ Y_2 \end{bmatrix} = \gamma \begin{bmatrix} -s^2 + c^2 z^{-1} & -jcs(a + z^{-1}) \\ -jcs(a + z^{-1}) & c_1 c_2 - s_1 s_2 z^{-1} \end{bmatrix} \begin{bmatrix} X_1 \\ X_2 \end{bmatrix} \tag{A.1}$$

A.3 Modelling, Simulation and Verification of MZI

A.3.1 Effective Index Method

Exact solution of Maxwell's equations for step-index slab waveguide has been shown to be obtainable; however, there are many practical integrated-optic like rectangular core step-index waveguide that there is no exact solution for them. Although attempts have been made to find a rigorous approximate solution, ad-hoc technique such as effective- index-method can be used to get an approximate effective index of a waveguide with less computational time and good accuracy. This effective index is used to calculate phase shift for different physical lengths of the waveguide. A key parameter in the design of a MZI is the specific amount of phase shift, π, required for one of the



(a) (b)

Figure A.2: Deriving effective refractive index using EIM (structures were simulated by Lumerical's FDTD Solutions package [184]): (a) 2-D simulated structure used as the first step to calculate effective index by EIM, (b) Final 2-D simulated structure used as the last step to calculate effective index by EIM

branches of MZI with respect to the other that can be derived by (A.2).

$$\text{phase shift} = \beta l = \frac{2\pi n_{eff} l}{\lambda} \tag{A.2}$$

Two structures required to be simulated for the EIM method are shown in Fig. A.2. Variation of effective refractive index by increasing FDTD's mesh accuracy (a bigger number means a finer mesh) is shown in Fig. A.3. The effective refractive index's relative error is calculated using (A.3); Table A.1 shows both the relative error and average value of effective refractive index, which are calculated based on different FDTD's mesh sizes, for each wavelength. Considering fabrication uncertainties and also effective refractive index's relative error, average value of effective refractive index (with good approximation) can be used for subsequent design process.

$$\begin{aligned} \text{Relative Error} &= \text{RE,Effective Refractive Index} = \text{ERI} \\ \text{RE} &= \frac{\text{max(ERI)-average(ERI)}}{\text{average(ERI)}} \times 100 \end{aligned} \tag{A.3}$$

A.3.2 Power Splitter

The structure of $50\%-50\%$ power splitter is shown in Fig. A.4. It is shown in

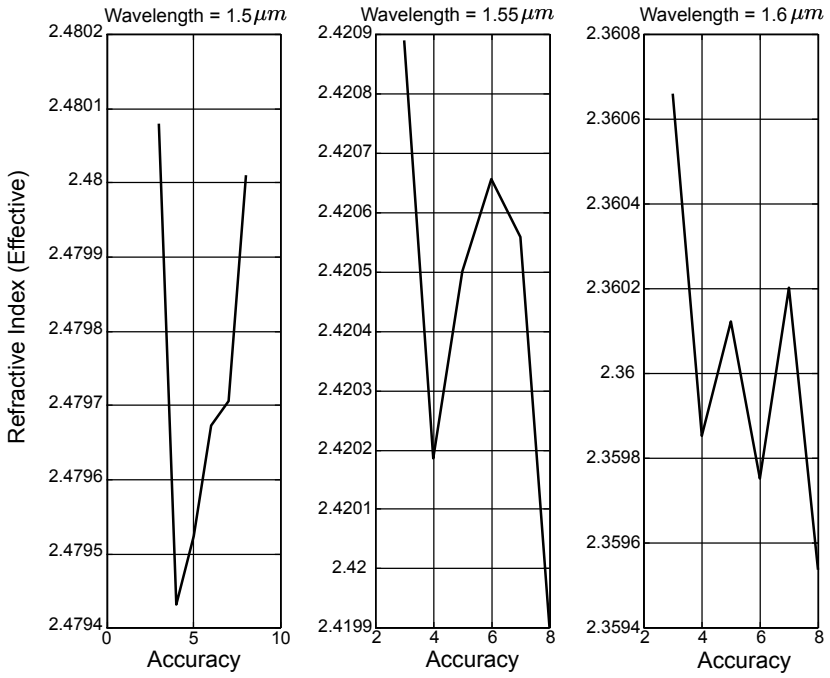


Figure A.3: Dependency of effective refractive index on FDTD's mesh accuracy for different wavelengths

Table A.1: Effective Refractive Index's Relative Error and Average (FDTD's Mesh Accuracy has been changed to calculate Relative Error)

Wavelength	Relative Error	Average Effective Index
$1.5\mu m$	0.014%	2.48
$1.55\mu m$	0.018%	2.42
$1.6\mu m$	0.028%	2.36

Fig. A.5 that by increasing Total_Y and decreasing Total_X and Bend_X, i.e. making the bend sharper, radiation because of this sharpness will increase; consequently, the amount of power in each branch will decrease; power profile of the structure in Fig. A.5b is shown in Fig. A.6.

A.3.3 Power Coupler

The structure of $50\% - 50\%$ power coupler is shown in Fig. A.7. Simulation

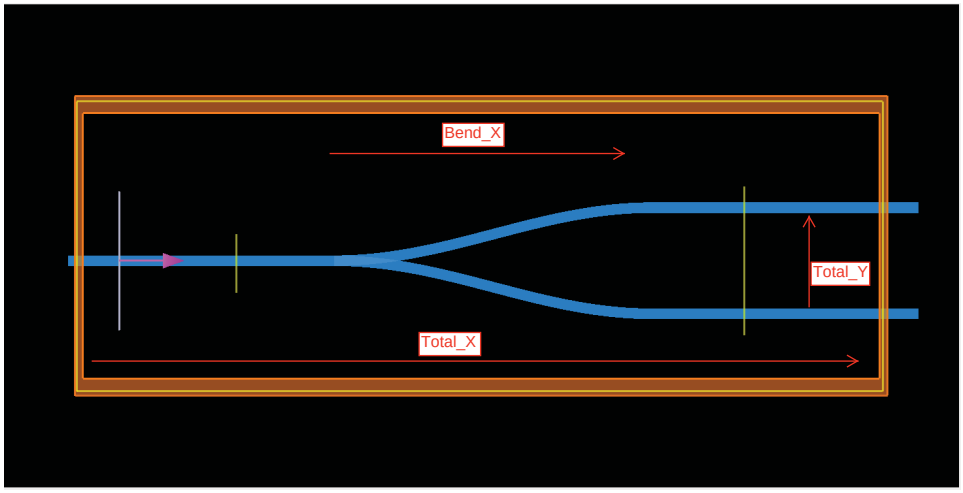
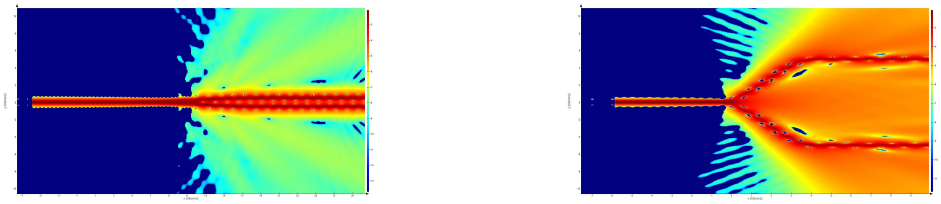


Figure A.4: 2-D Structure of power splitter; the distance between branches have effect on the performance of the power splitter



(a) (b)

Figure A.5: Bend sharpness' effect on the its radiation: 2-D Power Flow (Px) (Logarithmic Scale) (a) Total_Y=1μm, Total_X=40μm, and Bend_X=15μm, (b) Total_Y=5μm, Total_X=20μm, and Bend_X=10μm

results using different values for "Couple Length" are shown in Fig. A.8. The results shown in Fig. A.8 have been obtained where the light source, propagation mode, has injected from down branch; The results of using up branch injection are shown in Fig. A.9. In both of Fig. A.8 and Fig. A.9, simulation wavelength has set to 1.5μm. To get nearly equal power division from both up and down branch, according to Fig. A.8 and Fig. A.9, the "Coupler Length" is set to 9.7μm (refer to Fig. A.9(c,d)).

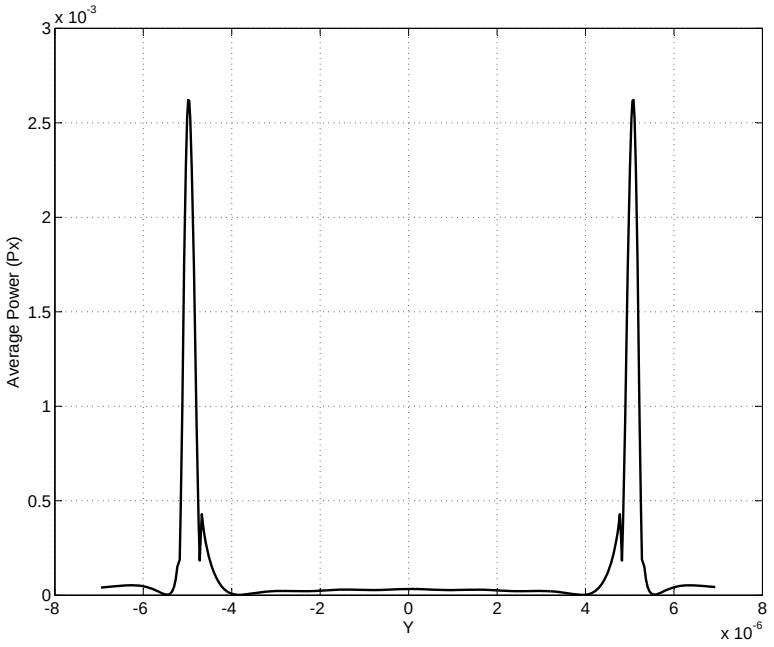


Figure A.6: 1-D power profile (Px) of power splitter: Total_Y=5μm, Total_X=20μm, and Bend_X=10μm

A.3.4 Final Structure

In the previous sections, the performance of different components of a MZI has been examined; in this section all of those components will be combined to make a MZI. The schematic of MZI is shown in Fig. A.10. In Fig. A.10, the section shown by an ellipse, "Phase Shifter", creates the required phase shift. To be able to change the length of this section, the whole section acts like a parametrized cell; simulation results are shown in Fig. A.11; as you can see from Fig. A.11 the optimum length for the "Phase Shifter" section is near 3.43μm (refer to Fig. A.11 (d)). To see the performance of the MZI in other wavelengths, the structure has been simulated at wavelength=1.55μm and 1.6μm; the result of simulation is shown in Fig. A.12. It can bee seen from Fig. A.12 that the tuned MZI is working properly: in wavelength=1.5μm and 1.6μm nearly all of the power are coming out of the down branch and at wavelength= 1.55μm most of the power are coming out of up branch; to

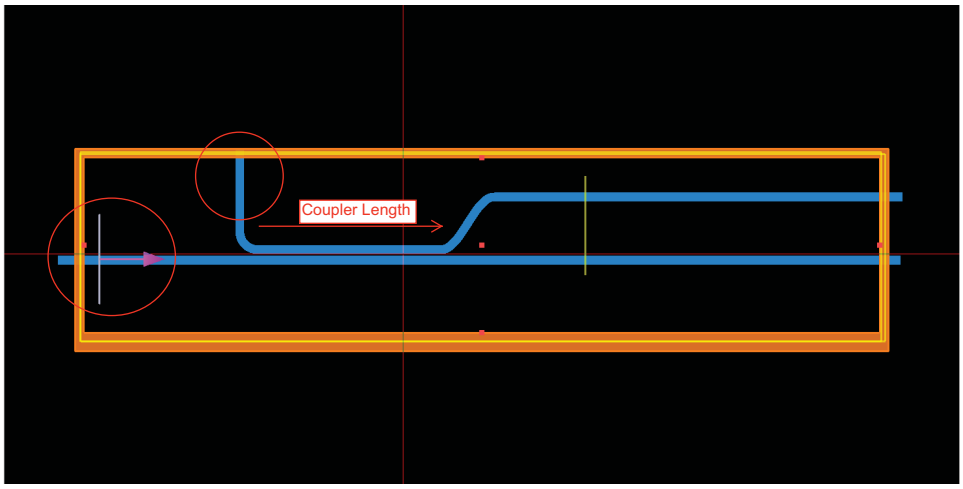


Figure A.7: 2-D Structure of the coupler; to get $50\% - 50\%$ performance from the coupler the "Coupler Length" has been swept for different position of the source

Table A.2: Effective Refractive Index Based on 2-D and 3-D FDTD at Different Wavelengths (FDTD's Mesh Accuracy for 3-D Simulation Was Set to 4)

	Effective Index 2-D	Effective Index 3-D
wavelength=$1.5\mu m$	2.48	2.44
wavelength=$1.6\mu m$	2.36	2.29

get a better understanding of this switching behaviour, 2-D power profiles of the MZI are shown in Fig. A.13 for different wavelengths. 3-D structure of the final MZI is shown in Fig. A.14; to verify previous results and make the final tuning, the effective refractive index has been calculated using full 3-D FDTD. The difference between two effective refractive indices is shown in Table A.2. Based on the 3-D refractive index, the length of the "Phase Shifter" for MZI's proper switching behaviour was calculated, and the final design was submitted for fabrication based on that.

A.4 Measurement Results

Fabricated die photo is shown in Fig. A.15, and measurement results calculated as the measured power difference between the top and bottom branch are shown Fig. A.16. These measurements have been done for temperatures

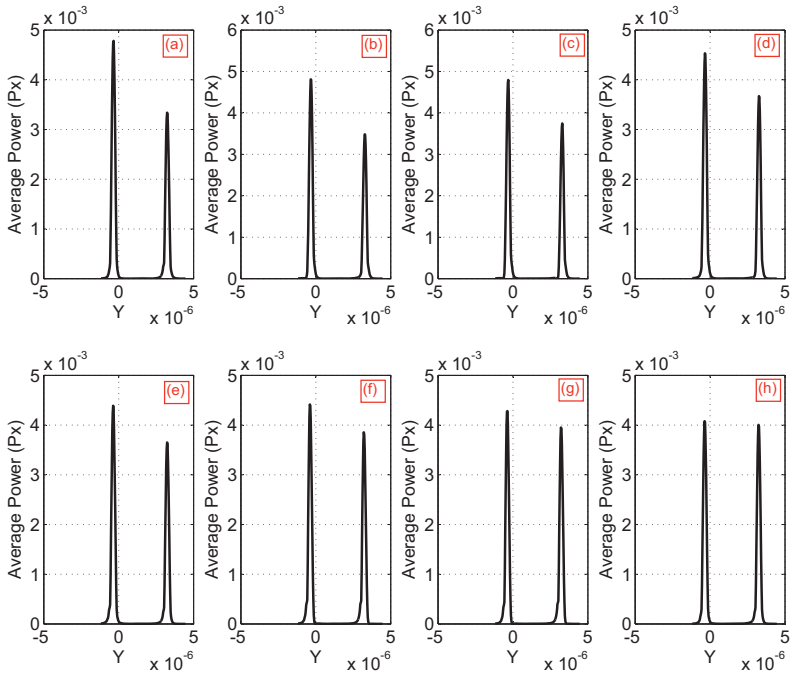


Figure A.8: Coupler performance for different values of "Couple Length" (source has been Injected from down branch):(a)9.3μm (b)9.472μm (c)9.643μm (d)9.814μm (e)9.986μm (f)10.016μm (g)10.329μm (g)10.5μm

Table A.3: Wavelength Values, for Different Temperatures, where the Power Difference Between Two Branches Attains its Minimum and Maximum (refer to Fig. A.16)

Temperature	Minimum	Maximum	Minimum
$20°C$	$1558nm$	$1576nm$	$1590nm$
$40°C$	$1560nm$	$1578nm$	$1592nm$

ranging from $20°C$ to $40°C$. Fig. A.16 shows the measurement results for $20°C$, $27.5°C$, and $40°C$. Table A.3 shows the wavelength values, for different temperatures, where the power difference between two branches attains its minimum and maximum. As you can see from Table A.3, the rate of change for the switching behaviour of the MZI with respect to temperature is approximately $0.1nm/°C$.

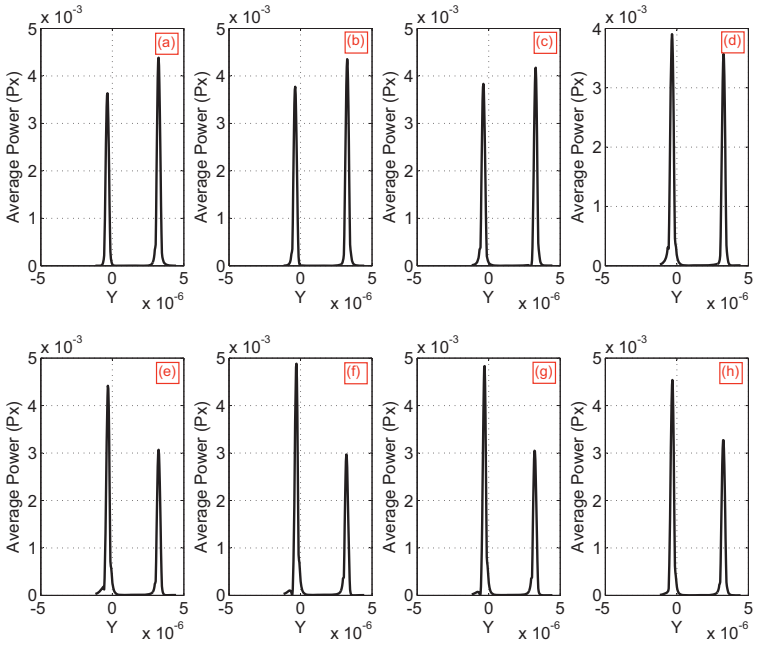


Figure A.9: Coupler performance for different values of "Couple Length" (source has been Injected from up branch):(a) $9.3\mu m$ (b) $9.472\mu m$ (c) $9.643\mu m$ (d) $9.814\mu m$ (e) $9.986\mu m$ (f) $10.016\mu m$ (g) $10.329\mu m$ (h) $10.5\mu m$

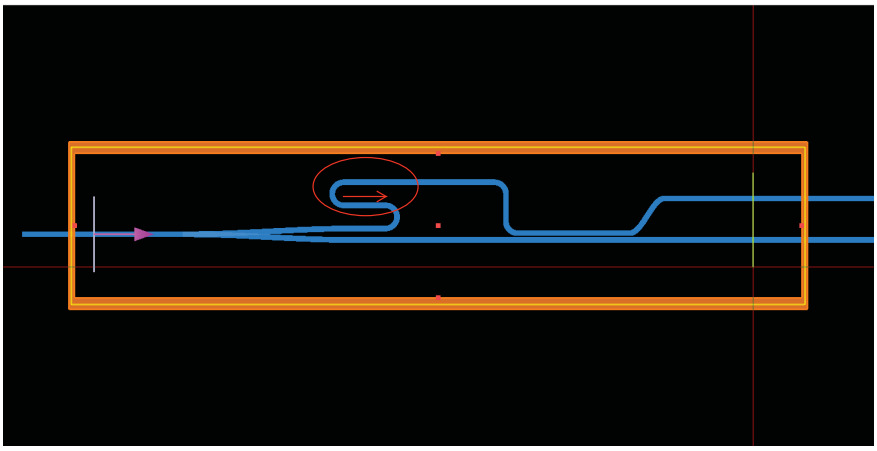


Figure A.10: 2-D Structure used to analyze MZI

A.5 Conclusion

In this paper the methodology to design an asymmetric MZI has been discussed; performance of different components used in the design of MZI has been simulated, and at the end the final design based on 3-D FDTD simulations was used for fabrication purpose. Measurements have been done on the fabricated structure to see its general behaviour and also its performance with respect to temperature variation. As it can been seen from both Fig. A.16 and Fig. A.13 the general behaviour of simulated structure and fabricated one is almost the same; however, in 2-D simulation results power different between two branched, up branch minus down branch, will be maximized at wavelength = $1.55\mu m$ however in the measurement results it will be maximized at wavelength = $1.576\mu m$. It was shown that the switching behaviour of the MZI depends on the temperature, $0.1nm/^{\circ}C$, however this dependency is not significant.

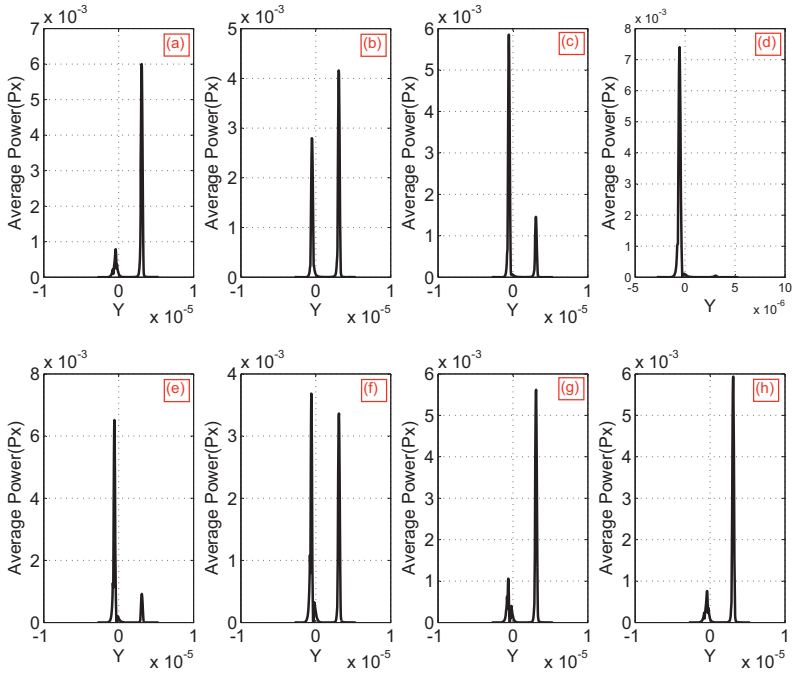


Figure A.11: Performance of the MZI for different length of the "Phase Shifter" section (Refer to Fig. A.10): (a) Length=3.3μm (b) Length = 3.35μm (c) Length = 3.39μm (d) Length = 3.43μm (e) Length = 3.47μm (f) Length = 3.52μm (g) Length = 3.56μm (h) Length = 3.6μm

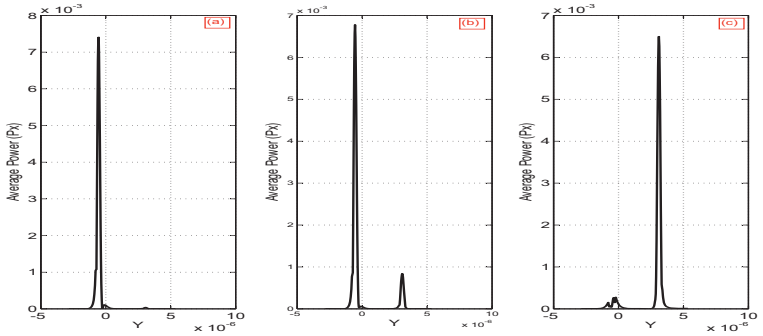
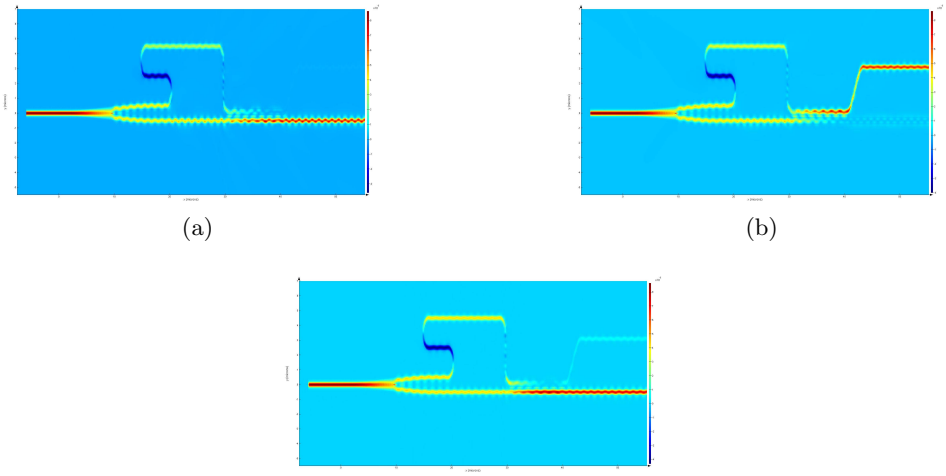


Figure A.12: Simulation of tuned MZI at other wavelengths: (a) Wavelentgh = 1.5μm (b) Wavelentgh = 1.6μm (c) Wavelentgh = 1.55μm



(a) (b)

(c)

Figure A.13: 2-D Power Profile (Px) of the MZI: (a) wavelength=1.5μm (b) wavelength=1.55μm, and (c) wavelength=1.6μm

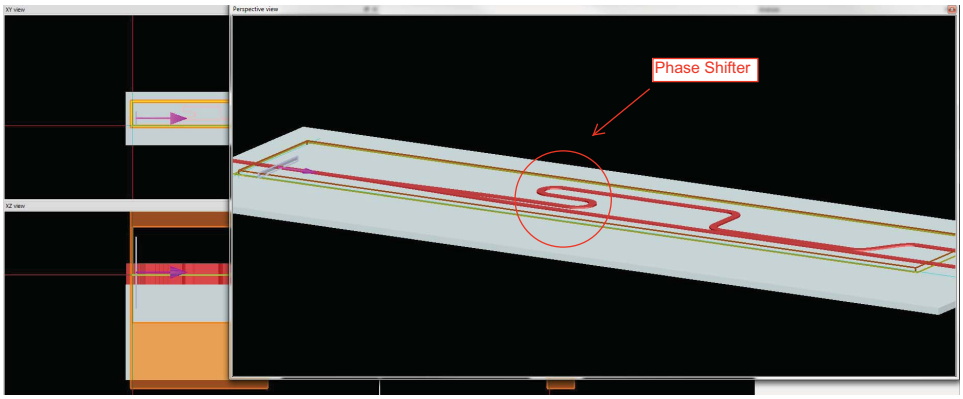


Figure A.14: 3-D Structure used to simulate Mach-Zehnder interferometer(MZI) using 3-D FDTD

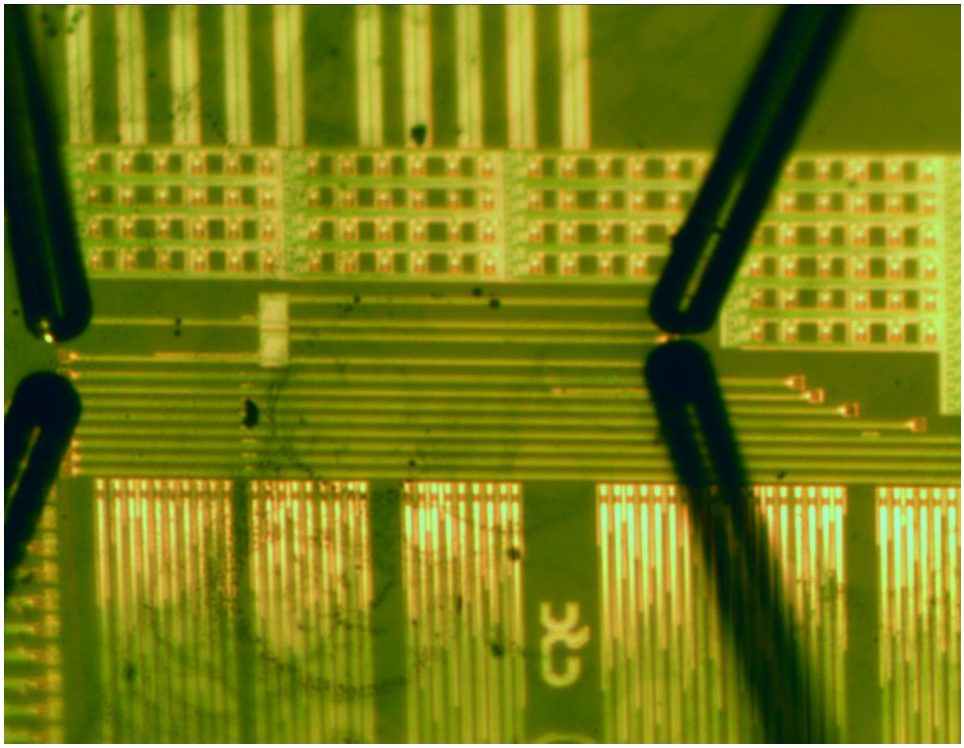


Figure A.15: Fabricated design in IMEC photonic process: silicon-on-insulator, 220-nm top Silicon film, 2000-nm buried oxide

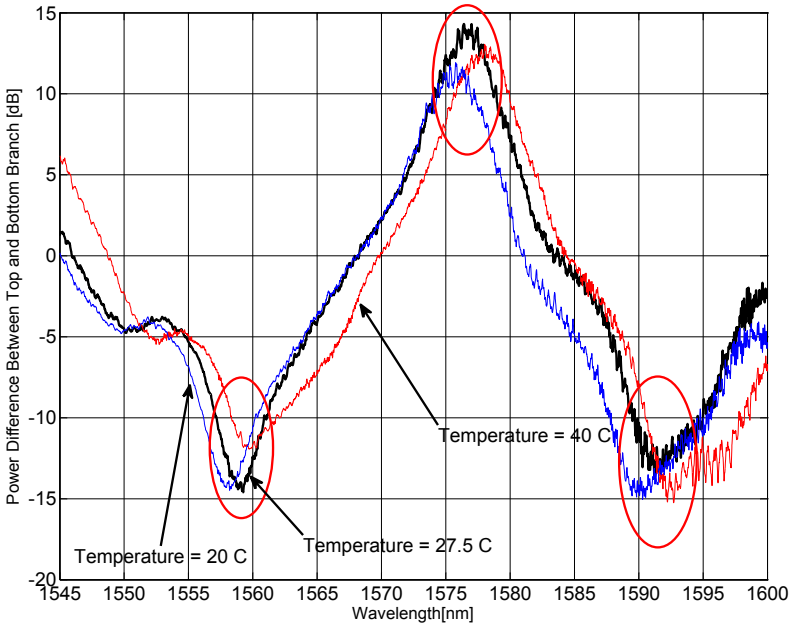


Figure A.16: Measurement results: power difference between the top and bottom branch for temprature (a) $20°C$, (b) $27.5°C$, and (c) $40°C$

Appendix B

Unified Modelling Language (UML) Diagrams of INTERCONNECT-Cadence Integration Package

In the following, some UML diagrams of INTERCONNECT-Cadence integration is shown. The two diagrams that are shown below are related to class ans sequence diagram.

B.1 UML Class Diagram

The relationships between some of the defined classes in the integration package and OASIS classes are shown in Fig. B.1.

B.2 UML Sequence Diagram

Two of important use cases that an ADE user could benefit from are specifying INTERCONNECT as the simulation engine instead of Spectre, which is the default one; and generating optical netlist and run optical simulation inside ADE. These sequence diagrams of these use cases are shown in Fig. B.2 and Fig. B.3 respectively.

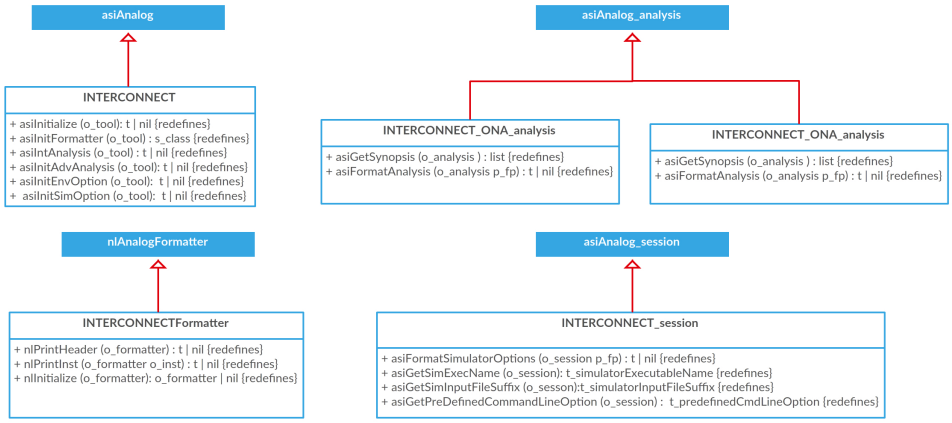


Figure B.1: UML class diagram of some classes used in the INTERCONNECT-Cadence Integration package

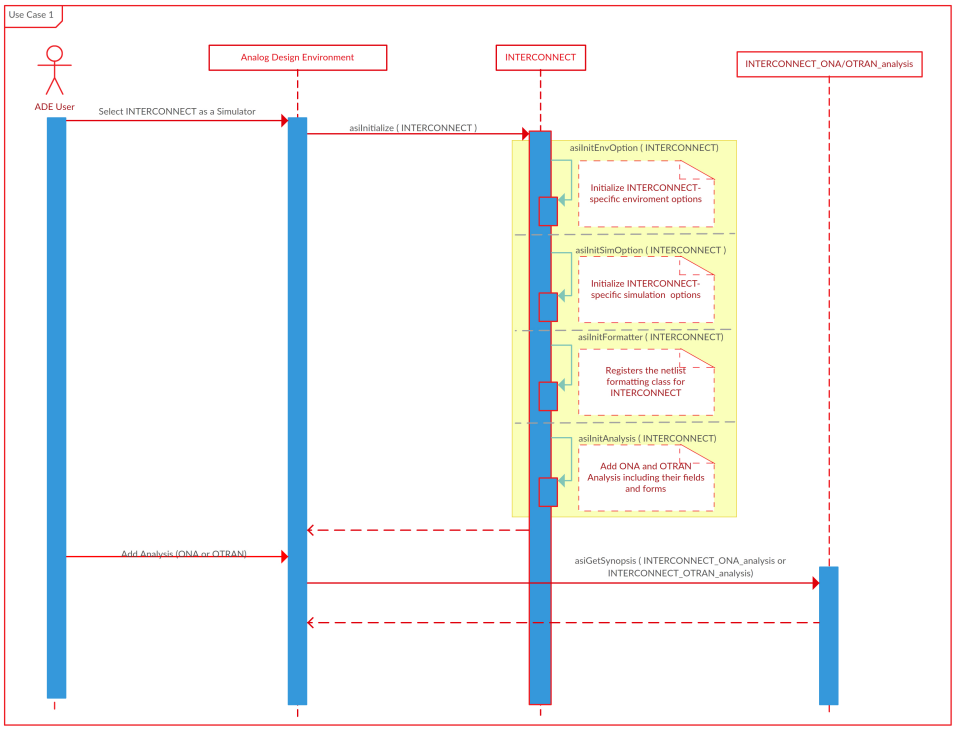


Figure B.2: Use Case: Select INTERCONNECT as the simulator inside Analog Design Environment (ADE)

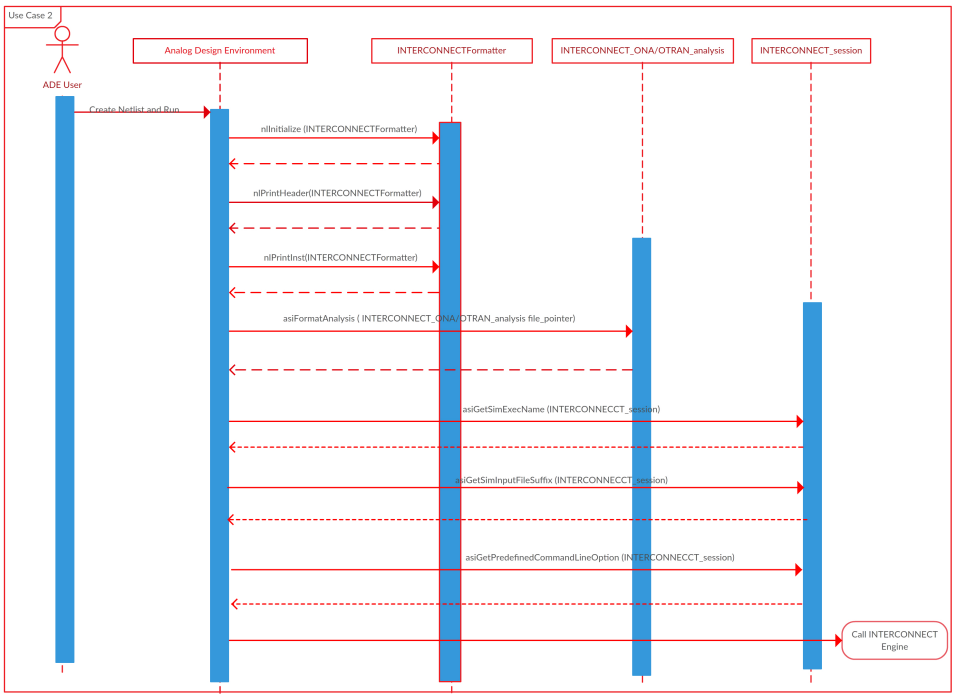


Figure B.3: Use Case: Create netlist and run inside Analog Design Environment (ADE)