INVESTIGATION OF BRIDGELESS SINGLE-PHASE SOLUTIONS FOR AC-DC POWER FACTOR CORRECTED CONVERTERS

by

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Abstract

In modern power supplies and battery chargers, a front-end power factor correction (PFC) AC-DC converter is used to comply with regulatory requirements for input current harmonics. The prevalence of standards and recommended practices to meet harmonic current limits has gained, and continues to gain, momentum over recent years. Additionally, the improvement of overall converter efficiency is critical for the emergence and acceptance of these converter technologies, to meet the standard of efficiency and power factor requirements.

This dissertation presents some innovative solutions for bridgeless non-isolated and isolated PFC AC-DC converters. All proposed converter solutions realize bridgeless converter operation to reduce conduction losses and operate in hybrid resonant pulse-width-modulation (HRPWM) mode. The PWM switches share the same gating signal, so the converter does not need extra circuitry to sense the positive and negative ac input line-cycle operation.

The first contribution is a non-isolated bridgeless AC-DC converter, which has inherent inrush current-limiting capabilities. The converter architecture also enables simple implementation of lightning and surge protection systems. Moreover, this converter can survive sustained over-voltage events and can limit the voltage stress on the converter and downstream components.

The second contribution is a non-isolated bridgeless AC-DC converter, which realizes soft-switching operation to reduce switching losses. This converter can operate at high switching frequency to increase power density.

The third contribution is a three-level non-isolated bridgeless AC-DC converter, which has high voltage gain. This converter also provides soft-switching operation of all the power devices. Due to the three level architecture, all commutations occur with a voltage level equivalent to half the output voltage, which further reduces switching losses. This converter can utilize lower voltage rated devices, which reduces system cost.

The final contribution is a single-stage bridgeless isolated AC-DC converter. This converter shows low conduction loss due to bridgeless operation and low voltage stress of the secondary diodes, low switching loss due to soft-switching operation, and a transformer that has no dc magnetizing current and does not store energy. These characteristics minimize the transformer size and increases transformer efficiency.

Preface

I am the lead investigator for this research work, responsible for performing literature survey, topology investigation, theoretical analysis, design, simulation and experimentation. This work was done under the guidance of my thesis supervisor Dr. Wilson Eberle. This work was also supervised by Dr. Fariborz Musavi, Dr. Deepak Gautam, Mr. Chris Botting and Mr. Nicholas Dohmeier of Delta-Q Technologies Corp. This thesis contains four contribution chapters that present results that have been published or going to be submitted for consideration in the form of IEEE refereed papers and scientific journals of which I am the lead author.

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List of Abbreviations

AC, ac	Alternating Current
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
DC, dc	Direct Current
DCM	Discontinuous Conduction Mode
EMI, emi	Electro-Magnetic Interference
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
RMS, rms	Root Mean Square
SiC	Silicon Carbide
TCM	Triangular Conduction Mode
VA	Volt-Ampere
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Prefixes for SI Units

G	Giga (10^{9})
k	Kilo (10^{3})
M	Mega (10^{6})
m	Milli (10^{-3})
n	Nano (10^{-9})
p	Pico (10^{-12})
µ	Micro (10^{-6})

SI Units

A	Amperes
C	Coulombs
F	Farads
H	Henries
Hz	Hertz
s	seconds

V	Volts
W	Watts
Ω	Ohms
°	Degrees

Acknowledgements

I would like to give my extended gratitude to my supervisor, Dr. Wilson Eberle, for his patience and guidance throughout my graduate studies. Most of all, I would like to thank him for giving me this opportunity and providing me with the support to expand my knowledge and participate in this rewarding field. I would also like to thank all of my past and present colleagues from Delta-Q Technologies. In particular, I would like to thank Chris Botting, Deepak Gautam, Marian Craciun, Colin Lee, Steve Blaine, Fariborz Musavi and Murray Edington for all their support and valuable discussions on several topics.

Additionally, I would like to thank my graduate classmates and friends, Colin Clark, Wayne Lu and Hamidreza Hafezinasab, for their help and valuable discussions on several topics. I would also like to thank Delta-Q for allowing me their generous use of personnel and lab space at their Burnaby office.

I thank my family for their love, care and patient over the years. Special gratitude and appreciation goes to my wife, Sharmin Akhtar, who has stood with me and positively influenced my life. Her encouragement has always been a comfort to me whenever I was undergoing hardships.

Thanks and praise be to God, who makes all things possible. He is my provider and His grace is sufficient for me. To Him be all the glory and love.

To my family

1 Introduction

The front-end AC-DC converter is a key component of power supplies and battery charger systems [1]. AC-DC converters are found in a wide variety of industrial and consumer electronics products such as battery chargers for industrial and automotive systems, telecommunication rectifiers, cellular phones, and personal computers. As the adoption rate of these products increases, the stress on the utility grid is projected to increase significantly at times of peak demand. Therefore, efficient and high power factor charging is critical in order to minimize the utility load stress, and reduce the charging time. In addition, a high power factor is needed to limit the input current harmonics drawn by these chargers and to meet regulatory standards, such as IEC 61000-3-2 [2]. This thesis focuses on high-performance single-phase solutions for non-isolated and isolated AC-DC power factor corrected converters.

A variety of circuit topologies and control methods have been developed for the PFC application [3]-[6]. Single-phase active PFC techniques can be divided into two categories: the single-stage approach and the two-stage approach. In both cases, due to safety regulations, since both the line voltage and the intermediate bus voltage are at hazardous voltage levels, galvanic isolation (usually achieved using an isolation transformer) is required to keep the (generally much lower) output voltage touch-safe (i.e. less than 60 V). The single-stage approach is suitable for low power applications where power is processed in one stage that includes an isolation transformer. In the two-stage approach, power is processed first by a front-end PFC stage, followed by a second DC-DC converter stage and the isolation transformer is usually included in DC-DC converter.

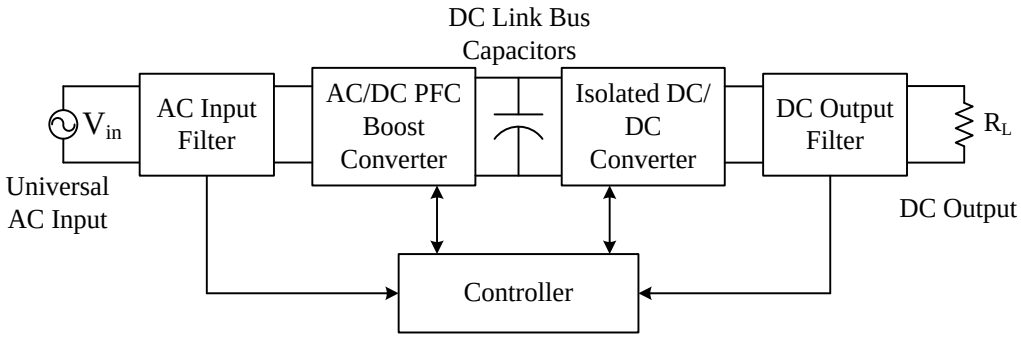


Figure 1.1 Simplified system block diagram of a universal two-stage converter system.

Figure 1.1 illustrates a simplified block diagram of a universal input two-stage PFC technique. The PFC stage rectifies the input AC voltage and transfers it into a regulated intermediate DC link bus. The converter is controlled to shape the input current for near-unity power factor. The following DC-DC stage then converts the DC bus voltage into a regulated output DC voltage, which is required to meet the regulation and transient requirements.

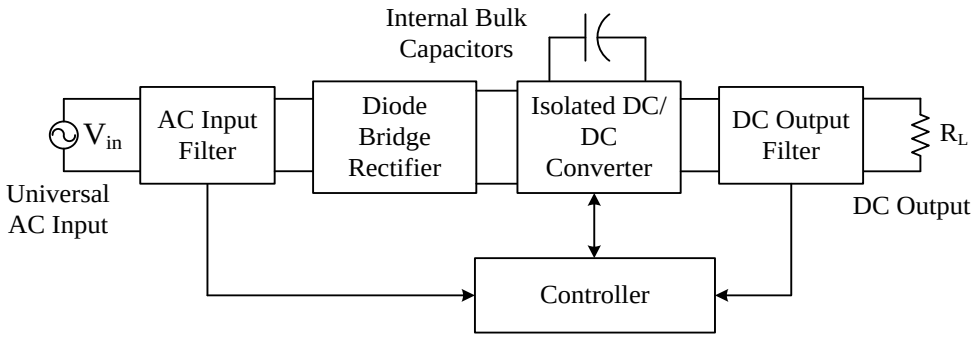


Figure 1.2 Simplified system block diagram of a universal single-stage converter system.

Figure 1.2 illustrates a simplified block diagram of a universal input single-stage PFC technique. In a single-stage converter there is no dedicated PFC converter in the front end. The isolated DC-DC converter with diode bridge rectifier in the front end both controls shaping of the input current to achieve near-unity power factor and regulates the output voltage. An internal bulk capacitor is used to handle the instantaneous

difference in power between the input pulsating power and the constant output power. Unlike in the two-stage PFC converter, the bulk-capacitor voltage in the single-stage converter is not regulated since the control freedoms are reduced by the integration of the PFC AC-DC and DC-DC switches into one single switch.

1.1 General Background

Power quality is an important concept in the design and analysis of AC-DC converters [7]. In this section, an overview of total harmonic distortion (THD) and power factor (PF) is presented. In addition, hard-switching and soft-switching operation are discussed to clarify the importance of soft-switching transition in a power converter.

1.1.1 Total Harmonic Distortion

THD is defined as the ratio of the non-fundamental rms values to the rms fundamental component. The total harmonic distortion for current is given by

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}} \tag{1-1}$$

Requirements and regulations for the line voltage THD are strict, and a voltage THD of only 10% can cause problematic interactions with sensitive loads [8]. Since the power grid line voltage is generally well regulated and has minimal distortion, it is a reasonable to assume the input voltage is perfectly sinusoidal to simplify analytical techniques. Input current THD, however, can easily exceed 100%, depending on the load and converter used.

1.1.2 Power Factor

The ratio of real power, *P*, to the apparent power, *S*, is defined as power factor. Real power contributes to actual work through the transfer of energy. A resistance heater, for instance, generates heat purely

through real power. Apparent power is a scalar quantity and is the product of the rms current I_{rms} and rms voltage V_{rms}, as given in (1-2). If a load is purely resistive and consumes all transferred energy, its apparent power is equal to its real power. If however, apparent power is not equal to the real power, there exist energy storage devices, such as capacitors and inductors, storing and releasing energy during the energy conversion process. If such a case, a byproduct is incomplete net energy transfer to the load.

$$S = I_{rms}V_{rms} \tag{1-2}$$

Power factor provides a dimensionless measure of useable energy efficiency, with values constrained between one and zero. This relationship is shown in equation (1-3). When the sinusoidal source voltage is perfectly in phase with the sinusoidal source current, as in Figure 1.3, the power factor is unity.

$$\text{PF} = \frac{P}{S} \tag{1-3}$$

With unity power factor, the current drawn from the source is minimized and the load appears purely resistive from the input source, thereby maximizing power transfer to the load. Practically, unless the load is purely resistive, unity power factor is impossible, but power factors exceeding 0.99 are achievable. If a normally non-sinusoidal load, such as a computer power supply, is controlled to draw a sinusoidal load current, this control method is called power factor correction (PFC).

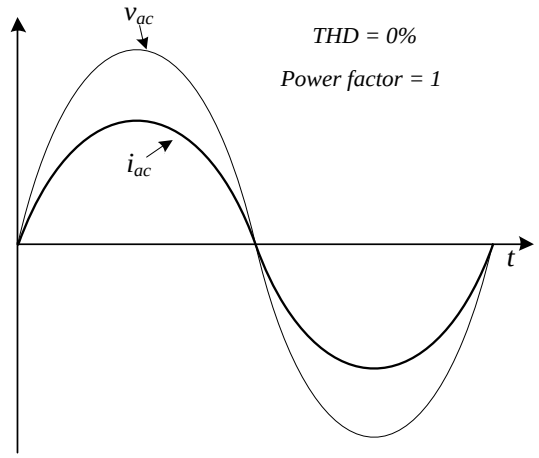


Figure 1.3 Ideal input current and voltage with unity power factor and no current distortion.

There is a direct relationship between total harmonic distortion and power factor. A term called the displacement factor, that relates the fundamental current phase φ_1 to the fundamental voltage phase θ_1, is defined by equation (1-4). In addition to the displacement factor, a term called the distortion factor, which relates the fundamental rms current to the total rms current, is defined by equation (1-5).

$$\text{displacement factor} = \cos(\varphi_1 - \theta_1) \tag{1-4}$$

$$\text{distortion factor} = \frac{I_{1,rms}}{I_{rms}} \tag{1-5}$$

The definition of power factor is the product of the displacement and distortion factor (1-6), and with no DC current component, as given by (1-7).

$$\text{PF} = (\text{distortion factor})(\text{displacement factor}) \tag{1-6}$$

$$\text{PF} = \left(\frac{1}{\sqrt{1 + (\text{THD})^2}}\right)\cos(\varphi_1 - \theta_1) \tag{1-7}$$

1.1.3 Hard-Switched Converters

Typically, conventional power factor correction converters operate in hard-switching mode, which means the power devices (e.g. IGBTs or MOSFETs) are turning on and turning off with the presence of voltage and current during the switching transition. In PFC applications, a power device turning on has the bus voltage (typically in the range of 350-600 V) across it as it changes state. During a switching interval (less than 0.5 microseconds), there is a finite time when the power device begins to conduct, and the voltage across the device begins to fall at the same time as current begins to flow through it. The simultaneous presence of voltage across the transistor and current through it (overlap between voltage and current) means that power is being dissipated within the device during the switching transition time. A similar phenomenon occurs when a transistor turns off with the full current flowing through it. Typical voltage, current and switching loss power waveforms during the turn-on and turn-off transitions in a hard-switched converter are shown in Figure 1.4.

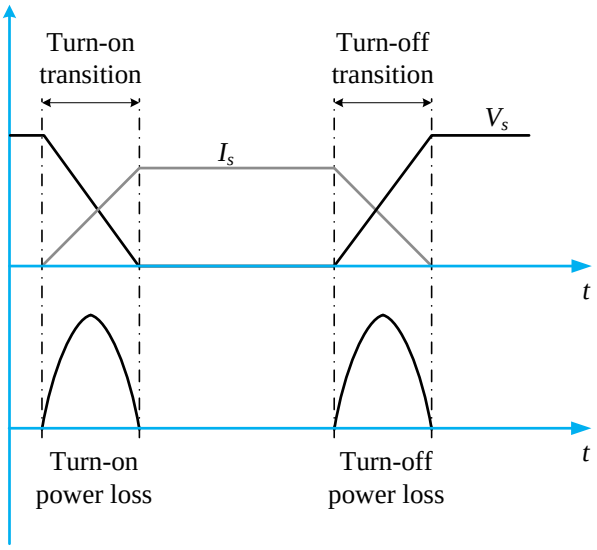


Figure 1.4 Turn-on and turn-off transition in a hard-switched converter.

Furthermore, high frequency operation is desirable to reduce passive components size and increase power density. However, high switching frequency operation increases switching losses, resulting in reduced converter efficiency. Hence, it is desirable to have soft-switching operation at high switching frequency operation (e.g. typically above 100 kHz).

1.1.4 Soft-Switched Converters

The overlap between voltage and current prior to switching transitions has to be reduced to achieve an efficiency improvement and lower electro-magnetic-interference (EMI) noise. The purpose of soft-switching techniques is to decrease or eliminate the simultaneous presence of voltage and current through the power device without reducing the switching frequency. Soft-switching techniques usually refer to zero voltage switching (ZVS) and zero current switching (ZCS) as shown in Figure 1.5 and Figure 1.6 respectively, which reduces the turn-on losses and turn-off losses respectively. Moreover, the low EMI noise generated from a soft-switched converter allows the converter to be switched at a higher frequency to increase power density.

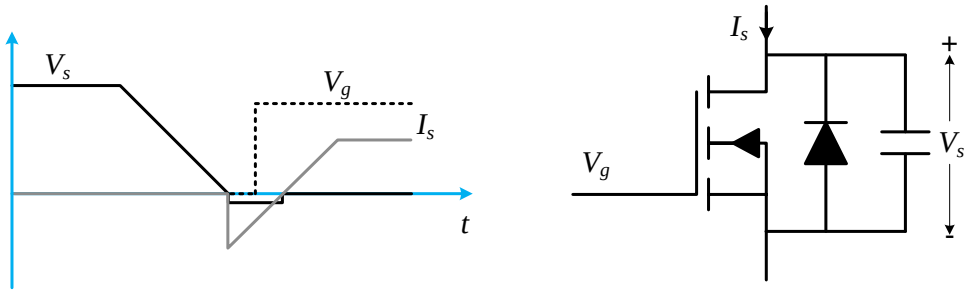


Figure 1.5 Zero Voltage Switching (ZVS).

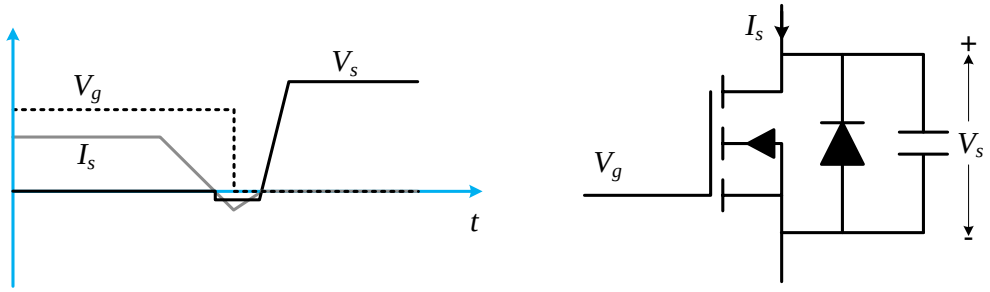


Figure 1.6 Zero Current Switching (ZCS).

As shown in Figure 1.5, ZVS can be achieved by forward biasing the anti-parallel diode of the semiconductor switch prior to applying gating signal to turn-on the switch and similarly ZCS can be achieved by reducing the current through the switch to zero prior to turning off the gating signal as shown in Figure 1.6. If a converter operates with ZVS, then the turn-off losses can be easily reduced by placing a lossless snubber (capacitor) directly across the switch. By doing this, the switches are naturally protected from large di/dt at turn-on with the help of ZVS and from large dv/dt with the lossless snubber capacitor. Therefore, ZVS operation is mainly considered in this research.

1.2 Research Motivation

The objective of this thesis is to investigate and conduct research on the high-performance single-phase solutions for AC-DC power factor corrected converters for electric vehicle battery chargers. The thesis investigates both single-stage and two-stage PFC approaches.

A variety of circuit topologies have been developed for PFC applications. The two-stage approach is the most commonly used approach. In this approach, a PFC stage is used at the front-end to force the line current to track the line voltage while the second stage isolated DC-DC converter provides a regulated output DC voltage. While the two-stage approach is cost effective in high-power applications, its cost-effectiveness is diminished in low-power applications due to the additional PFC power stage and control

circuit. A low cost alternative solution to this problem is the single-stage approach where the PFC input-stage is integrated with the isolated DC-DC converter. In both cases, the improvement of overall converter efficiency is critical for the emergence and acceptance of these converter technologies; as the charger efficiency increases, the converter size decreases. Additionally, to meet the efficiency and power factor requirements and regulatory standards for the AC supply mains, power factor correction is essential.

In conventional PFC converters, it is very important to design proper circuitry to reduce inrush current, as they inherently have high inrush current at start-up and lack of lightning and surge protection due to the direct connection of the AC input voltage through the PFC diode and PFC inductor to the bus capacitors. Addressing this drawback in conventional PFC converters requires additional circuitry, complexity, and often impacts system efficiency. In this dissertation, PFC circuit topologies which have inherent inrush current limiting capabilities are investigated.

Due to the requirement for high power density, power supplies and chargers are required to deliver more power with smaller volume. As a key component of a charger system, the front-end AC-DC converter must achieve high efficiency and power density. In this dissertation, several conventional non-isolated and isolated front-end AC-DC converter topologies are investigated and three new bridgeless non-isolated and one new bridgeless isolated power factor corrected converter are proposed to improve the efficiency, which is critical to minimize the converter size.

1.3 Thesis Organization

This thesis is organized into six chapters. In Chapter 1, the importance and need for PFC AC-DC converters is introduced, establishing the motivation for this thesis. Chapter 2 provides a detailed literature review of non-isolated and isolated PFC AC-DC converters.

In Chapter 3, a new non-isolated bridgeless AC-DC converter is proposed, which has inherent inrush current-limiting capabilities. The circuit description and modes of operation in the steady state are

presented. The converter is validated with an experimental prototype and results are presented, demonstrating the effectiveness and its suitability for inrush current-limiting capabilities.

In Chapter 4, a new non-isolated bridgeless AC-DC converter is proposed, which realizes soft-switching operation to reduce switching losses. The modes of operation, detailed design procedure and a complete loss analysis are presented. The soft-switching operation is validated with an experimental prototype and results are presented.

In Chapter 5, a new three-level non-isolated bridgeless AC-DC converter is proposed, which has high voltage gain. The circuit description, modes of operation, design procedure in steady state, and a complete loss analysis are presented. Finally, the proposed converter is experimentally validated showing the feasibility of the three-level operation along with soft-switching transition of all power devices.

In Chapter 6, a new single-stage bridgeless isolated AC-DC converter is proposed, which shows low conduction loss due to bridgeless operation and low voltage stress of the secondary diodes, low switching loss due to soft-switching operation, and a transformer that operates with no dc magnetizing current and no stored energy. The circuit description, modes of operation, a design procedure in steady state, and a complete loss analysis are presented. These benefits are validated with an experimental prototype and results are presented.

Chapter 0 summarizes the contributions of this thesis and provides possible areas of future work and improvement for applications of bridgeless AC-DC converter for power factor correction.

2 Literature Review

The general form of PFC implementation can be achieved by using an AC-DC converter at the front end followed by a DC-DC converter. This is referred to as the two-stage PFC approach. Depending on the current through the inductor in the first stage, the PFC AC-DC converter can operate in continuous conduction mode (CCM) [9], boundary conduction mode (BCM) [10]-[11], or discontinuous conduction mode (DCM) [12]-[13]. Recently, triangular conduction mode (TCM) operation has also been proposed [14]. In a particular switching cycle, the mode of operation depends on the continuity of the inductor current [15]. The implementation of PFC in the BCM, DCM and TCM modes of operation is relatively easier than CCM. However, in these modes, it requires a large input filter due to the inherently high current ripple. The high current ripple also introduces high RMS currents, which leads to high conduction losses, and high turn-off current in the PFC switch, which leads to high switching losses. The EMI impact is also adverse with these modes of operation. As a result, they are not a good choice for medium to high power applications, and are restricted for lower power applications. On the other hand, the CCM mode of operation offers low current ripple, which minimizes conduction and switching losses, hence it is the most common mode used in PFC converters.

In PFC applications, the buck, buck-boost converter and boost converter topologies can e used. However, the boost converter operating in CCM is the most popular PFC topology for the following reasons:

- The boost converter generates low peak current compared with buck and buck-boost converters. Low peak current translate to low switching losses and hence improved efficiency.
- The discontinuous input current in the buck and buck-boost converters make them less favorable for achieving unity power factor. It also generates high differential-mode EMI current.
- To reduce the line current harmonics, the buck and buck-boost converters use relativity larger inductors compared with the boost converter, which results in poor load transient response.

- Buck and buck-boost converters have higher line current distortion compared with boost converters. This happens when the input voltage is lower than the output voltage.

The boost converter operating in CCM is used in this thesis as the benchmark candidate for the non-isolated single-phase PFC AC-DC converter. The objectives of the PFC converter are to maintain unity power factor at the input side, and to regulate bus voltage at the output side. On the other hand, in single-stage isolated PFC converter, the power is processed by one stage, unlike the two-stage PFC approach. This converter can also operate in CCM, BCM or DCM. However, CCM is also preferred in the single-stage approach for the reasons discussed above.

2.1 Non-isolated AC-DC PFC Topologies

2.1.1 Passive AC-DC PFC Topologies

The objective of this section is to provide a concise summary of the methodologies and problems associated with uncontrolled passive AC-DC rectification circuits. The performance of the basic uncontrolled full-wave rectifiers are presented and their limitations in terms of THD and power factor are shown.

The most popular uncontrolled rectifier, illustrated in Figure 2.1, is used as a single-phase AC-DC converter [16]. This solution is very simple and effective. It has a low component count, making it an inexpensive solution to provide a DC voltage from an AC source. This converter also does not require control. As observed in Figure 2.1, a filter capacitor is added after the input diode bridge to minimize the output voltage ripple. For PFC applications, this solution is not attractive as the power factor is very low due to the pulsed current shape of the input ac current, as shown in Figure 2.2.

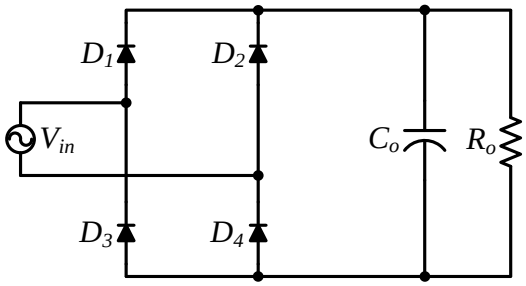


Figure 2.1 Uncontrolled full-wave rectifier.

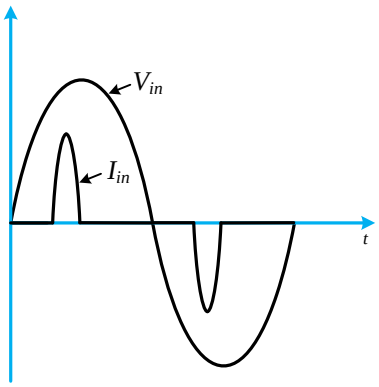


Figure 2.2 V_{in} and I_{in} of uncontrolled full-wave rectifier with capacitive filter.

The topology shown in Figure 2.3 adds a large inductor, which forces the input current to be continuous over the half-line AC input cycle without high peak currents, as is the case with the uncontrolled rectifier with capacitive filter. Although the input current is continuous (Figure 2.4), the power factor and THD are again unacceptable in meeting the regulatory standards. Furthermore, due to the low line frequency AC input, the physical size of the inductor impractically large and expensive for many applications.

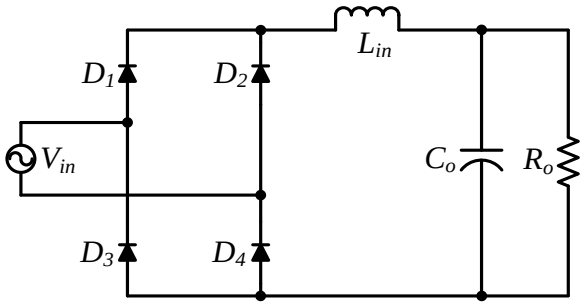


Figure 2.3 Uncontrolled full-wave rectifier with inductive filter.

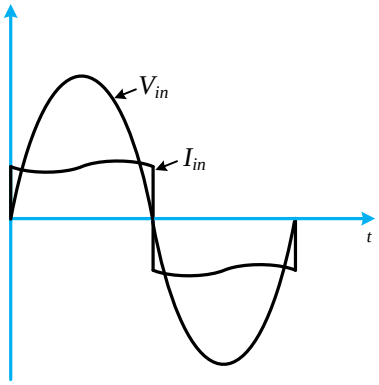


Figure 2.4 V_{in} and I_{in} of uncontrolled full-wave rectifier with inductive filter.

Generally, for PFC applications at power levels exceeding 50 W, the uncontrolled full-wave converter is not suitable due to high harmonic currents, low power factor, and a significant reduction in the maximum available power deliverable to the load. Other passive filtering techniques are possible, but suffer from inflexibility when load, or input conditions change, as well as large volume and size, and high cost [17]. Significant benefits can be realized through the use of controlled active PFC, therefore allowing considerably greater output power levels.

2.1.2 Active AC-DC PFC Topologies

The boost converter following a diode bridge rectifier and operating in CCM is the most widely used AC-DC PFC converter [18]. It uses a front-end diode bridge to rectify the AC input voltage to DC, which

is then followed by the boost section, as shown in Figure 2.5. This converter is very simple, and near-unity power factor can be achieved with proper control techniques. The inductor ripple current is directly seen at the converter's input and requires filtering to meet EMI specifications. The diode output current is discontinuous and needs to be filtered out by the output capacitor C_o. In this topology the output capacitor ripple current is very high, and its value is the difference between the diode current and the DC output current [19].

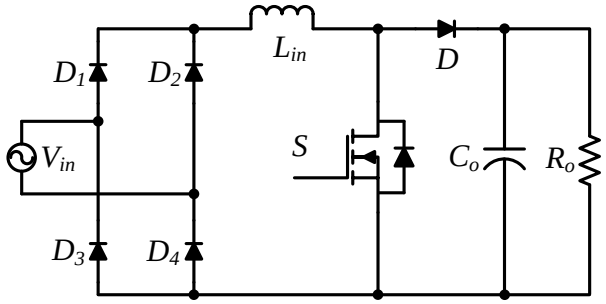


Figure 2.5 Conventional boost PFC converter.

Due to high switching losses in the boost switch and high conduction losses in the diode bridge, this converter suffers from poor efficiency. Moreover, in high frequency operation the boost diode reverse recovery charge introduces diode turn-off losses and EMI. In practical applications as the power level increases, the diode bridge losses become significant, causing challenges both for overall converter efficiency, and for cooling localized hot spots.

The interleaved boost PFC converter illustrated in Figure 2.6 is simply two boost converters in parallel operating with the switch gating signals 180° out of phase. The input current is the sum of the two inductor currents I_{Lin1} and I_{Lin2}. Because the inductor's ripple currents are out of phase, they tend to cancel each other out and therefore reduce the input ripple current caused by the boost inductors [22]-[22]. Interleaving also reduces the output capacitor ripple current as a function of the duty cycle [23]. In addition, the interleaved boost converter takes advantage of effectively paralleling semiconductors, and by having them switched

out of phase, it doubles the effective switching frequency, reducing the required input EMI filter size [24]. But it still has the problem of high-switching losses and heat management for the input rectifier diode bridge, and suffers from lower efficiency at light load, and low line conditions, compared to the non-interleaved boost PFC converter.

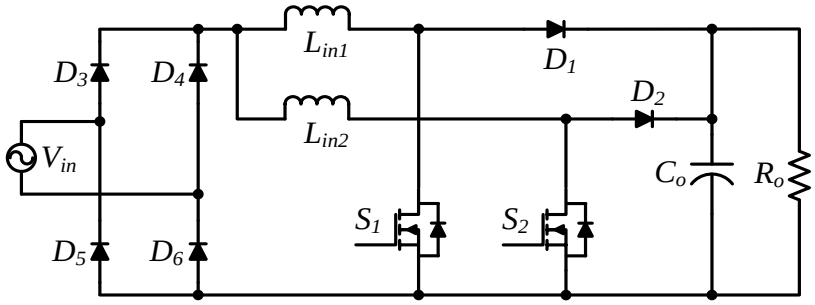


Figure 2.6 Interleaved boost PFC converter.

Unlike the boost and interleaved boost PFC converters, there is no diode bridge rectifier in the dual boost/bridgeless boost converter topology - shown in Figure 2.7 [25]-[27]. This topology reduces the total semiconductor count from six to four, and reduces conduction losses and the associated heat management issue in the input rectifier bridge. However, the dual boost converter also has high switching losses due to hard-switching operation of the PWM switches. In the semi-bridgeless converter, shown in Figure 2.8, since the return path inductance conducts only a small portion of the total return current, the total converter inductance is twice that of the conventional boost PFC converter [28]-[30].

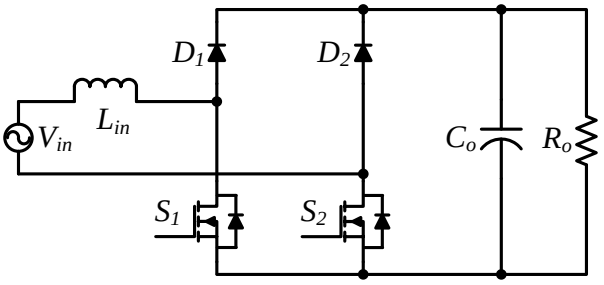


Figure 2.7 Bridgeless boost PFC converter.

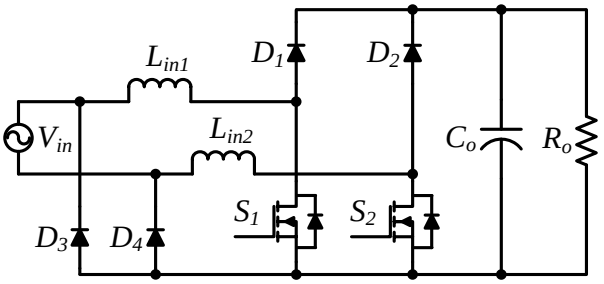


Figure 2.8 Semi-bridgeless boost PFC converter.

To reduce the switching losses of bridgeless and semi-bridgeless converters, soft-switching topologies have been proposed [31]-[35]. However, the topology proposed in [31], [33], and [34] reduces turn-off losses only and the auxiliary circuit of the proposed converter in [32] and [35] is complex. The H-bridge converter proposed in [36] requires three isolated current sensors, increasing complexity.

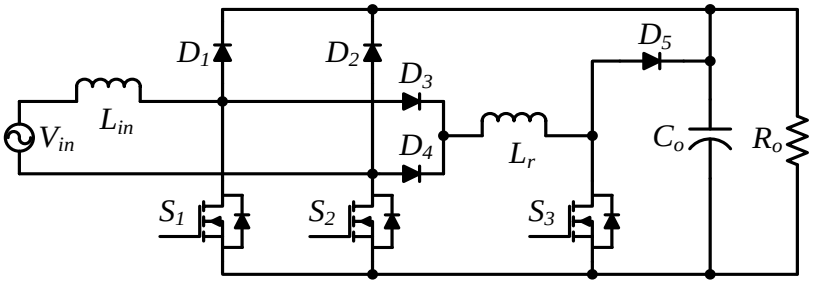


Figure 2.9 Soft-switching bridgeless boost PFC converter proposed in [34].

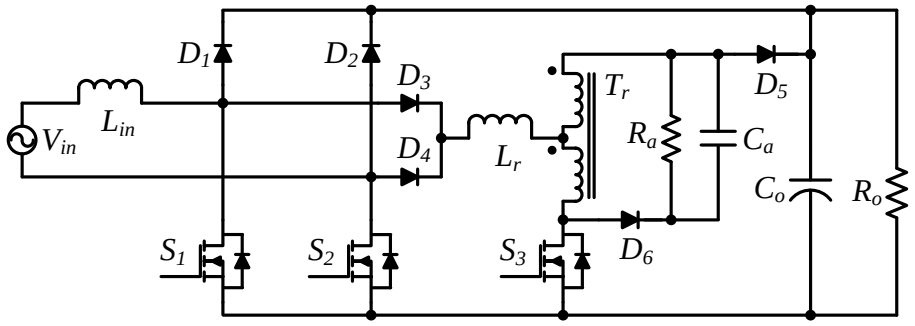


Figure 2.10 Soft-switching bridgeless boost PFC converter proposed in [35].

The totem-pole converter, illustrated in Figure 2.11, does not need two PFC inductors as the semi-bridgeless converter does [37]. However, the totem-pole converter uses the MOSFET body diode to carry the load current, creating a reverse recovery problem, which makes it unfavorable to use in CCM operation [38]. To reduce the reverse recovery losses of the body diode, the topologies in [39]-[42] have been proposed. However, in these circuits it is necessary to sense the positive and negative line-cycle operation to properly control the PWM switches, therefore the control and sensing is somewhat complex. As a solution, the totem-pole converter proposed in [43] can be driven with the same PWM signals for both PWM switches. The drawback of this converter is the increased number of passive elements. The converter proposed in [44] realizes high utilization of the power semiconductors while reducing the boost inductor size and line filter requirements. The drawback of this converter is the high number of semiconductors.

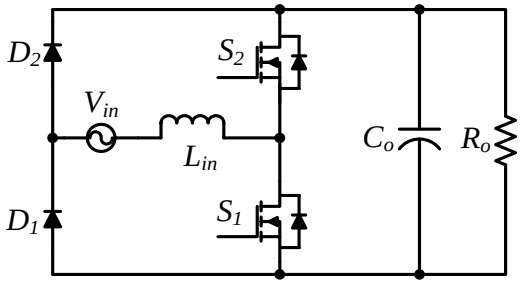


Figure 2.11 Totem-pole PFC boost converter.

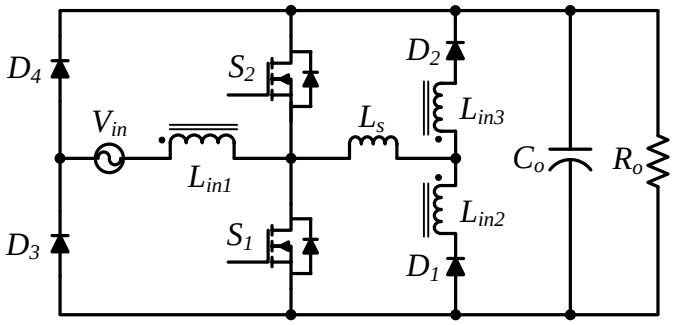


Figure 2.12 Converter topology proposed in [40].

To reduce conduction loss, variations of the bridgeless PFC topologies based on the Cuk and SEPIC converters have been proposed [45]-[52]. The second inductor used in the Cuk and SEPIC converters is relatively large in size, which reduces power density. Moreover, the topologies proposed in [45], [48], [50] and [52] have an increased number of passive elements, which add cost and reduce power density.

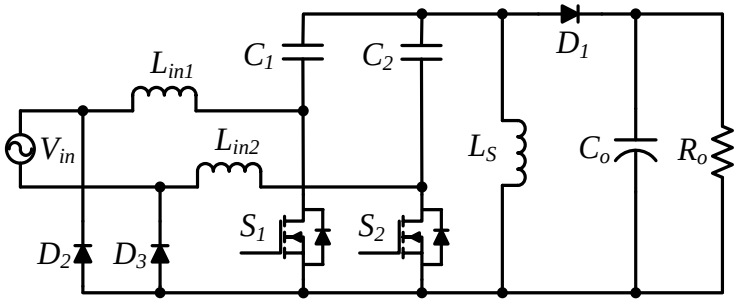


Figure 2.13 Converter topology proposed in [46].

The DC-DC converter proposed in [53] can realize ZVS for both switches, and has galvanic isolation. For AC-DC conversion, this converter requires a diode bridge rectifier, increasing conduction losses. The AC-DC boost converter topology proposed in [54] realizes bridgeless converter operation to reduce conduction losses. The drawback of this converter is the undesirable voltage spike across the PWM switches, limiting its use for high frequency and high power applications. Moreover, this converter requires complex variable switching frequency digital control, and the PWM switches are hard-switched. The

topology proposed in [55] operates in DCM, and is best suited for low power applications (i.e. below 300 W).

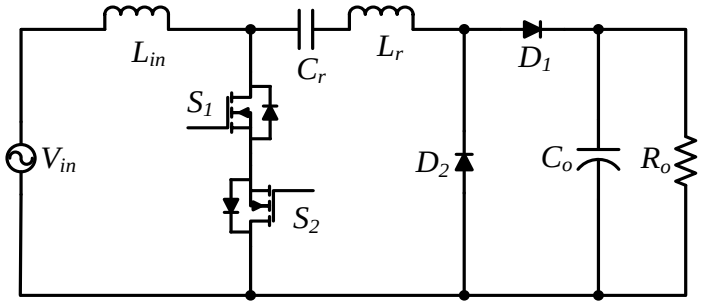


Figure 2.14 Converter topology proposed in [54].

2.2 Single-stage isolated AC-DC PFC Topologies

In single-stage isolated AC-DC PFC converters, the power is processed by one stage. The traditional two-stage PFC converter has good power factor and can be used for wide ranges of input voltage and output power and is well known and has relatively good overall performance. However, the two-stage approach needs an additional PFC stage; hence, the component count and total cost are high, which is undesirable for low power application.

For low power applications, to reduce the component count and cost, alternatives have been investigated by attempting to integrate the PFC input stage with the isolated DC-DC converter [56]-[58]. A PFC inductor is still necessary to shape the input current. An internal bulk-capacitor is needed to handle the instantaneous difference in power between the input pulsating power and the constant output power. Unlike in the two-stage PFC converter, the bulk-capacitor voltage in the single-stage converter is no longer regulated since the control freedoms are reduced by the integration of the PFC AC-DC and DC-DC switches into one single switch, or single switch network.

In a single-stage converter, the front-end integrated PFC can be a boost, buck/boost, forward or flyback converter. The flyback converter is the simplest and most common of the single-stage topologies. It has the minimum number of semiconductor devices, which makes it favorable for low cost implementation. The flyback converter has several disadvantages, including high voltage stress on the PWM switch, high switching losses due to hard-switched operation of the PWM switch, and high conduction losses due to the diode bridge rectifier. Moreover, the flyback transformer needs to store energy, requiring a larger transformer core size. The forward converter does not need to store energy in the transformer, hence the transformer size becomes smaller compared with the flyback converter. However, all other drawbacks remain. As a result, the flyback and forward converters are suitable only for low power applications.

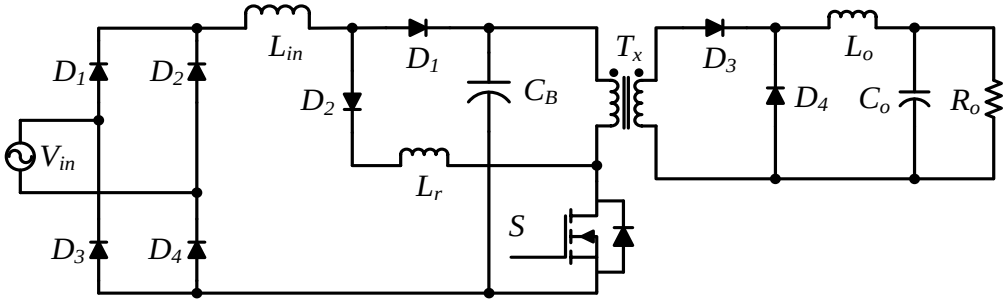


Figure 2.15 CCM single-stage PFC topology proposed in [56], [57].

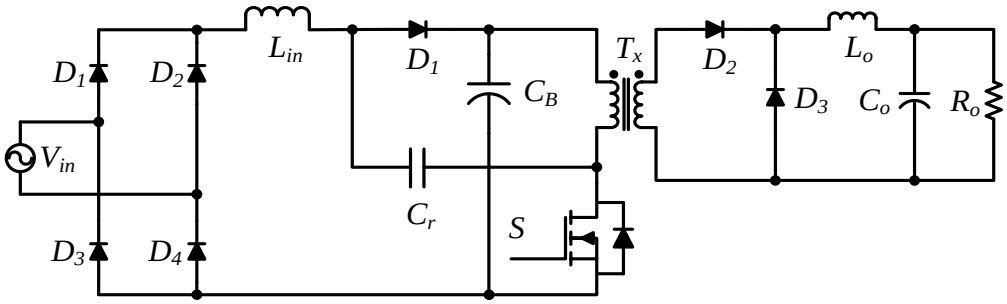


Figure 2.16 CCM single-stage PFC topology proposed in [58].

Single-stage AC-DC converters based on the half-bridge converter provide low voltage stresses and ZVS operation of the PWM switches [59]-[61]. Active-clamping techniques [62]-[64] have been applied to the single-stage PFC AC-DC converters. However, the majority of these development efforts have been focused on only reducing switching power losses. The previous single-stage PFC AC-DC converters [59]-[64] need a full-bridge diode rectifier. Use of a full-bridge diode rectifier increases the conduction losses and decreases the power efficiency. Especially at low line voltage, the full-bridge diode rectifier causes high conduction losses, resulting in additional thermal management. These problems can be overcome by eliminating the full-bridge diode rectifier.

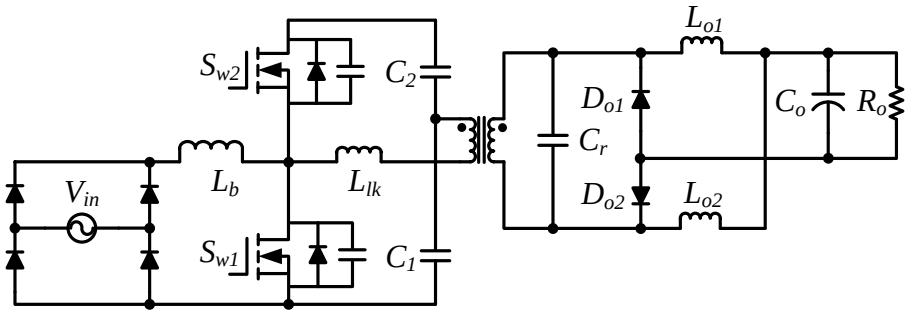


Figure 2.17 ZVZCS single-stage PFC topology proposed in [61].

The single-stage converter proposed in [65] doesn't need a diode bridge rectifier. This converter can achieve ZVS for the PWM switches to reduce switching losses. However, this converter operates in DCM and therefore is limited to very low power applications. The single-stage bridgeless converter proposed in [54] realizes simple implementation with a minimum number of semiconductor devices. This converter reduces the transformer size and increases the transformer efficiency, as the transformer does not store energy and has no DC magnetizing current. However, this converter operates with hard switching, increasing the switching losses.

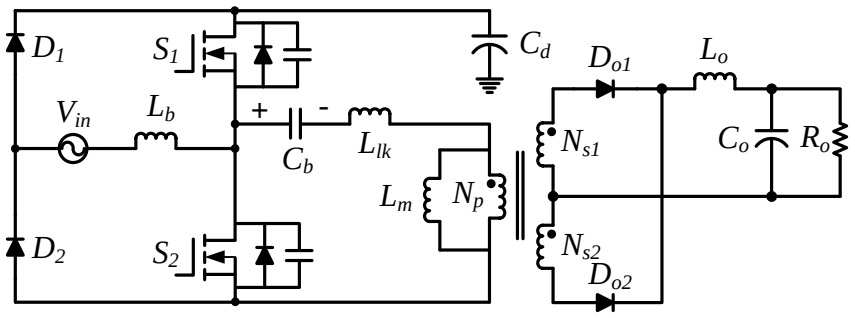


Figure 2.18 Bridgeless single-stage half-bridge PFC topology proposed in [65].

2.3 Summary

This section presented an overview of non-isolated two-stage and single-stage isolated AC-DC PFC topologies. The limitations of passive AC-DC PFC topologies were explored; their high THD and low power factor contribute to poor power quality, explaining the necessity of active power electronic devices to realize high power quality through power factor correction. Active PFC topologies were discussed, and specifically the boost and boost derived PFC converter topologies were presented.

The limitations of the boost PFC converter topology were discussed. The disadvantages of the front end diode-bridge rectifier was explained, showing the desirability of bridgeless PFC operation. The advantages of the dual boost/bridgeless converter were discussed. The bridgeless converters can minimize semiconductor conduction losses. The limitations of hard switching operation of boost and bridgeless boost converter were presented, explaining the desirability of soft-switching operation in PFC converters.

PFC topologies based on Cuk and SEPIC converters were presented. The advantages of these topologies were discussed. The PFC topologies with bridgeless and soft-switching operation were presented. Advantages including lower switching and conduction losses show why bridgeless operation with soft-switching capability is desirable for PFC converters. The state-of-the-art bridgeless soft-switching PFC topologies create high voltage stress on the PFC switches, limiting them to lower power applications

only. New PFC converter topologies with bridgeless and soft-switching operation are needed for high power applications.

Finally, an investigation into existing single-stage isolated AC-DC PFC topologies was presented. The limitations of the flyback and forward topologies were shown, including high voltage stress and larger transformer size. Different soft-switching single-stage topologies were discussed. Bridgeless soft-switching isolated topologies were presented and their advantages discussed. All the state-of-the-art bridgeless soft-switching topologies operate in DCM mode and so are suitable only for lower power applications. New single-stage bridgeless soft-switching PFC converter topologies are needed that can operated in CCM for high power applications.

3 A Hybrid Resonant Bridgeless AC-DC Power Factor Correction Converter[†]

3.1 Overview

In boost derived PFC converters, it is very important to design proper circuitry to reduce the inrush current as they inherently have high inrush current at start-up and lack of lightning and surge protection due to the direct connection of the AC input voltage through the PFC diode and PFC inductor to the bus capacitors. In these converters, inrush currents occur when the PFC circuit is connected to an input voltage with a peak higher than the instantaneous DC bus voltage. Similarly, if an AC power interruption occurs during normal operation for a period long enough for the dc bus capacitor to discharge below the peak of the AC input, inrush currents will flow upon restoration of AC power. Addressing these drawbacks in boost-derived converters requires additional circuitry, complexity, and often impacts system efficiency. Hence, for practical applications these converters require inrush current and surge-limiting to prevent damage on connection to AC power.

For high efficiency PFC converters of several hundred Watts and greater (i.e. > 400 W), in-rush current and surge-limiting is typically achieved by placing a current-limiting device (e.g. a resistor or positive temperature co-efficient device (PTC)) in series with the PFC circuit and shorting this device out with a relay after the difference between the bus voltage and peak rectified AC input is sufficiently small. These surge-limiting circuits add cost, complexity, and often regulatory difficulties when requiring voltage

[†] The content of this chapter has been published, and is in press in the following conference proceedings and journal, respectively:
[1] M. Alam, W. Eberle and N. Dohmeier, "An Inrush Limited, Surge Tolerant Hybrid Resonant Bridgeless PWM AC-DC PFC Converter," in *Proc. IEEE Energy Conversion Congress and Exposition*, Sept. 2014, pp. 5647-5651.
[2] M. Alam, F. Musavi and W. Eberle, "A Hybrid Resonant Bridgeless AC-DC Power Factor Correction Converter for Off-road and Neighborhood Electric Vehicle Battery Charging," in *Proc. IEEE Applied Power Electronics Conf*., Mar. 2014, pp. 1641-1647.
[3] M. Alam, D. Gautam, C. Botting, N. Dohmeier, F. Musavi and W. Eberle, "A Hybrid Resonant Pulse-Width Modulation Bridgeless AC–DC Power Factor Correction Converter" *in press*, IEEE Transactions on Industry Applications, DOI: 10.1109/TIA.2016.2638806.

sensing and control of the relay crossing isolation boundaries (if there is an isolated dc-dc converter followed by the PFC converter).

These surge-limiting circuits also need to be tolerant of AC power brownouts and blackouts which again add cost and complexity. Consider the scenario where the AC surge-limiting resistor has been shorted out by the relay and the AC power drops out for several cycles, preventing the PFC from maintaining the PFC bus voltage. During this short time the dc bus voltage (output voltage of the PFC converter) will drop while it supplies downstream loads. When AC power is restored the AC input relay will still be shorting out the surge-limiting resistor and allow a potentially damaging surge current to flow through the PFC components and eventually damage the power devices. This and many other AC power quality issues can make a robust surge-limiting implementation complex and expensive.

In boost derived PFC converters, a metal-oxide-varistor (MOV) is designed to protect the charger against an overvoltage transient. To do this, the MOV will begin to conduct current when the voltage across it reaches its clamping voltage. This action clamps (limits) the voltage by applying a short circuit across the AC line. The current handling capability of a MOV during this type of event – most commonly caused by lightning – is tremendously high, and will limit the voltage rise at the MOV to under 700 V, even with thousands of amperes flowing through the MOV. Typically, a MOV is rated for its energy handling capacity in joules, and its clamping voltage – the voltage at which the MOV begins to conduct. Because the MOV protects against overvoltage by shorting the AC line, the length of event that it will protect against is very limited. The current required to reduce the voltage of the AC line is very high – hundreds of amperes. Since the MOV in a charger/power supply is rated 275 V and 300 J, even a 100 A surge at 275 V can only last 10 ms before the MOV would be damaged. As previously discussed, monitoring at only one site showed that surges lasted minutes to hours – and thus there are MOV failures.

The purpose of this chapter is to propose a hybrid resonant pulse-width modulated (HRPWM) AC-DC PFC converter, which has inherent inrush current-limiting capabilities. The converter architecture also enables simple implementation of lightning and surge protection systems. Moreover, this converter can survive sustained over-voltage events and can limit the voltage stress on the converter and downstream components. These properties help to make a robust and reliable converter system.

Section 3.2 provides the operating principles of HRPWM converters. A detailed operating condition for the HRPWM converter is presented. In Section 3.3, the modes of operation of the proposed converter is presented. Section 3.4 provides the proposed converter operation during start-up. Section 3.5 provides a detailed analysis and a design example of the proposed converter. Finally, Section 3.6 presents experimental results showing the inherent in-rush current limiting and sustained over-voltage capability of the converter, along with a summary in Section 3.7.

3.2 Proposed Converter Operating Principles

The proposed HRPWM AC-DC PFC converter topology is illustrated in Figure 3.1. It is bridgeless and has only one input inductor. The switches S_1 and S_2 can be driven with the same PWM signal; hence it is not necessary to sense the positive or negative AC line-cycle operation. The voltage conversion ratio of the proposed converter is the same as the boost converter. However, during start-up this converter operates with step-down characteristics at very low duty cycles, reducing the start-up inrush current. Therefore, the converter architecture inherently exhibits lightning and surge protection. The HRPWM operation virtually eliminates the reverse recovery problems with the body diodes of the PWM switches. The input voltage is clamped with two slow diodes D_3 and D_4.

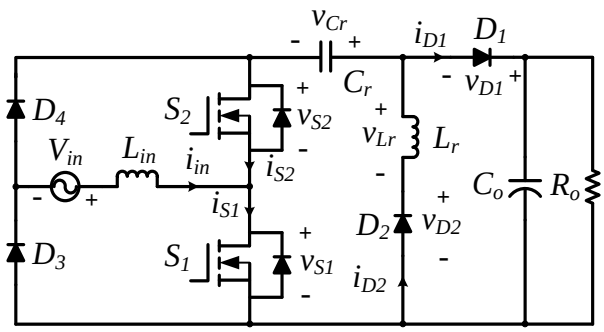


Figure 3.1 Proposed HRPWM PFC converter.

The HRPWM converter operates in hybrid-resonant mode when the switches are on and pulse-width-modulation (PWM) mode when the switches are off. Both modes occur during a single switching cycle. In the resonant mode, inductor L_r and capacitor C_r resonate. The resonant frequency has a significant impact on the operation of the converter, and can be higher, lower or equal to the switching frequency. Thus, there can be three possible resonant modes of operation when the switches are on, which are described in the sub-sections that follow.

3.2.1 Resonant Frequency Operation

The condition for at-resonant frequency operation, where the resonant frequency is equal to the switching frequency, is given by (3-1), where the resonant period T_r of the resonant tank L_r-C_r is defined by (3-2). The current waveforms for switches S_1 and S_2 and diode D_2 are provided in Figure 3.2. The converter circuit is provided in Figure 3.3 with the current paths noted during the resonant period.

$$T_r = 2T_{on} \tag{3-1}$$

$$T_r = 2\pi\sqrt{L_r C_r} \tag{3-2}$$

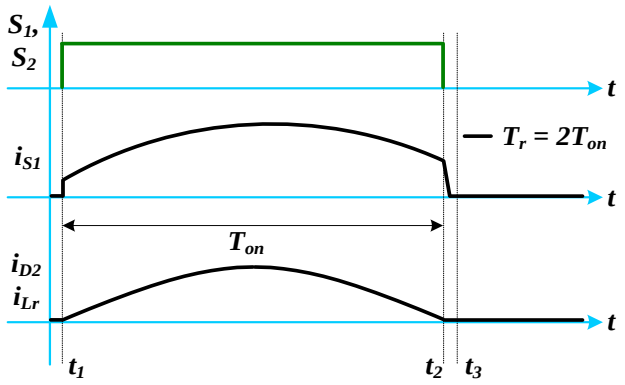


Figure 3.2 Waveforms for gating signal and current through S_1 and D_2 during resonant frequency operation

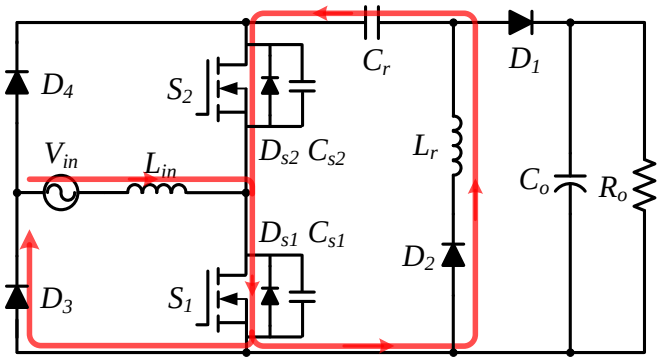


Figure 3.3 Converter operation during t_1-t_2.

With resonant frequency operation, diode D_2 turns off at zero-current, enabling the turn-off current of S_1 to be low, thereby reducing the turn-off switching losses in S_1. However, in an AC-DC converter the duty cycle, D varies significantly. In order to maintain a constant on-time interval for operation at resonance, the converter needs to operate with a variable switching frequency, which increases complexity.

3.2.2 Above Resonance Operation

At above-resonance operation, the resonant period is longer than the switching period. The condition for above-resonance operation is given by (3-3). The current waveforms for switches S_1 and S_2 and diode

D_2 are provided in Figure 3.4. The converter equivalent circuits for this mode are provided in Figure 3.5 and Figure 3.6, with the current paths noted.

$$T_r > 2T_{on} \tag{3-3}$$

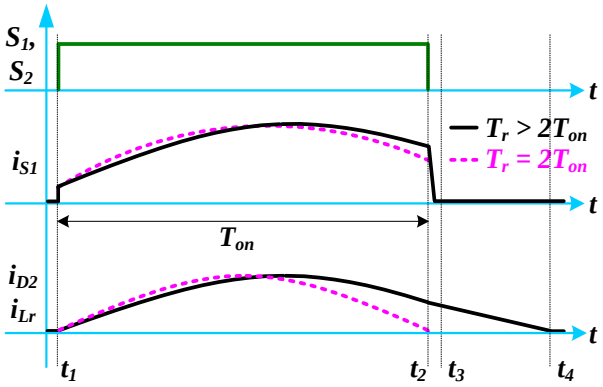


Figure 3.4 Waveforms for gating signal and current through S_1 and D_2 during above-resonance operation.

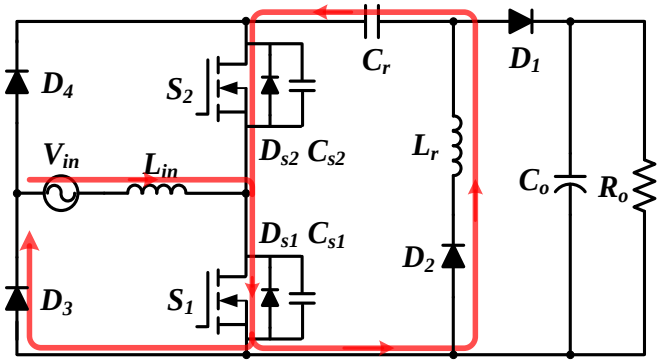


Figure 3.5 Converter operation during t_1-t_2.

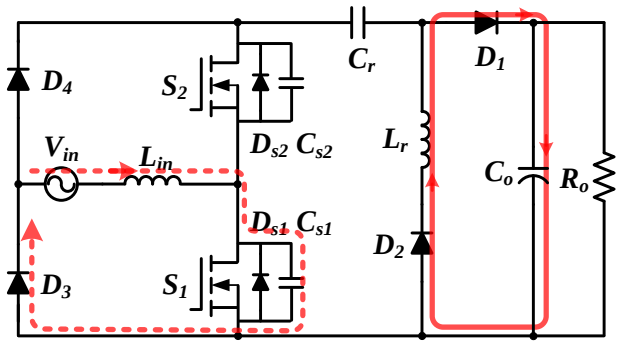


Figure 3.6 Converter operation during t_2-t_4.

It can be observed from Figure 3.4 that during the interval (t_1-t_2,) the resonant current i_{Lr} follows the current path as shown in Figure 3.5 and the current path changes during (t_2-t_4,) as shown in Figure 3.6. The switch S_1 turns off while there is current in the L_r-C_r resonant branch. This hard turn-off of S_1 increases loss and electromagnetic interference. However, one benefit of this mode is that it does not require variable switching frequency operation as is required for resonant frequency operation. Therefore, the control can be implemented using a standard average current mode control integrated circuit (IC).

3.2.3 Below Resonance Operation

At below-resonance operation, the resonant period is shorter than the switching period. Thus the condition for below-resonance operation is given by (3-4). Current waveforms for switches S_1 and S_2 and diode D_2 are provided in Figure 3.7. The converter circuit is provided in Figure 3.8 with the current paths noted.

$$T_r < 2T_{on} \tag{3-4}$$

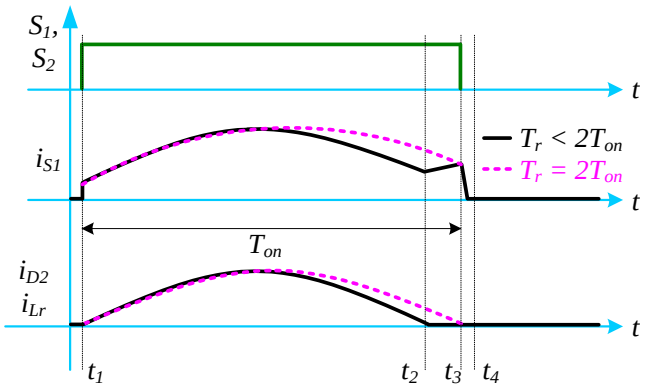


Figure 3.7 Waveforms for gating signal and current through S_1 and D_2 during below-resonance operation.

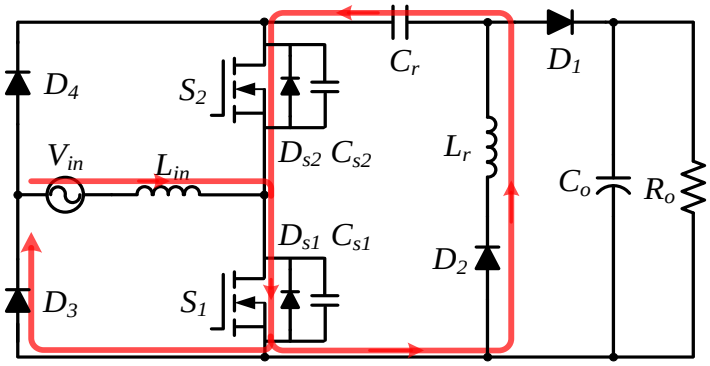


Figure 3.8 Converter operation during t_1-t_2.

It can be observed from Figure 3.7 that D_2 turns off with zero current at t_2, and the turn-off current of S_1 is low compared with above-resonance operation. Thus, it reduces the turn-off losses of S_1. Below-resonance operation also does not require a variable switching frequency, hence it can be easily implemented using a standard average current mode control IC. However, one drawback of below-resonance operation is high peak current at low duty cycles when the input voltage is high.

In order to use a standard commercially available average current mode control IC, fixed switching frequency operation of the proposed converter is required. In addition, as the input voltage and duty cycle slowly change over a line cycle, the converter transitions through all three resonant operating modes.

3.3 Modes of Operation

For simplicity, the discussion that follows refers only to the positive AC half-line cycle operation. Key waveforms for the proposed converter are provided in Figure 3.9, over one switching cycle, for below-resonance operation.

Interval-1(t_0-t_1): This interval starts when switches S_1 and S_2 are turned on. The input current, i_{in} stores energy in the input inductor, L_{in}, as illustrated in Figure 3.10. This interval ends when the resonant current i_{Lr} is zero. The input current i_{in}, the resonant current i_{Lr} and the voltage across the resonant capacitor v_{Cr} are given by (3-5)-(3-7), respectively.

$$i_{in}(t) = \frac{V_{in}}{L_{in}}(t - t_0) + i_{in}(t_0) \tag{3-5}$$

$$i_{Lr}(t) = -\,i_{Cr}(t) = \frac{V_{Cr(max)}}{Z}\,\sin\big(\omega_r(t - t_0)\big) \tag{3-6}$$

$$v_{Cr}(t) = V_{Cr(max)}\big[\cos\big(\omega_r(t - t_0)\big) - 1\big] + v_{Cr}(t_0) \tag{3-7}$$

where, $Z = \sqrt{L_r/C_r}$ and $\omega_r = 1/\sqrt{L_r C_r}$.

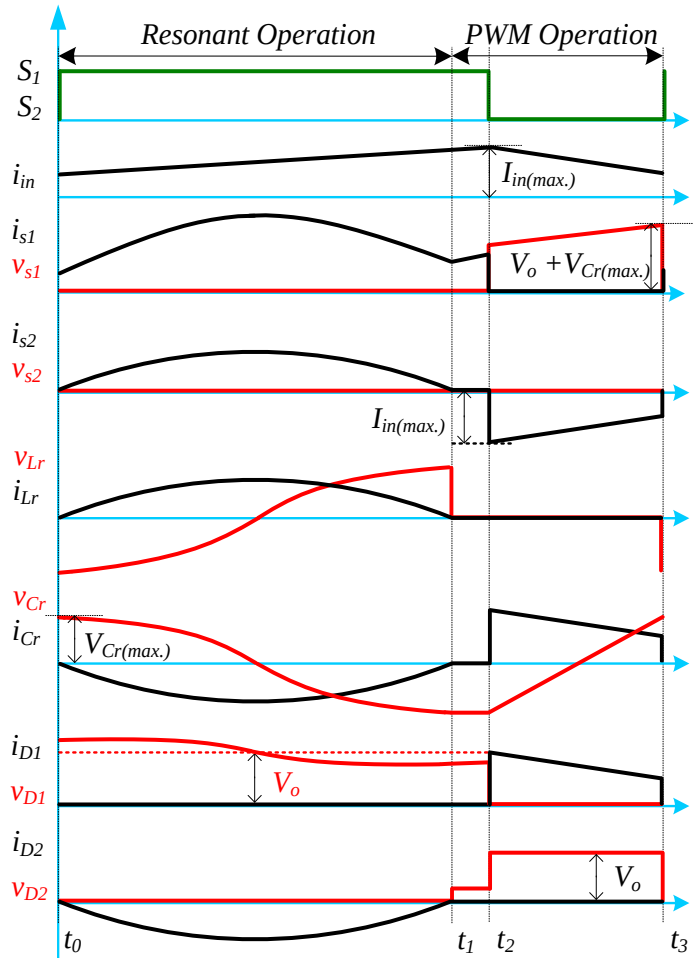


Figure 3.9 Proposed HRPWM converter waveforms in CCM.

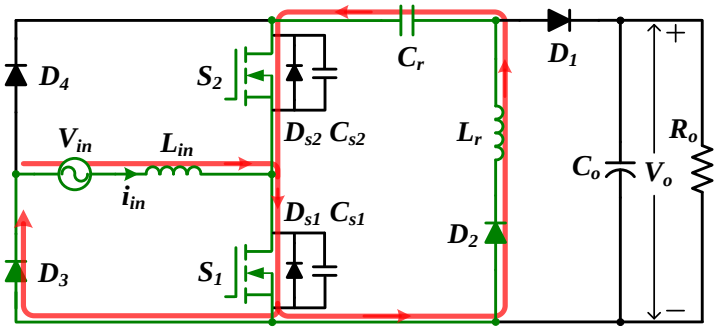


Figure 3.10 HRPWM bridgeless topology conduction path during *Interval-1*.

Interval-2(t_1-t_2): This interval starts when D_2 stops conducting and there is no current in the resonant branch. The inductor, L_{in} continues to store energy similar to traditional boost operation, as illustrated in Figure 3.11. This interval ends when S_1 and S_2 are turned off.

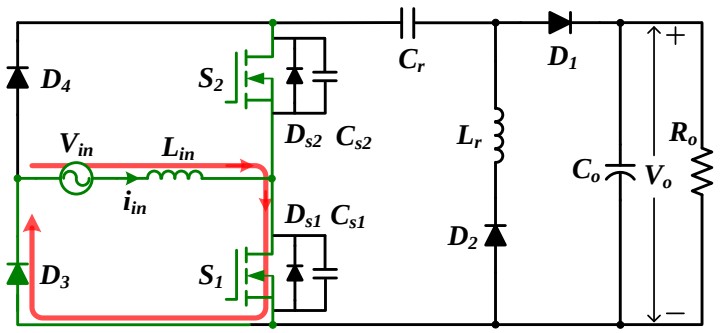


Figure 3.11 HRPWM bridgeless topology conduction path during *Interval-2*.

Interval-3(t_2-t_3): In this interval, the energy stored in the input inductor L_{in} is transferred to the load, as illustrated in Figure 3.12. This interval ends when S_1 and S_2 are turned on at t_3/t_0 and interval-1 starts. The input current i_{in} is given by (3-8).

$$i_{in}(t) = \frac{V_{in} - V_{Cr(min)} - V_0}{L_{in}} (t - t_2) + i_{in}(t_2) \tag{3-8}$$

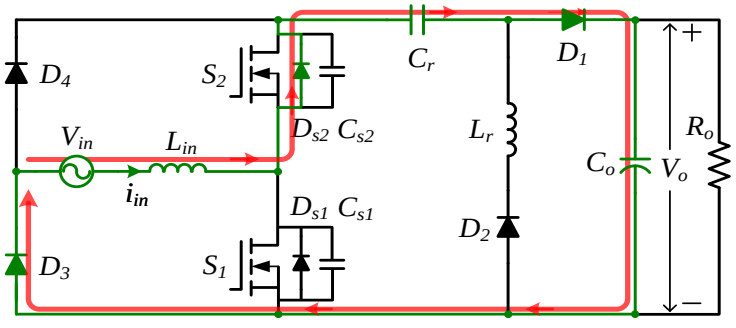


Figure 3.12 HRPWM bridgeless topology conduction path during *Interval-3*.

3.4 Operation during Startup and In-rush Considerations

Figure 3.13 illustrates the proposed converter's operation during startup. It can be seen that, unlike the conventional boost converter, the input current of the proposed converter flows through the resonant capacitor, C_r and the bus capacitor, C_o when the PWM switches are not activated. For $C_o >> C_r$, the equivalent circuit after the initial application of power is provided in Figure 3.14.

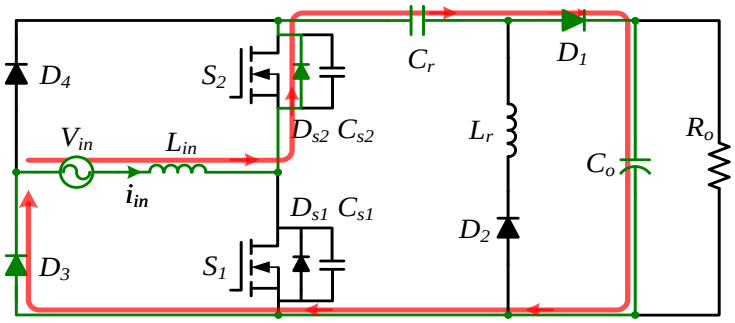


Figure 3.13 Inrush current path for positive line cycle.

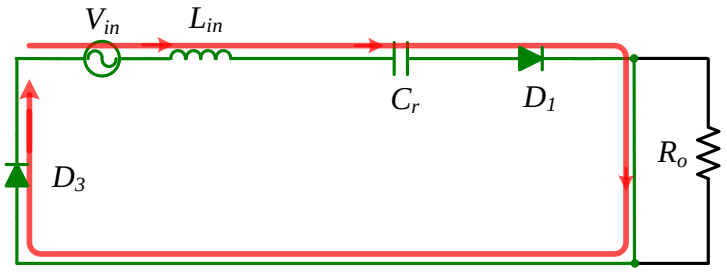


Figure 3.14 Equivalent circuit during startup neglecting the low impedance of C_o.

The worst-case inrush current equation (3-9) is determined using the following conditions: high line input voltage connection to the PFC converter at a phase angle corresponding to the highest peak; $C_r << C_o$; ideal L_{in} and C_r; no initial currents in Lin or voltages on C_r and C_o; and assuming no source impedances or converter resistances.

$$i_{inrush}(t) = \sqrt{2}\, V_{in(max)} \sqrt{\frac{C_r}{L_{in}}} \sin \omega t \tag{3-9}$$

where, $\omega = 1/\sqrt{L_{in} C_r}$

3.5 Analysis and Design

In this section, key design equations, including the converter DC conversion ratio and current and voltage stresses are provided in addition to a design example.

3.5.1 DC Voltage Conversion Ratio

The DC voltage-conversion ratio is the same as a boost converter at normal operating condition and is given by (3-10). Hence, standard duty cycle control can be used for this converter.

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D} \tag{3-10}$$

3.5.2 Voltage Stress Analysis

A stress analysis was performed on the proposed converter. The voltage stress on the resonant components and the diodes is the output voltage, V_o. The voltage stress on MOSFETs, S_1 and S_2 is given by (3-11).

$$V_{S1\_S2(max)} = V_o + V_{Cr(max)} \tag{3-11}$$

In steady-state, the average load current equals the average current in diodes D_1 and D_2. Thus, the average load current is given by (3-12).

$$I_{D2}(avg) = \left[\frac{1}{T_s} \int_0^{T_r/2} V_{Cr(max)} \sqrt{\frac{C_r}{L_r}} \sin(\omega_r t) dt \right] \tag{3-12}$$

Using (3-12), $V_{Cr(max)}$ is given by (3-13).

$$V_{Cr(max)} = \frac{I_o}{2C_r f_s} \tag{3-13}$$

3.5.3 Design Example

A design example is provided to determine the optimal resonant frequency of the resonant tank, L_r-C_r. The example specifications are listed in Table 3.1.

Table 3.1 Design specifications

Table Parameter	Value
Input voltage range, V_{in}	85-265 V
Nominal input voltage, $V_{in(nom)}$	180 V
Switching frequency, f_s	70 kHz
Rated output power, P_o	650 W
Output Voltage, V_o	400 V

In order to reduce the turn-off losses of the PFC MOSFETs, below-resonance operation has been selected and from (3-4) and (3-10) the optimal resonant frequency is 64 kHz calculated using (3-14).

$$f_r \geq \frac{f_s V_o}{2\left(V_o - V_{in(nom)}\right)} \tag{3-14}$$

Using (3-13) and setting $V_{Cr(max)}$ to 25 V, C_r is given by (3-15).

$$C_r = \frac{I_o}{2V_{Cr(max)} f_s} \tag{3-15}$$

Therefore, an off-the-shelf 1 µF capacitor was selected using (3-15).

The resonant inductance, L_r is given by (3-16) and is calculated using (3-2).

$$L_r = \frac{1}{4\pi^2 f_r^2 C_r} \tag{3-16}$$

Therefore, a 6 μH inductor was selected.

To ensure inherent inrush current and energy limiting, all the components in the inrush current path need to sustain the peak inrush current, which can be calculated using (3-9) to be 18.74 A as given by (3-17).

$$i_{inrush}(peak) = \sqrt{2}\, V_{in(max)} \sqrt{\frac{C_r}{L_{in}}} = 18.74\ A \tag{3-17}$$

The energy limit associated with peak inrush current is calculated as 0.022 A^2s as given by (3-18).

$$I_{inrush}^2(peak) T_r = \left(\sqrt{2}\, V_{in(max)} \sqrt{\frac{C_r}{L_{in}}} \right)^2 \pi \sqrt{L_{in} C_r} = 0.022\ A^2 s \tag{3-18}$$

When provided in the datasheets, the peak current, peak voltage and energy limits of the devices in the inrush current path are provided in Table 3.2. It can be seen that the peak current and energy limits of the devices are far beyond the worst-case surge currents and energies calculated in (3-17) and (3-18), respectively.

3.6 Experimental Results

An experimental prototype was built to verify the operation of the proposed converter. A complete schematic is provided in Figure A- 2 in the Appendix. A photo of the prototype is provided in Figure 3.15. The converter was designed according to the parameters listed in Table I using average current mode control. The key components specified in Table 3.2 were used.

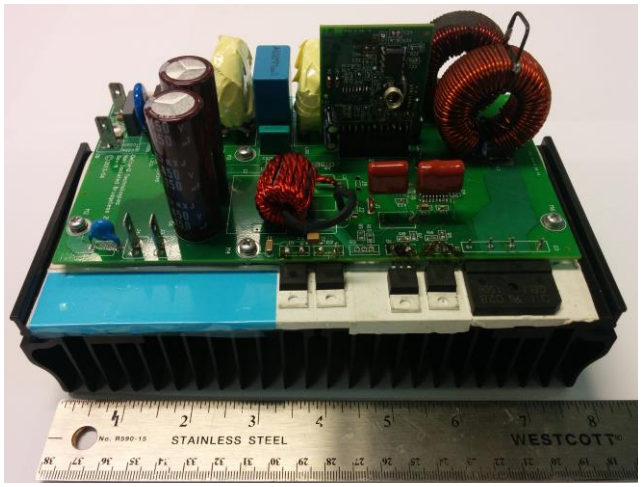


Figure 3.15 Proposed converter experimental prototype.

Table 3.2 List of key converter components

Component	Part Number	Peak current limit	I^2T or energy limit	Peak voltage limit
S_1, S_2	IPP65R110CFD	100 A	N/A	650 V
D_1, D_2	IDH08G65C5	>60 A	18 A^2s	650 V
D_3, D_4	GBJ1506	240 A	240 A^2s	600 V
C_o	450TXW150MEFC(2 in parallel)	N/A	N/A	450 V
C_r	ECW-F2225JA (2 in series)	N/A	N/A	500 V
L_r	6 µH	N/A	N/A	N/A
L_{in}	370 µH	N/A	N/A	N/A
Gate Driver	IRS2113	N/A	N/A	N/A

The experimental input voltage, input current and output voltage waveforms for the proposed converter are provided in Figure 3.16. Test conditions were as follows: V_{in}= 120 V, V_o= 400 V, P_o= 650 W, f_s= 70 kHz. The input current is in phase with the input voltage, and its shape is close to a sinusoidal waveform, as expected. Waveforms of the voltage across switch S_1, V_{S1} and the gating signal for S_1, V_g are provided in Figure 3.17 for positive line cycle operation when S_1 is working as a PWM switch. The voltage across the switch is nominally the output voltage, V_o (e.g. 400 V) plus the relatively small ripple voltage (e.g. 25 V) across C_r.

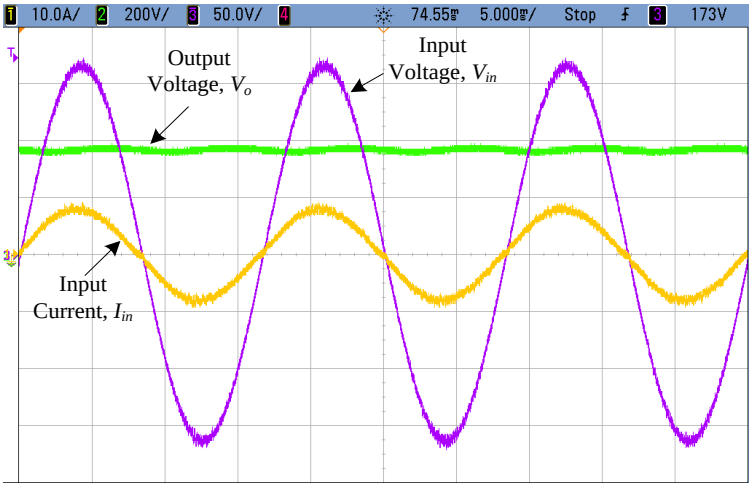


Figure 3.16 Proposed converter experimental waveforms at 5ms/div of input voltage, V_{in} (ch3: 50 V/div), input current, I_{in} (ch 1: 10 A/div) and output voltage, V_o (ch2: 200 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 70 kHz.

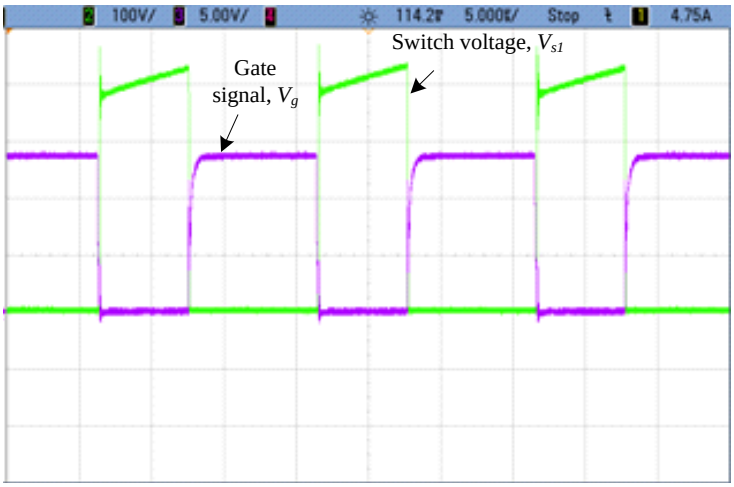


Figure 3.17 Proposed converter experimental waveforms at 5μs/div of voltage across switch S_1, V_{S1} (ch2: 100 V/div) and gating signal for S_1, V_g (ch3: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 70 kHz.

Waveforms of the voltage across the resonant capacitor C_r, V_{Cr} and the current through the resonant inductor L_r, I_{Lr} are provided in Figure 3.18. During the resonant period, the resonant capacitor discharges in a sinusoidal resonant fashion and during PWM operation, the resonant capacitor charges linearly. Figure 3.19 shows the measured inrush current of a conventional boost converter without additional inrush current limiting circuitry. The peak inrush current was expected to exceed 300 A; however, limitations in the electronic AC source and measurement equipment prevented capturing the real world worst case inrush current.

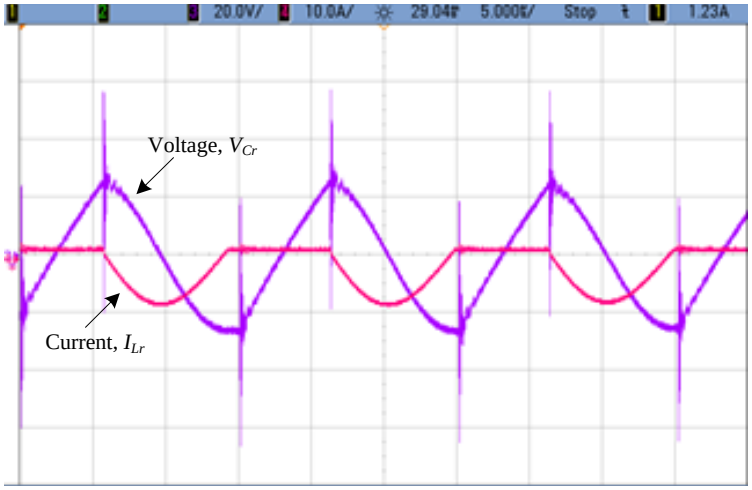


Figure 3.18 Proposed converter experimental waveforms at 5μs/div of voltage across capacitor C_r, V_{Cr} (ch 3: 20 V/div) and current through inductor L_r, I_{Lr} (ch 4: 10 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 70 kHz.

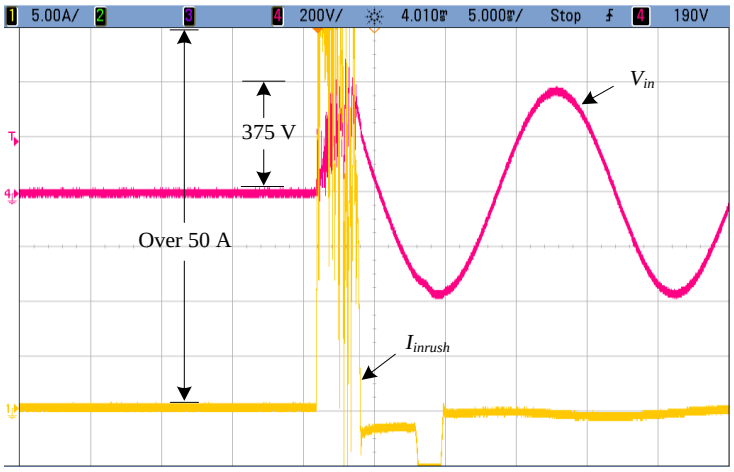


Figure 3.19 Conventional boost converter experimental waveforms at 5ms/div of inrush current, I_{inrush} (ch 1:5A/div), and input voltage, V_{in} (ch 4:200V/div) at V_{in} = 265V, V_o = 0 V.

The inrush current of the proposed HRPWM converter was recorded as 5.2 A, with a pulse width of 800 μs, corresponding to a I^2T of 0.021 A^2s, as illustrated in Figure 3.20. The measured shape and period of the surge current differs from the predicted worst case due to several factors: most importantly source impedances, dv/dt and fast current-limiting of the electronic AC source, and the many complex impedances

in the EMI filter. However, the inrush energy matches closely with the predicted value. Hence, the proposed converter can be utilized without any extra inrush current protection circuit. On the other hand, with identical circuit parameters, the inrush current of a conventional boost converter without additional inrush current-limiting circuitry would exceed 300 A. Therefore, a conventional boost converter requires inrush current-limiting circuitry, which adds cost and complexity.

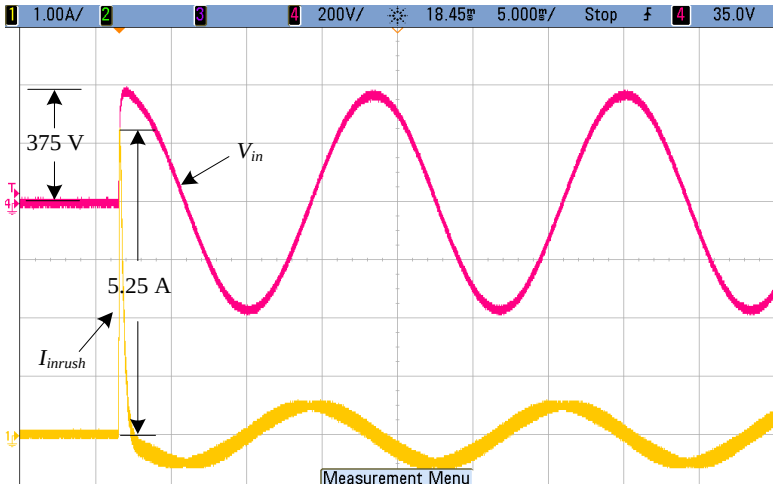


Figure 3.20 Proposed converter experimental waveforms at 5ms/div of inrush current, I_{inrush} (ch 1:1A/div), and input voltage, V_{in} (ch 4:200V/div) at V_{in} = 265V, V_o = 0 V.

Figure 3.21 shows the result of increasing AC input voltage from 265 V to 320 V for the conventional boost converter. When this happens the converter's controller disables switching, but it is clear that the converter output voltage rises to the peak of the AC input (~460 V peak). The converters output is connected to the DC bus capacitance and downstream components. Hence, it is necessary to use higher voltage rated bus capacitors. Figure 3.22 shows the result of increasing the AC input voltage from 265 V to 320 V for the proposed HRPWM prototype converter. As with the boost converter, the controller disables switching when the AC input voltage becomes excessive; however, the peak rectified AC input appears

across the resonant capacitor, C_r and does not pass to the converters output. As a result the voltage stress on the bus capacitor of the proposed converter is lower than conventional boost converter.

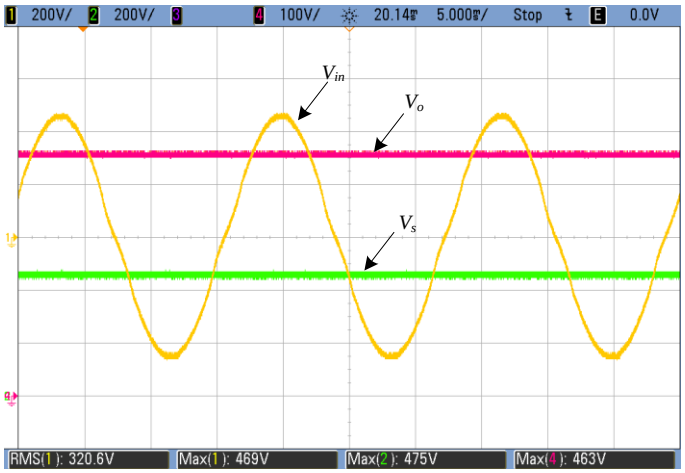


Figure 3.21 Conventional boost converter experimental waveforms at 5ms/div of withstand input voltage, V_{in} (ch1: 200 V/div), voltage across boost switch, V_s (ch 2: 200 V/div) and output voltage, V_o (ch4: 100 V/div).

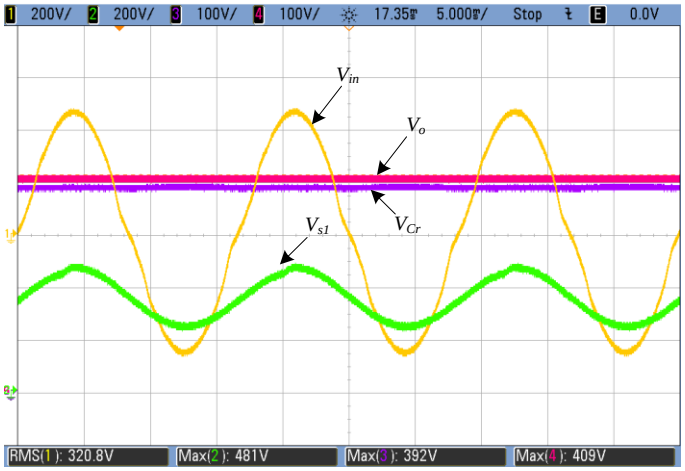


Figure 3.22 Proposed converter experimental waveforms at 5ms/div of withstand input voltage, V_{in} (ch1: 200 V/div), voltage across boost switch, V_{s1} (ch 2: 200 V/div), voltage across resonant capacitor C_r, V_{Cr} (ch 3: 100 V/div) and output voltage, V_o (ch4: 100 V/div).

As a evidence of the heat spreading features of the proposed converter, thermal images of the diode bridge for both the conventional boost PFC converter and the proposed converter are provided in Figure 3.23 and Figure 3.24, respectively. It is observed that the maximum temperature of the diode bridge of the boost PFC converter is 88.8^{o} C compared to 64.9^{o} C for the proposed converter.

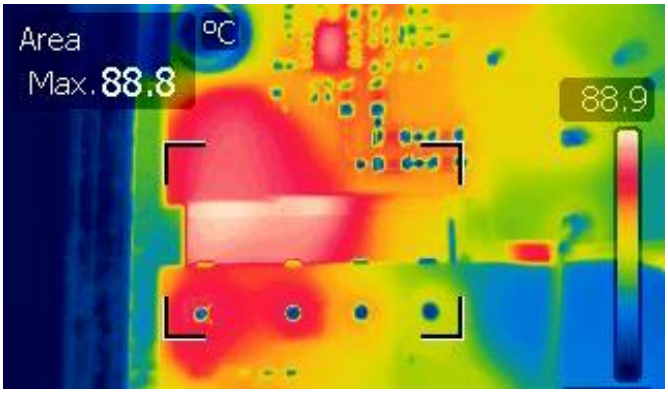


Figure 3.23 Thermal image of diode bridge rectifier of boost PFC converter at 650W.

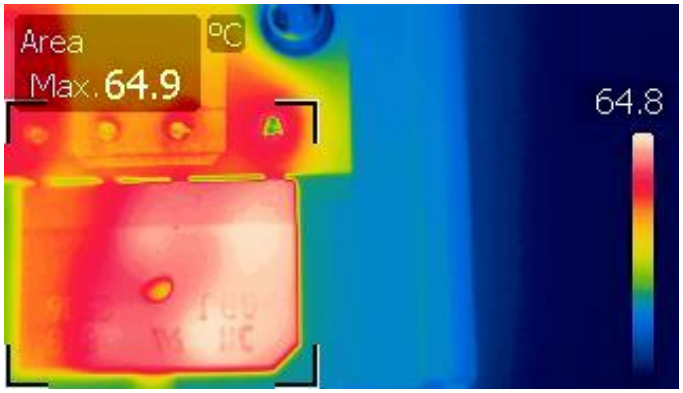


Figure 3.24 Thermal image of diode bridge rectifier of proposed converter at 650W.

Curves of the measured converter efficiency versus output power at 120 V, 220 V and 240 V input are provided in Figure 3.25. The proposed converter achieves high efficiency over the entire load range. A peak efficiency of 97.5% was measured at 240 V input and 205 W load.

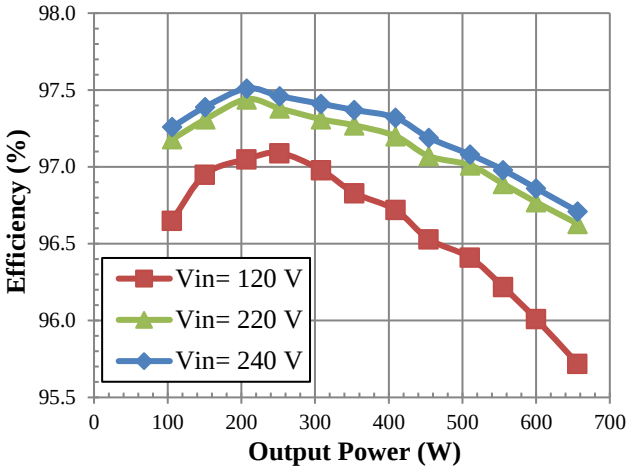


Figure 3.25 Proposed HRPWM converter measured efficiency as a function of output power at f_s =70 kHz.

Curves of the measured converter power factor versus output power at 120 V, 220 V and 240 V input are provided in Figure 3.26. The power factor is greater than 0.98 from 50% load to full load.

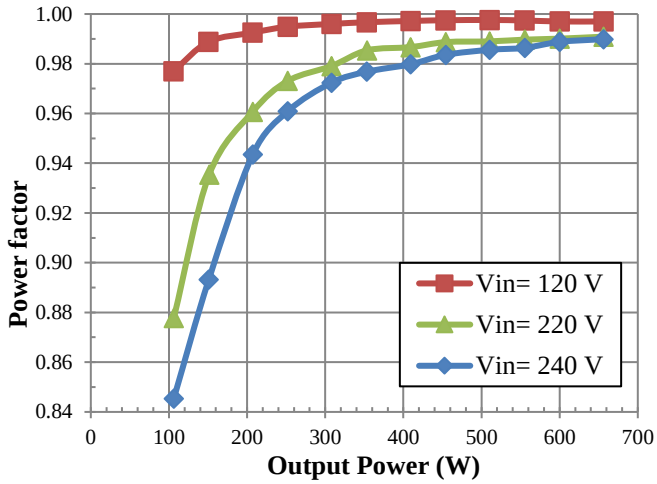


Figure 3.26 Proposed HRPWM converter power factor as a function of output power at f_S =70 kHz.

In order to verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the EN 61000-3-2 standard in Figure 3.27 for 120 V and 240 V input. All converter harmonics are well below IEC standard.

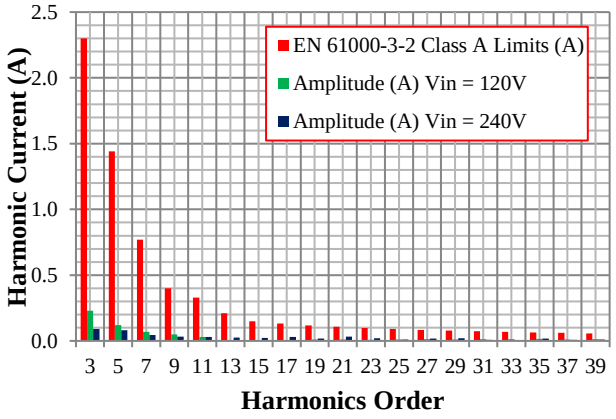


Figure 3.27 Input current harmonics at V_{in} = 120 V and 240 V at full load condition for proposed converter.

3.7 Summary

This chapter presented a new HRPWM PFC converter. The limitations of boost derived PFC converters, in particular, high in-rush current and lack of lightning and surge protection, were discussed,

which further motivated the necessity of a PFC converter with inherent inrush limiting capability. A detailed explanation of the proposed converter operating principles and modes of operation was presented. A step-by-step design procedure was described. Experimental results demonstrated that the proposed converter inherently limits the in-rush current and has the capability to withstand sustained over voltage conditions. The converter power factor and efficiency measurements were provided as a function of load power at 120V, 220V and 240V input. The power factor is greater than 0.97 from half load to full load. The proposed converter achieves a peak efficiency of 97.5% at 240 V input and 200 W output power.

4 A Soft-Switching Bridgeless AC-DC Power Factor Correction Converter*

4.1 Overview

In Chapter 3, a HRPWM PFC converter was proposed. This converter operates with hard-switching, meaning that there is simultaneous presence of voltage across the MOSFET and current through it during switching, so power is dissipated within the device during the switching transition. This chapter presents a new soft-switching HRPWM AC-DC PFC converter which also has inherent inrush current-limiting capabilities. The purpose of soft-switching techniques is to decrease, or eliminate the simultaneous presence of voltage and current through the power device during switching. Unlike the conventional boost or bridgeless boost converters, the proposed converter minimizes switching losses by achieving ZVS for all switches. Moreover, ZCS is achieved for the output rectifier diodes, which reduces the reverse recovery losses. The proposed converter also realizes bridgeless converter operation, eliminating the heat management issues in diode bridge rectifier required with the conventional boost converter. Unlike the totem-pole converter, the proposed converter can be driven with the same PWM signal and it doesn't require sensing both the positive and negative AC line cycle operation, enabling simplified control. The resonant components used in the proposed converter are relatively small in size compared with the size of the passive elements in the Cuk and SEPIC converters. The proposed converter can operate at high switching frequency without the undesirable voltage spike across the PWM switches in the resonant topology in [38]. The proposed soft-switching bridgeless AC-DC PFC converter topology is illustrated in Figure 4.1.

* The content of this chapter has been published and is in press in the following conference proceeding and journal, respectively:
[1] M. Alam, W. Eberle, D. Gautam and F. Musavi, " A Soft-Switching Bridgeless AC-DC Power Factor Correction Converter for Off-Road and Neighborhood Electric Vehicle Battery Charging," in *Proc. IEEE Applied Power Electronics Conf*., Mar. 2014, pp. 103-108.
[2] M. Alam, W. Eberle, D. Gautam and C. Botting, "A Soft-Switching Bridgeless AC-DC Power Factor Correction Converter" *in press*, IEEE Transactions on Power Electronics, DOI: 10.1109/TPEL.2016.2632100.

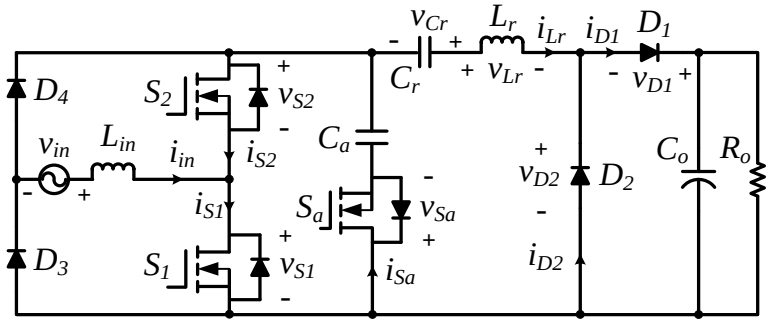


Figure 4.1 Proposed soft-switching bridgeless AC-DC PFC converter topology.

Section 4.2 presents the modes of operation of the proposed converter. In Section 4.3, a detailed analysis and a design example for the proposed converter is presented along with a loss analysis. Finally, Section 4.4 provides the experimental results, showing the soft-switching operation. The chapter summary is presented in Section 4.5.

4.2 Modes of Operation

In the paragraphs that follow, the operation of the proposed converter is explained in detail and a mathematical analysis of its steady-state operation is provided. This converter operates in hybrid-resonant mode when the switches are on and PWM mode when the switches are off. Both modes occur during a single switching cycle. In the resonant mode, inductor L_r and capacitor C_r resonate. The resonant frequency has a significant impact on the operation of the converter, and can be higher, lower or equal to the switching frequency. As discussed in section 3.2 that the below resonance operation is preferred to reduce switching losses so the following discussion refers to below resonance operation. The key waveforms for the proposed converter are provided in Figure 4.2. For simplicity, the discussion that follows refers only to the low frequency positive AC half-line cycle operation over one high frequency switching cycle.

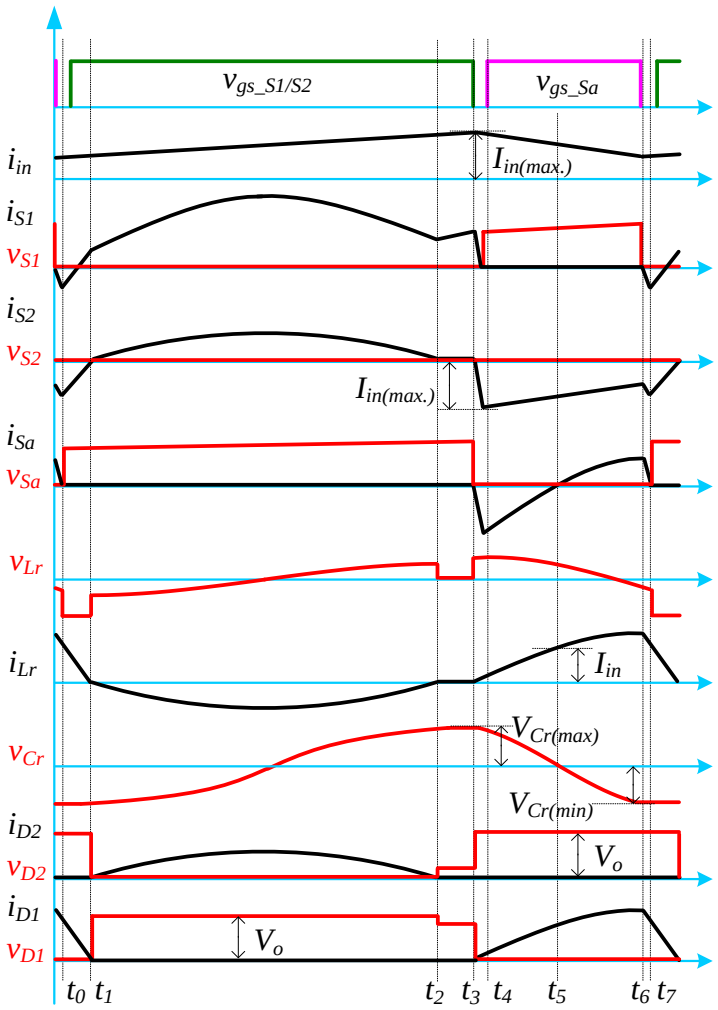


Figure 4.2 Proposed soft-switching HRPWM converter waveforms in CCM.

Interval-1(t_0-t_1): The equivalent circuit is provided in Figure 4.3(a). This interval starts when the output capacitor C_{s1} of switch S_1 is fully discharged and the output capacitor C_{sa} of switch S_a is fully charged (i.e. the end of interval-7). The switch current of S_1 is clamped by the body diode D_{s1} to initiate ZVS turn-on of switch S_1. The gating signal $v_{gs\_S1/S2}$ enables ZVS turn-on for both S_1 and S_2. The input current i_{in} and the resonant current i_{Lr} are given by (4-1) and (4-2), respectively.

$$i_{in}(t) = \frac{V_{in}}{L_{in}}(t - t_0) + i_{in}(t_0) \quad (4\text{-}1)$$

$$i_{Lr}(t) = \frac{V_{Cr(min)} - V_o}{L_r}(t - t_0) + i_{Lr}(t_0) \quad (4\text{-}2)$$

Interval-2(t_1-t_2): The equivalent circuit is provided in Figure 4.3(b). During this interval the switch current i_{s1} follows the resonant current i_{Lr}, and is the sum of the input current i_{in} and resonant current i_{Lr}. The input current i_{in} stores energy in the input inductor L_{in}. This mode ends when the resonant current i_{Lr} is zero, which enables D_2 to turn-off with ZCS. The resonant current i_{Lr} and the voltage across the resonant capacitor v_{Cr} are given by (4-3) and (4-4), respectively.

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{Cr(min)}}{Z}\sin(\omega_r(t - t_1) \quad (4\text{-}3)$$

$$v_{Cr}(t) = V_{Cr(min)}\left[\cos\left(\omega_r(t - t_1)\right) - 1\right] + v_{Cr}(t_1) \quad (4\text{-}4)$$

where $Z = \sqrt{(L_r/C_r)}$ and $\omega_r = 1/\sqrt{(L_r C_r)}$

Interval-3(t_2-t_3): The equivalent circuit is provided in Figure 4.3(c). This interval starts when D_2 stops conducting, and there is no current in the resonant branch. In this interval the input inductor L_{in} stores energy, similar to traditional boost operation. This interval ends when switch S_1 is turned off.

Interval-4(t_3-t_4): The equivalent circuits are provided in Figure 4.3(d) and Figure 4.3(e). At $t = t_3$, the switch S_1 is turned off. The input current i_{in} charges the output capacitor C_{s1} of switch S_1, and discharges the output capacitor C_{sa} of switch S_a (Figure 4.3(d)). The switch current of S_a is then clamped by the body diode D_{sa} with the equivalent circuit provided in Figure 4.3(e). The input current i_{in}, resonant current i_{Lr}, and voltage across the resonant capacitor v_{Cr}, are given by (4-5), (4-6) and (4-7), respectively.

$$i_{in}(t) = \frac{V_{in} - V_{Ca}}{L_{in}}(t - t_3) + i_{in}(t_3) \quad (4\text{-}5)$$

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{Cr(max)}}{Z}\sin(\omega_r(t - t_3)) \quad (4\text{-}6)$$

$$v_{Cr}(t) = V_{Cr(max)}\left[\cos\left(\omega_r(t - t_3)\right) - 1\right] + v_{Cr}(t_3) \quad (4\text{-}7)$$

where $Z = \sqrt{(L_r/C_r)}$ and $\omega_r = 1/\sqrt{(L_r C_r)}$

Interval-5(t_4-t_5): The equivalent circuit is provided in Figure 4.3(f). In this interval the gating signal v_{gs_Sa} enables ZVS turn-on for switch S_a after D_{sa} begins conducting in the previous interval.

Interval-6(t_5-t_6): The equivalent circuit is provided in Figure 4.3(g). This interval starts when i_{Lr} equals i_{in}, and the current through switch S_a starts flowing from its drain to source. Hence, the current through switch S_a changes its direction. This mode ends when switch S_a is turned off.

Interval-7 (t_6-t_7): The equivalent circuit is provided in Figure 4.3(h). During this interval the input current i_{in} charges capacitor C_{sa}, and discharges capacitor C_{s1}. The current through switch S_1 is clamped by the body diode D_{s1} in the next interval, interval-1.

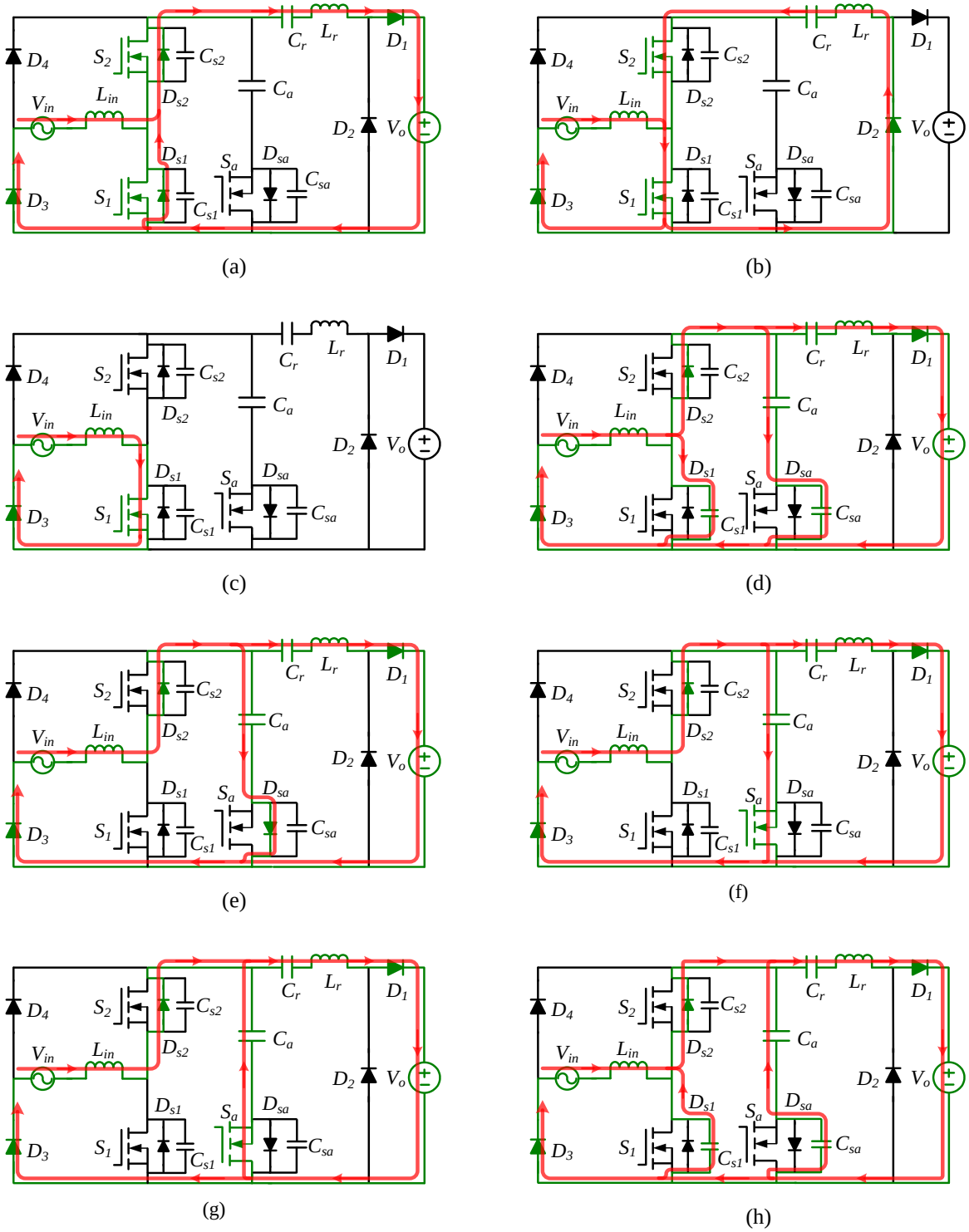


Figure 4.3 Proposed converter modes of operation.

4.3 Analysis and Design

4.3.1 DC Voltage Conversion Ratio

In steady state, the DC voltage conversion ratio of the proposed converter can be found using average voltages. In one switching period, the net volt-second product across L_{in} and L_r is equal to zero, i.e. $V_{Lin(avg)} = V_{Lr(avg)} = 0$ V. Therefore, the average switch voltages, V_{s1} and V_{s2} are equal to the input voltage, V_{in}. When the switch S_1 is on, the switch voltage V_{s1} is zero and when switch S_1 is off, the switch voltage, V_{s1} is $V_{Cr}+V_{D2}$, since $V_{Lr} = 0$ V. Accordingly, when switch S_1 is on, the diode D_2 conducts the resonant current, thus $V_{D2} = 0$ V, and when switch S_1 is off it blocks the output voltage V_o. Hence, the volt-second balance is given by (4-8).

$$V_{in}T_s = (V_o + V_{Cr})(1 - D)T_s \tag{4-8}$$

Since during the on-time interval only the voltage V_{Cr} is applied to the inductor L_r, the average voltage V_{Cr} must be zero. Therefore, using (4-8) with $V_{Cr} = 0$, the DC voltage conversion ratio is given by (4-9), which is the same conversion ratio as the boost converter.

$$\frac{V_o}{V_{in}} = \frac{1}{1 - D} \tag{4-9}$$

4.3.2 Voltage Stress Analysis

The maximum voltage stress on switches S_1 and S_2 is the output voltage plus the peak resonant capacitor voltage, as given by (4-10).

$$V_{S1\_S2(max)} = V_o + V_{Cr(max)} \tag{4-10}$$

In steady-state, the average load current can be obtained from interval-2 and interval-4 and is given by (4-11).

$$I_{D2}(avg) = \frac{V_o}{R_o} = \left[\frac{1}{T_s}\int_0^{T_r/2} V_{Cr(max)}\sqrt{\frac{C_r}{L_r}}\,\sin(\omega_r t).\,dt\right] \tag{4-11}$$

Using (4-11), $V_{Cr(max)}$ is given by (4-12).

$$V_{Cr(max)} = \frac{I_o}{2C_r f_s} \tag{4-12}$$

4.3.3 ZVS Condition for the Switches

To achieve ZVS for S_1, it must be turned on during interval-1 (t_0-t_1). The current required to achieve ZVS for the PWM switches is determined by the difference between i_{in} and i_{Lr} at t_0, as given by (4-13).

$$I_{s1-S2(ZVS)} = I_{Lr(peak)} - I_{in(min)} = \frac{T_s I_o \omega_r sin(\omega_r(1-D)Ts)}{2} - \frac{P_o}{V_{in}} + \frac{DT_s V_{in}}{2L_{in}} \tag{4-13}$$

Rearranging, (4-13) can be expressed as (4-14).

$$I_{s1-S2(ZVS)} = \frac{L_{in}[V_{in} I_o T_s \omega_r\, sin(\omega_r(1-D)Ts) - 2P_o] + DT_s V_{in}^2}{2V_{in}L_{in}} \tag{4-14}$$

In addition to the timing requirement, there must also be sufficient energy stored in the resonant inductor L_r to completely discharge C_{s1}. To ensure ZVS turn-on of the PWM switches S_1 and S_2, the condition in (4-15) must be satisfied.

$$\frac{1}{2}\,L_r\,I_{s1-S2(ZVS)}^2 \geq \frac{1}{2}(C_{s1} + C_{sa})\left(\frac{V_{in}}{1-D}\right)^2 \tag{4-15}$$

In (4-15), C_{s1} and C_{sa} are the output capacitances of S_1 and S_a, respectively.

The ZVS condition for the auxiliary switch S_a is achieved when the PWM switches are turned off at t_3. The current in the auxiliary switch is the peak input current, which is given by (4-16).

$$I_{sa(ZVS)} = I_{in(max)} = \frac{2P_o L_{in} + DT_s V_{in}^2}{2} \tag{4-16}$$

At t_3, there must also be sufficient energy stored in inductor L_{in} to completely discharge the switch capacitance C_{sa}. Hence, to ensure ZVS turn-on of S_a, (4-17) must be satisfied.

$$\frac{1}{2} L_{in} I_{in(max)}^2 \geq \frac{1}{2}(C_{s1} + C_{sa}) \left(\frac{V_{in}}{1-D}\right)^2 \tag{4-17}$$

4.3.4 Design Methodology

A design example is provided to determine the input inductor L_{in}, the optimal resonant frequency f_r, the resonant inductor L_r, the resonant capacitor C_r and the clamping capacitor C_a. The example specifications are listed in Table 4.1. The input voltage range is the universal AC line voltage of 85 V to 265 V, which includes a 10 % tolerance for the nominal values.

Table 4.1 Design Specifications

Parameter	Value
Input voltage range, V_{in}	85 - 265 Vac
Input current ripple, $I_{\%Ripple}$	25%
Switching frequency, f_s	150 kHz
Rated output power, P_o	650 W
Output Voltage, V_o	400 Vdc

Using the design specifications, the input inductor, L_{in} is calculated using (4-18).

$$L_{in} = \frac{V_{in(min)}^2}{I_{\%Ripple}\, f_s\, P_o} \left(1 - \frac{\sqrt{2}\, V_{in(min)}}{V_o}\right) = 207\ \mu H \tag{4-18}$$

In order to calculate the resonant frequency, the condition in below-resonance operation is used to reduce the turn-off losses of the PFC switches. Hence, using (3-4) and (4-9), where $T_r = 1/f_r$ and $T_{on} = D/f_s$, the minimum resonant frequency is f_r = 107 kHz. The resonant inductor value is determined using (4-15) as L_r = 10 µH to maintain ZVS. Using (3-2), the resonant capacitor value is calculated to be C_r = 0.25 µF.

The value of clamp capacitor C_a is chosen based on the design of L_r and C_r. The resonant frequency formed by the clamp capacitor and the resonant capacitor with resonant inductor should be sufficiently low so that there is not excessive resonant ringing across the PWM switch when it is turned off. However, using too large a value of C_a yields no improvement in clamping performance at the expense of a larger (more costly and bulky) capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and the resonant capacitor with resonant inductor exceeds the maximum off time of PWM switch, as given by (4-15). Therefore an off-the-shelf 5 µF capacitor was selected using (4-19).

$$C_a \gg \frac{(1-D)^2}{\pi^2 L_r f_s^2} - C_r \tag{4-19}$$

4.3.5 Converter Loss Analysis

A detailed engineering loss analysis was performed using standard analytical techniques and PSIM simulation results (to model conduction losses) for the benchmark AC-DC boost converter and the proposed HRPWM ZVS converter. The estimated loss distribution is provided in Figure 4.4 at 150 kHz switching frequency, 100 V input and 650 W load. The low line 100 V input operating point was chosen since semiconductor conduction losses are highest at this point, therefore it is the point used to size heatsinks.

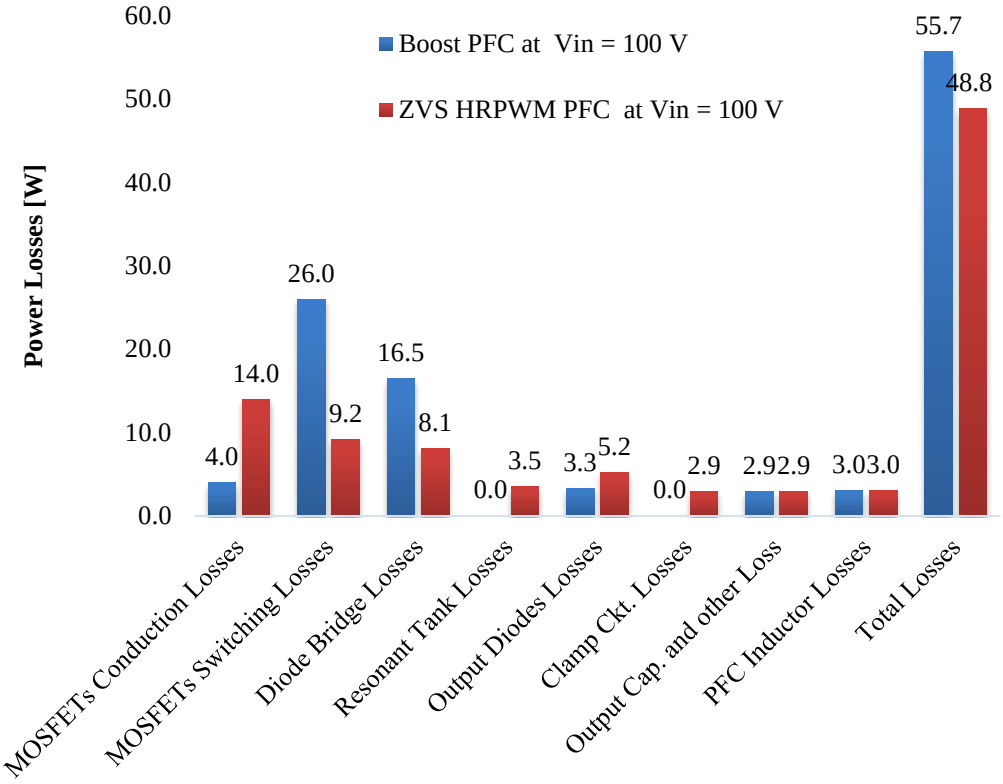


Figure 4.4 Loss distribution comparison at V_{in} = 100 V, f_s = 150 kHz, P_o = 650 W, V_o = 400 V.

Total losses in the converter are estimated to be reduced by 6.9 W (55.7 W – 48.8 W) compared to the benchmark boost PFC. The proposed converter reduces switching losses by 16.8 W (26 W – 9.2 W). In addition to the cost of the additional circuit components, the performance penalty for adding the auxiliary components includes increased circulating currents, resulting increased conduction losses by 10 W (14 W – 4 W). However, given the reduction in frequency dependent losses, the increased conduction losses are more than offset (i.e. by 6.8 W). Compared to the conventional boost PFC converter, one of the main benefits of the proposed converter is improved heat distribution, since the most lossy components (i.e. the PFC MOSFETs and bridge diodes) will run cooler due to lower losses. It is noted that these results are at 150 kHz switching frequency. At higher frequencies, the loss reduction would be more substantial. The

experimental results presented in the next section verify the analysis results and the primary conclusion related to reduced losses in the PFC MOSFETs and bridge diodes.

4.4 Experimental Results

Experimental prototypes of the proposed ZVS HRPWM converter and the conventional boost PFC converter were built to verify and compare the feasibility of the converter. A complete schematic of the proposed converter and the conventional boost PFC converter are provided in Figure A- 3 and Figure A- 1 respectively in the Appendix. A photo of the proposed experimental prototype is provided in Figure 4.5. The converter was designed to operate at up to 650 W output power according to the parameters listed in Table 4.1. Standard average current mode control was used. The key components of the proposed converter and the conventional PFC boost converter are provided in Table 4.2 and Table 4.3, respectively.

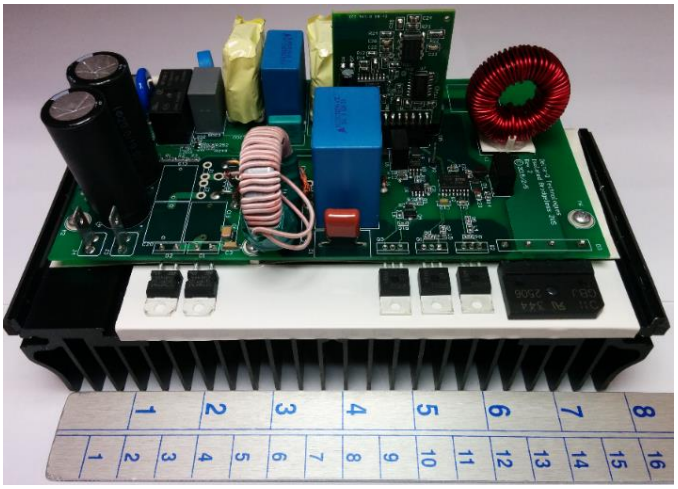


Figure 4.5 Proposed converter experimental prototype.

Table 4.2 Key components for the HRPWM converter.

Component	Device Description
S_1, S_2, S_a	IPP65R099C6
D_1, D_2	STTH8R06D
D_3, D_4	GBJ2506
L_{in}	250 µH
L_r	10 µH
C_r	0.27 µF, ECW Series
C_a	5 µF, B32674 Series

Table 4.3 Key components for the conventional boost PFC converter.

Component	Device Description
PFC switch	IPP65R099C6 (2 in parallel)
PFC diode	STTH8R06D
Diode bridge	GBJ2506
PFC inductor	250 µH

The experimental input voltage, input current, and output voltage waveforms for the proposed converter are provided in Figure 4.6. Test conditions were as follows: V_{in} = 120 V, V_o = 400 V, P_o = 650 W, f_s = 150 kHz. The input current is in phase with the input voltage, and its shape is close to a sinusoidal waveform, as expected.

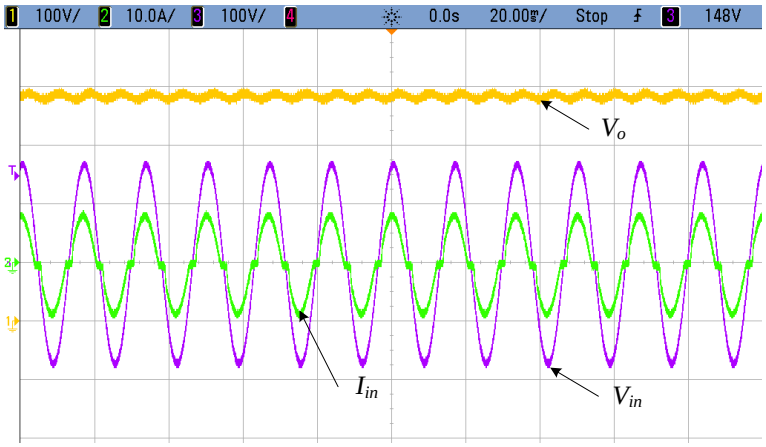


Figure 4.6 ZVS HRPWM converter experimental waveforms at 20ms/div of input voltage V_{in} (ch3: 100 V/div), input current I_{in} (ch2: 10 A/div) and output voltage V_o (ch1: 100 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Waveforms for the ZVS transition during turn-on for S_1 are provided in Figure 4.7 for positive line cycle operation, when S_1 is working as a PWM switch. According to Figure 4.7, there is no Miller plateau region in the gate voltage waveform, which confirms ZVS for S_1. ZVS occurs due to the negative current supplied by L_r, which discharges the body capacitance, C_{s1}, of S_1 prior to applying the gate signal. Once the voltage across the MOSFET has become zero, the gate signal is applied to the MOSFET. Note that the voltage across the switch is nominally the output voltage V_o (400 V) plus the relatively small ripple voltage (50 V) across C_r. The waveforms of the ZVS transition during turn-on for S_2 for negative line cycle operation are provided in Fig. 11 where S_2 is working as a PWM switch. It can be observed from Figure 4.8 that S_2 also achieves ZVS.

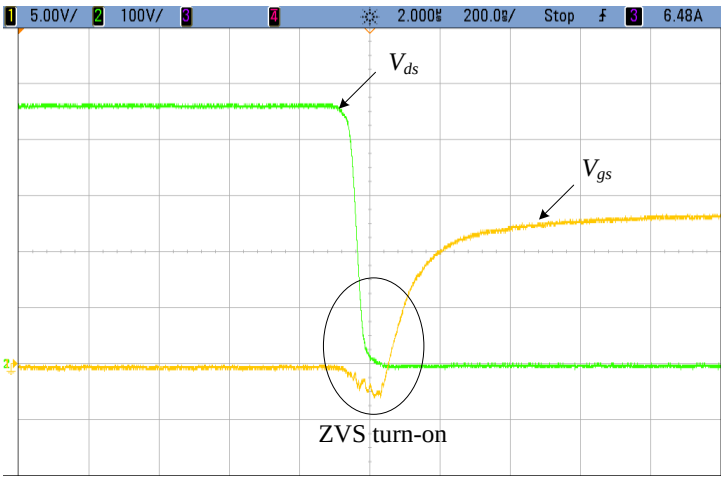


Figure 4.7 ZVS HRPWM converter experimental waveforms at 200ns/div of voltage across switch S_1, V_{ds} (ch2: 100 V/div) and gating signal for S_1, V_{gs} (ch1: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

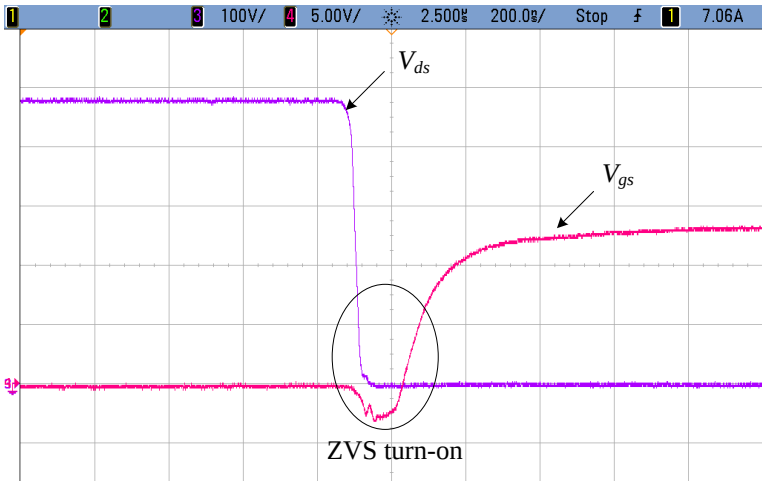


Figure 4.8 ZVS HRPWM converter experimental waveforms at 200ns/div of voltage across switch S_2, V_{ds} (ch3: 100 V/div) and gating signal for S_2, V_{gs} (ch4: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Waveforms of the current through the resonant inductor I_{Lr}, voltage across the resonant capacitor V_{Cr}, input current I_{in} and the gating signal for S_1 are provided in Figure 4.9.

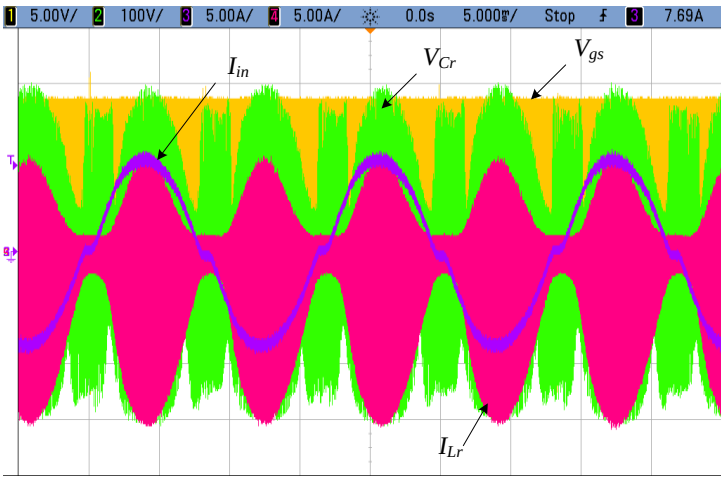


Figure 4.9 ZVS HRPWM converter experimental waveforms at 5ms/div of voltage across capacitor C_r, V_{Cr} (ch 2: 100 V/div), current through inductor L_r, I_{Lr} (ch 4: 5 A/div), input current I_{in} (ch3: 5 A/div) and gating signal for S_1, V_{gs} (ch1: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Waveforms of the resonant inductor current I_{Lr}, voltage across the resonant capacitor V_{Cr} and the gating signal for S_1 near the peak of AC input voltage are provided in Figure 4.10. It can be observed that the current through L_r is negative when the V_{gs} is high. This negative current initiates the ZVS transition during the turn-on period of PWM switches S_1 and S_2. It can be seen that there is a voltage spike on V_{Cr} which is due to coupled noise from the experimental prototype (coupled via EMI) with the change of the drain to source voltages across S_1 and S_2.

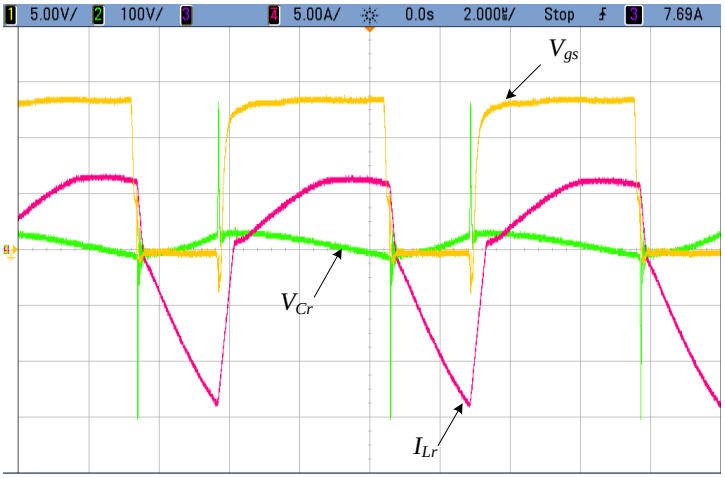


Figure 4.10 ZVS HRPWM converter experimental waveforms at 2μs/div of voltage across capacitor C_r, V_{Cr} (ch 2: 100 V/div), current through inductor L_r, I_{Lr} (ch 4: 5 A/div) and gating signal for S_1, V_{gs} (ch1: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Figure 4.11 and Figure 4.12 shows the waveforms of the current and voltage across D_1 and D_2, respectively. As shown in Figure 4.11 and Figure 4.12, the diode D_1 and D_2 are both turned off with ZCS. This happens due to the current flowing through L_r when the diodes are turned off. This way it can reduce some switching losses and switching noise.

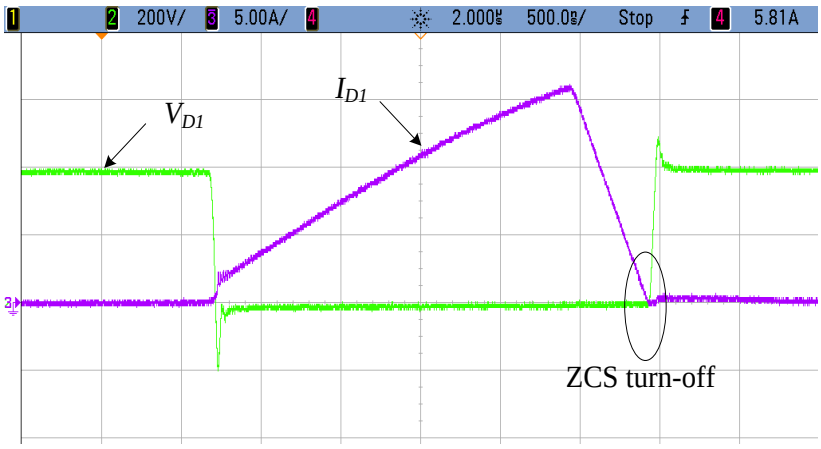


Figure 4.11 ZVS HRPWM converter experimental waveforms at 500ns/div of voltage across diode D_1, V_{D1} (ch 2: 200 V/div) and current through diode D_1, I_{D1} (ch 3: 5 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

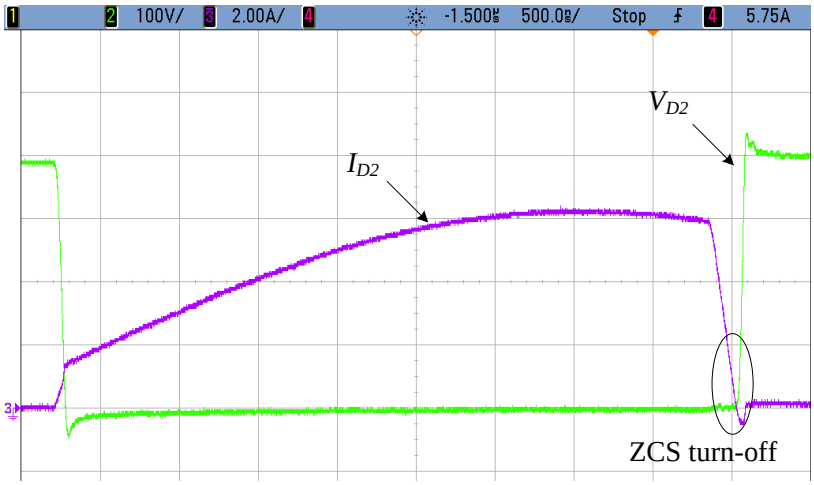


Figure 4.12 ZVS HRPWM converter experimental waveforms at 500ns/div of voltage across diode D_2, V_{D2} (ch 2: 100 V/div) and current through diode D_2, I_{D2} (ch 3: 2 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Curves of the measured converter efficiency versus output power at 100 V and 240 V input are provided in Figure 4.13. Total loss curves are provided in Figure 4.14 at 100 V input for the ZVS HRPWM and conventional boost PFC converter. The proposed converter achieves a peak efficiency of 96.95 % at 240 V input and 650 W load. The proposed converter maintains greater efficiency and lower power loss across the entire load range, and most notably at low input line operation, where the thermal stresses are maximum. Furthermore, the efficiency improvement at full load is 1 percentage point, representing a total power loss savings of 7 W. Note that the loss savings of 7 W is very close to the 6.9 W predicted in section 4.3.5. The improvement in the efficiency can be attributed to the fact that the proposed converter eliminates, or minimizes three major sources of losses compared with the conventional boost - these are the conduction losses in the diode bridge rectifier, the turn-on losses of the PFC switches and the reverse recovery losses of the output diodes. As further evidence of the loss reduction and heat spreading features of the proposed converter, thermal images of the PFC MOSFETs and the diode bridge for both the conventional boost PFC converter and the proposed soft-switching converter are provided in Figure 4.15 and Figure 4.16. It is observed that the maximum temperature of the diode bridge of the boost PFC converter is 88.8^{o}C compared

to 64.9° C for the proposed converter. Similarly, the PFC MOSFETs of the proposed converter operate cooler (i.e. max 93.4° C) compared with the PFC boost MOSFETs (i.e. max 105° C), showing the advantage of ZVS operation.

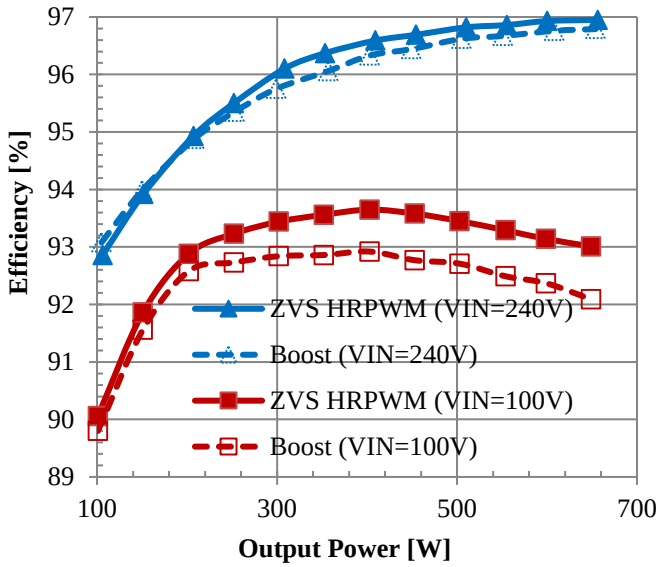


Figure 4.13 Efficiency as a function of load at V_{in} = 100 V and 240 V, V_o = 400 V and f_s = 150 kHz for the ZVS HRPWM and boost PFC converters.

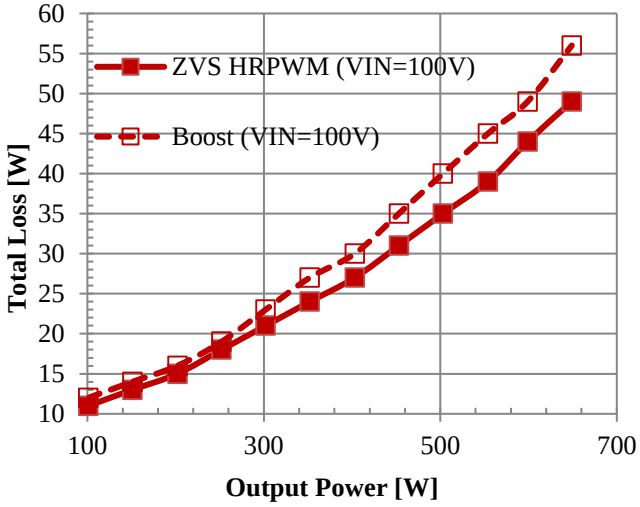
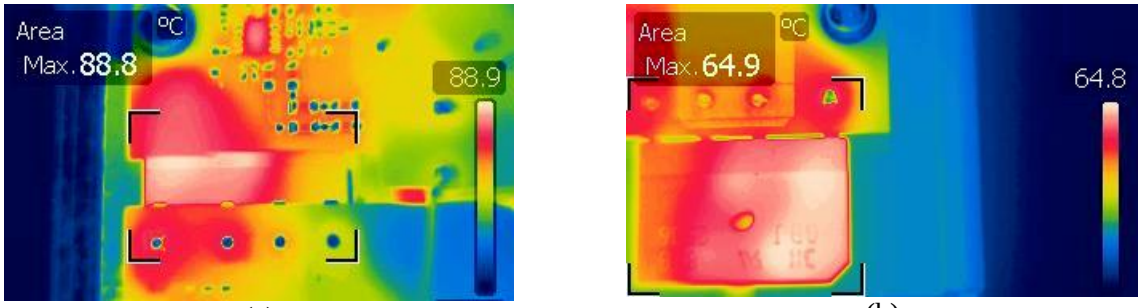
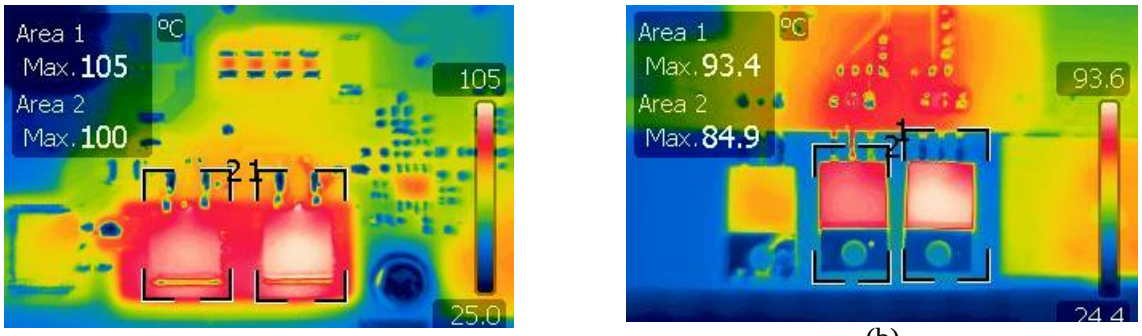


Figure 4.14 Total loss as a function of load at V_{in} = 100 V, V_o = 400 V and f_s = 150 kHz for the ZVS HRPWM and boost PFC converters.



(a) (b)

Figure 4.15 Thermal images of diode bridge rectifier: (a) boost PFC converter, and (b) ZVS HRPWM converter.



(a) (b)

Figure 4.16 Thermal images of PFC MOSFETs: (a) boost PFC converter, and (b) ZVS HRPWM converter.

Curves of the measured converter power factor versus output power for the proposed ZVS HRPWM converter are provided in Figure 4.17 at 100V and 240V input, respectively. It can be observed that the power factor is greater than 0.98 from half load to full load.

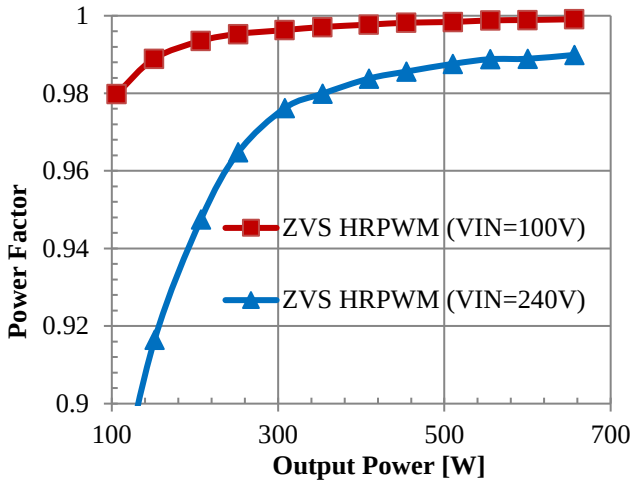


Figure 4.17 Power factor as a function of load at V_{in} = 100 V and 240 V, V_o = 400 V for proposed ZVS HRPWM converter.

In order to verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the EN 61000-3-2 standard in Figure 4.18 for 100 V and 240 V input. All converter harmonics are well below IEC standard.

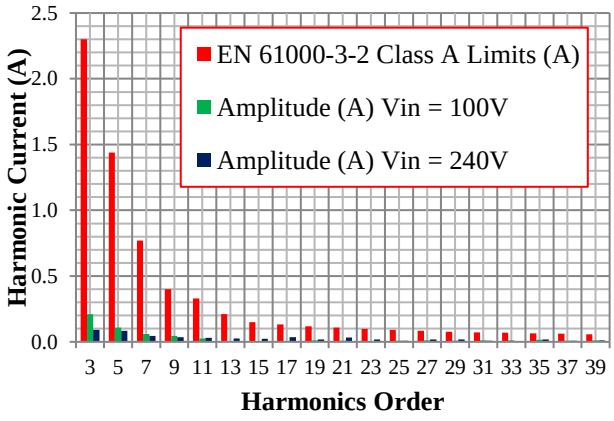


Figure 4.18 Input current harmonics at V_{in} = 100 V and 240 V at full load condition for proposed ZVS HRPWM converter.

4.5 Summary

This chapter presented a new soft-switching AC-DC PFC converter. The proposed converter has many advantages for practical implementation. This converter has inherent inrush current-limiting capabilities and can be easily implemented with standard average current mode control and the PWM switches can be driven with the same PWM signal, so extra circuitry is not required to sense both the positive, or and negative line-cycle operation. Moreover, the bridgeless operation eliminates the problem with heat management in a traditional diode rectifier preceding a boost PFC converter. The proposed converter reduces switching losses by realizing ZVS for the two PFC MOSFETs and one auxiliary MOSFET, and ZCS for the output rectifier diodes. An experimental prototype was been built to verify the proof-of-concept and the key experimental waveforms were provided. The converter power factor and efficiency measurements were provided as a function of load power at 100V and 240V input. The power factor is greater than 0.98 from half load to full load. The proposed converter achieves a peak efficiency of 96.95% at 240 V input and 650 W output power. Compared to the conventional hard-switched PFC boost converter at the maximum loss operating point (full load and 100 V AC input), the proposed converter achieves 1 percentage point efficiency improvement and operates with lower semiconductor device temperatures.

5 A High Voltage Gain Soft-Switching Bridgeless AC-DC Power Factor Correction Converter‡

5.1 Overview

In Chapter 4, a soft-switching AC-DC PFC converter was proposed and analyzed. In this converter, the voltage stress on the diodes is equal to the output voltage. In this chapter, a high voltage gain soft-switching AC-DC PFC converter is proposed which also has inherent inrush current-limiting capabilities. Unlike the converters presented in Chapters 3 and 4 and conventional boost and bridgeless boost converters, the switching transitions of the proposed converter in this Chapter occur with a voltage level equivalent to half of the output voltage, which reduces switching losses. With reduced voltage stress, a low voltage drop fast recovery silicon diode can also be used. Moreover, this converter nearly eliminates turn-on switching losses by achieving ZVS for all switches and ZCS at turn-off for the output rectifier diodes, which nearly eliminates reverse recovery losses. The proposed converter is also bridgeless, which eliminates the heat management issues in diode bridge rectifier. The proposed soft-switching bridgeless AC-DC PFC converter topology is illustrated in Figure 5.1.

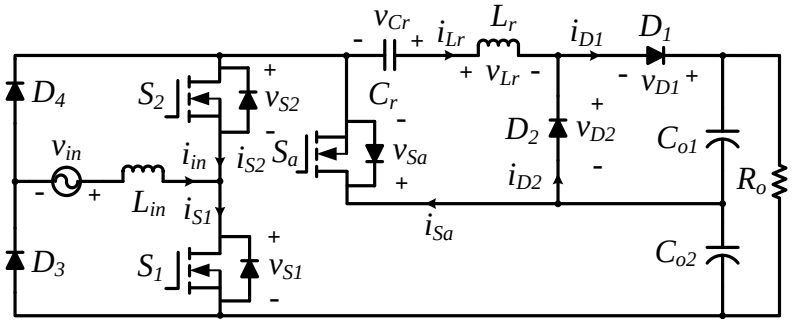


Figure 5.1 Proposed soft-switching bridgeless AC-DC PFC converter topology.

‡ The content of this chapter has been submitted to the following journal:
[1] M. Alam, W. Eberle, D. Gautam and C. Botting, "A High Voltage Gain Single-Phase Soft-Switching Bridgeless Power Factor Correction Rectifier" IEEE Transactions on Power Electronics.

Section 5.2 provides the modes of operation of the proposed converter and the detailed operating conditions for soft-switching are presented. In Section 5.3, a detailed analysis and a design example of the proposed converter is presented along with a converter loss analysis. Finally, Section 5.4 provides experimental results showing soft-switching operation. A summary is provided in Section 5.5

5.2 Modes of Operation

In the paragraphs that follow, the operation of the proposed converter is explained in detail and a mathematical analysis of its steady-state operation is provided. This converter operates in hybrid-resonant mode when the switches are on and PWM mode when the switches are off. Both modes occur during a single switching cycle. In the resonant mode, inductor L_r and capacitor C_r resonate. The resonant frequency has a significant impact on the operation of the converter, and can be higher, lower or equal to the switching frequency. As discussed in Chapter 3 section 3.2, below resonance operation is preferred to reduce switching losses so the following discussion assumes below resonance operation. The waveforms of the key components and the different modes of operation of the proposed converter are given in Figure 5.2 and Figure 5.3, respectively. The modes of operation discussed below refer to the positive line cycle operation of the AC input. The below-resonance operation has five different modes of operation during one switching period and they are discussed as follows.

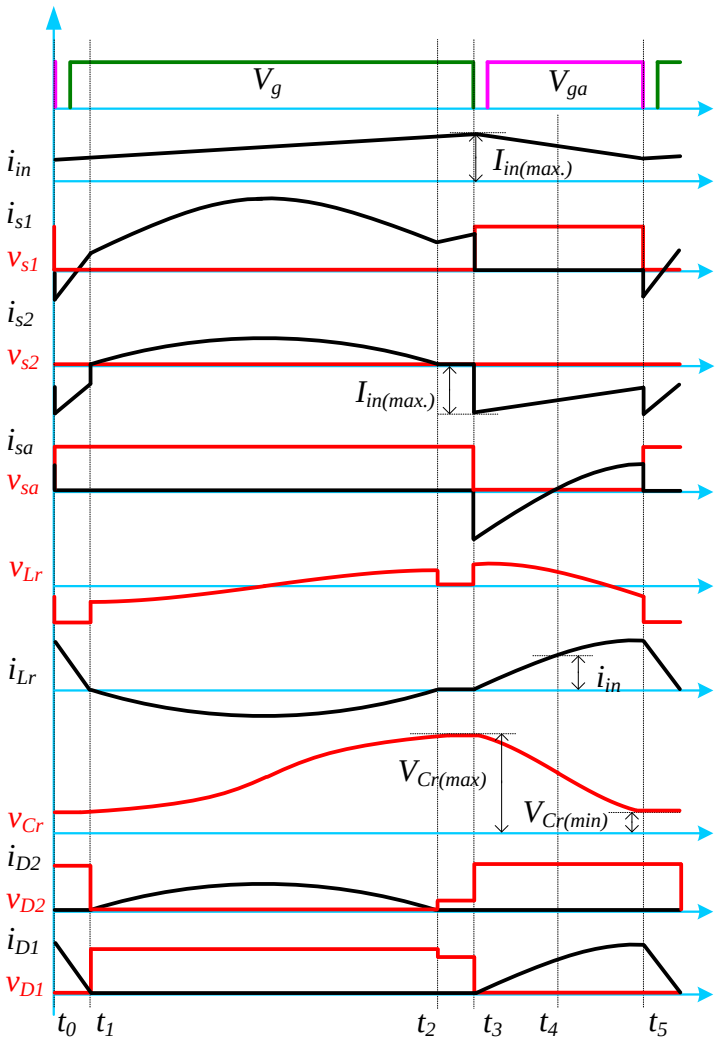


Figure 5.2 Proposed soft-switching converter waveforms in CCM.

Interval-1(t_0-t_1): This mode starts when switch S_a turns off. In order to achieve ZVS at turn-on for switch S_1, capacitor C_{s1} must be fully discharged. After discharge is complete, the current through switch S_1 is clamped by body diode D_{s1}, and the gate pulse of switch S_1 has to be applied before the current through switch S_1 changes and starts charging C_{s1}. The gate signal V_g enables the soft transition condition for switch S_1 and minimizes switching losses. During this interval the resonant current i_{Lr} and input current i_{Lin} linearly

decrease and increase, respectively, and are given by (5-1) and (5-2), respectively. The diodes D_1 and D_2 also realize ZCS turn-off and turn-on respectively. The equivalent circuit is provided in Figure 5.3(a).

$$i_{Lin}(t) = \frac{V_{in}}{L_{in}}(t - t_0) + i_{Lin}(t_0) \tag{5-1}$$

$$i_{Lr}(t) = \frac{V_{Cr(min)} - V_0}{L_r}\,(t - t_0) + i_{Lr}\,(t_0) \tag{5-2}$$

Interval-2(t_1-t_2): This interval begins with the resonance between L_r and C_r. The resonant current i_{Lr} continues to flow through switch S_1 and the input current still increases linearly. Hence, the switch current i_{S1} during this interval is the summation of the input current i_{Lin} and the resonant current i_{Lr}. When the resonant current i_{Lr} is zero, it enables ZCS turn-off of diode D_2. The current i_{Lr} and the voltage v_{Cr} of the resonant tank are given by (5-3) and (5-4), respectively. The equivalent circuit is provided in Figure 5.3(b).

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{r1}}{Z}\,\sin\big(\omega_r(t - t_1)\big) \tag{5-3}$$

$$v_{Cr}(t) = V_{r1}\left[\cos\big(\omega_r(t - t_1)\big) - 1\right] + v_{Cr}(t_1) \tag{5-4}$$

where $V_{r1} = V_{Cr(min)} - V_{C2}$, $Z = \sqrt{(L_r/C_r)}$ and $\omega_r = 1/\sqrt{(L_r\,.\,C_r)}$

Interval-3(t_2-t_3): This mode starts when the resonant current i_{Lr} is zero and the diode, D_2 stops conducting. The input current i_{Lin} still increases linearly and stores energy in L_{in}. This interval ends when the gate signal V_g turns off switch S_1. It should be noted that the turn-off current of switch S_1 is the same as the turn-off current of the conventional PFC boost switch. The equivalent circuit is provided in Figure 5.3(c).

Interval-4(t_3-t_4): This interval starts when the switch S_1 turns off. During this interval the capacitor C_{sa} discharges to initiate the ZVS turn-on of switch S_a. The gate pulse of switch S_a has to be applied before the current through switch S_a reverses. The gate signal V_{ga} enables the ZVS transition for switch S_a and minimizes the turn-on switching losses. The resonant operation between L_r and C_r is started and the input

current i_{Lin}, the resonant current i_{Lr} and the voltage v_{Cr} of the resonant tank are given by equations (5-5), (5-6) and (5-7), respectively. The equivalent circuit is provided in Figure 5.3(d).

$$i_{Lin}(t) = \frac{V_{in} - V_{C2}}{L_{in}}(t - t_3) + i_{Lin}(t_3) \tag{5-5}$$

$$i_{Lr}(t) = -\,i_{Cr}(t) = \frac{V_{r2}}{Z}\sin\big(\omega_r(t - t_3)\big) \tag{5-6}$$

$$v_{Cr}(t) = V_{r2}\big[\cos\big(\omega_r(t - t_3)\big) - 1\big] + v_{Cr}(t_3) \tag{5-7}$$

where $V_{r2} = V_{Cr(max)} - V_{C1}$, $Z = \sqrt{(L_r/C_r)}$ and $\omega_r = 1/\sqrt{(L_r\,.\,C_r)}$

Interval-5(t_4-t_5): This mode starts when the current through switch S_a reverses and the input current i_{Lin} equals the resonant current i_{Lr}. Hence, the resonant current i_{Lr} during this interval is the summation of the input current i_{Lin} and the switch current of S_a. This interval ends when the gate signal V_{ga} turns off switch S_a. The equivalent circuit is provided in Figure 5.3(e).

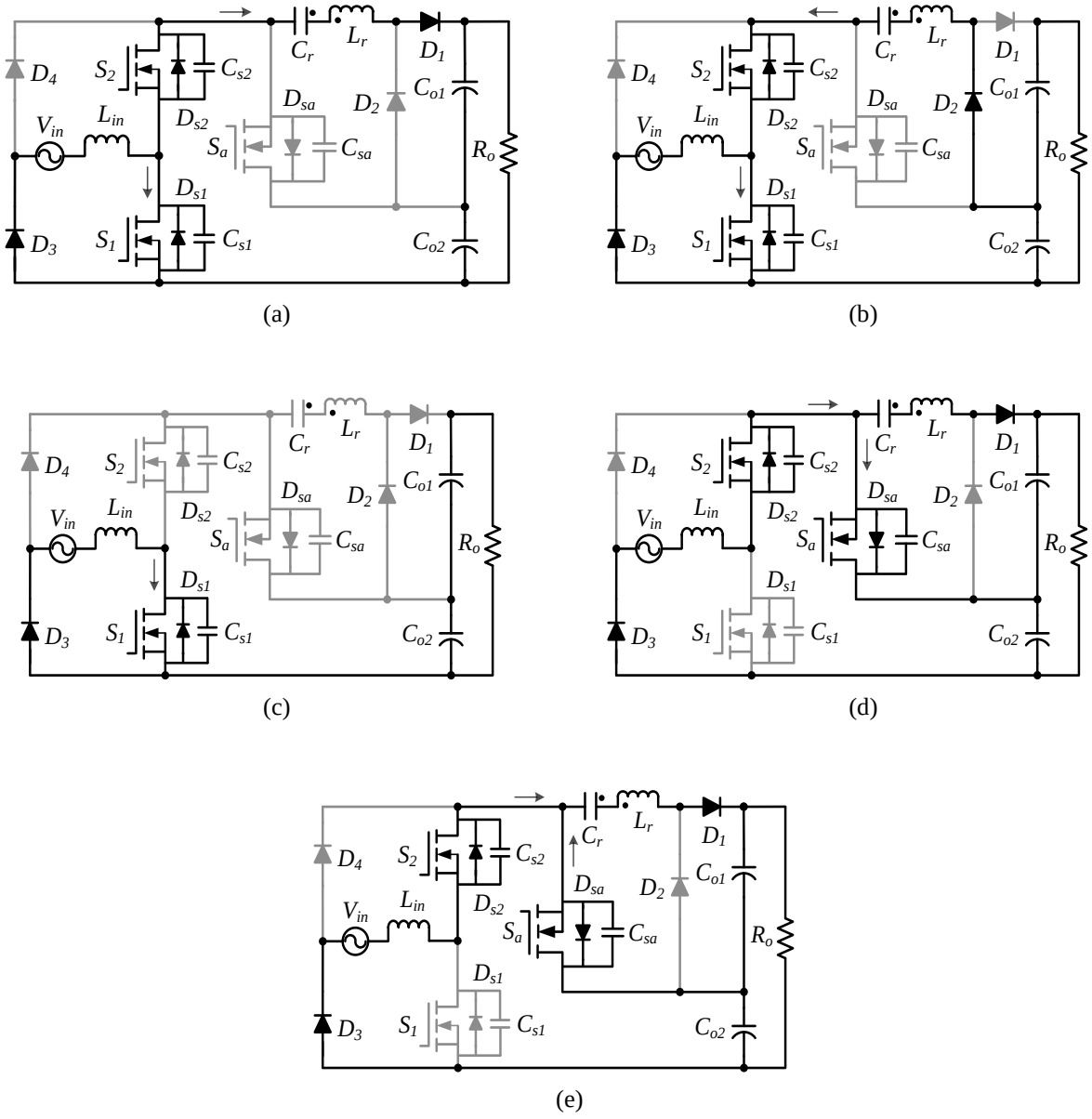


Figure 5.3 Proposed converter modes of operation.

5.3 Analysis and Design

5.3.1 DC Voltage Conversion Ratio

In steady state, it is assumed that the voltages across capacitors C_1 and C_2 are constant in a switching period. Thus the DC voltage conversion ratio can be calculated in a similar way as discussed in Chapter 4 section 4.3.1 and is given by (5-8).

$$V_o = V_{C1} + V_{C2} = \frac{2}{1-D}\ V_{in} \tag{5-8}$$

where V_{C1} and V_{C2} are given by (5-9) and (5-10) respectively.

$$V_{C2} = \frac{1}{1-D}\ V_{in} \tag{5-9}$$

$$V_{C1} = \frac{1}{1-D}\ V_{in} \tag{5-10}$$

In steady-state operation, the average load current can be found from interval-2, and is given by (5-11).

$$I_o = \frac{V_o}{R_o} = \left[\frac{1}{T_s}\int_0^{\frac{T_r}{2}} \left(V_{Cr(min)} - V_{C2}\right)\sqrt{\frac{C_r}{L_r}}\ \sin(\omega_r t)dt\right] \tag{5-11}$$

The minimum and maximum resonant capacitor voltage can be obtained from (5-11) and are given by (5-12) and (5-13) , respectively.

$$V_{Cr(min)} = V_{C2} - \frac{I_o}{2C_r f_s} \tag{5-12}$$

$$V_{Cr(max)} = V_{C2} + \frac{I_o}{2C_r f_s} \tag{5-13}$$

5.3.2 ZVS Requirements for the Switches

In order to achieve ZVS for PFC switches S_1 and S_2, the gate signal V_g has to be applied when the switch S_a turns off during interval-1 at t_0. The current required to achieve ZVS is determined by the difference between the input current i_{Lin} and the resonant current i_{Lr}. Hence, the ZVS current $I_{S1\_S2(ZVS)}$ is given by (5-14).

$$I_{s1\_S2(ZVS)} = \frac{L_{in}[V_{in}I_oT_s\omega_r\, sin(\omega_r(1-D)Ts) - 2P_o] + DT_sV_{in}^2}{2V_{in}L_{in}} \tag{5-14}$$

The current required to achieve ZVS for switch S_a is determined by the maximum input current i_{Lin} when the PFC switches S_1 and S_2 are turned off during interval-5. Hence, this current, $I_{Sa(ZVS)}$ is given by (5-15).

$$I_{sa(ZVS)} = \frac{2P_oL_{in} + DT_sV_{in}^2}{2} \tag{5-15}$$

The energy stored in the resonant inductor L_r has to be sufficient to discharge the body capacitor C_{s1} of switch S_1 during interval-1 to initiate the ZVS condition. As a result the condition in (5-16) has to be satisfied in order to achieve ZVS for the PFC switches S_1 and S_2.

$$\frac{1}{2}\, L_r\, I_{s1-S2(ZVS)}^2 \geq \frac{1}{2}(C_{s1} + C_{sa})\left(\frac{V_{in}}{1-D}\right)^2 \tag{5-16}$$

Similarly, the energy stored in the input inductor L_{in} has to be sufficient to discharge the body capacitor C_{sa} of switch S_a during interval-3 to achieve ZVS. Therefore, the condition in (5-17) must be satisfied for switch S_a to achieve ZVS.

$$\frac{1}{2}\, L_{in}\, I_{in(max)}^2 \geq \frac{1}{2}(C_{s1} + C_{sa})\left(\frac{V_{in}}{1-D}\right)^2 \tag{5-17}$$

5.3.3 Design Methodology

A design example is provided to determine the input inductor L_{in}, the optimal resonant frequency f_r, the resonant inductor L_r and the resonant capacitor C_r. The specifications for the example are listed in Table 5.1. The input voltage range is the AC line voltage of 85 V to 140 V, which includes a 10 % tolerance for the nominal values.

Table 5.1 Design Specifications

Parameter	Value
Input voltage range, V_{in}	85 - 140 Vac
Input current ripple, $I_{\%Ripple}$	25%
Switching frequency, f_s	150 kHz
Rated output power, P_o	650 W
Output Voltage, V_o	400 Vdc

In order to calculate the input inductor L_{in} it is considered to have 25% input current ripple, $I_{\%Ripple}$ Therefore, L_{in}, is determined to be 207 µH, using (5-18).

$$L_{in} = \frac{V_{in(min)}^2}{I_{\%Ripple}\, f_s\, P_o}\left(1 - \frac{\sqrt{2}\, V_{in(min)}}{V_o}\right) = 207\ \mu H \tag{5-18}$$

In order to calculate the resonant frequency, below-resonance operation is assumed in order to reduce the turn-off losses of the PFC switches. Hence, using (3-4) and (5-8), where $T_r = 1/f_r$ and $T_{on} = D/f_s$, the minimum resonant frequency is f_r = 130 kHz. The resonant inductor value can be determined to maintain ZVS by using (5-16) and (3-2) as $L_r \geq 20$ µH and $C_r \geq 0.5$ µF.

5.3.4 Converter Loss Analysis

A detailed loss analysis was performed using standard analytical techniques and PSIM simulation results (to model conduction losses) for the benchmark AC-DC boost converter and the proposed high gain

HRPWM ZVS converter. The estimated loss distribution is provided in Figure 5.4 using 150 kHz switching frequency, 100 V input and a 650 W load. The low line 100 V input operating point was chosen since semiconductor conduction losses are highest at this point, therefore it is the point used to size the heatsinks for a prototype.

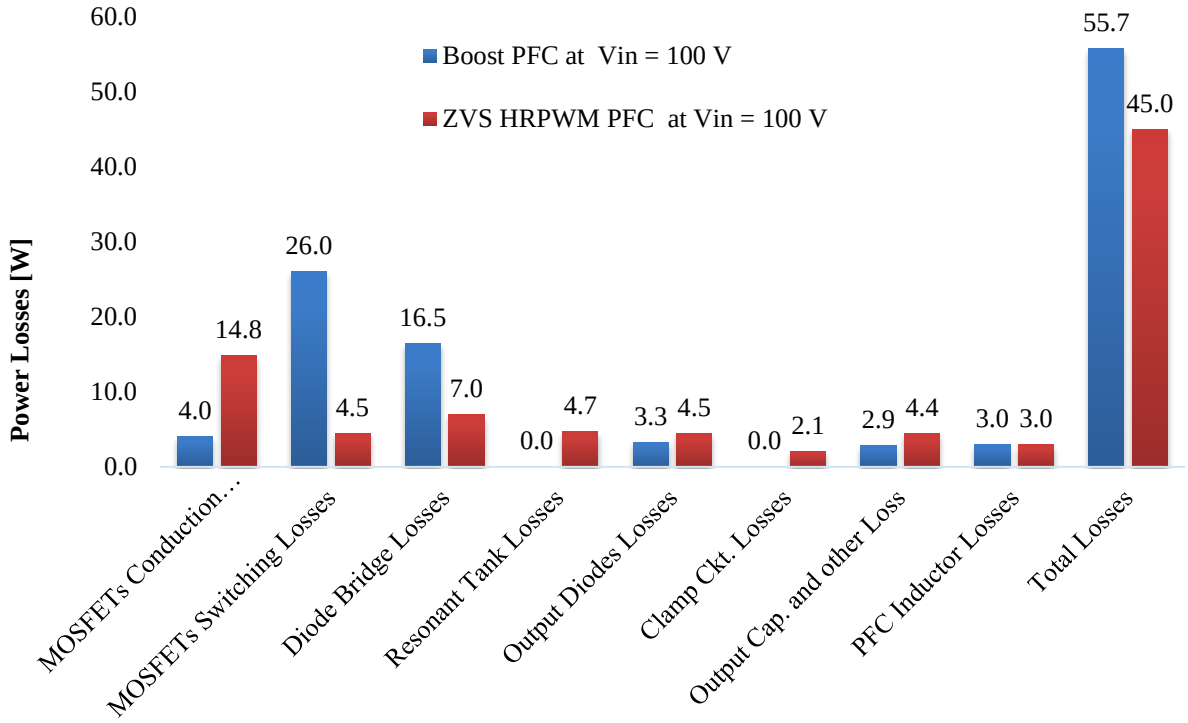


Figure 5.4 Loss distribution comparison at V_{in} = 100 V, f_s = 150 kHz, P_o = 650 W, V_o = 400 V.

Total losses in the converter are estimated to be reduced by 10.7 W (from 55.7 W to 45 W) compared to the benchmark boost PFC. The proposed converter nearly eliminates the switching losses, so the PFC MOSFET losses, including both conduction and switching are lower and the diode bridge conduction losses are reduced by 9.5 W (from 16.5 W to 7 W). In addition to the cost of the additional circuit components, the performance penalty for adding the auxiliary components includes increased circulating currents, resulting in slightly increased conduction losses. However, given the reduction in frequency dependent losses, the increased conduction losses are more than offset (i.e. by 10.7 W). Compared to the conventional

boost PFC converter, one of the main benefits of the proposed converter is improved heat distribution, since the most lossy components (i.e. the PFC MOSFETs and bridge diodes) will run cooler due to lower losses. It is noted that these results are at 150 kHz switching frequency. At higher frequencies, the loss reduction would be more substantial. The experimental results presented in the next section verify the analysis results and the primary conclusion related to reduce losses in the PFC MOSFETs and bridge diodes.

5.4 Experimental Results

The performance of the proposed ZVS converter was evaluated and compared to the performance of the conventional PFC boost converter using 650 W experimental prototype circuits. A complete schematic of the proposed converter is provided in Figure A- 4 in the Appendix. Table 5.2 and Table 5.3 show the key components used in the proposed ZVS converter and conventional PFC boost converter, respectively.

Table 5.2 Key components for the high gain ZVS HRPWM converter.

Component	Device Description
S_1, S_2, S_a	IPP65R099C6
D_1, D_2	STTH8R06D
D_3, D_4	GBJ2506
L_{in}	250 µH
L_r	25 µH
C_r	0.5 µF, ECW Series

Table 5.3 Key components for the conventional PFC converter.

Component	Device Description
PFC switch	IPP65R099C6 (2 in parallel)
PFC diode	MUR860
Diode bridge	GBJ2506
PFC inductor	250 µH

The experimental input voltage and input current waveforms for the proposed converter are provided in Figure 5.5. Test conditions were as follows: V_{in} = 120 V, V_o = 400 V, P_o = 650 W, f_s = 150 kHz. The input current is in phase with the input voltage, and its shape is close to a sinusoidal waveform, as expected.

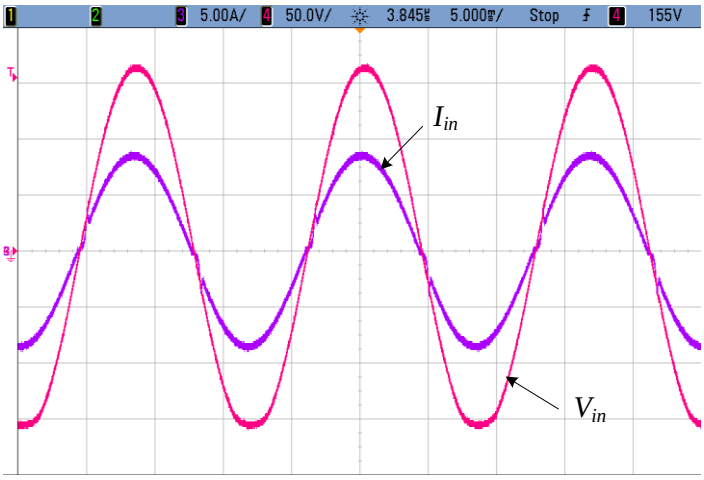


Figure 5.5 High voltage gain soft-switching converter experimental waveforms at 5ms/div of input voltage V_{in} (ch3: 100 V/div) and input current I_{in} (ch3: 5 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

The voltages across the MOSFETs S_1 and S_2 are presented in Figure 5.6 and Figure 5.7, respectively, where S_1 and S_2 are working as a PFC switch for the positive and negative line cycle operations, respectively. It can be seen that the gate voltage waveforms are clean and there is no Miller plateau region, indicating ZVS for S_1 and S_2 during the turn-on transitions. It is also noted that all commutations occur with a voltage level equivalent to near half the output voltage V_o, even though all the switches block the full dc-link voltage. This yields low switching losses.

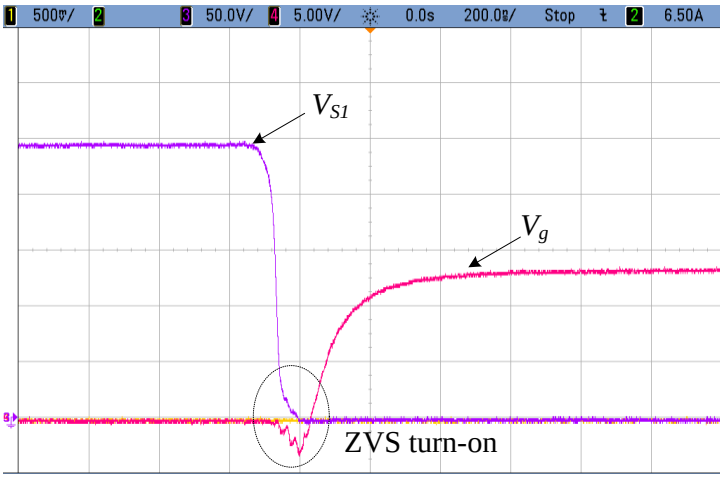


Figure 5.6 High voltage gain soft-switching converter experimental waveforms at 200ns/div of voltage across switch S_1, V_{S1} (ch3: 50 V/div) and gating signal for S_1, V_{GS1} (ch4: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

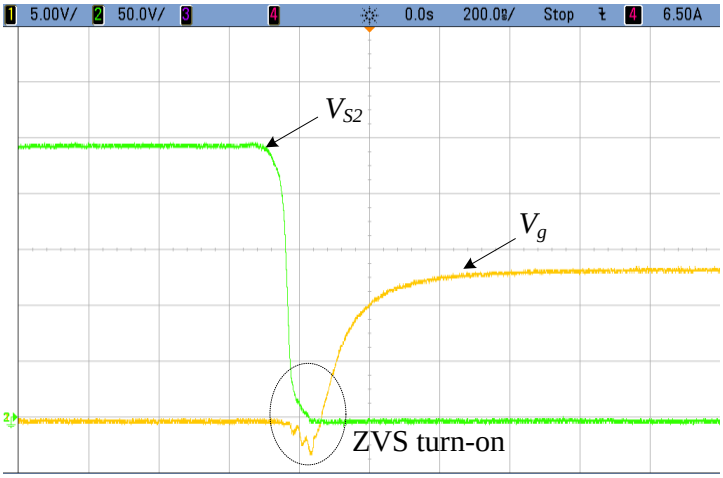


Figure 5.7 High voltage gain soft-switching converter experimental waveforms at 200ns/div of voltage across switch S_2, V_{S2} (ch2: 50 V/div) and gating signal for S_2, V_{GS2} (ch1: 5 V/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Figure 5.8 and Figure 5.9 show the waveforms of the current and voltage across diodes D_1 and D_2, respectively. As shown in Figure 5.8 and Figure 5.9, the diode D_1 and D_2 are both turned off with ZCS. With ZCS, the diode losses and switching noise are minimized.

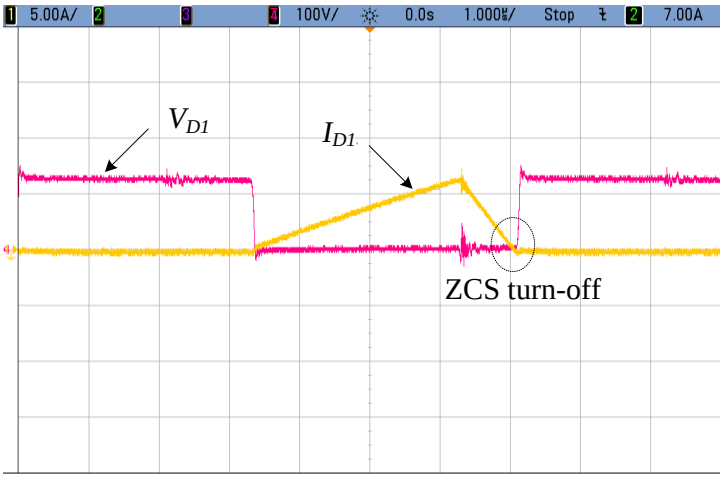


Figure 5.8 High voltage gain soft-switching converter experimental waveforms at 1µs/div of voltage across diode D_1, V_{D1} (ch 4: 100 V/div) and current through diode D_1, I_{D1} (ch 1: 5 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

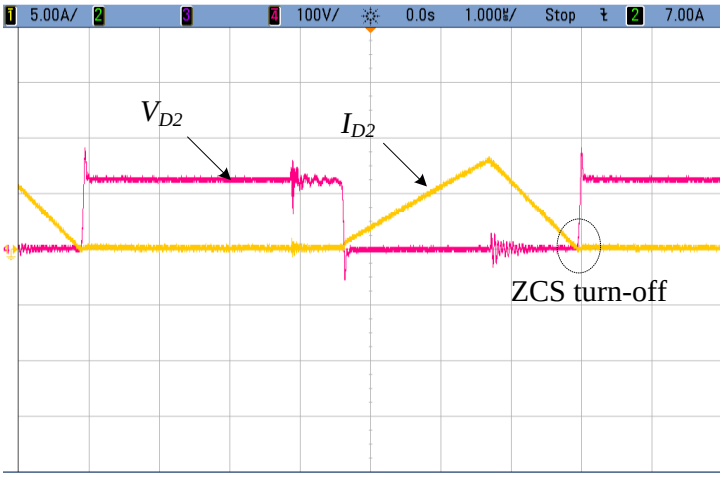


Figure 5.9 High voltage gain soft-switching converter experimental waveforms at 1µs/div of voltage across diode D_2, V_{D2} (ch 4: 100 V/div) and current through diode D_2, I_{D2} (ch 1: 5 A/div) at V_{in} = 120 V, V_o = 400 V, P_o = 650 W and f_s = 150 kHz.

Curves of the measured converter efficiency versus output power at 100 V input are provided in, Figure 5.10. Curves of total loss are provided in Figure 5.11 for 100 V input for the high gain ZVS HRPWM and conventional boost PFC converters, respectively. The proposed converter achieves a peak efficiency of 94.6 % at 350 W load. The proposed converter maintains greater efficiency and lower power loss across the

entire load range. Furthermore, the efficiency improvement at full load is 1.5 percentage points, representing a total power loss savings of 10 W. Note that the measured loss savings of 10 W is very close to the 10.7 W predicted analytically in section 5.3.4. The efficiency improvement can be attributed to the proposed converter eliminating, or minimizing three major sources of loss compared with the conventional boost: the conduction losses in the diode bridge rectifier, the turn-on losses of the PFC switches, and the reverse recovery losses in the output diodes.

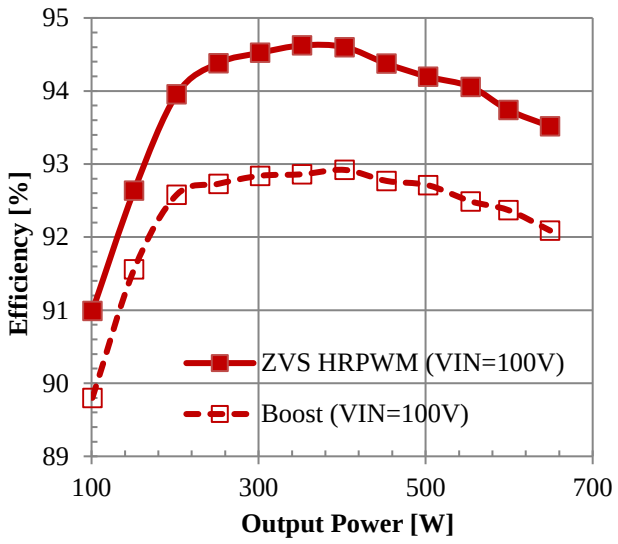


Figure 5.10 Efficiency as a function of load at V_{in} = 100 V, V_o = 400 V and f_s = 150 kHz for the proposed high gain ZVS HRPWM and the benchmark boost PFC converters.

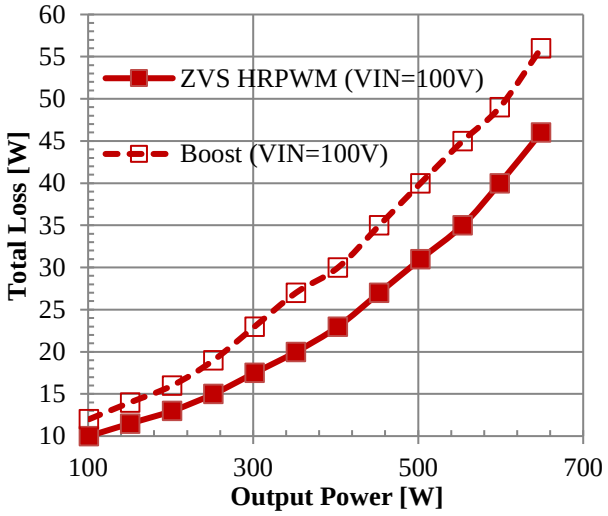


Figure 5.11 Total loss as a function of load at V_{in} = 100 V, V_o = 400 V for the proposed high gain ZVS HRPWM and the benchmark boost PFC converters.

The curve of the measured converter power factor versus output power for the proposed high gain ZVS HRPWM converter is provided in Figure 5.12 at 100V input. The power factor is greater than 0.99 from 25% load to full load.

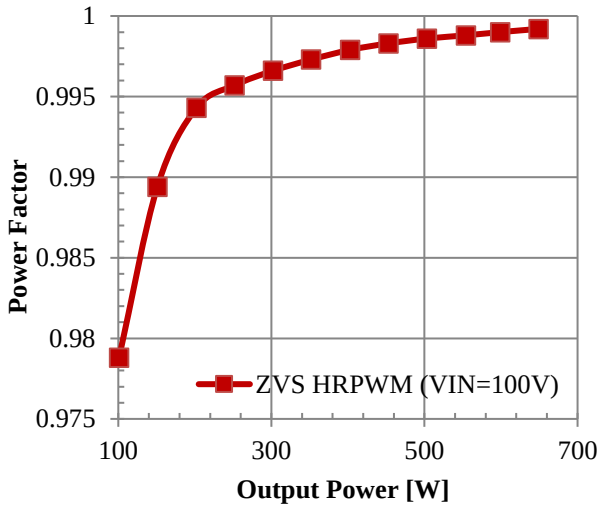


Figure 5.12 Power factor as a function of load at V_{in} = 100 V, V_o = 400 V for the proposed high gain ZVS HRPWM converter.

In order to verify the quality of the input current in the proposed topology, its harmonics up to the 39th harmonic are given and compared with the EN 61000-3-2 standard in Figure 5.13 for 100 V and 240 V input. All converter harmonics are well below IEC standard.

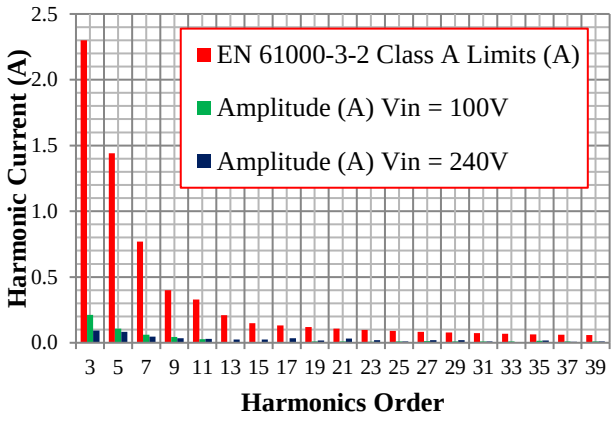


Figure 5.13 Input current harmonics at V_{in} = 100 V and 240 V at full load condition for proposed ZVS HRPWM converter.

5.5 Summary

A new high voltage gain soft-switching HRPWM AC-DC PFC converter was presented in this chapter. Unlike the conventional boost, or bridgeless boost converters, the switching commutations of the proposed converter occur with a voltage level equivalent to the summation of half of the output voltage and the voltage ripple on the resonant capacitor, which yields low switching losses. This converter has inherent inrush current-limiting capabilities. Moreover, the proposed converter minimizes switching losses by achieving ZVS for all switches and ZCS for the output rectifier diodes, which reduces the reverse recovery losses. The proposed converter is also bridgeless, which minimizes the heat management issues in diode bridge rectifier required before the input of the conventional boost PFC. The high voltage gain soft-switching converter operation and analysis were presented. An experimental prototype was built to verify the proof-of-concept and the key experimental waveforms were provided. The converter power factor and efficiency measurements were provided as a function of load power at 100V input. The power factor is

greater than 0.99 from 25% load to full load. The proposed converter achieves a peak efficiency of 94.6% at 100 V input and 350 W output power. Compared to the conventional hard-switched PFC boost converter at the maximum loss operating point (full load and 100 V ac input), the proposed converter achieves a 1.5 percentage point efficiency improvement.

6 A Soft-Switching Bridgeless Isolated Single-Stage AC-DC PFC Converter

6.1 Overview

In Chapters 3, 4 and 5, three novel non-isolated AC-DC PFC converters were proposed and analyzed. As discussed in Chapter 1, in most applications, following an AC-DC PFC converter, a secondary DC-DC stage is required to meet the regulation and galvanic isolation. This second stage converts the DC bus voltage of the front end non-isolated AC-DC PFC converter into a regulated output DC voltage. Typically, this system is known as two-stage system and it is well suited for high power applications. In this chapter, a soft-switching single-stage AC-DC PFC converter is proposed such that there is no dedicated PFC converter in the front end. The motivation for the work is the common use of single-stage PFC converters in low power applications requiring isolation. The proposed converter features inherent inrush current-limiting capabilities, low conduction loss due to low voltage stress of the secondary diodes, no dc magnetizing current for the transformer, and no stored energy in the transformer. Moreover, since the primary MOSFETs are turned on with ZVS and the secondary diodes are turned off with ZCS, the proposed converter has minimal switching losses. In addition, the input filter size can be minimized due to a continuous input current (i.e. CCM operation), and the output filter does not require an inductor. Therefore, the proposed converter has the desired features of high efficiency and high power density. The two primary MOSFETs can be driven with the same PWM signal, and sensing both the positive and negative AC line cycle operation is not required, enabling simplified control. The proposed soft-switching bridgeless single-stage AC-DC PFC converter topology is illustrated in Figure 6.1.

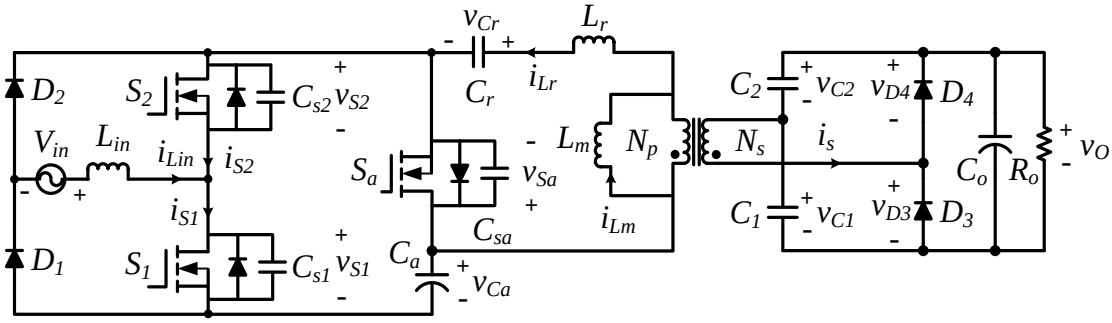


Figure 6.1 Proposed soft-switching bridgeless single-stage isolated converter.

Section 6.2 provides the modes of operation of the proposed converter, including the details of soft-switching operation. In Section 6.3, a detailed analysis and a design example of the proposed converter is presented. Finally, Section 6.4 provides the simulation results showing the soft-switching operation.

6.2 Modes of Operation

In the paragraphs that follow, the operation of the proposed converter is explained in detail and a mathematical analysis of its steady-state operation is provided. For simplicity, the discussion refers only to the positive AC half-line cycle operation over one switching cycle, and all components are ideal except the MOSFETs, which include the output capacitance and anti-parallel body diode. It is also assumed that the capacitances of C_a, C_r, C_1 and C_2 are large enough to be considered constant voltage sources. The key waveforms and operational modes for the proposed converter are provided in Figure 6.2 and Figure 6.3, respectively.

Interval-1(t_0-t_1): This mode starts when the secondary current I_s reaches zero and D_3 turns off at t_0. At t_1, D_4 turns on as shown in Figure 6.3(a). During this mode, the MOSFET S_1 is carrying a portion of the boost inductor current I_{Lin} and the transformer primary current I_{Lr}, which increase linearly. The slope of the boost inductor current I_{Lin} and the transformer primary current I_{Lr} are given by (6-1) and (6-2), respectively.

$$\frac{d}{dt} I_{Lin} = \frac{V_{in}}{L_{in}} \tag{6-1}$$

$$\frac{d}{dt} I_{Lr} = \frac{1}{L_r}\left[(V_{Ca} - V_{Cr}) - \frac{N_P}{N_S} V_{C2}\right] \tag{6-2}$$

The transformer's secondary current I_s flows through D_4, and increases linearly while C_1 is discharged and C_2 is charged.

Interval-2(t_1-t_2): This mode starts when S_1 turns off at t_1. During this interval, the sum of I_{Lin} and I_{Lr} initially flows through C_{s1} and C_{sa}, and when C_{sa} is fully discharged to zero the sum of I_{Lin} and I_{Lr} flows to the body diode D_{sa}. This situation initiates the ZVS turn-on of S_a. The gate signal V_{g_Sa} is applied to turn-on S_a with ZVS. During this mode, the boost inductor current I_{Lin} and the transformer primary current I_{Lr} decrease linearly. The equivalent circuit for this mode of operation is shown in Figure 6.3(b). The slope of the boost inductor current I_{Lin} and the transformer primary current I_{Lr} are given by (6-3) and (6-4), respectively.

$$\frac{d}{dt} I_{Lin} = \frac{V_{in} - V_{Ca}}{L_{in}} \tag{6-3}$$

$$\frac{d}{dt} I_{Lr} = \frac{1}{L_r}\left[(-V_{Cr}) - \frac{N_P}{N_S} V_{C2}\right] \tag{6-4}$$

The transformer's secondary current I_s flows through D_4, and decreases linearly while C_2 is discharged and C_1 is charged.

Interval-3(t_2-t_3): This mode starts when I_s decreases to zero at t_2 and D_4 turns off. During this mode D_3 is turned on, and the boost inductor current I_{Lin} and the transformer primary current I_{Lr} decrease linearly; their slopes are given by (6-3) and (6-5), respectively. The transformer's secondary current I_s flows through D_3, and decreases linearly while C_2 is discharged and C_1 is charged. The equivalent circuit for this mode of operation is shown in Figure 6.3(c).

$$\frac{d}{dt}I_{Lr} = \frac{1}{L_r}\left[(-V_{Cr}) + \frac{N_P}{N_S}\,V_{C1}\right] \tag{6-5}$$

Interval-4(t_3-t_4): This mode starts when S_a is turned off at t_3. During this interval, the sum of I_{Lin} and I_{Lr} initially flows through C_{s1} and C_{sa} while charging C_{sa} and discharging C_{s1}. When C_{s1} is fully discharged to zero, the sum of I_{Lin} and I_{Lr} flows to the body diode D_{s1}. This situation initiates the ZVS turn-on of S_1. The gate signal $V_{g\_S1/S2}$ is applied to turn-on S_1 with ZVS. The boost inductor current I_{Lin} increases linearly similarly as interval-1 and the transformer primary current I_{Lr} increases abruptly and is given by (6-6).

$$\frac{d}{dt}I_{Lr} = \frac{1}{L_r}\left[(V_{Ca} - V_{Cr}) + \frac{N_P}{N_S}\,V_{C1}\right] \tag{6-6}$$

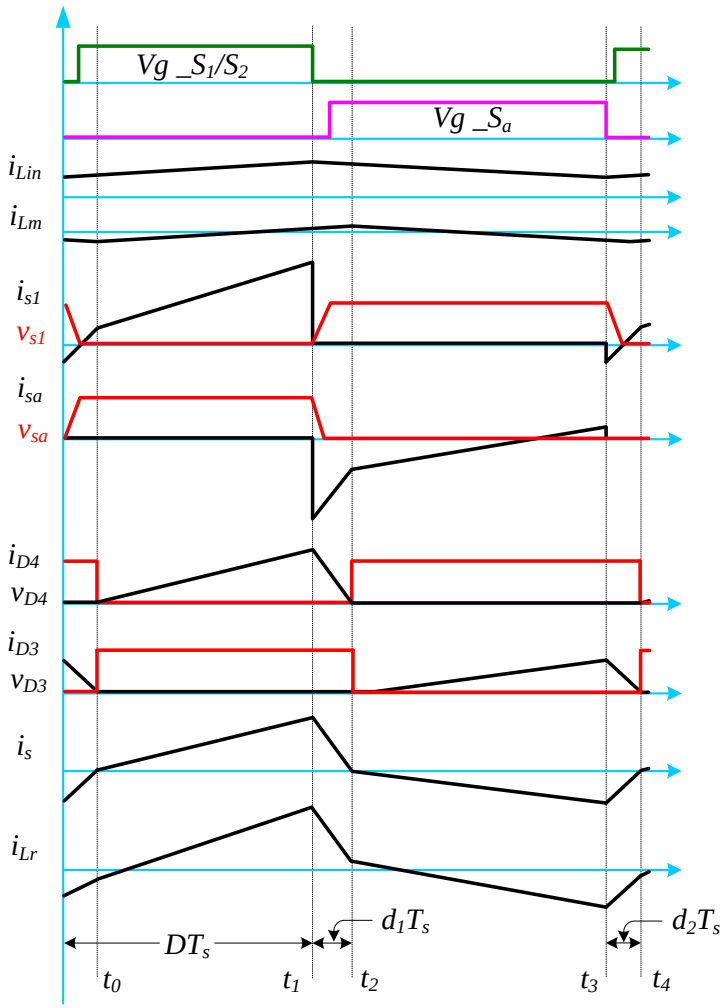
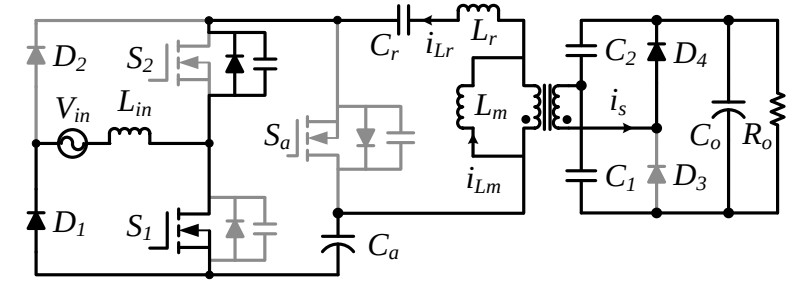
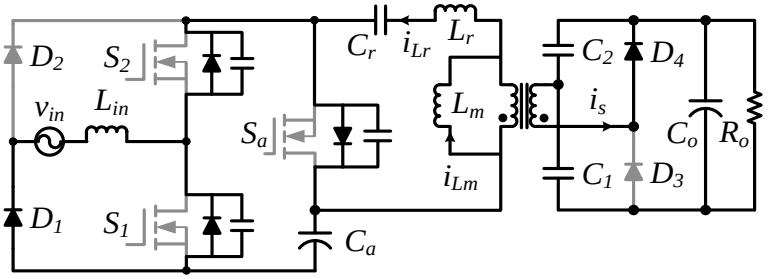


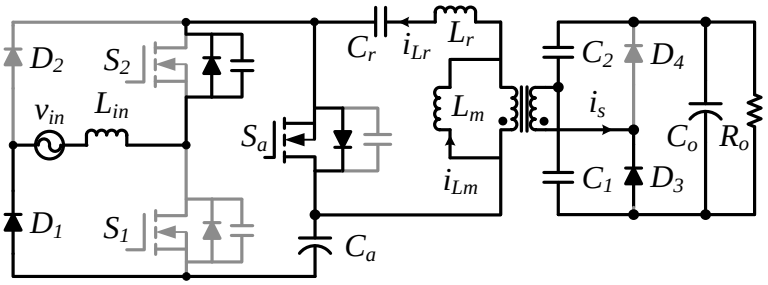
Figure 6.2 Proposed single-stage soft-switching converter waveforms in CCM.



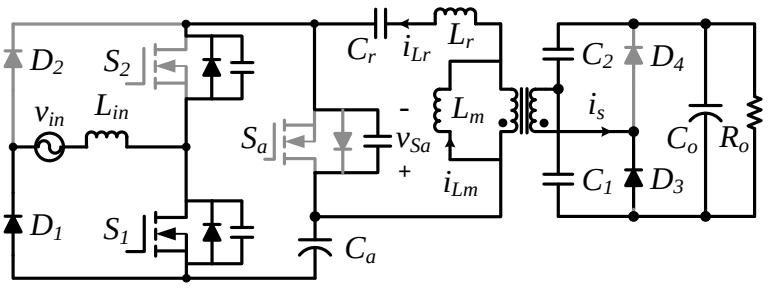
(a)



(b)



(c)



(d)

Figure 6.3 Proposed soft-switching single-stage converter waveforms in CCM.

6.3 Analysis and Design

6.3.1 DC Voltage Conversion Ratio

By applying the volt-second product equations on L_{in}, L_r and L_m during one switching period, the following equations can be easily obtained:

$$V_{Ca} = \frac{1}{1-D}\, V_{in} \tag{6-7}$$

$$V_{Cr} = D\, V_{Ca} \tag{6-8}$$

$$V_{C2} = (1 - D - d_1 + d_2)\, V_o = (1-D)\, V_o - \gamma \tag{6-9}$$

$$V_{C1} = (D + d_1 - d_2)\, V_o = \ D\, V_o + \gamma \tag{6-10}$$

where D is the duty ratio of S_1 and γ is the correction factor given by $\gamma = \ (d_1 - d_2)\, V_o$. From (6-7) to (6-10), the peak currents of the secondary diodes are given by (6-11) and (6-12).

$$I_{D4(peak)} = \frac{N_P}{N_S}\, \frac{D\, T_S}{L_r} \left[(1-D) \left(V_{Ca} - \frac{N_P}{N_S}\, V_o \right) + \ \frac{N_P}{N_S}\, \gamma \right] \tag{6-11}$$

$$I_{D3(peak)} = \frac{N_P}{N_S}\, \frac{(1-D)\, T_S}{L_r} \left[D \left(V_{Ca} - \frac{N_P}{N_S}\, V_o \right) - \frac{N_P}{N_S}\, \gamma \right] \tag{6-12}$$

Now γ can be obtained by applying the ampere-second balance on C_1 and C_2 and is given by (6-13).

$$\gamma = \frac{D\ (1-D)\ (1-2D)}{D^2 + \ (1-D)^2}\, \frac{N_S}{N_P} \left(V_{Ca} - \frac{N_P}{N_S}\, V_o \right) \tag{6-13}$$

By substituting (6-13) into (6-11) and (6-12) the peak current of D_4 and D_3 can be found by (6-14) and (6-15), respectively.

$$I_{D4(peak)} = \frac{N_P}{N_S}\,\frac{D\,T_S}{L_r}\,\frac{(1-D)^2}{D^2 + (1-D)^2}\left(V_{Ca} - \frac{N_P}{N_S}\,V_o\right) \tag{6-14}$$

$$I_{D3(peak)} = \frac{N_P}{N_S}\,\frac{(1-D)\,T_S}{L_r}\,\frac{D^2}{D^2 + (1-D)^2}\left(V_{Ca} - \frac{N_P}{N_S}\,V_o\right) \tag{6-15}$$

The load current can be given by (6-16).

$$I_o = \frac{V_o}{R_o} = \frac{1}{2}\,DT_S I_{D4(peak)}\frac{1}{T_S} = \frac{1}{2}\,(1-D)T_S I_{D3(peak)}\frac{1}{T_S} \tag{6-16}$$

Therefore, from (6-14) and (6-16) the ratio of V_o to V_{Ca} can be given by (6-17).

$$\frac{V_o}{V_{Ca}} = \frac{\frac{N_S}{N_P}\,D^2(1-D)^2}{D^2(1-D)^2 + \left(\frac{N_S}{N_P}\right)^2 \frac{2\,L_r f_s}{R_o}\,[D^2 + (1-D)^2]} \tag{6-17}$$

where f_s is the switching frequency.

Now by substituting (6-7) into (6-18), the input-output voltage conversion ratio can be given by (6-18).

$$\frac{V_o}{V_{in}} = \frac{\frac{N_S}{N_P}\,D^2(1-D)}{D^2(1-D)^2 + \left(\frac{N_S}{N_P}\right)^2 \frac{2\,L_r f_s}{R_o}\,[D^2 + (1-D)^2]} \tag{6-18}$$

6.3.2 ZVS Conditions for the Switches

The ZVS conditions for S_1 and S_2 depend in part on the input current I_{Lin} and the transformer primary current I_{Lr} at the switching instant. The ZVS condition for the auxiliary switch S_a is achieved when the PWM switches are turned off at t_1. The current during the ZVS transition of S_a is the sum of $I_{Lr}(t_1)$ and $I_{Lin}(t_1)$ as given by (6-19).

$$I_{sa(ZVS)} = I_{Lr}(t_1) + I_{Lin}(t_1) \tag{6-19}$$

$I_{Lr}(t_1)$ can be calculated from (6-4), (6-7), (6-8) and (6-13) and is given by (6-20) and $I_{Lin}(t_1)$ can be calculated from (6-3) and is given by (6-21).

$$I_{Lr}(t_1) = \frac{1}{L_r F_S} \frac{D(1-D)^2}{D^2 + (1-D)^2} \left(\frac{1}{1-D} V_{in} - \frac{N_P}{N_S} V_o \right) \tag{6-20}$$

$$I_{Lin}(t_1) = \frac{V_o^2}{\eta V_{in} R_o} + \frac{V_{in}}{2 L_{in} F_S} D \tag{6-21}$$

and η is the efficiency of the proposed converter.

For ZVS of S_a, there must also be sufficient energy stored in the input inductor, L_{in} at t_1 to completely discharge the switch capacitance C_{sa}. Hence, to ensure ZVS turn-on of S_a, (6-22) must be satisfied, where C_{S1} and C_{Sa} are the output capacitances of S_1 and S_a respectively.

$$\frac{1}{2} L_r I_{Sa(ZVS)}^2 \geq \frac{1}{2(1-D)^2} (C_{S1} + C_{Sa}) V_{in}^2 \tag{6-22}$$

To achieve ZVS for S_1, it must be turned on during interval-4 (t_3-t_4). The current required to achieve ZVS for the PWM switches is determined by the difference between i_{Lr} and i_{in} at t_3, as given by (6-23), where $I_{Lr}(t_3)$ can be calculated from (6-6), (6-7), (6-8) and (6-13) and is given by (6-24) and $I_{Lin}(t_3)$ can be calculated from (6-1) and is given by (6-25).

$$I_{s1(ZVS)} = |I_{Lr}(t_3)| - I_{Lin}(t_3) \tag{6-23}$$

$$|I_{Lr}(t_3)| = \frac{1}{L_r F_S} \frac{D^2(1-D)}{D^2 + (1-D)^2} \left(\frac{1}{1-D} V_{in} - \frac{N_P}{N_S} V_o \right) \tag{6-24}$$

$$I_{Lin}(t_3) = \frac{V_o^2}{\eta\, V_{in} R_o} - \frac{V_{in}}{2 L_{in} F_S}\, D \tag{6-25}$$

In addition to the timing requirement, there must also be sufficient energy stored in the resonant inductor L_r to completely discharge C_{s1}. To ensure ZVS turn-on of the PWM switches S_1 and S_2, the inequality in (6-26) must be satisfied.

$$\frac{1}{2}\, L_r I_{S1(ZVS)}^2 \geq \frac{1}{2(1-D)^2}\, (C_{S1} + C_{Sa})\, V_{in}^2 \tag{6-26}$$

6.4 Simulation Results

The proposed converter can be designed using (6-22) and (6-26) to achieve ZVS for all MOSFETs. The example specifications for the proposed converter were as follows: V_{in} = 85 - 265 VAC, V_o = 48 V, P_o = 650 W, f_s = 70 kHz. In order to have ZVS for S_1, S_2 and S_a the inductor value is determined using (6-22) and (6-26) as L_r = 40 µH, considering (C_{s1} + C_{sa}) ≥ 1.5 nF. The value of the capacitors C_r, C_1, and C_2 is chosen based on the design of L_r. The resonant frequency, f_r formed by C_r and C_1 (or C_2) with L_r should be sufficiently low compare with switching frequency, f_s so that there is not excessive resonant current circulating through the PWM switch when it is turned on. A good compromise for design purposes is to select resonant frequency, f_r one-third of the switching frequency, f_s. Thus, considering f_r as 20 kHz the capacitors value can be calculated as C_r= 2 µF, C_1 = C_2 = 6 µF. The value of the clamping capacitor C_a can be calculated from (4-19) as 100 µF.

The simulated input voltage, input current, and output voltage waveforms for the proposed converter are provided in Figure 6.4. Test conditions were as follows: V_{in} = 120 V, V_o = 48 V, P_o = 650 W, f_s = 70 kHz. The input current is in phase with the input voltage, and its shape is close to a sinusoidal waveform, as expected. Moreover, the continuous input current demonstrates that the converter operates in CCM.

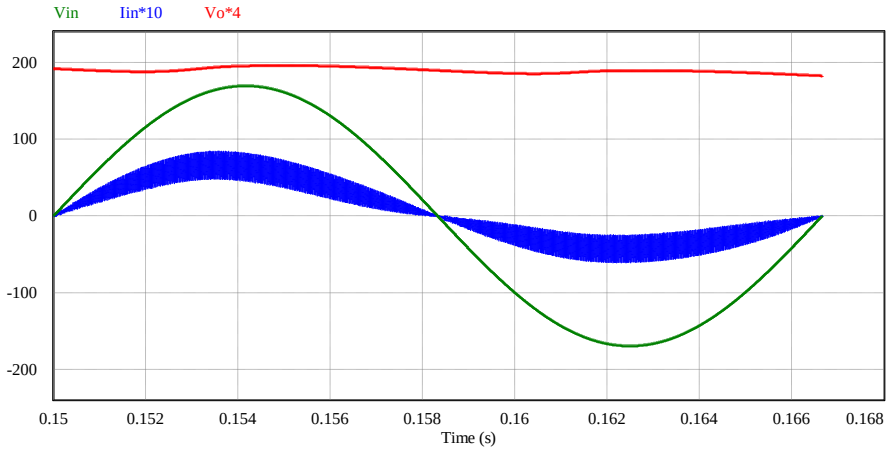


Figure 6.4 Soft-switching single-stage converter experimental waveforms at 2ms/div of input voltage V_{in} (100 V/div), input current I_{in} (10 A/div) and output voltage V_o (25 V/div) at V_{in} = 120 V, V_o = 48 V, P_o = 650 W and f_s = 70 kHz.

The waveform illustrating the ZVS transition during turn-on for S_1 is provided in Figure 6.5 for positive line cycle operation, when S_1 is working as the PWM switch. S_1 is turned on when current is flowing in the negative direction, which indicates that during the turn-on transition, current is flowing through the body diode of S_1 to ensure ZVS. The waveform illustrating the ZVS transition during turn-on for S_2 for negative line cycle operation is provided in Figure 6.6, when S_2 is working as the PWM switch. It can be observed from Figure 6.6 that S_2 also achieves ZVS.

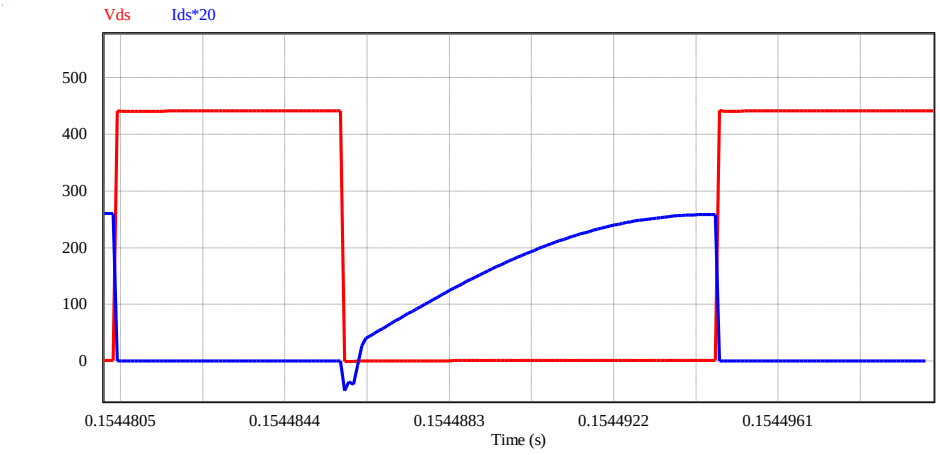


Figure 6.5 Soft-switching single-stage converter simulation waveforms at 2μs/div of voltage across switch S_1, V_{ds} (100 V/div) and current through S_1, I_{ds} (5 A/div) at V_{in} = 120 V, V_o = 48 V, P_o = 650 W and f_s = 70 kHz.

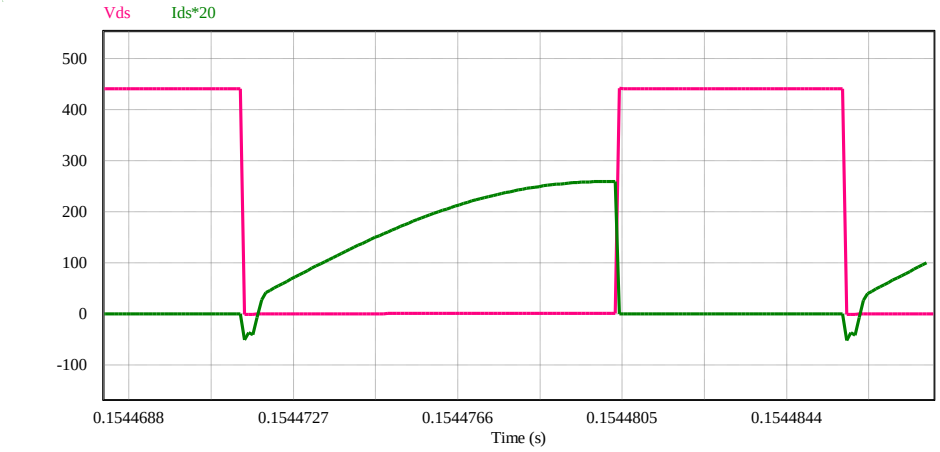


Figure 6.6 Soft-switching single-stage converter simulation waveforms at 2μs/div of voltage across switch S_2, V_{ds} (100 V/div) and current through S_2, I_{ds} (5 A/div) at V_{in} = 120 V, V_o = 48 V, P_o = 650 W and f_s = 70 kHz.

The waveforms of the current through and voltage across diodes D_4 and D_3 are provided in Figure 6.7 and Figure 6.8, respectively. As shown in Figure 6.7 and Figure 6.8, the diodes D_4 and D_3 are both turned

off with ZCS. Unlike most single-stage converters, the voltage across the rectifier diodes D_4 and D_3 is equal to the output voltage (i.e. 48V in this example).

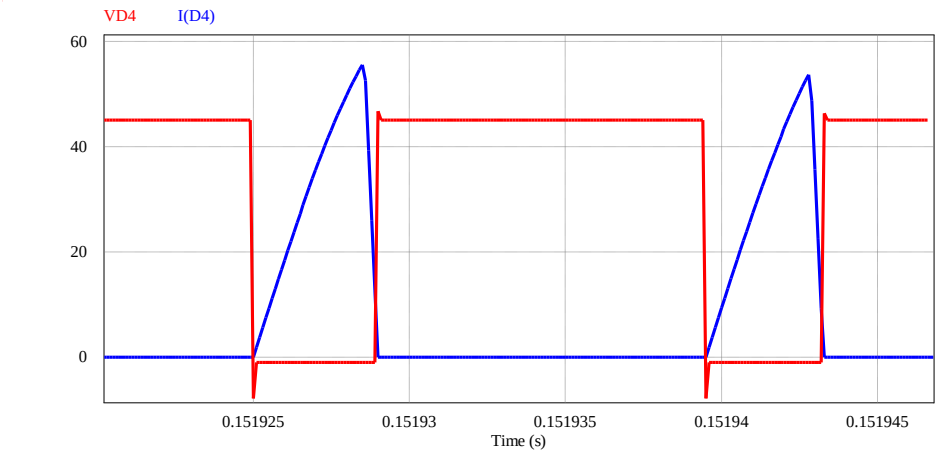


Figure 6.7 Soft-switching single-stage converter simulation waveforms at 5µs/div of voltage across diode D_4, V_{D4} (20 V/div) and current through diode D_4, I_{D4} (20 A/div) at V_{in} = 120 V, V_o = 48 V, P_o = 650 W and f_s = 70 kHz.

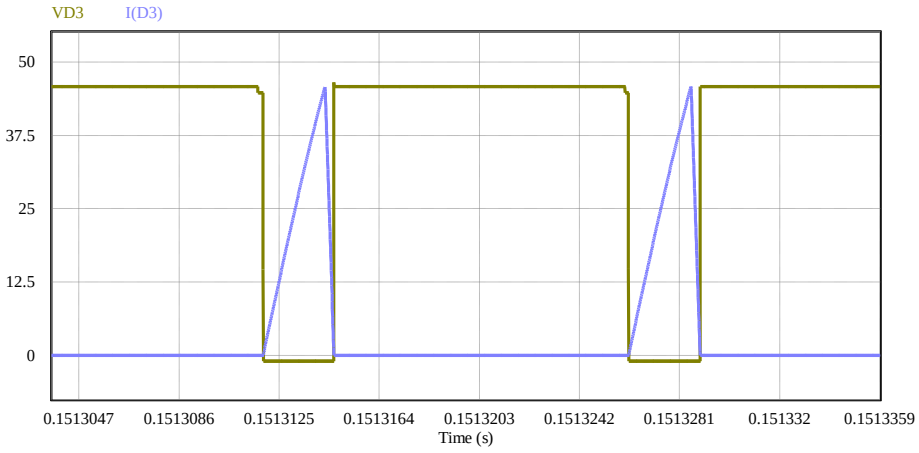


Figure 6.8 Soft-switching single-stage converter simulation waveforms at 5µs/div of voltage across diode D_3, V_{D3} (20 V/div) and current through diode D_3, I_{D3} (20 A/div) at V_{in} = 120 V, V_o = 48 V, P_o = 650 W and f_s = 70 kHz.

6.5 Summary

This chapter presented a soft-switching bridgeless single-stage AC-DC PFC converter topology. A detailed explanation of the proposed converter operating principles and modes of operation was presented. Simulation results demonstrated the steady-state operation of the proposed topology. The proposed converter reduces switching losses by realizing ZVS for the two PFC MOSFETs and one auxiliary MOSFET, and ZCS for the output rectifier diodes. The proposed converter has many advantages for practical implementation. This converter has inherent inrush current-limiting capabilities and standard average current mode control can be easily implemented, and the PWM switches can be driven with the same PWM signal, so extra circuitry is not required to sense both the positive and negative line-cycle operation. The simulation results shows that unlike most single-stage converters, the voltage across the rectifier diodes D_4 and D_3 is equal to the output voltage.

7 Conclusions

The growing demand for electronic devices with high-quality input current necessitates power factor corrected AC-DC converters. Moreover, the demand for ever-increasing power density requires both higher efficiency (to reduce losses and device temperatures) and higher frequency operation (to reduce passive component sizes). In a traditional hard-switching AC-DC converter, the requirements for high efficiency and high frequency are in direct conflict; increasing the switching frequency increases switching losses. Soft-switching converters can greatly reduce switching losses, allowing operation at high frequency while maintaining required efficiency targets. This thesis proposed three new non-isolated topologies and one new isolated single-stage topology for efficient single-phase AC-DC converters as outlined in the following sub-sections.

7.1.1 A Hybrid-Resonant Bridgeless AC-DC Power Factor Correction Converter

The first contribution, presented in Chapter 3, is a novel bridgeless HRPWM AC-DC PFC converter, which has inherent inrush current-limiting capabilities. The converter architecture also enables simple implementation of lightning and surge protection systems. Moreover, the proposed converter also realizes bridgeless converter operation which minimizes the heat management issues of a diode bridge rectifier. A detailed explanation of the proposed converter operating principles and modes of operation was presented. A step-by-step design procedure was described. Experimental results demonstrated the proposed converter's inherent in-rush current limiting, and its ability to withstand sustained over voltage conditions.

7.1.2 A Soft-Switching Bridgeless AC-DC PFC Converter

In Chapter 4, the second contribution presented was a soft-switching bridgeless HRPWM AC-DC PFC converter. Unlike the conventional boost, or bridgeless boost converters, the proposed converter minimizes switching losses by achieving (ZVS) for all switches. Moreover, (ZCS) for the output rectifier diodes reduces the reverse recovery losses. The proposed converter also realizes bridgeless converter operation

which minimizes the heat management issues of a diode bridge rectifier. An experimental prototype was built and presented in order to verify the proof-of-concept. Key experimental waveforms were provided. The converter power factor and efficiency measurements were provided as a function of load power at 100V and 240V input. The power factor exceeds 0.98 from half load to full load. The proposed converter achieved a peak efficiency of 96.95% at 240 V input and 650 W output power. At the maximum loss operating point (full load and 100 V AC input), the proposed converter achieves an efficiency improvement of one percentage point versus the conventional hard-switched PFC converter, and it also operates with lower semiconductor device temperatures.

7.1.3 A High Voltage Gain Soft-Switching Bridgeless AC-DC PFC Converter

The third contribution, presented in Chapter 5, is a high voltage gain soft-switching bridgeless HRPWM AC-DC PFC converter. Unlike the conventional boost, or bridgeless boost converters, the switching commutations of the proposed converter occur with a voltage level equivalent to half of the output voltage, which reduces switching losses and device stress. Moreover, the proposed converter minimizes switching losses by achieving ZVS for all switches and ZCS for the output rectifier diodes, which reduces the reverse recovery losses. The proposed converter also realizes bridgeless converter operation, which minimizes the heat management issues of a diode bridge rectifier. The high voltage gain soft-switching converter operation and analysis were presented. An experimental prototype was built to verify the proof-of-concept, and the key experimental waveforms were provided. The converter power factor and efficiency measurements were provided as a function of load power at 100 V AC input. With a 100 V AC input, the proposed converter achieves a peak efficiency of 94.6% at 350 W output power, and power factor exceeding 0.99 from 25% load to full load. Compared to the conventional hard-switched PFC boost converter at the maximum loss point (full load and 100 V ac input), the proposed converter achieves an efficiency improvement of 1.5 percentage points.

7.1.4 A Soft-Switching Bridgeless Single-stage AC-DC PFC Converter

In Chapter 6, the fourth and final contribution presented was a single-stage isolated soft-switching bridgeless HRPWM AC-DC PFC converter. A detailed explanation of the proposed converter operating principles and modes of operation was presented. Simulation results were presented to demonstrate soft-switching operation of the proposed converter. The converter reduces switching losses by realizing ZVS for the two PFC MOSFETs and one auxiliary MOSFET, and ZCS for the output rectifier diodes. The proposed converter has many advantages for practical implementation. It can be easily implemented with standard average current mode control, and the PWM switches can be driven with the same PWM signal, so extra circuitry is not required to sense both the positive and the negative line-cycle operation.

7.1.5 Comparison and Feature Summary of the Proposed Topologies

Table 7.1 provides a comparison of the proposed topologies in terms of soft-switching capability, relative size and cost (based on component count), and full load and peak efficiency. All data is reported at 400 V DC output. The HRPWM PFC, presented in chapter 3 has the lowest relative cost and achieved the highest peak efficiency, however the results are presented at 70 kHz switching frequency. The topologies presented in chapters 4 and 5 were tested at 150 kHz switching frequency, so the advantage of soft-switching inherent in these topologies is offset by increases in other frequency dependent losses in the converters. It is noted that the full-load efficiency of the topology presented in chapter 4 is higher than that in chapter 3. This is significant since total losses are maximum at full load, so higher efficiency here means less heat dissipation in the converter and potentially improved longevity. The high-gain ZVS PFC results presented in chapter 5 are reported at a significantly lower AC line input voltage of 100 V, as compared to those in chapters 4 and 5 since this topology cannot provide a 400 V output at high line conditions (i.e. 240 V). At low AC input line voltage, conduction losses increase for a given power level, hence the lower reported efficiency results in the 93-95 % range are expected.

Table 7.1 Comparison and feature summary of the proposed topologies

Topology	Features	Relative size and cost	AC Input voltage and switching frequency test conditions	Full Load (650 W) Efficiency	Peak Efficiency
Proposed HRPWM PFC (chapter 3)	Bridgeless, inrush current limit	Low	240 V 70 kHz	96.71 %	97.51 %
Proposed ZVS bridgeless PFC (chapter 4)	Bridgeless, inrush current limit, soft-switching	Medium	240 V 150 kHz	96.95 %	96.95 %
Proposed High-gain ZVS PFC (chapter 5)	Bridgeless, inrush current limit, soft-switching, low voltage rated devices	Medium	100 V 150 kHz	93.52 %	94.62 %
Proposed ZVS bridgeless isolated PFC (chapter 6)	Bridgeless, inrush current limit, soft-switching, isolated	High (includes isolation)	N/A	N/A	N/A

7.2 Future Work

This section provides possible recommendations to expand on the work done in this thesis.

7.2.1 Experimental Validation of Bridgeless Single-stage AC-DC PFC Converter

In chapter 6, a soft-switching bridgeless single-stage AC-DC PFC converter has been proposed. The simulation work shows the feasibility of the converter. However, an experimental work is needed to further validate the converter operation.

7.2.2 Interleaved Soft-switching AC-DC PFC Converter

Most of the soft-switching PFC boost topologies discussed in this dissertation are best suited for medium power applications (i.e. 500 W to 1000 W). For high power applications, more research activities are needed to achieve optimized soft-switching operation in interleaved PFC converters.

7.2.3 High Frequency Converter Operation

The very high frequency operation of power converter can further increase the power density of the converter system, but conventional silicon superjunction MOSFETs are not suitable for operation above a few 100 kHz. The newly developed Gallium Nitride (GaN) devices open up a wide research area for very high frequency operation of power converters at the MHz switching frequencies.

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Appendix

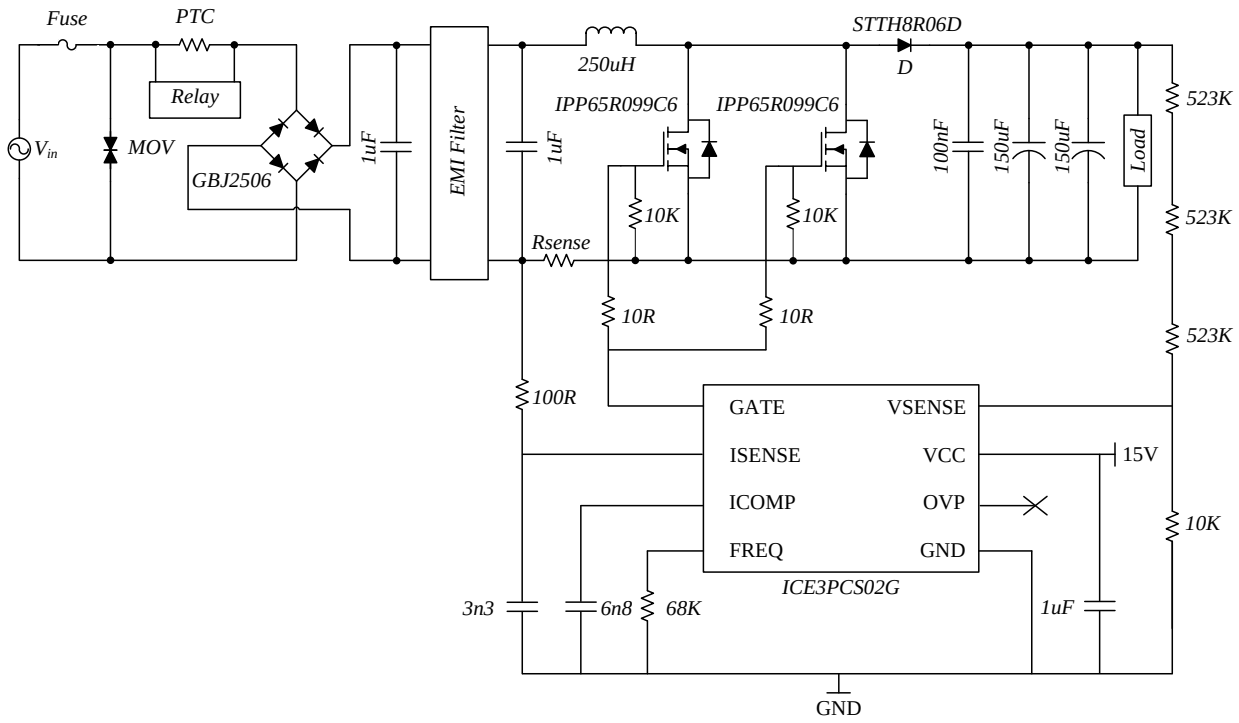

Figure A- 1 Circuit schematic of the conventional boost converter.

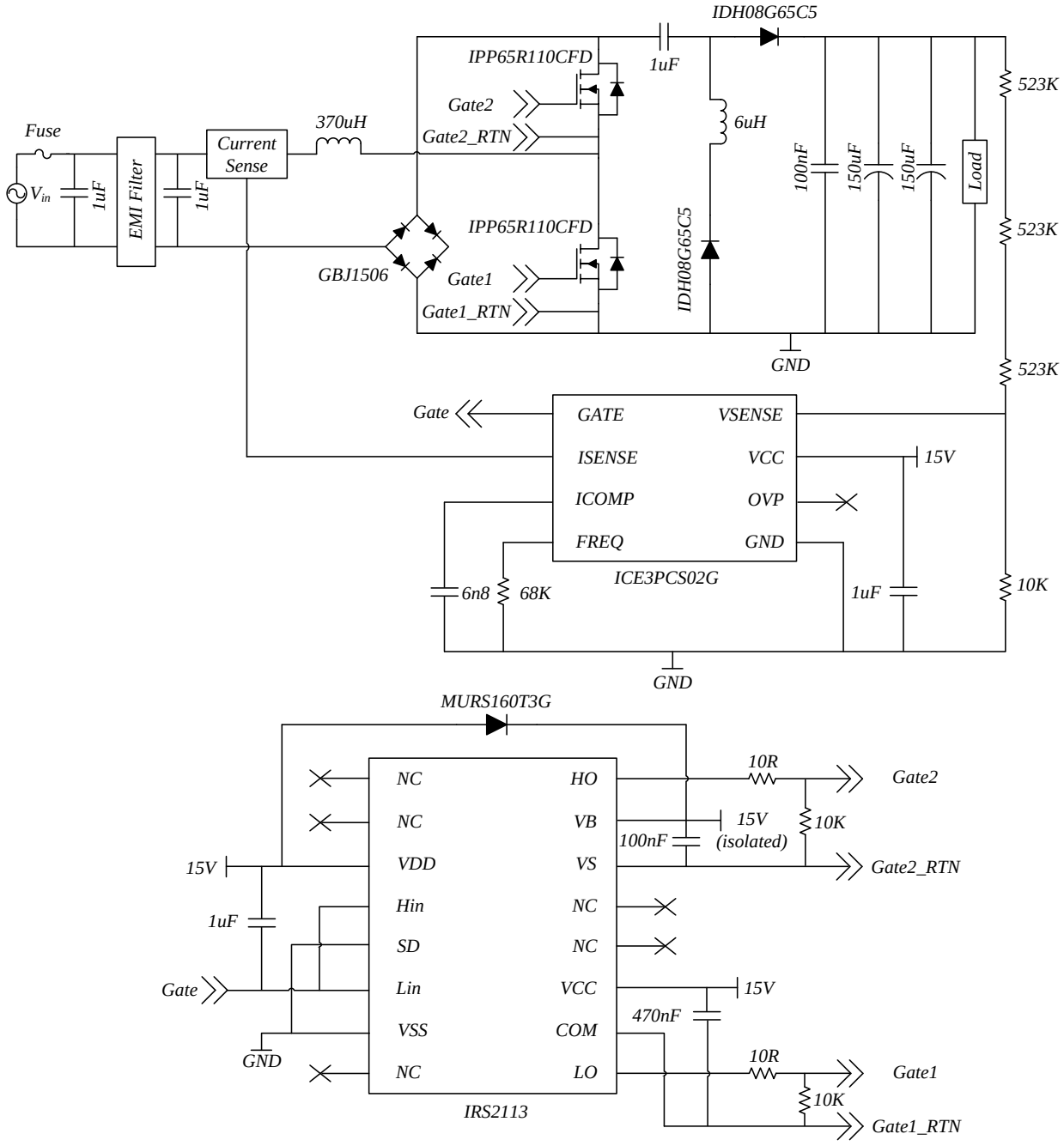

Figure A- 2 Circuit schematic of the converter proposed in Chapter 3.

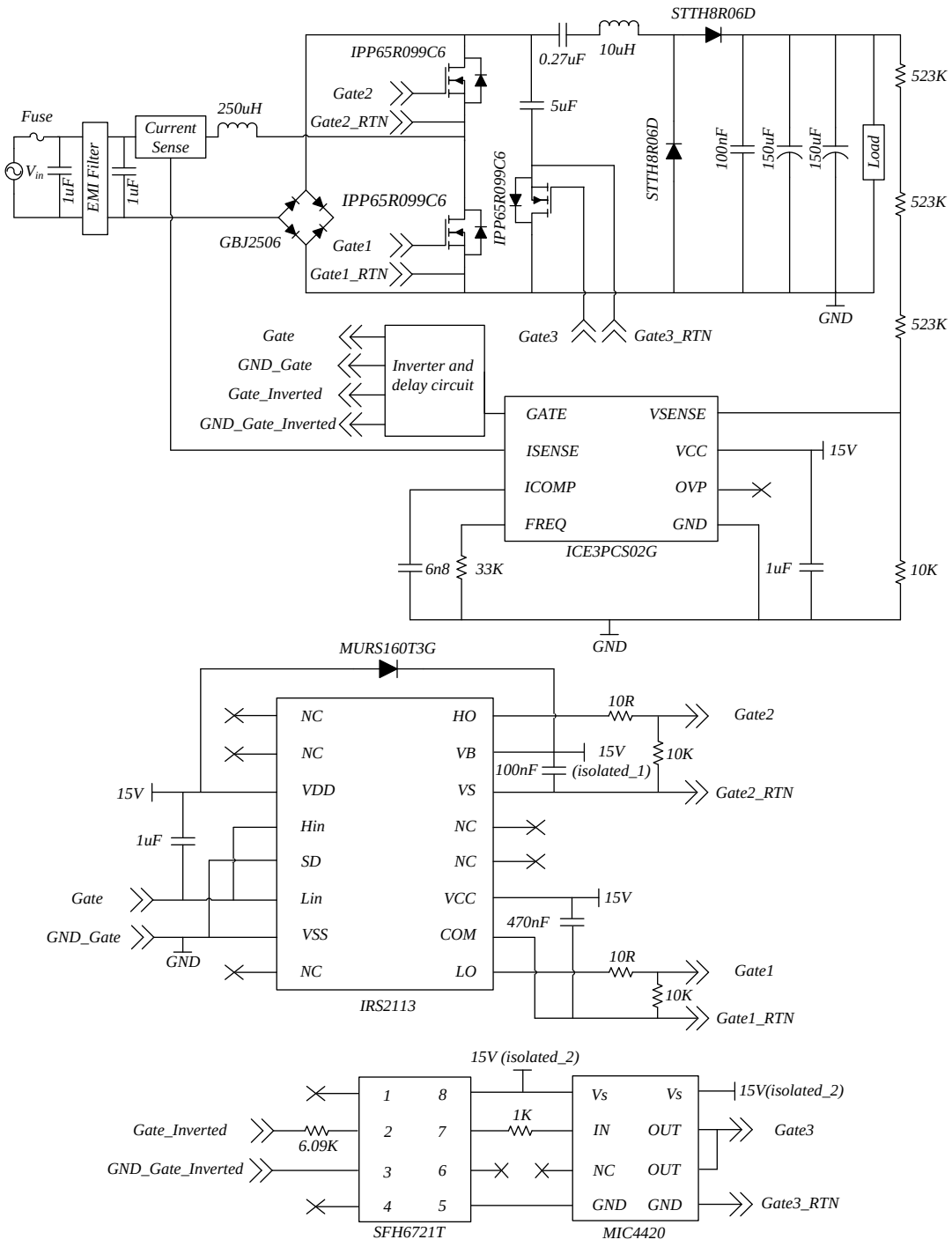

Figure A- 3 Circuit schematic of the converter proposed in Chapter 4.

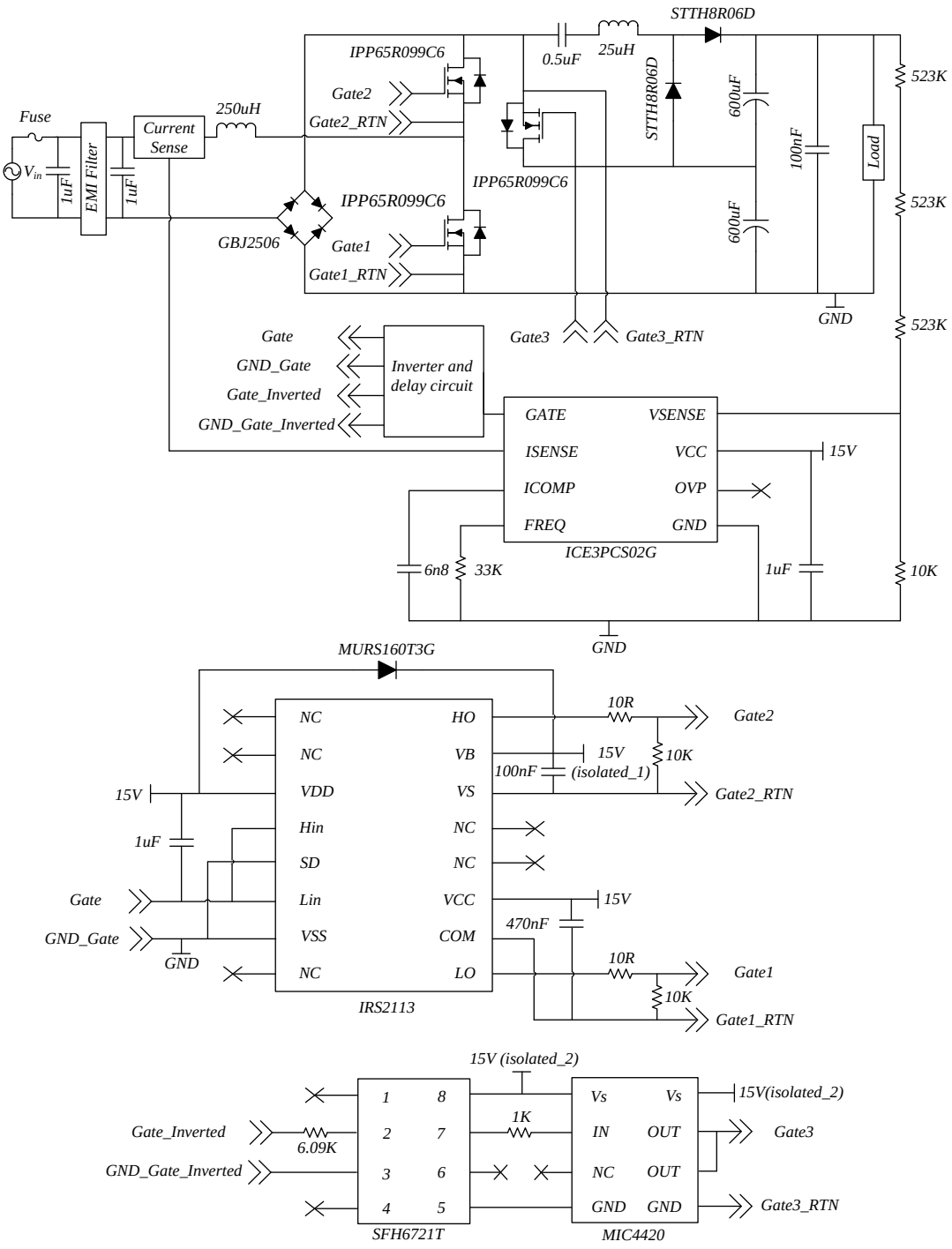

Figure A- 4 Circuit schematic of the converter proposed in Chapter 5.