AN ABSTRACT OF A DISSERTATION

ANALYTICAL AND COMPACT MODELING OF HIGHLY ASYMMETRICAL INDEPENDENT DOUBLE-GATED TRANSISTORS

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Doctor of Philosophy in Engineering

Recent research has focused on dynamic and flexible threshold multi-gate transistors that enable ultra-low-power (ULP) and reconfigurable CMOS integrated circuits. Independently-Double-Gated (IDG) fully-depleted channel MOSFETs have the advantage of being able to use the voltage applied at the second gate to shift the threshold voltage of the transistor to zero or less in the "ON" state and to VDD or more in the "OFF" state, allowing optimization of the standby power vs. speed tradeoff. This work developed an analytical model for highly asymmetrical independently double-gated MOSFET that allows the threshold voltage to be reconfigured by the second gate with a very high dynamic threshold voltage control factor. This work also develops a SPICE-compatible compact model for highly asymmetrical independent double-gate nanoscale MOSFETs that can be exported to the IC design community worldwide.

This work used a novel surface potential-based approach, as opposed to a threshold voltage-based approach and studied the effects of device design parameters like silicon channel thickness, gate oxide thickness, and gate work functions. Performance metrics such as threshold voltage and dynamic threshold control factor are analyzed for two different independently-double-gated device structures, namely, FinFET and FlexFET. Six different combinations of top and bottom gate work functions were modeled, (including varying the silicon and oxide thicknesses) and divided based on their work function asymmetry. A primary finding of this work was that both an asymmetrical device structure (IDG-FlexFET) and asymmetrical top and bottom gate work functions were needed to meet the targets for ultra low power applications.

A Verilog-A compact model has been developed for highly asymmetrical IDG-FlexFET. The results generated by the compact model closely match the analytical model for full-asymmetry and half-asymmetry cases and to a good extent in case of the symmetrical one. The result of the compact model with all physical effects turned on compared with actual experimental data and the results are comparable to a reasonable degree.

ANALYTICAL AND COMPACT MODELING OF HIGHLY ASYMMETRICAL INDEPENDENT DOUBLE-GATED TRANSISTORS

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ANALYTICAL AND COMPACT MODELING OF HIGHLY ASYMMETRICAL INDEPENDENT DOUBLE-GATED TRANSISTORS

By

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DEDICATION

This dissertation is dedicated to all those who believe that…

"It matters if you just don't give up"

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TABLE OF CONTENTS

Page

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

Page

Page

Page

LIST OF TABLES

Page

Page

Page

Page

CHAPTER 1

INTRODUCTION

The semiconductor industry's workhorse technology is silicon Complementary Metal Oxide Semiconductor (CMOS), and the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is the building block of CMOS [1-7]. Figure 1.1 shows a basic block diagram of a MOSFET.The figure shows a typical example of a bulk single-gated MOSFET, with a lightly doped p-type substrate and heavily doped n-type source and drain regions. A metallic gate of length *L* and width *W* covers the region between source and drain and is separated from the substrate by an oxide layer. The voltage bias between the source and the drain is referred to as *Vds* and that between the gate and the source is *Vgs*.

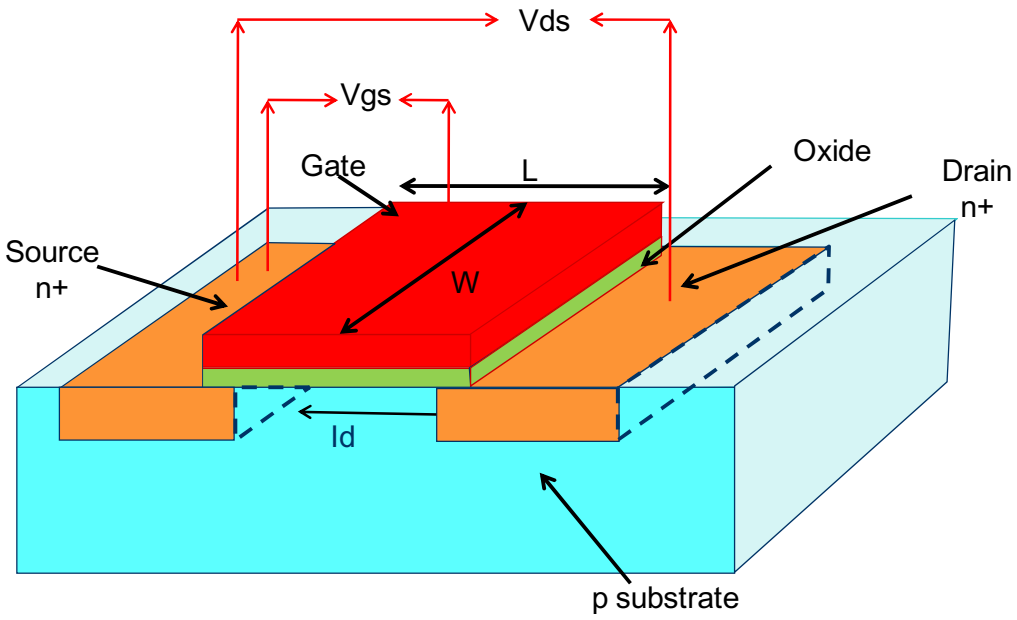

Figure 1.1. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

Electrons flow from the source to the drain and current, *Id,* in the opposite direction. As a positive voltage is applied to the gate, electrons are attracted to the oxide-semiconductor interface. By increasing the positive bias on the gate, it is possible to increase the electron population in the substrate region between the source and the drain. At a particular bias voltage known as the *threshold voltage*, *Vt*, the number of electrons (minority carriers) in the substrate, near the oxide-semiconductor interface becomes high enough to invert the region between the source and the drain into an n-type region, thus forming an *"n-channel"* of electrons between source and drain. Now if a positive bias is applied at the drain end, these channel electrons will flow from source to drain and current will in turn flow from drain to source. This is the working principle of a MOSFET.

Depending upon the biases applied at the gate-source, *Vgs,* and the drain-source, *Vds,* the MOSFET operates in three different modes.

(1) Triode/Linear Mode: - If *Vgs* > *Vt* and *Vds* < Vgs-*Vt*, then the n-channel is continuous all the way from source to drain. The source and drain are connected by a sheet (or a resistor) of a given resistance. The drain current increases if the voltage between source and drain increases. The channel resistance depends on how much charge is injected at the source-end, which in turn is controlled by *Vgs*.

(2) Saturation: - If *Vgs* > *Vt* and *Vds* > Vgs-*Vt*, then n-channel is present (or induced) at the source-end, but the channel is depleted at the drain-end. That is, the n-channel is *"pinched off"* at the drain-end. Once the drain-end of

channel is pinched off, the current no longer increases with the voltage drop between source and drain, but saturates. As a result, increasing *Vds* after this point results in very little change in the drain current.

(3) Sub-Threshold: - *Vgs* < *Vt.* The *n-channel* is not present, so no current should flow. However, some highly energetic electrons surmount the source barrier and reach the drain end, thereby resulting in a small drain leakage current. This current is known as sub-threshold current. Though each transistor gives rise to only femto-to-micro amps of leakage current, the cumulative leakage current from an integrated circuit with tens of millions of transistors is a significant amount.

Figure 1.2 shows the typical I-V characteristics and the three operating regions of a MOSFET.

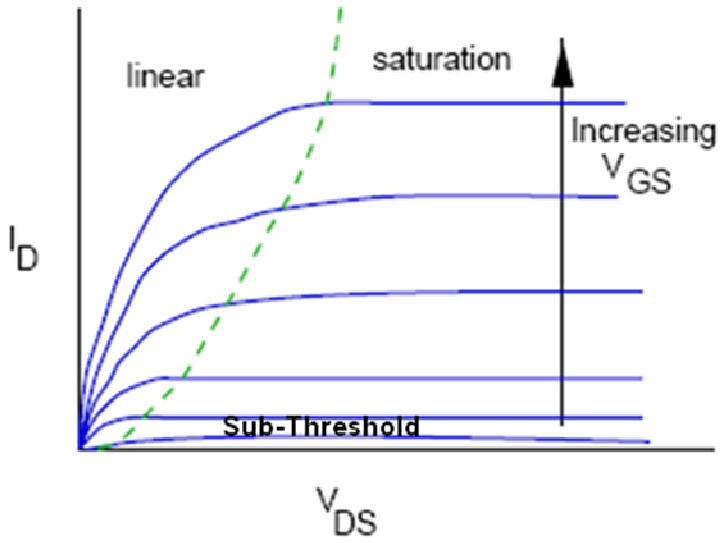

Figure 1.2.I-V characteristics of a MOSFET

1.1 MOSFET Scaling and Moore's Law

For the last forty years the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are integration density, cost, speed, power, compactness, and functionality. The industry's ability to exponentially reduce the minimum feature sizes used to fabricate these integrated circuits has resulted in dramatic improvements in these trends. These trends follow Moore's law, which describes the evolution of transistor density in integrated circuits [8-14]. It states that the number of transistors per chip will quadruple every three years or double every 18 months.

The changes and improvements in semiconductor device technology, commonly referred to as *"scaling,"* are the result of large R and D investments. In order to both drive and accurately predict the future of the semiconductor industry trends, the International Technology Roadmap for Semiconductors (ITRS) is published [15-19]. The main objective of the ITRS is to provide reports annually that serve as benchmarks for the semiconductor industry. They help in describing the type of technology, design tools, and equipment that must be developed in order to keep pace with the progress of semiconductor devices as predicted by Moore's law. Figure 1.3 shows the evolution of the number of transistors per chip as predicted for DRAMs and high performance microprocessors by the ITRS 2005. The linear dimensions of a typical transistor have been reduced significantly in order to keep pace with the predictions of Moore's Law. In the early 1980's the sub-micron barrier was overcome and by 2010 transistors with a gate length of 20nm will be produced on a regular basis.

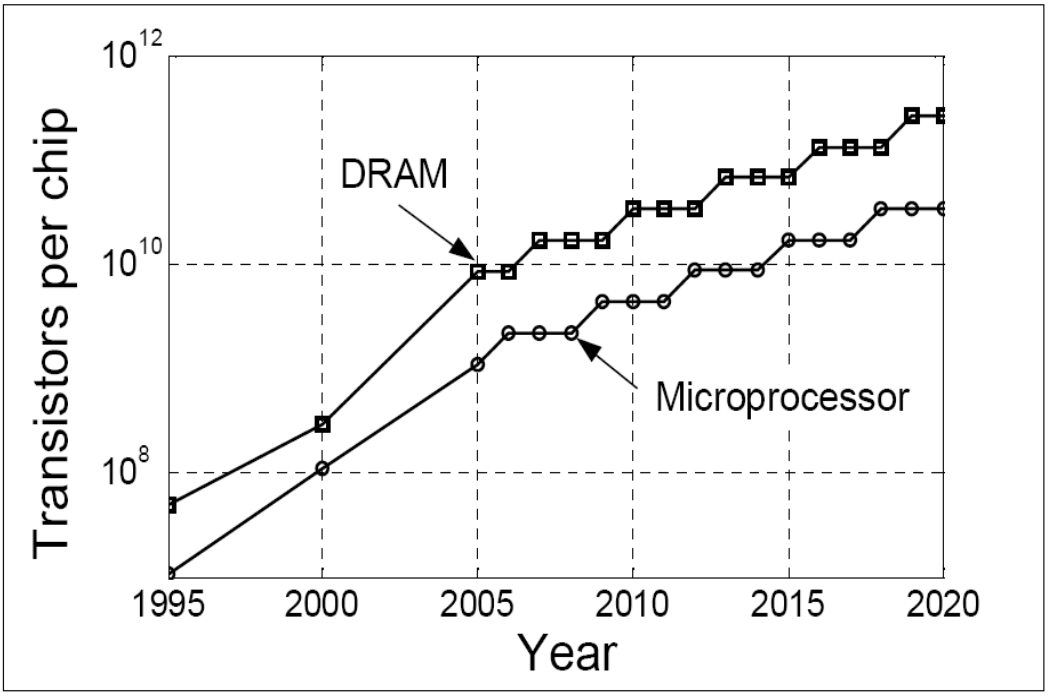

Figure 1.3. Evolution of the number of transistors per chip predicted by ITRS 2005 for DRAMs and high performance microprocessors [2]

However by the end of 1990's, it was evident that significant improvement in performance can only be obtained by switching to a new type of silicon transistor technology which uses a Silicon-On-Insulator (SOI) substrate [20-22].

1.2. Transition from Bulk MOSFETs to SOI MOSFETs

The ever-increasing need for enhancement in Complementary Metal-Oxide-Semiconductor (CMOS) performance has given rise to accelerated research in non-classical transistors. Traditionally research in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) focused on Bulk transistors. With scaling of device dimensions, newer technologies like Silicon-On-Insulator (SOI) MOSFETs came into existence [23-29].

The typical structure of an SOI MOSFET is shown in Figure 1.4. SOI devices are built in an ultra-thin crystalline Si layer which lies on top of an insulating layer called the Bottom Oxide (BOX). There are two primary classifications of single-gated SOI MOSFET transistors: Partially depleted (PD) and fully depleted (FD). If the depletion region below the channel does not extend completely through the entire silicon film thickness, then it is called a partially depleted device and if the depletion region does extend completely through the silicon film thickness, then it is called a fully depleted device. There was a time when novel transistor structures proposed by SOI researchers were often considered exotic and impractical, but the recent success of SOI in the field of microprocessor manufacturing has finally given this technology the credibility and acceptance it deserves. The adoption of SOI substrates for manufacturing (by IBM and AMD) of mainstream semiconductor products such as game-box microprocessors has given SOI research an unprecedented impetus.

There are several advantages of SOI technology over bulk MOSFET. In processing bulk MOSFETs, N-wells and P-wells have to be inserted separately in the silicon substrate to fabricate PMOS and NMOS transistors, respectively.

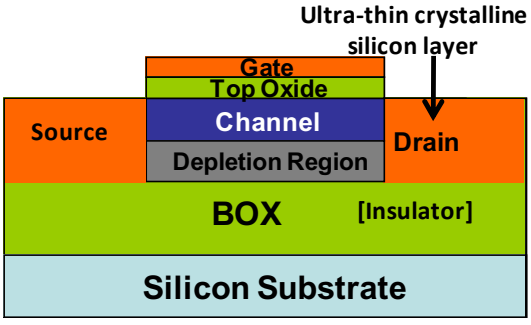

Figure 1.4. SOI MOSFET

In the case of SOI processing, there is no need for N-wells and P-wells, because the device bodies are BOX isolated/insulated from each other. This gives rise to simpler IC processing techniques and also a higher density per chip as more transistors now fit in the same area. Also, in case of bulk CMOS devices, the source-substrate and drain-substrate junction capacitance is high. In SOI, the capacitances between the substrate and source/drain are reduced due to the thick BOX isolation between them. This factor helps SOI device, to switch faster. Another advantage of SOI over bulk MOSFETs is if ionizing radiation passes through a CMOS device, they create electron hole pairs, which are collected by the reverse bias p-n junctions as leakage current. Due to this, the voltage at that particular node is disturbed. However, since the volume of depleted silicon is very small, SOI devices do not face this Single Event Upset (SEU) problem.

In a continuous effort to increase current drive and have a better control of short channel effects, SOI MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure, such as FinFET and FlexFET.

1.3. Need for this Study – Motivation

The increasing need for ultra-low-power (ULP), reconfigurable CMOS integrated circuits has given rise to recent research in dynamic and flexible threshold multi-gate transistors. Many future ULP digital and mixed-signal applications will demand that VDD be less than or equal to the threshold voltage Vt (less than 0.5V). However, with standard fixed-Vt CMOS technology, this would result in insufficient gate voltage drive

and low current and performance. The threshold voltage of the transistor can be made dynamically adjustable or programmable by using a second independent gate to shift the VT to zero or less in the "on" state and to VDD or more in the "off" state. Independently-double-gated fully-depleted channel MOSFETs has the advantage of being able to use the voltage applied at one gate to control the threshold voltage of the other gate. This feature enables the threshold voltage to be reconfigured dynamically as required, avoiding the traditional standby power vs. speed tradeoff.

Most modern day portable electronic applications like cell-phones, laptops, iPods, etc., have the most advanced ULP ICs in them to carry out a number of functions. The performance of any IC is determined by the transistors that build it. Figure 1.5 shows the standby power and speed as a function of bottom/second gate voltage.

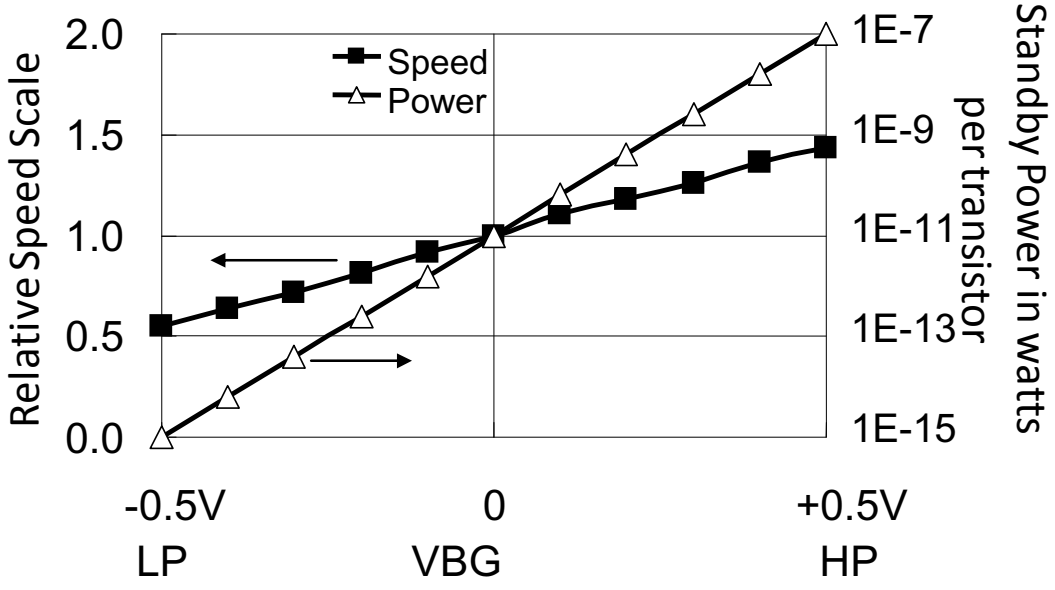

Figure 1.5. Power Vs Speed Trade Off of dynamic/flexible threshold IDG MOSFET transistors

As can be seen from this figure, as the speed or performance of the device increases, the standby power consumed by the devices increases exponentially and the battery life of these devices decreases. So it is desirable to operate the same transistor at the low power (left of figure) point at times and at the high performance (right hand of the figure) point at other times.

Figure 1.6 shows the DC *Id-Vg* characteristic variation of drain current with respect to gate voltage for different devices. It can be seen that for device 1 the threshold voltage is very low, which means that the transistor would be turned on with the application of a very small bias voltage. On the other hand its sub-threshold current or the *Ioff* current is very high which would mean that this device would consume a great amount of power, even in the stand-by mode. Now, in case of device 3, it can be seen that the threshold voltage is very high, indicating that a high input bias is required to turn the device on. However, this device has a relatively low *Ioff* value, which results in lower stand-by power consumption.

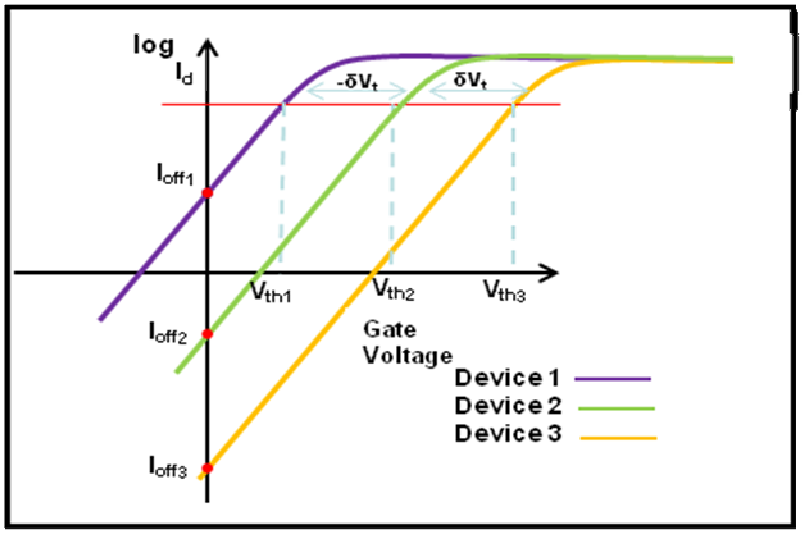

Figure 1.6. Sub-Threshold Leakage Current and Threshold Voltage relationship

For a given device with fixed dimensions, such as silicon film thickness, top and bottom oxide thicknesses, the threshold voltage is fixed and cannot be changed after fabrication. However, with the advent of multi-gated more precisely independently-double-gated transistors, the threshold voltage of a device is affected not only by device dimensions but also by the voltage bias applied at the bottom or the second gate.

In a number of applications, the transistor is designed to operate at a particular threshold voltage. Over a period, due to aging effects or radiation exposure, the threshold voltage will shift to a different value from what the application was designed to work at. This is an undesirable effect and may result in unnecessary power loss and circuit failure. In case of single gate transistors, the circuit would be un-repairable and non-configurable. But in the case of independently double-gated transistors, the threshold voltage can be dynamically tuned to compensate for aging shifts, retaining full circuit functionality by merely adjusting the bottom or the second gate bias.

Independent double gated transistors have a variety of applications starting from aerospace, accelerators, ring oscillators, x-ray machines and other applications that might be subjected to change in threshold voltage variation due to either aging or radiation effects. In a circuit with thousands of transistors it is possible to tie the bottom gates together and place a the circuit in a control loop where any shift in threshold voltage is monitored and the bottom gate voltage of these transistors is adjusted to bring it back to the operating point.

1.4. Problem Statement

This work aims to analytically model a highly asymmetrical independently double gated MOSFET that allows the threshold voltage to be reconfigured by the second gate with a very high dynamic threshold voltage control factor. This work uses a novel surface potential-based approach, and studies the effects of device design parameters like silicon channel thickness, gate oxide thickness, and gate work functions on performance metrics such as threshold voltage and dynamic threshold control factor for two different independently-double-gated device structures, namely FinFET and FlexFET. The goal of this work is to develop both an analytical and a compact model for highly asymmetrical independent double gate nanoscale MOSFETs that can be exported to the IC design community worldwide.

1.5. Organization of the Dissertation

This dissertation is divided into six chapters. The second chapter deals with the different kinds of SOI devices in literature and the different approaches used to Study them so far. The third chapter presents the analytical model used to analyze the performance characteristics of two different kinds of independent double-gated transistors, FinFET and FlexFET. The fourth chapter presents the results and discussions generated by the analytical model, establishing the superiority of highly asymmetrical FlexFET over FinFET in terms of dynamic threshold voltage control factor. The fifth chapter presents the Verilog-A compact model developed for FlexFET. This chapter presents the results of this compact model in comparison with that of the analytical model

as well as some experimental data. The sixth chapter presents a summary and a set of conclusions based on this work.

CHAPTER 2

LITERATURE REVIEW

Manufacturing of mainstream semiconductor products such as microprocessors with silicon-on-insulator substrates has given SOI research a great boost. However, owing to the reduction in device dimensions and scaling trends, the classical SOI planar structure has had to be replaced by non-classical structures like double-gated, triple-gated, multi-gated transistors, in order to keep pace with Moore's Law. Also, with scaling device structures and geometries, the analytical device physics models used to determine the device performance characteristics have undergone changes.

This chapter focuses on the evolution of SOI technology from a single-gated transistor to an independent double-gated transistor and the different variations proposed under each category. It also discusses the analytical approaches that are used in Studying transistor characteristics.

2.1. Evolution of SOI Technology

Figure 2.1 shows the *"family tree"* of SOI MOSFETs showing the transition from partially depleted single-gated SOI to fully depleted multi-gated SOI. Starting from 1982 all the way to 2006, different variations have been proposed to the device structure and geometry of a MOSFET. Each of them has its own set of unique advantages and limitations.

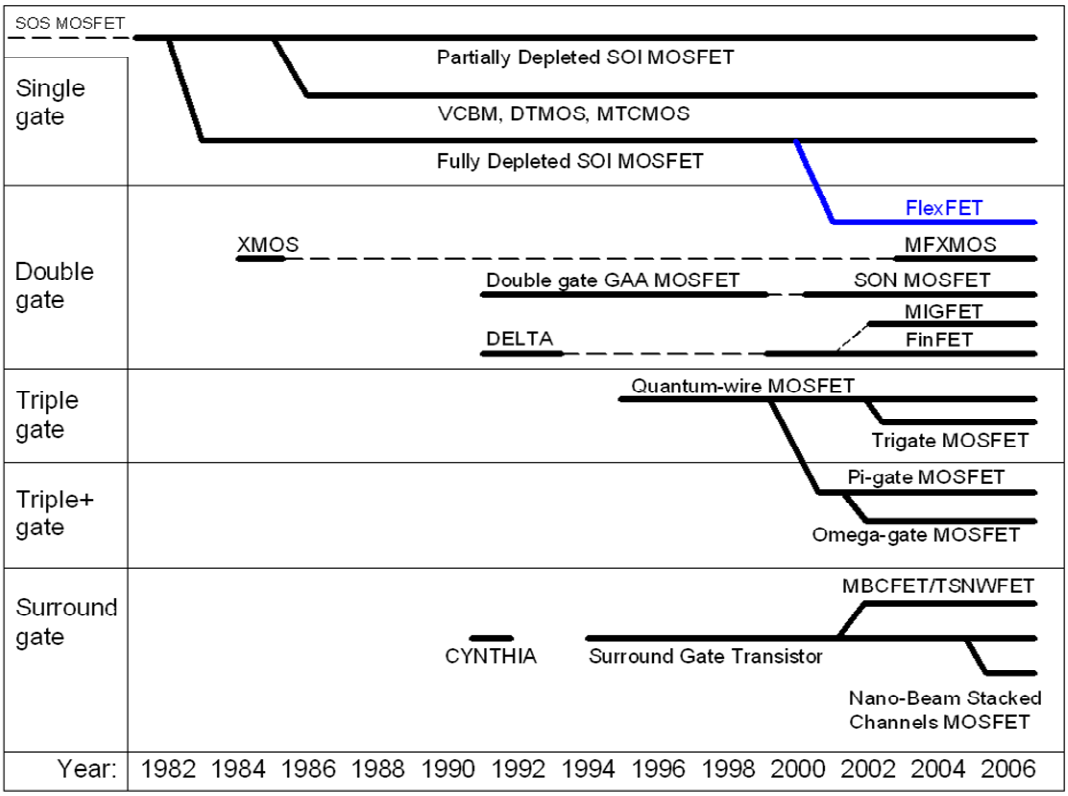

Figure 2.1 Family tree of SOI MOSFETs [2]

2.1.1. Single-Gated Transistors

As the gate bias *Vgs* is increased, the region near the oxide-semiconductor interface starts depleting of majority carriers. Depending upon the thickness of the depletion layer and the silicon body thickness, the device can be classified as either Partially Depleted or Fully Depleted.

Figure 2.2 shows a block diagram of a partially depleted single-gated SOI transistor (PDSOI). It can be seen here that the thickness of the depletion region below the channel is not as much as the thickness of the silicon film [30-38].

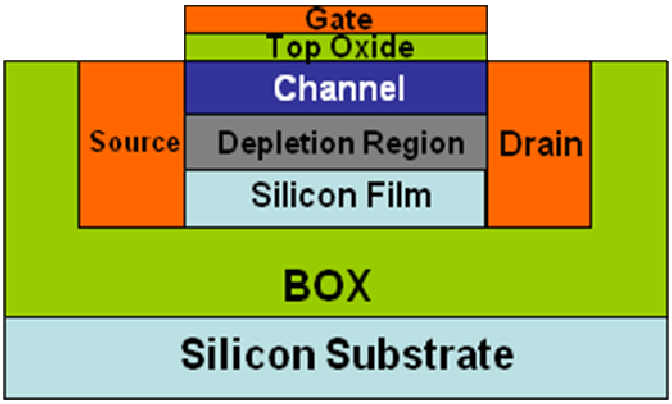

Figure 2.2. Partially Depleted Single-Gated Transistor

PDSOI MOSFETs are used for applications such as radiation-hardened and high-temperature electronics. PDSOI is the mainstream technology for producing high performance microprocessors. The low-voltage DTMOS version of PDSOI can be achieved by creating a contact between the gate electrode and the floating body of the device. This improves the sub-threshold slope, transconductance, and current drive. However, this results in limiting the DTMOS device operation to sub-1V supply voltages.

Parke et al., proposed slight modification in the structure of a single-gated PDSOI transistor by tying body and gate together. This gives rise to a dynamic threshold voltage MOSFET (DTMOS). This device has an ideal 60 mV/dec sub-threshold swing. As the gate voltage is raised, the threshold voltage of a DTMOS device decreases, which results in much higher current drive than a regular MOSFET. Among the various advantages that this structure has to offer, it is ideal for low voltage operation, it solves the floating body problems of PDSOI MOSFET. It also enhances carrier mobility. However, the device is prone to have nonuniform threshold voltage along its width, increased junction capacitance and slow switching speed, which are not desirable.

A fully depleted SOI (FDSOI) device is one whose depletion region extends completely through the silicon channel thickness [39]. Figure 2.3 shows the structure of a FDSOI device.

FDSOI devices have better electrostatic coupling between the gate and the channel as most field lines propagate through the buried oxide before reaching the channel region. This higher electrostatic coupling results in better linearity, sub-threshold slope, body coefficient, and current drive. FDSOI technology is employed in a wide range of applications from low-voltage, low-power to RF integrated circuits.

2.1.2. Double-Gated Transistors

A more powerful device configuration, as compared with the single-gated transistor, is the double-gated transistor. Here a fully depleted SOI device is placed in between two gate electrodes, which are connected together. The electric field lines from the source to the drain terminate on the bottom gate electrode and therefore cannot reach the channel.

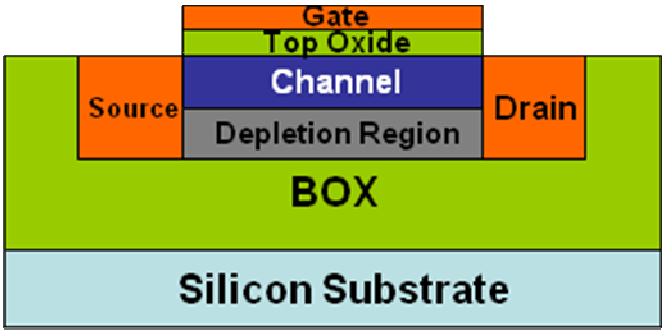

Figure 2.3. Fully Depleted Single-Gated Transistor

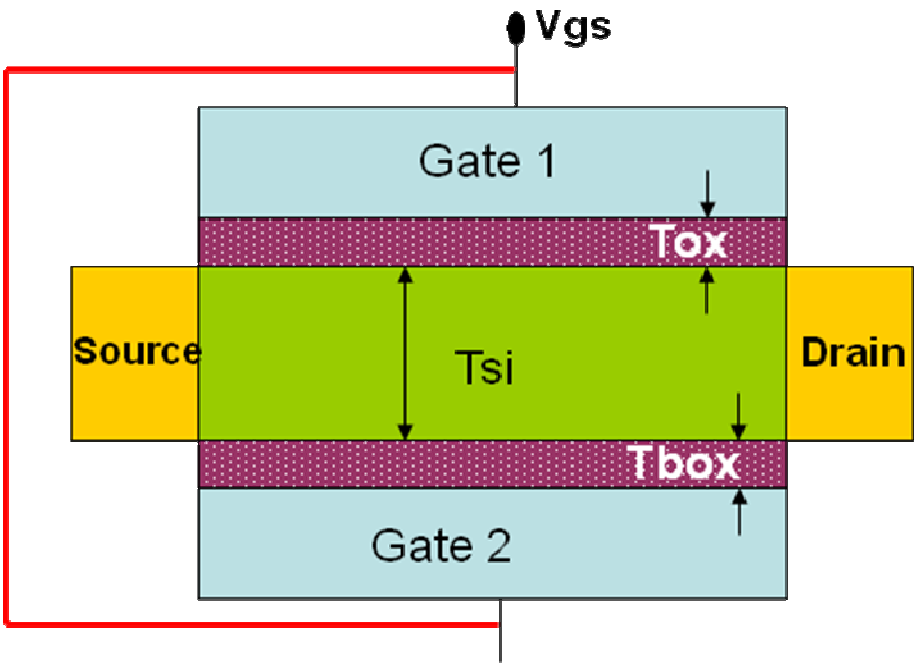

Figure 2.4. Double-Gated Transistor

As a result of this the two gates have better control of the channel. Here only the field lines that can penetrate through the silicon film can reach the channel region and degrade the gate control over the channel. Figure 2.4 shows the structure of a double-gated MOSFET.

DG MOSFETs have advantages such as 60 mV/dec sub-threshold slopes, volume inversion, and the flexibility of setting the threshold voltage by changing the gate work function. Avoiding dopant and many other fluctuation effects, double-gated devices have become more and more studied. It is to be noted that in a double-gated device the top and bottom gate voltages are tied together, i.e., they are dependent.

T. Sekigawa and Y. Hayashi published the first article on double gated transistors in 1984 [40]. The device was called XMOS, because its cross section looks like the

Greek letter *Xi.* This configuration helped gain a better control of the channel depletion region than in the case of a regular SOI MOSFET. Also the influence of the drain electric field on the channel is reduced, which reduces short channel effects [41].

In 1992 Laux and Fischetti published a paper that explores the ultimate scaling of the silicon MOSFET [42]. They present a more complete modeling of the MOSFET using Monte Carlo Simulations. This article claims that ultimate silicon device is a double-gated SOI MOSFET with a gate length of 30 nm, an oxide thickness of 3nm, and a silicon film thickness range of 5nm – 20 nm. This type of device does not show any kind of short channel effect for gate lengths of 70 nm and more. It also provides transconductance values of up to 2300 mS/mm.

The "fully DEpleted Lean-channel TrAnsistor (DELTA)" was the first double gated transistor to be fabricated [43]. This device was made in a tall and narrow silicon island called a "finger" or "fin." FinFET is a device similar in structure to that of DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin [44-47]. The purpose of the hard mask is to prevent the formation of parasitic inversion channels at the top corners of the device. Figure 2.5 and Figure 2.6 show the structures of DELTA and FinFET, respectively.

There are several other vertical-channel implementations of SOI MOSFETs. Gate-All-Around (GAA), which is planar MOSFET with a gate electrode wrapped around the channel region, the Silicon-On-Nothing (SON) MOSFET, the Multi-Fin XMOS (MFXMOS), the triangular wire SOI MOSFET are a few such examples [48-53].

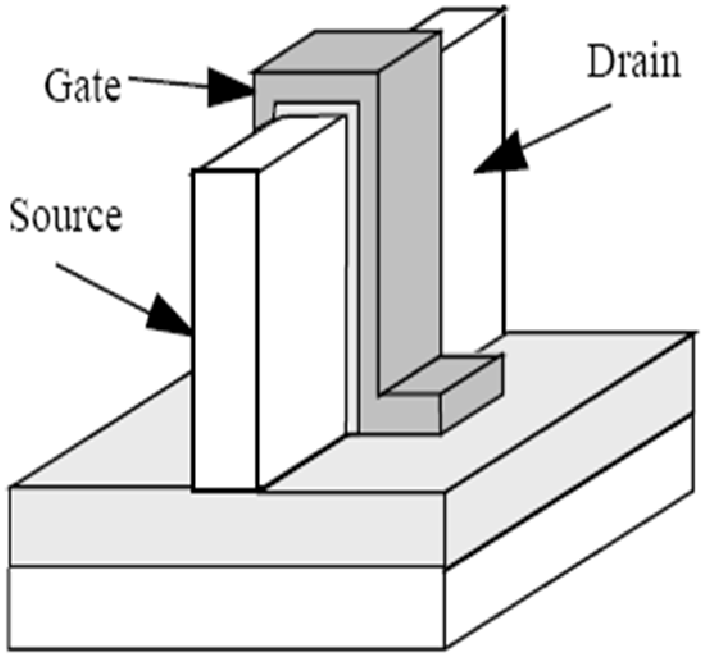

Figure 2.5. DELTA MOSFET [2]

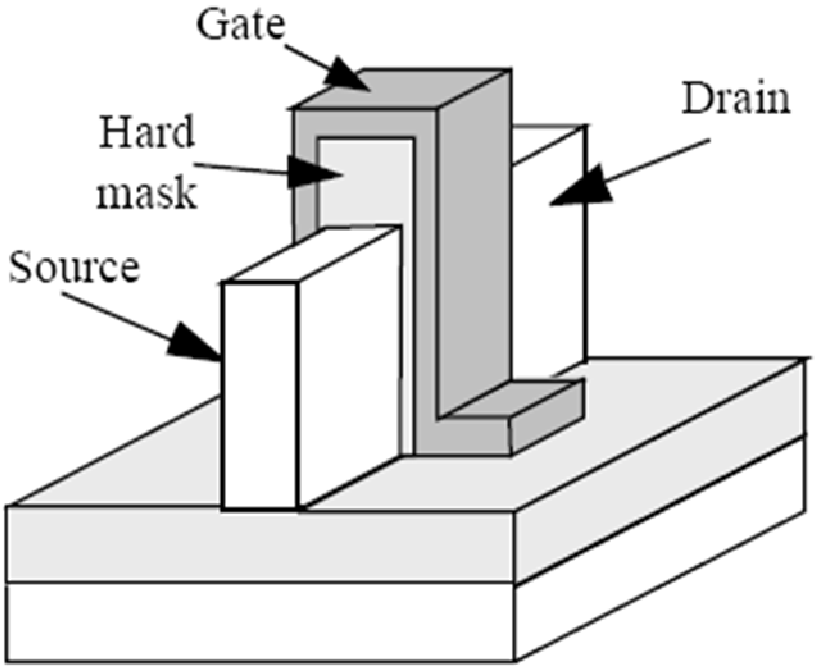

Figure 2.6. FinFET [2]

2.1.3. Triple-Gate SOI MOSFETs

The triple-gate MOSFET has a gate on three sides of a thin film, narrow silicon island [54]. The electrostatic integrity, which is a measure of the electric field lines from the drain influencing the channel region causing short channel effects, can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide. This can be improved further by extending the gate even underneath the channel region as in the case of omega gate implementations [55, 56]. The quantum wire SOI MOSFET is another implementation under this category [57].

2.1.4. Surrounding Gate or Quadruple Gate SOI MOSFETs

The Gate-All-Around or Surrounding Gate structure offers the best electrostatic integrity factor and hence the best possible control of the channel region by the gate. Devices like CYNTHIA [58] and the cylindrical/pillar surrounding-gate MOSFET are fabricated by wrapping a gate electrode around vertical silicon cylindrical/pillar [59]. The current drive per unit area can be increased in these cases by simply stacking multiple surrounding-gate channels one on top of another, while sharing a common gate, source, and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET), the Twin-Silicon-Nanowire MOSFET (TSNWFET), or the Nano-beam Stacked Channels (GAA) MOSFET [60-63] .

The schematic cross section of different types of device implementations can be seen in Figure 2.7.

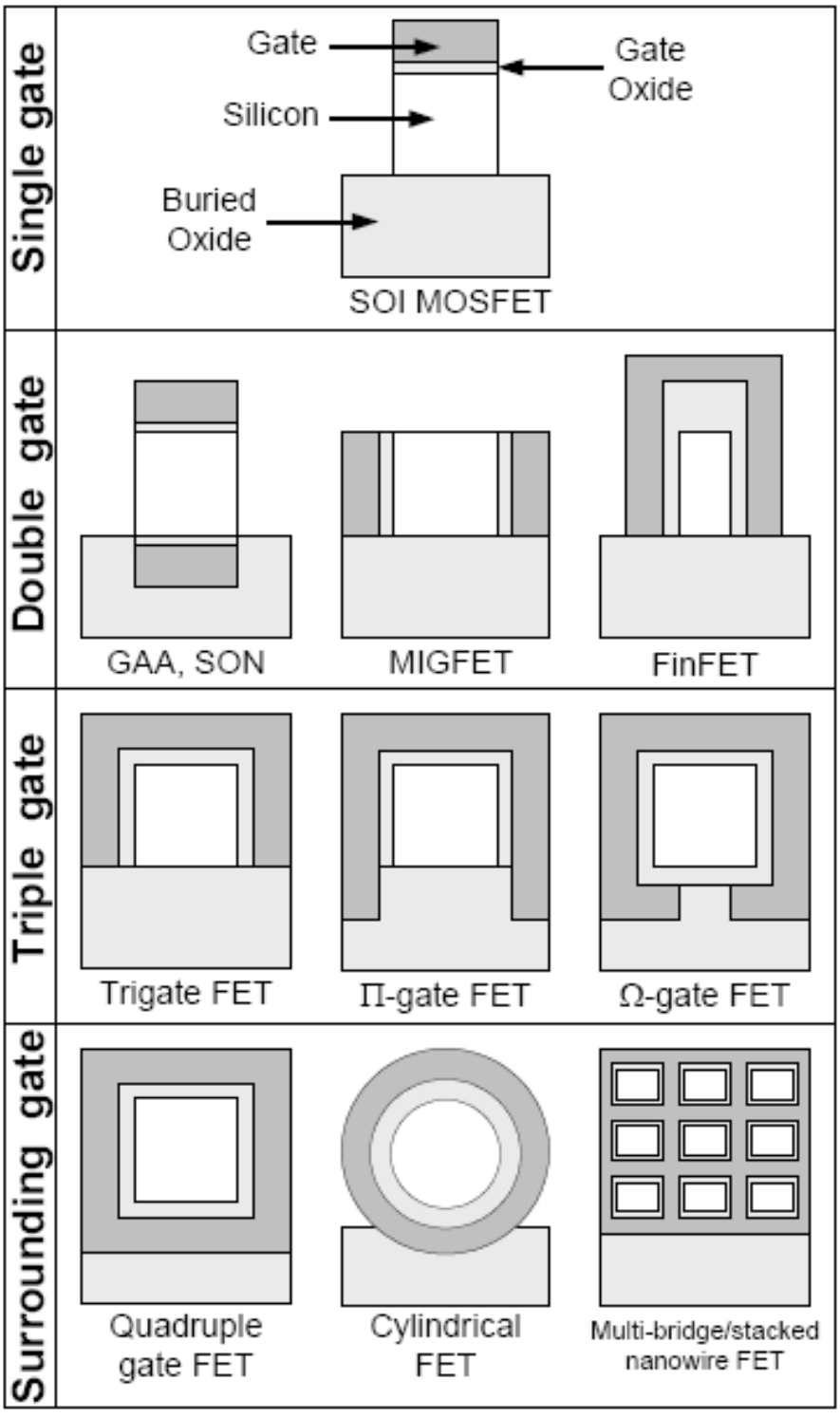

Figure 2.7. Schematic Cross-Section of Different Gate Structures

2.2. Independent Double-Gated (IDG) Transistors

IDG transistors are a variation of the Double-Gated Transistor category. Here the two gates are not tied together as in the case of double-gated transistors, but are separate electrodes, independent of each other. It means that a different input voltage or signal bias can be applied at each gate. Independent double-gated transistors have all the advantages of a double-gated transistor, like 60mV/dec sub-threshold slopes, high volume inversions, and flexibility of setting the threshold voltage by changing the gate work functions. In addition to these, IDG transistors have the ability to dynamically change the threshold voltage of the device by changing the back/bottom/second gate voltage.

2.2.1. IDG FinFET

One of the most popular modes of double-gated and hence independent double-gated transistor model is the IDG FinFET. Figure 2.8 shows a schematic of the device [64]. It is a vertical structure with a MOSFET front gate and MOSFET back gate. A front gate bias of *Vg1* and a gate bias of *Vg2* can be applied to the device to achieve dynamic reconfiguration of the threshold voltage. Asymmetry can be introduced to this device by differences in the gate biases, the front and back gate work functions, and the front and back gate oxide thickness.

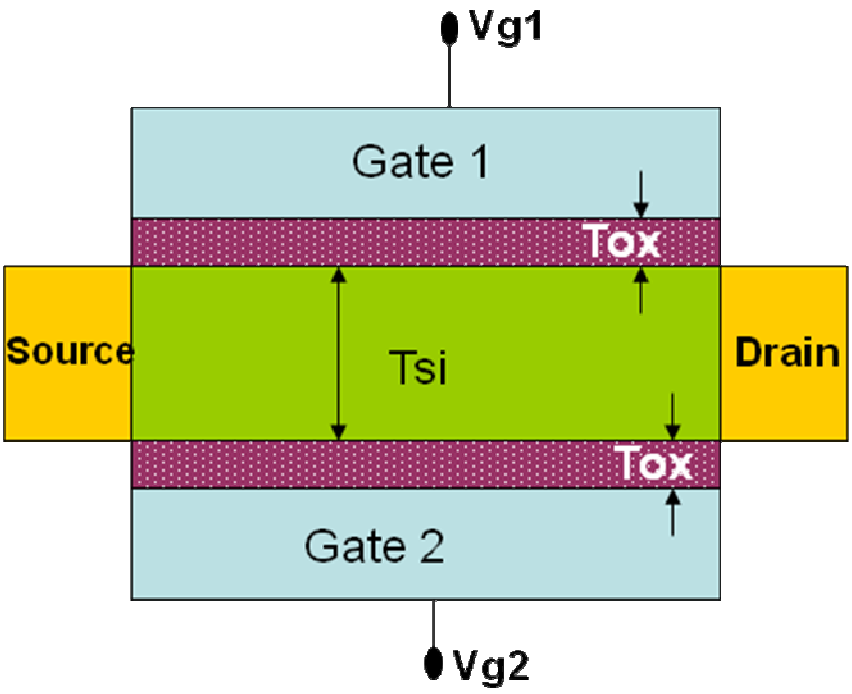

Figure 2.8. IDG FinFET

The Device Research group at University of California, Berkeley, is the pioneer in developing FinFETs. All around the world, many device laboratories are analyzing the characteristics of FinFETs and proposing improvements to the structure. Most research focuses on fully symmetric versions of FinFET where, the front and back gate oxides are equal. This is the simplest way of fabricating an inherently symmetrical structure [65].

There is an urgent need to explore the virtues offered by asymmetrical versions of this device. However, fabricating a vertical FinFET device with asymmetric oxide thicknesses or asymmetric gate work functions is a rather difficult task. This can be overcome by using a planar IDG device, FlexFET.

2.2.2. IDG FlexFET

IDG FlexFET is a device with inherent asymmetry in its structure. It has a MOSFET top gate and a JFET bottom gate. Figure 2.9. shows the structure of an IDG FlexFET.

Since the bottom gate is a JFET, there is no bottom oxide layer in this device unlike FinFET and the other double gated devices in literature. The absence of the bottom oxide layer helps in promoting better back gate channel control, which helps in controlling the threshold voltage of the device more closely. FlexFET is a planar device which makes it fabrication a lot simpler, especially including the structural asymmetry.

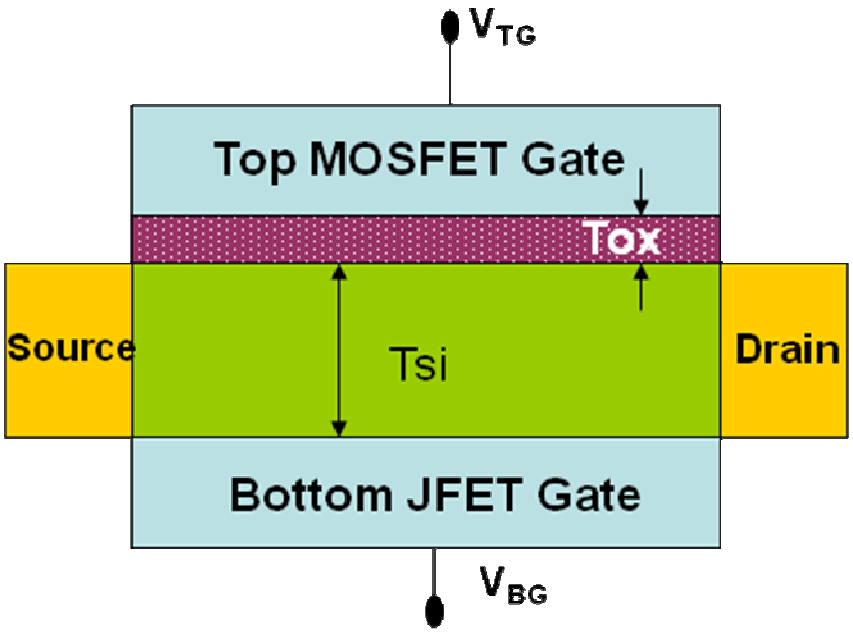

Figure 2.9. IDG FlexFET

This device was first published and patented by the research team at American Semiconductor in 2003. Since it is a relatively new device, not a lot of research has been carried out on it so far [66-71].

2.3. Analytical Models for Transistors

There are two different approaches to model a transistor behavior; Threshold Voltage-based approach and the Surface Potential-based approach. These two approaches will be discussed briefly in this section.

2.3.1. Threshold Voltage-Based Approach

Traditionally, most both SOI and bulk device researchers used threshold voltage-based approaches to model transistor behavior [72]. In this approach, all electrical variables like currents at the source and drain, capacitances, and charges are derived from the threshold voltage of the device. The calculation of the threshold voltage is therefore the core of this approach.

A top gate threshold voltage equation was developed as a function of bottom gate, with all the other physical parameters fixed. In the partially depleted case (PDSOI), since there is no charge coupling between the top and the bottom gates, the top gate threshold voltage is given by Bulk MOSFET equation, which is

$$V_T = V_{TFB} + 2\phi_B - \frac{Q_B}{C_{TOX}} \tag{2.1}$$

where V_{TFB} is the top gate flat band voltage, $2\phi_B$ is the surface potential, and $\frac{Q_B}{C_{TOX}}$ is the voltage drop across the top oxide [73]. When the silicon film is fully depleted (FDSOI) by the top gate threshold voltage, and when the bottom surface is depleted, the threshold voltage equation is given as

$$V_T = V_{TFB} - 2\phi_B\left[\frac{C_D \| C_{BOX}}{C_{TOX}} + 1\right] - \frac{Q_B}{2C_{TOX}} \tag{2.2}$$

The equation for a double-gated SOI MOSFET is given as

$$V_T = \frac{V_{FBTG}}{1+f} + \frac{\left(1 + \frac{C_{SI}}{C_{Tox}} - f\frac{C_{SI}}{C_{BOX}}\right)}{1+f}\phi_{ST} - \frac{f}{1+f}[V_{BG} - V_{FBBG}] \tag{2.3}$$

And that of independently double-gated SOI MOSFET

$$V_{TG} = V_{FBTG} + (1+f)\phi_{ST} - f[V_{BG} - V_{FBBG}] \tag{2.4}$$

2.3.2. Surface Potential-Based Approach

In this approach, all electrical variables like currents at the source and drain, capacitances, and charges are derived from the surface potential at the drain and the source ends of the device. The calculation of the surface potential forms the basis of this approach. A surface potential-based compact model has been developed by the Device Research Group [74]. The surface potential at the front and back oxide/silicon interfaces of the device are given as

$$\psi_{sf} = Vtg - Vfbtg - 12\frac{Tox}{Tsi}\beta\phi_t \coth(\alpha - \beta) \tag{2.5}$$

$$\psi_{sb} = Vbg - Vfbbg + 12\frac{Tbox}{Tsi}\beta\phi_t \coth(\alpha + \beta) \tag{2.6}$$

where the front and back surface potentials of the device are represented as Ψ_{sf} and Ψ_{sb}. The unknowns in the equation, α and β, are determined by solving the boundary conditions which are obtained by using the definition of the potential profile explained in detail in the chapter to follow. The drain current can be expressed in these terms.

$$I_d = 2 * \mu * \frac{W}{L} * (f(\psi_s - \psi_d) \tag{2.7}$$

where μ is the carrier mobility, W and L are the channel width and length, and

$$f(\psi_s) = \frac{Q_{inv}^2}{2 * C_{ox}} + 2\phi_t Q_{inv} - \phi_t(\frac{5\varepsilon_{si}\phi_t}{Tsi} + Qbulk) * (\ln(\frac{5\varepsilon_{si}\phi_t}{Tsi} + Qbulk + Q_{inv}) \tag{2.8}$$

$f(\psi_s)$ is a term computed at the source end and $f(\psi_d)$ is a term computed at the drain end. These models are used to analyze the electrical characteristics of a device.

2.3.3. Main Features Threshold Voltage and Surface Potential-Based Approaches

This work uses the relatively new surface potential approach to model a highly asymmetrical independent double gate device namely FlexFET. The asymmetry is not limited to just the work function differences, and gate oxide thicknesses but extends to the device structure since FlexFET has a MOSFET top gate and a Junction Field Effect Transistor (JFET) bottom gate. As this device does not have a bottom oxide layer, it has a better charge coupling between the bottom gate and the channel, which in turn leads to a better channel control. This device is capable of reconfiguring the threshold voltage better than the symmetrical structured FinFET.

Table 2.1. Main Features of Surface Potential and Threshold Based Approaches

Feature	Threshold Voltage Model	Surface Potential Model
Complexity	This is a simple model. It comprises simple linear algebraic equations which can be solved by any analytical tool.	This model comprises transcendental non-linear equations, which need to be solved using iterative methods.
Operating Regions	This model has separate equations for threshold voltage in accumulated, inverted and depleted modes.	This model uses a continuous potential profile to develop the surface potentials. As a result these equations would holds good in all three modes.
Accuracy	This model is based on assumptions to lead to its simplicity. This costs some part of accuracy.	More accurate (if the roots are found accurately)
Highlighting Nuances	Cannot highlight the slight variations in parameters being tested.	The complexity of this model is due to fact that accurately projects and highlights the subtle variations in parameters. This is because of the exponential terms that magnify any changes.

CHAPTER 3

SURFACE POTENTIAL-BASED ANALYTICAL MODEL

With scaling of device dimensions, continuing with classical planar CMOS devices is not possible. Multi-Gated transistors like FinFET and FlexFET are the best possible options to move into the sub 25 nm gate length regimes. Gate leakage and sub-threshold leakage are two of the most difficult issues with the short channel devices. The strong coupling between source and drain can be reduced to a great extent by using multiple gates that generate a strong electrostatic control over the channel. This helps with better control of the threshold voltage and helps reduce the leakage current and sub-threshold current. A significant amount of research is being carried out to facilitate the manufacturing of multi-gated transistors. There is a need for analytical and compact models that will help circuit designers to evaluate the performance of these devices before finalizing the parameters for fabrication.

This chapter presents a new analytical model that defines the electrical characteristics of highly asymmetrical independent double-gated devices like FlexFET. It also presents the I-V model used to evaluate the performance of the FinFET and FlexFET.

3.1. Surface Potential Model for Independent Double-Gated Transistors

The analytical models used to analyze the behavior of conventional transistors have been based on threshold voltage. In the recent times, compact models, PSP [75],

HiSIM [76], and BSIM [77], developed for the non-classical modes of transistors are beginning to use surface potential-based analytical models. It is a relatively new approach with an inherent advantage of yielding continuous and smooth expressions for terminal currents and charges over different operating regions like sub-threshold, linear, and saturation. Though far more complex than regular threshold voltage models, they accurately project and highlight the subtle variations in metrics due to change in device parameters.

The analytical models for analyzing IDG-FinFET and IDG-FlexFET are based on the surface potential model developed by the device research group at University of California, Berkeley. These models assume a lightly doped silicon body. The threshold voltage of the independent double-gated devices using these models can be tuned by adjusting the back gate voltage.

3.1.1. Analytical Model for IDG-FinFET

This section describes the equations used to model the behavior of IDG-FinFET [2]. Figure 3.1 shows the schematic of a typical IDG-FinFET. The figure shows FinFET with a MOSFET front gate with work function Φ_{m1} and a back/second MOSFET gate with work function Φ_{m2}. The top oxide thickness is *Tox* and that of the bottom oxide is *Tbox*. The Silicon channel thickness is *Tsi*. $V_{ch}(y)$ is the channel potential and it is equal to zero at the source end and equal to *Vds* at the drain end. The front and back surface potentials of the device are represented as Ψ_{s1} and Ψ_{s2}. By solving the 1-D Poisson's

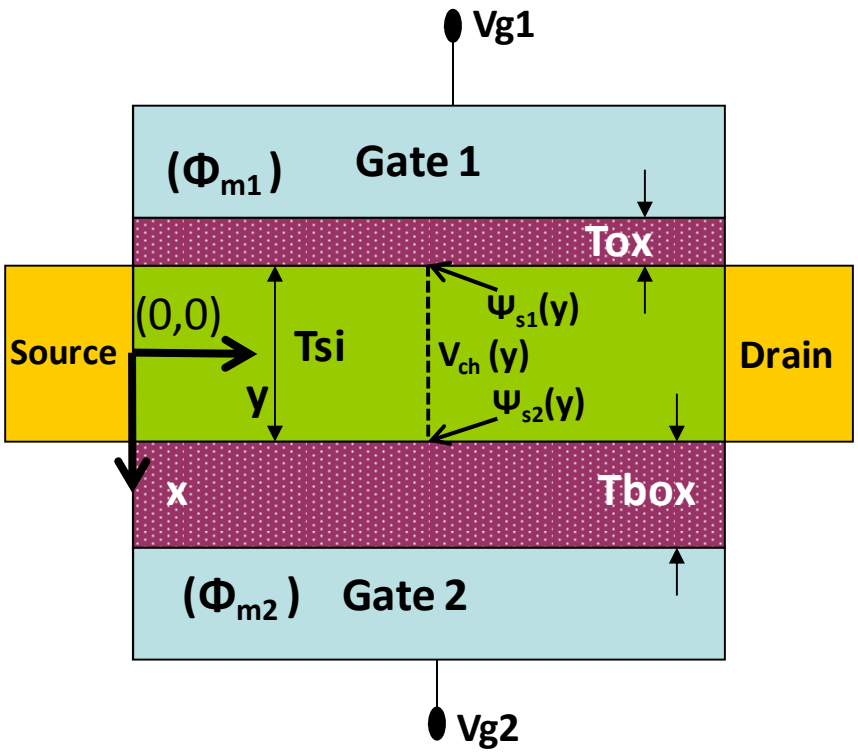

Figure 3.1. Schematic of an IDG-FinFET showing the asymmetry in dielectric thickness and the gate work functions.

equation together with Gauss's law at the front and back surfaces as the boundary conditions, the electronic potential in the body is obtained.

The 1-D Poisson's equation for the lightly doped device can be written as

$$\frac{\partial^2 \psi(x,y)}{\partial x^2} = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q(\psi(x,y)-V_{ch}(y))}{kT}} \tag{3.1}$$

where q is the charge of an electron and n_i is the intrinsic carrier concentration, ε_{si} is the relative permittivity of silicon, k is the Boltzmann constant and T is temperature in Kelvin. Gauss's law at the front and back surface give rise to the following equation,

$$V_{g1} - V_{fb1} - \psi_{s1}(y) = -\frac{\varepsilon_{si}}{C_{ox1}} \cdot \left.\frac{\partial \psi(x,y)}{\partial x}\right|_{x=-\frac{T_{si}}{2}} \qquad (3.2a)$$

$$V_{g2} - V_{fb2} - \psi_{s2}(y) = \frac{\varepsilon_{si}}{C_{ox2}} \cdot \left.\frac{\partial \psi(x,y)}{\partial x}\right|_{x=+\frac{T_{si}}{2}} \qquad (3.2b)$$

The solution of Eq. (3.1) depends upon the existence of a zero electric field plane, $\left.\frac{\partial \psi(x,y)}{\partial x}\right|_{x=x_0} = 0$. In cases where the device is heavily asymmetrical in terms of work function difference between the two gates, the front and back oxide thickness, the bias applied at both the gates, (as the devices under consideration for this research are) the zero electric plane may not exist at all. In this case, the potential profile in the body is given as

$$\psi(x,y) = V_{ch}(y) - \frac{2kT}{q} \cdot \ln\left(\frac{T_{si}}{2\beta}\sqrt{\frac{q^2 n_i}{2\varepsilon_{si}kT}}\sinh\left(\frac{2\beta x}{T_{si}} + \alpha\right)\right) \qquad (3.3)$$

The unknowns in the equation, α and β, are determined by solving the new boundary conditions which are obtained by using the definition of the potential profile in Eq. (3.2):

$$V_{g1} - V_{fb1} - V_{ch}(y) = r_0 + \frac{2kT}{q}\ln\left(\frac{2\beta}{\sinh(\alpha-\beta)}\right) + r_1\beta\coth(\alpha-\beta) \qquad (3.4a)$$

$$V_{g2} - V_{fb2} - V_{ch}(y) = r_0 + \frac{2kT}{q}\ln\left(\frac{2\beta}{\sinh(\alpha+\beta)}\right) - r_2\beta\coth(\alpha+\beta) \qquad (3.4b)$$

here, $r_0 = \frac{kT}{q}\ln\left(\frac{2\varepsilon_{si}kT}{q^2 n_i T_{si}^2}\right)$, $r_1 = \frac{4kT\varepsilon_{si}}{qC_{ox}T_{si}}$,and $r_2 = \frac{4kT\varepsilon_{si}}{qC_{box}T_{si}}$. If the zero electric plane does exist then instead of the hyperbolic functions (sinh) ordinary trigonometric functions (sin) would be used to model the device.

By solving transcendental nonlinear equations in Eq. (3.4a) and Eq. (3.4b) for the roots α and β and substituting it in Eq. (3.2a) and Eq. (3.2b), front and back surface potentials can be calculated. Figure 3.2 shows the front and back surface potentials of IDG-FinFET with gate works functions set to 4.05eV and 5.1eV, the front and back gate oxide set to 1.5 nm each. The silicon film set to 20 nm. Figure 3.3 shows the front and back surface potentials for a fully symmetric FinFET (front and back work functions set to 5.1eV). It can be seen that both front and back surface potentials are equal in this case.

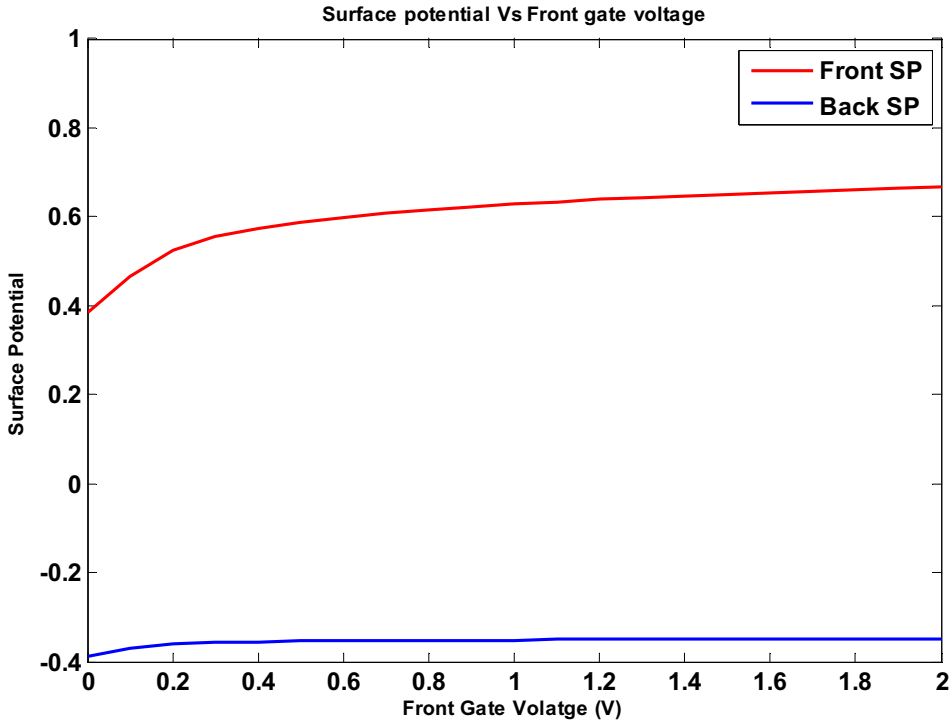

Figure 3.2. Front and Back Surface potentials of an IDG-FinFET

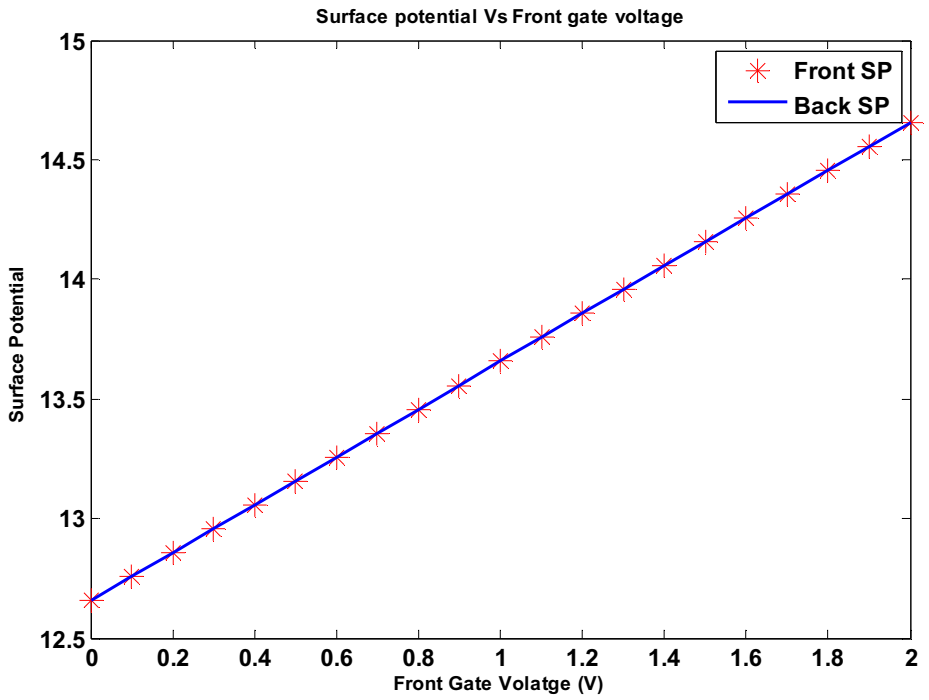

Figure 3.3. Front and Back Surface potentials of a fully symmetric IDG-FinFET

3.1.2. Analytical Model for IDG-FlexFET

This section describes the equations used to model the behavior of IDG-FlexFET. Figure 3.4 shows the schematic of a typical IDG-FlexFET. The figure shows a typical FlexFET with a MOSFET top gate with work function Φ_{m1} and a bottom JFET gate with work function Φ_{m2}. The top oxide thickness is *Tox* and there is no bottom oxide layer in the case of a FlexFET. The Silicon channel thickness is *Tsi*. $V_{ch}(y)$ is the channel potential and it is equal to zero at the source end and equal to *Vds* at the drain end. The front and back surface potentials of the device are represented as Ψ_{s1} and Ψ_{s2}.

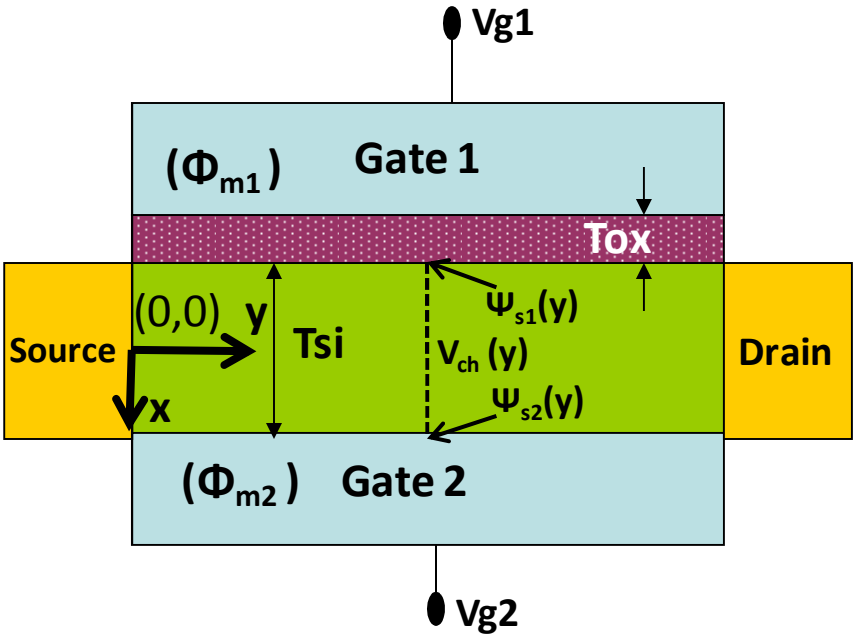

Figure 3.4. Schematic of an IDG-FlexFET showing the asymmetry in structure and the gate work functions.

The difference in IDG-FinFET and IDG-FlexFET structurally is the absence of a bottom oxide layer in the latter. In terms of the difference in analytical models, the IDG-FlexFET would have different boundary conditions which are affected by the absence of *Tbox* or effectively *Tbox*=0. The Gauss's law at the front and back surface for this device are now

$$V_{g1} - V_{fb1} - \psi_{s1}(y) = -\frac{\varepsilon_{si}}{C_{ox1}} \cdot \left.\frac{\partial \psi(x,y)}{\partial x}\right|_{x=-\frac{T_{si}}{2}} \qquad (3.5a)$$

$$\psi_{s2}(y) = V_{g2} - V_{fb2} = \text{Constant} \qquad (3.5b)$$

The surface potential of the bottom gate in the case of a IDG-FlexFET is a constant with respect to device parameters and front gate voltage and varies only with respect to bottom gate voltage. The constants that the device parameters affect, $r_0 = \frac{kT}{q}\ln\left(\frac{2\varepsilon_{si}kT}{q^2 n_i T_{si}^2}\right)$, $r_1 = \frac{4kT\varepsilon_{si}}{qC_{ox}T_{si}}$,and $r_2 = 0$ as Tbox=0. This affects the boundary conditions, which would become

$$V_{g1} - V_{fb1} - V_{ch}(y) = r_0 + \frac{2kT}{q}\ln\left(\frac{2\beta}{\sinh(\alpha-\beta)}\right) + r_1\beta\coth(\alpha-\beta) \qquad (3.6a)$$

$$V_{g2} - V_{fb2} - V_{ch}(y) = r_0 + \frac{2kT}{q}\ln\left(\frac{2\beta}{\sinh(\alpha+\beta)}\right) \qquad (3.6b)$$

By solving transcendental nonlinear equations in Eq. (3.6a) and Eq. (3.6b) for the roots α and β and substituting it in Eq. (3.5a) and Eq. (3.5b), front and back surface potentials of IDG-FlexFET can be calculated. Figure 3.5 shows the front and back surface potentials of IDG-FlexFET with gate works functions set to N+ and P+, the front and back gate oxide set to 1.5 nm each. The silicon film set to 20 nm.

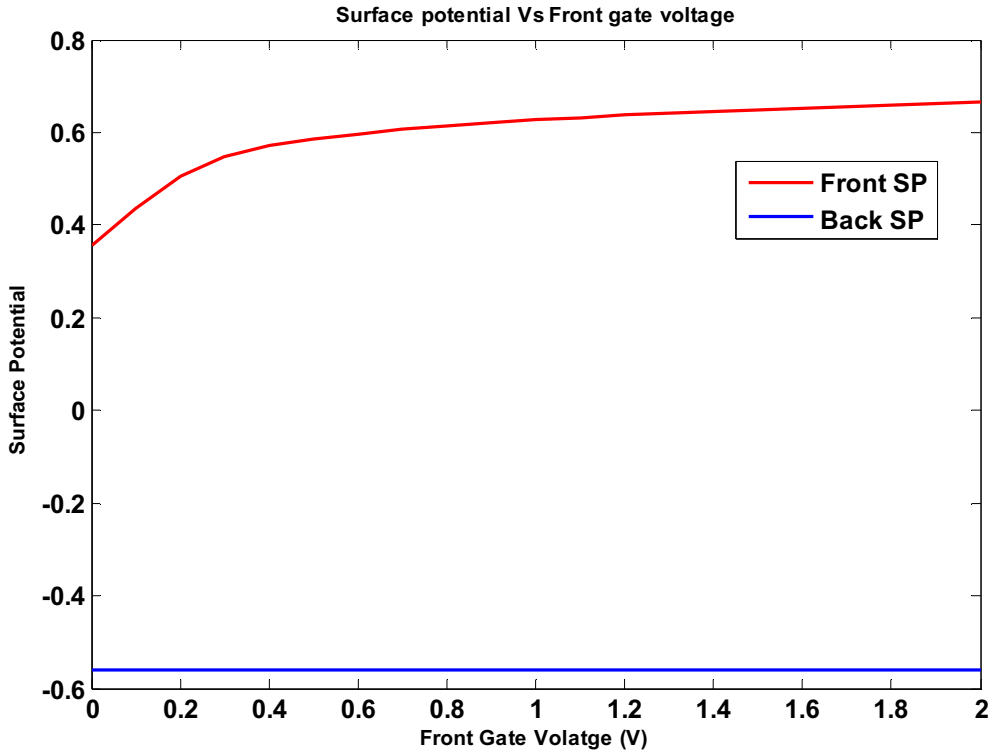

Figure 3.5. Front and Back Surface potentials of an IDG-FlexFET

The surface potentials in both these models at the source end and the drain end are obtained by solving these equations at *Vch=0* for source end and *Vch=Vds* for drain end.

3.2. I-V Model

In order to analyze and evaluate the performance of any transistor, the output of the device, i.e, the drain current is common measure. The drain current of a double gated transistor can be modeled as

$$I_d = 2 * \mu * \frac{W}{L} * (f(\psi_s) - f(\psi_d)) \tag{3.7}$$

where μ is the carrier mobility, W and L are the channel width and length, $f(\psi_s)$ is the term computed at the source end and $f(\psi_d)$ is the term computed at the drain end, $f(\psi_s)$ is given as

$$f(\psi_s) = \frac{Q_{inv}^2}{2 * C_{ox}} + 2\phi_t Q_{inv} - \phi_t \left(\frac{5\varepsilon_{si}\phi_t}{Tsi} + Qbulk\right) * \left(\ln\left(\frac{5\varepsilon_{si}\phi_t}{Tsi} + Qbulk + Q_{inv}\right)\right) \tag{3.8}$$

Here Q_{inv} is the inversion charge in one of the body. The factor of two accounts in the expression for the drain current accounts for the other half of the inversion charge. Inversion charge is computed as

$$Q_{inv} = Q_{total} - Q_{bulk} \tag{3.9}$$

In case of a lightly doped body the bulk charge would be negligible as a result of which inversion charge is equal to the total charge in the body. The total charge in the body is given as

$$Q_{total} = C_{ox}(V_{gs} - V_{fb} - \psi_s) \tag{3.10}$$

where ψ_s is the front surface potential computed at either the source or the drain end depending upon if $f(\psi_s)$ or $f(\psi_d)$ is being computed.

The surface potentials computed using the equations in the analytical model sections for both IDG-FinFET and IDG-FlexFET are used in computing the drain current

generated by each of these devices for comparing their performance using different metrics.

CHAPTER 4

IDG FETS AND HIGH DYNAMIC THRESHOLD CONTROL FACTOR

With the increasing need for Ultra Low Power transistors and ICs, ULP research is being carried out to explore new device models that can deliver to that end. This chapter analyzes the performance of two independent double gated transistors, FinFET and FlexFET, in terms of threshold voltage and the dynamic threshold control factor. The effect of different design parameters on each of these metrics has been analyzed to determine which device model meets the ULP requirement closely.

4.1. Performance Metrics

In order to design a device that can be useful for ULP applications, it is important to have a device that can be turned ON with the application of a reasonable amount of bias or input voltage. This means that the threshold voltage of the device needs to be less than the supply voltage so that turning it ON is not too hard. Nor should it be too low, so that even when it is turned off the sub-threshold leakage current would be too high.

Also, with the passage of time most of these devices are subjected to aging effects which cause the designed threshold of the device to degrade to a value that the circuit/ application was not originally designed for. If the only way to change the threshold voltage back to its original design point were to change the physical dimensions of the device, it would be impossible. It is desirable to have a device that can be **dynamically** reconfigured to restore its threshold to the value of choice.

With these requirements for ULP devices, the metrics used to evaluate the performance of the independent double-gated transistors, are threshold voltage and dynamic control factor; both of these are explained in detail later in this section. For a given device it is desirable to have a low threshold voltage and a high dynamic control factor in order to achieve ultra low power circuit designs.

4.1.1. Threshold Voltage

Threshold voltage is the gate voltage at which the device is turned "ON." For this work, the threshold voltage is defined as the voltage where the drain current equals a magnitude of 100 nA $\frac{W}{L}$. In case of IDG transistors it is possible to change the threshold voltage dynamically by merely changing the back gate voltage applied to the device. From Figure 4.1 the definition of threshold voltage in this work is clear.

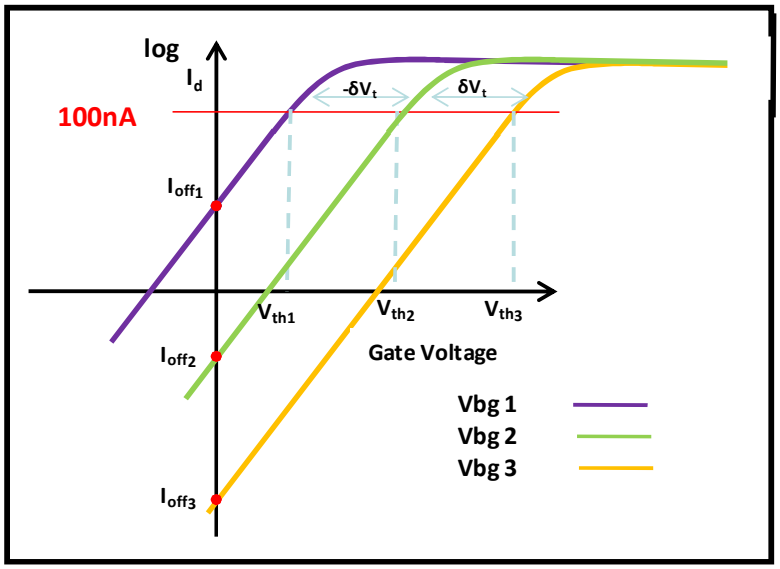

Figure 4.1. Definition of Threshold Voltage

It can be seen that a certain back gate voltage, Vbg1, results in a low threshold voltage, and high Ioff1 or leakage current. Also a back gate voltage of Vbg3, results in a high threshold voltage and an Ioff3, or leakage current which is very low. The aim of this work is come up with device models with appropriate device parameters that result in giving a threshold voltage variation from 0 V to 1 V for a back gate voltage variation from 0.5 V to -0.5 V, respectively. Table 4.1 gives the summary of this.

4.1.2. Dynamic Threshold Control Factor

The dynamic threshold control factor (f) is the rate at which the threshold voltage changes in response to the change in bottom gate voltage in the region of V_{BG}=0. This is the transition from the accumulated mode, to the inverted mode as can be seen in Figure 4.2. The transition through the depleted mode, where the device is switched OFF to a point where it is switched ON, needs to be as abrupt as possible. Ideally, the higher the dynamic threshold control factor, the better for most applications.

Table 4.1. Objective for an Ideal Device for ULP applications

V_{BG} (V)	V_T (V)
-0.5	1
0	0.5
0.5	0

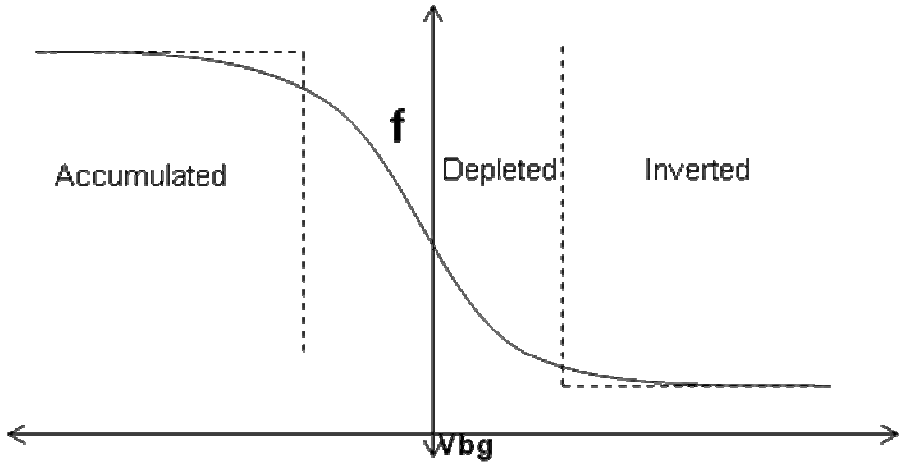

Figure 4.2. Definition of Dynamic Threshold Control Factor

4.2. Device Parameters

This work aims at identifying different designs of IDG devices that have a dynamic threshold control factor greater than or equal to 1.

The different device parameters considered for this work are top oxide thickness, silicon film thickness, and the top/front and bottom/back gate work functions. Each of these parameters was varied to Study their effect on the threshold voltage and dynamic threshold control factors of different models of FinFET and FlexFET.

4.2.1. Top Oxide Thickness

Threshold voltage of a given device is directly proportional to the top oxide thickness of the device. This can be explained as follows: As the insulator layer increases more bias is needed for the field to penetrate it. As this occurs, more minority carriers are

attracted to the metal-semiconductor interface, thereby causing the formation of the inversion channel and thus conduction of current. This trend can be seen in Figure 4.3.

In case of FinFET, the front and back gates are both MOSFETs. The front and back gate oxide thickness, has been fixed at 3 nm for this cases simulation purposes. In case of FlexFET, the bottom gate is a JFET which means that the buried oxide layer is zero. The top oxide was fixed to 3 nm while simulating the effects of varying other parameters. To Study the effect of top oxide thickness on the devices, it has been varied from 1 nm to 10 nm.

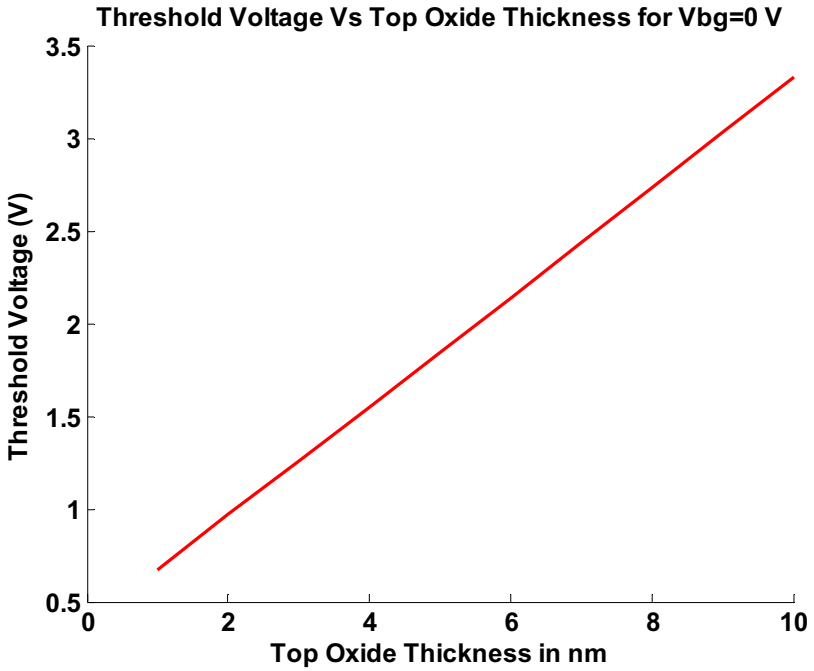

Figure 4.3. Variation of Threshold Voltage with Top Oxide Thickness

4.2.2. Silicon Film Thickness

Threshold voltage of a device is inversely proportional to the change in the silicon film thickness. As the silicon film thickness increases, the carrier concentration increases, which means that with a little input bias, a greater amount of charge carriers accumulate near the metal-semiconductor interface, causing depletion and thereby inversion to take place quickly, resulting in lower threshold voltages. The trend of threshold voltage to silicon film thickness variation can be seen in Figure 4.4.

The silicon film thickness was kept at 10 nm for simulations where other parameters were varied. To Study the effect of silicon film thickness on FinFET and FlexFET, it has been varied from 6 nm to 30 nm.

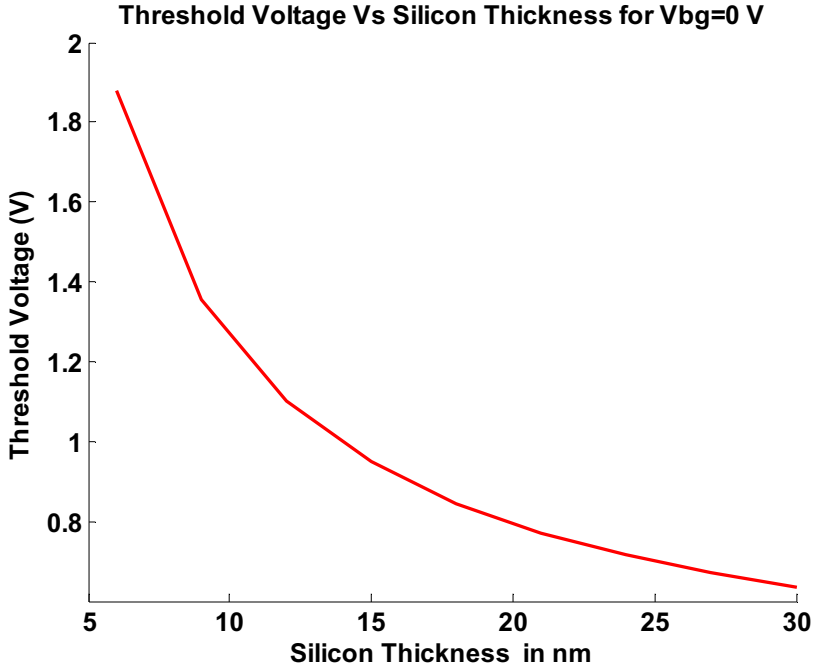

Figure 4.4. Threshold Voltage variation with variation in Silicon Film Thickness

4.2.3. Gate Work Functions

The gate work functions of the IDG FinFET and IDG FlexFET used for simulations are

(a) N+ - 4.00eV

(b) Midgap – 4.55eV

(c) P+ - 5.1eV.

The top/ front gate of both IDG FinFET and IDG FlexFET can be any of the three work functions mentioned. However in case of the bottom/back gate only P+ and Midgap gates can be used, since FlexFET has a JFET bottom gate and using a N+ gate with a n-channel would result in electrical short between source, bottom gate, and drain.

4.3. Device Models

Overall six different combinations of top and bottom gate work functions were modeled, including varying the silicon and oxide thicknesses. Each of these six cases can be divided into three categories based upon the level of asymmetry in the work functions used for the top and bottom gates. The devices used can also be seen in Table 4.2.

(a) Symmetrical

a. Midgap (Top gate) – Midgap (Bottom gate)

b. P+ (Top gate) – P+ (Bottom gate)

(b) Half-Asymmetry

a. Midgap (Top gate) – P+ (Bottom gate)

b. P+ (Top gate) – Midgap (Bottom gate)

c. N+(Top gate) – Midgap (Bottom gate)

(c) Full-Asymmetry

a. N+ (Top gate) – P+ (Bottom gate)

Table 4.2. Device Models used for research

	Top/Front Gate			
Bottom\Back Gate	Work Functions	4.0 eV(N+)	4.55 eV (Midgap)	5.1 eV (P+)
	4.55 eV (Midgap)	Half Asymmetry	Symmetrical	Half Asymmetry
	5.1 eV (P+)	Full Asymmetry	Half Asymmetry	Symmetrical

4.4. Simulation Results

The trends for threshold voltage and dynamic threshold control factor were computed for variation in silicon film thickness, top oxide thickness for different values of back gate voltages; namely, -0.5V, 0V, 0.5V. The aim of the work was to optimize the IDG design parameters that give rise to a threshold voltage that could range between 0 V to 1 V and a dynamic control factor that was higher than 1.0. The simulations were run in MATLAB for all six cases in three different categories of asymmetry.

Each different case would have different roots for the boundary equations to compute the surface potentials and thereby compute the drain current, threshold voltage and dynamic threshold control factor. The roots have to be computed using iterative methods where the starting point is fed into the algorithm manually. Initial starting point is important at arriving at the global minimum for the equations. By trial and error method the starting point for each case needs to be manually tuned to arrive at the right set of roots to ensure convergence. Also each simulation takes up to 3 to 5 minutes per single transistor cases.

4.4.1. Symmetrical

Here the top and bottom gates are identical for both IDG FinFET and IDG FlexFET. The results under two cases under this category would be presented in this section.

4.4.1.1. Midgap (top gate) – Midgap (bottom gate). Here the top gate is set to 4.55eV and the bottom gate is set to 4.55eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.5, Figure 4.6, and Figure 4.7, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.8. Table 4.3 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to

1V. In case of IDG-FlexFET, the threshold voltage increases sharply with increase in top oxide thickness; however, around 3 nm of top oxide thickness it can be observed that the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

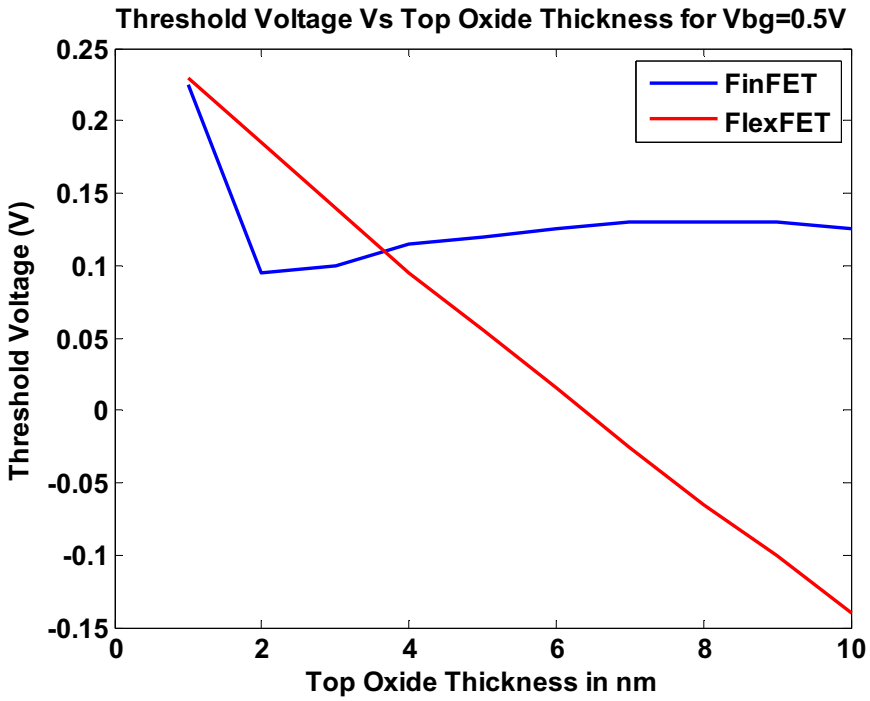

Figure 4.5. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V - Midgap (TG) – Midgap (BG)

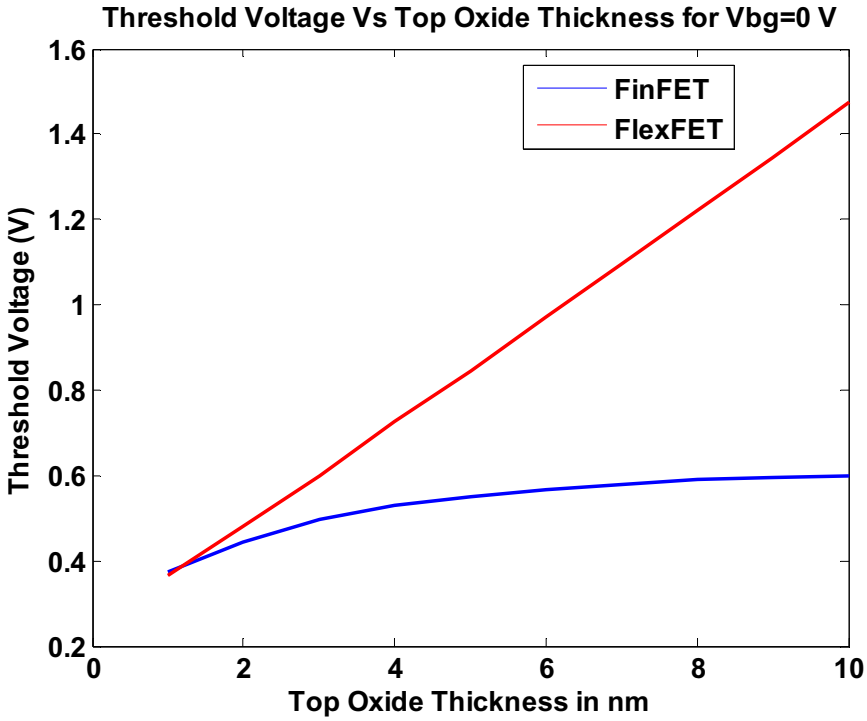

Figure 4.6. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0 V Midgap (TG) – Midgap (BG)

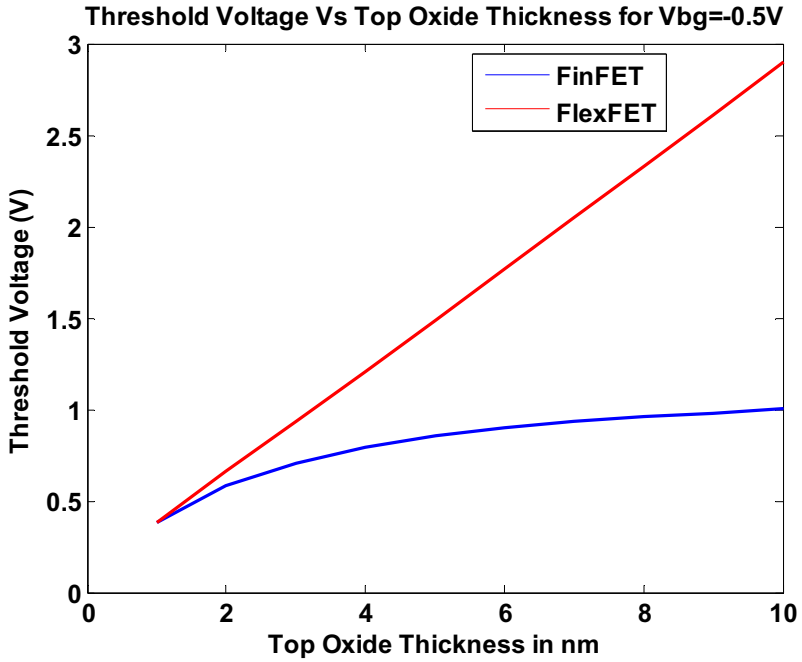

Figure 4.7. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5 V- Midgap (TG) – Midgap (BG)

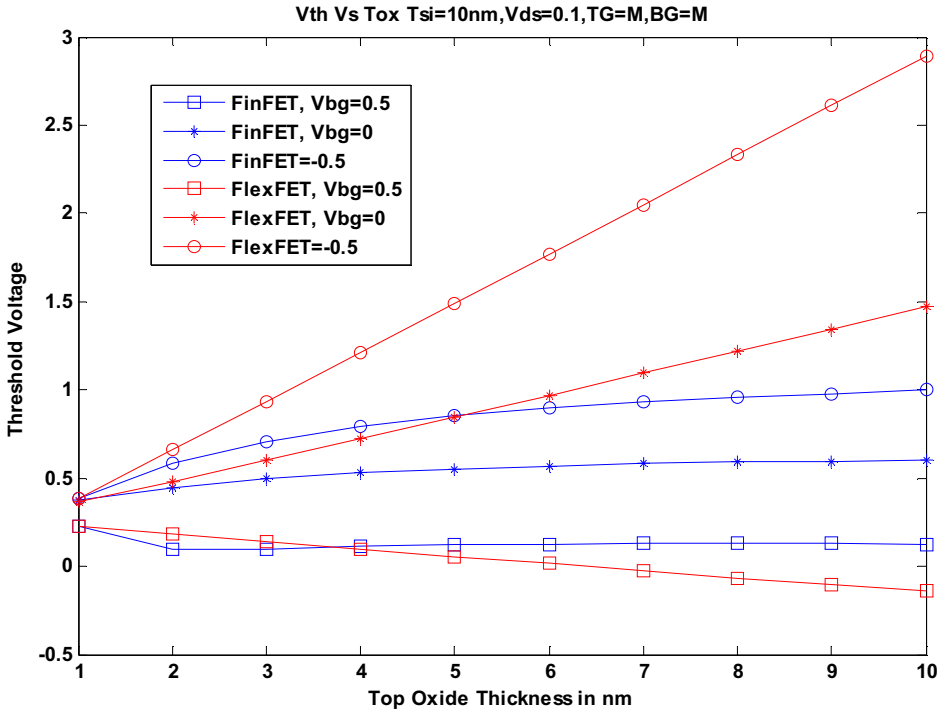

Figure 4.8. Variation of Threshold Voltage with Change in Top Oxide Thickness Midgap (TG) – Midgap (BG)

Table 4.3. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg- Midgap (TG) – Midgap (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	0.225	0.375	0.385	0.23	0.365	0.385
2	0.095	0.445	0.585	0.185	0.48	0.66
3	0.1	0.495	0.71	0.14	0.6	0.935
4	0.115	0.53	0.795	0.095	0.725	1.21
5	0.12	0.55	0.855	0.055	0.845	1.49
6	0.125	0.565	0.895	0.015	0.97	1.77
7	0.13	0.58	0.93	-0.025	1.095	2.05
8	0.13	0.59	0.96	-0.065	1.22	2.33
9	0.13	0.595	0.98	-0.1	1.345	2.61
10	0.125	0.6	1	-0.14	1.475	2.895

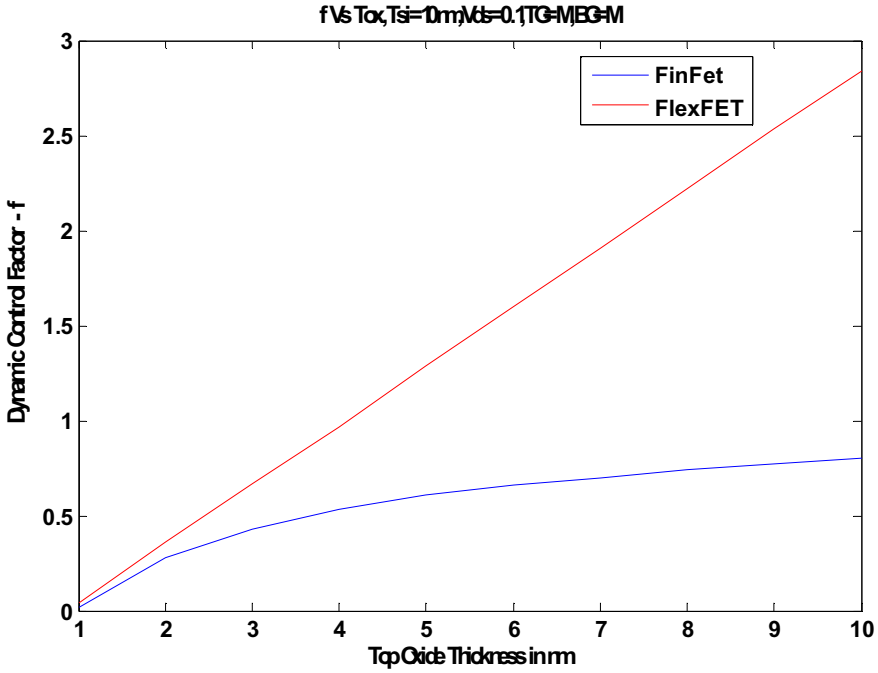

Figure 4.9. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness Midgap (TG) – Midgap (BG)

Table 4.4. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness -- Midgap (TG) – Midgap (BG)

TOX in nm	FinFET f	FlexFET f
1	0.3	0.27
2	0.7	0.59
3	0.79	0.92
4	0.83	1.26
5	0.86	1.58
6	0.88	1.91
7	0.9	2.24
8	0.92	2.57
9	0.93	2.89
10	0.95	3.23

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.9 and the data are in Table 4.4. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness; whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

So as far as top oxide thickness variation is concerned, only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in this case.

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.10, Figure 4.11, and Figure 4.12, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.13. Table 4.5 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to 1V. In case of IDG-FlexFET, the threshold voltage decreases with increase in silicon film thickness; the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

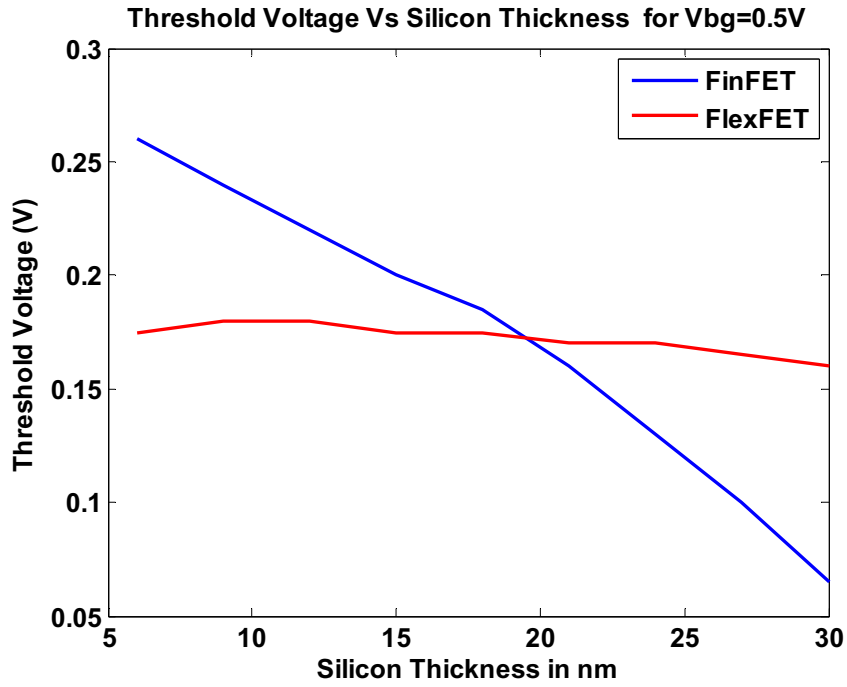

Figure 4.10. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0.5 V- Midgap (TG) – Midgap (BG)

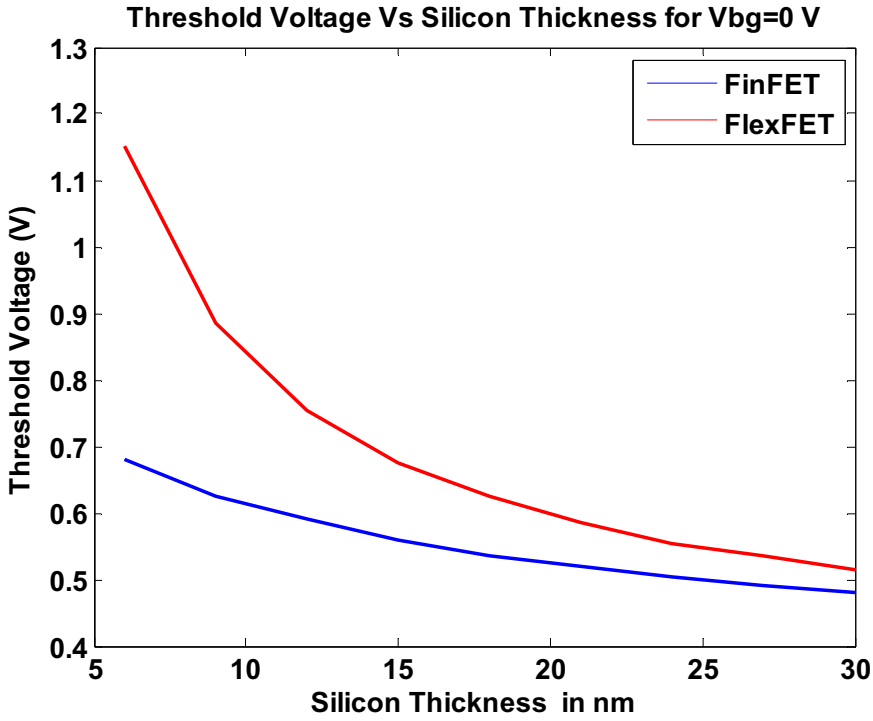

Figure 4.11. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0 V- Midgap (TG) – Midgap (BG)

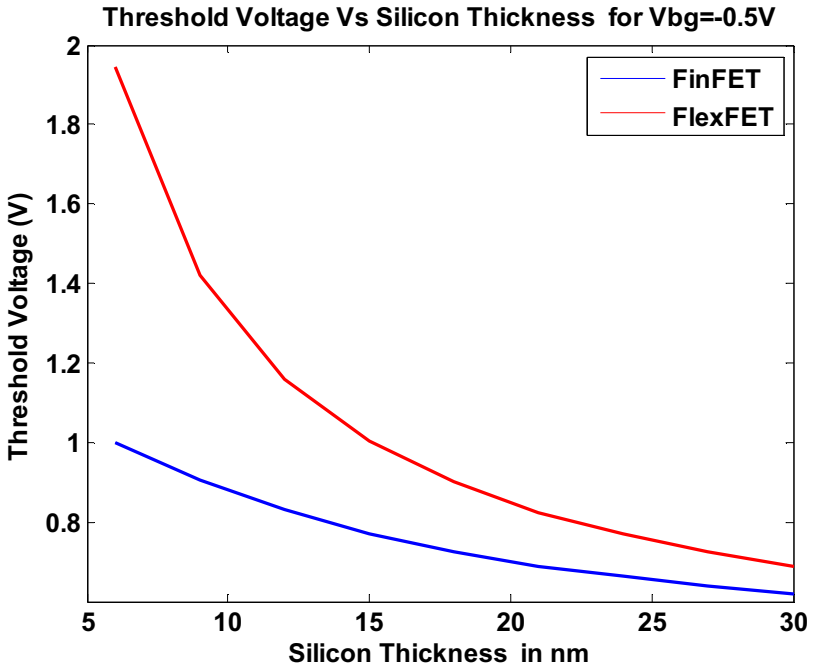

Figure 4.12. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=-0.5 V- Midgap (TG) – Midgap (BG)

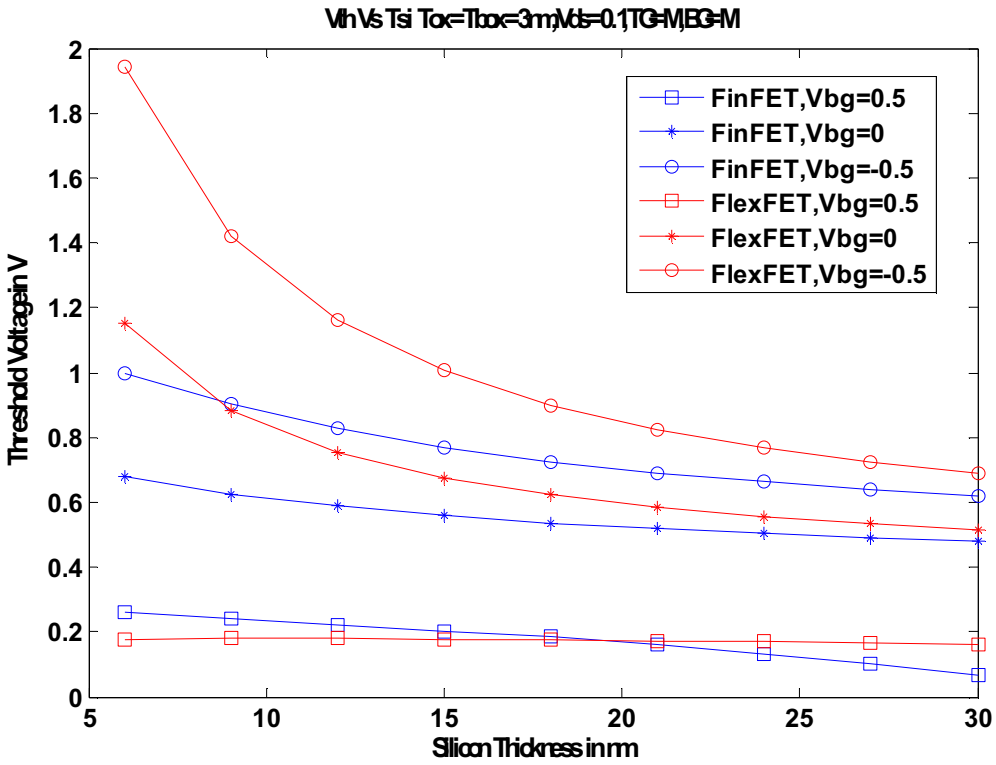

Figure 4.13. Variation of Threshold Voltage with Change in Silicon Film Thickness Midgap (TG) – Midgap (BG)

Table 4.5. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg- Midgap (TG) – Midgap (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	0.26	0.68	1	0.175	1.15	1.945
9	0.24	0.625	0.905	0.18	0.885	1.42
12	0.22	0.59	0.83	0.18	0.755	1.16
15	0.2	0.56	0.77	0.175	0.675	1.005
18	0.185	0.535	0.725	0.175	0.625	0.9
21	0.16	0.52	0.69	0.17	0.585	0.825
24	0.13	0.505	0.665	0.17	0.555	0.77
27	0.1	0.49	0.64	0.165	0.535	0.725
30	0.065	0.48	0.62	0.16	0.515	0.69

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.14 and the data are in Table 4.6. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So even with silicon film thickness variation only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in this case. IDG-FlexFET with Midgap (Top gate) and Midgap (Bottom gate) meets both the threshold voltage and dynamic threshold control factor criteria.

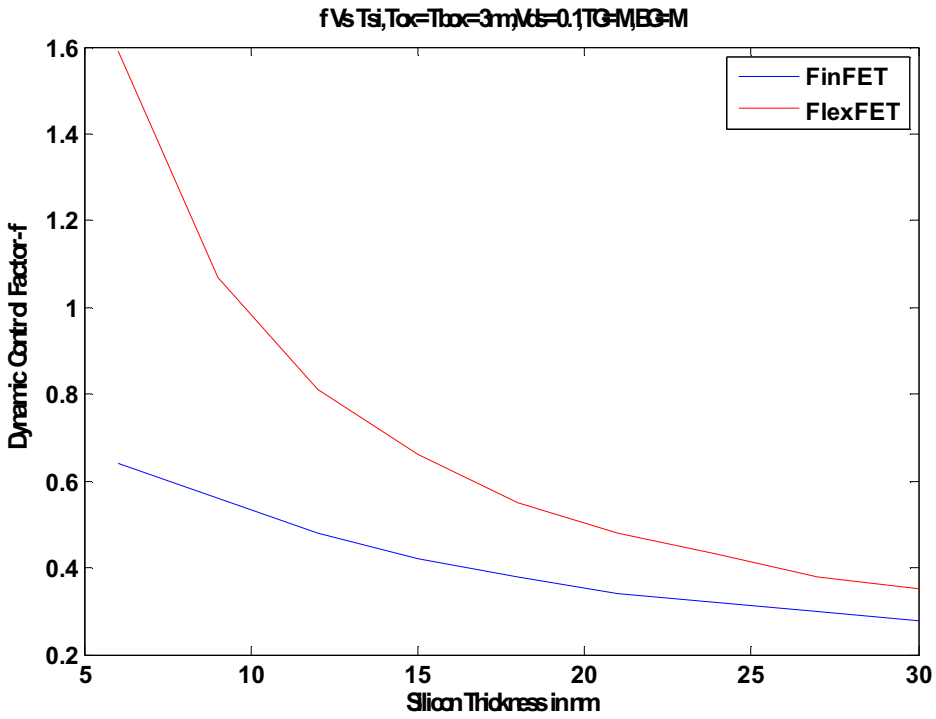

Figure 4.14. Variation of Dynamic Control Factor with Change in Silicon Film Thickness Midgap (TG) – Midgap (BG)

Table 4.6. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness- Midgap (TG) – Midgap (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.84	1.95
9	0.77	1.41
12	0.74	1.15
15	0.72	1
18	0.7	0.9
21	0.72	0.83
24	0.75	0.77
27	0.78	0.74
30	0.83	0.71

4.4.1.2. P+ (top gate) – P+ (bottom gate). Here the top gate is set to 5.1eV and the bottom gate is set to 5.1eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.15, Figure 4.16, and Figure 4.17, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.18. Table 4.7 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET that the threshold voltage in case of all three back gate voltages is out of the required range of 0V to 1V.

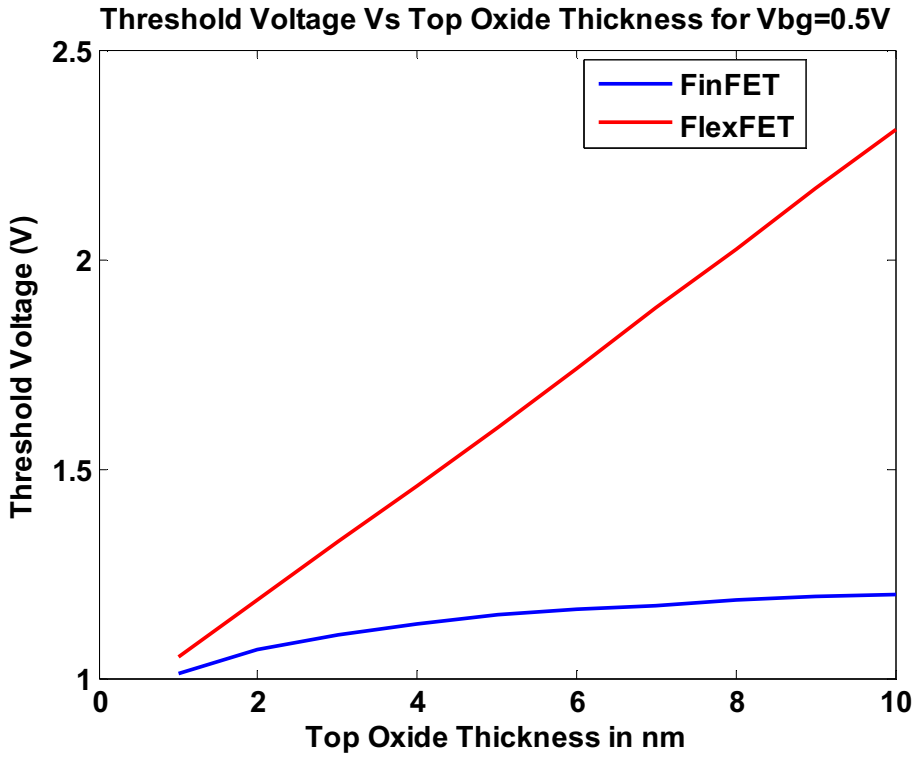

Figure 4.15. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V for P+ (TG) – P+ (BG)

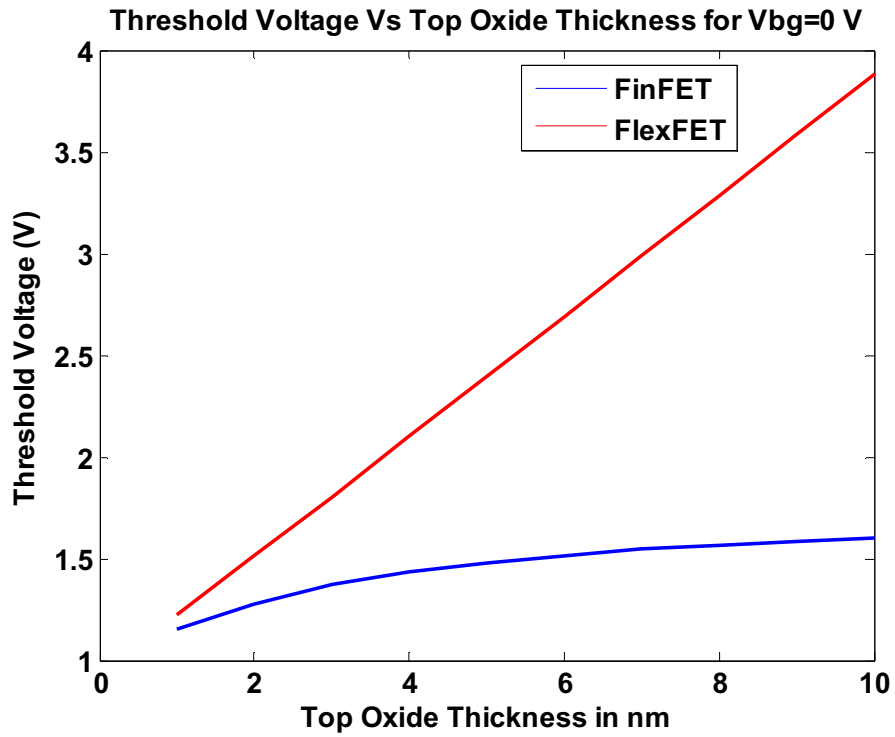

Figure 4.16. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0 V for P+ (TG) – P+ (BG)

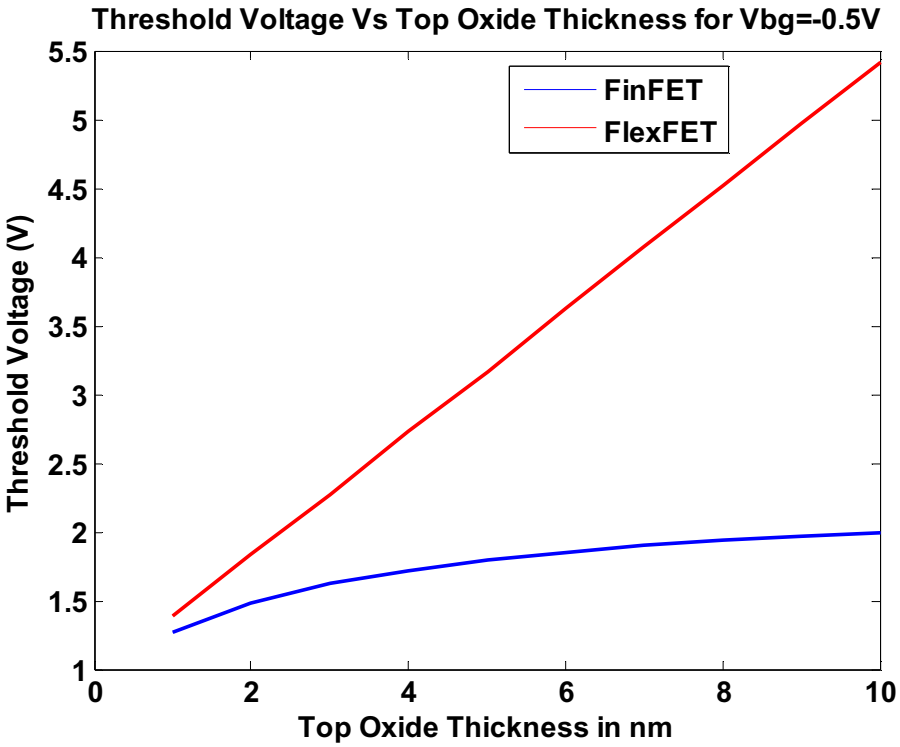

Figure 4.17. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5V for P+ (TG) – P+ (BG)

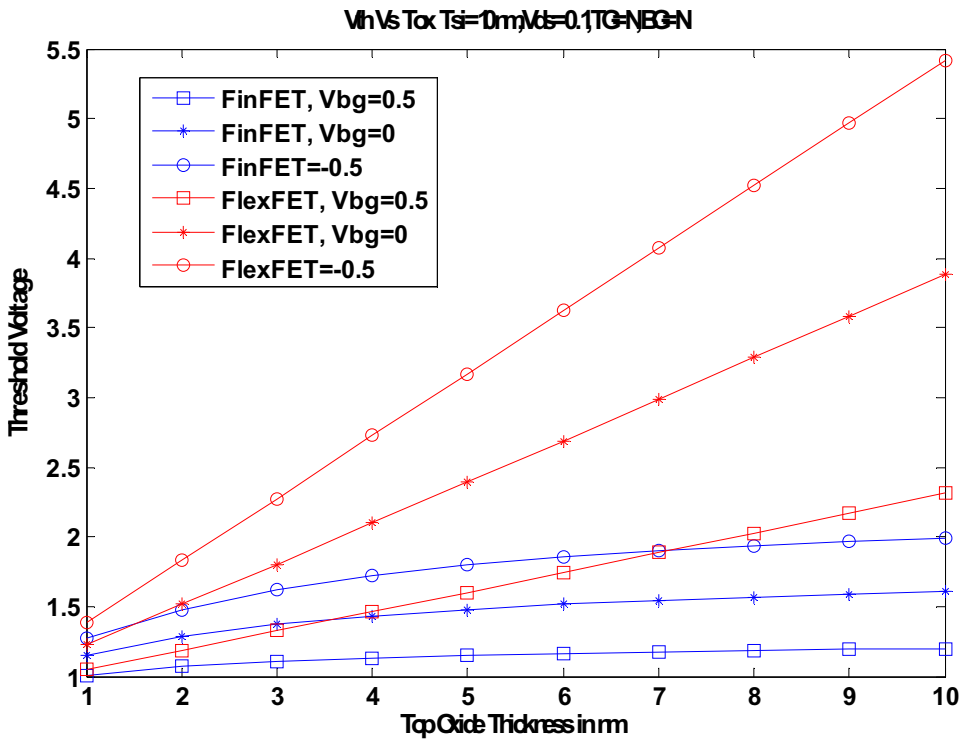

Figure 4.18. Variation of Threshold Voltage with Change in Top Oxide Thickness for P+ (TG) – P+ (BG)

Table 4.7. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg –P+ (TG) –P+ (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	1.01	1.15	1.275	1.05	1.225	1.39
2	1.07	1.28	1.48	1.185	1.515	1.83
3	1.105	1.37	1.62	1.325	1.805	2.275
4	1.13	1.435	1.72	1.46	2.1	2.725
5	1.15	1.48	1.795	1.6	2.395	3.17
6	1.165	1.515	1.855	1.74	2.69	3.62
7	1.175	1.545	1.9	1.885	2.99	4.07
8	1.185	1.57	1.94	2.025	3.285	4.52
9	1.195	1.585	1.97	2.17	3.585	4.97
10	1.2	1.605	1.995	2.31	3.88	5.42

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.19 and the data are in Table 4.8. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness, whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

However both the devices did **not** meet the threshold voltage criterion for top oxide thickness variation in this case.

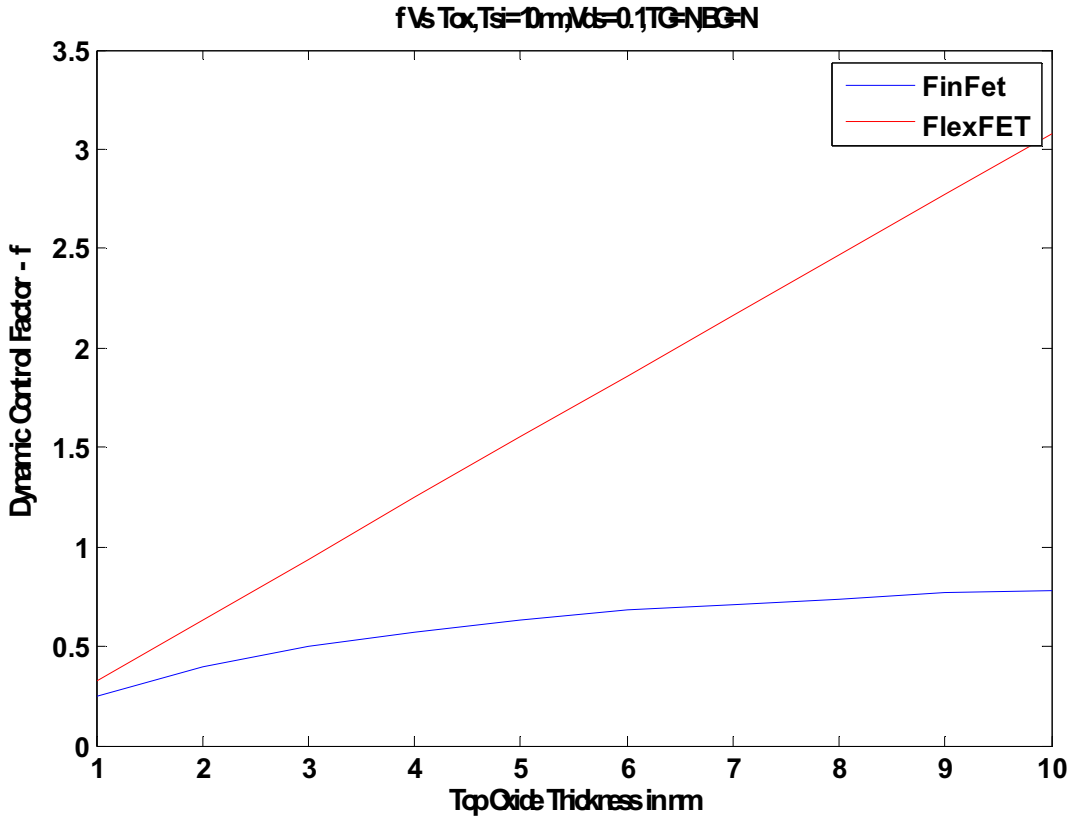

Figure 4 19. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness P+ (TG) – P+ (BG)

Table 4.8. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness- P+ (TG) – P+ (BG)

TOX in nm	FinFET f	FlexFET f
1	0.28	0.35
2	0.42	0.66
3	0.53	0.96
4	0.61	1.28
5	0.66	1.59
6	0.7	1.9
7	0.74	2.21
8	0.77	2.52
9	0.78	2.83
10	0.81	3.14

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.20, Figure 4.21, and Figure 4.22, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.23. Table 4.9 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET that the threshold voltage in case of all three back gate voltages is out of the required range of 0V to 1V for P+ (TG) – P+ (BG).

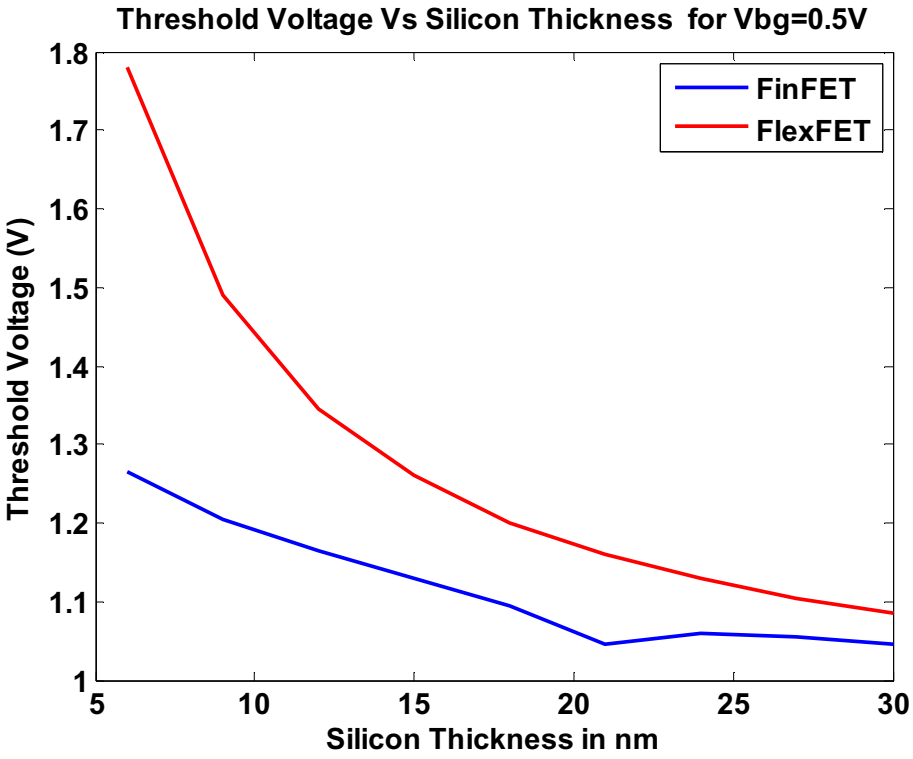

Figure 4.20. Variation of Threshold Voltage with Change in Silicon Film Thickness P+ (TG) – P+ (BG)

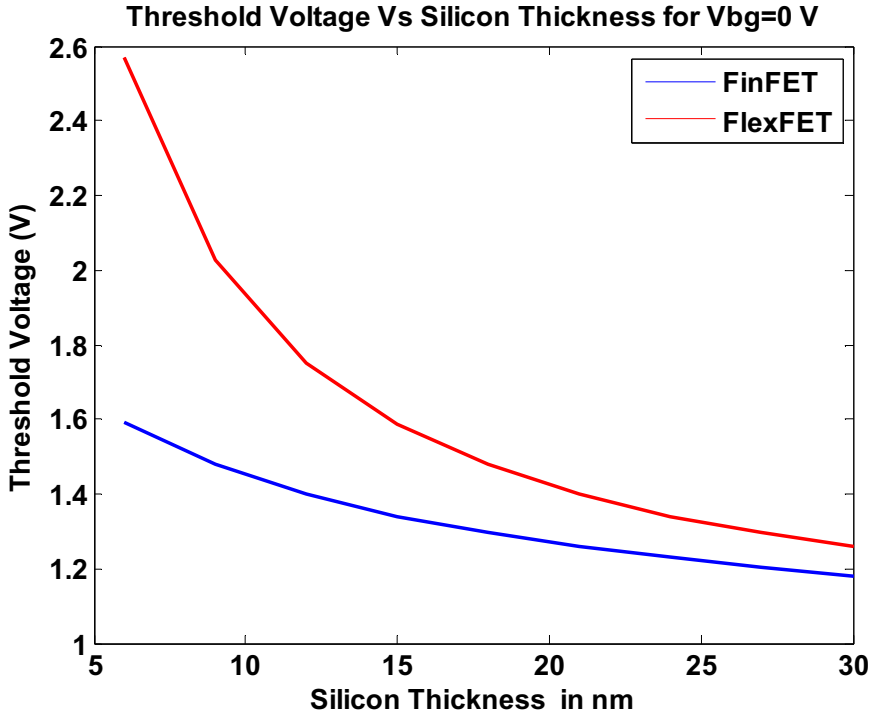

Figure 4.21. Variation of Threshold Voltage with Change in Silicon Film Thickness P+ (TG) – P+ (BG)

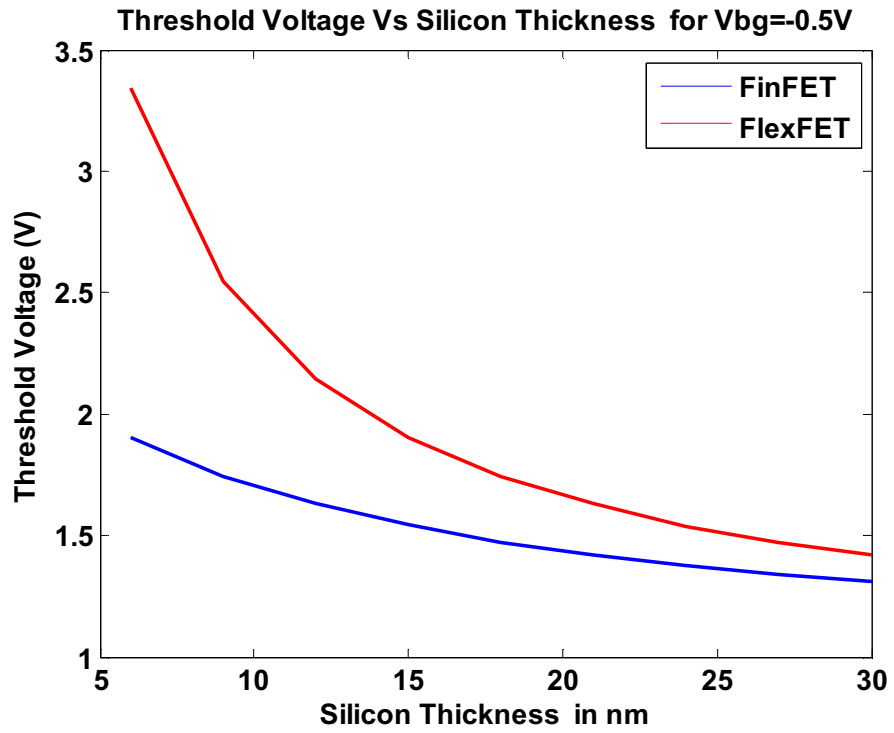

Figure 4.22. Variation of Threshold Voltage with Change in Silicon Film Thickness P+ (TG) – P+ (BG)

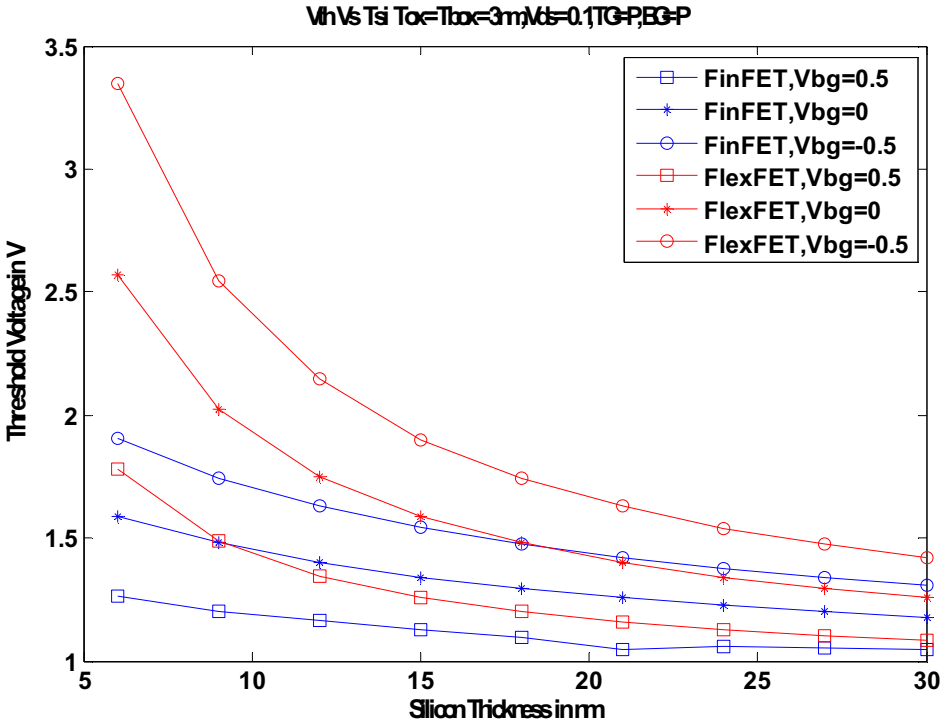

Figure 4.23. Variation of Threshold Voltage with Change in Silicon Film Thickness P+ (TG) – P+ (BG)

Table 4.9. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg - P+ (TG) – P+ (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	1.265	1.59	1.905	1.78	2.57	3.345
9	1.205	1.48	1.745	1.49	2.025	2.545
12	1.165	1.4	1.63	1.345	1.75	2.145
15	1.13	1.34	1.545	1.26	1.585	1.9
18	1.095	1.295	1.475	1.2	1.48	1.745
21	1.045	1.26	1.42	1.16	1.4	1.63
24	1.06	1.23	1.375	1.13	1.34	1.54
27	1.055	1.205	1.34	1.105	1.295	1.475
30	1.045	1.18	1.31	1.085	1.26	1.42

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.24 and the data are in Table 4.10. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So with silicon film thickness variation neither IDG-FinFET nor IDG-FlexFET meet the required criteria of threshold voltage and only IDG-FlexFET meets the dynamic control factor in the case of P+ (TG)- P+(BG).

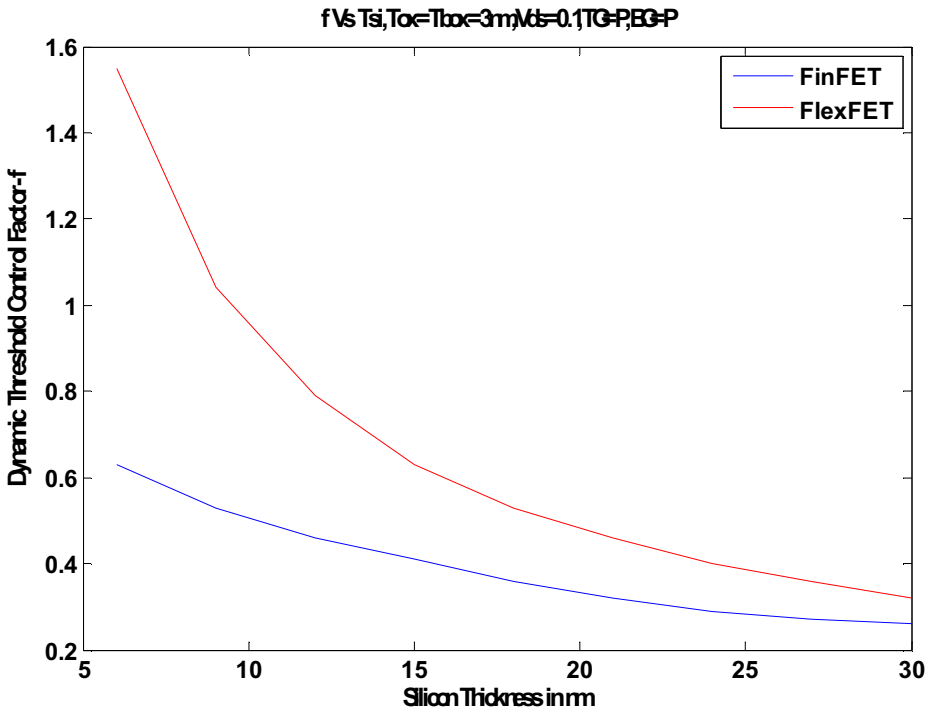

Figure 4.24. Variation of Dynamic Threshold Control Factor with Change in Silicon Film Thickness P+ (TG) – P+ (BG)

Table 4.10. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness - P+ (TG) – P+ (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.65	1.58
9	0.55	1.07
12	0.47	0.81
15	0.42	0.65
18	0.4	0.56
21	0.43	0.48
24	0.34	0.42
27	0.3	0.38
30	0.27	0.35

To summarize the symmetrical cases, the dynamic control factor for FlexFET is high in both the cases but that of FinFET is below 1.0 for the range of oxide and silicon thicknesses tested. The inherent asymmetry in structure that FlexFET has contributes to this advantage. Threshold voltage is in the required range for the case with mid-gap work functions, but not for P+/P+ work functions for FlexFET design. For FinFET the threshold voltage is within the required range in case of mid-gap and P+ work functions but since the dynamic control factor is low, FlexFET with mid-gap work functions is a better design.

4.4.2. Half-Asymmetry

Here there is 0.55eV difference in work function between the top and bottom gates for both IDG FinFET and IDG FlexFET. The results under three cases under this category would be presented in this section.

4.4.2.1. Midgap (top gate) – P+ (bottom gate). Here the top gate is set to 4.55eV and the bottom gate is set to 5.1eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.25, Figure 4.26, and Figure 4.27, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.28. Table 4.11 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to

1V. In case of IDG-FlexFET, the threshold voltage increases sharply with increase in top oxide thickness; however around 3 nm of top oxide thickness it can be observed that the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

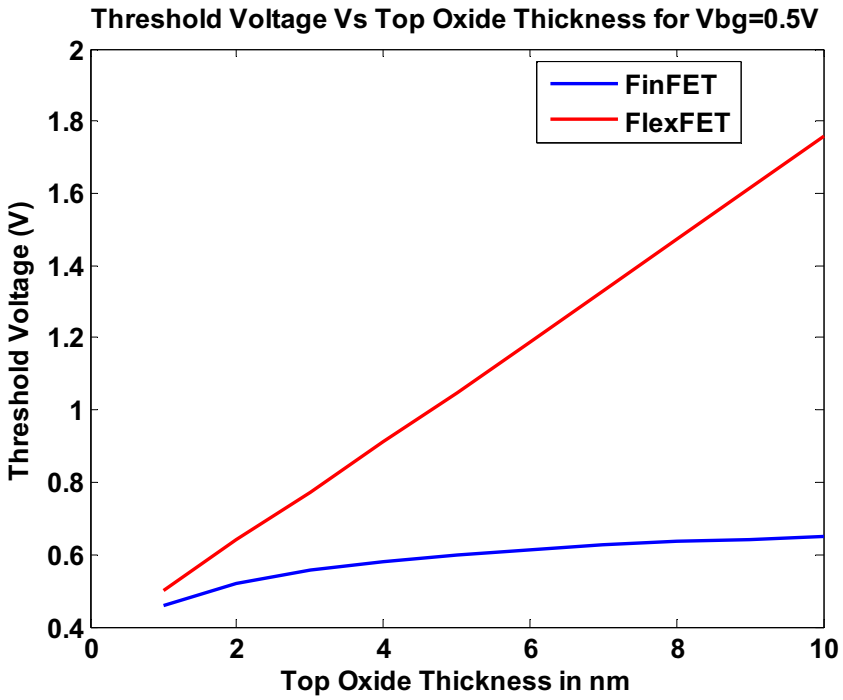

Figure 4.25. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V for Midgap (TG) – P+ (BG)

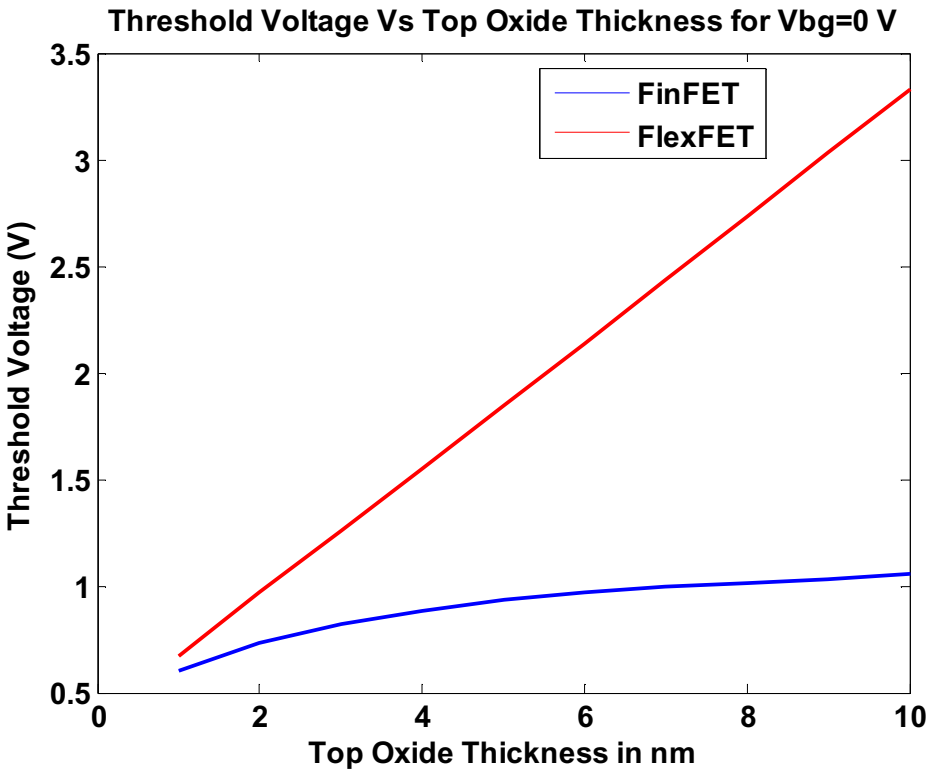

Figure 4.26. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0V for Midgap (TG) – P+ (BG)

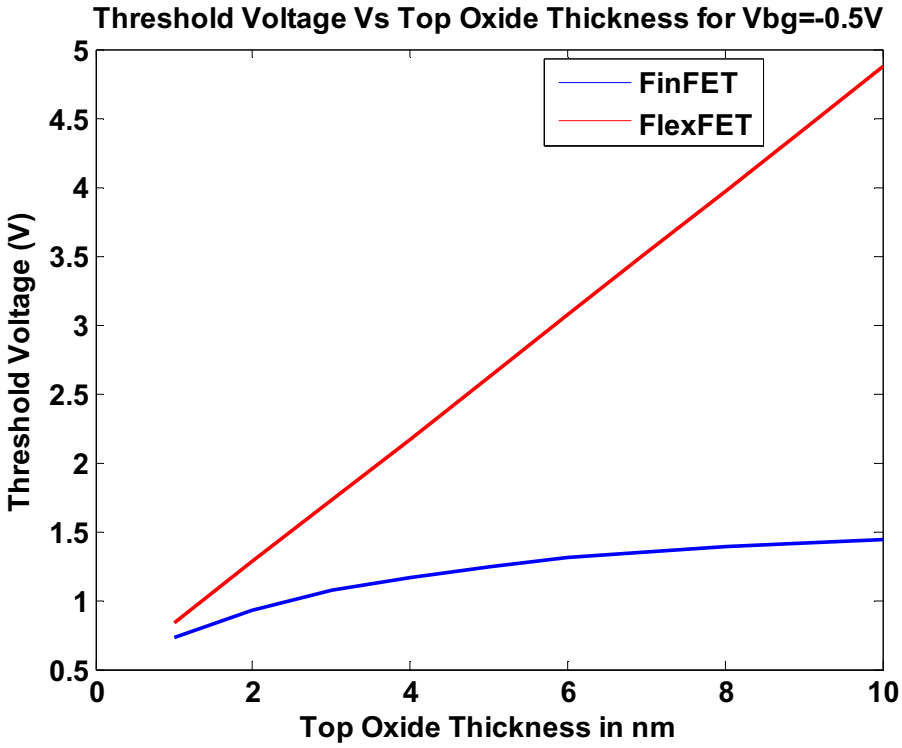

Figure 4.27. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5V for Midgap (TG) – P+ (BG)

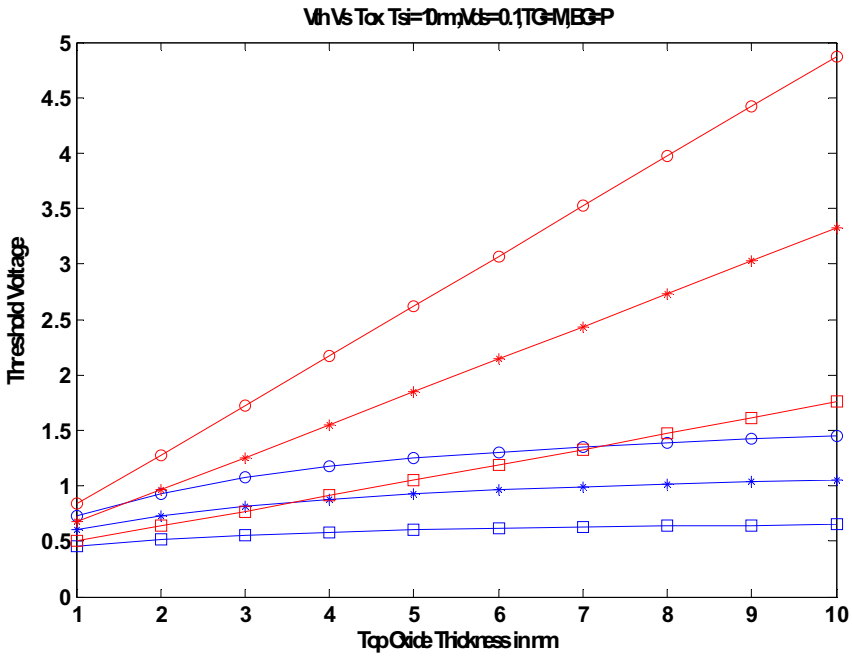

Figure 4.28. Variation of Threshold Voltage with Change in Top Oxide Thickness for Midgap (TG)-P+ (BG)

Table 4.11. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg – Midgap (TG) –P+ (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	0.46	0.6	0.725	0.5	0.675	0.835
2	0.52	0.73	0.93	0.64	0.965	1.28
3	0.555	0.82	1.07	0.77	1.255	1.725
4	0.58	0.88	1.17	0.91	1.55	2.17
5	0.6	0.93	1.245	1.05	1.845	2.62
6	0.615	0.965	1.305	1.19	2.14	3.07
7	0.625	0.995	1.35	1.33	2.435	3.52
8	0.635	1.015	1.385	1.475	2.735	3.97
9	0.64	1.035	1.42	1.615	3.03	4.42
10	0.65	1.055	1.445	1.76	3.33	4.87

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.29 and the data are in Table 4.12. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness; whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

So as far as top oxide thickness variation is concerned only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in this case.

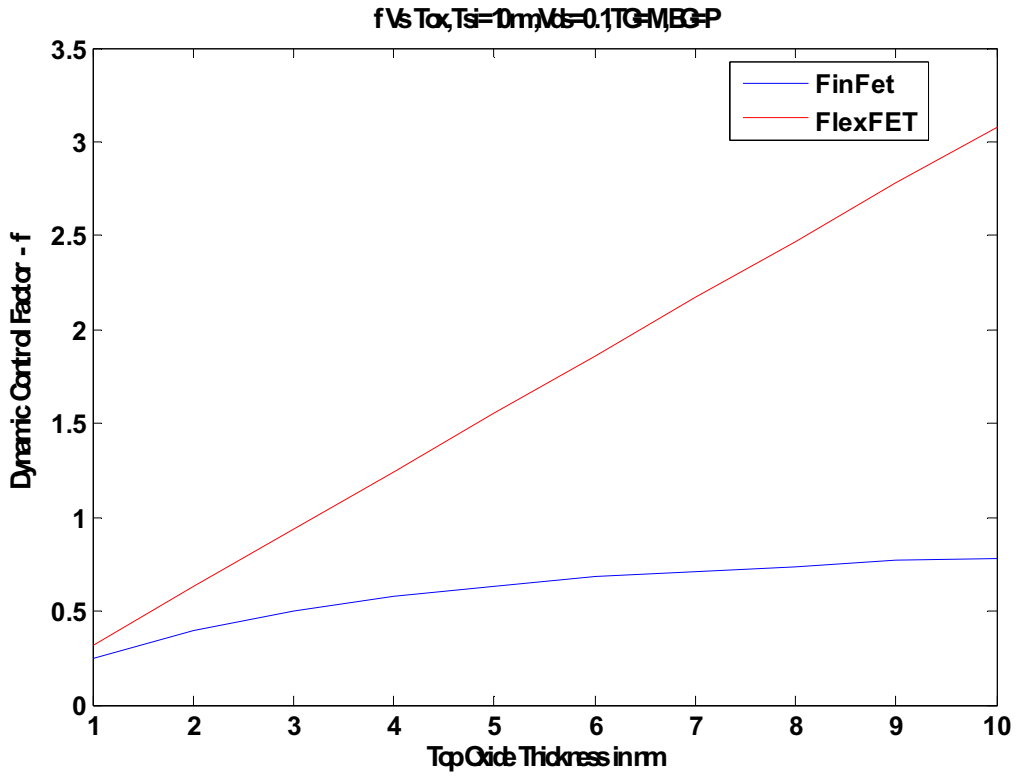

Figure 4.29. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness Midgap (TG) – P+ (BG)

Table 4.12. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness- Midgap (TG) – P+ (BG)

TOX in nm	FinFET f	FlexFET f
1	0.28	0.35
2	0.42	0.65
3	0.53	0.97
4	0.6	1.28
5	0.66	1.59
6	0.7	1.9
7	0.74	2.21
8	0.76	2.52
9	0.79	2.83
10	0.81	3.14

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.30, Figure 4.31, and Figure 4.32, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.33. Table 4.13 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to 1V. In case of IDG-FlexFET, the threshold voltage decreases with increase in silicon film

thickness, the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

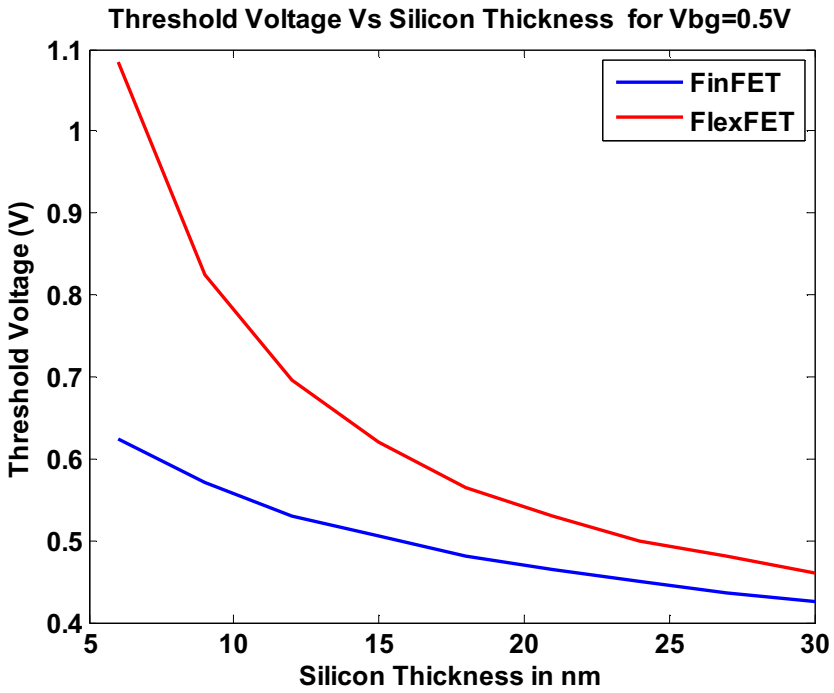

Figure 4.30. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0.5 Midgap (TG) – P+ (BG)

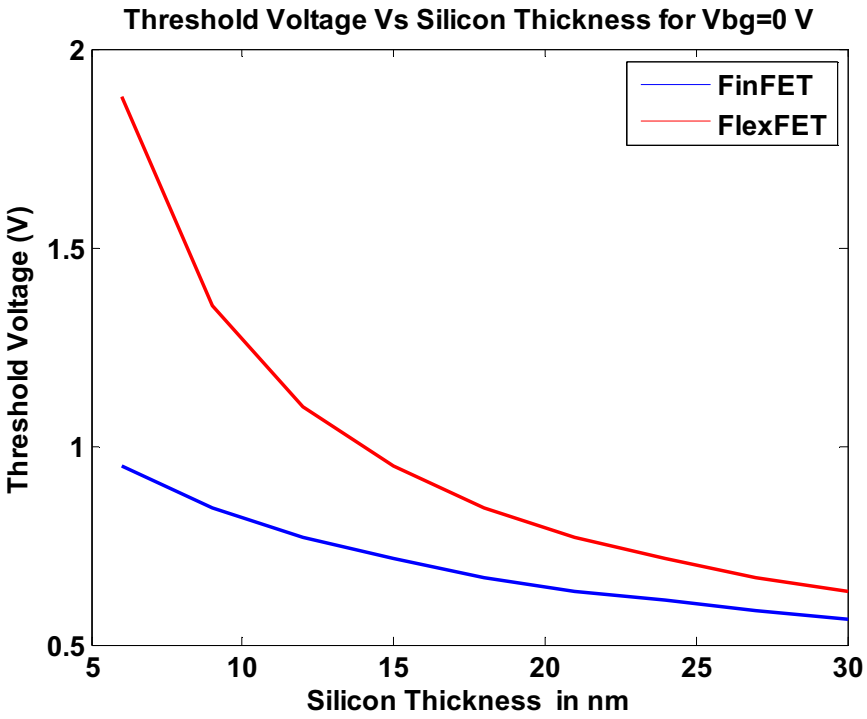

Figure 4.31. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0V Midgap (TG) – P+ (BG)

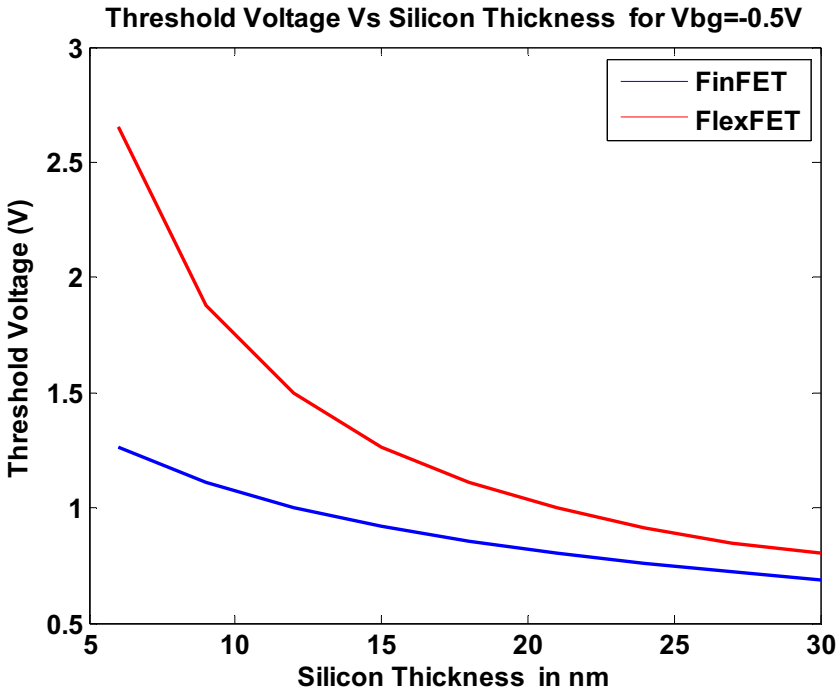

Figure 4.32. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=-0.5 Midgap (TG) – P+ (BG)

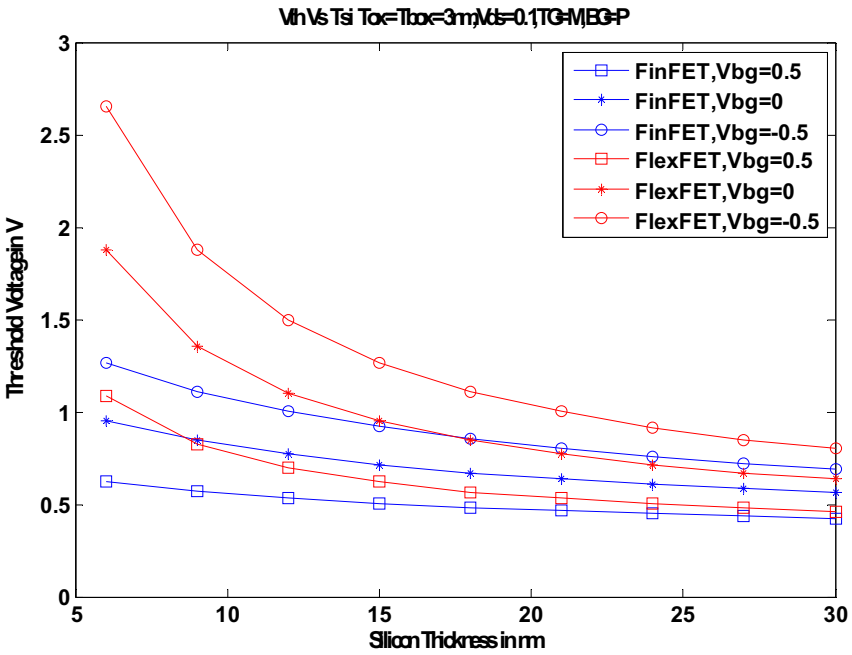

Figure 4.33. Variation of Threshold Voltage with Change in Silicon Film Thickness Midgap (TG) – P+ (BG)

Table 4.13. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg - Midgap (TG) – P+ (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	0.625	0.95	1.265	1.085	1.88	2.655
9	0.57	0.845	1.11	0.825	1.355	1.88
12	0.53	0.77	1	0.695	1.1	1.495
15	0.505	0.715	0.92	0.62	0.95	1.265
18	0.48	0.67	0.855	0.565	0.845	1.11
21	0.465	0.635	0.8	0.53	0.77	1
24	0.45	0.61	0.76	0.5	0.715	0.915
27	0.435	0.585	0.72	0.48	0.67	0.85
30	0.425	0.565	0.69	0.46	0.635	0.8

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.34 and the data are in Table 4.14. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So even with silicon film thickness variation only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in the case of Midgap (TG) - P+(BG). IDG-FlexFET with Midgap (Top gate) and Midgap (Bottom gate) meets both the threshold voltage and dynamic threshold control factor criteria.

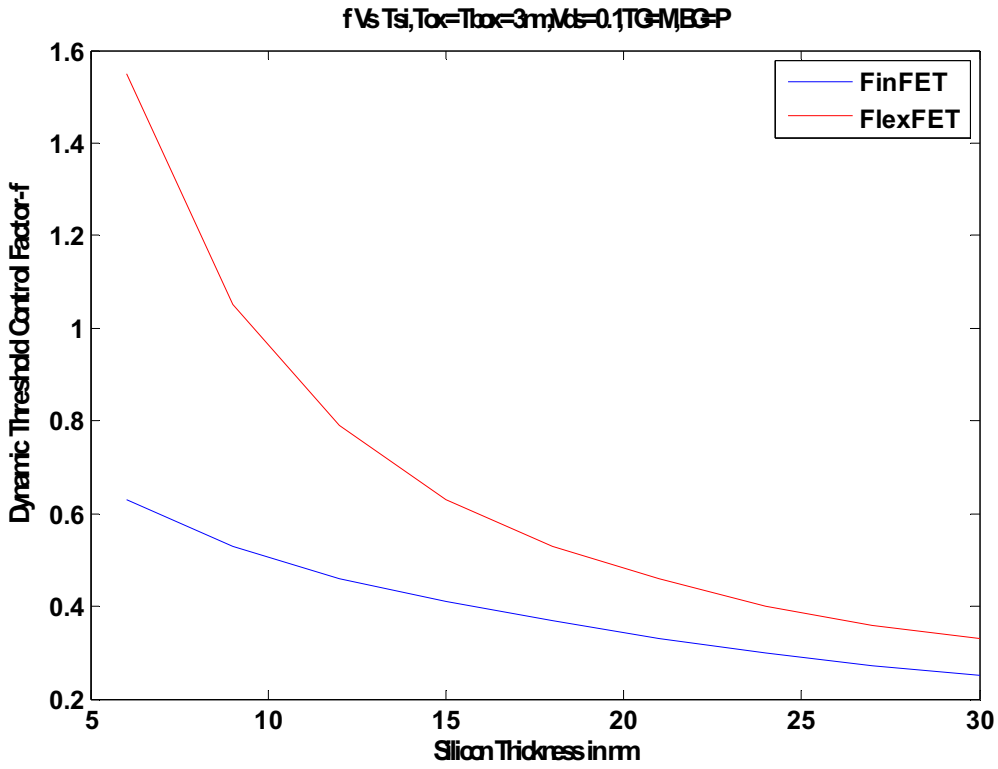

Figure 4.34. Variation of Dynamic Control Factor with Change in Silicon Film Thickness Midgap (TG) – P+ (BG)

Table 4.14. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness - Midgap (TG) – P+ (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.65	1.59
9	0.55	1.06
12	0.48	0.81
15	0.42	0.66
18	0.38	0.56
21	0.34	0.48
24	0.32	0.43
27	0.3	0.38
30	0.28	0.35

4.4.2.2. P+ (top gate) – Midgap (bottom gate). Here the top gate is set to 5.1eV and the bottom gate is set to 4.55eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.35, Figure 4.36, and Figure 4.37, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.38. Table 4.15 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET that the threshold voltage in case of all three back gate voltages is too high and definitely out of the required range of 0V to 1V.

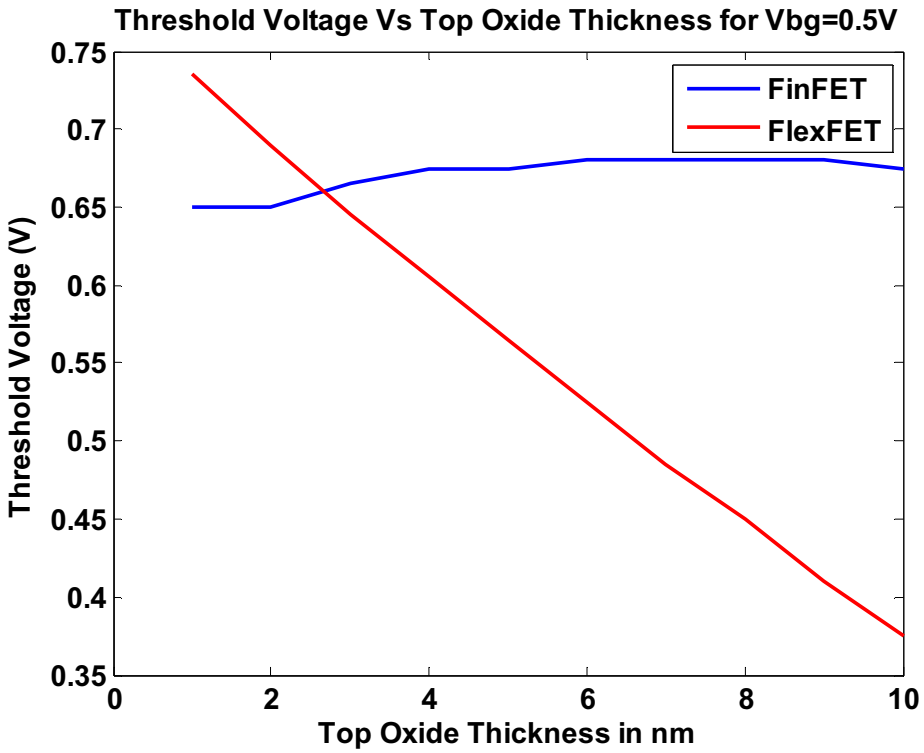

Figure 4.35. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V for P+ (TG)- Midgap (BG)

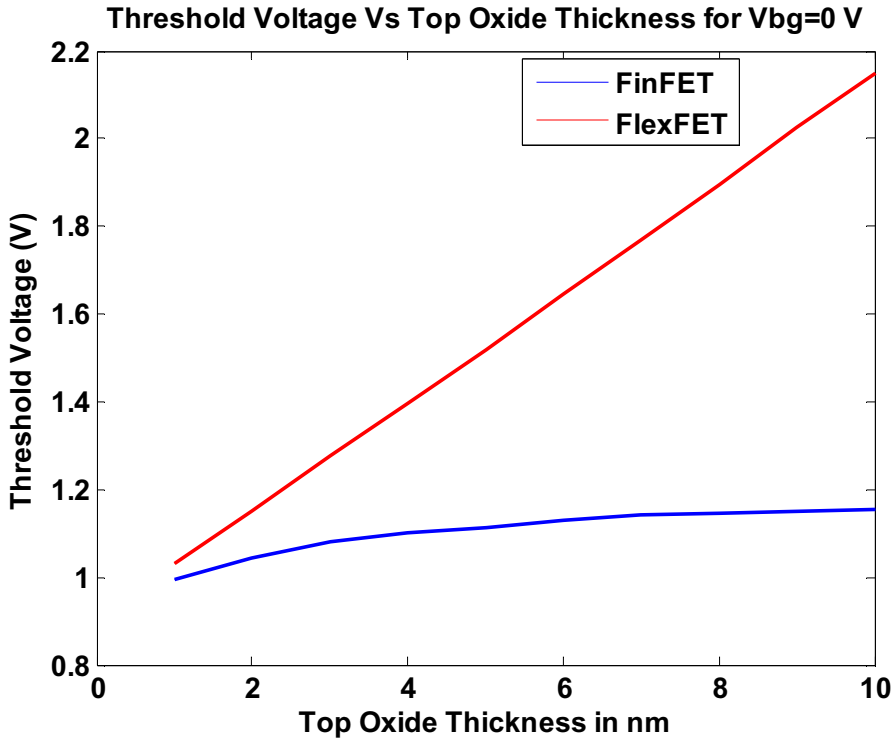

Figure 4.36. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0V for P+ (TG)- Midgap (BG)

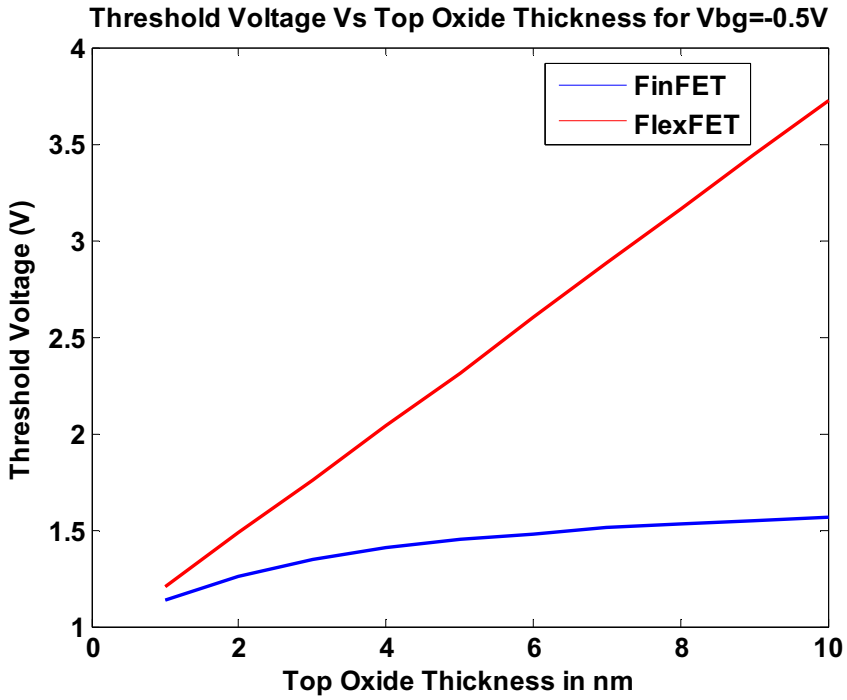

Figure 4.37. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5V for P+ (TG)- Midgap (BG)

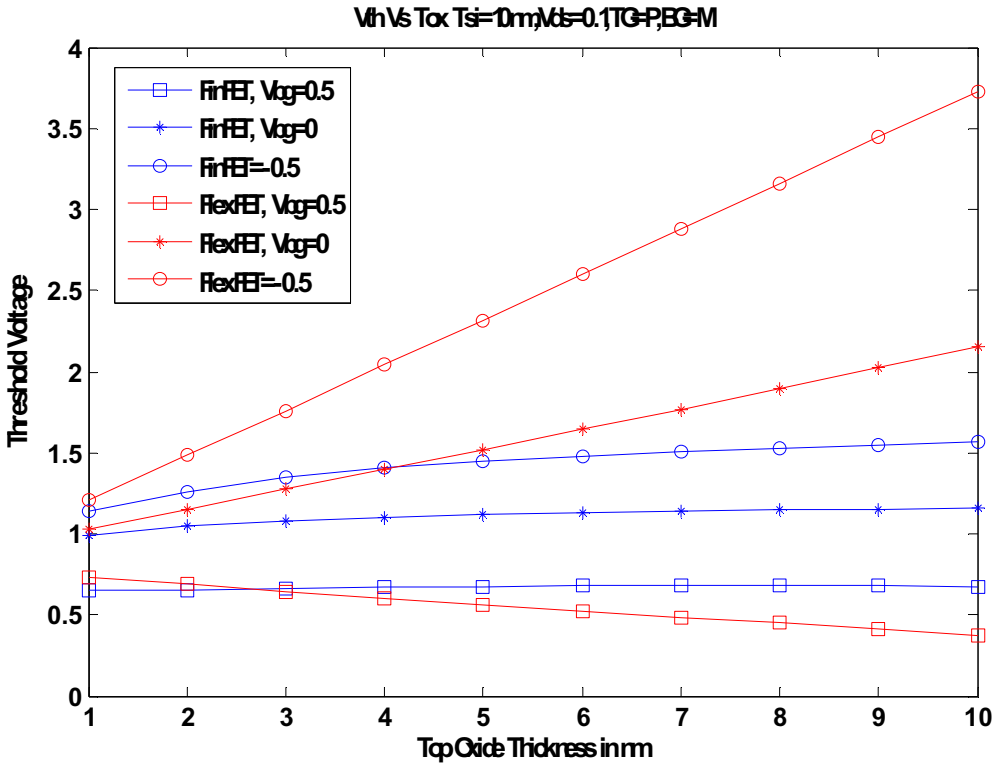

Figure 4.38. Variation of Threshold Voltage with Change in Top Oxide Thickness for P+ (TG)- Midgap (BG)

Table 4.15. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg – P+ (TG)- Midgap (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	0.65	0.995	1.135	0.735	1.03	1.21
2	0.65	1.045	1.26	0.69	1.15	1.485
3	0.665	1.08	1.345	0.645	1.275	1.76
4	0.675	1.1	1.405	0.605	1.395	2.04
5	0.675	1.115	1.45	0.565	1.52	2.315
6	0.68	1.13	1.48	0.525	1.645	2.6
7	0.68	1.14	1.51	0.485	1.77	2.88
8	0.68	1.145	1.53	0.45	1.895	3.16
9	0.68	1.15	1.55	0.41	2.025	3.445
10	0.675	1.155	1.565	0.375	2.15	3.725

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.39 and the data are in Table 4.16. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness; whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

However both the devices did not meet the threshold voltage criterion for top oxide thickness variation in the case of P+(TG)- Midgap (BG).

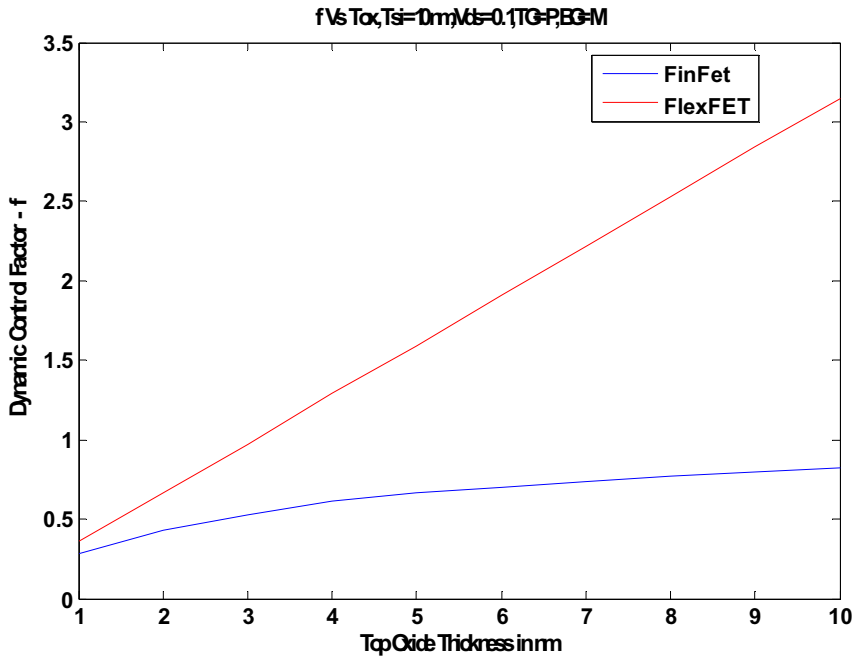

Figure 4.39. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness P+ (TG) - Midgap (BG)

Table 4.16. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness- P+ (TG) - Midgap (BG)

TOX in nm	FinFET f	FlexFET f
1	0.69	0.59
2	0.79	0.92
3	0.83	1.26
4	0.85	1.58
5	0.88	1.91
6	0.9	2.24
7	0.92	2.57
8	0.93	2.89
9	0.94	3.23
10	0.96	3.55

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.40, Figure 4.41, and Figure 4.42, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.43. Table 4.17 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET that the threshold voltage in case of all three back gate voltages is out of the required range of 0V to 1V in case of P+ (TG)- Midgap (BG)

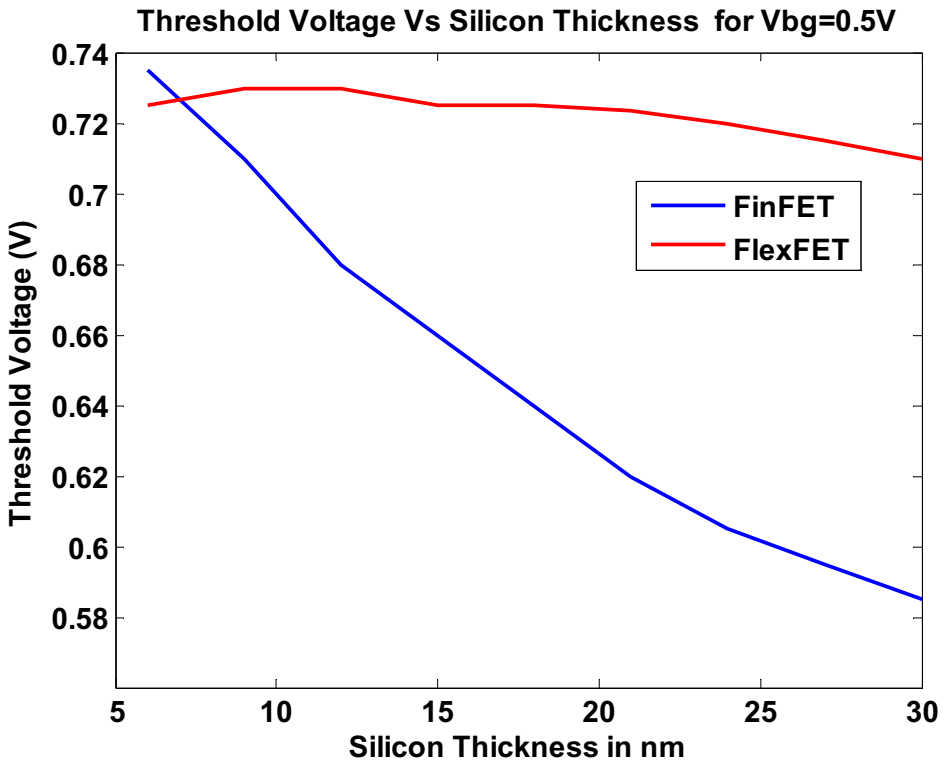

Figure 4.40. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0.5 P+ (TG) - Midgap (BG)

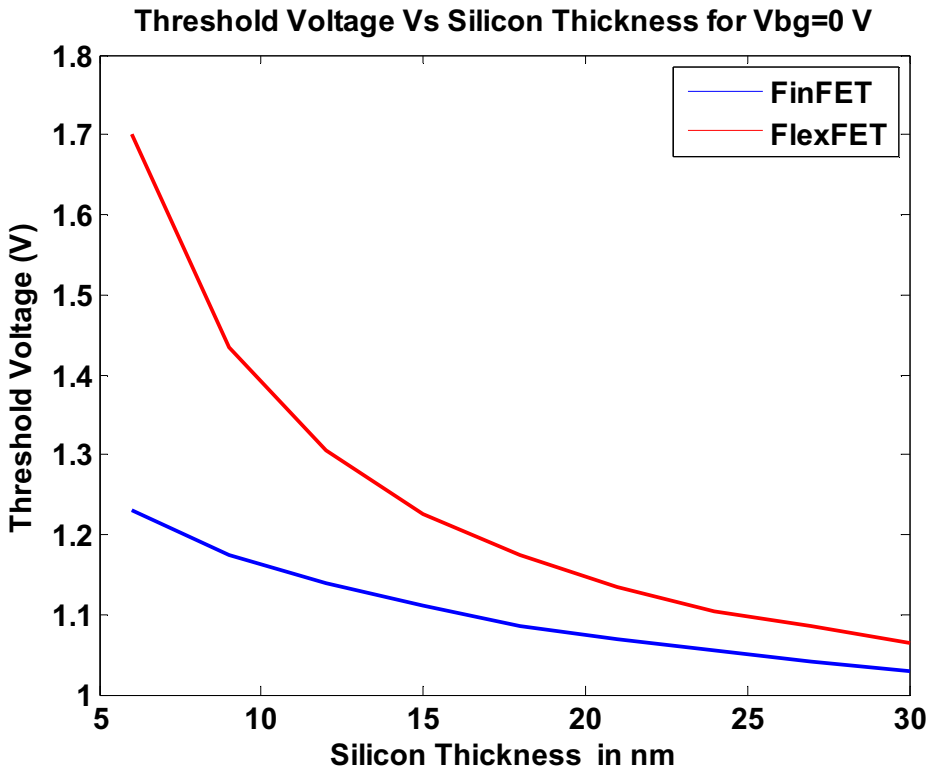

Figure 4.41. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0V P+ (TG) - Midgap (BG)

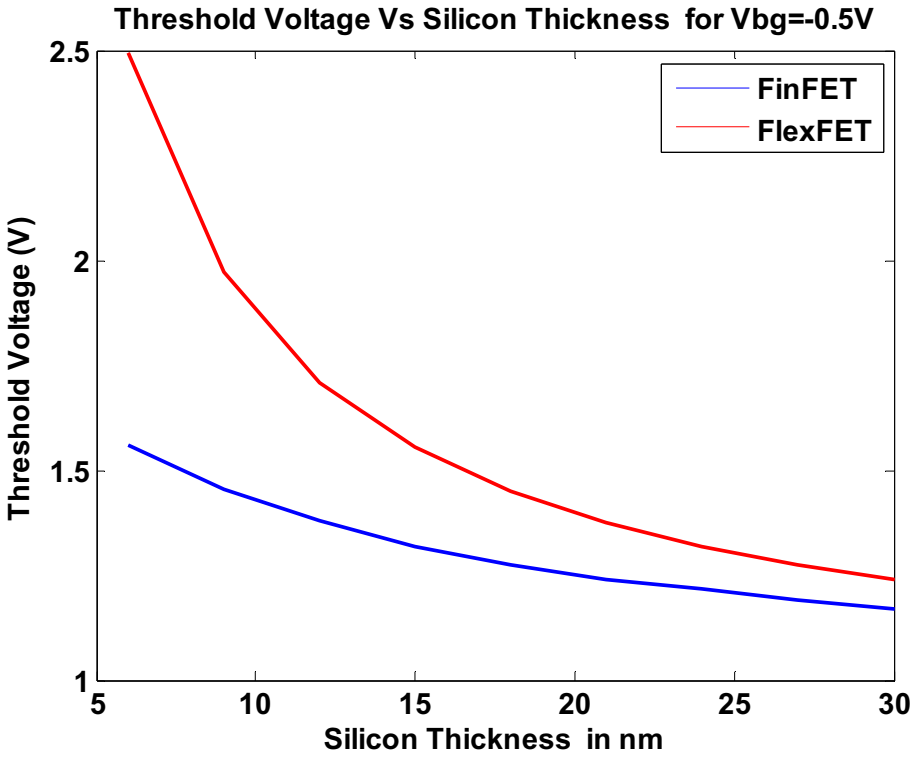

Figure 4.42. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=-0.5 P+ (TG) - Midgap (BG)

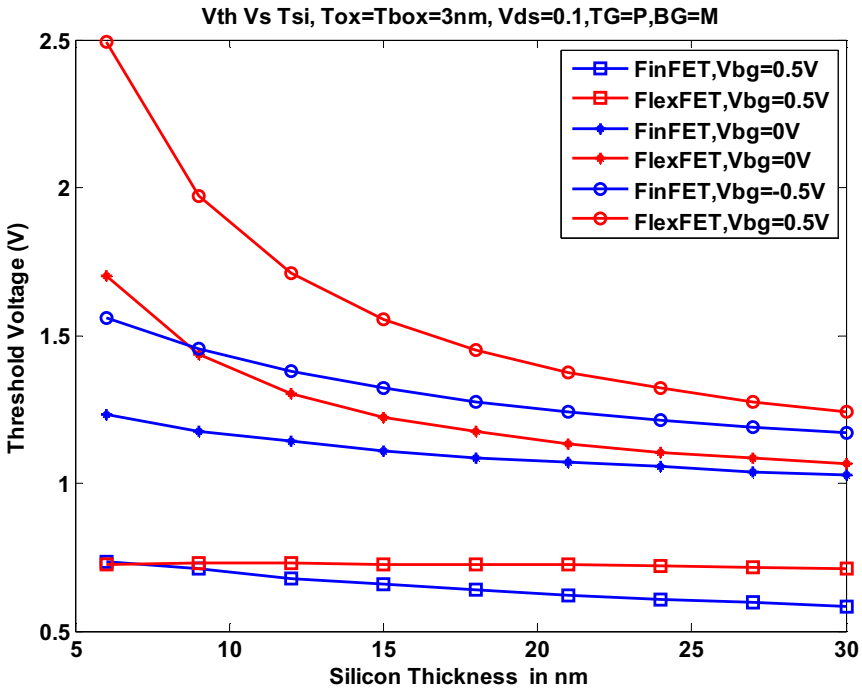

Figure 4.43. Variation of Threshold Voltage with Change in Silicon Film Thickness P+ (TG) - Midgap (BG)

Table 4.17. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg - P+ (TG) - Midgap (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	0.735	1.23	1.56	0.725	1.7	2.495
9	0.71	1.175	1.455	0.73	1.435	1.97
12	0.68	1.14	1.38	0.73	1.305	1.71
15	0.66	1.11	1.32	0.725	1.225	1.555
18	0.64	1.085	1.275	0.725	1.175	1.45
21	0.62	1.07	1.24	0.975	1.135	1.375
24	0.605	1.055	1.215	0.72	1.105	1.32
27	0.595	1.04	1.19	0.715	1.085	1.275
30	0.585	1.03	1.17	0.71	1.065	1.24

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.44 and the data are in Table 4.18. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So with silicon film thickness variation neither IDG-FinFET nor IDG-FlexFET meet the required criteria of threshold voltage and only IDG-FlexFET meets the dynamic control factor in case of P+(TG) - Midgap (BG).

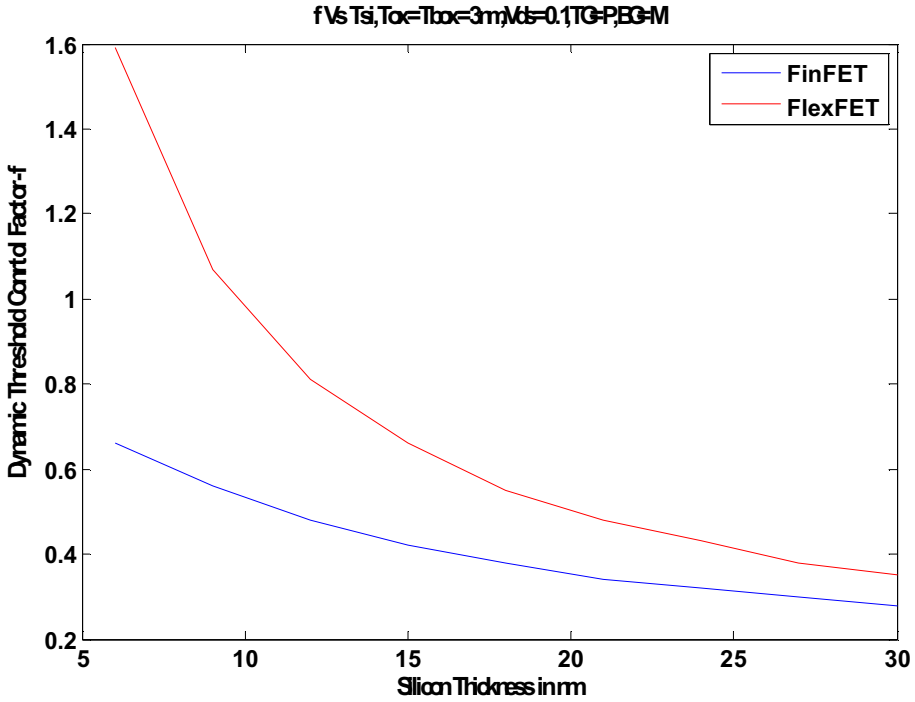

Figure 4.44. Variation of Dynamic Control Factor with Change in Silicon Film Thickness P+ (TG) - Midgap (BG)

Table 4.18. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness - P+ (TG) - Midgap (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.66	1.59
9	0.56	1.07
12	0.48	0.81
15	0.42	0.66
18	0.38	0.55
21	0.34	0.48
24	0.32	0.43
27	0.3	0.38
30	0.28	0.35

4.4.2.3. N+ (top gate) – Midgap (bottom gate). Here the top gate is set to 4.0eV and the bottom gate is set to 4.55eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.45, Figure 4.46, and Figure 4.47, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.48. Table 4.19 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET the threshold voltage for all three back gate voltages are very low and is definitely out of the required range of 0V to 1V.

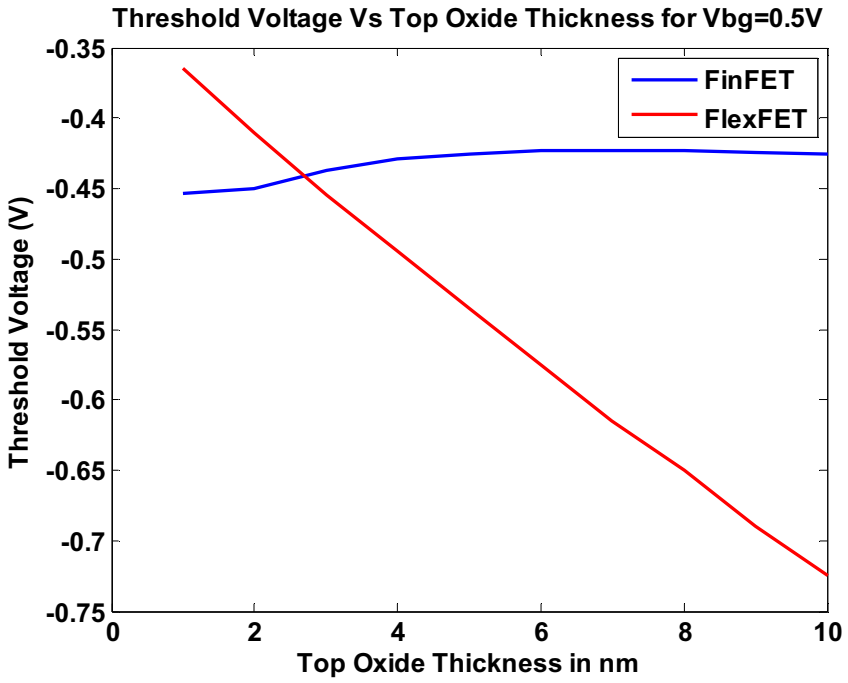

Figure 4.45. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V for N+ (TG)- Midgap (BG)

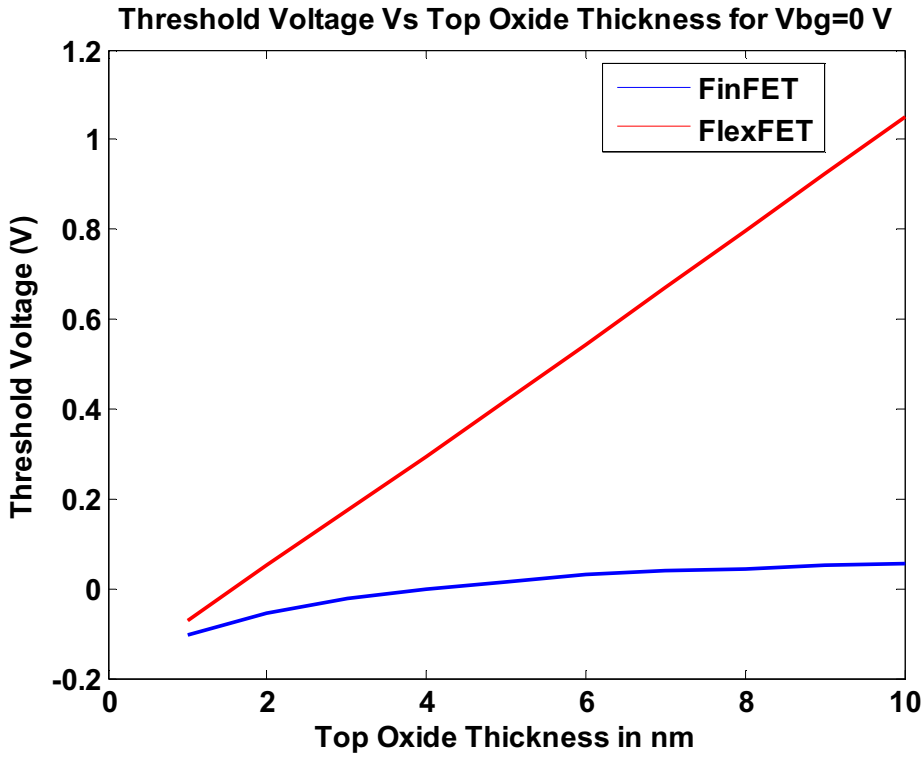

Figure 4.46. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0V for N+ (TG)- Midgap (BG)

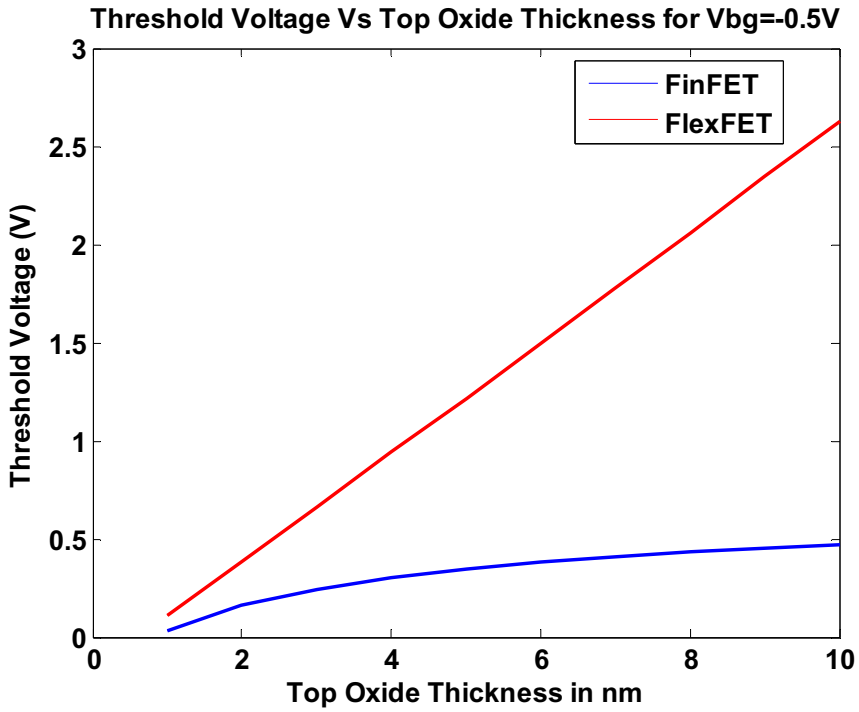

Figure 4.47. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5V for N+ (TG)- Midgap (BG)

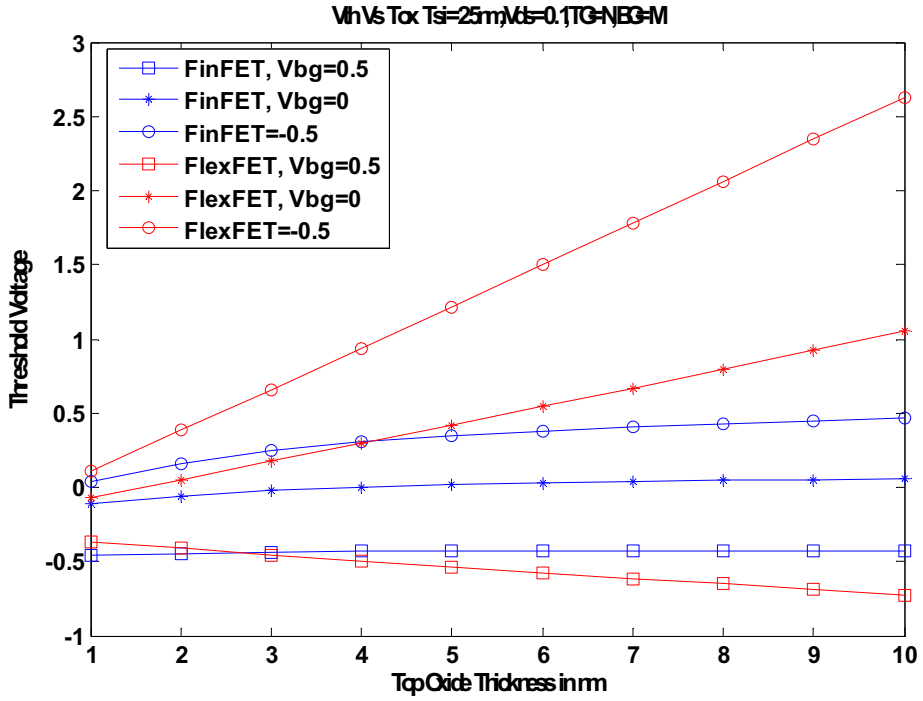

Figure 4.48. Variation of Threshold Voltage with Change in Top Oxide Thickness for N+ (TG)- Midgap (BG)

Table 4.19. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg – N+ (TG)- Midgap (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	-0.454	-0.105	0.035	-0.365	-0.07	0.11
2	-0.45	-0.055	0.16	-0.41	0.05	0.385
3	-0.437	-0.02	0.245	-0.455	0.175	0.66
4	-0.4295	8.21E-16	0.305	-0.495	0.295	0.94
5	-0.4255	0.015	0.35	-0.535	0.42	1.215
6	-0.4235	0.03	0.38	-0.575	0.545	1.5
7	-0.423	0.04	0.41	-0.615	0.67	1.78
8	-0.4235	0.045	0.43	-0.65	0.795	2.06
9	-0.424	0.05	0.45	-0.69	0.925	2.345
10	-0.425	0.055	0.465	-0.725	1.05	2.625

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.49 and the data are in Table 4.20. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness; whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

However both the devices did not meet the threshold voltage criterion for top oxide thickness variation in case of N+ (TG)- Midgap (BG).

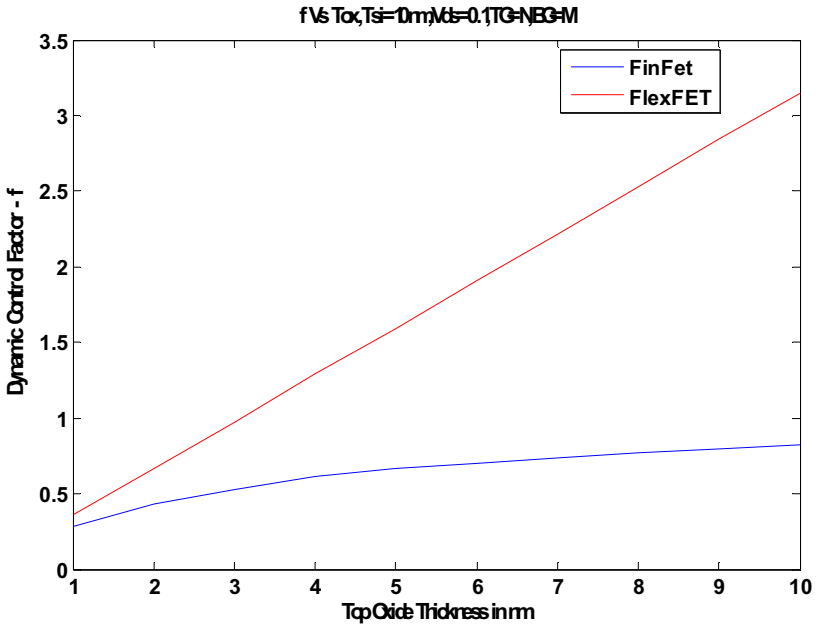

Figure 4.49. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness N+ (TG) - Midgap (BG)

Table 4.20. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness- N+ (TG) - Midgap (BG)

TOX in nm	FinFET f	FlexFET f
1	0.698	0.59
2	0.79	0.92
3	0.834	1.26
4	0.859	1.58
5	0.881	1.91
6	0.907	2.24
7	0.926	2.57
8	0.937	2.89
9	0.948	3.23
10	0.96	3.55

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.50, Figure 4.51, and Figure 4.52, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.53. Table 4.21 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET and IDG-FlexFET that the threshold voltage in case of all three back gate voltages is very low and is out of the required range of 0V to 1V in case of N+ (TG) – Midgap (BG).

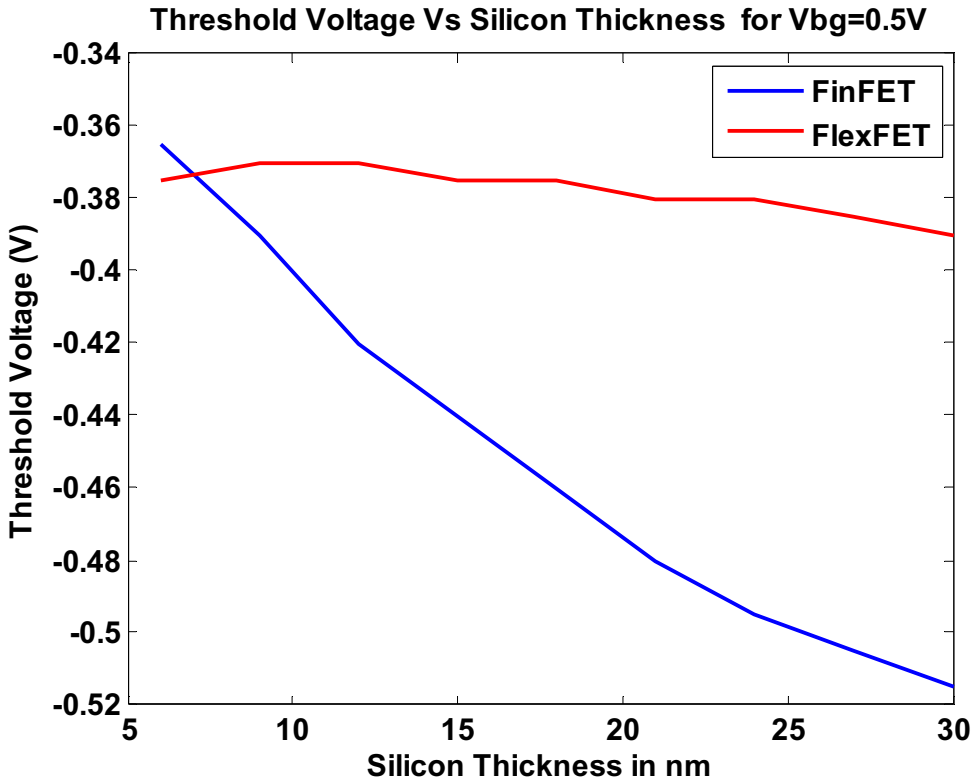

Figure 4.50. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0.5 V N+ (TG) - Midgap (BG)

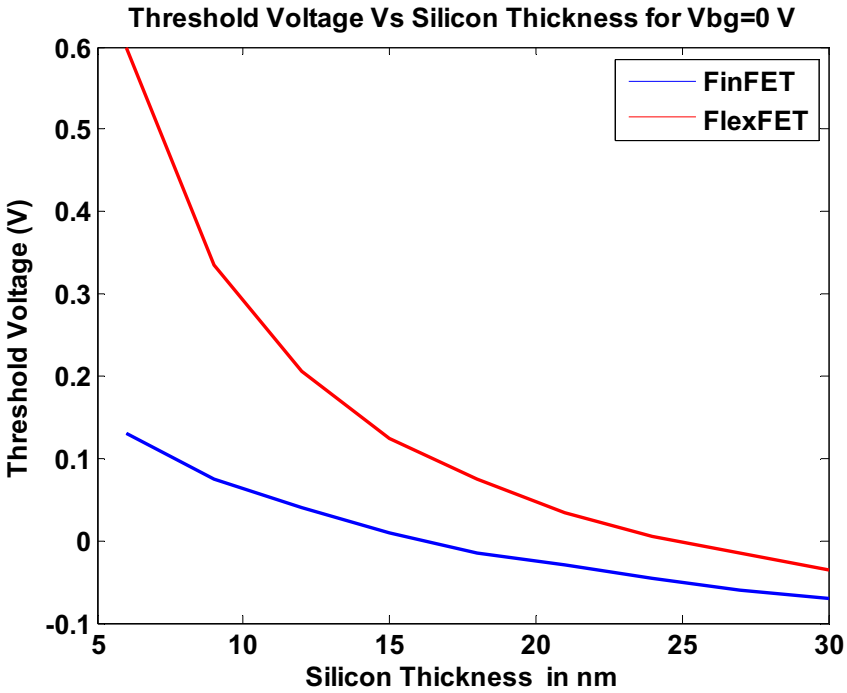

Figure 4.51. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0V N+ (TG) - Midgap (BG)

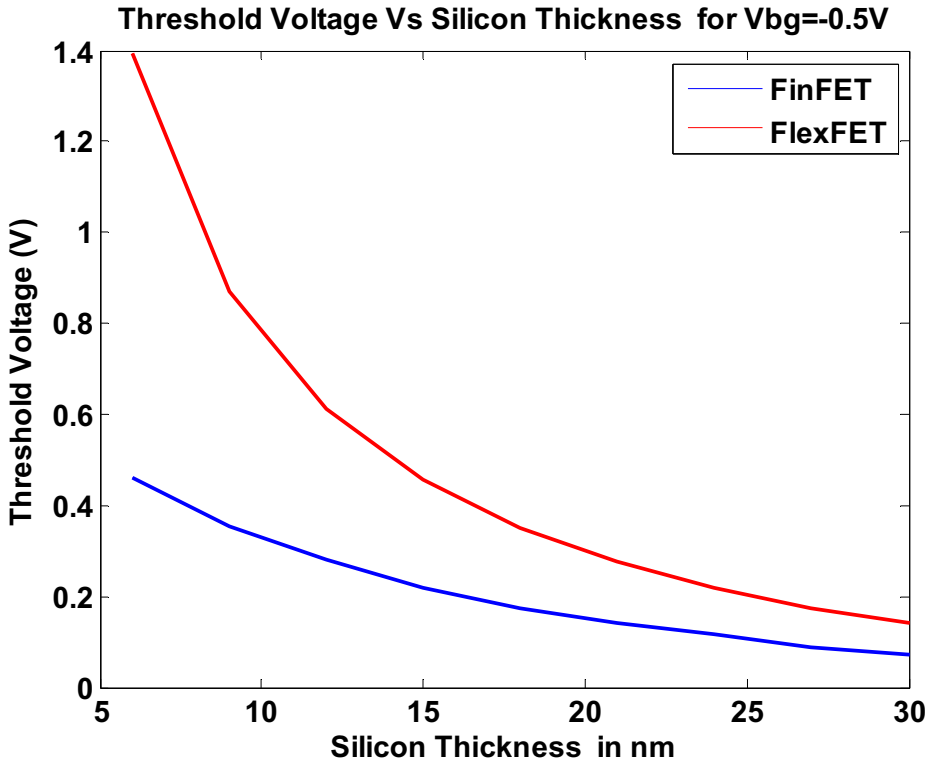

Figure 4.52. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=-0.5 V N+ (TG) - Midgap (BG)

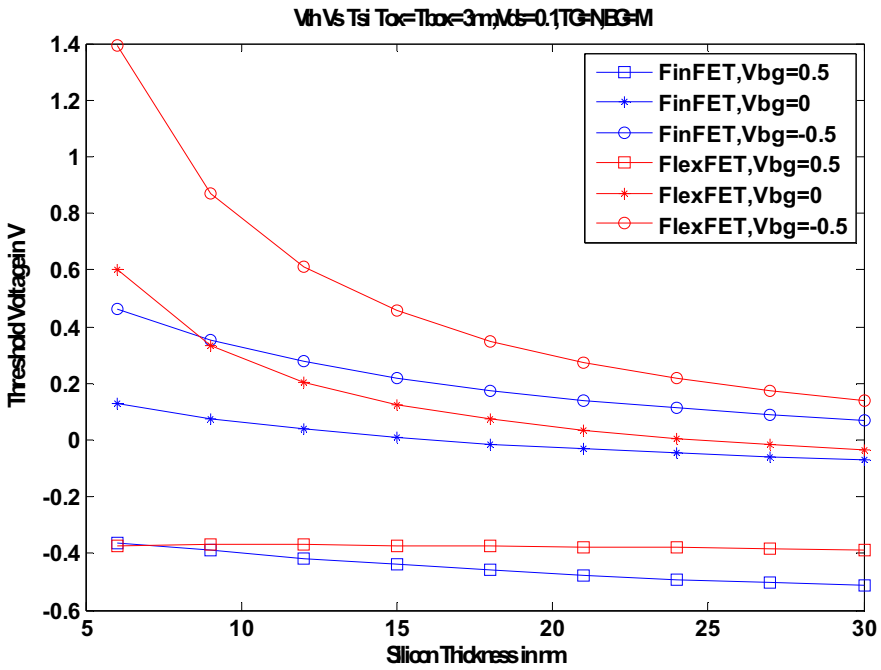

Figure 4.53. Variation of Threshold Voltage with Change in Silicon Film Thickness N+ (TG) - Midgap (BG)

Table 4.21. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg - N+ (TG) - Midgap (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	-0.365	0.13	0.46	-0.375	0.6	1.395
9	-0.39	0.075	0.355	-0.37	0.335	0.87
12	-0.42	0.04	0.28	-0.37	0.205	0.61
15	-0.44	0.01	0.22	-0.375	0.125	0.455
18	-0.46	-0.015	0.175	-0.375	0.075	0.35
21	-0.48	-0.03	0.14	-0.38	0.035	0.275
24	-0.495	-0.045	0.115	-0.38	0.005	0.22
27	-0.505	-0.06	0.09	-0.385	-0.015	0.175
30	-0.515	-0.07	0.07	-0.39	-0.035	0.14

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.54 and the data are in Table 4.22. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So with silicon film thickness variation neither IDG-FinFET nor IDG-FlexFET meet the required criteria of threshold voltage and only IDG-FlexFET meets the dynamic control factor in the case of N+ (TG) – Midgap (BG).

To summarize the half-asymmetry case, the threshold voltage is <u>too high</u> in the case of P+ (TG) - Midgap (BG) and it is <u>too low</u> in the case of N+ (TG) – Midgap (BG), for both FinFET and FlexFET designs. The case with Midgap (TG) - P+ (BG) work functions has a moderate dynamic control factor ranging in comparison with the symmetrical case for both designs. The threshold voltage in case of Midgap (TG) - P+ (BG), is in the required range. This is the actually fabricated FlexFET by American Semiconductor, Inc.

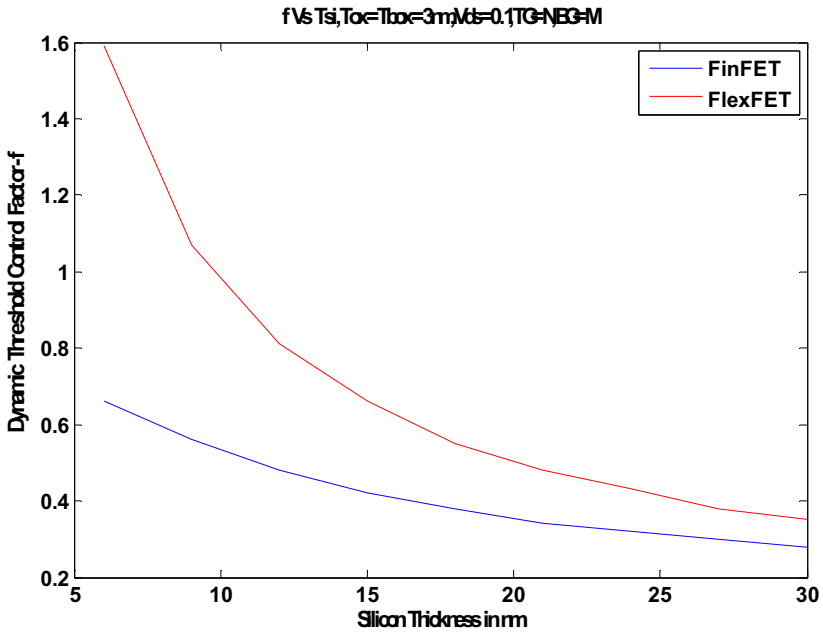

Figure 4.54. Variation of Dynamic Control Factor with Change in Silicon Film Thickness N+ (TG) - Midgap (BG)

Table 4.22. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness - N+ (TG) - Midgap (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.66	1.59
9	0.56	1.07
12	0.48	0.81
15	0.42	0.66
18	0.38	0.55
21	0.34	0.48
24	0.32	0.43
27	0.3	0.38
30	0.28	0.35

4.4.3. Full-Asymmetry

Here the top and bottom gates are 1.1eV apart from each other for both IDG FinFET and IDG FlexFET. The results under under this category would be presented in this section.

4.4.3.1. N+ (top gate) – P+ (bottom gate). Here the top gate is set to 5.1eV and the bottom gate is set to 4.0eV. The threshold voltage variation with respect to top oxide variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.55, Figure 4.56, and Figure 4.57, respectively. The consolidated view of the effect of back voltages and top oxide thickness on threshold voltage can be seen in Figure 4.58. Table 4.23 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to 1V. In case of IDG-FlexFET, the threshold voltage increases sharply with increase in top oxide thickness; however, around 3 nm of top oxide thickness it can be observed that the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

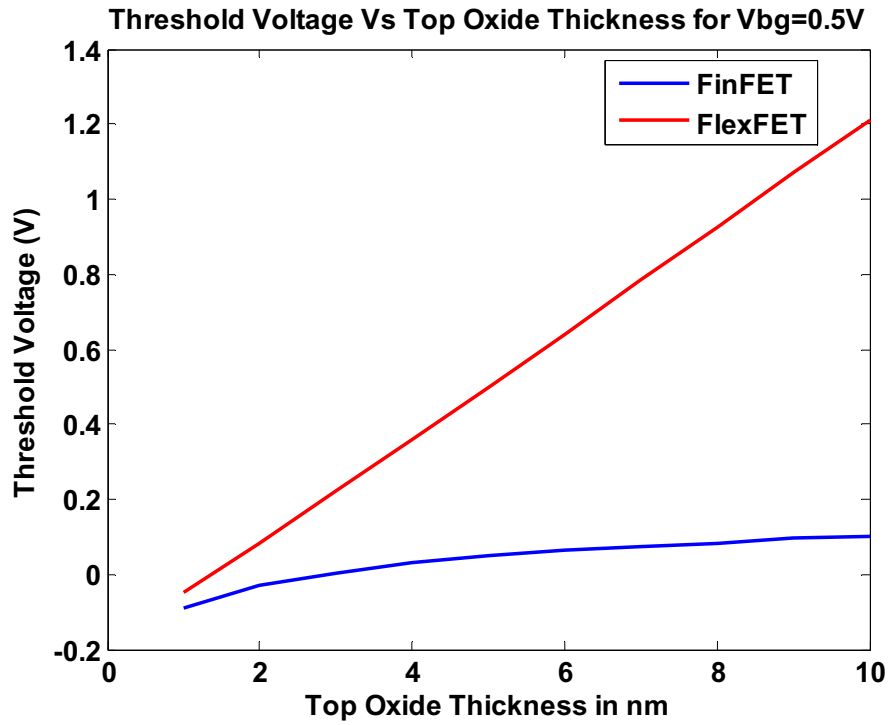

Figure 4.55. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0.5V N+(TG) – P+ (BG)

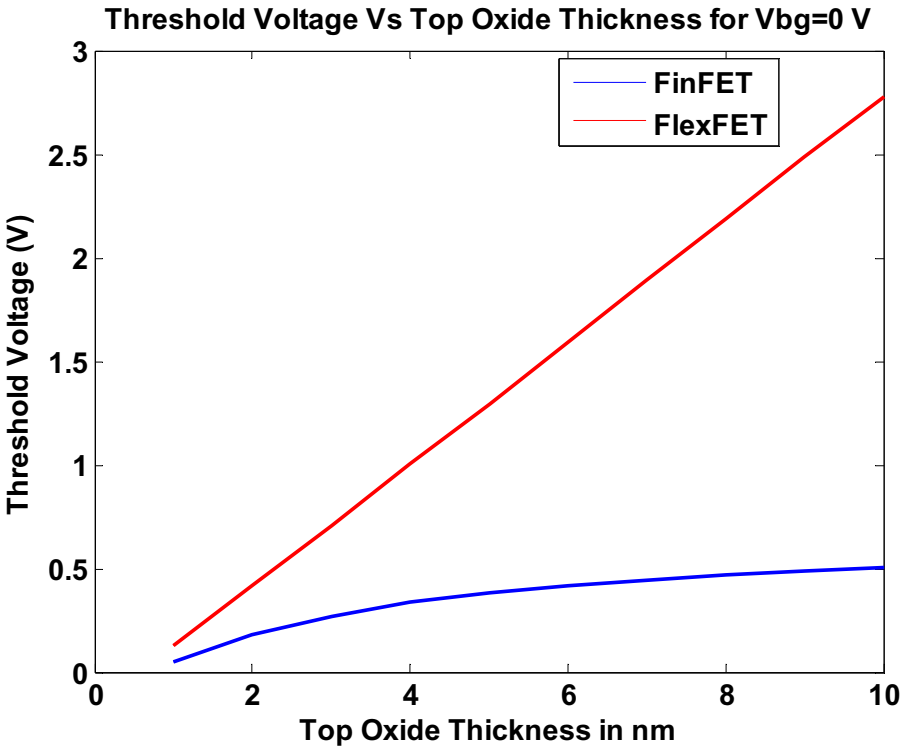

Figure 4.56. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=0V N+(TG) – P+ (BG)

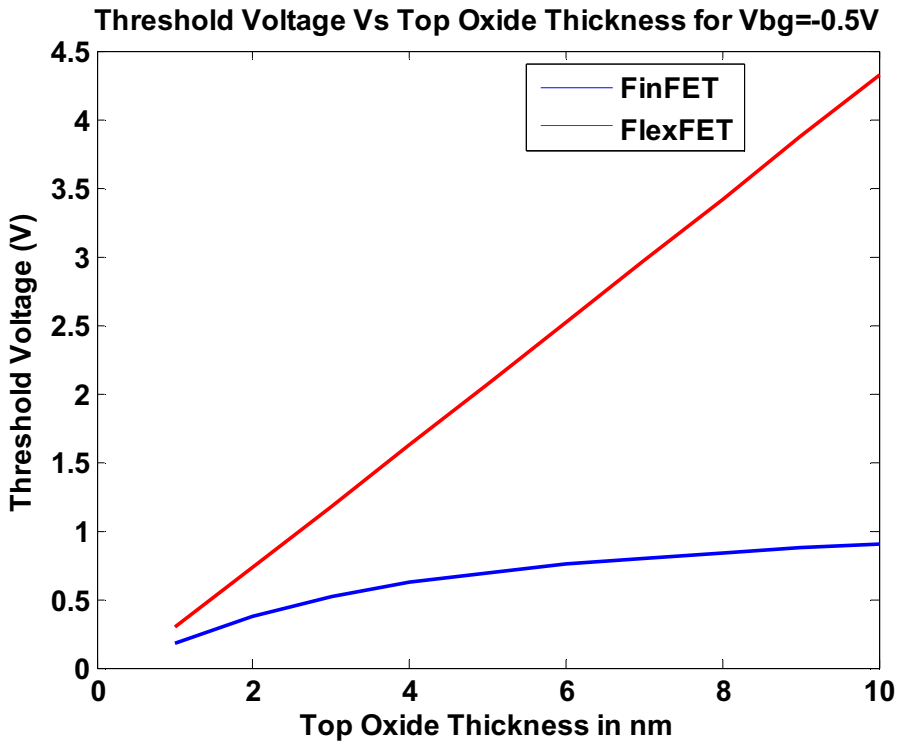

Figure 4.57. Variation of Threshold Voltage with Change in Top Oxide Thickness at Vbg=-0.5 V- N+(TG) –P+ (BG)

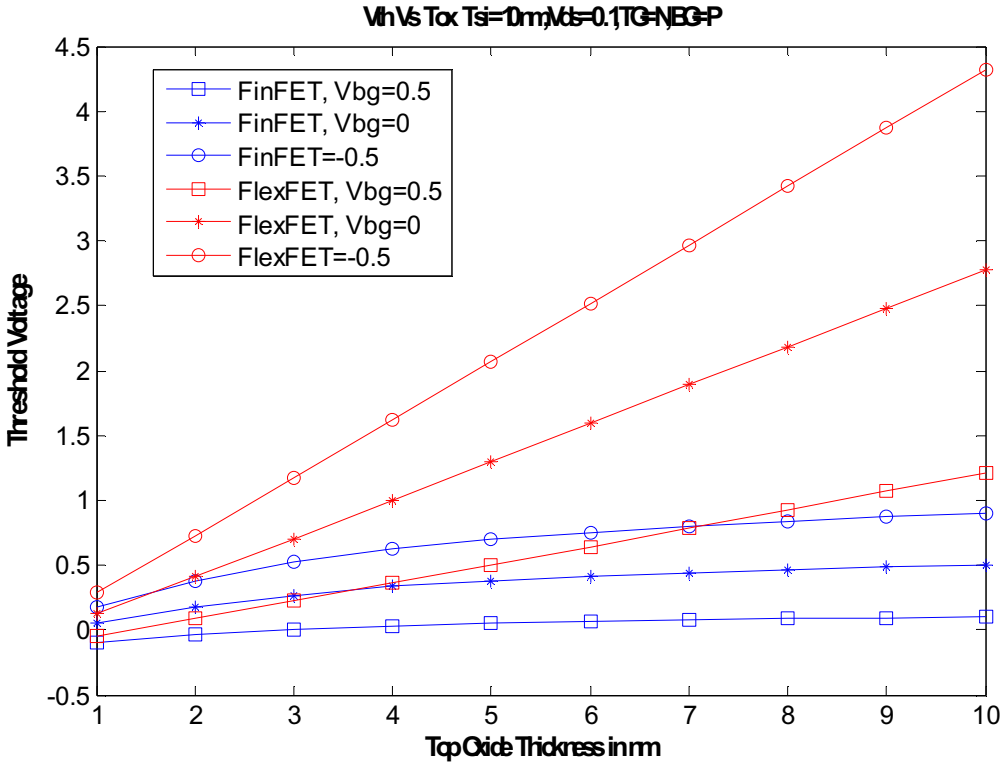

Figure 4.58. Variation of Threshold Voltage with Change in Top Oxide Thickness N+(TG) – P+ (BG)

Table 4.23. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg- N+(TG) – P+ (BG)

TOX in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
1	-0.09	0.05	0.175	-0.05	0.125	0.29
2	-0.03	0.18	0.38	0.085	0.415	0.73
3	0.005	0.27	0.52	0.225	0.705	1.175
4	0.03	0.335	0.62	0.36	1	1.625
5	0.05	0.38	0.695	0.5	1.295	2.07
6	0.065	0.415	0.755	0.64	1.59	2.52
7	0.075	0.445	0.8	0.785	1.89	2.97
8	0.085	0.47	0.84	0.925	2.185	3.42
9	0.095	0.485	0.87	1.07	2.485	3.87
10	0.1	0.505	0.895	1.21	2.78	4.32

The dynamic threshold control factor variation with top oxide thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.59 and the data are in Table 4.24. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of top oxide thickness; whereas, in case of IDG-FlexFET the dynamic control factor is way above for most values of top oxide thickness.

So as far as top oxide thickness variation is concerned only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in the case of N+ (TG) - P+ (BG).

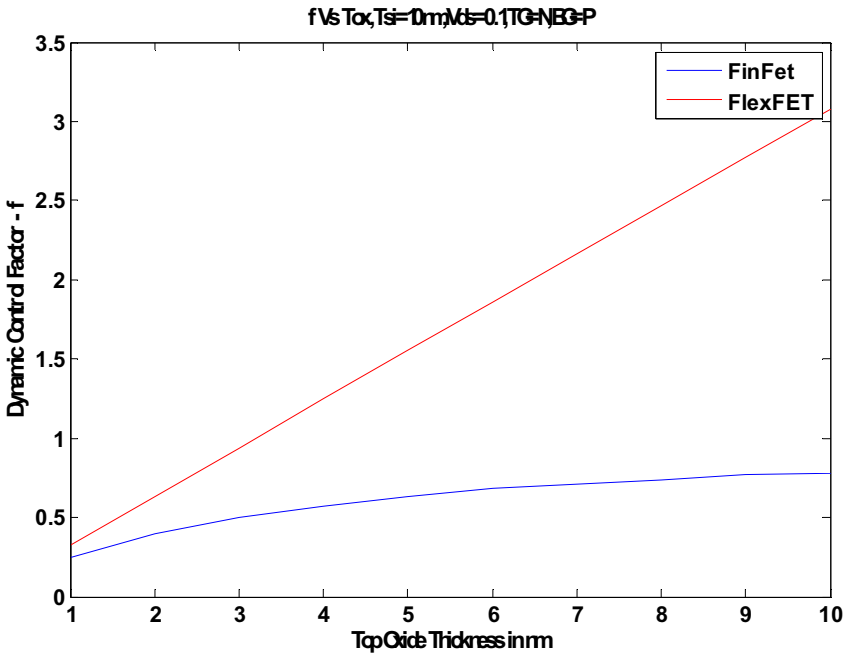

Figure 4.59. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness N+(TG) – P+ (BG)

Table 4.24. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Top Oxide Thickness -- N+(TG) – P+ (BG)

TOX in nm	FinFET f	FlexFET f
1	0.25	0.33
2	0.4	0.63
3	0.5	0.94
4	0.57	1.25
5	0.63	1.55
6	0.68	1.86
7	0.71	2.16
8	0.74	2.47
9	0.77	2.77
10	0.78	3.08

The threshold voltage variation with respect to silicon film thickness variation is presented for back gate voltages of 0.5V, 0V, and -0.5V in Figure 4.60, Figure 4.61, and Figure 4.62, respectively. The consolidated view of the effect of back voltages and silicon film thickness on threshold voltage can be seen in Figure 4.63. Table 4.25 gives the data used to generate these graphs.

It can be seen from these sets of graphs that in case of IDG-FinFET the threshold voltage in case of all three back gate voltages is well within the required range of 0V to 1V. In case of IDG-FlexFET, the threshold voltage decreases with increase in silicon film thickness; the threshold voltage varies from almost 0V at 0.5V of Vbg to around 1V at -0.5V of Vbg, which is one of the required criterions.

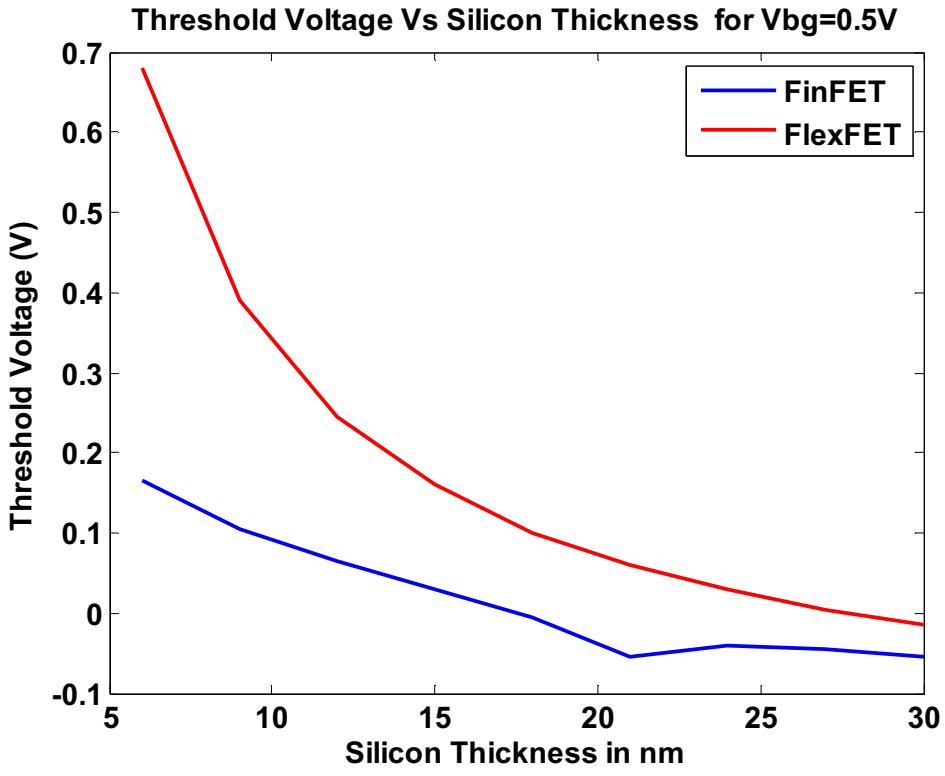

Figure 4.60. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0.5 V N+(TG) – P+ (BG)

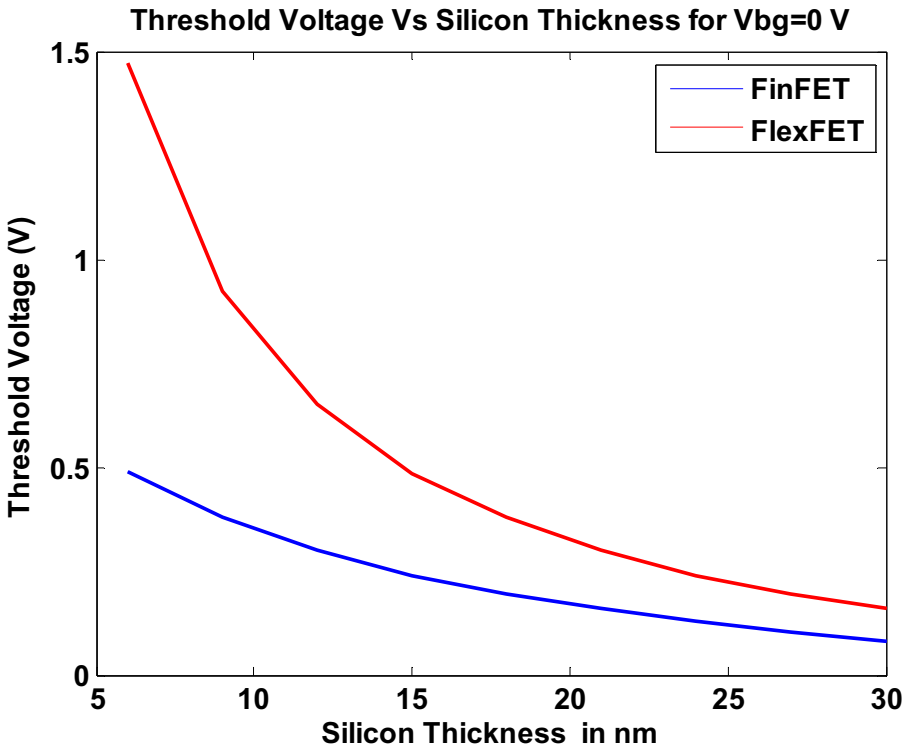

Figure 4.61. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=0 V- N+(TG) – P+ (BG)

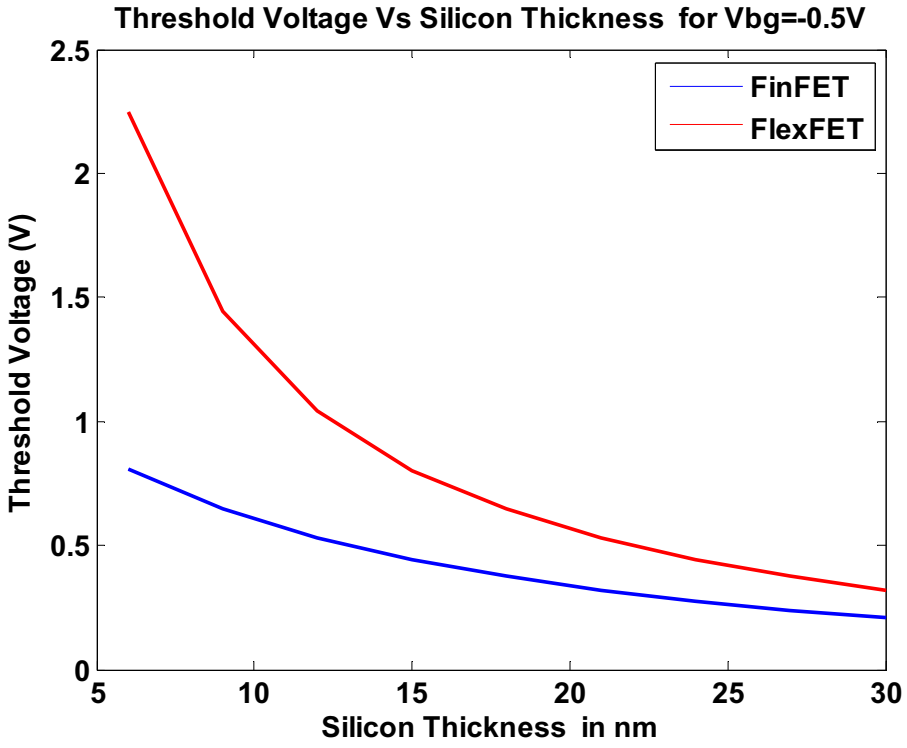

Figure 4.62. Variation of Threshold Voltage with Change in Silicon Film Thickness at Vbg=-0.5 V- N+(TG) – P+ (BG)

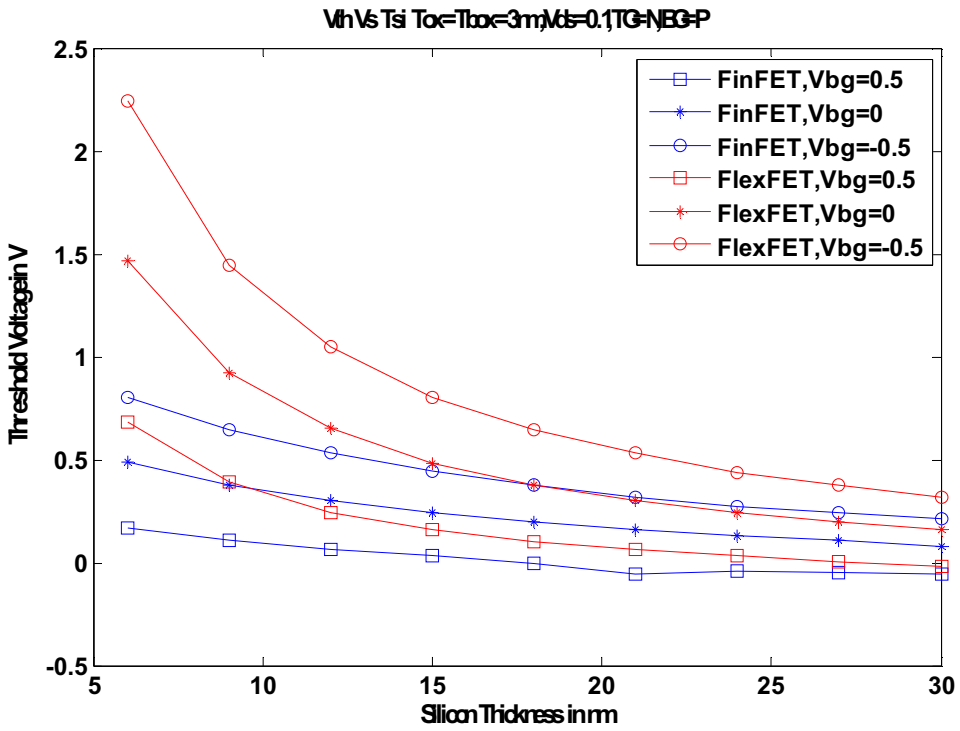

Figure 4.63. Variation of Threshold Voltage with Change in Silicon Film Thickness N+(TG) – P+ (BG)

Table 4.25. Variation of Threshold Voltage and in IDG FinFET and IDG FlexFET for different values of Silicon Film Thickness and different values of Vbg- N+(TG) – P+ (BG)

Tsi in nm	FinFET Vbg=0.5V	FinFET Vbg=0V	FinFET Vbg=-0.5V	FlexFET Vbg=0.5V	FlexFET Vbg=0V	FlexFET Vbg=-0.5V
6	0.16	0.49	0.80	0.68	1.47	2.24
9	0.10	0.38	0.64	0.39	0.92	1.44
12	0.06	0.3	0.53	0.24	0.65	1.04
15	0.03	0.24	0.44	0.16	0.48	0.8
18	-0.005	0.195	0.37	0.1	0.38	0.64
21	-0.05	0.16	0.32	0.06	0.3	0.53
24	-0.04	0.13	0.27	0.03	0.24	0.44
27	-0.04	0.105	0.24	0.005	0.19	0.37
30	-0.05	0.08	0.21	-0.02	0.16	0.32

The dynamic threshold control factor variation with silicon film thickness for both IDG-FinFET and IDG-FlexFET can be seen in Figure 4.64 and the data are in Table 4.26. It can be seen that in case of IDG-FinFET the dynamic control factor is less than 1 for entire range of silicon film thickness; whereas, in case of IDG-FlexFET the dynamic control factor is above for most values of silicon film thickness.

So even with silicon film thickness variation only IDG-FlexFET meets the required criteria of threshold voltage and dynamic control factor in the case of N+ (TG) - P+ (BG). IDG-FlexFET with Midgap (Top gate) and Midgap (Bottom gate) meets both the threshold voltage and dynamic threshold control factor criteria.

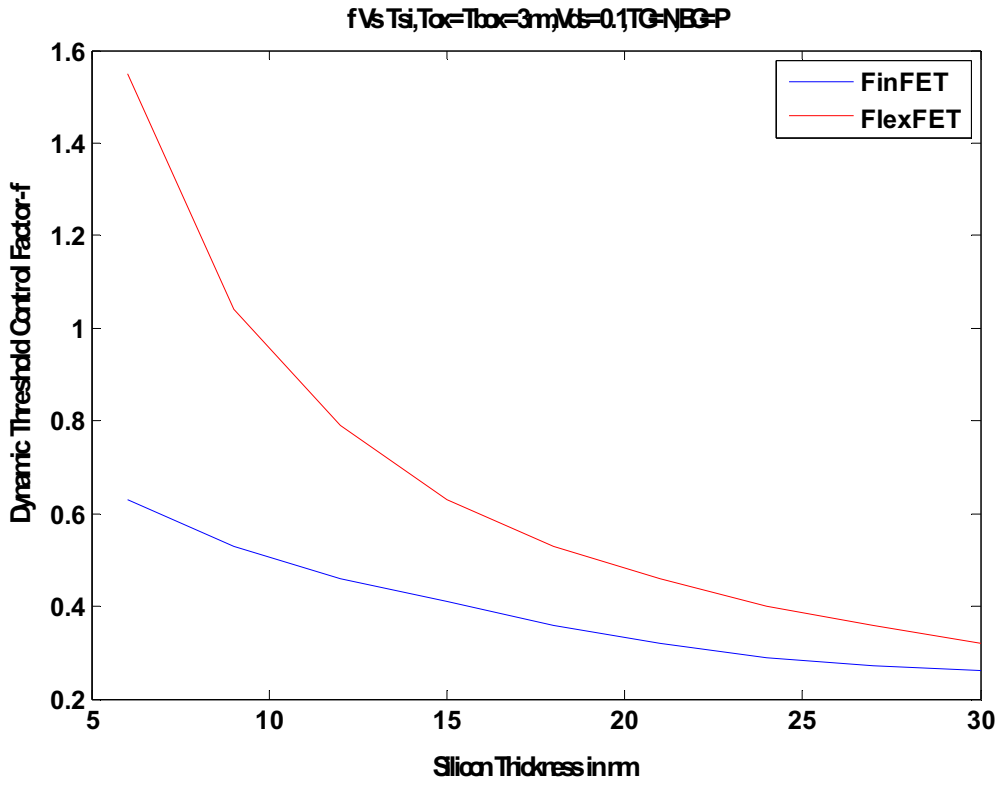

Figure 4.64. Variation of Dynamic Control Factor with Change in Silicon Film Thickness N+(TG) – P+ (BG)

Table 4.26. Dynamic Threshold Control Factor and in IDG FinFET and IDG FlexFET for variation in Silicon Film Thickness- N+(TG) – P+ (BG)

Tsi in nm	FinFET f	FlexFET f
6	0.63	1.55
9	0.53	1.04
12	0.46	0.79
15	0.41	0.63
18	0.36	0.53
21	0.32	0.46
24	0.29	0.4
27	0.27	0.36
30	0.26	0.32

With the top gate to N+ and bottom gate set to P+, this device model has full asymmetry with respect to work functions. It has a high dynamic control factor as well as a threshold voltage that is within the required range for the FlexFET design. For FinFET the threshold voltage is too low and so is the dynamic control factor.

The dynamic threshold control factor in all three categories: symmetrical, half asymmetrical, and fully asymmetrical was greater than unity for all of the FlexFET designs. This can be attributed to the inherent asymmetry in FlexFET structure, which results in stronger channel control by the bottom gate. The dynamic threshold control factor for FinFET was lower in all cases considered, but best for the fully asymmetrical N+ - P+ gate work function case. Of the FlexFET cases considered, both half and fully asymmetrical cases met the threshold criteria. In conclusion, both an asymmetrical device

structure (FlexFET) and asymmetrical top and bottom gate work functions are desirable to meet the targets for ultra low power applications.

4.5. I-V Characteristics of Half-Asymmetry and Full Asymmetry Devices

Based on the results from the previous section, it is evident that IDG-FlexFET is the better design option for ULP applications, owing to its high dynamic threshold control voltage. This can also be seen in the I-V curves for these devices. Figure 4.65 and Figure 4.66 show the drain current variations with front gate voltage for back gate voltage of -0.5 V, 0V, and 0.5 V, for both IDG-FinFET and IDG-FlexFET. These curves have been generated with an optimum top oxide thickness of 3 nm and silicon film thickness of 10 nm for the ideal half-asymmetry case of Midgap (TG) – P+ (BG) and full-asymmetry case of N+ (TG) – P+ (BG).

It can be seen from both figures that the Dynamic Threshold Control is higher for IDG-FlexFET when compared with IDG-FinFET.

Table 4.27 gives the summary of the analytical Study of IDG-FinFET and IDG-FlexFET in terms of threshold voltage and dynamic threshold control factor.

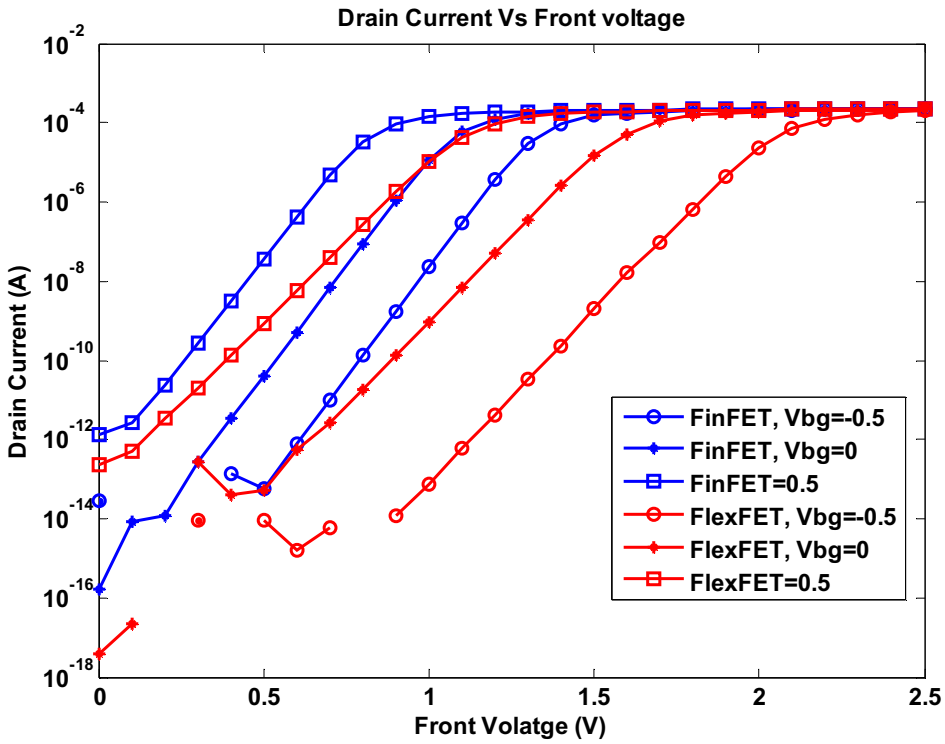

Figure 4.65. Variation of Dynamic Control Factor with Change in Silicon Film Thickness Midgap (TG) – P+ (BG)

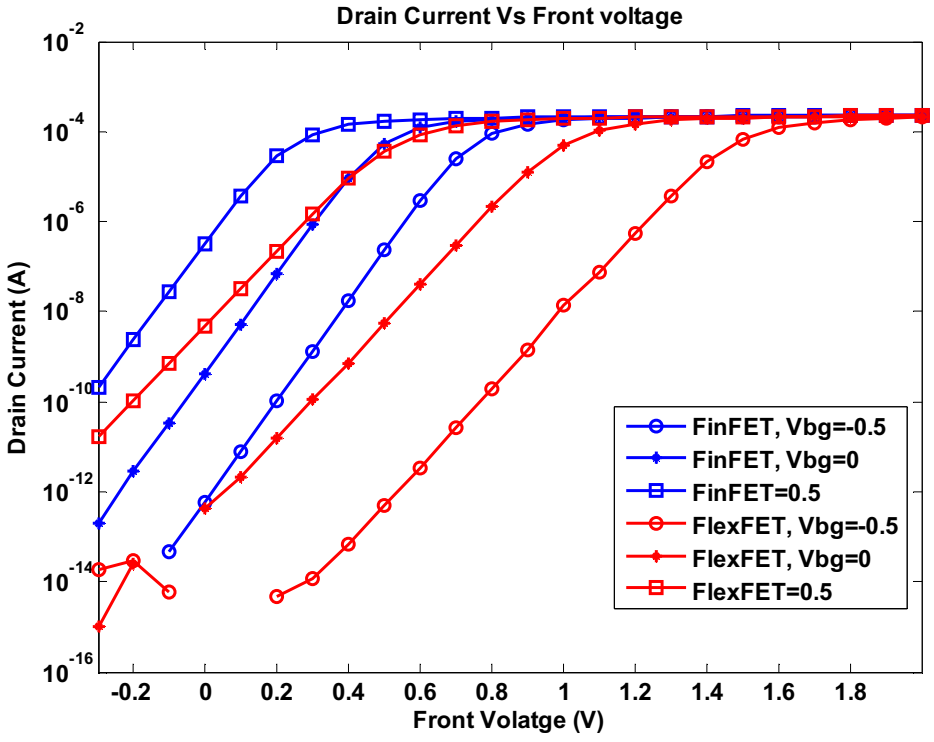

Figure 4.66. Variation of Dynamic Control Factor with Change in Silicon Film Thickness N+(TG) – P+ (BG)

Table 4.27. Summary of the Analytical Study of IDG-FinFET and IDG-FlexFET

Device [TG –BG]	Threshold Voltage (Vt)		Dynamic Threshold Control (f)	
	FinFET	FlexFET	FinFET	FlexFET
Midgap - Midgap	In range	In range	Too low	In range
P+ - P+	Too High	Too High	Too Low	In range
Midgap – P+	In range	In range	Too Low	In range
P+ - Midgap	Too High	Too High	Too Low	In Range
N+ - Midgap	Too Low	Too Low	Too Low	In Range
N+ - P+	In Range	In Range	Too Low	In Range

On the basis of the analytical model it has been established that IDG-FlexFET is the design option for ULP applications and therefore there is a need for a compact model that closely defines the electrical characteristics of this device enabling the circuit/process design cooptimization. Simple analytical tools like MATLAB though accurate to a good extent are not as efficient, robust and fast as industry tools like SPICE and other circuit simulators. A single transistor simulation that takes around 5-10 minutes in MATLAB can be completed in less than a second using powerful CAD tools. This is one of the powerful motivational factors behind developing a compact model which is the source code behind a SPICE model for IDG-FlexFET.

CHAPTER 5

RESULTS OF THE COMPACT MODEL FOR FLEXFET

Analytical modeling of IDG-FINFET and IDG-FLEXFET in the previous chapter made it evident that IDG-FLEXFET was the design choice for ULP applications that need a high dynamic threshold control factor. It has been observed that designs with asymmetrical structures have an inherent advantage of giving rise to a high a variation in threshold voltage by merely adjusting the back gate voltage. This criterion makes IDG-FLEXFET unique and calls for more research to be carried out in a more efficient manner so as to help the industry capitalize on the dynamic threshold variation this device can offer.

A compact model is a link between process technology and circuit design. It is a concise mathematical description of the complex device physics in the transistor. A compact model maintains a fine balance between accuracy and simplicity. An accurate model based on physics allows the process engineer and circuit designer to make projections beyond the available silicon data for scaled dimensions and also enables fast circuit/device co-optimization. The simplifications in the physics enable very fast analysis of device/circuit behavior when compared to the much slower numerically-based TCAD simulations. It is thus necessary to develop a compact model of multi-gate FETs for technology/circuit development in the short-term and for product design in the long-term [78].

The Device Group at University of California, Berkeley, has developed and studied the BSIM family of compact model for both common and independent gate transistors [79, 80]. They have focused their work on symmetrical structures like FinFETs. The aim of this research is modify the UC Berkeley BSIM compact model which is a generic model for multi-gate devices, and modify it to suit highly asymmetrical devices like FlexFET. The beta Verilog-A code was shared by the Berkeley research team. This chapter will focus on regenerating the results obtained for the IDG-FlexFET cases that proved to be useful for ULP applications using the analytical surface potential approach. The result of this work would be a compact model that models, highly asymmetrical independent double-gated transistors that can be exported to the user community.

5.1. Compact Model for IDG-FlexFET

Commercial and industrial analog simulators (such as SPICE) need to add device models as technology advances and earlier models become inaccurate. The **Compact Model Council** is a working group in the Electronic Design Automation industry formed to choose, maintain, and promote the use of standard models. Before this group was formed, new transistor models were largely proprietary, which severely limited the choice of simulators that could be used. New models are submitted to the Council, where their technical merits are discussed, and then potential standard models are voted on to become compact models that can be used by commercial and industrial analog simulators.

The compact model for IDG-FlexFET allows users to model electrical characteristics of independent double-gated structures with high asymmetry in structures. It allows for different top and bottom gate work functions, dielectric thicknesses, and dielectric constants. It models the independent double-gated structure as a four terminal device, containing the source, drain, top gate, and bottom gate terminals. The two gates can be biased at different voltages. It is a VERILOG-A code, based on the surface potential approach. Here the surface potentials at the source and drain end are obtained by solving the Poisson's equation in fully depleted, lightly doped body and calculating with efficient analytical approximations.

One of the main problems of modeling independent double-gated devices using surface potential approach was the computation of transcendental nonlinear equations that need to be solved accurately to arrive at the right roots to compute the surface potentials at source and drain end. It is a tedious process where the roots need to be computed through iterative methods where the initial starting points have to be mostly provided manually and the right starting point is crucial in determining the accuracy of the roots. The optimization process in this method takes up a lot of time for generating a single I-V curve. This is not desirable for a compact model that needs to be used in the industry where thousands of transistors would be simulated on a circuit under test. In order to overcome this problem, an approximation method has been employed in the compact model for IDG-FlexFET. Surface potentials at source and drain end are computed separately as explained in the previous chapter. Some common calculations to source and drain end surface potentials are

$$A = \frac{2q_i n_i V_t}{\epsilon_{si}} \quad (5.1)$$

$$G^2 = A\left(\frac{Tox}{V_t}\right)^2 \quad (5.2)$$

$$x_{inv,0} = -1.2.\ln(G^2) \quad (5.3)$$

$$V_{gfb1eff} = Vtg - Vfbtg \quad (5.4)$$

The procedure for calculating surface potential at the source end is as follows

$$x_g = \frac{V_{gfb1eff}}{Vt} \quad (5.5)$$

$$x_n = \frac{V_{cheff,s}}{Vt} \quad (5.6)$$

where $V_{cheff,s}$= Vch at source end, i.e., zero.

$$x_{inv} = x_n + x_{inv0} \quad (5.7)$$

$$\eta = \frac{1}{2}.(x_g + x_{inv} - \sqrt{(x_g - x_{inv})^2 + 10}) \quad (5.8)$$

$$a = (x_g - \eta)^2 \quad (5.9)$$

$$c = 2.(x_g - \eta) \quad (5.10)$$

$$\tau = x_n - \eta + \ln\left(\frac{a}{G^2}\right) \quad (5.11)$$

$$v = a + c \quad (5.12)$$

$$\mu = \frac{v^2}{\tau} + \frac{c^2}{2} - a \quad (5.13)$$

$$x_{inv} = \eta + \frac{av}{\mu + \frac{Vc}{\mu}\left(\frac{c}{3}c^2 - a\right)} \quad (5.14)$$

$$e_0 = \frac{V_{gfb1eff} - V_{gfb2effs}}{TSi + Tox} \quad (5.15)$$

$V_{gfb2effs}$=Vbg-Vfbbg (5.16)

$$x_{sub} = x_g - \frac{e_0 Tox}{V_t} \quad (5.17)$$

$$\delta = 0.05 \quad (5.18)$$

$$T_0 = x_{inv} - x_{sub} - \delta \tag{5.19}$$

$$x_{init} = x_{inv} - \frac{1}{2}.(T_0 + \sqrt{T_0^2 + 20\delta}) \tag{5.20}$$

$$x_s = \frac{e_0^2}{A} + 10000 \tag{5.21}$$

$$x_0 \leftarrow x_{init} \tag{5.22}$$

The following algorithm is executed three times

$$\Delta_0 \leftarrow \exp(x_0 - x_n) \tag{5.23}$$

$$p \leftarrow 2(x_g - x_0) + G^2\Delta_0 \tag{5.24}$$

$$q \leftarrow (x_g - x_0)^2 + G^2(x_s + \Delta_0) \tag{5.25}$$

$$x_0 \leftarrow x_0 + \frac{2q}{p + \sqrt{p^2 - 2q(2 - G^2\Delta_0)}} \tag{5.26}$$

Then,

$$\psi_{fs} \leftarrow x_0.Vt \tag{5.27}$$

which is the surface potential at the source end. Surface potential at the drain end is computed with the same procedure except that *Vch* at drain end would be equal to *Vds*. The I-V model is consistent with that presented in the previous chapter.

5.2. Comparison of Compact Model Results with the Analytical Model

This section presents the comparison between the results generated by the analytical model and that of the compact model for the device models that had a high dynamic threshold control factor and a threshold voltage in and around the range of 0V to 1V according to the analysis in the previous sections.

The IDG-FlexFET devices considered are those with N+ (TG) – P+ (BG), Midgap (TG) – P+ (BG), and Midgap (TG) – Midgap (BG). The performance metrics are the same as in the case of analytical model analysis, threshold voltage, and dynamic threshold control factor. The compact model simulations were carried out with the same conditions as those in the analytical model simulations. The top oxide thickness has been fixed for 3 nm for cases where other device parameters have been varied and it has been varied from 1 nm to 10 nm in to Study the effect of top oxide thickness on performance metrics. The silicon film thickness has been fixed to 10 nm when top oxide thickness was varied and it has been varied from 6 nm to 30 nm while Studying its effect on the performance metrics.

5.2.1. N+ (TG) – P+ (BG)

The effect of top oxide thickness on the threshold voltage is observed in Figure 5.1. The figure shows the variation of threshold voltage with oxide thickness for bottom gate voltage of -0.5V, 0V, and 0.5V for analytical model and compact model. It can be seen from the figure that compact model follows the trend generated by the analytical model very closely. Table 5.1 shows the values used to generate these curves.

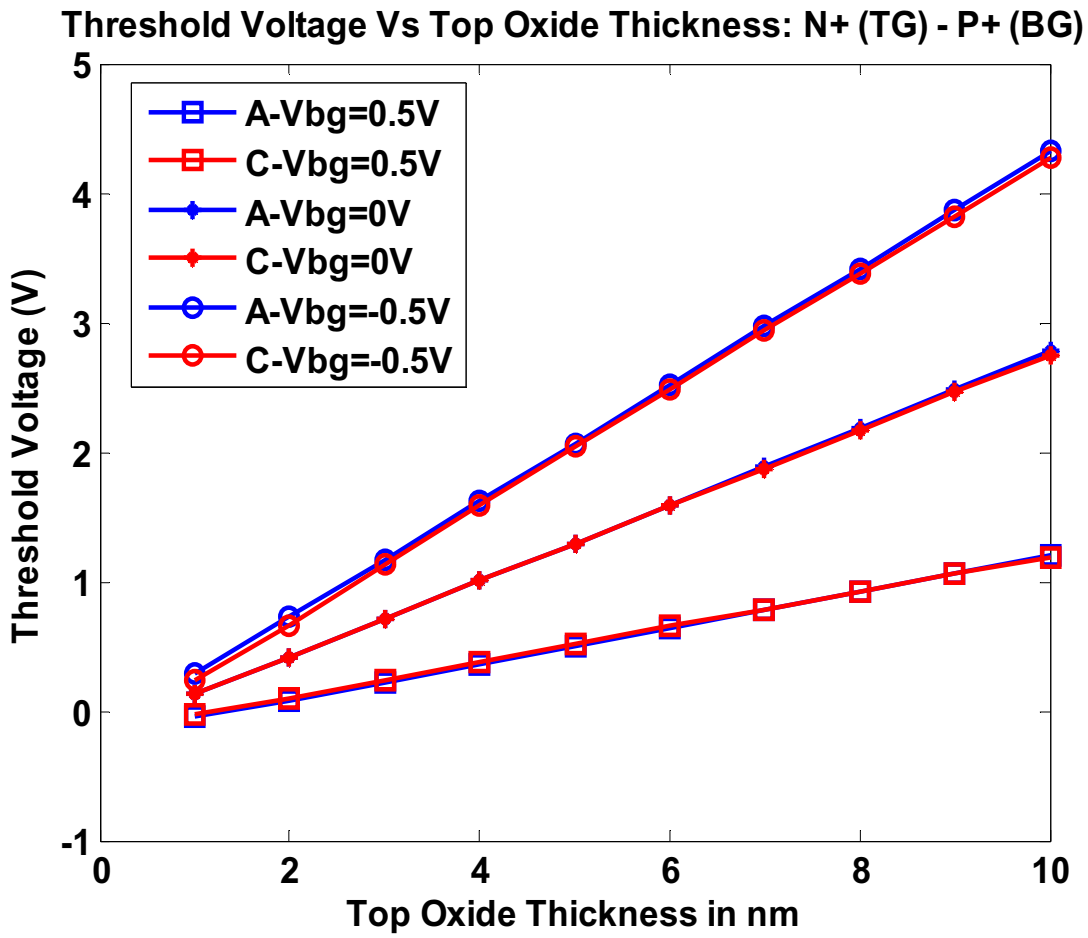

Figure 5.1. Variation of Threshold Voltage with Change in Top Oxide Thickness N+ (TG) – P+ (BG)

Table 5.1. Variation of Threshold Voltage in analytical and compact models for IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg N+ (TG) – P+ (BG)

TOX in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
1	-0.05	0.13	0.29	-0.03	0.13	0.23
2	0.09	0.42	0.73	0.10	0.41	0.66
3	0.23	0.71	1.18	0.24	0.71	1.14
4	0.36	1.00	1.63	0.37	1.00	1.59
5	0.50	1.30	2.07	0.51	1.30	2.04
6	0.64	1.59	2.52	0.65	1.59	2.49
7	0.79	1.89	2.97	0.78	1.88	2.93
8	0.93	2.19	3.42	0.92	2.17	3.38
9	1.07	2.49	3.87	1.06	2.46	3.82
10	1.21	2.78	4.32	1.19	2.75	4.27

The dynamic threshold control factor variation with oxide thickness is shown in Figure 5.2 for both analytical and compact models. The values used to generate the graphs and the percentage discrepancy of the compact model generated values from those of the analytical model ones are also presented in Table 5.2. It can be seen from the figure and the table that the compact model follows the analytical model very closely. The error percentage in most cases is less that 1.7%.

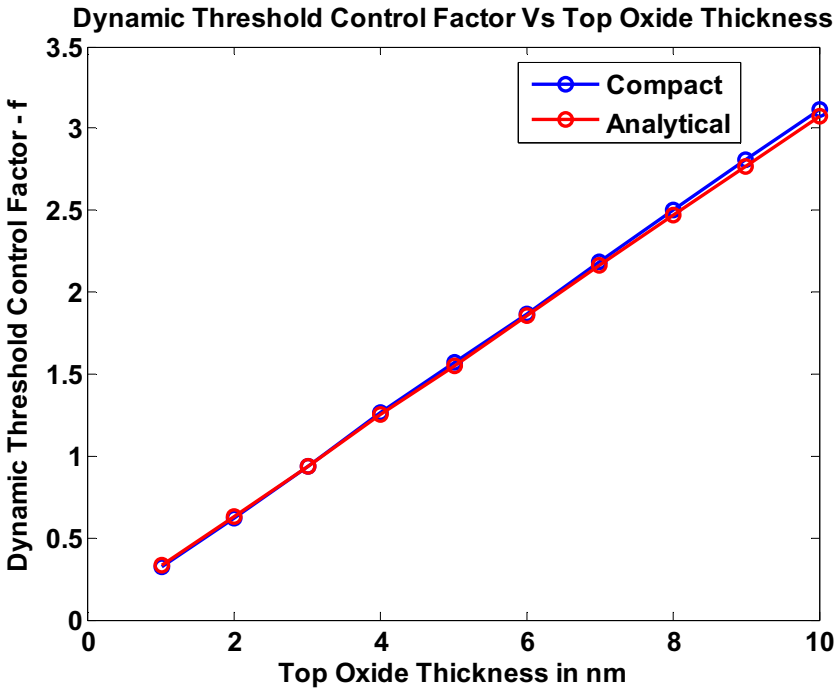

Figure 5.2. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness for analytical and compact models – N+ (TG) – P+ (BG)

Table 5.2. Dynamic Threshold Control Factor IDG FlexFET in case of analytical and compact models for variation in Top Oxide Thickness: N+ (TG) -P+ (BG)

TOX in nm	Analytical f	Compact f	Error Percentage
1	0.33	0.32	1.71
2	0.63	0.62	1.77
3	0.94	0.94	0.03
4	1.25	1.26	0.84
5	1.55	1.57	1.30
6	1.86	1.87	0.58
7	2.16	2.19	1.23
8	2.47	2.50	1.16
9	2.77	2.81	1.38
10	3.08	3.12	1.33

The variation of threshold voltage with silicon film thickness in case of analytical and compact model can be seen in Figure 5.3. The values used to generate these graphs are presented in Table 5.3. Again the compact model follows the trend of the analytical model very closely. The little shift in the curves generated by compact model can be attributed to the fact that it uses an approximation method to compute the surface potentials at the source and the drain end, which result in the shift in case of silicon film thickness variation.

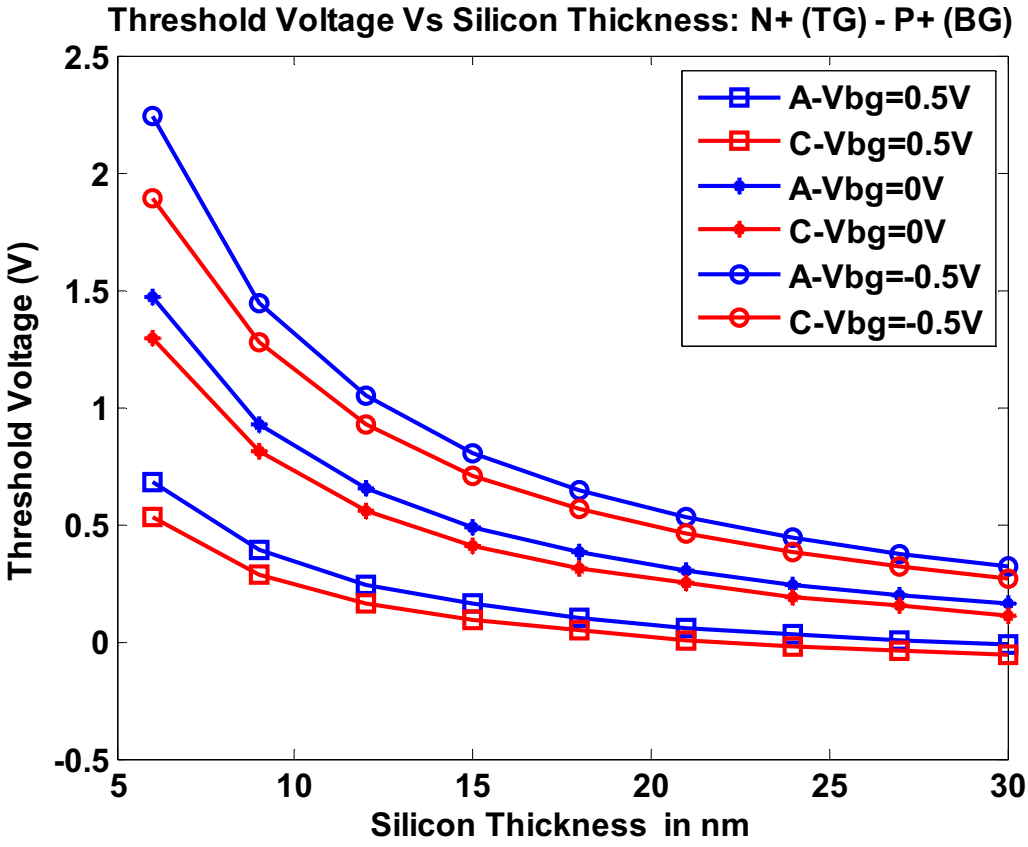

Figure 5.3. Variation of Threshold Voltage with Change in Silicon Film Thickness N+ (TG) – P+ (BG)

Table 5.3. Variation of Threshold Voltage in analytical and compact models IDG-FlexFET for different values of Silicon Film Thickness and different values of Vbg- N+ (TG) – P+ (BG)

Tsi in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
6	0.68	1.47	2.25	0.53	1.30	1.89
9	0.39	0.93	1.45	0.29	0.81	1.27
12	0.25	0.65	1.05	0.16	0.56	0.92
15	0.16	0.49	0.80	0.09	0.41	0.71
18	0.10	0.38	0.65	0.05	0.31	0.56
21	0.06	0.30	0.53	0.01	0.25	0.46
24	0.03	0.24	0.44	-0.02	0.19	0.38
27	0.01	0.20	0.38	-0.04	0.15	0.32
30	-0.02	0.16	0.32	-0.05	0.11	0.27

The dynamic threshold control factor variation for silicon film thickness for analytical and compact models can be seen in Figure 5.4. The data used to generate these graphs can be seen in Table 5.4. The error percentage of difference in the two sets of values is evident that the compact model follows the analytical model closely in terms of the dynamic threshold control factor.

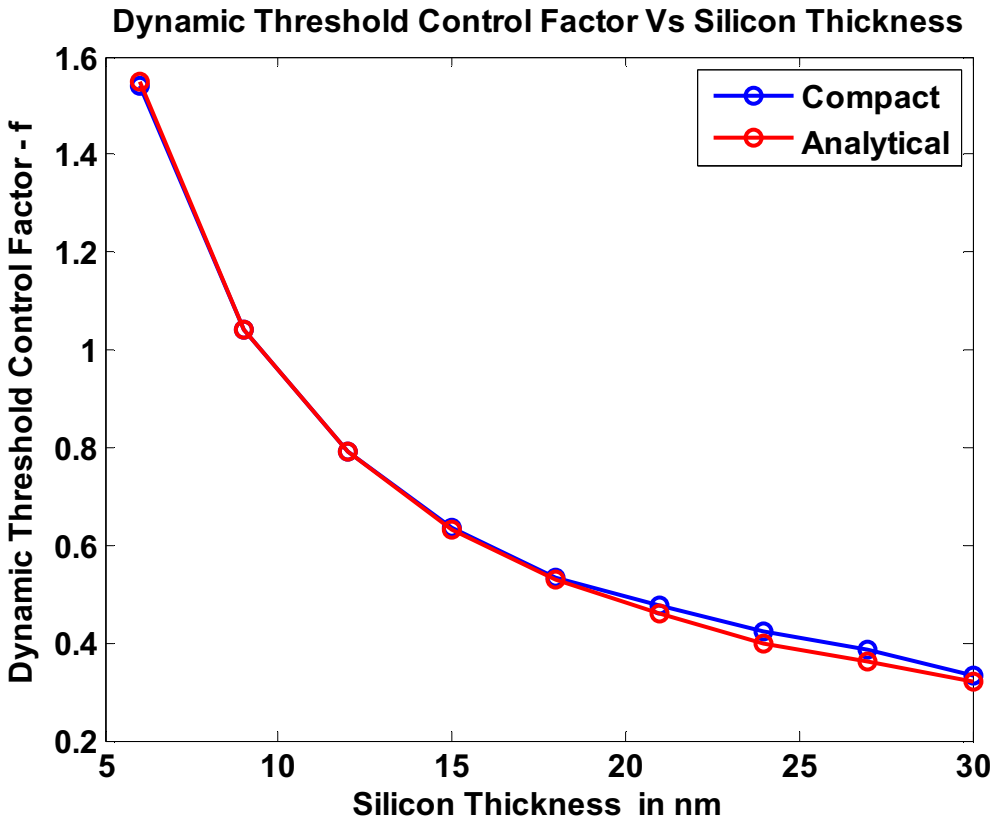

Figure 5.4. Variation of Dynamic Control Factor with Change in Silicon Film Thickness N+ (TG) – P+ (BG)

Table 5.4. Dynamic Threshold Control Factor in analytical and compact models for IDG FlexFET for variation in Silicon Film Thickness- N+(TG) – P+ (BG)

Tsi in nm	Analytical f	Compact f	Error Percentage
6	1.55	1.54	0.66
9	1.04	1.04	0.08
12	0.79	0.79	0.42
15	0.63	0.63	0.74
18	0.53	0.53	0.51
21	0.46	0.48	3.98
24	0.40	0.42	6.03
27	0.36	0.39	7.10
30	0.32	0.33	3.50

5.2.2. Midgap (TG) – P+ (BG)

The effect of top oxide thickness on the threshold voltage is observed in Figure 5.5. The figure shows the variation of threshold voltage with oxide thickness for bottom gate voltage of -0.5V, 0V, and 0.5V for analytical model and compact model. It can be seen from the figure that compact model follows the trend generated by the analytical model very closely. Table 5.5 shows the values used to generate these curves.

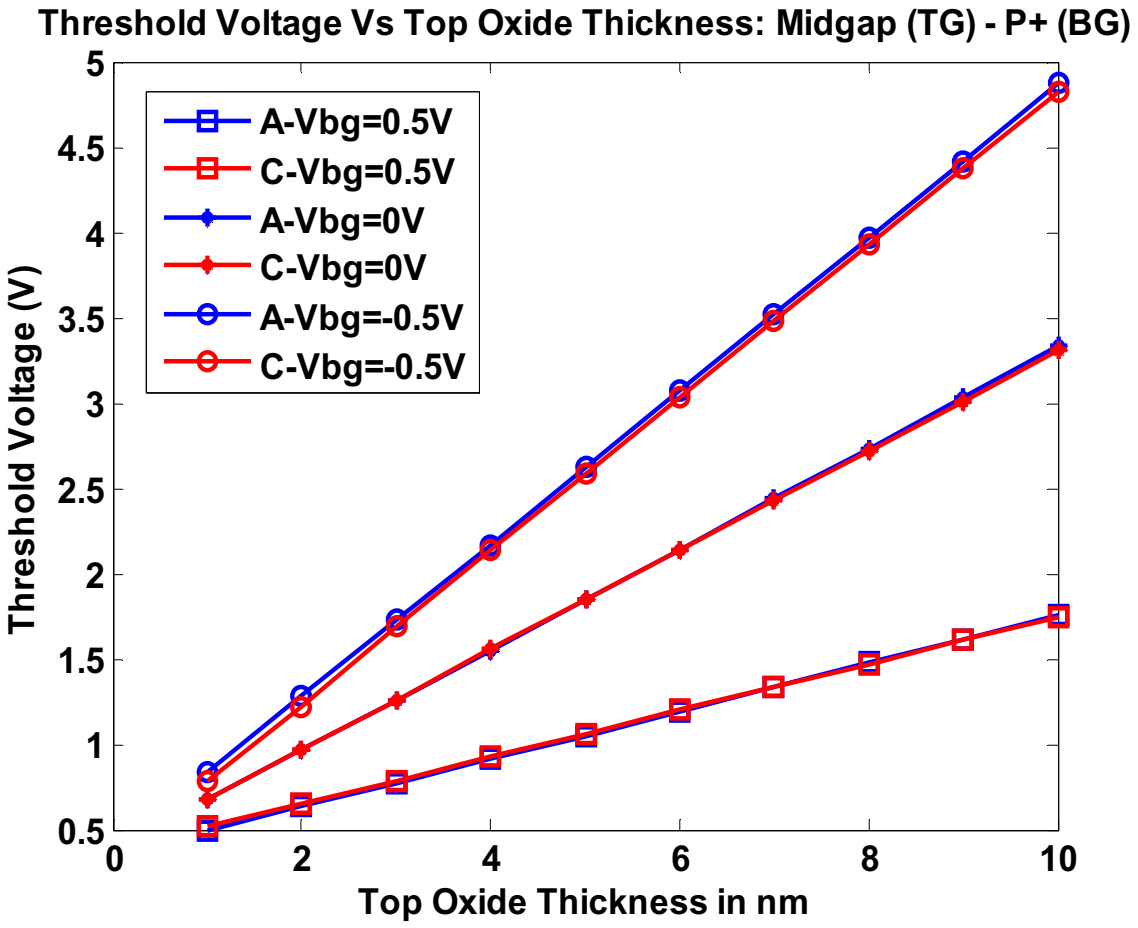

Figure 5.5. Variation of Threshold Voltage with Change in Top Oxide Thickness Midgap (TG) – P+ (BG)

Table 5.5. Variation of Threshold Voltage in analytical and compact models for IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg Midgap (TG) – P+ (BG)

TOX in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
1	0.50	0.68	0.84	0.52	0.68	0.78
2	0.64	0.97	1.28	0.65	0.96	1.21
3	0.77	1.26	1.73	0.79	1.26	1.69
4	0.91	1.55	2.17	0.92	1.55	2.14
5	1.05	1.85	2.62	1.06	1.85	2.59
6	1.19	2.14	3.07	1.20	2.14	3.04
7	1.33	2.44	3.52	1.33	2.43	3.48
8	1.48	2.74	3.97	1.47	2.72	3.93
9	1.62	3.03	4.42	1.61	3.01	4.37
10	1.76	3.33	4.87	1.74	3.30	4.82

The dynamic threshold control factor variation with oxide thickness is shown in Figure 5.6 for both analytical and compact models. The values used to generate the graphs and the percentage discrepancy of the compact model generated values from those of the analytical model ones are also presented in Table 5.6. It can be seen from the figure and the table that the compact model follows the analytical model very closely.

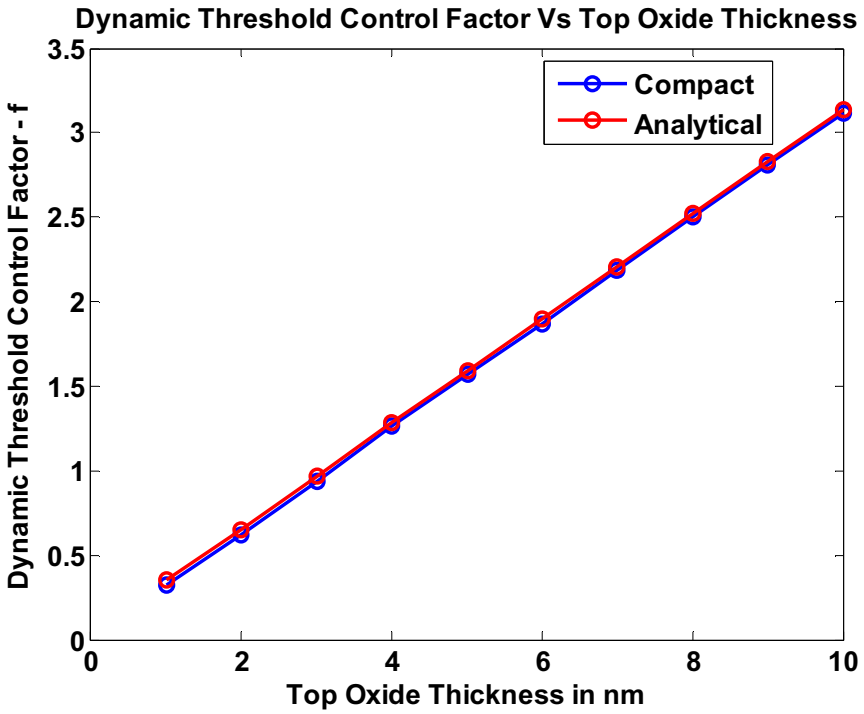

Figure 5.6. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness for analytical and compact models – Midgap (TG) – P+ (BG)

Table 5.6. Dynamic Threshold Control Factor IDG FlexFET in case of analytical and compact models for variation in Top Oxide Thickness: Midgap (TG) -P+ (BG)

TOX in nm	Analytical f	Compact f	Error Percentage
1	0.35	0.32	7.33
2	0.65	0.62	4.79
3	0.97	0.94	3.12
4	1.28	1.26	1.52
5	1.59	1.57	1.26
6	1.90	1.87	1.54
7	2.21	2.19	1.06
8	2.52	2.50	0.85
9	2.83	2.81	0.77
10	3.14	3.12	0.61

The little shift in the curves generated by compact model can be attributed to the fact that it uses an approximation method to compute the surface potentials.

The variation of threshold voltage with silicon film thickness in case of analytical and compact model can be seen in Figure 5.7. The values used to generate these graphs are presented in Table 5.7. Again the compact model follows the trend of the analytical model very closely.

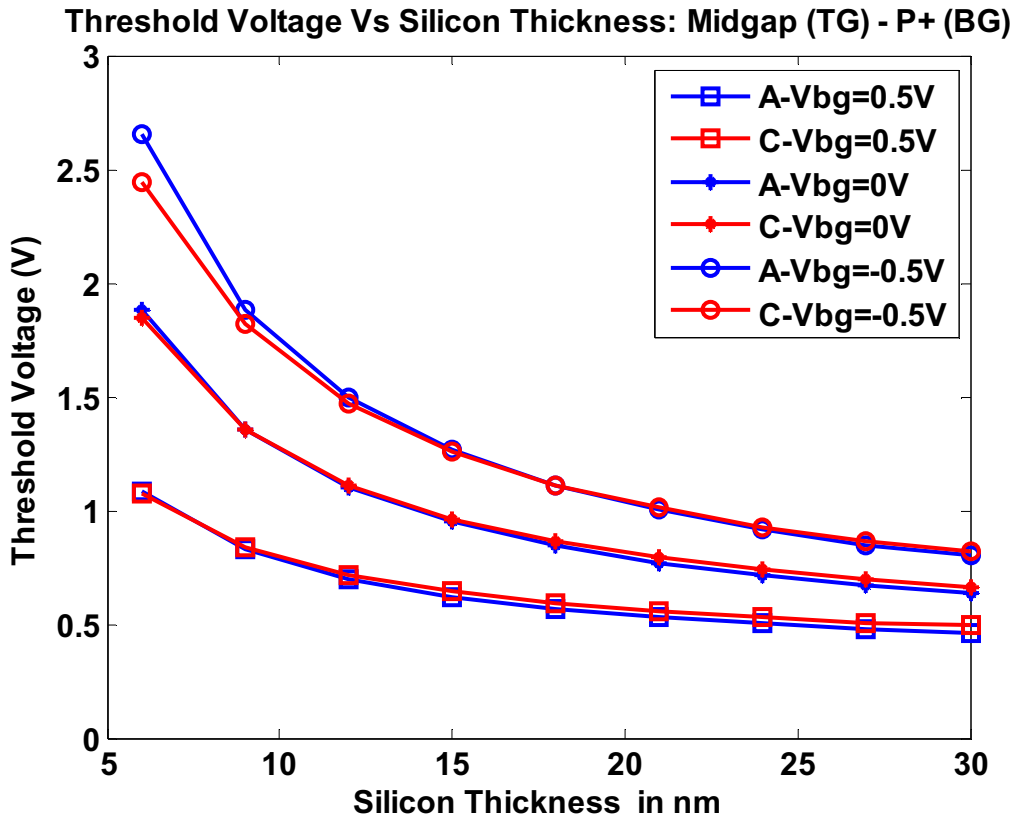

Figure 5.7. Variation of Threshold Voltage with Change in Silicon Film Thickness Midgap (TG) – P+ (BG)

Table 5.7. Variation of Threshold Voltage in analytical and compact models IDG-FlexFET for different values of Silicon Film Thickness and different values of Vbg- Midgap (TG) – P+ (BG)

Tsi in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
6	1.09	1.88	2.66	1.08	1.85	2.44
9	0.83	1.36	1.88	0.84	1.36	1.82
12	0.70	1.10	1.50	0.71	1.11	1.47
15	0.62	0.95	1.27	0.64	0.96	1.26
18	0.57	0.85	1.11	0.60	0.86	1.11
21	0.53	0.77	1.00	0.56	0.80	1.01
24	0.50	0.72	0.92	0.53	0.74	0.93
27	0.48	0.67	0.85	0.51	0.70	0.87
30	0.46	0.64	0.80	0.50	0.66	0.82

The dynamic threshold control factor variation for silicon film thickness for analytical and compact models can be seen in Figure 5.8. The data used to generate these graphs can be seen in Table 5.8. The error percentage of difference in the two sets of values is evident that the compact model follows the analytical model closely in terms of the dynamic threshold control factor.

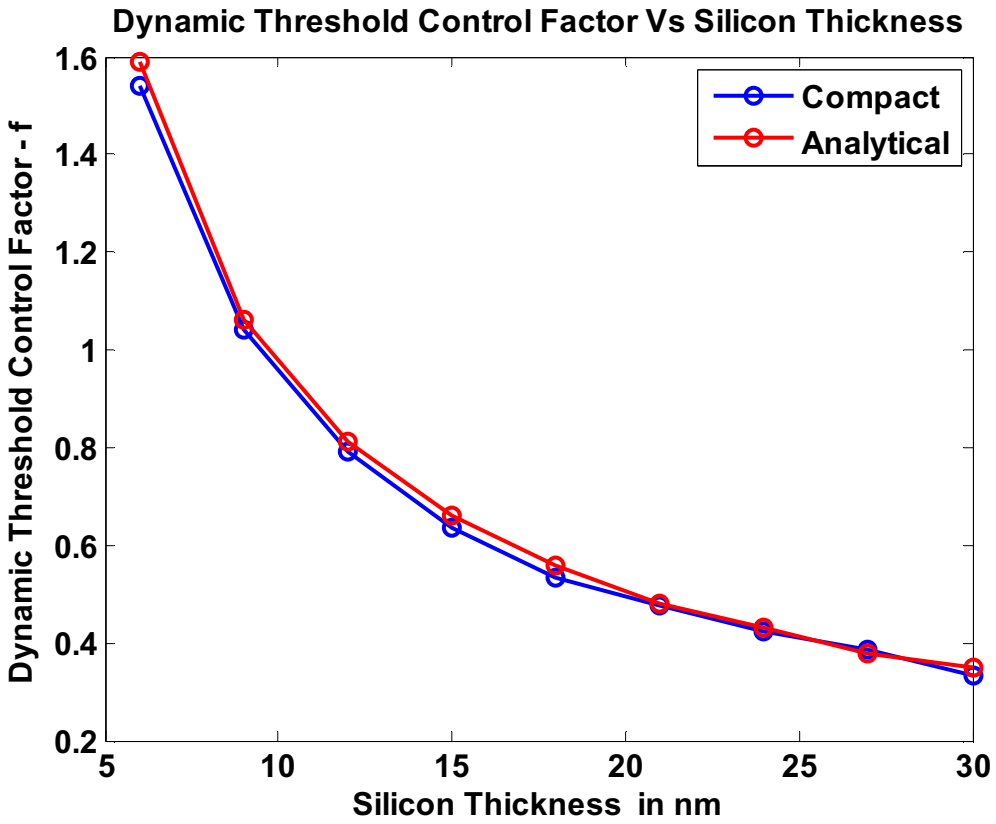

Figure 5.8. Variation of Dynamic Control Factor with Change in Silicon Film Thickness Midgap (TG) – P+ (BG)

Table 5.8. Dynamic Threshold Control Factor in analytical and compact models for IDG FlexFET for variation in Silicon Film Thickness- Midgap (TG) – P+ (BG)

Tsi in nm	Analytical f	Compact f	Error Percentage
6	1.59	1.54	3.16
9	1.06	1.04	1.82
12	0.81	0.79	2.07
15	0.66	0.63	3.84
18	0.56	0.53	4.88
21	0.48	0.48	0.35
24	0.43	0.42	1.37
27	0.38	0.39	-1.46
30	0.35	0.33	5.38

5.2.3. Midgap (TG) – Midgap (BG)

The effect of top oxide thickness on the threshold voltage is observed in Figure 5.9. The figure shows the variation of threshold voltage with oxide thickness for bottom gate voltage of -0.5V, 0V, and 0.5V for analytical model and compact model. It can be seen from the figure that compact model follows the trend generated by the analytical model but not as closely as in the case of half-asymmetry and full-asymmetry. Table 5.9 shows the values used to generate these curves.

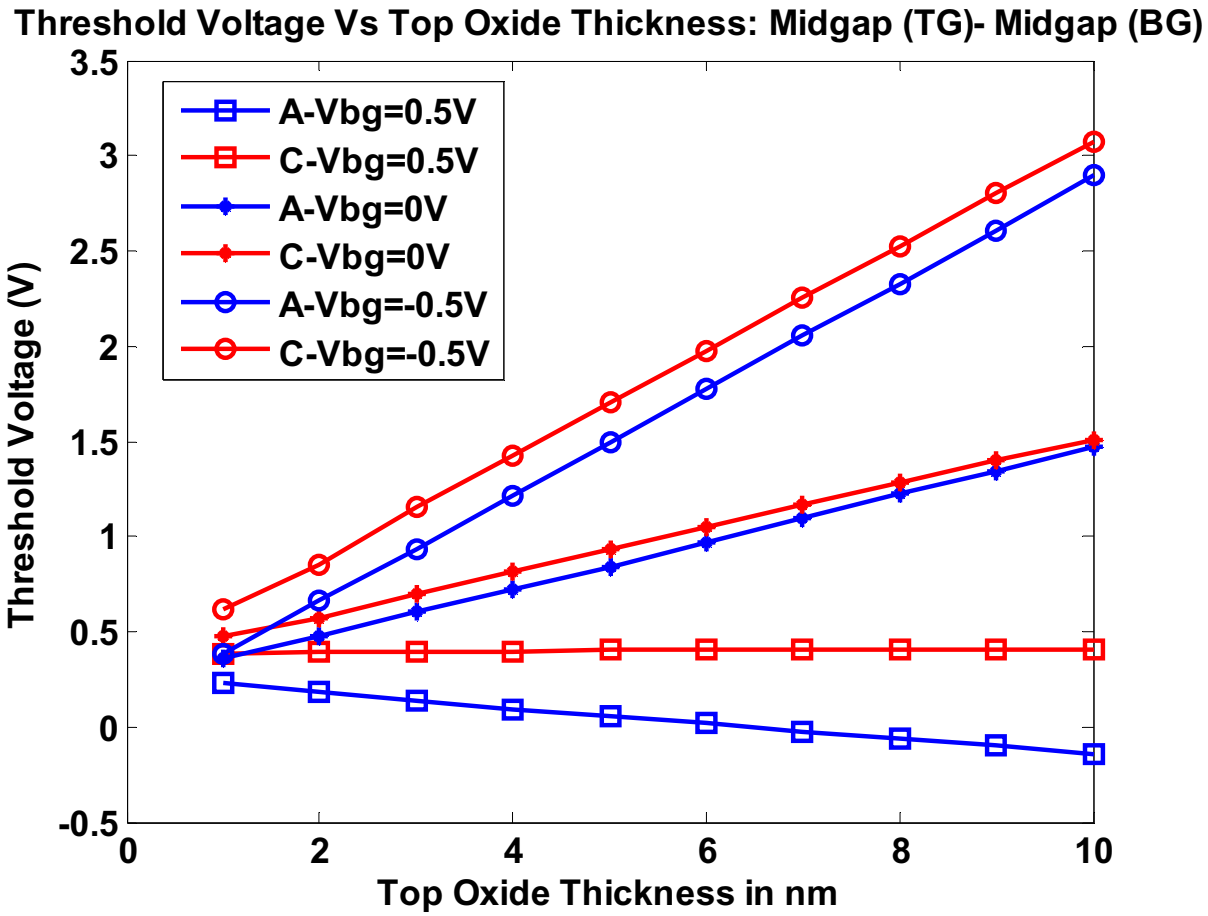

Figure 5.9. Variation of Threshold Voltage with Change in Top Oxide Thickness Midgap (TG) – Midgap (BG)

Table 5.9. Variation of Threshold Voltage in analytical and compact models for IDG FlexFET for different values of Top Oxide Thickness and different values of Vbg Midgap (TG) – Midgap (BG)

TOX in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
1	0.23	0.37	0.39	0.38	0.48	0.62
2	0.19	0.48	0.66	0.39	0.57	0.85
3	0.14	0.60	0.94	0.40	0.70	1.15
4	0.10	0.73	1.21	0.40	0.81	1.43
5	0.06	0.85	1.49	0.40	0.93	1.71
6	0.02	0.97	1.77	0.40	1.05	1.98
7	-0.03	1.10	2.05	0.40	1.16	2.25
8	-0.07	1.22	2.33	0.40	1.28	2.53
9	-0.10	1.35	2.61	0.40	1.40	2.80
10	-0.14	1.48	2.90	0.40	1.51	3.07

The dynamic threshold control factor variation with oxide thickness is shown in Figure 5.10 for both analytical and compact models. The values used to generate the graphs and the percentage discrepancy of the compact model generated values from those of the analytical model ones are also presented in Table 5.10. It can be seen from the figure and the table that the compact model follows the analytical model very closely in terms of dynamic threshold control factor very closely when compared to the threshold voltage.

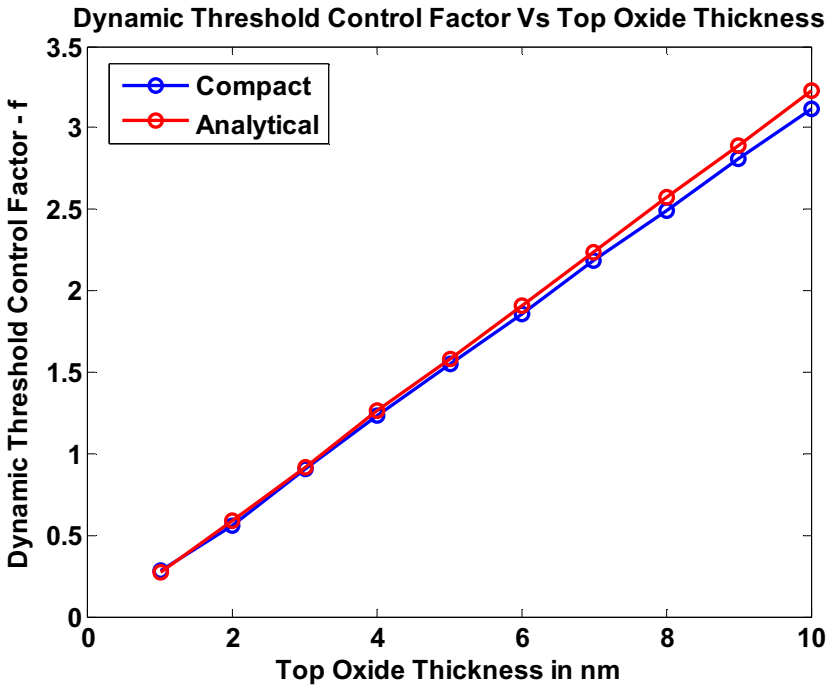

Figure 5.10. Variation of Dynamic Threshold Control Factor with Change in Top Oxide Thickness for analytical and compact models – Midgap (TG) - Midgap (BG)

Table 5.10. Dynamic Threshold Control Factor IDG FlexFET in case of analytical and compact models for variation in Top Oxide Thickness: Midgap (TG) - Midgap (BG)

TOX in nm	Analytical f	Compact f	Error Percentage
1	0.27	0.28	4.70
2	0.59	0.56	5.19
3	0.92	0.90	1.71
4	1.26	1.23	2.45
5	1.58	1.55	1.68
6	1.91	1.86	2.70
7	2.24	2.18	2.52
8	2.57	2.49	2.96
9	2.89	2.81	2.83
10	3.23	3.12	3.44

The variation of threshold voltage with silicon film thickness in case of analytical and compact model can be seen in Figure 5.11. The values used to generate these graphs are presented in Table 5.11. Again the compact model follows the trend of the analytical model but not as closely as the asymmetrical cases. The little shift in the curves generated by compact model can be attributed to the fact that it uses an approximation method to compute the surface potentials.

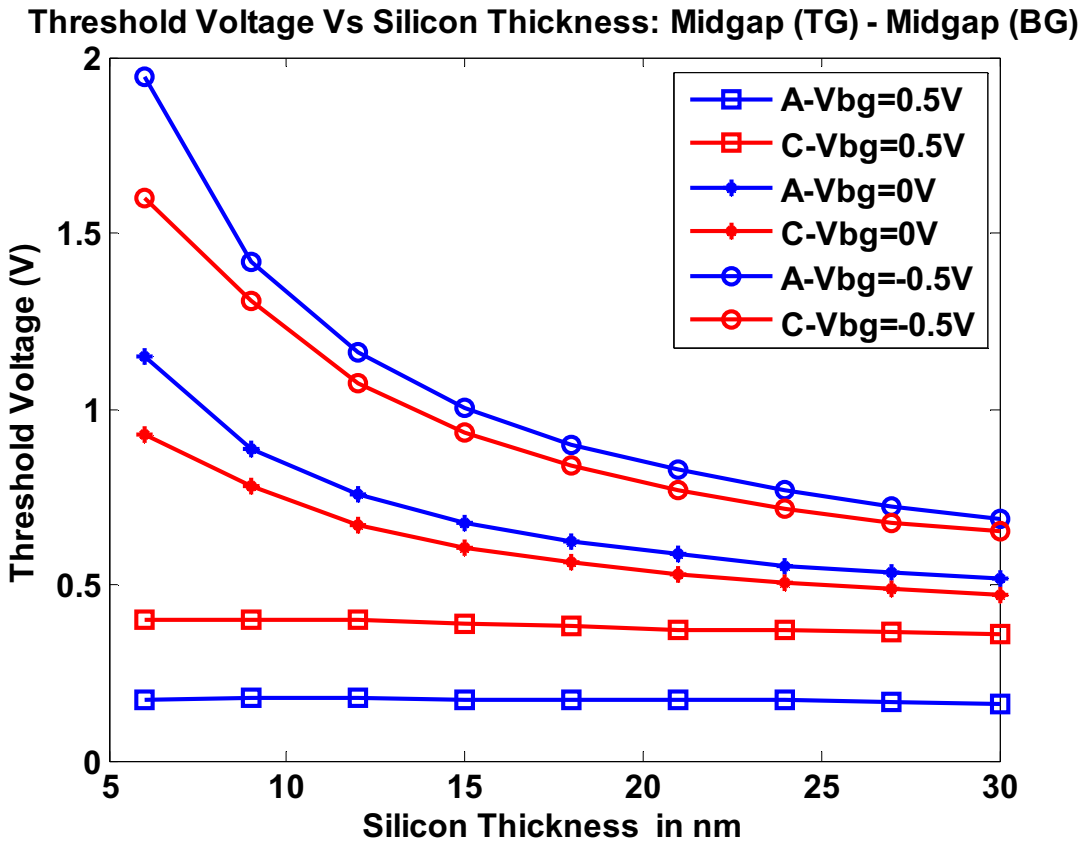

Figure 5.11. Variation of Threshold Voltage with Change in Silicon Film Thickness Midgap (TG) – Midgap (BG)

Table 5.11. Variation of Threshold Voltage in analytical and compact models IDG-FlexFET for different values of Silicon Film Thickness and different values of Vbg Midgap (TG) - Midgap (BG)

Tsi in nm	Analytical Vbg=0.5V	Analytical Vbg=0V	Analytical Vbg=-0.5V	Compact Vbg=0.5V	Compact Vbg=0V	Compact Vbg=-0.5V
6	0.18	1.15	1.95	0.40	0.93	1.60
9	0.18	0.89	1.42	0.40	0.78	1.31
12	0.18	0.76	1.16	0.40	0.67	1.07
15	0.18	0.68	1.01	0.39	0.61	0.93
18	0.18	0.63	0.90	0.38	0.56	0.84
21	0.17	0.59	0.83	0.37	0.53	0.77
24	0.17	0.56	0.77	0.37	0.51	0.72
27	0.17	0.54	0.73	0.37	0.49	0.68
30	0.16	0.52	0.69	0.36	0.47	0.65

The dynamic threshold control factor variation for silicon film thickness for analytical and compact models can be seen in Figure 5.12. The data used to generate these graphs can be seen in Table 5.12. The error percentage of difference in the two sets of values is evident that the compact model follows the analytical model closely for most silicon film thickness in terms of the dynamic threshold control factor.

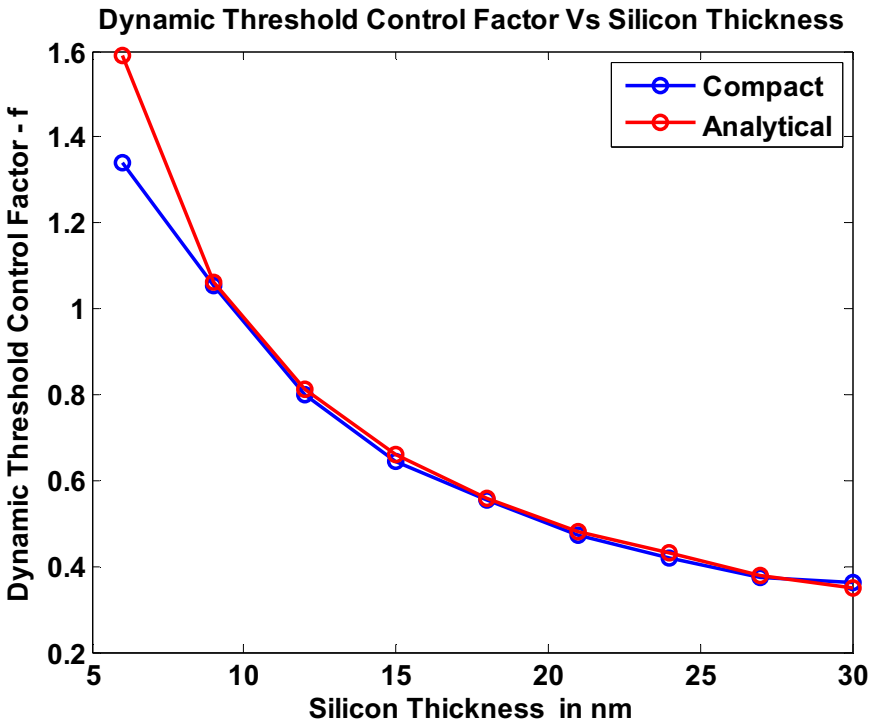

Figure 5.12. Variation of Dynamic Control Factor with Change in Silicon Film Thickness Midgap (TG) – Midgap (BG)

Table 5.12. Dynamic Threshold Control Factor in analytical and compact models for IDG FlexFET for variation in Silicon Film Thickness- Midgap (TG) – Midgap (BG)

Tsi in nm	Analytical f	Compact f	Error Percentage
6	1.59	1.34	15.65
9	1.06	1.05	0.80
12	0.81	0.80	1.39
15	0.66	0.65	2.10
18	0.56	0.55	1.29
21	0.48	0.47	1.23
24	0.43	0.42	2.89
27	0.38	0.37	1.74
30	0.35	0.36	3.29

5.3. Comparison of I-V Characteristics of Half-Asymmetry and Full Asymmetry Devices

This section presents the comparison between the I-V curves generated by the analytical model and the compact model for half-asymmetry and full-asymmetry devices. Figure 5.13 and Figure 4.14 show the drain current variations with front gate voltage for back gate voltage of -0.5 V, 0V, and 0.5 V. These curves have been generated with an optimum top oxide thickness of 3 nm and silicon film thickness of 10 nm for the ideal half-asymmetry case of Midgap (TG) – P+ (BG) and full-asymmetry case of N+ (TG) – P+ (BG).

It can be seen that the new FlexFET Verilog-A compact model is accurate in following the trend established by the analytical model.

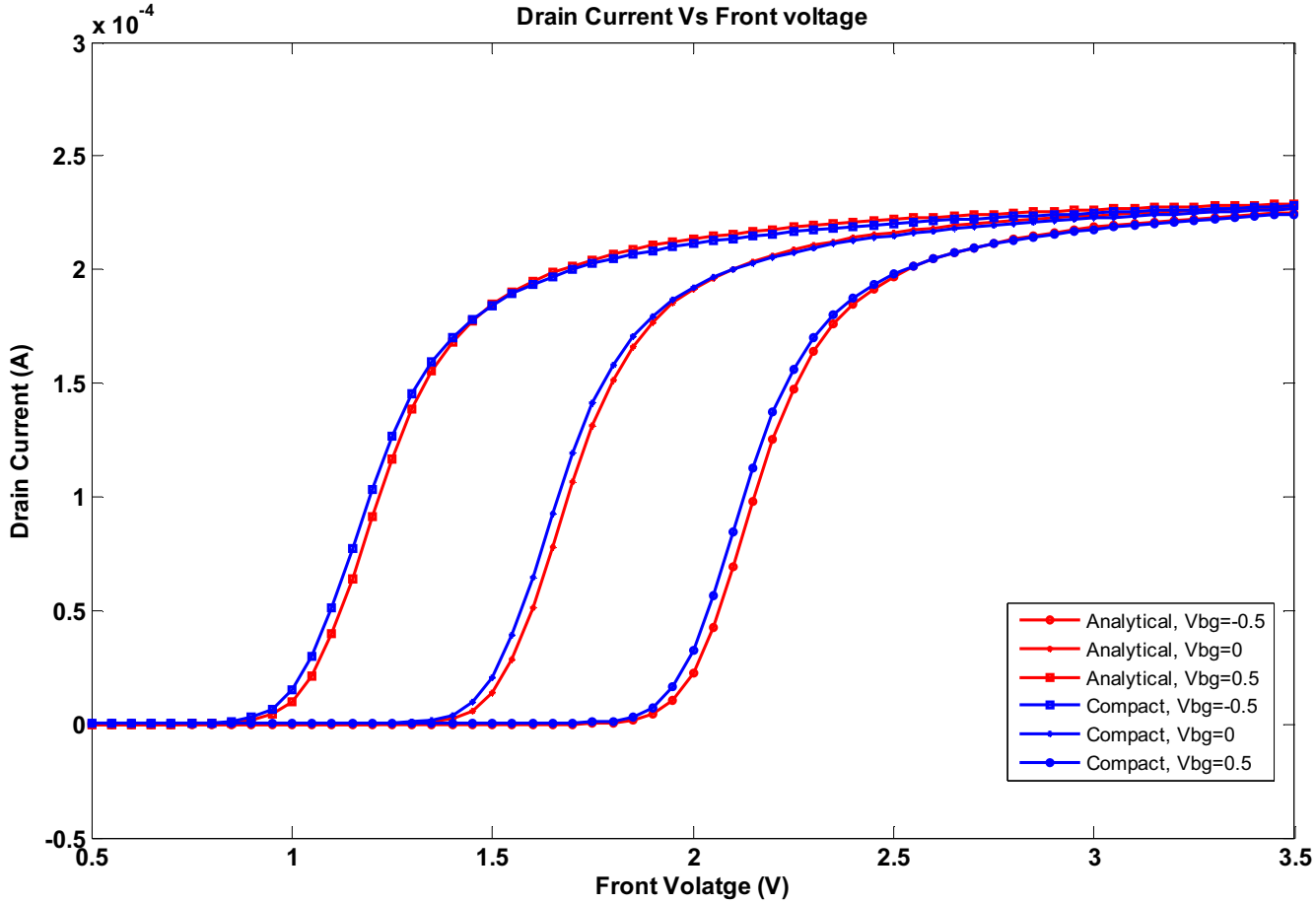

Figure 5.13. Drain Current Vs Front Gate Voltage for Different Back Gate Voltages- Midgap (TG)- P+ (BG)

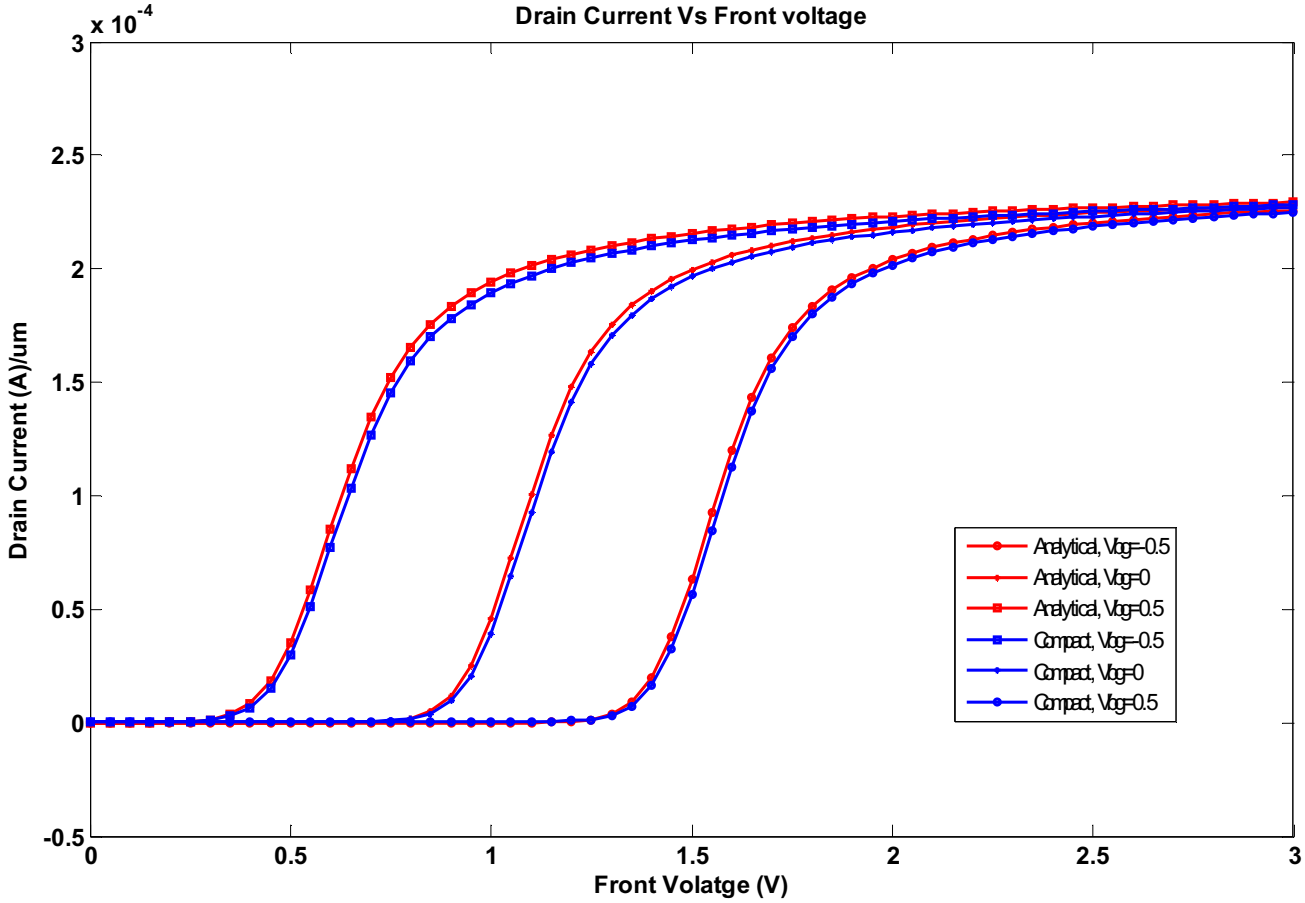

Figure 5.14. Drain Current Vs Front Gate Voltage for Different Back Gate Voltages- N+ (TG)- P+ (BG)

5.4. Comparison of the Compact Model with ASI Experimental Data

In order to evaluate the merit of the compact model developed, its results are compared against measured data from recently fabricated FlexFET nmos-transistors. These data were obtained from Mr. Dale Wilson at American Semiconductor, Inc. It has been taken from 0.18um FlexFET, with 4.5nm of oxide thickness and 77.5nm of silicon film thickness. It has a Midgap top gate and a P+ bottom gate. The supply voltage is at 1.8V.

In order to compare the performance of the compact model with real data, features like short channel effects, quantum mechanical effects, output conductance model, velocity overshoot model, GIDL, DIBL, Body doping effects, Drain Saturation Voltage, Mobility degradation, Channel length modulation, Current degradation factor, have been turned on in the code so as to match the real data trend. These modules have been developed by the Berkeley device research group for generic multi-gate IDG transistor and have been modified in this work to suit IDG-FlexFET in particular. Figure 5.15 shows the variation of drain current with respect to top gate voltage for different bottom gate voltages. It can be seen that the compact model closely follows the trend of the real-time data. The discrepancy can be attributed the values of the many unknown parameters used by the real device. Figure 5.16, Figure 5.17, and Figure 5.18 show the comparison between the real data, compact model with just the core physics, and the compact model with the full short channel physics turned on for different values of bottom gate voltages, respectively.

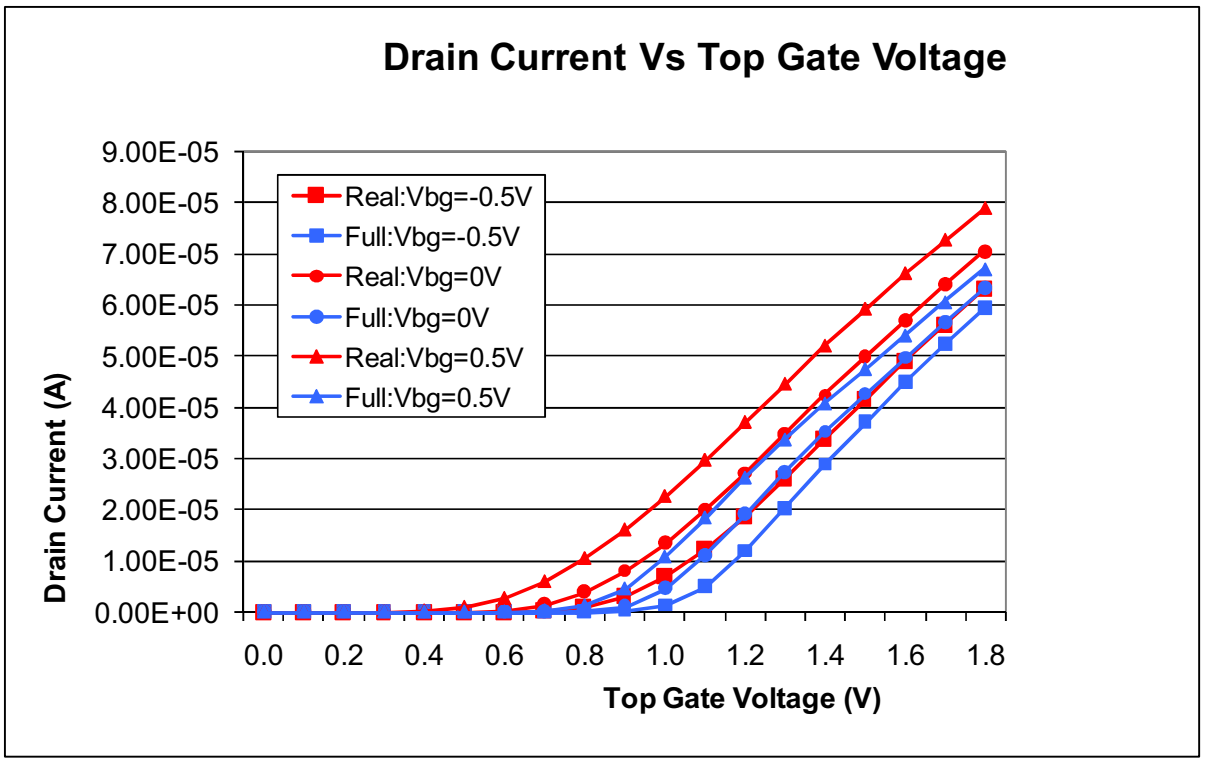

Figure 5.15. Real Experimental data Vs Data generated by the Compact model

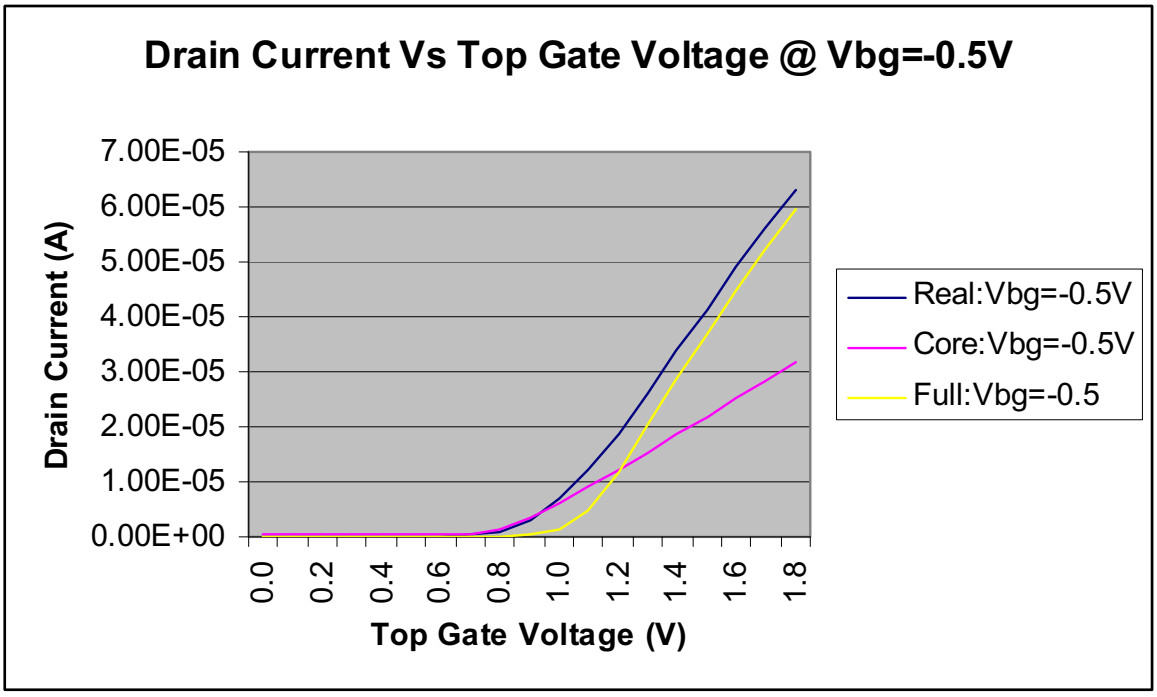

Figure 5.16. Real Experimental data, Core-Compact Model and Full-Compact Model for Vbg=-0.5V

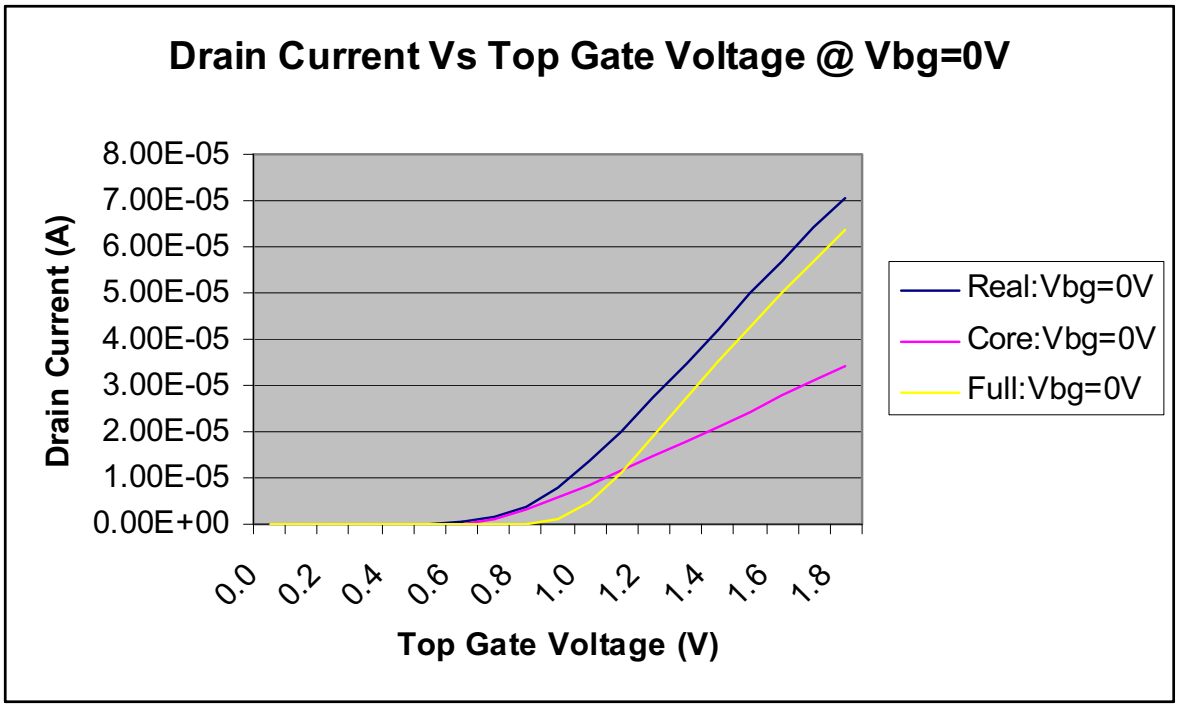

Figure 5.17. Real Experimental data, Core-Compact Model and Full-Compact Model for Vbg=0V

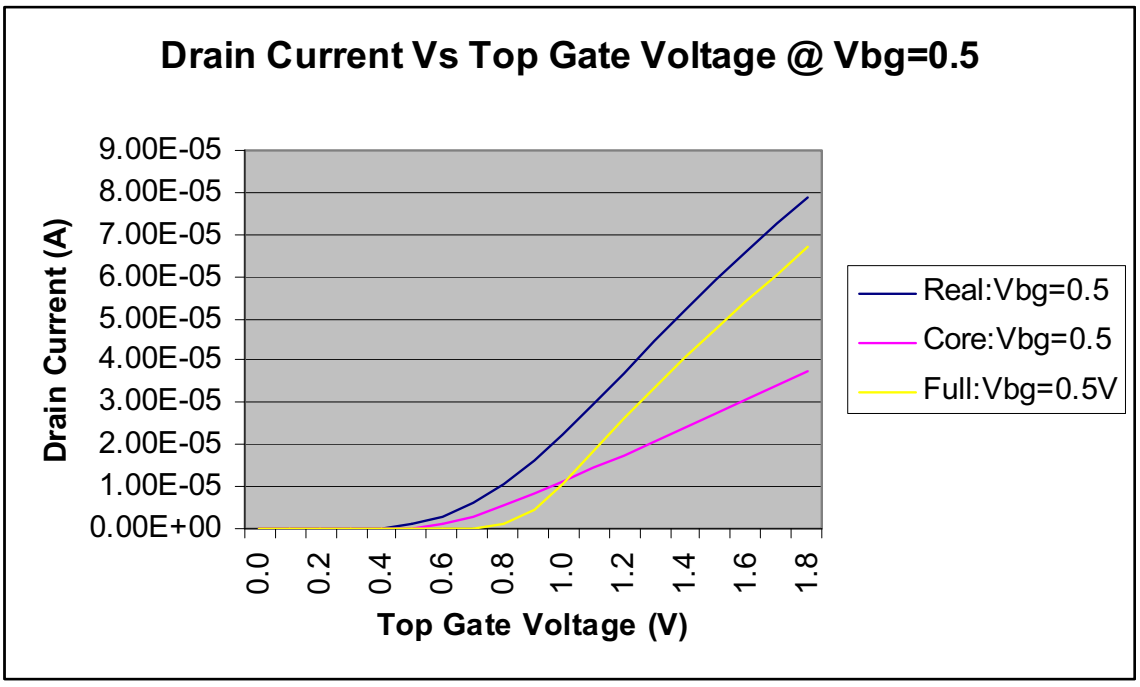

Figure 5.18. Real Experimental data, Core-Compact Model and Full-Compact Model for Vbg=0.5V

In summary, the results generated by the compact model have been compared to that of the analytical model for three cases: Midgap (TG) – Midgap (BG), Midgap (TG) - P+ (BG), N+ (TG) – P+ (BG). The results generated by the compact model closely for full-asymmetry and half-asymmetry cases and to a good extent in case of the symmetrical one. The result of the compact model with full features turned on has been compared with the real experimental data taken from an IDG-FlexFET and the results are comparable to a reasonable degree.

CHAPTER 6

CONCLUSIONS

The ever-increasing need for enhancement in CMOS performance has given rise to accelerated research in non-classical multi-gate transistors. Many applications demand ultra low power that can only be achieved by using IDG transistors with high dynamic threshold voltage control factor. The transition between the ON state and the OFF state in a transistor needs to be as sharp as possible. Ideally, the threshold voltage of the device can be dynamically adjusted. Independent double-gated devices have the advantage of being able to use the applied voltage at one gate to control the threshold at the other gate. This structure enables the device threshold voltage to be varied linearly in response to a simple adjustment in the applied back gate voltage.

This research work was aimed at analyzing the performance of independent double-gated transistors, which have the inherent feature of dynamic threshold control. It identified and optimized specific FinFET and FlexFET device designs that have a high dynamic threshold control factor ($f>1$) and a low threshold voltage ($Vt<0.5V$). As a part of this research work, a new surface potential-based analytical model has been developed to calculate the electrical characteristics of IDG-FinFET and IDG-FlexFET. A Verilog-A compact model from the BSIM group at UC Berkeley suitable for use in production SPICE simulators has been modified to capture the inherent asymmetry in the structure of an IDG-FlexFET, in order to facilitate simulations and advanced IC design using this device.

6.1. Surface Potential-Based Analytical Model

Typically, both SOI and bulk device researchers have used threshold-based models. Recent compact models, such as PSP, HiSIM, and BSMG, have introduced a surface potential approach to model symmetrical devices as opposed to the threshold voltage-based approach. Threshold voltage is the top gate voltage at which the device is turned 'ON'. For this work the threshold voltage was defined as the voltage where the drain current equals a magnitude of 10^{-7}A (W/ L). The dynamic control factor was defined as the rate at which the threshold voltage changes in response to the change in bottom gate voltage in the region of VBG=0. For a given device it is desirable to have a low threshold voltage and a high dynamic control factor, in order to achieve ultra low power circuit designs. In view of the scaling device dimensions, oxide and silicon channel thicknesses used in simulations were in the sub 10 nm range. Different combinations of top gate and bottom gate materials (work functions) have been investigated to optimize the IDG MOSFET designs like IDG-FinFET and IDG-FlexFET in terms of threshold voltage and dynamic threshold voltage control factor behaviors.

Six different combinations of top and bottom gate work functions were modeled, including varying the silicon and oxide thicknesses. Each of these six cases can be divided into three categories based upon the level of asymmetry in the work functions used for the top and bottom gates. The performance metrics were low nominal threshold voltage, less than 0.5V and high dynamic control factor, greater than 1.0. The trends for these metrics were recorded for bottom gate voltages of -0.5V, 0V, and 0.5V. The simulations were carried out in MATLAB.

The dynamic threshold control factor in all three categories: symmetrical, half asymmetrical and fully asymmetrical was greater than unity for all of the FlexFET designs. This can be attributed to the inherent asymmetry in the FlexFET structure, which results in stronger channel control by the bottom gate. The dynamic threshold control factor for FinFET was lower in all cases considered, but best for the fully asymmetrical work functions case. Of the FlexFET cases considered, both half and fully asymmetrical cases met the desired criteria. The following fundamental conclusion is derived based on this analytical work: **Both an asymmetrical device structure and asymmetrical top and bottom gate work functions are needed to permit effective threshold control for ultra low power applications.**

6.2. Compact Model for IDG-FlexFET

A compact model is a powerful tool for circuit and process designers to analyze and estimate the behaviors of devices that are yet to be fabricated. By optimizing the device physics using the computer aided design tools, better device models can be developed. IDG-FlexFET is non-classical device structure that was introduced only in the year 2003. There is a lot of opportunity for further research on this device in order to explore the advantages it has to offer. With the analytical work done as a part of this research, it has been established that IDG-FlexFET is highly suitable for ULP applications owing to it high dynamic threshold control factor. This research work modified an existing Verilog-A code from BSIM group at UC Berkeley for independent double gated devices to also work for IDG-FlexFET, by modeling the bottom gate as a

JFET, and thus come up with a compact model that specifically captures the behavior of IDG-FlexFET.

The effects of varying oxide and silicon film thickness, as generated by the compact model have been compared with those generated by the analytical model. It has been observed that the results from the compact model follow that of the analytical model very closely in case of half-asymmetry and full-asymmetry cases when compared to the symmetrical case.

The results generated by the compact model with it full features, such as short channel effects, quantum mechanical effects, output conductance model, velocity overshoot model, GIDL, DIBL, Body doping effects, Drain Saturation Voltage, Mobility degradation, Channel length modulation, Current degradation factor, have been turned ON to compare the results measured from an IDG-FlexFET. It has been observed that the simulated results are comparable with measured experimental data from ASI, proving that the device physics used to develop the compact model are highly accurate.

6.3. Future Work Recommendations

In this dissertation, IDG-FinFET and IDG-FlexFET have been analytically modeled using a surface potential-based approach and their characteristics have been compared. A compact model has been developed for IDG-FlexFET, keeping in mind the core physics of the transistor.

However at channel dimensions of only a few nanometers effects such as quantum mechanical and non-quasi-static effects, on IDG-FlexFET device structure need to be further investigated.

REFERENCES

[1] J.P. Colinge, *FinFET and Other Multi-gate Transistors,* Springer, 2008.

[2] A. Rambhatla, D.R. Hackler, S.A. Parke, *"Quest for the ultimate sub-50 nm CMOS transistor structure,"* University/Government/Industry Microelectronics Symposium, Proceedings of the 15th Biennial, 30 June-2 July 2003. Pages: 222-225.

[3] J.G. Fossum, W. Zhang, "Performance projections of scaled CMOS devices and circuits with strained Si-on-SiGe channels*," IEEE Transactions on Electron Devices*, Volume 50, Issue 4, April 2003 Page(s):1042 – 1049.

[4] M. Lundstrom, J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation,* Springer, New York, 2005.

[5] Y. Taur, T. H. Ning, *Fundamentals of Modern VLSI Devices,* Cambridge Univ. Press, 1998.

[6] S. Parke, K. DeGregorio, M. Goldston, R. Hayhurst, D. Hackler, A. Horvath, S. Parsa, *"Complementary sidewall-spacer-diffused ultrashallow SD CMOS,"* SOI Conference, 2004 IEEE International.

[7] J. G. Fossum, G. F. Derbenwick, B. L. Gregory, "Design Optimization of Radiation-Hardened CMOS Integrated Circuits," *IEEE Trans on Nuclear Science*, Volume 22, Issue 6, Dec. 1975 Page(s):2208 – 2213.

[8] G. Moore, "Cramming more components onto integrated circuits," *Electronics*, 38, 114 (1965).

[9] T. Skotnicki, G. Merckel, T. Pedron, "The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects," *IEEE Electron Device Letters,* 9, 109 (1988).

[10] T. Skotnicki, "*Heading for decananometer CMOS - is navigation among icebergs still a viable strategy?,*" Proceedings of the 30th European Solid- State Device Research Conference. Frontier Group, Gif-sur-Yvette, France, 19 (2000).

[11] W. Xiong, K. Ramkumar, S.J. Jamg, J.T. Park, J.P. Colinge, "*Self-aligned ground-plane FDSOI MOSFET,*" Proceedings of the IEEE International SOI Conference, 23 (2002).

[12] T. Sekigawa, Y. Hayashi, "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate," *Solid-State Electronics* 27, 827 (1984).

[13] T. Sekigawa, Y. Hayashi, K. Ishii, "Feasibility of very-short-channel MOS transistors with double-gate structure," *Electronics and Communications in Japan*, Part 2. 76-10, 39 (1993).

[14] T. Skotnicki, "*Ultimate scaling of SOI MOSFETs,*" MIGAS Short Course, Villard de Lans, France (2004).

[15] http://www.itrs.net/.

[16] T. Skotnicki, F. Boeuf, R. Cerutti, S. Monfray, C. Fenouillet-Beranger, M. Muller, A. Pouydebasque, "New materials and device architectures for the end-of-roadmap CMOS node," *Materials Science & Engineering B (Solid-State Materials for Advanced Technology)* 124-125, 3 (2005).

[17] C. Fenouillet-Beranger, T. Skotnicki, S. Monfray, N. Carriere, F. Boeuf, "Requirements for ultra-thin-film devices and new materials for the CMOS roadmap," *Solid-State Electronics* 48-6, 961(2004).

[18] T. Skotnicki, J.A. Hutchby, T. King, H.-S.P. Wong, F. Boeuf, "The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits and Devices Magazine* 21-1, 16 (2005).

[19] T. Skotnicki, F. Boeuf, "*CMOS Technology Roadmap − Approaching Uphill Specials,*" Proceedings of the 9th Intl. Symp on Silicon Materials Science and Technology, ECS Volume 2002-2, 720, 2002.

[20] J.P. Colinge, *Silicon-on-Insulator Technology,* Materials to VLSI, 3rd Ed Springer, New York, 2004.

[21] S. Cristoloveanu, S. Li, *Electrical Characterization of Silicon-on-Insulator Materials and Devices,* Springer, New York, 1995.

[22] J.B. Kuo, Ker-Wei Su, *CMOS VLSI Engineering,* Springer, New York, 1998.

[23] S. Parke, *"Comparison of existing & proposed SOI MOSFET device structured for minimizing total dose radiation damage,"* Aerospace Conference, 2004. Proceedings 2004 IEEE, Volume 4, 6-13 Mar 2004 Pages: 2427-2430, Vol. 4.

[24] J. G. Fossum, A. Ortiz-Conde, "Effects of grain boundaries on the channel conductance of SOl MOSFET's," *IEEE Transactions on Electron Devices*, Volume 30, Issue 8, Aug 1983 Page(s):933 – 940.

[25] M. M. Pelella, J. G. Fossum, C. T. Chuang, O. A. Torreiter, H. Schettler, R. Puri, M. B. Ketchen, M. G. Rosenfield, *"Low-temperature off-state bipolar effect in floating-body PD/SOI MOSFETs,"* IEEE International SOI Conference, 2-5 Oct. 2000 Page(s):84 – 85.

[26] D. Weiser, D. Munteanu, S. Cristoloveanu, O. Faynot, J. L. Pelloie, J. Fossum, "*Multiple transient effects in SOI transistors: Systematic measurements and simulation,"* IEEE International SOI Conference, Proceedings, 6-9 Oct. 1997 Page(s):138 – 139.

[27] G. O. Workman, J. G. Fossum, "*Dynamic effects in BTG/SOI MOSFETs and circuits due to distributed body resistance,"* IEEE International SOI Conference, Proceedings, 6-9 Oct. 1997 Page(s):28 – 29.

[28] M. M. Pelella, J. G. Fossum, S. Dongwook, S. Krishnan, K. A. Jenkins, "*Low-voltage transient bipolar effect induced by dynamic floating-body charging in PD/SOI MOSFETs,"* IEEE International SOI Conference, Proceedings, 3-5 Oct. 1995 Page(s):8 – 9.

[29] A. Oblea, R. Hayhurst, D. Wilson, D. Hackler, *"A Silicon-on-Insulator Transistor Resistant to Substrate Potential,"* IEEE Workshop on Microelectronics and Electron Devices, 20-20 April 2007 Page(s):25 – 26 .

[30] J.P. Colinge, "An SOI voltage-controlled bipolar-MOS device," *IEEE Trans. Electron Devices,* 34, 845, (1987).

[31] S.A. Parke, C. Hu, P.K. Ko, "Bipolar-FET hybrid-mode operation of quarter-micrometer SOI MOSFETs," *IEEE Electron Device Letters*. 14, 234 (1993).

[32] M. Matloubian, "*Analysis of hybrid-mode operation of SOI MOSFETs,*" IEEE International SOI Conference Proceedings, 106, (1993).

[33] T. Douseki, S. Shigematsu, J. Yamada, M. Harada, H. Inokawa, T. Tsuchiya, "A 0.5-V MTCMOS/SIMOX logic gate," *IEEE Journal of Solid-State Circuits* 32, 1604 (1997).

[34] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P.K. Ko, C. Hu, "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation," *Tech. Digest of IEDM,* 809 (1994).

[35] Z. Xia, Y. Ge, Y. Zhao, "*A Study of varied threshold voltage MOSFET (VTMOS) performance and principle,*" Proceedings 22nd International Conference on Microelectronics (MIEL), 1, 159 (2000).

[36] V. Ferlet-Cavrois, A. Bracale, N. Fel, O. Musseau, C. Raynaud, O. Faynot, J.L. Pelloie, "*High frequency characterization of SOI dynamic threshold voltage MOS (DTMOS) transistors,*" Proceedings IEEE Intl. SOI Conference, 24 (1999).

[37] A. Yagishita, T. Saito, S. Inumiya, K. Matsuo, Y. Tsunashima, K. Suguro, "Dynamic threshold voltage damascene metal gate MOSFET (DT-DMGMOS) technology for very low voltage operation of under 0.7 V," *IEEE Transactions on Electron Devices* 49-3, 422 (2002).

[38] J.P. Colinge, J.T. Park, "Application of the EKV model to the DTMOS SOI transistor," *Journal of Semiconductor Technology and Science*, 3-4, 223 (2003).

[39] T. Sakurai, A. Matsuzawa, T. Douseki, *Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications,* Springer, New York, 2006.

[40] T. Sekigawa and Y. Hayashi, "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate," *Solid-State Electronics* 27, 827 (1984).

[41] B. Agrawal, V.K. De, J.M. Pimbley, J.D. Meindl, "Short channel models and scaling limits of SOI and bulk MOSFETs," *IEEE Journal of Solid-State Circuits* 29-2, 122 (1994).

[42] D.J. Frank, S.E. Laux, M.V. Fischetti, "Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?," *Technical Digest of IEDM*, 553 (1992).

[43] D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, "A fully depleted leanchannel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET," *Technical Digest of IEDM*, 833 (1989).

[44] X. Huang, W. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. Choi, K. Asano, V. Subramanian, T. King, J. Bokor, C. Hu, "Sub 50-nm FinFET: PMOS," *Technical Digest of IEDM*, 67 (1999).

[45] D. Hisamoto, W. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. King, J. Bokor, C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices* 47-12, 2320 (2000).

[46] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.Yang, C. Tabery, C. Ho, Q. Xiang, T. King, J. Bokor, C. Hu, M. Lin, D. Kyser, "FinFET scaling to 10 nm gate length," *Technical Digest of IEDM*, 251 (2002).

[47] L. Chang, Y. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, T.J. King, "Extremely scaled silicon nano-CMOS devices," *Proceedings of the IEEE* 91-11, 1860 (2003).

[48] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J.L. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, S. Monfray, "Silicon-on-Nothing (SON)-an innovative process for advanced CMOS," *IEEE Transactions on Electron Devices* 47-11, 2179 (2000).

[49] S. Harrison, P. Coronel, F. Leverd, R. Cerutti, R. Palla, D. Delille, S. Borel, S. Jullian, R. Pantel, S. Descombes, D. Dutartre, Y. Morand, M.P. Samson, D. Lenoble, A. Talbot, A. Villaret, S. Monfray, P. Mazoyer, J. Bustos, H. Brut, A. Cros, D. Munteanu, J.L. Autran, T. Skotnicki, "Highly performant double gate MOSFET realized with SON process," *Technical Digest of IEDM*, 18.6.1 (2003).

[50] J. Pretet, S. Monfray, S. Cristoloveanu, T. Skotnicki, "Silicon-on-nothing MOSFETs: performance, short-channel effects, and backgate coupling," *IEEE Transactions on Electron Devices* 51-2, 240 (2002).

[51] Y. Liu, K. Ishii, T. Tsutsumi, M. Masahara, E. Suzuki, "Ideal rectangular cross-section Si-Fin channel double-gate MOSFETs fabricated using orientation-dependent wet etching," *IEEE Electron Device Letters* 24-7, 484 (2003).

[52] T. Hiramoto, "*Nano-scale silicon MOSFET: towards non-traditional and quantum devices,*" IEEE International SOI Conference Proceedings, 8 (2001) .

[53] Z. Jiao, A.T. Salama, "*A Fully Depleted Delta Channel SOI NMOSFET. Electrochem,*" Society Proceedings 2001-3, 403 (2001).

[54] M.C. Lemme, T. Mollenhauer, W. Henschel, T. Wahlbrink, M. Baus, O. Winkler, R. Granzner, F. Schwierz, B. Spangenberg, H. Kurz, "Subthreshold behavior of triple-gate MOSFETs on SOI Material," *Solid State Electronics* 48-4, 529 (2004).

[55] R. Chau, B. Doyle, J. Kavalieros, D. Barlage, A. Murthy, M. Doczy, R. Arghavani, S. Datta, "*Advanced depleted-substrate transistors: single-gate, double-gate and tri-gate,*" Extended Abstracts of the International Conference on Solid State Devices and Materials (SSDM), 68 (2002).

[56] F.L. Yang, H.Y. Chen, F.C. Cheng, C.C. Huang, C.Y. Chang, H.K. Chiu, C.C. Lee, C.C. Chen H.T. Huang, C.J. Chen, H.J. Tao, Y.C. Yeo, M.S. Liang, C. Hu, "25 nm CMOS Omega FETs," *Technical Digest of IEDM*, 255 (2002).

[57] X. Baie, J.P. Colinge, V. Bayot, E. Grivei, "*Quantum-wire effects in thin and narrow SOI MOSFETs,*" Proceedings IEEE International SOI Conference, 66 (1995).

[58] S. Miyano, M. Hirose, F. Masuoka, "Numerical analysis of a cylindrical thin pillar transistor (CYNTHIA)," *IEEE Transactions on Electron Devices* 39-8, 1876 (1992).

[59] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, F. Masuoka, "Multi-pillar surrounding gate transistor (M-SGT) for compact and high-speed circuits," *IEEE Transactions on Electron Devices* 38-3, 579 (1991).

[60] S. Lee, S. Kim, E. Yoon, C. Oh, I. Chung, D. Park, K. Kim, "Three-dimensional MBCFET as an ultimate transistor," *IEEE Electron Device Letters* 25-4, 217 (2004).

[61] E. Yoon, S. Lee, S. Kim, M. Kim, S.H. Kim, L. Ming, S. Suk, K. Yeo, C. Oh, J. Choe, D. Choi, D. Kim, D. Park, K. Kim, B. Ryu, "Sub 30 nm multi-bridge-channel MOSFET (MBCFET) with metal gate electrode for ultra high performance application," *Technical Digest of IEDM*, 627 (2005).

[62] D. Park, "*3 dimensional GAA transitors: twin silicon nanowire MOSFET and multi-bridge-channel MOSFET,*" Proceedings IEEE International SOI Conference, 131 (2006).

[63] T. Ernst, C. Dupre, C. Isheden, E. Bernard, R. Ritzenthaler, V. Maffini- Alvaro, J. Cluzel, A. Toffoli, C. Vizioz, S. Borel, F. Andrieu, F. De Crecy, V. Delaye, D. Lafond, G. Rabille, J.-M. Hartmann, M. Rivoire, B. Guillaumot, A. Suhm, P. Rivallin, O. Faynot, G. Ghibaudo, S. Deleonibus, "Novel 3D Integration Process for Highly Scalable Nano-Beam Stackedchannels GAA (NBG) CMOSFETs with HfO2/TiN Gate Stack," *Technical Digest of IEDM*, paper 38.4 (2006).

[64] S. A. Tawfik, L. Zhiyu, V. Kursun, "*Independent-gate and tied-gate FinFET SRAM Circuits: Design guidelines for reduced area and enhanced stability,"* Microelectronics, ICM International Conference on 29-31 Dec. 2007 Page(s):171 – 174.

[65] W. Zhang, J. G. Fossum, L. Mathew, D. Yang, "Physical insights regarding design and performance of independent-gate FinFETs," *IEEE Transactions Electron Devices*, on Volume 52, Issue 10, Oct. 2005 Page(s):2198 – 2206.

[66] S. Parke, K. DeGregorio, M. Goldston, R. Hayhurst, D. Hackler, *"FlexFet: A Low-Cost, Rad-Hard Independent-Double-Gate SOI CMOS Technology with Flexible, Dynamic Reconfigurability,"* Aerospace, 2005 IEEE Conference 5-12 March 2005 Pages: 1-8.

[67] S. Parke, K. DeGregorio, M. Goldston, R. Hayhurst, D. Hackler, *"Ultra-low-power dynamic-threshold digital circuits in the FlexFET independently-double-gated SOI CMOS technology,"* Microelectronics and Electron Devices, 2006, WMED'06, IEEE Workshop on 14 April 2006.

[68] S. Parke, K. DeGregorio, M. Goldston, R. Hayhurst, D. Hackler, A. Horvath, S. Parsa, *"FlexFET: a low-cost planar, self-aligned independent-double-gateMOSFET with Flexible, dynamic threshold control,"* Microelectronics and Electron Devices, WMED '05 IEEE Workshop on April, 2005 Pages : 35-37.

[69] K. Modzelewski, R. Chintala, H. Moolamalla, S. Parke, D. Hackler, *"Design of a 32nm Independently-Double-Gated FlexFET SOI Transistor,"* University/Government/Industry Micro/Nano Symposium, UGIM, 17th Biennial 13-16 July 2008 Page(s):64 – 67.

[70] D. Wilson, R. Hayhurst, A. Oblea, S. Parke, D. Hackler, "*Flexfet: Independently-Double-Gated SOI Transistor With Variable Vt and 0.5V Operation Achieving Near Ideal Subthreshold Slope,"* SOI Conference, IEEE International 1-4 Oct. 2007 Page(s):147 – 148.

[71] B. Meek, D. Wilson, "*FlexFET Independently-Double-Gated CMOS for Dynamic Circuit Control,*" ASI WMED 2009 (submitted).

[72] H.K. Lim, J.G. Fossum, "Threshold Voltage of Thin-Film Silicon-On-Insulator (SOI) MOSFETs," *IEEE Trans. Electron Devices*, 30, 1244-1251, 1983.

[73] R. Chintala, "*Design Optimization of a 35nm Independently-Double-Gated Flexfet SOI Transistor,*" Thesis, 2007, TTU.

[74] D. D. Lu, M. V. Dunga, C.H. Lin, A.M. Niknejad, C Hu, "A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation," *IEDM*, Vol.10, No.12, 2007.

[75] W Wu, et al., "Compact Modeling of Junction Current in Dynamically Depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, Vol. 55, No. 11, 2008.

[76] S. Miyamoto, et al., *"Advanced Compact MOSFET Model HiSIM2 Based on Surface Potentials with Minimum Number of Approximation,"* NSTI-Nanotech 2006, 2006.5.

[77] M. V. Dunga et al., "*BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design,*" Proceedings of the VLSI Technology Symposium, 80 (2007).

[78] www.eigroup.org/cmc/.

[79] C Hu, et al., "*Compact Modeling of FinFETs Featuring Independent-Gate Operation Mode,*" IEEE International Symposium on VLSI Technology, Systems and Applications, 2005.

[80] M. V. Dunga, C. H. Lin, X. Xi, D. D. Lu, A. M. Niknejad, C. Hu, "Modeling Advanced FET Technology in a Compact Model," *IEEE Trans. Electron Devices* 53, 1971 (2006).

APPENDIX A

MATLAB CODE

The analytical modeling of IDG-FinFET and IDG-FlexFET to evaluate their performance in terms of threshold voltage and dynamic threshold control factor was carried out in MATLAB. The MATLAB code takes in the Device Dimensions, Work functions, input bias as the inputs and computed the drain current, threshold voltage and the dynamic threshold control factor and plots the same using the surface potential approach. The code used to generate the front and back surface potentials of a double gated transistor, code used to generate the threshold voltage and dynamic threshold control variation with top oxide thickness and silicon film thickness and the code used to generate the drain current variation with front gate voltage for different back gate voltages are presented in this Appendix.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% MATLAB Program to compute the front and back Surface Potentials
%of IDG-FinFET and IDG-FlexFET

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc;
clear all;
close all;

%Constants

q=1.602e-19;          %charge of an electron
ni=1.5e+10;           %intrinsic carrier concentration
absie=8.85e-14;
resie=11.7;
sie=absie*resie;      %Silicon permitivity
Vt=0.0259;            %Thermal Voltage =26mV
Vfbtg=0.56;           %Flat band voltage of the front gate
Vfbbg=0.56;           %Flat band voltage of the bottom gate
Tox=1.5e-7;           %Top Oxide Thickness
Tbox=1.5e-7;          %Bottom Oxide Thickness for IDG-FinFET
%Tbox=0;              %Bottom Oxide Thickness for IDG-FlexFET
Tsi=20e-7;            %Silicon Film Thickness
Vch=0;                %Channel Potential

%Process

ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox/Tsi;
rb=12*Vt*Tbox/Tsi;
Vtg=0:0.1:2;
stepmax=10000;

for i=1:21
   Vbg=Vtg(i);
   k1 = Vtg(i)-Vfbtg-Vch-ro;
   k2 = Vbg-Vfbbg-Vch-ro;
   x_new=fsolve(@(x) New_func(x,Vt,rb,rt,k1,k2),[239;567]);
   fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
   al=abs(x_new(1));   %alpha
   bt=abs(x_new(2));   %beta

   %Computing the surface potential at the top and the bottom by plugging in
```

```
    %the values of alpha and beta

    spf(i)=(Vtg(i)-Vfbtg-12*(Tox*Vt*bt/Tsi)*coth(al-bt));     %Surface Potential of front
gate @x=-Tsi/2
    spb(i)=Vbg-Vfbbg+12*(Tbox*Vt*bt/Tsi)*coth(al+bt);        %Surface Potential of the
back gate @x=Tsi/2
end
figure(1)
plot(Vtg,spf,'r*','MarkerSize',12)
hold on
xlabel('Front Gate Volatge (V)')
ylabel('Surface Potential')
title('Surface potential Vs Front gate voltage')
plot(Vtg,spb,'b','LineWidth',2)
legend('Front SP','Back SP');
hold off
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Plotting Threshold Voltage and Dynamic Threshold Control Factor f
% Taking Vt=Vtg @Id=1e-7, for both IDG-FlexFET & IDG-FinFET
%Tox being varied from 1nm -10 nm
%f computed as dVt/dVbg
%Vt plotted for Vbg=0.5, Vbg=0,Vbg=-0.5

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc;
clear all;
close all;

%Constants

q=1.602e-19;          %charge of an electron
ni=1.5e+10;           %intrinsic carrier concentration
permfs=8.85e-14;
resie=11.7;
sie=permfs*resie;       %Silicon permitivity
oxe=3.9*permfs;         %Gate Oxide Permitivitty
Vds=0.1;              %Voltage bias at the bottom gate
Vt=0.0259;             %Thermal Voltage =26mV
Tsi=10e-7;            %Silicon Film Thickness
W=1e-4;               %Gate Width
L=30e-7;              %Gate Length
u=600;                %Mobility coefficient
Vch=0;                %Channel Potential
Tox=1e-7:1e-7:10e-7;    %Top Oxide Thickness
Toxax=1:1:10;
nb=max(size(Tox));
Vfbtg=0.03;           %Flat band voltage of the front gate
Vfbbg=0.58;            %Flat band voltage of the bottom gate

%Plotting Vt Vs Tox, Vt=Vtg @ Id=1e-7-FinFET
%Vbg=0.5;
tic
Vbg=0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=Tox(i);
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
```

```
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox(i);
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
      end

    end
   Vthc(i)=Vtg;

end
t1=toc;
figure(1)
plot(Toxax,Vthc,'bs-')
xlswrite('tox_m_p', Vthc', 'B2:B11')
hold on
```

```
%Vbg=0;
tic
Vfbtg=0.03;            %Flat band voltage of the front gate
Vfbbg=0.58;             %Flat band voltage of the bottom gate
Vbg=0;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=Tox(i);
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox(i);
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
```

```
        end

     end
    Vtha(i)=Vtg;

end
t2=toc;
figure(1)
plot(Toxax,Vtha,'b*-')
xlswrite('tox_m_p', Vtha', 'C2:C11')
hold on
%Vbg=-0.5;
tic
Vbg=-0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=Tox(i);
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox(i);
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
```

```
        fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
        fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
        Ids=(2*u*W/L)*(fs-fd);

        if ((Ids>=1e-7) && (Ids<=2e-7))
           break;
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vthb(i)=Vtg;

end
t3=toc;
figure(1)
plot(Toxax,Vthb,'bo-')
xlswrite('tox_m_p', Vthb', 'D2:D11')
xlabel('Top Oxide Thickness in nm')
ylabel('Threshold Voltage')
title('Vth Vs Tox Tsi=10nm,Vds=0.1,TG=M,BG=P')
fa=(Vtha-Vthb)/(-0.5);
xlswrite('f_m_p', fa', 'B2:B11')

figure(2)
plot(Toxax,fa,'b')
hold on
figure(3)
[AXa,H(1),H(2)]=plotyy(Toxax,Vthc,Toxax,fa);
set(AXa,{'YLimMode'},{'auto'}) ;
hold on
fa=0;
Vtha=0;
Vthb=0;

%Plotting Vt Vs Tox, Vt=Vtg @ Id=1e-7-FlexFET
tic
Vbg=0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=0;
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
rb=12*Vt*Tbox/Tsi;
```

```
Coxt=oxe/Tox(i);

    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
      end

    end
   Vthc1(i)=Vtg;

end
t4=toc;
figure(1)
plot(Toxax,Vthc1,'rs-')
xlswrite('tox_m_p', Vthc1', 'E2:E11')
hold on
%Vbg=0;
```

```
tic
Vbg=0;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=0;
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox(i);

    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
      end
       end
   Vtha(i)=Vtg;
```

```
 end
t5=toc;
figure(1)
plot(Toxax,Vtha,'r*-')
xlswrite('tox_m_p', Vtha', 'F2:F11')
hold on
%Vbg=-0.5;
tic
Vbg=-0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
Tbox=0;
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox(i)/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox(i);

    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox(i)*Vt*bts/Tsi)*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox(i)*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);
```

```
        if ((Ids>=1e-7) && (Ids<=2e-7))
           break;
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vthb(i)=Vtg;

end
t6=toc;
figure(1)
plot(Toxax,Vthb,'ro-')
xlswrite('tox_m_p', Vthb', 'G2:G11')
%legend('FinFET, Vbg=0.5','FinFET, Vbg=0','FinFET=-0.5','FlexFET,
Vbg=0.5','FlexFET, Vbg=0','FlexFET=-0.5')
hold off
fb=(Vtha-Vthb)/(-0.5);
xlswrite('f_m_p', fb', 'C2:C11')

figure(2)
plot(Toxax,fb,'r')
xlabel('Top Oxide Thickness in nm')
ylabel('Dynamic Control Factor - f')
title('f Vs Tox,Tsi=10nm,Vds=0.1,TG=M,BG=P')
legend('FinFet','FlexFET')
hold off
figure(3)
[AX,H(3),H(4)]=plotyy(Toxax,Vthc1,Toxax,fb);
set(AX,{'YLimMode'},{'auto'})
xlabel('Top Oxide Thickness in nm')
ylabel(AX(1),'Threshold Voltage(V)')
ylabel(AX(2),'Dynamic Control Factor')
line(Toxax,fb,'Parent',AXa(2))
set(H(3),'marker','*');
set(H(4),'marker','*');
title('Tox Vs Vt & f,Tsi=10nm,Vds=0.1,TG=M,BG=P')
legend(H,'FinFET-Vt','FinFET-f','FlexFET-Vt','FlexFET-f')
hold off
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Plotting Threshold Voltage and Dynamic Threshold Control Factor f
% Taking Vt=Vtg @Id=1e-7, for both IDG-FlexFET & IDG-FinFET
%Tsi being varied from 6nm - 30 nm
%f computed as dVt/dVbg
%Vt plotted for Vbg=0.5, Vbg=0,Vbg=-0.5

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc;
clear all;
close all;

%Constants

Vfbtg=0.03;             %Flat band voltage of the front gate
Vfbbg=0.58;              %Flat band voltage of the bottom gate
q=1.602e-19;            %charge of an electron
ni=1.5e+10;             %intrinsic carrier concentration
permfs=8.85e-14;
resie=11.9;
sie=permfs*resie;       %Silicon permitivity
oxe=3.9*permfs;          %Gate Oxide Permitivitty
Vds=0.1;                %Voltage bias at the bottom gate
Vt=0.0259;              %Thermal Voltage =26mV
W=1e-4;                 %Gate Width
L=30e-7;                %Gate Length
u=600;                 %Mobility Coeeficient
Vch=0;                 %Channel Potential
Tox=3e-7;               %Top Oxide Thickness
Tbox=3e-7;               %Bottom Oxide Thickness
%Tbox-0;                %Bottom Oxide Thickness for IDG-FlexFET
Tsi=6e-7:3e-7:30e-7;     %Silicon Film Thickness
Tsiax=6:3:30;
nb=max(size(Tsi));

%Plotting Vt Vs Tsi, Vt=Vtg @ Id=1e-7-FinFET
%Vbg=0.5;
tic
Vbg=0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
```

```
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
      end

    end
   Vthc(i)=Vtg;

end
t1=toc;
figure(1)
plot(Tsiax,Vthc,'bs-')
```

```
xlswrite('tsi_m_p', Vthc', 'B2:B10')

hold on

%Vbg=0;
tic
Vbg=0;
dvtg=0.005;
for i=1:nb
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
```

```
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vtha(i)=Vtg;

end
t2=toc;
figure(1)
plot(Tsiax,Vtha,'b*-')
hold on
xlswrite('tsi_m_p', Vtha', 'C2:C10')

%Vbg=-0.5;
tic

Vbg=-0.5;
dvtg=0.005;
for i=1:nb
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;

      while(1==1)
        %Computing alpha & beta at the source end, Vch=0
        k1s = Vtg-Vfbtg-Vch-ro;
        k2s = Vbg-Vfbbg-Vch-ro;
        x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
        %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
        als=abs(x_new(1));   %alpha
        bts=abs(x_new(2));   %beta

        %Computing alpha & beta at the drain end, Vch=Vds
        k1d = Vtg-Vfbtg-Vds-ro;
        k2d = Vbg-Vfbbg-Vds-ro;
        x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
        %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
        ald=abs(x_new(1));   %alpha
        btd=abs(x_new(2));   %beta

        %Computing the drain current
```

```
        sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
        spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
        qstoti=Coxt*(Vtg-Vfbtg-sps);
        qdtoti=Coxt*(Vtg-Vfbtg-spd);
        fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
        fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
        Ids=(2*u*W/L)*(fs-fd);

        if ((Ids>=1e-7) && (Ids<=2e-7))
           break;
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vthb(i)=Vtg;

end
t3=toc;
figure(1)
plot(Tsiax,Vthb,'bo-')
xlswrite('tsi_m_p', Vthb', 'D2:D10')

fa=(Vtha-Vthb)/(-0.5);
xlswrite('f_m_p', fa', 'B2:B10')

figure(2)
plot(Tsiax,fa,'b')
hold on
figure(3)
[AXa,H(1),H(2)]=plotyy(Tsiax,Vthc,Tsiax,fa);
set(AXa,{'YLimMode'},{'auto'}) ;
hold on
Vtha=0;
Vthb=0;

%Plotting Vt Vs Tsi, Vt=Vtg @ Id=1e-7-FlexFET
%Vbg=0.5;
tic
Vbg=0.5;
dvtg=0.005;
Tbox=0;
for i=1:nb
```

```
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);

      if ((Ids>=1e-7) && (Ids<=2e-7))
         break;
      else
      Vtg=Vtg+dvtg;
      end

    end
   Vthc(i)=Vtg;

end
t4=toc;
```

```
figure(1)
plot(Tsiax,Vthc,'rs-')
xlswrite('tsi_m_p', Vthc', 'E2:E10')


%Vbg=0;
tic
Vbg=0;
dvtg=0.005;
Tbox=0;
for i=1:nb
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current

      sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
      spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
      qstoti=Coxt*(Vtg-Vfbtg-sps);
      qdtoti=Coxt*(Vtg-Vfbtg-spd);
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
      Ids=(2*u*W/L)*(fs-fd);
```

```
        if ((Ids>=1e-7) && (Ids<=2e-7))
           break;
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vtha(i)=Vtg;
end
t5=toc;
figure(1)
plot(Tsiax,Vtha,'r*-')
xlswrite('tsi_m_p', Vtha', 'F2:F10')


%Vbg=-0.5;
tic
Vbg=-0.5;
dvtg=0.005;
Tbox=0;
for i=1:nb
Vtg=0;
ro=Vt*log((2*sie*Vt)/(q*ni*(Tsi(i))^2));
rt=12*Vt*Tox/Tsi(i);
rb=12*Vt*Tbox/Tsi(i);
Coxt=oxe/Tox;
    while(1==1)
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg-Vfbtg-Vch-ro;
      k2s = Vbg-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg-Vfbtg-Vds-ro;
      k2d = Vbg-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[7;2]);
      %fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta
```

```
        %Computing the drain current

        sps=(Vtg-Vfbtg-12*(Tox*Vt*bts/Tsi(i))*coth(als-bts));
        spd=(Vtg-Vfbtg-12*(Tox*Vt*btd/Tsi(i))*coth(ald-btd));
        qstoti=Coxt*(Vtg-Vfbtg-sps);
        qdtoti=Coxt*(Vtg-Vfbtg-spd);
        fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qstoti);
        fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-
Vt*(5*sie*Vt/Tsi(i))*log((5*sie*Vt/Tsi(i))+qdtoti);
        Ids=(2*u*W/L)*(fs-fd);

        if ((Ids>=1e-7) && (Ids<=2e-7))
           break;
        else
        Vtg=Vtg+dvtg;
        end

     end
    Vthb(i)=Vtg;

end
t6=toc;
figure(1)
plot(Tsiax,Vthb,'ro-')
xlswrite('tsi_m_p', Vthb', 'G2:G10')

xlabel('Silicon Thickness in nm')
ylabel('Threshold Voltagein V')
title('Vth Vs Tsi Tox=Tbox=3nm,Vds=0.1,TG=M,BG=P ')
legend('FinFET,Vbg=0.5','FinFET,Vbg=0','FinFET,Vbg=-
0.5','FlexFET,Vbg=0.5','FlexFET,Vbg=0','FlexFET,Vbg=-0.5')
hold off
fb=(Vtha-Vthb)/(-0.5);
xlswrite('f_m_p', fb', 'C2:C10')

figure(2)
plot(Tsiax,fb,'r')
xlabel('Silicon Thickness in nm')
ylabel('f')
title('f Vs Tsi,Tox=Tbox=3nm,Vds=0.1,TG=M,BG=P')
legend('FinFET','FlexFET')
hold off
figure(3)
[AX,H(3),H(4)]=plotyy(Tsiax,Vthc,Tsiax,fb);
```

```
set(AX,{'YLimMode'},{'auto'})
xlabel('Sililcon Thickness in nm')
ylabel(AX(1),'Threshold Voltage in V')
ylabel(AX(2),'Dynamic Control Factor')
line(Tsiax,fb,'Parent',AXa(2))
set(H(3),'marker','*');
set(H(4),'marker','*');
title('Tsi Vs Vt & f,Tox=Tbox=3nm,Vds=0.1,TG=M,BG=P')
legend(H,'FinFET-Vt','FinFET-f','FlexFET-Vt','FlexFET-f')
hold off
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Drain Current Vs Drain Voltage for
%IDG-FinFET and IDG-FlexFET
%SP calculated separately at source and drain ends

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clc;
clear all;
close all;
%FinFET
%Constants

q=1.602e-19;          %charge of an electron
ni=1.5e+10;           %intrinsic carrier concentration
permfs=8.85e-14;
resie=11.7;
sie=permfs*resie;
oxe=3.9*permfs;       %Gate Oxide Permitivitty
Vds=0.1;              %Voltage bias at the bottom gate
Vt=0.0259;            %Thermal Voltage =26mV
Vfbtg=0.56;           %Flat band voltage of the front gate
Vfbbg=0.03;           %Flat band voltage of the bottom gate
Tox=3e-7;             %Top oxide thickness
Tbox=Tox;             %Bottom oxide thickness for IDG-FinFET
%Tbox=0 ;             %Bottom oxide thickness for IDG-FlexFET
Tsi=10e-7;            %Silicon Film Thickness
W=1e-4;               %Gate Width
L=30e-7;              %Gate Length
u=600;                %Mobility coefficient
Vch=0;                %Channel Potential

%Process

ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox;
a=7;
b=1;

Vtg=0.5:0.1:3;
Vbg=[-0.5 0 0.5];
n=max(size(Vtg));
```

```
for i=1:3
   for j=1:n
      %Computing alpha & beta at the source end, Vch=0
      k1s = Vtg(j)-Vfbtg-Vch-ro;
      k2s = Vbg(i)-Vfbbg-Vch-ro;
      x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[a;b]);
      fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      als=abs(x_new(1));   %alpha
      bts=abs(x_new(2));   %beta

      %Computing alpha & beta at the drain end, Vch=Vds
      k1d = Vtg(j)-Vfbtg-Vds-ro;
      k2d = Vbg(i)-Vfbbg-Vds-ro;
      x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[a;b]);
      fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
      ald=abs(x_new(1));   %alpha
      btd=abs(x_new(2));   %beta

      %Computing the drain current
      sps(j)=(Vtg(j)-Vfbtg-12*(Tox*Vt*bts/Tsi)*coth(als-bts));
      spd(j)=(Vtg(j)-Vfbtg-12*(Tox*Vt*btd/Tsi)*coth(ald-btd));
      qstoti=Coxt*(Vtg(j)-Vfbtg-sps(j));
      qdtoti=Coxt*(Vtg(j)-Vfbtg-spd(j));
      fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
      fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
      Ids(j)=(2*u*W/L)*(fs-fd);
   end

   figure(1)
   plot(Vtg,Ids,'b','LineWidth',2)
   hold on
   Ids=0;
End

%FlexFET

%Process
Tbox=0;
ro=Vt*log((2*sie*Vt)/(q*ni*Tsi^2));
rt=12*Vt*Tox/Tsi;
rb=12*Vt*Tbox/Tsi;
Coxt=oxe/Tox;
for i=1:3
   for j=1:n
      %Computing alpha & beta at the source end, Vch=0
```

```
        k1s = Vtg(j)-Vfbtg-Vch-ro;
        k2s = Vbg(i)-Vfbbg-Vch-ro;
        x_new=fsolve(@(x) alp_bet_sour(x,Vt,rb,rt,k1s,k2s),[a;b]);
        fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
        als=abs(x_new(1));   %alpha
        bts=abs(x_new(2));   %beta

        %Computing alpha & beta at the drain end, Vch=Vds
        k1d = Vtg(j)-Vfbtg-Vds-ro;
        k2d = Vbg(i)-Vfbbg-Vds-ro;
        x_new=fsolve(@(x) alp_bet_drain(x,Vt,rb,rt,k1d,k2d),[a;b]);
        fprintf ('Root = [alpha beta] = [%f %f]\n',x_new(1),x_new(2));
        ald=abs(x_new(1));   %alpha
        btd=abs(x_new(2));   %beta

        %Computing the drain current
        sps(j)=(Vtg(j)-Vfbtg-12*(Tox*Vt*bts/Tsi)*coth(als-bts));
        spd(j)=(Vtg(j)-Vfbtg-12*(Tox*Vt*btd/Tsi)*coth(ald-btd));
        qstoti=Coxt*(Vtg(j)-Vfbtg-sps(j));
        qdtoti=Coxt*(Vtg(j)-Vfbtg-spd(j));
        fs=((qstoti^2)/2*Coxt)+2*Vt*qstoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qstoti);
        fd=((qdtoti^2)/2*Coxt)+2*Vt*qdtoti-Vt*(5*sie*Vt/Tsi)*log((5*sie*Vt/Tsi)+qdtoti);
        Ids(j)=(2*u*W/L)*(fs-fd);
    end

    figure(1)
    plot(Vtg,Ids,'r','LineWidth',2)
    hold on
    xlabel('Front Volatge (V)','fontsize',12,'fontweight','b')
    ylabel('Drain Current (A)','fontsize',12,'fontweight','b')
    title('Drain Current Vs Front voltage','fontsize',12,'fontweight','b')
   legend('FinFET, Vbg=-0.5','FinFET, Vbg=0','FinFET=0.5','FlexFET, Vbg=-
0.5','FlexFET, Vbg=0','FlexFET=0.5')
   set(gca,'fontsize',12,'fontweight','b')
    Ids=0;
end
```

VITA

Manjeera Jeedigunta was born in Guntur, Andhra Pradesh, India, on July 23rd 1982. She did her schooling from St. Ann's High School, Secunderabad. She obtained her Bachelor's degree in electronics and communications from Muffakham Jah College of Engineering, Hyderabad, in 2004. She continued her pursuit for higher education by joining the graduate school at Tennessee Technological University in August 2004 and received her Master of Science degree in Electrical Engineering in August 2006. She enrolled for the PhD program for Electrical Engineering the same year and is now a Candidate for Doctor of Philosophy in Electrical Engineering.