Design Techniques for Low Voltage Wideband Delta-Sigma Modulator

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Abstract

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Submitted by **HE Xiao Yong**

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The development of low-voltage design techniques for analog circuits has recently received a lot of attention due to the continuous shrinking of the supply voltage in modern CMOS technologies, which is projected to reduce to 0.5V for low power applications within ten years in the International Technology Roadmap for Semiconductor. This thesis focuses on developing circuit techniques for low-voltage delta-sigma modulator, a functional block that is widely used in mixed-signal integrated circuits. Several delta-sigma modulators operating at supply voltages below 0.9V have been reported in the open literature. However, none of them supports a signal bandwidth wider than 100kHz with a reasonable performance.

In this thesis, we present research works on developing a low-voltage delta-sigma modulator with a wide signal bandwidth. Specifically, a 0.5V complex low-pass continuous-time (CT) third-order delta-sigma modulator that has a single-sided signal bandwidth of 1MHz, targeting for application in Bluetooth receivers, is presented

without using any internal voltage boosting techniques which are potentially harmful to the reliability of the device. The wide bandwidth of the modulator at this low supply voltage is enabled by a special common-mode (CM) level arrangement in the system level and by new low-voltage amplifies. Realized in a 0.13μm CMOS process the proposed modulator achieves a 61.9-dB peak signal-to-noise-and-distortion ratio at the nominal supply of 0.5V with 3.4mW consumption, and occupies an active area of 0.9mm^2. The modulator achieves the best figure-of-merit among its class.

Furthermore, a new dynamic CM level shifting technique for low-voltage CT delta-sigma modulators that employ a return-to-open feedback DAC is reported in the thesis. The technique maintains a stable CM level at the amplifier's inputs for this type of modulators. Simulation results show that it improves the modulator's SNDR by 11%.

Finally, another new 0.5V fully differential wideband amplifier, which can be used in the wideband modulator, has been proposed. The gate-input two-stage amplifier employs a DC common-mode feedback circuit that uses a Miller-amplified capacitor for its frequency compensation. With the proposed technique, the power consumption of the low-voltage amplifier is drastically reduced.

摘要

参照国际半导体技术的演进蓝图，在未来十年内低电压应用的供电电压将降低到 0.5 伏。由于现代 CMOS 技术工艺尺寸的不断降低激起模拟电路的低电压设计技术的研究。本论文集中讨论低电压过采样调制解调器这一广泛应用于混合信号集成电路功能模块的电路设计技术。公开的文献里已经报道了多个供电电压低于 0.9 伏的过采样调制解调器，但是它们在合理的性能下的带宽都不超过 100k 赫兹。

本论文呈现设计低压宽带过采样调制解调器所进行的工作。具体的说，本论文呈现一个单边信号带宽为 1M 赫兹的三阶连续时间复数低通过采用调制解调器，应用目标为蓝牙接收器，工作电压为 0.5 伏。在本设计中，并没有采用有害于器件的可靠性内部电压推进技术。 本调制解调器在低压下的高宽带特性的取得要归功于系统级的特殊共模电压布局以及一个新的运算放大器。本论文提出的调制解调器实现于 0.13 微米 CMOS 工艺，取得了 61.9dB 的峰值信噪比，供电电压为 0.5V，功耗为 3.4 毫瓦，占用米面积为 0.9 平方毫米，在同类调制解调器中，取得了最佳的性能指数。

此外，本论文提出一个新的动态共模电压提升技术，可用于采用 RTO DAC 的低压连续时间调制解调器中。此技术，在放大器的输入端维持了一个稳定的共模电压。仿真结果表明，采用此技术调的制解调器的信噪比提升了 11%。

最后，论文提出了另一个新的 0.5 伏全差分的宽带运算放大器，可用于宽带调制解调器中。这个栅输入的两级运算放大器，采用了米勒放大电压电容的频率补偿直流共模负反馈电路。这一米勒放大电容频率补偿负反馈技术，极大的降低了低压运放的功耗。

Acknowledgement

This thesis could not be finished without the help and support of many people who are gratefully acknowledged here.

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Chapter 1 Introduction

1.1. Research motivation

For past several decades, the CMOS technology has continuously advanced according to "Moore's law," and it is expected that this scaling will maintain for at least another decade. The International Technology Roadmap for Semiconductor (ITRS) gives us a unique opportunity to look into the projected future of semiconductor technology. The feature-size of CMOS technology is projected to keep scaling deeper into nanoscale dimensions. As a consequence of this technology scaling, functionality density, the intrinsic speed of the devices and the signal processing capability of circuits will continuous increase. Specially, digital signal processing technique is becoming more and more ubiquitous, and digital circuits will continue to benefit from the projected advances in technology feature size. Fig 1.1 shows the projections for the device feature size, supply voltage, and the threshold voltage, based on [1].

However, for nanoscale devices with ultra-thin gate-oxide, the lifetime degrades exponentially with the supply voltage, rather than with the electric field across the oxide layer, as reported in [2][3]. In order to keep reliability, to avoid circuit breakdown, to avoid thermal problems and to reduce power density, the maximum supply voltage has to be scaled down appropriately.

Supply voltage down scaling is mainly driven by the digital circuits since it reduces the power consumption quadratically. Along with a reduction in the supply voltages, the transistor threshold voltage, V_T, is reduced but not as aggressively, in order to maintain good ON/OFF characteristic of the MOS device, and to reduce static leakage levels in digital logic circuits. Even though the power supply voltage scaling is pushed by digital regime, the analog counterpart still needs relatively high supply to maintain performance.

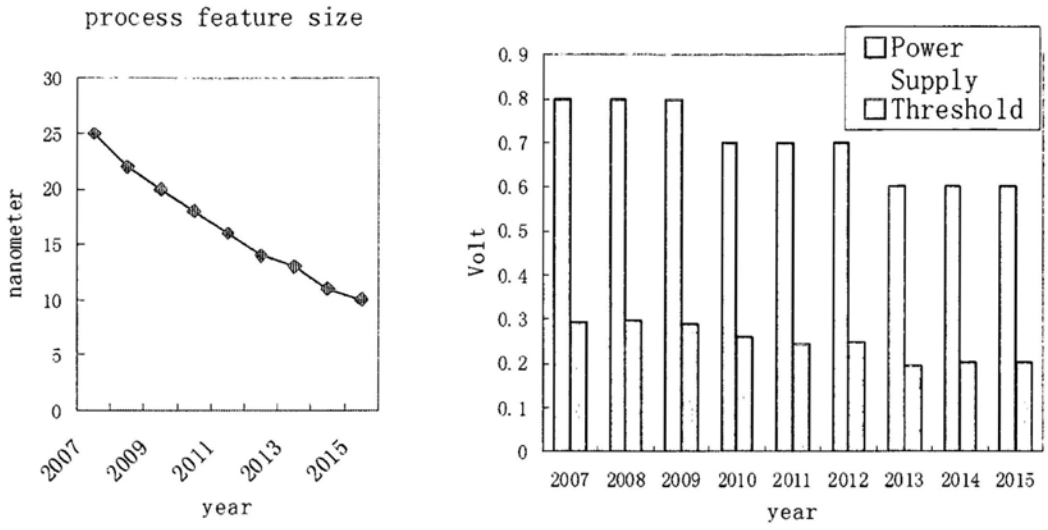


Fig 1.1 Process feature sizes (left), supply and threshold voltage scaling (right)

Digital circuits benefit from both size and power supply scaling. It is not clear, however, that analog circuits will benefit from further technology scaling. Device scaling lowers the supply voltage, thereby leaving less headroom for analog circuit design. Also, a lowered supply voltage means reduced dynamic range unless the noise floor is also reduced, which typically requires increased analog power dissipation [4][5]. This situation will be exacerbated as state-of-the-art CMOS technologies enter the sub-1V supply regime. Moreover, the ITRS roadmap projects supply voltages down to 0.5V and even 0.45V for low power applications in [1]. For energy constrained applications, such as wireless micro-sensors, implantable devices, and devices relying on ambient energy scavenging, true low supply voltages are desirable to achieve the most energy efficient operation.

Definitely it is indispensable for the interfaces, mainly the analog circuits, such as data converters and filters, servicing as a bridge between digital regime and the real analogous world. Nowadays it is very common that both the digital parts and such analog interfaces circuits are integrated on a single chip, so called SoC (System-on-Chip). For systems-on-chip integrated circuits, it is desirable to develop

analog interfaces that operate with supply voltages that remain compatible with the low supply voltages for extremely scaled technologies.

Scaling down of power supply driven by the complex digital systems brings a big challenge on analog circuit design if the SoC maintains a single supply for both such interface circuits and digital parts. Many interested design techniques are investigated and several analog blocks operating in 0.5V power supply are implemented, such as analog fifth-order ecliptic filter [8], 8-bit 10MSps pipeline Analog-to-Digital converter [7], ultra-low power low speed SAR Analog-to-D converter [6]. The resolutions of such Nyquist-rate low-voltage ADCs are limited to about 5 to 8 bits [6][7] (effective number of bits). On the other hand, over-sampling modulators can offer higher resolutions at the expense of speed. As for delta-sigma ($\Delta\Sigma$) modulators operating below 0.9V, researches reported in [9][10] have pushed the SNDR to as high as 77dB, but only over a very limited signal bandwidth ranging from 8kHz to 25kHz, suitable only for voice/audio applications.

This research investigates the design of wideband analog-to-digital converter operating normally at 0.5V. Due to the challenge of the wideband requirements under low power supply, the analog blocks inside the data converter will suffer from circuit imperfections. Considering this, the over-sampling delta-sigma ADC, which is generally believed to be less sensitive to circuit imperfections, is chosen in this research.

A key challenge in low-voltage modulator design is to realize the low-voltage switches that need to pass signals at a level around Vdd/2, e.g. the switches at the input and at the op-amps' outputs. One popular approach is to use techniques that eliminate signal path switches, which include the switched-opamp [11][12][13][14], and switched-RC techniques [10]. The switched-opamp technique offers good performance, but typically requires internal clock voltage boosting for the input sampling switches and sometimes other switches [10][11], which has the potential of degrading the reliability of the circuits. The switched-RC solution does not need internal clock boosting, but the resistors used in the signal path may impose a limit on the speed of circuit. Another solution is to use low-threshold devices to realize the

low-voltage switches [15]. This approach offers a true low-voltage solution, but the leakage of low threshold devices remains a problem to be addressed to improve the performance of the modulators.

The continuous-time (CT) modulator architecture [9][16] is adopted in this research to avoid some of the problems associated with the low-voltage switches, despite the modulator's higher sensitivity to the clock jitter noise. CT modulators do not need switches except in the clocked comparator and the feedback digital-to-analog converters (DAC). In [9], a return-to-open (RTO) DAC concept was introduced that further removes the switches operating at Vdd/2 in the differential DAC by using RTO signaling.

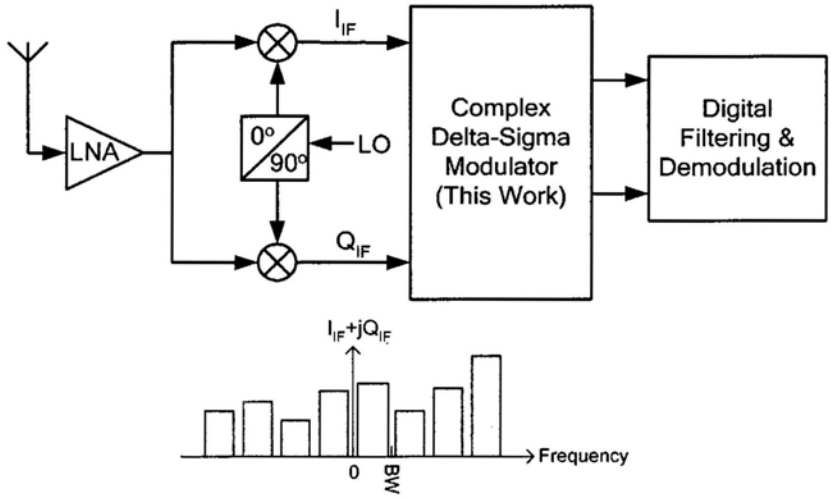


Fig 1.2 A low-IF receiver architecture

The main objective of this research is to develop a true low-voltage delta-sigma modulator with a wide signal bandwidth for analog-digital conversion in wireless receivers. Specifically, we target to design a modulator for direct IF digitization in a Bluetooth receiver that employs a low-IF structure as shown in Fig 1.2. The Bluetooth receiver, which operates in the 2.4 GHz ISM band [25], has a baseband signal bandwidth of 1MHz. In the low-IF receiver structure shown in Fig 1.2, the input of the IF ADC occupies a single-sided band (SSB) from DC to 1MHz, so our modulator will be a complex one. Given that several RF front-ends at low supply voltage have

been demonstrated [17]-[22], the low-voltage modulator presented in this thesis can enable the realization of fully integrated, highly digital low-voltage wireless receivers [23][24].

1.2. Original contribution of this thesis

This thesis is focused on investigating the design techniques of implementing a wideband modulator operating in supply as low as 0.5V. The original contributions of the research work are summarized below.

i. With a proposed CM level arrangement in system level design and high speed amplifier, a continuous-time complex 1-MHz delta-sigma modulator is designed and implemented in 0.13μm CMOS process with standard threshold transistors, without adopting a voltage boost technique which commonly exists in ultra-low voltage circuits. The demonstrated prototype chip achieves 65.7dB dynamic range and consumes 3.4mW in normal conditions test. The full function and performance against variable supply voltage, different input amplitude and temperature, are also provided in this thesis. To our best knowledge, this research is the first one demonstrating the bandwidth of 1MHz modulator with a supply below 0.8V.

ii. A miller compensated DC-CMFB loop is proposed to reduce the low-voltage amplifier's power consumption. The amplifier's performance and stability are verified by extensive simulation. The performance and feasibility of proposed topology are verified by silicon chip.

iii. A CM level shift technique is proposed for low-speed modulator for better performance. The performance of improvement with the proposed technique is verified by simulation.

1.3. Thesis organization

This thesis covers the theoretical analysis of CT delta-sigma A/D converters, the system level and the circuit level design of a wideband, low-voltage CT delta-sigma modulator, and the measurement of the prototype chips.

Chapter 2 reviews the basic concepts of delta-sigma A/D converters and complex signal processing.

Chapter 3 talks about the mapping from discrete time (DT) architecture to CT architecture and discussing the system design of complex CT delta-sigma modulator.

Chapter 4 describes the design issues for delta-sigma modulators with CT implementations. Effects of various non-idealities and potential solutions to deal with them are discussed. Details of the design of the modulator are presented and important simulation results are included.

Chapter 5 covers the layout, measurement setup and measurement results.

Chapter 6 presents a new 0.5V fully differential amplifier topology that does not require replica biasing. Simulation results of the amplifier and the modulator that uses it are included.

Chapter 7 discusses a dynamic common-mode level shift technique proposed for low-voltage CT delta-sigma modulators.

Chapter 8 concludes this thesis and proposes recommendations for future research.

Chapter 2 Overview of delta-sigma modulator and quadrature signal processing

2.1. Basic of delta-sigma modulator

A generic block diagram of oversampling delta-sigma A/D converter (low pass or band pass) is shown in Fig 2.1. For DT modulator, generally an anti-aliasing filter is used to attenuate out-of-band frequency components of the analog input signal so that its output becomes band-limited and the anti-aliasing filter also suppresses the aliasing due to sampling inside the following delta-sigma modulator. For CT modulator, this filter is not necessary because the anti-aliasing is an inherent property of the CT delta-sigma modulator [26]. The delta-sigma modulator converts the input analog signal to a high bit-rate digital signal. The last stage in the Fig 2.1, called the decimation filter and down-sampler, converts the modulator output into a high-resolution digital signal normally at the Nyquist frequency, and the result is signals coded in a large number of bits at the Nyquist rate. This research focuses only on the modulator design and its implementation.

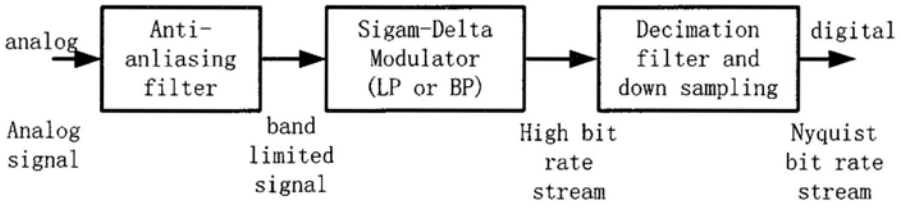


Fig 2.1 Block Diagram of Oversampling Delta-Sigma Modulator

The modulator, as the core of a delta-sigma A/D converter, has a typical topology consisting of a high pass filter, one quantizer and the feedback DAC, shown in Fig 2.2.

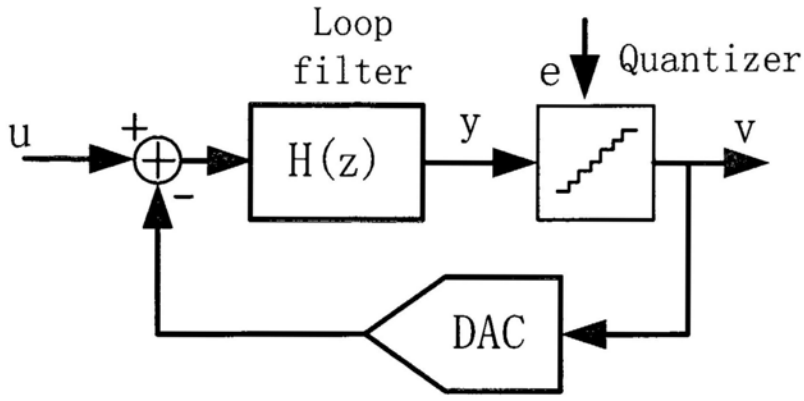


Fig 2.2 General architecture of a delta-sigma modulator

A. Loop filter, H(z)

For a CT modulator, the DT loop filter H(z) should be replaced by a CT loop filter H(s). The loop filter has large gain within the signal band while it attenuates out-of-band signals. The loop filter can be implemented by a switched-capacitor circuit in DT case and an active RC circuit, for instance, in the CT case.

B. Quantizer

The quantizer works as an internal A/D converter to generate the modulator output. Its output can be single-bit or multi-bit (for multi-bit modulator). A single-bit quantizer is realized by a comparator. A multi-bit quantizer is normally realized by a flash ADC for high speed conversion.

C. Feedback DAC

The feedback DAC is employed to convert the digital modulator output to analog and subtract it from the modulator input. For a single bit modulator, the output of the feedback DAC switches between two distinct values. For multi-bit modulator, the output switches among a multiple of values depending on the comparator output. The quantizer is essentially a non-linear circuit and the delta-sigma modulator can not be considered as a linear feedback system in a strict sense. However, the quantization

error inherent in quantizing can be modeled as white noise, and the nonlinear quantizer can thus be approximated as an adder and the modulator is modeled as a linear system as shown in Fig 2.3.

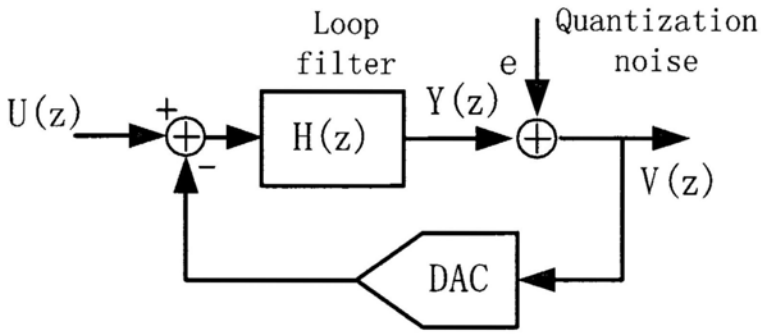


Fig 2.3 z-domain linear model of delta-sigma modulator

In Fig 2.3, U denotes the analog input, and Y is the quantizer's input. V is the modulator output and E is the quantization noise. Considering the DT case, the relationship between U, V and E can be readily derived as

$$V(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z) \tag{2-1}$$

where the STF(z) and NTF(z) are called signal transfer function and noise transfer function, respectively, of the modulator. From the expression of NTF(z), the zeros of NTF(z) are the poles of the H(z). When the loop filter H(z) has a high gain, i.e., $|H(z)| >> 1$, in the band of interest, we have

$$V(z) \approx U(z)$$

In other words, the output signal contains almost unchanged input signal plus quantization noise shaped by NTF(z). Since quantization noise is largely pushed out-of-band by NTF, high in-band signal-to-noise ratio (SNR) can be obtained.

2.2. NTF noise shaping of delta-sigma modulator

In Fig 2.3, if the signal active at the input of the quantizer is sufficiently busy, the quantization error e(n) can be approximated as an random number uniformly distributed between $\pm\Delta$, where delta is the difference between two consecutive quantization level. The mean square value of the quantization noise, i.e., its power, can be calculated from its probability density function as follows:

$$P_e = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{2-2}$$

The noise power is independent of the sampling frequency f_s. Assume the quantization noise is white as shown in Fig 2.4, i.e., having a flat power spectral density (PSD), the PSD can be obtained as:

$$t = \frac{1}{\sqrt{12 f_s}} \tag{2-3}$$

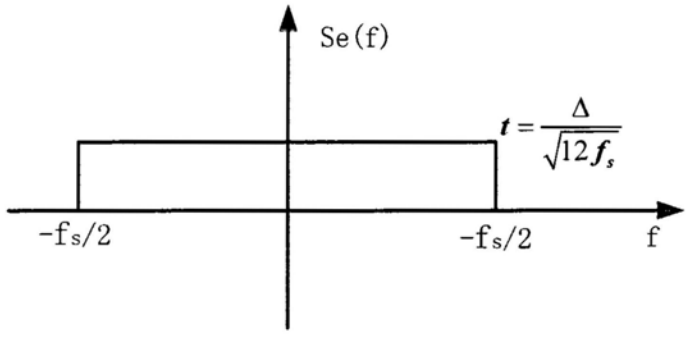


Fig 2.4 Power spectral density of uniformly distributed quantization noise

NTF of the modulator pushes much of the quantization into high frequency, normally much higher than the interest bandwidth, resulting in a high in-band signal-to-noise ratio (SNR).

2.3. First-order and second-order low-pass modulators

Fig 2.5 shows a first-order Δ-Σ modulator architecture when the H(z) in Fig 2.3 is replaced with $\frac{1}{1-z^{-1}}$ and the DAC with z^{-1}. If the quantizer in Fig 2.5 is replaced with another first-order modulator, a second-order Δ-Σ modulator is formed, shown in Fig 2.6.

The system transfer function of first-order and second-order Δ-Σ modulators can be derived from Fig 2.5 and Fig 2.6 in z-domain as,

$$\boldsymbol{V}(z)=\boldsymbol{U}(z)+(1-z^{-1})\boldsymbol{E}(z) \tag{2-4}$$

for the first-order one, and

$$\boldsymbol{V}(z)=\boldsymbol{U}(z)+(1-z^{-1})^2\boldsymbol{E}(z) \tag{2-5}$$

for the second-order one.

The signal transfer functions for both modulators are the same, $\boldsymbol{STF}(z)=1$. In other words, both modulators do not alter their inputs. The noise transfer functions of the first-order and second-order modulators are $(1-z^{-1})$ and $(1-z^{-1})^2$, respectively. The NTF of the second-order modulator is the square of the first-order's NTF, so we expect increased attenuation of quantization noise at low frequencies for the second-order one.

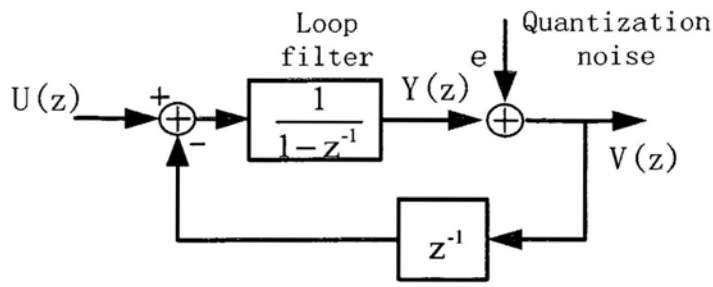


Fig 2.5 First-order delta-sigma modulator

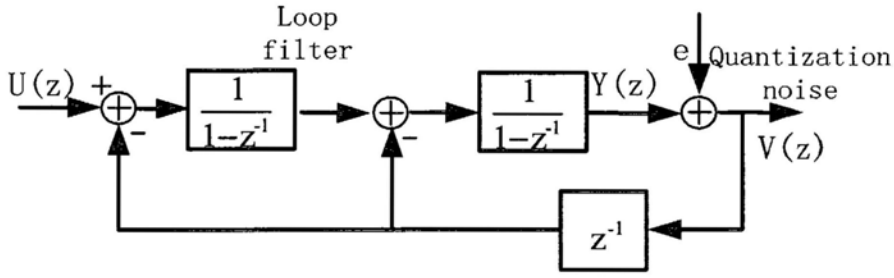


Fig 2.6 Second-order delta-sigma modulator

Quantization noise shown Fig 2.4 is shaped by the modulator's NTF. Output spectrums of two modulators are shown in Fig 2.7 and Fig 2.8, respectively. From the simulated output spectrum, NTF noise shaping of first-order and second-order modulator are 20 dB/decade and 40 dB/decade, respectively.

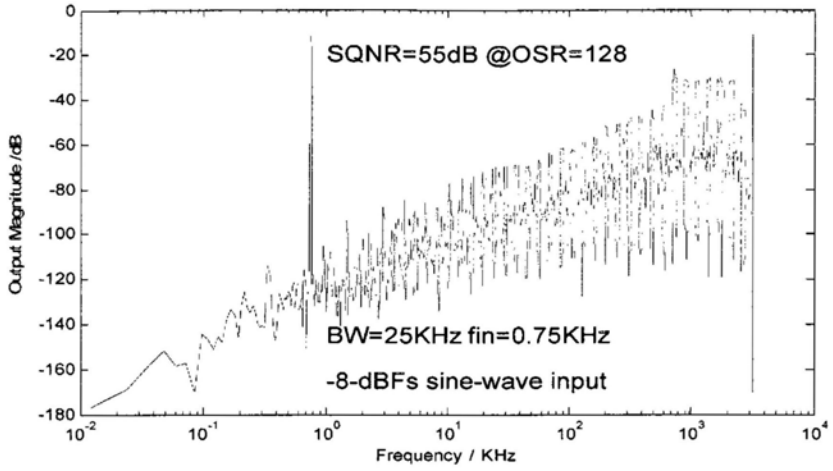


Fig 2.7 Output spectrum of first-order delta-sigma modulator with -8dBFs sine-wave input

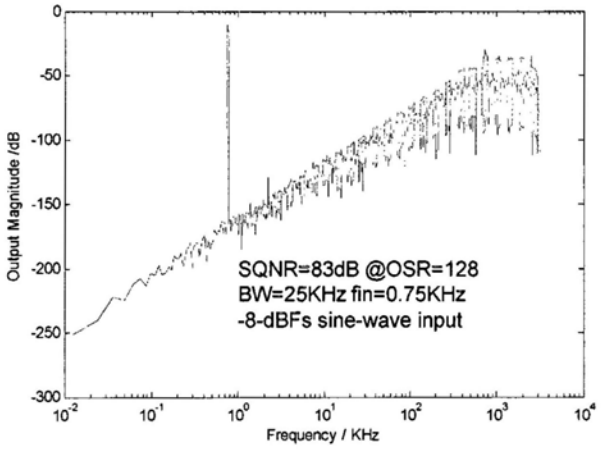


Fig 2.8 Output spectrum of second-order delta-sigma modulator with -8dBFs sine-wave input

For an L^{th} order modulator with a noise transfer function of $(1-z^{-1})^L$, the total in-band quantization noise power can be approximately calculated as [27],

$$q_{rms}^2 = \int_{f_B}^{f_B} \boldsymbol{P_e(f)} \left| \boldsymbol{NTF} \right|^2 \boldsymbol{df}$$

$$= \int_{-f_B}^{f_B} \frac{\Delta^2}{12} \frac{1}{f_s} |NTF|^2 \, df$$

$$\approx \frac{\pi^2 L}{(2L+1)(OSR)^{2L+1}} \frac{\Delta^2}{12} \tag{2-6}$$

where $P_e(f)$ is the quantization noise power spectral density; OSR is the oversampling ratio, defined as the ratio of the sampling frequency to the Nyquist frequency; Δ is the quantizer step size; L is the modulator loop order and f_B is the signal bandwidth.

The dynamic range (DR) is:

$$DR = 10\log\frac{P_s^2}{q_{rms}^2} = 10\log\frac{\frac{1}{2}\frac{\Delta^2}{2}}{\frac{\pi^2 L}{(2L+1)(OSR)^{2L+1}}\frac{\Delta^2}{12}}$$

$$= 10\log[\frac{3(2L+1)}{2\pi^2 L}(OSR)^{2L+1}] \tag{2-7}$$

where P_s^2 is the signal power and $P_s^2 = \frac{1}{2}\frac{\Delta^2}{2}$ when considering single bit quantizer.

The ENOB (effective number of bits) of the converter can be derived from the dynamic range:

$$ENOB = \frac{DR - 1.76}{6.02} \tag{2-8}$$

2.4. Topologies of delta-sigma modulators

Depending on the number of quantizers used in the modulator, there two major types of topologies for delta-sigma modulators, single-stage modulator and multi-stage modulator. From (2-7), one way of increasing the DR and the SNR is to raise the order of the modulator. However, for low OSR modulators, it is no longer

possible to obtain high SNR values in a single quantizer modulator since the permissible input signal amplitude is limited due to stability considerations in high-order loops. The limited input range counteracts the improved noise suppression benefited from higher order loop. Another way to improve the SNR is to use multibit quantizer for the modulator, but this requires a flash ADC and also means to insure the in-band linearity of the internal DAC. Also, the complexity of the quantizer grows exponentially with the number of bits used in the quantizer.

The other way to improve the SNR is to use a multi-stage (also called cascade) topology instead of single stage for the modulator. Multi-stage relies on the quantization noise cancellation rather than filtering to improve the SNR performance.

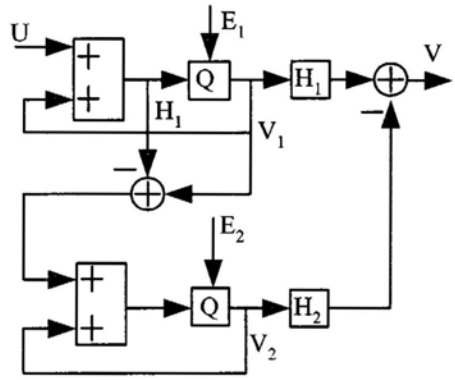


Fig 2.9 Two-stage cascade topology modulator

Fig 2.9 shows a two-stage cascade structure modulator. The output of the first-stage is easily derived from the Fig 2.9

$$\boldsymbol{V}_1(z) = \boldsymbol{STF}_1(z)\boldsymbol{U}(z) + \boldsymbol{NTF}_1(z)\boldsymbol{E}_1(z) \tag{2-9}$$

where $STF_1(z)$ and $NTF_1(z)$ are the signal and noise transfer functions, respectively. The output of signal of the second stage in z-domain is given by

$$\boldsymbol{V}_2(z) = \boldsymbol{STF}_2(z)\boldsymbol{U}(z) + \boldsymbol{NTF}_2(z)\boldsymbol{E}_2(z) \tag{2-10}$$

where $STF_2(z)$ and $NTF_2(z)$ are the signal and noise transfer functions, respectively, of the second stage. The overall output V(z) of the system is

$$V(z) = H_1 V_1 - H_2 V_2 \tag{2-11}$$

with mathematical derivation, if

$$H_1 NTF_1 - H_2 STF_2 = 0 \tag{2-12}$$

The first-stage error $E_1(z)$ is cancelled in the overall output V(z) of the system according to (2-12). Considering (2-12),

$$V(z) = H_1 V_1 - H_2 V_2$$

$$= STF_1 \bullet STF_2 \bullet U - NTF_1 \bullet NTF_2 \bullet E_2 \tag{2-13}$$

In typical cases, both stages contain a second-order loop, and their transfer function is

$$STF_1 = STF_2 = z^{-2} \tag{2-14}$$

And

$$NTF_1 = NTF_2 = (1 - z^{-1})^2 \tag{2-15}$$

The output will become

$$V(z) = z^{-4} U_1 - (1 - z^{-1})^4 E_2 \tag{2-16}$$

From (2-16), the NTF of the overall system is that of a fourth-order single-loop modulator, but the stability is that of a second-order one. Cascade structure increases the signal amplitude while maintain the low order modulator stability so as to achieve high SNR performance. However, the performance of the cascade topology is

contaminated due to the matching problem between mixed-signal (analog and digital) transfer functions $\boldsymbol{H_1 \bullet NTF_1}$ and $\boldsymbol{H_2 \bullet STF_2}$. In reality, $\boldsymbol{H_1}$ and $\boldsymbol{H_2}$ are normally implemented in digital circuits and $\boldsymbol{NTF_1}$ and $\boldsymbol{NTF_2}$ are realized by analog or mixed-signal circuits. The digital logic can be made very accurately while the analog blocks are always relatively coarse especially in submicron digital process. Consequently, since $\boldsymbol{H_1 \bullet NTF_1}$ and $\boldsymbol{H_2 \bullet STF_2}$ are not identical, the first-stage quantization noise $E_1(z)$ will not be cancelled totally. Some portion of $E_1(z)$ will leak to the final modulator output V(z) and may eventually limit the performance. Based on this consideration, second-order loops are normally used as the first stage of multistage topology to reduce the amplitude of the leaked quantization noise. Multi-bit quantizers can also be used to further reduce this leaked error, at the cost of adding DAC mismatch errors. Which topology used depends on the specific applications.

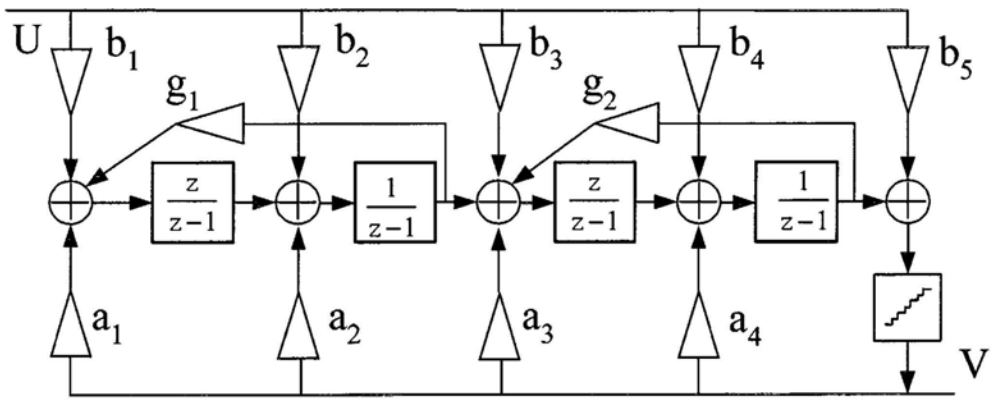


Fig 2.10 Single stage modulator with distributed input and distributed feedback topology

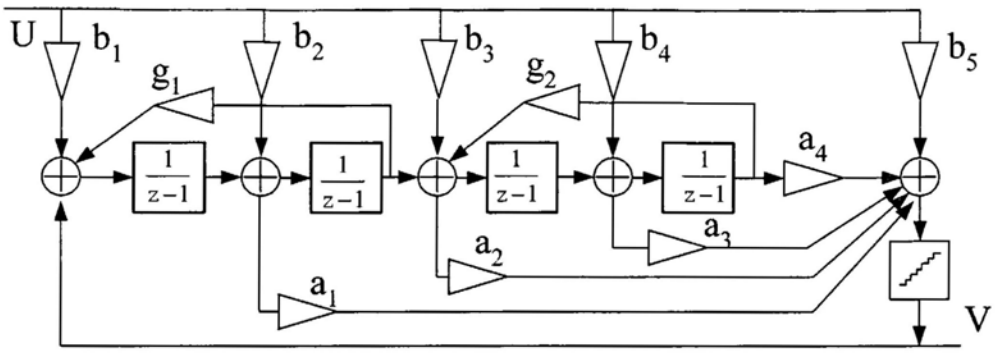


Fig 2.11 Single stage modulator with distributed input and distributed feedforward topology

For single stage modulator topologies, there is only one quantizer. The digital output of the quantizer is the input to the DAC. The output of the DAC is subtracted from the analog input signal and (or) the intermediate integrator outputs.

There are two general single-stage topologies [27]. Cascade of resonators with distributed feedback and distributed input, shown in Fig 2.10; and chain of integrators with feedforward summation and local resonator feedbacks, shown in Fig 2.11.

Both in Fig 2.10 and Fig 2.11, there are two local resonators. The effect of the these resonators is to shift the zeros of the NTF(z), or the poles of the loop filter, to some in-band frequencies other than DC. The overall effect of the zero shift of NTF is to further reduce the in-band quantization noise power and increase the SNR consequently. The optimized zero location of NTF improves the SNR around 3.5dB for second-order modulator and even more for higher order one. This optimum zero-placement technique is very useful especially for wideband high resolution delta-sigma modulators where the oversampling ratios are relatively low.

One shortcoming of these two topologies is that all integrator outputs will contain both input signal as well as filtered quantization noise. This will make the signal swing at each integrator's output large. In many implementation, the distributed input is not used, only the first integrator accepts the input signal; that is $b_i = 0$, for $i > 1$. In this case, since the loop filter does not process the input signal u(n), the requirements

on its linearity will be greatly reduced, and the integrator outputs are considerably reduced, especially if a multi-bit quantizer is used.

It is well known that only first-order modulator is unconditionally stable when single-bit quantizer is used for the single-stage topology. For high order single-stage modulators, the stability can be achieved by methods such as limiting the input signal in stable input range, adding "sensing-and-resetting" circuitry to detect the loop instability and reset the integrators to pull the modulators back to stable status [27].

2.5. Quadrature signal processing

Since this research is to implement a complex CT delta-sigma modulator, a brief review of quadrature, or complex, signal processing is given below.

A quadrature signal is an abstract signal composed of two real signals, I and Q, viewed as a single complex entity $u = I + jQ$. In the context of communications, the real part and imaginary part will be expressed as in-phase (I) and quadrature phase (Q). Often, a trigonometric form is always used to describe a quadrature signal. Fig 2.12 illustrates how a trigonometric form represents a real signal **Error! Reference source not found.**.

Quadrature analog signals are often created via quadrature mixing. In a quadrature down-conversion mixer, a real signals is multiplied by the quadrature signal $e^{-j\omega_{LO}t}$, which we will refer to as the LO (local oscillator), as illustrated in Fig 2.13.

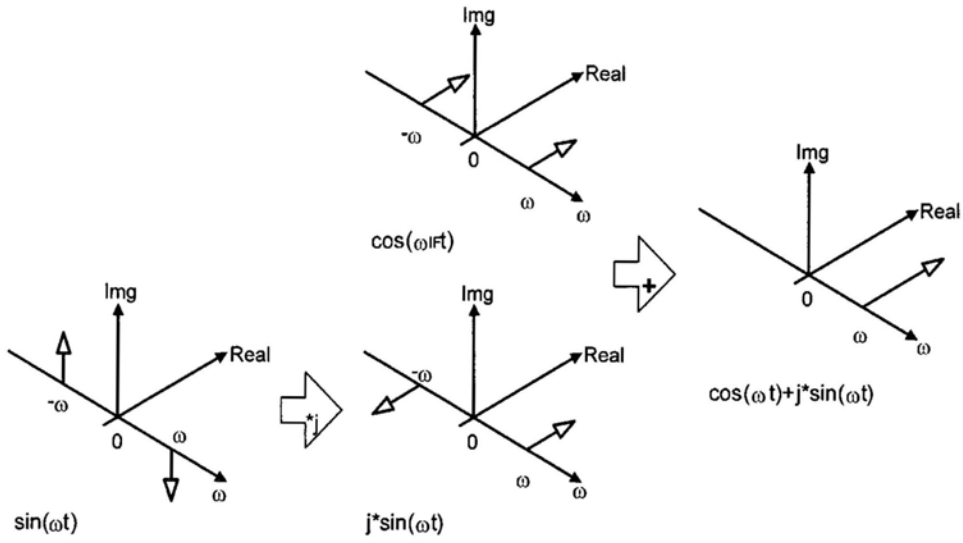


Fig 2.12 Trigonometric format of a real signal

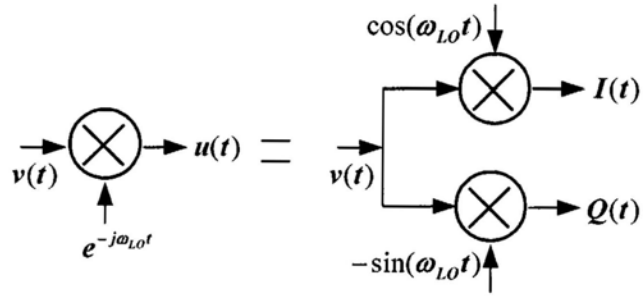


Fig 2.13 Quadrature mixing

Considering that the analog signal input to such a mixer is the real signal $v(t) = A\cos((\omega_{LO} + \omega)t)$, then the output of the mixer is

$$v(t) = A\cos((\omega_{LO} + \omega)t) \times e^{-j\omega_{LO}t}$$

$$= A\frac{e^{j(\omega_{LO}+\omega)t} + e^{-j(\omega_{LO}+\omega)t}}{2} \times e^{-j\omega_{LO}t}$$

$$= \frac{A}{2} e^{j\omega t} + \frac{A}{2} e^{-j(2\omega_{LO}+\omega)t} \tag{2-17}$$

In above expression, the second term will be removed by a low pass filter. A frequency-shifted version of the original signal, will result and center at the angular frequency, ω.

A block diagram of a delta-sigma converter with a built-in quadrature mixer is shown in Fig 2.14. In the upper path the signal is mixed with a cosine function, giving an in-phase output signal. The upper path is referred as I channel. On the other hand, the signal in the lower path is mixed with a sine function, so it results in quadrature-phase and the lower path is referred as Q channel. The two low-pass filters following the mixer are used to remove the high frequency components generating from the mixer and result quadrature signal as

$$v(t) = I_v + jQ_v$$

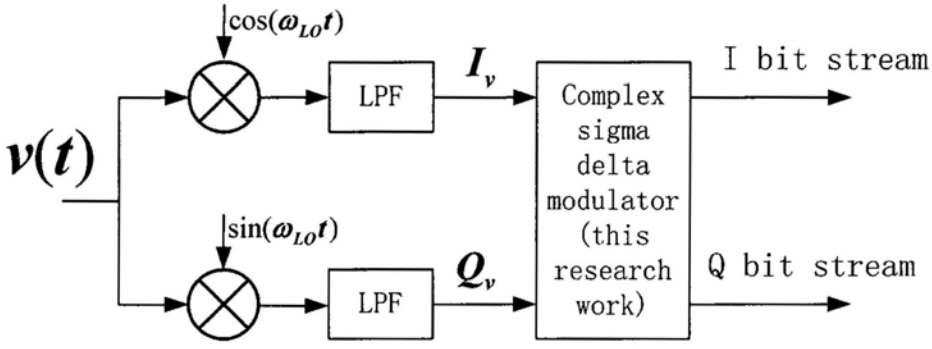


Fig 2.14 Diagram of a complex delta-sigma converter including the quadrature mixer

A complex delta-sigma modulator is used to converter the quadrature signal to digital bit. Fig 2.15 shows the spectrum of signals along I and Q channel and by complex adding of their output (I-j*Q), image are removed and only desired signal remained **Error! Reference source not found.**.

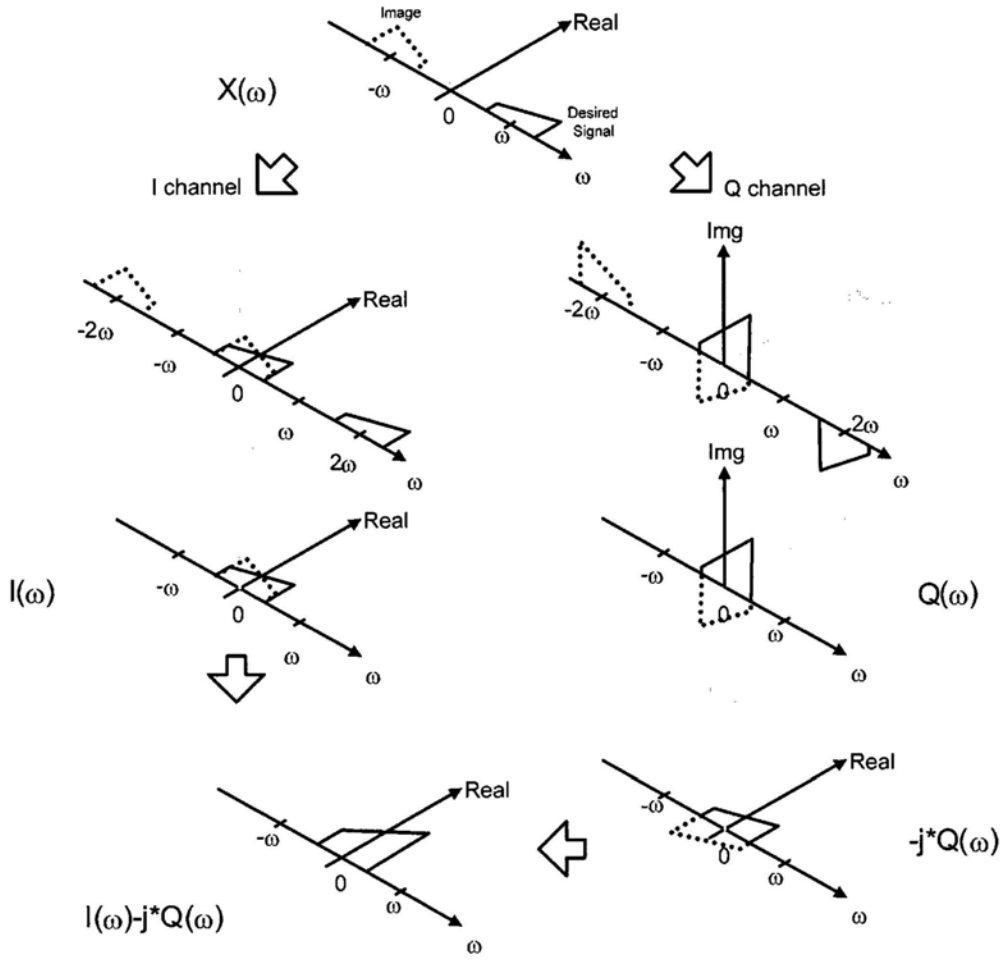


Fig 2.15 Spectrum of signals along the I and Q channels

In summary, this chapter reviews the fundamental of delta-sigma modulators and the basics of quadrature signal processing.

Chapter 3 System design of complex CT delta-sigma modulator

The focus of this research is on low-voltage delta-sigma modulators. It is mentioned in Chapter one that the CT modulator, which avoids the switching challenge commonly existing in low-voltage DT modulator, is selected. Besides, the single-stage architecture is selected as the SNR performance of the multi-stage modulator is affected by the mismatch between the analog and digital circuits as mentioned in Chapter two. This performance decreasing due to the mismatch is more serious for CT modulator than the DT modulator because the matching in DT multistage modulator normally depends on capacitor matching which can be better than 0.1% in current mainstream digital CMOS process. However, the matching in CT modulator is limited by the very coarse time constant that depends on resistor and capacitor variations, and these variations of resistor and capacitor values are up to 13% [29] or even more depending on the process options. Most CT modulators reported in the open literature are of single stage type instead of multistage type, with only a few exceptions [30] [38]. Nonetheless, this is not to say that CT multi-stage architecture is not possible for low-voltage designs. It is still a good alternative research direction and the aforementioned challenges could be solved by circuit-level and/or system-level innovations.

As we have selected the CT single-stage architecture for the desired complex modulator for use in wireless receivers, we present the system-level synthesis of such type of modulator in this chapter.

3.1. Mapping of CT modulators from DT prototypes

The DT Δ-Σ modulator has evolved for several decades since its prelude. Many verified loop filters for DT modulators are available in the literature. The loop filter function of a DT modulator can be found in a straightforward way by using

commercial filter design packages, or with the help of a widely used delta-sigma design toolbox [27]. For the CT delta-sigma modulator, the simplest way to get its loop filter is to pick a DT loop filter *H(z)* meeting the given resolution requirement and then transform it into the equivalent CT loop filter *H(s)*.

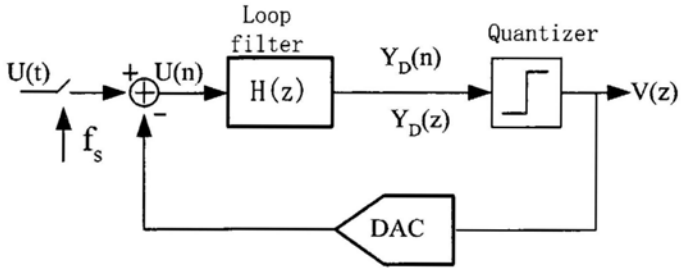


Fig 3.1 Block diagram of DT delta-sigma modulator

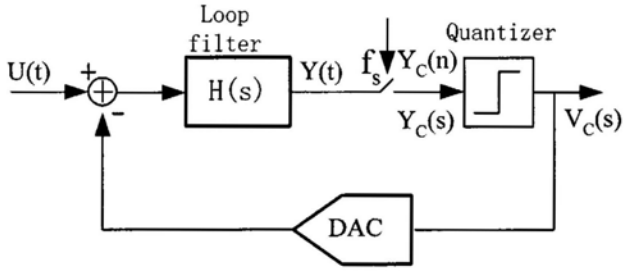


Fig 3.2 Block diagram of CT delta-sigma modulator

Block diagrams of a DT modulator and a CT modulator are shown in Fig 3.1 and Fig 3.2, respectively. Suppose that the same input is applied to the two modulators. If both the CT and DT modulator produce the same sequence of bits in the time domain, then we can say these two modulators are equivalent. Assume that each quantizer makes the same decision about what output bit to produce when fed with the same input. It is guaranteed that the two modulators will produce the same output bit sequences if the inputs to their quantizer are the same at the sampling instants.

To find the equivalences between the DT and CT loop filters, we break the modulator loop at the input of quantizer with zeroed modulator input as shown in Fig 3.3 and Fig 3.4 [31]. The DAC operation of CT modulator is also shown in Fig 3.3,

which is thought of as a discrete-to-continuous converter, taking sample $v(n)$, and producing full-period rectangular pulse. The output pulse of DAC in Fig 3.3 is filtered by the H(s) and then sampled, where it becomes the discrete-time output of the open-loop system $Y_C(t)$, $t = nT_S$.

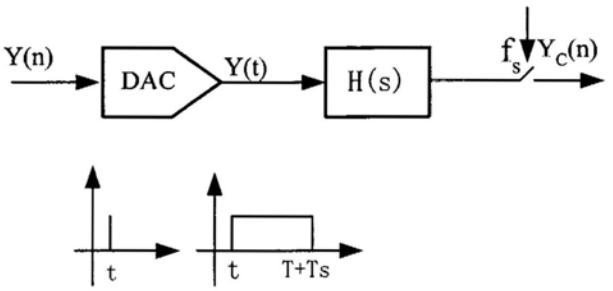


Fig 3.3 Block diagram of open loop of CT modulator

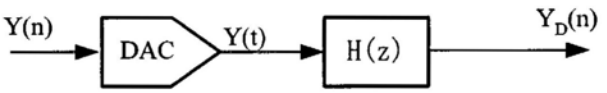


Fig 3.4 Block diagram of open loop of DT modulator

This same-input condition at the sampling instants can be described as,

$$Y_D(n) = Y_C(t)\big|_{t=nTs} \tag{3-1}$$

This can be satisfied if the open loop impulse responses are the same at sampling instants, which can be written as [32]

$$Z^{-1}\{H(z)\} = L^{-1}\{H_{DAC}(s)H(s)\}\big|_{t=nTs} \tag{3-2}$$

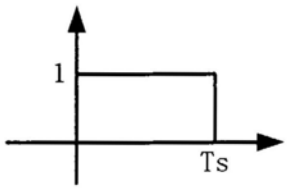
or in the time domain [33]

$$h(n) = [\widehat{r(t)} * h_C(t)]\big|_{t=nTs} \tag{3-3}$$

where $\widehat{r(t)}$ is the impulse response of the DAC in CT modulator, and $h(n)$ and $H_C(t)$ is the impulse response of DT loop filter H(z) and CT loop filter H(s), respectively. This transformation between the DT and CT domains is referred to as the Impulse Invariant Transformation (IIT), as implied by its name [34].

Now if we have a DT modulator with a filter H(z) satisfying the given resolution requirements, we can build a CT modulator with identical noise-shaping behavior by first choosing a DAC pulse shape $\widehat{r(t)}$, and then using (3-2) and (3-3) to find H(s).

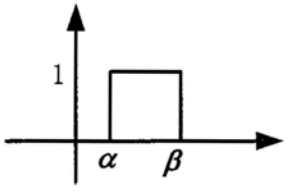
From (3-2) and (3-3), the transformation results depend on the DAC feedback shapes. So we should first define the DAC shapes before performing the mapping from DT to CT. Rectangular-pulsed feedback DAC implementations are predominately incorporated in the CT delta-sigma modulator for several years due to their intrinsic characteristic that their waveforms can be generated simply by switching the feedback current or voltage sources on or off with system clock or its derivative clock. Other possible DAC shapes include linear-decaying DAC and quadratic-decaying DAC [35]. A straight forward way for the mapping is to get their Laplace transform for (3-2). Considering the complexity of their corresponding Laplace transform and the clock generation to control DAC feedback shapes, the rectangular-shaped feedback DAC waveform is most used. Rectangular feedback DAC pulses can be grouped into non-return-to-zero (NRZ) type and return-to-zero (RZ) type, the latter including the special case of half-delay-return-to-zero (HRZ) [36]. The RZ feedback DAC shape produces constant valid output in a certain fraction of a clock period, i.e., from α ($0 \leq \alpha <$Ts) to β ($\alpha < \beta <$Ts). Fig 3.5 and Fig 3.6 show the impulse responses of NRZ and RZ and their corresponding Laplace transform, respectively.



$$\widehat{r_{NRZ}(t)} = \begin{cases} 1, 0 \le t \le Ts \\ 0, otherwise \end{cases} \tag{3-4}$$

$$\widehat{R_{NRZ}(s)} = \frac{1 - e^{-sTs}}{s} \tag{3-5}$$

Fig 3.5 NRZ DAC impulse response and corresponding laplace transform



$$\widehat{r_{RZ}(t)} = \begin{cases} 1, \alpha \le t \le \beta, 0 \le \alpha \le \beta \le Ts \\ 0, otherwise \end{cases} \tag{3-6}$$

$$\widehat{R_{RZ}(s)} = \frac{e^{-\alpha s} - e^{-\beta s}}{s} \tag{3-7}$$

Fig 3.6 RZ DAC impulse response and corresponding laplace transform

Once the DAC feedback pulse shaped is determined and the DT loop filter *H(z)* is defined, the mapping from DT to CT can be done with the following two steps.

Firstly, we expand *H(z)* to a partial fraction expression.

Second, we convert each partial fraction from z-domain to s-domain.

Symbolic mathematical software like Maple [37] can be used to solve (3-2). Table 3-1 summarizes the CT equivalents transformed from DT loop filter from the first to fourth-order when rectangular-shape feedback DACs are used [38] .

Table 3-1 CT equivalents for DT loop filter poles

z-domain pole	CT equivalent with $f_s = 1$
$\frac{1}{z-1}$	$\frac{r_0}{s}, r_0 = \frac{f_s}{\beta - \alpha}$
$\frac{1}{(z-1)^2}$	$\frac{r_1 s + r_0}{s^2}, \; r_0 = \frac{f_s^2}{\beta - \alpha}, \; r_1 = \frac{1}{2}\frac{f_s(\alpha + \beta - 2}{\beta - \alpha})$
$\frac{1}{(z-1)^3}$	$\frac{r_2 s^2 + r_1 s + r_0}{s^3}, \; r_0 = \frac{f_s^3}{\beta - \alpha}, \; r_1 = \frac{1}{2}\frac{f_s^2(\alpha + \beta - 3)}{\beta - \alpha}$ $r_2 = \frac{1}{12}\frac{f_s(\beta(\beta - 9) + \alpha(\alpha - 9) + 4\alpha\beta + 12)}{\beta - \alpha}$
$\frac{1}{(z-1)^4}$	$\frac{r_3 s^3 + r_2 s^2 + r_1 s + r_0}{s^4}, \; r_0 = \frac{f_s^4}{\beta - \alpha}, \; r_1 = \frac{1}{2}\frac{f_s^3(\alpha + \beta - 4)}{\beta - \alpha}$ $r_2 = \frac{1}{12}\frac{f_s^2((\beta - \alpha)^2 + 2\alpha\beta - 12(\beta + \alpha) + 22))}{\beta - \alpha}$ $r_3 = \frac{1}{12}\frac{f_s((\beta^2(\alpha - 2) + \alpha^2(\beta - 2) - 8\alpha\beta + 11(\alpha + \beta) - 12)}{\beta - \alpha}$

3.2. Synthesis for complex CT modulators

The target of this research is to design a low-voltage complex delta-sigma modulator for analog-to-digital conversion in wireless receivers, as shown in Fig 1.2. As shown in Fig 2.14, the signal fed to the modulator is complex, occupying a single-sided band from DC to BW. In this design, the target application is GFSK receivers, and the input signal band is from DC to +1MHz.

The major problem of rectangular-pulsed feedback realization comes from the purity of the sampling clock. The timing jitter in the sampling clock directly influences the comparator decision point and the rise/fall edges of the DAC output. This shift of rise/falle edges will change the quantity of the DAC feedback signals and result in DAC error. Due to the resulting DAC error introducing directly into the modulator input, the timing jitter limits the overall delta-sigma modulator performance. Even though the other feedback pulse shapes [35] are helpful to reduce the DAC error, the circuits as well as the clock scheme controlling the generation of these kinds of DAC feedback signals are complex and difficult to implement at low supply voltage.

Considering the 0.5V target supply voltage of this work, we adopt the rectangular feedback shape DAC for its simplicity. Though multi-bit modulator has relaxed requirements on the clock jitter, it is very challenging to linearize a multi-bit DAC at 0.5V. Furthermore, a 1-bit modulator is perfectly linear.

3.2.1. The DT complex loop filter prototype H(z)

As discussed before, the simplest way of designing H(s) is to map from the loop filter H(z) if the feedback shape DAC is determined.

Now the synthesis of H(s) begins with the selection of a desired DT NTF meeting the requirement. Considering that the achievable unity-gain-bandwidth (UGF) of the 0.5V amplifier, which will be discussed in Chapter 4, is less than 100MHz, the sampling frequency f_s of the modulator is chosen as 64MHz. The bandwidth of interest is 1MHz and thus the oversampling ratio (OSR) is 64, an integer power of 2 which easies the design of the subsequent decimation filter. To minimize the total noise power in the signal band, the zeros are spread over the bandwidth instead of in DC. In this H(z) design, three zeros of the NTF are evenly placed across the signal band at DC, 0.5MHz, and 1MHz, and the poles are selected as the same frequency of the zeros, located at DC, 0.5MHz and 1MHz. Three poles are added to the NTF to

make the maximum amplitude of the NTF to be 1.5, typical value for a stable high-order 1-bit modulator. The magnitude of the pole is defined by

$$\left|\frac{z-1}{p-1}\right|^{order} \leq 1.5,$$

in this case, the order of the modulator is 3. When z=-1, the above equation reach maximum, the magnitude of the pole is

$$|p| = \frac{2}{1.5^{1/3}} - 1$$

Fig 3.7 shows the pole-zero map and frequency response of the designed NTF.

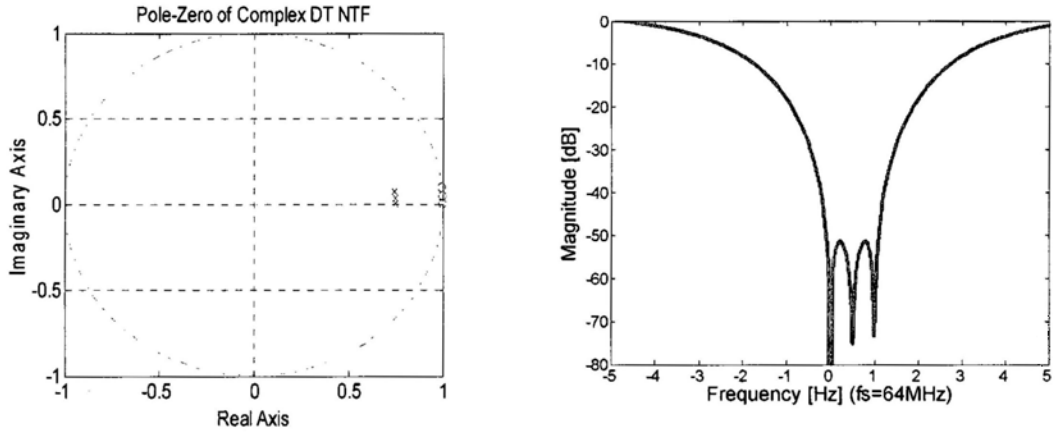


Fig 3.7 Noise Transfer function H(z) (a) pole-zero map; (b) Frequency response.

With Matlab, based on the defined zeros, the created NTF of the modulator, is shown in below

$$\boldsymbol{NTF}(z) = \frac{z^3 - (2.994 + 0.1471\boldsymbol{i})z^2 + (2.983 + 0.2938\boldsymbol{i})z - (0.9892 + 0.1467\boldsymbol{i})}{z^3 - (2.237 + 0.1099\boldsymbol{i})z^2 + (1.665 + 0.164\boldsymbol{i})z - (0.4126 + 0.0612\boldsymbol{i})} \quad (3\text{-}8)$$

Or in zpk format,

$$\mathrm{NTF}(z) = \frac{(z - 1)(z - (0.9988 + 0.0491\mathrm{i}))(z-(0.9952 + 0.0980\mathrm{i}))}{(z-0.7472)\,(z-(0.7463+0.03666\mathrm{i}))\,(z-(0.7436+0.07323\mathrm{i}))} \quad . \quad (3\text{-}9)$$

With H(z)=1-1/NTF(z), the loop filter H(z) is written in

$$H(z)=\frac{-(0.757+0.03719i)z^2+(1.318+0.1298i)z-(0.5766+0.08553i)}{z^3-(2.994+0.1471i)z^2+(2.983+0.2938i)z-(0.9892+0.1467i)} \quad (3\text{-}10)$$

Or in zpk format

$$H(z)=\frac{(-0.757-0.037189i)\ (z-(0.8763-0.0341i))(z-(0.8687+0.1199i))}{(z-1)(z-(0.9988+0.0491i))(z-(0.9952+0.0980i))} \quad (3\text{-}11)$$

3.2.2. Transformation from H(z) to H(s)

Now the DT loop filter H(z) is defined in (3-11). We need to get the CT H(s) from the designed H(z). For the H(z) described by (3-11), there are two couples of complex zero-poles, and the two poles are out of DC. Table 3-1 describes the transformation from DT to CT from first to fourth order when all poles are located in DC. In this modulator system design, though all poles of the loop filter are out of DC, we can still use the impulse invariant DT to CT transformation described by (3-2) and (3-3) with the defined feedback DAC shape. Applying the transformation described in [31], the CT modulator loop filter H(s) is transformed from (3-10) and the transformed result is shown in (3-12)

$$H(s)=\frac{-(1.351+0.03019i)s^2-(0.3655-0.1251i)s-(0.03162-0.01726i)}{s^3-0.1473is^2-0.004819s} \quad (3\text{-}12)$$

Or in zpk format

$$H(s)=\frac{(-1.3509-0.030186i)\ (s+(0.1345+0.03755i))\ (s+(0.1338-0.1362i))}{s\ (s-0.04909i))\ (s-0.09817i))} \quad (3\text{-}13)$$

The NTF of CT modulator can be found from

$$NTF(s)=\frac{1}{1-H(s)} \quad (3\text{-}14)$$

In zpk format

$$\text{NTF(s)} = \frac{\text{s (s-0.04909i)) (s-0.09817i))}}{\text{(s+(1.029-0.01641i)) (s+(0.1614+0.03691i)) (s+(0.1605-0.1376i))}} \quad (3\text{-}15)$$

From (3-15), the CT modulator also creates three zeros in the noise transfer function NTF.

In the above DT to CT transformation, the rectangular feedback DAC pulse shape is adopted, and the RZ type DAC is used for minimizing inter-symbol interference (ISI). The RZ DAC waveform has 50% duty cycle and its rising edge is delayed by 20%Ts (Ts is the clock period) from the starting moment of each clock cycle. According to Fig 3.6, α and β equal to 0.2 and 0.7, respectively, for the DAC adopted here.

3.2.3. The synthesized complex CT modulator

Considering the loop filter described in (3-13), the core terms of the loop filter are, $\frac{1}{s}$, $\frac{1}{(s-j0.04909)}$ and $\frac{1}{(s-j0.09817)}$. The first one, $\frac{1}{s}$, can be implemented by a regulator integrator. The second and third terms, having complex coefficients, can be realized by a quadrature resonator structure shown in Fig 3.8.

The transfer function of the Fig 3.8 is

$$H(s) = \frac{I_{out} + jQ_{out}}{I_{in} + jQ_{in}} = \frac{\omega_0}{s - j\omega_0} \quad (3\text{-}16)$$

In Fig 3.8, real and imaginary parts are cross coupled to implement the imaginary coefficient. The loop filter H(s) given in (3-13) can be implemented by a distributed feedback topology or a feed-forward one. The latter, having smaller signal swing at integrators outputs [39], is not chosen because it requires accurate transconductance cells which are hard to design at 0.5V.

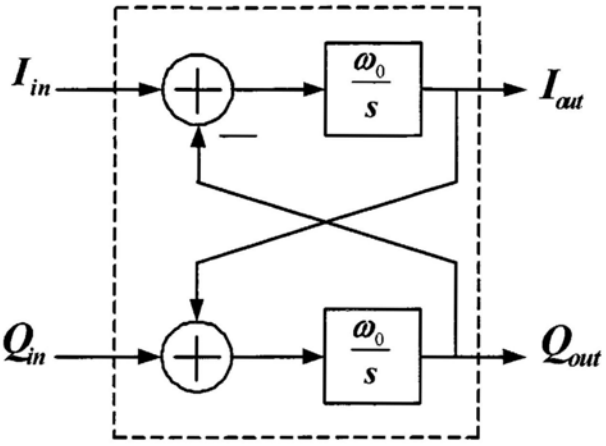


Fig 3.8 Quadrature resonator realizing.

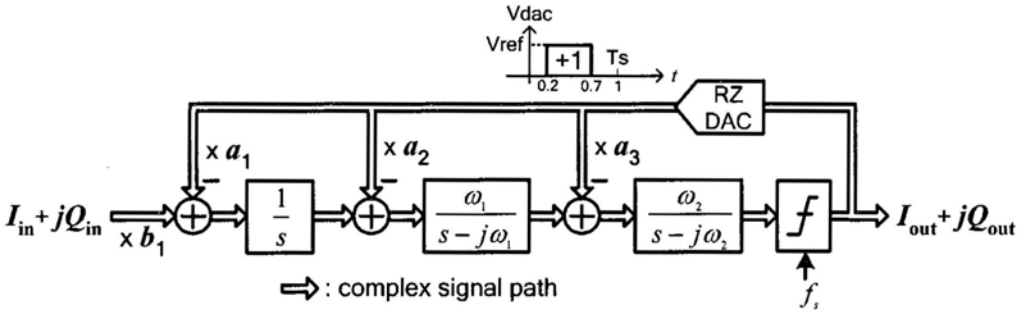


Fig 3.9 Topology of the CT complex modulator with distributed feedback

The signal flow diagram of the synthesized modulator is shown Fig 3.9. The coefficients of the modulators in the Fig 3.9 are

$$\omega_1=0.0491, \omega_2=0.0982 \tag{3-17}$$

and

$$a_1=6.56+j3.58, a_2=7.55+j12.2, a_3=13.76-j0.307 \tag{3-18}$$

The input coefficient b_1 in Fig 3.9 only scales the signal transfer function and does not affect the NTF. Its value selection is based on criterion of achieving maximum

SNR and maintaining the modulator's stability. From extensive simulation it is chosen to 3 here. It corresponds to the maximum stable input level 0dB. In this single bit modulator design, the maximum stable input level is referred to the feedback DAC reference voltage, which is 0.5V.

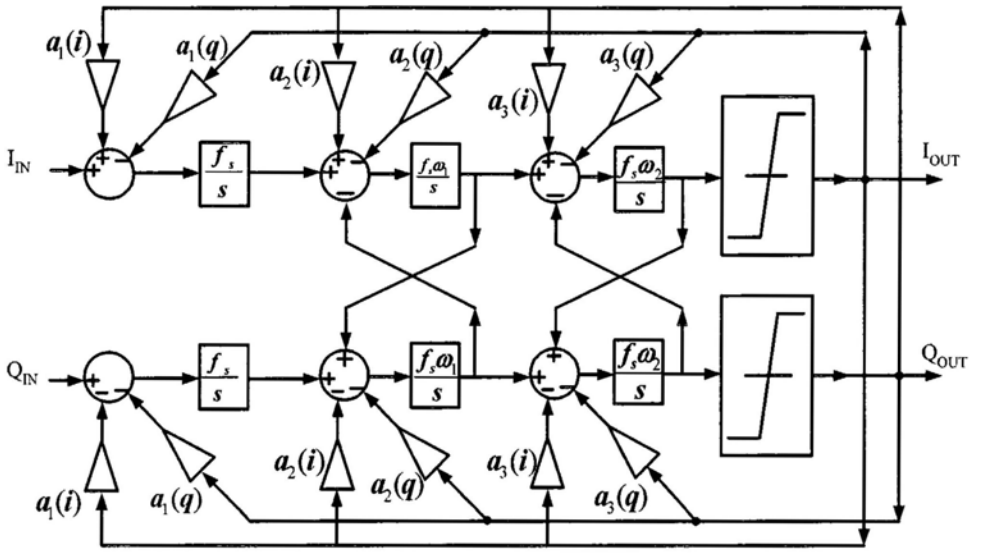


Fig 3.10 The architecture of the complex CT modulator

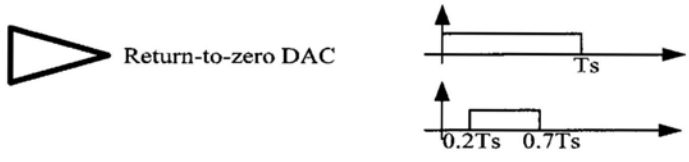


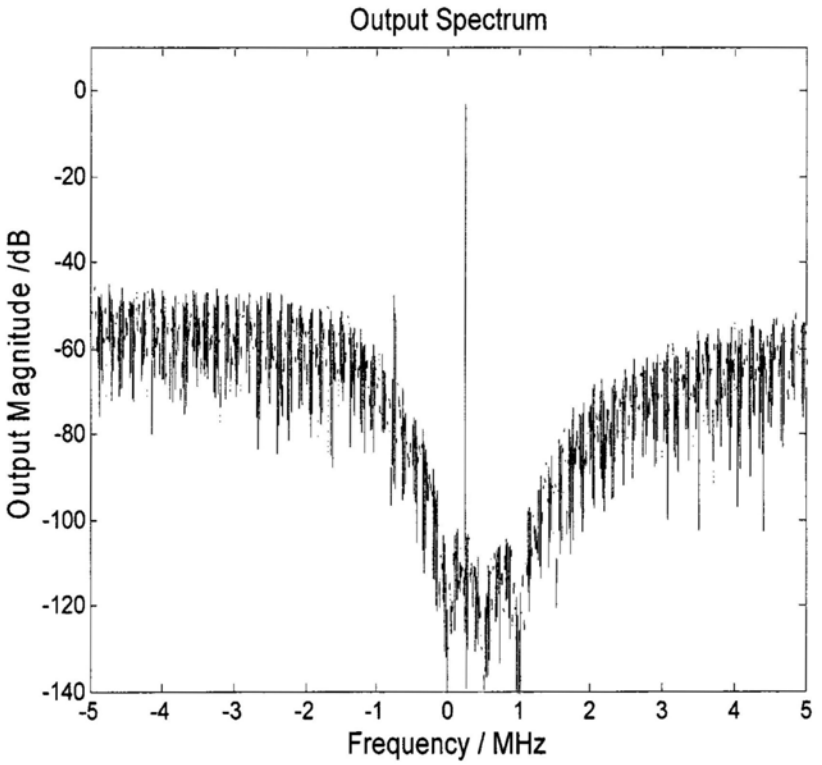
Fig 3.11 Return-to-Zero DAC and its control clock

3.2.4. Simulations of the synthesized modulator

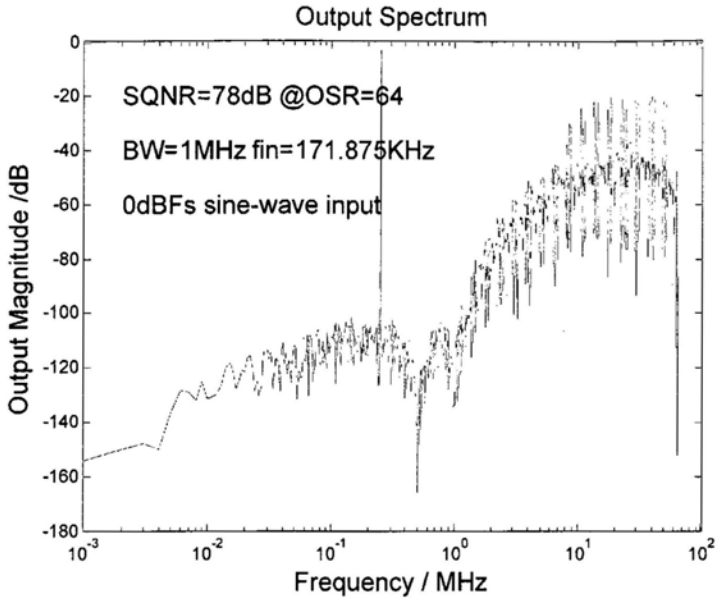
Fig 3.10 shows the architecture of the synthesized CT complex delta-sigma modulator with RZ feedback DAC. The coefficients are given in (3-17) and (3-18). $a_{x=1,2,3}(i)$ and $a_{x=1,2,3}(q)$ are the real and imagery part of and (3-18), respectively. The modulator model has been simulated in Matlab Simulink to verify its correctness.

Fig 3.11 shows the control clock for the RZ DAC. Since the sampling frequency f_s is 64MHz, all variables s in Fig 3.10 must be replaced by s/f_s in Fig 3.10. The RZ DAC is modeled by the RZ pulse generator following the comparator (not shown in the Fig 3.10).

A simulated output spectrum the modulator for a full-scale input is shown in Fig 3.12, where a third-order shape and desired transfer function zeros are clearly observed.



(a) Spectrum output



(b) Spectrum output, single side

Fig 3.12 Simulated output spectrum of the complex CT modulator.

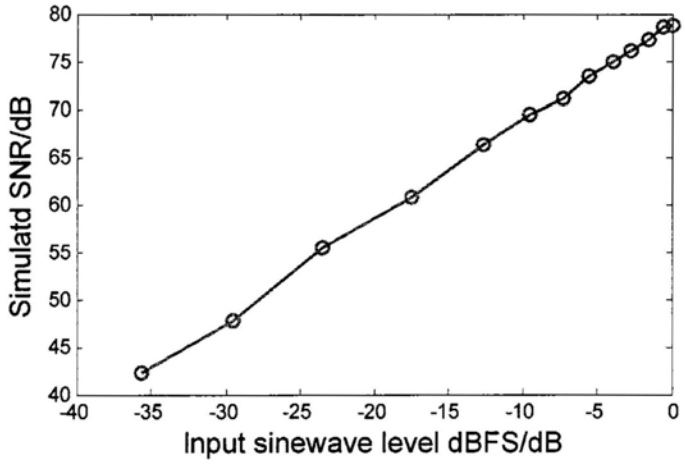


Fig 3.13 Simulated SNR performance versus input level.

Fig 3.13 shows the SNR of the modulator at various input levels. The maximum stable input is found when the highest SNR is achieved. In this case, the simulated maximum SNR of the modulator is 78dB. From the above results, the function of the synthesized modulator is proven correct.

Chapter 4 Implementation of complex CT delta-sigma modulator

This chapter describes the design and simulation results of the synthesized CT delta-sigma modulator using active RC circuits. The modulator was implemented in a 0.13μm triple-well CMOS process and the regular transistor NMOS/PMOS with threshold voltages of 0.22V/-0.25V was used.

The influence of the components nonidealities is first discussed. The 0.5V circuit blocks are then presented followed by circuit simulation results.

4.1. Nonidealities in oversampling delta-sigma modulator

An active-RC implemented modulator mainly consists of op-amps (operational amplifiers), comparators and passive components including resistors and capacitors. The main non-idealities of modulator include: finite gain/bandwidth/slew rate, thermal noise and 1/f noise of opamps, RC time constant variation due to process variation, quantizers' delay/offset/hysteresis/metastability, feedback DAC elements mismatch and their unequal rise/fall time, and clock jitter. All of these nonidealities adversely affect the performance of delta-sigma modulator. However, due to their different mechanisms and different occurring locations inside a modulator, their effects on the performance of the modulator are different. These non-ideal phenomena are discussed before the modulator circuit is presented.

4.1.1. Op-amp non-idealities

The loop filter transfer function is the key performance determining factor for a delta-sigma modulator because it defines modulator's noise-transfer function and the quantization noise-shaping behavior. The complete loop filter usually consists of several integrators realized by either RC or gm-C circuits, or even LC-resonators for band-pass modulators. For any architecture modulator, the nonidealities of the

integrator appearing in the first stage are not suppressed by the high loop gain, and thus impact the modulator performance to a large extent. The effects of the opamp's nonidealities on active-RC modulator are discussed next.

4.1.1.1 Finite gain and gain bandwidth

Fig 4.1 shows a typical RC integrator used for CT modulators [40]. The resistor Rn driven by the quantizer, input signal or output of preceding stage, performs a linear V/I conversion. The current charging the integrator capacitor period is a full sampling period for NRZ or half period for RZ.

In ideal case, the transfer function of the RC integrator is

$$\frac{V_o(s)}{V_n(s)} = \frac{-1}{sR_nC} = \frac{f_s \times k_n}{s} \tag{4-1}$$

where Rn is the value of n-th resistor while C is the value of the integration capacitor, k_n is the scaling coefficient, which is mapped to RC product and f_s is the clock frequency. The R and C value of Fig 4.6 is calculated from (4-1) according to the Matlab model shown Fig 3.10.

When considering the amplifier as a one-pole amplifier, we have:

$$A(s) = \frac{A_0}{1 + s/\omega_0} \tag{4-2}$$

The RC integrator transfer function with one-pole amplifier is,

$$\frac{V_o(s)}{V_n(s)} = -\frac{1}{sR_nC} \frac{1}{1 + \frac{1}{A(s)} + \frac{1}{sRC}\frac{1}{A(s)}} \tag{4-3}$$

With (4-2), the integrator transfer function is rewritten as

$$\frac{V_o(s)}{V_n(s)} = -\frac{1}{s^2\frac{R_nC}{A_0\omega_0} + s(\frac{1}{A_0\omega_0} + R_nC + \frac{R_nC}{A_0}) + \frac{1}{A_0}} \tag{4-4}$$

When only finite DC gain is considered, (4-4) becomes,

$$\frac{V_o(s)}{V_n(s)} = -\frac{1}{s(R_nC + \frac{R_nC}{A_0}) + \frac{1}{A_0}} \approx -\frac{f_s \times k_n}{s + \frac{1}{A_0R_nC}} \tag{4-5}$$

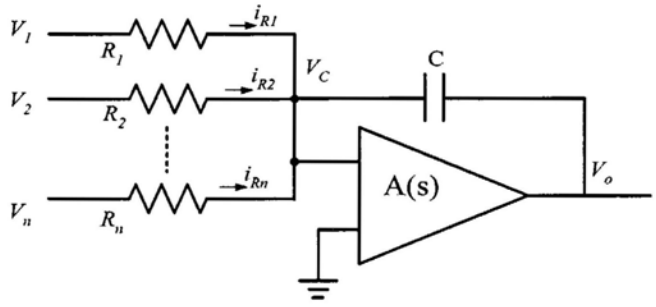


Fig 4.1 Typical RC integrator with single pole amplifier used in CT modulators.

Obviously the integrator transfer function has a pole at $\frac{1}{A_0R_nC}$, away from dc. Following (3-14), the zeros of NTF come from the poles of the loop filter. Thus, all zeros of the NTF are pushed away from dc, which reduces the amount of attenuation of the quantization noise in the base-band. This nonideality is known as leaky integration. The additional in-band noise due to the leaky integrator is not so serious. In case of single-loop architecture, the performance attenuation of SNR is around 0.2~1 dB with the requirement of the dc gain of the amplifier $A_0 > OSR$ [41][42]. Usually, this requirement is very easy to satisfy.

Assume $A_o >> 1$, formula, (4-5) can be rewritten to [40]:

$$\frac{V_o(s)}{V_n(s)} = -\frac{1}{s^2\frac{R_nC}{A_0\omega_0} + s(\frac{1}{A_0\omega_0} + R_nC)} = -\frac{k_nf_s}{s}\frac{GE_{GBW}}{\frac{s}{\omega_2}+1} \tag{4-6}$$

$$GE_{GBW} = \frac{GBW}{GBW + k_nf_s} \tag{4-7}$$

$$\omega_2 = GBW + k_nf_s \tag{4-8}$$

where GE_{GBW} is the integrator gain error due to finite gain-bandwidth product, and ω_2 is the additional pole introduced by the limited gain-bandwidth product (GBW).

Equation (4-6) shows that a practical RC integrator can be modeled as an ideal integrator scaled with a gain error and followed by a single-pole roll off. For low values of the GBW, which is the usual case for low-voltage design, the added second integrator pole ω_2 introduces an extra loop delay in the feedback path, which has the worst influence on the performance degradation of CT modulator.

The effects of the amplifier's finite gain bandwidth on the performance of the modulator can be modeled in simulation. Based on the results in [43] and the simulation results, a GBW of the amplifier around the sampling clock does not give severe degradation on the modulator's SNR performance if the induced extra loop delay is controlled. Even more, the GBW can be chosen lower than the sampling frequency with delay compensation technique in the feedback path [44].

4.1.1.2 Slew rate

Another nonideality of the amplifier incorporated in the integrator is the finite slew rate (SR), which is arisen from the limited current capability of charging the integrating capacitor and the amplifier internal compensation capacitor. In DT implementation, the signal transitions are very fast and the finite slew late results incomplete settling. Unlike the errors due to finite GBW, finite SR is a purely nonlinear effect and signal dependant, which results in distortion as well as an

increase of the noise floor [45]. In single-loop architecture modulator, the distortion is a key performance limiting factor [41].

For DT modulator, the requirement on amplifier's SR is usually high. One way to relax the requirement of SR is by using multi-bit internal quantization to reduce the signal swing feeding into integrator. In CT modulator, the slew rate specifications can be relaxed even for one bit quantization. The reason behind this is the signals in CT modulator are changing much slowly.

Considering a single-bit modulator, from Fig 4.1, the maximum slew rate of integrator can be described as,

$$SR_{\max} = \left|\frac{dV_o}{dt}\right|_{\max} = f_s V_{in}\big|_{\max} \tag{4-9}$$

$$V_{in}\big|_{\max} = \sum_{i}^{m} k_{i,fd} V_{fd} + \sum_{l}^{n} k_{l,fb} V_{ref} \tag{4-10}$$

where $k_{i,fd}$, $k_{l,fb}$ are the integrator scale coefficient as described in (4-1); V_{fd} is the forward signal, i.e, the modulator's input signal or the output of preceding integrator; and V_{ref} is the reference voltage of the modulator.

The first integrator is the most critical one in all kinds of modulator regardless of their architectures because its input referred errors are not suppressed by the loop filter and thus any error caused from limited SR will directly appear in the output spectrum. Errors induced by SR in the integrators after the first one are suppressed by the preceding filters. Taking the first integrator into account, the input signal almost does not change its amplitude during one sampling clock period due to the over-sampling. The feedback signal is assumed to be RZ pulses. During one sampling clock, the feedback signal is changed from V_{dd} (assume $V_{ref} = V_{dd}$) to zero or vice versa. The slew rate of one-bit modulator in the worst case can be approximated from (4-9), and rewritten as

$$SR\big|_{\max,int1} = f_s(k_{in}V_{in} + k_l V_{ref}) \tag{4-11}$$

k_{in} is the input scaling coefficient and V_{in} is the input signal amplitude, which is around half V_{dd}. Usually, the value calculated from (4-11) is not hard to satisfy even for amplifier operating at 0.5V.

4.1.2. Time constant variation

For R-C integrator-based CT modulators, the integrator gains are mapped into R-C products. In modern mainstream CMOS processes, the values of resistor and capacitor vary over process, temperature, voltage, etc. For the most of this type of modulators, the resistors are mainly realized by doped poly-silicon. The variation of the absolute resistor component values is up to 13% [29] or even more. Taking the variation of capacitor into account, the possible variation of the RC-product is more than 20%.

Considering the variation of the RC product, (4-1) is rewritten as

$$\frac{V_o(s)}{V_n(s)} = \frac{-1}{sR_nC(1+\delta_{RC})} = \frac{f_s \times k_n}{s} GE_{RC} \tag{4-12}$$

$$GE_{RC} = \frac{1}{(1+\delta_{RC})} \tag{4-13}$$

Equation (4-12) shows the integrator transfer function is scaled gain error induced by the variation of RC product.

Obviously, for the last integrator in the modulator, which is in the front of the quantizer, the effect of its gain error induced by RC product variation is negligible because the quantizer makes its decision based on the sign of its input and regardless of whether its inputs is scaled or not.

As for the variation of R-C products, there are two cases, positive variation or negative variations. For the positive one, which yields reduced integrator scaling

coefficients k_n in (4-1), and thus less aggressive noise-shaping behavior is resulted [35]. The less aggressive noise-shaping will increase the in-band noise, but will not affect the stability. A negative shift of the RC product value will increase the scaling coefficients k_n and thus more aggressive noise shaping, which will slightly increase the performance since more noise will be pushed out of band of interest. But the potential of the instability of the modulator, caused by the more loop gain, is increased [35]. Also the stability of the modulator strongly depends on the input amplitude and the out-of-band gain of the ideal modulator loop filter. In the system design of the modulator, besides meeting the common criterion of $|NTF| \leq 1.5$ for single-bit high order modulators, the modulator need to be extensively simulated with varying RC product and different input amplitude.

4.1.3. Comparator nonidealites

Usually, for oversampling modulator, the comparator is the most uncritical building block because it locates at the most insensitive place of the loop. It is preceded with the whole loop filter. The errors induced by the comparator nonidealities, which are usually known as delay, offset, hysteresis, and metastability, are shaped by the high-pass shaping characteristic of NTF. Nonetheless, for high resolution delta-sigma modulator, special attention has still to be paid on the nonidealites of the quantizer.

4.1.3.1.Comparator offset and hysteresis

The comparator offset is largely attenuated by the loop filter of the modulator. In single-bit modulators, the error induced by offset almost has no effect on the performance of modulator. For multi-bit quantizers, offset can cause an increase in the noise-floor and the harmonic distortion, thus degrade the SNDR. The comparator hysteresis is a kind of "memory" effect, which causes the output of comparator does not change even when its input level has surpass a threshold. The hystersis cause additional noise and in-band distortion, but like comparator offsets, hysteresis also

experiences the same shaping as the offsets [41]. The influence of hysteresis on the modulator performance is mostly negligible if reset circuit is added to cancel the memory effect such as shorting differential internal nodes in the latch to one of the power supplies or shorting them together in the reset phase by switching.

4.1.3.2. Metastability

Comparator metastability is the phenomenon of long time decision of the comparator when a very small input is applied. The caused extra delay will be added into the loop delay, which is problematic for the performance of CT modulator. Possible ways to mitigate the performance degradation include: scaling the quantizer input to have as large a span as possible; adding a preamplifier circuit to decrease the regeneration time; and increasing the gain-bandwidth product of the regenerative circuits to improve regeneration speed. Another way to mitigate the metastability problem is to adopt Gray coding between thermometer and binary codes [46]. But, the added decoding stage circuit costs more time and may not be preferred for some high speed designs.

4.1.3.3.Comparator delay

In realities, the comparator cannot produce the correct comparison result right after the input signal feeds in. The delay is related to the comparator design and the manufacture process. Even more, the time needed to regenerate the comparison result is depending on the signal amplitude and signal slope. Obviously, the comparator makes its decision more quickly when feed by a large overdrive input differential signal.

The delay between the comparator clock edge and the point of valid DAC output is called excess loop delay, which includes the finite time for the feedback DAC signal regeneration, the time for comparator decision, and the delay of signal processing blocks for multi-bit modulator, which includes dynamic element matching (DEM) and/or calibration circuitry in the feedback path to suppress DAC element mismatch errors.

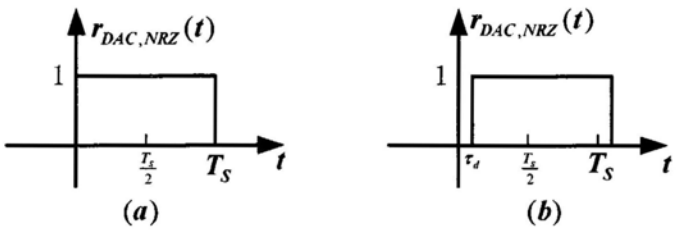


Fig 4.2 Excess loop delay of NRZ DAC (a) ideal case (b) practical case with delay

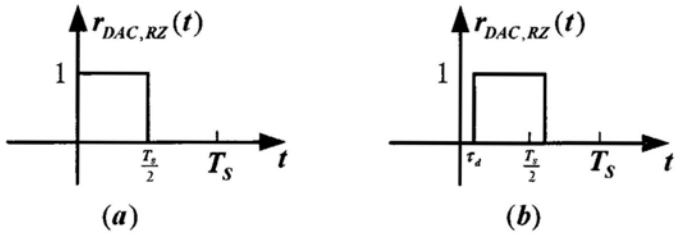


Fig 4.3 Excess loop delay of RZ DAC (a) ideal case (b) practical case with delay

Fig 3.5 and Fig 3.6 show the ideal waveforms of NRZ and RZ DACs. Their impulse invariant transformation depends on proper shape of the DAC pulse. Equation (3-5) and (3-7) is the Laplace transformation of NRZ and RZ DAC signals. Due to the loop delay of τ_d in the practical modulator, the feedback DAC output is shifted by τ_d to the right side in the time domain, as shown in Fig 4.2 and Fig 4.3 for NRZ and RZ DAC feedback respectively. Consequently, the DAC transfer function described by (3-5) will change to,

$$\widehat{R_{NRZ}(s)} = \frac{e^{-s\tau_d} - e^{-s(Ts+\tau_d)}}{s} \tag{4-14}$$

Compared to the ideal case for NRZ DAC, the excess loop delay in the practical implementation will cause the DAC pulse fall-edge passes T_S, resulting in that the

order of the actual modulator is increased by one, the noise shaping performance will be degraded, the maximum stable amplitude is decreased and even instability is caused [47][48].

As for the RZ feedback DAC we chose, any delay of the real circuit will also shift the DAC pulse. But as long as the total delay is not more than half a clock period, the fall-edge will not pass T_S, thus the equivalent modulator still has the same order.

As shown in the Fig 4.6, the 20% of clock is considered as the excess loop delay for RZ DAC feedback implementation.

4.1.4. Feedback DAC nonidealites

All errors introduced by the first and outermost feedback path DAC directly add to the input of the overall modulator. The nonliearities, like noise and distortion, of feedback DAC are as important as that of the first integrator.

Considering a rectangular DAC feedback waveform, the nonidealities of the feedback DAC can be classified into two categories: the one caused by timing errors and the one due to DAC levels variations caused by mismatch (which displays its influence mainly in the multi-bit implementation). The errors related to timing include the constant delay of the pulse by τ_d, which is discussed before and known as excess loop delay, and the statistical variation of the point of sampling edge or even the duration of sampling time caused by clock jitter [49][50], which will be discussed in next section.

Due to the intrinsic characteristic of integrated circuits, the excess loop delay cannot be completely avoided in a CT modulator circuit implementation, especially for high speed circuits. It is necessary to take measurement to circumvent its effects. Excess loop delay cancellation and loop delay compensation by auxiliary feedback path were proposed in [48][51][52][53].

For RZ DAC feedback, if the pulse is not shifted to next clock cycle, the order of the loop filter and the noise-transfer function are not changed. But its excess loop

delay still yields increased quantization in-band noise and possibly reduced stability (maximum stable amplitude). The reason behind this is the scaling mismatch. The calculated scaling coefficients come from the designed set of $[\alpha T_s, \beta T_s]$ shown in Fig 4.3 (a), where $\alpha = 0, \beta = 1/2$. But due to a shift of the feedback pulse from these designed values $[\alpha T_s + \tau_d, \beta T_s + \tau_d]$ in real circuits, scaling coefficient mismatch occurs in the calculated design and the real implementation. The straightforward solution is to calculate the scaling coefficient not for the ideal pulse position but for the delayed one $[\alpha T_s + \tau_d, \beta T_s + \tau_d]$. τ_d used in the calculation is an estimated value for specific application.

In addition to the excess loop delay discussed above, the DAC levels themselves are also affected by mismatch: In the case of multi-bit internal quantization and thus multi-bit DAC, the variation of the feedback levels yields a signal-dependent feedback error, which is directly fed to the modulator input and thus not suppressed by the loop filter. As a consequence, the linearity requirement on the feedback DAC is very high even for low resolution modulator [54]. For a single-bit internal quantizer, this requirement is always satisfied because a two level DAC is intrinsically linear. To achieve the linearity requirement, many linearization techniques and digital or analog correction are proposed [55][56][57][58]. But the advantage of these techniques needs the cost of rather complex circuits, rising additional area and consuming more power consumption. Moreover, the circuits of fulfilling the linearization in CT modulator implementations unavoidably cause additional time delay, which is a critical issue as disused above. In the multibit implementation, there is trade-off between the linearization and the feedback DAC.

4.1.5. Clock jitter

Due to the contaminated clock source, which is unavoidable in integrated circuits, the sampling time shifts. The statistical characteristic of this sampling variation is known as clock jitter. As for DT modulator, the jitter effects can be

improved by the oversampling ratio. Compared to Nyquist data converter, the DT modulator is more tolerant to timing jitter [41]. The secret behind this is that the integrators of DT modulator are allowed to settle to a designed accuracy within half clock period. Therefore, the effect of clock jitter on the performance degradation is mainly caused by the errors in the frond-end sample-hold circuits, in which clock jitter caused sampling misalignment produces an equivalent amplitude error. The increased in-band noise due to clock jitter is very limited and the performance SNDR degradation is very small [41].

However, clock jitter damages the performance of CT modulators more severely than their DT counterparts, as reported in [50] [61]. The clock jitter is usually regarded as the major disadvantage of CT delta-sigma modulator implementation. Fig 4.4 shows there are two clock jitter error sources in typical CT modulator. The first one, as like in the DT modulator, comes from the internal quantizer, which is prone to jitter affected sampling timing. But these errors can be neglected in practice because they are suppressed by the high-pass loop filter. The major influence of clock jitter on the performance degradation of CT modulator comes from the second one, which appears in the feedback DAC. Because the most outer feedback DAC directly feeds into the input of the first integrator, the errors directly modulates the modulator's performance.

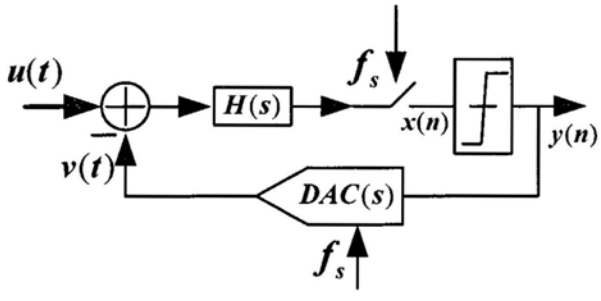


Fig 4.4 Clock jitter error source in typical CT modulator

In CT delta-sigma modulator, the integrator capacitor integrates the feedback waveform over time. The variation of the feedback waveform pulse length due to the clock rising and falling edge variations, in other words, clock jitter, directly modulates the amount of feedback charge errors integrated in the capacitor during the corresponding clock cycle. For commonly used NRZ DAC or RZ DAC feedback waveform, this error is proportional to the clock jitter variance $\sigma_{\Delta t}^2$, which adds directly to the input of overall modulator through the outermost feedback path.

Fig 4.5 shows the typical RZ DAC feedback waveform with amplitude $I_{RZ,DAC}(t)$, in which sequence of {1, -1, 1, 1} is used as example. Fig 4.5(c) shows the feedback uncertainty due to the jitter. The jitter alters the falling and rising edge of the feedback waveform, thus the length of the waveform width of the current charging the integrator capacitor. The charge error in the integrator capacitor degrades the performance mainly through the outermost feedback path into the overall input of the modulator [63].

The error induced by the jitter sequence can be modeled as [64][65],

$$e_{RZ} = [y(n) - y(n-1)]\frac{\Delta t(n)}{T_s} \quad \text{.....(4-15)}$$

Where $y(n)$ is the n-th output bit, T_s the clock period and $\Delta t(n)$ is the clock timing error.

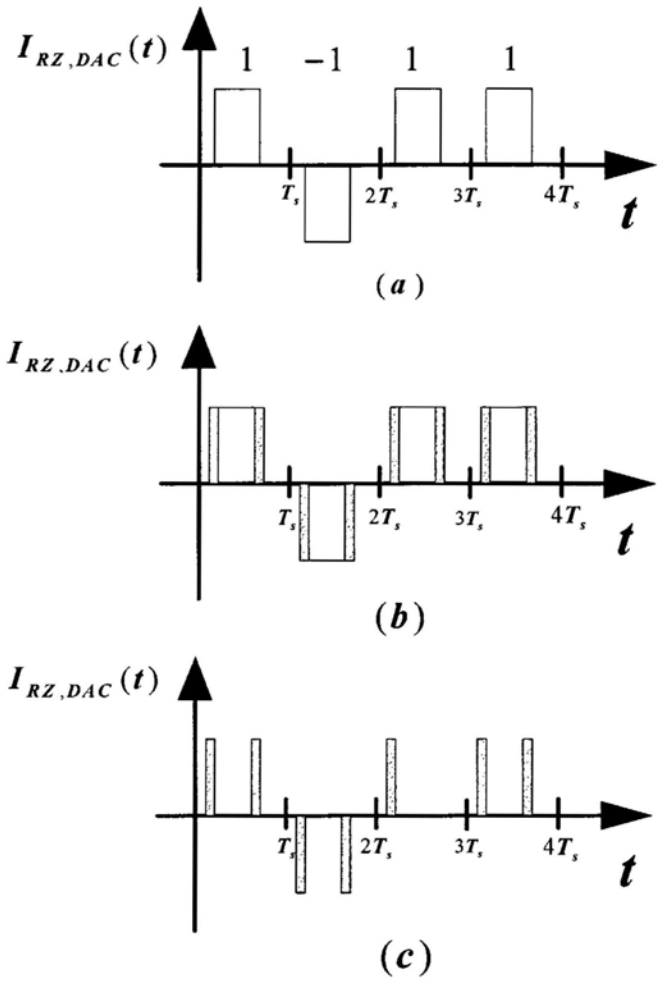


Fig 4.5 DAC output (a) without jitter (b) with jitter (c) and the uncertainty

For calculation purposes, it is commonly assumed that the clock jitter follows a uniformly distributed random process and is considered as white noise. This jitter error can be written as

$$\sigma_{\epsilon_{RZ}}^2 = \sigma_{\Delta y,RZ} \frac{\sigma_{\Delta t}^2}{T_s^2} \tag{4-16}$$

Where $\sigma_{\Delta y,RZ}^2$ is the variance of the adjacent output difference, and $\sigma_{\Delta t}^2$ is the variance of the clock jitter.

The jitter error is spread of overall sampling frequency, thus the in-band jitter error is reduced from (4-16) by OSR. The signal-to-jitter noise ratio can be written by [65]

$$SNR_{jitter} = \frac{P_s}{P_{jitter}} = \frac{A^2/2}{\sigma_{eRZ}^2 / OSR} = \frac{OSR \times A^2}{2\sigma_{\Delta v,RZ}^2 \frac{\sigma_{\Delta t}^2}{T_s^2}} \tag{4-17}$$

Where OSR is the oversampling ratio, and A is the signal amplitude. Equation (4-17) gives preliminary requirement on the clock jitter. The actual jitter noise contaminating the modulator's performance depends on the amount of timing error in each clock cycle $\sigma_{\Delta t}^2$, the magnitude of the feedback pulse at the time of jitter occuring, and the feedback path with its scaling coefficients, through which the jitter noise enters the modulator.

Jitter sensitivity is still the limiting factor for CT modulator used in high speed applications where the requirement of enough low clock jitter is not easy to satisfy.

Compared to RZ DAC feedback implementation, the clock jitter of NRZ DAC feedback has less severely influence on the performance degradation. The jitter noise depends on the difference between two adjacent feedback pulses. For NRZ implementation, the state (1 or -1) transition of the pulse stream does not always occur in every clock. However, for RZ implementation, its state always returns to zero in very clock period. Generally, the jitter noise of RZ implementation will be 6 dB (1 bit) worse than NRZ in the band of interest [66]. Shaped feedback waveform DAC and multi-bit feedback DAC are also helpful for the clock jitter [63].

4.2. Circuit simulation using ideal models

The proposed modulator is implemented with an active-RC circuit shown in Fig 4.6, which explicitly shows the real and imaginary paths of the complex signals. In the modulator, the RZ DAC is modeled as RTO DAC [9]. The RTO DAC has the same feedback pulse shape as RZ DAC except that RTO DAC is floating in inactive

phase but RZ DAC is driven to zero. The clock controlling the RTO DAC is twenty percent delayed version of the sampling clock. The circuit is shown in single-ended form for simplicity, but the actual implementation is fully differential. Fig 4.7 shows the fully differential circuits, in which the pull up resistors connected to V_{dd} in the input terminals of each amplifier are not shown for simplicity. The pull up resistor will be discussed later in this chapter. Negative resistors are implemented by exchanging the positive and negative terminals in the differential circuit. The complex feedback coefficients are realized by feeding both the I and Q outputs back to both the I and Q integrators, as shown in Fig 3.8.

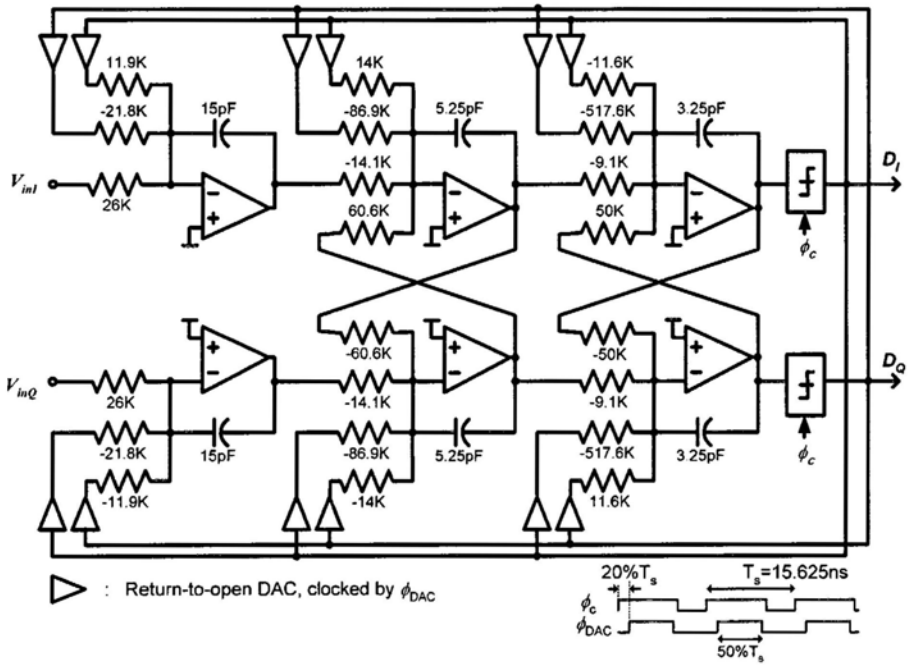


Fig 4.6 Simplified circuit of the CT complex delta-sigma modulator.

After the modulator is synthesized, we now implement the modulator in circuit level with amplifier model and comparator model. With the ideal amplifier and comparator models, we can verify the effect of R-C product variation, which change the loop filter coefficients, to simulate the modulator's stability. The simulation tells that the modulator is stable for over 20% of R-C product variation.

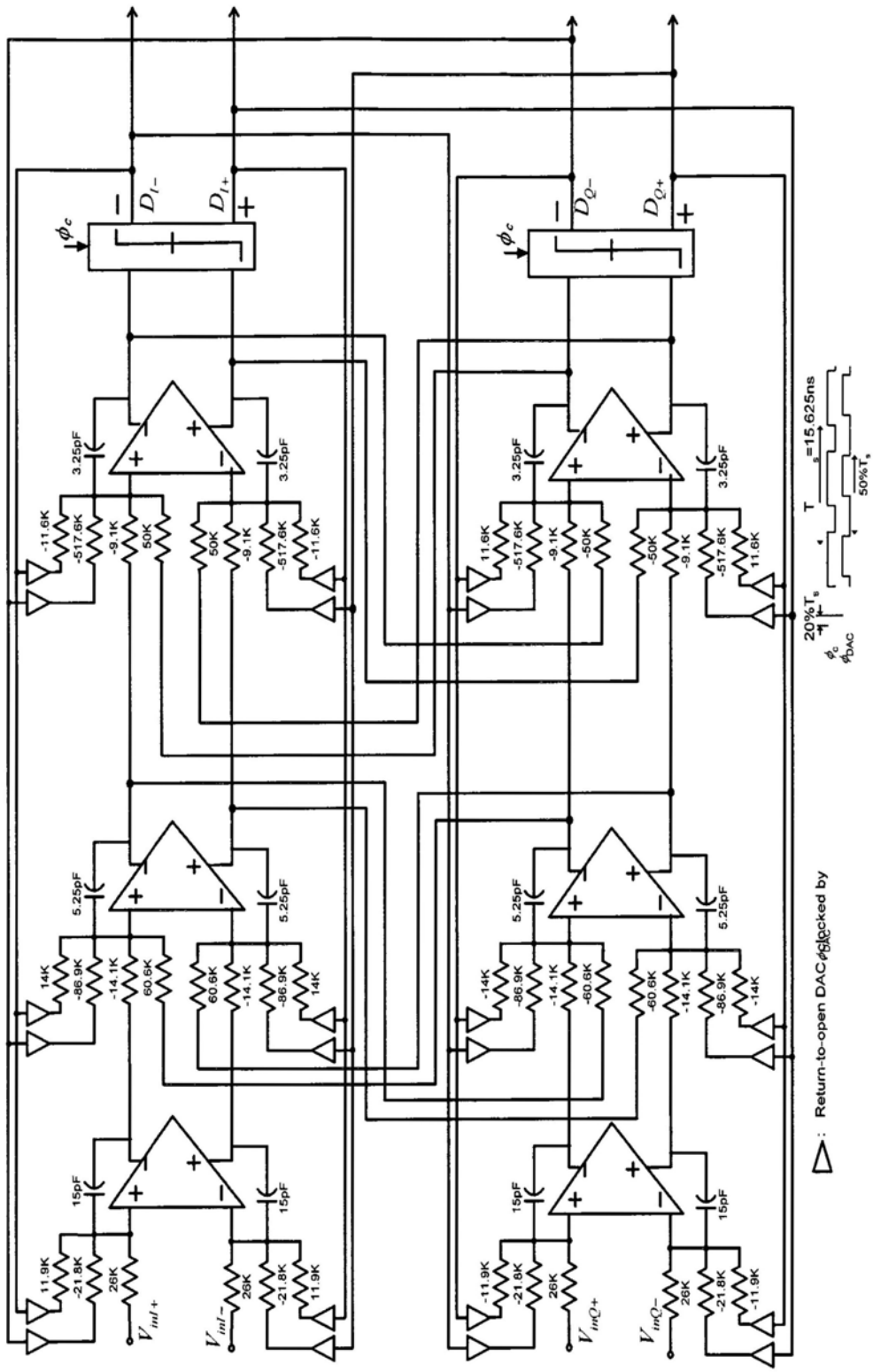


Fig 4.7 Fully differential schematic circuit of the proposed modulator

4.3. Circuit implementation

There are two main challenges for designing the modulator at 0.5V for a high sampling frequency of 64MHz. First, at a 0.5V supply, a comparator's output often cannot settle fast enough, and its settling transient can be data-dependent and degrade the modulator's performance. Second, the amplifiers must have a unity-gain bandwidth comparable to the value of fs under a capacitive load up to 15pF and a resistive load that can be as heavy as 9.1kΩ. The large capacitor depends on the noise performance requirement and heavy loading resistor is defined by the loop filter coefficient as shown in Fig 4.6.

To alleviate these design challenges, a number of system-level solutions have been implemented. First, to allow the comparator to fully settle, the rising edge of ϕ_{DAC} for the DAC is delayed by 20%Ts from the rising edge of clock ϕ_C for the comparator (see Fig 4.6), and RTO technique [9], was adopted. The details of the operation and design of the comparator were presented in section 4.3.5.

Second, the common-mode (CM) levels at the input of the amplifiers, $V_{in,cm}$, are set to a level higher than $V_{dd}/2$ so that the amplifiers can have a larger DC gain and wider bandwidth, because the input transistors of the amplifiers can be biased with a larger gate-to-source voltage. In this design, the desired value of $V_{in,cm}$ is set to 0.35V. Section 4.3.2 covers the design detail of the amplifier.

Before we discuss the circuit implementation, we discuss the noise aspects of modulator first.

4.3.1. Noise consideration

The first integrator in the I-channel is used to explain the noise consideration. The dominant noise sources are shown in Fig 4.8. The input-referred amplifiers noise $\overline{v}_{n,ota}^2$ includes flicker and thermal noise. The resistor noise is thermal noise and inherently white. V_{ref} is connected to V_{dd} or ground depending on the DAC

feedback output in active phase or floating in inactive phase. The detail operation of the integrator will be discussed in section 4.3.3. The total input-referred noise power is

$$\overline{v}_{n,in}^2 = 2(\overline{v}_{n,Ra}^2 + \frac{1}{2}\overline{v}_{n,R_b}^2(\frac{R_a}{R_b})^2 + \frac{1}{2}\overline{v}_{n,R_c}^2(\frac{R_a}{R_c})^2 + \overline{v}_{n,R_{cmp}}^2(\frac{R_a}{R_{cmp}})^2)$$

$$+\overline{v}_{n,ota}^2(1+\frac{R_a}{R_b}+\frac{R_a}{R_c}+\frac{R_a}{R_{cmp}})^2 \qquad (4\text{-}18)$$

Where $\overline{v}_{n,R_b}^2$ and $\overline{v}_{n,R_c}^2$ is halved in the thermal noise calculation because of the RTO operation of the feedback DAC [9]. As preliminary hand noise calculation, the resistor noise of upper part in Fig 4.8 is,

$$\overline{v}_{n,in}^2 = \overline{v}_{n,R_a}^2 + \frac{1}{2}\overline{v}_{n,R_b}^2(\frac{R_a}{R_b})^2 + \frac{1}{2}\overline{v}_{n,R_c}^2(\frac{R_a}{R_c})^2 + \overline{v}_{n,R_{cmp}}^2(\frac{R_a}{R_{cmp}})^2 \qquad (4\text{-}19)$$

The signal is a 0.5Vpp single-ended sinusoidal input, and the calculated SNR is 70.5dB in room temperature according to (4-19). There is one dB less of SNR when $\overline{v}_{n,R_b}^2$ and $\overline{v}_{n,R_c}^2$ is not halved. Now we consider differential coherent complex signals. The maximum input amplitude becomes 2Vpp, increased by 12dB. However, the noise power is increased by 6dB since four times resistors are concerned. The resulted SNR is 76.5dB.

The noise performance, including the effects of the amplifier, of the integrator shown in Fig 4.8 is simulated. The input is 0.5Vpp sinusoidal signal, and the simulated signal to the total input referred noise ratio is 72.8dB. Considering the overall modulator, the input signal power increases 6dB but the noise power only increases 3dB. The resulting SNR is 75.8dB. The input referred noise due to $\overline{v}_{n,R_b}^2$ and $\overline{v}_{n,R_c}^2$ is halved during the noise simulation.

The reason of the halving the noise contribution from $\overline{v}_{n,R_b}^2$ and $\overline{v}_{n,R_c}^2$ is that the the RTO DAC operation.

When comparing the calculated SNR and the simulated one, the contribution to the total input referred noise from the amplifier is quite small. In band of interest 1MHz, the total input amplifier equivalent noise $\overline{v}_{n,ota}^2$ is around 2.81e-11. As for the modulator, the input referred noise due to the amplifier only contributes 3.9% in the total input referred noise according to the (4-18) within the band of interest. The good noise performance of the amplifier comes from quite large input pair trans-conductance and large size of the input devices. The CM mode level shift resistors $\boldsymbol{R}_{cmp}$ and $\boldsymbol{R}_{cmn}$ give 4dB less in the total calculated SNR.

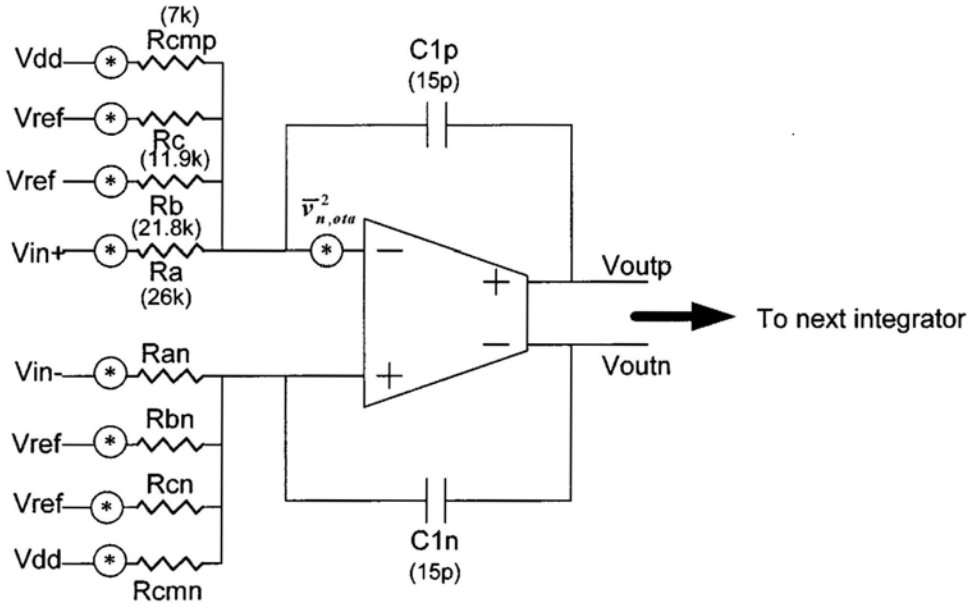


Fig 4.8 First integrator with additional noise source caused by amplifier and resistors

Last, it is also worth to note that, similar to [23][23], the modulator here employs a single clock phase for both I and Q comparators and another single clock phase for I

and Q feedback DACs. Therefore, I and Q phase imbalance problem, which commonly appears in complex signal processing circuits, does not exist here.

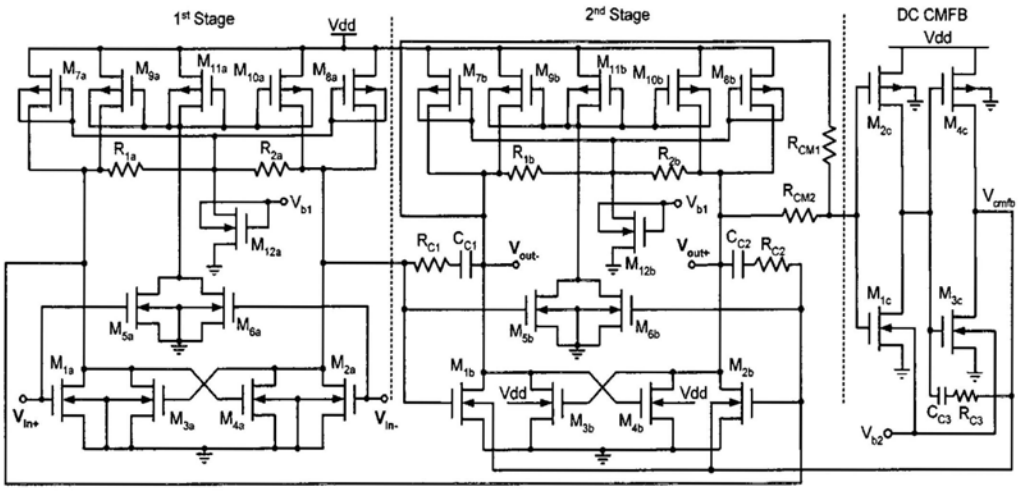


Fig 4.9 Schematic for the low-voltage gate-input two-stage OTA

4.3.2. Amplifier design

The target design normally operates in 0.5V supply. Thus the amplifier, as one of the key block of the modulator preferably operates in 0.5V too. Considering the supply of 0.5V, only two devices are stacked between V_{dd} and ground so as to leave high enough headroom for drain-source of the transistor.

Fig 4.9 shows the schematic of the amplifier designed for modulator operating with 64MHz sampling frequency, which is similar to amplifiers reported in [8][67] with a few difference. The amplifier used in this design is self-biased and does not require a replica to tune the DC gain and to set the output DC value at $V_{dd}/2$, whereas the amplifiers in [8][67] do need replicas for these purposes. Obviously, to achieve the same performance requirement the amplifier here is more power and area efficient without the replica.

The amplifier consists of two gain stages and a DC CMFB stage that is used to precisely set the output CM level at $V_{dd}/2$ for maximum swing. Let us focus on

the first stage now. The DC bias of the first stage is shown in Fig 4.10. The CM level at the gates of the input pair M_{1a} and M_{2a} is set above $V_{dd}/2$, at 0.35V (see Fig 4.10), to bias them in strong inversion to achieve the desired high operation speed (the amplifier practically doesn't work for an input CM level of 0.25V). V_{b1} is a fixed DC bias voltage, generated by the circuit shown in Fig 4.18, to make M_{12a} a constant current source. The differential-mode small-signal voltage gain, A_{dd}, of the first stage is

$$A_{dd} = \frac{g_{m1a}}{\frac{1}{R_{1a}} + g_{ds1a} + g_{ds7a} + g_{ds9a} + g_{ds3a} - g_{m3a}} \tag{4-20}$$

Where g_{mn} denotes transconductance of device M_n and g_{dsn} denotes its drain-source output conductance. The negative conductance, $-g_{m3a}$, formed by M_{3a} and M_{4a}, enhances the differential voltage gain. We have sized it to be 70% of the total load conductance, below the generally suggested value of 75% [8][68], to avoid latching under any process or temperature variation. Simulations at all possible cases of process corners in combination with temperature variation from -25℃ to 80 ℃ and ±10% supply voltage variation confirmed that the circuit is safe from latching. To prevent the CM signal from being amplified through the amplifier, a feed-forward CM cancellation path, formed by M_{5a}, M_{6a}, M_{11a}, M_{9a} & M_{11a}, and a local CM negative feedback path, formed by (R_{1a}, R_{7a}) and (R_{2a}, M_{8a}), are used. The first stage's common-mode-in common-mode-out small-signal voltage gain, Acc, is

$$A_{cc} = \frac{g_{m1a} - (g_{m9a} + g_{mb9a})\frac{2g_{m5a}}{g_{m11a} + g_{mb11a}}}{g_{ds1a} + g_{ds7a} + g_{ds9a} + g_{ds3a} + g_{m3a} + g_{m7a} + g_{mb7a}} \tag{4-21}$$

The negative term in the numerator of (4-21) represents the CM feed-forward cancellation. Transistors M_{7a} and M_{3a} become diode-connected for CM signals and reduce the magnitude of A_{cc}, as shown in (4-21).

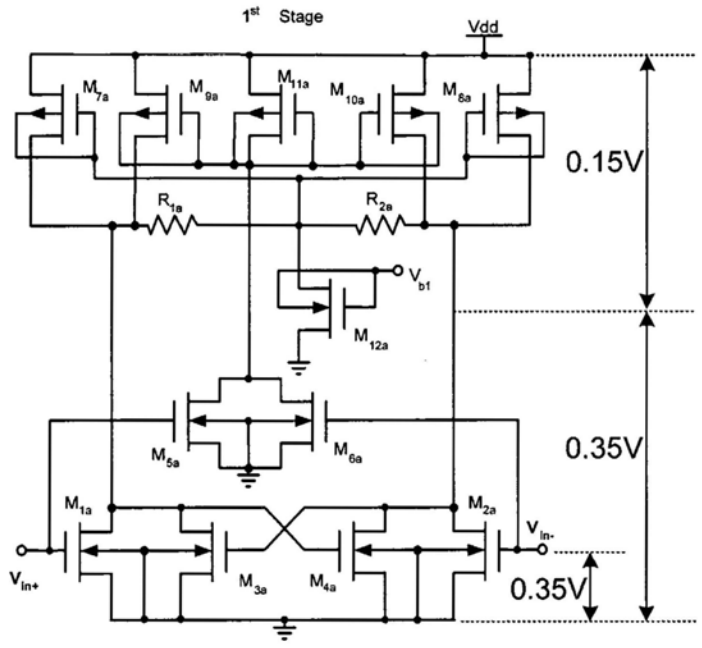


Fig 4.10 The DC bias of the first stage

The nominal DC value of the 1st stage's output CM level is set to 0.35V to turn the 2nd stage's input pair on strongly (see Fig 4.10). The second stage has a similar topology as the 1st stage except two minor differences. First, the bodies of M_{3b} and M_{4b} are tied to V_{dd} to compensate for their lower gate-source voltage, which equals the output CM level ($=V_{dd}/2$). Second, the bodies of M_{1b} and M_{2b} are used as the CM control input for the DC CMFB loop. The negative conductance, $-g_{m3b}$, is also set to 70% of the total conductance at the output nodes. The two-stage amplifier is

Miller compensated with feedback capacitors C_{C1} and C_{C2} and feed-forward zero–cancellation resistors R_{C1} and R_{C2}.

The amplifier has a built-in DC CMFB circuit to set the output CM level to $V_{dd}/2$. The CM output is sensed by R_{CM1} and R_{CM2} and then compared to $V_{dd}/2$ by two inverter amplifiers formed by M_{1c} - M_{2c} and M_{3c} - M_{4c}. The inverter amplifiers are biased so that their operating points are exactly at $V_{dd}/2$ and are insensitive to PVT variations (see Fig 4.18 and its explanation later). The amplified CM error is then fed-back to the bodies of M_{1b} and M_{2b} in the second stage to control the output CM level. Note that the DC CMFB stage has a limited bandwidth due to the slow inverter error amplifier whose devices operate in weak inversion. However this path only needs to control the DC component of the output CM whereas the CM signals are suppressed in each stage by the CM feed-forward cancellation path and by the local CMFB loop described earlier in this section.

The transistor sizes and component values for the most critical, first stage amplifier in the modulator are listed in Table 4-1. The value of integrator capacitor is defined from the noise consideration. At the same time, the amplifier also needs to achieve the UGF around the sampling frequency under the integrator capacitor load. To reduce the flicker noise, large size of device in the first stage of the amplifier is adopted. Channel length of 1.5μm is used for the input pair device. The large device size and large trans-conductance of the input pair result in quite small noise (as discussed in section 4.3.1. Fig 4.11 shows the simulated differential-in, differential-out voltage gain (A_{dd}), common-mode-in and common-mode-out voltage gain (A_{cc}) and the CMRR (A_{dd}/A_{cc}) of the amplifier with a load of 15pF at each of the positive and negative outputs. The amplifier has a 57dB DC gain, a 72MHz UGF and over 120dB CMRR at 1kHz and 50dB CMRR at 1MHz in simulation.

Table 4-1 Transistor Sizes and Component Values

First Stage	Second Stage	DC CMFB
M_{1a}: 76/1.5	M_{1b}: 50/0.36	M_{1c} 4/0.4
M_{3a}: 16/2	M_{3b}: 14/2	M_{2c} 7.5/0.36
M_{5a}: 42/1.5	M_{5b}: 25/0.36	M_{3c} 16/0.4
M_{7a}: 9/2	M_{7b}: 36/2	M_{4c} 30/0.36
M_{9a}: 300/2	M_{9b}: 100/0.36	$C_{c3} = 4\ pF$
M_{11a}: 220/2	M_{11b}: 70/0.36	$R_{c3} = 5.5\ k\Omega$
M_{12a}: 7.2/0.36	M_{12b}: 3.6/0.36	$R_{CM1} = R_{CM2} = 60\ k\Omega$
$R_{1a} = R_{2a} = 40\ k\Omega$	$R_{1b} = R_{2b} = 40\ k\Omega$	
$R_{c1} = R_{c2} = 0.6\ k\Omega$ $C_{c1} = C_{c2} = 5\ pF$		

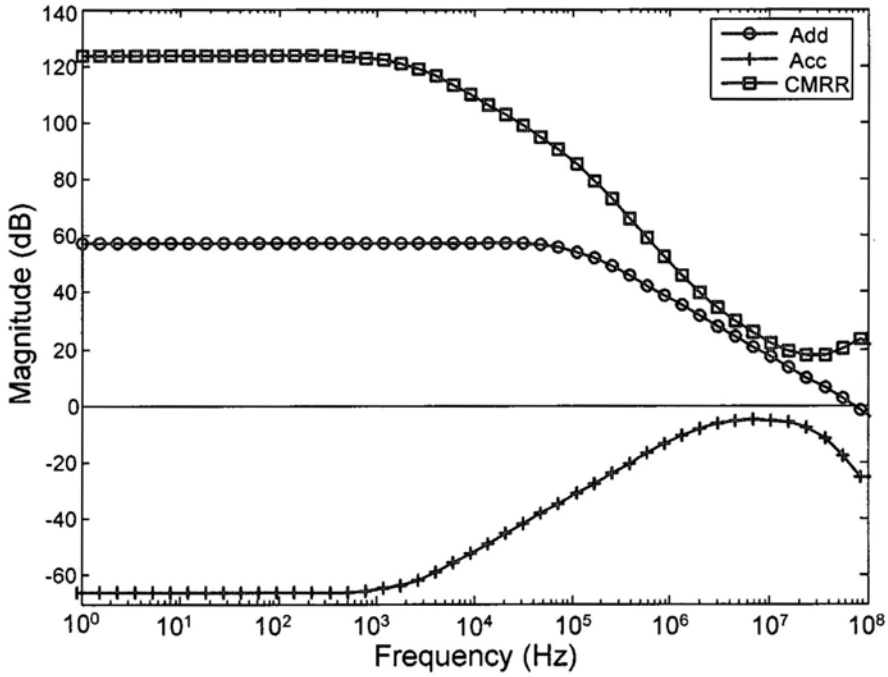
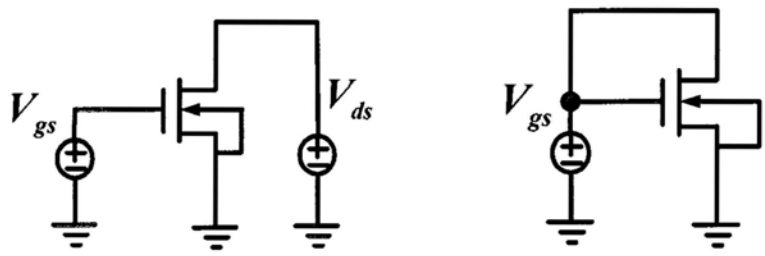


Fig 4.11 Simulated performance of Add, Acc, and Add/Acc the amplifier

To save power, the second and third amplifiers in the signal path have their currents and transistor sizes scaled down in proportion to their load. The ratio of current consumption among three amplifiers is 15:5:3.

The I-V characteristic of devices in the amplifier is also simulated. During the supply varying from 0.45V to 0.55V, the gate potential at the input pair M_{1a}/M_{2a} changes from 0.325V to 0.375V because it is overall set by the system, including DAC resistors driven by comparator outputs and the pull up resistors connected to V_{dd}. Because of cross-connection, both the gate and drain potential of the negative g_m pair of M_{3a}/M_{4a}, are varying from 0.28 to 0.4V when the supply varying from 0.45 to 0.55V. Consequently, the drain current is change dramatically, showing the dependence of the power supply. This is a drawback of the design (further design could be with by current bias). The I-V characteristic curves of the input pair and the negative g_m pair are shown in Fig.4.13. The schematic used for I-V curve simulation is shown Fig. 4.12. Due to the input pair operating in strong inversion, the drain current mainly depends on the gate-source voltage and less depends on its drain-source voltage.

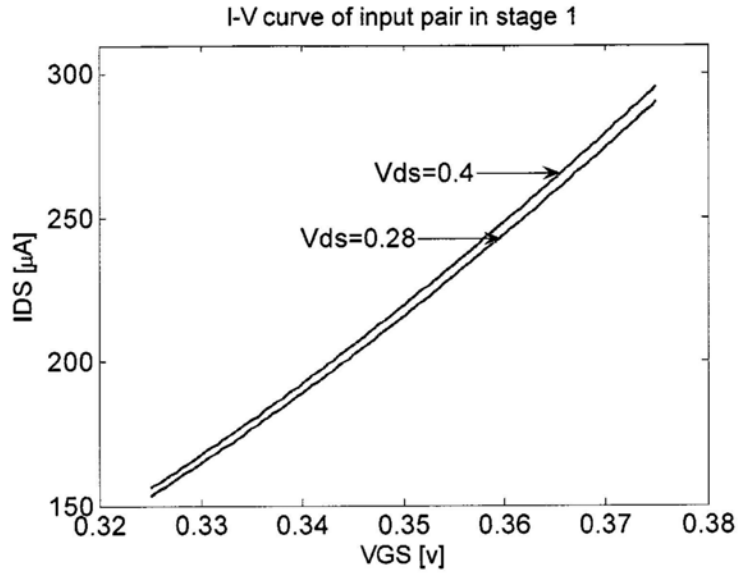


(a) (b)

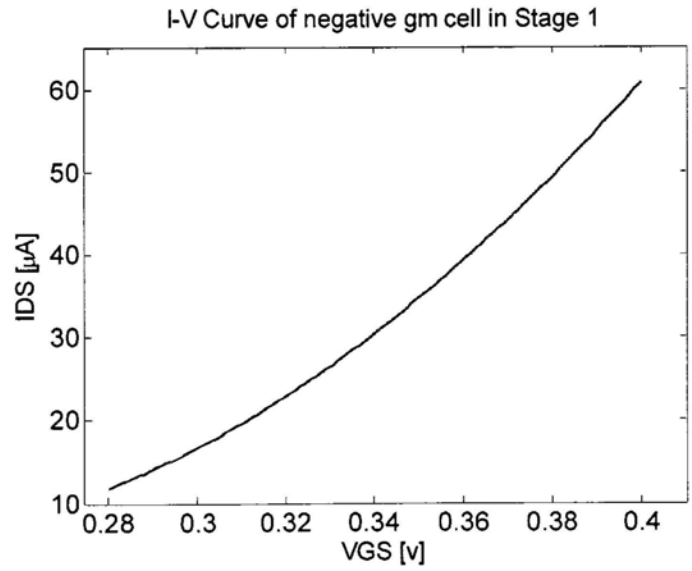
Fig 4.12 I-V curve simulation schematic for (a) Input pair and (b) negative gm pair

For the second stage, the gate potential of M_{1b}/M_{2b} varies from 0.28V to 0.4V and the potential at the drain node varies form 0.225V to 0.275V when the supply sweeps from 0.45 to 0.55V. M_{1b}/M_{2b} works in saturation and the drain current shows less dependence on drain-source voltage. The operation of M_{3b}/M_{4b} is similar

to that of M_{3a}/M_{4a} with the exception of gate/drain voltage varying from 0.225 to 0275. The I-V characteristic curves of M_{1b}/M_{2b} and M_{3b}/M_{4b} are shown fig 4.14.

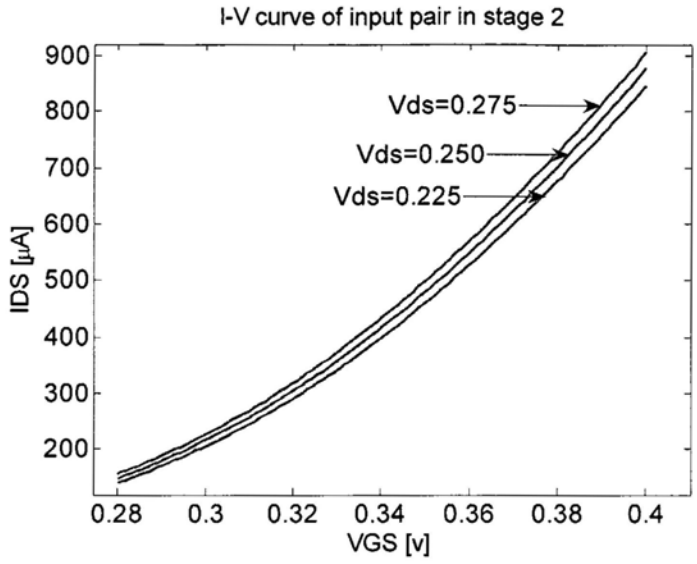


(a)

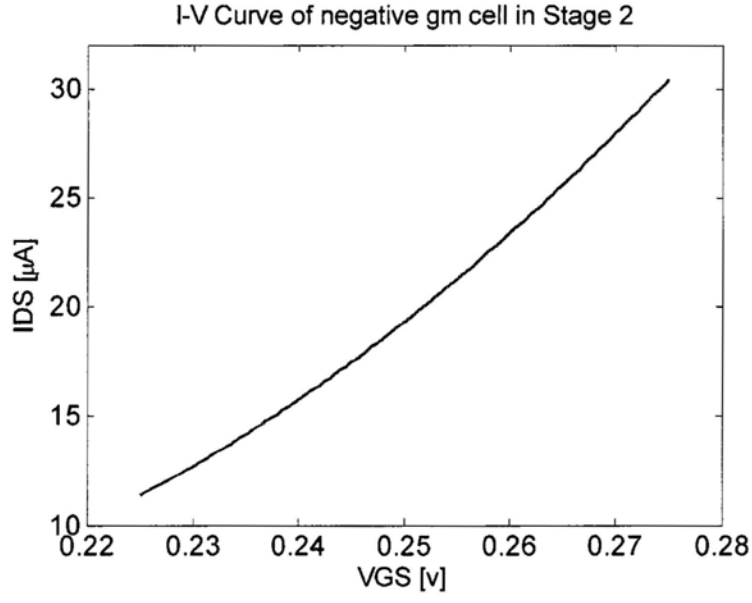


(b)

Fig 4.13 I-V curve of the device of (a)M1a/M2a (b)M3a/M4a



(a)



(b)

Fig 4.14 I-V curve of the device of (a)M1b/M2b (b)M3b/M4b

Almost all devices are working in forward biased, but latch up problem does not exist in this circuit due to maximum supply of 0.55V. The bulk current of the negative g_m cell M_{3b}/M_{4b} is simulated. The bulk current is shown in fig. 4.16. The

maximal bulk current is less than 16nA when V_{bs} of M_{3b}/M_{4b} is biased with 0.55V, which is the maxim operation voltage for the whole circuit.

Except that M9a/M10a/M11a and M5a/M6a operate in linear region, which work for common mode signal cancellation, all other transistors work in saturation region with the benefit of reduced threshold voltage by forward bias.

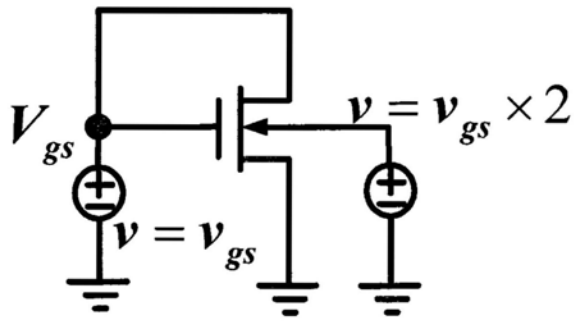


Fig 4.15 Schematic of bulk current simulation

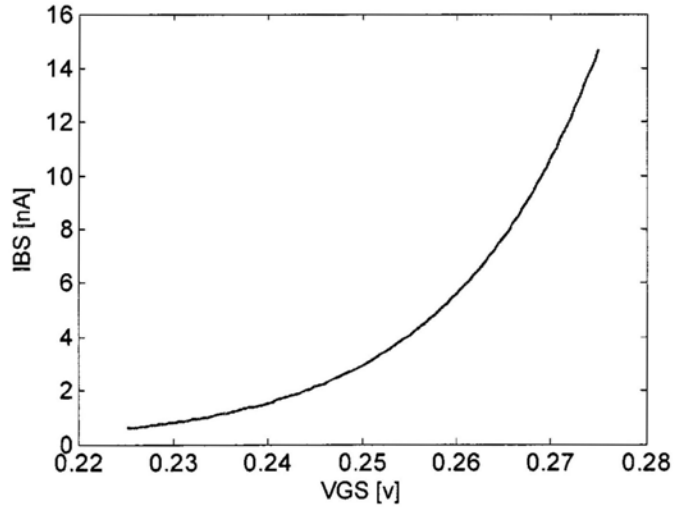


Fig 4.16 Bulk current of M3b/M4b

4.3.3. Operation of the integrator

Fig 4.17 shows the detailed circuit level implementation of the second integrator of the I-path, which is similar to the first integrator shown in Fig 4.8. The third integrator has the exactly same topology. All of integrators in the modulator have the similar operation. Now the second integrator in the I-path is used to explain the operation. The output CM level of the integrator is defined by the amplifier's CMFB, which is set at $V_{dd}/2$ for maximal signal swing. The amplifier's inputs have a CM level ($V_{in,cm}$) determined by the CM levels of the integrator input voltage pairs (V_{on1i}, V_{op1i}), (V_{op2q}, V_{on2q}), (V_c, V_e), (V_b, V_d) and (V_{dd}, V_{dd}), which have DC paths to the amplifier's inputs. The CM levels of (V_{on1i}, V_{op1i}), (V_{op2q}, V_{on2q}) are $V_{dd}/2$, set by the output of other stages. The resistor pair R_{2cmp} and R_{2cmn}, between the amplifier's inputs and V_{dd}, are used to lift up the $V_{in,cm}$ to the desired level of 0.35V. The CM values of (V_c, V_e) and (V_b, V_d) are $V_{dd}/2$ when the RTO DACs are "active", and are changing towards $V_{in,cm}$ when the DACs become "open", resulting in a variation in $V_{in,cm}$. However, the variation in $V_{in,cm}$ is very small due to the short time interval of the "open" state (=Ts/2=7.8ns) compared to the time constant formed by R_{2dp} and C_{2p} (=73.5ns) or that formed by R_{2cp} and C_{2cp} (=456ns). Fig 4.17 further shows typical voltage waveforms at nodes a, b and c (V_f is virtually the same as V_a and therefore not shown) and the feedback current signals. It can be seen that the amplifier's inputs stay around the desired level of 0.35V with a variation of less than 20mV. Unlike for lower speed RTO DACs [9], in the "open" state (ϕ_{DAC} LOW) the RTO DACs here cannot completely settle their outputs (V_b and V_c) to the desired CM level (0.35V) within Ts/2, which means a large memory effect; this would destroy the purpose of the RZ signaling. To overcome this, when entering the "open" state, the DAC outputs (e.g., c and e) are all shorted to ground momentarily

(by the DAC circuit itself, Fig 4.19) to reset any memory effects, then rise together from 0V towards 0.35V with time constants set by the parasitic capacitances at nodes c and e. The differential current from the feedback DACs (i1–i4) is indeed zero when the DACs are "open" (ϕ_{DAC} LOW) (see Fig 4.17), realizing the desired RZ function. The simulation results in Fig 4.17 show that a variation of $V_{in,cm}$ exists. Amplifiers with a sufficiently high CMRR are desired.

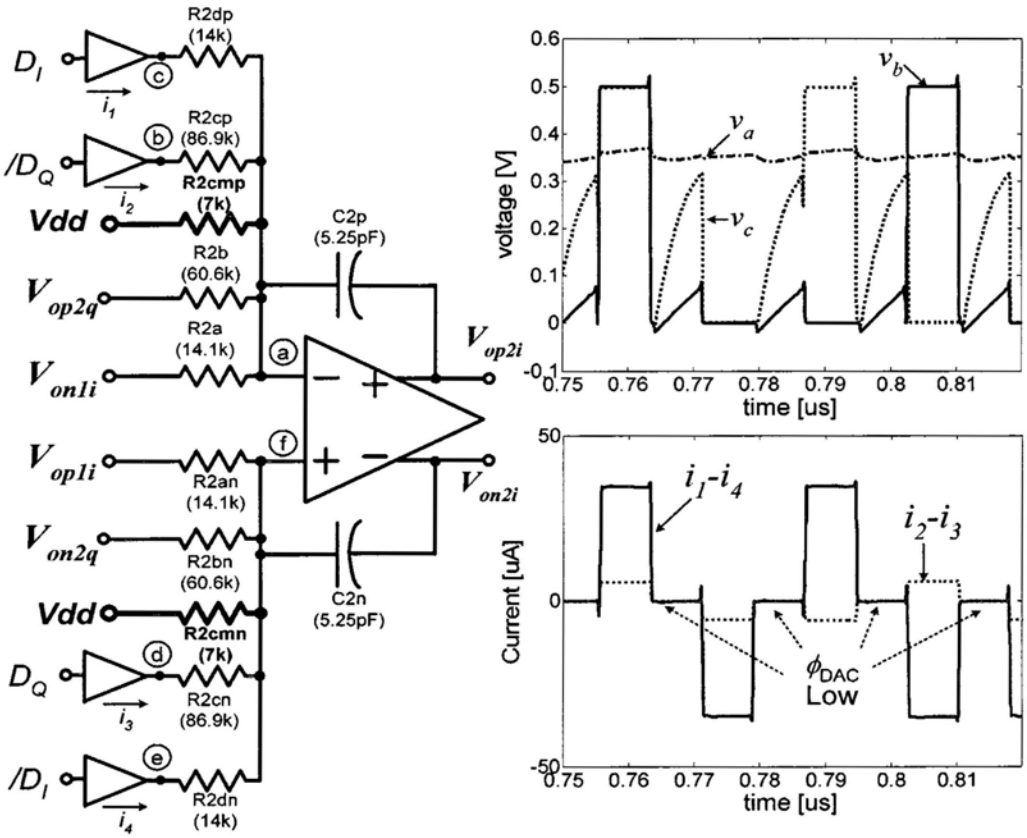


Fig 4.17 Detailed circuit for the second integrator in the I-path

4.3.4. Bias circuit

The DC bias voltages V_{b1} and V_{b2} are generated by the bias circuit shown in Fig 4.18. V_{b2} is the output of three identical error amplifiers connected in cascade,

and V_{b2} is directly fed back to the bodies of the NMOS transistors. The negative feedback forces the operating points of the error amplifiers to be exactly at $V_{dd}/2$ regardless of PVT variations [8]. V_{b1} is generated by the right part of the circuit in Fig 4.18 to make M_1 in Fig 4.18 and thus its mirrors M_{12a} and M_{12b} in Fig 4.9 operate as constant current sources. As the voltage V_X at the bottom of R_4 is set at $V_{dd}/2$ by the negative feedback loop formed by error amplifiers Amp4 and Amp5 and M_1, the current through M_1 is

$$I_{M1} = \frac{V_{dd}}{2}\frac{1}{R_4}. \tag{4-22}$$

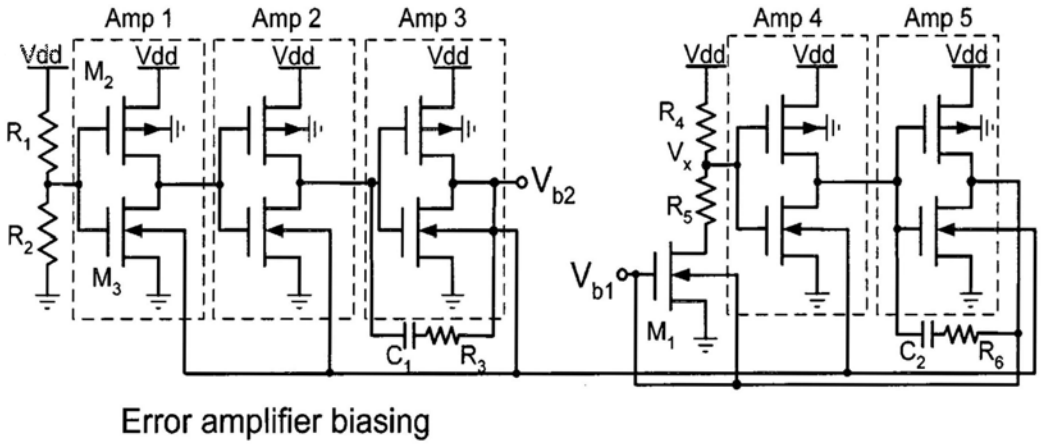


Fig 4.18 Bias generation circuit for V_{b1} and V_{b2} in Fig 4.9

This current is independent of the transistor's process variations but still depends on the supply voltage and the resistor's process variation. This causes the biasing of internal nodes (the first stage's output nodes) and the performance of the amplifier to depend on supply voltage and resistance variations. This shortcoming can be easily addressed in a future redesign by using a different biasing strategy for V_{b1}, such as using an external reference current.

The transistor sizes and component values for the biasing circuit are listed in Table 4-2.

Table 4-2 Transistor Sizes and Component Values for the Bias

Component	Value	Component	Value
M_1	1.8/0.36	R_1 , R_2	40 kΩ
M_2	7.5/0.4	R_3	8 kΩ
M_3	4/0.4	R_4	125 kΩ
R_6	10 kΩ	R_5	75 kΩ
C_2	3 pF	C_1	5 pF

4.3.5. Comparator and DAC

Fig 4.19 shows the circuit of the comparator and RTO DAC, and their transistor sizes are given in Table 4-3. The comparator has a typical latched-comparator topology [69]. However, since its input signals have a 0.25V CM level, which is not sufficient to turn on a regular gate-input comparator in this technology, this comparator uses the bodies of M_1 and M_2 as the input terminals, with the gates of M_1 and M_2 set to V_{dd} to bias them in strong inversion (see Fig 4.19). To further ensure other transistors operating in strong inversion, their body-source junctions are forward-biased as shown in the schematic.

The RTO DAC uses the topology introduced in [9]. The DAC circuit is fast enough with this technology for operation at 64MHz. When ϕ_{DAC} is high, the DAC simply produces an output of 0V or V_{dd}, depending on its input. When ϕ_{DAC} is low, the drain of M_{d5} and M_{d4} becomes a high impedance node, and may contain signal component due to parasitic coupling of input transient through C_{gd} of M_{d5} and M_{d4}. This potential signal component is then cleared by M_{d7} and the subsequent stage consisting of M_{d8} - M_{d10} produces a high impedance output that is free of input's influence. It is important to note that M_{d7} turns on slightly earlier

than M_{d8} turns off, so the outputs of the DAC momentarily short to ground before becoming floating, which is essential for the removal of any signal-dependent memory effects at the outputs.

Table 4-3 Transistor Sizes for the 0.5V comparator and DAC.

Comparator	DAC
M_1, M_2: 225/0.2	M_{d1}: 20/0.15
M_3, M_4:135/0.2	M_{d2}: 27.5/0.15
M_5, M_6: 45/0.2	M_{d3}: 80/0.2
M_7, M_8: 360/0.2	M_{d4}: 80/0.2
M_9, M_{10}: 225/0.2	M_{d5}: 80/0.2
	M_{d6}: 50/0.2
	M_{d7}: 100/0.2
	M_{d8}: 50/0.15
	M_{d9}: 50/0.15
	M_{d10}: 50/0.15

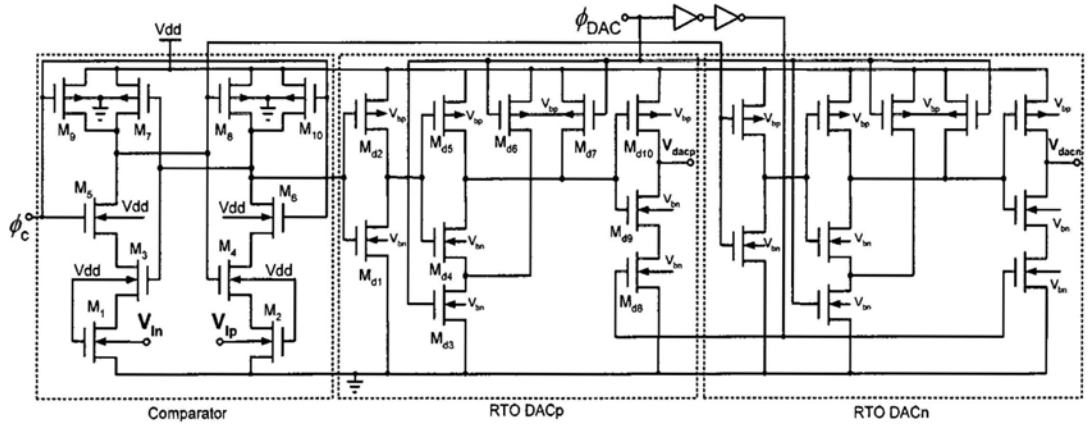


Fig 4.19 Comparator and RTO DAC circuit

4.4. Transistor-level simulation results of the modulator

As discussed above, the input CM level of the overall modulator is $V_{dd}/2$, but the input CM level of the amplifier is shifted up to 0.35V by the CM shift resistors.

Fig 4.20 shows the input nod waveform of the amplifier in the I channel. Clearly, the level of the input node is increased from 0.25V to 0.35V after a few clock cycles.

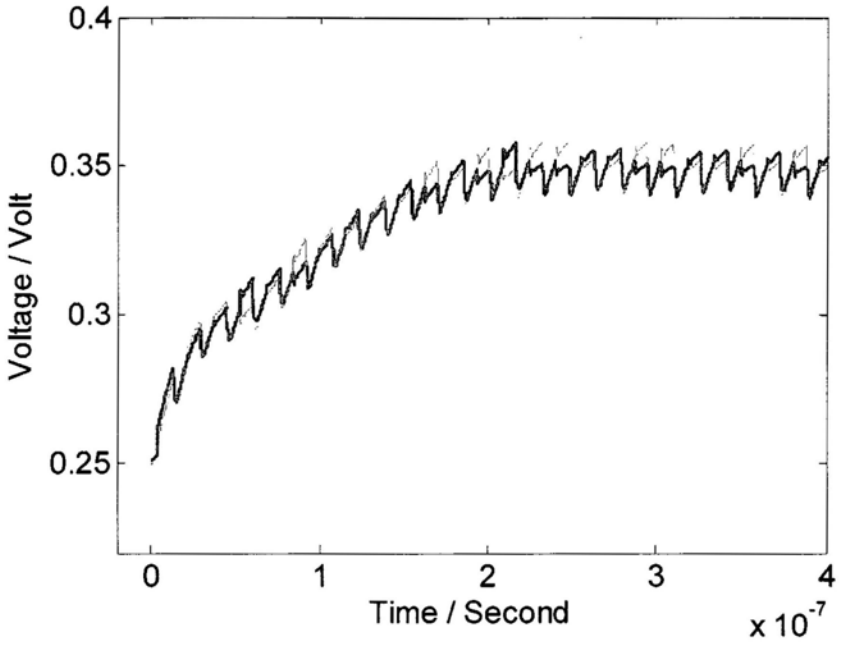
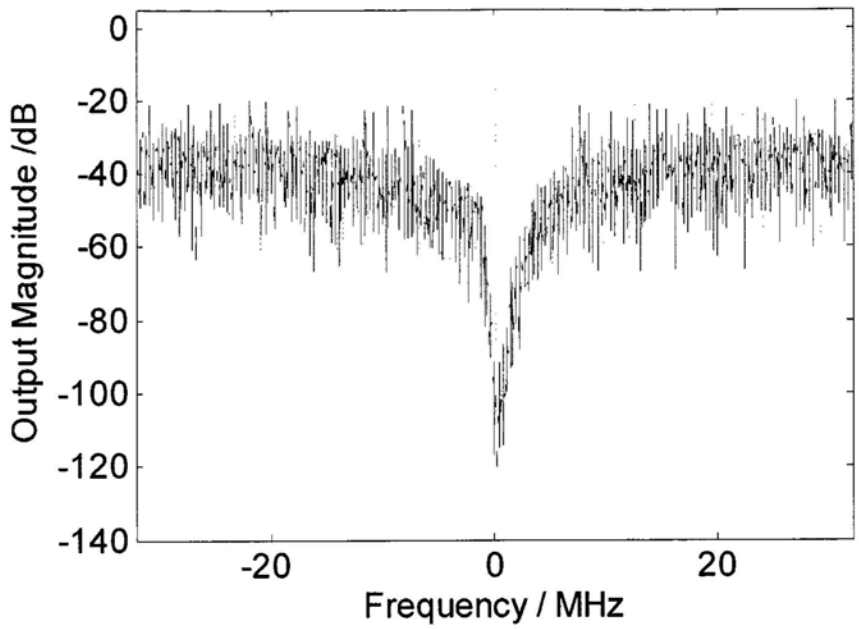
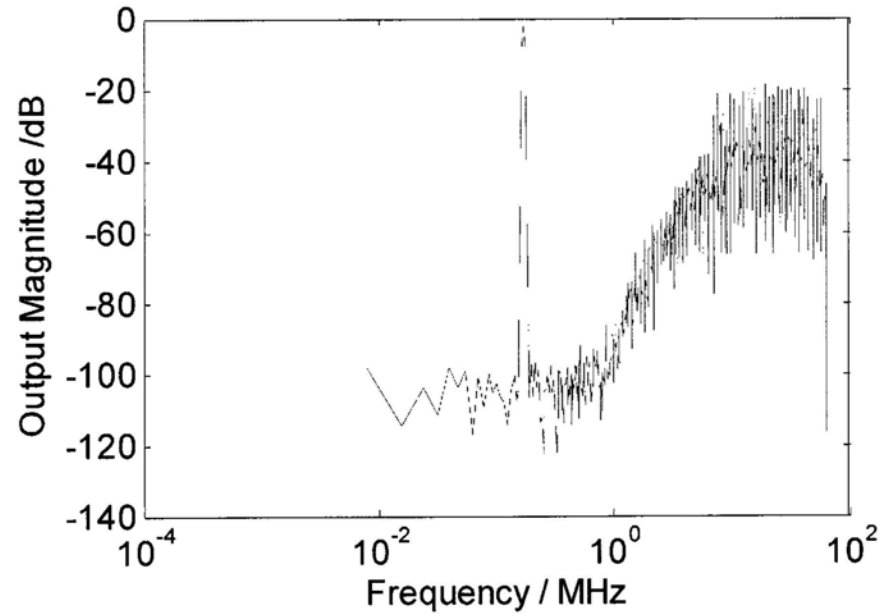


Fig 4.20 Waveform of input node of the amplifier in I channel

The whole modulator is simulated and Fig 4.21 shows the simulated performance. The peak SNR is achieved at 72.5dB with 0dB-V_{ref},+171.875kHz complex input.



(a)



(b)

Fig 4.21 Simulated output spectrum of modulator

4.5. Layout of the modulator

The CT delta-sigma modulator is essentially a mixed signal circuit. The third order filter loop filer is a pure analog circuit but it also has purely digital blocks such as the RTO control logic and clock generator. Fig 4.22 shows the chip die photo of the CT modulator which labels some major blocks. The main considerations for the floor-plan are to minimize the coupling from digital blocks to analog blocks, offset and parasitics. Several commonly used layout techniques were employed. Inter-digitization and dummy layout techniques for resistors and integrator capacitors fulfilling the loop coefficients are adopted to minimize the mismatch. A deep n-well is used to separate the clock generator and quantizer plus RTO DAC. Clock generator, RTO DAC, and the comparator have separate power supplies. The reason is that the clock to drive the DAC should have low jitter, and the comparator has four transistors stacked from V_{dd} to ground. Separated supply for comparator reduces the coupling effects from neighbor circuits and the fluctuation is also reduced.

There are total six integrators plus two comparators implemented in the modulator. A separate power supply is provided for the amplifiers in the most critical, first integrator due to its comparatively large current consumption. The other amplifiers spreading in the second and third integrators are grouped together.

The error amplifiers inside the integrator amplifiers (shown in Fig 4.9) are grouped together with the error amplifiers within the bias circuit for better match.

The design is implemented in 0.13μm triple-well mixed-signal CMOS technology. Power supplies are mainly implemented by layer metal 8 or metal 7 for their low sheet resistor. Additional amplifier of the first integrator is implemented in the silicon for measurement purpose. Four output buffers are used to help the output signal to drive the pad and measurement equipment.

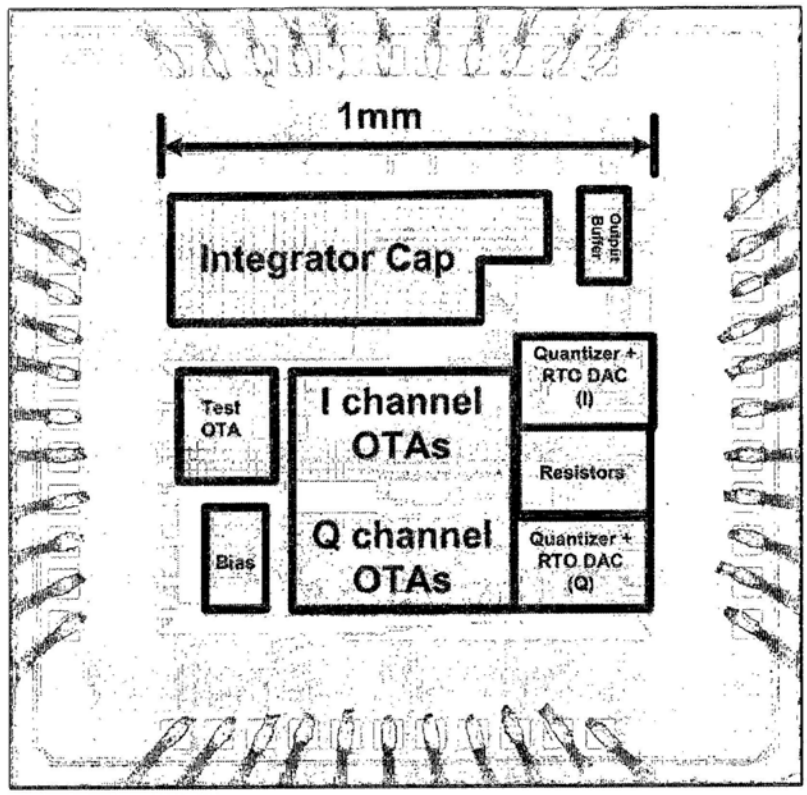


Fig 4.22 Die photo of the 0.5V complex ΔΣ modulator in a 0.13μm CMOS.

Chapter 5 Measurement results

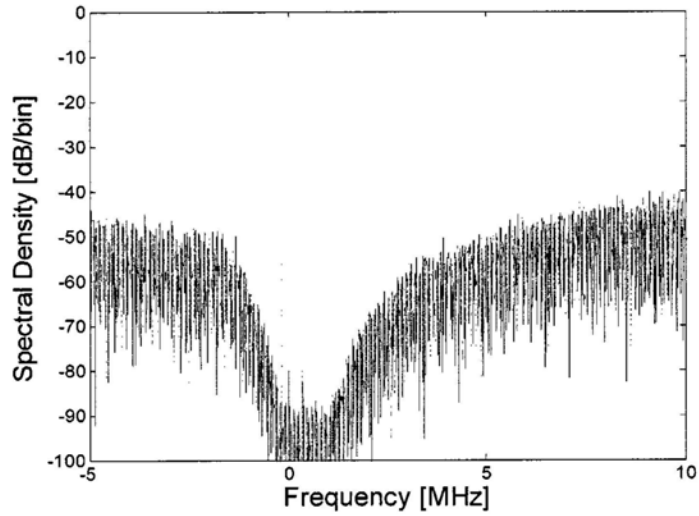
The designed modulator was fabricated in a 0.13μm triple-well mixed-signal CMOS technology. The five packaged devices available to us were tested and performed very closely. The chip consumes 3.4mW at 0.5V, breaking down to 2.98mW and 0.42mW for the analog part and digital part (comparators + DACs) respectively. The modulator occupies an active area of $0.9mm^2$. The capacitors, with a total nominal value of 94pF, account for almost half of the area.

5.1. Measurement results with 171.875KHz sine-wave input

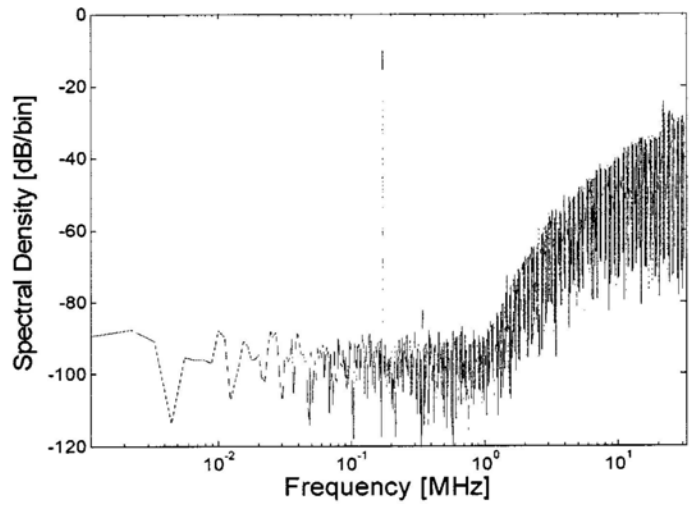
To measure the performance of the fabricated chip, a single tone of 171.875KHz is feed to the modulator. Considering the bandwidth interest of 1MHz, five harmonics can be observed

A four-channel signal generator was used to generate the four-phase input signals, i.e. differential in-phase and differential quadrature-phase inputs. The digital outputs of the modulator were captured by oscilloscope. A complex output spectrum computed off-line from captured I and Q-bit streams using Hanning windowing is shown in Fig 5.1 for a +171.875kHz, -10dB V_{ref} (V_{ref} = |1+j|Vpp-diff) complex input. The second harmonic is 70dB below the fundamental component; the third harmonic is masked by the noise floor, which is 81dB below the fundamental; and the image component at -171.875kHz is 46.3dB below the signal. The number of points in the FFT is 57344. The relatively high second harmonic is likely caused by the CM variations at the amplifier's input as shown in the simulated waveforms in Fig 4.17. The residual image component are caused by gain mismatch between the I-channel and Q-channel sub-modulators (as pointed out before, this modulator does not require separate I and Q clock phases and phase mismatch does not exist), and by gain and phase mismatches between the external I and Q inputs. As we cannot generate a perfect complex input, the image rejection capability of the modulator cannot be

measured to its fullest extent, but is at least 46.3dB, sufficient for application in low-IF receivers [24]. The measured SNDR for varying input levels and 0.5V supply is presented in Fig 5.2. A peak SNDR of 61.9dB and a peak SNR of 62.7dB are achieved in the 1MHz BW (SSB).



(a)



(b)

Fig 5.1 Measured output spectrum (a) and (b)

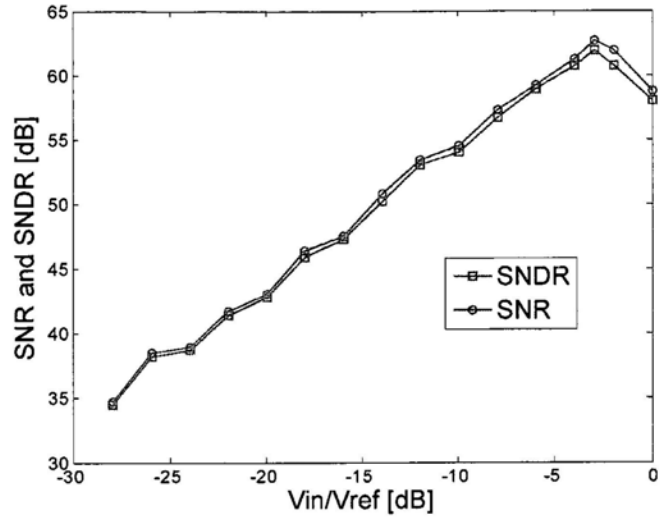


Fig 5.2 Measured SNR and SNDR versus Vin at 0.5V supply (Vref = |1+j|Vpp-diff).

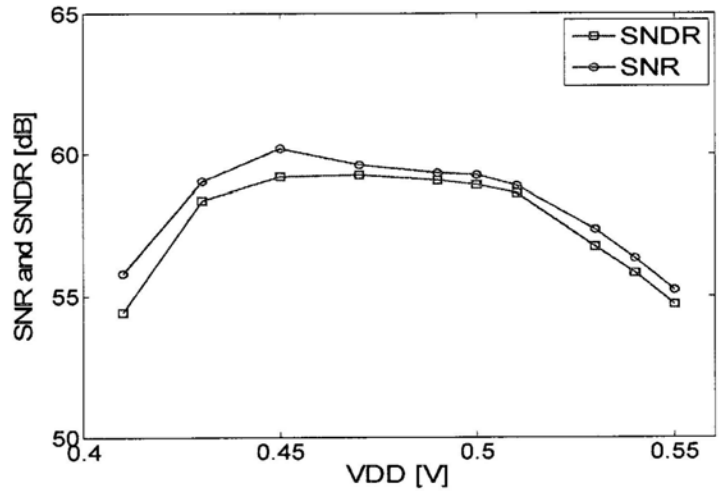


Fig 5.3 SDR and SNDR versus supply voltage

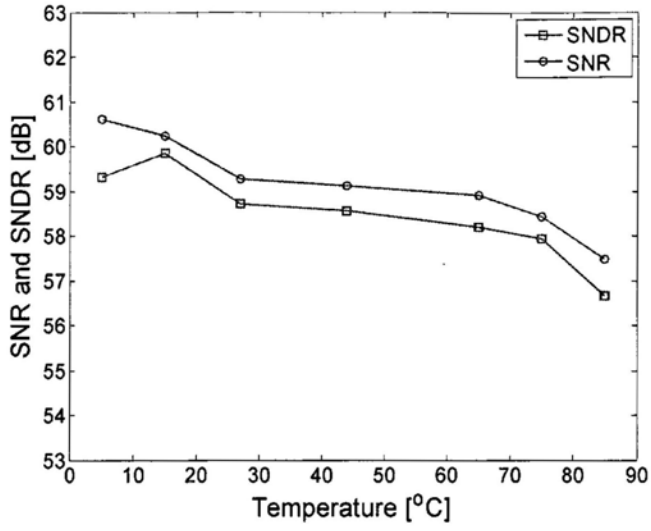


Fig 5.4 SNR and SNDR versus temperature.

Fig 5.3 shows the measured SNDR and SNR for supply voltage varying by ±10% of its nominal value and beyond. The data were recorded with a complex input of magnitude V_{in} = -6dBVref (Vref = |1+j|Vpp-diff) at room temperature (27°C). It is observed that with Vdd dropping from 0.5V to 0.45V, a very close performance is achieved, with a less than 1dB SNDR variation and a less than 1.5dB SNR variation. It stops functioning when the supply drops below 0.42V at which point the amplifiers may have become latches. On the other side, when V_{dd} increases from 0.5V to 0.55V, both the SNR and SNDR drop by about 4dB. The supply dependence of the modulator's performance is mainly due to the amplifiers. As presented in section 4.3.2, the amplifiers' DC gain is sensitive to its input common-mode level, which in turn depends on the supply voltage.

Fig 5.4 shows the SNDR and SNR for temperature varying from 5°C to 85°C, measured at V_{in} = –6dB V_{ref} (V_{ref} = |1+j|Vpp-diff) and V_{dd} = 0.5V. The modulator achieves a fairly constant performance, with less than 3dB SNR and SNDR variations for temperature ranging from 5°C to 75°C. The measured IRR for all the chips are better than 43dB. For each chip, the IRR has a virtually constant value over the whole

V_{dd} and temperature ranges as the IRR is mainly limited by gain mismatches between the I and Q signal paths caused by device mismatches.

The modulator performance is summarized in Table Table 5-1. The power consumption's dependence on supply voltage is mainly due to two reasons. First, when V_{dd} increases, the CM voltage at the amplifier's inputs increases. The current through M_{1a} and M_{2a} will then increase in a non-linear way. Second, the biasing currents for M_{12a} and M_{12b} are proportional to V_{dd}, as depicted in (4-22). The power consumption's sensitivity on supply voltage can be improved in a redesign by using a better biasing strategy.

The performance is also compared with reported low-voltage modulators in Table 5-2, where the Figure-of-Merit (FoM) is defined as:

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times 2 \times \text{Bandwidth}} \quad \text{[J/conversion step]}$$

Where ENOB = (SNDR[dB]–1.76)/6.02 is the effective number of bits. First of all, this modulator achieves a bandwidth that is 40 to 100 times wider than the reported low-voltage modulators with $V_{dd} \leq 0.8$V. Secondly, this modulator achieves the best FoM (recorded at $V_{dd} = 0.45$V) for truly low-voltage modulators (those without internal clock boosting).

Table 5-1 Performance summary

Modulator type	1-bit, 3rd order, CT, complex modulator		
Signal band	0-1MHz (SSB)		
Sampling frequency / OSR	64MHz / 64		
Input range (both I and Q) Complex	$1V_{pp\text{-}diff}$ $\|1+j\|V_{pp\text{-}diff}$		
Supply voltage	0.45 V	0.5 V	0.55 V
Dynamic Range	65.9 dB	65.7 dB	61.2dB
Peak SNDR	62.0 dB	61.9 dB	57.9 dB
Peak SNR	62.9 dB	62.7 dB	58.2 dB
Image rejection ratio	46.8 dB	46.3 dB	45 dB
Power consumption (Total, exclude o/p buffers) Analog (Amplifiers + Bias) Digital (Comparator + DAC)	1.8 mW 1.44 mW 0.36 mW	3.4 mW 2.98 mW 0.42 mW	5.88 mW 5.25 mW 0.62 mW
Active die area	0.9 mm^2		
Technology	0.13 μm CMOS (standard V_T, triple-well, MIM, and HiRes Poly)		

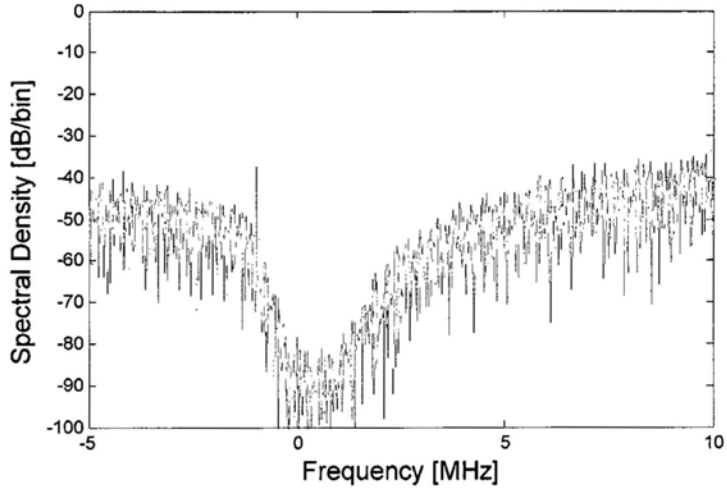
Table 5-2 Performance comparison with sub-1V Delta-Sigma modulators

	VDD [V]	Type	Internal Voltage Boosting	SNDR [dB]	ENOB (bit)	Band-width [kHz]	Power [μW]	Area [mm^2]	CMOS [μm]	FOM [pJ/conv.]
Ueno'04 [16]	0.9	CT	No	50.9	8	1920	1500	0.12	0.13	1.36
Peluso'98 [71]	0.9	SO	No	62	10	16	40	0.85	0.5	1.22
Goes'06 [12]	0.9	SO	Yes	80	13	10	200	0.06	0.18	1.22
Révérend'03 [13]	0.8	SC	No	64	10	10	60	0.23	0.35	2.32
Sauerbrey'02 [14]	0.7	SO	No	67	11	8	80	0.082	0.18	2.73
Chae'08 [11]	0.7	SC	Yes	81	13	20	36	0.715	0.18	0.098
Park'09 [70]	0.7	SC	Yes	95	15	25	870	2.16	0.18	37.9
Ahn'05 [10]	0.6	SRC	No	77	12	24	1000	2.88	0.35	3.60
Ishida'05 [15]	0.5	SC	No	39.6	6	8	75	0.025	0.15	60.1
Pun'06 [9]	0.5	CT	No	74	12	25	300	0.6	0.18	1.46
This work	**0.5**	**CT**	**No**	**61.9**	**10**	**1000**	**3400**	**0.9**	**0.13**	**1.67**
This work	**0.45**		**No**	**62.0**	**10**		**1800**			**0.87**

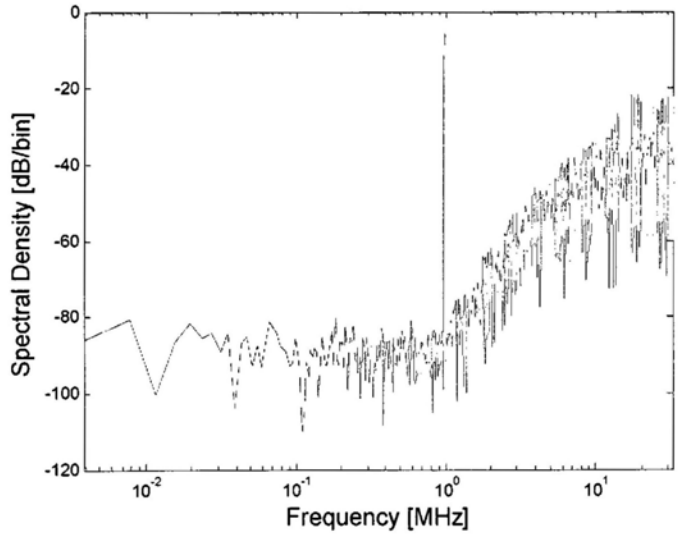
SO = Switched Opamp; CT = Continuous-time;
SC = Switched Capacitor; SRC = Switched-RC.

5.2. Measurement result with 1MHz sinewave input

The bandwidth of the designed modulator is 1MHz. To demonstrate its performance at the bandwidth limit, the fabricated prototype is also measured with 1MHz input sine-wave.



(a)



(b)

Fig 5.5 Measured output spectrum (a) and (b) with 980.5kHz input

Fig 5.5 shows the measured output spectrum for a +980.5kHz, -5dB V_{ref} (V_{ref} = |1+j|Vpp-diff) complex input. The measured output SNR is 58.5dB shown in fig 5.5. The number of points in the FFT is 16834.

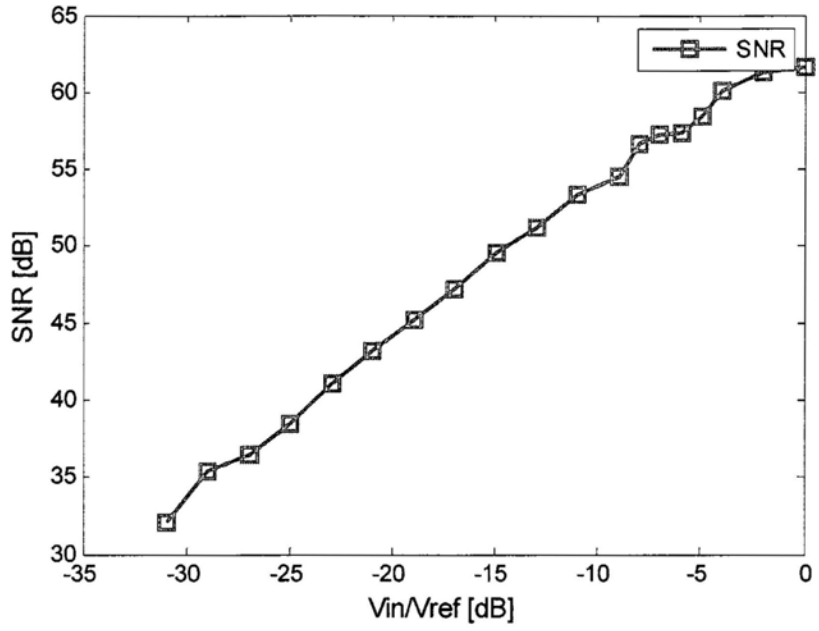


Fig 5.6 Measured SNR versus Vin at 0.5V supply with fin=980.5kHz.

The measured SNR for varying input levels at 0.5V supply is presented in fig 5.6. The measured peak SNR is 61.6dB with FS input in the 1MHz BW(SSB). Compared to measurement result with +171.875kHz input, the performance of the modulator shows no dependence of input frequency within the designed bandwidth. Even though the performance of the modulator with varying supply voltage/temperature when fed with 1MHz input is not measured, the performance is very likely similar to those with 171.875kHz input based on the measurement results of varying input level.

Chapter 6 A 0.5V Amplifier for a 1MHz CT Complex Delta-Sigma Modulator

The amplifier discussed in chapter 4 adopts pseudo-differential input stage and additional devices are used to implement the CM signal cancellation, which is not area and power efficient. This chapter presents a wideband amplifier with truly differential input stage and the amplifier still operates in 0.5V [73]. The amplifier employs a gate-input two-stage structure and a DC common-mode feedback circuit that uses a Miller-amplified capacitor for frequency compensation. Designed in a 0.13μm triple-well CMOS process with regular V_T transistors, the amplifier achieves a simulated performance of 51dB DC open-loop gain, 112MHz unity gain-bandwidth and 67° phase margin with a load of 6.5pF//19.6kΩ, and consumes 600μW at 0.5V supply. The proposed amplifier is incorporated in the CT complex delta-sigma modulator synthesized previously in Chapter 3. Simulation results show that the modulator achieves a 72.5dB SNDR and consumes 2.3mW at 0.5V.

6.1. 0.5V wide band amplifier

In the proposed amplifier design, 0.13μm triple well CMOS process is selected for access to the body terminals of n-channel transistors. The n- and p-channel transistors used have regular threshold voltages of 0.22V and –0.25V, respectively.

Fig 6.1 shows the schematic of the proposed 0.5-V wideband fully differential amplifier with rail-to-rail output. It consists of two gain stages and a DC CMFB stage that utilizes a Miller-amplified capacitor for frequency compensation. The designed values for the input and output CM voltages are 0.4V and 0.25V, respectively, for the nominal supply voltage. The former is to provide a sufficient overdrive for high speed operation and the latter is for maximum output voltage swing.

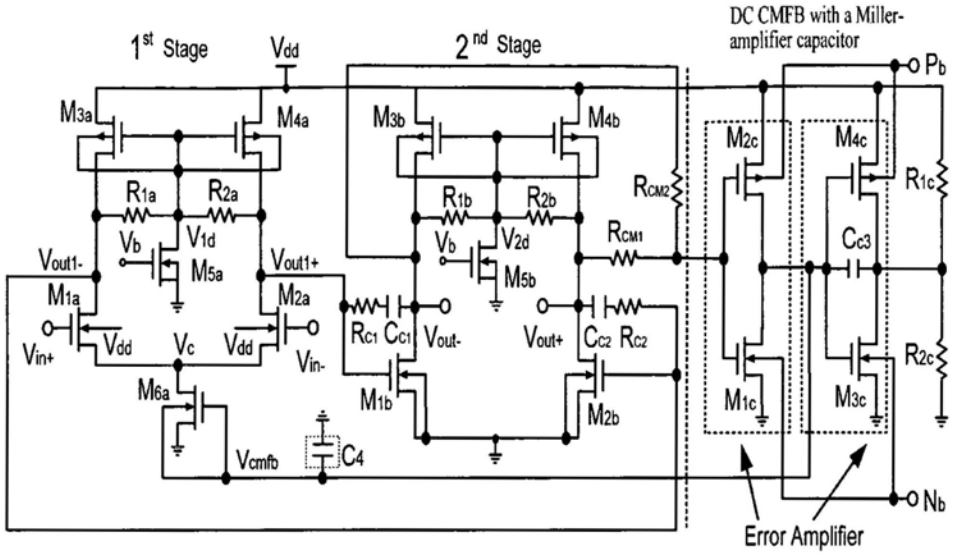


Fig 6.1 The fully differential amplifier with overall miller-compensated CMFB Loop.

Table 6-1 Transistor Sizes and Component Values for amplifier

Component	Value	Component	Value
M_{1a} , M_{2a}	350/1	R_{1a} , R_{2a}	100 kΩ
M_{3a} , M_{4a}	200/1	R_{1b} , R_{2b}	100 kΩ
M_{1b} , M_{2b}	97/1	R_{CM1} , R_{CM2}	100 kΩ
M_{3b} , M_{4b}	250/1	R_{C1} , R_{C2}	500
M_{5a}	11/2	C_{C1} , C_{C2}	6pF
M_{5b}	5.5/2	C_{C3}	5 pF
M_{6a}	450/1	M_{1c}	4/0.36
M_{2c}	14.4/0.36	M_{3c}	16/0.36
M_{4c}	57.6/0.36	R_{1C} , R_{2C}	15 kΩ

The first stage of the amplifier adopts the traditional gate-input differential pair structure, which has good common-mode rejection capability. Gate-input approach is chosen over body-input one for higher transconductance [8], which leads to better gain, speed and noise performance. However, gate-input approach requires a high input CM level and thus puts a constraint on the system level design. The input transistors M_{1a} and M_{2a} further have their bodies biased to V_{dd} to lower the threshold to increase their speed. Under a 0.5V supply, latch-up is not a problem [8], M_{3a}, M_{4a}, R_{1a} and R_{2a} form a local CM feedback loop [74], which suppresses the

CM gain (the tail current source M_{6a} also contributes to the CM suppression) but does not affect the differential-mode gain as long as the values of R_{1a} and R_{2a} are sufficiently large. M_{5a} acts as a current source to create a DC level shift between the gate and drain of M_{3a}.

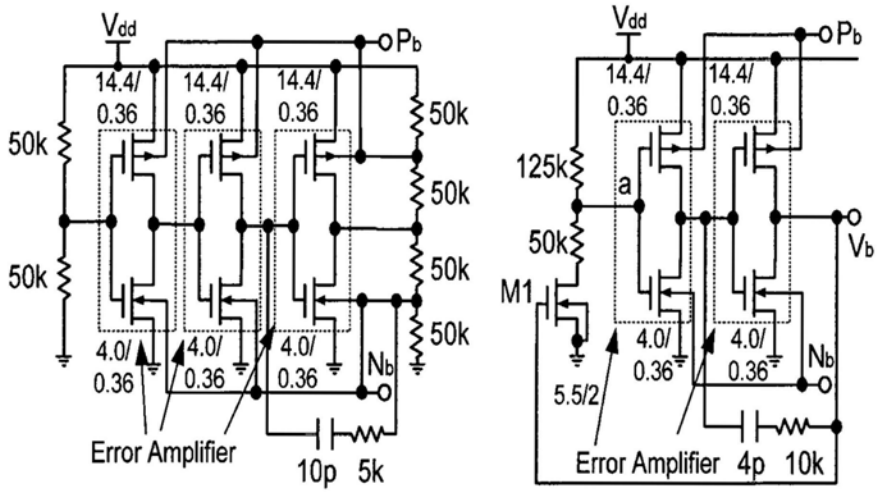


Fig 6.2 Bias generation circuit for the amplifier

The second stage is similar to the first stage except that the tail current of the differential pair is removed to allow for a sufficient gate-source voltage for the input pair (M_{1b}, M_{2b}). The CM output level of the first stage is around 0.33V under nominal condition, biasing the input transistor of the second stage in strong inversion. A local CMFB loop formed by M_{3b}, M_{4b}, R_{1b} and R_{2b} is used to suppress the CM gain in this stage.

One way to control the output DC level to the desired value of $V_{dd}/2$ is the master-slave approach as reported in [8]. In that approach, the master circuit, consisting of a replica of the main amplifier, adjusts the biasing voltage V_b in a feedback loop to achieve the desired output CM level for both the master and the

slave (the main amplifier). However, different replicas are needed for differently sized amplifiers. In applications like the complex third-order ΔΣ modulator discussed in chapter 4, three types of amplifiers and thus three replicas would be needed, which is power- and area- inefficient even if scaled-down versions of the amplifiers can be used. Moreover, the matching between the master and slaves can further be a limiting factor.

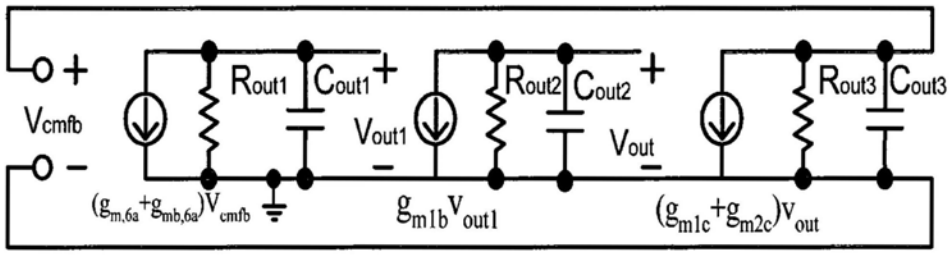


Fig 6.3 Small signal model of the CMFB loop

In this proposed amplifier topology, we use a simple DC CMFB stage for each amplifier as shown in Fig 6.1. The bias signal P_b, N_b and V_b generated by the circuit shown in Fig 6.2 make the error amplifiers have their threshold voltage exactly at $V_{dd}/2$ irrespective of process/voltage/temperature (PVT) variations [8][9]. The voltage at node a in Fig 6.2 is precisely set to $V_{dd}/2$ regardless of PVT variation by the feedback loop consisting of two error amplifiers and the current source M_1, and the current of M_1 is exactly equal to 2μA in normal conditions.

The first error amplifier in Fig 6.1, consisting of M_{1C} and M_{2C}, compares its threshold level ($V_{dd}/2$) with the amplifier's output CM level, feeding back the error voltage to control the current source M_{6a}. The second error amplifier, consisting of M_{3C} and M_{4C}, is four times as big in size as the first error amplifier. It amplifies the

capacitance of C_{C3} to provide a large capacitive load to the first error amplifier for frequency compensation of the CMFB loop. The small signal model of the CMFB loop is shown in Fig 6.3. R_{out1}, C_{out1} and R_{out2}, C_{out2}, are the resistors and capacitors in the output of the first and second stage, respectively. R_{out1} is $1/(g_{m,3a}+g_{mb,3a}+g_{ds,3a})$, and R_{out2} is $1/(g_{m,3b}+g_{mb,3b}+g_{ds,1b}+g_{ds,3b})$. It should be noted that C_{C1} and C_{C2} in Fig 6.1 encounter negligible Miller amplification for common-mode signals because the common-mode gain of the second stage is very small, equal to $g_{m,1b}/(g_{m,3b}+g_{mb,3b}+g_{ds,3b}+g_{ds,1b})$. R_{out3} is $R_{ds,1C}//R_{ds,2C}$; C_{out3} is the Miller-amplified capacitor and equals to $C_{C3}(g_{m,3C}+g_{m,4C})R_{ds,3C}//R_{ds,4C}//R_{1C}//R_{2C}$.

If the Miller-amplification technique is not used, the poles at the outputs of first stage, second stage and the error amplifier would be closely located in frequency domain, resulting in negative CMFB loop phase margin. With the use of the Miller-amplification, the pole at the error amplifier's output becomes dominant and a satisfactory PM is achieved.

A problem of using the error amplifier (M_{3C}, M_{4C}) for Miller amplification is that its output (node c in Fig 6.1) can easily drift to V_{dd} or ground, given the large gain of this error amplifier and with PVT variations, leaving the error amplifier out of its high gain region and diminishing the Miller amplification effect. To tackle this problem, R_{1C} and R_{2C} are added to force this error amplifier to stay in strong inversion, ensuring its high gain against PVT variations.

Obviously, a huge capacitor C_4 (in dotted box in Fig 6.1) between V_{cmfb} and ground can also stabilize the CMFB loop. Simulation result shows that a C_{C3} of 5pF is equivalent to the effect of a C_4 of 240pF, 48 times larger.

The transistor sizes and component values for the amplifier are given in Table 6-1. The lengths of $M_{1a}-M_{4a}$ and $M_{1b}-M_{4b}$ are about eight times of the minimum channel length. Increasing the transistor length improves the output impedance and also reduces the threshold voltage in advanced CMOS technology. The channel lengths of current source transistors M_{5a}, M_{5b} are large (2μm) for better matching and higher output impedance. Constant currents of M_{5a} and M_{5b} are useful for the local CMFB loop to maintain high CM rejection against PVT variation.

Table 6-2 Simulated performance of the proposed amplifier

Power supply (V)	0.45			0.5			0.55		
Temperature (°C)	0	27	85	0	27	85	0	27	85
DC open loop gain (dB)	52.5	48.5	40	55.3	51	42	55.2	51.9	45
UGF(MHz)	52	61	62	103	112	107	195	192	166
PM	54°	59°	69°	66°	67°	71°	62°	63°	67°
SR+ (V/us)	12.89	13.61	15.69	21.8	23.34	23.9	29.69	34.18	36.91
SR- (V/us)	11.8	12.05	12.28	20.35	21.83	21.98	26.50	28.62	34.09
Noise @1KHz (nV/√Hz)	13.24	13.9	16.9	13.43	14.3	16.6	13.93	14.95	17.01
Noise @1MHz (nV/√Hz)	3.22	3.18	3.42	2.5	2.5	2.7	2.05	3.1	2.30
CMRR @DC (dB)	128.5	124.5	115.6	129	124	114	123.8	119	113
CMRR @1MHz (dB)	66.5	69	69	72	83.5	72	74	74	77
PSRR+ @ DC (dB)	56.9	53.3	47.7	60.2	55.9	49.7	60.2	55.9	48.9
PSRR- @ DC (dB)	57.1	53.2	47.7	59.9	55.7	49.7	59.8	55.5	48.8
Power Consumption (μW)	240	333	453	469	600	760	819	990	1080

The amplifier achieves a 51dB DC open-loop gain and a 112MHz UGF in simulation under nominal conditions. Table 6-2 summarizes the simulated performance of the amplifier. The simulated frequency responses under PVT corners (0°C to 85°C, 0.45V to 0.55V, plus process corners) are shown in Fig 6.4. The

amplifier achieves a DC CMRR of over 110dB for all corners, much higher than those amplifiers reported in [8][9][67]. The PM of overall CMFB loop is at least 39° for any of the above mentioned PVT combinations. A low level of input referred noise is also achieved due to the high gm and large sizes of the input differential pair. The slew rate is also comparable to classical amplifiers even though it is not critical for CT ΔΣ modulators. At 0.45V supply, the amplifier still achieves 61MHz UGF and 59°PM, and consumes 333μW only.

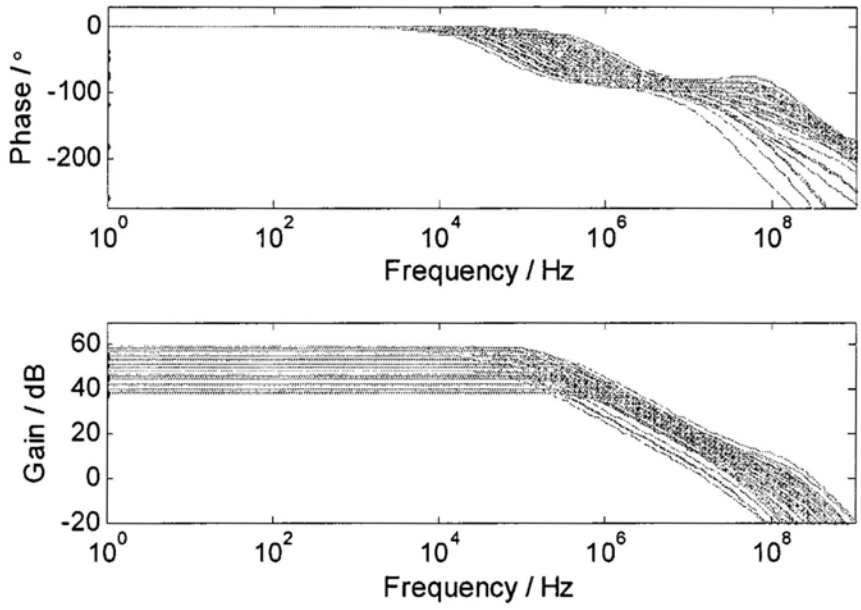


Fig 6.4 AC response of the amplifier over PVT corners

6.2. The Modulator Design

The proposed amplifier is incorporated in the modulator, which has the same topology as the one shown in Fig 4.6. The modulator discussed in this chapter is also operating in 64MHz with OSR 64, but its resistor or capacitor values are optimized for power and area efficiency. Fig 6.5 shows the architecture of the CT complex delta-sigma modulator, where the proposed amplifier is applied. The circuit is shown in the single-end form for simplicity and the actual circuit is realized in fully-differential form.

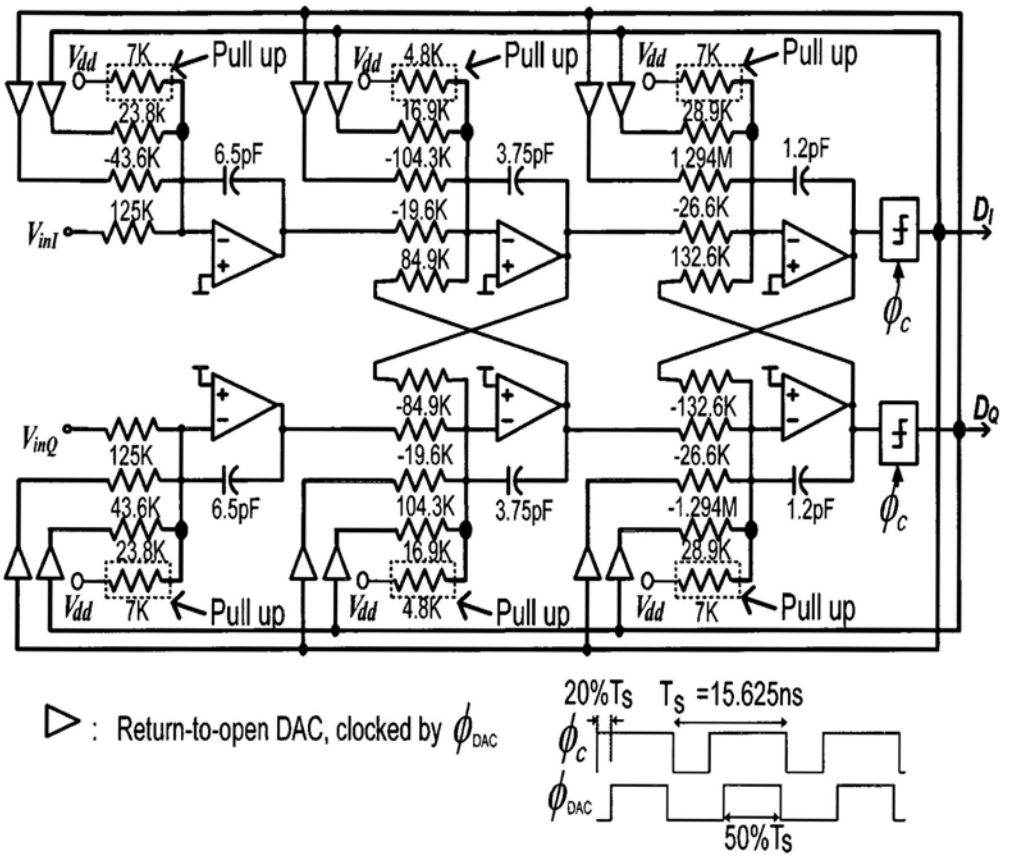


Fig 6.5 Simplified schematic of the ΔΣ modulator

As discussed in section 6.1, the input CM levels of the amplifiers are set to 0.4V, instead of $V_{dd}/2$, to meet the speed and gain requirements in different PVT corners. The output CM level is set to $V_{dd}/2$ for maximum signal swing. A CM level shift technique for low-voltage CT delta-sigma modulators has been reported in [75], which needs switches in its operation. In this design, a simpler solution, which does

not need switches, is adopted. The scheme is briefly described below. To pull up the

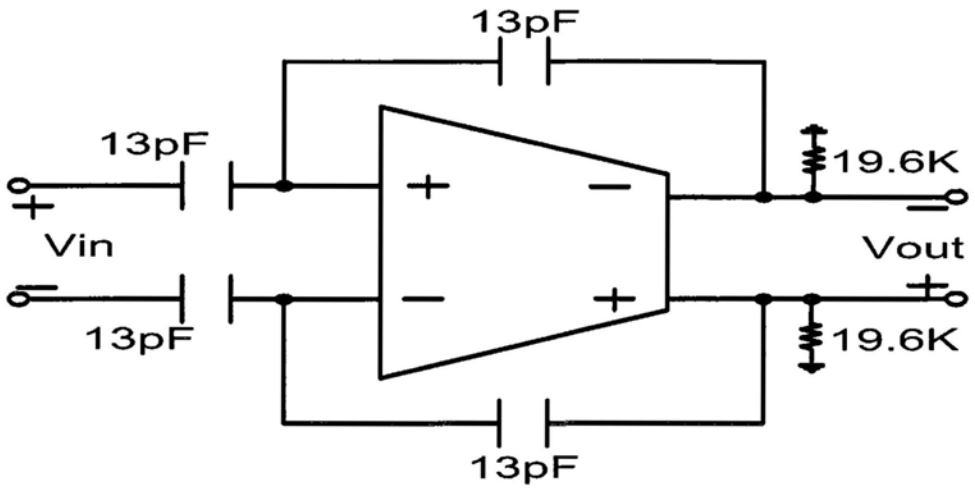


Fig 6.6 Schematic for simulation of amplifier's output settling.

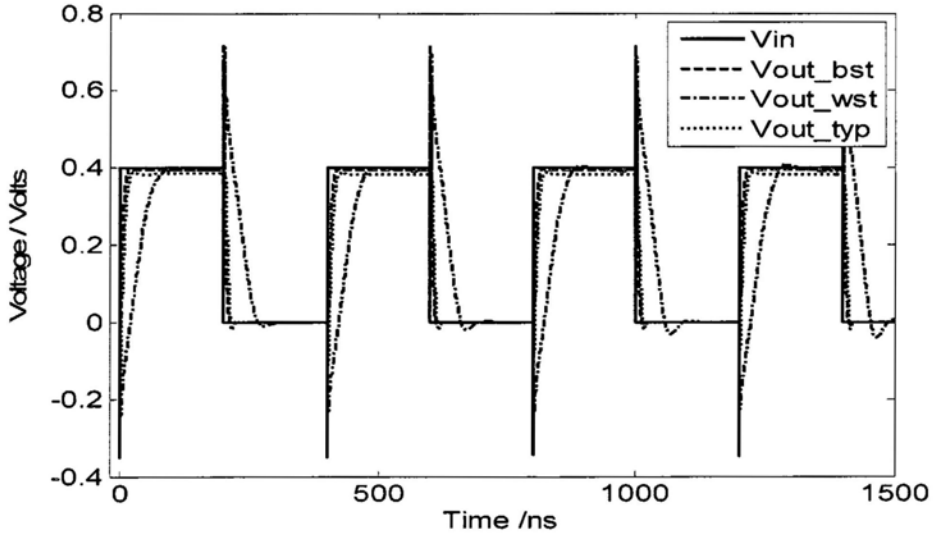


Fig 6.7 Differential output waveform of the amplifier

CM level of amplifier's inputs from $V_{dd}/2$ to the desired level of 0.4V, a pair of pull-up resistors, connected to V_{dd}, is used for each amplifier. As the RTO DAC [9]

is used, the CM voltage at the amplifier's inputs varies when the DAC switches between the active state and inactive (open) state. However, due to the short clock period relative to the RC time constants at the amplifier's inputs, this CM voltage variation is small.

The amplifier shown in Fig 6.1 is used in the 1st stage. The amplifiers for the second and third stages use the same topology but their currents are scaled down for their smaller load capacitors and that the non-idealities introduced by these stages are at least first-order high-pass shaped by the modulator. The ratio of current consumption between the first, second and third stages is 2.9:1.7:1. The amplifiers in the second and third stages, with their respective load, achieve a very close performance (except the power) to the first amplifier in all process corners. When the power supply increased to 0.55V or downed to 0.45V, the amplifier's input CM level is slightly above or below 0.4V. However, simulations indicate that the amplifier's performance is virtually not affect by this small CM level variation.

The comparator used in this modulator is basically a classical latched-comparator but with the bodies of its input devices used as the input terminals to accommodate an input CM signal level of $V_{dd}/2$. The gates of the input devices are set to V_{dd} to ensure strong inversion mode of operation. The RTO DAC topology [9] is used and scaled for fast operation for the 64MHz clock. The RTO DAC operates in two phases: active phase, (ϕ_{DAC} high) and inactive phase (ϕ_{DAC} low). The rising edge of ϕ_{DAC} for the DAC is delayed by 20%Ts from the rising edge of ϕ_C for the comparator to allow complete settling of the comparator, shown in Fig 6.5.

6.3. Simulation Results

Apart from simulations reported in section 6.1, the proposed amplifier is also simulated with square wave stimulus to verify its stability and output settling, as shown in Fig 6.6. Ignoring the parasitic capacitors at the output nodes, the equivalent capacitor and resistor load for the amplifier are 6.5pF and 19.6K, respectively,

identical to the first amplifier's load in the modulator. The amplitude of the square-wave input is $0.4V_{pp,diff}$, for producing full swing outputs. Note that the single-ended output full swing is 0.2Vpp, which is 0.3V lower than the 0.5V supply for leaving 0.15V drain-source headroom for M_{1b}, M_3 (in Fig 6.1) each.

Fig 6.7 shows the simulated transient waveform of the amplifier's differential output. In normal conditions, the output settles to 99% of the final value within 22.1ns for $0.4V_{pp,diff}$ output and to 99.9% in 22.5ns for a 0.2 $V_{pp,diff}$ output. The best and worst case scenarios are also simulated and no stability problem occurs.

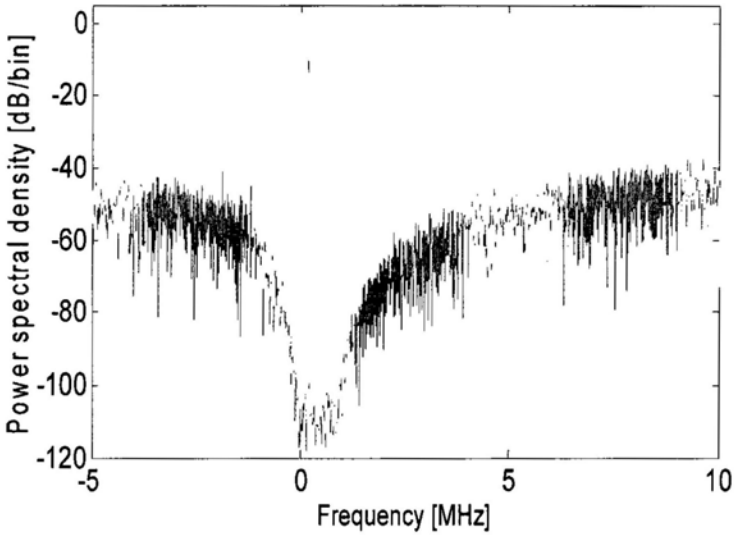


Fig 6.8 Simulated output spectral density double-sided plot

Fig 6.8 and Fig 6.9 show the simulated output power spectral density of the modulator adopting the proposed amplifier under nominal conditions for 0dB-V_{ref}, +171.875kHz complex input. The number of points in the FFT is 16834. The achieved peak SNDR is 72.5dB. At the supply voltage of 0.45V and 0.55V, the simulated SNDR values are 64.2dB and 72.9dB respectively. The modulator performance versus temperature is also simulated. Under 0.5V supply the nominal process conditions, the modulator achieves an SNDR of 54.9dB, 57.8dB, 60.7dB,

72.5dB, 70.9dB, 69.7dB and 67dB at -15°, 0°, 5°, 27°, 45°, 65° and 85°, respectively. All the simulations reported in this manuscript are pre-layout simulations which include estimated parasitics for all capacitors.

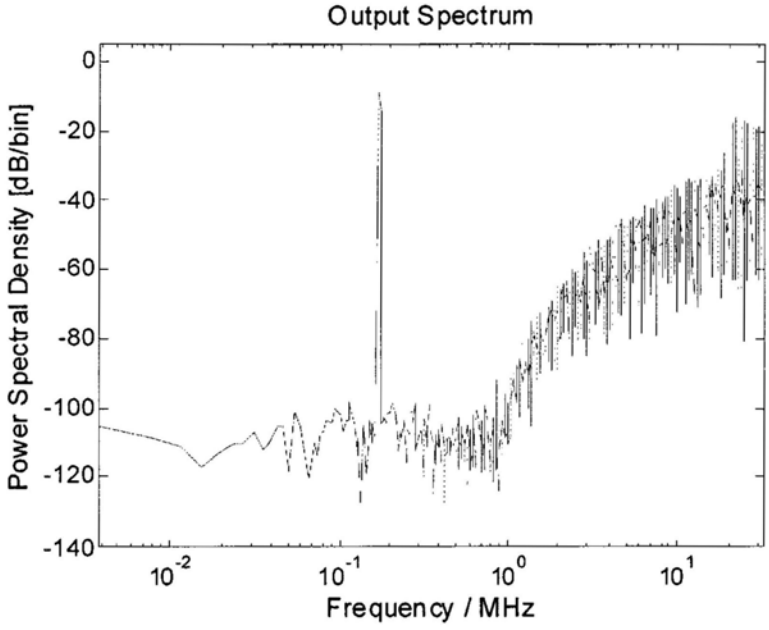


Fig 6.9 Simulated output spectral density of the modulator single-sided

Chapter 7 Dynamic CM shift technique for CT Delta-sigma modulator

The amplifiers used in modulator in Chapter 4 and Chapter 6 have a input CM level over $V_{dd}/2$. CM level shifters are used to enable the amplifiers' operation in the modulator. Due to the high frequency operation, 64MHz, the clock cycle is relatively small compared to the time constant associated with the input terminal of the amplifiers, as discussed in Chapter 4 and Chapter 6. However, for low frequency operation, because the clock period is more than the time constant, the input CM level of the amplifier would vary when output DAC switched between active and inactive (open) state. To solve this problem, dynamic CM level shift technique for CT delta-sigma RTO DAC modulator is discussed in this chapter.

7.1. Dynamic CM shift techinque

The CM level shifting technique used in Chapter 4 and Chapter 6 or the technique reported in [76] has limited use for low speed modulator with RTO DACs, because the OTA input CM varies when the DAC changes its state from active to open or vice versa. The dynamic CM shift technique presented below is used to address this problem for CT modulators employing an RTO DAC.

Fig 7.1 shows an integrator stage in an active-RC modulator that employs RTO DACs. The desired CM input voltage V_{CM1} at the OTA inputs, i.e., nodes "***a***" and "***b***" in Fig 7.1, is set to 0.35V in order to use a gate-input OTA with NMOS input transistors operating with $V_{dd} = 0.5V$. The input signal (V_{in}) has a CM voltage ($V_{in,cm}$) of $V_{dd}/2$ for maximum signal swing. To pull up V_{CM1} due to the lower value of

$V_{in,cm}$, two equal-valued resistors, R_{1acp} ,and R_{1acn}, connected between the OTA inputs and V_{dd}, are added as in [8][76]. Ignoring R_{1bp}, R_{1bn}, R_{1bcp}, and R_{1bcn} for now, V_{CM1} is governed by the following expression:

$$\frac{V_{dd}-V_{CM1}}{R_{1ac}}=\frac{V_{CM1}-V_{in,cm}}{R_{1a}} \qquad (7\text{-}1)$$

where $R_{1a}=R_{1ap}=R_{1an}$ and $R_{1ac}=R_{1acp}=R_{1acn}$. If we choose R_{1ac} = 1.5x R_{1a}, then $V_{CM1}=0.35V$.

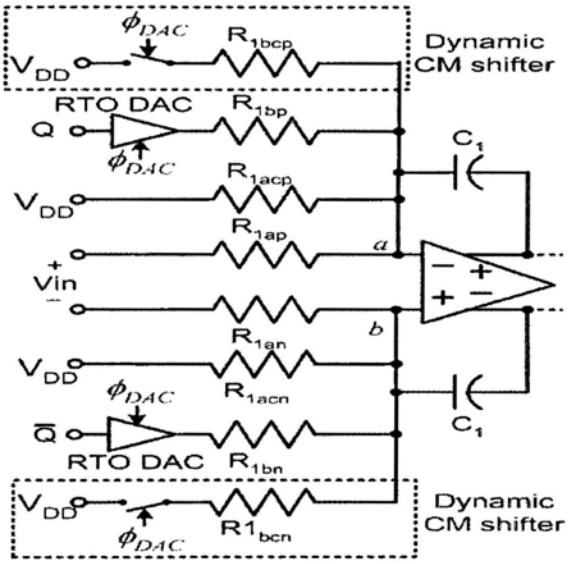


Fig 7.1 An active RC integrator stage and dynamic CM level shifting

Now consider the effect of the RTO DACs on V_{CM1}. Assume that the time constants associated with the DACs' output nodes (due to parasitic capacitors) are much shorter than the clock period such that the RTO operation can be considered ideal [9]. In the inactive phase (ϕ_{DAC} low), the outputs of the RTO DACs are open-circuited and draw no current so V_{CM1} is not affected. In the active phase (ϕ_{DAC}

high), the DAC in the upper half circuit and the one in the lower half circuit have their output connects to V_{dd} or GND (depending on their inputs Q and $\overline{Q}$) in a complementary manner. So, in this phase, the CM output voltage ($V_{DAC,cm}$) at the RTO DACs' outputs is $V_{dd}/2$. This will pull down V_{CM1} through resistors R_{1bp} and R_{1bn}.

To eliminate this CM variation, we add another pair of resistors, R_{1bcp} and R_{1bcn}, connected from the OTA inputs to V_{dd} through switches controlled by ϕ_{DAC} (see Fig 7.1). The switches are implemented by a PMOS transistor with its gate connected to $\overline{\phi_{DAC}}$ and its body tied to V_{dd}. When ϕ_{DAC} is low, the switches are opened and no current flows through R_{1bcp} and R_{1bcn}, so V_{CM1} is not affected and is still governed by (7-1). When ϕ_{DAC} is high, the switches are closed and R_{1bcp} and R_{1bcn} are connected to V_{DD} and will pull up V_{CM1} and counter act the pull down effect of $V_{DAC,cm}$ on V_{CM1}. The equation governing V_{CM1} in this phase is:

$$\frac{V_{dd}-V_{CM1}}{R_{1ac}}+\frac{V_{dd}-V_{CM1}}{R_{1bc}}=\frac{V_{CM1}-V_{in,cm}}{R_{1a}}+\frac{V_{CM1}-V_{DAC,cm}}{R_{1b}} \qquad (7\text{-}2)$$

Where $R_{1bc}=R_{1bcp}=R_{1bcn}$. If we choose R_{1bc} = 1.5x R_{1b} and with R_{1ac} = 1.5x R_{1a}, we have $V_{CM1}=0.35V$. Therefore, V_{CM1} is kept at a constant level of 0.35V in both active and inactive phases of the RTO DAC. Note that the CM level shifting resistors have no effect on the differential transfer function of the integrator.

The CM shifting in subsequent stages is defined in the same way since the CM voltage of all the amplifiers' outputs are $V_{dd}/2$, the same as $V_{in,cm}$, for maximum signal swing.

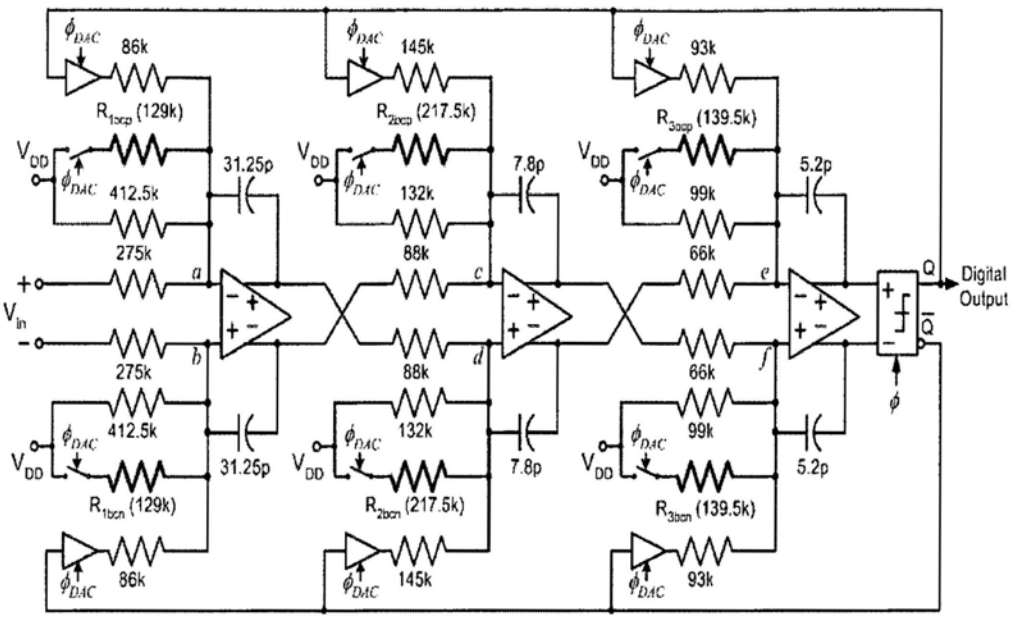


Fig 7.2 A 3rd 1-bit CT low-pass modulator with dynamic CM level shifting

7.1. Simulation results

Fig 7.2 shows the complete circuit of a 0.5V third order 1-bit CT low-pass modulator. The modulator topology is the same as the one in [9] except that gate-input OTAs as in [8] were used and the proposed CM level shifting technique is applied. The sampling rate of the modulator is 3.2MHz and the clocks are the same as in [9]. The modulator was designed in a 0.13μm triple-well CMOS process. The RTO DAC circuit is the same as the one in [9], and a gate-input comparator was designed using low threshold devices.

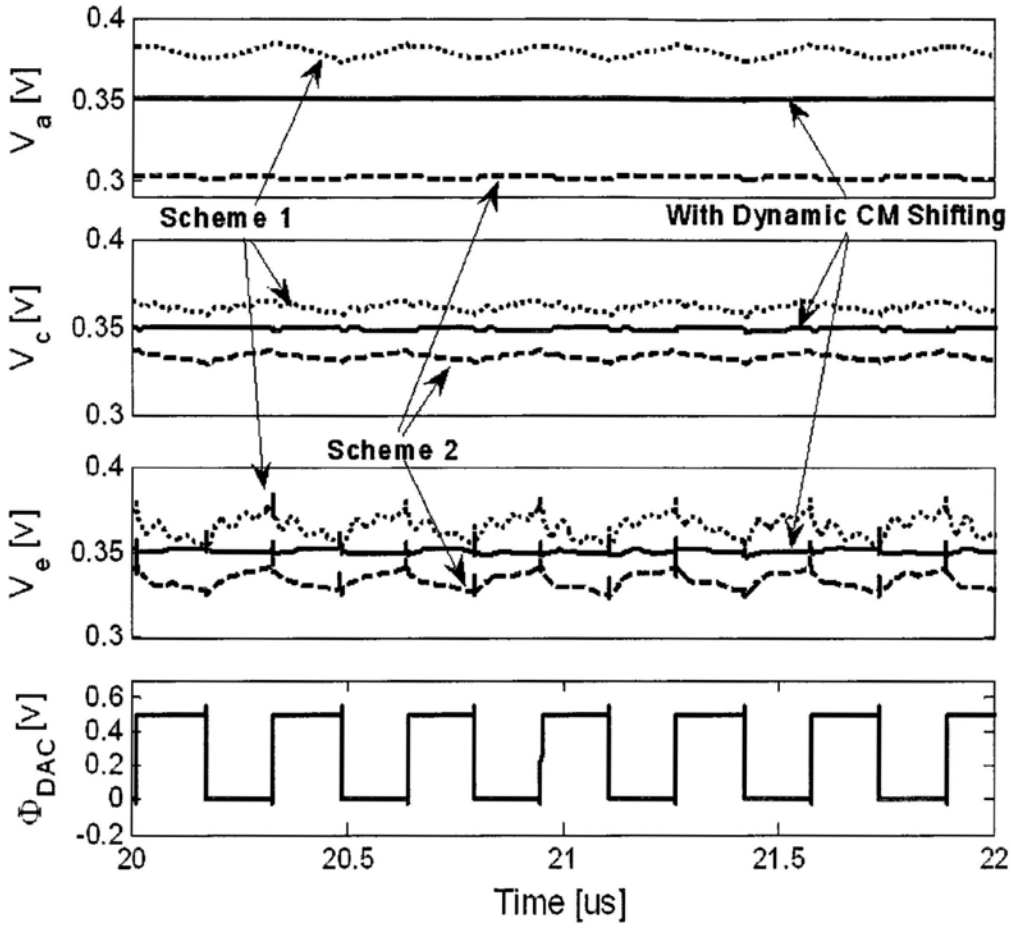


Fig 7.3 Simulated waveforms at nodes a, c and e for different CM shifting techniques

Fig 7.3 shows the simulated waveforms of the OTAs' input nodes a, c and e (see Fig 7.2) (waveforms at nodes b, d and f are identical to those at nodes a, c and e respectively) for different CM shifting techniques. We can see that the OTAs' input voltages are maintained at 350mV when the dynamic CM shifting technique is applied (solid curves). The dashed curves are obtained with resistors R_{ibcp} and R_{ibcn} (i=1,2,3) removed, which is indicated as scheme 2, and the dotted curves, which is indicated as scheme 1 are obtained with resistors R_{ibcp} and R_{ibcn} (i=1,2,3) directly tied to V_{dd} and in both cases the OTAs' input voltages vary substantially when the RTO clock changes state.

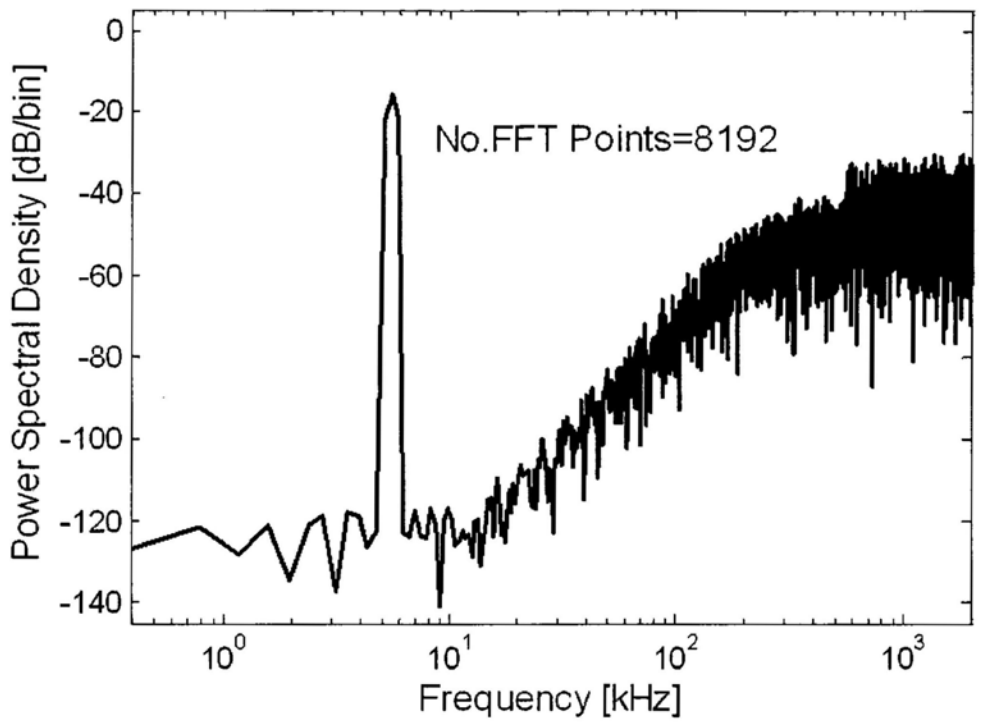


Fig 7.4 Simulated output spectrum for a $1V_{pp,diff}$ 5.47kHz input

Fig 7.4 shows the output spectrum of the modulator for a 5.47kHz 1V peak-to-peak differential input. No distinguishable harmonic is observed. The peak SNDR is 81dB over a 25kHz bandwidth with power consumption comparable to that of the modulator in [9].

Comparatively, the modulator is also simulated with scheme 1 and scheme2, which are discussed above. In simulation, the modulator achieves 74dB and 73dB with scheme 1 and scheme 2, respectively. With the proposed dynamic CM level shift technique, the improvement of the SNR performance is about 11% and 9%.

Low-voltage gate-input OTAs in active-RC CT modulators require a CM level shift between the OTA inputs and the integrator's inputs and outputs. This level shift results in CM variations for different clock phases when RTO feedback DACs are used. A dynamic CM shifting circuit has been presented in this chapter which maintains a constant CM level by dynamically changing the level shift resistors. The

functionality of the proposed circuit has been verified by transistor-level circuit simulations.

Chapter 8 Conclusions and recommendation for future work

In this thesis, a 0.5V 1-MHz signal bandwidth continuous-time complex ΔΣ modulator has been demonstrated in a 0.13μm CMOS technology without using low-threshold devices or internal voltage boosting. To the best of our knowledge, a 1-MHz-wide signal bandwidth ΔΣ modulator has been realized for the first time for a supply voltage below 0.8V. Low-voltage operation for the 64MHz sampling rate modulator has been enabled by special architectural level design and amplifiers. At architectural level, a special CM lifting up technique for the CT modulator, which adopts return-to-open feedback DACs, has been employed such that the amplifiers' input transistors can be biased in or near strong inversion to meet the speed requirements. At the circuit level, a gate-input, self-biased, high speed (in the context of low-voltage designs) amplifier has been developed. The modulator achieves a 62dB peak SNDR in a 1-MHz-wide signal bandwidth with 1.8mW consumption at a 0.45V supply, which corresponds to a FoM that is the highest among the reported true low-voltage delta sigma modulators. As several low-voltage RF front-ends have been demonstrated, this modulator can be further integrated with such a front-end to form a highly digital GFSK receiver.

Furthermore, to reduce the power consumption, a new fully differential amplifier with Miller-compensated DC CMFB loop is proposed. Simulation results with different process corner show its robustness. A third-order CT complex modulator incorporating the proposed amplifier achieves quite reliable performance with varying temperature and varying power supply. Last, a dynamic CM shift technique is proposed for low-speed low-voltage modulator that employs return-to-open feedback DAC. The technique can improve the modulator's SNR by 11% in transistor-level circuit simulations.

8.1. Future works

There are many interesting future works along the direction of this research. First, a 0.5V PLL could be investigated to feed better clock signals to the modulator to minimize the clock jitter. The clock generator in this work was implemented based on simple inverter and other logic gates. It is not easy to achieve accurate timing, e.g., 50% duty cycle and 20%Ts delay, in all process corners. Second, a better biasing strategy could be studied to make the low-voltage modulator's current consumption less sensitive to the supply voltage variation.

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Appendix

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