# Fixed-Frequency Multi-Mode Multiple-Output Arbitrary-Type DC-DC Switching-Mode Power Converters with Variable-Frequency Control

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A Thesis Submitted in Partial Fulfillment
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Abstract of thesis entitled:

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Submitted by **ZHENG, Yanqi**
for the degree of **Doctor of Philosophy**
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Switching-mode power converter (SMPC) is an important circuit block in electronic systems. In the modern SMPC system, constant frequency voltage or current-mode control technique is commonly used. However, some limitations are raised due to some preliminary settings in the design. In this thesis, the switching frequency or period is no longer a constant but a design variable. Then, an additional frequency-control loop (FCL) is introduced in order to obtain a fixed frequency operation in the steady state. Three individual designs implemented with different types of FCL are proposed to verify the concept.

Firstly, a pseudo-PWM hysteresis voltage-mode buck converter is proposed. It achieves fast transient speed by the hysteresis control, estimable switching spectrum with a locking frequency and fast mode switching between PWM and PFM depending on the loading change. Measurement results show that the recovery time under the load transient is around 5μs, which is 5 times of the switching period. The boundary of the recovery time is defined by the value of the off-chip inductor.

Then, a four-channel SIMO converter based on FCL is developed, together with auto-phase allocation technique. This circuit not only solves the problem of imbalance

loading of different channels, but it also keeps the idle period of the inductor sufficient short in the full operation region. By combining with all channel controllers, FCL makes fast load transient response without degrading the power efficiency. Moreover, linear auto converter-type adaption technique is also used, which makes the converter surviving from a wide input range and output range. Measurement results show that the proposed converter can achieve a peak efficiency of 89%, a total output power of 1.46W, a load transient response time of less than 70μs, and an idle inductor period of <10%.

Finally, a four-channel SIMO converter with direct combination but optimal switching sequence for arbitrary converter sequence and converter type is presented. The theoretical optimal 1st-order inductor waveform from this proposed control algorithm is introduced. FCL is involved in this design to realize the algorithm. Moreover, a current-modulated ramp signal, which couples to different controllers, is included to compensate the original deep correlated power stages. By using all of the proposed techniques, Measurement results show that both conduction loss and dynamic loss can be suppressed because of the optimized switching sequence. The load transient response time is around 100μs. The peak efficiency is 89% with a 2.5-V power supply. A maximum output power of 1.66W can be achieved.

# 摘要

开关式电源转换器（SMPC）是一种在电子系统的重要电路模块。在现代的 SMPC 系统，最常用的是固定频律下的电压或电流模式控制技术。然而，固定频率设置导致一些工作性能上的限制。在这篇论文中，开关频率或周期已经不再是一个常数，而是一个设计变量。然后，一个额外的频率控制环路（FCL）将会被引入，以取得稳定状态下系统以固定频率运行。三个不同的设计基于三种不同类型的 FCL 实现方法在将会在下面提出来验证这个设计的概念。

首先，一种虚拟的 PWM 电压模式降压转换器将会被提出来。它实现了快速瞬态响应速度，可预见的开关频谱以及在模式 PWM 和 PFM 根据负载变化而切换。测量结果表明，对负载瞬态响应恢复时间在 5 微秒左右，这是开关周期的 5 倍。这个时间主要是由外接电感的大小决定。

然后，4 通道多输出转换器整（SIMO）将会被提出来，加上自动相位分配技术。该电路不仅解决了不同通道负荷不平衡的问题，它也保持了足够的电感在各种工作状态下都保持短时间的闲置时期。通过与所有通道控制器的协同控制，在不减低效率的情况下实现快速负载瞬态响应。此外，线性的转换器自适应技术的使用，这使得该转换器由可以适用于宽输入范围和输出范围。测量结果表明，该转换器的效率

可以达到了 89%，总的输出功率为 1.46W，负载瞬态响应小于 70 微秒以及对<10%的电感闲置时间。

最后，一个直接的，优化组合的，任意切换转换器顺序的多输出转换器整（SIMO）将会被提出来。理论上最佳的一阶电感电流波形控制算法将会被介绍。FCL 将参与这个算法的实现。此外，电流斜坡信号调制，互相耦合的控制器，被用于对付深度耦合的功率输出级别。利用以上所有技术，测量结果表明，无论是静态传导损耗还是动态损耗，可由优化的开关顺序所抑制。负载瞬态响应时间约为 100 微秒。在 2.5V 输入电源下，峰值效率为 89%，最大输出功率可以达到 1.66W。

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# Table of Content

## Chapter 3 – A Fixed-Frequency Arbitrary Type Wide Loading Range SIQO DC-DC Converter with Efficient Switching Sequence



## Chapter 4 – Conclusion and Future Work

# List of Figures

# List of Tables

Table 4-1 Simulation setting. **4-3**

# Chapter 1

# Introduction

## 11 Single-Inductor Multiple -Output DC-DC Converter

Switching-mode dc-dc power converters (SMPC) have been widely used in many portable and non-portable electronic devices due to its high power-conversion efficiency and flexible range of output voltage (step-down, step-up and inverted). In the recent years, SMPC is adopted to the design of IC systems which need multiple supply voltages to achieve high performance and low power simultaneously. One example is the dynamic voltage scaling (DVS) technique for high-density digital systems [1]. This technique enables ultra-low power consumption in the standby (idle) mode while provides sufficient power to the digital IC system in the full-power mode. As a matter of fact, the multiple supplies for an IC system have different maximum output powers. It implies that different supplies have different regulated voltages and different maximum output currents. They work independently and are controlled by the power-management control unit based on the operation mode of the IC system.

In the past decade, there is a growing trend to develop single-inductor multiple-output (SIMO) dc-dc converter since only one inductor is needed and shared by multiple channels according to time-multiplexing scheme. The advantage of this approach is, obviously, that only one inductor is needed and so the cost is lower due to less component count. Moreover, the problem of electromagnetic interference (EMI) generated by the inductor is potentially less serious. The disadvantage of this approach is that the output power is limited since the inductor is needed to be completely isolated when used by each output channel of the SIMO dc-dc converter

individually. Thus, the normal operation mode is the discontinuous conduction mode (DCM) [2]. Although pseudo-DCM has been proposed [3], the cross-regulation effect among different channels is still a problem. This problem becomes serious when the output powers of the output channels are greatly unbalanced. Another problem of SIMO dc-dc converter is the conduction loss for a converter with a wide conversion ratio. A common converter type to meet a wide conversion ratio is non-inverting flyback dc-dc converter. In general, the average inductor current is high (to be explained in detail in Chapter 2) in non-inverting flyback dc-dc converter. In SIMO dc-dc converter, typically, the channel with the highest output current affects the average inductor current. As a result, the *IR* due to the on-resistance and routing resistance is serious when the average inductor current is high. This implies the efficiency of a SIMO dc-dc converter is greatly affected.

## 1.2 Single-Inductor Multiple-Output DC-DC Converter with Variable Frequency Control

Before stepping into the major topic of this thesis, it is inspirational to review a single-output buck converter design. In the conventional single-output dc-dc converter design, PWM control is a popular controller design method. Compared with other control methods, it has advantages such as small output ripple voltage, predictable frequency tones and easy implementation. However, due to the intrinsic sampling system property, its dynamic response such as the load and line transient response will be worse than other control methods such as hysteretic voltage control and sliding-mode control.

In order to achieve the advantages of the afore-mentioned control algorithms, a design based on hysteretic voltage control with fixed switching frequency was

reported in [4]. Similar to this idea, a load-dependent pseudo-PWM buck converter with multiple operation modes is designed and fabricated it in AMS CMOS 0.35-μm 2P4M process. From the circuit diagram shown in Fig. 1-1, it is found that under heavy and moderate load, the buck converter operates in the pseudo-PWM (either CCM or DCM) mode, which using dual feedback loop with one based on a phase-locked loop (PLL) as shown in Fig. 1-2 to control the voltage regulation and the switching frequency. The converter will operate at PFM under light load and standby (STB) mode under ultra light load. Together with a segmented power-stage technique, degradation of efficiency in the light-load condition will be attenuated. Moreover, an on-chip active filter together with variable gain charge pump is designed for the frequency feedback loop, which occupies chip area of 600μm × 260μm. The micrograph of the converter is shown in Fig. 1-3.

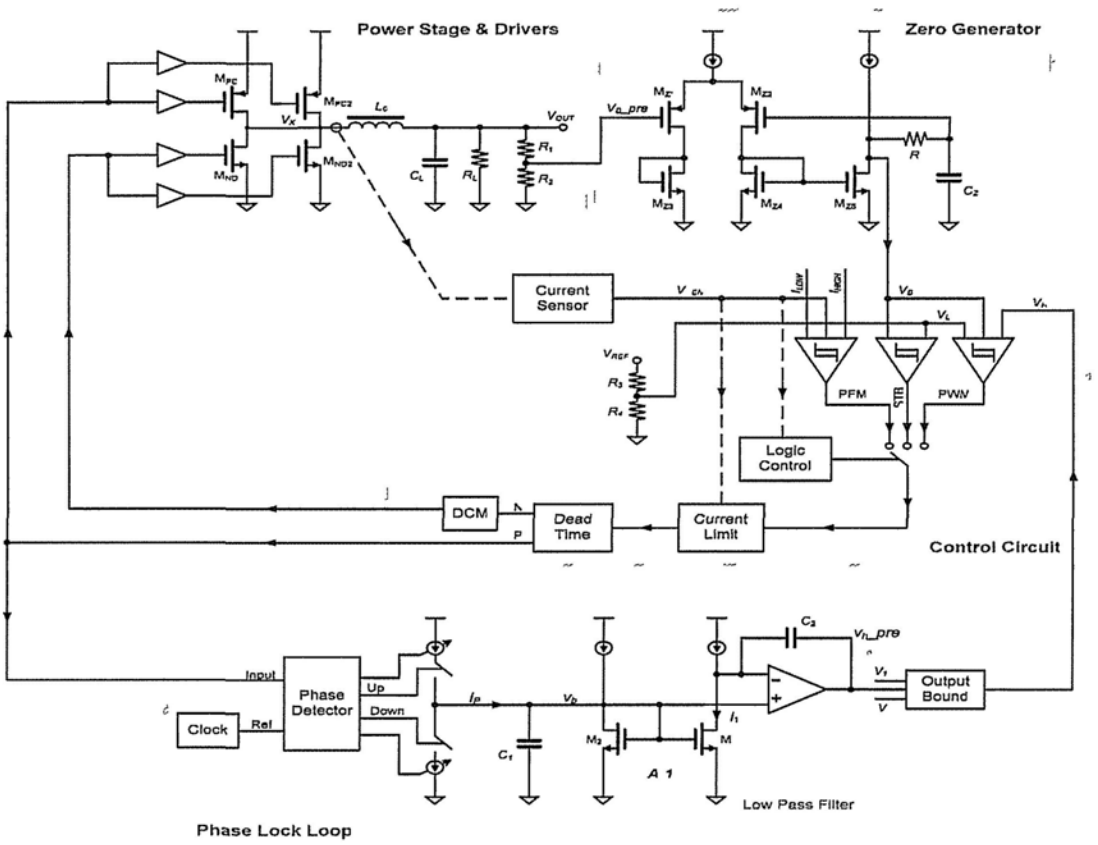


Fig. 1-1 Pseudo-PWM buck converter with load-dependent multiple-operation mode.

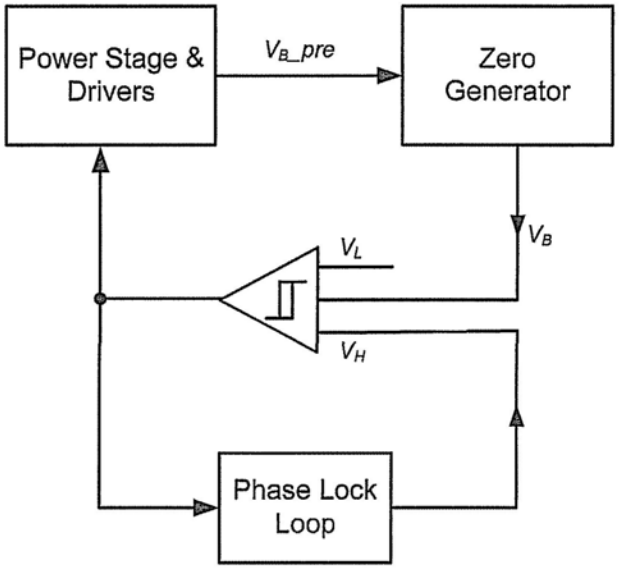


Fig. 1-2 Comparator-based voltage feedback loop and frequency locked loop.

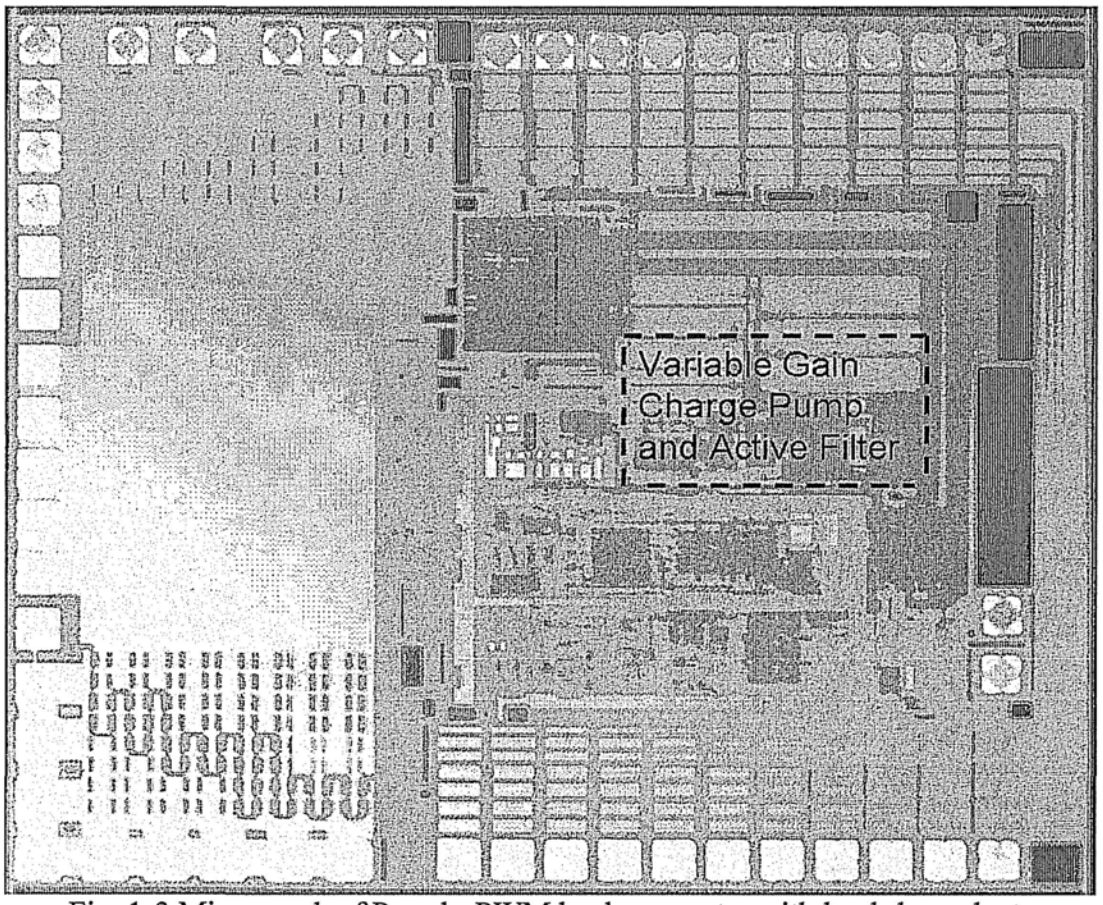


Fig. 1-3 Micrograph of Pseudo-PWM buck converter with load-dependent multiple-operation mode.

The measurement setting is shown in Table 1-1. From the measurement results shown in Figs. 1-4(a) and 1-4(b), it is found that the switching frequency is locked to the reference clock of 1MHz without any pre-setting and independent of the output

current. From the measurement results shown in Figs. 1-5(a) and (b), it is found that the settling time of load transient response of a 200-mA load-current step is around 5μs, which is faster than a conventional buck converter with a PWM controller operating at 1MHz.

Table 1-1 Measurement setting.

| | |
|---|---|
| Output voltages | 1.8V |
| Input voltage (nominal) | 3.3V |
| Inductor and its ESR | 4.7μH and 25mΩ |
| Capacitor and its ESR for each channel | 4.7μF and 50mΩ |
| Operation frequency | 1MHz |

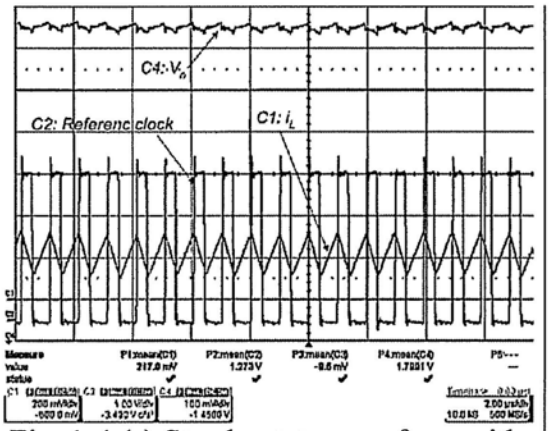


Fig. 1-4 (a) Steady-state waveform with load current of 200-mA.

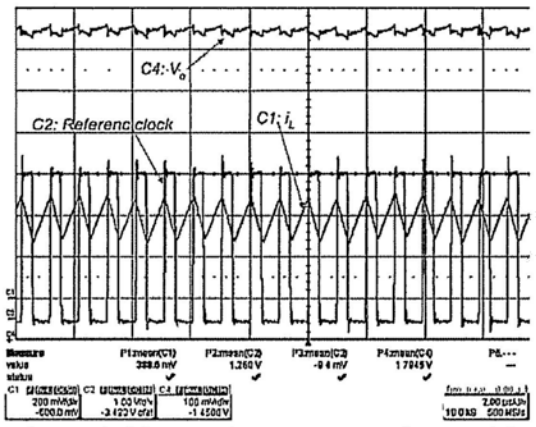


Fig. 1-4 (b) Steady-state waveform with load current of 380mA.

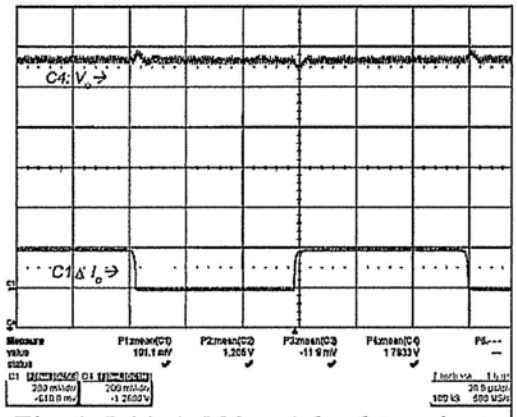


Fig. 1-5 (a) A 200-mA load transient response.(150mA → 350mA)

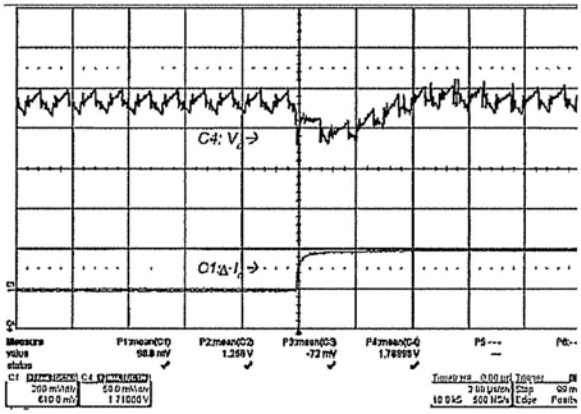


Fig. 1-5 (b) A 200-mA load transient response (zoom-in of Fig. 3-5(a)).

According to the design shown above, it is found that it is possible to make the switching frequency as a variable and then control it to a targeted value by an additional control loop. This concept is quite helpful to the SIMO converter design. It is known that the sub-converters of a SIMO share the same switching period. As a result, the variation of duty cycle which is used to respond for the disturbance by one or more than one channel will affect other channels seriously. By involving the variable frequency technique to the SIMO converter design, it is possible to attenuate this effect by distributing the sub-periods for sub-converter to a larger period temporarily and then fix the switching period back to the desired frequency after completed some controls. This idea will be introduced in detail later in this thesis. As a final remark, the required circuit and additional component to achieve the variable frequency control is small, and so the chip area of the frequency compensator is suitable for integration into the same chip.

## 1.3 Research Goal and Thesis Outline

The research goal of this thesis is to design high-efficiency SIMO dc-dc converters with fixed switching frequency. The works presented in this thesis will be focused on reducing the average inductor current, reducing channel cross-regulation effect, providing arbitrary type of the sub-converters (i.e. no pre-defined converter type is needed) and achieving optimized sub-period allocation scheme for each sub-channel under largely unbalanced situation.

There are totally two designs presented in this thesis. In Chapter 2, a fixed-frequency single-inductor quadruple-output (SIQO) auto buck-boost dc-dc converter with wide input and loading ranges based on the Class-1 (i.e. time multiplexing sub-channel opeartion) inductor waveform [2] will be presented. Then,

in Chapter 3, a fixed-frequency arbitrary-type SIQO dc-dc converter with efficient switching sequence and wide loading range will be introduced. This design is based on the Class-2 (i.e. direct combined sub-channel operation) inductor waveform [2]. Both designs will be addressed in accompany with theory, simulations and experimental results. The contribution of this thesis is to provide two design structures of SIMO dc-dc converters to solve the general problems such as low efficiency, fixed converter type and non-constant switching frequency happened in the SIMO dc-dc converter design.

# References


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[3] D. Ma, W. H. Ki, and C. Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007-1014, Jun. 2003.

[4] C.-H. Tso and J.-C. Wu, "A ripple control buck regulator with fixed output frequency," *IEEE Power Electronics Letters*, vol. 1, no. 3, pp. 61-63, Sep. 2003.

# Chapter 2

# A Fixed-Frequency SIQO Auto Buck-Boost DC-DC Converter with Wide Input and Loading Ranges

## Introduction

Nowadays, single-inductor multiple-output (SIMO) dc-dc converter such as TPS65120 [1] is a potential solution for some applications requiring multiple supplies whereas the supply voltages and the output power of each supply are largely different. In fact, a SIMO dc-dc converter has to handle a wide loading range with unbalanced loadings among different channels. Moreover, high power-conversion efficiency is one of the important performance requirements. In the past decade, some works were reported to solve these problems and to improve the performance of a SIMO dc-dc converter. For example, to tackle limited output power in the DCM operation, the pseudo-DCM (P-DCM) operation was proposed [2]. Both the constant offset inductor current and the fixed sub-period for each output channel cause serious limitations to the input and loading range of the SIMO dc-dc converter. As shown from the inductor current ($i_L$) in Fig. 2-1, the maximum output power able to be delivered by one of the channels is determined by an offset inductor current ($I_{offset1}$) and the value of the external inductor. However, the light-loaded output channels have a long idle time since the offset inductor current is unnecessarily high for them. Large conduction loss occurs across the lumped resistance (the ESR of the inductor, the on-resistance of the power MOSFET and the routing resistance) connected to inductor. Thus, the power-conversion efficiency is seriously degraded.

The motivation of the work presented in this chapter is to overcome the limitations in SIMO dc-dc converter design such as a wide input-voltage range, a high output-current range, unbalanced output power by each channel, large conduction power loss and non-constant switching frequency. The proposed SIMO dc-dc converter is applicable to general applications.

For the design proposed in this chapter, it is a SIMO dc-dc converter with Class-1 inductor-current waveform [3]. The goal is to make the inductor-current waveform act as the idea presented in Fig. 2-2. The sub-period of each channel is not an equally divided timing constant. Instead, the sub-period of each channel can be varied according to the required output power of the channel. This approach can reduce the offset inductor current so that the conduction loss of the proposed dc-dc converter is lower than that of the P-DCM counterparts. To realize the proposed approach, a control scheme by combining a phase-locked loop (PLL) to the current-mode controller is used. In addition, an auto buck-boost technique is also proposed to provide a wide input range to the proposed SIMO dc-dc converter. It will be demonstrated by a single-inductor quadruple-output (SIQO) dc-dc converter. The rule of thumb of this SIQO dc-dc converter design is to make each output channel behave as a single output channel buck-boost dc-dc converter. The details of the proposed design will be presented in the following sections in this chapter.

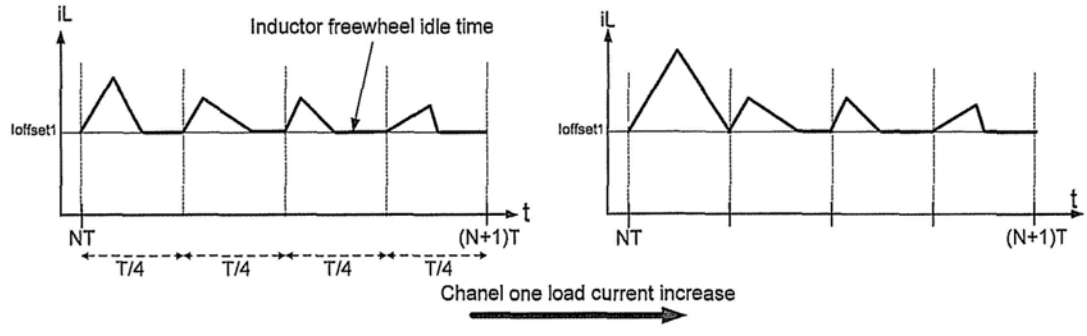



Fig. 2-1 Inductor-current waveform of a P-DCM SIQO dc-dc converter.

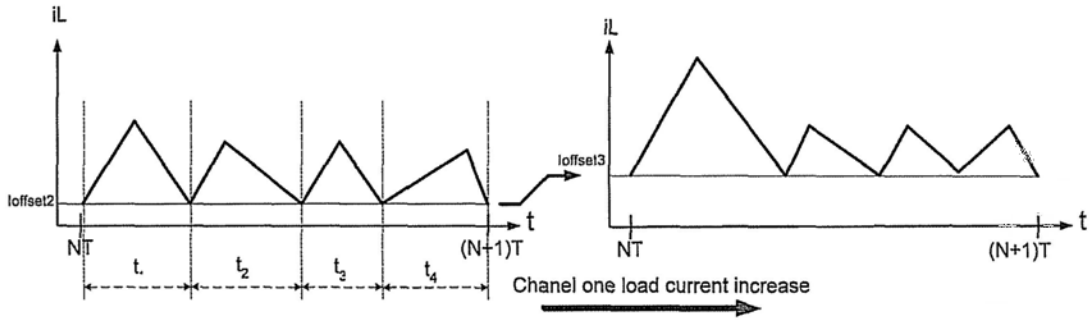



Fig. 2-2 Inductor-current waveform of the proposed SIQO dc-dc converter.

## 2.1 Proposed Auto Buck-Boost Power Stage

Conventionally, non-inverting flyback topology is an inherent auto buck-boost topology which covers voltage conversion ratio from less than one (for stepping down) to larger than one (for stepping up). This topology can solve the problem of the limited cycle oscillation in a generic buck converter and a generic boost converter when the duty cycle ($D$) is close to one. The inductor-current flow of a single-channel non-inverting flyback power converter is shown in Fig. 2-3. The operation is divided into two phases: charging and discharging the inductor ($L_0$). When only the switches SW_PI and SW_NO are closed, $L_0$ is energized by the voltage source ($V_g$). In the second phase, since only SW_NI and SW_PO are closed, the energy stored in $L_0$ is delivered to the load. The drawback of this operation is that the output current is delivered to the load only during the second phase in a switching period. As a result, the inductor current is higher than that of a buck and a boost converter. The average inductor current of a dc-dc buck converter is given by

$$avg[i_L] = I_o \tag{2-1}$$

and the average inductor current of a non-inverting flyback dc-dc converter is

$$avg[i_L] = I_o \times (V_g + V_o)/V_g \tag{2-2}$$

From (2-2), it shows that the average inductor current is kept increasing when $V_o$ approach to $V_g$. In fact, there are some power-saving buck-boost converters such as LTC3440 and TPS63000 [4], [5]. In these typical designs, prior frequency information is needed to make the switching frequency fixed. However, this approach is not suitable to translate into the proposed SIQO dc-dc converter with adaptive sub-period since it will make the design very complicated and introduce a lot of constraints into the design as well.

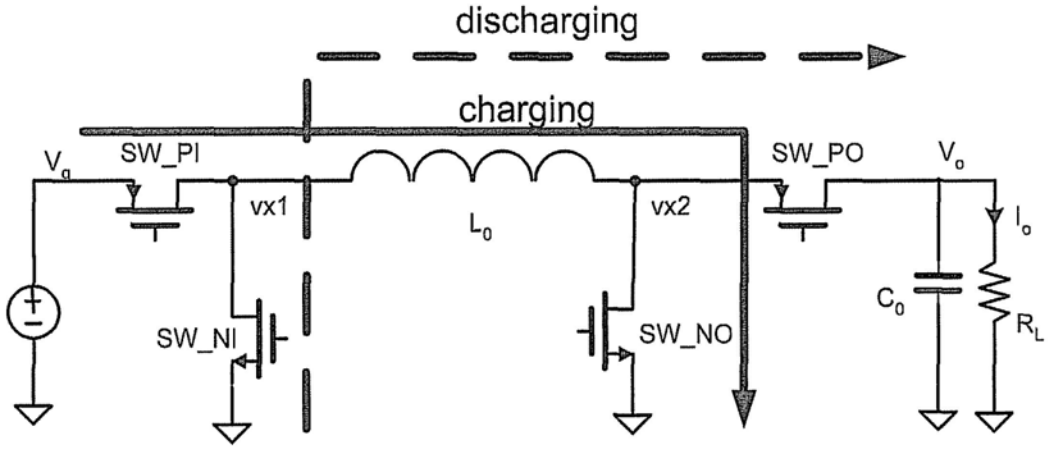



Fig. 2-3 Inductor-current flow of non-inverting flyback dc-dc converter.

### 2.1.1 Inductor-current flows

Before introducing the proposed auto buck-boost power stage with its inductor-current flow, the possible inductor current flows are investigated below. They will be used to complete the inductor-current waveform shaping to achieve the proposed dc-dc converter.

1. Charging the inductor (denoted as "SW_C")

   As shown in Fig. 2-4, when only SW_PI and SW_NO are closed, the inductor is connected in parallel with $V_g$. The inductor current is increasing with slope of $V_g/L_0$. It is noted that $T_{SW\_C}$ denotes the duration of the SW_C operation.

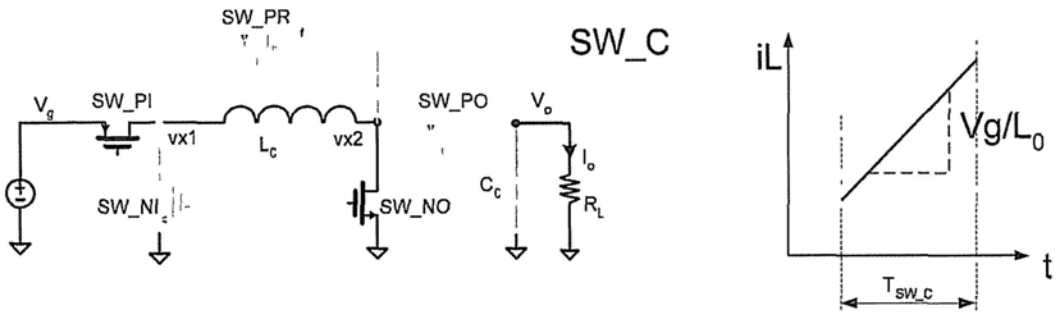



Fig. 2-4 SW_C: Charging the inductor.

2. Delivery charges to the output (denoted as "SW_D")

   Fig. 2-5 shows when only SW_NI and SW_PO are closed, the energy stored in $L_0$ will be transferred to the output. The inductor current will decreases with slope of $-V_o/L_0$. It is noted that $T_{SW\_D}$ denotes the duration of the SW_D operation.

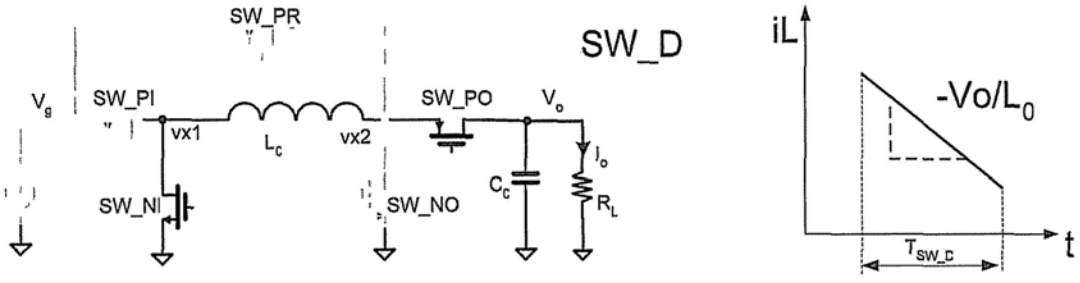



Fig. 2-5 SW_D: Delivery charges to the output.

3. Direct path from the supply to the output (denoted as "SW_B").

   In Fig. 2-6, a direct path to connect $V_g$ to $V_o$ is formed when only SW_PI and SW_PO are closed. Energy from the supply transfers to the output through the inductor. Depending on the voltage conversion ratio between $V_o$ and $V_g$, the inductor current may increase or decrease. When $V_g > V_o$, the inductor current increase. Similarly, when $V_g < V_o$, the inductor current decreases. For both cases, the slope of the inductor-time waveform is $(V_g - V_o)/L_0$. It is positive when $V_g > V_o$ and is negative when $V_g < V_o$. $T_{SW\_B}$ denotes the duration of the SW_B operation.

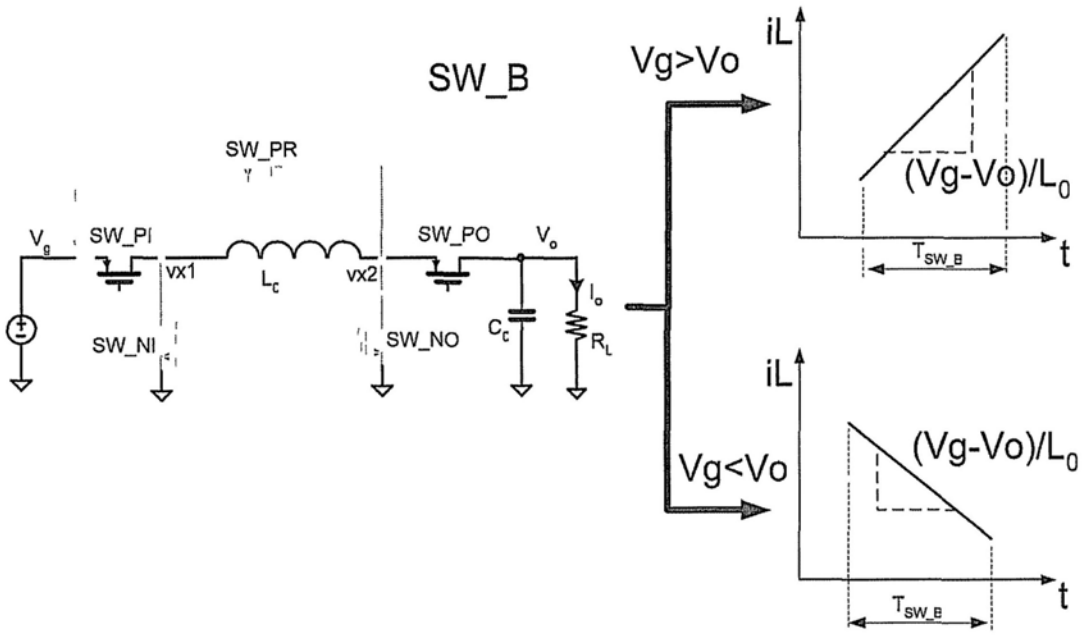



Fig. 2-6 SW_B: Direct path from the supply to the output.

4. Holding the inductor current (denoted as "SW_H")

   When only SW_NI and SW_NO are closed, as illustrated in Fig. 2-7, the terminals of $L_0$ are shorted. The inductor current will flow through itself and remains a constant. It is noted that $T_{SW\_H}$ denotes the duration of the SW_H operation.

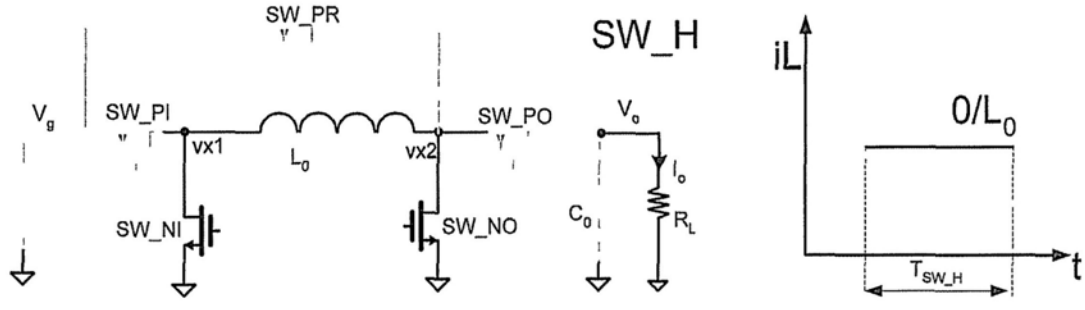



Fig. 2-7 SW_H: Holding the inductor current.

5. Reserve flow of the inductor current (denoted as "SW_R")

   Finally, Fig. 2-9 shows the case when only SW_NI and SW_PR are closed, the energy stored in the inductor is transferred back to the source. The inductor

current decreases with slope of $-V_g/L_0$. t is noted that $T_{SW\_R}$ denotes the duration of the SW_R operation.

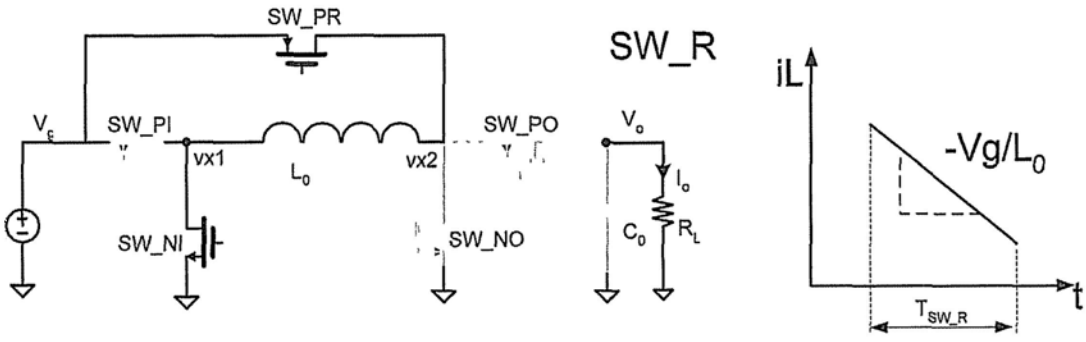



Fig. 2.8 SW_R: Reserve flow of the inductor current.

### 2.1.2 Proposed inductor-current flow scheme

In order to reduce the average inductor current for decreasing the conduction loss, the inductor current is designed to flow in three possible paths within one switching period. Fig. 2-9 shows the inductor current flows: charging, direct and discharging path. As it is well-understood that the best way to provide energy to the load is to make it by the voltage supply directly, the proposed approach is to maximize the directly path within a switching period.

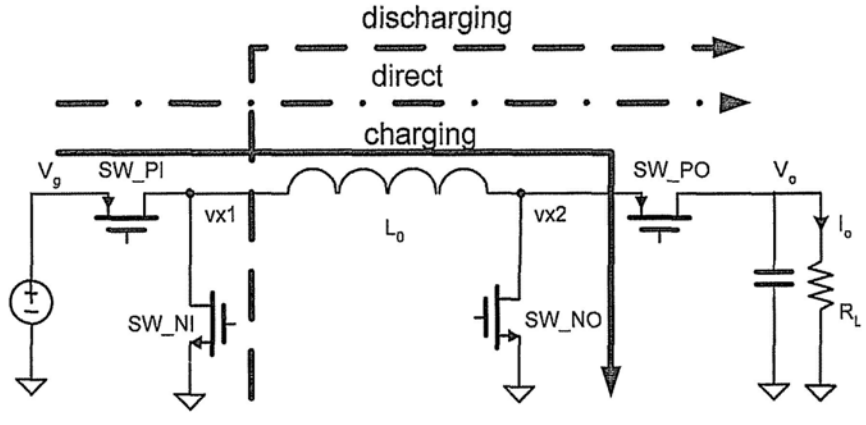



Fig. 2-9 Proposed inductor-current flows.

Fig. 2-10 shows the three possible inductor-current waveforms of the proposed auto buck-boost dc-dc converter. They are

1. Operation approaching to a buck converter (i.e. $V_o/V_g < 1$) or a deep buck converter (i.e. $V_o/V_g << 1$)
2. Operation approaching to a boost converter (i.e. $V_o/V_g > 1$)
3. Operation approaching to a deep boost converter (i.e. $V_o/V_g >> 1$)

The switching sequence for Case 1 and 2 is SWC, SW_B, SW_D and SW_H. For Case 3, it is SWC, SW_B and SW_H. It is noted the period SW_H is for locking the switching frequency using a PLL. The details will be presented later in this chapter.

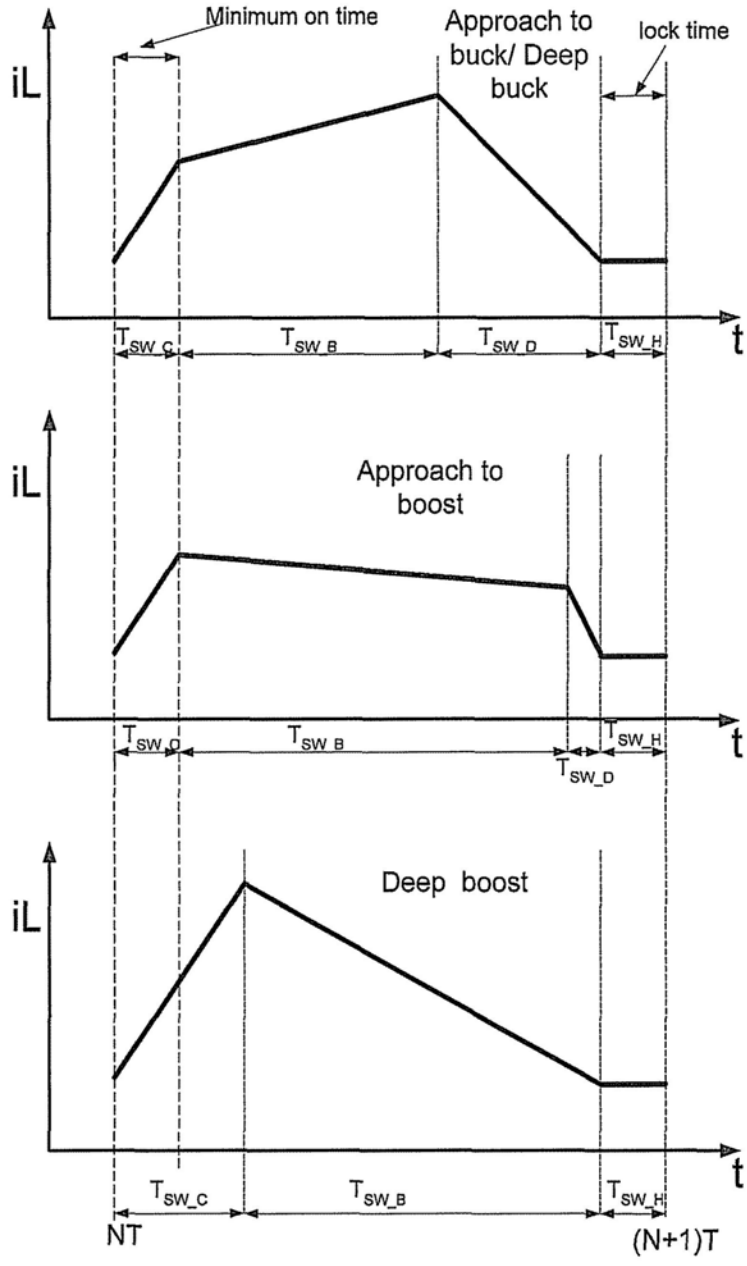



Fig. 2-10 Inductor-current waveform of proposed auto buck-boost dc-dc converter.

The average inductor current of the proposed auto buck-boost dc-dc converter for Case 1 and 2 is given by

$$avg[i_L]=\frac{1}{T_s}\left[\frac{V_g\cdot T_{MOT}^{\ 2}}{2L_0}+\frac{V_g^2\cdot T_{MOT}^{\ 2}}{2V_o\cdot L_0}+\frac{V_g\cdot T_{MOT}}{L_0}\left(T_s-T_{MOT}-T_{LCK}-\frac{V_g}{V_o}T_{MOT}\right)+\frac{V_g-V_o}{2L_0}\cdot\frac{V_o}{V_g}\left(T_s-T_{MOT}-T_{LCK}-\frac{V_g}{V_o}T_{MOT}\right)^2\right]$$
$$\frac{\frac{V_g^2\cdot T_{MOT}^{\ 2}}{2V_o\cdot L_0}+\frac{V_g\cdot T_{MOT}}{L_0}\left(T_s-T_{MOT}-T_{LCK}-\frac{V_g}{V_o}T_{MOT}\right)+\frac{V_g-V_o}{2L_0}\cdot\frac{V_o}{V_g}\left(T_s-T_{MOT}-T_{LCK}-\frac{V_g}{V_o}T_{MOT}\right)^2}{T_s-T_{MOT}-T_{LCK}}$$
$$+I_o\frac{T_s}{T_s-T_{MOT}-T_{LCK}} \tag{2-3}$$

The average inductor current shown in (2-3) is a bit complicated. A more intuitive result can be obtained if the inductor ripple is ignorable which means that $L_0$ is sufficiently large.

$$\begin{aligned} &V_g\left(D_1+D_2\right)=V_o\left(D_2+D_3\right)\\ &D_1+D_2+D_3+D_4=1\\ &avg[iL]=\frac{I_o}{D_2+D_3} \end{aligned} \tag{2-4}$$

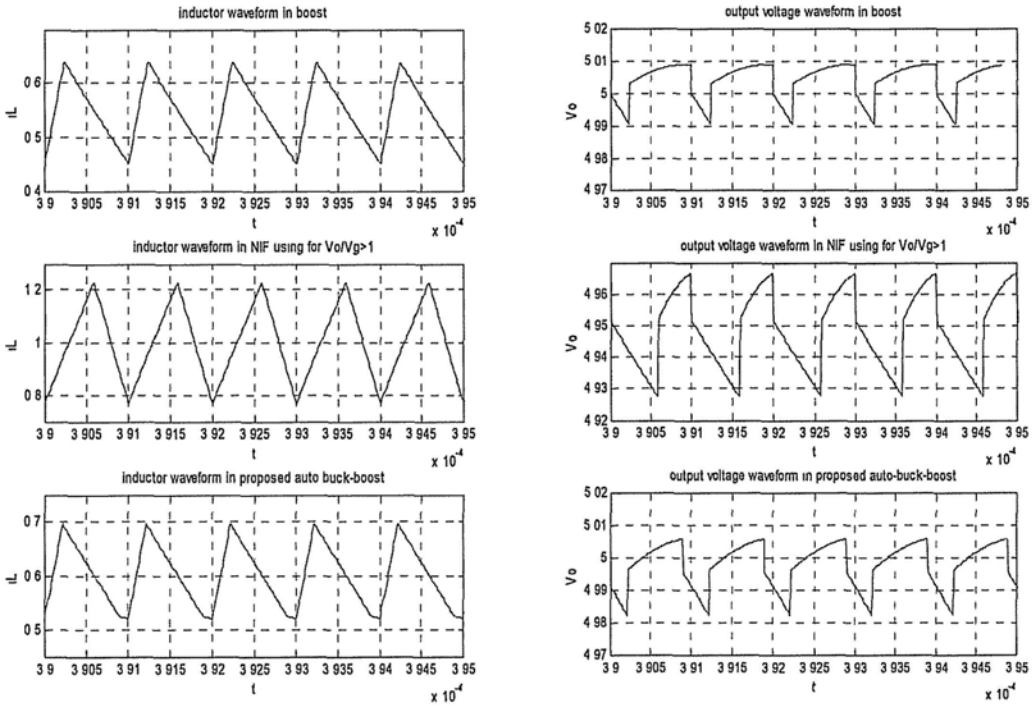
where $D_1$, $D_2$, $D_3$ and $D_4$ is the duty cycle for SW_C, SW_B, SW_D and SW_H individually, and

$$D_2+D_3=\frac{V_g\left(1-D_3-D_4\right)}{V_o} \tag{2-5}$$

As a result, from (2-4), it can be found that a larger ($D_2$ + $D_3$) results in a lower average inductor current. By observing (2-5) and provided that $D_4$ = 0, it can be found that $D_3$ = 0 is the solution for $V_g < V_o$, while $D_2 + D_3 = 1$ is the solution for $V_g > V_o$. They are exactly the conditions for the boost converter and buck converter individually.

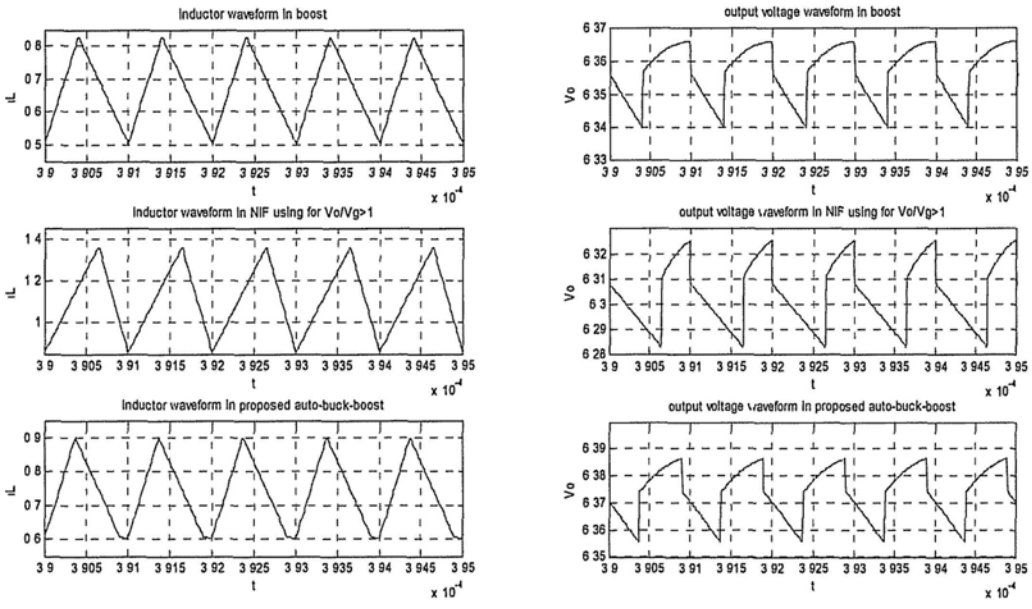
Finally, in order to prove the reduced average inductor by the proposed scheme, some simulations are performed.

Simulation 1: Boost vs. Non-inverting flyback vs. Proposed for $V_o/V_g > 1$




(a) (b)

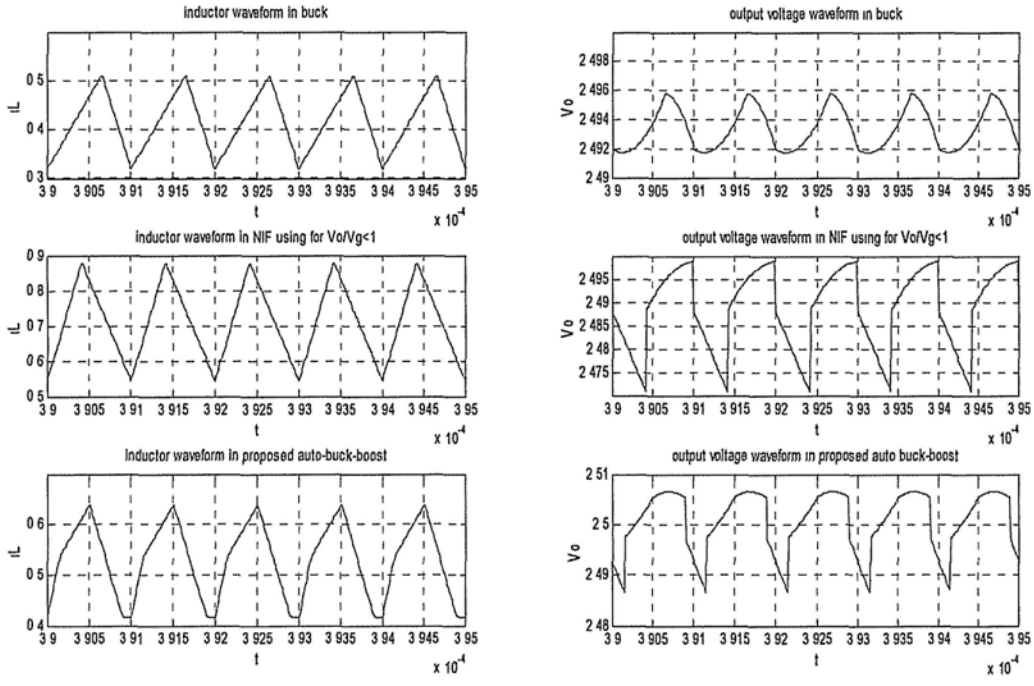
Fig. 2-11 Simulation $V_g = 4\text{V}$, $V_o = 5\text{V}$, $I_o = 416\text{mA}$.




(a) (b)

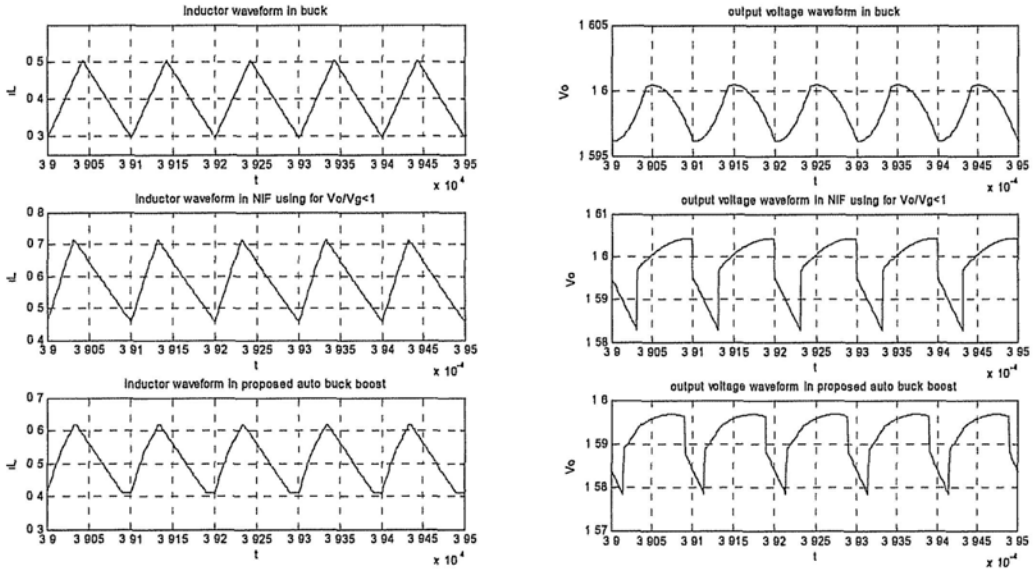
Fig. 2-12 Simulation $V_g = 4\text{V}$, $V_o = 6.4\text{V}$, $I_o = 400\text{mA}$.

Simulation 2: Buck vs. Non-inverting flyback vs. Proposed for $V_o/V_g < 1$




(a) (b)

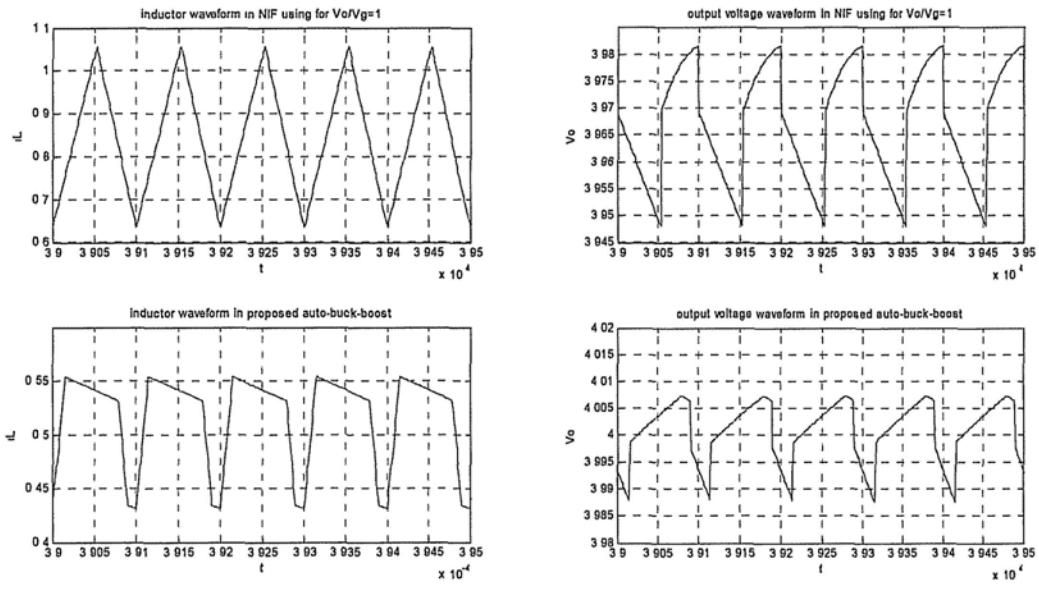
Fig. 2-13 Simulation $V_g = 4\text{V}$, $V_o = 2.5\text{V}$, $I_o = 416\text{mA}$.




(a) (b)

Fig. 2-14 Simulation $V_g = 4\text{V}$, $V_o = 1.6\text{V}$, $I_o = 400\text{mA}$.

Simulation 3: Non-inverting flyback vs. Proposed for $V_o/V_g = 1$




(a) (b)

Fig. 2-15 Simulation $V_g = 4\text{V}$, $V_o = 4\text{V}$, $I_o = 400\text{mA}$.

The numerical results of the simulations shown in Figs. 2-11 to 2-15 are summarized below. It is noted that NIF = non-inverting flyback, $T_s$ = switching period, $T_{\text{MOT}}$ = minimum on-time, $T_{\text{LCK}}$ = locking time and $I_{LA}$ = average inductor current

Table 2-1 Simulation $V_g = 4\text{V}$, $V_o = 5\text{V}$, $I_o = 416\text{mA}$.

| | $V_g$ (V) | $V_o$ (V) | $L$ (H) | $\text{ESR}_\text{L}$ (Ω) | $C$ (F) | $\text{ESR}_\text{C}$ (Ω | $I_o$ (A) | $T_s$ (s) | $T_{\text{MOT}}$ (s) | $T_{\text{LCK}}$ (s) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Boost** | 4 | 5 | 4.7μ | 0.3 | 10μ | 0.02 | 416m | 1μ | – | – | 0.54 |
| **NIF** | | | | | | | | | – | – | 1 |
| **Proposed** | | | | | | | | | 100n | 100n | 0.6 |

Table 2-2 Simulation $V_g = 4\text{V}$, $V_o = 6.4\text{V}$, $I_o = 400\text{mA}$.

| | $V_g$ (V) | $V_o$ (V) | $L$ (H) | $\text{ESR}_\text{L}$ (Ω) | $C$ (F) | $\text{ESR}_\text{C}$ (Ω | $I_o$ (A) | $T_s$ (s) | $T_{\text{MOT}}$ (s) | $T_{\text{LCK}}$ (s) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Boost** | 4 | 6.4 | 4.7μ | 0.3 | 10μ | 0.02 | 400m | 1μ | – | – | 0.67 |
| **NIF** | | | | | | | | | – | – | 1.11 |
| **Proposed** | | | | | | | | | 100n | 100n | 0.74 |

Table 2-3 Simulation $V_g = 4V$, $V_o = 2.5V$, $I_o = 416mA$.

| | $V_g$ (V) | $V_o$ (V) | $L$ (H) | $ESR_L$ (Ω) | $C$ (F) | $ESR_C$ (Ω | $I_o$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Buck** | 4 | 2.5 | 4.7μ | 0.3 | 10μ | 0.02 | 416m | 1μ | – | – | 0.42 |
| **NIF** | | | | | | | | | – | – | 0.71 |
| **Proposed** | | | | | | | | | 100n | 100n | 0.53 |

Table 2-4 Simulation $V_g = 4V$, $V_o = 1.6V$, $I_o = 400mA$.

| | $V_g$ (V) | $V_o$ (V) | $L$ (H) | $ESR_L$ (Ω) | $C$ (F) | $ESR_C$ (Ω | $I_o$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Buck** | 4 | 1.6 | 4.7μ | 0.3 | 10μ | 0.02 | 400m | 1μ | – | – | 0.4 |
| **NIF** | | | | | | | | | – | – | 0.51 |
| **Proposed** | | | | | | | | | 100n | 100n | 0.59 |

Table 2-5 Simulation $V_g = 4V$, $V_o = 4V$, $I_o = 400mA$.

| | $V_g$ (V) | $V_o$ (V) | $L$ (H) | $ESR_L$ (Ω) | $C$ (F) | $ESR_C$ (Ω | $I_o$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **NIF** | 4 | 4 | 4.7μ | 0.3 | 10μ | 0.02 | 400m | 1μ | – | – | 0.84 |
| **Proposed** | | | | | | | | | 100n | 100n | 0.52 |

From the simulations, it is found that not only the average inductor current is lowered when using the proposed auto-buck-boost technique, but the output voltage ripple will also be smaller. Normally, the ripple voltage is dominated by the ESR value of the output capacitor provided that $L_0$ or $C_0$ is sufficiently high to suppress the ripple voltage. As a result, the lowered average inductor current indirectly implies the smaller output ripple. Moreover, for the buck converter or buck-boost converter, SW_PO will not be always turned on. It will introduce a large voltage spike when it is switching. The magnitude of the spike depends on the current transient speed and its magnitude. It is obvious that low average inductor current will give large benefit on this. Finally, the average inductor current of the buck, boost, non-inverting flyback and the proposed scheme are shown in Fig. 2-16. It is found that the

proposed scheme provides a much lower average inductor current at different $V_o$. Although the average inductor current of the proposed scheme is not the lowest, it can cover a wide range of voltage conversion ratio. Thus, the proposed scheme is much better than the non-inverting flyback counterparts.

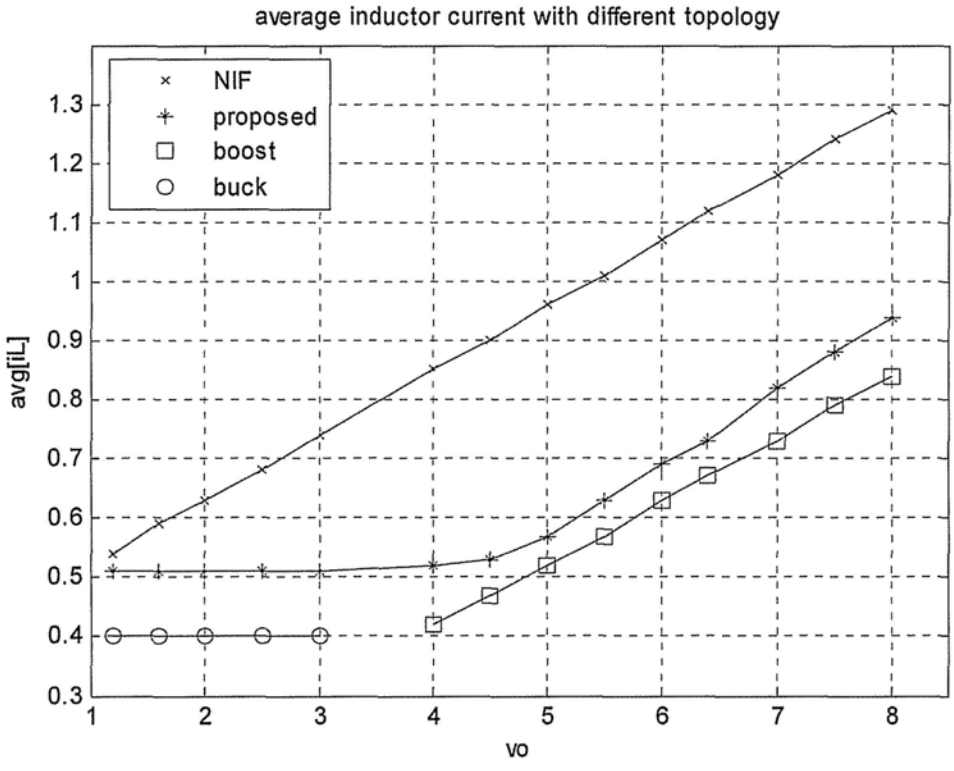



Fig. 2-16 A comparison of the average inductor current of all investigated schemes (noted that $V_g = 4$V).

### 2.1.3 Reverse inductor discharge control

When the output current of a SIMO dc-dc converter is ultra low, the inductor current cannot return to the pre-defined offset level. A general solution is use PFM or pulse-skipping technique in single-output dc-dc converter design. This approach implies that the switching frequency is no longer fixed. Although the pulse-skipping is also available for the SIMO power converter for the sub-channel with ultra light load, it does not work when strictly fixed frequency operation is required. Since the pulse-skipping scheme used in SIMO dc-dc converter design cannot achieve perfect

hold switching period, sub-harmonic oscillation will happen. Another typical solution applied in single output dc-dc converter is let the inductor reverse charging although power loss will be significant in the CCM operation. As a matter of fact, this approach is usually an option in many commercial products [6].

One design using an additional dummy on-chip output inductor to create a discharge path was reported in [7]. This approach can achieve an exact PWM operation. However, more external device is needed and the power-conversion efficiency will suffer more due to the resistance associated with the discharge path achieved by the on-chip inductor.

In this chapter, a reverse inductor-current discharge period for ultra-light load sub-channel is proposed. The operation principle is showed in Fig. 2-17. It is known that when using the Auto buck-boost controller, the minimum output current is defined by the triangle size under the inductor-current waveform in the time domain. In order to further reduce this limit, the SW_D period is reduced and the SW_R period is added to discharge inductor current to $I_{offset}$. The drawback of this control technique is slight efficiency degradation. Since the charging and discharging cycles occupy non-zero period, this will affect the conduction loss due to the idle inductor-current period (i.e. the SW_H period). The weighting of this power loss is quite related to the selection of the minimum on-time and the switching frequency. As a result, trade-offs should be made carefully between noise immunity, switching frequency and power-conversion efficiency.

For the selection of the minimum on-time in the SW_C period, normally, it mainly depends on the duration where data (duty cycle) is valid to be sampled in PWM-based dc-dc converter. Since the switching mechanism gives large switching noise to the control circuits such as the comparator in the analog controller and the

ADC in the digital controller, sampling during switching is very unstable. In general, if the inductor current has larger magnitude and switches faster, the minimum on-time should be longer. For a current-mode based PWM control dc-dc converter, the current sensor also requires a non-zero settling time. Moreover, in the proposed design, the duty-control signal should be sampled earlier. Based on all these considerations, the chosen minimum on-time is around 100ns.

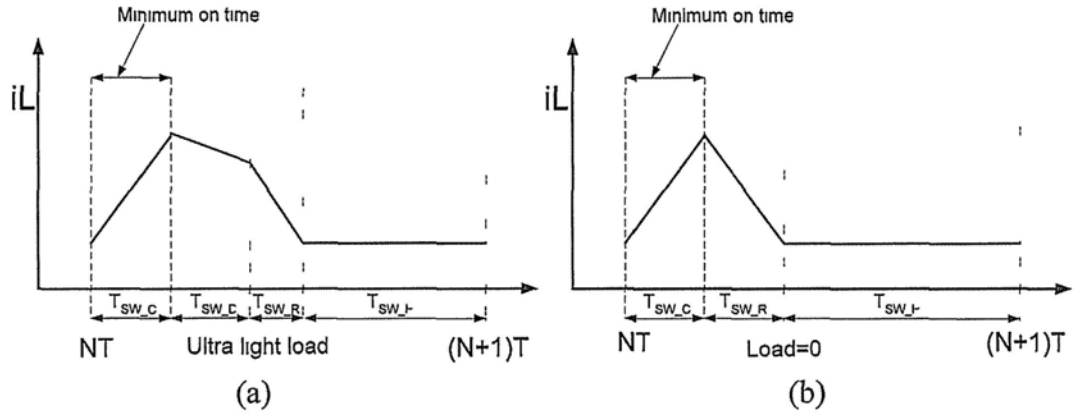



Fig. 2-17 Inductor current with proposed reverse inductor-current discharge scheme (a) for light-load condition (b) for no load condition.

## 2.2 Power Stage of the SIQO DC-DC Converter

The power stage of the SIQO dc-dc converter is shown in Fig. 2-18. Although the design goal is to make each channel to be auto buck-boost sub-converter, in order to simplify the design, only the sub-converter 3 is designed to be an auto-buck-boost converter for demonstrating the proposed concept. In this design, the first sub-converter has an output voltage ($V_{o1}$) which is, by default, the highest output voltage. Therefore, the substrate connections of all power PMOSFET on the output side are connected to $V_{o1}$. A substrate selection technique can be adopted if this assumption is not preferred [8].

In typical SIMO converter, the output stages of each sub-converter are connected to a common node $V_{X2}$ (one of the inductor terminal) through power

switch. This switch can be implemented by either an NMOSFET [9] or a PMOSFET [2]. For realizing a boosted output voltage, a gate-drive boosting circuit is needed when using NMOSFET. In this design, a PMOSFET used as the output switch with a level shifter to realize the boosted gate drive signal is used.

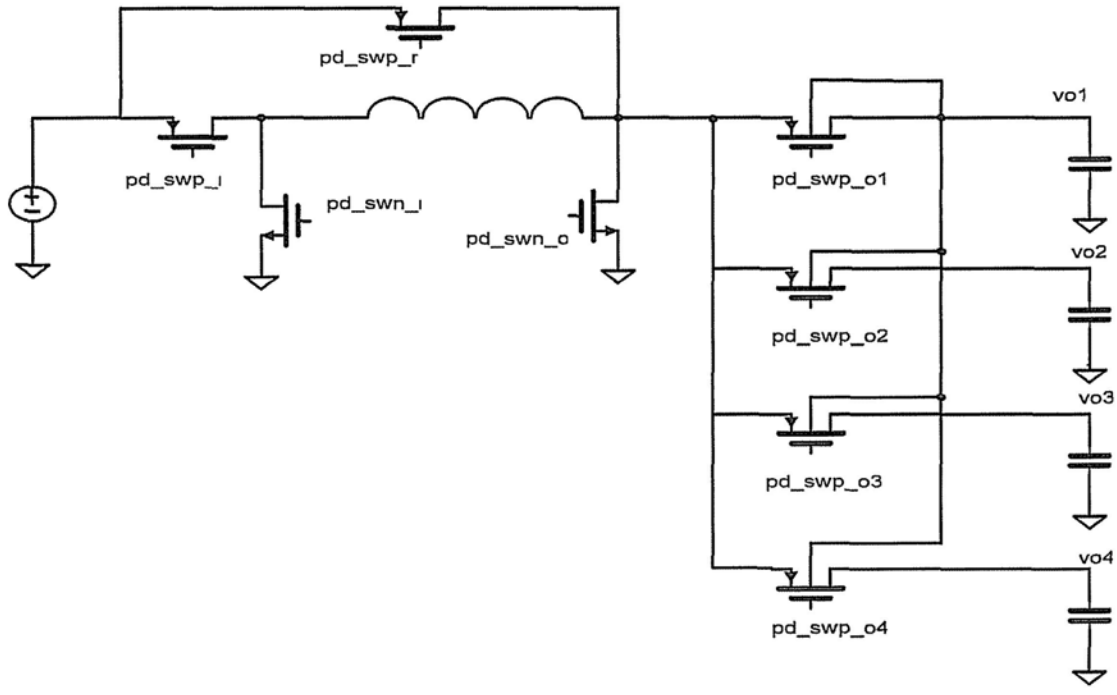



Fig. 2-18 Power stage of the SIQO dc-dc converter.

However, different from a single output converter, the switching at $V_{X2}$ will cause large voltage spikes in SIMO dc-dc converter design. The origin of this large voltage spike is due to the voltage difference between $V_{X2}$ and the output voltage of each sub-converter. For example, when $V_{o1}$ = 3.4V and $V_{o4}$ = 1.8V, the voltage difference between $V_{o1}$ and $V_{o4}$, defined as the clamping voltage ($V_{clamp4}$), is given by

$$V_{clmp4} = | V_{o4} - V_{x2} | \approx V_{o1} - V_{o4} + V_d \tag{2-6}$$

which is equal to [(3.4V + 0.7V) – 1.8V] = 2.3V where $V_{X2} = V_{o1} + 0.7$V (where $V_d$ = 0.7V due to the body diode). Fig. 2-19 shows the amplitude of $V_{X2}$ for each channel. This large voltage difference will cause an in-rush current flowing from $V_{X2}$ to $V_{o4}$ instantaneously and generate a large spike.

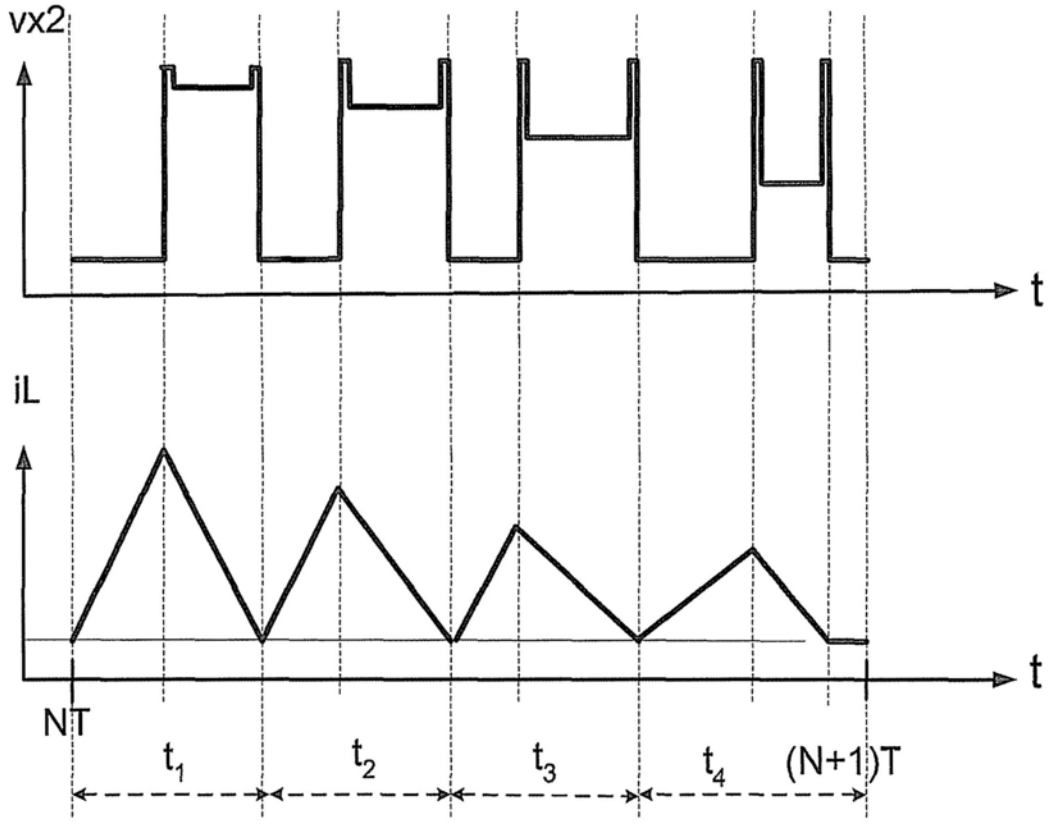



Fig. 2-19 Amplitude of $V_{X2}$ in a typical SIQO dc-dc converter.

To avoid of this voltage spike generated, a two-step gate-drive scheme is proposed. The benefit of this scheme is to make the output voltage spike of each channel similar to the single output-channel case independent of the voltage difference between two arbitrary channels. The proposed gate driving scheme is shown in Fig. 2-20. The gate driver of each channel (i.e. the buffer) has dual supplies. One supply voltage is the highest output voltage (i.e. $V_{o1}$) of the SIQO dc-dc converter. Another supply voltage is obtained from the output of the corresponding channel. The buffer itself will select the supply voltage based on a control signal (d4) for Channel 4 as an example.

The operation principle can be explained using Fig. 2-20. In the SIMO power converter with Class-1 inductor-current waveform, the SW_C period goes before delivering power to each output. The minimum duration of the SW_C period

depends on the minimum on-time as mentioned in the previous section in this chapter. Thus, the gate of the output PMOSFET can be pre-discharged during the SW_C period of the corresponding channel. Therefore, during the dead-time between the SW_C period and the SW_B period, $V_{X2}$ will be discharged to a voltage approximated to the output voltage of the corresponding sub-channel plus one diode voltage drop.

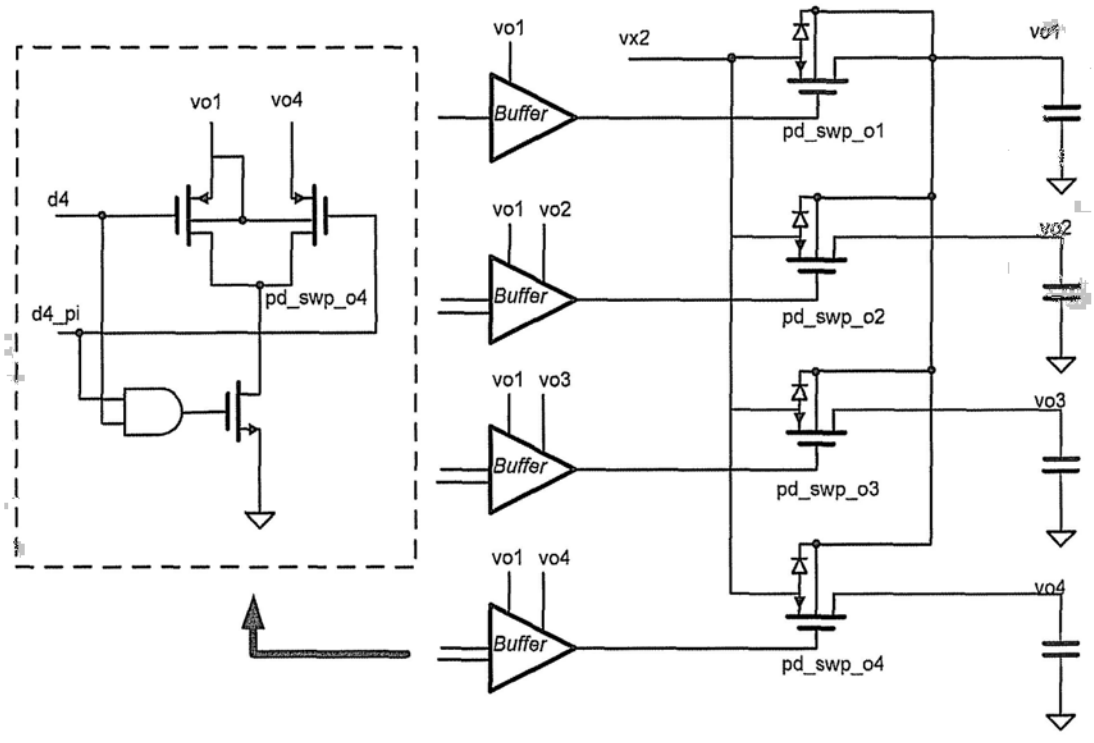



Fig. 2-20 Proposed two-step gate driver.

Thus, the clamping voltage is given by

$$V_{clamp4}' = | V_{o4} - V_{x2} | \approx V_d \tag{2-7}$$

which is much lower than the case without the proposed two-step scheme. The reduction of the clamping voltage can reduce the voltage spike, especially the channel with the lowest output voltage.

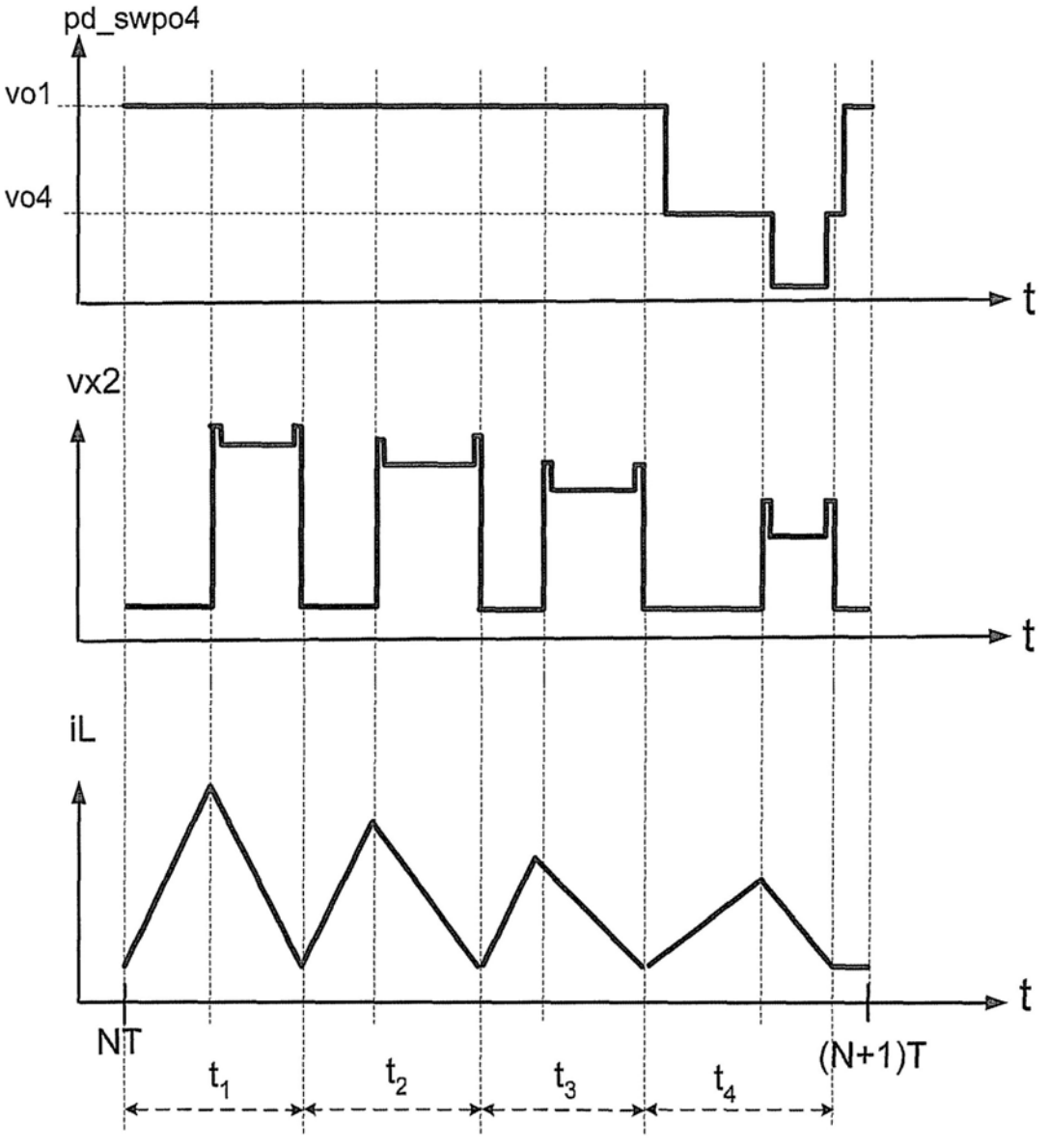



Fig. 2-21 Switching of gate drive for Channel 4 with proposed two-step scheme.

Figs. 2-22(a) and 2-22(b) show the simulation result without the proposed two-step driver. Figs.2-23(a) and 2-23(b) show the simulation result with the proposed two-step driver. From the results, it is found that the proposed two-step driver design can effectively achieve smaller voltage spike. On the other hand, by preventing $V_{x2}$ charging to unnecessary high voltage, switching loss will be reduced.

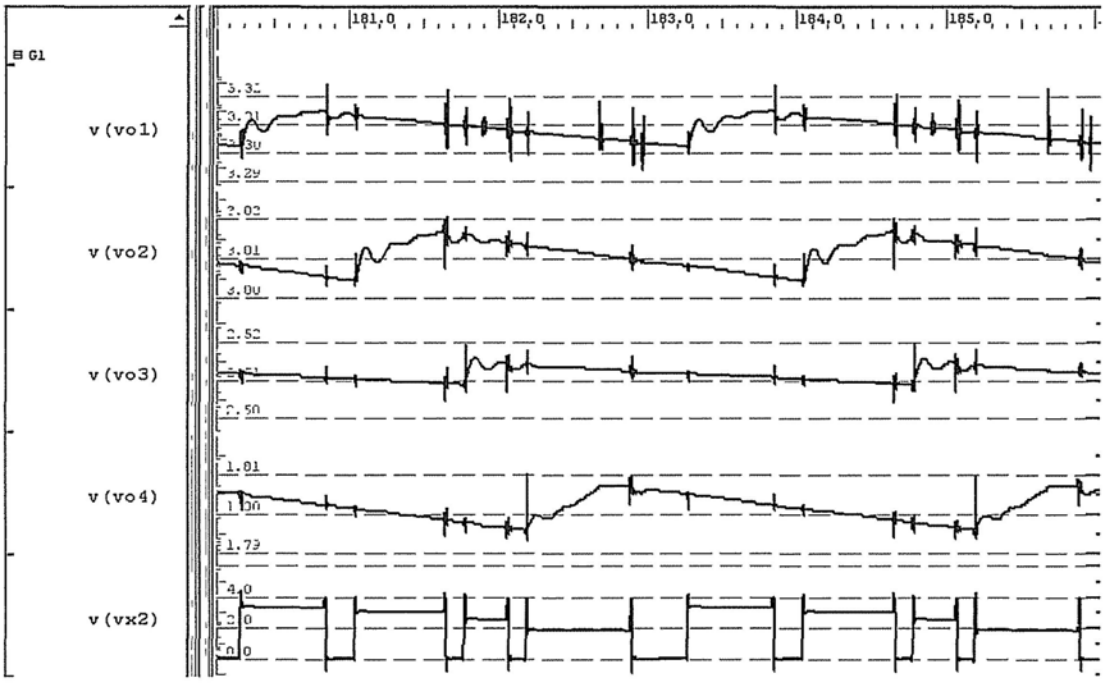



Fig. 2-22(a) Simulation: $V_{X2}$ without two-step gate drive scheme.

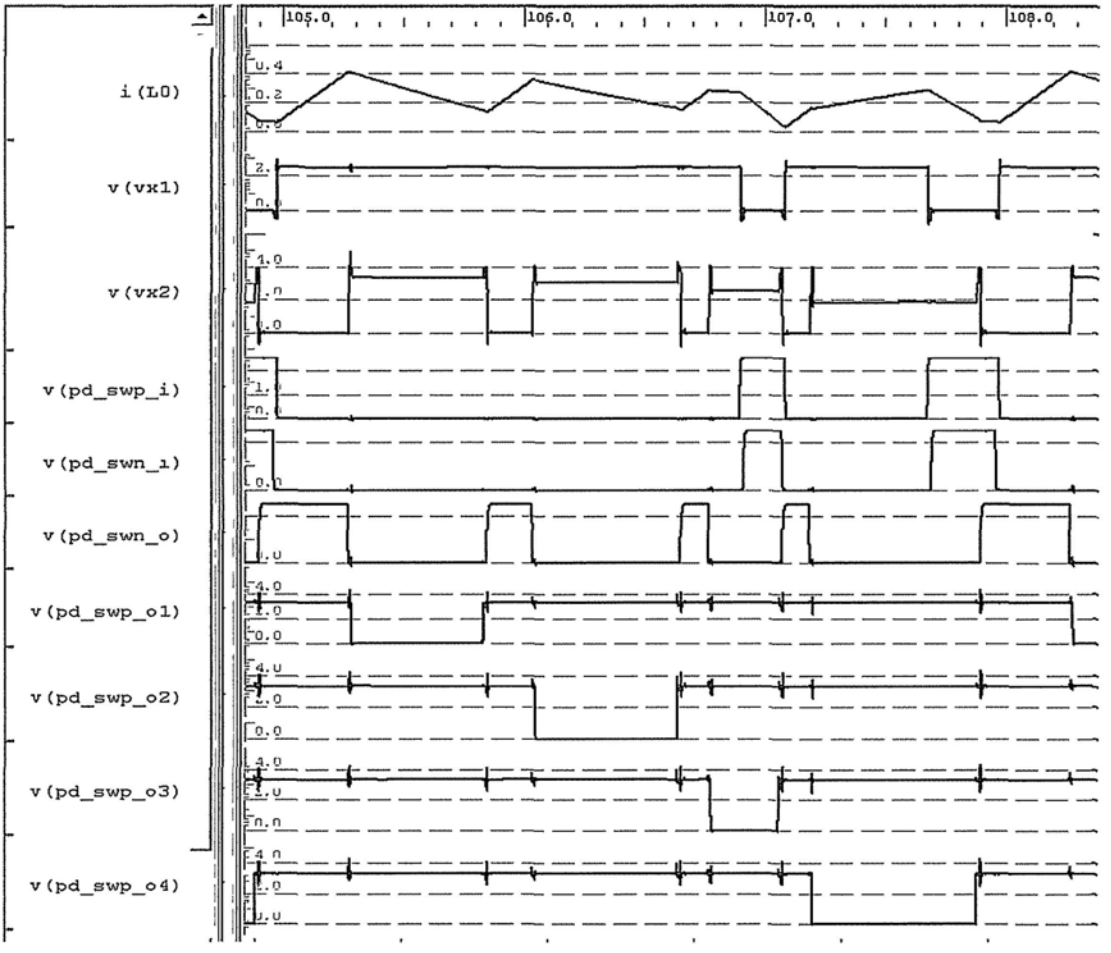



Fig. 2-22(b) Simulation: $V_{X2}$ without two-step gate drive scheme.

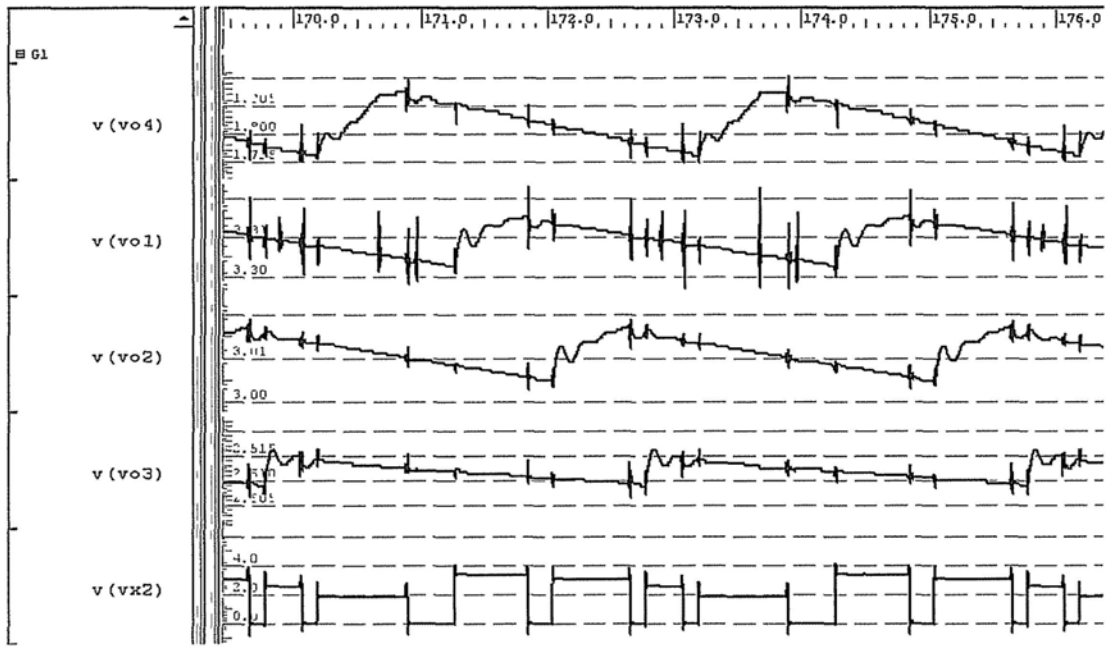



Fig. 2-23(a) Simulation: $V_{X2}$ with two-step gate drive scheme.

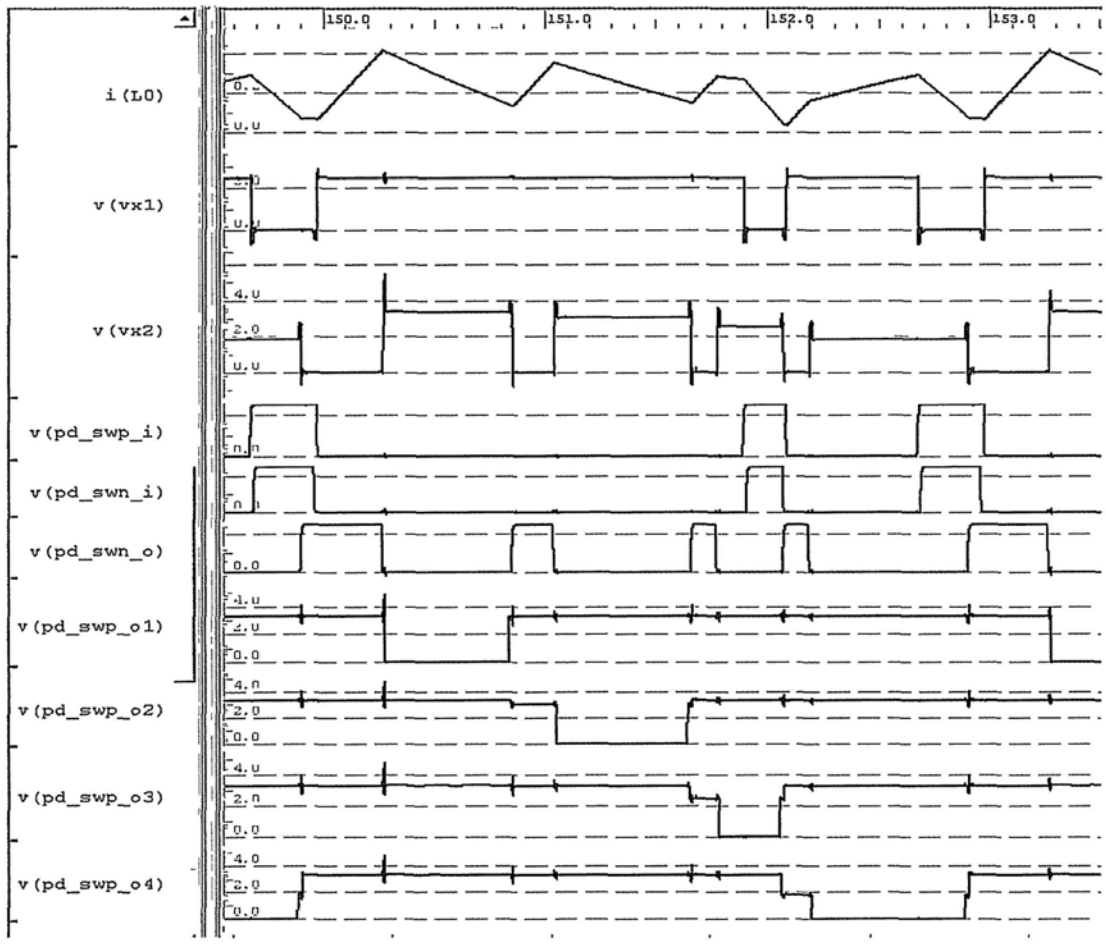



Fig. 2-23(b) Simulation: $V_{X2}$ with two-step gate drive scheme.

## 2.3 Controller Design and Control Mechanism

According to the operation of the power stage described above, a related control mechanism and its implementation will be presented in this section.

The circuit diagram of the controller is shown in Fig. 2-24. The input signals include: $V_{ref}$ = voltage reference, $V_{fb}$ = feedback signal from the output voltage, $I_{sense}$ = current-sensed signal from the inductor-current sensor, $I_{offset}$ = offset inductor current generated by the PLL, and *clk* = the clock pulse for state initialization. The output signals include *rst_cpm* = a duty command signal to control the SW_C period, *en_SW_PIN* = a duty command signal to control the SW_B period, *en_SW_R* = a duty command signal to control the SW_D period. Some internal signals include: $clk_1$ = a clock pulse with a falling edge delay comparing to *clk*, *rst_cpm_pi* = a duty command signal generated within the minimum on-time, *vr_swb* = ramp signal used to define the SW_B period in the buck-boost mode, *vr_swb* = ramp signal used to define the SW_D period in the reverse inductor discharge mode, and *vl* = conrol signal used to define the SW_B period or the SW_D period.

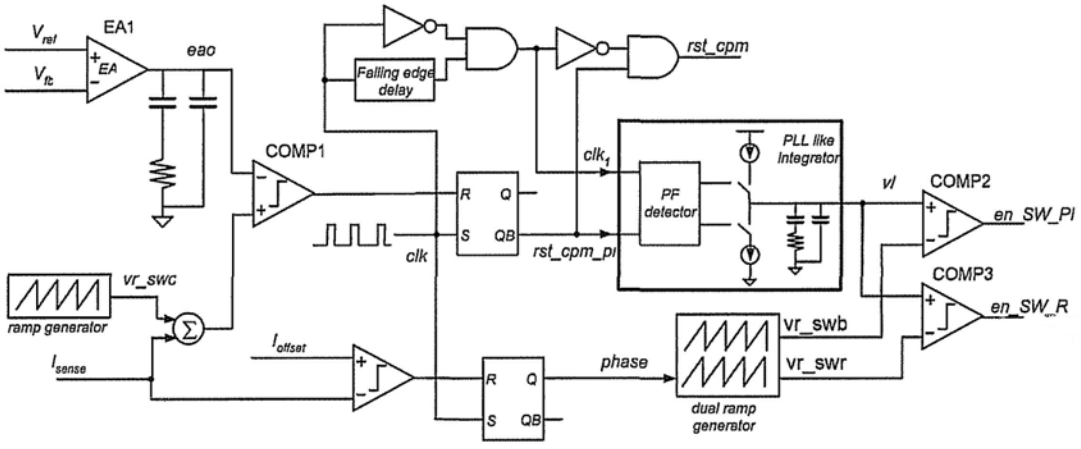



Fig. 2-24 Proposed controller circuit diagram.

The operation principle can be divided into four parts as below.

1. Auto buck-boost mode

After *clk* resets all the registers, the power stage enters inductor charging period (i.e. the SW_C period). Before the falling edge of $clk_1$, the output of COMP1 will be sampled by the RSFF as the signal *rst_cpm_pi*. If *rst_cpm_pi* = 1, it implies that *rst_cpm* will turn "1 after the minimum on-time. Then, if *vl* cuts the ramp signal *vr_swb*, it implies that the converter operate in the auto-buck-boost mode. The power stage will enter the SW_B operation after the end of the minimum on-time. The SW_B cycle will end after *en_SW_PI* resets and then the operation of the power stage enters the SW_D period. Finally, the power stage enters the SW_H operation when the signal phase resets when the inductor current falls to a pre-defined value defined by the signal $I_{offset}$. Detailed waveforms are shown in Fig. 2-25.

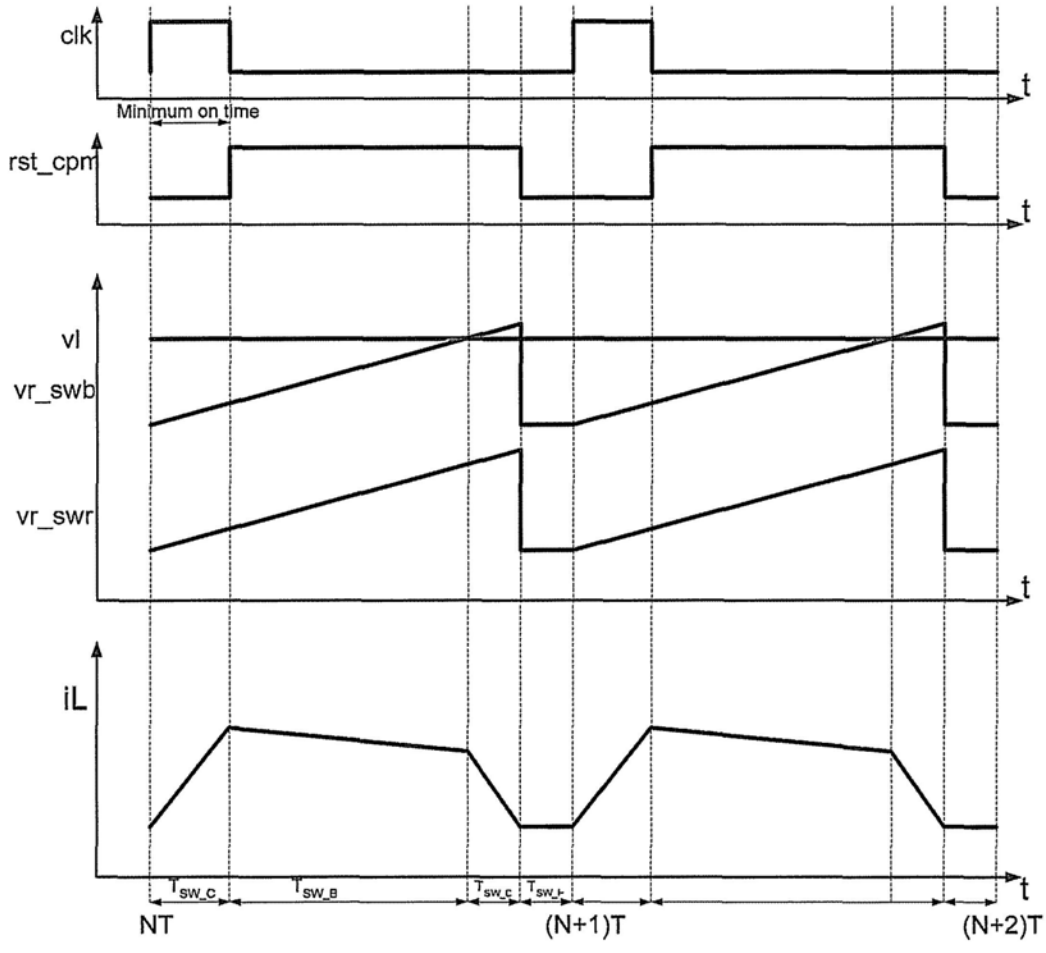



Fig. 2-25 Auto buck-boost mode.

2. Ultra light load mode (reverse inductor discharging mode)

Beginning from the end of the minimum on-time and *rst_cpm_pi* = 1, if *vl* stays below the initial dc level of *vr_swb*, it implies that the converter operates in ultra light load mode. The power stage will enter the SW_D period immediately after the minimum on-time. The SW_D cycle will end after *en_SW_PR* resets and then the operation enters the SW_R cycle. Finally, the power stage enters the SW_H period when signal *phase* resets when the inductor current falls to a pre-defined value defined by the signal $I_{offset}$. Detailed waveforms are shown in Fig. 2-26.

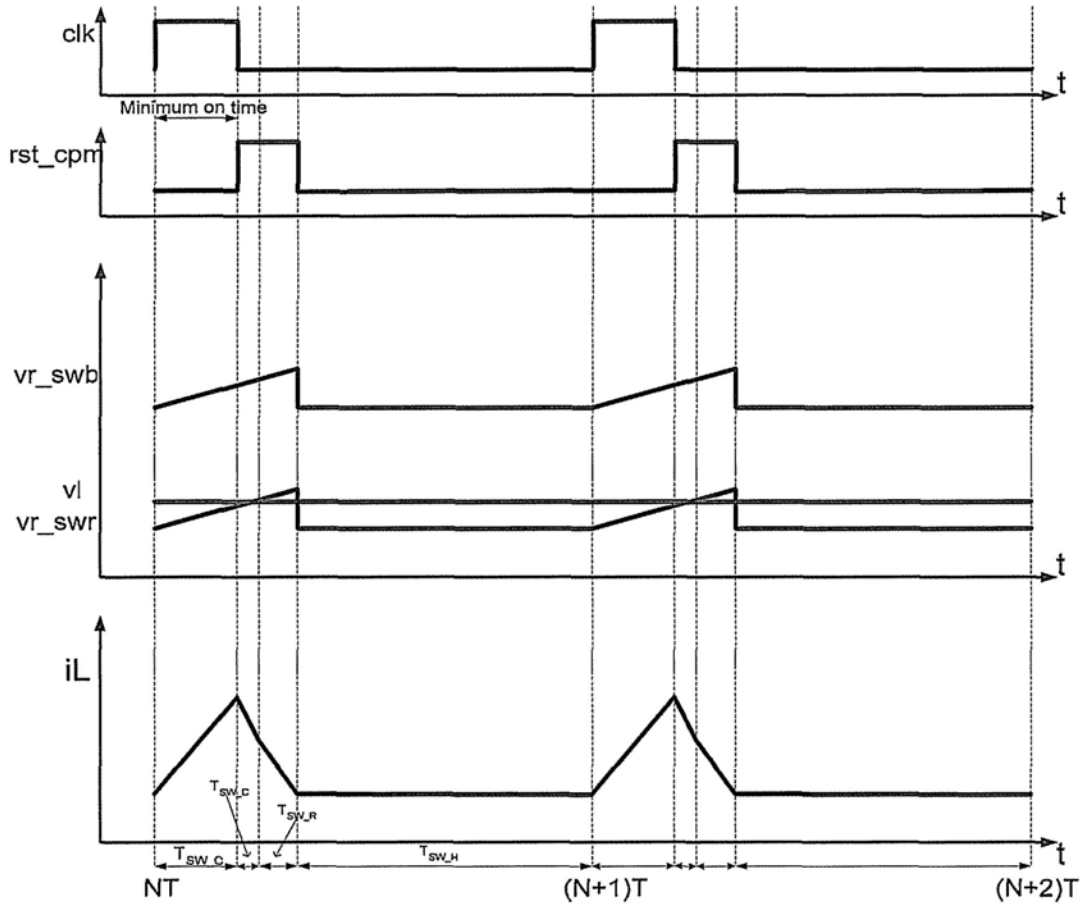



Fig. 2-26 Ultra light load mode.

3. Deep boost mode

If *rst_cpm_pi* = 0 at the falling edge of *clk1*, it implies that the SW_C cycle will be kept after the minimum on-time. The converter operates in the deep boost mode.

*rst_cpm* will keep equal to "0 after the minimum on-time. The SW_C cycle will end after *rst_cpm* resets to "1 and then the operation enters the SW_B period. For the deep boost mode operation, the inductor current normally has a large negative slope. As a result, the SW_B period will end and the power stage will then enter the SW_H period when the signal *phase* resets when the inductor current falls to a pre-defined value defined by the signal $I_{offset}$. Detailed waveforms are shown in Fig. 2-27.

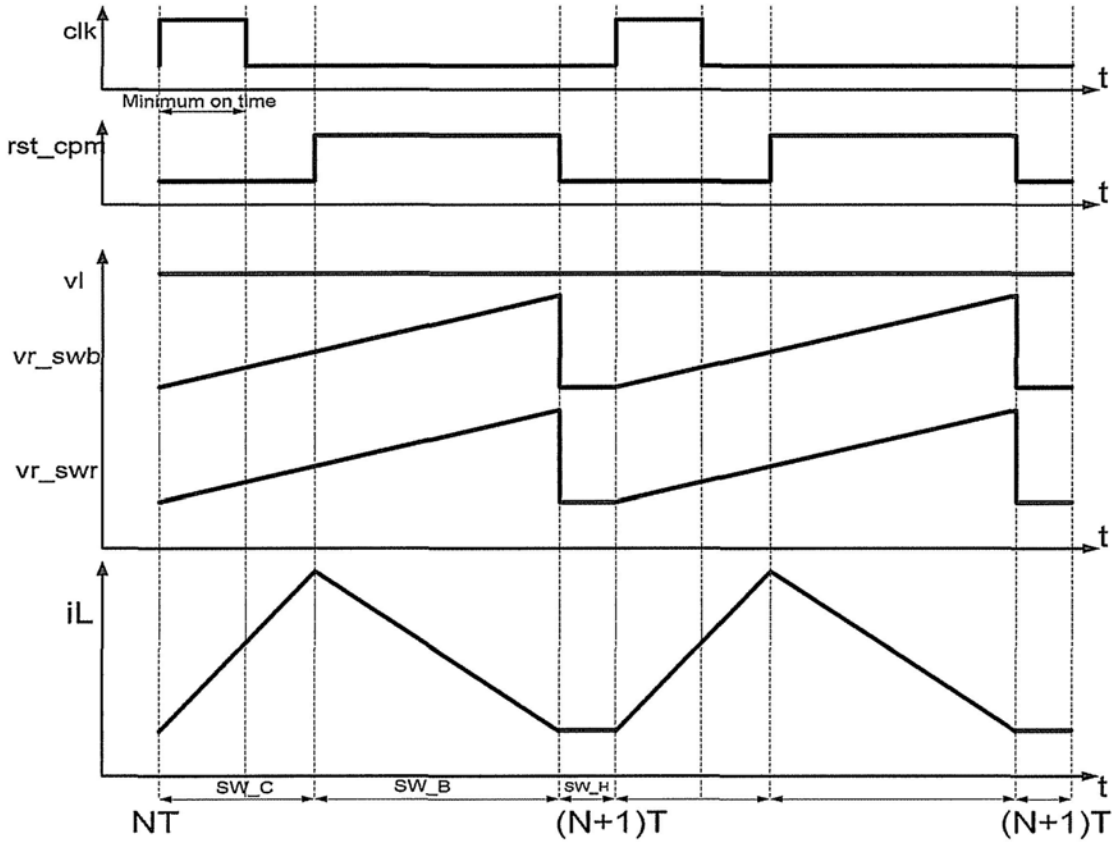



Fig. 2-27 Deep boost mode.

4. Switching between different modes

The steady-state behavior of the proposed dc-dc converter operating in different modes has been addressed before. However, other than using a hysteresis sensor to define the operation region, in this design, profiting from the control signals *eao* and *vl* generated by the conventional compensator and the additional PLL function like an integrator individually, the transient response between different modes is seamless.

In fact, *vl* can be considered as an extra control variable extracted from the major control variable *eao*. It provides more information for this multiple-mode controller. From the circuit diagram in Fig. 2-24, it is found that when the rising edge of *rst_cpm_pi* is after the falling edge of $clk_1$, *vl* will be charged up to saturation, which implies there is no intersection between *vl* and the dual ramp signals. As a result, this controller is similar to conventional current-mode controller. If disturbance happens such as loading changes or input-voltage changes, the falling edge of *rst_cpm_pi* may vary to appear before the falling edge of $clk_1$. Then, *vl* will be discharge to a proper level and define the SW_D period or the SW_R period based on when it interacts with the dual ramp signals. All these operations are continuous.

There are some requirements for the seamless transient between the ultra light load mode and the auto buck-boost mode. Referring to the circuit diagram of dual ramp generator in Fig. 2-28, there are some requirements for the separation between the dual ramp signals. Since these two operations will not exist at the same time, the SW_R period will appear only when *vl* cuts *vr_swr* but not *vr_swb*. The separation between these two ramps is used to ensure that the SW_R period can be a value approaching to 0. In other words, the switching mechanism can be seamlessly translated from the auto buck-boost mode to the reverse inductor discharge mode when the loading current decreases. The requirement of the amplitude of the ramp is stated in (2-8). It is noted that the signal *phase* is aligned to the starting and the end point of every channel.

$$\Delta V_{ramp} > S_{vr\_swr} \times \left( T_{mot} + \frac{T_{mot} \cdot V_g}{V_o} \right) \tag{2-8}$$

where $T_{mot}$ = minimum on-time, $\Delta V_{ramp}$ = separation between *vr_swb* and *vr_swr*, and $S_{vr\_swr}$ = slope of *vr_swr*, respectively.

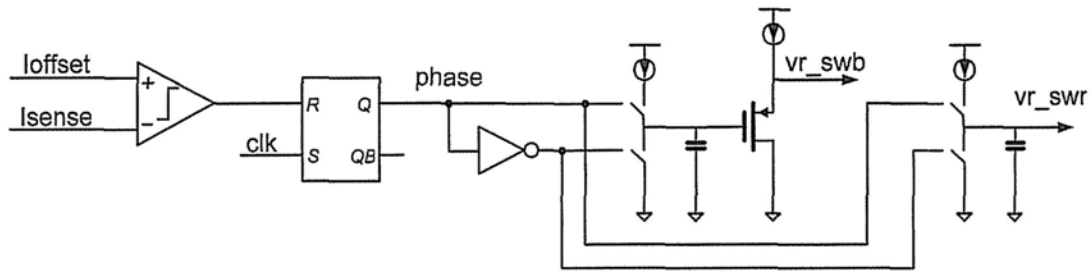



Fig. 2-28 Dual ramp generator.

The operation of multiple-mode controller is demonstrated in Channel 3 ($V_{o3}$) of the proposed SIQO dc-dc converter. The different operation modes corresponding to different load conditions are shown by simulations illustrated in Figs. 2-29, 2-30, 2-31 and 2-32. The specifications of the input and output voltages are $V_g$ = 2.5V, $V_{o1}$ = 3.3V, $V_{o2}$ = 3V, $V_{o3}$ = 2.5V and $V_{o4}$ = 1.8V. Fig. 2-29 shows the boost-mode operation where $I_{o3}$ = 220mA. Fig. 2-30 shows the auto buck-boost mode operation where $I_{o3}$ = 20mA and $I_{o1}$ = 50mA. Fig. 2-31 shows the ultra light load operation where $I_{o3}$ =20mA and $I_{o1}$ = 200mA. Fig. 2-32 shows Channel 3 mode transition due to the load transient of Channel 1 ($I_{o1}$ = 50mA → 200mA).

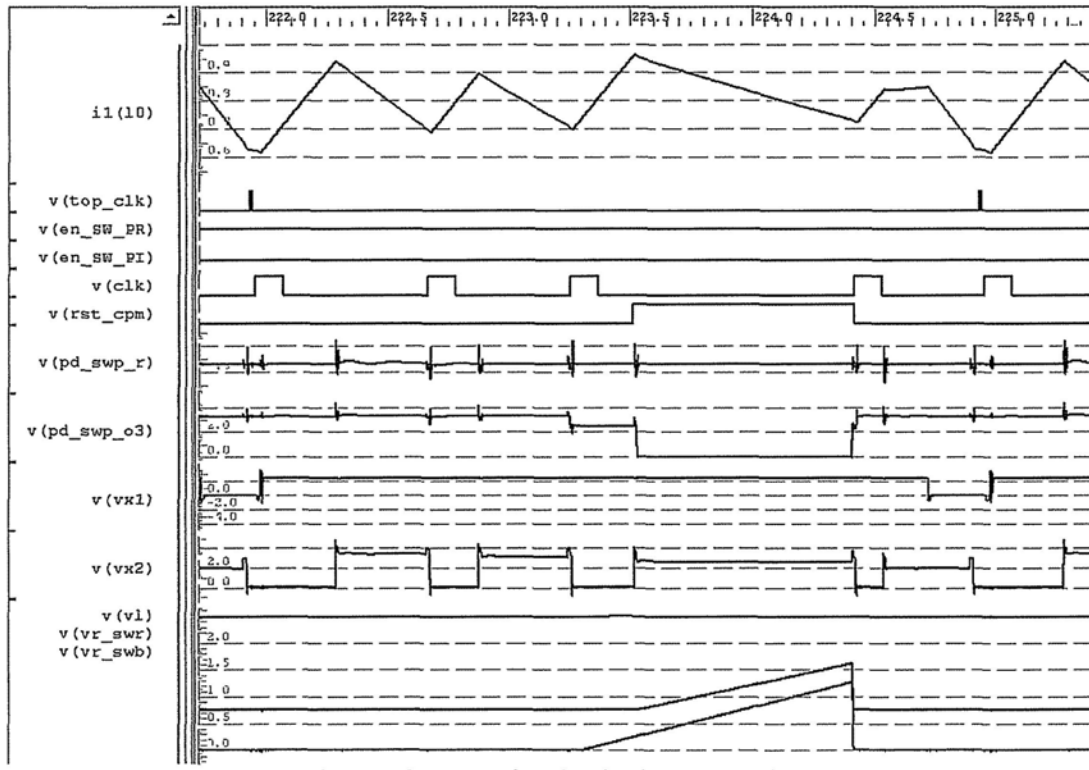



Fig. 2-29 Operating in the boost mode.

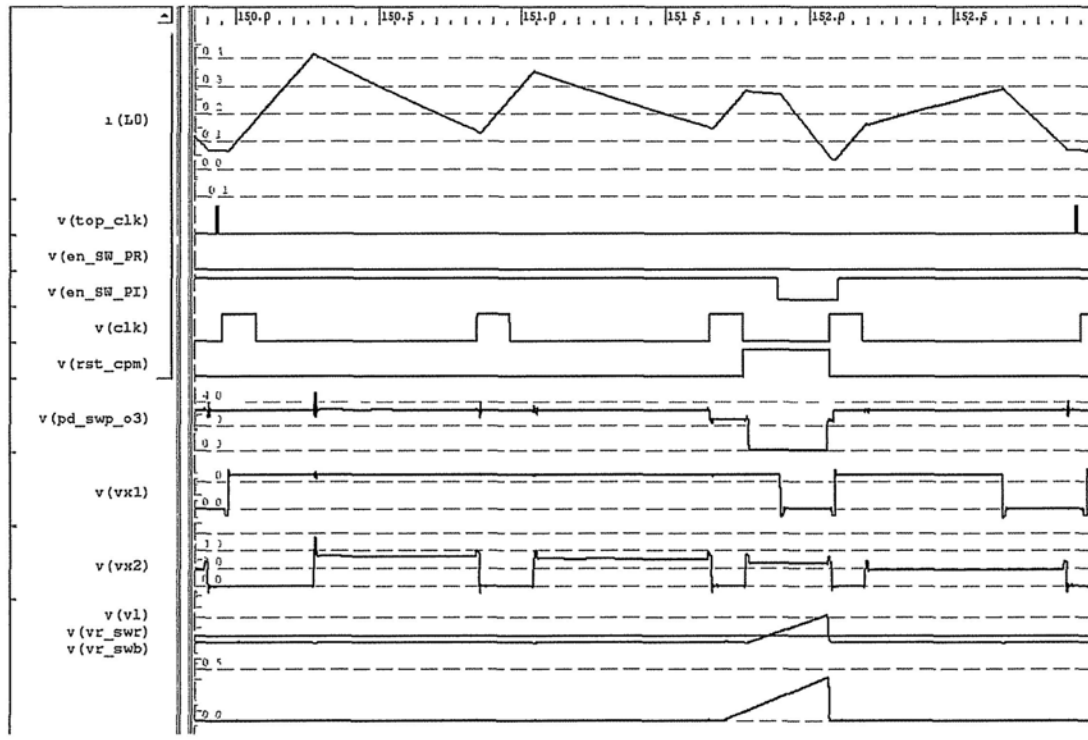



Fig. 2-30 Operating in the auto buck-boost mode.

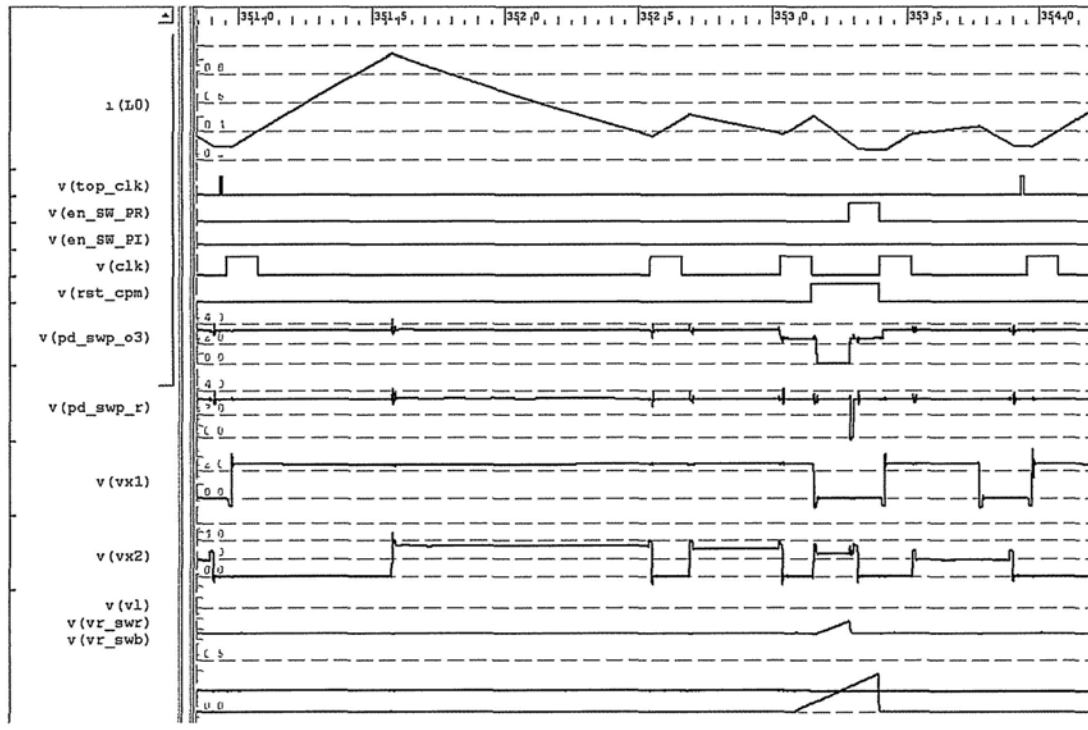



Fig. 2-31 Operating in ultra light load mode.

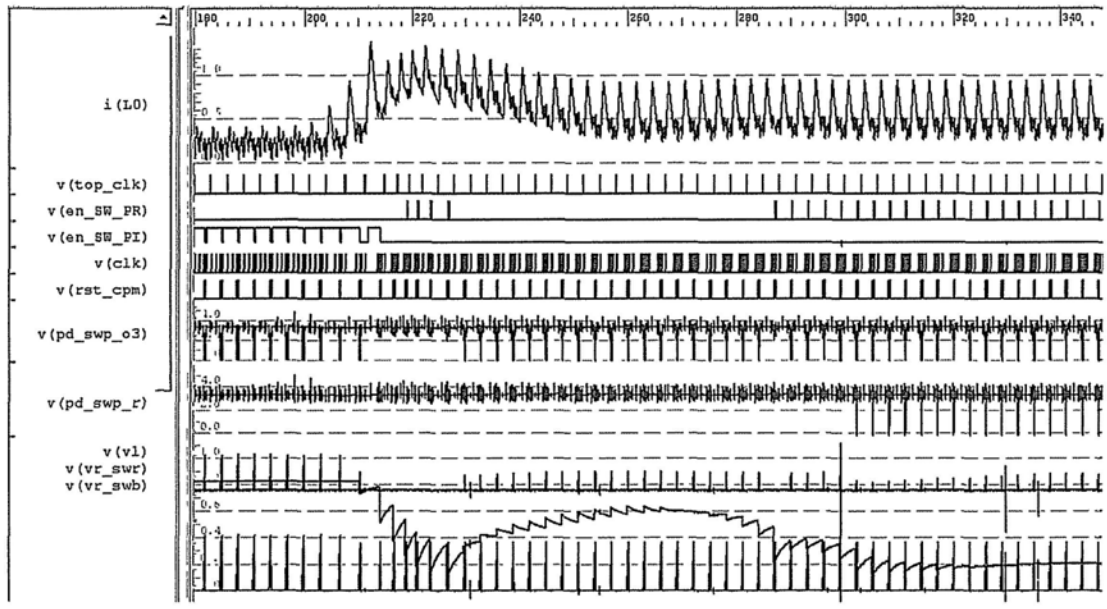



Fig. 2-32(a) Mode changes from the auto buck-boost to the ultra light load mode.

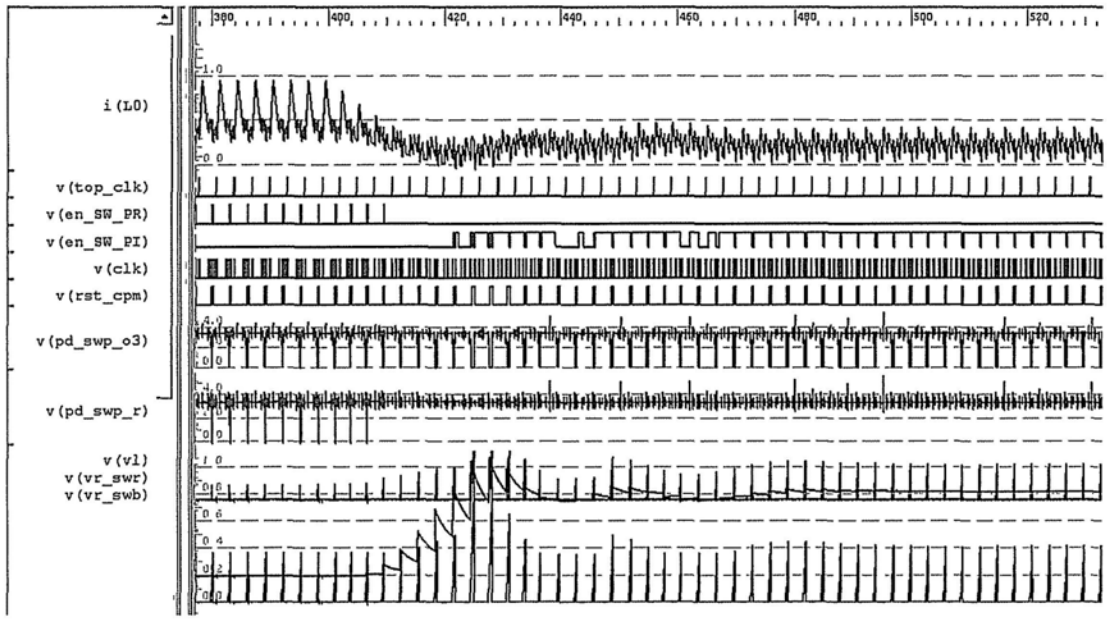



Fig. 2-32(b) Mode changes from the ultra light load to the auto buck-boost mode.

From the simulations, it is found that the mode switching of the observed channel not only depends on its load condition, but it also relates to the load condition of other channels. As a result, in this demonstration, although $V_{o3} = V_g = 2.5$V, it is still possible that this channel operates in the deep boost mode as shown in Fig. 2-29. The reason is that there is a lumped resistance connected in series with the inductor

including the on-resistance of switches, the ESR of inductor and the routing resistance. It makes the slope of the inductor-current waveform become very negative even when $V_g = V_o$. It is also the reason why it is not practical to use hysteresis switching.

## 2.4 Fixed-Frequency Operation with Adjustable Offset Inductor Current Based on PLL method

As aforementioned, in the multiple-mode controller, an input signal Ioffset is needed. The function of this signal is to dynamically define the offset inductor current shared by all sub-channels. The concept can be explained using Fig. 2-33.

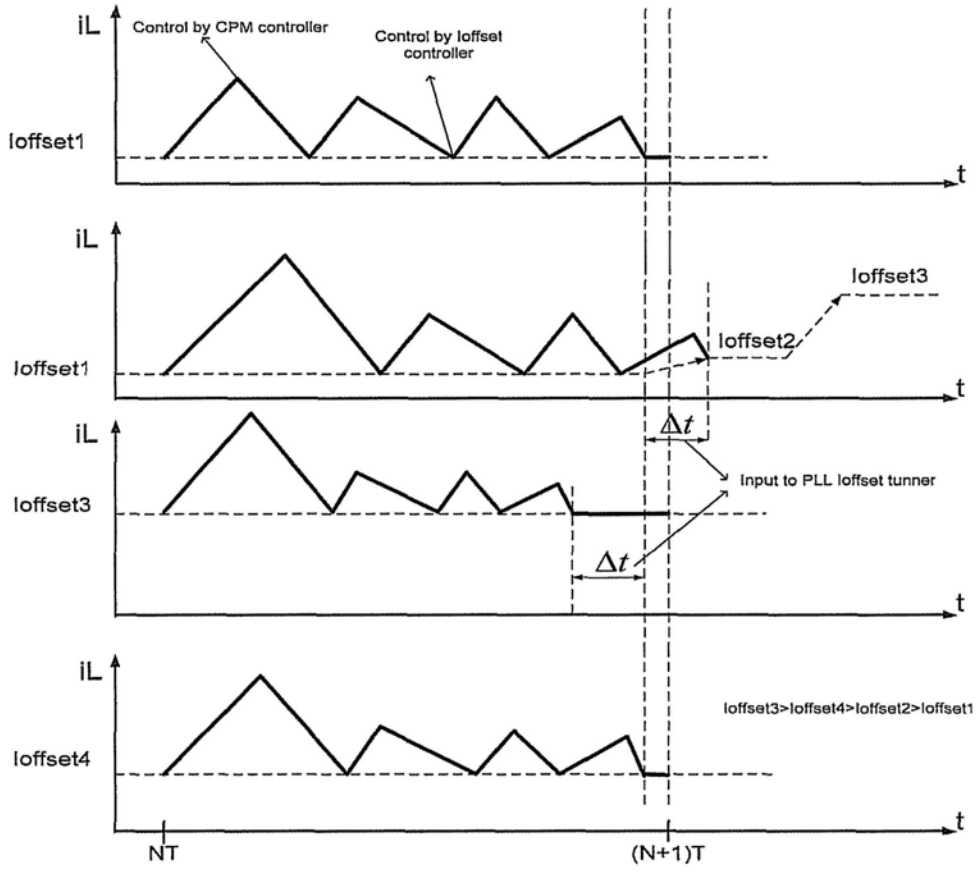



Fig. 2-33 Proposed fixed-frequency operation with adjustable offset inductor current based on PLL method.

When the loading currents of some channels are increased, the switching period will increase temporarily since the sub-period of the sub-channel is increased. Based on this information (the difference between the temporarily increased switching period and the reference switching period), $I_{offset}$ will be increased so that the offset inductor current will be increased. Since higher $I_{offset}$ will have higher power delivery capability with the same switching period [2], the ultimate switching period will be locked within one reference switching period. This operation is similar to a conventional PLL's operation. However, due to the special application in this SIMO design, some more modifications will be needed. In the following of this section, $I_{offsest}$ generator (the Ioffset tuner) and the peripheral circuits (a variable clock generator and a phase generator) which are used to complete the offset inductor current feedback loop in the control of the SIQO dc-dc converter will be presented in detail.

1. Offset inductor current feedback loop

The circuit diagram of the offset inductor current feedback loop is shown in Fig. 2-34. It can be found that in addition to the major voltage and current feedback loop shown in shadow, an offset inductor current feedback loop is involved. The input signals include $I_{sense}$ = the current-sensed signal from the inductor-current sensor, $I_{offset}$ = the offset inductor current generated by the Ioffset tuner, and lock_clk = an external clock pulse and its pulse width defines $T_{lck}$. The output signals include *phase_end* = a digital signal which shows that the operation of all channels completed in one period. Some important internal signals include *ref_clk* = a clock pulse generate by the falling edge of *lock_clk*, *insert_clk* = a clock pulse generated by the rising edge *phase_end*, and *sub_phase_end* = the offset current comparator output.

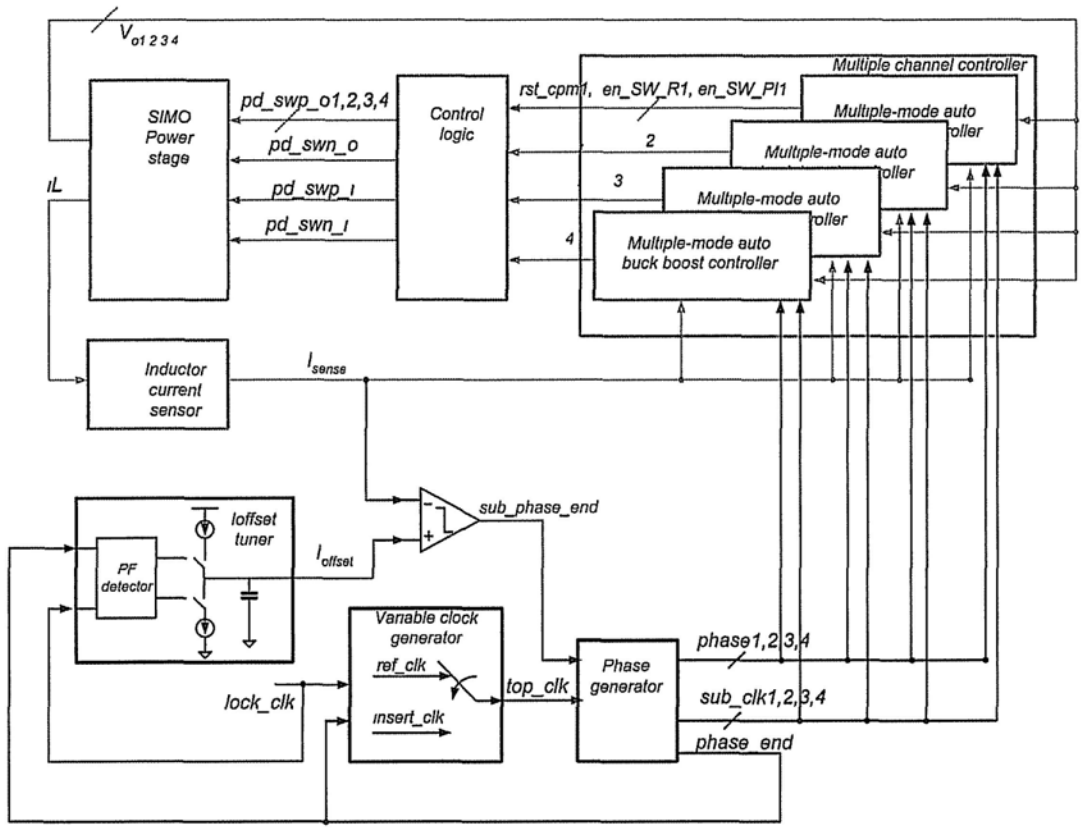



Fig. 2-34 Circuit diagram of the offset inductor current feedback loop.

As shown in Fig. 2-35, in the first period, the system operates in steady state. During the second period, the loading current of Channel 1 increases suddenly. The multiple-channel controller in the voltage feedback loop makes this sub-channel charging cycle increase. As a result, the total phase width is enlarged and *phase_end* appears after the rising edge of *lock_clk*. The phase difference between the rising edge of *phase_end* and the rising edge of *lock_clk* becomes the input to the $I_{offset}$ tuner. This will charge the capacitor inside the Ioffset tuner and then $I_{offset}$ will be increased.

On the other hand, since *phase_end* appears after the falling edge of *lock_clk*, *ref_clk* will be missed and the system clock signal *top_clk* is generated by the falling edge of *phase_end* and then it triggers the next phase operation. This variable clock generation scheme will be presented later in this section.

$I_{offset}$ is kept increasing until *phase_end* appears before the rising edge of *lock_clk*. This can be found at the end of $(N + 4)T$. After that, the offset inductor current feedback loop will perform a phase lock action, since *top_clk* is no longer generated by *phase_end* but is created by *lock_clk*. Before *ref_clk* appears, the power stage will perform a hold action to retain the inductor current. The phase difference will enter the $I_{offset}$ tuner and decrease $I_{offset}$ to be a suitable value so that the phase error will finally approach to zero, and it is shown that the rising edge of *lock_clk* relates to $(N + 5)T$. Similarly, when the loading current decreases, the feedback mechanism will directly enter the phase-locking procedure.

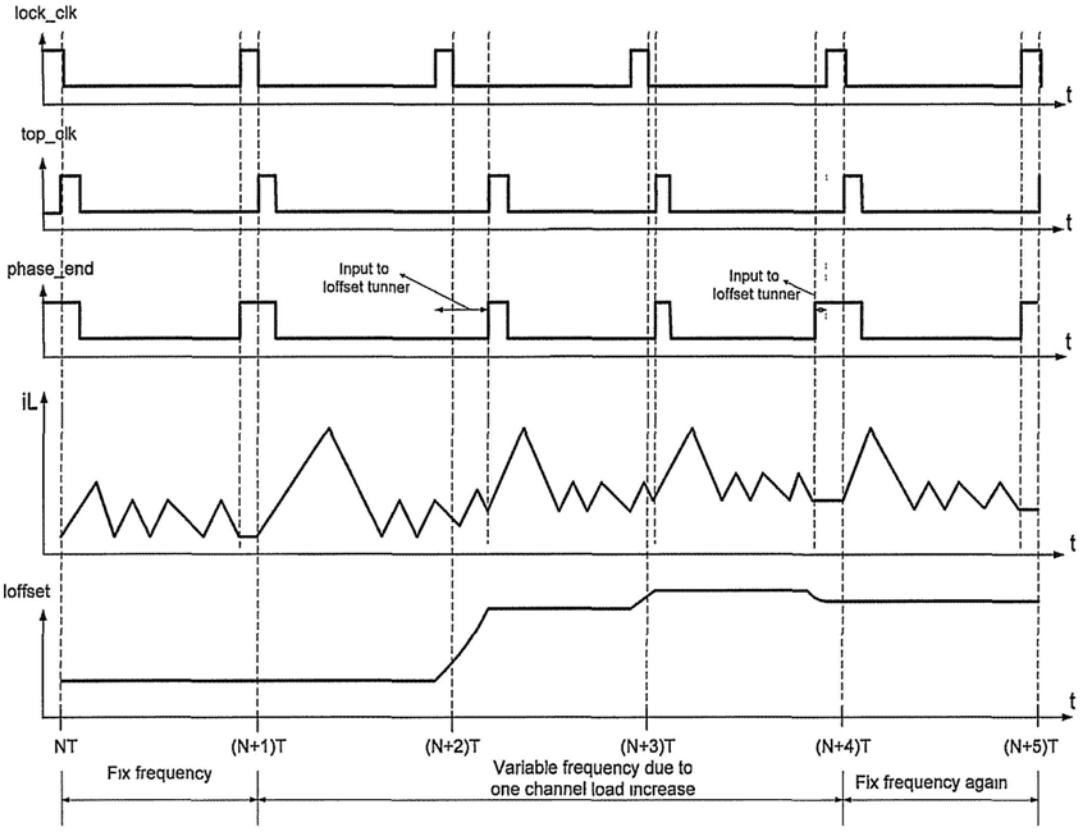



Fig. 2-35 Transient waveforms of the offset inductor current feedback loop.

2. *I*-offset tuner design and its order

As referred above, the appearance of the hold period (i.e. SW_H) makes this control mechanism a bit different from the conventional PLL design. This *I*-offset tuner adopts a quasi-frequency locking which combines both the frequency locking

(large signal) and the phase locking (small signal) together. The advantage of this technique is that a first-order discrete time controller is sufficient for the feedback. Figs. 2-36(a) and 2-36(b) show the gain factor ($K_{pipk}$) between the peak-current control signal (i.e. $i_{pk}$) and the phase difference (i.e. $\Delta\phi$). Figs. 2-36(c) and 2-36(d) show the gain factor $K_{piof}$ between $I_{offset}$ and $\Delta\phi$.

$$K_{pipk} = \frac{\Delta\phi}{\Delta i_{pk}} = \frac{\Delta\phi_2 - \Delta\phi_1}{\Delta i_{pk}} \tag{2-9}$$

$$K_{piof} = \frac{\Delta\phi}{\Delta I_{offset}} = \frac{\Delta\phi_2 - \Delta\phi_1}{\Delta I_{offset}} \tag{2-10}$$

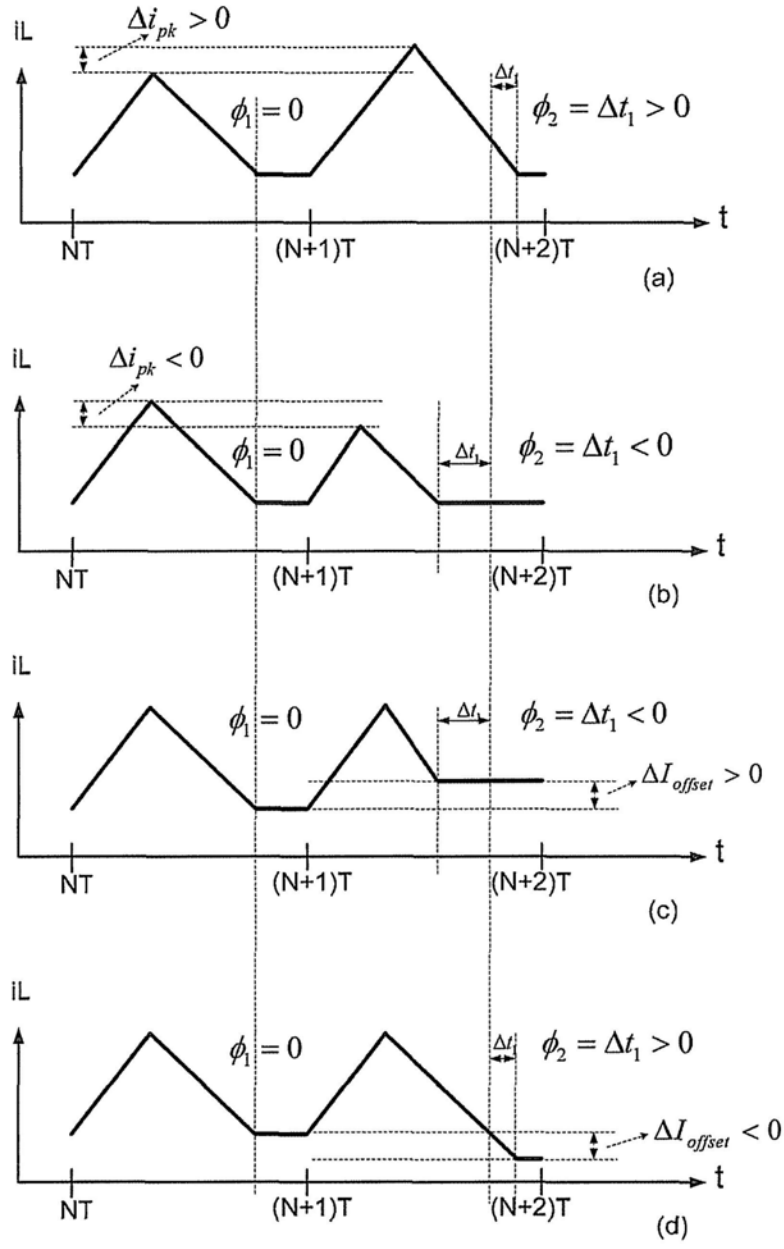



Fig. 2-36 Small-signal model deviation during phase locking.

Their values depend on the operation region of the power stage. It is obvious that it is due to excluding the integration effect from frequency to phase. In the phase-locking period, the offset inductor-current feedback loop can be controlled by a single-pole integrator. Moreover, once there is a large disturbance which makes the system enters the frequency-locking period, the control mechanism will always shift the system into the phase-locking period. Normally, there will not be a system clock variation provided that converge is smooth without any ringing. However, even though system clock variation arises due to over compensation due to continuous system combining, the system will keep damping in the phase-locking period. The signal flow graph (SFG) of the controller and its transient response are shown in Fig. 2-37.

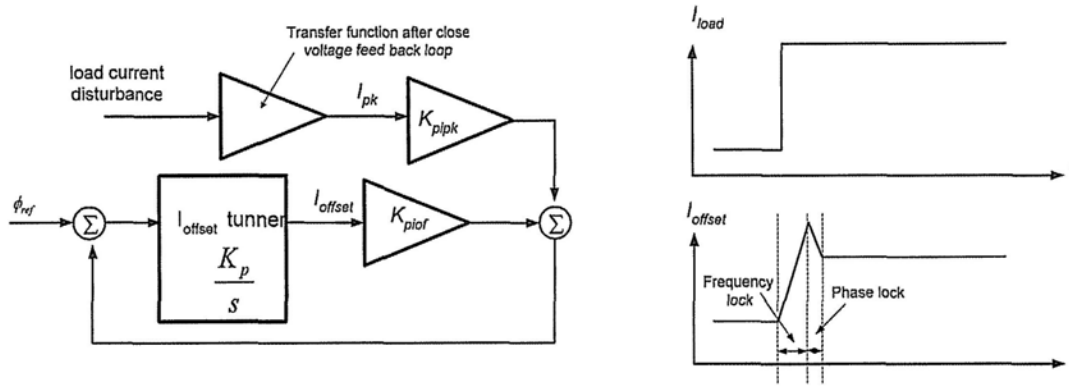



Fig. 2-37 Offset inductor current feedback loop SFG and its transient response.

The only drawback of this approach is a non-zero locking time is always needed for the locking-phase mechanism. However, when the locking time is much smaller than the operation period, e.g. <5%. The loss due to the locking time is ignorable. In fact, it may be quite deserved to have this trade-off between the order of the controller and noise immutability.

3. Variable clock generator and phase generator

The function of variable clock generator is to determine the appearance of *top_clk* which is used to reset and initialize the phase generator. After being reset, the phase generator will generate a phase enable signal *phase(X) (X=1, 2, 3 or 4)* and a related clock signal *sub_clk(X) (X* =1, 2, 3 or 4*)* for each channel one by one. All these digital signals are used to initiate or enable the operation of the sub-channels. The circuit diagram of the variable clock generator and the related waveform of phase generator are shown in Fig. 2-38. It is found that *phase(X)* will appear one after another seamless without overlapping. The end point of *phase(X)* is the starting point of *phase(X+1)*, and both of them are triggered by *sub_phase_end.* A signal appears when the sensed inductor current falls to $I_{offset}$. The operation of phase generator ensures that, in the steady state, total period will be adaptively allocated to each channel, provided that $T_{lck}$ is ignorable.

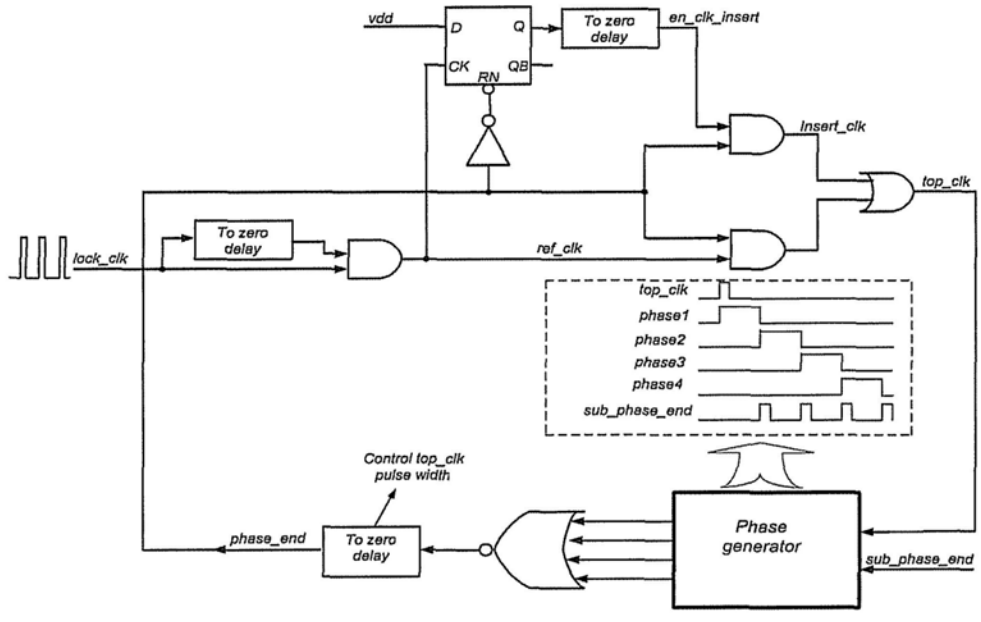



Fig. 2-38 Variable clock generator and phase generator.

As referred earlier in this section, the operation of offset inductor-current feedback loop combines both the phase-locking state and the frequency-locking state.

*top_clk* is generated based on the state of the system is located in. The state information is reflected by the signal *en_clk_insert*. In fact, *top_clk* will be aligned to either the rising edge of *ref_clk* or the rising edge of *phase_end*. As shown in Fig. 2-39, when operating in the steady state (i.e. Fig. 2-39(a)) or phase-locking state (i.e. Fig. 2-39(c)), *phase_end* appears earlier than the falling edge of *lock_clk*. *top_clk* is aligned to *ref_clk*.

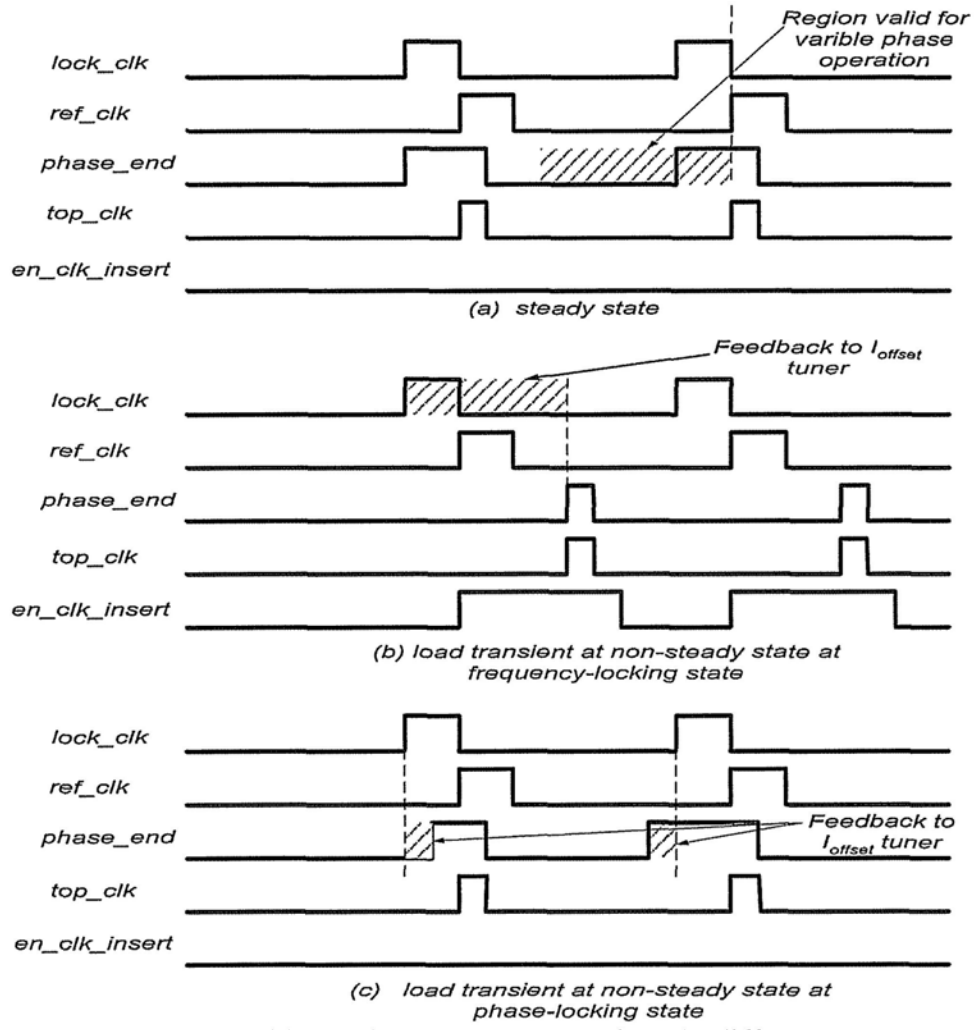



Fig. 2-39 Variable clock generator's waveform in different states.

When operating in the frequency-locking state (i.e. Fig. 2-39(a)), *phase_end* appears earlier than the falling edge of *lock_clk*. *top_clk* is aligned to *insert_clk*. From these waveforms, it can be found that the criterion is the appearance sequence of the rising edge of *phase_end* and the falling edge of *lock_clk*.

4. Simulation

The simulation in Fig. 2-40 shows the phase-locking state and the settling of the offset current control variable (i.e. $I_{offset}$), responding to the loading of Channel 1 decreases.

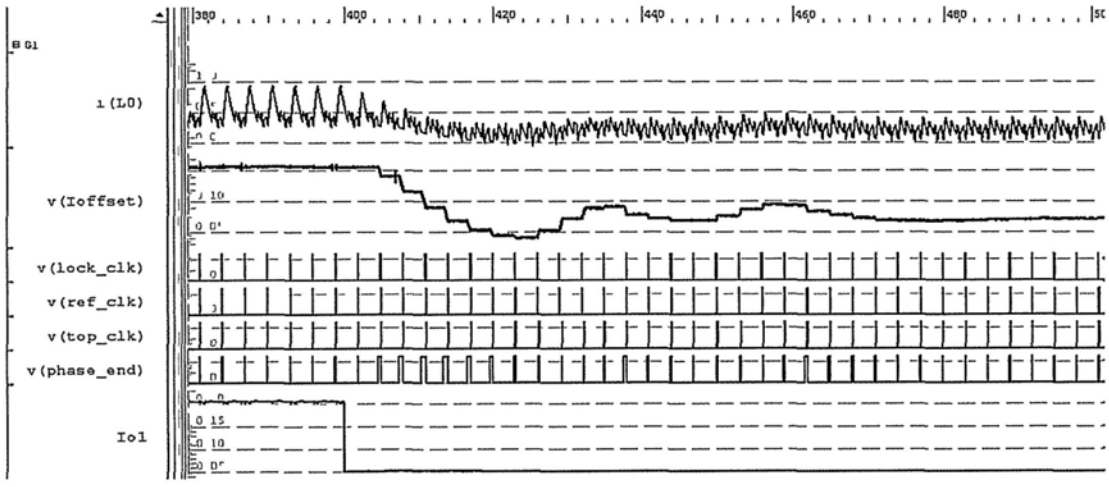



Fig. 2-40 A 150-mA step-down load transient response of Channel 1.

The simulation in Fig. 2-41 shows the frequency-locking state (200μs to 220μs), phase-locking state (after 220μs) and settling of the offset current control variable (i.e. $I_{offset}$), responding to the loading of Channel 1 increases.

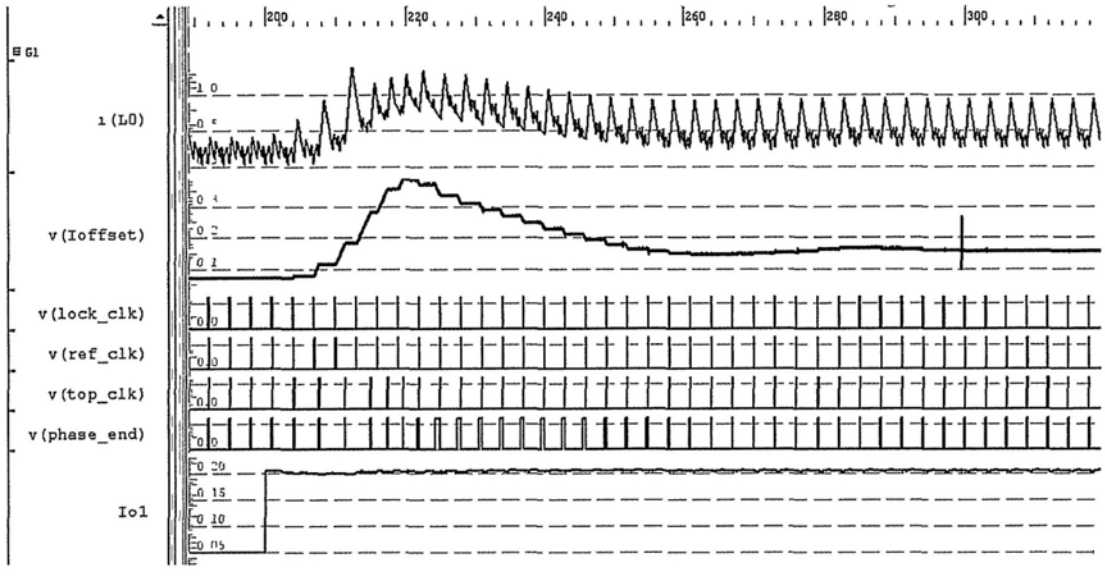



Fig. 2-41 A 150-mA step-up load transient response of Channel 1.

## 2.5 Full-Wave Inductor-current Sensing Circuit

As shown in Fig. 2-42, a full-wave inductor-current sensing circuit is not only needed to realize the current program mode (CPM) based multiple-output controller and used in the current limiter to avoid the inductor current over maximum rating, but it also provide an input to the offset inductor-current comparator to complete the offset inductor-current feedback loop. Based on this operation, different from the inductor-current sensing circuit used in a conventional single-channel CPM controller, a full-wave inductor-current sensing circuit (to extract slopes of the rising and the falling edge of the inductor-current waveform) is needed in this design. It is shown in Fig, 2-42 that either SW_PI or SW_NI in the input of the power stage is connected to *vx1*. As a result, the combination of these two power switches can be used to represent the full-wave inductor current.

The schematic of the full-wave current-sensing circuit is shown in Figs. 2-43(a) and 2-43(b). Signal *en_p_sense* = 1 when SW_PI is on, and *en_p_sens* = 0 when SW_NI is on. In Fig. 2-42(a), when *en_p_sense* = 1, the current of SW_PI is sensed by PMOS MP_SENSE. Since vx1 is connected to n4, n5 will track vx1 by the feedback loop formed by MN9, MN10, MN8, MN7, the four-input OTA, MP1, MP2, MN4 and MN5. At the same time, since both n+ and n- are tight to the ground, these two inputs will only give a common-mode signal to the OTA. As a result, MP_SENSE will have the same gate, source and drain voltage as SW_PI has, and so its drain current will be $i_L/K$. Since MN5 and MN6 have same size, the inductor current $i_L$ will be sensed according to the ratio of $I_{sense} = i_L/K$.

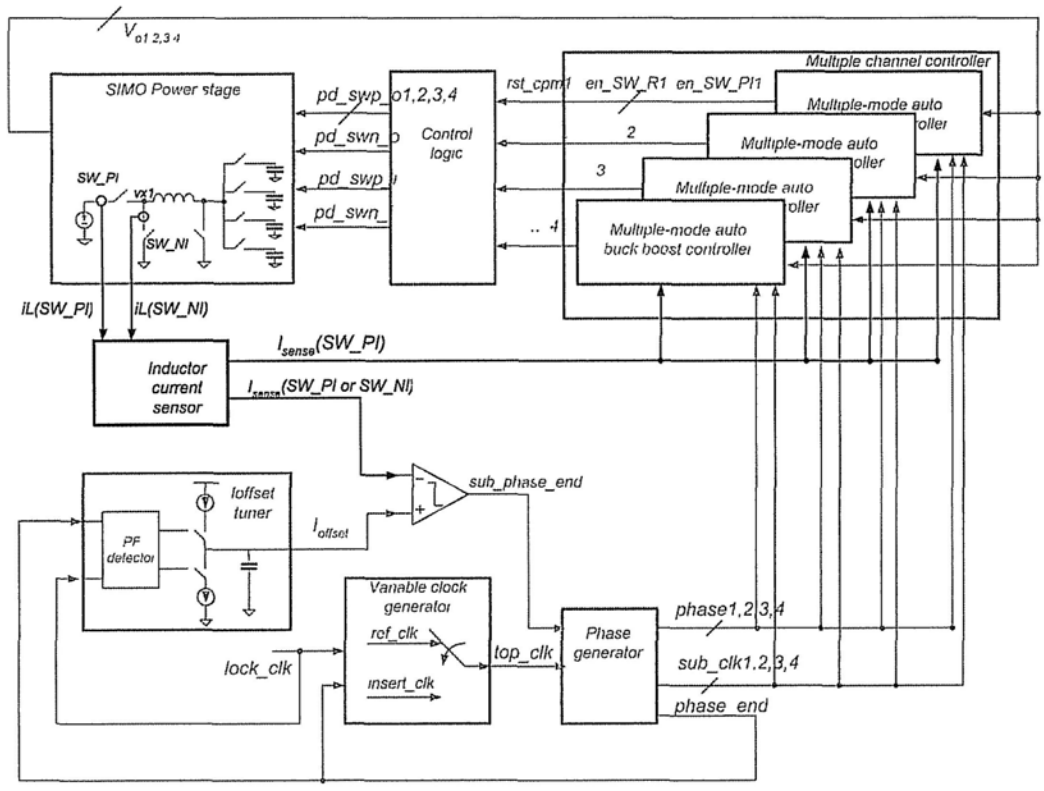



Fig. 2-42 Connection and function of the full-wave current-sensing circuit.

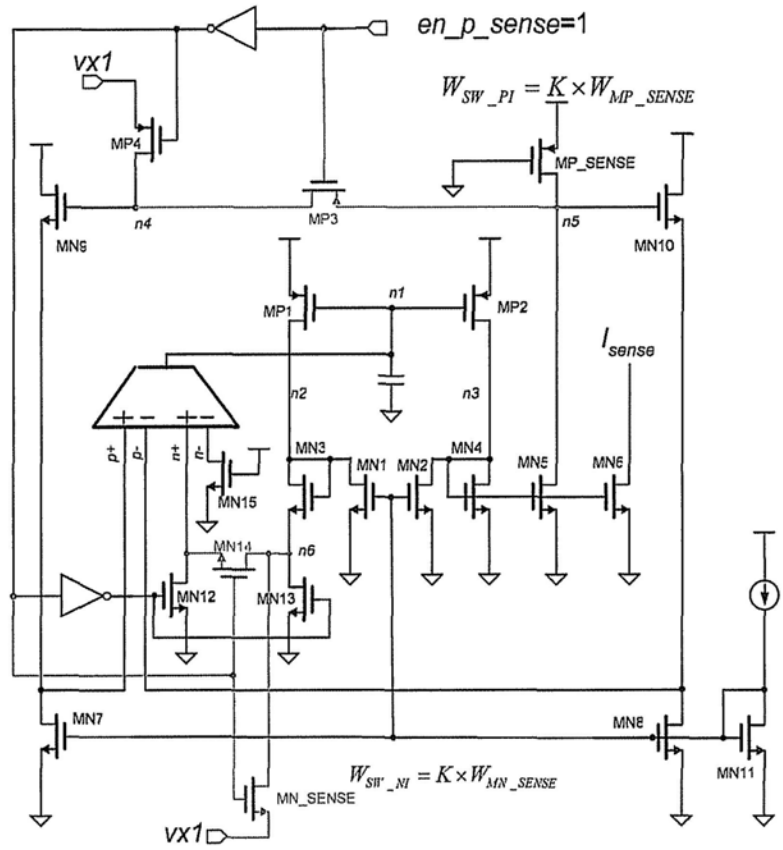



Fig. 2-43(a) SW_PI current sensing.

In Fig.2-43(b), when *en_p_sense* = 0, the current of SW_PI is sensed by MN_SENSE. Since n+ is connected to n6, n6 will be defined to the ground by the feedback loop formed by MN14, the four-input OTA, MP1, MP2 and MN3. At the same time, p+ and p- will provide a common-mode signal since n4 and n5 are tight together. As a result, MP_SENSE will have the same gate, source and drain voltage as SW_NI has, and so its drain current will be $i_L/K$. Since MN3, MN4, MN5 and MN6 have same size, the inductor current $i_L$ will be sensed according to the ratio of $I_{sense} = i_L/K$.

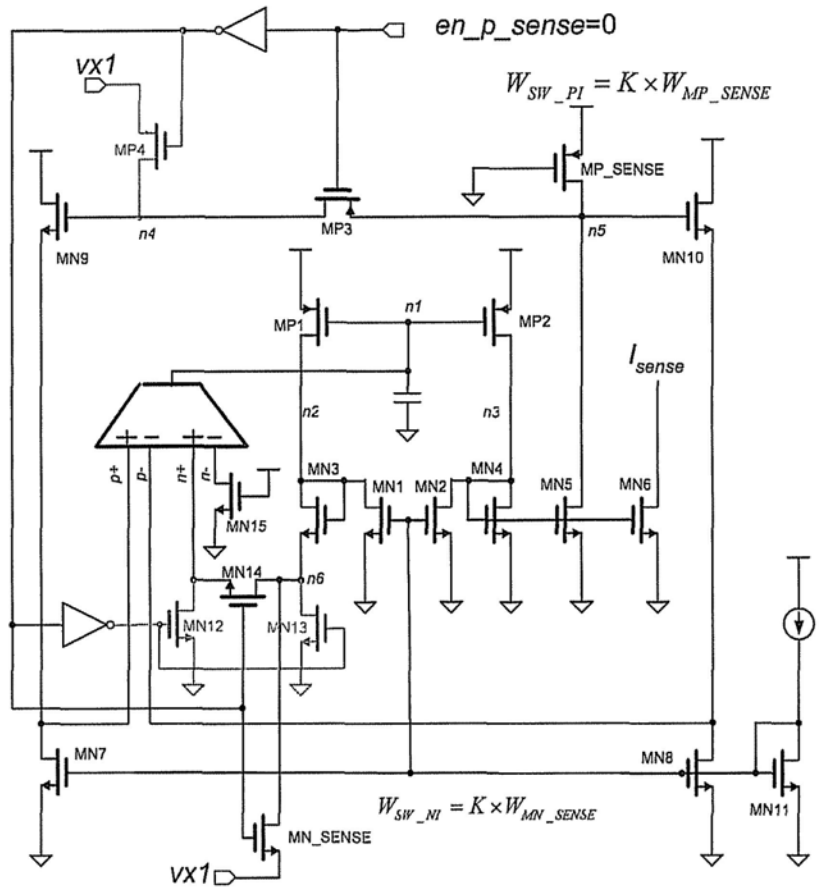



Fig. 2-43(b) SW_NI current sensing.

The schematic of the four-input OTA is shown in Fig. 2-44. It uses a folded-cascode architecture with the two pairs of gm cell with their drain currents summed at nodes s1 and s2.

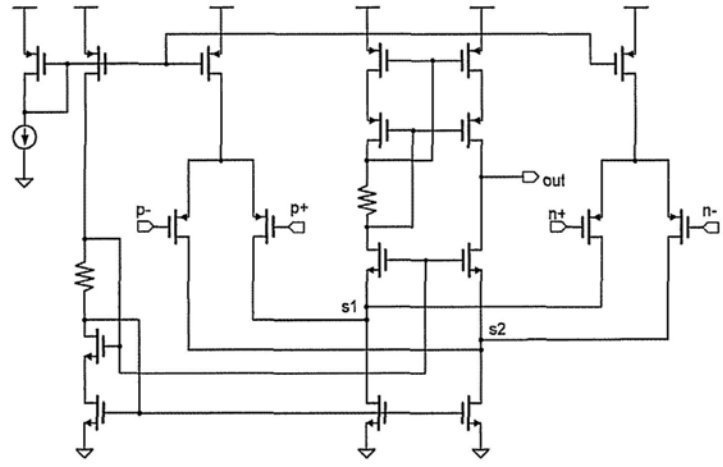



Fig. 2-44 Four-input OTA in the inductor-current sensing circuit.

It is found that no matter in the current-sensing state for SW_PI or for SW_NI, the only high impedance node is n1. As a result, dominant-pole compensation is sufficient and a 150-fF capacitor is added at node n1 to create the dominant pole. Diode-connected NMOSFETs MN3 and MN4 are used to provide a minimum biasing to prevent parasitic poles appearing at low frequency when $i_L$ approaches to zero. An independent transient and frequency simulation of the proposed full-wave inductor-current sensing circuit is shown in Fig. 2-45 and Fig. 2-46. The simulation for the sensing circuit combined with the whole system is shown in Figs. 2-47(a), 2-47(b) and 2-47(c). It is found that the sensing circuit works properly in different loading conditions and in different controller modes.

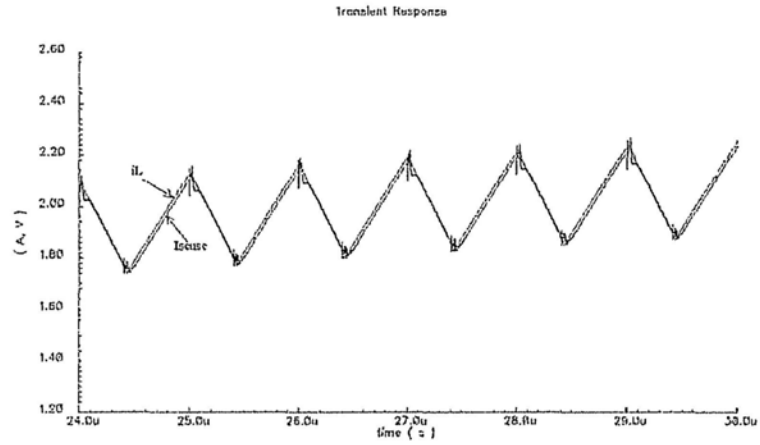



Fig. 2-45 Transient response of the inductor-current sensing circuit.

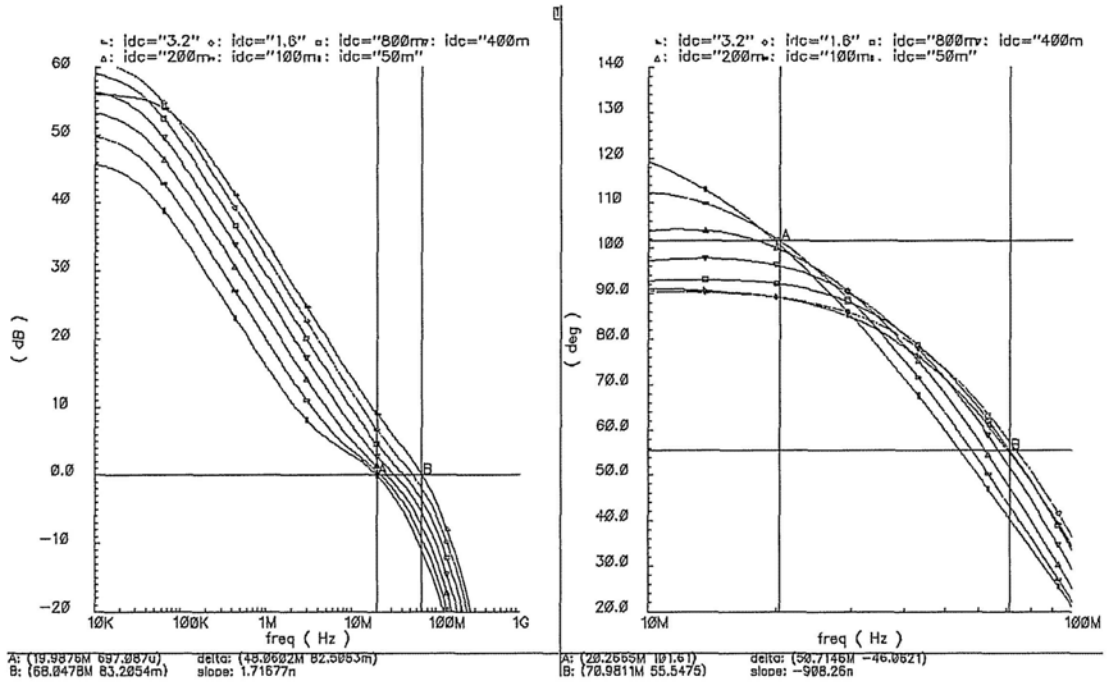



Fig. 2-46 Frequency response of the inductor-current sensing circuit (where $i_{dc}$ = biased inductor current).

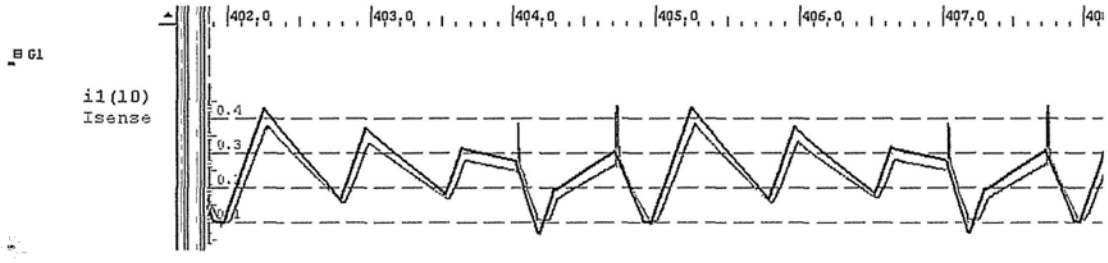



Fig. 2-47(a) Sensed-current waveform @ $I_{o1} = I_{o2} = I_{o3} = I_{o4} = 50\text{mA}$.

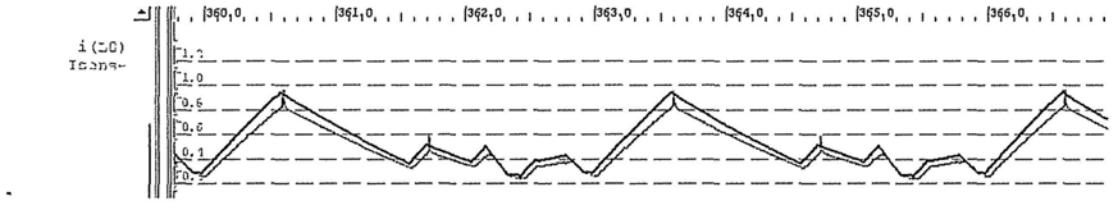


Fig. 2-47(b) Sensed-current waveform @ $I_{o1} = 200\text{mA}$, $I_{o2} = I_{o4} = 50\text{mA}$ and $I_{o3} = 20\text{mA}$.

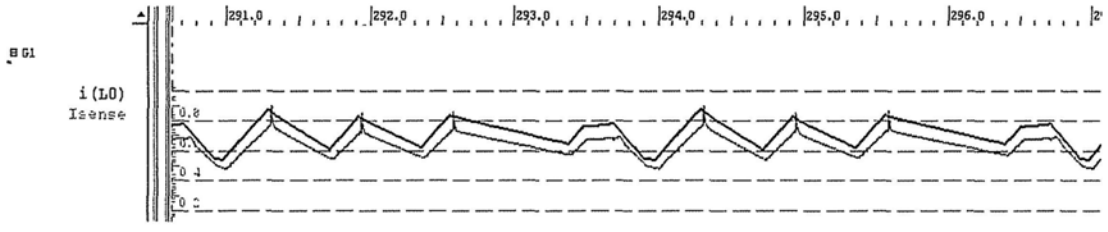



Fig. 2-47(c) Sensed-current waveform @ $I_{o1} = I_{o2} = I_{o4} = 100\text{mA}$ and $I_{o3} = 200\text{mA}$.

The drawback of the proposed inductor-current sensing circuit is the unpredictable sensor ratio due to the mismatches for PMOS_IN and NMOS_IN, which will introduce a different end point as the $I_{sense}$ and $I_{offset}$ crossover. There is a current-sensing circuit design by sensing the current of the output PMOSFET [2]. This design shows better matching from the measurement results due to the same type of transistor. Thus, it is also a potential solution by using this sensing circuit design for the offset inductor-current comparator and using SW_PI current-sensor for the CPM controller.

## 2.6 Start-up and Current Limiting

Similar to a single-output dc-dc converter, the proposed design uses current-limit method to prevent the inductor-current over the maximum rating during start-up or some unexpected conditions such as overloading. Comparing to the well-known soft-start technique such as the method using a slow ramping-up voltage reference, the proposed method gives a faster start-up since it provides maximum power during this start-up period. On the other hand, it is supposed that no converter type information is pre-determined. Permanently using the SW_D cycle to discharge inductor may make a boost converter have long settling time during the start-up or be locked into the NIF mode such that no heavy load can be provided, as shown in Fig. 2-48a). Moreover, start-up may be a frequent action in the operation of a SIMO converter when some of the channels have to be turned on or turned off in on-line operation. Based on all these considerations, the proposed SIMO dc-dc converter uses a current-limiting detection and control logic to prevent the operation mode being locked to the NIF mode. Its operation can be shown in Fig. 2-48(b), and the control logic is shown in Fig. 2-49.

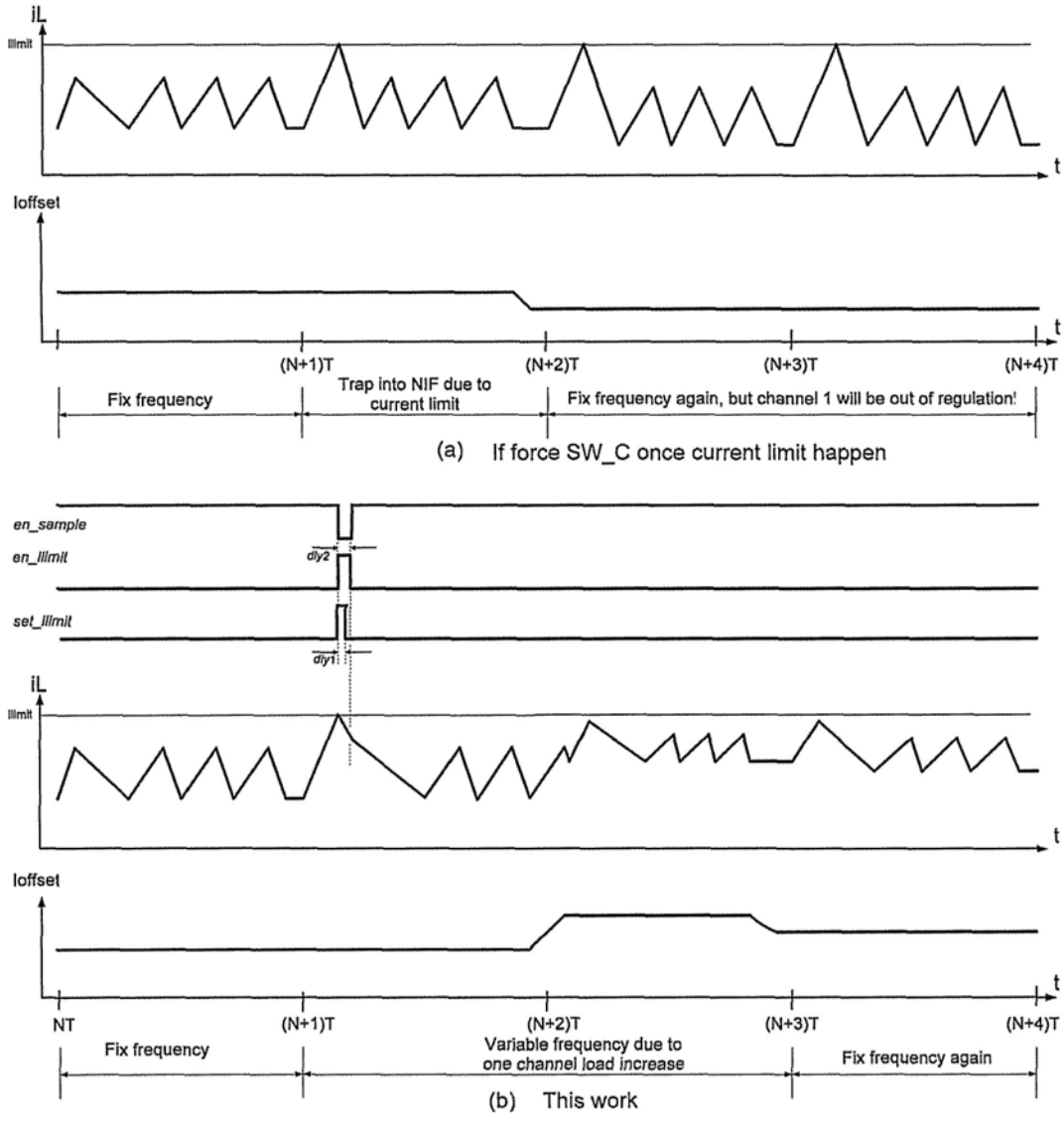



Fig. 2-48 Current limit control waveform.

when $i_L$ > *ilimit*, *set_ilimit* = 1. It is generated by a comparator. *set_ilimit* is sampled and latched, so that *en_ilimit* = 1. The system will unconditionally enter the SW_D period. Provided that the inductor current falls immediately after *en_ilimt* = 1, *dly1* will be the comparator delay. *en_sample* will turn 1 again after a constant delay (i.e. dly2) in order to immunize from the significant noise when inductor current approaches to the current limit. Once *set_ilimit* = 0 and is sampled by *en_ilimit*, the system will go back to the SW_B period again. As a result, no matter it is in start-up period or in the load-transient state, the system will not be mistakenly locked into the NIF mode.

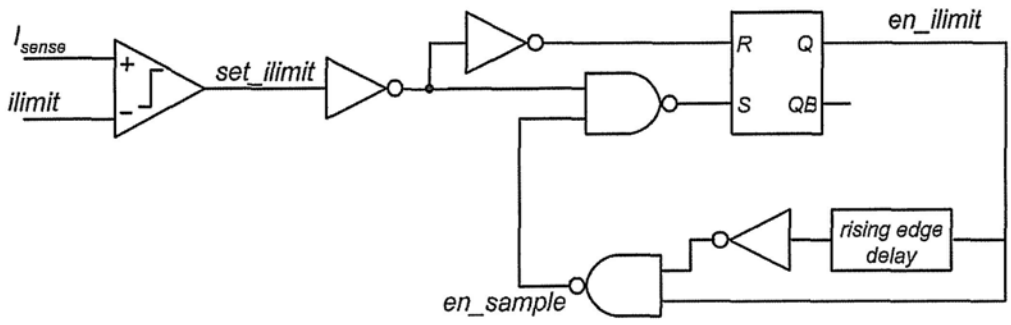



Fig. 2-49 current limit control logic.

Fig. 2-50(a) and 2-50(b) show a simulation of Channel 3 during its start-up when other channels have been operating in the steady state. It is found that the current limit happens and finally recovers to the normal operation after around 200μs. Fig. 2-51 shows a simulation of all channels starting up simultaneously with a loading current of 50mA provided by each channel.

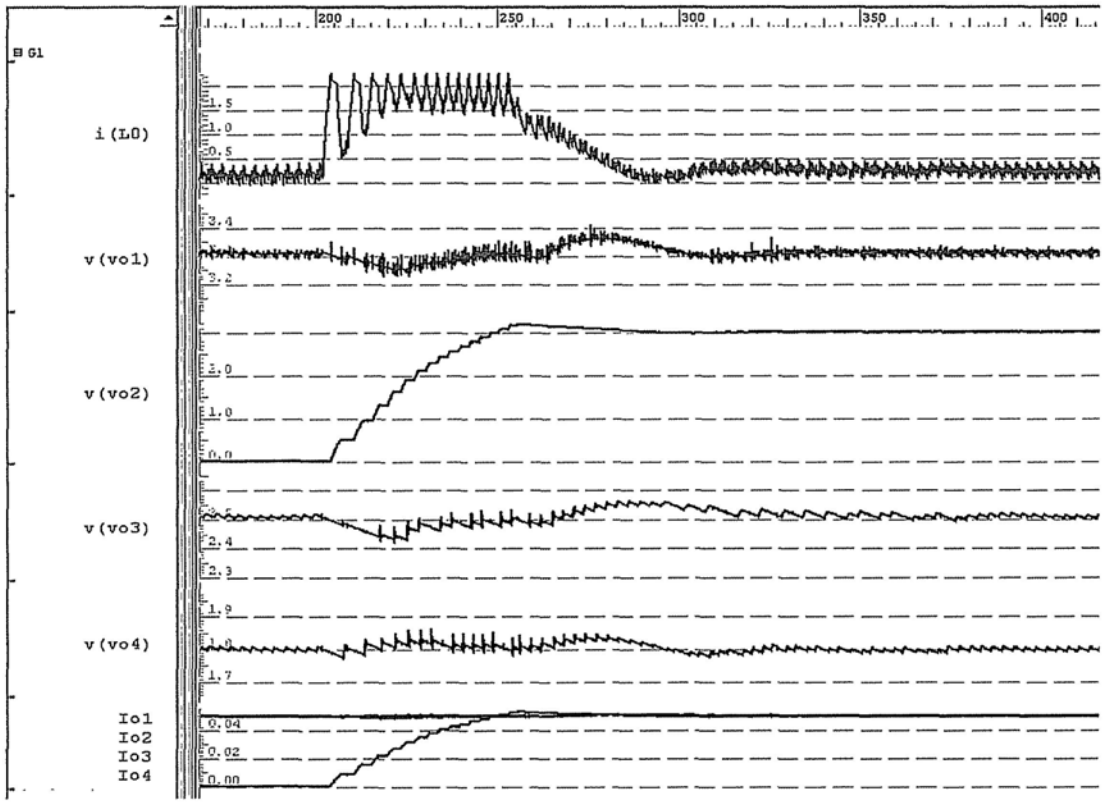



Fig. 2-50(a) Start-up of Channel 3 when other channels are in the steady state.

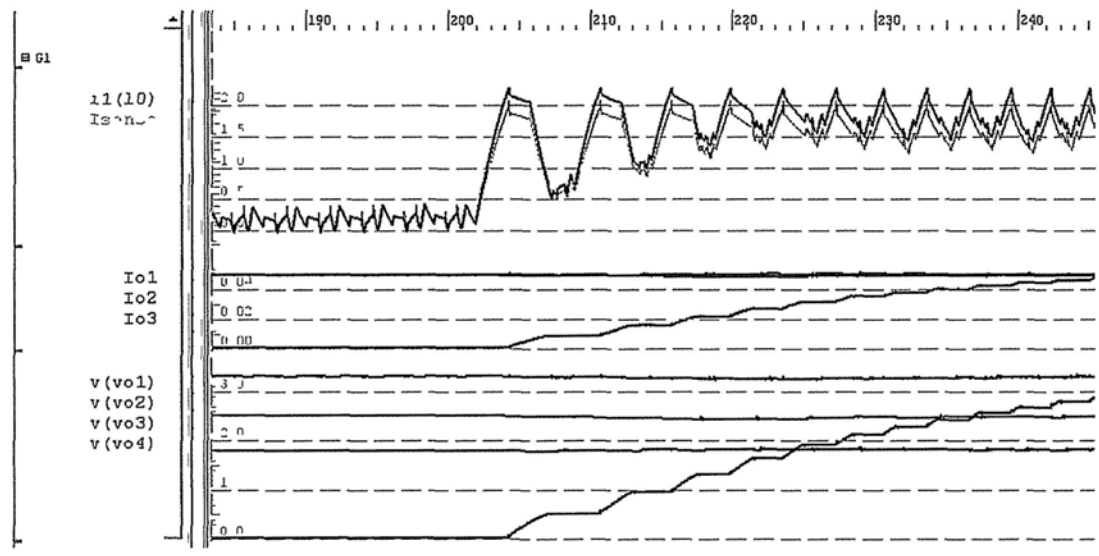



Fig 2-50(b) Zoom-in waveforms of Channel 3 shown in (a).

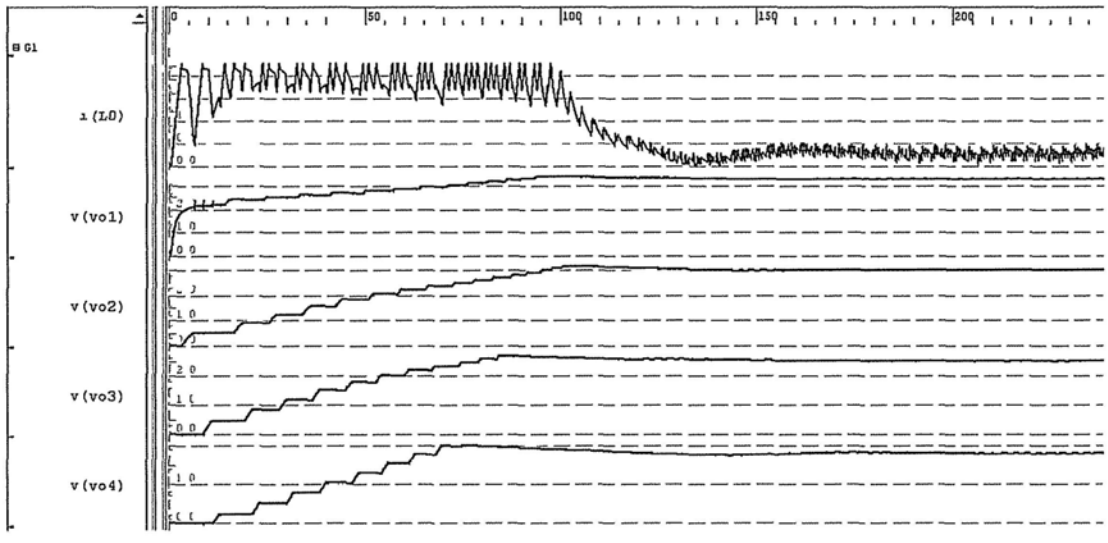



Fig. 2-51 All channels start up simultaneously.

## 2.7 Measurement result

The design presented above has been fabricated in AMS CMOS 0.35-μm 2P4M process. The chip area is 5000μm × 1850μm. The micrograph is shown in Fig. 2-52. The power switches are located on the left of the chip, whereas the control circuit is positioned on the right. In order to reduce routing resistance, all the four layers of metal are used with maximizing the contacts and vias. The multiple pads are used to reduce the effective routing resistance.

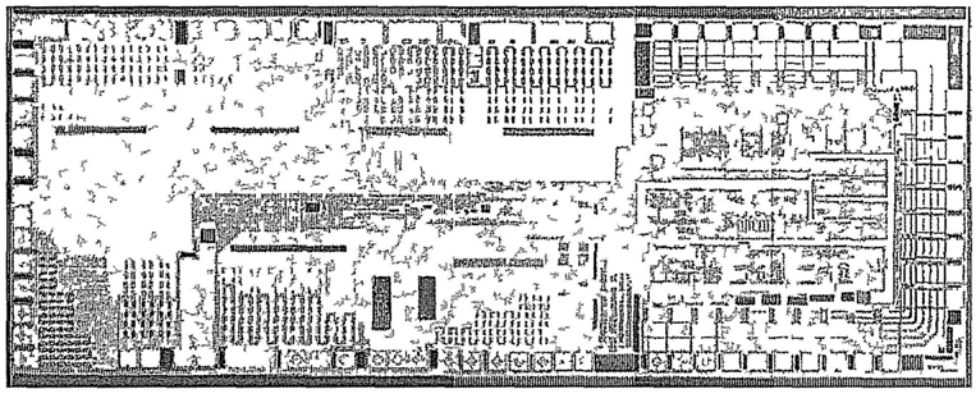


Fig. 2-52 Micrograph of the chip.

The settings of the measurement are shown in Table 2-6. For the measurement presented in this part, the results are based on the parameters listed in the table.

Table 2-6 Measurement setting.

| | |
|---|---|
| Output voltages | $V_{o1}$ = 3.4V, $V_{o2}$ = 3V, $V_{o3}$ = 2.5V, $V_{o4}$ = 1.76V |
| Input voltage (nominal) | 2.5V |
| Inductor and its ESR | 3.3μH and 25mΩ |
| Capacitor and its ESR for each channel | 10μF and 20mΩ |
| Operation frequency | 250kHz |

1. Line regulation with Channel 3 working in different modes shown in Figs. 2-52(a) to 2-52(l) which are measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA, $I_{o4}$ = 53mA.

It is shown that Channel 3 operates in the auto buck-boost mode when $V_g \geq$ 2.56V (i.e. Figs. 2-53(a) to 2-53(e)). When $V_g$ is lower than this value, Channel 3 operates in the deep boost mode. Moreover, when $V_g$ = 2.66V > $V_{o3}$ (i.e Fig. 2-53(d)), It is found that the inductor current has a slope approaching to 0. From this it can find that the lumped resistance due the routings and equivalent on-resistance of the power switches from $V_{o3}$ to $V_g$ is given by $R_p = \frac{Vg - Vo3}{I_L} \approx \frac{2.66 - 2.5}{0.3} \approx 0.5\Omega$, which is the major loss source when operating in the heavy-load condition.

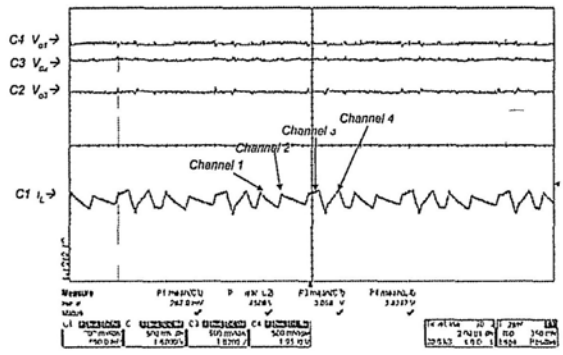



Fig. 2-53(a) $V_g = 2.96$V.

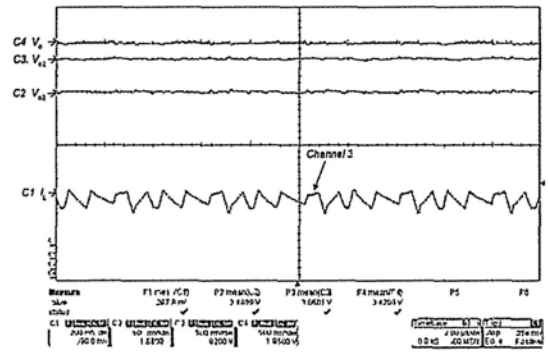



Fig. 2-53(b) $V_g = 2.86$V.

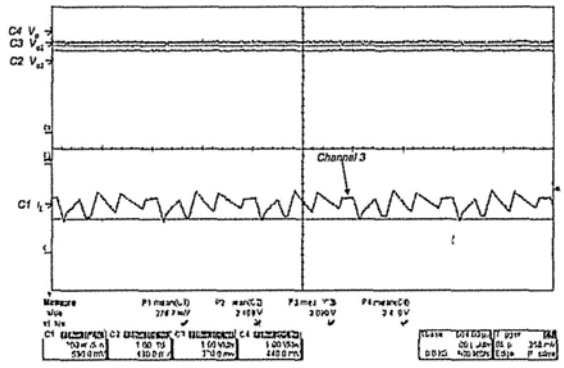



Fig. 2-53(c) $V_g = 2.76$V.

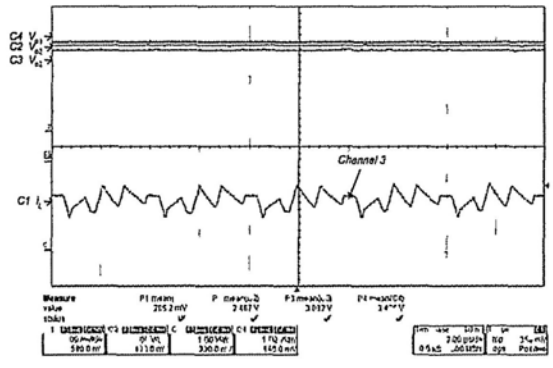



Fig. 2-53(d) $V_g = 2.66$V.

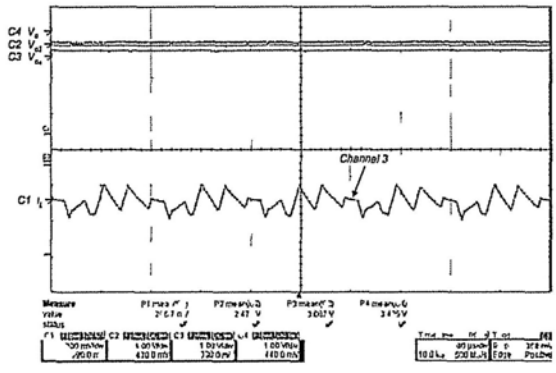



Fig. 2-53(e) $V_g = 2.56$V.

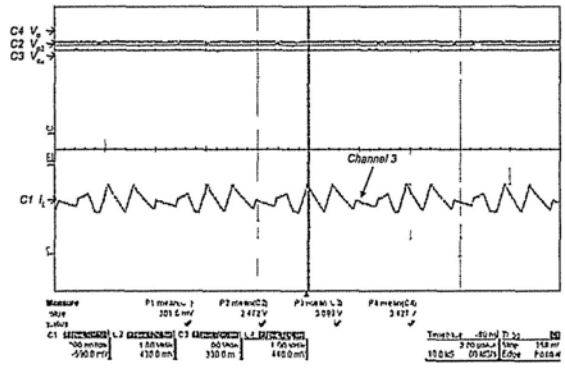



Fig. 2-53(f) $V_g = 2.46$V.

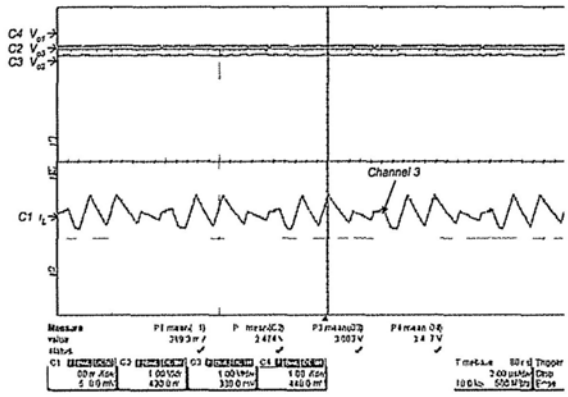



Fig. 2-53(g) $V_g = 2.36$V.

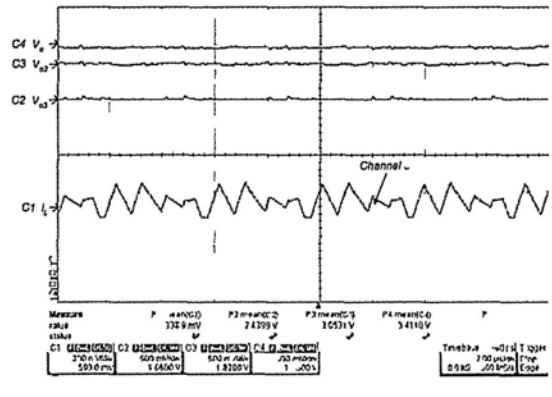



Fig. 2-53(h) $V_g = 2.26$V.

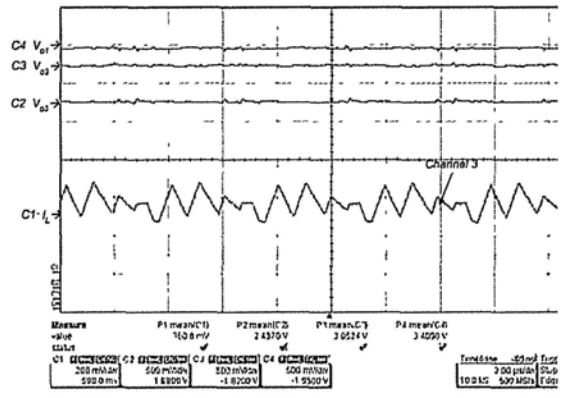



Fig. 2-53(i) $V_g = 2.16$V.

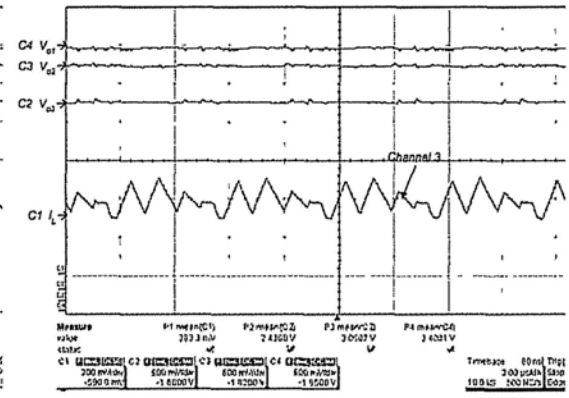



Fig. 2-53(j) $V_g = 2.06$V.

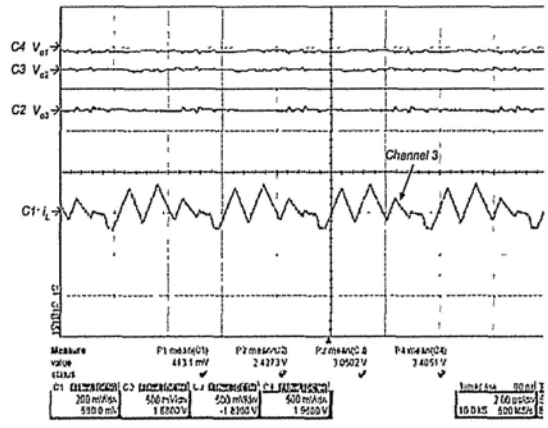



Fig. 2-53(k) $V_g = 1.96$V.

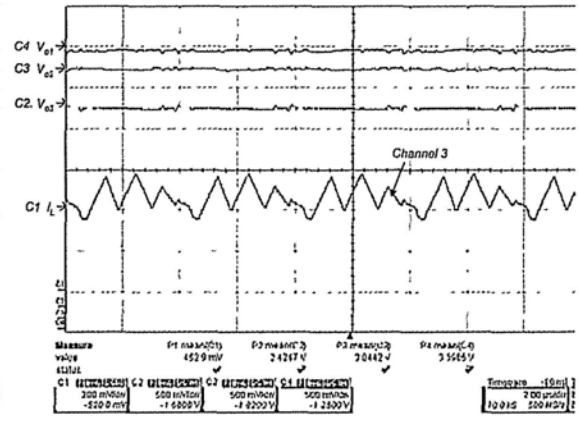



Fig. 2-53(l) $V_g = 1.86$V.

2 Efficiency vs. input voltage (Fig. 2-54) and total output power (Fig. 2-55)

From the above measurements, the relationship between the average inductor current and $V_g$ has been shown. In Fig. 2-54, it shows the efficiency drop due to the higher average inductor current when the dc-dc converter operates from the close-to-buck mode to deep boost mode. Fig. 2-55 shows the conduction loss dominates the power loss of the whole dc-dc converter since the higher output power implies more output current for fixed output voltages. The drop of efficiency is due to the IR drop across the routing resistance and the on-resistance of the power switches. According to peak efficiency measurement condition, it shows that the condution loss corresponding with the routing resistance is around 0.045 W. The

switching loss consumed by the driver is around 0.019W.

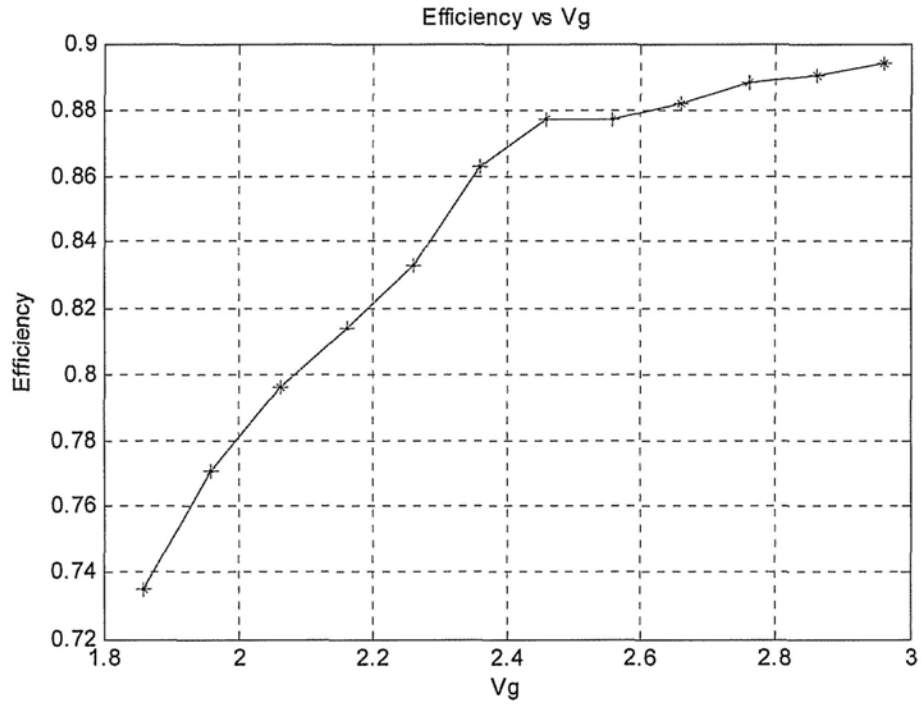



Fig. 2-54 Efficiency for different input voltages
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

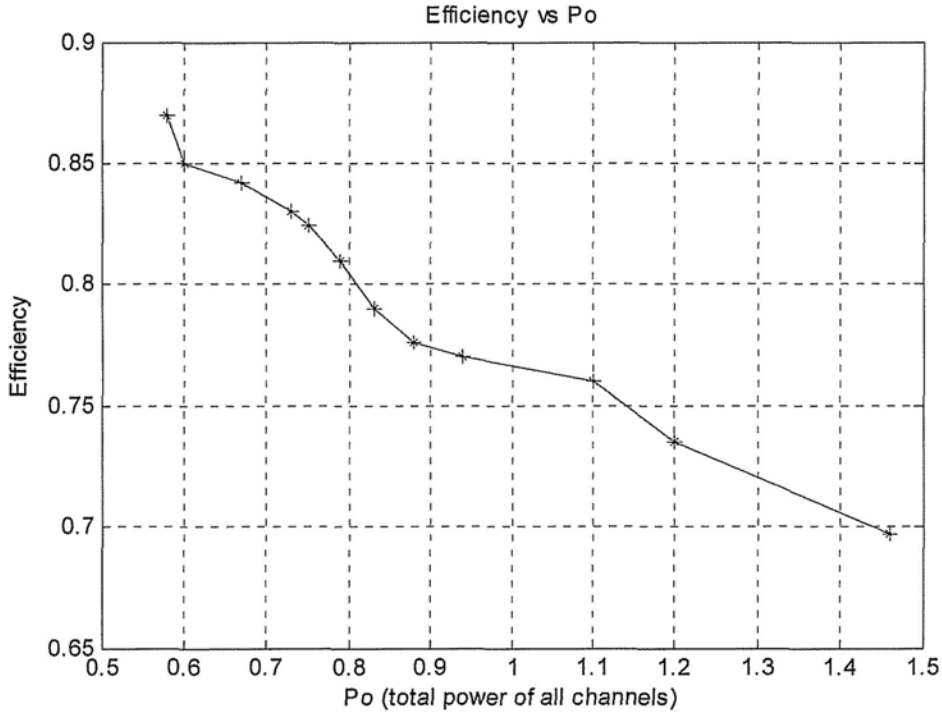



Fig. 2-55 Efficiency for different output powers
(measured at $V_g$ = 2.44V).

3 Loading transient response of different sub-channels (Figs. 2-56 to 2-61).

In the following, a loading-current step is applied to different channels to investigate the load transient response. The transient voltage derivations for different output channels are measured. The magnitudes of the transient voltage derivations are summarized in Table 2-7.

As shown in Fig. 2-56(a), a 50-mA load-current step is applied to Channel 1. $V_{o1}$ has a transient voltage change of 50mV, whereas $V_{o2}$ and $V_{o3}$ have a transient voltage change of 10mV and 20mV, respectively.

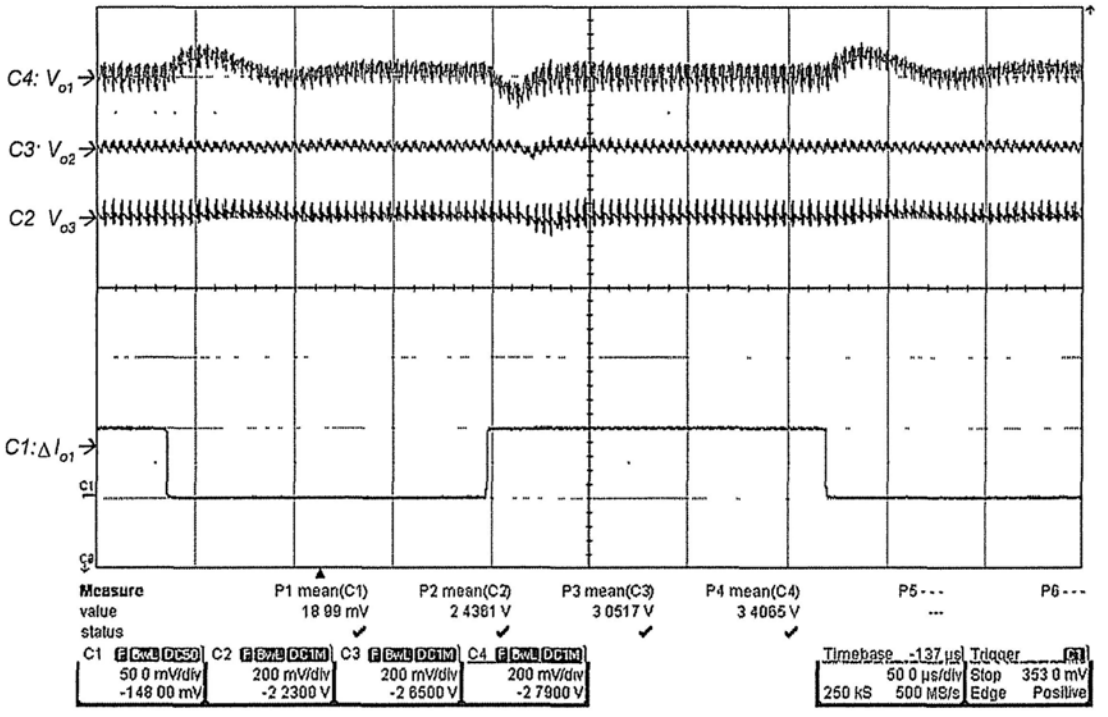



Fig. 2-56(a) $V_{o1}$ undergoing a 50-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

As shown in Fig. 2-56(b), it is found that the offset inductor current is increased and decreased by 50mA in responding to the 50-mA load-current step at Channel 1.

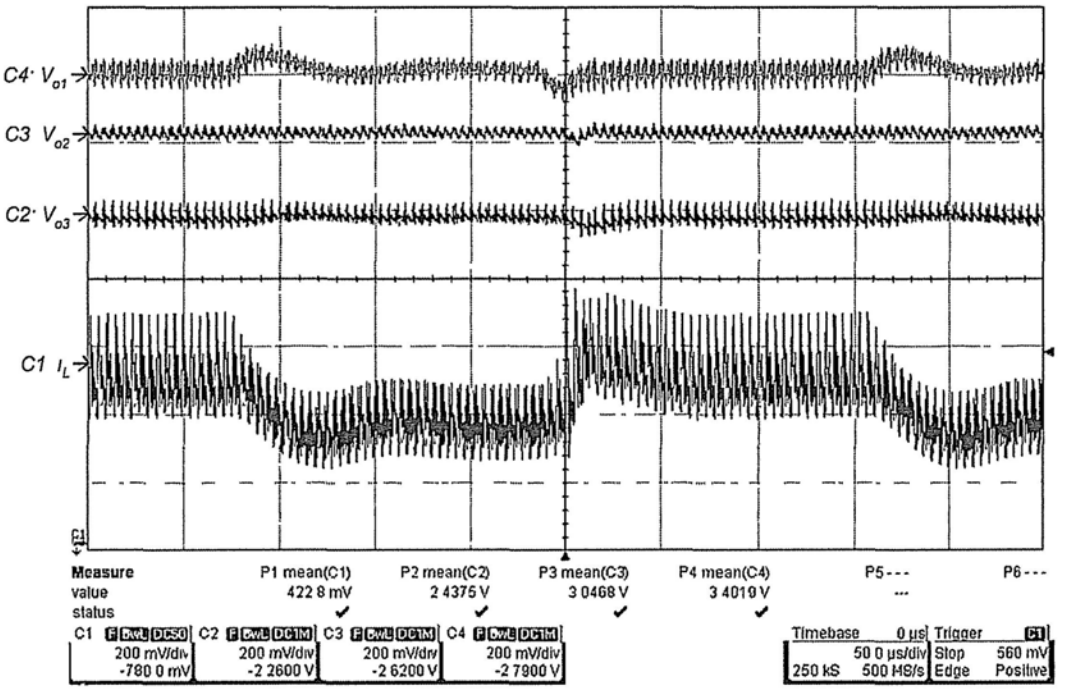



Fig. 2-56(b) Inductor waveform when $V_{o1}$ undergoes a 50-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

As shown in Fig. 2-57, a 70-mA load-current step is applied to Channel 1. $V_{o1}$ has a transient voltage change of 80mV, whereas $V_{o2}$ and $V_{o3}$ have a transient voltage change of 10mV and 40mV, respectively.

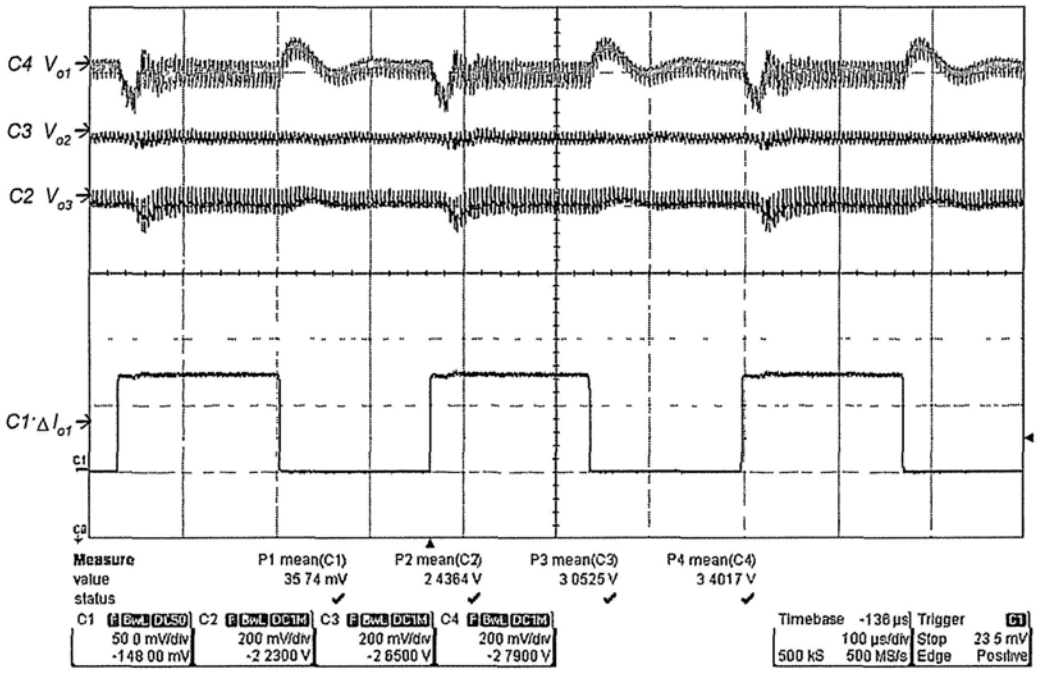



Fig. 2-57 $V_{o1}$ undergoing a 70-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

As shown in Fig. 2-58, a 100-mA load-current step is applied to Channel 1. $V_{o1}$ has a transient voltage change of 140mV, whereas $V_{o3}$ and $V_{o4}$ have a transient voltage change of 40mV and 50mV, respectively.

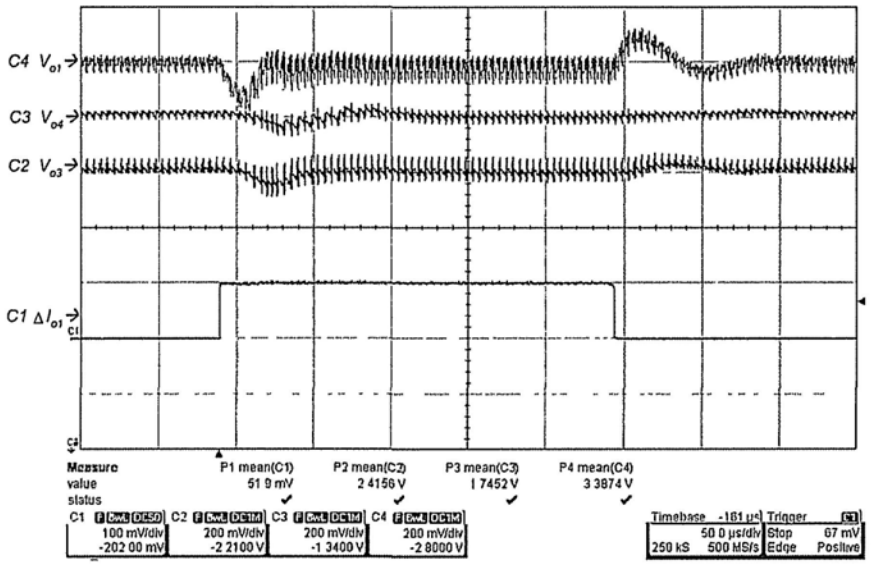



Fig. 2-58 $V_{o1}$ undergoing a 100-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

As shown in Fig. 2-59, a 65-mA load-current step is applied to Channel 2. $V_{o2}$ has a transient voltage change of 50mV, whereas $V_{o1}$ and $V_{o3}$ have a transient voltage change of 10mV and 40mV, respectively.

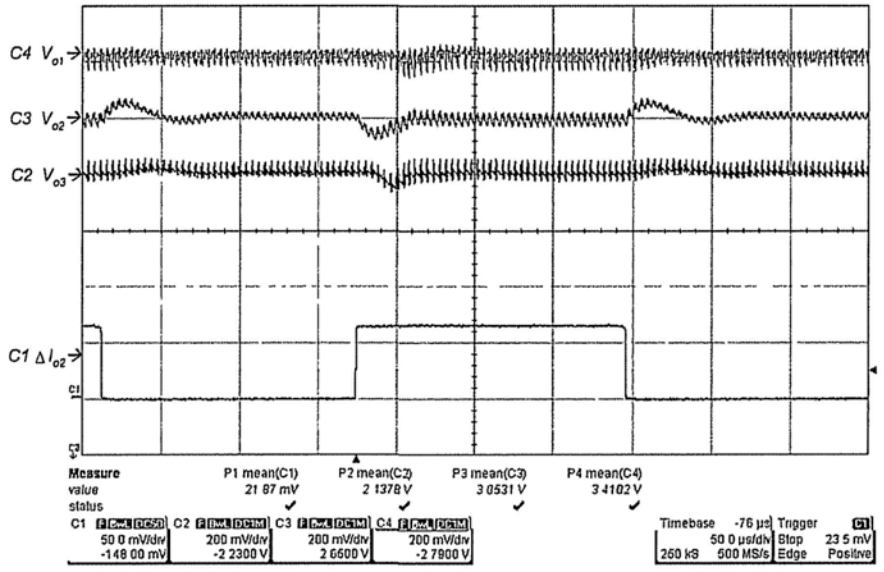



Fig. 2-59 $V_{o2}$ undergoing a 65-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

As shown in Figs. 2-60(a) and 2-60(b), a 120-mA load-current step is applied to Channel 3. $V_{o3}$ has a transient voltage change of 80mV, whereas $V_{o1}$, $V_{o2}$ and $V_{o4}$ have a transient voltage change of 20mV, 10mV and 10mV, respectively.

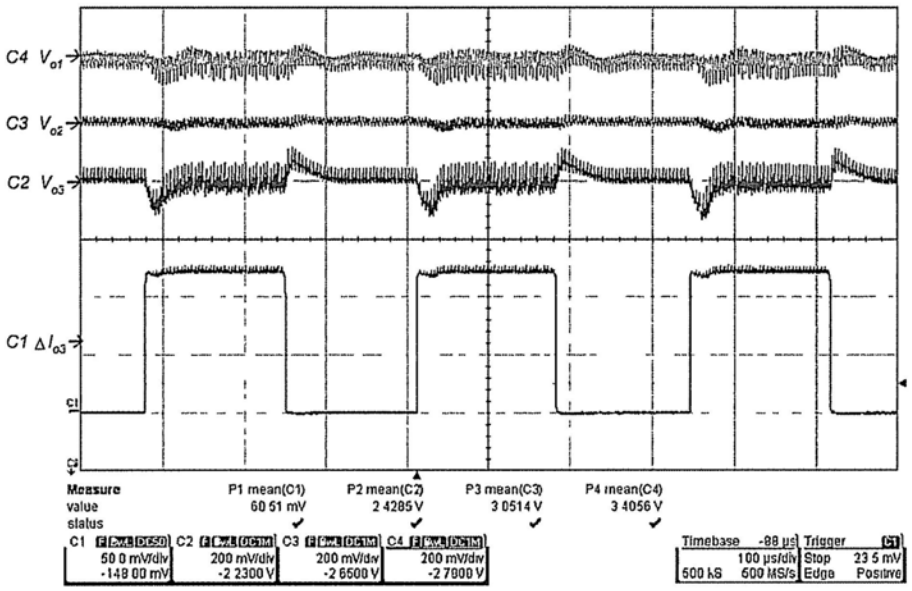



Fig. 2-60(a) $V_{o3}$ undergoing a 120-mA load-current transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

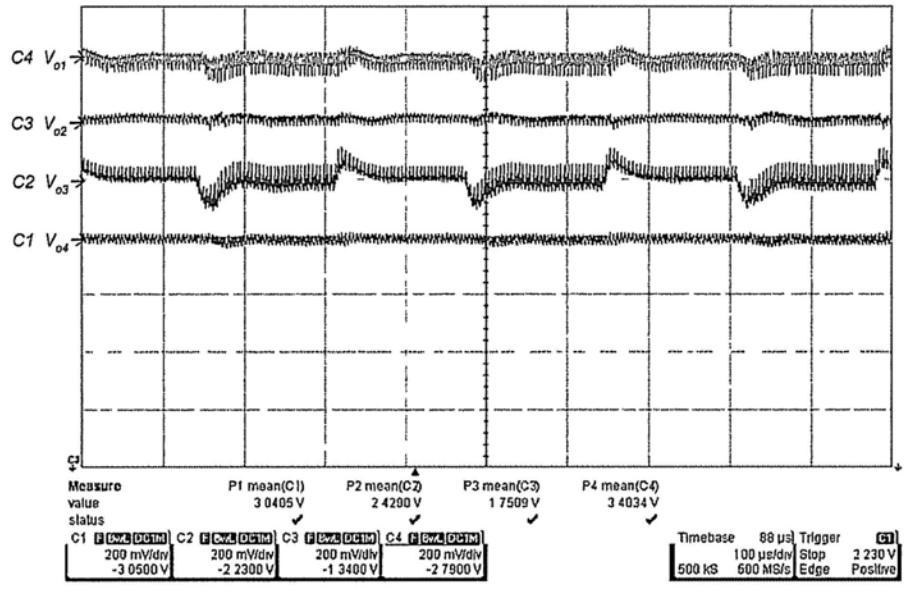



Fig. 2-60(b) $V_{o3}$ undergoing a120-mA load-current transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mAI and $I_{o4}$ = 53mA).

As shown in Fig. 2-61, a 100-mA load-current step is applied to Channel 4. $V_{o4}$ has a transient voltage change of 90mV, whereas $V_{o1}$, and $V_{o3}$ have a transient voltage change of 20mV and 30mV, respectively.

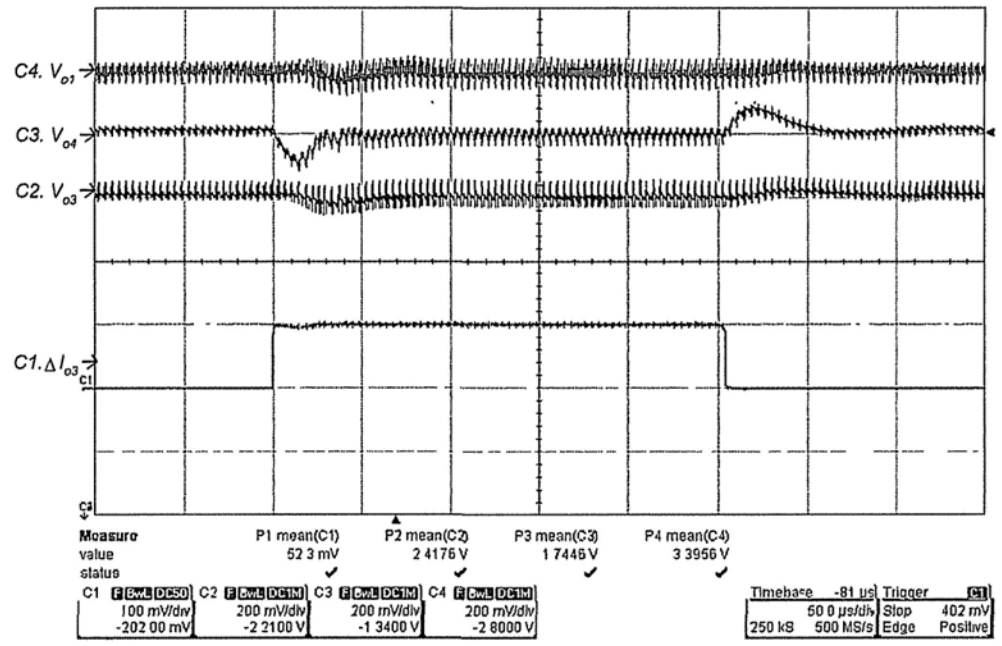



Fig. 2-61 $V_{o4}$ undergoing a 100-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

## 4 Startup

As shown in Fig. 2-62, all channels start up and settle to the preset value within 500µs.

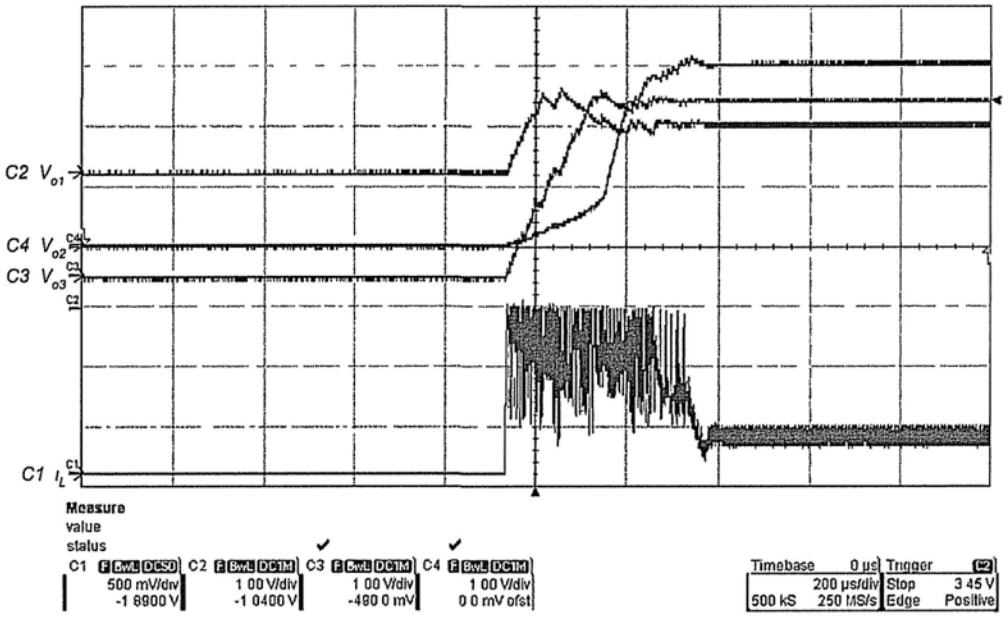



Fig. 2-62 Startup of 4 channels in which Channel 4 is not included
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

5. Steady state waveform (Figs. 2-63 to 2-66)

As shown in Fig. 2-63, the rising edge of the external clock reference (i.e. *lock_clk*) is aligned to the phase end of the last channel. $V_{X1}$ is kept connected to $V_g$ when both the adjacent channels operate as a boost converter.

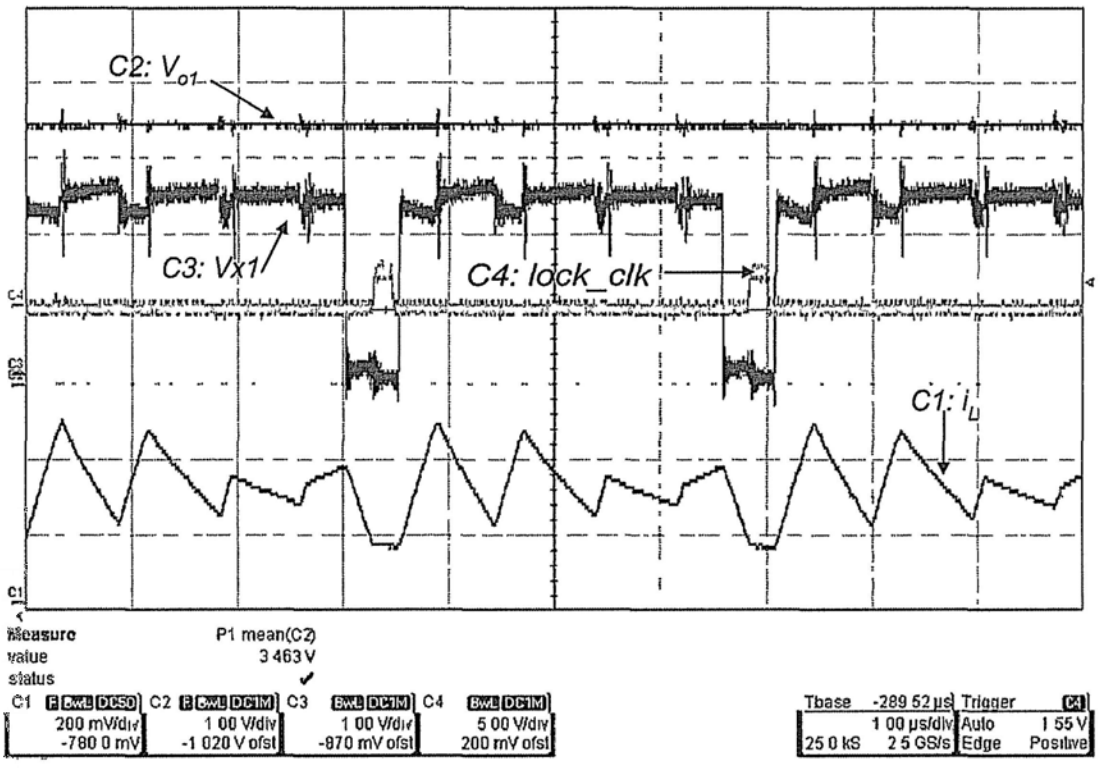



Fig. 2-63 $V_{X1}$ waveform
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

Fig. 2-64 shows that $V_{X2}$ is aligned to the power deliver period of each sub-channel (i.e. the SW_B or SW_D period). Moreover, the proposed two-step buffer makes $V_{X2}$ clamped by the gate voltage of the corresponding output PMOSFET (i.e. SW_PO). As a result, $V_{X2}$ will not be charged to unnecessary high voltage.

As shown in Fig. 2-65, when Channel 3 and Channel 4 are disable, Channel 1 and Channel 2 may deliver higher power comparing to the case when all four channels occupy one switching period.

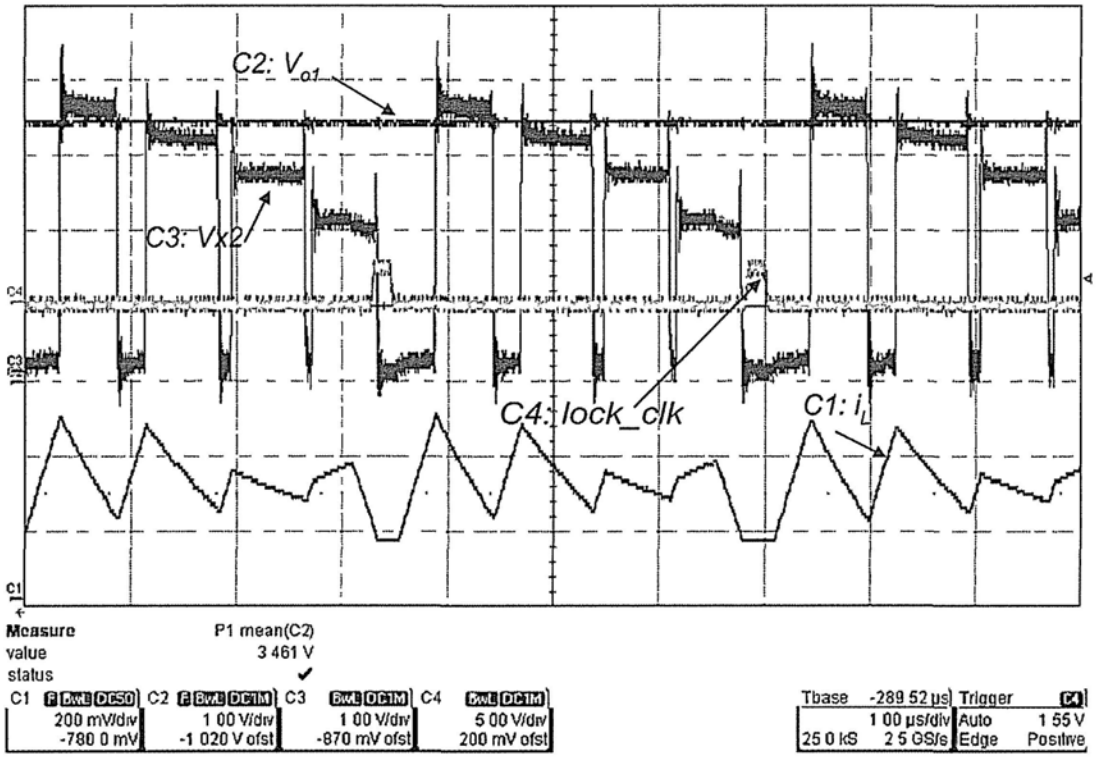



Fig. 2-64 $V_{X2}$ waveform
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

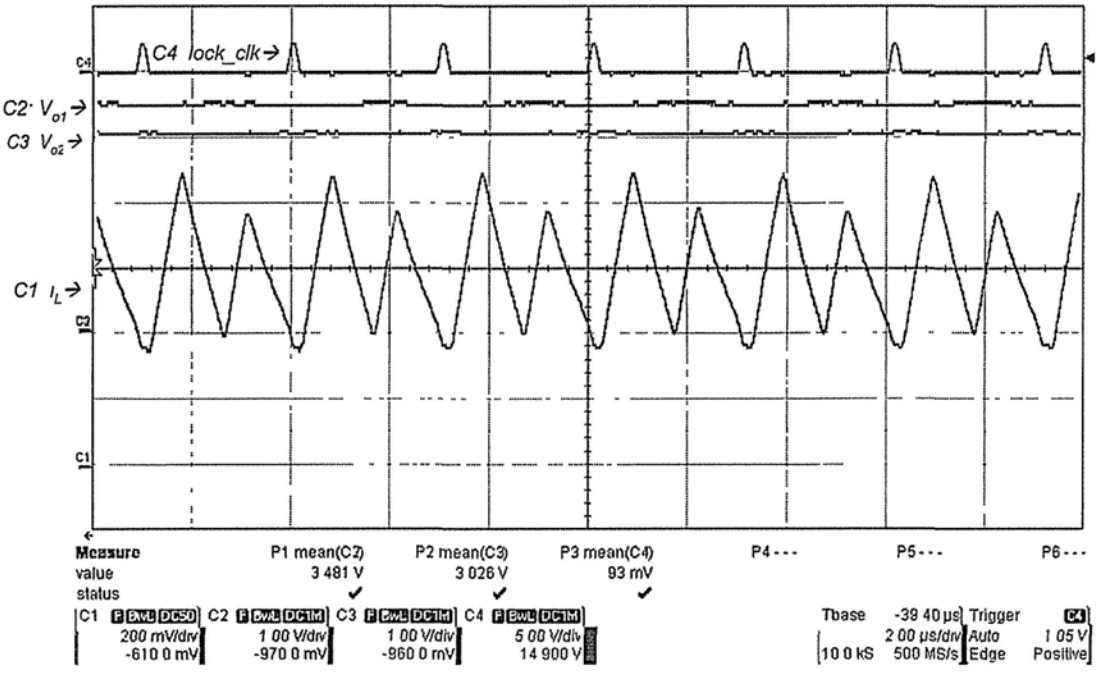



Fig. 2-65 Channels 3 and 4 disabled
(measured at $I_{o1}$ = 120mA and $I_{o2}$ = 160mA).

As shown in Fig. 2-66, when Channel 4 is disabled, the average inductor current is around 1A.

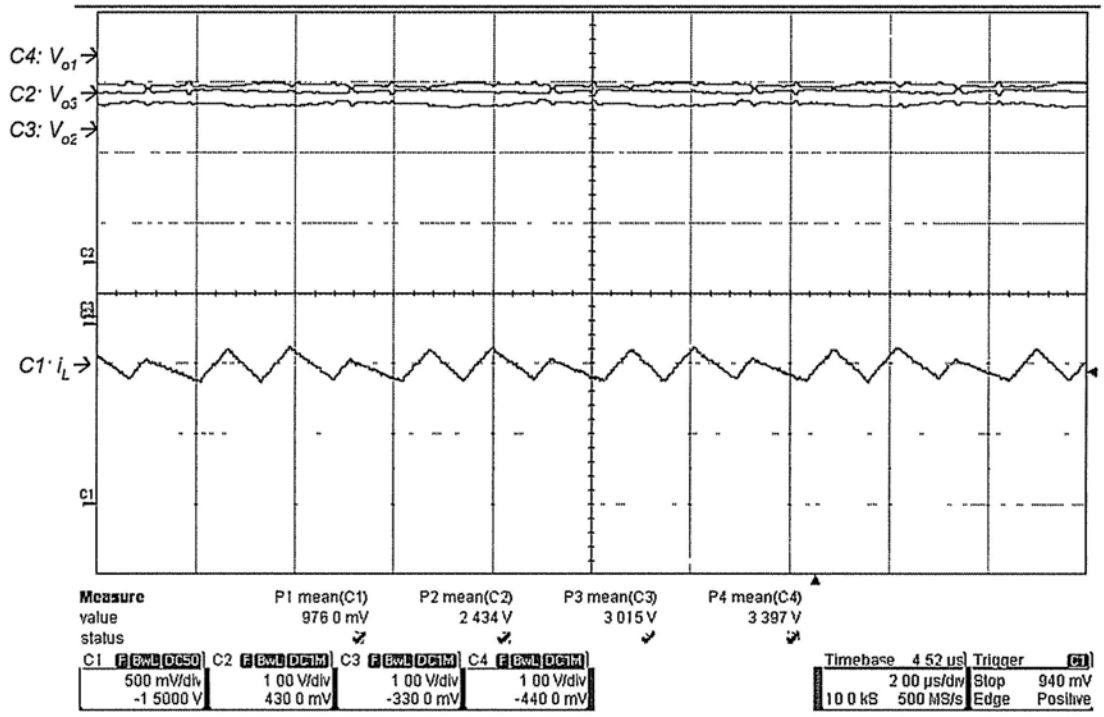



Fig. 2-66 Channel 4 disabled
(measured at $I_{o1}$ = 153mA, $I_{o2}$ = 155mA and $I_{o3}$ = 197mA).

Table 2-7 Measured transient voltage changes ($L_0$ =3.3uH, $C_o$ = 10uF × 4).

| | $V_{o1}$ (mV) | $V_{o2}$ (mV) | $V_{o3}$ (mV) | $V_{o4}$ (mV) |
|---|---|---|---|---|
| 50mA transient @ Channel 1 | 50 | 10 | 20 | N/A |
| 70mA transient @ Channel 1 | 80 | 10 | 40 | N/A |
| 100mA transient @ Channel 1 | 140 | N/A | 40 | 50 |
| 65mA transient @ Channel 2 | 10 | 50 | 40 | N/A |
| 120mA transient @ Channel 3 | 20 | 10 | 80 | 10 |
| 100mA transient @Channel 4 | 20 | N/A | 30 | 90 |

The performance of some recently-reported state-of-art SIMO designs are summarized in Table 2-8. The design in [2] is a SIMO operating in the P-DCM mode. Its output current is limited by the freewheel inductor current and is also dependent on the inductance. The design in [10] is a SIBO operating with freewheel inductor-current feedback. Although it shows fast transient response by combining freewheel inductor-current feedback and comparator-based control for local voltage

regulation, it has problem when applied to multiple channels since the comparator proceeds an instant response which makes the priority of the response of the channel decrease according to its apparent sequence. Moreover, the comparator-based controller has weaker noise immunity and is difficult to achieve small output ripple voltage. The design in [11] is a SIDO operating in DCM and PFM. Although it is control to operate in a frequency with $1/2^n$ of the fundamental frequency, its frequency will decreases when its loading current increases. This is a violation to common PFM application which usually used in light load. As a result, it will induce large voltage ripple in the output. Moreover, the DCM operation makes this converter can only increase its loading ability by selecting a small inductor which also affects the efficiency and induces unnecessary large spikes. The design in [12] uses a state machine to fine-tune the sub-channel period allocation $I_{offset}$ value with discrete values. However, it can be found that its state machine is a nonlinear relationship to the input error signal which means that no matter how large the mismatch of the idle time is sampled, the $I_{offset}$ or sub-channel period will increase one quantized unit. This will saturate the system response and suffer from large load transient. Moreover, the quantization effect in current-mode control is considerable and may affect the trade-offs between the quantization level and the idle time. The design in [13] combines the PLL technique and the comparator-based control. This approach can attenuate cross coupling between channels during the transient by releasing the effect of the sequence of the sub-converter. However, it is a pure buck operation and it is not straightforward when re-design to buck and boost applications since a pure comparator is not sufficient for the voltage regulation loop in the boost converter.

For the design presented in this chapter, it is found that the load transient response time is about 70μs which is similar to a single output DC-DC converter working at the same switching frequency. The design has a good balance between its output power, power efficiency, transient response, sub-channel independency and auto-selection of the converter type by combining the auto buck-boost control technique and the PLL technique. However, the major drawback of the design is too many switching cycles in one period which is also a common property of the dc-dc converter with Class-1 inductor waveform in reported in [3]. As a result, it is difficult to operate at a higher frequency and its channel capacity is quite limited. Therefore, in the next chapter, a new design will be presented to address and solve this design problem.

Table 2-8 Performance comparison.

| | 2003 [2] | 2008 [10] | 2009 [11] | 2010 [12] | 2010 [13] | This work |
|---|---|---|---|---|---|---|
| Type of inductor waveform | Class-1 | Class-2 | Class-1 | Class-1 | Class-2 | Class-1 |
| Channel number | 2 | 2 | 2 | 2 | 6 | 4 |
| Sub-converter type | Boost | Boost (bipolar) | Boost | Boost | Buck | Buck & boost |
| Auto buck-boost | No | No | No | No | No | Yes |
| Switching frequency | 1MHz | 0 8MHz | Not fix (DCM) | 0 5MHz | 2MHz | 0 25MHz |
| IC technology | 0 5μm CMOS | 0 5μm BiCMOS | 0 35μm CMOS | 0 13μm CMOS simulation | 0 35μm CMOS | 0 35μm CMOS |
| Input voltage | 1 25 – 2 25V | 2 7 – 4 5V | 1 8 – 2 4V | 1 5V | 5V | 2 – 3V |
| Output voltages | 2 5V & 3V | -4 8V & 4 8V | 3 – 3 6 | 1 8 & 2 5V | 1V, 1 3V, 1 6V, 1 9V, 2V & 3V | 1 76V, 2 5V, 3V & 3 4V |
| Maximum output power | 0 6W | N/A | N/A | N/A | N/A | 1 46W |
| Peak efficiency | 89 4% | 81%@250mA | 87 8% | N/A | N/A | 89% |
| Transient voltage change and settling time | N/A | 100mV & 25μs @$\Delta I_o$ = 100mA | 500mV & 50us @$\Delta I_o$ = 200mA | 60mV & 50μs @$\Delta I_o$ = 50mA | 75mV & 100μs @$\Delta I_o$ = 71mA | refer to Table 2-7 |

# Conclusion of Chapter

A fixed-frequency SIQO auto buck-boost dc-dc converter with wide input and loading ranges has been introduced in this chapter. The principle of operation of the

proposed dc-dc converter has been given and the performance of the dc-dc converter has been verified by experimental results.

# References


[1] TPS65136 Single-inductor, multiple-output (SIMO) regulator for AMOLED, Texas Instruments.

[2] D. Ma, W. H. Ki, and C. Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1007-1014, Jun. 2003.

[3] T. Li, "Single inductor multiple output boost regulator," *U.S. Patent 6075295*, Jun. 13, 2000.

[4] TPS63000 High efficient single inductor buck-boost converter with 1.8-A switches, Texas Instruments.

[5] LTC3440 Micropower synchronous buck-boost DC/DC converter, Linear Technology.

[6] LTC3401 1A, 3MHz micropower synchronous boost converter, Linear Technology.

[7] K.-S. Seol, Y.-J. Woo, G.-H. Cho, G.-H. Cho, J.-W. Lee and S.-i. Kim, "Multiple-output step-up down switching DC-DC converter with vestigial current control," in *IEEE ISSCC Dig. Tech. Papers*, Feb.2009, pp. 442, 443 & 443a.

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[10] Y.-J. Woo, H.-P. Le, G.-H. Cho, G.-H. Cho and S.-I. Kim, "Load independent control of switching dc-dc converters with freewheeling current feedback," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 446 626.

[11] X. C. Jing, P. K. T. Mok, M. C. Lee, "A wide-load-range single-inductor-dual-output boost regulator with minimized cross-regulation by constant-charge-auto-hopping (CCAH)" in *IEEE Custom Integrated Circuit Conference*, Sep. 2009, pp. 299 302.

[12] Y. Zhang, D. Ma, "Digitally Controlled Integrated Pseudo-CCM SIMO Converter with Adaptive Freewheel Current Modulation," in *IEEE Applied Power Electronics Conference*, Feb. 2010, pp. 284 288.

[13] K.-C. Lee, C.-S. Chae, G.H. Cho and G.-H. Cho, "A PLL-based high-stability single-inductor 6-channel output DC-DC buck converter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 200 201.

# Chapter 3

# A Fixed-Frequency Arbitrary Type Wide Loading Range SIQO DC-DC Converter with Efficient Switching Sequence

## Introduction

The design presented in this chapter is a SIQO dc-dc converter based on the Class-2 inductor-current waveform [1]. As known from the performance comparison made in Chapter 2, the complex operation in each sub-channel in last design makes it difficult to operate at higher frequency and increase the channel capacity. In Fig. 3-1, a simplified (fixed sub-channel type) inductor waveform for a SIMO converter which has boost (Channel 1, 2 and 3) and buck (Channel 4) sub-converters using the proposed control technique in Chapter 2 is shown where $t_1$, $t_2$, $t_3$ and $t_4$ are sub-channel phases (including charging inductor and delivering power to output) for Channel 1, 2, 3 and 4, respectively. It is found that in every period, the power stage switches 8 times. The switching mechanism becomes more when the type of the sub-converters is unknown and when using the auto buck-boost technique presented in last chapter.

In this chapter, it is expected that the inductor-current waveform acts like the one shown in Fig. 3-2. It is found that $t_2$, $t_3$, $t_4$ and $t_5$ are sub-channel power delivering phases for Channel 1, 2, 3 and 4, respectively, whereas $t_1$ is a phase for charging the inductor current to a proper level. The switching times in one period are only 5. If this approach is extended to an $N$-channel converter, the number of switching is $2N$ for the design shown in Fig. 3-1, while $N + 1$ for the one in Fig. 3-2.

It is a very significant switching reduction when the number of sub-converters is needed to increase.

The comparison of the average-inductor current of both approaches is not straightforward. A simple proof will be given later in this chapter and it will show that the Class-2 inductor-current waveform has a potential to become optimal inductor-current waveform in the SIMO design.

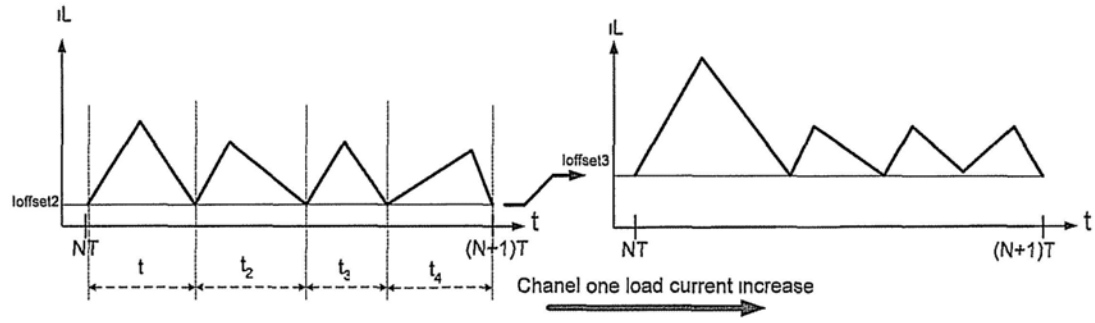



Fig. 3-1 Inductor-current waveform of SIMO with fixed boost and buck sub-channels using the proposed control technique presented in Chapter 2.

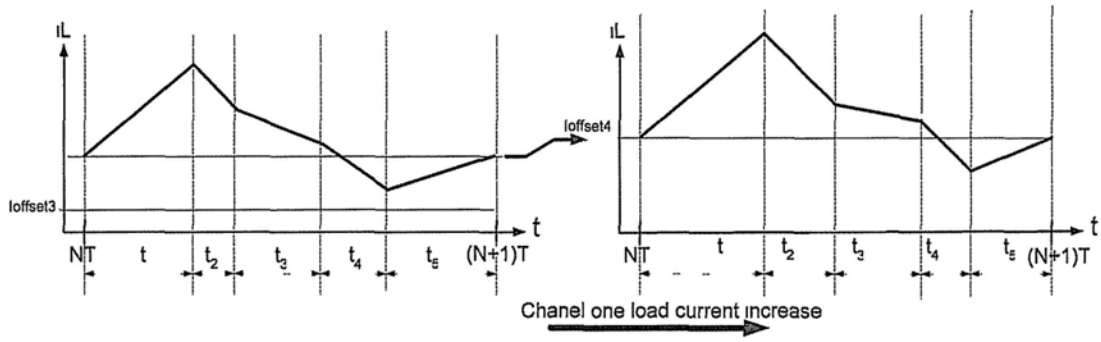



Fig. 3-2 Targeted inductor-current waveform.

Since this design originates from the Class-2 inductor current waveform, which inherent the advantages such as fewer number of switching, total power optimized, higher channel capacity in one switching period, it also will suffer from the disadvantage such as serious cross-regulation effect between different channels. Moreover, the waveform shown in Fig. 3-2 is a boost-dominated SIMO (the concept of boost dominated will be given later). In order to achieve an auto buck-boost dc-dc converter for all channels, a $V_{\lambda 1}$-switching control technique (will be discussed)

should be also involved, so that inductor current acts like the one shown in Fig. 3-3 which is nominated as buck-dominated. In the following, a design will be presented to show how to solve these problems and the ideas will be demonstrated by a SIQO dc-dc converter. The rule of thumb is to make the switching sequence optimal independent of the sequence of the converter type without any hysteretic deduction.

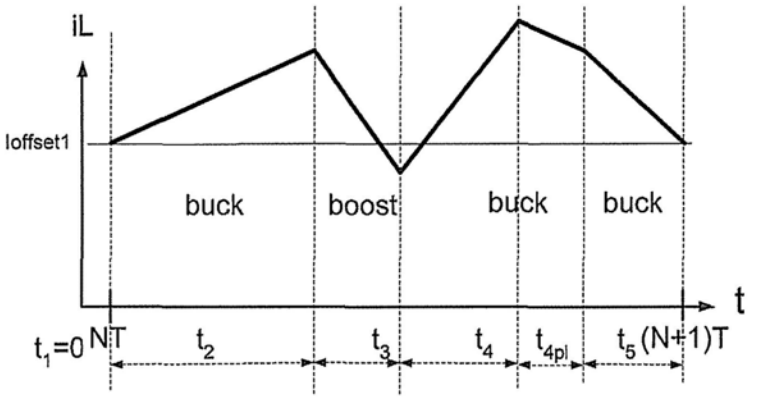



Fig. 3-3 Targeted inductor-current waveform in buck-dominated.

## 3.1 Basic Idea of Optimal Switching Sequence and Concept of Power Efficient Buck-Boost SIMO DC-DC Converter

In Chapter 2, the magnitude of the average inductor current of different converter types (pure buck or boost, NIF and auto buck-boost) has been analyzed and made comparison. It is obvious that the NIF type is the most power-inefficient since its SW_B period is zero. In this section, a similar conclusion will be found when observing the average inductor current with the Class-1 and Class-2 inductor-current waveform of a SIMO converter. It is found that, as shown in Figs. 3-4(a)-(d), both the SW_C and SW_D cycles appear simultaneously, which is similar to the problem of the NIF converter. On the other hand, in Figs. 3-5(a)-(d), it shows either the SW_C cycle or the SW_D cycle appears, which is similar to a single-output boost or buck converter. Since the only dc criterion of a dc-dc converter is Voltage Second Balance (V. S. B.), no matter it is a SISO converter or a SIMO converter, with the same

reason discussed in Chapter 2, the inductor-current waveform in Fig. 3-5 will give a lower average inductor current for the same output power. Fig. 3-4(a) is a two channels (buck and boost) SIMO converter. It is found that when SIMO operating in the Class-1 topology with different output types, intrinsically, its average inductor current is not optimized. In contrast, Fig. 3-5(a) is a dual-channel (dual boost) SIMO converter. Its inductor current operates in the optimal average inductor current mode. It is also true for the dual buck operation.

Define input period $T_g$ and output period $T_o$ as below

$$T_g = \Sigma T_{SW\_C} + \Sigma T_{SW\_B}$$
$$T_o = \Sigma T_{SW\_D} + \Sigma T_{SW\_B}$$

The criterion for the optimal first-order inductor-current operation is

$$T_g = T_s \quad \text{or} \quad T_o = T_s \tag{3-1}$$

$$\text{i.e. } \Sigma T_{SW\_C} \bigcap \Sigma T_{SW\_D} = 0$$

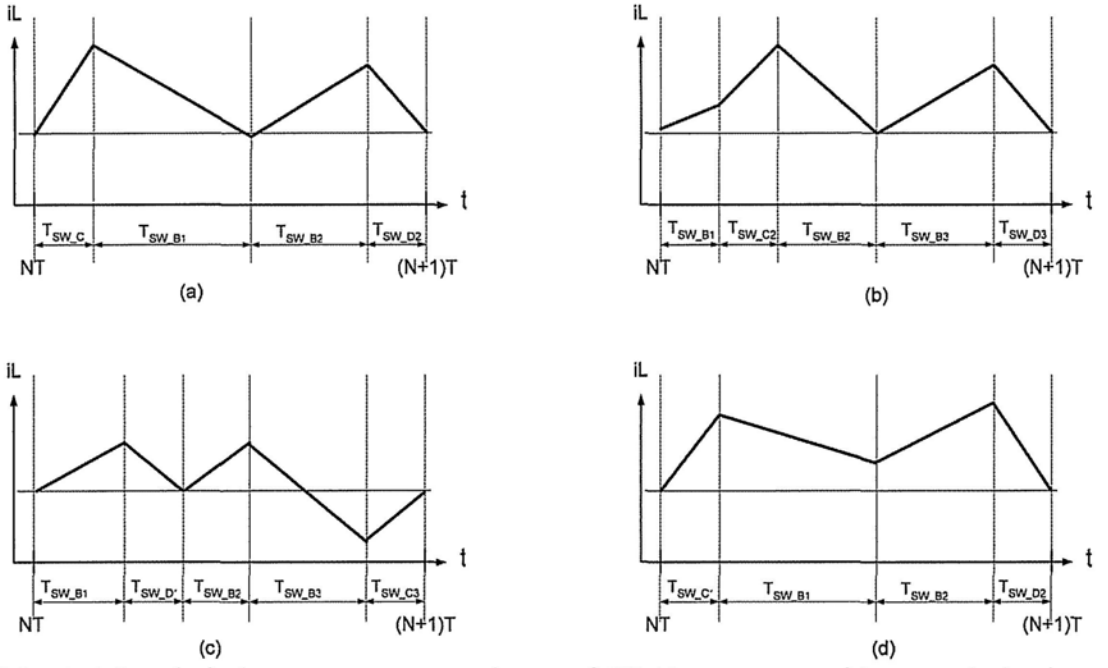


Fig. 3-4 Steady inductor current waveforms of SIMO converter without optimization.

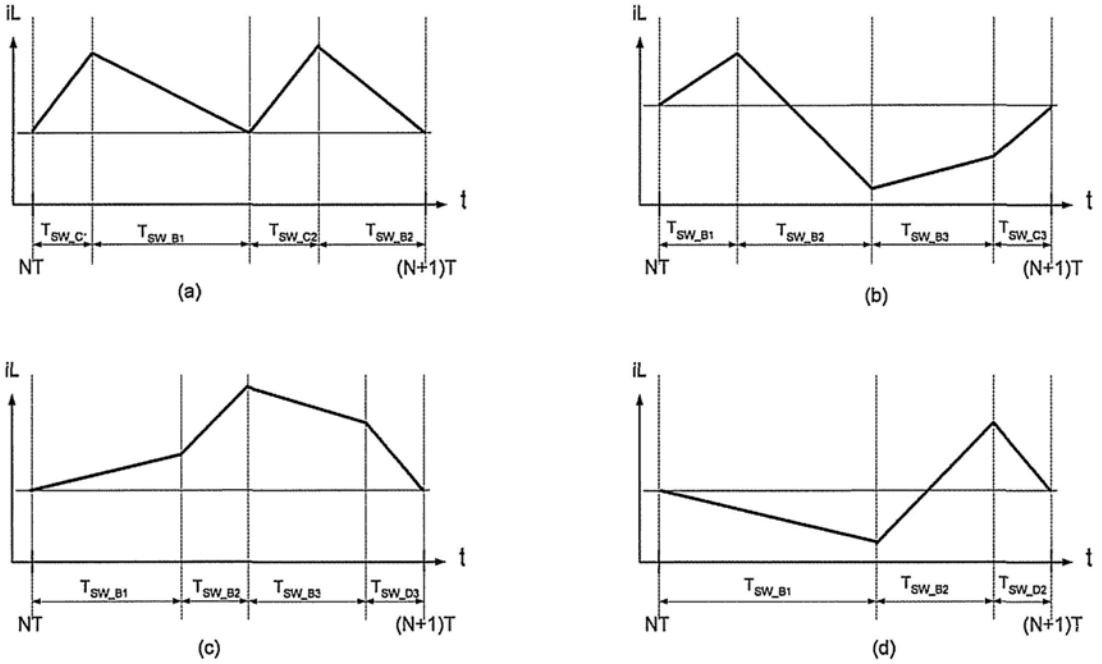



Fig. 3-5 Optimized steady-state inductor-current waveforms of a SIMO converter.

Take a SIDO dc-dc as an example.

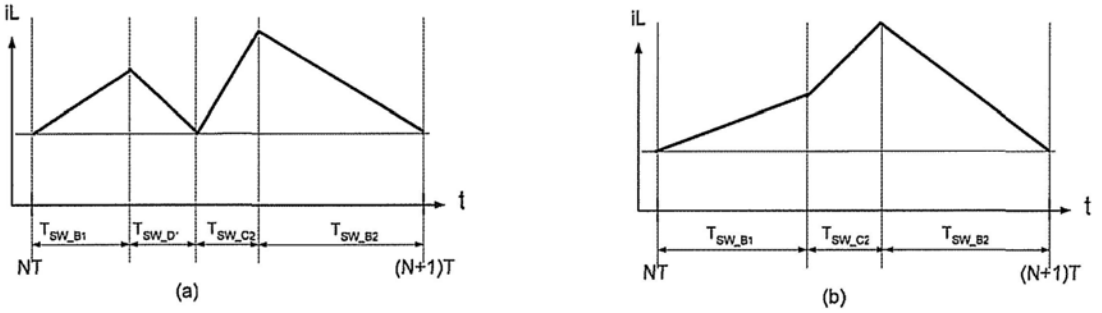



Fig. 3-6 Steady-state inductor-current waveforms of a SIDO with design presented in Chapter 2 and in this chapter.

V. S. B. →

$$\begin{cases} V_g \cdot T_{SW\_B1} = V_{O1}[T_{SW\_B1} + T_{SW\_D1}] \\ V_g[T_{SW\_B2} + T_{SW\_C2}] = V_{O2} \cdot T_{SW\_B1} \\ I_{O1} = I_L(T_{SW\_B1} + T_{SW\_D1})/T_S \\ I_{O2} = I_L \cdot T_{SW\_B2}/T_S = K \cdot I_{O1} \\ T_{SW\_B1} + T_{SW\_D1} + T_{SW\_C2} + T_{SW\_B2} = T_S \\ M_1 = \dfrac{V_{O1}}{V_g} < 1; \quad M_2 = \dfrac{V_{O2}}{V_g} > 1 \end{cases} \tag{3-2}$$

where $K$ is a parameter which indicates the ratio between $I_{o1}$ and $I_{o2}$.

$$I_L = \frac{1 + M_2 \cdot K}{M_1 + M_2 \cdot K}[M_1 + M_2 \cdot K]I_{o1} \tag{3-3}$$

V. S. B. →

$$\begin{cases} V_g[T_{SW\_B1} + T_{SW\_C2} + T_{SW\_B2}] = V_{O1} \cdot T_{SW\_B1} + V_{O2} \cdot T_{SW\_B2}] \\ I_{O1} = I_L \cdot T_{SW\_B1} / T_S \\ I_{O2} = I_L \cdot T_{SW\_B2} / T_S = K \cdot I_{O1} \\ T_{SW\_B1} + T_{SW\_D1} + T_{SW\_C2} + T_{SW\_B2} = T_S \\ M_1 = \frac{V_{O1}}{V_g} < 1; \quad M_2 = \frac{V_{O2}}{V_g} > 1 \end{cases} \tag{3-4}$$

So that

$$\begin{cases} I_{Lopt} = \frac{V_{O1} + V_{O2} \cdot K}{Vg} I_{O1} = [M_1 + M_2 \cdot K]I_{o1} \\ K \geq \frac{1 - M_1}{M_2 - 1} \end{cases} \tag{3-5}$$

$$\eta = \frac{avg[iL]_b}{avg[iL]_a} = \frac{M_1 + M_2 \cdot K}{1 + M_2 \cdot K} + 1 = \frac{M_1 - 1}{1 + M_2 K} + 1 \tag{3-6}$$

Make

$$K = \frac{1 - M_1}{M_2 - 1} \tag{3-7}$$

which maximizes $\eta$, and then

$$\eta = 1 - \frac{1}{\frac{1}{1 - M_1} + \frac{1}{M_2 - 1} + 1} \tag{3-8}$$

From (3-8), it is found that when $M_2 \rightarrow \infty$ (i.e. $V_{o2}$ is in deep boost) and M1 → 0 (i.e. $V_{o1}$ is in deep buck, $\eta \rightarrow 50\%$. This is the theoretical maximum difference between the Class-1 and the optimal Class-2 SIMO dc-dc converter. In other words, the advantage in the average inductor current when using the Class-2 SIMO topology will be obvious when one channel is in deep boost and another channel is in deep

buck. Moreover, the loading current of these channels are approximately satisfied with (3-7). Some more practical values based on (3-8) are shown in Table 3-1.

Table 3-1 Average inductor current difference with and without optimization.

| $V_g$ | $V_{o1}$ | $V_{o2}$ | $M_1$ | $M_2$ | $\eta$ |
|---|---|---|---|---|---|
| 2.5 | 1.8 | 3.3 | 0.72 | 1.32 | 87% |
| 2.5 | 1.2 | 5 | 0.48 | 2 | 75% |

Moreover, when

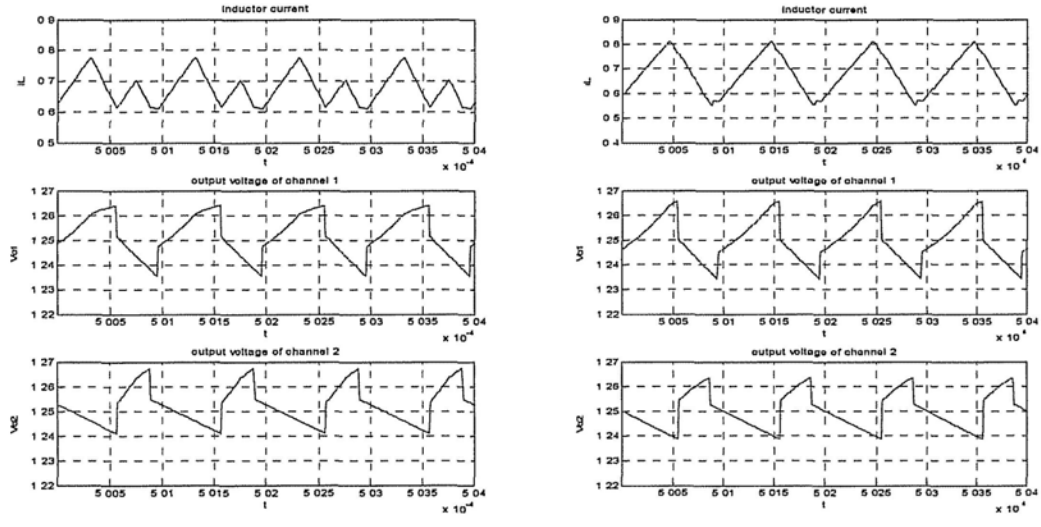
$$T_{SW\_C} = 0 \quad \text{and} \quad T_{SW\_D} \neq 0 \tag{3-9a}$$

As shown in Fig. 3-5(c) and 3-5(d), it is called as the buck-dominated SIMO converter. When

$$T_{SW\_D} = 0 \quad \text{and} \quad T_{SW\_C} \neq 0 \tag{3-9b}$$

As shown in Fig. 3-5(a) and (b), it is called as the boost-dominated SIMO converter. In the following, some simulation results between two types of SIMO converter implemented as the one in Chapter 2 and the design in this chapter are shown below.

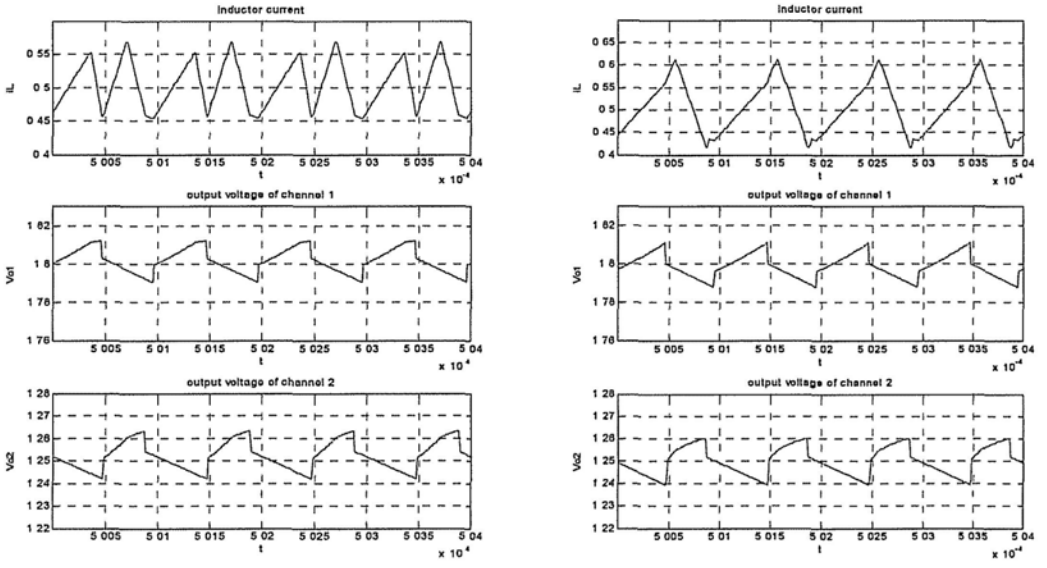
Simulation 1




(a) (b)

Fig. 3-7 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1}$ = 1.25V, $V_{o2}$ = 1.25V, $V_g$ = 2.5V, $I_{o1}$ = 416mA, $I_{o2}$ = 210mA.

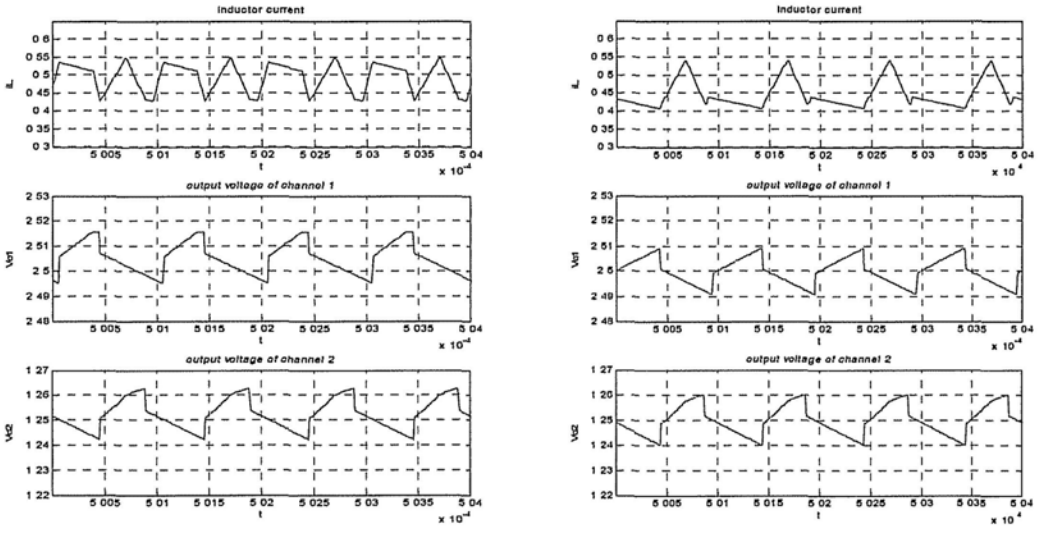
Simulation 2




(a) (b)

Fig. 3-8 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1} = 1.8$V, $V_{o2} = 1.25$V, $V_g = 2.5$V, $I_{o1} = 260$mA, $I_{o2} = 210$mA.

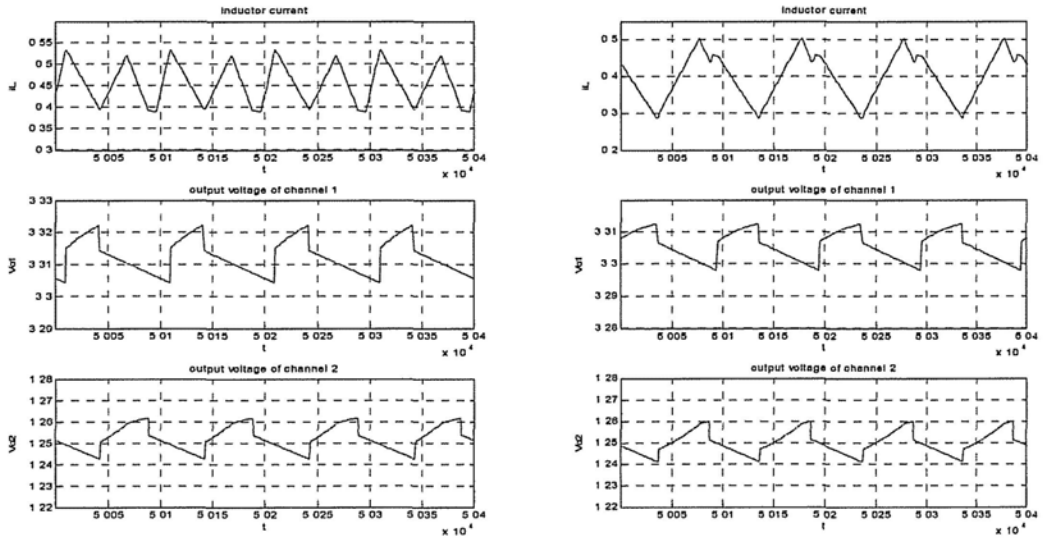
Simulation 3




(a) (b)

Fig. 3-9 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1} = 2.5$V, $V_{o2} = 1.25$V, $V_g = 2.5$V, $I_{o1} = 200$mA, $I_{o2} = 210$mA.

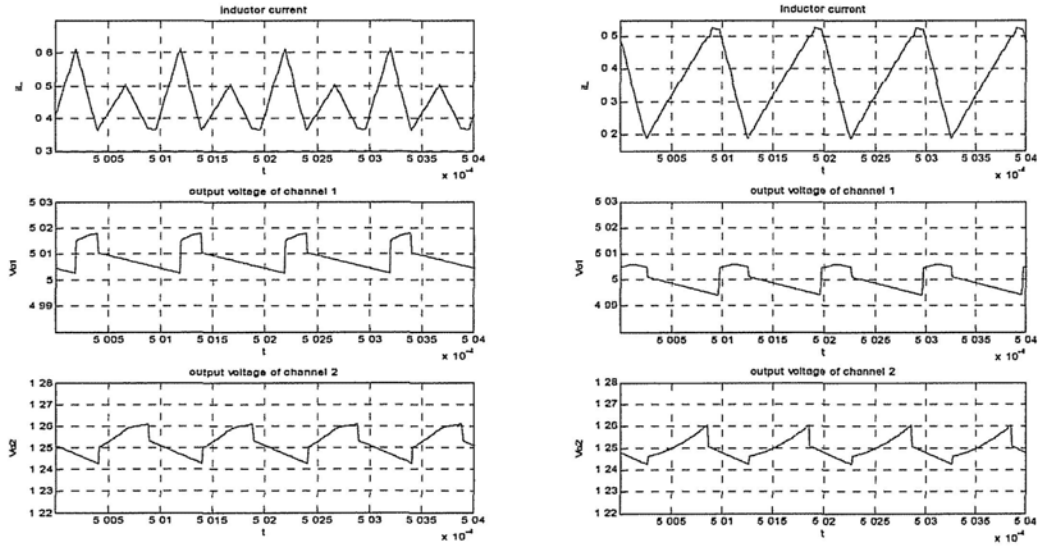
Simulation 4




(a) (b)

Fig. 3-10 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1} = 3.3\text{V}$, $V_{o2} = 1.25\text{V}$, $V_g = 2.5\text{V}$, $I_{o1} = 150\text{mA}$, $I_{o2} = 210\text{mA}$.

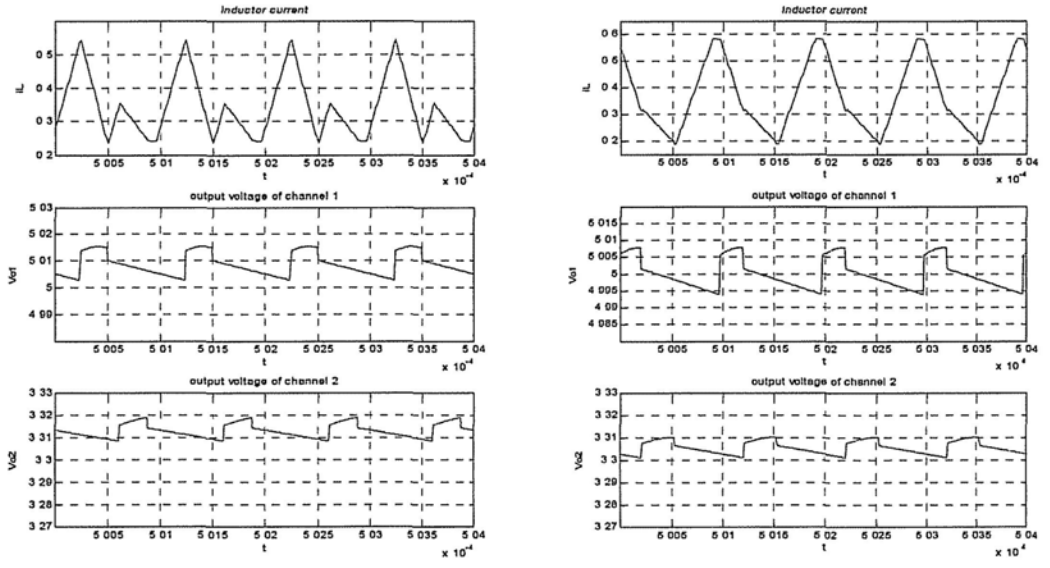
Simulation 5




(a) (b)

Fig. 3-11 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1} = 5\text{V}$, $V_{o2} = 1.25\text{V}$, $V_g = 2.5\text{V}$, $I_{o1} = 100\text{mA}$, $I_{o2} = 210\text{mA}$.

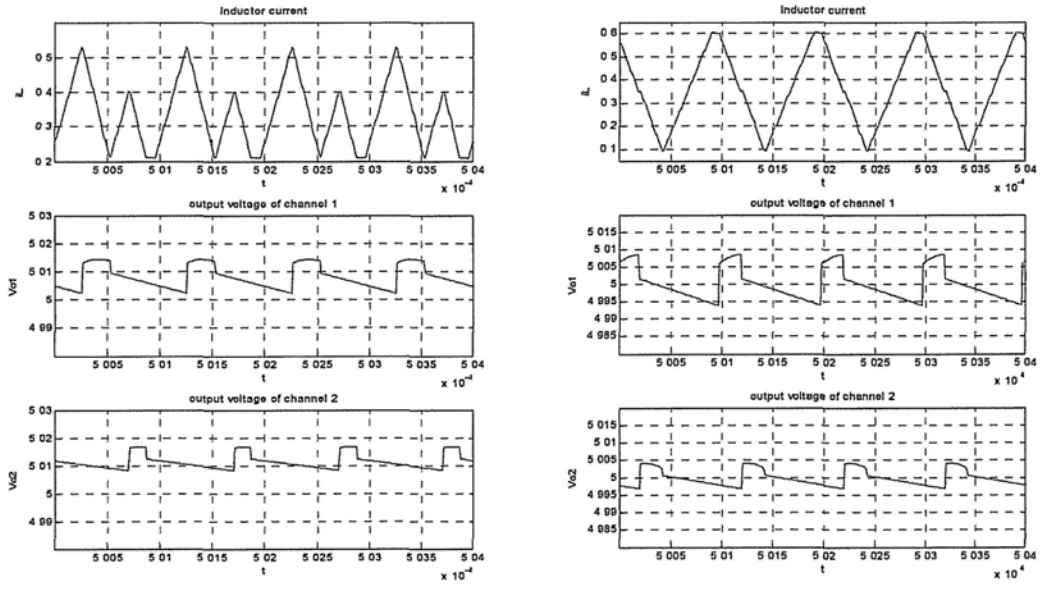
Simulation 6




(a) (b)

Fig. 3-12 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1}$ = 5V, $V_{o2}$ = 3.3V, $V_g$ = 2.5V, $I_{o1}$ = 100mA, $I_{o2}$ = 80mA.

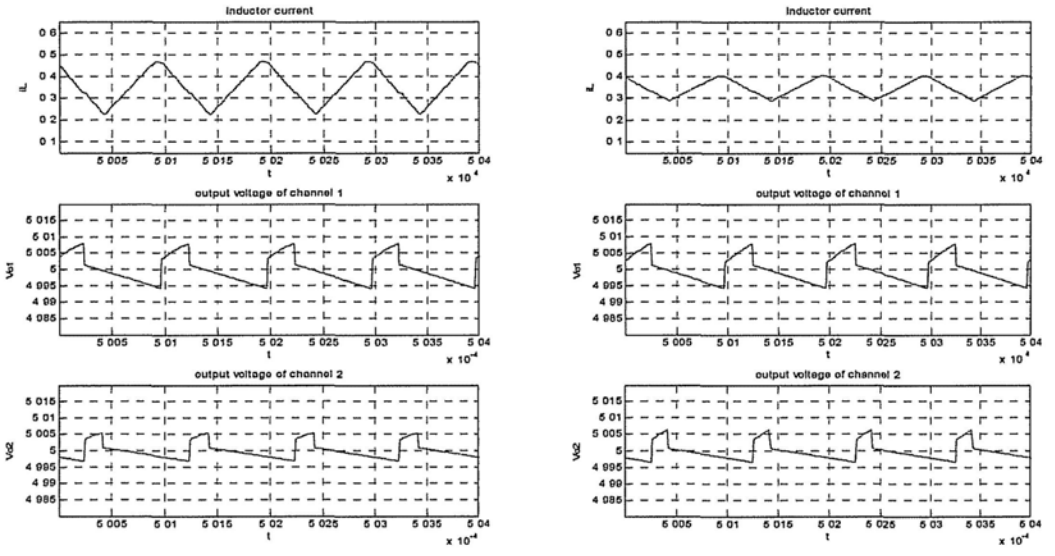
Simulation 7




(a) (b)

Fig. 3-13 Class-1 vs. Class-2 SIMO for dual outputs, when $V_{o1}$ = 5V, $V_{o2}$ = 5V, $V_g$ = 2.5V, $I_{o1}$ = 100mA, $I_{o2}$ = 50mA.

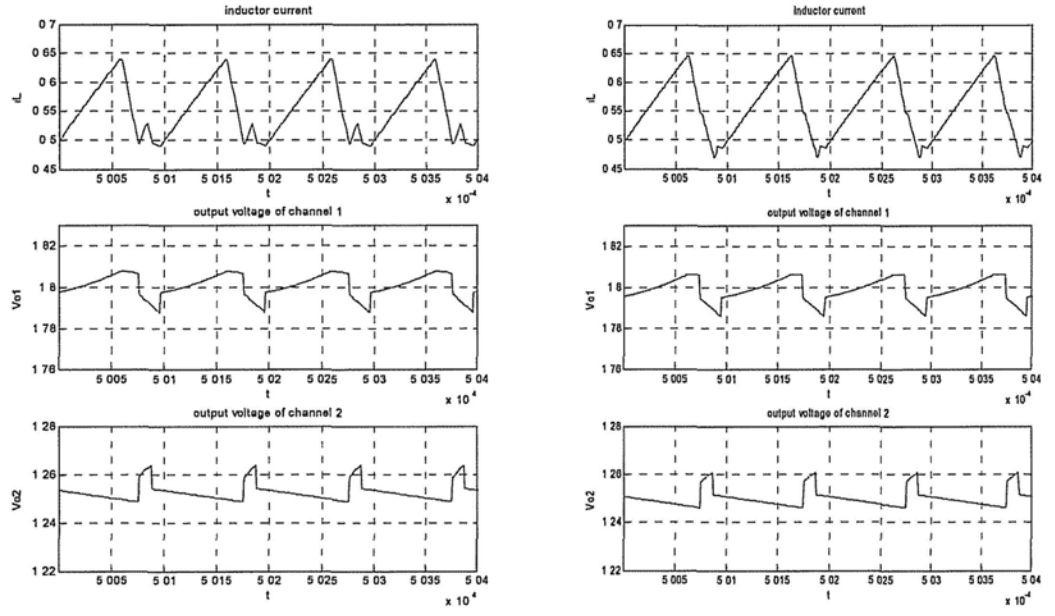
Simulation 8




(a) (b)

Fig. 3-14 Class-2 SIMO for dual outputs, when $V_{o1}$ = 5V, $V_{o2}$ = 5V, $V_g$ = 2.5V, $I_{o1}$ = 100mA, $I_{o2}$ = 50mA with different inductor values.

Simulation 9




(a) (b)

Fig. 3-15 Class-1 vs Class-2 SIMO for dual outputs, when $V_{o1}$ = 1.8V, $V_{o2}$ = 1.25V, $V_g$ = 2.5V, $I_{o1}$ = 450mA, $I_{o2}$ = 64mA.

Simulation 10

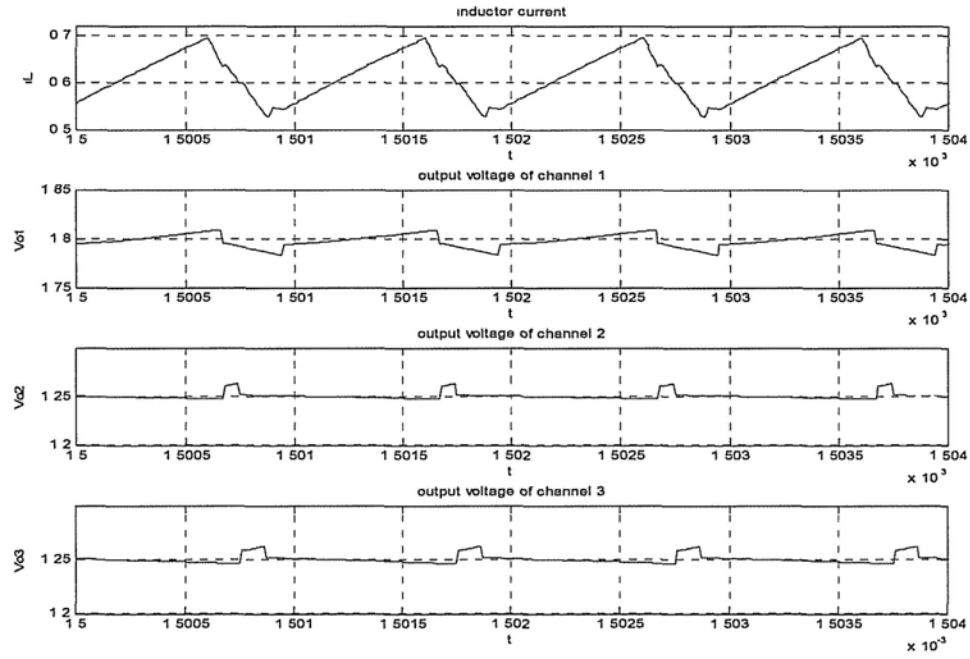



Fig. 3-16 Class-1 vs Class-2 SIMO for triple outputs, when $V_{o1}$ = 1.8V, $V_{o2}$ = 1.25V, $V_{o3}$ = 1.25V, $V_g$ = 2.5V, $I_{o1}$ = 450mA, $I_{o2}$ = 42mA, $I_{o3}$ = 62mA.

The numerical results of the simulations shown in Figs. 3-7 to 3-16 are summarized below. It is noted that Design 1 = the SIMO design in Chapter 2, Design 2 = the SIMO design in this Chapter, $T_s$ = switching period, $T_{\mathrm{MOT}}$ = minimum on-time, $T_{\mathrm{LCK}}$ = locking time and $I_{LA}$ = average inductor current, $P_o$ = total output power. The output capacitor is 10uF with 20mΩ ESR for each channel.

Table 3-2 Simulation $V_g$ = 2.5V, $V_{o1}$ = 1.25V, $V_{o2}$ = 1.25V.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $\mathrm{ESR_L}$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{\mathrm{MOT}}$ (s) | $T_{\mathrm{LCK}}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 1 25 | 1 25 | 2 2μ | 0 3 | 416m | 210m | 1μ | 100n | 70n | 0 78 | 0 68 |
| **Design 2** | | | | | | | | | – | 70n | | 0 68 |

Table 3-3 Simulation $V_g = 2.5V$, $V_{o1} = 1.8V$, $V_{o2} = 1.25V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 1 8 | 1 25 | 2 2μ | 0 3 | 260m | 210m | 1μ | 100n | 70n | 0 73 | 0 50 |
| **Design 2** | | | | | | | | | – | 70n | | 0 51 |
| **Design 1** | | | | | | 450m | 64m | 1μ | 50n | 70n | 0 89 | 0 55 |
| **Design 2** | | | | | | | | | – | 70n | | 0 56 |

Table 3-4 Simulation $V_g = 2.5V$, $V_{o1} = 2.5V$, $V_{o2} = 1.25V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 2 5 | 1 25 | 2 2μ | 0 3 | 200m | 210m | 1μ | 100n | 70n | 0 76 | 0 49 |
| **Design 2** | | | | | | | | | – | 70n | | 0 45 |

Table 3-5 Simulation $V_g = 2.5V$, $V_{o1} = 3.3V$, $V_{o2} = 1.25V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 3 3 | 1 25 | 2 2μ | 0 3 | 150m | 210m | 1μ | 100n | 70n | 0 76 | 0 46 |
| **Design 2** | | | | | | | | | – | 70n | | 0 4 |

Table 3-6 Simulation $V_g = 2.5V$, $V_{o1} = 5V$, $V_{o2} = 1.25V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 5 | 1 25 | 2 2μ | 0 3 | 100m | 210m | 1μ | 100n | 70n | 0 76 | 0 45 |
| **Design 2** | | | | | | | | | – | 70n | | 0 37 |

Table 3-7 Simulation $V_g = 2.5V$, $V_{o1} = 5V$, $V_{o2} = 3.3V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 5 | 3 3 | 2 2μ | 0 3 | 100m | 80m | 1μ | 100n | 70n | 0 76 | 0 34 |
| **Design 2** | | | | | | | | | – | 70n | | 0 37 |

Table 3-8 Simulation $V_g = 2.5V$, $V_{o1} = 5V$, $V_{o2} = 5V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) | $I_{LA}$ (A) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 1** | 2 5 | 5 | 5 | 2 2μ | 0 3 | 100m | 50m | 1μ | 100n | 70n | 0 75 | 0 33 |
| **Design 2** | | | | | | | | | – | 70n | | 0 36 |
| **Design 2** | 2 5 | 5 | 5 | 4 7u | 0 3 | 100m | 50m | 1u | – | 70n | | 0 35 |
| **Design 2** | 2 5 | 5 | 5 | 10u | 0 3 | 100m | 50m | 1u | – | 70n | | 0 34 |

Table 3-9 Simulation $V_g = 2.5V$, $V_{o1} = 1.8V$, $V_{o2} = 1.25V$, $V_{o3} = 1.25V$.

| | $V_g$ (V) | $V_{o1}$ (V) | $V_{o2}$ (V) | $V_{o3}$ (V) | $L$ (H) | $ESR_L$ (Ω) | $I_{o1}$ (A) | $I_{o2}$ (A) | $I_{o2}$ (A) | $T_s$ (s) | $T_{MOT}$ (s) | $T_{LCK}$ (s) | $P_o$ (W) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Design 2** | 2 5 | 1 8 | 1 25 | 1 25 | 2 2μ | 0 3 | 450m | 80m | 80m | 1μ | 100n | 70n | 1 37 |

From the simulation result shown above, it is found that other than fewer switching cycles in each operation period, the presented switching sequence gives a lower average inductor current in wide range of loading and arbitrary combination of the type of sub-converters. Although in all buck or all boost case, due to larger ac component, the average inductor will be a little bit higher (Table. 3-3, 3-7 and 3-8), This can be compromised by using a larger inductor (Table. 3-8). Moreover, due to the "not return to $I_{offset}$" operation, the correlated problem such as ultra small triangle waveform of inductor current (Fig. 3-15) caused by the minimum on-time can be eliminated. Finally, since the converter type of the SIMO converter will be treated as a SISO converter and it is evaluated by the criterion (3-9(a) and (b)), the auto buck-boost will be used only when total SIMO type is located in buck-boost region. This considerably reduces the system complexity. In contrast, the auto buck-boost technique should be used to each channel of a Class-1 SIMO converter as shown in Fig. 3-9. The simulation data of these two topologies is shown in Figs. 3-17(a)-(c). It is shown that when SIMO has deep-boost and deep-buck sub-converters at the same

time, the total converter type is near to buck-boost balance (3-7) and the optimized Class-2 SIMO topology has a lower average inductor current than the Class-1 counterpart does.

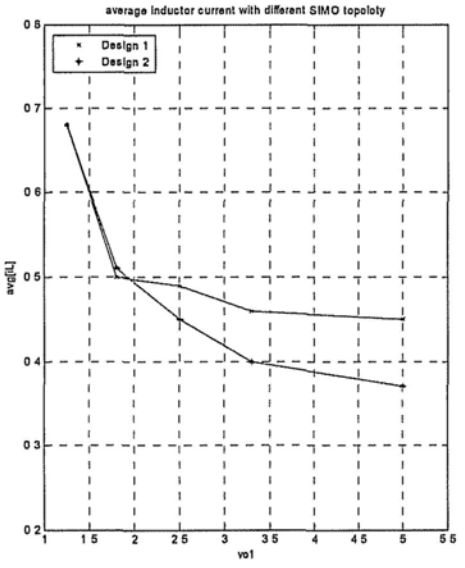



Fig. 3-17(a) Average inductor current vs. $V_{o1}$ @ $V_{o2}$ = 1.25V.

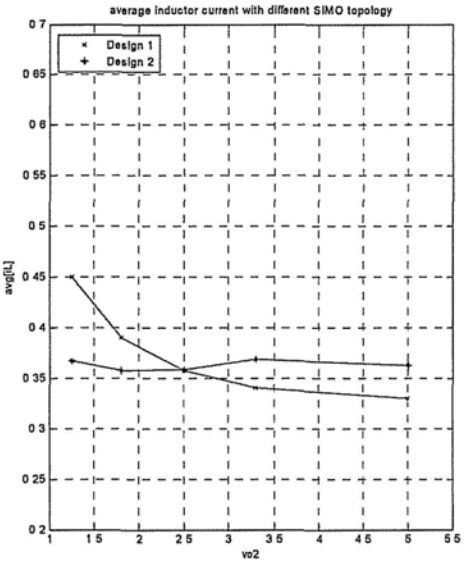



Fig. 3-17(b) Average inductor current vs. $V_{o2}$ @ $V_{o1}$ = 5V.

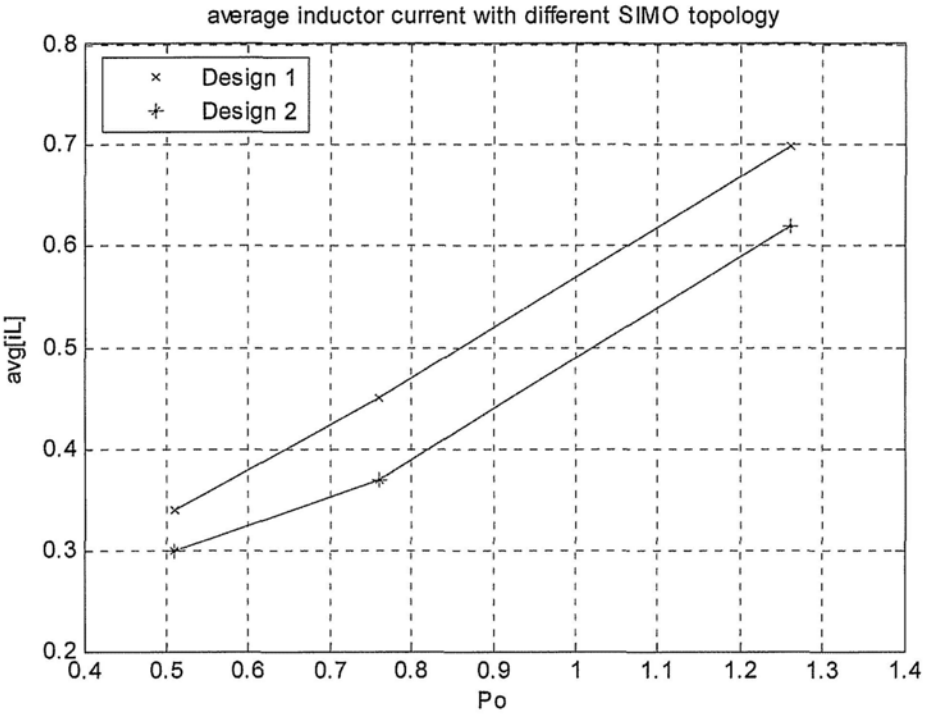



Fig. 3-17(c) Average inductor current of the Class-1 and Class-2 inductor-current waveform against output power under different $M_1$ = 0.5 and $M_2$ = 2.

## 3.2 Overview of the Operation

The circuit diagram of the proposed SIQO converter is shown in Fig. 3-18. The blocks in shadow have the same implementation as that introduced in Chapter 2, and so they will not be repeated in this chapter.

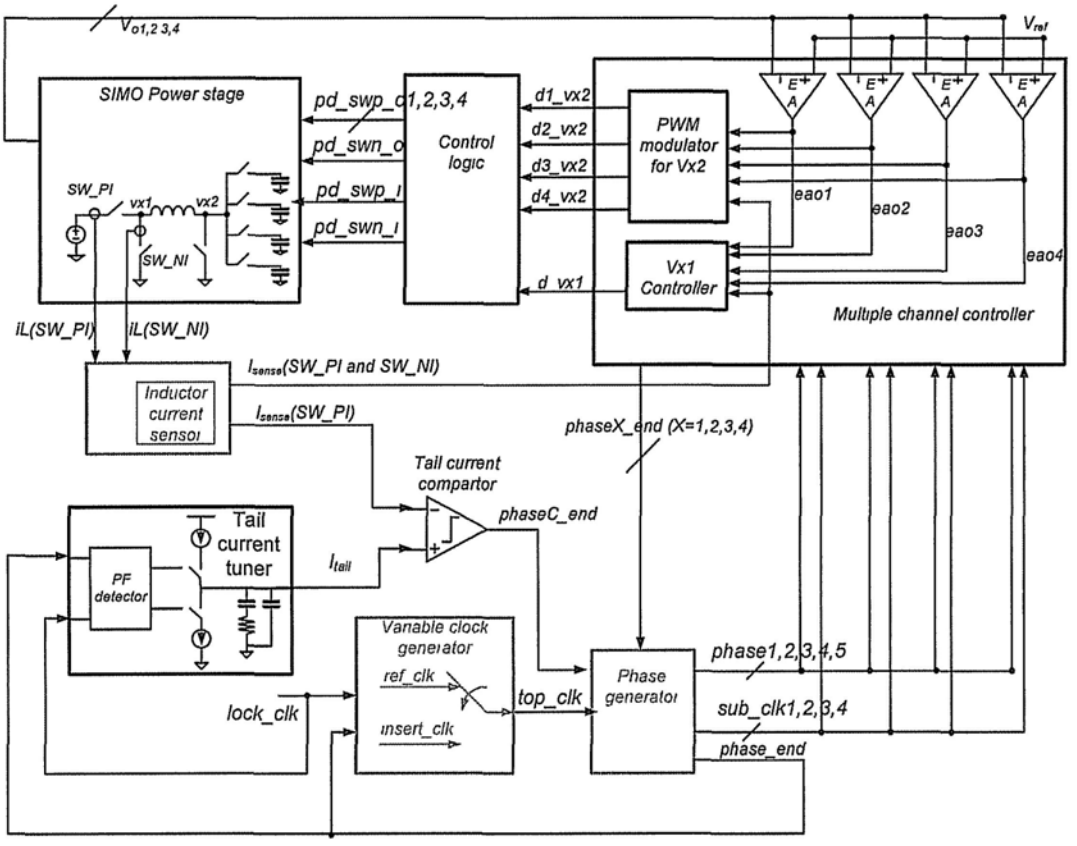



Fig. 3-18 Overall system of the proposed SIQO dc-dc converter.

As showed in the circuit diagram, the converter involves two feedback loops. Firstly, the output voltage of each channel is regulated by the controller similar to the conventional current-mode controller, and so this creates the voltage feedback loop. However, the major difference is that the control variable *eaoX* ($X$ = 1 - 4) in this design is used to define the power delivery time (i.e. the SW_B cycle) no matter that the sub-converter is a buck, boost or buck-boost converter. This operation ensures the optimal switching sequence, which means that the power efficient switching cycle (i.e. the SW_B cycle) will be processed first. In fact, these control variables reflect

the power distribution information among the multiple channels, but it is not sufficient to increase the output power especially for the boost sub-converter. The waveform of the system operating in the steady state is shown in Fig. 3-19. The voltage relationship is $V_{o1} > V_{o3} > V_{o4} > V_g > V_{o2}$. It is noted that *rampX* ($X = 1$ - 4) is a signal generated for duty cycle of the sub-channel. Details will be covered later.

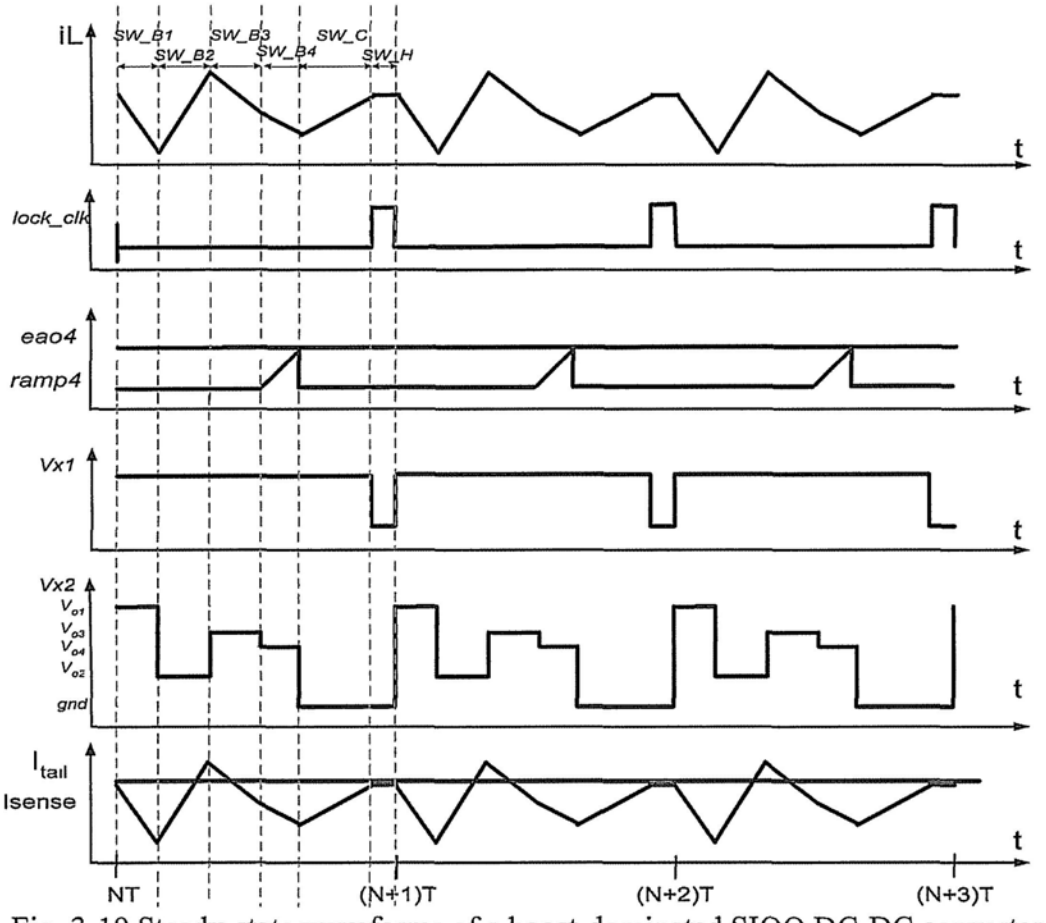


Fig. 3-19 Steady-state waveforms of a boost-dominated SIQO DC-DC converter.

Secondly, the tail current of the inductor is controlled by another control signal $I_{tail}$, which is defined by a PLL-like $I_{tail}$-tuning circuit in order to lock the switching frequency. This circuit creates the tail current of the inductor feedback loop. Moreover, $I_{tail}$ indicates the output power of the SIQO converter. As a result, it is possible to control the output power for the SIQO converter by controlling $I_{tail}$. Due to this relationship, the tail inductor-current tuning circuit should dominate the dynamic performance which means that inserting zero in this controller is necessary.

The waveform of the system operation at loading transient is shown in Fig. 3-20. It is found that when the loading current of one channel increases, $I_{tail}$ will increase. At the same time, *eaoX* ($X$ = 1 - 4) will increase or decrease to a proper value. In the end, the total output power of the SIQO converter increases while the power distribution of each sub-channel is reallocated.

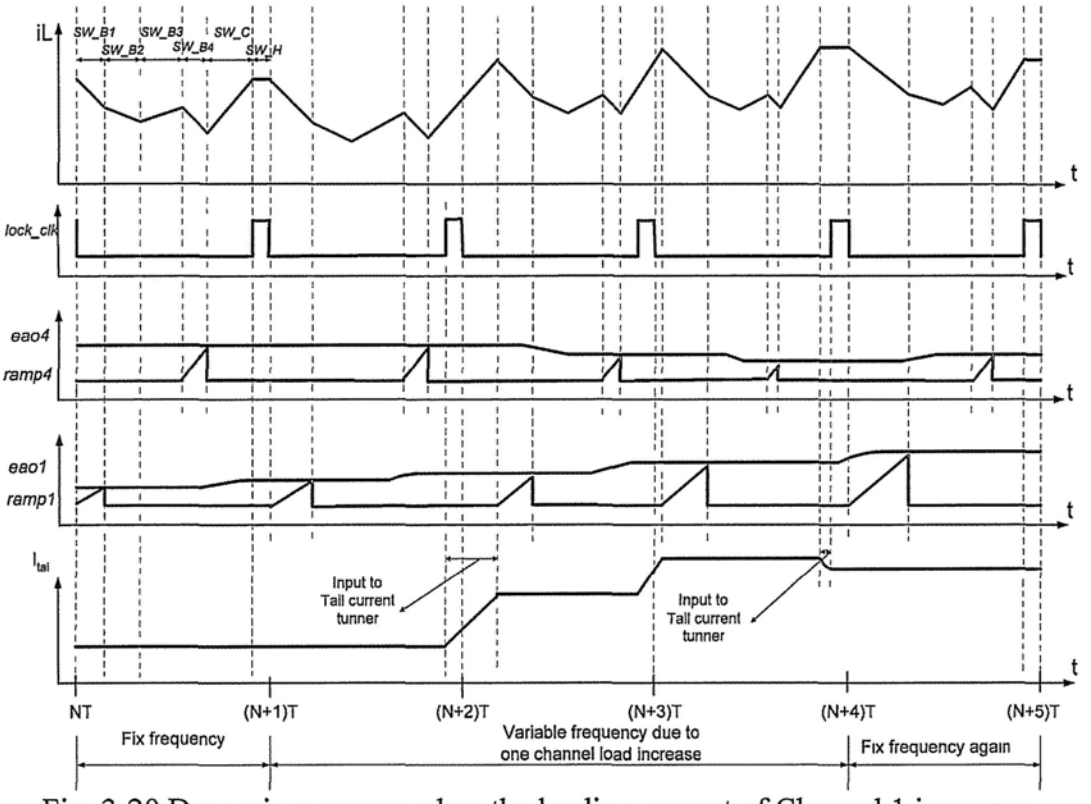



Fig. 3-20 Dynamic response when the loading current of Channel 1 increases.

For a general auto buck-boost application, the inductor current may need to fall down (i.e. $V_{x1}$ = 0) if the SIQO is buck-dominated as shown in Fig. 3-21. A $V_{x1}$-control circuit is needed to determine when $V_{x1}$ tights to the ground so to define the inductor discharging period (i.e. the SW_D cycle). Moreover, in order to design a seamless transition when the SIMO converter operates in the buck-dominated, boost-dominated or buck-boost balance mode (i.e. $T_{SW\_C}$ = 0 and $T_{SW\_D}$ = 0), an artificial NP mismatch current sensor cooperates with the tail-current tuning circuit to prevent limit-cycle oscillation during the mode transition. The voltage relationship

is $V_{o1} > V_g > V_{o2} > V_{o3} > V_{o4}$. *ramp_piX* ($X = 1 - 4$) is a signal generated for the $V_{x1}$-control circuit which will be mentioned in detail in later section.

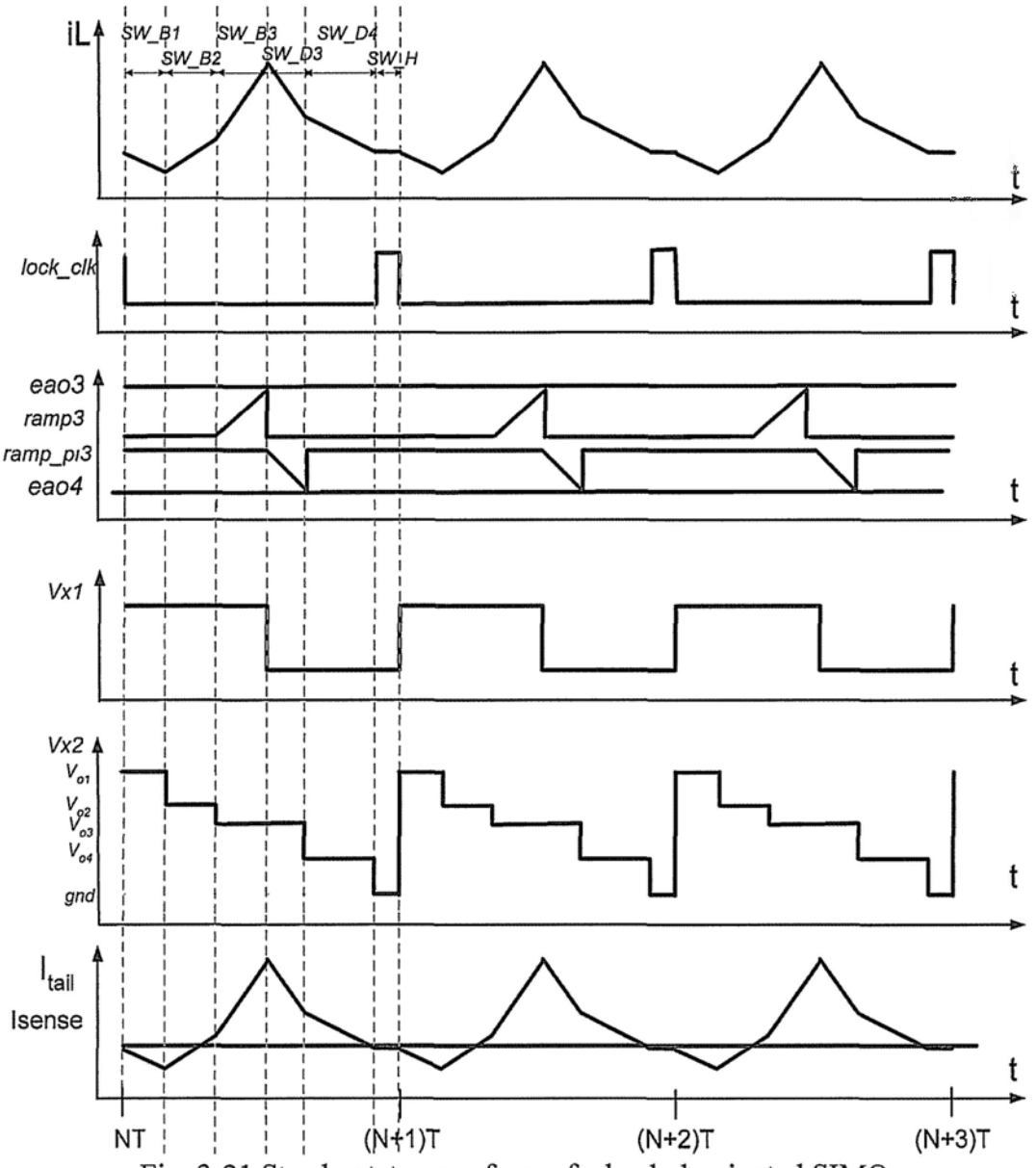



Fig. 3-21 Steady-state waveform of a buck dominated SIMO.

## 3.3 Single-Channel Auto Buck-Boost Controller Extensible for Multi-Channels

In Chapter 2, a multi-channel extensible single-channel auto buck-boost controller based on three-segment control has been presented. In that controller, the switching sequence is SW_C → SW_B → SW_D, which is suitable to extend to the

Class-1 SIMO converter. In this section, another multi-channel extensible single-channel auto buck-boost controller will be presented. Since it is targeted for the optimized Class-2 SIQO converter, the control variable is selected to be the duty cycle of the SW_B cycle no matter that it is a buck, boost or buck-boost sub-converter. The circuit diagram is shown in Fig. 3-22.

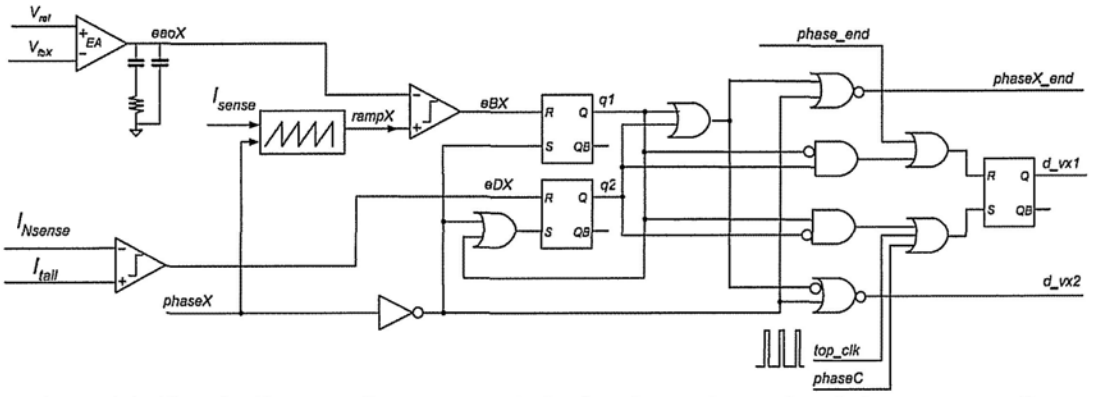



Fig. 3-22 Circuit diagram for proposed single-channel auto buck-boost controller.

The input signals include: $V_{ref}$ = voltage reference; $V_{fbX}$ = feedback signal from the output voltage; $I_{Nsense}$ = current-sensed signal from the inductor-current sensing circuit when the power transistor SW_NI is turned on; $I_{tail}$ = inductor tail-current reference generated by the tail-current tuning circuit; *phaseX* = channel enable signal; *phaseC* = the inductor charging cycle (i.e. the SW_C cycle), its generation can be referred to Fig. 2-38 in Chapter 2; *phase_end* = a signal used to indicate end of sub-period; *top_clk* = the clock pulse for state initialization. The output signals include *phaseX_end* = signal used to disable the operation of current channel (i.e. make *phaseX = 0*); *d_vx2* = a duty command signal used to control power deliver period (i.e. SW_B and SW_D); *d_vx1* = a duty command signal used to control when $V_{x1}$ is tied to ground. Some internal signals include: *rampX* = an inductor current modulated ramp signal used to create RSFF reset signal, it is generated by the circuit shown in Fig. 3-23; *eBX* = a reset signal used to end SW_B; *eDX* = a reset signal used to end SW_D; *eaoX* = the output of the compensator.

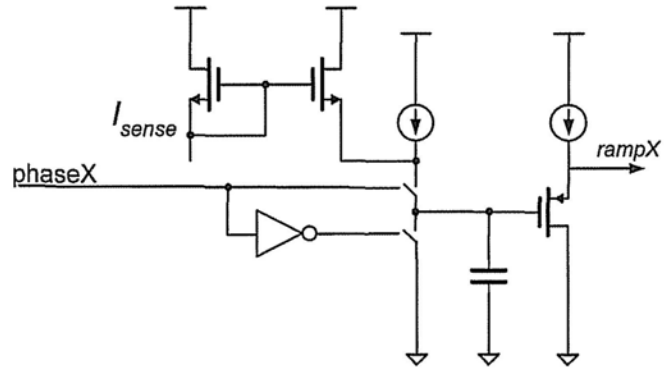


Fig. 3-23 Current-modulated ramp generator.

The operation principle is shown in Fig. 3-24(a) and Fig. 3-24(b). After initialization, $q1 = 1$, $q2 = 1$, $d\_vx1 = 1$ and $d\_vx2 = 1$, the SW_B cycle is enabled and then the inductor current goes from the power supply to the output capacitor. After *eaoX* and *rampX* intersect, $q1 = 0$ and $d\_vx1 = 0$. The SW_B cycle is disabled and the SW_D cycle is enabled. If the converter is buck type, in order to stabilizing inductor current waveform based on V. S. B, $I_{tail}$ will locate in a position so that the SW_D cycle will hold a certain period until $I_{Nsense}$ and $I_{tail}$ intersect. After that, $q2 = 0$ and $d\_vx2 = 0$. the SW_D cycle is disabled, *phaseX_end* will generate a short pulse so that *phaseX* = 0 and the power delivery period is ended. Successively, *phaseC* = 1 and the SW_C cycle is enabled. The operation of SW_C is generated from the circuit diagram in Fig 3-25(a). It is found that the SW_C cycle will persist until $I_{Psense} > I_{tail}$. Since it is a buck operation, *phaseC_end* will be turned to 1 immediately after several comparator delays. Finally, *phase_end* will be turned to 1. The switching period is ended and the converter enters idle period (SW_H). The operation will repeat until next *top_clk* and *phaseX* signal are detected.

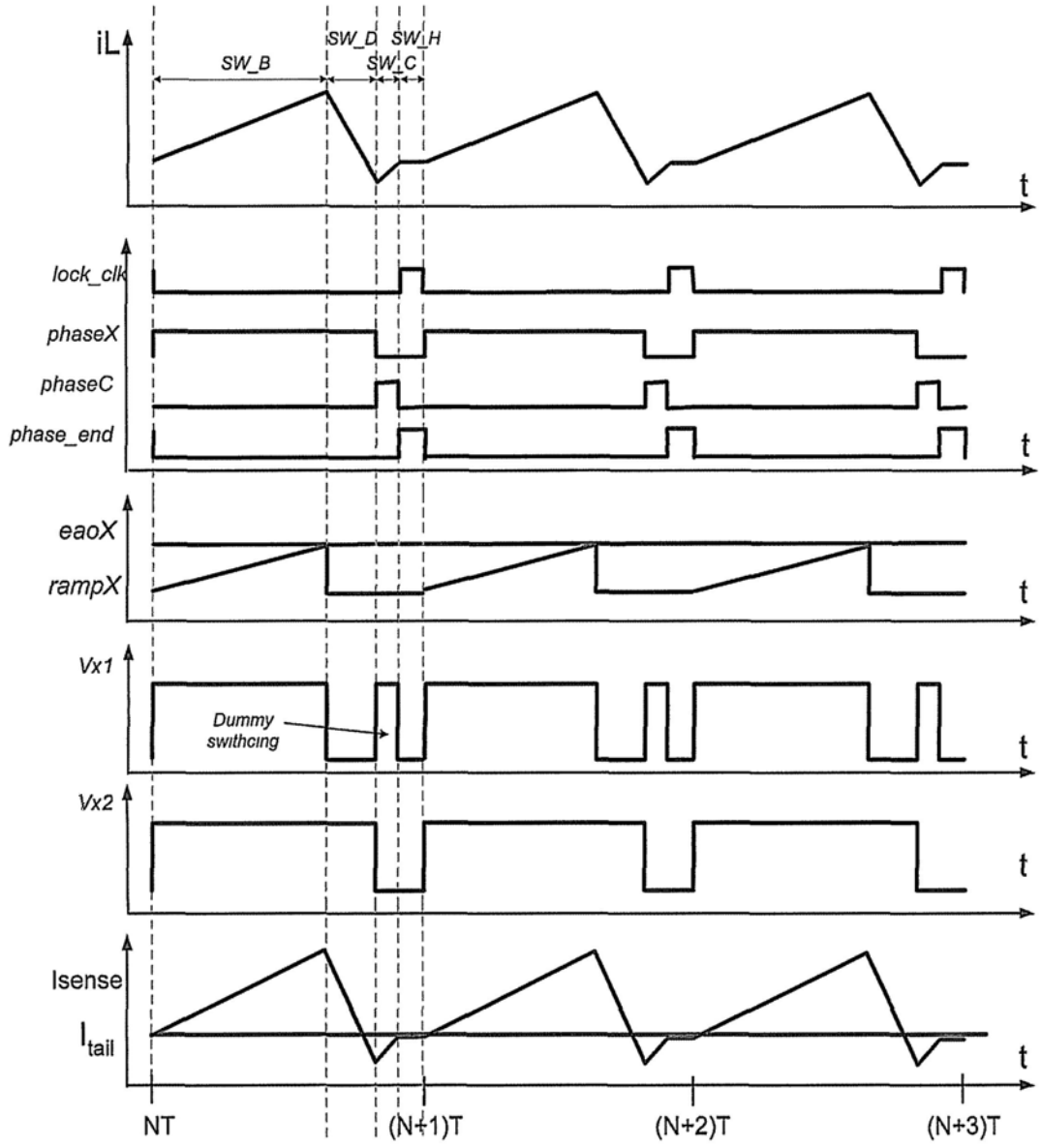



Fig. 3-24(a) Applied the controller to a buck converter.

If the converter is of boost type, the operation is similar. As shown in Fig. 3-24(b), after the SW_D cycle is enabled, in order to stabilize the inductor current waveform based on V. S. B, $I_{tail}$ will locate in a position larger than $I_{Nsense}$ so that SW_D cycle will end immediately after $q2$ is enabled to be reset. After that, the SW_C period is enabled and be held until $I_{Psense} > I_{tail}$.

It is found that this control scheme can be directly used in the buck-boost converter, which has been verified in the simulation of Section 3.2. Comparing to the auto buck-boost technique presented in Chapter 2, it presents a different switching

sequence. The switching sequence of this design is SW_B → SW_D → SW_C. In the single-channel application, there is no large difference between this two switching sequences. However, the sequence and the selected control variable (duty cycle of SW_B) in this design make it more suitable to translate to the SIMO applications.

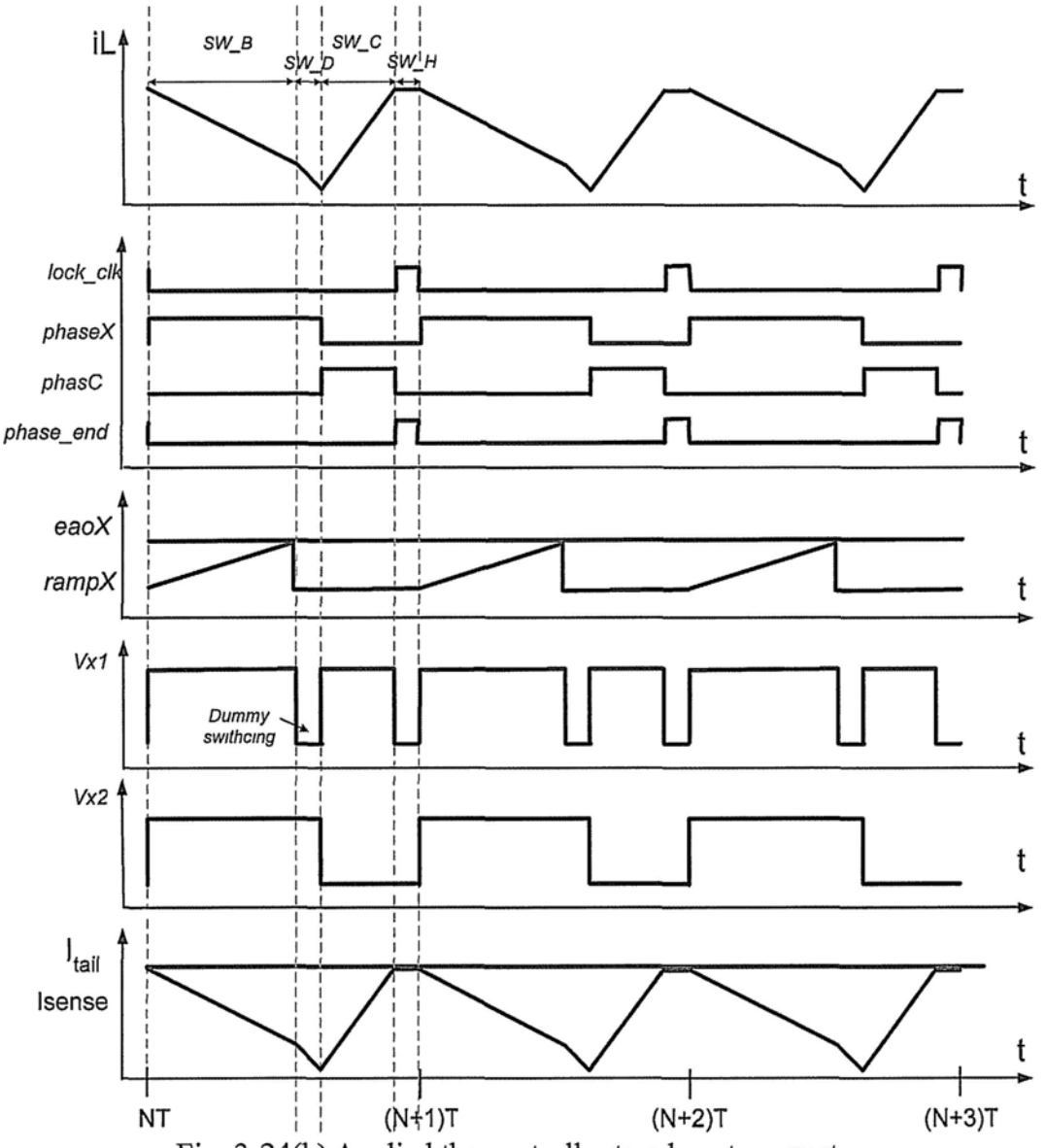



Fig. 3-24(b) Applied the controller to a boost converter.

In practical implementation, NP mismatch of full wave current sensor will affect the system operation. In the design presented in Chapter 2, as shown in Fig. 3-25(b), a non-uniform inductor bottom current (defined by $I_{offet}$) for sub-channel is generated,

since using $I_{Psense}$ or $I_{Nsense}$ to compare with $I_{offset}$ is unknown. In this design, as shown in Fig. 3-22 and Fig. 3-25(b), no matter what type of the converter is, $I_{Nsense}$ is specified in the SW_D cycle while $I_{Psense}$ is specified in the SW_C cycle. Moreover, the state machine (generated by the phase generator) in this control algorithm enforces these two comparisons appear one after another. As a result, the uncertainty referred above is eliminated. Comparing Fig. 3-24(a) and 3-24(b) to Fig. 3-19 and Fig. 3-21, it is found that this switching sequence adds a dummy switching cycle. However, it is deserved to achieve a stable operation independent of the mismatch of current sensor.

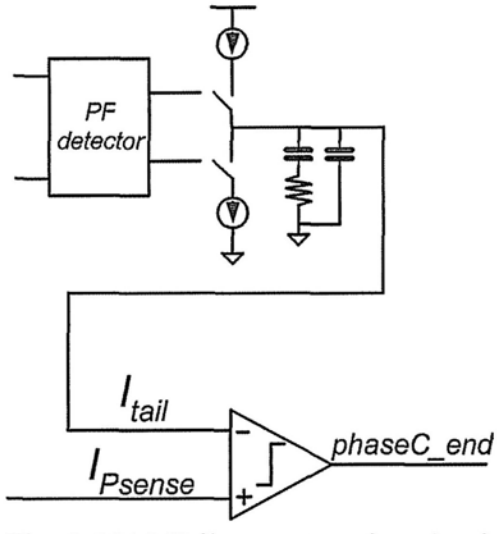



Fig. 3-25(a) Tail-current tuning circuit.

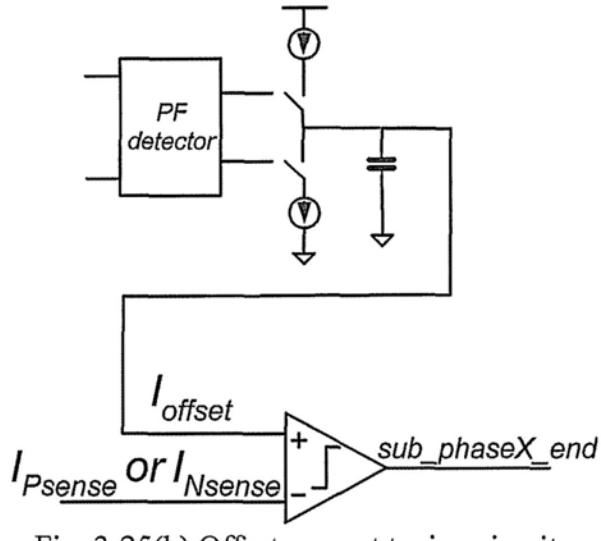



Fig. 3-25(b) Offset-current tuning circuit.

In Fig. 3-26 and Fig. 3-27, the possible inductor-current waveforms related to different mismatch case are shown. It is found that both cases can operate properly. However, in Fig. 3-27(a), there are large SW_C and SW_D period appear simultaneously, which is related to the quantity of the mismatch in current sensor. This is violation to optimized average inductor current theory presented above. And efficiency will drop depend on how much the mismatch is. A result, in this design, $I_{Psense}$ is artificially set to two times of $I_{Nsense}$ in order to dominate the mismatch of current sensor and ensure inductor tail current operate as Fig. 3-26.

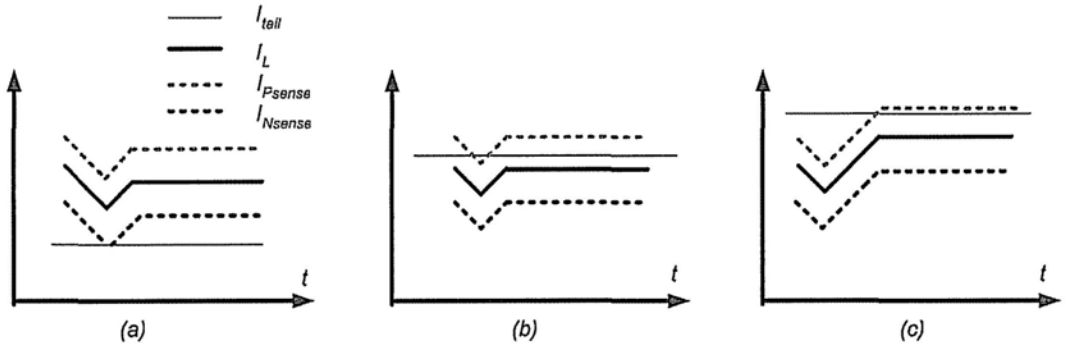



Fig. 3-26 Tail-current control with current sensor mismatch when $I_{Psense} > I_{Nsense}$.

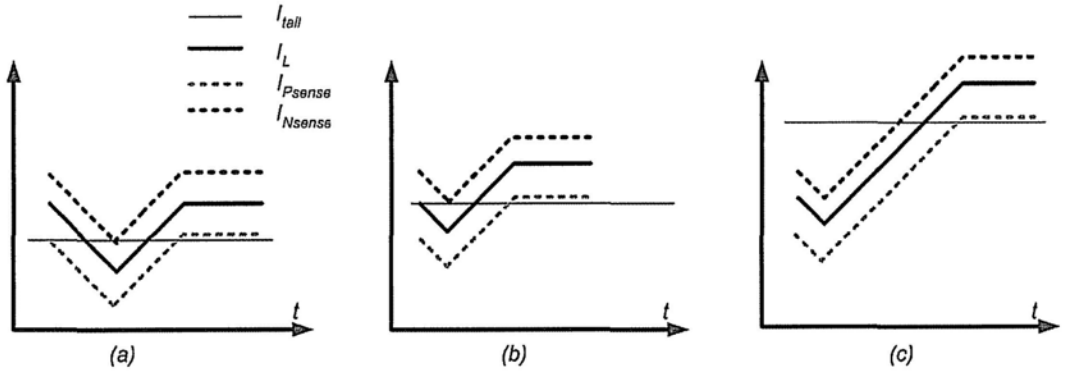



Fig. 3-27 Tail-current control with current sensor mismatch when $I_{Nsense} > I_{Psense}$.

A tail-current tuning shown in Fig. 3-25(a) is designed to complete frequency feedback loop by defining the control variable $I_{tail}$. As shown in Fig. 3-24(b), it is obvious that the duty cycle of SW_B controlled by the voltage feedback loop is out of phase which means that increasing the SW_B period cannot increase $V_o$ or power delivery ability. This is the major difference between using the SW_C cycle as the control variable in the conventional boost converter and using the SW_B cycle in this design. As a result, controlling the inductor tail current by the frequency feedback loop is necessary to regulate the output voltage in this design, not only for locking the switching frequency to the reference clock. In order to make the tail-current controller dominate the frequency response, a TYPE II charge pump which can create a low frequency zero is used. The difference between the tail-current controller and the offset current controller is shown in Fig. 3-25(a) and 3-25(b).

## 3.4 $V_{x1}$-Control Circuit and Extension to Multiple Channels

According to the analysis presented above, the auto buck-boost controller will execute a state machine as shown in Fig. 3-28(a). In order to extend to SIMO converter, it is straightforward to design a state machine as shown in Fig. 3-28(b). However, it is not a universal solution for arbitrary type and output loading.

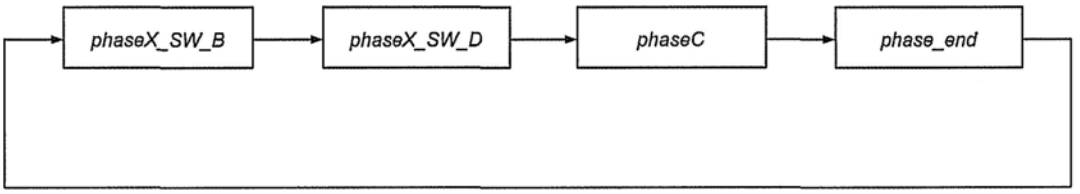



Fig. 3-28(a) State machine for SISO dc-dc converter.

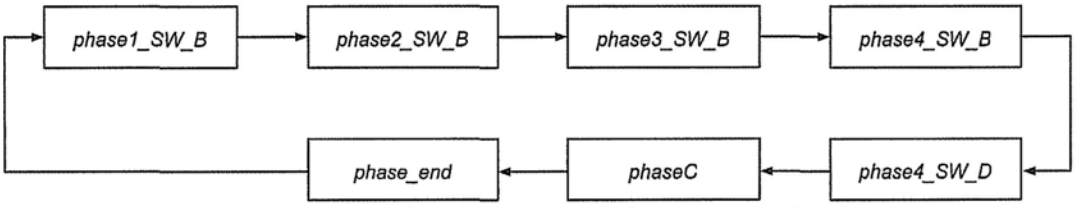



Fig. 3-28(b) State machine for SIQO dc-dc converter (not arbitrary).

Provided that the SIMO converter is buck-dominated, at the meantime, the last channel (Channel 4 in this example) has a very light load comparing to the other channel as shown in Fig. 3-29. It is found that although SW_B4 = 0, which is controlled by the voltage feedback loop of Channel 4. This indicates *eao4* has gone to saturation (*eao*4 = 0) and the voltage feedback loop for Channel 4 is broken. Since the inductor discharging period is controlled by the tail-current controller, $V_{o4}$ will be charged to an unexpected value and the system will then be out of regulation.

As a result, in order to support general case and make the SIMO converter operate as shown in Fig. 3- 21. A state machine is provided in Fig. 3-30. It is obvious that this state machine can provide arbitrary load for arbitrary type of sub-converter. However, it should be noted that based on the optimal switching sequence presented in Section 3.2, one more constrain should be added. In the steady state, when $V_{x1}$ is

tied to the ground (SW_D($X$) ($1 \le X \le 3$) cycle is enabled), it should not be tight to the power supply again (SW_B($X + 1$) ($1 \le X \le 3$) cycle should not be enabled). Based on this criterion, two solutions to implement Fig. 3-31 are provided as below.

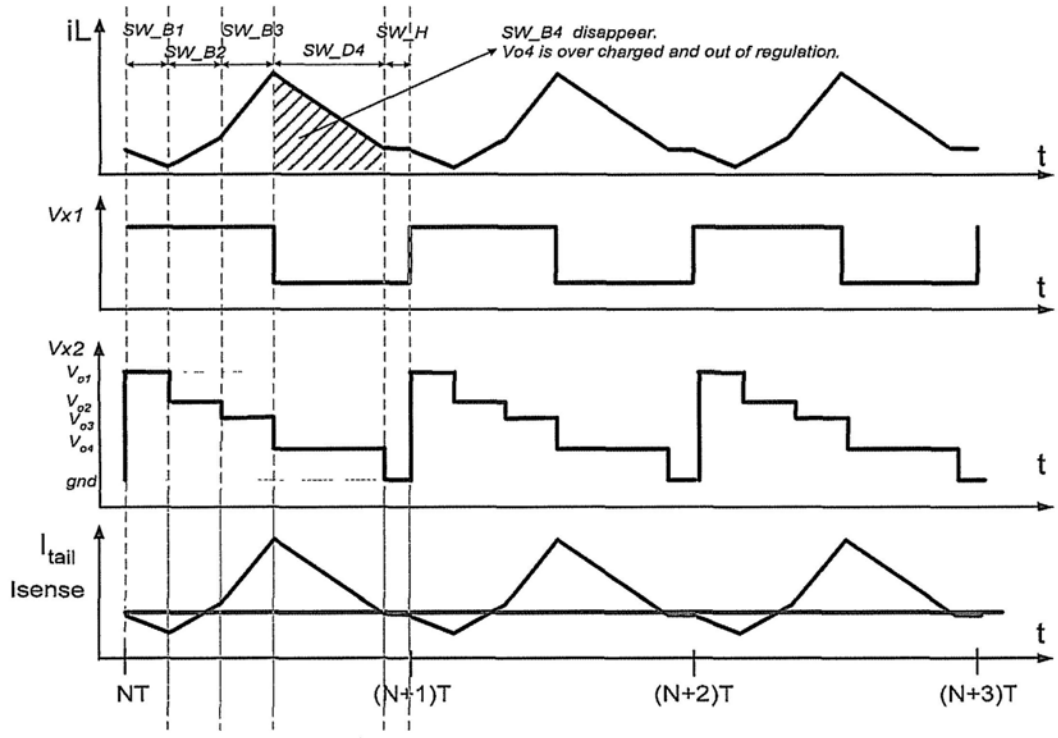



Fig. 3-29 Unregulated steady state of a SIMO dc-dc converter based on the control algorithm in Fig. 3-29.

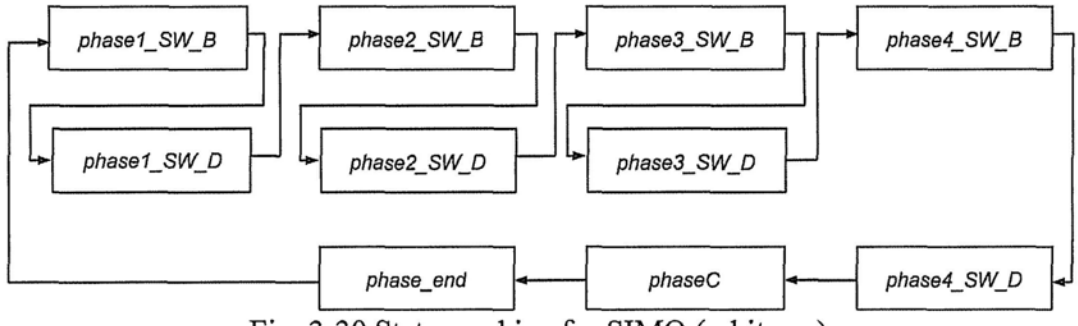



Fig. 3-30 State machine for SIMO (arbitrary).

1. Independent $V_{x1}$ controller.

The independent $V_{x1}$ controller can be implemented as Fig 3-31. The signal *phaseC* which represents the inductor charging cycle SW_C will be compared to a minimum SW_C cycle. As a result, in the steady state, phaseC will be larger than or at least equal to the minimum SW_C cycle (100ns in this design). As a result, even

though the SIMO converter is buck-dominated, it will still work in a virtual boost-dominated mode. This is shown in the simulation result in Fig. 3-32.

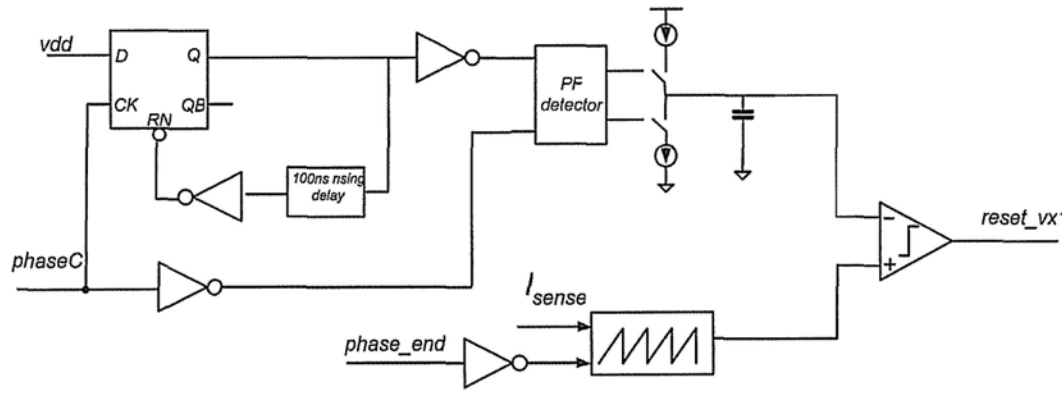



Fig. 3-31 State machine for SIMO (arbitrary).

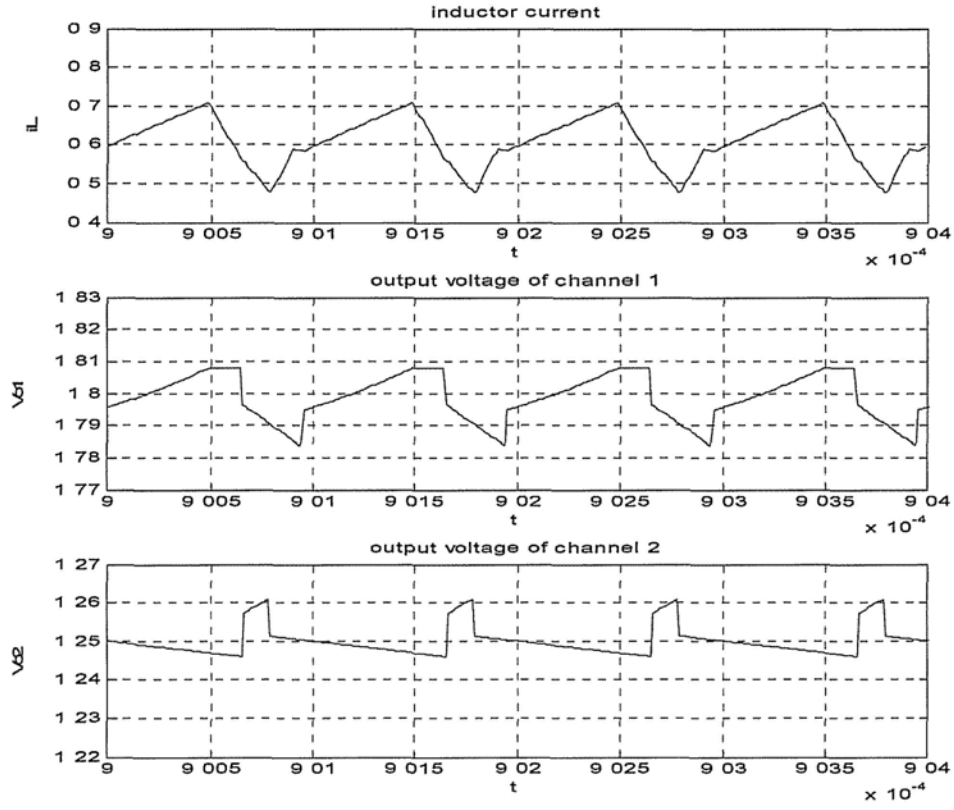



Fig. 3-32 Steady state for a buck dominated SIMO working in virtual boost dominated mode ($V_{o1}$ = 1.8V, $V_{o2}$ = 1.25V $V_g$ = 2.5V, $I_{o1}$ = 450mA, $I_{o2}$=64mA).

The advantage of this control scheme is that it has sufficient design freedom. However, the major drawback is that it needs a minimum SW_C period which may increase the average inductor current in buck-dominated operation.

2. Extending SISO single-channel controller to DIDO channel coupling controller

Since the violation of voltage is induced by saturation of *eao*4, which originates from the channel coupling effect when extending the SISO to SIMO converter, it is possible to extend *eaoX* operation range by making it as a coupling input to the adjacent channel. The SIMO controller circuit diagram is shown in Fig. 3-33.

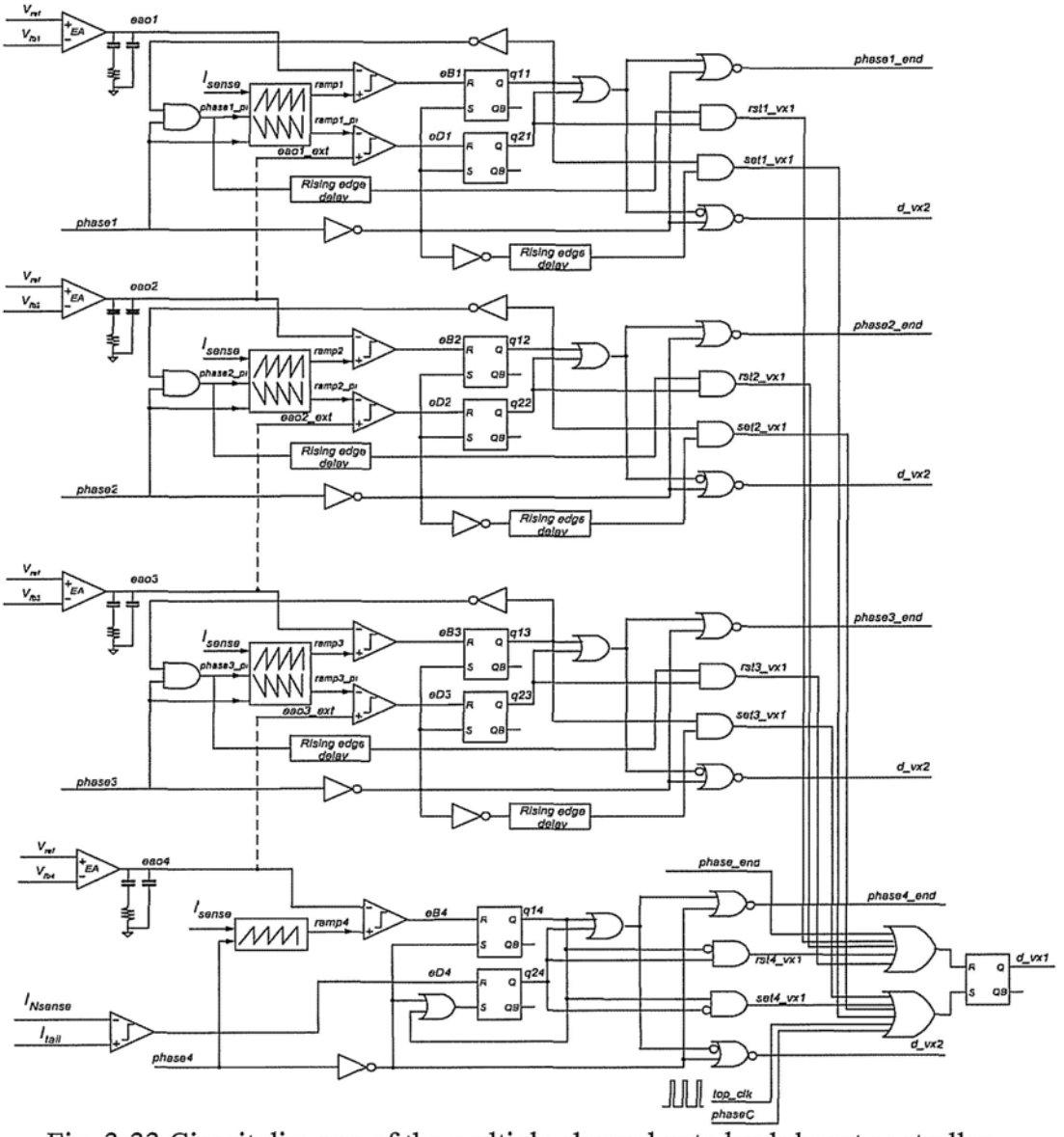



Fig. 3-33 Circuit diagram of the multiple channel auto buck-boost controller.

It is found that the extra input "*eaoX_extra* is connected to the output of the error amplifier of the adjacent channel *eao(X+1)*. The rising edge delay in the circuit diagram is used to ensure not capturing an error signal and reset d_vx1. The rule of

signals' nomination is similar to the single-channel controller, while in here, $X$ is replaced by 1, 2, 3 and 4. It is shown that by introducing the dual ramp generator (Fig. 3-34), *eaoX* will act as second input to channel $X$ - 1 when it is saturated in its own channel. Moreover, the crossover of *eaoX* and *ramp*($X$ - 1)*_pi* will create a duty cycle for SW_D($X$ - 1).

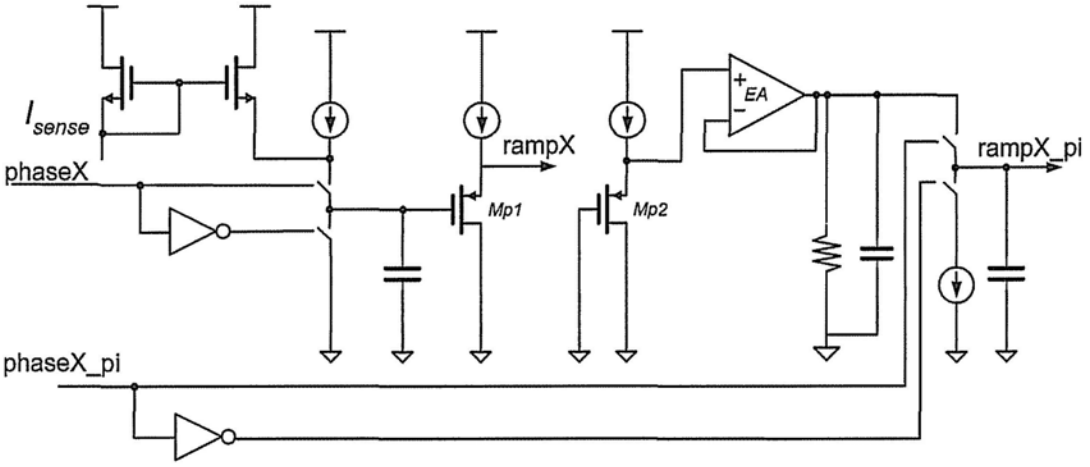



Fig. 3-34 Dual ramp generator.

Therefore, the original SISO single-channel current-mode controller is extended to dual-input dual-output (DIDO) channel-coupling current-mode controller. The operation principle and the generation of duty periods for different switching cycles are shown in Fig. 3-35. Since eao4 stays below the dc level of ramp4, the register's output $q14$ will turn to 0 immediately after *phase4* is enabled. SW_B4 = 0 and SW_D4 are defined by the tail-current controller. Different from the unregulated state shown in Fig. 3-30, the error voltage of $V_{o4}$ induced by overcharging of SW_D4 and loop broken due to saturated eao4 will continuously decrease eao4 and feed back to Channel 3. Since eao4 is located in the range of *ramp3_pi*, the operation range of eao4 is successfully extended.

When *phase*3 is enabled, as shown in Fig. 3-35, $q13$ will turn to 0 until *eao*3 and *ramp*3 intersect, which defines the period of SW_B3. After that, *phase3_pi* is enabled. The second register is then programmable and $q23$ will turn to 0 until eao4

and *ramp3_pi* intersect, which defines the period of SW_D3. As a result, $V_{x1}$ is tied to the ground during the duty period of Channel 3 and shares the function of discharging inductor current with Channel 4. It is straightforward that this operation can be translated to other channels and makes this SIMO controller meet the arbitrary load and converter-type requirement. Moreover, It is noted that in the steady state, SW_DX ≠ 0 implies that $eao(X+1)$ stays below $ramp(X+1)$, so that SW_B$(X+1)$ = 0. This propagation property makes it satisfied with the citizen of the optimal switching sequence.

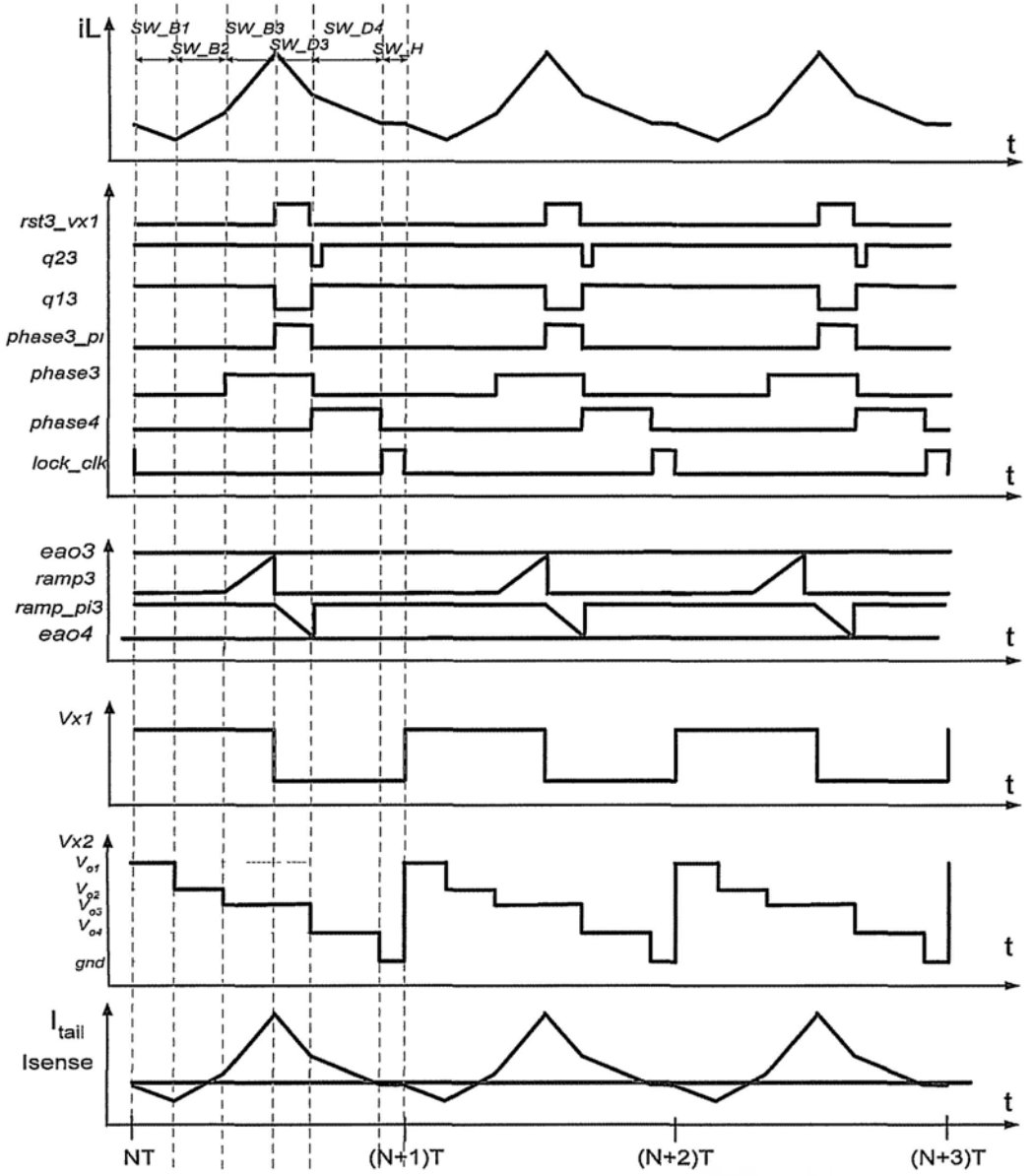



Fig. 3-35 Steady-state waveform of a buck-dominated SIMO when $V_{o4}$ has a relative light load.

The simulation results of the boost-dominated and buck-dominated of the SIQO converter and the transition between these two types are shown in Figs. 3-36, 3-37 and 3-38.

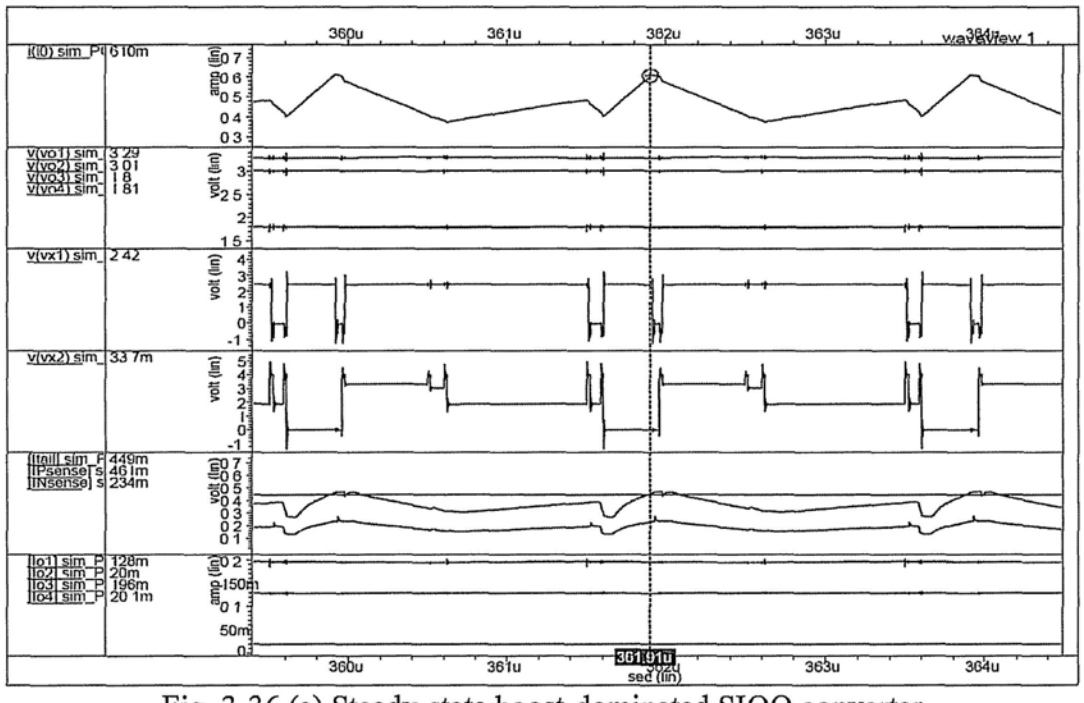



Fig. 3-36 (a) Steady-state boost-dominated SIQO converter $V_g$ = 2.5V, $V_{o1}$ = 3.3V, $V_{o2}$ = 3V, $V_{o3}$ = $V_{o4}$ = 1.8V, $I_{o1}$ = 128mA, $I_{o2}$ = 20mA, $I_{o3}$ = 200mA, $I_{o4}$ = 20mA.

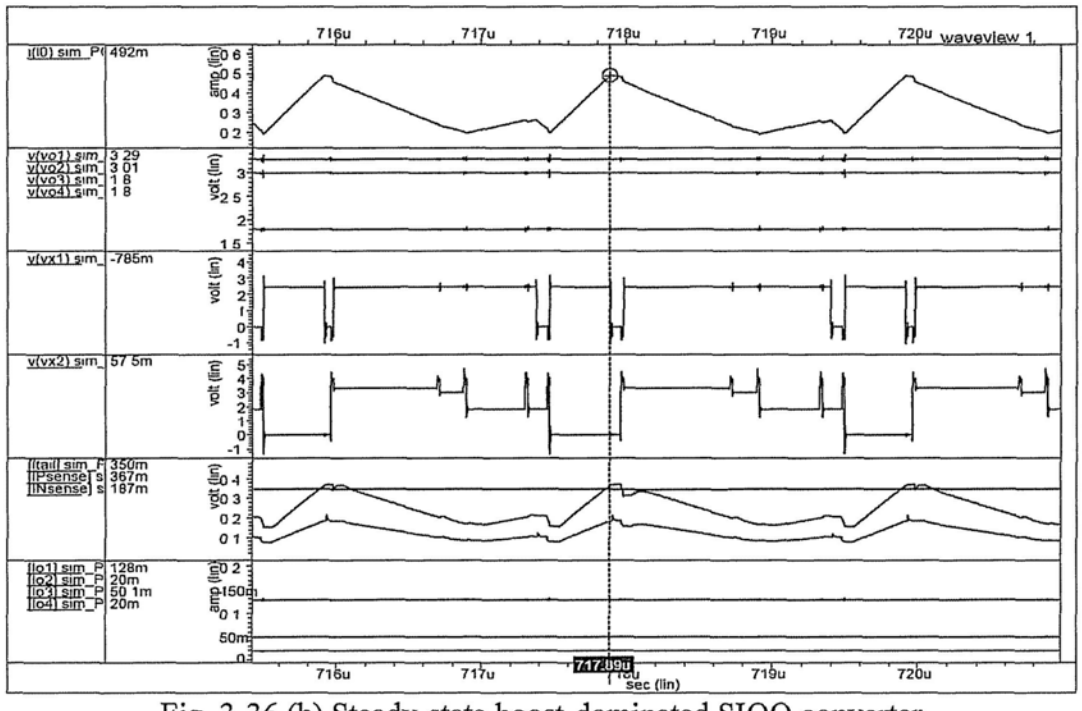



Fig. 3-36 (b) Steady-state boost-dominated SIQO converter $V_g$ =2.5V, $V_{o1}$ = 3.3V, $V_{o2}$ = 3V, $V_{o3}$ = $V_{o4}$ = 1.8V, $I_{o1}$ = 128mA, $I_{o2}$ = 20mA, $I_{o3}$ = 50mA, $I_{o4}$ = 20mA.

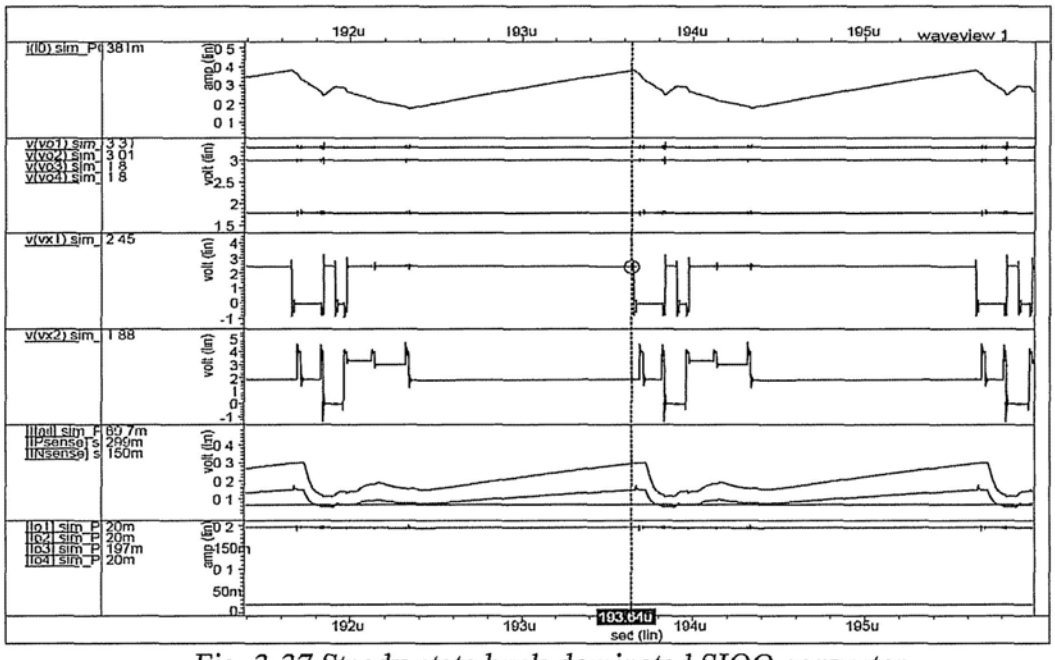



Fig. 3-37 Steady-state buck-dominated SIQO converter $V_g = 2.5\text{V}$, $V_{o1} = 3.3\text{V}$, $V_{o2} = 3\text{V}$, $V_{o3} = V_{o4} = 1.8\text{V}$, $I_{o1} = 20\text{mA}$, $I_{o2} = 20\text{mA}$, $I_{o3} = 200\text{mA}$, $I_{o4} = 20\text{mA}$.

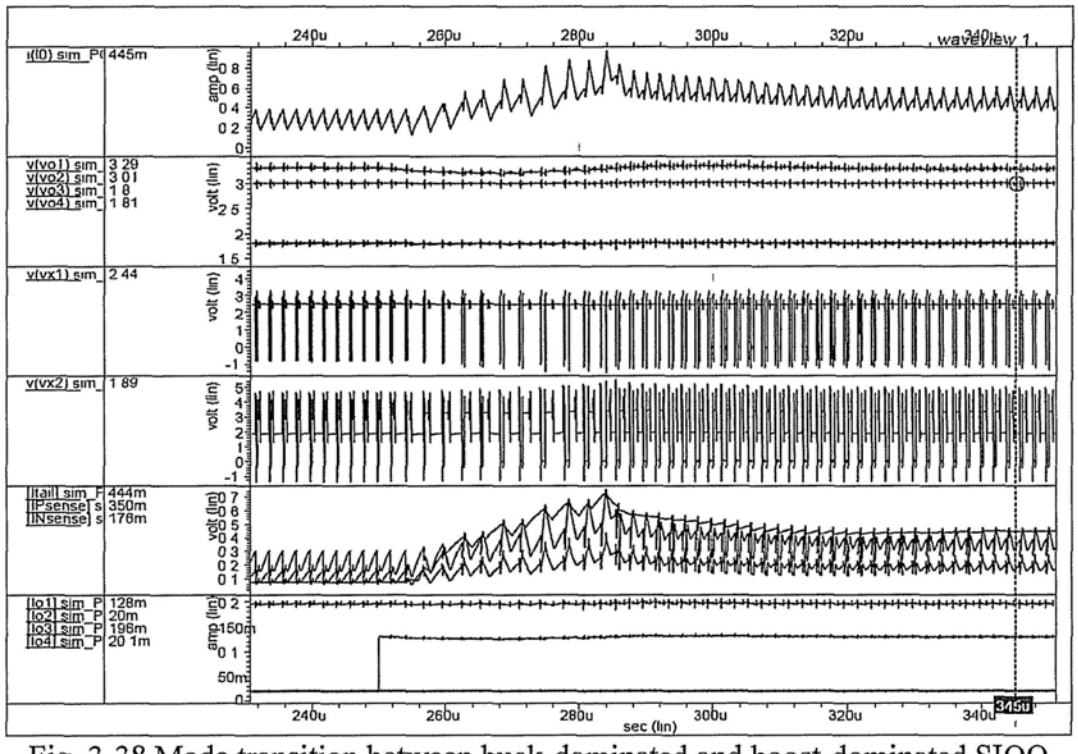



Fig. 3-38 Mode transition between buck-dominated and boost-dominated SIQO converter $V_g = 2.5\text{V}$, $V_{o1} = 3.3\text{V}$, $V_{o2} = 3\text{V}$, $V_{o3} = V_{o4} = 1.8\text{V}$, $I_{o1} = 20\text{mA} \rightarrow 128\text{mA}$, $I_{o2} = 20\text{mA}$, $I_{o3} = 200\text{mA}$, $I_{o4} = 20\text{mA}$.

From the above simulations, it is found that the proposed control algorithm is suitable for a wide sub-converter type and different loading combinations no matter

that it is boost or buck-dominated. It also abides the rule for optimal switching sequence so that the conduction loss will be kept low.

## 3.5 Measurement Results

The design presented above has been fabricated in AMS CMOS 0.35-μm 2P4M process. The chip area is 5000μm × 2000μm. The micrograph is shown in Fig. 3-39. The power switches are located on the left of the chip, whereas the control circuit is positioned on the right. In order to reduce routing resistance, all the four layers of metal are used with maximizing the contacts and vias. The multiple pads are used to reduce the effective routing resistance.

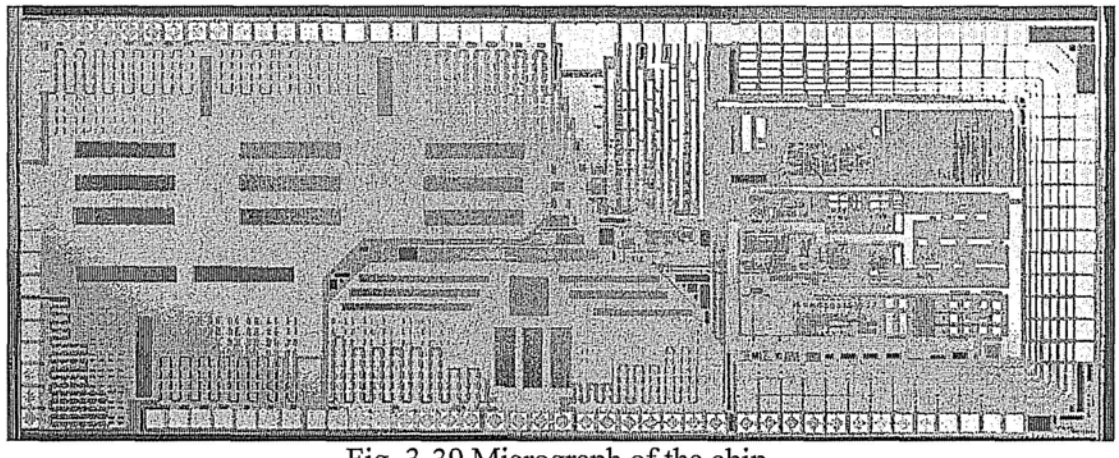


Fig. 3-39 Micrograph of the chip.

The settings of the measurement are shown in Table 3-10. For the measurement presented in this part, the results are based on the parameters listed in the table.

Table 3-10 Measurement setting.

| | |
|---|---|
| Output voltages | $V_{o1}$ = 3.4V, $V_{o2}$ = 3V, $V_{o3}$ = 2.4V, $V_{o4}$ = 1.76V |
| Input voltage (nominal) | 2.3V – 3.3V (limited by nwell connection.)<br>Nominal 2.5V |
| Inductor and its ESR | 4.7μH and 25mΩ |
| Capacitor and its ESR for each channel | 10μF and 20mΩ |
| Operation frequency | 250kHz – 450kHz (Nominal 300kHz) |

1. Efficiency vs. Total output power ($P_o$) and Input voltage ($V_g$)

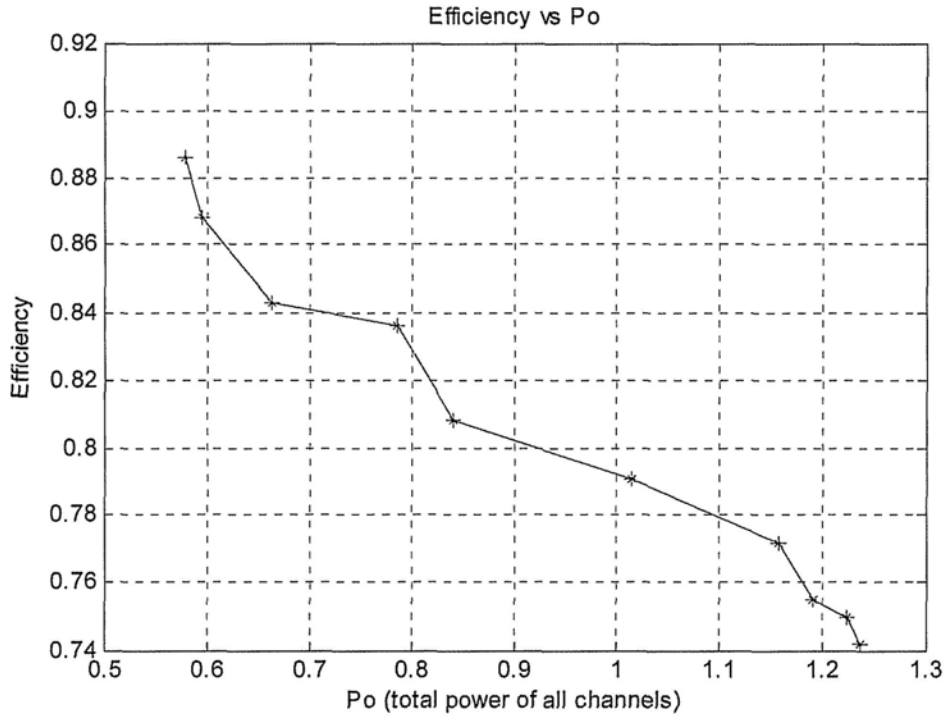



Fig. 3-40 Efficiency for different output powers (measured at $V_g = 2.44$V, $F_s = 300$kHz).

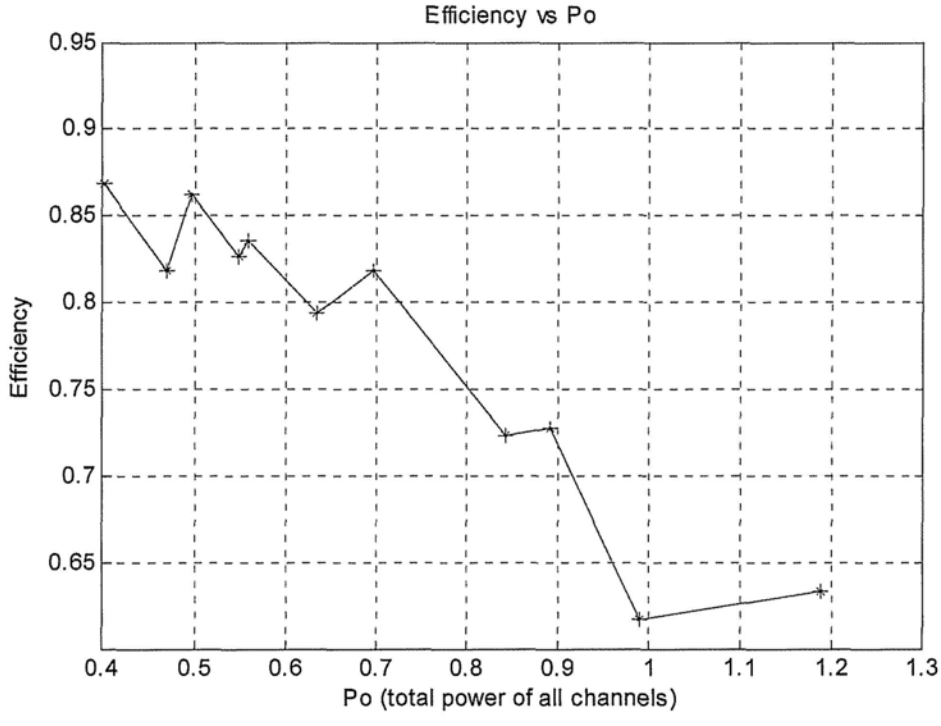



Fig. 3-41 Efficiency for different output powers (measured at $V_g = 2.44$V, $F_s = 400$kHz).

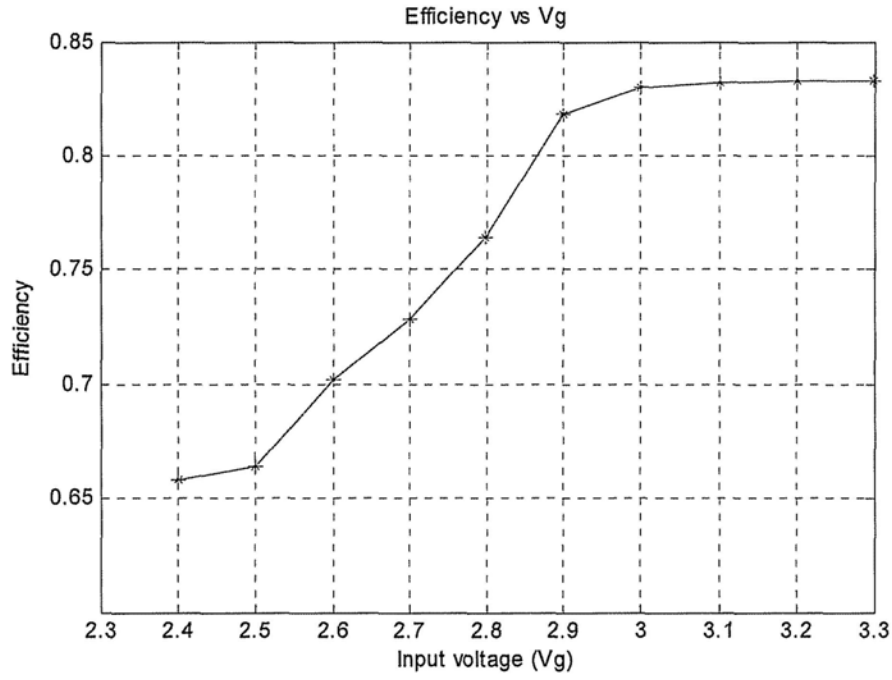



Fig. 3-42 Efficiency for different input voltages
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 66mA, $I_{o3}$ = 53mA and $I_{o4}$ = 53mA).

From the efficiency plots shown in Fig. 3-40 to Fig. 3-42, it is found that the efficiency decreases as total power increases. For the same output power, due to different power distribution in the sub-converters, efficiency will also vary (the reason of this is shown in Fig. 3-17). This induces the ringing in Fig. 3-41. Finally, similar to the design in Chapter 2, efficiency will increase with input voltage increases due to the lower average inductor current.

2. Line regulation with Channel 3 working in different modes shown in Figs. 2-52(a) to 2-52(l) which are measured at $V_{o1}$ = 3.4V, $V_{o2}$ = 3V, $V_{o3}$ = 2.4V, $V_{o4}$ = 1.77V, $I_{o1}$ = 50mA, $I_{o2}$= 64mA, $I_{o3}$ = 35mA, $I_{o4}$ = 226mA.

As shown in Figs. 3-43 (a) to 3-43(e), the inductor-current waveforms show that the SIQO converter operates in buck-dominated mode, which is corresponding to a input voltage changing from 3.3V to 2.9V. From 3-43(f) to 3-43(k), the SIQO converter operates in boost-dominated mode, which is corresponding to the input

voltage changing from 3.3V to 2.9V. During the input voltage decreases, the average inductor current is found to be increasing (shown in the measurement of P1: mean (C1)). This is the reason to explain the efficiency plot in Fig. 3-42. Moreover, these line regulation results verifies that the transition from boost-dominated to buck-dominated is related to the input voltage, the output voltage, the sub-channel loading current, frequency, etc.. The switching boundary is ambiguous. As a result, it is needed to include also these uncertainty to the feedback loop, and in this design, tail current control handle its seamless transition.

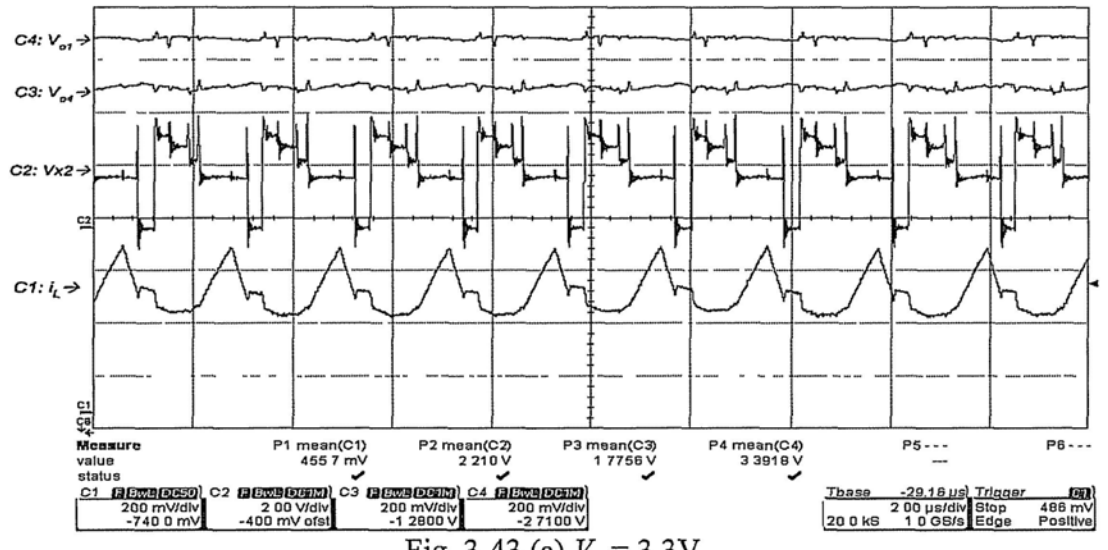


Fig. 3-43 (a) $V_g = 3.3$V.

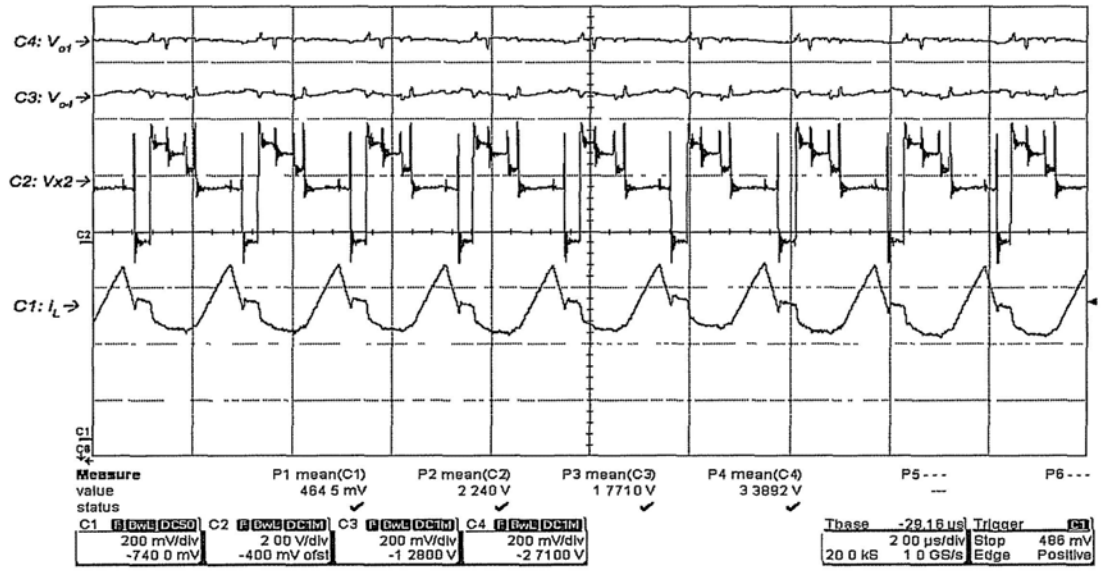


Fig. 3-43 (b) $V_g = 3.2$V.

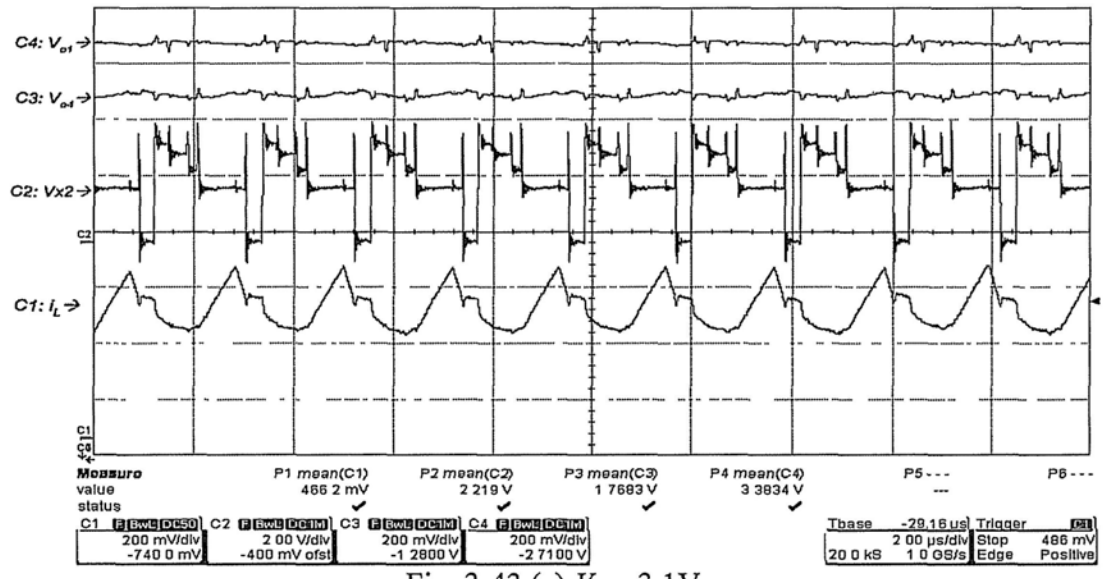



Fig. 3-43 (c) $V_g = 3.1$V.

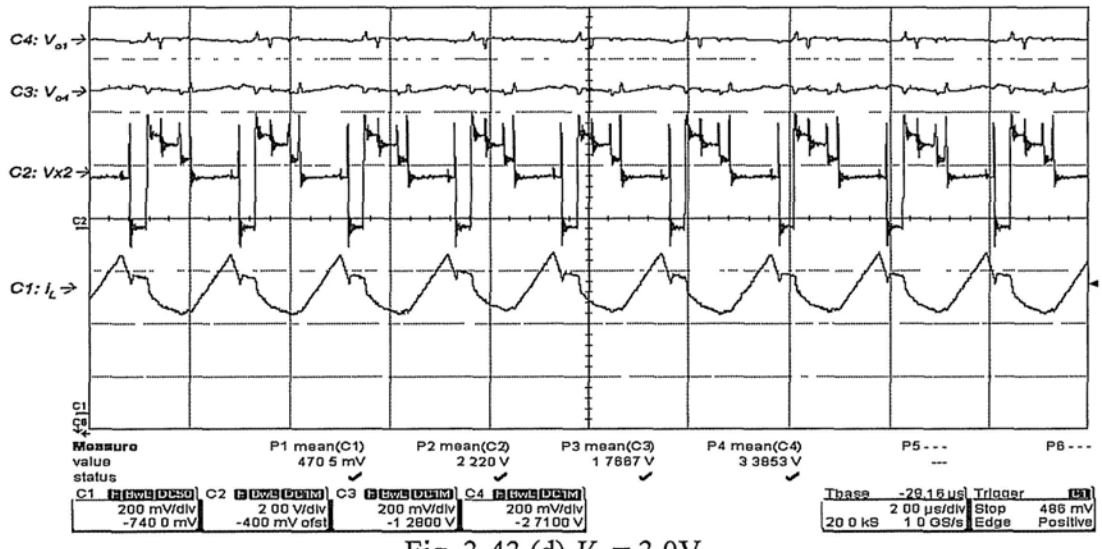



Fig. 3-43 (d) $V_g = 3.0$V.

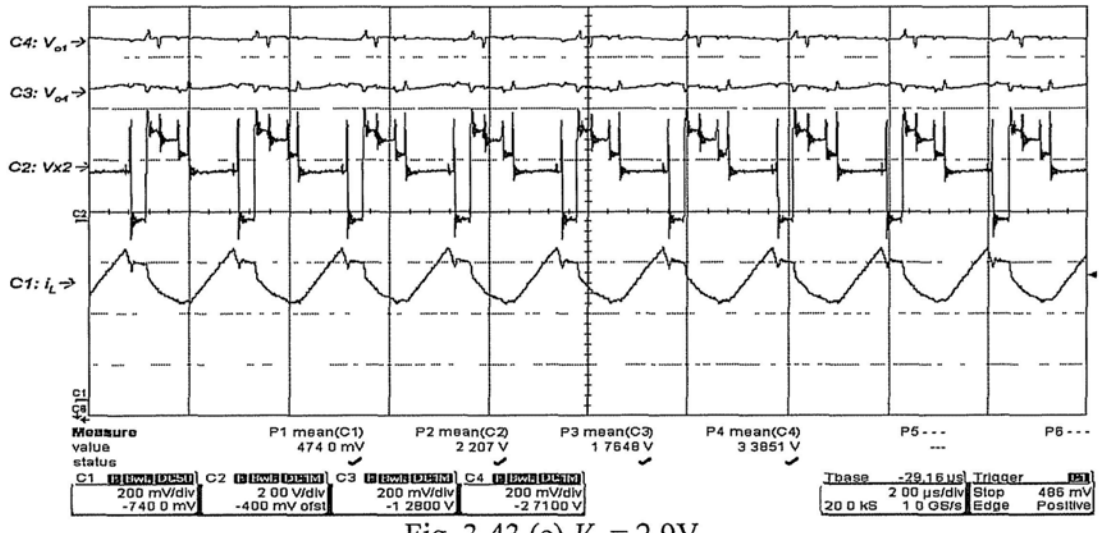



Fig. 3-43 (e) $V_g = 2.9$V.

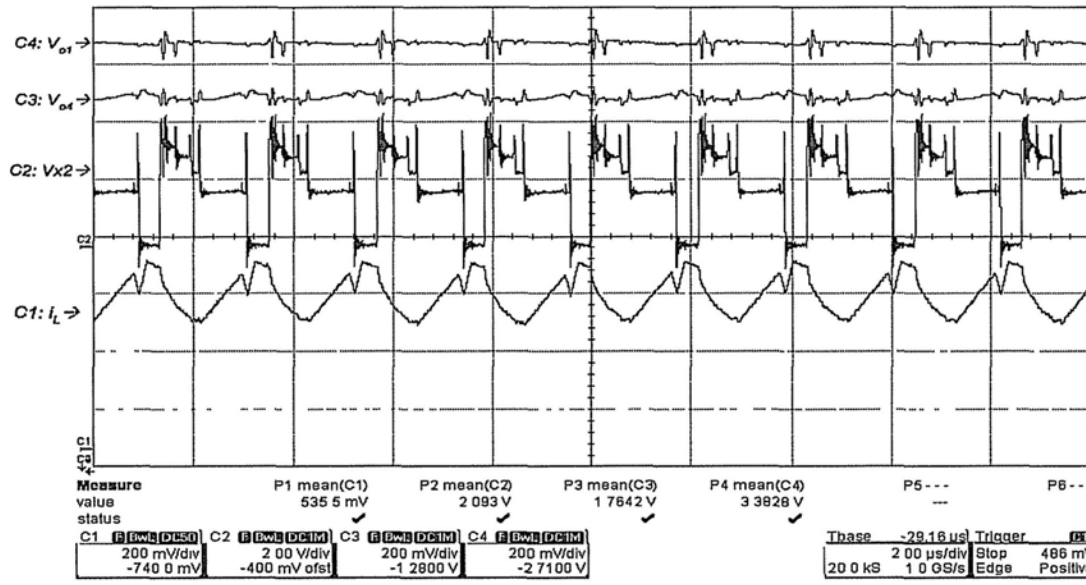



Fig. 3-43 (f) $V_g$ = 2.8V.

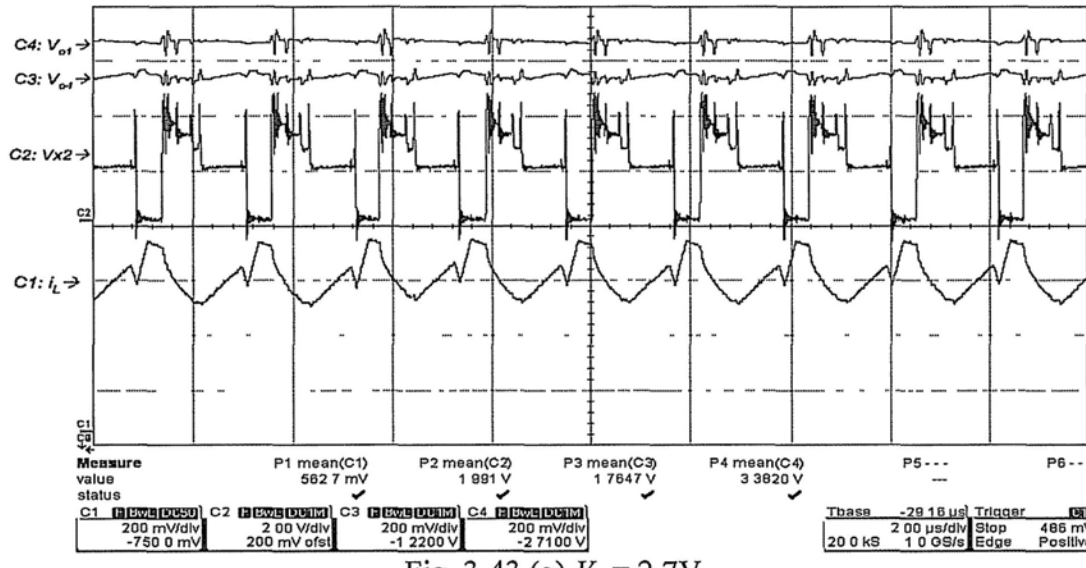



Fig. 3-43 (g) $V_g$ = 2.7V.

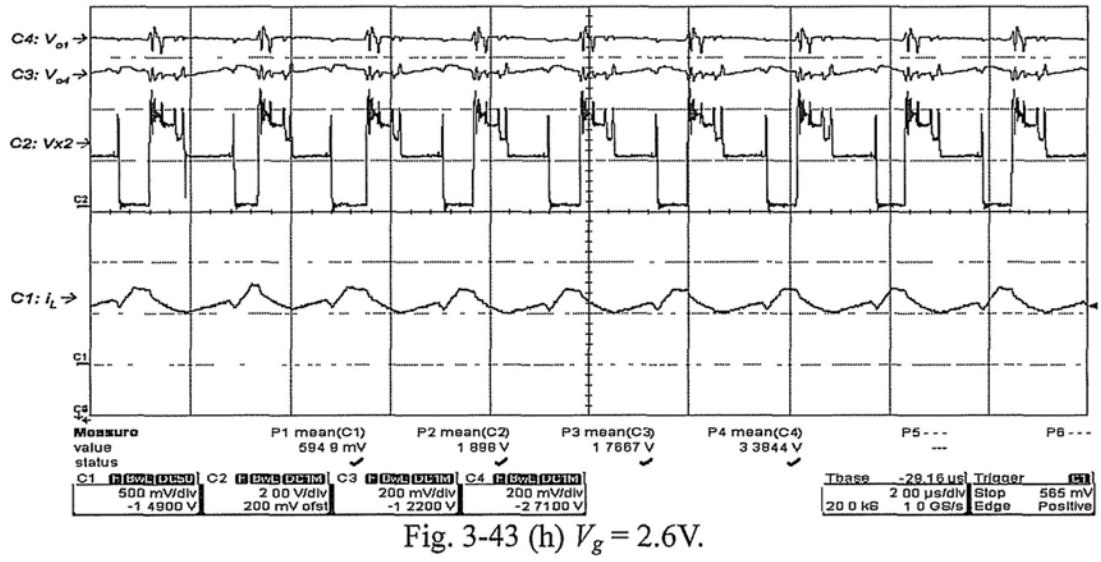



Fig. 3-43 (h) $V_g$ = 2.6V.

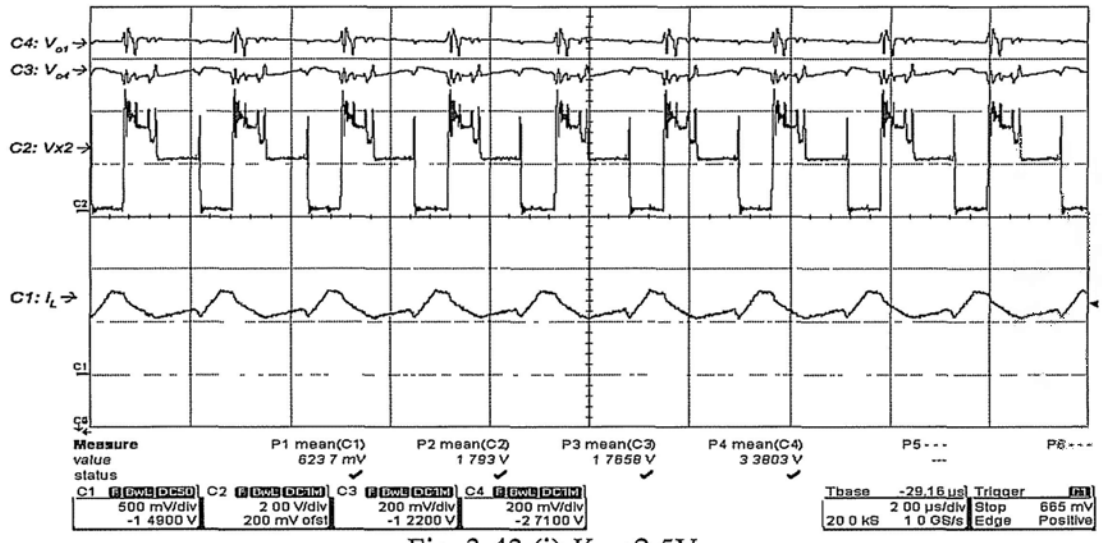



Fig. 3-43 (i) $V_g = 2.5$V.

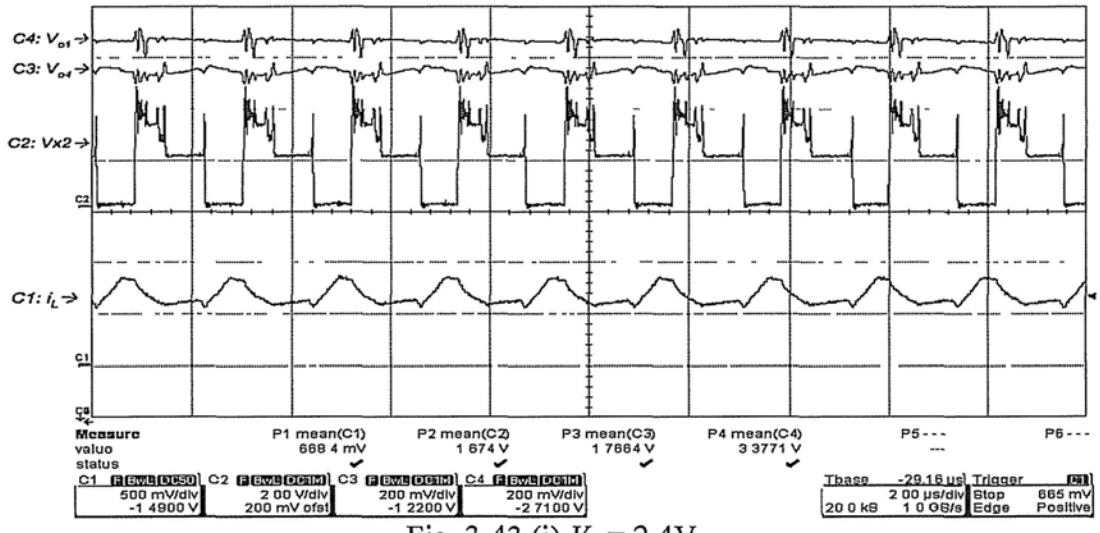



Fig. 3-43 (j) $V_g = 2.4$V.

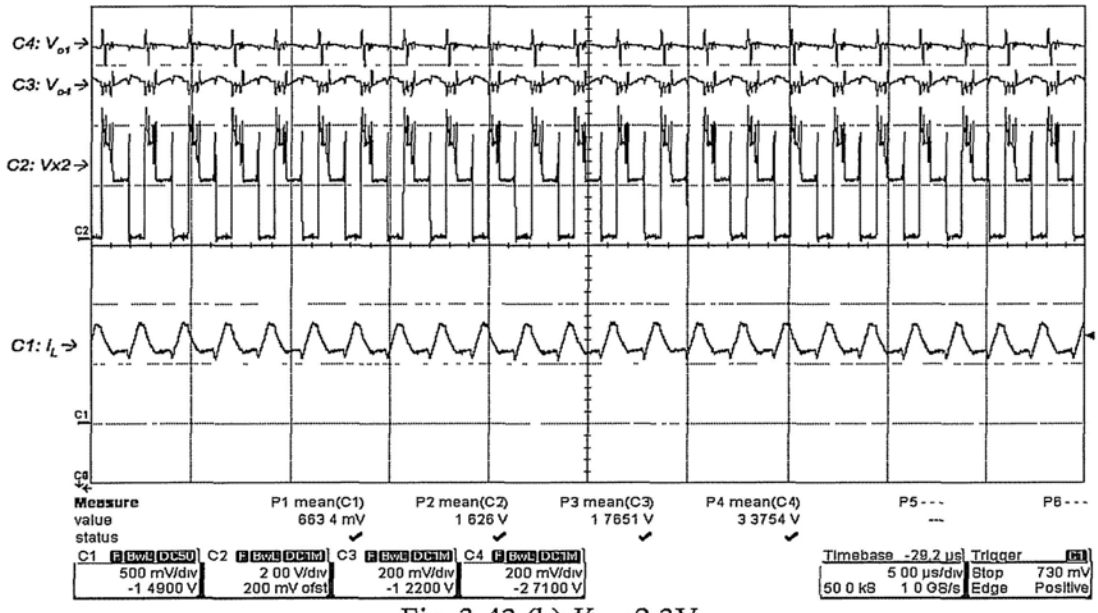



Fig. 3-43 (k) $V_g = 2.3$V.

3. $V_{x1}$-control when $V_{o1}$ in relative light load

In the two plots shown below, it is found that the SIQO operates in buck-dominated mode. Moreover, the last channel (.i.e. $V_{o4}$) has a relative light load. As a result, $V_{x1}$-controller make $V_{x1}$ tie to the ground (the moment inductor current start to fall down) in its operation period.

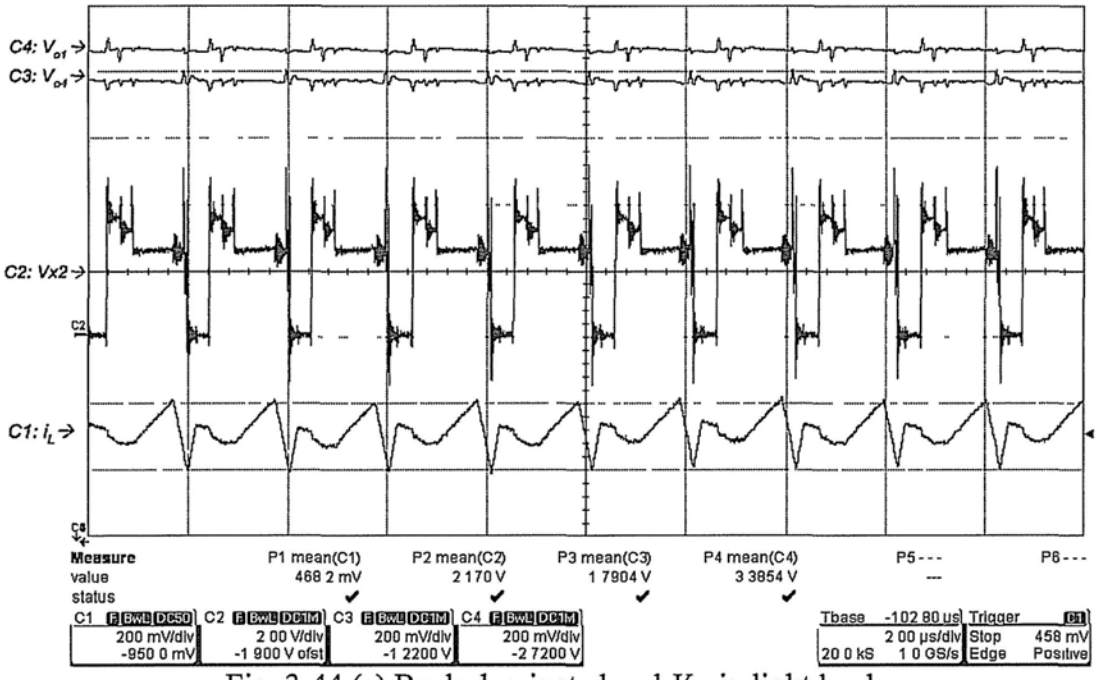



Fig. 3-44 (a) Buck-dominated and $V_{o1}$ in light load
(measured at $I_{o1}$ = 50mA, $I_{o2}$ =35mA, $I_{o3}$ = 250mA and $I_{o4}$ = 12mA).

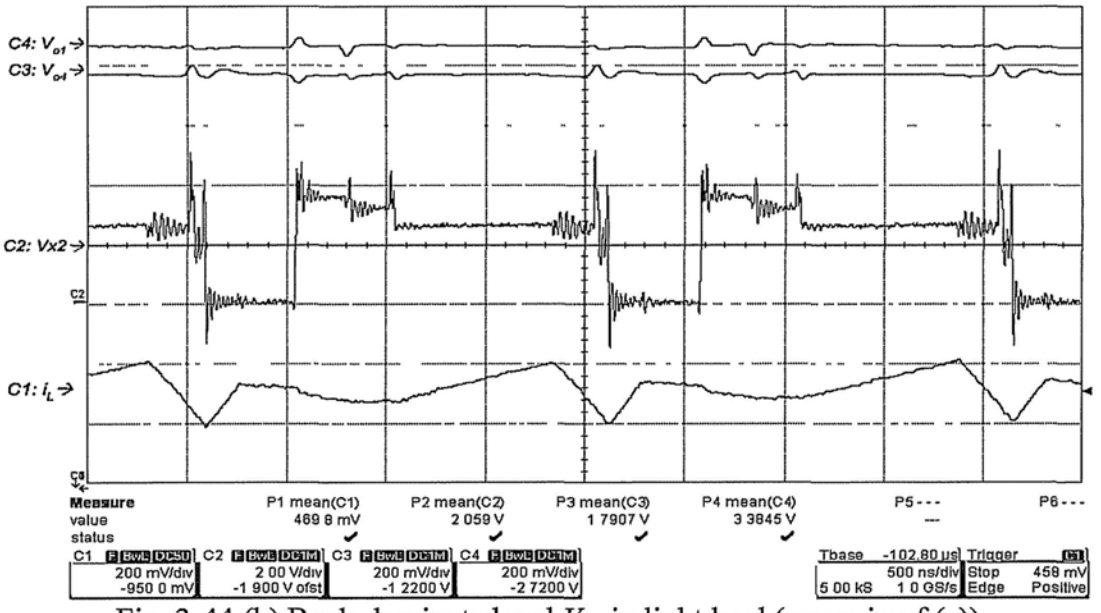



Fig. 3-44 (b) Buck-dominated and $V_{o1}$ in light load (zoom-in of (a))
(measured at $I_{o1}$ = 50mA, $I_{o2}$ =35mA, $I_{o3}$ = 250mA and $I_{o4}$ = 12mA).

2. Change of output channel sequence.

Figs. 3-45(a) and 3-45(b) show the steady state when changing the output voltage sequence of Channel 3 and Channel 4. It is obvious that the SIQO converter's operation is independent of the channel sequence. Normally, as demonstrated in the simulation in Section 3.2, it can fulfill the sub-converter type changing from full buck to full boost. Only one criterion is that $V_{o1}$ should tight to the highest voltage. Since the fixed subtracted connection is used in this design for reducing layout complexity. More about substrate technique can be referred to [2]

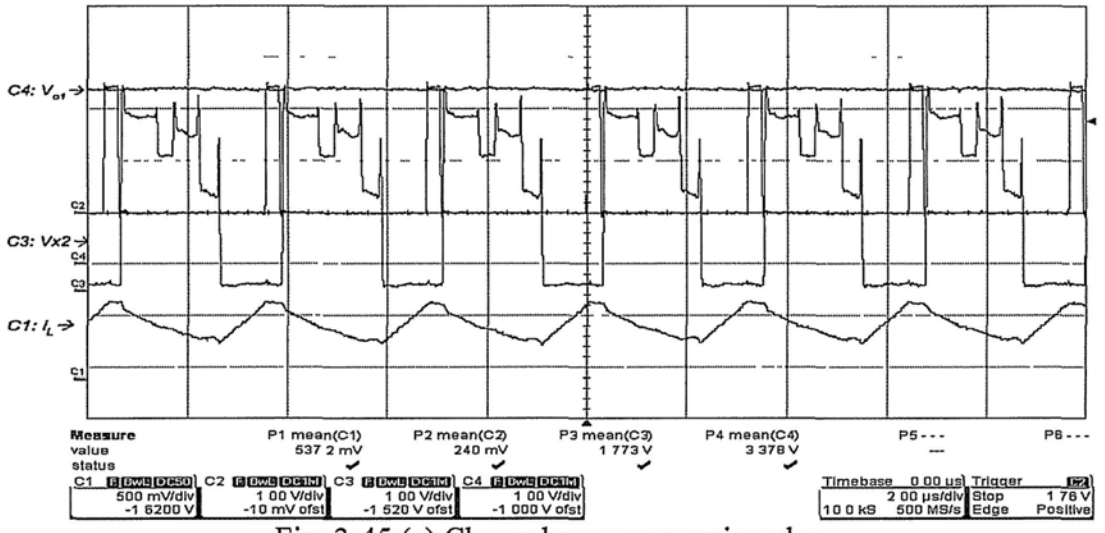



Fig. 3-45 (a) Channel sequence assigned as
$V_{o1} = 3.4\text{V}$, $V_{o2} = 2.4\text{V}$, $V_{o3} = 3\text{V}$, $V_{o4} = 1.77\text{V}$.

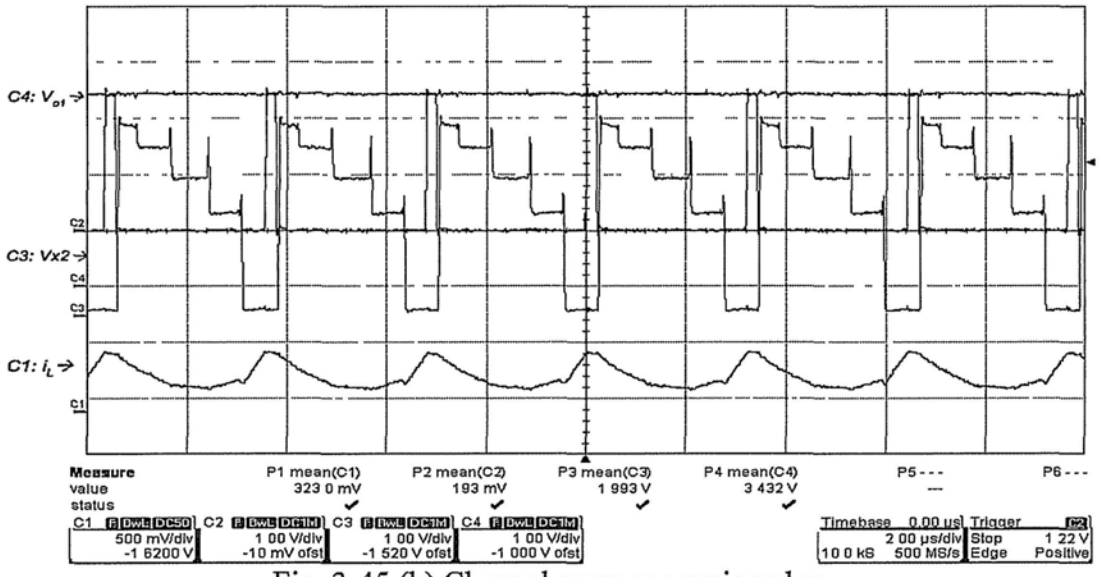



Fig. 3-45 (b) Channel sequence assigned as
$V_{o1} = 3.4\text{V}$, $V_{o2} = 3\text{V}$, $V_{o3} = 2.4\text{V}$, $V_{o4} = 1.77\text{V}$.

4. Dummy switching for tail-current control.

In Fig. 3-46 and Fig. 3-47, the switching node of inductor is shown. In Fig. 3-46, there is a short period of $V_{x1}$ which is tied to the ground. This is the dummy switching which used to complete the proposed tail-current control algorithm. As described in Section 3.4, it maintains the system's operation immune of current sensor mismatch. Its duration (100 – 200ns in this design), which is related to the settling time of the current sensor and the comparator delay, is a violation to optimal switching sequence. It is one reason for lower efficiency when frequency increases.

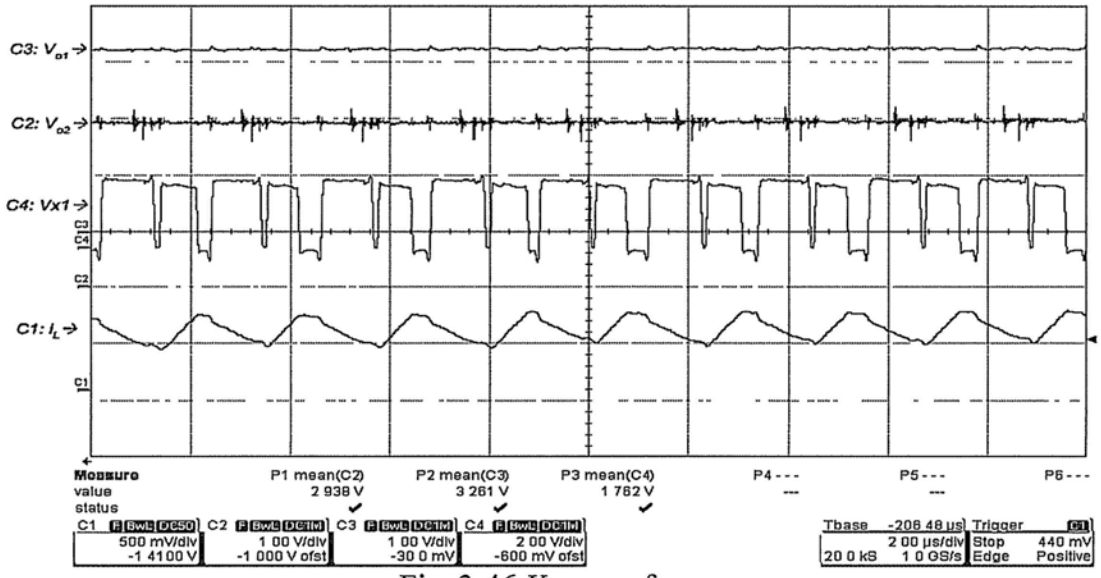



Fig. 3-46 $V_{X1}$ waveform
(measured at $I_{o1}$ = 118mA, $I_{o2}$ = 44mA, $I_{o3}$ = 26mA and $I_{o4}$ = 26mA).

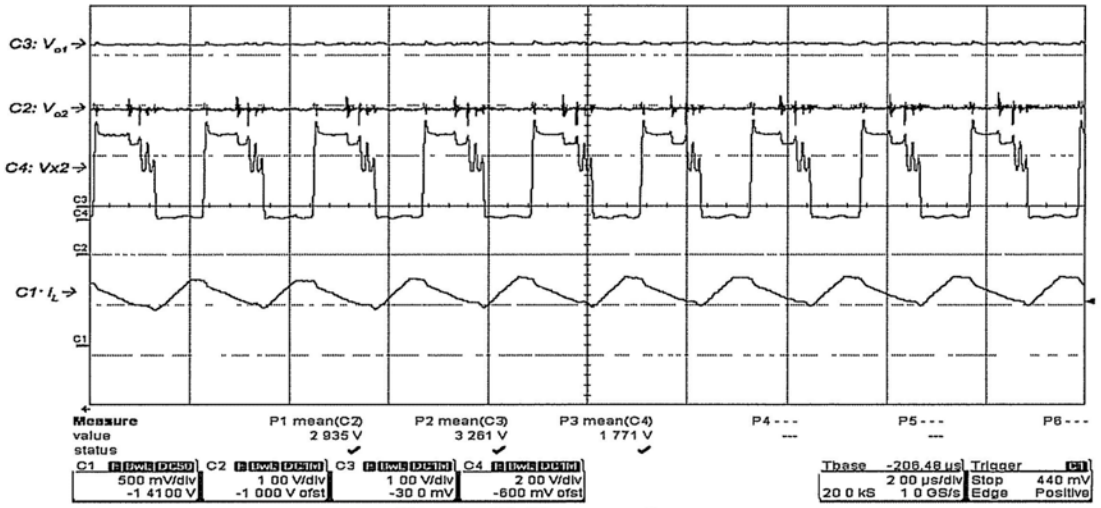



Fig. 3-47 $V_{X2}$ waveform
(measured at $I_{o1}$ = 118mA, $I_{o2}$ = 44mA, $I_{o3}$ = 26mA and $I_{o4}$ = 26mA).

5. Start-up

Fig. 3-48 and Fig. 3-49 show the start-up of the system with different loadings. Its mechanism is similar to that used in last design. From Fig. 3-49, it is found that current limit is triggered and all channels will start up and settle within 400μs.

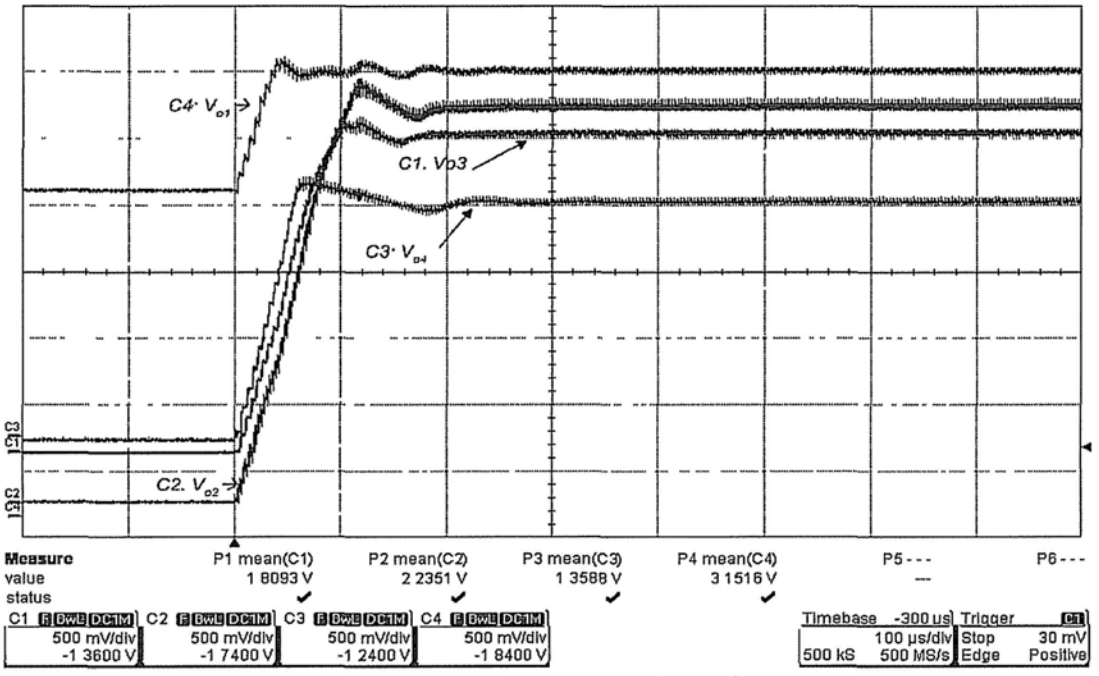



Fig. 3-48 Start-up of 4 channels
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

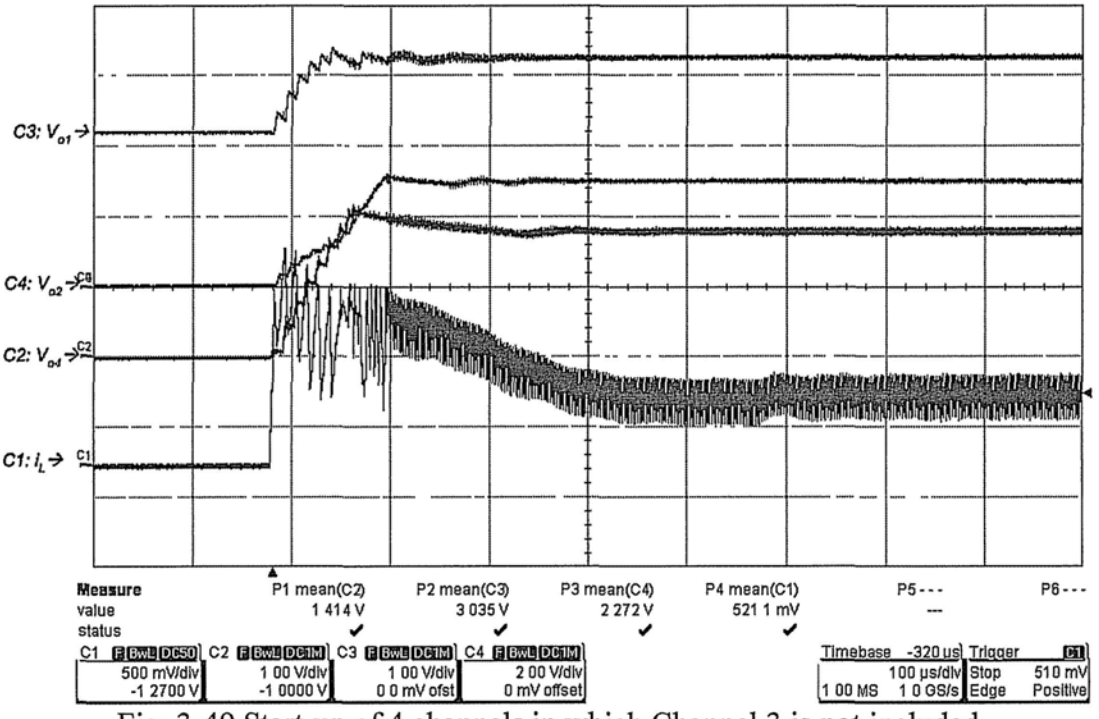



Fig. 3-49 Start-up of 4 channels in which Channel 3 is not included
(measured at $I_{o1}$ = 118mA, $I_{o2}$ = 44mA, $I_{o3}$ = 26mA and $I_{o4}$ = 26mA).

6. Load transient response

The loading transient response of different channels is shown in Figs. 3-50 to 3-55. Moreover, the cross-regulation to other channels during transient is also monitored. The details of the data are listed in Table 3-11.

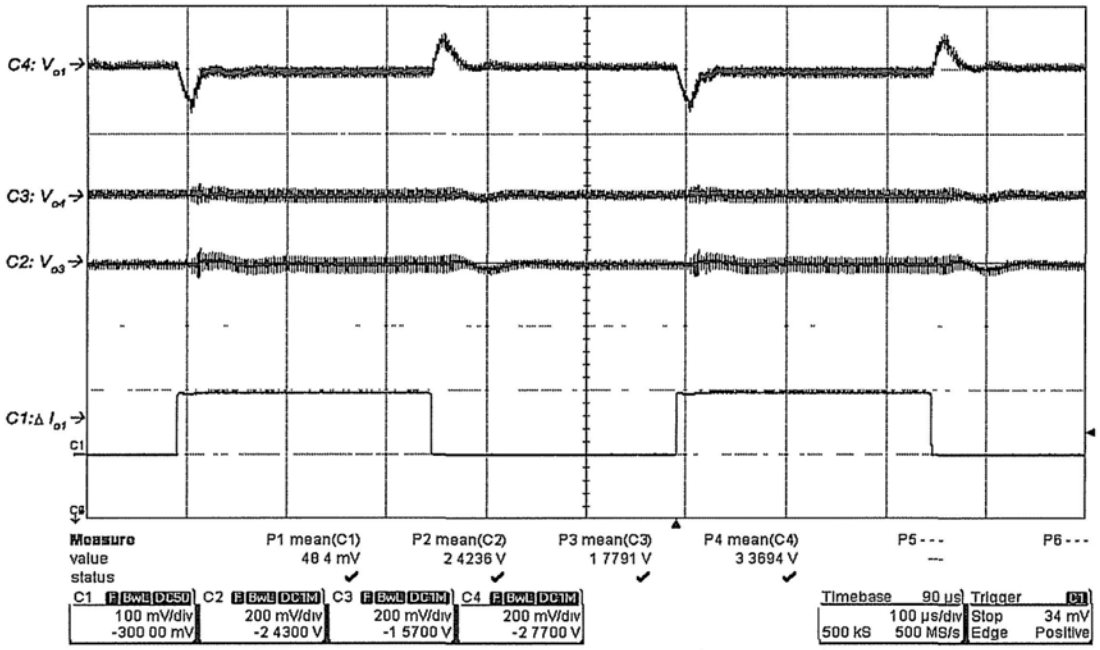



Fig. 3-50 $V_{o1}$ undergoing a 100-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

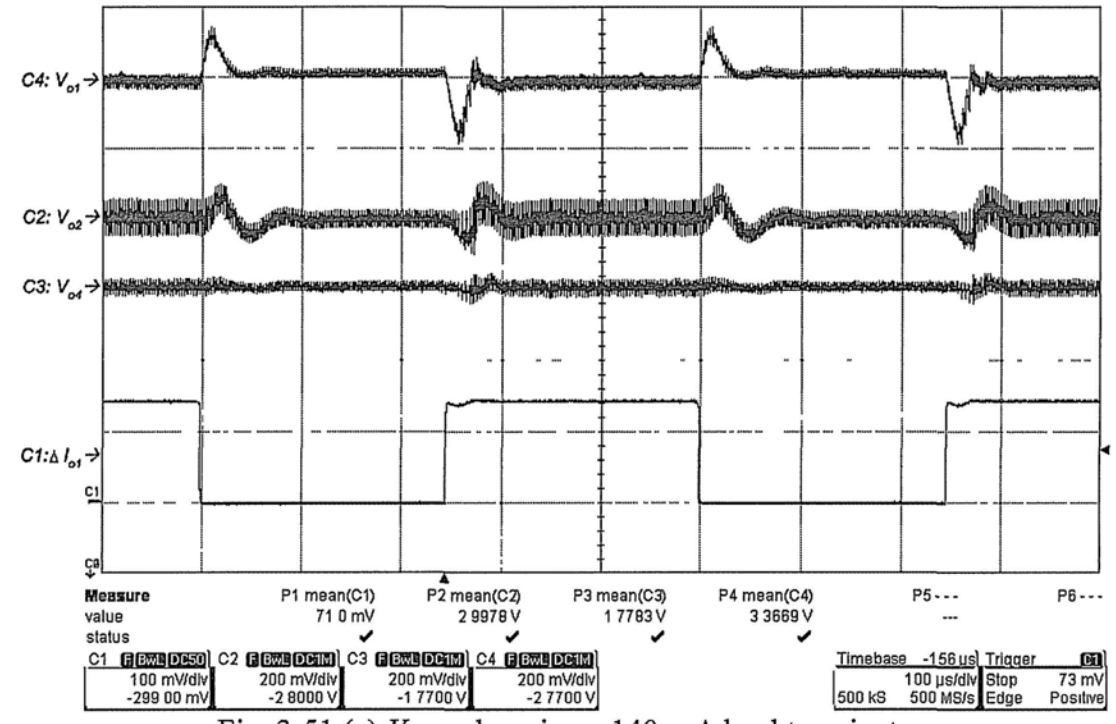



Fig. 3-51 (a) $V_{o1}$ undergoing a 140-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

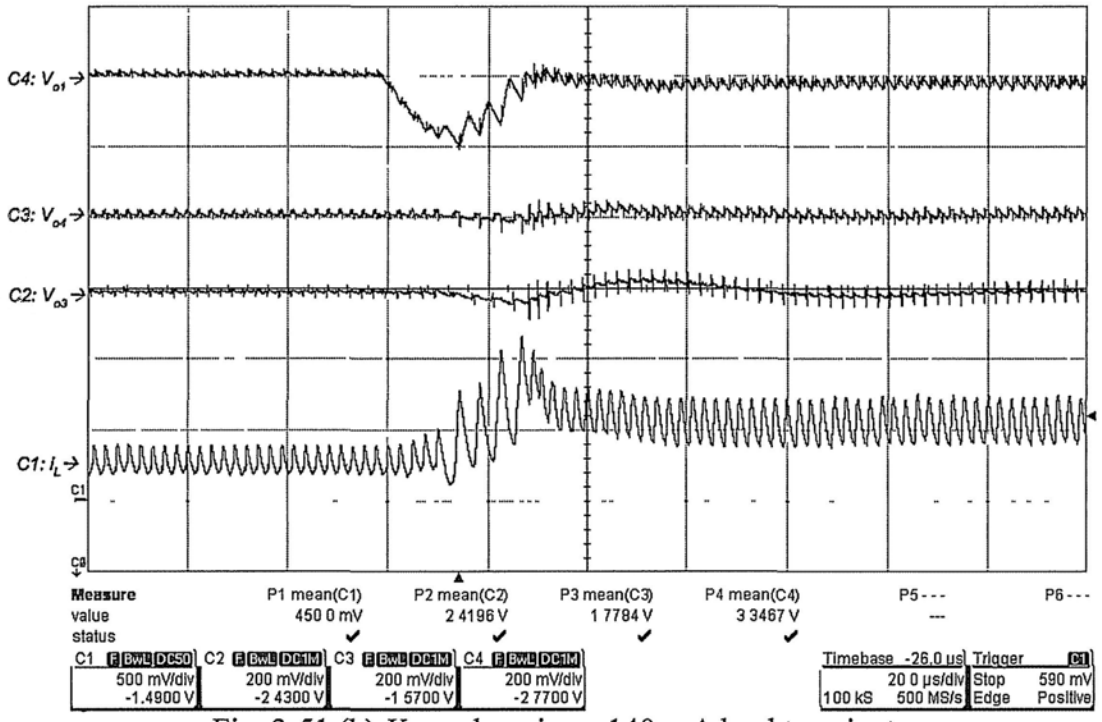



Fig. 3-51 (b) $V_{o1}$ undergoing a 140-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

The above plot shows the inductor current during loading transient of $V_{o1}$. It is found that the operation period is enlarged and return to reference period after it is settled.

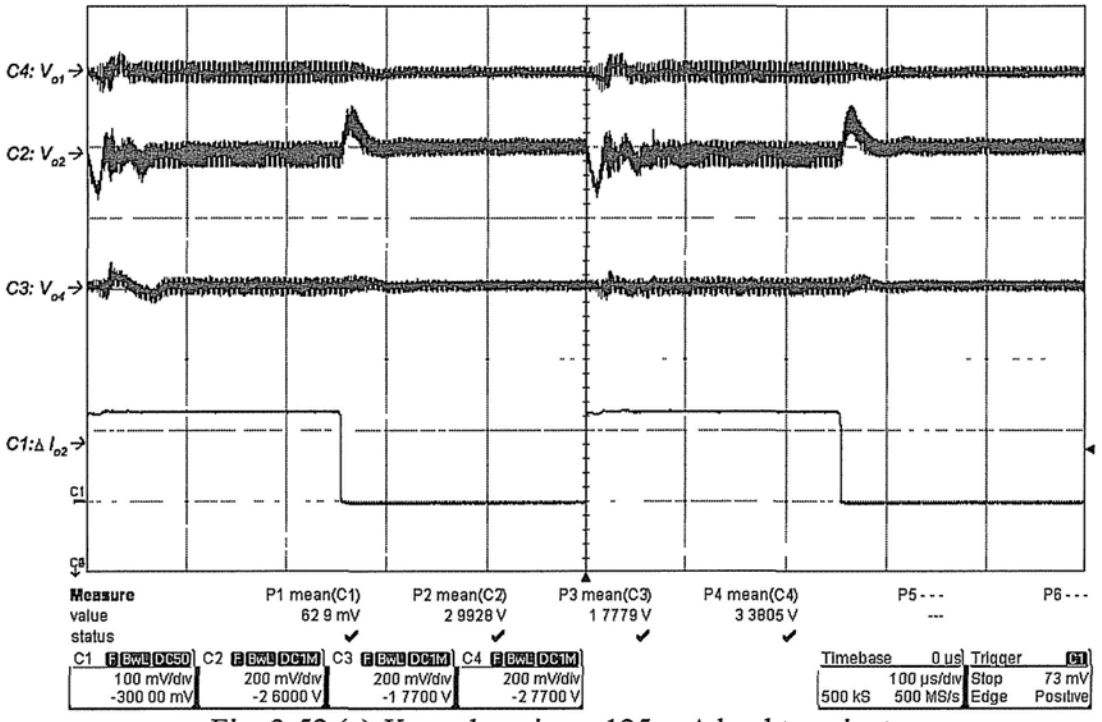



Fig. 3-52 (a) $V_{o2}$ undergoing a 125-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

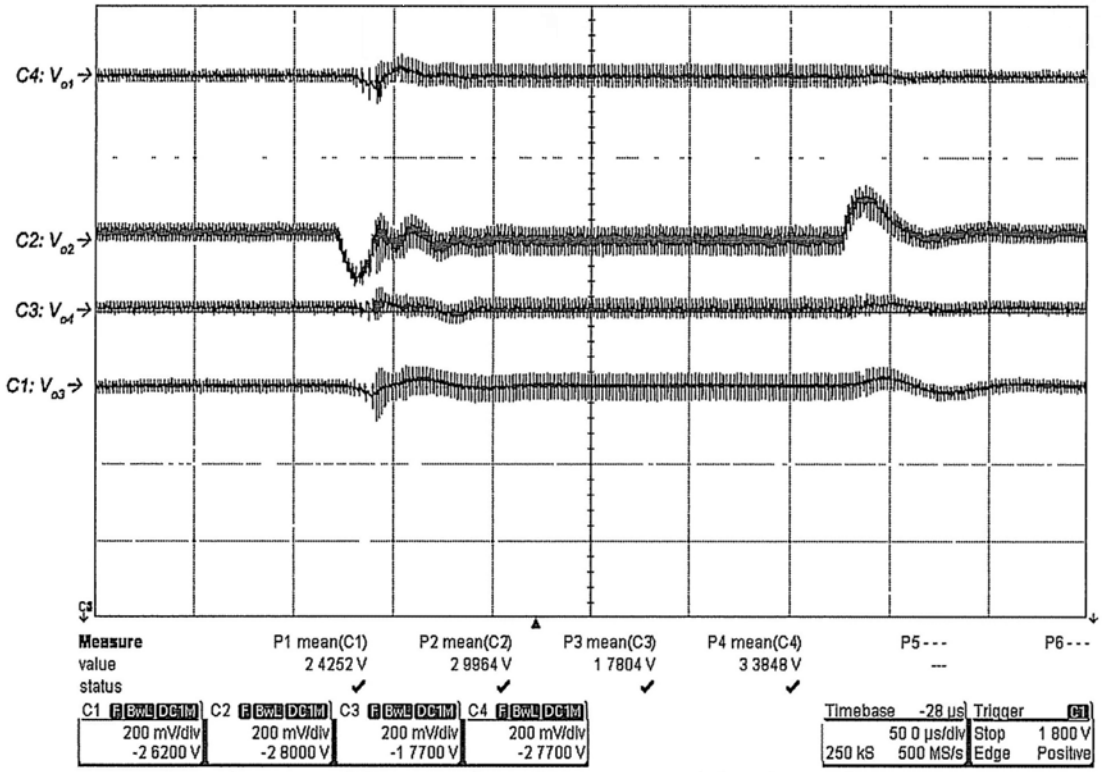



Fig. 3-52 (b) $V_{o2}$ undergoing a 125-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

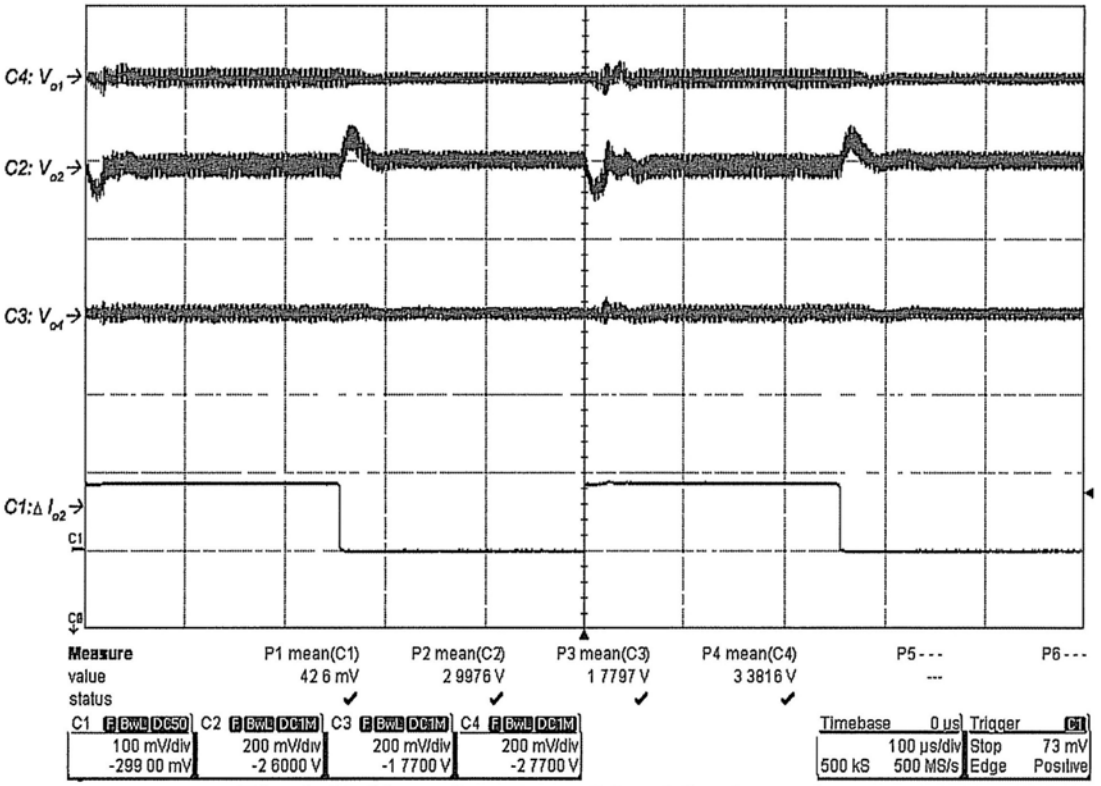



Fig. 3-53 $V_{o2}$ undergoing a 85-mA load transient
(measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

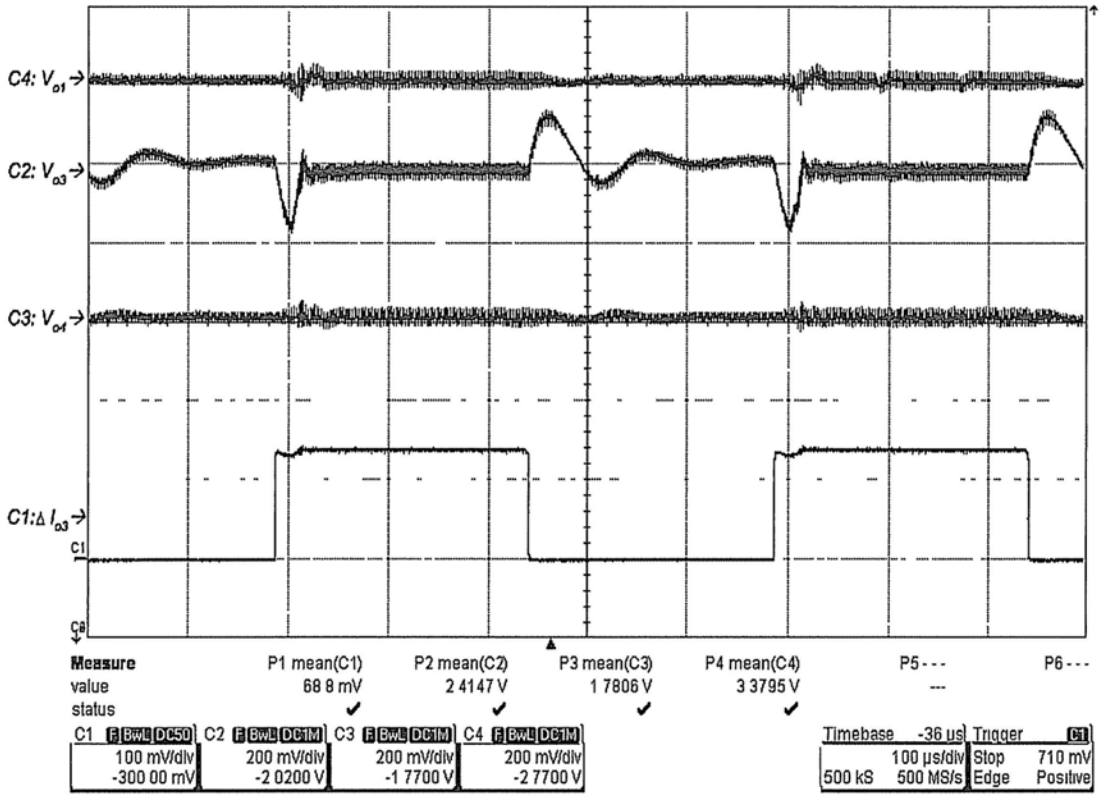



Fig. 3-54 (a) $V_{o3}$ undergoing a 140-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

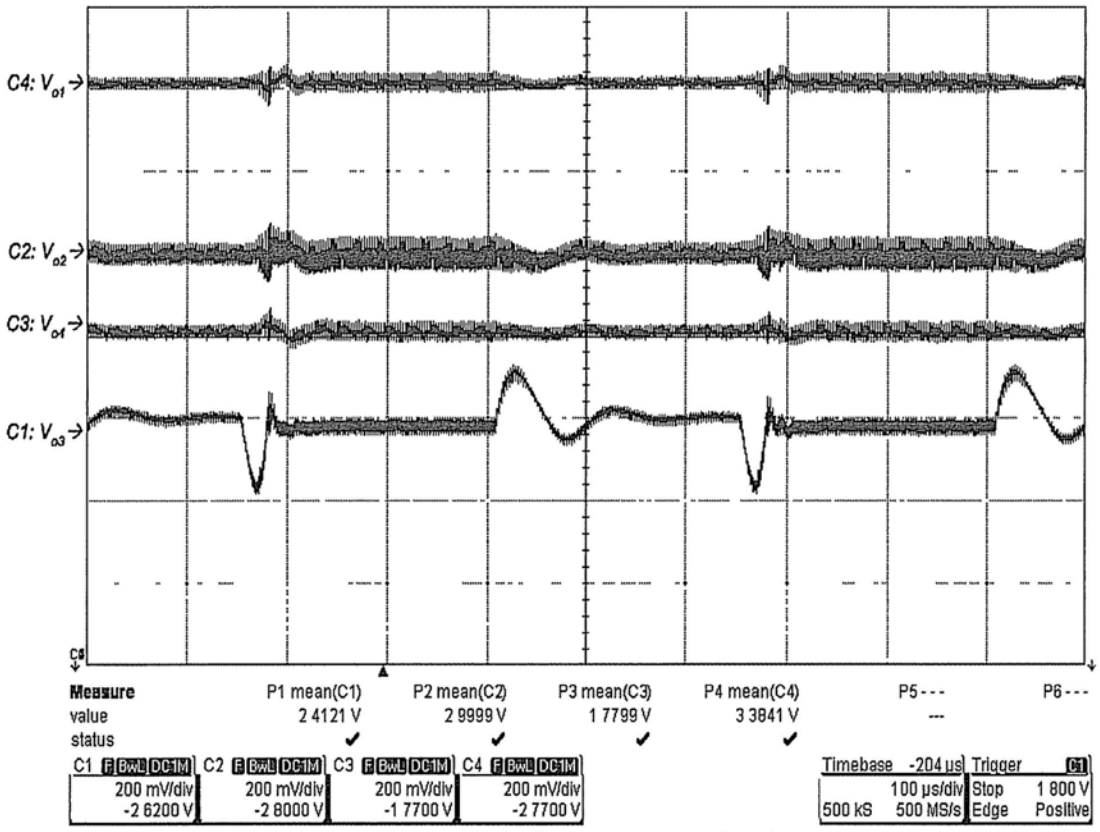



Fig. 3-54 (b) $V_{o3}$ undergoing a 140-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

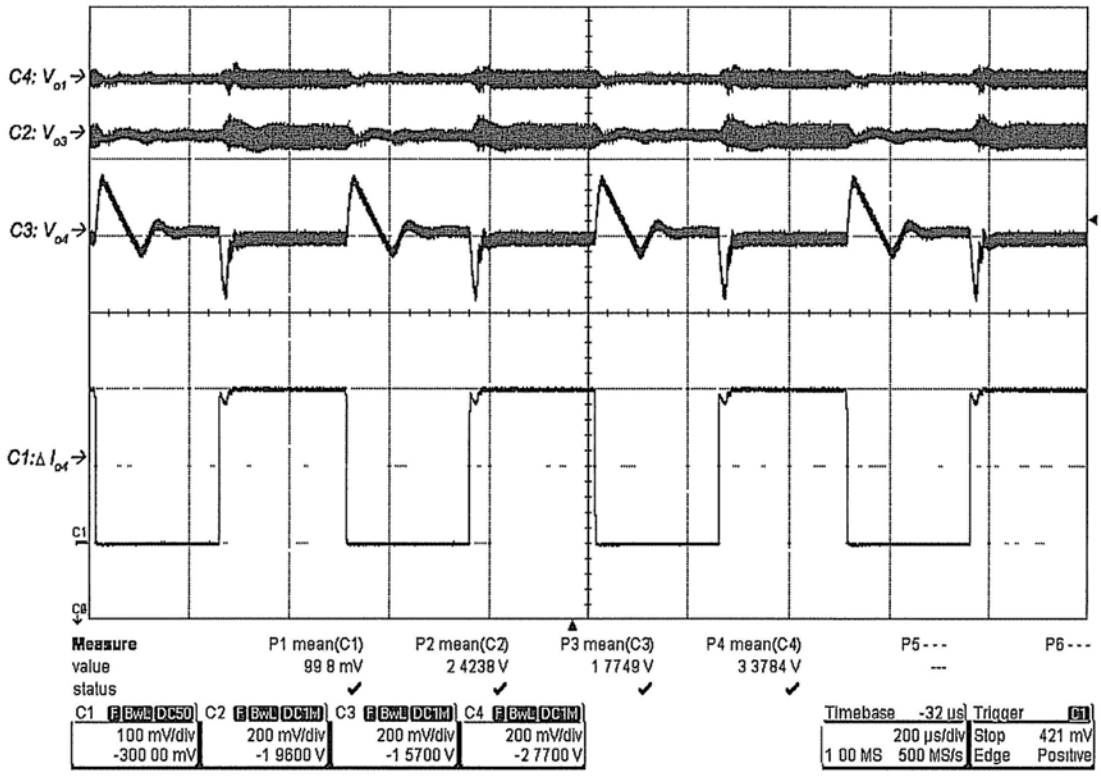



Fig. 3-55 (a) $V_{o4}$ undergoing a 200-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

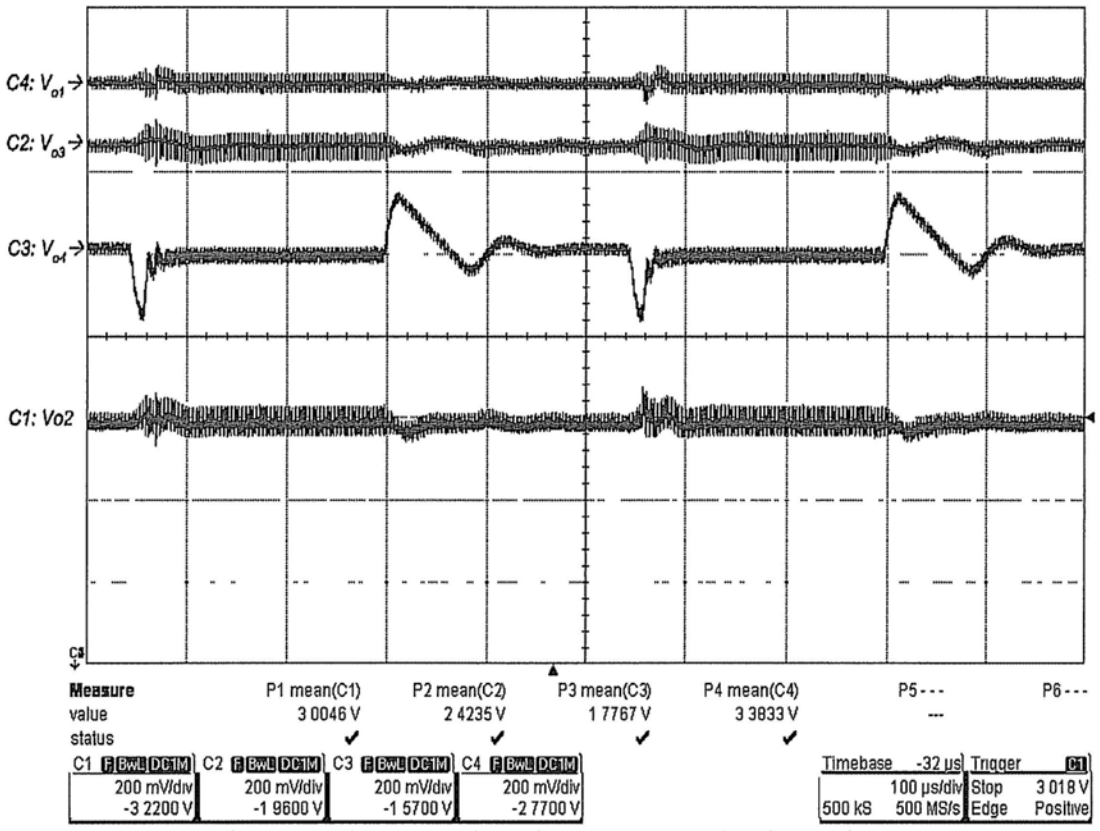



Fig. 3-55 (b) $V_{o4}$ undergoing a 200-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

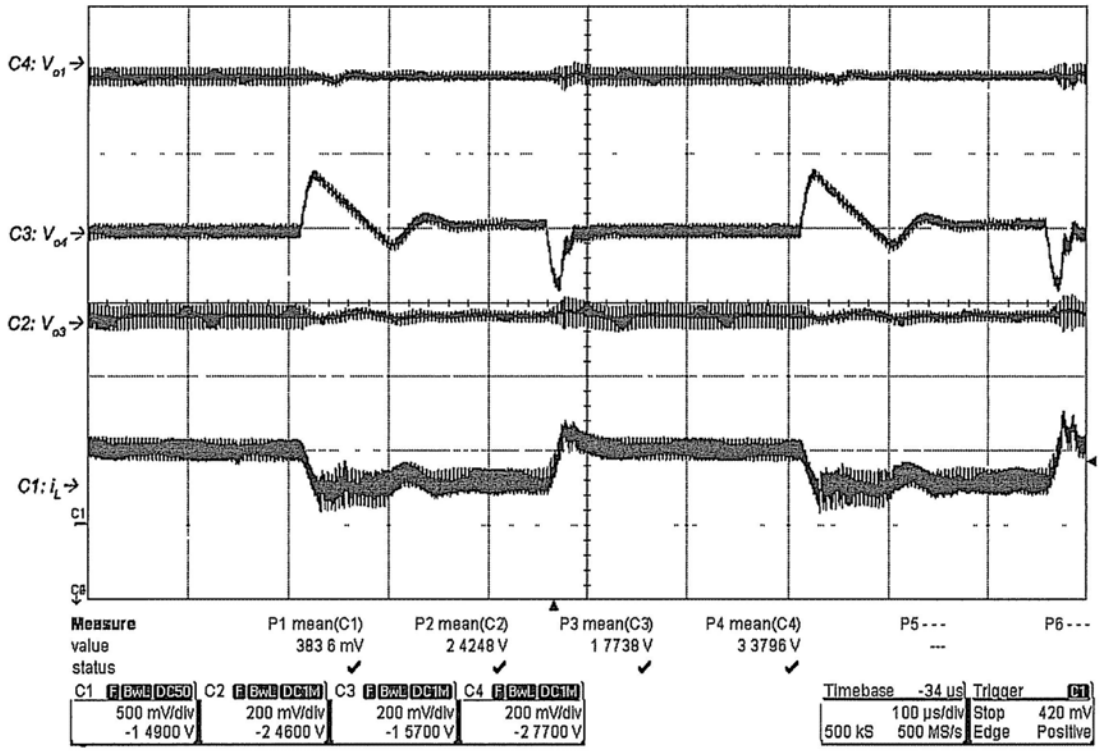



Fig. 3-55 (c) $V_{o4}$ undergoing a 200-mA load transient (measured at $I_{o1}$ = 50mA, $I_{o2}$ = 64mA, $I_{o3}$ = 35mA and $I_{o4}$ = 26mA).

Table 3-11 Measured transient voltage changes ($L_0$ =3.3uH, $C_o$ = 10uF × 4).

| | $V_{o1}$ (mV) | $V_{o2}$ (mV) | $V_{o3}$ (mV) | $V_{o4}$ (mV) |
|---|---|---|---|---|
| 100mA transient @ Channel 1 | 100 | N/A | 10 | 10 |
| 140mA transient @ Channel 1 | 160 | 50 | 40 | 20 |
| 85mA transient @ Channel 2 | 10 | 70 | N/A | 10 |
| 125mA transient @ Channel 2 | 20 | 120 | 20 | 10 |
| 140mA transient @ Channel 3 | 20 | 20 | 180 | 20 |
| 200mA transient @Channel 4 | 20 | 20 | 20 | 140 |

The performance of some recently-reported state-of-art SIMO designs are summarized in Table 3-12. The design in [3] is a digital controlled SIDO converter. It inserts a sensed inductor current signal into the voltage feedback loop which attenuates the cross-regulation during loading transient. The design in [5] is an auto buck-boost converter without the need to pre-define the type of the sub-converter. However, it needs an additional inductor discharge path formed by an extra inductor,

a diode, a switch and a capacitor which increase the cost of production. Moreover, its efficiency will be degraded seriously when the total power stage is buck-dominated. The design in [6] has similar problem as the design in [5] does. Moreover, it requires preliminary information of the type of the sub-converters. The advantage and limitation of design [4] and [7] have been presented in Chapter 2.

Table 3-12 Performance comparison.

| | 2008 [3] | 2008 [4] | 2009 [5] | 2009 [6] | 2010 [7] | This work |
|---|---|---|---|---|---|---|
| Type of inductor waveform | Class-2 | Class-2 | Class-2 | Class-2 | Class-2 | Class-2 |
| Channel number | 2 | 2 | 5 | 4 | 6 | 4 |
| Sub-converter type | Buck | Boost (bipolar) | Buck & boost | Buck & boost | Buck | Buck & boost |
| Auto buck-boost | No | No | Yes (need additional discharge path) | No | No | Yes |
| Switching frequency | 0.5MHz | 0.8MHz | 1MHz (not fixed) | 0.66MHz | 2MHz | 0.3MHz |
| IC technology | FPGA | 0.5μm BiCMOS | 0.5μm BiCMOS | 0.25μm CMOS | 0.35μm CMOS | 0.35μm CMOS |
| Input voltage | 2.5 – 5V | 2.7 – 4.5V | 2.5 – 4.5V | 1.8 – 2.2V | 5V | 2.3 – 3.3V |
| Output voltages | 0.9V – 1.5V | -4.8V & 4.8V | 2 – 9.5V | 1.25V, 1.35V, 2V & 2.25V | 1V, 1.3V, 1.6V, 1.9V, 2V & 3V | 1.77V, 2.4V, 3V & 3.4V |
| Maximum output power | N/A | N/A | 1.5W | 0.69W | N/A | 1.66W |
| Peak efficiency | N/A | 81%@250mA | 83% | 93% | N/A | 89% |
| Transient voltage change and settling time | 220mV &60us @$\Delta I_o$ = 400mA | 100mV & 25μs @$\Delta I_o$ = 100mA | N/A | N/A | 75mV & 100μs @$\Delta I_o$ = 71mA | refer to Table 3-7 |

For the design presented in this chapter, it is found that it can support a wide input and output-loading range. Moreover, it achieves auto buck-boost based on the optimized Class-2 SIMO switching sequence. Its transient response is competitive to the state-of-art SIMO converter design without suffering from some specified preliminary settings. Comparing to the design in Chapter 2, it has advantages such as higher efficiency, higher operation frequency enabled, higher channel capability, smaller switching times and lower requirement for current-sensor matching. However, comparing to the Class-1 SIMO design, it has disadvantages such as high

correlated power stage, complexity in the compensator design, unpredictable inductor-current waveform and difficult to operate in DCM.

## Conclusion of Chapter

A fixed-frequency SIQO arbitrary type dc-dc converter with wide loading range and with efficient switching sequence has been introduced in this chapter. The principle of operation of the proposed dc-dc converter has been given and the performance of the dc-dc converter has been verified by experimental results.

## References


[1] T. Li, "Single inductor multiple output boost regulator," *U.S. Patent 6075295*, Jun. 13, 2000.

[2] M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovarti, T. Peltola and T. Teppo, "A 4-output single-inductor DC-DC buck converter with self–boosted switch drivers and 1.2A total output current," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 444 445.

[3] D. Trevisan, P. Mattavelli, P. Tenti, "Digital control of single-inductor multiple-output step-down DC–DC converters in CCM," *IEEE Trans. Industrial Electronics*, vol. 55, no. 9, pp. 3476 3483, Sep. 2008.

[4] Y.-J. Woo, H.-P. Le, G.-H. Cho, G.-H. Cho and S.-I. Kim, "Load independent control of switching dc-dc converters with freewheeling current feedback," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 446 626.

[5] K.-S. Seol, Y.-J. Woo, G.-H. Cho, G.-H. Cho, J.-W. Lee and S.-i. Kim, "Multiple-output step-up down switching DC-DC converter with vestigial current control," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 442, 443 & 443a.

[6] M.-H. Huang and K.-H. Chen, "Single-inductor multi-output (SIMO) DC-DC converters with high light-load efficiency and minimized cross-regulation for portable devices," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1099 1111,

Apr. 2009.

[7] K.-C. Lee, C.-S. Chae, G.H. Cho and G.-H. Cho, "A PLL-based high-stability single-inductor 6-channel output DC-DC buck converter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 200 201.

# Chapter 4

# Conclusion and Future work

## 4.1 Conclusion

In the previous chapters, the design and implementation of two types of SIMO dc-dc converters for general applications have been presented. Both of them can survive from the changes of the converter type and sub-channel loading. It makes them suitable for DVS applications and general independent sub-channel loading applications. Moreover, different from adding some power-consuming pre-settings such as constant offset inductor current, fixed output channel type or sequence, or using NIF control topology, both of the proposed two control methodologies make the SIMO converter operate in prior of using low average inductor current, which obeys the trend of green power operation for electronic devices.

The major contributions of this thesis are summarized as below:

1. A frequency control technique is used in Class-1 SIMO converter to suppress cross-coupling during loading transient and fulfil wide range loading application with lower average inductor current

2. An auto buck boost technique is used in Class-1 SIMO converter to enable sub-channel's converter type adaption.

3. Another frequency control technique is used in Class-2 SIMO converter to suppress cross-coupling during loading transient and fulfil wide range loading application with lower average inductor current.

4. Another auto buck boost technique is used in switching sequence optimized Class-2 SIMO converter for both buck-dominated and boost-dominated cases.

The accurate modeling of the proposed designs and bandwidth optimization will be further investigated in the future.

## 4.2 Prospect of Control Algorithm for SIMO Converter

It is found that the idea of variable frequency control in single-output buck converter referred in Chapter 1 is successfully applied to SIMO converter by using instantaneous varying switching period to distribute power to the sub-converters. There is a further question. The essential of the operation is to use an indirect method to redistribute the duty cycle in the flow as following: sub-channel duty period → total duty period → frequency difference → offset/tail inductor current tuning circuit → redistribution of the sub-channel duty period. According to this observation, the possibility of using a strictly fixed-frequency operation to achieve a similar performance is desirable. As a result, a fixed-frequency SIMO with internal duty cycle redistribution and $V_{x1}$ control is proposed in the following. Both the theory and simulation will be shown briefly in the following.

The simplified key control algorithm is shown in (4-1)

$$\begin{cases} d_n = \dfrac{e_n \cdot (1-r)}{\Sigma e_n} \\ c = (1-\Sigma e_n - r)\cdot H(s) \\ r = \begin{cases} -c & if\ c \le 0 \\ 0 & if\ c > 0 \end{cases} \\ f = \begin{cases} c & if\ c > 0 \\ 0 & if\ c \le 0 \end{cases} \end{cases} \tag{4-1}$$

where $e_n$ stands for the pre-duty cycle of each channel; $d_n$ stands for the post-duty cycle after redistribution; $c$ stands for an internal variable which integrates the error

caused by the overflow of the pre-duty cycle; $r$ stands for the duty cycle for charging inductor (i.e. SW_C); $f$ stands for the duty cycle for discharging inductor (i.e. SW_D). From this control algorithm, it is found that the duty cycle is immediately redistributed responding to any change of the duty cycle of the sub-channel. It ensures that the total period is equal to the switching period. As a result, a strict fixed-frequency operation can be achieved. Moreover, both $r$ and $f$ are variables which are used to control $V_{x1}$ switching. It is noted that either one of them will be equal to 0, which obeys the optimal switching sequence for low average inductor current. $H(s)$ is a compensator which can be implemented in continuous or discrete time form. Other than fixed-frequency operation, this design has a potential to implement at high-frequency operation since the inductor-current comparator is not used. Although current-sensing circuit is still needed for the compensator design, it will lower the requirement than that in the previous two designs. Some simulations of this proposed SIMO converter is shown below, with the same design requirement as in the previous two designs. The simulation setting is shown in Table 4-1.

Table 4-1 Simulation setting.

| | |
|---|---|
| Output voltages | $V_{o1}$ = 3.4V, $V_{o2}$ = 3V, $V_{o3}$ = 2.4V, $V_{o4}$ = 1.8V |
| Input voltage (nominal) | 2.5 |
| Inductor and its ESR | 4.7μH and 25mΩ (add 0.3Ω in series with the inductor to model the routing resistance) |
| Capacitor and its ESR for each channel | 10μF and 20mΩ |
| Operation frequency | 1MHz |

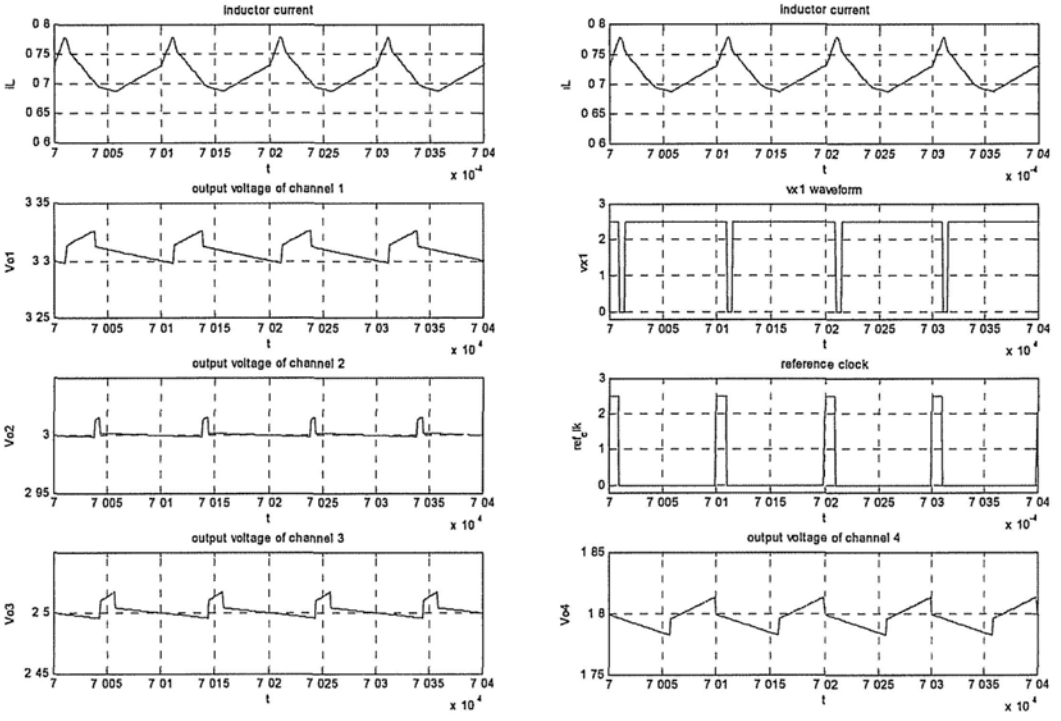



Fig. 4-1 Steady-state of Boost dominated
(measured at $Io1$ = 40mA, $Io2$ = 64mA, $Io3$ = 35mA and $Io4$ = 26mA).

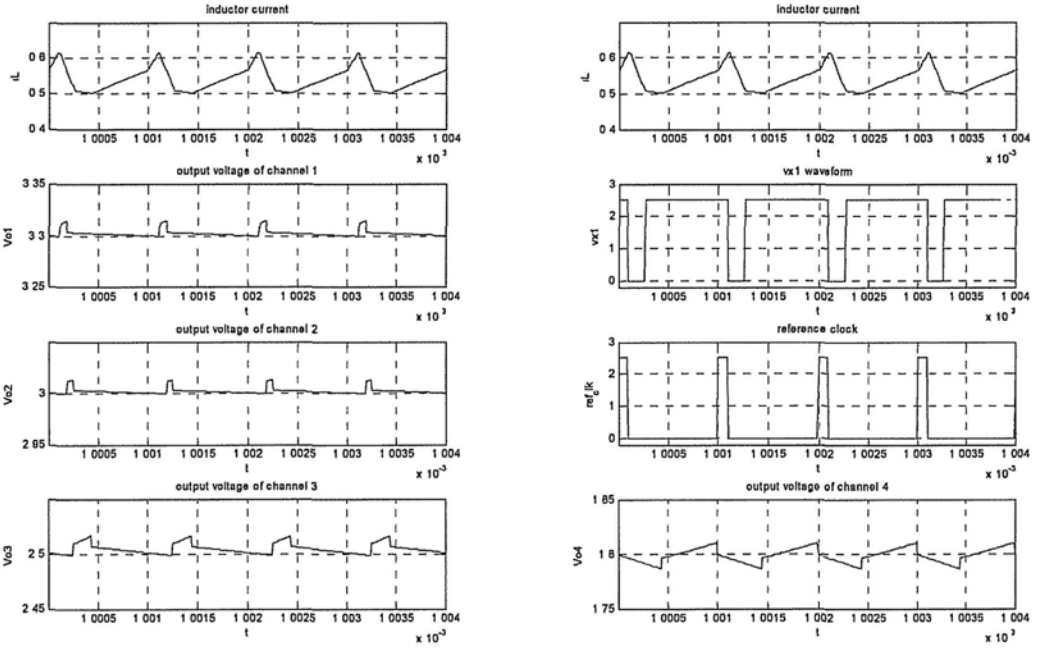



Fig. 4-2 Steady-state of buck-dominated SIMO
(measured at $Io1$ = 40mA, $Io2$ = 64mA, $Io3$ = 35mA and $Io4$ = 226mA).

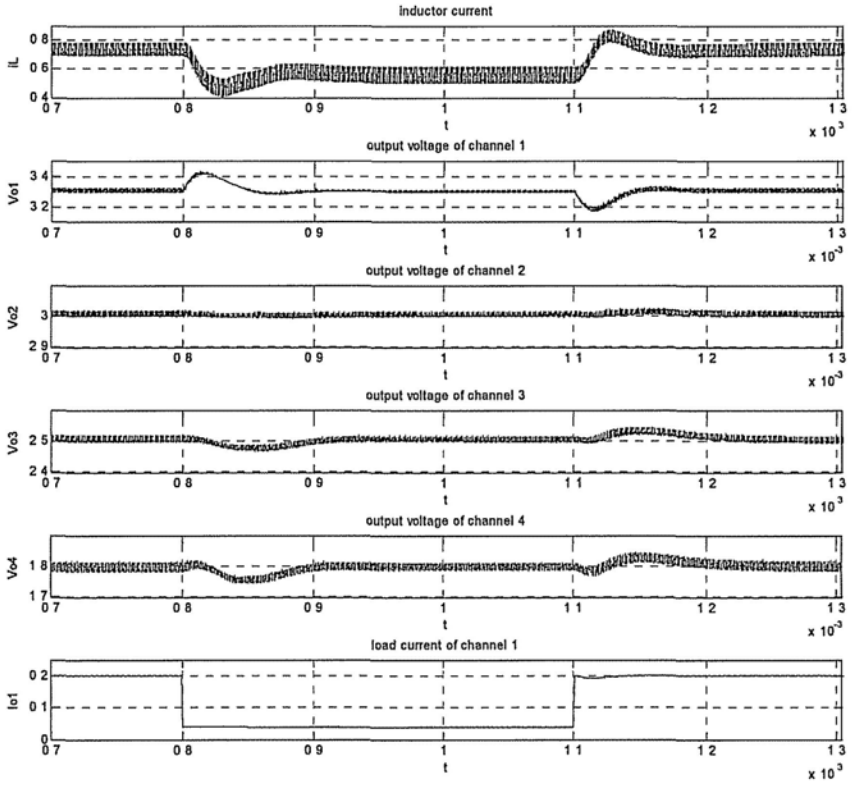



Fig. 4-3 $V_{o1}$ undergoing a 160-mA load transient
(measured at $I_{o1}$ = 40mA, $I_{o2}$ = 33mA, $I_{o3}$ = 100mA and $I_{o4}$ = 200mA).

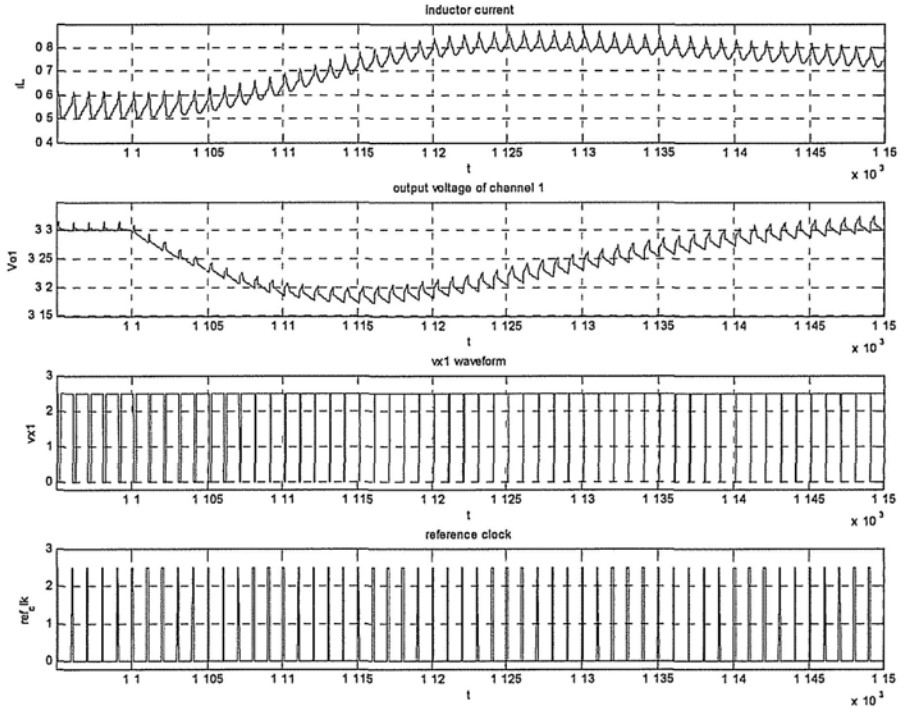



Fig. 4-4 $V_{o1}$ undergoing a 160-mA load transient
(measured at $I_{o1}$ = 40mA, $I_{o2}$ = 33mA, $I_{o3}$ = 100mA and $I_{o4}$ = 200mA).

From the simulation results shown in Figs. 4-1 and 4-2, it is found that its steady state obeys the optimized switching sequence requirement. From the load transient response shown in Fig. 4-3, it shows that it has a competitive dynamic performance with the state-of-art SIMO converter. Moreover, from Fig. 4-4, it is shown that is a strictly fixed-frequency multiple-channel PWM operation.

## 4.3 Digital/Hybrid Implementation of the Controller and its SoC Applications

The possibility of fully integration of the controller with an on-chip active filter has been discussed in previous chapter. On the other hand, in these two designs, they are benefited from the quasi-frequency locking loop method. The switching period is not higher than the reference frequency. It makes it easy to translate to digital implementation.

Accompany with the scaling of IC technology, the implementation the controller using digital form is much more effective. Comparing to the analog counterpart, although the cost of the additional implementation of the specified A/D converter and scarification of performance due to the quantization effect and calculation delay, the outstanding feature in the design flexibility and possibility in more complicated control algorithm make it valuable in the controller design of SMPC. However, in a SoC application, due to the large switching noise of the power switches, it is more effective to separate the power stage and controller into two chips as shown in Fig. 4-5. Due to this separation, it is possible to fabricate the high-density SoC IC with a state-of-art nanotechnology IC process. Some power

application specified IC processes can be used to fabricate the power-switch IC. It can achieve the design flexibility and make it reusable in other SoC applications. In the SIMO applications, in order to save the pin count, multiple-level encoder and decoder which essentially are some low-resolution A/D and D/A converter can be used to save the pin count. Moreover, in order to compensate the performance attenuated by the quantization effect and decrease the requirement of the A/D converters, it is proposed to use a hybrid-compensator method which utilizes both the advantage of analog and digital controller [1]-[3]. It is especially useful in the multiple-channel designs.

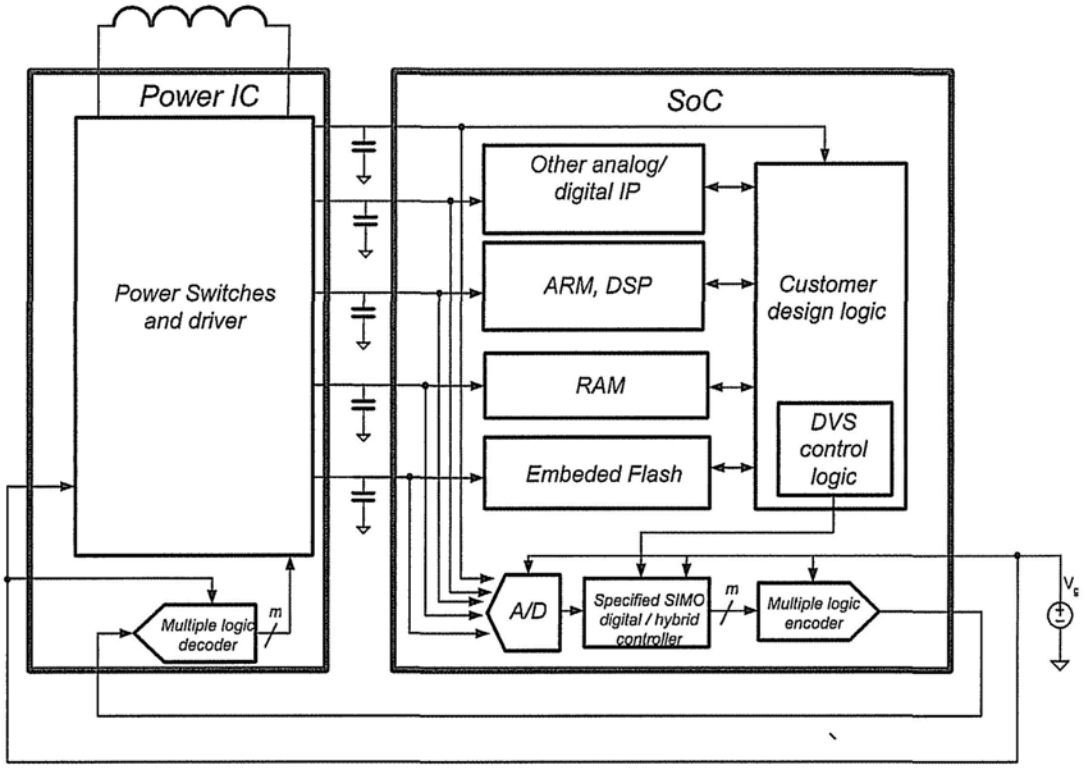



Fig. 4-5 Circuit diagram when applied the SIMO converter to a SoC application.

## 4.4 System Identification and Auto-tuning Controller

In the conventional PWM-control dc-dc converter, it is known that its dynamic performance is related to the compensator design. The parameters and the

architecture of the compensator are highly dependent on the operation points of the dc-dc converter. Although hysteretic voltage control may attenuate the compensator design in voltage feedback loop when a fixed frequency is desired, the compensator design in the frequency feedback loop is also operation-point dependent. As a result, it is desirable to make the compensator design optimized in different operation points. According to these, some research works reported methods to tune the parameters of the compensator based on the sensed operation-point information [4]-[5]. However, since the observation and the tuning parameters are related to the pre-known parameters of the transfer function and the relationship of the operation points, it may be very difficult to do the mapping when parameters are too many and the performance is not guaranteed when the estimated model and the real model derivate from each other too much. Another solution is to use on-line model identified technique combined with on-line dynamic performance measurement. Theoretically, this approach guarantees the system operate with an optimized-compensator design in any local operation point. However, this approach depends on extensive calculations and may suffer from the response time of the processor used for the model identification and the controller parameter tuning. Some research works have been presented such as [6]-[8]. All these refer above show that model identification and controller auto-tuning is still an open topic in this research area. It may have more challenges when extending it to the multiple-channel SMPC design.

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