Efficient Test Methods for RF Transceivers

by

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Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering in the Graduate School of Duke University
2010

Abstract

(Electrical and Computer Engineering)

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Abstract

Advancements of the semiconductor technology opened a new era in wireless communications which led manufacturers to produce faster, more functional devices in much smaller sizes. However, testing these devices of today's technology became much harder and expensive due to the complexity of the devices and the high operating speeds. Moreover, testing these devices becomes more important since decreasing feature sizes increase the probability of parametric and catastrophic faults because of the severe effects of process variations. Manufacturers have to increase their test budgets to address quality and reliability concerns. In the radio frequency (RF) domain, overall test cost are higher due to equipment costs, test development and test time costs. Advanced circuit integration, which integrates various analog and digital circuit blocks into single device, increases test costs further because of the additional tests requiring new test setups with extra test equipments.

Today's RF transceiver circuits contain many analog and digital circuit blocks, such as synthesizers, data converters and the analog RF front-end leading to a mixed signal device. Verification of the specifications and functionality of each circuit block and the overall transceiver require RF instrumentation and lengthy test routines. In this dissertation, we propose efficient component and system level test methods for RF transceivers which are low cost alternatives to traditional tests.

In the first component level test, we focus on in-band phase noise of the phase locked loops (PLL). Most on-chip self-test methods for PLLs aim at measuring the

timing jitter that may require precise reference clocks and/or additional computation of measured specs. We propose a built in test (BiT) circuit to perform a go/no-go test for in-band PLL phase noise. The proposed circuit measures the band-limited noise power at the input of the voltage controlled oscillator (VCO). This noise power is translated as the high frequency in-band phase noise at the output of the PLL. Our circuit contains a self calibration sequence based on a simple sinusoidal input signal to make it robust with respect to process variations.

The second component level test is a built in self test (BiST) scheme proposed for analog to digital converters (ADC) based on a linear ramp generator and efficient output analysis. The proposed analysis method is an alternative to histogram based analysis techniques to provide test time improvements, especially when the resources are scarce. In addition to the measurement of differential nonlinearity (DNL) and integral nonlinearity (INL), non-monotonic behavior of the ADC can also be detected with the proposed technique. The proposed ramp generator has a high linearity capable of testing $13 - bit$ ADCs.

In the proposed system level test methods, we utilize the loop-back configuration to eliminate the need for an RF instrument. The first loop-back test method, which is proposed for wafer level test of direct conversion transceivers, targets catastrophic and large parametric faults. The use of intermediate frequencies (IF) generates a frequency offset between the transmit and receive paths and prevents a direct loop-back connection. We overcome this problem by expanding the signal bandwidth through saturating the receive path composed of low noise amplifier (LNA) and mixer. Once the dynamic range of the receiver path is determined, complete transceiver can be tested for catastrophic signal path faults by observing the output signal. A frequency spectrum envelope signature technique is proposed to detect large parametric faults.

The impact of impairments, such as transmitter receiver in-phase/quadrature (I/Q) gain and phase mismatches on the performance have become severe due to

high operational speeds and continuous technology scaling. In the second system level loop-back test method, we present BiST solutions for quadrature modulation transceiver circuits with quadrature phase shift keying (QPSK) and Gaussian minimum shift keying (GMSK) baseband modulation schemes. The BiST methods use only transmitter and receiver baseband signals for test analysis. The mapping between transmitter input signals and receiver output signals are used to extract impairment and nonlinearity parameters separately with the help of signal processing methods and detailed nonlinear system modeling.

The last system level test proposed in this dissertation combines the benefits of loop-back and multi-site test approaches. In this test method, we present a 2x-site test solution for RF transceivers. We perform all operations on communication standard-compliant signal packets, thereby putting the device under the normal operating conditions. The transmitter on one device under test (DUT) is coupled with a receiver on another DUT to form a complete TX-RX path. Parameters of the two devices are decoupled from one another by carefully modeling the system into a known format and using signal processing techniques.

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List of Abbreviations and Symbols

Abbreviations

ADC	Analog to Digital Converter
ADS	Advanced Design System
ATE	Automatic Test Equipment
BER	Bit Error Rate
BiT	Built in Test
BiST	Built in Self Test
BoST	Built off Self Test
BSS	Blind Source Separation
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CUT	Circuit Under Test
CUT	Clock Signal Under Test
DAC	Digital to Analog Converter
DfT	Design for Test
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
EVM	Error Vector Magnitude
FC	Failure Coverage

FLOP	Floating Point Operation
FT	Fourier Transform
GMSK	Gaussian Minimum Shift Keying
HPC	Hit per Code
IC	Integrated Circuit
IF	Intermediate Frequency
IFA	IF Amplifier
IIP_3	Third Order Input Intercept
INL	Integral Nonlinearity
I/O	Input and Output
I/Q	In-Phase and Quadrature
L	Transistor Length
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
LS	Least Squares
LSB	Least Significant Bit
MIPS	Million Instructions per Second
MOS	Metal Oxide Semiconductor
NLS	Nonlinear Least Squares
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Phase Detector
PER	Packet Error Rate
PSD	Power Spectral Density

PSRR	Power Supply Rejection Ratio
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
RX	Receiver
SiP	System in Package
SNR	Signal to noise Ratio
SoC	System on Chip
VDL	Vernier Delay Line
TD	Time Domain
TDC	Time to Digital Conversion
TX	Transmitter
VCCS	Voltage Controlled Current Source
VCO	Voltage Controlled Oscillator
W	Transistor Width
YC	Yield Coverage

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Introduction

The demand for high performance, multi-functional and smaller size consumer electronic products is the driving force on the semiconductor technology. In each technology cycle, the amount of circuit integration increases as the devices get smaller. Advances in the integration techniques combine digital and analog circuits on the same silicon chip or in the same integrated circuit (IC) package resulting in multi-functional and complex mixed-signal devices with low power consumption.

As in all operational domains of electronic circuits (low frequency, high frequency, digital, analog), RF circuits also benefit from the advanced integration so that bulky, unreliable passive components, such as inductors and capacitors are pulled into the IC packages. Passive filters and passive synthesizer components (inductors of the oscillator circuits) are integrated with the other blocks of RF circuits resulting in single chip (or package) transmitter/receiver circuits instead of circuit boards containing can-tuners, discrete amplifiers and mixers. With the integration of digital circuit blocks into RF circuits, mixed-signal RF circuits have been introduced to the market. The digital functionality of these devices offers more robust operation and application flexibility. Therefore, mixed-signal RF circuits become a very important component in the designs of today's electronic products.

In a mixed-signal RF transceiver circuit, usually the high frequency parts (or RF-band circuitry) are built with analog circuit blocks, such as LNA, mixer, power amplifier (PA) and synthesizer (or PLL). Low frequency parts (or baseband circuitry)

on the other hand, are built with mixed-signal and digital circuit blocks, such as data converters (ADC, digital to analog DAC) and digital signal processors (DSP). Since the device contains both analog and digital circuitry on various frequency bands, traditional production test methods require high calibre mixed-signal testers capable of handling high frequency analog signals as well as low frequency digital baseband signals. However, as the device operating frequencies increase continuously with the improvements in the semiconductor technology, mixed-signal testers quickly become obsolete. High frequency parasitics of the test system do not allow an accurate characterization of the DUT.

Researchers have proposed alternative test methods to solve the problems associated with RF production test [1–12]. Within these methods, component level tests are specialized on specific RF blocks, such as PA, mixers and PLLs whereas system level tests are tailored for specific RF systems, such as transmitters, receivers and transceivers. In general, most of the alternative RF test methods try to eliminate processing high frequency signals so that high frequency mixed-signal testers will be bypassed by using on-chip or on-board (test board) resources.

On-chip resources can be data converters and baseband signal processing units. On-board test resources can be any circuit specific to the required test of the DUT. Usually, the on-board test circuitry is not available on the tester and it is not feasible to integrate the circuit with the DUT. Using these on-chip and on-board resources, researchers have proposed BiST and built-off-self-test (BoST) approaches for analog and RF circuits [13–19] where the test procedures utilize available test resources to obtain the test decision about the DUT.

Aside from the available on-chip and on-board test resources, researchers have proposed BiST methods utilizing special on-chip circuitry to test RF circuits [19–23]. Since these circuits are not a part of the original design of the RF device, they should meet several goals and requirements. The on-chip circuit has to be robust to process

variations to yield high test coverage and low yield loss. Special design techniques may be required to minimize the effects of the process variations. Moreover, the circuit has to verify itself with a self test phase before testing the analog circuit. This self test phase may also preceded by a calibration phase to cancel out some drawbacks of analog circuits such as DC offsets. Most importantly, these on-chip test circuits should not interfere with the operation of the analog circuit under test while performing the test in order to provide accurate results. Generally, on-chip test circuits are tailored to measure specific parameters of the DUT, which may vary with respect to the application domain.

According to available RF test approaches and the test demands of new RF devices, a feasible RF test solution should be cost efficient. Thus, the new test approach should use simple testers and the test times should not be the dominating factor in the test costs. Moreover, the new test method should be as accurate and as reliable as the traditional test methods in order to be a substitute for the traditional test.

This dissertation work aims at developing cost efficient and accurate test methods for individual RF circuit blocks as well as complete RF systems. The proposed component level alternative test methods are designed for PLLs and ADCs, which are the most common building blocks in RF circuits. These component level test methods are BiST approaches providing pass/fail decision based on the measured specifications. The BiST method for the PLLs measures the in-band phase noise of the PLL output and the BiST method for ADCs measures the characteristic parameters of the ADC.

The proposed system level test methods are for I/Q modulation RF transceiver circuits which are used in many communication standards. In order to eliminate RF signal analysis in the test of transceiver circuits, loop-back test technique [5–12] is utilized in the proposed methods. In the first loop-back test method for wafer level

tests, out-of-band signals are used to detect catastrophic and large parametric faults of the receiver circuit. The second loop-back test method is to measure parametric faults in I/Q modulation transceiver circuits. The proposed method is capable of decoupling I/Q mismatch, I/Q time skew and nonlinearity characteristics of the transmitter and the receiver. Based on this loop-back test method, we proposed a new multi-site test approach for I/Q modulation transceiver circuits which is capable of testing an even number of RF transceivers at the same time to measure a set of impairment parameters including I/Q imbalance, I/Q time skew, input/output DC offsets and nonlinearity characteristics of the transmitter and the receiver separately.

1

Motivation and Related Work

The semiconductor technology constantly improves with continuous down scaling of the feature sizes. The direct result from the reduction in semiconductor device sizes is integrating more devices with less parasitic capacitances. Electronic products which utilize these devices evolve in parallel with this improvement.

Today's handheld devices can communicate over various networks with multiple radios integrated into single chip. They utilize faster data processors which provide the speed to support the required functionality. Low power consumption achieved with advanced power control techniques increasing battery life. All these properties are beneficial to consumers however, manufacturer faces with verification challenges due to the complexity of the product. To assure quality, manufacturer has to test the product thoroughly while maintaining a reasonable final sale price.

For each communication network, the RF front end of the product has to be tested for the compliance to the specifications of the communication standard. Baseband and digital functionality needs to be tested with special equipments which mimic the real operational and signaling conditions. As the products become more complex the share of the verification costs increases due to lengthy test methods that require

special equipments.

The overall cost of testing RF devices can have two major contributors: the equipment cost and the cost associated with the test time per device. Traditional RF tests require high frequency mixed signal testers that generate/analyze RF signals in order to measure performance specifications of the circuit. In fact, the equipment cost may easily dominate the overall test cost since the average cost of the tester increases almost exponentially with the operating frequency of the RF device.

The cost associated with the test time per device is the other major factor in the overall test cost. The test time per device is gradually increased over time because the DUTs are becoming more complex.The DUT spends more time on the tester for the various test routines to measure all the performance parameters required by the communication standard.

1.1 RF Test Challenges

Traditional test methods for RF devices require multiple test setups utilizing various RF instruments to measure specific parameters of the device. Each test setup may require a dedicated load board to automate the test process. Switching from one test setup to another not only increases RF instrumentation costs and design/verification costs of load boards but also increases test times because of RF settling times. Usually, RF settling times are longer than data capture times.

Longer test times and the need for high frequency, high calibre test instruments are the common drawbacks of traditional test methods for almost all RF devices. These drawbacks, result in a substantial increase in the over all test costs, are also the common test challenges that needs to be overcome in the new test methods for RF circuits. Other test challenges may be specific to the RF circuit or the test setup. In this dissertation, we proposed component level test methods for PLLs and ADCs and system level test methods for RF transceiver circuits configured mainly in the

loop-back mode. Therefore, we will explain the test challenges specific to these RF circuits and RF systems in the following sections along with the examples from recent studies.

1.1.1 Test of PLL Phase Noise

Even the systems, which may be considered as *purely* digital circuits, such as microprocessors, have an on-chip synthesizer or a PLL for clock generation. PLLs may seem to be accessed easily from outside since every PLL has an outside reference signal input and the overall system may have a clock output for the other devices placed on the same printed circuit board (PCB). However, these input/output pins may not be sufficient to test the PLL or the signals may be degraded by the other circuit blocks on the signal path, such as input/output (I/O) buffer circuitry. More importantly, PLL output phase noise is very hard to measure because of the high frequency output signals. In order to measure phase noise at the PLL output, high calibre test equipments are required to perform spectral analysis.

The difficulty of analyzing high frequency PLL output for phase noise has diverted researchers into BiST methods [2,24–27] for measuring the timing jitter at the output of a PLL instead of the phase noise. The timing jitter and the output phase noise are shown to be closely correlated parameters [28–30]. Therefore, it is preferred as another metric to characterize the PLL output.

In [26], the authors propose a solution to the inherent delay mismatch problem of the Vernier Delay Line (VDL) jitter measurement method by replacing the two delay lines with ring oscillators having distinct frequencies. Although the modification increases the accuracy of the measurement method, there is still a need for a jitter free reference signal to perform the measurement. In [24], a solution is proposed to this problem by eliminating the reference clock and feeding the reference clock input with the delayed version of the clock under test (CUT). In [2,25], the authors improve

the Time to Digital Conversion (TDC) BiST technique in terms of circuit complexity, implementation area, and robustness to process variability. In addition to the timing jitter, the BiST method presented in [27] also measures output frequency and duty cycle of a PLL while improving the jitter measurement resolution and eliminating the clean reference clock requirement.

The only on-chip BiST method to measure phase noise, which is presented in [31], performs an indirect phase noise measurement by multiplying the CUT with a delayed version of itself to obtain an output signal correlated to the phase noise. The delay line is calibrated in a self calibration phase to increase the dynamic range of the BiST circuit. Although this is an on-chip measurement method with a very high measurement sensitivity, the response of the circuit has to be analyzed in the frequency domain with a Fourier Transform (FT) block in order to obtain the results.

The recent studies on the PLL test listed above are mainly focused on the timing jitter at the PLL output rather than the phase noise because of the difficulties of the phase noise measurements. These methods require additional on-chip resource, such as a DSP or additional off-chip computation/analysis of the obtained data in order to provide the test results.

1.1.2 Test of Static ADC Nonlinearity

Analog to digital converters, which are common blocks in today's digital communication circuits, require mixed signal testers in the production test since data conversions between analog and digital domains are inevitable duties that should be performed with analog/mixed-signal devices. In order to overcome the biggest ADC test challenge that is the need for an mixed-signal tester, researchers have proposed to use BiST techniques that are specifically tailored for ADCs [32–36].

Histogram based BiST approaches have been popular in testing important static nonlinearity parameters of ADCs, such as DNL and INL [33–35,37,38]. In histogram

based ADC testing, code frequency statistics are collected based on a known input signal (ramp or sinusoidal) and analyzed to compute INL, DNL, offset voltage and gain error in terms of the ADC's effective least significant bit (LSB). To collect the data, most histogram based BiST techniques require access to an on-chip memory and a DSP. In the absence of such an access due to either a lack of on-chip memory or layout constraints, the studies presented in [33–35] suggest collecting the histogram of each code in a sequential manner.

These BiST methods also require either an on-chip or an external signal source to excite the ADC. Histogram analysis with ramp inputs has been a more popular ADC BiST approach than sinusoidal input because of its uniform code distribution and reduced storage requirement. A common method of generating on-chip ramp signals is to charge a capacitor by a voltage controlled current source. In [19], the authors propose a cascode current mirror based current source architecture. The reported linearity of the ramp is $15-bit$ for $3V$ full-scale range, which is translated to $1V$ full scale range as $13-bit$. With a modification to this current source circuit, a triangular wave generator is proposed in [22]. The authors utilize the same principles for discharging the capacitor and controlling the slope of the voltage ramp. The reported linearity of the triangular wave is about $14-bit$ for $\pm 1V$ full-scale range.

These studies on ADC BiST eliminate the mixed signal tester requirement however, they require on-chip data storage and computational resources in order to obtain the result of the targeted parameter. If these resources are not available, the test time is substantially increased with the time decomposition technique suggested in [33–35]. Another problem with histogram based analysis is that it cannot detect non-monotonic behavior. The ADC may fluctuate between consecutive codes for an increasing signal however, the histogram method collects code counts regardless of the order. Moreover, most of the proposed on-chip signal generation methods are not capable of testing ADC with resolution more that $11-bit$.

1.1.3 Loop-Back Test of RF Transceivers

Traditional test approaches for the RF transceivers require high frequency test equipments and a two-step test procedure wherein transmitter and receiver paths are tested individually. Although this approach guarantees to characterize the transceiver circuit, it requires long test times and different test setups, both of which increase the overall test cost.

In order to reduce test times and the reliance on expensive RF instrumentation researchers have introduced loop-back test method for transceivers to measure circuit characteristics [5–12, 39]. Although this test setup has the equipment and test time advantage, it has new test challenges that need to be overcome.

Generally, the transmitter and the receiver in the transceiver circuit do not operate at the same frequency. Simple loop-back configuration, which connects the transmitter output to the receiver input, does not generate a signal at the receiver output because of the frequency offset between the carriers of the transmitter and the receiver. Researchers proposed various solutions to obtain an observable signal at the output. For example in [9, 10], a second output from the local oscillator (LO) is used to drive the receiver so that the system operates as in normal mode. This method is suitable only for full-duplex systems, which can have separate carriers for both transmit and receive paths. For systems with a single LO output, a switching and attenuating loop-back connection is inserted between the transmitter and the receiver [8]. In this method, with the inserted loop-back connection the input of the receive path stays connected to the transmitter output according to the duty cycle of the switching signal. The frequency of the switching signal is adjusted to fall within the pass-band of the receiver such that the transmitter output signal is basically mixed with the switching signal. Another similar solution is to insert an offset mixer between the transmitter and the receiver [7, 11, 12]. The inserted mixer

in this method simply shifts the signal into the pass-band of the receiver. All these methods are proposed for specification measurements of the transceivers and they may not be suitable for wafer-level tests because the inserted loop-back paths (a high frequency switch or an offset mixer driven by a separate mixing signal) should be implemented on the transceiver chip.

Delaying the transmitted signal with a characterized delay line [5, 6] is another solution that generates an observable signal at the receiver output. A digital design for test feature (DfT) is utilized in [5, 6] to increase fault coverage and to enable measurement of some specifications of the transceiver circuit.

Even with a proper loop-back configuration that generates an observable signal at the receiver output, the parameters of the transmitter an the receiver may not be decoupled and measured accurately. Since the overall system response is observed from the receiver output, the received signal contains the composite effects of both the transmitter and the receiver. Because of the masking between the transmitter and the receiver, cascaded effects of the circuit impairments at the received signals may not be detected as abnormal behavior. Some of the proposed loop-back test methods distinguish gain and nonlinearity parameters of the single channel direct frequency conversion transceiver circuits [7, 39]. However, decoupling of other transceiver impairments, such as I/Q mismatch and I/Q time skew parameters have not been addressed in previous studies.

Recently proposed measurement methods for these parameters focus on either the transmitter or the receiver side of the transceiver circuit [40, 41]. However, they are not applicable in a loop-back configuration. In [40], the authors propose a test method to characterize single- and multi-carrier I/Q modulation transceivers. With this method, either the receiver or the transmitter nonlinearity and I/Q mismatch parameters can be measured by using signal constellation data. The technique in [41] employs an analytically driven algorithm to calculate I/Q mismatch parameters as

well as the time skew on the Q channel of the transmitter. Test input is a multi-tone sinusoidal signal and the power/phase data on the sideband signal is used to calculate the impairments.

Another difficulty associated with the loop-back test configuration is the delay introduced by the physical loop-back path. Unless intentionally used and characterized [5, 6], this delay complicates measurements by introducing an additional unknown parameter to the system. For example in QPSK, delay in the loop-back path results in asynchronous transmitter/receiver carriers (in terms of phase) and a time shift in the received symbol times.

1.1.4 Multi-site Test of RF Transceivers

The transceiver circuit usually designed to operate either in the transmit mode or in the receive mode unless the device has a full duplex mode. Designers may not recommend full characterization of the transceiver circuit in the loop-back mode because of the isolation problems between the transmitter and the receiver. Therefore, the loop-back configuration may not be suitable for these devices as an accurate test approach. The two-step traditional test method may seem to be the only choice. However, as highlighted in the above discussion, two-step test requires RF equipments and long test routines to characterize the RF transceiver circuit. Fortunately, there is recent trend towards multi-site testing in high volume production environment which can take advantage of multiple devices on the load boards [42, 43]. Multi-site testing reduces the test times per device by reducing the overall test setup times and by using the same input signal for all the devices.

Current practice in multi-site testing is to treat each device as a separate path and still test the transmitter and the receiver in different test setups. While the input signal is shared, the output signals have to be analyzed separately. This approach requires either multiplexing the output signals or sampling them at the same time,

requiring more resources. Moreover, since the receiver and the transmitter are tested separately, RF instrumentation, either at the ATE or on the load-board is necessary.

1.2 Summary of Research Needs

As discussed in the above sections, traditional test approaches both for system level and component level RF tests have the common drawback of high equipment costs. Mixed signal structure of today's RF transceivers and transceiver components increases the equipment costs further by introducing the requirement of mixed signal testers. Other common drawback is the elongated test times due to complexity of the devices. Alternative test methods for RF systems and system blocks have to utilize low cost testers while decreasing the test times. In addition to these common drawbacks, alternative RF test methods have to overcome challenges specific to the circuit or the test setup.

1.2.1 Component Level Test

Today's RF transceiver circuits usually employ analog and/or mixed signal blocks, such as PLLs and ADCs. Component level test methods proposed for these circuit blocks are able to provide decent test coverage however, some improvement is needed to eliminate some of the remaining drawbacks.

Most of the research on the PLL BiST is focused on the timing jitter and the research about in-band phase noise BiST is very sparse due to complexity of phase noise measurements. Moreover, presented methods in [2, 24–27, 31] require further computation on the experimental data to decide on the test outcome. An attempt to fill this void, we propose a simple and a robust go/no-go based PLL BiST for the characterization of the in-band phase noise of the PLL.

Histogram based BiST methods for ADC have been popular alternative test methods [19,22,33–35,37,38] which eliminate the need for a mixed signal tester. However,

test times are substantially increased in the expense of limiting test resources. In this dissertation, we propose a faster BiST method for ADCs requiring less test resources. We also propose an on-chip slow ramp signal generator for the BiST method capable of testing ADCs with resolution $14-bit$ and higher.

1.2.2 System Level Test

The loop-back test configuration eliminates the need for RF test equipments to test RF transceivers. However, frequency offset, transmitter-receiver parameter decoupling and loop-back path delay are the inherent test challenges associated with this method. Prior work has addressed some of these issues for simple transceiver architectures [5–12,39]. For rapid wafer level tests to diagnose catastrophic and parametric faults, some of these methods are too complicated to be implemented on-chip since they utilize circuits residing on the loop-back path to perform switching or mixing functions on the RF signal. In specification measurements on the other hand, some studies [7, 39] achieved to decouple gain and nonlinearity parameters of the transmitter and the receiver of a single channel direct conversion transceiver circuit. However, a research on decoupling impairments of a transmitter and a receiver in an I/Q modulating transceiver has not been addressed in the prior work.

When the loop-back test is infeasible due to the design limitations of the transceiver circuit, the transmitter and the receiver has to be tested individually in separate test setups. Since RF instrumentation is required in these test setups to generate/analyze RF signals, test cost reduction may only be possible by decreasing test times. Researchers have proposed multi-site test approaches [42, 43] testing multiple DUTs at the same time to reduces overall test time per device.

In these multi-site approaches, DUTs are tested in parallel with the same test signals to decrease test setup times. However, the equipment cost increased with the number of parallel test sites because the multi-site test simply extends the test sites

of traditional transceiver test. Therefore, a multi-site test application is only feasible if the test time is the dominating factor in the overall test cost of the RF device. In order to apply this approach to to RF transceivers requiring high calibre test equipments, traditional two-step transceiver test method should be abandoned. In this dissertation, we propose a special multi-site test approach to test even number of RF transceivers at the same time. The proposed test has the reduced test time advantage of the multi-site tests without requiring expensive RF instrumentation.

1.3 Thesis Outline

The remainder of the thesis is organized as follows. In Chapter 2, we introduce go/no-go based PLL BiST to characterize the in-band phase noise of a PLL. In Chapter 3, we propose a limited test resource ADC BiST with a high linearity ramp generator. Chapter 4 presents a rapid wafer level test method utilizing loop-back configuration to diagnose catastrophic and parametric faults of an RF transceiver. In Chapter 5, we present a loop-back based BiST method for RF transceivers measuring I/Q mismatch, I/Q time skew and nonlinearity parameters of the transmitter and the receiver. Based on the findings of Chapter 5, Chapter 6 presents a special multi-site test method for RF transceivers. Chapter 7 includes concluding remarks and future research directives.

2

BiST Method for Synthesizer Phase Noise

All RF transceivers employ frequency synthesizers to set the carrier frequencies. The most important parameter of the synthesizer is the phase noise, which directly impacts the signal-to-noise-ratio (SNR) of the output signal and the Bit Error Rate (BER).

Synthesizers are typically completely embedded with only the reference input accessible from outside the chip. Due to the access restrictions, synthesizers are good candidates for BiT solutions. However, measuring the synthesizer phase noise is particularly challenging since it requires accurate analysis for a high frequency signal. Analyzing the high frequency PLL output on-chip with the required frequency resolution is a costly venture.

In this chapter, we focus on PLL phase noise performance. We introduce a new BiST technique for go/no-go based test of PLLs to predict output phase noise performance without making measurements at the PLL output. We utilize the closed loop feature of the PLL and introduce an observation method relating the amplitude noise at the input of the VCO to the PLL output phase noise. The noise power at the input of the VCO is measured in the time domain based on the Rayleigh's

Energy Theorem [44] by a BiST circuit composed of a time domain squarer and an integrator.

In order to yield high test coverage and low yield loss, any BiST method must be robust with respect to process variations since the BiST circuit is manufactured with the DUT. In our case, the measurement result of the proposed BiST circuit may deviate due to process variations. Therefore, the result of this measurement is not taken as the test result. Instead, we compare this result to a threshold set in a calibration/self-test phase to generate a pass/fail test response. The test threshold is set in the calibration/self-test phase with a simple sinusoidal test input based on given PLL specifications. This threshold mechanism increases robustness of our BiST method because it eliminates reliance on absolute circuit parameters by using the actual BiST circuit to setup the test threshold. The complete BiST circuit, including the calibration components, is implemented with an area equivalent to roughly 800 2-input minimum size NAND gates. Experimental results show that the BiST circuit can flag phase noise levels that are higher than the specified threshold and can provide more than 95% yield under process variations.

2.1 Measuring The Signal Power

The power of a signal can be measured both in the time domain or in the frequency domain depending on the application and the required accuracy. Both methods require capturing and storing samples of the targeted signal for a short period of time. On one hand, the stored samples are squared and integrated in the time domain method to obtain the average signal power. On the other hand, the stored samples are used to calculate the FT of the signal in the frequency domain method in order to obtain the power of the fundamental signal component.

In most cases, on-chip implementation of the time and frequency domain methods may not be feasible due to the limited test resources. For example, an on-chip ADC is

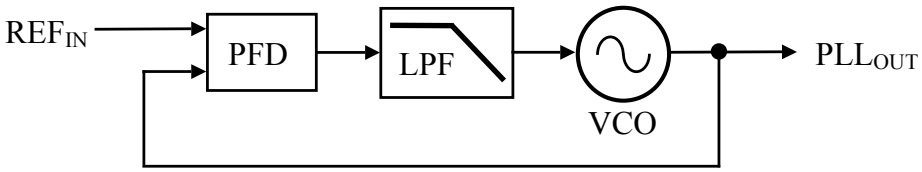


FIGURE 2.1: PLL block diagram

required to sample the targeted signal. ADCs have already been used as popular on-chip components however, the sampling frequency of the ADC may not be sufficient to cover the bandwidth of the targeted signal especially in RF band. Moreover, an on-chip DSP is required for both measurement methods to perform necessary calculations such as the FT.

2.2 The Loop Dynamics

Synthesizers are closed loop control systems, as shown in Figure 2.1. The difference in the phase of the reference signal and the VCO output signal is filtered and used as the control signal for the VCO. Typically, the feedback path contains either an integer or a fractional divider block to generate the desired frequency at the PLL output. The divider block is not included in the representation for simplicity.

Figure 2.2 shows the linear phase model of the PLL along with the transfer function of each block. The overall transfer function for the phase is calculated by $\phi_{out}(s)/\phi_{in}(s)$. The phase detector (PD) is represented by a subtraction with an associated gain. The low-pass filter (LPF) is assumed to have a linear voltage transfer function $G_{LPF}(s)$. The VCO is characterized as an integrator to convert the voltage to instantaneous phase.

Each block in the synthesizer loop contributes to the phase noise at the output signal. The effect of the VCO phase noise to the output phase noise can be easily proved to have high-pass characteristic. Therefore, the VCO contributes only to the out-of-band portion of the phase noise. The noise generated by all other components

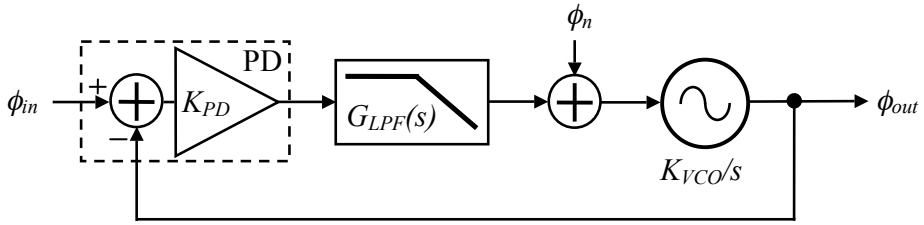


FIGURE 2.2: Linear phase model of a PLL

in the loop can be assumed to accumulate at the input of the VCO, ϕ_n, as shown in Figure 2.2. The transfer function between the output phase noise and ϕ_n is derived as:

$$\frac{\phi_{out}(s)}{\phi_n(s)} = \frac{K_{VCO}}{s + K_{PD}K_{VCO}G_{LPF}(s)}. \tag{2.1}$$

Thus, the noise at the input of the VCO is low-pass filtered and is the major contributor to the in-band phase noise.

In-band phase noise is the most important parameter of the synthesizer. In some applications, the synthesizer performance is determined by the statistical characteristics of the timing jitter at the output relying on the strong correlation between the variance of the timing jitter and the in-band-phase noise [28–30]. Thus, in most cases the synthesizer is characterized either by in-band phase noise or by the timing jitter depending on the application.

2.3 Alternative PLL Phase Noise Characterization

The phase noise at the output of a synthesizer is not an easy to measure parameter especially with an on-chip test circuitry. High resolution and high frequency spectral analysis is required. The test circuit may have limitations due to very high operation frequency. Luckily, as discussed in Section 2.2, the one-to-one correspondence between the output phase noise and the noise at the input of the VCO can be utilized

Table 2.1: Relation between PLL in-band phase noise and VCO input noise power

VCO Input Noise Power (dBm)	-13.90	-10.92	-9.17	-7.93
PLL Phase Noise (dBc/Hz)	-70.91	-67.98	-65.66	-64.47

to characterize the PLL performance in terms of in-band phase noise. At a given frequency, the in-phase noise at the PLL output can be predicted with the transfer function given in Equation 2.1, if we know the noise power at the input of the VCO.

We perform MATLAB simulations to test this correlation. A charge-pump PLL composed of a second order loop filter and a VCO with phase noise is modeled in MATLAB. With the help of an external noise source, noise signals with different power levels are injected to the VCO control input. Table 2.1 reports the noise power at the VCO control input as well as the PLL output phase noise at $10KHz$ offset from the fundamental frequency. As can be seen, the linear relation between the noise power and the in-band phase noise indicates the gain of the transfer function given in Equation 2.1.

In our BiST method, we propose to measure the amplitude noise at the input of the VCO in order to predict the PLL performance in terms of in-band phase noise. Since the signal at the VCO control input is limited by the synthesizer loop bandwidth, the operation frequency of the BiST circuit is very low compared to the PLL output. However, the traditional noise power measurement method based on spectral analysis can not be implemented on-chip due to the overhead of sampling, digitizing and computational circuits. We propose an alternative measurement method based on Rayleigh's Energy Theorem performing a time domain power measurement on the band limited noise signal at the VCO input

2.3.1 Time Domain Power Measurement

Rayleigh's Energy Theorem states that the energy of a signal, $g(t)$, defined over the interval $-\infty < t < \infty$ having a FT denoted by $G(f)$ can be calculated both in time domain and in frequency domain:

$$E = \int_{-\infty}^{\infty} |g(t)|^2 dt = \int_{-\infty}^{\infty} |G(f)|^2 df \ . \tag{2.2}$$

In order to utilize Rayleigh's Energy Theorem in our method, we need to limit window of integration because computing the power of a signal over an infinite window is physically infeasible.

For a limited time window of duration T, the average power of the signal can be calculated as:

$$P = \frac{1}{T} \int_{0}^{T} |g(t)|^2 dt \ . \tag{2.3}$$

We define a new function $y(t)$ as $y(t) = x(t).g(t)$, where $x(t)$ is a rectangular pulse function with a value 1 between interval $0 \leq t \leq T$. The FT of $x(t)$ will be:

$$X(f) = Tsinc(fT)exp(-j\pi fT) \ , \tag{2.4}$$

and the FT of the new function $y(t)$ can be calculated as using the multiplication-convolution property of FT as:

$$Y(f) = \int_{-\infty}^{\infty} G(\lambda)X(f-\lambda)d\lambda \ . \tag{2.5}$$

Since $X(f)$ is a *sinc* function we can approximate its FT by an impulse, δ function evaluated at f, if the time window is sufficiently large. Therefore, $Y(f)$ can be approximated as:

$$Y(f) \approx G(f) \ . \tag{2.6}$$

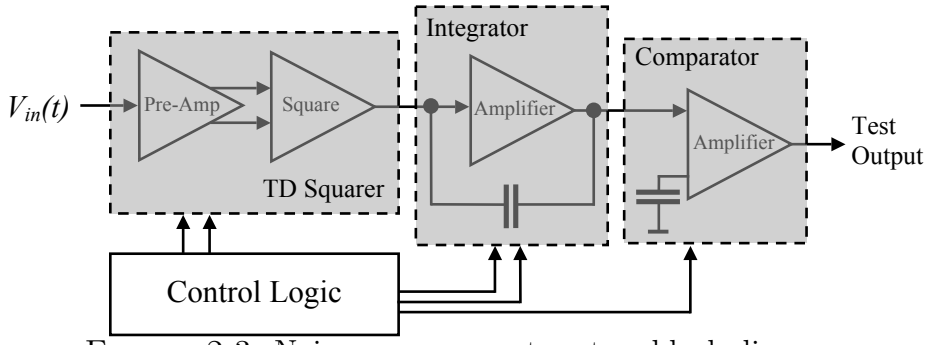


FIGURE 2.3: Noise measurement system block diagram

We finally obtain the power of the desired signal in a given time window as:

$$P = \frac{1}{T}\int_{0}^{T} |g(t)|^2 dt \approx \frac{1}{T}\int_{-\infty}^{\infty} |G(f)|^2 df \ . \tag{2.7}$$

Based on these derivations, in order to get an accurate estimation on the power of a signal, in our case the noise signal at the VCO input, we need to keep the integration window as large as possible.

2.3.2 Noise Measurement System

Our BiST method for measuring the noise power is based on integrating the square of the VCO input signal for a short time window as given in Equation 2.7. We implemented the proposed BiST method with four major circuit blocks: the time domain (TD) squarer, the integrator, the comparator and the control logic. The block diagram of the overall system can be seen in Figure 2.3.

The VCO control signal, $V_{in}(t)$, which is the input signal to the BiST circuit, is amplified and squared by the TD squarer block. Then, the output signal of this block is applied to the integrator block, which calculates the noise power of the input signal using the squared signal. The comparator block generates a binary pass/fail test output based on the calculated noise power from the integrator. Overall test sequence is governed by the control logic block, which generates the required

digital pulses to operate certain parts of the measurement system throughout the test process.

TD Squarer

The TD Squarer block is composed of two amplifiers: a preamplifier, which amplifies weak noise signals and the squaring amplifier, which calculates the squared signal for the integration. A capacitor is placed at the input of the preamplifier to filter out the DC component of the VCO control signal. The physical connection between the VCO control signal and the preamplifier input is established by a transistor switch activated by the control logic block in the test mode of the DUT. The differential output signals of the preamplifier are also followed by DC blocking capacitors to prevent saturation of the squaring amplifier. However, the squaring amplifier output is not filtered with a capacitor since it may contain essential DC components of the squared input signal.

Integrator

The integrator block is composed of an analog integrator, which calculates the noise power. The squared signal is integrated over a limited time window. At the end of each integration window, the integrator is reset by discharging the feedback capacitor with a transistor switch. A pulse coming from the control logic block activates the transistor switch for very short period of time.

Comparator

Before resetting the integrator, the calculated noise power is compared to a threshold value by the comparator block for the pass/fail decision of the test. The threshold value is set in the calibration phase of the test sequence, which also performs an offset cancellation at the integrator output before the actual measurement.

Control Logic

The control logic block is responsible for controlling the test sequence by generating required digital pulses. The functionality of this block may be replaced by the digital test equipment, if there are enough digital test pins of the DUT available to reach the BiST circuit.

2.3.3 The Test Sequence

The integrator generates an output value proportional to the integrated noise power at the input of the VCO. However, this final integration result is affected by several factors. The overall gain of the BiST circuit introduces a coefficient to the integrated value. The length of the integration window and the integrator parameters introduce another coefficient. Moreover, all the DC offsets generated after the squarer as well as the noise introduced before the squarer will be accumulated by the integrator, generating an offset at the output. Thus, the output of the integrator is of the following form:

$$Vout = C_0 + C_1 \int_0^T |g(t)|^2 dt \ , \tag{2.8}$$

where C_0 is a constant due to the DC offsets and accumulated BiST circuit noise and C_1 represents all the other coefficients. Both C_0 and C_1 are internal parameters of the circuit. During production of the DUT, all the circuit parameters will deviate due to process variations and each DUT will have unique coefficients for the BiST circuit output. Therefore, calculating and using the output coefficients associated with the integrator circuit has no benefit.

In our method, the actual test of the synthesizer is preceded by a calibration phase to eliminate the reliance on the absolute parameters of the BiST circuit. In the calibration phase, we apply a characterized sinusoidal waveform (in terms of amplitude

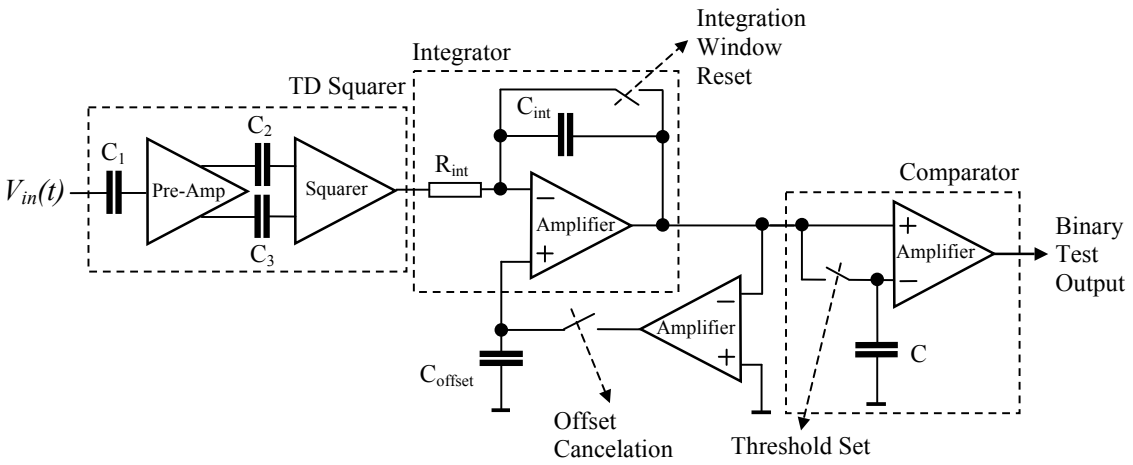


FIGURE 2.4: The complete BiST system with calibration pulses

and noise) to the circuit and the output is stored on a capacitor to serve as a threshold. This waveform, which we call the *reference sinusoidal signal*, is constructed according to the synthesizer specifications. During the test of the synthesizer, the noise signal will be passed through the same circuit with the same parameters, enabling an energy comparison without an actual read out. This scheme provides a go/no-go based testing where synthesizer with an integrated noise power above the threshold will fail. In order to store the energy level of the reference sinusoidal signal and compare it with the noise power level from the synthesizer circuit, we use the comparator block with the threshold capacitor. The detailed block diagram of the overall measurement system can be seen in Figure 2.4.

The test sequence of out BiST method is composed of the following steps which help to increase robustness and the reliability:

- Offset cancellation
- Threshold setting
- Test

The Offset Cancellation Phase

Although we use a reference sinusoidal signal to set the threshold for the pass/fail decision, offset cancellation is necessary to prevent the DC offsets generated after the squarer block from saturating the path. DC offsets can generally be filtered by DC blocking capacitors in analog circuits. However, the squared signal contains a necessary DC component. Therefore, using of a blocking capacitor is not feasible after the squaring amplifier. We introduce an offset cancellation scheme from the output of the integrator to the input of the integrator. It should be noted that a precise offset cancellation is not necessary since the same amount of energy will be stored both for the reference sinusoidal signal and the test signal. However, our goal is to reduce the offset to a degree where it does not saturate the path.

At the beginning of the offset cancellation step, the input of the circuit is grounded and a pulse with duration of 2μsec is applied to the *offset cancellation* signal. During this period, the DC offset at the integrator output is canceled by the negative feedback formed by the amplifier and the input offset value is stored at the capacitor.

The Threshold Setting Phase

The second step of the calibration sequence is to set the threshold value for pass/fail comparison. The synthesizer's in-band phase noise specification determines the maximum tolerable integrated noise power level. We determine the amplitude of a sinusoidal waveform that corresponds to the same power level. This sinusoidal waveform constitutes our reference sinusoidal signal. The amplitude of this sinusoidal signal is determined during the test development phase and it also impacts the desired gain of the preamplifier. It should be noted that the amplitude of the reference signal is much bigger compared to the amplitude of the noise signal since its power is concentrated on one frequency location.

The integration window for the reference sinusoidal and the noise signal are iden-

tical. At the end of the calibration window, the comparator input is set to a voltage level that is representative of the reference signal power (related to the synthesizer phase noise limit).

The Test Phase

After the calibration is completed, the actual test operation starts with the self test phase. We switch the input of the BiST circuit to a small resistor connected to ground to observe a 0 output (A 0 at the comparator output means a *pass*). For the actual DUT test, we connect the BiST circuitry to the noise signal to be measured and perform the test.

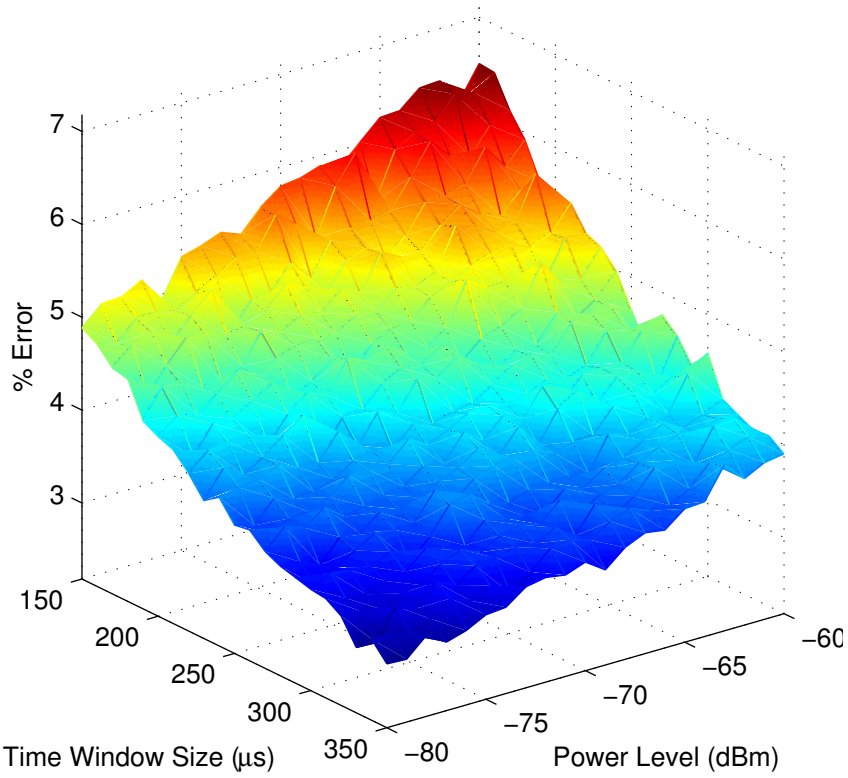


FIGURE 2.5: The effect of time window size on the accuracy of noise estimation using Rayleigh's Theorem

2.3.4 The Length of The Integration Window

As mentioned in Section 2.3.1, longer integration windows give better a approximation in Equation 2.7. As an example, Figure 2.5 shows the impact of the length of the time window on the estimation accuracy of the noise power. The noise bandwidth in this example is set at $50kHz$. For various noise power levels and time window lengths, the noise power has been calculated using Equation 2.7, and compared to the actual total noise power level. The z-axis indicates the error in computing the noise power using Equation 2.7 for a limited time window. It is clear that as the time window length increases, the estimation accuracy increases. This trend is due to the random nature of noise, which requires a prolonged observation period in order to estimate its characteristics. However, longer integration window means larger accumulated noise power at the output of the integrator block. Therefore, for a practical CMOS implementation of the proposed BiST method, the longer integration window may result in poor dynamic range of the measurement system.

An alternative way of reducing the overall error without increasing the integration window length is to repeat the measurements multiple times. The results from multiple measurements can be combined by averaging. As an example, Table 2.2 shows the effect of observing the noise signal over multiple windows for $-70dBm$ total noise power and a time window duration of 250μs. Clearly, measuring the noise power over multiple windows and taking an average reduces the error, since it effectively increases the time window size. In our BiST scheme, we determine the time window size based on the dynamic range of the circuit implementation as well as the expected noise power level (as given by the synthesizer specification). We then determine the number of time windows to be observed to meet the accuracy requirements.

As indicated above, in order to achieve the desired levels of accuracy, it may be

Table 2.2: Error in noise estimation for various numbers of observation windows

Number of windows	1	3	5	7	9	11
Error (%)	4.8	3.4	2.9	2.6	2.4	2.3

necessary to repeat the measurements multiple times. We utilize a majority voting scheme to take the *pseudo* average of multiple measurements. Once we determine an odd number of integration windows to be observed to satisfy the accuracy requirements, we take the majority of the test results as the pass/fail decision. For $(2n+1)$ time windows, the pass/fail result of each individual time window is recorded. The overall pass/fail condition is determined by the majority result of $(n+1)$ outcomes. For example, for 5 time windows, if the comparator output reads (00110), the circuit passes since there are 2 *fail* and 3 *pass* results.

2.3.5 BiST Circuit Implementation

Each block in the system shown in Figure 2.4 is implemented with 0.8μm CMOS technology. The circuits are supplied with $\pm 1.65V$ supply voltages.

The preamplifier in Figure 2.4 is a two stage differential input, differential output amplifier. It has a voltage gain $40dB$ for both arms. The negative differential output is obtained by inverting the positive differential output through a current mirror and a resistor-like connected transistor. This configuration brings some gain mismatch between differential outputs but it has the advantage of the current feedback utilized in the differential input stage. The CMOS implementation of the preamplifier is given in Figure 2.6.

The novel squarer circuit given in Figure 2.7 is a differential input single-ended output configuration. Unlike a traditional differential pair, the transistors at the positive and the negative inputs are split into two branches. As a result, instead of two regular inputs we have two input pairs, $M1-M2$ and $M3-M4$. Theoretically,

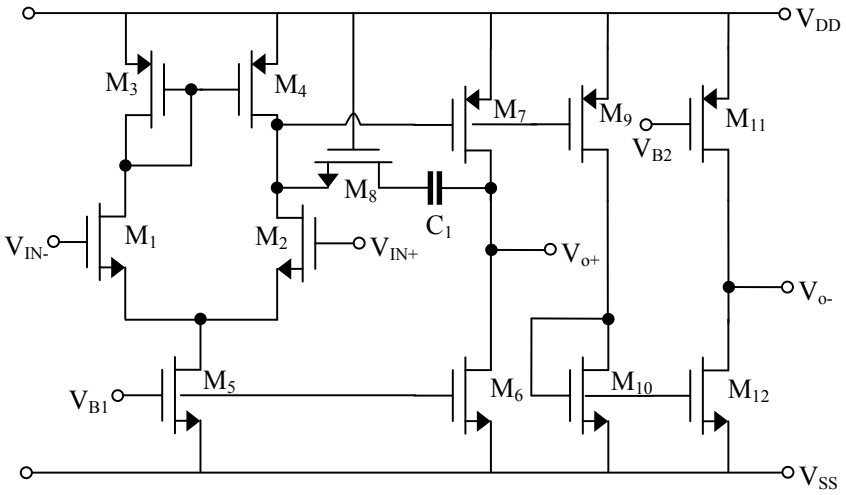


FIGURE 2.6: Preamplifier circuit

we do not need to split the right hand side input transistor into $M1$ and $M3$ but in that case we loose the symmetry of the circuit which can be a problem in the presence of process variations. The outputs of the preamplifier are applied to one input pair of the squarer and the other input pair is grounded. In fact, the $\pm$ inputs of the squarer are connected to ground with large resistances (which are not included in Figure 2.7 for simplicity) to obtain a path for biasing the input transistors.

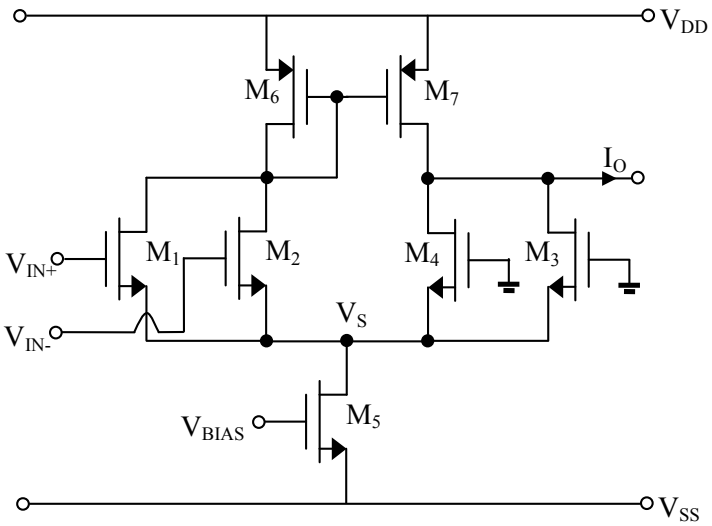


FIGURE 2.7: Squarer circuit

The output current (voltage) of the squarer can be calculated by solving the MOSFET Level-1 current equations and assuming equal currents in the current mirror transistors $M6$ and $M7$.

$$
\begin{aligned}
I_{D1} &= \frac{k}{2}(V_{IN} - V_S - V_{TN})^2 \\
I_{D2} &= \frac{k}{2}(-V_{IN} - V_S - V_{TN})^2 \\
I_{D3} &= \frac{k}{2}(-V_S - V_{TN})^2 \\
I_{D4} &= \frac{k}{2}(-V_S - V_{TN})^2 \\
I_O &= I_{D1} + I_{D2} - I_{D3} - I_{D4} \\
I_O &= kV_{IN}^2
\end{aligned} \tag{2.9}
$$

The squarer can be used in two modes, voltage amplifier or voltage-to-current converter (trans-conductance amplifier). For the voltage amplifier the load impedance should be bigger than the parallel combinations of the output impedances of transistors $M7$ and $M3 - M4$ and for the voltage-to-current converter it should be smaller. In our circuit, we chose the voltage amplifier mode because we have increased the number of parameters to adjust the gain of the integrator, which is $1/RC$ by introducing the resistor R_{int} in Figure 2.4.

The amplifier block in Figure 2.4 is a regular, two stage, single ended OpAmp with output compensation network composed of a transistor and a capacitor. The open loop gain bandwidth is reduced by the capacitor in the compensation network in order to meet the stability criteria. The CMOS implementation of the amplifier is the same circuit as in Figure 2.6 excluding the inversion stages.

2.3.6 PLL Implementation

We implemented a simple charge-pump PLL with 0.5μm CMOS process to perform experiments on our BiST circuit. The implemented PLL has the basic charge-pump PLL blocks without the frequency divider block on the feedback path. An all-digital phase detector is utilized to generate *Up* and *Down* signals for the charge-pump block. The loop filter of the PLL is chosen as an off-chip second order low-pass filter attached to the VCO control pin. This configuration provides an easy access to the control voltage of the VCO. A current-starved 5-stage ring oscillator is used as the VCO core architecture where the power supply current of the ring oscillator is limited with the voltage on the control pin of the VCO. The VCO core is followed by a buffer to drive off-chip capacitive loads up to $30pF$.

The PLL and the TD Squarer Block was fabricated with 0.5μm 3-metal CMOS

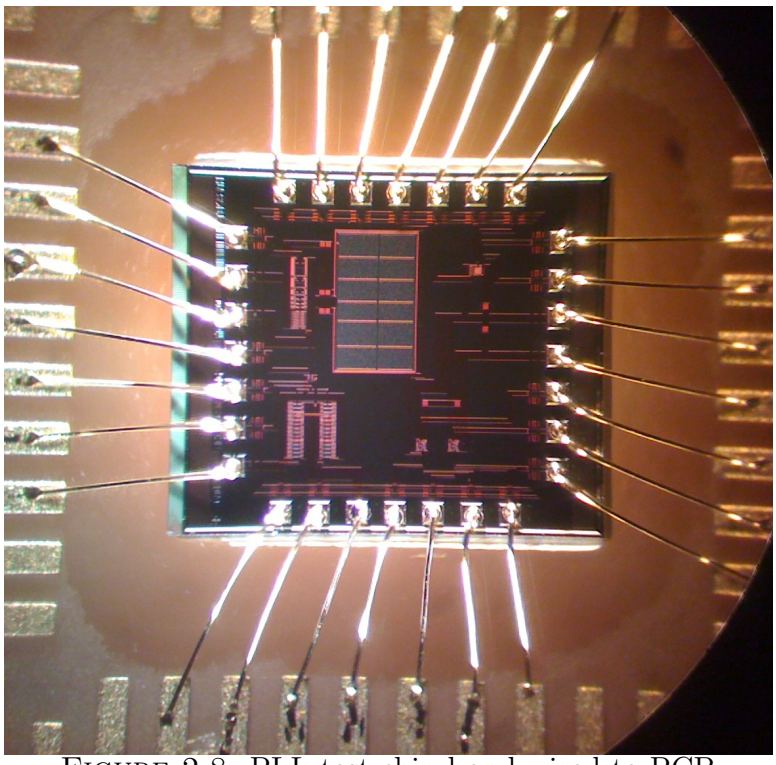


FIGURE 2.8: PLL test chip bond-wired to PCB

process. A die-photograph of the fabricated chip, which was bond-wired to a test PCB, is shown in Figure 2.8. Due to the limited number of I/O pins, only the TD Squarer Block was fabricated with the PLL. The remaining integration function of the BiST circuit is performed on the collected data in MATLAB.

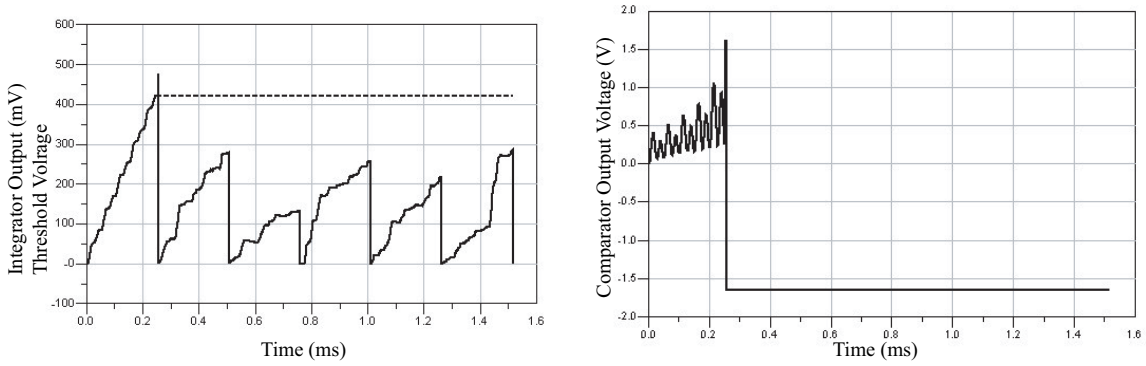
2.4 Experimental Results

We performed transistor level simulations of the proposed BiST circuit in ADS to verify the circuit operation with the nominal circuit parameters and the robustness of the system to process variability, such as transistor parameters (W, L) or the gate-oxide thickness. We also performed measurements on the fabricated charge-pump PLL test chip to verify the functionality of the BiST circuit blocks as well as the theory behind the proposed test method.

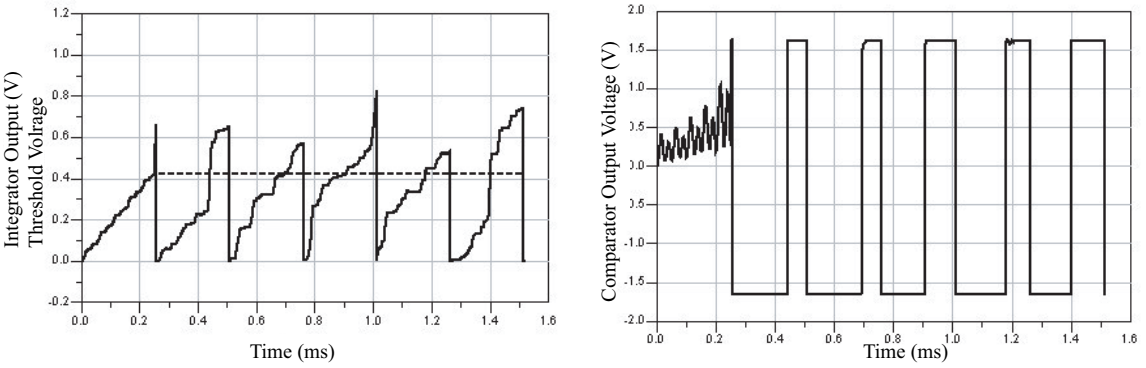
2.4.1 Simulation of the Circuit Operation

The overall BiST circuit was constructed using the CMOS implementations of each block including the calibration switches. Based on the available dynamic range of the circuits, we set the time window size to 250μs. We arbitrarily set our accuracy goal to 2.5%. This accuracy goal indicates that for noise levels that are at least 2.5% above the defined threshold, the system is expected to provide a *fail* response and for noise levels that are at least 2.5% below the defined threshold, the system is expected to provide a *pass* response.

The threshold for phase noise level of the circuit under test is set at $0.27\mu V/\sqrt{Hz}$ with a $50kHz$ bandwidth (BW), corresponding to $-71.4dBm$ integrated noise power. The reference sinusoidal signal has a peak-to-peak level of $120\mu V$, corresponding to the same power level. For the noise source, we use the embedded noise generator of ADS. As test inputs, we use a $0.2\mu V/\sqrt{Hz}, 50kHz$ BW noise source corresponding to $-73.4dBm$ (*pass condition*) and a $0.3\mu V/\sqrt{Hz}, 50kHz$ BW noise source correspond-



(a) Integrator output (the stored threshold is given in dashed line) and comparator output for the low input noise level (1.5dB lower than reference signal)



(b) Integrator output (the stored threshold is given in dashed line) and comparator output for the high input noise level (2 dB higher than reference signal)

FIGURE 2.9: The responses of the integrator and the comparator for the two noise power levels for 5 time windows

ing to $-70.5dBm$ (*fail condition*). In the first time window, the circuit calibrates itself with the reference sinusoidal at $20kHz$ and sets its threshold value. Then the input is switched to the noise source and the circuit measures the noise power for 5 time windows. Figure 2.9 shows the *Noise Power* output and comparator (binary decision) output of the circuit for both of the noise inputs. As can be seen from the upper plots of Figure 2.9, the comparator output does not flip to high logic value since the integrated noise power is smaller than the threshold in each time window. The opposite case is true for the lower plots in Figure 2.9.

2.4.2 Monte Carlo Simulations to Estimate the Yield of the Test Circuit

The BiST circuit is affected by both the production and the operation environments as the DUT. In the production, the parameters of the on-chip BiST circuit deviate due to process variations, whereas the thermal noise contaminates signals of both the DUT and the on-chip BiST circuit. Since the effects of both the production and the operation environments are uncorrelated random events, we evaluate their impact on circuit yield sequentially and then derive an overall impact.

Effect of Process Variations

In order to determine the robustness of our circuit to process variability, we perform Monte Carlo simulations of the transistor level simulation configuration with the low input noise power level by varying the Ws and Ls of transistors.

For single transistors we define W variations as:

$$W = [(W_n - 1) + 1(\pm 3\%)]\mu m \tag{2.10}$$

where W_n is the nominal W. For the matched transistors we define an extra mismatch parameter, $w_m = 0.1(\pm 1.5\%)\mu m$, which is added to the W.

$$W = [(W_n - 1.1) + 1(\pm 3\%) + w_m]\mu m \tag{2.11}$$

The length L is defined as $L = 0.7(\pm 4\%)\mu m$ for all transistors also a geometrical matching parameter, $l_m = 0.1(\pm 1.5\%)\mu m$ is defined and added to the transistor that are close to each other in the layout.

$$L = [0.7(\pm 4\%) + l_m]\mu m \tag{2.12}$$

Based on the digital response of the 5 measurements we decide on a pass/fail condition by majority voting. Out of the 100 Monte Carlo runs, we have only 2 cases where the circuit yields incorrect result using the majority voting mechanism.

Effect of Thermal Noise

The noise measurement system also produce thermal noise, which may impact the accuracy or the sensitivity of the overall measurements. As indicated in Section 2.3.3, the noise generated before the squarer block will add an offset to the overall measurement. Theoretically, this offset will be the same for both the sinusoidal signal input and the actual noise signal input. However, due to the limitation in the time window size, there may be slight fluctuations in this offset amount, creating a mismatch between the set threshold and the noise signal to be measured. Moreover, noise generated after the squarer block may not completely average out during the operation. This integrated noise is another source of error.

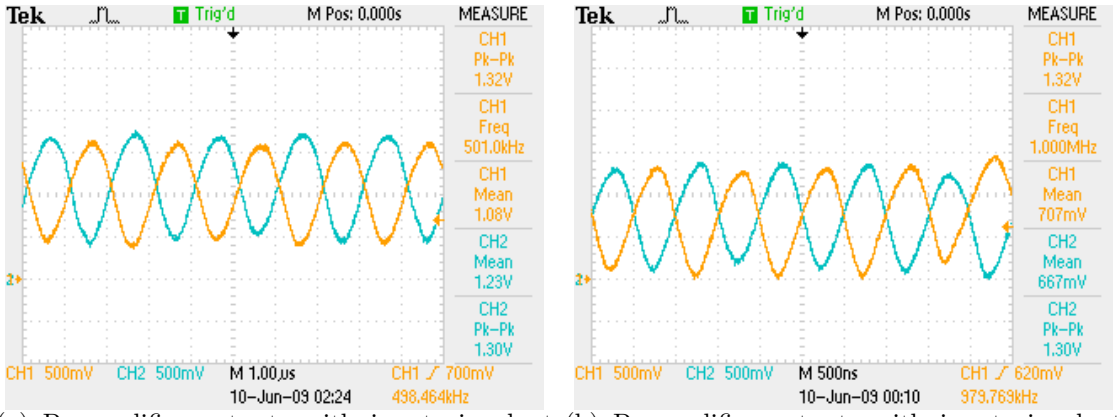
In order to evaluate the effect of both sources of error, we run Monte-Carlo simulations on the noise patterns for the measurement circuit. Based on our majority voting scheme over 5 windows and for 100 Monte-Carlo runs, the system response yields a misclassification for only 2 cases, resulting in a 98% yield.

Overall Yield

Since the two sources of yield loss (random nature of noise and process variations) are uncorrelated, we estimate the overall yield of the system by the product of the two individual yields. Thus, the overall yield of the system is 96% for an accuracy level of 2.5%. If this number is not satisfactory, the number of integration windows can be increased at the expense of test time.

2.4.3 Test Chip Measurements

We started measurements of the fabricated test chip from verifying the TD Squarer block and the PLL. After verifying the test chip functionality, we collected coherent signal samples form the PLL output and the TD Squarer Block output to verify the relation between the noise power at the VCO control input and the in-band phase



(a) Preamplifier outputs with input signal at 500KHz

(b) Preamplifier outputs with input signal at 1MHz

FIGURE 2.10: Preamplifier outputs with 10mV (peak) input signal

noise of the PLL output.

TD Squarer Block

As mentioned earlier, the TD Squarer Block contains both the preamplifier and the squaring amplifier. We tested the preamplifier with an input signal applied through a DC blocking capacitor. In Figures 2.10(a) and 2.10(b), the preamplifier differential output signals are shown for $10mV$ amplitude (peak) input signals with frequencies $500kHz$ and $1.0MHz$ respectively. The voltage gains of the differential arms are around $35dB$ for both frequencies and there is only $0.1dB$ gain mismatch between differential arms.

The differential output signals of the preamplifier are applied to the squaring amplifier with DC blocking capacitors since the DC levels of the preamplifier outputs and the squaring amplifier inputs do not mach. In Figure 2.11 the output of the squaring amplifier is shown together with the preamplifier outputs for an input signal with $3mV$ amplitude (peak) at $100kHz$. As can be seen, the output signal of the squaring amplifier has twice the frequency of the preamplifier differential outputs indicating the squaring operation.

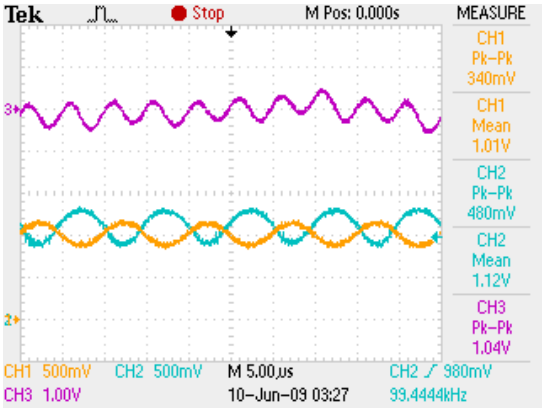


FIGURE 2.11: Squaring amplifier output signal

Charge Pump PLL

In the PLL design, in order to enable the use of sinusoidal reference signals, the reference signal input is buffered by multiple inverters. Since the phase detector is built with digital logic gates, this buffer structure is required to transform sinusoidal waveforms to digital square waves. There is not any frequency divider implemented on the feedback path. Therefore, the output signal of the PLL and the reference input signal have the same frequency ranging from $1MHz$ to $65MHz$. The output of the PLL has a buffer structure similar to the reference input. Thus, it generates a square wave having a DC offset equal to half the supply voltage. In Figure 2.12, the PLL output signal and the VCO control signal can be seen for a $10MHz$ reference input signal.

We compared the phase noise performances of the standalone VCO signal at $10MHz$ and the PLL output signal obtained with a $10MHz$ reference input signal in order to verify the PLL functionality. Figure 2.13 plots the power spectral density (PSD) of open loop VCO output signal and the output signal of PLL containing the same VCO. As can be seen from Figure 2.13, the PLL filters out the phase noise of the VCO and generates a much cleaner signal.

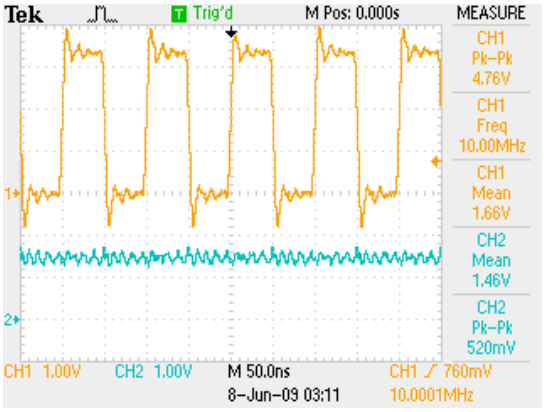


FIGURE 2.12: PLL output and VCO control signal for 10MHz reference input signal

VCO Input Noise Power and PLL Phase Noise Correlation Measurements

In the correlation measurements, our main goal is to verify the theory behind our test method. As explained in Section 2.2, the noise power at the control input of the VCO has a one-to-one mapping to the in-band phase noise at the output of a synthesizer. By looking at the noise power at the VCO input, we can predict

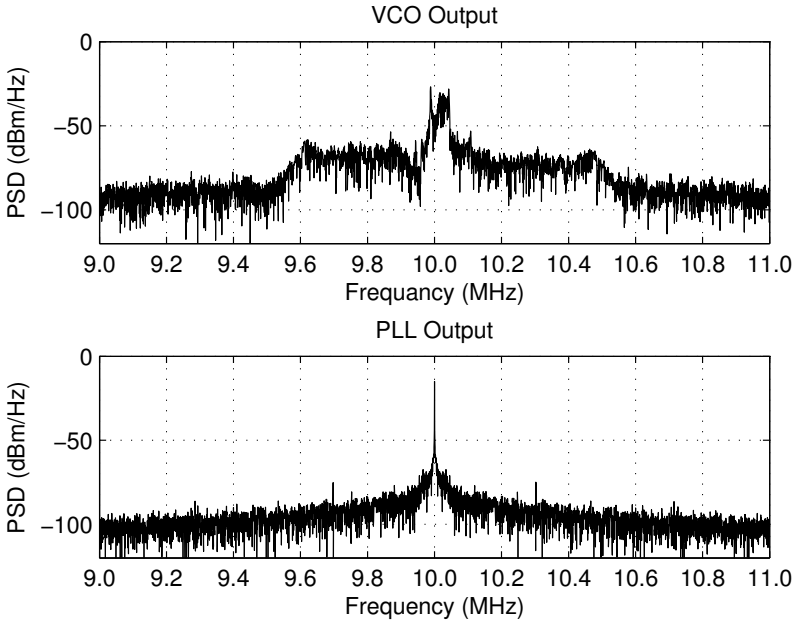


FIGURE 2.13: PSD of VCO signal and PLL output signal at 10MHz

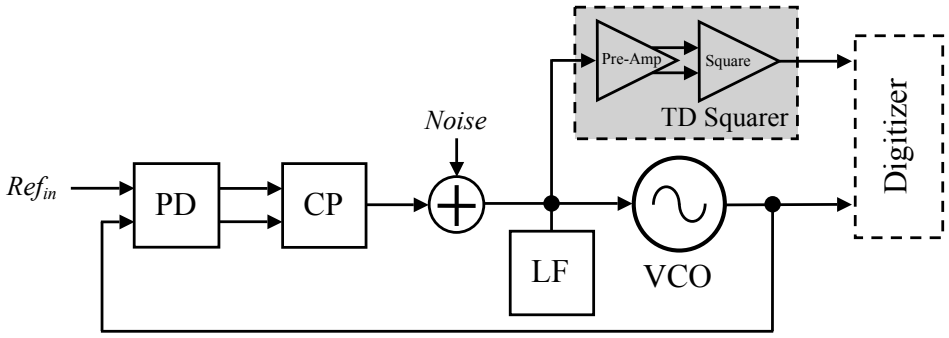


FIGURE 2.14: The measurement setup

the phase noise performance of the PLL. One way of proving this mapping is to take measurements from various test chips and analyze the measurement data for any correlation. Eventually, the test chips would have slightly different phase noise characteristics due to process variability, which maintains enough dimensions in the collected test data to extract the mapping function. This would be a perfect solution, if we could take sample chips from a production line. However, we do not have many test chips to measure.

We solved this data collection problem by injecting Gaussian noise signals to the control pin of the VCO with different power levels. A different PLL circuit instance is generated with the injection of the noise signals having different power levels. An arbitrary waveform generator with a MATLAB interface is used to generate necessary noise signals at desired power levels (with $5dB$ steps). The measurement setup to collect correlation data is shown in Figure 2.14.

The signal at the control pin of the VCO is fed to the TD squarer block in order to obtain the squared version. The output of the TD squarer block and the PLL output are captured with a digitizer card for various frequencies of the reference input signal. The captured signal samples are transferred to MATLAB to calculate the in-band output phase noise and the noise power at the VCO control pin.

We collected measurement data for reference input signals at $10MHz$, $12MHz$ and $15MHz$ while injecting noise signals with $5dB$ power steps. For each frequency of

Table 2.3: In-Band phase noise and VCO input signal noise power correlation

Reference: 10 MHz		
VCO Input Noise Power (dBm)	In-Band Phase Noise (dBc/Hz)	Difference (dB)
-42.69	-55.71	-13.02
-36.96	-50.34	-13.38
-32.35	-42.41	-10.07
-28.29	-40.98	-12.68
-23.60	-33.96	-10.36
-18.76	-30.03	-11.26
Difference: Mean = 11.79 dB STD = 1.30 dB		

Reference: 12 MHz		
VCO Input Noise Power (dBm)	In-Band Phase Noise (dBc/Hz)	Difference (dB)
-42.55	-55.82	-13.27
-36.63	-49.42	-12.78
-32.38	-46.33	-13.94
-28.24	-40.55	-12.31
-23.57	-36.98	-13.40
-18.72	-30.19	-11.47
Difference: Mean = 12.85 dB STD = 0.80 dB		

Reference: 15 MHz		
VCO Input Noise Power (dBm)	In-Band Phase Noise (dBc/Hz)	Difference (dB)
-42.49	-54.94	-12.45
-36.97	-49.39	-12.42
-32.21	-45.25	-13.04
-28.16	-39.97	-11.81
-23.56	-36.14	-12.58
-18.70	-30.88	-12.18
Difference: Mean = 12.41 dB STD = 0.37 dB		

the reference input signal, we measured the in-band phase noise and the VCO input noise power for each injected noise power level. In Table 2.3, measured noise power and in-band phase noise values are tabulated according to the reference frequency. As can be seen, the Difference column of Table 2.3, which effectively indicates the gain of the transfer function given in Equation 2.1 for that frequency, has varia-

tion less than $1.5dB$ for all measurement frequencies. In fact, the variation of the Difference column is mainly due to the in-band phase noise measurements. The noise power measurements of the same injected noise levels are very consistent for all measurement frequencies.

2.5 Summary

We have proposed a go/no-go BiST system for the synthesizer phase noise. Our technique takes advantage of the inherent relation between the output phase noise of the PLL and the amplitude noise on the control voltage of the VCO. We design a BiST circuit that is capable of determining whether the low frequency band-limited integrated noise power at the input of the VCO is above a given threshold. This information effectively enables a pass/fail decision on the synthesizer circuit based on its phase noise specifications.

Our proposed circuit performs a square operation followed by a limited-time integration to calculate the energy of the noise signal. The circuit has a calibration phase that sets a threshold for the noise power level to determine the pass/fail condition. This calibration sequence obviates the need to rely on the absolute values of the circuit parameters. In addition, the effects of process variability are minimized in the calibration phase by the offset cancellation feedback.

Monte-Carlo simulations that take both the process variations and the random nature of noise signals into account indicate that our circuit gives incorrect decisions in only 4% of cases for an accuracy level of 2.5%. Measurements on the fabricated test chip proved the proposed functionality of the implemented portion (TD Squarer) of the BiST circuit. Moreover, the data collected with this circuit on the simple charge-pump PLL implemented in the test chip, yields $1.3dB$ maximum measurement variation of the proposed test method.

3

BiST Method for ADCs

As the feature sizes for semiconductor devices decrease with the advances in the semiconductor technology, the severity of the role of process variations increases. Therefore, in new RF transceiver designs engineers choose to digitally implement as much circuitry as possible since digital circuits are more robust to process variations. However, RF operation and data conversion are inevitable duties that should be performed with mixed-signal devices. This trend results in mostly digitally implemented RF transceivers containing analog RF front-ends and mixed-signal data converters.

Analog to digital converters, which are common mixed-signal blocks in today's digital communication circuits, require expensive mixed signal testers in the production test. In order to obviate the reliance on mixed-signal testers, researchers have proposed to use histogram based BiST techniques that are specifically tailored for ADCs [32–38] measuring static nonlinearity parameters, such as DNL and INL. Most histogram techniques require access to on-chip resources, such as a memory and a DSP. They also can not detect non-monotonic behavior of the ADC.

In this chapter, we propose an alternative analysis technique for ADC BiST that does not increase the test time appreciably in the absence of a large memory,

while also detecting non-monotonic behavior. Our technique uses a counter along with a bit-flip detector to record the code widths. Since code widths are recorded every time a code switch occurs, a full pass of the linear input ramp can be used to calculate static nonlinearity parameters and check for non-monotonicity. We present two implementation options depending on the availability of on-chip resources. With our sequential analysis scheme, we pipeline the data collection for each code with the data storage (or shifting) of an earlier code. Thus, our scheme can be used in conjunction with a digital tester or an on-chip memory and a DSP.

We also propose a linear ramp generator to be used as an on-chip test stimuli generator for the ADC testing. This ramp generator is implemented in CMOS 0.5μ technology and has a voltage control capability to adjust the slope of the ramp. Based on the post-layout simulations performed in HSpice, the ramp generator has 15-bit linearity on $1V$ full-scale range.

3.1 Alternative ADC BiST Scheme

The most critical parameters of ADCs are DNL, INL, offset voltage and gain. Thus, BiST work on ADCs has concentrated on these parameters [33–35,37,38]. Histogram analysis is a powerful tool to measure code widths when input signals do not follow each code sequentially (e.g. sinusoidal inputs). The ramp input is a special case since it passes through each code sequentially. This property of the ramp input can be exploited to reduce the reliance on the on-chip resources.

3.1.1 The BiST Scheme and Implementation

As an alternative to histogram analysis, we propose a different output analysis scheme. Rather than relying on measuring the *code frequency* as in the histogram technique, our technique uses a counter along with a code change detector to directly measure the *code width*. By sequentially passing through each code and recording

the code width, our technique can also detect non-monotonic behavior.

In order to measure the widths of the output codes, a slow ramp signal is needed. The implementation of the on-chip ramp generator will be discussed in the next section.

With a given ramp signal input, the code widths at the output are automatically translated to time durations such that they can be measured by a simple on-chip counter. After the transition from one code to another, the counter value is recorded and then the counter is reset to measure the width of the next code. Since there is at least one bit flip from one code transition to another, a simple bit-flip detector composed of XOR gates and an OR-tree can be used to detect the code transitions.

The sequential analysis also enables the detection of non-monotonic behavior. To test for non-monotonicity, we employ a second counter that is incremented every time there is a code change. A mismatch between the ADC output and the counter value indicates non-monotonic behavior (missing codes).

We will discuss two options to implement the proposed technique based on the availability of on-chip resources. First, we will assume that the chip contains an accessible on-chip memory (a buffer) and an on-chip DSP as suggested in of most prior work [33–35] (option 1). In this case, the width of each code can be recorded in the buffer and analyzed by the DSP as shown in Figure 3.1. In order to increase the accuracy of measurements and reduce the effect of noise, multiple passes through the codes are preferred. Therefore, the code width values will be updated after each pass by the addition operation of the DSP. Finally, the DSP analyzes the results and makes a pass/fail decision. The additional resources needed for the BiST scheme are two counters, and the code transition detector.

The advantage of this scheme over the histogram analysis is that the memory does not need to be accessed every clock cycle. Memory accesses only occur after each code transition, thus a slower access does not inhibit the application of our

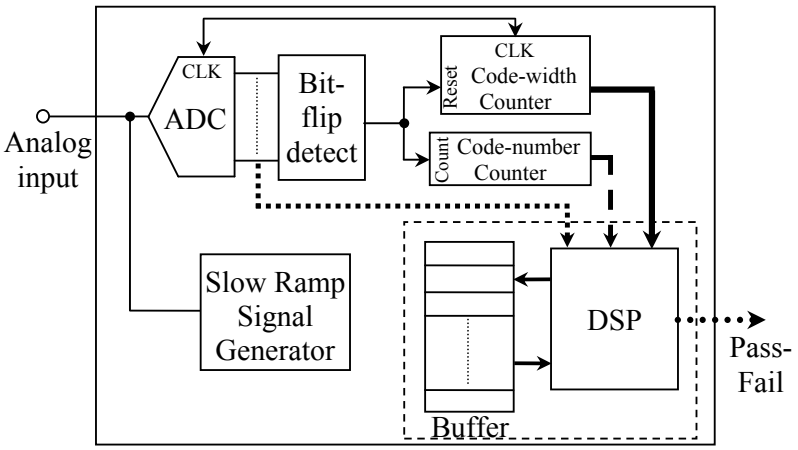


FIGURE 3.1: The BiST scheme with the DSP and the buffer

technique.

In the second implementation option (option 2), where there is no available on-chip memory or the memory is not accessible due to layout limitations, the values of the counters and the ADC output code are written to the registers as shown in Figure 3.2. During the measurement of the current code width, the previous code width measurement is scanned out to the digital tester from the registers. Multiple passes are also possible such that the results are updated by the digital tester after each pass.

Application of histogram techniques when there is no available on-chip memory requires collecting each code's data in a sequential manner [34,35], increasing the test time by 2^n where n is the ADC resolution. With our technique, the test application does not change.

3.1.2 Implementation Details

The proposed BiST scheme uses 2 counters, a bit-flip detector, and up to 3 registers (depending on whether option 1 or option 2 is used).

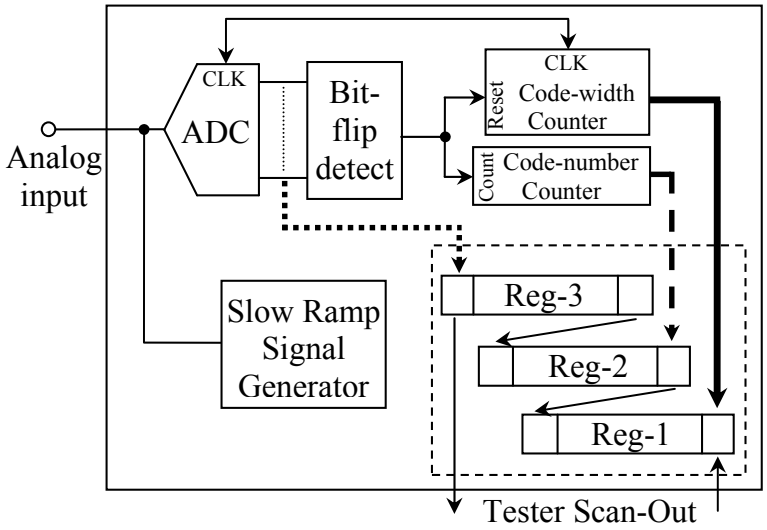


FIGURE 3.2: The BiST scheme with the digital tester

The Bit-flip Detector

The bit-flip detector is composed of n, $2-bit$ shift registers to compare the current digital code with the previous one. With each output from the ADC, shift registers will shift and the difference between the two output codes will be detected by an XOR-OR network.

The Counters

The desired accuracy of the test scheme determines the size of the code-width counter. For example, an ADC test with 16 hits-per-code (HPC: total number of conversions per ADC code) and $0.5LSB$ maximum DNL requires a final counter value of 25 $(16 \times 1.5 + 1)$ assuming that the maximum acceptable code width is 24. Therefore, a $5-bit$ counter is sufficient for this test setup for a $1/16LSB$ accuracy. The code-number counter should be the same size as the ADC resolution since there are 2^n digital output codes to be passed.

Additional Components Needed for Option 1 and Option 2

According to the two previously mentioned implementation options, the BiST scheme will utilize different on-chip resources. In option 1, where a buffer and a DSP are available, the analysis is performed by the DSP using the recorded values in the buffer. The size of the storage needed in the buffer is determined by the desired accuracy and by the number of repeated measurements of the BiST scheme. In the second case, three required scan-out registers should be able to keep the numbers generated by the counters and by the ADC. Therefore, their sizes depend on the ADC resolution and the size of the code width counter.

3.1.3 Accuracy, Test Time and Area Overhead Analysis

Clearly, the test time and the implementation area mainly determined by the resolution of the ADC as well as the desired accuracy of the test scheme. The accuracy of the test scheme is impacted by three factors: HPC, noise, and the linearity of the ramp. The error due to the quantization of the code width can be calculated in terms of LSB by:

$$\varepsilon_{HPC} = \frac{1}{HPC_{ramp} \times N} = \frac{1}{HPC}, \tag{3.1}$$

where N is the number of passes through the ramp.

The measurement error due to the nonlinearity of the ramp signal can be determined in a similar manner:

$$\varepsilon_{NL} = \frac{1}{2^{(N_{ramp} - N_{ADC})}}, \tag{3.2}$$

where N_{ramp} represents the linearity of the ramp signal.

The accuracy also depends on the thermal noise in the system, where the random noise spikes may result in incorrect data conversions. The impact of thermal noise on the accuracy can be evaluated assuming Gaussian distribution for the amplitude

of the noise spikes having an average of 0 and standard deviation of σ_n. If we call the fractional part of the analog input signal as v_f, which has a uniform distribution, $p_v(v_f)$ from 0 to $1LSB$, the amplitude of the noise spike should be either smaller than $-v_f$ or greater than $LSB - v_f$ to change the digital output code. The probability of incorrect output code due to the noise spike can be calculated as:

$$P_n = 2 \times \int_0^{0.5LSB} p_v(v_f) \times [\int_{\frac{0.5LSB-v_f}{\sigma_n}}^{\infty} p_n(u)du]dv_f, \tag{3.3}$$

where $p_n(u)$ is obtained by a change of variables:

$$p_n(u) = \frac{1}{\sqrt{2\pi}} \exp(-u^2/2). \tag{3.4}$$

If the distribution of v_f is discretized and the integration inside the square brackets is referred as the Q function, the probability can be recalculated as:

$$P_n = 2 \times \frac{1}{K} \sum_{i=1}^{K} Q(\frac{0.5LSB - v_f(i)}{\sigma_n}), \tag{3.5}$$

where $v_f(i) = i \cdot 0.5LSB/K$.

Using the probability obtained for incorrect conversion, the error in the DNL measurement due to the thermal noise effects can be calculated as:

$$\varepsilon_n = \sum_{i=1}^{HPC} C(HPC, i) P_n^{(i)} (1 - P_n)^{(HPC-i)} \frac{i}{HPC}. \tag{3.6}$$

Since all error components are uncorrelated, the overall error will be:

$$\varepsilon_{overall} = \varepsilon_{HPC} + \varepsilon_{NL} + \varepsilon_n \tag{3.7}$$

It is also clear from Equation 3.7 that increasing HPC beyond a certain point will not necessarily increase the accuracy. As an example, for an $LSB = 61\mu V$, a $\sigma_n =$

$0.01LSB$ (corresponding to $-191dBm/Hz$ noise PSD for a $100MHz$ bandwidth), and $(N_{ramp} - N_{ADC}) = 3$ the error due to ramp linearity, (ε_{NL}) will become the dominating factor (i.e. $\varepsilon_{NL} > 10\varepsilon_n$, $\varepsilon_{NL} > 10\varepsilon_{HPC}$), when $HPC = 80$. Therefore, increasing HPC beyond 80 will not provide any benefit for the measurement error.

The test time is determined by the ADC properties, such as the resolution and the sampling frequency $F_{sampling}$ as well as HPC. The total test time can be calculated by:

$$TestTime_{Total} = \frac{HPC \times 2^n}{F_{sampling}} sec. \tag{3.8}$$

The required slope of the ramp signal for a given full-scale-range FS of the ADC can also be calculated with the test parameters as:

$$RampSlope = \frac{F_{sampling} \times FS}{HPC_{ramp} \times 2^n} Volts/sec. \tag{3.9}$$

The area overhead introduced by the digital part of the BiST scheme will be negligible for both of the options of available on-chip resources since the added blocks are the counters, the bit-flip detector and a maximum of three registers.

3.1.4 Comparison with Histogram Techniques

Since the accuracy is mainly determined by HPC, the accuracy of our test scheme is the same as the histogram methods with equal test time.

If an available on-chip memory is assumed (option 1) our scheme also has the same test time as the histogram technique. The advantage of our scheme for option 1 stems from the fact that memory does not have to be accessed every clock cycle. For the histogram methods without an on-chip memory [33–35], our method will utilize similar implementation area but a very short test time since the time decomposition technique increases test time exponentially as the resolution of the ADC increases. As an example,in our test method without any on-chip memory, a $14 - bit$ ADC

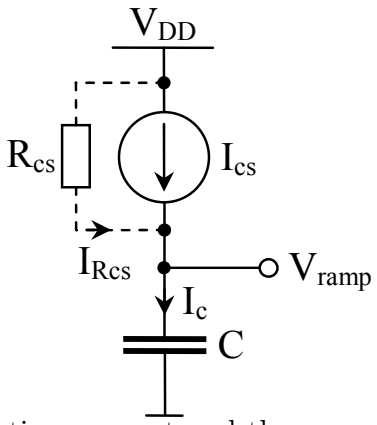


FIGURE 3.3: Ramp generation concept and the current source output impedance

can be tested in 0.5 seconds at the sampling frequency of $1MHz$ with an accuracy of $0.03LSB$. The same test would require more than 5 hours with the histogram method proposed in [35].

Another advantage of our scheme is that it can detect the non-monotonic behavior of the ADC.

3.2 On-Chip Ramp Generator

A common way to generate a voltage ramp is to charge a capacitor by a constant current source as shown in Figure 3.3. The capacitor voltage will be the ramp voltage having the following expression:

$$V_{ramp}(t) = \frac{I_c}{C} \cdot t, \tag{3.10}$$

where I_c is the current that charges the capacitor C over the time period t.

Since the current source is implemented using a MOS transistor, its finite output impedance, as shown in Figure 3.3, deviates the ramp voltage from its ideal value and decreases the linearity of the ramp signal.

3.2.1 Ramp Generator with Feedback

A carefully designed circuit should fix the voltage on the current source such that the charging current will be *constant*. To obtain an almost constant voltage on the current source, a differential amplifier can be used in a feedback configuration [23] as shown in Figure 3.4.

If the differential amplifier is ideal i.e. with infinite gain, the circuit will behave as the circuit in Figure 3.3 except for the direction of the ramp signal (a negative ramp). If the differential amplifier has a finite gain i.e. A, the voltage on the current source will vary but the variation is limited to only a fraction of the ramp voltage, which is:

$$\Delta V_{cs}(t) = \frac{V_{ramp}(t)}{A}. \tag{3.11}$$

Therefore, the output impedance degradation effect can be lowered by increasing the gain of the differential amplifier. The direction of the ramp signal can be easily inverted through an inverting amplifier, which also allows us to increase the effective overall gain. In order to adjust the final value of the ramp, a voltage controlled current source (VCCS) is needed to control the slope of the ramp.

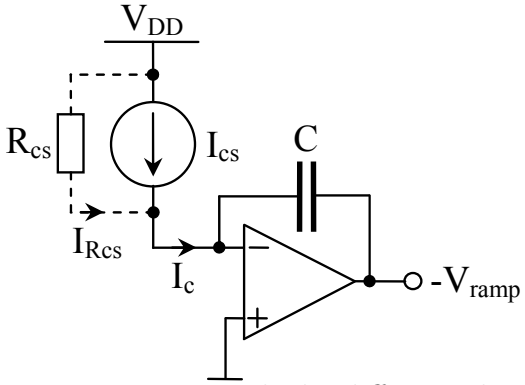


FIGURE 3.4: Ramp generation with the differential amplifier feedback

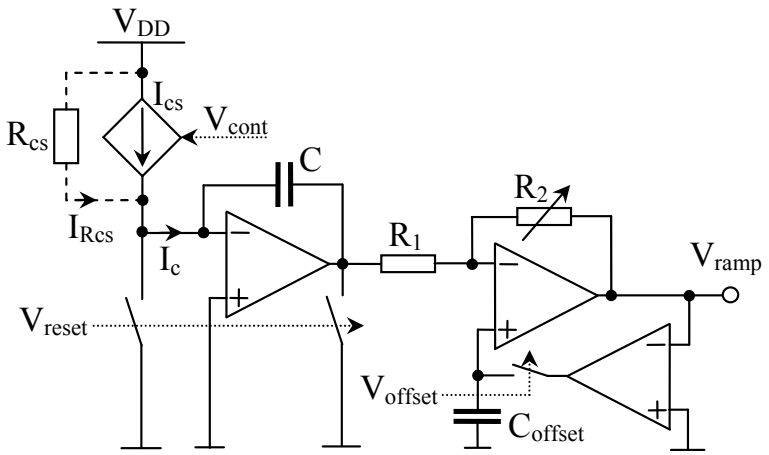


FIGURE 3.5: The complete ramp generator circuit with the offset cancelation

3.2.2 Offset Cancelation

We propose a simple offset cancelation feedback mechanism to initialize the beginning of each ramp to $\pm 10\mu V$ maximum. The feedback loop is composed of a switch, a capacitor and a differential amplifier such that the loop will be closed by a digital signal at the beginning of each ramp signal for a short period of time. The complete ramp generator circuit with offset cancelation feedback can be seen in Figure 3.5.

The overall circuit operation is controlled by two digital signals to initialize the ramp signal and an analog signal to control the slope of the ramp. This analog signal can also be used in a feedback loop as in [19,22,23] to automatically control the ramp slope in the presence of process variations.

3.2.3 Circuit Implementations

The VCCS and the differential amplifiers are implemented in $0.5\mu m$ CMOS process. The circuits are supplied with $\pm 1.65V$ supply voltages. The output stage transistors are adjusted to have minimum offset voltage at the outputs of the circuits.

The high output impedance VCCS is realized by a cascode current mirror and a high power supply rejection ratio (PSRR) self biasing network, which is controlled by the slope control voltage. The bias generated by the applied slope control voltage

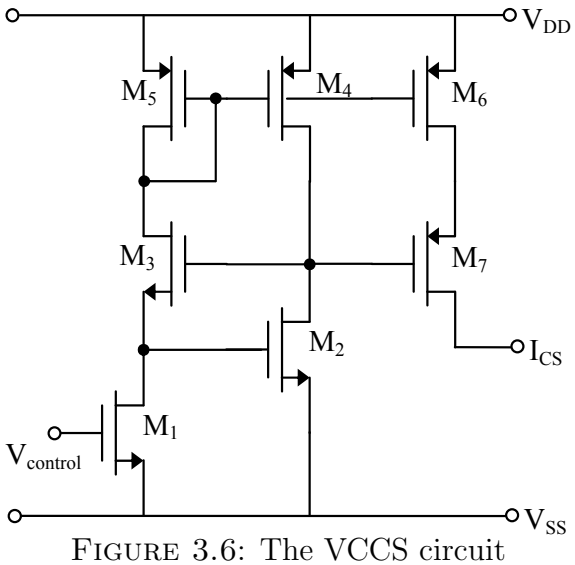


FIGURE 3.6: The VCCS circuit

in the self biasing network ($M1$ through $M5$), is turned into the capacitor charging current by the cascode current source of $M6$ and $M7$. The CMOS implementation of the circuit can be seen in Figure 3.6.

The amplifier block is a regular, two stage, differential input, single-ended output circuit [45].

The analog part of the BiST scheme which consists of the ramp generator covers a chip area of $0.017mm^2$ for an off-chip charging capacitor. With an on-chip capacitor the implementation area will be $0.9mm^2$. The chip layout of the ramp generator can be seen in Figure 3.7.

3.2.4 Post Layout Simulations

Post layout simulations are performed for each block in HSpice individually to determine the parameters of the VCCS and to adjust the compensation network for the stability of the differential amplifier.

In HSpice simulations, the ramp generator circuit is configured by the control signals to produce consecutive voltage ramps of $1ms$ duration with a full-scale range from $0V$ to $1V$. The final value of the negative ramp signal (the output of the

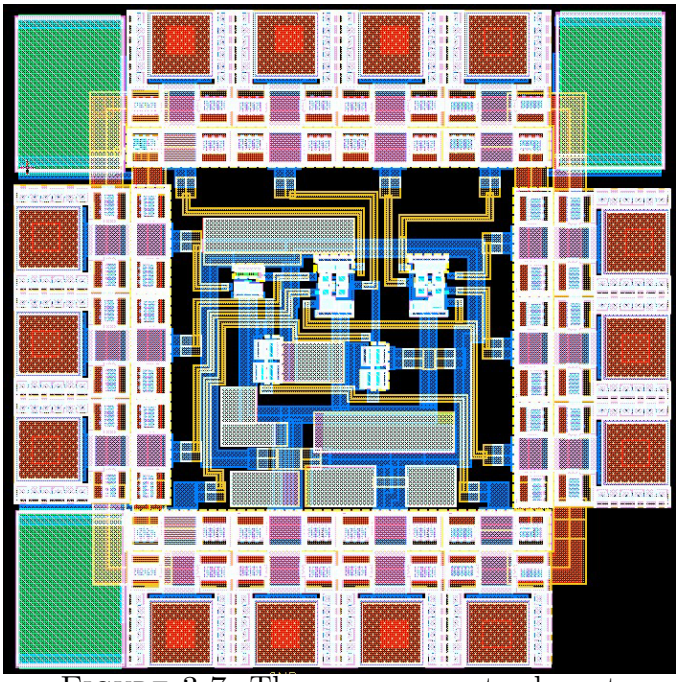


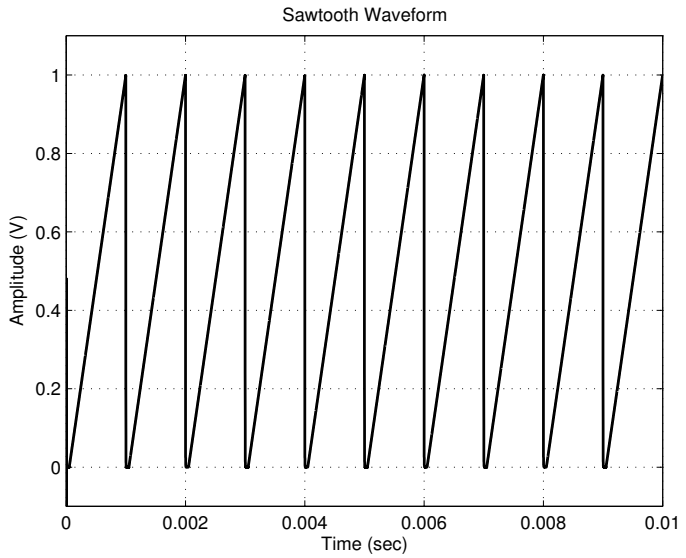
FIGURE 3.7: The ramp generator layout

first differential amplifier) is adjusted to $-0.5V$ by the slope control voltage. The inverting amplifier is set to have a gain of -2 to obtain the $1V$ final ramp value. At the beginning of each voltage ramp, the ramp capacitor is discharged by the switches and the output DC offset is canceled by the offset cancelation feedback loop. This initialization phase takes about 50μ seconds.

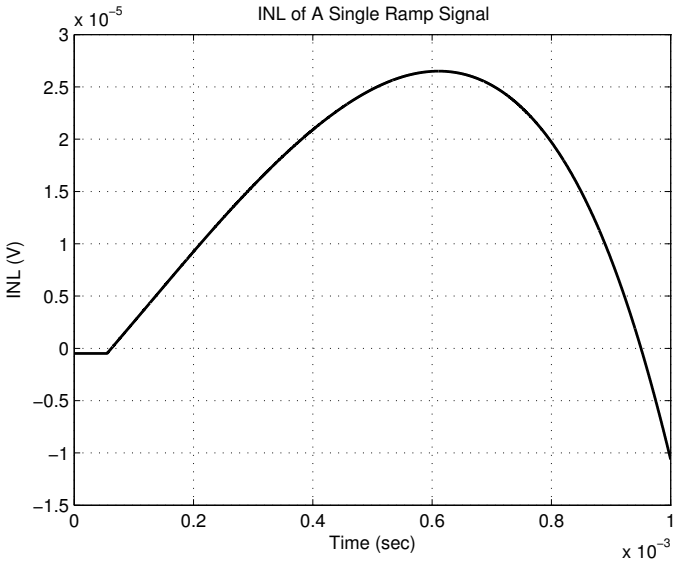
The overall circuit simulations show that the generated ramp voltage signal has $15-bit$ linearity over $1V$ full-scale range with $\pm 10\mu V$ maximum DC offset error around $0V$. In Figures 3.8(a) and 3.8(a), the plots of V_{ramp} sawtooth signal and the corresponding INL error for a single ramp are shown respectively.

3.3 Summary

We have proposed a complete ADC BiST scheme based on sequential code analysis at the output rather than code frequency analysis, as in histogram based testing. We also proposed a ramp generator with $15-bit$ linearity over $1V$ full-scale range.



(a) The generated V_{ramp} signal



(b) The INL error of a single ramp signal

FIGURE 3.8: Post layout simulation results

Our analysis scheme has several advantages over the traditional histogram based analysis. First, it is capable of detecting non-monotonicity. Second, when an on-chip memory is available, our scheme does not need fast access to the memory, which is practically hard to achieve. Third, when no on-chip memory is available, histogram based techniques require too long of a test time to be practically applicable, whereas

our scheme does not increase the test time. We believe the proposed sequential code analysis is preferable to histogram based techniques when ramp inputs are used.

4

Wafer Level Loop-Back RF Test

While manufacturing costs for RF devices have been on a downward slope, test and packaging costs have not followed suit making them an appreciable percentage of the overall cost. Increasing packaging costs make wafer level tests mandatory for overall cost reduction. In the wafer level test, the IC goes through a very simple test that validates the basic functionality of the silicon die. Some of the steps of the final production test have already been moved to wafer level. However, increasing the fault coverage of the wafer level tests may not always reduce overall costs because increased fault coverage requires longer test times. Moreover, testing a specific functionality and some specifications of the IC in the wafer level requires high-end test equipments and complex test setups. Therefore, simple wafer level tests may reduce overall costs as well as maintain the desired final yield by preventing defective dies from being packaged.

Generally, test of RF ICs requires high frequency test equipments. Due to very high output frequencies of the circuit under test (CUT), some of the specifications may even become impossible to measure because preserving the integrity of the observed RF signals is challenging while transferring from the CUT to the tester.

These drawbacks are more severe in the wafer level because of the RF probing issues at the silicon die interface. However, loop back test methodologies [5–12], which are simply based on feeding the transmitter output to the receiver input, may be utilized in wafer level tests to relax tester requirements and eliminate some of the drawbacks of RF test. In loop-back methods, IF or base-band signals are used to test the functionality and to measure specifications of the transceivers such that RF signal analysis is not necessary.

In this chapter, we propose a wafer level loop-back test method for catastrophic and large parametric (more than 25% variation) faults on the transmitter or the receiver paths of direct conversion transceiver architectures. A major challenge in loop-back based testing for RF transceivers is the frequency offset problem. This problem arises from the fact that most transceivers today employ an intermediate frequency that makes the transmit signal fall out of band for the receiver channel filter. Therefore, simple loop-back configuration will not produce a signal in the receiver pass-band. Our strategy to overcome this problem is to expand the bandwidth of transmitted signals so that some of the energy of the transmitted signal will fall into the channel filter pass-band, producing observable signals at the output. For output signal analysis, we propose to use frequency domain signatures since catastrophic faults as well as large parametric deviations may alter the expected signature.

4.1 The Transceiver and Loop-Back Connection

The transceiver system is composed of a transmitter and a receiver path as shown in Figure 4.1. During the transmit phase, the IF signal at the input of the transmitter path is up-converted by the mixer and amplified by the PA to drive the antenna. During the receive phase, the signal captured by the antenna is amplified by the LNA and down converted by the mixer. The system synthesizer or LO switches to appropriate carrier frequencies for the transmit and receive phases. Channel

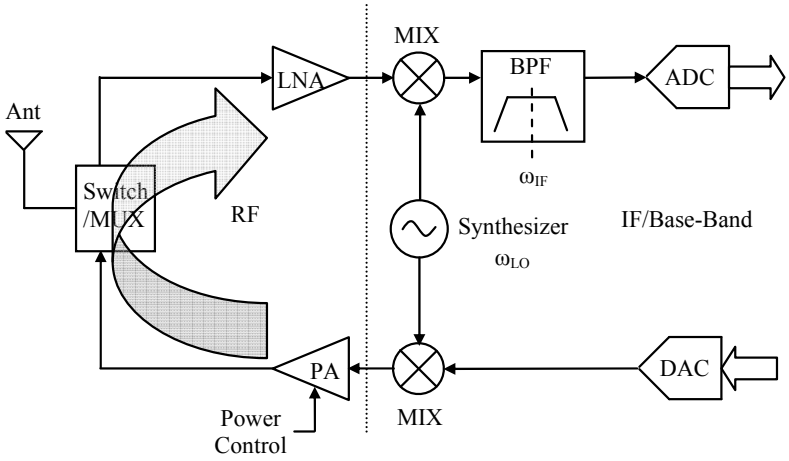
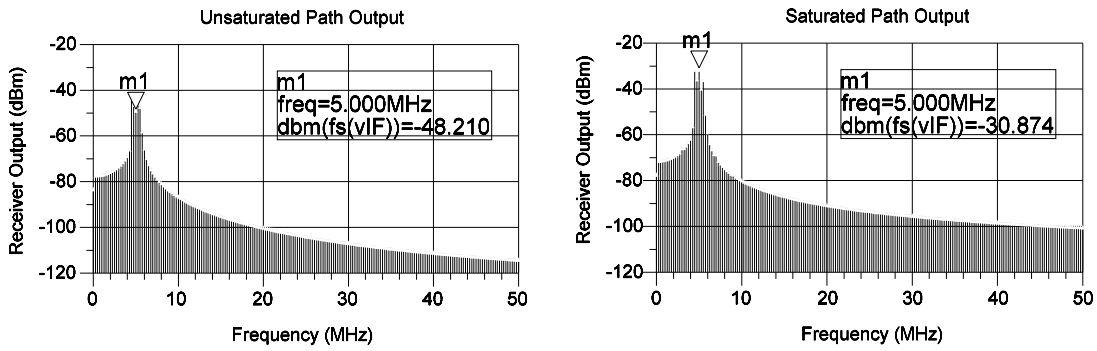


FIGURE 4.1: Direct conversion transceiver and the loop-back connection

selectivity is achieved by the channel filter following the mixer on the receiver side. The system may either have separate antennas for each path or a single antenna controlled by a RF switch-multiplexor block.

Transceivers are designed according to the thermal noise level of the system so that the ADC output codes will not change due to noise spikes. Therefore, the LSB of the ADC should be chosen higher than the noise floor at the channel filter output. Moreover, the non-linear terms at the output signal should also be kept below the noise floor otherwise, non-linear components of the adjacent channel signals may result in bit flips in LSB or higher bits. In the normal operation of the system, all the blocks should operate in their linear regions so that, non-linear terms of adjacent channel signals will be kept below the noise floor.

In the wafer level loop-back test, the CUT will be configured to feed the transmitter output signals to the receiver input as shown in Figure 4.1. Simple analog-RF switch DfT feature can be included to establish the loop-back path in the test mode. However, the PA output signals are usually too powerful to be fed into the LNA. Therefore, the analog-RF switch block should also have an attenuation capability [46] to adjust the power of the signal that enters the LNA.



(a) Unsaturated path response (b) Saturated path response

FIGURE 4.2: Receiver path responses

4.2 Loop-Back Test Strategy

One option to obtain an observable signal at the output is to saturate the receive path such that strong enough non-linear terms produced by the LNA or the Mixer will fall into the channel filter pass-band. The power of the signal entering the receive path can be increased by either decreasing the attenuation on the loop-back path or by increasing the power output of the PA via the power control feature. In Figure 4.2, unsaturated and saturated responses of the receiver path can be seen.

With the saturated receive path, the presence of a signal at the output may be useful for detection of catastrophic signal path faults because in the case of signal path fault, only the thermal noise will be observed at the output. Eventually, the ADC will filter out the noise since its mean will be lower than the LSB. On the other hand, if the system is fault free, the ADC output will toggle due to the non-linear terms generated by the saturated receive path.

A second option to detect signal path faults is to observe the frequency spectrum signature at the output of the channel filter. Since the looped-back transceiver path has a cascaded gain composed of the gains of signal path blocks, the output noise power will be different in the case of a fault on the signal path [47]. Therefore, without saturating the receiver path, observing the frequency spectrum signature

detects not only catastrophic faults but also parametric faults that affect gains of blocks on the signal path.

4.3 Faults and Simulation Setup for Loop-Back Test

In this work, we concentrate on catastrophic and large parametric signal path faults. We use receive-path saturation technique to detect catastrophic faults and frequency spectrum signature observation technique to detect large parametric faults.

4.3.1 Faults

During wafer level testing, the goal is to prune away catastrophically defective dies to prevent them from packaging. Therefore, we concentrate on such catastrophic defects. Our fault list consists of hard faults, which are modeled as broken connections at the transistor level and soft faults, which are modeled as large parametric deviations inside the transceiver. The deviations are injected into the widths of the transistors.

4.3.2 Simulation Setups

Simulation setups for both detection techniques are the same except for observing the output. ADC digital output codes are observed for the catastrophic faults whereas, frequency spectrum at the channel filter analog output is observed for large parametric faults.

Simulation circuit shown in Figure 4.3 for catastrophic faults is composed of the looped-back transceiver driven by an IF signal source and an ADC connected to the receiver output. The IF amplifier (IFA) is placed to obtain full-scale swing at the ADC input. ADC sensitivity (LSB) is adjusted to filter out thermal noise effects such that thermal noise spikes will not result in bit-flips at the ADC output.

In the simulation circuit shown in Figure 4.4 for detecting large parametric faults,

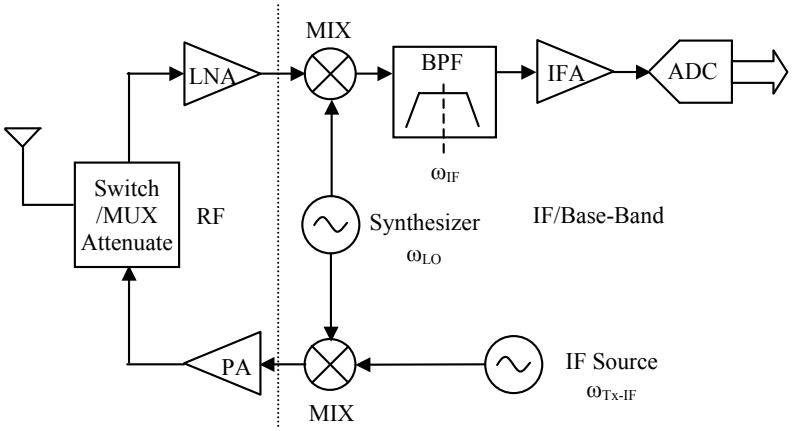


FIGURE 4.3: The simulation setup for catastrophic faults

the output of the channel filter is observed for any amplitude change in the frequency spectrum. Both saturated and unsaturated signatures of the system are captured for a comparison with faulty circuit responses.

4.3.3 Circuit Implementations

The transceiver blocks are implemented with $0.18\mu m$ CMOS process having $1.8V$ supply voltage and 50Ω input-output impedances. The RF carrier frequency for both blocks is $900MHz$.

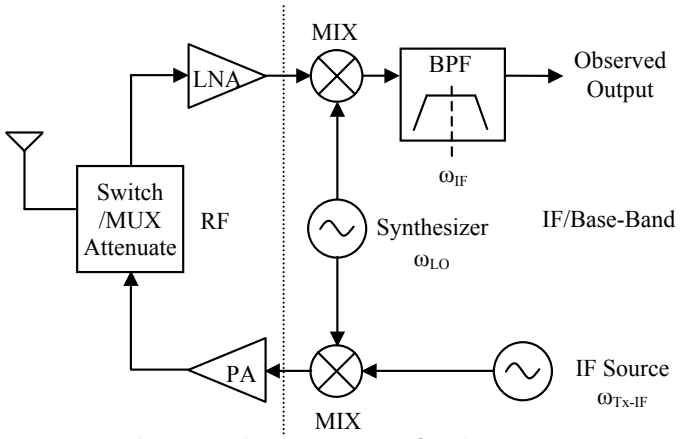


FIGURE 4.4: The simulation setup for large parametric faults

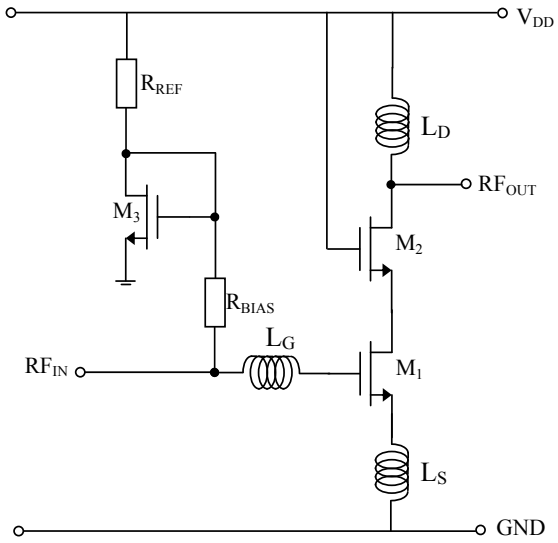


FIGURE 4.5: CMOS LNA Circuit

LNA

The LNA circuit, which is shown in Figure 4.5, is a cascode common source amplifier. The third transistor ($M3$) is responsible for biasing the other two. Power gain of the amplifier is $13.5dB$ with $1.0dB$ noise figure. IIP_3 and P_{1dB} are $4.5dBm$ and $-7.1dBm$ respectively.

Catastrophic faults for this circuit are breaks on the inductors whereas, large parametric faults are 25% variation on transistor widths (W).

Power Amplifier

The PA circuit shown in Figure 4.6 is a class AB type two stage amplifier with a power gain of $29.2dB$. The circuit has a noise figure of $2.7dB$. The linearity parameters of the PA are $-12.3dBm$ for IIP_3 and $-21.3dBm$ for P_{1dB}.

Large parametric faults defined for this circuit are 25% variation of widths of the two transistors. Similar to the LNA circuit, catastrophic faults are defined as breaks on the inductors and the interstage capacitor.

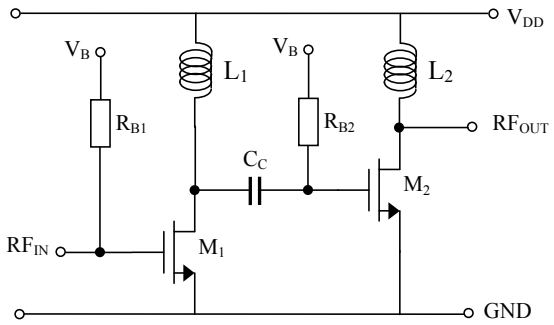


FIGURE 4.6: CMOS power amplifier circuit

Mixer

The mixer circuit is the CMOS implementation of the Gilbert Multiplier Cell. As seen in the simplified circuit schematic shown in Figure 4.7, resistive loads are used at the output to enable easy adjustment of output impedance. The circuit has $5.2dB$ conversion gain with $3.9dB$ single sideband noise figure and the linearity parameters are $3.2dBm$ for IIP_3 and $-9.5dBm$ for P_{1dB}.

Load resistors and gate-source inductors are considered for catastrophic faults. Similar to the other blocks, widths of the transistors are varied by 25% for the large parametric faults.

4.4 Simulation Results

Simulations are performed in separate sessions for catastrophic faults and large parametric faults according to the described techniques in Section 4.2. Catastrophic faults are tested according to the digital ADC output whereas, large parametric faults are tested with signature of the output frequency spectrum.

4.4.1 Catastrophic Faults

The idea behind catastrophic fault detection is to have a signal at the pass-band of the receiver. If there is a signal path fault that results in signal loss, there will not be any signal observed at the output. Therefore, an observable signal at the output

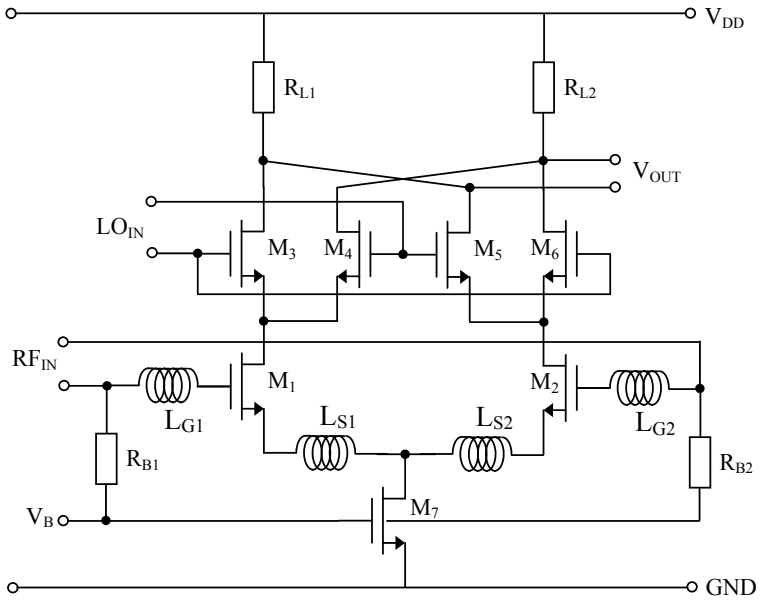


FIGURE 4.7: CMOS mixer circuit

means a *pass* for the test because an observable signal at the output means a fault free signal path from the transmitter IF input to the receiver IF output.

In fact, the observed signal is not the signal sent by the transmitter because the receive path is saturated with the transmitted signal to generate a signal at the receiver pass-band. The observed signal at the receiver output is the higher order nonlinear terms of the transmitted signal.

In order to discriminate observed signals from thermal noise, ADC input sensitivity is adjusted to filter out thermal noise. Normally, in receiver paths ADC LSB should not flip with noise spikes. ADC resolution, full scale range and IF amplifier gain are adjusted in the simulation circuit shown in Figure 4.3 to filter out thermal noise spikes and to maximize the dynamic range.

Once the proper operation of the transceiver is guaranteed with the available thermal noise, catastrophic faults can be simply tested by saturating the receive path and observing the ADC output for bit-flips. Lack of bit-flip indicates a signal loss, which means a catastrophic signal path fault.

Catastrophic faults declared for the transceiver blocks in Section 4.3.3 as well as the loop-back path and the interconnect faults were tested and all faults were detected in the presence of thermal noise.

4.4.2 Large Parametric Faults

As described in Section 4.2, large parametric faults will be tested with signatures generated from receive path frequency spectrum output. The signatures are collected from fault free circuit instances having 5% process variability. Using the collected signatures a frequency spectrum envelope is obtained determining the borders of the frequency spectrum signatures for fault free circuits. A fault will be detected, if the circuit response violates the frequency spectrum envelope.

Detecting large parametric faults with signature analysis can be in two ways: first, the faults can change the noise floor level depending on the fault location and the severity of the fault effect on the block gains [47]. Second, the fault may result in signal loss for the saturated receive path. In either case the faulty circuit response may violate the spectrum envelope. Therefore, we collected two sets of fault free circuit response for normal transmit power and for the transmit power that saturates the receive path. Spectrum envelopes shown in Figure 4.8 were obtained with the collected data sets from 500 circuit instances generated by Monte-Carlo simulations. The upper plot in Figure 4.8 is for normal transmit power spectrum envelope whereas, the lower plot is for transmit power saturating the receive path.

Signature comparison was done within the pass-band of the receiver channel filter which has $2MHz$ bandwidth centered around $5MHz$. For each fault, $\pm 25\%$ mean variation was assumed for the widths of the transistors. There were 3 faults for LNA, 2 faults for PA and 7 faults for the each mixer. Total of 19 faults were analyzed with the proposed method.

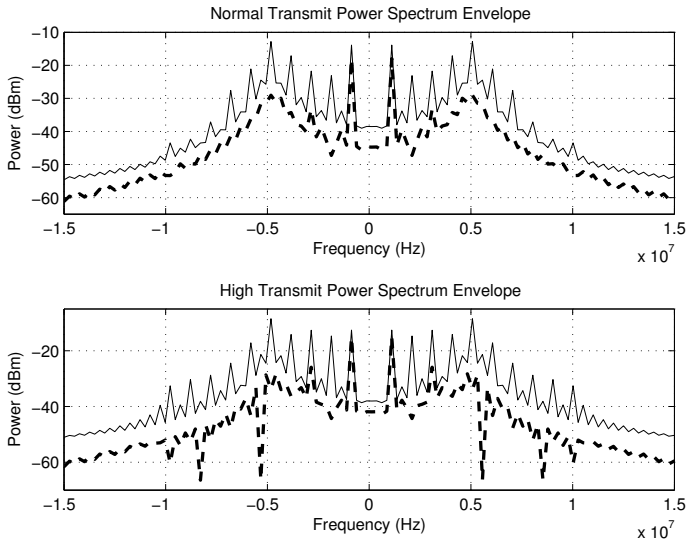


FIGURE 4.8: Spectrum envelopes for different transmit powers

4.4.3 Calculation of Failure and Yield Coverages

Fault coverage is not always a good metric since some faults may not result in a specification violation. Instead, we need to determine the failure coverage (i.e. how many of the failing circuits can we detect). We also should evaluate the yield coverage.

In order to determine the failure coverage and the yield coverage of the test method, circuit specifications (path gain and path IIP_3) are used to group all circuit instances as *acceptable* or *unacceptable*. We generate 500 Monte-Carlo samples having 5% process variability with no fault injection to obtain specification distributions and spectrum envelopes. Thresholds for the specifications are set to pass 97% of the fault free circuit instances. We then generate 200 Monte-Carlo samples for each fault.

We define pass/fail criteria on the signatures based on the response of the *acceptable* circuits. For circuits that are classified as *acceptable*, if the signature technique results in a *fail* decision, then we consider these circuits as *yield loss*. For circuits that are claimed as *unacceptable*, if the signature technique results in a *pass* deci-

sion, then we consider these circuits as *failure coverage loss*. We also include the probability of each fault occurrence into our computations. Here, we will assume a 90% overall yield. The overall failure and yield coverage (FC and YC respectively) for the proposed test method can be calculated as:

$$FC = 1 - \frac{1}{N+1}(FCLoss_{FaultFree} + \sum_{i=1}^{N} FCLoss_i) \tag{4.1}$$

$$YC = 1 - (0.9YLoss_{FaultFree} + \frac{0.1}{N}\sum_{i=1}^{N} YLoss_i), \tag{4.2}$$

where N is the total number of faults including 22 catastrophic faults tested with ADC response. $FCLoss_{FaultFree}$ and $YLoss_{FaultFree}$ are failure coverage loss and yield loss calculated for the fault free circuit instances.

Overall failure and yield coverage are calculated separately with frequency spectrum envelopes obtained with normal transmit power and high transmit power. Also the results are combined for both envelope comparisons. Overall failure coverage and and yield coverage figures are given in Table 4.1.

As can be seen from Table 4.1, overall yield coverage figures for both separate and combined spectrum envelopes are around 99%. However, failure coverage figures are around 70% due to the masking effect of process variations in the spectrum envelope. Since the spectrum envelope method basically compares magnitudes of the signals, the fault with severe effect on the transceiver block gains such as mixer RF-input port transistors ($M1$ and $M2$) widths can be detected very easily. On the other hand, faults with less effect on block gains have a low failure coverage. The

Table 4.1: Failure coverage and yield Coverage (%)

Signature Envelope	Failure Coverage	Yield Coverage
Normal Power	70.6	99.5
High Power	64.7	99.6
Combined	76.1	99.3

Table 4.2: Combined Envelope Failure Coverage (%)

Fault	Failure Coverage	Fault	Failure Coverage
$MIX1_{F1}$	99.0	$MIX2_{F1}$	88.4
$MIX1_{F2}$	100	$MIX2_{F2}$	97.9
$MIX1_{F3}$	42.3	$MIX2_{F3}$	36.4
$MIX1_{F4}$	26.7	$MIX2_{F4}$	30.0
$MIX1_{F5}$	28.0	$MIX2_{F5}$	36.8
$MIX1_{F6}$	35.0	$MIX2_{F6}$	13.3
$MIX1_{F7}$	18.9	$MIX2_{F7}$	84.4
LNA_{F1}	86.7	PA_{F1}	29.7
LNA_{F2}	20.5	PA_{F2}	71.4
LNA_{F3}	25.0		

individual failure coverage for large parametric faults are given in Table 4.2.

4.5 Summary

We have proposed a loop-back test method for wafer level verification of transceiver circuits for detecting catastrophic and large parametric faults. In the proposed method, the transmitter output is directly connected to the receiver input with simple RF attenuator-switch DfT feature. To obtain an observable signal at the output of the receiver, the receive path is saturated with the high power from the transmitted signal in order to expand the bandwidth of the received signal.

The results of the simulations show that loop-back test method utilizing the use of out-of-band signals can be used for catastrophic signal path fault detection. Once the dynamic range of the system is known, a catastrophic fault on the signal path can be determined by observing the output signal from ADC output codes since lack of a code change indicates a signal path break.

We also proposed a signature analysis method based on frequency spectrum envelopes for large parametric signal path faults. Fault free circuit responses are collected to obtain spectrum envelopes and faulty circuit responses are compared with these envelopes for fault detection. An envelope violation indicates the presence of

a large parametric fault. Failure and yield coverage for the proposed method are calculated according to the chosen specifications of the system. Although overall yield coverage for the test method is satisfactory, failure coverage figures should be improved for the faults being transparent for the spectrum envelope comparison technique.

5

Loop-Back Based RF Transceiver BiST

Continuous demand for high functionality, faster and smaller electronic devices challenges circuit and system designers for new techniques. In parallel to advances in semiconductor technology, circuits and data processing methods evolve enabling high level of system integration in much smaller volumes. Highly integrated System on Chip (SoC) or System in Package (SiP) designs have already started to take control over the market since they provide single-device solutions for consumer electronics manufacturers in almost all market segments. These designs contain not only analog but also digital subsystems to establish functionality of a complete system. An example can be the single chip IC for mobile phones which may contain mixed signal and digital blocks, such as data converters and DSP cores besides to analog transmitter and receiver blocks.

Due to the integration and power consumption requirements, low complexity RF front-end modulation techniques, such as I/Q modulation are preferred in the transmitter/receiver blocks. In I/Q modulation RF front-end implementation, signals are transmitted through two channels with orthogonal carriers having 90° phase difference.

High operating frequencies and increasing data rates dictate more stringent performance requirements. Impairments in the analog/RF front-end, such as the I/Q imbalance and nonlinearity, severely affect the device performance. With the increasing use of wide-band communications, the I/Q time skew also becomes a limiting factor [41].

To compensate some of the impairments of RF transceivers, baseband signal processing techniques have been introduced [48–53]. These techniques can be grouped into two as data-aided and non-data-aided compensation. Data-aided methods are mainly based on adaptive filtering and signal estimation algorithms which use a reference signal or training signals for convergence [51, 52]. Non-data-aided methods do not require any reference signal or training signals. They obtain signal estimates by statistical analysis [48], and special methods based on source separation [49]. Blind source separation (BSS) [49], which is an example for source separation methods, builds a separation matrix (based on an equivariant adaptive separation algorithm explained in [50]) to recover I/Q signals in the presence of carrier phase and frequency offsets.

These compensation methods are mainly developed for I/Q mismatch to be used in the receiver digital baseband [53]. They are not dedicated to be used in manufacturing test because quantitatively measuring the gain and phase mismatch parameters between I and Q arms is not the objective.

Traditionally, the transceiver system is tested in two steps with separate setups for transmitter and receiver paths utilizing high-calibre RF instrumentation and mixed signal testers. Since today's transceiver systems contain many on-chip functional blocks, BiT approach receives much attention [9–11] recently. In this approach, the required test is performed with available on-chip functional blocks. In some test methods, which are also known as BiST, the DUT may generate the actual test results.

In BiST approaches for transceiver systems, the circuit blocks are configured in a loop-back mode to obtain a continuous signal path from the transmitter baseband input to the receiver baseband output in order to eliminate the need of RF instrumentation. Researchers have used the loop-back setup for transceivers to measure circuit characteristics [5–12, 39].

In this chapter, we focus on testing I/Q modulating transceiver systems in the loop-back mode. We propose two BiST methods, which are both capable of decoupling transmitter and receiver impairment parameters. They analyze only low frequency baseband I/Q signals in the digital domain to extract the parameters.

The proposed BiST methods have differences in the transceiver baseband modulation schemes, the decoupled impairment parameter set and the parameter extraction technique. The first method is applied to I/Q modulating transceiver using QPSK baseband modulation scheme. I/Q mismatch, I/Q time skew and receiver DC offsets are the impairment parameters for this method to be extracted with the Least Squares (LS) estimation method [54, 55]. In the second BiST method, we generalize the first method to accept any baseband modulation scheme. We also extend the list of impairment parameters to include transmitter and receiver nonlinearity characteristics. The parameters are extracted by the Nonlinear Least Squares (NLS) technique [56–58] which is applied on the data collected in two consecutive measurements having different loop-back path attenuation settings. In this method, both measurements yield I/Q mismatch and I/Q time skew parameters. However, transmitter and receiver nonlinearity characteristics are obtained through solving intermediate parameters extracted by NLS. Changing the loop-back path attenuation creates different conditions and increases the number of equations to extract the nonlinearity behavior of the transmitter and the receiver paths separately.

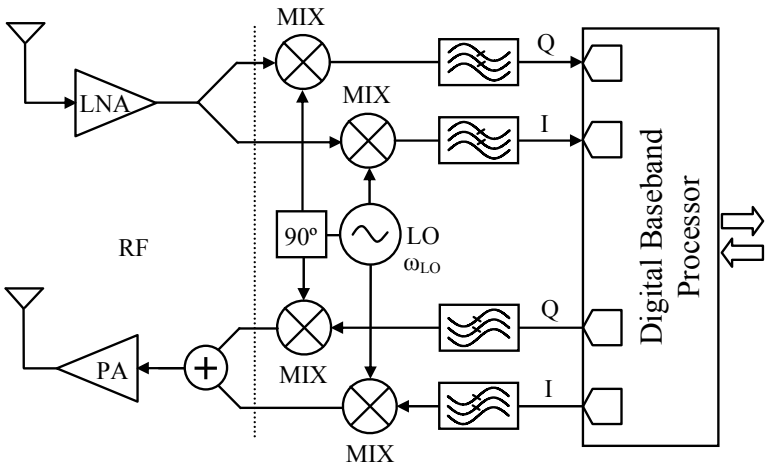


FIGURE 5.1: I/Q modulating RF transceiver

5.1 I/Q Modulating RF Transceiver

As circuit integration demands increase, direct conversion transceivers become more popular over the multiple-IF transceivers that require multiple filtering stages in their receiver paths. However, the down conversion technique on single-channel with nonzero IF comes with the image rejection problem which is often solved with an image rejection filter placed in the RF stages of the receiver. This RF filter is usually constructed with passive components that are undesirable for circuit integration. Therefore, system designers adopt the I/Q modulation/demodulation technique which has ideally infinite image rejection to eliminate the RF image rejection filter.

In I/Q modulation/demodulation technique, regardless of the digital baseband modulation, signals are modulated through I and Q channels having orthogonal carriers. The orthogonality of the carriers of both the transmitter and the receiver ensures proper demodulation of the I/Q signals at the receiver. As the orthogonality is degraded, infinite image rejection is no longer possible and the demodulated I/Q signals become mixtures of originally transmitted I/Q signals.

Usually, a low-cost I/Q modulating transceiver with a block diagram depicted in Figure 5.1, employs single LO for generating the orthogonal carrier signals. In the

normal operation mode, either the transmitter or the receiver is active. Therefore, one LO is sufficient for the system.

Most of the today's communication systems utilize digital baseband modulation schemes. Analog RF front-end (transmitter and receiver) is interfaced with data converters as shown in Figure 5.1. Transmitted signals are constructed digitally and transferred to analog domain whereas, received signals are digitized and processed in the digital domain. Therefore, digital signal processing at the baseband is very essential for the main functionality for the transceiver system.

The RF transceiver can be integrated with a DSP on the same chip for baseband signal processing or it can be followed by a separate DSP chip. In this chapter, we focus on single LO transceiver systems having on-chip data converters and a DSP as shown in Figure 5.1.

5.1.1 Transceiver Impairments

Ideal I/Q modulating transceiver has all the desired properties such as high image rejection and low BER. However, the RF front-end is an analog circuitry, which is prone to parametric deviations due to process variability. Therefore, the transceiver should be characterized in terms of impairment parameters such as I/Q gain/phase mismatch, I/Q time skew and transmitter/receiver nonlinearity.

The proper operation of the transceiver depends on the orthogonality of the carriers both on the transmitter and on the receiver side. Orthogonality of the I/Q arms degraded by phase mismatch between I/Q channels. The main contributor of the phase mismatch is the phase shift error of the 90° phase shifter block of the LO. Moreover, the time skew between I/Q channels on the RF side of the frequency conversion mixers (RF time skew) degrades the alignment of the I/Q signals which also results in as I/Q phase mismatch. The time skew between I/Q channels on the IF or baseband side of the frequency conversion mixers (baseband time skew) results

in a shift in the received symbol time intervals causing an error in received symbol calculation.

Gain mismatch between I/Q channels is an another impairment causing unbalanced received signal amplitudes and reducing receiver sensitivity. Systems with nonlinear characteristics suffer more because the I/Q gain mismatch effects are amplified by nonlinearity behavior of the signal path.

The transceiver nonlinearity, which is an inherent drawback of all analog circuits, is mainly due to the system amplifiers and frequency conversion mixers. The composite RF signal transmitted through the TX antenna contains both linearly and nonlinearly up-converted/amplified signal terms. On the receiver side, the signal captured by the RX antenna is amplified/down-converted while adding more nonlinear terms due nonlinear gains of the analog circuit blocks on the receive path. Therefore, the received signal contains nonlinear terms due to both transmitter and the receiver paths. In fact, most of the nonlinear terms are due to composite effects of transmitter and receiver nonlinearities since the circuits operate in a cascaded configuration.

DC offset at the receiver outputs is a common problem of direct frequency conversion architectures and it is caused by insufficient isolation between LO and RF ports of the down-conversion mixers at the receiver side.

5.1.2 Modeling Transceiver Impairments

In order to characterize the transceiver in terms of the impairment parameters, we need to develop mathematical models for the impairment effects. The impairments are inserted as gray shaded blocks to the block diagram of the transceiver as shown in Figure 5.2. In the following paragraphs we will explain the effects of these blocks mathematically.

Error of the phase shifter block (I/Q phase mismatch) can be modeled as an

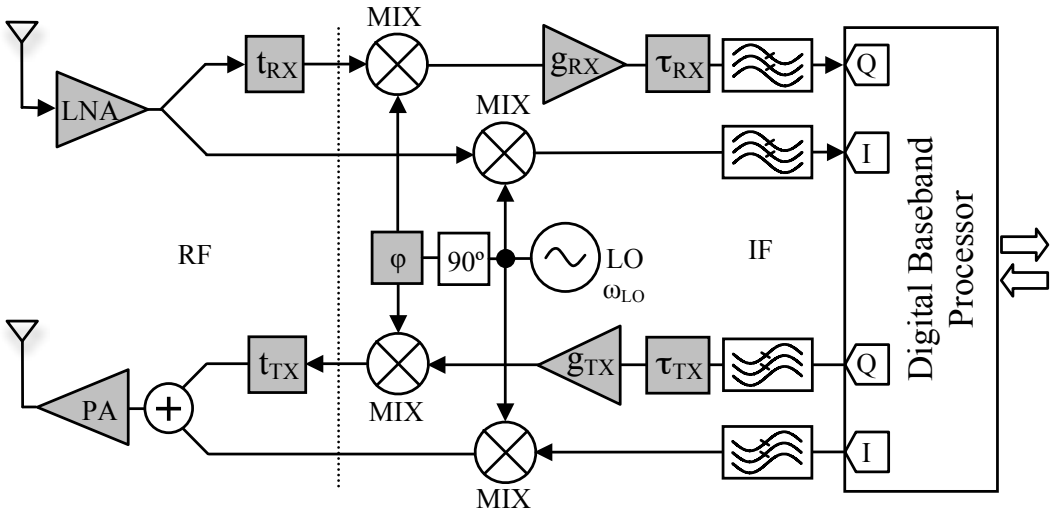


FIGURE 5.2: Transceiver with impairments

additional phase to the quadrature carrier signal of the LO. Therefore, LO signals are initially modeled as $\cos(\omega_C t)$ and $-\sin(\omega_{LO} t + \varphi)$ for the transceiver. However, time delays at the RF part of the mixers (RF time skew) alter the error of the phase shifter block differently for the transmitter and the receiver sides. In order to incorporate time delays (t_{TX}, t_{RX} in Figure 5.2), we model the phase shift error as two different variables for the transmitter and the receiver. Therefore, the LO signals for the transmitter and the receiver will be:

$$\begin{aligned} LO_{TXI} &= \cos(\omega_{LO} t) \\ LO_{TXQ} &= -\sin(\omega_{LO} t + \varphi_{TX}) \\ LO_{RXI} &= \cos(\omega_{LO} t) \\ LO_{RXQ} &= -\sin(\omega_{LO} t + \varphi_{RX}). \end{aligned} \tag{5.1}$$

I/Q gain mismatch is modeled on the Q channels of the transmitter and the receiver as additional gain blocks with respect to I channels. These gain blocks will amplify the Q channel signals by $1+g$, where g is the gain mismatch. Two parameters are defined for the I/Q gain mismatch since transmitter and receiver have separate

gain mismatches (g_{TX} and g_{RX} respectively).

Baseband time skew, which is the time delay mismatch at the baseband side of the mixers between I/Q channels, is modeled as the time shifts of Q channel signals with respect to I channel signals ($Q_{TX}(t-\tau_{TX})$ or $Q_{RX}(t-\tau_{RX})$). The time shift is a positive quantity. However, since we are taking I channel as a reference, the time shift can be negative for faster Q channels.

Nonlinearity of the transmitter and the receiver paths are modeled as third order polynomial gain functions covering the whole path from input to the output as expressed respectively in the following equations:

$$\begin{aligned} Gain_{TX}(x) &= \alpha_1 \cdot x + \alpha_2 \cdot x^2 + \alpha_3 \cdot x^3 \\ Gain_{RX}(x) &= \beta_1 \cdot x + \beta_2 \cdot x^2 + \beta_3 \cdot x^3. \end{aligned} \tag{5.2}$$

It is possible to define third order gain functions for each analog circuit block on the transmitter or the receiver path. However, this approach results in too many distinct nonlinear gain function coefficients to be extracted and the analytical analysis of the system model becomes almost impossible due to vast amount of parameters and nonlinear signal terms. Instead, we target at measuring nonlinearity of the transmitter part or the receiver part rather than individual components.

Baseband channel filters on the receiver side have not been included in the transceiver model derivation. The filter delays are assumed as transport delays, although a typical filter delay is frequency dependent. Using narrow bandwidth test signals minimizes the signal slope changing effect of the channel filter which is due to the frequency dependency of filter delays.

5.2 Loop-back Test Configuration and Test Challenges

In order to eliminate RF signal handling and enable the use of on-chip resources while testing the transceiver, we need a test configuration that takes low frequency

test inputs and generates low frequency test outputs. The solution to the problem have been proposed earlier as the loop-back test.

The loop-back test configuration of the transceiver circuit is obtained by connecting the output of the transmitter to the input of the receiver so that only baseband signals are used in the overall test. The test input is composed of digitally constructed I/Q signals. The baseband DSP can be used to generate the test inputs for the transmitter and analyze low frequency test response of the receiver. Conversion of test signals between analog and digital domain is achieved by on-chip data converters.

5.2.1 Physical Loop-back Path

The loop-back path is a physical signal path placed on the test board to connect the transmitter output to the receiver input. An attenuator may be needed to reduce the high power transmitter output to within the dynamic range of the receiver [46].

In our BiST approach, we assume a zero-IF receiver. Simple signal trace on the load board is sufficient for the loop-back path because down converted signal falls into the channel filter pass-band. Our technique is also applicable for low-IF receivers with a low-pass channel filter. A characterized offset mixer [12] may be necessary for wide-IF receivers (which require bandpass channel filter) to shift the down-converted signal frequency back to the pass-band of the channel filter. Since neither the RF attenuator nor the offset mixer alter the transceiver characteristics, our technique is applicable in both scenarios.

5.2.2 Test Challenges

The biggest challenge in the loop-back test is the decoupling the transmitter parameters from the receiver parameters in addition to decoupling distinct parameters from one another. Since we do not have access to RF signals, the only observed test

signal is the signal at the receiver output. The received signal is affected by both the transmitter and the receiver parameters. As such, we observe the composite impact of all impairments of both transmitter and receiver signal paths on the output signal. We introduce a detailed signal flow model for the transceiver and use various signal processing techniques to decouple transmitter and receiver impairment parameters.

Another challenge in loop-back testing is the inherent time delay associated with the physical loop-back path. This time delay degrades the alignment of the transmitted signal with respect to the down-conversion LO signal. In the normal operation mode of the transceiver circuit, this time delay is not a problem because transmitting and receiving parties are different circuits having separate carrier signals. Initially unsynchronized carriers are synchronized in terms of phase by carrier recovery or clock data recovery mechanisms. However, in the loop-back mode these mechanisms are inoperable because the transmitter and the receiver are operated by the same synthesizer. Therefore, we included the effect of time delay in the derived transceiver model.

In the following sections, (Sections 5.3 and 5.4) we will present two BiST methods based on loop-back configuration to characterize I/Q modulating transceiver circuits in terms of impairment parameters. Both methods propose features to overcome loop-back test challenges while reducing overall test costs.

5.3 Loop-back BiST Method for QPSK Baseband Modulation

In the first loop-back based BiST method presented in this section, we assume QPSK modulation scheme for the baseband modulation of the transceiver. In the QPSK modulation scheme, the binary data is modulated into four symbols placed on the unity circle with equal distances. The QPSK symbols and corresponding modulated RF waveforms for I/Q channels can be seen in Figure 5.3. During the symbol period, the amplitudes of the pulses at the baseband inputs of I/Q channels stay

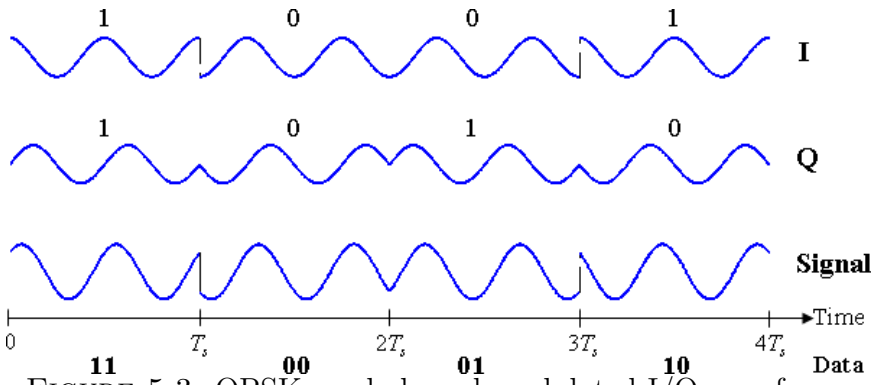


FIGURE 5.3: QPSK symbols and modulated I/Q waveforms

constant. The transmitter modulates, the pulses with the orthogonal carriers before transmitting the signals through the TX antenna. The RF signal reaches to the RX antenna with the loop-back connection and it is demodulated at the receiver with the same orthogonal carriers to obtain baseband I/Q signals. The QPSK symbols are recovered through integration of baseband I/Q signals of the receiver over the symbol period. Any impairment of the transceiver and any non-ideal condition, such as ambient noise affect calculated symbol values.

In the proposed BiST method we use the mapping between transmitted and received symbols to estimate I/Q mismatch and I/Q time skew parameters of the transceiver. The mapping between transmitted and received symbols includes the effects of all impairment parameters and it is derived by using the mathematical definitions of the transceiver impairments given in Section 5.1.2.

The proposed test method is composed of two steps as illustrated in Figure 5.4. In the first step, a set of intermediate parameters are estimated by using LS estimation [54, 55]. DC offsets for the receiver I/Q channels are also estimated at this point. In the second step, the intermediate parameters are mapped to I/Q mismatch and time skew parameters of the transmitter and the receiver by using a nonlinear solver based on least-squares-minimization [57, 58].

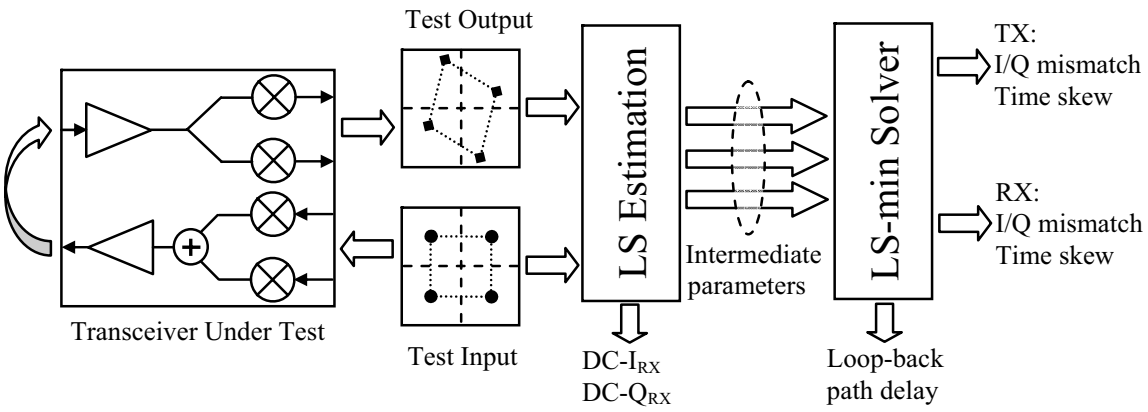


FIGURE 5.4: First BiST method analyzing QPSK Signals

5.3.1 Mathematical Transceiver Model

System model of the transceiver can be derived by starting from the transmitter baseband signals, which are QPSK modulated waveforms. If transmitter I/Q signals are $I(t)$ and $Q(t)$, and the I arm is taken as reference, signals at the inputs of the up-conversion mixers will be:

$$\begin{aligned} I'(t) &= I(t) \\ Q'(t) &= (1 + g_{TX}) \cdot Q(t - \tau_{TX}) \end{aligned} \tag{5.3}$$

where g_{TX} is the gain mismatch and τ_{TX} is the time skew of the transmitter. Using the LO signals given in Equation 5.1 for up-conversion and including the time skew and gain mismatch of the transmitter in the calculation, the transmitted signal can be expressed as:

$$\begin{aligned} r_{RF}(t) &= I'(t) \cdot \cos(\omega_{LO}t) - Q'(t) \cdot \sin(\omega_{LO}t + \varphi_{TX}) \\ &= I(t) \cdot \cos(\omega_{LO}t) - (1 + g_{TX}) \cdot Q(t - \tau_{TX}) \cdot \sin(\omega_{LO}t + \varphi_{TX}). \end{aligned} \tag{5.4}$$

This signal will be delayed by the loop-back path before it reaches the receiver as follows:

$$
\begin{aligned}
r_{RF}(t-t_D) &= I(t-t_D)\cdot\cos(\omega_{LO}(t-t_D)) - \\
&\qquad (1+g_{TX})\cdot Q(t-\tau_{TX}-t_D)\cdot\sin(\omega_{LO}(t-t_D)+\varphi_{TX}) \\
&= r_{RF-RX}(t). \qquad (5.5)
\end{aligned}
$$

Continuing in the receiver down-conversion path, we can express the received I/Q signals as:

$$
\begin{aligned}
I_{RX}(t) &= r_{RF-RX}(t)\cdot\cos(\omega_{LO}t) \\
Q_{RX}(t) &= -(1+g_{RX})\cdot r_{RF-RX}(t)\cdot\sin(\omega_{LO}t+\varphi_{RX}). \qquad (5.6)
\end{aligned}
$$

Channel filtering eliminates the high frequency components of the down converted I/Q signals due to the frequency mixing operation. Finally, substituting $r_{RF-RX}(t)$ into the above equation and delaying the Q signal yield the I/Q signals at the receiver output (after filtering) as:

$$
\begin{aligned}
I_{RX}(t) &= 0.5\cdot[I(t-t_D)\cdot\cos(\omega_{LO}t_D) - \\
&\qquad (1+g_{TX})\cdot Q(t-\tau_{TX}-t_D)\cdot\sin(\varphi_{TX}-\omega_{LO}t_D)] \\
Q_{RX}(t) &= -0.5\cdot(1+g_{RX})\cdot[I(t-\tau_{RX}-t_D)\cdot\sin(\varphi_{RX}+\omega_{LO}t_D) - \\
&\qquad (1+g_{TX})\cdot Q(t-\tau_{TX}-\tau_{RX}-t_D)\cdot\cos(\varphi_{TX}-\varphi_{RX}-\omega_{LO}t_D)]. \qquad (5.7)
\end{aligned}
$$

Equation 5.7 indicates that, the introduced time delay parameters shift the transmitted signals as well as rotate the signal constellation diagram. Time delays of the transmitted I/Q signals degrade the alignment of the integration intervals to the symbol intervals. Therefore, the symbol value obtained by integrating during the symbol duration will depend on the current and the previously received symbol. Due to the QPSK digital baseband modulation, four possibilities of the previously received symbol will result in four constellation points instead of each original constellation point. This phenomenon is illustrated in Figure 5.5, where diamond shape

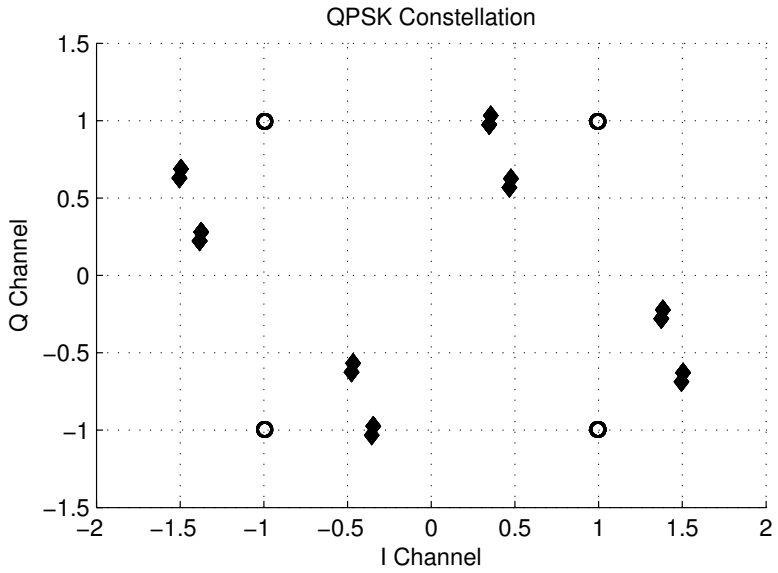


FIGURE 5.5: Effects of the loop-back time delay and the time skews on the symbol constellation diagram

points are the received signal constellation points and circle shaped points are the ideal locations.

Note that, the alignment of the integration intervals to the symbol intervals is not necessary because an additional integration interval time shift will appear in the loop-back time delay, which is not an impairment parameter of the transceiver. Since the overall amounts of time shifts of the received I/Q signals also included loop-back path delay, additional integration interval time shift will not affect the calculation of the transmitter and receiver time skew parameters. Therefore, the starting instant for integration can be random.

Assuming a rectangular pulse shape for each bit in the QPSK symbol enables the extraction of time delay parameters in terms of pulse duration since during symbol integration periods sampled pulse value stays constant as shown in Figure 5.6. If the pulses are not rectangular, time delay parameters can still be extracted. However, proper pulse profiling is required for translating the integrated pulse to time durations.

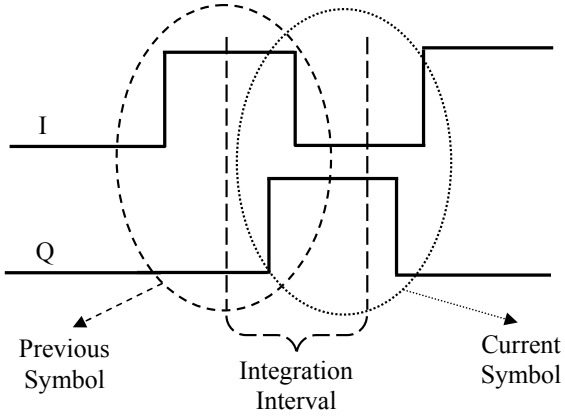


FIGURE 5.6: Integration of symbols

After sampling the received I/Q signals and integrating samples to obtain QPSK symbols, the system equation can be written in terms of received symbol values in matrix form as:

$$\begin{bmatrix} I_{RXn} \\ Q_{RXn} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} I_n \\ Q_n \end{bmatrix} + \begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} I_{n-1} - I_n \\ Q_{n-1} - Q_n \end{bmatrix} + \begin{bmatrix} DC_I \\ DC_Q \end{bmatrix} + \begin{bmatrix} w_I \\ w_Q \end{bmatrix} \tag{5.8}$$

where I_n and Q_n are the transmitted symbols for I/Q channels and n is the symbol index. Matrix entries A through D and a through d are the intermediate parameters and they can be written as functions of impairment parameters:

$$\begin{aligned} A &= 0.5 \cdot \cos(\omega_{LO} t_D) \\ B &= -0.5 \cdot (1 + g_{TX}) \cdot \sin(\varphi_{TX} - \omega_{LO} t_D) \\ C &= -0.5 \cdot (1 + g_{RX}) \cdot \sin(\varphi_{RX} + \omega_{LO} t_D) \\ D &= 0.5 \cdot (1 + g_{RX}) \cdot (1 + g_{TX}) \cdot \cos(\varphi_{TX} - \varphi_{RX} - \omega_{LO} t_D) \\ a &= A \cdot t_D / T_B \\ b &= B \cdot (t_D + \tau_{TX}) / T_B \\ c &= C \cdot (t_D + \tau_{RX}) / T_B \\ d &= D \cdot (t_D + \tau_{TX} + \tau_{RX}) / T_B \end{aligned} \tag{5.9}$$

where T_B is the pulse duration. DC levels at the I/Q channels of the receiver and

ambient noise are defined as two separate 2×1 vectors added to the end of Equation 5.8.

5.3.2 Parameter Extraction

Once the system response is collected with the test inputs, impairment parameters of the transceiver can be calculated with a two-step process. In the first step, the LS estimation method [54,55] is used to estimate the intermediate parameters, which are the matrix entries in Equation 5.8. In the second step, using the derived relations in Equation 5.9, system parameters are extracted with a LS-minimization based nonlinear solver.

LS Estimation

In a linear signal observation model (for N samples) of the form:

$$y(n) = x(n)\theta + \epsilon(n) \quad n = 1, .., N \tag{5.10}$$

where $\epsilon(n)$ is a zero-mean disturbance, which can be the Gaussian noise, it is possible to estimate the unknown parameter θ using statistical signal processing [54, 55]:

$$E[\theta] = (\mathbf{x}^T\mathbf{x})^{-1}\mathbf{x}^T\mathbf{y}. \tag{5.11}$$

In order to use this formula in our system, we need to arrange our system model as in Equation 5.10. System model in Equation 5.8 can be arranged in the symbol form containing I/Q channel symbols as vectors:

$$\mathbf{s}_{RX}(n) = \mathbf{M}_1\mathbf{s}_{TX}(n) + \mathbf{M}_2[\mathbf{s}_{TX}(n-1) - \mathbf{s}_{TX}(n)] + \mathbf{dc} + \mathbf{w}(n) \tag{5.12}$$

where $\mathbf{s}$ stands for symbols and $\mathbf{M}_1, \mathbf{M}_2$ are matrices with entries A through D and a through d respectively. If we take transpose of both sides of Equation 5.12 and

define $\mathbf{y}(n), \mathbf{x}(n)$ and θ as:

$$\begin{aligned}\mathbf{y}(n) &= \mathbf{s}_{RX}(n)^T \\ \mathbf{x}(n) &= [\mathbf{s}_{TX}(n)^T \ [\mathbf{s}_{TX}(n-1) - \mathbf{s}_{TX}(n)]^T \ 1] \\ \theta &= \begin{bmatrix}\mathbf{M}_1^T \\ \mathbf{M}_2^T \\ \mathbf{dc}^T\end{bmatrix}\end{aligned} \tag{5.13}$$

we obtain the linear observation model for our system.

$$\mathbf{Y} = \mathbf{X}\theta + \mathbf{W}^T \tag{5.14}$$

Using the formula given in Equation 5.11, intermediate parameters as well as the receiver I/Q channel DC offsets can be estimated using only the digital test inputs and the received I/Q baseband signals.

Solving for System Parameters

Once the intermediate parameters are obtained, the system performance parameters can be solved using the derived relations in Equation 5.9. We have defined 6 performance parameters for the system: transmitter/receiver I/Q mismatches (gain and phase) and I/Q time skews. An additional parameter appearing in equations as an unknown is the loop-back path delay resulting in a total number of 7 unknowns. To solve for all unknowns, we obtain 8 equations from the LS-estimation step and use an LS minimization based nonlinear solver. The solver takes lower and upper bounds for the performance parameters and tries to minimize the error defined by the sum of squares of function values obtained from the equation set [57, 58].

5.3.3 Simulation Results

We conduct experiments on our test method in MATLAB to determine its accuracy and robustness in the presence of additive Gaussian noise and LO leakage. In our simulations, we utilize LS-minimization nonlinear solver of MATLAB.

Simulation Test Setup

The transceiver model shown in Figure 5.2 is implemented in MATLAB with the defined impairment parameters. Since we did not model the path nonlinearity for the transmitter and the receiver in this BiST method, we did not implement nonlinearity characteristics for the PA and the LNA shown in Figure 5.2.

Digital baseband test input is generated as a randomized bit sequence with a pulse duration of $1\mu sec$. The carrier frequency is chosen as $900MHz$. Receiver I/Q channels are sampled and digitized with a 10 to $12-bit$ ADC operating at $100MHz$. With this configuration, each pulse is represented by 100 time samples. Received symbol values are calculated by integrating the collected signal samples.

To mimic the real operational condition, we introduce LO leakage. LO leakage is obtained by adding a proportion of LO signal to the corresponding RF port of the receiver mixers. Although it is unlikely to have huge variations on the receiver I/Q channels' DC offsets, our model can discriminate DC offsets of the receiver I/Q channels.

Test Accuracy

The accuracy of the test method is evaluated by observing the RMS estimation errors of the system parameters under various ADC resolutions and lengths of test vectors.

The applied test input vector is converted to analog polar waveform of values $1, -1$, which is translated as $13dBm$ signal power. $10-bit$ and $12-bit$ ADCs allow $60.2dB$ and $72.2dB$ maximum SNR respectively. This configuration yields around $-47dBm$ $-60dBm$ noise power for the system. Therefore, we vary power of the noise signal form $-50dBm$ to $-60dBm$ to simulate ADC quantization noise for 10 to $12-bit$ ADCs. Evaluated test vector lengths are $200-bit$, $500-bit$ and $1000-bit$. RMS errors are calculated from 100 simulations for various noise power and test vector length configurations. RMS estimation error results for the

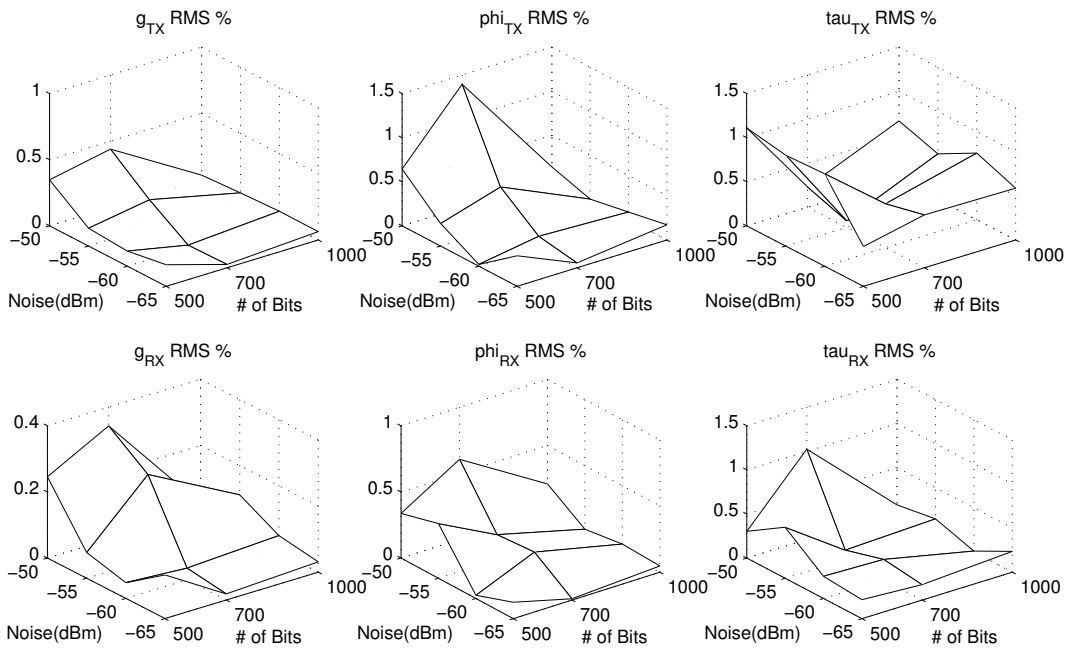


FIGURE 5.7: RMS estimation errors for transceiver impairments

transceiver parameters are plotted in Figure 5.7. These results indicate that, errors generally decrease as the test vector length increases. The data points violating this general trend are due to the errors of the nonlinear solver which sometimes converges to a high error root. In the overall, all estimation errors are below $1.5\%RMS$ even for the shortest test vector length with $10-bit$ system ADC. Results of a sample simulation with $500-bit$ test vector and $12-bit$ ADC ($-60dBm$ noise) are listed in Table 5.1.

ADC sampling frequency is the lower limit for the estimation resolution of the I/Q time skew parameters, τ_{TX} and τ_{RX} since sampling interval is the minimum measurable time delay.

Computational Complexity and Test Time

Computational complexity of the test method is evaluated in terms of floating-point-operations (FLOP). These FLOPs are due to the LS estimation and LS-minimization

Table 5.1: Results for a sample simulation of the loop-back BiST method

Parameter	Injected	Measured	units
τ_{TX}	20	19.876	nsec
τ_{RX}	40	40.916	nsec
g_{TX}	0.2	0.205	-
g_{RX}	-0.25	-0.254	-
φ_{TX}	7	6.898	deg
φ_{RX}	6	6.041	deg
DC_I	0.2	0.2001	volt
DC_Q	0.3	0.3001	volt

based solver. The LS estimation algorithm FLOP count depends on the test vector length. Based on the matrix operations of the LS estimation algorithm, we determine the computational overhead as $115 * N$, where N is the test vector length. The complexity of the LS nonlinear solver does not depend on test vector length since in all cases, we have 8 equations and 7 unknowns. The nonlinear solver converges in 8 iterations on the average, which translates to around 500 FLOPs. The total computational need for our technique therefore is $500 + 115 * N$.

The test time depends on the total FLOP count of the test method, which includes the FLOPs due to parameter extraction and basic signal processing with data collection. The FLOP count and components of test time according to different length test input vectors is listed in Table 5.2 assuming $1\mu sec$ pulse durations and an 80 million-instructions-per-second (MIPS) DSP [59].

Table 5.2: Test overheads (80 MIPS DSP)

Bits	FLOP	Data Coll.	Data Proc.	Test Time
500	58k	$500\mu s$	$725\mu s$	$1.23ms$
700	81k	$700\mu s$	$1.01ms$	$1.71ms$
1000	115.5k	$1.0ms$	$1.44ms$	$2.44ms$

5.4 Loop-back BiST Method for All Baseband Modulations

In this second loopback based BiST method, we improved the previous BiST method presented in Section 5.3 by extending the impairment list to include nonlinearity characteristics of the transmitter and the receiver. We also relax the first BiST method in terms of the baseband modulation requirement of the transceiver so that the new test signals can belong to any kind of baseband modulation scheme.

5.4.1 Test Method

The test method illustrated in Figure 5.8 performs two consecutive measurements. Both measurements yield DC offsets, I/Q mismatch and I/Q time skew parameters as well as the composite nonlinearity parameters of the transceiver. Parameters are extracted by NLS method which constructs a system of equations describing the input/output mapping of the transceiver.

The nonlinearity characteristics of the transmitter and the receiver paths are extracted by solving for gain function coefficients of each path using the equations built with composite parameters extracted by NLS. An attenuator is used as the loop-back path to decrease the power of signals at the transmitter output. The

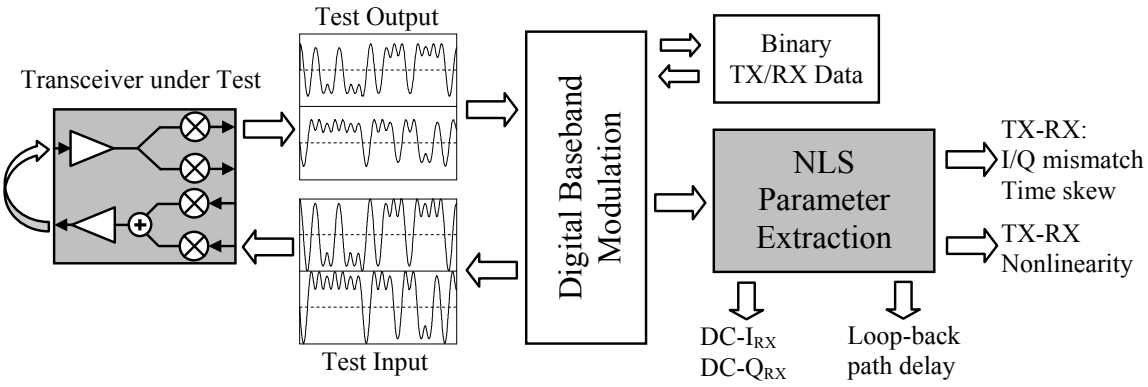


FIGURE 5.8: Second BiST method for I/Q mismatch, I/Q time skew and Nonlinearity

attenuation amount is determined to operate the receiver in its linear region. Two different attenuation settings will provide sufficient number of equations to extract nonlinearity behaviors of the transmitter and the receiver paths.

5.4.2 Test Signals

Test inputs are digitally modulated low frequency baseband signals. The signal processing technique used in our method accepts almost any kind of digitally modulated signals as well as plain signals such as two-tone waveforms. We have used GMSK digital modulation technique to generate test input signals in our test to be compatible with GSM transceiver standards.

GMSK signals are generated from a random bit pattern in MATLAB obeying the principles of the GMSK modulation. In the experiments, the I/Q signals are formatted to be accepted by the pattern generator and the RF tester programming interfaces. The modulated I/Q signals can be seen in Figure 5.9 with the random input data.

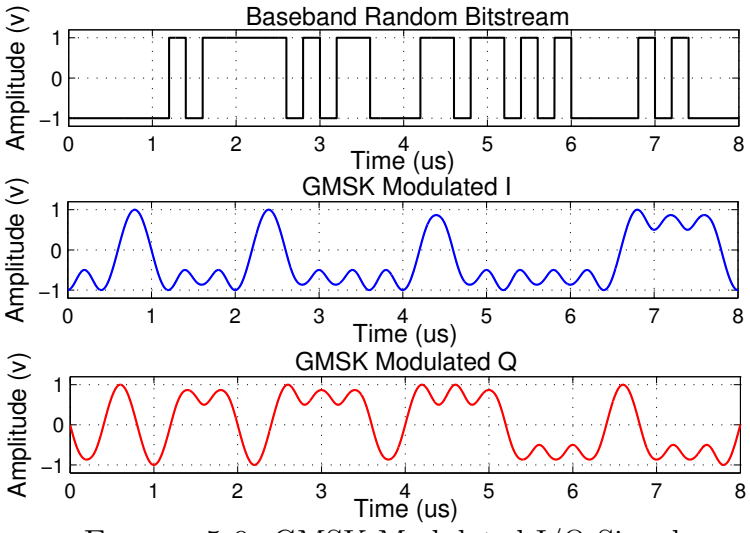


FIGURE 5.9: GMSK Modulated I/Q Signals

5.4.3 Mathematical Transceiver Model

In the previous BiST method presented in Section 5.3, we did not include the nonlinearity parameters of the transmitter and the receiver in the derived transceiver model since the BiST method extracts only I/Q phase mismatch and I/Q time skew parameters as well as the DC offsets. In this BiST method, we improve the mathematical transceiver model derived in Section 5.3.1 by including nonlinearity characteristics of the transmitter and the receiver paths.

The inherent nonlinearity behavior of the analog circuit blocks of the transceiver eventually generates nonlinear signal terms at the received I/Q signals. However, using small signal amplitudes at the input suppresses the nonlinearity behavior and the transceiver can be modeled as a linear system. Relying on this approach, first we will modify the transceiver model derived in Section 5.3.1 to include linear path gains and the loop-back path attenuation. Later, we will include nonlinearity characteristics of the transmitter and the receiver using third order gain functions given in Equation 5.2 to develop analytical nonlinear model.

Linear Model

We modify the transceiver model given in Equation 5.7 to add transmitter and receiver linear path gains as well as the loopback path attenuation. The new linear model is expressed as:

$$\begin{aligned} I_{RX}(t) = \frac{0.5}{k} \cdot G_{TX} \cdot G_{RX} \cdot [I(t-t_D) \cdot \cos(\omega_{LO} t_D) - \\ (1+g_{TX}) \cdot Q(t-\tau_{TX}-t_D) \cdot \sin(\varphi_{TX} - \omega_{LO} t_D)] \\ Q_{RX}(t) = -\frac{0.5}{k} \cdot G_{TX} \cdot G_{RX} \cdot (1+g_{RX}) \cdot [I(t-\tau_{RX}-t_D) \cdot \sin(\varphi_{RX} + \omega_{LO} t_D) - \\ (1+g_{TX}) \cdot Q(t-\tau_{TX}-\tau_{RX}-t_D) \cdot \cos(\varphi_{TX} - \varphi_{RX} - \omega_{LO} t_D)]. \end{aligned} \quad (5.15)$$

where G_{TX} and G_{RX} are transmitter and receiver path gains respectively. k is the attenuation introduced by the loop-back path.

Nonlinear Model Development

Equation 5.15 is the complete linear response of the transceiver including all impairment parameters except for the nonlinearities. Nonlinear response of the transceiver will include Equation 5.15 as the linear term in addition to nonlinear signal terms. To obtain the nonlinear model, gain functions defined in Equation 5.2 are assigned to the transmitter and the receiver and the steps followed to derive the linear model are repeated with the help of a symbolic solver. Since the nonlinearity of the whole transmitter or the receiver path can be approximated with the gain functions defined in Equation 5.2, we can use linear gain coefficients (α_1 and β_1) of the transmitter and the receiver instead of G_{TX} and G_{RX} in Equation 5.15.

After simplifying and low-pass filtering, the nonlinear response of the transceiver can be obtained as:

$$\begin{aligned} I_{RX}(t) = 0.5 \cdot [&I(t - t_D) \cdot \cos(\omega_{LO} t_D) - \\ &(1 + g_{TX}) \cdot Q(t - \tau_{TX} - t_D) \cdot \sin(\varphi_{TX} - \omega_{LO} t_D)] \cdot \sum \kappa \\ Q_{RX}(t) = -0.5 \cdot (1 + g_{RX}) \cdot [&I(t - \tau_{RX} - t_D) \cdot \sin(\varphi_{RX} + \omega_{LO} t_D) - \\ &(1 + g_{TX}) \cdot Q(t - \tau_{TX} - \tau_{RX} - t_D) \cdot \\ &\cos(\varphi_{TX} - \varphi_{RX} - \omega_{LO} t_D)] \cdot \sum \kappa, \end{aligned} \tag{5.16}$$

where κ is the coefficient vector due to nonlinearity and it contains cascaded linear and nonlinear gain coefficients. κ is calculated with a symbolic solver by using the

gain coefficients as:

$$\kappa = [c_0 \quad c_1 p \quad c_2 p^2 \quad c_3 p^3 \quad c_4 p^4]$$

$$c_0 = \frac{\alpha_1 \beta_1}{k}$$

$$c_1 = \frac{3}{4}\frac{\alpha_3 \beta_1}{k} + \frac{3}{2}\frac{\alpha_1 \alpha_2 \beta_2}{k^2} + \frac{3}{4}\frac{\alpha_1^3 \beta_3}{k^3}$$

$$c_2 = \frac{5}{4}\frac{\alpha_2 \alpha_3 \beta_2}{k^2} + \frac{15}{8}\frac{\alpha_1 \alpha_2^2 \beta_3}{k^3} + \frac{15}{8}\frac{\alpha_1^2 \alpha_3 \beta_3}{k^3}$$

$$c_3 = \frac{105}{64}\frac{\alpha_2^2 \alpha_3 \beta_3}{k^3} + \frac{105}{64}\frac{\alpha_1 \alpha_3^2 \beta_3}{k^3}$$

$$c_4 = \frac{63}{128}\frac{\alpha_3^3 \beta_3}{k^3}$$

$$p = [I(t - t_D)]^2 + (1 + g_{TX})^2 \cdot [Q(t - \tau_{TX} - t_D)]^2 - 2I(t - t_D) \cdot Q(t - \tau_{TX} - t_D) \cdot (1 + g_{TX}) \cdot \sin(\varphi_{TX}), \tag{5.17}$$

where k is the gain of the attenuation block placed on the loop-back path between the transmitter output and the receiver input.

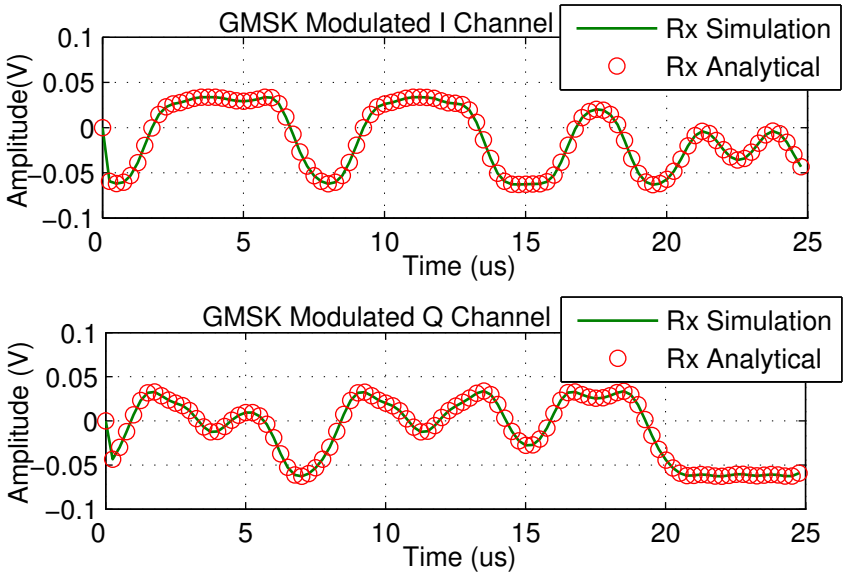


FIGURE 5.10: Transceiver response: simulation versus analytical

In Figure 5.10, the actual and analytically calculated I/Q responses of a nonlinear transceiver can be seen. To obtain these waveforms, a transceiver model is constructed in MATLAB including nonlinear frequency conversion mixers and nonlinear amplifiers, PA and LNA. Then, overall nonlinearity parameters for transmitter and receiver paths are determined through two-tone measurements and they are used in the analytical model Equations 5.16 and 5.17. Received signals plotted with solid line are obtained by passing the transmitter I/Q signals through the nonlinear transceiver model, whereas the received signals plotted with circles are obtained by the analytical derivation given in Equations 5.16 and 5.17. The difference between to responses are also given as an error plot in Figure 5.11. The maximum error is around $60\mu V$ which is very low compared to signal amplitude. This analysis confirms that each block in the receiver or transmitter path may contain nonlinear terms however, the overall nonlinearity can be modeled at the input (or output) node of the system without much loss in accuracy. As a result, the use of the simplified analytical model is warranted.

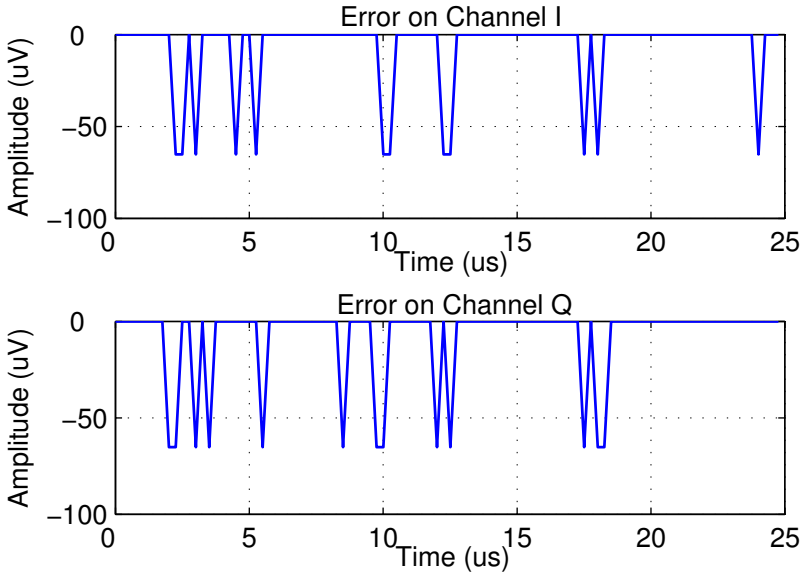


FIGURE 5.11: Difference between simulation and analytical signals

5.4.4 Symbol Calculation

In demodulators, receiver output signals are digitized by the on-chip data converters synchronized with the system clock. Depending to the digital modulation technique of the system either the signal samples or symbols calculated from samples may be needed. Most of the digital modulation techniques integrate signal samples over a time period to obtain symbol values.

In order to extract the time-shift information, we shorten the integration period as shown in Figure 5.12. Since our integration interval is different than that of the modulation scheme, we call the resulting values *quasi-symbols*. The integration to obtain quasi-symbols is done in the digital domain by software. In our test method, we store the integration results for the signal samples of both the receiver outputs and the transmitter inputs.

Extraction of Time Related Parameters with Quasi-Symbols

Baseband time skew is an impairment parameter for both the transmitter and the receiver and it degrades the time alignment between the I/Q channels. In order to extract the time skew parameters, we express the model given in Equations 5.16 and

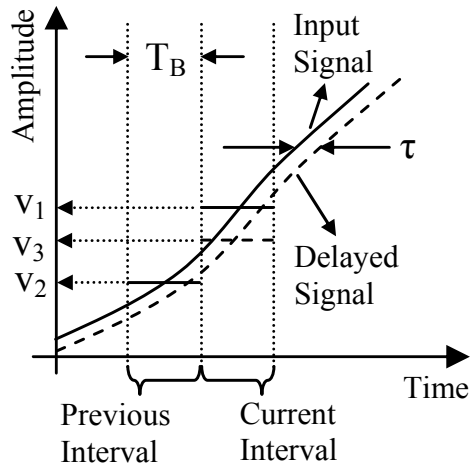


FIGURE 5.12: Integration of test symbols

5.17 in terms of transmitted and received quasi-symbols.

The transmitted quasi-symbols do not contain any impairments effects, whereas received quasi-symbols have the composite effects of transmitter and receiver impairments. In order to obtain the amount of time shift in the received signals, we need to relate the time shift to the received quasi-symbol values. We rely on the assumption that the analog signal at the receiver output is approximately linear (as shown in Figure 5.12) within the integration interval composed of couple of signal samples. This assumption is valid since the sampling frequency of the system is sufficiently higher than the signal bandwidth. Therefore, the received signal does not change rapidly between sampling intervals. The time shift can be calculated by solving the following equation:

$$v_3 \cdot T_B = v_1 \cdot T_B + (v_2 - v_1) \cdot \tau, \tag{5.18}$$

where v_1 through v_3 are average signal amplitudes. T_B is the integration interval length and τ is the time delay. If we call v_3 as the received quasi-symbol and v_1, v_2 as current and previous transmitted quasi-symbols, we can rewrite the equation in terms of quasi-symbols.

$$s_D(n) = s_I(n) + [s_I(n-1) - s_I(n)]\frac{\tau}{T_B}, \tag{5.19}$$

where s_D and s_I are quasi-symbols of delayed and input signals and n is the symbol index.

Integration Interval

The error introduced with this quasi symbol approach is a function of the integration interval. Hence, choosing the integration interval appropriately minimizes the error while increasing the accuracy of the proposed method. We will explain the relation between the integration interval and the measurement error on a basic observation

model composed of N samples with a nonlinear system function $f(x)$ given as:

$$y_n = f(x_n) + \omega_n, \quad n = 1, ..., N, \tag{5.20}$$

where x_n is the input, ω_n is a zero-mean Gaussian disturbance and y_n is the observed output of the system. We choose the integration interval as m samples and lets assume N is an integer multiple of m for simplicity. We calculate the input and the output quasi symbols as:

$$\acute{y}_k = \frac{1}{m} \cdot \sum_{n=(k-1)\cdot m+1}^{k\cdot m} y_n, \quad k = 1, ..., \frac{N}{m}$$

$$\acute{x}_k = \frac{1}{m} \cdot \sum_{n=(k-1)\cdot m+1}^{k\cdot m} x_n, \quad k = 1, ..., \frac{N}{m}. \tag{5.21}$$

The norm function of the form $F(\acute{x}_k) = 0$ can be obtained with the calculated quasi symbols in Equation 5.21 as:

$$F(\acute{x}_k) = \left(\sum_{k=1}^{\frac{N}{m}} \left(\acute{y}_k - f(\acute{x}_k)\right)^2 \right)^{\frac{1}{2}}. \tag{5.22}$$

As can be seen from Equation 5.22, the error is due to the nonlinear characteristics of the system function. It is also seen that, the error decreases as the integration interval gets shorter, since the quasi symbols calculated with shorter intervals may approximate signal samples much better. However, the integration interval has to be bigger than the time delay that is calculated with the quasi symbols.

We performed a simulation to evaluate the norm function obtained from the nonlinear transceiver model given in Equations 5.16 and 5.17 as in the basic observation model given in Equation (5.20). The 3-D plot given in Figure 5.13 shows the error with respect to the integration interval and the test vector length. We use the integration interval that gives the minimum error for the given test vector

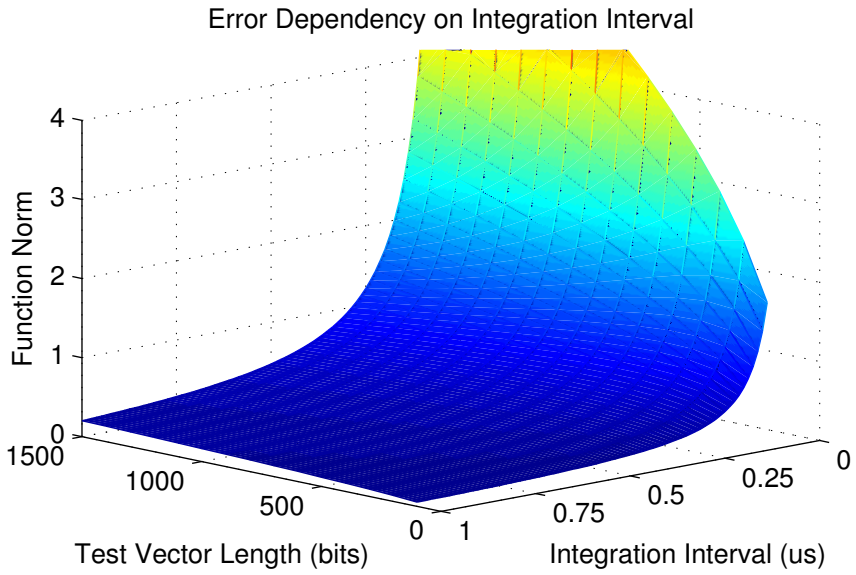


FIGURE 5.13: Error due to integration interval

length. System parameters, such as sampling frequency and bit duration affect the simulation. Therefore, the integration interval should be chosen according to the transceiver system.

5.4.5 Quasi-symbol Based System Equations

After sampling the received I/Q signals and integrating samples to obtain symbols, linear system equations of the transceiver can be written in terms of received quasi-symbol values in matrix form as:

$$\begin{bmatrix} I_{RXn} \\ Q_{RXn} \end{bmatrix} = \frac{\alpha_1\beta_1}{k}\left[\begin{bmatrix} A & B \\ C & D \end{bmatrix}\begin{bmatrix} I_n \\ Q_n \end{bmatrix} + \begin{bmatrix} a & b \\ c & d \end{bmatrix}\begin{bmatrix} I_{n-1} - I_n \\ Q_{n-1} - Q_n \end{bmatrix}\right] + \begin{bmatrix} DC_I \\ DC_Q \end{bmatrix} + \begin{bmatrix} w_I \\ w_Q \end{bmatrix} \quad (5.23)$$

where I_n and Q_n are the transmitted quasi-symbols for I and Q channels and n is the symbol index. Matrix entries A through D and a through d, which are the intermediate system parameters, are the same as in the previous BiST method. The intermediate system parameters are given in Equation 5.9.

Note that, $\frac{\alpha_1\beta_1}{k}$ in Equation 5.23, is the parameter c_0 in Equation 5.17, is nothing but the linear coefficient of the transceiver response. Therefore, the nonlinear

response of the transceiver is constructed easily by multiplying the linear part of Equation 5.23 with coefficients given in κ.

5.4.6 Parameter Extraction

Once the system response is collected in two consecutive measurements with different attenuator settings, the impairment and nonlinearity parameters of the transceiver can be calculated with a two-step process. In the first step, for both of the consecutive measurements the NLS estimation method [56–58] is used to extract the impairment parameters together with the composite nonlinearity parameters of c_0 through c_4 given in Equation 5.17. In the second step, the nonlinearity parameters of the transmitter and the receiver paths are extracted with a nonlinear solver using the system of equations constructed with composite parameters from NLS.

NLS Estimation

The input output behavior of the transceiver with N quasi-symbols is of the form:

$$y(n) = x(n)f(\theta) + \epsilon(n) \quad n = 1, .., N \tag{5.24}$$

$\epsilon(n)$ is a zero-mean disturbance (i.e. noise). Each data point pair (input/output) in the collected observation data are used to extract the parameter θ. Therefore, it is possible to construct a vector function of the form $F(\mathbf{x}) = 0$ from Equation 5.24 by using all N quasi-symbols.

$$\begin{aligned} F(x(1)) = 0 &= y(1) - x(1)f(\theta(1)) - \epsilon(1) \\ &\vdots \\ F(x(n)) = 0 &= y(n) - x(n)f(\theta(n)) - \epsilon(n) \end{aligned} \tag{5.25}$$

NLS takes this vector function $F(\mathbf{x})$ with predefined boundaries for the unknown parameter θ and finds a solution set within the boundaries with (usually Gauss-Newton) iterations based on normal equations constructed form the vector function.

In our system model, we have a data set for both I and Q channels resulting in $2N$ data points of inputs and outputs. The vector function is constructed with the received and the transmitted quasi-symbol vectors for both I and Q channels using Equations 5.16 and 5.17. Unknowns of the normal equation set are our transceiver impairment parameter list composed of transmitter and receiver I/Q gain/phase mismatch, I/Q time-skew and receiver DC offsets as well as the composite nonlinearity parameters of c_0 through c_4 given in Equation 5.17.

Nonlinear Solver and Boundaries

In the proposed test method, NLS operates on a system of equations constructed with $2N$ input/output quasi-symbols for both of the I and the Q channels. Since the collected data produce many quasi-symbol pairs, the number of equations will be always larger than the number of unknowns. The boundaries for each parameter are defined to limit the search space of the solver and are kept at several times the specification range. If the circuit is severely degraded, the algorithm converges to the boundaries. In our observations form simulations however, we encountered some convergence issues for some legitimate transceiver circuits having specifications within the solver boundaries. For those cases, the convergence issues are believed to be arise form LO signals phase-delay relation introduced by the loop-back time delay. In some cases the solver converged to the circuit specifications with different loop-back time delays. Therefore, having a controllable loop-back time delay may be beneficial for the solver to increase convergence chance.

5.4.7 Results and Discussion

We perform simulations on our test method in MATLAB to determine its accuracy and robustness in the presence of additive Gaussian noise and LO leakage with various ADC resolutions. In our simulations, we utilize LS-minimization nonlinear

solver of MATLAB. We also conduct two sets of experiments. The first set is on a transceiver circuit built with off-the-shelf components whereas, the second set is on a RF tester with programmable RF attenuator (LitePoint IQnxn and IQExpress). The digital test input/output data in both experiment sets is then processed with the same test routines as used in the simulations.

Simulation Results

The transceiver model shown in Figure 5.2 is implemented in MATLAB with the defined performance parameters. Digital baseband test inputs are generated as randomized GMSK signals compatible with the GSM standard. The random bit stream has a bit duration of $1.25\mu s$. The carrier frequency is chosen as $2.4GHz$. Receiver I and Q channels are sampled and digitized with $6-bit$ and $10-bit$ ADCs operating at $80MHz$. The transceiver model has a PA with a $15dB$ power gain. Therefore the attenuation values for the consecutive measurements are chosen as $25dB$ and $30dB$ in order to lower the signal power below the $1-dB$ ($-10dBm$) compression point of the receive path. Similarly transmitter input signal amplitudes are chosen according to the $1-dB$ compression point of the transmitter path ($0dBm$).

Received quasi-symbol are calculated by integrating time samples for $0.3\mu s$. Since there is no carrier phase synchronization as explained in Section 5.2.2, the starting instant of the integration interval can be random. Therefore, we start integrating received signal samples form the beginning of the sample vector. As in the previous BiST method simulations, we introduce LO leakage to mimic the real operational condition of the trasnceiver.

The accuracy of the test method is evaluated by observing the RMS extraction errors of the impairment and nonlinearity parameters calculated from 100 simulations under various lengths of test vectors and ADC resolutions. RMS error results for the transceiver I/Q mismatch, time skew and nonlinearity parameters are given

Table 5.3: RMS Errors over 100 Simulations

Parameter	Injected	Error: 6-bit ADC 200-bit length	Error: 6-bit ADC 500-bit length	Error: 10-bit ADC 200-bit length	Error: 10-bit ADC 500-bit length	Solver Bounds
φ_{Tx}	5.0°	0.118°	0.114°	0.116°	0.103°	± 15°
g_{Tx}	-0.25	0.003	0.003	0.002	0.002	± 0.5
φ_{Rx}	-4.3°	0.033°	0.026°	0.051°	0.027°	± 15°
g_{Rx}	0.1	0.008	0.008	0.003	0.003	± 0.5
τ_{TX}	38 ns	1.95 ns	1.70 ns	0.50 ns	0.45 ns	0 - 200 ns
τ_{RX}	51 ns	1.02 ns	1.73 ns	0.54 ns	0.53 ns	0 - 200 ns
DC_I	0.2 V	9.71 mV	9.71 mV	8.76 mV	8.76 mV	± 0.5 V
DC_Q	0.15 V	7.51 mV	7.51 mV	6.59 mV	6.59 mV	± 0.5 V
$TX - IIP_3$	10 dBm	1.486 dB	1.121 dB	1.073 dB	1.128 dB	$0 - 20$ dBm
$RX - IIP_3$	1 dBm	1.293 dB	1.410 dB	0.892 dB	0.905 dB	± 10 dBm

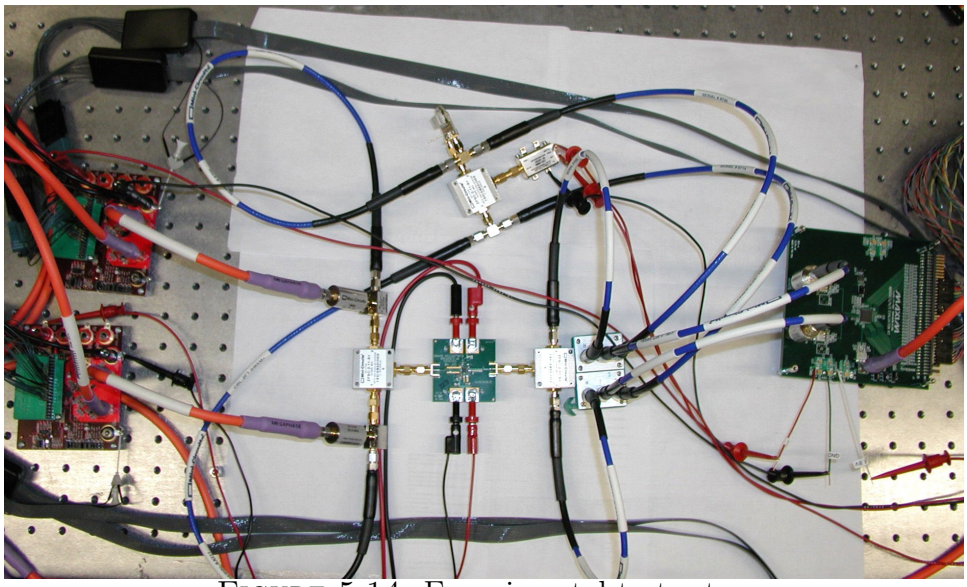


FIGURE 5.14: Experimental test setup

in Table 5.3. These results indicate that the RMS errors are well below the typical transceiver specifications for the extracted impairments and will not affect the transceiver performance. Nonlinearity parameters are extracted with $1.4dB$ RMS errors which are much less than $4.4dB$ reported in [7].

Experiment Results

In the first set of experiments, the transceiver model shown in Figure 5.1 is built with of-the-self components from MiniCircuits. Test signals are generated in MATLAB and loaded to a pattern generator that interfaces the transmitter with $12-bit$ DACs (MAXIM 5873). Test response is captured by $12-bit$ ADCs (TI ADS6125) and recorded with a logic analyzer. Instead of a complete synthesizer, a voltage controlled oscillator and a phase shifter are used so that the controllable phase shift amount is utilized to generate different circuit instances. Since the mixers used in the transceiver are passive, a PA is placed on the loop-back path to amplify transmitter output signals. The experimental test setup can be seen in Figure 5.14.

GMSK signals used in the measurements have $100MHz$ sampling rate and $1\mu s$ bit

duration. They are generated in MATLAB and formatted according to the pattern generator input file. The carrier frequency is adjusted as $900MHz$ because the VCO can operate between $800MHz$ and $1GHz$. Receiver output channels are sampled synchronized to the test inputs and stored for analysis. Synchronization is achieved through a master clock signal driving both ADCs, DACs, the pattern generator and the logic analyzer. For each channel, $12 - bit$ wide output is recorded for every sampling instance. Then, the recorded output data is written into a text file to be uploaded into MATLAB.

Results of our method are compared to traditional test methods which involve up/down frequency conversion to test the transmitter and the receiver separately. We used a third mixer on this purpose with sinusoidal signals as the traditional test signals. In Table 5.4, results of traditional and proposed methods are compared for I/Q gain and phase mismatches of two circuit instances. Both results are obtained through averaging 10 measurements.

The second set of experiments are performed on the RF tester, which is configured into loopback mode with the help of a RF attenuator seen in Figure 5.15. The tester contains a fully calibrated transceiver that is parameterizable through test software. The test programming interface also controls the 2-path RF attenuator by enabling

Table 5.4: Experimental results for traditional and proposed methods

Parameter	Traditional	Proposed	RMS Error	Unit
φ_{RX1}	3.21	3.03	0.25	deg
g_{RX1}	-0.21	-0.24	0.021	-
φ_{TX1}	-2.81	-2.79	0.07	deg
g_{TX1}	0.2	0.2	0.004	-
φ_{RX2}	6.72	6.77	0.13	deg
g_{RX2}	-0.25	-0.27	0.018	-
φ_{TX2}	1.69	1.67	0.05	deg
g_{TX2}	0.21	0.2	0.005	-

FIGURE 5.15: Experimental test setup, LitePoint RF Tester and RF Attenuator

the attenuator path and changing the attenuation. Thus, both equipments establish an excellent experimental setup to evaluate the accuracy of our technique. Test signals generated in MATLAB are uploaded to the RF tester and the test response is transferred to MATLAB for analysis. A sample of transmitted and captured signals for the I/Q channels can be seen in Figure 5.16.

To inject impairment parameters, the transceiver of the RF tester is modified through its control interface. The first path of the RF attenuator is adjusted to $15dB$ and $20dB$ attenuations for the consecutive measurements. The transmitter

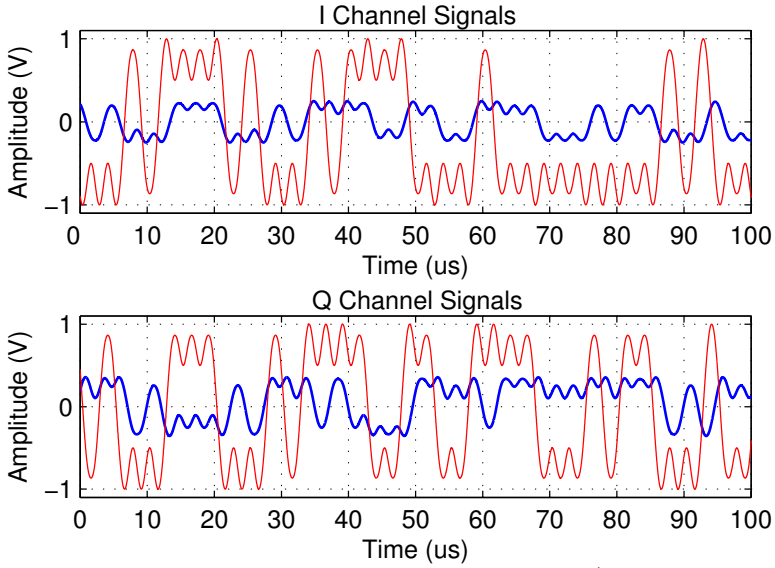


FIGURE 5.16: Experimental test signals (on RF tester)

output power is programmed at $5dBm$ such that the input to the receiver is kept under $1-dB$ compression point with the chosen attenuation values. The carrier and the sampling frequencies are the same as in the simulations. The captured signals are analyzed by the MATLAB routine and RMS errors are calculated over multiple measurements. Table 5.5 summarizes the RMS errors according to the impairment parameters. The nonlinearity of the testers are determined with $2-tone$ measurements to obtain the baseline using the attenuator values given above. As seen from Table 5.5, absolute errors are still very low for the same injected impairment parameters used in simulations.

There is a $0.8dB$ deviation in the receiver IIP_3 which indicates that the extraction method may have a bias for high IIP_3 values. With such high linearity of the tester transceiver, the nonlinear signal terms are greatly suppressed and become comparable to the noise floor. A normal transceiver linearity is not expected to be as high as these testers. Therefore, the proposed test method performs much better with more detectable nonlinear signals terms at the captured response.

Table 5.5: Measurement RMS Errors over 20 Runs

Parameter	Injected	Mean	ST Dev.	RMS Error
φ_{Tx}	5.0 °	4.936 °	0.202 °	0.207 °
g_{Tx}	-0.25	-0.256	0.0079	0.095
φ_{Rx}	-4.3 °	-4.347 °	0.146 °	0.150 °
g_{Rx}	0.1	0.095	0.0038	0.0059
τ_{TX}	38 ns	39.28 ns	0.79 ns	1.49 ns
τ_{RX}	51 ns	48.70 ns	2.23 ns	2.53 ns
DC_I	0.2 V	0.195 V	2.57 mV	5.55 mV
DC_Q	0.15 V	0.155 V	3.95 mV	6.33 mV
Parameter	2-tone	Mean	ST Dev.	RMS Error
$TX-IIP_3$	24.70 dBm	24.32 dBm	0.23 dB	0.43 dB
$RX-IIP_3$	16.97 dBm	17.84 dBm	0.34 dB	0.94 dB

Test Time and Digital Modulation Requirements

The total test time of the proposed method has three components, which can be listed as the test setup time, the capture time and the analysis time. Test setup time is due to initialization of the DUT and the tester. The capture time, which is determined by the test vector length, also affects the analysis time since longer test vector means more data to process. According to the experiments, all three components of the total test time are comparable to each other and they are on the order of $100ms$. These numbers are roughly measured with test routines that are not currently optimized for speed.

The test method is suitable for all digital baseband modulation schemes generating I/Q channels since it calculates quasi-symbols by integrating I and Q signals. In constant pulse modulation schemes such as QPSK and QAM, altering integration interval may not be necessary since the time shifts can be easily associated with real symbol values.

BiST and BoST Implementation Options

According to the available on-chip resources, the test method may have different implementations. BiST application requires a baseband DSP and on-chip memory such that all data collection and data processing can be performed on-chip. Due to the nature of the NLS estimation technique, data collection and data processing should be pipelined.

If the on-chip resources are limited to digitizing and storage, the test method can be implemented as a BoST scheme such that computation is performed on the digital tester. In that case, the memory requirement is increased by the number of time samples per pulse because time samples of a pulse will be integrated to symbol values in the digital tester. The access of the digital tester to the on-chip memory can be obtained through a data bus.

5.5 Summary

This chapter presents a loop-back based BiST approach for quadrature modulation transceiver circuits to decouple impairment parameters of the transmitter and the receiver paths by using only baseband input/output signals.

The first BiST method of the proposed test approach measures I/Q mismatch and I/Q time skew parameters and determines DC carrier leakage at the receiver output in a single test. Our method utilizes the LS estimation technique to extract the impairment parameters using QPSK modulated test signals. A realistic system model is derived including loop-back path delay as well as time delays on both sides of mixers. Test method accuracy is evaluated with MATLAB simulations. RMS estimation errors for the impairment parameters are below 1.5% for the shortest test vector and highest noise power.

In the second BiST method, we modify the previous BiST method to include nonlinearity characteristics of the transmitter and the receiver in the derived transceiver model. We also eliminate the baseband modulation requirement of the previous test method to be compatible with any kind of modulation scheme. The impairment parameters are extracted with NLS method in two consecutive measurements obtained with different loop-back attenuation settings.

The test method accuracy is evaluated with MATLAB RMS simulations. RMS errors for I/Q phase mismatch and I/Q gain mismatch are 0.1° and 0.008 respectively. Time skew and DC offset parameters are extracted with and $2ns$ and $9mV$ RMS errors. Nonlinearity parameters extraction error is around $1.4dB$ RMS. Conducted experiments on a transceiver circuit built with off-the-shelf components yield 10% RMS error when compared with traditional test methods. Results of extended experiments on an RF tester (LitePoint IQnxn) are in good agreement with simulations.

Low complexity, short test time, digitally implemented signal processing and numerical analysis routines enable the BiST implementation of our test method since the only required test resource is an on-chip DSP with data converters.

6

2x-Site Test of RF Transceivers

New generation handheld devices achieve high levels of functionality by providing users multiple communication options. Each of these options employs a different communication standard. Within a handheld device, multiple communication standards are usually implemented with separate radios or transceivers due to the diversity of the required specifications of these standards. Extensive allocation of frequency bands in the communication spectrum makes these specifications more aggressive. Even small parametric deviations of the device characteristics may lead to a failure of compliance with the specifications of the communication standard. For example, 2% gain imbalance and 2 ° phase imbalance between I/Q channels reduce the infinite image rejection of the quadrature modulation receiver to $-40dBc$ [60–62]. Therefore, each device coming out of the production line has to be tested thoroughly in order to guarantee the proper operation.

The native structure of the RF transceiver has traditionally led test engineers into a two-step test process where the transmitter and the receiver are tested separately. In the recent years, this approach become a very expensive test solution due to the advancements in the semiconductor technology. New generation devices not only

operate at very high frequencies but also become very complex in order to achieve required specifications.

Many solutions have been proposed to reduce overall test cost of RF transceivers [5–12, 39, 63–65]. Earlier, the main focus in these test approaches is to reduce the equipment cost by utilizing low cost testers. In the test approaches focusing on lowering test time per device, test engineers introduce new high level performance parameters such as error-vector-magnitude (EVM) and packet(bit)-error-rate (PER) to skip lengthy test routines [43]. These parameters provide an overlook on the performance of the device including effects of all the low level performance characteristics such as I/Q imbalance and nonlinearity. EVM is usually used to determine the quality of transmitters whereas PER is usually measured to determine the receivers' input sensitivity. However, these parameters are not sufficient to characterize the transceiver circuit since the effects of low level performance parameters are not equally represented. Moreover, some parameters may mask the effects of others in the measurements of EVM or PER.

Another test approach targeting to lower both equipment and test time costs is proposed as BiST, which utilizes available on-chip resources such as data converters and baseband DSP for test purposes [9–11, 63, 64]. In the previous chapter we proposed loop-back based BiST methods for QPSK [63] and GMSK [65] systems to measure impairment parameters such as I/Q imbalance, I/Q time skew, and transmitter/receiver nonlinearity.

In any loop-back test for an RF transceiver, the transmitter and the receiver have to be active at the same time in order to establish the low-frequency path from transmitter inputs to receiver outputs. However, the transmitter and the receiver may not be designed to operate simultaneously. Designers may not recommend full characterization of the device in the loop-back mode due to isolation issues between the transmitter and the receiver. Therefore, the traditional 2-step test scheme may

seem to be the only choice for accurate measurements. However, the multi-site test approach, which is a recent trend in high volume production environment, may be utilized for RF transceivers to decrease the test time per DUT [42, 43]. Having multiple devices on the load board [42] reduce overall test setup times. Moreover, analysis for each device placed on the load board can be performed in parallel. Therefore, the test time per DUT can be reduced by a factor, which is theoretically equal to the number of devices placed on the load board.

In the current multi-site test approach, each RF transceiver is treated as a separate path and the transmitter and the receiver are still tested separately. While the test is performed for each device on the load board at the same time with the shared input signal, the output signals have to be captured separately. This approach requires sampling the output signals at the same time, requiring more test resources. Moreover, since the receiver and the transmitter are tested separately, RF instrumentation, either at the automatic test equipment (ATE) or on the load-board is necessary.

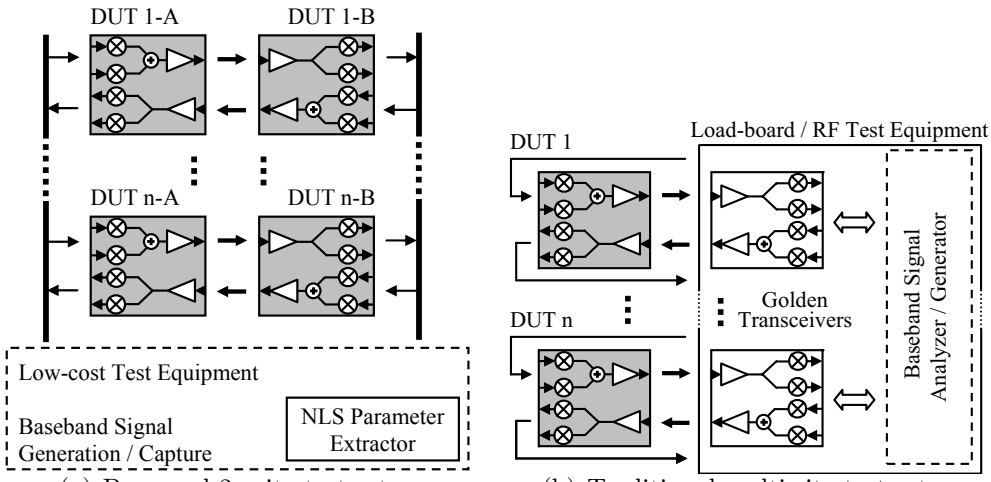
In this chapter, we propose a 2-xsite test scheme, which is a special case of multi-site test, capable of testing an even number of RF transceivers at the same time to measure a set of impairment parameters including I/Q imbalance, I/Q time skew, nonlinearity and DC offsets of the transmitter and the receiver. In this method, we combine the advantages of loop-back based testing with that of multi-site testing and propose a solution where the transmitter of one device is connected to the receiver of another to create a complete path with low frequency digital baseband inputs and outputs. The test method apply digital signals to the path input and it captures the digital response at the path output. The impairment parameters are extracted from the relation between these digital input/output test signals. We avoid the leakage and performance degradation issues since the transmitter and the receiver reside on separate chips. Moreover, the frequency offset between the transmitter

and the receiver is not an issue as the two synthesizers can be set to the desired frequencies independently. This makes the approach applicable to a wide range of architectures, including low-IF, and wide-IF architectures, where direct loop-back is not feasible [66]. Our approach can be used with any number of sites as long as there are an even number of transceiver chips that can be connected into a full path.

In our method, we focus on GMSK modulated signals with a packet-based solution, where the transceivers are operated under their normal conditions enabling accurate evaluation of parameters that may be affected by the duration of activity, such as the LO frequency drift. We support the proposed theory with MATLAB simulations as well as two sets of experiments performed on RF testers and on an RF transceiver built with discrete components. Results of both simulations and experiments confirm the accuracy of the proposed method.

6.1 The Test Method

Our method takes advantage of the signal path obtained by the transmitter-to-receiver (TX-RX) connection shown in Figure 6.1(a). The low-cost test equipment utilized in the proposed method only analyzes baseband input/output signals in order to extract impairment parameters of the RF transceiver. This may resemble the loop-back based BiST methods that we proposed in the previous chapter. However, substantial differences exist and we need to deal with new challenges of the new test setup. First, the synthesizers are not coherent because the transmitter and the receiver reside on separate chips. The captured signals on the receiver have additional artifacts due to the frequency/phase mismatch between LOs. Moreover, in the case of a LO frequency mismatch, an additional time dependency of received signals comes into the picture, which prevents us from using the the estimation technique presented in the BiST method for QPSK modulation scheme. Therefore, we adopt a modified version of the analysis technique used in the second BiST method



(a) Proposed 2x-site test setup (b) Traditional multi-site test setup

FIGURE 6.1: Proposed and traditional muti-site test setups

with the extended set of impairment parameters. The analysis technique is based on NLS method [56, 57] to handle the time-dependent mapping between baseband input/output signals and system impairments without the necessity of introducing intermediate parameters.

We introduced a packet based analysis scheme to mimic the normal operational conditions of the transceiver since the actual data transferred is over signal packets defined by the communication standard. Non-packet based continuous analysis techniques have the drawback of shifting the device characteristics due to continuous power dissipation and frequency drift.

The main advantage of the proposed method over the current practice in multi-site testing is that both of the devices on the load board are under test at the same time. In a more traditional two-step multi-site test scheme (depicted in Figure 6.1(b)), the complementary device on the signal path (receiver or transmitter) either resides in the test equipment or on the load board (fully pre-characterized golden transceiver) and it used for testing the DUT. Our full-path multi-site test approach allows us to test all of the devices placed on the load board. Effectively, a single

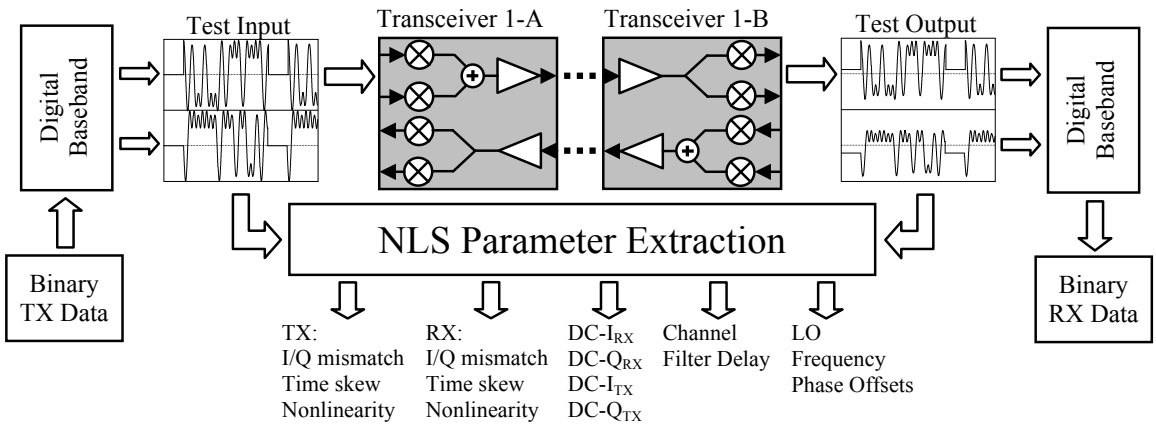


FIGURE 6.2: 2-site Test Method

measurement yields all the impairment parameters of both the transmitter and the receiver of the RF transceiver separately.

6.1.1 2x-site Test Setup

The 2x-site test setup for two transceivers (2-site only) is shown in Figure 6.2. As long as there are enough resources, the test setup can be extended to any number of sites with an even number of devices. Pin count and the available data storage of the test equipment determine the number of sites for the test setup. The proposed NLS parameter extraction algorithm runs on the test equipment analyzing digitally modulated baseband I/Q signals collected from the test inputs and outputs. Therefore, the low-cost test equipment needs only baseband signaling capabilities including signal generation/capture. Depending on the transceiver baseband interface (analog/digital), the tester may need to have data converters. For fully integrated transceivers having a DSP, the test equipment is only needed for data storage and signal analysis since the baseband test signals can be generated and captured on-chip.

The RF paths between devices are physical signal paths placed on the test board to connect transmitters to receivers. An attenuator may be needed to reduce the powerful transmitter output to within the dynamic range of the receiver [46].

6.1.2 Test Method Challenges

In our test method, we derived an analytical transceiver model to include effects of all the impairment parameters of the transceiver on the test output signals. Given the input test signal, the derived model can predict output signals of the transceiver. We utilize this model to establish the mapping between input/output signals. The NLS algorithm uses the derived model and the test input/output signals to solve for the impairment parameters while minimizing the error associated with the mapping function. Hence, the model of the transceiver or the DUT has to be accurate enough to extract impairment parameters with the lowest error possible.

However, developing the analytical model of a transceiver is not an easy task since it has many cascaded blocks with nonlinear characteristics. Since we adopted the modified version of our loop-back BiST approach with the similar analytical transceiver model, same loop-back test challenges such as TX-RX parameter decoupling and physical RF path delay also appear in this method. In addition to these loop-back test challenges, we have to deal with the relative LO frequency/phase mismatch problem of the 2x-site test setup while deriving the new transceiver model. Since the LO frequency/phase mismatch are unknown, the received baseband signals can not be down-converted to the correct IF. We introduced additional model parameters for LO frequency/phase mismatch in order to include their effect in the mapping function.

After carefully modeling the effect of all impairment parameters on the signals, we can obtain expressions that relate the time-dependent sampled input/output signals to system impairments. We basically form a new equation from each collected data point pair to preserve the time-variant information. As a result, we have many more equations than unknowns, and use the NLS estimation technique to extract the unknowns.

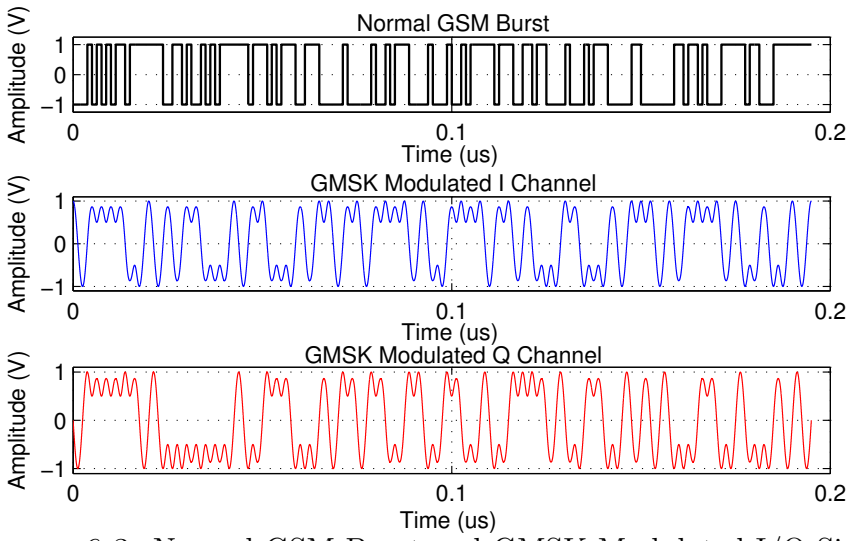


FIGURE 6.3: Normal GSM Burst and GMSK Modulated I/Q Signals

6.1.3 Test Signals

Signals used in the proposed test method are digitally modulated low frequency baseband signals. There is no requirement on the test signals other than the constraints of the communication standard. The signal processing technique used in our method accepts almost any kind of digitally modulated signals as well as plain signals such as single- or two-tone waveforms.

For the presentation of our method, we used GMSK modulated I/Q baseband signal packets of $156 - bit$ length to be compatible with the packet based GSM standard. Modulated I/Q signals can be seen in Figure 6.3 with the GSM Burst [67].

6.2 Transceiver Model

The RF front end of the transceiver is an analog circuit. Thus, it is prone to parametric deviations due to process variability. As the specifications deviate from the nominal values, the signals at the receiver output start to degrade in many ways, such as shifting in time and mixing with I or Q channel.

6.2.1 Impairments

In this chapter, we extend the transceiver model explained in Section 5.1 so that the new model includes all the impairments shown in Figure 6.4 as shaded blocks as well as new impairment parameters and parameters due to the new test setup. We will explain the effects of new impairment and test setup parameters in the following paragraphs.

DC Offsets

DC offset is a common problem in analog circuits. It can affect the circuit performance by reducing the dynamic range. In the new transceiver model, we define separate DC offset parameters for the transmitter inputs and for the receiver outputs. The DC offsets at the transmitter inputs are mainly due to the DACs. If the transmitting and receiving parties match in terms of LO frequency, the effects of transmitter DC offsets and receiver DC offsets are combined at the receiver outputs. However, if there is a slight LO frequency mismatch, a sinusoidal signal component at

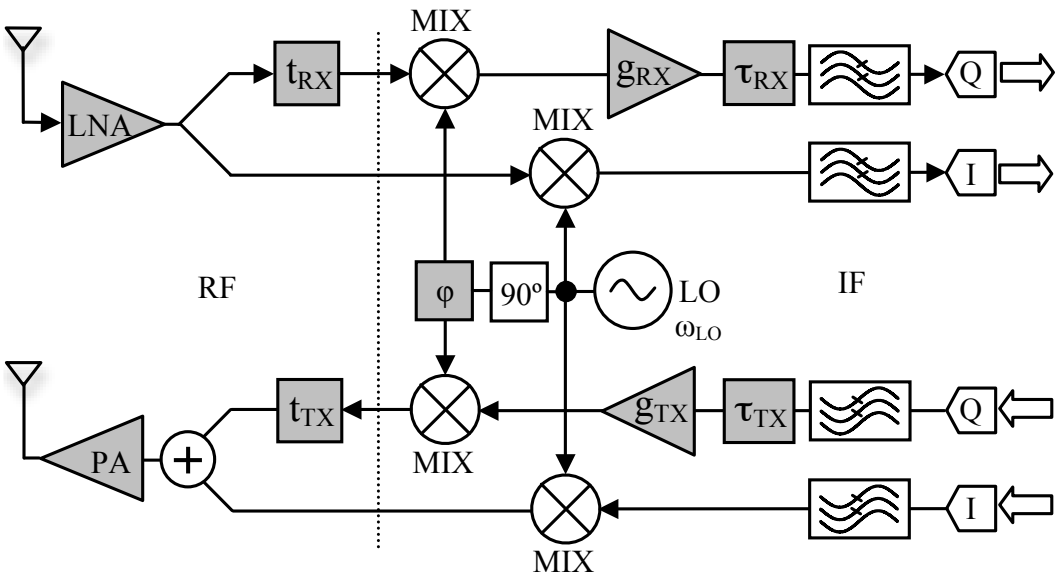


FIGURE 6.4: Transceiver Block Diagram with Impairments

the mismatch frequency degrades the receiver output with an amplitude proportional to the DC offset at the transmitter input. DC offsets at the receiver output are usually due to the insufficient isolation between RF and LO ports of the down-conversion mixers.

Receiver Channel Filter Delay

We define a time delay parameter for the receiver channel filters to include the effect of their group delays. Group delay may not be an impairment parameter because every filter has an inherent group delay. However, we need to define this parameter for the accuracy of the transceiver model. This parameter may include delays of the following blocks on the signal path such as the ADC. Since delays of these cascaded blocks are accumulated as the signal travels down on the channel, there is no possible way to discriminate the delays of individual blocks.

LO Frequency Drift

As a consequence of the proposed test setup, the relative frequency drift between LO signals of two transceivers may be defined as another impairment parameter because the LO frequencies of the transceivers should match for proper operation. Since it is a relative parameter we can not determine the faulty transceiver, if the frequency drift does not fall in the given specification range. Further investigation is required to determine the faulty device. We define a LO frequency mismatch parameter in our transceiver model together with a LO phase mismatch parameter. The LO phase mismatch parameter is required for the transceiver model to count for incoherency effects at the output signals because the transceivers' LOs are not coherent as in the loop-back case.

6.2.2 The Linear Transceiver Model

Following the small signal amplitude assumption of Section 5.4.3 at the transmitter inputs, we will derive the transceiver model assuming linear circuit blocks with additional impairment parameters of transmitter input DC offsets and channel filter delay. Then, we will include nonlinearities of the transmitter and the receiver using third order gain functions to develop analytical nonlinear model.

We add the transmitter baseband input DC offsets as additional components to the I/Q baseband signals. If the I/Q signals at the input of the transmitter are $I(t)$ and $Q(t)$, and the I channel is taken as the reference, the signals at the inputs of the up-conversion mixers will be:

$$\begin{aligned} I'(t) &= I(t) + DCI_{TX} \\ Q'(t) &= (1 + g_{TX}) \cdot [Q(t - \tau_{TX}) + DCQ_{TX}], \end{aligned} \tag{6.1}$$

where g_{TX} is the gain mismatch, τ_{TX} is the baseband time skew, and DCI_{TX} and DCQ_{TX} are the DC offsets at the input of the transmitter. Since we take I channels as the reference for both the transmitter and the receiver, we model LO signals with I/Q phase mismatch parameters (φ_{TX} and φ_{RX}) as follows:

$$\begin{aligned} LOI_{TX} &= \cos(\omega_{LO}t) \\ LOQ_{TX} &= -\sin(\omega_{LO}t + \varphi_{TX}) \\ LOI_{RX} &= \cos((\omega_{LO} + \omega_d)t + \varphi_d) \\ LOQ_{RX} &= -\sin((\omega_{LO} + \omega_d)t + \varphi_d + \varphi_{RX}), \end{aligned} \tag{6.2}$$

where ω_d is the relative frequency drift and φ_d is the relative phase offset between LOs. Using the modeled LO signals for up-conversion with the signals expressed in Equation (6.1) including the baseband time skew, gain mismatch and DC offsets of the transmitter, the RF signal transmitted through the antenna can be expressed

as:

$$\begin{aligned} r_{RF}(t) &= I'(t) \cdot \cos(\omega_{LO}t) - Q'(t) \cdot \sin(\omega_{LO}t + \varphi_{TX}) \\ &= G_{TX} \cdot \{[I(t) + DCI_{TX}] \cdot \cos(\omega_{LO}t) - \\ &\quad (1 + g_{TX}) \cdot [Q(t - \tau_{TX}) + DCQ_{TX}] \cdot \sin(\omega_{LO}t + \varphi_{TX})\}, \end{aligned} \tag{6.3}$$

where G_{TX} is the gain of the transmitter of DUT 1-A in Figure 6.2. This signal may be attenuated by the RF path to be compatible with the receiver dynamic range.

As the transmitting and receiving parties are in different devices, the LOs do not match in terms of phase even if their frequencies mismatch perfectly. Therefore, defining a delay between the transmitter and the receiver in terms of time does not make much sense. In this new transceiver model, we eliminate the time delay between the transmitter and the receiver by embedding its effect in the LO phase mismatch. This modification allows us to define an additional delay parameter for the receiver side apart from the time skew to count for the delays of the receiver channel filters and the following blocks on the signal path.

In a similar way to up-conversion , we can express the I/Q signals at the output of the down-conversion mixer of the receiver of DUT 1-B in Figure 6.2 as:

$$\begin{aligned} I'_{RX}(t) &= \frac{G_{RX}}{k} \cdot r_{RF}(t) \cdot \cos((\omega_{LO} + \omega_d)t + \varphi_d) \\ Q'_{RX}(t) &= -\frac{G_{RX}}{k} \cdot r_{RF}(t) \cdot (1 + g_{RX}) \cdot \sin((\omega_{LO} + \omega_d)t + \varphi_d + \varphi_{RX}), \end{aligned} \tag{6.4}$$

where G_{RX} is the gain of the receiver and k is the attenuator gain. Channel filtering eliminates the high frequency components of the down-converted I/Q signals due to the frequency mixing operation. Finally, substituting $r_{RF}(t)$ into the above equation

and delaying the I/Q signals for receiver time skew and filter group delay yield:

$$\begin{aligned} I_{RX}(t) = 0.5 \cdot G \cdot \{&[I(t - t_{LPF}) + DCI_{TX}] \cdot \cos(\alpha(t)) - \\ &(1 + g_{TX}) \cdot [Q(t - t_1) + DCQ_{TX}] \cdot \sin(\varphi_{TX} - \alpha(t))\} \\ Q_{RX}(t) = -0.5 \cdot G \cdot (1 + g_{RX}) \cdot \{&[I(t - t_2) + DCI_{TX}] \cdot \sin(\varphi_{RX} + \alpha(t) - \beta) - \\ &(1 + g_{TX}) \cdot [Q(t - t_3) + DCQ_{TX}] \cdot \cos(\varphi_{TX} - \varphi_{RX} - \alpha(t) + \beta)\}, \end{aligned} \quad (6.5)$$

where the simplification parameters are defined as:

$$\begin{aligned} G &= \frac{G_{TX}G_{RX}}{k} \\ t_1 &= \tau_{TX} + t_{LPF} \\ t_2 &= \tau_{RX} + t_{LPF} \\ t_3 &= \tau_{TX} + t_{RX} + t_{LPF}. \\ \alpha(t) &= \omega_d t + \varphi_d - \omega_d \cdot t_{LPF} \\ \beta &= \omega_d \cdot \tau_{RX}. \end{aligned} \quad (6.6)$$

$\alpha(t)$ is due to frequency/phase offsets between LOs and the channel filter delay, whereas β is due to frequency offset between LOs and receiver time skew.

6.2.3 The Nonlinear Transceiver Model

Equation 6.5 is the complete linear response of the transceiver including all impairment parameters except for the nonlinearities. Nonlinear response of the transceiver will include Equation 6.5 as the linear term in addition to nonlinear signal terms. In order to derive the nonlinear transceiver model, we assign nonlinear gain functions given in Equation 5.2 to the transmitter and the receiver paths up the third order. The linear model derivation steps are followed with the help of a symbolic solver to obtain the full analytical response. Since the nonlinearity of the whole transmitter or the receiver path can be approximated with the gain functions defined in Equation

5.2, we can use linear gain coefficients (α_1 and β_1) of the transmitter and the receiver instead of G_{TX} and G_{RX} in Equation 6.5.

After following the simplification and necessary channel filtering steps the nonlinear analytical response of the signal path of the proposed test setup can be obtained as:

$$\begin{aligned} I_{RX}(t) &= 0.5 \cdot \{[I(t-t_{LPF}) + DCI_{TX}] \cdot \cos(\alpha(t)) - \\ &\quad (1+g_{TX}) \cdot [Q(t-t_1) + DCQ_{TX}] \cdot \sin(\varphi_{TX} - \alpha(t))\} \cdot \sum \kappa \\ Q_{RX}(t) &= -0.5 \cdot (1+g_{RX}) \cdot \{[I(t-t_2) + DCI_{TX}] \cdot \sin(\varphi_{RX} + \alpha(t) - \beta) - \\ &\quad (1+g_{TX}) \cdot [Q(t-t_3) + DCQ_{TX}] \cdot \\ &\quad \cos(\varphi_{TX} - \varphi_{RX} - \alpha(t) + \beta)\} \cdot \sum \kappa \end{aligned} \tag{6.7}$$

where κ is the coefficient vector due to nonlinearity and it contains cascaded linear and nonlinear gain coefficients. κ is calculated with a symbolic solver by using the gain coefficients as:

$$\begin{aligned} \kappa &= [c_0 \quad c_1 p \quad c_2 p^2 \quad c_3 p^3 \quad c_4 p^4] \\ c_0 &= \frac{\alpha_1 \beta_1}{k} \\ c_1 &= \frac{3}{4}\frac{\alpha_3 \beta_1}{k} + \frac{3}{2}\frac{\alpha_1 \alpha_2 \beta_2}{k^2} + \frac{3}{4}\frac{\alpha_1^3 \beta_3}{k^3} \\ c_2 &= \frac{5}{4}\frac{\alpha_2 \alpha_3 \beta_2}{k^2} + \frac{15}{8}\frac{\alpha_1 \alpha_2^2 \beta_3}{k^3} + \frac{15}{8}\frac{\alpha_1^2 \alpha_3 \beta_3}{k^3} \\ c_3 &= \frac{105}{64}\frac{\alpha_2^2 \alpha_3 \beta_3}{k^3} + \frac{105}{64}\frac{\alpha_1 \alpha_3^2 \beta_3}{k^3} \\ c_4 &= \frac{63}{128}\frac{\alpha_3^3 \beta_3}{k^3} \\ p &= [I(t-t_{LPF}) + DCI_{TX}]^2 + (1+g_{TX})^2 \cdot [Q(t-t_1) + DCQ_{TX}]^2 - \\ &\quad 2 \cdot [I(t-t_{LPF}) + DCI_{TX}] \cdot (1+g_{TX}) \cdot [Q(t-t_1) + DCQ_{TX}] \cdot \sin(\varphi_{TX}) \end{aligned} \tag{6.8}$$

Equations 6.7 and 6.8 provide complete nonlinear response of the signal path containing a transmitter and a receiver on separate test chips. Defining nonlinearity parameters to transmitter or receiver paths instead of nonlinear blocks inside these paths may seem less accurate at the first sight. However, since we are interested in the overall nonlinearity of the transmitter or the receiver, we can always model the nonlinearity at the input (or output) node of the system without much loss in accuracy. In Section 5.4.3, we performed a simulation for our loop-back based BiST method having a similar nonlinear transceiver model to prove this concept.

6.3 Test Signals and Parameter Extraction

The nonlinear model of the transceiver is the basis for the parameter extraction algorithm which uses baseband test inputs and test outputs. The test signals are digitized samples of actual signals collected at the corresponding instants since the derived transceiver model is time dependent. This is important especially for the accurate extraction of time related parameters such as time skews and the filter delay.

6.3.1 Symbol Calculation

The collected signal samples can not be used directly in the extraction algorithm because of the time related parameters. Since the transmitted signals usually do not have constant pulse profiles except for some of the modulation schemes such as QPSK, it is impossible to relate time shifts or time delays to an arbitrary shaped pulse without altering the signal samples. As in all communication standards, the received signals are integrated over a time period to calculate actual symbols which are finally translated into actual binary data. In our test method, we use the symbol calculation method explained in Section 5.4.4 to calculate the quasi-symbols which have basically

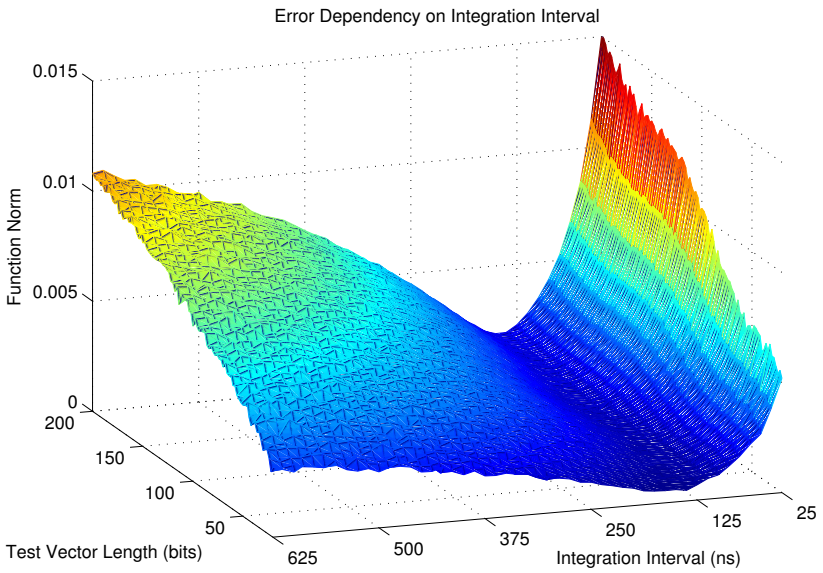


FIGURE 6.5: Error due to Integration Interval

shorter integration intervals than the actual symbol period. The integration to obtain quasi-symbols is done in the digital domain by software. Since we need to preserve time-dependent information for both the inputs and the outputs to extract the time related parameters, we store the integration results for both signals.

We performed a simulation similar to the previous chapter to evaluate the error introduced by using quasi-symbols. The norm of the function obtained from the nonlinear transceiver model given in Equations 6.7 and 6.8 is our error metric. The 3-D plot given in Figure 6.5 shows the error with respect to the integration interval and the test vector length. We use the integration interval that gives the minimum error for the given test vector length. System parameters, such as sampling frequency and bit duration affect the simulation. Therefore, the integration interval should be chosen according to the transceiver system.

6.3.2 Nonlinear System Equations

After obtaining the quasi-symbols, the nonlinear system equations of the complete TX-RX path of two separate devices can be constructed by using the nonlinear

transceiver model derived in Equations 6.7 and 6.8. We will construct the complete equation starting from the linear term:

$$LT_n = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} I_n \\ Q_n \end{bmatrix} + \begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} I_{n-1} - I_n \\ Q_{n-1} - Q_n \end{bmatrix} \tag{6.9}$$

where I_n and Q_n are the transmitted quasi- symbols and n is the symbol index. Matrix entries A through D and a through d are time varying parameters and they can be written as functions of impairment parameters:

$$\begin{aligned} A &= 0.5 \cdot \cos(\alpha(t)) \\ B &= -0.5 \cdot (1 + g_{TX}) \cdot \sin(\varphi_{TX} - \alpha(t)) \\ C &= -0.5 \cdot (1 + g_{RX}) \cdot \sin(\varphi_{RX} + \alpha(t) - \beta) \\ D &= 0.5 \cdot (1 + g_{RX}) \cdot (1 + g_{TX}) \cdot \cos(\varphi_{TX} - \varphi_{RX} - \alpha(t) + \beta) \\ a &= A \cdot (t_{LPF})/T_B \\ b &= B \cdot (t_{LPF} + \tau_{TX})/T_B \\ c &= C \cdot (t_{LPF} + \tau_{RX})/T_B \\ d &= D \cdot (t_{LPF} + \tau_{TX} + \tau_{RX})/T_B \end{aligned} \tag{6.10}$$

where T_B is the integration interval and $\alpha(t)$ and β are given in Equation 6.6. In order to calculate the nonlinear terms, we need to calculate the discrete version of $p(t)$ given in Equation 6.8 for every signal sample:

$$\begin{aligned} \acute{I}_n &= \begin{bmatrix} 1 & \frac{t_{LPF}}{T_B} \end{bmatrix} \begin{bmatrix} I_n \\ I_{n-1} - I_n \end{bmatrix} + DCI_{TX} \\ \acute{Q}_n &= (1 + g_{TX}) \cdot \begin{bmatrix} 1 & \frac{t_{LPF}+\tau_{TX}}{T_B} \end{bmatrix} \begin{bmatrix} Q_n \\ Q_{n-1} - Q_n \end{bmatrix} + DCQ_{TX} \\ p_n &= \acute{I}_n{}^2 + \acute{Q}_n{}^2 - 2 \cdot \sin(\varphi_{TX}) \cdot \acute{I}_n \cdot \acute{Q}_n. \end{aligned} \tag{6.11}$$

Combining all the calculated linear (Equation 6.9) and nonlinear terms (Equation 6.11) according to Equation 6.7 will finally yield the complete nonlinear response

$$\begin{bmatrix} I_{RXn} \\ Q_{RXn} \end{bmatrix} = \left[\begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} I_n \\ Q_n \end{bmatrix} + \begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} I_{n-1} - I_n \\ Q_{n-1} - Q_n \end{bmatrix} \right] \begin{bmatrix} c_0 & c_1 & c_2 & c_3 & c_4 \end{bmatrix} \begin{bmatrix} 1 \\ p_n \\ p_n^2 \\ p_n^3 \\ p_n^4 \end{bmatrix} + \begin{bmatrix} DCI_{RX} \\ DCQ_{RX} \end{bmatrix} + \begin{bmatrix} \omega I_n \\ \omega Q_n \end{bmatrix} \tag{6.12}$$

of the signal path. The last two vectors in Equation 6.12 are DC levels at the I/Q channels of the receiver and the ambient noise present in the communication channel.

6.3.3 Parameter Extraction

In our earlier loop-back based BiST method for QPSK signals presented in the previous chapter, the matrix entries in Equation 6.10 representing the system behavior were time-independent. As a result, we could use the Linear Least Squares method to extract impairment parameters. With the time dependent mapping between GMSK modulated input/ output signals, we can not use Least Squares method. Fortunately, the formulation of the system behavior in terms of quasi-symbols enables us to use the NLS estimation technique explained in Section 5.4.6 for parameter extraction.

In our system model, we have a data set for both I and Q channels, therefore we have $2N$ data samples of inputs and outputs. The time dependent parameter is α which is divided into three different parameters as expressed in Equation 6.6. The vector function is constructed with the time vector and transmitted/received quasi-symbol vectors for both I and Q channels. Unknowns of the normal equation set is our transceiver impairment parameter list composed of transmitter and receiver I/Q gain/phase mismatch, I/Q time-skew, nonlinearity, DC offsets, and relative LO frequency drift. The channel filter group delay and LO phase offset may not be considered as impairments however, they are needed for an accurate model.

In our test method, we keep the solver boundaries several times the specification

range of the circuit. If the circuit is severely degraded, the algorithm converges to the boundaries indicating a faulty circuit. For the circuits which have minor/moderate degradation, the algorithm extracts the impairment parameters. The convergence of this method is more robust than the second BiST method presented in the previous chapter since the time dependent mapping between input/output signal decrease the linear dependency within the system of equations.

6.4 Results and Discussion

We perform numerical simulations in MATLAB to evaluate the accuracy and the robustness of our test method in the presence of additive Gaussian noise, LO phase noise and LO leakage. We also perform measurements on RF testers and on a transmitter-receiver 2- site setup built with off-the-shelf components to compare simulation and measurement results.

6.4.1 Simulation Test Setup and Results

In MATLAB, we implemented the transmitter and the receiver paths depicted in Figure 6.4 with all the impairments. We used digital baseband test inputs generated as randomized GMSK signals with pulse duration of $1.25\mu s$. The test vectors are $156-bit$ length in the GSM packet format defined in [67] . The carrier and the sampling frequencies are chosen as $2.4GHz$ and $80MHz$ respectively to be compatible with the RF test equipments (LitePoint IQnxn) used in the experiments.

In order to evaluate the accuracy, we performed RMS simulations over multiple runs with $8-bit$ and $12-bit$ ADC resolutions. To mimic the real operation, we introduce channel noise to the RF signal path with power of $-110dB/Hz$. We also add phase noise ($-70dBc$) and leakage characteristics to the both transceiver LOs. Table 6.1 shows the simulation results with a $8-bit$ and $12-bit$ resolutions for the data converters. The injected LO leakage characteristic is measured as the receiver

Table 6.1: RMS Errors over 170 Packets

		8-bit ADC			12-bit ADC			
Parameter	Injected	Mean	STD	RMS Error	Mean	STD	RMS Error	Solver Bounds
φ_{TX}	4.1°	4.12°	0.054°	0.056°	4.12°	0.055°	0.059°	± 20°
g_{TX}	0.14	0.139	0.0009	0.0012	0.139	0.0008	0.0011	± 0.3
τ_{TX}	15.0 ns	15.06 ns	0.468 ns	0.471 ns	14.97 ns	0.489 ns	0.489 ns	0 - 100 ns
DCI_{TX}	-55 mV	-55 mV	0.0 mV	0.0 mV	-55 mV	0.0 mV	0.0 mV	± 0.2 V
DCQ_{TX}	4 mV	4 mV	0.0 mV	0.0 mV	4mV	0.0 mV	0.0 mV	± 0.2 V
$Gain_{TX}$	3.16	2.87	0.114	0.310	2.86	0.118	0.322	0 - 10
$IIP3_{TX}$	7.3 dBm	7.22 dBm	0.368 dB	0.375 dB	7.20 dBm	0.415 dB	0.427 dB	± 20 dBm
φ_{RX}	-6.1°	-6.09°	0.049°	0.049°	-6.1°	0.045°	0.045°	± 20°
g_{RX}	-0.1	-0.1	0.0005	0.0007	-0.1	0.0005	0.0007	± 0.3
τ_{RX}	13.0 ns	16.76 ns	0.85 ns	3.86 ns	16.68 ns	0.76 ns	3.76 ns	0 - 100 ns
DCI_{RX}	27 mV	27 mV	0.0 mV	0.0 mV	27 mV	0.0 mV	0.0 mV	± 0.2 V
DCQ_{RX}	13 mV	13 mV	0.0 mV	0.0 mV	13 mV	0.0 mV	0.0 mV	± 0.2 V
$Gain_{RX}$	0.36	0.39	0.016	0.039	0.39	0.016	0.040	0 - 10
$IIP3_{RX}$	4.0 dBm	4.59 dBm	0.19 dB	0.628 dB	4.63 dBm	0.221 dB	0.670 dB	± 20 dBm
f_{Drift}	5.0 kHz	5.0 kHz	6.3 Hz	6.3 Hz	5.0 KHz	6.3 Hz	6.3 Hz	0 - 15 kHz
t_{LPF}	9.3 ns	7.70 ns	0.40 ns	1.65 ns	7.68 ns	0.37 ns	1.65 ns	0 - 100 ns

DC offset at I/Q channel outputs. RMS errors are obtained with a single packet test vector through 170 runs with random bit patterns. As can be seen from the RMS error results, there no significant difference between $8-bit$ and $12-bit$ ADC resolutions. These results also indicate that the RMS errors are well below the typical GSM specifications for the extracted impairments and will not affect the transceiver performance.

6.4.2 Experimental Results

In the first set of experiments, we use two RF testers (LitePoint IQnxn) and a programmable RF attenuator box (LitePoint IQexpress) in the middle connected in 2-site test setup shown in Figure 6.6. We choose these testers because they contain fully calibrated and parameterizable transceivers with software control. Bi-directional RF ports can be assigned as either signal generator or signal analyzer. Except for the LO phase offset and time-skew parameters, all the impairments are injected by using the RF tester features. Time-skew parameters are injected to the test input/output signals by shifting transmitted and received samples accordingly.

The testers are configured to operate at $2.4GHz$ carrier frequency with $80MHz$

FIGURE 6.6: Experimental Test Setup, LitePoint RF Testers

sampling rate. The test signals composed of GSM packets are chosen to be identical to the patterns used in the simulations. The first tester, which is configured as the transmitter, is loaded with the test signals. The second RF tester is configured as the receiver to capture the whole test vector with some gap duration between transmitted packets. The RF attenuator is programmed to attenuate RF signals by $10dB$. In this measurement setup, we did not measure transmitter DC offsets, since the effects of this impairment were not modeled in the extraction algorithm at the time of the experiments. In fact, the effect of the transceiver DC offsets were discovered during the second set of experiments that we performed on the transceiver built with off-the-shelf components. The signal generator/analyzer cards used in the second experiment had small DC offsets at the waveform generator output which degraded the received test signals. The IQnxn RF tester has an automatic calibration to eliminate these DC offsets. Therefore, it did not appear at the output signal.

The captured signals are analyzed with the test inputs to extract impairment parameters with the analysis routines used in the simulations with the slight difference in the extraction algorithm omitting the transmitter DC offsets. Table 6.2 summarizes the RMS errors according to the impairment parameters as well as a sample measurement of a single GSM packet. As seen from Table 6.2, absolute errors are still very low for the injected impairment parameters. Since the transmitter and the receiver are the actual RF tester components, the reported nonlinearity characteristics may seem too optimistic. However, as the system gets linear the nonlinear terms get smaller and become comparable to the noise floor. Even with these high linearity characteristics, our method achieved very good error performance on nonlinearity parameters.

In the second set of experiments, we built a transmitter and receiver with discrete transceiver components from MiniCircuits. The transmitter and the receiver have separate LOs, which can be set to have frequency mismatch with steps of $5KHz$.

Table 6.2: RMS Errors over 10 Packets

Parameter	Injected	Mean	STD	RMS Error
φ_{TX}	5.3 °	5.23 °	0.10 °	0.116 °
g_{TX}	-0.2	-0.20	0.0014	0.0018
τ_{TX}	12.5 ns	12.45 ns	0.76 ns	0.72 ns
$Gain_{TX}$	3.16	2.92	0.10	0.26
$IIP3_{TX}$	24.5 dBm	25.11 dBm	0.32 dB	0.68 dB
φ_{RX}	-3.8 °	-3.72 °	0.226 °	0.228 °
g_{RX}	0.15	0.15	0.0024	0.0022
τ_{RX}	25.0 ns	24.96 ns	0.82 ns	0.78 ns
DCI_{RX}	0.1 V	0.099 V	0.4 mV	0.5 mV
DCQ_{RX}	0.15 V	0.149 V	0.6 mV	0.8 mV
$Gain_{RX}$	10.0	10.64	0.35	0.72
$IIP3_{RX}$	16.7 dBm	16.86 dBm	0.20 dB	0.25 dB
f_{Drift}	3 kHz	2.96 kHz	24.5 Hz	43.8 Hz
t_{LPF}	9.3 ns	7.83 ns	1.57 ns	2.09 ns

The transceiver baseband is interfaced with PCI cards installed in a PC and they are controlled through MATLAB. Baseband test signals are generated with the arbitrary waveform generator card and test responses are captured with the digitizer card.

In the test setup shown in Figure 6.7, transmitter and receiver LOs are set to $900.000MHz$ and $900.005MHz$ respectively to have $5Khz$ frequency mismatch. Voltage controlled (90 °) phase shifters are used to inject I/Q phase mismatch to both transmitter and receiver LO signals. However, there is no precise way to set the impairment parameters as in the RF tester experiments. Therefore, we measure most of the impairments in traditional methods such as measuring the IIP_3 with two-tone signals. We compare these measurements with the results of our test method.

Table 6.3 lists the results for both traditional method and our test method including standard deviations calculated over 10 repeated traditional measurements and 10 packets respectively. The empty entries in the table are for the parameters that we could not measure traditionally. Therefore, we can not provide any comparison for those parameters. Generally the two measurement methods are in good

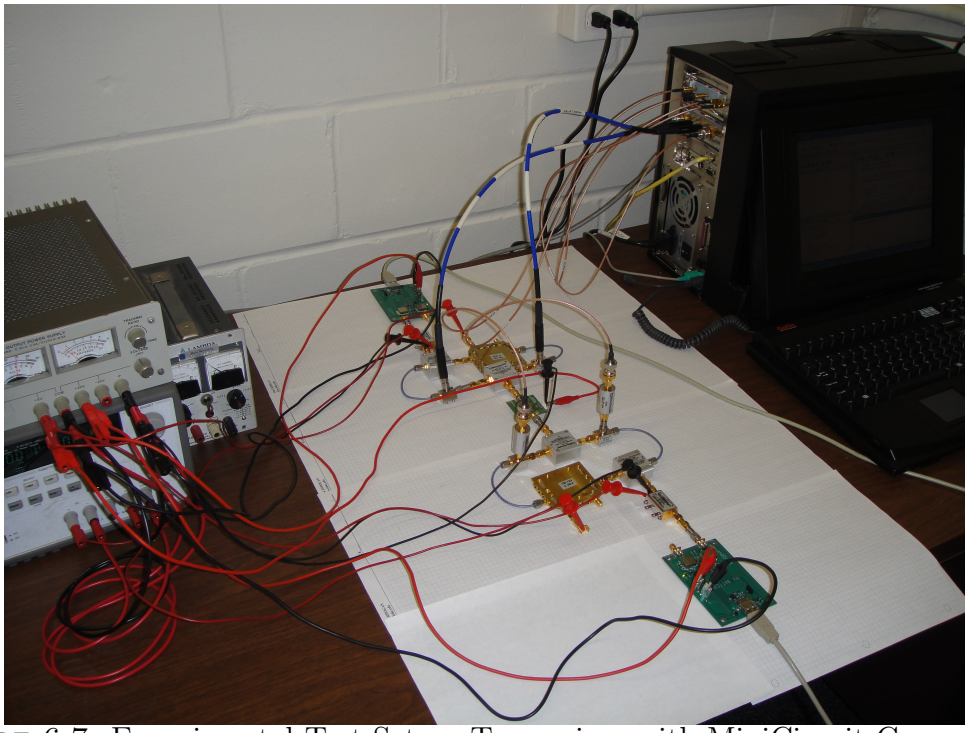


FIGURE 6.7: Experimental Test Setup, Transceiver with MiniCircuit Components

agreement in terms mean values of the parameters. Also the traditional method has slightly smaller standard deviations compared to the proposed method except for the nonlinearity parameters. The standard deviations of the proposed method for the transmitter and receiver IIP_3 parameters are less than the traditional method. This may be due to the two-tone measurement technique of the traditional method, which is more prone to error, since it requires double readouts with different power signal inputs. If we make a comparison between the two test methods in terms of test setup, simplicity and test time, our proposed test method is much better than the traditional test since it provides all the impairment parameters of the transmitter and the receiver separately with only one signal capture.

6.4.3 Test Time Analysis and Baseband Signal Requirements

The capture time per GSM packet is around $200\mu s$ once the tester is initialized. Data analysis for each packet, depends on the convergence time of the algorithm, can be

Table 6.3: STDs of Proposed and Traditional Methods over 10 Packets

	Proposed Method		Traditional Method	
Parameter	Mean	STD	Mean	STD
φ_{TX}	4.075°	0.27°	4.14°	0.169°
g_{TX}	0.139	0.004	0.142	0.001
τ_{TX}	52.19 ns	1.36 ns	-	-
DCI_{TX}	-55 mV	0.0 mV	-55 mV	0.0 mV
DCQ_{TX}	4 mV	0.0 mV	4 mV	0.0 mV
$Gain_{TX}$	2.82	0.23	3.13	0.003
$IIP3_{TX}$	7.27 dBm	0.16 dB	7.03 dBm	0.62 dB
φ_{RX}	-6.16°	0.21°	-6.04°	0.012°
g_{RX}	-0.099	0.003	-0.098	0.0001
τ_{RX}	64.19 ns	2.07 ns	-	-
DCI_{RX}	27 mV	0.0 mV	27 mV	0.0 mV
DCQ_{RX}	13 mV	0.0 mV	13 mV	0.0 mV
$Gain_{RX}$	0.53	0.04	0.50	0.001
$IIP3_{RX}$	4.47 dBm	0.53 dB	4.45 dBm	0.76 dB
f_{Drift}	5.0 kHz	25.2 Hz	5.0 kHz	-
t_{LPF}	128.98 ns	12.12 ns	-	-

optimized by decreasing the sampling frequency, increasing the integration interval and narrowing the solver bounds. Analysis time for the current configuration is in the order of ms and it can be conducted in a pipelined manner, thus will not add to the test time.

There is no specific requirement for the baseband signals since the proposed test method can handle both constant profile and arbitrary shaped pulses. In the constant pulse profile modulation schemes such as QPSK and quadrature amplitude modulation (QAM), the quasi- symbol approach may be omitted to speed up the analysis since the actual symbol values can be used in the parameter extraction algorithm.

6.5 Conclusion

This chapter presents a 2x-site test method where two DUTs are tested as a full RF path. While analyzing only baseband input/output signals, the impairment parameters of the two devices are decoupled from one another using signal processing techniques. We derive a realistic system model with impairments including I/Q mismatch, relative frequency drift, nonlinearity, receiver channel filter delay, transmitter/receiver DC offsets, as well as time delays on both sides of frequency conversion mixers. Test inputs and responses, which are in the GSM packet format, are analyzed with simple test routines to extract performance parameters of the transceiver. Effectively, single measurement yields all the parameters of the transceiver.

Test method accuracy is extensively evaluated with MATLAB simulations as well as two sets of experiments conducted on RF testers and a transmitter/receiver setup built with discrete transceiver components. RMS errors for the I/Q mismatch and time skew parameters are well below specification ranges for the GSM standard. Measurement results using two RF testers and the transmitter/receiver connected in the 2-site test configuration are consistent with each other and with simulations. They confirm the high accuracy of our technique.

Low complexity, short test time and digitally implemented signal processing analysis routines of the proposed test method enable the use of low-cost testers and it also reduces the test time further by the possibility of increasing the number of test sites.

7

Conclusions and Future Work

Today's RF transceiver circuits contain many analog and digital circuit blocks, such as synthesizers, data converters and the analog RF front-end leading to a very complex mixed signal device. Verification of the specifications and functionality of each circuit block and the overall transceiver require RF instrumentation and lengthy test routines. In parallel to the complexity of today's RF devices, overall test costs tend to have an increasing trend in recent years because of the equipment costs, test design/verification costs and costs due to test time. As a result, a substantial portion of the final cost of RF device is allocated by the test costs. The goal of this research is to provide efficient component and system level test methods for RF transceivers which will be low-cost alternatives of traditional tests.

In this thesis, we have proposed component level BiST methods for PLL in-band phase noise and ADC static nonlinearity parameters. Using a clever threshold setting mechanism, the PLL BiST method provides a very robust pass/fail decision with respect to process variations and thermal noise. The proposed ADC BiST detects non-monotonic behavior and provides significantly lower test time if the on-chip resources are limited. Proposed system level tests for RF transceivers are mainly

based on loop-back configuration. Wafer level test method for direct conversion RF transceiver successfully detects catastrophic faults and provides good failure coverage for large parametric faults using a frequency domain envelope signature technique. Loop-back based BiST methods and 2x-site test method successfully decouple all impairment parameters of an I/Q modulating RF transceiver for various baseband modulation schemes.

7.1 Thesis Contributions

Chapter 2 presented a go/no-go BiST system for the synthesizer phase noise which takes advantage of the inherent relation between the output phase noise of the PLL and the amplitude noise on the control voltage of the VCO. The proposed BiST circuit is capable of determining whether the low frequency band-limited integrated noise power at the input of the VCO is above a given threshold. This information effectively enables a pass/fail decision on the synthesizer circuit based on its phase noise specifications without making any measurement at the synthesizer output.

Chapter 3 proposed a complete ADC BiST scheme based on sequential code analysis including a $15-bit$ linear on-chip ramp generator. The analysis scheme has the advantage of detecting non-monotonic behavior of the ADC. When compared to the traditional histogram based analysis, the proposed BiST scheme does not need fast access to the memory when an on-chip memory is available. If an on-chip memory is not available, histogram based techniques require very long test times that are practically inapplicable. The proposed BiST scheme does not increase the test time for those conditions.

Chapter 4 introduced a loop-back test method for wafer level verification of transceiver circuits for detecting catastrophic and large parametric faults. In the proposed method, the transmitter output is directly connected to the receiver input with simple RF attenuator/switch DfT feature. To obtain an observable signal at

the output of the receiver, the receive path is saturated with the high power from the transmitted signal in order to expand the bandwidth of the received signal. Catastrophic faults are detected by checking the presence of the receiver output signal. A signature analysis method based on frequency spectrum envelopes was also proposed for detection of large parametric signal path faults.

Chapter 5 presented a loop-back based BiST approach for quadrature modulation transceiver circuits to decouple impairment parameters of the transmitter and the receiver paths by using only baseband input/output signals. The first BiST method of the proposed test approach measures I/Q mismatch and I/Q time skew parameters and determines the DC carrier leakage at the receiver output in a single test. It utilizes the LS estimation technique to extract the impairment parameters while using QPSK modulated test signals.

The second BiST method modifies the previous BiST method to include nonlinearity characteristics of the transmitter and the receiver in the derived transceiver model. It also eliminates the baseband modulation requirement of the previous test method to be compatible with any kind of modulation scheme. The impairment parameters are extracted with NLS method in two consecutive measurements obtained with different loop-back attenuation settings.

Chapter 6 proposed a 2x-site test method where two DUTs are tested as a full RF path. While analyzing only baseband input/output signals, the impairment parameters of the two RF devices are decoupled from one another. The derived system model with impairments includes relative frequency drift, nonlinearity, receiver channel filter delay, transmitter/receiver DC offsets, as well as time skew on both sides of frequency conversion mixers. Test inputs and responses, which are in the GSM packet format, are analyzed with simple test routines to obtain performance parameters of the transceiver.

7.2 Future Work

This thesis mainly explored system level efficient test methods for RF transceivers. Both of the loop-back BiST methods and the 2x-site test method do not rely on the payload of data modulated into the transmitted baseband signals. In the simulations and experiments, the test signals are generated using random payload data. However, in some baseband modulation schemes, such as orthogonal frequency division multiplexing (OFDM) the demodulated data at the receiver yields some of the impairments of the transceiver system, either the transmitter of the receiver side. This feature of the baseband modulation scheme may be utilized to improve some properties of the proposed test methods.

7.2.1 I/Q Mismatch and LO Phase Error

The analysis of the OFDM signal transmitted by a non-ideal transmitter yields I/Q mismatch and LO phase error of the transmitter when captured and demodulated by a golden receiver. In our test methods, since we are utilizing both transmitter and the receiver at the same time to obtain the signal path from transmitter inputs to receiver outputs, the analysis of the OFDM or any other prospective baseband modulation signals have to be investigated mathematically in the case of a receiver with impairments.

The result of the baseband modulated data analysis can be used to assist the solver for faster convergence or it can be used to extend the parameter list of the transceiver, if the investigation yields separation of transmitter and receiver impairments.

7.2.2 Predistortion and Time Delay for Better Convergence

The loop-back based BiST method proposed for generic baseband modulation schemes exhibits a fragile convergence behavior for some particular impairment parameter

sets. Our investigations yields a strong dependence on the time delay parameter that is the time delay of the loop-back path. However, the 2x-site test method, which is obtained by modifying the loop-back test method for the new test setup, does not experience this behavior. The time dependent mapping of the transceiver between the input/output test signals creates a linearly independent equation system that leads to better convergence behavior for the impairment parameters.

Artificially injecting this time dependency behavior to the transmitter signals may improve the convergence behavior of the proposed BiST method. This approach may be implemented simply by multiplying test signals with time varying functions before entering the transmitter. Moreover, an adjustable test feature of the loop-back path time delay may also improve convergence since we have observed better convergence behavior for particular time delays. The relation between the loop-back time delay and convergence, which we believe to be dependent on system parameters, such as carrier frequency, can be used to improve the BiST method.

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Biography

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Personal Data

Date of birth: May 10, 1979
Place of birth: Istanbul, Turkey.

Education

Doctor of Philosophy, Duke University, USA, expected 2010
Master of Science, Duke University, USA, 2006
Master of Science, Bogazici University, Turkey, 2004
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Publications

- **Refereed Conference Papers**

1. E.S. Erdogan and S. Ozev, "A Packet Based 2x-Site Test Solution for GSM Transceivers with Limited Tester Resources", *Proc. IEEE VLSI Test Symposium 2009 (VTS)* [64]

2. E.S. Erdogan and S. Ozev, "Single-Measurement Diagnostic Test Method for Parametric Faults of I/Q Modulating RF Transceivers", *Proc. IEEE VLSI Test Symposium 2008 (VTS)* [63]

*3. E.S. Erdogan, S. Ozev and L.M. Collins, "Online SNR Detection for Dynamic Power Management in Wireless Ad-Hoc Networks", *Proc. PhD Research in Microelectronics and Electronics 2008 (PRIME)* [68]

*4. E.S. Erdogan, S. Ozev and P. Cauvet, "Diagnosis of Assembly Failures for System-in-Package RF Tuners", *Proc. IEEE Int. Symposium on Circuits and Systems 2008 (ISCAS)* [69]

5. E.S. Erdogan and S. Ozev, "An ADC-BiST Scheme Using Sequential Code Analysis", *Proc. IEEE Design Automation and Test 2007 (DATE)* [70]

6. E.S. Erdogan and S. Ozev, "A Robust, Self-Tuning Circuit for Built-in Go/No-Go Testing of Synthesizer Phase Noise", *Proc. IEEE International Test Conference 2006 (ITC)* [71]

- **Refereed Journal Papers**

1. E.S. Erdogan and S. Ozev, "Detailed Characterization of Transceiver Parameters Through Loop-Back-Based BiST", *Trans. IEEE Very Large Scale Integration 2009 (TVLSI)* [65]

*2. E.S. Erdogan, R.O. Topaloglu, O. Cicekoglu, H. Kuntman and A. Morgul, "Novel Multiple Function Analog Filter Structures and A Dual-mode Multifunction Filter", *International Journal of Electronics 2006 (IJE)* [72]

*3. E.S. Erdogan, R.O. Topaloglu, O. Cicekoglu and H. Kuntman, "New Current-mode Special Function Continuous Time Active Filters Employing Only OTAS and Opamps Design", *International Journal of Electronics 2004 (IJE)* [73]

- **Workshop Presentations**

1. E.S. Erdogan and S. Ozev, "An Integrated BiST Solution for I/Q Modulation RF Transceivers", in Wireless Test Workshop 2008

2. E. S. Erdogan and S. Ozev, "Wafer Level Loop-Back Test with Out-of-Band Signals", in IEEE North Atlantic Test Workshop 2007

*3. E. S. Erdogan and S. Ozev, "SiP: Test and Diagnosis Challenges for RF Components", in European Microwave Week RF System-in-Package Workshop 2005

Professional Activities

- IEEE student member
- Served as a reviewer for the IEEE Transactions on VLSI, International Test Conference, VLSI Test Symposium, Design Automation and Test Conference, European Test Symposium.

Work Experience

- LitePoint, Sunnyvale, CA – Advanced Technology – RF System Engineer 1, March 2010 - Present
- LitePoint, Sunnyvale, CA – Applications – Coop Engineer Jun 2009 - Sep 2009

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- Philips Semiconductors, France – SiP Test – Internship Jun 2006 - Aug 2006
- Philips Semiconductors, France – SiP Test – Internship Jun 2005 - Aug 2005
- Duke University, Durham, NC – Research Assistant, Aug 2004 - Mar 2010
- Bogazici University, Turkey – Teaching Assistant, May 2001 - Aug 204
- Profilo Telra, Turkey, – Internship Jan 2001 - Feb 2001
- Siemens Corp., Turkey, – Internship Aug 2000 - Sep 2000
- NCR IT, Turkey, – Internship Jan 2000 - Feb 2000

[0] *Not related to Ph.D. thesis work.