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Advances in electronic systems have lead to the demand for high resolution, high bandwidth Analog-to-Digital Converters (ADCs). Oversampled ADCs are well-known for high accuracy applications since they benefit from noise shaping and they usually do not need highly accurate components. However, as a consequence of oversampling, they have limited signal bandwidth. The signal bandwidth (BW) of oversampled ADCs can be increased either by increasing the sampling rate or reducing the oversampling ratio (OSR). Reducing OSR is a more promising method for increasing the BW, since the sampling speed is usually limited by the technology. The advantageous properties (e.g. low in-band quantization, relaxed accuracy requirements of components) of oversampled ADCs are usually diminished at lower OSRs and preserving these properties requires complicated and power hungry architectures.

In this thesis, different combinations of delta-sigma and pipelined ADCs are explored and new techniques for designing oversampled ADCs are proposed. A Hybrid Delta-Sigma/Pipelined (HDSP) ADC is presented. This ADC uses a pipelined ADC as the quantizer of a single-loop delta-sigma modulator and benefits from

the aggressive quantization of the pipelined quantizer at low OSRs. A Noise-Shaped Pipelined ADC is proposed which exploits a delta-sigma modulator as the sub-ADC of a pipeline stage to reduce the sensitivity to the analog imperfection. Three prototype ADCs were fabricated in 0.18μm CMOS technology to verify the effectiveness of the proposed techniques. The performance of these architectures is among the best reported for high bandwidth oversampled ADCs.

Design of Low OSR, High Precision Analog-to-Digital Converters

by

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Omid Rajaee, Author

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All praise belongs to God, the Compassionate, the Merciful

To my dearest parents for their unconditional sacrifice and support

&

To my treasured wife, Azadeh, for her endless love and kindness

CHAPTER 1. INTRODUCTION

1.1 Motivation

In the past two decades, many applications have replaced much analog circuitry with their digital counterparts. However, analog circuit design is still required for many applications like digitizing physical signals. In addition, recent advances in communication and electronics systems have lead to the demand for high speed and power efficient analog front-ends. Even though the analog circuitry usually occupies only small portion of the large systems, it may determine the performance of the overall system. For instance, inaccurate digitization of physical signals can result in the failure of a digital signal processing system.

Among analog front-end circuits, Analog-to-Digital converters (ADCs) play a crucial role in the performance of the communication systems. New applications continue to appear in which ADCs with higher bandwidths and higher resolutions are required. ADCs are divided in two categories: Nyquist rate and oversampled ADCs.

Nyquist rate ADCs (e.g. Pipelined [1], SAR [2], Folding ADCs [3]) are widely known for high-bandwidth medium-accuracy conversions. Although these architectures enable high-bandwidth implementation, high accuracy is difficult to achieve without extensive calibration. The performance of Nyquist ADCs is usually limited to the component mismatch, low device intrinsic gain, low input signal swing range and etc. This problem is growing more severe at the scaled CMOS technologies.

In contrast, oversampled ADCs are commonly used in the high-accuracy, low-to-medium bandwidth applications. Delta-Sigma ($\Delta\Sigma$) modulators are the most popular oversampled ADCs. The $\Delta\Sigma$ architecture had its origins in the early development phases of pulse code modulation (PCM) systems [4]. Although the basic $\Delta\Sigma$ ADC architecture had been well known since the 1950s and 1960s [5]-[7], the first actual commercial $\Delta\Sigma$ ADC was offered in 1988 by Crystal Semiconductor used for voice-band digitization. The digital audio market generated a demand for $\Delta\Sigma$ ADCs with higher bandwidths and greater resolution. CMOS $\Delta\Sigma$ ADCs became the architecture of choice for measurement, voice-band, and audio ADCs in the late 1980s and early 1990s [8],[9]. The data converter trends that started in the 1990s have continued into the 2000s. Power dissipation has dropped, and along with it, power supply voltages. Supplies of 5V, 3.3V, 2.5V, and 1.8V have followed as CMOS line spacings shrank to 0.6μm, 0.35μm, 0.25μm, and 0.18μm.

In the past decade, different techniques are employed to make the $\Delta\Sigma$ modulators viable candidate for applications with up to 20MHz signal bandwidth and more than 12-Bits resolution. Most of efforts were toward increasing the sampling rate of $\Delta\Sigma$ ADCs to increase the signal bandwidth as well. Although, the sampling rate is usually limited by the technology, continuous $\Delta\Sigma$ loop filters can alleviate the sampling rate limitation significantly [11]-[12]. The theoretical limit on the clock rate of a CT modulator is determined by the regeneration time of the quantizer and the update rate of the front-end DAC [10]. However, the inferior linearity and accuracy of CT loop filters makes them less attractive for high resolution application. On the other hand, Discrete Time (DT) $\Delta\Sigma$s exhibit both good linearity and good accuracy, but their sampling rate is usually limited by the opamp settling requirement. Hence, alternative techniques are required to increase the signal bandwidth of oversampled ADCs and preserve their accuracy.

1.2 Contribution

In this work, new oversampled ADCs were developed that achieve high precision at low oversampling ratios with minimal design complexity and with reduced sensitivity to the analog imperfections. These architectures include:

a) A Hybrid Delta-Sigma Pipelined (HDSP) ADC which exploits a pipelined ADC as the quantizer of a single-loop modulator and uses the latency of the pipelined quantizer to increase the order of noise shaping.

b) A Noise-Shaped Two-Step (NSTS) ADC which can be configured as a standalone ADC, as the quantizer of a single-loop modulator or the individual stage of a cascaded ADC. The NSTS ADC requires only one amplifier for multi-order (e.g. 3^{rd} order) noise shaping and two-step quantization.

c) A Noise-Shaped Pipelined ADC with reduced sensitivity to analog imperfections. This pipelined ADC requires only 9-bit linearity in the front-end stage for more than 13-bit accuracy.

1.3 Organization

This dissertation is organized as follows: Chapter 2 introduces the state-of-the-art high precision oversampled ADCs working at a low oversampling ratio (OSR). The proposed HDSP modulator is presented in chapter 3 and measurement results are provided. Chapter 4 proposes the NSTS ADC and its different configurations. The design and implementation of the proposed Noise-Shaped Pipelined ADC is studied in chapter 5. Finally, conclusions are given in chapter 6.

CHAPTER 2. HIGH BANDWIDTH, LOW OSR OVERSAMPLED ADCS

2.1 Introduction

An important challenge in design of $\Delta\Sigma$ modulators is to obtain higher bandwidth without a significant loss in accuracy. One approach for increasing the signal bandwidth (BW) of $\Delta\Sigma$ modulators is to reduce the OSR. At low OSRs, higher orders of noise shaping and higher number of quantization levels are required to preserve the high-accuracy advantage of the oversampled ADCs. However, higher order of noise shaping usually increases the signal swing at the internal nodes of the architecture and degrades the stability of the oversampled ADC. One way to improve the stability is to increase the number of the quantization levels. However, the number of quantization levels is limited by the design complexity.

Several techniques for designing high order and high resolution oversampled ADCs have been reported. In this chapter, state-of-the-art oversampled ADCs are briefly introduced. In section 2.2, high bandwidth single-loop $\Delta\Sigma$ modulators and their properties are presented. Cascaded modulators are studied in section 2.3. Section 2.4 describes oversampled pipelined ADCs and finally conclusions are given in 2.5.

2.2 High bandwidth single-loop $\Delta\Sigma$ modulators

Single-loop $\Delta\Sigma$ modulators are widely used in oversampling applications. They offer a potential low-power solution because of their relative low sensitivity to the integrator inaccuracies. However, they are usually used in the applications with low signal bandwidth and high oversampling ratios. In single-loop $\Delta\Sigma$ ADCs, in order to maintain the performance at a reduced OSR, it is necessary to reduce the in-band quantization noise density. Each additional quantizer bit improves the overall signal-to-quantization-noise ratio (SQNR) by 6 dB and also improves the modulator stability , which permits aggressive noise shaping. However, the number of quantization levels is limited by the front-end digital-to-analog converter (DAC) due to the increased burden in the dynamic element matching (DEM) circuitry. Furthermore, the power dissipation quickly becomes unmanageable because of the exponential increase in the complexity of the internal flash ADC.

The two-step flash quantizer architecture can potentially solve this problem. However, performing two-step quantization within a single-stage modulator is challenging because only one-half clock cycle quantizer delay is permitted for stability reasons [13], [32] and [14]. The architecture of the modulator with a two-step quantizer is shown in Fig. 2.1. The output signal of the loop filter is sampled and MSB-bits are resolved first. Later, the residue signal is generated, processed by the second stage and the LSB-bits are resolved. The whole operation is performed in a half-clock cycle. The half-clock cycle of the two-step quantizer can be merged with the transfer function of the loop filter to avoid any stability issue. This can be done by using half-delay integrators in the loop filter.

In this architecture, one can use the segmented DACs (MSB/LSB DACs) to greatly reduce the number of unit elements in the DAC. The quantization of the

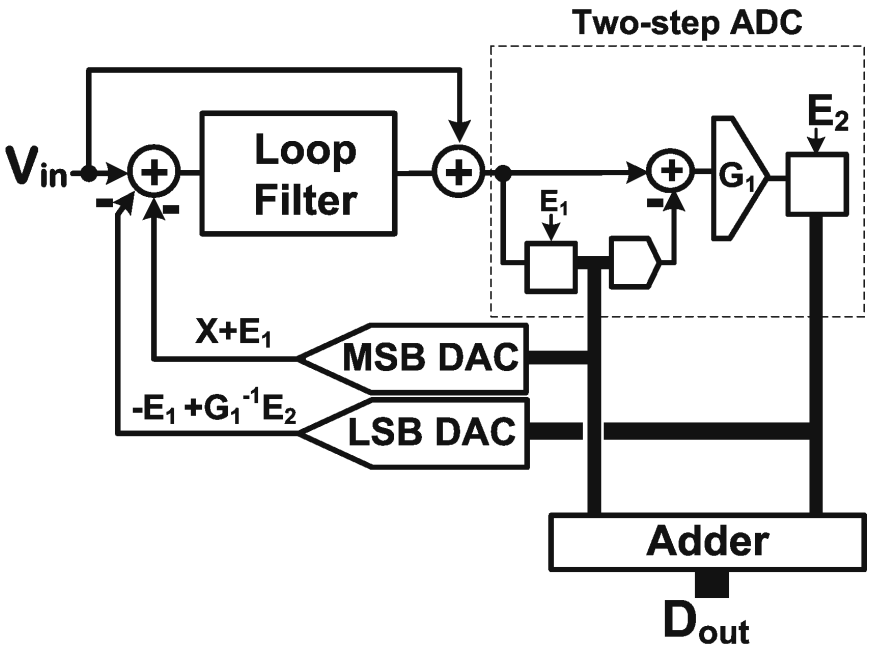

Figure 2.1: The single-loop $\Delta\Sigma$ ADC with Two-Step quantizer

first stage (E_1) appears at both the MSB and LSB output words and is canceled out at the input of the modulator. Any mismatch between LSB and MSB DACs causes quantization noise leakage and severe accuracy degradation. The leakage problem can be alliviated by combining and reallocating MSB and LSB bits with a digital $\Delta\Sigma$ modulator as shown in Fig. 2.2. The MSB and LSB bits are first concatenated to form an N-bit signal. This signal is then requantized to N_C-bits using a digital $\Delta\Sigma$ modulator. The MSB signal is then subtracted from the original N-bits signal to form a new LSB signal with $N_F + 1$-bits. After requantization, the new MSB and LSB bits are

$$Y_C = Y(z) + Q_C(1 - z^{-1}) \tag{2.1}$$

$$Y_F = -Q_C(1 - z^{-1}) \tag{2.2}$$

Signals Y_C and Y_F then pass through the independent DACs and are summed at

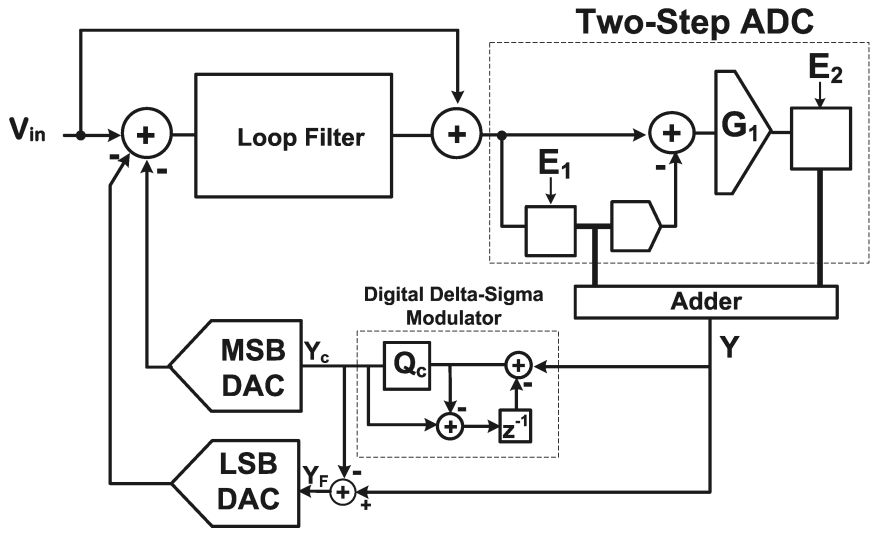

Figure 2.2: The single-loop $\Delta\Sigma$ ADC with Two-Step quantizer and mismatch correction scheme

the input of the modulator. The leakage noise component due to the DAC gain mismatch gets shaped by the order of the loop filter. This methods requires extra hardware and increases the latency of two-step quantization further. Although employing a two-step quantizer in $\Delta\Sigma$ modulators provides aggressive quantization and noise shaping properties, the latency of two-step quantization and the difficulty of leakage cancellation make this approach less attractive for high accuracy, high bandwidth applications.

2.3 Cascaded $\Delta\Sigma$ modulators

One useful technique for reducing the quantization noise power is cascading several stages of processing. In a cascaded ADC, the quantization errors in each stage are processed by the following stage. Outputs of the stages are combined to cancel the quantization errors of all stages preceding the last stage. Cascading

is common to a broad class of ADCs, including pipelined ADCs and MASH $\Delta\Sigma$ modulators. MASH converters use a cascade of $\Delta\Sigma$ modulator loops to increase the order of the noise shaping without degrading the stability of the individual stages.

2.3.1 Cascaded $\Delta\Sigma$-pipelined ADC

Pipelined converters use a cascade of quantizers to increase the overall resolution without increasing the complexity of the individual quantizers. One can cascade a $\Delta\Sigma$ modulator with a pipelined ADC to reduce the in-band quantization noise and achieve high SQNR at a low oversampling ratio. The cascaded $\Delta\Sigma$-pipelined ADC,[44], [15] and [16], is shown in Fig. 2.3.

In this architecture, the quantization noise of the $\Delta\Sigma$ modulator is extracted and processed by a high resolution pipelined ADC. In low distortion $\Delta\Sigma$ modulator with feed-forward, the quantization noise is available at the output of the loop filter and it can be directly processed by the pipelined ADC. A problem common to all types of the cascaded ADC architectures is that analog signal processing operations in early stages of the converter must be accurately known in order to cancel the quantizer errors. Any mismatch between digital NTF and NTF of the front-end stage causes quantization noise leakage and degrades the overall accuracy. Hence, high gain amplifiers and closely matched capacitors are required in the front-end stage to alleviate this problem. This analog/digital NTF mismatch issue can also be addressed by digital calibration. However, the digital calibration circuitry is usually power hungry.

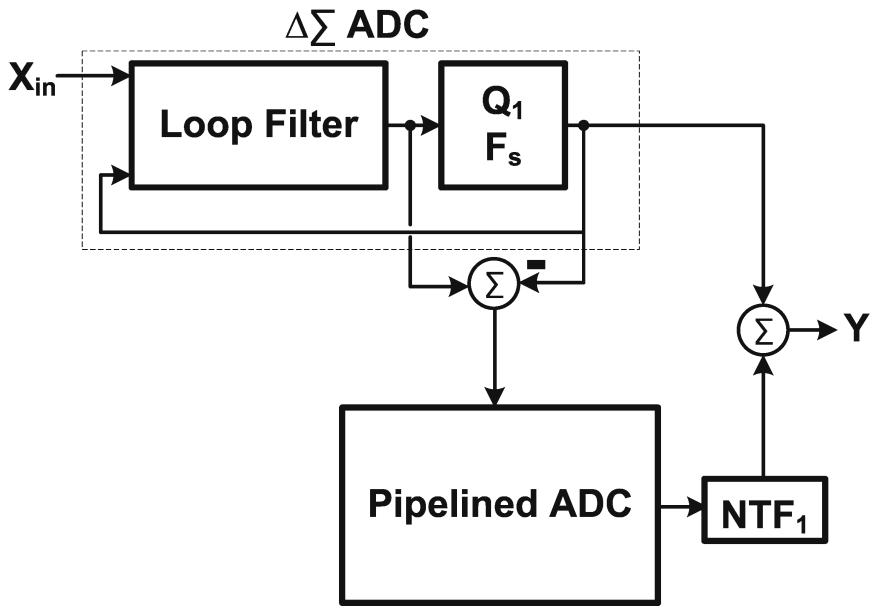

Figure 2.3: The cascaded ΔΣ-pipelined ADC

2.3.2 0-N MASH ΔΣ modulator

The popularity of the MASH for low OSR stems from the improvement in the achievable SQNR when compared to the single-loop topologies. The SQNR advantage is due to high order of noise shaping and aggressive quantization of the sampled signal. Two well-known configurations of the MASH topology (ΔΣ-ΔΣ MASH and ΔΣ-0 MASH) demonstrate this property. The missing piece of the MASH topology, 0-ΔΣ, is recently reported in [41]. The 0-ΔΣ preserves the SQNR advantage of the MASH topology. However, it is found that the 0-ΔΣ MASH is stable for a larger input-signal level than any traditional topology and it can achieve a higher Dynamic Range (DR), if the inter-stage gain is scaled properly.

The 0-ΔΣ modulator is shown in Fig. 2.4. The two stage example is used for

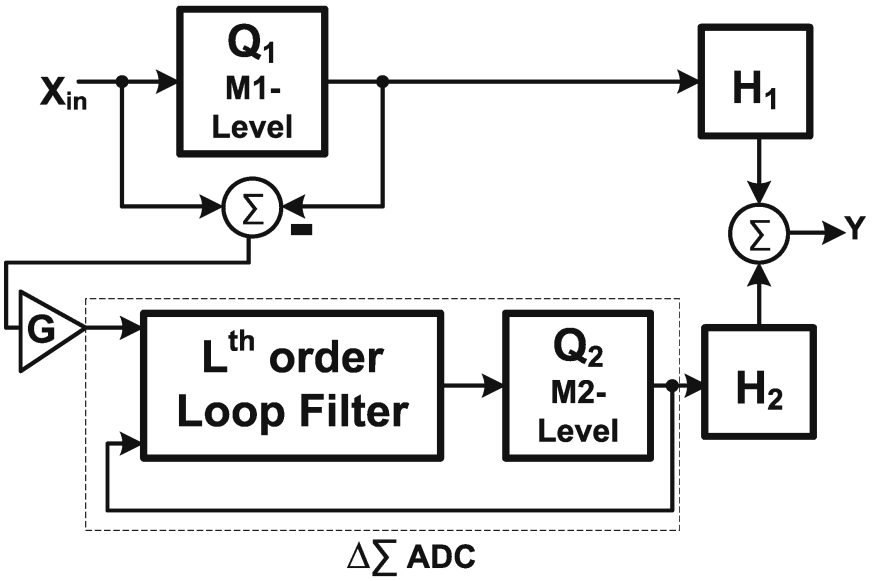

Figure 2.4: The 0-$\Delta\Sigma$ MASH modulator

simplicity but the results are nonetheless applicable to the higher-order cascading. The first-stage is the zero-order quantizer. The second stage is an L^{th} order single-loop $\Delta\Sigma$ modulator. In addition, there are two digital filters, H_1 and H_2, that process the digital code to generate the finaloutput Y from the 0-L MASH. The quantization of the first stage (Q_1) is fed to a $\Delta\Sigma$ modulator in the second stage after an optional inter-stage gain. The output from both stages is processed in the digital domain to obtain the final output Y.

In this architecture, the overall input signal range can be considerably increased by reducing the inter-stage gain (G). Reducing G extends the redundancy between the two stages and as a result, the proposed modulator can process input signals higher than reference voltage. The first quantizer (Q_1) chops off the over full-range signal and the $\Delta\Sigma$ modulator sees a fraction of the input signal. However, this extra signal does not overload the second stage (since G is reduced), but it is quantized. In other words, the redundancy between stages absorbs the over

full-range input signal. The maximum over full-range signal depends on G.

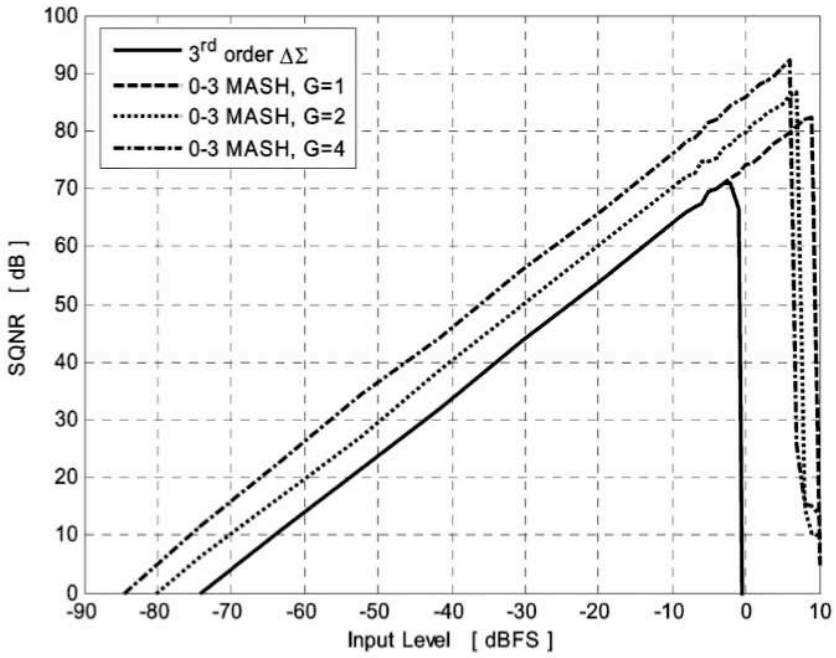

Figure 2.5: The SNDR plot of 0-3 MASH modulator with various inter-stage gains (1,2 and 4)

A design example is shown in Fig. 2.5. For a 0-3 MASH modulator with the inter-stage gain of 1, the maximum input signal can be as high as 9 dB full scale which is 3.5 time higher than a 3^{rd} single-loop $\Delta\Sigma$ modulator. As G increases, the magnitude of the maximum over full-range signal is reduced, but the peak SQNR is improved. The quantization noise of the second stage is scaled by the inter-stage gain. Hence, increasing G suppresses the overall quantization power and improves SQNR. The trade-off between the peak SQNR and maximum over full-range input signal is the main drawback of the 0-$\Delta\Sigma$ MASH topology.

2.3.3 Multi-rate MASH modulator

In the MASH topology, the first stage is the main contributor in the overall power consumption. The main idea behind the multi-rate MASH modulators, [17]-[21], is to reduce the sampling rate of the first stage to decrease its power consumption and compensate the resulting loss in resolution by increasing the sample rate of the back-end stage. The back-end stage has relaxed design requirements and its power consumption is not significant even at higher sampling rates.

The system-level architecture of the multi-rate cascaded modulator is shown in Fig. 2.6. The cascaded structure consists of a first stage operating at a sampling frequency of F_1, an upsampler with an integer up-sampling factor N and a second stage operating at a sampling frequency of $F_2 = N.F_1$. The digital output streams of both stages are recombined within the digital cancellation logic that, ideally, eliminates the quantization noise of the first stage. This recombination can be done at two different rates: either the output of the first stage is up-sampled or the output of the second stage is down-sampled. The transfer function of multi-rate 1-1 MASH is as following

$$D_1 = X_{in} + (1 - z^{-1})E_1 \tag{2.3}$$

$$D_2 = -H_{F1}E_1 + (1 - z^{-\frac{1}{N}})E_2 \tag{2.4}$$

$$Y = D_1H_{F1} + (1 - z^{-1})D_2 = H_{F1}X_{in} + (1 - z^{-1})(1 - z^{-\frac{1}{N}})E_2 \tag{2.5}$$

D_1, D_2 and Y are the digital outputs of the first stage, the second stage and the final output respectively. H_{F1} is the transfer function of the up-sampler

$$H_{F1} = \frac{(1 + z^{-1} + ... + z^{-N})}{N + 1} \tag{2.6}$$

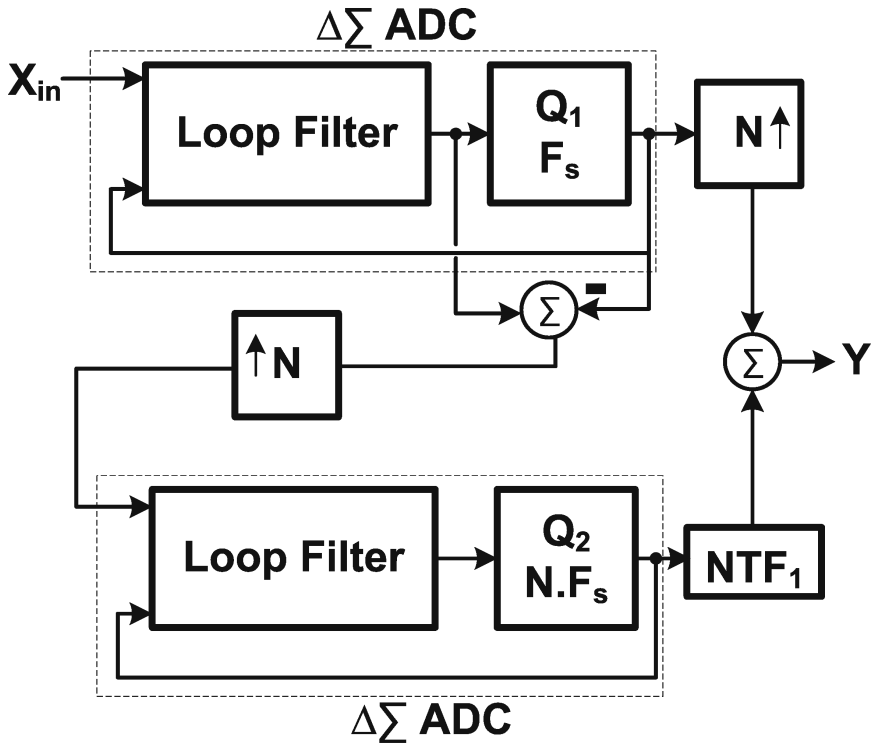

Figure 2.6: The multi-rate MASH modulator

The $(1 - z^{-\frac{1}{N}})$ term of the final noise transfer function provides much more aggressive noise shaping compared to original $(1 - z^{-1})$ transfer function. This allows achieving higher bandwidth without running the first stage at higher frequencies. This topology is a good candidate for low OSR applications. However, it still suffers from quantization noise leakage similar to the traditional MASH modulators.

2.4 Oversampled pipelined ADC

At very low OSRs, the benefits of the $\Delta\Sigma$ modulation tend to disappear. Low-OSR $\Delta\Sigma$ ADCs have complex architectures and are usually prone to com-

ponent mismatch. An alternative method to achieve high resolution at low OSRs is to over-sample a pipelined ADC. The pipelined ADC provide a robust method for resolving a large number of bits. However, its performance is limited to the capacitor mismatch, the opamp gain error and the settling error. An oversampled pipelined ADC is introduced in [22] and [23]. This architecture solves the capacitor mismatch problem at low OSRs by exploiting mismatch shaping.

In the single-bit pipeline flip-around gain stage, the input signal is first sampled on two capacitors. Later in the amplification phase, one of the capacitors operate as the flip-around feedback capacitor and the others is connected between the DAC reference voltages and the input of the amplifier. The charge sampled on this capacitor is transferred to the feedback capacitor. Any mismatch between these two capacitors makes the inter-stage gain inaccurate and causes harmonic distortion. In an oversampled pipelined ADC, this problem can be simply addressed by swapping capacitors C_1 and C_2 in the alternate clock phases. In one amplification phase, C_1 is the feedback capacitor and in the succeeding phase C_2 is the feedback capacitor. This scheme is shown in Fig. 2.7 versus traditional flip-around architecture. Assuming $C_1 = C_2 + C_\alpha$, the inter-stage gain error in one clock cycle is $\frac{C_\alpha}{C_2}$ and in the succeeding clock cycle is almost $-\frac{C_\alpha}{C_2}$. Hence, the average mismatch error of two phases is $0.5\frac{C_\alpha}{C_2}(1-z^{-1})$ which is first order shaped.

This method addresses only the capacitor mismatch issue in the oversampled pipelined ADC. Other sources of distortion (e.g. opamp gain error, settling accuracy) remain untouched. Furthermore, a high number of pipelined stages are required to suppress the final quantization error and this increases the power consumption significantly. Generalizing this method to the multi-bit pipeline MDACs is also difficult.

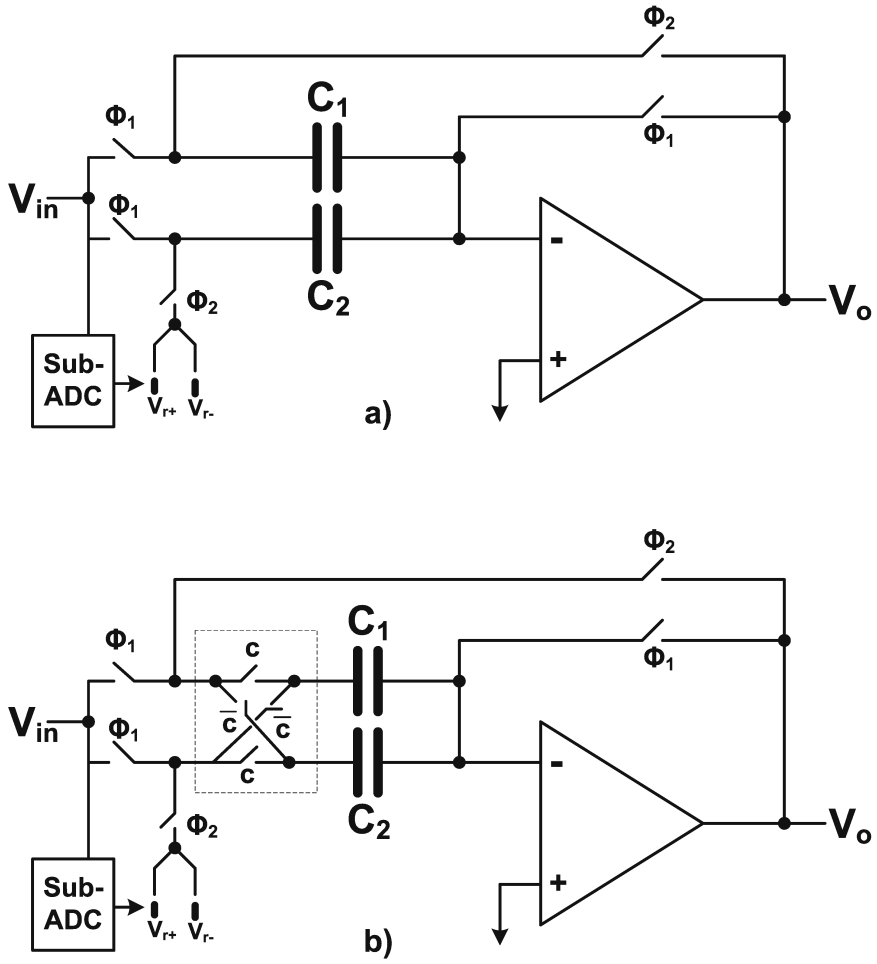

Figure 2.7: a) Traditional flip-around pipeline MDAC b) The flip-around pipeline MDAC with mismatch shaping scheme

2.5 Conclusions

In this chapter, the conventional methods for reducing OSR and increasing the signal bandwidth of oversampled ADCs are studied. The common problem of all these architectures are the design complexity and the sensitivity to the analog imperfections. At low OSRs, oversampled ADCs usually use multi-step quantization and integration and consequently they are prone to quantization noise leakage

and the component mismatch. The main challenge in low OSR applications is to keep the design simple while increasing the order of noise shaping and the number of quantization levels.

CHAPTER 3. DESIGN OF A HYBRID DELTA-SIGMA/PIPELINED ADC

3.1 Introduction

The salient constraint in design of low-OSR $\Delta\Sigma$ ADCs is increasing the number of quantization levels and keeping the design simple. The hybrid Delta-Sigma/pipelined (HDSP) modulator presented in this chapter employs a pipelined ADC as a quantizer of a single-loop DSM. This offers the possibility of improving the accuracy without imposing stringent design requirements on either the loop filter or the feedback DAC. Furthermore, the delay of the pipelined ADC is not only resolved but it is also used to increase the order of noise shaping. Hence, even very low-order loop filters are sufficient for most designs. Also, the DAC at the input of the modulator is only associated with the digital outputs of the first pipelined stage. Consequently, the number of the quantization levels could be increased without increasing the number of elements of this DAC.

This chapter is organized as follows: In section 3.2, a general concept of the HDSP modulator is studied. Design requirements of the proposed structure is presented in section 3.3. In section 4.4, the design of third order HDSP modulator is discussed. Measurement results are provided in section 3.5 to validate the effectiveness of this structure. Finally, conclusions are given.

3.2 The proposed Hybrid Delta-Sigma/Pipelined (HDSP) modulator

Single-loop delta sigma ADCs are well-known for their relaxed loop filter design requirements. Accuracy of these modulators can be improved by increasing the number of quantization levels. Pipelined ADC architecture provides a power efficient way for realizing medium resolution ADCs, often ranging from 8 to 12 bits [27]-[30], and it has the potential to replace the high resolution quantizer in the $\Delta\Sigma$ ADCs. The use of the pipelined ADC as a quantizer of a single-loop DSM is illustrated in Fig. 3.1 where the low distortion topology is used as the loop filter [31]. The pipelined ADC quantizes the output signal of the loop filter. The digital outputs of the quantizer are converted to the analog voltage by the feedback DAC at the input of the loop filter. The pipelined quantizer allows aggressive quantization of the input signal and increases the SQNR accordingly. However, the modulator architecture shown in Fig. 3.1 has two practical problems. First, the large number of the unit elements required in the feedback DAC will degrade the linearity of the DSM. Thus a complex dynamic element matching (DEM) circuity is required. Second, the latency of the pipelined quantizer degrades the noise-shaping of the DSM. These problems will be explored and solutions will be provided in the following.

3.2.1 Simplification of the feedback DAC

In the regular single-loop DSMs, all the digital outputs of the quantizer are fed back to the input of the modulator. This feedback carries the input signal of the quantizer and the added quantization noise (X and Q in Fig. 3.1). However, in

case of the pipelined quantization, the final digital output is the weighted sum of the digital outputs of the pipelined stages. These digital outputs can be fed back either by using the unit element or the segmented DAC [32]. The unit element DAC requires 2^B elements where B is the number of the output bits. This may not be practical when more than 6-bits quantization is used due to the minimum unit element size. On the other hand, the segmented DAC suffers from the gain mismatch between the segments [32].

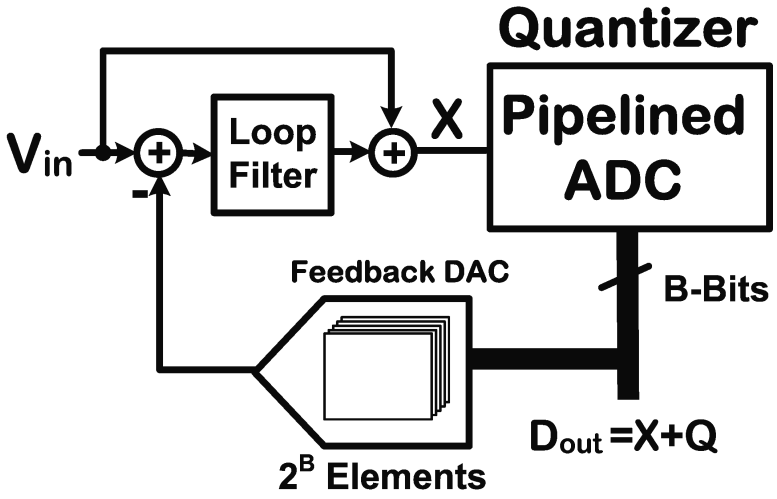

Figure 3.1: A potential/problematic DSM with a pipelined ADC as quantizer

One way to simplify the feedback DAC is to generate the signal information provided by this path (i.e. X and Q) differently. It should be noted that in an ideal pipelined ADC, only the scaled quantization noise of the last stage (Q) appears at the output; the quantization noise from all the preceding stages are canceled out. The last stage of the pipelined ADC is usually a flash sub-ADC. Its quantization noise (Q) can be easily extracted in the analog form by adding a multiplying-DAC (MDAC) as shown in Fig. 3.2. The extracted quantization noise, along with the digital output and the residue of the first stage, can be used to replace the complex

feedback DAC.

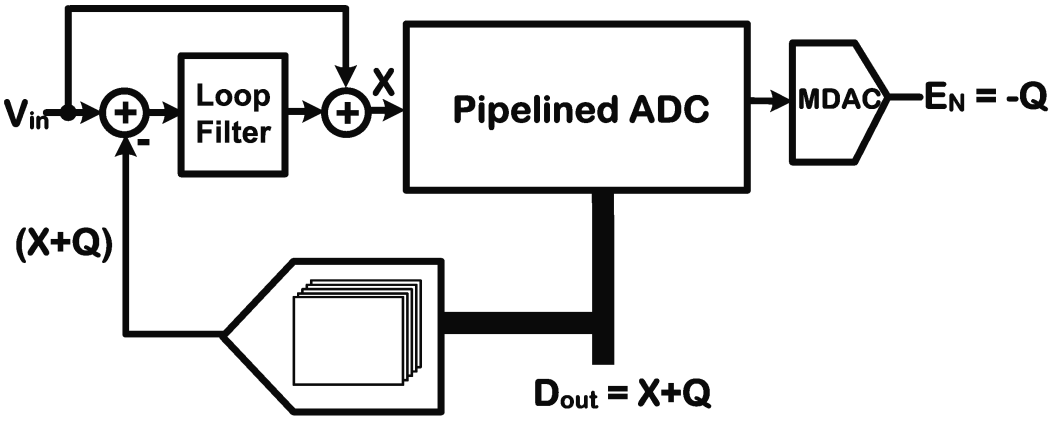

Figure 3.2: Extracting the pipelined quantization noise Q in analog form

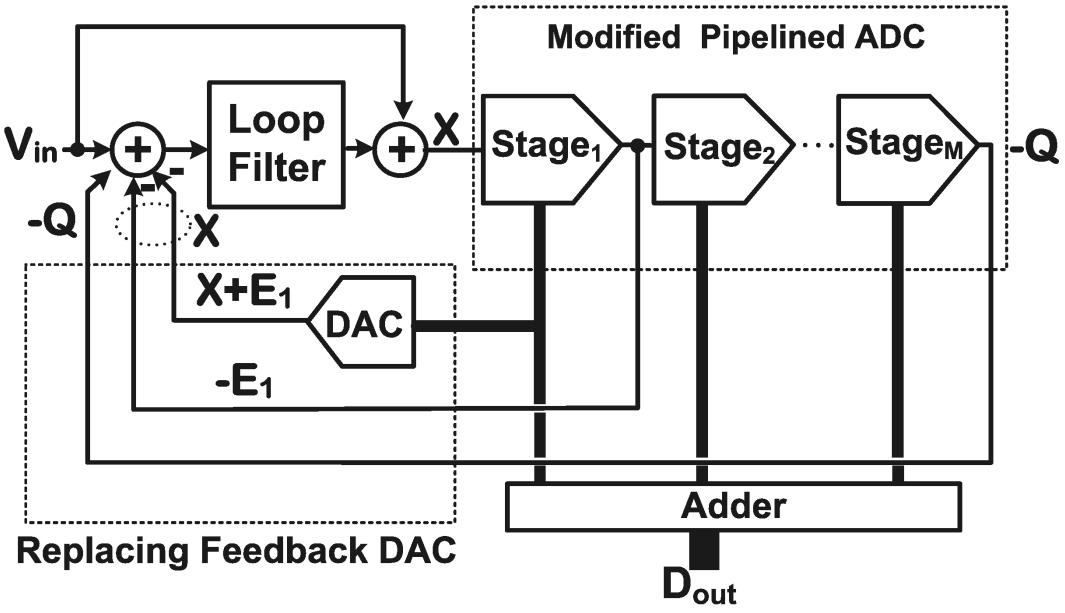

Figure 3.3: Replacing the feedback DAC in DSM with a pipelined ADC as quantizer

The modified version of the $\Delta\Sigma$ ADC with an M-stage pipelined quantizer is illustrated in Fig. 3.3. The feedback DAC in Fig. 3.1 is replaced with three feedback paths; one from the digital outputs of the first pipelined stage, another from the analog residue of the first stage, and the third from the analog residue of

the last pipelined stage.

The feedback path from the digital outputs of the first stage provides the input signal of the pipelined ADC (X) and the quantization noise of the first stage (E_1). E_1 is also available as the analog residue of the first stage and is used to cancel out the unwanted E_1 in the DAC path. Finally, the analog residue of the last stage provides Q. The combined signal provided by these three feedback paths together ($X+Q$) is the same as the signal provided by the complex feedback DAC of Fig. 3.1. The required gain scaling for the residue voltages in the feedback paths are not shown for the sake of simplicity.

The DAC at the input of the modulator needs to convert only the digital outputs of the first stage of the pipelined ADC (only MSBs), while the modulator benefits from processing the small quantization error of the entire pipelined ADC. For instance, if an 8-bit pipelined ADC resolving 2-bits in the first stage is used, the feedback DAC of the modulator is only 2-bits, while the modulator loop processes the quantization error of an 8-bit ADC.

3.2.2 Solving the pipelined ADC latency issue

If the latency of the pipelined ADC shown in Fig. 3.1 and Fig. 3.3 is assumed to be zero, the input of the pipelined ADC (X) can be written as

$$X = V_{in} + (NTF_L - 1)Q \tag{3.1}$$

where NTF_L is the high-pass noise transfer function of the loop filter. NTF_L is an L^{th} order polynomial with L zeros either at DC or in the signal bandwidth and can be expressed as (e.g. zeros at DC)

$$NTF_L = (1 - z^{-1})^L. \tag{3.2}$$

The output of the pipelined ADC (D_{out}) can therefore be rewritten as

$$D_{out} = X + Q = V_{in} + NTF_L Q. \tag{3.3}$$

The above equation shows that the overall noise transfer function of DSM is solely determined by the loop filter. However, when the pipelined ADC latency is considered, the overall NTF is modified. As illustrated in Fig. 3.4, each stage of the pipelined ADC introduces half a clock cycle delay. For proper operation of the pipelined ADC, the digital outputs of each stage are delayed, until the last quantization is complete, and then combined. The output signal of the ADC considering this effect is

$$\begin{aligned} D_{out} &= Xz^{-N} + Q \\ &= V_{in}z^{-N} + \Big[(NTF_L - 1)z^{-N} + 1\Big]Q \end{aligned} \tag{3.4}$$

modifying the overall NTF to

$$NTF_{modified} = (NTF_L - 1)z^{-N} + 1 \tag{3.5}$$

where N represents the number of the full delays introduced by the pipelined ADC. The overall noise transfer function, $NTF_{modified}$, is converted to a higher order polynomial. Consequently, the location of some (or all) zeros is changed and the quantization noise is not shaped properly. This delay may even cause instability.

The delay problem can be solved by converting the $NTF_{modified}$ polynomial to a high-pass filter with all zeros either at DC or in the signal bandwidth. This can be done by adding some additional delay terms to the $NTF_{modified}$.

$$H = A_1 z^{-1} + A_2 z^{-2} + ... \tag{3.6}$$

$$NTF_{new} = (NTF_L - 1)z^{-N} + 1 + H = (1 - z^{-1})^{L+N} \tag{3.7}$$

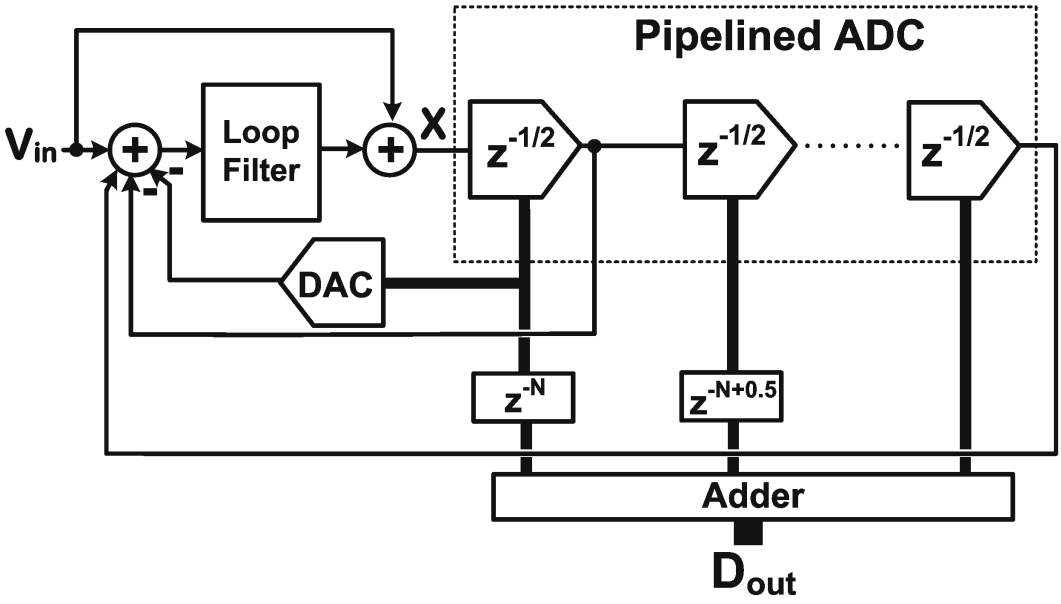

Figure 3.4: Latency in the $\Delta\Sigma$ modulator with a pipelined ADC as quantizer

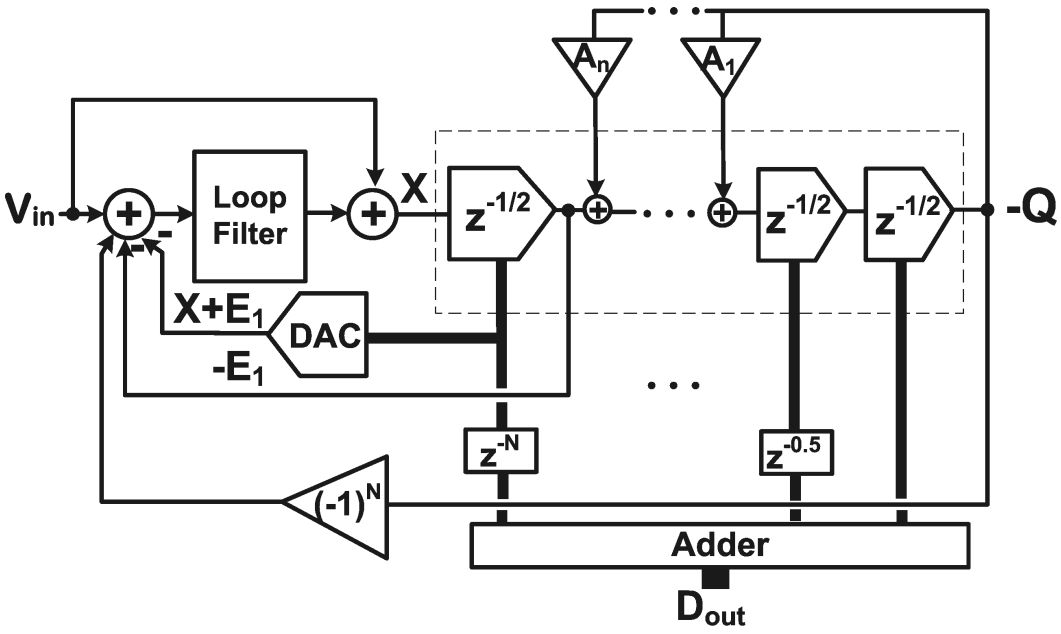

Figure 3.5: The proposed Hybrid Delta-Sigma/Pipelined (HDSP) Modulator

here H denotes the additional polynomial terms needed for obtaining the desired high-pass noise transfer function (NTF_{new}). The order of NTF_{new} is $N + L$, indicating that the latency of the pipelined ADC is used to increase the order of noise shaping. This concept can be explained clearly with an example. In an HDSP modulator with a second order loop filter ($NTF_L = (1 - z^{-1})^2$), if two full delays are generated in the pipelined ADC ($N = 2$), the overall NTF will be changed to

$$NTF_{modified} = (NTF_L - 1)z^{-2} + 1 = z^{-4} - 2z^{-3} + 1. \tag{3.8}$$

The modified NTF can be converted to a full fourth order high-pass NTF by adding $H = A_1z^{-1} + A_2z^{-2} + A_3z^{-3}$ to it.

$$NTF_{new} = z^{-4} + (A_3 - 2)z^{-3} + A_2z^{-2} + A_1z^{-1} + 1 = (1 - z^{-1})^4 \tag{3.9}$$

for $A_1 = -4$, $A_2 = 6$ and $A_3 = -2$.

Lets consider the case when an odd N is generated in the pipelined ADC. For $N = 1$ and a second order loop filter, the $NTF_{modified}$ will be

$$NTF_{modified} = (NTF_L - 1)z^{-1} + 1 = z^{-3} - 2z^{-2} + 1. \tag{3.10}$$

For converting the modified NTF to a full second order high-pass NTF, an $H = A_1z^{-1} + A_2z^{-2}$ is required and the polarity of z^{-3} and z^{-2} terms should also be changed.

$$NTF_{new} = -z^{-3} + (A_2 + 2)z^{-2} + A_1z^{-1} + 1 = (1 - z^{-1})^3 \tag{3.11}$$

for $A_1 = -3$ and $A_2 = 1$. These examples show that equation (3.7) just holds for even Ns and it can be extended to odd Ns by changing the polarity of $z^{-(N+L)}$ term. The general NTF which works for both odd and even Ns can be expressed as

$$NTF_{new} = (NTF_L - 1)(-z)^{-N} + 1 + H = (1 - z^{-1})^{L+N}. \tag{3.12}$$

This technique is used to solve the pipelined ADC latency issue in the HDSP modulator as depicted in Fig. 3.5. The feedback from the residue of the last stage to the input of the loop filter is multiplied by $(-1)^N$ to ensure the correct noise transfer function for both odd and even number of delays. Since the quantization noise of the pipelined ADC (Q) is available in the analog form as the residue of the last MDAC, it can be used for generating the delayed terms desired in H. This is accomplished in the proposed modulator by feeding the last stage's residue (Q) back to the input of the preceding pipelined stages. The gain blocks $(A_1, .., A_n)$ in Fig. 4.18 provide the desired coefficients. The proposed HDSP architecture overcomes the latency by using it to enhance the order of noise shaping.

It should be noted that the derived noise transfer function is only for Q, since the quantization noise of all the preceding pipelined stages are ideally canceled in the digital output of the pipelined ADC.

3.3 Design requirements of the HDSP modulator

3.3.1 Digital and analog feedbacks

In the HDSP architecture, similar to the other $\Delta\Sigma$ modulators, the feedback DAC requires DEM if it resolves multi-bits.

The other feedbacks in the HDSP modulator are analog signals and can be realized easily. The two analog feedbacks to the input of the loop filter (Fig.3.5) can share capacitors with the feedback DAC, hence dedicated capacitors are not needed. This will help avoiding mismatch between the digital and the analog feedback paths from the first pipelined ADC stage. Mismatch between these paths can cause quantization noise (E_1) leakage which appears at the output unfiltered. The

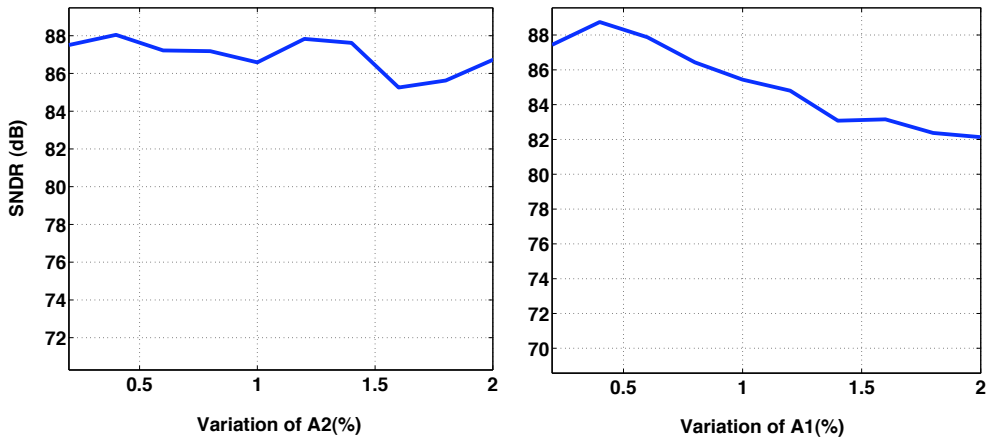

Figure 3.6: Sensitivity to the analog feedback coefficients, A_1 and A_2 in (3.11)

overall noise transfer function coefficients in the proposed architecture is determined by the analog feedbacks $(A_1, ..., A_n)$ from the last pipelined stage (Fig.3.5). Simulation results demonstrate that variations of these coefficients do not seriously affect the overall performance. These variations slightly change the location of the zeros in the NTF. Fig. 3.6 shows the effect of the variation of these coefficients on the overall SNDR of the HDSP modulator with a second order loop filter realizing third order NTF as described in (3.11). An 8-bit quantization is used in the pipelined ADC. Fig. 3.6 clearly shows that the overall SNDR only drops a few dBs for up to 2 percent variation in A_2 and A_1 coefficients. All these coefficients are determined by the capacitor ratios, and capacitor matching of 1-2 percent can be easily achieved in the modern CMOS process.

3.3.2 The loop filter

The HDSP modulator is inherently a single-loop modulator and hence, has relaxed DC gain requirements for the loop filter integrators. This is an important advantage of the HDSP architecture over the cascaded structures. In the cascaded DSMs, highly accurate analog transfer functions are needed to match the digital noise cancellation filters. But in the HDSP structure, no digital noise cancellation filters are used. Although the feedback DAC is only associated with the first

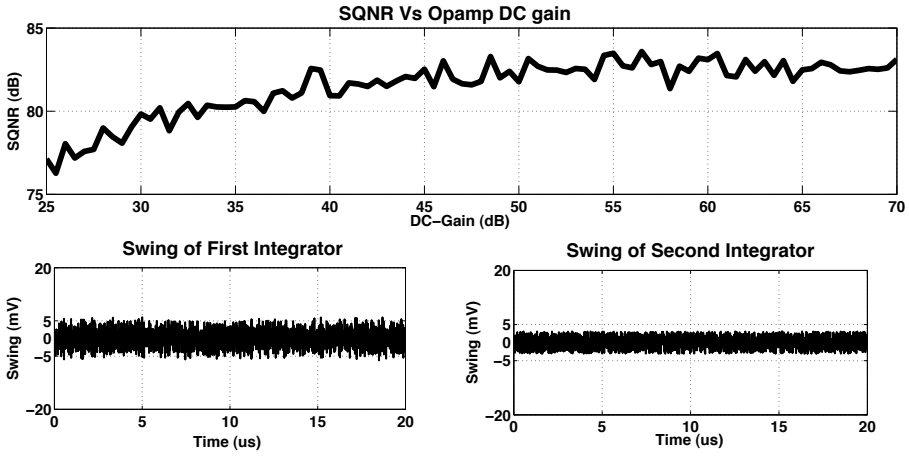

Figure 3.7: The gain and swing requirements of the loop filter integrators (Full scale = +/-800mV)

pipelined quantizer, the HDSP modulator benefits from processing the quantization error of the entire pipelined ADC. The reduced quantization noise prevents signal overload at the internal nodes of the modulator; the output of the integrators and the residue amplifiers. In the HDSP modulator with signal feed-forward, the integrators process only the quantization noise of the pipelined ADC, and as a result, the output swing of the integrators is just a few millivolts. This greatly relaxes the slewing requirements of the integrators.

The sensitivity of the HDSP modulator to the DC gain of the integrators is shown in Fig. 3.7. This simulation is performed for a third order HDSP modulator with the second order loop filter and an 8-bit pipelined quantizer. The overall SQNR changes only a few dBs when the first integrator DC gain varies between 25 to 70 dB. This small SQNR variation is due to the change in the location of the NTF zeros. Fig.3.7 also shows the output swing of the two integrators used in the loop filter. The output swing is less than 10 mV since the HDSP structure benefits from an 8-bit quantization error in the loop.

The relaxed design requirements of the loop filter in the HDSP modulator allows using very simple and fast integrators. This makes the HDSP modulator a potential choice for the high-speed/high-bandwidth applications.

3.3.3 The pipelined ADC

Non-idealities generated by the pipelined MDACs, including the DAC nonlinearity, the opamp gain error, and the capacitor mismatch, can affect the overall performance of the modulator and need careful consideration. Design requirements of the pipelined stages in the HDSP architecture is different from the regular pipelined ADCs.

In the HDSP architecture, the output residue of the first pipelined stage is fed back to the input of the loop filter. Consequently, any error from the first stage will be processed by the loop filter and shaped. This includes the DAC nonlinearities, the MDAC noise, the capacitor matching and the opamp linear/nonlinear gain error.

Fig. 3.8 shows the loop filter and the first two pipelined stages of the HDSP modulator. This block diagram can be used for deriving an expression for the first

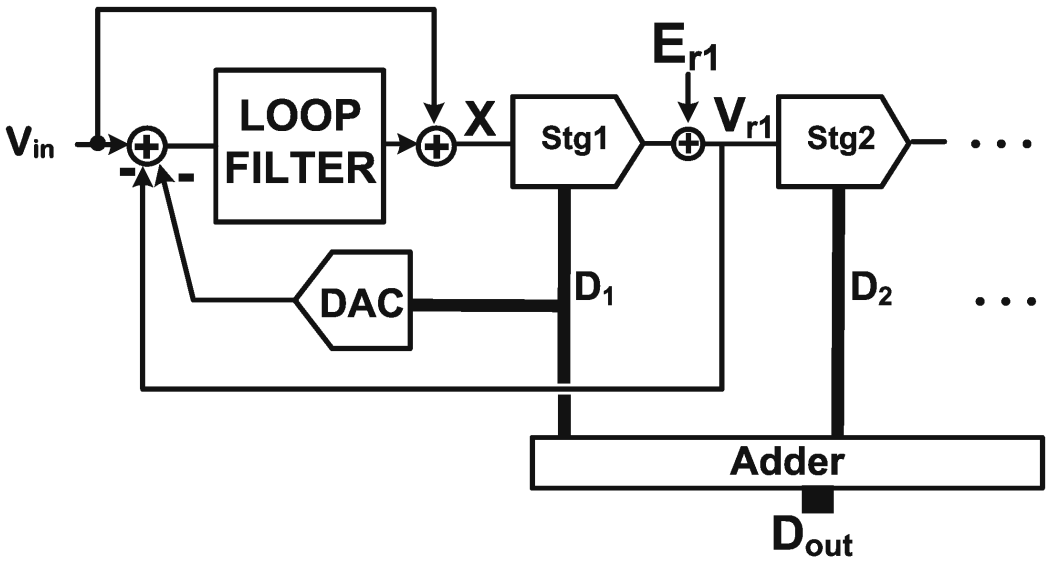

Figure 3.8: Analyzing errors from the first pipelined stage

stage error at the output of the modulator. The first MDAC errors are modeled by E_{r1} which is added at the output of the first stage. For simplicity, the later stages of the pipelined ADC and the feedbacks from the last stage are not shown. Also the output residue of the MDAC is scaled.

$$\frac{D_{out}}{E_{r1}} = NTF_L = (1 - z^{-1})^L \tag{3.13}$$

Equation (3.13) shows that errors generated by the first pipelined stage are shaped by the loop filter (L). This will greatly relax the design requirements of the first pipelined stage. Errors from the succeeding stages of the pipelined ADC appear directly at the output and are not processed by the loop filter. However, these errors are suppressed by the inter-stage gain of the preceding stage(s). Consequently, if enough number of bits are resolved at the first stage, errors from the succeeding stages will be sufficiently reduced. The output representation of the errors from the later pipelined stages is derived in the following expression.

$$\frac{D_{out}}{E_{ri}} = \frac{1}{G_1...G_{i-1}} \tag{3.14}$$

where E_{ri} and G_{i-1} denote errors from the i^{th} pipelined stage and the gain of the $(i-1)^{th}$ pipelined MDAC, respectively.

The HDSP architecture is flexible enough to accommodate large number of the pipelined stages. Increasing the number of the pipelined stages introduces more delays in the quantization. However, more analog feedbacks can be employed to stabilize the overall system and enhance the order of noise shaping.

Finding the proper number of the pipelined stages depends on several design considerations. Some of these design considerations are the simplicity of the feedback DAC, the total number of the amplifiers, the simple configuration of the analog feedbacks and the accuracy requirements of the pipelined stages. SQNR requirements should also be considered in choosing the number of the pipelined stages. Equation (3.15) express the SQNR of the HDSP modulator as a function of M (the number of bits resovled in the pipelined ADC), L (the order of the loop filter), N (the number of full delays in the pipelined ADC) and OSR.

$$SQNR_{max}[dB] = 6.02M + 1.76 + (20(L+N)+10)log_{10}(OSR) - 10log_{10}(\frac{\pi^{2(L+N)}}{2(L+N)+1}) \tag{3.15}$$

The number of bits resolved per each pipelined stage can also vary from one bit to multi-bits. Resolving higher number of bits in the first stage is recommended, since it will relax the design requirements of the succeeding pipelined stages. However, resolving only 1.5 bits in the first stage avoids the need for DEM in the digital feedback path. This comes with a price of higher accuracy requirements for the succeeding stages.

Table 3.1: Comparing HDSP modulators with different combinations

	First HDSP modulator	**Second HDSP modulator**
Order of the HDSP modulator	3^{rd} **order**	3^{rd} **order**
Number of bits	**7 bits**	**7 bits**
Number of bits in the first stage	**1.5 bits**	**3.5 bits**
SQNR (Ideal components)	**77 / 86 dB @ OSR=6 / 8**	**77 / 86 dB @ OSR=6 / 8**
Order of the loop filter (L)	1^{st} **order**	2^{nd} **order**
number of the pipelined stages	**Five stages**	**Three stages**
Number of the loop filter amplifiers	**One**	**Two**
Number of the amplifiers in pipelined ADC	**Three (opamp sharing)**	**Two (opamp sharing)**
Number of delays in pipelined ADC (N)	**Two**	**One**
H **in (3.12)**	$3z^{-2} - 3z^{-1}$	$z^{-2} - 3z^{-1}$
NTF_{new} **in (3.12)**	$(1 - z^{-1})^3$	$(1 - z^{-1})^3$
Errors of the 1^{st} **stage** (E_{r1})	1^{st} **order shaped as shown in (3.13)**	2^{nd} **order shaped as shown in (3.13)**
Errors of the 2^{nd} **stage** (E_{r2})	**Suppressed by** $G_1 = 2$ **(3.14)**	**Suppressed by** $G_1 = 8$ **(3.14)**
The feedback factor of the 1^{st} **stage**	**High**	**Low**
DEM	**Not required**	**Required**

Table I compares the design of two third order HDSP modulators with 7-bits pipelined quantizers. The first HDSP modulator uses a first order loop filter and five pipelined stages. The second HDSP modulator uses a second order loop filter and three pipelined stages. Properties listed in table I show that both of these architectures have similar SQNRs, overall order of noise shaping and number of the amplifiers. However, the design requirements of the pipelined ADC in the second approach is more relaxed compared to the first one.

3.4 Design of the third order HDSP modulator

The third order HDSP modulator is shown in Fig. 3.9. In this figure, the integrators of the loop filter are denoted as I_1 and I_2. The first and the third stages of the pipelined ADC resolve 3.5-bits while the second stage resolves 1.5-bits giving total 8-bits effective quantization. The second order loop filter and the extra delay of the pipelined ADC together yield a third order noise shaping. Similar to the general architecture in Fig. 3.5, three feedback paths are used at the input of the loop filter (two from the first stage and one from the last stage). The two local feedback paths, from the residue of the third stage to the input of the second stage, generate a z^{-1} and a z^{-2} term to complete the third order NTF as detailed in (3.11).

In the HDSP modulator (Fig. 3.9), the addition of the feed-forward signals is performed at the input of the first pipelined stage which implies signal addition at the input of both the flash sub-ADC and the residue amplifier as shown in Fig. 3.10(a). To avoid the need for a dedicated active adder or a complicated passive summation at the input of the sub-ADC, the feed-forward signals are added at the input of the residue amplifier. Only the input signal is connected to the

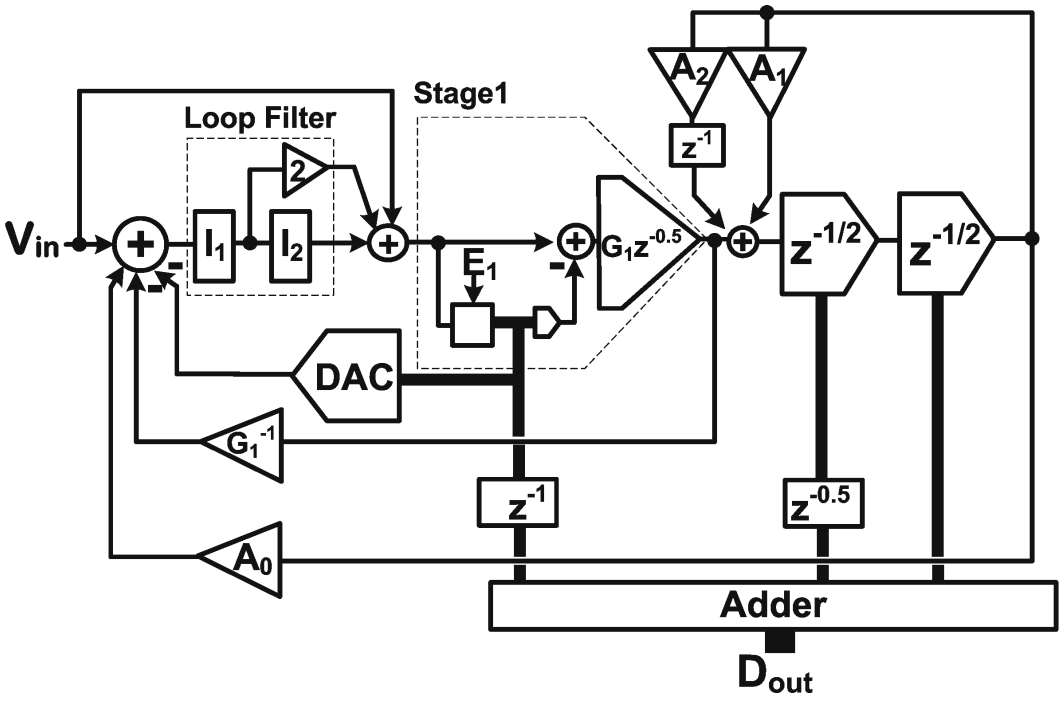

Figure 3.9: Third order HDSP modulator using second order loop filter and three stage pipelined quantizer

sub-ADC, as shown in Fig. 3.10(b).

These modifications do not change the proper operation of the HDSP modulator. Two features of the HDSP modulator make this simplification possible. First is the availability of the extra feedback paths from the first residue amplifier to the input of the loop filter. Hence, the output signal of the integrators are fed back to the loop filter through this path. Second is the very small swing of the integrators which does not increase the MDAC output swing significantly. It should be mentioned that E_1 is canceled at the input of the modulator and it does not appear at the output of the integrators. Hence, NTF with respect to the contribution of E_1 will also remain unchanged.

The adder simplification is also applied to the local feedback paths (A_2 and

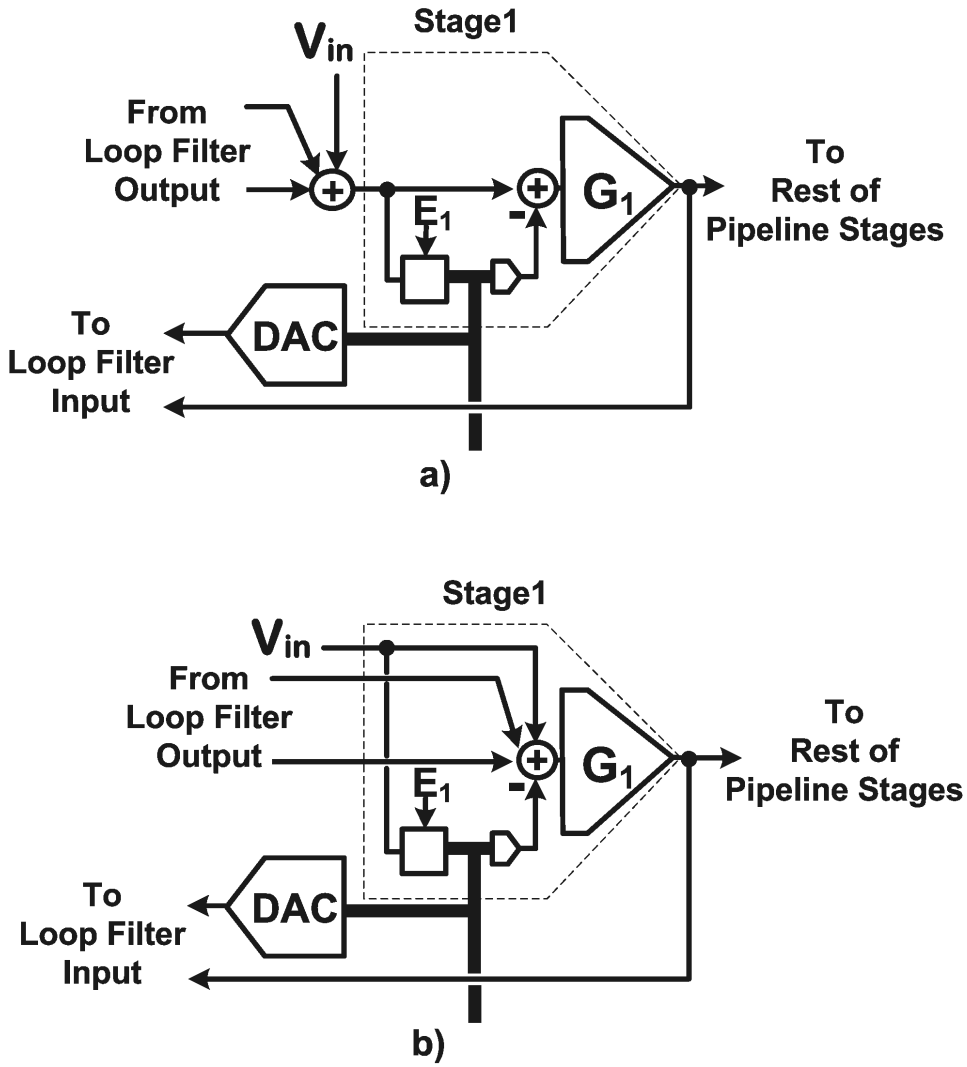

Figure 3.10: a) Signal addition at input of both sub-ADC and the residue amplifier b) Signal addition at input of just the residue amplifier

A_1) to the input of the second pipelined stage. Hence, the HDSP modulator requires no active/passive adders for the sub-ADCs in the pipelined stages.

Fig. 3.11 shows the details of the implemented modulator including the simplifications mentioned earlier. The first integrator has only a half clock-cycle delay. This will allow a half clock-cycle for the DEM in the feedback path [32] and the

first MDAC to operate. The input signal is also applied to the loop filter with a half-clock cycle delay to obtain a unity signal transfer and to ensure that the loop filter only processes the quantization noise.

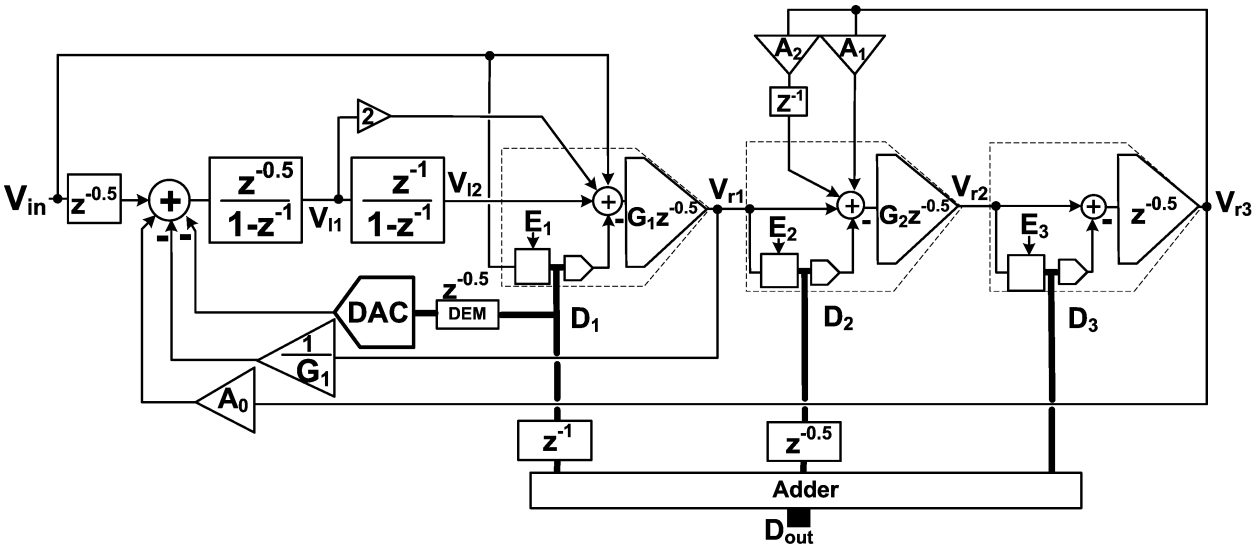

Figure 3.11: The implemented third order HDSP modulator

The detailed transfer functions of the third order architecture in Fig. 3.11 are given in appendix. The resulting noise transfer function is a complete 3^{rd} order polynomial with independent coefficients for each term, allowing the designer to set zero locations as desired. The zero optimization can be easily done by choosing A_1 and A_2 properly.

3.4.1 loop filter circuit implementation

The switched-capacitor realization of the loop filter is shown in Fig. 3.12. Single-ended implementation is shown for simplicity. Signals provided by the feedback DAC and the analog feedbacks from the pipelined ADC are all added at the

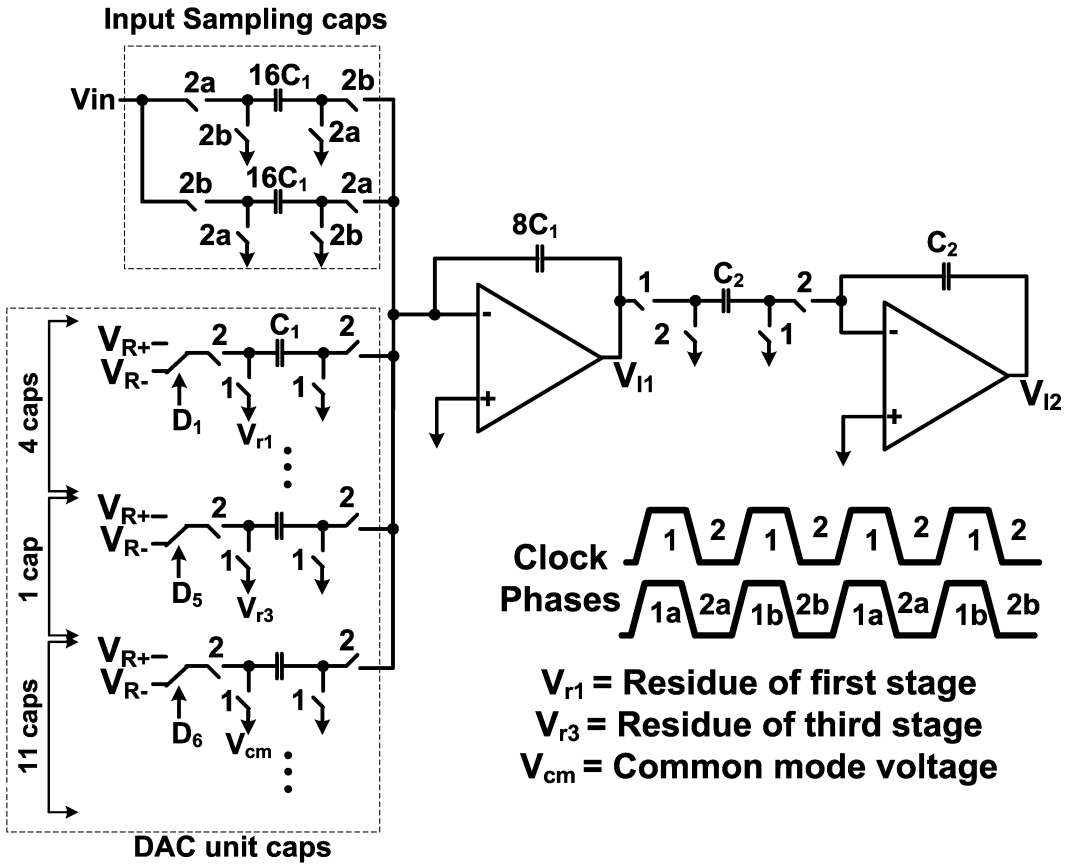

Figure 3.12: The switched-capacitor realization of the loop filter

input of the first integrator. Separate input and DAC capacitors are used at the input of the loop filter. Some of the DAC capacitors are shared with feedbacks from the analog residue of the first and the last pipelined stage. The feedback DAC has sixteen unit elements. To realize the attenuation ($\frac{1}{G_1} = \frac{1}{4}$) needed on the residue of the first pipelined stage, four out of the sixteen DAC unit elements are used. A single DAC unit element is used to realize the attenuation ($\frac{1}{G_1 G_2} = \frac{1}{16}$) needed on the residue of the last pipelined stage.

The half clock cycle delay on the input signal is realized using two sampling capacitors alternately. The alternate sampling phases are shown in Fig. 3.12.

Due to the relaxed gain and swing requirements of the integrators, single-stage telescopic amplifiers are used. A GBW of more than 1 GHz and DC gain of about 40 dB are designed for the first integrator opamp. These parameters were scaled down for the second integrator to conserve power. Conventional data weighted averaging (DWA) was applied to filter the mismatch errors of the 16-level DAC and to achieve the required linearity [48].

3.4.2 Pipelined ADC circuit implementation

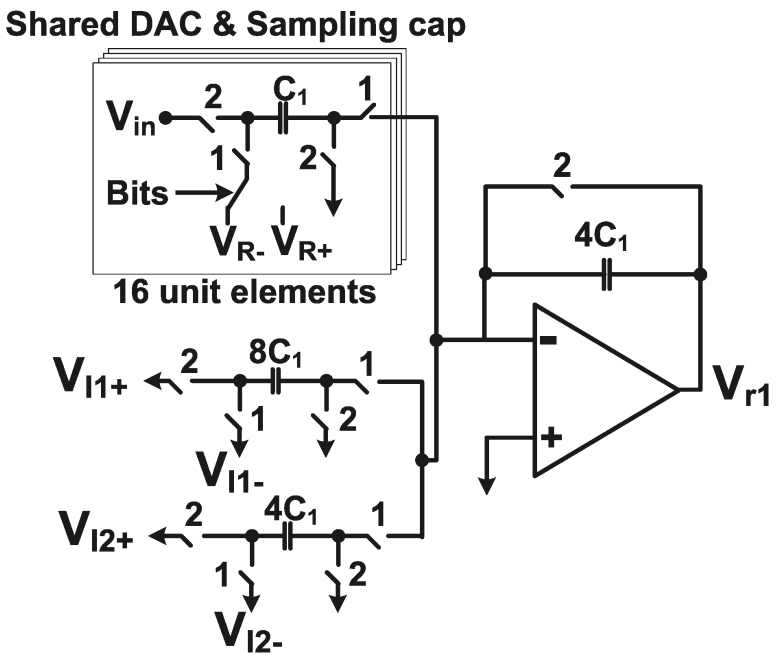

Figure 3.13: The switched-capacitor realization of the first pipelined stage

Circuit realization of the first pipelined stage is shown in Fig. 3.13. One set of capacitors are shared between the input signal and the 16-level DAC. Output signals of the loop filter integrators are also added at the input of the residue amplifier using dedicated capacitors.

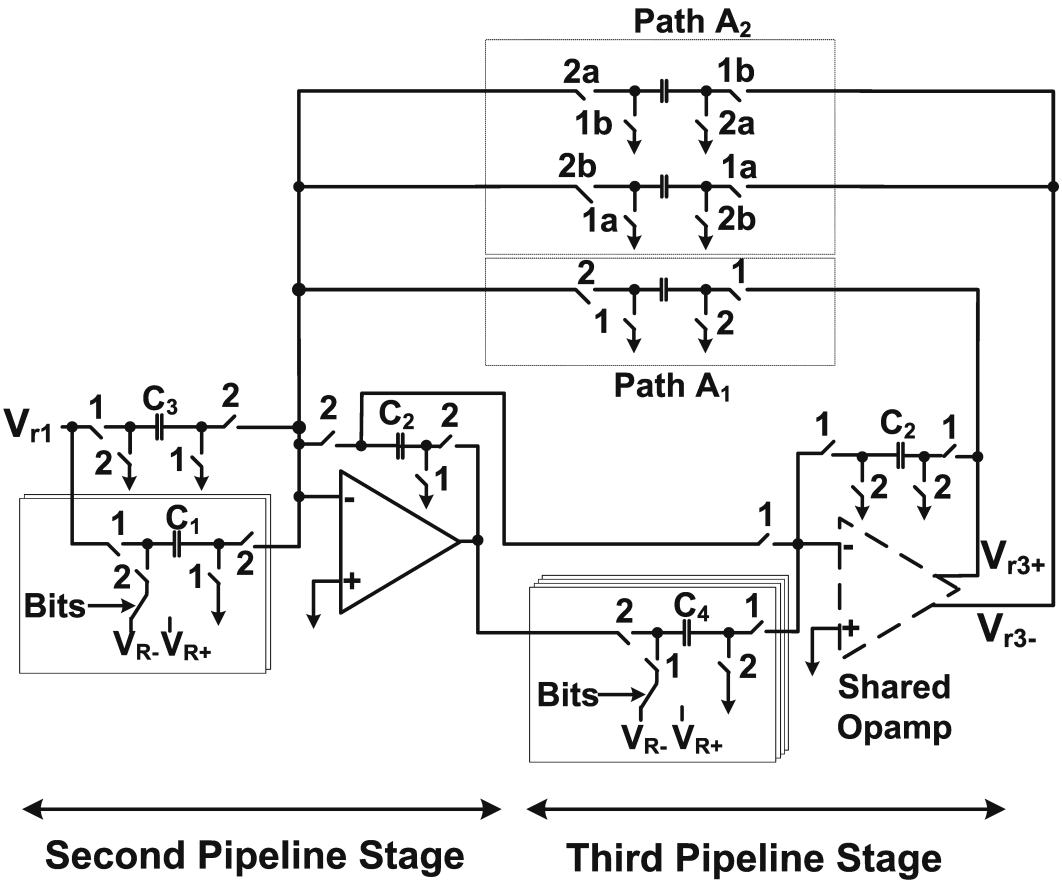

Figure 3.14: The switched-capacitor realization of the second and the third pipelined stages

Several techniques are employed to keep the feedback factor of the first stage reasonable. First, the gain of the first stage and the reference of the second stage sub-ADC are halved. This allows the feedback factor to be increased without reducing the effective number of resolved bits. Second, the gain of the integrators is doubled, and hence the feed-forward signals capacitors are halved. Third, by sampling the integrator outputs twice (in both phases), these capacitors are further reduced, resulting in one-fourth the original capacitor size.

Feedback capacitor in Fig. 3.13 is reset in the sampling phase (2). Parasitic

capacitance introduced by the reset switch changes the closed-loop gain. The measurement results indicated that this parasitic capacitance changes the closed-loop gain significantly (about seven percent) as a result of a minor design oversight. The reduced closed-loop gain is compensated in the digital domain. The digital compensation is not required in a more careful design.

The circuit implementation of the second and the third pipelined stages is shown in Fig. 3.14. The third stage shares an amplifier with the second pipelined stage [29]. The two local feedback paths from the output of the third stage to the input of the second pipelined stage are also shown in this figure. The delayed feedback path (A_2) is realized by using two capacitors for sampling the last stage residue alternately. In addition to the opamp sharing, capacitor and switch sharing is also used for further simplification.

Output signal swing requirement of the residue amplifiers is similar to that of the conventional pipelined stages. The loop gain requirement of the first pipelined stage is about 37dB for 13-bits overall accuracy at an OSR of 6. To realize this gain, a two-stage residue amplifier is used.

Bootstrap switches are used for sampling the input signal [46]. Offset canceled comparators composed of a preamplifier, regeneration and SR latches are used in the implementation [47].

3.5 Measurement Results

The proposed HDSP architecture was designed and fabricated in a 2P4M 0.18μm CMOS process [49]. The die photograph is shown in Fig. 4.22. The HDSP modulator contains three main blocks (loop filter, first pipelined MDAC and shared second/third MDACs). The total die area is $3.75mm^2$.

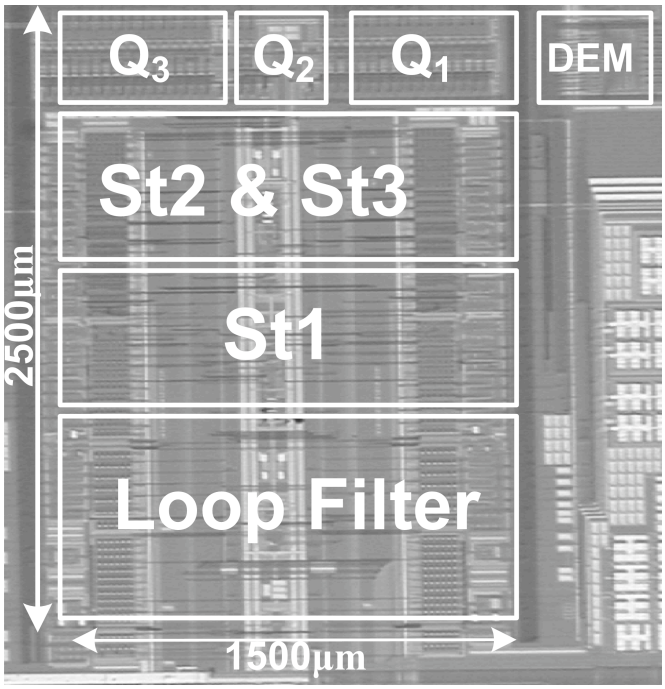

Figure 3.15: The chip die micrograph

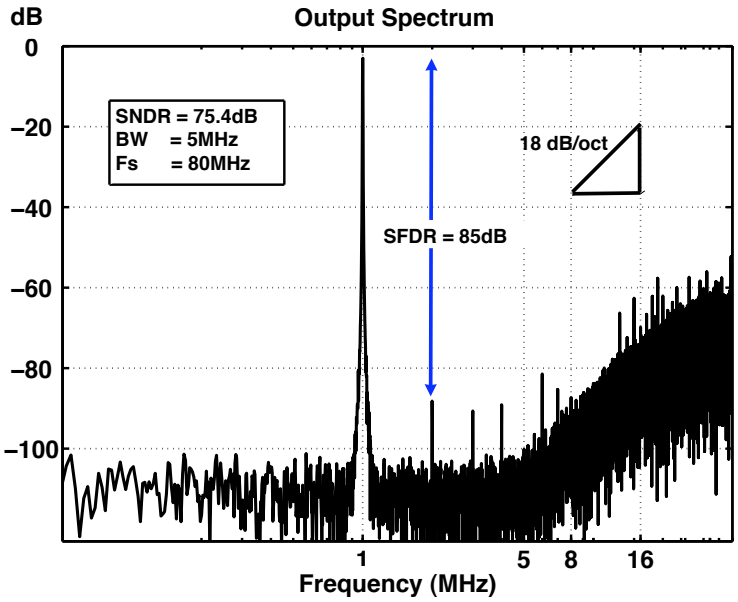

Figure 3.16: The output spectrum at 80 MHz sampling rate (32K points FFT)

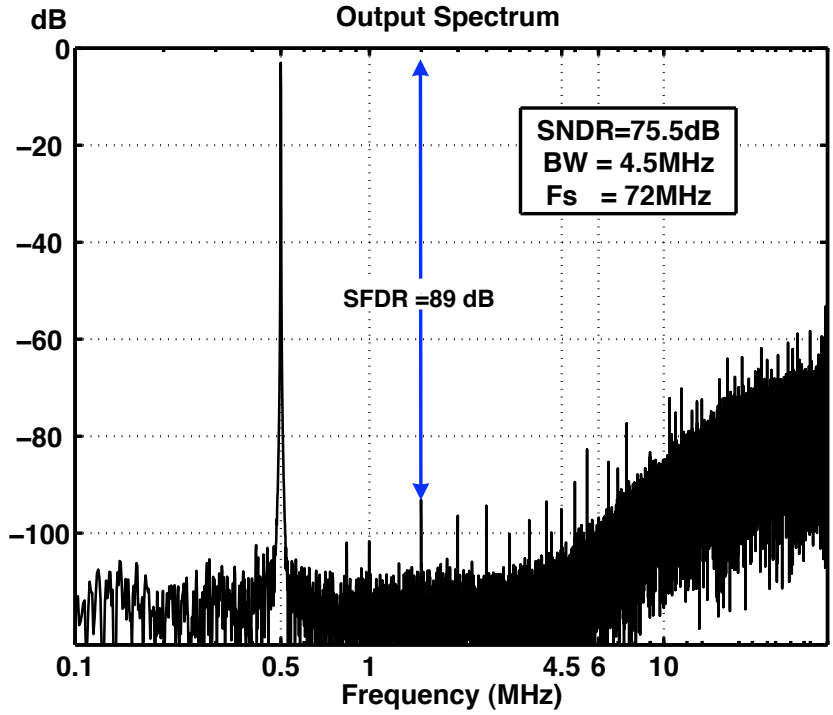

Figure 3.17: The output spectrum at 72 MHz sampling rate (64K points FFT)

The measured output spectrum is shown in Fig. 5.16 for 80 MHz sampling rate and 1MHz input signal. The peak SNDR is 75.4dB at OSR of 8 and 72dB at OSR of 6. The 18 dB/octave slope of the quantization noise demonstrates the third order noise shaping is achieved. Fig. 5.17 shows the output spectrum at 72 MHz sampling and 0.5MHz input signal. In this case, the peak SNDR at OSR of 8 and 6 is 75.5dB and 71.8dB, respectively. The SNDR plot for varying input signal amplitude is shown in Fig. 5.18 for 80 MHz sampling rate (OSR of 8 and 6). At 72 MHz, lower supply voltages are used to decrease the power consumption. The measurement results (summarized in Table II) demonstrate the effectiveness of this modulator down to 6X OSR.

This proposed structure combines the efficiency of a pipelined ADC with

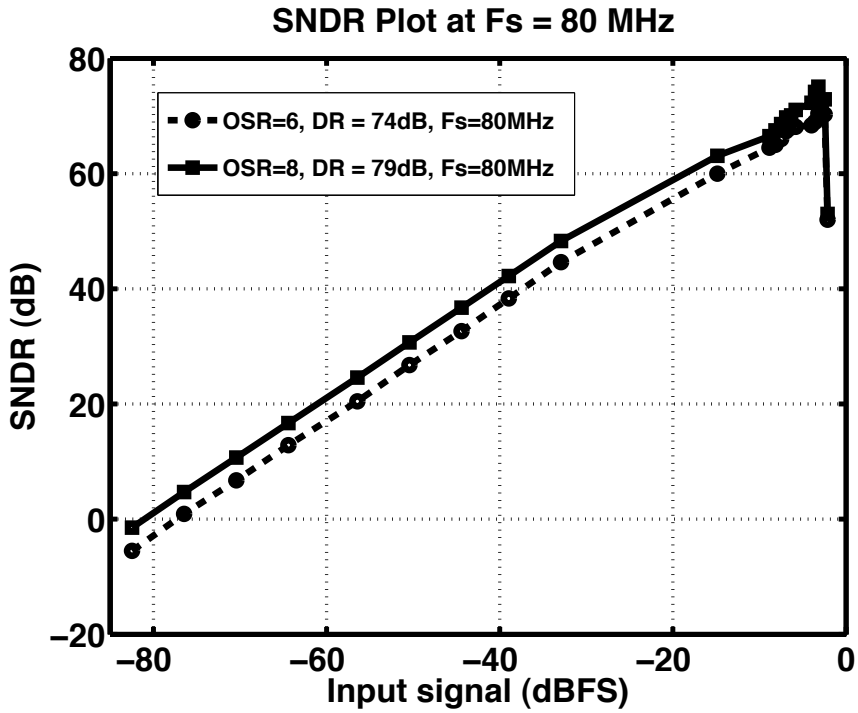

Figure 3.18: SNDR plot at 80 MHz sampling rate

the noise shaping property of a single-loop $\Delta\Sigma$ modulator. The figure-of-merit ($FOM = \frac{Power}{2BW.2^{ENOB}}$) [35] of this modulator is among the best reported for high bandwidth switch-capacitor (SC) $\Delta\Sigma$ ADCs.

3.6 Conclusions

A new hybrid Delta-Sigma/pipelined analog-to-digital converter is proposed. This structure combines the efficiency of the pipelined ADC with the noise shaping property of a $\Delta\Sigma$ modulator. Even though the loop filter benefits by processing only the small amount of the quantization noise from the full pipelined ADC, the DAC at the input of the modulator is only associated with the first pipelined stage.

Table 3.2: Summary of measurment results

Sampling Frequency	**Fs =72MHz**		**Fs=80Mz**	
OSR	**8**	**6**	**8**	**6**
Signal BW (MHz)	**4.5**	**6**	**5**	**6.66**
Fin (MHz)	**0.5**	**0.5**	**1**	**1**
SFDR (dB)	**89**	**80**	**85**	**78**
SNR (dB)	**76**	**72.2**	**76**	**72**
SNDR (dB)	**75.5**	**71.8**	**75.4**	**72**
FOM (pJ/conv)	**0.67**	**0.77**	**0.75**	**0.81**
Input Range (Diff)	**1.8 Vp-p**		**1.8 Vp-p**	
Power (W)	**13m(D),16.4m(A)**		**14m(D),22m(A)**	
Power Supply(V)	**1.7(D),1.65(A)**		**1.8**	
Core Area	**3.75** mm^2			
Technology	**0.18μm CMOS**			

Delays of the pipelined stages are used to provide additional noise shaping. Furthermore, zero-optimization can be applied easily since all coefficients needed are in the analog form. All these advantages makes this structure a suitable candidate for high-accuracy wideband (low OSR) applications.

APPENDIX I. Detailed Transfer Function

Signal transfer functions at each node of the HDSP modulator of Fig.11 verifies the concepts discussed in the sections 3.2 and 3.3. In the following transfer functions no simplification is made. Latency and gain of the pipelined stages and the details of the loop filter are all taken into account. Writing the transfer function of the digital output and the residue of each MDAC will result in

$$D_1 = V_{in} + E_1 \tag{3.16}$$

$$D_2 = V_{r1} + E_2 \tag{3.17}$$

$$D_3 = V_{r2} + E_3 \tag{3.18}$$

$$V_{r1} = G_1(V_{I2} + 2V_{I1} - E_1)z^{-0.5} \tag{3.19}$$

$$V_{r2} = G_2(A_2V_{r3}z^{-1} + A_1V_{r3} - E_2)z^{-0.5} \tag{3.20}$$

$$V_{r3} = -E_3z^{-0.5} \tag{3.21}$$

$$V_{I1} = \frac{z^{-0.5}}{1-z^{-1}}\Big[V_{in}z^{-0.5} - \frac{V_{r1}}{G_1} - D_1z^{-0.5} + A_0V_{r3}\Big] \tag{3.22}$$

$$V_{I2} = \frac{z^{-1}}{1-z^{-1}}V_{I1}. \tag{3.23}$$

Here V_{Ii}, V_{ri} and D_i denote the output of the i^{th} integrator, the output of the i^{th} residue amplifier, and the output of the i^{th} quantizer, respectively. The output of the integrators can be obtained by replacing (3.16),(3.19) and (3.21) in (3.22), yielding

$$\begin{aligned} V_{I1} &= \frac{z^{-1}}{1-z^{-1}}\Big[-A_0E_3 - (2V_{I1} + V_{I2})\Big] \\ &= -z^{-1}(1-z^{-1})A_0E_3 \end{aligned} \tag{3.24}$$

$$V_{I2} = -z^{-2}A_0E_3. \tag{3.25}$$

Equations (3.24) and (3.25) show that the integrators in this architecture only process a scaled quantization error of the last pipelined stage. It will be

shown later that the coefficient A_0 should be inverse of all the inter-stage gains product, which is a small value. This explains the small swing of the integrators in the HDSP modulator.

The output expressions of the residue amplifiers can now be simplified to

$$V_{r1} = G_1\Big[- A_0E_3(-z^{-2} + 2z^{-1}) - E_1\Big]z^{-0.5} \tag{3.26}$$

$$V_{r2} = -G_2\Big[(A_2z^{-1} + A_1)z^{-1}E_3 + E_2z^{-0.5}\Big] \tag{3.27}$$

$$V_{r3} = -E_3z^{-0.5} \tag{3.28}$$

as a result, the digital output of each quantizer will be

$$D_2 = G_1\Big[A_0E_3(z^{-2} - 2z^{-1}) - E_1\Big]z^{-0.5} + E_2 \tag{3.29}$$

$$D_3 = -G_2\Big[(A_2z^{-1} + A_1)z^{-1}E_3 + E_2z^{-0.5}\Big] + E_3 \tag{3.30}$$

and finally the overall digital output can be derived as

$$\begin{aligned} D_{out} &= D_1z^{-1} + \frac{D_2}{G_1}z^{-0.5} + \frac{D_3}{G_1G_2} \\ &= V_{in}z^{-1} + \frac{1}{G_1G_2}\Big[A_0G_1G_2z^{-3} + (-2A_0G_1G_2 - A_2G_2)z^{-2} \\ &\qquad -A_1G_2z^{-1} + 1\Big]E_3. \end{aligned} \tag{3.31}$$

Equation (3.31) shows the signal and the noise transfer function of this structure. It can be seen that a third order polynomial is achieved for the noise transfer function as expected. The delay in the signal transfer function is a result of the delay in the back-end stages, which is formed outside the modulator loop and will not affect the loop filter. Coefficients A_0, A_1 and A_2 should be determined properly to achieve the desired NTF. For example, to achieve a third order NTF with all the zeros placed at DC, the feedback coefficients should be set as follows

$$A_0 = -\frac{1}{G_1G_2}, A_2 = -\frac{1}{G_2}, A_1 = \frac{3}{G_2} \tag{3.32}$$

yielding

$$D_{out} = V_{in}z^{-1} + (1 - z^{-1})^3 \frac{E_3}{G_1 G_2}. \tag{3.33}$$

It should also be noted that G_1G_2 is the product of the inter-stage gains of the pipelined ADC and $\frac{E_3}{G_1G_2}$ is the equivalent quantization noise of the pipelined ADC.

CHAPTER 4. DESIGN AND APPLICATION OF A NOISE-SHAPED TWO-STEP QUANTIZER

4.1 Introduction

In the previous chapter, the Hybrid Delta-Sigma/Pipelined modulator (HDSP), is introduced as an efficient choice for low OSR, high bandwidth applications, since it improves the accuracy at low OSRs without increasing the design complexity. However, this architecture still needs to be further simplified for the low power applications. The loop filter in the HDSP modulator has relaxed design requirements and it plays a less significant role in the overall power dissipation. Hence, simplifying the pipelined quantizer is essential for improving the power efficiency.

A two-step quantizer is the simplest form of the pipelined ADC and it can provide enough resolution for the HDSP architecture. In this chapter, efficient implementation of the two-step quantizer for oversampling applications is studied. A new Noise-Shaped Two-Step ADC (NSTS) is presented which provides high order noise-shaping without using any extra amplifier. A new capacitor/opamp sharing scheme is employed for the simple realization of the NSTS quantizer. The proposed architecture can be used either as a standalone oversampled ADC, as individual stage of a cascaded ADC or as the quantizer of the HDSP modulator. These three representations are introduced in this chapter.

This chapter is organized as follows: in section 4.2, the NSTS ADC is in-

troduced and its properties are studied. In section 4.3, the application of the NSTS ADC in a low OSR cascaded architecture is discussed. The implementation of a power efficient two-step HDSP modulator is presented in section 4.4. Finally, conclusions are given in section 4.5.

4.2 The proposed Noise-Shaped Two-Step (NSTS) quantizer

Two-step (or sub-ranging) converters are among the most popular approaches for high-speed, medium accuracy ADCs owing to their simple architecture over their flash counterpart [38]. In two step ADCs, the MSB bits are resolved first, the residue is extracted and amplified. The second sub-ADC resolves the remaining LSBs (Fig. 4.1.a). The quantization noise of the first stage is ideally canceled out and only the scaled quantization noise of the second stage appears at the digital output.

The proposed NSTS quantizer is shown in Fig. 4.1.b. In this architecture, a multiplying-DAC (MDAC) is used for the second stage to extract its quantization noise in the analog form. This quantization noise is fed back to the input of ADC with the transfer function $H(z)$. The signal provided by the feedback path appears at the final digital output and provides noise shaping for the quantization noise of the second stage (E_2). The feedback path can be configured to provide first, second or higher order noise shaping. The residue amplifier of the two-step ADC can be shared between the first and the second MDACs. Hence, no extra amplifier is required for achieving noise shaping. The output transfer function of the proposed NSTS ADC can be derived as following

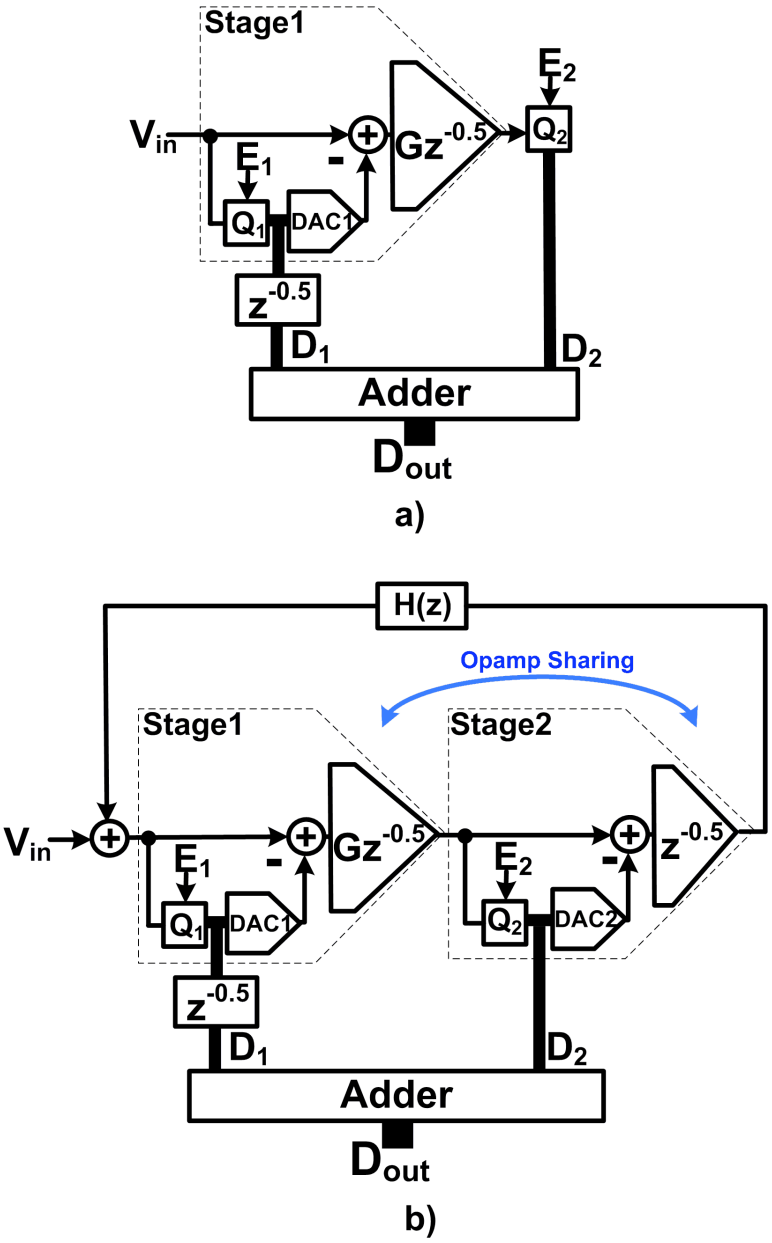

Figure 4.1: a) Traditional two-step quantizer b)The proposed NSTS quantizer

$$D_1 = X_{in} + E_1 - H(z)E_2 z^{-0.5} \tag{4.1}$$

$$D_2 = -GE_1 z^{-0.5} + E_2 \tag{4.2}$$

$$D_{out} = D_1 z^{-0.5} + \frac{D_2}{G} = X_{in} z^{-0.5} + \frac{(-GH(z)z^{-1} + 1)E_2}{G} \tag{4.3}$$

$$H(z) = \frac{A_1 + A_2 z^{-1} + ...}{G} \tag{4.4}$$

$$NTF = 1 - A_1 z^{-1} - A_2 z^{-2} + ... \tag{4.5}$$

Each stage of the two-step ADC provides half a clock-cycle delay. This delay along with the delaying terms in $H(z)$ form the overall noise transfer function. For the first order noise shaping, only one feedback path is required ($A_1 = 1$). Second and third order noise shaping can be achieved by using extra feedback paths ($A_1 = 2$, $A_2 = -1$ for the second order noise shaping and $A_1 = 3$, $A_2 = -3$, $A_3 = 1$ for the third order noise shaping). The delaying terms in $H(z)$ can be generated by using a passive FIR network. The complexity of the feedback path for the 1^{st}, 2^{nd} and 3^{rd} order noise shaping is minimal.

4.2.1 Properties of the NSTS ADC

The proposed NSTS architecture can be employed as a standalone oversampling ADC. The standalone architecture needs only one residue amplifier for resolving high number of bits (e.g. 7-8 bits) and high orders of noise shaping (e.g. 3^{rd} order). This make the NSTS architecture an attractive choice for most of the oversampling applications. For instance, a third order 7-bit NSTS ADC can ideally achieve around 85dB SQNR at OSR of only 8X with significantly lower hardware requirements compared to the equivalent MASH [39] and single-loop $\Delta\Sigma$ modulators [40]. However, this advantage comes with a price. Similar to the cascaded (MASH) modulators, the standalone NSTS ADC is prone to the quantization noise leakage of the first stage (E_1) and it requires relatively high gain residue amplifier.

E_1 is canceled out at the final digital output and the gain error of the residue amplifier makes the cancellation imperfect. The residue amplifier is also reused to extract E_2 in the second stage. However, the gain error of the residue amplifier as the second stage only changes the location of the NTF zeros slightly and doesn't affect the performance significantly. The gain error of the amplifier in each stage is modeled in Fig. 4.2. The gain error appears at the output as following

$$E_{r1} = \frac{G}{\beta_1 A} E_1 z^{-0.5} \tag{4.6}$$

$$E_{r2} = \frac{1}{\beta_2 A} E_2 z^{-0.5} \tag{4.7}$$

$$D_{out} = X_{in} + NTFE_2 + \frac{E_{r1}}{G} + \frac{(1-NTF)E_{r2}}{G} - E_{D1} - \frac{(1-NTF)E_{D2}}{G} \tag{4.8}$$

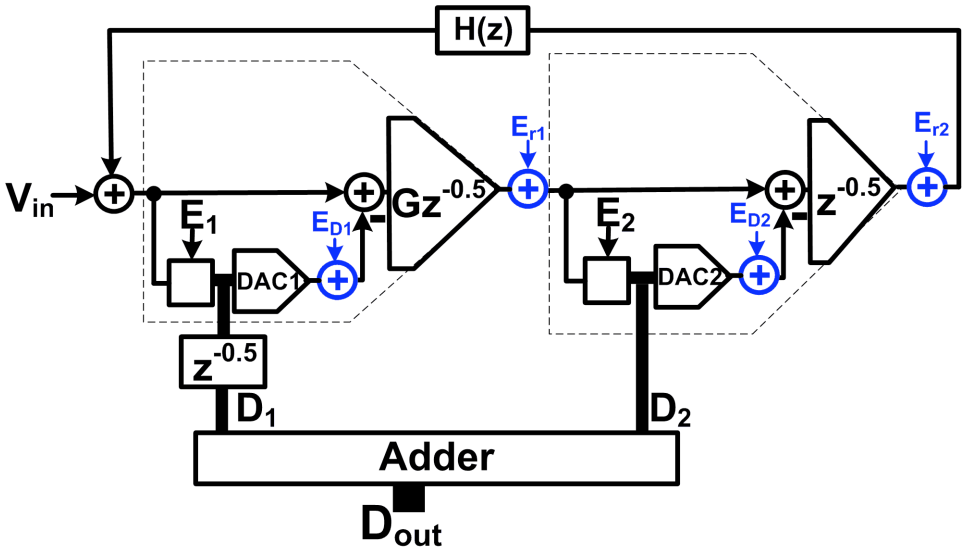

Figure 4.2: Opamp and DAC error modeling in NSTS ADC

Here, A is the DC gain of the amplifier and β_1 and β_2 are the feedback factors of the first and the second stage respectively. (4.8) shows that first stage gain error ($\frac{E_1}{\beta_1 A}$) directly appears at the output, but the gain error of the second

stage is suppressed by the inter-stage gain (G). In (4.8), E_{D1} and E_{D2} represents the non-linearity of the DAC in the first and the second stage respectively. E_{D1} directly appears at the output without any suppression. Hence, the first DAC requires dynamic element matching (DEM). DEM for this DAC can operate in the non-overlapping time between the sampling and the amplification phases. The linearity requirement of the DAC in the first stage is similar to the front-end DAC in the traditional $\Delta\Sigma$ ADCs. However, any error generated by the DAC in the second stage is suppressed by the inter-stage gain and this DAC does not need DEM.

Sub-ADCs in the first and second stage have relaxed design requirements. Errors generated by these sub-ADCs are treated like the quantization noise of the relevant sub-ADCs. Hence, the errors from the first sub-ADC appear at the digital outputs of both stages and consequently are canceled out. The errors from the second sub-ADC are shaped through the feedback path.

4.2.2 The simplified NSTS ADC with extended dynamic range

Feedback signal addition at the input of the first stage of the NSTS ADC, implies signal addition at the input of both sub-ADC and the residue amplifier. In the high order NSTS ADC, the signal addition at the input of the sub-ADC is complex. The need for a dedicated adder at the input of the sub-ADC can be avoided by adding the feed-forward signals at the input of only the residue amplifier as shown in Fig. 4.3. In this realization, the feedback information ($H(z)E_2$ in (4.1)) appears at the digital output of the second stage (D_2) instead of the first stage (D_1), but NTF remains unchanged. However, the added information increases the output swing of the residue amplifier and it may overload this am-

plifier. Opamp overload can be prevented by either increasing the number of bits resolved in the second stage or extending the redundancy between the pipelined stages. The former reduces the quantization noise power (reduces signal provided by the feedback path) and the later increases the reference range of the second sub-ADC (allows higher output swing range for the first stage). In the proposed architecture, the built-in redundancy is extended by adding extra comparators to the second quantizer to increase the reference range.

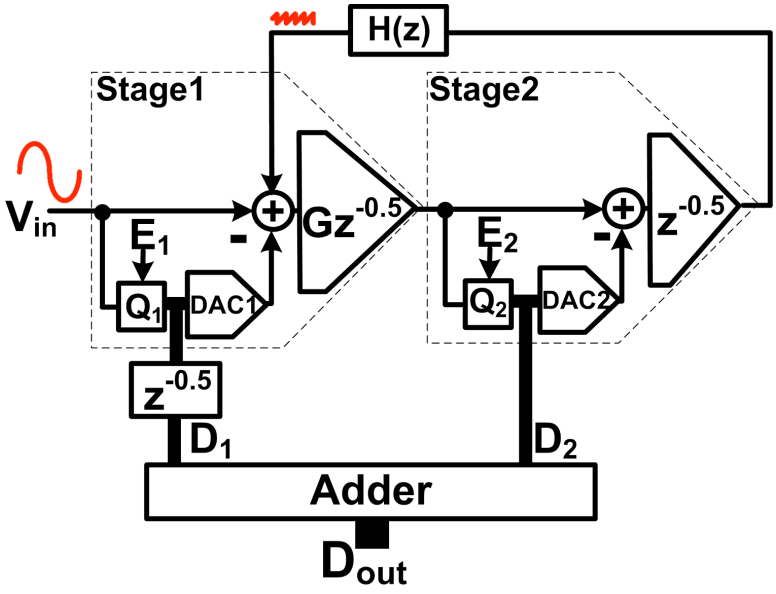

Figure 4.3: The NSTS ADC with the simplified signal addition

In the simplified NSTS, the first quantizer (Q_1) is directly connected to the input signal. Hence, the full scale input signal can be applied to the first quantizer, Q_1. If the input signal of Q_1 exceeds the reference voltage, Q_1 chops off the over-range input signal and the residue amplifier sees a fraction of the input signal. Thanks to the extended redundancy, the simplified NSTS ADC can tolerate even over full-range input signals without overloading the residue amplifier. Simulation results shows that a third order NSTS ADC with a 8-levels quantizer in the first

stage and a 20-levels quantizer (16 regular comparators +4 additional comparators to extend the redundancy) can tolerate up to 2dB over full-range input signals. The over-range operation of the NSTS ADC can be further extended by increasing the redundancy between the first and second stages further as described in [41] and [42].

4.2.3 Circuit realization

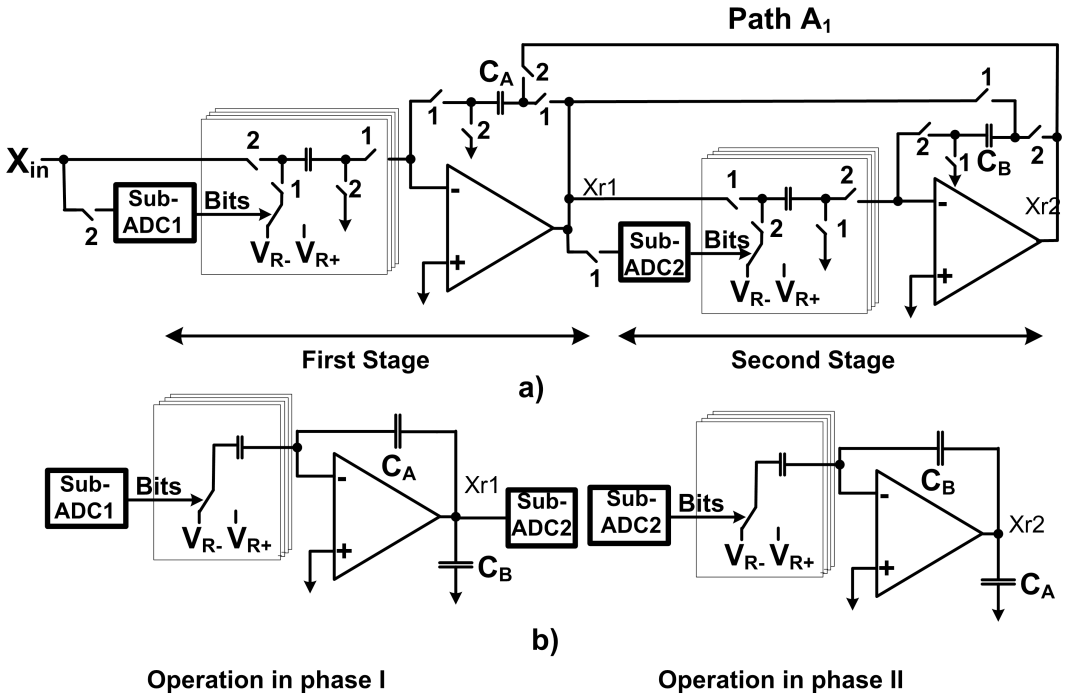

Figure 4.4: The potential circuit realization of the NSTS ADC

The potential circuit implementation of the first order NSTS architecture is shown in Fig. 4.4.a. In this potential realization, the residue of the first and the second stages (X_{r1} and X_{r2}) are extracted in phase 1 and 2 respectively. The first stage uses separate sampling and feedback capacitors. In order to implement

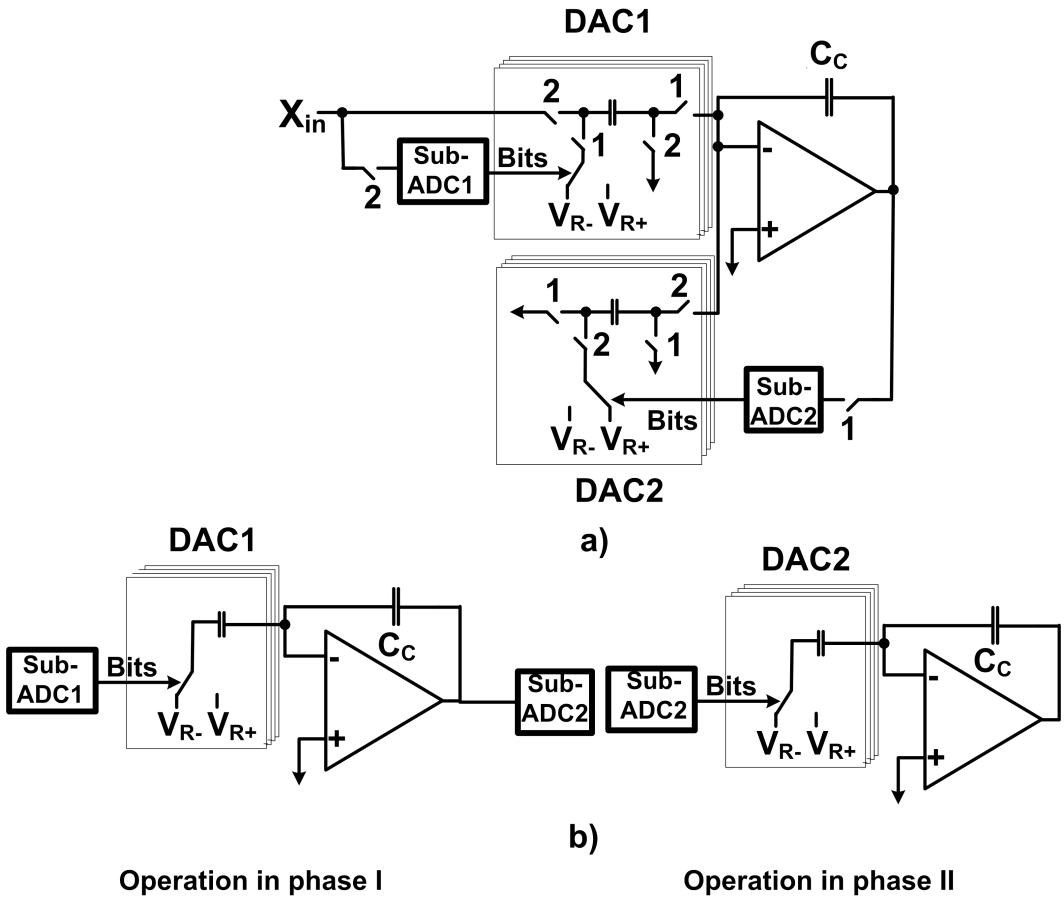

Figure 4.5: The simplified circuit realization of the NSTS ADC

the feedback path A, X_{r2} (sampled on the C_A in the preceding phase 2) is added to the output residue of the first stage. The second stage uses the flip-around architecture and C_B is the flip-around sampling capacitor. The operation of this circuit in phase 1 and phase 2 is shown in Fig. 4.4.b. In this two-step quantizer, C_A and C_B both carry X_{r1} at the end of phase 1 and X_{r2} at the end of phase 2. Hence, the two stages can share the feedback capacitor and the residue amplifier, as shown in Fig. 4.5. In phase 1, the gain stage works as the first stage and the charge stored on C_c (in the preceding phase 2) plays the role of the feedback path A. In phase 2, the gain stage operates as the second stage where C_c is the flip-around sampling

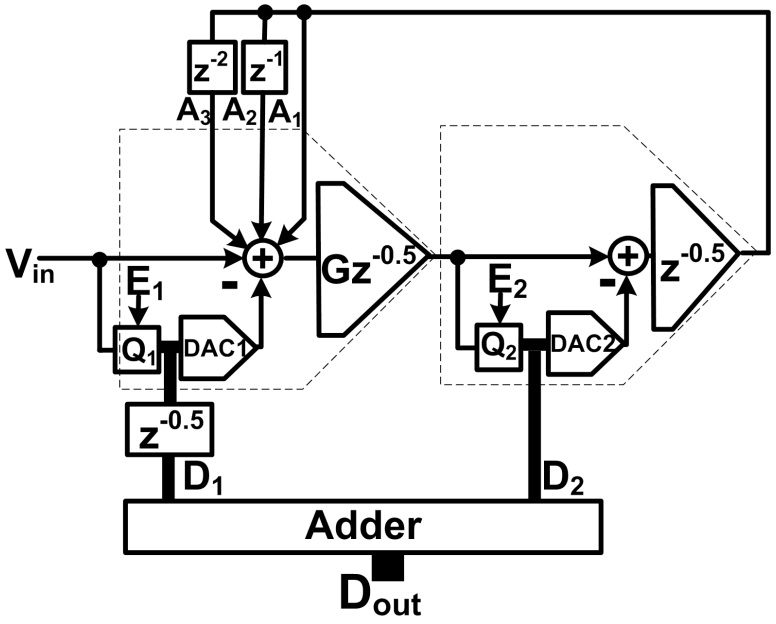

Figure 4.6: The third order NSTS ADC

capacitor. Respectively, the output voltage of the gain stage in phase 1 is X_{r1} and in phase 2 is X_{r2}. Note that the output signal of the amplifier is not integrated through the feedback path. This is because the output voltage of the amplifier is quantized in phase 1 and the output voltage memory is wiped out in the succeeding phase 2. The proposed capacitor and opamp sharing technique reduces the design complexity (number of the switches and capacitors) and the output loading of the amplifier, since C_c simultaneously plays the role of the sampling capacitance and the output load. This respectively decreases the power consumption.

Higher order implementation of the NSTS quantizer requires a passive capacitive network to generate the delaying terms in $H(z)$. For introducing one delay in the feedback path, two capacitors sample the signal in the alternate clock phases and the sampled charge is used with one cycle delay. Similarly, two delays can be generated by using three capacitors sampling the signal in alternate clock

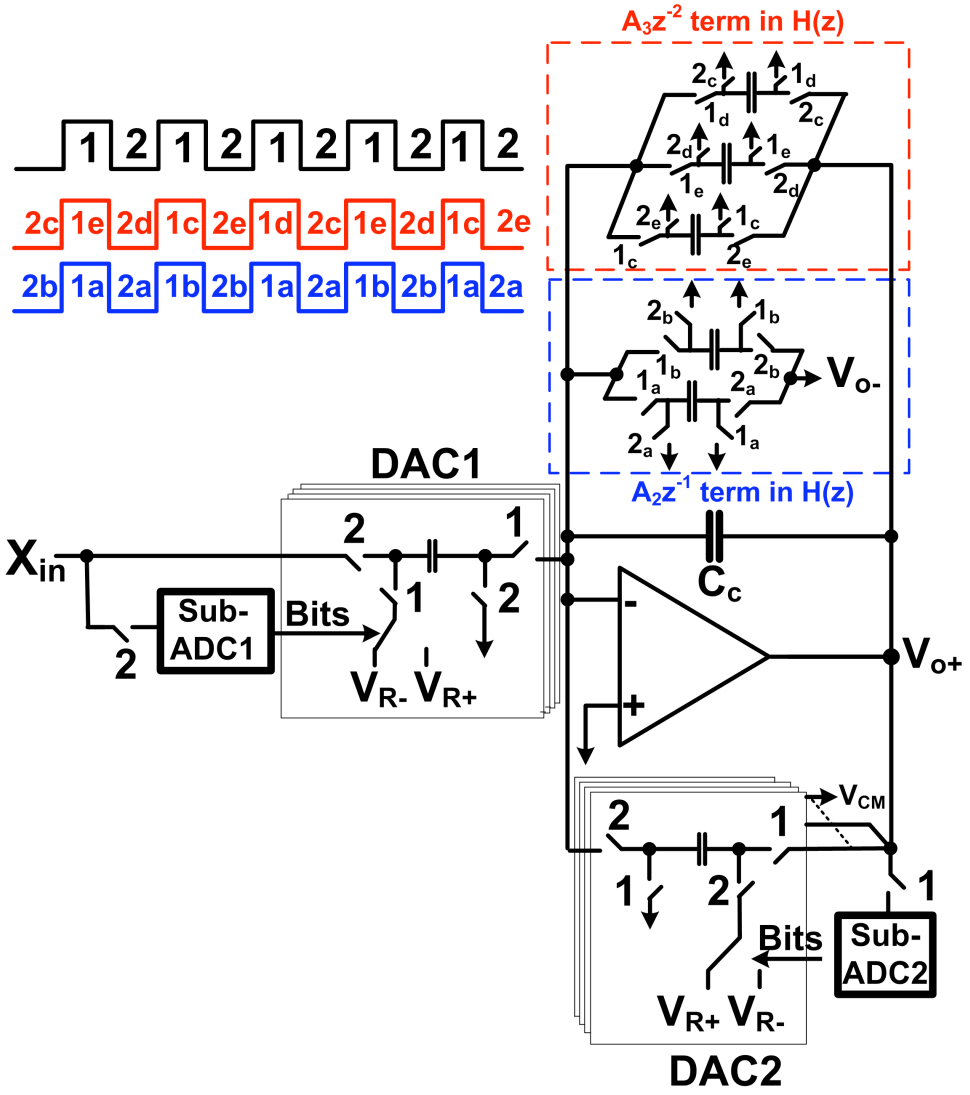

Figure 4.7: The circuit realization of the third-order NSTS ADC

phases and using the sampled voltages with two cycle delays. The system-level and the circuit-level realization of the third order NSTS are shown in Fig. 4.6 and Fig. 4.7. Compared to the first order implementation, the $H(z)$ has two more delaying terms. The delaying terms are generated by using the passive sampling network discussed earlier. Capacitor connections are flipped to realize negative

coefficients in $H(z)$. Note that the single-ended architecture is shown in Fig. 4.7 for the sake of simplicity.

In the first order NSTS, the coefficient A_1 is one. Hence, the inter-stage gain of the second stage is also set to one for the proper realization of the feedback path. For the third order NSTS, A_1 is three. Accordingly, the inter-stage gain of the second stage is scaled up to three to keep the core gain stage unchanged. In order to achieve the gain of three for the second stage, some of the second DAC capacitors are shared with the signal path.

4.3 The application of the NSTS ADC in the cascaded architecture

4.3.1 The NSTS ADC as the counterpart of the MASH ADC

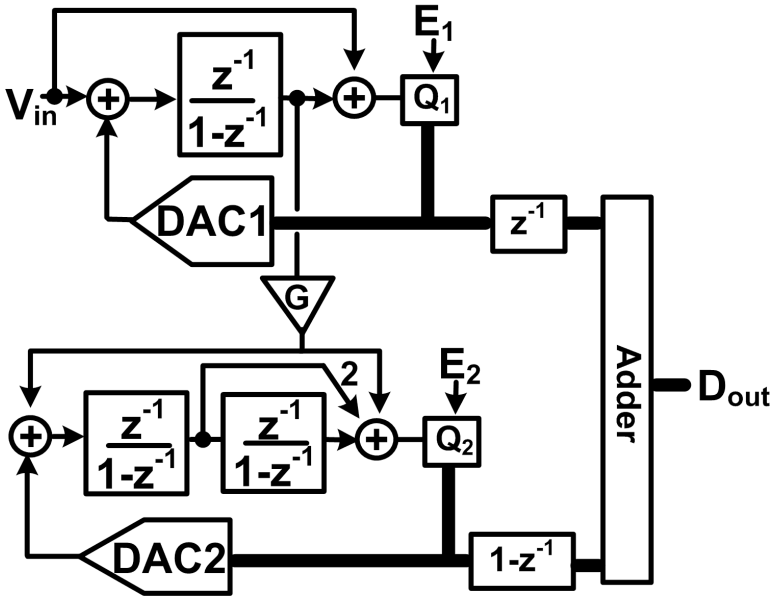

Figure 4.8: Traditional 1-2 MASH ADC

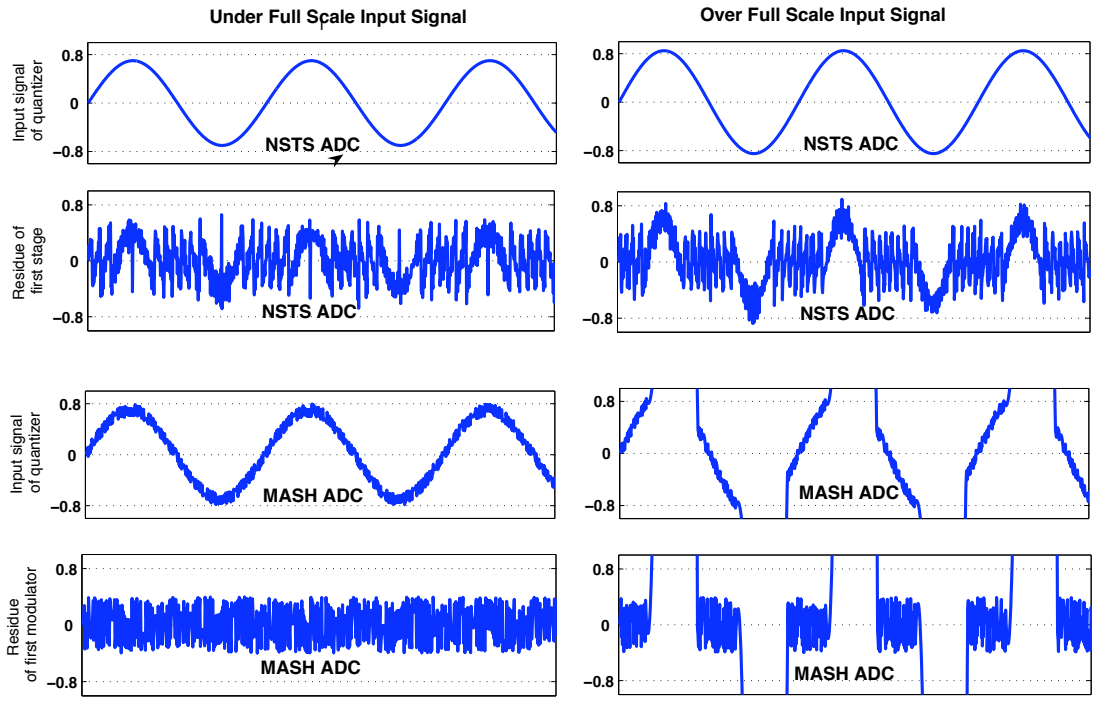

Figure 4.9: The swing of the internal nodes of the MASH and the NSTS ADCs for under and over full scale input signals

The proposed NSTS ADC can be considered as the counterpart of the MASH (cascaded) $\Delta\Sigma$ modulator since both architectures use multi-step quantization and ideally quantization noise of only last stage appears at the final output. Although, both architectures are prone to the first stage quantization leakage, the NSTS ADC has two main advantages over its MASH counterpart. First, the NSTS ADC requires only one amplifier for the two-step quantization and multi-order noise shaping, while in the MASH modulator, the number of the amplifiers is proportional to the order of noise-shaping. Moreover, the NSTS ADC requires no dedicated (active or passive) adder at the input of quantizers. Second, the NSTS ADC can process over full-scale input signals unlike its MASH counterpart. As

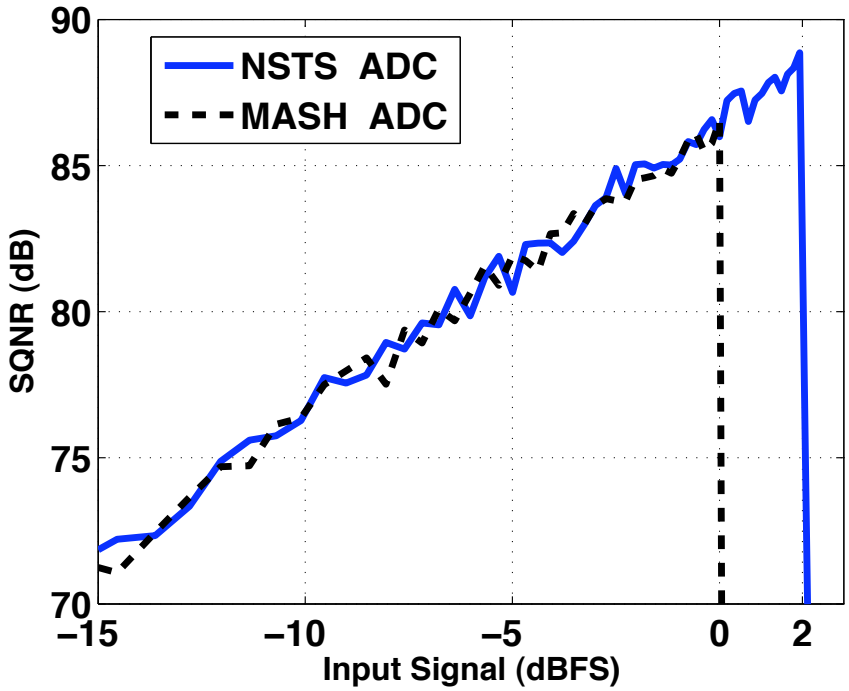

Figure 4.10: The SNDR plot versus the input signal in the MASH and the NSTS ADCs

mentioned earlier, the first quantizer of the NSTS ADC chops off the over full-range input signal and the redundancy between the two stages absorbs it. However, in the MASH modulator, the quantization of the first stage (E_1 which appears at the output of the integrator) limits the maximum input signal of the first quantizer and it does not allow over full-range operation.

A 3^{rd}-order MASH $\Delta\Sigma$ modulator (MASH 1-2) is shown in Fig. 4.8. This modulator requires three integrators and two dedicated adders at the input of the quantizers compared to the only amplifier of the NSTS ADC. The swing of internal nodes of this MASH modulator is compared with a third order NSTS in Fig. 4.9. Both 1-2 MASH modulator and the third-order NSTS ADC resolve similar number of the bits (3-bits in the first stage and 4-bits in the second stage).

In both architectures, the inter-stage gain is four and the built-in redundancy is extended by using four additional comparators in the second stage. In Fig. 4.9, voltage swings of the internal nodes of both architectures are shown for two cases: one with input signal less than the reference range and one with input signal higher than reference range. In the NSTS ADC, the over full-range voltage is chopped off as expected. Although the swing of the residue amplifier is increased, it is still within the reference range of the second stage. In the MASH modulator, the first loop filter is saturated when the input signal exceeds the reference range and redundancy between stages can not recover the distorted signal. The SNDR plot for both architectures is also shown Fig. 4.10. The NSTS ADC achieves higher SQNR (2dB) as a result of over full-range operation.

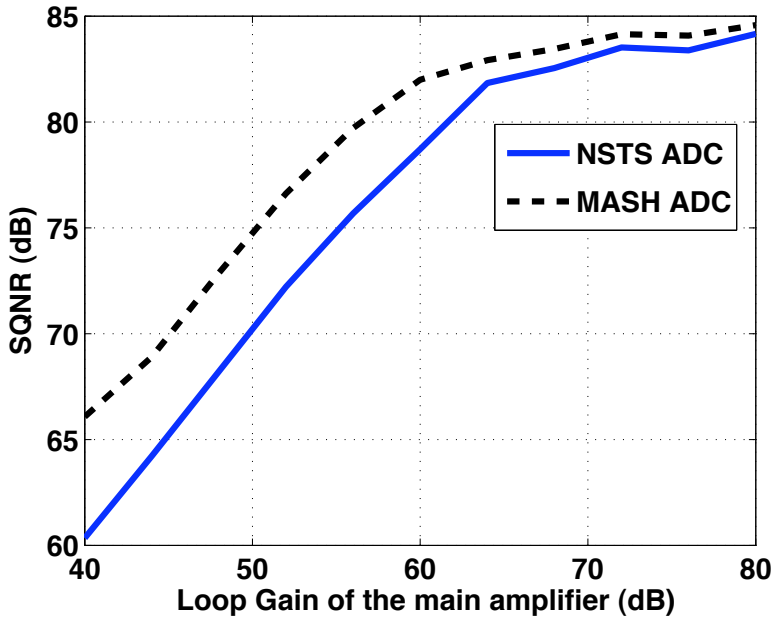

Figure 4.11: The SNDR plot versus the gain of the first integrator in the MASH ADC and the gain of the amplifier in the NSTS ADC

The loop gain requirement of the main amplifier (the first integrator in the MASH modulator and the residue amplifier in the NSTS ADC) is shown in

Fig. 4.11. This plot shows the SQNR of both architectures versus the loop gain of the main amplifier. The opamp gain requirement in both architectures is very similar as denoted earlier.

4.3.2 The cascaded NSTS ADC

NSTS ADCs can be cascaded as shown in Fig. 4.12 similar to the traditional $\Delta\Sigma$ modulators. This approach allows aggressive quantization of the input signal and very high orders of noise shaping for low OSR applications. The quantization of the second stage in the NSTS architecture is available in the analog form and it can be processed by another NSTS ADC. This allows cascading several NSTS ADCs with minimal hardware requirements. In the proposed architecture, the digital output of the back-end NSTS ADC is applied to a digital NTF (which is equal to NTF_1 of the front-end NSTS) and then is added with the digital output of the front-end NSTS. As a result, the quantization noise of the last stage appears at the output and quantization of all preceding stages is canceled out. This can be inferred from the following transfer functions

$$D_1 = V_{in} + E_1 \tag{4.9}$$

$$D_2 = -G_1E_1 + E_2 - G1H(z)E_2z^{-1} = -G_1E_1 + NTF_1E_2 \tag{4.10}$$

$$D_{1,2-out} = D_1 + \frac{D_2}{G_1} = V_{in} + \frac{NTF_1E_2}{G_1} \tag{4.11}$$

$$D_3 = -G_2E_2 + E_3 \tag{4.12}$$

$$D_4 = -G_3E_3 + E_4 - G_3H(z)E_4z^{-1} = -G_3E_3 + NTF_2E_4 \tag{4.13}$$

$$D_{3,4-out} = D_3 + \frac{D_4}{G_3} = -G_2E_2 + \frac{NTF_2E_4}{G_3} \tag{4.14}$$

$$D_{out} = D_{1,2-out} + \frac{NTF_1D_{3,4-out}}{G_2G_1} = V_{in} + \frac{NTF_1NTF_2}{G_1G_2G_3}E_4 \tag{4.15}$$

here, $D_{1,2-out}$, $D_{3,4-out}$ and D_{out} are the digital outputs of the first NSTS, the second NSTS and the cascaded modulator respectively. E_i and G_i represent the quantization noise and inter-stage gain of i^{th} stage. Moreover, NTF_1 and NTF_2 are the noise transfer functions of the first and the second NSTS ADCs respectively. In the cascaded modulators, imperfect cancellation of the quantization noise can limit overall accuracy. In the proposed architecture, only quantization leakage of the first stage (E_1) is important. This is because, any leakage from the second stage (E_2) is suppressed by $\frac{1}{G_1}$ and the third stage quantization (E_3) leakage is both shaped by NTF_1 and suppressed by ($\frac{1}{G_1 G_2}$). In this architecture, the design requirements of all stages (except the first stage) is relaxed due to inter-stage suppression and noise shaping. It is apparent from the digital output expression (4.15) that the final

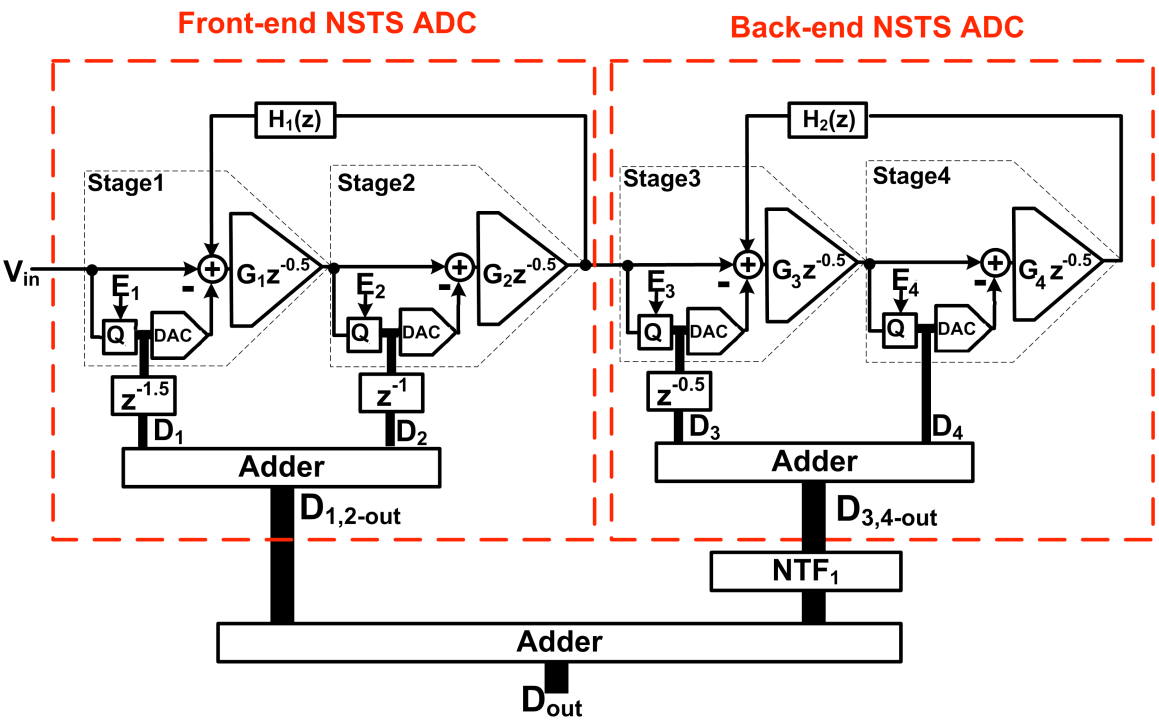

Figure 4.12: The proposed cascaded NSTS ADC

quantization noise is greatly suppressed by the inter-stage gain product ($\frac{1}{G_1 G_2 G_3}$)

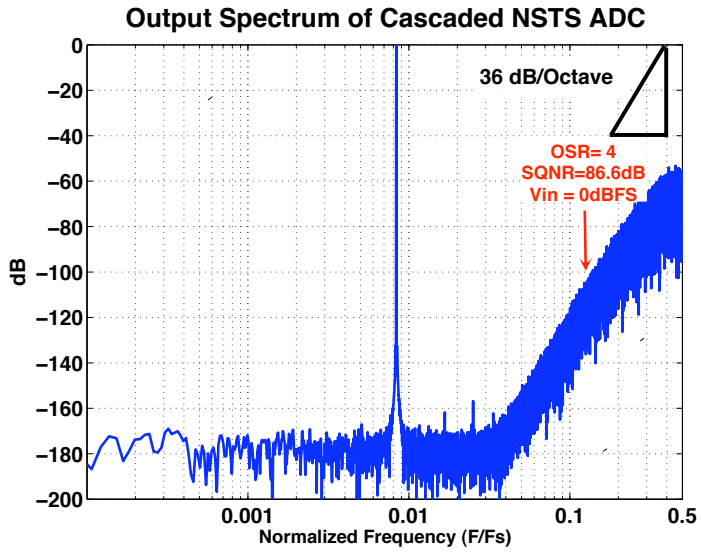

Figure 4.13: The spectrum of the cascaded NSTS ADC

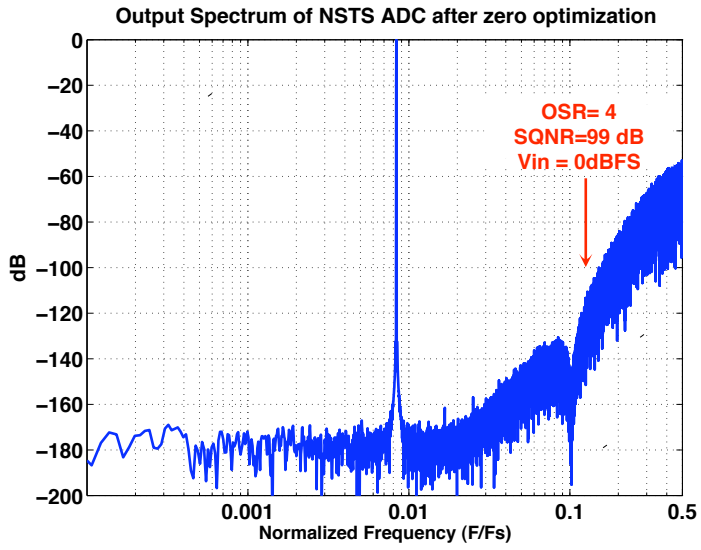

Figure 4.14: The spectrum of the cascaded NSTS ADC after zero optimization

and aggressively shaped by the noise shaping product (NTF_1NTF_2). For instance, the overall SQNR of a two cascaded NSTS ADCs with 10-bit quantization and 6^{th} order noise shaping (3^{rd} order each stage) is 86dB (for full scale input signal)

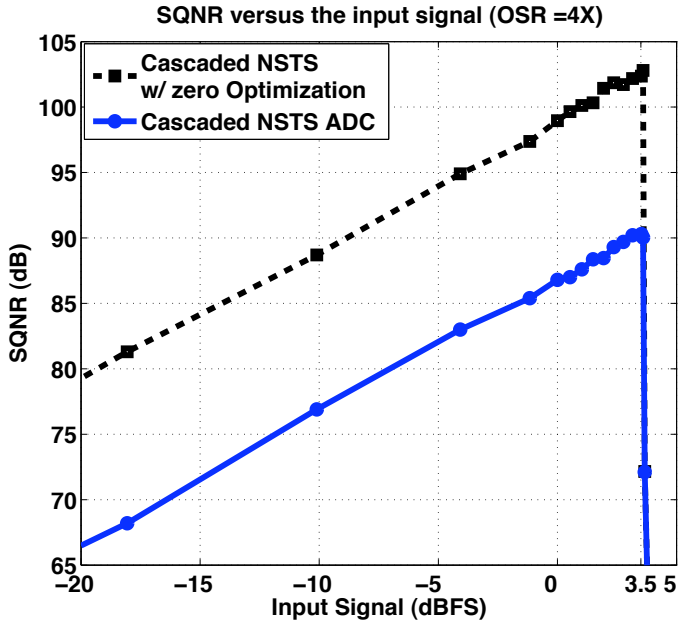

Figure 4.15: The SQNR plot of the cascaded NSTS ADC versus input signal (dBFS)

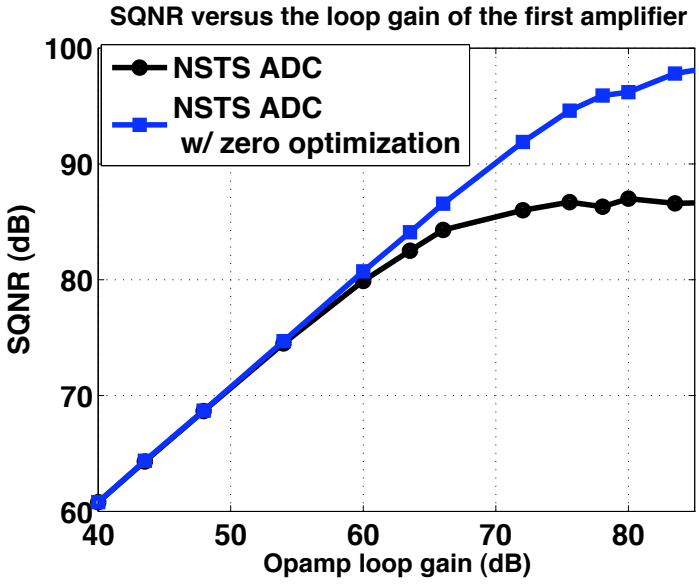

Figure 4.16: The SQNR plot versus the loop gain of the amplifier in the front-end NSTS ADC

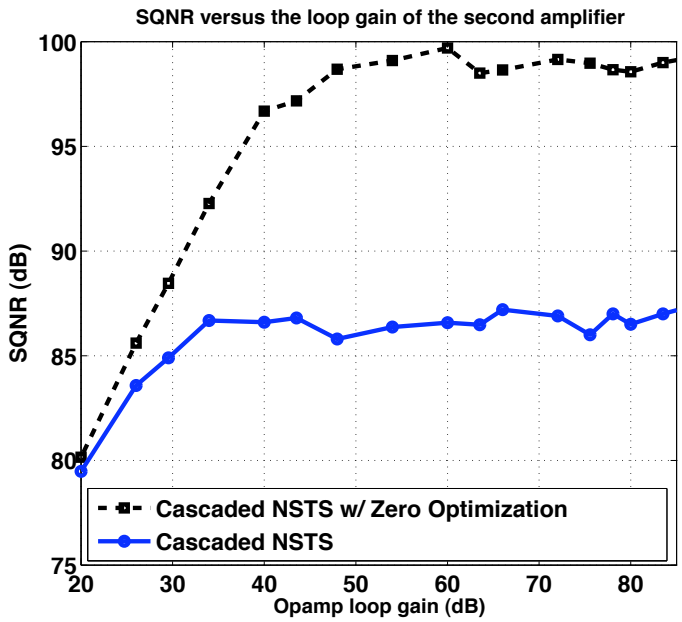

Figure 4.17: The SQNR plot versus the loop gain of the amplifier in the back-end NSTS ADC

at OSR of only 4. The output spectrum for this example is shown in Fig. 4.13. Zero optimization can be employed to improve the performance further. This can be done simply by changing the coefficients of $H(z)$ in the back-end NSTS ADC. The zero optimization increases the SQNR to 99dB at 4X OSR (Fig. 4.14). Although, the overall order of noise shaping is very high, this architecture still benefits from over full-range operation of the NSTS ADC. This is because the noise shaping properties and signal processed by the front-end NSTS ADC remain unchanged. The SQNR of the proposed cascaded NSTS ADC is shown versus the input signal in Fig. 4.15. In this example, the frond-end NSTS ADC benefits from 2.5-bits redundancy between stages and can accommodate up to 3.5 dB over full range input signal. This architecture needs only two amplifiers to achieve this performance: one in the first NSTS ADC and one in the second NSTS ADC. The

loop gain requirements of these two amplifiers is plotted in Fig. 4.16 and Fig. 4.17. The loop gain requirement of the amplifier in the front-end NSTS for 80dB SQNR at 4X OSR is around 60dB. The gain requirement of the amplifier in the back-end NSTS is very relaxed. It requires less than 30dB loop gain for +80dB SQNR.

4.4 The enhanced HDSP ADC with NSTS quantizer

Properties of the NSTS ADC and its features at low OSRs is studied in the previous section. Simple implementation of the standalone and cascaded NSTS ADCs makes these architectures an inevitable candidate for the low OSR applications. In this section, application of the NSTS ADC as the quantizer of a single-loop $\Delta\Sigma$ modulator is studied.

The HDSP modulator (Fig. 4.18), introduced in the previous chapter, employs a pipelined ADC as the quantizer of a single-loop $\Delta\Sigma$ modulator. In this architecture, the integrators have relaxed design requirements. Hence, the loop filter plays a less significant role in the overall power consumption compared to the pipelined quantizer and simplifying the quantizer greatly can improve the power efficiency.

The two-step ADC is the simplest form of the pipelined ADC. Hence, the NSTS ADC can replace the pipelined ADC in the HDSP modulator. The noise shaping properties of the NSTS ADC can be merged with the noise shaping of the HDSP modulator. This allows design of higher order HDSP modulator with minimum hardware requirements and with improved power efficiency.

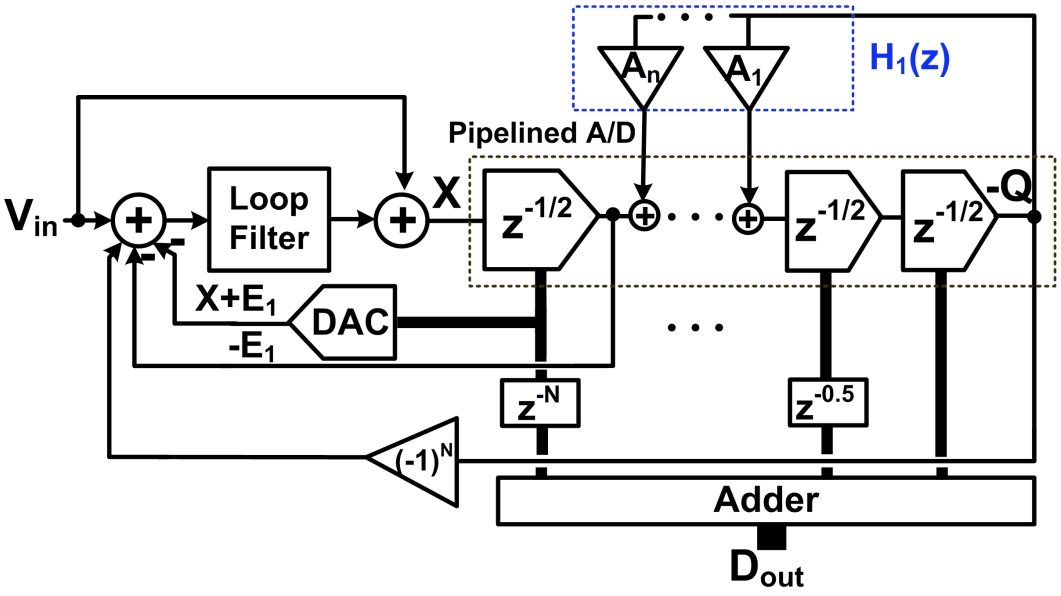

Figure 4.18: The conventional Hybrid Delta-Sigma/Pipelined (HDSP) ADC

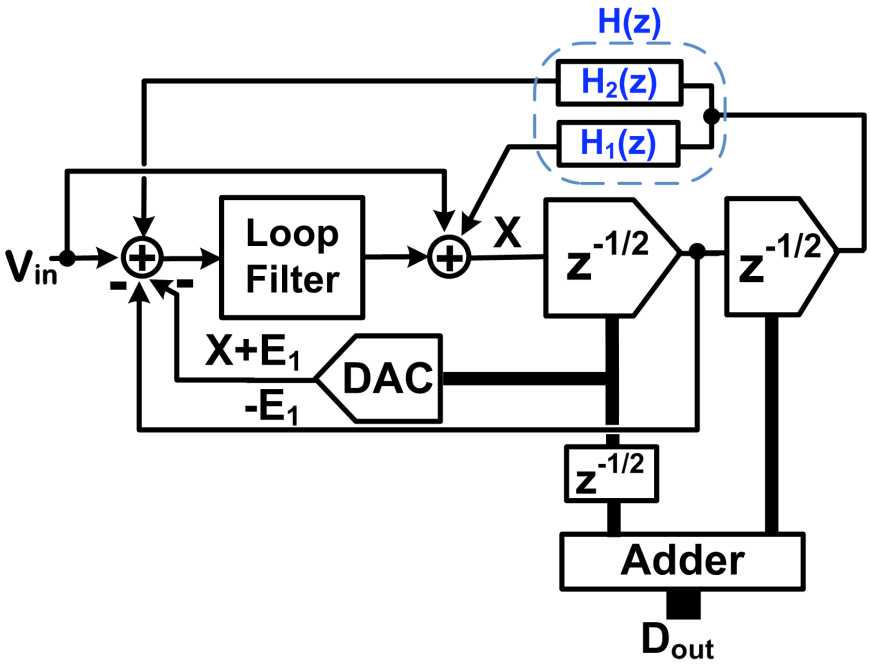

Figure 4.19: The enhanced HDSP ADC using the NSTS quantizer

4.4.1 The enhanced HDSP ADC

One possible realization of an enhanced HDSP modulator is shown in Fig. 4.19. This modulator uses a NSTS ADC as a quantizer. The feedback transfer function of the NSTS quantizer ($H(z)$ in Fig. 4.1.b) is split into two transfer functions ($H_1(z)$ and $H_2(z)$). $H_1(z)$ is fed back to the input of the NSTS quantizer while $H_2(z)$ is fed back to the input of the first integrator. The Noise transfer function of the enhanced HDSP modulator is:

$$H_1 = A_1 z^{-1} + A_2 z^{-2} + ... \tag{4.16}$$

$$H_2 = B_1 z^{-1} + B_2 z^{-2} + ... \tag{4.17}$$

$$NTF_{EnhancedHDSP} = ((1 - z^{-1})^L - 1)(-z)^{-N} H_2 + H_1 + 1 = (1 - z^{-1})^{L+N+M} \tag{4.18}$$

This can be compared with the NTF of the original HDSP modulator which was

$$NTF_{HDSP} = ((1 - z^{-1})^L - 1)(-z)^{-N} + 1 + H_1 = (1 - z^{-1})^{L+N} \tag{4.19}$$

Here, N is the latency of the pipelined ADC, L is the order of filter and M is the number of delays introduced in $H_2(z)$. The maximum order of noise shaping in the original HDSP modulator is directly proportional to the order of the loop filter and the number of pipelined stages. This means at least $N + L$ amplifiers are required for $N + L$ order noise shaping. In the enhanced HDSP modulator, only two pipelined stages are used and N is only $\frac{1}{2}$. However, the order of noise shaping is proportional to M as well as $N + L$. These delays (which can be generated by a passive FIR network) increase the order of noise shaping in the enhanced HDSP modulator without using any extra amplifier. In theory, the enhanced HDSP modulator is flexible enough to accommodate large number of delays in the

quantization path, since H_1 and H_2 can be chosen freely to form the desired NTF. Moreover, the quantization noise is very small and stability can be guaranteed for high order noise transfer functions. The enhanced modulator improves the power efficiency and the noise shaping properties of the HDSP architecture while it preserves all other properties of the original HDSP.

Unlike the standalone or cascaded NSTS ADC, the enhanced HDSP modulator is not sensitive to the quantization noise leakages. This is because, any error generated by the first stage of NSTS is processed by the loop filter and is shaped. This includes the gain error of the amplifier in the NSTS quantizer, noise (thermal and flicker) generated by the first MDAC, feedback and sampling capacitors mismatch, the non-linearity of the first DAC in the NSTS. On other hand, the cascaded NSTS ADC uses two or more NSTS quantizers. Hence, it can provide higher orders of noise shaping and more aggressive quantization compared to the enhanced HDSP modulator. Properties of the cascaded NSTS ADC and the enhanced HDSP ADC are compared in Table I.

4.4.2 Design example

The relaxed design requirements of the loop filter and NSTS quantizer allows low power and low voltage design of the enhanced HDSP modulator. Power efficient implementation of the HDSP modulator will be discussed here. Detailed schematic of a 4^{th} order, 7-bit enhanced HDSP modulator is shown in Fig. 4.20. The second order loop filter, the half delay of the two-step quantizer and the additional 1.5 clock cycle delays in the quantization (provided by path $H_2(z)$) together

Table 4.1: The cascaded NSTS ADC versus the enhanced HDSP modulator

	The Cascaded NSTS ADC (Fig. 4.12)	**The Enhanced HDSP ADC (Fig. 4.19)**
Number of NSTS ADCs	**Two NSTS ADCs**	**One NSTS quantizer**
Order of the individual NSTS ADC	M^{th} **order**	M^{th} **order**
Resolution of the individual NSTS ADC	B **bits**	B **bits**
Order of the loop filter	**Not Applicable**	L^{th} **order**
Overall order of noise shaping	$2M$	$M + L$
Total number of amplifiers	**2 (1 per each NSTS)**	**1+L**
Overall number of the resolved bits	$2B - 1$	B
Loop gain requirements of opamps	**High for the First NSTS /Low for the second NSTS**	**Low for the Loop Filter / Low for the NSTS**
Design Example	$B = 6$, $M = 3$	$B = 6$, $L = 2$ **and** $M = 3$
Overall order of noise shaping	**6**	**5**
Total number of amplifiers	**2**	**3**
Overall number of the resolved bits	**11**	**6**
OSR	**4**	**8**
SQNR	**90dB**	**85dB**
Loop gain requirements of opamps	**65dB for the First NSTS /20dB for the second NSTS**	**20dB for the Loop Filter / 30dB for the NSTS**

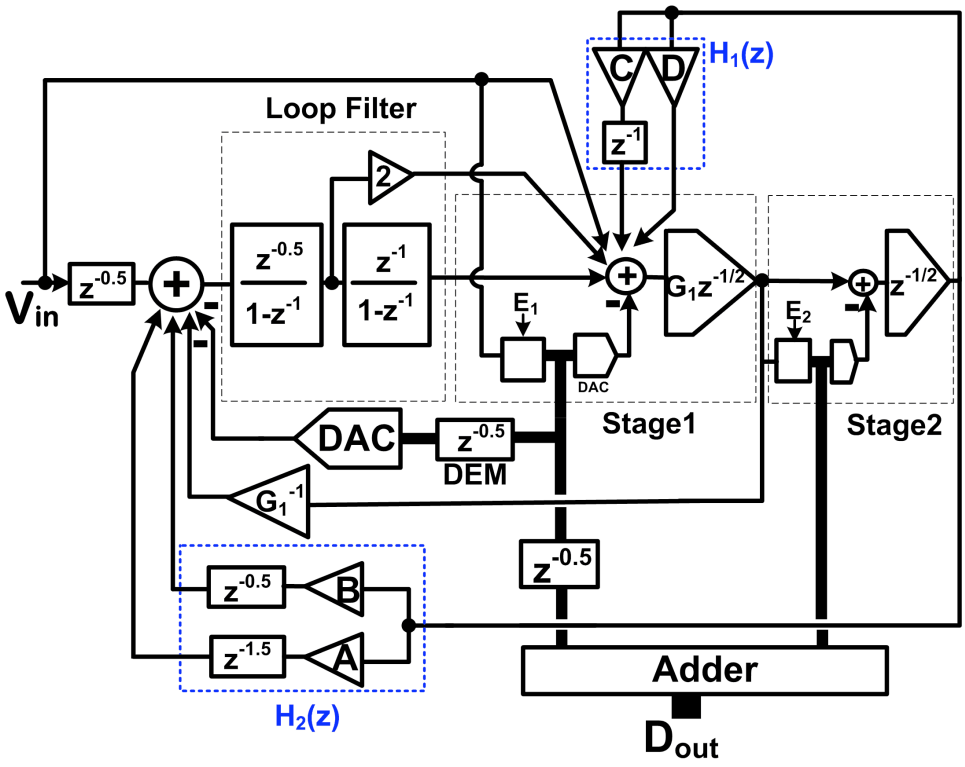

Figure 4.20: The detailed realization of the enhanced HDSP ADC

yield an overall fourth order NTF. Compared to the HDSP modulator in previous chapter, the order of noise shaping is increased from 3 to 4, while the number of the amplifiers are reduced from 4 to 3. This reduces the power consumption significantly. Four feedback paths (A, B, C, D) provide all the delaying terms needed in the noise transfer function as following

$$NTF = G_1((A-C)z^{-4} + (-2A+B+2C-D)z^{-3} + (2D-2B-C)z^{-2} - Dz^{-1}) + 1 \tag{4.20}$$

One feature of this design is the simplicity of the zero optimization. Zero optimization can be done only by tweaking the coefficient D. This is because D appears in z^{-1}, z^{-2} and z^{-3} terms in the NTF.

Power efficiency of the proposed HDSP ADC can be further improved by

reducing the supply voltage. Relaxed gain and swing requirements of the HDSP modulator [49] make this architecture a good candidate for low voltage operation. The only concern is the full range swing of the residue amplifier in the pipelined quantizer. In the HDSP modulator, the inter-stage gain of the first pipelined stage and the references of the second stage sub-ADC are halved. This will accordingly reduce the swing of this amplifier to half without reducing the effective number of resolved bits. Hence, all the amplifiers in the HDSP modulator can operate at very low supply voltages. In order to preserve the DR of the modulator at a reduced analog supply voltage, the DAC and comparator references are increased beyond the supply voltage by 20 percent. Thanks to the NSTS quantizer, the HDSP modulator can accommodate over full-range input signals and benefit from maximum available DR. Swing of all internal nodes of the HDSP modulator is considerably less than the supply voltage even with increased references. This is shown in Fig. 4.21.

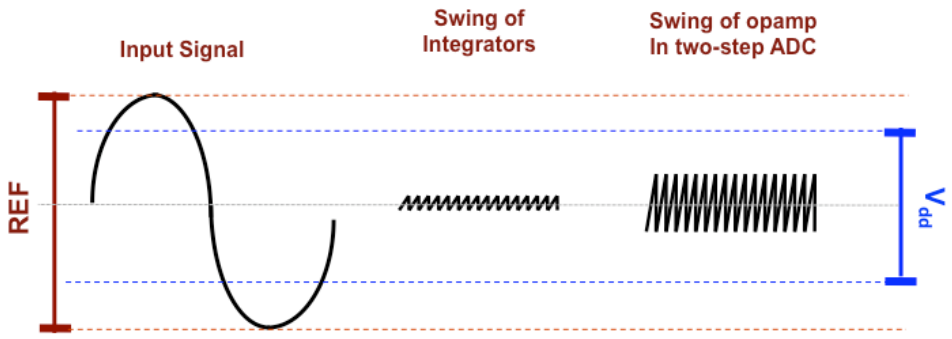

Figure 4.21: The swing of internal nodes of the enhanced HDSP modulator

Table 4.2: Summary of measurement results

Analog Supply(V)	**1.2**
Input Range (Diff)	**3.1 Vpp**
Comparator Reference voltage	**1.47 V**
OSR	**8**
SFDR (dB)	**87.5**
DR (dB)	**78**
SNDR (dB)	**75**
Analog Power Consumption (mW) (Resistor ladder is excluded)	**2.6mW**
Digital Power/Digital Supply	**3.75mW/1.5V**
Signal Bandwidth/Sampling Rate	**1.56 MHz /25 MHz**
Core Area	**3.79** mm^2

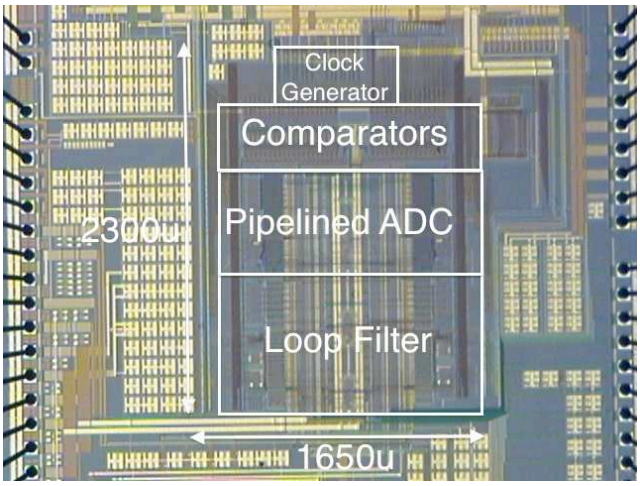

Figure 4.22: Die Micrograph

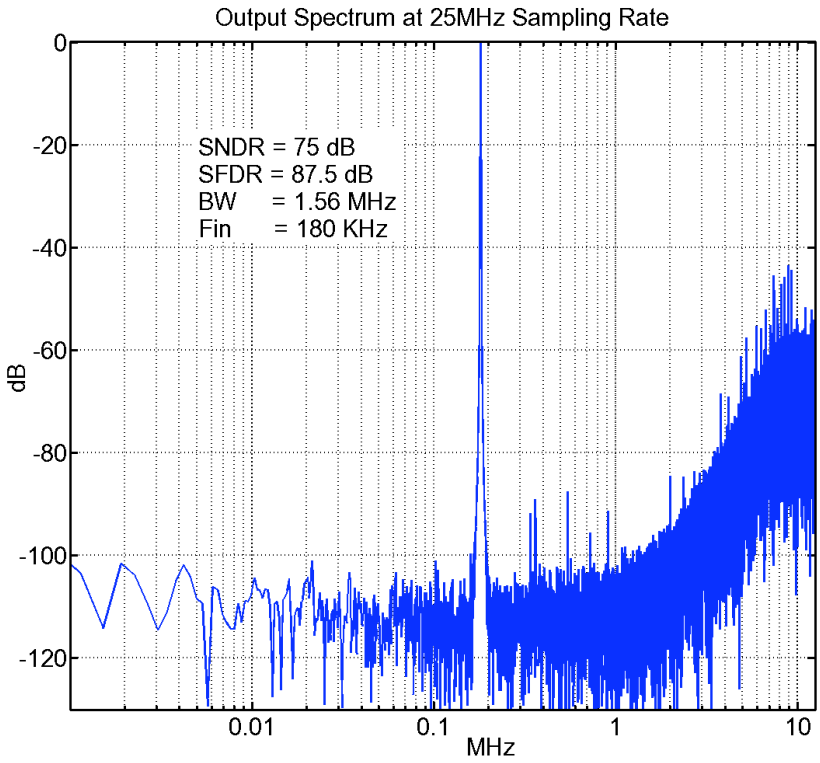

Figure 4.23: The output spectrum of the ADC

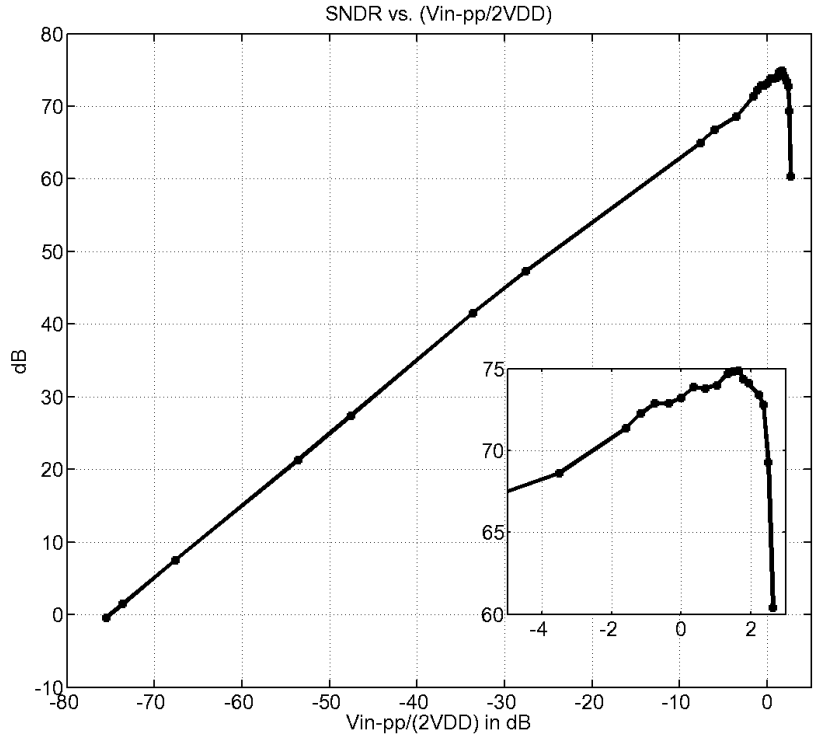

Figure 4.24: SNDR Plot

4.4.3 Measurement results

The prototype of the enhanced HDSP modulator is fabricated in a 0.18 μm process [52]. Shown in Fig. 4.22 is the die photograph. Measured output spectrum and SNDR plot are shown in Fig. 4.23 and in Fig. 4.24. The measurement results are summarized in Table II. This ADC can be used in moderate BW wireless applications. Compared to the HDSP modulator in [26], the analog supply voltage of this enhance HDSP modulator is reduced (from 1.8 V) to 1.2 V while the input signal range is increased (from 1.8 V_{pp}) to 3.1 V_{pp}. Hence, in the enhanced HDSP implementation, the maximum input signal is about 2 dB greater than the analog

supply voltage. In this prototype, the extended input signal range and higher order of noise shaping preserve and enhance the overall accuracy. The simplified design and low voltage operation of the proposed HDSP modulator make this architecture a feasible power efficient candidate for wireless applications.

4.5 Summary and Conclusions

In this chapter, a noise shaped two-step (NSTS) ADC is presented. This ADC requires only one residue amplifier for high orders of noise shaping (e.g. third order) and aggressive quantization of the input signal (e.g. 7-8 bits). This ADC can also achieve high DR since it can process input signal larger than reference voltage. The NSTS ADC can be configured as a standalone ADC, as a cascaded $\Delta\Sigma$ modulator or as the quantizer of the HDSP modulator. These configurations are studied and compared in this paper. The common feature of all these configurations is the design robustness and simplicity which makes the NSTS architecture an inevitable candidate for low OSR and low power applications.

Finally, the NSTS ADC is also flexible enough to adopt performance enhancement techniques which is normally employed in the nyquist rate pipelined ADCs (e.g. digital calibration, gain enhancement techniques, ...) and in $\Delta\Sigma$ modulators (e.g. zero optimization).

CHAPTER 5. A NOISE-SHAPED PIPELINED ADC WITH REDUCED SENSITIVITY TO ANALOG IMPERFECTIONS

5.1 Introduction

In previous chapters, new ADC architectures for oversampling applications were introduced. These methods merge the aggressive quantization of the pipelined ADC with the noise shaping properties of the delta-sigma modulators. In these architectures, the focus was on reducing the in-band quantization noise without increasing design complexity.

In this chapter, a different approach is studied which still benefits from the low in-band quantization noise, provided by the combination of the pipelined and delta-sigma ADCs. However, it mainly focuses on reducing the overall sensitivity to the analog imperfections like the opamp gain error and the capacitor mismatch. In the proposed architecture, noise shaping is exploited both in the front-end and the back-end stages of a pipelined ADC. A new pipeline front-end stage is introduced which uses a delta-sigma modulator as its sub-ADC. As a result, the shaped quantization noise is processed by the front-end stage and MDAC analog imperfections are attenuated. The NSTS ADC is used as the back-end stage to suppress the final quantization noise power. The prototype ADC is fabricated in 0.18μm CMOS technology.

This chapter is organized as following: In section 5.2, the noise-shaped pipeline stage (NSPS) is introduced. The proposed noise-shaped pipelined ADC is presented in section 5.3. In section 5.4, the circuit realization is provided. The measurement results and conclusions are given in sections 5.5 and 4.5.

5.2 The proposed Noise-Shaped Pipeline Stage (NSPS)

Errors from the front-end stages usually limit the overall accuracy of the pipelined ADC. The noise shaping properties of delta-sigma ADCs can be used to reduce the sensitivity to the imperfections of the front-end stages. This possibility will be studied in this section.

5.2.1 The proposed noise-shaped pipeline stage

Fig. 5.1 shows the systematic realization of the noise-shaped pipeline stage (NSPS) in comparison with a conventional pipeline stage. In both cases, the circuit is used as the front-end stage of a pipelined ADC. In the conventional stage, the sub-ADC quantizes the input voltage (V_{in}), and the DAC converts its digital output to an analog signal. Finally, the quantization noise (E) is extracted and multiplied by the inter-stage gain (G). In the conventional pipeline stage, any error from the residue amplifier makes the output residue ($V_o = -G.E$) inaccurate, and causes harmonic distortion.

In the proposed stage, the sub-ADC is a simple delta-sigma quantizer. Its output signal is applied to a passive low-pass filter and converted to analog form by the DAC. The input signal (V_{in}) is also low-pass filtered. The difference between

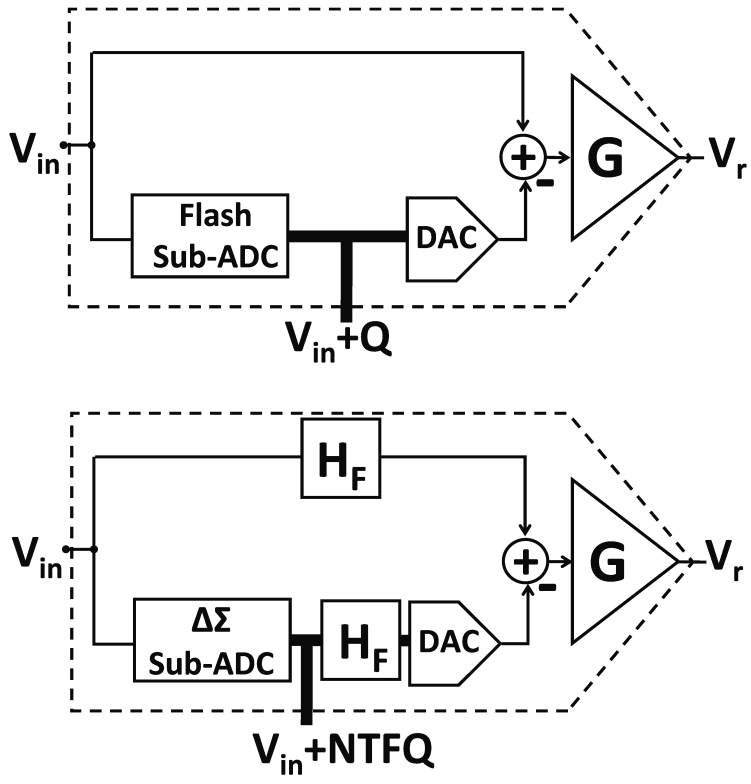

Figure 5.1: Front-end stages in a pipelined ADC: a) conventional stage; b) the proposed noise-shaped pipeline stage (NSPS)

the DAC output voltage and the filtered input signal is amplified by the inter-stage gain G. The output of the residue amplifier is given by

$$V_o = -(H_F NTF)GE \tag{5.1}$$

In (5.1), H_F and NTF denote the frequency response of the low-pass filters and the noise transfer function of the delta-sigma modulator, respectively. The output residue of the NSPS is the shaped quantization noise. As a result, the power of the in-band quantization noise is reduced, and the noise due to gain error and nonlinear distortion is suppressed. Thus it becomes possible to use a residue amplifier with low-to-moderate gain requirements even in high precision pipelined ADCs. The high-pass NTF of the delta-sigma modulator amplifies the out-of-band quan-

tization noise. The role of the low-pass filter H_F in the NSPS is to suppress the out-of-band quantization noise, and to prevent the overload of the amplifier. The low-pass filter should be used both in the signal path and the sub-ADC path so that the input signal V_{in} is processed identically in both paths. A possible choice for low-pass filter is the FIR filter with the transfer function

$$H_{filter} = \frac{(1+z^{-1})^N}{2^N} \tag{5.2}$$

Here, N is determined by the order of the noise-shaping. Note that this FIR semi-sinc filter is not used here for decimation, only to realize N zeros at $\frac{f_s}{2}$, and to suppress the out-of-band quantization noise. In an NSPS with an Nth-order $NTF = (1-z^{-1})^N$ and Nth order FIR filter, the output of the residue amplifier becomes

$$V_o = -\frac{(1-z^{-2})^N}{2^N} GE \tag{5.3}$$

The transfer function in (5.3) has N zeros at DC, and N zeros at $\frac{f_s}{2}$. The peak value of the frequency response of V_o is $V_{omax} = GE$, the same as for a conventional stage. Thus, the output overload conditions remain the same in the NSPS as in the conventional stage.

5.2.2 Error suppression in NSPS

As mentioned earlier, the main feature of the NSPS is the reduced sensitivity to analog imperfections. This includes sensitivity to any error which changes the inter-stage gain from its nominal value. The complete transfer function for the output voltage of MDAC is

$$V_{out} = GE = -\frac{C_S}{C_F}\frac{\beta A_{DC}}{1+\beta A_{DC}}(1-e^{-\frac{t}{\tau}})E \tag{5.4}$$

here, C_S and C_F are the sampling and feedback capacitors. β is the feedback factor, A_{DC} is the dc gain of the amplifier, and τ is the time constant of the amplifier. Mismatch between capacitors(C_F and C_S), finite DC gain of the opamp and settling error make the inter-stage gain inaccurate and causes static or dynamic settling error. In the proposed architecture, the shaped quantization noise is processed by the MDAC and the output expression is changed to

$$V_{out} = -\frac{C_S}{C_F}\frac{\beta A_{DC}}{1+\beta A_{DC}}(1-e^{-\frac{t}{\tau}})\frac{(1-z^{-2})^N}{2^N}E \tag{5.5}$$

This expression has N zeros at DC. Hence, the in-band quantization noise is shaped. Additionally, both static (opamp DC gain error, capacitor mismatch) and dynamic (settling) errors are shaped.

Nonlinear inter-stage gain error is also suppressed in this architecture. The rms power of the MDAC output signal (V_{out}) is significantly reduced compared to the traditional pipeline MDAC. Hence, its respective nonlinear distortion power is attenuated as well. However, this holds only when both in-band and out-of-band quantizations are shaped. Shaping just in-band quantization (i.e. when using a delta-sigma sub-ADC without a low-pass filter) increases the out-of-band rms quantization power and consequently the overall nonlinear distortion power. Simulation results show that first order in-band and out-of-band noise shaping ($\frac{1-z^{-2}}{2}$) reduces the overall rms quantization power by a factor of 1.7 while first order in-band noise shaping ($1-z^{-1}$) increases the rms quantization noise power by a factor of 2. The output spectrum and swing of these two cases is compared with a regular pipeline stage in Fig. 5.2.

To demonstrate the effectiveness of the proposed NSPS, Matlab simulations have been performed on the proposed NSPS and the conventional pipeline input stage. The sub-ADC used in stages resolves 3.5 bits. In both cases, the input

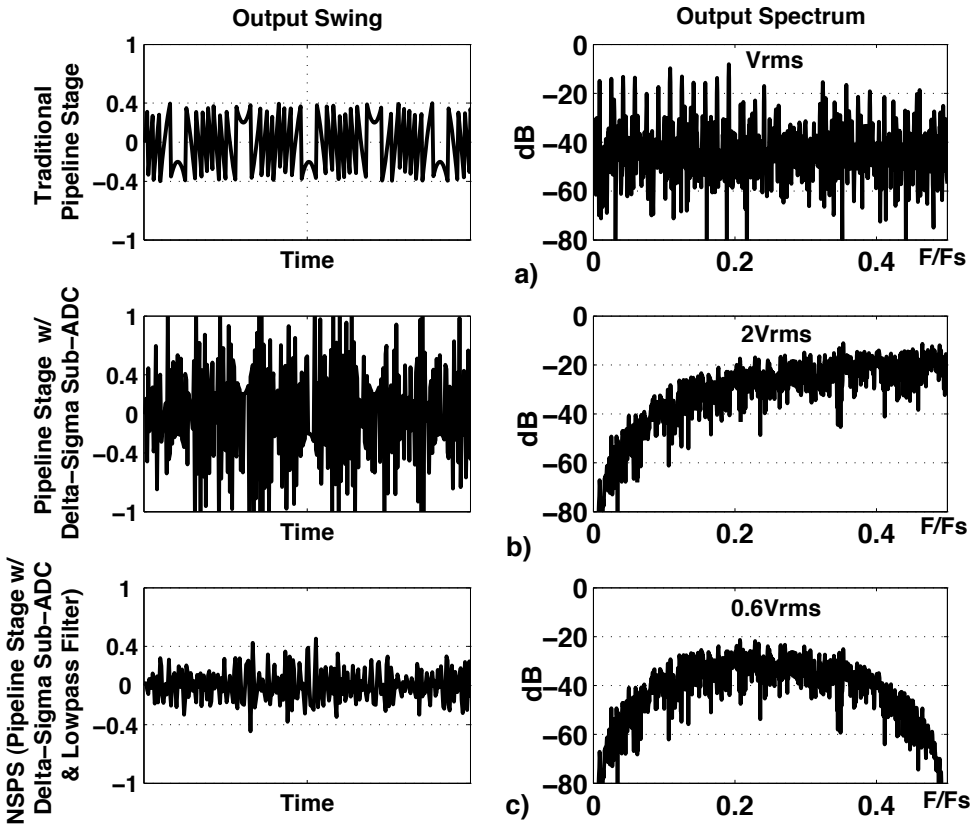

Figure 5.2: The MDAC output voltage and spectrum: a) Traditional pipeline stage; b) Pipeline stage w/ delta-sigma sub-ADC and without low-pass filter c) The proposed NSPS utilizing both delta-sigma sub-ADC and low-pass filter

stage is followed by an ideal back-end ADC, to study only the front-end effects. The residue amplifier was assigned a nonlinear DC gain, such that effective loop gain changes from $40dB$ to $28dB$ when its input voltage swings from $0.6V_{omax}$ to V_{omax} , and from $-0.6V_{omax}$ to $-V_{omax}$. For input voltages between $-0.6V_{omax}$ and $+0.6V_{omax}$, the effective loop gain is $40dB$. The output spectra of the ADC are shown in Fig. 5.3 for the NSPS with first- and second-order noise shaping, and for the conventional stage. Clearly, harmonics caused by the nonlinear opamp gain are suppressed efficiently in the NSPS, even at low OSRs. At an OSR of only 4, and

with nonlinear opamp gain, the SNDR is $73dB$ for the first-order NSPS, and $80dB$ for the second-order one. The conventional stage gives only $62dB$. At $OSR = 8$, the $SNDR$ is $78dB$ and $91dB$ for the first-order and the second-order NSPS, respectively, while for the conventional stage $SNDR = 66dB$. These simulation results show that even low order (1^{st} or 2^{nd} order noise shaping) can provide enough error suppression.

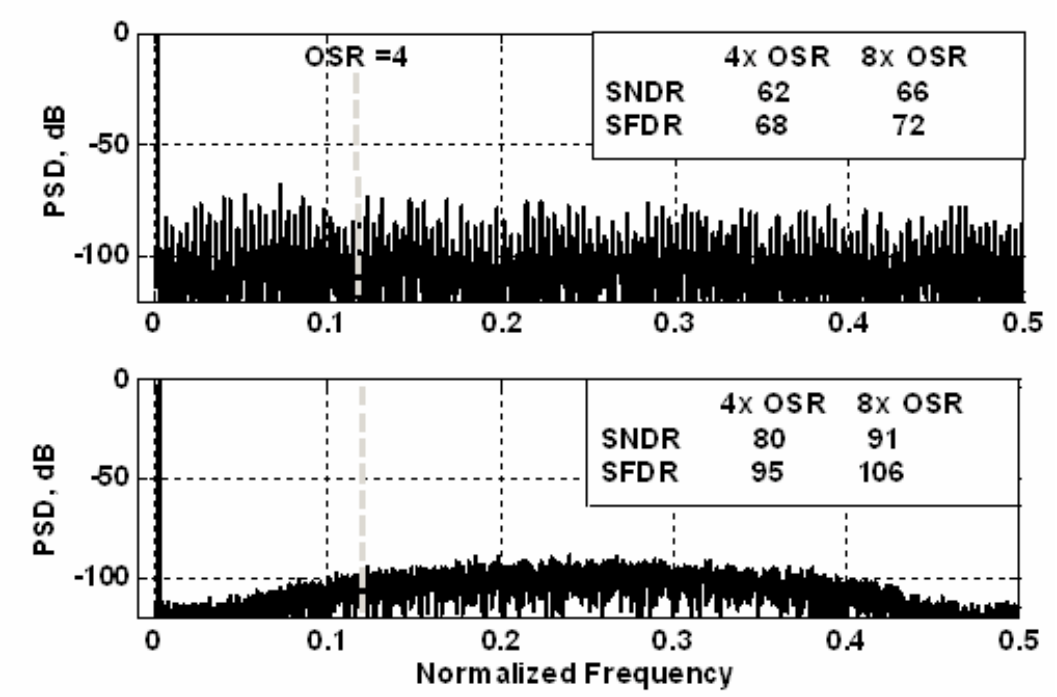

Figure 5.3: Output spectrum of ADC with traditional and NSPS front-end stages (Nonlinear gain is assigned to opamp)

The proposed technique does not suppress thermal/flicker noise and the front-end DAC nonlinearity since the former is independent of MDAC output voltage and the later is function of both input signal and quantization noise. The thermal/flicker noise and DAC linearity requirements are the same as conventional pipeline stage and it benefits from oversampling. Data Element Matching (DEM) can be used for the front-end DAC similar to the traditional delta-sigma modula-

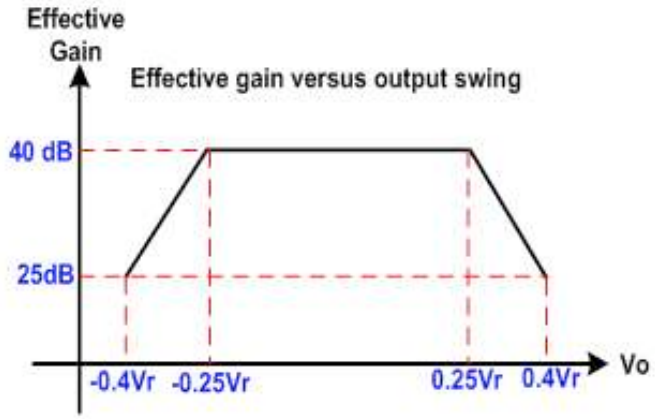

Figure 5.4: Gain of the opamp used in Fig. 5.3 vs output swing of the opamp

tors. DEM can operate in the non-overlapping time between the sampling and the amplification phases.

5.2.3 Design requirements of the delta-sigma sub-ADC

The role of the delta-sigma sub-ADC is the coarse quantization of the input signal. Any error generated by the delta-sigma sub-ADC appears at the digital outputs of the NSPS stage. This error also appears at the output residue and consequently digital outputs of the succeeding stage. Hence, it is canceled out at the final digital output which is weighted sum of the digital outputs of all stages. The sub-ADC errors are modeled with E_{SA} in Fig. 5.5 and following transfer functions shows how E_{SA} is canceled at the output

$$\frac{D_1}{E_{SA}} = 1 \tag{5.6}$$

$$\frac{D_2}{E_{SA}} = -G \tag{5.7}$$

$$\frac{D_{out}}{E_{SA}} = \frac{D_1 + \frac{D_2}{G}}{E_{SA}} = 0. \tag{5.8}$$

E_{SA} refers to any error generated by the delta-sigma sub-ADC including gain error, the coefficient mismatch, thermal/flicker noise, nonlinearity of the DAC in the delta-sigma sub-ADC. Hence, the delta-sigma sub-ADC has very relaxed loop filter design requirements and it can be implemented with minimum power dissipation and area consumption.

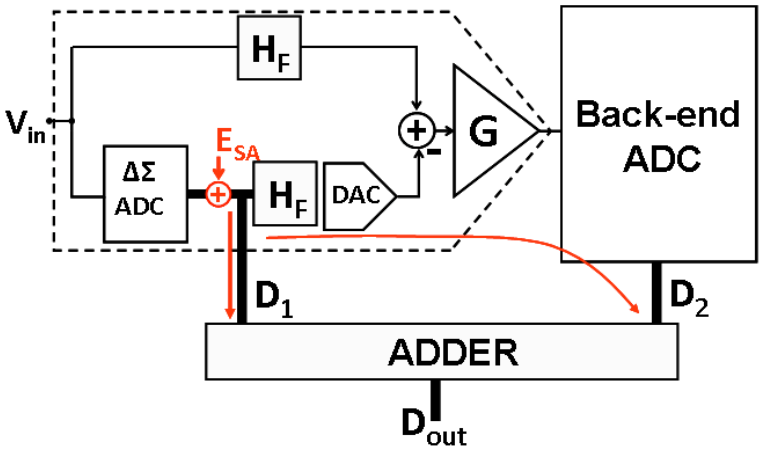

Figure 5.5: Modeling sub-ADC errors in NSPS

5.2.4 Design requirements of the FIR filter

As mentioned earlier, the FIR filter plays an essential role in NSPS since it prevents the opamp overload, reduces the rms quantization power at the output and consequently suppress the nonlinear distortion power. The FIR filter should be chosen such that magnitude of $(H_F(z)NTF)$ product does not exceed 0dB over the (0 to $\frac{F_s}{2}$) frequency range. A potential choice for FIR filter is the $H_F(z)$ in 5.4. The minimum order of the FIR filter (N in 5.4) should the same as order of the delta-sigma ADC to ensure the magnitude of $(H_F(z)NTF)$ product is equal to or less than 0dB. Although identical FIR filters are used in the signal and the sub-

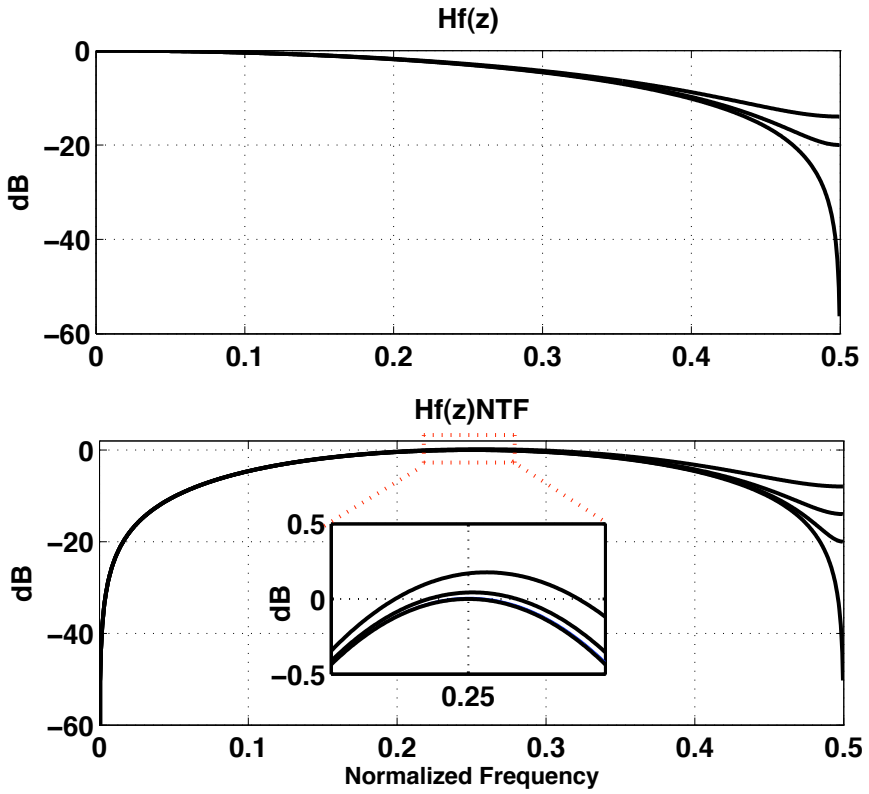

Figure 5.6: Effect of mismatch between filter coefficients on the filter transfer function and the transfer function of NSPS output residue

ADC paths, matching between the filters is not critical. A fraction of input signal (V_{in} in Fig. 5.1) appears at MDAC output as a result of the mismatch between two FIR filters. However, this will only increase the MDAC output swing slightly without degrading the overall performance. The low-pass transfer function of the FIR filter contains several delaying terms ($H_F = A_0 + A_1 z^{-1} + A_2 z^{-2} + ...$). The weighted sum of filter coefficients ($A_0 + A_1 + ...$) should be accurate enough (e.g. 1 percent matching for +12 bit accuracy), since it determines the inter-stage gain. However, the mismatch between coefficients (A_1, A_2,...) only changes the location of the zeros of the filter and degrades the high frequency noise shaping as shown

in Fig. 5.6. In this figure, ideal first order transfer function ($H_F(z)NTF$ product) is compared to a case with 10 and 20 percent mismatch between filter coefficients. Although high frequency noise shaping is degraded, the maximum magnitude of the $H_F(z)NTF$ product increases only slightly (0.2dB) even for the large coefficient mismatches. Hence, the coefficients have relaxed matching requirements. Passive realization of the FIR filter with minimum power penalty is possible. The delaying terms of $H(z)$ can be generated by sampling the input signal in the alternate clock phases. The complexity of the SC network (realizing the coefficient of the FIR filter) is minimal for the first and the second order architectures.

5.3 The proposed noise-shaped pipelined ADC

A pipelined ADC provides a simple and power efficient method for realizing moderate resolution ADCs and it potentially can be oversampled for achieving higher accuracy. The NSPS can be used as the front-end stage of an oversampled pipelined ADC to reduce the sensitivity to the analog imperfections and reduce the linearity requirements of the front-end stage. High resolution pipelined ADCs usually use a high number of pipelined stages to reduce the final quantization noise sufficiently. Although the power dissipation and the area consumption of the back-end stages can be scaled down, using high number of the pipelined stages is not the most power efficient choice, especially in an oversampling application where noise shaping can reduce the amount of in-band quantization noise significantly even at low OSRs. The NSTS ADC is a good candidate for the back-end stage since it provides both aggressive quantization and noise shaping with minimal hardware requirements.

The proposed noise-shaped pipelined ADC is shown in Fig. 5.7. The first

two front-end stages are NSPS and the back-end ADC is a noise-shaped two-step (NSTS) ADC. The front-end stages resolve the MSB-bits (3-bits each stage) and generate an accurate residue voltage. The residue voltage is applied to the back-end NSTS ADC which generates the LSB-bits and shapes the final quantization. The NSTS ADC resolves 5-bits and provides 3^{rd} order noise shaping. Detailed operation of the NSTS ADC was described in the previous chapter. The pipelined ADC resolves totally 9-bits and also has 9-bit linearity. The first stage of the pipelined ADC is a second order NSPS and the second stage is a first order NSPS. An amplifier is shared between the front-end stages. The NSTS ADC requires only one amplifier for two-step quantization and 3^{rd} order noise shaping. In the

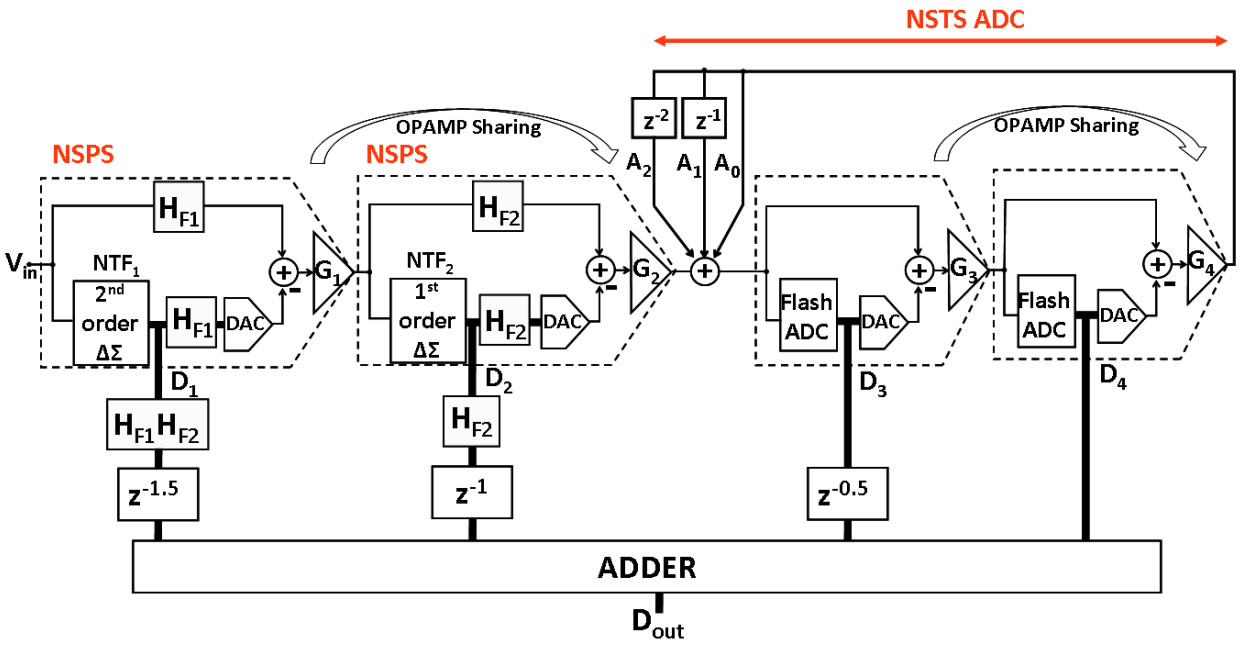

Figure 5.7: The proposed noise-shaped pipelined ADC

traditional pipelined ADCs, the final digital output is the weighted sum of all the digital outputs. In the proposed architecture, the digital outputs of the first and the second stages should be first applied to the $H_{F1}(z)H_{F2}(z)$ and $H_{F2}(z)$ digital

filters respectively and later added with the output of the NSTS ADC. This will cancel out quantization of all stages preceding the back-end NSTS ADC at the final output. Digital output (D_i) and output residue (X_{ri}) of all the pipelined stages can be expressed as following

$$D_1 = V_{in} + NTF_1 E_1 \tag{5.9}$$

$$X_{r1} = -G_1 H_{F1}(z) NTF_1 E_1 z^{-0.5} \tag{5.10}$$

$$D_2 = X_{r1} + NTF_2 E_2 = -G_1 H_{F1}(z) NTF_1 E_1 z^{-0.5} + NTF_2 E_2 \tag{5.11}$$

$$X_{r2} = -G_2 H_{F2}(z) NTF_2 E_2 z^{-0.5} \tag{5.12}$$

$$D_3 = X_{r2} + E_3 - H(z) z^{-0.5} E_4 = -G_2 H_{F2}(z) NTF_2 E_2 z^{-0.5} + E_3 - H(z) z^{-0.5} E_4 \tag{5.13}$$

$$X_{r3} = -G_3 E_3 z^{-0.5} \tag{5.14}$$

$$D_4 = X_{r3} + E_4 = -G_3 E_3 z^{-0.5} + E_4 \tag{5.15}$$

$$\begin{aligned} D_{out} &= D_1 H_{F1}(z) H_{F2}(z) z^{-1.5} + \frac{H_{F2}(z) D_2 z^{-1}}{G_1} + \frac{D_3 z^{-0.5}}{G_1 G_2} + \frac{D_4}{G_1 G_2 G_3} \\ &= V_{in} H_{F1}(z) H_{F2}(z) z^{-1.5} + \frac{NTF_4 E_4}{G_1 G_2 G_3} \end{aligned} \tag{5.16}$$

$$NTF_4 = 1 - G_3 H(z) z^{-1} \tag{5.17}$$

here, E_i, G_i, NTF_i and H_{Fi} represent the quantization noise, the inter-stage gain, the noise transfer function and the filter transfer function of the i^{th} pipeline stage. In the final digital output, shaped quantization of only last stage appears. This quantization is also scaled by the inter-stage gain product of all preceding stages. The input signal transfer function ($H_{F1}(z) H_{F2}(z) z^{-1.5}$) is a low pass FIR filter. The in-band attenuation of this transfer function is not significant even at low OSRs (less than 1dB at 4X OSR). As mentioned earlier, the inter-stage gain error

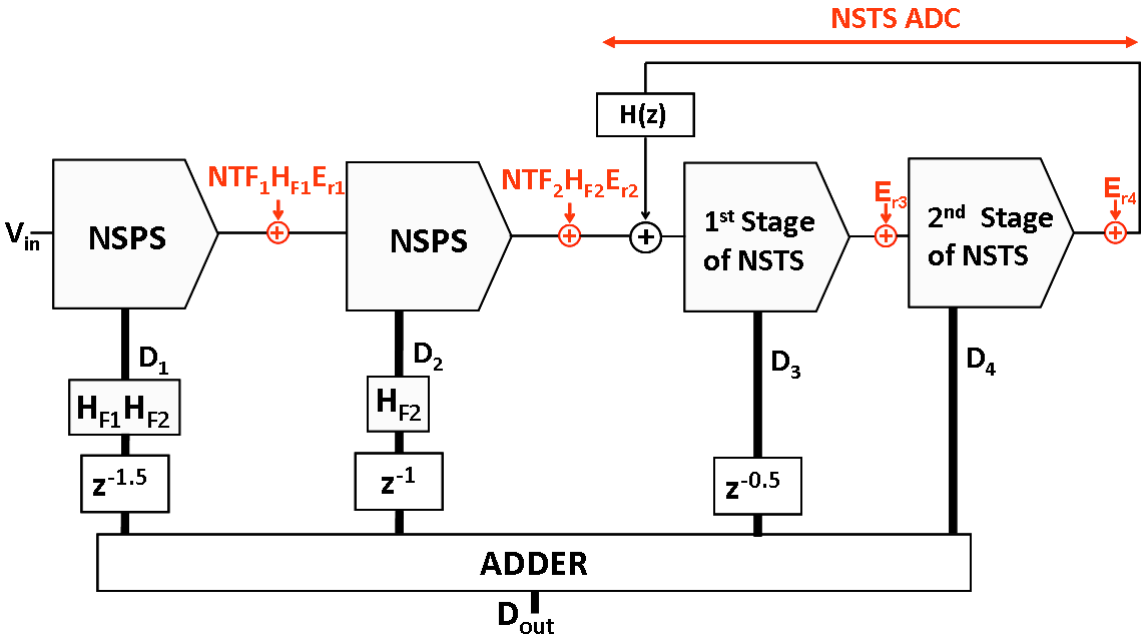

Figure 5.8: Modeling inter-stage errors in the proposed architecture

(E_{r1}) from the first NSPS is shaped. Moreover, the inter-stage error of the second stage (E_{r2}) is both shaped and suppressed by G_1. E_{r3} and E_{r4} from the NSTS ADC are not shaped but scaled by the inter-stage gain product of the succeeding stages. Hence, both front-end and back-end stages have relaxed design requirements. These errors are modeled in Fig. 5.8 and output representation of these errors can be summarized as following

$$\frac{D_{out}}{E_{r1}} = NTF_1 H_{F1} \tag{5.18}$$

$$\frac{D_{out}}{E_{r2}} = \frac{NTF_2 H_{F2}}{G_1} \tag{5.19}$$

$$\frac{D_{out}}{E_{r3}} = \frac{1}{G_1 G_2} \tag{5.20}$$

$$\frac{D_{out}}{E_{r4}} = \frac{NTF_4 - 1}{G_1 G_2 G_3} \tag{5.21}$$

It should be noted that E_{ri} includes any error that makes the inter-stage gain

inaccurate (e.g. opamp gain error, settling error and capacitor mismatch).

5.4 The circuit realization of the noise-shaped pipelined ADC

The circuit realization of the proposed architecture will be discussed in this section. Several techniques are employed to simplify the SC implementation of the NSPS and the back-end NSTS. These techniques together improve the power efficiency and reduce the area consumption.

5.4.1 The circuit realization of the NSPS

Fig. 5.9 shows a simple circuit-level realization of the NSPS with a first-order delta-sigma loop and a passive first-order filter. In this realization, separate sampling and DAC capacitors are used. The transfer function of the first-order filter is $H(z) = 0.5 + 0.5z^{-1}$. This filter is realized in the input signal path by dividing the sampling capacitor into smaller capacitors; one of them (C_{B3}) represents the 0.5 term in $H(z)$ and the other capacitor set (C_{B1} and C_{B2}) realize the delaying term ($0.5z^{-1}$). The total sampling capacitance ($C_{B3} + C_{B1,2}$) is the same as the conventional pipeline stage. The inter-stage gain is $\frac{C_{B3}+C_{B1,2}}{4C_U}$. The capacitor set ($C_{B1}$ and C_{B2}) sample the input voltage in alternate clock phases (ϕ_{1a} and ϕ_{1b}), and the stored charge is used with a one cycle delay. Mismatch between C_{B1} and C_{B2} changes the signal transfer function in the alternate clock phases, and generates an undesired image at frequencies close to $\frac{f_s}{2}$. However, due to oversampling, this image will be outside the signal band. Hence, matching between input sampling capacitors is not a concern.

The main concern in the design of NSPS is the simple realization of the low-pass filter in the sub-ADC path without increasing the number of DAC unit elements. The straight implementation of the first-order filter ($H(z) = 0.5(1+z^{-1})$) is to use one set of DAC unit elements for each filter term. Assuming X-level quantizer is used, this approach requires a front-end DAC with 2X unit elements for the first-order filter which is not desirable. Hence, the filter in the sub-ADC path is implemented differently. The output words of the sub-ADC are delayed in the digital domain to realize the delaying term of $H(z)$. One set of DAC unit elements are used to process both the current and the delayed digital outputs of the sub-ADC. During the ϕ_1 cycle, reference values corresponding to the delayed samples are stored on the DAC capacitors. During the next ϕ_2 cycle, the DAC is connected to the opamp, and the current digital outputs apply the reference voltages to the DAC. Thus, the number of the DAC unit elements is the same as the traditional pipeline stage.

The second-order NSPS can also be implemented without increasing the number of the DAC unit elements. The second order NSPS is shown in Fig. 5.10. The transfer function of the second-order filter is $H(z) = 0.25(1 + 2z^{-1} + z^{-2})$. Similar to the first-order NSPS; reference values (V_{r+} or V_{r-}) corresponding to z^{-1} term are stored on the DAC capacitors in ϕ_1. During the next cycle ϕ_2, the sum of the current and the two-cycle delayed digital outputs $(1 + z^{-2})$ select the reference voltages to the DAC. In this phase, the DAC unit elements are connected to three-level reference voltages (V_{r-} , V_{cm} and V_{r+}), since the $(1 + z^{-2})$ addition doubles the number of the sub-ADC output words. The DC magnitude of the $0.5z^{-1}$ term is the same as the $0.25(1 + z^{-2})$ term. Hence, identical DAC unit elements can be shared between the two terms. In summery, each DAC unit element resolves 5-levels; two-levels in ϕ_1 and three levels in ϕ_2.

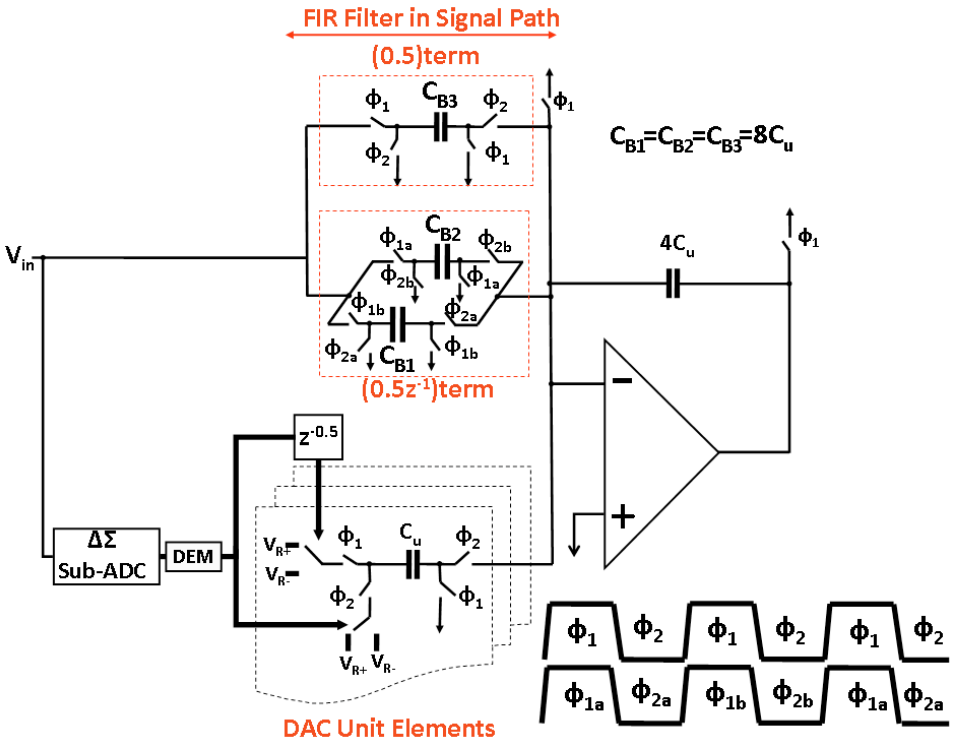

Figure 5.9: The circuit realization of the first-order NSPS

The second-order filter in the signal path is also realized by splitting the sampling capacitor into smaller parts which are sampling the input signal in alternate clock phases similar to the first-order architecture.

5.4.2 Improving the DAC linearity

In the SC gain stages, mismatch between the DAC unit elements causes harmonic distortion. DAC non-linearity causes even harmonics as well as odd harmonics in the output spectrum. Even harmonics appear at the output because errors, corresponding to each code, do not scatter symmetrically around the common mode code. In a multi-bit DAC, each unit element has the actual value

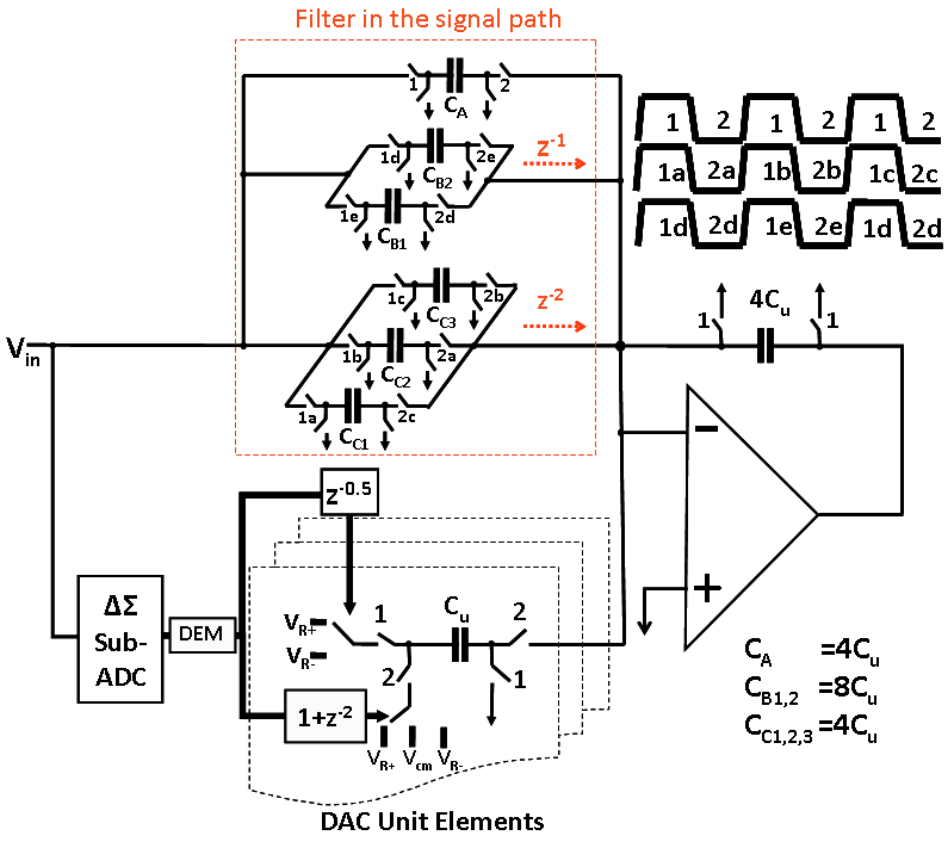

Figure 5.10: The circuit realization of the second-order NSPS

$u_j = U + d_j$ $(j = 1, 2, ..., 2M)$ where U is the average unit element and d_j is the deviation of u_j from the average. It should be noted that $\sum_{j=1}^{2M} d_j = 0$, since U is defined as $U = \sum_{j=1}^{2M} \frac{u_j}{2M}$. The middle code is M and DAC errors are distributed asymmetrically since mismatch error for code $M + i$ $(E_{M+i} = \sum_{j=1}^{M+i} d_j)$ is different from the mismatch error for code $M - i$ $(E_{M-i} = \sum_{j=1}^{M-i} d_j)$.

In the proposed NSPS architecture, the DAC unit elements are shared between the current and the delayed digital outputs. The even harmonic, caused by

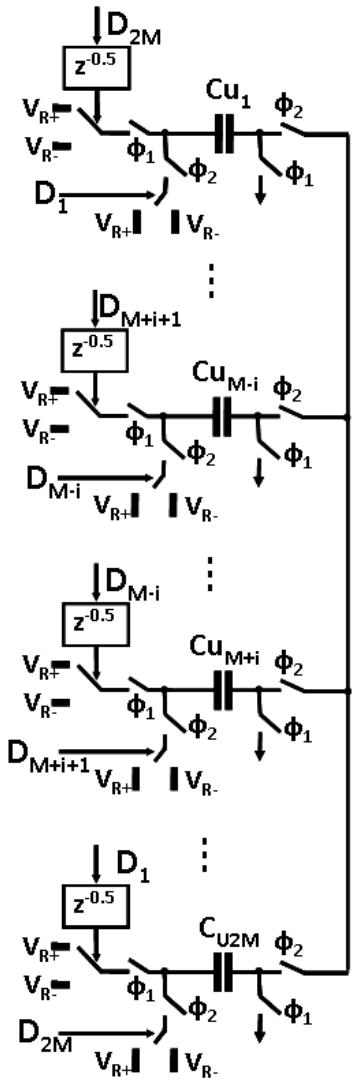

Figure 5.11: The common centriod selection of DAC unit elements

the DAC non-linearity, can be avoided simply by common centroid selection of the unit elements as shown in Fig. 5.11. In this scheme, codes 1-2M are applied to the unit elements 1-2M in ϕ_1 while, inversely codes 2M-1 are applied to the unit

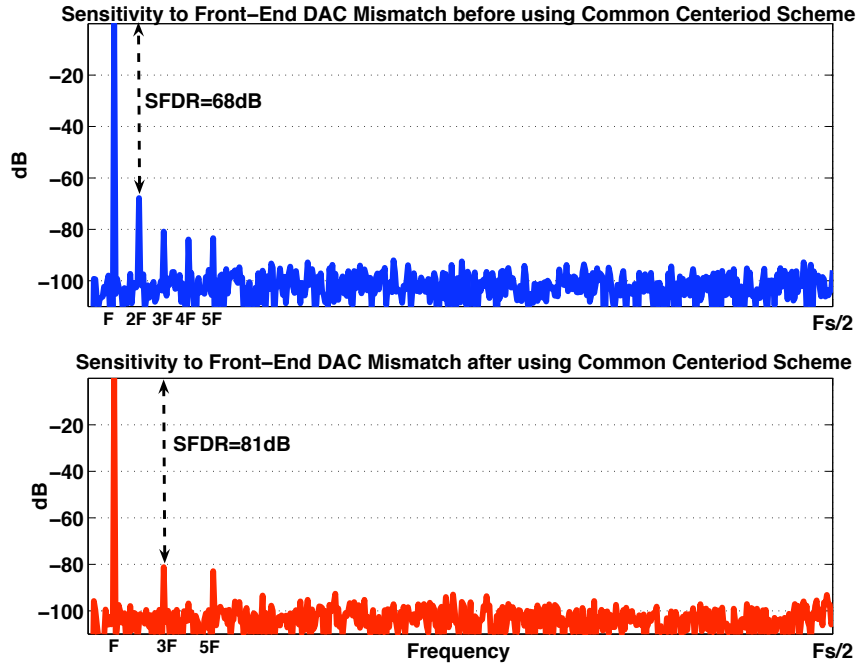

Figure 5.12: The DAC nonlinearity suppression acheived by using common centriod scheme

elements 1-2M in ϕ_2. The average error for each code is

$$E_{M+i} = 0.5(\sum_{j=1}^{M+i} d_j + \sum_{j=M-i+1}^{2M} d_j) = 0.5(\sum_{j=1}^{2M} d_j + \sum_{j=M-i+1}^{M+i} d_j) = 0.5 \sum_{j=M-i+1}^{M+i} d_j \tag{5.22}$$

$$E_{M-i} = 0.5(\sum_{j=1}^{M-i} d_j + \sum_{j=M+i+1}^{2M} d_j) = 0.5(\sum_{j=1}^{2M} d_j - \sum_{j=M-i+1}^{M+i} d_j) = -0.5 \sum_{j=M-i+1}^{M+i} d_j \tag{5.23}$$

It is apparent from these expressions that errors are distributed symmetrically in this scheme since $E_{M-i} = -E_{M+i}$. Hence, even order harmonics are avoided. Fig. 5.12 shows the output spectrum of NSPS before and after applying the proposed common-centroid scheme. For one percent mismatch between DAC unit

elements, the proposed scheme eliminates even harmonics and improves SFDR by around 13dB. This scheme is very useful for the low OSR applications where DEM techniques are not very effective. In the implemented prototype, a very simple one-bit scrambler is used along with the common centroid scheme to suppress the odd harmonics as well. The proposed technique can also be used for the second order NSPS.

5.4.3 Design of delta-sigma sub-ADC

The delta-sigma modulator in the NSPS is used only for the coarse quantization of the input signal, and it has relaxed accuracy requirements. Hence, minimum-size capacitors can be used in the delta-sigma modulator, and the loop filter amplifiers have relaxed gain requirements. This allows low-power design of the sub-ADC. In the proposed noise-shaped pipelined ADC, second-order and first-order delta-sigma sub-ADCs are used. The system level realization of the second-order delta-sigma sub-ADC is shown in Fig. 5.13. The low-distortion feed-forward architecture is modified to reduce its hardware requirements. The loop filter consists of half-delay cells instead of integrators and a single amplifier is shared between the half-delayed cells. Only one DAC is required at the input of the modulator and the loop filter generates only one output signal. This simplifies the signal addition at the input of the quantizer. The circuit realization of this delta-sigma sub-ADC is shown in Fig. 5.13. A z^{-1} delay term in the loop filter is generated by a set of sampling capacitors operating in alternate clock phases. A resistor ladder is shared between the flash quantizer and the front-end DAC of the delta-sigma modulator. Relaxed $\frac{KT}{C}$ noise requirements of the delta-sigma sub-ADC allow choosing very small sampling and feedback capacitors. The sampling

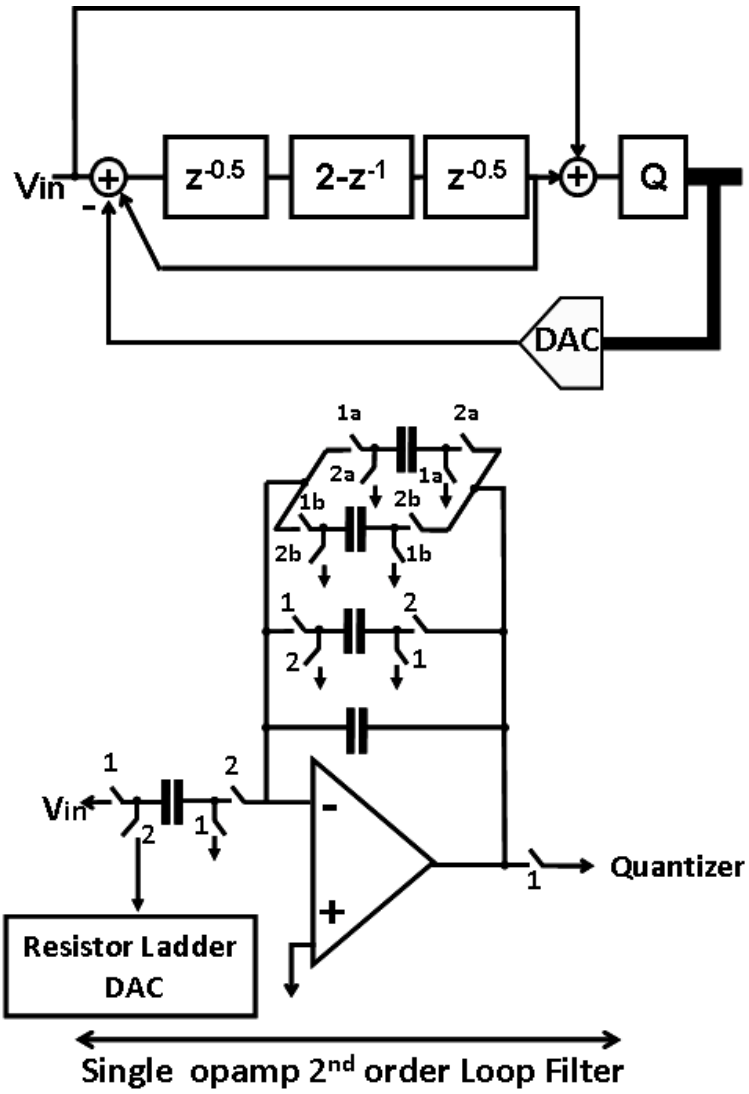

Figure 5.13: The system level and circuit level realization of the second-order delta-sigma sub-ADC

capacitor is only 50fF and power consumption of the amplifier used in this modulator is around 200uW which is less than 2 percent of the total power consumption. The area consumption of the loop filter is also less than 2 percent of the total chip area.

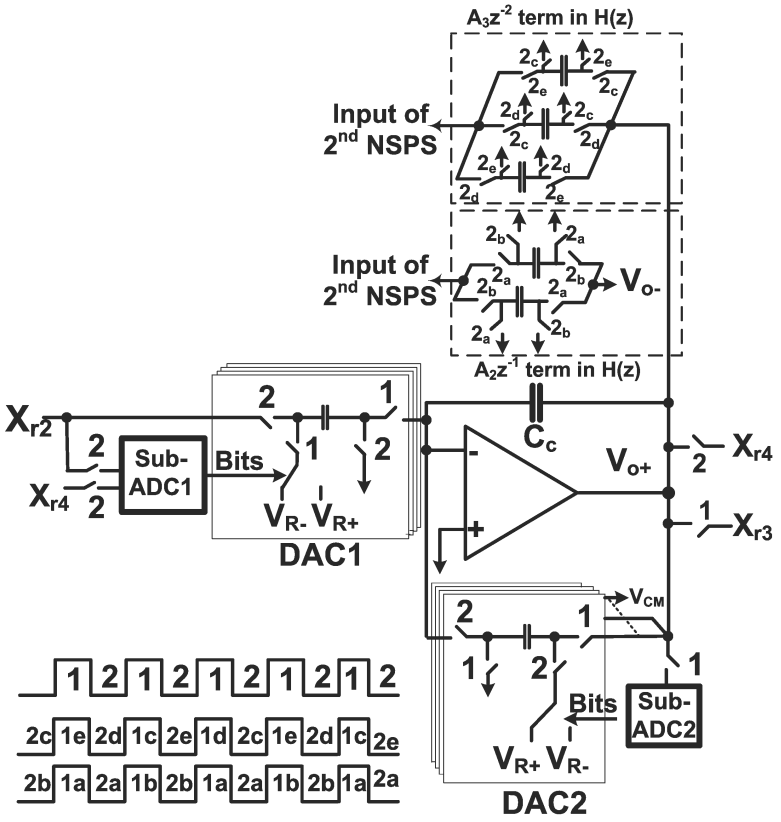

Figure 5.14: The circuit realization of the back-end NSTS ADC

5.4.4 The circuit realization of the back-end NSTS

The design of NSTS ADC was discussed in the previous chapter. A third-order NSTS ADC is used as the back-end of the noise-shaped pipelined ADC. The feedback path $H(z)$ has three terms. The A_1 and A_2 feedbacks are added at the input of the second NSPS stage to simplify the signal addition at the input of the quantizer. The circuit realization of the NSTS is shown in Fig. 5.14. The opamp/capacitor sharing scheme, introduced in the previous chapter, is employed in the back-end NSTS ADC.

5.5 Measurement results

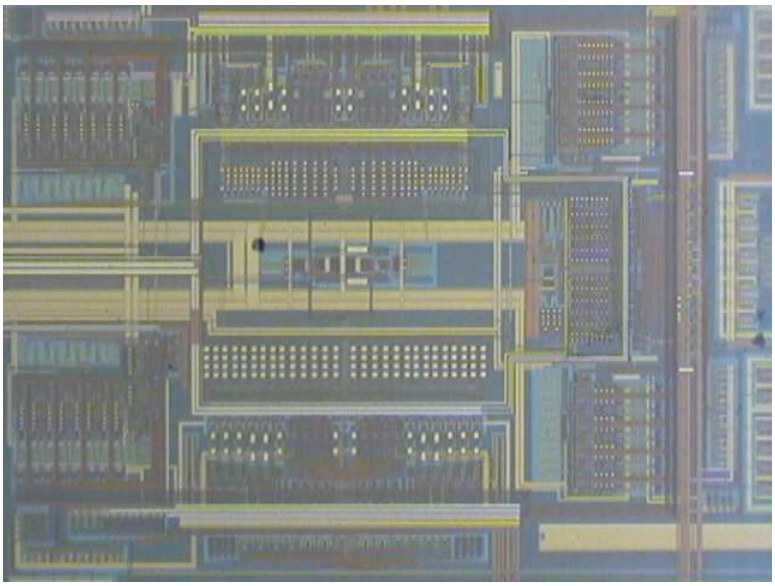

Figure 5.15: Die Micrograph

The proposed noise-shaped pipelined ADC was designed and fabricated in a 2P4M 0.18μm CMOS process. The die photograph is shown in Fig. 5.15. The total die area is $1.2mm^2$.

An option was implemented to disable the loop filter in the delta-sigma sub-ADC and show the effectiveness of the proposed NSPS. The sub-ADC works as a regular flash sub-ADC and the properties of the front-end stage are similar to the traditional pipeline stage when the loop filter is disabled. The loop gain of the amplifier in the front-end stage is around 45-50dB.

The measured output spectrum is shown in Fig. 5.16 and Fig. 5.17 for 64 MHz sampling rate before and after activating the delta-sigma sub-ADC. At 6X OSR, the peak SNDR and SFDR are improved 15dB and 26dB respectively when NSPS is activated. These properties are well matched with the simulation results given in

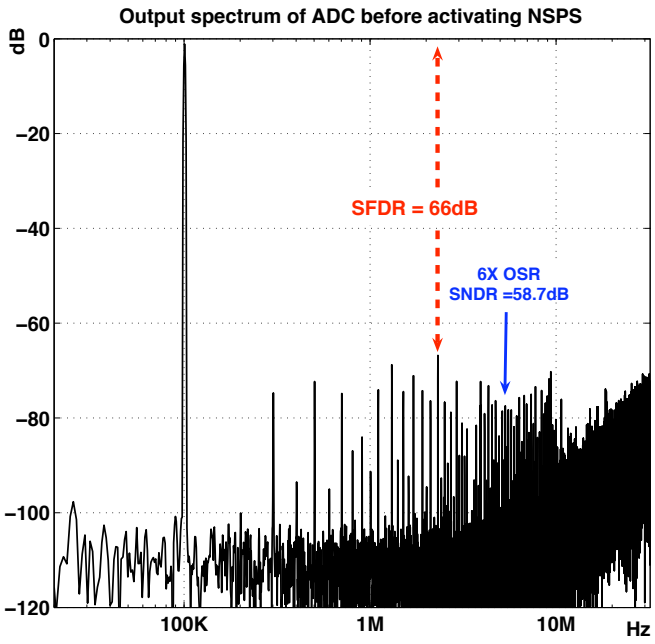

Figure 5.16: The output spectrum of the ADC before activating the NSPS

section 5.2. The power dissipation of the loop filter in each delta-sigma sub-ADC is only 200uW. The total analog and digital power consumptions are 8.2mW and 5.7mW respectively. The SNDR plot for varying input signal amplitude is shown in Fig. 5.18 for 64 MHz sampling rate (OSR of 6). The FOM of the proposed pipelined ADC is among the best reported for the low OSR oversampled ADCs.

5.6 Conclusions

In this chapter, a noise-shaped pipelined ADC is presented. This ADC uses a coarse delta-sigma sub-ADC and a passive loop filter in the front-end stage to suppress both linear and nonlinear inter-stage gain errors. This technique achieves 15dB SNDR improvement at 6x OSR by burning only 200uW extra power in the

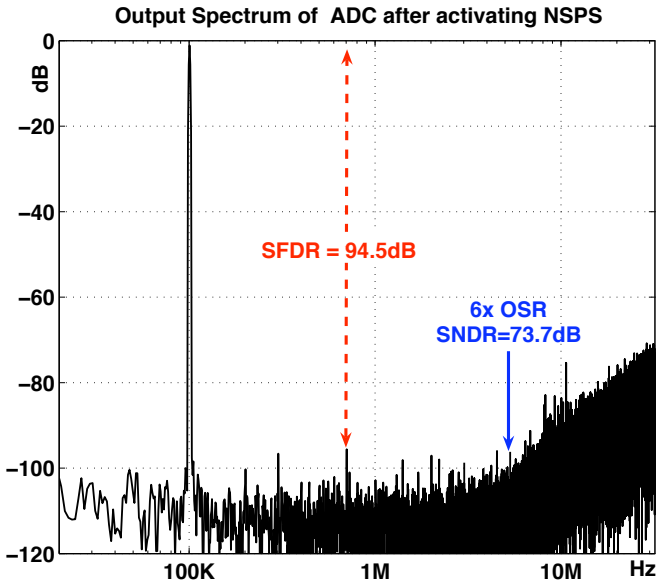

Figure 5.17: The output spectrum of the ADC after activating the NSPS

delta-sigma sub-ADC. The back-end NSTS ADC shapes and suppress the final quantization with minimal design overhead.

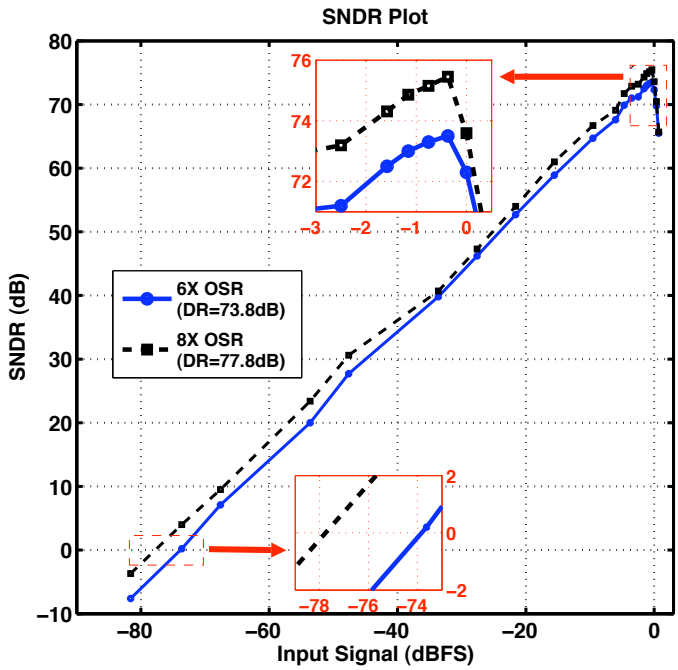

Figure 5.18: The SNDR plot for 8X and 6X OSR

Table 5.1: Summary of the measurement results

Sampling Rate	**64 MHz**
Signal Bandwidth	**5.33 MHz**
OSR	**6**
SFDR (dB)	**94.5**
DR (dB)	**73.8**
SNDR (dB)	**73.7**
Input Range (Diff)	**2.2 Vpp**
Comparator Reference voltage	**1.2 V**
Analog Supply(V)	**1.3**
Digital Supply(V)	**1.55**
Analog Power	**8.2mW**
Digital Power	**5.7mW**
Core Area	**1.2** mm^2

CHAPTER 6. CONCLUSION

Oversampled ADCs are commonly used for applications with high oversampling ratios and high resolution. However, as the demand for ADCs with higher bandwidth increases, designers have to contend with lower OSRs. Simple and power efficient implementation is the main challenge in design of low OSR oversampled ADCs. New architectures are proposed to address this challenge and improve on the shortcomings of the conventional oversampled ADCs. The proposed architectures combine the noise shaping properties of delta-sigma ADCs with aggressive quantization of pipelined ADCs without imposing stringent design requirements on the building blocks. Three prototype ADCs were designed and fabricated. Measurement results demonstrate the effectiveness of the proposed architectures.

A Hybrid Delta-Sigma/Pipelined (HDSP) ADC is proposed. In this architecture, a pipelined ADC is employed as the quantizer of a single-loop delta-sigma modulator. The frond-end DAC is only associated with the digital outputs of the first pipelined stage. However, two analog feedback paths from the residue of the first and the last pipelined stages provide the rest of signal information and the quantization noise of a full pipelined ADC is processed by the loop filter. The integrators in the loop filter have relaxed swing and gain requirements. Furthermore, the latency of the pipelined ADC is employed to increase the order of noise shaping. Enhanced noise shaping and quantization properties of the HDSP modulator makes this architecture a suitable candidate for low OSR applications. Fabricated in CMOS 0.18μm technology, with an 80MHz clock, and an oversampling ratio of

8 (5MHz bandwidth), the measured dynamic range and SNDR of this prototype IC are 79dB and 75.4dB. The figure-of-merit ($FOM = \frac{Power}{2BW.2^{ENOB}}$) of this ADC is 0.67 $\frac{pJ}{Conv}$.

A Noise-Shaped Two-Step (NSTS) ADC is presented. This ADC requires only one residue amplifier for high orders of noise shaping (e.g. third order) and two-step quantization (e.g.7-8 bits). This ADC can be configured as a standalone ADC, as a cascaded delta-sigma modulator or as the quantizer of a single-loop modulator. The standalone NSTS ADC can be considered as the counterpart of the MASH modulator. However, it requires less number of the amplifiers compared to the MASH modulator. Unlike the MASH architecture, NSTS ADC also takes full advantage of the redundancy between stages to extend the input signal range. Extensive simulations are provided to show the effectiveness of the NSTS ADC. The NSTS ADC is also exploited as the quantizer of the HDSP modulator to reduce the hardware requirements and power consumption. Fabricated in CMOS 0.18μm technology, the FOM of the HDSP architecture is improved from 0.67 to 0.44 $\frac{pJ}{Conv}$.

Finally, a noise-shaped pipelined ADC with reduced sensitivity to the analog imperfections is proposed. In the front-end stage of this ADC, the sub-ADC is replaced with a coarse delta-sigma modulator which is followed by a low-pass passive filter. The shaped quantization noise is extracted and processed by the pipelined MDAC. Hence, both linear and non-linear inter-stage gain errors are suppressed. Measurement results shows that the proposed technique improves SNDR by 15dB at 6X OSR compared to the conventional pipeline stage. This is achieved by burning only 200uW extra power in the delta-sigma sub-ADC. NSTS quantizer is used as the back-end stage of the pipelined ADC to shape and suppress the final quantization error. Implemented in CMOS 0.18μm technology, with a

64MHz clock, and an oversampling ratio of 6 (5.3MHz bandwidth), the measured dynamic range and SNDR of this prototype IC are 73.8dB and 73.7dB. The FOM of this ADC is 0.33 $\frac{pJ}{Conv}$.

The FOM [35] of these ADCs is among the best reported for high bandwidth oversampled ADCs. Fig. 6.1 compares the performance of the proposed architectures with the most recent oversampled and Nyquist ADCs. The resolution of the ADCs (used in this survey) is between 11 to 13bits.

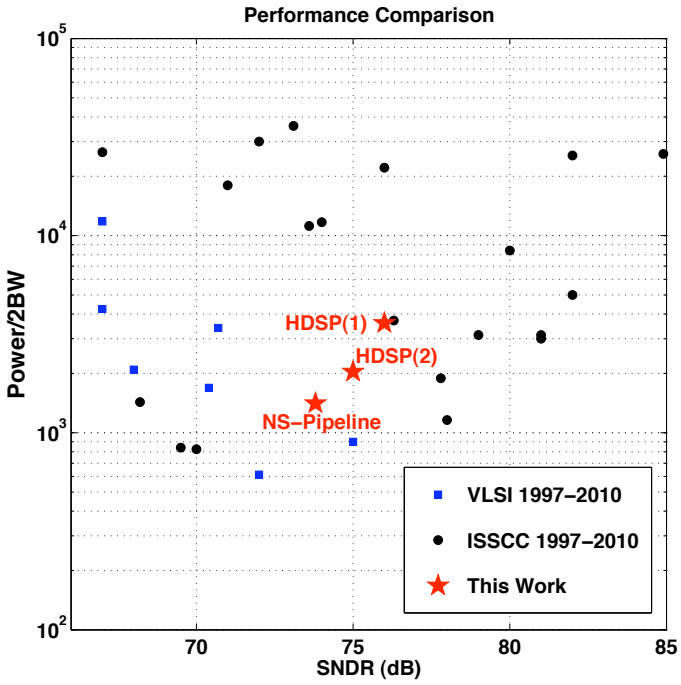

Figure 6.1: Comparing performance of the proposed architectures with the state of the art ADCs ($\frac{Power}{2BW}$ vs SNDR)

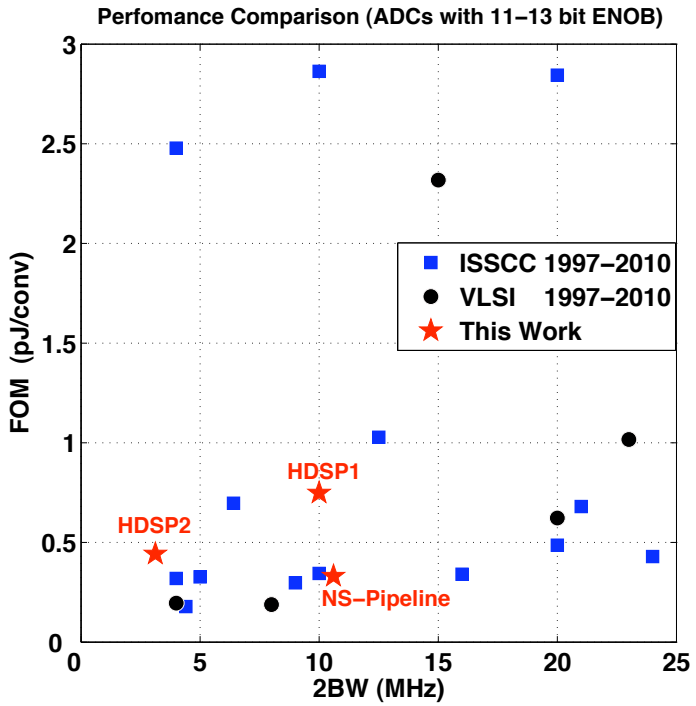

Figure 6.2: Comparing performance of the proposed architectures with the state of the art ADCs (FOM vs. BW)

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