Novel Performance Enhancement Techniques for Delta Sigma Modulators for Telecom, Audio and Sensor Applications

LI, Bing

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for Delta Sigma Modulators
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Submitted by **LI, Bing**
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The rapid growth of the market for portable, battery operated systems for communications, computer and consumer electronics (3C), and the trend of moving functionality to the digital domain in very large scale integration (VLSI) systems have resulted in an enormously increasing interest in analog-to-digital converter (ADC) design.

Combining both oversampling and quantization error shaping techniques, delta sigma (ΔΣ) ADCs achieve a high degree of insensitivity to analog circuit imperfections. Nevertheless, the design of CMOS ΔΣ ADCs involves a number of practical issues and trade-offs that must be taken into account in order to optimize their performance in terms of power consumption, silicon area, and time-to-market deployment. This thesis proposes a number of novel performance-enhancement techniques on different design levels, including algorithm, architecture and circuit

level, for ΔΣ ADCs in various application circumstances, such as telecom, audio, sensor, and so on.

First, novel techniques are proposed to mitigate I/Q mismatches in switched-capacitor quadrature bandpass Delta-Sigma modulators (DSMs) used in low-IF wireless receivers. The I/Q mismatches result in a nearby channel at the image frequency, the mirrored image of the desired signal around its center frequency (self-image) and the quantization noise to corrupt the desired signal, degrading the dynamic range of the modulator. A dynamic element matching scheme and a bilinear scheme are the proposed solution to reduce all the above-mentioned I/Q mismatch effects. Furthermore, a multiplexing scheme for the sharing of op-amps, quantizers and DACs between the I and Q channels is investigated for smaller chip area. A prototyping DSM was designed and fabricated in a 0.18 μm CMOS, measuring an image rejection ratio of 73 dB, being the best reported.

Second, a pulse-width-modulation (PWM) technique is proposed for on-chip automatic *RC* time constant tuning for cascaded continuous-time (CT) DSMs for audio application. The demand for high signal-to-noise-plus-distortion ratio (SNDR) and low power brings a wealth of opportunities to the CT DSMs. In CT DSMs, cascading low-order stages provides an effective way to achieve stable high-order modulation. However, compared to CT single-loop modulators, CT cascaded modulators are more sensitive to variation of *RC* time constant and finite dc gain of the opamps as these nonidealities affect the precise cancellation of the quantization

noises between the analog and digital paths. In the CT cascaded modulator presented here, we propose to apply a PWM technique for on-chip automatic *RC* time constant tuning. The application of PWM in turn enables the use of the correlated double sampling (CDS) technique, which is conventionally confined to discrete-time circuits, to boost the effective dc gain. The PWM further allows the use of a finite-opamp-bandwidth compensation technique for power saving. Analysis on PWM tuning, CDS, anti-aliasing filtering, noise and jitter in the CT modulator are presented and verified with extensive simulations. Measurement results on a prototype CT cascaded 2-2 DSM in a 0.18-μm CMOS show that the proposed techniques can improve the dynamic range (DR), SNDR and spurious-free dynamic range (SFDR) of the modulator by at least 28 dB.

Third, a high-precision capacitance-to-digital converter (CDC) is proposed, which can be configured to interface with single-ended or differential capacitive sensors. In the conventional CDC, charge injection from bottom-plate switches depends on the digital output and the value of the sensing capacitor. Nonlinearity is resulted especially when the varying ranging of the sensing capacitor is wide. In this thesis, new switching and calibration schemes are proposed to reduce these charge injection. A prototyping 2nd order CDC employing the proposed techniques is fabricated in a 0.18-μm CMOS process and achieves a 53.2aFrms resolution in a 0.5ms measuring time. The proposed techniques improve the CDC's linearity from 9.3 bits to 12.3 bits in the single-ended sensing mode, and from 10.1 bits to 13.3 bits in the

differential sensing mode, with a wide sensing capacitor range from 0.5 to 3.5pF. The CDC is also demonstrated with real-life pressure (single-ended) and acceleration (differential) sensors.

摘 要

在過去的十年裡，隨著便攜式通訊，電腦與消費電子市場的快速發展，以及在超大規模積體電路中，越來越多的功能實現被轉移到數字領域中，這些都引起了人們對模數轉換器研究的極大關注。

基於過採樣與量化誤差整形技術，ΣΔ 模數轉換器對與類比電路中的非理想特性具有很強的容忍度。然而，爲了優化其在功耗，硅片面積與上市時間等方面的性能，ΣΔ 模數轉換器的設計需要對眾多實際問題做出折中考慮。本文在不同的設計層次上提出了一些創新，包括算法，架構及電路設計，從而提升其在通訊，語音與傳感等應用領域中的性能指標。

本文第一部份提出的新技術主要解決運用於低中頻無線接收器中開關電容型正交帶通 ΣΔ 模數轉換器的 I/Q 通道的不匹配問題。這些 I/Q 通道的不匹配將導致位於臨近信道的鏡像信號，自鏡像信號及量化噪聲混疊至輸入信道，從而降低模數轉換器的動態範圍。為此，本文提出了一種新的動態單元匹配技術與一種雙線性技術來解決上述問題。同時通過在 I/Q 信道間複用運算放大器，比較器與數模轉換器，芯片的面積得到了大幅的降低。基於以上技術，在 0.18 微米 CMOS 工藝上設計實現了開關電容型正交帶通 ΣΔ 模數轉換器的測試樣片，其鏡像抑制比可達到 73dB，這是迄今為止公開發表論文中報告的最高值。

在本文的第二部份，我們關注 ΣΔ 模數轉換器在音頻領域的應用。其對動態範圍與功耗提出的較高要求為級聯型連續時間ΣΔ模數轉換器帶來了機遇。然而，相比于單環型，級聯型連續時間 ΣΔ 模數轉換器對於電阻-電容時間常數的偏離及

摘 要

有限的運放低頻增益等非理想特性表現得更加敏感,因為這些不理想因素將影響量化噪聲在模擬與數字路徑中的精確抵消。為此,我們提出了使用脈寬調製技術來對片上的電阻-電容時間常數進行自動調整。基於脈寬調製技術,我們可以使用在離散時間電路中常用的相關雙採樣技術來提高運放的有效低頻增益。同時我們提出了一種有限運放帶寬補償技術來節省芯片的功耗。另外,本文對基於連續時間 ΣΔ 模數轉換器的脈寬調製技術,相關雙採用技術,反混疊濾波,噪聲與抖動效應等方面均做出了詳盡的仿真與分析。最後我們對一顆基於 0.18 微米 CMOS 工藝設計的樣片進行了測試。測試結果表明,採用本文提出的技術可以將 ΣΔ 模數轉換器的動態範圍提高 28dB 以上。

本文的第三部份展示了一種可用於單端或差分電容傳感器的高精度電容-數字轉換器。在傳統的電容-數字轉換器中,由電容底板開關引入的電荷注入與數字輸出結果及被感知電容的容值有關。當被感知電容的容值變化範圍較大時,這些電荷注入將產生很大的非線性。對此本文提出了一種新的開關控制與校準算法。我們對一顆基於 0.18 微米 CMOS 工藝設計的二階電容-數字轉換器樣片進行了測試。測試結果表明,其在 0.5 毫秒的測試時間內可達到 53.2aFrms 的精度。同時本文提出的技術可以在 0.5pF 至 3.5pF 的較寬電容範圍內,使得電容-數字轉換器在單端電容傳感模式下的線性度(準確度)從 9.3 位提高至 12.3 位;在差分電容傳感模式下的線性度(準確度)從 10.1 位提高至 13.3 位。最後,本文對連接微機電電容型壓力傳感器和加速度傳感器的實際應用情境進行了測試。

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CHAPTER 1. Introduction

1.1 Motivation

The rapid growth of the market for portable, battery operated systems for communications, computer and consumer electronics (3C), and the trend of moving functionality to the digital domain in very large scale integration (VLSI) systems have resulted in an enormously increasing interest in analog-to-digital converter (ADC) design.

There exist plenty of possibilities to implement an A/D conversion. For different ranges of resolution and speed, different conversion methods are considered optimal. One favorable option is the delta-signal (ΔΣ) ADC. Since the first idea underlying the operation of ΔΣ ADCs was patented [1] around 50 years ago, there have been a huge number of circuits and systems exploiting ΣΔ ADCs in many different industrial applications from instrumentation, audio, sensor interface to communications [2]-[17]. Combining oversampling and quantization error shaping techniques, ΣΔ ADCs achieve a high degree of insensitivity to analog circuit imperfections. This is achieved through extensive use of digital signal post-processing, which is actually highly preferred in modern VLSI technology where the implementation of dense and fast digital circuits can be better realized than accurate analog functions. ΣΔ ADCs are thus a good choice for embedded ADCs in modern systems-on-chip (SoCs) integrated in aggressively scaled CMOS technologies.

In spite of the aforementioned advantages, the design of CMOS ΣΔ ADCs involves a number of practical issues and trade-offs that must be taken into account in order to optimize their performance in terms of power consumption, silicon area, and time-to-market deployment. The objectives of this thesis are to improve these performances of ΣΔ ADCs in some specific application domains through innovations in system and circuit levels.

1.2 Original contributions and outline of the thesis

In this thesis, we concentrate on ΔΣ ADCs for three specific application domains and propose original methods on algorithmic, architectural and circuit levels to improve their performances. Two of them are DT ΣΔ ADCs and one CT.

First, novel techniques are proposed to mitigate I/Q mismatches in switched-capacitor quadrature bandpass Delta-Sigma modulators (DSMs) used in low-IF wireless receivers. The I/Q mismatches result in a nearby channel at the image frequency, the mirrored image of the desired signal around its center frequency (self-image) and the quantization noise to corrupt the desired signal, degrading the dynamic range of the modulator. A dynamic element matching scheme and a bilinear scheme are the proposed solution to reduce all the above-mentioned I/Q mismatch effects. Furthermore, a multiplexing scheme for the sharing of op-amps, quantizers and DACs between the I and Q channels is investigated for smaller chip area. A prototyping DSM was designed and fabricated in a 0.18 μm CMOS, measuring an

image rejection ratio of 73 dB, being the best reported. This work is presented in Chapter 2.

Second, a pulse-width-modulation (PWM) technique is proposed for on-chip automatic *RC* time constant tuning for cascaded continuous-time (CT) DSMs for audio application. The demand for high signal-to-noise-plus-distortion ratio (SNDR) and low power brings a wealth of opportunities to the CT DSMs. In CT DSMs, cascading low-order stages provides an effective way to achieve stable high-order modulation. However, compared to CT single-loop modulators, CT cascaded modulators are more sensitive to variation of *RC* time constant and finite dc gain of the opamps as these nonidealities affect the precise cancellation of the quantization noises between the analog and digital paths. In the CT cascaded modulator presented here, we propose to apply a PWM technique for on-chip automatic *RC* time constant tuning. The application of PWM in turn enables the use of the correlated double sampling (CDS) technique, which is conventionally confined to discrete-time circuits, to boost the effective dc gain. The PWM further allows the use of a finite-opamp-bandwidth compensation technique for power saving. Analysis on PWM tuning, CDS, anti-aliasing filtering, noise and jitter in the CT modulator are presented and verified with extensive simulations. Measurement results on a prototype CT cascaded 2-2 DSM in a 0.18-μm CMOS show that the proposed techniques can improve the dynamic range (DR), SNDR and spurious-free dynamic range (SFDR) of the modulator by at least 28 dB. This work is presented in Chapter 3.

Third, a high-precision capacitance-to-digital converter (CDC) is proposed, which can be configured to interface with single-ended or differential capacitive sensors. In the conventional CDC, charge injection from bottom-plate switches depends on the digital output and the value of the sensing capacitor. Nonlinearity is resulted especially when the varying ranging of the sensing capacitor is wide. In this thesis, new switching and calibration schemes are proposed to reduce these charge injection. A prototyping 2nd order CDC employing the proposed techniques is fabricated in a 0.18-μm CMOS process and achieves a 53.2aFrms resolution in a 0.5ms measuring time. The proposed techniques improve the CDC's linearity from 9.3 bits to 12.3 bits in the single-ended sensing mode, and from 10.1 bits to 13.3 bits in the differential sensing mode, with a wide sensing capacitor range from 0.5 to 3.5pF. The CDC is also demonstrated with real-life pressure (single-ended) and acceleration (differential) sensors. This work is presented in Chapter 4.

Finally, the conclusions and future works are given in Chapter 5.

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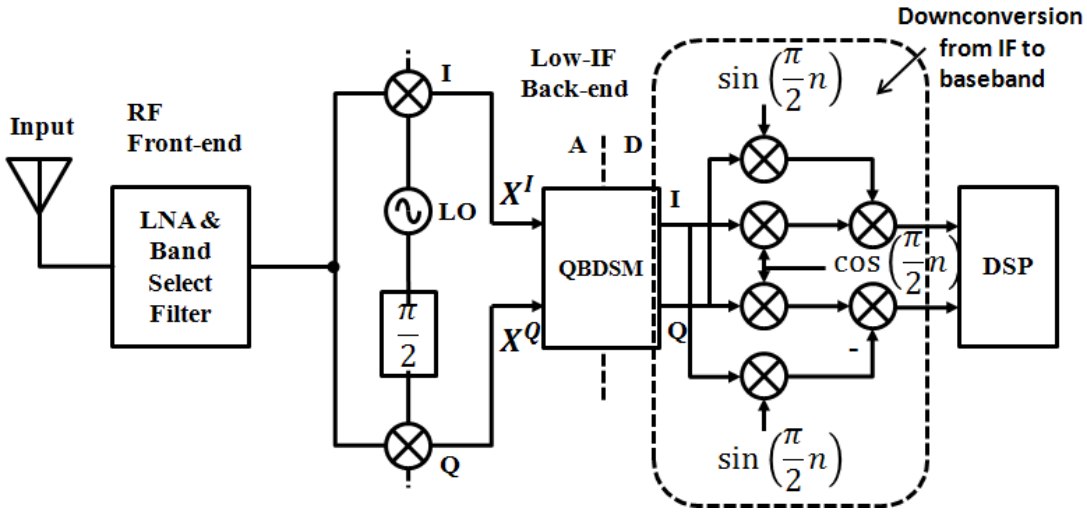
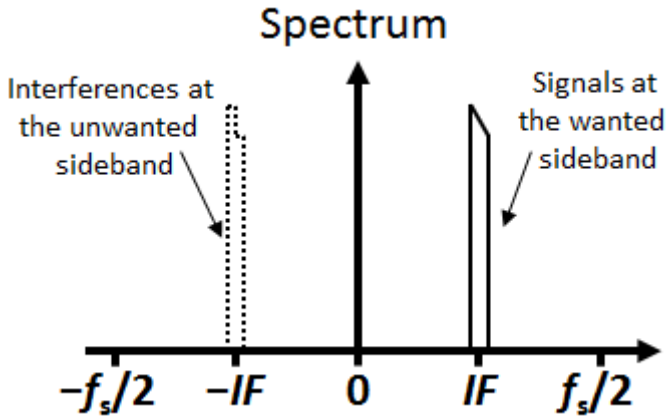
CHAPTER 2. A High Image-Rejection SC Quadrature Bandpass DSM for Low-IF Receivers

Quadrature Bandpass Delta-Sigma Modulators (QBDSM) are widely used for digitization of intermediate-frequency (IF) signals in low-IF receivers. Fig. 2.1(a) shows a block diagram of a low-IF receiver. The quadrature mixer converts the received real RF signal to a complex low-IF [1] signal, which is directly digitalized by the QBDSM to generate in-phase (I) and quadrature-phase (Q) digital bit streams for further processing. In the digital domain, the demodulation from IF to the baseband is often performed by choosing the sampling frequency f_s equal to four times the IF [2]. This down conversion can be implemented very efficiently by applying only simple multiplexing and inversion operations, as the oscillator inputs to the second complex digital mixer are simply ± 1 or 0.



(a)



(b)

Fig. 2.1: (a) Low-IF receiver architecture; (b) a spectrum of the complex signal $(X^I + jX^Q)$ at the mixer's output.

One of the claimed advantages of the low-IF architecture is that it avoids the problems of DC offset and 1/*f* noise while maintaining a high level of integration. However, it generally has higher image rejection requirement than a zero-IF receiver. In the zero-IF receiver, where the image signal is the desired signal itself so a relatively low image rejection (about 40 dB) suffice for many applications [3][4]. In the low-IF topology, the image signal comes from an nearby channel that can be 20-30 dB larger than the desired signal [3][4]. The image signal is aliased into the signal band due to gain and phase mismatches between the I and Q signal paths. In order to minimize this image interference, a high image-rejection capability is desirable for the low-IF receiver and for the QBDSM, which plays a crucial role in the receiver (as shown in Appendix I). Further to the problem of aliasing the image channel into the signal band, the I/Q mismatches in the QBDSM also cause: (i) the unshaped quantization noise at

the image frequency to leak into the signal band; and (ii) a mirrored image of the desired signal around its center frequency, i.e., the self-image, to arise.

Various techniques dealing with different aspects of I/Q mismatches have been reported in the literature [1][2][5]-[10]. In [5], an adaptive mismatch cancellation system to correct I/Q mismatches at the cost of complex digital signal processing was proposed. In [1], a notch is placed in the image band of the noise transfer function (NTF) to address the issue of aliasing of the quantization noise. This complicates the NTF design and wastes an NTF zero in noise shaping in the desired band [6]. A dynamic element match shaping (DEM) method through a randomized swapping of I/Q components was proposed in [7], which raises the noise floor of the modulator and hinders the noise shaping in the desired band. Another DEM method that swaps I/Q components alternately was introduced and verified by simulation results in [8], but it causes a self-image problem. A mismatch insensitive double-sampling QBDSM with a resonator with a bilinear input circuit was reported in [2], however, the self-image problem remains to be tackled. Moreover, the bilinear branch for the feedback DAC signal, which is included in the loop of the modulator, complicates its architecture design. An I/Q path-sharing technique for high image rejection is reported in [9] for a complex switched-capacitor (SC) Delta Sigma modulator, which deals with real, not complex, IF inputs. Since it does not take a complex input, the modulator in [9] cannot apply to the receiver shown in Fig. 2.1(a).

In this chapter, new DEM [10] and bilinear techniques are proposed for high image-rejection SC QBDSMs that have their notch frequency located at $f_s/4$.

Furthermore, an I/Q channel multiplexing scheme to share the op-amps, quantizers and DACs between the I and Q channels is proposed to eliminate some components of the I/Q mismatches as well as to reduce chip size. To verify the proposed techniques, a prototyping SC QBDSM was designed and fabricated in a 0.18μm CMOS technology and measured results are reported.

2.1 Mismatch in Complex Gain Blocks

Coefficient mismatch in a complex filter has been modeled in [11]. To lay a background for analyzing the mismatch in QBDSM, the coefficient mismatch for a general complex gain block is reviewed here following the approach in [11].

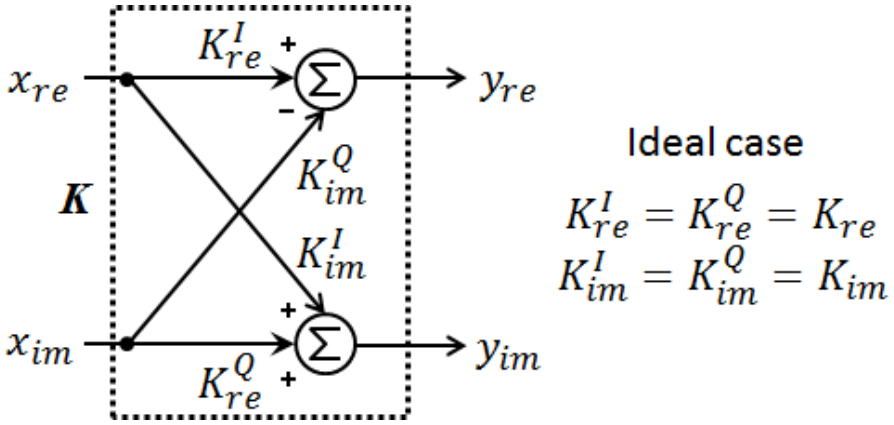
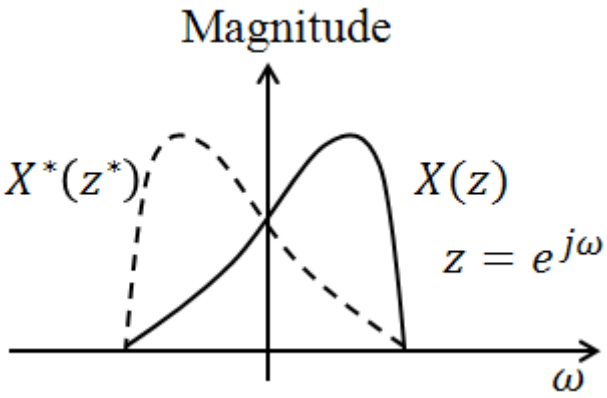


Fig. 2.2. Realizing a complex gain block with real gain blocks.



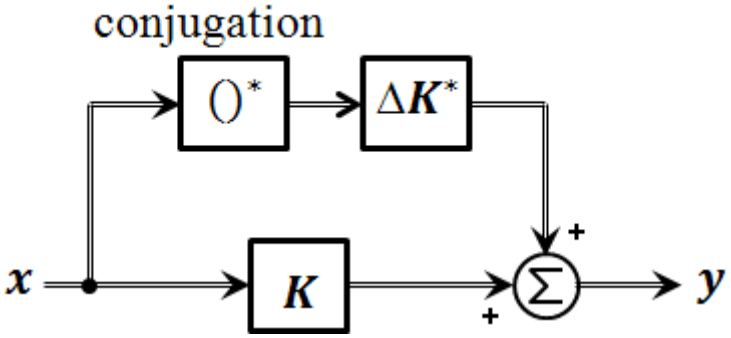


Fig. 2.3. A complex gain block model with coefficient mismatch.

A complex signal $\boldsymbol{x} = x_{re} + jx_{im}$ multiplied by a complex gain factor $\boldsymbol{K} = K_{re} + jK_{im}$ can be realized by real multiplication blocks as shown in Fig. 2.2. In the ideal case, $K_{re}^{I} = K_{re}^{Q} = K_{re}$, $K_{im}^{I} = K_{im}^{Q} = K_{im}$, and the time-domain output is[†]:

$$\boldsymbol{y} = \boldsymbol{K}\boldsymbol{x} = K_{re}x_{re} - K_{im}x_{im} + j(K_{re}x_{im} + K_{im}x_{re}) \tag{2.1}$$

In the complex gain block, there are two paths (I and Q) for each of the real coefficients K_{re} and K_{im}. Due to process variation, mismatches exist between these I and Q path coefficients. In general, $K_{re}^{I} \neq K_{re}^{Q}$ and $K_{im}^{I} \neq K_{im}^{Q}$. Here we propose to represent the coefficient mismatch in complex form:

$$\begin{gathered} K_{re}^{I} = K_{re} + \Delta K_{re} \quad K_{re}^{Q} = K_{re} - \Delta K_{re} \\ K_{im}^{I} = K_{im} + \Delta K_{im} \quad K_{im}^{Q} = K_{im} - \Delta K_{im} \\ \Delta\boldsymbol{K} = \Delta K_{re} + j\Delta K_{im}. \end{gathered} \tag{2.2}$$

Based on the definitions in Eq. (2.2), the time-domain output of the complex gain block becomes:

$$\begin{aligned} \boldsymbol{y} &= \boldsymbol{K}\boldsymbol{x} + \Delta K_{re}x_{re} - \Delta K_{im}x_{im} + j(-\Delta K_{re}x_{im} - \Delta K_{im}x_{re}) \\ &= \boldsymbol{K}\boldsymbol{x} + \Delta K_{re}(x_{re} - jx_{im}) - \Delta K_{im}(x_{im} + jx_{re}) \end{aligned} \tag{2.3}$$

[†] In this chapter, complex coefficients and time-domain variables are shown in bold for a contrast to real ones, while z-domain variables are not since they are complex by definition.

$$= \boldsymbol{K}\boldsymbol{x} + \Delta K_{re}(x_{re} - jx_{im}) - j\Delta K_{im}(x_{re} - jx_{im})$$

$$= \boldsymbol{K}\boldsymbol{x} + \Delta\boldsymbol{K}^{*}\boldsymbol{x}^{*}$$

The asterisk in Eq. (2.3) indicates complex conjugation. For discrete-time systems, applying z-transform to Eq. (2.3), we obtain:

$$Y(z) = \boldsymbol{K}X(z) + \Delta\boldsymbol{K}^{*}X^{*}(z^{*}). \tag{2.4}$$

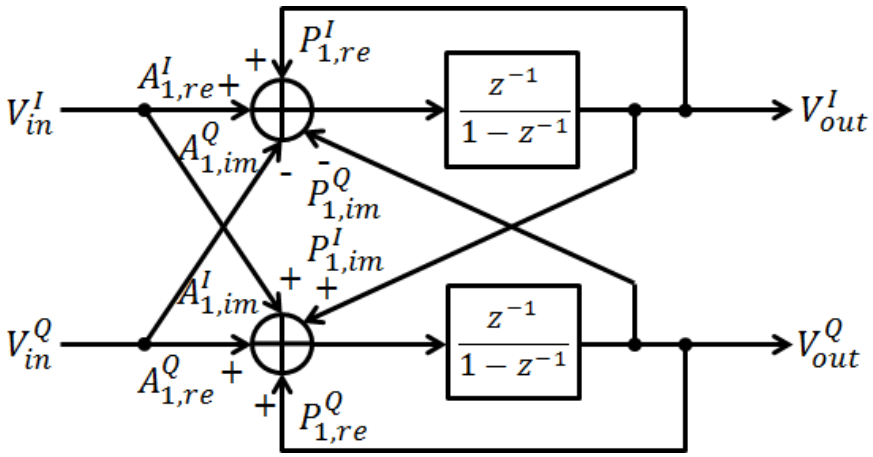
Eq. (2.4) is resulted with the use of the linearity property of z-transform and that $\mathcal{Z}\{\boldsymbol{x}^{*}\} = X^{*}(z^{*})$. The mismatch effect is modeled in Fig. 2.3. It is seen that the I/Q coefficient mismatch adds to the output an error term that is proportional to the conjugate – the frequency-domain mirror image - of the input as shown in Fig. 2.3. We define the image rejection ratio (*IRR*) as the ratio of the gain magnitude of the desired signal ($X(z)$) to that of the image signal ($X^{*}(z^{*})$), i.e.,$IRR = |\Delta\boldsymbol{K}|/|\mathbf{K}|$ for this gain block. In this thesis, we consider the mismatch being frequency-independent, which is generally true for narrow band systems. The above results form the basis for our analysis in subsequent sections.

2.2 Mismatches in QBDSM

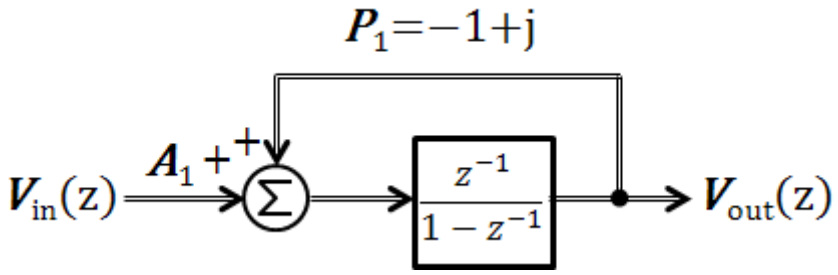
A main building block of a QBDSM is the complex resonator. Fig. 2.4(a) shows a conventional discrete-time (DT) complex resonator realizing by real integrators that have a transfer function $z^{-1}/(1 - z^{-1})$. Assume there is no I/Q mismatch, i.e., $P_{1,re}^{I} = P_{1,re}^{Q} = P_{1,re}, P_{1,im}^{I} = P_{1,im}^{Q} = P_{1,im}, A_{1,re}^{I} = A_{1,re}^{Q} = A_{1,re}, A_{1,im}^{I} = A_{1,im}^{Q} = A_{1,im}$. The resonator's output is:

$$V_{out}(\mathrm{z}) = \frac{\boldsymbol{A}_1 z^{-1}}{1 - (1 + \boldsymbol{P}_1)z^{-1}} V_{in}(z) \tag{2.5}$$

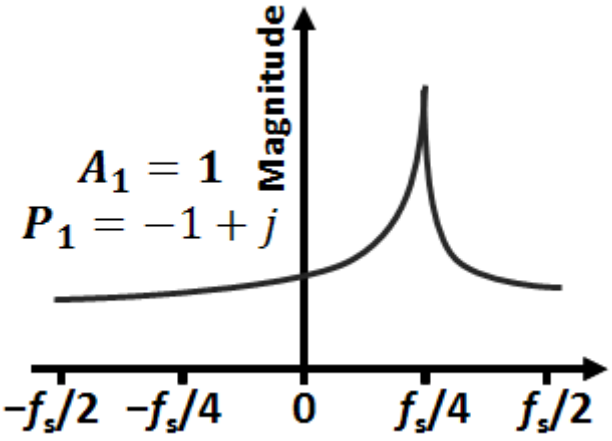
where $\boldsymbol{P}_1 = P_{1,re} + jP_{1,im}$, $\boldsymbol{A}_1 = A_{1,re} + jA_{1,im}$, $V_{in}(z) = V_{in}^I(z) + jV_{in}^Q(z) = \mathcal{Z}\{v_{in}^I + jv_{in}^Q\}$ and $V_{out}(z) = V_{\text{out}}^I(z) + jV_{out}^Q(z) = \mathcal{Z}\{v_{out}^I + jv_{out}^Q\}$ with $\mathcal{Z}\{\cdot\}$ denoting the z-transform. The signal flow diagram of the ideal resonator is simplified in Fig. 2.4(b) using complex coefficients.



(a)



(b)



(c)

Fig. 2.4: (a) Complex resonator realized with real integrators; (b) signal flow diagram with complex representation of coefficients with mismatch; (c) a magnitude plot of the resonator.

When we set $\boldsymbol{P}_1 = -1 + j$ such that the resonator has its pole frequency located at $f_s/4$ (a pole in the resonator translates to a notch in the noise transfer function of the QBDSM), the output is simplified to:

$$V_{out}(\mathrm{z}) = \frac{\boldsymbol{A}_1 z^{-1}}{1 - jz^{-1}} V_{in}(z) \tag{2.6}$$

The transfer function of Eq. (2.6) is plotted in Fig. 2.4(c).

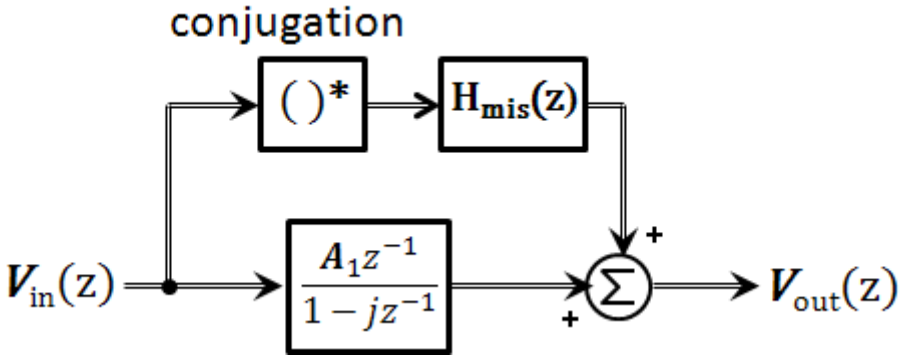


Fig. 2.5. Signal flow diagram of the complex resonator with coefficient mismatches.

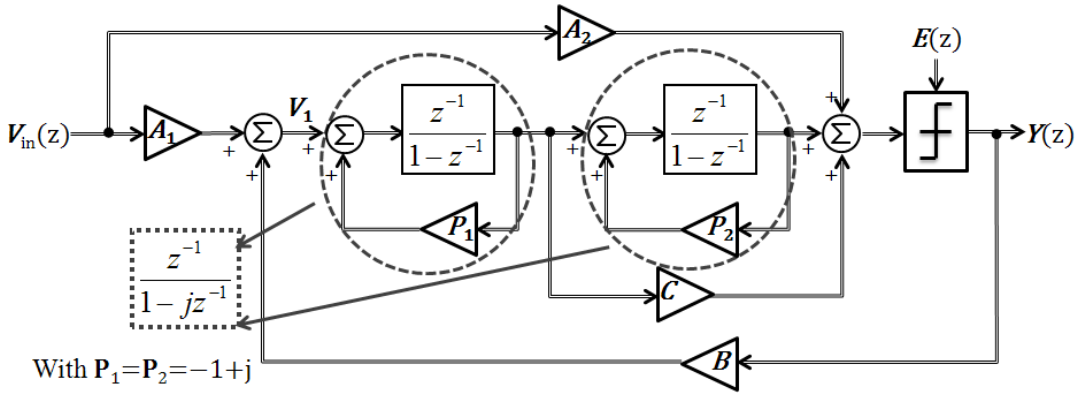


Fig. 2.6 A second order QBDSM with CIFF architecture. All the coefficients and signals are complex here.

Now consider I/Q mismatches between the following pairs of real coefficients: $(A^I_{1,re},\ A^Q_{1,re})$, $(A^I_{1,im},\ A^Q_{1,im})$, $(P^I_{1,re},\ P^Q_{1,re})$, and $(P^I_{1,im},\ P^Q_{1,im})$. We use the complex

mismatch notation defined in Eq. (2.2) ($\boldsymbol{K}$ stands for $\boldsymbol{A}_1$ or $\boldsymbol{P}_1$**)**. Assuming that the magnitudes of the mismatch terms $\Delta\mathbf{A}_1$ and $\Delta\mathbf{P}_1$ are small compared to the magnitude of $\boldsymbol{A}_1$ and $\boldsymbol{P}_1$ respectively and that $\Delta\mathbf{A}_1$ and $\Delta\mathbf{P}_1$ are independent of each other (circuit mismatches are regarded as independent random variables), with steps similar to Eqs. (2.3) and (2.4) one can show that the complex resonator's output becomes:

$$V_{out}(\mathrm{z}) \approx \frac{\boldsymbol{A}_1 z^{-1}}{1 - jz^{-1}} V_{in}(z) + H_{mis}(z) V_{in}^*(z^*) \tag{2.7}$$

where

$$H_{mis}(z) = \frac{z^{-1}}{1 - jz^{-1}} \left(\Delta\boldsymbol{A}_1^* + \boldsymbol{A}_1^* \Delta\boldsymbol{P}_1{}^* \frac{z^{-1}}{1 + jz^{-1}} \right) \tag{2.8}$$

Eq. (2.8) is obtained with the use of the linearity of z-transform ($\mathcal{Z}\{\boldsymbol{v}_{in}^*\} = \mathcal{Z}\{v_{in}^I - jv_{in}^Q\} = V_{in}^I(z) - jV_{in}^Q(z)$) and the property of z-transform on complex conjugation that $\mathcal{Z}\{v_{in}^*\} = V_{in}^*(z^*)$. Compared with Eq. (2.6), a term related to the input's mirror image $V_{in}^*(z^*)$ is added due to the I/Q mismatches on $\boldsymbol{A_1}$ and $\boldsymbol{P_1}$. The signal flow diagram of the resonator in the presence of coefficient mismatch is shown in Fig. 2.5.

Linear-model analysis of the QBDSM shows that it has two complex transfer functions: the signal transfer function (STF) and the noise transfer function (NTF). With I/Q mismatches, there are two additional transfer functions: the $ISTF$ which represents the gain from the image of input to the output; the $INTF$ for the gain from the image of the quantization noise "input" to the output. Consequently, the output of the modulator can be expressed as a sum of four terms:

$$Y(z) = STF(z) \cdot V_{in}(z) + NTF(z) \cdot E(z) + ISTF(z) \cdot V_{in}^{*}(z^{*}) + INTF(z) \cdot E^{*}(z^{*}). \tag{2.9}$$

The $INTF$ plays a critical role in the SNR performance of the QBDSM, and the $ISTF$ plays a critical role in the image-rejection performance of the QBDSM [11].

Next, this research will focus on a second order QBDSM with Chain of Integrators with weighted Feed-Forward summation (CIFF) architecture, which has been realized in silicon, to further illustrate the problem and demonstrate the solution. The CIFF topology uses feed-forward paths rather than feedback ones to create the zeros of the NTF. This results in relaxing the output range and output linearity requirement of the op-amp [12].

The architecture of the modulator is shown in Fig. 2.6, where all the coefficients are complex numbers. Without I/Q mismatch, the QBDSM has $\mathrm{ISTF(z)} = \mathrm{INTF(z)} = 0$. With the resonator pole frequency located at $\mathrm{f_s}/4$, $\mathrm{P_{1,2}} = -1 + \mathrm{j}$, the STF and NTF are:

$$\mathrm{STF(z)} = \frac{\mathrm{A_1 z^{-2}} + \mathrm{A_1 C z^{-1}}(1 - \mathrm{j z^{-1}}) + \mathrm{A_2}(1 - \mathrm{j z^{-1}})^2}{\mathrm{D(z)}} \tag{2.10}$$

$$\mathrm{NTF(z)} = \frac{(1 - \mathrm{j z^{-1}})^2}{\mathrm{D(z)}} \tag{2.11}$$

where $\mathrm{D(z)} = -\mathrm{B z^{-2}} - \mathrm{BC z^{-1}}(1 - \mathrm{j z^{-1}}) + (1 - \mathrm{j z^{-1}})^2$.

With I/Q mismatches, from Eq. (2.9), an ISTF and INTF arise. The modulator coefficients altered by mismatch are denoted by Eq. (2.2), where K stands for any of the modulator coefficients $\mathrm{P_1, P_2, A_1, A_2, B}$ and C in Fig. 2.6. It can be shown that the $\mathrm{STF(z)}$ and $\mathrm{NTF(z)}$ are the same as no mismatch case (Eqs. (2.10) and (2.11)), while the $\mathrm{ISTF(z)}$ and $\mathrm{INTF(z)}$ become:

$$\mathrm{ISTF}(z) \approx \frac{z^{-2}\left(\Delta A_1^* + \triangle B^* A_2^*\right)}{D(z)} + (A_1 + B \cdot A_2)^* \cdot \frac{\triangle P_1^* z^{-3}}{1 + jz^{-1}} \tag{2.12}$$

$$\mathrm{INTF}(z) \approx \frac{z^{-2} \triangle B^* (1 + jz^{-1})^2 + z^{-3} B^* \Delta P_1^* (1 + jz^{-1})}{D(z) D^*(z)} \tag{2.13}$$

Eqs. (2.12) and (2.13) assume that all the coefficient mismatches are small and independent of each other.

A close inspection of Eqs. (2.12) and (2.13) suggests that: (i) the I/Q mismatches of coefficients A_1, P_1 and B (ΔA_1^*, ΔP_1^* and ΔB^*) affect the ISTF, causing the image signal to alias into the signal band, and thus adversely affecting the IRR of the modulator; (ii) I/Q mismatches of coefficients P_1 and B (ΔP_1^* and ΔB^*) affect the INTF, causing the complex conjugate of the quantization noise to alias into the signal band, thus impairing the SNR of the modulator. For the other parameters, such as P_2, A_2, C, thanks to the first or second order noise shaping, their I/Q mismatch induced errors are negligible.

2.3 Proposed High Image-Rejection QBDSM

2.3.1 Technique to remove I/Q mismatches in the first complex resonator (for P_1 in Fig. 2.6)

To investigate the effect of I/Q mismatches associated with the parameter $\boldsymbol{P_1} = -1 + j$ in Fig. 2.6 alone, all the other parameters are assumed to have no I/Q match error. In other words, we let:

$$\Delta \boldsymbol{A_1} = \Delta \boldsymbol{B} = 0. \tag{2.14}$$

The effect on INTF due to the I/Q mismatch of coefficient P_1 is considered

firstly. From Eqs. (2.13) and (2.14), the INTF of the QBDSM becomes:

$$\mathrm{INTF}_{P_1}(z) = \frac{z^{-3}B^*}{|D(z)|^2}\Delta P_1^*(1+jz^{-1}) \tag{2.15}$$

The INTF has a term of $(1+jz^{-1})$, meaning there is a notch at $-f_s/4$ for the response of the complex conjugate of the quantization noise. Fig. 2.7 illustrates this effect: the mismatch tends to fill in the NTF notch of $+f_s/4$ with the noise item $E^*(z^*)\mathrm{INTF}_{P_1}(z)$, which has a notch at $-f_s/4$. Here it is assumed the desired signal $V_{in}(z)$ is located at $+f_s/4+\Delta f_{in}$, and the undesired image signal $V_{img}(z)$ is located at $-f_s/4-\Delta f_{img}$ respectively.

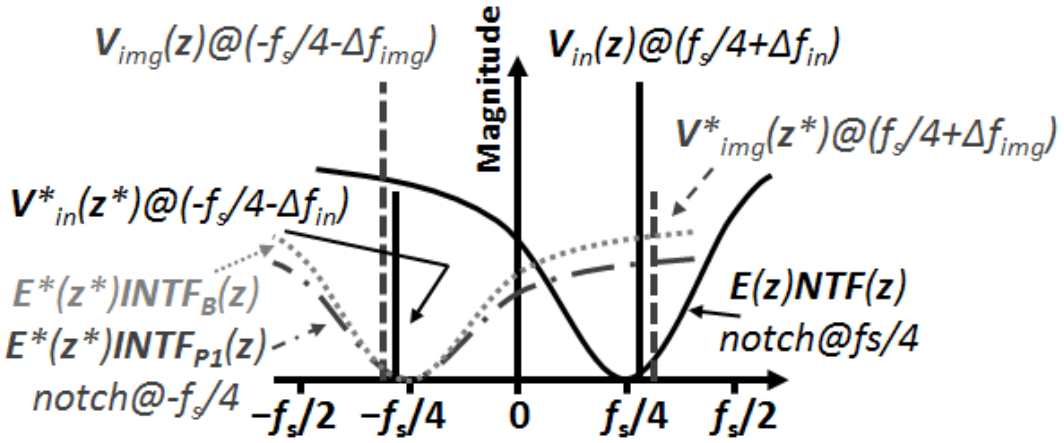
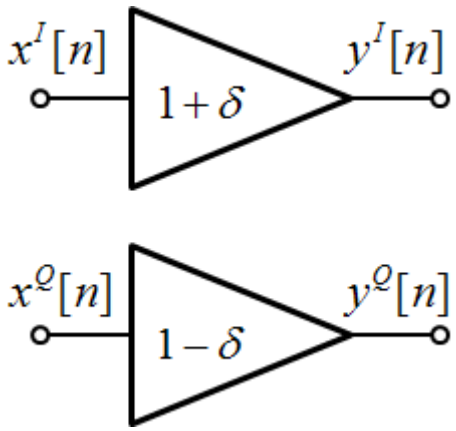
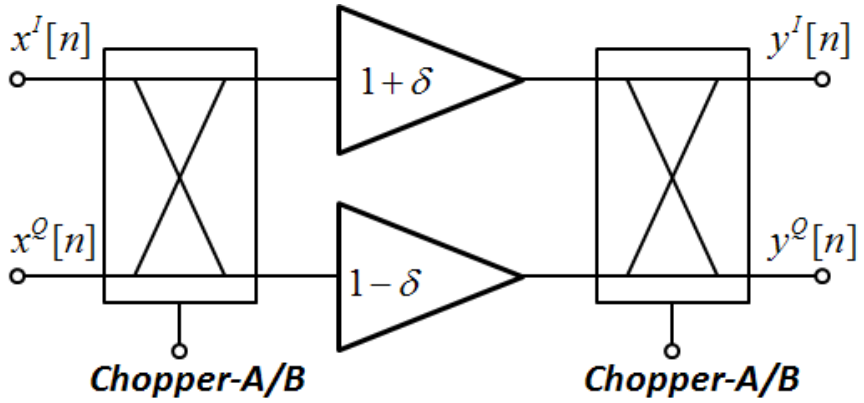


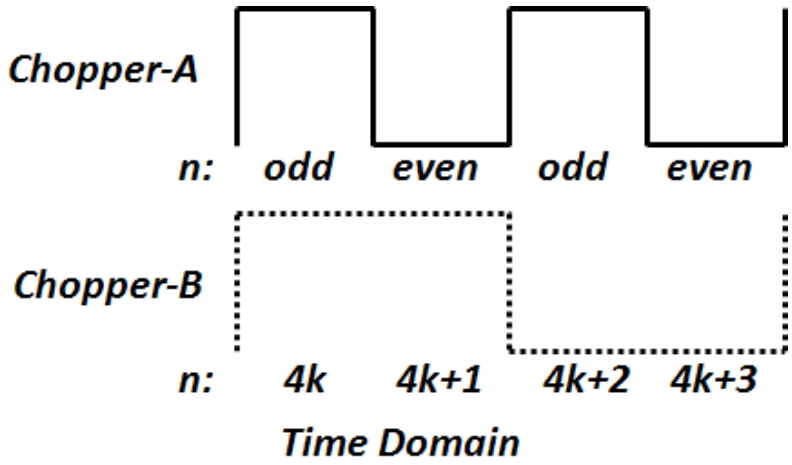
Fig. 2.7 Qualitative illustration of I/Q mismatch effects in the QBDSM.



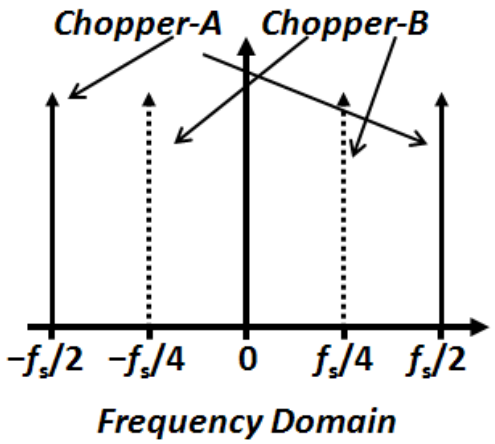
(a)



(b)



(c)



(d)

Fig. 2.8 Complex unity gain block: (a) with mismatch; (b) with Chopper-A or B; (c) Chopper-A and B in the time domain; (d) Chopper-A and B in the frequency domain.

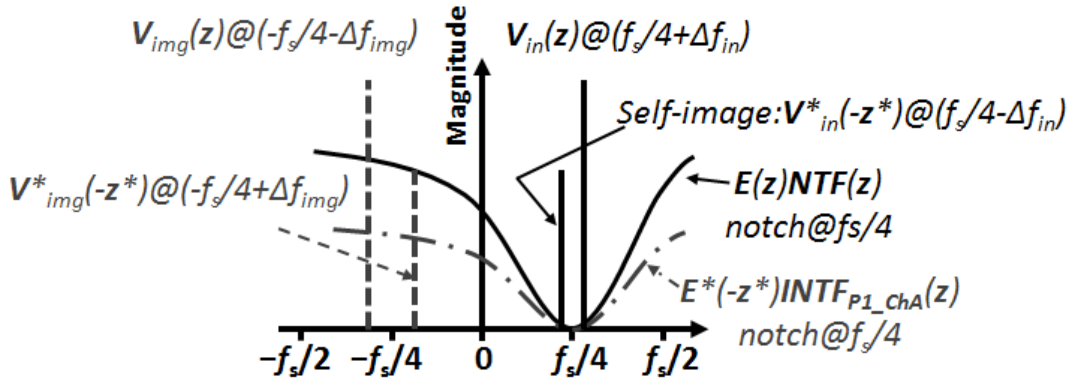


Fig. 2.9 Qualitative illustration of the effect of applying Chopper-A on parameter $\mathbf{P_1}$ of the QBDSM.

The chopper (a special case of DEM) technique in [8] is commonly used to suppress mismatches. This technique, referred to as Chopper-A here, is employed to suppress the I/Q mismatches associated with parameter P_1 in this work. The operation of Chopper-A is shown in Fig. 2.8 (c) and (d) in the time and frequency domain respectively. For even input samples, the complex resonator operates in its normal way. For odd input samples, the real and imaginary paths are swapped. The chopper frequency is $f_s/2$.

Consider a complex unity gain block with I/Q gain mismatch of δ as shown in Fig. 2.8(a) [8]. Chopper-A operation generates an output $y[n]$ as shown in Fig. 2.8(b), n being the integer time index, of

$$y[n] = x[n] + (-1)^n \delta x^*[n] \tag{2.16}$$

when responding to a complex input $x[n]$. The complex conjugate of $x[n]$ is thus multiplied by δ and $(-1)^n$, i.e., $\cos(n\pi)$, or $(e^{j\pi n} + e^{-j\pi n})/2$. This means the complex conjugate term, $x^*[n]$, is mixed with tones at $\pm f_s/2$. In the z-domain, we have $\mathcal{Z}\{x^*[n]\} = X^*(z^*)$. The mixing of $x^*[n]$ with $(e^{j\pi n} + e^{-j\pi n})/2$ is equivalent

to replacing the z variable ($z = e^{j\omega}$, ω being the angular frequency) in $X^*(z^*)$ by $e^{j(\omega+\pi)}(= -z)$ and $e^{j(\omega-\pi)}(= -z)$, and then taking their average. So, the z-domain expression for Eq. (2.16) is:

$$Y(z) = X(z) + \delta X^*(-z^*) \tag{2.17}$$

Similarly, when Chopper-A operation is applied on the complex resonator parameter P_1 (on both the real and imaginary parts of P_1), the INTF changes from Eq. (2.15) to:

$$INTF_{P_{1\_ChA}}(z) = INTF_{P_1}(-z) = \frac{-z^{-3}B^*}{|D(-z)|^2}\Delta P_1^*(1 - jz^{-1}) \tag{2.18}$$

The term $(1 + jz^{-1})$ in Eq. (2.15) becomes $(1 - jz^{-1})$ now. So the notch of the INTF is shifted from $-f_s/4$ to $+f_s/4$, coinciding with the notch of the NTF of the QBDSM [8], as illustrated in Fig. 2.9. As a result, the quantization noise does not fold into the signal band around $+f_s/4$.

Now the effect of the I/Q mismatch associated with coefficient P_1 on ISTF is investigated. From Eqs. (2.12) and (2.14), the ISTF of the QBDSM becomes:

$$ISTF_{P_1}(z) \approx (A_1 + B \cdot A_2)^* \cdot \frac{\Delta P_1^* z^{-3}}{1 + jz^{-1}} \tag{2.19}$$

Considering the ISTF only, the output of the modulator is:

$$Y_{P_1}(z) = ISTF_{P_1}(z) \cdot V_{in}^*(z^*) \tag{2.20}$$

where $V_{in}^*(z^*)$ refers to the mirror image of $V_{in}(z)$ around DC. With Chopper-A to avoid the noise item $E^*(z^*)INTF_{P_1}(z)$ discussed above in this section, the output becomes:

$$Y_{P_1}(z) = ISTF_{P_1}(-z) \cdot V_{in}^*(-z^*) \tag{2.21}$$

Here $V_{in}^*(-z^*)$, the mirror image of $V_{in}(z)$ around its center frequency, is called

self-image, the spectrum of which is that of $V_{in}^{*}(z^{*})$ shifted by $\pm f_s/2$ as shown in Fig. 2.9. If there is an input signal at $\frac{1}{4}f_s + \Delta f_{in}$ entering the first complex resonator, then this signal will leak to $\frac{1}{4}f_s - \Delta f_{in}$ due to the mismatch on parameter P_1 and the Chopper-A applied. The self-image impairs the SNDR of the QBDSM.

However, if we can make $A_1 + B \cdot A_2 = 0$ in the synthesis of the coefficients of the QBDSM shown in Fig. 2.6, the ISTF in Eq. (2.19) becomes zero. Moreover, the STF in Eq. (2.10) becomes:

$$STF(z) = A_2 \tag{2.22}$$

Then the input to the first integrator, V_1 shown in Fig. 2.6, is:

$$V_1(z) = A_1 \cdot V_{in}(z) + B \cdot Y(z) = B \cdot E(z) \cdot NTF(z) \tag{2.23}$$

It does not contain the signal input $V_{in}(z)$, but only the quantization noise $E(z)$.

With the condition $A_1 + B \cdot A_2 = 0$, we get:

$$ISTF_{P_1}(-z) = ISTF_{P_1}(z) = 0 \tag{2.24}$$

From Eqs. (2.21) and (2.24), it can be seen the self-image is removed. So this condition is assumed hereafter in this research.

Moreover, if mismatch is considered, $A_1 + B \cdot A_2 = \Delta\eta \neq 0$, then Eq. (2.19) becomes:

$$ISTF_{P_1}(z) = \Delta\eta^{*} \cdot \frac{\Delta P_1^{*} z^{-3}}{1 + jz^{-1}} = \frac{(\Delta\eta \cdot \Delta P_1)^{*} z^{-3}}{1 + jz^{-1}} \tag{2.25}$$

The magnitude of the product $\Delta\eta \cdot \Delta P_1$ is very small and the resulted mismatch effect can thus be ignored. Nevertheless, it shows that the self-image cannot be completely avoided.

2.3.2 Technique to remove I/Q mismatches in the Feedback DAC (for $\boldsymbol{B}$ in Fig. 2.6)

We consider the effect of I/Q mismatches associated with the feedback parameter B (see Fig. 2.6) alone in this subsection. Let

$$\Delta \boldsymbol{A}_1 = \Delta \boldsymbol{P}_1 = 0 \tag{2.26}$$

then:

$$ISTF_B(z) = \frac{z^{-2}\boldsymbol{A}_2^*\Delta \boldsymbol{B}^*}{D(z)} \tag{2.27}$$

$$INTF_B(z) = \frac{z^{-2}\Delta \boldsymbol{B}^*}{|D(z)|^2}(1+jz^{-1})^2 \tag{2.28}$$

The mismatch associated with feedback DAC influences both the $ISTF$ and $INTF$. As shown in Fig. 2.7, both the undesired image signal and the image of the quantization noise are aliased into the desired signal band, impairing the SNDR of the modulator.

The Chopper-A operation can be used to mitigate this mismatch effect as well. With Chopper-A on $\boldsymbol{B}$ (on both B_{re} and B_{im}), the $INTF$ becomes:

$$INTF_{B\_ChA}(z) = INTF_B(-z) = \frac{z^{-2}\Delta \boldsymbol{B}^*}{|D(-z)|^2}(1-jz^{-1})^2 \tag{2.29}$$

The $INTF$ becomes 2nd order noise shaped with a notch at $+f_s/4$, i.e., the signal band. So Chopper-A can reject the image of the quantization noise at the signal band.

Meanwhile, the $ISTF$ becomes:

$$ISTF_{B\_ChA}(z) = ISTF_B(-z) = \frac{z^{-2}\boldsymbol{A}_2^*\Delta \boldsymbol{B}^*}{D(-z)} \neq 0 \tag{2.30}$$

The self-image is also produced when Chopper-A is applied on parameter $\boldsymbol{B}$. The reason is the same as that when Chopper-A is applied on parameter $\boldsymbol{P}_1$ if $A_1 + B \cdot$

$A_2 \neq 0$ discussed above. As shown in Fig. 2.9, the self-image $V_{in}^*(-z^*)$ located at $f_s/4 - \Delta f_{in}$ impairs the SNDR of the QBDSM.

In summary, when Chopper-A is applied on parameter $\boldsymbol{B}$, the self image arises, impairing the SNDR of the modulator.

A solution to this self-image problem is to make $\Delta\boldsymbol{B} = 0$. This can be achieved by sharing the feedback DAC branch between I/Q channels and applying the "I/Q channel multiplexing" scheme. The implementation details are presented in section 2.4. By this arrangement of making $\Delta\boldsymbol{B} = 0$, we have:

$$ISTF_B(z) = 0,\ \ INTF_B(z) = 0\ ,\ \ ISTF_B(-z) = 0 \tag{2.31}$$

So the image signal, image quantization noise and self-image signal do not impair the SNDR of the modulator.

2.3.3 Technique to remove I/Q mismatches in the Input Coefficient (for A_1 in Fig. 2.6)

In this subsection, we consider the effect of I/Q mismatches associated with the input parameter A_1 (see Fig. 2.6) alone. Let

$$\Delta\boldsymbol{P}_1 = \Delta\mathbf{B} = 0 \tag{2.32}$$

Then the $ISTF$ and $INTF$ of the QBDSM become:

$$ISTF_{A_1}(z) = \frac{z^{-2}\Delta\boldsymbol{A}_1^*}{D(z)} \tag{2.33}$$

$$INTF_{A_1}(z) = 0 \tag{2.34}$$

The mismatch on the input branches only influences the $ISTF$, as the quantization noise does not go through the input branches. Fig. 2.7 shows only the image signal,

not the $E^*(z^*)$, is aliased into the signal band ($V^*_{img}(z^*)$) to impair SNDR performance.

Applying Chopper-A to parameter $\boldsymbol{A_1}$ causes self-image problem, just as in the case for parameter $\boldsymbol{B}$. Unlike for parameter $\boldsymbol{B}$, sharing the input signal branches between I and Q channels is not feasible because the input signals for I and Q channels must be sampled simultaneously by different sampling capacitors.

Two schemes to overcome the mismatch on the parameter $\boldsymbol{A_1}$ are proposed below.

2.3.3.1 Chopper-B

An alternative chopper operation, called "Chopper-B", is used. Its operations in the time and frequency domain are shown in Fig. 2.8 (c) and (d) respectively. When the DT time index n is $4k$ or $4k+1$, where k is a positive integer, the real paths and the imaginary paths for A_1 are swapped; when n is $4k+2$ or $4k+3$, the paths for the complex coefficient A_1 remain their normal configuration. Note that the chopper frequency here is $f_s/4$ while it is $f_s/2$ in Chopper-A. It is also noted that chopper-B itself is a common chopper, however, to the best of our knowledge, there is no other reported work using Chopper-B to remove the self-image.

When Chopper-B is applied on a complex unity gain stage with I/Q imbalance δ as shown in Fig. 2.8(b), then,

$$y[n] \approx x[n] + (-1)^{\lceil \frac{n}{2} \rceil} \delta x^*[n] \tag{2.35}$$

The complex conjugate term $x^*[n]$ is multiplied by the sequence $(-1)^{\lceil \frac{n}{2} \rceil} =$

$1, 1, -1, -1, 1, 1$ .... The latter can be represented by a cosine function:

$$(-1)^{\lfloor \frac{n}{2} \rfloor} = \frac{\sqrt{2}}{2}\left[e^{j\left(\frac{n\pi}{2}-\frac{\pi}{4}\right)} + e^{-j\left(\frac{n\pi}{2}-\frac{\pi}{4}\right)}\right] \tag{2.36}$$

This means the complex conjugate term, $x^*[n]$, is mixed with tones at $\pm f_s/4$. In the z-domain, the mixing of $x^*[n]$ with $e^{j\left(\frac{n\pi}{2}-\frac{\pi}{4}\right)} + e^{-j\left(\frac{n\pi}{2}-\frac{\pi}{4}\right)}$ is equivalent to replacing the z variable ($z = e^{j\omega}$, ω being the angular frequency) in $X^*(z^*)$ by $e^{j(\omega+\frac{\pi}{2})}(= jz)$ and $e^{j(\omega-\frac{\pi}{2})}(= -jz)$. So, the z-domain expression for Eq. (2.35) is:

$$Y(z) = X(z) + \delta\frac{\sqrt{2}}{2}\left[e^{-j\frac{\pi}{4}}X^*((jz)^*) + e^{j\frac{\pi}{4}}X^*((-jz)^*)\right] \tag{2.37}$$

Similar to the function of Chopper-A discussed above, the aliased image term $V^*_{img}(z^*)$ and $V^*_{in}(z^*)$ are mixed with a cosine at $f_s/4$ when Chopper-B is applied. It is shifted to the left and right by $f_s/4$. Both the desired signal around $f_s/4$ and the image around $-f_s/4$ will end up appearing around DC and $f_s/2$ as a result of the mismatches on A_1 and the Chopper-B applied. So both the image and self-image problem are avoided. As shown in Fig. 2.10, there is no aliased image and self-image signal in the desired signal band.

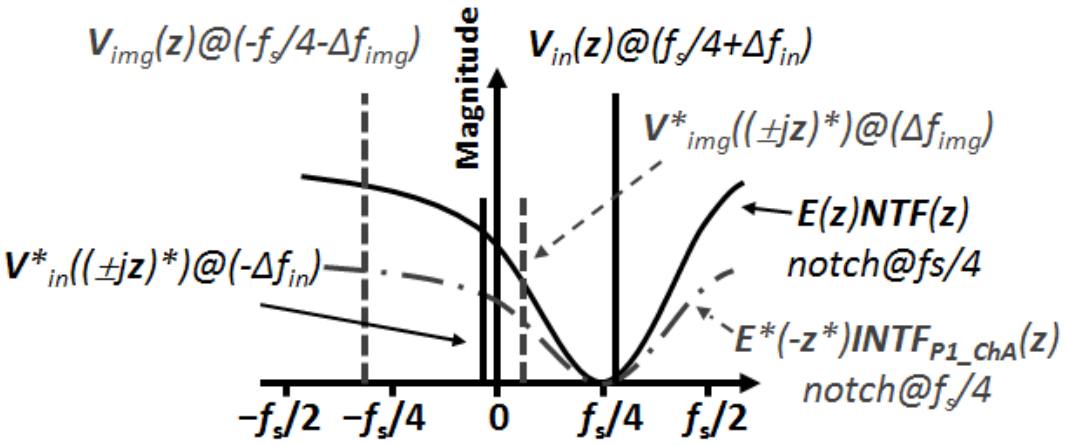


Fig. 2.10 Qualitative illustration of the effect of applying Chopper-B on parameter $\mathbf{A_1}$of the QBDSM.

A consequence of Chopper-B operation on A_1 is that signals originally around DC and $f_s/2$ will be aliased to the signal band of $f_s/4$. Signals around $f_s/2$ are not a problem because these are attenuated by the anti-aliasing filter required before the SC modulator. DC offset is a problem. However, it is only the mismatch-caused residue component of the DC offset that will end up at the signal band. For a 1% difference between the I and Q paths of the real or imaginary part of A_1, the DC offset will be suppressed by 46 dB when it appears in the signal band. The DC offset here is much less of a problem than it is in the direct conversion receiver, where the DC offset is not attenuated at all.

2.3.3.2 "Bilinear" Operation

A double-sampling resonator by two cross-coupled delay cells with a bilinear-transformed input circuit was reported in [2] so that noise and signals exhibits first-order shaping before folding to the band of interest. However, the mismatch between the double-sampling branches (in addition to the mismatch between I/Q paths) introduces self-image, which needs to be cancelled by an offline calibration strategy. In this research, a new resonator with bilinear-transformed input is proposed as shown in Fig.2.11. It uses cross-coupled real integrators instead of cross-coupled delay cells, and there are no double-sampling branches for avoiding self-image.

The output of the modified bilinear resonator is:

$$Y_{out}(z) = \frac{A_1(1+jz^{-1})}{1-jz^{-1}} V_{in}(z) + H_{mis,bili}(z) V_{in}^{*}(z^{*}) \tag{2.38}$$

where

$$H_{mis,bili}(z) = \Delta A_1^* \frac{(1 - jz^{-1})}{(1 - jz^{-1})} \tag{2.39}$$

Rewrite Eq. (2.8) with $\Delta P_1 = 0$ here for comparison:

$$H_{mis}(z) = \Delta A_1^* \frac{z^{-1}}{(1 - jz^{-1})} \tag{2.40}$$

Eq. (2.39) shows that the image component $V_{in}^*(z^*)$ is filtered by the complex notch filter $1 - jz^{-1}$ when comparing to the case where the bilinear transform is not applied (see Eq. (2.40)). Therefore, the image rejection capability of the modulator can be improved effectively.

With the bilinear transform, the input signal $V_{in}(z)$ is filtered by an extra complex notch filter $(1 + jz^{-1})$. Although $(1 + jz^{-1})$ is almost constant in the signal band around $f_s/4$, the STF of the original QBDSM is changed and the input V_1 to the first integrator contains some portion of signal $V_{in}(z)$ and a self-image is induced when Chopper-A is applied on parameter P_1 in the first complex resonator, just like what we have discussed with Eq. (2.21).

Fig. 2.12 shows a new bilinear QBDSM architecture to solve the self-image problems. The differences from Fig. 2.6 are: the input capacitor branch A_1 is bilinear and the feed-forward branch A_2 in Fig. 2.6 is removed. The parameter "D" is just for scaling purpose to make the second op-amp's output swing within a reasonable range, and it can be ignored in the analysis.

The modulator has:

$$STF_{bili}(z) = \frac{A_1 z^{-1}(1 + jz^{-1}) + A_1 C(1 + jz^{-1})(1 - jz^{-1})}{D(z)} \tag{2.41}$$

$$NTF_{bili}(z) = \frac{(1 - jz^{-1})^2}{D(z)} \tag{2.42}$$

The input to the first complex resonator is:

$$\begin{aligned} & V_{in}(z) \cdot A_1(1 + jz^{-1}) + Y(z)Bz^{-1} \\ & \quad = \frac{A_1(1 + jz^{-1})}{D(z)}(1 - jz^{-1})^2 \cdot V_{in}(z) + E(z) \cdot B \\ & \quad \cdot NTF(z)z^{-1} \end{aligned} \tag{2.43}$$

Eq. (2.43) shows that in the proposed QBDSM architecture the desired input signal $V_{in}(z)$ is first filtered by the second order complex notch filter $(1 - jz^{-1})^2$ before feeding to the first complex resonator. So the self-image problem concerned above is avoided effectively. It also reduces distortion because no input signal component but only quantization noise is injected to the first complex resonator.

Compared with [2], here the bilinear transform has only been implemented for the input branch $\mathbf{A_1}$, but not for the feedback DAC branch **B**. So the poles of STF and the NTF do not change and the stability of QBDSM is not influenced. The modulator has its ISTF and INTF changed to:

$$ISTF_{A_1,bili}(z) = \frac{z^{-1}}{D(z)}\Delta A_1^*(1 - jz^{-1}) \tag{2.44}$$

$$INTF_{A_1,bili}(z) = 0 \tag{2.45}$$

As shown in Fig. 2.13, the aliased image signal $V_{img}^*(z^*)$ is filtered by the complex notch filter $1 - jz^{-1}$, thus improving the IRR and SNDR of the modulator effectively.

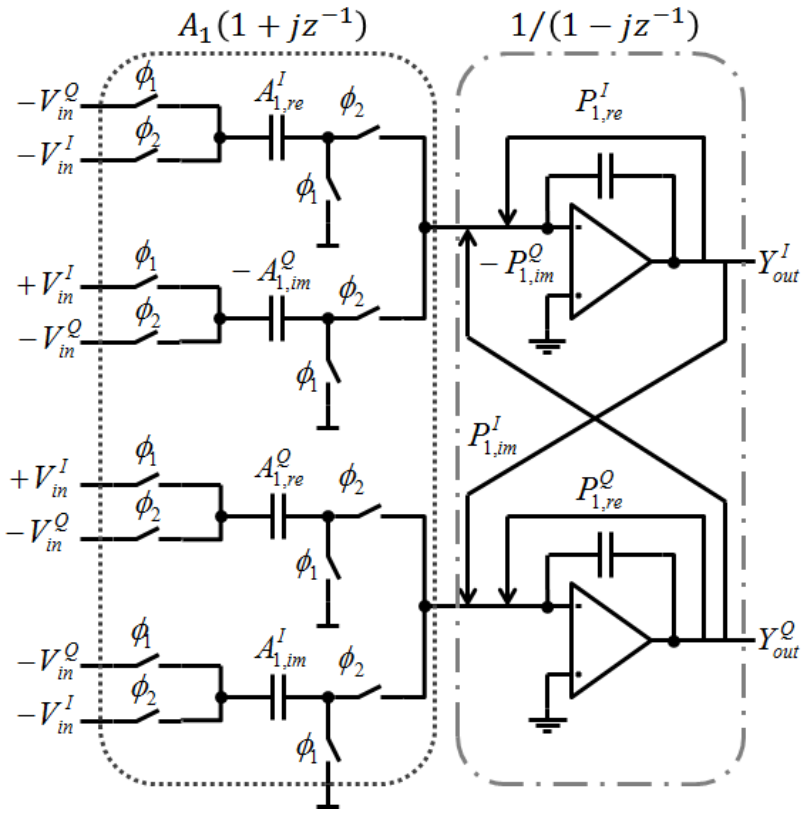


Fig. 2.11 Simplified SC complex resonator with bilinear transformed input.

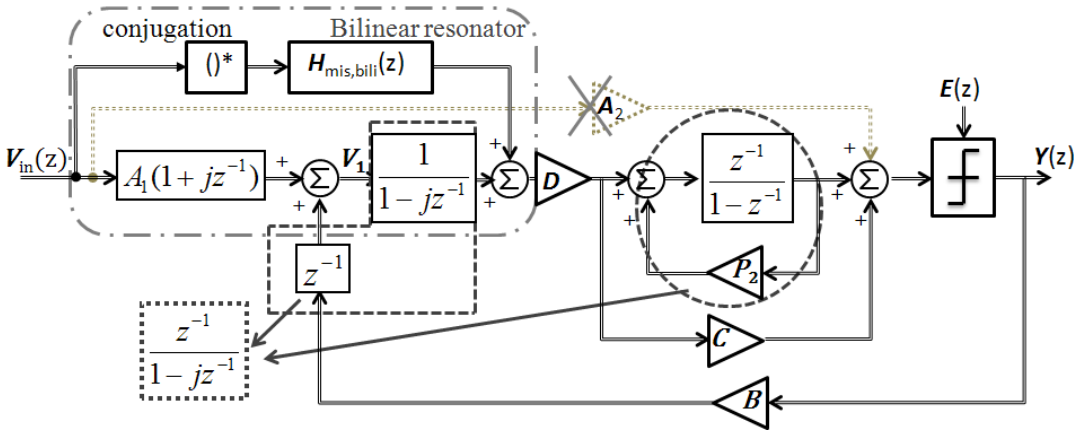


Fig. 2.12 New QBDSM architecture with bilinear-transformed input to remove self-image.

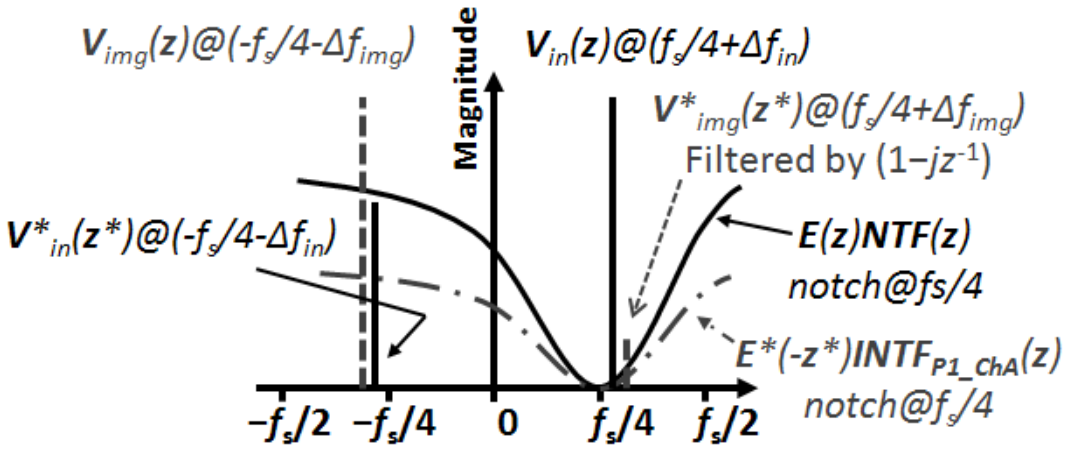


Fig. 2.13 Qualitative illustration of the effect of applying bilinear transform on parameter $\mathbf{A_1}$ of the QBDSM.

2.3.4 Summary and Simulation Results

The proposed techniques to tackle I/Q mismatches in the SC QBDSM are summarized in Table I. To suppress the effect associated with the input coefficient $\boldsymbol{A_1}$, there are two options: Chopper-B or the bilinear transform technique. The group of the techniques that includes Chopper-B on $\boldsymbol{A_1}$ is called Scheme I here; the group that includes the bilinear transform technique on $\boldsymbol{A_1}$ is called Scheme II.

Behavioral simulations have been conducted to verify the feasibility of two proposed mismatch cancellation schemes. In the simulations, when considering the I/Q mismatch associated with any modulator coefficient K, a fixed 2% mismatch is set as follows: $\mathrm{K}_{\mathrm{re}}^{\mathrm{I}} = \mathrm{K}_{\mathrm{re}} + 1\% \cdot \mathrm{K}_{\mathrm{re}}$; $\mathrm{K}_{\mathrm{im}}^{\mathrm{I}} = \mathrm{K}_{\mathrm{im}} + 1\% \cdot \mathrm{K}_{\mathrm{im}}$; $\mathrm{K}_{\mathrm{re}}^{\mathrm{Q}} = \mathrm{K}_{\mathrm{re}} - 1\% \cdot \mathrm{K}_{\mathrm{re}}$ and $\mathrm{K}_{\mathrm{im}}^{\mathrm{Q}} = \mathrm{K}_{\mathrm{im}} - 1\% \cdot \mathrm{K}_{\mathrm{im}}$ (see Eq.(2.2)).

The simulated output power spectral densities (PSDs) are shown from Fig. 2.14 to Fig. 2.21. In estimating the PSD [21] in Fig. 2.14 to Fig. 2.21, eight 32k-point Fast Fourier Transforms (FFTs) are computed and their magnitude average is used as the

PSD.

The effect of each of the techniques in Scheme I is shown from Figs.2.14 to 2.16. The output PSDs of the QBDSM with all the techniques in Scheme I turned on, with and without mismatches, are shown in Fig. 2.17. It can be observed that the aliased image quantization noise and image signal are effectively eliminated. The IRR is improved from 39.4 dB to 84.9 dB, and the in-band noise power is reduced from –48.8 dBFS to –79.1 dBFS, which is just 2 dB higher than the no-mismatch case.

The effect of each of the techniques in Scheme II is shown from Figs. 2.18 to 2.20. The output PSDs of the QBDSM with all the techniques in Scheme II turned on, with and without mismatches, are shown in Fig. 2.21. It is found that the aliased image quantization noise and image signal are effectively erased. The IRR is improved from 34.4 dB to 78.7 dB, and the in-band noise power is reduced from –38.9 dBFS to –79.8 dBFS, which is only 3.8 dB higher than the no-mismatch case.

The spurious free dynamic range (SFDR) versus amount of I/Q mismatch with and without the proposed schemes are plotted in Fig. 2.22. It shows that with the proposed schemes, the SFDR can be improved by more than 30 dB for mismatch ranging from 1% to 10%. Table II summarizes the simulated performance of the two schemes.

Table I Summary on techniques in Scheme I and Scheme II.

Techniques for:	Mismatch on A_1	Mismatch on B	Mismatch on P_1	Self-image
Scheme I on QBDSM in Fig. 6	Chopper-B	Capacitor Sharing + I/Q Multiplex	Chopper-A	$A_1 + B \cdot A_2 = 0$ with CIFF (Fig. 6)
Scheme II on QBDSM in Fig. 12	Bilinear Transform	Capacitor Sharing+ I/Q Multiplex	Chopper-A	A new QBDSM Architecture (Fig. 12)

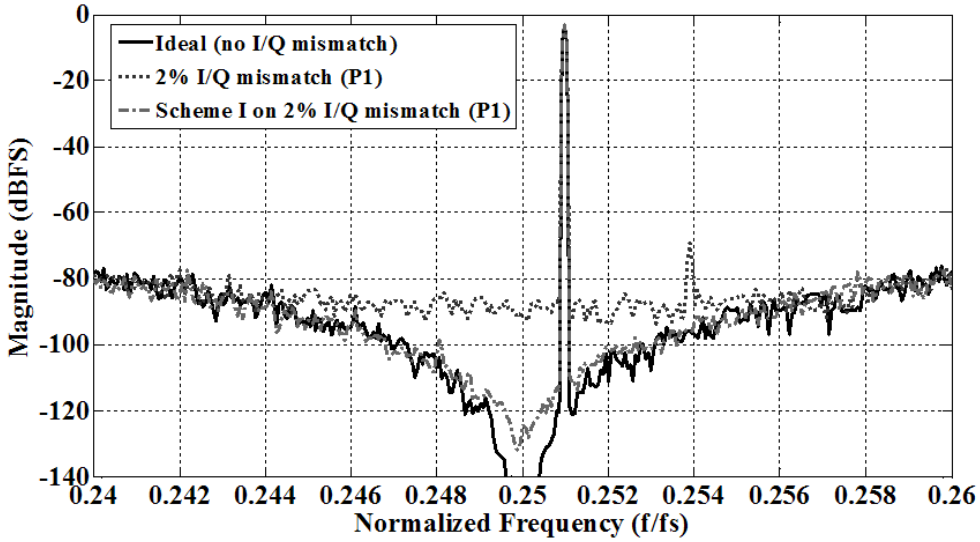


Fig. 2.14 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.6 with the Chopper-A of Scheme I applied on P_1.

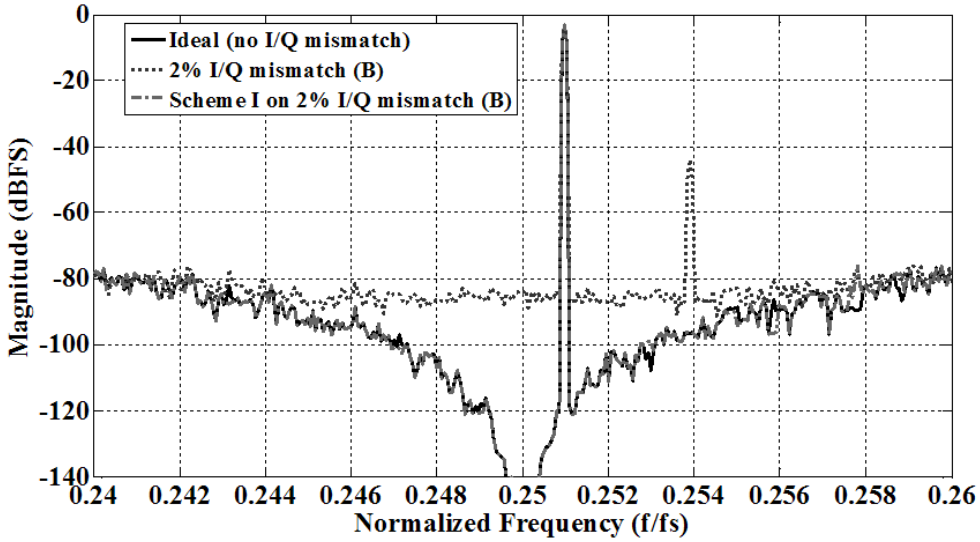


Fig. 2.15 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.6 with the

"capacitor sharing" technique of Scheme I applied on $\boldsymbol{B}$.

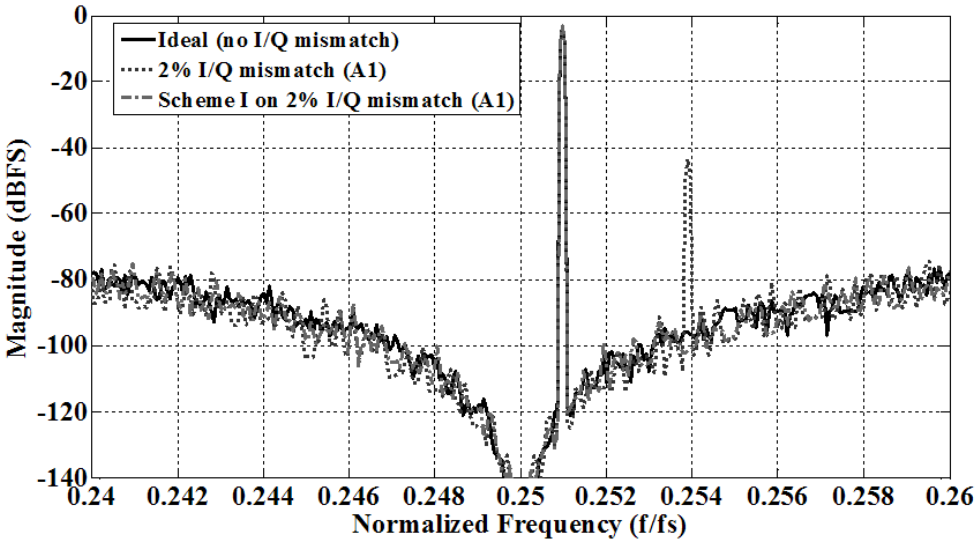


Fig. 2.16 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.6 with Chopper-B of Scheme I applied on $\boldsymbol{A_1}$.

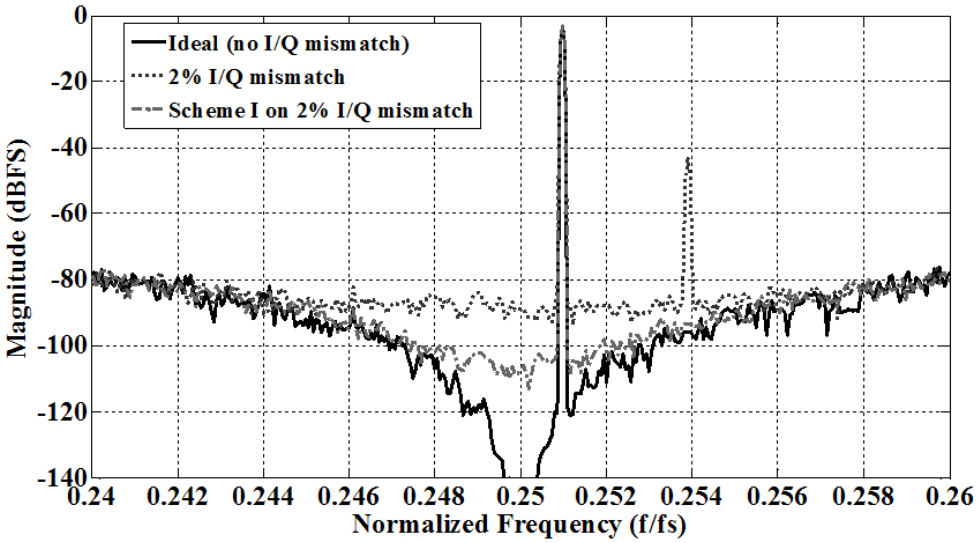


Fig. 2.17 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.6 with all the techniques in Scheme I applied.

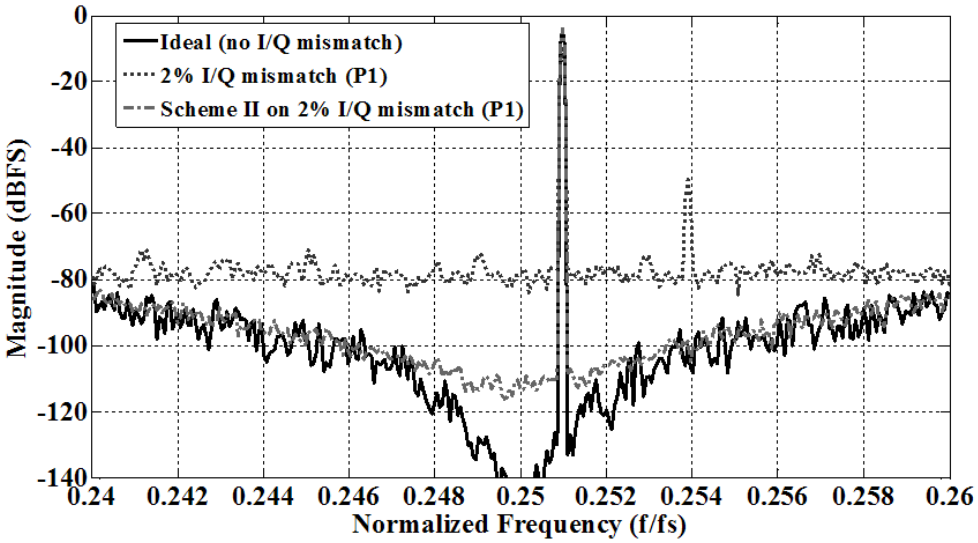


Fig. 2.18 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.12 with the Chopper-A of Scheme II applied on $\boldsymbol{P_1}$.

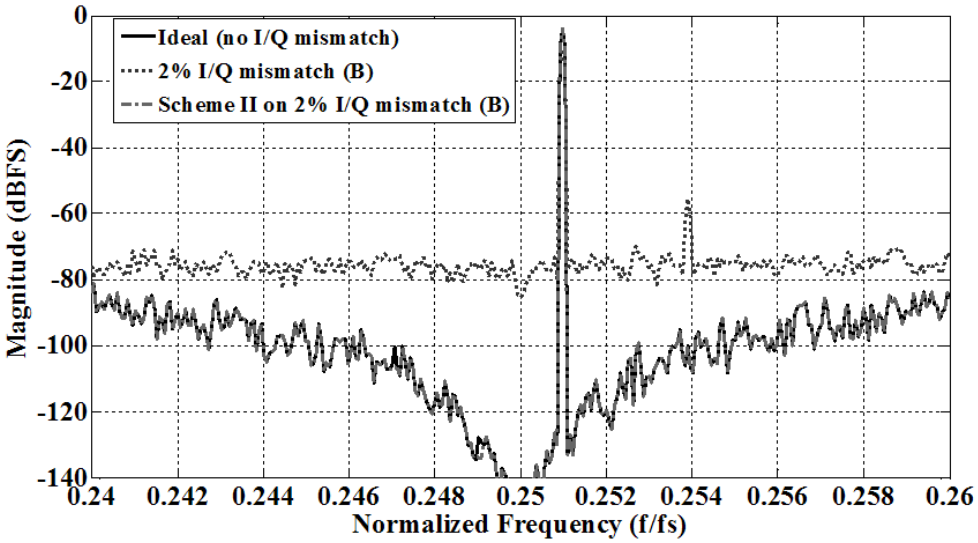


Fig. 2.19 Behavioral simulated output PSD (32k points) of the QBDSM in Fig. 2.12 with the "capacitor sharing" technique of Scheme II applied on $\boldsymbol{B}$.

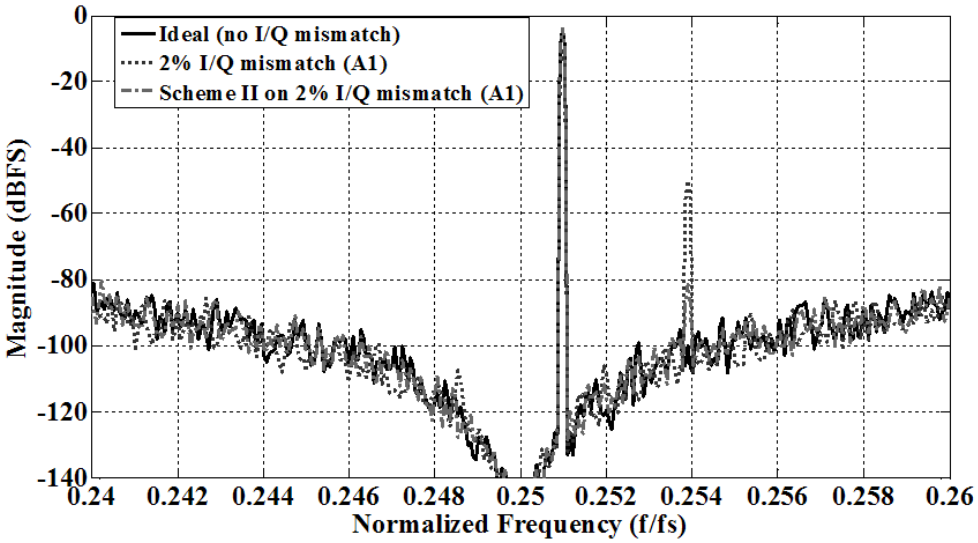


Fig. 2.20 Behavioral simulated output PSD (32k points) of QBDSM in Fig. 2.12 with the Bilinear transform technique of Scheme II applied on $\boldsymbol{A_1}$.

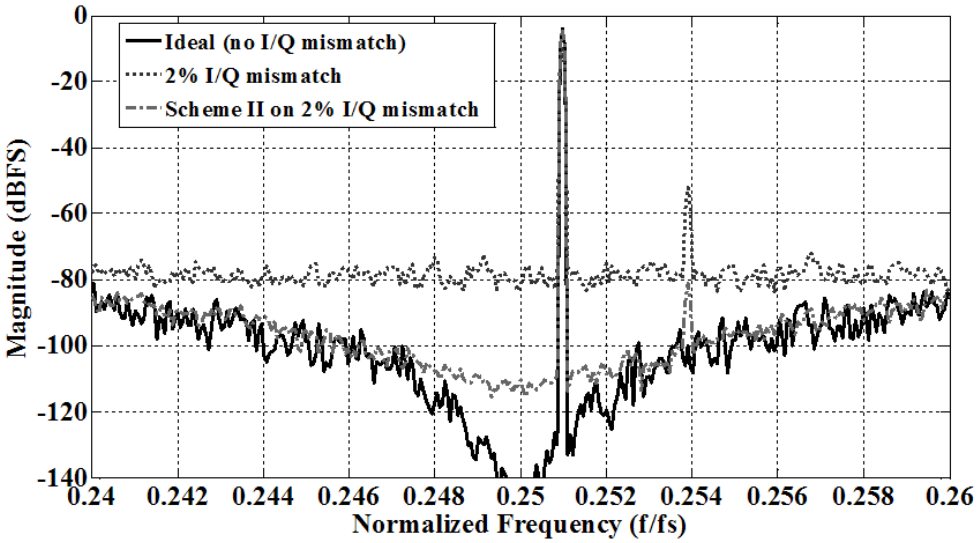


Fig. 2.21 Behavioral simulated output PSD (32k points) of QBDSM in Fig. 2.12 with all the techniques in Scheme II applied.

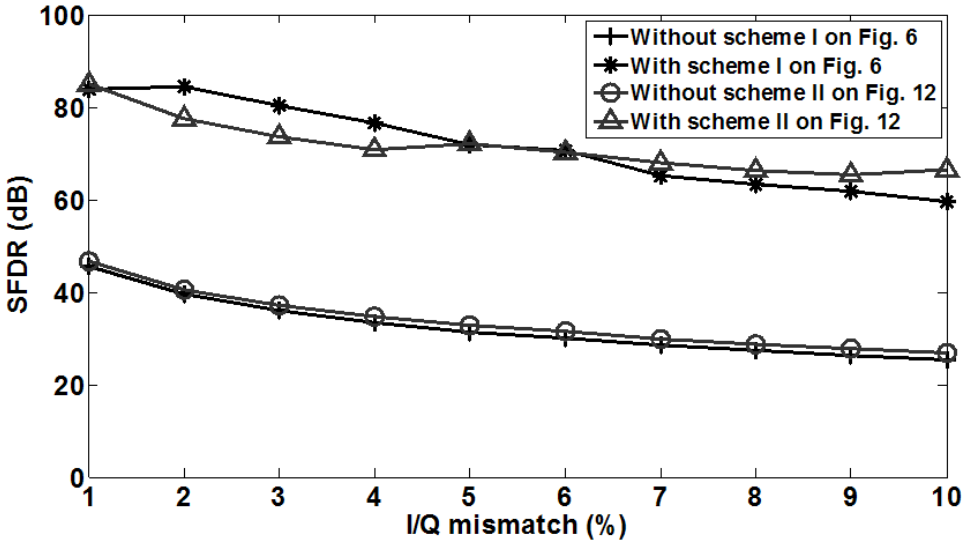


Fig. 2.22 Simulated SFDR versus amount of I/Q mismatch with and without the proposed schemes.

Table II Comparison of behavioral, transistor-level simulation and measurement results.

Objective	Verification Method	Condition	IRR(dB)	In-band Noise Power (dBFS)
Scheme I on QBDSM in Fig. 6	Behavioral Level Simulation	Ideal (no I/Q mismatch)	Infinite	–81.1
		2% I/Q mismatch	39.4	–48.8
		Scheme I on 2% I/Q mismatch	84.9	–79.1
	Transistor Circuit Level		79	-77.2
	Measurement	Fabricated Chip	73	-72
Scheme II on QBDSM in Fig. 12	Behavioral Level Simulation	Ideal (no I/Q mismatch)	Infinite	–83.6
		2% I/Q mismatch	34.4	–38.9
		Scheme II on 2% I/Q mismatch	78.7	–79.8
	Transistor Circuit Level		75	-77.8

2.4 I/Q Multiplexing Schemes and Circuit Implementation of the QBDSM

To minimize certain I/Q mismatches and to reduce chip area, op-amp, feedback DAC capacitors and quantizer are shared between I and Q channels for the presented QBDSM. In other words, multiplexing of the I and Q signals through a common circuitry is implemented. There are several blocks in the signal processing chain in the modulator, including the resonator, the feedback DAC and the quantizer. The multiplexing schemes for each of them are presented below.

Fig. 2.23 shows the conventional SC complex resonator circuit [1]. There are two clock phases, namely, sampling (ϕ_1) and integration (ϕ_2). The upper and lower channels can share one op-amp instead of using two. An op-amp sharing scheme is illustrated in Fig. 2.24, where one clock period is divided into four phases. ϕ_1 and ϕ_2 are sampling for Q and I channel respectively. ϕ_3 and ϕ_4 are integration for I and Q channel respectively. The negative valued capacitors in Fig. 2.24 are easily realized in the actual fully-differential implementation.

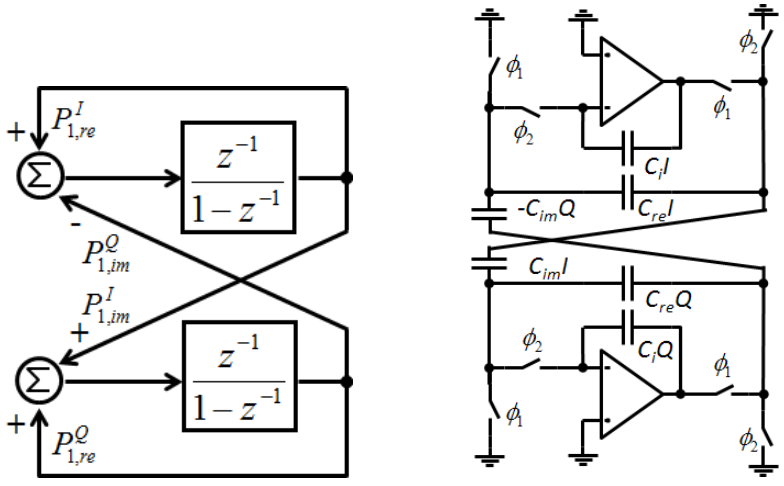


Fig. 2.23 The conventional SC complex resonator. ϕ_1 and ϕ_2 are non-overlapping clocks.

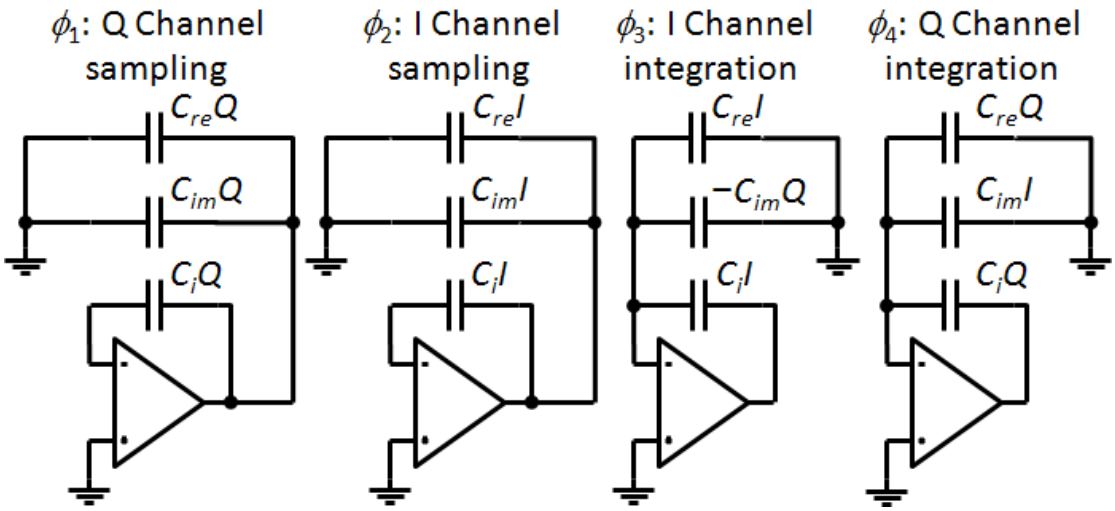


Fig. 2.24 I/Q multiplexing scheme for the conventional complex resonator.

In order to apply Chopper-A operation on the complex resonator (for $\boldsymbol{P}_1$ in Fig. 2.6 and Fig. 2.12), we need to divide one clock period into 8 phases. Operation in ϕ_5 to ϕ_8 are similar to that in the ϕ_1 to ϕ_4, but the capacitor $C_{im}I$ and $C_{im}Q$, $C_{re}I$ and $C_{re}Q$, C_iI and C_iQ interchange with each other. The swapping between $C_{im}I$ and $C_{im}Q$, $C_{re}I$ and $C_{re}Q$ are easy to implement. Eight switches are used to swap I and Q channel capacitors in different phases. However the swapping between C_iI and C_iQ is difficult. As capacitors C_iI and C_iQ are used to perform charge integration, using eight switches to swap destroys the basic transfer function of the complex resonator. To avoid this problem, a pair of auxiliary capacitors, namely, C_iTI and C_iTQ, are used as a temporary station to store the previous integration results before swapping. The detailed configuration is shown in Fig. 2.25. Compared with in ϕ_1 to ϕ_4, in ϕ_5 to ϕ_8 the capacitors C_iI and C_iQ swap with each other. In short, during ϕ_3, ϕ_4, ϕ_7 and ϕ_8, C_iTI and C_iTQ are used to store the results temporarily. During ϕ_1, ϕ_2, ϕ_5 and ϕ_6, C_iI and C_iQ swap with each other.

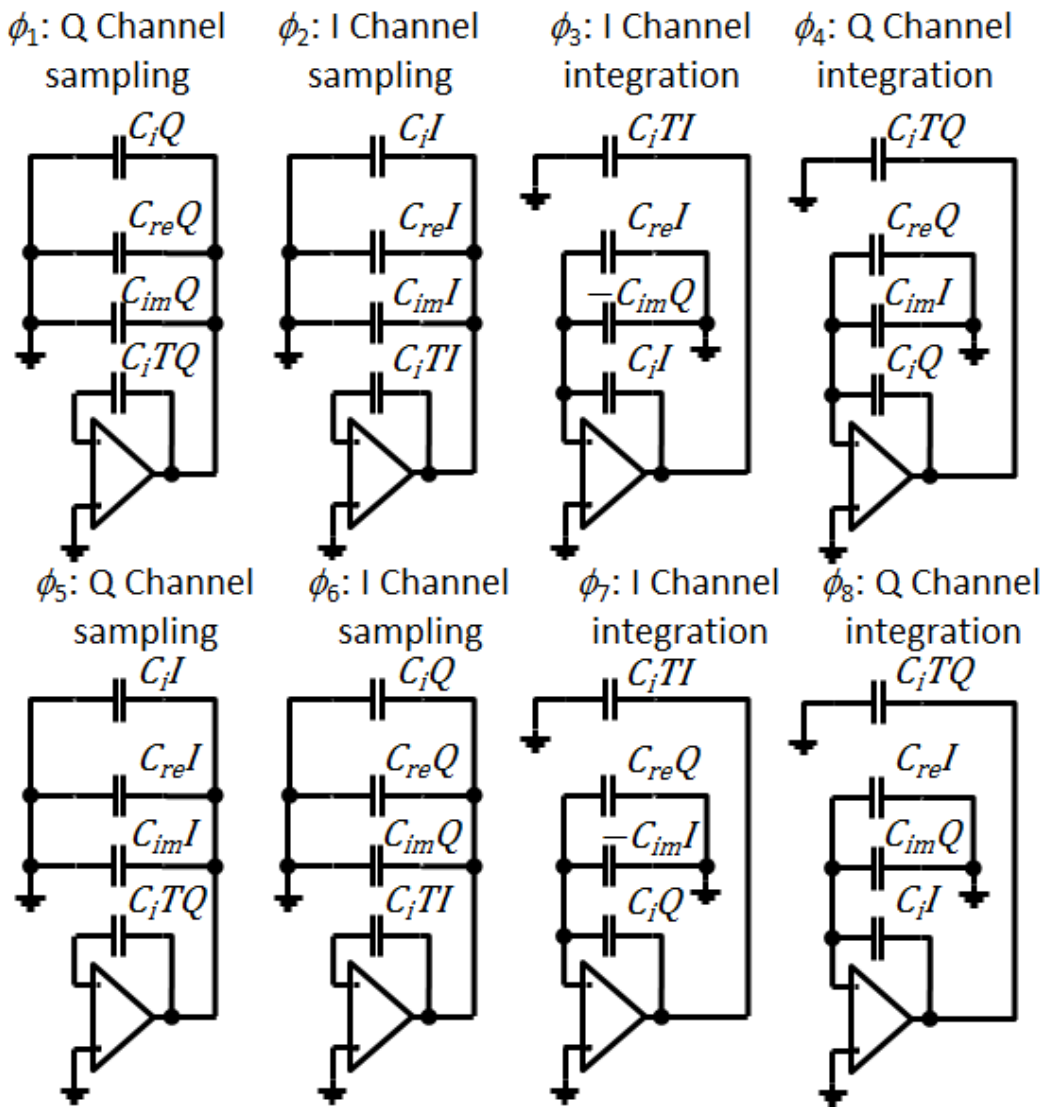


Fig. 2.25 I/Q multiplexing scheme for the complex resonator with Chopper-A.

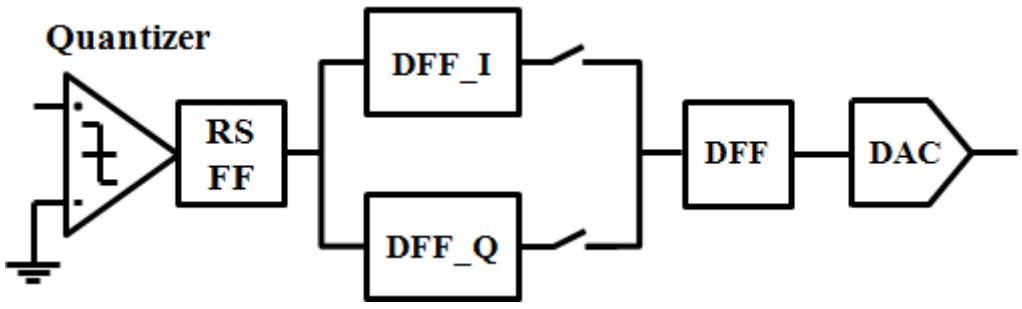


Fig. 2.26 Sharing of the quantizer and DAC between I/Q channels.

Fig. 2.26 shows a scheme to share the same quantizer and DAC between I and Q channels. Two D-type flip-flops (DFF) are employed to register the quantizer's output for I and Q channel respectively. A single feedback DAC is also multiplexed between I

and Q channels. This is feasible for two reasons. First, integration of I and Q signals in the resonator is time-interleaved. Secondly, different DFFs are used to register the I and Q quantization outputs separately. However, for the input sampling capacitors, they cannot be shared between I/Q channels for reasons discussed earlier. The Chopper-B presented above can be implemented by two groups of switches which are used to select the appropriate capacitors in different phases.

Fig. 2.27 shows a way of I/Q channel multiplexing when bilinear (shown in Fig. 2.11) is employed. An extra auxiliary op-amp is required to perform Q channel integration in ϕ_3 and ϕ_7 (I channel integration phases). The auxiliary op-amp only operates in ϕ_3 and ϕ_7 and can be turn off during other phases for power saving.

Two 2nd order high image-rejection QBDSM prototypes are designed in a 0.18μm CMOS process with a supply voltage of 1.8V. The device thresholds of the process are 0.45V and –0.5V. MIM capacitors are used. The sampling frequency is $f_s = 20MHz$. The modulator passband is centered around 5MHz ($f_s/4$) with a bandwidth of 200 *k*Hz. The coefficients of the QBDSM with Scheme I (see Fig. 2.6) are chosen as:

$$\boldsymbol{B} = 0.5, \boldsymbol{A}_1 = -1, \boldsymbol{A}_2 = 2, \boldsymbol{P}_1 = \boldsymbol{P}_2 = -1 + j, \boldsymbol{C} = -2j. \quad (2.46)$$

The coefficients of the QBDSM with Scheme II (see Fig. 2.12) are chosen as:

$$\boldsymbol{B} = 1, \boldsymbol{A}_1 = 0.5, \boldsymbol{P}_1 = \boldsymbol{P}_2 = -1 + j, \boldsymbol{C} = -2j \quad (2.47)$$

To save area, I/Q channel multiplexing is applied on the loop filter of the modulator, including the 2nd resonator. The op-amp is a single-stage folded-cascode operational transconductance amplifier (OTA) with gain-boosting and an SC common-mode feedback (CMFB), which provides fast and linear operation at low

power dissipation.

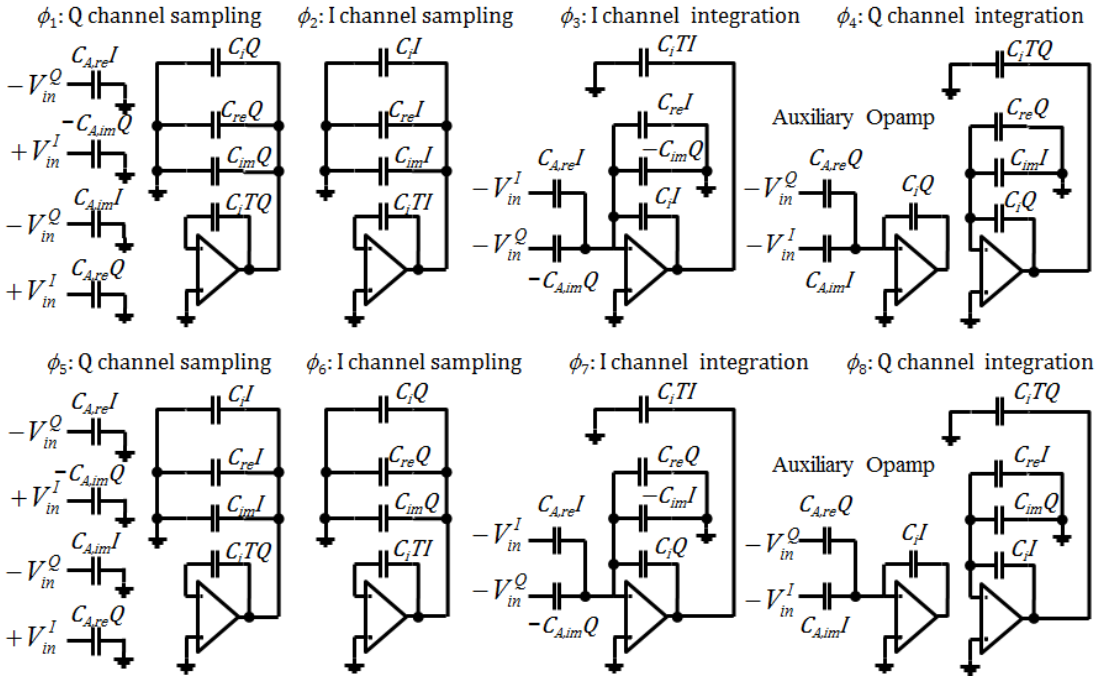
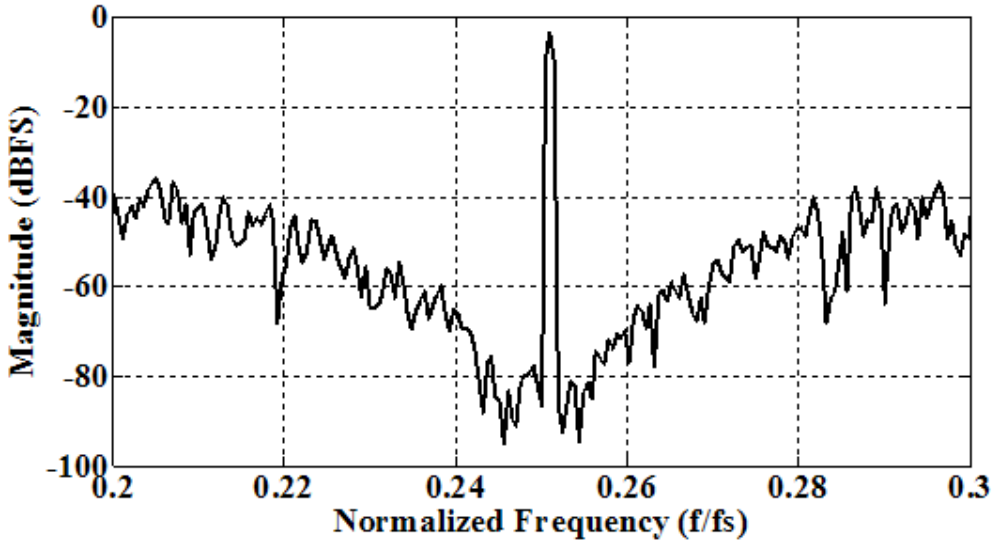
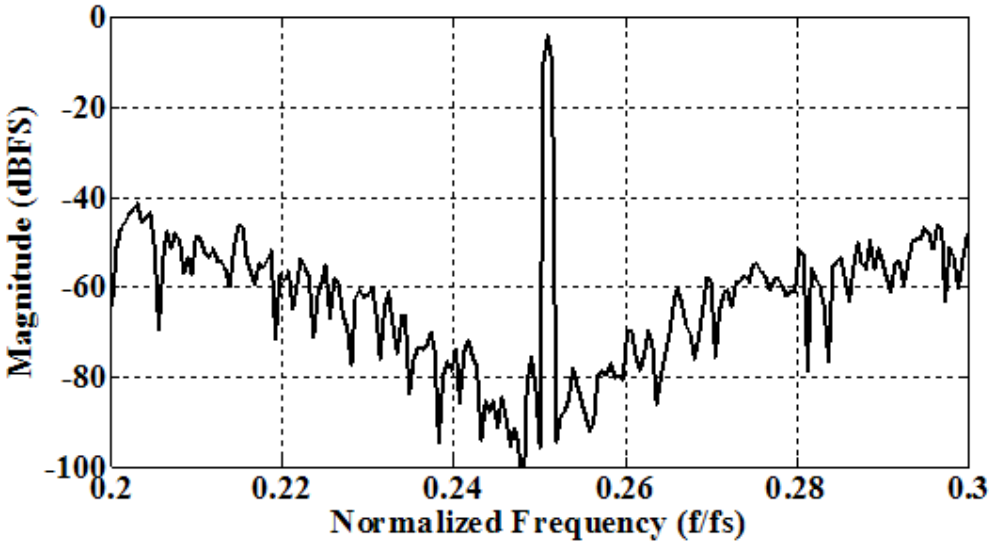


Fig. 2.27 Implementation of bilinear transformed input with I/Q multiplexing.



(a)



(b)

Fig. 2.28 FFTs on transistor-level simulated output (2k points) of (a) the QBDSM with Scheme I and (b) the QBDSM with Scheme II. All pairs of capacitors for the same coefficients are assigned with 2% mismatch in both QBDSMs.

The two QBDSMs are simulated at the transistor level. Fig. 2.28 shows the simulated output spectral density. All pairs of capacitors for the same coefficients are assigned with 2% mismatch. Referring to Eq. (2.2), $\Delta K_{re}/K_{re}$ and $\Delta K_{im}/K_{im}$ are 1%, or $\frac{|K_{re}^{I}-K_{re}^{Q}|}{K_{re}} = 2\%$ and $\frac{|K_{im}^{I}-K_{im}^{Q}|}{K_{im}} = 2\%$, $\boldsymbol{K}$ being any complex parameter. The stimulus for these two QBDSMs is the sum of two complex tones at +5.02 MHz and –5.08 MHz. From the figure, the QBDSM with Scheme I achieves an −80.2 dBW in-band noise power and an *IRR* of larger than 79 dB, and the QBDSM with Scheme II achieves an −80.8 dBW in-band noise power and an *IRR* of larger than 75 dB. The aliasing of the –5.08 MHz tone to the positive frequency of +5.08 MHz and the self-image from the +5.02 MHz to +4.98 MHz are virtually invisible for both schemes.

2.5 Measurement Results Analysis

The prototyping IC for the QBDSM with Scheme I (Fig. 2.6) was selected to fabricate in the 0.18μm CMOS. Here we do not have the flexibility in the prototyping IC to incorporate the testing of the DSM without applying the described mismatch corrections for comparison, as a typical QBDSM by SC circuits was reported in [1], which is a good candidate for the comparison. Moreover, we fabricated only Scheme I. For Scheme II, we only have transistor-level simulation results. The two schemes differ only on the techniques used to remove I/Q mismatches associated with the input coefficient $\mathbf{A_1}$. Scheme I employs Chopper-B on $\mathbf{A_1}$; Scheme II employs Bilinear transform on $\mathbf{A_1}$. Scheme I was chosen for fabrication for it is a little simpler than Scheme II. However, we think there is value to report Scheme II because it provides an alternative solution for the mismatch on $\mathbf{A_1}$.

The die micro-photograph is shown Fig. 2.29. The active chip area of the QBDSM is about 0.75 mm^2, and it draws 9.8 mA from 1.8V supply. The full-scale input amplitude is 2 $V_{pp,diff}$. The modulator outputs are captured using a logic analyzer for both I and Q channels and the data was processed offline on a personal computer. The testing setup and environment are shown in Fig. 2.30 and Fig. 2.31 respectively.

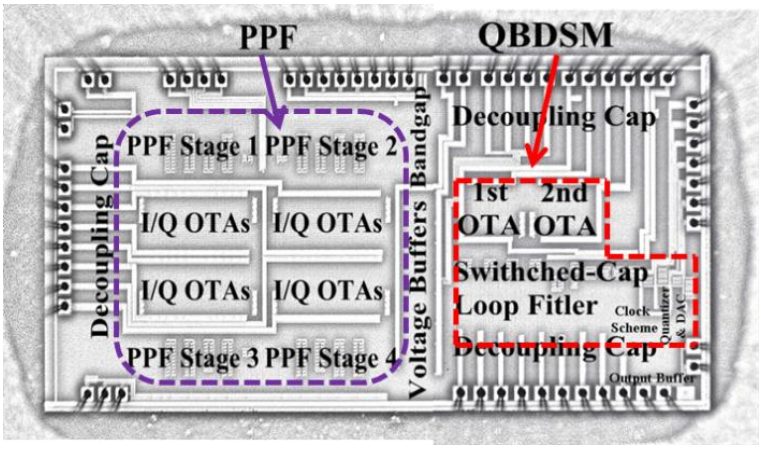


Fig. 2.29 Die micrograph of the QBDSM and poly phase filter (PPF).

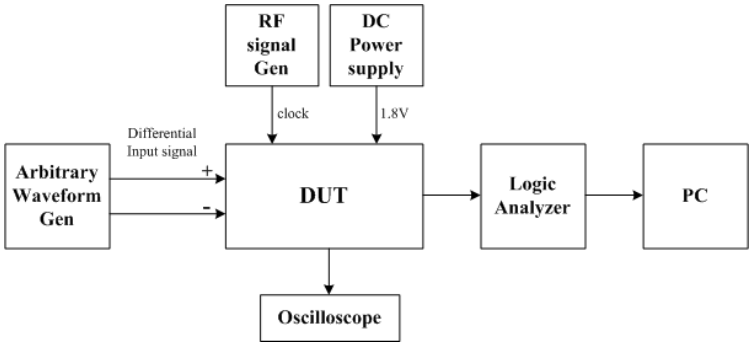


Fig. 2.30 Measurement setup

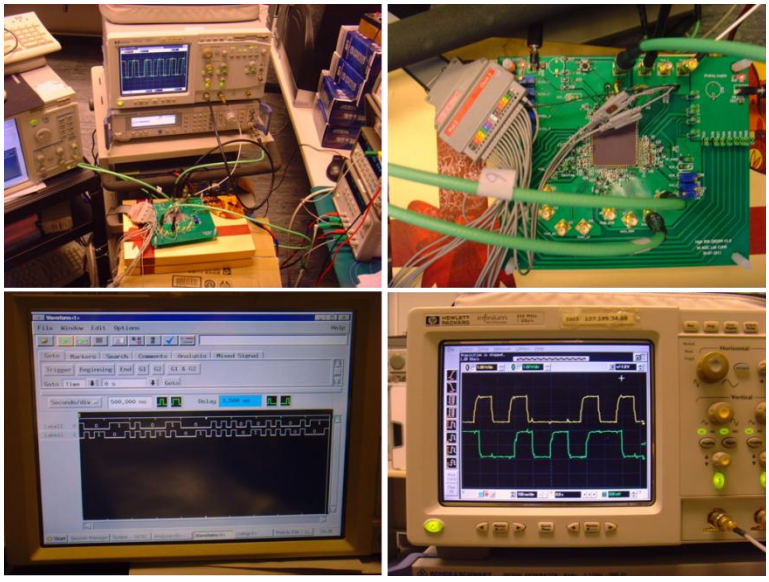
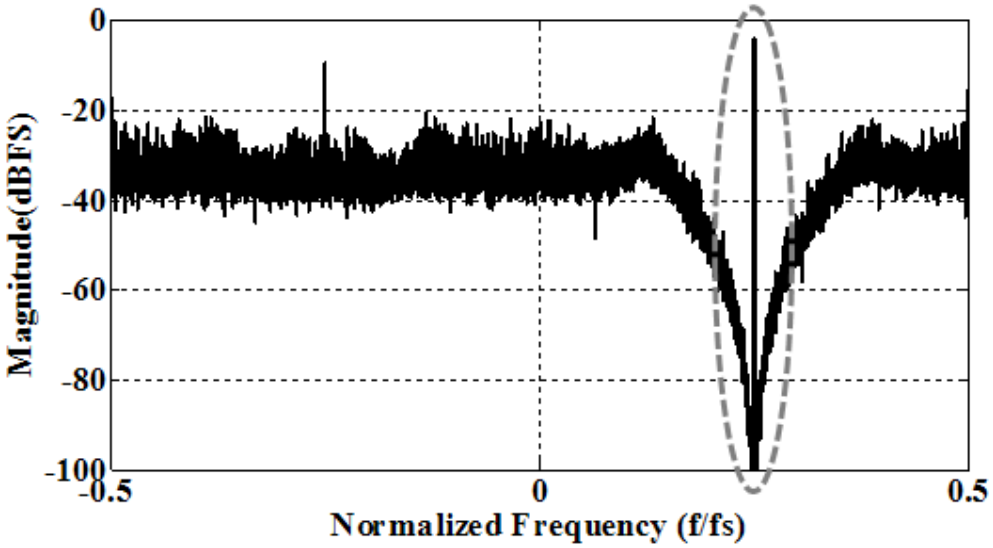


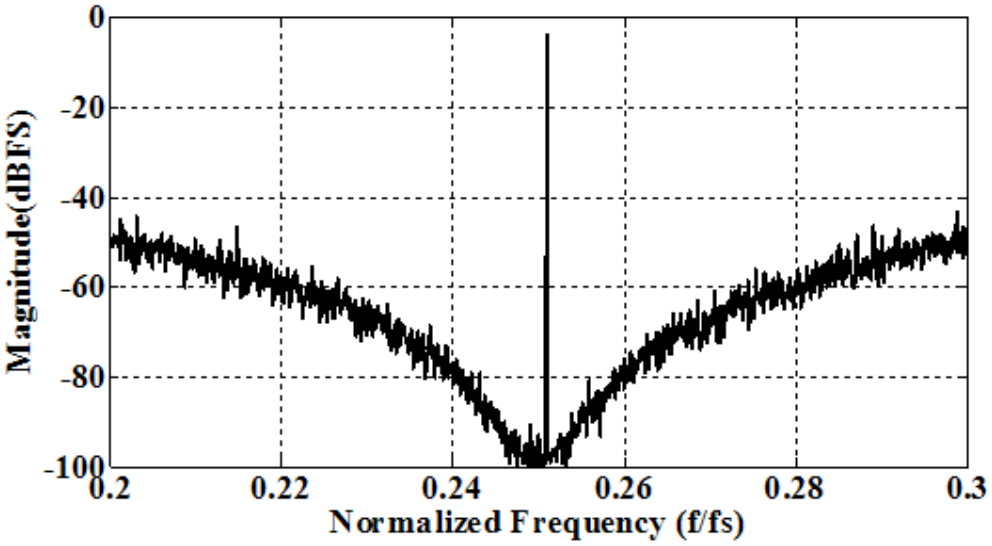
Fig. 2.31 Measurement environment.

Fig. 2.32 shows a measured output spectral density of the QBDSM for a 5.02MHz sinusoidal input to the I-channel and a zero input to the Q-channel. Fig. 2.33

shows the measured SNDR of the modulator versus I-channel's input level (Q-channel input is zero). The peak SNDR is 68.3 dB and the dynamic range is 71 dB. The important result here is that the measured the noise floor in the signal band (around $+0.25f_s$) is about 70dB lower than that in the image band (around $-0.25f_s$) (see Fig. 2.21). This proves the effectiveness of proposed techniques in eliminating the leakage of the quantization noise from the image band to the signal band due to I/Q mismatch. Table III summarizes the behavioral, transistor level simulation and measurement results for comparison.



(a)



(b)

Fig. 2.32 (a) Measured output PSD (32k points) of the QBDSM for a 5.02 MHz sinusoidal input to the I channel and a zero input to the Q channel; (b) the zoom–in view around signal band.

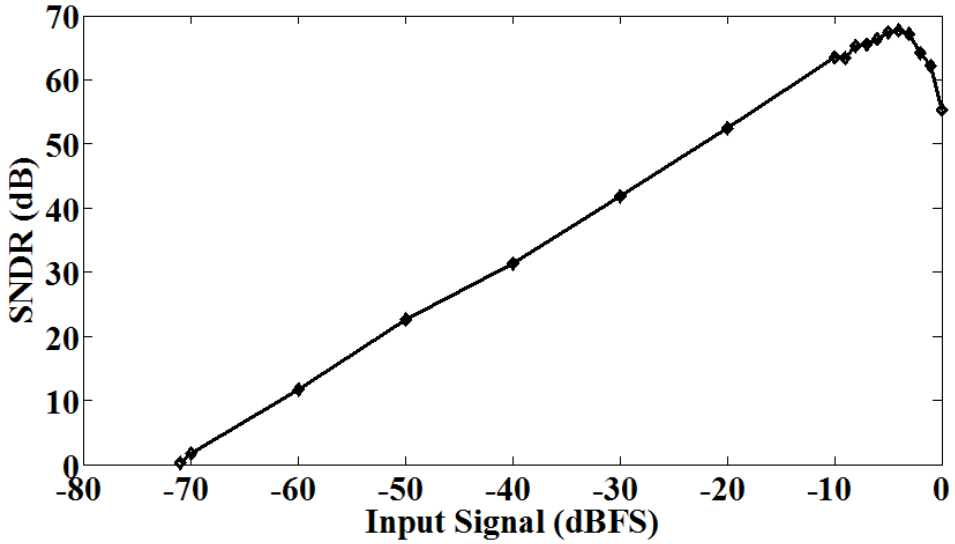
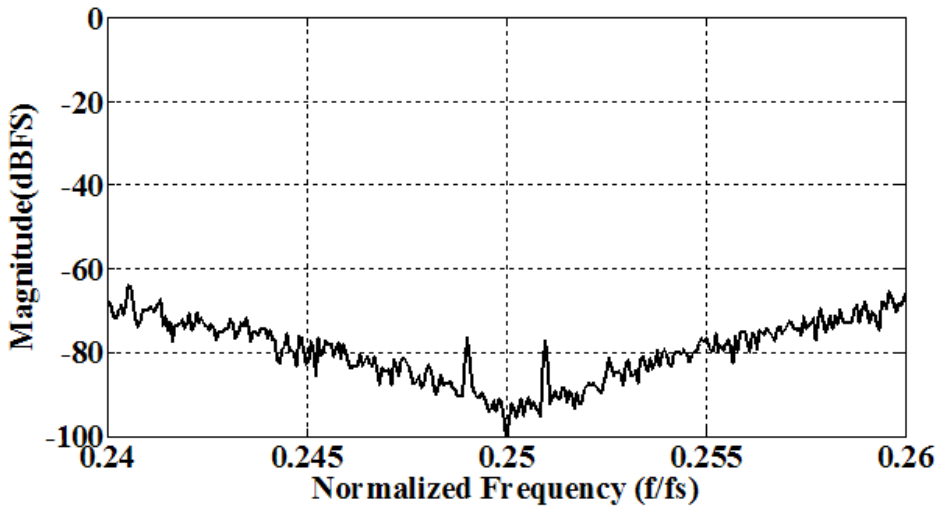


Fig. 2.33 Measured SNDR versus input level.

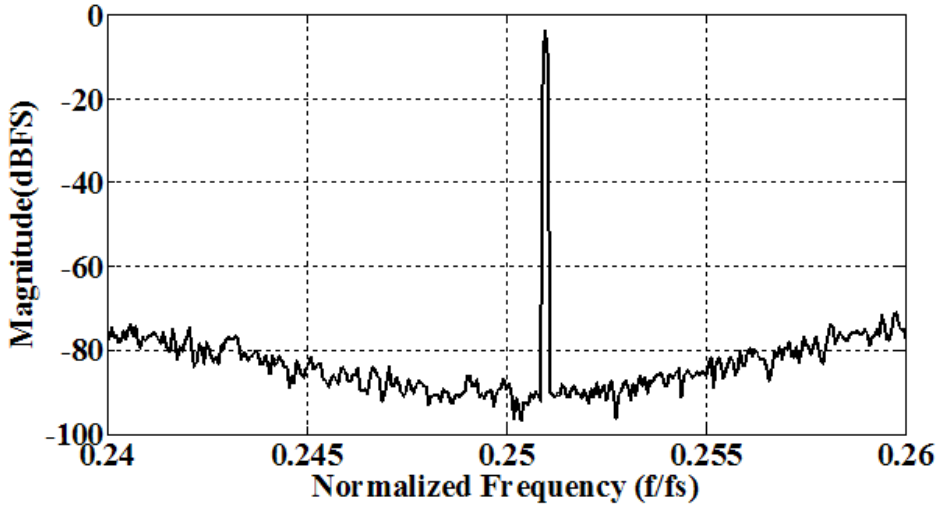
There is a practical difficulty in measuring the image rejection performance of a high image-rejection QBDSM. The problem is that the IRR measured at the output of the QBDSM cannot be better than the IRR of the complex input signal itself, no matter how good the IRR of the modulator itself is. Practically, it is hard to find a

complex signal generator with a high IRR (>50dB). Here, an IRR measurement method is developed without needing a high IRR complex signal source. It requires a high IRR PPF. By placing it before the QBDSM, the PPF can provide the QBDSM with the expected high IRR complex signal source. The measurement consists of two measurement modes (as shown in Appendix): mode A and mode B. For mode A (Fig. 2.40(a) in Appendix II), the passband of PPF is configured at $-f_s/4$, and the noise shaping of QBDSM is configured at $f_s/4$; For mode B (Fig. 40(b) in Appendix II), the passband of PPF is reconfigured from $-f_s/4$ to $f_s/4$. The high IRR PPF with Chopper-B operator has been implemented and fabricated in the same chip. Its passband has a bandwidth of 600 kHz and can be configured at $f_s/4$ or $-f_s/4$ (5 MHz or –5 MHz). The I/Q channel output signals of PPF are buffered for the I/Q channel inputs of QBDSM. The die micrograph is shown in the left of Fig. 2.29.

A 5.02 MHz sinusoidal input and a zero input are injected to the I channel and Q channel of the PPF respectively. For mode *A* configuration, the measured spectral density at the modulator's output is shown in Fig. 2.34 (a). The magnitude of the tone



(a)



(b)

Fig. 2.34 Measured output PSD (32k points) of the modulator for IRR estimation: (a) Mode A; (b) Mode B.

located at 5.02 MHz (0.251 on the normalized frequency scale), which is the aliased image signal, is −77.1 dB. The magnitude of the tone located at 4.98 MHz (0.249 on the normalized frequency scale), which is the self-image signal, is -76.2 dB; For mode *B* configuration, the measured spectral density at the modulator's output is shown in Fig. 2.34(b). The magnitude of the tone located at 5.02 MHz (0.251 on the normalized frequency scale) is −3.8 dB. Therefore, it can be concluded that the *IRR* of the QBDSM is at least 73 dB, and the self-image rejection ratio is greater than 72 dB. Seven packaged chips were measured and they all perform closely. The average and standard deviation of the image rejection ratio are 72.8 dB and 0.8 dB respectively, and those values for the self-image rejection ratio are 71.6 dB and 0.7 dB.

Table III summarizes the measured performance the modulator. Table IV compares the measuring *IRR* of the proposed modulator with that of some recently published quadrature bandpass modulators, implemented by either continuous-time or

discrete-time circuits. The *IRR* of this work is superior to the others. In the comparison table IV, there are indeed some wider bandwidth designs. Although the image rejection problem is more challenging in a wider bandwidth modulator, the proposed I/Q mismatch cancellation schemes on every coefficient are independent to the bandwidth and must be effective in wider bandwidth applications.

Table III Measured performance of the proposed QBDSM with Scheme I.

Process	0.18 μm CMOS
Modulator Type	2^{nd} order single-bit QBDSM
Sampling Frequency	20 MHz
Pass-band center frequency	5 MHz
Bandwidth	200 kHz
Over sampling ratio	100
Input Signal Range	2 $V_{pp,diff}$
Peak SNDR	68.3 dB
Dynamic Range	71 dB
Image rejection ratio	>73 dB
Supply Voltage	1.8 V
Current consumption	9.8 mA
Active Area	0.75 mm^2

Table IV IRR performance comparison of recently reported QBDSMs.

	This Work	[1]	[19]	[20]	[17]	[16]	[15]	[18]
Modulator Type	**DT QBP**	**DT QBP**	**CT QBP**	**CT QBP**	**CT QBP**	**CT QBP**	**CT QBP**	**CT QBP**
Bandwidth (MHz)	**0.2**	**0.2**	**0.27**	**1**	**2**	**8.5**	**20**	**20**
IRR (dB)	**>73**	**>45**	**>65**	**>46.3**	**>37**	**>50**	**>47.2**	**>55**

2.6 Conclusions

In this chapter, the effects of I/Q mismatches in SC QBDSMs that have their passband centered at $f_s/4$ have been analyzed. Chopper and circuit sharing techniques to overcome the I/Q mismatches in the input, global feedback and resonator local feedback coefficients have been proposed together with an architectural selection criterion.

Measurement results on a 0.18μm CMOS prototype QBDSM show that these techniques enable the modulator to achieve: (i) an excellent IRR ratio of at least 73 dB; (ii) a self-image rejection ratio of 72dB; and (iii) virtual elimination of the leakage of quantization noise from the image band to the signal band. Last, the circuit sharing technique also helps to reduce chip area.

APPENDIX I: I/Q Mismatches in Low-IF Receivers

This appendix gives a qualitative analysis of the I/Q mismatch issue in each of the following blocks in the low-IF receiver: a quadrature mixer, a polyphase filter (PPF) and a QBDSM (see Fig. 2.35).

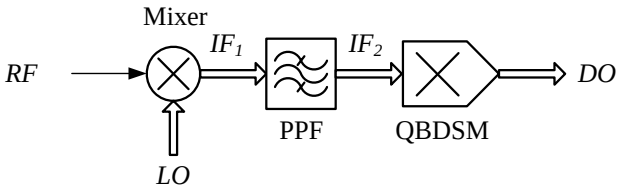


Fig. 2.35 Analysis model for low-IF receiver.

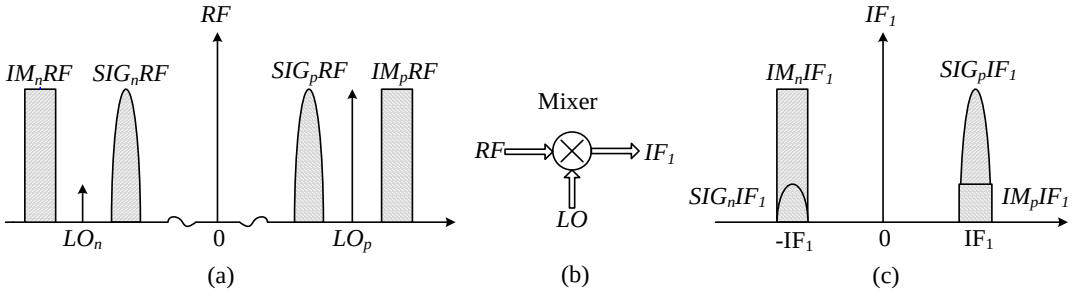


Fig. 2.36 Signal spectrum of mixer: (a) Input signal "RF" and "LO" (b) Signal flow of the mixer (c) Output signal "IF_1".

A. I/Q Mismatch in Mixer

The input "RF" to the quadrature mixer is a real signal. The input "LO" is a complex signal, typically generated from a quadrature local oscillator. Ideally, the "LO" is a pure tone "LO_p" located at a positive frequency (or "LO_n" a negative frequency). Due to gain and phase mismatches between the I and Q paths in the mixer, "LO_p" will leak to the negative frequency "LO_n". We define the signal-to-image ratio of the "LO" ISR_{LO} as:

$$ISR_{LO} = |LO_p|/|LO_n| \tag{2.48}$$

where $|\cdot|$ denotes the magnitude of the argument. Without loss of generality, all the I/Q mismatches associated with the quadrature mixer can be represented by the I/Q mismatches in the "LO".

As shown in Fig. 2.36 (a)-(c), four sub-sidebands of the "RF", namely, "SIG_pRF", "SIG_nRF", "IM_pRF" and "IM_nRF", will be down-converted to the IF. The four IF components at the output of the mixer, "SIG_pIF_1", "SIG_nIF_1", "IM_pIF_1" and "IM_nIF_1", are:

$$\begin{gathered} SIG_pIF_1 = SIG_nRF \cdot LO_p, \\ SIG_nIF_1 = SIG_pRF \cdot LO_n, \\ IM_pIF_1 = IM_pRF \cdot LO_n, \\ IM_nIF_1 = IM_nRF \cdot LO_p \end{gathered} \tag{2.49}$$

B. I/Q Mismatch in Polyphase Filter

Polyphase filters are a kind of complex filters that block signals around a positive or a negative frequency. The output IF_2 of the PPF in Fig. 2.35 can be expressed as:

$$IF_2(s) = STF_{PPF}(s) \cdot IF_1(s) + ITF_{PPF}(s) \cdot IF_1^*(s) \tag{2.50}$$

where STF_{PPF} is the signal transfer functions of the PPF, and ITF_{PPF} is the image transfer function of the PPF due to mismatch, and IF_1 is the input. Fig. 2.37 (b) illustrates the frequency response of the PPF. To simplify the analysis, it is assumed the magnitude of ITF_{PPF} in the signal passband and the image-band are equal. IRR_{PPF} has been used to define the ratio of magnitude of STF_{PPF} in passband to that of ITF_{PPF}, and IMA_{PPF} is the image attenuation at the stop band of the PPF.

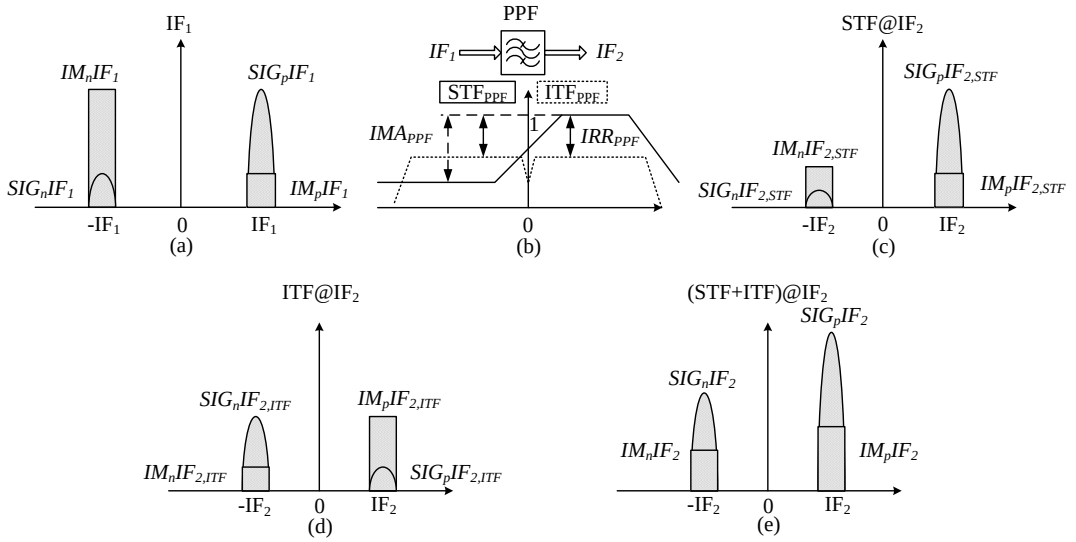


Fig. 2.37 Signal spectrum of PPF: (a) Input signal "IF_1"; (b) STF_{PPF} and ITF_{PPF}; (c) Output signal component of "IF_2" for STF_{PPF}; (d) Output signal component of "IF_2" for ITF_{PPF}; (e) Output signal "IF_2": $((c)+(d))$.

To get the output of PPF (IF_2), the multiplication of "IF_1" by STF_{PPF} and ITF_{PPF} should be calculated, and then combined. "$SIG_pIF_{2,STF}$", "$SIG_nIF_{2,STF}$", "$IM_pIF_{2,STF}$" and "$IM_nIF_{2,STF}$" are four sub-sideband outputs for STF_{PPF}; "$SIG_pIF_{2,ITF}$", "$SIG_nIF_{2,ITF}$", "$IM_pIF_{2,ITF}$" and "$IM_nIF_{2,ITF}$" are four sub-sideband outputs for ITF_{PPF}. Assuming the magnitude of STF_{PPF} in passband is unity, and then it has:

$$\begin{aligned} SIG_pIF_2 &= SIG_pIF_{2,STF} + SIG_pIF_{2,ITF} = SIG_pIF_1 + SIG_nIF_1/IRR_{PPF} \\ SIG_nIF_2 &= SIG_nIF_{2,STF} + SIG_nIF_{2,ITF} = SIG_nIF_1/IMA_{PPF} + SIG_pIF_1/IRR_{PPF} \\ IM_pIF_2 &= IM_pIF_{2,STF} + IM_pIF_{2,ITF} = IM_pIF_1 + IM_nIF_1/IRR_{PPF} \\ IM_nIF_2 &= IM_nIF_{2,STF} + IM_nIF_{2,ITF} = IM_nIF_1/IMA_{PPF} + IM_pIF_1/IRR_{PPF} \end{aligned} \quad (2.51)$$

The output signal of PPF, "IF_2", also has four sub-sidebands, called "SIG_pIF_2", "SIG_nIF_2", "IM_pIF_2" and "IM_nIF_2", as shown in Fig. 2.37.

C. I/Q Mismatch in QBDSM

The QBDSM has a signal transfer function and noise transfer function, denoted

as STF_{DSM} and NTF_{DSM} respectively. Due to I/Q mismatch, each of them has an image counterpart, called image transfer function (ITF_{DSM}) and image noise transfer function ($INTF_{DSM}$) respectively. To simplify the analysis, it is assumed the magnitude of STF_{DSM} and ITF_{DSM} in the signal passband and the image-band are equal, as shown in Fig. 2.38. Ignoring the quantization noise input, the output "*DO*" of the QBDSM has four components "SIG_pDO", "SIG_nDO", "IM_pDO" and "IM_nDO" given below:

$$\begin{aligned} SIG_pDO &= SIG_pDO_{STF} + SIG_pDO_{ITF} = SIG_pIF_2 + SIG_nIF_2/IRR_{DSM} \\ SIG_nDO &= SIG_nDO_{STF} + SIG_nDO_{ITF} = SIG_nIF_2 + SIG_pIF_2/IRR_{DSM} \\ IM_pDO &= IM_pDO_{STF} + IM_pDO_{ITF} = IM_pIF_2 + IM_nIF_2/IRR_{DSM} \\ IM_nDO &= IM_nDO_{STF} + IM_nDO_{ITF} = IM_nIF_2 + IM_pIF_2/IRR_{DSM} \end{aligned} \tag{2.52}$$

where "SIG_pDO_{STF}", "SIG_nDO_{STF}", "IM_pDO_{STF}" and "IM_nDO_{STF}" are four sub-sidebands for STF_{DSM}; "SIG_pDO_{ITF}", "SIG_nDO_{ITF}", "IM_pDO_{ITF}" and "IM_nDO_{ITF}" are four sub-sidebands for ITF_{DSM}, and IRR_{DSM} is the ratio of the magnitude of STF_{DSM} in passband to that of ITF_{DSM}.

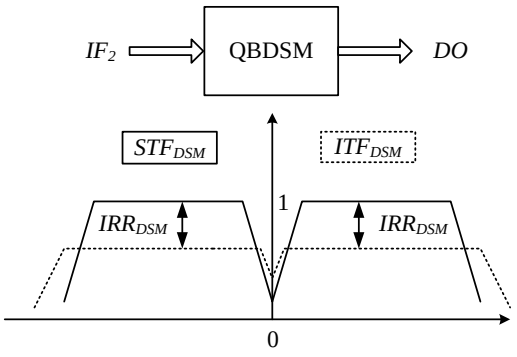


Fig. 2.38 STF_{DSM} and ITF_{DSM} of QBDSM.

D. I/Q Imbalance Analysis for whole receiver

Based on the above analysis, the IRR of the whole low-IF receiver can be found as:

$$IRR_{low-IF} = \frac{\frac{SIG_pDO}{IM_pDO}}{\frac{SIG_pRF}{IM_pRF}} \approx \frac{SIG_pIF_1+SIG_nIF_1/IRR_{PPF}}{IM_pIF_1+IM_nIF_1/IRR_{PPF}} \cdot \frac{IM_pRF}{SIG_pRF} = \frac{1}{\frac{1}{ISR_{LO}}+\frac{1}{IRR_{PPF}}} \quad (2.53)$$

$$\Longrightarrow \quad (ISR_{LO} \parallel IRR_{PPF})$$

The above equation shows that the IRR of the low-IF receiver depends on two important factors: the signal to image ratio of the quadrature LO signal (ISR_{LO}) and the image rejection ratio of PPF (IRR_{PPF}). The image rejection ratio of QBDSM (IRR_{DSM}) is shielded by IMA_{PPF} and IRR_{PPF}.

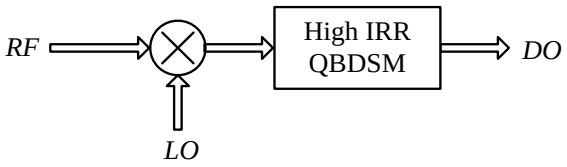


Fig. 2.39 Low-IF receiver with high IRR QBDSM.

However if a high IRR QBDSM can be achieved, the PPF between the mixer and the QBDSM can be removed (Fig. 2.39). In this case, the overall IRR becomes:

$$IRR_{Low-IF} = \frac{\frac{SIG_pDO}{IM_pDO}}{\frac{SIG_pRF}{IM_pRF}} = \frac{SIG_pIF_1+SIG_nIF_1/IRR_{DSM}}{IM_pIF_1+IM_nIF_1/IRR_{DSM}} \cdot \frac{IM_pRF}{SIG_pRF} = \frac{1}{\frac{1}{ISR_{LO}}+\frac{1}{IRR_{DSM}}} \quad (2.54)$$

$$\Rightarrow (ISR_{LO} \parallel IRR_{DSM})$$

As a result, the IRR of whole Low-IF receiver is determined by the ISR_{LO} and IRR_{DSM}. Compared with conventional case in Fig. 2.1, the high IRR PPF can be removed, less power consumption and silicon area cost can be anticipated.

APPENDIX II: IRR Measurement Method

Here, an IRR measurement method is developed without needing a high *IRR*

complex signal source. It requires a high *IRR* PPF. By placing it before the QBDSM, the PPF can provide the QBDSM with the expected high *IRR* complex signal source.

The measurement consists of two measurement modes: mode *A* and mode *B.* The input is a real sinusoidal signal.

For mode *A* (Fig. 2.40(a)), the passband of PPF is configured at $-f_s/4$, and the noise shaping of QBDSM is configured at $f_s/4$. Assuming the magnitude of STF of the PPF in the signal passband ($-f_s/4$) is unity, then the positive frequency tone of the output of PPF ($SIG_{p,FO,A}$) is:

$$SIG_{p,FO,A} = \frac{SIG_{p,IN,A}}{IMA_{PPF}} + \frac{SIG_{n,IN,A}}{IRR_{PPF}} = SIG_{p,IN,A}\left(\frac{1}{IMA_{PPF}} + \frac{1}{IRR_{PPF}}\right) \qquad (2.55)$$

where $SIG_{p,IN,A}$ and $SIG_{n,IN,A}$ are the input magnitude at the positive and negative frequencies respectively, IRR_{PPF} is the *IRR* of the PPF, and IMA_{PPF} is the image attenuation at the stop band of the PPF, as indicated in Fig. 2.40(a). In the above equation, $SIG_{p,IN,A} = SIG_{n,IN,A}$ is used as the input is a real signal.

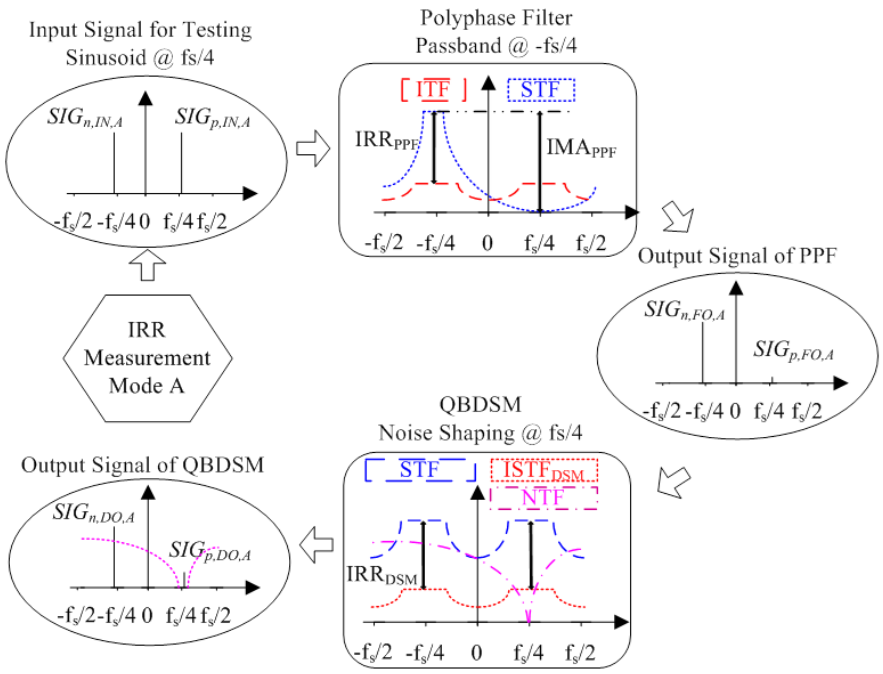
The magnitude of the negative frequency tone at the output of PPF ($SIG_{n,FO,A}$) is:

$$SIG_{n,FO,A} = SIG_{n,IN,A} + \frac{SIG_{p,IN,A}}{IRR_{PPF}} = SIG_{p,IN,A}\left(1 + \frac{1}{IRR_{PPF}}\right) \qquad (2.56)$$

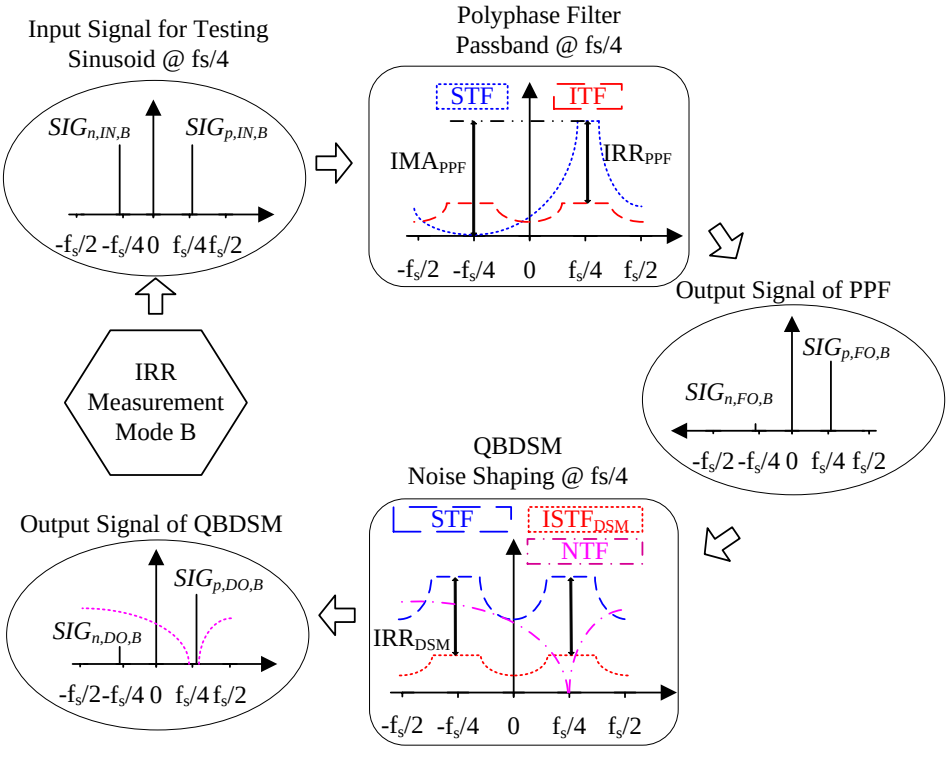
Assuming the magnitude of the STF of the QBDSM in the signal passband ($f_s/4$) is unity, the magnitude of the positive frequency tone at the output of QBDSM ($SIG_{p,DO,A}$) is:

$$\begin{aligned} SIG_{p,DO,A} &= SIG_{p,FO,A} + \frac{SIG_{n,FO,A}}{IRR_{DSM}} \\ &= SIG_{p,IN,A}\left(\frac{1}{IMA_{PPF}} + \frac{1}{IRR_{DSM}} + \frac{1}{IRR_{PPF}}\right. \\ &\quad \left. + \frac{1}{IRR_{DSM} \cdot IRR_{PPF}}\right) \end{aligned} \qquad (2.57)$$

where IRR_{DSM} is the *IRR* of the QBDSM.



(a)



(b)

Fig. 2.40 IRR measurement method: (a) Mode A; (b) Mode B.

For mode *B* (Fig. 2.40(b)), the passband of PPF is reconfigured from $-f_s/4$ to

$f_s/4$. This is done by inverting the sign of a coefficient of the PPF, which is convenient to implement in the differential PPF. By this change, the STF and ITF of PPF is just the original ones mirrored along DC. Meanwhile, the notch of the *NTF* of the QBDSM is still located at $f_s/4$, the same as in mode *A*. Then, the magnitude of the positive frequency tone at the output of PPF becomes:

$$SIG_{p,FO,B} = SIG_{p,IN,B} + \frac{SIG_{n,IN,B}}{IRR_{PPF}} = SIG_{p,IN,B}\left(1 + \frac{1}{IRR_{PPF}}\right) \tag{2.58}$$

The same input signal is applied as in mode *A*, so $SIG_{p,IN,B} = SIG_{n,IN,B} = SIG_{p,IN,A} = SIG_{n,IN,A}$. The magnitude of the negative frequency tone at the output of PPF is:

$$SIG_{n,FO,B} = \frac{SIG_{n,IN,B}}{IMA_{PPF}} + \frac{SIG_{p,IN,B}}{IRR_{PPF}} = SIG_{p,IN,B}\left(\frac{1}{IMA_{PPF}} + \frac{1}{IRR_{PPF}}\right) \tag{2.59}$$

So the magnitude of the positive frequency tone at the output of the QBDSM is:

$$\begin{aligned} SIG_{p,DO,B} &= SIG_{p,FO,B} + \frac{SIG_{n,FO,B}}{IRR_{DSM}} \\ &= SIG_{p,IN,B}\left(1 + \frac{1}{IRR_{PPF}} + \frac{1}{IRR_{DSM} \cdot IRR_{PPF}}\right. \\ &\quad \left. + \frac{1}{IRR_{DSM} \cdot IMA_{PPF}}\right) \end{aligned} \tag{2.60}$$

The ratio of the magnitude of the positive frequency tone at the output of the QBDSM in mode *B* to that in mode *A* is then calculated:

$$\frac{SIG_{p,DO,B}}{SIG_{p,DO,A}} \approx \frac{1}{\frac{1}{IMA_{PPF}} + \frac{1}{IRR_{DSM}} + \frac{1}{IRR_{PPF}}} = IMA_{PPF} \| IRR_{PPF} \| IRR_{DSM} \tag{2.61}$$

This equation shows that if the measured $SIG_{p,DO,B}/SIG_{p,DO,A}$ is greater than a certain value, say 70dB, then each and every of the IRR_{DSM}, IRR_{PPF}, and IMA_{PPF} must be larger than 70dB.

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CHAPTER 3. A Continuous-time Cascaded Delta-Sigma Modulator with PWM-Based Automatic RC Time Constant Tuning and Correlated Double Sampling

Continuous-time (CT) Delta-Sigma modulators (DSM) have recently drawn large attention for high-speed, low-power or low-voltage analog-to-digital (A/D) conversion in deep sub-micrometer CMOS technologies [1]-[5]. Most of the reported CT modulators employ a single-loop topology rather than a cascaded structure. However, there are increasing research interest on CT cascaded modulators to tap on their benefits of modularity and stability [6]-[8].

Fig. 3.1 depicts a generic architecture of a CT cascaded two-stage DSM [9]. The first stage's quantization noise E_1 is cancelled by selecting proper digital filters $H_1(z)$ and $H_2(z)$ such that:

$$H_1(z) \cdot NTF_1(z) - H_2(z) \cdot STF_2(z) = 0 \tag{3.1}$$

where $NTF_1(z)$ and $STF_2(z)$are the impulse-invariant *z*-domain equivalents of the noise transfer function (NTF) in the first stage and that of the signal transfer function (STF) in the second stage, respectively. Normally, $H_1(z) = STF_2(z)$ and $H_2(z) = NTF_1(z)$ are selected. Accurate matching between the analog NTF_1 and the digital H_2 are thus required. However, the *RC* time constant variation (in case of active-*RC* circuit implementation, or equivalently the g_m/C variation in g_m-C implementations) and finite opamp dc gain affect the accuracy of NTF_1, leading to imperfect

cancellation of the first stage's quantization noise [9]-[11].

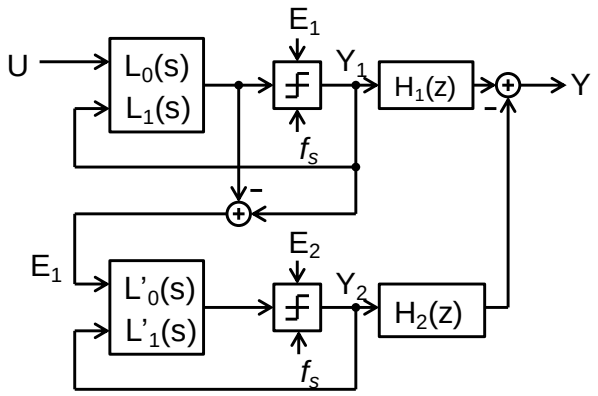


Fig. 3.1 A generic cascaded 2-stage DSM architecture.

For the *RC* time constant variation problem alone, prior works have been reported for CT filters and CT DSMs. The schemes in [12]-[19] involve adjusting the capacitance or resistance within a set of discrete values by digital trimming. Their tuning accuracy is limited by the available resolution of the trimming element array, and high precision tuning may lead to excessive die area. The linearized behavior of a MOS transistor operating in triode region can also be employed for resistance tuning [20][21], but the decrease in supply voltage may cause a decrease in the linearity of the MOS resistor and available tuning range severely. The digital quantization noise leakage calibration scheme in [22]-[24] requires design overhead like injection of special input tones, digital signal processing, etc.

Another type of *RC* time constant tuning methods is the pulse-width-modulation (PWM) technique. In this method, the tuning is implemented in the time domain. Several circuits applying this variable duty cycle approach have been presented [25]-[37]. In [35], such a technique is applied in a single-loop hybrid CT and discrete-time (DT) modulator.

In this work, we propose to apply the PWM technique, together with a simple automatic duty cycle generation circuit, in a CT cascaded modulator. We further observe that the PWM technique enables us to use the correlated double sampling (CDS) technique, which is conventionally confined to discrete-time circuits, to boost the effective dc gain of the opamp. Furthermore, an opamp bandwidth compensation technique is proposed so that low gain-bandwidth product (GBW) opamps can be used for power saving. To improve the anti-aliasing capability of the CT modulator, a simple anti-aliasing filter scheme is presented. To verify the efficacy of the proposed techniques, a prototype CT 2-2 cascaded modulator is designed in a 0.18-μm CMOS.

The rest of this chapter is organized as follows. Section 3.1 gives a detailed description and analysis on the PWM technique for on-chip automatic tuning of *RC* time constants. Section 3.2 presents the CDS-based opamp dc gain enhancement scheme. In Section 3.3, the finite opamp GBW compensation scheme is introduced. The jitter noise characteristics are discussed in Section 3.4. The design of the prototype chip and the measurement results are presented in Section 3.5 and Section 3.6 respectively, followed by conclusions in Section 3.7.

3.1 PWM for on-chip *RC* Time Constant Tuning

The use of PWM to tune the *RC* time constant in CT filters has been reported in [28]-[34], where the resulting filters are called switched-R-MOSFET-C (SRMC) filters. Fig. 3.2 shows an SRMC integrator. It can be regarded as an integrator with a track-and-hold function. By adjusting the ratio of track to hold time using a variable

duty-cycle clock, the effective input resistance and thereby the *RC* time constant of the integrator can be varied.

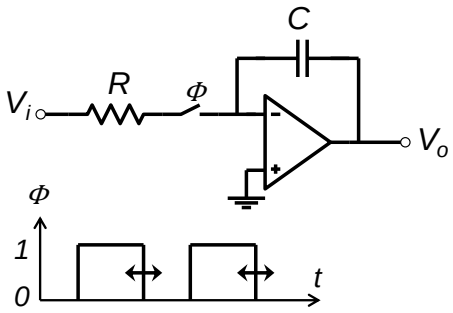


Fig. 3.2 Switched-R-MOSFET-C integrator with PWM tuning.

The circuit in Fig. 3.2 can be described by the following time domain equation:

$$C\frac{dv_0(t)}{dt} = \frac{v_i(t)}{R}\phi(t) \tag{3.2}$$

where the clock signal $\phi(t)$ is a square wave, having a value of either 0 ("low") or 1 ("high") such that the switch passes either no current or full current. By Fourier transformation, Eq. (3.2) becomes:

$$RCj\omega V_0(\omega) = V_i(\omega) * \Phi(\omega) \tag{3.3}$$

where "*" denotes convolution, ω is the angular frequency, and $V_0(\omega)$ and $\Phi(\omega)$ are the Fourier transforms of $v_0(t)$and $\phi(\mathrm{t})$ respectively. The Fourier transform $\Phi(\omega)$ of the periodic signal $\phi(t)$ can be represented as a weighted sum of time-shifted impulses:

$$\Phi(\omega) = \sum_{n=-\infty}^{\infty} c_n \delta(\omega - n\omega_{clk}) \tag{3.4}$$

where ω_{clk} is the angular frequency of the clock signal and $\delta(\omega)$ is the Dirac delta function. The coefficients c_n in Eq. (3.4) are the Fourier series coefficients of $\phi(t)$, given by:

$$c_n = d \cdot \mathrm{sinc}(nd) \tag{3.5}$$

where d $(0 \le d \le 1)$ is the duty-cycle of $\phi(t)$, and $\mathrm{sinc}(x) = \sin(\pi x)/\pi x$. Note that $c_0 = d$. From Eq. (3.3) and Eq. (3.4), we have:

$$V_0(\omega) = \frac{1}{j\omega CR/c_0} \sum_{n=-\infty}^{\infty} \frac{c_n}{c_o} V_i(\omega - n\omega_{clk}) \tag{3.6}$$

The equivalent RC time constant of the integrator becomes RC/c_0, or RC/d. In Eq. (3.6) it is shown that the input signal is frequency-shifted, scaled and super-positioned before being integrated.

A signal flow diagram of the SRMC integrator described by Eq. (3.6) is given in Fig. 3.3. The SRMC is modeled as a mixer followed by an integrator. The integrator has a duty-cycle-tuned time constant of RC/d; the effective mixing clock is amplitude-scaled by the duty-cycle d.

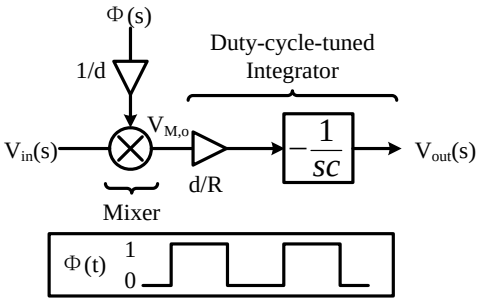


Fig. 3.3 A model of the SRMC integrator.

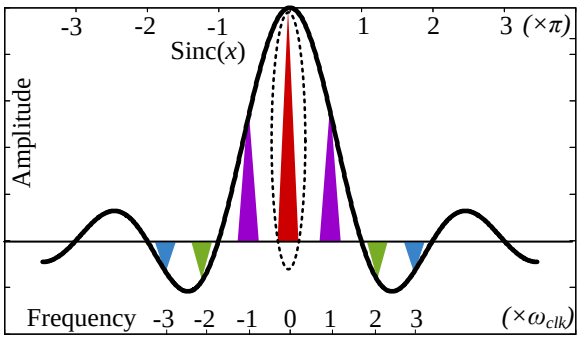


Fig. 3.4 Spectrum of the signal $V_{M,o}$ in Fig. 3.3.

The spectrum of signal $V_{M,o}$ at the mixer's output in Fig. 3.3 is shown in Fig. 3.4. When the signal band located at dc is considered alone, then,

$$V_0(\omega)|_{@DC} = \frac{V_i(\omega)}{j\omega CR/d}. \tag{3.7}$$

That means if the input signal has not been aliased, i.e. the switching frequency is larger than the Nyquist frequency, the transfer function of SRMC integrator becomes that of a conventional CT integrator with a varied resistance value, which is the basis of the *RC* time constant tuning by PWM.

3.1.1 Integrator Gain Error

In switched-capacitor (SC) DSMs, the integrator gains are determined by capacitor ratios, whose inaccuracy can be as low as 0.1%. In contrast, variations of the integrator gains are a well-known non-ideal characteristic of CT DSMs. In a CT DSM, the integrator gains are mapped into resistor-capacitor products, which vary largely over process and temperature. Process variations of 10% and 20% are common for the absolute values of capacitors and resistors respectively, leading to a *RC* product variation of more than 30%. To model the *RC* product variation, the transfer function of the conventional active *RC* integrator can be expressed as

$$ITF_{conv} = \frac{1}{RC}\frac{1}{s} = \frac{1}{R_{nom}C_{nom}(1+\Delta\delta_{RC})}\frac{1}{s} = GE_{RC}\frac{1}{R_{nom}C_{nom}}\frac{1}{s} \tag{3.8}$$

where R_{nom} and C_{nom} are the nominal values of resistor and capacitor respectively, $\Delta\delta_{RC}$ is the percentage variation of *RC* product, and GE_{RC} is the gain error of the integrator. The GE_{RC} induced by 30% *RC* variation can impair the dynamic range of modulator severely [10][11].

3.1.2 Automatic Generation of PWM Clock

The transfer function of an SRMC integrator can be represented as:

$$ITF_{SRMC} = \frac{t_{on}}{T_s}\frac{1}{R_{nom}C_{nom}(1+\Delta\delta_{RC})}\frac{1}{s} \tag{3.9}$$

where t_{on} is the switch-on time in a period T_s.

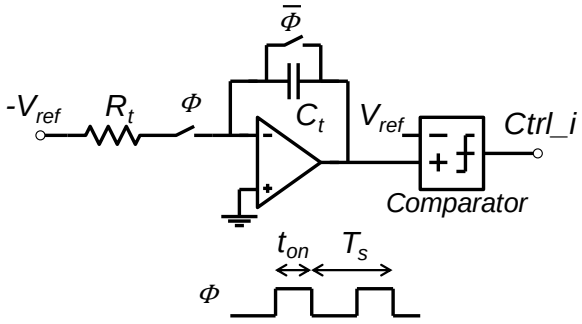


Fig. 3.5 Proposed PWM control signal generator.

To get a proper duty cycle, a simple PWM clock signal generator is proposed as shown in Fig. 3.5. The circuit works as follows. Firstly the charge on the integrating capacitor C_t is cleared, then the PWM control signal ϕ goes up to connect the reference voltage ($-V_{REF}$) to the input and to start the integration. Ideally, the output of integrator (V_O) rises linearly. When it reaches V_{REF}, the continuously-operating comparator detects it and resets ϕ to "low". Thereby, t_{on} is governed by:

$$\frac{V_{ref}}{R_t}t_{on} = C_t V_{ref} \tag{3.10}$$

$$t_{on} = R_t C_t = R_{t,nom}C_{t,nom}\left(1+\Delta\delta_{RC,t}\right) \tag{3.11}$$

where $\Delta\delta_{RC,t}$ is the percentage RC product variation, which is supposed to be the same as that in the main integrators ($\Delta\delta_{RC}$) as matching of R and C values in the same die can be very accurate. From (3.10) and (3.11) we have

$$ITF_{SRMC} = \frac{t_{on}}{T_s}\frac{1}{RC}\frac{1}{s} = \frac{R_{t,nom}C_{t,nom}(1+\Delta\delta_{RC,t})}{T_s s}\frac{1}{R_{nom}C_{nom}(1+\Delta\delta_{RC})} = \frac{R_{t,nom}C_{t,nom}}{T_s}\frac{1}{R_{nom}C_{nom}}\frac{1}{s} \quad (3.12)$$

As a result, the *RC* product variation can be corrected automatically by the PWM technique. In [32]-[34], a similar SRMC filter has been implemented to automatically tune its corner frequency. The automatic duty-cycle-tuning schemes reported in [32]-[34] employ a SC circuit with an accurate time constant as the reference, which is equal to the period of an extra clock multiplies by a capacitor ratio. Compared with that of [32]-[34], the advantage of the tuning scheme here is multifaceted. It is not only for automatic tuning of the *RC* time constant, but also for the compensation of the finite-opamp-bandwidth-induced error, which will be discussed in section IV.

3.1.3 Modulator Architecture

To verify the efficacy of the proposed schemes, a CT cascaded 2-2 modulator is designed as shown in Fig. 3.6. The signal bandwidth is 20 kHz and the sampling frequency is 2.56 MHz with an oversampling ratio (OSR) of 64. To accommodate a ±30% RC time constant variation, the modulator coefficients are synthesized by allocating 9/13 of the clock period (Ts) for integration (under nominal R and C values) and a 1/10 of Ts for the excess loop delay. For a +30% RC time constant variation, the integration time will be extended to about 9/10 of Ts; and for a -30% variation, the integration time will be reduced to about 1/2 of Ts. A 10% of Ts is allocated for the comparator and feedback DAC to settle in order to avoid excess loop delay (ELD) caused by the comparator and the DAC. The comparator starts resolving bits right after

the loop filter enters sleep mode (PWM pulse being “low”). The comparator and the DAC only need to settle before the loop filter awakes in the next clock cycle, which is sufficient.

The CT modulator is synthesized from a DT prototype assuming a Non-Return-to-Zero (NRZ) DAC pulse for the CT modulator. The feedback DAC pulse employed may look like a Return-to-Zero (RTZ) one due to the PWM, but it is essentially NRZ in the sense that the DAC pulse active time is the same as the input signal integrating time. During the “off” phase of the PWM, the input and feedback DAC branches of each integrator are cut off together by the switches (see Fig. 3.6), and the integrators enter asleep mode until the coming of PWM “on” phase in the next period.

Fig. 3.7 reports the behavioral simulation results conducted in Matlab for a -3dBFS 5-*k*Hz input. For comparison, a conventional CT 2-2 cascaded modulator without PWM tuning is also simulated. The two modulators have the same architecture, equivalent coefficients, and the same signal-to-noise-plus-distortion ratio (SNDR) under nominal *RC* values. The simulations sweep the *RC* time constant from -30% to 30% of its nominal value. For the conventional case, its performance in terms of the SNDR is extremely sensitive to *RC* variations. In contrast, the SNDR of the PWM-tuned modulator remains largely unchanged in the presence of the *RC* time constant variation.

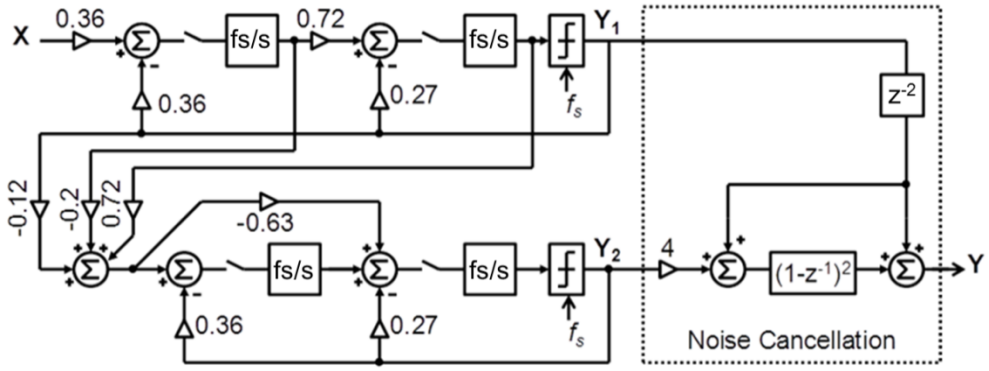


Fig. 3.6 Block diagram of a CT cascaded 2-2 modulator.

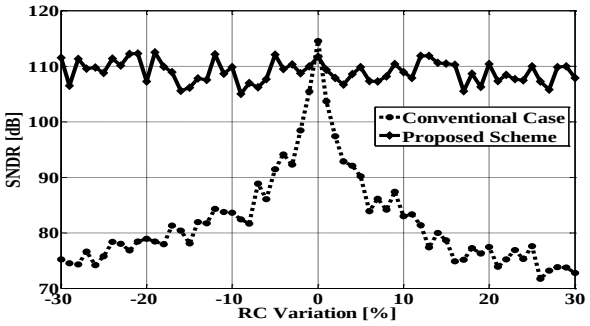


Fig. 3.7 SNDR versus *RC* product variation from behavioral simulations.

3.1.4 Anti-aliasing Filtering

Although the anti-aliasing advantage of continuous-time DSM has been shown to be limited when the opamp finite gain effects is considered [65], if adding the discrete-time nature of the PWM, the anti-aliasing capability of the PWM-tuned CT modulator will degrade further. As shown in Fig. 3.3, the mixing function occurs before the integration, so an anti-aliasing filter is needed. However, as the clock frequency of the modulator can be set high relative to the signal bandwidth, a low-order anti-aliasing filter will suffice for most applications.

Here, we use a first-order active anti-aliasing filter merged into the CT modulator [66], as shown in Fig. 3.8. It is noted that when ϕ is low, the right terminal of R_2 in Fig.

3.8 is not open-circuited in actually implementation (Fig. 3.19). Rather, it is connected to a DC voltage that has the same potential as the virtual ground of the opamp. The input resistor of the first SRMC integrator is divided into two parts, and a capacitor is placed between them. The transfer function of the circuit is:

$$\frac{V_o}{V_{in}} = \frac{1}{sC_i(R_1+R_2)} \frac{1}{1+sC_f(R_1 \| R_2)} \tag{3.13}$$

As shown in Eq. (3.13), the circuit is essentially an integrator preceded by a low-pass filter with a corner frequency of $1/(2\pi C_f R_1 \parallel R_2)$. The input resistance of the SRMC integrator is $R_1 + R_2$. Note that the anti-aliasing filter requires no extra opamp, and thus no extra power consumption.

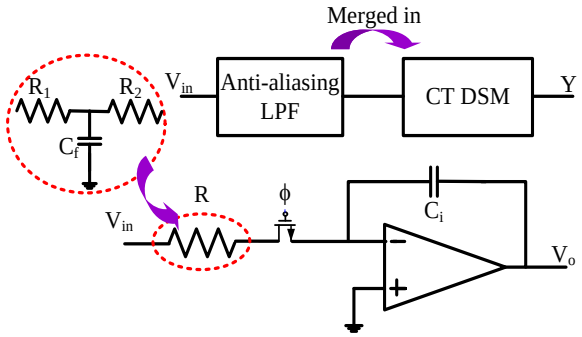


Fig. 3.8 Anti-aliasing low-pass filter merged with SRMC integrator.

3.1.5 Noise Analysis

The resistor and opamp are the two dominant noise sources of the SRMC integrator. Noise from the on-resistance of the switching MOSFET can be negligible or absorbed to the input resistor. Fig. 3.9 shows a representation of the noise sources, where the opamp noise is modeled as a voltage source at its non-inverting input. Both the thermal noise and flicker noise exist in the opamp. However, only the thermal component is analyzed here because it is fundamental and the flicker noise can be

minimized by using large area or other techniques.

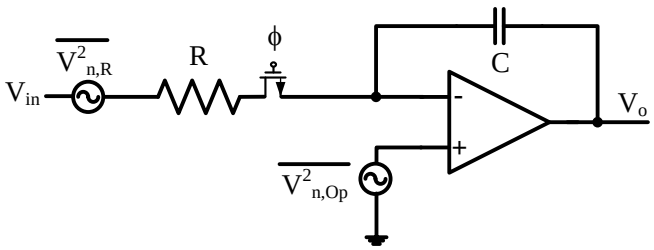


Fig. 3.9 SRMC integrator for noise analysis.

Although it is a time-varying system, the white thermal noise can be considered to be mixed with a PWM signal [33], then the noise power spectral density (PSD) is replicated and scaled by the squared value of each of the Fourier series coefficients of the PWM. Each of these replicas is considered a noise sideband. Because the noise is white, noises in separate sidebands are uncorrelated and their PSDs simply add up [38]. The input resistor's thermal noise is modeled as white noise with double-sided PSD of $S_{R,i} = 2\,kTR$ and the PSD of the opamp's input-referred thermal noise is $S_{Op,i}$. The output thermal noise's PSD is given by:

$$S_{o,SMRC}(\omega) = \sum_{n=-\infty}^{\infty}\left(S_{R,i}\left|\frac{sinc(nd)}{\frac{j\omega RC}{d}}\right|^2\right) + \sum_{n=-\infty}^{\infty}\left(S_{OP,i}\left|sinc(nd)\frac{1+\frac{j\omega RC}{d}}{\frac{j\omega RC}{d}}\right|^2\right) =$$

$$\frac{2KTR\frac{1}{d}}{\left(\frac{\omega RC}{d}\right)^2} + S_{Op,i}\frac{1+\left(\frac{\omega RC}{d}\right)^2}{\left(\frac{\omega RC}{d}\right)^2}\frac{1}{d} \tag{3.14}$$

where the following approximation is applied:

$$\sum_{n=-\infty}^{\infty} sinc^2(nd) \approx \sum_{n=BW_n/f_s}^{BW_n/f_s} sinc^2(nd) \approx 1/d \tag{3.15}$$

Here, BW_n and f_s are the noise bandwidth and the PWM clock frequency respectively [39]. We can now compare this output-referred noise PSD to that of an equivalent CT *RC* integrator, which is:

$$S_{o,CT}(\omega) = 2KTR_c\frac{1}{(\omega R_cC)^2} + S_{Op,i}\frac{1+(\omega R_cC)^2}{(\omega R_cC)^2} = 2KTR\frac{1/d}{(\omega RC/d)^2} + S_{Op,i}\frac{1+(\omega RC/d)^2}{(\omega RC/d)^2} \quad (3.16)$$

Here, R_c and C are the CT resistor and capacitor values respectively, and $R_c = R/d$. A comparison between Eq. (3.14) and Eq. (3.16) shows that the noise contribution from the resistors in the SRMC integrator is the same as that of an equivalent CT integrator, independent of duty cycle. For the opamp noise, there is a duty-cycle dependency in the SRMC integrator, and it is slightly larger in the SRMC case.

3.2 Proposed SRMC Integrator with CDS

The non-ideality induced by the finite opamp dc gain of integrator is known as leaky integration, which damages the performance of DSMs, especially for cascaded ones. Here we propose to apply the CDS technique, which is traditionally used in SC circuits [40]-[44] and CT filters [67], in the SRMC CT modulator to enhance the effective dc gain of the opamp, in addition to the side functions of flicker noise and offset suppression. In this case, compared with the DT counterparts by SC circuits, the CTDSMs with CDS also have most of the inherent advantages of conventional CTDSMs, such as relaxed opamp speed requirements, higher sampling frequency possible with low power consumption.

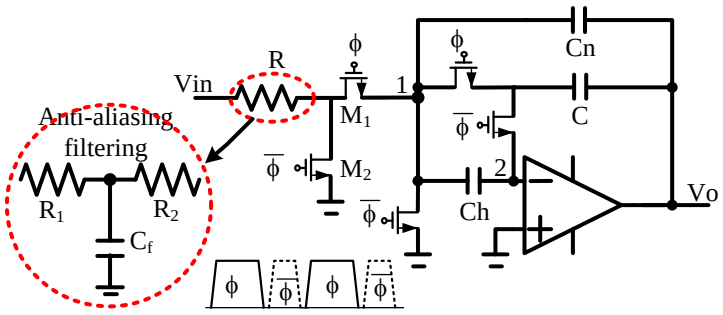


Fig. 3.10 Proposed SRMC integrator with CDS.

Fig. 3.10 shows the schematic of the proposed SRMC integrator with CDS. C_h is an error holding capacitor. During the $\bar{\phi}$ phase, the voltage V_2 at node 2, being equal to $V_{o,phi\_end}/A_{dc}$ (where A_{dc} is the opamp dc gain, and V_{o,phi_end} is the output voltage at the end of the ϕ phase), is sampled across C_h; during the ϕ phase, C_h is placed in series with the inverting input of opamp. Due to the correlation between successive samples of V_2, the magnitude of the error due to low opamp gain seen at node 1 during phase ϕ is cancelled to the first order, resulting in a significant reduction for the finite-gain effect [40]-[44]. Meanwhile, the flick noise and offset from opamp can also be cancelled effectively.

The value of the hold capacitor C_h needs to be designed carefully. If its value is too large, during phase $\bar{\phi}$, more charges leak from the integration capacitor C to C_h. On the other hand, if its value is too small, e.g., comparable with the parasitic capacitor of its periphery switches, the charge on these parasitic capacitor will make the voltage V_2different from its original value $V_{o,phi\_end}/A_{dc}$, thus the reduction for the finite-gain effect will be affected.

Another auxiliary capacitor C_n, connecting between the output node and node 1, is used to provide feedback during the non-overlapping period between the ϕ phase and

the $\bar{\phi}$ phase. It is not necessary if the parasitic capacitor of its periphery switches can provide this function [45].

An extra switch M_2 driven by phase $\bar{\phi}$ is added [33] to steer current to ground in phase $\bar{\phi}$ such that the current loading through the resistor branches is consistent over both clock phases. This also helps to minimize signal feed-through in phase $\bar{\phi}$.

3.2.1 Analysis on the opamp gain enhancement

The transfer function of the conventional CT integrator with finite gain opamp is [10]:

$$ITF_{A_{dc}}(s)|_i \approx -\frac{1}{R}\frac{1}{sC-\frac{1}{A_{dc}R}} \tag{3.17}$$

which is represented by solid line in the signal flow graph (SFG) in Fig. 3.11. By applying the CDS, a feedback path is built, represented by the dotted line in the SFG. With the CDS, the integrator's transfer function changes to:

$$\left(\frac{V_{in}(s)}{R}-V_o(s)\frac{-1}{A_{dc}}\frac{1}{R}e^{-sT}\right)\frac{-1}{sC-\frac{1}{A_{dc}R}}=V_o(s)$$

$$\frac{V_o(s)}{V_{in}(s)}=-\frac{1}{R}\frac{1}{sC-\frac{1}{A_{dc}R}(1-e^{-sT})} \tag{3.18}$$

where the relationship between the z-variable (z-transform) and s-variable (Laplace transform) of $z^{-1}=e^{-sT}$ is used.

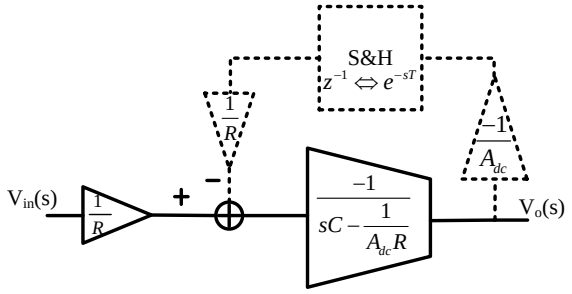


Fig. 3.11 Signal flow graph of the integrator with opamp gain enhancement by CDS.

Compared with the conventional case in Eq. (3.17), the finite-gain induced pole error is first order high-passed now. That means the effective gain of opamp at the signal band is enhanced by the CDS technique.

For the PWM control signal generator, the gain enhancement by the CDS technique is not applied for the reasons below, although it could be useful to reduce the flicker noise and offset.

The finite opamp gain induced error in the PWM control signal generator is less important compared to that in the modulator's loop filter. The analysis can be based on its transfer function:

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{1}{RC}\frac{1}{s-\frac{1}{A_{dc}RC}}$$

$$V_{in}(t) = -V_{ref} = constant$$

$$V_o(t) = \frac{V_{ref}}{RC}\int_0^{t_{on}} e^{\frac{1}{A_{dc}RC}t}dt = \frac{V_{ref}}{RC}t_{on} + \frac{V_{ref}}{RC}\frac{1}{A_{dc}RC}\frac{t_{on}^2}{2} +$$

$$\frac{V_{ref}}{RC}\frac{\left(\frac{1}{A_{dc}RC}\right)^2}{2}\frac{t_{on}^3}{3} + \cdots \approx \frac{V_{ref}}{RC}t_{on} + \frac{V_{ref}}{RC}\frac{1}{A_{dc}RC}\frac{t_{on}^2}{2} = \mathrm{V_{ref}}$$

$$t_{on} = RC(\sqrt{(A_{dc}+1)^2-1} - A_{dc}) \qquad (3.19)$$

For ideal case, which is with infinite opamp gain $A_{dc} \to \infty$,

$$t_{on,ideal} = RC \tag{3.20}$$

A t_{on} error is defined as

$$\frac{t_{on}-t_{on,ideal}}{t_{on,ideal}} = \sqrt{(A_{dc}+1)^2-1} - (A_{dc}+1) \tag{3.21}$$

For example:

Type equation here.

$$\frac{t_{on}-t_{on,ideal}}{t_{on,ideal}} = -0.5\% \text{ when } \mathrm{A_{dc}} = 100$$

$$\frac{t_{on}-t_{on,ideal}}{t_{on,ideal}} = -0.98\% \text{ when } \mathrm{A_{dc}} = 50$$

Fig. 3.12 shows the relationship between the t_{on} error and the opamp dc gain. Essentially, the t_{on} error is equivalent to the integrator gain error. Fig. 3.7 shows that the 1% integrator gain error does not have significant impact on the SNDR of the CT cascaded DSM (drops from 117dB to 113 dB).

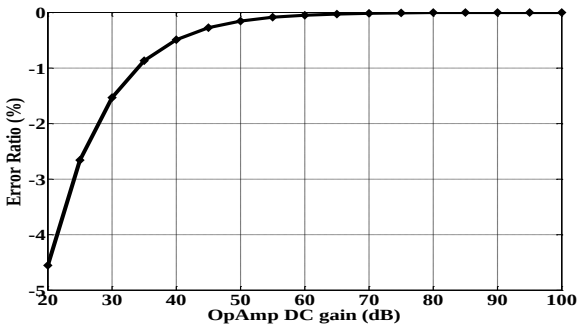


Fig. 3.12 Effect of opamp dc gain on the t_{on} error in the PWM control signal generator.

3.2.2 Simulation Results

Behavioral simulations are conducted on the modulator of Fig. 3.6 for a -3dBFS 5-*k*Hz input. The simulations sweep the first opamp gain from 10dB to 100dB, and keep the other opamps ideal. The simulated SNDR is shown in Fig. 3.13. It is seen that

for the conventional case without the CDS technique, the SNDR degrades significantly due to a drop in opamp gain variation; but with the CDS technique, the SNDR remain largely unchanged for the said range of opamp dc gain.

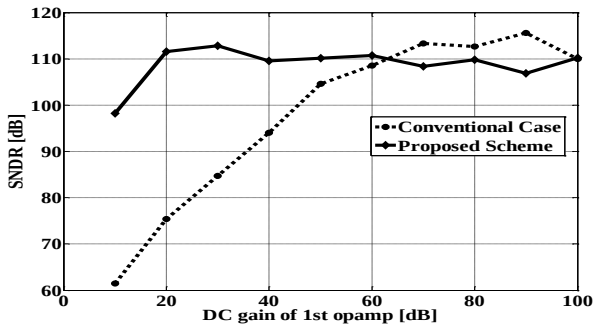


Fig. 3.13 SNDR versus opamp dc gain from behavioral simulations.

3.3 Compensation for Finite-Opamp-Bandwidth-Induced Error

Finite opamp bandwidth is known to cause distortion and increased in-band noise in SC modulators. The GBW requirement is even higher in cascaded SC modulators due to their adverse effect on quantization noise cancellation. The GBW in those modulators needs to be at least 7-10 times of the sampling frequency [46]-[50].

In contrast, single-loop CT modulators have been claimed to be able to work with much lower GBW of the opamps [51]-[52], largely attributed to the absence of the high-current peaks that exist in SC modulators. However, for CT cascaded modulators, high opamp GBW is still required in order not to degrade the quantization noise cancellation [10][11]. An extended finite GBW model has been proposed in [10][11] to do the compensation by adjusting the CT loop filters. It is depending on the estimation of GBW, which is not accurate for process variations.

3.3.1 Compensation for fininte opamp bandwidth

The integrator's transfer function with finite opamp bandwidth can be expressed as [10]:

$$ITF_{GBW}(s)|_i \approx \frac{GBW}{GBW+\omega_{i,eff}} \frac{1}{RC} \frac{1}{s} \tag{3.22}$$

where $\omega_{i,eff} = k_i f_s = 1/RC$ is the corner frequency of integrator and GBW represents gain-bandwidth product of the opamp. If GBW is infinite, transfer function in (3.22) reduces to the ideal one:

$$ITF_{GBW}(s)|_i \approx \frac{1}{RC} \frac{1}{s} \tag{3.23}$$

To compensate for the finite bandwidth induced error, a trivial method is to use corrected modulator coefficients based on the simulated GBW values:

$$ITF_{GBW,corr}(s)|_i \approx \frac{GBW}{GBW+\omega_{i,eff}} \frac{1}{R_d C_d} \frac{1}{s} = \frac{1}{RC} \frac{1}{s} \tag{3.24}$$

if $R_d C_d = RC \frac{GBW}{GBW+\omega_{i,eff}}$.

However, this rough correction method is not accurate for two reasons: 1) GBW variation due to process variation; 2) discrepancy between simulation and the real circuit.

Here we propose another method to compensate for the finite opamp bandwidth. In the previous section, an auxiliary SRMC integrator has been employed to correct the *RC* product variation. Here, we use the same circuit block to deal with the finite opamp bandwidth problem.

Assuming the opamp is single-stage, the finite-opamp-bandwidth-induced gain

error in the first SRMC integrator of the CT cascade DSM is

$$GE_{GBW,1st} = \frac{GBW_{1st}}{GBW_{1st}+\omega_{\mathrm{eff},1st}} = \frac{\frac{g_{m1}}{C_1}}{\frac{g_{m1}}{C_1}+\frac{1}{R_{1,\mathrm{eff}}C_1}} = \frac{g_{m1}}{g_{m1}+\frac{1}{R_{1,\mathrm{eff}}}} \quad (3.25)$$

where g_{m1} is the input transistor's transconductance of the opamp, C_1 and $R_{1,eff}$ are the integration capacitor and equivalent integration resistor of the first SRMC integrator. Meanwhile, the finite-opamp-bandwidth-induced gain error in the auxiliary SRMC integrator is

$$GE_{GBW,aux} = \frac{GBW_{aux}}{GBW_{aux}+\omega_{\mathrm{eff},aux}} = \frac{g_{m,aux}}{g_{m,aux}+\frac{1}{R_{aux,\mathrm{eff}}}} \quad (3.26)$$

where $g_{m,aux}$, C_{aux} and $R_{aux,eff}$ correspond to those of the auxiliary SRMC integrator. In the design phase, if we make

$$g_{m1}R_{1,eff} = g_{m,aux}R_{aux,eff} = k\ (constant) \quad (3.27)$$

then the gain error of the main integrator traces that of the auxiliary integrator:

$$GE_{GBW,aux} = GE_{GBW,1st} = \frac{k}{k+1} \quad (3.28)$$

Thereby, the finite-opamp-bandwidth-induced gain error in the first SRMC integrator can be automatically tuned out by the PWM control signal generator circuit, just as the automatic tuning of *RC* time constant.

It is well known that the first integrator is the dominant error source and the most power consuming block in a modulator. To fulfill thermal noise requirements, the capacitor of the first integrator is often very large. The use of a low bandwidth opamp based on the proposed compensation scheme can save power consumption substantially.

One compensation circuit cannot support multiple integrators, that is,

$$g_{m1}R_{1,eff} = g_{m,aux}R_{aux,eff} = k \neq g_{m2}R_{2,eff} \neq \cdots \quad (3.29)$$

The above proposed compensation scheme does not work for the other integrators in the modulator. However, their integration capacitors are often much smaller and their errors are suppressed by the modulator so the finite-opamp-bandwidth compensation is not necessary for other integrators.

In addition to the induced gain error, the finite GBW also introduces a second pole which may increase the ELD. However, for cascaded CT DSM, the finite GBW induced gain errors dominate the behavior due to the cascaded structures' high sensitivity to it, and the second pole effect can be ignored [10].

3.3.2 Behavorial Simulation Results

Behavioral simulations in Matlab are carried out on the modulator of Fig. 3.6 to verify the finite-opamp-bandwidth compensation scheme. Again, a -3dBFS 5-*k*Hz input is used. The simulations sweep the GBW of the first opamp from 0.1 to 100 times the sampling frequency, and keep other opamps ideal. The simulation results depicted in Fig. 3.14 show that for the conventional case without the compensation scheme, the SNDR can drop by 40dB; but with the compensation scheme, its SNDR remains largely unchanged for the said range of GBW.

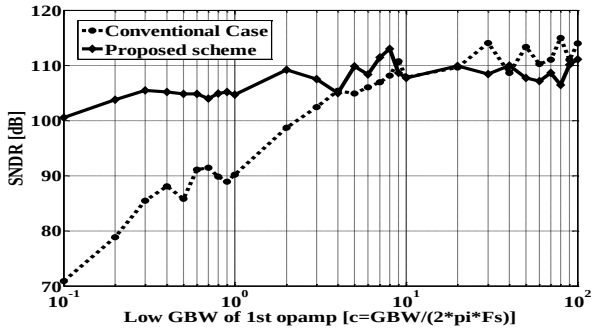


Fig. 3.14 SNDR versus opamp's GBW from behavioral simulations.

3.4 Jitter Analysis

The sampling action in a CT modulator occurs at the input of the quantizer, so the error induced by the sampling clock jitter is suppressed by the feedback loop in the band of interest and is usually not important. However, the error induced by the clock jitter of the feedback DAC is equivalent to an error at the input. It is not attenuated by the feedback loop at all and thus needs special attention [10].

Various jitter analysis approaches can be found in the literature [10][52][53]. Here, the clock-jitter-induced error of a signal is modeled as an error in the signal's magnitude.

The jitter effect in the proposed PWM-tuned modulator may be falsely regarded as the same as in the return-to-zero (RZ) DAC case. They are different. For the RZ DAC case, both the rising and falling edges of the clock encounter jitter errors. However, in the proposed PWM-tuned modulator, only the rising edge encounters jitter (Fig. 3. 15(b)). The falling edge is not affected by the clock signal, but by the duty cycle fluctuation due to the noise in the PWM generator circuit. The duty cycle

fluctuation is referred to as *duty cycle jitter* here (Fig. 3. 15(c)). The overall jitter error is the superposition of these two error sources (Fig. 3. 15(d)).

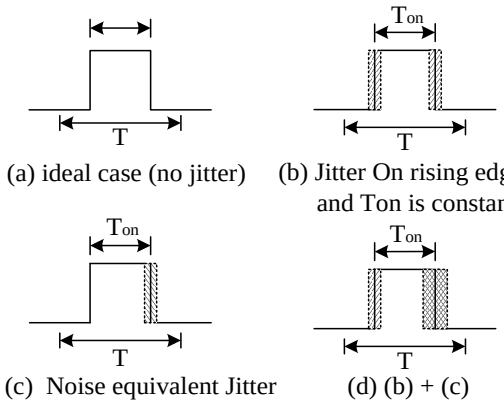


Fig. 3.15 Jitter components.

3.4.1 Jitter on Rising Edges

Let us first consider the jitter error on rising edge alone (no duty cycle jitter). In this case, only input signal branch is affected, as the pulse width of PWM signal will not be impacted, and then the integration from the feedback DAC branch will not be influenced. Let the timing error on the rising edge be $\Delta t_r(n)$ at time *n*, and assume it be much smaller than the on-time T_o of the PWM clock. The resulted equivalent input magnitude error $e_{j,r}(n)$ in the n^{th} cycle is:

$$e_{j,r}(n) \approx \big(u_E(n) - u_S(n)\big)\frac{\Delta t_r(n)}{T_s} \tag{3.30}$$

where $u_S(n)$ and $u_E(n)$ are the integrator's input at the start and end, respectively, of the integration time of the nth period. Fig. 3.16 illustrates this error model.

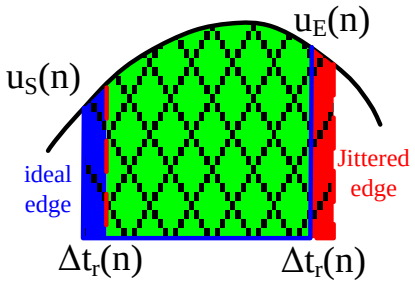


Fig. 3.16 Error induced by the rising edge clock jitter.

The input difference $\left(u_E(n) - u_S(n)\right)$ and the rising edge jitter $\Delta t_r(n)$ can be considered as statistically independent. If the rising edge jitter is a white noise process, the jitter-induced noise power in the band of interest is:

$$\begin{aligned}\sigma_{e_{j,r}}^2\Big|_{\text{inband}} &= \frac{1}{OSR}\left(\frac{\sigma_{j,r}}{T_s}\right)^2 \sigma_{(u_E(n)-u_S(n))}^2 \\ &= 4 \cdot OSR \cdot BW^2 \cdot \sigma_{j,r}^2 \cdot \sigma_{(u_E(n)-u_S(n))}^2\end{aligned} \tag{3.31}$$

where $\sigma_{j,r}^2$ and $\sigma_{(u_E(n)-u_S(n))}^2$ are the variances of the rising-edge clock jitter and the signal $\left(u_E(n) - u_S(n)\right)$ respectively, BW is the signal bandwidth and T_s is the period.

For a sinusoidal input $u_S(n) = A \cdot \sin\left(\omega_{sig} \cdot nT_s\right)$, we have the following expression for the difference $\left(u_E(n) - u_S(n)\right)$:

$$\begin{aligned}u_E(n) - u_S(n) &= A \cdot \sin\left(\omega_{sig} \cdot (nT_s + T_o)\right) - A \cdot \sin\left(\omega_{sig} \cdot nT_s\right) \\ &= 2Acos\left(\omega_{sig}\frac{2nT_s+T_o}{2}\right)\sin\left(\omega_{sig}\frac{T_o}{2}\right) \\ &= 2A\sin\left(\frac{d\pi}{2OSR_{sig}}\right)\cos\left(\omega_{sig}\frac{2nT_s+T_o}{2}\right)\end{aligned} \tag{3.32}$$

where $d = T_o/T_s$ is the duty cycle, $OSR_{sig} = f_s/2f_{sig}$, which is larger than or equal to the OSR for $f_{sig} \le BW$. If $d\pi/2OSR_{sig} \ll 1$, then:

$$u_E(n) - u_S(n) \approx \frac{Ad\pi}{OSR_{sig}}\cos\left(\omega_{sig}\frac{2nT_s+T_o}{2}\right) \tag{3.33}$$

So, the power of the signal-related component of the $\left(u_E(n) - u_S(n)\right)$ is given by

$\sigma^2_{(u_E(n)-u_S(n))} \approx \frac{(Ad\pi)^2}{2(OSR_{sig})^2}$. The rising edge jitter-induced error power in the band of interest becomes:

$$\sigma^2_{e_{j,r}}\Big|_{\text{inband}} = 4 \cdot OSR \cdot BW^2 \cdot \sigma^2_{j,r} \cdot \frac{(Ad\pi)^2}{2(OSR_{sig})^2} \tag{3.34}$$

which is equivalent to the jitter effect on the DT modulator.

To verify the above analysis, behavioral level simulations on the modulator of Fig. 3.6 are conducted in Matlab. A clock pulse with jittered edges is used to implement the start instants of the PWM control signal. In the simulations, a -9 dBFS 5-*k*Hz input signal is used to estimate the in-band noise (IBN). The simulated IBN and the calculated IBN by Eq. (3.34) are shown in Fig. 3.17. Although Eq. (3.34) only gives a rough estimation of the rising edge jitter, it is clearly seen that in both simulated and calculated results, the IBN caused by the rising edge jitter is way below that by the duty cycle jitter (to be discussed in the next subsection). Thereby the rising-edge jitter can be ignored in the design.

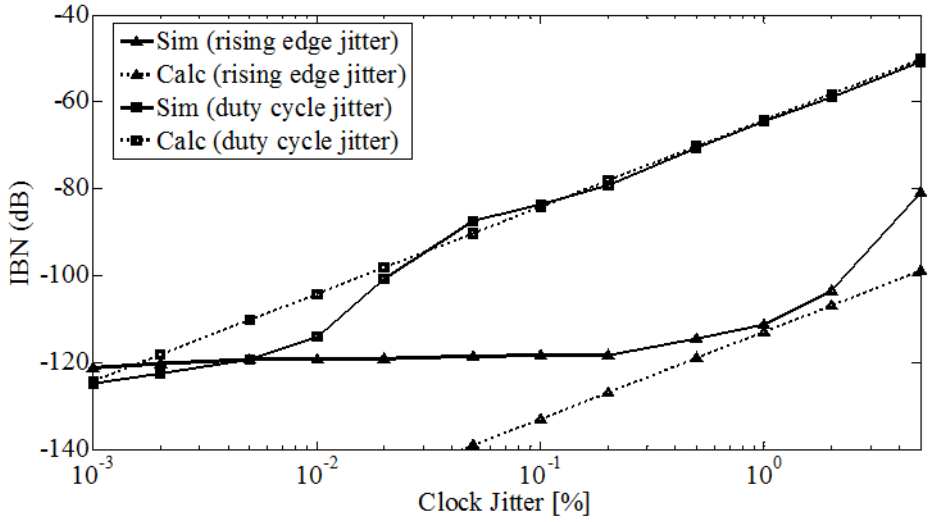
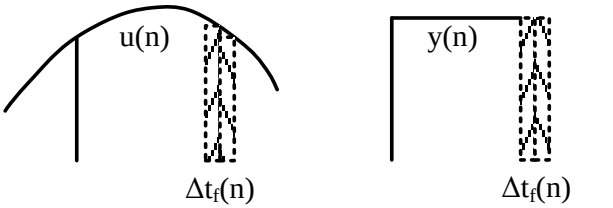


Fig. 3.17 Simulated and calculated jitter-induced in-band noise.

3.4.2 Duty cycle jitter

Let us now consider the *duty cycle jitter* alone now. This jitter has an effect in both the input signal and the feedback DAC, as illustrated in Fig. 3.18.



(a) Input branch error (b) DAC branch error

Fig. 3.18 Duty cycle jitter.

Let the duty cycle jitter at n[th] period be $\Delta t_f(n)$, which is also the timing error of the falling transition edge. The equivalent magnitude error $e_{j,f}(n)$ in the n^{th} period is

$$e_{j,f}(n) = \big(y(n) - u(n)\big)\Delta t_f(n)/T_S \tag{3.35}$$

where $y(n)$ is the DAC's output at time n. Assume the signal transfer function of modulator is unity, then $y(n) - u(n)$ equals to the quantization noise filtered by the noise transfer function *NTF*. Thereby,

$$\sigma_{e_{j,r}}^2\Big|_{\text{inband}} = \frac{1}{OSR}\sigma_{e_{j,f}}^2 = \frac{4}{d^2}OSR \cdot BW^2\sigma_{j,f}^2\frac{\Delta^2}{12}\frac{1}{2\pi}\int_{-\pi}^{\pi}\left|NTF(e^{j\omega})\right|^2 d\omega \tag{3.36}$$

where $\sigma_{j,f}^2$ is the variance of the duty cycle jitter, and Δ is the step size of the quantizer. Behavioral simulations in MATLAB are carried out on the modulator of Fig. 3.6 to verify the above analysis on duty cycle jitter. Here, a voltage noise source with root-mean-squared value $\sigma_{j,f}$ is added in the front-end of the comparator in the PWM generator to imitate the duty cycle jitter. A -9 dBFS 5-*k*Hz input is used for IBN estimation. The results are depicted in Fig. 3.17. It is seen that Eq. (3.36) is in a good agreement with the simulated results.

3.5 Prototyping Modulator Design

The CT cascaded modulator of Fig. 3.6 with the proposed techniques is designed in a 0.18-μm 1P6M twin-well CMOS technology. The device threshold voltages in the technology are 0.45V and -0.5V for NMOS and PMOS respectively. Metal-insulator-metal (MIM) capacitors and non-salicide N+ poly resistors are used.

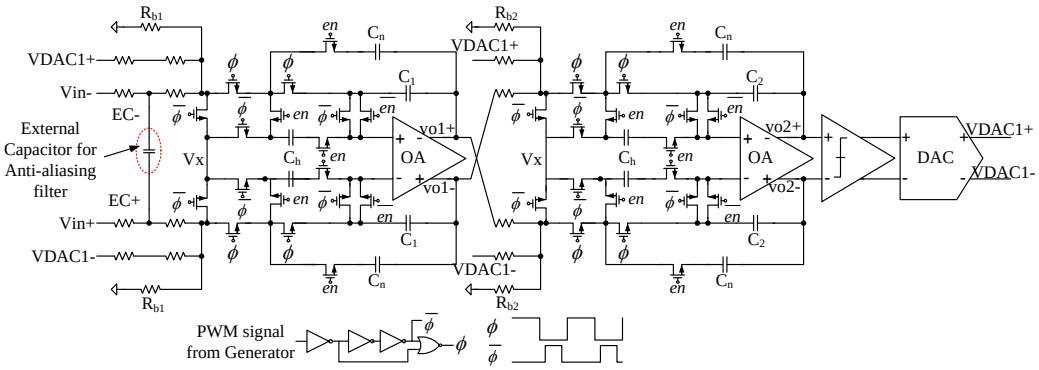


Fig. 3.19 Schematic of the first stage of the proposed CT 2-2 cascaded modulator

Fig. 3.19 shows the schematic of the first stage of the CT 2-2 cascaded modulator. The second stage is similar. The loop filter for each stage uses two SRMC integrators. One-bit quantizers are used for both stages. As stated earlier, the modulator operates at a sampling frequency 2.56 *M*Hz for a 20 *k*Hz signal band. It is noted that the proposed scheme also applies to multi-bit modulators, where dynamic element matching operation can be performed during the "low" time of the PWM signal to avoid generating extra ELD. The CT modulator in Fig. 3.19 displays some similarity to a discrete-time modulator, but it is indeed a CT one. First, as analyzed in Fig. 3.4, the input signal is not sampled, but mixed with a square waveform. Second, there is no switch at the input of the modulator and the outputs of the opamps. It uses switches only around the virtual ground nodes and at the DAC's outputs. These are

narrow-voltage-swing switches and do not generate nonlinearity. Last, the inputs to the integrators (from the input signal and from the feedback DAC) are CT. The settling requirement on the opamps is thus lower than that for a DT modulator.

In the circuit, the CDS technique is enabled by putting the control signal "en" high and "$\overline{\text{en}}$" low, and is disabled by the complementary setting of these signals. Incorporating such a control signal allows us to compare modulator's performance with and without the CDS. An external capacitor is used for anti-aliasing. The off-chip capacitor is not necessary if anti-aliasing is not a concern.

The modulator operates from a low supply voltage of 0.8 V. For simplicity and flexibility, external references are used in the PWM signal generator (see Fig. 3.5). From Eq. (3.11), the duty cycle is not a function of the reference voltage. However, the reference must be clean as any noises there will bring in duty cycle jitter. The offset infection in the PWM signal generator should also be considered: the opamp offset can be cancelled by CDS technique; for the comparator, good matching in the layout can make its offset less than 5mV, which will induce about 1% absolute error on the PWM pulse width, also the dynamic range will not be impacted largely (see Fig. 3.7).

For the PWM tuning circuit implementation, some non-idealities should be considered in the following: first, enough opamp GBW in the PWM signal generator is required to avoid the opamp non-linearity induced pulse width error under different RC time constant variation; second, the comparator induced delay should be cancelled by using some delay cell to postpone the start point of integration; third, the noise at

the input nodes of comparator should be optimized, as the noised induced duty cycle jitter will degrade the dynamic range of the modulator as shown in Fig. 3.17.

For the opamp bandwidth compensation, we chose $g_{m1}R_{1,eff} = g_{m,aux}R_{aux,eff}$. In the layout, the resistors and capacitors of PWM generator are placed close to those in the first SMRC integrator for better matching.

To accommodate for the low supply voltage, additional resistors R_b (see Fig. 3.19) are used to bias the opamp's input common-mode (CM) voltage at about 0.2 V to allow the pmos-input opamp to have a sufficient gate-to-source bias voltage [54]. The dc voltage V_x in Fig. 3.19 is thus set at 0.2V. During the "off" phase of the PWM, it dumps currents from the input, feedback DAC and R_b branches to ground. This V_x can thus be power-efficiently buffered by a class-AB buffer if on-chip buffer is desired. Besides, the input CM voltage needs not to be very accurate; low-gain low-power buffer can be used. In this implementation, however, off-chip buffers are used for V_x. The dc settings here also help the NMOS switches to turn on and off sufficiently under the 0.8-V supply. For NMOS switches, proper sizing can make their resistance only 1/1000 of that in the input signal branch. A beauty of the proposed modulator is that all the switches only need to handle narrow-voltage-swing signals as these signals are all near the virtual ground nodes of the op-amps. Thereby, the distortion induced by the varying resistance of NMOS switches is negligible.

With the aim of verifying the effectiveness of the opamp dc gain compensation by CDS, a single-stage telescopic opamp is designed to barely meet the minimum dc gain requirement (30dB). The schematic of the opamp is shown in Fig. 3.20. The

opamp's output CM level is set at 0.4V by a CT common-mode feedback (CMFB) circuit. Its differential output swing is about $\pm$0.38V. A low GBW of 9 *M*Hz is intentionally designed to save power and for verifying the effectiveness of the proposed GBW compensation scheme.

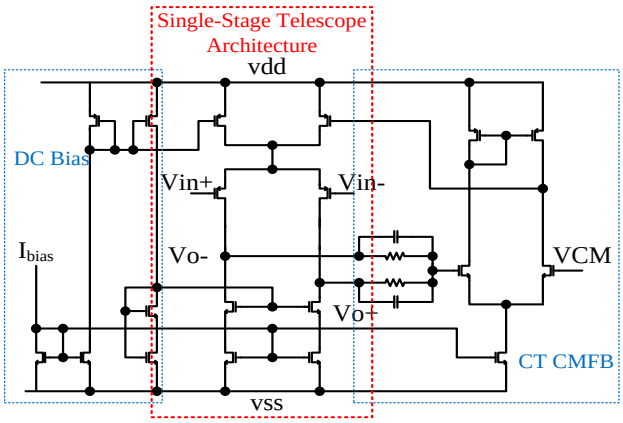


Fig. 3.20 Schematic of the telescopic opamp.

Fig. 3.21 shows an output spectrum of the modulator obtained from transistor-level simulations. The stimulus is a 5-*k*Hz 0.6-V_{pp} differential signal. The simulated SNDR is 87.2dB, SNR is 88.6dB, and spurious-free dynamic range (SFDR) is 92.6dB under nominal *RC* values. Fig. 3.22 shows the SNDR when the *RC* time constants are swept from -25% to 25% of their nominal values. The results show that the SNDR of the modulator varies by less than 3 dB for the said *RC* time constant variation range.

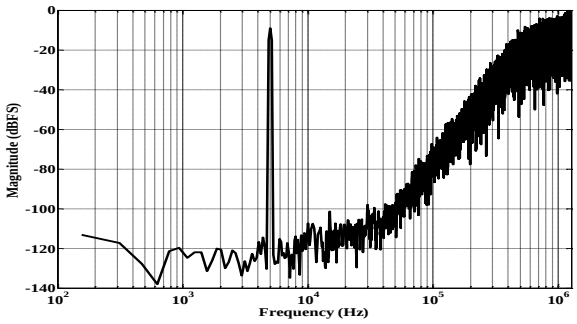


Fig. 3.21 Output spectrum of the proposed modulator for a 5-kHz 0.6-$V_{pp,diff}$ input from transistor-level simulations.

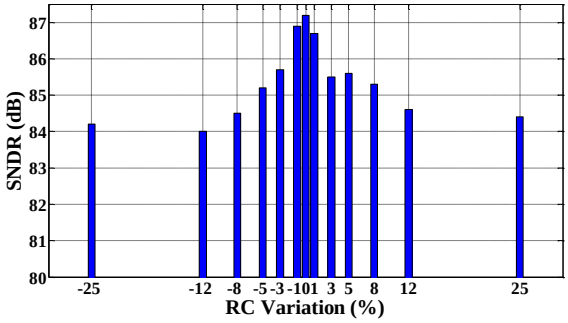


Fig. 3.22 SNDR versus *RC* time constant variation from transistor-level simulations.

3.6 Measurement Results

The prototype modulator was fabricated in the 0.18-μm 1P6M twin-well CMOS technology. Fig. 3.23 shows the die photograph. The active die area is 0.78 mm^2. Compared with the conventional implementation, the prototype design involves an auxiliary PWM signal generator and some extra switches and error holding capacitors in every stage. The corresponding area overhead can be within 15% of total area. The CDS will not affect the total current consumption.

In the measurement, the modulator outputs were captured using a logic analyzer and the data was processed offline on a computer. The testing setup and environment are shown in Fig. 3.24 and Fig. 3.25 respectively.

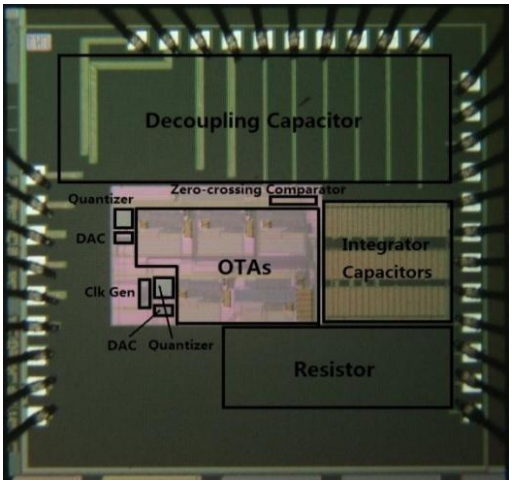


Fig. 3.23 Die microphotograph.

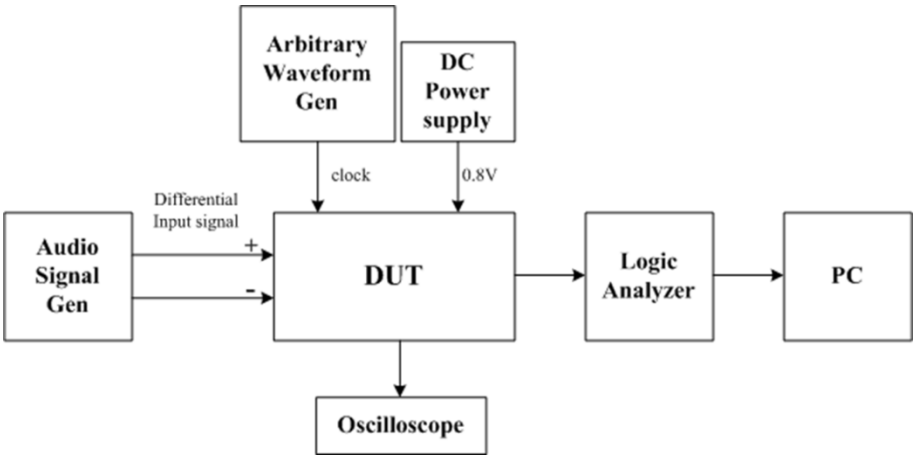


Fig. 3.24 Measurement setup

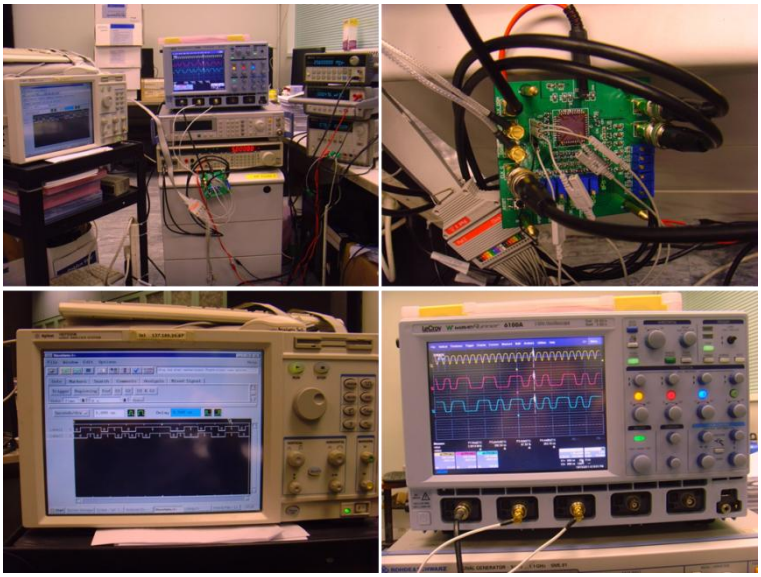


Fig. 3.25 Measurement environment

Fig. 3.26 shows the measured SNR and SNDR of the modulator for input magnitude varying from -100dBFS to 0 dBFS (0 dBFS = $1.6V_{pp}$ differential). The results for CDS being enabled and disabled are both shown. The SNDR measurement uses a 5-*k*Hz sinusoidal input so that the third harmonic appears in the signal band, while the SNR measurement uses a 15-*k*Hz tone. The peak SNR, SNDR and DR are 83.4 dB, 82.7 dB and 87dB respectively when the CDS technique is enabled. The gaps to the simulated values are attributed to noise and some other non-ideal effect that cannot be modeled accurately in the transistor-level. These values become 57.8 dB, 54.8 dB and 58dB when the CDS technique is disabled. The measured SNDR and SNR values are closed to the simulated values presented in the previous section. It is seen that the CDS improves the modulator's performance significantly.

Fig. 3.27 (a) and (b) shows the measured output spectrum of the modulator when the CDS is enabled and disabled, respectively, for a -3 dBFS 5-*k*Hz input. It can be seen that the CDS technique reduces both the in-band noise and the harmonic tones substantially. The SFDR significantly improves from 65dB to 90.4dB when the CDS is enabled.

Fig. 3.28 shows the measured anti-aliasing performance. A -3 dBFS 2.565 *M*Hz (2.56 *M*Hz + 5 *k*Hz) signal was used as the stimulus. Comparing Fig. 3.25 (a) to Fig. 3.26, it is found that the aliasing signal is suppressed by 54 dB, a good agreement with the theoretical calculation.

Table V summarizes the modulator's performance. To quantify its overall performance, the following figures-of- merit (FoMs) are used [55]:

$$FoM_1 = \frac{Power(W)}{2^{ENOB(bits)} \cdot DOR(S/s)} \cdot 10^{12} \quad (3.37)$$

$$FoM_2 = 2kT \frac{3 \cdot 2^{ENOB(bits)} \cdot DOR(S/s)}{Power(W)} \cdot 10^5 \quad (3.38)$$

where k is the Boltzmann constant and T is the circuit temperature (measured in K). FoM_1 emphasizes power consumption, whereas FOM_2 emphasizes effective resolution. The smaller the FoM_1 and the larger the FoM_2, the better the DSM is. The modulator achieves an FoM_1 of 0.36pJ/conv and an FoM_2 of 126.

Table VI compares the performance of the presented modulator with other state-of-the-art cascaded modulators. In [7][8][56]-[61][66], switched-capacitor implementation is employed in different applications. The large power is mainly attribute to high opamp GBW for opamp settling requirement in discrete time system. In In [6][23][62][63] by continuous time, large RC time constant variation requires enough enough dynamic range design margin, which should reduce the energy efficiency accordingly. In the proposed design, attributed to techniques described, this modulator shows the best FOM_2 among these cascade modulators. Its FoM_1 is also among the best. It is stressed that the presented modulator was mainly designed to verify the effectiveness of the proposed techniques. There is much room for further power optimization.

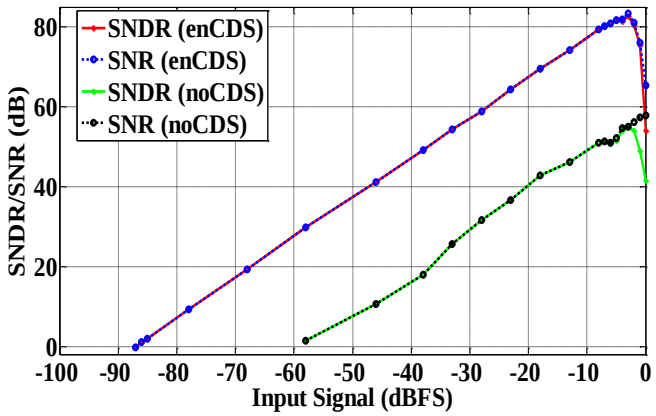
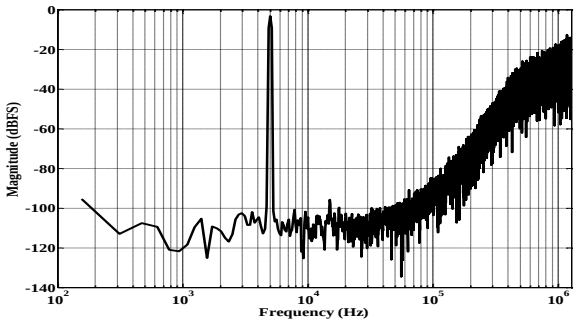
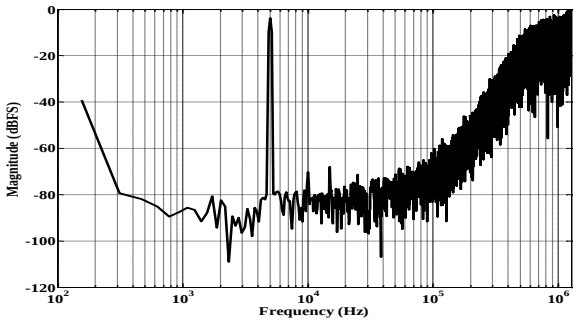


Fig. 3.26 Measured SNR and SNDR versus input magnitude (0 dBFS = $1.6V_{pp}$ differential). "enCDS" and "noCDS" stand for CDS enabled and disabled respectively.



(a)



(b)

Fig. 3.27 Measured output spectrum for a -3 dBFS 5-*k*Hz input when (a) the CDS is enabled and (b) the CDS is disabled.

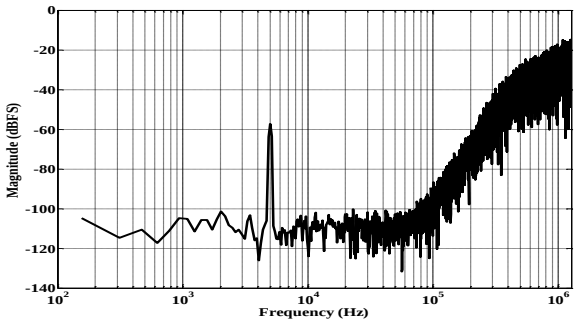


Fig. 3.28 Measured output spectrum for a -3 dBFS, 2.565 *M*Hz input.

Table V Modulator Performance Summary.

Modulator Type	CT cascaded 2-2 single-bit	
Sampling Frequency	2.56 *M*Hz	
Signal Bandwidth	20 *k*Hz	
Supply Voltage	0.8 V	
Total Current Consumption	0.33 *m*A	
Input Signal Range	$1.6V_{pp}$ differential	
	CDS enabled	CDS disabled
Peak SNDR	82.7 dB	57.8 dB
Peak SNR	83.4 dB	54.8 dB
DR	87 dB	58 dB
SFDR	90.4 dB	65 dB
ENOB	14.2 bit	-
Area	0.78 mm^2	
Process	0.18 μm CMOS	

Table VI Performance Comparison with State-Of-The-Art Cascade Modulator.

Reference	Type	ENOB (bit)	Bandwidth (MHz)	Process (μm CMOS)	Power (mW)	FoM_1 (pJ/conv)	FoM_2
Bosi 2005 [56]	SC-Cascade	12.2	10	0.18	240	2.55	4.6
Dezzani 2003 [57]	SC-Cascade	13.4	0.1	0.13	2.4	1.11	24.2
		10.4	1.92	0.13	4.3	0.83	4.0
Tabatabaei 2003 [58]	SC-Cascade	8.5	40	0.13	175	6.04	0.1
Malla 2008 [59]	SC-Cascade	11.4	20	0.09	27.9	0.26	26.0
Paramesh 2006 [60]	SC-Cascade	10.8	20	0.09	78	1.09	4.0
Yu 2005 [61]	SC-Cascade	9.4	2	0.09	2.1	0.78	2.2
		10.7	1		2.1	0.63	6.5
		12.5	0.2		2.1	0.91	15.9
Ahn 2005 [66]	SRC-Cascade	12.8	0.024	0.35	1	2.86	6.3
Zanbaghi 2011 [7]	SC-cascade	12.3	5	0.13	16	0.32	39.4
Asl 2011 [8]	SC-VCO-cascade	12.5	4	0.13	13.8	0.298	51.7
Breems 2004 [6]	CT-Cascade	10.9	10	0.18	122	3.19	1.5
		10.9	20		216	2.83	1.7
Shu 2010 [23]	CT-Cascade	11.0	18	0.18	183	2.48	2.0
Breems 2007 [62]	CT-Cascade	12.5	20	0.09	56	0.24	59.5
Sauerbrey 2010 [63]	CT-Cascade	9.8	15	0.065	10.5	0.39	5.6
		11.3	10		10.5	0.21	30.1
This Work	CT-Cascade	14.2	0.02	0.18	0.264	0.36	126.0

3.7 Summary

In this chapter, a PWM scheme has been proposed to address the important problem of RC time constant variation in cascaded CT DSMs. The application of PWM technique enables the use of a CDS in the CT modulators to boost the effective dc gain of the opamp. A finite opamp GBW compensation technique has also been proposed. These techniques can improve the matching between the analog and digital paths required for the cancellation of first stage's quantization noise. The use of PWM also allows the comparator and the DAC to settle within the PWM "low" time to avoid ELD caused by the comparator and DAC. Although the proposed techniques add switches to the modulator, the added switches are low-voltage-swing ones that can operate from a low supply voltage and virtually do not generate distortion. To prove the concept, a low-voltage CT 2-2 cascaded DSM has been designed and

fabricated in a 0.18-μm CMOS. Experimental results show that with the CDS the SNDR of the modulator is 28 dB higher than that of the same modulator when the CDS is turned off. A drawback of the PWM approach is the degradation of anti-aliasing filtering, which is mitigated by an off-chip capacitor in this implementation.

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CHAPTER 4. A High-Linearity Capacitance to Digital Converter with Techniques Suppressing Charge Injection from Bottom-Plate Switches

This section presents a high-precision capacitance-to-digital converter (CDC) that can be configured to interface with single-ended or differential capacitive sensors. In the conventional CDC, charge injection from bottom-plate switches depends on the digital output and the value of the sensing capacitor. Nonlinearity is resulted especially when the varying ranging of the sensing capacitor is wide. In this chapter, new switching and calibration schemes are proposed to reduce these charge injection. A prototyping 2nd order CDC employing the proposed techniques is fabricated in a 0.18μm CMOS process and achieves a 53.2aFrms resolution in a 0.5ms measuring time. The proposed techniques improve the CDC's linearity from 9.3 to 12.3 bits in the single-ended sensing mode, and from 10.1 to 13.3 bits in the differential sensing mode, with a wide sensing capacitor range from 0.5 to 3.5pF. The CDC is also demonstrated with real-life pressure (single-ended) and acceleration (differential) sensors.

4.1 Introduction

Micro-Electro-Mechanical System (MEMS) capacitive sensors are widely applied due to their high sensitivity, high linearity, low power consumption, and small temperature drift [1]. MEMS sensors can be broadly divided into two categories, namely, single-ended and differential sensors. In single-ended sensors, which are often used for humidity and pressure sensing, the ratio of the sensing capacitor to a

reference capacitor is read. In differential sensors, which are often applied in acceleration and displacement sensing, there are two sensing capacitors built in each device, and their values change in opposite directions in response to the variation of the sensed physical quantity, but the total sum always remains constant. The ratio between one sensor capacitor and their total sum is measured.

To generate digital reading from a MEMS capacitive sensor, a switched-capacitor (SC) capacitance-to-digital converter (CDC) employing oversampling Sigma-Delta modulation technique is widely used [2]-[4][6]. As differential MEMS sensors are more difficult to manufacture and thus more expensive than single-ended MEMS sensors, many recent works on CDCs use single-ended circuits to interface with single-ended MEMS sensors [3]-[6].

In a SC Sigma-Delta CDC, charge injections and clock feed-through via gate-drain overlapping capacitance of the MOSFET switches are major sources of nonlinearity. The widely used bottom-plate sampling technique, which opens the switches near the opamp's virtual ground slightly earlier than those at the other side of the capacitor, can be very effective in removing the charge injection and clock feedthrough errors from the top-plate switches in the SC CDC, as in other SC circuits. However, unlike in other SC circuits, in the SC CDC the charge injection and clock feedthrough errors generated from the bottom-plate switches depend on the digital output of the CDC and the value of the sensing capacitor (to be detailed in Section II). They cannot be treated as an offset, but is a source of nonlinearity, especially when the sensing capacitor has a wide varying range (Ex. for a MEMS pressure sensor, its sensing capacitance can be ranging from 1.7 pF to 3.2 pF with the atmosphere pressure sweeping from 50 kPa~105 kPa). Some calibration techniques have recently been reported to tackle this problem [2]-[6]. However, they achieve limited linearity,

with the reported best one being 12-bit [5]. Furthermore, these CDCs have narrow capacitance ranges [2]-[6].

This chapter presents new switching and calibration schemes to improve the linearity of CDCs. The proposed techniques are applicable to CDCs interfacing with single-ended as well as differential sensors. They are also valid when the sensing capacitor varies widely.

4.2 Proposed CDC Switching and Calibration Schemes

4.2.1 Single-Ended Sensing Mode

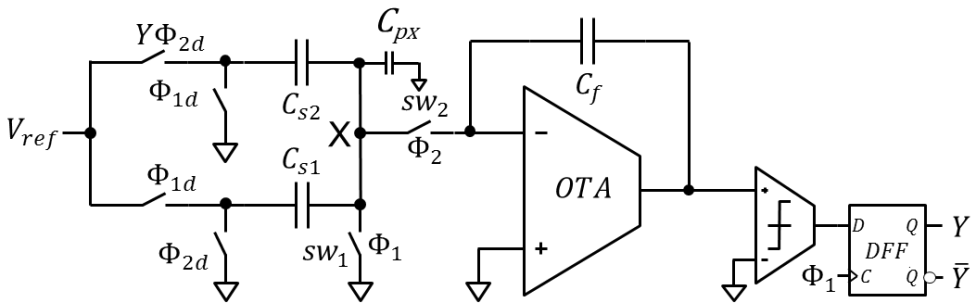


Fig. 4.1 Conventional switching scheme in a first-order CDC interfacing with a single-ended sensor. Φ_1 and Φ_2 are non-overlapping clocks. Φ_{1d} and Φ_{2d} are slightly delayed versions of Φ_1 and Φ_2 respectively.

Fig. 4.1 shows the traditional switching scheme in a first-order CDC interfacing with a single-ended sensor. Here C_{s1} and C_{s2} denote the sensing and reference (fix-valued) capacitors respectively. C_{px} represents the total parasitic capacitance at node X. The CDC employs an oversampling technique and uses logic feedback to balance the charge flows from C_{s1} and C_{s2} to integrating capacitor C_f. The feedback and the integrating function of C_f force the averaged amount of charge from C_{s1} and C_{s2} to C_f to be close to zero. Suppose that the total number of clock cycles is N in a measurement, then the total charge from C_{s1} to C_f is $-NC_{s1}V_{ref}$,

while the charge from C_{s2} is $nC_{s2}V_{ref}$, where *n* is the number of "1"s in the output bit stream Y. Thereby, we have

$$-NC_{s1}V_{ref} + nC_{s2}V_{ref} = 0 \tag{4.1}$$

where n/N is the average value of Y. The ratio of the two capacitors can be obtained from the averaged value of Y (i.e., n/N) :

$$Y_{ave,m} = \frac{n}{N} = \frac{\mathrm{C_{s1}}}{\mathrm{C_{s2}}} \tag{4.2}$$

The main error sources here are charge injection and clock feed-through from the switches due to the single-ended nature of the CDC circuit. The error charges from the switches to the left of $\mathrm{C_{s1}}$ and $\mathrm{C_{s2}}$ can be effectively suppressed by the bottom-plate sampling scheme. However, unlike in other SC circuits, the error charges from switches $\mathrm{sw_1}$ and $\mathrm{sw_2}$ are problematic in this CDC.

Let us consider switch $\mathrm{sw_1}$ only for simplicity. Denote Q_1, Q_2 and Q_{px} as the error charges injected into C_{s1}, C_{s2} and C_{px}, respectively, when $\mathrm{sw_1}$ turns off. From the switching scheme shown in Fig. 4.1, it can be observed that Q_2 is transferred to the integrating capacitor C_f in the next phase (Φ_2) only when Y is "1", while Q_1 and Q_{px} are transferred to C_f in every clock cycle. The charge balancing equation, Eq. (4.1), is now modified as:

$$-NC_{s1}V_{ref} + nC_{s2}V_{ref} + NQ_1 + nQ_2 + NQ_{px} = 0 \tag{4.3}$$

The average of the output Y becomes:

$$Y_{ave,m} = \frac{n}{N} = \frac{\mathrm{C_{s1}}\cdot V_{ref} - Q_1 - Q_{px}}{\mathrm{C_{s2}}\cdot V_{ref} + Q_2} \tag{4.4}$$

Eq. (4.4) shows that the error charges Q_1, Q_2 and Q_{px} affect the output of the CDC in a nonlinear way. There is one more source of nonlinearity. The error charges Q_1, Q_2 and Q_{px} originate from the charge stored in the channel region of $\mathrm{sw_1}$ (realized by a MOS transistor) when it on. A portion of the channel charge is

injection to node X (hold by C_{s1}, C_{s2} and C_{px}), and the rest to the other side of the switch (ground). The channel charges injected to node X (Q_1, Q_2 and Q_{px}) depends on the impedance at node X. When C_{s1} varies in response to the sensed physical quantity, the impedance at node X changes and so does the error charges Q_1, Q_2 and Q_{px}. This makes Q_1, Q_2 and Q_{px} signal-dependent. Large non-linearity is generated especially when C_{s1} varies widely.

For switch sw_2, an phenomenon similar to the one describe by Eq. (4.4) occurs. The charge injection error of this switch also introduces non-linearity. In addition, the charge redistribution at node X caused by the clock feed-through via gate-drain overlapping capacitance of the two switches exhibit similar nonlinear phenomenon of Eq. (4.4).

To suppress these nonlinearities, two measures have been taken in the proposed switching scheme, which is shown in Fig. 4.2. First, a dummy phase $\overline{\mathrm{Y}}\Phi_{2\mathrm{d}}$ is added for sw_3 as shown in Fig. 4.2(a). This extra phase does not affect the function of the CDC but takes effect in reducing non-linearity as will be seen shortly. Second, the sensing process is divided into two steps: measurement and calibration steps. The switching scheme of the calibration step is given in Fig. 4.2(b).

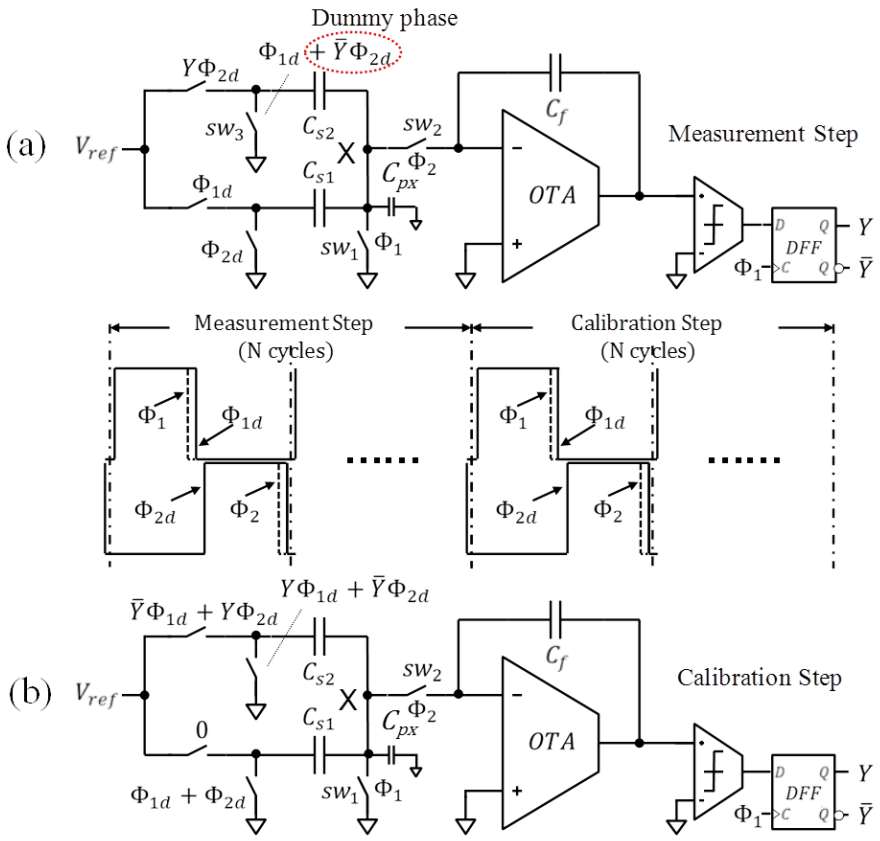


Fig. 4.2 Proposed switching scheme in a first-order CDC interfacing with a single-ended sensor: (a) measurement step; (b) calibration step.

Denote $Q_{s1,m}$, $Q_{s2,m}$ and $Q_{px,m}$ as the error charges injected into C_{s1}, C_{s2} and C_{px}, respectively, from sw_1 when it turns off in the measurement step. From the switching scheme shown in Fig. 4.2(a), it can be observed that with the addition of the dummy phase $\overline{\mathrm{Y}}\Phi_{2\mathrm{d}}$ for sw_3, $Q_{s2,m}$ is transferred to C_f in Φ_2 in every clock cycle, regardless of Y being "1" or "0". The charge balancing equation becomes:

$$-NC_{s1}V_{ref} + nC_{s2}V_{ref} + NQ_{s1,m} + NQ_{s2,m} + NQ_{px,m} = 0 \tag{4.5}$$

The averaged value of Y is:

$$Y_{ave,m} = \frac{n}{N} = \frac{C_{s1}}{C_{s2}} - \frac{Q_{s1,m}+Q_{s2,m}+Q_{px,m}}{C_{s2}\cdot V_{ref}} \tag{4.6}$$

For switch sw_2, similar effects are resulted. From Eq. (4.6), if $Q_{s1,m}$, $Q_{s2,m}$, $Q_{px,m}$ and C_{s2} are constants, they merely lead to an offset in $Y_{ave,m}$. However, as these error charges vary when the sensing capacitor C_{s1} varies for the reason

explained previously, they still introduce nonlinearity. This nonlinearity is cancelled in the calibration step presented below.

Denote $Q_{s1,c}$, $Q_{s2,c}$ and $Q_{px,c}$ as the error charges injected into C_{s1}, C_{s2} and C_{px} respectively from sw_1 when it turns off in the calibration step. From the switching scheme shown in Fig. 4.2(b), no signal charge is injected to C_f in the C_{s1} branch, and charge packets of $+C_{s2}V_{ref}$ and $-C_{s2}V_{ref}$ are transferred to C_f in every clock cycle when Y is "1" and "0" respectively. With $Q_{s1,c}$, $Q_{s2,c}$ and $Q_{px,c}$ taken into account, the charge balancing equation in this step is:

$$nC_{s2}V_{ref} - (N-n)C_{s2}V_{ref} + NQ_{s1.c} + NQ_{s2.c} + NQ_{px,c} = 0 \tag{4.7}$$

The averaged value of Y becomes:

$$Y_{ave,c} = \frac{n}{N} = \frac{1}{2} - \frac{1}{2}\frac{Q_{s1,c}+Q_{s2,c}+Q_{px,c}}{C_{s2}\cdot V_{ref}} \tag{4.8}$$

A close look at the switching schemes in Fig. 4.2(a) and (b) reveals that at every moment when sw_1 or sw_2 turn off (the moment of error charge generation), the settings of the circuit in the measurement and calibration steps are identical. Thereby,

$$Q_{s1,m} = Q_{s1,c},\ Q_{s2,m} = Q_{s2,c} \text{ and } Q_{px,m} = Q_{px,c} \tag{4.9}$$

From Eqs. (4.6), (4.8) and (4.9), the capacitor ratio can be obtained from the averaged outputs in the two steps:

$$\frac{\mathrm{C_{s1}}}{\mathrm{C_{s2}}} = Y_{ave,m} - 2\,Y_{ave,c} + 1 \tag{4.10}$$

The error charges from switch sw_1 (and sw_2) are removed with simple digital operations of addition, subtraction and divide-by-two (a bit shifting).

4.2.2 Differential Sensing Mode

The concept proposed above can also be applied to CDCs interfacing with differential sensors. Fig. 4.3 shows the conventional switching scheme for a CDC

interfacing with a differential sensor. In the circuit of Fig. 4.3, C_{s1} and C_{s2} respond to the sensed quantity simultaneously but in complementary ways so that the sum of their values is fixed. Acceleration and displacement sensors often fall into this category.

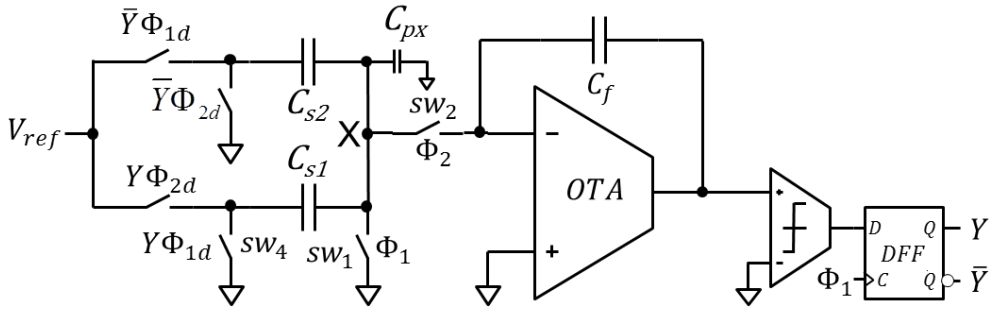


Fig. 4.3 Conventional switching scheme in a first-order CDC interfacing with a differential sensor.

For the CDC in Fig. 4.3, the fact that the net amount of charge flowing into the integrating capacitor C_f is forced to zero by the feedback loop results in:

$$-(N-n)C_{s2}V_{ref} + nC_{s1}V_{ref} = 0 \tag{4.11}$$

Thus,

$$Y_{ave} = \frac{n}{N} = \frac{C_{s2}}{C_{s1}+C_{s2}} \tag{4.12}$$

Now consider charge injection from switch sw_1. Denote Q_1, Q_2 and Q_{px} as the error charges injected into C_{s1}, C_{s2} and C_{px} from sw_1 when it turns off. The charge balancing equation becomes:

$$-(N-n)C_{s2}V_{ref} + nC_{s1}V_{ref} + nQ_1 + (N-n)Q_2 + NQ_{px} = 0 \tag{4.13}$$

The averaged value of Y becomes:

$$Y_{ave} = \frac{n}{N} = \frac{\mathrm{C_{s2}}\cdot V_{ref} - Q_2 - Q_{px}}{\mathrm{C_{s1}}\cdot V_{ref} + \mathrm{C_{s2}}\cdot V_{ref} + Q_1 - Q_2} \tag{4.14}$$

The error charges Q_1, Q_2 and Q_{px} also affect the output of the CDC in a nonlinear way. They can themselves be dependent on the values of the sensing capacitors C_{s1} and C_{s2}, resulting in more nonlinearity.

Fig. 4.4 shows the proposed switching scheme for the CDC interfacing with differential sensors. The capacitance-to-digital conversion is divided into measurement and calibration steps. In the measurement step, dummy clock phases $Y\Phi_{1d} + Y\Phi_{2d}$ and $\bar{Y}\Phi_{1d} + \bar{Y}\Phi_{2d}$ are added for sw_3 and sw_4, respectively, as shown in Fig. 4.4(a).

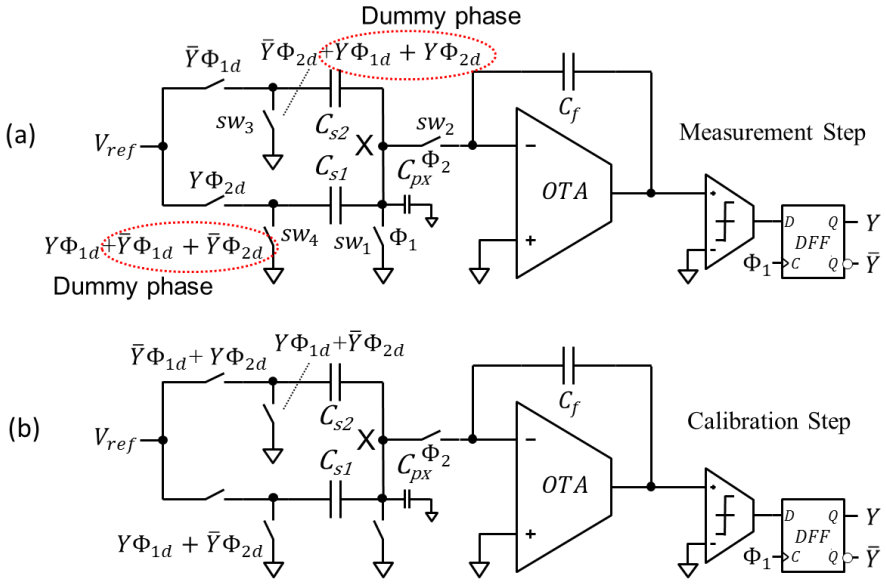


Fig. 4.4 Proposed switching scheme in a first-order CDC interfacing with a differential sensor: (a) measurement step; (b) calibration step.

Denote $Q_{s1,m}$, $Q_{s2,m}$ and $Q_{px,m}$ as the error charges injected into C_{s1}, C_{s2} and C_{px}, respectively from sw_1 when it turns off in the measurement step. From the switching scheme in Fig. 4.4 (a), $Q_{s1,m}$, $Q_{s2,m}$ and $Q_{px,m}$ will always be transferred to C_f in very clock cycle, regardless of Y being "1" or "0". The charge balancing equation is written as:

$$-(N-n)C_{s2}V_{ref} + nC_{s1}V_{ref} + NQ_{s1,m} + NQ_{s2,m} + NQ_{px,m} = 0. \quad (4.15)$$

Thus,

$$Y_{ave,m} = \frac{n}{N} = \frac{C_{s2}}{C_{s1}+C_{s2}} - \frac{Q_{s1,m}+Q_{s2,m}+Q_{px,m}}{(C_{s1}+C_{s2})\cdot V_{ref}} \quad (4.16)$$

From Eq. (4.16), if $Q_{s1,m}$, $Q_{s2,m}$, $Q_{px,m}$ and $C_{s1}+C_{s2}$ are constants, they

merely lead to an offset in $Y_{ave,m}$. However, as these error charges vary when the sensing capacitor C_{s1} varies for the reason explained previously, they still introduce nonlinearity. This nonlinearity is cancelled in the calibration step shown in Fig. 4.4 (b).

It can be derived that the averaged value of Y in the calibration step is:

$$Y_{ave,c} = \frac{1}{2} - \frac{1}{2}\frac{Q_{s1,c}+Q_{s2,c}+Q_{px,c}}{(C_{s1}+C_{s2})\cdot V_{ref}} \tag{4.17}$$

where $Q_{s1,c}$, $Q_{s2,c}$ and $Q_{px,c}$ are error charges injected into C_{s1}, C_{s2} and C_{px} respectively from sw_1 in the calibration step. The circuit settings in the measurement and calibration steps are identical when sw_1 (and sw_2) turns off, so $Q_{s1,m} = Q_{s1,c}$, $Q_{s2,m} = Q_{s2,c}$ and $Q_{px,m} = Q_{px,c}$. The capacitor ratio is calculated as:

$$\frac{C_{s2}}{C_{s1}+C_{s2}} = Y_{ave,m} - 2\,Y_{ave,c} + 1 \tag{4.18}$$

The errors caused by switch sw_1 are removed. The errors caused by switch sw_2 are removed in a similar way.

4.3 Circuit Implementation

A second-order CDC with the proposed switching scheme was designed in a 0.18μm CMOS process. Fig. 4.5 shows its simplified schematic. The clocks operate at 512 kHz and the nominal supply voltage is 1.8V. Capacitors C_{s1} and C_{s2} are off-chip sensing capacitor or reference capacitor. The second integrator stage in the CDC is a bilinear stage [7] without feedback from output Y.

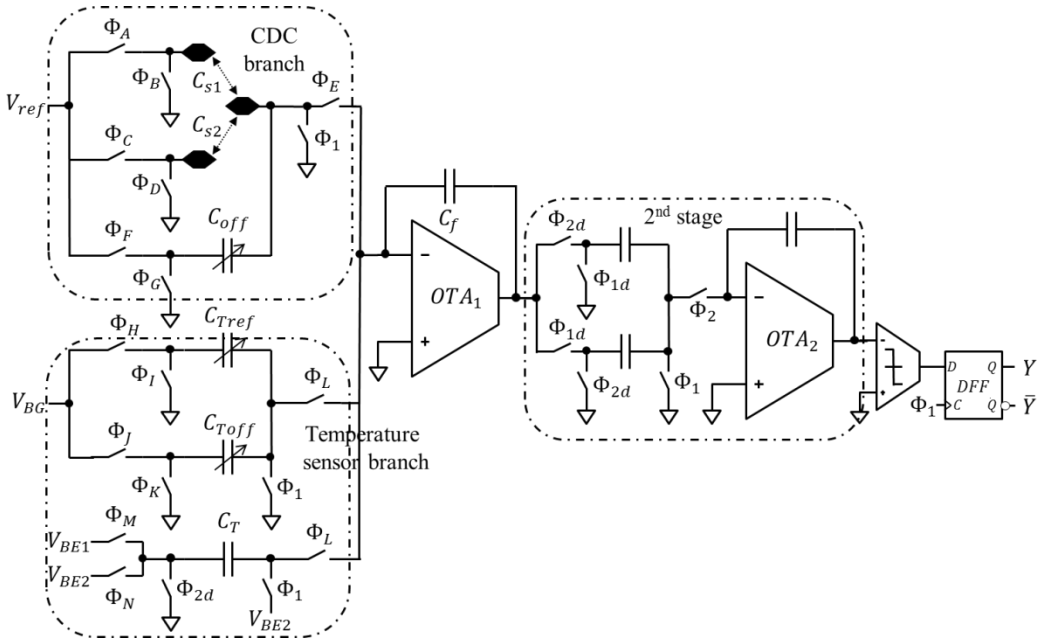


Fig. 4.5 Simplified circuit diagram of the implemented second-order CDC with a temperature input branch. Off-chip sensing/reference capacitors C_{s1} and C_{s2} are shown with their pins only.

In Fig. 4.5, clock phases Φ_A to Φ_E are digitally configurable for interfacing with single-ended or differential sensors. Clock phases Φ_F to Φ_N are also configurable. The upper input branch indicated in the circuit is the main CDC branch, where C_{off} is used for offset tuning in some applications. The lower input branch is a temperature sensing branch, which is included to meet product requirements for sensor temperature compensation in certain applications. The temperature signal comes from a PTAT circuit on the same die. With the clock scheme configured as the single-ended sensing mode, a PTAT voltage ($\Delta V_{BE} = V_{BE1} - V_{BE2}$) is used to charge an internal capacitor (C_T), and a bandgap reference voltage (V_{BG}) is used to charge the offset trimming capacitor and the reference trimming capacitors (C_{Toff} and C_{Tref}). The temperature readout is：

$$D_{Temp} = \frac{\Delta V_{BE} \cdot C_T - V_{BG} \cdot C_{Toff}}{V_{BG} \cdot C_{Tref}} \tag{4.19}$$

Fig. 4.6 shows the schematic of the operational transconductance amplifiers

(OTAs), which are PMOS-input ($M_{1,2}$) two-stage ones with Miller-compensation (R_z and C_m). In the 1st stage, two vertical NPN bipolar ($B_{1,2}$), instead of nMOS, are used to constitute an active current mirror load to decrease $1/f$ noise. Two degeneration resistors ($R_{1,2}$) are in series with NPN transistor's emitter terminal to decrease its transconductance (g_m) or thermal noise. The NPN transistor was fabricated in a triple-well CMOS process with deep Nwell, and its cross section has been shown in Appendix. To mitigate the impacts from $1/f$ noise further, choppers (CH_1 and CH_2) are applied across the first transconductance stage [8][9], the Miller capacitor (C_m) across the 2nd stage can also be taken as a low-pass filter to attenuate the modulated $1/f$ noise portion in high frequency.

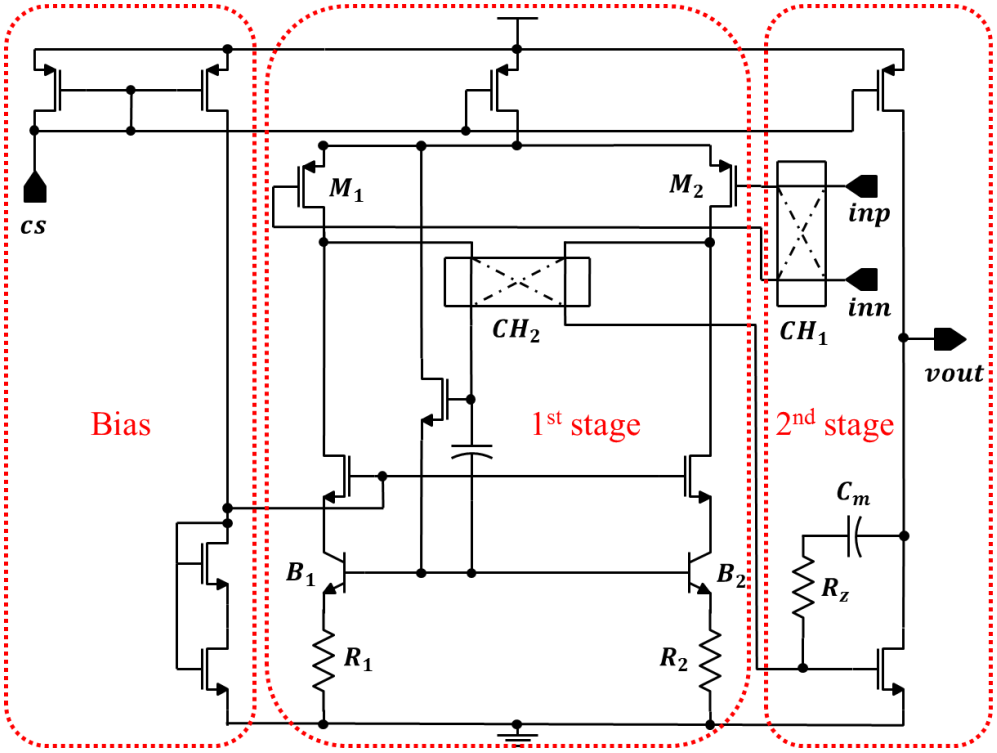


Fig. 4.6 OTA circuit.

Fig. 4.7 depicts the circuit of the comparator (1-bit quantizer), which consists of a CMOS regenerative latch followed by a Set-Reset latch (not shown). The comparator does not consume static current. The regenerative latch [10] is composed of an nMOS flip-flop ($M_{8,9}$) with a pair of nMOS switches ($M_{5,6}$) for strobing and a nMOS switch

(M_7) for resetting, and a pMOS input ($M_{3,4}$) with a pair of pMOS pre-charge switches ($M_{1,2}$). The positive feedback is activated at the end of the integration phase (when Φ_{2d} goes low) in order to make the latch react before the integrators outputs change at the beginning of Φ_1. Again, a D-type flip-flop latches new result Y at the rising edge of Φ_1, which is the feedback to balance the charge flows.

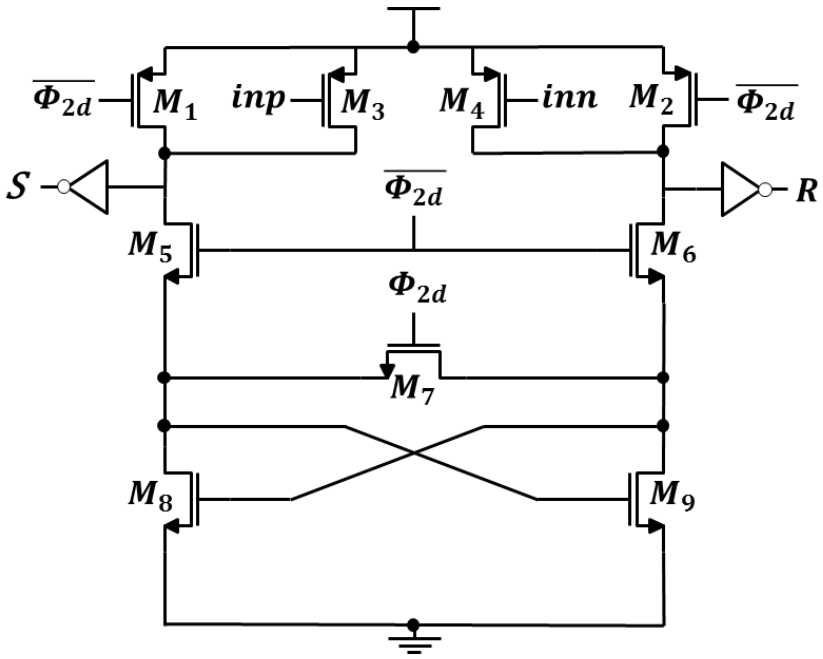


Fig. 4.7 Comparator circuit.

4.4 Measurement Results

Fig. 4.8 shows the micro-photograph of the test chip fabricated in the 0.18μm CMOS process. The active die area is 0.2mm^2. The on-chip capacitors are MIM capacitors. The mode re-configuration logic is implemented on-chip. With a sampling rate of 512 *kHz* and an oversampling ratio of 256, the CDC draws 50μA from a 1.6 to 2.0 V supply. For flexibility, a third-order cascaded integrator-comb (CIC) decimation filter is implemented in a FPGA board that displays the measurement results real time. Six packaged chips were measured and they all perform closely. The testing board and testing setup are shown in Fig. 4.9 and Fig. 4.10 respectively.

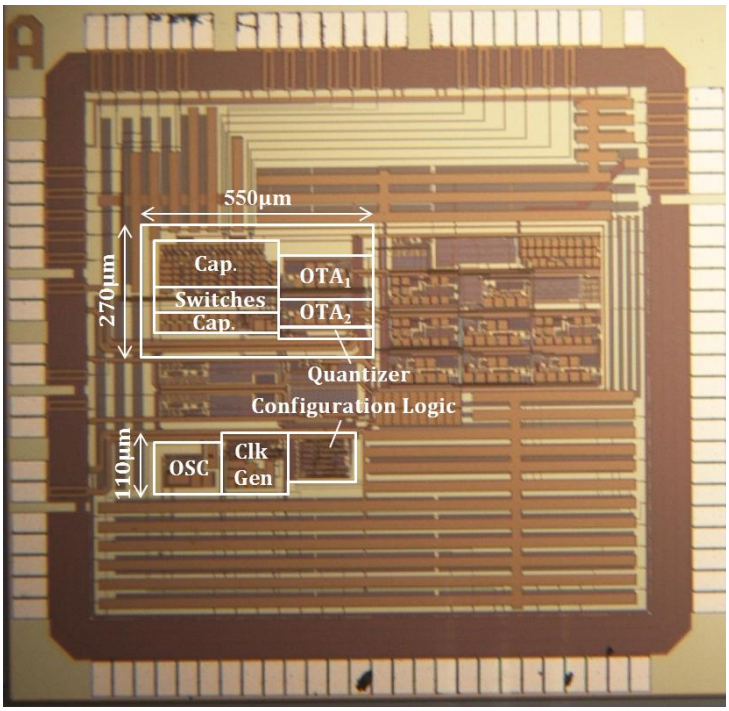


Fig. 4.8 Die photo of the test chip in 0.18µm CMOS.

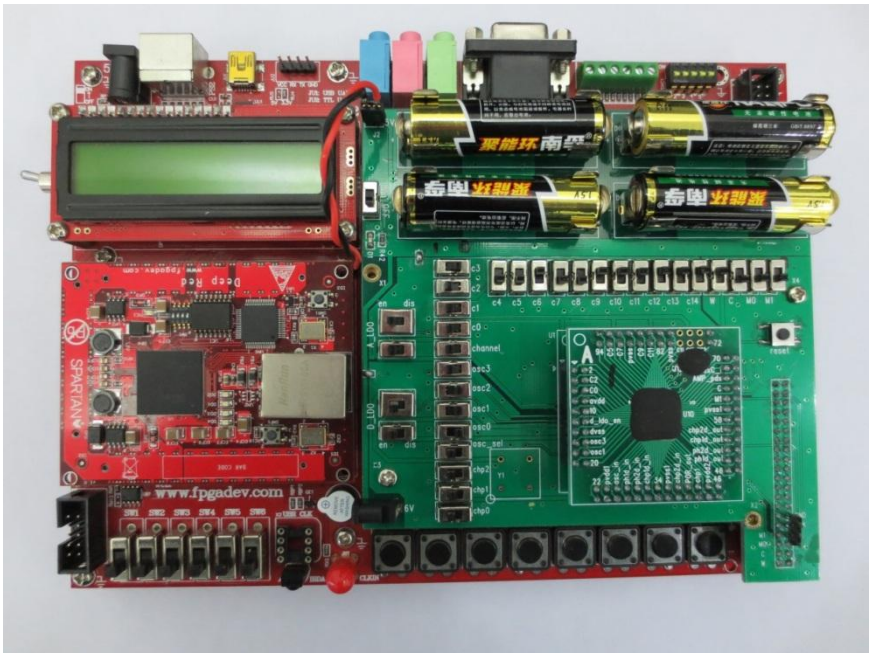


Fig. 4.9 Testing board including a CDC chip and a FPGA board

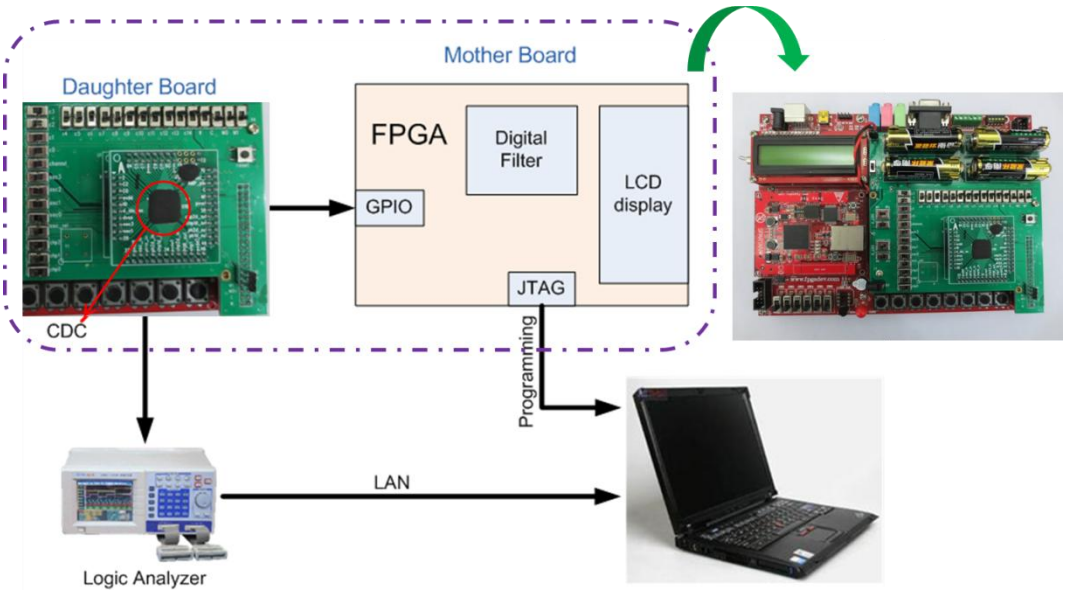


Fig. 4.10 Measurement setup

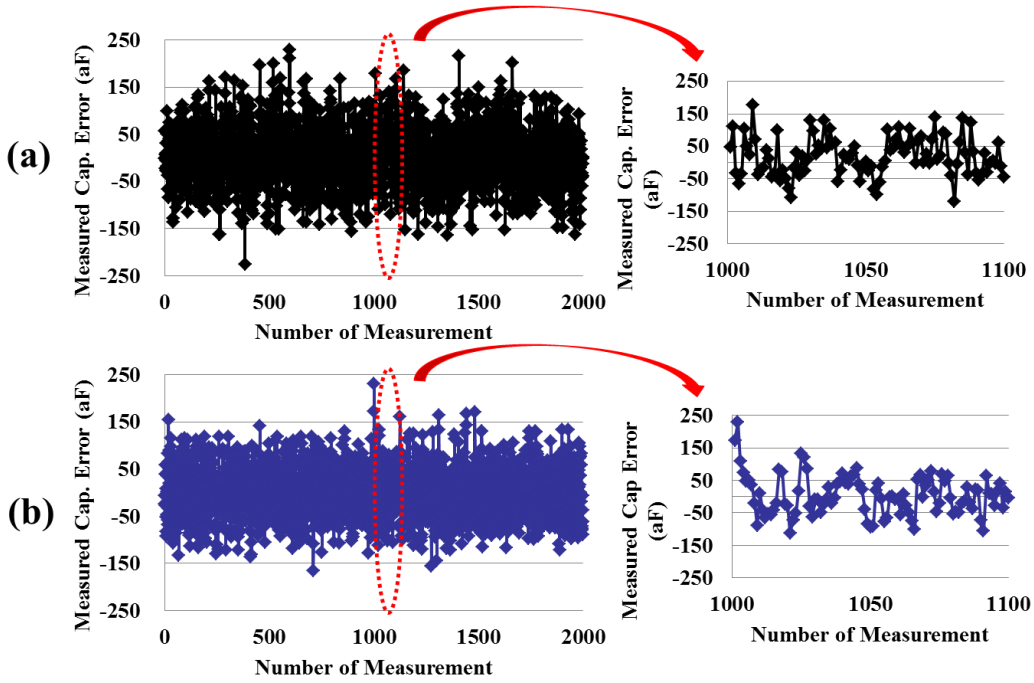


Fig. 4.11 Measured resolution in (a) single-ended sensing mode and (b) differential sensing mode.

Fig. 4.11 shows the capacitance error distribution in a 2000-times measurement. In the single-ended sensing mode, we take $C_{s1} = C_{s2} = 3.5pF$, $C_{off} = 3pF$ and $Y_{ave} = (C_{s1} - C_{off})/C_{s2}$. The measured *rms* capacitor error is 62.5aF$_{rms}$, corresponding to a resolution of 15.8 bit. In the differential sensing mode, we take

$C_{s1} = C_{s2} = 3.5pF$ and $Y_{ave} = C_{s2}/(C_{s1} + C_{s2})$. The measured capacitor error is 53.2aF$_{rms}$, corresponding to a resolution of 16 bit. Fig. 4.12 shows the measured output spectrum respectively.

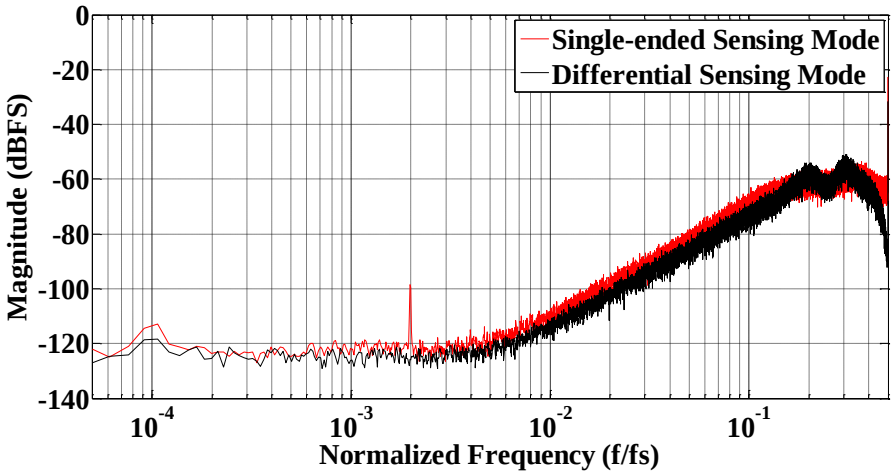


Fig. 4.12 Measured CDC's output spectrum in single-ended and differential sensing modes.

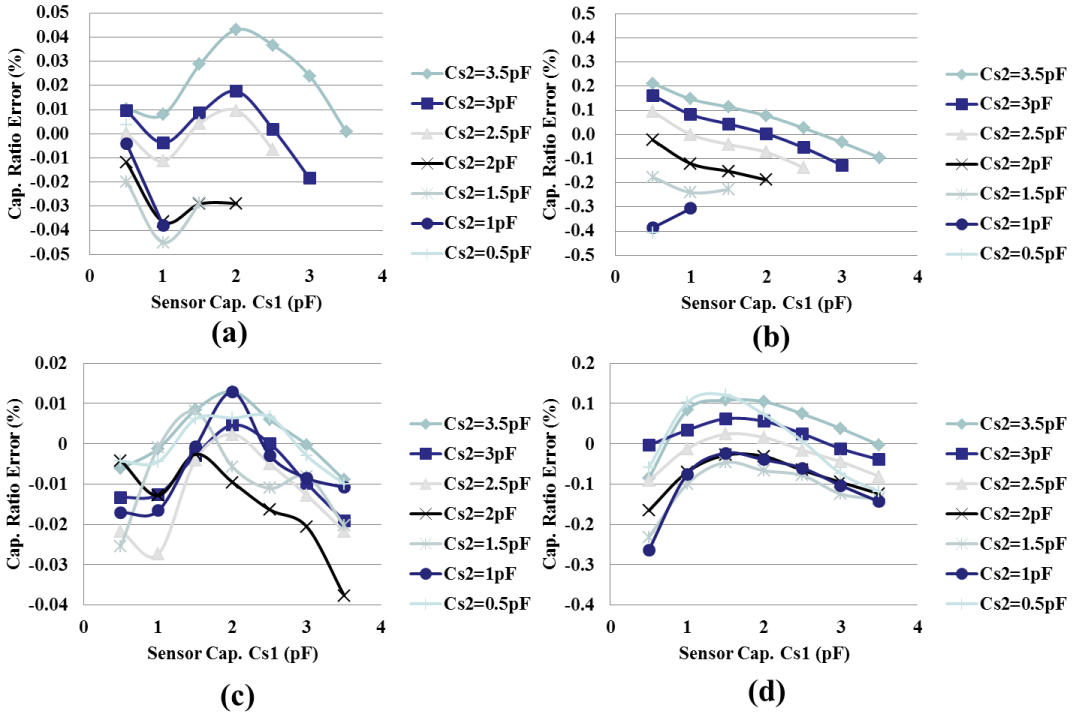


Fig. 4.13 Measured linearity performance: (a) after and (b) before calibration in the single-ended sensing mode; (c) after and (d) before calibration in the differential sensing mode.

To test the linearity (accuracy) of the CDC, two capacitor arrays that can be configured from 0.5pF to 3.5pF are used as the sensing capacitors. The measured

capacitor ratio (Y_{meas}) is fed to a linear fitting algorithm to obtain the ideal capacitor ratio Y_{LFA}. The capacitor ratio error is then calculated as $Err_{abs} = (Y_{meas} - Y_{LFA})/FS \times 100\%$, where FS is the full-scale value. As shown in Fig. 4.13, in the single-ended sensing mode, the *rms* value of Err_{abs} improves from 0.16% to 0.02% when the proposed calibration technique is applied. In other words, the linearity is improved from 9.3 to 12.3 bits. In the differential sensing mode, the *rms* value of Err_{abs} improves from 0.09% to 0.01%, or equivalently, the linearity improves from 10.1 to 13.3 bits, after calibration.

When configured as a temperature sensor, the CDC measures an inaccuracy of –0.5°C/0.6°C over –20°C to 125°C range using second-order three-point (0°C, 38°C and 100°C) calibration, and an inaccuracy of –0.65°C/0.65°C using 1st order two-point (0°C and 85°C) calibration, as shown in Fig. 4.14.

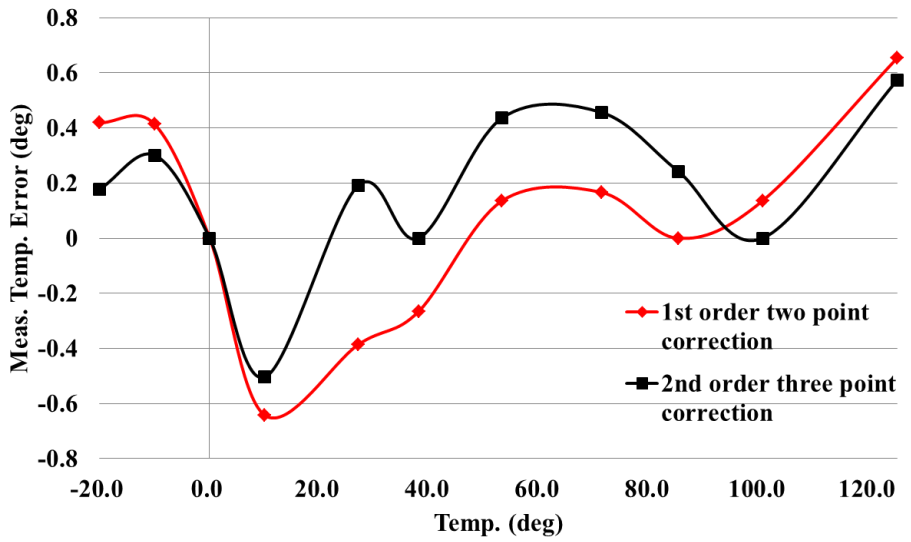


Fig. 4.14 Measured temperature inaccuracy when the CDC is configured as a temperature sensor.

To demonstrate this CDC in field applications, measurements with two real life sensors have been conducted. For the single-ended sensing mode, a pressure sensor with the proposed CDC has been measured in a pressure vessel (see Fig. 4.15). As

shown in Fig. 4.16, the measured sensing capacitance ranges from 1.7 pF to 3.2 pF with the pressure sweeping from 50 kPa~105 kPa. The nonlinearity shown in the figure is due to the inherent characteristic of sensor. For the differential sensing mode, a 3.2 fF/g sensitivity accelerometer with the proposed CDC has been collided with a pillow to mimic the automotive air bag application(see Fig. 4.17). Fig. 4.18 shows that its acceleration can reach over 10 g (9.8 m^2/s) in the moment of collision. These measurement results are in good agreement with these sensors' characteristics.

Fig. 4.15 The pressure vessel for pressure sensor testing

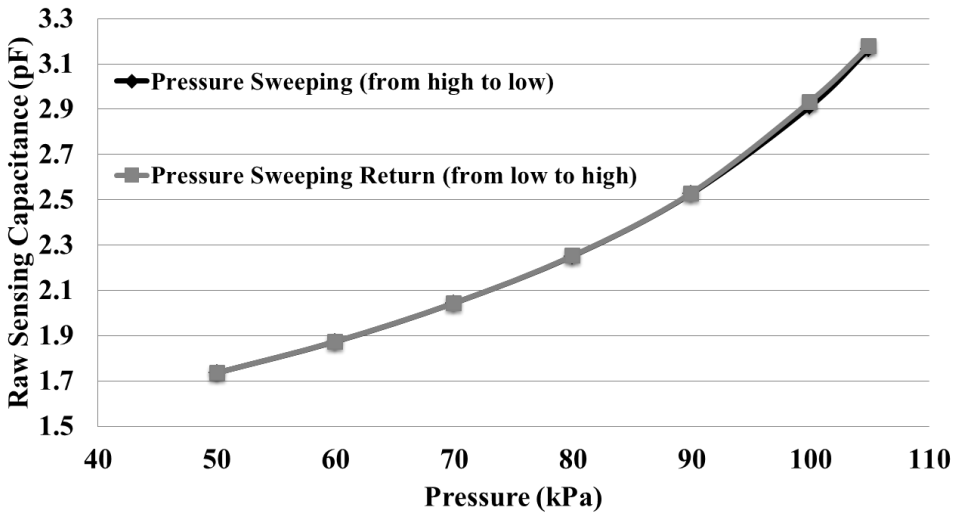


Fig. 4.16 Measured sensing capacitance for a pressure sensor with the pressure sweeping from 50 kPa to 105 kPa

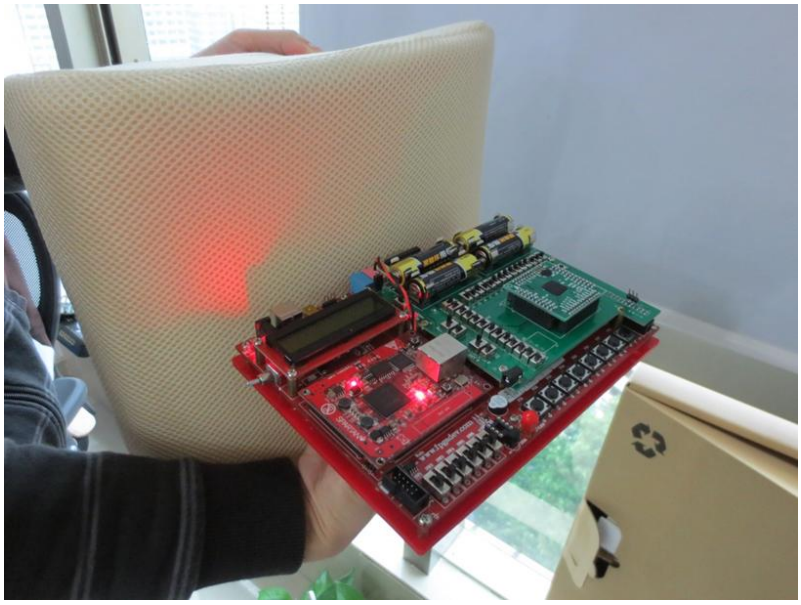


Fig. 4.17 The CDC collided with a pillow to mimic the automotive air bag application

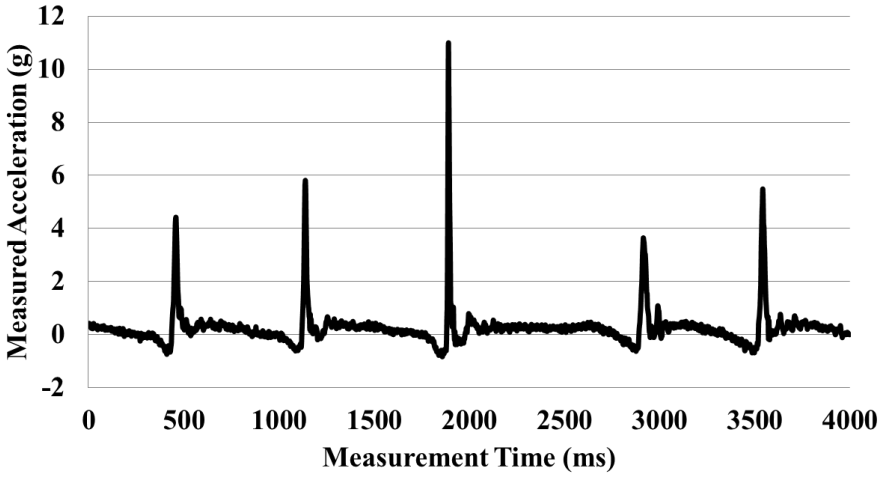


Fig. 4.18 Measured acceleration of an accelerometer when collided with a pillow to mimic the automotive air bag application

Table VII Performance summary and comparison.

CDC	[2]	[3]	[4]	[5]	[6]	This Work	This Work
Cap. Meas. Mode	S.E.S.①	S.E.S.	S.E.S.	S.E.S.	S.E.S.	D.S.②	S.E.S.
Circuit Topology	F.D.C. ΔΣM③	S.E.C. ΔΣM④	P.F.D.C. ΔΣM⑤	P.M.⑥	P.F.D.C .ΔΣM	S.E.C. ΔΣM	S.E.C. ΔΣM
Abs. Cap. Resolution (aFrms)	70	490	65	-	-	53.2	62.4
Cap. Range (pF)	0.8±0.26	±0.5	10±1.6	6.8	-	0.5~3.5	0.5~3.5
Meas. Time (ms)	0.8	0.128	0.02	7.6	0.025	0.5	0.5
Rel. Cap. Resolution (bits)	12.5	10.2	17.2	15	13	16	15.8
Power (μW)	10.3	1440	15000	211	828	80	80
Linearity (bits)	-	10.5	-	12	-	13.3	12.3
FOM⑦ (pJ/step)	1.4	157	1.95	49	2	0.6	0.7

①S.E.S.: Single-Ended Sensing Mode
②D.S.: Differential Sensing Mode
③F.D.C. ΔΣM: Fully-Differential Circuit ΔΣM
④S.E.C. ΔΣM: Single-Ended Circuit ΔΣM
⑤P.F.D.C. ΔΣM: Pseudo-Fully-Differential Circuit ΔΣM
⑥P.M.: Period Modulation

⑦FoM is defined [3] as $\mathrm{FoM} = \frac{\mathrm{Power} \times \mathrm{T}_{\mathrm{conversion}}}{2^{\mathrm{Resolution}}}$, where $\mathrm{Resolution} = \log_2\left(\frac{\text{Sensor Capacitance}}{\text{Absolute Capacitance Resolution}}\right)$

A performance summary and a comparison with other state-of-the-art capacitive sensor interfaces are shown in Table VII. In [3] fabricated in a 0.35 um CMOS process and at a 3.3-V supply, a charge-mode digital-to-analog converter and a successive approximation register are utilized to automatically calibrate the zero point of the interface circuit, which adds hardware complexity and degrades the energy efficiency. A pseudo-fully-differential topology is built with a replica capacitive input network in [4] to increase its robustness to charge-injection errors. However, it does not work for a large sensing capacitor range, as the replica capacitor used to cancel the charge-injection errors is fixed. In [5], a period-modulation-based interface converts the sensor capacitance to a time interval. The auto-calibration algorithm including three consecutive measurements and division operation also needs large additional hardware cost. Besides, a generic sensor interface chip proposed in [6], it contains capacitance-to-voltage converters, a SC amplifier and a CT ΔΣM. Transforming the

sensing capacitor value by an intermediate step in the voltage domain, the circuit complexity is large with 9.3mm^2 on 0.5μm CMOS process.

The figure-of-merit (FoM) normalizes the energy consumption to the resolution, and is calculated as [4]:

$$\text{FoM} = \frac{Power \times T_{conversion}}{2^{Resolution}} \tag{4.20}$$

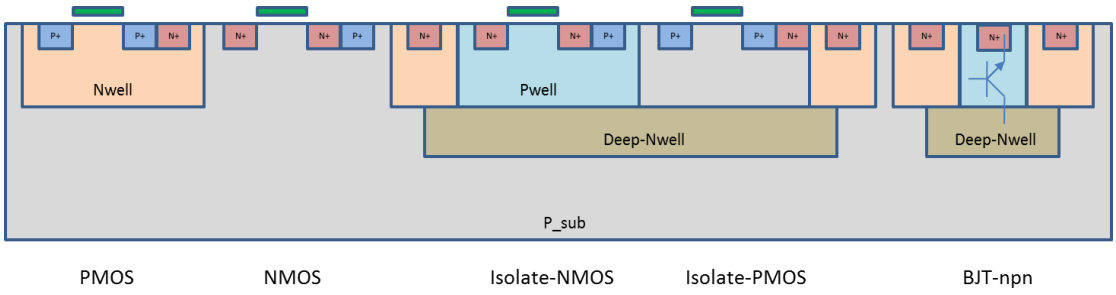
where $$\text{Resolution} = \log_2\left(\frac{Sensor\ Capacitance}{Absolute\ Capacitance\ Resolution}\right) \tag{4.21}$$

It is seen that the proposed CDC has the best energy efficiency (0.6pJ/step), the highest linearity.

4.5 Conclusion

A high-precision capacitive sensor interface that can be configured for interfacing with single-ended or differential sensors has been presented in this chapter. Enabled by new switching and calibration schemes on the single-ended circuit implementation, the switch charge injection is effectively cancelled. Measurement results show this 0.18μm CMOS CDC supports a wide sensing capacitor range from 0.5pF to 3.5pF and achieves a 53.2aFrms resolution in 0.5ms measuring time for both sensing mode. Measurement results show that the proposed switching and calibration schemes improved the CDC's linearity from 9.3 to 12.3 bits in the single-ended sensing mode, and from 10.1 to 13.3 bits in the differential sensing mode, both with the wide sensing capacitor range from 0.5 to 3.5pF.

APPENDIX: The cross section of NPN transistor in triple-well CMOS process



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CHAPTER 5. Conclusions and future works

5.1 Conclusions

A number of performance enhancement techniques for ΔΣ ADCs for telecom, audio and sensing applications have been presented in this thesis. To summarize, the thesis made the following original contributions:

First, the I/Q channel mismatch problem in SC QBDSM for telecom application has been thoroughly analyzed and two novel schemes to suppress the effects caused by these mismatches, including the corruption of the received signal by the image signal, the self-image, and the quantization noise from the image frequencies. The measurement results of a prototype SC QBDSM fabricated in a 0.18μm CMOS show that the proposed techniques improve the image rejection ratio to 73 dB, being the best ever reported. It also eliminates the self-image and quantization noise from the image frequencies. Meanwhile, it also reduces silicon area by I/Q channel multiplexing for the OpAmps, quantizers, and DACs.

Second, a pulse-width-modulation (PWM) technique is proposed for on-chip automatic RC time constant tuning for cascaded continuous-time (CT) DSMs for audio application. The application of PWM technique further enables the use of the CDS in the CT modulator to boost the effective dc gain of the opamp. A finite opamp GBW compensation technique, also enabled by the adoption of the PWM, has been proposed so that opamps with low GBW can be used for power saving. A simple

active RC filter is merged into the modulator to compensate for the degraded anti-aliasing capability caused by the adoption of PWM. Measurement results on a prototype CT 2-2 cascaded DSM in a 0.18-μm CMOS show that these techniques can improve the DR, SNDR, SNR and SFDR of the modulator by at least 28 dB.

Finally, precision techniques for capacitive sensor interface employing ΔΣ modulation have been presented. A prototyping 2nd order CDC employing the proposed techniques has been fabricated in a 0.18-μm CMOS process and achieves a 53.2aFrms resolution in a 0.5ms measuring time. The proposed techniques improve the CDC's linearity from 9.3 bits to 12.3 bits in the single-ended sensing mode, and from 10.1 bits to 13.3 bits in the differential sensing mode, with a wide sensing capacitor range from 0.5 to 3.5pF.

5.2 Future works

There are many interesting topics for further research inspired by the work described in this thesis.

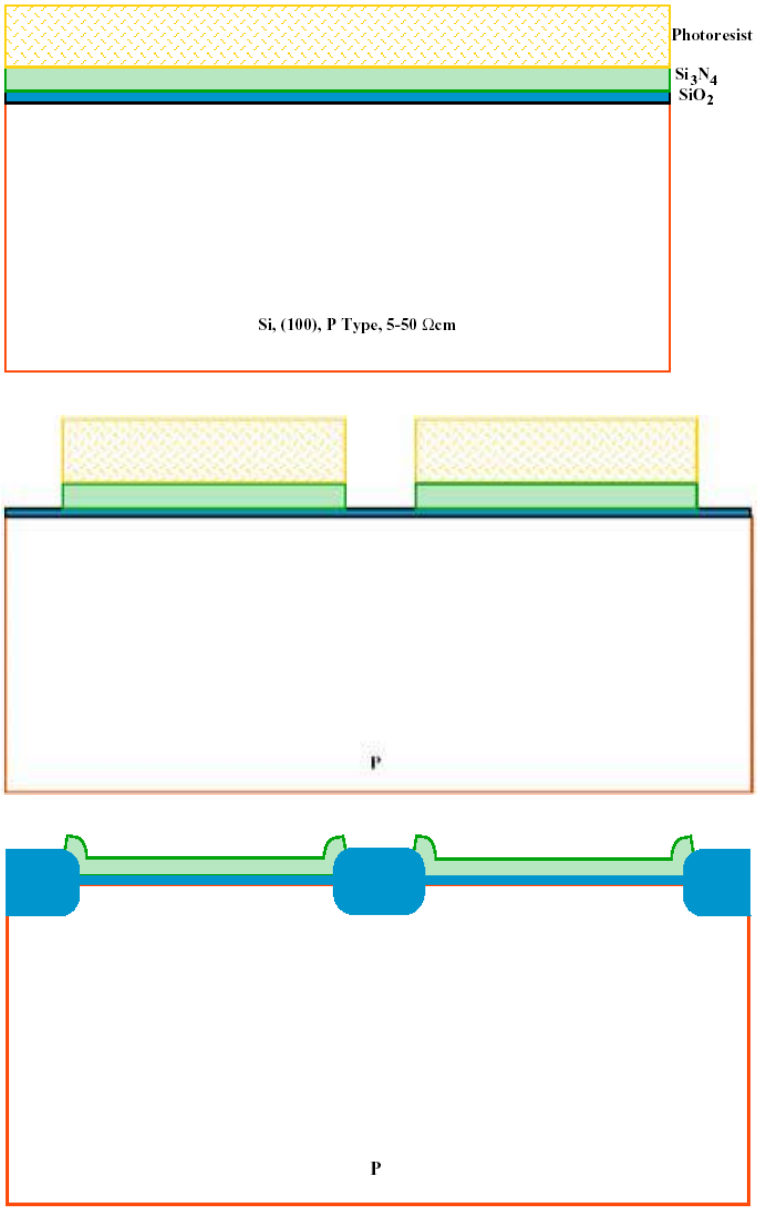
(1) We have proposed two novel schemes to deal with the I/Q channel mismatch problem in SC QBDSM, the next step can be to transplant these techniques in CT QBDSM.

(2) For the CT 2-2 cascaded DSM for audio application, further power reduction should be explored.

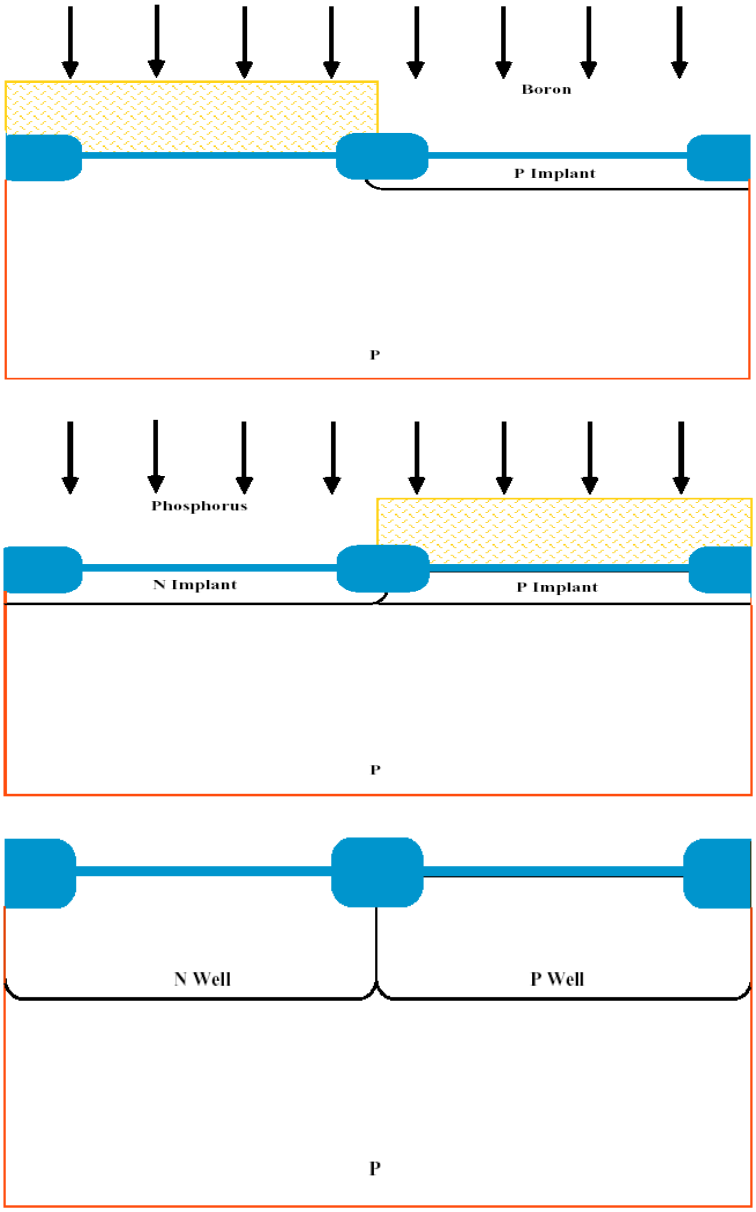
(3) For the high-precision capacitive sensor interface, time-to-digital technique can be a good attempt to cover even wider capacitance range.

APPENDIX: A typical CMOS fabrication process flow (1 poly/2 M, twin well CMOS)

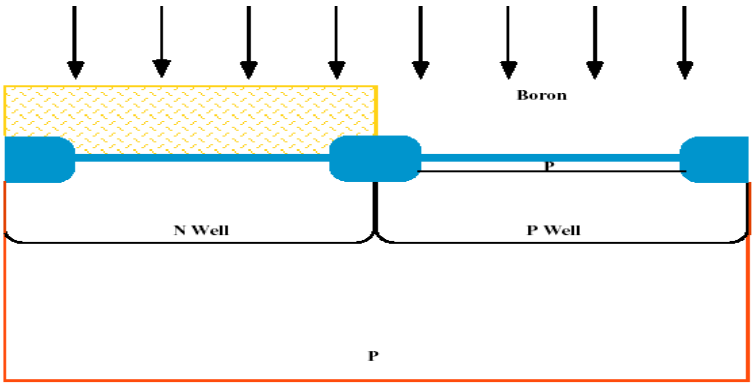
1. Device active area definition by LOCOS isolation

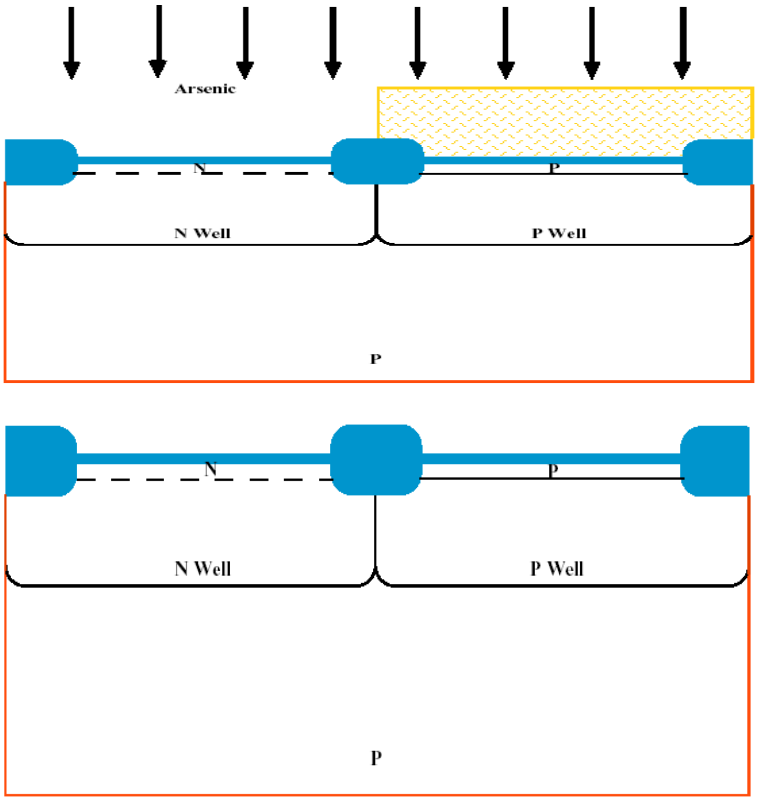


2. Twin well formation

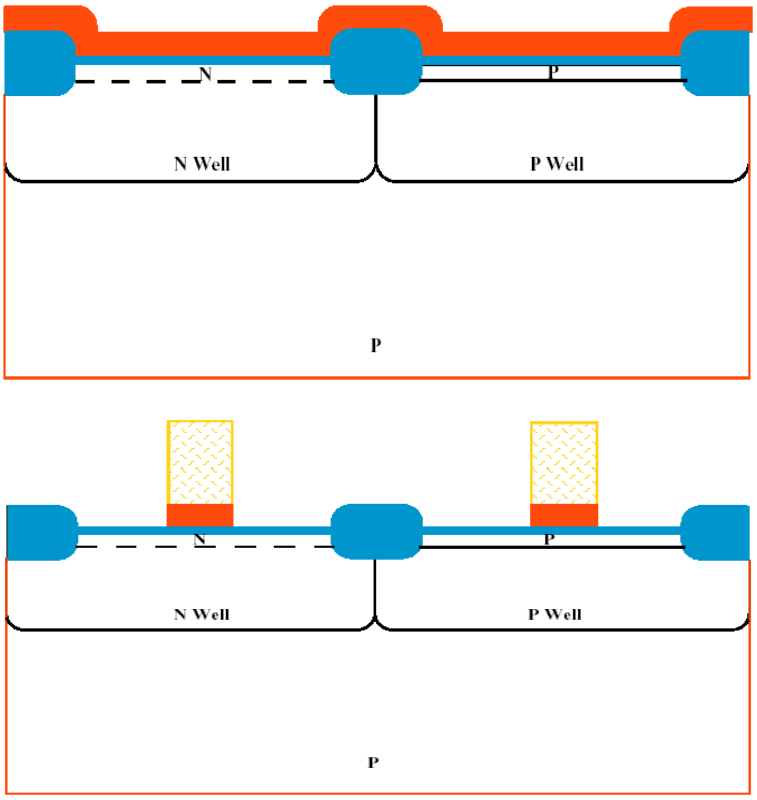


3. MOSFET threshold voltage (VTH) adjust implant

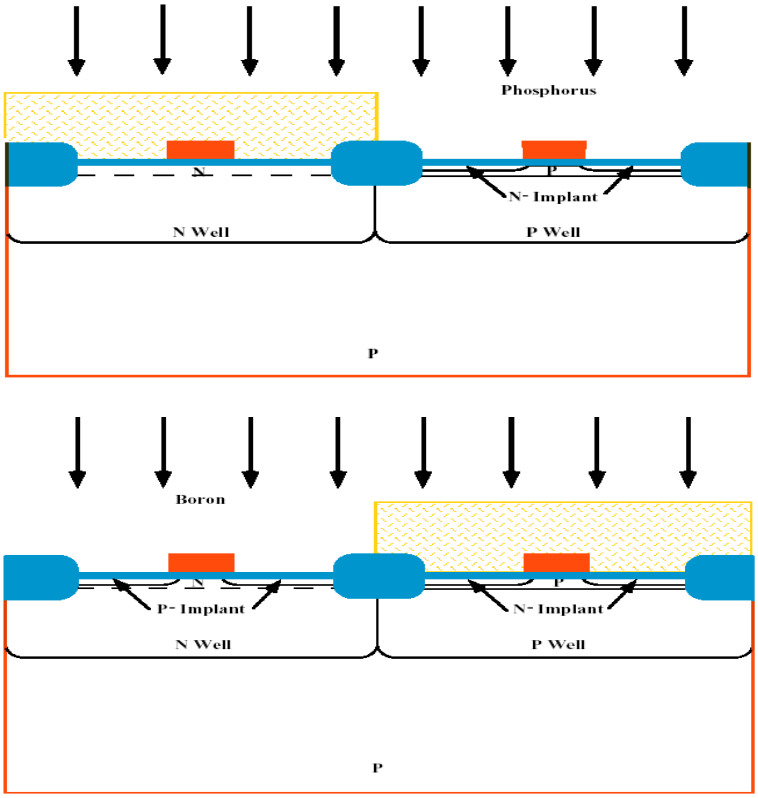




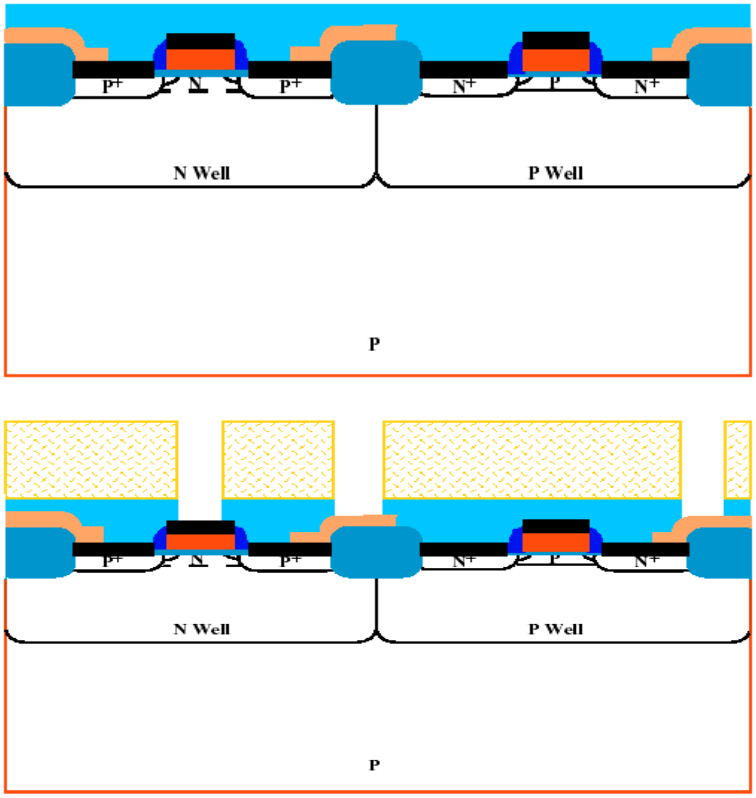
4. Gate oxide and poly-Si gate process

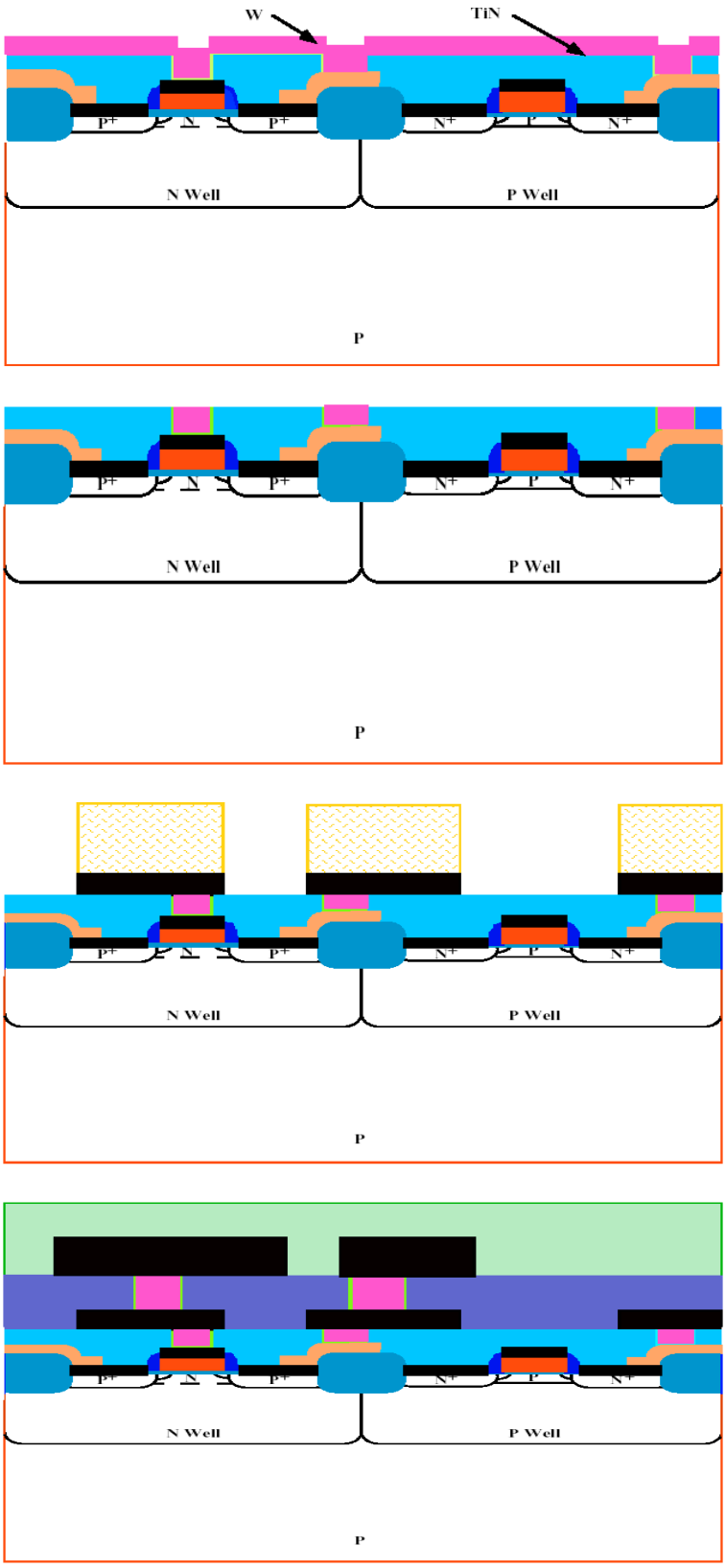


5. Self-aligned S/D formation



6. Multi-level interconnection

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