DESIGN OF DIGITALLY ASSISTED ADAPTIVE ANALOG AND RF CIRCUITS AND SYSTEMS

A Doctoral Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
Atlanta, GA 30332

December 2013

DESIGN OF DIGITALLY ASSISTED ADAPTIVE ANALOG AND RF CIRCUITS AND SYSTEMS

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Dedicated to my parents…

ACKNOWLEDGEMENTS

First and foremost, I would like to express my heartfelt gratitude to my advisor Professor Abhijit Chatterjee for his outstanding guidance, support and encouragement. This thesis would not have been possible without his vision and brilliance. I am thankful to Dr. Hua Wang, Dr. David Keezer, Dr. Alenka Zajic and Dr. Satish Kumar for their valuable suggestions as committee members of my PhD defense.

I would like to acknowledge the support from Gigascale Systems Research Center (GSRC), National Science Foundation (NSF) and Samsung during various stages of my graduate study in Georgia Tech. I am grateful for the support and encouragement from IEEE Microwave Theory and Techniques Society and IEEE Circuits and Systems Society from whom I received Graduate Fellowship Award and Student Travel Award respectively.

Special thanks are due to my friends and colleagues in my research lab who made this journey a memorable one. I would like to thank Hyun Choi, Vishwanath Natarajan, Shreyas Sen, Sehun Kook, Shyam Devarakond, Jayaram Natarajan, Josh Wells, Debesh Bhatta, Debashis Banerjee, Xian Wang, Nicholas Tzou, Thomas Moon, Sen-Wen Hsiao, Sabyasachi Deyati, Barry Muldrey and Suvadeep Banerjee for their wonderful company. I am also grateful to the seniors of our lab – Soumendu Bhattacharya and Ganesh Srinivasan, for providing valuable technical help from industry.

I feel lucky to have the opportunity to collaborate with Prof. Azad Naeemi and to learn from the courses that I have taken at Georgia Tech. I would like to thank Fernando Mujica, Arthur Redfern and Lei Ding for my wonderful experience during two internships in Texas Instruments, Dallas and all my talented colleagues in Kilby Labs and Systems and Applications R&D Center for their help.

I would like to express my deepest gratitude to my parents – Krishna Banerjee and Ashis Banerjee. Nothing of this would ever have been possible without their encouragements, unconditional love and constant support.

Finally, I am thankful to all my friends who made my stay in Atlanta and Dallas enjoyable – Debrup, Parag, Ashish, Ayan, Piu, Tapobrata, Saikat, Payel, Padmanava, Arup, Rita, Nand, Neha, Arindam Basu, Arindam Khan, Sourav, Anshuman, Abhishek, Monodeep, Sandeep, Swarnava, Arkadeep, Ananda, Tonmoy, Atri, Lipilekha, Prabir, Prateeti, Subho, Proma, Kousik, Priya, Ravi, Rimi and Samit.

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SUMMARY

The objective of the proposed research is to design adaptive analog/RF circuits and systems with digital enhancement techniques for higher performance, better process variation tolerance, and more reliable operation and developing strategy for testing the proposed adaptive systems.

A new design paradigm is emerging toward digitally assisted analog and RF circuits and systems aiming to leverage digital correction and calibration techniques to improve the analog and RF performance. With more and more integration of analog and RF circuits in the scaled CMOS technologies, it is becoming increasingly difficult to exert sufficient control on process variations to ensure proper functionality and performance of analog and RF systems. Calibration and tuning circuits are often needed to detect and compensate for the resulting manufacturing imperfections. This type of tuning requires design of adaptive RF components that allow the performance of the device to be traded off against power consumption with the help of proper adaptation algorithms. Additionally, similar adaptation framework is also necessary to allow the analog and RF systems to adapt to changing workloads and environment to minimize power consumption. These challenges create a pressing need for design of adaptive analog and RF circuits and systems that exploit the availability of large numbers of inexpensive on-chip digital circuits to enhance the RF performance that can match or exceed that of traditional RF circuits.

A more revolutionary trend is the new digital friendly topological and architectural transformations of RF circuits. To maintain the reliability of deeply scaled CMOS devices, supply voltage is being reduced which decreases the voltage headroom and makes it difficult to process the analog information in voltage domain in the presence of noise. On the other hand, as the transistors are becoming faster improving the time

resolution of the edge transition of the digital signal, it is becoming easier to encode and process the analog information in the time domain. These observations are causing analog/RF designers to move away from traditional RF circuits and investigate digitally intensive architectures that rely on ultra-fast deeply scaled MOS devices.

In this research, digital friendly and performance tunable analog and RF circuits and systems are designed and adaptation algorithms are developed that allow calibration to mitigate process variation effects, adaptation for improving performance and reliability, and offer a high level of integration with the help of fast, small, high density, and low power digital signal processing. An adaptation framework is developed for process variation tolerant RF systems. This adaptation framework has two parts – optimized test stimulus driven diagnosis of individual modules and power optimal system level tuning. Another direct tuning approach is developed and demonstrated on a carbon nanotube based analog circuit. An adaptive switched mode power amplifier is designed which is more digital-intensive in nature and has higher efficiency, improved reliability and better process resiliency. Finally, a testing strategy for adaptive systems is shown which reduces test time and test cost compared to traditional testing. The research presented in this thesis targets to enable the development of robust, ultra-low power, intelligent, and flexible RF communication systems of the future.

CHAPTER 1

INTRODUCTION

The objective of the proposed research is to design adaptive analog/RF circuits and systems with digital enhancement techniques for higher performance, better process variation tolerance, and more reliable operation and developing strategy for testing the proposed adaptive systems.

1.1. Origin and History of the Problem

With the advancement of CMOS process technology, number of transistors in an integrated circuit doubles every 18-24 months following the Moore's Law. Also the speed of operation of the transistors improves proportionately with the scaling of feature size. This implies faster digital processing and integration of more digital functions in the same chip area. But analog and RF circuit designers did not enjoy the benefits of transistor scaling as much as digital circuits mainly because of imperfections coming from process variation, nonlinearity and mismatch in advanced technology nodes. In the nanometer regime, controllability of the fabrication process has reduced significantly resulting in variability in the devices and hence it became difficult to meet the performance requirement in the presence of process variation.

Recently, more and more research have been focusing on integrating digital baseband with analog and RF front ends on the same radio chip in order to reduce the total solution cost. In an integrated system-on-chip (SoC) solution, efficient digital signal processing resources available on chip can be used to improve the performance of analog and RF circuits and compensate the effects of process variation. This possibility opens up a new paradigm of digitally assisted and enhanced analog and RF circuits and systems

design. Instead of traditional static design of analog and RF circuits which are amenable to performance degradation due to process variation, they are being designed with adaption settings or tuning knobs which allows them to trade-off performance with power consumption. These tuning knobs can be used not only to counter the adverse effects of process variation, but also to dynamically adapt the system to changing environment, to use the flexible system for different standards (software defined radio) and to compensate temporal effects such as aging. During adaptation, the baseband unit detects the quality of the process from the results of built-in tests applied to the system or senses the environment through channel estimation and other metrics using algorithms running on the baseband processor. This, in turn, is used to actuate control procedures implemented in the baseband unit that sets the values of the tuning knobs in an iterative manner until performance convergence is achieved and eventually improvement is obtained in performance, process resiliency and reliability.

1.2. Prior Work in Digitally Assisted Adaptive Analog / RF

This section summarizes the research people have done so far in the domain of digitally assisted adaptive analog and RF circuits and systems. Module level and system level adaptation in analog-RF circuits are explained and then new digital intensive architectures of RF systems are discussed.

1.2.1. Digitally assisted power amplifier (PA)

The job of the power amplifier is to amplify the modulated RF signal to meet the requirement of transmission power in a wireless transmitter. Typical examples of digital assistance in RF power amplifiers are predistortion and peak to average power ratio (PAPR) reduction that improve linearity and efficiency of power amplifiers [1], [2]. Recently digital enhancement techniques have been applied to power amplifiers to nullify

process variation effects (self-healing). An integrated mm-wave self-healing power amplifier is proposed in [3] and [4] that can adapt to mitigate the effects of process variation, modeling inaccuracies, load mismatch and catastrophic failures with the help of integrated sensors, actuators and digital ASIC running the healing algorithm. Another 60 GHz self-healing power amplifier is designed in 65 nm CMOS with adaptive feedback bias control that improves linearity and increases yield [5]. Design of an integrated power amplifier in 90 nm CMOS is presented in [6] where a varactor based digital calibration technique improves the efficiency by a factor of 2.8. Adaptive baseband companding and bias control of the power amplifier using cannel quality information are proposed in [7] that lead to significant power saving compared to traditional PAs. In [8], the authors propose a digitally assisted dual-switch envelope amplifier for a wideband envelope-tracking power amplifier, where a digital signal processing algorithm and analog hysteretic feedback are used to control high efficiency switchers and reduce power consumption. A digitally assisted feed-forward compensation technique that enhances the bandwidth and linearity of a Cartesian-feedback power amplifier is presented in [9].

1.2.2. Digitally assisted mixer

In an RF transceiver, the mixer performs the operation of up-conversion of the baseband signal to the carrier frequency or down-conversion of the received modulated signal. A self-healing image reject mixer, that runs the healing algorithm in the baseband processor and mitigates the effects of process variation, environmental changes and aging, is proposed in [10]. Different performance parameters, such as image rejection ratio, conversion gain and 1 dB compression point, are tuned through control elements such as bias currents and control voltages of the VGA. An adaptive IIP2 calibration technique, that uses digital signal processing to cancel second order intermodulation distortion in RF down-conversion mixer, is reported in [11].

1.2.3. Digitally assisted low noise amplifier (LNA)

The purpose of the low noise amplifier in a wireless receiver system is to amplify the received signal to acceptable level with minimum noise addition. An adaptive LNA is presented in [12] where orthogonal tuning knobs are introduced that can control different performance parameters independently. Another self-healing LNA with bias control is designed in SiGe HBT technology where process variation is detected with the help of a source measure unit [13]. A regression based post-manufacture tuning technique for process variation tolerance is developed in [14] and applied to a CMOS LNA.

1.2.4. Digitally assisted analog-to-digital converter (ADC)

Analog-to-digital converter is a critical block in an RF receiver which digitizes the received signal after being down-converted by the mixer. In [15], the author explains the trade-off between power consumption in an ADC and its speed and precision. He shows how matching and linearity of the components can be improved using digital processing techniques that ultimately lead to lower power consumption. Finally an example of digitally assisted pipelined ADC is shown that achieve a very low power operation using simplified weakly nonlinear amplifiers which are calibrated through polynomial correction functions as calculated by a least means square algorithm. In [16], the authors propose an environment adaptive delta-sigma analog to digital converter where spectrum sensing is performed dynamically and modulator order is reconfigured depending on the signal and blocker power ratio.

1.2.5. Digitally assisted phase-locked loop and frequency synthesizer

Frequency synthesizers are used to generate very precise RF local oscillator signal. A self-healing CMOS frequency synthesizer is presented in [17] where on-chip spurious tone detection and correction techniques are applied. In [18], phase noise cancellation technique is shown for a CMOS delta-sigma fractional-N phase locked loop (PLL). A dual loop PLL with self-calibration technique is proposed in [19] which

desensitizes the PLL's small signal transfer function to gain variations of the non-linear components.

1.2.6. System-level adaptation in transceiver

Research efforts in digitally assisted system level adaptation of the transceiver have mainly focused on three applications: low power, process tolerance (self-healing) and multi-standard software defined radio. Here the key research papers in this domain are presented.

1.2.6.A. Adaptation for low-power operation

An environment-aware adaptive power management strategy for RF systems, where performance of the front-end is traded-off for power consumption in such a way that operation of system is maintained at or below a specified bit-error rate (BER) across temporally changing channel conditions, is proposed in [20]. In [21], the effects of process variation are considered in the previous framework and operation of the RF system is ensured at the minimum power level without compromising the system-level performance requirement across all channel conditions and process corners.

1.2.6.B. Adaptation for process tolerance (self-healing)

System level adaptation mechanisms of RF front-ends for mitigating effects of process variation are presented in [22]-[25]. Tuning algorithms based on gradient-search [22] and Augmented Lagrange [23] are proposed for post-manufacture yield improvement of RF systems considering multiple performance specifications. Another technique, presented in [24], relies on extracting a signature from the device that suffers from process variation and tuning using minimal on-chip digital resources. A detailed cost model for post production tuning is developed in [25].

1.2.6.C. Adaptative software defined multi-standard radio

The motivation behind software defined radio is to build a flexible and adaptive radio front-end that can support multiple modes and standards of communication in the same programmable platform. Building a software defined radio requires digital signal processing algorithms to support highly adaptive RF front-end. Developments in this area are shown in [26].

1.2.7. Digitally intensive RF architecture

In recent years, RF circuit design is going through a big paradigm shift as the need for single chip integration of digital, analog and RF is becoming a necessity in nanoscale CMOS. Instead of just making RF circuits tunable, a fundamental change is taking place in the way RF circuits are designed as the available voltage headroom is reducing with the scaling of supply voltage. RF architectures are becoming more and more digitally intensive where they tend to process analog information in time domain exploiting the fast switching response of scaled CMOS devices [27]. Example of such an architecture is Texas Instrument's digital RF [27] which employs digital power amplifier (DPA), all-digital PLL (ADPLL) featuring time-to-digital converter (TDC) and digitally controlled oscillator (DCO) and the discrete time receiver using sophisticated analog and digital signal processing. The basic structural difference between the conventional RF transceiver and the new digitally intensive RF architecture, as discussed in [27], is shown in Figure 1.

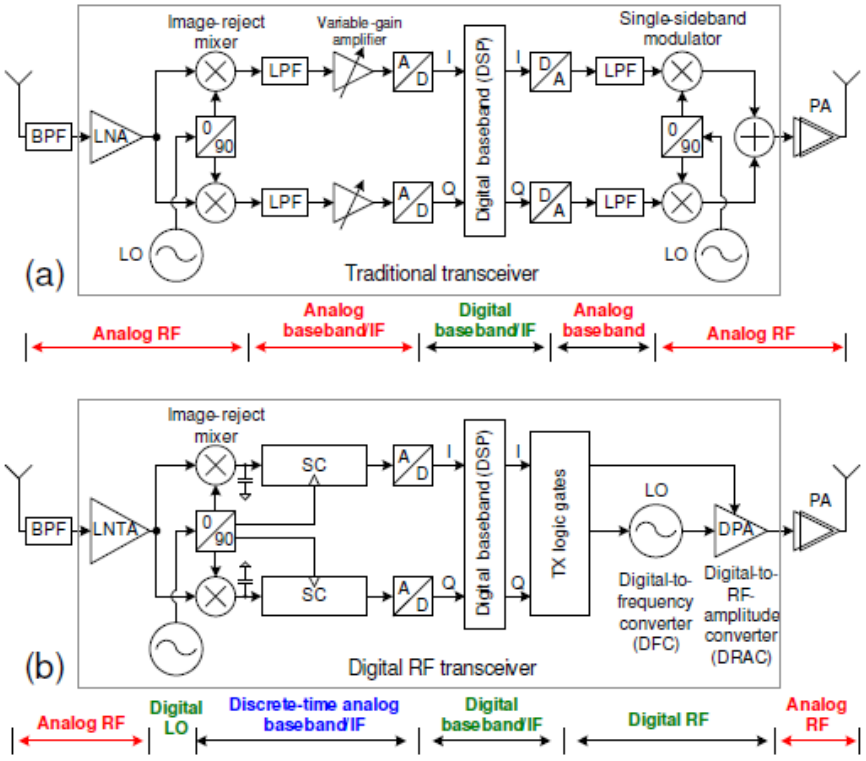


Figure 1. (a) Traditional RF transceiver and (b) Digital RF transceiver [27]

1.3. Proposed Research

Overview of the key aspects of this thesis is shown in Figure 2. An adaptation framework is developed for process variation tolerant RF systems. This adaptation framework has two parts – optimized test stimulus driven diagnosis of individual modules and power optimal system level tuning. The proposed diagnosis technique is described in Chapter 2 and the tuning methodology is explained in Chapter 3. Another direct tuning approach is developed and demonstrated on a carbon nanotube based analog circuit which is presented in Chapter 4. An adaptive switched mode power amplifier is designed which is more digital-intensive in nature (as opposed to traditional linear power amplifiers) and has higher efficiency, improved reliability and better process variation tolerance. Operation of this adaptive power amplifier is discussed in Chapter 5. In

Chapter 6, a testing strategy for adaptive systems is shown which reduces test time and test cost compared to traditional testing. Finally conclusions and possible future works are discussed in Chapter 7.

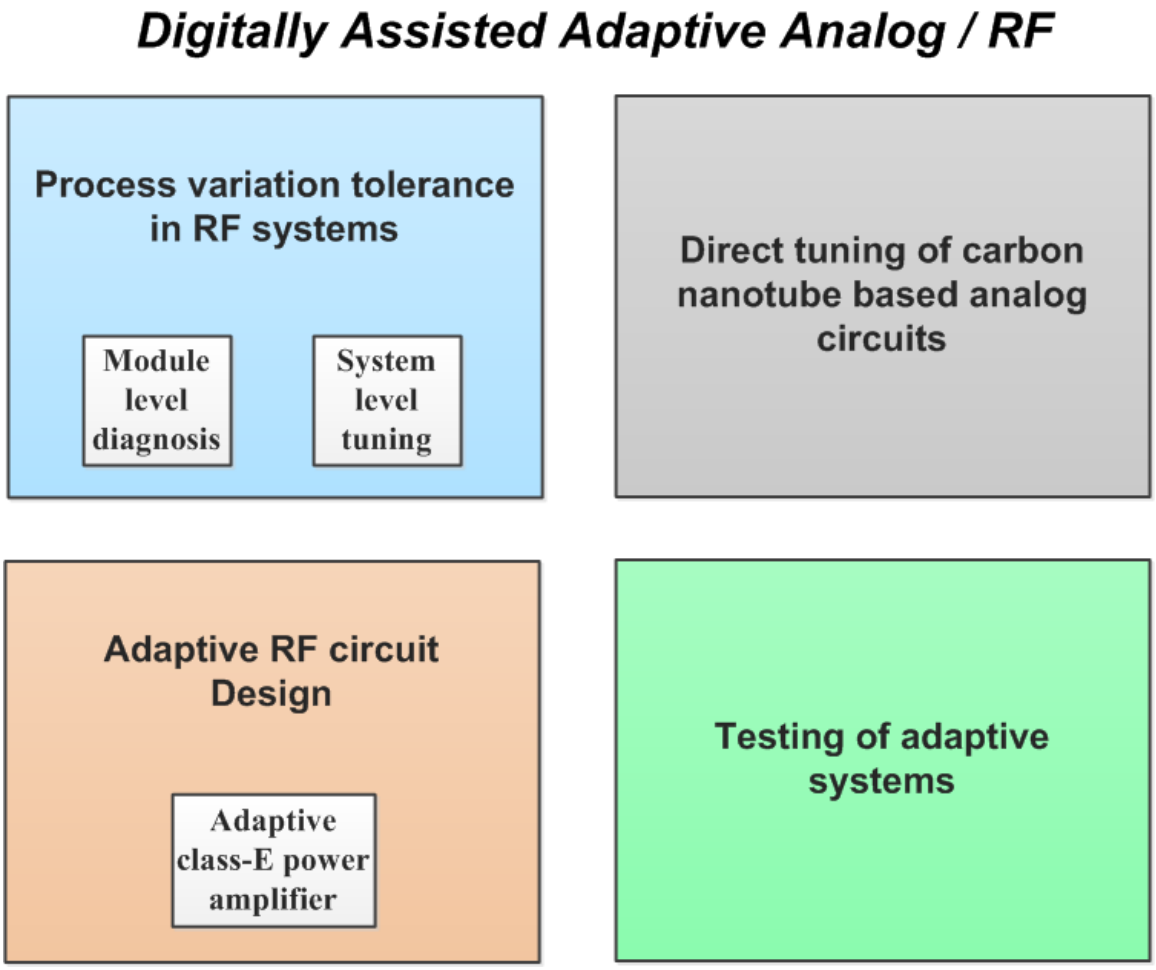


Figure 2. Overview of research contribution

CHAPTER 2

OPTIMIZED TEST STIMULUS DRIVEN DIAGNOSIS OF RF SYSTEMS

Automated generation of optimized test signals for diagnosis of RF systems, which is a key aspect of the proposed process variation tolerant adaptation framework, is discussed in this chapter. The proposed approach of designing process variation tolerant adaptive analog / RF systems involves using adaptive circuit modules with tuning knobs that are controlled by the adaptation algorithm running on the digital signal processor. The general architecture of a digitally assisted adaptive RF transmitter system is shown in Figure 3, where a set of digital "tuning control (TC)" registers determine the values of the tuning knobs of the adaptive modules. During process adaptation, the baseband unit senses the quality of the process from the results of built-in tests applied to the system captured by built-in performance sensors (envelope detector at the output of the power amplifier in Figure 3), using algorithms running on the baseband processor. This, in turn, is used to actuate control procedures implemented in the baseband unit that sets the values of the TC registers in an iterative manner until performance convergence is achieved.

Fundamentally, process variation tolerant adaptation involves two steps: (a) diagnosis of mixed-signal/RF performance parameters at the system and module level and (b) adjustment of digital and analog "tuning knobs" designed into the mixed-signal/RF and baseband signal processing modules that allow their performances to be traded off for power consumption so that overall system level performances are met with the least impact on total power consumption. Diagnosis of RF systems using optimized test signals (first step of the proposed adaptation framework) is discussed here.

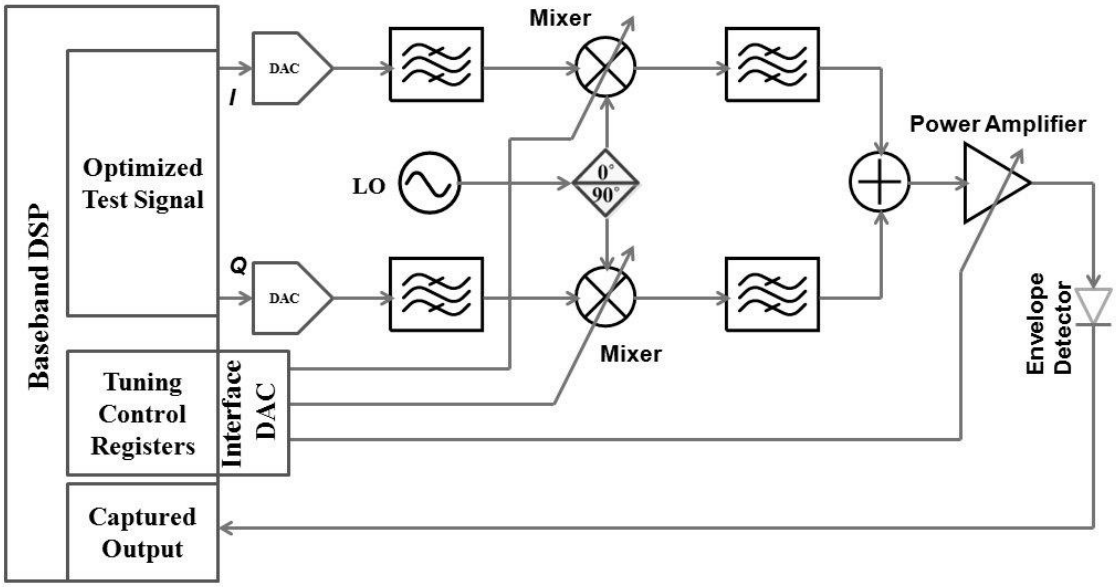


Figure 3. Adaptive RF transmitter with sensing and control circuits

2.1. Prior Work

Several diagnosis techniques have been proposed in the past that can be applied to the problem of calibration/tuning of RF systems. Standard testing techniques for RF systems employ different tests for each test specification and incur significant test time and require expensive test instruments which can not be used in the proposed process tolerant (self-healing) framework. The "alternate testing" approach has been used in the past to predict multiple specifications from a single test application [28], [29]. This has the benefit of incorporating the inaccuracies of the test measurement system into the test data obtained. However, the technique involves the development of regression models [30] and the "training" procedure used to develop the regression models requires the use of standard testing procedures. In contrast, behavioral model parameter estimation based test and diagnosis techniques have been used in the past for determining nonidealities of mixed-signal/RF systems. These iterative techniques do not require any supervised learning or training and RF DUT specifications can be predicted directly from the raw downconverted output using a single data acquisition resulting in a very fast test and

diagnosis procedure. Iterative algorithms for determining the parameters of predistortion filters to compensate for amplitude and phase nonlinearities of RF power amplifiers are well known and used extensively in wireless handsets [31], [32]. In [33], Senguttuvan has shown how the model parameters of a transmitter and thereby the inverse distortion characteristics of a predistortion filter can be derived from transient response analysis of the transmitter output through use of an iterative least mean squares (LMS) solver. In [34] and [35], Cherubal and Chatterjee have proposed a device parameter computation based diagnosis methodology for analog integrated circuits. A nonlinear solver is used to determine the critical Spice-level model parameters of devices such as amplifiers directly from the transient response of the device to an optimized test stimulus. In [36], the authors have shown how the parameters of a Volterra series model of nonlinear mixed-signal devices can be estimated from the results of pseudorandom tests. The problem of loopback testing of RF transceiver systems has been investigated in [37] by Halder and it has been shown for the first time how the Gain and IIP3 values of the transmitter and receiver could be decoupled from the results of loopback tests. This has been further applied to decouple the nonlinearities of cascaded RF modules (e.g. mixer, PA) from envelope detector data by Han, Bhattacharya and Chatterjee in [38]. In [39], Erdogan and Ozev describe a method for characterizing the RF transceiver parameters from analysis of demodulated loopback data. In addition to the fundamental nonlinearity parameters diagnosed in [37]-[38], they are also able to diagnose other parameters such as I-Q mismatch and DC offset values from the looped back test data. While the methods of [37]-[38] use regression based techniques to decouple embedded RF module parameters, the method of [39], [40] uses a nonlinear solver to do the same (as in [33]-[35]). In [37], [38], optimized multitones are used as test stimuli but only gain and IIP3 specifications are targeted. In [39], a larger set of performance specifications is targeted, but OFDM frames containing random data are used as test stimuli, resulting in longer test times. In each of the above methods [33]-[40] the device parameter values are extracted from

observed test data using accurate simulation models of the DUT that incorporate the parameters being diagnosed.

2.2. Key Contributions

The key contributions of the proposed optimized test stimulus driven diagnosis and testing technique are as follows:

- *An algorithmic test stimulus generation technique* for behavioral model parameter computation of RF transceiver systems is proposed. A compact test signal is derived that allows a nonlinear solver to determine the behavioral model parameters accurately from the observed time-domain test response which leads to significant reduction in test time. Prior methods have used either random stimuli resulting in relatively long test times or solved for a limited number of behavioral model parameters and specifications (Gain, IIP3).
- It is shown that different types of deterministic test signals (as opposed to random OFDM data which incurs longer test times) are sufficient to diagnose complex transmitter and receiver parameters. 5 different optimized test signals are shown: (a) a single optimized OFDM data frame, (b) optimized orthogonal multi-tone (4 tones) signal, (c) optimized non-orthogonal multi-tone (4 tones) signal, (d) time domain transient test signal and (e) optimized pulse sequence.
- It is shown that *the RF power amplifier's 5^{th} order nonlinearity with AM-PM distortion and memory effects (Wiener model), nonlinearity of mixer and low noise amplifier, I/Q gain and phase mismatch and DC offset* can be diagnosed concurrently from the applied compact test. Data from an envelope detector connected to the output of the transmitter and downconverted baseband data of the receiver are used to perform diagnosis of the transmitter and receiver performance metrics. One of the requirements of model parameter estimation based diagnosis and testing technique is that the models have

to be accurate in the ability to represent all critical nonidealities of the system. With regard to this concern, the proposed model is the most comprehensive.

- It is shown that with the use of only one sensor (an envelope detector attached to the output of the transmitter), it is possible to accurately diagnose nonlinearities of individual modules such as PA, LNA and mixers (decoupling nonlinearities of cascaded blocks) along with other nonidealities of the transceiver in loopback connection. If the envelope detector is not used, then the nonlinearity of whole transmitter and receiver can be obtained accurately from the downconverted output of the receiver but module level diagnosis suffers from loss of accuracy.

2.3. Overview of Proposed Approach

The steps involved in the diagnosis of RF transceiver systems using automatically generated tests are shown in Figure 4. The method is supported by comprehensive behavioral models of the critical nonidealities of RF transceiver systems (box 1 of Figure 4). In addition to the complete RF transceiver system, the modeling framework also includes models of design for testability (DfT) structures embedded in the hardware to facilitate testing. Specifically, model of an envelope detector sensor for observing the output of the transmitter is included and allows simulation of the complete test setup of the transceiver shown in Figure 5. The diagnosis procedure involves two key steps:

(a) Test stimulus generation to facilitate model parameter computation from the observed DUT response (data from envelope detector sensor as well as the "looped back" output of the receiver of Figure 5). The accuracy with which all the model parameters can be computed from the DUT test response is used as a measure of the "goodness" of a candidate test stimulus during stimulus optimization. This is shown in box (2) of Figure 4.

(b) Diagnosis of the transceiver model parameters (and consequently the test specifications of the transceiver) from the observed DUT response using a nonlinear solver. The nonlinear solver finds the combination of model parameter values that produces the same (or as close to) model response as that observed at the output of the DUT on application of the optimized test stimulus determined earlier. The resulting model parameters are then used to compute performance specifications. This is shown in box (3) of Figure 4.

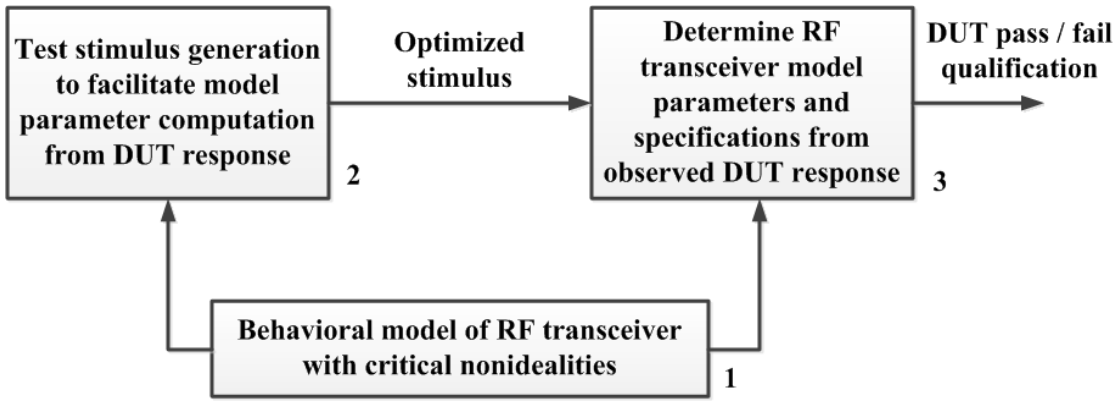


Figure 4. Overview of the proposed optimized test stimulus driven diagnosis technique

2.4. Diagnosis Framework

The diagnosis setup is shown in Figure 5. The RF transmitter and receiver are connected in loopback mode and an envelope detector is placed at the output of the transmitter to capture the low frequency envelope of the PA output. The optimized test stimuli are applied to the I and Q inputs of the transmitter from the baseband unit. The test signals are upconverted by the quadrature mixers with local oscillator frequency of 2.4 GHz and then amplified by the power amplifier. The low frequency envelope of the

modulated signal at the output of the PA is captured by the envelope detector. The output of the PA is "looped back" to the input of the receiver. The received signal is amplified by the LNA and then down-converted by the mixers and subsequently the I and Q baseband signals are analyzed. The digitized envelope detector output and the I and Q output signals in the receiver are used for computing the model parameters of the transceiver system. First, the nonlinear solver computes the model parameters of the transmitter from the output of the envelope detector. Once the transmitter model parameter values are known, the nonlinear solver is used to determine the receiver's model parameters using the I and Q signals within the receiver. The targeted parameters of the transceiver are I/Q gain and phase mismatch, nonlinearity (AM-AM) and AM-PM with memory effects of the PA, nonlinearity of LNA and mixer and DC offset due to LO leakage. Note that diagnosis of the transmitter and receiver model parameter values is also possible without the use of the envelope detector at the output of the transmitter, using just the I and Q signals produced by the receiver, at the cost of some accuracy of diagnosis.

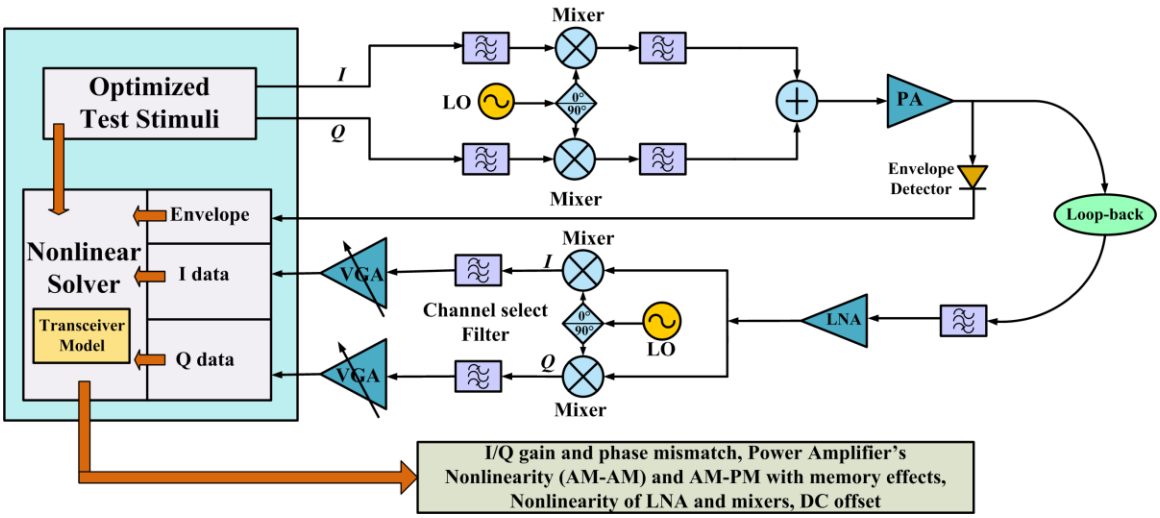


Figure 5. Diagnosis framework

2.5. Behavioral Model of the Transceiver

A comprehensive behavioral model of the OFDM RF transceiver is built in MATLAB in presence of different nonidealities of its components as described in this section.

2.5.1. I/Q imbalance in transmitter

In OFDM systems I-Q modulation is used where quadrature mixers are employed to up-convert and down-convert the I and Q signals separately. The information to be transmitted is modeled as a complex signal having I and Q components:

$$X(t) = I(t) + jQ(t) \tag{1}$$

After up-conversion by the mixers, the modulated signal can be written as:

$$Y(t) = \text{Real}(X(t)e^{j2\pi f_c t}) = I(t)\cos(2\pi f_c t) - Q(t)\sin(2\pi f_c t) \tag{2}$$

Ideally, the carriers used for modulating the I and Q signals have same amplitude and are phase shifted by 90° from each other. However, due to quadrature mismatch [41]-[42] the relative amplitude and phase difference of the carriers on the I and Q paths differ from their ideal values. If the effects of I/Q mismatch are included, then (2) becomes:

$$Y(t) = I(t)\cos(2\pi f_c t) - (1+\varepsilon_{TX})Q(t)\sin(2\pi f_c t + \phi_{TX}) \tag{3}$$

where ε_{TX} is the magnitude mismatch and ϕ_{TX} is the phase mismatch.

2.5.2. DC offset

Due to capacitive feed through from the local oscillator (LO leakage) and self-mixing, a dc signal component appears in the signal path [42]. This phenomenon is modeled by adding a dc component with the signal which depends on the extent of capacitive coupling.

2.5.3. Distortions in the RF power amplifier

A complex envelope driven memory-less behavioral modeling of the power amplifier is done. This model reflects the instantaneous variation in the output envelope of the PA due to change in the input envelope [43]. The input signal to the PA can be written as

$$s(t) = r(t)\cos(\omega_c t + \psi(t)) = \mathrm{Re}\left[r(t)e^{j\{\omega_c t + \psi(t)\}} \right] \tag{4}$$

where the complex envelope $r(t)e^{j\psi(t)}$ modulates the RF carrier of frequency ω_c.

If the envelope of the input signal is expressed as $r'(t)$ then the output of the power amplifier is modeled as:

$$s'(t) = f(r'(t))[\cos(\omega_c t + \psi(t) + g(r'(t)))] \tag{5}$$

where $f(r'(t))$ implements the AM-AM (amplitude to amplitude) and $g(r'(t))$ models the AM-PM (amplitude to phase) behavior of the PA. These functions can be represented as fifth order and third order polynomials respectively:

$$f(r'(t)) = \sum_{i=0}^{5} \alpha_{i(PA)} \left[r'(t) \right]^i \tag{6}$$

$$g(r'(t)) = \sum_{k=0}^{3} \beta_{k(PA)} \left[r'(t) \right]^k \tag{7}$$

where $\alpha_{1(PA)}$ is the gain of the power amplifier. The input to the power amplifier is given by (3) which is to be expressed in the form of (4) for modeling AM-AM and AM-PM effects. Trigonometric identities are used to transform the signal from one representation to the other:

$$\begin{aligned} Y(t) &= I(t)\cos(\omega_c t) - (1+\varepsilon_{TX})Q(t)\sin(\omega_c t + \phi_{TX}) \\ &= \cos(\omega_c t)[I(t) - (1+\varepsilon_{TX})Q(t)\sin(\phi_{TX})] - \sin(\omega_c t)[(1+\varepsilon_{TX})Q(t)\cos(\phi_{TX})] \end{aligned} \tag{8}$$

From the definitions below,

$$V_1(t) = I(t) - (1+\varepsilon_{TX})Q(t)\sin(\phi_{TX}) \tag{9}$$

$$V_2(t) = (1+\varepsilon_{TX})Q(t)\cos(\phi_{TX}) \tag{10}$$

two other variables in terms of $V_1(t)$ and $V_2(t)$ can be defined as:

$$A(t) = \sqrt{V_1(t)^2 + V_2(t)^2} \tag{11}$$

$$\gamma(t) = \tan^{-1}(V_2(t) / V_1(t)) \tag{12}$$

From (8) and using (9), (10), (11) and (12) we can write:

$$Y(t) = A(t)\cos[\omega_c t + \gamma(t)] \tag{13}$$

Equation (13) is in the form of (4) and AM-AM and AM-PM effects can be included in (13) easily by finding the envelope of Y(t) and using (6) and (7) to calculate the amplitude and phase components.

Memory effects in PA - Wiener model: An alternative and more accurate modeling of the power amplifier is done which captures the memory effects. Memory effects in nonlinear power amplifiers can be captured by Volterra series models. But number of coefficients in the Volterra series increases very quickly with memory length and degree of nonlinearity and hence it increases computational cost in the proposed model parameter calculation technique. In this work, power amplifier's nonlinearity and memory effects are captured using the Wiener model which is a special case of the Volterra series [44]. In this model a linear time invariant system is followed by a 5^{th} order nonlinearity as shown below:

$$z[n] = \sum_{q=1}^{R} D_q \left[\sum_{p=0}^{M-1} C_p x[n-p] \right] \left| \sum_{p=0}^{M-1} C_p x[n-p] \right|^{q-1} \tag{14}$$

where x[n] is the input to the power amplifier and z[n] is its output, C_p are the coefficients of the LTI system and D_q are the nonlinearity coefficients, q is odd and R is 5 in this work. This model is more accurate as it captures the memory effects but it also requires more computation time in the proposed parameter estimation based diagnosis technique. Both of the models are used for simulation in this work and depending of the requirement (computation vs. accuracy), one of the models can be chosen.

2.5.4. Nonlinearity of LNA and mixer

The nonlinear characteristics of the low noise amplifier and up and down-conversion mixers are modeled as third order polynomials:

$$v(t) = \sum_{h=0}^{3} \alpha_h \left[u(t)\right]^h \tag{15}$$

where *u(t)* and *v(t)* are the input and output signal of the nonlinear block respectively.

2.5.5. I/Q imbalance in receiver

The I/Q gain and phase mismatch in the receiver is modeled in the same way as for the transmitter. The local oscillator signal with I-Q imbalance is expressed as:

$$s_{LO}(t) = \cos(2\pi f_{LO} t) - j(1+\varepsilon_{RX})\sin(2\pi f_{LO} t + \phi_{RX}) \tag{16}$$

where ε_{RX} is the magnitude mismatch and ϕ_{RX} is the phase mismatch of the receiver LO signal.

2.5.6. Computation of specifications from model parameters

The gain and input IP3 specifications of nonlinear modules are calculated from model parameters using the following relations [42]:

$$Gain = 20\log_{10}(\alpha_1) \text{ dB} \tag{17}$$

$$AIP3 = \sqrt{(4/3)\left|\alpha_1/\alpha_3\right|} \text{ volts} \tag{18}$$

Other performance specifications such as I-Q gain and phase imbalance and dc offset are found directly from the computed parameters.

2.6. Optimized Test Signal Generation

A Genetic Algorithm (GA) driven test generation technique is proposed which improves the accuracy of model parameter computation. The test stimuli are optimized in such a way that the error in the prediction of the model parameters is reduced as shown in

Figure 6. Genetic Algorithms (GA) are a class of evolutionary algorithms that are extensively used for solving optimization problems [45]. Candidate solutions of the optimization problem are constructed as structures called 'Chromosomes'. Finite populations of such chromosomes represent the solution set found in each stage of evolution. The algorithm starts with a randomly generated population set and for each chromosome computes the fitness function that is to be optimized. Selection rules are applied to find out the candidate solutions with better fitness value which corresponds to chromosomes with better chance of survival from evolution. Crossover and Mutation techniques are applied on the set of selected chromosomes and new generation of sibling chromosomes are created. Crossover operator combines two chromosome structures and generates a new chromosome and Mutation introduces random local perturbation into the constitution of selected chromosomes. For each generation, GA determines the best solution and the fitness value for the best chromosome approaches the global optima with the convergence of the algorithm.

At first, a multitude of RF transceiver instances (nominal as well as from different process corners) are created in ADS simulation by introducing process variation and used for the proposed test generation. In this work, chromosomes or candidate solutions of the genetic optimization are a set of test signals. GA starts with a randomly generated set of test signals which is the initial population of candidate solutions. For each test signal, cost function of the optimization is calculated (as defined later). Test inputs with better cost metric are selected and from those test signals GA creates next generation of candidate solutions. For evaluating cost function for each test stimuli, the test signal is applied to all of the transceiver instances and their model parameters are calculated from output response (this model parameter computation technique is explained in detail in Section 2.7). Total parameter computation error across all these instances is defined as the cost function. For computing model parameters of a particular transceiver instance using a particular test input, the test stimulus is applied to the transceiver instance with

known model parameters (from ADS simulation) and its generic behavioral model with unknown model parameters (x_i). In the beginning, the simulation is done with some initial guess of parameters x_i and response of the transceiver instance and its generic model are captured as shown in Figure 6. Then a nonlinear solver modifies the model parameters x_i so that response of the generic model (y) matches with the response of the transceiver instance (z). When the squared error between the two waveforms (y and z in Figure 6) becomes minimum, the nonlinear solver stops and generates the model parameter values. For each test stimulus, this step is repeated for all process varied instances generated in ADS and errors between the actual and predicted values of the parameters are evaluated and the total absolute error (normalized) in parameter computation is calculated as shown in Figure 6. This computation error is defined as the cost function of GA which is to be minimized as shown in Equation (19).

$$\textbf{Cost Function: } Minimize \sum_{i=1}^{n} \sum_{j=1}^{m} \left| p_a(i,j) - p_c(i,j) \right| \tag{19}$$

where $p_a(i,j)$ is the actual value (normalized) of j^{th} model parameter of i^{th} device instance, $p_c(i,j)$ is the computed value (normalized) of j^{th} model parameter of i^{th} device instance, n is the number of device instances and m is the number of model parameters for each device. Depending on the evaluated cost metric, a new generation of chromosomes is produced. The genetic algorithm stops when the maximum allowed simulation time is exceeded or improvement in the fitness value is no longer possible. There are two levels of optimization involved in this method. The nonlinear solver minimizes the difference between two output waveforms while the GA minimizes the parameter computation error.

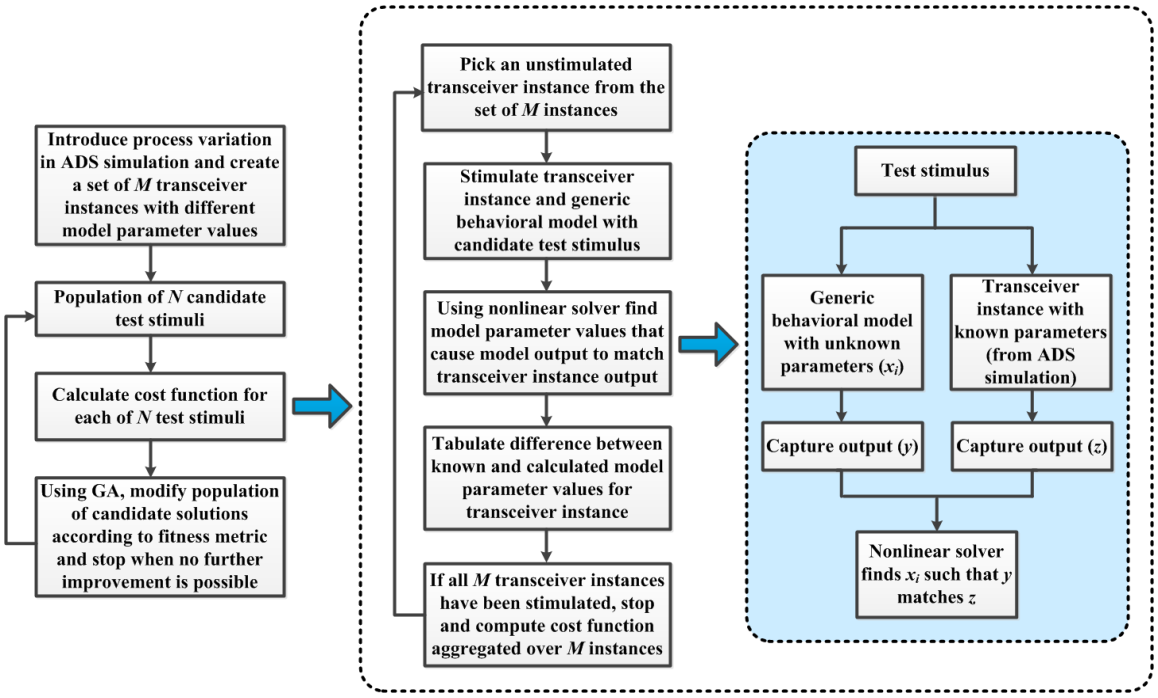


Figure 6. Test generation procedure for model parameter computation based diagnosis

In the proposed approach parameters of the behavioral model are computed from the information contained in the output waveform. It has to be ensured that the output waveform captures the effects of all the parameters that are to be computed. Generation of an optimized test input is necessary that stimulates all the parameters of the model so that their effects show up in the output waveform. For example, let us assume that the DUT shows nonlinear behavior only for large amplitude signal and for small signal the behavior of the DUT is completely linear. Now if the amplitude of the test stimulus is so small that it is within the linear region of the DUT characteristic, then the response of the DUT will never contain any nonlinear effects of the device. Hence just analyzing the output waveform it will not be possible to calculate the nonlinearity. This necessitates use of a test stimulus that has sufficiently large amplitude in order to excite the nonlinearity of the DUT so that the distortion effects show up at the output.

5 different types of test signals are generated in this work as explained below.

(1) Optimized 64 tones (single OFDM data frame): In this case, I and Q test stimuli are combination of 64 equally spaced tones (subcarriers) within 20 MHz bandwidth. The candidate solution (chromosome) of the genetic algorithm is a vector containing amplitude and phase angle levels corresponding to the input tones and the genetic algorithm optimizes the amplitude and phase of each tone.

(2) Optimized orthogonal 4 tone signal: Next, number of tones in orthogonal multitone test signal is minimized using GA and optimized 4-tone (orthogonal) signals are generated. It should be noted that minimizing the number of tones in a multitone test signal minimizes the "intermodulation noise" due to nonlinearities in the on-chip data converters used to drive the test.

(3) Optimized non-orthogonal 4 tone signal: The tones in the multitone test signal can be non-orthogonal as well. Using genetic algorithm optimized non-orthogonal 4 tone test signals are generated where cost function formulation and minimization are done similarly as explained earlier.

(4) Time domain optimized transient test signal: Optimized high frequency time domain transient test signals are generated for I and Q inputs. In this case, a chromosome in genetic optimization represents amplitude values at different sample points. Resulting transient signal is band pass filtered and then applied to the transceiver and corresponding cost function value is calculated in a similar way.

(5) Optimized pulse sequence as test stimulus: For testing receiver or stand-alone RF component (without up-converter), high frequency test signal needs to be generated directly using inexpensive resources available on chip. One such approach is to generate the test signal from an optimized pulse sequence produced by on chip LFSR or state machine and simple digital logic and using that signal to compute basic non-idealities of the RF DUT. This approach is explained in detail in Section 2.8. The optimized pulse sequence for testing the RF DUT is found out using genetic algorithm in a similar way.

The candidate solution of the optimization problem is the bit sequence of the FSM or LFSR from which the pulse pattern can be derived using AND / OR gates. The cost function for the genetic algorithm is formulated such that the total error in the computed values of the model parameters is minimized.

In the following subsections, analysis of two aspects of test generation and model parameter computation are given: (A) Accuracy of model fitting using least square technique and (B) Decoupling nonlinear parameters of two cascaded blocks.

2.6.1. Accuracy of model fitting using least square technique

Let us consider a m^{th} order nonlinear model of the DUT so that input (x) and output voltages (y) are related by the following relation:

$$y = c_0 + c_1 x + c_2 (x)^2 + c_3 (x)^3 + ... + c_m (x)^m \tag{20}$$

Now an optimized test input is applied to the DUT and at 'n' time points the input amplitude (x) and output amplitudes (y) are captured. In general $n >> m$ which means number of data points are much larger than the number of c_i coefficients. It leads to the following system of linear equations:

$$\begin{aligned} y_1 &= c_0 + c_1.x_1 + c_2.(x_1)^2 + c_3.(x_1)^3 + ... + c_m.(x_1)^m \\ y_2 &= c_0 + c_1.x_2 + c_2.(x_2)^2 + c_3.(x_2)^3 + ... + c_m.(x_2)^m \\ &\vdots \\ y_n &= c_0 + c_1.x_n + c_2.(x_n)^2 + c_3.(x_n)^3 + ... + c_m.(x_n)^m \end{aligned} \tag{21}$$

It can be written in a compact form as: $\vec{y} = A\vec{c}$ where the matrix A is defined as:

$$A=\begin{bmatrix} 1 & x_1 & (x_1)^2 & . & . & (x_1)^m \\ 1 & x_2 & (x_2)^2 & . & . & (x_2)^m \\ 1 & x_3 & (x_3)^2 & . & . & (x_3)^m \\ . & . & . & & & . \\ . & . & . & & & . \\ 1 & x_n & (x_n)^2 & . & . & (x_n)^m \end{bmatrix} \tag{22}$$

As the number of equations is larger than the number of variables (c_i s), in most of the cases this linear system is inconsistent and a least square solution is obtained by minimizing the error $\left\|\vec{y}-A\vec{c}\right\|$ [46]. Inconsistency of the linear system implies that the vector $\vec{y}$ is not in the image of the matrix A. The vector in the image of A which is closest to the vector $\vec{y}$ is its orthogonal projection on the image of A. If $\overrightarrow{c^*}$ is a least square solution of this system, then $A\overrightarrow{c^*}=proj_V\left(\vec{y}\right)$ where $V=image(A)$. Hence the vector $\vec{y}-A\overrightarrow{c^*}$ is in $V^{\perp}=(image(A))^{\perp}=Kernel(A^T)$. The least square solution of the given system is the exact solution of the "normal equation" given by: $A^TA\vec{c}=A^T\vec{y}$ and when $Kernel(A)=\left\{\vec{0}\right\}$ the matrix A^TA is invertible and the unique least square solution is given by: $\overrightarrow{c^*}=(A^TA)^{-1}A^T\vec{y}$. If there are nonzero vectors in the kernel of A, that means there are free variables in the system $A\vec{c}=0$ which implies that $rank(A)<m$. This condition can happen if some rows of the matrix A are linear combination of some other rows. Effectively it implies that the linear equations of (21) are not linearly independent. This condition is avoided by performing test generation. It ensures that $rank(A)=m$ so that the situation is avoided where we can have infinitely many number of solutions.

2.6.2. Decoupling nonlinear parameters of two cascaded blocks

As discussed in [37]-[39], the presence of nonlinearity in an RF system allows the computation of the individual specifications of two cascaded RF modules from end-to-end

measurements on the cascaded chain. Let us assume that two RF blocks are connected in cascade and their behaviors can be expressed by (23) and (24) respectively:

$$r(t) = m_1 x(t) + m_2[x(t)]^2 + m_3[x(t)]^3 \tag{23}$$

$$s(t) = n_1 r(t) + n_2[r(t)]^2 + n_3[r(t)]^3 \tag{24}$$

where *x(t)* is the input to the first block, *r(t)* is the output of the first block and *s(t)* is the final output coming out of the second block. If (23) and (24) are combined then the behavior of the complete system can be expressed as:

$$s(t) = \sum_{i=1}^{9} c_i [x(t)]^i \tag{25}$$

$$\text{Where } c_i = f_i(m_1, m_2, m_3, n_1, n_2, n_3) \tag{26}$$

Equations (25) and (26) show that third order nonlinear behavior of the two blocks effectively results in a 9th order nonlinear transfer function of the total system where each coefficient of $[x(t)]^i$ is a function of the *m* and *n* coefficients of individual blocks. If using the model fitting technique all the c_i coefficients are accurately calculated by analyzing the input and output waveforms, then a set of 9 equations are obtained in terms of the parameters of Equation (26). These 9 equations containing 6 unknown variables (*m* and *n* coefficients) define a system of equations from which the approximate values of the unknown variables can be calculated using standard least square techniques.

Two important aspects have to be considered while decoupling parameters of individual components from system response. First let us consider the case when the second block is completely linear i.e. $n_2 = 0$ and $n_3 = 0$. The combined equation becomes:

$$s(t) = n_1 m_1 x(t) + n_1 m_2[x(t)]^2 + n_1 m_3[x(t)]^3 \tag{27}$$

Here we have 3 equations with 4 unknown variables which mean multiple solutions are possible. If the applied signal amplitude level is very small and one or both of the blocks operate in the linear region (if *x(t)* is very small then $r(t) \approx m_1 x(t)$

and $s(t) \approx n_1 r(t)$) then decoupling will not be possible. By optimizing the test stimulus it is ensured that the nonlinear behavior of both of the blocks are excited.

Secondly, even if the system under consideration shows 9^{th} order nonlinear behavior as shown in Equation (25), the test must be designed in such a way that information upto the 9^{th} order harmonic or relevant intermodulation terms are preserved in the observed output signature. In the presence of filters inherent in RF systems, the effects of higher order nonlinear behavior should be captured in the intermodulation frequency components within the passband of the system.

2.7. Model Parameter Computation Based Diagnosis Technique

Testing and diagnosis are performed by estimating the parameters of the behavioral model of the DUT and then computing the performance specifications from those behavioral models. Test signals are applied to the DUT and its behavioral model, and the responses are captured. Then a nonlinear equation solver adjusts the behavioral model parameters iteratively until the simulated model response to the applied test matches the observed DUT test response. When the difference between the simulated and actual output is minimized sufficiently, the nonlinear solver stops and generates the computed model parameters (shown in Figure 7). In this work, the optimized test stimuli are applied to the I and Q inputs of the RF transmitter when the transmitter and receiver are connected in loopback mode and an envelope detector is placed at the output of the transmitter as shown in Figure 5. The signatures of the DUT are obtained by capturing the envelope output from the envelope detector and I and Q outputs of the receiver. First, from the output of the envelope detector, which is a function of the transmitter nonidealities, parameters of the transmitter are computed. The response (envelope detector output) of the behavioral model of the transmitter is obtained in simulation. A MATLAB based nonlinear equation solver [47] computes the behavioral model parameters of the

transmitter in such a way that the difference between the actual envelope detector response and the simulated envelope output is minimized. Next, the I and Q output at the receiver, which are functions of both transmitter and receiver parameters, are used by the nonlinear equation solver to find out the receiver parameters in a similar way. In this step, calculated values of the transmitter parameters are used as known variables by the nonlinear equation solver.

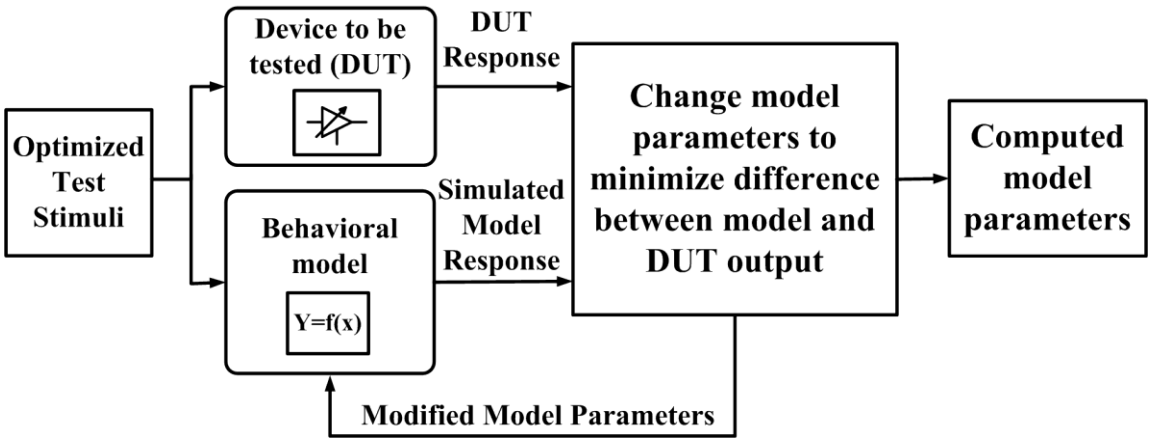


Figure 7. Behavioral model parameter computation method

A MATLAB based nonlinear data fitting problem solver [47] is used in this work for parameter computation of the transceiver model. The nonlinear solver uses "trust-region-reflective" nonlinear equation solving algorithm to compute the specifications of the transceiver system. The algorithm is based on trust-region method [48] and interior-reflective Newton method [49]. In trust-region method a model function is built which is an approximation of the original objective function around the current point. The neighborhood of the current point where the approximated function reflects the behavior of the original function is called the "trust-region". Then the approximated model function

is solved in the trust-region. If the candidate solution does not improve the original objective function then the trust region is shrunk and the algorithm searches for a new solution. In this work, for quick convergence of the nonlinear solver, range of variation for each model parameter is found from simulation and bounds are applied on both sides of model parameter values during parameter computation to restrict the search space and avoid aliasing.

2.8. Pulse Based Diagnosis

Optimized pulse based diagnosis and testing approach described in this section is fundamentally similar to the test generation and model parameter computation technique explained before, but this one is targeted towards the situation when very limited hardware resources are available for test purposes. Test and diagnosis costs can be lowered significantly if signal derived from a digital pattern can be adapted to serve as test stimulus for RF circuits. An optimized pulse stream containing a combination of spectral components within a specified RF frequency band is used as the test stimulus in this approach. This technique would be very effective while testing a receiver or standalone RF modules (PA, LNA) where upconversion of a low frequency test signal requires extra overhead and direct RF test stimulus generation using simple hardware resources is preferred.

In this work, a digital-compatible test stimulus generation approach for diagnosis and testing of RF circuits is developed. The proposed method uses optimized pulse sequences as input that can be driven by simple inexpensive digital circuits. Response analysis requires the use of a low-speed (relative to RF frequencies) A/D converter to digitize the down-converted response of the RF device under test (DUT). Down conversion of the RF test response is performed by a simple envelope detector placed at the output of the DUT. It is shown that the proposed approach allows critical gain and

nonlinearity specifications of the RF DUT to be determined accurately using a single data acquisition. The above technique eliminates the requirement of multiple-level power measurements or the use of expensive high frequency test instrumentation.

2.8.1. Key contributions of proposed pulse based diagnosis

The key contributions of this work are:

(1) Development of a novel digital compatible test generation algorithm for testing RF circuits using optimized pulse sequences.

(2) Use of a Finite State Machine or a modified Linear Feedback Shift Register (LFSR) along with simple digital circuitry for generating the RF test.

(3) Determination of multiple RF DUT specifications from a single data acquisition without requiring the use of supervised learning methods.

2.8.2. Core concepts

In this section, the core ideas that form the basis of this work are discussed.

2.8.2.A. Model parameter extraction in pulse based diagnosis:

In past research, the alternate test methodology [28]-[29] has been proposed and it involves the development of regression models [30] to predict multiple specifications of a DUT from a single test signature measurement. This test methodology has been shown to be scalable across a multitude of test specifications for a large variety of analog/mixed-signal/RF devices. However, the learning mechanism associated with alternate test is lengthy and requires the use of standard test techniques. In contrast, a test and diagnosis approach is developed that relies on the extraction of model parameters of the RF DUT and obviates the need to use a supervised learning algorithm specifically for the gain and nonlinearity specifications of RF devices. A key aspect of this approach is that the associated test time (complexity) is comparable to those of prior alternative RF test methods.

The RF test stimulus is derived from a pulse sequence optimized using Genetic Algorithm such that response of the RF DUT shows strong statistical correlation with its test specification values under multi-parameter DUT perturbations. The DUT is excited by the RF test stimulus and its response, which is distorted by the DUT nonidealities, is down-converted using an envelope detector. The down-converted signal is digitized for analysis and is called the *Distorted Response Signal*. Next, the test input signal is directly down-converted by the same envelope detector and digitized by a data converter. This is the ideal or *Golden Reference Signal*. Due to the simplified method of pulse based test signal generation (as opposed to more complex test signal generation techniques discussed earlier), only basic nonidealities and corresponding performance specifications (gain and IIP3) of the DUT can be computed in this technique using a simplified nonlinearity model. Given a finite order nonideality model (such as the 3rd order nonlinearity shown in Equation (15)) for the RF DUT, the model parameters are computed iteratively by mapping the golden reference signal to the distorted output of the DUT through the RF DUT model. The golden reference signal is treated as the input to the model and the model parameters are computed in such a way that the output of the model corresponds to the distorted response signal. In this work, the model is assumed to be of polynomial form of degree three. The third order polynomial is defined as $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$ where x is the input to the model and y is the distorted output signal of the model. The polynomial that maps the golden reference signal to the distorted response signal captures the distortion characteristics of the nonlinear transfer function of the RF device under test (DUT). For an ideal device, α_1 = gain, α_2 = 0 and α_3 = 0. After the polynomial $y = f(x)$ of the DUT model is computed, the specifications (gain and IIP3) of the device can be calculated using Equations (17) and (18).

2.8.2.B. Nonlinearity parameter computation

For a given test setup, if the Golden Reference and the Distorted Response Signal of the DUT are known, then the polynomial that characterizes the distortion can be computed by constructing the "Vandermonde" matrix *V*. Let the golden reference is x and the distorted response is y. The objective is to determine the polynomials p that maps x to y. If the degree of the polynomial is n, the Vandermonde matrix can be constructed as follows:

$$v_{i,j} = x_i^{n-j} \tag{28}$$

where $v_{i,j}$ is an element of the Vandermonde matrix *V* with row index *i* and column index *j*. Once the Vandermonde matrix is computed, the polynomials are obtained by solving the following equation in the 'least square' sense.

$$V.p \approx y \tag{29}$$

Equation (29) is solved by using standard QR factorization techniques $\left(inv(V) * y\right)$ to calculate *p* in a computationally efficient manner. In practical scenario the distorted response undergoes transformations from all the measurement setup in addition to the distortion characteristics of the RF device. However since the golden reference is captured into the digital signal processor via the same measurement path, the distortion introduced by the measurement setup is ignored here.

2.8.2.C. Pulse generation methodology

The pulse generation technique employs low cost digital circuitry consisting of a Linear Feedback Shift Register (LFSR) and basic logic gates. The pulses are constrained by the finite pulse width and rise and fall times. The bit stream of the LSFR, running at a relatively slow clock speed, is passed through an inverter and a logical AND / OR operation is performed on the original bit stream and the (delayed) inverter output. This creates sharp pulses whose width is determined by the delay of the inverter. The high frequency components of these pulses are utilized to test the RF device. For the AND

gate structure, pulses are generated at each positive edge of the bit sequence and for the OR gate, pulses are produced at every negative edge as shown in Figure 8 and Figure 9 respectively.

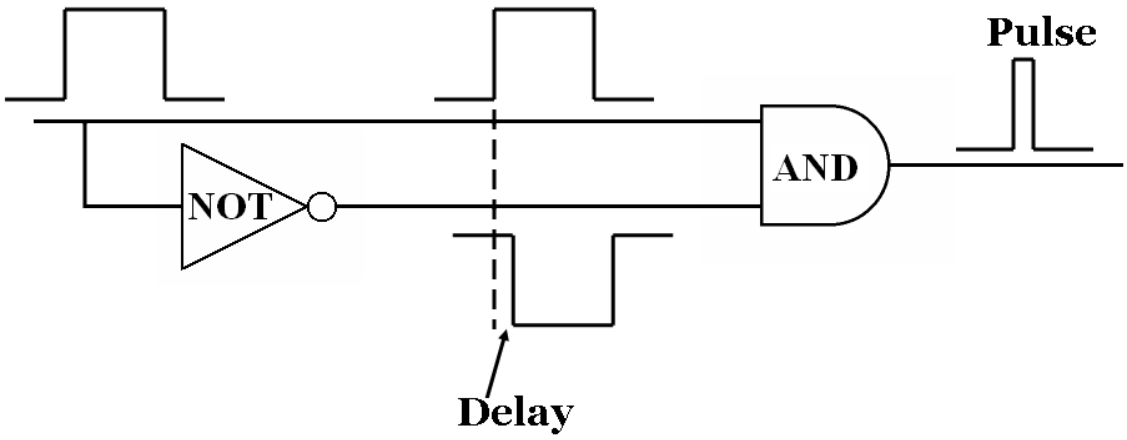


Figure 8. Pulse generation using AND gate and inverter

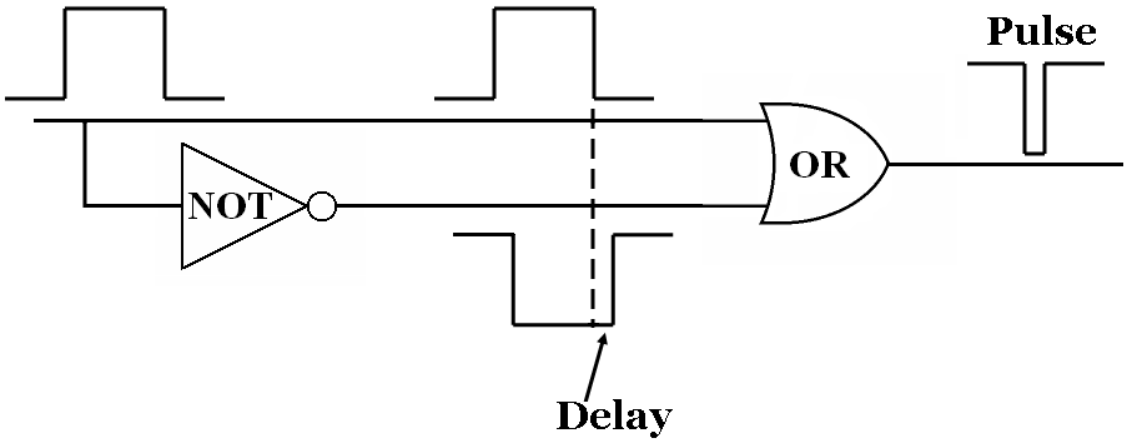


Figure 9. Pulse generation using OR gate and inverter

In the frequency domain, a pulse is represented by a *sinc* function of the form $\tau \text{sinc}(\omega\tau/2)$ where τ is the width of the pulse. A pulse sequence comprises of several pulses which are time shifted version of a pulse at *t = 0*. The Fourier transform of a signal *g(t)* which is shifted in the time domain can be expressed as:

$$g(t-t_0) \Leftrightarrow G(\omega)e^{-j\omega t_0} \tag{30}$$

where $g(t)$ is the original signal in the time domain and $G(\omega)$ is its Fourier transform. When the signal is time shifted by t_0, its phase spectrum changes by $-\omega t_0$ [50]. The goal of the optimization process is to find the right time shifted sequence of pulses so that using the frequency components of the pulse sequence in the frequency band of interest, the coefficients of the third order polynomial of device model can be estimated accurately. A limitation in pulse generation comes from the fact that a pulse can not be made infinitely narrow. The delays of the inverter gates of Figures 8 and 9 define the minimum achievable pulse width. As the pulse width increases, the main lobe of the sinc function narrows down in the frequency domain while its magnitude at low frequency increases as shown in Figure 10. It should be ensured that at the target RF frequency the signal component has enough amplitude so that it can excite the nonlinearity of the RF DUT. Another limiting factor is the finite rise and fall time of the pulses which is approximately 10% of the clock time period. As the rise and fall time increases, the high frequency component of the signal reduces as shown in Figure 11.

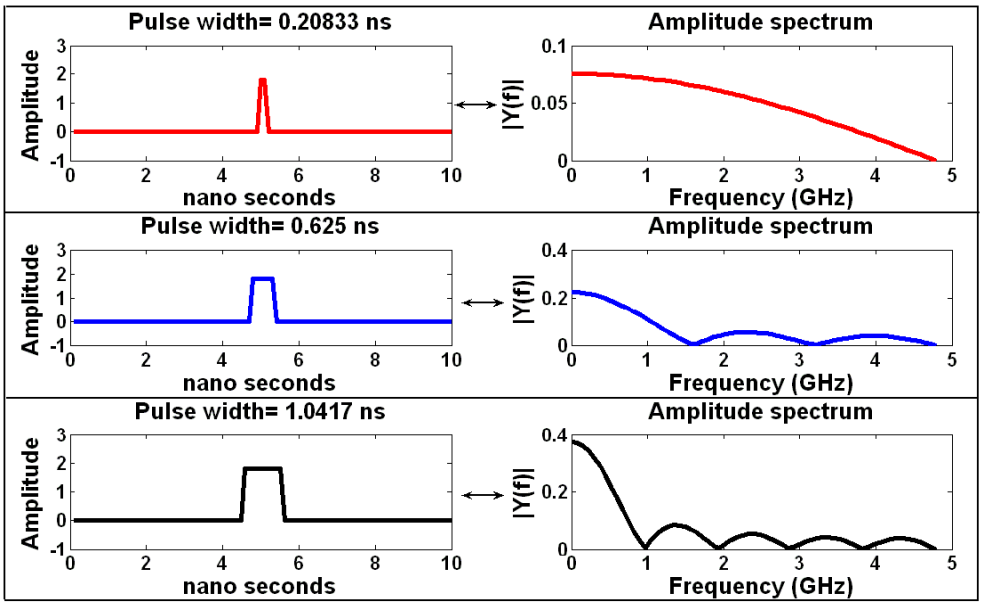


Figure 10. Variation in frequency spectrum with change in pulse width

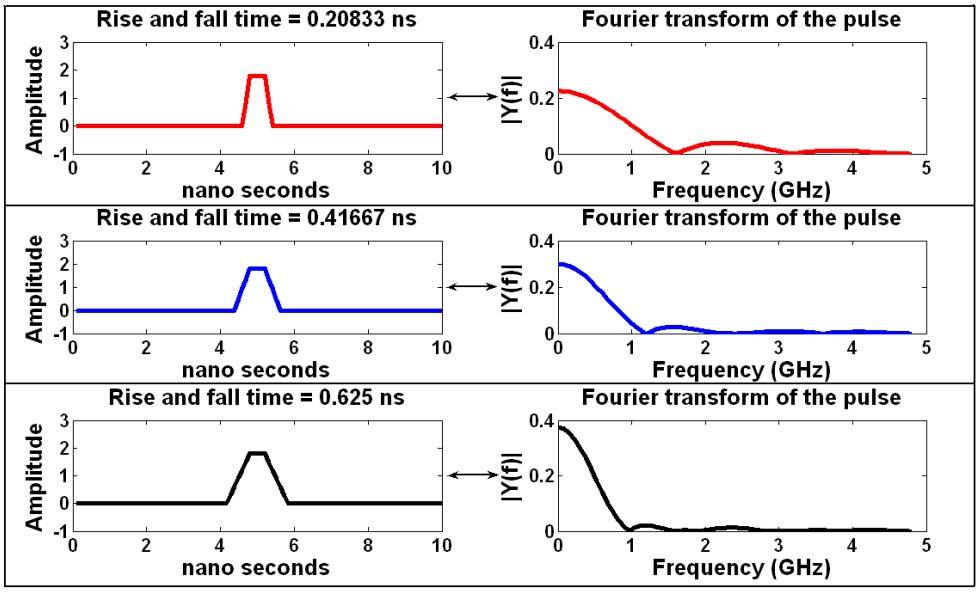


Figure 11. Change in frequency component distribution with different rise and fall time

2.8.3. Pulse based diagnosis framework

A WLAN OFDM power amplifier operating at 2.4 GHz is used for validating the proposed approach. Figure 12 illustrates the diagnosis framework.

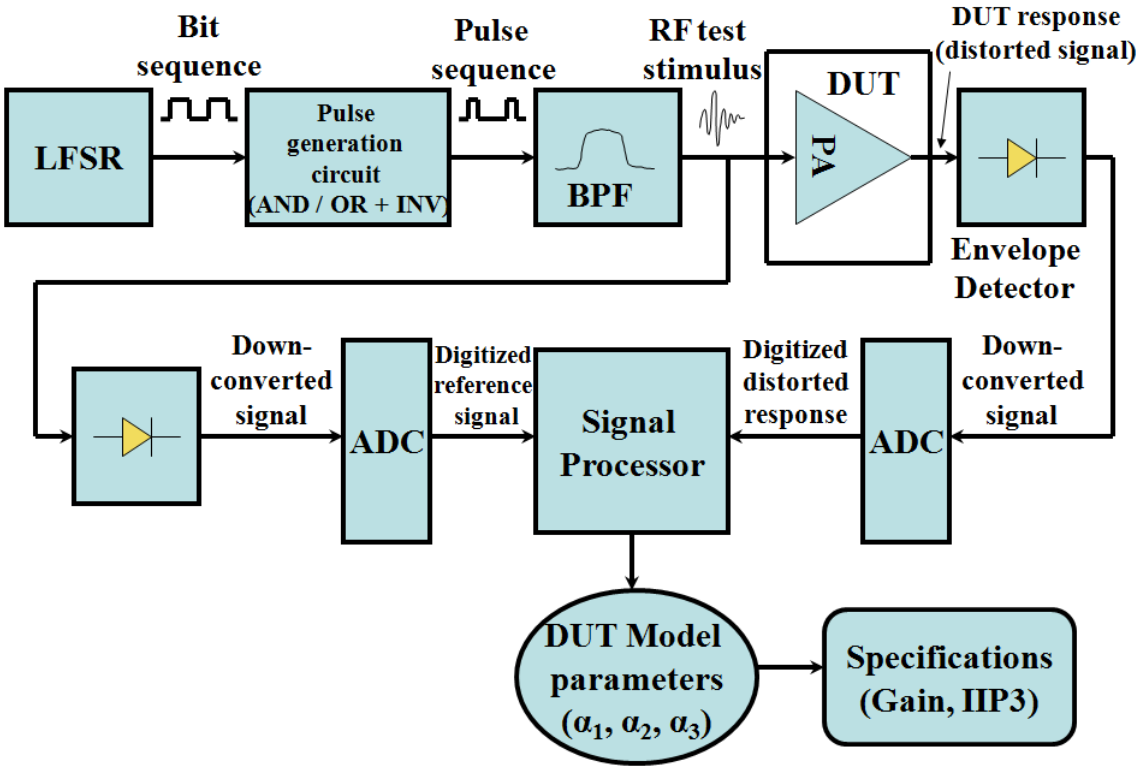


Figure 12. Pulse based testing and diagnosis framework

The test stimulus (bit stream) is generated from a Finite State Machine (FSM) or a modified linear feedback shift register (LFSR) running at relatively low frequency (200 MHz). Using the AND / OR gate and inverter configurations of Figure 8 and Figure 9, sharp pulses are generated at each positive / negative transition of the original bit signal. Note that the minimum spacing between two closest pulses is limited by the period of the original LFSR bit signal. The derived pulse stream is passed through a band pass filter

whose center frequency is 2.4 GHz. In this way RF test signal is directly generated from the digital circuit without any up-conversion and without extra hardware. The response of the DUT to this test stimulus is captured, down-converted using an envelope detector, and digitized. The golden response and the distorted response signals are captured. Based on the captured signals, the values of the model parameters (α_1, α_2 and α_3) of the RF DUT are calculated in the digital signal processor by mapping the golden reference to the distorted response through the DUT model. Finally the specifications of the RF DUT are calculated using the extracted parameter values from Equation (17) and (18).

2.8.4. Optimized pulse sequence generation using GA

The best pulse sequence for testing the RF DUT is computed using a genetic algorithm with an appropriate cost function. The candidate solution of the optimization problem is the bit sequence of the FSM or LFSR from which the pulse pattern can be derived using AND / OR gates. The cost function for the genetic algorithm is formulated such that the error in the predicted values of the model parameters (α_1, α_2 and α_3) is minimized. The block diagram of the optimization technique is illustrated in Figure 13. The genetic algorithm starts with a random population of candidate solutions (bit patterns). This bit sequence is used to calculate the DUT model parameters as shown in Figure 12. The extracted parameter values are compared with the actual parameter values found from ADS simulation. Depending on the error value, the cost metric is evaluated and a new generation of chromosomes is produced. The genetic algorithm stops when the maximum allowed simulation time is exceeded or improvement in the fitness value is no longer possible. For the optimized bit pattern, corresponding FSM can be designed very easily. From simulation it is verified that for the optimal pulse sequence, which is derived from the optimized bit sequence, the computed values of the DUT model parameters are very close to their measured values.

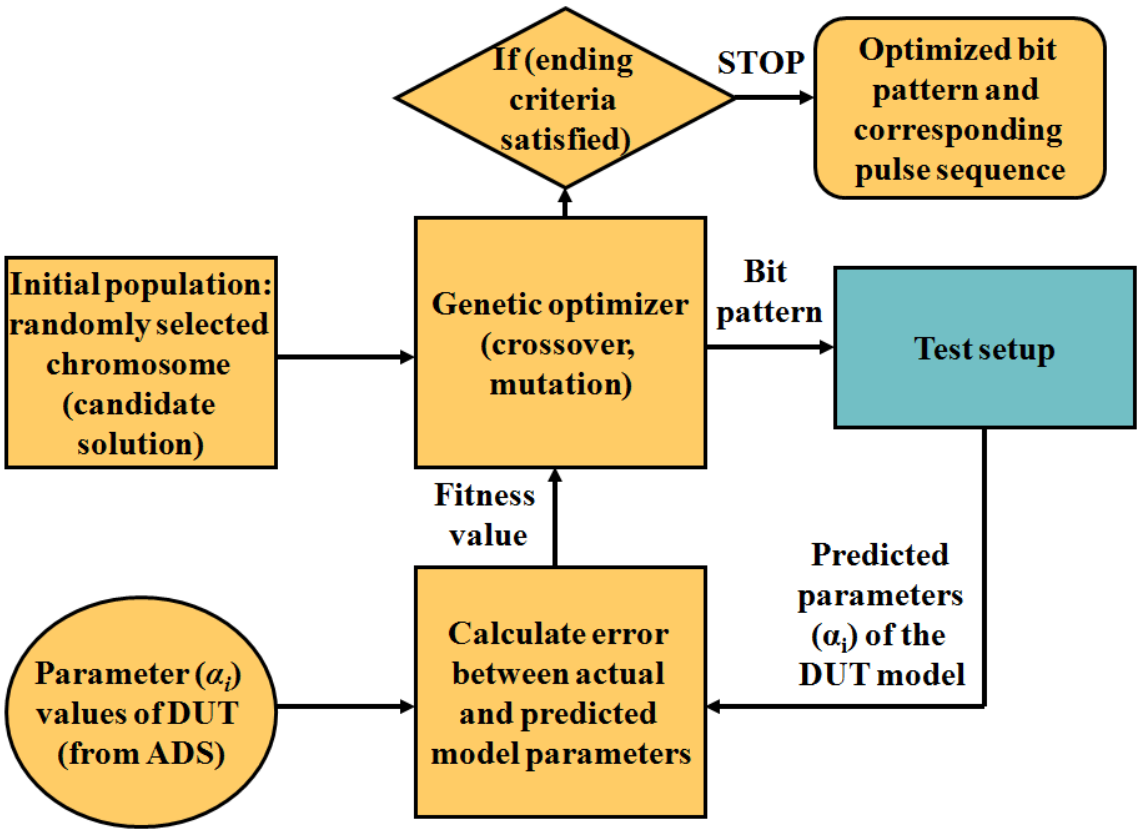


Figure 13. Optimized pulse pattern generation process

2.9. Simulation Results

An RF OFDM transceiver for 2.4 GHz carrier frequency is designed and circuit simulation is performed in Advanced Design System (ADS) and the parameter values from that simulation are used to build the behavioral model of the transceiver in MATLAB. The genetic algorithm based test generation is performed in MATLAB simulation and the optimized test signals are used for predicting the parameters of the transceiver model using the non-linear solver as described in previous sections. To introduce measurement noise in simulation, the downconverted I and Q outputs of the receiver and envelope detector response are digitized with a 10 bit analog-to-digital converter model.

2.9.1. Test generation results

Monte-Carlo simulation is performed in Advanced Design Systems (ADS) to introduce realistic process variation in the components of the transceiver. Then behavioral model parameters of those process varied instances are computed and the parameter values are used in MATLAB simulation. Some example model parameters extracted from one such instance are given here: I-Q gain mismatch = 0.06, phase mismatch = 3°, power amplifier's alpha parameters (AM-AM): α_5 = -3.89, α_4 = 19.96, α_3 = -34.07, α_2 = 16.94, α_1 = 8.95, power amplifier's beta parameters (AM-PM): β_3 = -1.62, β_2 = 3.03, β_1 = 11.89, dc offset = 150 mV. Elitism based genetic algorithm is used for test generation in MATLAB. Several process varied instances are used for test generation whose model parameters are computed using a nonlinear equation solver and minimizing computation error is defined as the objective function of GA. The performance of GA for finding optimized 64 tone test stimulus is shown in Figure 14 where the fitness function value decreases over the generations of the genetic algorithm. The genetic algorithm converged after 70 generations and the fitness function value, which corresponds to model parameter estimation error, shows almost 5 times improvement in best solution and almost 10 times improvement in mean fitness value.

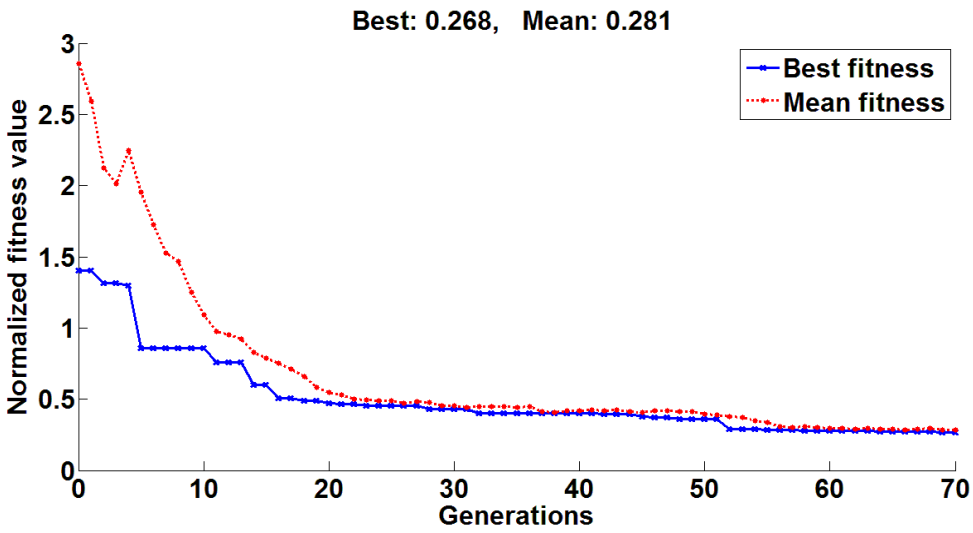


Figure 14. Convergence of the genetic algorithm while optimizing 64-tone test signal

2.9.2. Optimized test signals

Five different types of test signals are generated in simulation as explained in Section 2.6. First, optimized OFDM data frames are generated which consist of 64 orthogonal subcarriers within 20 MHz bandwidth. Amplitude and phase levels of these 64 tones are optimized by GA in such a way that parameter computation accuracy is improved. Resulting 64 tone optimized I and Q test signals are shown in Figure 15.

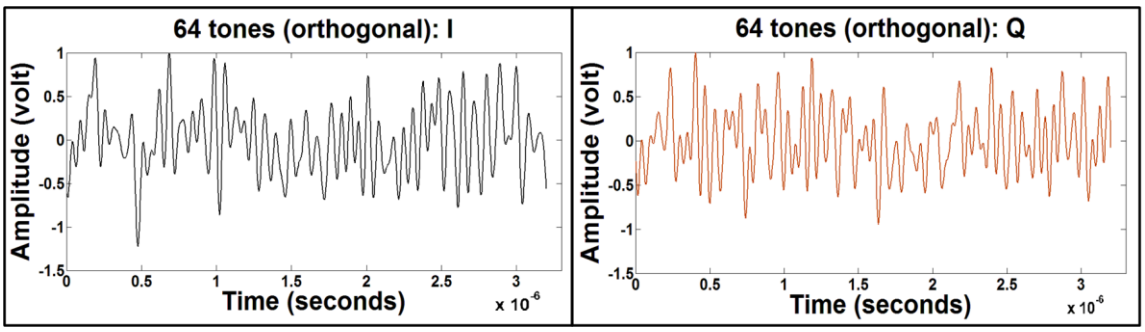


Figure 15. Optimized OFDM data frame with 64 orthogonal subcarriers

Next, GA is used to optimize the number of tones and their amplitude and phase levels in the multi-tone (orthogonal) test signal. Optimized 4 – tone test signals for I and Q inputs are obtained (shown in Figure 16) which can be used to compute model parameters of the transceiver with decent accuracy.

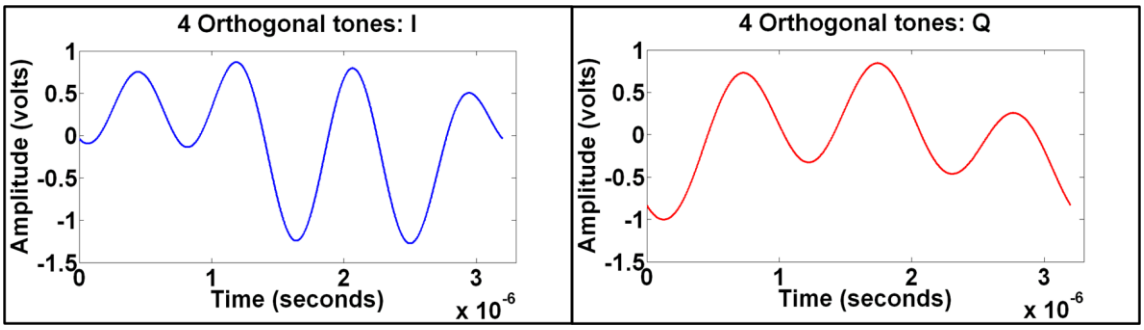


Figure 16. Optimized 4-tone (orthogonal) test signals

Then similar GA based test stimulus optimization is done for a multi-tone signal where the tones are not orthogonal to each other. Optimized 4-tone (non-orthogonal) test signals are shown in Figure 17.

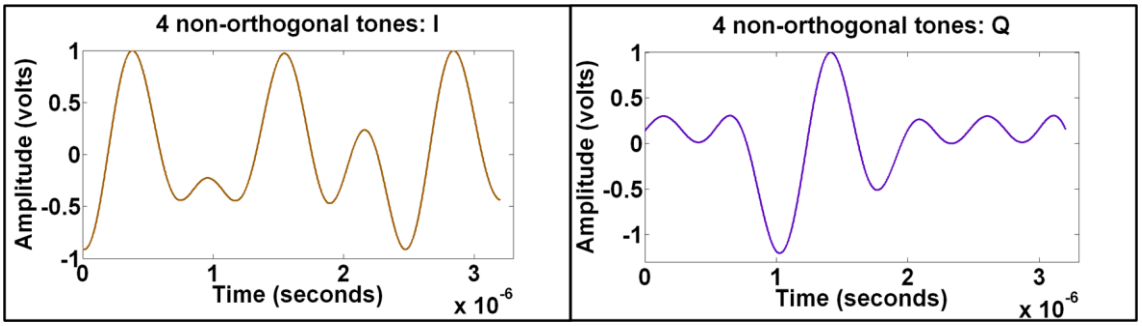


Figure 17. Optimized 4-tone (non-orthogonal) test signals

In the fourth step, optimized time domain test signals are generated for I and Q inputs (Figure 18) within the bandwidth of interest. In this case, a chromosome of genetic algorithm is a set of amplitude values corresponding to different sample time points.

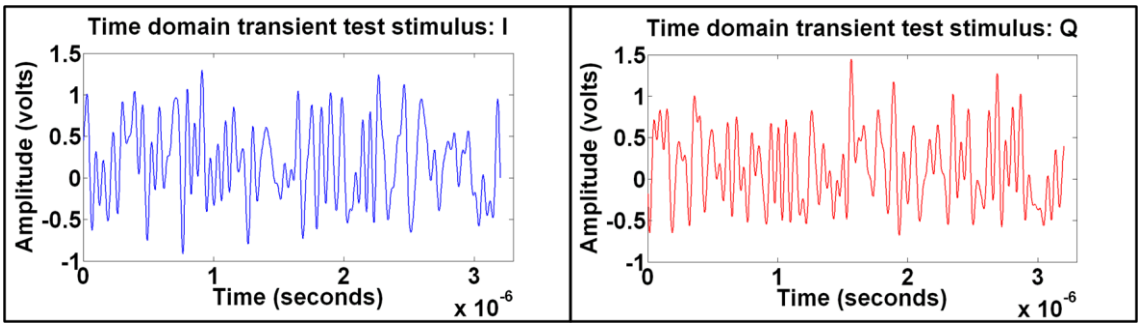


Figure 18. Optimized time domain test signal

2.9.3. Results of model parameter computation

Using Monte-Carlo simulation 50 instances with process variation are created in ADS. The optimized test signals are applied to those instances and output responses are captured. Then behavioral model parameters are computed using a MATLAB based nonlinear equation solver [47]. Computed parameters of the transceiver are I/Q magnitude and phase imbalance, Nonlinearity (AM-AM) of the PA, AM-PM and memory effects of the PA, nonlinearity of mixer and LNA and DC offset. First, the parameters of the transmitter are computed from the envelope detector output. Values of the computed transmitter parameters are used as known parameters in the second step while computing the receiver parameters from the digitized I and Q outputs. Some of the computed parameters are presented in Figure 19 which shows that the nonlinear solver can accurately compute the parameters from the output signals. In terms of parameter computation accuracy, the optimized 64-tone test signals had the best performance

compared to other optimized test signals. Maximum computation error was within 10% in this simulation. Due to the use of compact deterministic test signals, model parameter computation time was 4X-5X faster than prior parameter estimation techniques. Simulation without the envelope detector was also performed and the I-Q outputs of the receiver are used for computing model parameters. In this case, nonlinearity of the whole transmitter and the whole receiver were computed accurately, but module level (mixer, PA, LNA) diagnosis suffered from loss of accuracy and increase in computation time.

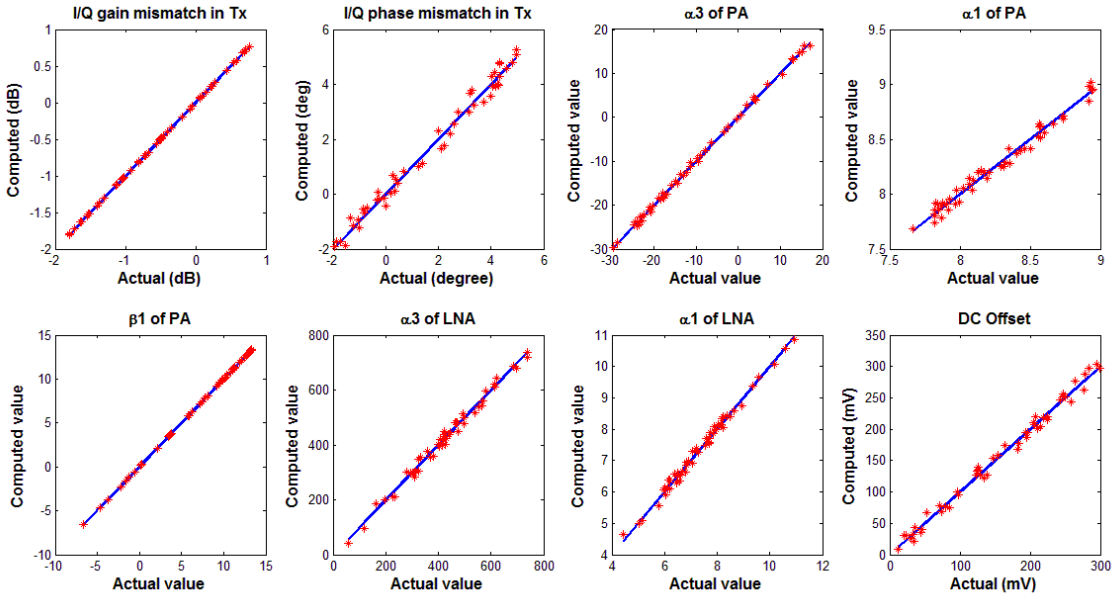


Figure 19. Results of parameter computation

2.9.4. Results of pulse based diagnosis and testing

Circuit simulations performed in Advanced Design System (ADS) are utilized to build behavioral model of the Power Amplifier. Using the model of power amplifier extensive simulation is done in MATLAB to validate the proposed concept of test

generation using optimized pulse sequences. The whole test setup starting from FSM / LFSR and pulse generation circuit to envelope detector and ADC are simulated in MALAB with the DUT (PA) model and the parameters of the DUT are predicted by fitting the reference signal to the distorted DUT response as illustrated in Section 2.8.

The optimized pulse sequence is found using elitism based Genetic Algorithm and the optimization process converges after 250 generations. After convergence of the genetic algorithm, the value of the fitness function for the best candidate solution is found to be 0.0498 which implies that the prediction error is very small for this optimized test input. The optimized pulse pattern that is derived from the bit sequence obtained by the genetic optimizer is shown in Figure 20.

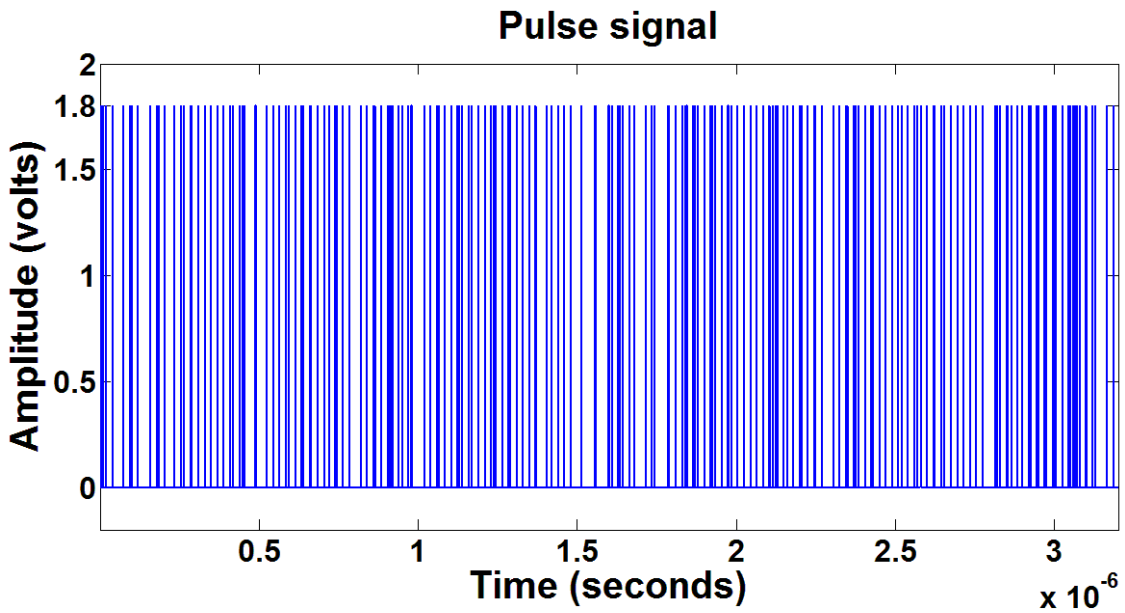


Figure 20. Optimized pulse sequence

The optimized pulse sequence of Figure 20 consists of several frequency components extending from DC to RF. The multi-frequency characteristic of the optimized pulse sequence is utilized to produce a multitone test signal at 2.4 GHz which

is used to test the RF DUT. The multitone test stimulus is obtained from the digital pulse sequence by band pass filtering it at 2.4 GHz. The frequency domain characteristic of the filtered high frequency test stimulus is shown in Figure 21. This multi-tone test signal is directly applied as a test input to the RF DUT. From the down-converted and digitized response of the DUT, the model parameters and the gain and IIP3 specifications of the RF PA are computed using Equations (17) and (18). The predicted specifications of the device show excellent correlation with its original specifications.

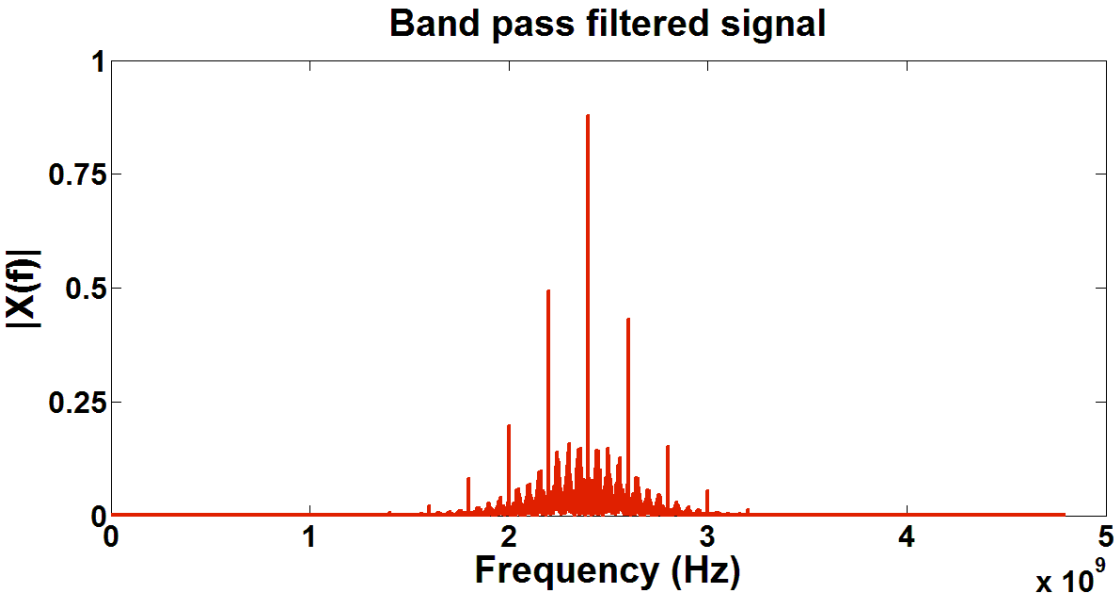


Figure 21. Band pass filtered test stimulus derived from pulse signal

The specifications obtained using the optimized pulse sequence is compared with the specifications predicted using a random pulse sequence for 50 instances. In both of the cases, gain prediction is perfect and is evident from figure 22. However IIP3 computation with the optimized pulse sequence is superior to that computed using the random pulse pattern which is shown in Figure 23. This comparison proves the necessity of optimizing the pulse sequence using the proposed test optimization procedure.

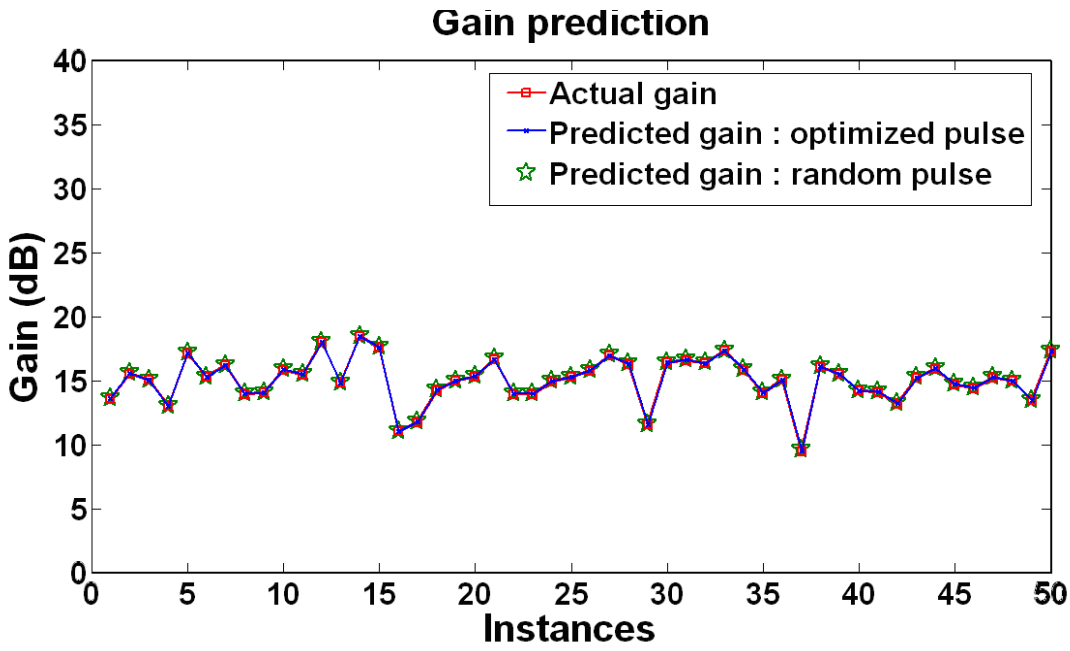


Figure 22. Gain prediction using optimized pulse sequence and a random pulse sequence

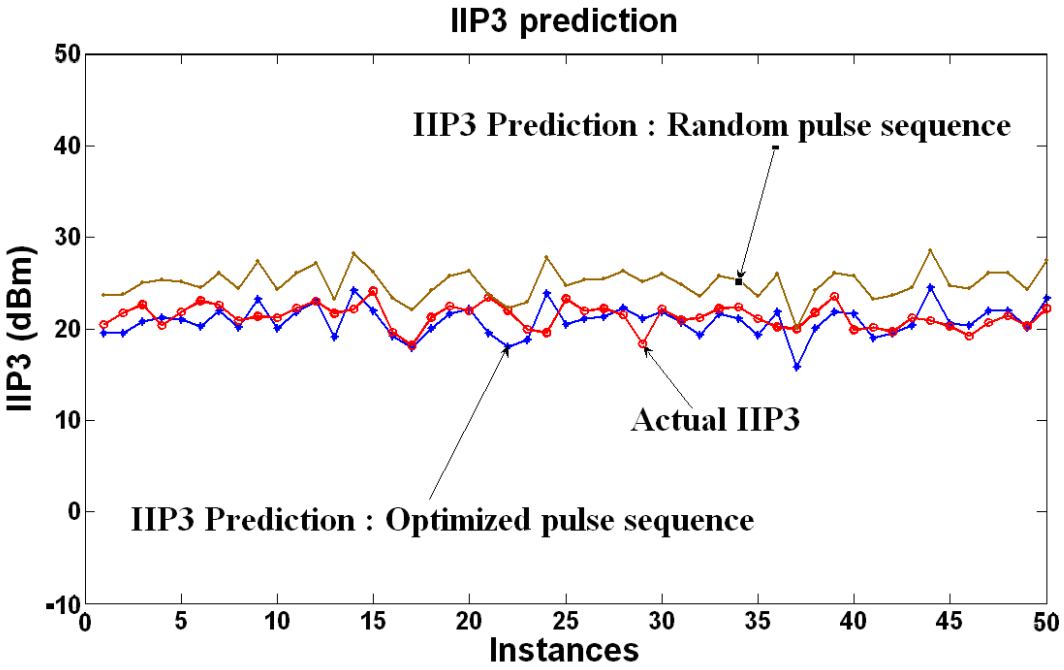


Figure 23. IIP3 prediction using optimized pulse sequence and a random pulse sequence

Performance of a clock signal running at 2.4 GHz for computing the gain and IIP3 specifications is also compared with that of the optimized test signal. As before, the gain computation perfectly matches with the original gain values as shown in Figure 24. However, the IIP3 computation plot of Figure 25 clearly demonstrates that the optimized pulse sequence is far better than the clock signal for determining IIP3 values.

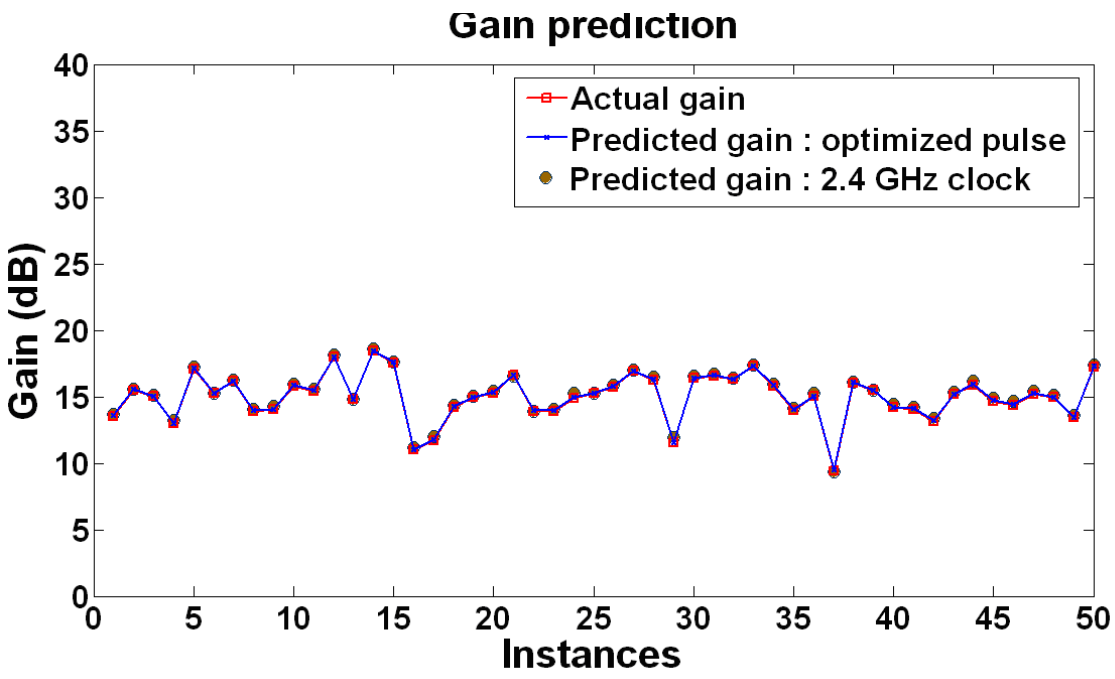


Figure 24. Gain prediction using optimized pulse sequence and clock signal running at 2.4 GHz

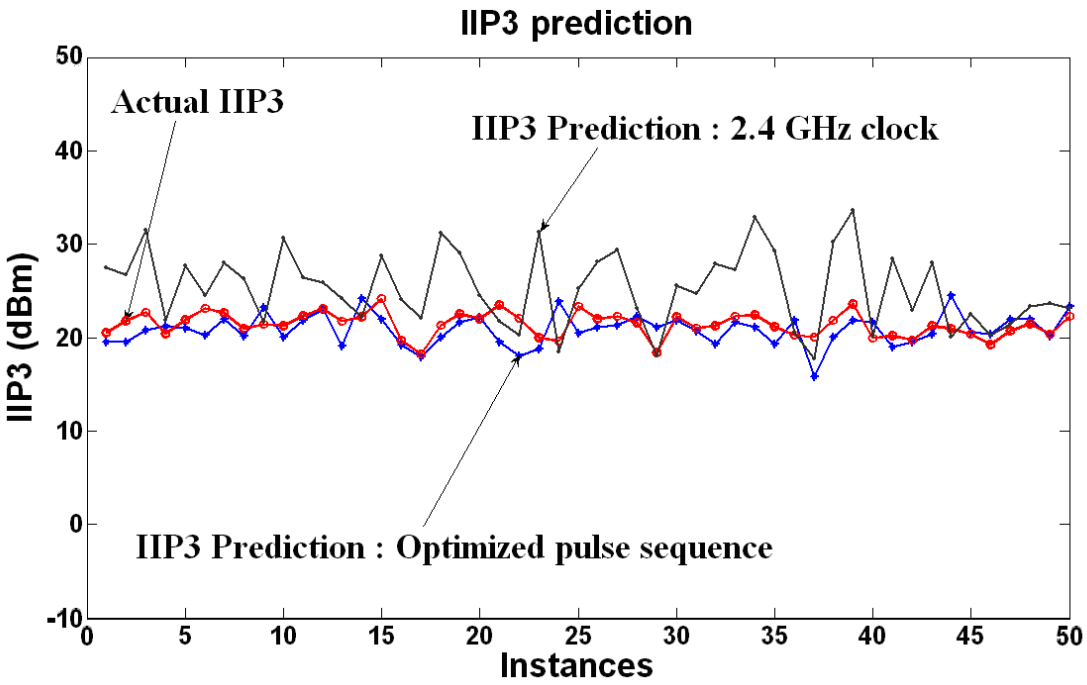


Figure 25. IIP3 prediction using optimized pulse sequence and clock signal running at 2.4GHz

Table 1 shows the error values in the prediction of the PA model parameters for three different cases - optimized pulse sequence, a random pulse sequence and a clock running at 2.4 GHz.

Table 1. Error values for different input test stimuli

Input	Optimized pulse sequence	Random pulse sequence	Clock @ 2.4 GHz
Average error (in predicted alpha values)	0.0498	0.2211	1.7835

2.10. Experimental Validation

To demonstrate the validity the proposed approach experiments are performed on hardware prototypes. Two hardware experiments are done on two different setups and the results of the hardware experiments are shown below:

2.10.1. Hardware experiment 1

The first experimental setup is shown in Figure 26. Power amplifiers manufactured by Texas Instruments are used as DUT (device under test). Power amplifier instances from different process corners are used in this experiment. A data acquisition module by National Instruments (NI PXIe-1073) is used to interface the RF front-end with PC. The optimized test signal is applied through the digital to analog converter of the data acquisition module. The test signal is up-converted to 2.4 GHz by a mixer from Maxim (MAX2041) and applied to the power amplifier instances. Output of the power amplifier is down-converted by a mixer (MAX2041) and captured by the digitizer of the data acquisition module. LO signals of 2.4 GHz are generated by an RF signal generator (Agilent E4432B) and power supply and bias of power amplifier and mixer are generated from Keithley 2400 dc supplies.

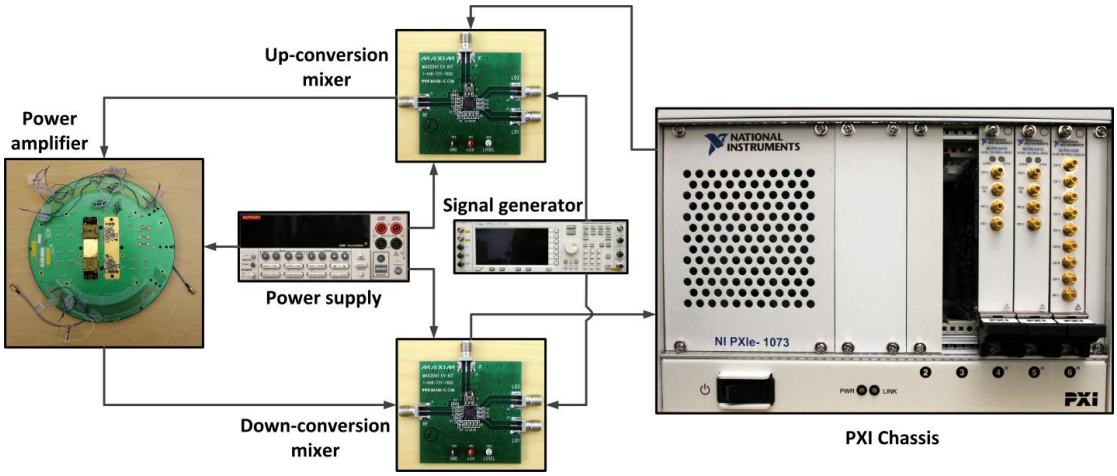


Figure 26. Experimental setup 1 for model parameter computation based diagnosis

Optimized multitone test signals are applied to the behavioral model of the experimental setup where the power amplifier nonlinearity is assumed to be of fifth order. Nonlinearity of the power amplifier instances are computed using the nonlinear equation solver in such a way that the simulated output matches with the test response captured by the data acquisition module. Input vs. output nonlinearity of a particular PA instance is shown in Figure 27 where it can be seen that the computed model parameters match closely with actual nonlinearity characteristic.

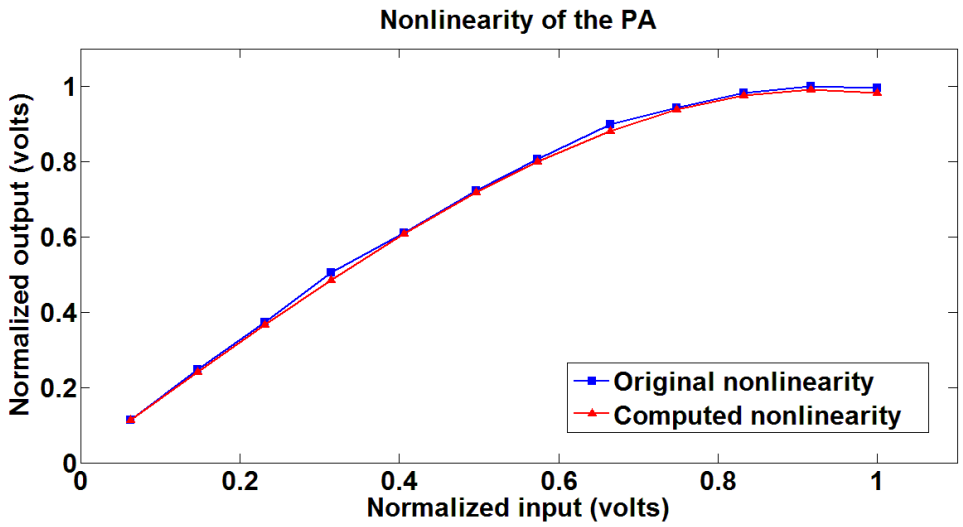


Figure 27. Nonlinearity computation from hardware experiment

From computed input-output nonlinear characteristics of 8 power amplifier instances, their gain and IIP3 specifications are calculated quite accurately which are shown in Table 2.

Table 2. Gain and IIP3 computation from hardware experiment 1

Instance	Original gain (dB)	Computed gain (dB)	Original IIP3 (dBm)	Computed IIP3 (dBm)
1	13.39	13.50	2.10	2.84
2	14.37	14.18	5.15	5.40
3	5.48	4.81	2.09	1.93
4	12.37	12.34	0.71	0.77
5	13.88	13.13	5.69	5.76
6	13.32	13.96	2.59	2.96
7	16.39	16.65	2.18	2.27
8	11.22	10.91	4.42	4.67

2.10.2. Hardware experiment 2

The second hardware setup is shown in Figure 28. A data acquisition module by National Instruments (NI PXIe-1073) is used to interface the RF front-end with PC. The optimized multitone test stimulus is up-converted by a mixer RF2638 by RFMD. The upconverted signal passes through a power amplifier (MAX2247) followed by a low noise amplifier (RF2370) connected in loopback. The LNA output is downconverted by another mixer MAX2039. Results of the hardware measurements are shown in Table 3.

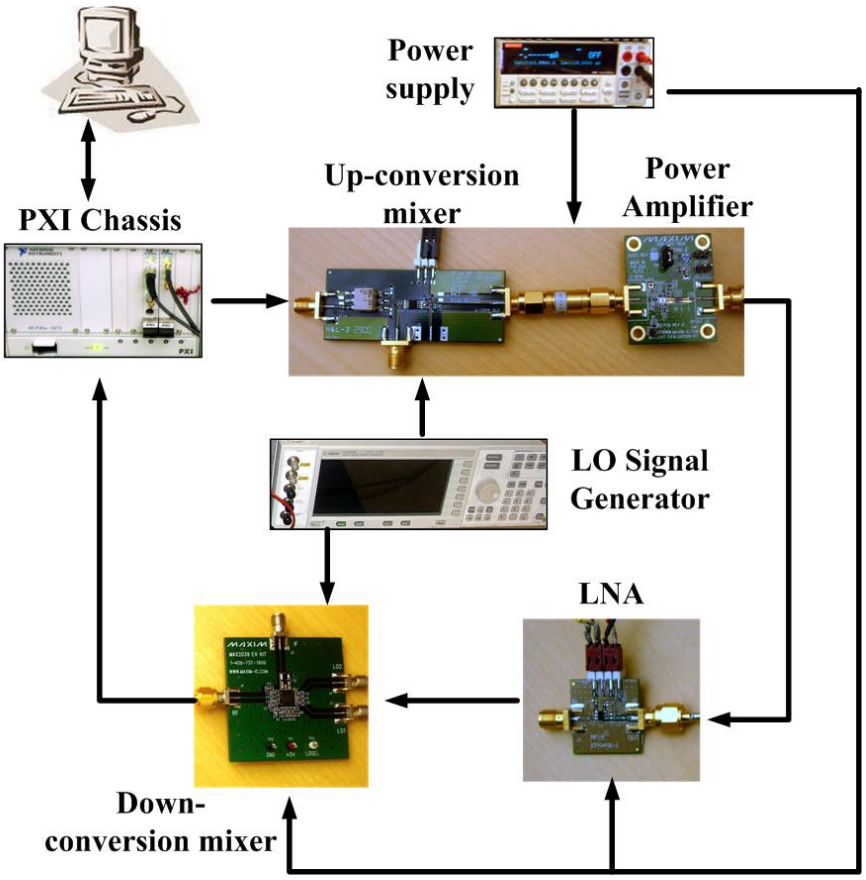


Figure 28. Experimental setup 2 for model parameter computation based diagnosis

Table 3. Error in specification computation in 2nd hardware experiment

Specifications	PA gain	PA IIP3	LNA gain	LNA IIP3
Average error	5.85%	11.72%	4.61%	9.88%

CHAPTER 3

ADAPTATION FOR PROCESS VARIATION TOLERANCE IN RF SYSTEMS

In this chapter digitally assisted process variation tolerant adaptation technique for RF systems is discussed that uses the diagnosis results of Chapter 2. An adaptation / tuning algorithm is developed that efficiently finds out optimal settings of the tuning knobs of the individual modules of the RF system and trades off performance and power in such a way that overall system level performance requirements are met with least amount of total power consumption.

3.1. Prior Work

There has been significant work in the past on digital calibration techniques that compensate for nonlinearity in RF circuitry [51]-[56]. Digital calibration is performed through the use of a predistortion filter in the transmitter or a postdistortion filter in the receiver whose coefficients are calibrated via application of dedicated multitone tests or transmitted/received symbol measurements. In addition to digital techniques, analog tuning can also be performed by adjusting capacitor/inductor values or bias currents and voltages of the analog modules of a mixed-signal/RF system (performing analog and digital tuning concurrently gives the best results). In [14], a technique for predicting the "best" tuning knob values directly from the results of alternative test measurements is described. Another approach to perform post-production calibration is described in [25].

An attractive way to perform post-manufacture testing and tuning of RF circuits and systems is to use software running on the baseband DSP to activate and control built-in testing and tuning of the complete RF system [22]-[23], [57]-[60]. Typically, the method of [14] is used to predict the initial values of the (digital and analog) tuning knobs

of the circuit. Then, starting with these initial tuning knob values, either a *Gradient* based [22] or *Augmented Lagrange* based [23] search/optimization engine is used to iteratively *tune the module level performances* until *system-level performance metrics* are satisfied at minimum power cost. At each step of the iterative procedure, an alternate test [28]-[29] is used to predict system level specifications from test response data. Such test response data is obtained from sensors [61] inserted into the RF datapath and from looped-back RF response data. All of the test activation and tuning knob control functions are performed by software running on the baseband DSP. In [24] and [62] tuning is driven by similar test-tune-test mechanisms. However, the tuning algorithms are simplified to the point that they can be controlled by minimal additional circuitry on the RF chip rather than by software running on the baseband DSP. Some loss of yield recovery is traded off for simplicity of design. Another approach for tuning RF circuits using parameter estimation with optimal power consumption is presented in [63]. Some other examples of prior research in process variation tolerant analog / RF circuits include an integrated mm-wave self-healing power amplifier [3]-[4], a 60 GHz power amplifier with adaptive feedback bias control [5], a power amplifier with a varactor based digital calibration technique [6], a self-healing image reject mixer [10], a self-healing LNA with bias control [13], digitally assisted pipelined ADC [15] and a dual loop PLL with self-calibration technique [19]. It should be noted that prior to application of any tuning procedure, it is first necessary to determine if the system is free from "catastrophic" defects. It is assumed that a "defect filter" [64] is used to filter out such devices that can not be tuned and devices that are not defective are passed on for further tuning.

3.2. Key Contributions

Key contributions of the proposed adaptation technique are listed below:

(a) The proposed yield-improvement/tuning method requires only a single test application at 5 tuning knob settings. Tuning is performed iteratively. However, through the use of two-level hierarchical behavioral models, it is not necessary to apply the test for each iteration of the tuning procedure as with the algorithms of [22]-[23] and [57]-[60]. This saves test time.

(b) The method of [14] allows the best tuning knob values to be predicted directly from the observed alternate test response. However, the underlying supervised learners need to be trained across a more diverse set of process corners for RF systems as opposed to the individual devices of [14]. Obtaining devices at such process corners for training of the supervised learners is difficult and time-consuming. For the same reason, performance/power prediction at process corners of the RF system can be inaccurate as well. Instead, the proposed approach decomposes the problem into tuning knob vs. performance vs. power modeling problems for the RF modules individually. Power and performance prediction for individual modules (as opposed to the whole transmitter) reduces dimensions of the tuning problem. This reduction in dimensions results in (i) testing at less number of knob settings which saves time, (ii) improvement in accuracy of predicted power - performance models at module level and (iii) usage of simple quadratic models for power-performance prediction technique which does not require any training as opposed to [14]. System level performance is then determined by composing the performances of the individual modules of the complete RF system.

It should be noted that the relationships between the tuning knob values for each RF module and its performances as well as power consumption are functions of the process corner (or process point) corresponding to that module. In the proposed approach, quadratic models are used to capture this dependence for each individual RF module (as opposed to the complete RF system - a difficult problem). These models are then used during the tuning process to drive the search for the best tuning knob values that meet performance while minimizing power consumption.

3.3. Overview of Proposed Tuning Approach

In this section the core tuning ideas are illustrated using a transmitter as a test case (the receiver can be tuned using a similar procedure). The key steps involved in the proposed approach are shown in Figure 29.

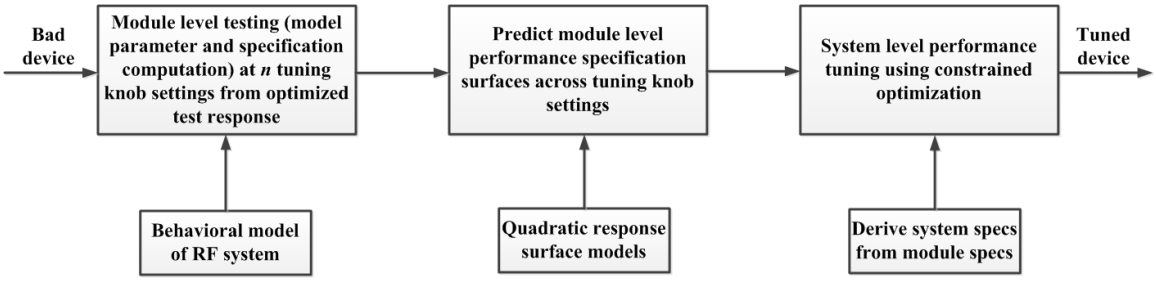


Figure 29. Overview of the proposed tuning approach

The steps involved in the proposed tuning approach are explained below:

(1) The first step is a top-down analysis step. A comprehensive behavioral model of the transmitter is built and an optimized test stimulus is generated for which the correlation between the model parameters and output waveform is maximized. The optimized multitone test is applied to the transmitter from the baseband unit and the response (output signature) from the envelope detector (placed at the output of the transmitter) is captured. A nonlinear least squares fitting algorithm is used to determine the behavioral model parameters of the mixer and power amplifier from the simulated model in such a way that the model output is consistent with the test response waveform. In this way, module level diagnosis is performed at 'n' different tuning knob settings (n is 5 in this case) where $n \ll m$ [m is the total number of tuning knob settings of the transmitter]. These 'n' tuning knob settings are determined by performing D-optimal Design of Experiments (DoE). From the computed model parameters, performance specifications (gain, IIP3) of the modules are found at those 'n' tuning knob settings.

Also from the sensors attached to the power supply, power consumptions of the modules are found at the 'n' tuning knob settings. This step of module level diagnosis is explained in detail in Section 3.5.

(2) In the second step, quadratic models are used to represent performance surfaces (gain, IIP3, power) of the modules (mixer, PA) of the transmitter instances across all tuning knob settings. Coefficients of the quadratic models for every process varied instance are found from the 'n' test results of step (1) using Response Surface Methodology (RSM). This step is explained in Section 3.6.

(3) A constrained optimizer is then used to optimize the mixer and power amplifier tuning knob values so that system level (transmitter) performance metrics are satisfied and power is minimized. It is possible to do this from knowledge of the performance vs. power vs. tuning knob relationships for the mixer and PA individually (obtained from step (2)) and the manner in which transmitter performance and power consumption are related to mixer and power amplifier's performance and power consumption. This bottom-up analysis step is explained in Section 3.7.

3.4. Adaptation Framework

The proposed adaptation framework for the self-healing transmitter is shown in Figure 30. Power amplifier and mixer of the transmitter have multiple adaptation settings that can be controlled from the baseband unit to trade-off their performance and power consumption. On-chip sensors are attached to the modules for sensing how performance and power change with process variation and adaptation settings. An envelope detector is attached to the output of the power amplifier that captures the low frequency envelope of the modulated signal. Current sensing of mixer and power amplifier is done by attaching sensors to the power converter modules as shown in [65]-[66]. Optimized test signals are generated that facilitate accurate diagnosis of the modules by model parameter

computation method as explained in Section 3.5. These optimized test stimuli are applied from the baseband unit and response of the system is captured by the envelope detector. From the envelope response, model parameters of mixer and power amplifier are computed as described in Section 3.5 and from current measurement data from current sensors, power consumption of individual modules are calculated. This procedure is repeated '*n*' times and computed model parameters and power consumption are used to predict performance specification and power consumption of mixer and PA of the particular transmitter instance across all tuning knob settings as explained in Section 3.6. The predicted power and performance surfaces are used by the tuning control algorithm to find out optimal tuning knob settings for mixer and PA such that system level performance requirements are met with minimum power consumption as shown in Section 3.7.

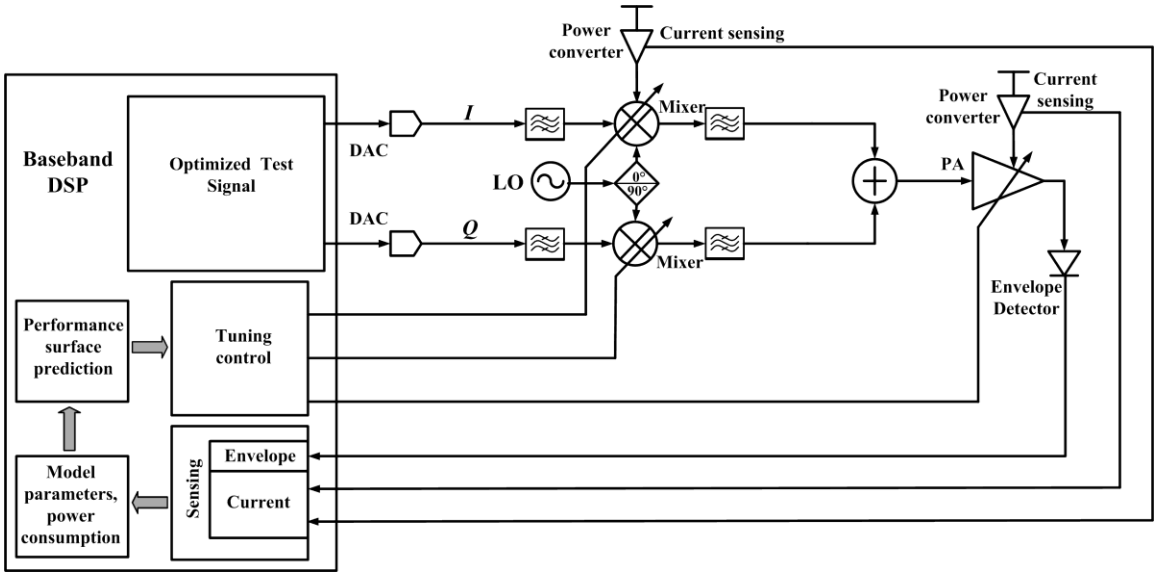


Figure 30. Adaptation framework for RF transmitter

3.5. Top-Down Diagnosis by Test Generation and Parameter Computation

In this section the key concepts involved in diagnosis (step 1 of the proposed approach as described in Section 3.3) are explained. This top-down diagnosis technique is same as the diagnosis method described in Chapter 2.

3.5.1. Behavioral model of the transmitter

A comprehensive behavioral model of the RF transmitter is built including critical non-idealities such as: *I-Q gain and phase mismatch, 3^{rd} order nonlinearity of the mixer, AM-AM (5^{th} order) and AM-PM (3^{rd} order) distortion of the power amplifier*. Details of the behavioral models are given in Section 2.5. Specifications of the modules are computed from their behavioral models using standard relations such as Equation (17) and (18).

3.5.2. Optimized test stimulus generation

Optimized multi-tone test signals are generated that facilitate accurate computation of behavioral model parameters of the mixer and PA from the test response of the transmitter captured by the envelope detector. Flowchart of the test generation process is shown in Figure 31. Detailed description of this test generation technique is given in Section 2.6.

3.5.3. Model parameter computation based diagnosis

Using a nonlinear equation solver, behavioral model parameters of mixer and power amplifier are computed for every process shifter transmitter instance in such a way that the simulated response of the model to the optimized test signal matches with the actual response of the transmitter instance. This method of model parameter computation is explained in Section 2.7.

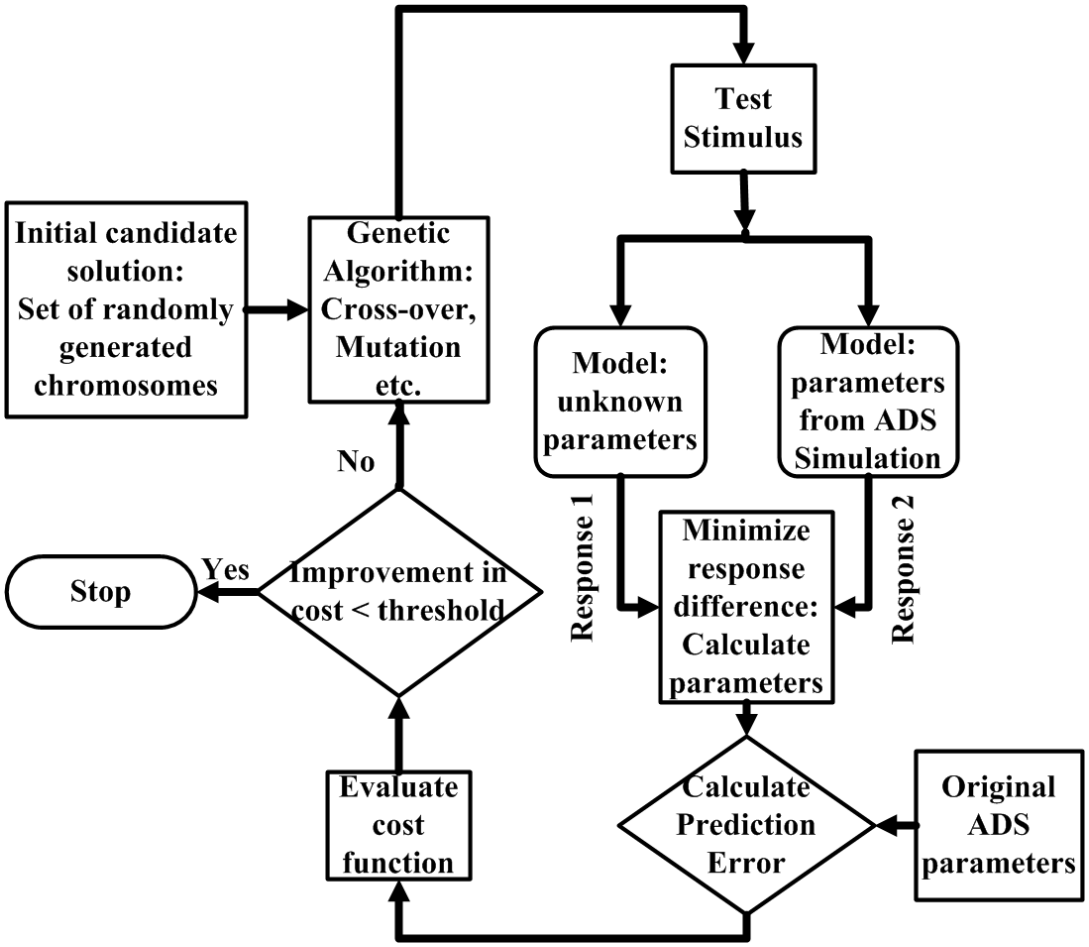


Figure 31. Test generation for model parameter computation

3.6. Prediction of Performance Specification Surfaces

In presence of process variation, relation between specification (S_i) and tuning knob (T_j) of a component changes from its nominal relation. This functional relation can be expressed as $S_i = f_k\left(T_1, T_2, ..., T_j\right)$, where S_i is the i^{th} specification of interest, $\left\{T_1, T_2, ..., T_j\right\}$ are the tuning knobs of the device and f_k is the functional relation between specification S_i and tuning knobs for k^{th} process varied instance. Due to process variation, this function f_k changes from one instance to other and knowledge of this

functional relation for every instance is required if that instance has to be tuned successfully.

In the proposed approach, it is assumed that some basic knowledge of the functional relationship between tuning knob and specification is available from design phase. Depending on the pattern how specifications change with tuning knobs, a particular type of response surface model can be used. For simulation and hardware experiments presented here, quadratic models without interaction terms are used. Another approach is presented in Section 3.10 which targets the situation when no prior knowledge is available regarding specification surfaces or when variation of specification is much more complex.

A process varied device instance is tested at few specific tuning know settings (5 knob settings for a quadratic model) and from the test results model parameters and performance specifications of individual modules of the instance are computed. Then from those computed values, performance specifications of individual modules are predicted across all tuning knob settings using Response Surface Methodology (RSM). Finally the tuning solution is found by running constrained optimization on the predicted performance surfaces. In this section the theory behind selection of specific tuning knob settings for testing and performance specification surface prediction are explained.

D-optimal design of experiments are performed in order to select the tuning knobs where the device should be tested so that the performance surfaces can be predicted accurately. Design of Experiments (DoE) are used in scientific observation to obtain maximum information about the studied object while minimizing the number of experiments [67]. In this work, the objective is to obtain information about the performance specifications of the device across all tuning knobs and also the number of tests has to be minimized in order to reduce test cost and test time. In DoE, there are two types of variables – factors and responses, where factors are the input variables of the experiment and responses are the outcomes of experiments. In this case, tuning knob

settings where the device is tested are factors and test results (computed model parameters and performance specifications at those tuning knob settings) are responses.

An optimized test stimulus is generated in such a way that using that test signal behavioral model parameters of the device can be computed accurately as explained in Section 2.7. For every device, this process of model parameter computation is repeated '*n*' times at '*n*' different tuning knob settings. In this step, model parameters of individual modules of transmitter and receiver (mixer, PA, LNA) are computed separately as explained earlier. Then from those computed model parameters critical performance specifications (gain, IIP3) of those modules are found using standard relations. Power consumption at those knob settings are obtained from current sensors attached to the power converters for those modules. Then by using "Response Surface Methodology" (RSM) [68], performance specifications and power consumption across all tuning knob settings are predicted for individual modules. For Response Surface Methodology, different kind of models can be used such as linear model, linear model with interaction terms, quadratic model and quadratic model with interaction terms. In this work, quadratic models without interaction terms are used to model gain, IIP3 and power surfaces across tuning knob settings of individual modules as shown below:

$$y_i = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 \tag{31}$$

where y_i is a particular performance specification of the device, x_1 and x_2 are two tuning knobs of that module and β_j are the coefficients of the quadratic performance model. Number of terms in this model can be reduced if the dropped terms do not have any significant effect on the performance surface.

In this case, objective of the DoE is to find out different (minimum) set of values for x_i s for the experiment (testing the device). For those chosen set of values of x_i s, equation (31) can be written in matrix form as:

$$y = X\beta + \varepsilon \tag{32}$$

where X is the design matrix whose number of rows equals number of tuning knob settings where the device is tested and number of columns represents number of coefficients in the model (5 in this case) and ε is the random part of the model. Least square solution of equation (32) gives:

$$\hat{\beta} = \left(X^T X\right)^{-1} X^T y \tag{33}$$

where $\left(X^T X\right)$ is the information matrix. Now the objective of D-optimal Design of Experiments is to form the design matrix X in such a way that the determinant of the information matrix $\left(\left|X^T X\right|\right)$ is maximized. This implies that the experiments span the largest volume possible in the experimental region [67]. D-optimal design gives lower number of experiments (test points in this case) compared to other DoE techniques. In this work, MATLAB based coordinate exchange algorithm is used for D-optimal design and QR factorization is used for computing the least square solutions of quadratic model coefficients.

Key benefits and critical aspects of the proposed performance surface prediction process are listed below:

- Instead of predicting the performance specification surfaces of the whole transmitter, performance specification surfaces of mixer and power amplifier are predicted separately by decoupling their behavioral model parameters from system response as explained earlier. By decoupling performance specification surfaces of individual modules the complexity of the problem is reduced. If mixer has x number of tuning knobs and the PA has y number of tuning knobs ($x = y = 2$ in this case), then each specification of the transmitter will have $(x + y)$ number of independent variables and $2(x + y) + 1$ number of terms in its quadratic response surface model without interaction terms. It means that outcome of D-optimal DoE will contain at least $2(x + y) + 1$ experiments and the transmitter has to be tested at $2(x + y) + 1$ tuning knob

settings. On the other hand, if model parameters and performance specifications of mixer and power amplifier can be decoupled, then mixer and PA will have $2x+1$ and $2y+1$ number of terms in their quadratic models. Hence testing has to be performed at $2x+1$ number of tuning knob settings (if $x \geq y$) or $2y+1$ number of tuning knob settings (if $y \geq x$) which is much less than the number of tests needed without decoupling. It should be noted that this reduction in number of tests is made possible by the fact that running a single experiment (test) on the transmitter, results of experimental outcome (model parameters and performance specifications) of mixer and PA are obtained simultaneously when tuning knob settings of the mixer and the PA are selected from their respective design matrices (found by performing DoE separately for mixer and PA). Also by reducing the number of variables in the model, simplified performance specification surfaces are predicted more accurately.

- Number of tests and number of terms in the model can be increased for more accurate prediction at the cost of longer testing time. In simulation and hardware experiments of this work it is observed that a quadratic model (without interaction terms) with minimum number of experiments (equals number of terms in the model) can accurately represent the specification surfaces of the modules that are used.

- The fact that though performance specification surfaces change due to process variation, the basic patterns remain same in most of the cases, is utilized here by using models of fixed complexity (quadratic). If a particular specification increases with a particular tuning knob, then in most of the cases this increasing trend will be maintained, but the absolute value of the specification and the rate of change will vary from instance to instance which can be captured by a model of a fixed order. This obviates the need to use regression training for model building for different instances and simplifies the prediction method.

3.7. System Specification Tuning

The tuning process can be formulated as an optimization problem where solution in terms of tuning knob values can be found by minimizing the difference between nominal specifications and specifications of the tuned circuit. But for efficient performance of the tuned circuit, power consumption should be considered as well by ensuring that tuning has least impact on power consumption. In this work, a power conscious tuning approach is taken where bounds are assigned for different specifications and the objective function is defined as the power consumption of the whole transmitter which is to be minimized.

It should be noted that if the specifications of the individual components of the transmitter are tuned considering their individual nominal values it will result in acceptable specifications of the whole transmitter. But that solution may not be optimal in terms of power consumption. Another solution may exist for which tuned specifications of individual components are different from their nominal values but overall system specifications are satisfactory and this solution may result in less amount of power consumption compared to component level tuning in a particular process varied instance. To find out the optimal solution, specifications of the whole system are to be considered during constrained optimization. Transmitter gain, IIP3 and power consumption can be computed from the specifications of mixer and power amplifier using following relations:

$$Gain_{(TX)} = Gain_{(Mixer)} * Gain_{(PA)} \tag{34}$$

$$\frac{1}{\left(A_{IP3(TX)}\right)^2} = \frac{1}{\left(A_{IP3(Mixer)}\right)^2} + \frac{\left(Gain_{(Mixer)}\right)^2}{\left(A_{IP3(PA)}\right)^2} \tag{35}$$

$$Power_{(TX)} = Power_{(Mixer)} + Power_{(PA)} \tag{36}$$

In the proposed constrained optimization problem, gain and IIP3 specifications of the tuned transmitter have to remain within bounds for successful tuning and at the same

time power consumption of the whole system is minimized as much as possible. Following equations illustrate the formulation of the constrained optimization:

$$Gain_{nom} - Tol_{gain} < Gain_{(TX)} < Gain_{nom} + Tol_{gain} \tag{37}$$

$$IIP3_{nom} \leq IIP3_{(TX)} \tag{38}$$

$$Minimize\left(Power_{(TX)}\right) \tag{39}$$

Equations (37)-(38) specify the constraints while Equation (39) is the optimization objective function. Tol_{gain} represents the tolerance limit on both sides of gain from its nominal value and $Spec_{nom}$ is the nominal specification. Equation (38) signifies that the tuned IIP3 has to be equal or greater than its nominal value. But Equation (37) shows that for gain, bounds are specified on both sides of its nominal value. It ensures that the tuned gain does not become too high because for a very high gain the output amplitude can go beyond the linear operating region of the system saturating the signal.

3.8. Simulation Results

Simulation results of the different steps of the proposed tuning approach are presented in this section.

3.8.1. Behavioral model of transmitter

A two-stage power amplifier is designed in ADS with CMOS 0.18 μm technology. A double balanced Gilbert cell architecture is used for implementing the mixer. The tuning knobs for power amplifier are two bias voltages. On the other hand, supply voltage and bias are used as tuning knobs for the mixer. Monte-Carlo simulation is performed in ADS to create process variation. The input-output characteristics of the instances are imported to MATLAB and behavioral models are built.

3.8.2. Test stimulus optimization

Total error in model parameter computation is defined as the cost function for test stimulus generation as shown in Section 2.6. Figure 32 shows this fitness value (parameter computation error) vs. number of generations of the genetic algorithm which converges after 70 iterations. Multi-tone test stimuli are generated for the I and Q inputs of the transmitter where test time for each of the optimized stimuli is 3.6µs.

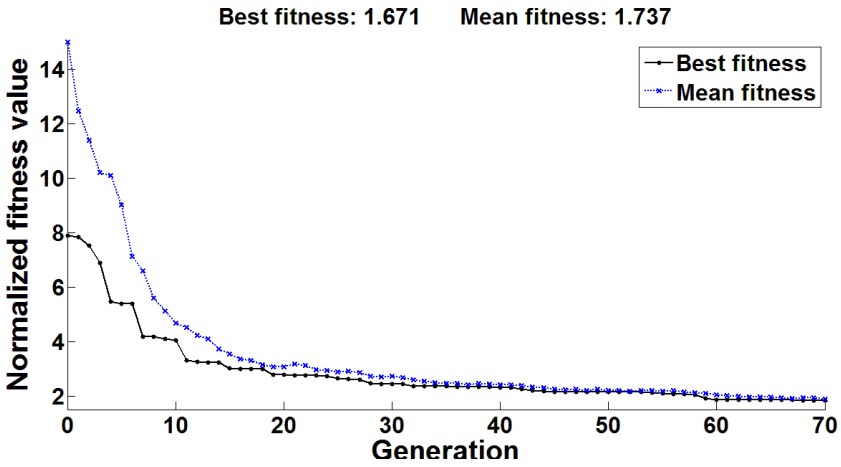


Figure 32. Convergence of genetic algorithm

3.8.3. Model parameter computation

A MATLAB based nonlinear equation solver [47] is used for computation of model parameters using the optimized test stimuli. The parameters that are computed are I/Q gain and phase mismatch of transmitter, all coefficients of 5^{th} order nonlinearity of the PA, coefficients of AM-PM distortion of the PA and coefficients of the 3^{rd} order nonlinear model of the mixer. Figure 33 shows some of the computed model parameters. From these computed model parameters, performance specifications of individual modules are calculated.

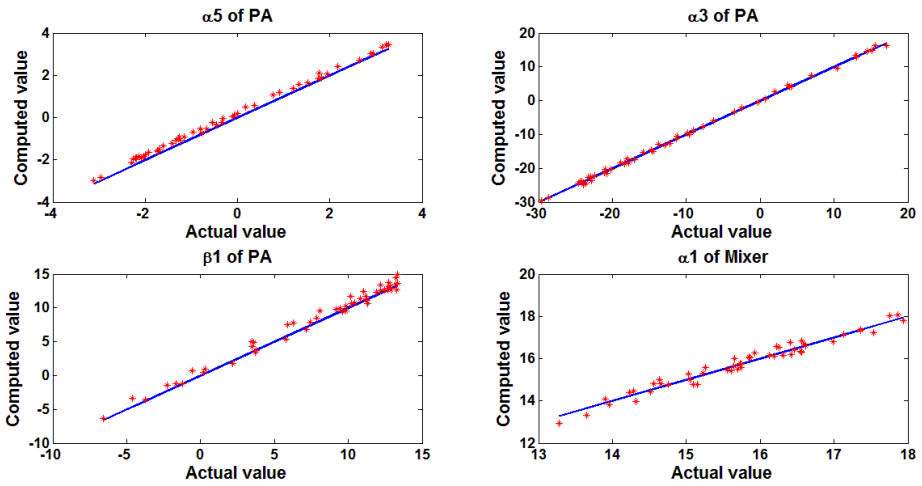


Figure 33. Accuracy of parameter computation

3.8.4. Performance specification surface prediction

The computed model parameters and current consumption data of the mixer are used to build and predict its gain, IIP3 and power surfaces while power amplifier's model parameters and current consumption data are used for PA's specification surface prediction using quadratic models and Response Surface Methodology. The original and predicted surfaces for different specifications of mixer and PA of a particular transmitter instance are shown in Figure 34.

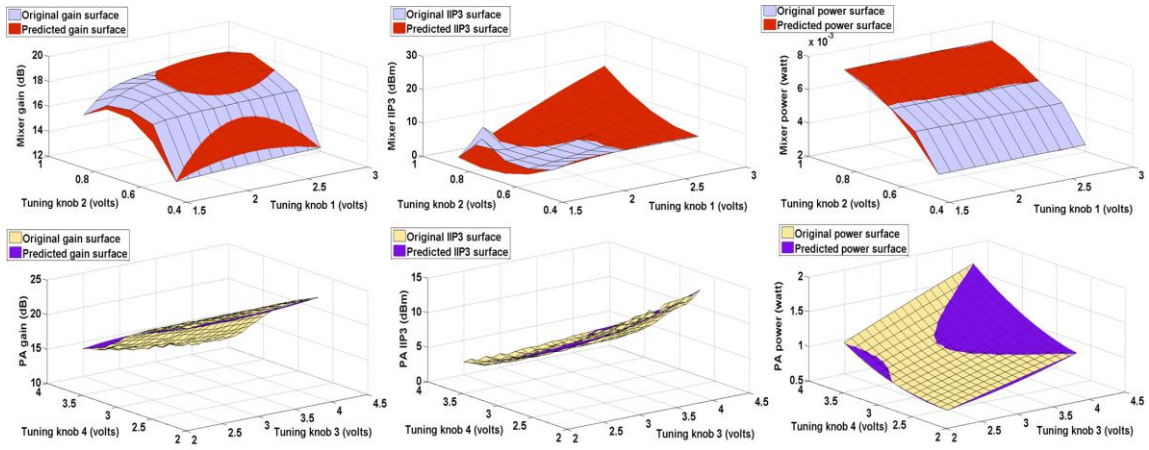


Figure 34. Specification surface prediction of mixer and power amplifier

3.8.5. Constrained optimization

Using the predicted specification surfaces of mixer and power amplifier of the transmitter instances, the optimal tuning knob settings are found by using a MATLAB based constrained minimization tool (different from the non-linear equation solver). Nominal gain of the transmitter is 46 dB and a bound of 3dB is placed on both sides. For IIP3, a device is considered as a good device if the IIP3 is greater than -4dBm. Gain, IIP3 and power distribution of 880 instances before and after tuning and bound on these specifications are shown in Figure 35. For this particular simulation setup and introduced process variation, an overall yield improvement of 29.8% is obtained.

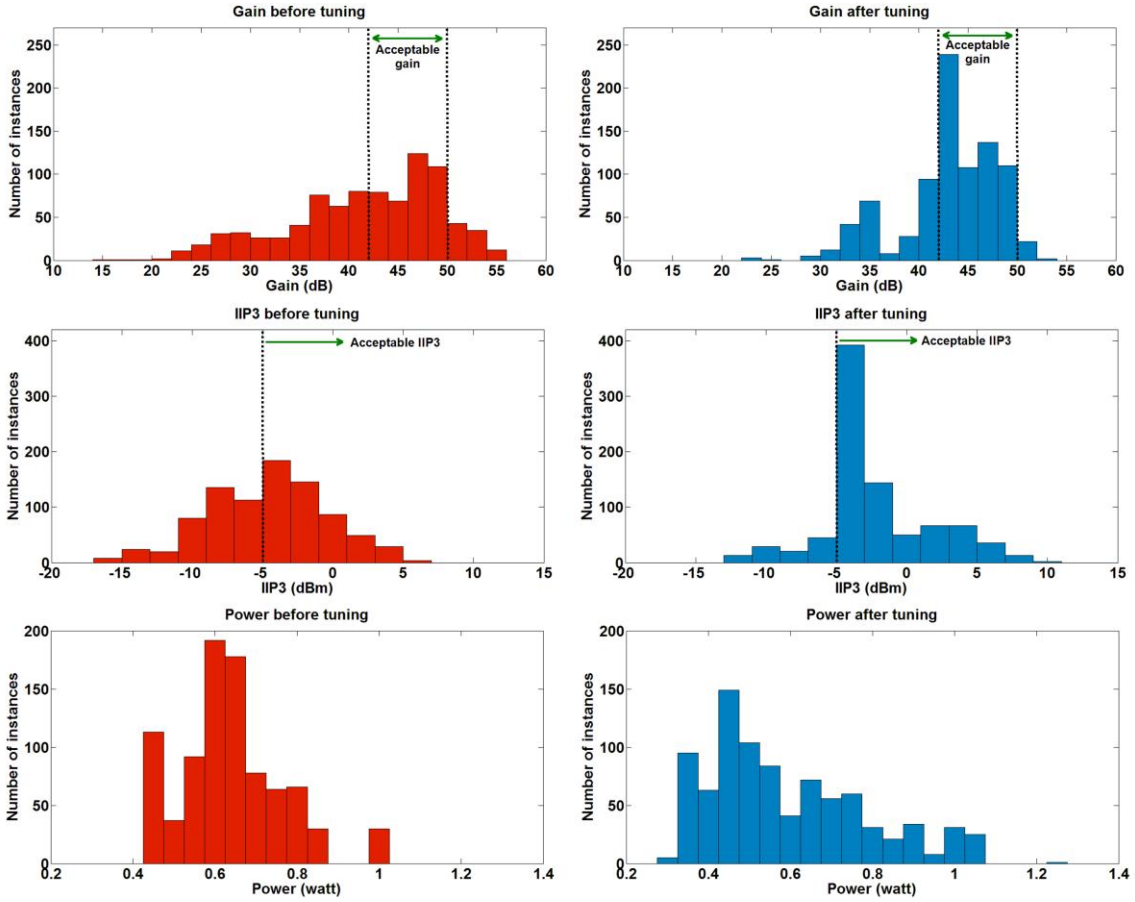


Figure 35. Specifications of the transmitter before and after tuning

3.9. Experimental Validation

The validity of the proposed tuning technique is validated by performing an experiment on a hardware prototype of a transmitter. The hardware setup is shown in Figure 36. A 802.11 a/b/g RF PA in production at Texas Instruments is used in the experiment. Power supply (V_{cc}) and control voltage ($V_{control}$) of the PA are used as tuning knobs which affect gain, IIP3 and power consumption of the PA. Tuning range for both of the tuning knobs are from 2.6 volts to 3.8 volts. A data acquisition module by National Instruments (NI PXIe-1073) is used to interface the RF front-end with PC. The optimized test signal is applied through the digital to analog converter of the data acquisition module. The test signal is up-converted to 2.4 GHz by a mixer from Maxim (MAX2041) and applied to the power amplifier instances placed on the tester board. LO signal of 2.4 GHz is generated by an RF signal generator (Agilent E4432B). Low frequency envelope of the output of the power amplifier is captured using an envelope detector and then digitized by the digitizer of the data acquisition module. V_{cc} and $V_{control}$ of power amplifier and supply voltage of mixer are generated from Keithley 2400 dc supplies. Power supplies that set the tuning knobs (V_{cc} and $V_{control}$) are controlled from the PC via GPIB controller.

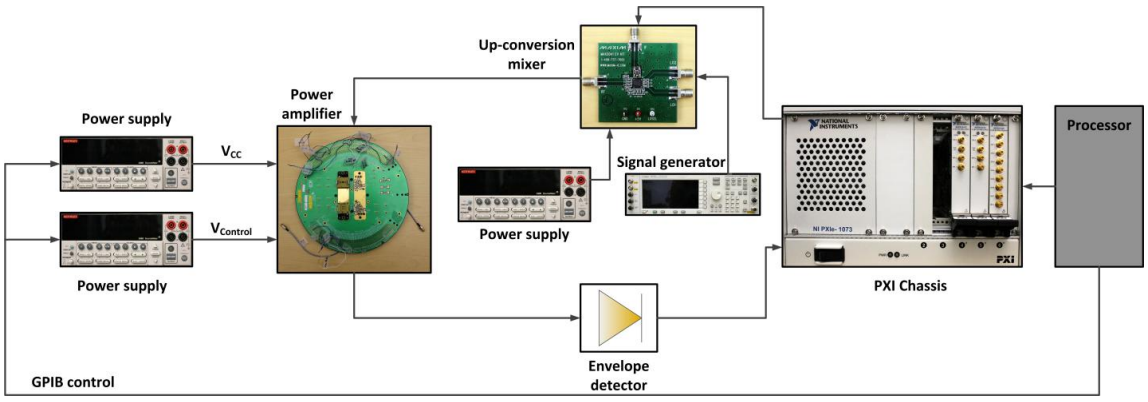


Figure 36. Hardware experimental setup for transmitter tuning

Nominal gain of the transmitter is 11 dB and a guard band of 0.3 dB applied on both sides which implies that to be considered as a good instance the transmitter should have a gain between 10.7 dB and 11.3 dB. On the other hand, IIP3 of the transmitter has be greater than 5 dBm for successful tuning. Figure 37 shows original and predicted gain and power surfaces of a particular process varied instance with tuning knob settings. It can be observed from Figure 37 that the predicted surfaces follow the original surfaces quite closely.

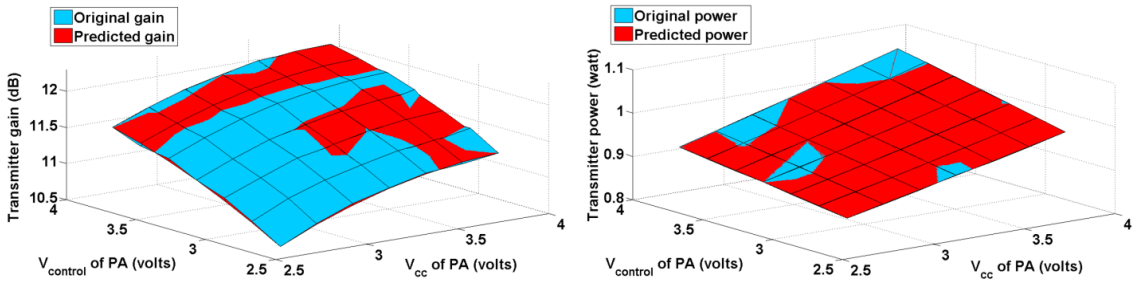


Figure 37. Gain and power prediction of transmitter

The proposed tuning technique is applied to the transmitter setup with 16 process varied power amplifier instances. Results of the tuning are shown in Table 4. Out of the 16 bad instances, 14 are tuned successfully (instances 1 to 14) and two instances (instance 15 and 16) failed to meet specification requirements after tuning as they did not have enough tuning range in their specification space. In Table 4, performance specifications that did not meet the requirements are highlighted in grey.

Table 4. Tuning results from hardware experiment

Instance	Gain before tuning (dB)	IIP3 before tuning (dBm)	Power before tuning (watt)	Gain after tuning (dB)	IIP3 after tuning (dBm)	Power after tuning (watt)
1 (✓)	8.56	7.14	0.92	10.72	6.68	1.03
2 (✓)	9.31	0.80	0.93	11.02	5.39	1.02
3 (✓)	10.78	4.41	0.95	10.74	5.90	0.97
4 (✓)	7.21	0.39	0.89	10.77	5.72	1.01
5 (✓)	8.38	1.15	0.90	11.21	6.40	1.04
6 (✓)	8.94	0.36	0.94	10.74	5.18	1.01
7 (✓)	10.77	3.45	0.95	10.76	5.89	0.98
8 (✓)	9.09	0.87	0.92	10.80	5.24	1.00
9 (✓)	8.70	0.49	0.94	10.83	5.03	1.04
10 (✓)	8.64	1.18	0.90	10.96	5.71	1.02
11 (✓)	9.12	1.11	0.92	10.94	5.16	1.02
12 (✓)	9.07	0.81	0.93	10.89	5.31	1.03
13 (✓)	7.95	8.81	0.97	10.72	6.23	1.04
14 (✓)	11.10	0.79	0.95	10.83	5.06	1.00
15 (×)	8.51	5.63	0.98	9.84	5.12	1.05
16 (×)	9.45	1.33	0.87	9.80	4.39	1.08

3.10. Alternative Technique for Performance Surface Prediction

An alternative technique for predicting performance specification surfaces of the individual modules of the transmitter is shown in this section. This technique is applicable to the situation when no prior knowledge of the relation between specification and tuning knob is available or the relation is complex. Here instead of assuming a fixed quadratic model of the performance specification surfaces, Multivariate Adaptive Regression Splines (MARS) [30] is applied for building the models using training instances.

3.10.1. Overview of the approach

The key steps involved in the proposed approach are shown in Figure 38 and Figure 39 and explained below:

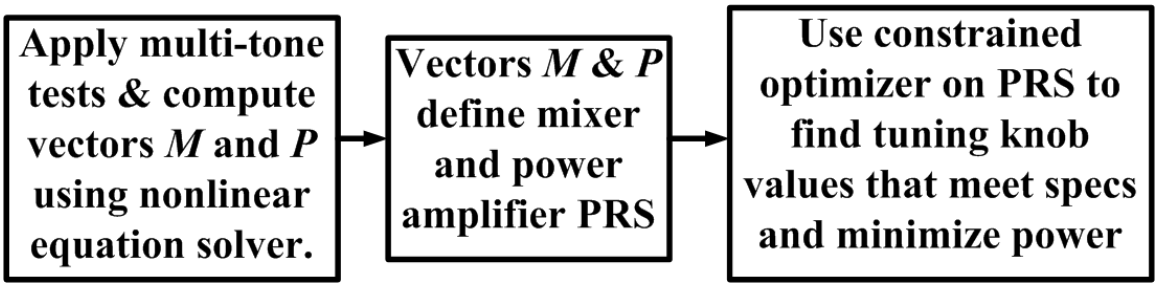


Figure 38. Overview of the alternative tuning approach

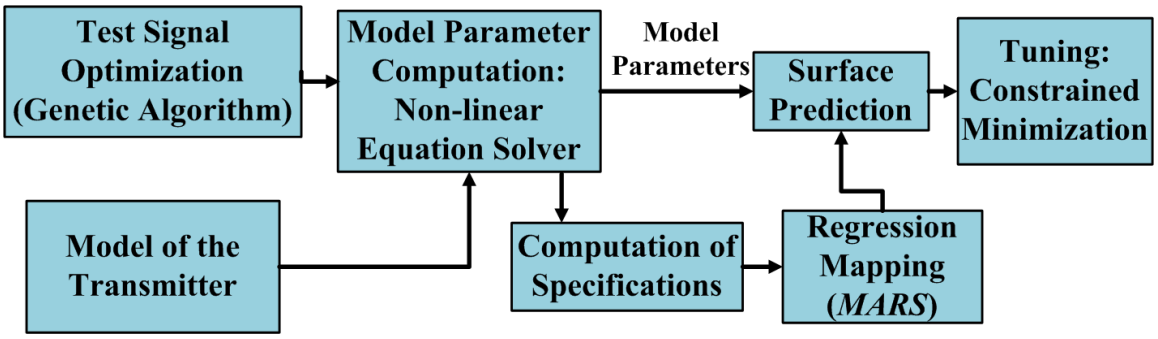


Figure 39. Steps involved in the alternative tuning technique

(a) The top-down diagnosis step involving optimized test signal driven model parameter computation is explained earlier in Chapter 2. This diagnosis is performed for nominal as well as two other tuning knob settings - minimum possible values of all tuning knobs and maximum values of all tuning knobs. In total, 3 tuning knob settings across the 4 tuning knobs for the mixer and PA combined are used: nominal and two extreme settings. Let the behavioral model parameters of the mixer computed for the 1st, 2nd and 3rd tuning knob settings be given by the vector $M = [m(1), m(2), m(3)]$ for a specific DUT and the behavioral model parameters of the PA computed for the 1st, 2nd and 3rd tuning knob settings be given by the vector $P = [p(1), p(2), p(3)]$ for the same

DUT. The *m(i)* and *p(i)* are vectors of behavioral model parameters for the mixer and power amplifier respectively diagnosed from the multitone test application for i^{th} tuning knob setting. The vectors *M* and *P* uniquely and accurately quantify where the mixer and the power amplifier are in their respective manufacturing process spaces. By considering them independently, across-die as well as within-die process variations are taken into account. For a nominal device, the vectors *M* and *P* will have nominal behavioral model parameter values. For a DUT at a process corner, the distance of the obtained vectors *M* and *P* from their nominal value will be very large. Furthermore, for different process corners, their vector values will be different. Hence, the step of computing the vectors *M* and *P* can be thought of as "process detection" for the mixer and the power amplifier, respectively.

(b) Regression models are built that map the vectors *M* and *P* across multi-parameter process perturbations to the specifications of the mixer and power amplifier, respectively, for any given combination of tuning knob values of the same using a set of "training" devices sampled from the process space. Subsequently, for any specific DUT lying in an arbitrary point within the process space, any performance specification (and power consumption) of the mixer or PA can be computed for any of the allowed (discretized) tuning knob values. Such a mapping that allows the specs and the power consumption of the RF modules to be predicted for any given value of *M* or *P* is called performance response surface prediction for the mixer or PA since the *n*-dimensional (*n* is the number of tuning knobs) surface of a particular specification is predicted using a regression mapping.

(c) A constrained optimizer is then used to optimize the mixer and power amplifier tuning knob values so that system level (transmitter) performance metrics are satisfied and power is minimized as explained in Section 3.7.

3.10.2. Performance response surface prediction

Prediction of performance response surface (PRS) of mixer and PA of a transmitter instance is performed from the knowledge of its position in the process space. Model parameters of an instance computed at particular tuning knob settings are used for identifying the unique position of that instance in its process space ('process detection'). Process detection for mixer and PA of each transmitter instance is performed by computing their model parameters at three tuning knob settings: nominal, maximum and minimum values of tuning knobs (*M* and *P* vectors as explained in Section 3.10.1). Then a regression mapping is built between the computed model parameter set (*M* vector for mixer and *P* vector for power amplifier) and specifications at all possible tuning knob settings (PRS) separately for mixer and PA of the instances. Multivariate Adaptive Regression Splines (MARS) [30] is used for constructing the regression mapping function from the knowledge of *M* and *P* vectors and corresponding PRS of the training instances. PRS prediction is performed for 3 critical specifications of mixer and power amplifier: gain, IIP3 and power consumption. Once the regression function is built, PRS of mixer and power amplifier of a DUT can be predicted from their computed model parameter set in the evaluation phase. Important aspects of this surface prediction process are listed below:

- Instead of predicting the specification surfaces of the whole transmitter, PRS of mixer and power amplifier are predicted separately to reduce the complexity of the problem. If mixer has *X* tuning knob settings and power amplifier has *Y* tuning knob settings, then for predicting the PRS of the whole transmitter, specifications at (*X***Y*) tuning knob settings have to be computed which complicates the process of construction and evaluation of the regression model and reduces the prediction accuracy. On the other hand, when separate surfaces are built for mixer and power amplifier, total (*X*+*Y*) specification values are required. Also, a better tuning solution is obtained by effectively decoupling a component from the other.

- Theoretically, the surface prediction can be performed using the model parameters computed at nominal tuning knob setting only. But in that case less number of variables are available to identify the process and the aliasing probability will be higher. 'Aliasing' implies the effect of different process variations being mapped to a single set of model parameters and hence similar surface prediction for all of them. The aliasing probability reduces as the number of variables used to identify the process instance increases. Hence, usage of more number of tuning knob settings for model parameter computation results in better process detection at the cost of increased test time. In this work, three tuning knob settings are used for model parameter computation (the nominal knob setting, all tuning knobs at their minimum values and all knobs at their maximum values) so that enough information can be obtained for process detection without significantly increasing the test time. The choice of minimum and maximum values for tuning knob settings can be justified by the fact that those are the corner points in the specification surface and distance of those points are maximum from nominal which is generally close to the middle point of tuning knob range. These three knob settings effectively cover the whole specification surface.
- Though specification surface changes due to process variation, the basic pattern remains same in most of the cases. When the regression model is built, it "learns" about the pattern of the surfaces from the training instances. This knowledge helps it to effectively predict the surfaces of other instances in the evaluation phase.

3.10.3. Simulation results

Design of mixer and PA is done in ADS and the results are imported to MATLAB to build the behavioral models. The computed model parameters of the mixer and PA are used to build and predict their gain, IIP3 and power surfaces respectively. 100 instances of mixer and PA are used for training MARS. The original and predicted surfaces for different specifications of mixer and PA are shown in Figure 40. Using the predicted

specification surfaces of mixer and power amplifier of the transmitter instances, the optimal tuning knob settings are found by using a MATLAB based constrained minimization tool and results of tuning are shown in Figure 41. For this particular simulation setup and introduced process variation, an overall yield improvement of 27.86% is obtained. The yield improvement results shown here and in Section 3.8.5 not only depend on the type of models (quadratic vs. regression based), but also number of tuning knob settings used for testing the device (5 for quadratic model and 3 in this case) which determine the accuracy of specification surface prediction.

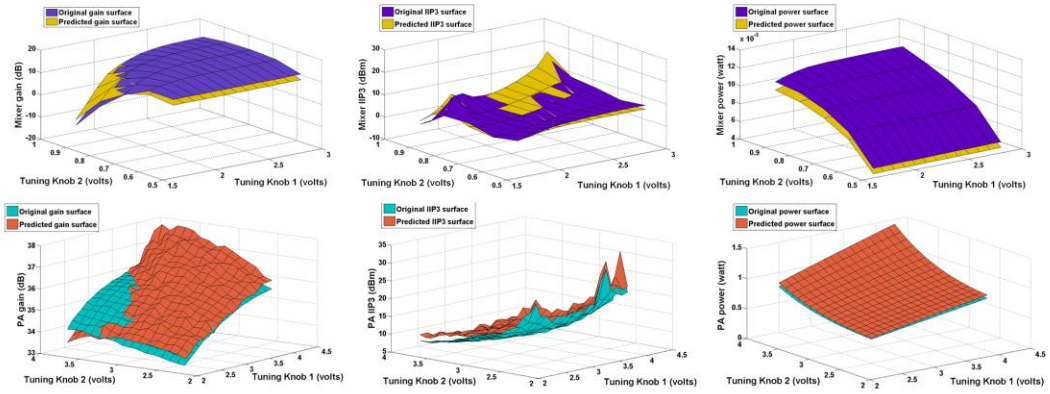


Figure 40. Specification surface prediction for the alternative tuning approach

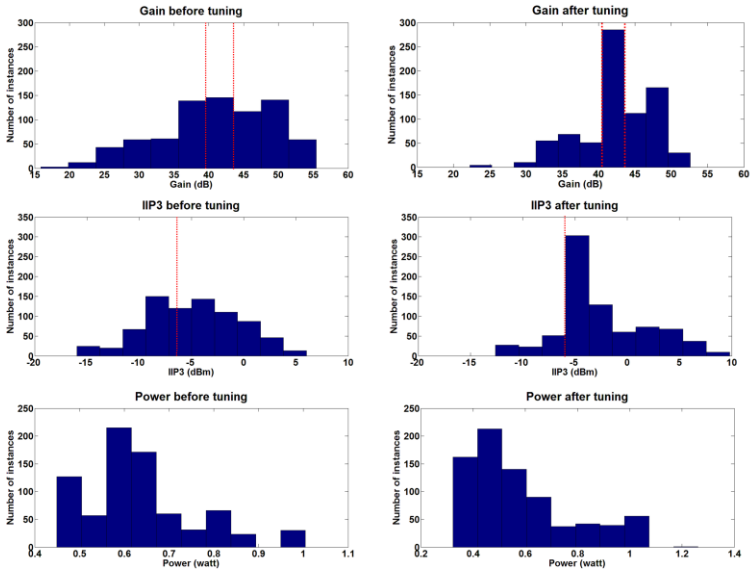


Figure 41. Specifications of the transmitter before and after tuning (alternative approach)

3.10.4. Experimental validation

A 802.11 a/b/g RF front end (PA/LNA) in production at Texas Instruments is used in the experiment A quadrature modulator AD8349 from analog devices is used for up-converting the baseband signal. An RF source (Agilent E4432B) is used to generate a 2.4 GHz Local Oscillator signal for up-conversion. The up-converted output from AD8349 is fed into the tester board provided by TI. A set of 8 instances of the 802.11 a/b/g front-end is used in this experiment. The PA is set to operate at 2.4 GHz and the supply voltage of the PA (V_{cc}) and PA's digital control (V_{ctrl}) voltages are used as tuning knobs. The output response of the transmitter is captured by deploying a board level design of an envelope detector. The output of the envelope detector is sampled by an Alazar ATS460 digitizer. The power supplies used in this work are Keithley 2400s that are capable of remote control by a PC via a NI 488.2 GPIB controller. A total of 8 instances are considered for the tuning purposes. The nominal gain of the transmitter is 9 dB with a bound of 1 dB on both sides and the nominal IIP3 is 1 dBm. The constrained optimization is performed on the gain and IIP3 surfaces of these instances using the MATLAB based minimization tool. Tuning results are given in Table 5 which shows that all of the 8 instances are tuned efficiently within the bounds.

Table 5. Results of hardware experiment (alternative tuning approach)

Instance	Gain before tuning (dB)	IIP3 before tuning (dBm)	Gain after tuning (dB)	IIP3 after tuning (dBm)
1	7.86	-0.02	8.10	1.84
2	6.99	-0.74	8.02	1.05
3	7.85	-0.40	8.16	1.04
4	10.79	5.98	9.55	6.20
5	11.43	6.32	9.51	2.28
6	8.99	0.71	8.07	1.69
7	10.18	5.08	8.11	1.81
8	10.45	-0.75	9.17	2.12

CHAPTER 4

ADAPTIVE ANALOG CIRCUITS BASED ON NANODEVICES

In this chapter a direct tuning approach is proposed which predicts power optimal tuning solution from the test response of the circuit. This tuning technique is applied to a carbon nanotube based operational amplifier as described in this chapter.

4.1. Introduction

Until recently, performance enhancement by scaling of CMOS technology has followed trends predicted by Moore's law. However, as manufacturing technology approaches atomic dimensions, quantum effects start dominating transistor behavior. Also increased leakage and process variability make it extremely challenging to keep pace with aggressive performance requirements. In this context, non-CMOS nanodevices such as Graphene Nanoribbon (GNR), Carbon Nanotube (CNT) and spin based devices have shown a lot of promise. The primary advantage of such emerging nanodevices (GNRs, CNTs) is due to ballistic transport of electrons offering a longer mean free path for elastic scattering. These devices are also compatible with high-k materials enabling fabrication of devices with high gate oxide thickness without losing control over device ON current. For digital applications to fully utilize the advantages of such nanodevices, the band gap of such devices has to be significantly high to keep the ON to OFF current ratio small. This band gap requirement forces the construction of nanodevices with very small dimensions where it is difficult to ensure reliable manufacturability. However, since the ON to OFF current ratio is not a serious issue in analog and RF domain, there is considerable promise for the future use of such nanodevices.

In this research, variability issues in analog circuits manufactured with CNT nanodevices are addressed through use of a post-manufacture tuning methodology.

Considerable work has been done in the past on characterization and modeling of CNFETs [70]-[71]. Applicability of CNFETs to digital as well as analog circuits has been explored in [72]-[73]. However, practical implementation challenges of CNFET technology need to be considered while proposing novel design ideas, since imperfections and variations in the device manufacturing process pose a daunting challenge for this emerging technology. In [74]-[75], the authors addressed the variability problem but the applications are limited in digital domain only.

A key problem with Carbon Nanotube (CNT) devices is that controlled growth of such devices during fabrication is difficult to achieve. This means that while fabricating CNTs of a particular type (semiconductor) and a particular chirality, the result is a mixture of different types of CNTs (metallic and semiconductor) with varying chirality. This effect is compounded by variations in the diameter and pitch of the CNTs. The combined variation effects can lead to consequences ranging from reduced yield to functional failure. In this work, the imperfections due to variations in diameter, chiral angle and number of semiconducting nanotubes after removal of metallic CNTs are considered.

After the circuit is manufactured, the specifications of the same are determined using intelligent alternative testing methods. Using intelligent test generation algorithm the statistical correlation between the output response and the specifications are maximized and then by analyzing the response, specifications are computed with the help of nonlinear regression models [29]. The devices that fail to satisfy the specification requirements due to process shifts, undergo post-manufacture tuning to compensate for process-induced performance variations. Tuning is performed by modulating specially designed circuit-level “tuning-knobs” so that the specifications of the same can be controlled to lie within acceptable limits, perhaps at the cost of additional power consumption. To perform tuning, the alternative tests are administered to the CNT-based device under test (DUT). Algorithms running on DSP determine how to modulate the

circuit level tuning knobs to compensate for process induced performance loss. Tuning algorithms have been reported in the past for CMOS based analog and RF circuits [59], [78]. In contrast, a power aware tuning algorithm for yield improvement of CNT based analog circuits is proposed in this work. The handling of testing and tuning challenges posed by the use of CNT based nanodevice in the analog circuits is a key contribution of this work. The tuning method involves selection of appropriate tuning parameters, formulation of an objective function, optimization of the input test stimulus and building regression model between output response and tuning knob setting. The concept of power optimal tuning is introduced by selecting the solution corresponding to minimum power consumption during regression model building.

4.2. Power Aware Post-Manufacture Tuning Methodology

Due to process variations during fabrication, the performance of the manufactured circuit may not be able to satisfy all the targeted specifications. Such process variation effects are severe in scaled CMOS and emerging nanodevices such as carbon nanotube and graphene based transistors. To offset the effects of such manufacturing process variations, a set of external parameters are considered. The external parameters are called "tuning knobs" which are introduced into the circuit during the design phase. Let '*S*' denote the specifications of the circuit, '*P*' the set of process parameters and '*T*' the set of tuning knobs designed into the circuit. Then for all *i*,

$$S_i = f_i(P_1, P_2, ..., P_n, T_1, T_2, ..., T_m) \tag{40}$$

Equation (40) signifies that each of the specifications of the circuit is a function of *n* process parameters and *m* tuning knobs. The nominal set of process parameter values combined with the nominal set of tuning knob values result in the CNT based analog circuits having nominal specification values. The process parameters (*P*) are affected by manufacturing variations and cause the specifications (*S*) to deviate from their nominal values. To restore the nominal operation of the circuit, the set of tuning knob values (*T*)

are changed in such a way that even in the presence of "shifted" process parameter values, the CNT based analog circuit has specification values that are within acceptable limits. The changed tuning knob values can be determined using a search algorithm that minimizes the difference between the nominal specifications of the analog circuit and the specifications of the circuit in the presence of manufacturing process variations. In general, multiple tuning solutions exist that result in the same improvement in the specification values of the "untuned" circuit. It is desirable to pick the solution out of this set of solutions that results in the least amount of power consumption in the "tuned" circuit while ensuring that all specification values are within acceptable limits. Finding such a solution can be formulated as a constrained optimization problem in which the constraints are given by the acceptable limits of the different specifications of the DUT and cost is a function of the power consumption of the DUT. The constraints are to be satisfied for successful tuning and at the same time the power consumption of the circuit is minimized as much as possible.

In the proposed tuning approach, a regression model is developed using supervised learning method that maps the output response of the (untuned) DUT to the optimal tuning knob settings that force all the DUT specifications to lie within acceptable limits while consuming the least amount of power. A key objective during test generation is to maximize the correlation between the DUT response and the optimal tuning knob settings corresponding to "acceptable specification values" and the least power consumption for the DUT. Once the regression model is developed using "training" devices, the optimal tuning knob settings for arbitrary DUTs can be found by capturing the response of the DUT to the optimized test stimulus and mapping the DUT response to the best tuning knob values using the regression model above.

The steps of the power conscious post-manufacture tuning method developed in this work are explained below:

4.2.1. Test generation

In analog testing and tuning problem test generation plays a critical role. The response of the circuit to a particular test signal is analyzed to find out health of the circuit and optimal setting of the tuning knobs. By generating an optimized test stimulus it is ensured that the effects of process shift are reflected to the output waveform of the circuit enabling accurate diagnosis and tuning. In this work genetic algorithm based test stimulus optimization is performed in such a way that the prediction error in the estimation of tuning knob setting by regression model is minimized.

4.2.2. Regression based tuning

In [14] the authors showed that by building a regression mapping between output response and optimal tuning knob setting of a CMOS low-noise-amplifier (LNA) it can be tuned accurately. In this work the concept of power minimization is added by choosing the solution corresponding to lowest power. Different combination of tuning knob settings can tune the circuit back within its performance bounds. But different solutions of tuning knob settings will result in different amount of power consumption though all of the solutions may have same effect on specifications of the circuit. Among these several solutions only one solution is chosen for which the power consumption of the circuit is minimum. Now a regression model is built between the measurement space and tuning knob setting space using multivariate adaptive regression splines (MARS) [30]. In "alternate test" method [29], a regression model is built between measurement space and specification space and then by capturing the output response of the DUT to the optimized test stimulus and using the regression model, the specifications of the DUT are computed. In this work, during the training phase of the regression model building, optimal values of tuning knob settings corresponding to minimum power consumption are found and response of the circuit before tuning is captured. Then MARS models are built between response of the circuit and tuning knob setting for several training

instances. During the evaluation phase, response of the DUT and the MARS models are used to predict the optimal tuning knob setting which gives minimum power consumption and satisfy all performance requirements.

4.3. Design and Tuning of a Carbon Nanotube Based Operational Amplifier

To demonstrate the concept of post manufacture tuning on analog circuits based on emerging nanodevices, a Carbon Nanotube based operational amplifier is designed using Stanford University's CNFET HSPICE model [69]-[71]. To show the effects of variability on the op-amp performance, metallic CNT growth, variation in CNT diameter and chirality variation are considered. As a case study, these effects are included in the HSPICE simulation, resulting degradation in op-amp specifications are observed and tuning algorithm is applied to show improvement in performance.

4.3.1. Design of the operational amplifier

The schematic of the CNFET based Miller compensated two stage operational amplifier with zero nulling resistor (N8) is shown in Figure 42. In the opamp topology N5 is the tail transistor of the differential pair and N7 is used for biasing the second stage. C1 is the miller compensation capacitor used for pole splitting and N8 is used as a resistor to nullify the zero on the right half plane.

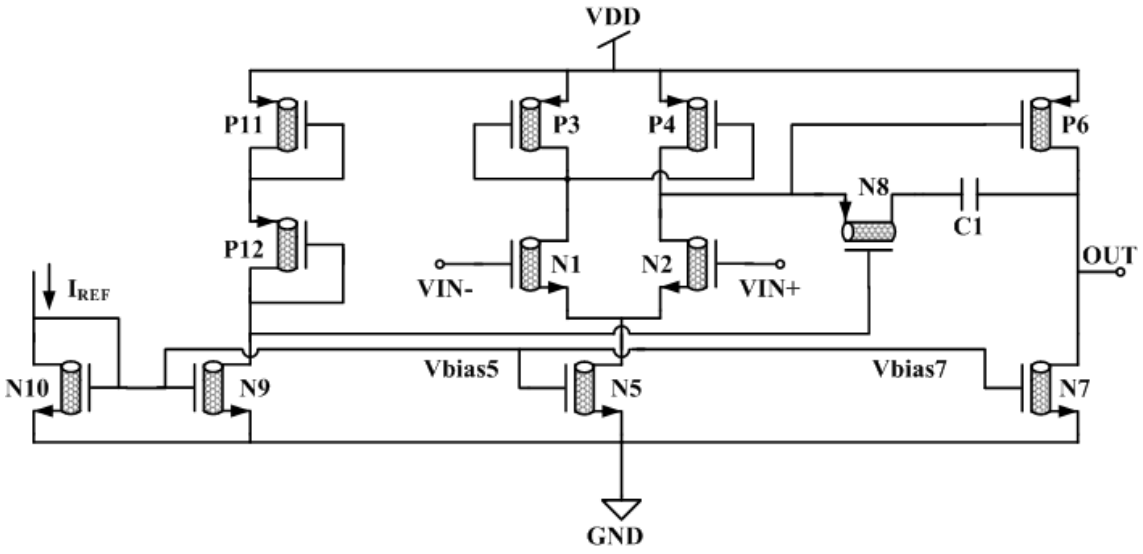
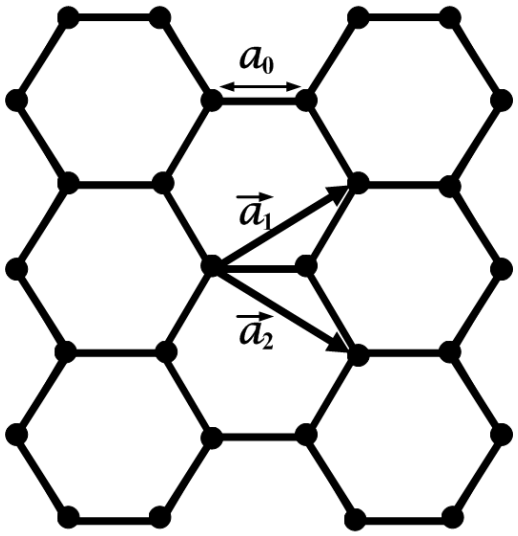


Figure 42. Schematic of the CNFET based Opamp

4.3.2. Variability effects

Three types of variability in CNFETs are considered in the simulation framework which are described below.

(1) Diameter of CNT: The hexagonal honeycomb lattice structure of graphene is shown in Figure 43. A carbon nanotube is basically a rolled sheet of graphene. $\vec{a_1}$ and $\vec{a_2}$ are basis vectors of graphene lattice and $\vec{c}$ is the circumference vector of rolled graphene sheet that determines the properties of carbon nanotube. The pair of integers (*m*,*n*) is called the chiral vector that defines how the graphene sheet is wrapped up [76]. The diameter (*d*) of the nanotube depends on the values of *m* and *n* and the expression of *d* is shown in Figure 43. Controlling the diameter of CNT during manufacturing is a serious issue and the diameter variation [75] causes the properties of the nanotube to change.



$$\vec{c} = m.\vec{a_1} + n.\vec{a_2}$$

$$d = \frac{\sqrt{3}a_0}{\pi}\sqrt{m^2 + n^2 + mn}$$

$$\theta = \tan^{-1}\left(\frac{\sqrt{3}.n}{2m+n}\right)$$

Figure 43. Hexagonal lattice structure

(2) Chiral Angle: The chiral angle (θ) of CNT is defined as the angle between the chiral vector and the zigzag direction. The expression of the chiral angle is shown in Figure 43. Change in chiral angle from its nominal value during manufacturing process is considered in this work.

(3) Metallic Nanotube: Due to random shift in chirality 1/3 of the CNTs become metallic [76] which behave as short circuit. For proper operation of the circuit the metallic nanotubes are removed by electrical burning [77]. To include the effects of metallic CNTs, the opamp is over-designed and each FET in the opamp is designed with 1.5 times more number of CNTs so that after removal of 1/3 metallic CNTs we are left with required number of nanotubes for nominal operation. But this statistical process does not ensure exactly 1/3 and 2/3 distribution of metallic and semiconducting CNTs respectively for all FETs. It signifies that after over-design and removal of metallic CNTs, the number of remaining semiconducting nanotubes may slightly vary from their desired numbers. The exact number of semiconducting CNTs in the transistors determines the specifications of the circuit.

4.3.3. Selection of tuning knobs

The parameters selected as tuning knobs are discussed below:

(1) Bias voltages: The gate bias voltage of the tail transistor (Vbias5) and the gate bias of N7 (Vbias7) are used as tuning knobs in this work. The selection of tuning knobs depends on the specifications that are to be tuned. In this work gain and phase margin of the op-amp are considered as specifications that have to be tuned. Gain of the op-amp depends on the bias current flowing through the branches of first and second stage of the op-amp. Bias currents in these two branches are controlled by gate voltages applied to N5 and N7 respectively. Hence gain of the op-amp can be changed by changing Vbias5 and Vbias7. If amount of current flowing though the branches are increased, gain of the op-amp decreases but bandwidth increases. The programmable bias circuit can be designed by combining parallel current mirrors using digital switches.

(2) Nulling Resistor: The nulling resistor, which is implemented by transistor N8 operating in triode region, is used as the third tuning knob. By proper selection of the nulling resistor value, phase margin and stability of the op-amp can be improved. Purpose of the nulling resistor is to cancel the right-half plane zero in the frequency response of the op-amp in order to improve stability. Selection of the nulling resistor is governed by the following equation:

$$R_z = 1/g_{m6} \tag{41}$$

where g_{m6} is the transconductance of the transistor P6. Due to process variation, transconductance of P6 will change from its nominal value and to obtain proper phase margin the nulling resistor has to be varied too.

Due to variation in diameter, chirality and number of CNTs in a transistor as discussed in Section 4.3.2, the matching between N1-N2 and P3-P4 is violated which results in performance degradation. Random device mismatches can be reduced by adaptively selecting appropriate fingers of transistors [78]. To maintain the matching

requirement between critical transistors, N1, N2, P3 and P4 can be divided in several fingers where each finger consists of nanotubes which are susceptible to process shift. If *K* number of fingers are needed for optimum performance of the transistor, *L* number of extra fingers are added during design where $L < K$. The algorithm that selects the optimum setting of tuning knobs, chooses *K* fingers from *(L+K)* fingers by applying proper digital logic to the controlling switches connected to the fingers in such a way that the matching is improved. For intuitive understanding, let us consider variation in only number of CNTs in a transistor. The variation can be both positive and negative from the nominal value. If the fingers are selected in proper way then positive error in a finger will be canceled by the negative error in another finger and the number of CNTs in all of the selected fingers will add up to the nominal value. In the simulation framework of this work, initially CNT fingers are properly selected to reduce mismatches in number of CNTs. Then the tuning algorithm is applied to find out the values of the primary tuning knobs (bias voltages and nulling resistor).

4.3.4. Formulation of the cost function

The tuning procedure is formulated as a constrained optimization problem where two specifications (gain and phase margin) and power consumption are considered. Following equations describe the constrained optimization:

$$Gain_{nom} - Tol_{gain} < Gain < Gain_{nom} + Tol_{gain} \tag{42}$$

$$PM_{nom} - Tol_{pm} < PM < PM_{nom} + Tol_{pm} \tag{43}$$

$$Minimize(P_{tot}) \tag{44}$$

Equations (42)-(43) represent the constraints while Equation (44) is the optimization objective function. Tol_i represents the tolerance limit on specification *i* from its nominal value and $Spec_{nom}$ represents the nominal specification of the opamp while P_{tot} is the total power consumption. For gain and phase margin (PM), bounds are

specified on both sides. If the gain becomes too high, the bandwidth of the circuit is reduced as the gain bandwidth product remains constant. Also very high gain will saturate the stage next to the opamp in actual system. A small phase margin causes the output to ring and the settling time becomes slow. On the other hand, for a very high value of phase margin the output takes a long time to reach the final value. Hence, both gain and phase margin should be limited within a certain range on both sides of their nominal values.

4.4. Simulation Results

Simulation results are shown in this section.

4.4.1. Opamp design

The op-amp shown in Figure 42 is designed using the Stanford CNFET model [69]-[71] in HSPICE with a channel length of 32 nm and supply voltage of 0.9 volt and a phase margin of 81.8° is achieved. The ac gain and phase plots for the nominal design are shown in Figure 44. The nominal setting of Vbias5 and Vbias7 are both 0.4 volts. Value of the nulling resistor in compensation circuit is 3k. The specifications of the designed operational amplifier are shown in Table 6.

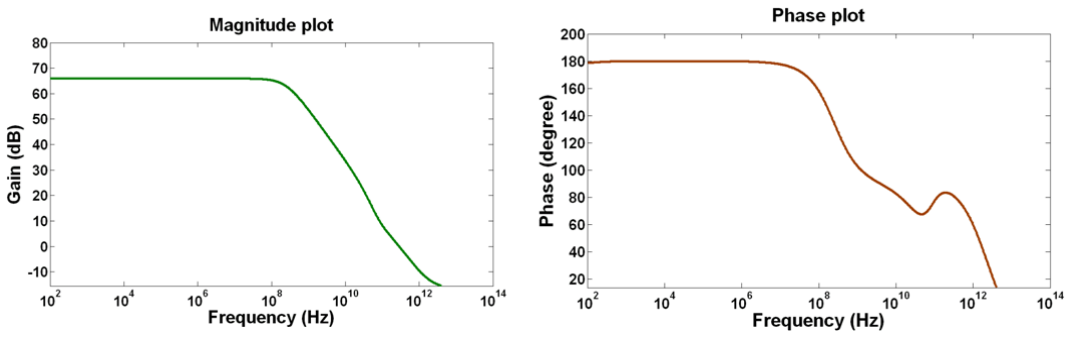


Figure 44. Gain and phase plot of the opamp

Table 6. Specifications of the designed op-amp

Gain	Bandwidth	Phase Margin	Unity Gain Frequency	Power
66 dB	249 MHz	81.8°	287.5 GHz	0.76 mW

4.4.2. Test generation

Time domain test stimulus optimization is performed using elitism based genetic algorithm. Performance of the genetic optimizer is shown in Figure 45. The cost function is defined as the squared prediction error in computation of optimal tuning knob setting using regression model. From Figure 45 it can be observed that GA converged after 50 generations and the resulting optimized test signal has a normalized fitness value of 0.0276.

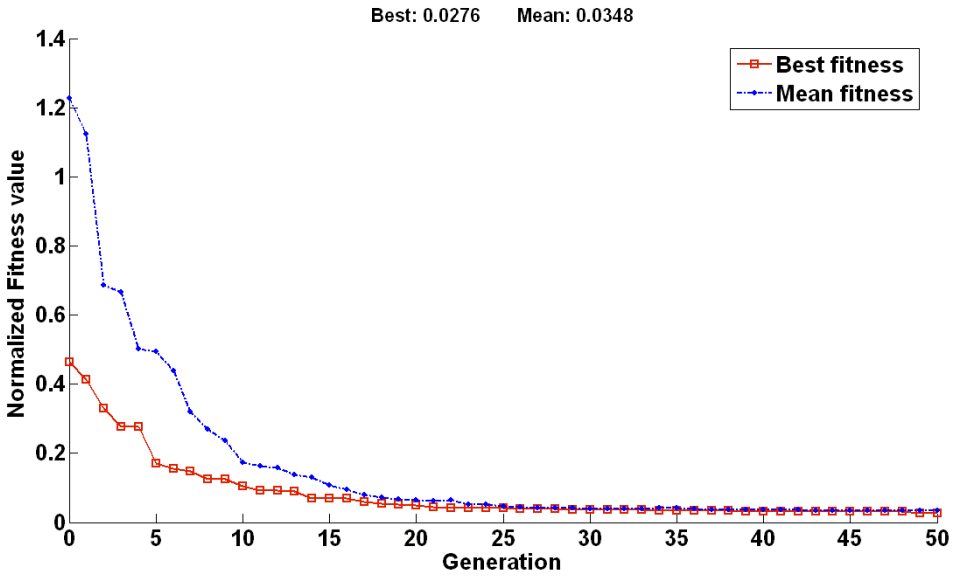


Figure 45. Performance of genetic algorithm for test generation of CNFET based opamp

4.4.3. Tuning

The effects of variability are introduced in the HSPICE simulation in terms of diameter, chiral angle and CNT numbers. Each of N1, N2, P3 and P4 is subdivided into fingers and proper finger selection is performed to improve matching. Then a MATLAB based searching tool [47] is used to find out the optimal setting of Vbias5, Vbias7 and nulling resistor R_z. Variation of gain with Vbias5 and Vbias7 is shown in Figure 46 for a particular instance. Regression models are built using training instances and during the evaluation phase optimal values of the bias voltages and nulling resistor are found from the output response of the instances to the optimized test signal. Nulling resistor value as found by the regression models are shown in Figure 47. As case study, two instances with process variation are considered and optimal settings of tuning knobs are found for which the specifications are restored within the bounds with minimum power consumption. Gain, Phase Margin (PM) and power consumption for these instances before and after tuning are presented in Table 7 which shows that the instances can be tuned efficiently using this algorithm.

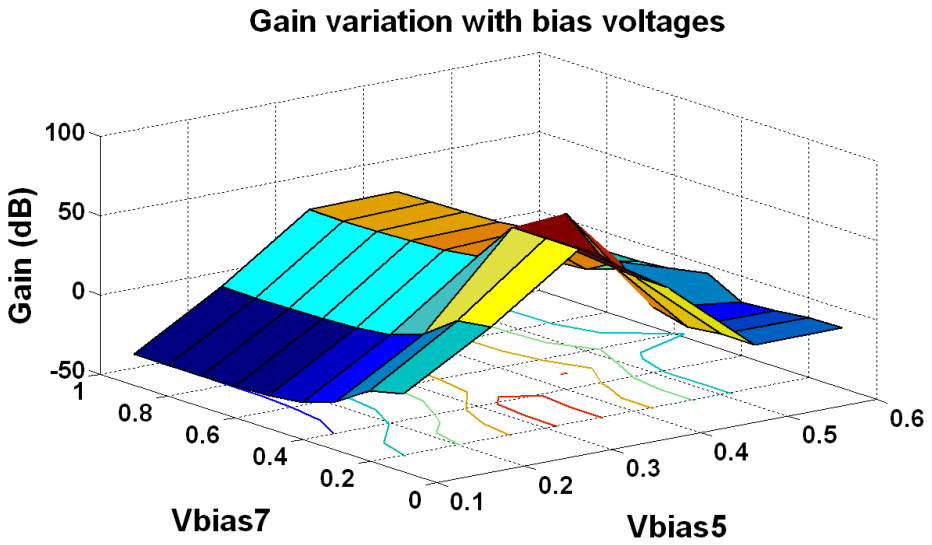


Figure 46. Variation in gain with two tuning knobs

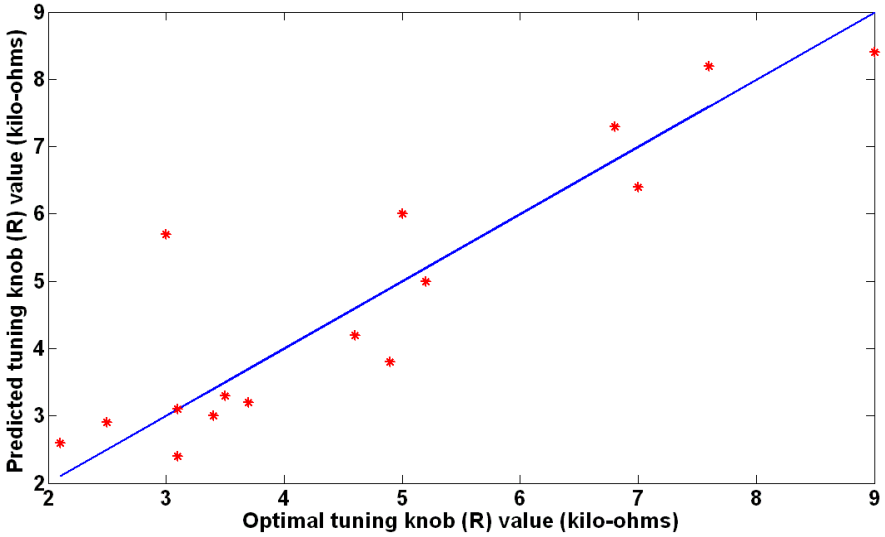


Figure 47. Prediction of nulling resistor value from regression models

Table 7. Specifications of two process varied opamp instances

Specs		Gain (dB)	PM	Power (mW)
Instance 1	Process shifted	55.4	104.3°	0.67
	Tuned	64.2	80.8°	0.64
Instance 2	Process shifted	75.7	84.2°	0.57
	Tuned	64.3	80.6°	0.86

4.4.4. Yield improvement

The specifications of the circuit before and after tuning are shown in Figure 48. Bounds are specified on gain and phase margin as illustrated in Figure 48. The shift in specifications from their nominal values depends on the amount of process variation introduced. The distribution of specification shown in Figure 48 reflects the process variation considered in the simulation. For this simulation, yield is observed to be 41.54%

before tuning. After tuning is done, yield becomes 66.92% which results in an overall yield improvement of 25.38%.

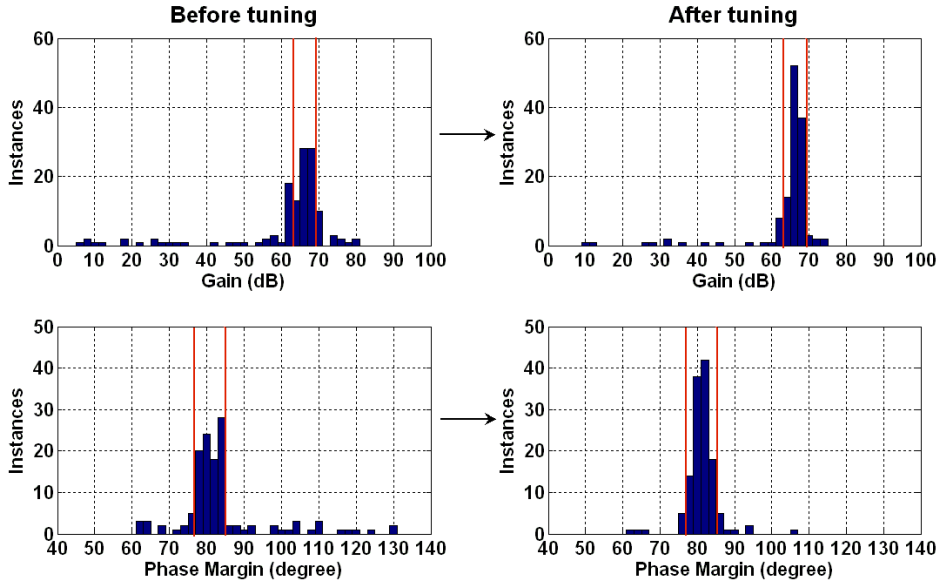


Figure 48. Yield plots (left: before tuning and right: after tuning)

CHAPTER 5

DESIGN OF ADAPTIVE POWER AMPLIFIER

In this chapter design of an adaptive class-E RF power amplifier is discussed which can be used in the proposed adaptation framework for RF transmitters. Proposed adaptive power amplifier has higher efficiency with power back-off, better reliability and can mitigate process variation effects.

5.1. Introduction

Modern wireless communication systems require high data rates and efficient spectrum utilization which result in non-constant envelope modulation schemes and signals having high peak-to-average power ratios (PAPR). This causes the power amplifier (PA) in the transmitter to operate at large power back-off where traditional PAs show poor efficiency. Efficiency of the power amplifier is critical in portable wireless devices as a higher efficiency of the PA leads to longer battery lifetime. In base station applications, high efficiency PAs are necessary for reducing power consumption and heat sinking costs.

With more and more integration of RF power amplifiers in deeply scaled CMOS technologies, it is becoming increasingly difficult to exert sufficient control on process variations to ensure proper functionality and performance of the PA. Another challenge is posed by the reliability issues such as oxide break down and hot carrier stress which are critical in power amplifiers due to large signal excursions [79].

The challenges of dealing with efficiency reduction with power back-off, performance degradation due to process variation and reliability issues are addressed in the past by modifying traditional power amplifier circuits. Efficiency improvement techniques include Doherty architecture, envelope tracking (ET) and envelope

elimination and restoration (EER) techniques, Outphasing or linear amplification using nonlinear components (LINC) and pulse-width modulation [80]. An emerging trend is to design adaptive power amplifiers and tune it properly with the help of on-chip digital logic or digital signal processor to ensure high efficiency at all output power levels. In [81] and [82], adaptive class-E power amplifier designs are presented where the matching networks are tuned dynamically to ensure high efficiency with power back-off. Similarly, digitally assisted adaptation techniques are used to nullify process variation and stress effects. A self-healing power amplifier is presented in [3] that uses integrated sensors, actuators and digital ASIC, which runs the healing algorithm and mitigates the effects of process variation, modeling inaccuracies, load mismatch and aging.

In this work, design of an adaptive class-E power amplifier is proposed that uses an LC tuning network with a variable capacitor and addresses all three challenges - (i) improvement of efficiency with power back-off, (ii) improving reliability and (iii) compensation of process variation effects. The proposed tuning network is much simpler than those proposed in [81] and [82] and uses only one tunable capacitor with a certain tuning range. The capacitor is tuned dynamically at the rate of the envelope signal only.

5.2. Proposed Adaptive Power Amplifier

The proposed adaptive class-E power amplifier is shown in Figure 49. Traditional class-E power amplifiers [83] consist of one NMOS switch ($\boldsymbol{M}$), a parallel capacitor ($\boldsymbol{C_P}$) which can be the parasitic output capacitance of the NMOS transistor and / or a separate capacitor, a choke inductor ($\boldsymbol{L_C}$) connecting the drain of the NMOS switch to the power supply and a series LC network ($\boldsymbol{C_A}$ and $\boldsymbol{L_A}$) connected to the load resistance ($\boldsymbol{R}$). In the proposed circuit, another series LC network ($\boldsymbol{L_B}$ and $\boldsymbol{C_B}$) is connected to the drain of the NMOS where the capacitor $\boldsymbol{C_B}$ has a variable capacitance as shown in Figure 49. The power amplifier is driven by pulse-width or duty cycle modulated signal [81]. In pulse-

width modulation technique, amplitude modulation of the RF signal is created by changing the duration for which the switching transistor is turned on.

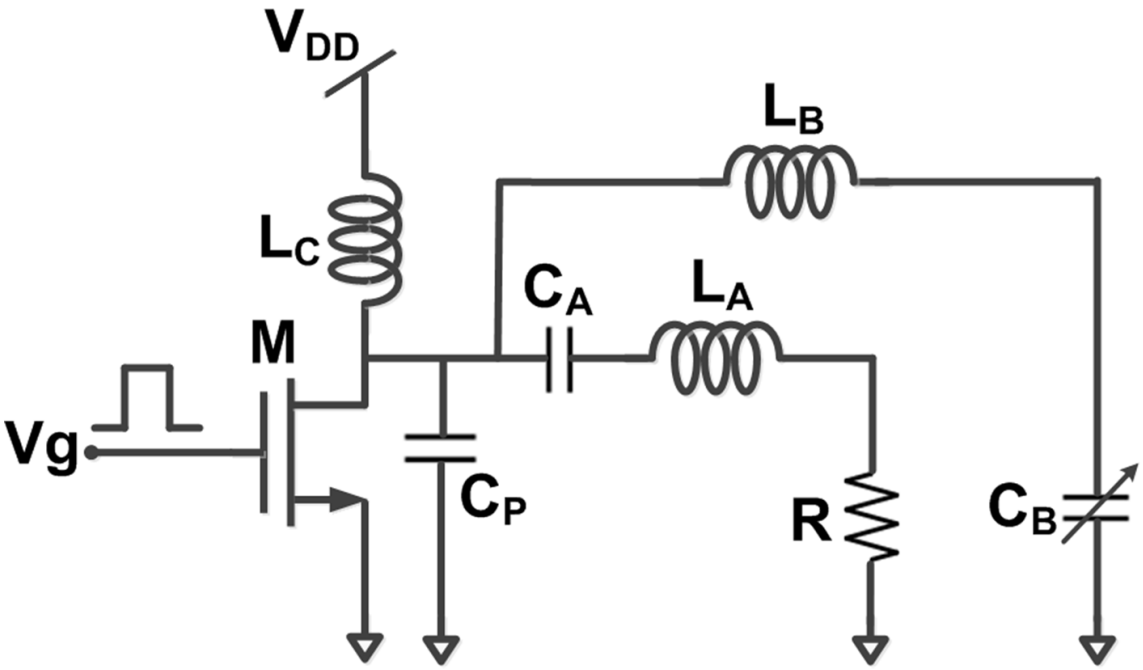


Figure 49. Schematic of the proposed adaptive power amplifier

5.2.1. Tuning for efficiency, reliability and self-healing

The capacitance of the capacitor C_B is tuned dynamically using the digital resources available on chip to satisfy three requirements: (1) improvement of reliability, (2) increasing efficiency with power back-off and (3) process variation tolerance or self-healing as discussed below:

5.2.1.A. Improvement of reliability:

The output power achievable in a class-E power amplifier is limited by the constraints on the maximum drain voltage swing of the NMOS switch as high peak drain voltage can cause break-down. For peak output power (50% duty cycle) and power levels close to the peak power, capacitance of $\boldsymbol{C_B}$ is set in such a way that $\boldsymbol{C_B}$ and $\boldsymbol{L_B}$ form a series resonance network tuned to the 3rd harmonic of the carrier frequency and it introduces a 3rd harmonic current in the circuit that charges the parallel capacitor $\boldsymbol{C_P}$ when the gate voltage is low and the NMOS switch is turned off. This 3rd harmonic contribution shapes the drain voltage waveform in such a way that the peak value of the drain voltage is reduced and hence it improves reliability of the power amplifier. In this case, the power amplifier actually operates in class-E/F_3 mode as explained in [84]. Analysis of the effect of this tuning network on the drain voltage of the NMOS switch is presented in Section 5.2.2.

5.2.1.B. Improvement of efficiency:

High peak-to-average power ratio in a modulated signal forces the power amplifier to operate at large power back-off where PAs perform poorly in terms of efficiency. Class-E power amplifiers show very high efficiency due to ZVS and ZdVS conditions (as explained in Section 5.2.2) which ensure that when the NMOS switch is turned on, voltage across the switch is minimum and power loss due to discharge of the capacitor $\boldsymbol{C_P}$ is minimized. In a static design of class-E power amplifier, ZVS and ZdVS conditions can be satisfied at a fixed duty cycle of the driving waveform and for other duty cycles discharge of the capacitor $\boldsymbol{C_P}$ reduces efficiency. The proposed adaptive power amplifier is designed to satisfy zero voltage switching condition at 50% duty cycle. For other duty cycles, capacitor $\boldsymbol{C_B}$ is tuned properly so that the current introduced by the $\boldsymbol{C_B}$-$\boldsymbol{L_B}$ branch shapes the drain voltage in such a way that it minimizes the voltage across the switch when it is turned on. This leads to improvement of efficiency with

power back-off as shown in Section 5.3. While determining the values of C_B for different duty cycles, it is also ensured that introduction of the additional current does not create a high peak voltage at the drain of the NMOS and thus maintains reliability of the device at all duty cycles. It should be noted that for improving efficiency with power back-off, dynamic adaptation of the capacitor C_B has to be done at the envelope frequency only.

5.2.1.C. Process variation tolerance (self-healing):

With scaling of CMOS transistors, RF circuits are becoming more and more susceptible to process variation and maintaining the required performance of the circuit in presence of such manufacturing defects is a big challenge. Self-healing techniques [3] ensure that by making RF circuits tunable and using available on-chip digital logic to control the values of the tuning knobs, effects of process variation can be mitigated. In the proposed power amplifier, process variation affects the active and passive components and results in degradation of performance. It is shown that in the presence of process variation, optimal settings of the tunable capacitor C_B with duty cycle variation will be different from the nominal case. Using built-in-self-test (BIST) techniques, effects of process variation can be detected and settings of C_B can be determined accordingly to obtain best possible performance from that particular process shifted instance.

5.2.2. Analysis of the tuning circuit

The tuning circuit (L_B-C_B) contributes a current that charges the parallel capacitor C_P and modifies the drain waveform of the transistor switch. For peak output power (50% duty cycle), L_B-C_B creates a series resonant network for 3rd harmonic of the carrier frequency such that $3f_0 = 1/\left(2\pi\sqrt{L_B C_B}\right)$ where f_0 is the carrier frequency. It reduces peak drain voltage and the PA actually operates in class-E/F_3 mode [84] in this case. The following analysis shows how the tuning circuit affects the drain swing of the NMOS transistor for 50% duty cycle.

Class-E power amplifiers operate based on the principle of zero voltage switching (ZVS) and zero voltage slope switching (ZdVS). The NMOS transistor, which behaves as a switch, is turned on when the voltage across the transistor and its slope are both zero which, in the ideal case, ensures that no power is lost due to the discharge of the parallel capacitor and high efficiency is achieved. The ZVS and ZdVS conditions can be written as [85]:

$$V_D\left(2\pi/\omega\right)=0 \tag{45}$$

$$\left.\frac{dV_D\left(t\right)}{dt}\right|_{t=2\pi/\omega}=0 \tag{46}$$

where $V_D\left(t\right)$ is the drain voltage of the switching transistor, the switch is closed during the time interval $0\le t<d\pi/\omega$ and open during $d\pi/\omega\le t<2\pi/\omega$ and ω and d denote the angular switching frequency and duty cycle, respectively. When the switch is open, the current flowing in the circuit charges the parallel capacitor ($\boldsymbol{C_P}$ in Figure 49) and current through the capacitor $\boldsymbol{C_P}$ in the presence of the proposed tuning circuit can be written as:

$$I_C\left(t\right)=\frac{1}{L_C}\int_{d\pi/\omega}^{t}\left(V_{DD}-V_D\left(t\right)\right)dt+I_L\left(d\pi/\omega\right)+I_A\left(t\right)+I_B\left(t\right) \tag{47}$$

where $\boldsymbol{L_C}$ is the inductor connecting the drain to the supply ($\boldsymbol{V_{DD}}$) and $I_L\left(t\right)$, $I_A\left(t\right)=I_f\sin\left(\omega t+\phi_1\right)$ and $I_B\left(t\right)=I_{3f}\sin\left(3\omega t+\phi_3\right)$ are the currents flowing through the inductor $\boldsymbol{L_C}$, the load resistance $\boldsymbol{R}$ and the tuning circuit ($\boldsymbol{L_B}$-$\boldsymbol{C_B}$), respectively. Equation (47) can be written in the form of differential equation:

$$L_CC_P\frac{d^2V_D\left(t\right)}{dt^2}+V_D\left(t\right)-V_{DD}-\omega L_CI_f\cos\left(\omega t+\phi_1\right)-3\omega L_CI_{3f}\cos\left(3\omega t+\phi_3\right)=0 \tag{48}$$

Solving Equation (48), the drain voltage of the NMOS transistor can be found as:

$$V_D(t) = A_1 \cos\left(\frac{t}{\sqrt{L_C C_P}}\right) + A_2 \sin\left(\frac{t}{\sqrt{L_C C_P}}\right) + V_{DD} + \frac{\omega L_C I_f}{1-\omega^2 L_C C_P}\cos(\omega t + \phi_1) + \frac{3\omega L_C I_{3f}}{1-9\omega^2 L_C C_P}\cos(3\omega t + \phi_3) \quad (49)$$

Values of A_1 and A_2 are found from the conditions given in Equation (45) and (46). The last term in Equation (49) is the contribution of the third harmonic current flowing in the tuning circuit and this third harmonic component, added with other terms in Equation (49), shapes the drain waveform in such a way that peak swing is reduced as compared to the case when there is no third harmonic current.

For other duty cycles, capacitance of $\boldsymbol{C_B}$ is changed which results in a different shaping that minimizes the voltage across the transistor at the time when the switch is turned on.

5.3. Simulation Results

The proposed adaptive power amplifier is designed in an advanced 65nm CMOS process for 2.4 GHz frequency. A finite inductor is used in place of the choke inductor $\boldsymbol{L_C}$. Inductors are assumed to be on-chip inductors with a quality factor of 10.

5.3.1. Tuning for reliability

Figure 50 shows gate driving waveform with 50% duty cycle and zero voltage switching waveform at the drain of the NMOS switch with and without the tuning network ($\boldsymbol{L_B}$-$\boldsymbol{C_B}$). In this case when the gate driving waveform has 50% duty cycle, $\boldsymbol{C_B}$ is tuned such that $\boldsymbol{C_B}$ and $\boldsymbol{L_B}$ form a series resonant circuit at 3rd harmonic which is 7.2 GHz. This 3rd harmonic current reduces the peak of the drain voltage swing from 5.1 volts to 3.7 volts as shown in Figure 50 and thus improves the reliability of the power amplifier. 100 mW of peak output power is obtained from the power amplifier at 50% duty cycle with 76% peak efficiency. The efficiency loss is contributed by resistive components of the inductors and finite on-resistance of the NMOS switch.

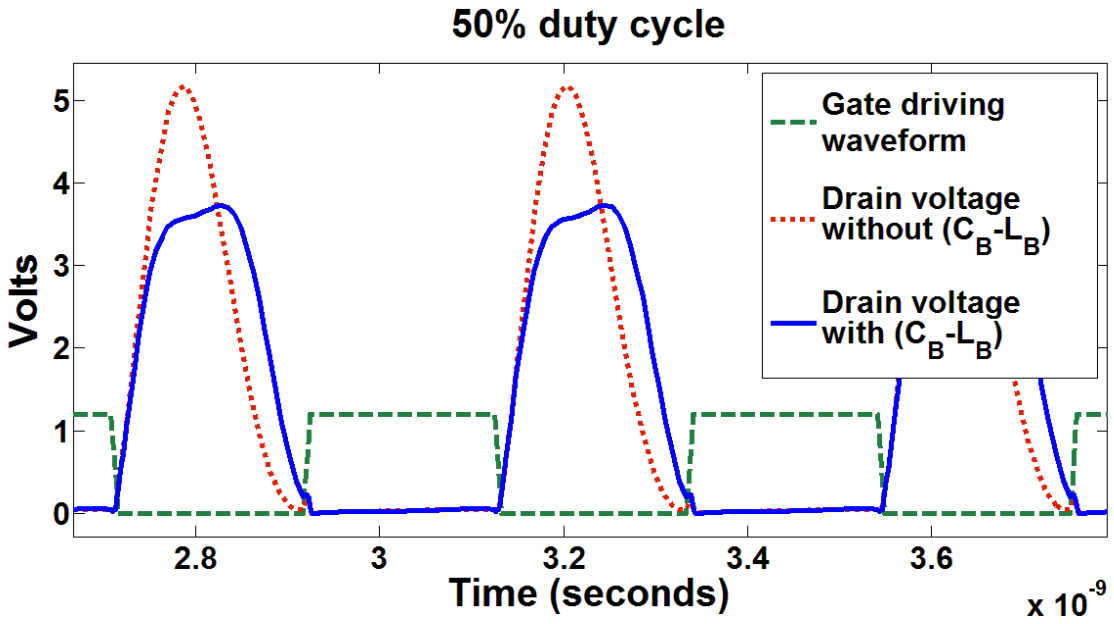


Figure 50. Drain waveform with and without tuning circuit for 50% duty cycle

5.3.2. Tuning for efficiency

Power back-off is created by reducing the duty cycle of the gate driving waveform. At a lower duty cycle, ZVS condition gets violated and the switch is turned on when there is significant voltage across the switch. This results in discharge of the capacitor C_P and loss of efficiency. By tuning C_B properly and controlling the current added by the network C_B-L_B, drain voltage waveform can be modified such that voltage across the switch is reduced at the time of turn on for any duty cycle. This reduces power dissipation due to discharge of capacitor C_P which in turn improves efficiency at lower duty cycles. Figure 51 shows two cases: drain voltage waveforms at 30% duty cycle with C_B kept fixed at its value of 50% duty cycle (C_B-L_B tuned to the 3rd harmonic) and with C_B tuned properly to reduce drain voltage at turn on time for 30% duty cycle. It is evident from Figure 51 that by tuning C_B properly at different duty cycles, power dissipation can be reduced. While tuning C_B to improve efficiency, it is also ensured that peak of drain voltage does not go beyond 3.7 volts which is the reliability limit. Figure 52 shows

efficiency of the power amplifier at different duty cycles with C_B tuned to reduce power dissipation and with C_B kept fixed at its value of 50% duty cycle (class-E/F_3 operation). It is evident from Figure 52 that tuning C_B for different duty cycles can improve efficiency significantly with power back-off. Capacitance values of C_B required at different duty cycles to achieve this efficiency improvement are plotted in Figure 53 which shows that a tuning range of 0.5 pF to 2.1 pF is needed. This tunable capacitor C_B can be implemented as a varactor as shown in [82] or as a set of unit capacitors connected through switches where different amount of capacitance can be obtained by turning on appropriate number of switches as demonstrated in [81].

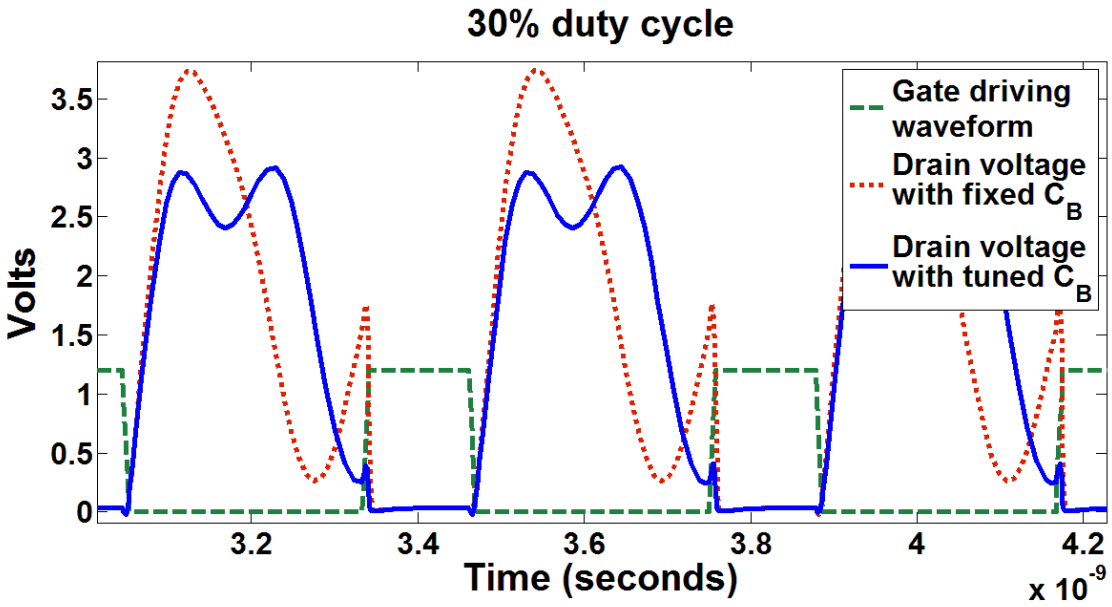


Figure 51. Drain waveform with fixed C_B and C_B tuned for 30% duty cycle

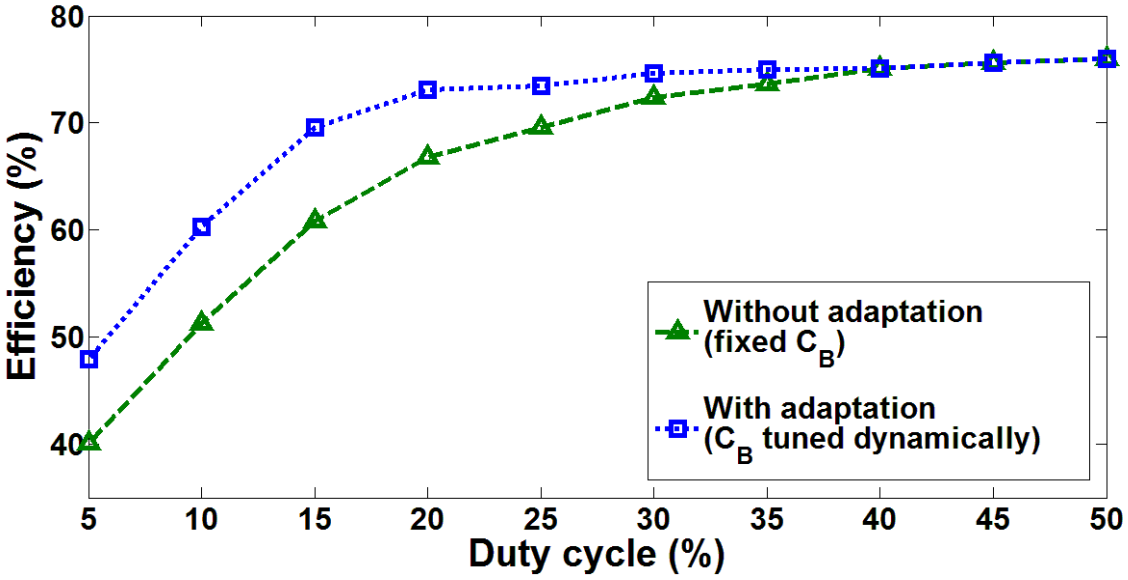


Figure 52. PA efficiency for different duty cycles of the driving waveform

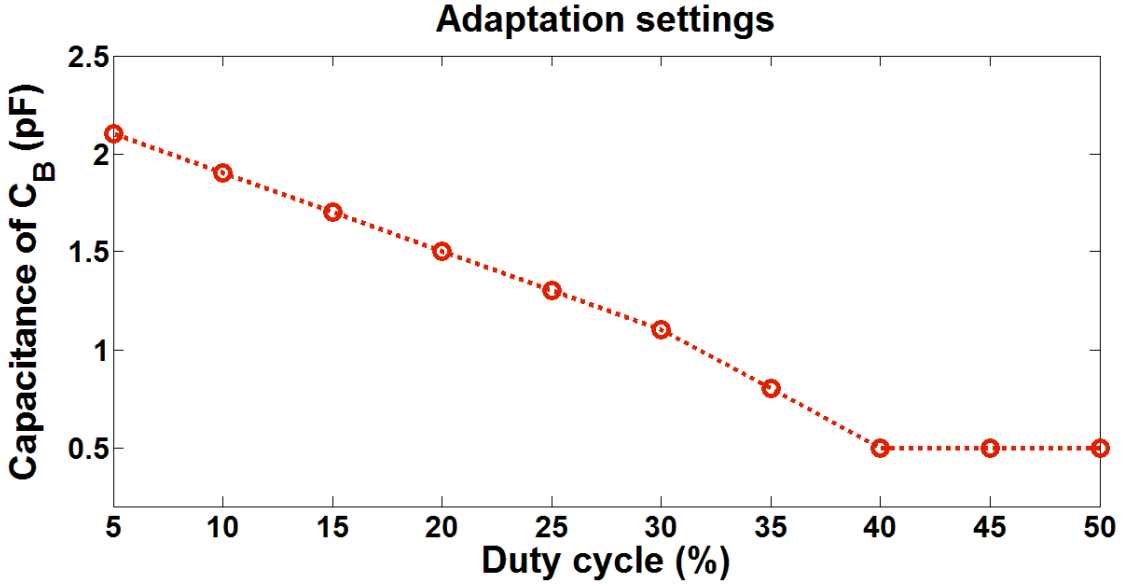


Figure 53. Adaptation settings (capacitance of C_B) for improving efficiency at different duty cycles

5.3.3. Tuning for process variation tolerance

Process variation effects are introduced in the simulation framework and a particular process shifted instance of the PA is considered to validate the proposed process variation tolerant adaptation scheme. This PA instance is simulated with different duty cycles of the driving waveform with $\boldsymbol{C_B}$ tuned dynamically as shown in Figure 53 (nominal adaptation) and efficiency is measured. Now, the adaptation settings computed for the nominal instance may not be optimal for a process shifted instance and performance improvement is possible by finding out best adaptation settings for that particular instance. This can be done by applying built-in-self-test (BIST) techniques and measuring performance of the PA using on-chip sensors and using integrated digital signal processor to determine best tuning knob settings for a process varied instance in a standard self-healing framework [3]. Optimal settings of $\boldsymbol{C_B}$ at different duty cycles are computed for the process shifted PA considered in this simulation so that efficiency is maximized without violating the reliability constraint of peak drain voltage swing. The optimal adaptation settings for this instance are found to be different from that of a nominal instance. Efficiency values of the process shifted instance are shown in Figure 54 with nominal adaptation (broken line) and optimal adaptation for this particular instance (solid line). It is evident from Figure 54 that using this process variation tolerant adaptation scheme, performance degradation (efficiency reduction) due to process shift can be mitigated to certain extent by finding out best adaptation settings for each process varied instance. If due to process variation, capacitance values of $\boldsymbol{C_B}$ change at different settings, that will be taken care of by the proposed process variation tolerant adaptation scheme as it finds out the best setting to maximize efficiency without violating reliability constraints at each duty cycle.

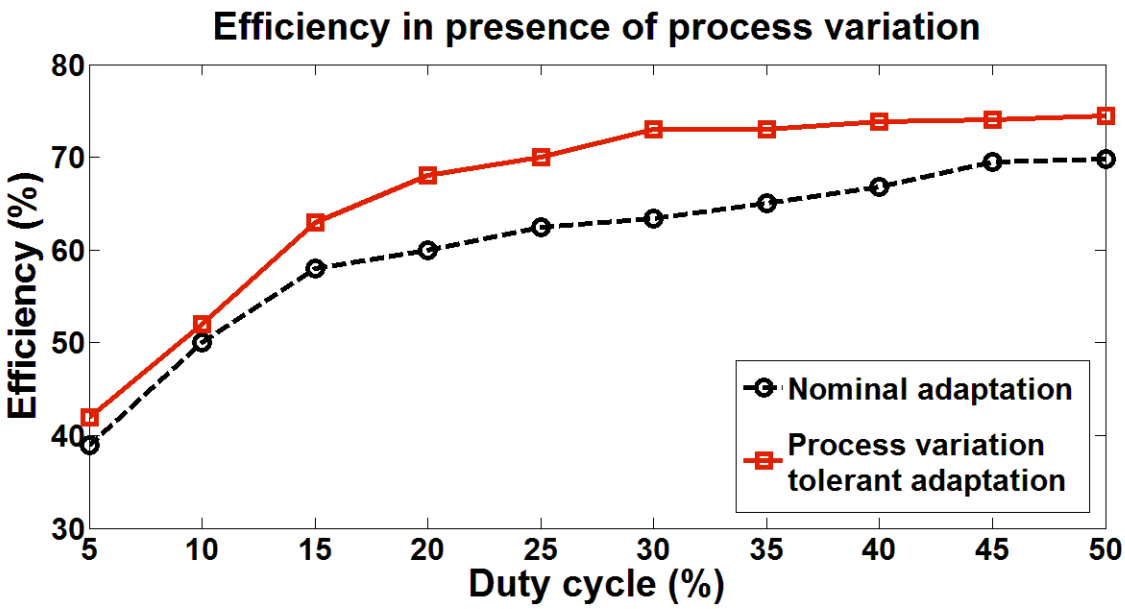


Figure 54. Efficiency at different duty cycles for nominal adaptation and process variation tolerant adaptation

CHAPTER 6

TESTING OF ADAPTIVE SYSTEMS

In this chapter a prediction based testing technique is proposed for adaptive analog / RF systems that does not require the system to be tested at all tuning knob settings and thus saves test time.

6.1. Introduction

With the current progression towards lower technology nodes it is becoming increasingly difficult to exert sufficient control on process variations to ensure that the circuit specifications remain within their nominal bounds. Additional analog and digital correction circuitry is often needed to detect and compensate for the resulting manufacturing imperfections. The effects of excessive process variations can be corrected by incorporating tunable components (such as tunable mixers, LNAs) into the analog/RF circuitry itself. These tunable components are designed to have "tuning knobs" that allow the performance of the relevant devices to be traded off against power consumption. A relevant tuning knob may be the bias current of the LNA, for example. If such knobs are judiciously incorporated, the same can be used to "tune" an RF/mixed-signal system if the specifications of the RF system are not within acceptable bounds post-manufacture [22]-[23]. Additionally, similar tuning knobs may be incorporated into circuitry to allow the system to adapt to changing workloads. When workload demands are high, the individual module performances are increased and vice versa, thereby saving power consumption when workload demands are not high. For RF systems, the workload is represented by channel conditions. When the wireless channel quality is good, the system does less work to achieve a specified bit error rate. When the wireless channel quality is poor, the RF system has to work much harder and thereby consumes more power [20].

Both of these paradigms for process resiliency and low-power workload adaptive operation are extremely critical for the next generation of analog/mixed-signal/RF systems where the goal is to have the highest yields for reducing the cost of individual product units and ultra-low power operation for long battery life of portable devices.

The problem of testing such process and workload-adaptive devices is critical as test cost can add significantly to the final cost of the manufactured product. In this research, the focus is on automated testing of devices that adapt to process and workload conditions and thereby have intrinsic performance monitoring driven feedback control algorithms built into them that use the feedback control to appropriately modulate the device "tuning knob" values described earlier. The problem is made complicated due to the large number of tuning knob combinations that are designed into the system and the test/monitoring effort needed to find the right tuning knob combinations across process/workload effects that allow acceptable system level performance for the least power consumption.

6.2. Prior Work

Previous works in testing of adaptive systems have explored digitally assisted analog circuits. In [86] the difference between uncalibrated and calibrated output codes are used for testing of adaptive ADC. In [87] calibration data is used to predict which devices would fail selected static and dynamic specifications. In [88], this concept is applied to equalizers by looking at the final static states of the adaption engine as well as the dynamic convergence trajectory of these states to predict the presence of faults. Test generation for the same using genetic algorithm is demonstrated in [89]. In [90], design for testability features and test stimuli are explored in addition to adaptation engine state inspection to predict faults. In [91], the digital calibration circuitry in a Weaver image-reject receiver is modified to introduce DFT features to create a go/no-go type of test. In [25], the authors have proposed a mid-point test method where they predict performance

at all knob settings from the measurement at a single setting for a low noise amplifier. While considering different specifications of the RF system, single test method results in larger prediction error which necessitates testing of the system at multiple knob settings as evident from the simulation results in this work.

6.3. Key Contributions

In this work a new open loop test technique is proposed for adaptive RF systems and from the results of the test, closed loop performance is predicted. The test time involved is significantly less than the time needed to actually tune the system for process variations or to test the adaptation across different workloads.

6.4. Overview of the Approach

The general model of a digitally assisted adaptive RF/mixed-signal system consists of the architecture shown in Figure 3. The proposed test procedure consists of the following steps:

1. Apply a set of optimized tests to the DUT with the tuning knobs (determined by the contents of the TC registers as shown in Figure 3) set to predetermined (optimized) values. The optimization procedures are described later and are a key contribution of this research. Note that while these tests are performed, the normal feedback control mechanisms are disabled. Hence these tests are “open loop” tests. The test time involved is significantly smaller than the time taken to tune the system for process variations and even much more smaller than the time that would be needed to test the system’s ability to adapt across a variety of possible workloads.

2. From the results of these tests, the relationship between the tuning knob values and the RF/mixed-signal system level specifications are determined (called “response surfaces”).

3. Once the response surfaces are known, the manner in which the control algorithms that reside in the baseband unit will control the performance specifications of the RF/mixed-signal system for process perturbed devices or workload variations (i.e. the manner in which the system will adapt) can be determined analytically.

4. From the results of this analysis and the open-loop test, it is possible to predict how the adaptation will work in closed loop and whether the adaptation will succeed or not without performing expensive test-time adaptation (for process and workload perturbations).

The focus of this work is to find out the best possible tuning knob settings where the system should be tested so that the performance surface can be predicted most accurately. Results of this performance prediction can be used for process and workload adaptation.

6.5. Proposed Test Technique

While testing a static analog / RF system, a test signal is applied to the system and the corresponding response is captured. From the captured signature, specifications of the system are obtained by computing parameters of the behavioral model or using regression mapping. Testing an adaptive system is much more complicated than that since the adaptive system has different ‘states’ and the specifications at all these states are to be measured. If the system is tested at all possible tuning knob settings and specifications are computed for those settings then it will incur significant test time. In this work a fast testing method for adaptive systems is proposed which consists of test stimulus generation, performance prediction across different knob settings and selection of optimal tuning knob settings which give best prediction. Using the proposed method, the test responses of the system at a few selected tuning knob settings are captured and from these responses, specifications at all knob settings are predicted. The concept of

performance prediction, test generation and tuning knob selection are explained below followed by the description of the whole adaptive system testing approach.

6.5.1. Performance prediction

The key aspect of the proposed technique is testing the system at a few knob settings and from those responses prediction of specifications for all knob settings. This is performed using a regression tool: Multivariate Adaptive Regression Splines (MARS) [30]. Let there are 'n' number of tuning knob settings in total and for each knob setting there are 's' number of specifications and the system is tested at 'm' number of knob settings where $m << n$. From the 'm' number of captured responses, ($n*s$) number of specifications are predicted using MARS. During training phase, instances from different process corners are selected and their responses (m) and specifications ($n*s$) are used to train MARS models and then in the evaluation phase, using the responses of the evaluation instances, their specifications are predicted.

6.5.2. Test generation

In the proposed approach, the system is tested at a few selected tuning knob settings and from those test responses, specifications are predicted for those and all other knob settings. When the system is tested at those selected knob settings, different test stimuli are applied for different settings. A genetic algorithm based test generation algorithm is proposed that finds out the best test signal for a particular knob setting so that the specifications are predicted with highest accuracy from the test response. The test stimulus is a multitone signal and the genetic algorithm optimizes the amplitude and phase angles of the tones. Let us take the case where the system is kept at a knob setting (K_a) while testing and the optimum test stimulus for this setting is to be found out. Genetic algorithm starts with a random population of candidate solutions where each candidate solution represents a combination of amplitudes and phase angles. Next, the

multitone test signals corresponding to those candidate solutions are applied to a set of process varied instances and all of these instances are kept at knob setting K_a. The objective function for each test signal is calculated in the following way: for every test signal, responses of all of the instances are captured at K_a knob setting. Then a regression mapping is built (as explained in previous section) between the output waveforms (at K_a) of these instances and their specifications (gain, IIP3 and power consumption) at all tuning knob settings. Finally the same test signal is applied to another set of process varied instances (evaluation set) and from the response (at K_a), specifications are predicted for all tuning knob settings using previously built regression models. The difference between the actual specifications and predicted specifications is the prediction error and the total normalized prediction error for all specifications at all knob settings of all evaluation instances is defined as the objective function. Depending on the values of the objective functions, genetic algorithm creates new set of chromosomes (candidate solutions) using cross-over and mutation operators [45]. When genetic algorithm converges, the optimum candidate solution (test stimulus) is obtained and if the system is tested keeping it at K_a knob setting and from the response, specifications for all possible knob settings are predicted then the prediction error will be minimum for this test stimulus.

6.5.3. Tuning knob selection

In this step, the best set of tuning knobs are selected from all possible tuning knob settings so that when the system is tested at those carefully selected knob settings and specifications for all knob settings are predicted then prediction error becomes as small as possible. This is achieved by using a gradient based search algorithm. If '*m*' number of knob settings are selected for testing, then initially the search is performed in the whole tuning knob space and the best knob is selected for which the prediction error is minimum with optimized test signal. While selecting the next best knob setting, the

search is performed within the knob settings where specification prediction accuracy was poor in previous step. Every time this search is performed, test generation is done for each of the knob settings. The key idea here is that result of test generation and accuracy of regression models will be different for a large knob space and a smaller sub-region of that knob space.

6.5.4. Adaptive system testing

The complete concept of adaptive system testing is shown in Figure 55. The flow chart is explained below.

A gradient based search algorithm is applied to select the tuning knob settings where the system should be tested. This is done in an iterative way for selecting '*m*' number of optimal knobs. When the system is tested at a particular knob setting and specifications are predicted for other knob settings from the test result, prediction accuracy will be poor in certain regions of the tuning knob space. Hence, an iterative algorithm is developed and the knob space is gradually shrunk in every iteration. After the iterations are complete, several sub-regions of the tuning knob space are obtained and the optimal knob setting for each subregion is determined which gives best prediction for that subregion. Let us define S_k to be the set of all tuning knobs settings where the performance of the system has to be predicted in an iteration (initially S_k is the whole tuning knob space).

For selecting the first optimal knob setting, the gradient based search algorithm selects a knob K_i from S_k (the whole knob space initially) and an optimized test stimulus is generated for K_i. Then the system is kept at K_i and from the test response of the system, different specifications (gain, IIP3 and power consumption) are predicted for all knob settings in S_k using a trained regression model. Then the gradient based search algorithm repeats this process for other tuning knob settings and finds the tuning knob setting for

which the total prediction error is minimum. This knob setting is chosen as the first optimal tuning knob setting.

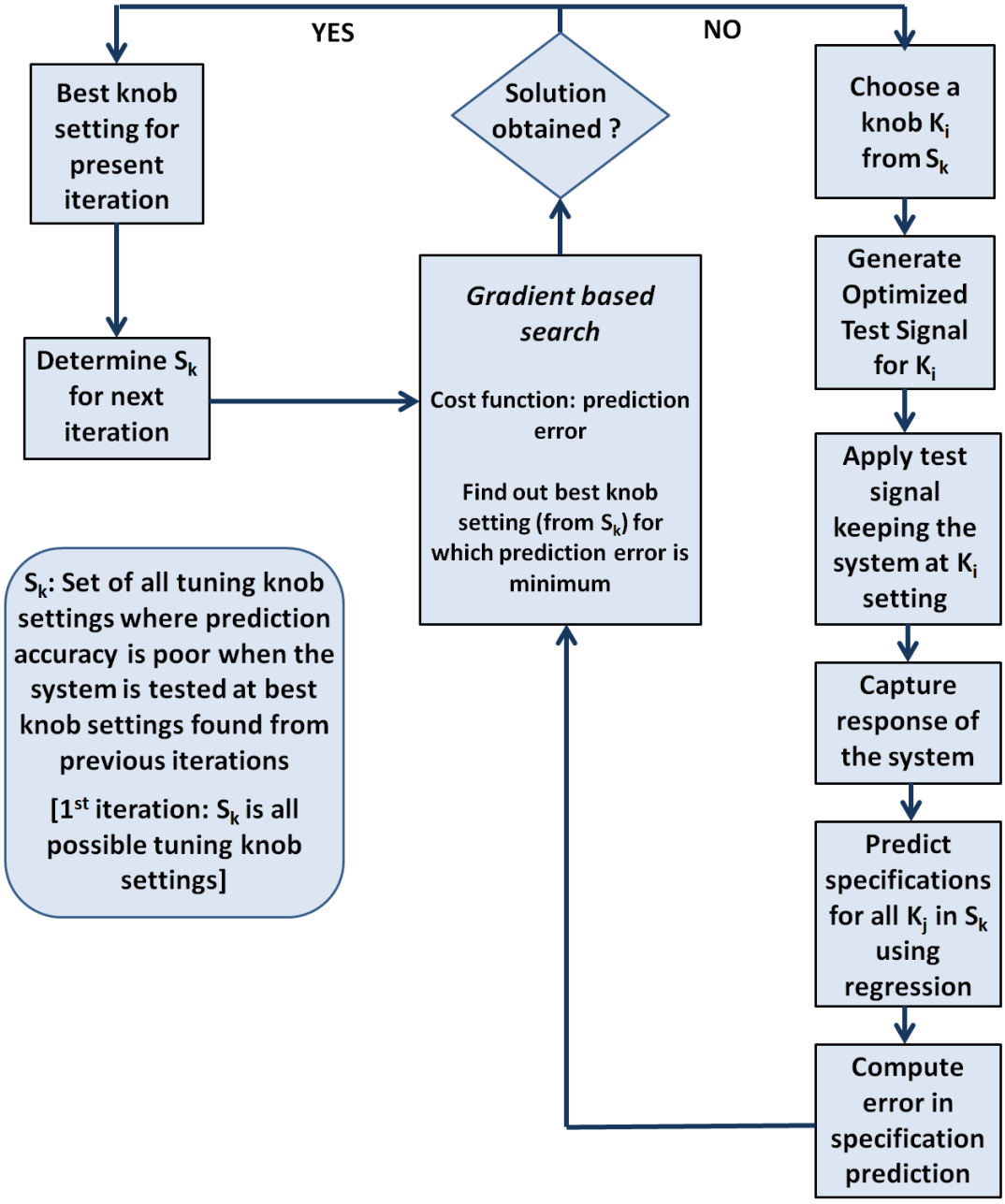


Figure 55. Adaptive system testing approach

Now, the knob settings are found where the prediction is not accurate when the system is tested at first optimal knob setting. A threshold is assigned in accuracy of specification prediction for this purpose. The knob settings where the prediction error is greater than this threshold value are selected and this set of knobs is called 'S_{error}'. The first optimal knob setting is used to predict specifications for the knob space [S_k - S_{error}].

Then the knob space S_{error} (where prediction accuracy is poor when the system is tested at the first optimal knob) is chosen as the new S_k for the next iteration. The second optimal knob setting is found from this new S_k and the objective function for this second knob selection is defined as the prediction error for knobs in this new S_k. Again test stimulus optimization algorithm and gradient search algorithm are applied in this new S_k knob space and the second optimal knob setting is selected. Now the threshold value is increased from the first iteration and the knobs where prediction error is greater than this new threshold are selected (new S_{error}). Second optimal knob is used for specification prediction of the space [new S_k - new S_{error}]. This procedure is repeated for further optimal tuning knob settings and the threshold value for selecting S_k in each iteration is increased gradually.

6.6. Simulation Results

The proposed concept is validated by performing simulation and the results are presented in this section.

6.6.1. Adaptive transmitter design

An adaptive RF transmitter is designed in ADS for 2.4 GHz where tuning knobs are incorporated in the upconversion mixer. Bias voltage and power supply of the mixer are used as two tuning knobs which are controlled from the baseband unit. An envelope detector is placed at the output of the transmitter that captures the low frequency envelope response of the transmitted signal as shown in Figure 3. Process variation is

introduced in ADS simulation and several instances are created. Three specifications of the system - gain, IIP3 and power consumption are considered for testing. The schematic of the adaptive double balanced Gilbert cell up-conversion mixer is shown in Figure 56.

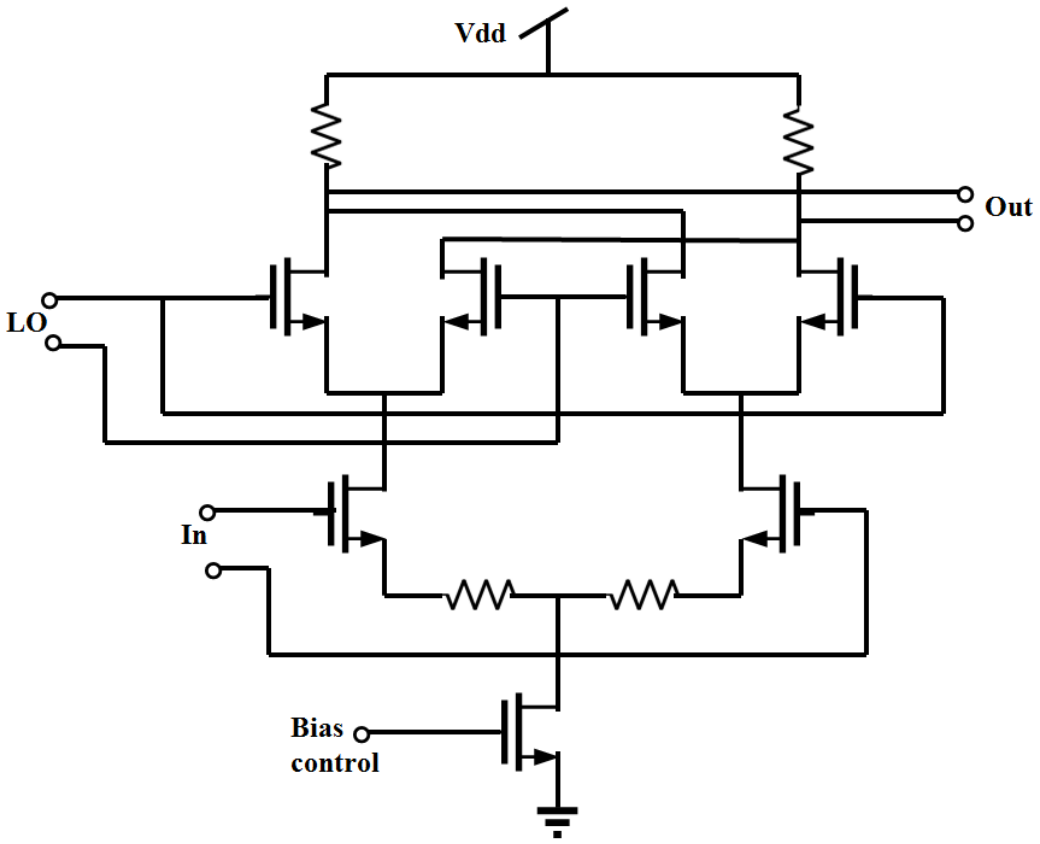


Figure 56. Adaptive Gilbert cell mixer

6.6.2. Test generation

Genetic algorithm based test stimulus optimization is performed in MATLAB and the performance of the Genetic algorithm for one of the tuning knob settings is shown in Figure 57. It shows how the value of objective function (error in specification prediction when the system is tested at that particular setting) reduces as GA converges. The

optimized multi-tone OFDM test signals for I and Q inputs for that knob setting are presented in Figure 58.

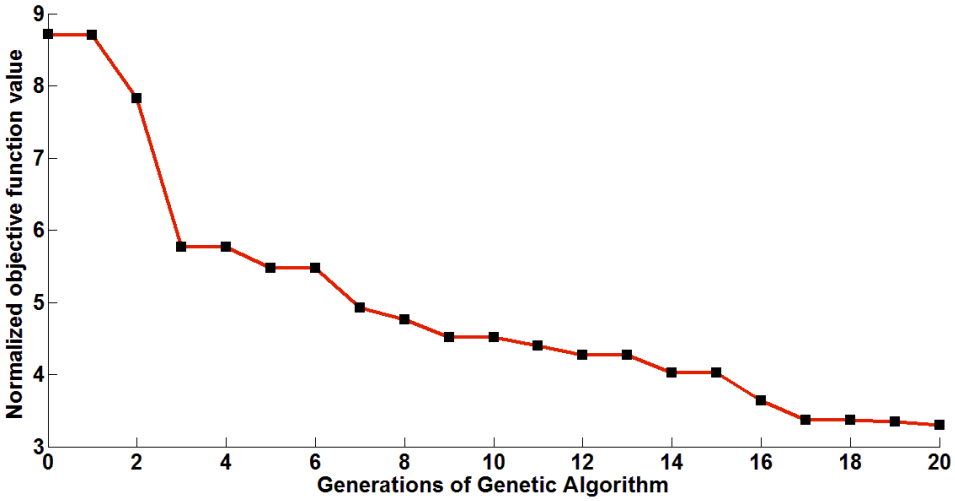


Figure 57. Test generation using GA

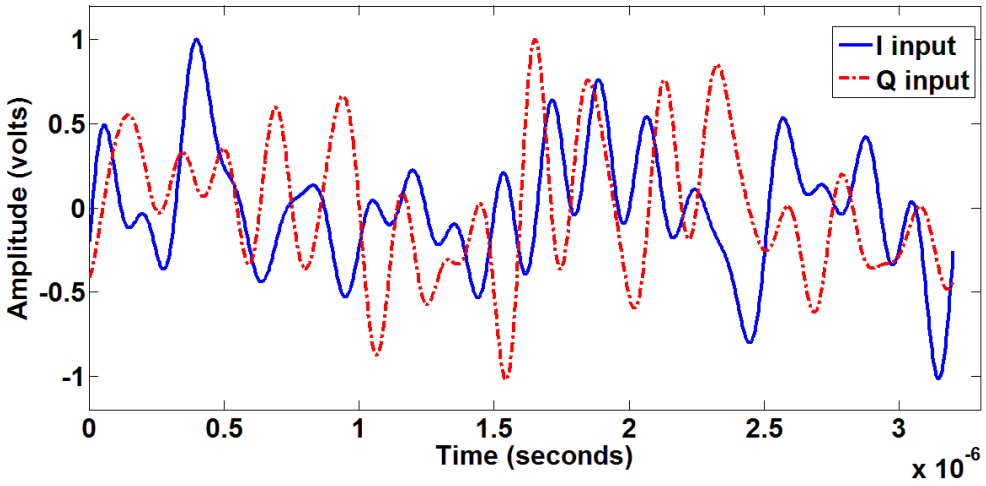


Figure 58. Optimized multi-tone test stimuli

6.6.3. Tuning knob selection

Tuning knob settings where the system should be tested are found using a MATLAB based gradient search algorithm [47]. The first tuning knob is selected in such a way that total prediction error across all knob settings is minimized. The threshold value for selecting S_k of next iteration is set adaptively. The first optimal knob setting is found to be *knob1 = [Vdd: 2 volts, bias: 0.8 volts]*. The next step is to determine S_k for second knob setting. The threshold is set to 1.5 of total normalized prediction error for all of the specifications considered. 15 knobs settings are obtained out of 65 knob settings where this error value is greater than 1.5 and these knob settings construct S_k for second iteration. In the second iteration the search is performed again within these 15 knob settings to find the best one where the system should be tested for best prediction accuracy. The second knob setting is found to be *knob2 = [Vdd: 2.8 volts, bias: 0.6 volts]*. Next, the error threshold is set to 2.5 and 4 knobs which fall outside this error threshold construct S_k for third knob selection. The gradient based optimizer finds the third knob as *knob3 = [Vdd: 2.7 volts, bias: 0.5 volts]*.

6.6.4. Surface prediction results

In the validation phase, another set of process varied transmitter instances are selected and all of them are tested at the 3 knob settings found in Section 6.6.3 using corresponding optimized multi-tone test signals. First, the instances are tested at *knob1* and the responses of the instances to the optimized test signal for *knob1* are captured. Then the instances are kept at *knob2* and responses to the optimized signal for *knob2* are captured. Similarly, they are tested for *knob3* as well. Then 60% of these instances are used to train MARS [30]. Regression models are built between the following parameters: response at *knob1* and specifications of 50 knob settings, response at *knob2* and 11 knob settings and response at *knob3* and 4 knob settings. For the rest of the 40% instances, their gain, IIP3 and power consumption specifications are predicted using their responses

and the regression models built. Prediction results for a particular instance are shown in Figure 59, 60 and 61. Total normalized prediction error for all these 3 specifications over the 40% of the validation instances is shown in Figure 62.

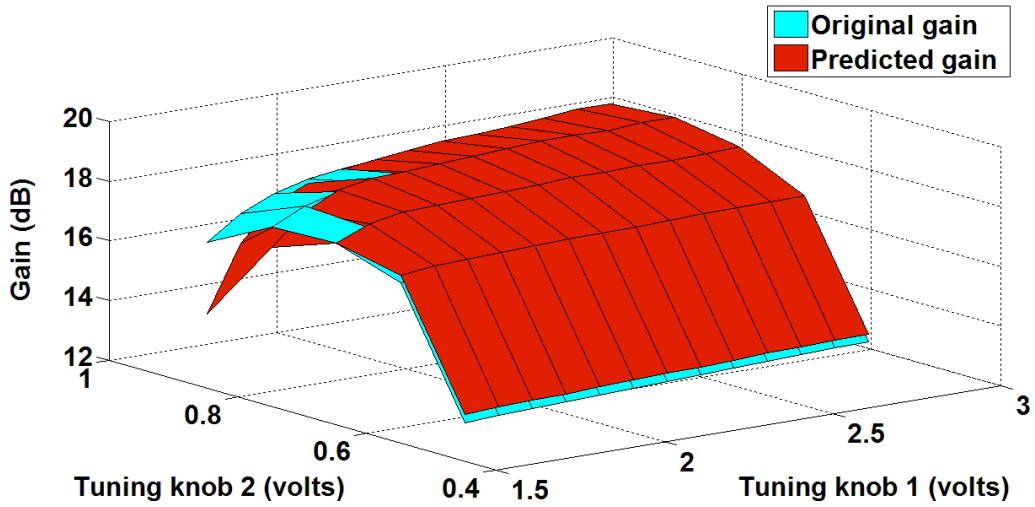


Figure 59. Gain prediction

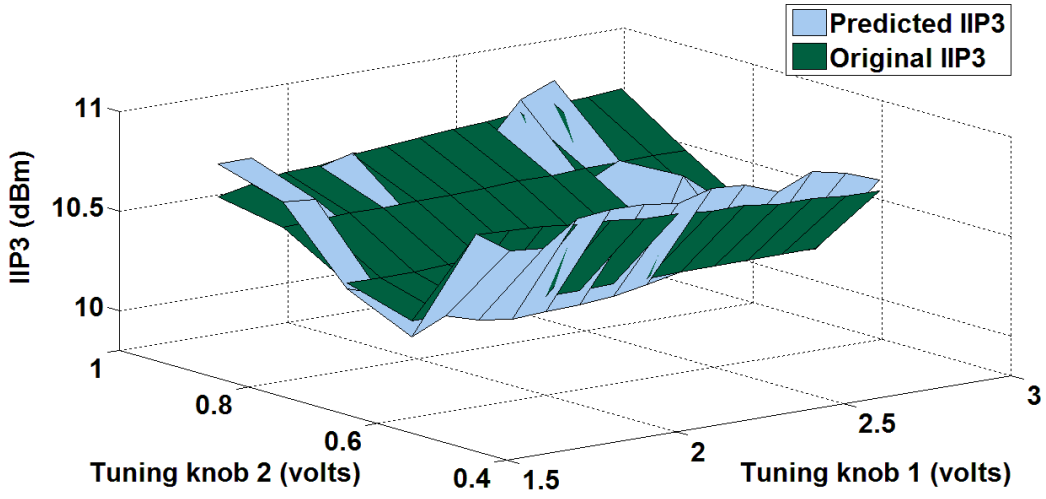


Figure 60. IIP3 prediction

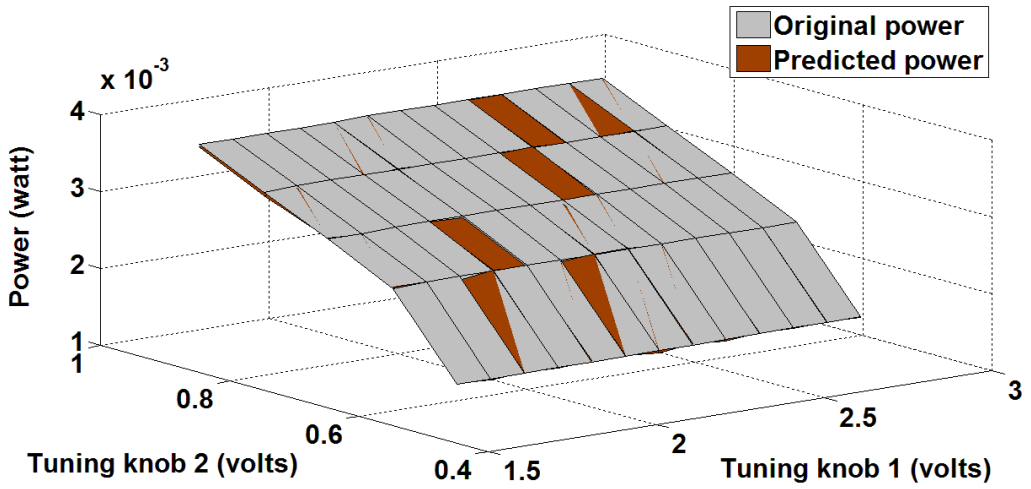


Figure 61. Power consumption prediction

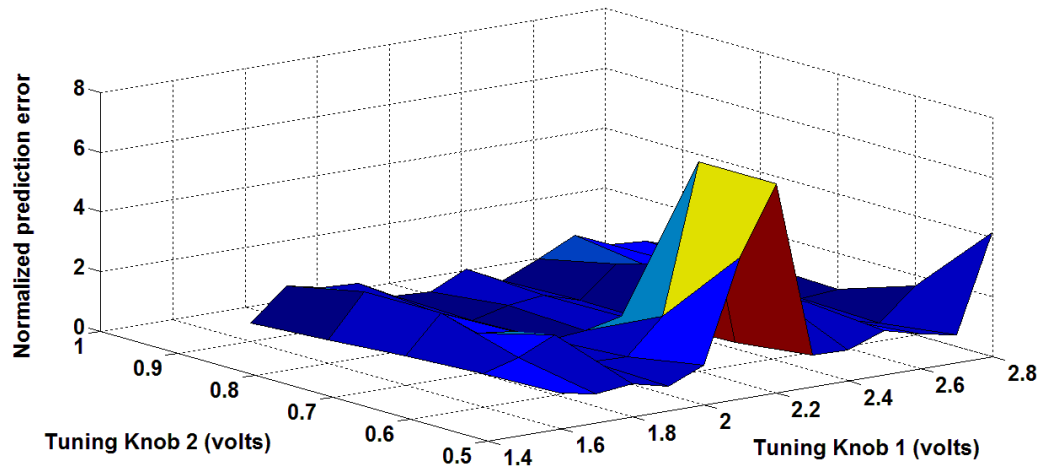


Figure 62. Total normalized error distribution

6.7. Measurement Results

The validity of the proposed test technique is shown by conducting experiment on a hardware prototype as shown in Figure 63. A 802.11a/b/g power amplifier in

production at TI is used in the experiment. A data acquisition module by National Instruments (NI PXIe-1073) is used to interface the RF front-end with PC. Multi-tone test signal is up-converted using a mixer from RFMD (RF2638) and LO signal is generated using RF source Agilent E4432B. This up-converted signal is fed to the RF tester board that hosts the power amplifier module. Output of the power amplifier is down-converted using the mixer MAX2039 and digitized by the ADC from NI. In this experiment 12 process varied instances of power amplifier are used while the mixers are kept static. Power supply and a control voltage of the power amplifier are used as tuning knobs. Out of these 12 instances, 9 are used to build the regression model and performance (gain) of rest of the 3 instances are predicted using built regression models. Average prediction error for these three instances are shown in Table 8. Original and predicted gain surfaces of one of these instances are presented in Figure 64.

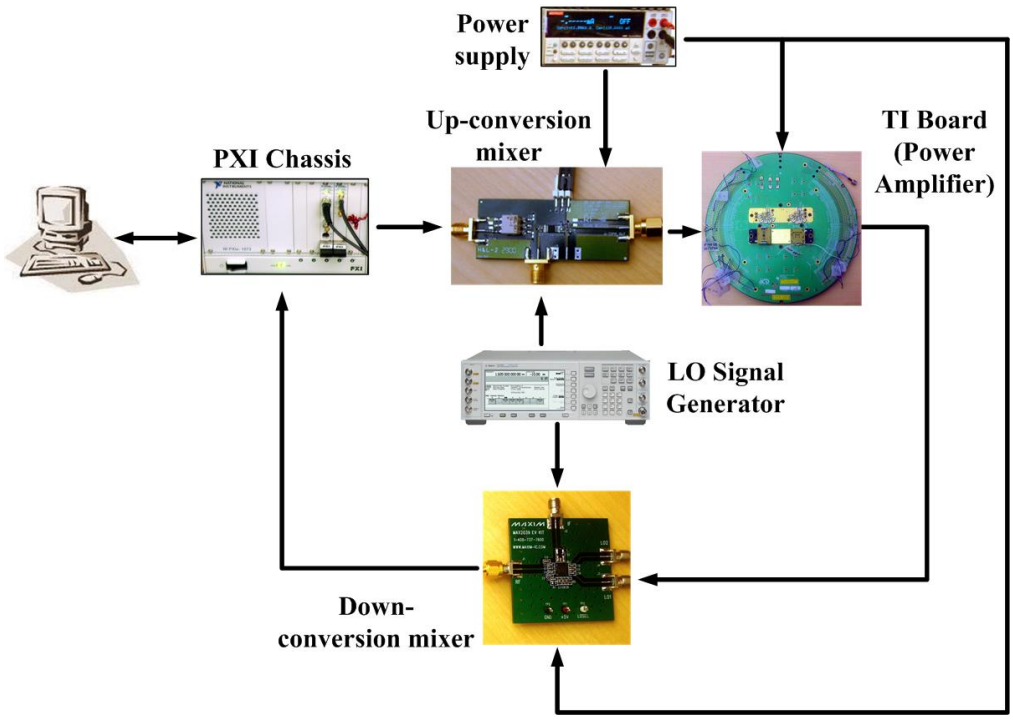


Figure 63. Hardware experiment setup for the proposed adaptive system test

Table 8. Prediction error in hardware experiment

Instance number	Instance 1	Instance 2	Instance 3
Average error	4.4 %	7.2%	3.6%

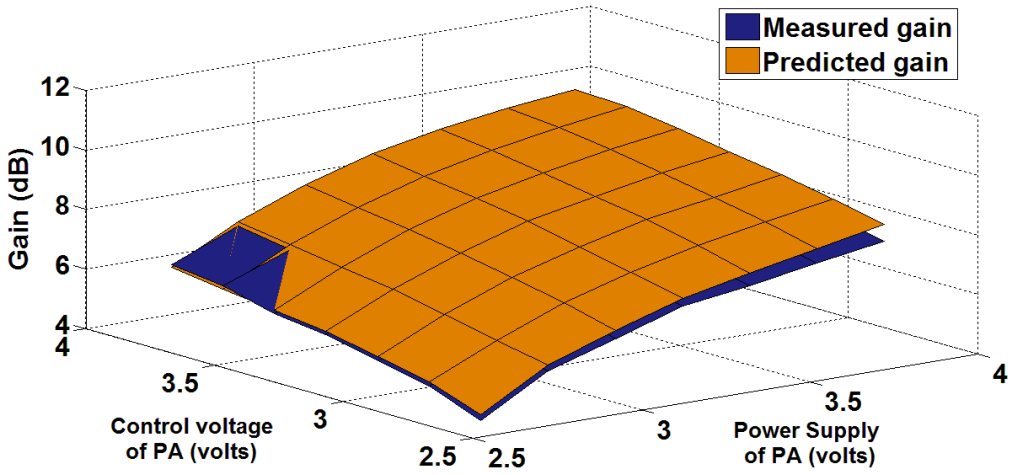


Figure 64. Gain prediction results of the hardware experiment

6.8. Application of the Proposed Test

Using the proposed method, performance of an adaptive system can be predicted across different tuning knob settings. This prediction result can be used in following ways:

6.8.1. Process adaptation

Once the results of the proposed test are obtained, power conscious tuning algorithms can be applied directly on the predicted performance surfaces of the system. Thus the proposed method can save significant tuning time. On the other hand, if the

tuning (search) algorithm is applied on hardware (for better accuracy) [22], then the results of the same tuning algorithm on the predicted surfaces can provide starting point of the hardware iteration and help in fast convergence.

6.8.2. Workload adaptation

In the case of workload adaptation, the results of the proposed test can be equally useful. For a system to adapt to its workload (channel condition for a RF transceiver) in a power optimal way, enough tuning range is required in its specifications. Whether a particular process varied instance can be used in such an adaptation mechanism can be determined by the results of the proposed test which clearly shows the tuning range for every specification. Different workload conditions can be simulated and adaptation mechanism can be verified by directly using the prediction data.

CHAPTER 7

CONCLUSION AND FUTURE WORK

The objective of the proposed research is to design adaptive analog/RF circuits and systems with digital enhancement techniques for higher performance, better process variation tolerance, and more reliable operation and developing strategy for testing the proposed adaptive systems.

7.1. Conclusions

An adaptation framework for RF systems is developed that can mitigate the effects of process variation by trading-off power and performance of the individual modules. The proposed framework has two parts – (1) optimized test stimulus driven top-down diagnosis, where module level performance and nonidealities are computed from the system level test response of the RF transceiver and (2) bottom-up tuning (adaptation) that utilizes diagnosis results to predict performance vs. power vs. tuning knob relations and finds out optimal tuning knob settings to meet performance requirements with minimum power consumption. Another adaptation technique is proposed for process variation tolerance that directly finds out power optimal tuning solution from the test response of the circuit. This tuning mechanism is successfully applied to an adaptive analog circuit (operational amplifier) designed using carbon nanotube transistors which show different types of manufacturing variation compared to CMOS. An adaptive switched mode power amplifier is also designed which has higher efficiency with power back-off, better process variation tolerance and higher reliability compared to a static design. This power amplifier can be used in the proposed adaptation framework as one of the adaptive modules of the RF system. Finally, a testing strategy is developed for the

proposed adaptive system and the proposed test methodology obviates the need to test the device at all possible tuning knob settings and thus saves test time and test cost.

Key contributions of this PhD thesis are listed below:

(A) The proposed diagnosis technique uses compact and deterministic test stimuli which are optimized to improve accuracy of model parameter computation. Usage of these optimized test stimuli results in significant reduction in diagnosis and testing time. A comprehensive behavioral model of the RF transceiver is developed and using that model the proposed algorithm can find out nonidealities of individual modules of the RF transceiver from the system level response only, which minimizes the number of sensors to be used in the RF path.

(B) A process variation tolerant adaptation or tuning technique is developed which performs module level diagnosis and predicts performance specifications and power consumption across tuning knob settings. By predicting performance surfaces at the module level and then finding out system level tuning solution, dimensions of the tuning problem is reduced which results in less number of diagnosis points, more accurate prediction of performance surfaces and obviates any training requirement. Eventually it leads to faster adaptation of the RF system.

(C) Tuning of carbon nanotube based analog circuit demonstrates the efficiency of the direct tuning approach in presence of manufacturing variations which are different in nature (compared to CMOS based circuits) and shows requirement of different kind of tuning knobs in such an environment.

(D) Proposed adaptive class-E power amplifier demonstrates better reliability, process variation tolerance and higher efficiency with power back-off. Simplicity of the proposed tuning circuit results in less overhead and simple control law which is easy to implement.

(E) Proposed adaptive system testing approach finds out optimal tuning knob settings where the device should be tested and predicts performance for all other knob

settings. Thus, it leads to reduction in test time and test cost for adaptive analog / RF systems by predicting closed loop performance from open loop test results.

7.2. Future Work

This PhD work contributes to the development of digitally assisted adaptive analog / RF circuits and systems and some possible extensions of the proposed research are listed below:

(1) In the proposed diagnosis technique any effect which is not captured by the behavioral model can be incorporated by using some learning algorithm which can improve the DUT model iteratively.

(2) The adaptation framework can be extended to compensate temporal effects (aging) and lifetime of the RF system can be increased by distributing stress appropriately across the modules.

(3) Manufacturing variations in other nanodevices (such as Graphene) can be studied and efficient self-healing mechanism can be developed for circuits built using those devices by finding out effective tuning parameters (knobs).

(4) Tunable design of other RF modules (mixers, low noise amplifiers) can be further explored with different adaptation settings for simultaneous improvement in process tolerance, performance and reliability which can be used in the proposed framework.

7.3. Publications

[A1] Aritra Banerjee, Shyam Devarakond, Vishwanath Natarajan, Shreyas Sen and Abhijit Chatterjee, "Optimized digital compatible pulse sequences for testing of RF front end modules," *IEEE 16th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW)*, pp. 1-6, 7-9 June 2010.

[A2] Aritra Banerjee, Vishwanath Natarajan, Shreyas Sen, Abhijit Chatterjee, Ganesh Srinivasan and Soumendu Bhattacharya, "Optimized Multitone Test Stimulus Driven Diagnosis of RF Transceivers Using Model Parameter Estimation," *IEEE 24th International Conference on VLSI Design*, pp. 274-279, 2-7 Jan. 2011.

[A3] Aritra Banerjee, Shreyas Sen, Shyam Devarakond and Abhijit Chatterjee, "Automatic test stimulus generation for accurate diagnosis of RF systems using transient response signatures," *IEEE 29th VLSI Test Symposium (VTS)*, pp. 58-63, 1-5 May 2011.

[A4] Aritra Banerjee, Subho Chatterjee, Azad Naeemi and Abhijit Chatterjee, "Power Aware Post-manufacture Tuning of Analog Nanocircuits," *16th IEEE European Test Symposium (ETS)*, pp. 57-62, 23-27 May 2011.

[A5] Aritra Banerjee, Shreyas Sen, Shyam Devarakond and Abhijit Chatterjee, "Accurate signature driven power conscious tuning of RF systems using hierarchical performance models," *IEEE International Test Conference (ITC)*, pp. 1-9, 20-22 Sept. 2011.

[A6] Aritra Banerjee, Shyam Devarakond, Shreyas Sen, Debashis Banerjee and Abhijit Chatterjee, "Optimal Testing of Digitally Assisted Adaptive RF Systems," *IEEE 18th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW)*, pp. 46-51, 14-16 May 2012.

[A7] Aritra Banerjee, Shyam Devarakond, Shreyas Sen, Debashis Banerjee and Abhijit Chatterjee, "Testing of digitally assisted adaptive analog/RF systems using tuning knob - performance space estimation," *17th IEEE European Test Symposium (ETS)*, pp. 1, 28-31 May 2012.

[A8] Aritra Banerjee and Abhijit Chatterjee, "An Adaptive Class-E Power Amplifier With Improvement In Efficiency, Reliability And Process Variation Tolerance," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 745-748, 19-23 May 2013.

[A9] Aritra Banerjee and Abhijit Chatterjee, "Automatic Test Stimulus Generation for Diagnosis of RF Transceivers Using Model Parameter Estimation," under review in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

[A10] Aritra Banerjee and Abhijit Chatterjee, "Signature Driven Hierarchical Post-manufacture Tuning of RF Systems for Performance and Power," to be submitted in *IEEE Transactions on Very Large Scale Integration Systems*.

[A11] Shyam Devarakond, Shreyas Sen, Aritra Banerjee, Vishwanath Natarajan and Abhijit Chatterjee, "Built-in performance monitoring of mixed-signal/RF front ends using real-time parameter estimation," *IEEE 16th International On-Line Testing Symposium (IOLTS)*, pp. 77-82, 5-7 July 2010.

[A12] Vishwanath Natarajan, Shreyas Sen, Aritra Banerjee, Abhijit Chatterjee, Ganesh Srinivasan and Friedrich Taenzler, "Analog Signature Driven Post-manufacture Multidimensional Tuning of RF Systems," *IEEE Design & Test of Computers*, Vol. 27, No. 6, pp. 6-17, Nov.-Dec. 2010.

[A13] Shyam Devarakond, Shreyas Sen, Vishwanath Natarajan, Aritra Banerjee, Hyun Choi, Ganesh Srinivasan and Abhijit Chatterjee, "Digitally Assisted Concurrent Built-In Tuning of RF Systems Using Hamming Distance Proportional Signatures," *19th IEEE Asian Test Symposium (ATS)*, pp. 283-288, 1-4 Dec. 2010.

[A14] Sehun Kook, Aritra Banerjee and Abhijit Chatterjee, "Signature Testing and Diagnosis of High Precision ΣΔ ADC Dynamic Specifications Using Model Parameter Estimation," *16th IEEE European Test Symposium (ETS)*, pp. 33-38, 23-27 May 2011.

[A15] Shyam Devarakond, Debashis Banerjee, Aritra Banerjee, Shreyas Sen and Abhijit Chatterjee, "DSP Driven Parallel EVM Testing of Embedded MIMO-OFDM RF Modules," *IEEE 18th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW)*, pp. 40-45, 14-16 May 2012.

[A16] Sabyasachi Deyati, Aritra Banerjee and Abhijit Chatterjee, "Pilot symbol driven monitoring of electrical degradation in RF transmitter systems using model anomaly diagnosis," *IEEE 18th International On-Line Testing Symposium (IOLTS)*, pp. 142-145, 27-29 June 2012.

[A17] Vishwanath Natarajan, Hyun Choi, Aritra Banerjee, Shreyas Sen, Abhijit Chatterjee, Ganesh Srinivasan, Friedrich Taenzler and Soumendu Bhattacharya, "Low Cost EVM Testing of Wireless RF SoC Front-Ends Using Multitones," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 31, No. 7, pp. 1088-1101, July 2012.

[A18] Debashis Banerjee, Shreyas Sen, Aritra Banerjee and Abhijit Chatterjee, "Low-power adaptive RF system design using real-time fuzzy noise-distortion control," *ACM/IEEE international symposium on Low power electronics and design (ISLPED)*, pp. 249-254, 30 July - 1 Aug. 2012.

[A19] Abhijit Chatterjee, Sabyasachi Deyati, Barry Muldrey, Shyam Devarakond and Aritra Banerjee, "Validation signature testing: A methodology for post-silicon validation of analog/mixed-signal circuits," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 553-556, 5-8 Nov. 2012.

[A20] Abhijit Chatterjee, Sabyasachi Deyati, Barry Muldrey, Shyam Devarakond, Aritra Banerjee and Michael Giardino, "Signature Testing for Post Silicon Validation of RF/Analog Circuits," *8th IEEE International Workshop on Silicon Debug and Diagnosis (SDD)*, 8-9 Nov. 2012.

[A21] Shreyas Sen, Aritra Banerjee, Vishwanath Natarajan, Shyam Devarakond, Hyun Choi and Abhijit Chatterjee, "BIST/Digital-Compatible Testing of RF Devices Using Distortion Model Fitting," *Journal of Electronic Testing*, Vol. 28, No. 4, pp. 405-419, 2012.

[A22] Sabyasachi Deyati, Aritra Banerjee, Barry J. Muldrey and Abhijit Chatterjee, "VAST: Post-Silicon VAlidation and Diagnosis of RF/Mixed-Signal Circuits Using Signature Tests," *IEEE 26th International Conference on VLSI Design*, pp. 314-319, 5-10 Jan. 2013.

[A23] Debashis Banerjee, Aritra Banerjee and Abhijit Chatterjee, "Adaptive RF Front-end Design via Self-discovery: Using Real-time Data to Optimize Adaptation Control," *IEEE 26th International Conference on VLSI Design*, pp. 197-202, 5-10 Jan. 2013.

[A24] Debesh Bhatta, Aritra Banerjee, Sabyasachi Deyati, Nicholas Tzou and Abhijit Chatterjee, "Low Cost Signal Reconstruction Based Testing of RF Components Using Incoherent Undersampling," *14th Latin American Test Workshop*, pp. 1-5, 3-5 April 2013.

[A25] Shyam Kumar Devarakond, Debashis Banerjee, Aritra Banerjee, Shreyas Sen and Abhijit Chatterjee, "Efficient System-Level Testing and Adaptive Tuning of MIMO-OFDM Wireless Transmitters," *18th IEEE European Test Symposium*, pp. 1-6, 27-31 May 2013.

[A26] Suvadeep Banerjee, Aritra Banerjee, Abhijit Chatterjee and Jacob Abraham, "Real-Time Checking of Linear Control Systems Using Analog Checksums," *19th IEEE International On-Line Testing Symposium (IOLTS)*, 8-10 July 2013.

[A27] Debashis Banerjee, Aritra Banerjee, Shyam Devarakond and Abhijit Chatterjee, "Adaptive MIMO RF Systems: Post-Manufacture and Real-Time Tuning for Performance Maximization and Power Minimization," *IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1095-1099, 4-7 Aug. 2013.

[A28] Sehun Kook, Aritra Banerjee and Abhijit Chatterjee, "Dynamic Specification Testing and Diagnosis of High Precision Sigma-Delta ADCs," accepted in *IEEE Design & Test of Computers*.

[A29] Abhijit Chatterjee, Hua Wang, Aritra Banerjee, Debashis Banerjee and Vishwanath Natarajan, "Towards Design of Truly Scalable Self-Healing Mixed-Signal/RF Systems and Support CAD Tools," submitted in *27th International Conference on VLSI Design*, 2014.

[A30] Vishwanath Natarajan, Aritra Banerjee et al., "Yield Recovery of RF Transceiver Systems Using Iterative Tuning-Driven Power Conscious Performance Optimization," to be submitted in *IEEE Design & Test of Computers*.

[A31] Debesh Bhatta, Aritra Banerjee, Sabyasachi Deyati, Nicholas Tzou and Abhijit Chatterjee, "Low cost measurement of amplitude and phase distortion of RF components using incoherent undersampling," to be submitted in *Journal of Electronic Testing*.

[A32] Shyam Devarakond, Aritra Banerjee, Shreyas Sen, Ganesh Srinivasan and Abhijit Chatterjee, "Digitally Assisted Concurrent Built-In Tuning of RF Systems Using Hamming Distance Proportional Signature," to be submitted.

[A33] Suvadeep Banerjee, Aritra Banerjee, Debashis Banerjee and Abhijit Chatterjee, "Built-In Self Test of RFID Tags for Pass/Fail Detection," to be submitted.

7.4. Patent

[B1] Aritra Banerjee and Abhijit Chatterjee, "Adaptive Power Amplifiers and Methods of Making Same," Georgia Tech Research Corporation Ref. No. 6210, MARCO Ref. No. P1412, U.S. Patent Application Serial No.: 13/897,152, filed on 17th May 2013.

7.5. Awards

[C1] Received IEEE MTT-S Graduate Fellowship 2012 by IEEE Microwave Theory and Techniques Society (this award was given to 10 students all over the world).

[C2] Received Student Travel Award 2013 by IEEE Circuits and Systems Society.

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