EXPERIMENTAL AND THEORETICAL ASSESSMENT OF THROUGH-SILICON VIAS FOR 3D INTEGRATED MICROELECTRONIC PACKAGES

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EXPERIMENTAL AND THEORETICAL ASSESSMENT OF THROUGH-SILICON VIAS FOR 3D INTEGRATED MICROELECTRONIC PACKAGES

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To my grandmother
To my parents
To my uncle and aunt

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LIST OF SYMBOLS AND ABBREVIATIONS

2D	Two dimensional
2.5D	Two-and-a-half-dimensional
3D	Three dimensional
AFM	Atomic force microscopy
BGA	Ball grid array
BW	Bandwidth
CFDA	Centered finite-difference approach
CLT	Classic laminate theory
CPU	Central processing unit
CTE	Coefficient of thermal expansion
Cu	Copper
$CuCl_2$	Copper (II) chloride
DAXM	Differential aperture x-ray microscopy
DC	Direct current
DISC	Digital image speckle correlation
DMA	Dynamic mechanical analysis
DOE	Design of experiment
DOS	Design of simulation
DRAM	Dynamic random access memory
FC	Flip-chip
FE	Finite-element
GPU	Graphic processing unit
IC	Integrated circuit

ICP	Inductively coupled plasma
IMC	Intermetallic compound
I/O	Input/output
LGA	Land grid array
PCB	Printed circuit board
PDF	Powder diffraction file
PECVD	Plasma-enhanced chemical vapor deposition
PiP	Package in package
PoP	Package on package
RDL	Re-distribution layer
SEM	Scanning electron microscope
Si	Silicon
SiO_2	Silicon dioxide
Ti	Titanium
TSV	Through-silicon via
UV	Ultraviolet
VCCT	Virtual crack closure technique
X-MAS	X-ray microdiffraction analysis software
XRD	X-ray diffraction

SUMMARY

With continued push toward 3D integrated packaging, Through-Silicon Vias (TSVs) play an increasingly important role in interconnecting stacked silicon dies. Although progress is being made in the fabrication of TSVs, experimental and theoretical assessment of their thermomechanical reliability is still in infancy. This work explores the thermomechanical reliability of TSVs through numerical models and innovative experimental characterization techniques. Starting with free-standing wafers, this work examines failure mechanisms such as Si and SiO_2 cohesive cracking as well as SiO_2/Cu interfacial cracking. Such cohesive crack propagation and interfacial crack propagation are studied using fracture mechanics finite-element modeling, and the energy available for crack propagation is determined through crack extension using the proposed centered finite-difference approach (CFDA). In parallel to the simulations, silicon wafers with TSVs are designed and fabricated and subjected to thermal shock test. Cross-sectional SEM failure analysis is carried out to study cohesive and interfacial crack initiation and propagation under thermal excursions. In addition, local micro-strain fields under thermal excursions are mapped through synchrotron X-ray diffraction. To understand the 3D to 2D strain measurement data projection process, a new data interpretation method based on beam intensity averaging is proposed and validated with measurements. Building upon the work on free-standing wafers, this research studies the package assembly issues and failure mechanisms in multi-die stacks. Comprehensive design-of-simulations study is carried out to assess the effect of various material and geometry parameters on the reliability of 3D microelectronic packages. Through experimentally-measured strain fields, thermal cycling tests, and simulations, design guidelines are developed to enhance the thermomechanical reliability of TSVs used in future 3D microelectronic packages.

CHAPTER 1

INTRODUCTION

1.1 Background

In 1965, Gordon Moore stated that the number of transistors per integrated circuits (IC) doubles approximately every two years [1]. Over the last 50 years, both industry and academia have been striving to make this empirical assessment prevail (Figure 1.1). Advances in nanotechnology may extend the trend for a much longer time than we expected. However, as IC/transistor miniaturization reaches its physical limit and the associated cost spike, we are compelled to search for new, more cost-effective innovations (Figure 1.2) to continue advances in microelectronics [2-4]. Three-dimensional (3D) package integration is one such innovation, which has garnered tremendous interest in recent years.

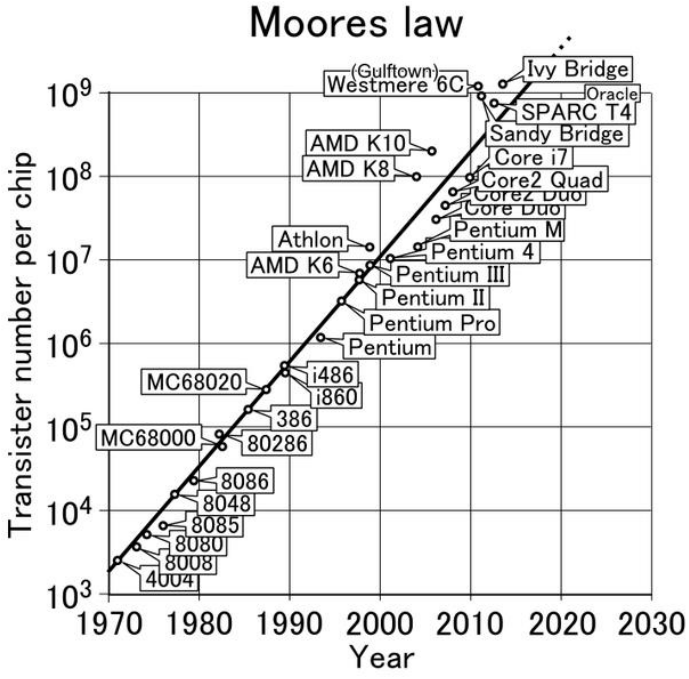


Figure 1.1: Moore's law (Source: Wikimedia)

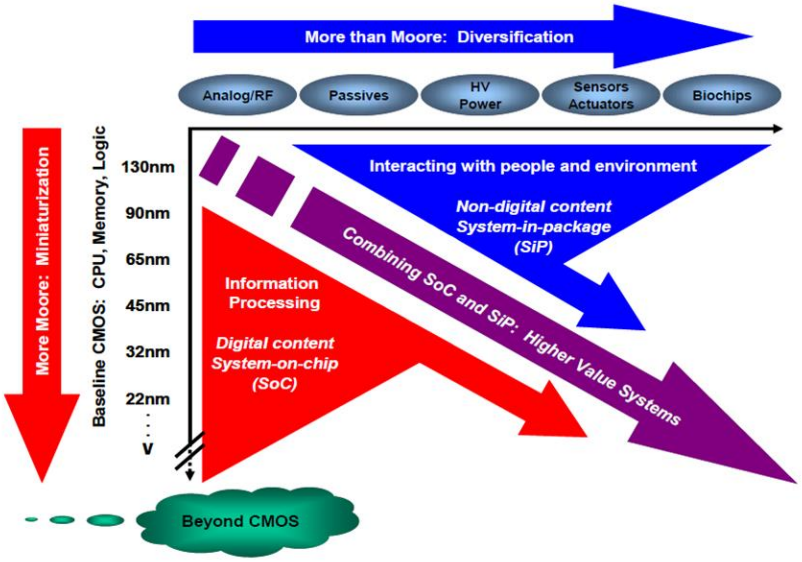


Figure 1.2: More-than-Moore (Source: ITRS white paper "More-than-Moore")

1.1.1 Motivation for 3D integrated packaging with TSVs

As discussed above, over the last decade, electronic systems continue to move toward 3D integration to meet the ever-increasing demands of better performance, more functions, higher I/O density, smaller form factor, lower power consumptions, and lower cost [2, 4-6]. Various 3D integration technologies have been proposed, for example, Package on Package (PoP) (Figure 1.3), System in Package (SiP) (Figure 1.4), 3D IC integration (Figure 1.5 and Figure 1.6), 3D silicon integration (Figure 1.7). Among them, PoP, PiP, and die stack with wire bond are mature technologies and are already in production. 3D stacked die with TSVs and 3D silicon integration are mostly in the research and development stage due to yield, test, and thermal management issues.

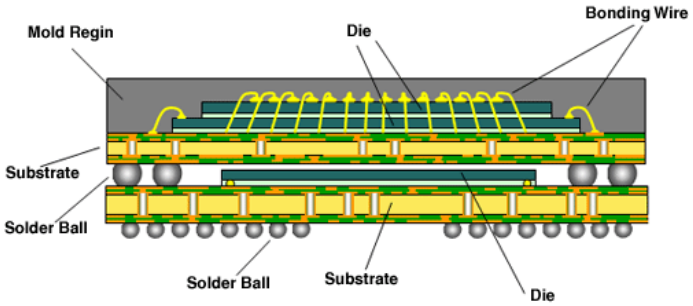


Figure 1.3: Package on package (Source: Toshiba)

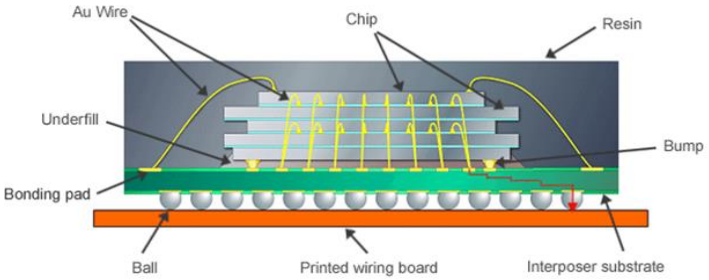


Figure 1.4: System in package (Source: Renesas Electronics)

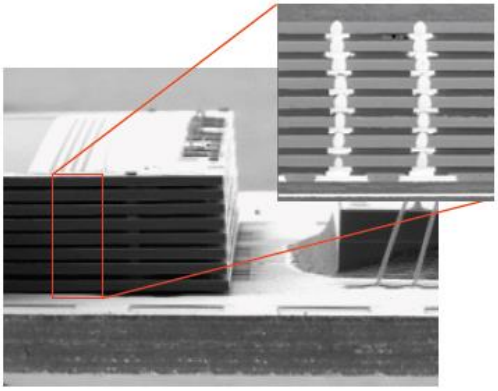


Figure 1.5: Die stack with TSVs (Source: Samsung)

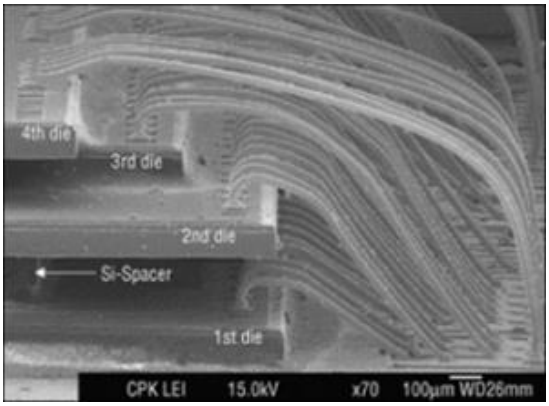


Figure 1.6: Die stack with wire bonds (Source: soccentral.com)

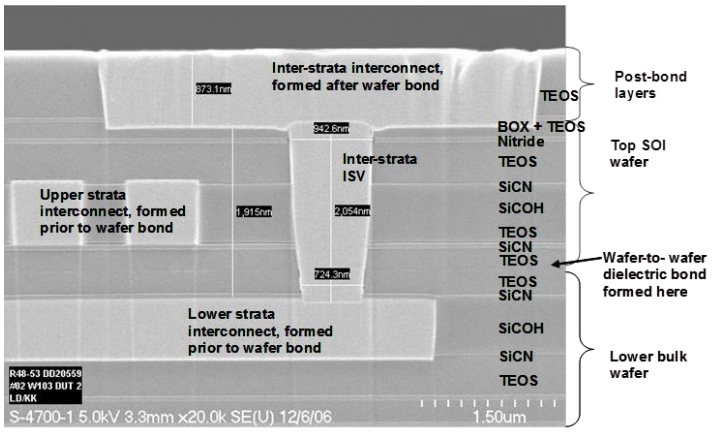


Figure 1.7: 3D silicon integration (Source: Freescale)

Among the various 3D integration technologies, stacked dies with through-silicon vias provide the shortest interconnection between different tiers. Thus, potentially it may be one of the most promising technologies that can achieve the ultimate goal of 3D integration. Take a computer or graphic system as an example. Memory bandwidth (BW) is a major bottleneck that limits system performance. This is even more crucial in multi-core, high-performance computing and graphic systems, where demand for memory BW quickly reaches the scale of tera-byte per second (TB/s). This bottleneck is mainly due to limited memory bus width and input/output (I/O) speed. Memory bus width is determined by the number of interconnections between a logic chip, such as a central or graphic processing unit (CPU/GPU), and a memory sub-system [7-11]. Packaging and interconnect technologies play a vital role in defining memory sub-system performance. As discussed in [7], traditional off-package interconnections between logic chips and memory chips cannot scale to meet the required future TB/s memory BW. Therefore, the trend is to adopt on-package interconnection between logic and memory chips. These on-package interconnections offer short electrical paths between logic and memory chips, and thus boost the memory BW and help lower the power consumption.

The logic and memory can share a package in either a 2D or 3D format. In the 2D format (Figure 1.8), the logic and memory chips are interconnected side-by-side on a shared package substrate. In this 2D format, when a traditional laminate substrate is used,

the interconnect density of the laminate limits the density between the logic and memory chips. Therefore, in this case, the memory BW is not scalable as expected. In another 2.5D case (Figure 1.9), the laminate substrate can be replaced by a silicon interposer with much higher interconnect density.

In the 3D format, as shown in Figure 1.10, either a logic chip is stacked vertically on top of a memory chip or a memory chip is stacked on top of the logic chip. The interconnection between them can be through wire bonds or TSVs. The wire bonding interconnections are limited by interconnect density due to the bond pads and wire bonding technology. On the other hand, TSVs provide the highest number of I/O and the shortest interconnection between different tiers, which potentially can boost the performance, reduce power consumption, miniaturize package size, and facilitate heterogeneous integration.

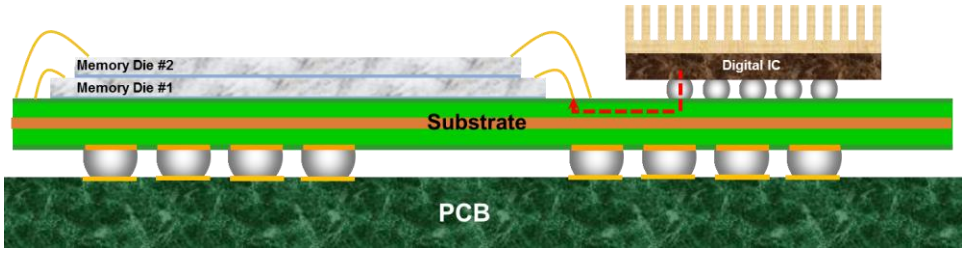


Figure 1.8: 2D package layout

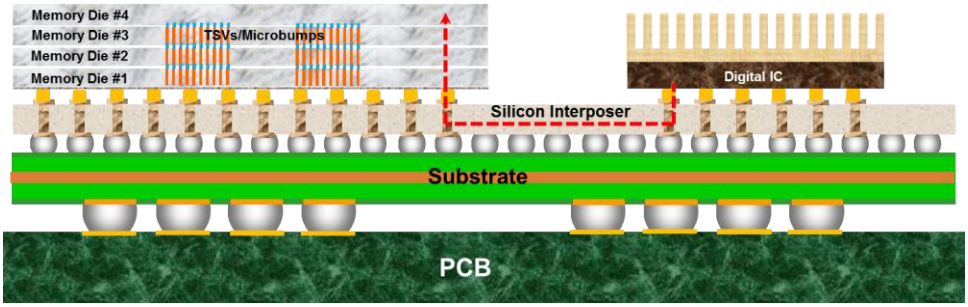


Figure 1.9: 2.5D integration with silicon interposer

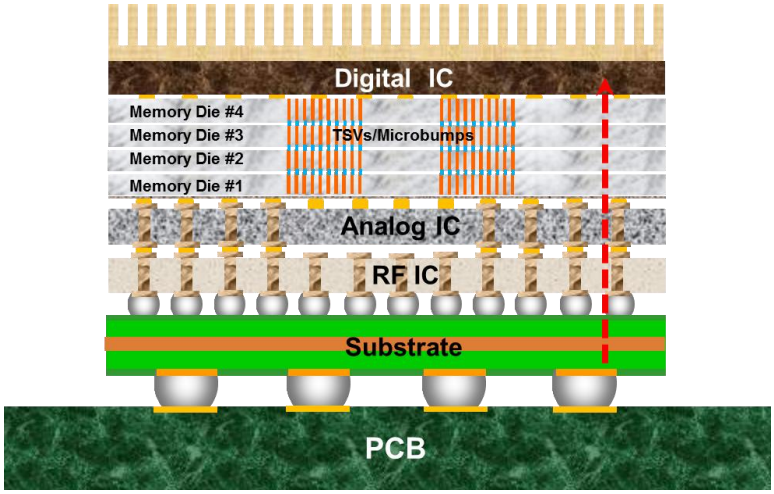


Figure 1.10: 3D integration with TSVs

1.1.2 Challenges

Although 3D integration with TSVs provides the ultimate 3D solution to meet the demands in the microelectronics industry, there are numerous challenges associate with this relative new technology, such as fabrication [4, 12-16], assembly [3, 17], test [6], thermal management [4], and reliability [3, 18]. Significant research effort [3, 5, 6, 19] has been devoted to the development and improvement of the 3D integration techniques. However, there are cost, test and manufacturability issues that still need to be solved.

Among the aforementioned challenges, reliability has attracted tremendous attention recently. As shown in Figure 1.11, due to the high mismatch in the coefficient of thermal expansion (CTE) between the silicon substrate, dielectric layer and metal core, large stresses may develop. These stresses may lead to various reliability issues, such as cohesive cracking (Figure 1.12) and/or interfacial separation. Another challenge is the assembly of the 3D integrated packages. With more silicon dies or interposers stacked on top of the organic substrate (Figure 1.9 and Figure 1.10), a larger volume of silicon is present in the 3D packages compared to traditional 2D packages. The high CTE mismatch between the thick die stack and the organic substrate may induce large warpage, which can prohibit the successful assembly of the other components. Also, high CTE

mismatch plus the stiff thick die stack may lead to the failure of interconnects in the 3D packages.

In addition, after TSVs have been integrated in packages, the fabrication, and assembly induced residual stress plus the CTE mismatch due to the existence of other components complicate the TSV reliability analysis. Therefore, there is a compelling need to study TSV reliability through both experimental test and numerical analysis, and thus to develop geometry, material, and processing guidelines that will result in reliable TSV structures.

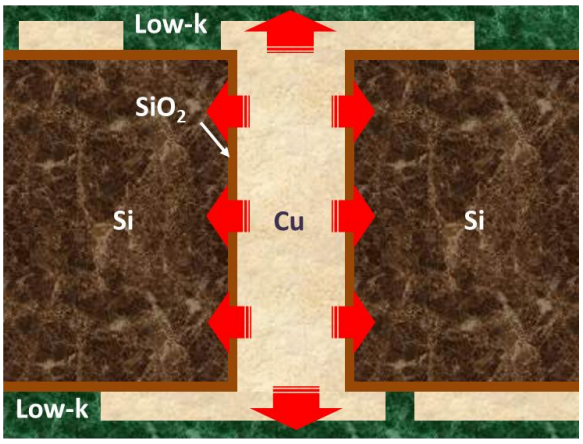


Figure 1.11: CTE mismatch induced stress in TSV structure

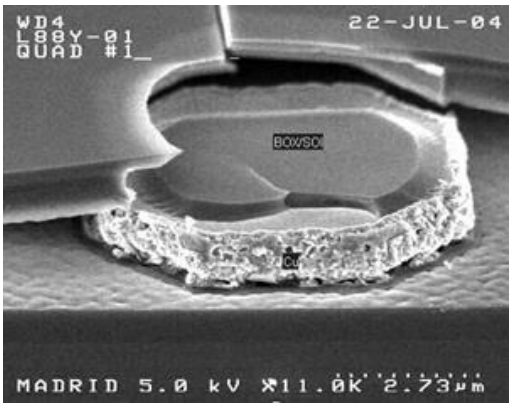


Figure 1.12: CTE mismatch induced dielectric cracking (Source: Tezzaron)

1.2 Gaps in existing research

Although 3D packages integrated with TSVs are being pursued aggressively by the industry, there has been a lack of thermomechanical analysis of TSVs and stacked dies. Tremendous research effort has been devoted to the development and improvement of various TSV fabrication processes [13-15, 19]. However, relatively less work has addressed the TSV thermomechanical stress and reliability issues [4, 20-24]. Available information in open literature mostly focuses on thermomechanical stress analysis of TSVs in a free-standing wafer without considering the global thermal mismatch and loading from other components in a 3D integrated package.

Various experimental techniques have been applied to study TSV reliability, including x-ray diffraction(XRD), digital image speckle correlation (DISC), piezo stress sensor, and bending beam measurements for TSV micro-stress measurement technique [25-28]; atomic force microscopy (AFM), and scanning electron microscope (SEM) for Cu pumping study [29, 30]; thermal cycling for fatigue life assessment [30, 31]. However, limited experimental failure analysis data has been reported in the literature.

As mentioned above, prior efforts in TSV stress/strain measurements for understanding these reliability challenges include micro-Raman spectroscopy, bending beam technique, indentation, and x-ray micro-diffraction. Micro-Raman spectroscopy works on the principle of measuring the frequency shift of an impinging laser to quantify localized near-surface silicon stress [21, 32]. However stresses in copper cannot be measured using micro-Raman spectroscopy. The bending beam technique works on the principle of measuring the curvature of the sample to quantify the stress in silicon and copper [33]. However the measured stresses using the bending beam technique are averaged across the sample. Indentation techniques work on the principle of analyzing the residual-stress-induced normal load to measure localized stress in silicon and copper [34]. However, it is difficult to measure residual stress in the absence of a known stress-

free state using the indentation techniques. Synchrotron x-ray diffraction (XRD) can measure all the stress components in a copper via and the surrounding silicon [26]. However, data interpretation is challenging for thick structures. Depth resolved x-ray diffraction techniques such as DAXM (Differential Aperture X-ray Microscopy) could in principle be employed but data collection would be prohibitively long to map an entire sample [35]. Raster scanning the sample under a micro focused beam provides a 2D strain distribution map of the sample, whereas the strain distributions in TSVs are 3D in nature. How the strain distribution along the x-ray penetration depth direction is averaged and projected is a complicated matter as it involves multiple factors such as x-ray energy, type of materials, as well as dynamical effects. This may not be an issue for thin structures [36, 37], however it is essential for the interpretation of measurement results of thick samples like a silicon wafer with embedded copper TSVs.

Also, comparatively there is a limited body of work [17, 38-43] that focuses on the chip warpage issue during assembly and its effect on package reliability. One reason is that 3D stacked dies interconnected with TSVs are still under development stage. Chip warpage has not caught enough attention and limited prototype samples are available for warpage studies. Another reason is that numerical simulation of 3D package is computationally expensive. In 3D packages, the in-plane dimensions are on the mm-scale. However, the out-of-plane dimensions, TSVs, and microbumps are on the μm-scale, which results in a tremendously increased finite-element mesh density in order to meet the finite-element element aspect ratio requirements. Moreover, there are usually hundreds or thousands of TSVs/Microbumps in each layer. It remains a challenge to economically and effectively study this 3D package warpage problem.

1.3 Objective and approach

The objective of this work is to experimentally test and numerically analyze TSV structures in a systematical manner to gain fundamental understanding into TSV reliability in free-standing wafers as well as in 3D integrated packages.

In this work, TSVs in free-standing wafers will be fabricated in the cleanroom in cooperation with other research groups. Different fabrication processes and parameters will be applied to improve the yield and sample quality.

Various experimental techniques will be applied to characterize the fabricated TSVs to provide initial assessment on TSV sample quality, which is essential for the subsequent failure testing.

Thermal shock testing on TSV samples with daisy chains will be conducted. Failure analysis will be carried out. A numerical fracture model will be developed to understanding the reason behind different failure mechanisms.

In-situ micro-strain in fabricated TSV structures will be measured by using synchrotron XRD. A data interpretation method based on beam intensity averaging will be proposed to understand this 3D to 2D strain measurement data projection process. Full field strain distributions in different TSV samples are going to be obtained to provide fundamental understanding of TSV thermomechanical reliability.

An analytical model will be formulated to analyze the warpage issue of 3D packages with TSVs. In addition, simplified numerical models will be developed for the warpage study.

Numerical models calibrated by experimental warpage measurement will be built to analyze TSV reliability in 3D integrated packages as well as in free-standing wafers. Design of Simulation (DOS) will be implemented to identify critical design parameters and for the development of TSV and package design guidelines.

1.4 Thesis outline

This thesis is organized as follows:

CHAPTER 1 briefly introduces the background and motivation for this work. The gaps and challenges of exiting research and the scope of this work are also discussed

CHAPTER 2 presents the process of TSV fabrication on free-standing wafers. Fabricated TSV samples are characterized with various experimental techniques. Numerical simulations are carried out to study TSV thermomechanical behavior under temperature excursions and the effect of different TSV designs. Also, fabrication induced defects on TSV thermomechanical reliability are analyzed.

CHAPTER 3 shows the work of a thermal shock test on fabricated TSV samples. Failure analysis is conducted on the test samples to identify various failure mechanisms under temperature excursions. For numerical fracture analysis, a centered finite-difference approach (CFDA) based on Griffith's energy balance has been proposed to calculate the energy release rate. Fracture analysis explains the fundamental cause of different failure mechanisms.

In CHAPTER 4, local strain fields under thermal excursions are studied by using synchrotron X-ray diffraction. To understand this 3D to 2D strain measurement data projection process, a data interpretation method based on beam intensity averaging is proposed and validated with measurements. Another indirect comparison methodology based the aforementioned data interpretation method has also been proposed to study the thermomechanical strain field of several TSV designs.

CHAPTER 5 proposes an analytical approach to study the warpage issue of 3D packages interconnected with TSVs. Numerical models are also developed for the warpage study.

CHAPTER 6 focuses on 3D package thermomechanical reliability. Critical locations have been identified. Design of simulation (DOS) is applied for the parametric study. Design guideline for both TSV and 3D packages has been developed.

CHAPTER 7 summarizes the findings from this work and provides an outline of potential future work.

CHAPTER 2

TSV FABRICATION INDUCED DEFECTS AND STRESS ANALYSIS

As discussed in CHAPTER 1, CTE mismatch induced stress in TSV structures can potentially cause various reliability issues. To experimentally study TSV thermomechanical reliability, TSV samples with daisy chains have been fabricated[1]. Finite element models have been built to analyze the stress/strain distribution in the TSV structures. Based on the models, different via designs, such as circular, square, and annular vias have been analyzed and compared to be able to design current and future TSVs with optimum thermomechanical performance. In addition, defects due to fabrication such as voids in the Cu core during electroplating have been considered in the models to assess their effect on TSV reliability under thermal loading.

2.1 TSV sample fabrication

TSVs were fabricated on 4-inch silicon wafers according to the full process flow shown in Figure 2.1. After cleaning the wafer, lithography was performed to pattern the TSV structures using Dow Chemical SPR™ 220 positive acting photoresist and Karl Suss MA6 Mask Aligner located in the cleanroom. The average thickness of the photoresist was 7.5 μm. After a 35 minute bake dry and exposure, the photoresist was developed by using MF®-319 developer.

After lithography process, the sample wafer was attached to a handle wafer and then put into the STS-ICP machine for blind via etching using Bosch Process. In the process of blind via etching the larger features have faster etching speed and vias with similar dimensions have similar etching speed. After blind via etching, back grinding and

[1] By collaboration with Package Research Center at Georgia Institute of Technology

final polish was used to expose the backside of the vias to form through vias. In order to open the 40 µm diameter alignment vias on the back side, the wafer was thinned down to ~260 µm.

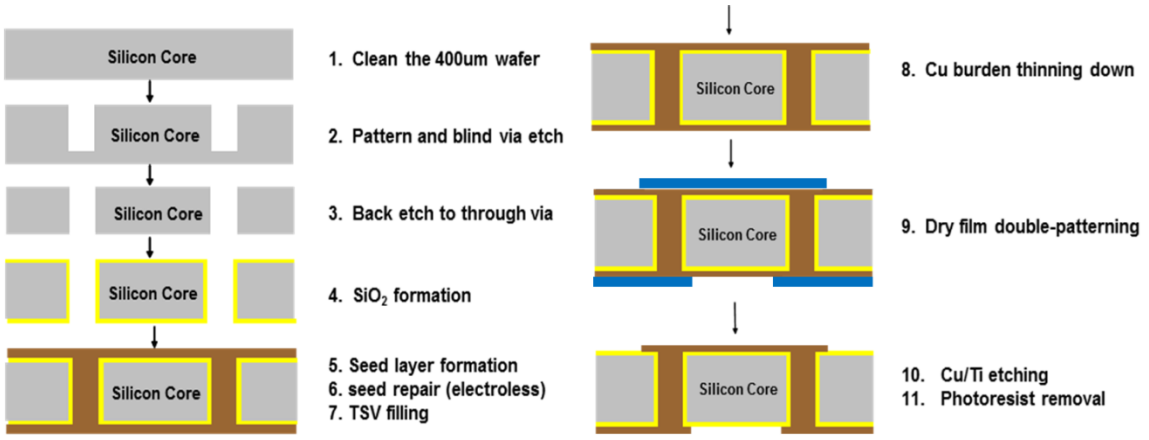
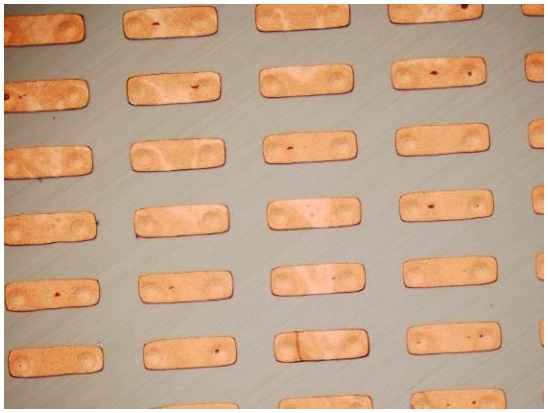


Figure 2.1: Process flow for TSV fabrication

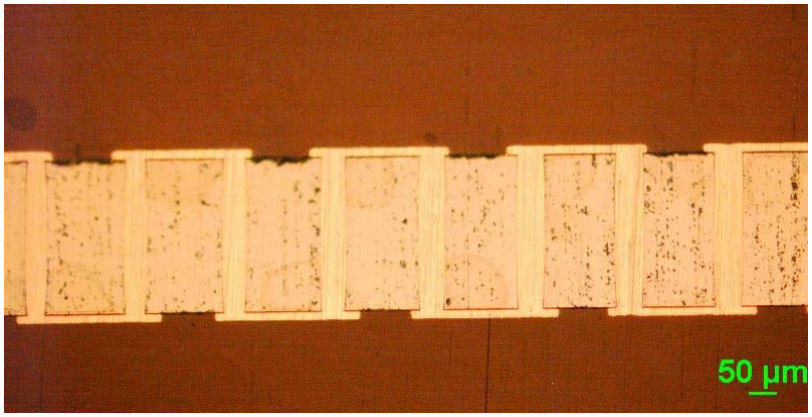
After removing the residual photoresist by using Acetone, a 2 µm thick SiO_2 dielectric isolation layer was deposited by plasma enhanced chemical vapor deposition (PECVD) process at 250 ℃ on both sides of the wafer using a Plasma-Therm PECVD or STS-PECVD tool. A 30 nm Ti (barrier for Cu diffusion into SiO_2) and 1 µm thick copper seed layer were grown on both sides of the sample wafer by using CVC DC Sputter to provide the electrical contact for the electroplating process. The sequence of barrier and seed layer sputter deposition for the through vias was Ti/Cu sputter on one side of the wafer, followed by flipping the wafer and Ti/Cu sputtering on the other side to get complete coverage on the through via. For high aspect ratio vias, Cu electroless plating process was used to deposit a thin layer of Cu to ensure complete coverage of the metal seed and fix any spots on the via side wall where the sputtered seed layer was not able to reach. A DC electroplating process was then used to plate copper and fill the TSVs. The holding time between seed repair and electroplating was minimized in order to avoid oxidation of Cu and a 10% sulfuric acid clean was performed for 1-2 minutes just before

the electroplating step. A current of 4 ampere was used for 8 hours in this process. The final thickness of the Cu burden on both sides was around 80 µm, which was then thinned down during the Cu pad formation process.

The Cu pad formation process starts with thinning of the Cu burden by double sided micro-etch process using a dilute $CuCl_2$ solution. The target finished Cu thickness was 12-15 µm. After thinning the Cu burden, a double-sided lithography process was done using dry film photoresist applied to the thin wafer by vacuum lamination. The UV exposure was done with precise alignment using a mask aligner, followed by spray developing using a 1% sodium carbonate solution. The patterned photoresist mask was used to etch back the Cu by wet etching ($CuCl_2$ chemistry), followed by Ti seed removal using wet or dry etching. The final step in the process sequence was stripping of the photoresist using a potassium hydroxide solution to result in Cu pad structures. Figure 2.2 shows the top view and micro-section images of a representative TSV daisy chain with 65 µm diameter vias. The defined copper pads for the through vias can be seen on both sides of the wafer with a thickness of 260 µm.



(a) Top view



(b) Cross-sectional view

Figure 2.2: Top view and cross-sectional view fabricated TSVs with daisy chains

2.2 TSV sample characterization

Various experimental techniques, such as stress measurement with XRD, resistance measurement with four point probes, non-destructive 3D x-ray imaging, and SEM imaging on cross-sectioned samples, have been applied to characterize the fabricated TSV samples, which provides input for the followed finite element modeling analysis.

2.2.1 Stress measurements using XRD

Large arrays of filled TSVs were subjected to XRD analysis using Cu-Kα as the characteristic XRD source, at different temperatures ranging from 25 ℃ to 425 ℃ in steps of 25 ℃. The analysis was also done in the reverse direction with the temperature going from 425 ℃ to 25 ℃ in steps of -25 ℃. The temperature change leads to strain and stress in the TSV structure. In the X-Ray stress measurement, the strain is detected by a shift in the 2θ peak at the different temperatures of measurement. A monotonic peak shift downwards with increasing temperature was detected for each Cu peak of the XRD spectra. An example of this is shown as Figure 2.3 for the 2θ=89.933°, which

corresponds to the Cu (311) texture. From the measured 2θ change at different temperatures, we can use the following equation to determine the stress in the TSV.

$$\sigma = \frac{E \cot\theta \Delta 2\theta}{2\nu} \times \frac{\pi}{180}$$

where,

σ: Stress

E: Young's modulus

υ: Poisson ratio

Figure 2.4 shows the stress calculated in the TSVs at different temperatures, where the 2θ peak shift is determined relative to the Powder Diffraction File (PDF) for Cu. The 2θ angle for the sample tested in 50 ℃ is nearly the same as the angle of the powder diffraction file and is therefore assumed to be the zero-stress condition. It can be seen that plastic deformation of Cu is occurring at temperatures as low as 100 ℃.

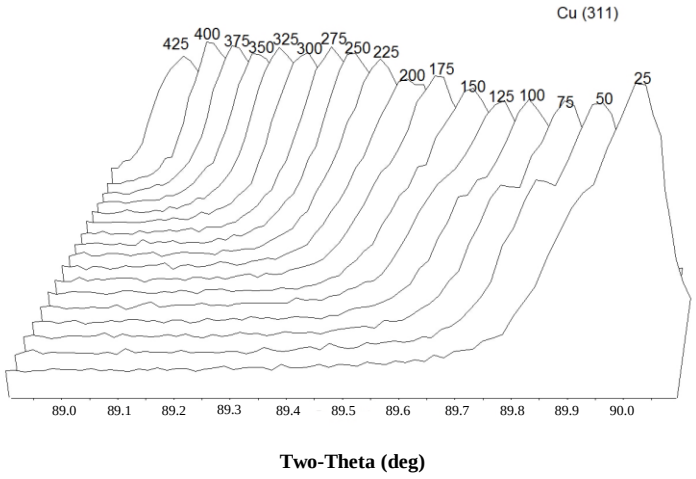


Figure 2.3: XRD pattern (near 2θ=89.933°) for Cu at different temperatures

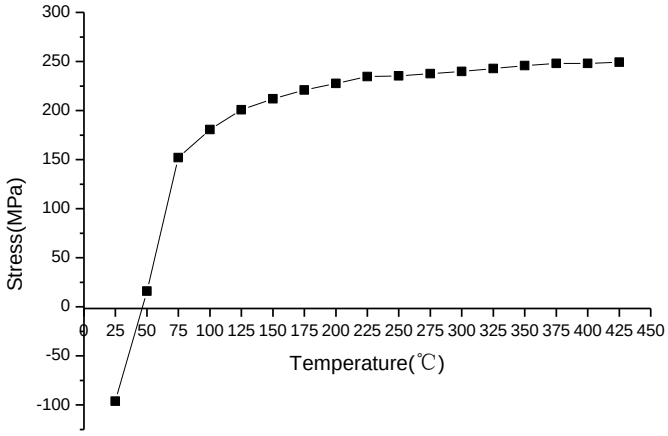


Figure 2.4: Stress in TSVs at different temperatures

This XRD method does not provide a spatial distribution of the stresses on the wafer. It is instead an average measurement of the stresses near the top of the TSV structure. Thus, the stresses determined by this method were used for stress free temperature determination for finite element models.

2.2.2 3D X-ray characterization

Dage X-Ray XD7600NT™ was used before the thermal cycling to analyze the inner structure of the filled via. Voids were observed inside filled copper on some coupons, as shown in Figure 2.5. This defect could be due to the high current density used during the plating process for through vias with such high aspect ratio. For this particular report, we focused on the structure that has voids in the vias since we want to study the effect of voids on the reliability. Theoretical calculation for a chain of 3364 vias predicted a resistance of 4.6 ohms (resistivity 1.7 μΩ.cm [44, 45]), while a four-point probe measurement (Figure 2.6) gave a value of 9 ohms for the same group of vias on the real sample. The existence of voids could be the reason for higher measured initial resistance compared to the theoretical estimate.

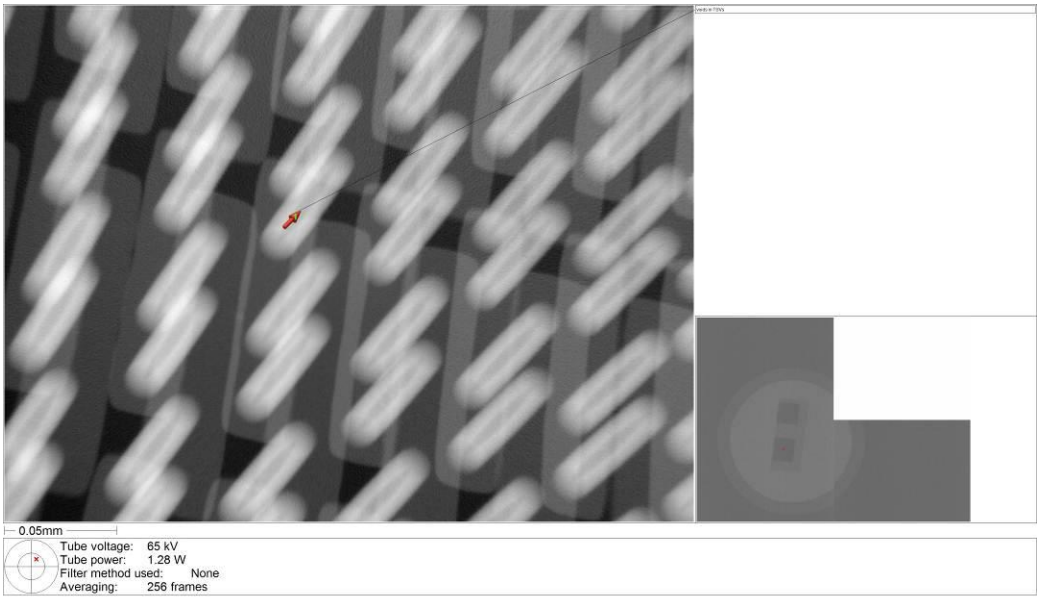


Figure 2.5: Fabrication induced voids in Cu vias

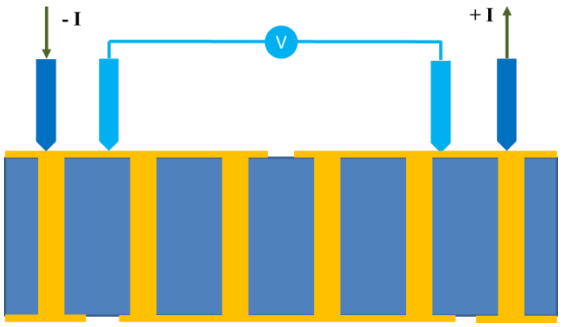


Figure 2.6: Schematic Cross section of studied TSV design and resistance measurement

2.2.3 Cross-sectioning and SEM imaging

To protect the sample and to avoid any artificial cracking during sample handling and cross-sectioning, TSV samples were molded with epoxy first. Then, the molded samples were fine polished to expose the TSVs. As shown in Figure 2.7, daisy-chain loops covered four TSVs, two in parallel, as shown in the cross-section. As seen, the TSVs have no separation or delamination or cracking. The only visible defect is the

presence of voids at the center of some of the TSVs after electroplating, which can also be seen in Figure 2.5.

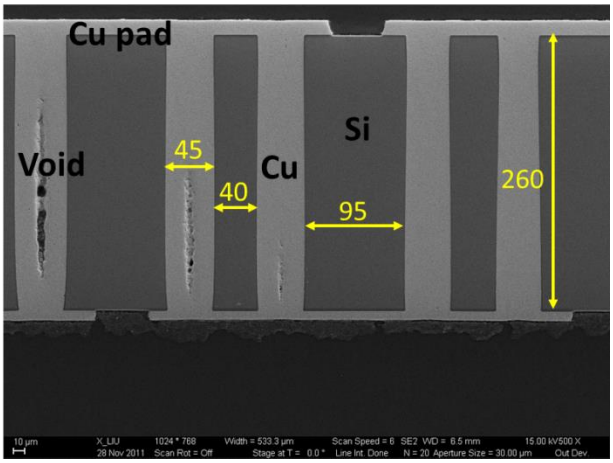


Figure 2.7: Cross-section of as-fabricated TSVs with daisy chain (units: μm).

2.3 Numerical analysis

Two-dimensional axisymmetric model, reported in our paper [22], are limited in scope. In order to compare different via geometries such as circular, annular, and square and also to study fabrication induced defects, comprehensive 3-D models are needed. Such circular, annular and square vias were modeled using finite elements, as shown in Figure 2.8 to Figure 2.11. In these models, one quarter of the top view of the via was modeled. Also, only the upper half of the via was modeled, and thus, each via model was $1/8^{th}$ of the actual via structure. As the vias are periodic in a large array, the top planar view of the models was a square with each side being half the via pitch. In the models, symmetry boundary conditions were applied on the two inner surfaces of the models, while coupled boundary conditions were applied on the two outer surfaces of the via square cell to mimic the periodic layout. In these models, TSVs were completely filled with copper. The thickness of Si wafers was 300 μm and the thickness of the dielectric layer was 2 μm. Other dimensions and materials of circular, annular, and square vias are listed in Table 2.1 to Table 2.5. The assumptions made in these models are as follows:

1. The thin barrier Ti layer was neglected in the models.
2. All materials were assumed to be isotropic.
3. Si and SiO_2 were assumed to be thermo-elastic.
4. The stress-free temperature for the TSV structure was taken to be 50 ℃ to mimic typical plating temperature as well as XRD measurements, reported in Section 2.2.1.
5. Perfect bonding was assumed at the interfaces.

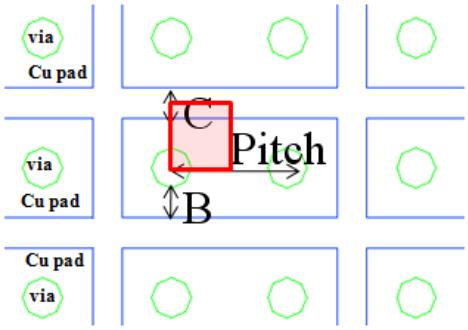


Figure 2.8: TSV sample design (top view)

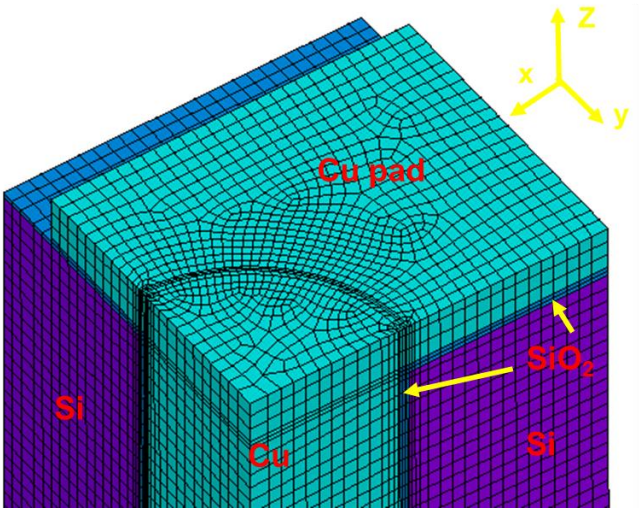


Figure 2.9: 3D finite-element mesh of a circular via

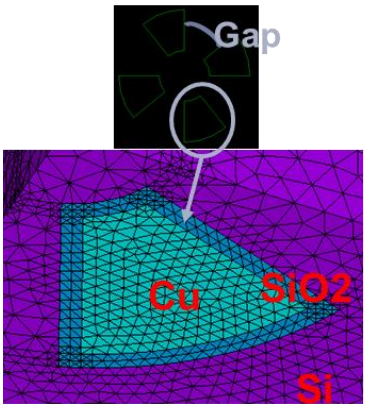


Figure 2.10: 3D finite-element mesh of an annular via (bottom view)

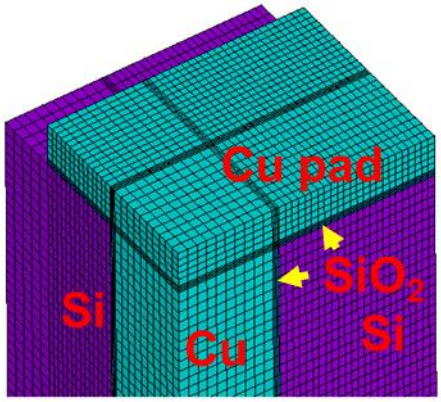


Figure 2.11: 3D finite-element mesh of a square via

Table 2.1: Circular vias

	Diameter	B	C	Pitch
Circular	65 µm	30 µm	30 µm	155 µm

Table 2.2: Annular vias

	Inner diameter	Outer diameter	Gap	B	C	Pitch
Annular	25 µm	65 µm	20 µm	30 µm	30 µm	155µm

Table 2.3: Square vias

	Side	B	C	Pitch
Square	57 µm	30 µm	38 µm	155 µm

Table 2.4: Material properties [46]

	Cu	SiO_2	Si
Young's Modulus (GPa)	Table 2.5	71.4	131.00
Poison ratio	0.3	0.16	0.28
CTE (ppm/ ℃)	17.3	0.5	2.6

Table 2.5: Material properties of Cu [47]

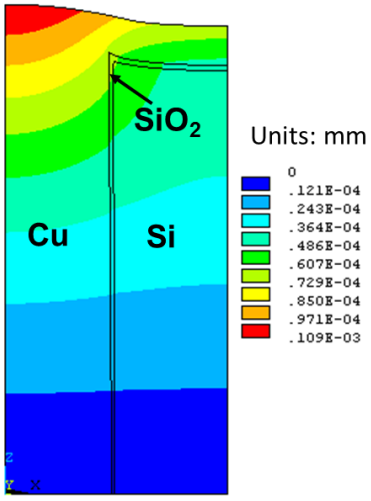
Temperature (℃)	27	38	95
Young's Modulus (GPa)	121.00	120.48	117.88
Temperature (℃)	149	204	260
Young's Modulus (GPa)	115.24	112.64	110.00
Temperature (℃)	27		
Plastic Curve - stress (MPa) vs. strain	121@ 0.001ε 186@ 0.004ε 217@ 0.01ε 234@ 0.02ε 248@ 0.04ε		

2.3.4 Cu pumping and Cu sinking in circular vias

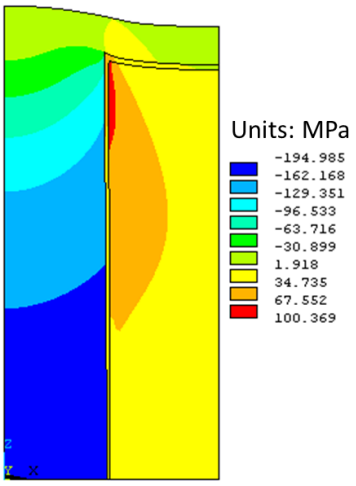
Thermomechanical analysis of circular via was carried out by starting with a stress-free temperature of 50 ℃. The structures were simulated to be heated to 125 ℃ and then cooled to -40 ℃. The distributions of the axial displacement, stress as well as plastic strain of the vias are shown in Figure 2.12 and Figure 2.13. As shown in Figure 2.12 (a) and (b), at 125 ℃, because the CTE of Cu is about 5 times that of Si, Cu tends to expand more than the surrounding Si. This higher CTE of Cu results in two axial phenomena: 1) Cu "pumps" out of the TSV, as illustrated in Figure 2.12 (a). Such Cu pumping could lead to failure of other layers deposited on top. 2) Compressive axial stresses develop near the center of the TSV due to the presence of lower CTE silicon surrounding the copper core (Figure 2.12 (b)). This CTE mismatch also results very high shear stress and 1st principal stress in the dielectric layer near via top edge (Figure 2.12 (c)(d)), which may cause interfacial debonding and/or crack the dielectric layer. In summary, under heating, cohesive cracking of SiO_2, interfacial cracking of Cu/SiO_2

interface, and top layer delamination due to copper pumping are some of the reliability concerns that need additional attention. The plot of equivalent plastic strain (Figure 2.12 (e)) indicates that Cu yielding is limited and occurs near the Cu pad corner. The critical stress locations, the stress contours, and the stress magnitude in the current 3D model are comparable to the results obtained in the 2D model, and the TSV stress distribution under heating has been compared against experimental XRD data in our previous publication [22].

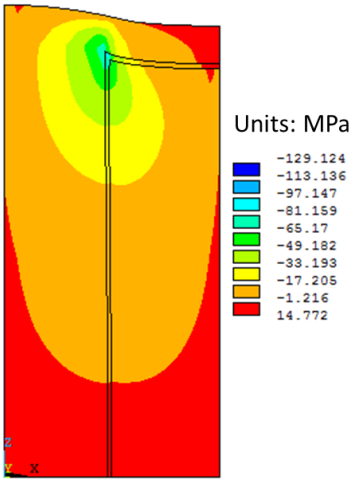
Upon cooling to -40 ℃, the displacement and stress directions are reversed. At -40 ℃, as shown in Figure 2.13, Cu tends to sink into the Si hole. At the same time, Cu experiences significant amount of tensile stress in the axial direction due to the presence of lower CTE Si/SiO_2 materials surrounding the copper core. Also, large stress gradient exists at the Cu/SiO_2 interface, especially near the Cu pad inner corner. Furthermore, tensile peel stresses develop in the radial direction. Therefore, when TSVs are thermal cycled, debonding of Cu/SiO_2 interface is of concern.



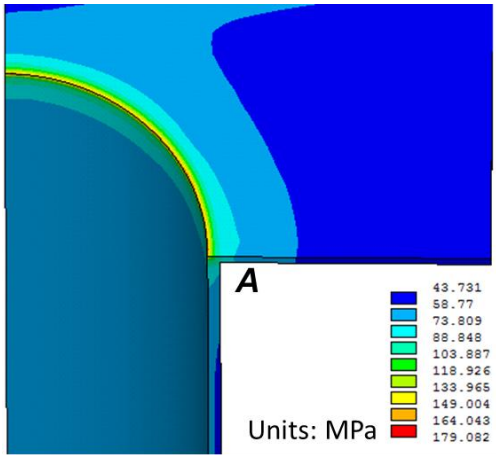
(a) Axial displacement U_y(Cu pumping)



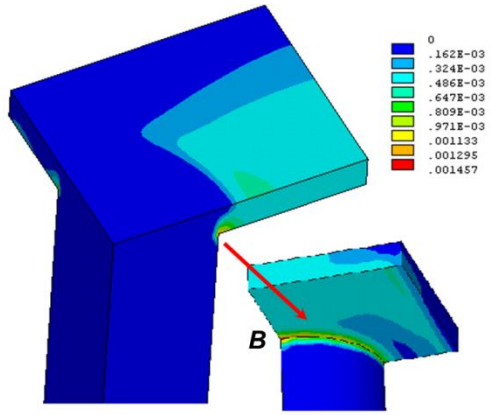
(b) Axial stress σ_y



(c) Shear stress σ_{xy}

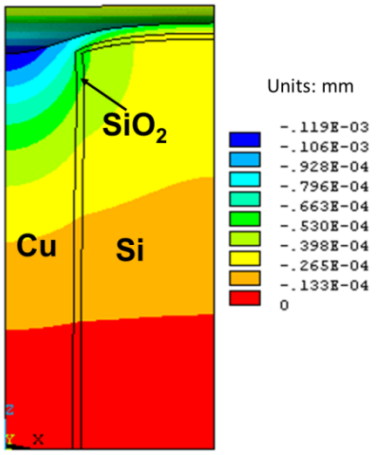


(d) 1st principal stress in dielectric layer

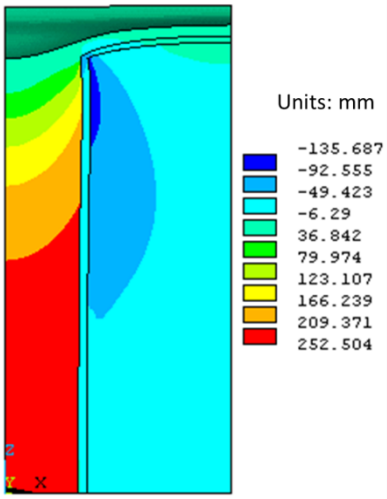


(e) Equivalent plastic strain in Cu

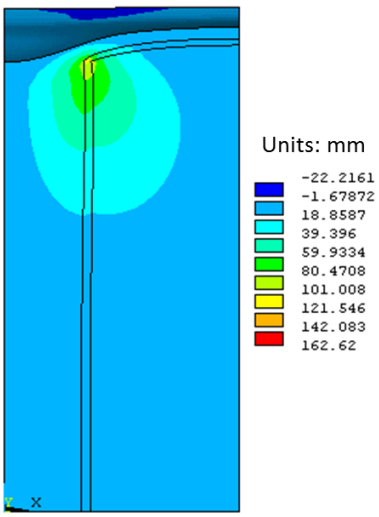
Figure 2.12: Thermomechanical analysis of a circular via at 125 ℃



(a) Axial displacement (Cu sinking)



(b) Axial stress



(c) Shear stress σ_{xy}

Figure 2.13: Thermomechanical analysis of a circular via at -40 ℃

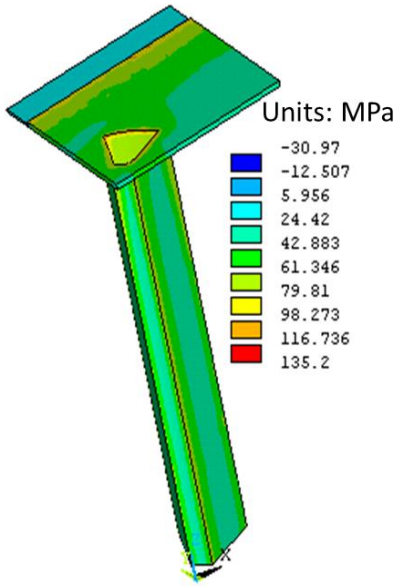
2.3.5 Comparative study of circular, annular and square vias

To compare the annular via and the square via with the circular via, an annular via with the same outer diameter as the circular via and a 57 μm×57 μm square via, which has roughly the same Cu volume as that of the circular via were built and analyzed at 125 ℃.

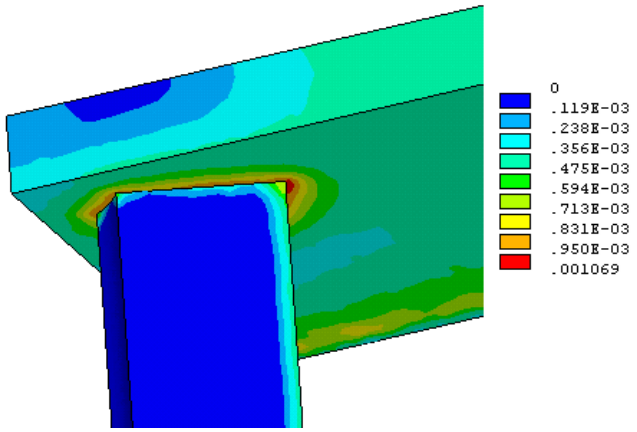
As Figure 2.14 and Figure 2.15 show, the stress distribution in the annular via and the square via is similar to that of the circular via, having the same critical locations near the via top corners and Cu pad outer edges. However, the magnitudes of the 1st principal stress in the dielectric layer and equivalent plastic strain in copper are higher, especially near the sharp corners of square via, as would be expected. Unless there are compelling reasons, square via is unlikely be adopted in future TSV design.

Figure 2.16 provides a comparison of the three via geometries. As seen, the annular via has the minimum stress in the dielectric among the three designs, because it has less Cu than the circular and square vias. Also, the plastic strain in Cu for the annular case is less than the plastic strain in Cu for the circular and square vias. Based on these

observations alone, it can be said that the annular vias are likely to be more thermo-mechanically reliable. However, one needs to take into consideration the fabrication as well as the electrical issues before selecting an appropriate via geometry.

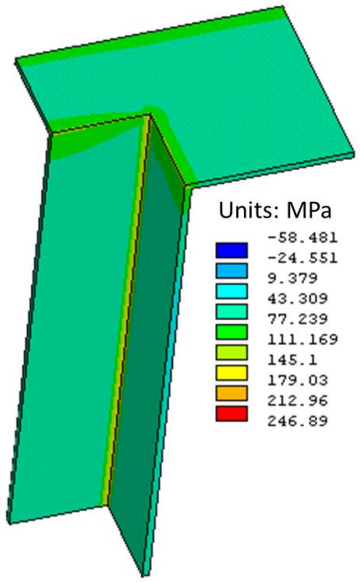


(a) 1st principal stress in dielectric layer

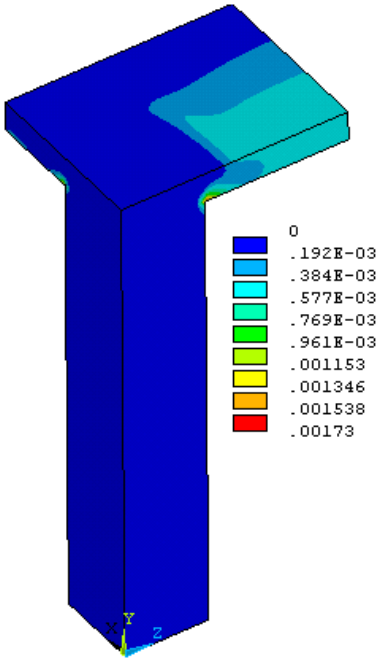


(b) Equivalent plastic strain in Cu

Figure 2.14: Thermomechanical analysis of an annular via at 125 ℃

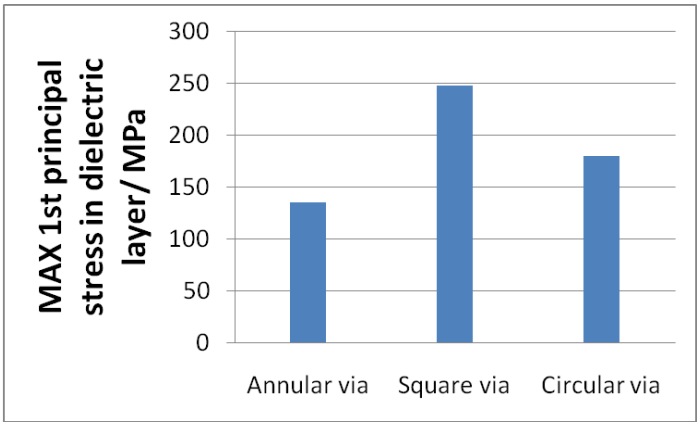


(a) 1st principal stress in dielectric layer, MPa

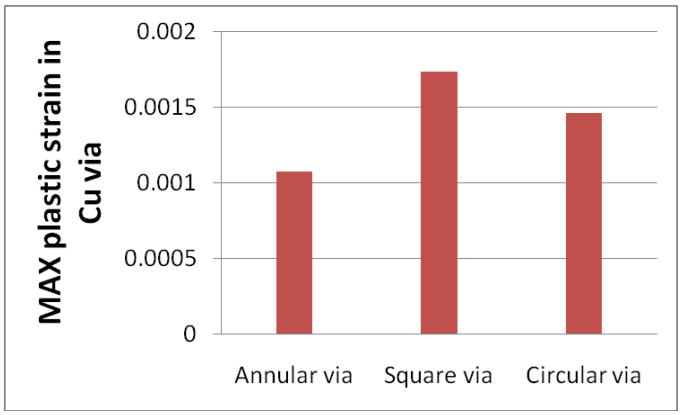


(b) Equivalent plastic strain in Cu

Figure 2.15: Thermomechanical analysis of a square via at 125 ℃



(a) 1st principal stress in dielectric layers



(b) Equivalent plastic strain in Cu

Figure 2.16: Comparison study of annular, square and circular vias at 125 ℃

2.3.6 Parametric study

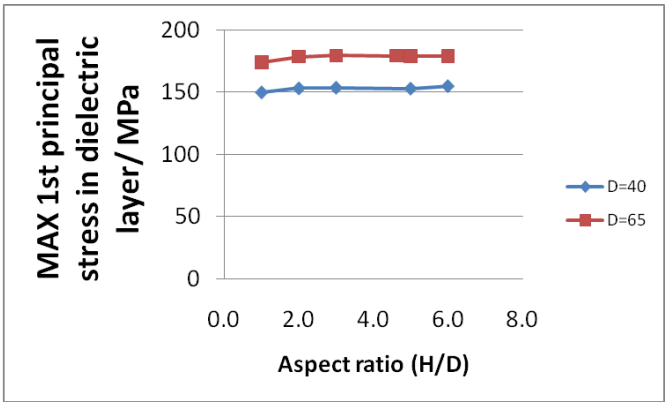
In our earlier work [22], we have studied the Cu/dielectric layer interfacial cracking as well as dielectric cracking using fracture mechanics. We have also examined the effect of some of the geometry parameters on the energy release rate available for crack propagation. In this section, we will examine the stresses in the dielectric layer without using the fracture mechanics approach. We will use the dielectric stress magnitude to study the effect of via dimensions. In addition to dielectric stress, we will also study the plastic strain in copper. Since circular vias are more widely used in industry, the rest of this chapter will focus on circular vias only.

As illustrated in Figure 2.12 (d), the dielectric stress at the dielectric/copper interface (location ***A***) near the edge is of concern, and as seen in Figure 2.12 (e), the copper strain in the copper via and pad corner (location ***B***) is of concern. Thus, the effect of various via dimensions on these dielectric stress (location ***A***) and copper strain (location ***B***) have been discussed in this section. To analyze the effect of aspect ratio (***H/D***) and via diameter, both the wafer thickness and the via diameter were changed, as listed in Table 2.6. The via pitch was kept as constant. As Figure 2.17 shows, for a given aspect ratio, both the dielectric stress and Cu plastic strain increase with the via diameter. This is because as the via diameter increases for a given TSV pitch, Cu volume percentage increases in a square cell, and thus greater stresses develop in the surrounding dielectric layer.

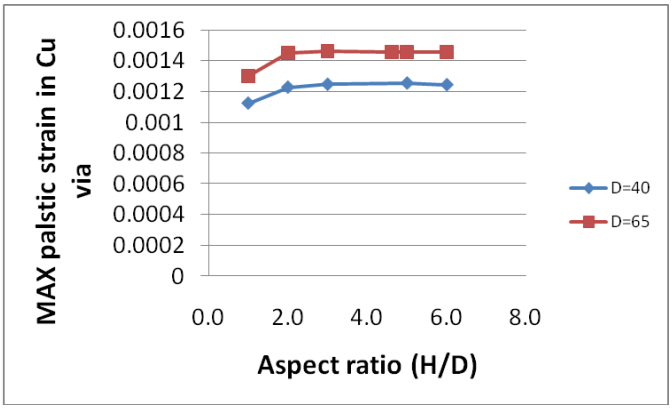
For vias with the same diameter, stresses increase with higher aspect ratio. However, stresses demonstrate a plateauing effect with the aspect ratio. This can be explained through free-edge effect. Free-edge effects are present through a depth of about one to two TSV diameters, and thus, as the aspect ratio increases, the edge effect tapers off.

Table 2.6: Modeling matrix

	Aspect ratio (*H/D*) study
Via pitch	155 µm
Aspect ratio	1,2,3,5,6 for D=40 and 65 µm



(a) Dielectric stress vs. aspect ratio



(b) Equivalent plastic strain vs. aspect ratio

Figure 2.17: Effect of aspect ratio (*H/D*) on the thermomechanical behavior of a circular via (at 125 ℃)

2.3.7 Effect of fabrication induced defects

The above analyses are based on the assumption that the TSVs are perfectly fabricated without any initial interfacial debonding or voids in Cu core. However, in actual fabrication, process-induced defects are common, and therefore, in the following sections, the effect of such defects on TSV reliability is discussed.

Although Cu electroplating is a well-established process used for TSV filling, void-free filling is still a challenge, especially for fast filling and high aspect ratio TSV filling (Figure 2.18) [13]. To analyze how those voids will affect the TSVs reliability, randomly generated voids were created within the Cu core (Figure 2.19) of circular vias given in Table 2.1. In this analysis, all the voids were assumed to be spherical with 3 μm radius.

Figure 2.19 shows equivalent stress distribution with 20% void volume in Cu, while Figure 2.20 shows the equivalent plastic strain in Cu. Comparison of Figure 2.20 and Figure 2.12 (e) shows that the introduction of voids results in higher maximum plastic strain in the Cu core. Moreover, the location of maximum plastic strain switches

from the Cu pad inner corner to near the voids. This indicates that copper cracking may initiate from those highly stressed voids.

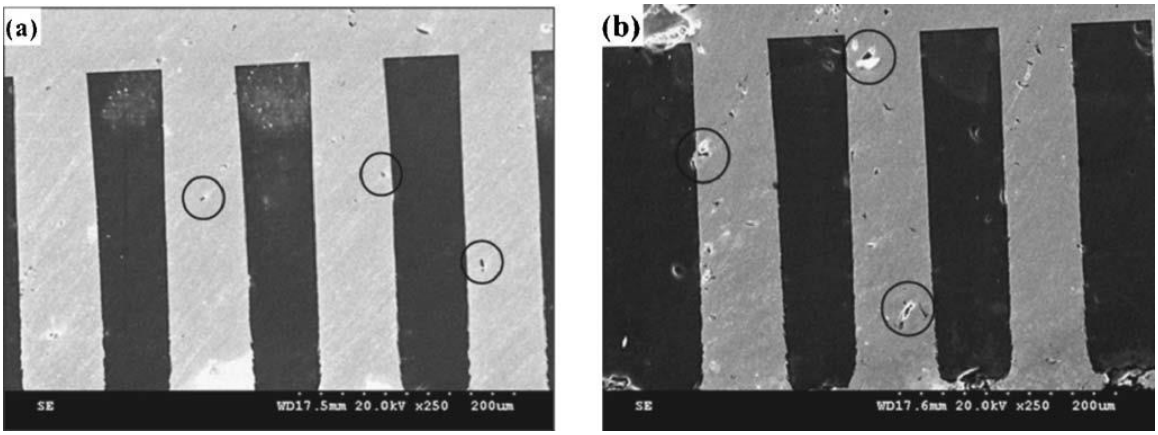


Figure 2.18: Cross-sectional image of 60-μm-diameter electroplated through holes in 300-μm-thick silicon wafer by continuous power supply at different current densities: (a) 10 and (b) 20 mA/cm^2. Voids are shown in circle (Source: Dixit [13]).

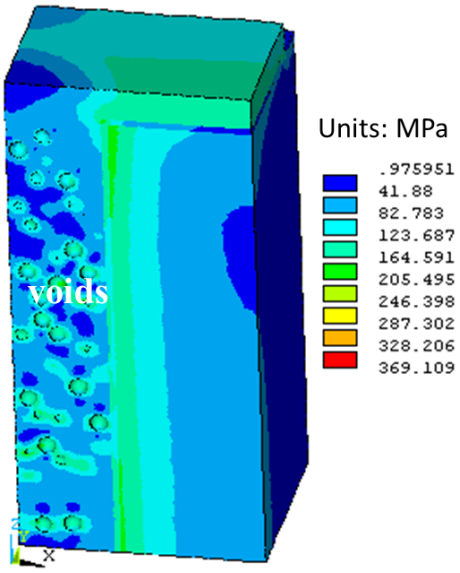


Figure 2.19: von Mises stress distribution in TSV at 125 ℃ for a circular via with 20% voids and with a void radius of 3 μm (Cross-sectional view)

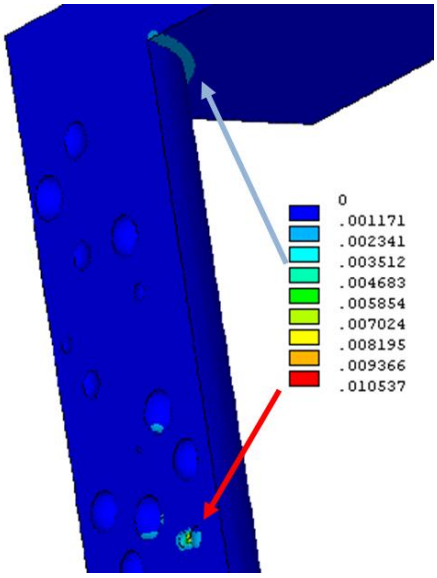
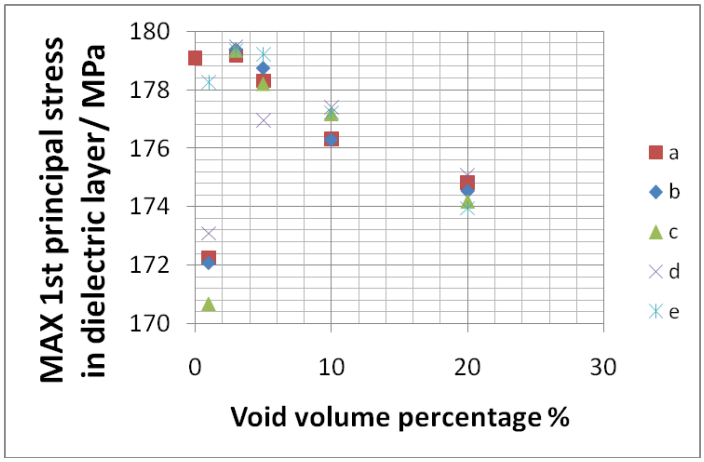


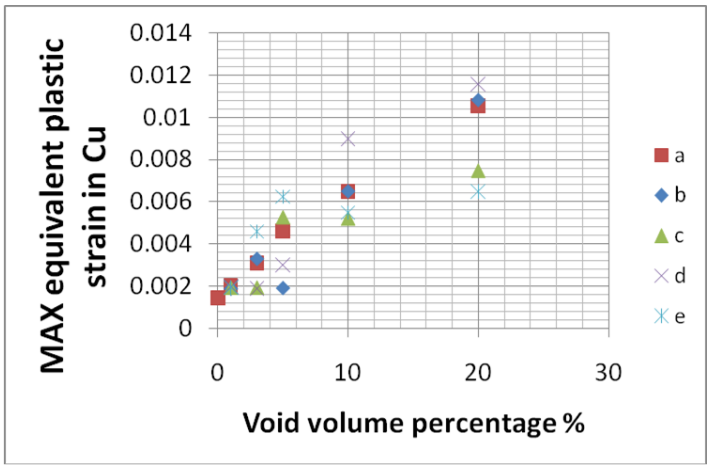
Figure 2.20: Equivalent plastic strain distribution at 125 ℃ in Cu core for a circular via with 20% voids and with a void radius of 3 μm

Effect of void volume percentage

To study the effect of void volume percentage (V_{void}/V_{Cu}), void radius was fixed at 3 μm, and the TSV was simulated to be heated to 125 ℃. Since the voids were randomly generated, five data points (a - e) were calculated for each case. As Figure 2.21 (a) shows, the existence of voids does alleviate the stress in the dielectric layer, because the existence of voids reduces the volume percentage of Cu in a unit cell. On the other hand, the equivalent plastic strain in the Cu keeps increasing with higher void percentage (Figure 2.21 (b)), and therefore, Cu cracking near the voids may occur as well as bridging of voids with crack propagation may occur.



(a) 1st principal stress vs. void percentage



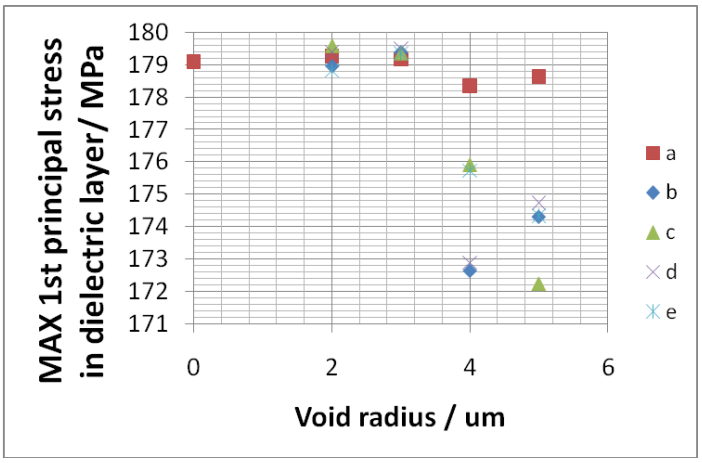
(b) Equivalent plastic strain vs. void percentage

Figure 2.21: Effect of void volume percentage with a void radius of 3 μm (at 125 ℃)

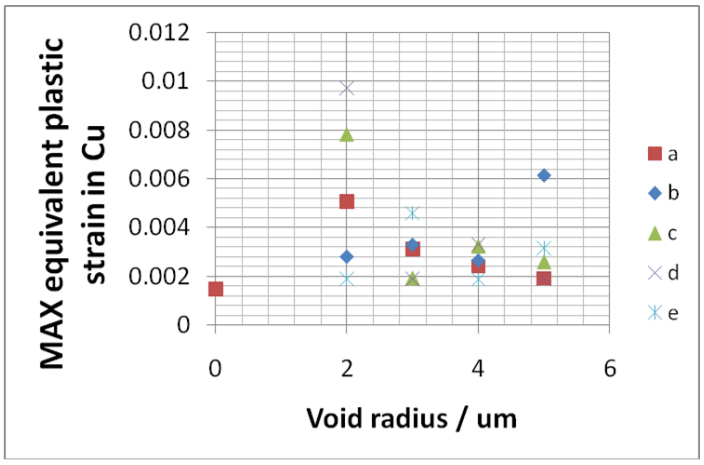
Effect of void size

Void size study was carried out by fixing the void volume percentage to be 3%, and varying the void radius from 2 μm to 5 μm. From Figure 2.22, it can be said that the presence of voids decreases the dielectric stress and increases Cu equivalent plastic strain, as discussed in previous sections. However, no clear trend can be identified based on this study. Additional simulations are needed with higher volume percentage of voids, different proximity voids to one another, and different void geometry as in fabricated

TSV structures. Only then, conclusive findings can be drawn based on void size and geometry.



(a) 1st principal stress vs. void size



(b) Equivalent plastic strain vs. void size

Figure 2.22: Effect of void size on the thermomechanical behavior of a circular via with a void volume percentage of 3% (at 125 ℃)

Effect of void location

In addition to void volume percentage and void size study, the effect of location of voids was also considered. As Figure 2.23 shows, four cases are studied: 1) Voids randomly distributed in the "Up" region; 2) Voids randomly distributed in "Center" region; 3) Voids randomly distributed in "Inner" region; and 4) Voids randomly

distributed in “Outer” region. For this study, all the voids had a radius of 3 μm and the void volume percentage was 10%.

As Figure 2.24 (a) shows, when the voids are distributed in the “Up” region, the dielectric layer has the lowest principal stress among the four cases. This is because the maximum stress in dielectric layers usually occurs near the Cu pad inner corner, which is shown in Figure 2.12 (d). The existence of voids near this region relieves the stress due to thermal mismatch between Cu and Si/SiO_2. On the other hand, when the voids are concentrated in the “Center” region, far away from the Cu pad inner corner, this stress relieving due to the existence of voids is reduced, and therefore, this case has the highest dielectric stress.

The equivalent plastic strain in Cu increases significantly compared to that of void-free case (Figure 2.24 (b)). However, the difference due to different locations is not obvious.

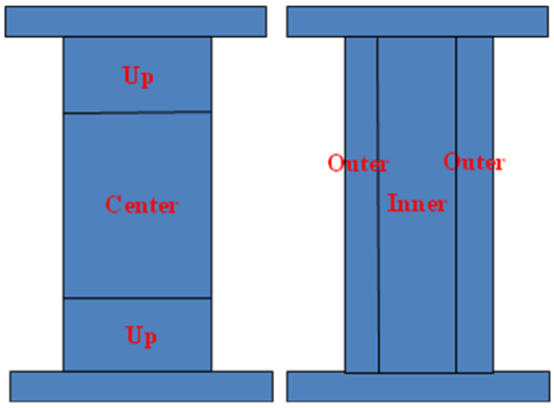
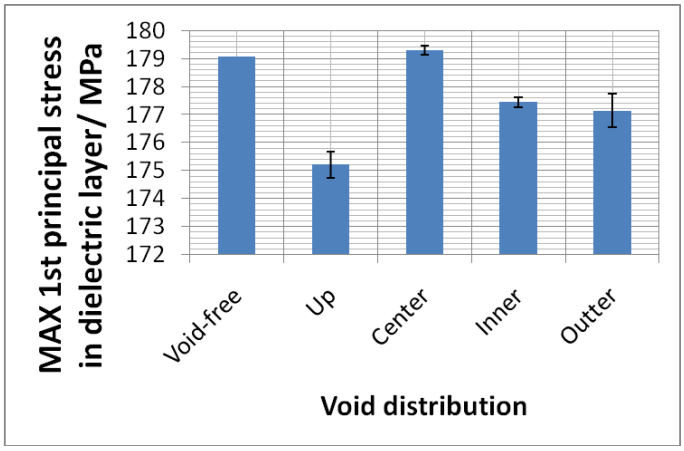
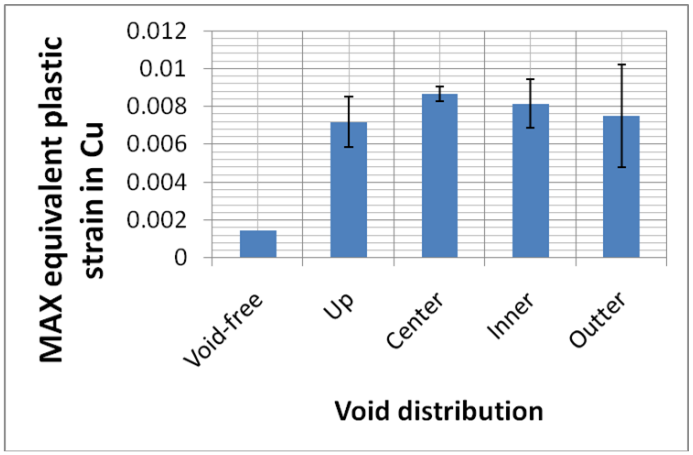


Figure 2.23: Cross-section of Cu core for void location/distribution study



(a) 1st principal stress in dielectric layer



(b) Equivalent plastic strain in Cu core

Figure 2.24: Effect of void location with a void percentage of 3% and a void radius of 3 μm (at 125 ℃)

Effect of void type

In addition to the small scattered voids, another type of large center elliptical voids in Cu vias has been observed (Figure 2.5). To study this type of void, a 40 μm-long elliptical center void was built in the circular via (Table 2.1) model. Figure 2.25 shows that the introduction of voids results in higher maximum plastic strain in the Cu core than that of the perfectly filled via in Figure 2.12 (e). Also, due to the existence of the void, less amount of Cu available for thermal expansion. Thus, smaller force was applied on surround SiO_2, as shown in Figure 2.26. However, as seen in Figure 2.27, the stress and

strain magnitude changes are small. Therefore, the 40-μm-long elliptical center void effect on TSV reliability may be limited.

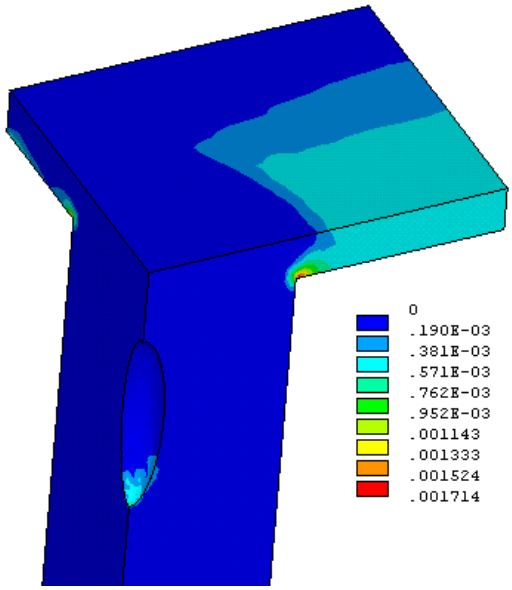


Figure 2.25: Equivalent plastic strain distribution at 125 ℃ in Cu core for a circular via with a 40-μm-long elliptical center void

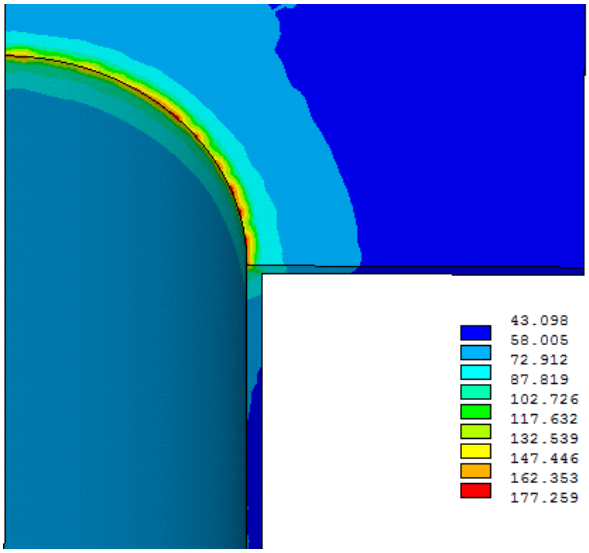
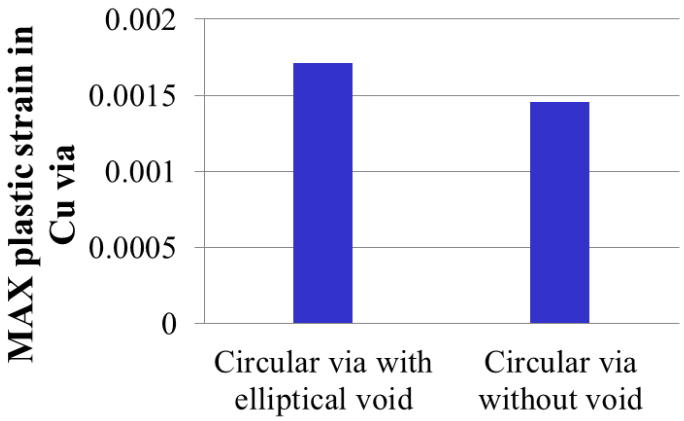
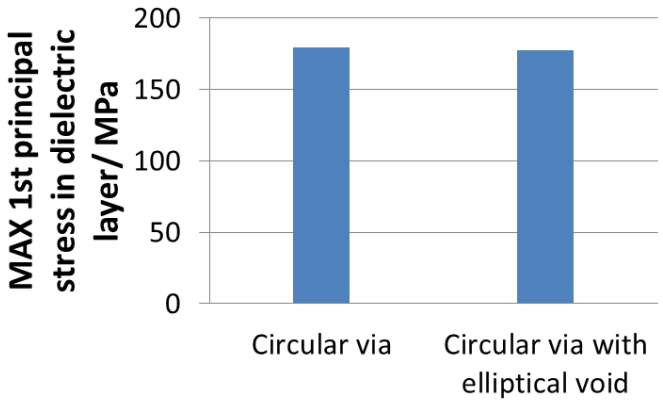


Figure 2.26: 1st principal stress in dielectric layer for a circular via with a 40-μm-long elliptical center void



(a) Equivalent plastic strain in Cu core



(b) 1st principal stress in dielectric layer

Figure 2.27: Effect of 40-μm-long elliptical center void on TSV reliability (at 125 ℃)

CHAPTER 3

FAILURE TEST AND ANALYSIS OF TSV STRUCTURES

In this work, the fabricated TSV samples, as discussed in CHAPTER 2, have been tested in thermal shock chamber from -55 ℃ to 125 ℃. Various experimental techniques, such as resistance measurements with four-point probes, non-destructive 3D X-ray imaging, and scanning electron microscope (SEM) imaging on cross-sectioned samples, have been used to study the failure mechanisms. Finite-element (FE) based fracture models have been developed to understand the interfacial/cohesive crack initiation and propagation mechanisms. A centered finite-difference approach (CFDA) based on Griffith's energy balance has been developed to determine the energy release rate for crack propagation. Also, the virtual crack closure technique (VCCT) has been applied for the interfacial/cohesive cracking analysis. The results from the two approaches - CFDA and VCCT - have been compared. Fracture model results have also been used to explain the reasons behind various interfacial/cohesive failure mechanisms observed in the thermal shock test.

3.1 Thermal-shock test and failure analysis

3.1.1 Thermal shock test

To study the thermomechanical solvability of TSV under external thermal excursions, thermal shock test was conducted. Two samples, each with 3364 TSVs, were cut out from the fabricated wafer and were cycled from -55 ℃ to 125 ℃ by dwelling at each temperature extreme for 15 minutes. The samples were taken out at 100, 200, 500 cycles, and every 500 cycles thereafter, and the electrical resistance of the daisy chain was measured. The resistance of each tested daisy chain was stable around 9 Ω through 4,500 thermal cycles. Although there was no obvious resistance increase, two samples

were taken out after 4,500 cycles to characterize the TSV structures by cross-sectional imaging analysis. After 10,000 cycles, daisy chain failures were detected in some of the samples, followed by another cross-sectional imaging analysis.

3.1.2 Experimental failure analysis

After thermal shock testing, the samples were molded to be able to protect the TSV samples and to avoid any artificial cracking during sample handling and cross-sectioning. Then, the molded samples were fine polished to expose the TSVs. Screening of the cross-sectioned TSV samples was carried out by using Zeiss Ultra 60 FE-SEM® to check any interfacial/cohesive failures. After one row of TSVs was checked, samples were then polished to the next row, and the screening process was repeated.

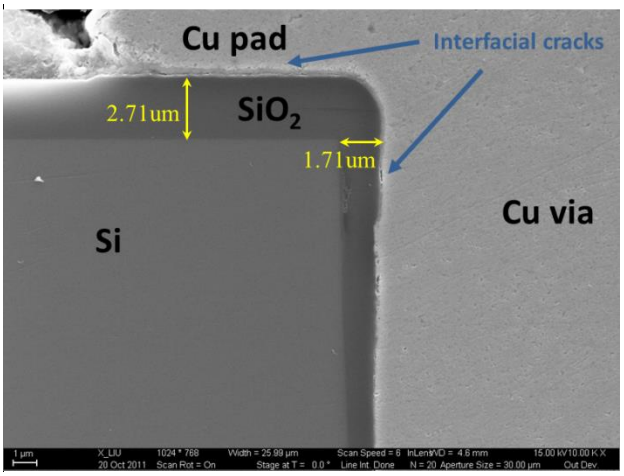
No Cu cracking was found either in Cu vias or in the Cu pads/traces after 4,500 cycles, which may explain why there was no obvious resistance change even after 4,500 cycles. Even after 10,000 cycles, only a limited number of small cracks were found near the Cu pad corners (Figure 3.3). It should be point out that through cracks in the Cu pad/trace must exist in some of the samples because of the detected daisy chain failures.

Cu/SiO_2 interfacial separation and cohesive cracking in SiO_2/Si failures were found at various locations. Representative images were taken at different locations with different magnification to analyze those interfacial/cohesive failures. Although only some of the cross-sectional images are shown in this work, it was commonly seen that a large number of TSVs exhibited interfacial cracking under the pad or on the via side wall. On the other hand, although cohesive cracking was less prevalent, it was still seen in a number of TSVs.

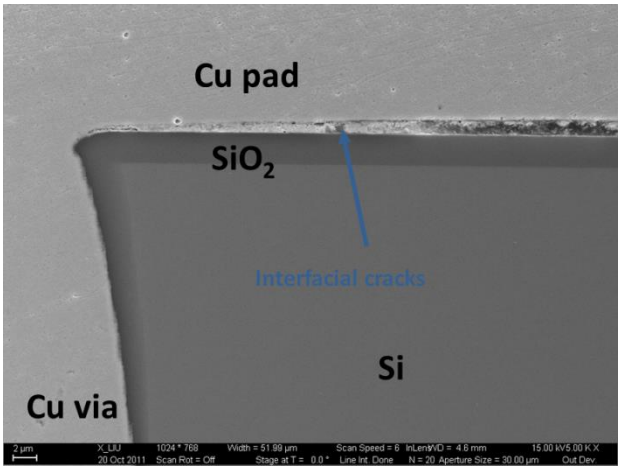
As shown in Figure 3.1 (a) and (b), most of the Cu pads/traces separated from the dielectric layer on wafer top after 4,500 cycles. Also, Cu/SiO_2 interfacial separations had occurred in a number of locations. As the zoom-in picture in Figure 3.1 (c) shows, those interfacial separations generally occurred near the ultra-thin Ti/Cu seed layers, where Cu

vias were electro-plated. Interfacial cracks at those weak interfaces also show a trend to link together and to form longer cracks, which can be seen from the cross-sectional image after 10,000 cycles (Figure 3.4).

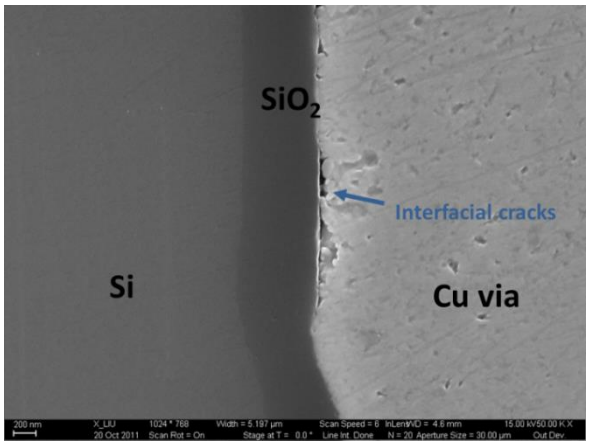
Figure 3.2 (a) shows the semi-loop cohesive cracks, which grew from SiO_2 dielectric to Si, and propagate back to Cu/SiO_2 interface. Figure 3.2 (b) shows another type of cohesive cracking. Multiple cracks grew from SiO_2 towards Si. Some of the small cracks joined each other and formed longer cracks, which grew away from the interfaces.



(a) Interfacial cracks under Cu pad and on the TSV side wall

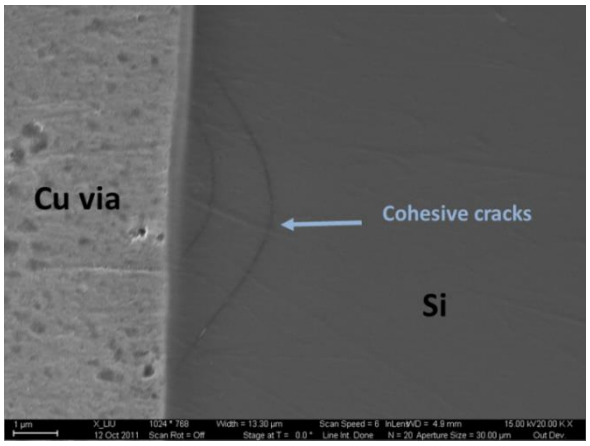


(b) Interfacial cracks under Cu pad/trace

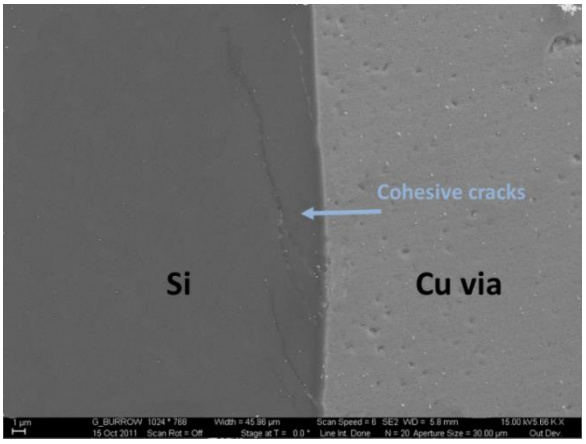


(c) Interfacial cracks on the TSV side wall

Figure 3.1: Cu/SiO_2 interfacial separation after 4,500 cycles



(a) Semi-loop cohesive cracks



(b) Multiple cohesive cracks

Figure 3.2: Si/SiO_2 cohesive cracking after 4,500 cycles

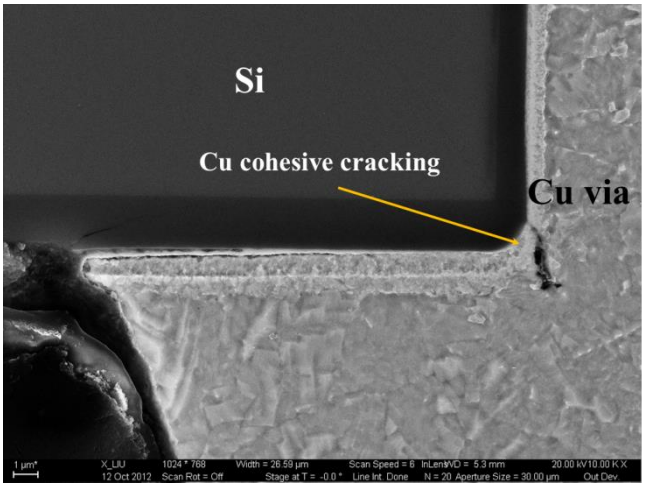


Figure 3.3: Cu cohesive cracking after 10,000 cycles

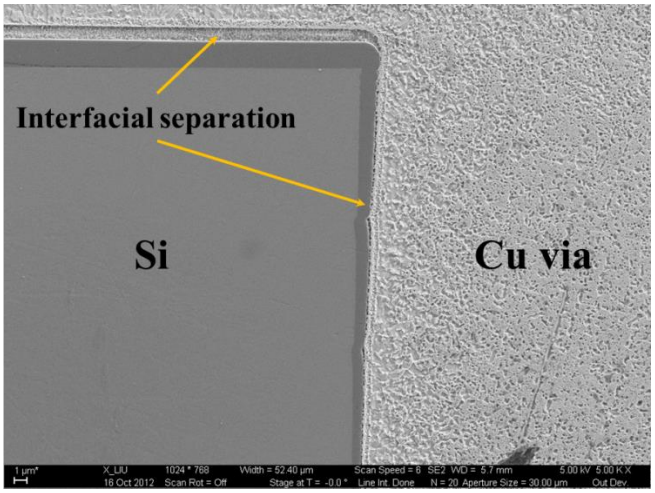


Figure 3.4: Cu/SiO_2 interfacial separation after 10,000 cycles

3.2 Numerical failure analysis

3.2.3 Geometry and material modeling

In parallel to the experiments, finite-element models were developed to simulate the thermal-shock testing of TSVs using ANSYS® V13. For computational reasons, an axisymmetric model was employed in this study. As shown in Figure 3.5, the radial axis is the *x* axis and the vertical axis along the center of TSV is the *y* axis. Due to near-planar symmetry between top and bottom, as a first approximation, only top half of the TSV structure was modeled and symmetric boundary conditions were applied at *y=0*.

Axisymmetric boundary conditions were applied along the center axis of TSV (*x=0*). Also, in this study, coupled periodic boundary conditions were applied on the right edge of the model to mimic the periodicity a TSV in a TSV array. The stress-free temperature for the TSV structure was taken to be 50 ℃ to mimic Cu plating temperature as well as to correlate with XRD measurements, reported in our earlier paper [22]. It is to be noted that although the SiO_2 layer was deposited at 250 ℃, the SiO_2 and Si were assumed to be stress-free at 50 ℃ due to the thin SiO_2 layer as well as due to the minimum difference in CTE between SiO_2 and Si, and thus, the stresses induced by cooling from 250 ℃ to 50 ℃ will be negligible.

For the geometry shown in Figure 3.5, the main dimensions are listed in Table 3.1. The models represented the TSV geometry as close as possible, and the tapered Cu pad edge, different thickness of dielectric layer due to PECVD deposition (Figure 3.1 (a)), filleted via top corners were all accurately modeled. Such a filleted corner will address unusually high stresses due to stress singularity, if the corners were modeled as sharp corners with no fillet. Table 2.4 and Table 2.5 provide the thermomechanical properties of materials.

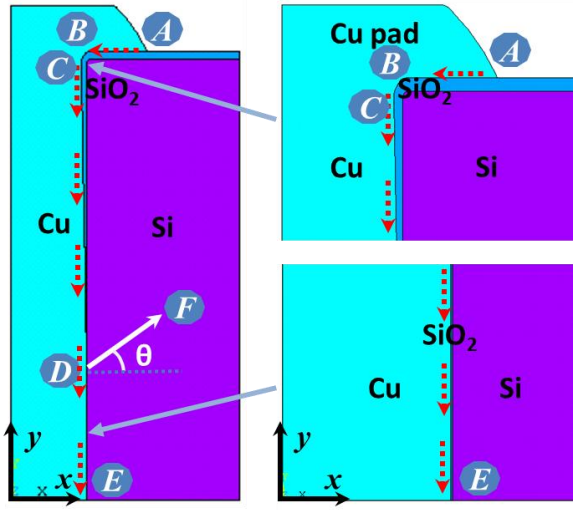


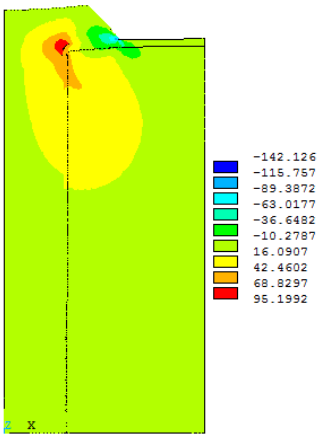
Figure 3.5: TSV model geometry

Table 3.1: TSV sample dimensions

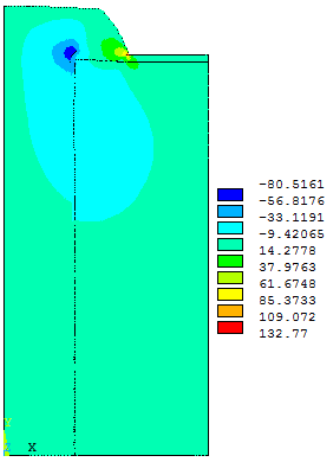
Description	Dimension (μm)
TSV diameter	45
TSV pitch	135
Wafer thickness	260
Cu pad diameter	80
Cu pad thickness	14

3.2.4 Stress analysis

Looking through the failure modes in Figure 3.1 and Figure 3.2, it is clear that wherever there is a SiO_2/Cu interfacial cracking, there is usually no cohesive Si or SiO_2 cracking, and similarly, wherever, there is Si or SiO_2 cohesive cracking, there is usually no interfacial cracking. This is because when one failure mode occurs, it relieves the local stresses, and thus, there is no secondary failure mode in the vicinity. Keeping this in perspective, Figure 3.6 and Figure 3.7 present the stress distribution along SiO_2/Cu interface ***A-B-C-D-E.*** In these figures, S_x represents stress in SiO_2 along the X (radial) direction, S_{xy} represents the shear stress along Cu/SiO_2 interface, and S_1 represents the principal stress in SiO_2. As seen in Figure 3.6 (a) and (b), region ***A-B-C*** has higher interfacial stress, especially at -55 ℃. This high interfacial stress in combination with opening-type tensile radial stress along ***B-C*** at -55 ℃ causes the interface to delaminate. The normal or radial stress along ***B-C*** is tensile at -55 ℃ due to the contraction of higher-CTE Cu compared to the surrounding low-CTE SiO_2 and Si. In the region, ***C-D-E*** where the interfacial stresses are not dominant, SiO_2 tends to crack due to high principal stress, as illustrated in Figure 3.2.

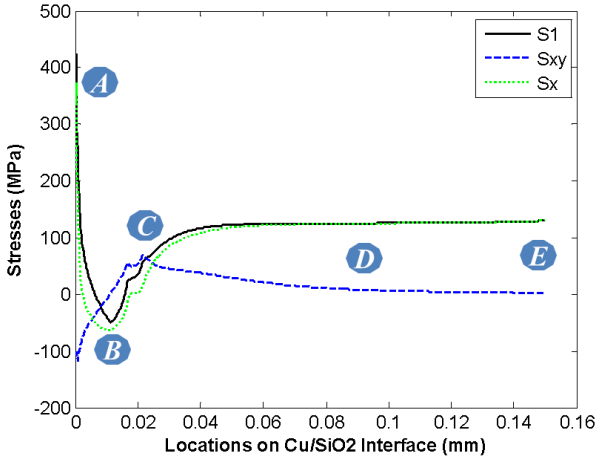


(a) Shear stress at -55 ℃

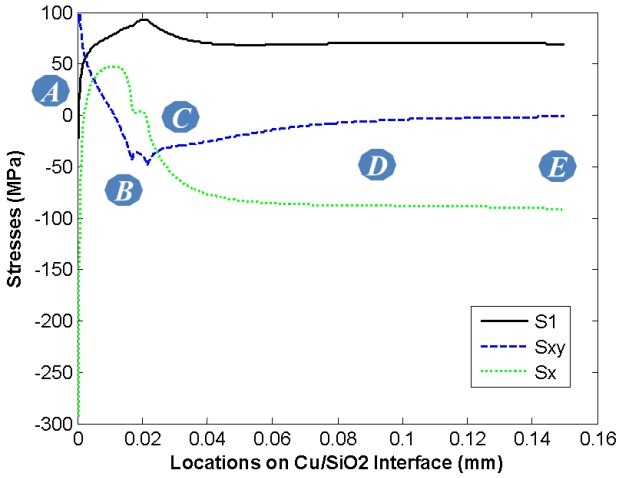


(b) Shear stress at 125 ℃

Figure 3.6: Shear stress in TSV structure



(a) Stresses along Cu/SiO_2 interface at -55 ℃



(b) Stresses along Cu/SiO_2 interface at 125 ℃

Figure 3.7: Stresses along Cu/SiO_2 interface

3.2.5 Fracture-mechanics methodology

Based on the stress analysis, a fracture mechanics analysis was also performed to determine the likelihood of interfacial crack propagation along the Cu/SiO_2 interface as well as cohesive crack propagation in Si/SiO_2 material. Starting with an initial crack of 1 μm, either along the Cu/SiO_2 interface or in Si/SiO_2 material, the energy release rate (G) for crack propagation was determined. The starting locations for the crack were determined by the stress contours presented in the previous section. Two techniques, as discussed below, have been employed for determining G.

A. Centered finite-difference approach (CFDA)

Under thermomechanical loading, no external work is performed, and therefore, the energy release rate can be determined as the rate of change in strain energy with crack extension. Based on Griffith's energy balance [48], two FE models need to be built for each analysis [16], one with a crack length of a, and another with a crack length $a+\Delta a$. The change in the total strain energy between the two models can be divided by the increase in crack surface area (ΔA) to approximate energy release rate G:

$$G = -\frac{U_{a+\Delta a} - U_a}{\Delta A} \tag{3.1}$$

where $U_{a+\Delta a}$ is the strain of the entire model for a crack length of $a+\Delta a$ and U_a is the strain energy of the entire model for a crack length of a. For an interfacial crack along the vertical wall of the TSV, ΔA linearly changes with Δa, while along the pad or circumferential area at the top of the TSV (along ***A-B-C***), every crack increment Δa represents a revolved crack surface. Thus, for the same increment Δa, the radius of the revolved surface may be different depending on the location and direction of the crack. Therefore, the crack surface area increment ΔA keeps changing as crack propagates.

One concern with applying (3.1) for G value calculation is that it requires a sufficient small crack increment Δa ($\Delta a/a \leq 1.0\%$) to calculate G value at crack length a. For such a small increment, numerical error may result in unstable and unreliable G value [49]. On the other hand, if we need to continuously monitor crack propagation, for each crack length a along the crack propagation path, two models of crack length a and $a+\Delta a$ need to be calculated, which doubles the calculation time.

Since (3.1) is mathematically the slope at crack length a, G values corresponding to each crack length along the crack propagation path can be approximated by calculating the slopes of the total strain energy vs. crack surface area curve. Numerically, centered difference method gives higher order of accuracy than the first forward difference method and the backward difference method [50], thus, we rewrite (3.1) as:

$$G = -\frac{U_{a+\Delta a} - U_{a-\Delta a}}{A_{a+\Delta a} - A_{a-\Delta a}} \tag{3.2}$$

where $U_{a-\Delta a}$ and $U_{a+\Delta a}$ are the total strain energies at crack $a-\Delta a$ and $a+\Delta a$. However, theoretically, equation (3.2) applies only to equal crack surface area increment ($A_{a+\Delta a} - A_a = A_a - A_{a-\Delta a}$), which applies to the vertical wall of the TSV, but not for the Cu pad/SiO_2 interface region. Therefore, the following equation should be applied to calculate G at crack length a:

$$G = -\left[U_{a-\Delta a1}\frac{A_a - A_{a+\Delta a2}}{\left(A_{a-\Delta a1} - A_a\right)\left(A_{a-\Delta a1} - A_{a+\Delta a2}\right)} + U_a\frac{2A_a - A_{a+\Delta a2} - A_{a-\Delta a1}}{\left(A_a - A_{a-\Delta a1}\right)\left(A_a - A_{a+\Delta a2}\right)} + U_{a+\Delta a2}\frac{A_a - A_{a-\Delta a1}}{\left(A_{a+\Delta a2} - A_{a-\Delta a1}\right)\left(A_{a+\Delta a2} - A_a\right)}\right] \quad (3.3)$$

Here Δa_1 and Δa_2 are the crack increment before and after crack at a, and Δa_1 and Δa_2 can be different.

B. Virtual crack closure technique (VCCT)

The virtual crack closure technique is developed by Rybicky and Kanninen in 1977 [51] based on the assumption that the energy released when crack propagates from a to $a+\Delta a$ is the same as the energy required to close the crack increment Δa. For quadratic 2D plane element, we have:

$$G_I = -\frac{1}{2\Delta A}\left[Y_i\left(v_l - v_{l*}\right) + Y_j\left(v_m - v_{m*}\right)\right] \quad (3.4)$$

$$G_{II} = -\frac{1}{2\Delta A}\left[X_i\left(u_l - u_{l*}\right) + X_j\left(u_m - u_{m*}\right)\right] \quad (3.5)$$

Here, X_i, X_j, Y_i, and Y_j are nodal forces in X and Y directions, respectively, at nodes i and j in Figure 3.8. u_l, u_{l*}, u_m, and u_{m*} are displacement in the X direction at node l, m, $l*$, and $m*$. Similarly, v_l, v_{l*}, v_m, and v_{m*} are displacement in the Y direction at node l, m, $l*$, and $m*$. ΔA is the crack surface area increment corresponding to each crack increment Δa for axisymmetric analysis, as discussed above.

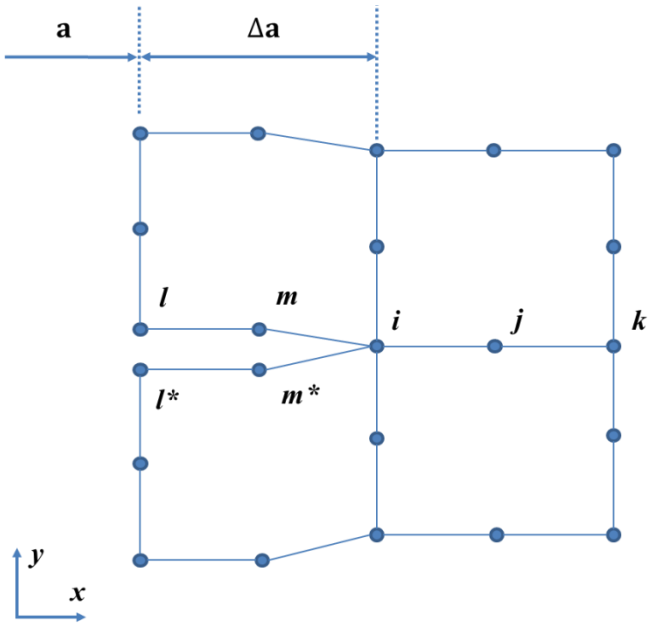


Figure 3.8: Eight-node quadratic plane element around crack tip

3.2.6 Fracture analysis

Cu/SiO$_2$ interfacial separation

Stress analysis in Figure 3.6 and Figure 3.7 show that large interfacial stress invariably occurs near the Cu pad outer corners (point ***A*** in Figure 3.5). Also, as shown in Figure 3.1, experimental observations indicate large amount of interfacial separations occur under the Cu pads/traces. Therefore, the interfacial fracture model assumes crack initiates from Cu pad outer corners and propagates along Cu/SiO$_2$ interface through point ***B***, ***C*** and ***D*** in Figure 3.5. This interfacial crack path is chosen to analyze whether the cracks under the Cu pad, which were frequently observed in the experimental test, can grow through the Cu pad corner and cause catastrophic complete separation between Cu via and the surrounding SiO$_2$/Si. Based on the results presented in this work, the interfacial crack is less likely to propagate beyond the TSV corner, and if it propagates beyond the corner, it is likely to quickly propagate along the vertical wall of TSV toward the center of the via. Mesh convergence study was conducted first. Uniform mesh was used along the crack path ***A-B-C-D-E***. For the crack propagation analysis, a crack

increment $\Delta a = 0.4\,\mu m$ was used. The small crack increment ensures the accuracy of *G* value calculation with CFDA. Also, it helps capture any sharp *G* change near the corners/edges.

As shown in Figure 3.9, the total strain energy (*U*) of the entire TSV structure at each crack increment was plotted against the total crack surface area. The *G* values at each crack increment were then computed using equation (3.3) of CFDA. Figure 3.10 shows the interfacial *G* values calculated using CFDA and VCCT for at -55 ℃. It shows that both techniques give perfectly matched *G* value for linear elastic case, where Cu plastic deformation is not considered. If Cu plastic deformation is considered, VCCT overestimates the *G* along path ***B-C-D-E***, especially at point ***E***, where the interfacial crack almost separates Cu via from the surrounding silicon substrate (Figure 3.11). The discrepancy is because that VCCT is only applicable to linear elastic fracture mechanics (LEFM) [51], which requires plastic deformation to be confined in a small region surrounding the crack tip. As seen in Figure 3.11, plastic strain on path ***B-C-D-E*** is larger than that along ***A-B***, which may explain why CFDA matches with VCCT better on path ***A-B*** than that on ***B-C-D-E*** when Cu plasticity is considered. Figure 3.10 also shows that the *G* values are generally smaller when Cu plasticity is applied in the model due to plastic work dissipation. In general, *G* vs. crack surface area curve of both elastic-plastic and linear-elastic cases show similar trend. In the rest of this work, only elastic-plastic results will be presented.

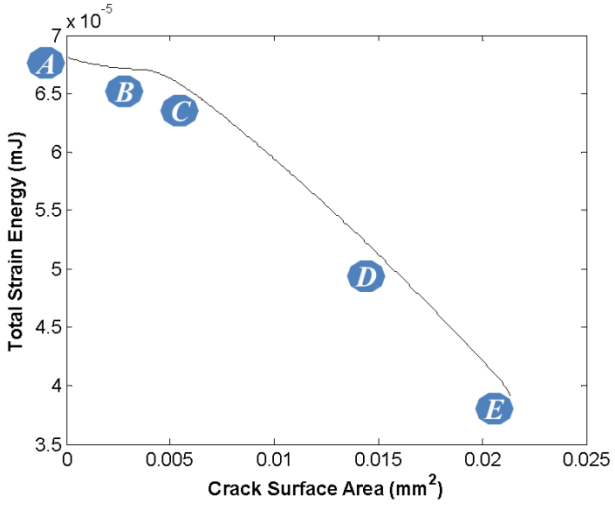


Figure 3.9: Total strain energy vs. crack surface area for Cu/SiO_2 interfacial separation at -55 ℃

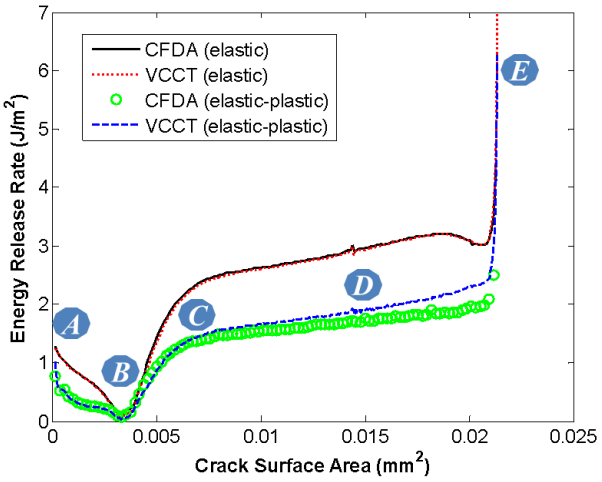


Figure 3.10: *G* vs. crack surface area for Cu/SiO_2 interfacial separation at -55 ℃

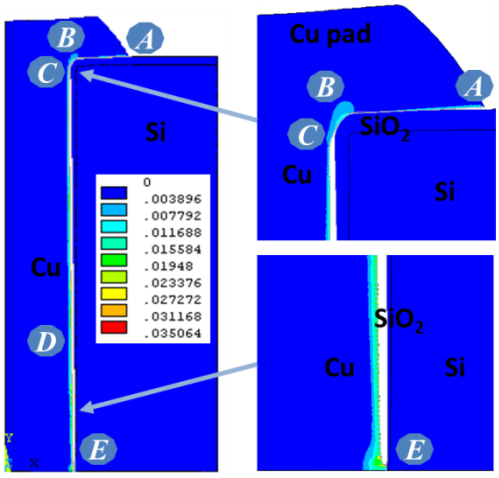


Figure 3.11: Equivalent plastic strain contours at -55 ℃ (deformation is scaled ×20 for clarity)

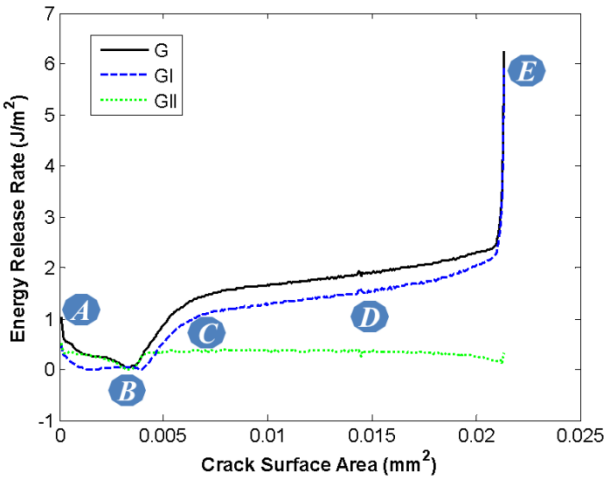


Figure 3.12: *G, G_I, and G_{II}* vs. crack surface area for Cu/SiO_2 interfacial separation at -55 ℃

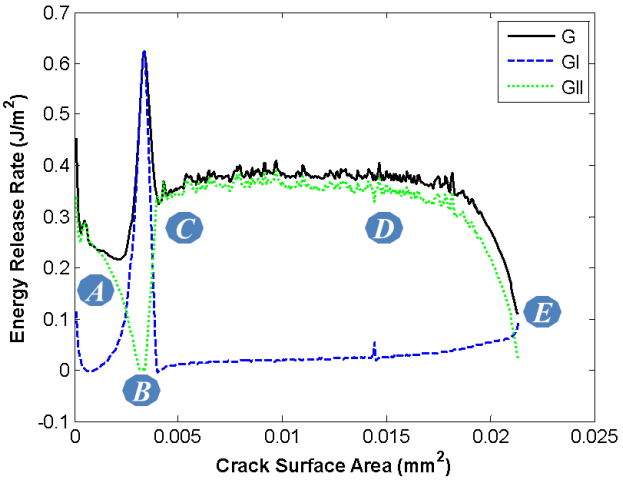


Figure 3.13: *G, G_I, and G_{II}* vs. crack surface area for Cu/SiO_2 interfacial separation at 125 ℃

In the literature, the Cu/SiO_2 debonding energy varies from about 0.7 J/m^2 to 10 J/m^2 depending on the mode mixity [52]. Based on the results presented in Figure 3.12 and Figure 3.13, it is seen that the computed *G* values at some of the locations are of comparable magnitude to interfacial debonding energy, and therefore, interfacial crack propagation is possible in these locations.

Figure 3.12 presents the mode mixity analysis of the Cu/SiO_2 interfacial crack propagation at -55 ℃. At point ***A***, crack initiation are due to the combined effect of high shear stress caused by the differential shrinkage of Cu pad and Si substrate and the sinking of Cu via, which pulls the Cu pad inward and causes an open force on the Cu pad edge. However, as crack propagates towards ***B***, G_{II} is much higher than G_I, sliding mode dominates. *G* decreases almost to zero when crack grows from Cu pad bottom to Cu via side (***A-B***). When the crack propagates to point ***B***, it is almost closed. On the contrary, at 125 ℃ (Figure 3.13), there is a spike at location ***B***, induced by large G_I, indicating an open crack. Therefore, it is possible that crack is able to propagate through ***B*** in thermal shock test. However, because the *G* values at 125 ℃ is one order of magnitude smaller than those at -55 ℃, the chance for crack to grow through ***B*** is slim, which may explain

why no interfacial crack has been found propagating all the way from Cu pad edge to via side in the thermal shock test.

In summary, it can be said that any interfacial crack that starts near the pad is not likely to crack propagate beyond the TSV corner. However, if the interfacial cracks grow through the TSV corner, catastrophic complete separation between the Cu via and surrounding SiO_2/Si will occur. Also, any interfacial crack that originates in the vertical wall due to processing defects is likely to propagate toward the center of the via, if there is no cohesive cracking of SiO_2/Si. It should be pointed out that in all of these studies, G value at 125 ℃ and -55 ℃ have been used for crack propagation analysis, while in reality, the interfacial crack grows due to thermal shock cycling, and thus, ΔG needs to be considered in the context of Paris-law like model.

SiO_2/Si cohesive cracking

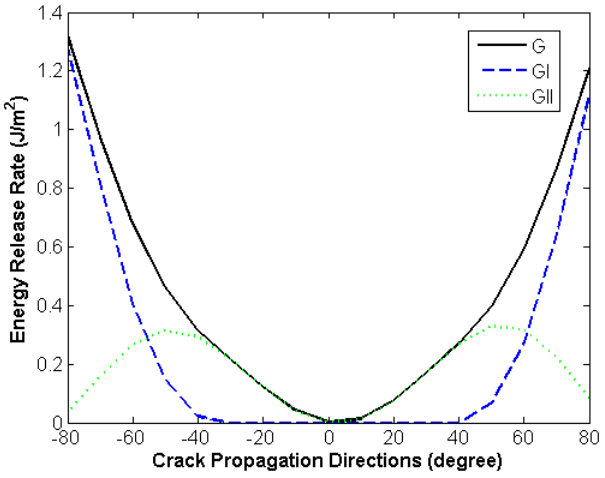
As discussed earlier, SiO_2/Si cohesive cracking is more likely to occur along ***C-D-E***, where SiO_2 principal stress is high but shear stress is relatively low. In this study, cohesive cracking in SiO_2/Si is assumed to initiate at point ***D***, which is 90 μm from the wafer top. Crack grows through SiO_2 and then propagates into surrounding silicon. As shown in Figure 3.5, to find possible crack initiation/propagation directions, cracks ***D-F*** along different directions θ have been modeled.

Figure 3.14 (a) shows the variation of G_I and G_{II} as well as G as a function of angle of the crack. As discussed earlier, an angle of 0 ºindicates that the crack is along the horizontal or x direction, and an angle of 90 ºindicates that the crack is along the vertical or y direction. At -55 ℃, due to the greater Cu CTE, SiO_2 is under tension in x direction and under compression in y direction. Thus, a crack is likely to open at higher angles and thus, G_I dominates. On the other hand, at 125 ℃, the opposite stress field takes place, and thus, G_I dominates in lower angles, as shown in Figure 3.14 (b). Furthermore, it is seen that the energy available for crack propagation is much greater at -55 ℃ than at 125 ℃, and therefore, the cracks are likely to propagate during low-temperature dwelling. Figure

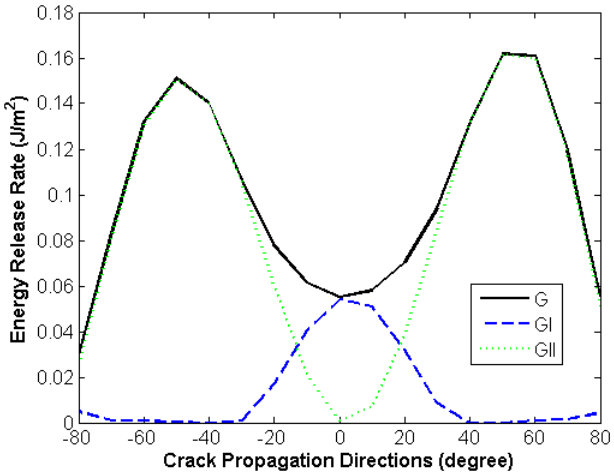
3.14 shows that *G* values are high at both high and low temperature extremes when the angle of crack propagation is around (40 ºto 60 º) or (-40 ºto -60 º). Thus, we take these angle ranges as the potential cohesive crack growth directions, which can also be seen in the SEM images in Figure 3.2.

Propagation analysis of all the cohesive cracks that start with different initial angle of θ, *G* values invariably level off. This indicates cracks may arrest or grow back to the interface, and forming semi-loop cracks, as shown in Figure 3.2 (a). To analyze this, models were built with cracks initially grow along 50 ºdirection (Figure 3.15), then turn to different directions: back to interfaces by turning another 30 º inward (Back), continuing along 40 º(Straight), and away from interfaces by turning another 30 ºoutward (Away). Results in Figure 3.16 show that although at 125 ℃, cracks are more likely either go straight or away from the interfaces, cracks will quickly go back to the interfaces at -55 ℃, which has much higher *G* values.

In summary, it can be said that cohesive cracks are likely to start at an angle of 30 ºto 50 ºfrom the TSV wall, and depending on the crack length, they will loop back to the TSV wall, as seen in experimental cross-sections and finite-element models.



(a)



(b)

Figure 3.14: *G* vs. crack propagation directions for SiO_2/Si cohesive cracking at (a) -55 ℃, (b) 125 ℃

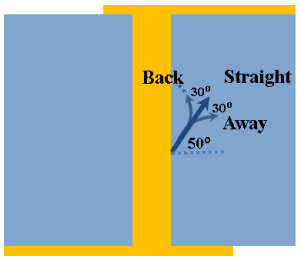


Figure 3.15: SiO_2/Si cohesive cracking directions

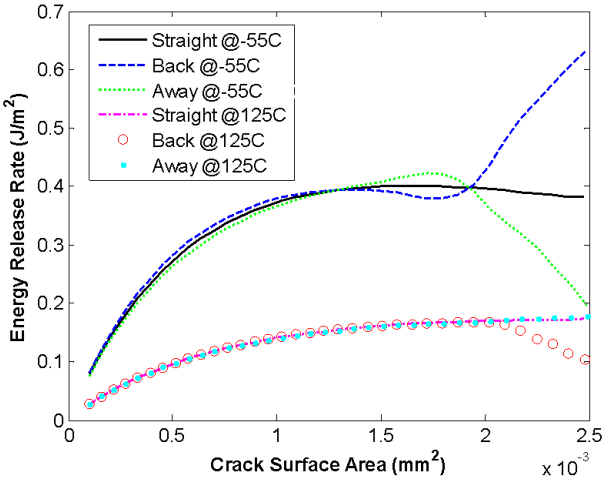


Figure 3.16: *G* vs. crack surface area for SiO_2/Si cohesive cracking

CHAPTER 4

IN-SITU MICRO STRAIN MEASUREMENTS OF TSV STRUCTURES

To study thermomechanical strain induced by the CTE mismatch TSV structures and thus provide fundamental understanding of TSV thermomechanical reliability, strain measurements have been performed using synchrotron x-ray diffraction (XRD). The measured strains are available as two-dimensional (2D) distribution maps, whereas the strain distributions in TSVs are three-dimensional (3D) in nature. To understand this 3D to 2D data projection process, a data interpretation method based on beam intensity averaging is proposed and validated with measurements. The proposed method is applicable to XRD strain measurements on thin as well as thick samples.

4.1 Sample preparation

TSVs were fabricated[2] with silicon dioxide and photodefined polymer (SU-8) liners. With respect to the fabrication of TSVs with silicon dioxide liner [15], a silicon dioxide layer was deposited on one side of a silicon wafer, as shown in Figure 4.1. Vias were etched in the silicon wafer using anisotropic etching, followed by the etching of a group of micro-vias, called mesh [15], in the suspended silicon dioxide layer at the base of the vias. Thermal oxidation was performed as a next step followed by a titanium-copper seed layer deposition over the silicon dioxide layer at the mesh end of the vias. After seed layer deposition, copper electroplating was performed to pinch off the openings in the mesh. Once the mesh openings were pinched off, bottom up copper

[2] TSV samples were fabricated by Mr. Paragkumar A. Thadesar at the Georgia Tech Institute for Electronics and Nanotechnology

electroplating of the vias was performed followed by chemical-mechanical polishing (CMP) to remove overburden copper. TSVs with polymer liner [53] were fabricated with mesh, similar to the TSVs with silicon dioxide liner. SU-8 was spin coated to fill the etched vias and photolithography of the SU-8 was performed to obtain a thick polymer liner. Once the polymer liner was fabricated, mesh pinch off, bottom up TSV copper electroplating and CMP were performed.

The dimensions of the fabricated TSV samples are shown in Table 4.1. Once the TSV samples were fabricated, cross-section polishing was performed until a specifically defined amount of silicon was left in front of the first row of TSVs to preserve the TSV/silicon mechanical boundary condition, as shown in Figure 4.2.

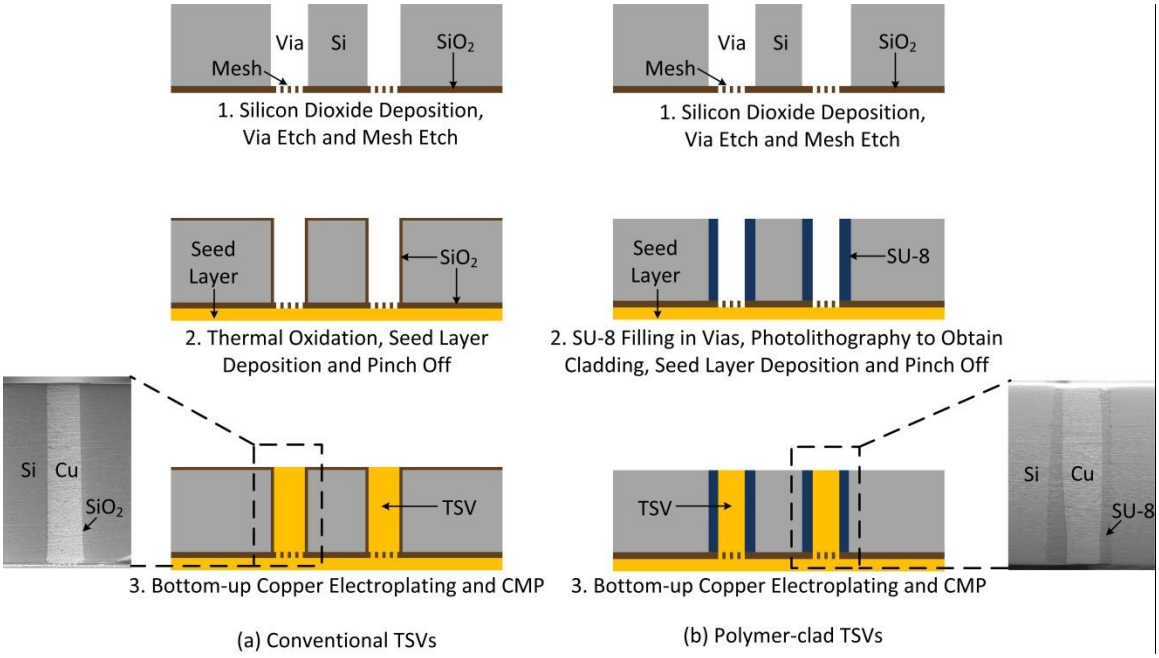


Figure 4.1: TSV fabrication processes

Table 4.1: Dimensions of the fabricated TSVs

Sample No.	**S1**	**S2**	**S3**	**S4**
TSV Diameter (µm)	30	50	80	80
TSV Pitch (µm)	60	150	250	250
TSV Height (µm)	300	300	390	390
Front Si Thickness (µm)	13	50	55	40
Liner Thickness (µm)	1	1	1	25
Liner Material	SiO_2	SiO_2	SiO_2	SU-8

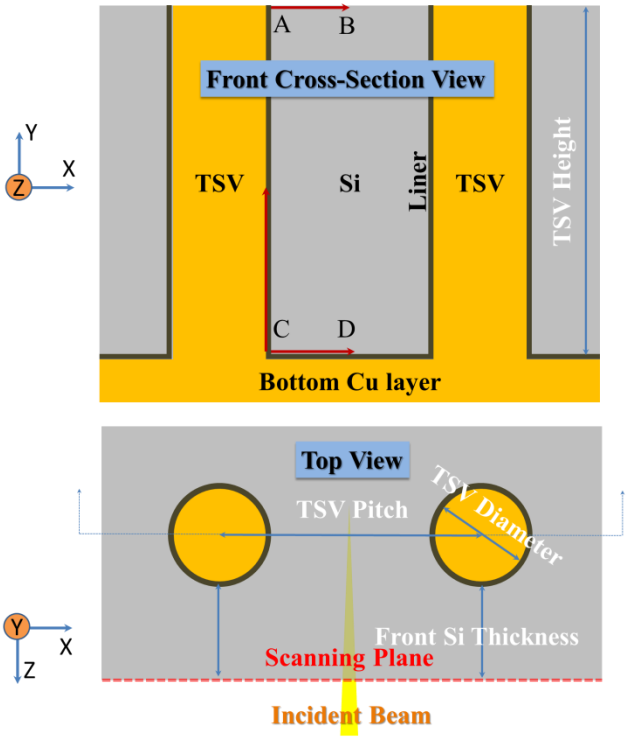


Figure 4.2: Schematic view of a representative TSV array

4.2 Synchrotron XRD measurements

Synchrotron XRD measurements were performed on the fabricated TSV samples at beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL). Before the test, samples were mounted on a high-precision stage [54], with the scanning plane being 45° from the incident beam (Figure 4.3). As shown in Figure 4.4, X-ray fluorescence scans were initially conducted on the scanning plane to locate target TSVs. A polychromatic Laue diffraction scan (5keV to 22keV in 0.01keV steps) was then performed at 150 ℃ to measure the deviatoric strain distribution, followed by a hydrostatic strain measurement of the TSVs at multiple locations on the scanning plane using monochromatic scan. However, due to limited information obtained from the monochromatic scans of the selected locations, only deviatoric strain distributions were analyzed for the entire TSV scanning plane. The x-ray beam was

focused to a 1 micron size via a pair of elliptically bent Kirkpatrick-Baez mirrors. Laue pattern data analysis and monochromatic powder diffraction analysis were carried out using X-ray Microdiffraction Analysis Software (X-MAS) [55, 56] to calculate the full strain tensor.

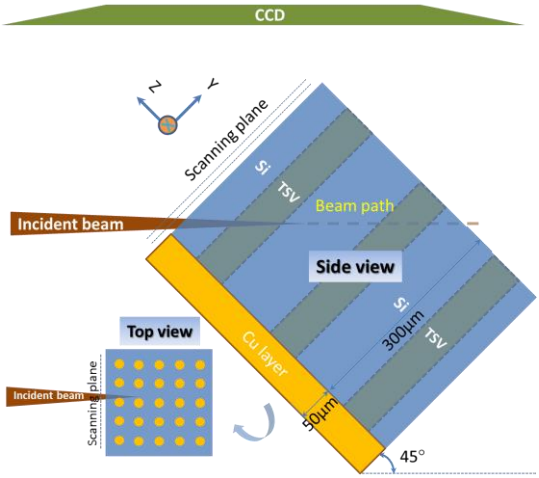


Figure 4.3: TSV array sample under synchrotron x-ray diffraction test

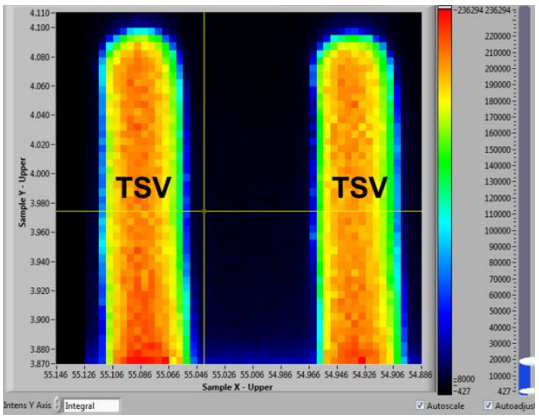


Figure 4.4: Fluorescence scans to locate TSVs

4.3 Data interpretation methodology development

Figure 4.5 shows the measured 2D equivalent deviatoric strain map of silicon, where two neighboring TSVs were scanned to study the interactions between them. As seen, the highly stressed regions are near the TSVs. However, as discussed before, the 2D strain maps actually represent 3D strain distributions in silicon around TSVs. Since x-

rays attenuate (Figure 4.6) as they penetrate through the TSV sample due to photoelectric absorption, scattering, and pair production [57], the strongest signal and thus the major component of the collected information is from the front section of the TSVs. This raises two questions: how deep is the front section and how the information from the front section is represented in the 2D strain maps? The answers to these questions are essential for the interpretation of measurement results and thus understanding the TSV thermomechanical reliability.

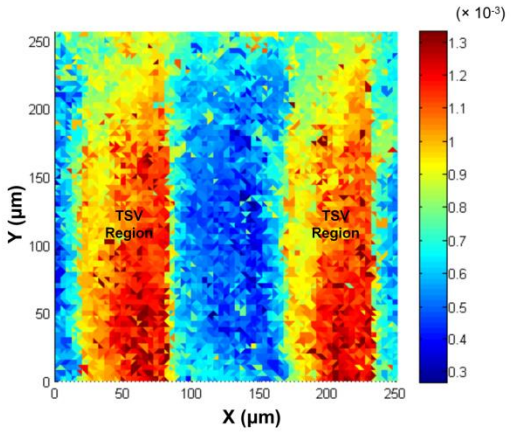


Figure 4.5: Measured equivalent deviatoric strain $\varepsilon_{eq}^{'}$ (Eq. (1)) distribution map of silicon at 150 °C

$$\varepsilon_{eq}^{'} = \frac{2}{3}\sqrt{\frac{(\varepsilon_{xx}^{'}-\varepsilon_{yy}^{'})^2+(\varepsilon_{yy}^{'}-\varepsilon_{zz}^{'})^2+(\varepsilon_{zz}^{'}-\varepsilon_{xx}^{'})^2+6(\varepsilon_{xy}^{'\,2}+\varepsilon_{yz}^{'\,2}+\varepsilon_{xz}^{'\,2})}{2}} \tag{4.1}$$

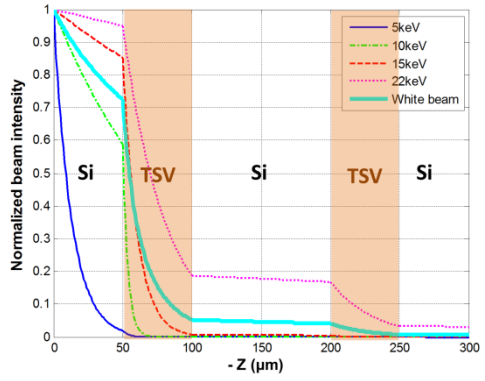


Figure 4.6: Beam intensity attenuation in the TSV sample

To answer the above questions, a beam intensity based data averaging method is proposed. Due to thermomechanical strain deformation in the sample, kinematical conditions apply in silicon crystals, and thus we assume that the contribution of the collected data to the final 2D strain maps depends on the distribution of the beam intensity along the beam penetration direction. In other words, since the beam intensity is higher near the front section, the strain data in this section has larger effect on the 2D strain maps, which is realized through beam intensity based weight function. The detailed data interpretation process is presented in Figure 4.7. The proposed beam intensity based data averaging method calculates the intensity of the incident beam taking the white beam (5keV to 22keV) in 0.01keV steps [54] as the beam passes through the TSV center lines. In this beam intensity averaging model, the flux corresponding to each energy spectrum of the white beam is taken into account using the corresponding mass attenuation coefficients. The fluxes with different energies have different penetration depth. Consequently, each flux can only be considered for a specific penetration depth and thus the hkl corresponding to their energy spectrum contribute only up to a certain depth. The penetration depth is defined as the distance from the surface to where the intensity of x-rays falls to 1/*e* of its value at the surface, where *e* is the Euler's number. Since the TSV critical failures are mainly caused by cohesive cracks in silicon and interfacial separation between the copper and the silicon [18], silicon was selected as the material of interest. Only the fluxes corresponding to the beam intensities in the silicon are calculated and then normalized to form the white beam intensity weight function $w(z)$, where $\sum w_i(z) = 1$. Simultaneously, finite element TSV array models are built with the same geometry (Table 4.1) and materials (Table 4.2) as the tested TSV samples. It should be pointed out that different copper mechanical properties are used in current models than that listed in Table 2.4. This is because mechanical properties of copper change with different electroplating parameters. An in-house nanoindentation test on the

fabricated TSV samples indicates that the copper Young's modulus is around 70 GPa, and therefore, similar copper properties [58] are used for current models. Comparison study reveals that models using these two different copper mechanical properties predict very similar strain distribution with 10%~15% magnitude difference. To capture the process-induced stress of the TSV array, the thermal profile of the fabrication process (Figure 4.1) is sequentially applied to the model. To mimic the sequential fabrication process, all the materials are activated sequentially at their process stress-free temperature through the ANSYS® element birth-and-death approach. Since no adhesion layers exist between copper vias and surrounding liner materials in current TSV samples, contact elements are applied on the Cu/SiO_2 interfaces. Thereafter, the deviatoric or hydrostatic strains along the beam penetration depth direction are read out and multiplied by the beam intensity based weight function ($\varepsilon = \sum w_i \varepsilon_i$) to get a strain value at any given point on the scanning plane. This process is repeated until all the points on the scanning plane are covered. Depending on the materials along the penetration path, the penetration depth and the weight function keep changing as the beam moves in the scanning plane.

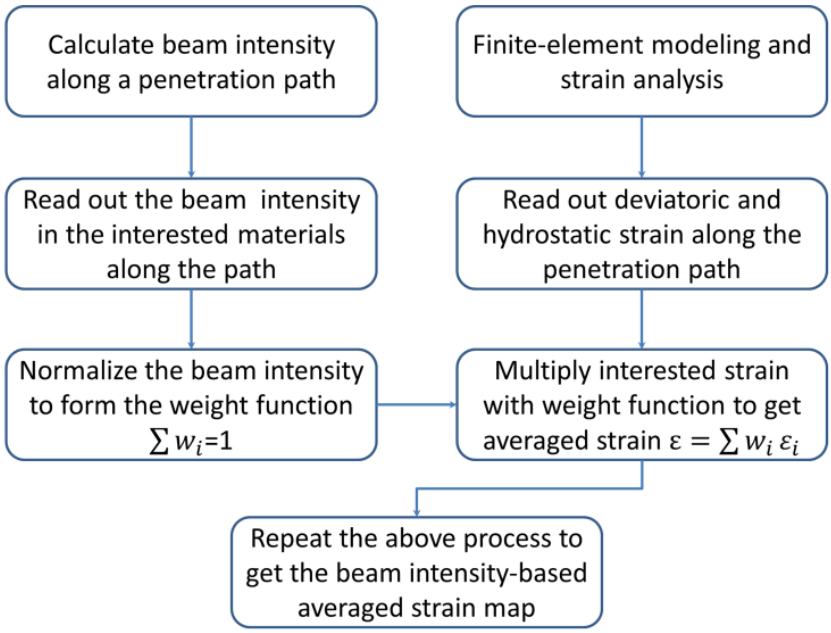
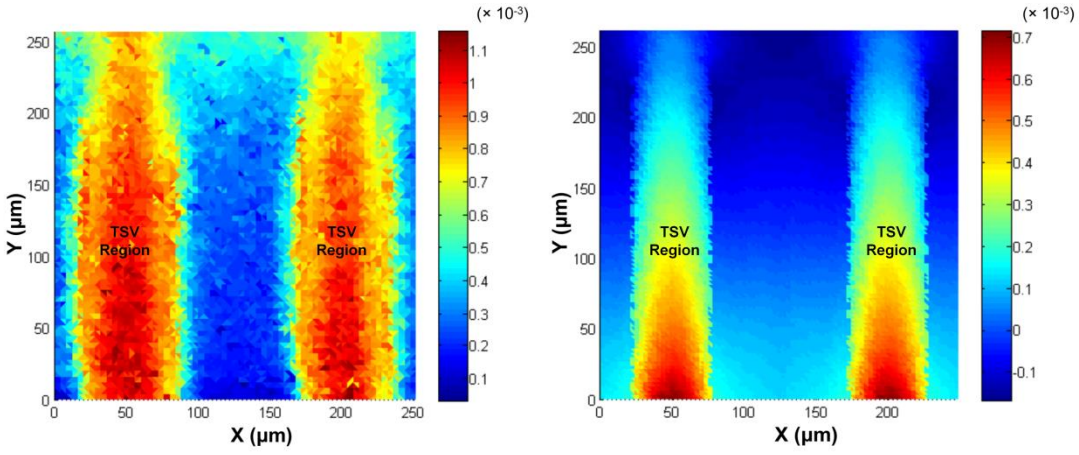


Figure 4.7: Process flow of the beam intensity based data averaging method

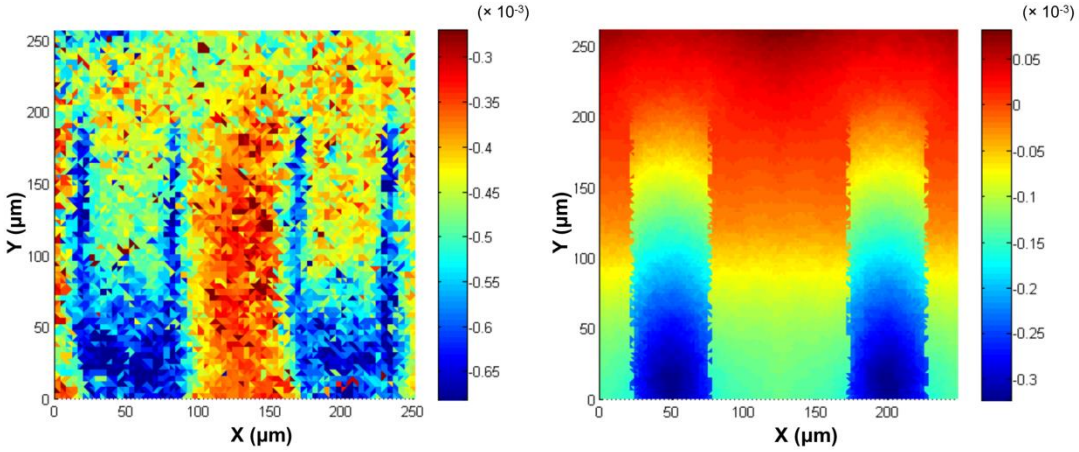
Table 4.2: Material properties [18, 58, 59]

	Cu	Si	SiO_2	SU-8
Young's modulus (GPa)	70	130.9	71.4	4.02
Poison ratio	0.3	0.28	0.16	0.22
CTE (ppm/°C)	17.3	2.6	0.5	52

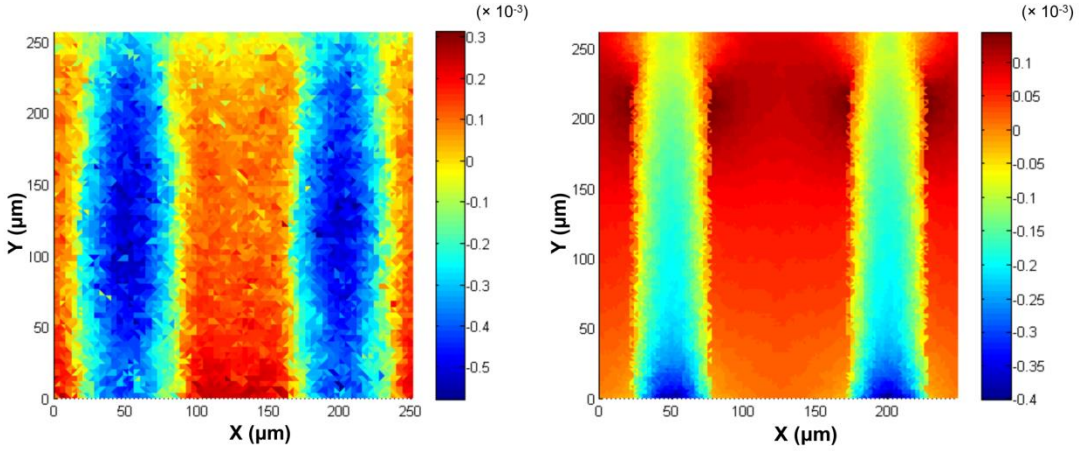
Figure 4.8 shows all the measured silicon deviatoric strain components at 150 °C and the model prediction using beam intensity based data averaging method for sample S1 in Table 4.1. The model shows that the CTE mismatch induced copper pumping at 150 °C causes large stress near the copper silicon interfaces, which is consistent with previous understandings [18]. The comparison shows that the model results generally agree well with the measurement data on strain distribution with some discrepancies due to various reasons. First, it was observed that while repeating the measurements on the same sample, a few measured values differed from the modeled values due to the stress history during the high temperature measurements. However, the strain distribution remained unchanged. Second, the finite element model considers an ideal thermal loading case without accounting for the fabrication induced defects and copper grain coarsening during the fabrication. Even with the discrepancies in some of the strain magnitudes, both of the modeled and measured strain distribution trends matched well for all the six components, and the trends are useful to identify critical locations in the silicon.



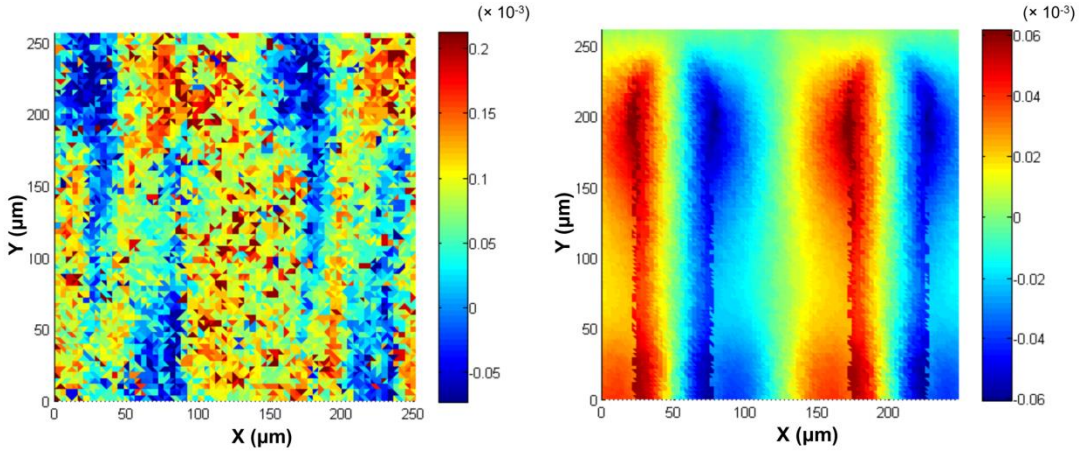
$(a)\ \varepsilon'_{xx}$



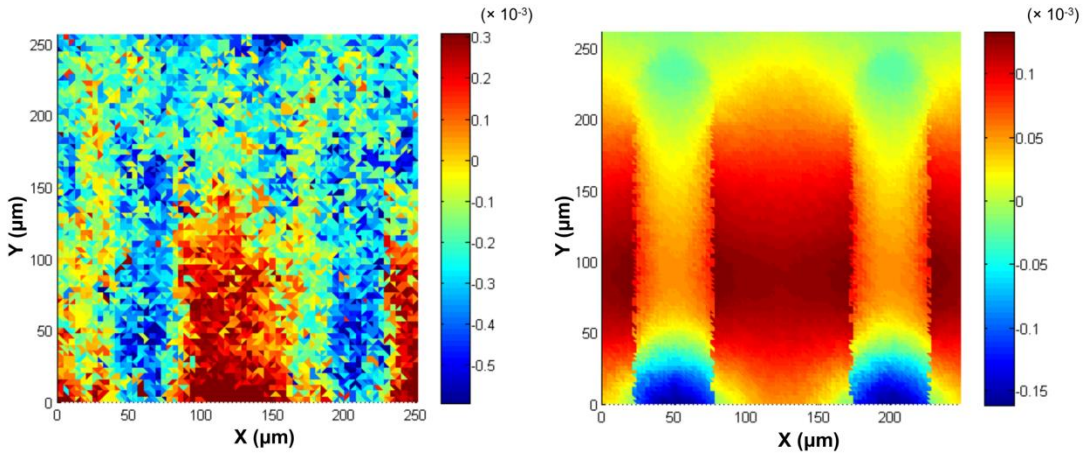
$(b)\ \varepsilon'_{yy}$



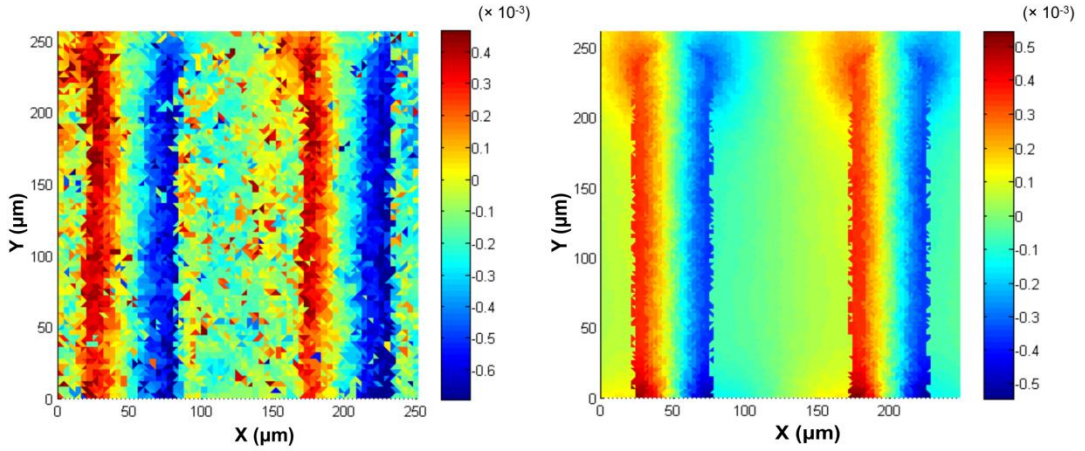
$(c)\ \varepsilon'_{zz}$



$(d)\ \varepsilon'_{xy}$



$(e)\ \varepsilon'_{yz}$



$(f)\ \varepsilon'_{xz}$

Figure 4.8: Measured deviatoric strain distribution maps of silicon (left) vs. model predicted strain maps (right) at 150 °C (S2)

The above analysis with beam intensity based data averaging method used the white beam intensity for data analysis. As seen in Figure 4.7, different energy spectrums will result in different penetration depths and different weight function shapes. Thus, it is necessary to understand the effect of beam energy spectrum on the final results. Taking ε'_{xx} as an example, Figure 4.9 shows the strain distribution using 5keV, 10keV, 15keV, and 22keV for the beam intensity based data averaging method. With energies higher than 15keV, the predicted strain distributions stabilize, which indicates that the high

energy spectrums dominate the final strain results. This also means that the final 2D strain map is a combined strain along the penetration depth instead of just near the front surface.

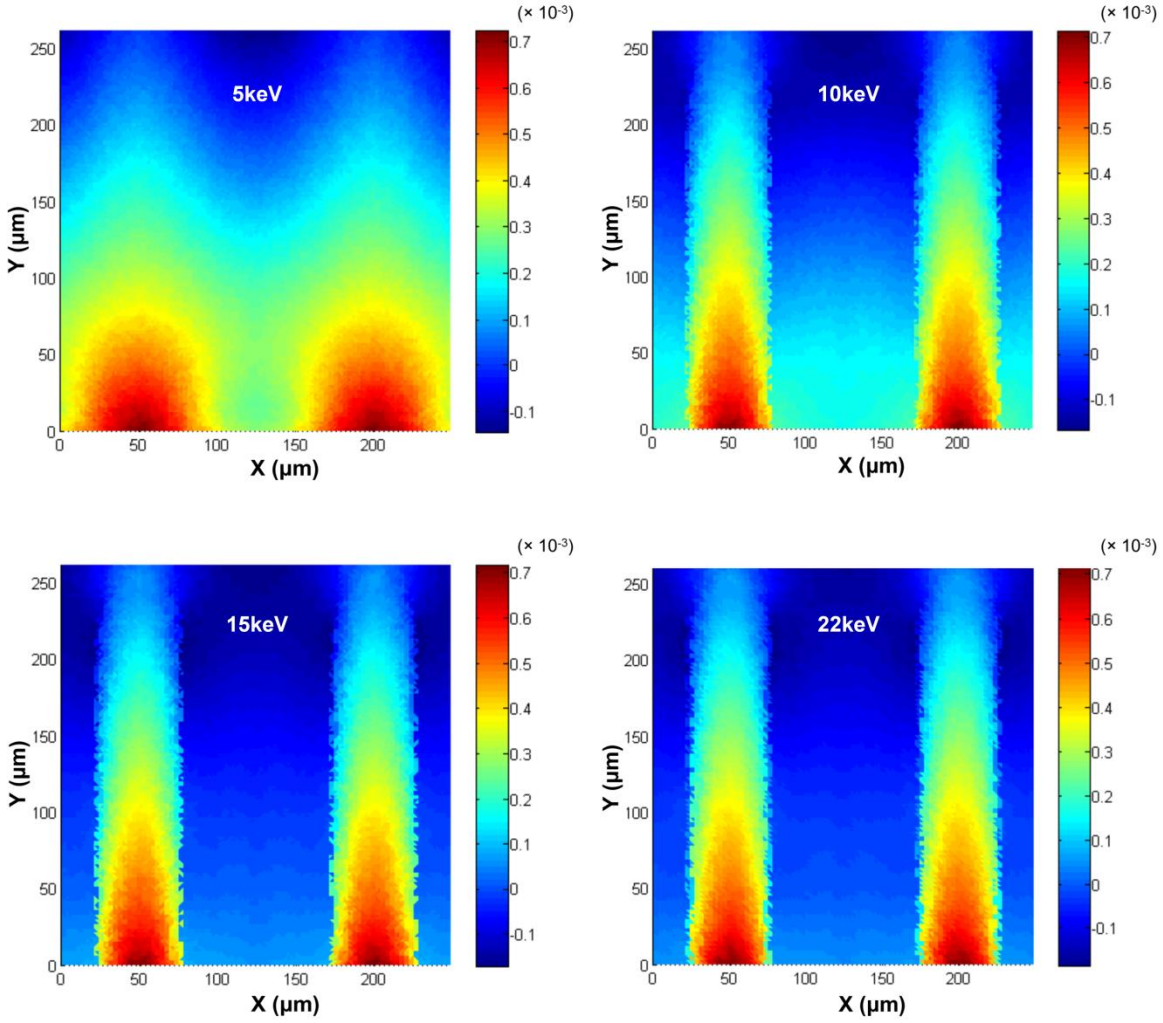


Figure 4.9: Predicted $\varepsilon_{xx}^{'}$ distribution maps of silicon with different monochromatic beam energy (S2)

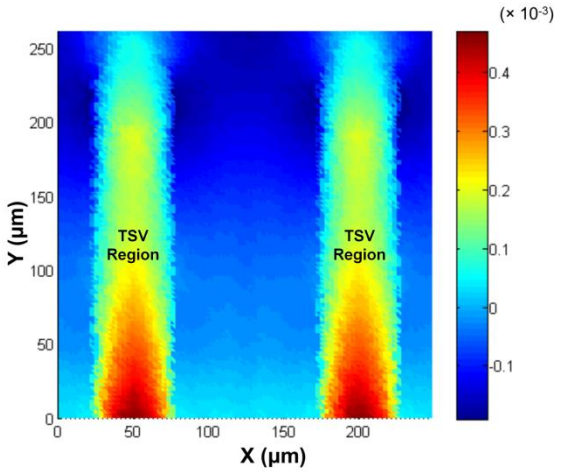


Figure 4.10: Predicted $\varepsilon_{xx}^{'}$ distribution map of silicon with even average method (S2)

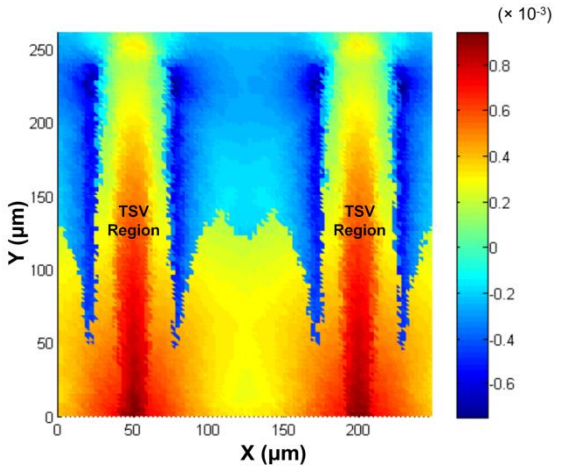


Figure 4.11: Predicted $\varepsilon_{xx}^{'}$ distribution map of silicon with maximum strain method (S2)

In addition, other possible data processing methods are investigated for comparison purpose. One method is an even average along the penetration path ($\varepsilon = mean(\varepsilon_i)$). The results show that the even averaged results change with different chosen averaging depth. Figure 4.10 shows the result with full x-ray penetration depth. As seen, the even average method may be applicable to strain data interpolations for thin film type samples, but is not applicable to the data analysis of thick samples. Another method only picks the strain with the maximum absolute value along each path (

$\varepsilon = sign\{\max[abs(\varepsilon_i)]\} \times \max[abs(\varepsilon_i)]$). As shown in Figure 4.11, this maximum strain method also gives misleading strain distribution.

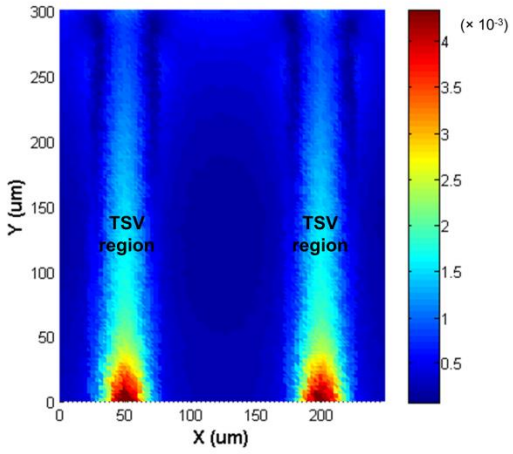
In summary, this proposed a beam intensity based data averaging method successfully predicts the general trend of the strain distribution. Comparisons show that the higher energy end of the applied white beam spectrum dominates the final 2D maps. Also, the even average method and maximum strain method may give misleading results for thick samples.

4.4 Indirect comparison methodology

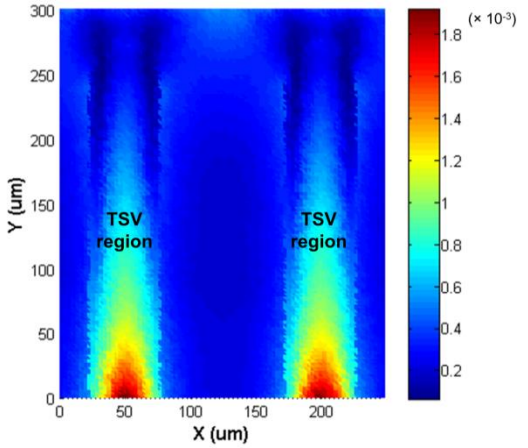
As discussed in Section 4.1, a certain thickness of silicon was kept unpolished in front of the first row of TSVs and called the front silicon thickness as shown in Figure 4.2. The front silicon thickness for each sample was determined by TSV diameter and pitch to preserve the mechanical boundary condition. The front silicon thicknesses affect the measured 2D strain maps in several ways. First, the dimension dependent mechanical boundary conditions of the TSVs near the scanning plane change with varying front silicon thicknesses. Second, the different front silicon thicknesses affect the x-ray penetration depth and consequently affect the captured strain information along the penetration depth, as discussed in Section 4.3.

Taking sample S2 as an example, as shown in Figure 4.12, the models predict that different front silicon thicknesses result in different 2D strain distribution maps and magnitudes, with strains increasing as the front silicon thickness decreases. Moreover, the 3D FEM results in Figure 4.13 show higher strain in the front silicon as the front silicon thickness reduces. In addition, the strain near the front section has larger contribution to the final 2D strain distribution maps. The samples with thicker front silicon have larger contribution from the volume of the lower strained front silicon (Figure 4.13 (c)) and thus

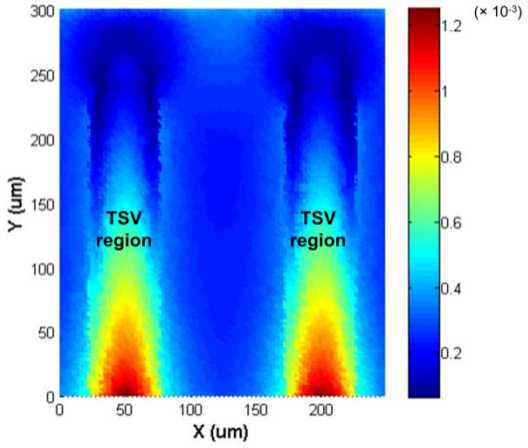
their averaged 2D strain distribution maps show lower strain values, as shown in Figure 4.12 (c). Therefore, it is essential to take the effect of the front silicon thickness into consideration when we use the 2D strain distribution maps obtained from synchrotron XRD measurements in order to realistically compare different TSV designs, in order to avoid front silicon thickness induced artifacts. One example is the comparison of the measured strain maps of sample S1 in Figure 4.15 (a) and sample S2 in Figure 4.5. Direct comparison of their 2D strain distribution maps shows that sample S1 is under higher thermomechanical strain than sample S2. This conclusion is incorrect since sample S2 has larger diameter copper vias diameter than sample S1. Sample S2 is expected to experience larger CTE mismatch induced thermomechanical strains [60], as evidenced by the comparison of Figure 4.13 (c) and Figure 4.16.



(a) 10 μm

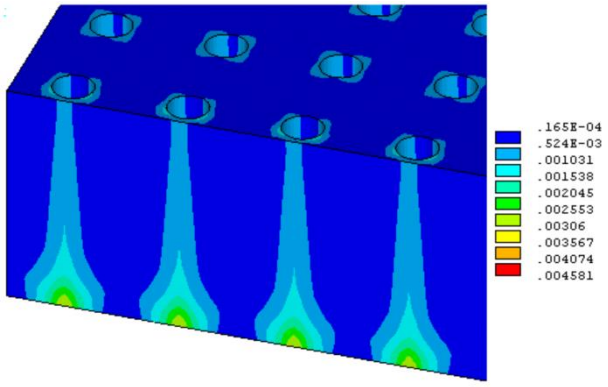


(b) 30 μm

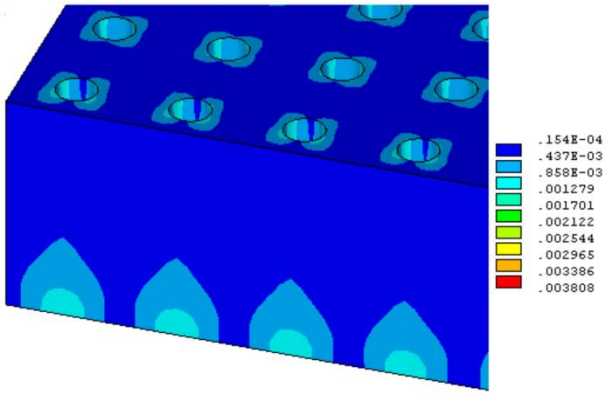


(c) 50 μm

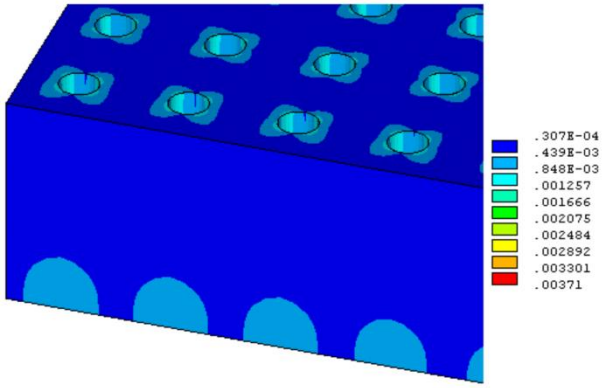
Figure 4.12: Predicted sample S2 2D ε'_{eq} maps with different front silicon thickness at 150 ℃



(a) 10 μm



(b) 30 μm



(c) 50 μm

Figure 4.13: Predicted sample S2 $\varepsilon_{eq}^{'}$ 3D distribution with different front silicon thickness at 150 ℃

To address this issue, an indirect approach is applied by using the measured 2D strain distribution maps to calibrate a 3D finite element analysis (FEA) model (Figure 4.14), and then the calculated strain from the 3D FEA model is used to compare different

TSV designs. To calibrate the 3D FEA models, the aforementioned beam intensity based data averaging method is applied to project the 3D strain distribution from the 3D FEA models onto 2D strain distribution maps. This allows a direct comparison between the measured and the predicted strain data. Figure 4.15 compares the measured strain map with the predicted strain map for sample S1; Figure 4.5 and Figure 4.12 (C) for sample S2; Figure 4.17 for sample S3; Figure 4.18 for sample S4. The comparison shows that the model results generally agree well with the measurement data on strain distribution. The remaining discrepancies are due to the following reasons. First, it is observed that while repeating the measurements on the same sample, a few measured values differed from the modeled values due to the stress history during the high temperature measurements. Second, the finite element model considers an ideal thermal loading case without accounting for the fabrication induced defects and copper grain coarsening during the fabrication. Even with the discrepancies in the some of the strain magnitudes, both of the modeled and measured strain distribution trends matched well for all the four samples, and the trends are useful to identify critical locations in the silicon.

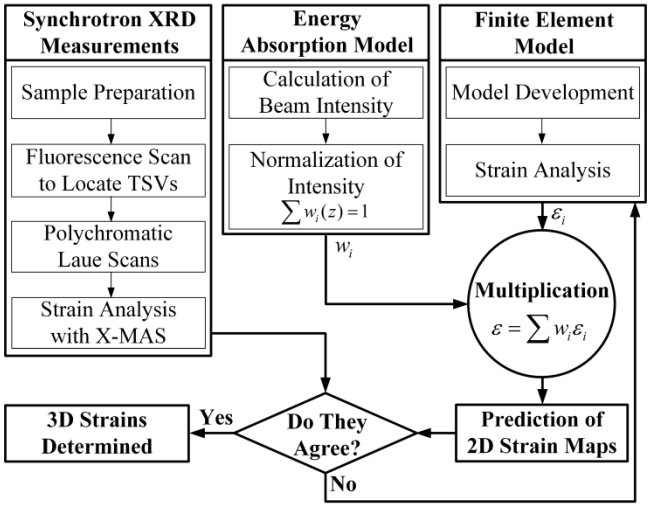


Figure 4.14: Procedure for experimental measurements and analysis

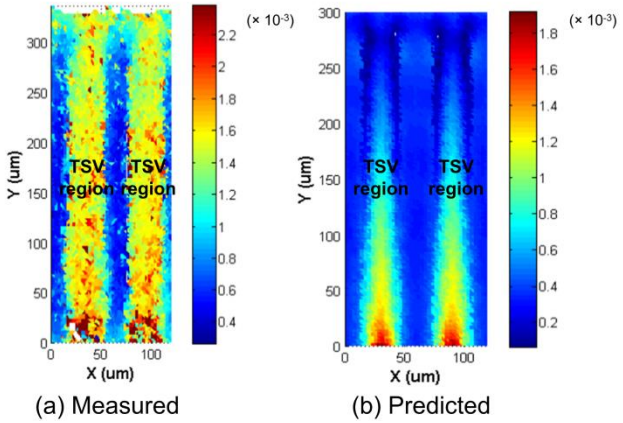


Figure 4.15: Measured and predicted sample S1 2D $\varepsilon_{eq}^{'}$ distribution map of silicon at 150 ℃

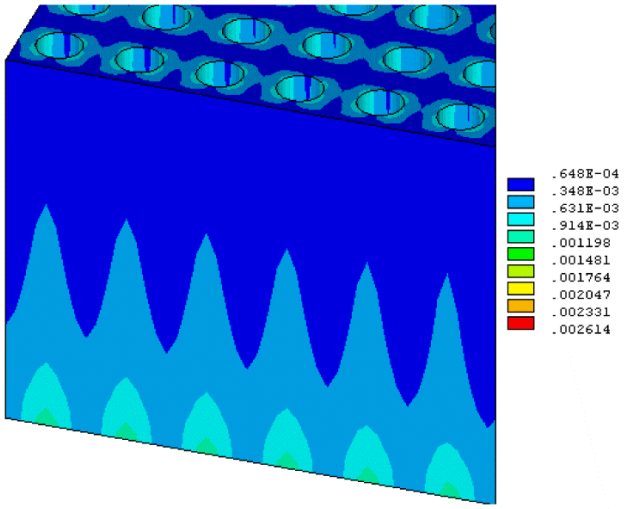
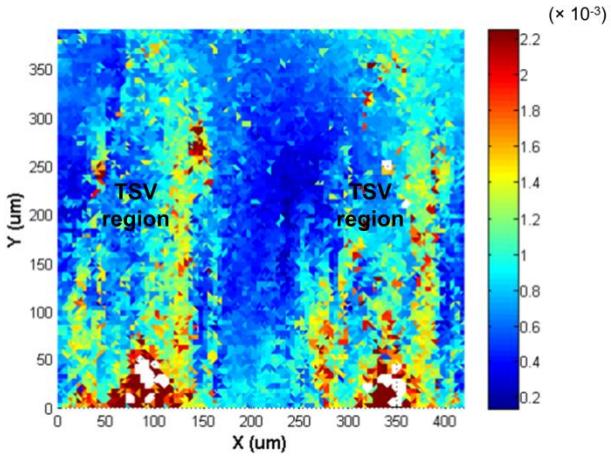
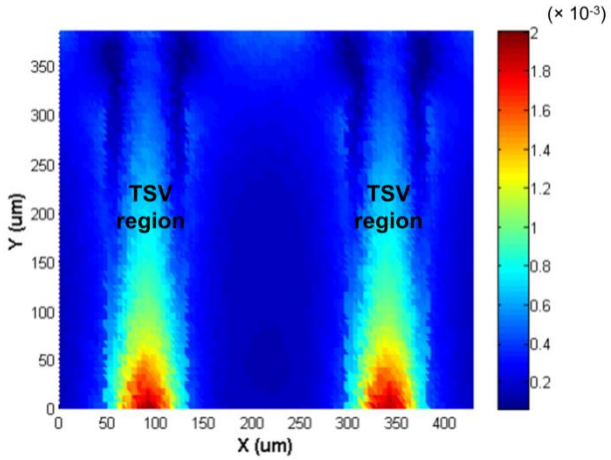


Figure 4.16: Predicted sample S1 3D $\varepsilon_{eq}^{'}$ distribution of silicon at 150 ℃



(a) Measured



(b) Predicted

Figure 4.17: Measured and predicted sample S3 2D ε'_{eq} distribution map of silicon at 150 ℃

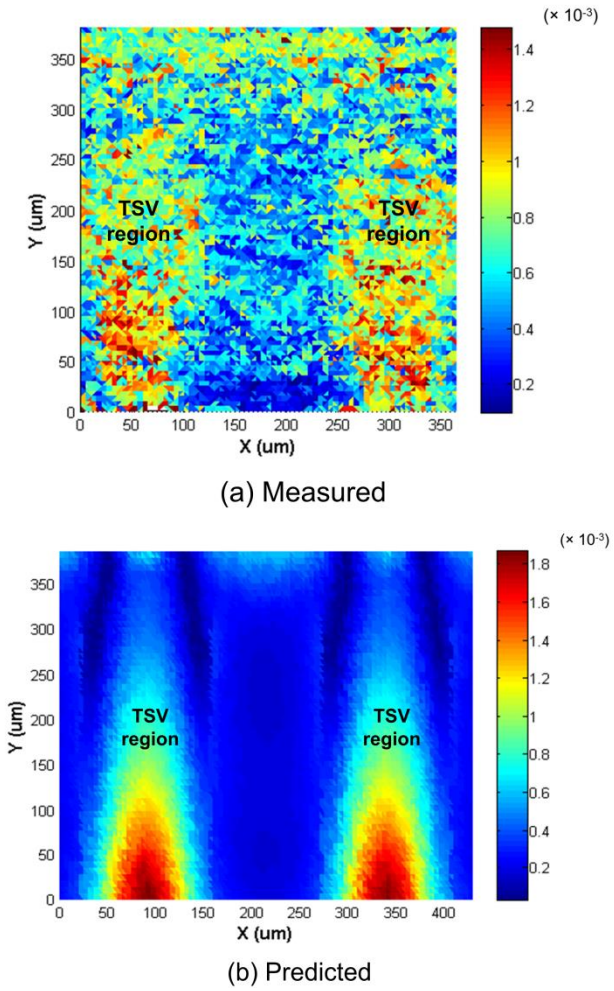


Figure 4.18: Measured and predicted sample S4 2D ε'_{eq} distribution map of silicon at 150 ℃

4.5 Comparison study

4.5.1 Effect of TSV dimensions

To study the effect of TSV dimensions on TSV thermomechanical reliability, samples S1, S2, and S3 are compared. They have different TSV diameter, pitch and height, but the same fabrication process, liner material (silicon dioxide) and liner thickness (1 μm). Since the dominating TSV thermomechanical failure modes are silicon

cracking and copper/liner separation[3], the first principal strain ε_{11} in the silicon and the copper/liner interfacial shear strain are compared. As shown in Figure 4.19 and Figure 4.20, the CTE mismatch between silicon and copper induces high strain near the TSV edges. The strain decreases quickly and then levels off when moving away. Larger copper via diameter generally results in higher strain in the surrounding silicon, thus making the silicon more prone to cracking. The existence of a bottom copper layer causes even higher strain in the silicon near the TSV bottom (path ***C-D*** in Figure 4.2) than near the TSV top (path ***A-B*** in Figure 4.2). To investigate the possibility of interfacial separation at the copper/liner interfaces, the interfacial shear strain ε_{xy} along the TSV side wall of the cross-section (path ***C-A*** in Figure 4.2) are plotted in Figure 4.21. It shows that high interfacial shear strain occurs near the TSV top and bottom, especially near the bottom due to the presence of the bottom copper layer. Similarly, a larger TSV diameter induces higher interfacial shear strain, and consequently is more likely to cause copper/liner separation.

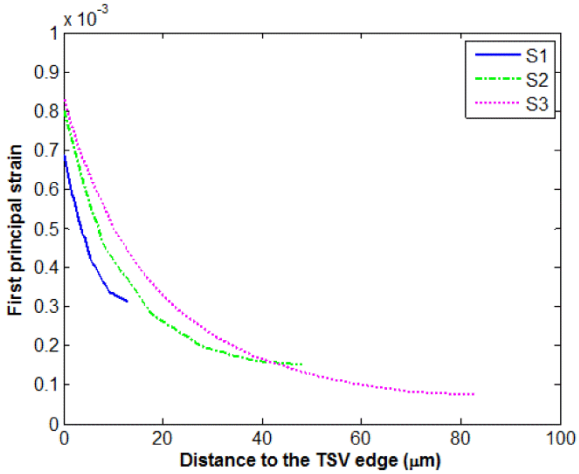


Figure 4.19: Predicted first principal strain ε_{11} of silicon along path *A-B* at 150 ℃

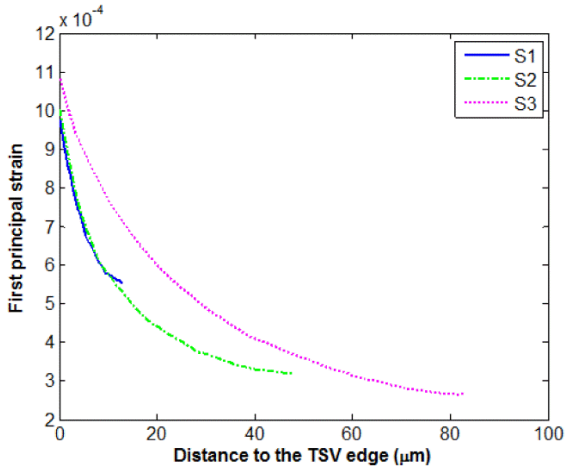


Figure 4.20: Predicted first principal strain ε_{11} of silicon along path *C-D* at 150 ℃

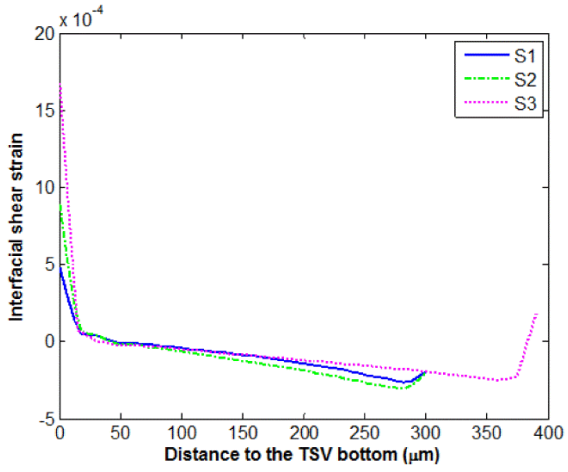


Figure 4.21: Predicted interfacial shear strain ε_{xy} along copper/liner interface *C-A* at 150 ℃

4.5.2 Effect of liner material

To study the effect of liner material on the thermomechanical reliability of TSVs, sample S4 with a thick (25 μm) SU-8 liner is compared to sample S3 with the same copper via dimensions but with a thin (1 μm) silicon dioxide liner. Figure 4.22 shows that the thick SU-8 liner serves as a cushion layer, reducing the thermomechanical force applied to the surrounding silicon as the copper via expands at a high temperature. Also,

as shown in Figure 4.23, the SU-8 liner mitigates the interfacial shear strain, and thus reduces the possibilities of interfacial separation.

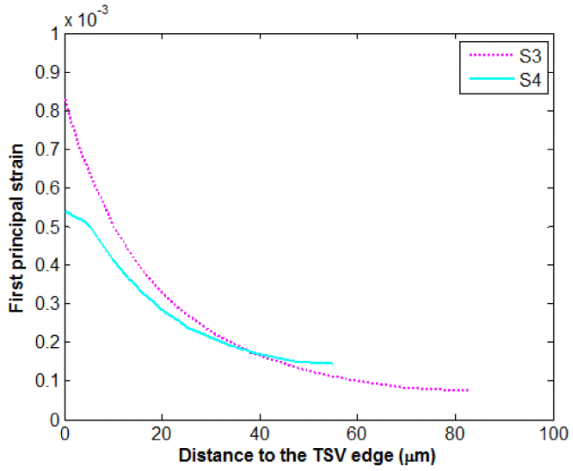


Figure 4.22: Predicted first principal strain ε_{11} of silicon along path *A*-*B* at 150 ℃

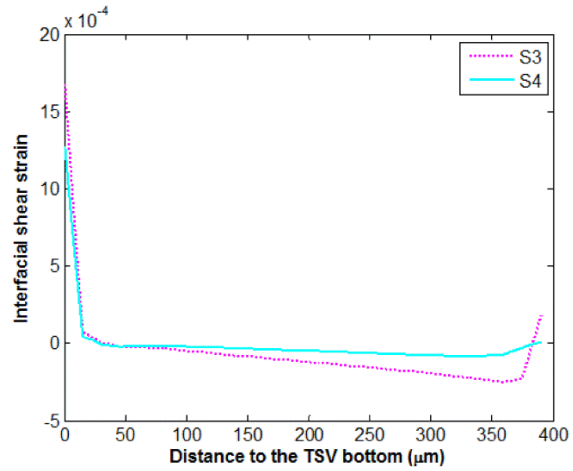


Figure 4.23: Predicted interfacial shear strain ε_{xy} along copper/liner interface *C*-*A* at 150 ℃

In summary, TSVs with different dimensions and liner material have been fabricated and measured at 150 ℃ using synchrotron XRD. To interpret the measured 2D strain distribution maps, a beam intensity based data averaging method has been applied. The analysis shows that a direct comparison of the measured 2D strain distribution maps of different TSV samples may yield results dependent on artifact related to sample

preparation. Thus, an indirect comparison approach based on experimentally calibrated FEA calculations is adopted. Comparisons show that TSVs with larger diameter generally induce higher strain in the silicon as well as at the copper/liner interface, thus have more reliability issues. Moreover, TSVs with thick SU-8 liner experience lower strains compared to TSVs with thin silicon dioxide liner.

CHAPTER 5

WARPAGE STUDY OF 3D INTEGRATED PACKAGES WITH TSVS

As discussed in CHAPTER 1, although 3D packaging integrated with TSVs provides the ultimate packaging solution to meet the demands in the microelectronic industry, there are numerous challenges associated with this relatively new technology, such as yield, assembly, test, and reliability challenges. Significant research effort has been devoted to the development and improvement of the 3D integration techniques. Comparatively, there is a limited body of work focuses on the 3D stacked die package warpage issue during assembly and its effect on package reliability (Figure 5.1). One reason is that 3D stacked dies interconnected with TSVs are still under development stage. Package warpage problem has not caught enough attention and limited prototype samples are available for warpage study. Another reason is that numerical simulation of 3D package is computationally expensive. In 3D packages, the in-plane dimensions are on *mm*-scale. However, the out-of-plane dimensions, TSVs, and microbumps are in *μm*-scale, which tremendously increases the finite-element mesh density to meet the element aspect ratio requirements. Moreover, there are usually hundreds or thousands of TSVs/microbumps in stacked dies. Thus, it remains a challenge to economically and effectively study the 3D package warpage problem.

In this chapter, an analytical model will be formulated to quickly estimate the warpage of stacked dies and the substrate in 3D packages. Also, a simplified smeared finite-element model will be developed and verified with detailed package assembly model. Using the analytical model and the smeared model, different 3D package design parameters will be screened to understand the warpage behavior of 3D stacked die packages.

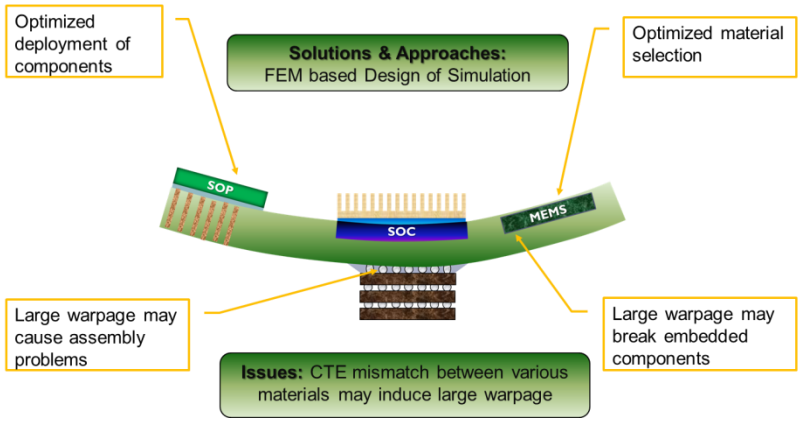


Figure 5.1: Warpage issue of 3D integrated packages

5.1 Analytical approach

To estimate the warpage of the 3D integrated packages, a theoretical approach based on laminate theory [61, 62] has been formulated. In the 3D integrated packages with stacked dies, the in-plane dimensions of each layer are generally in mm level, much larger than the out-of-plane dimensions, which are in μm level. Thus, the layers can be treated as two-dimensional planes under plane stress state. As shown in Figure 5.3,each layer of material in the 3D packages is assumed to be orthotropic, with the stress-strain relationship in the principal material coordinates (*1-2* in Figure 5.3) being

$$\begin{Bmatrix}\sigma_1\\ \sigma_2\\ \tau_{12}\end{Bmatrix}=\begin{bmatrix}Q_{11} & Q_{12} & 0\\ Q_{21} & Q_{22} & 0\\ 0 & 0 & Q_{66}\end{bmatrix}\begin{Bmatrix}\varepsilon_1\\ \varepsilon_2\\ \gamma_{12}\end{Bmatrix}=[Q]\begin{Bmatrix}\varepsilon_1\\ \varepsilon_2\\ \gamma_{12}\end{Bmatrix} \tag{5.1}$$

where

$$Q_{11}=\frac{E_1}{1-\nu_{12}\nu_{21}}$$

$$Q_{12}=Q_{21}=\frac{\nu_{21}E_1}{1-\nu_{12}\nu_{21}}=\frac{\nu_{12}E_2}{1-\nu_{12}\nu_{21}}$$

$$Q_{22}=\frac{E_2}{1-\nu_{12}\nu_{21}}$$

$$Q_{66}=G_{12}$$

Here E_1 and E_2 are moduli in longitudinal and transverse directions, respectively. G_{12} is the in-plane shear modulus. ν_{12} and ν_{21} are the Poisson's ratios.

By transformation, the stress and strain relationship in the *X*-*Y* coordinates is

$$\begin{Bmatrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{Bmatrix} = \begin{bmatrix} \bar{Q}_{11} & \bar{Q}_{12} & \bar{Q}_{16} \\ \bar{Q}_{21} & \bar{Q}_{22} & \bar{Q}_{26} \\ \bar{Q}_{61} & \bar{Q}_{62} & \bar{Q}_{66} \end{bmatrix} \begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \gamma_{xy} \end{Bmatrix} \tag{5.2}$$

where

$$\bar{Q}_{11} = Q_{11}\cos^4\theta + 2\,(Q_{12} + 2Q_{66})\sin^2\theta\cos^2\theta + Q_{22}\,\sin^4\theta$$

$$\bar{Q}_{12} = \bar{Q}_{21} = (Q_{11} + Q_{22} - 4Q_{66})\sin^2\theta\cos^2\theta + Q_{12}\,(\sin^4\theta + \cos^4\theta)$$

$$\bar{Q}_{22} = Q_{11}\sin^4\theta + 2\,(Q_{12} + 2Q_{66})\sin^2\theta\cos^2\theta + Q_{22}\,\cos^4\theta$$

$$\bar{Q}_{16} = \bar{Q}_{61} = (Q_{11} - Q_{12} - 2Q_{66})\sin\theta\cos^3\theta + (Q_{12} - Q_{22} + 2Q_{66})\,\sin^3\theta\cos\theta$$

$$\bar{Q}_{26} = \bar{Q}_{62} = (Q_{11} - Q_{12} - 2Q_{66})\sin^3\theta\cos\theta + (Q_{12} - Q_{22} + 2Q_{66})\sin\theta\cos^3\theta$$

$$\bar{Q}_{66} = (Q_{11} + Q_{22} - 2Q_{12} - 2Q_{66})\sin^2\theta\cos^2\theta + Q_{66}\,(\sin^4\theta + \cos^4\theta)$$

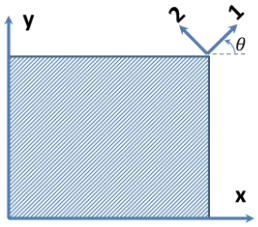


Figure 5.2: Coordinates of a single layer

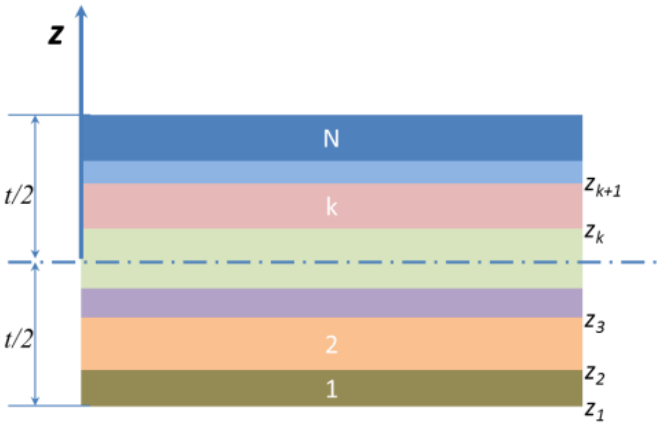


Figure 5.3: Cross-sectional view of multi-layer package structure

Based on the Kirchhoff-Love plate theory [63], in a laminate as shown in Figure 5.4, the strain and stress in layer *k* is given by:

$$\begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \gamma_{xy} \end{Bmatrix} = \begin{Bmatrix} \frac{\partial u_0}{\partial x} \\ \frac{\partial v_0}{\partial y} \\ \frac{\partial u_0}{\partial y} + \frac{\partial v_0}{\partial x} \end{Bmatrix} + z \begin{Bmatrix} -\frac{\partial^2 w}{\partial x^2} \\ -\frac{\partial^2 w}{\partial y^2} \\ -2\frac{\partial^2 w}{\partial xy} \end{Bmatrix} = \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + z \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \tag{5.3}$$

$$\begin{Bmatrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{Bmatrix}_k = [\bar{Q}]_k \begin{Bmatrix} \varepsilon_x \\ \varepsilon_y \\ \gamma_{xy} \end{Bmatrix}_k = [\bar{Q}]_k \left\{ \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + z \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \right\} \tag{5.4}$$

Notice that $[\bar{Q}]_k$ varies from layer to layer.

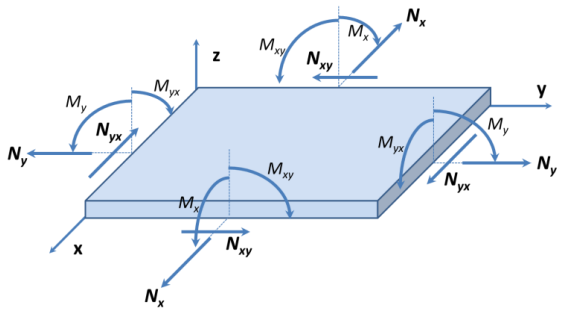


Figure 5.4: Resultant forces and moments of the multi-layer structure

By integrating the stress along the thickness direction of the multi-layer package structure (Figure 5.3), the resultant forces (N_x, N_y, and N_{xy}) and moments (M_x, M_y, and M_{xy}) as shown in Figure 5.4, of the multi-layer structure can be obtained.

$$\begin{Bmatrix} N_x \\ N_y \\ N_{xy} \end{Bmatrix} = \sum_{k=1}^{n} [\bar{Q}]_k \left\{ \int_{z_k}^{z_{k+1}} \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} dz + \int_{z_k}^{z_{k+1}} \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} z dz \right\} \tag{5.5}$$

$$\begin{Bmatrix} M_x \\ M_y \\ M_{xy} \end{Bmatrix} = \sum_{k=1}^{n} [\bar{Q}]_k \left\{ \int_{z_k}^{z_{k+1}} \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} z dz + \int_{z_k}^{z_{k+1}} \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} z^2 dz \right\} \tag{5.6}$$

Since ε_x^0, ε_y^0, γ_{xy}^0, k_x, k_y, and k_{xy} are not functions of *z*, thus

$$\begin{Bmatrix} N_x \\ N_y \\ N_{xy} \end{Bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{16} \\ A_{21} & A_{22} & A_{26} \\ A_{61} & A_{62} & A_{66} \end{bmatrix} \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + \begin{bmatrix} B_{11} & B_{12} & B_{16} \\ B_{21} & B_{22} & B_{26} \\ B_{61} & B_{62} & B_{66} \end{bmatrix} \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \tag{5.7}$$

$$\begin{Bmatrix} M_x \\ M_y \\ M_{xy} \end{Bmatrix} = \begin{bmatrix} B_{11} & B_{12} & B_{16} \\ B_{21} & B_{22} & B_{26} \\ B_{61} & B_{62} & B_{66} \end{bmatrix} \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + \begin{bmatrix} D_{11} & D_{12} & D_{16} \\ D_{21} & D_{22} & D_{26} \\ D_{61} & D_{62} & D_{66} \end{bmatrix} \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \tag{5.8}$$

where

$$A_{ij} = \sum_{k=1}^{n} \left(\bar{Q}_{ij}\right)_k (z_{k+1} - z_k)$$

$$B_{ij} = \frac{1}{2} \sum_{k=1}^{n} \left(\bar{Q}_{ij}\right)_k (z_{k+1}^2 - z_k^2)$$

$$D_{ij} = \frac{1}{3} \sum_{k=1}^{n} \left(\bar{Q}_{ij}\right)_k (z_{k+1}^3 - z_k^3)$$

When a layer is heated or cooled uniformly,

$$\begin{Bmatrix} \varepsilon_1^H \\ \varepsilon_2^H \\ \gamma_{12}^H \end{Bmatrix} = \begin{Bmatrix} \alpha_1 \\ \alpha_2 \\ 0 \end{Bmatrix} \Delta T \tag{5.9}$$

Thus,

$$\begin{Bmatrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{Bmatrix}_k = [\bar{Q}]_k \left\{ \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + z \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} - \begin{Bmatrix} \varepsilon_x^H \\ \varepsilon_y^H \\ \gamma_{xy}^H \end{Bmatrix} \right\} \tag{5.10}$$

For thermal loading only,

$$\begin{Bmatrix} N_x \\ N_y \\ N_{xy} \end{Bmatrix} = \begin{Bmatrix} M_x \\ M_y \\ M_{xy} \end{Bmatrix} = \begin{Bmatrix} 0 \\ 0 \\ 0 \end{Bmatrix} \tag{5.11}$$

Thus,

$$\begin{Bmatrix} N_x^H \\ N_y^H \\ N_{xy}^H \end{Bmatrix} = [A] \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + [B] \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \tag{5.12}$$

$$\begin{Bmatrix} M_x^H \\ M_y^H \\ M_{xy}^H \end{Bmatrix} = [B] \begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \end{Bmatrix} + [D] \begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} \tag{5.13}$$

where

$$\begin{Bmatrix} N_x^H \\ N_y^H \\ N_{xy}^H \end{Bmatrix} = \sum_{k=1}^{n} \left(\bar{Q}_{ij}\right)_k (z_{k+1} - z_k)[T]_k^{-1} \begin{Bmatrix} \alpha_1 \\ \alpha_2 \\ 0 \end{Bmatrix}_k \Delta T_k$$

$$\begin{Bmatrix} M_x^H \\ M_y^H \\ M_{xy}^H \end{Bmatrix} = \frac{1}{2} \sum_{k=1}^{n} \left(\bar{Q}_{ij}\right)_k (z_{k+1}^2 - z_k^2)[T]_k^{-1} \begin{Bmatrix} \alpha_1 \\ \alpha_2 \\ 0 \end{Bmatrix}_k \Delta T_k$$

Notice that ΔT_k can vary from layer to layer to consider different material stress-free temperatures in the 3D packages.

Solve above equations for mid-plane strains and curvatures

$$\begin{Bmatrix} \varepsilon_x^0 \\ \varepsilon_y^0 \\ \gamma_{xy}^0 \\ k_x \\ k_y \\ k_{xy} \end{Bmatrix} = \begin{bmatrix} A & B \\ B & D \end{bmatrix}^{-1} \begin{Bmatrix} N_x^H \\ N_y^H \\ N_{xy}^H \\ M_x^H \\ M_y^H \\ M_{xy}^H \end{Bmatrix} \tag{5.14}$$

where *A*, *B*, *C*, and *D* are matrixes in Equations (7) and (8).

Considering a laminate (size: $a \times b$) sitting on the plane z = 0 plane, at least three corner points should on the plane. Thus, we can set the boundary conditions as: $(0,0) = 0$, $w(a,0) = 0$, and $w(0,b) = 0$.

From above laminate analysis, we know the curvature and displacement relationship

$$\begin{Bmatrix} k_x \\ k_y \\ k_{xy} \end{Bmatrix} = \begin{Bmatrix} -\frac{\partial^2 w}{\partial x^2} \\ -\frac{\partial^2 w}{\partial y^2} \\ -2\frac{\partial^2 w}{\partial xy} \end{Bmatrix} \tag{5.15}$$

Solve above differential equations by considering the boundary conditions, we can get the warpage of the mid-plane as a function of *x* and *y*

$$w(x,y) = -\frac{1}{2}k_x x^2 - \frac{1}{2}k_y y^2 - \frac{1}{2}k_{xy} xy + \frac{1}{2}k_x ax + \frac{1}{2}k_y by \tag{5.16}$$

5.2 Numerical modeling

5.2.1 Assembly process modeling

To simulate the assembly process of the 3D integrated package with stacked dies as shown in Figure 5.5, sequential three-dimensional finite-element (FE) models are built. Due to symmetry, one quarter of the package is modeled, and symmetric boundary conditions are applied on the symmetric plane, which is shown in Figure 5.6. One node at the center of the bottom die is rigidly held to prevent rigid body motion of the package. It should be pointed out that the TSVs are connected to the solder bump through re-distribution layers, and in the current model, such re-distribution layers are not modeled for the warpage study.

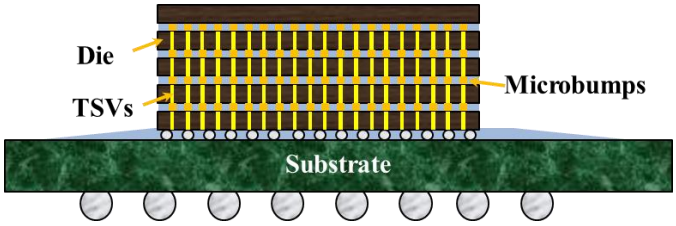


Figure 5.5: 3D package with stacked dies

The focus of this model is to understand the warpage evolution during the assembly process. Therefore, the solder bumps, micro bumps, and TSVs are simplified as cylinders, as shown in Figure 5.7.

To capture the process-induced warpage of the package, the thermal profile of the assembly process is applied on the package in a sequential basis. Figure 5.8 shows an example 3D integrated package with a 2-die stack. This case starts with a die 1. Die 2 with micro-bumps is reflow-attached on the top pads of the die 1 and with no flow underfill (NUF). The two-die stack is then reflow-attached on the top side of the substrate and then underfilled. Then the flip-chip solder bumps, and the substrate are activated as stress-free at solder melting temperature of 220 ℃, and subsequently, the underfill is

activated as stress-free at its curing temperature of 165 ℃. Such a sequential activation is done through ANSYS® Ver. 14.5 element birth-and-death approach.

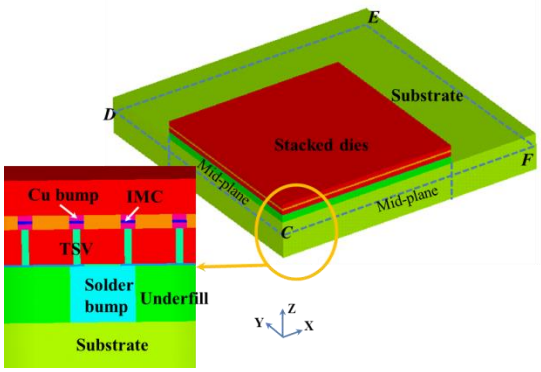


Figure 5.6: Quarter symmetric FEM model of the 3D package with two stacked dies

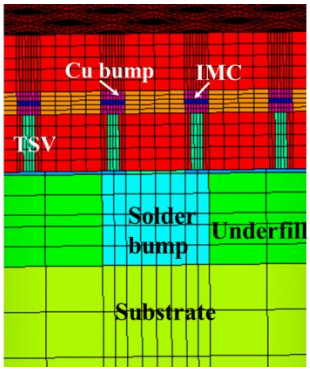


Figure 5.7: Cross-sectional view of the finite-element mesh

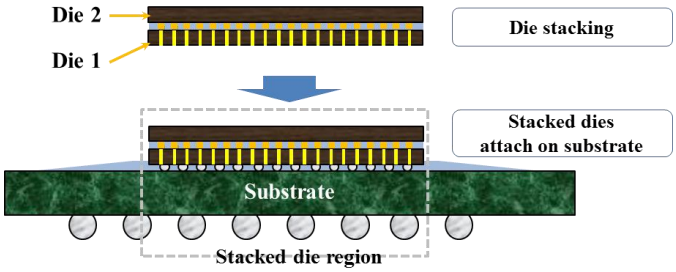


Figure 5.8: Example assembly process of 2-die stack

The dimensions of the assembly model are listed in Table 5.1. As seen in Table 5.1, a very small 2-die stack package is modeled due to the limitation of the computing power. Even this small quarter model has 1600 TSVs/microbumps, and another 100 flip-chip solder bumps.

Table 5.2 and Table 5.3 provide the thermo-mechanical properties of materials used in the package, which is provided by the manufacturer or found in open literature.

Table 5.1: Package dimensions

Description	**Dimension (mm)**
Substrate size	6×6×0.4
Die size	4×4×0.05
Diameter of TSVs in stacked dies	0.01
Diameter of flip-chip solder bumps	0.09
Pitch of TSVs/Microbumps in stacked dies	0.05
Pitch of flip-chip solder bumps	0.20
Microbump height in-between dies	0.02
Flip-chip solder bump height	0.08

Table 5.2: Material properties

	E (GPa)	**υ**	**CTE (ppm/℃)**	**T_g (℃)**
Cu[58]	70	0.3	17.3	N/A
Si[17]	130.91	0.28	2.8	N/A
IMC[64]	108.3	0.299	19	N/A
Solder[65]	38.7-0.176T	0.35	25	N/A
Substrate[38]	29@25 ℃ 18@250 ℃	0.2	XY: 11 Z:22 XY: 6 Z:115	180
Flip-chip underfill[38]	5.8@25 ℃ 1.2@250 ℃	0.3	α_1: 31.1 α_2: 63.5	88
Die to die underfill[38]	2.5@25 ℃ 0.056@250 ℃	0.39	α_1: 59.0 α_2: 159.0	125

Table 5.3:Anand model constants for Sn3.0Ag0.5Cu [66]

	Sn3.0Ag0.5Cu
Initial value of s (s_0)	2.15 MPa
Activation energy (Q/R)	9970 K
Pre-exponential factor (A)	17.994 s^{-1}
Stress multiplier (ξ)	0.35
Strain rate sensitivity of stress (m)	0.153
Hardening coefficient (h_0)	1525.98 MPa
Coefficient for deformation resistance saturation value ($\hat{s}$)	2.536 MPa
Strain rate sensitivity of saturation value (n)	0.028
Strain rate sensitivity of hardening coefficient (a)	1.69

5.2.2 Simplified smeared modeling

The 2-die stack package quarter model (Figure 5.6), although with a coarse mesh (Figure 5.7), still has 3,487,600 elements, which takes a 16-core server 38 hours to solve. Case study with three or more dies stacked pacakges or larger size packages will be computationally prohibitive. Thus, it is imperative to further simplify the FE models. Since the focus of this paper is to perform a warpage analysis of the stacked die package, smeared properties are applied in three regions, including: 1) the solder bump and underfill of the flip chip on organic substrate; 2) the microbumps and underfill in-between the dies; and 3) the TSVs surrounded by silicon. The smeared properties can be obtained by creating a representative unit cell that contains detailed structures. Take microbump region in-between dies as an example, as shown in Figure 5.9, copper pillar, IMC, dielectric, and underfill geometries and their properties are modeled in detail. The unit cell is then subjected to mechanical loading in various normal and shear directions to get the effective tensile and shear modulus values in various directions. Similarly, the unit cell is subjected to thermal excursions to be able to determine the effective coefficient of thermal expansion in different directions. There are a number of publications that provide details on the determination of smeared properties using the finite-element technique [42]. Thus, the aforementioned three regions can be modeled thermo-elastic and orthotropic layers, which reduces the model element number to 14,400 and brings computational time down to less than 10 minutes. However, with the flip-chip being modeled as one layer of orthotropic material, flip-chip solder reflow and underfilling process cannot be simulated sequentially. Thus, the reflow and underfilling process are simulated in one step by activating the smeared solder and underfill region as stress free at the underfill curing temperature of 165 ℃, however setting the die stack and substrate stress free at solder melting temperature of 220 ℃. The validity of the

simplified smeared modeling approach for warpage study will be discussed in the followed section.

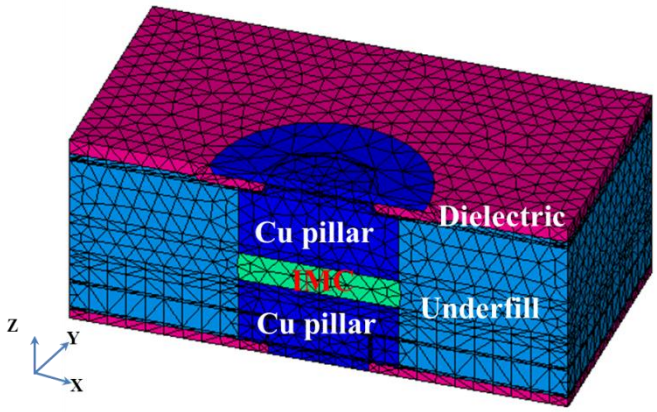


Figure 5.9: Cross-sectional view of the cell model of the microbump region in-between the dies

5.3 Correlation of different models

In this section, three modeling approaches proposed in previous sections are applied to analyze the 2-die stack package. Comparison of the results of different modeling approaches will be carried out by comparing the warpage values of different components, where the warpage value of each component is defined as the peak to valley difference of the out-of-plane displacement.

As discussed above, the analytical model can only predict the warpage of the mid-plane in the stacked die region (Figure 5.6 and Figure 5.8). However, as seen in Figure 5.10, for this package, the peaks invariably occur at the package center, and the valleys are at the outermost corners. Therefore, the substrate warpage can be approximated by linearly extrapolating along a tangent plane at one corner of the warped mid-plane. Figure 5.12 shows one tangent plane at corner (*x=0, y=0*), the function of which can be derived as

$$f(x,y) = -\frac{1}{2}k_x ax - \frac{1}{2}k_y by \tag{5.17}$$

Then the warpage of the substrate can be approximated with Equations (5.16) and (5.17) as

$$w_{sub} = w\left(\frac{l_{die}}{2}, \frac{l_{die}}{2}\right) - f\left(\frac{l_{die}}{2} - \frac{l_{sub}}{2}, \frac{l_{die}}{2} - \frac{l_{sub}}{2}\right) \tag{5.18}$$

where l_{die} and l_{sub} are the in-plane edge length of die and substrate respectively.

It should be pointed out that since the package warpage are all in dome shape for this study (Figure 5.10 and Figure 5.11), the dome shape warpage values are defined as positive. In addition, to make the stacked die region warpage comparable, the mid-plane warpage contours of the stacked die region are extracted out from FE models (Figure 5.11 (a), (b)).

As discussed above, all the three models predict very similar dome shape of the package at 25 ℃. Component warpage values list in Table 5.4 also show very good match, except the analytical model overestimate the substrate warpage about 10% due to the liner extrapolation approach discussed above.

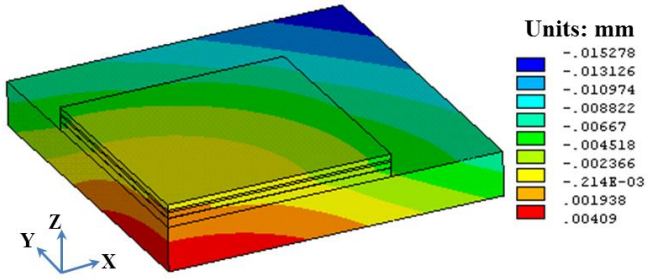


Figure 5.10 (a): Final warpage contours of the assembly model at 25 ℃

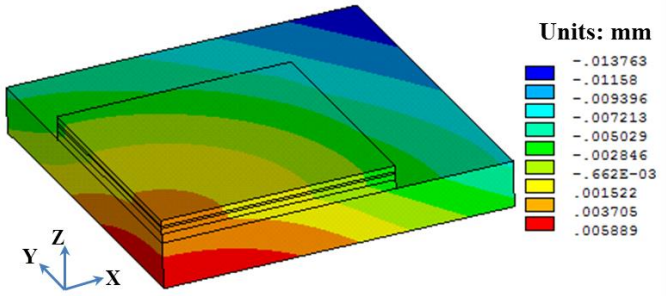


Figure 5.10 (b): Final warpage contours of the smeared model at 25 ℃

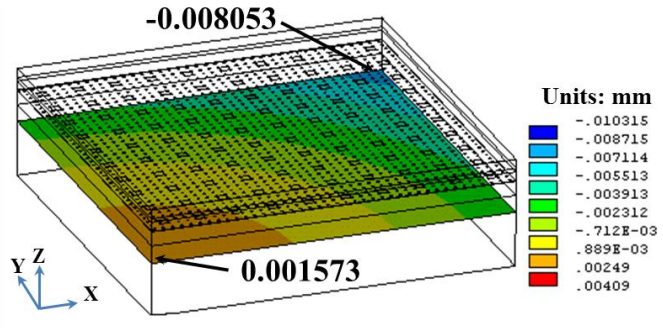


Figure 5.11 (a): Stacked die region mid-plane warpage contours of the assembly model at 25 ℃

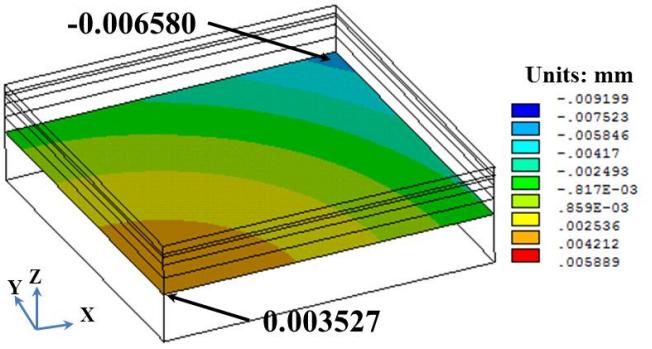


Figure 5.11 (b): Stacked die region mid-plane warpage contours of the smeared model at 25 ℃

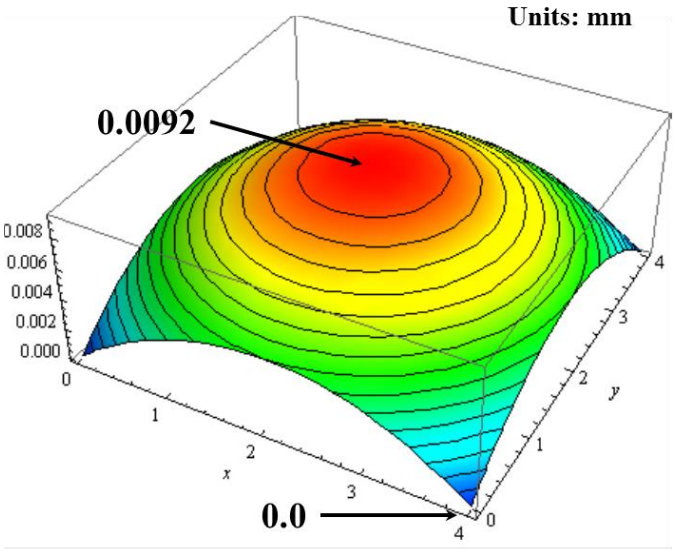


Figure 5.11 (c): Stacked die region mid-plane warpage contours from the analytical model at 25 ℃

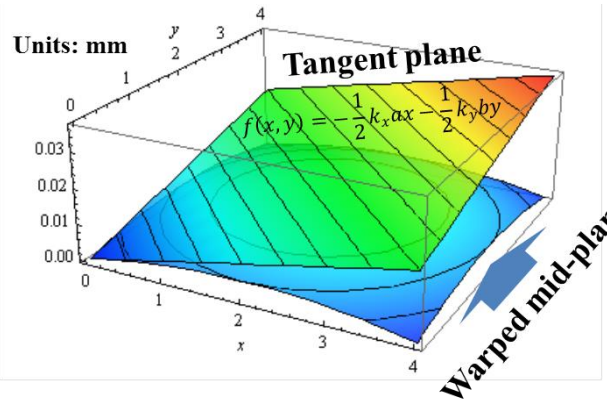


Figure 5.12: The tangent plane of warped mid-plane

Table 5.4: Warpage values of different models

	Substrate warpage (μm)	**Stack die region mid-plane warpage (μm)**
Assembly model	16.5	9.6
Smeared model	16.8	10.1
Analytical model	18.4	9.2

Aforementioned models used isotropic silicon material properties. However, silicon is a single crystal material. There is a concern whether using isotropic material properties is appropriate for warpage study. Thus, another smeared model with the same geometry but using (100) silicon orthotropic material properties [67] has been applied. As shown in Figure 5.13, model with orthotropic silicon material properties predicts the same warpage shape as model with isotropic silicon material properties (Figure 5.10 (b)). The predicted warpage values of the substrate and mid-plane of the stacked dies region are 17.2 μm and 10.3 μm respectively, which are very close to the values listed in Table 5.4. Therefore, temperature-dependent isotropic silicon material properties, which are easier to be obtained, are applicable for warpage study and will be used for the following study.

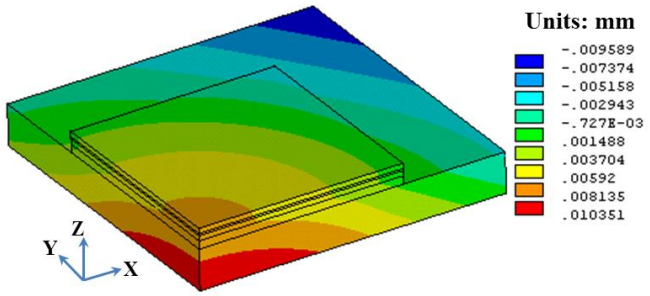


Figure 5.13: Final warpage contours of the smeared model with orthotropic silicon material properties at 25 ℃

5.4 Warpage study of single-sided 3D packages

The comparison study in previous section indicates that all the models agree well with each other on the package warpage analysis. Thus, the analytical model and simplified smeared model will be used for the following package parametric study since they are much more time efficient.

5.4.3 Effect of the stacked dies

A small package is used in above comparison study due to the limitation of computing power for the detailed assembly model. In this section, a package with larger substrate (35×35 mm) will be used. The dimensions of other components will be the same as given in Table 5.1, except the die size, the number of stacked dies, and the substrate thickness.

To study the effect of the die size on package warpage, packages with 5 dies stacked on top of the substrate have been analyzed by changing the die size from 5×5 mm to 25×25 mm. Figure 5.14 shows the warpage of the stacked die region and the warpage of the substrate. It shows that they invariably increase with larger dies. This is due to the fact that larger dies result in higher silicon volume available for the CTE mismatch

between silicon dies and the organic substrate, thus, induce larger warpage of both the stacked die region and the substrate.

The effect of the number of stacked dies on package warpage has been studied by using the same substrate (35×35×1 mm) but changing the number of dies stacked (each die: 20×20×0.05 mm) on top of it. As seen in Figure 5.15, that the substrate and stacked die region warpage shows similar trend as the number of stacked dies increases from 2 to 20, whereas $t_{die-stack}/t_{substrate}$ ratio increases from 0.2 to 1.46. Both substrate and stacked die region warpage reach maximum when the ratio is around 0.3.

The effect of the substrate thickness is analyzed by keeping the substrate size being 35×35 mm and using the same 10 die-stack (each die: 20×20×0.05 mm). Figure 5.16 shows that as the substrate thickness decreases from 1.5 mm to 0.4 mm, whereas the die-stack to substrate aspect ratio increases from 0.45 to 1.7, the substrate and stacked die region warpage also increases then levels off when the aspect ratio reaches 1.4.

Above analysis indicates that the stacked die packages behave similar as the traditional one die flip-chip package studied in Park's study [68]. Further analysis reveals that this is because the smeared effective in-plane thermomechanical properties of the stacked dies, which dominate CTE induced package warpage [42, 68], are very close to the material properties of silicon (Table 5.2). Take room temperature as an example, the effective tensile moduli are 106.81 GPa, 106.81 GPa, and 47.58 GPa in *X*, *Y*, and *Z* directions. The effective shear moduli are 29.77 GPa, 27.72 GPa and 7.99 GPa in the *XY*, *YZ*, and *ZX* planes. The effective CTE in *X*, *Y*, and *Z* directions are 3.69 ppm/℃, 3.69 ppm/℃, and 13.35 ppm/℃ respectively. As seen, the in-plane thermomechanical properties are very close to these of silicon (Table 5.2). Thus, if die-on-die stacking process is not considered, 3D stacked die package can be approximated as one die flip-chip package for warpage study, ideally above effective properties should be used for stacked die region.

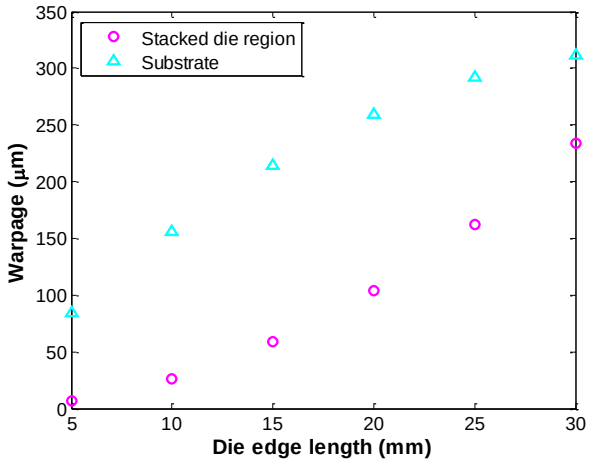


Figure 5.14: Effect of die stack in-plane edge length

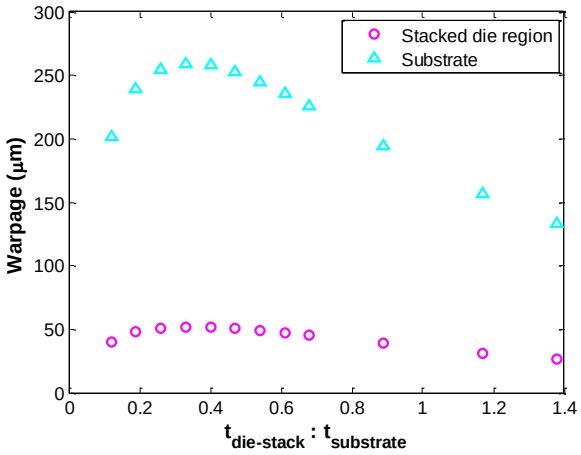


Figure 5.15: Effect of the number of stacked dies (constant substrate thickness)

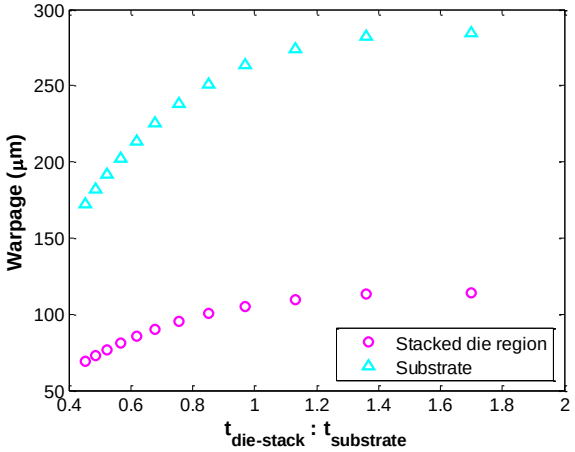
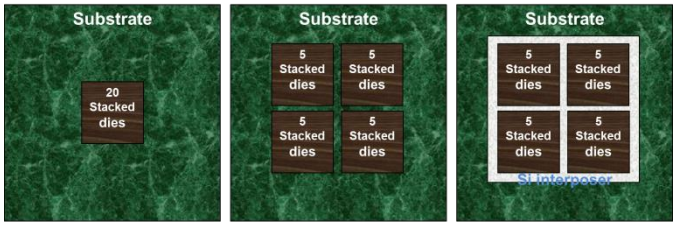


Figure 5.16: Effect of substrate thickness (constant die stack thickness)

5.4.4 Effect of the package layout

To study the effect of different die layout designs on package warpage, the analytical model cannot be applied. Thus the simplified smeared model is used. Three types of package layout are proposed for comparison. As seen in Figure 5.17(a), Case 1 has 20 dies (each die: 10×10×0.05 mm) stacked directly on top of an organic substrate (35×35×1 mm). In Case 2, the 20 dies are divided into 4 stacks, with each stack having 5 stacked dies (Figure 5.17 (b)). Case 3, as shown in Figure 5.17 (c), is similar to Case 2, except the stacked dies are attached to a silicon interposer (23×23×0.1 mm), which connects to the organic substrate.



(a) Case 1 (b) Case 2 (c) Case 3

Figure 5.17: Different package layout

Table 5.5: Warpage and stress results of different design

	Substrate Warpage (μm)	Top die warpage (μm)	Top die MAX 1st principal stress (MPa)	Flip-chip region MAX von Mises stress (MPa)
Case 1	62.94	19.23	55.44	172.50
Case 2	206.96	97.54	20.18	196.61
Case 3	243.26	116.74	9.50	150.27

It is seen from Table 5.5 that Case 1 has the smallest warpage of the top die and the substrate after assembly. However, stacking 20 dies creates a very stiff stacked die structure, constraining package warpage, thus causing high stress on the flip-chip joints connecting stacked dies with the organic substrate. Dividing the dies into 4 stacks (Case 2) lessens the stiffening effect as that in Case 1. However it causes high warpage due to lower stiffness in each stack and also 4 times larger area on the substrate. Inserting a

silicon interposer in between the die stack and the substrate (Case 3) mitigates the reliability issue in the flip-chip interconnecting region and on dies. However, larger size and higher volume of silicon on top of substrate also cause high warpage in the package, which may raise some assembly concerns.

5.5 Warpage study of double-sided flip-chip assembly with a stiffener ring

In this section, another 3D package scheme is presented. The schematic of this 3D system is shown in Figure 5.18 and one of the assembled test pacakges is shown in Figure 5.19. In this configuration, a logic controller chip is attached to the top of the substrate and a memory controller with its associated TSV dynamic random-access memory (DRAM) stack are attached to the bottom of the substrate. Various advanced packaging technologies are employed to achieve this 3D stacked system. The advanced packaging technologies include TSVs, wafer-level re-distribution layers (RDL), and a build-up laminate substrate. With this architecture, the total memory BW of this 3D package can reach 256 GB/s.

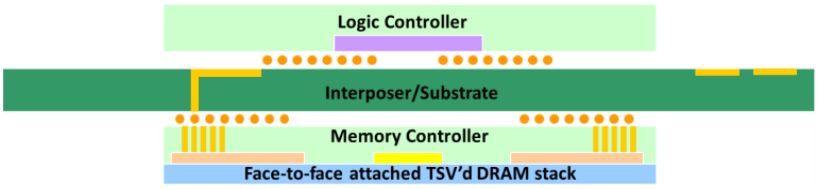


Figure 5.18: Double-sided 3D package illustration

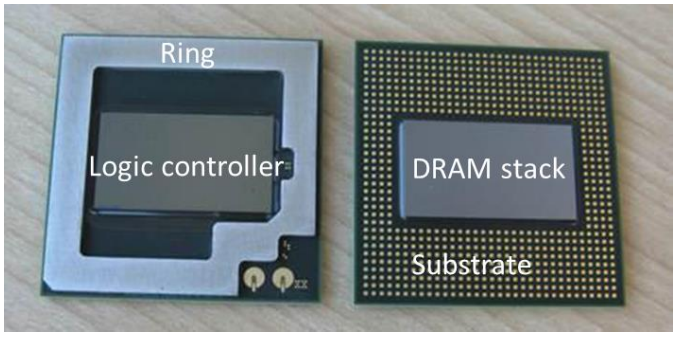


Figure 5.19: Assembled double-sided package with austenitic stainless steel ring

In this 3D package, the laminate substrate creates thermal isolation between the powerful logic chip and the DRAM stack. In addition, the top logic chip can be cooled with a fan and heat sink and the less power-consuming DRAM stack will be cooled through the PCB; details are given in Section 5.5.5. The real challenge for this configuration is the assembly where flip-chip attachment is required on both sides of the laminate substrate. The substrate warpage after the flip-chip attachments is a concern. This work addresses this concern using both modeling prediction and experimental validation, and optimizes the assembly sequence to minimize the warpage through the double sided flip-chip attachments.

5.5.5 Prototype assembly flow and test considerations

The package concept discussed above and shown in Figure 5.19 has been separated into a top logic (controller) device and a bottom memory controller with attached DRAM stack. This system requires a two-sided, flip-chip reflow assembly process. Figure 5.20 and Figure 5.21 show the overall physical configurations of this system. As shown in Figure 5.20, provisions have been made for early prototype probing test and thermal characterization. The modeling work, detailed in Section 5.5.6, indicates that the laminate substrate warpage induced from the assembly solder reflow and LGA socket loading processes present challenges.

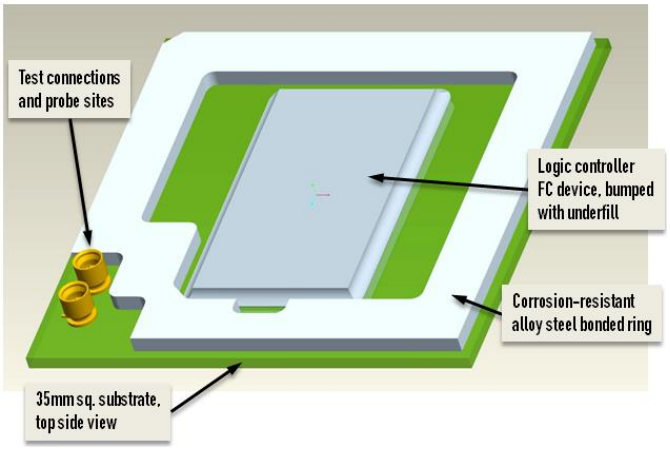


Figure 5.20: Top side view of assembly showing logic controller device, stiffener ring, and prototype test connections

Based on the modeling work, the initial prototype assembly flow includes bonding a corrosion-resistant alloy steel ring to the top of the build-up substrate (Figure 5.20). This ring acts as a stiffener during the assembly process. The memory controller and DRAM stack device will then be flip chip (FC) assembled to permit testing of the 3D DRAM stack. Tin-lead eutectic solder alloy will be used for the prototypes to reduce process temperatures. The tested package would then undergo a second reflow process to attach the pre-tested logic controller device (Figure 5.20).

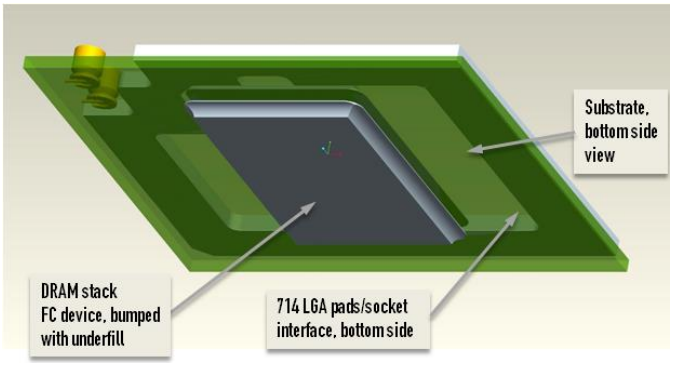


Figure 5.21: Bottom side view of assembly showing the DRAM stack device with the 714 land grid array (LGA) pad interface

Figure 5.22 and Figure 5.23 show the spatial configuration of the logic and memory packaged devices in relation to the system, socket, and PCB. The entire device is mounted in a 35 mm, 714 pad LGA socket assembly. The design permits top and bottom side access for both probing and mounting of the thermal solutions. Simulations also indicate substrate deflection could be induced by the LGA socket. To mitigate connectivity and test challenges, a bolster structure is mounted to the back of the PCB assembly to balance forces from both the socket and thermal solutions.

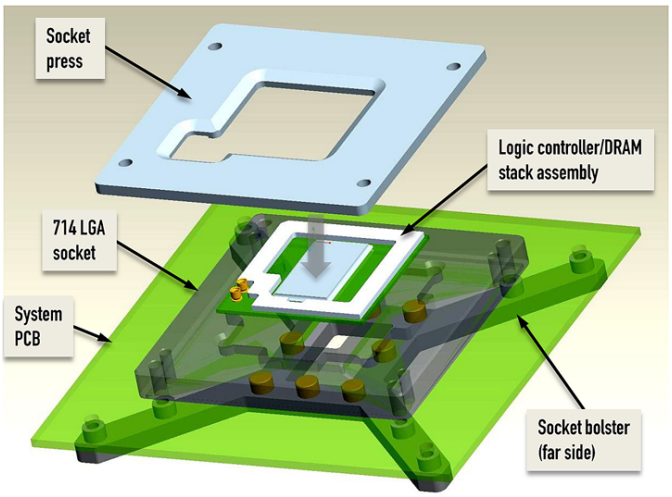


Figure 5.22: Top view of device, test PCB, and socket assembly

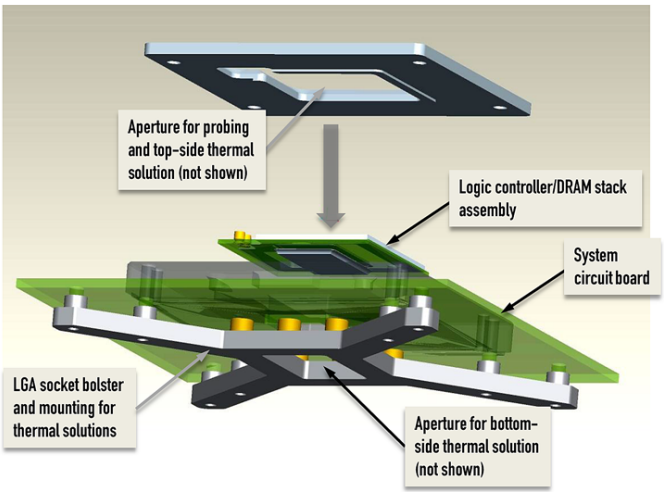


Figure 5.23: Bottom view of device, test PCB, and socket assembly

5.5.6 Assembly process modeling

To simulate the assembly process of the double-sided flip chip system discussed above, sequential three-dimensional Finite Element (FE) models are built. Due to near-planar symmetry, as a first approximation, one quarter of the package is modeled and symmetric boundary conditions are applied on the inner surfaces (*XY* and *YZ* planes), which is shown in Figure 5.24. One node at the coordinate origin is rigidly held to prevent rigid body motion of the package.

The main focus of this model is to understand the substrate, DRAM stack and logic controller warpage evolution during the assembly process. Therefore, the solder bumps are modeled as cubic blocks, as shown in Figure 5.25. Also, the memory stack and direct attached DRAM-interface, shown in Figure 5.18 and Figure 5.19, are simplified as one single silicon chip based on previous finding in 5.4. For the substrate, two types of modeling approaches have been applied. The first approach is to model the substrate layer by layer in detail using temperature-dependent elastic material properties. In this approach, layered structural version of ANSYS® Ver. 14 SOLID185 is used to model the build-up layers of the substrate. As the build-up layers have much higher in-plane dimensions compared to out-of-plane or thickness direction, the layered solid elements will be able to keep the aspect ratio within acceptable limits. At the same time, the elements can also capture the warpage of the substrate structure. A second approach is to model the substrate as one single smeared material with experimentally-characterized temperature-dependent elastic and viscoelastic properties. The layered elastic model uses temperature-dependent elastic properties for all materials except solder which is modeled as viscoplastic. The smeared viscoelastic model uses smeared properties of the substrate and models the underfill and the substrate as viscoelastic. These viscoelastic properties are experimentally characterized, as discussed later.

To capture the process-induced warpage of the package assembly, the thermal profile of the assembly process is applied on the package in a sequential basis. Figure 5.26 shows an example for a Ring middle "Ring mid" case. This case attaches the stiffener ring in the middle of the assembly process between the logic and memory controller assembly steps. This "ring mid" case starts with a bare substrate, the DRAM stack is reflowed to the bottom side and then underfill is added. The ring attachment follows on the top side of the substrate and then the logic controller is attached on the same side of substrate as the ring. In this simulation, the substrate, DRAM stack and solder bumps are first activated as stress-free at a solder melting temperature of 183 ℃, and subsequently, the underfill is activated as stress-free at its curing temperature of 165 ℃. On the other side of the substrate, the ring and the seal band are activated as stress-free at the seal band curing temperature of 150 ℃. Thereafter, the logic controller and its solder bumps are activated as stress-free at solder melting temperature of 183 ℃ followed by underfill activation as stress-free at its curing temperature of 165 ℃. Such a sequential activation is done through ANSYS® element birth-and-death approach.

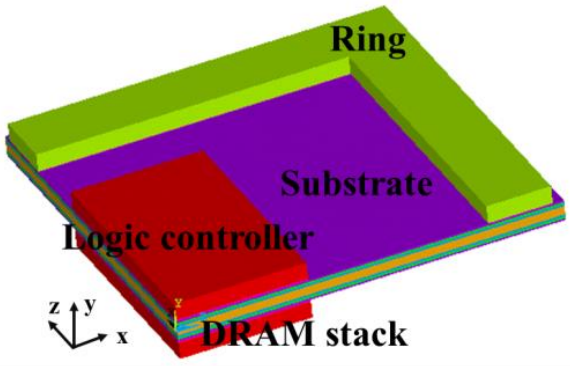


Figure 5.24: Quarter-symmetric FEM model of the double-sided flip-chip package

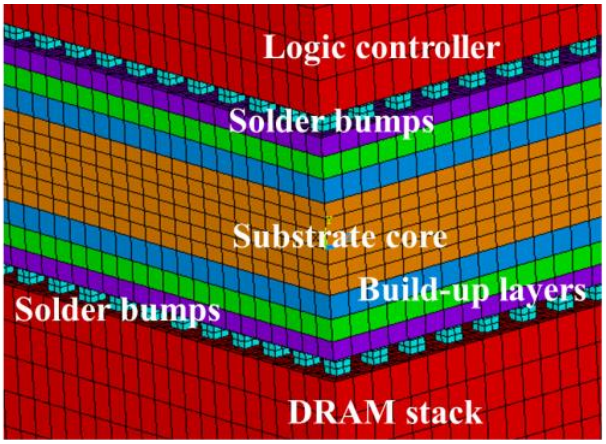


Figure 5.25: Mesh of the substrate and flip-chip solder bump region (underfills are hidden for clarity)

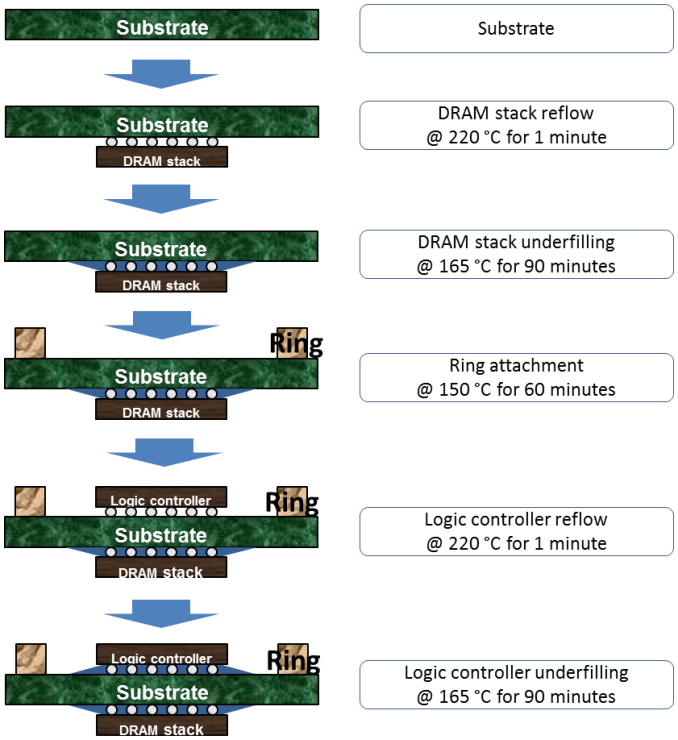


Figure 5.26: Assembly process of "Ring mid"

The dimensions of the assembly process model and the probing test model are listed in Table 5.6. Table 2.5, Table 5.7, and Table 5.8 provide the thermo-mechanical properties of materials used in the package, which is provided by the manufacturer or found in open literature.

Table 5.6: Package dimensions

Description	Dimension (mm)
Substrate size	35×35×0.968
DRAM stack size	12.3×21.8×0.785
Logic controller size	12.3×21.8×0.775
Ring size	3(W) ×0.84(T)
Gap between chip long edge and ring edge (X direction in Figure 5.24)	8.35
Gap between chip short edge and ring edge (Z direction in Figure 5.24)	3.6
Seal band thickness	0.03
Flip-chip solder bump diameter	0.10
Flip-chip solder bump height	0.09
Flip-chip solder pitch	0.20

Table 5.7: Material properties

	E (GPa)	υ	CTE (ppm/℃)	T_g (℃)
Cu	Table 2.5	0.3	17.3	N/A
Si	130.91	0.28	2.6	N/A
Sn/Pb	Table 5.8	0.4	21	N/A
Substrate core	29	0.2	α_1: XZ:15 Y:25 α_2: XZ:11 Y:150	210
Build-up layer (ABF-GX13)	Figure 5.27	0.258	α_1: XZ:46 Y:47 α_2: XZ:120 Y:155	170
Underfill	Figure 5.28	0.3	α_1: 36.0 α_2: 120.0	75
Austenitic stainless steel	193	0.3	17.3	N/A
Seal band	2.46@25 ℃ 0.01@250 ℃	0.4	α_1: 40.0 α_2: 100.0	85

Table 5.8: Material properties of Sn/Pb [69]

Temperature (℃)	Young's Modulus (GPa)
-25	27.39
25	19.65
85	15.27
125	11.68
Creep Model	$\dot{\varepsilon}_s = (1.84 \times 10^{-4})\sigma^{5.2} e^{-\left\{\frac{50}{[(8.314\times10^{-3})\times T]}\right\}}$

5.5.7 Material characterization

Beyond the values obtained from vendors and literature, some of the materials were characterized using in-house experiments. For example, to capture the time-dependent and temperature-dependent behavior of organic materials, including the build-up layer, substrate, and underfill, TA Instruments Q800® dynamic mechanical analyzer (DMA) was used to characterize the temperature-dependent elastic properties and viscoelastic material properties.

For the sample preparation, ABF-GX13 build-up thin film samples were cut from a large thin prepreg film, with the sample size being 63.3 mm×7.7 mm×0.04 mm. Then the samples were cured at 180 ℃ for 30 minutes, which is the same temperature profile as that of the substrate build-up process.

For underfill samples, the underfill material NAMICS U8439-1 was squeezed into a homemade Teflon sample makers and vacuumed in a vacuum chamber for two hours to remove bubbles. Then the samples were cured at 165 ℃ for 90 minutes to mimic the assembly process conditions. The cured underfill sample sizes were 30 mm×12.89 mm. The samples were then polished to obtain uniform thickness. The thickness for different samples ranged from 0.92 to 1.34 mm.

For the substrate, samples were cut from a larger package substrate. The substrate sample size was 35 mm in length and 0.968 mm in thickness. The width for different samples ranged from 2.7 to 2.98 mm. For the temperature-dependent modulus characterization, ABF-GX13 samples were tested using a tension clamp, while underfill and substrate samples were tested in a bending mode on a three-point bending clamp. The temperature was ramped from 25 ℃ to 175 ℃ for ABF-GX13 sample, from 25 ℃ to 175 ℃ for underfill samples, and from 30 ℃ to 230 ℃ for substrate samples. The maximum temperatures were chosen depending on the stability of the materials at these temperatures and the temperatures these materials will be exposed to during assembly

processing. Figure 5.27, Figure 5.28, and Figure 5.29 present the measured storage/loss modulus of the ABF-GX13, underfill, and substrate, respectively. These figures show that the glass transition temperature (T_g) of the ABF-GX13 is about 170 ℃, the T_g of the underfill is around 75 ℃, and the T_g of the substrate is about 165 ℃. It should be noted that the T_g values shown in Table 5.7 is for the substrate core and is from the vendor sheet, while the T_g of 165 ℃ is an in-house measured value and is for a multi-layer substrate with a core as well as buildup layers on top and bottom.

To determine the material viscoelastic properties, stress relaxation tests were performed with DMA. Samples were loaded for 20 minutes, followed by 10 minutes recovery. Then the above processes were repeated after every 5 ℃ increment until temperature reached 80 ℃ for the underfill and 215 ℃ for the substrate. The stress relaxation data was converted into a shear relaxation modulus by assuming isotropy condition. Then the data was shifted and formed into the master curves [69], as shown in Figure 5.31 and Figure 5.33. The corresponding shift factors are plotted in Figure 5.32 and Figure 5.34, which were fitted with Williams-Landel-Ferry (WLF) function by assuming both materials are Thermo-Rheologically Simple (TRS) [69]

$$\log_{10}(a_T) = \frac{-C_1\left(T - T_{ref}\right)}{C_2 + \left(T - T_{ref}\right)}$$

where C_1 and C_2 are the WLF constants. T_{ref} is the selected reference temperature for shifting. Figure 5.31 and Figure 5.33 present the shift factors and fitted curves. Table 5.9 lists the fitted WLF constants for underfill and substrate. Here we have negative constants for underfill material because all the experimental test data were obtained below T_g.

The master curves were curve-fitted using MATLAB™ to an eight-term Prony Series [70]

$$\mathrm{G}(t) = G_0\left[\alpha_\infty + \sum_{i=1}^{8} \alpha_i e^{\left(-\frac{t}{\tau_i}\right)}\right]$$

where G_0 is the shear relaxation modulus at $t = 0$. α_i is the relative moduli. τ_i is the relaxation time. Figure 5.31 and Figure 5.33 show the fitted curve, with the fitted α_i and τ_i listing in Table 5.10 and Table 5.11.

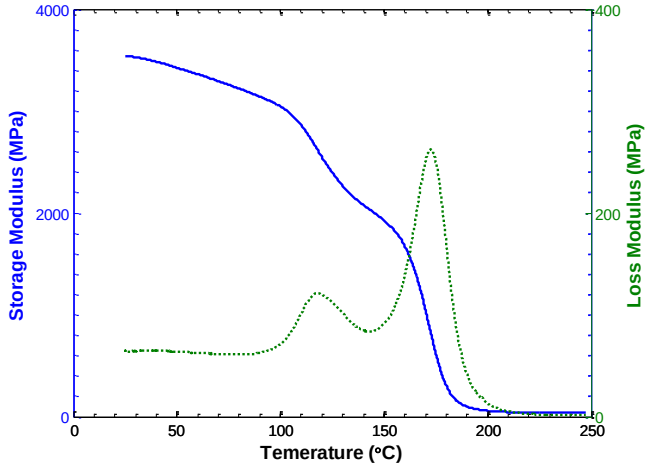


Figure 5.27: Modulus of the built-up layer ABF-GX13

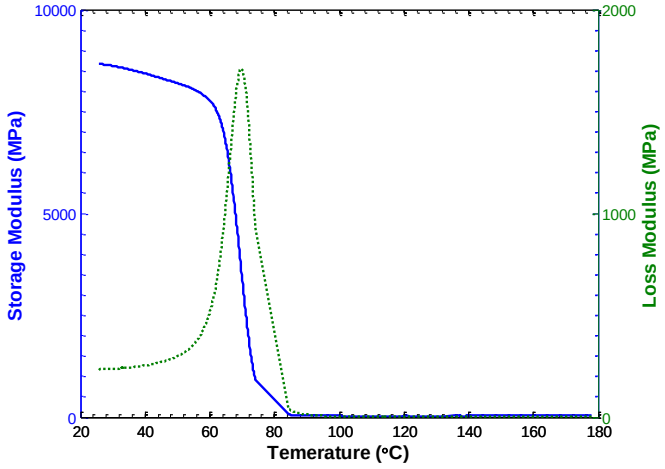


Figure 5.28: Modulus of the underfill NAMICS U8439-1

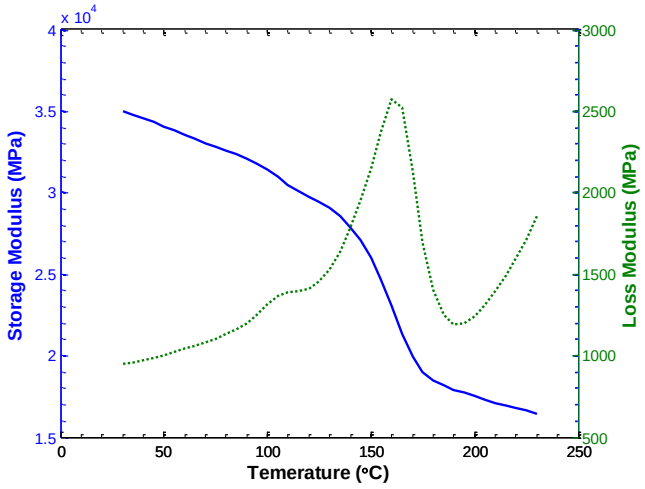


Figure 5.29: Modulus of the organic substrate

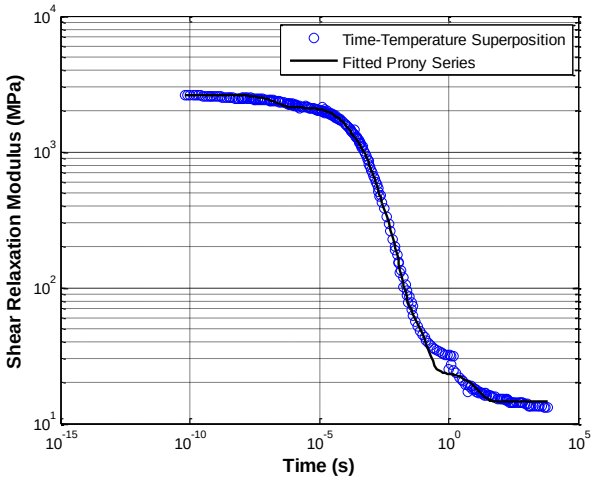


Figure 5.30: Log-Log plot of the master curve of the underfill NAMICS U8439-1 at 75 ℃

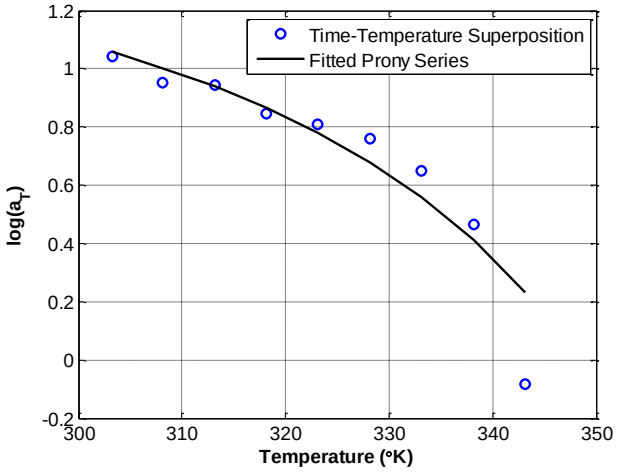


Figure 5.31: Shift function of the underfill NAMICS U8439-1

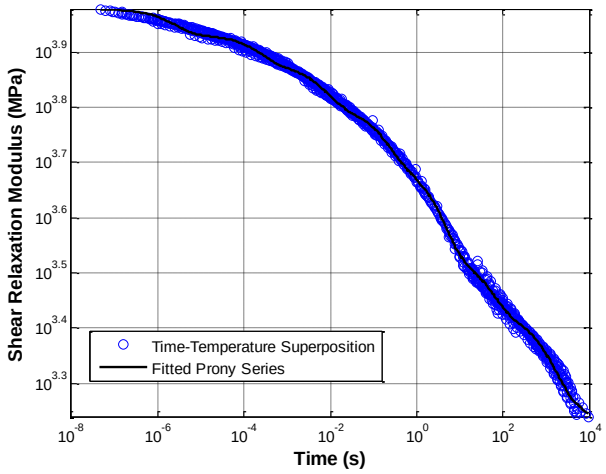


Figure 5.32: Log-Log plot of the master curve of the organic substrate at 165 ℃

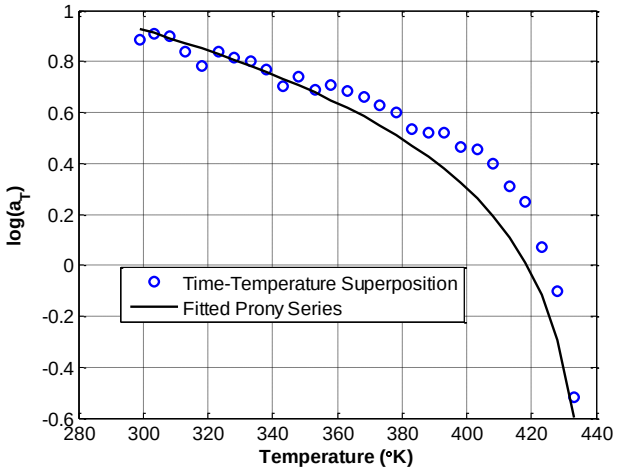


Figure 5.33: Shift function of the organic substrate

Table 5.9: Fitted WLF material constants for underfill and substrate

WLF constant	Underfill	Substrate
T_{ref} (°K)	348.15	438.15
C_1	-1.916	38.79
C_2 (°K)	-36.42	776.2

Table 5.10: Prony Series constants for underfill (G_0=2,626 MPa)

i	α_i (MPa)	τ_i (s)
1	0.003594961	12.06417538
2	0.245594057	9.13576E-05
3	0.021828378	0.099619536
4	0.093407944	0.000995244
5	0.257258968	0.000702763
6	0.18680745	2.05243E-07
7	0.065764817	0.009325692
8	0.120211699	0.004919816

Table 5.11: Prony Series constants for substrate (G_0=9,511 MPa)

i	α_i (MPa)	τ_i (s)
1	0.136246871	0.205971016
2	0.077913566	54.78186101
3	0.102819434	0.000250592
4	0.101512075	2.62496E-06
5	0.081986458	1370.628997
6	0.170487331	3.882425013
7	0.129082038	0.007806104
8	0.042831072	21276.90148

5.5.8 Model validation

The warpage results from the models were validated using shadow moiré experimental data as discussed below.

Assembly process model validation

To validate the assembly process model, a simplified configuration was used. In this configuration, the logic die was reflowed and assembled on one side of the substrate, and a stainless steel was attached on the same side of the substrate. The backside of the substrate did not have any die and was used to measure warpage using shadow moiré technique. First, a warpage test was carried out using shadow moiré (ThermoiréAXP®) on a bare substrate to determine the incoming substrate warpage at room temperature. Then the logic controller was reflowed and underfilled added on the top side of the substrate. After cooling down to room temperature, another warpage measurement of the substrate back side was conducted. Eventually, a stainless steel ring was attached on the same side as the logic controller and followed by warpage measurement on the substrate back side at room temperature.

Figure 5.34 (a) shows the measured warpage shape of the incoming substrate at 26 ℃. Figure 5.34 (b) shows the warped shape at 26 ℃ after the logic die assembly and Figure 5.34 (c) shows the warped shaped at 26 ℃ after stainless steel ring attachment. The warpage values are calculated by reading the out-of-plane displacement along path *A*-*B* and *C*-*D* in Figure 5.34 (a). The warpage value of each path is defined as the peak to valley difference. Then the averaged warpage values along the two paths are used as the warpage of the substrate at the corresponding temperature, with the sign convention defined in the inset in Figure 5.34 (a).

In the FE models, the substrate is assumed to be flat initially. Then the assembly process is simulated by the activation of corresponding components at their process temperatures. Figure 5.35 (a) shows the simulated warped geometry at 26 ℃ after the

logic die assembly, while Figure 5.35 (b) shows the warped geometry at 26 ℃ after the subsequent ring attachment. The warpage contours in Figure 5.35 are obtained from the viscoelastic model. As the shadow moiré experiments measured the warpage on the bare backside of the substrate, the models were also appropriately inverted to be able to easily compare the contours. It should also be pointed out that the simulated warpage values cannot be directly compared against experimental warpage values, as the experiments have warpage values for incoming substrate, while the simulation assumes the incoming substrate to be flat.

The warpage magnitude between models and experiments are compared in Figure 5.36, where the measured warpage of the incoming substrate is subtracted from subsequent measured warpage values. Figure 5.36 shows that both the linear elastic model and the viscoelastic model predict the trend of the warpage change in the right direction. However, the prediction of the viscoelastic model matches better than that of the linear elastic model. The latter overestimates the substrate warpage.

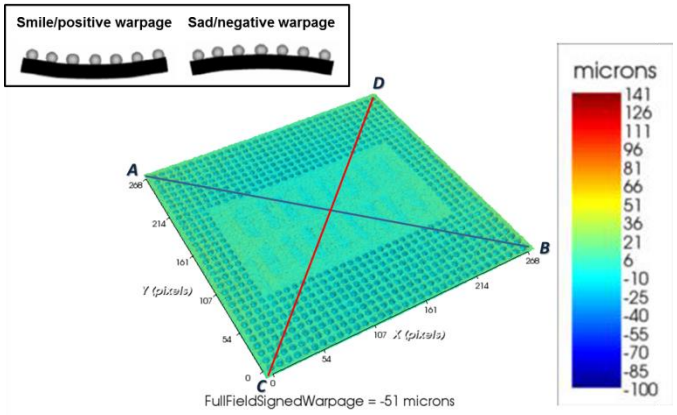


Figure 5.34 (a): Substrate incoming warpage at 26 ℃

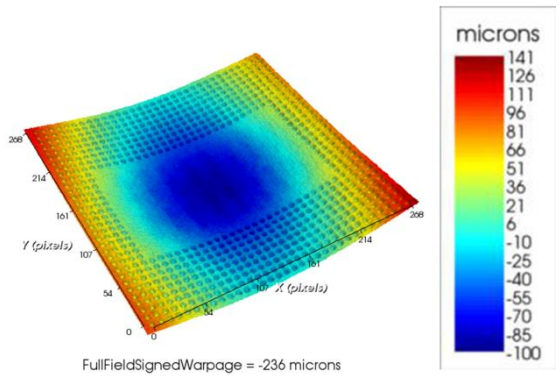


Figure 5.34 (b): Measured substrate warpage at 26 ℃ after logic controller assembly

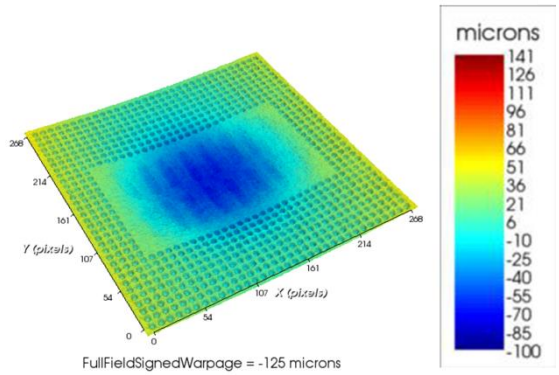


Figure 5.34 (c): Measured substrate warpage at 26 ℃ after ring attachment

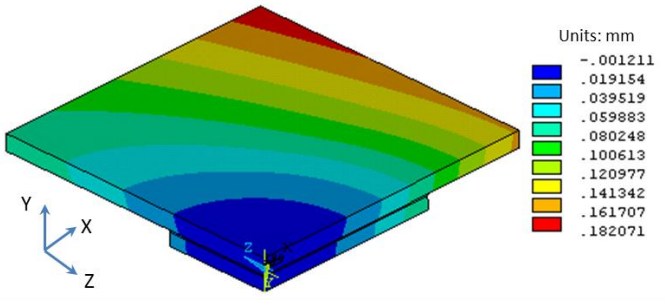


Figure 5.35 (a): Predicted substrate warpage shape at 26 ℃ after logic controller assembly

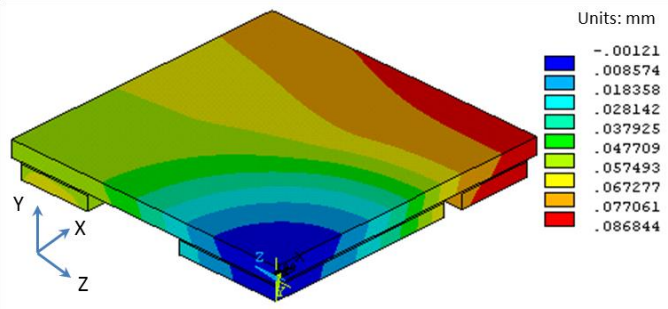


Figure 5.35 (b): Predicted substrate warpage shape at 26 ℃ after ring attachment

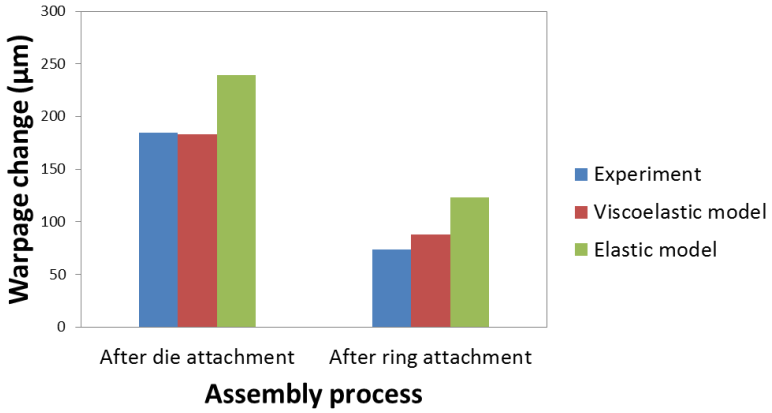


Figure 5.36: Substrate warpage comparison at 26 ℃ during assembly

Assembled package validation under temperature excursions

As shown in Figure 5.37, a test package was assembled following the "Ring mid" process as shown in Figure 5.26. This assembled package was then subjected to external temperature excursions. The warpage contours of the DRAM stack external surface at multiple temperature points were obtained using shadow moiré (TherMoiré AXP). Here, the DRAM stack top surface was chosen because it could be conveniently accessed through the Moiré system. Figure 5.37 shows the warpage contours at 183 ℃ during the warpage experiments and at 26 ℃ after the experiments; the results indicate that at both temperatures, the DRAM stack warps inward toward the substrate. The warpage values for each temperature were calculated following the same procedure as discussed in the previous section. Table 5.12 lists the measured DRAM stack warpage data at multiple temperatures. As seen in Table 5.12, the DRAM stack warpage is very small, within 2

μm change between 183 ℃ and 26 ℃. This is at the resolution limit of the shadow moiré system 2~3 μm.

Similar to the experiments, simulations are carried out to determine the DRAM stack warpage at the same test temperatures. In these simulations, the package assembly process are first simulated following the "Ring mid" process as discussed earlier, and then the entire package goes through the same simulation temperature profile as in the physical test. Figure 5.38 shows the warpage contours (U_y) of the DRAM stack at 183 ℃ and 26 ℃. The warpage contours show that the DRAM stack warped inward at both temperature extremes, which matches the measured warpage shape. As listed before, the model result coordinate *Y* axis is reversed to match the measurement result coordinate. Figure 5.39 shows the warpage values of the experiments and simulations follow similar trends. Also, the viscoelastic model gives closer prediction than the elastic model.

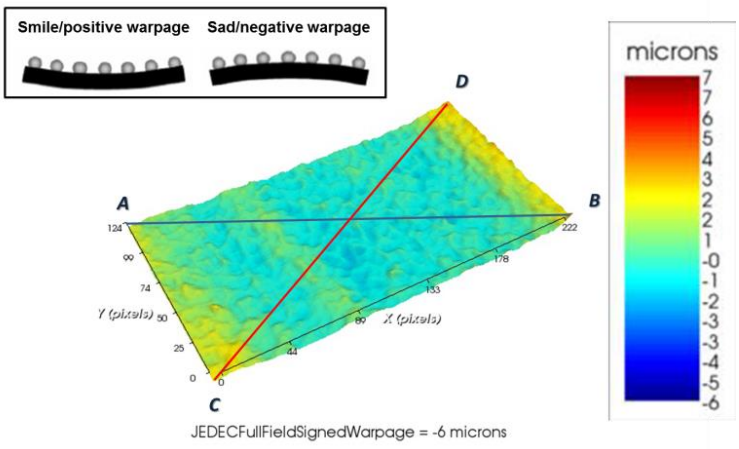


Figure 5.37 (a): DRAM stack warpage contours at 183 ℃

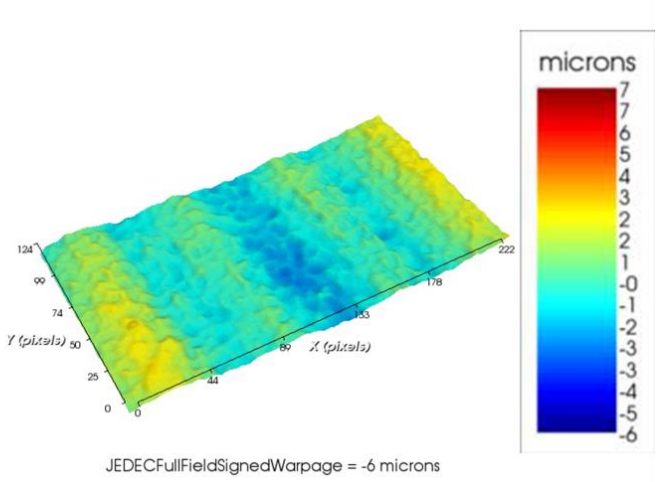


Figure 5.37 (b): DRAM stack warpage contours at 26 ℃

Table 5.12: Shadow moiré measured of DRAM stack warpage

Temperature (℃)	Warpage (μm)
26	5
80	4
125	5
150	5
165	6
183	6
165	5
150	5
125	4
80	5
26	6

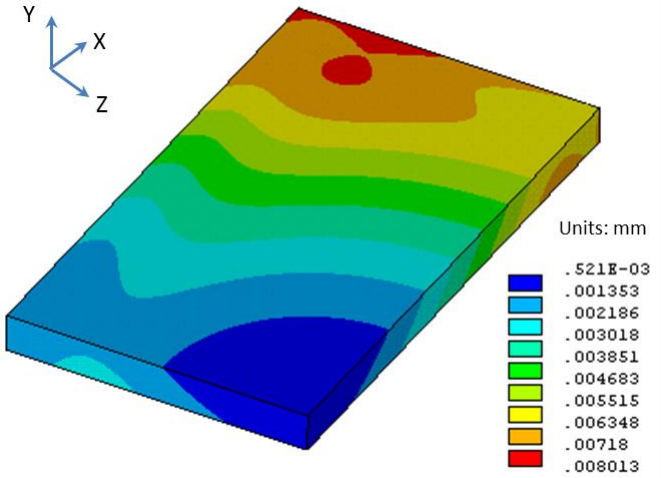


Figure 5.38 (a): Predicted DRAM stack warpage at 183 ℃

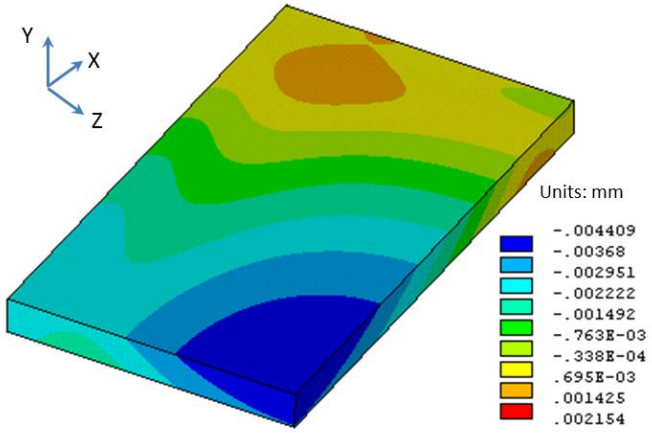


Figure 5.38 (b): Predicted DRAM stack warpage at 26 ℃

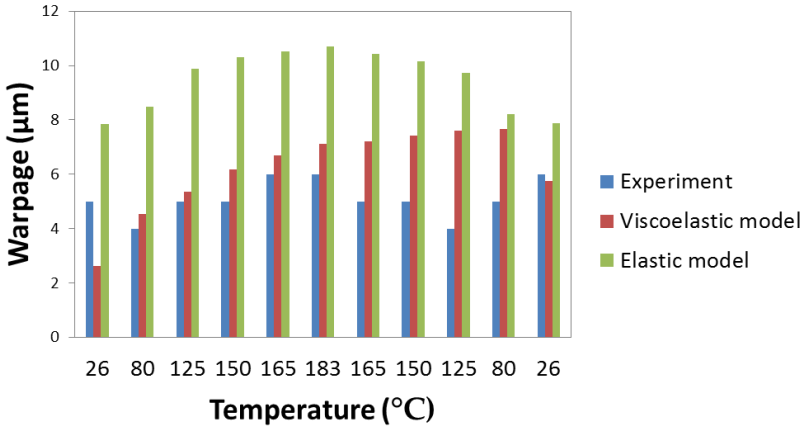


Figure 5.39: DRAM stack warpage comparison

5.5.9 Assembly process analysis

The above model validation indicates that the viscoelastic model generally gives more accurate warpage prediction than that of the elastic model. Thus, the viscoelastic model will be used in the following package assembly study.

Because the double-sided flip-chip package has both a large DRAM stack and a large logic controller relative to the small laminate substrate, thermo-mechanically it becomes a silicon-dominant package. Therefore, the CTE mismatch between the laminate substrate and silicon chips can induce large warpage, as shown in Figure 5.40. In addition, this double-sided flip chip on a laminate substrate poses unique assembly

problems. As Figure 5.40 shows, when we assemble the logic controller on the top side of the substrate, the substrate is already warped due to the CTE mismatch between the DRAM stack and the substrate. This incoming warpage may cause solder open/short problem at the logic controller center/edges. Thus, assembly process and package material selection should be optimized to prevent or at least mitigate this problem. In this work, three types of assembly processes are proposed and compared. They are: "Ring first", where the austenitic stainless steel ring is attached on a bare substrate on the logic controller side before any chip attachment; "Ring mid", where the ring is attached after DRAM stack assembly and underfilling, as shown in Figure 5.26; and "Ring last", where the ring is attached after both the DRAM stack and logic controller have been assembled.

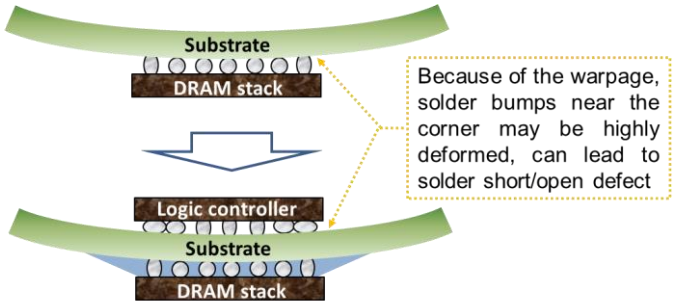


Figure 5.40: Double-sided flip-chip package warpage at room temperature

Here the austenitic stainless steel "Ring mid" case is discussed as an example. Figure 5.41shows the warpage evolution of the substrate, DRAM stack, and logic controller during the assembly process. Positive warpage indicates a concave bowl shape and negative warpage means a convex dome shape. The value shown in Figure 5.41 is the peak to valley vertical distance.

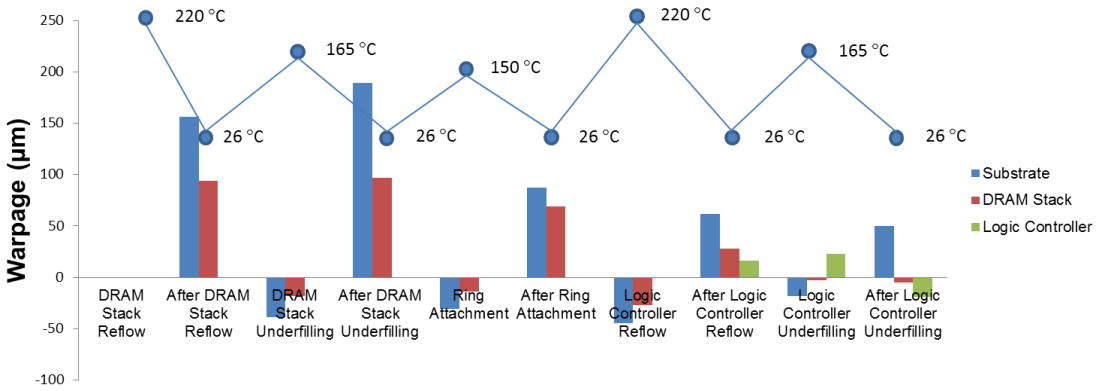


Figure 5.41: Warpage evolution during assembly process for austenitic stainless steel "Ring first" case

As seen in Figure 5.41, when the DRAM stack is reflow attached on the bottom side of the substrate and then cooled down to room temperature, the substrate structure has a concave bowl shape due to the higher CTE of the substrate compared to the silicon. A larger warpage spike occurs after the DRAM stack underfilling, and the assembly has a concave bowl shape at room temperature. This large concave warpage occurs because of the stronger mechanical coupling between the DRAM stack and the substrate due to the presence of the underfill. When the austenitic stainless steel ring is attached using sealband at 150 ℃ and cooled to room temperature, the substrate-ring-DRAM stack assembly still has a bowl shape. However, this warpage is somewhat smaller due to the presence of the ring. Subsequently, when the logic controller is reflow attached and then underfilled (Figure 5.42), the overall warpage of the assembly is less than various intermediate steps. This shows that the presence of the DRAM stack and the logic controller on both sides of the laminate substrate balances and reduces the warpage, compared to cases where both chips are assembled on the same side. Thus, the proposed design is also helpful for the subsequent BGA or LGA assembly onto the PCB.

The above case study indicates that the attachment of a ring can effectively reduce the intermediate and final substrate warpage. To find the optimal assembly process with the minimum intermediate and final warpage, three different cases were simulated. Table

5.13 lists the assembly warpage with austenitic stainless steel ring, where all three ring attachment cases are analyzed and compared. It shows that "Ring first" case gives reasonable intermediate/final warpage and therefore, it should be considered for the double-sided flip assembly design.

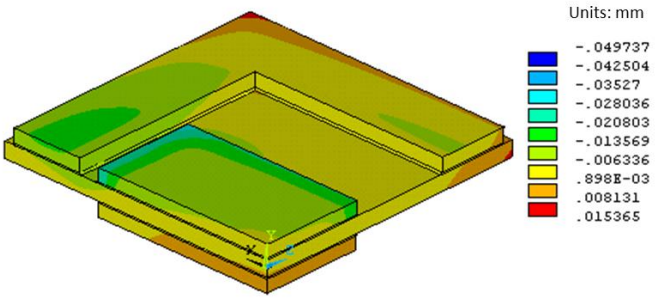


Figure 5.42: Final warpage shape the double-sided flip chip for the austenitic stainless steel "Ring mid" case

Table 5.13: Warpage during assembly with austenitic stainless steel ring

Substrate warpage/um	**After ring attach**	**After DRAM stack reflow**	**After logic controller reflow**	**Final warpage**
Ring first	-16	88	72	57
Ring mid	87	156	62	50
Ring last	35	156	95	35
DRAM stack warpage/um	**After ring attach**	**After DRAM stack reflow**	**After logic controller reflow**	**Final warpage**
Ring first	N/A	77	32	8
Ring mid	69	94	28	-5
Ring last	-3	94	33	-3
Logic controller warpage/um	**After ring attach**	**After DRAM stack reflow**	**After logic controller reflow**	**Final warpage**
Ring first	N/A	N/A	14	-15
Ring mid	N/A	N/A	16	-19
Ring last	-18	N/A	14	-18

CHAPTER 6

THERMOMECHANICAL RELIABILITY STUDY OF 3D INTEGRATED PACKAGES WITH TSVS

Previous chapter discussed package warpage issue during and after the package assembly. In this Chapter, three-dimensional thermomechanical finite-element models have been built to analyze the TSV reliability in free-standing wafers as well as in 3D integrated packages containing stacked dies with TSVs, inter-chip microbumps, mold compound, and underfilled solder bumps that connect the stacked dies to an organic substrate. Based on those FE models, thermomechanical performance of TSVs in free-standing wafers and 3D integrated packages have been analyzed and compared.

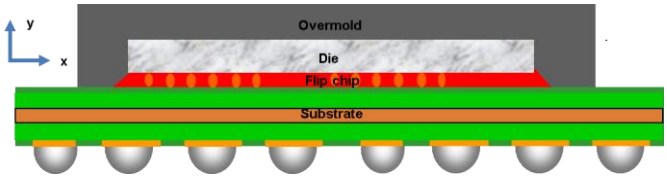
6.1 Finite-element modeling

Comprehensive three-dimensional finite element models have been developed to capture the details of the 3D packages. Schematic views of two of the packages modeled in this work are shown in Figure 6.1. As shown in Figure 6.1 (a), the package ***A*** has just one die and no TSV, and this package is used for FE model validation, because of the availability of warpage data for this package. Also, this package has similar materials as the 3D integrated package ***B*** shown in Figure 6.1 (b). In this 3D integrated package ***B***, two dies are stacked and interconnected by TSVs and microbumps in between. The dimensions of packages ***A*** and ***B*** are list in Table 6.1 and Table 6.2.

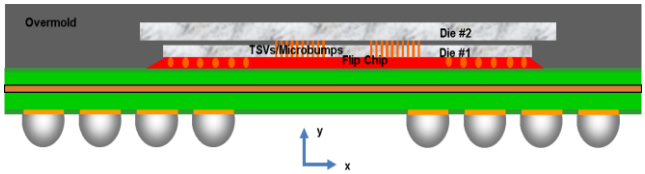
Due to planar symmetry, one quarter of the top view of the packages was modeled and symmetric boundary conditions were applied on the inner surfaces (XY and YZ plane), which are shown in Figure 6.2. One node at the origin is rigidly held to prevent rigid body motion of the package. Since the focus of this work is to perform a thermomechanical stress analysis of the stacked die region, the solder bump and underfill region of the flip chip on organic substrate is modeled using smeared underfill and solder

bump thermomechanical properties. The smeared properties can be obtained by creating a representative unit cell that contains detailed copper pillar, solder, and underfill geometries and their representative properties. The unit cell is then subjected to mechanical loading in various normal and shear directions to get the effective normal and shear modulus values in various directions. Similarly, the unit cell is subjected to thermal excursions to be able to determine the effective coefficient of thermal expansion in different directions. Thus, the underfill and solder bump layer is modeled thermo-elastic and orthotropic. All interfaces have been assumed to be perfectly bonded.

Table 6.3, Table 2.5, and Table 6.4 provide the thermomechanical properties of materials used in packages A and ***B***, and these properties are similar to the properties found in open literature.



(a) Package ***A*** without TSV



(b) 3D package ***B*** with stacked dies and interconnected by TSVs

Figure 6.1: Schematic view of packages

Table 6.1: Package *A* dimensions

Description	Dimension (mm)
Substrate size	12×12×0.334
Die size	8.4×8.2×0.1
Gap between die and substrate	0.025
Gap between die and mold cap top	0.125

Table 6.2: Package *B* dimensions

Description	Dimension (mm)
Substrate size	12×12×0.4
Die #1 size	8×8×0.05
Die #2 size	9×9×0.1
TSV diameter	0.01
TSV pitch	0.05
Cu pillar diameter	0.021
Cu pillar height	0.007
Solder layer between top/bottom Cu pillars	0.003
Gap between die #1 and substrate	0.035
Gap between die #2 and mold cap top	0.1
Gap between die #1 and die #2	0.2

Table 6.3: Material properties [46]

	E (GPa)	υ	CTE (ppm/℃)	T_g (℃)
Cu	Table 2.5	0.3	17.3	
SiO_2	71.4	0.16	0.5	
Si	130.91	0.28	2.6	
SnAg	Table 6.4	0.4	Table 6.4	
Substrate	29@25℃ 18@250℃	0.2	XZ: 11 Y:22 XZ: 6 Y:115	180
Die#1 to substrate underfill	5.8@25℃ 1.2@250℃	0.3	α_1: 31.1 α_2: 63.5	88
Die#1 to Die#2 underfill	2.5@25℃ 0.056@250℃	0.39	α_1: 59 α_2: 159	125
Mold compound	29@25℃ 18@150℃	0.3	α_1: 25 α_2: 85	145

Table 6.4: Material properties of SnAg [71]

Temperature (℃)	Young's Modulus (GPa)	CTE (ppm/℃)
-60	121.00	26.19
-40	120.48	26.60
25	117.88	27.91
50	115.24	28.42
125	112.64	29.90
Creep Model	$\dot{\varepsilon} = 178.6[\sinh(0.115\sigma)]^{4.75} exp^{-\frac{57.1}{kT}}$	

6.2 Model validation

As mentioned earlier, package ***A*** was used for model validation. Ten samples of package ***A*** were subjected to temperature excursion from 183 ℃ to 25 ℃, and the warpage contours at 183 ℃ and 25 ℃ were obtained using shadow moiré[3]. Table 6.5 presents the warpage data for the two temperature extremes. As seen in Table 6.5, the warpage is minimum at 183 ℃ and is maximum at 25 ℃. The difference between the two warpage values can be roughly taken to be the warpage induced by the thermal excursion from 183 ℃ to 25 ℃. Table 6.5 shows the average measured warpage for the 10 samples to be 109.09 μm with a standard deviation of 7.2 μm.

Similar to the experiments, simulations were carried out to determine the warpage at 25 ℃. In these simulations, the entire package was assumed to be stress-free and flat at 183 ℃. Figure 6.2 shows the warpage contours (U_y) of the package at 25 ℃. When the package was simulated to be cooled from 183 ℃ to 25 ℃, the package warped down in a convex shape, and the laminate warpage, as seen in Figure 6.2, was around 104.2 μm. Thus, the predicted warpage agrees well with the experimental test data within one standard deviation, which validates the model prediction of the global behaviors.

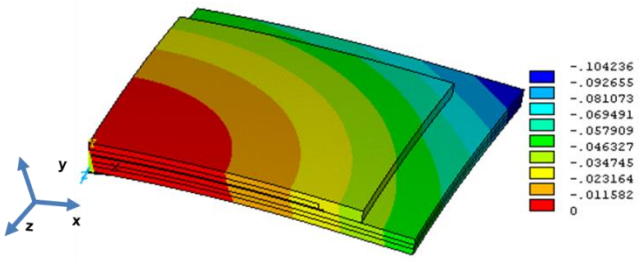


Figure 6.2: Warpage contours (in mm) of package *A* at 25 ℃

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[3] Shadow moiré warpage measurement was carried out in Texas Instruments Inc.

Table 6.5: Shadow moiré measurement of laminate warpage (μm)

Sample	Warpage at 183 ℃	Warpage at 25 ℃	Warpage change (μm)	Average warpage (μm) and std. dev.
1	-13	87	100	
2	-15	93	108	
3	-16	96	112	
4	-18	98	116	
5	-22	86	108	109.09
6	-21	81	102	and 7.2
7	-18	105	123	
8	-14	97	111	
9	-20	83	103	
10	-23	93	116	

6.3 Reliability analysis results and discussion

Once the thermomechanical finite-element modeling approach was validated, the package ***B*** was used in the following simulations for TSV analysis. In these simulations, different stress-free temperatures were used for each component to account for the residual stress resulting from the various fabrication process steps.

6.3.1 TSVs and microbumps in 3D packages

After validating the warpage results using Package ***A***, Package ***B*** with a TSV array pattern as shown in Figure 6.3 was then modeled. The TSV array has four symmetric blocks, and each block has 36 × 7 TSVs with a pitch of 50 μm. When the package was simulated to be cooled from 150 ℃ to -40 ℃, the package warped down in a convex shape, and this warpage pattern is similar to the warpage pattern in package ***A***, used for validation. Figure 6.4 shows the warpage (U_y) contours at -40 ℃. Figure 6.5 shows the warpage (U_y) contours in the TSV region.

In order to perform thermomechanical stress/strain analysis of TSVs and microbumps, the cut-boundary displacement method was applied. This method, based on St. Venant's principle, improves computational efficiency and is also able to capture the

detailed structure of TSVs and microbumps in the stacked die region. In this method, a relatively coarse global model was first built, in which all the components of the packages were modeled. Then a submodel was built with all the geometry details, and a denser mesh was applied in the regions of interest. The displacements of the cut boundary from the global model were applied on the submodel as input boundary conditions, and a subsequent analysis was carried out using the submodel.

Figure 6.6 (a) shows the TSV structure in the global model where die 2 on the top, microbump region surrounded by an underfill, die 1 with TSV, and part of solder bump and underfill smeared region are shown. The image shown in Figure 6.6 (a) is a cut view through TSV center plane. Therefore, the images appear rectangular, although the TSV and the interconnect geometries are modeled as cylindrical geometries. Figure 6.6 (b) shows the detailed submodel of the TSV where die 2 with its Cu pad, passivation layer, Cu pillars, solder, die 1, and TSV with the liner material were modeled. Figure 6.7 shows the total (elastic plus inelastic) strain distribution in the TSV, Cu pillar, and solder regions from the submodel. As seen, solder and Cu pillar near the solder interface experience high strains. Figure 6.8 (a) shows the solder creep strain, and Figure 6.8 (b) shows the time-independent plastic strain in Cu. As seen from these contours, solder and Cu pillar are some of the critical regions for further study.

Based on the discussion thus far, it is clear that the solder region is the critical region, and therefore, the location effect of the TSV/microbump array is studied here. The layout of the TSV/microbump array is shown in Figure 6.3, where ***a*** – ***i*** are the nine representative locations studied here to capture the overall distribution in the array. Results show that the solder creep strain is the highest in the corner region as opposed to the center region [72]. However, it should be pointed out that the difference between the corners to the center is not significant for the array studied in this work.

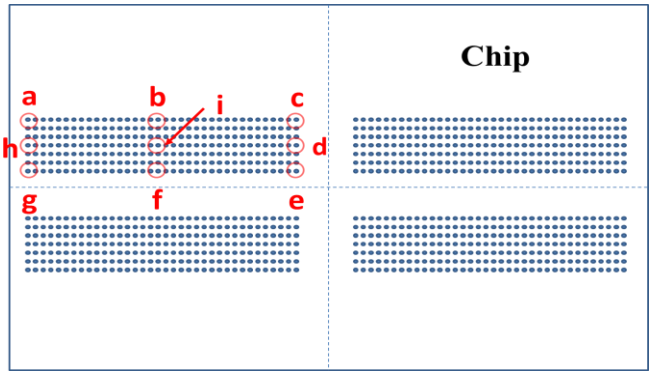


Figure 6.3: TSV array layout in 3D package *B*

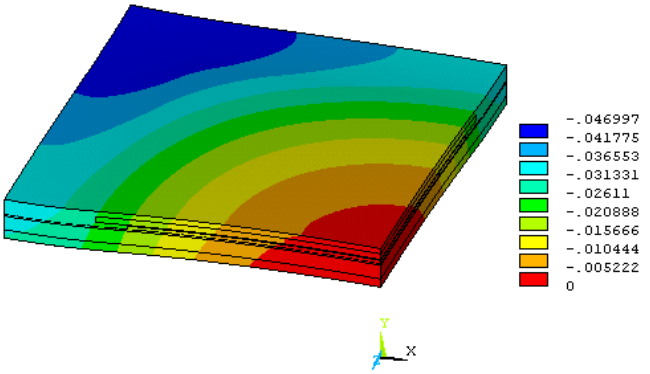


Figure 6.4: Warpage (U_y) contours (in mm) of package *B* at -40 ℃

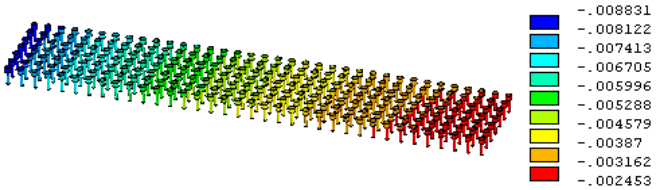


Figure 6.5: U_y contours (in mm) of TSV array in package *B* at -40 ℃

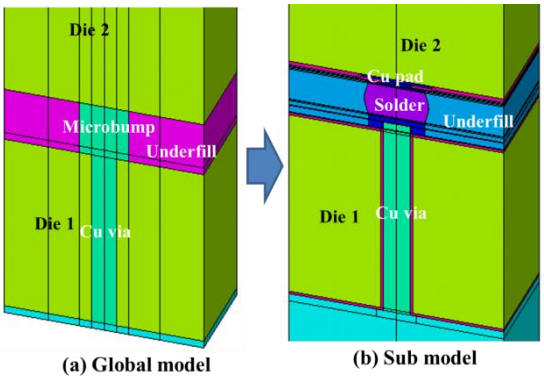


Figure 6.6: TSV and microbump in global and sub models

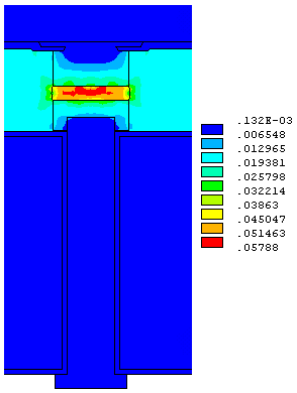
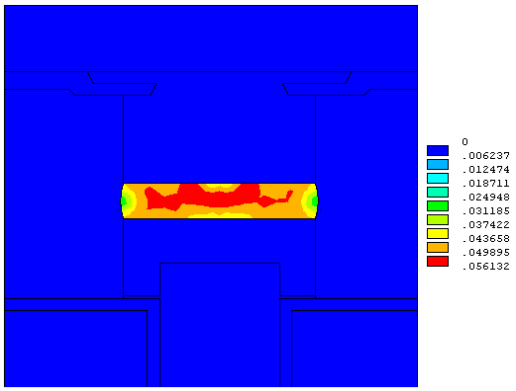
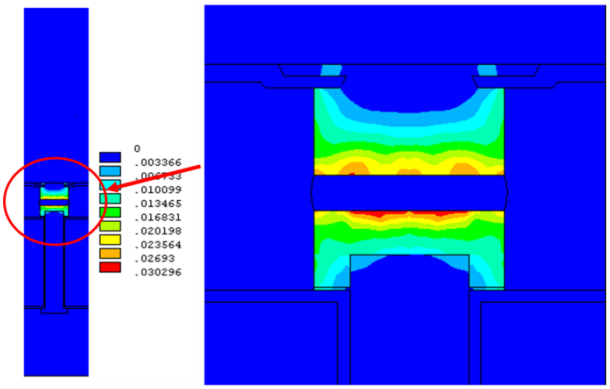


Figure 6.7: Total (elastic and inelastic) strain distribution at -40 ℃



(a) Equivalent creep strain distribution in solder at -40 ℃



(b) Equivalent plastic strain distribution in Cu via and Cu pillars at -40 ℃

Figure 6.8: Strain distribution near the Cu pillar region

6.3.2 Analysis of TSV/microbump in 3D integrated packages with stacked dies

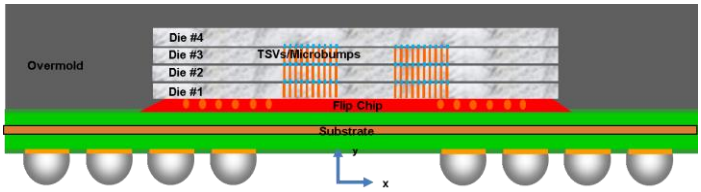


Figure 6.9: 3D integrated package with 4-stack dies and interconnected by TSVs/Microbumps

In addition to the above 3D package with two stacked dies, packages with three and four stacked dies (Figure 6.9), which have the same die size and die thickness as the stacked two dies package, have also been modeled to study the effect of multiple stacked dies on TSV/microbump reliability. Table 6.6 provides the dimensions of the multi-die package structure.

Table 6.6: Dimensions of the multi-die package

Description	Dimension (mm)
Substrate size	12×12×0.4
Die size	8×8×0.1
TSV diameter	0.01
TSV pitch	0.05
Cu pillar diameter	0.021
Cu pillar height	0.007
Solder layer between top/bottom Cu pillars	0.003
Gap between bottom die and substrate	0.035
Gap between top die and mold cap top	0.1
Gap between dies	0.2

It should be pointed out that although Si is stacked on Si, the high strains in the microbumps are possibly due to the presence of long Cu core in the TSVs, and these Cu cores contract more than the surrounding Si and SiO_2 resulting in higher solder strains. It should also be noted that the viscoplastic behavior of SnAg solder was modeled, as outlined in Table 6.4, and the IMC layer was not modeled for computational reasons as

well as for consistency, as this work compares microbump strains under different die stacking configurations. Therefore, to compare the microbump reliability of different interconnect levels, submodels were built for the furthermost corner TSVs/microbumps (location ***a*** in Figure 6.3).

The effect of the number of dies on the die warpage is shown in Figure 6.10. As seen, as more dies are stacked, the warpage decreases due to the stiffening effect of the stacked dies. Figure 6.11 shows the total strain contours in one outermost corner stack of TSVs and microbumps. The total strain in the microbump solder layer and Cu includes elastic and inelastic strains, while for all other materials in the stacked die assembly, total strain is the same as the elastic strain. As discussed for a two-die stack in Figure 6.8 (a), the microbump region shows the maximum total strain. Figure 6.12 compares the magnitude of total strain in the microbump regions for different die stacks. As seen in Figure 6.12, for the microbumps present in between die 1 and die 2, the magnitude of inelastic strain increases as the number of stacked dies is increased from two to four. This is because as the number of stacked dies increases, the stiffness of the package will increase and the warpage will decrease, and thus, the microbump strain will increase.

In addition to microbump reliability, interfacial delamination between SiO_2 and Cu via and dielectric cracking are some other reliability concerns. Interfacial shear stress (σ_{xy}) contours are similar from the bottom die to the top die. As Figure 6.13 shows, for a given TSV, the high interfacial shear stress occurs near the TSV edge (point ***A***), Cu pillar outer edges (point ***B***) and top pad edge (point ***C***), and the maximum value occurs at Cu/SiO_2 interface (point A). Figure 6.14 compares the magnitude of interfacial shear stress at Point ***A*** for various die stacking configurations. For a given die, the interfacial stress does not change much when one or more dies are stacked on top. The maximum interfacial shear stress, as shown in Figure 6.14, is primarily governed by the materials and geometries near the corner region, and thus is not influenced by the presence of additional dies on top. However, when the interfacial stresses across different interfaces

are compared, stresses show a variation of less than 20% with the middle interface showing the maximum shear stress. In other words, the interfacial stresses near the corners are governed by the material and geometry singularity at those locations and the minor variation in the magnitude is due to the overall shear variation across the warped structure. It should be pointed out that in all of these analyses, the mesh structure was kept identical, and therefore, the magnitude of the stresses across different interfaces could be compared.

Although the overall magnitude of warpage decreases with more number of dies stacked, the maximum principal stress in the top die increases with more number of dies (Figure 6.15). As the number of dies is increased, the overall thickness of the die stack increases resulting in high tensile stresses. This is because when bending is not considered, a silicon die on an organic substrate has axial compressive stress upon cooling, and this compressive stress in the die will decrease when the die thickness is increased. When the die-substrate structure warps down in a dome shape upon cooling or when bending is considered, the highest tensile axial stress occurs at the top layer of the die. The combination low compressive stress and high tensile stress makes the top die to have the highest principal stress. This discussion, although pertinent to a die stack on an organic substrate, has to be understood in the context of molding compound where additional singularity effects play a role near the die corners.

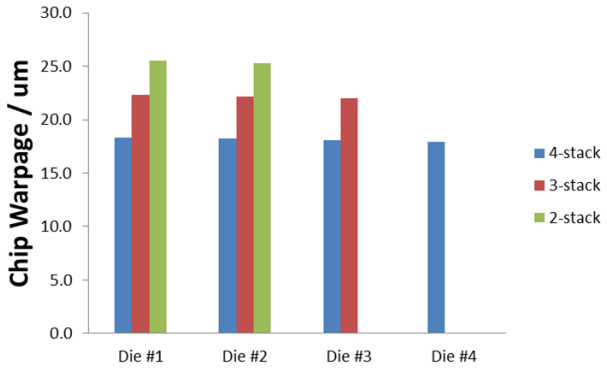


Figure 6.10: Chip warpage in 3D integrated packages

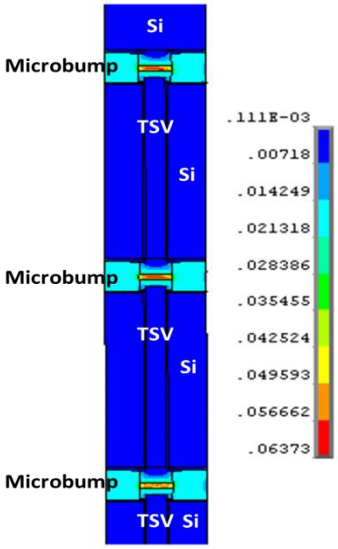


Figure 6.11: Microbump (at location *a*) total strain in four-stack packages

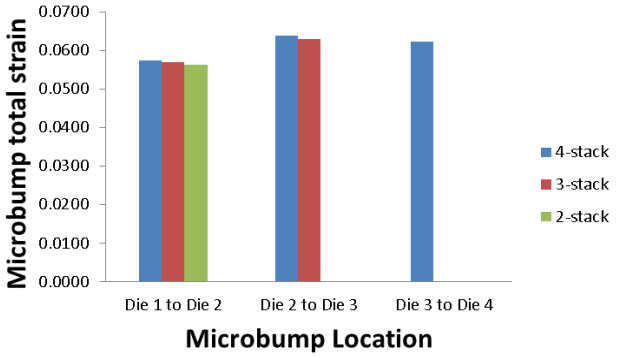


Figure 6.12: Microbump (at location *a*) total strain in 3D integrated packages

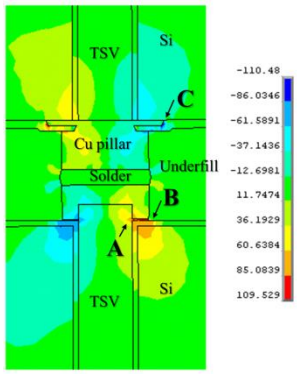


Figure 6.13: Interfacial shear stress distribution in the level 1 microbump of four-stacked die packages

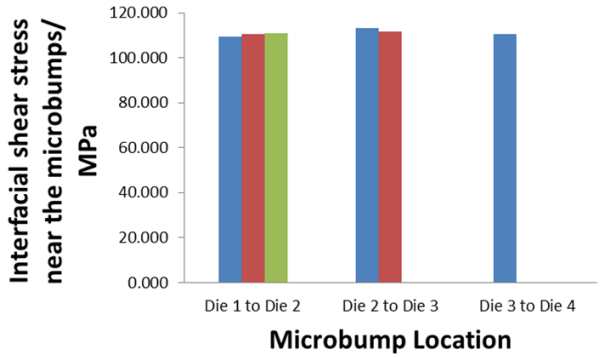


Figure 6.14: Cu/SiO_2 Interfacial shear stress at Point *A*

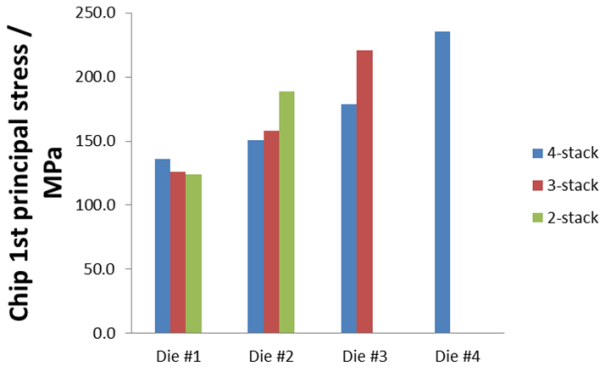


Figure 6.15: Max 1st principal stress of the stacked dies

6.3.3 Analysis of TSVs in a package versus in a free-standing wafer

Since TSVs in 3D integrated packages behave differently from those in free-standing wafers, it is worthwhile to compare the two cases. For this comparison, the TSV at location ***a*** (Figure 6.3) in the 4-die stack packaging configuration (Figure 6.9) was used. In parallel, another model of TSV in a free-standing wafer, which has exactly the same geometry and materials in the TSV region, was built. Similar periodic boundary conditions as in Section 2.3 were applied to mimic TSV layout in the free-standing wafer, and are discussed here briefly for the sake of completeness. Three-dimensional unit-cell TSV model was created where the planar dimension of the model was the pitch of the TSV and the vertical dimension was the entire axial length of the TSV with the end copper pillars on both sides. Such a square prism model included copper, dielectric, and

silicon in the unit cell with the TSV placed at the center. The normal displacements on the vertical planes of the model were coupled so that the model remained a square prism upon thermal loading, and one node was also constrained in the vertical direction to prevent rigid body motion.

The stress-free temperature for the TSV structure in free-standing wafer was taken to be 50 ℃ to mimic typical plating temperature as well as to correlate with XRD measurements [22]. Then, the free-standing wafer with the TSV was simulated to be cooled down to -40 ℃, and the results were compared against the results from the packaged stacked dies. It should be pointed out that the stress-free temperature of the free-standing wafer with TSVs was 50 ℃, while different components (underfill, microbump solder, molding compound, substrate, copper in TSV, etc.) in the packaged stacked dies had different stress-free temperatures.

As Figure 6.16 shows, the displacement U_y of TSV in the package is dominated by the warpage of the package, which can also be seen from Figure 6.5. Also, the U_y progressively decreases from the bottom to the upper dies, as shown in Figure 6.16 (a-c). This trend is to be expected, as the structure warps down (dome) upon cooling, the bottom die will experience most out-of-plane displacement. Also, it is important to notice the general gradient of deformation from left to right for a given die indicating the warped geometry. On the other hand, the free-standing wafer shows no warpage, as would be expected, due to the structural and material symmetry about the central plane of the wafer. The U_y contours shown in Figure 6.16 (d) are indicative of the contraction of the structure upon cooling in the thickness direction and the contours are essentially symmetric about the axis of the TSV. Also, it is seen that the copper core has contracted more than the surrounding Si/SiO_2 material, as would be expected.

Different from the U_y distribution discussed above, results show that in the stacked four-die package, the corner stress/strain distributions are similar in different

stack levels. Therefore, in the following study, only the stress/strain in Die#1 are used to compare with the free-standing case.

Figure 6.17 and Figure 6.20 show the stress contours of the two cases. Figure 6.17 shows the σ_{xy} shear stress distribution on the *xy* cross-sectional plane of the TSV. As seen, the shear stress contours as well as shear stress magnitude are roughly the same for the package case and the free-standing case. In both cases, the maximum shear stress occurs near the edges of TSV/SiO_2 interface. σ_{xx} contours on the *xy* cross-sectional plane of the TSV are presented in Figure 6.18. These stresses on *xy* plane can be thought of normal radial stresses. As seen, when the structure is cooled from high to low temperature, Cu shrinks more than the surrounding SiO_2 and Si, and thus results in tensile opening stress at the interface as illustrated for the free-standing wafer case. However, the radial stress near the Cu/SiO_2 interface of TSV in the package is generally compressive due to the presence of other components in the package, and particularly due to the compressive stresses induced by the shrinkage of the mold compound. Therefore, interfacial delamination in TSVs is a concern in free-standing wafers; however, it may not be a concern when TSVs are in a packaging configuration. Figure 6.19 presents the 1^{st} principal stress distribution in the dielectric. All other components are hidden to focus on the dielectric alone. As seen, the principal stress is generally higher in the dielectric in the core of the TSV for the free-standing wafer compared to the packaging configuration. All of these observations indicate that interfacial delamination and dielectric cracking could be more of a concern for TSVs in a free-standing wafer as opposed to TSVs in a packaging configuration. Figure 6.20 shows the plastic strain distribution in Cu. As seen, higher strains occur in Cu pillar that are bonded to solder material in the packaging configuration compared to the unconstrained Cu pillar in a free-standing wafer, and thus the critical location has shifted to the microbump region for a packaging configuration. It should be pointed out that all of these observations are drawn based on the comparison against a corner TSV (location ***a***) in a 4-die stack packaging configuration. Based on the

discussion in Section 6.3.2, the conclusions drawn for a 4-die stack are applicable for 2-die and 3-die stacks as well.

The findings in this work illustrate that the stresses in TSVs in a free-standing wafer are more of a reliability concern than the stresses in TSVs in a stacked-die packaging configuration. The presence of compressive stresses induced due to the shrinkage of various components, particularly the mold compound, is beneficial to the reliability of TSVs. Therefore, current practice of reliability testing of TSVs in free-standing wafers is somewhat conservative, given that the TSVs are intended for stacked die packages. This observation is based on the comparative studies done between TSVs in a free-standing wafer against TSVs in the type of packaging configurations considered in this work. General conclusions can be drawn by performing systematic studies done similarly on other packaging configurations. Also, experimental reliability testing of TSVs in free-standing wafers as well as in packaging configurations will provide additional insight into the failure mechanisms.

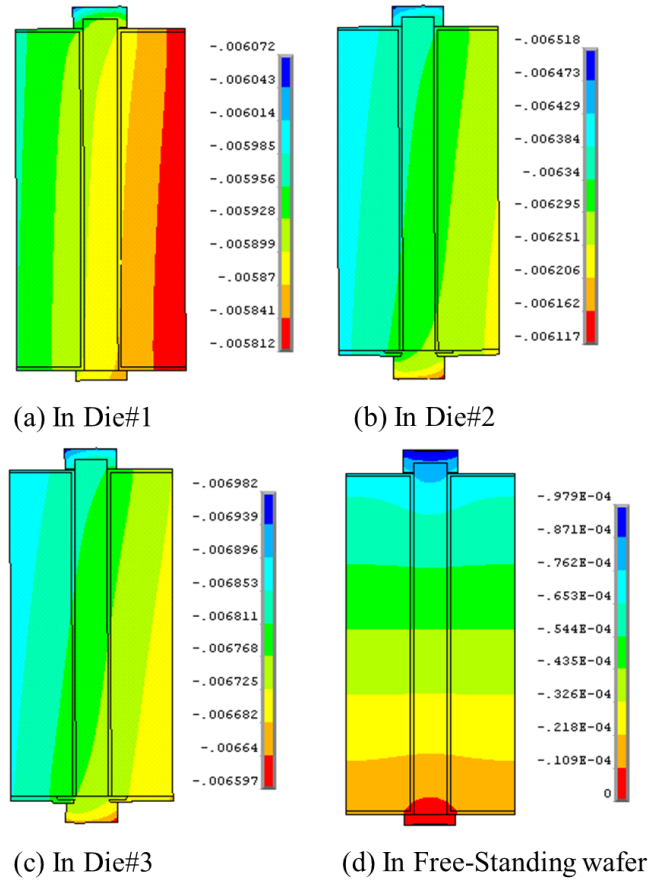


Figure 6.16: Displacement U_y of TSV in the 3D integrated package and in the free-standing wafers

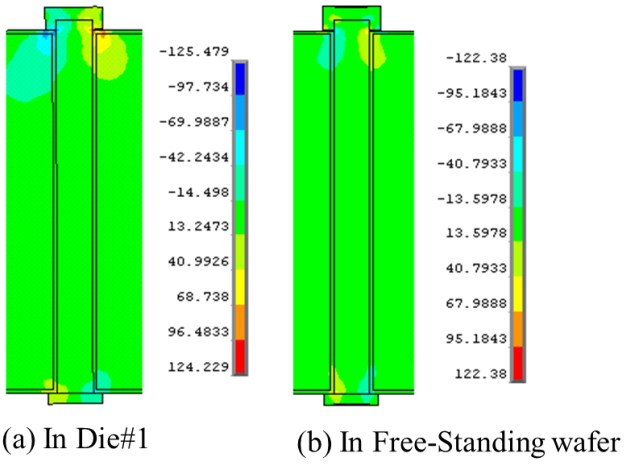


Figure 6.17: σ_{xy} distribution in TSV cross-sectional *xy* plane

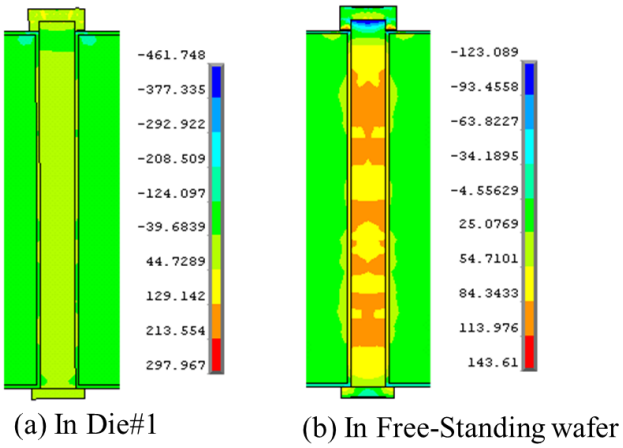


Figure 6.18: Radial stress in TSVs

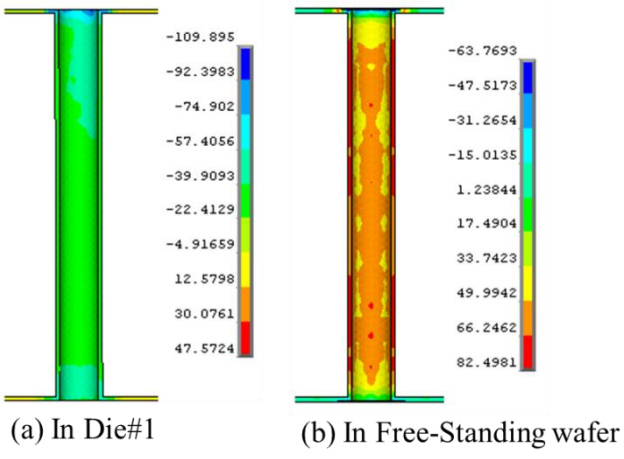


Figure 6.19: 1st principal stress in dielectric layers

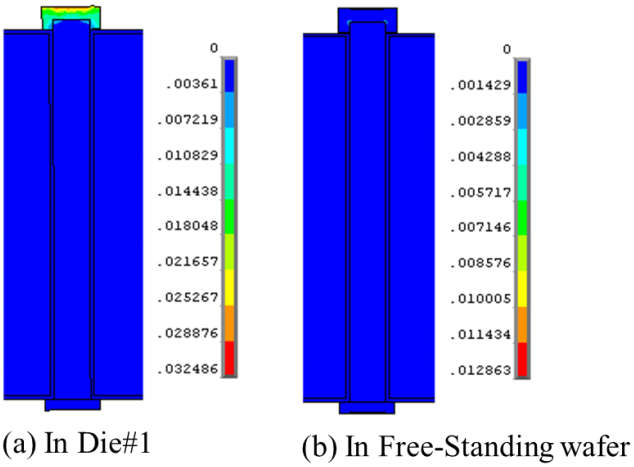


Figure 6.20: Equivalent plastic strain in TSVs

6.4 Parametric study and design guidelines

6.4.4 TSV/microbump in 3D integrated packages

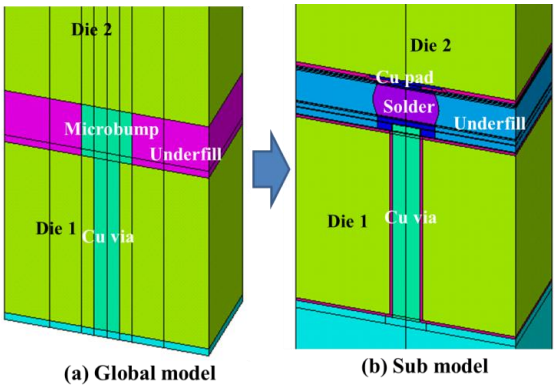
Design of simulation (DOS) based approach was utilized to understand the effect of various parameters (as listed in Table 6.7) on TSV/microbump reliability and to identify the critical factors that affect the TSV/microbump reliability in the integrated packages.

Figure 6.1 (b) shows the TSV structure in the global model where die 2 on the top, microbump region surrounded by an underfill, die 1 with TSV, and part of solder bump and underfill smeared region are shown. Figure 6.6 and Figure 6.21 shows the detailed submodel of the TSV where die 2 with its Cu pad, passivation layer, Cu pillars/solder, die 1, TSV with the liner material, and voids in TSV and underfill.

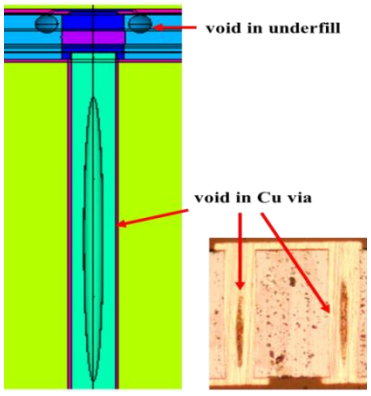
As discussed in Section 6.3.1, the maximum von Mises stress occurs in the Cu pillars, especially near the Cu pillar and solder interface, and Cu would yield in these regions. Figure 6.7 and Figure 6.8 shows the total strain distribution in the TSV, Cu pillar, and solders regions from the submodel. As seen, solder and Cu pillar near the solder interface experience high strains. Therefore, solder creep strain and Cu plastic strain near the interface were used as index to compare different designs in the DOE study. Also, in Section 6.3.1 we found the TSV/microbumps at the corners are more critical than the rest, thus the corner TSV/microbump of each design were used for the study, as shown in Figure 6.3 and Figure 6.22.

Table 6.7: Factors and levels of the design parameter screening for 3D integrated packages

Design factors	Levels		
Via diameter (μm)	5	10	15
Via pitch (μm)	50	65	80
TSV AP (H_{die}/D_{via})	5	7.5	10
Gap between dies(μm)	20	26	
Void in Cu Via	No void	With void	
Void in Underfill	No void	With void	
TSV array pattern	One-block	Four-block	
Microbump type	Cu pillar	Solder bump	
Underfill	***E*** (GPa) 2 @ +25C, 0.1 @ +250C ***CTE*** alpha 1 / alpha 2 60 / 160 ppm/C	***E*** (GPa) 7 @ +25C, 1 @ +250C ***CTE*** alpha 1 / alpha 2 30 / 60 ppm/C	
Mold compound	***E*** (GPa) 10 @ +25C, 0.1 @ +150C ***CTE*** alpha 1 / alpha 2 30 / 90 ppm/C	***E*** (GPa) 20 @ +25C, 1 @ +150C ***CTE*** alpha 1 / alpha 2 5 / 30 ppm/C	



(a) TSV and "Solder" type microbump in global and sub models



(b) Voids in TSVs and underfill

Figure 6.21: Model geometries

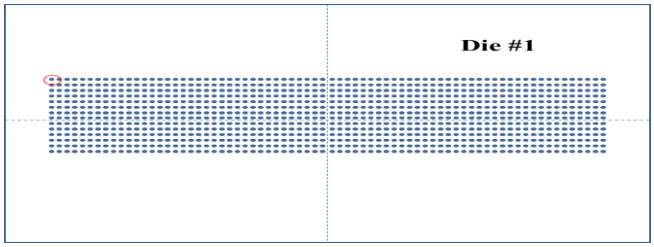


Figure 6.22: TSV array layout, "One-block" pattern

Using JMP software, as shown in Figure 6.23, 24 designs were generated base on the design factors and levels in Table 6.7. Equivalent solder creep strain and Cu plastic strain of the 24 cases were read out from the FE models and input into JMP.

Figure 6.24shows the effect test base on response of creep strain in solder. It can be seen that the dominating factors that affect solder creep strain are: "underfill materials", and "microbump type". On the other hand, as Figure 6.25 shows, if the response of equivalent plastic strain in the Cu pillars is considered, the dominating factors change to: "underfill material", "die to die gap size", "via aspect ratio" and "void in Cu via". "Void in underfill" is close to being critical for both creep strain response and plastic strain response.

Comparing the two kinds of responses in Figure 6.24 and Figure 6.25, we find the "void in the Cu via", which plays a dominating role in Cu reliability, has little effect on solder. Meanwhile, in the selected parameter range, "via aspect ratio" and "die to die gap size" are not dominating factors on solder either. It is also interesting to see that the TSV array pattern has negligible effect on both Cu and solder reliability.

The factor profiling results in Figure 6.26 shows that stiffer underfill with lower CTE greatly reduces the stress/strain in the solder and Cu. Stiffer mold compound increases the stress/strain, however, the effect is negligibly small. The solder bump design is more preferable than the Cu pillar design. The voids in underfill increase the stress/strain in the solder and Cu pillar, and should be avoided in the fabrication. And the

voids in Cu via increase the plastic strain in Cu, but slightly mitigate the creep strain in solder.

	Via diamete	Via pitch	Via aspect ratio	Underfill	Mold compound	TSV array pattern	Microbump type	Voids in Cu via	Voids in underfill	Die to Die gap
1	5	65	5	Low modulus	High modulus	Four block	Cu pillar	with voids	no void	25
2	15	80	7.5	Low modulus	Low modulus	Four block	Solder bump	with voids	with void	25
3	15	65	10	Low modulus	High modulus	One block	Cu pillar	with voids	with void	22.5
4	10	65	7.5	High modulus	Low modulus	Four block	Cu pillar	with voids	no void	20
5	10	50	10	High modulus	High modulus	Four block	Cu pillar	no Void	with void	22.5
6	10	80	5	Low modulus	Low modulus	One block	Cu pillar	no Void	with void	20
7	5	65	10	Low modulus	Low modulus	Four block	Solder bump	no Void	with void	20
8	10	65	7.5	High modulus	High modulus	One block	Solder bump	no Void	with void	25
9	5	80	10	High modulus	High modulus	One block	Solder bump	with voids	no void	20
10	10	50	10	Low modulus	Low modulus	One block	Solder bump	with voids	no void	25
11	5	50	7.5	High modulus	Low modulus	One block	Cu pillar	with voids	with void	22.5
12	15	50	5	High modulus	High modulus	Four block	Solder bump	with voids	with void	20
13	10	80	7.5	Low modulus	High modulus	Four block	Solder bump	no Void	no void	22.5
14	15	80	10	High modulus	Low modulus	Four block	Cu pillar	no Void	no void	25
15	15	50	7.5	Low modulus	High modulus	One block	Cu pillar	no Void	no void	20
16	15	65	5	High modulus	Low modulus	One block	Solder bump	no Void	no void	22.5
17	5	80	7.5	High modulus	Low modulus	Four block	Solder bump	with voids	with void	22.5
18	10	80	5	Low modulus	High modulus	One block	Solder bump	with voids	no void	22.5
19	5	50	5	High modulus	Low modulus	One block	Solder bump	no Void	with void	25
20	5	50	7.5	Low modulus	High modulus	Four block	Solder bump	no Void	no void	25
21	10	80	5	High modulus	High modulus	Four block	Cu pillar	with voids	with void	25
22	5	80	10	Low modulus	High modulus	One block	Cu pillar	no Void	with void	20
23	5	50	5	Low modulus	Low modulus	Four block	Cu pillar	no Void	no void	22.5
24	10	50	10	Low modulus	Low modulus	Four block	Solder bump	with voids	with void	20

Figure 6.23: DOS design table of 3D integrated packages

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Underfill[Low modulus]	0.0174758	0.001059	16.50	<.0001*
Microbump type[Cu pillar]	0.0062901	0.001042	6.03	0.0002*
Voids in underfill[no void]	-0.002389	0.001059	-2.26	0.0505
Via diameter*Via diameter	0.0048203	0.002137	2.26	0.0505
TSV array pattern[One block]	0.0021027	0.001042	2.02	0.0744
Die to Die gap*Die to Die gap	-0.003335	0.002184	-1.53	0.1611
Via diameter(5,15)	0.0019072	0.001323	1.44	0.1834
Mold compound[Low modulus]	-0.001441	0.001036	-1.39	0.1977
Via pitch*Via pitch	-0.002859	0.002366	-1.21	0.2577
Die to Die gap(20,25)	-0.001455	0.001294	-1.12	0.2899
Via pitch(50,80)	0.0008139	0.001187	0.69	0.5100
Via aspect ratio*Via aspect ratio	0.0010854	0.002203	0.49	0.6341
Voids in Cu via[no Void]	0.0002404	0.001036	0.23	0.8218
Via aspect ratio(5,10)	0.0001018	0.001283	0.08	0.9385

Figure 6.24: Parameter effect estimate on creep strain in solder

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Underfill[Low modulus]	0.0144957	0.000431	33.60	<.0001*
Die to Die gap*Die to Die gap	-0.003614	0.00089	-4.06	0.0028*
Via aspect ratio(5,10)	0.0015646	0.000523	2.99	0.0151*
Voids in Cu via[no Void]	-0.00122	0.000422	-2.89	0.0179*
Voids in underfill[no void]	-0.000975	0.000431	-2.26	0.0501
Microbump type[Cu pillar]	0.0009266	0.000425	2.18	0.0570
Via diameter(5,15)	0.00112	0.000539	2.08	0.0675
Via pitch*Via pitch	-0.00198	0.000964	-2.05	0.0701
Via aspect ratio*Via aspect ratio	0.001662	0.000898	1.85	0.0971
Die to Die gap(20,25)	0.0008315	0.000527	1.58	0.1491
Via pitch(50,80)	0.0007554	0.000483	1.56	0.1526
Mold compound[Low modulus]	-0.000633	0.000422	-1.50	0.1680
Via diameter*Via diameter	0.0004824	0.000871	0.55	0.5931
TSV array pattern[One block]	0.0001817	0.000425	0.43	0.6789

Figure 6.25: Parameter effect estimate on plastic strain in Cu pillar

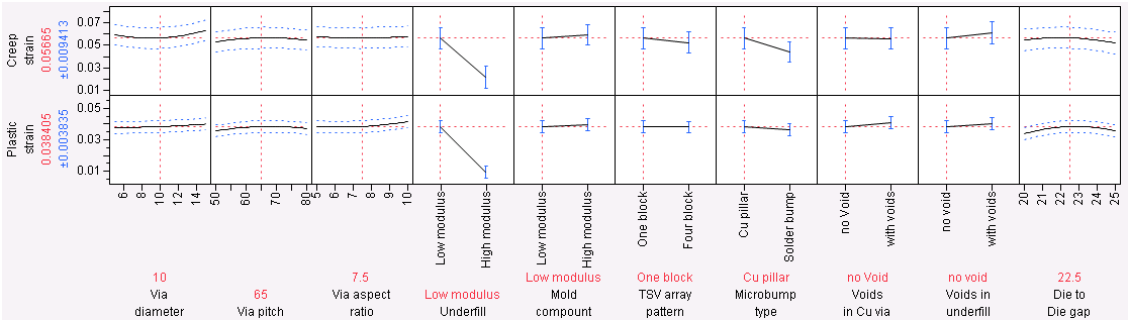


Figure 6.26: Factor profiling results of 3D integrated packages

6.4.5 TSVs in free-standing wafers

As shown in Figure 6.27, the models of TSVs in free-standing wafers have similar geometry and material as the submodels built for the 3D integrated packages. Different from the models for 3D integrated packages, coupled boundary conditions were applied on the two outer surfaces of the TSV cell models to mimic the periodic layout in the free-standing wafers. Since quarter models were built, symmetric boundary conditions were applied on the symmetrical planes. Also, the stress-free temperature for the TSV structure was taken to be 50 ℃ to mimic typical plating temperature as well as to correlate with XRD measurements, as reported in Section 2.2.1.

Stress/strain contours in Figure 6.28 show that both Cu and SiO_2 are highly stressed near the corners and Cu/SiO_2 interfaces. Potentially, Cu and SiO_2 would fail first in these regions, especially when fatigue loading is applied. Since Cu is ductile and SiO_2 is brittle in nature, Cu equivalent plastic strain and SiO_2 1^{st} principal stress near the

corners and interfaces were used as index to compare different designs in the DOS study. The design parameters are listed in Table 6.8. And the design table generated by JMP is shown in Figure 6.29.

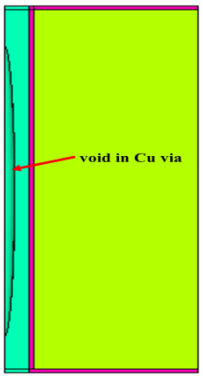
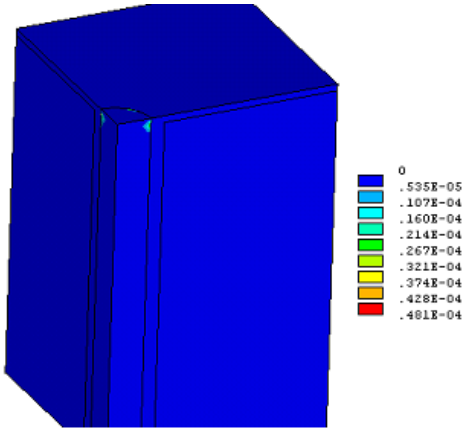
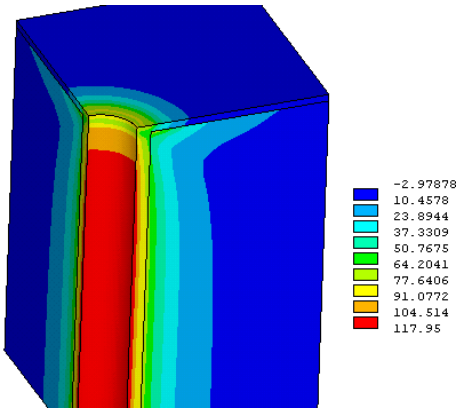


Figure 6.27: TSV in free-standing wafer



(a) Equivalent plastic strain distribution in at -40 ℃



(b) 1st principal stress distribution in SiO2/Si at -40 ℃ (Units: MPa)

Figure 6.28: Stress and strain contours of TSV in free standing wafer

Table 6.8: Factors and levels of the design parameter screening for TSV in free-standing wafers

Design factors	Levels		
Via diameter (µm)	5	10	15
Via pitch (µm)	50	65	80
TSV **AP** (H_{die}/D_{via})	5	7.5	10
Void in Cu Via	No void	With void	

	Via diameter	Via pitch	Via aspect ratio	Void in Cu via
1	5	50	7.5	no void
2	5	50	10	with voids
3	10	80	10	with voids
4	10	65	5	with voids
5	15	65	10	no void
6	5	80	10	no void
7	5	80	7.5	with voids
8	15	80	5	no void
9	15	50	5	with voids
10	15	65	7.5	no void
11	10	65	7.5	with voids
12	5	65	5	with voids
13	10	50	7.5	no void
14	15	50	10	with voids
15	10	50	5	no void
16	15	80	7.5	with voids
17	10	65	10	no void
18	15	50	10	with voids
19	5	50	5	no void
20	5	65	7.5	with voids
21	5	80	10	no void
22	15	65	5	no void
23	10	80	5	with voids
24	10	80	7.5	no void

Figure 6.29: DOS design table of TSV in free-standing wafers

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Void in Cu via[no void]	-0.000359	2.577e-5	-13.93	<.0001*
Via diameter(5,15)	0.0002281	0.000032	7.12	<.0001*
Via diameter*Via diameter	-0.000169	5.55e-5	-3.04	0.0078*
Via pitch*Via pitch	0.000105	5.55e-5	1.89	0.0767
Via aspect ratio(5,10)	0.0000188	0.000032	0.59	0.5655
Via aspect ratio*Via aspect ratio	-0.000018	5.55e-5	-0.33	0.7487
Via pitch(50,80)	-1.019e-5	0.000032	-0.32	0.7547

Figure 6.30: Parameter effect estimate on plastic strain in Cu in free-standing wafers

Sorted Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Via diameter(5,15)	11.14709	0.636117	17.52	<.0001*
Void in Cu via[no void]	3.3504031	0.5116	6.55	<.0001*
Via diameter*Via diameter	-6.675281	1.101788	-6.06	<.0001*
Via aspect ratio(5,10)	1.4078179	0.636117	2.21	0.0418*
Via aspect ratio*Via aspect ratio	-2.333521	1.101788	-2.12	0.0502
Via pitch*Via pitch	1.2493632	1.101788	1.13	0.2735
Via pitch(50,80)	0.3374887	0.636117	0.53	0.6030

Figure 6.31: Parameter effect estimate on 1st principal stress in of SiO_2 in free-standing wafers

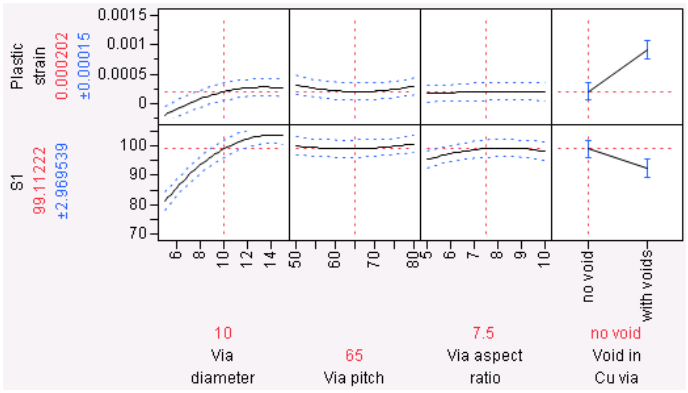


Figure 6.32: Factor profiling results of TSV in free-standing wafers

Figure 6.30 shows that both "void in Cu" and "via diameter" play dominating roles on Cu plastic strain. When stress in SiO_2 is considered, as shown in Figure 6.31, the "via aspect ratio" also plays an important role in addition to "void in Cu" and "via diameter".

As seen from Figure 6.32, although larger via diameter induces higher stress/strain in both Cu and SiO_2, it seems that the "sinking" of larger Cu via is more detrimental on surrounding SiO_2 than on Cu via itself. The "void in Cu" has opposite effect on Cu via and SiO_2. The introducing of void in Cu via creates a new stress concentration zone in Cu, resulting in higher plastic strain near these regions. However, since the void also reduces the amount of Cu, the effective CTE of Cu via decreases. The thermal mismatch between Cu and surround SiO_2/Si decreases, thus smaller pull force is

applied on surrounding SiO_2/Si at -40 ℃. Therefore, the existence of void in Cu via mitigates the stress in SiO_2. The above findings match previous study in Section 2.3.7.

Comparing the DOS study of free-standing wafers with that of 3D integrated packages in Section 6.4.4, it can be seen that the dominating factors for 3D packages are more related to the package levels factors, for example, “underfill materials”, “microbump type”, and “die to die gap size”, etc.

However, all the above DOE results are based on selected factor design range. Therefore, conclusions may not be valid if extrapolated out of the selected range.

In summary, following conclusion can be drawn based on the DOS study:

- Critical locations in the packaging configuration shift to the microbump region.
- Dominating factors for 3D packages are more related to the package levels factors, for example, “underfill materials”, “microbump type”, and “die to die gap size”, etc.
- Underfill material between dies is very important for TSV/microbump reliabilities. Also, voids in underfill should be avoided.
- Voids in Cu via affect the stress/strain locally, not as much on surrounding materials and other structures, such as microbumps.

CHAPTER 7

SUMMARY AND OUTLOOK

7.1 Summary and conclusions

Various experimental techniques and numerical analysis have been applied to fundamentally understand TSV reliability in free-standing wafers as well as in 3D integrated packages.

TSVs in free-standing wafers have been fabricated. Fabrication-induced defects, such as voids in Cu vias have been identified, and these voids result in higher daisy chain resistance. However, analysis shows that their effects on thermomechanical reliability are limited.

Thermal shock test results indicate that the TSVs connected with daisy chains in free-standing wafers are reliable up 4,500 cycles. Failure analysis shows that Si/SiO_2 cohesive cracking and Cu/SiO_2 interfacial separation are the dominating failure modes. Although the Cu/SiO_2 interfacial separations may not affect the electrical properties, they free the Cu/SiO_2 interface, and thus can result in greater Cu pumping at high temperature. Such Cu pumping may break redistribution layers and dielectric layers on top of TSVs. Cu cohesive cracking does occur at the Cu pad corners after 10,000 cycles, but only in a limited number of TSVs. As 4,500 cycles are well above the industry qualification requirements, the TSV structures fabricated in this study are thermomechanically reliable.

To understand the reasons behind different failure mechanisms, numerical facture models have been developed based on a proposed centered finite-difference approach (CFDA), which improves the numerical accuracy for energy release rate calculation and facilitates crack propagation analysis. Fracture analysis results successfully explain the causes of crack initiation and propagation directions observed in the experimental test.

Synchrotron XRD has been used for the full field in-situ micro-strain measurement of different TSV structures. For the first time, a data interpretation method based on beam intensity averaging has been proposed to understand this 3D to 2D strain measurement data projection process. The analysis shows that a direct comparison of the measured 2D strain distribution maps of different TSV samples may yield results dependent on artifacts related to sample preparation. Thus, another indirect comparison methodology has been proposed to compare different TSV designs. Comparison study shows that larger via diameters result in higher stress in the surrounding silicon because larger volume of copper available for CTE mismatch. Also, TSVs with thick polymer liners have lower stresses than TSVs with thin SiO_2 liners due to the cushion effect.

An analytical model has been formulated to study the warpage issue of 3D packages interconnected with TSVs. Simplified numerical models have also been developed for the warpage study during package assembly. Warpage analysis shows that the 3D packages with stacked dies behave similar to traditional single die flip-chip packages. Thus, for warpage study of 3D package with stacked dies, stacked dies can be simplified as single die with smeared properties for the single die. Assembly study of the double-sided flip-chip package indicates that high warpage may occur during the assembly process, which may affect the assembly of the followed components. Attaching the ring at the very beginning can effectively reduce the warpage during assembly.

Numerical models calibrated by experimental warpage measurement have been built to analyze TSV reliability in 3D integrated packages as well as in free-standing wafers. A design of simulation approach has been implemented for the parametric study. Results indicate that larger TSV diameter results in higher stress in surrounding SiO_2/Si. Whenever the via pitch is greater than twice the via diameter, the interference between vias is limited. Voids in Cu vias have larger effect on via reliability than on the surrounding SiO_2/Si. After the TSVs are integrated in the 3D package with two dies stacked and overmolded, TSV reliability is better than that in the free-standing wafer due

to thermomechanical effects from other components. In the 3D packages, microbump reliability is more critical than that of TSVs. DOS study of 3D package concludes that underfill material and microbump type are critical design parameters. Stiffer underfill with low CTE and solder bumps are preferred. In addition, voids during underfilling should be avoided.

7.2 Future work

The current research can be extended in the following directions:

- Although Cu has been widely adopted for the via filling, its thermomechanical reliability can be improved by using carbon nanotubes or metal nanowires for the interconnections (Figure 7.1). One of the challenges for this TSV design is how to achieve reliable bonding between the nanotube/nanowire to the contact pads.

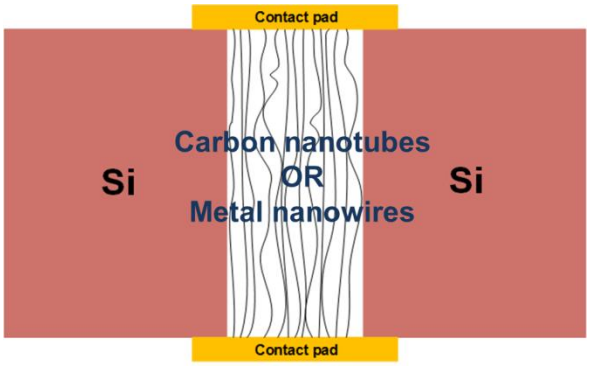


Figure 7.1: Other TSV design

- Other micro-strain measurement techniques should also be applied for the TSV strain measurement, for example, micro-DIC (Figure 7.2), micro-Raman, and indentation techniques. One challenge of these micro-strain measurements is acquiring reliable measurement data in micro-scale at different temperatures.

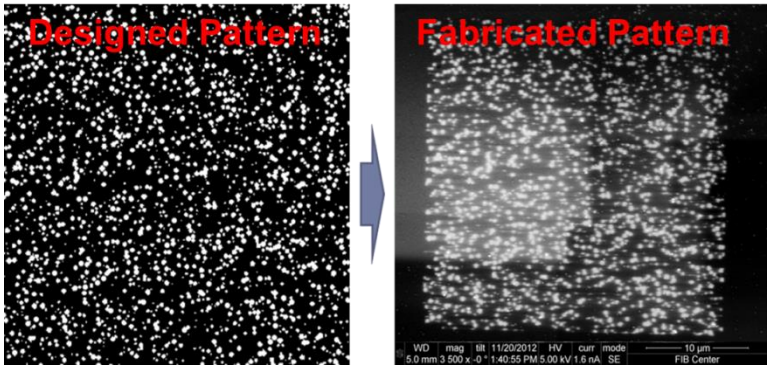


Figure 7.2: Micro-DIC pattern design

- Fabrication induced stress measurement is another interesting and important research topic. Monitoring residual stress step by step without interfering the fabrication process is a challenge.
- Cu/SiO_2 interfacial properties need to be characterized for more accurate failure analysis. However, as shown in Figure 7.3, accurately analyzing the scallop and waved surfaces between Si/SiO_2 and Cu is a challenge.

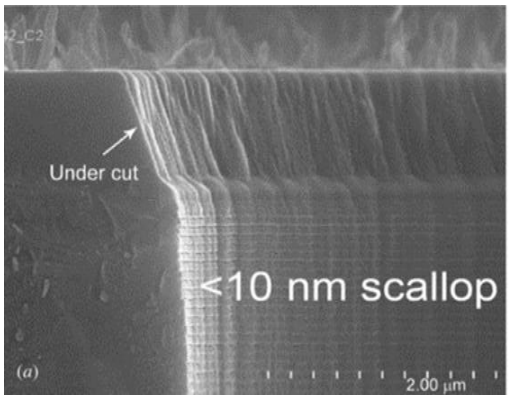


Figure 7.3: Scallop and undercut in etched via (Source: [16])

- Material thermomechanical properties characterization is essential for model input; especially for the copper, the properties of which change with different electroplating parameters.

APPENDIX A

PUBLICATIONS

A.1 Journal publications

- X. Liu and S. K. Sitaraman, “Analytical and Numerical Warpage Study of 3D Integrated Packages with Through-Silicon Vias," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, (to be submitted)
- X. Liu, M. Li, D. Mullen, J. Cline, and S. K. Sitaraman, "Experimental and Simulation Study of Double-Sided Flip-Chip Assembly with a Stiffener Ring, " *IEEE Transactions on Devices and Materials Reliability*, (revision submitted)
- X. Liu, P. A. Thadesar, C. L. Taylor, M. Kunz, N. Tamura, M. S. Bakir, and S. K. Sitaraman, "Dimension and Liner Dependent Thermomechanical Strain Characterization of Through-Silicon Vias using Synchrotron X-ray Diffraction, " *Journal of applied physics*, vol. 114, p. 064908, 2013.
- X. Liu, P. A. Thadesar, C. L. Taylor, M. Kunz, N. Tamura, M. S. Bakir, and S. K. Sitaraman, "Thermomechanical strain measurements by synchrotron x-ray diffraction and data interpretation for through-silicon vias," *Applied Physics Letters*, vol. 103, p. 022107, 2013.
- Y. Tian, X. Liu, J. Chow, Y. P. Wu, and S. K. Sitaraman, "Comparison of Sn-Ag-Cu Solder Alloy Intermetallic Compound Growth Under Different Thermal Excursions for Fine-Pitch Flip-Chip Assemblies," *Journal of Electronic Materials*, vol. 42, pp. 2724-2731, 2013/08/01.
- Y. Tian, J. Chow, X. Liu, Y. Wu, and S. Sitaraman, "Study of Intermetallic Growth and Kinetics in Fine-Pitch Lead-Free Solder Bumps for Next-Generation

Flip-Chip Assemblies," *Journal of Electronic Materials*, vol. 42, pp. 230-239, 2013/02/01.

- X. Liu, Q. Chen, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectronics Reliability*, vol. 53, pp. 70-78, 1/ 2013.
- X. Liu, Q. Chen, V. Sundaram, M. Simmons-Matthews, K. P. Wachtler, R. R. Tummala , and S. K. Sitaraman, "Reliability Assessment of Through-Silicon Vias in Multi-Die Stack Packages," *IEEE Transactions on Device and Materials Reliability*, vol. 12, p. 263, 2012.
- X. Liu, J. Zheng, and S. K. Sitaraman, "Hygro-Thermo-Mechanical Reliability Assessment of a Thermal Interface Material for a Ball Grid Array Package Assembly," *Journal of Electronic Packaging*, vol. 132, Jun 2010.

A.2 Conference publications

- Y. Tian, X. Liu, J. Chow, et al., "Comparison of IMC Growth in Flip-Chip Assembly with 100-and 200-μm-Pitch SAC305 Solder Joints," *63rd Electronic Components and Technology Conference*, Las Vegas, NV, May, 2013.
- X. Liu, M. Li, D. Mullen, J. Cline, and S. K. Sitaraman, "Design and assembly of a double-sided 3D package with a controller and a DRAM stack," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 1205-1212.
- X. Liu, M. Simmons-Matthews, K. P. Wachtler, and S. K. Sitaraman, "Reliable design of TSV in free-standing wafers and 3d integrated packages," in *ASME*

International Mechanical Engineering Congress and Exposition (IMECE), Denver, Colorado, USA, 2011.

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