

**HIGH- SPEED, HIGH-PERFORMANCE
WIRELESS AND WIRELINE APPLICATIONS USING
SILICON-GERMANIUM BICMOS TECHNOLOGIES**

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The Academic Faculty

by

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SUMMARY

The objective of the research in this dissertation is to demonstrate the viability of using silicon-germanium (SiGe) bipolar/complementary metal-oxide semiconductor (BiCMOS) technologies in novel high-speed, high-performance wireless and wireline applications. These applications include self-healing integrated systems, W-Band phased array radar systems, and multi-gigabit wireline transceiver systems. The contributions from this research are summarized below:

1. Design of a wideband 8-18 GHz signal source with the best reported tuning range and die area combination for self-healing applications [95].
2. Design of a robust, multi-band 8-10/ 16-20 GHz signal source with amplitude-locking for self-healing applications. A figure-of-merit (FoM) is proposed that combines tuning range and die area, and this work achieves the best FoM compared with state-of-the art [51].
3. First ever reported on-die healing of image-rejection ratio of an 8-18 GHz mixer integrated with the multi-band test signal source [52], [96].
4. Design of a 94 GHz differential Colpitts oscillator with 14% tuning range that spans 86-99 GHz for phased-array radar systems.
5. Identification of technology platform related bottlenecks in multi-gigabit wireline systems. A novel study of linearity of switching transistors in a current-mode logic (CML) gate.
6. A novel FoM that can be used to predict large-signal CML delay using small-signal Y-parameter techniques [97].

I INTRODUCTION

1.1 Origin and History of the Problem

Wireless communication devices consist of a radio-frequency (RF) front-end system (capable of detecting and receiving electromagnetic waves from the atmosphere) followed by a digital back-end system for signal processing. The RF front-end blocks today are capable of detecting signals from one gigahertz (GHz) to 110 GHz and beyond. The push in semiconductor research is to create high-performance, high-integration, and low-cost RF front-end blocks [1]. The preferred solution is to further integrate analog and digital applications onto one chip, which is the ultimate goal of SoC designs. SiGe BiCMOS technology makes this elusive goal a reality by providing high performance HBTs with switching speeds of 500 GHz, and scaled CMOS for compact digital and baseband processing. Examples of these highly integrated BiCMOS circuits have been demonstrated over the past few years, like Alcatel's 10 Gbps synchronous optical network (SONET) communication system, and Intersil's 11 megabits per second (Mbps) 802.11 wireless network solution [2].

Figure 1 provides a visual overview of the application space for SoC solutions ranging from cellular communication and automotive, to global positioning system (GPS) type navigation and defense applications involving radar systems [3]. The broad spectrum and diverse application set is testament to the immense potential for BiCMOS SoC solutions to demonstrate smaller chip size, lower cost, and improved manufacturability advantages over present day multi-chip solutions.

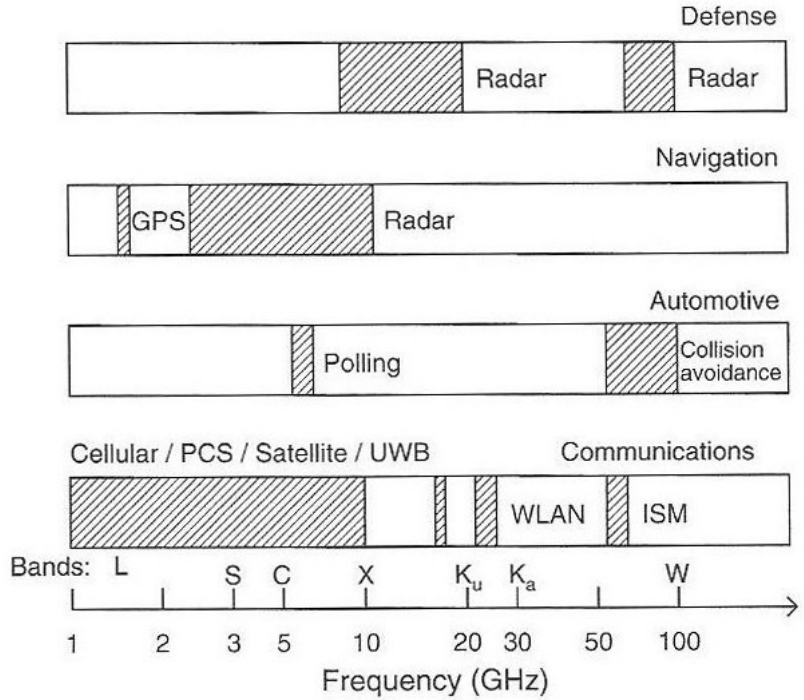


Figure 1. Application frequency bands for SiGe integrated circuits [3].

1.1.1 SiGe HBT Technology Overview and Critical Performance Metrics

The HBT concept was developed in the 1950s with H. Kroemer pioneering the theory behind using HBTs in 1957 [4]. The idea was to combine silicon and germanium to arrive at a narrower band gap that could be engineered to significantly improve performance over regular Si based bipolar-junction transistors (BJTs). It took almost 30 years after conceiving the HBT concept for the first SiGe HBT to be fabricated by IBM. The main bottleneck was the extremely difficult task of growing a thin and thermodynamically stable SiGe epi layer. The first generation high performance SiGe HBT was introduced in 1990 with a peak f_T (unity current-gain frequency) of 75 GHz. Since then, progress in SiGe device performance has been steady and spectacular as the technology has received considerable attention from industry and academia alike. State-of-the art devices today are capable of 300 GHz f_T and 500 GHz f_{max} (unity power-gain frequency). Sights have

been set for near terahertz operation in the coming years. Figure 2 plots some measured and estimated values for f_T with corresponding collector-emitter breakdown voltages (BV_{CEO}) of those devices generating the familiar $f_T \cdot BV_{CEO}$ Johnson's limit curve. The trend shows that device scaling necessarily involves a tradeoff between higher operating speed and lower device breakdown voltage.

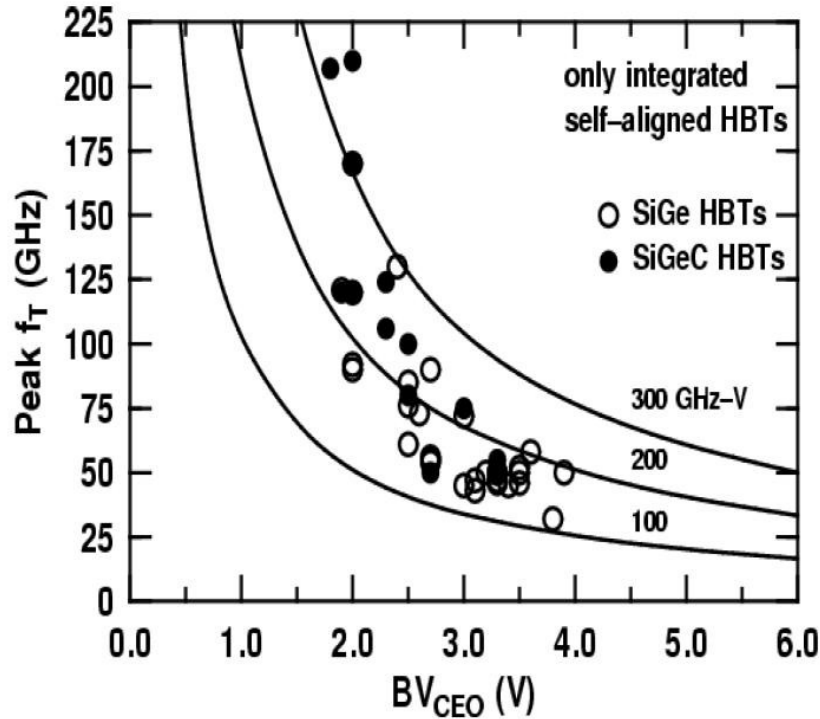


Figure 2. Measured and extrapolated f_T vs. BV_{CEO} data [4].

Figure 3 plots some current and projected f_{max} values demonstrating that SiGe devices are capable of delivering power at very high frequencies as well, which is critical for practical applications. As is seen in Figure 3, f_{max} and f_T are increasing in tandem with improvements in device scaling methods and advanced fabrication techniques. The reason for this simultaneous increase is because f_{max} is intimately tied to f_T by the following approximation:

$$f_{\max} \approx \sqrt{\frac{f_T}{8 \times \pi \times \tau_{cb}}}, \quad (1.1)$$

where τ_{cb} is the collector-base transit time.

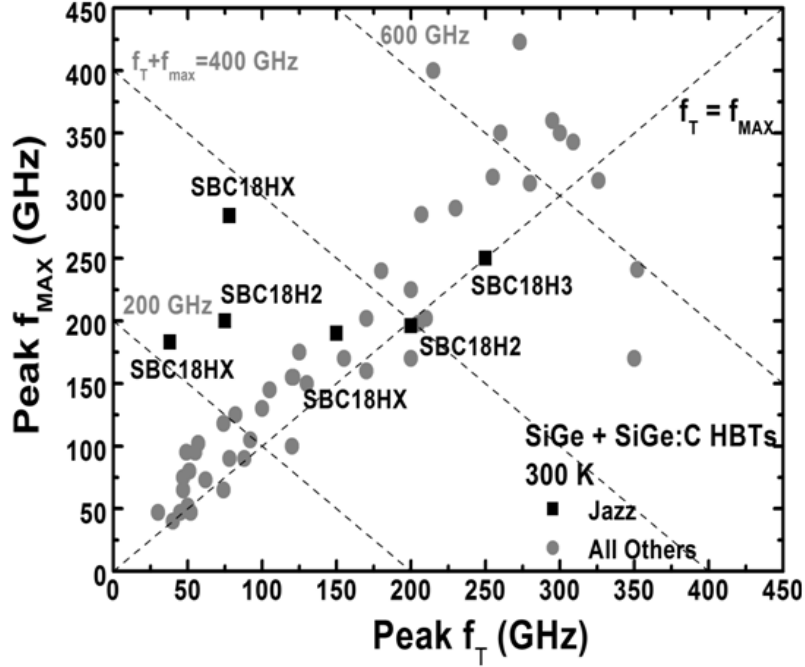


Figure 3. f_{\max} vs. f_T for SiGe Devices over the years and projections for future [4].

What these large f_T and f_{\max} values provide is the ability to push the upper bound on achievable system operating frequency. For example, the impetus in academia and industry today, is to develop low-cost (i.e. silicon based) radar systems that operate anywhere between 50-110 GHz. This development is clearly not possible without transistors that have a f_T of at least twice the operating frequency.

Another critical feature of a SiGe HBT is its noise performance, offering an inherently lower $1/f$ (flicker noise) corner frequency compared to CMOS devices. Flicker noise is usually characterized by the corner frequency (f_c) figure-of-merit given by

$$f_c = \frac{K \times J_c}{2 \times q \times \beta}, \quad (1.2)$$

where β is the transistor current gain, J_c is the current density, K is the flicker-noise coefficient, and q is the unit electric charge.

Figure 4 provides a comparison of residual phase-noise performance between a first generation SiGe device and a comparable Si BJT device. The impact of this figure-of-merit (FoM) is noticeable when calculating noise figure of SiGe devices and circuits.

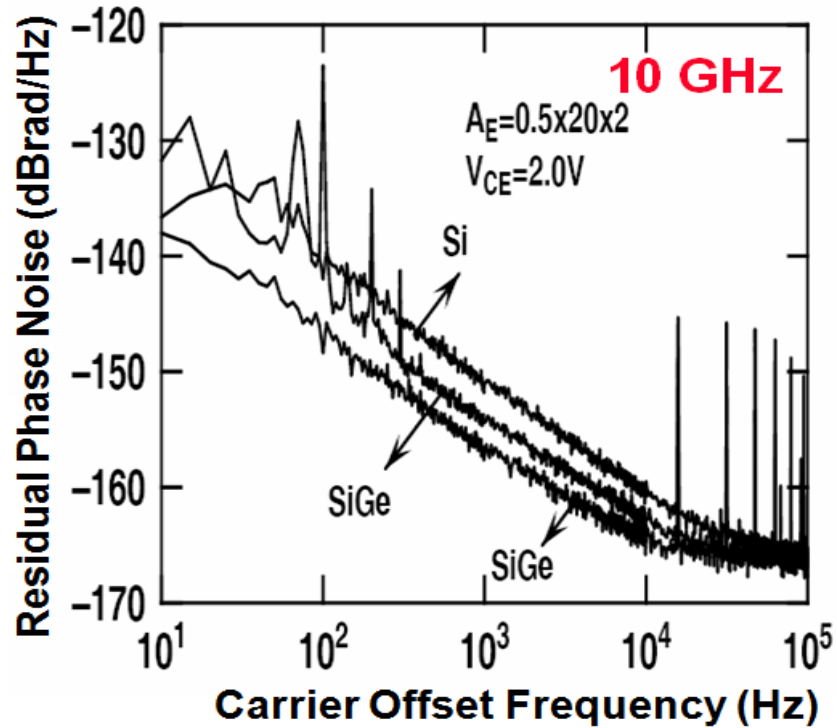


Figure 4. Residual noise comparison between SiGe HBT and Si BJT transistors [4].

As seen in Figure 4, the residual noise of an optimized SiGe HBT is -165 dBrad/Hz at a 10 kHz carrier offset, about 8 dB lower than a similar sized Si BJT. Lower noise contribution from individual transistors goes a long way in reducing the overall noise figure of the system.

1.1.2 Signal Generation Aspects in High-Performance Wireless and Wireline Applications

Frequency generation is one of the core functionalities of any wireless or wireline transceiver. The purpose of frequency generation and synthesis can vary depending on the application. For a wireless system, there is a need for local frequency generation to modulate and demodulate the signals of interest as depicted in Figure 5 [5]. In the case of modulation, the local oscillator (LO) signal is mixed with the baseband data signal to generate the modulated carrier. The reverse occurs during demodulation, where the incoming RF signal is demodulated by mixing with the LO, and transmitted to baseband for further signal processing. The oscillator is typically implemented inside of a phase-locked loop (PLL) to maintain strict spectral purity requirements. The LO signal frequency varies depending on the RF signal, which can be anywhere between 0.8-110 GHz in modern wireless systems [6]-[8].

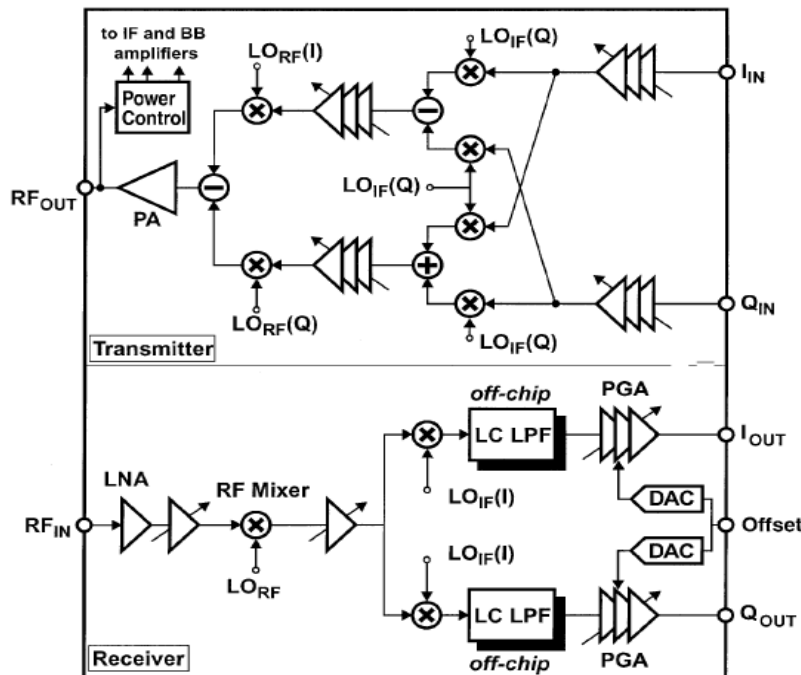


Figure 5. Wireless system depicting frequency modulation and demodulation [5].

A generic wireline transceiver is seen in Figure 6 with a PLL module on the transmit side and a clock and data recovery (CDR) module on the receive side to retrieve clock from the transmitted data [9]. Speed requirements of state-of-the-art wireline systems are usually characterized in multi-gigabits per second. Industry is routinely shipping backplane serial interconnects with 10 Gbps transfer speeds and is moving towards 40 and 100 Gbps nodes. SiGe is a strong contender in enabling these technological advancements with several recent reports of multi-gigabit transceivers [10]-[13].

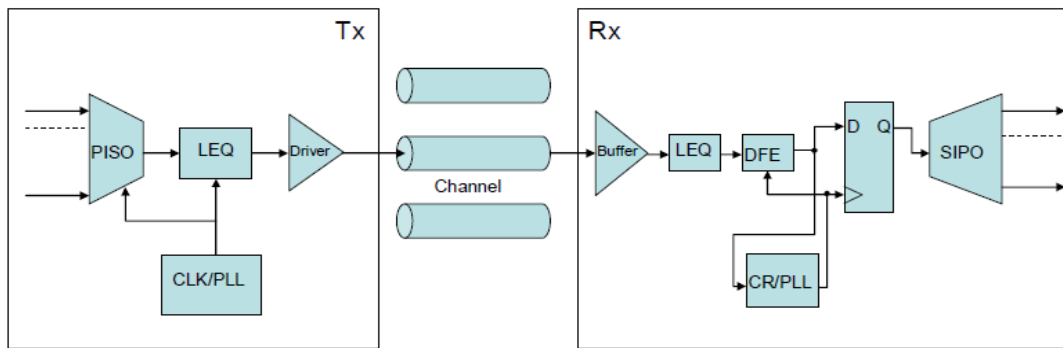


Figure 6. Wireline system depicting clock generation and recovery [9].

1.2 Purpose of the Proposed Research

The purpose of this research endeavor is to underscore the immense potential of SiGe BiCMOS technologies in advancing the capabilities of the semiconductor industry as a whole. In particular, SiGe helps to overcome the primary bottleneck of achieving high-speed, high-integration, and low-cost solutions simultaneously. In addition, SiGe technology is helping give rise to new markets and applications previously impossible for

silicon based platforms. Three such novel applications are addressed in this thesis spanning a wide range of industries, frequencies, and technical areas.

The first application area is self-healing, mixed-signal electronic systems. This application is motivated by the need to address semiconductor process yield issues from the view point of the circuit designer. It is well known that process parameters used by any foundry are subject to statistical variations, which in turn affect wafer to wafer, inter-die, and intra-die performance [14]. The application demonstrates enhancements made at the circuit level to overcome these variations and maintain system specifications across dies on a wafer and across wafers.

The second application area is millimeter-wave radar imaging systems. The ability to detect nearby objects on the scale of a few millimeters (mm) can be extremely advantageous for a variety of different reasons. Cloud profiling for climate and weather tracking, cancer cell detection for early diagnosis, and dust-cloud detection for safe landing of helicopters are just a few examples where millimeter-wave radars can find use.

The third application area is the development of robust multi-gigabit wireline transceivers. The IEEE P802.3ba 40 Gb/s and 100 Gb/s Ethernet Task Force was commissioned in June 2010 to propose technical standards that current and future wireline systems should satisfy. These include reliable 40 and 100 Gbps data transfer speeds to support local server applications and internet backbones respectively. Reliable achievement of these specifications at a low cost requires optimization of the bandwidth capability of existing serial data paths. This requirement translates to improved wireline circuit performance, which ultimately depends on the capabilities of the process

technology. Some of the challenges of process technology development for wireline applications are discussed in this section.

1.3 Organization and Contributions of the Dissertation

The dissertation is organized into three chapters, each dedicated to a particular application area. Each chapter begins with the motivation for the application area, followed by contributions made, and comparison to state-of-the-art.

In Chapter II, self-healing integrated systems are introduced as a technique to mitigate semiconductor process variations. Two wideband test signal sources are presented that are used to inject a tone into the RF signal path in order to perform local and global healing of RF path performance. On-die image-rejection healing is demonstrated for the first time by integrating the test signal with an image-reject mixer.

Chapter III addresses millimeter-wave phased-array radar applications at W-band frequencies (75-110 GHz). Some of the challenges associated with signal generation at these frequencies are discussed. The design of a 94 GHz differential Colpitts voltage-controlled oscillator (VCO) is presented that would be used to modulate the baseband signal and upconvert to W band.

Chapter IV looks at multi-gigabit wireline applications utilizing SiGe BiCMOS technologies. Technology benchmarking tools are discussed to evaluate the limits and bottlenecks for a given semiconductor process. A FoM is proposed that predicts large-signal CML gate delay using small-signal Y-parameter techniques. This FoM can significantly speed up the technology optimization cycle with quick feedback regarding the impact of any process tweaks on circuit performance.

II SELF-HEALING INTEGRATED SYSTEMS

2.1 Introduction

The concept of 'self-healing' dates back to the 1960s with the development of 'block-oriented' computers at Litton Industries [15]. The computers featured 'cellular redundancy' that ensured minimal impact on system performance in case of failure of any of the individual hardware cells. In addition, the computers would be reconfigurable through software algorithms that would disconnect the defective cells from the rest of the system. Hence, the original goal of self-healing was to overcome hardware failures using hardware redundancy and software algorithms. In subsequent years, self-healing appeared in the literature under various synonyms such as 'evolvable hardware,' 'adaptive circuits,' and 'anti-aging' [16]-[21]. Recent studies are emphasizing the need for self-healing in a wide variety of applications [22]-[52]. Some of these applications include communication and radar systems, sensor networks, smart power grids, robotics, genetics, and database systems. The overarching goal of self-healing in all of these use cases is to detect a system's present state and 'heal' to a desired state of operation. In the context of integrated electronics, technology scaling and operation under extreme environmental conditions are two important areas where self-healing can make a significant impact. These areas will be discussed in more detail below.

Over the years, aggressive semiconductor process technology scaling has enabled designers to integrate more transistors onto a single chip, resulting in low-cost electronics for end consumers. While scaling has proven to be extremely beneficial in most regards, one of the drawbacks of advanced scaling techniques is an inherent increase in the variations of process parameters [53]-[54]. This amplified variation in parameter values

directly translates to reduced circuit yield, which ultimately affects the profit margins of a business. A visual representation of the impact of scaling on system performance is depicted in Figure 7 [39].

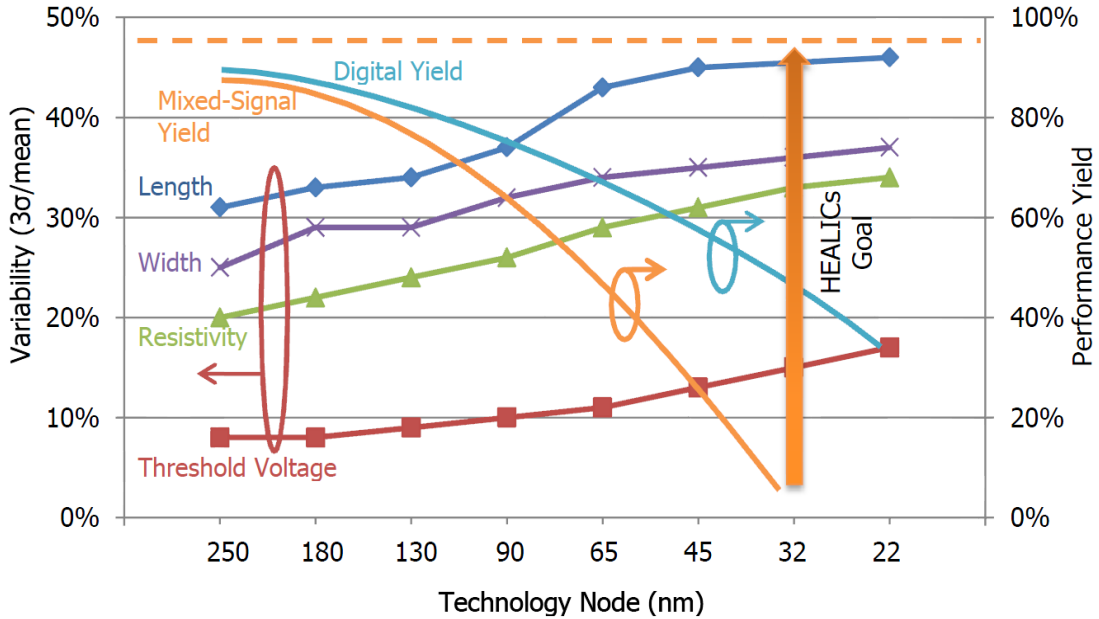


Figure 7. Variability in critical transistor parameters for submicron process nodes plotted alongside associated impact on performance yield for digital and mixed-signal circuits [39].

The percent variability in transistor parameters increases in more advanced technology nodes, consequently decreasing the associated yield for digital and mixed-signal circuits. Thus, there exists a need to overcome the yield issues associated with sustained scaling, so that designers can comfortably move to more advanced technology nodes. Self-healing, in this context, can prove to be extremely useful in recovering out-of-specification die and improving yield.

Communication and radar systems are routinely operated in environmental conditions such as those found in deep sea, deep underground, or in outer space, where

the systems are subject to extremes in temperature, pressure, corrosion, vibrations, and radiation effects (so-called “extreme environments” [55]). Once installed, these systems are required to operate reliably for extended periods of time, while also experiencing accelerated aging due to extreme environment conditions (e.g., via radiation damage in space systems). Regular repairs and maintenance in such extreme environments are impractical and cost prohibitive. In such applications, self-healing can be leveraged to potentially reconfigure a system rendered unusable by its environment and return it to a usable specification.

To achieve this ambitious goal of self-healing, the system should have the ability to detect its current state and heal itself to a new optimal state. In addition, it should achieve this self-healing without using hardware redundancy, in order to avoid power, die area, and cost overheads. This requires that one design for self-healing from the ground up in a way that is distinct from traditional design techniques. The critical blocks in the chain should incorporate ‘healing knobs’ that allow the healing algorithm the flexibility to tune RF performance, as required. As part of detecting its current state, a built-in-self-test (BIST) scheme is normally used at the system level, which requires a robust test signal source to be present to help calibrate across the intended bandwidth of operation [56]-[58]. A test signal of a known frequency and amplitude is injected into the RF chain at different points, as illustrated in Figure 8. The resulting baseband signal is then used to understand the present state and generate control signals to adjust the healing knobs of the individual blocks such as the analog-to-digital converter (ADC), low-noise amplifier (LNA), and mixer. This process of detection and correction is incrementally performed to eventually heal the complete system to an optimal state. It is important to note that self-

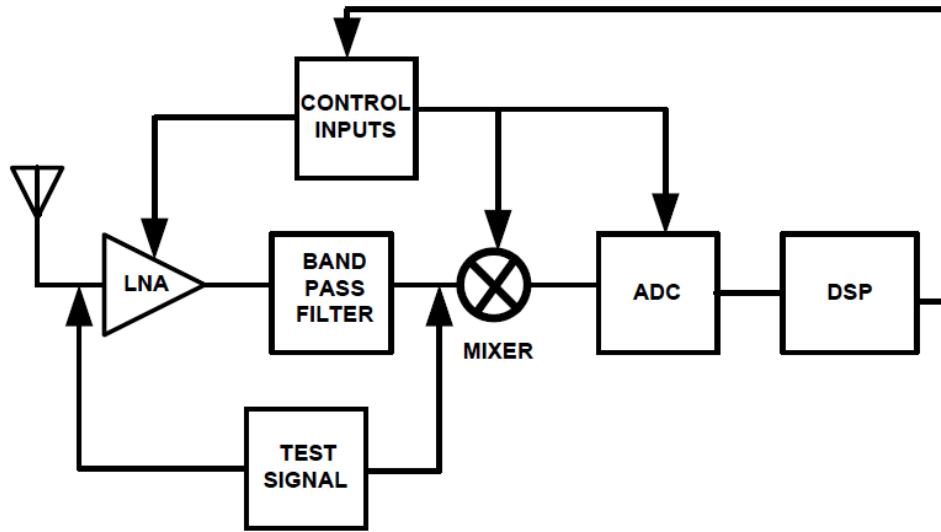


Figure 8. Conceptual calibration methodology for a self-healing system.

healing goes beyond simple BIST by adding a layer of hardware and software intelligence to the system that enables autonomous calibration. The present work seeks to showcase two wideband test signal source for on-die self healing of an 8-18 GHz (X to Ku band) receiver chain intended for use in radar applications. In order to exhibit healing, the second test signal source is integrated on die with a 6-20 GHz image-reject mixer. Automated IRR healing is performed on die as a demonstration of local block-level self-healing.

2.2 Wideband 8-18 GHz Signal Source with Shunt Peaking Inductors

2.2.1 Design Considerations

The top-level schematic of the first wideband ring oscillator is shown in Figure 9. The oscillator is a differential, four-stage ring with an output buffer to drive low impedances.

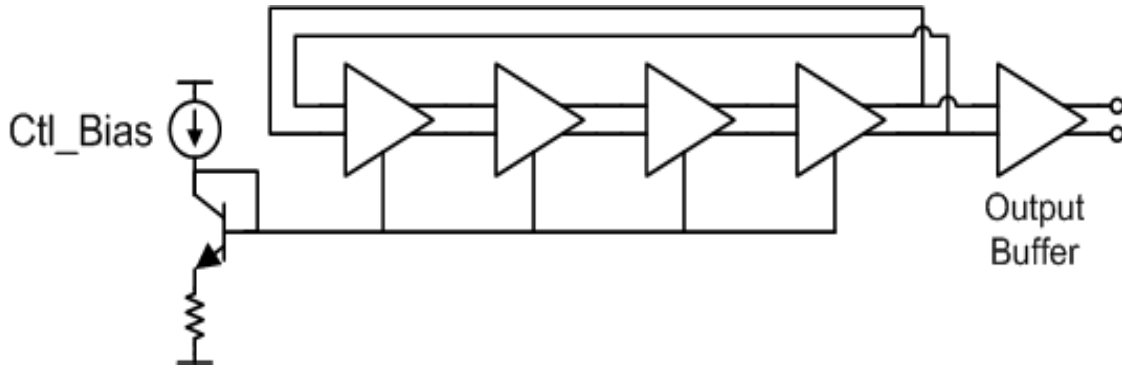


Figure 9. Top-level schematic of 8-17 GHz four-stage differential ring oscillator.

Each stage is comprised of a modified emitter-coupled logic (ECL) delay cell with shunt-peaking inductors for bandwidth enhancement, as depicted in Figure 10. The open loop transfer function of a ring oscillator is given by

$$H(j\omega) = [A(j\omega)]^N, \quad (2.1)$$

with $A(j\omega)$ representing the transfer function of the inverting stage and N being the number of stages. In order for oscillations to begin and be sustained in a ring oscillator, the open-loop gain must be greater than unity when the total phase shift around the loop is 2π radians.

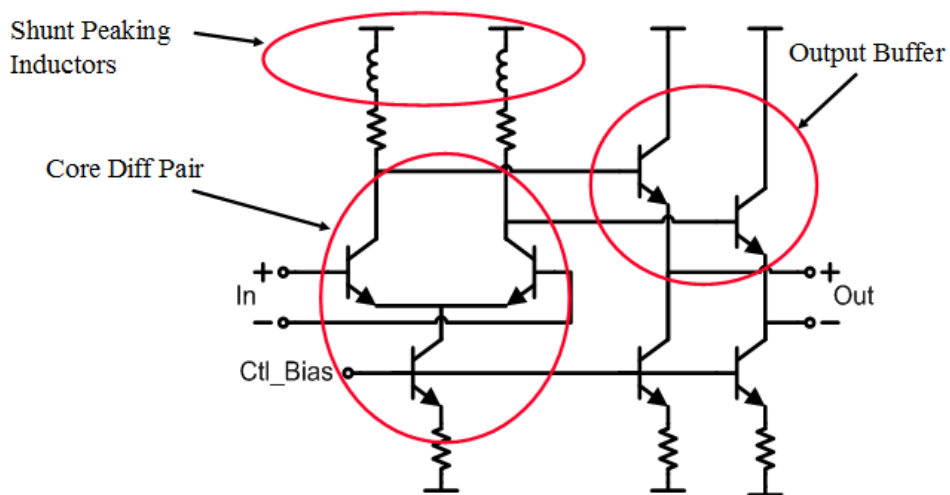


Figure 10. ECL delay cell with shunt peaking inductors.

Of the 2π radians total shift, π radians are contributed from the DC inversions that help avoid latchup conditions. The remaining π radians are contributed by frequency dependent phase shifts. These are the familiar Barkhausen criteria, and can be summarized by the following two equations:

$$|H(j\omega)| > 1, \quad (2.2)$$

and

$$\arg[H(j\omega)] = \pi. \quad (2.3)$$

The frequency dependent phase shift when divided across four stages sets the per-stage phase requirements to $\pi/4$ radians. The frequency at which this phase shift occurs is given by

$$\tan^{-1} \frac{\omega_{osc}}{\omega_o} = 45^\circ, \quad (2.4)$$

resulting in the condition that $\omega_{osc} = \omega_o$. This information can then be used to derive the per-stage gain requirements A_o as

$$\frac{A_o}{\sqrt{1 + \left(\frac{\omega_{osc}}{\omega_o}\right)^2}} = 1, \quad (2.5)$$

resulting in $A_o = \sqrt{2}$. The oscillation frequency for this ring oscillator is given by

$$f_{osc} = \frac{1}{2 \times N \times \tau_{delay}}, \quad (2.6)$$

where τ_{delay} is the delay through each ECL stage and N is the number of stages in the ring.

Bandwidth enhancement using inductors is a technique first explored in the 1930s during the early days of television [59]. The technique comes in two flavors, with the inductor being in series or in shunt with the load capacitance branch. The shunt-peaking

technique can provide close to 1.8X bandwidth enhancement. To understand this technique in a very intuitive manner, the inductor can be seen to introduce a zero in the output impedance of the delay cell, as given by the following simplified expression:

$$Z_{out}(s) = \frac{R[s(L/R) + 1]}{s^2 LC + sRC + 1}. \quad (2.7)$$

This zero offsets the complex pole introduced by the RLC network, making the load look more resistive over a wider frequency range. The complex valued pole pair in the right half of the s plane is what enables growing oscillations that are eventually limited by the nonlinear effects of the transistors.

2.2.2 Measurement Results

The frequency tunability is achieved by varying the tail bias current. The highest oscillation frequency of 17 GHz is achieved at a bias current setting of 1 mA, while the lowest frequency of 8 GHz occurs at a bias current of 9 mA. On-die measurements are performed using an output balun to convert differential signals to a single-ended form, which is then fed into a spectrum analyzer. Measured frequency and output power as a function of tail bias current are shown in Figure 11. A power switch made up of metal-oxide semiconductor field-effect transistors (MOSFETs) is also provided in the bias path, which can be turned on/off using the VSWITCH input. With 0 V input, the oscillator is in a low-power state consuming only 6 mW of DC power. With 3.3 V at the input, the oscillator consumes between 36 mW at 17 GHz and 185 mW at 8 GHz. One can say that the bias current is in fact the ‘tuning knob’ in the circuit that enables wideband operation.

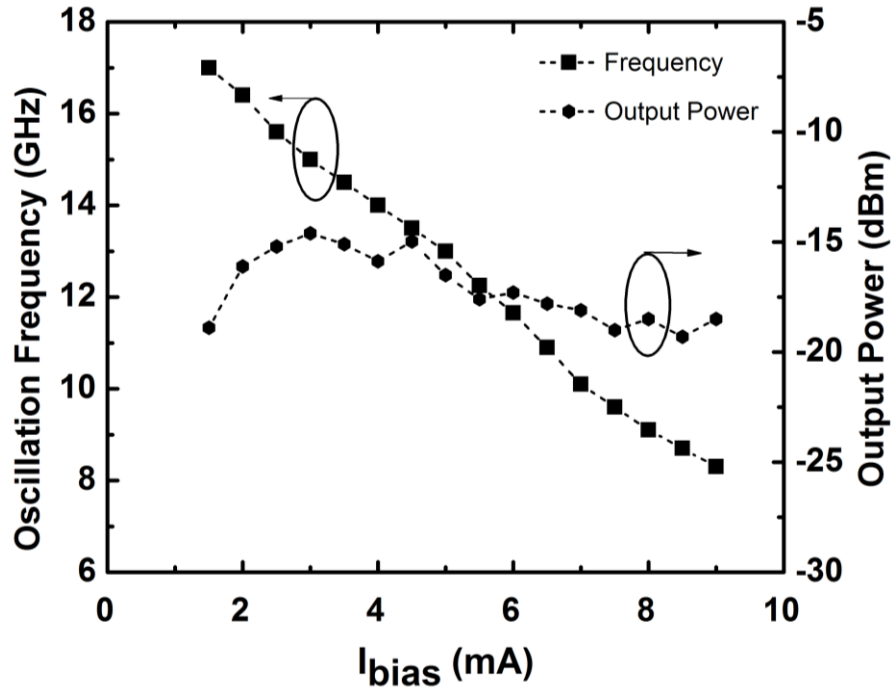


Figure 11. Measured frequency and calibrated output power vs. control bias current.

The die photomicrograph in Figure 12 shows the various pin outs and a size estimate of the circuit.

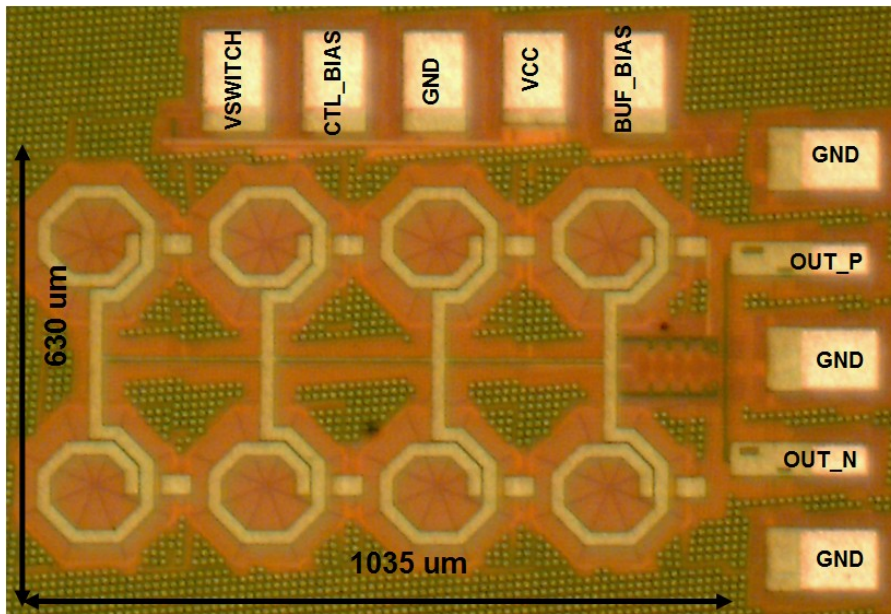


Figure 12. Photomicrograph of the ring oscillator with dimensions in μm .

2.2.3 Corner Simulations

Temperature and corner simulations are performed on the test signal using the foundry's corner models. The results are presented in Table 1.

Table 1 : 8-18 GHz Signal Source Process and Temperature Corner Simulations

Temperature	Slow Corner	Nominal Corner	Fast Corner
27 °C	49% (11-18 GHz)	76.9% (8-18 GHz)	92% (7.6-20.6 GHz)
-40 °C	52.7% (12-20.6 GHz)	73% (10-22.6 GHz)	95.8% (8.8-25 GHz)
85 °C	40.6% (10.6-16 GHz)	64% (8.5-16.5 GHz)	86.1% (7-17.6 GHz)

2.2.4 Comparison to State-of-the Art

Table 2 compares this work with state-of-the art signal sources across various performance metrics.

Table 2 : 8-18 GHz Signal Source Comparison to State-of-the Art

Reference	<i>Tuning Range</i> [GHz]	<i>% Tuning Range</i>	P_{diss} [mW]	Process	Active Area [mm ²]
[60]	13.75-21.5	43.9	130	InP	0.72
[61]	12-23	62.8	--	SiGe	0.44
[62]	8.7-13.8	45.3	32	SiGe	0.2
[63]	0.125-26	198	~1000	SiGe	4.4
[64]	9.9-21.9	75	~90	GaAs	2.66
This work	8-17	72	115	SiGe	0.65

This design offers the best combination of tuning range, area, and power dissipation compared with state-of-the art.

2.3 Compact Multi-Band Signal Source with Amplitude Locking

2.3.1 Motivation

Self-healing applications impose special requirements on the test signal used in the healing process. The most important characteristic of such a source would be its robustness to process and temperature variations. In addition, the source should be compact in size so as to meet die area constraints of the healing circuitry set by the system architects. For the intended application here, another important requirement is that the signal source be extremely wideband, spanning 8-18 GHz. Simultaneously meeting all these criteria requires that certain design choices be made concerning the topology of the signal source. While it is well-known that LC oscillators offer superior phase noise performance over ring oscillators for a given power dissipation [65], they occupy significantly greater die area due to the tank inductor. This tradeoff between phase noise and die area gets exacerbated when attempting to make the signal source wideband. Thus, a conscious choice was made to trade signal purity for compactness of design by choosing a ring oscillator topology. A key consideration here is the fact that the test signal has a very low duty cycle. In other words, the test signal is only turned on briefly during the healing process and then turned off during normal receiver operation. Hence, any phase noise degradation attributed to the ring topology can be recovered by dissipating additional DC power, with minimal impact on healing overhead targets. It is

noted here that a separate local oscillator (LO) is used for the mixer downconversion process. In addition, due to die area constraints, a phase-locked loop (PLL) was not implemented as part of the signal source.

The conceptual block diagram of the test signal source is shown in Figure 13, and it consists of a three stage differential ring oscillator, frequency divider, multiplexer, variable-gain amplifier (VGA), peak detector, op-amp, and digital-to-analog converters (DACs). The DACs are used to generate the frequency and amplitude tuning knobs. The signal source and DACs utilize 1.8-V, 3.3-V, and 4-V rails and a 100 μ A current source.

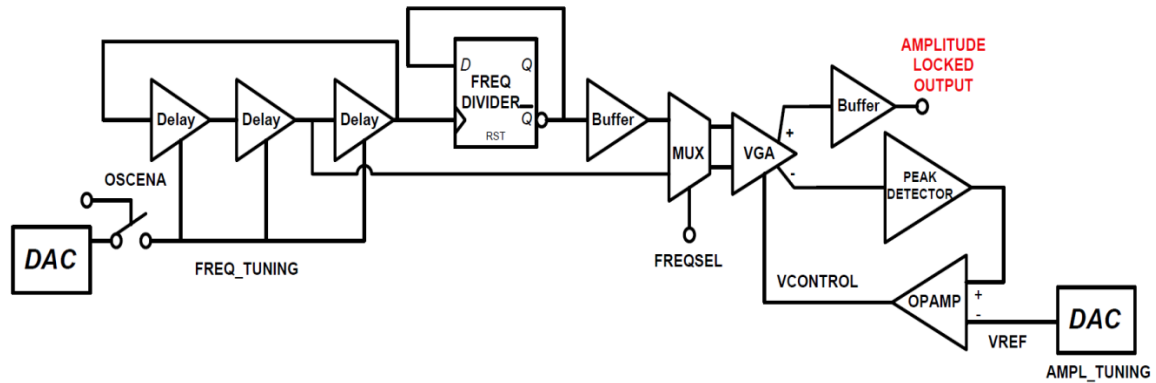


Figure 13. Block diagram of the amplitude-locked test signal source with DACs to provide tuning knobs.

2.3.2 Signal Generator Core

At the core of the multiband generator is a three-stage differential ring oscillator that is capable of generating frequencies between 16-20 GHz. Each stage consists of an emitter-coupled-logic (ECL) inverter with an emitter-follower buffer to maintain input/output signal levels. A static frequency divider synthesizes this oscillator signal to produce frequencies from 8-10 GHz. The divider, as well as the core ring outputs, are fed into a two-input multiplexer that enables band-select functionality. In-band tuning of frequency

is achieved by varying the tail current of the emitter-follower within each delay cell. Changing this tail current changes the transconductance of the emitter follower, which in turn tunes the pole at the output node of each delay cell. The stage delay is linked to oscillation frequency (f_{osc}) by equation 1.8.

The target signal amplitude of the signal source is -16 dBm when loaded by 50Ω . The ring oscillator, divider, and multiplexer blocks occupy only $300 \times 120 \mu\text{m}^2$ of die area. Uncalibrated spectrum plots of the signal source at 10.6 GHz and 18 GHz are shown in Figure 14 and Figure 15, respectively.

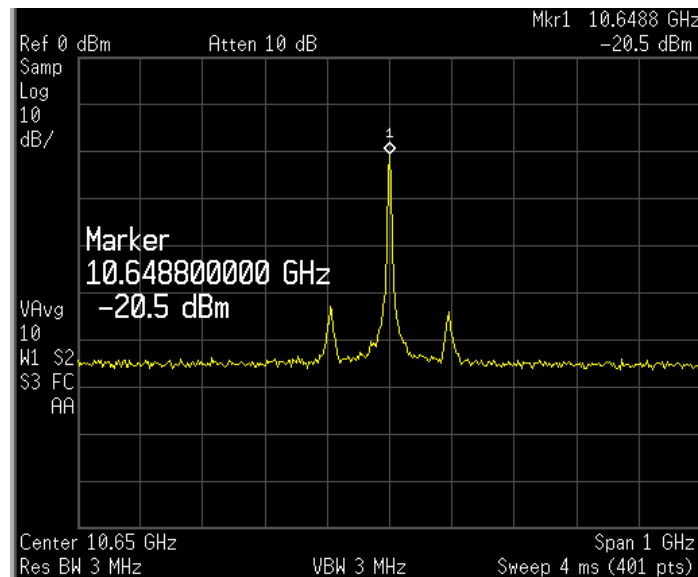


Figure 14. Spectrum of the test signal source at 10.6 GHz with an uncalibrated power level of -20.5 dBm.

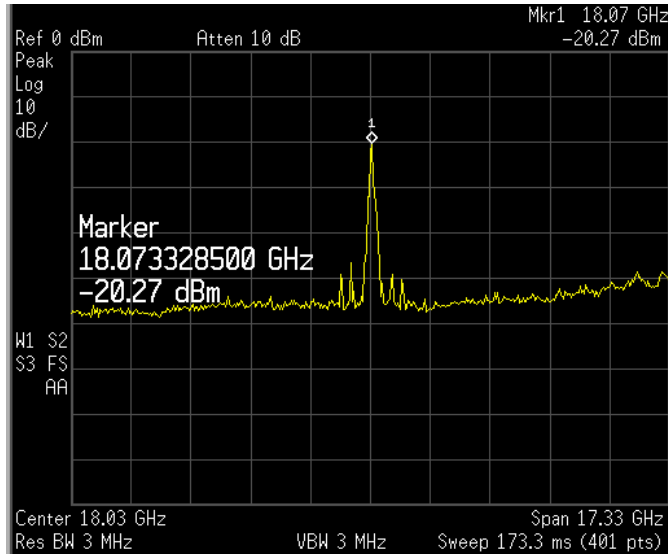


Figure 15. Spectrum of the test signal source at 18 GHz with an uncalibrated power level of -20.2 dBm.

2.3.3 Amplitude-Locked Loop

The amplitude-locked loop (ALL) adds an extra dimension of tuning, giving the user the ability to adjust test signal strength to avoid saturating the receiver chain, as well as mitigating the effects of process or environmental variations on signal amplitude. The amplitude locking is automated using a closed loop consisting of a VGA, peak detector, and op-amp. The VGA receives differential signals from the multiplexer. One of the outputs of the VGA is AC coupled into a low-power peak detector.

The VGA topology consists of a double-balanced Gilbert cell for four quadrant operation as shown in Figure 16. It consists of two differential pairs with their respective tail current sources to achieve both positive and negative gain conditions. The tail current of the right-side differential pair is fixed while the one on the left is variable. The V_{CTL} input is used to steer current between the two tail current sources and subsequently

achieve variable gain. When V_{CTL} is lower than V_{FIX} , most of the tail current is in the right branch and the VGA provides positive gain.

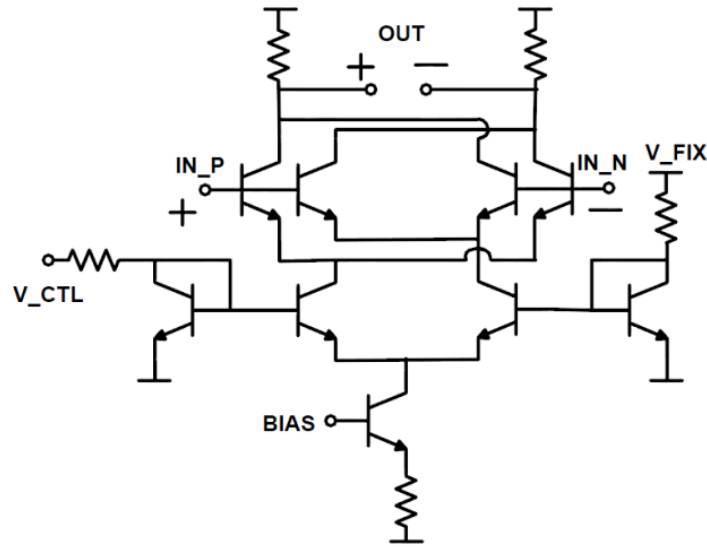


Figure 16. Schematic of the double-balanced VGA circuit.

When V_{CTL} equals V_{FIX} , the VGA gain is zero, and when V_{CTL} is greater than V_{FIX} , the VGA gain is negative. Thus, a smaller control signal corresponds to larger test signal amplitude and vice versa. The VGA provides 15 dB of gain control on the oscillator output signal.

The peak detector (Figure 17) utilizes a low-power, wideband topology consisting of a SiGe HBT acting as a non-linear rectifier and a holding capacitor, whose value is set based on the allowable output voltage droop [66]. The detector has a very wide linear dynamic range from 50 mV – 750 mV and consumes 200 μ A of current in each leg. In order to maintain a linear relationship between peak detector input and output for low input signal levels, the transistor and resistor sizes in the two branches are ratioed. In this case, the left transistor and biasing resistors are 2x in size compared to the offset cancellation branch on the right.

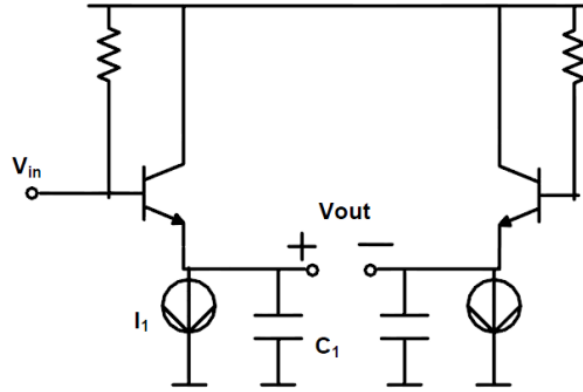


Figure 17. Schematic of the low-power peak detector circuit.

The detector accepts a sinusoidal input and produces an average DC voltage whose allowable droop is given by

$$\Delta(V_o) = -\frac{I_1}{C_1} \cdot \Delta t, \quad (2.8)$$

where Δt is half the period of the input signal. The detector is designed with a bias current of $220 \mu\text{A}$, which translates to an allowable droop of $593 \mu\text{V}$ at 9 GHz and $291 \mu\text{V}$ at 18 GHz . In addition, the frequency response of the peak detector is 47 GHz , which is more than sufficient to handle the entire bandwidth of interest, while consuming only 2.8 mW of DC power.

The opamp used in the feedback path of the ALL is a basic nFET input, two-stage amplifier with built-in Miller compensation that provides 62 degrees of phase margin and a unity gain cutoff frequency of 24 MHz . The opamp is designed primarily to drive low-capacitance, high-impedance nodes with a pull-down output drive of $800 \mu\text{A}$, while consuming 1.1 mA of quiescent current from a 3.3 V power rail. The complete circuit, including compensation, occupies a silicon area of only $60 \times 90 \mu\text{m}^2$, which is in line with the overall goal of minimizing die area.

The signal source and ALL together consume 30 mA of DC current at 8 GHz and 42 mA at 10 GHz from a 3.3-V rail.

2.3.4 Loop Transient Operation

The operation of the loop can be illustrated with the following test case. In steady state, for a given VREF of 1.6 V, the oscillator generates a 200 mV amplitude signal, which translates to a 1.6 V DC signal at the positive output of the peak detector. If VREF is now decreased, V_CTL increases until the peak detector output matches VREF. The effect of an increase in control voltage is to reduce the test signal amplitude, which then reduces the peak detector output until the detector's output equals VREF. The reverse occurs when VREF is increased. The range of values for VREF can be equated to the "locking" range of the ALL and is a function of the range of the peak detector output. On-die measurements are performed on the ALL to demonstrate its locking performance. Based on measured results over several die, the locking range is found to be between 1.5 and 1.8 V. The closed loop s-domain transfer function of the complete ALL system is given by

$$\frac{A_{OUT}(s)}{A_{DES}(s)} = H(s) = \frac{K}{1 + K} \cdot \frac{1 + \frac{s}{\omega_{PD}}}{1 + \frac{s}{\omega_{PD}}(1 + K)}, \quad (2.9)$$

where A_{DES} refers to the VREF signal applied, K represents the combined gain of the opamp and VGA, ω_{PD} is the pole of the peak detector, and the loop filter is assumed to be a simple gain block. This transfer function can be used to perform rudimentary stability tests on the ALL.

It is important to characterize the transient behavior of the loop to understand its impact on the overall healing process. The response time of each tuning knob translates to additional CPU cycles, which need to be accommodated into the budgeted cycles for

the healing routine. The transient response of the ALL at 9 GHz is captured in measurement (Figure 18) using a DPO71254C Tektronix oscilloscope with a 12.5 GHz analog bandwidth. A step change in the op-amp reference signal (VREF) is applied to the negative terminal of the op-amp, which translates to a lower VGA control voltage and a higher VGA output signal. The loop settling time is on the order of 150 μ s for the ALL which will need to be accounted for while calculating the overall CPU cycles needed for the healing algorithm.

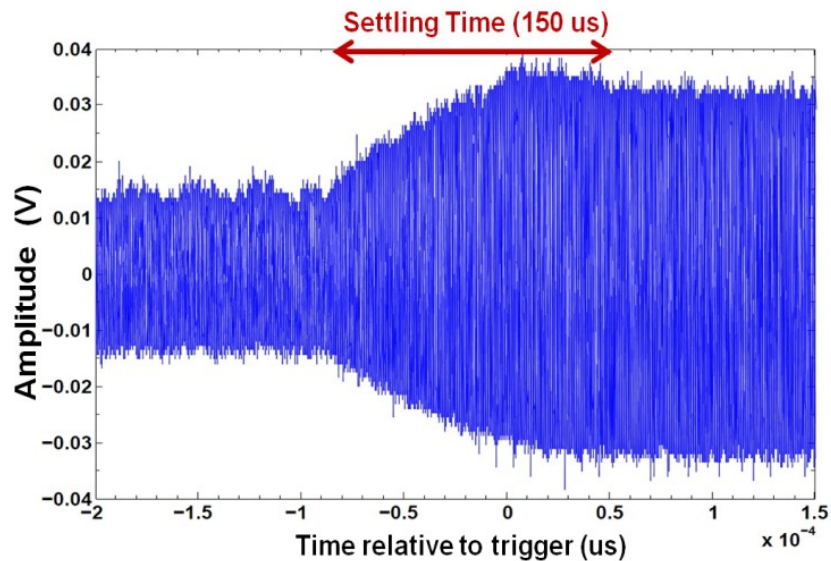


Figure 18. Measured loop settling time relative to the trigger point for the amplitude-locked loop. A step change in op-amp VREF voltage is applied, and the loop takes 150 μ s to settle.

2.3.5 Corner Simulations

Robust performance of the signal source is one of the important requirements for self-healing applications. In order to characterize variations in frequency over the extreme corners of process and temperature, simulations are performed in Cadence using the

corner models provided by the foundry and the results are shown in Figure 19 and Figure 20.

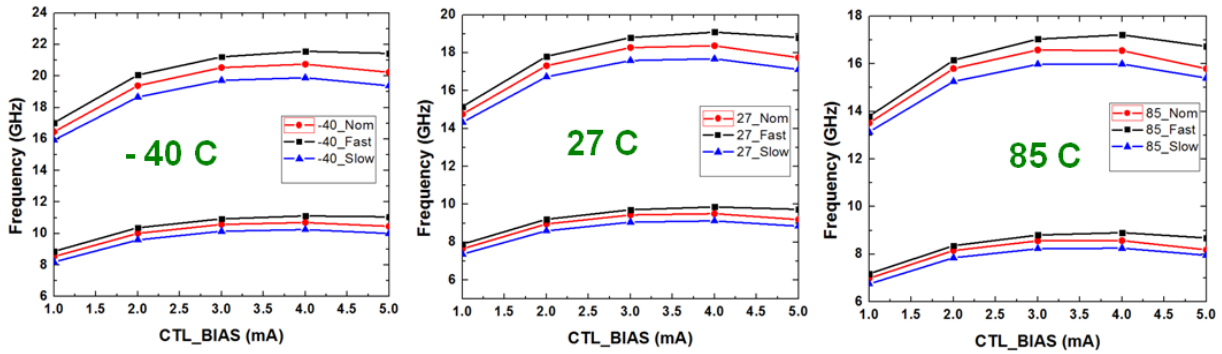


Figure 19. Process corner simulations over temperature capturing variations in frequency performance.

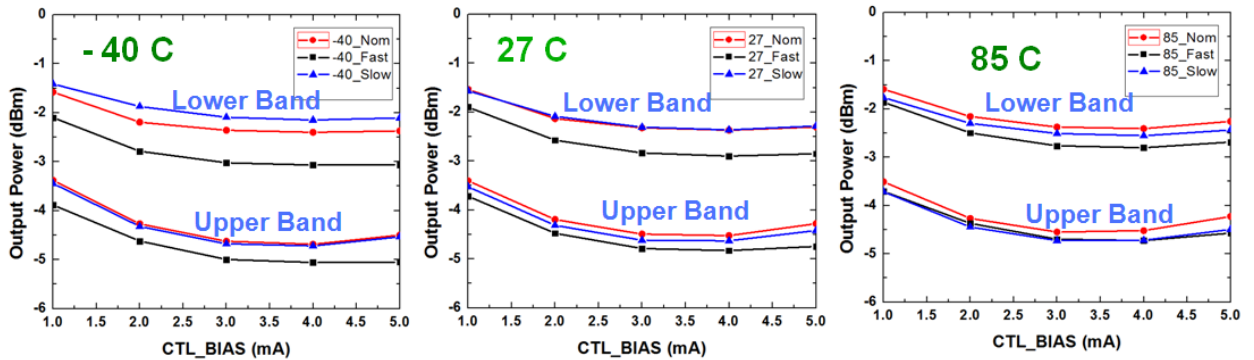


Figure 20. Process corner simulations over temperature capturing variations in amplitude performance.

Simulations reveal that the signal source is able to reliably generate the desired frequencies over military specifications for temperature range and process corners. The corner simulation results can also be utilized while performing the healing procedure to gauge which corner the die is performing in, and to set the ALL DAC codes accordingly.

2.3.6 Phase-Noise Performance

Phase noise performance of the signal source is important in the context of being able to resolve the test signal frequency during the healing routine. A custom delay-line discriminator based measurement setup (Figure 21) is used to obtain accurate close-in phase noise measurements of this free running signal source. The delay line de-correlates the noise in the RF and LO paths and translates frequency fluctuations into phase fluctuations. During the calibration procedure, a phase shifter is utilized to obtain quadrature phase between RF and LO signals in order to achieve maximum mixer gain. The mixer translates phase fluctuations into voltage fluctuations, which are then low-pass filtered and fed into the fast-fourier transform (FFT) analyzer.

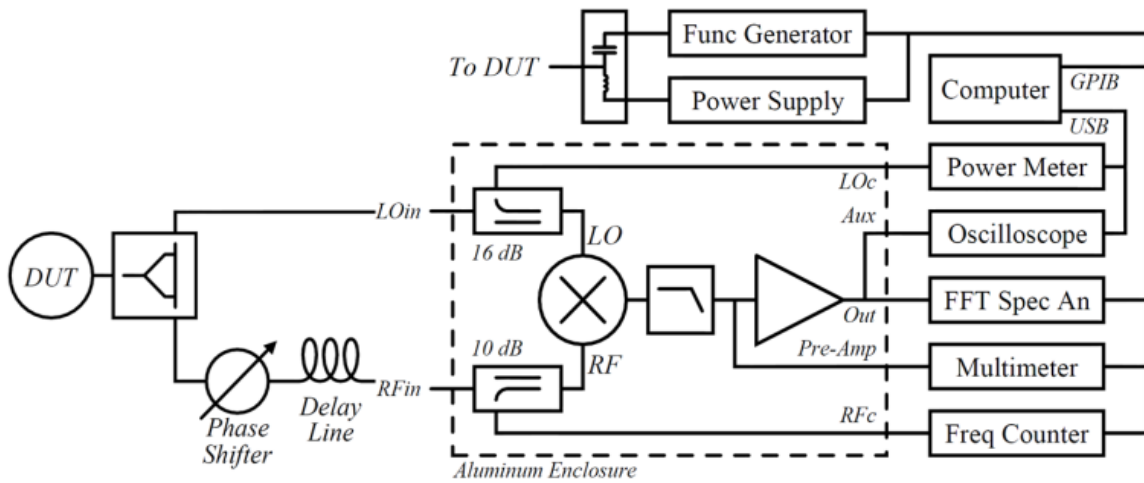


Figure 21. Delay-line frequency discriminator based custom phase noise measurement system

A custom MATLAB program controls all the equipment via GPIB and processes the FFT data in order to generate phase noise plots. A system calibration is first performed, prior to measuring phase noise on the DUT as shown in Figure 22. The phase noise of the DUT at 8.5 GHz oscillation frequency is -96 dBc/Hz measured at 1 MHz

offset from the carrier, as seen in Figure 23. Since this signal generator is not intended to be used as a reference signal for a mixer, the critical role of phase noise as it relates to maintaining channel selectivity and reducing crosstalk doesn't apply here. Thus, a design choice has been made to trade phase-noise performance for a wider tuning range, which is more critical for the intended application. From a BIST standpoint, the phase noise of the test signal source matters only so far as it translates to frequency resolution of the test signal. Frequency resolution ultimately determines the maximum sampling rate of the ADC that can unambiguously resolve the incoming test signal frequency, and is given by

$$FFT \text{ Bin Size} = \frac{f_s}{N}, \quad (2.10)$$

where f_s is the ADC sampling rate and N is the number of Fast-Fourier transform (FFT) points used. The sampling rate and FFT points should be chosen such that the FFT bin size is wide enough to accommodate the frequency instability of the oscillator.

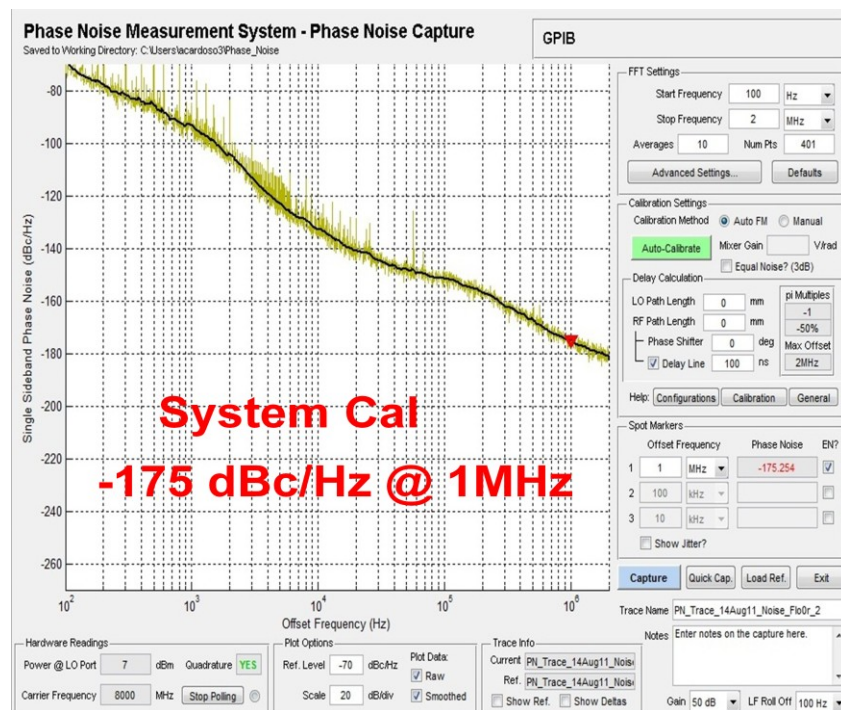


Figure 22. Phase-noise system calibration showing a -175 dBc/Hz system noise floor.

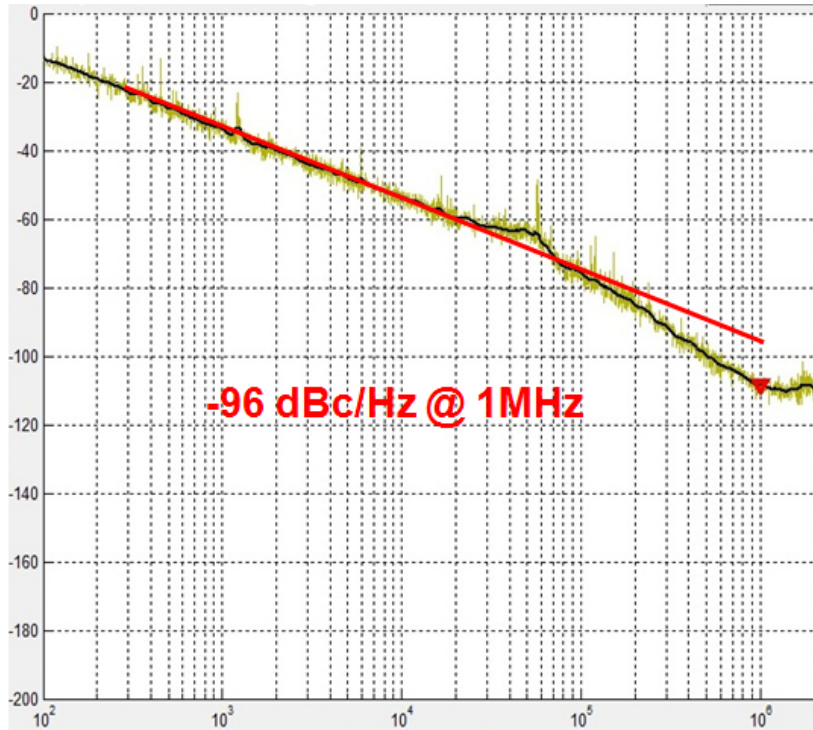


Figure 23. Measured phase noise of the signal source at 8.5 GHz.

2.3.7 Comparison to State-of-the Art

Table 3 compares this work with state-of-the art oscillators across various performance metrics.

Table 3 : Dual-Band Signal Source Comparison to State-of-the Art

Reference	<i>Tuning Range</i> [GHz]	Active Area [mm ²]	<i>FoM</i> [GHz/mm ²]	P_{diss} [mW]	Process
[67]	2.78-3.78	0.8	1.25	10.3	CMOS
[68]	--	0.3	--	0.36	CMOS
[69]	3.6-6	0.13	18.4	12.2	CMOS
[70]	4.9-5.9	0.502	1.99	~7.5	SiGe

[71]	6.78-7.19	0.66	0.62	3.7	CMOS
[72]	8-12	0.325	12.3	27	CMOS
This work	8.6-11.0 + 16.8-22.2	0.329	23.7	52	SiGe

A new FoM is proposed that combines two important test signal source parameters:

$$FOM = \frac{\text{Tuning Range (GHz)}}{\text{Core Die Area (mm}^2\text{)}} \quad (2.11)$$

A larger FoM represents a circuit improvement. Design II offers the best combination of tuning range and die area with a FoM of 23.7 GHz / mm².

2.4 Integrated Signal Source and Mixer for On-Die IRR Healing

In order to exhibit healing, the test signal source is integrated on die with a 6-20 GHz image-reject mixer. Automated IRR healing is performed on die as a demonstration of local block-level self-healing.

2.4.1 Image-Reject Mixer Topology

The image reject mixer (Figure 24) consists of a micromixer, followed by multi-tanh, elastic gm based VGAs in the in-phase (I) and quadrature (Q) paths. The mixer is designed to operate over 6-20 GHz RF input frequencies. The VGAs are used to control gain imbalances between the two paths in order to improve IRR. A two stage polyphase filter provides phase shifting and subsequent image cancellation at the output. Losses introduced by the filter are compensated with a backend VGA to produce a constant -5

dBm output power at an IF of 1.92 GHz. A differential LO is obtained externally and is converted to quadrature phases using a three stage polyphase filter. The mixer provides a tunable gain of 15-25 dB over the range of input frequencies with an OP1dB of 10 dBm. Further implementation and performance details of this mixer can be found in [49].

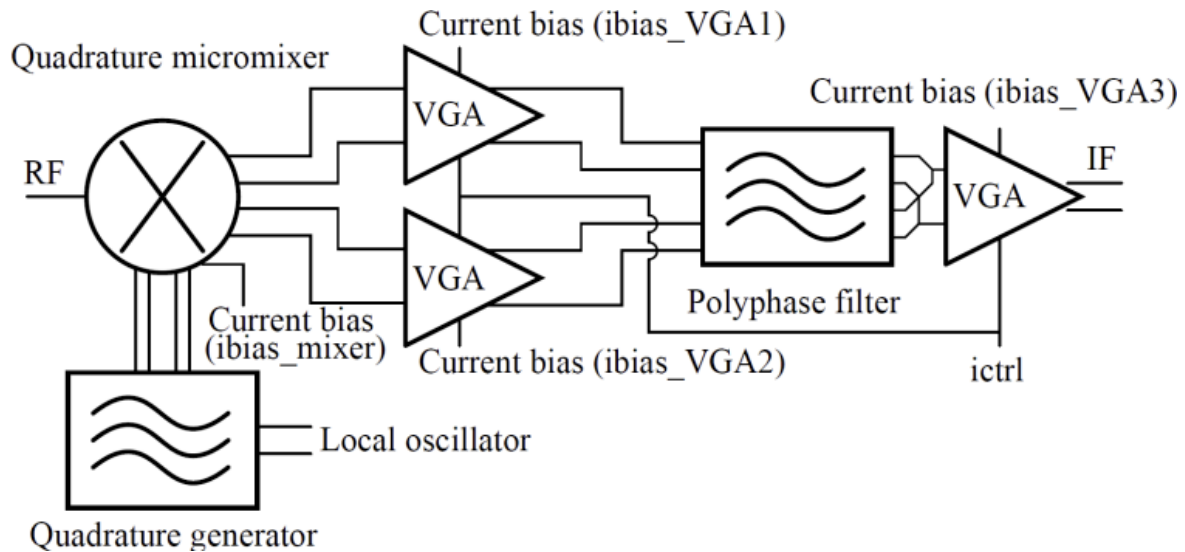


Figure 24. Mixer block diagram including micromixer, multi-tanh VGAs, and polyphase filters [49].

2.4.2 IRR Healing Test Setup

As a first step towards demonstration of automated on-die self-healing, the IRR of the image-reject mixer is healed using the test signal source. The integrated test signal source and mixer are on the same die and use on-chip DACs to generate the tuning knobs for both circuits. The measurement setup for the IRR healing is shown in Figure 25, with the portion marked in red representing on-chip components. A computer running MATLAB controls the signal source used for LO generation, the spectrum analyzer, and the programmable signal generator (PSG) via GPIB. The PSG is used to program the DACs, which generate tuning voltages and currents for the signal source and mixer. The signal

source uses one voltage DAC and one current DAC, while the mixer uses four current DACs. The DACs are 12 bit thermometer encoded with an R-2R ladder.

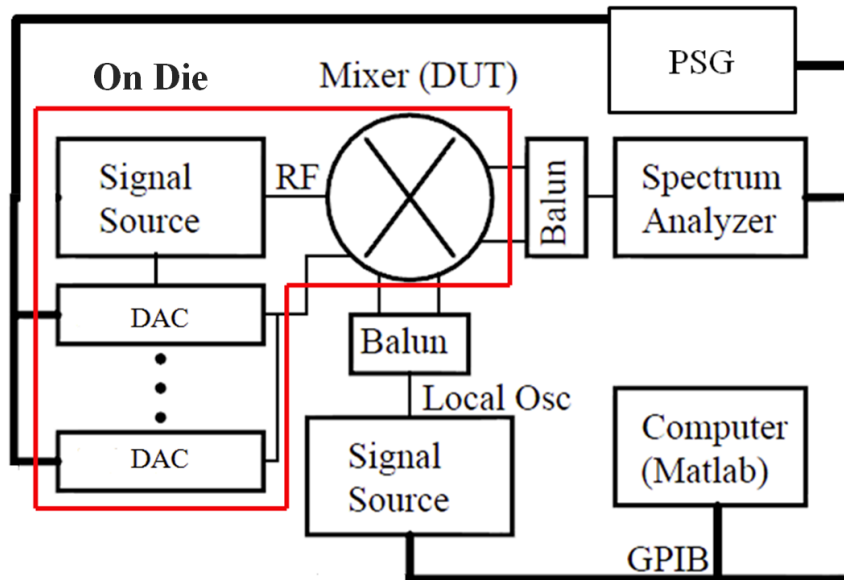


Figure 25. Measurement system for on-die IRR healing. The instruments are controlled via GPIB and a custom MATLAB algorithm is used to process FFT data and plot phase noise.

2.4.3 IRR Healing Algorithm

A custom MATLAB algorithm was used to implement the IRR healing routine and the logic is depicted in Figure 26. The first step in the algorithm is to set the RF frequency and obtain the desired IF frequency. The mixer is designed to operate with a low-side LO and thus the desired IF signal is when the LO is below the RF frequency. To emulate the image signal, the LO signal is tuned to a frequency above the RF at an offset frequency equal to the IF frequency. The current DAC of the signal source is programmed such that it produces the desired RF frequency, keeping in mind the possibility that the resultant RF frequency may not be precise. The LO is swept until an IF of 1.92 GHz is achieved as

captured by the spectrum analyzer. The actual RF frequency can then be calculated and any changes to the current DAC code can be made to adjust the RF frequency and obtain the desired IF frequency.

Once the RF and desired IF frequencies and corresponding power levels are recorded, the LO is moved to high side to emulate the image signal, and the corresponding power level of the image at IF is recorded. This first iteration of recording desired IF and image power levels is performed under nominal mixer bias settings with I and Q path VGA bias currents set to the same values ($\Delta I = 0$).

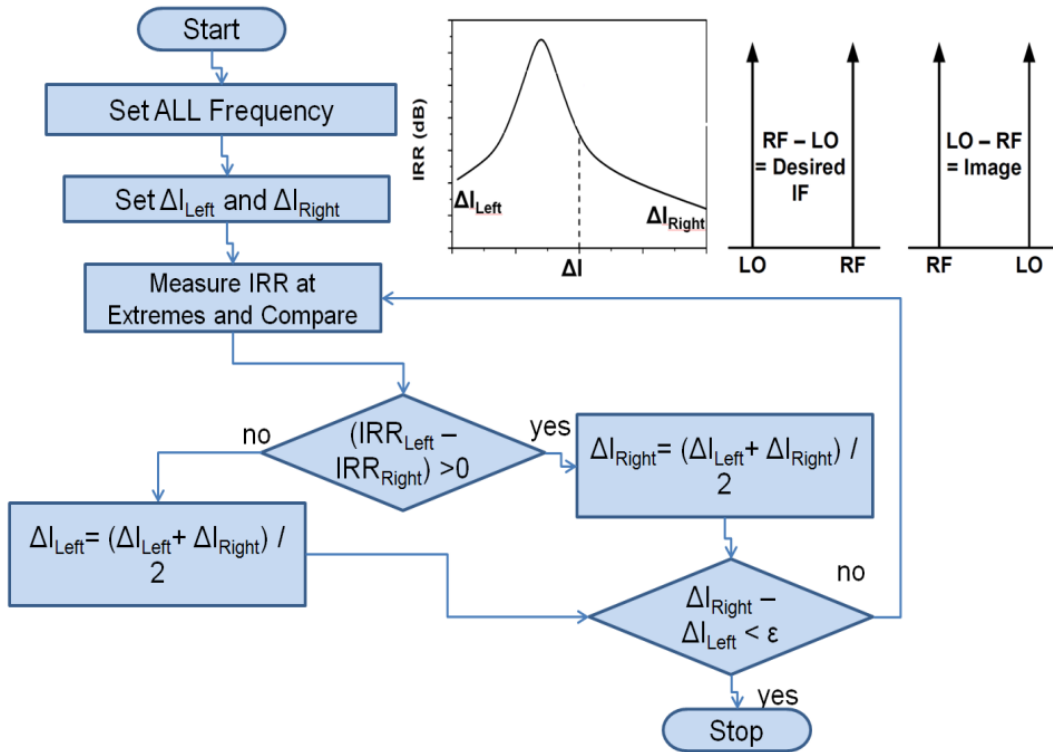


Figure 26. IRR healing algorithm that adjusts mixer I and Q path VGA bias currents to obtain a target IRR as required by system specifications.

The second step in the algorithm is to adjust the I- and Q-path VGA bias currents in order to heal the IRR by compensating for any gain imbalances in the two paths. Phase

imbalances are not addressed in the present mixer design. The algorithm starts by increasing the I-path VGA bias current to one extreme to obtain ΔI_{left} and then records IRR_{left} . This process is repeated with the Q-path VGA current to obtain ΔI_{right} and $\text{IRR}_{\text{right}}$. The IRRs at the two extreme bias settings are compared, and a decision is made whether to adjust the ΔI_{left} or ΔI_{right} value. If $(\text{IRR}_{\text{left}} - \text{IRR}_{\text{right}}) > 0$, ΔI_{right} is set half way between ΔI_{left} and ΔI_{right} . In the event that $(\text{IRR}_{\text{right}} - \text{IRR}_{\text{left}}) > 0$, ΔI_{left} is set half way between ΔI_{left} and ΔI_{right} . This iterative process of adjusting ΔI_{left} and ΔI_{right} is repeated until the difference between the two is less than a small, predefined ϵ value. At this point, the maximum IRR is achieved, the healing algorithm terminates, and the healed system resumes normal operation.

2.4.4 Measured IRR Healing Results

The algorithm was applied to a 9 GHz and 18 GHz RF signal, and IRR healing was performed at these two input frequencies for a wide range of IF frequencies between 1.2 - 2.8 GHz. The nominal IRR at 9 GHz and 18 GHz pre-healing are about 22 dB and 15 dB, respectively. Post-healing, the IRR at 9 GHz improved to 37 dB while the IRR at 18 GHz improved to 45 dB for 1.6 - 2.3 GHz IF frequencies, as shown in Figure 27. These are significant improvements from a system performance standpoint, and to the authors' knowledge is the first demonstration of such on-die automated IRR healing without the use of hardware redundancy.

The die photomicrograph of the integrated system is shown in Figure 28, and consists of the test signal source, image-reject mixer, DACs, and digital routing. The total area occupied by the die is $2.5 \times 2.6 \text{ mm}^2$ including the pad frame.

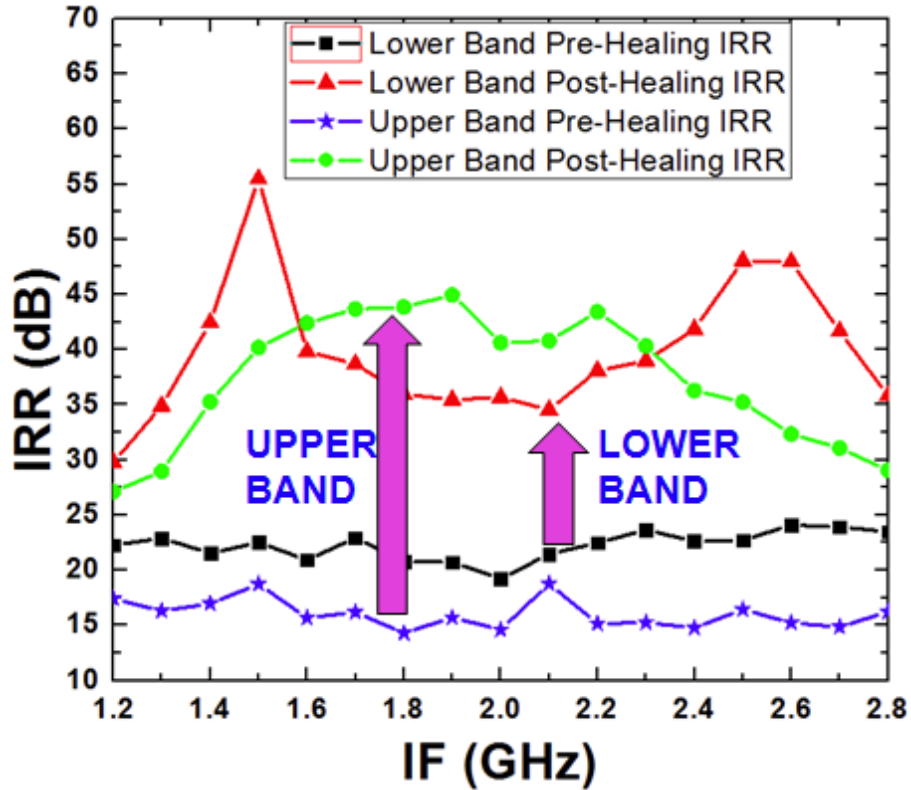


Figure 27. Measured IRR healing results for 9 GHz and 18 GHz RF signals over a range of IF frequencies. A 15 dB improvement is achieved for a 9 GHz input and 30 dB improvement for an 18 GHz input for 1.6 - 2.3 GHz IF frequencies.

A resistive coupler was added between the signal source and mixer to reduce the test signal power level from -16 dBm to -26 dBm at the input of the mixer. The coupling factor was determined by system requirements of the desired maximum mixer input levels.

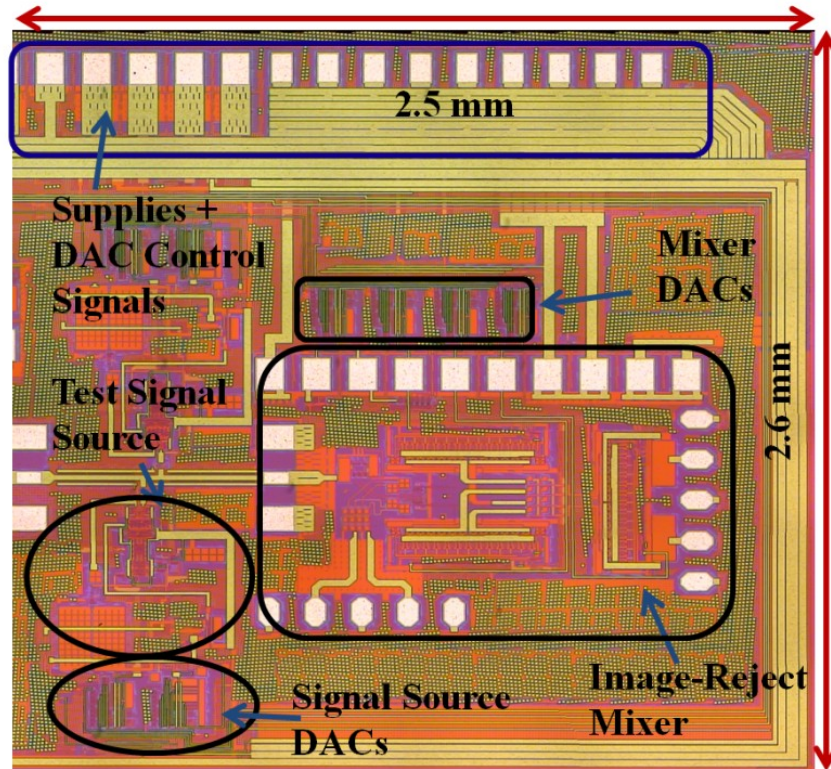


Figure 28. Die photo of integrated test signal source and image-reject mixer with supporting DACs and digital routing. Total area occupied is $2.5 \times 2.6 \text{ mm}^2$ including the pad frame.

To summarize, an integrated multiband test signal source and image-reject mixer spanning 8 - 18 GHz are implemented in a 180 nm SiGe BiCMOS process with 150 GHz f_T/f_{max} . The test signal is used for demonstration of automated self-healing of the IRR of the mixer as a first step towards local mixer healing, and ultimately global receiver chain healing. The signal source is able to reliably generate test signals in X- and Ku-bands over process and temperature corners. A 15 dB improvement in IRR is obtained for a 9 GHz test signal while a 30 dB improvement is obtained for an 18 GHz test signal at an intermediate frequency (IF) of 1.92 GHz. The motivation for this healing arises from

RF performance deviation in the receiver chain due to process variations, environmental effects, and circuit aging.

III W-BAND PHASED ARRAY RADARS

3.1 Introduction

Technology scaling is the process through which the minimum size geometry of transistors is continually reduced. This scaling requires constant development of new lithographic techniques to manufacture billions of these transistors in close proximity. The immediate benefit of this scaling is improved f_T and f_{max} frequencies, which eventually limit the maximum frequency of operation of circuits and systems. The f_{max} has a critical role to play in determining the maximum operating frequency of amplifiers and oscillators. A typical rule of thumb suggests that f_{max} should be 2-10 times the maximum frequency of circuit operation [73]. With cut-off frequencies above 300 GHz, state-of-the art silicon BiCMOS technologies enable novel applications in the mm-wave regime (30-300 GHz). These frequency regimes were historically dominated by III-V technologies, which suffered from lack of integration with existing silicon baseband systems. Now, with silicon based mm-wave frontends, the entire RF and baseband subsystems can be integrated on a single die for silicon area and cost savings.

In the mm-wave regime, some frequency bands are more conducive to communication than others as seen in Figure 29 [74]. This favorable operation depends on several factors including frequency dependent atmospheric attenuation, dust, fog, rain, and other weather conditions. The 75-110 GHz band, also known as the W band, offers natural benefits of reduced attenuation and is chosen for several applications such as gigabit wireless, security scanners, and radars for collision detection. One such application is the development of mm-wave imaging systems using radar technology.

Such systems typically use pulsed, chirped, or stepped-frequency topologies to achieve the imaging function [75]-[76].

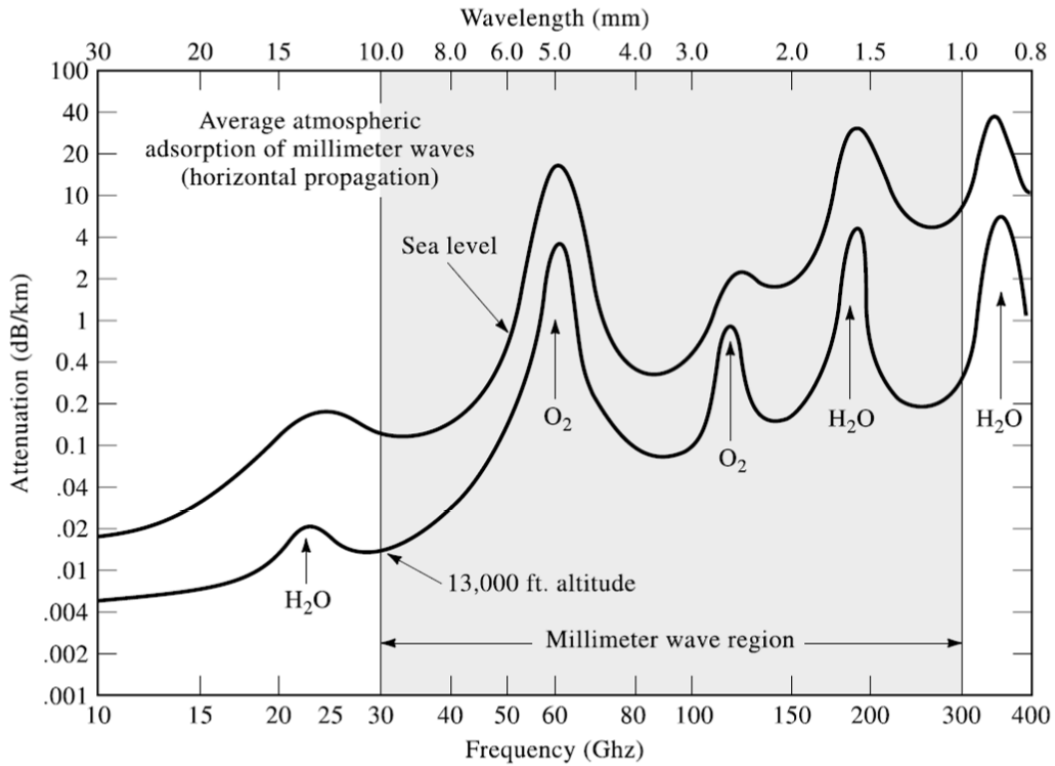


Figure 29. Atmospheric attenuation in dry air for mm-wave frequencies [74].

Recent works in the literature have demonstrated mm-wave phased-array solutions in the V and W bands. As an example, the work in [77] is a four channel SiGe based beam-forming radar operating around 91-97 GHz as seen in Figure 30. [78] has demonstrated a complex 736 x 736 Tx/Rx array operating around 72-80 GHz and is capable of detecting concealed objects as shown in Figure 31.

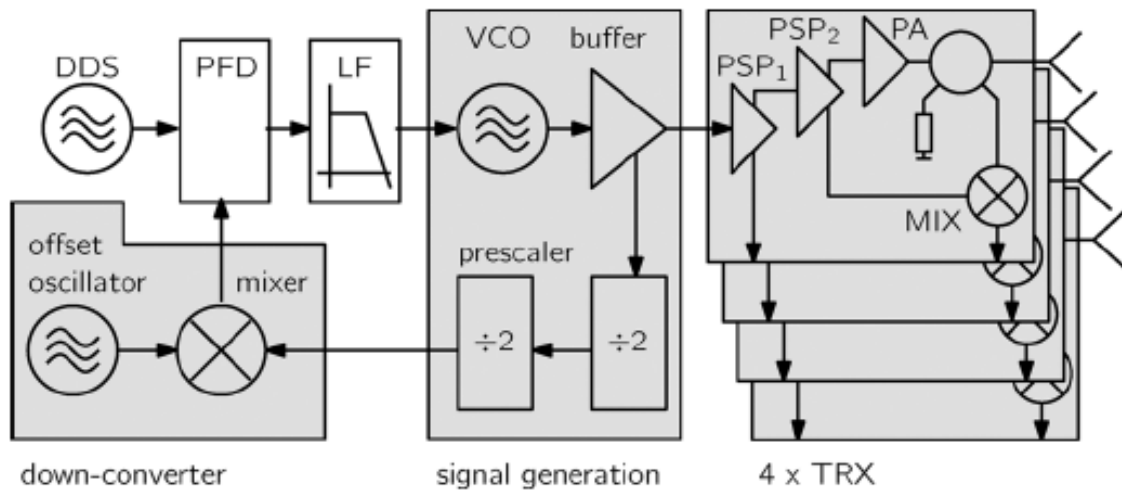


Figure 30. Four channel 91-97 GHz SiGe based beam-forming radar [77].

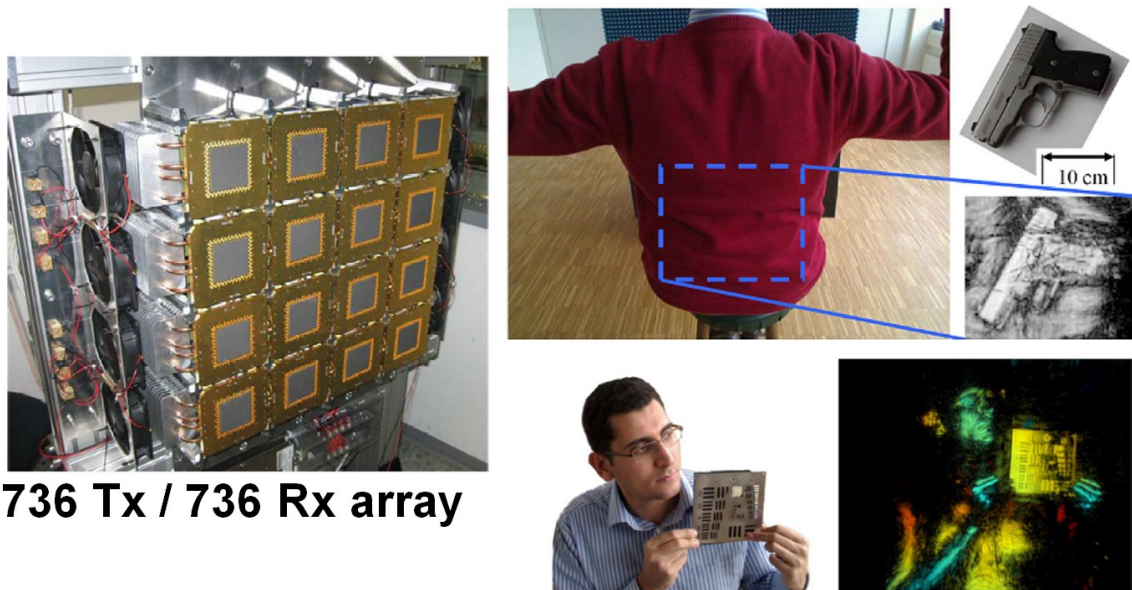


Figure 31. 736 x 736 Tx/Rx array for mm-wave imaging applications [78].

3.2 Radar Topology

While a pulsed radar suffers from low-energy signals compared with a frequency-modulated continuous-wave (FMCW) radar, the pulsed-radar topology simplifies the back-end signal processing required to extract range information. In addition, a pulsed-based system also consumes lower DC power than a comparable FMCW system. In this work a pulse based radar system is proposed. A conceptual system diagram of a pulsed-based imaging system is shown in Figure 32. The transmit side chain consists of a pulse generator, Gaussian pulse shaper, frequency synthesizer, buffers, phase shifters, power amplifier (PA), balun, and antenna. On the receive side, the signal is captured by a second antenna and passed forward to a balun, LNA, phase shifter, power divider, quadrature down-conversion mixer, and intermediate-frequency (IF) amplifiers. On the transmit side, the pulse generator produces short pulses on the order of 20-40 picoseconds (ps) that are fed into a Gaussian pulse shaper. This Gaussian pulse at baseband is then up converted to 94 GHz by multiplication with a carrier signal generated by the frequency synthesizer block. The pulses at 94 GHz are then appropriately phase shifted and amplified by the differential PA before being transmitted by the antenna. After being reflected by the target, the pulses are coupled into the receiving antenna and amplified by the LNA. The amplified pulses are then divided into in-phase (I) and quadrature (Q) paths for downconversion to 5 GHz IF. This downconversion is achieved by correlating the incoming pulses with delayed pulses generated by the pulse shaper at the mixer inputs. The degree of correlation between the pulses will determine the characteristics of the target being imaged. The differences in phase and amplitude of the received signals will ultimately help to distinguish between the target object and background noise.

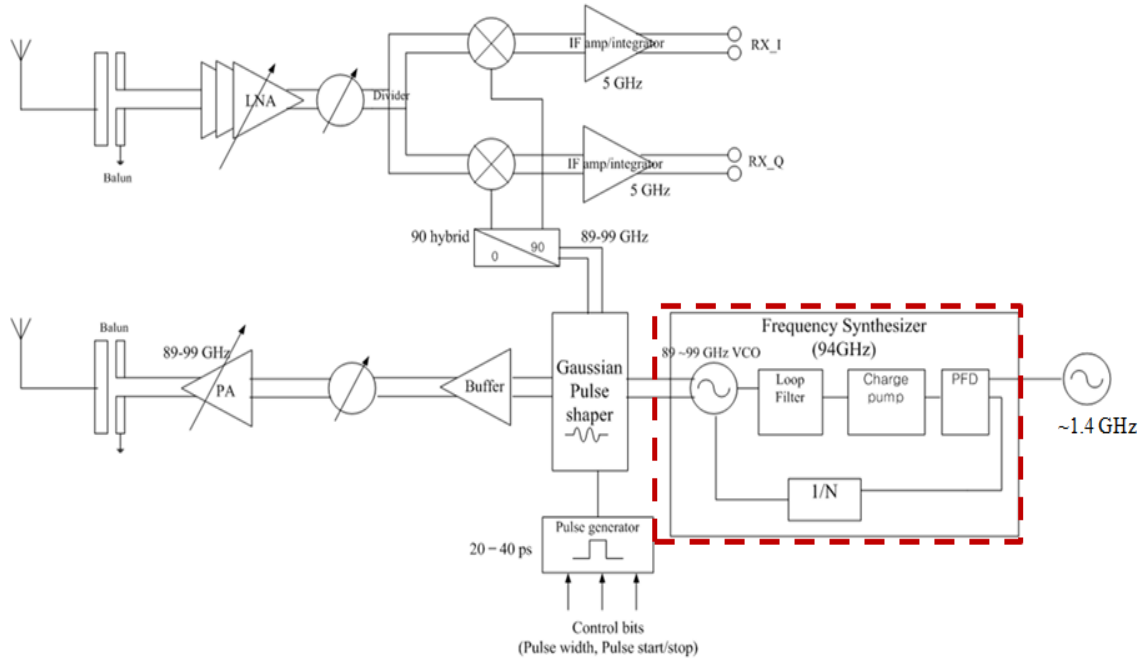


Figure 32. Proposed system diagram of a 94 GHz pulsed-radar imaging system.

This work is focused on signal generation aspects for the radar system. Further details of the 94 GHz PLL and the design challenges associated will be addressed.

3.3 Phase-Locked Loop Requirements for 94 GHz Systems

The upconversion of the Gaussian pulse requires an LO signal at 94 GHz with some tuning range around the center frequency. In addition, the LO must meet some output power and phase-noise specifications. In order to achieve close-in phase-noise requirements of the system, a PLL wrapped around the VCO is desirable. The block diagram of the PLL is seen in Figure 33. The 94 GHz oscillator is divided down using a chain of dividers to 1.4 GHz for comparison with a reference clock, f_{ref} , using a phase-frequency detector (PFD). The phase error is processed by a charge pump and loop filter to generate the appropriate control voltage for the VCO. Each of the circuit blocks have their own design challenges and require careful analysis of tradeoffs involved. For

instance, the divide ratio directly contributes to the phase noise inside of the loop bandwidth and is given by $20 \cdot \log N$, N being the divide ratio.

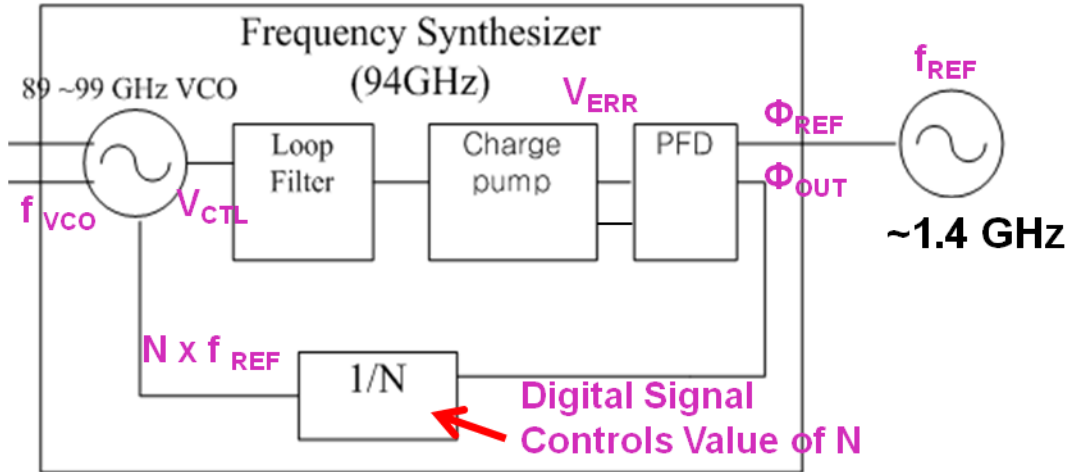


Figure 33. Proposed block diagram of 94 GHz PLL.

Thus there is an upper limit on the choice of N . On the other hand, if one chooses too small a divide ratio, then one needs to somehow generate a very high, yet pristine reference frequency which is extremely challenging for a fully integrated solution. In addition, if using a PFD / charge pump topology, the charge pump would need to switch at this high frequency which again can be a demanding design.

The dividers and VCO in particular require special attention as these blocks operate at the mm-wave frequencies. It is recommended to use different divider topologies over different frequency ranges in order to comply with power consumption requirements [79]. Typical divider topologies that can be used in a 94-GHz PLL are shown in Figure 34. Towards the upper end, injection-locked dividers are conducive as they can operate at very high frequencies with very low power dissipation. The main drawback with the topology is the narrow bandwidth. In the mid range, Miller regenerative dividers are preferred as they have a fairly wide tuning range and moderate

power dissipation. At the low end, static dividers can be used that have the widest tuning range at the cost of high power dissipation.

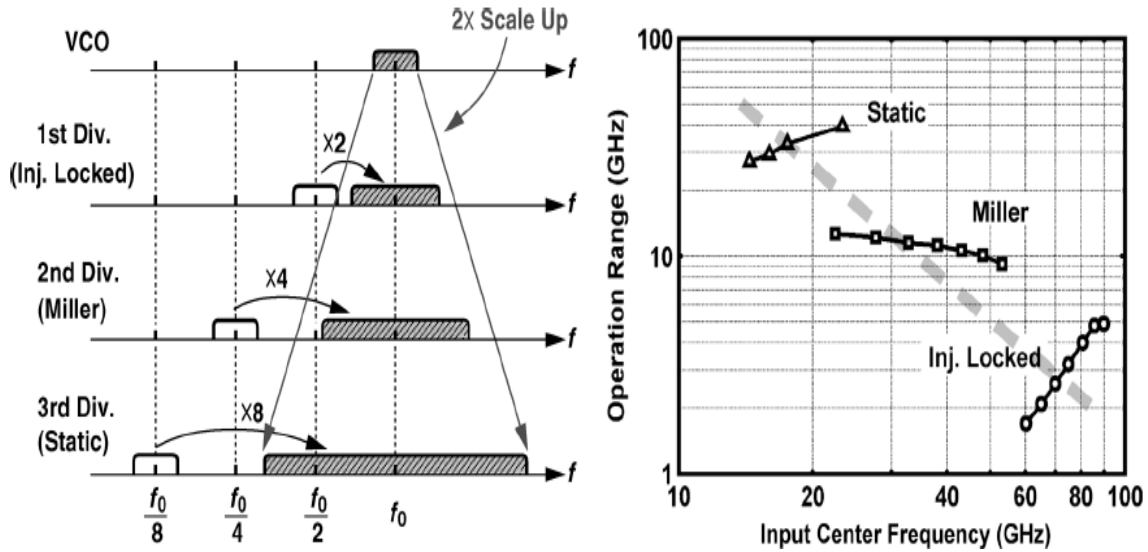


Figure 34. Recommended divider chain for mm-wave PLLs [79].

While designing these dividers, the tuning ranges of the dividers must have sufficient overlap to be able to operate successfully over process and temperature corners. Thus, each divider must be designed with at least a 2x margin to account for any of the variations.

3.4 A 94-GHz Differential Colpitts Voltage-Controlled Oscillator

3.4.1 Differential Colpitts Topology Considerations at 94 GHz

The two main oscillator topologies that can be considered for mm-wave operation include ring and inductor/capacitor (LC) based oscillators. While ring oscillators offer advantages of small form factor, wide tuning range, and inductor-less designs, they suffer from poor phase-noise performance. LC oscillators offer superior phase-noise performance at the cost of die area since inductors tend to occupy a large surface area. Thus, the choice of

topology is based on application driven requirements. For the present system, an LC based differential Colpitts topology is chosen as shown in Figure 35.

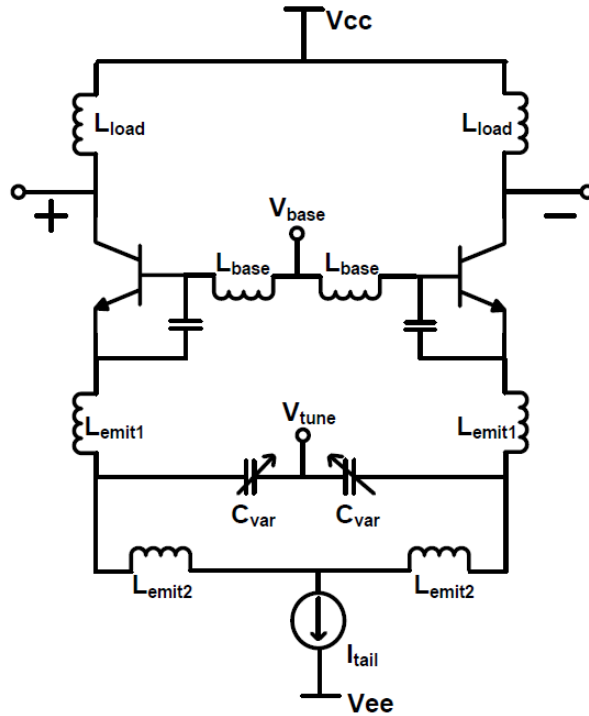


Figure 35. Schematic of the differential Colpitts VCO.

The classic single-ended Colpitts oscillator consists of a resonator LC tank with feedback to overcome parasitic tank-resistance losses, and to sustain oscillations. A typical common-collector configuration is depicted in Figure 36 to understand the operation of the circuit.

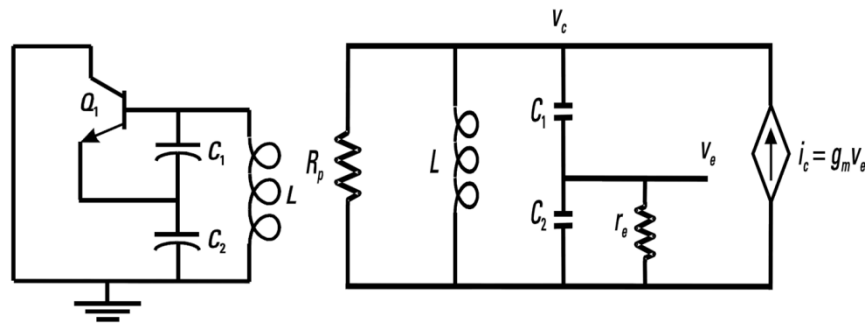


Figure 36. Schematic of a generic common-collector Colpitts VCO [80].

The tank consists of C_1 , C_2 , and L that resonate at

$$\omega = \sqrt{\frac{C_1 + C_2}{C_1 C_2} \frac{1}{L} + \frac{1}{r_e R_p C_1 C_2}}, \quad (3.1)$$

where ω is the resonance frequency of the tank, R_p is the parallel tank resistance, and r_e is the base-emitter resistance of the transistor. To sustain oscillations, the required transconductance (g_m) of the transistor is given by

$$g_m = \frac{1}{R_p} + \frac{1}{r_{e,tank}} \times \frac{C_1 + C_2}{C_1} = \frac{\omega(C_1 + C_2)}{Q_L}, \quad (3.2)$$

where Q_L is the quality factor of the inductor. The above two equations provide intuition for the various design variables and tradeoffs to achieve a certain oscillation frequency and output power. At mm-wave frequencies, there are additional concerns with performance that require modifications to the classic Colpitts topology. A few supplementary inductors are added at the collector and emitter terminals. With the presence of L_{emit2} , the DC current of the transistor is shunted to a virtual ground node. As a result, the parasitic capacitance of the tail transistor is not in shunt with the varactor anymore. This leads to improved tuning range and reduced phase noise performance. L_{emit1} improves the loaded quality factor of the tank contributing to reduced phase noise. A further requirement is to ensure that the resonance frequency of L_{emit1} - C_{var} is above the desired oscillation frequency, while that of L_{emit2} - C_{var} is below the oscillation frequency. In addition, the total admittance of L_{emit1} , L_{emit2} , and C_{var} should be purely capacitive over the desired range of oscillation [81].

3.4.2 Microstrip Short-Stub Inductor Design

As a result of high oscillation frequencies, values of the inductors are extremely small and thus difficult to implement with lumped element models. The inductors are realized with short microstrip lines with signal on top metal and ground on bottom metal in a six metal layer technology. The design iteration starts with ideal inductor values to obtain the desired oscillation frequency (f_{osc}). Next, the appropriate line width for 50 ohm matching is attained using Agilent's LineCalc tool. This is followed by electromagnetic (EM) simulations on the line with a line length guesstimate to extract inductance. The scattering (S) parameters from EM simulations are then plugged into the Cadence simulator to obtain a realistic estimation of f_{osc} . If the oscillation frequency is incorrect, the EM and Cadence simulations are repeated with a different line length until f_{osc} is achieved. The EM simulated values of inductance for L_{base} , L_{emit1} , and L_{emit2} are shown in Figure 37.

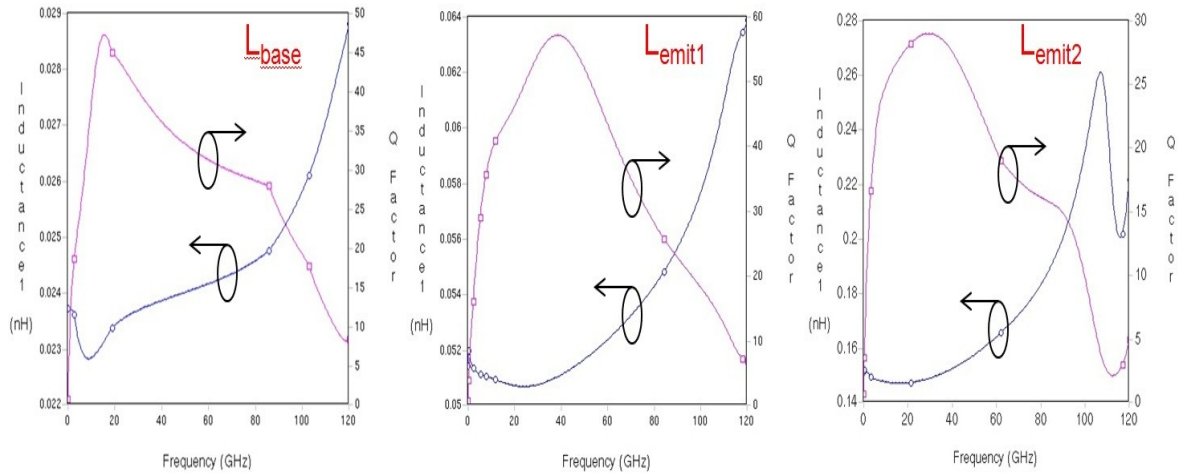


Figure 37. Inductance and Q factor for L_{base} , L_{emit1} , and L_{emit2} over frequency.

At the desired 94 GHz frequency, L_{base} is 26 pH, while L_{emit1} and L_{emit2} are 57 pH and 243 pH respectively.

3.4.3 Inversion-Mode MOS Varactor for Tuning

The varactor is the primary method to tune frequency, although changing core VCO tail current can also impact frequency. Several flavors of varactor technology exist ranging from simple diodes, accumulation-mode MOS (AMOS), inversion-mode MOS (IMOS), and hyper-abrupt junction varactors (which sport the widest tuning range). This work uses the steep tuning range offered by I-MOS varactors whose bulk is tied to ground. The I-MOS varactor is implemented with 14 parallel fingers with $0.8\ \mu\text{m}$ length and $1\ \mu\text{m}$ width. The tuning characteristics of a MOS with its bulk connected to source and drain is compared with that of an I-MOS in Figure 38. One notices that the I-MOS varactor utilizes the sharp slope where the MOSFET is transitioning from weak inversion to strong inversion. And, the device never enters accumulation while its bulk is tied to ground. In contrast, with the bulk tied to source and drain, the MOSFET potentially transitions between accumulation to weak inversion and finally strong inversion while in circuit operation. This could have a negative impact on frequency stability.

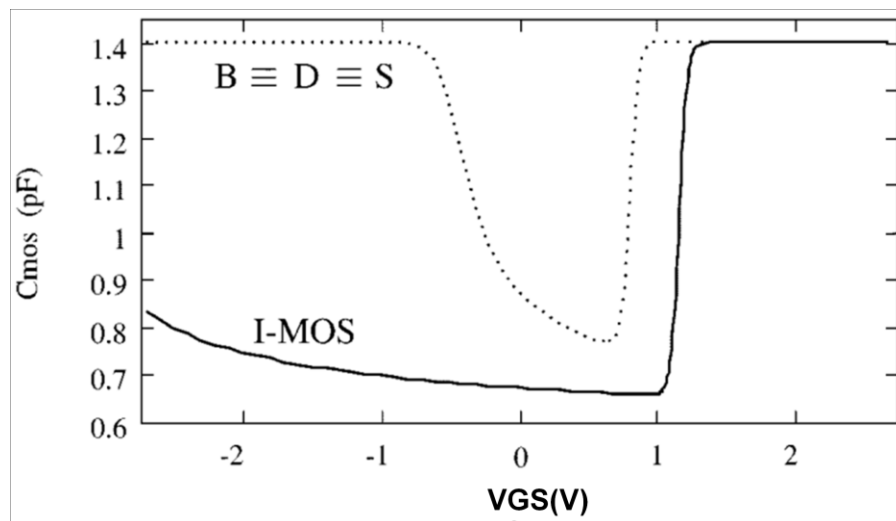


Figure 38. I-MOS varactor tuning characteristics compared with a MOSFET whose bulk is tied to source and drain [82].

The schematic and physical layout of the varactor is shown in Figure 39 with the gate terminal as the anode and source/drain terminals shorted together to form the cathode. Differential varactors are used to reduce upconversion of low frequency $1/f$ noise into the tank. The $1/f$ noise can be analyzed as a common-mode input since the tank inductor presents a low impedance at these frequencies. Thus the 'common-mode' noise produces equal and opposite changes in capacitance on the positive and negative legs, which cancel each other. Hence the capacitance is not modulated by the $1/f$ noise and hence the $1/f$ noise upconversion to phase noise does not take place. The degree of rejection depends on the symmetry and matching of the differential varactors.

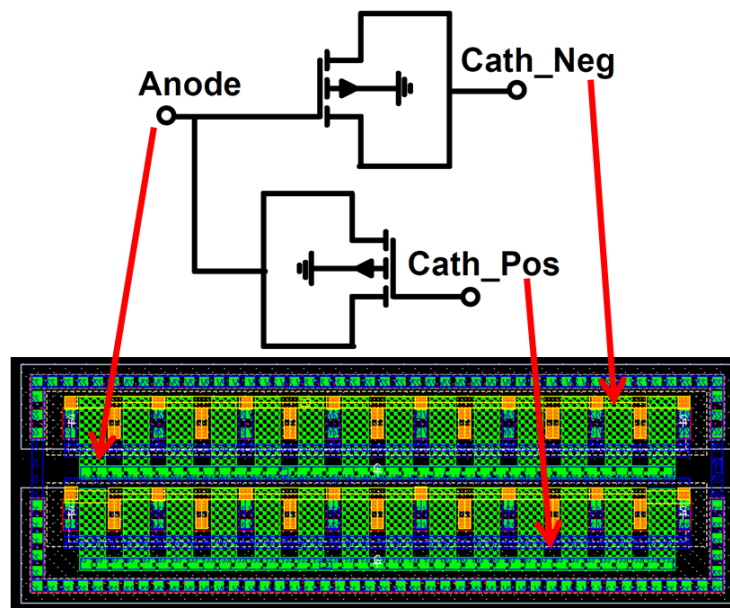


Figure 39. I-MOS Varactor schematic and layout.

3.4.4 Simulated and Measured Results

The tuning characteristics and output power of the VCO from simulations are shown in Figure 40. With the Cath_Pos node held at 1.5V, Cath_Neg is swept from 0.8V to 1.5V to achieve 16 GHz of tuning between 87-103 GHz. The output power over this range

drops by 1.4 dB from 5.4 dBm at 87 GHz to 4.2 dBm at 103 GHz. An emitter- follower output buffer is also placed between the VCO and the 50 ohm load to provide isolation and current drive.

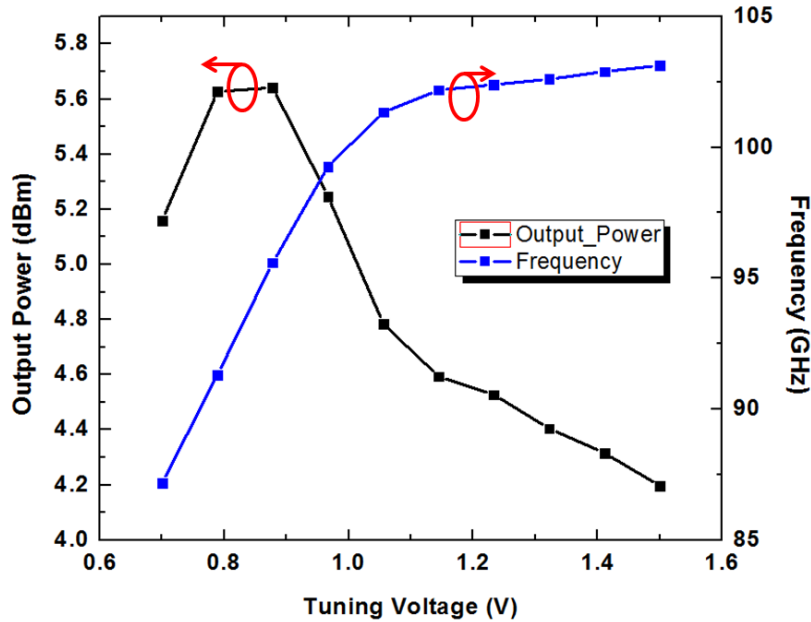


Figure 40. Frequency and output power simulations across tuning voltage of the VCO.

The range of frequencies is sufficient to provide flexibility in choosing the carrier signal frequency across process and temperature variations. The top-level layout of the VCO test structure is shown in Figure 41 with pads for DC inputs and RF differential outputs.

The oscillator is measured on die using 110 GHz 1 mm single-ended probes from GGB. In order to characterize frequency and output power, Agilent's 11970W waveguide harmonic mixer is utilized. The mixer is designed to interface with Agilent's E4446A spectrum analyzer. The LO signal for the mixer is provided by the analyzer while the RF input is connected to the GGB probes via a waveguide to 1 mm converter. The test setup is shown in Figure 42 while the mixer and its associated conversion losses are presented in Figure 43.

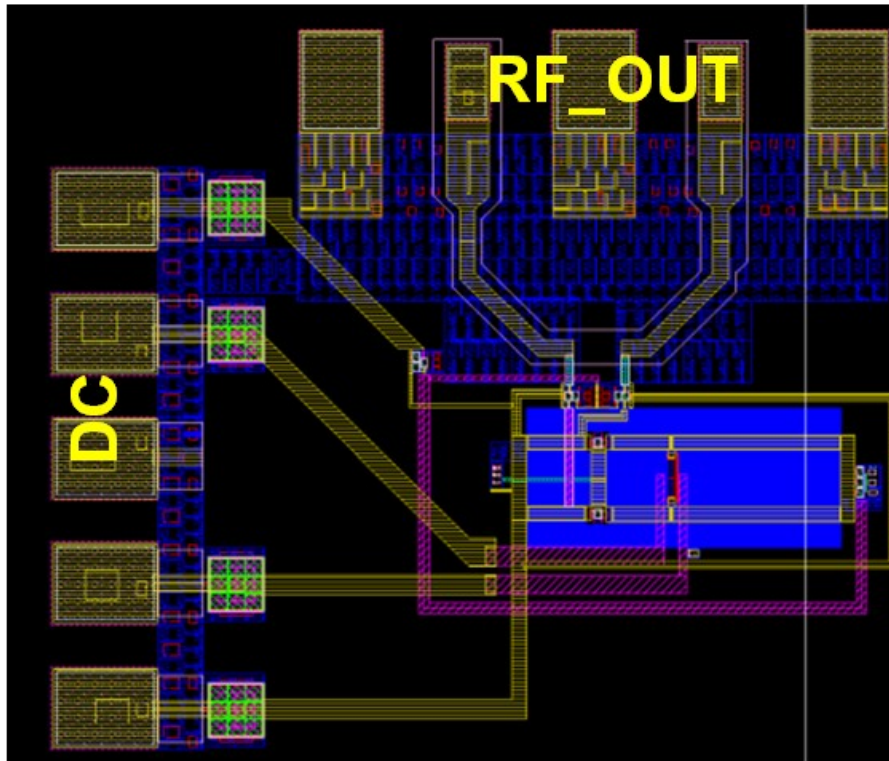


Figure 41. Layout of 94 GHz VCO test structure for standalone characterization.

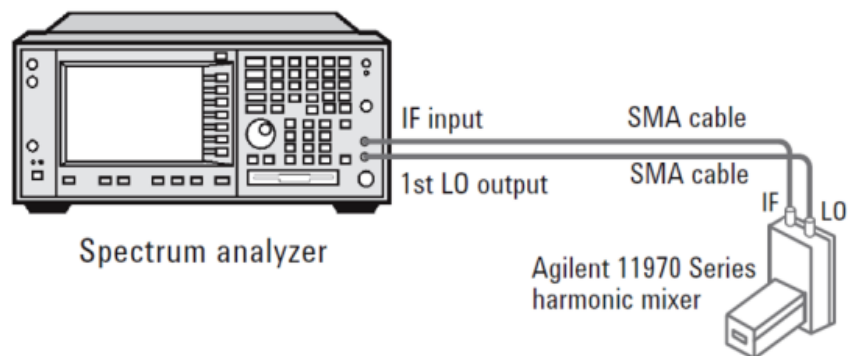


Figure 42. Test setup with Agilent's E4446A analyzer and the 11970W harmonic mixer.

The loss chart in Figure 43 suggests that the 11970W mixer has a conversion loss of about 40-45 dB in the W-band regime. These losses would need to be accounted for while calibrating the oscillator power that the analyzer displays.

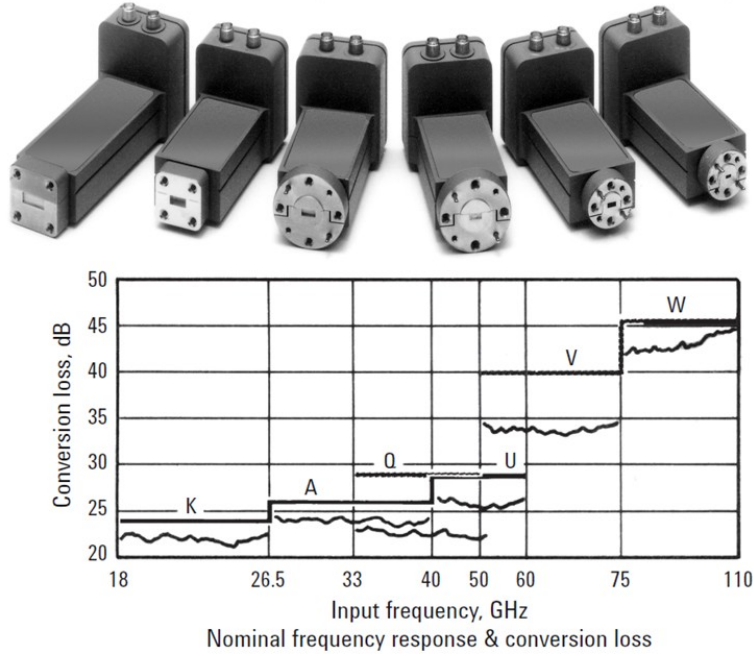


Figure 43. Conversion loss of the 11970W harmonic mixer.

Measured results of the single-ended output of the oscillator are captured in the following Figures 44-47.

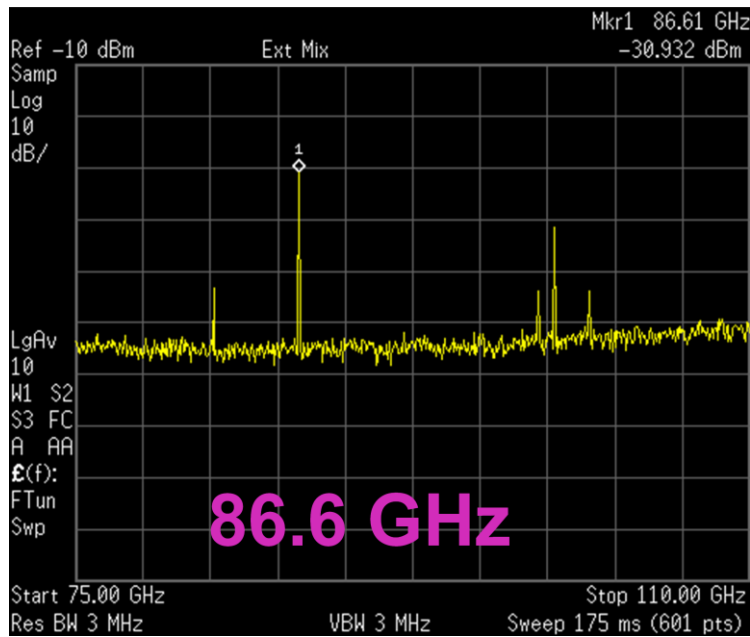


Figure 44. Measured performance of VCO at 86 GHz.

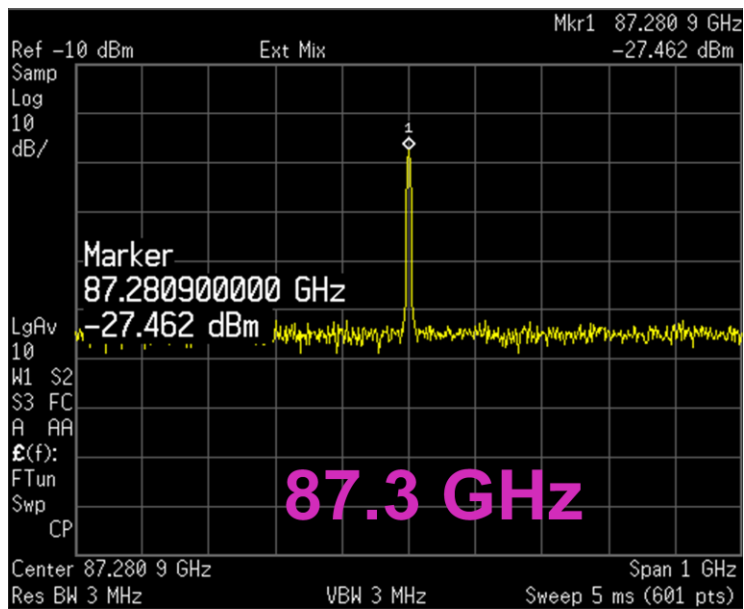


Figure 45. Measured performance of VCO at 87 GHz.

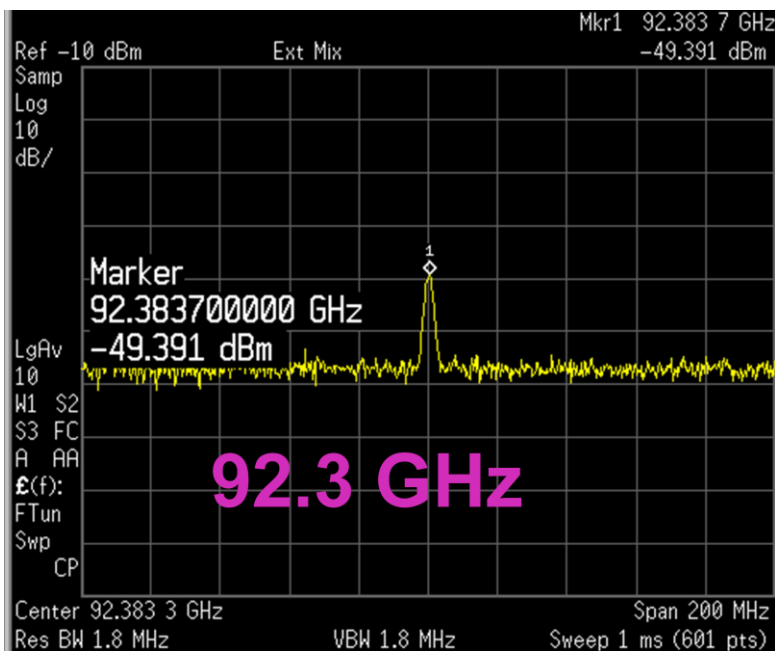


Figure 46. Measured performance of VCO at 92 GHz.

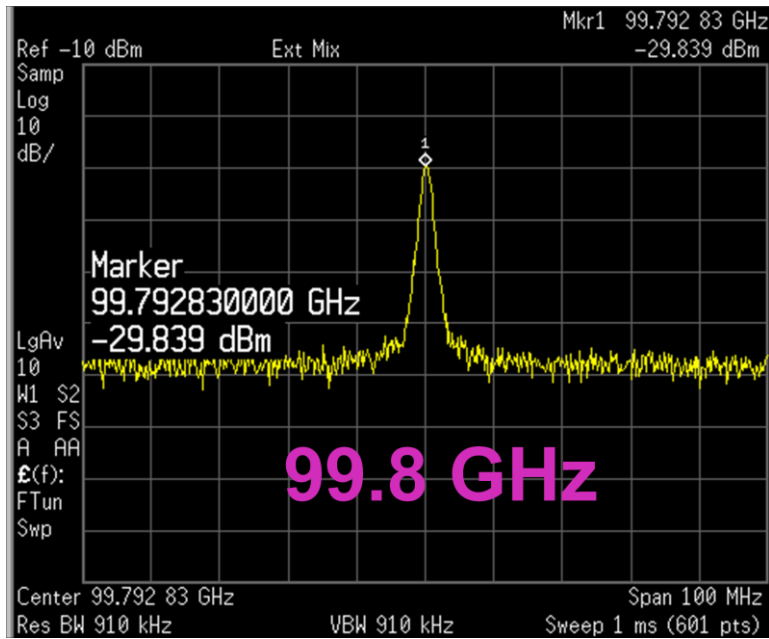


Figure 47. Measured performance of VCO at 99 GHz

The measured oscillator frequency range is within the desired band of interest and achieves a 14% tuning range in measurement between 86 - 99 GHz. It is worth mentioning that a combination of core bias tweaking and varactor tuning was required to achieve this wide span. The power levels are uncalibrated and need to be adjusted using the mixer conversion loss chart from Figure 43. The calibrated power levels are in the range of 5 - 10 dBm for most frequencies. Around 92 GHz, additional losses are experienced leading to a calibrated output power of -9 dBm. The main bottleneck at these frequencies is the varactor quality factor, and that could be a potential reason for the dip.

3.4.5 Comparison to State-of-the Art

This work is compared to state-of-the art in terms of tuning range in Table 4.

Table 4 : 94 GHz VCO Comparison to State-of-the Art

Reference	<i>Center Frequency</i> [GHz]	<i>BW</i> [GHz]	<i>% Tuning Range</i>	<i>Varactor Type</i>	<i>Process</i>
[83]	89	6	6.7	AMOS	SiGe
[77]	96	12	12.5	Diode	SiGe
[84]	96	10	10.6	Diode	SiGe
[85]	81	24.5	30	Hyperabrupt Junction	SiGe
[86]	90.5	11	12.1	-	SiGe
This work	92.5	13	14.5	IMOS	SiGe

While [85] offers the widest % tuning range, they achieve this with the use of special hyperabrupt junction varactors which require a tuning voltage range of -7 to 0 V. Generating these large voltages can be an issue particularly when trying to create fully integrated system-on-a chip solutions. In addition, most technology platforms do not offer this special varactor, and hence there are potential issues with commercializing products that use this type of varactor. The present work uses commonly available IMOS varactors and is still able to achieve an excellent 14 % tuning range, which is best in class.

IV MULTI-GIGABIT WIRELINE SYSTEMS

4.1 Challenges in High Data Rate Wireline Systems

Reliable 10 Gbps wireline systems are routinely being manufactured today by industry for various standards such as CEI/OIF (11.1 G) (chip-to-chip), XLAUI/CAUI (10.3125 G) (chip-to-chip and chip-to-module (optical)), and XFI (11G) and SFP+ (to 11G) (chip-to-module interfaces). The trend towards higher speeds is depicted in Figure 48 as a projection by the International Technology Roadmap for Semiconductors (ITRS) in 2007 [87]. Several bottlenecks to maintain the projected trend exist, including process technology limits, packaging limits, and high-speed testing limits. In this work, the focus will be on identifying the process technology limits to achieve higher signaling speeds.

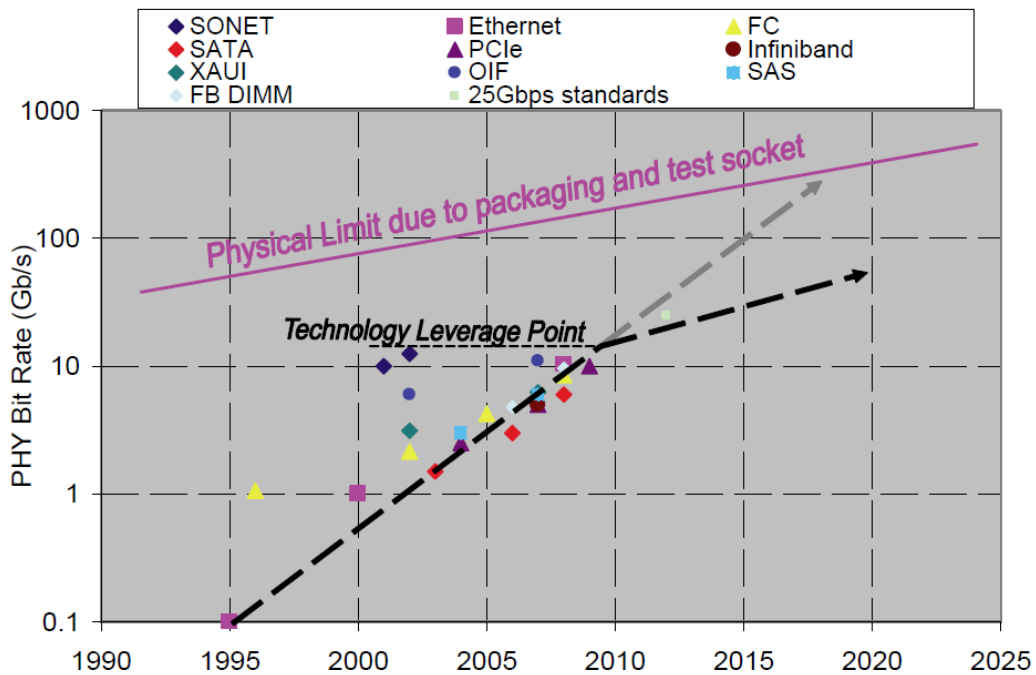


Figure 48. High-speed interface trend [87].

Moving towards robust 40/100 Gbps systems requires advancements at various levels including, circuit-level optimizations, device-level scaling, and process-level enhancements. The f_T of the HBTs used in the circuits is a critical performance metric that restricts the upper limit on transistor switching speed. A second performance metric is τ_{delay} , which quantifies the time delay of a single current-mode logic (CML) inverter stage that limits the speed of the entire system. Accurate characterization of f_T/f_{max} and τ_{delay} is an important step towards overcoming process technology bottlenecks. Knowledge of these metrics can be used to make process technology tweaks that enhance f_T/f_{max} and minimize τ_{delay} . Developing new figures-of-merit that relate circuit performance to device level parameters are also extremely useful to predict how a certain process tweak will ultimately affect circuit and system performance. An example of such a FoM is one that relates ring oscillator frequency to number of stages and stage delay as was given by equation (2.6). The ring oscillator is routinely used as a benchmarking tool to characterize a particular technology as the benchmark captures useful information beyond f_T and f_{max} of a single transistor. The ring is also used in CDR circuits that form the core building blocks of any modern wireline transceiver.

Linearity and noise figure of single devices are well understood phenomenon that also serve as performance metrics for a technology. From a wireline system standpoint, the impact of linearity and noise of single devices on critical circuit blocks is not well understood. Nonlinearities of a device can translate to time domain distortion in the form of jitter, and frequency domain distortion in the form of phase noise. Both jitter and phase noise are critical system level parameters that limit signaling speeds. Thus, comparison of

linearity of single devices with that of CML blocks is a first step towards quantifying the impact.

4.2 Technology Benchmarking

4.2.1 Robust f_T/f_{max} Extraction for Minimum Size Devices

Development of robust test structures to characterize f_T/f_{max} becomes critical with technology scaling as parasitics of test structures start to corrupt the measurement and extraction process. Accurate de-embedding of pad and feed line parasitics right up to the device metal contacts is required to extract the correct f_T and f_{max} of the single device. Open-Short de-embedding is a commonly used technique that assumes lumped element models for parasitic elements and is typically accurate up to 75 GHz. A typical coplanar waveguide (CPW) test structure is shown in Figure 49. The capacitance of signal pads is minimized by maintaining minimum size pads that can be probed ($50\mu\text{m} \times 50\mu\text{m}$). The distance between signal and ground pads is set appropriately to maintain a 50 ohm impedance match at the input and output ports. The transmission line from the pads to the device under test (DUT) is at the highest metal layer right up to the device contact to minimize the line capacitances. The DUT is a minimum size transistor in the given technology platform. The extracted f_T and f_{max} of the same device from the above test structure are compared with that of a poorly designed test structure in Figure 50. The contrast is clearly visible pointing to the importance of well designed test structures.

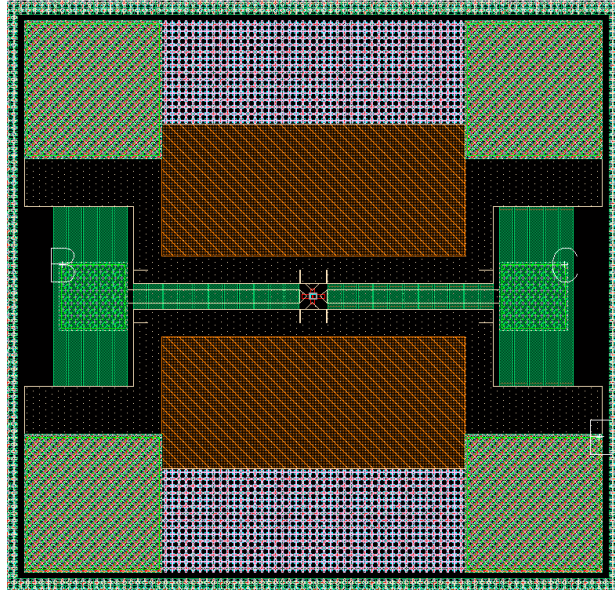


Figure 49. A CPW test structure for a single device.

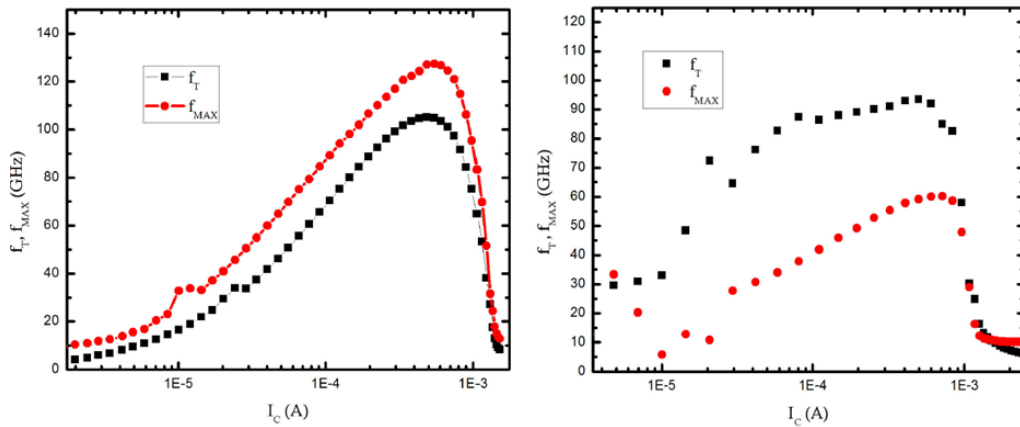


Figure 50. f_T/f_{max} comparison between well-designed and poorly-designed structures.

4.2.2 Gate Delay Characterization

To benchmark the speed of the technology, ring oscillator structures are constructed based on values determined from simulations. The oscillators can have either CML or ECL type gates and are connected in a ring formation as seen in Figure 51.

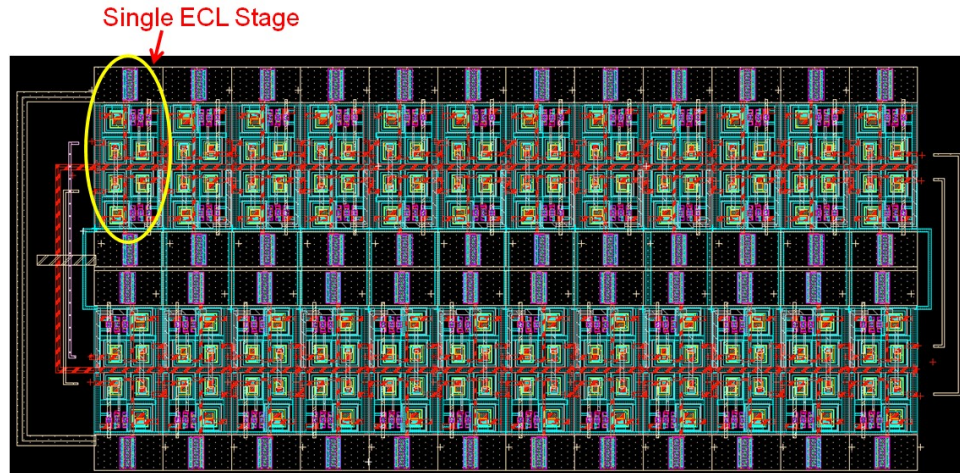


Figure 51. 24-stage ECL ring oscillator to characterize minimum gate delay.

The layout is made as compact as possible to reduce length of routing lines and the associated routing parasitics. The reason for choosing a large number of stages is to average out any variations in gate transition times to get a truly representative gate delay, repeatable to the nearest tenth of a picosecond. A large number of stages also make it easier to measure the oscillator since a larger number corresponds to a lower oscillation frequency.

The design methodology of a ring oscillator begins by fixing the desired voltage swing at the output. The swing is typically determined by system level considerations and varies for different applications. Once the swing is set, the tail current of the switching core transistors is set to the value that corresponds to peak f_T of the differential pair devices. Next, the value of the load resistor is deduced from simple equations relating voltage swing and tail current. For an ECL ring, the emitter-follower (EF) devices are sized according to the fan-out. In this case since the fan-out is one, the EF devices are similar in size to the switching devices and also carry the same current. Measured oscillation frequency and gate delay of the ECL ring are shown in Figure 52.

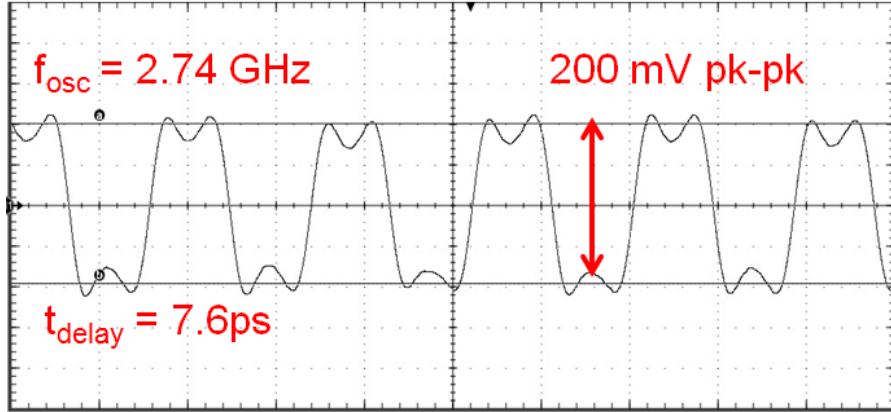


Figure 52. Measured oscillation frequency and gate delay for 200 mV swing.

The 7.6 ps delay corresponds to the minimum gate delay that the technology can support and is confirmed in extracted simulations.

4.2.3 Charting the Power-Delay Curve

Minimum delay is not necessarily the only design constraint. Power consumption also plays a critical role in making system design choices, and hence, the power-delay tradeoff characterization is also an important piece of the technology benchmarking process. To acquire the power-delay curve, an array of ring oscillators with varying load resistances are required to be fabricated. Next, the delay of each of the oscillators is measured with different tail currents while maintaining the fixed voltage swing at the output. To get an accurate power-delay curve, a large number of such ring oscillators would need to be fabricated, which takes up a lot of die area. An alternative would be to use a variable load resistor that can be tuned to a wide range of resistance values. This variable load can be realized through a PMOS device in place of the resistor with the ability to control the gate voltage. A schematic of such a modified CML gate is shown in Figure 53.

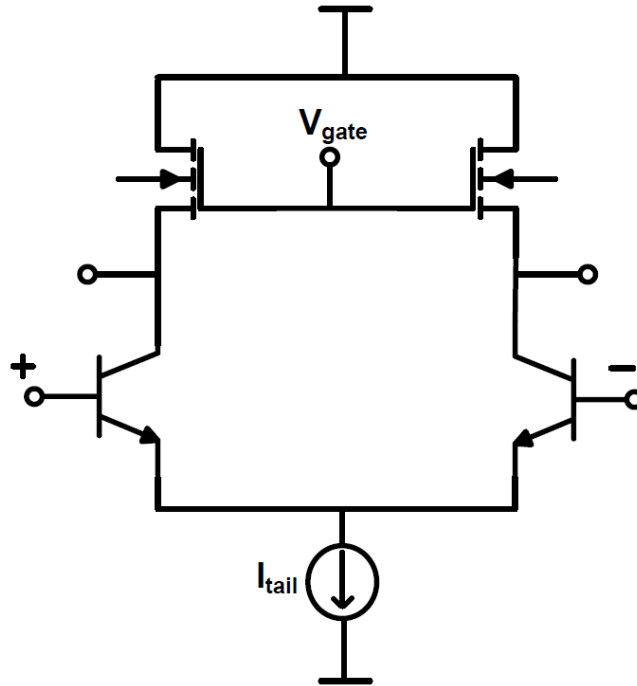


Figure 53. Modified CML gate with variable load PMOS resistor.

Thus, with a single test structure, one can obtain the entire power-delay curve that can be very advantageous from a die-area standpoint. The gate voltage for this structure is varied between 0.18-1.89 V with a 2.5 V supply. The tail current is adjusted as well for each gate voltage bias to maintain a 200 mV swing. An EF buffer is also present at the output of the ring to interface with a 50-ohm measurement environment. The power-delay curve generated using this test structure is shown in Figure 54 on a log-log scale. The y-axis represents τ_{delay} while the x-axis represents tail bias current. The curve with square symbols is the delay for various gate voltages over tail bias current. The curve however is the uncalibrated power-delay product since it includes additional parasitics of the PMOS transistor. With knowledge of minimum delay from the fixed load CML ring, it is possible to generate a calibrated curve. This calibrated curve now is a more accurate representation of power-delay tradeoffs of the technology. Depending on the type of

application, one can choose to sacrifice delay for power efficiency or choose speed at the cost of more DC power consumption.

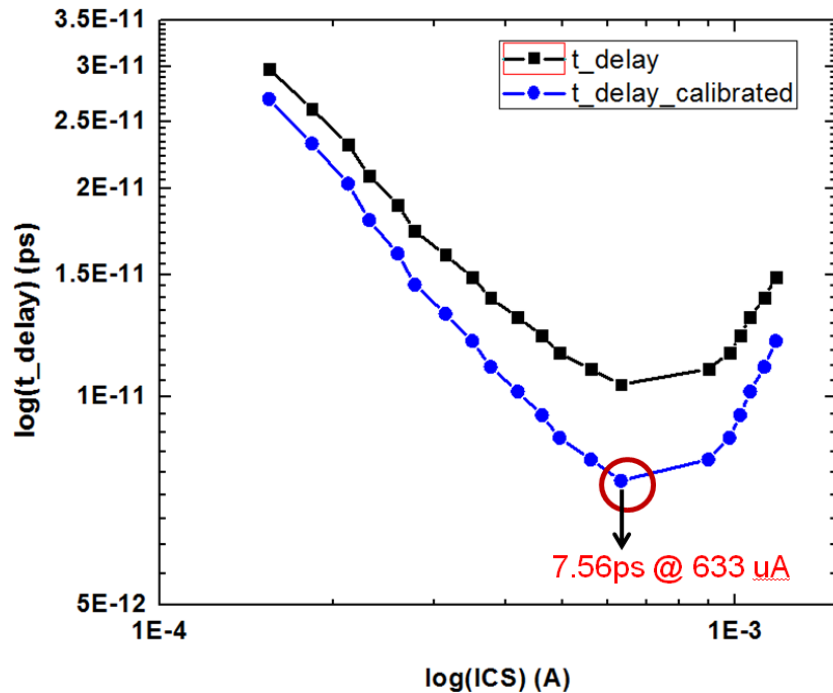


Figure 54. Calibrated and uncalibrated power-delay curves using a PMOS load.

4.3 Linearity Performance of Single Device and CML Gate

The linearity of a single transistor can be understood from either a large-signal or small-signal perspective. From a large-signal standpoint, linearity characterizes the ability of a device to accurately amplify input signals. The point where gain falls off by a dB is known as the one dB compression point or P1dB. A typical plot depicting measured gain and output power roll-off is shown in Figure 55. The P1dB point provides intuition into how large an input signal the device can handle before saturating or compressing. This information is useful when designing power amplifiers that typically handle large input signals. The small-signal linearity is different in the way it is characterized and usually involves presenting two closely spaced tones at the input of the device.

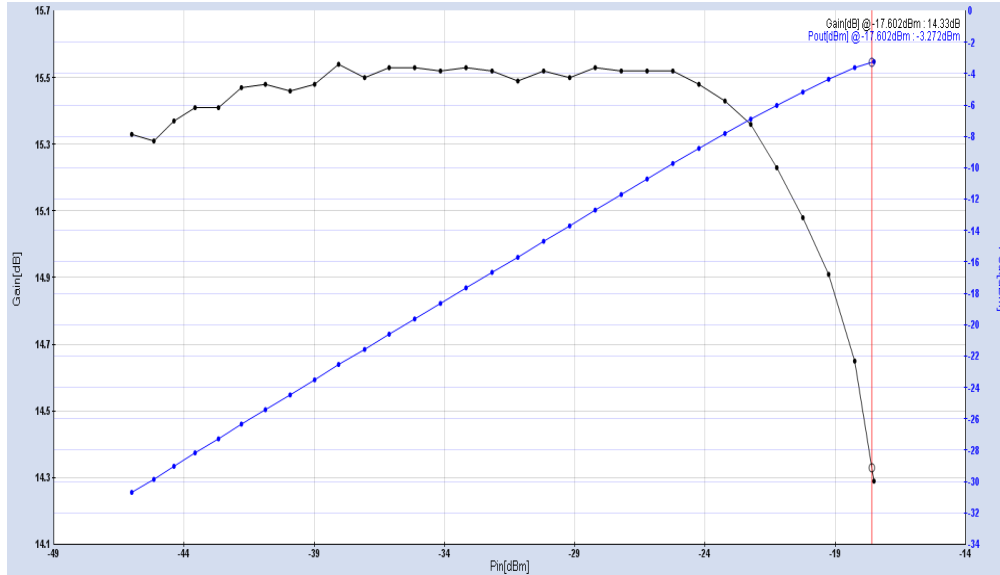


Figure 55. Measured P1dB point for a 0.15 x 2 μ m device.

The inherent I-V and C-V nonlinearities of the device act upon the two tones to produce intermodulation (IM) products given by

$$\begin{aligned}
 y(t) = & \left(k_1 A + \frac{3k_3 A^3}{4} + \frac{3k_3 A^3}{2} \right) \cos \omega_{1,2} t + \dots \\
 & + \frac{3k_3 A^3}{4} \cos(2\omega_{1,2} - \omega_{2,1}) t + \dots \\
 & + \dots
 \end{aligned} \tag{4.1}$$

where $\omega_{1,2}$ are the fundamental tones and $(2\omega_2 - \omega_1)$ and $(2\omega_1 - \omega_2)$ terms are the third-order IM tones. By inspection, one can see that while the fundamental tones grow at 1:1 ratio, the IM tones grow at a 3:1 ratio. A mathematical construct called the third-order intercept point (IP3) is defined as the point where the fundamental and IM tones intersect. A graphical representation of the phenomenon is shown in Figure 56 with an input IP3 (IIP3) of +10 dBm and an output IP3 (OIP3) of +20 dBm. In reality, one does not present such large input signals to the device. Instead, small signals (-30 to -20 dBm) that satisfy

the 1:3 ratio between fundamental and IM tone amplitudes are chosen for the characterization.

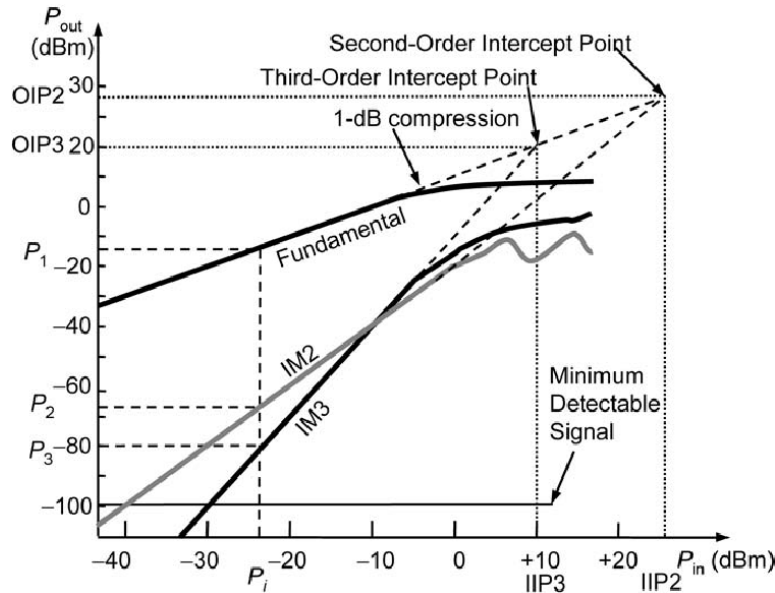


Figure 56. Conceptual plot of IIP2 and IIP3 using fundamental and IM tones.

In a CML/ECL ring oscillator, the switching core transistors experience a range of collector current (I_c) and collector-emitter voltage (V_{ce}) bias combinations. The IIP3 is fundamentally dependent on bias point and varies with changing bias conditions. Hence, characterizing the small-signal linearity of a switching transistor requires the extraction of IIP3 over a range of I_c - V_{ce} bias points. The bias transitions can be captured in a plot called the dynamic load line as shown in Figure 57. While I_c varies between 0-500 μ A, the V_{ce} varies between 980-720 mV. A subset of points is chosen to measure IIP3 of a single device and then compare that with the IIP3 of a device inside of the CML gate environment. The motivation for this comparison is that inside the CML gate, the switching device experiences a different impedance environment. The collector of the device connects to a resistor in parallel with the base of a transistor of the next stage,

while the emitter connects to the collector of the tail transistor. Hence, there is reason to believe that the IIP3 and thus linearity of a CML device may be different.

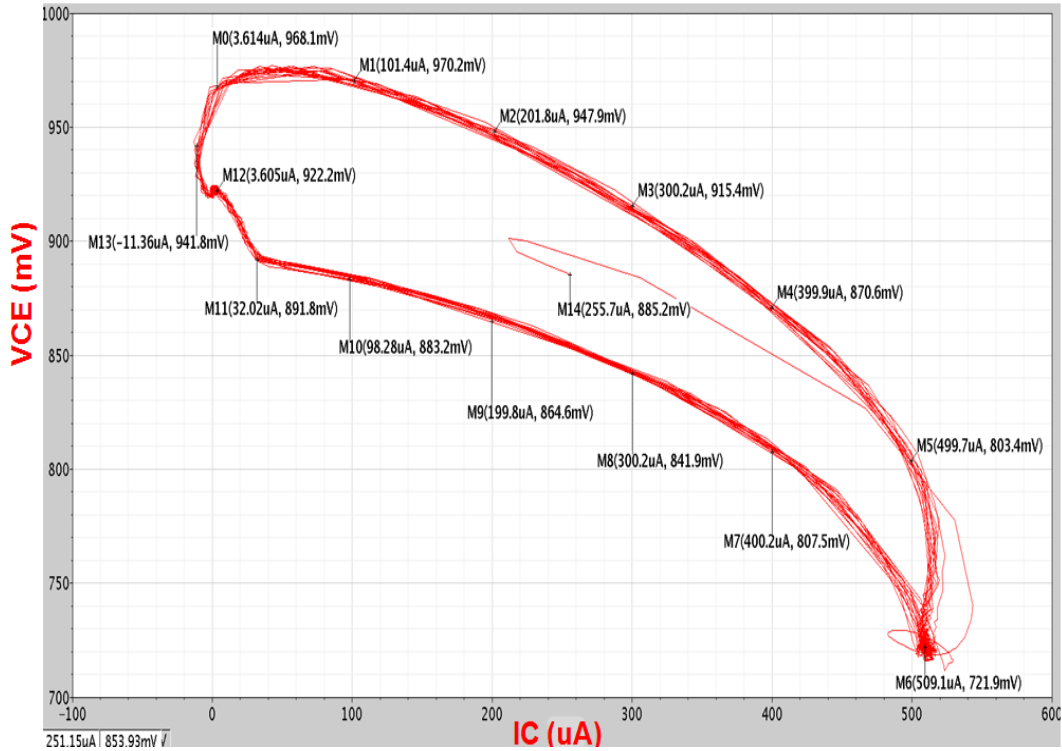


Figure 57. Dynamic load-line plot of CML gate switching transistor.

For an apples-to-apples comparison of linearity between a single device and a CML device, a custom test structure is fabricated that allows DC and RF probing of the switching device as shown in Figure 58. The structure consists of a single CML gate with the base and collector of the left-side switching transistor connected to RF IN and RF OUT respectively. The bases of both switching transistors are connected to VBASE with tail bias being mirrored by a 1:1 HBT mirror. The structure allows measurement of IIP3 of the switching device with the CML impedances. The measured and simulated linearity of a single $0.15 \times 0.41 \mu\text{m}$ device and that of a similar sized CML device are compared in

Figure 59. The bottom x-axis is the collector current while the top x-axis is the V_{ce} of the device.

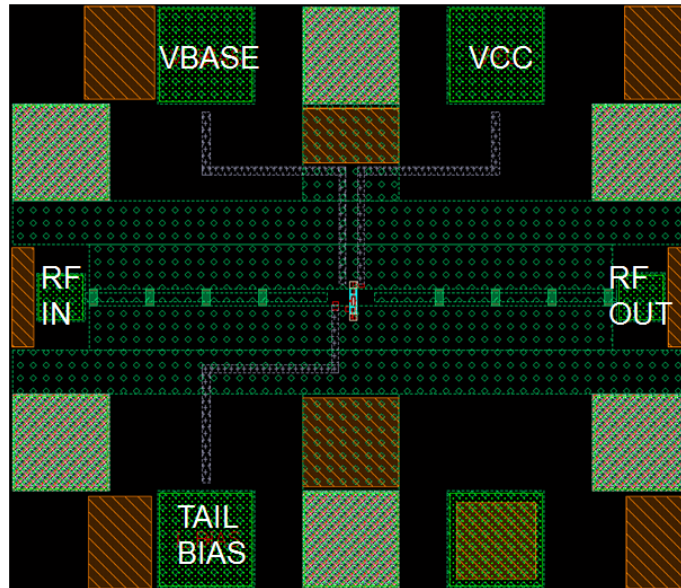


Figure 58. Custom test structure to probe CML switching device.

The shape of the IIP3 curves has a distinct resemblance to the big dipper. The curve begins on the left with zero I_c and maximum V_{ce} and starts moving clockwise until the curve reaches maximum I_c and minimum V_{ce} . Next the curve turns back continuing to move clockwise returning to zero I_c and maximum V_{ce} . The curves with square symbols are measured and simulated IIP3 over dynamic load-line bias points for a common-emitter standalone device. The peak IIP3 of -1 dBm occurs at an I_c of 300 μ A. The curves with star symbols are measured and simulated IIP3 of the CML device and are distinctly different in comparison with the standalone device. At 300 μ A I_c , the IIP3 of the CML device is degraded by almost nine dB to -10 dBm, and its peak occurs at 500 μ A. The slopes of the standalone device and CML device are also distinctly different. This comparison goes to show that the sources of nonlinearities are different between the two structures and that the dominant sources are also potentially different. Further

investigation into the individual nonlinearity contributors is required through a Volterra series analysis.

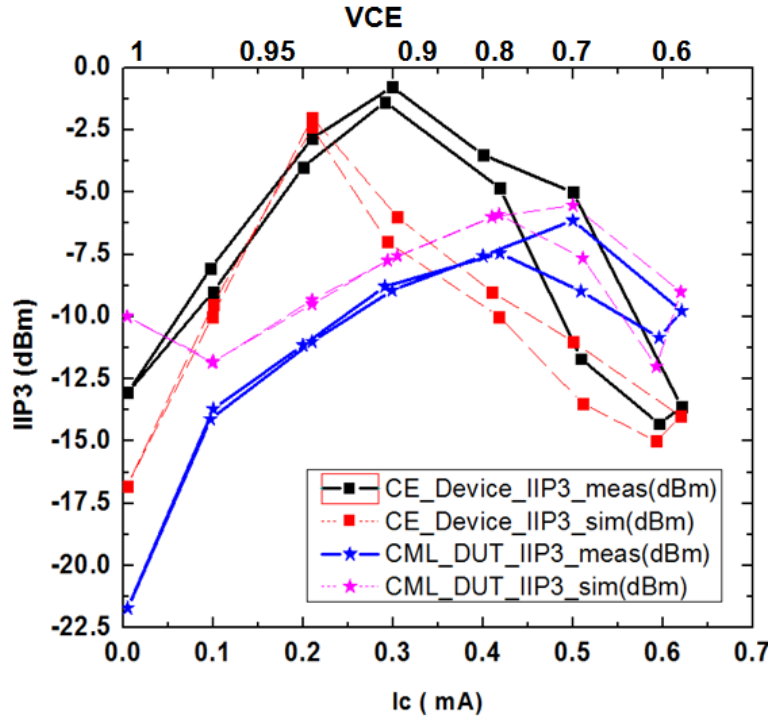


Figure 59. Comparison of IIP3 for a single device and a CML switching device.

4.4 Predicting Large-Signal Gate Delay Using Small-Signal Techniques

4.4.1 Motivation

Accurate prediction of large-signal CML or emitter-coupled logic (ECL) gate delay using small-signal techniques has been a subject of extensive study in the literature. The need for prediction arises from the fact that while f_T and f_{max} are useful benchmarking metrics, they fail to capture the impact of the technology limits on large-signal circuit performance. While f_T assumes the transistor output node is short-circuited, f_{max} assumes a conjugate match at the input and output of the transistor. In addition to being

small-signal extrapolations, the assumptions under which these metrics are extracted are also not realistic from a circuit standpoint.

The use of ring oscillators (ROs) to characterize gate delay is common practice, primarily to assess large-signal effects on gate delay that are not captured by f_T and f_{max} . Typically, several ROs are fabricated with varying load resistor and tail current combinations to trace out the power-delay curve. Although unavoidable, the down side to this approach is that it is extremely time consuming in the context of fast process optimization. As a result, the need to accurately predict gate delay in simulation has been recognized as extremely important for hastening the ramp up cycle of a new technology platform.

Various analytical techniques have been either derived using certain assumptions, or obtained using sensitivity analysis [88]-[93]. Several figures-of-merit (FoMs) have been proposed using these analytical techniques that express gate delay in terms of weighted RC time constants. There are several drawbacks of these existing FoMs. Some FoMs tend to be complex, with many terms, making it difficult to gain insight into the dependence of the gate delay on transistor parameters. Others have fairly large error percentages due to over simplification of the transistor model under various assumptions. Most importantly, these existing FoMs depend on compact model parameters that are themselves process dependent. Hence, the weighting constants need to be recalculated with each tweak made during the technology ramp up cycle in order to use the FoM. This facet can be debilitating since calculating the weighting coefficients requires significant simulation overhead.

A different approach also found in the literature is to use two-port, small-signal Y parameters to come up with useful FoMs that can predict large-signal circuit behavior [94]. The main attraction to using this approach is that the FoM can be directly extracted from Y-parameter measurements without the need for an equivalent compact model. This can tremendously speed up the process optimization cycle, since creating robust compact models can be very time consuming. In addition, the FoM obtained from this technique is more realistic, since it is not based on assumptions like the ones used for f_T and f_{max} . There are limitations to using the Y-parameter approach, however. First, if the two-port network is treated as a 'black box,' the FoM can suffer from lack of physical insight into the transistor components that contribute to delay. Second, expressions relating circuit performance to model parameters get cumbersome, with large numbers of circuit components inside the 'black box.' To overcome the first limitation, the FoM can be applied to a two-port simplified hybrid- π model to generate an expression for delay in terms of model parameters.

The present work seeks to improve upon the existing Y-parameter based FoM presented in [94] and compare the efficacy of the proposed small-signal delay FoM to large signal RO delay. There are many favorable implications of such a FoM. With simple Y-parameter simulations or measurements of a single transistor, one can potentially predict how complex circuits like ring oscillators, latches, and flip-flops will perform in a given technology platform, before those circuits are actually built. Section II will elaborate more on the limitations of existing Y-parameter based FoMs and presents our new FoM, along with an assessment of its validity. Section III will

supplement the new FoM with a corresponding model parameter based expression that provides added insight into the physical transistor components contributing to CML delay.

4.4.2 Y-Parameter Based Figure-of-Merit

A standard resistively loaded CML gate is shown in Figure 60, with load R_L and tail current I_{TAIL} . From a small-signal standpoint, this circuit can be analyzed either from a differential-mode or a common-mode perspective. For the purposes of the present work, only differential-mode analysis is considered. The differential-mode (DM) half-circuit equivalent is also shown in Figure 60, with load resistance represented as an equivalent shunt admittance Y_L .

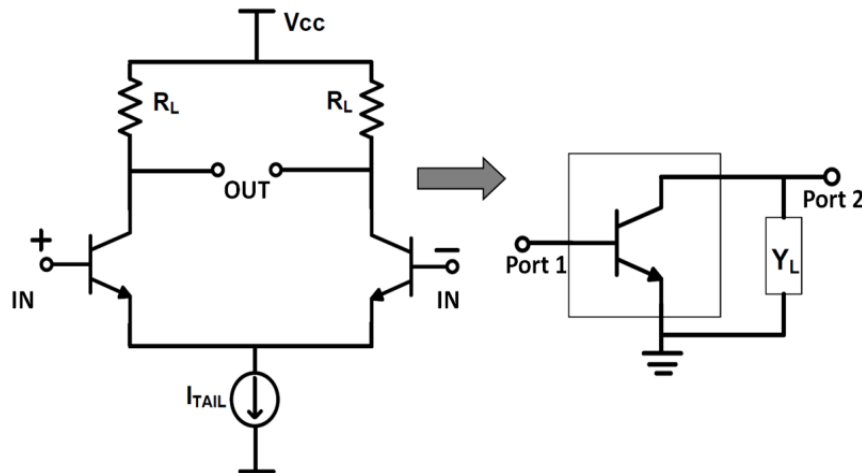


Figure 60. CML gate and equivalent two-port, differential-mode half circuit with load admittance used for Y-parameter analysis.

This equivalent two-port network is used as the basis for our proposed FoM. The idea is that any complex circuit that utilizes a common-emitter (CE) configuration as its building block can be analyzed by combining the Y-parameters of the CE device along with the Y-parameters of any passive components in the circuit. A useful metric obtained in this way is the voltage gain of the two-port network, given by

$$A_V = \frac{-Y_{21}}{Y_L + Y_{22}}. \quad (4.2)$$

This equation captures several delay components into one expression. Y_{21} captures the input time constants, Y_{22} captures the output time constants, and Y_L captures the contributions of any load admittance. A_V is set by the requirements of the application in question. The 3 dB bandwidth of A_V is the FoM that is proposed in [94] and is called the 'available bandwidth' or f_A . That FoM can be obtained for several collector current (I_C) and Y_L combinations for a given low-frequency gain. When plotted over I_C , it generates a curve that resembles the f_T vs. I_C curve. Unlike f_T , however, this FoM captures any delays resulting from the base resistance and input capacitance time constant. In addition, it can be measured directly without the need for any extrapolation, as is required for f_T .

There are several limitations to the f_A FoM. First, the fundamental assumption made was of a certain low-frequency small-signal voltage gain (A_{V0}) of 4 for digital applications and 10 for analog applications. In addition, f_A was made to depend intimately on A_{V0} , which limits the generality of the FoM. A second limitation was that while the FoM used the gain information and 3 dB bandwidth of A_V , it ignored any phase information embedded in the expression. This could potentially lead to discrepancies in accurately predicting large-signal gate delay. Third, the FoM was applied to a $0.4 \times 20.3 \mu\text{m}^2$ device, which was an arbitrarily large device and generally not the preferred choice when targeting high speed wireline applications, where often the smallest geometry transistors are typically used. Finally, the FoM predictions were not compared against large-signal RO simulations or measurements to gauge its efficacy with respect to CML gate delay.

Several of the aforementioned constraints are removed in the present work and a new FoM is proposed that improves upon the previous FoM. As a first step, the transistor size is chosen to be the minimum size available in the technology platform and one that is used for high-speed wireline applications. The next step is to relax the constraint of small-signal gain and instead relate the FoM to large-signal swing. The approach is to identify I_C - R_L combinations for the DM half circuit that would translate to a swing of 150 mV peak in a CML-based ring oscillator circuit, and apply the new FoM for those biasing conditions. With this approach, one can perform an apples-to-apples comparison of small-signal predicted delay and large-signal RO delay at the same biasing condition. The choice of swing is sufficient to switch the tail current almost entirely between the two legs. The I_C - R_L combinations used in this work are listed in Table 5.

Table 5 : I_C - R_L and Avg_ I_C - R_L combinations for the DM half circuit and CML RO circuit.

I_C (μ A)	Avg_ I_C (μ A)	R_L (Ω)
10	5	26k
100	50	2.15k
300	148	692
500	246	412
600	295	373
950	465	247

These are also the I_C - R_L combinations for the CML RO circuit that are used to generate the power-delay curve. Also listed in the table are the I_C values with correction factors to produce the Avg_I_C column. The motivation to include this column will be provided after presenting the new FoM.

As mentioned in the limitations of the previous FoM, the phase information of the A_V transfer function was essentially not used. As is known, the phase information in the transfer function of a two-port network captures phase shifts that a signal experiences as it propagates from input to output. These phase shifts are a result of the multiple dominant and non-dominant R-C poles that exist along the signal path. The phase signature can be quite complex, depending on the number of poles in the transfer function. Interesting observations can be made by looking more carefully at the phase shift and corresponding phase distortion information. The phenomenon of group delay is well known as a metric that captures the phase distortion for both dispersive (non-linear) and non-dispersive (linear) components in units of time. For any arbitrary device-under-test (DUT), its group delay can be represented by the negative derivative of phase over frequency as

$$\tau_{GRP} \stackrel{\text{def}}{=} \frac{-d}{d\omega} [\varphi(j\omega)]. \quad (4.3)$$

For non-dispersive components, the expectation is that τ_{GRP} is constant vs. frequency, while this may not be the case for dispersive components. In the case of the two-port, Y-parameter network utilized, we expect a mix of constant and non-constant segments in the group delay due to the complex nature of the phase shift in a CML gate. Furthermore, we are looking at the phase distortion of a specific transfer function comprising voltage gain in terms of Y-parameters. To gain more insight, we plot group delay, given by

$$\tau_{GRP_FoM} = \frac{-d}{d\omega} \left[\text{phase} \left(\frac{-Y_{21}}{Y_{22}} \right) \right], \quad (4.4)$$

for several Avg_ I_C - R_L combinations obtained from Table 1. There are two important points to be gleaned. First, the Y_L component that was used in equation (4.2) is dropped in equation 4.4, but still exists in the schematic. The addition of Y_L in the equation is observed to have an insignificant impact on the group delay. Second, the subsequent group delay plots use Avg_ I_C rather than I_C as the collector current. The reason for this becomes clear when we analyze the operation of a switching transistor within the CML gate. Over the switching cycle, each transistor conducts current only for a portion of the time. In order to obtain an apples-to-apples comparison between the RO switching delay and a DM half-circuit delay, we need to introduce a correction factor into the I_C for the two-port network. A simple correction factor of one-half the tail current is shown to be adequate. The group delay (equation 4.4) for six Avg_ I_C - R_L combinations over frequency is plotted in Figure 61, while Figure 62 zooms in on a portion of the frequency range in Fig. 2 to reveal further details. Each group delay curve has a distinct signature comprising constant and non-constant segments. Several observations can be made when examining these two plots. First, one notices a very interesting trend in the constant portion of the delay as I_C is swept for a fixed V_{CB} of 0.1 V. At very low I_C , delay on the order of 100 ps is obtained, and as I_C increases, the delay begins to fall until it reaches a minimum of 6.2 ps. The delay starts to rise back again beyond a certain I_C . The significance of the constant portion is that, in this region, the signal experiences a linear phase shift as compared to the non-constant portion where the signal undergoes non-linear phase changes.

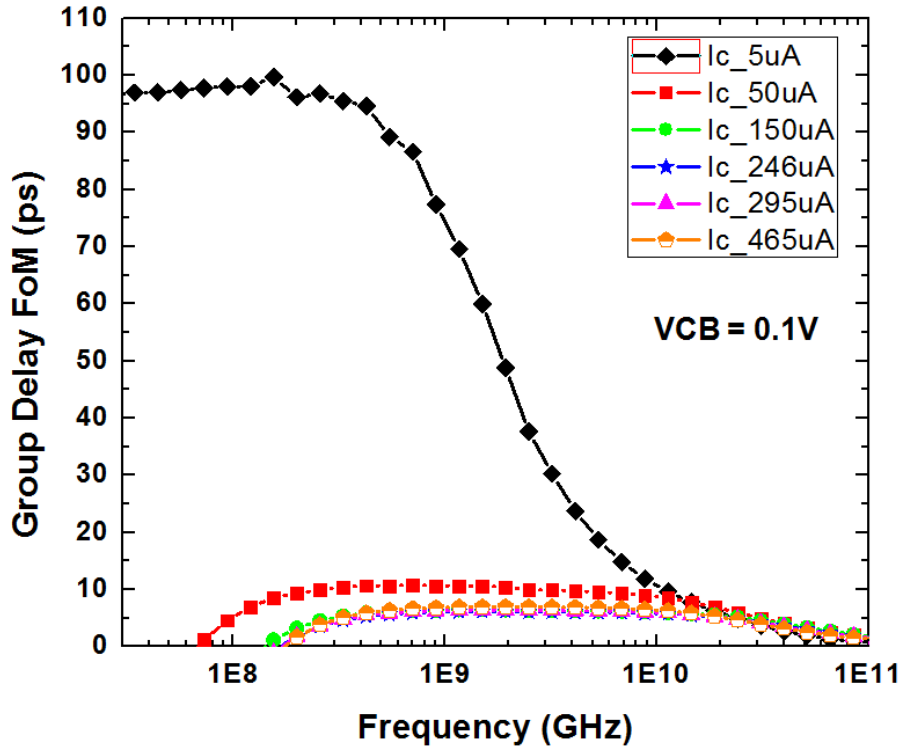


Figure 61. Group delay figure-of-merit plotted vs. frequency for several I_C - R_L combinations.

Second, the frequency range over which the group delay is constant is different for different bias conditions. Third, the group delay is constant for at least a decade of frequencies over the various bias conditions. Fourth, the trend in the constant portion of the group delay over bias is suspiciously similar to the trend noticed in a power-delay curve obtained from ROs. This fourth observation leads us to perform a comparison of group delay obtained from the constant portion with large-signal delay obtained from CML ring oscillators. For this experiment, six 4-stage CML ROs are built with R_L values obtained from Table 5, and minimum size transistors. Figure 62 captures the similarities in trends that we noticed with a log-log plot of gate delay over RO tail current. We observe several interesting phenomena through the curves. First, the group delay as

predicted by equation (4.4) using Avg_IC values closely follows the delay predicted by the simulated 4-stage RO. This is an extremely powerful occurrence since capturing large-signal, non-linear switching behavior with a simple small-signal expression can prove very useful as a prediction tool.

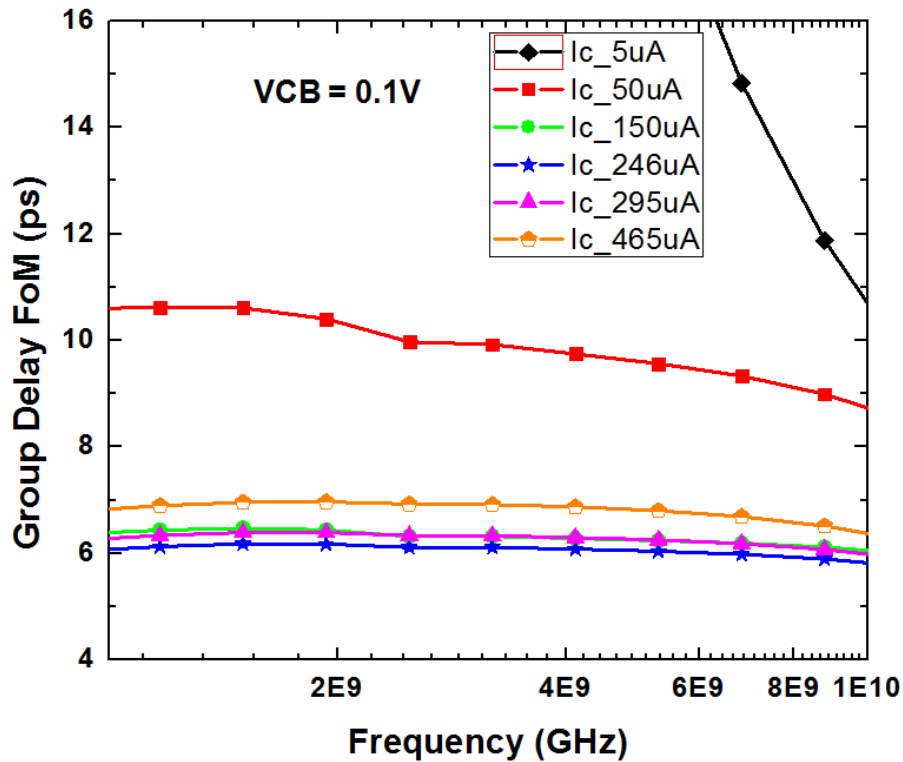


Figure 62. Zoom-in plot of group delay FoM depicting minimum achievable delay and corresponding collector current.

Second, when using the entire I_{TAIL} as I_C for the DM half-circuit, we observe deviations in delay prediction that we expect since the correction factor is not included. There is no better check for a small-signal FoM than to compare its efficacy against an RO. The simple yet accurate predictive behavior of equation (4.4) leads us to propose this as the new Y-parameter FoM. We also include some measured RO results that are available to further close the loop on the experiment.

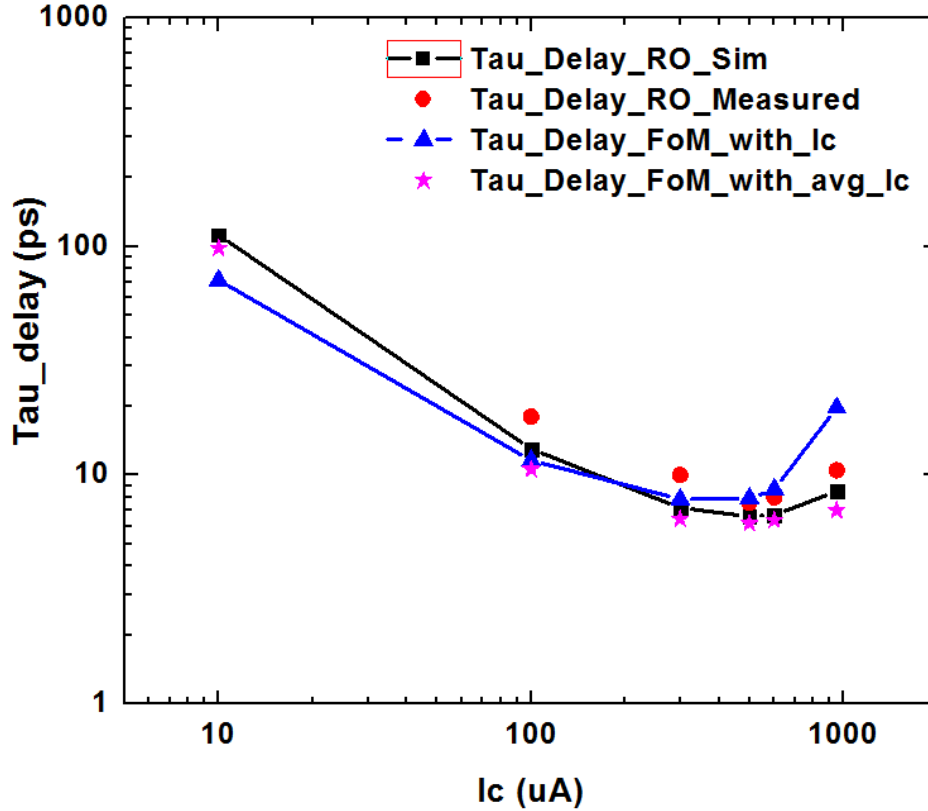


Figure 63. Power-delay curves obtained from simulated and measured ring oscillators compared with the FoM predicted delay.

4.4.3 Y-Parameters to Model Parameters

One of the limitations of a Y-parameter technique as pointed out earlier is that it lacks insight into the physical mechanisms of delay when the network is treated as a black box. This limitation is overcome by applying the same FoM to a two-port network comprising a simplified hybrid-pi model, and obtaining an expression for delay in terms of model parameters. This approach is presented by incrementally building the Y-parameter matrix and then using Y_{21} and Y_{22} components to then derive the delay equation. Figure 64 shows the various Y-parameter components obtained from the hybrid-pi model that

neglects series base resistance. The model captures input and load admittances, as well as contributions from C_{cb} and C_{cs} .

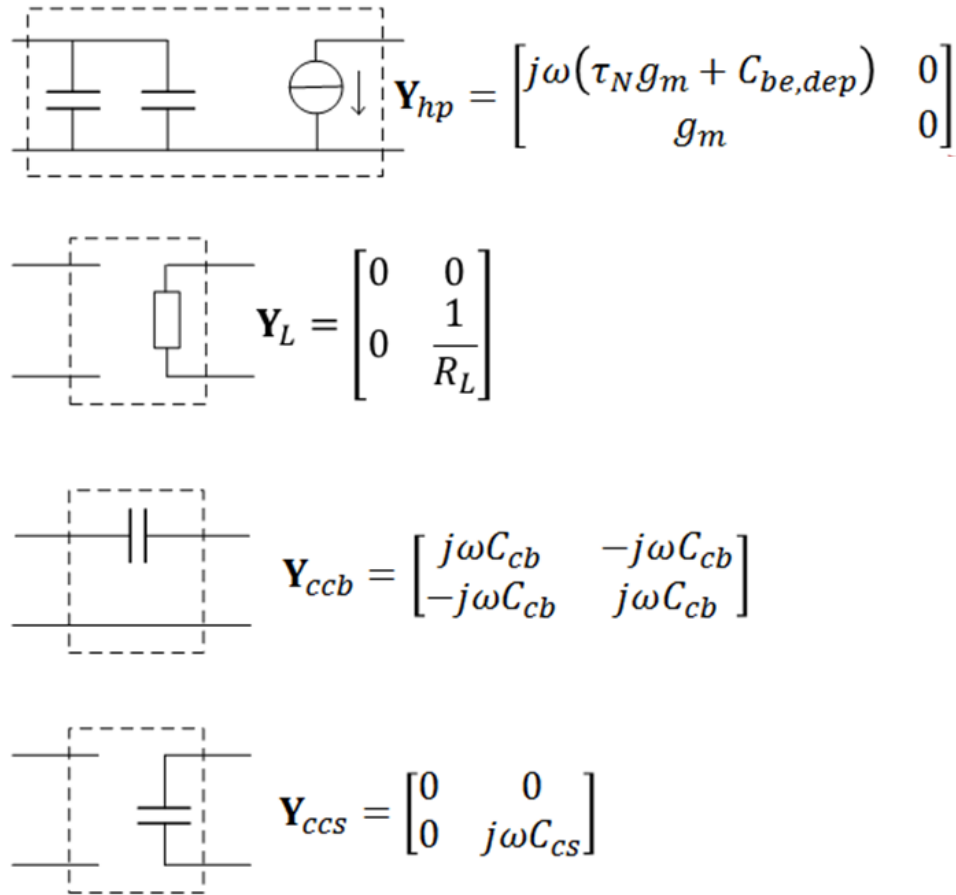
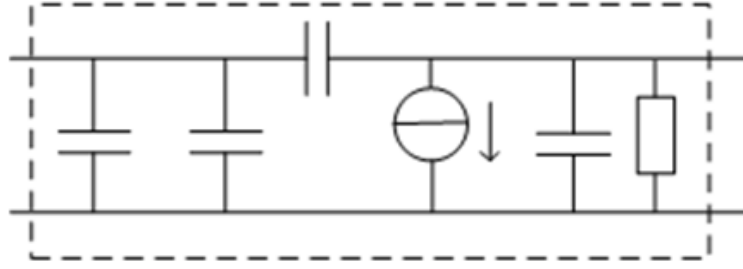


Figure 64. Y-parameter matrix for the different admittances of the two-port simplified hybrid-pi model.

Combining the four components, one obtains the complete Y-parameter matrix for the two-port network as shown in Figure 65 and given by equation (4.5).



$$\mathbf{Y}_{tot} = \mathbf{Y}_{hp} + \mathbf{Y}_L + \mathbf{Y}_{ccb} + \mathbf{Y}_{ccs}$$

Figure 65. Complete Y-parameter matrix incorporating individual admittance components.

$$Y_{Tot} = \begin{bmatrix} j\omega(g_m * \tau_F + C_{je} + C_{cb}) & -j\omega C_{cb} \\ g_m - j\omega C_{cb} & \frac{1}{R_L} + j\omega(C_{cb} + C_{cs}) \end{bmatrix} \quad (4.5)$$

Applying the group delay FoM to the above Y-parameter matrix, one obtains an expression for delay in terms of g_m , C_{cb} , C_{cs} , and R_L given by

$$\begin{aligned} \tau_{GRP_DELAY} &= \frac{C_{cb}}{g_m} \left(1 + \left(1 + \frac{C_{cs}}{C_{cb}} \right) * g_m R_L \right) \\ &= \frac{C_{cb}}{g_m} \left(1 + \left(1 + \frac{C_{cs}}{C_{cb}} \right) * \ln \left(\frac{I_{on}}{I_{off}} \right) \right) \end{aligned} \quad (4.6)$$

Equation (4.6) is derived under the assumption that there is no series base resistance, and that there is no charge partitioning (i.e. all dQ/dI is assumed between base and emitter). To verify its efficacy, we plot the expression in Figure 66 over bias and compare it with the FoM and RO performance. The expression is only valid for the left portion of the

power-delay curve. A more complex curve fitting process would be required to map the parabolic shape of the power-delay curve.

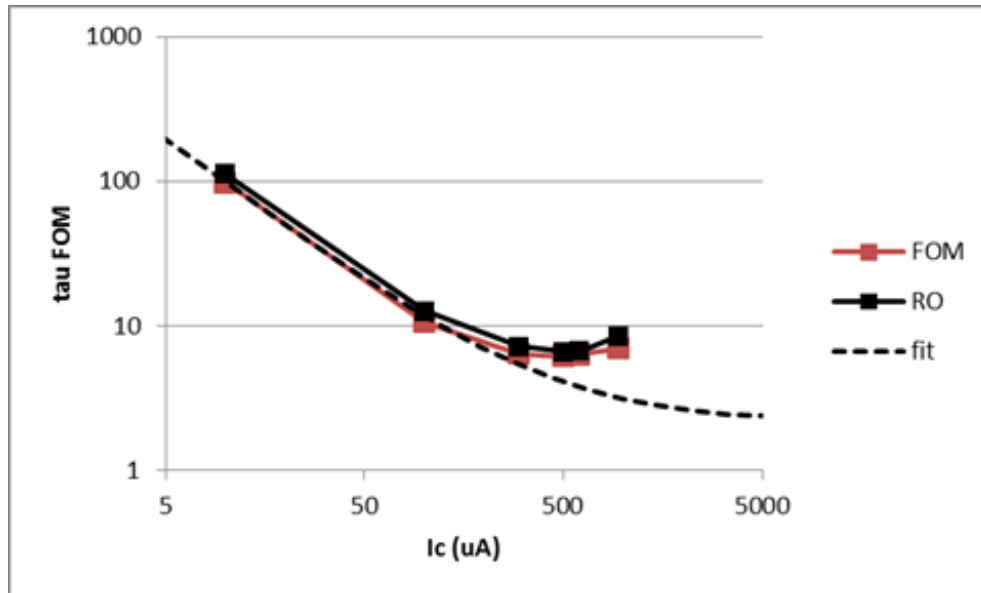


Figure 66. Comparison of Y-parameter FoM, RO, and model parameter expression over bias.

Predicting large-signal gate delay using small-signal techniques has been an extremely important tool from a modeling and technology optimization standpoint. Various techniques exist to accurately predict delay. Some are based on compact-model parameters and others use a Y-parameter approach. The present work uses the latter technique to create a FoM that can be obtained from simple Y-parameter simulations or measurements. The FoM is able to accurately map the power-delay curve and its efficacy is tested by comparison with ring oscillators. A model parameter equation extracted using the same technique is also presented to provide more physical insight into the delay components.

V CONCLUSIONS AND FUTURE WORK

5.1 Summary of Contributions

The objective of the proposed research is to demonstrate the design of frequency synthesizers in novel wireless and wireline systems using SiGe BiCMOS technologies. A secondary goal is to establish that SiGe HBTs provide manufacturers with a low-cost solution for complete system-on-a-chip integration in silicon. The research focuses on identifying three novel applications to demonstrate the stated goals. The first application addresses the incorporation of self-healing into mixed signal electronic systems. Such systems can be extremely beneficial in harsh (extreme) environments or for long duration missions such as required in space exploration, where repairs and maintenance are either impractical or cost prohibitive. A conceptual healing system is proposed, and test signal sources for self-healing are presented along with a demonstration of on-die IRR healing.

The second application is geared towards utilizing the high f_T/f_{max} values offered by state-of-the art process technologies. The high cut-off frequencies allow circuit designers to build systems at increasingly higher operating frequencies. A 94 GHz pulsed-radar imaging system is proposed that offers resolution on the order of a few millimeters. A 94 GHz oscillator that is used to upconvert the baseband pulse is demonstrated with 13 GHz of tuning range around the 92 GHz center frequency.

The third application focuses on emerging multi-gigabit wireline systems from a process technology development standpoint. Several important characterization techniques are demonstrated that can be used to tweak the process so as to ultimately support robust 40/100 Gbps signaling in wireline transceivers. A circuit invariant FoM is

proposed that predicts large-signal gate delay using small signal Y-parameter techniques for fast process optimization.

5.2 Future Work

Several logical research extensions of the present works can be made. A few of these are listed for each of the three application areas.

5.2.1 Self-Healing Receivers

In this work, it was shown that the test signal source was used to heal for IRR of the image-reject mixer. Efforts (not shown in this work) to demonstrate full receiver chain healing of gain, linearity, image rejection, and noise figure have also been successful for a few die. In the future, several die from different wafer lots would need to be measured in order to demonstrate the efficacy of self-healing over process variations. Self-healing as it applies to overcome temperature variations also need to be demonstrated at cryogenic and high temperatures. Lastly, self-healing in the context of radiation effects on electronics would also be of great interest to the scientific community.

5.2.2 Millimeter-Wave Systems

Measured results of the 94 GHz oscillator were shown in this work with 14% tuning range around 92.5 GHz. The next step would be to incorporate the VCO inside of a 94 GHz PLL to meet the phase noise specifications for imaging applications. New and emerging applications are also being proposed at ever higher frequencies. Meeting the challenging design specifications at 120 - 180 GHz would require innovative thinking and out-of-the box techniques for successful demonstrations.

5.2.3 Multi-Gigabit Wireline Systems

In Section 4.2, various benchmarking techniques were presented to assess the capabilities of a process technology geared towards robust 40 Gbps wireline applications. Accurate characterization of important figures-of-merit such as f_T/f_{\max} , τ_{delay} , and power-delay product were demonstrated. The CML gate was identified as the critical building block on which to perform further characterization and analysis.

In Section 4.3, preliminary data for linearity of single devices and CML structures was compared and noticeable degradation was found in the IIP3 of the CML structure. The next step would be to identify the various sources of nonlinearities in the single device and CML structure using Volterra series analysis technique. The technique is versatile and powerful in its ability to distinguish between the individual sources of nonlinearity and hence quantify the dominant and weak sources. A small signal model for the single device and CML gate can be created and Matlab code can be used to perform Volterra analysis on each of the models.

In Section 4.4, a FoM was proposed that predicts large-signal gate delay using Y-parameters. The efficacy of the FoM was verified by comparing it with ring oscillator simulations and measured results. The next step would be to use the FoM to predict delay of more complex circuit blocks such as latches, flip-flops, frequency dividers, and shift registers. In addition, a model parameter based FoM will also be required that provides insight into the components contributing to delay. While a simplified model parameter FoM was presented in this work, a more sophisticated model will be required to map the parabolic shape of the power-delay curve.

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