PRODUCTION AND PROPERTIES OF EPITAXIAL GRAPHENE ON THE CARBON TERMINATED FACE OF HEXAGONAL SILICON CARBIDE

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Physics

Georgia Institute of Technology
December 2013

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PRODUCTION AND PROPERTIES OF EPITAXIAL GRAPHENE ON THE CARBON TERMINATED FACE OF HEXAGONAL SILICON CARBIDE

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To my parents, Shiwen Wang and Yingyou Hu

ACKNOWLEDGEMENTS

I sincerely thank my advisor Dr. Walter de Heer for giving me the opportunity to work on the revolutionary research topic in a pioneering group. This work could not have been done without his support and guidance. I also gratefully appreciate the mentoring from Dr. Claire Berger during my graduate studies. I express my sincere gratitude toward my other committee members: Dr. Edward Conrad, Dr. Philip First, Dr. Zhigang Jiang, and Dr. Samuel Graham.

I greatly thank my lab members for their experimental help and insightful discussions: Dr. Jan Kunc, Dr. Xiaosong Wu, Dr. Michael Sprinkle, Dr. Ming Ruan, Dr. Xuebin Li, Dr. Fan Ming, Dr. Miguel Rubio, Dr. Farhana Zaman, Dr. Rui Dong, Dr. Lei Ma, John Hankinson, Zelei Guo, James Palmer, Baiqian Zhang, Karen Madiomanana, and Andrei Savu. I also thank my collaborators for the collaborations that enriched my knowledge: Dr. Elisa Riedo, Dr. Joseph Stroscio, Dr. Zhigang Jiang, Dr. Li You, Dr. Suenne Kim, Dr. Debin Wang, Dr. Anton Sidorov, Dr. Felipe Birk, Dr. Jia-An Yan, Dr. Jeremy Hicks, Feng Wang, Dr. Sonam Sherpa, Wenchao Jiang, Tien Hoang and Hsin-Ju Wu. I also would like to thank the graphene journal club members who brought enthusiastic discussions to the new discoveries: Dr. Joanna Hass, Dr. D. Lee Miller, Dr. Kevin Kubista, Dr. Chris Malec, Dr. Britt Torrance, and Yuntao Li.

I thank my friends for their support over years: Danjue Chen, Lede Xian, Yuzheng Guo, Chenyi Pan, Vrinda Khetan, Liwei Zhang, and Solomon Smith. I also thank my brave brother Yiting Hu. Last but not least, I would like to thank my parents for their unconditional love; their vision, support and discipline have made me who I am.

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LIST OF ABBREVIATIONS

Abbreviations	Descriptions
2DEG	two-dimensional electron gas
AFM	atomic force microscopy
ARPES	angle-resolved photoemission spectroscopy
CCS	confinement controlled sublimation
CMOS	complementary metal–oxide–semiconductor
CMP	chemical mechanical polishing
CNL	charge neutrality level
CVD	chemical vapor deposition
EBL	electron beam lithography
EFM	electrostatic force microscopy
EG	epitaxial graphene
FET	field effect transistor
GO	graphene oxide
HOPG	highly oriented pyrolytic graphite
I-AFM	current-atomic force microscope
ICP	inductively coupled plasma
LEED	low energy electron diffraction
LLs	Landau levels
MEG	multilayer epitaxial graphene
ML	monolayer
MOSFET	metal–oxide–semiconductor field effect transistor
QHE	quantum Hall effect

Abbreviations	Descriptions
RGO	reduced graphene oxide
RIE	reactive-ion etching
SCL	space-charge-limited
SdHOs	Shubnikov–de Haas Oscillations
SEM	scanning electron microscopy
SP	spontaneous polarization
STM	scanning tunneling microscopy
UHV	ultra-high vacuum
XPS	x-ray photoelectron spectroscopy

SUMMARY

Graphene is widely considered to be a promising candidate for a new generation of electronics, but there are many outstanding fundamental issues that need to be addressed before this promise can be realized. This thesis focuses on the production and properties of graphene grown epitaxially on the carbon terminated face (C-face) of hexagonal silicon carbide leading to the construction of a novel graphene transistor structure. C-face epitaxial graphene multilayers are unique due to their rotational stacking that causes the individual layers to be electronically decoupled from each other. Well-formed C-face epitaxial graphene single layers have exceptionally high mobilities (exceeding 10,000 $cm^2V^{-1}s^{-1}$), which are significantly greater than those of Si-face graphene monolayers. This thesis investigates the growth and properties of C-face single layer graphene. A field effect transistor based on single layer graphene was fabricated and characterized for the first time. Aluminum oxide or boron nitride was used for the gate dielectric. Additionally, an all graphene/SiC Schottky barrier transistor on the C-face of SiC composed of 2DEG in SiC/Si_2O_3 interface and multilayer graphene contacts was demonstrated. A multiple growth scheme was adopted to achieve this unique structure.

CHAPTER 1

INTRODUCTION

1.1 Graphene

Carbon is the basic element of organic materials. Depending on how the carbon atoms are bonded, carbon-based systems can be divided into groups with different physical and chemical properties. The three-dimensional (3D) allotrope of carbon, graphite, is well known for being used in pencils. Graphite can be viewed as layers of honeycomb carbon lattice weakly coupled together by van der Waals forces, stacking on top of each other with 60^{o} rotation. The zero-dimensional allotropes of carbon, buckminsterfullerene, were discovered in 1985 (Kroto, et al., 1985). They are molecules in which carbon atoms are arranged spherically. They can be viewed as one layer of a honeycomb carbon lattice rolled up with the introduction of pentagons. The one-dimensional allotrope of carbon is the nanotube, which has a cylindrical structure (Ijima, et al., 1993; Bethune, et al., 1993). It can be viewed as one layer of a honeycomb carbon lattice rolled at specific angles. The combination of the rolling angle and radius decides the nanotube properties. In summary, graphite, buckminsterfullerene, and carbon nanotube can be viewed as structures in different dimensions made of a two-dimensional honeycomb carbon lattice. This two-dimensional honeycomb carbon lattice structure, which is also considered as one layer graphite, is graphene.

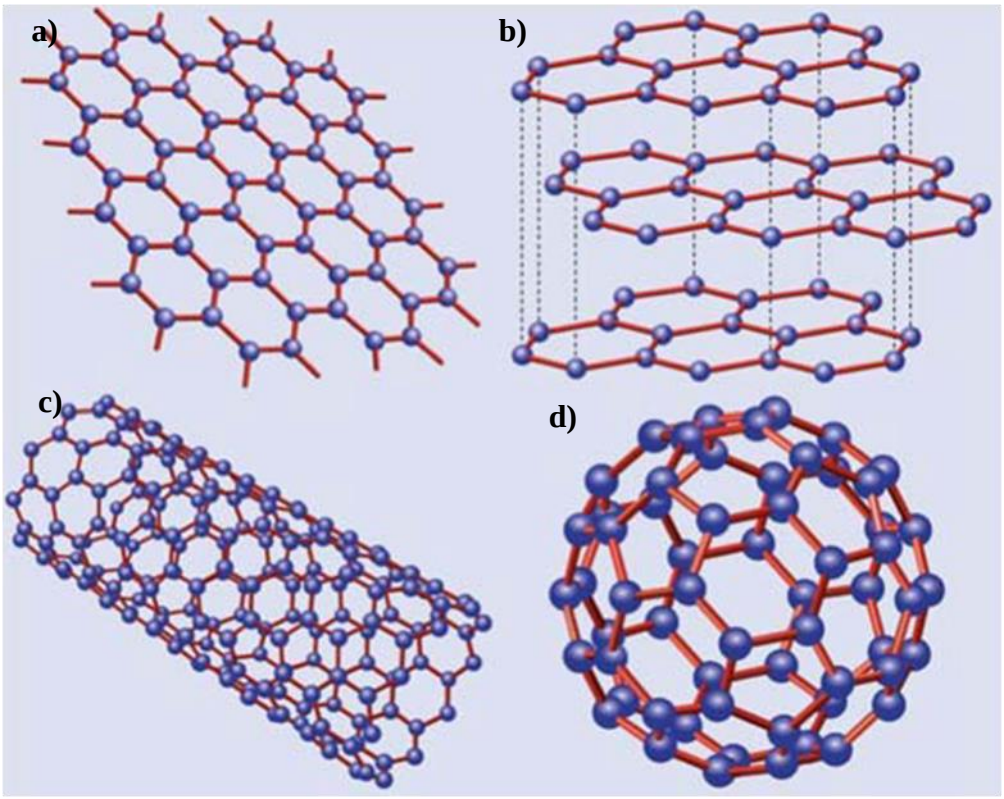

Figure 1.1 Graphene (a) is a honeycomb lattice of carbon atoms. Graphite (b) can be viewed as a stack of graphene layers. Carbon nanotubes (c) are rolled-up cylinders of graphene. (d) Fullerenes, e.g., C_{60}, are molecules consisting of wrapped graphene by the introduction of pentagons on the hexagonal lattice. (Castro Neto et al., 2006)

1.2 Graphene Band Structure

The graphene honeycomb structure can be considered as the repeat of a unit cell with two-atom basis, which has lattice vectors $a_1 = \left(\frac{a}{2}\right)(3, \sqrt{3})$ and $a_2 = \left(\frac{a}{2}\right)(3, -\sqrt{3})$, ($a \approx 1.42$ Å is the carbon-carbon lattice distance). The reciprocal lattice vectors are given as $b_1 = \frac{2\pi}{3a}(1, \sqrt{3})$, and $b_2 = \frac{2\pi}{3a}(1, -\sqrt{3})$. The two inequivalent corners of Brillouin zone are called Dirac points, defined as $K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right)$ and $K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right)$.

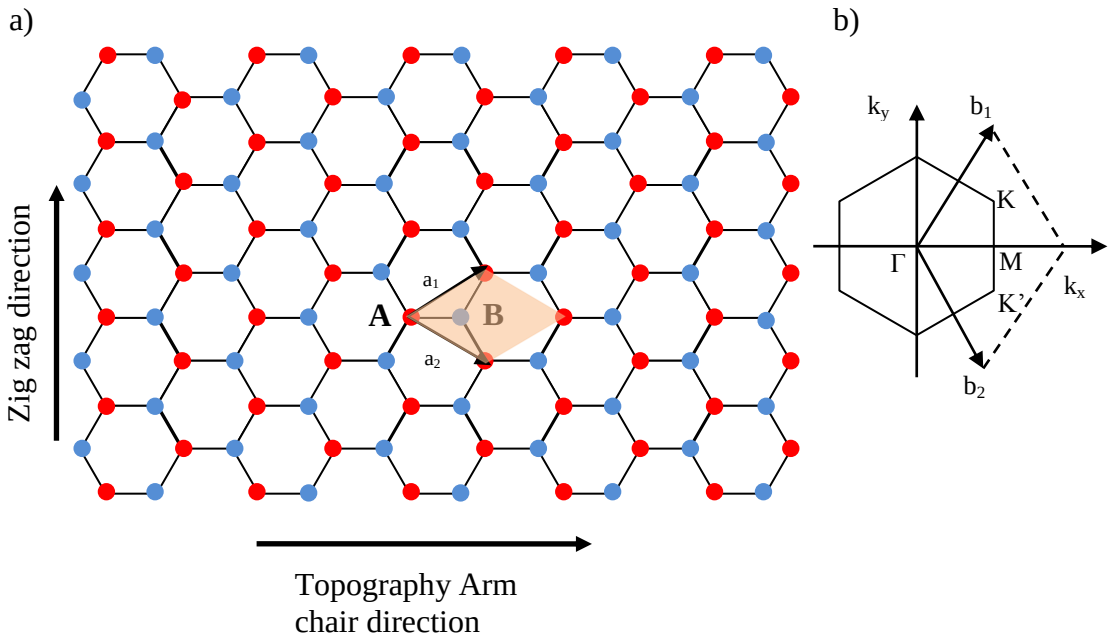

Figure 1.2: a) Graphene honeycomb lattice structure with two atoms in each basic unit cell. a_1 and a_2 are the lattice unit vectors. The horizontal direction is the armchair direction while the vertical direction is the zigzag direction. b) Corresponding Brillouin zone. The Dirac cones are located at the K and K' points.

The graphene electronic band structure can be calculated with tight binding model (Wallace, 1947) by considering that electrons can only hop to both the nearest (inter sub-lattice A→B) and next nearest neighbor atoms (intra sub-lattice A→A', or B→B'). An approximate analytical expression around the conduction band and valence band can be derived as

$$E_{\pm}(q) \approx 3t' \pm \hbar \upsilon_F |q| - \left(\frac{9t'a^2}{4} \pm \frac{3ta^2}{8} \sin(3\theta_q) \right) |q|^2 \qquad (1\text{-}1)$$

with $\upsilon_F = \frac{3ta}{2}$, $\theta_q = \arctan^{-1}\left[\frac{q_x}{q_y}\right]$, a is the carbon-carbon bond length, and t, t' are the nearest neighbor and the next nearest neighbor hopping amplitudes, $t \approx 2.7$ eV $>> t' \approx 0.1$ eV. When neglecting t' and considering only small q relative to the Dirac point, the above energy dispersion relation can be written as

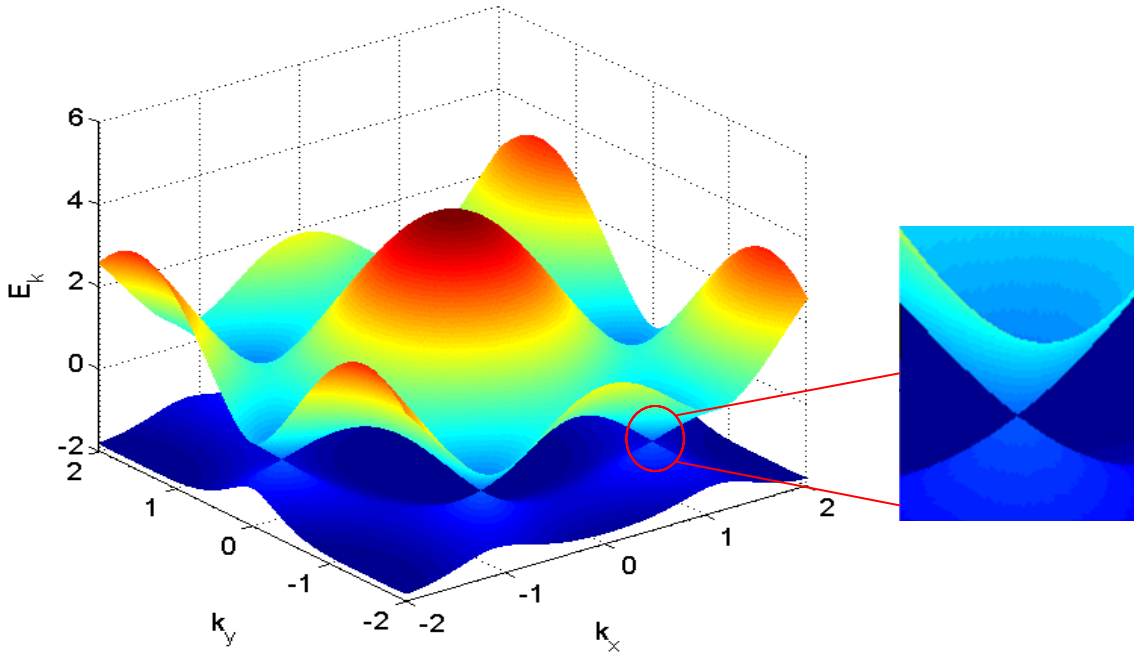

Figure 1.3: Electronic dispersion in the honeycomb lattice using the tight binding calculation. Left: energy spectrum (in units of t) for finite values of t and t', with t= -2.7 eV and t' =−0.1 eV. Right: energy bands close to one of the Dirac points.

$$E_{\pm}(q) \approx \pm \hbar \upsilon_F |q| + \mathrm{O}(\frac{q}{k})^2 \qquad (1\text{-}2)$$

The most intriguing feature from the graphene energy dispersion is the linear energy momentum relationship with the conduction and valence bands intersecting at q = 0, with no energy gap. Graphene is thus a zero band-gap semiconductor with linear long wavelength energy dispersion for electrons (holes) in the conduction (valence) band. The existence of two Dirac points at K and K', where the electron and hole band touches (Figure 1.3) each other in the momentum space, gives rise to a valley degeneracy g_v = 2 for graphene.

The constant $\upsilon_F = \frac{3ta}{2}$ at a = 1.42 Å, t = 2.7 eV gives a $v_F = 1\times10^6 m/s$. This linear energy momentum dispersion relation is significantly different from the traditional 2D materials with $E = \frac{p^2}{2m} = \frac{\hbar^2 k^2}{2m}$, and greatly resembles that of ultrarelativistic particles. These particles are quantum mechanically described by the Weyl-Dirac equation. This massless Dirac dispersion gives rise to some unique electronic properties in graphene unseen in other 2D materials. A few are listed below:

(1) The cyclotron mass depends on the electron density as its square root

$$m^* = \frac{\sqrt{\pi n}}{v_F} \qquad (1\text{-}3)$$

Experimental observation of the *n* dependence on the cyclotron mass provides evidence for the existence of massless Dirac quasiparticles in graphene (Novoselov, et al., 2005b; Zhang et al., 2005)

(2) The density of states close to Dirac point is proportional to energy

$$\rho(E) = \frac{2A_c}{\pi}\frac{|E|}{\upsilon_F{}^2} \qquad (1\text{-}4)$$

where A_c is the unit cell area given by $A_c = \frac{3\sqrt{3}a^2}{2}$

(3) In the presence of perpendicular magnetic field *B*, the energy level is given by (McClure, 1956)

$$E_{\pm}(N) = \pm\omega_c\sqrt{N} = \pm\sqrt{2N}\frac{v_F}{l_B} = \pm v_F\sqrt{2NeB\hbar} \quad (1\text{-}5)$$

where N is an integer number, $\hbar$ is the Planck constant, v_F is Fermi velocity.

1.3 Preparation Methods

Although the theoretical calculations about graphene properties have existed for many decades (Wallace, 1947) and graphite thin film has been grown by all types of

methods over decades, global interest in this material had not been sparked until two independent electrical measurement results were published in 2004. The Georgia Tech group (Berger, et al., 2004) demonstrated that ultrathin epitaxial graphite films grown on SiC with 2D electron gas behavior could be patterned via conventional lithographic techniques, and its conductance could be modulated with a top gate electrode. These key elements suggested that electronic device applications based on nanopatterned epitaxial graphene (NPEG) have the potential for large-scale integration. In the meantime, the Manchester group (Novoselov, et al., 2004) demonstrated that crystalline graphitic film with a few atoms thick exhibited a strong ambipolar electric field effect. Electrons and holes with room-temperature mobility of 10,000 cm^2/Vs can be introduced up to 10^{13} cm^{-2} in concentration by applying gate voltage. The breakthrough for those experiments is the optimized method to prepare and identify thin layer graphite or graphene. In this section, four most common methods to prepare graphene and their material property characterizations will be discussed.

1.3.1 Exfoliated Graphene

Exfoliated graphene can be obtained by mechanical exfoliation of thin graphitic layers from natural graphite or HOPG with scotch tape. This exfoliation method has also been applied to obtain other two-dimensional materials, such as hexagonal boron nitride (Alem, et al., 2009) and MoS_2 (Radisavljevic, et al., 2011). The original method is described as (Novoselov, et al., 2005a): A fresh surface of graphite is rubbed against another surface and left a variety of flakes attached to it. The preliminary identification of single layer amid thicker flakes and other residue is done in an optical microscope. Single layer becomes visible on top of an oxidized Si wafer (300nm SiO_2) since the interference color changes with respect to that of an empty substrate (phase contrast). Further analysis was done by atomic force microscopy (AFM), SEM and Raman microscopy. Graphene made from this method can virtually be transferred to any substrate or no substrate.

Suspended graphene was achieved by etching away SiO_2 underneath with wet chemistry (Bolotin, et al., 2008). Graphene on hexagonal boron nitride was demonstrated by transferring graphene onto the top of a few layer h-BN (Xue, et al., 2011).

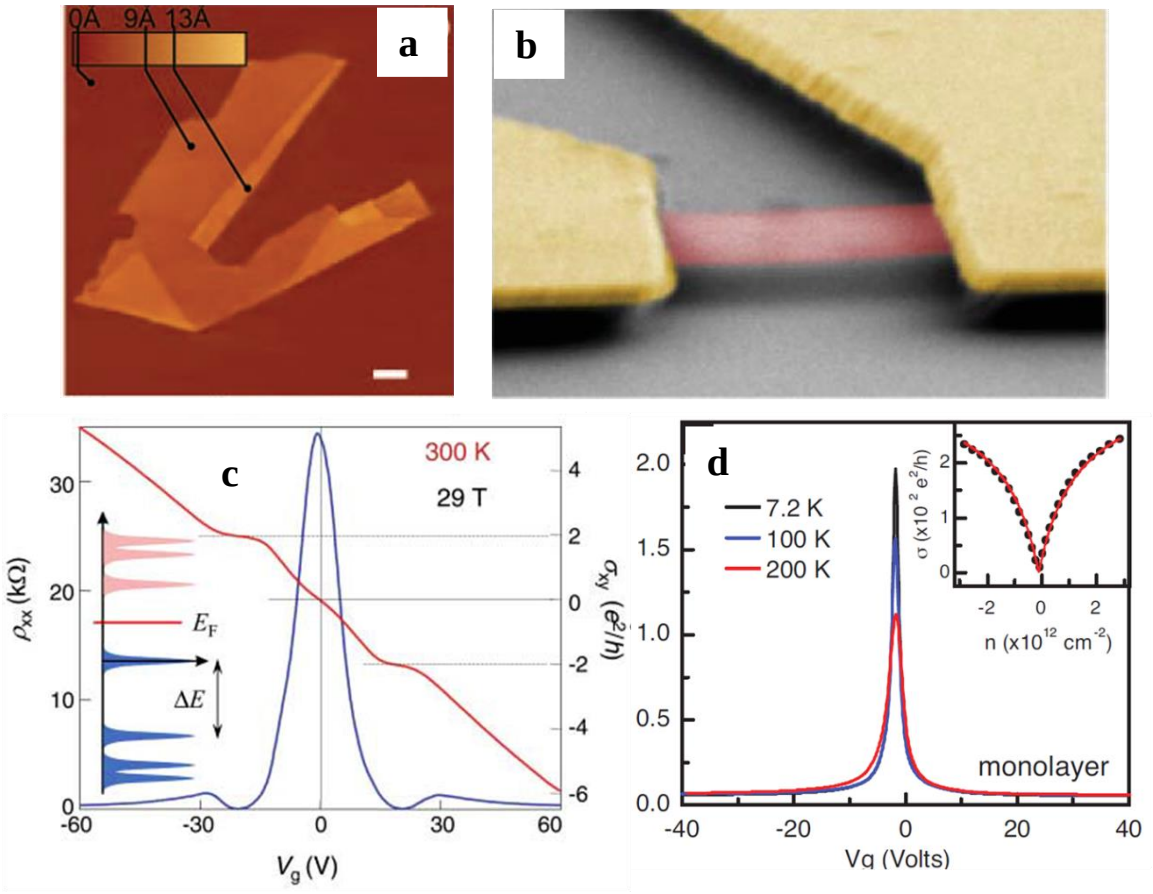

Figure1.4: Examples of exfoliated graphene. a) Single-layer crystallites graphite on top of an oxidized Si wafer visualized by AFM (Novoselov, et al., 2005). b) False-color scanning electron micrograph of a suspended graphene device. Single layer graphene (red) is suspended 150 nm above SiO_2/Si substrate (grey) and supported by two gold electrodes (yellow) (Bolotin, et al., 2009). c)Room-temperature quantum Hall effect in graphene (Novoselov, et al., 2007). d) Resistance versus applied gate voltage for monolayer graphene on h-BN and its FET mobility near the charge neutrality point is 140,000 cm^2/Vs (Dean, et al., 2010).

Application of exfoliated graphene is limited by the sample size available from exfoliation process (at most 100 μm). Thereafter it has attracted more interest in research lab for its easy accessibility. Many graphene characteristic properties have been demonstrated on exfoliated graphene, including unconventional integer quantum Hall

effect at cryogenic temperature (Novoselov, et al., 2005b; Zhang et al., 2005) and room temperature (Novoselov, et al., 2007), fractional quantum Hall effect (Du, et al., 2009; Bolotin, et al., 2009; Dean, et al., 2011), and ultrahigh mobility up to 125,000 cm^2/Vs at room temperature (Zomer, et al. 2011). Bi-layer and tri-layer exfoliated graphene are also of interest due to their tunable band gap opening under perpendicular electric field (Castro, et al. 2008; Lui, et al. 2011).

1.3.2 Chemical Vapor Deposition Graphene on Metals

The formation of graphite layers resulting from preparation of transition metal surfaces has been known for more than 50 years (Banerjee, et al., 1961). The growth mechanism of graphite was proposed to be the consequence of diffusion and segregation of carbon impurities from the bulk metal to the surface during the annealing and cooling stages. Graphene growth has been demonstrated (Mattevi, et al., 2010) on a variety of transition metals such as Ru (Sutter, et al. 2008), Ir (Coraux, et al., 2008), Ni (Rein, et al., 2009) via simple thermal decomposition of hydrocarbons on the surface or surface segregation of carbon upon cooling from a metastable carbon–metal solid solution. One example (Li, et al., 2009) of graphene CVD growth process on Cu foils is: (1) fill vacuum system with hydrogen, heat it to 1000 ^oC and maintain a H_2 pressure of 40 mTorr under a 2 sccm flow; (2) heat Cu film up to 1000 ^oC, and introduce 35 sccm of CH_4 for a desired period of time at a total pressure of 500 mTorr; (3) after exposure to CH_4, the furnace was cooled to room temperature.

Graphene grown by this method is proved to be the same two-dimensional material with mobility around 2000 cm^2/Vs. Different from exfoliated graphene, CVD graphene can grow into tens of inches in size depending on the substrate (Kim, et al., 2010). The opto-electronic properties of monolayer CVD graphene reveal transmittance value of 97.4% and conductance value of 125 Ω/sq (Bae, et al., 2010). Touch screens made of CVD graphene have been demonstrated and its replacement of ITO as

transparent conductor is promising. The major challenge of this method is the thickness inhomogeneity and low carrier mobility limited by graphene domain grain boundaries (Huang, et al., 2011; Tsen, et al., 2012).

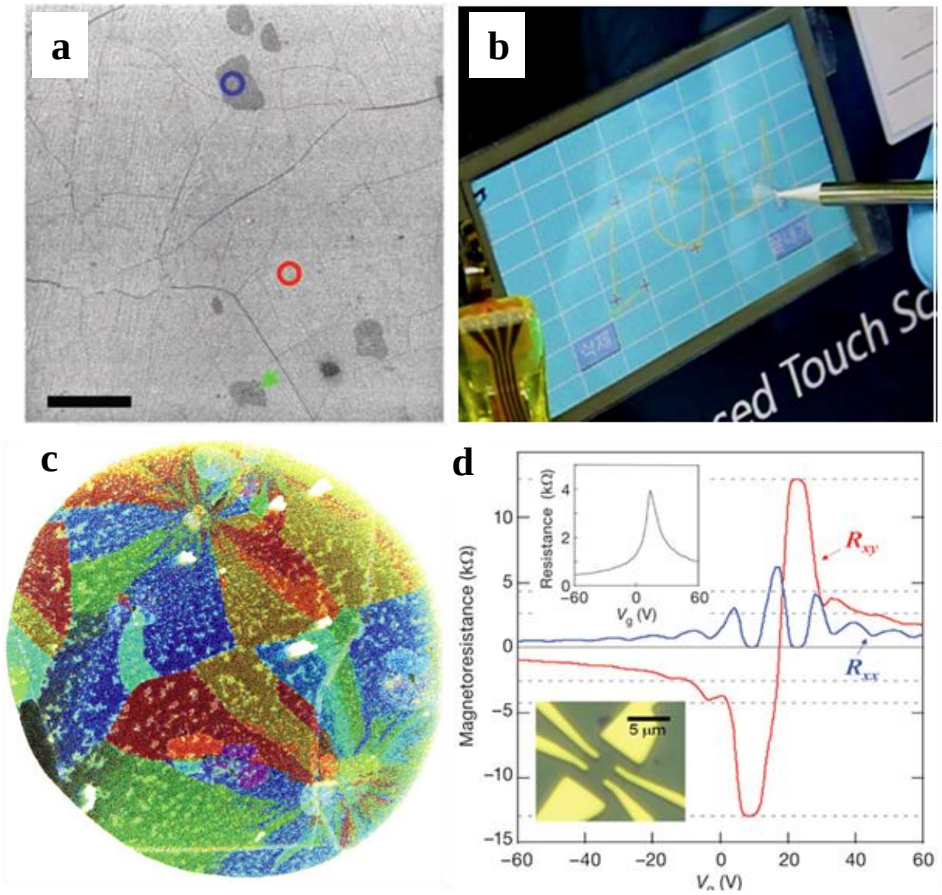

Figure 1.5: Examples of chemical vapor deposited graphene. a) SEM image of CVD graphene transferred on SiO_2/Si (285-nm-thick oxide layer) showing wrinkles, as well as two- and three-layer regions (Li, et al., 2009). b) A CVD graphene-based touch-screen panel connected to a computer with control software (Bae, et al., 2010). c) Large-scale CVD graphene grain imaging using dark field TEM (Huang, et al., 2011). d) Electrical properties of CVD monolayer graphene devices showing the unconventional integer quantum Hall effect and mobility 3750 cm^2/Vs at a carrier density of 5×10^{12} cm^{-2} (Kim, et al, 2009).

1.3.3 Reduced Graphene Oxide

The method to prepare graphite oxide from oxidizing graphite with $NaNO_3$ and H_2SO_4 mixed solution was first introduced in 1957 (known as Hummers' method). During the harsh oxidation and thermal expansion process, thin layers of graphite oxide

are formed. Additional ultrasonication of solution can expand the graphite oxide flakes into single layer graphene oxide. Researchers have found that by exposing such graphite oxide layers in the saturated vapor of dimethylhydrazine (Eda, et al., 2008), or through thermal annealing (Ganguly, et al., 2011) the oxygen functional groups in graphene oxide can be greatly reduced and material conductivity can be enhanced. Raman spectrum confirms such reduced graphene oxide has the graphene featured 2D peak (Eda, et al., 2008). A reduced graphene oxide (RGO) has a good conductivity compared to graphene oxide and can be made in large quantity. But the chemical process also introduces defects in RGO lattice structure and the oxygen functional groups formed during the oxidation process cannot be fully removed by the reduction method.

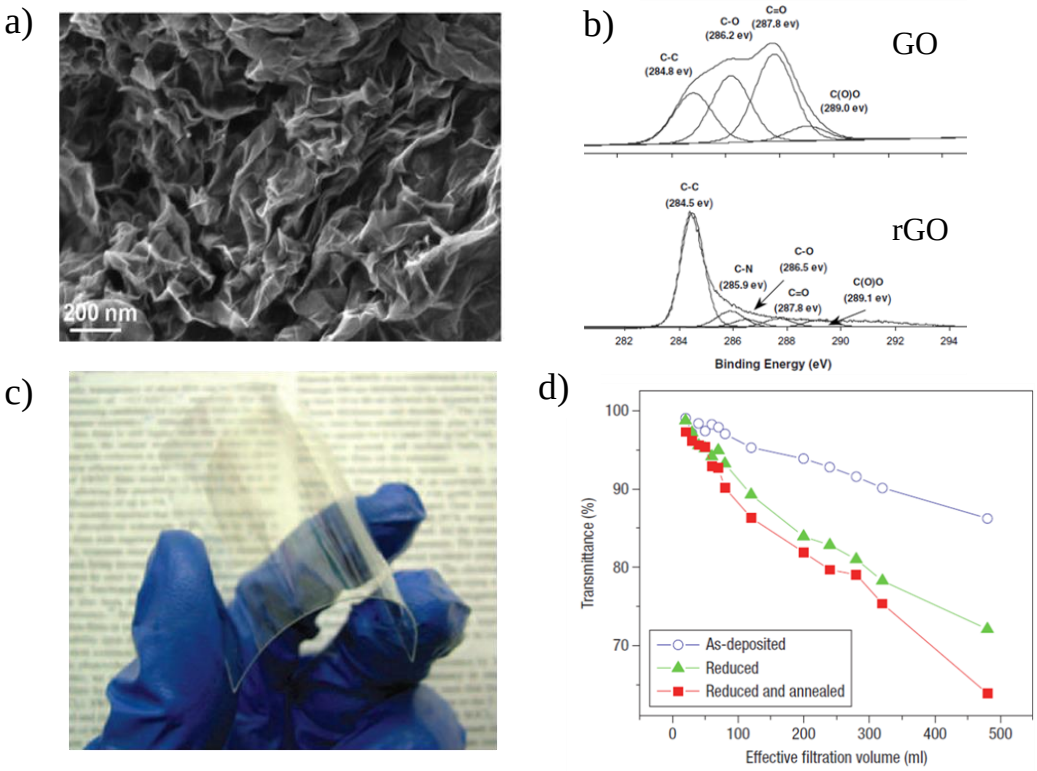

Figure 1.6: Examples of reduced graphene oxide. a) An SEM image of aggregated reduced GO sheets (Stankovich, et al. 2007). b) The C1*s* XPS spectra of GO and reduced GO (Stankovich, et al. 2006). c) Photographs of GO thin films on plastic substrates; d) transmittance at λ=550 nm as a function of filtration volume for reduced GO thin films (Eda, et al., 2008).

1.3.4 Epitaxial Graphene on Silicon Carbide

Graphite monolayer films were first grown and identified on hexagonal silicon carbide in ultrahigh vacuum (UHV) at temperature above 800°C (van Bommel et al., 1975). They are essentially electronically decoupled from the SiC substrate (Forbeaux, et al., 1998). Sublimation from the SiC causes a carbon rich surface that nucleates an epitaxial graphene layer. The graphene growth rate was found to depend on the specific SiC polar face: graphene forms much slower on the silicon-terminated face (Si-face) than the carbon-terminated face (C-face). The semi-insulating and large band gap SiC substrate makes it a natural platform for graphene device fabrication and operation (Berger, et al. 2004). The graphene-SiC system is considered to be compatible for electronic device applications.

1.3.4.1 Silicon Face SiC Epitaxial Graphene

Different from the original UHV graphitization process, large area mono layer Si-face graphene can grow by introducing 1 atmosphere argon into the UHV system. The morphology and electronic properties for as-grown graphene were significantly improved from that of UHV growth (Emtsev, et al., 2009). Low energy electron diffraction (LEED) and angle resolved photoemission spectroscopy (ARPES) reveal that Si-face monolayer graphene exhibits the characteristic graphene linear electronic band structure. Si-face graphene exhibits an intrinsic electron doping ($n=1\times10^{13}$ cm^{-2}) (Rollings et al., 2006; Ohta, et al., 2006). It is found there is a $6\sqrt{3}\times6\sqrt{3}$ reconstructed interface layer (Riedl, et al., 2007) in-between graphene and SiC substrate. This interface, called the buffer layer, consists of carbon atoms arranged in a graphene-like honeycomb structure except that about 30% of these carbon atoms are bound covalently one otherwise to the Si atoms of the SiC (0001) surface (Mattausch, et al., 2007). The buffer layer can be decoupled from

the substrate and converted into monolayer graphene through different molecular intercalations, for example, hydrogen intercalation (Riedl, et al., 2009), oxygen intercalation (Oida, et al., 2010) and gold intercalation (Gierz, et al., 2010). Like graphite, Si-face bilayer graphene exhibits parabolic bands and the band structure evolves to that of graphite with increasing thickness. A typical Si-face graphene has mobility about 1,000 cm^2/Vs due to the substrate interaction. Quasi-freestanding epitaxial graphene obtained by hydrogen intercalation has improved sample mobilities to 3,000 cm^2/Vs at a carrier density of $5\times10^{12}\ cm^{-2}$ (Speck, et al., 2011). Unconventional integer quantum Hall effect was observed on Si-face graphene with and without a top gate, which confirms the relativistic particle properties in epitaxial graphene on the Si-face of SiC (Shen, et al., 2009; Pan, et al., 2010; Jobst, et al., 2010; Tzalenchuk, et al., 2010).

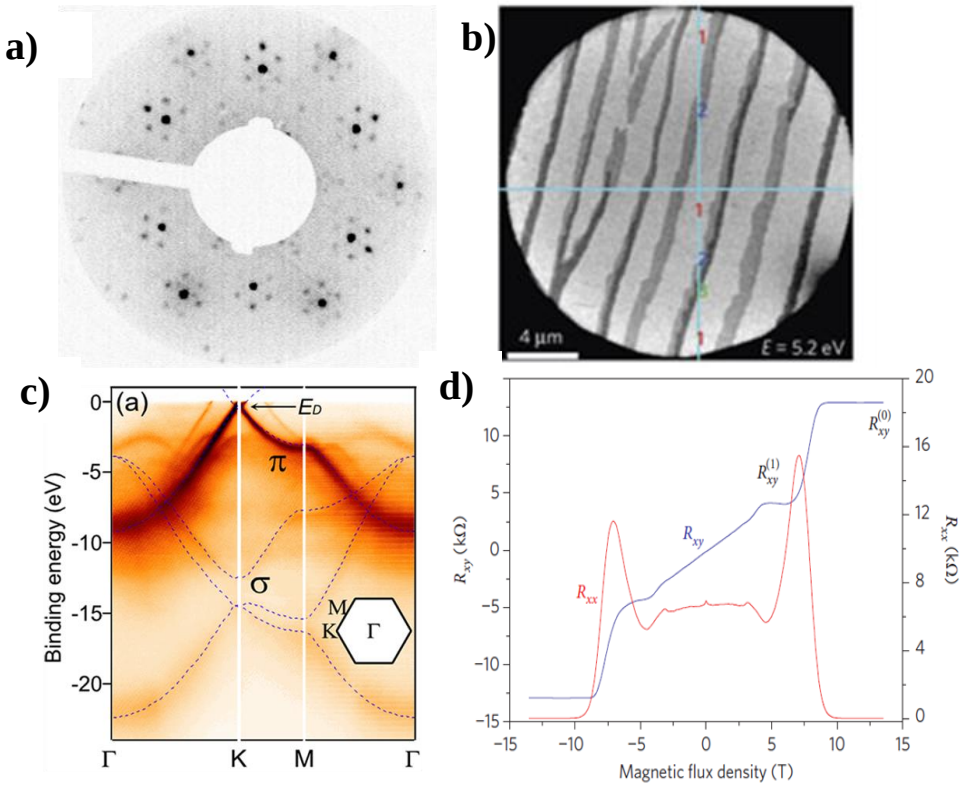

Figure 1.7 Examples of SiC Si-face graphene. a) LEED pattern of 1 ML graphene on 6H-SiC (0001) (Emtsev, et al., 2008). b) LEEM image revealing monolayer coverage on the terraces and bilayer/trilayer growth at the step edge of 6H-SiC (0001) (Emtsev, et al., 2009). c) Photoemission images revealing the band structure of single layer graphene (Ohta, et al., 2007). d) Transverse (R_{xy}) and longitudinal (R_{xx}) resistance of the 11.6 µm × 2 µm device measured at T=4.2 K (Tzalenchuk, et al., 2010).

1.3.4.2 Carbon Face SiC Epitaxial Graphene

On the C-face of SiC, epitaxial graphene can be grown in UHV or high vacuum. Different from the defective C-face graphene grown in UHV (van Bommel et al., 1975) , C-face graphene grown using the confinement controlled sublimation method developed at Georgia Tech (de Heer, et al., 2011) shows rotational order, consisting primarily of two principle rotational orientations (Hass, et al., 2008). Samples prepared this way demonstrate a Berry's phase of π with electronic confinement and coherence (Berger, et al., 2006); ultrahigh mobilities exceeding 250,000 cm^2/Vs (observed with infrared

Landau level spectroscopy (Orlita, et al., 2008)); splitting of Landau levels (Song, et al., 2010), and a linear electron band structure in multilayer epitaxial graphene (observed in ARPES (Sprinkle, et al., 2009) and scanning tunneling Landau level spectroscopy (Miller, et al., 2009)). In addition, C-face multilayer epitaxial graphene can be oxidized into epitaxial graphene oxide with Hummers' method (Wu, et al., 2008). A metastable structure has been proposed (Kim, et al., 2012) and a local thermal reduction method has been used to pattern nanostructures on this material for electronic applications (Wei, et al., 2010).

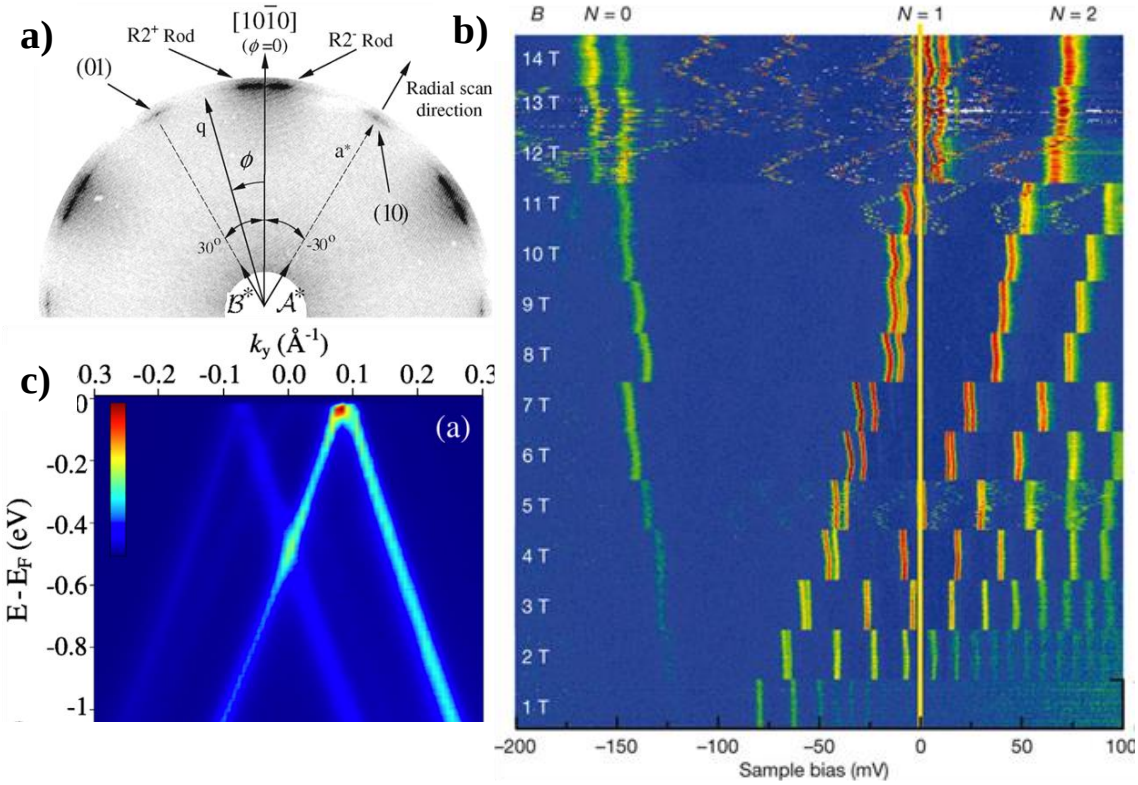

Figure 1.8: Example of C-face multilayer epitaxial graphene. a) LEED image acquired at 67.9 eV from 4H-SiC(000-1) with ~10 graphene layers, showing only graphene spots and diffuse arcs (Hass, et al., 2008). b) Landau levels of multilayer epitaxial graphene on SiC as a function of magnetic field. A splitting of the N=0, 1 and 2 Landau levels can been seen in different field range (Song, et al., 2010). c) ARPES measured band structure of an 11-layer C-face graphene film grown on the 6H-SiC. Three linear Dirac cones are visible (Sprinkle, et al., 2009).

1.4 Graphene Transistor

The two major areas of semiconductor electronics are digital logic devices and analog devices. Digital logic depends almost entirely on the performance of silicon metal–oxide–semiconductor field effect transistor (MOSFET). For decades, making MOSFETs smaller has been key to the progress in digital logic. Considering the on-going progress of reducing the size of Si MOSFET, the chip makers have been less enthusiastic about new materials to replace Si. As gate lengths continue to decrease, however, it is significant to explore new materials and new device concepts in order to maintain the trend of high device performance.

The focus in current CMOS industry is to design a device in which short-channel effects are suppressed and series resistances are minimized. For a logic circuit, excellent switching capability is required, which calls for the on and off current ratio to be between 10^4 ~10^7 (The International Technology Roadmap for Semiconductors (Semiconductor Industry Association, 2009)). The fact that graphene can be one atomic layer thick and maintain high mobility is its most attractive feature, but the zero band gap in graphene also presents a huge obstacle from being used in conventional digital logic.

In analog applications, however, a large on to off ratio is not required. In small-signal amplifiers, the transistor is operated in the on-state and small analog signals to be amplified are superimposed onto the dc gate–source voltage. Shorter gates, faster carriers and lower series resistances all contribute to the maximum oscillation frequency, which is the highest frequency at which an FET is useful in the radiofrequency applications. Drain current saturation, however, is essential to reach the maximum possible operating speed.

Top-gated graphene FETs have been made with exfoliated graphene (Lemme, et al., 2007; Liao, et al., 2009), graphene grown on metals such as nickel (Kedzierski, et al., 2009) and copper (Li, et al., 2009) and epitaxial graphene (Kedzierski, et al., 2008; Li, et al., 2009b). The on–off ratios reported for MOSFET devices with large-area-graphene channels are in the range 2–20. FETs with gigahertz capabilities have been reported.

These transistors possess large-area channels of exfoliated graphene (Lin, et al., 2009; Liao, et al., 2010), epitaxial graphene on the Si-face of SiC (Lin, et al., 2010; Moon, et al., 2009), epitaxial graphene on the C-face of SiC (Guo, et al., 2013) and CVD graphene (Wu, et al., 2011).

The key material properties for graphene MOSFETs are: its band gap, high mobility in short channel, low contact resistance and high saturation velocity.

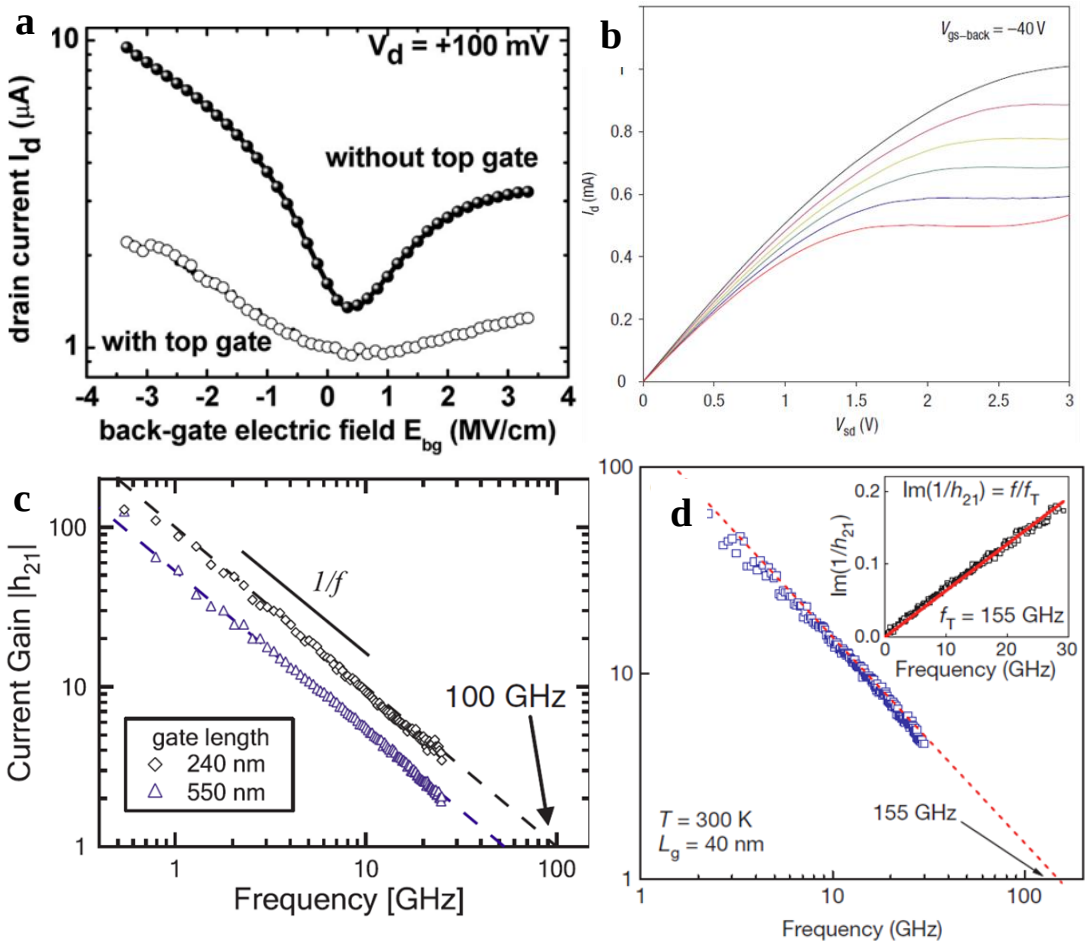

Figure 1.9: Example of graphene transistors characteristics. a) Back-gated graphene-FET characteristics with and without a top gate (Lemme, et al., 2007). b) Drain current (I_d) as a function of source-to-drain voltage (V_{sd}) $V_{gs\text{-}top}$ =-0.3 V, -0.8 V, -1.3 V, -1.8 V, -2.3 V and -2.8 V (from bottom to top). (Meric, et al., 2008). c) Cut-off frequencies, f_T, were 53 and 100 GHz for the 550 nm and 240 nm devices on Si-face epitaxial graphene (Lin, et al., 2010). d) Cut-off frequency for CVD graphene of 40nm gate length at room temperature is 155 GHz (Wu, et al., 2011).

1.5 Graphene Band Gap Opening

As discussed in ξ 1.4, the lack of a band gap in large area graphene is a fundamental problem inhibiting graphene from being used in traditional MOSFET applications. Opening a band gap in graphene would greatly increase the utility of graphene for electronic applications. The methods proposed include: 1) constraining large-area graphene to one dimension to form graphene nanoribbons, 2) biasing bilayer graphene, 3) applying strain to graphene and 4) chemical functionalization.

Theoretical calculations predict 2 out of 3 armchair edge graphene nanoribbons have a band gap inversely proportional to the ribbon width (Nakada, et al., 1996). This method requires very narrow nanoribbons with well-defined edges and width. With current oxygen plasma etching methods to form devices, when the size of ribbons is down to tens of nanometer, the edge disorder becomes dominant and forms mobility gaps instead of energy gaps (Han, et al., 2010). Sidewall graphene nanoribbons grown on a specific SiC facet have provided an alternative route to grow narrow ribbon without post-growth lithography process (Sprinkle, et al., 2010). A recent result shows that the bent region of sidewall graphene has a band gap energy >0.5 eV. It is narrow (~ 1.4 nm) and continuous over macroscopic lengths (Hicks, et al., 2013).

Bilayer graphene has parabolic shape band structure and a band gap can open up when a perpendicular electric field is applied (Castro, et al., 2007; Zhang, et al., 2009). Theoretical investigations have also shown that the size of the band gap depends on the strength of the perpendicular field and can reach values of 200–250 meV for high electric fields (1–3) × 10^7 V/cm.

Strain engineering in graphene band opening is also proposed theoretically. It requires a very specific deformation direction with respect to the substrate and a very high deformation magnitude (Ni, et al., 2008; Pereira, et al., 2009).

Examples of chemical functionalization (Georgakilas, et al., 2012) of graphene include reactions with organic (Sarkar, et al., 2012) and inorganic molecules (Si, et al.,

2008), chemical modification of the graphene surface (Elias, et al., 2008), and covalent (Wang, et al., 2009) and noncovalent interactions with graphene (Wang, et al., 2009b).

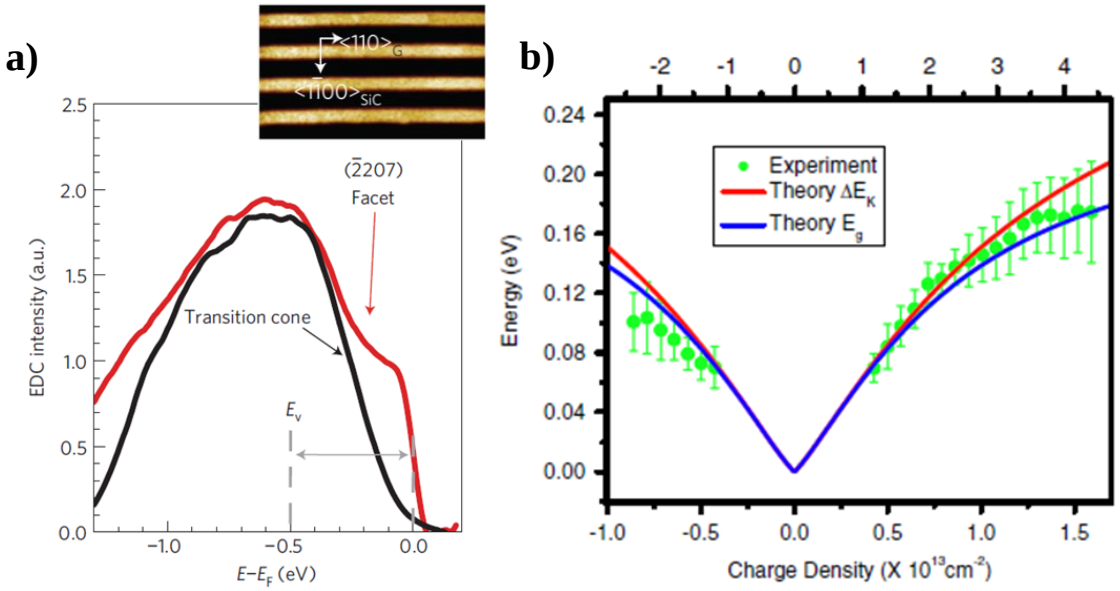

Figure 1.10 a) Comparison of the energy distribution curve (EDC) for the sidewall graphene and the graphene bent region (transition region). The graphene valance band is shifted 0.5 eV below E_F. This gives a minimum bang gap 0.5 eV (Hicks, et al., 2013). b) Dependence of the energy gap at the K point ΔE_K on the gate voltage and the charge doping density of the graphene bilayer (Mak, et al., 2009).

1.6 Thesis Outline

Epitaxial graphene grown on the C-face of SiC with the confinement controlled sublimation method will be first introduced in Chapter 2. The growth method, topography and Raman identification of single layer epitaxial graphene on the C-face of SiC will be discussed in detail in Chapter 2. Transport measurements on such material at cryogenic temperatures in the presence of magnetic field will be described in Chapter 3. In Chapter 4, I will analyze the characteristics of single layer epitaxial graphene FETs on the C-face of SiC at liquid helium temperatures with and without a magnetic field. Characterization of boron nitride grown on epitaxial graphene as a gate dielectric will also be covered in Chapter 4. In the last chapter (Chapter 5), I will present the preparation and characterization of a thin silicon oxide layer on the C-face of semi-insulating 6H-SiC. A Schottky barrier transistor based on the two-dimensional electron gas in the SiC /silicon oxide interface with multilayer graphene as contacts will be demonstrated and analyzed.

CHAPTER 2

SINGLE LAYER EPITAXIAL GRAPHENE GROWN ON THE C-FACE OF SILICON CARBIDE

2.1 Introduction

Multilayer epitaxial graphene on the C-face of SiC was grown with the confinement controlled sublimation (CCS) method (de Heer, et al., 2011) and has been confirmed to maintain the linear electronic band structure through the rotationally ordered stacking by LEED (Hass, et al., 2008), ARPES (Sprinkle, et al., 2009), STM (Miller, et al., 2009) and infrared spectroscopy (Orlita, et al., 2008). The transport measurement of multilayer epitaxial graphene in the magnetic fields also confirms the existence of Berry's phase of π (Berger, et al., 2006).

The unconventional integer quantum Hall effect, which is characteristic of two-dimensional graphene, however, was not observed on the multilayer epitaxial graphene. Theoretical calculations (Darancet, et al., 2008) show that the conducting states in a doped layer can couple to the zeroth Landau levels in the undoped layer, which is on top of the doped one. As a consequence, the conducting electrons of the doped layer are subjected to a scattering mechanism that increases with a magnetic field because the number of states in the zeroth Landau level increases with the magnetic field. This forbids the observation of strong Shubnikov–de Haas oscillations. In addition, the ultrafast midinfrared pump-probe spectroscopy experiments (Sun, et al., 2010) confirm that the vertical screening length in graphene is about one layer in graphene thickness.

This means that the external electrical field induced by a gate voltage can only affect the one or two graphene layers adjacent to the gate. One of the most important applications for graphene in electronics is the field effect transistor. The fact that the multilayer graphene conductivity will not vary significantly (Kedzierski, et al., 2008) affects its application potential as an electronic device. With all of these concerns, it is important to pursue a single layer graphene on the C-face of SiC. Although single layer graphene on the Si-face of SiC has been reported and characterized (Berger, et al., 2004; de Heer, et al., 2007; Emtsev, et al., 2009), large area (in the scale of tens of micrometers) single layer epitaxial graphene on the C-face of SiC and its electronic and transport properties were largely unknown.

In this chapter, I will introduce the substrate material (SiC) and the CCS method for epitaxial graphene growth. Then I will discuss the growth, topography and Raman characteristics of single layer epitaxial graphene on the C-face of SiC. Note that other research groups have also tried to understand the growth and properties of single layer epitaxial graphene on the C-face of SiC. Some of the work is reviewed in Hiebel, et al., 2009; Camara, et al., 2009; Tedesco, et al., 2010; Camara, et al., 2010; Zhang, et al., 2012.

2.1.1 Instrumentations

Scanning probe microscopy makes use of several distinct interaction forces between probe and material surface to reveal the material topography and properties. Atomic force microscopy (AFM), electrostatic force microscopy (EFM), current-atomic force microscopy (I-AFM) was used in this work. The experiment instrument is Park System XE70. The tip used in NC-AFM scan is type PPP-NCHR. The tip used in EFM

scan is type PPP-EFM. The tip used in I-AFM scan is type PPP-CONTSCPt. All tips are purchased from NANOSENSORS^{TM}.

Raman spectroscopy is a technique using the inelastic photon-phonon interaction to detect the vibration modes of lattice. The Raman experiments in this work were done with a LabRAM HR 800 from HORIBA Jobin Yvon. It is equipped with λ=532 nm laser with power 20 mW. Spectra in this work were collected at 5 mW with D06 filter if not specified. The optical microscope has X10, X50 and X100 magnification. Both front light (reflective light) and back light (transmitted light) sources are available.

Ellipsometry is an accurate thin film measurement technique. Multilayer graphene was measured with an ellipsometer, and its thicknesses were determined by a model built to fit graphene on SiC (Sprinkle, 2010b). The experimental instrument used in this work is an Auto SE Spectroscopic Ellipsometer from HORIBA Jobin Yvon. The spectral range is 440~1000 nm. The spot size used is 250 μm × 250 μm.

2.2 Confinement Controlled Sublimation Method

2.2.1 Silicon Carbide

2.2.1.1 Silicon Carbide Polycrystalline Type

Silicon carbide exists in various crystalline forms in nature. Based on the layer stacking, the most common SiC polytypes are α type SiC, hexagonal stacking, such as 2H-SiC, 4H-SiC and 6H-SiC, and β type SiC, zincblende stacking, such as 3C-SiC. Hexagonal SiC is widely produced because it is most suitable for epitaxial growth. 2, 4, and 6 denote the number of silicon-carbon bi-layer in each unit cell. Carbon and silicon atoms form the hexagonal structure within each plane respectively while the silicon carbon bi-layers are stacked vertically above each other by 0.25 nm. If we use the same letter to represent the repeat silicon carbon bi-layer, 2H-SiC stacking can be written as ABABABA…, 4H-SiC stacking can be written as ABCBABCB…, and 6H-SiC SiC

stacking can be written as ABCACBABCACB... Therefore, the 4H-SiC unit cell has a height of 1 nm and the 6H-SiC unit cell has a height of 1.5 nm. Figure 2.1 gives an example of the lattice structure of 4H-SiC. Depending on the terminated atom type, the SiC polar face is called as SiC (000-1) (C-face) (carbon atom terminated) and SiC (0001) (Si-face) (silicon atom terminated), respectively.

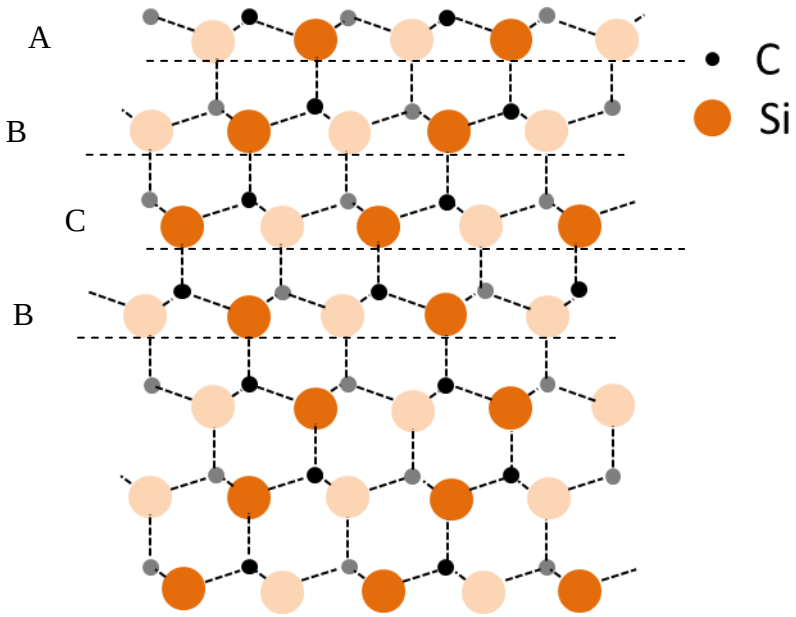

Figure 2.1: Crystal lattice structure of 4H-SiC (000-1). 4H-SiC unit cell is composed of 4 silicon-carbon bi-layers. The stacking sequence is denoted as ABCBABCB… The height of unit cell is 1.0 nm. Depending on whether it is terminated by carbon atom or silicon atoms, the SiC polar face is called as SiC (000-1) (C-face) or SiC (0001) (Si-face).

2.2.1.2 Silicon Carbide Surface

A research grade single crystal semi-insulating SiC wafer from Cree, Inc. was used in this work. The SiC wafer was cut on-axis with an orientation miscut angle less than 0.10°. The polar face for graphitization is epitaxy ready and chemical mechanical polished (CMP).

The as-received SiC sample was cleaned with an ultrasonicator in acetone for 30 minutes and in isopropyl alcohol (IPA) for another 30 minutes to remove the surface dirt

and possible grease. Hydrogen etching (Ramachandran, et al., 1998) was used to obtain an atomic flat surface on SiC when no CMP surface was available. For CMP sample, its surface was flat and free of deep mechanical scratches. In this research, hydrogen etching was not applied for the CMP samples. Instead, an annealing step with an extra 20 minutes at 1200 °C during the graphitization process was adopted to remove the native oxide on the SiC samples. Figure 2.2 shows AFM images for a non-CMP surface before and after hydrogen etching and a CMP surface after cleaning.

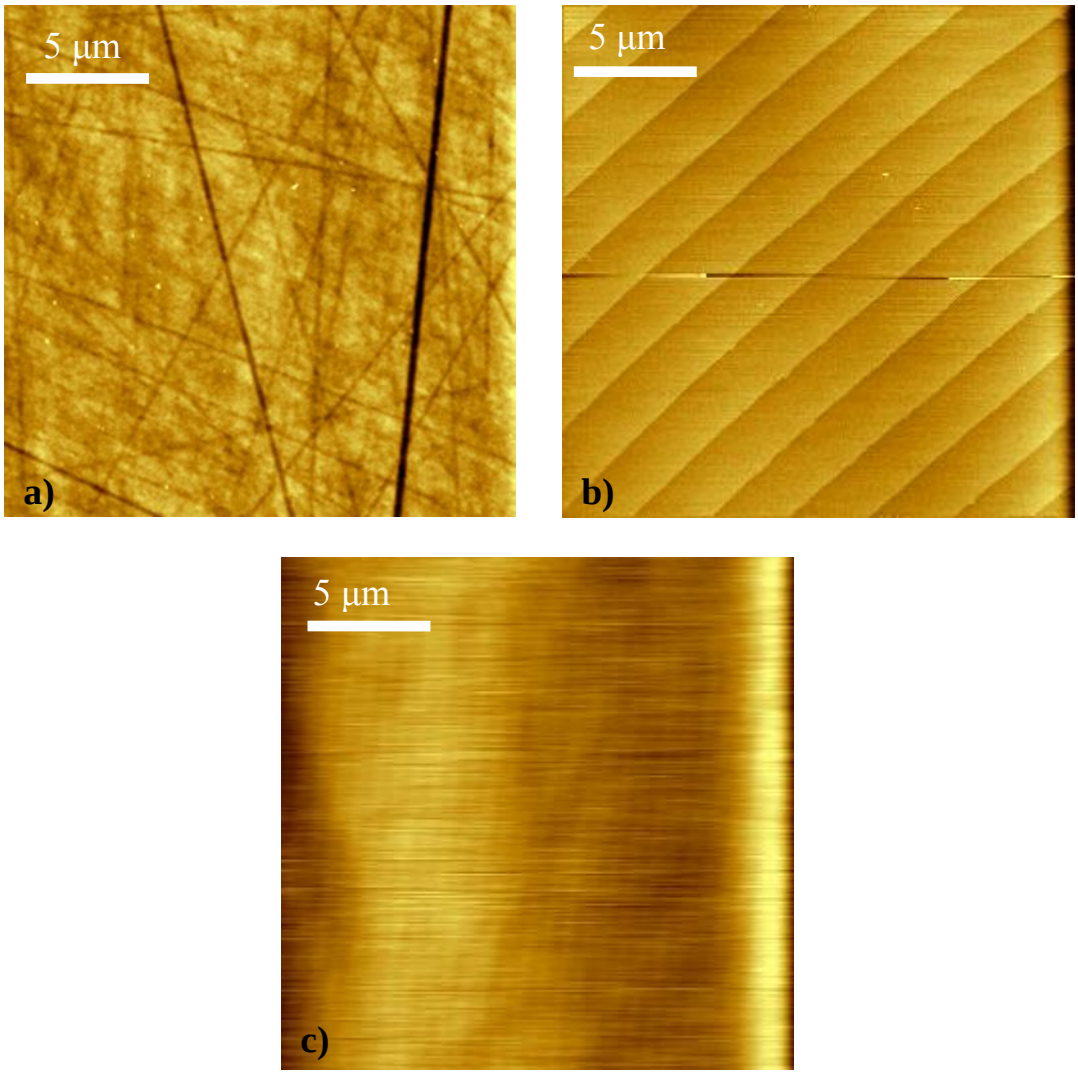

Figure 2.2: AFM morphology of SiC (000-1). a) non-CMP SiC surface, full of 10 nm deep scratches. b) Non-CMP SiC surface after hydrogen etching, atomic flat surface with natural SiC steps, c) CMP SiC surface after solvent cleaning. The surface is flat with no scratches visible. Scale bar: 5 µm.

2.2.2 Multilayer Epitaxial Graphene

2.2.2.1 High Vacuum Induction Furnace

The confinement controlled sublimation (CCS) method (de Heer, et al., 2011) was used to grow graphene. In this method, the SiC sample is heated at the target temperature for a specific period of time inside a home-made high vacuum induction furnace. A graphite tube with a small aperture works as the heating crucible for SiC. Figure 2.3 a) and b) is the design and picture for such a furnace. The graphene growth rate is proportional to the silicon depletion rate. Each evaporated silicon atom will leave one carbon atom behind. Based on the carbon atom density of SiC crystal and graphene, carbon from about 3 SiC bi-layers (Si-C) will form one layer of graphene. According to the study of vapor pressure during silicon carbide thermal sublimation (Lilov, 1993), the Si vapor pressure over SiC around the graphitization temperature is determined as $P_{si}(1500\ K)=1.6\times10^{-6}$ torr, $P_{si}(2000\ K)=1.1\times10^{-2}$ torr, while carbon vapor pressure at this temperature range is in the order of 10^{-10} torr. Since the base vacuum for such furnace is $1x10^{-6}$torr, only the silicon vapor pressure needs to be considered. After several thermal cycles, the graphite enclosure will be passivated by silicon atoms. As less and less evaporated silicon can be absorbed to the graphite enclosure, the silicon partial pressure increases, which will slow or even stop further silicon sublimation from SiC and hence stop graphene growth. In order to avoid such situation, a small aperture is designed on the graphite inset so that limited amount of silicon atoms can escape. Such a thermal dynamic equilibrium insures that silicon evaporates at a slower rate and graphene grows in a more controllable way. The graphene growth rate is controlled by silicon pressure in the chamber and can be adjusted by designing the graphite enclosure leak geometry. Graphene grown with this method produces large SiC step terraces and very smooth surface morphologies.

A typical heating sequence for the SiC graphitization process is shown in Figure 2.3 c). It consists of 20 minutes at 200 °C for the system out gassing, 20 minutes at 1200 °C to remove the SiC native oxide and prepare regular SiC step flow, and 10~30 minutes at around 1500 °C for graphitization. The temperature and time at the graphitization stage determines the graphene thickness.

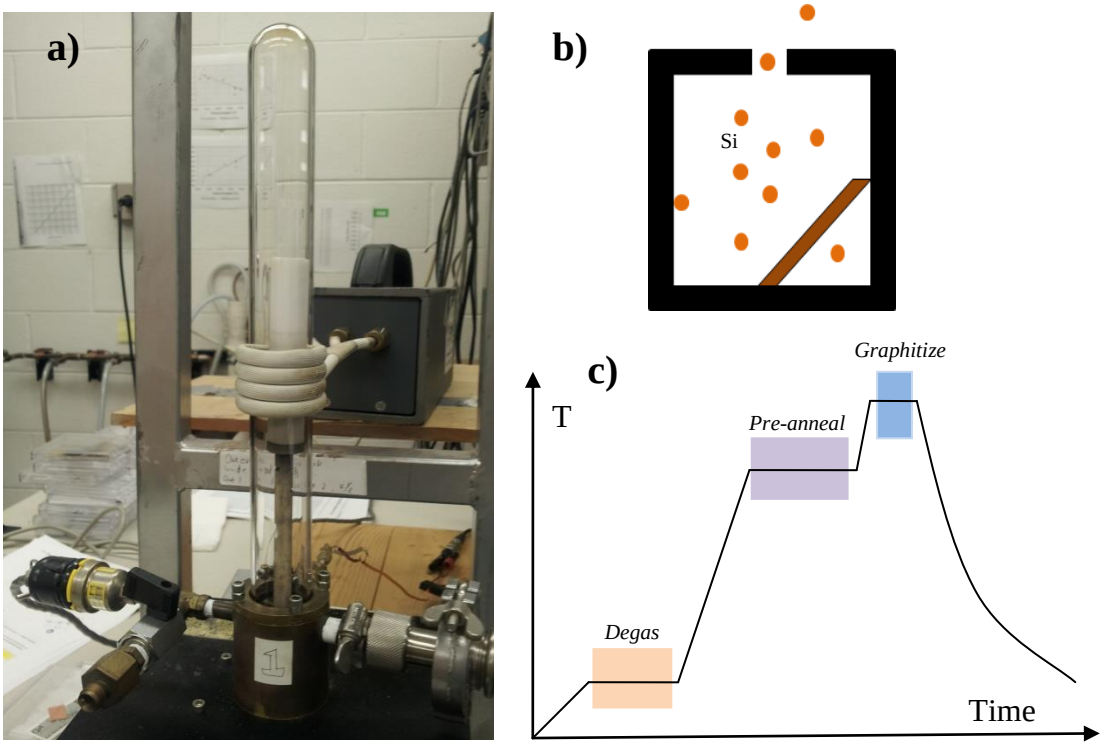

Figure 2.3: High vacuum furnace and graphitization heating sequence. a) Picture of a high vacuum furnace with heating unit. b) Illustration of the thermal sublimation of silicon atoms from SiC inside a graphite tube through a small aperture. c) Heating sequence for a typical graphitization process.

2.2.2.2 Silicon-Face SiC Graphitization Stage

Graphene grown on different SiC polar faces is significantly different in both topography and electrical properties. Figure 2.4 demonstrates the various stages of graphitization process on the Si-face of 6H-SiC. The hydrogen-etched surface (Figure 2.4a) exhibits 0.8 nm silicon carbide steps, half of the 6H-SiC unit cell height (1.5 nm). The sample was heated to several temperatures (Figure 2.4b-d) subsequently. The step

edge becomes rounded at 1450 °C and gets even rougher at 1500 °C. The step roughening is associated with the formation of buffer layer (a carbon rich layer strongly bonded to SiC substrate) as confirmed in low energy electron diffraction (LEED). The buffer layer was formed at 1080 °C in a UHV system (Riedl, et al., 2009). At 1580 °C, the first layer of graphene on silicon face starts to form. With the confinement controlled sublimation method, the graphene growth temperature is raised by about 400 K. The high temperature growth environment enables high atom mobility and hence improves the graphene quality.

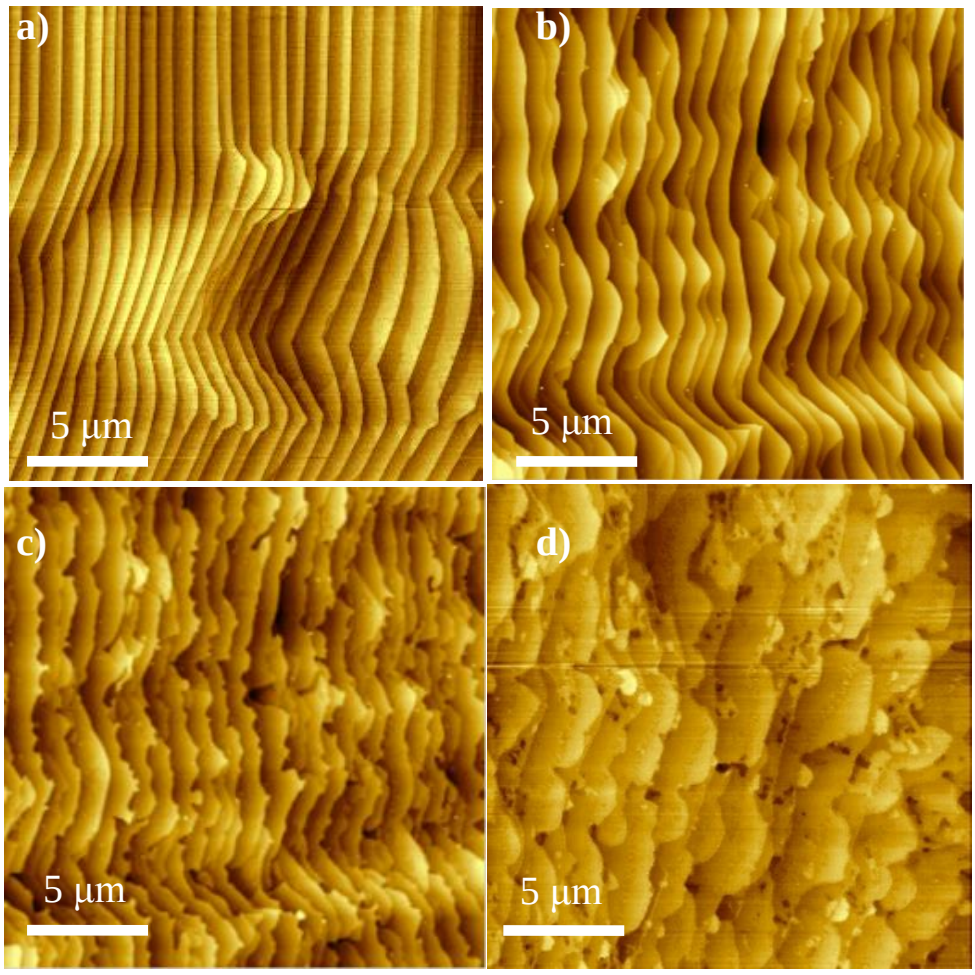

Figure 2.4: AFM images of the Si-face of 6H-SiC surface evolution upon annealing. a) Initial surface after hydrogen etching, showing half-unit cell height steps (0.8 nm). b) After CCS annealing at 1450 °C, substrate steps become rounded. c) After annealing at 1500 °C, the steps roughen. d) At 1580 °C, one layer of graphene is formed. Scale bar 5 µm.

2.2.2.3 Carbon-Face Multilayer Epitaxial Graphene

Different from the Si-face, graphene on the C-face starts to grow at a lower temperature (as low as 1490 °C) and forms up to 100 layers through changing the annealing temperature and time. Figure 2.5 shows two typical AFM images for a ten-layer graphene sample. Graphene grows across SiC step edges, covering the entire surface. The pleats (white lines seen on the figure) are formed due to the lattice mismatch between graphene and SiC during the cooling process, as revealed in STM (Biedermann, et al., 2009) and AFM (Prakash, et al., 2010). This can be used to identify the formation of graphene on the C-face.

Graphene has two prominent Raman features: the G peak (~1580 cm^{-1}) and the 2D peak (2700 cm^{-1}) (Ferrari, et al., 2006). The G peak is due to the doubly degenerate zone center E_{2g} mode (Tuinstra, et al., 1970). The 2D peak is due to a double resonance process, which links the phonon wave vectors to the electronic band structure (Thomsenand et al., 2000). The shape of the 2D peak can be used to distinguish a single layer graphene from few-layer graphite. For bi-layer graphene, the band splitting will cause 4 components in the 2D peak and gives a completely different 2D peak shape (Ferrari, et al., 2006).

The stacking of multilayer epitaxial graphene (MEG) on the C-face was shown to be rotationally ordered (Hass, et al., 2008). The way multilayer epitaxial graphene layers stack leads to very weak effective electronic coupling between the layers. Hence the graphene linear band structure is also maintained in MEG, which corresponds to a single Lorenzian shape 2D peak in Raman spectroscopy (Faugeras, et al. 2008). Figure 2.6 is the Raman spectrum collected on a 5-layer C-face MEG. In this example, the Raman spectrum is a combination of signal from graphene related G and 2D peak and signal from the SiC substrate, which are seen in the range of 1200 cm^{-1} to 2000 cm^{-1}. MEG on the C-face has a single Lorenzian shape of Raman 2D peak. The Raman 2D peak is located at frequency shift of 2694 cm^{-1} with a full width at half maximum (FWHM) of 34

cm^{-1}. The defects related D peak (around 1350 cm^{-1}) is not observed in the MEG Raman spectrum. It suggests that multilayer epitaxial graphene on the C-face is a perfect crystal without defects (or undetectable defects in Raman).

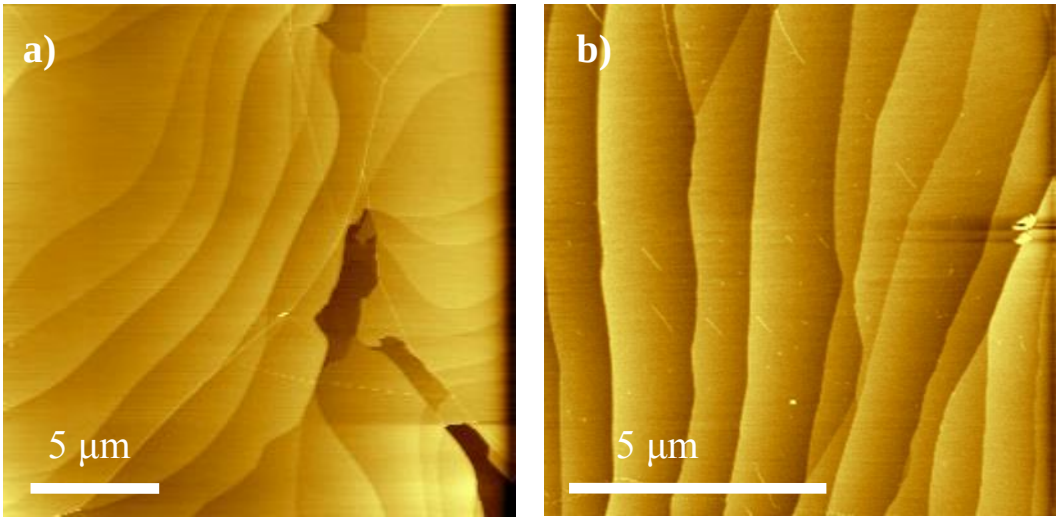

Figure 2.5: AFM image of a ten-layer graphene on C face 4H-SiC. SiC steps are clearly visible. The existence of graphene is confirmed by the formation of pleats (white lines in the image). Scale bar 5 µm.

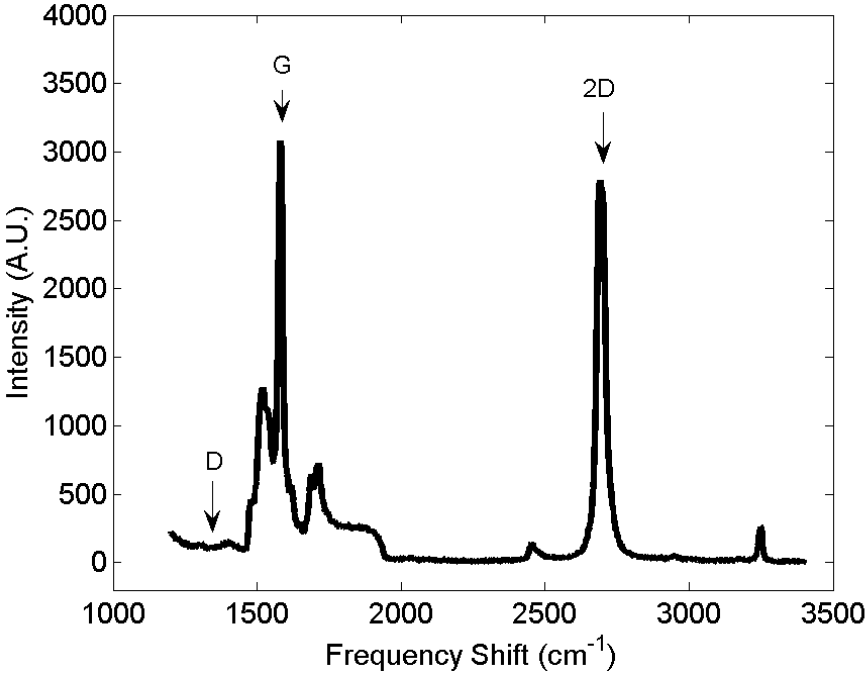

Figure 2.6: Raman spectra for a 5-layer C-face epitaxial graphene. The Raman spectrum of multilayer graphene on the C-face (black) also has a single Lorenzian 2D peak (f=2694 cm^{-1}, FWHM=34 cm^{-1}). No D peak (around 1350 cm^{-1}) is visible.

2.3 Single Layer Epitaxial Graphene on the C-face of SiC

2.3.1 Growth

Summarizing the epitaxial graphene thickness is determined by the amount of silicon depletion from the SiC surface. The graphitization temperature determines the ratio of how much silicon escapes from the SiC surface. The graphitization time determines how long the silicon atoms can continue to sublimate. In order to reduce the amount of escaped silicon and therefore the graphene thickness, a lower graphitization temperature and a shorter graphitization time is desired. The initial growth stage of C-face graphene is achieved by lowering the typical MEG growth temperature and reducing the graphitization time. Graphene grown in this way is normally sub-monolayer due to the non-uniform distribution of nucleation sites. By testing different temperatures and time combinations, large (>30 μm) regions of single layer graphene islands can be achieved. The typical sub-monolayer graphene growth temperature and time in this work is 1490 ℃ and 10 minutes.

2.3.2 Topography

C-face graphene grows from screw dislocations (mostly thread screw dislocations), as also observed by others (Hite, et al., 2011; Camara, et al., 2011). Fifty graphene islands grown on more than fifteen SiC sample pieces were selected for examination with optical microscope and AFM. The nucleation sites could be identified as screw dislocations, particles, and etched structures on the C-face of SiC. Graphene initiating around screw dislocation is found to grow faster than the surrounding area. Denser pleats are visible in the AFM image on top of the screw dislocation area, as demonstrated in Figure 2.7**.** The fast-growing nature of graphene associated with screw dislocations makes it difficult to control a uniform the growth rate.

There are other type of graphene islands associated with the unintentionally introduced particles or SiC surface morphology change. Raman spectrum and transport measurements of Hall bar structures made on those islands verify that those graphene islands are true single layer graphene (will be shown in Chapter 3). AFM images of those single layer islands reveal an average graphene size around 5 μm by 25 μm. Figure 2.8 gives an example of one such single layer graphene island. As seen in the AFM topography image, those graphene regions always correspond to the SiC step bunching regions, while the non-graphitized SiC areas keep the natural SiC step terraces. Those steps converge underneath the graphene. Most graphene islands are elongated along the SiC step terraces. The pleat heights are normally 1~2 nm or less.

Graphitization on intentionally induced SiC surface structures change was also investigated. Figure 2.9 a) is an AFM image of a graphitized hexagonal pit that was etched before on the C-face. Figure 2.9 b) and c) are the corresponding EFM amplitude and Raman 2D peak intensity map on the same area, respectively. It appears that graphene growth initiates at specific corners of the hexagonal pit. Further work will be needed to reveal whether this can lead to a process to direct the graphene growth.

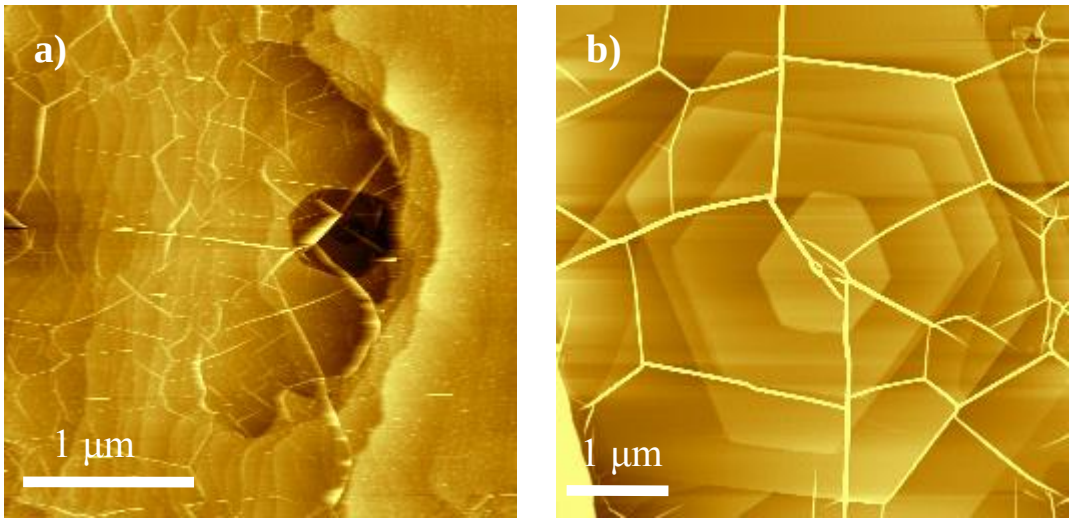

Figure 2.7: a) Graphene initiated from a screw dislocation. The deep, hollow cavity in the SiC corresponds to the screw dislocation region. Dense pleats reveal that graphene in this region is quite thick. b) Scan on one screw dislocation on SiC. Scale bar: 1 μm.

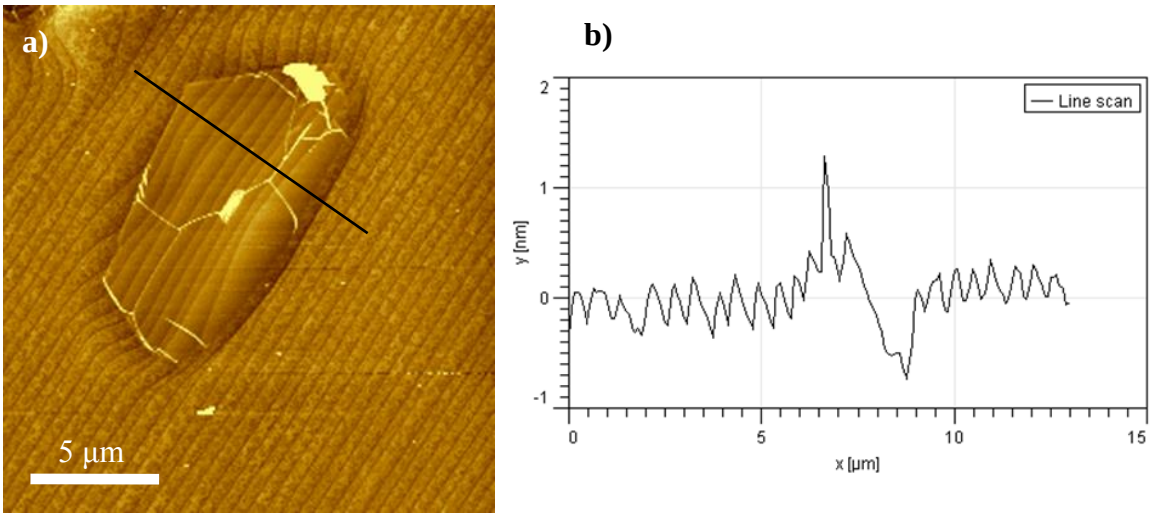

Figure 2.8: a) AFM image of a single layer graphene island on 4H-SiC (000-1). The Graphene region is on top of the SiC step bunching region. The SiC steps converge underneath the graphene and the steep step defines the edge of the graphene. b) A line profile across the graphene flake. The SiC steps keep their 0.5 nm half unit cell step height. The initial growth edge has a 1nm step height. Scale bar: 5 µm.

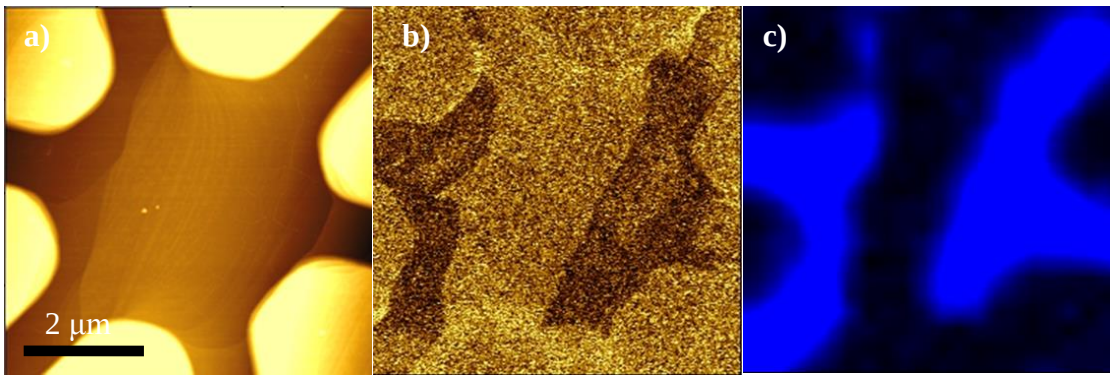

Figure 2.9: Single layer graphene growth on C-face 4H-SiC on a pre-patterned structure indicates preferred sites for graphene growth. a) AFM image for a hexagonal pit after graphitization. The structure was etched to a depth of ~50 nm. The SiC steps flow inside the pit. Faint graphene pleats are visible. b) EFM amplitude scan shows a contrast between the darker graphene regions and the lighter SiC regions as verified by a Raman 2D band intensity map in c). Scale bar: 2 µm.

2.3.3 Raman Indicator

2.3.3.1 Single Layer Graphene Determination

The single Lorenzian shape of Raman spectrum 2D peak (~2700 cm^{-1}) has been used to identify graphene (Ferrari, et al., 2006). This method, however, does not apply to epitaxial graphene since multilayer epitaxial graphene also shows a single Lorenzian shape of 2D peak. The epitaxial graphene Raman signal is the combination of the graphene Raman spectrum and the SiC Raman spectrum. After graphene grows on SiC, the SiC Raman peak intensity will be attenuated. The absolute Raman peak intensity is susceptible to experiment conditions (laser power, lens focus, etc.) and cannot be used to directly compare samples. Instead, the peak intensity ratio is a more robust parameter and can be used to derive information about graphene. Shivaraman and collaborators (Shivaraman, et al., 2009) have demonstrated the correlation between the logarithm (ln(S)) of the remaining fraction of the Raman signal after subtracting the SiC background and the graphene thickness, however, this method has a significant error for graphene films up to 5 layers thick and it does not provide a value for single layer epitaxial graphene. A more accurate way to directly determine single layer epitaxial graphene on the C-face is necessary and discussed below.

The bare SiC Raman spectrum features several peaks in the frequency shift range between 1000 cm^{-1} and 2000 cm^{-1}, as shown in Figure 2.10 a). The peak near 1520 cm^{-1} is the overtone of the SiC TO(X) at 761 cm^{-1}. The peak near 1713 cm^{-1} is a combination of SiC optical phonons with wave vectors near the M point at the zone edge. S_1 is the spectrum area intensity from wave number 1460 cm^{-1} to 1660 cm^{-1} and S_2 is the spectrum area intensity from wave number 1660 cm^{-1} to 1960 cm^{-1}. After the epitaxial graphene growth, the graphene G peak (around 1580 cm^{-1}) is overlaid with the SiC S_1 peak area. As demonstrated in Figure 2.10 b), the intensities of the SiC and graphene G peaks add up to S_1'=S_1+G, while the SiC S_2 peak area has no additional contribution from graphene.

The intensity of SiC S_2 peak is attenuated by the graphene overlayer. For the same type of SiC crystal, the intensity ratio $\frac{S_1}{S_2}$ remains the same. Hence

$$\frac{S_1'}{S_2'} = \frac{S_1 + G}{S_2} = \frac{S_1}{S_2} + \frac{G}{S_2} \qquad (2\text{-}1)$$

$$\frac{G}{S_2} = \frac{S_1'}{S_2'} - \frac{S_1}{S_2} \qquad (2\text{-}2)$$

By measuring S_1, S_2 for the bare SiC and S_1', S_2' for the epitaxial graphene sample, the value of $\frac{G}{S_2}$ can be determined. Five different bare SiC samples from 3 different SiC wafers (of the same polytype) are used to calculate $\frac{S_1}{S_2}$,which gives $\frac{S_1}{S_2} = 1.256 \pm 0.005$. More than 20 single layer graphene samples were evaluated with above method. The relative intensity ratio is given as $\frac{G}{S_2} = 0.061 \pm 0.017$. As a comparison, 18 graphene samples with thickness 2~3 layers were also investigated, $\frac{G}{S_2} = 0.139 \pm 0.020$ in this case. The nature of single layer graphene and multilayer graphene for all samples are confirmed by further electrical measurements (Chapter 3). This method avoids the background subtraction which can lead to additional noise level. Therefore, by calculating the relative intensity ratio of $\frac{G}{S_2}$ for any C-face epitaxial graphene Raman spectrum, if it falls to the range of 0.044~0.078, the epitaxial graphene sample is a single layer.

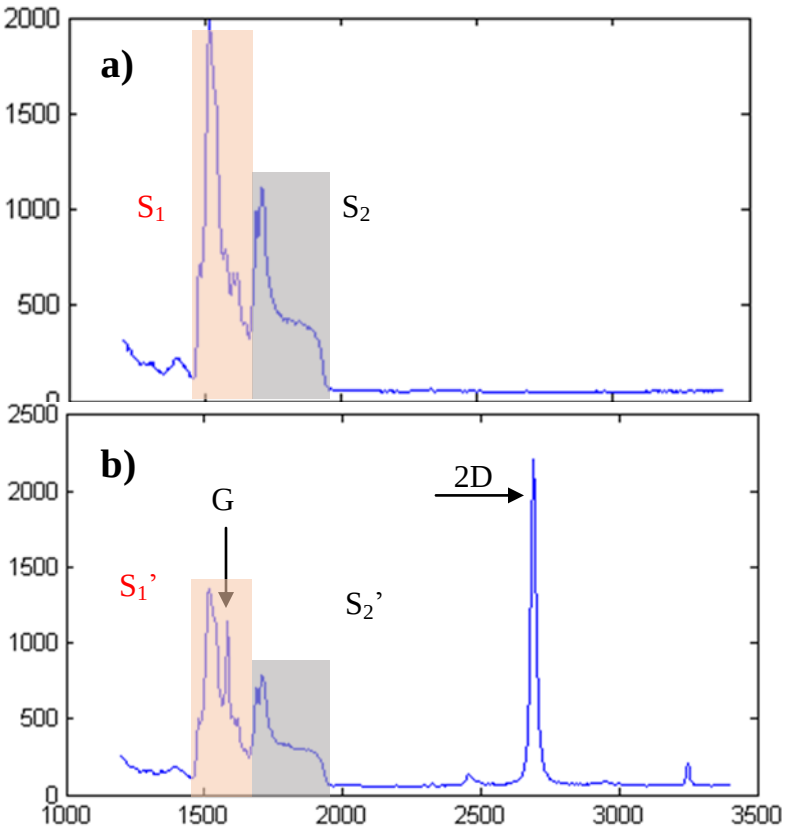

Figure 2.10: Raman spectrum to explain how the Raman attenuation method is used to distinguish single layer epitaxial graphene from multilayer epitaxial graphene. a) A typical bare SiC Raman spectrum. Define S_1 as the total intensity from frequency 1460 cm^{-1}~1660 cm^{-1}, and S_2 as the total intensity from 1660 cm^{-1}~1960 cm^{-1}. b) Raman spectrum for epitaxial graphene on the C face. S_1' is the combined signal of the SiC S_1 peak area and the graphene G peak, S_2'is the attenuated intensity from SiC S_2 peak area.

2.3.3.2 Single Layer Epitaxial Graphene Raman Properties

The single layer epitaxial graphene Raman spectrum is further analyzed in this section. For one single layer epitaxial graphene on the C-face, the following Raman features are observed: 1) The single layer graphene 2D peak is mostly centered at 2685 cm^{-1}, 2) The G peak position is strongly affected by the doping density and can change from 1585 cm^{-1} to 1595 cm^{-1}; 3) The integrated intensity ratio $\frac{I(2D)}{I(G)}$ can vary

from 2 to 9 from sample to sample depending on the carrier density; 4) Some single layer graphene samples have a 2D peak position around 2760 cm^{-1} and a G peak position around 1620 cm^{-1}. Figure 2.11 shows examples of two such Raman spectra with the SiC background signal subtracted.

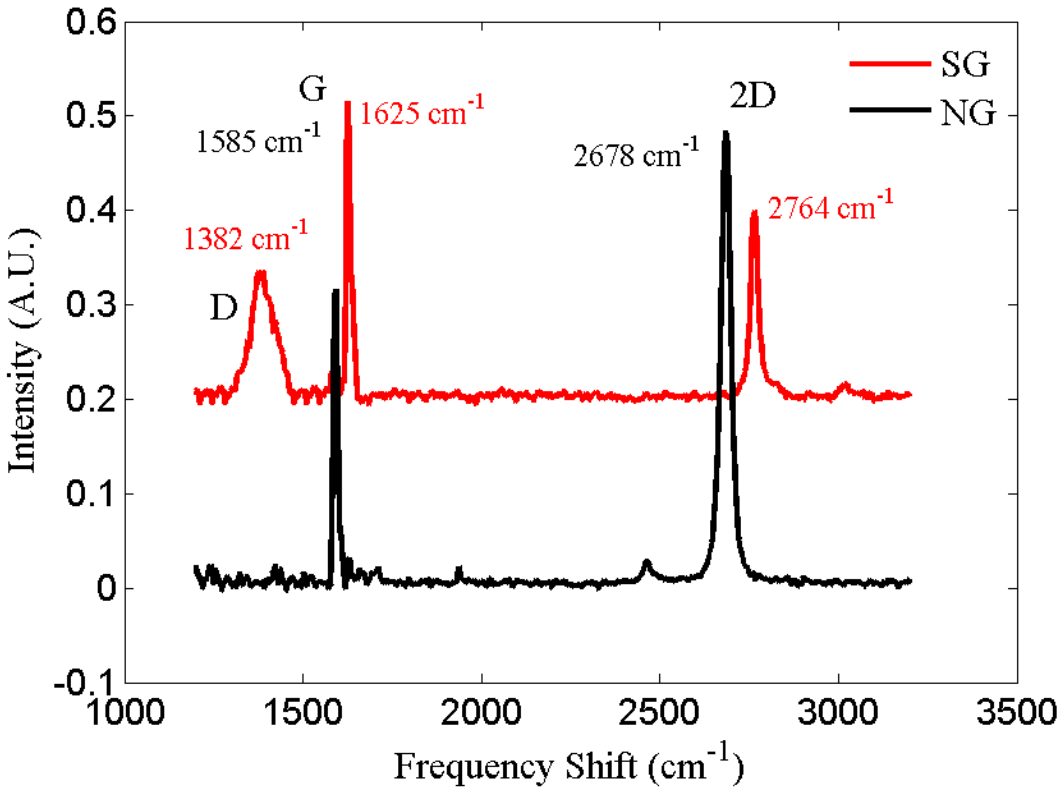

Figure 2.11: Raman spectra for two types of single layer epitaxial graphene on 4H-SiC (000-1). Normal graphene (NG) is the most typical spectrum found on single layer epitaxial graphene (black, lower spectrum). Its G, 2D peak position (1585 cm^{-1}, 2678 cm^{-1}) is close to neutral, non-stressed graphene and lacks a D peak. Strained graphene (SG) could be found occasionally with significant blue shift on the G peak (1625 cm^{-1}) and 2D peak (2764 cm^{-1}) position (red, upper spectrum). This type of spectrum is always accompanied by a visible D peak (1382 cm^{-1}). Laser λ=532 cm^{-1}.

For graphene islands that show strong blue shifts in the G peak and 2D peak position by 30 cm^{-1} and 70 cm^{-1} respectively, their morphology has something in common. Most of those islands are small in dimension (1~2 μm wide and 3~5 μm long), which means that the area where graphene terminates into SiC takes up large portion of

the entire graphene surface area. For large graphene islands, occasionally such a blue shift spectrum can be observed in the region devoid of pleats. Figure 2.12 is an example of one single layer graphene showing both types of Raman spectra as stated above. Figure 2.12 c) and d) is the intensity map for the regions with 2D peak centered at 2680 cm^{-1} and 2760 cm^{-1} respectively. Comparing the AFM topography and Raman peak position intensity map, there is a strong correlation between the area devoid of pleats and the 2D peak blue shift area. The Raman spectrum of those pleat-free areas exhibits a strong D peak, which is absent in a typical single layer epitaxial graphene. Such a blue shift in the Raman spectrum could be attributed to compressive strain caused by the lattice mismatch between graphene and SiC substrate. Graphene pleats on the C-face have been known to release the lattice stress between graphene and SiC (Ni, et al., 2008b). Calculations and experiments also confirm that compressive strain could introduce a blue shift in the 2D peak position up to 80 cm^{-1} (Mohiuddin, et al., 2009; Robinson, et al., 2009). External doping can introduce the 2D peak position shift, however, even the highest doping density possible (4×10^{13} cm^{-2}) will not move the 2D peak center by more than 30 cm^{-1} (Das, et al., 2008). Therefore, doping is not likely the reason for the peak position shift in this case. The presence of D peak in the blue shifted spectrum, which is normally a sign for defective graphene (sp^3- type defects or vacancy type defects) (Eckmann et al., 2012), also indicates the existence of a much stronger graphene/substrate interaction.

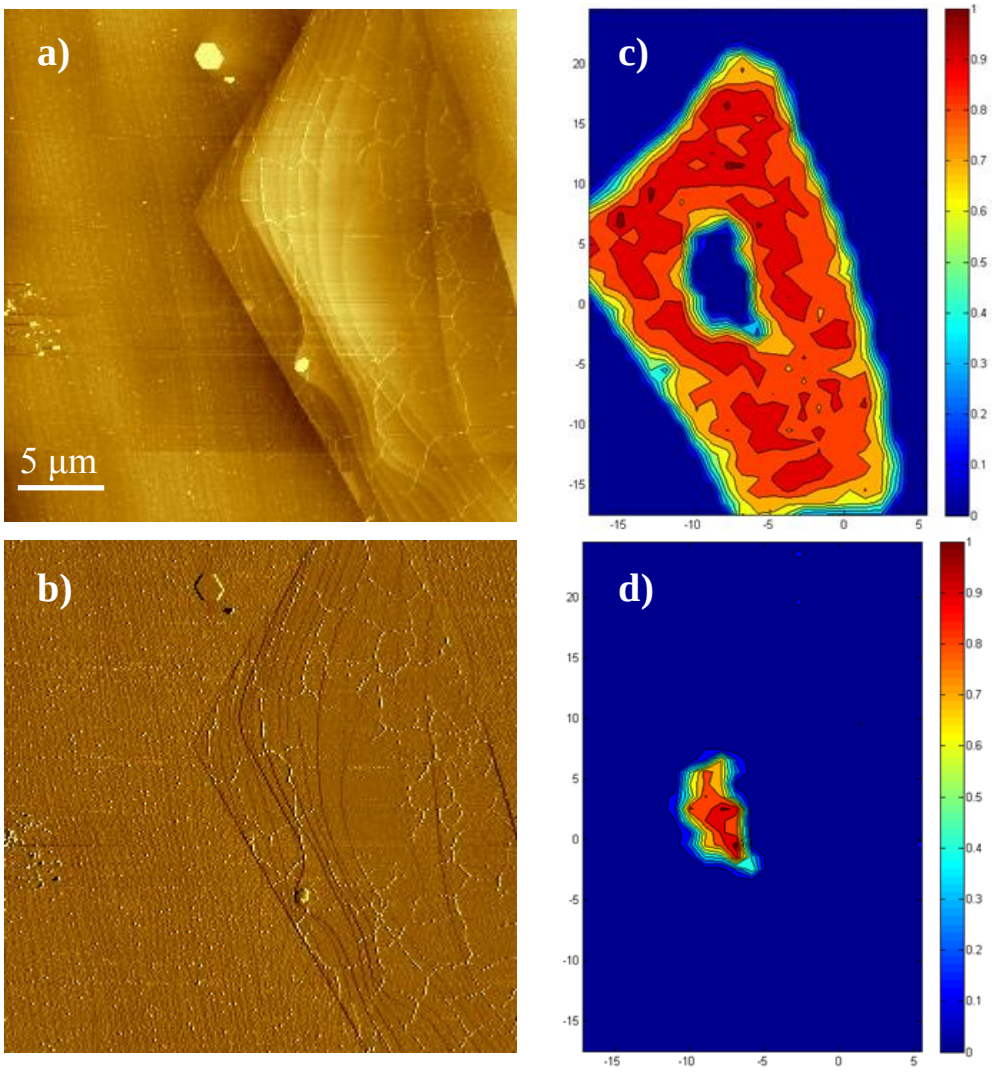

Figure 2.12: a) AFM topography image for a large single layer graphene sheet, draped over several SiC step terraces. b) Corresponding AFM error signal image for (a). The contrast on the error map reveals that the center of the flake is free of pleats. c) and d) are intensity maps for specific Raman peaks. c) Intensity map for 2D peak centered 2680 cm^{-1} and d) is the intensity map for 2D peak centered at 2760 cm^{-1}. Scale bar: 5 µm.

CHAPTER 3

TRANSPORT PROPERTIES OF SINGLE LAYER EPITAXIAL GRAPHENE ON THE C-FACE OF SILICON CARBIDE

3.1 Background

Magneto-transport results are important to investigating material properties and physical phenomena. a) In a low magnetic field, the conventional Hall effect is observed with a Hall coefficient linearly proportional to the magnetic field. b) In an intermediate magnetic field, oscillations in the longitudinal resistance are observed. c) In a strong magnetic field, the Hall coefficients start to quantize at specified values and the longitudinal resistance will demonstrate zero values. Figure 3.1 is an example of a typical Hall transport measurement on a GaAs-Al_xGal_xAs heterostructure without gate voltage at T=8 mK (Ebert, et al., 1982). Its longitudinal resistance and Hall resistance clearly demonstrates the evolution of the three regions with an increasing magnetic field.

In the quantum Hall region, Hall resistance has been observed to be quantized in units of $\frac{h}{2e^2}$ with an accuracy that is specified in parts per million. The accuracy of quantum Hall effect can be utilized as a resistance standard (Tzalenchuk, et al., 2010). The quantized Hall resistance plateaus are also used as the finger prints to characterize material properties, especially to confirm the existence of the 2D massless Dirac Fermions in graphene (Novoselov, et al., 2005; Zhang, et al., 2005). In this chapter, I will

demonstrate how to confirm single layer epitaxial graphene on the C-face is truely two-dimensional graphene with its characteristic quantum Hall effect.

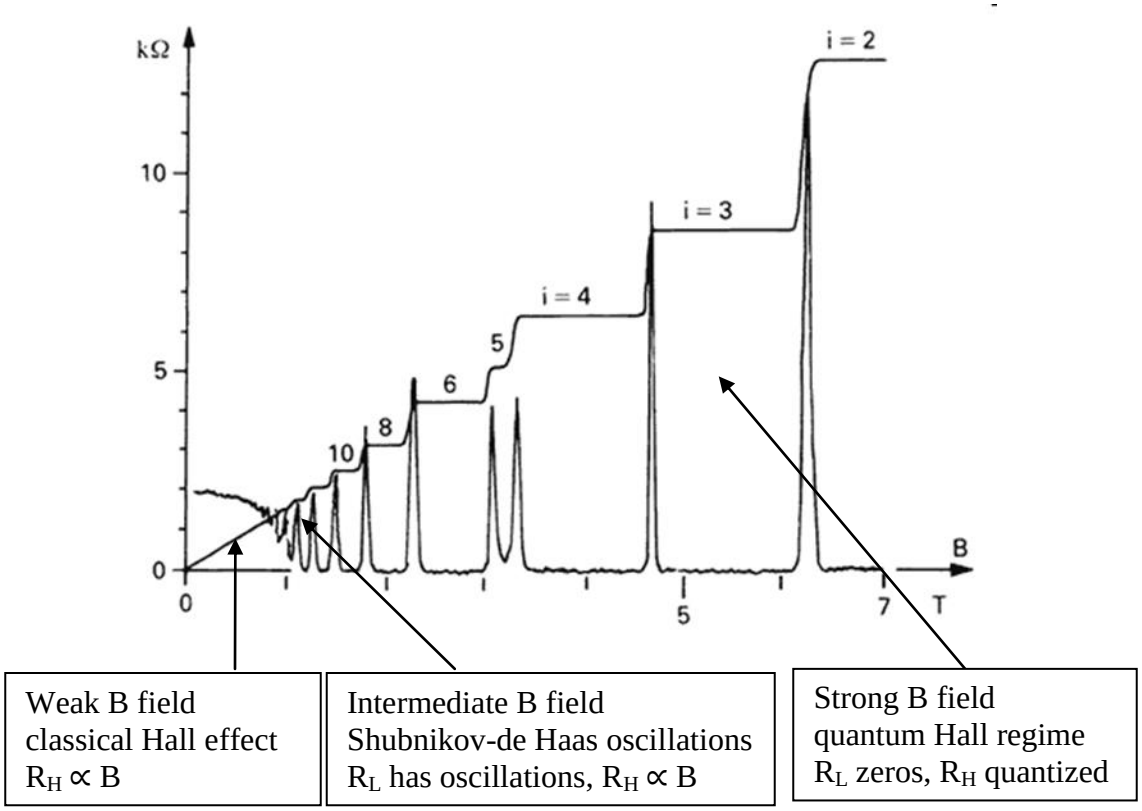

Figure 3.1: Example of longitudinal resistance and Hall resistance changes with an increasing perpendicular magnetic field at T=8 mK. For a sample with fixed carrier density and mobility, when B is small, the Hall resistance follows the classical Hall Effect, i.e., linear relation between ρ_{xy} and B. When B is intermediate, longitudinal resistance starts to evolve oscillations, i.e., Shubnikov de Hass oscillations, and the Hall resistance shows kinks. When B is strong enough, the longitudinal resistance will exhibit zero resistance at minima and Hall resistance will exhibit quantized plateaus (Ebert, et al., 1982).

3.1.1 Landau Quantization

For charged particles in a magnetic field, the momentum has to be written in a gauge invariant form (Jackson, 1999)

$$p \to \prod = p + eA(r) \qquad (3\text{-}1)$$

where A(r) is the vector potential that generates the magnetic field $B = \nabla \times A(r)$. This substitution is valid as long as the lattice spacing *a* is much smaller than the magnetic length $l_B = \sqrt{\frac{\hbar}{eB}}$. Because *a* is always in the order of several Ångströms to 1 nanometer, and $l_B \approx \frac{26nm}{\sqrt{B(T)}}$, this condition is fulfilled for all lattice constants, even under the highest magnetic field that current facilities can supply (45T for steady magnetic field and 80T for pulsed magnetic field)

With the substitution, the relativistic particle Hamiltonian in a magnetic field can be written as (see, for example, Zheng, et al., 2002; Sharapov, et al., 2004; Gusynin, et al., 2005b; Goerbig, et al., 2009)

$$H^B = \upsilon(p + eA(r)) \cdot \sigma \qquad (3\text{-}2)$$

where σ is the 2D spin operator. The commutator of the gauge invariant momentum is

$$\left[\prod_x, \prod_y\right] = -ie\hbar\left(\frac{\partial A_y}{\partial x} - \frac{\partial A_x}{\partial y}\right) = -ie\hbar(\nabla \times A)_z = -ie\hbar B = -i\frac{\hbar^2}{l_B^{\,2}} \qquad (3\text{-}3)$$

Ladder operators are introduced to provide a quantum mechanical treatment of the rescaling one-dimensional oscillator Hamiltonian:

$$a = \frac{l_B}{\sqrt{2}\hbar}(\prod_x - i\prod_y), \text{ and } a^+ = \frac{l_B}{\sqrt{2}\hbar}(\prod_x + i\prod_y)$$

$$\left[a, a^+\right] = 1$$

$$\prod_x = \frac{\hbar}{\sqrt{2}l_B}(a^+ + a), \text{ and } \prod_x = \frac{\hbar}{\sqrt{2}l_B}(a^+ - a)$$

Hence the relativistic particle Hamiltonian is rewritten with the ladder operators as

$$H^B = \upsilon\begin{pmatrix} 0 & \prod_x - i\prod_y \\ \prod_x + i\prod_y & 0 \end{pmatrix} = \sqrt{2}\frac{\hbar\upsilon}{l_B}\begin{pmatrix} 0 & a \\ a^+ & 0 \end{pmatrix} \qquad (3\text{-}4)$$

Solve the Schrödinger equation

$$H^{B}\varphi_n = \varepsilon_n \varphi_n$$

The eigenvalues of the equation are given by

$$\varepsilon_{\lambda,n} = \lambda \frac{\hbar \upsilon}{l_B}\sqrt{2n} = \lambda \hbar \upsilon \sqrt{\frac{2neB}{\hbar}} = \lambda \upsilon \sqrt{2neB\hbar} \qquad (3\text{-}5)$$

where λ, n are the quantum numbers, $\lambda = \pm$ and n is an integer.

The energy levels which electrons (holes) can occupy are quantized to discrete energy levels denoted as above, which are called as Landau levels (LLs). The LLs of graphene are depicted in Figure 3.2 a).

3.1.2 Shubnikov-de Haas Oscillations

Shubnikov-de Haas oscillations are quantum oscillations in the longitudinal resistance ρ_{xx} with a magnetic field. It provides information about the period of oscillation, phase shift of oscillation and amplitude of oscillation (Luk'yanchuk, et al., 2004; Zhang, et al., 2005; Berger, et al., 2006). The application of a magnetic field perpendicular to the sample surface will quantize the in-plane motion of charge carriers into specific energy levels (LLs). The energy levels positions are determined by the external magnetic field. With increasing magnetic field, the Landau levels are further separated. A maximum ρ_{xx} is expected when the Fermi level crosses a Landau level, where the scattering in the channel is increased. A dip in ρ_{xx} is expected when the Fermi level falls in-between two Landau levels. The ρ_{xx} oscillations can be observed either by changing the magnitude of magnetic field or by changing the charge carrier density (and hence the Fermi energy) with a gate voltage at fixed magnetic field (Novoselov, et al., 2005).

3.1.3 Unconventional Integer Quantum Hall Effect

3.1.3.1 Edge States

For wide conductors, a confining potential in the y- direction (in the same plane of but perpendicular to the current flow direction) is introduced and it changes the Hamiltonian eigenvalues of the system (Halperin, 1982). Figure 3.2 b) is the relativistic Landau levels with such confining potential. It shows the LLs are bent upwards when approaching the sample edge. The electrons move in a particular direction because of the upward bending of the confinement potential. This is called the edge state chirality. The chirality is the same for all edge states at the same sample edge where the confinement potential gradient does not change its direction. Even if an electron would be scattered from one edge state to another at the same edge, this would not change the direction of motion. Therefore the electron cannot backscatter unless the scattering processes to the opposite edge also reverse the chirality. Compared to the magnetic length l_B which determines the spatial extension of quantum states, however, a typical graphene Hall bar has a width of about 1 µm. The backscattering processes are therefore strongly suppressed.

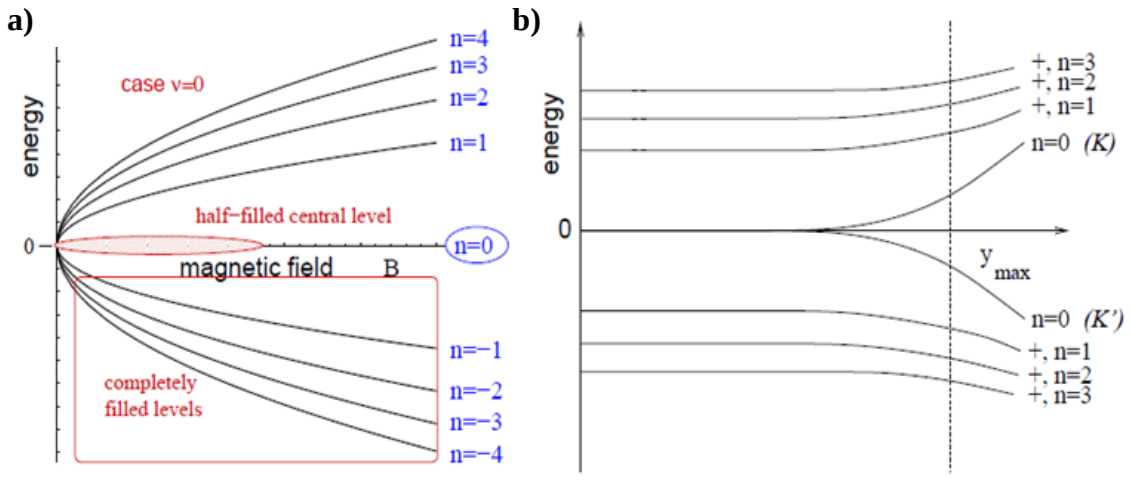

Figure 3.2: a) Filling of the bulk Landau levels at ν = 0. All electron-like LLs (λ = +) are unoccupied whereas all hole-like LLs (λ = −) are completely filled. The n = 0 LL is altogether half-filled. b) Relativistic Landau levels with confining potential. Whereas the electron-like LLs (λ = +) are bent upwards when approaching the sample edge, the hole-like LLs (λ = −) are bent downwards. (Goerbig, et al., 2009).

3.1.3.2 Zero Resistance in the Quantum Hall Regime

The most common configuration to measure a two-dimensional system is the six-terminal configuration. Figure 3.3 is a typical sample measurement diagram for a six-terminal Hall bar in the quantum Hall regime. As a result of the suppression of backscattering, electrons originating in the left contact enter the edge states carrying current to the right contacts, while electrons in the right contact enter the edge stats carrying current to the left contact. Therefore, the edges states carrying current to the right are in equilibrium with the left contacts and has a quasi Fermi level equal to μ_L, which makes $\mu_L = \mu_3 = \mu_4$ (Datta, 1997). Similarly, the edges states carrying current to the left are in equilibrium with the right contacts and has a quasi Fermi level equal to μ_R, which makes $\mu_R = \mu_5 = \mu_6$. The longitudinal resistance measured is

$$R_L = \frac{\mu_4 - \mu_3}{eI} = \frac{\mu_6 - \mu_5}{eI} = 0 \qquad (3\text{-}6)$$

The transverse voltage V_H measured by two probes located on the opposite sides of the sample is equal to the applied voltage

$$V_H = -\frac{\mu_4 - \mu_6}{e} = -\frac{\mu_L - \mu_R}{e} \qquad (3\text{-}7)$$

$$R_H = \frac{V_H}{I} = \frac{\mu_L - \mu_R}{eI} \qquad (3\text{-}8)$$

If the Fermi level lies on a bulk Landau level, then there is a continuous distribution of allowed states from one edge to the other. Electrons can scatter from the upper edge to the lower edge through the allowed energy states in the sample center. The backscattering gives rise to a maximum in the longitudinal resistance.

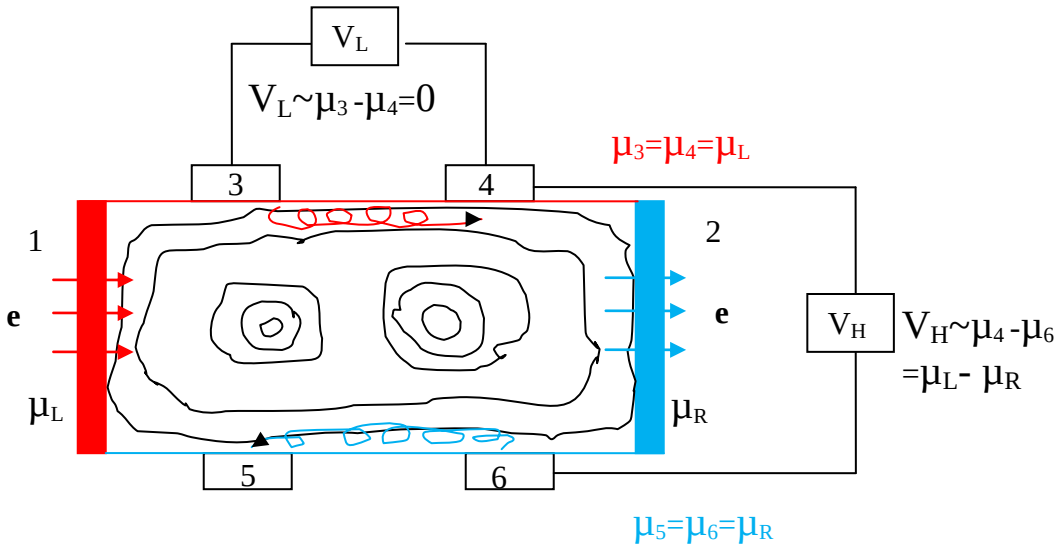

Figure 3.3: Hall bar at the quantum Hall regime. The longitudinal resistance measured between 2 and 3 (or 5 and 6) is $R_L = (\mu_3 - \mu_4)/eI = (\mu_5 - \mu_6)/eI = 0$. The Hall resistance is determined by the potential difference between the two edges and is thus measured between the contacts 4 and 6 (or 3 and 5), where $\mu_4 - \mu_6 = \mu_L - \mu_R$, and so $R_H = (\mu_L - \mu_R)/eI$.

3.1.3.3 Landau Level Conduction

The number of edge states, which is equal to the number of filled Landau levels in the bulk, determines the current in the conductor (Halperin, 1982)

$$I_n^x = -ge\sum_k \langle n,k|\upsilon_x|n,k\rangle \qquad (3\text{-}9)$$

where v_x is the carrier velocity, n is the Landau index, and k is the wave vector, g is the degeneracy. Using the energy dispersion relation above and considering the energy boundary, the above equation turns to

$$I_n = -\frac{e}{h} gn(\mu_{\max} - \mu_{\min}) \qquad (3\text{-}10)$$

where n is the number of edge states at the Fermi energy = number of bulk Landau levels below the Fermi energy. So the Hall resistance at quantized plateaus can be rewritten as:

$$R_H = \frac{h}{ge^2 n} \qquad (3\text{-}11)$$

As two-dimensional massless relativistic particles, graphene holds striking difference in quantum Hall effect compared to conventional two-dimensional materials. If it were a conventional two-dimensional material, taking into account the spin and valley degeneracy, the Hall resistance for graphene should be $R_H = \frac{h}{4e^2 n}$, $n = 1,2,3...$ However, the Dirac like dynamics of graphene give rise to an abnormal Hall quantization (Gusynin, et al., 2005)

$$R_H = \frac{h}{2(2n+1)e^2}, n = 0,\pm 1,\pm 2,\pm 3\ldots \qquad (3\text{-}12)$$

This difference comes from the quantum anomaly of the $n = 0$ Landau Level, i.e., by the fact that it has two times smaller degeneracy than the levels with $n > 0$ and its energy does not depend on the magnetic field (Gusynin, et al., 1994).

3.2 Fabrication Methods and Measurements

3.2.1 Epitaxial Graphene Hall Bar Fabrication

Epitaxial graphene Hall bar structure was fabricated on the single layer epitaxial graphene on the C-face of SiC to evaluate its material properties (Levinson, et al., 1997). The fabrication process is described as follows:

1. Spin coat 450 nm PMMA resist (950/A6) on the epitaxial graphene sample surface with a spin coater.
2. Pattern the alignment marks group on the resist with e-beam lithography. Develop the structure in PMMA developer (IPA: MIBK=3:1) for 30 seconds after the electron beam exposure.
3. Deposit 5 nm Cr as the adhesive layer at a rate of 0.5 Å/s and 45 nm Au at a rate of 1 Å/s. Lift off the metal layer in warm acetone ((~50 ºC in water bath).

4. Examine the graphene sample under Raman optical microscope. Select single layer graphene regions with the same method described in Chapter 2. Design Hall bar patterns on the chosen areas with e-beam lithography compatible software.
5. Pattern Hall bar with different electron beam current (10 pA, 100 pA, and 6 nA) and dosage on the surface coated with positive e-beam resist PMMA.
6. Develop the structure in PMMA developer and etch away extra graphene regions with oxygen plasma in reactive ion etching (RIE). Soak the sample in warm acetone for 1hr to remove PMMA mask.
7. Pattern metal contacts on the PMMA coated sample surface with e-beam lithography. Develop the structure with PMMA developer. Deposit 5 nm Cr and 40 nm Au with e-beam evaporator for the metal contacts. Lift off metal layers in warm acetone to obtain a finished Hall bar structure with metal contacts.

Figure 3.4 is a schematic diagram for this device fabrication process. Figure 3.4 k) and l) are the AFM image and optical image with false color for a finished device.

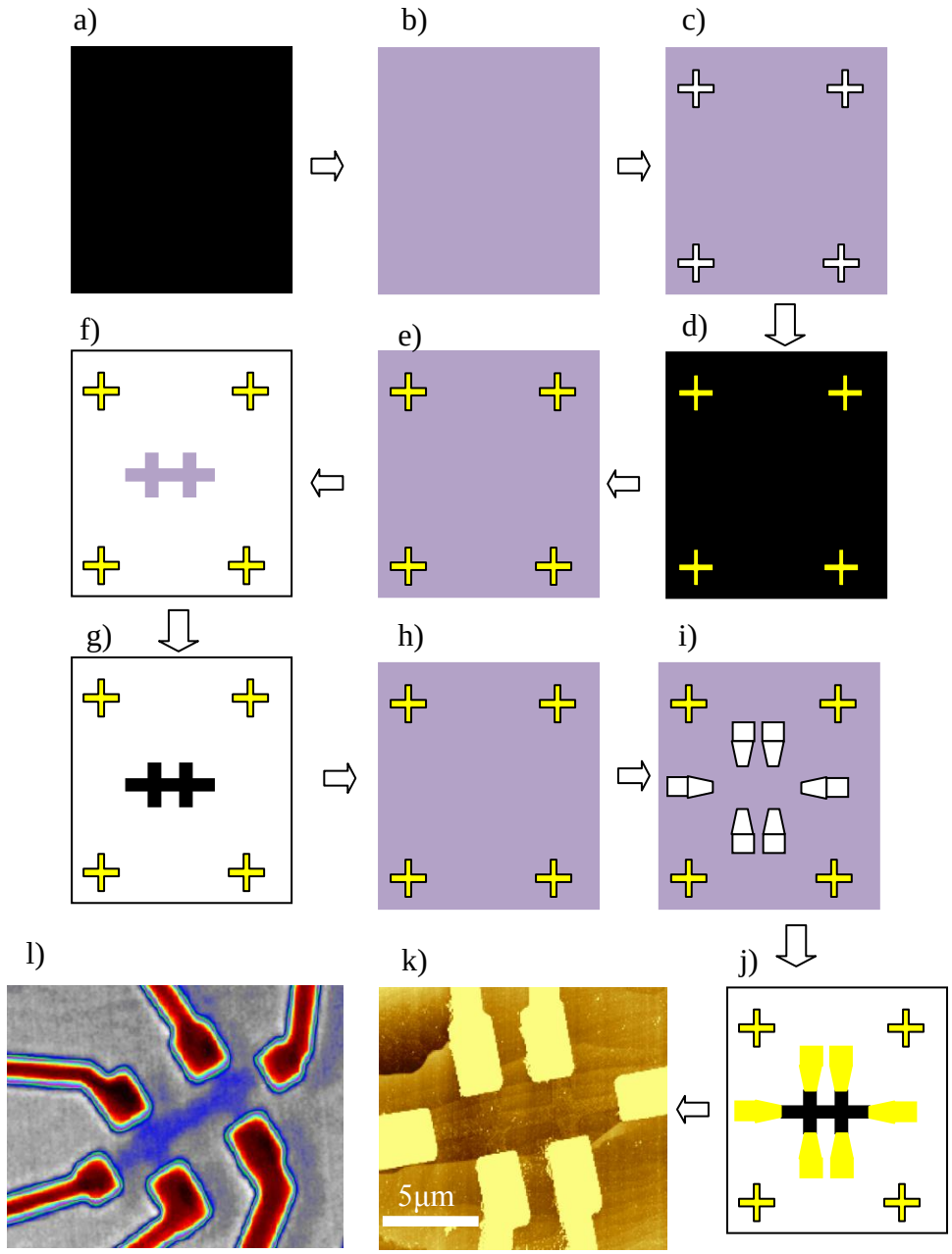

Figure 3.4: Schematic diagram of the fabrication process of an epitaxial graphene Hall bar on a selective area of silicon carbide. a)→b) PMMA spin coating. b)→c) Alignment mark patterning. c)→d) Alignment mark deposition and lift-off. d)→e) Determining the patterning area with Raman and AFM. e)→f) Defining the Hall bar geometry with patterning and RIE etching. f)→g) Removing the resist with acetone. g)→h) PMMA spin coating. h)→i) Contacts patterning and developing. i)→j) Contacts metal deposition and lift-off. k) AFM for one typical epitaxial graphene Hall bar device with metal contacts. The graphene structure can be seen as the darker area inside the contacts with 6 terminals. l) An optical image for one such device with a false color effect to emphasize the graphene Hall bar region. Scale bar: 5 µm.

3.2.2 Electrical Measurement

The electronic and transport properties of graphene were investigated through four-point and Hall effect measurements at room temperature and low temperature. For room temperature measurements, a four-point probe station connected to a lock-in amplifier was used. Low temperature measurements were carried out in a cryostat with a magnetic field power supply. The sample (SiC piece) was glued with epoxy on a chip carrier and the device contacts on SiC were bonded to the chip carrier pads with wire bonder using aluminum wires. Inside the cryogenic dewar, the sample was cooled down and warmed between liquid helium temperature (4 K) and 400 K. The maximum magnetic field from the power supply is 9T. For measurements done in the National High Magnetic Field Laboratory in Tallahassee FL, a maximum magnetic field of 18T and a temperature of 1.4 K was reached.

For the longitudinal and Hall resistance measurements, a small AC current (I=100nA) passed through the device current contacts. The lock-in amplifier was used as a constant current source with a series resistor of 20 MΩ. The output AC voltage was chosen to be 2 V. Two-point resistance of graphene device was measured to be of the order of several kΩ, so the current inside the circuit could be considered as constant. A typical measurement frequency was chosen to be 13 Hz. The transverse voltage (V_{xy}) and longitudinal voltage (V_{xx}) were measured by the lock-in amplifier input channel at the same frequency. For the Hall bar geometry, the magneto-resistance R_{xx} and Hall resistances R_{xy} are obtained from

$$R_{xx} = \frac{V_{xx}}{I}, R_H = \frac{V_{xy}}{I}$$

The device sheet carrier density can be deduced from

$$n = \frac{1}{R_H e} \qquad (3\text{-}13)$$

To characterize the sample quality, the sample mobility is defined by the semi-classical Drude model at large sheet carrier density range (~1×10^{12} cm^2)

$$\mu = \frac{R_H}{\rho_{xx}} = \frac{1}{en\rho_{xx}} \qquad (3\text{-}14)$$

$$\rho_{xx} = \frac{R_{xx}}{\left(\frac{L}{W}\right)} \qquad (3\text{-}15)$$

where ρ_{xx} is the 2D sheet resistivity, L is the channel length, and W is the channel width.

3.2.3 Device Surface Treatment

The nano fabrication process involves multiple resist coating and removing steps. The majority of the resist (PMMA) can be removed by its remover (acetone); however, clusters of polymer residue are always observed on the sample surface. To get rid of the resist residue, two methods can be applied.

The first method is to enhance the solubility of the resist polymer in a solvent. After e-beam exposure, the developing contrast between the exposed and unexposed regions of the film becomes higher as the molecular weight increases. The polymer solubility, however, is inversely proportional to the molecular weight (Miller-Chou, et al., 2003). It is shown that the PMMA chain breakage percentage increases with the temperature of the solvent, so increasing the lift-off solvent temperature and time will reduce the residue of resist. The condition used in this experiment is 50 °C water bath for 1 hour. 50 °C is chosen below the acetone flash point of 56 °C for safety reasons.

The forming gas method is another surface treatment method. After being soaked in a solvent, the sample is loaded into the vacuum chamber and annealed at 300 °C for 3 hour with a hydrogen and argon mixing gas (hydrogen is 2.9%) at a flow rate of 50 sccm. This method has been shown to clean up sample surface residue to meet STM measurement standards (Ishigami, et al., 2007). Epitaxial graphene samples can also be treated with the forming gas method. The surface appears to have significantly fewer

polymer residues, as shown in Figure 3.5. Before the forming gas treatment, the surface roughness is 0.6nm, after forming gas treatment the surface roughness reduces to 0.3 nm. No defects related Raman D peak was observed after forming gas treatment. Significant hole doping, as large as 10^{13} cm^{-2}, was observed on devices after the forming gas treatment. A reduction in sample mobility was also observed. Figure 3.6 plots the mobility and carrier density for several samples before and after the forming gas treatment.

Regarding our experiment purpose, medium and low doping devices are desired. So the warm-acetone-soaking is chosen for the device preparation.

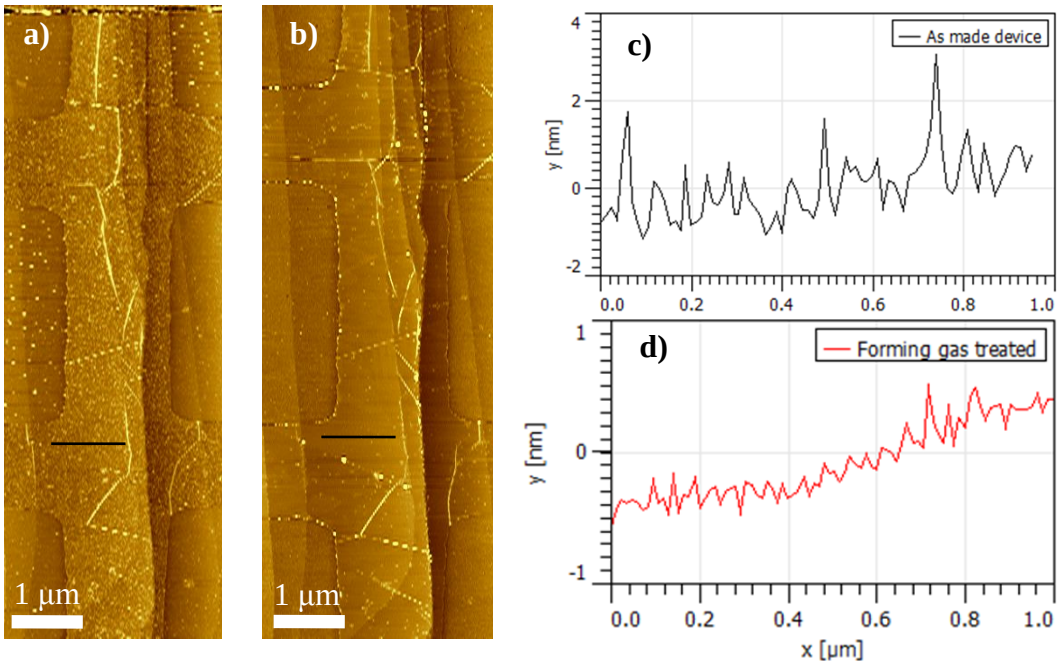

Figure 3.5: Epitaxial graphene surface morphology comparison before and after forming gas treatment. a) AFM image of one graphene Hall bar surface after removing PMMA resist with acetone. b) AFM image for the same structure after forming gas treatment. c) and d) are line scans on graphene regions from a) and b) respectively. Scale bar: 1 µm.

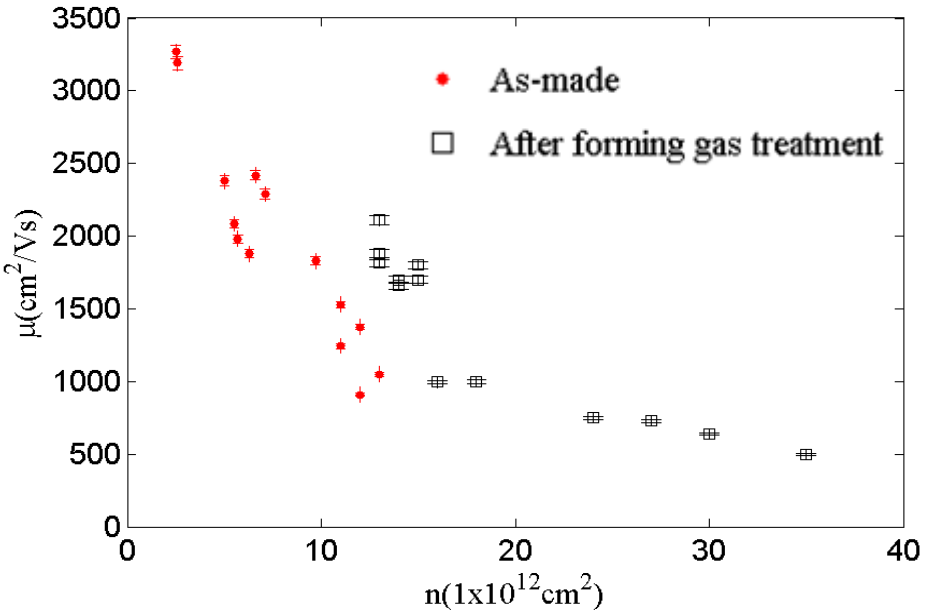

Figure 3.6: Comparison of the carrier density and mobility on samples before (red dot) and after the forming gas treatment (black open square). Heavy hole doping and low mobility are observed after the forming gas treatment on the epitaxial graphene samples.

3.3 Cryogenic Temperature Measurements

3.3.1 Resistance Temperature Dependence

A Hall bar sample made of single layer epitaxial graphene on the C-face was fabricated with the same method described in Appendix A. The dimension of this Hall bar is 1.8 μm×4.6 μm and the Hall bar lay across several SiC steps. Figure 3.7 is the sheet resistance versus temperature curve. The decreasing resistance with the decreasing temperature is expected from the metallic property of graphene. No resistance increase was observed below T=50 K.

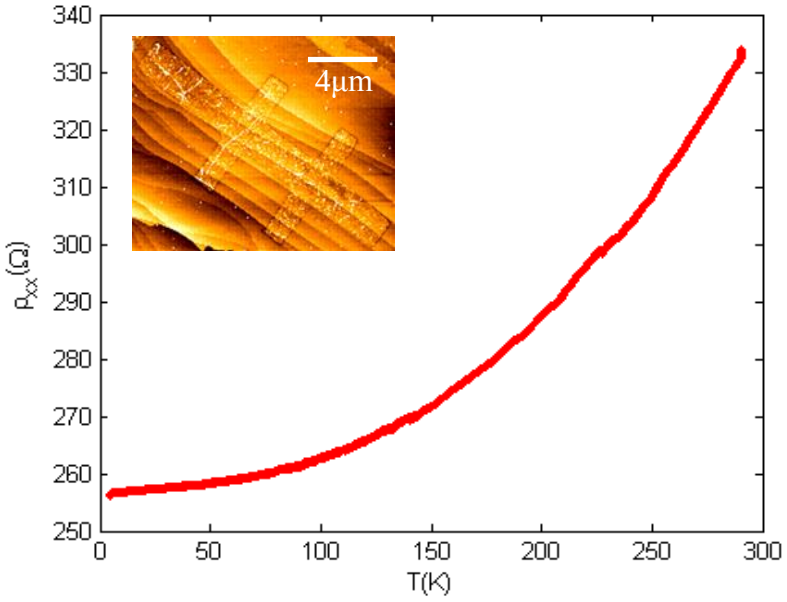

Figure 3.7 Sheet resistance versus temperature on graphene Hall bar (1.8 μm × 4.6 μm). Metallic temperature dependence is observed on a high mobility epitaxial graphene sample. Scale bar: 4 μm.

3.3.2 Shubnikov–de Haas Oscillations

When the sample cooled down to T=1.4 K, the longitudinal resistance ρ_{xx} in the presence of magnetic field was measured. Sample ρ_{xx} demonstrates local maxima and minima at different magnetic field up to 9 T, as seen in Figure 3.8 a). The Landau levels for Dirac electrons are given by Equation (3-5)

$$E_n(B) = \sqrt{2neBv_F{}^2\hbar}$$

where n is the landau index, v_F is Fermi velocity. Shubnikov–de Haas oscillations longitudinal maxima were observed at magnetic fields B_n when $E_n(B) = E_F$ (Soule, 1958; Soule, et al., 1964) . Defining

$$B_F = \frac{E_F{}^2}{2nev_F{}^2\hbar},$$

then

$$\frac{1}{B_n} = \frac{1}{B_F} n \qquad (3\text{-}16)$$

Figure 3.8 b) is a plot of n versus the inverse magnetic field at the ρ_{xx} local maxima (Soule, et al., 1964). Notice the intercept is at zero, which confirms the non-zero Berry's phase (Ando, et al.,1998; Mikitik, et al., 1999) and the existence of Dirac particles in the single layer epitaxial graphene on the C-face of SiC (Sharapov, et al., 2004; Luk'yanchuk, et al., 2004; Zhang, et al., 2005; Novoselov, et al., 2005).

For a two-dimensional electron gas in graphene, $E_F = \hbar v_F k_F$, where k_F is the Fermi wave vector and it can be written with B_F as

$$k_F = \sqrt{2eB_F / \hbar} \qquad (3\text{-}17)$$

The carrier density n_s can be derived from

$$n_s = \frac{g_s g_v k_F^{\,2}}{4\pi} \qquad (3\text{-}18)$$

where g_s and g_v as the spin and valley degeneracy both equal to 2. The sample carrier density calculated from the SdHOs is 1.31×10^{12} cm^{-2}.

SdHOs for the n=1 Landau level can still be seen up to 150 K. The damping of the oscillations with temperature is caused by the thermal broadening of the Landau levels. The temperature dependence of the peak amplitudes is given by (Gusynin, et al., 2005b)

$$A_k(T) = \frac{t_k}{\sinh(t_k)} \qquad (3\text{-}19)$$

Where $t_k = \dfrac{2\pi^2 k_B T \mu}{\hbar \upsilon_0^{\,2} eB}$

Here $A_k(T)$ is the k^{th} SdHOs peak amplitude at temperature T. μ, T, B, and v_0 are the chemical potential, temperature, magnetic field, and the Fermi velocity. Using this equation, the Fermi velocity is found as $v_0 = 1.14 \times 10^6$ m/s, which agrees with the v_0 of exfoliated graphene flakes on SiO_2 (Zhang, et al., 2005; Novoselov, et al., 2005). To

conclude, this Fermi velocity together with the non-zero Berry's phase confirms that single layer epitaxial graphene on the C-face of SiC is truly two-dimensional graphene. The interaction between graphene and the C-face substrate does not affect the graphene properties any more than other substrate such as SiO_2.

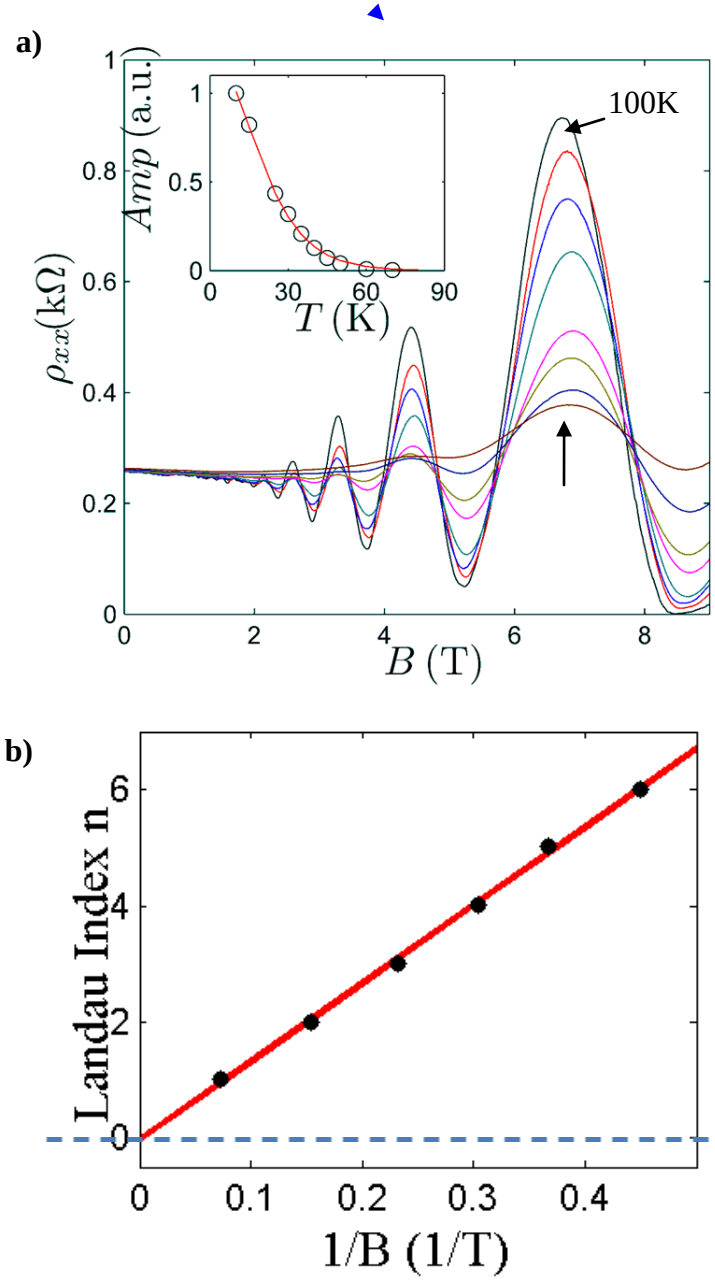

Figure 3.8: a) Temperature dependence of magneto resistance. Main panel, SdHOs at different temperatures, 1.4, 10, 20, 30, 50, 60, 80, and 100 K. Inset is the fitting of SdHOs amplitudes with temperature. b) Landau indices were plotted against the inverse magnetic field, confirming the Berry's phase π.

3.3.3 Unconventional Integer Quantum Hall Effect

As the fingerprint for massless two-dimensional material, unconventional integer quantum Hall effect was also observed on single layer epitaxial graphene on the C-face at T=4 K. QHE is well resolved in Figure 3.9. Quantum Hall plateaus are shown in the Hall resistance versus magnetic field, same as that observed in the exfoliated graphene flakes on SiO_2 (Zhang, et al., 2005; Novoselov, et al., 2005). The Hall plateaus correspond to the transverse resistances

$$R_{xy} = \frac{h}{4e^2(n+\frac{1}{2})} \qquad (3\text{-}20)$$

for n=0 to 3, where n is the Landau level index, which establishes the nontrivial Berry's phase of π, the same as the result from SdHOs plot. The SdHOs from the longitudinal resistance R_{xx} shows the Landau levels from n=0 up to n=8. The SdHOs develop into QHE in high fields, manifested by the characteristic zero resistance minima and Hall plateaus. The graphene charge density obtained from the Hall coefficient was found to be $n_s=1.27\times10^{12}$ cm^{-2} with hole doping. Graphene layers are negatively doped due to the work function difference in the SiC-graphene interface, so the positive doping here should come from the ambient environment. As a matter of fact, the graphene sample doping density was observed to change with the environment humidity. It was found the charge densities n_s were 0.9, 1.28, and 1.27 $\times10^{12}$ cm^{-2} during three times cooling processes in cryostat. The QHE was observed for all the three experimental runs. Although by changing the environment humidity the sample carrier density can be tuned, a method robust to environmental influence to control sample doping is desired and will be elaborated in the next chapter.

The mobility of the sample at 1.4 K was calculated to be 20,000 cm^2/Vs at n=1.27 $\times10^{12}$ cm^{-2} from the Hall measurement. Despite the fact that the graphene sample was transferred from one system to another, warmed up and cooled down multiple times,

doped by environment, and had pleats on multiple SiC steps, the mobility was still comparable to the exfoliated graphene on SiO_2 substrate of the highest quality. A similar measurement at room temperature gave μ=15,000 cm^2/Vs. This shows only a mild temperature dependence on graphene mobility. These observations demonstrate that: a) the scattering from impurities was weak; b) the electron-phonon scattering was suppressed; c) the graphene was continuous across steps on the SiC substrate.

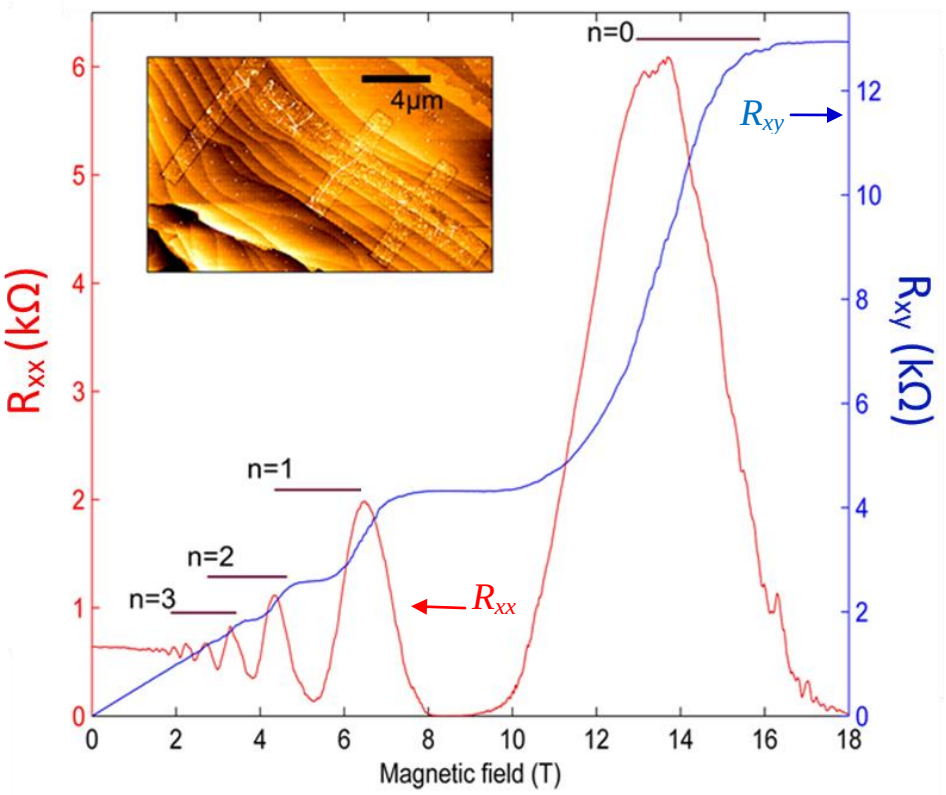

Figure 3.9: Quantum Hall effect in a C-face single layer epitaxial graphene sample measured at 1.4 K. Hall resistance (blue, on the right) as a function of magnetic field shows characteristic Hall plateaus at $R_{xy} = \frac{h}{4e^2(n+\frac{1}{2})}$, where n is the Landau level index. Magneto resistance R_{xx} (red, on the left) shows characteristic oscillations and drops to zero for low Landau indices. Inset: AFM image of the Hall bar under measurement.

3.3.4 Substrate Effect

To examine whether the SiC substrate terraces affect the transport properties of the top graphene layer, a device on top of a single, flat SiC step was fabricated. Six metal contacts were deposited on a selective single layer graphene island where the SiC underneath was step free. This device was loaded into the cryostat and measured at T=4 K. Fig 3.10 illustrates the magneto resistivity and Hall resistance dependence on the magnetic field. The unconventional integer quantum Hall effect was observed combined with the well resolved SdHOs. Using the linear part of Hall resistance, we can calculate the carrier density and mobility as n=0.92 ×10 ^{12} cm^{-2}, and μ=21,100 cm^2/Vs. This value is in the same range as that obtained on the graphene Hall bar across several SiC steps (μ=20,000 cm^2/Vs at n=1.27×10 ^{12} cm^{-2}). This confirms that the C-face SiC substrate step edge does not significantly affect the graphene mobility under the current device fabrication conditions. Other scattering sources are the major limiting factors for device mobilities.

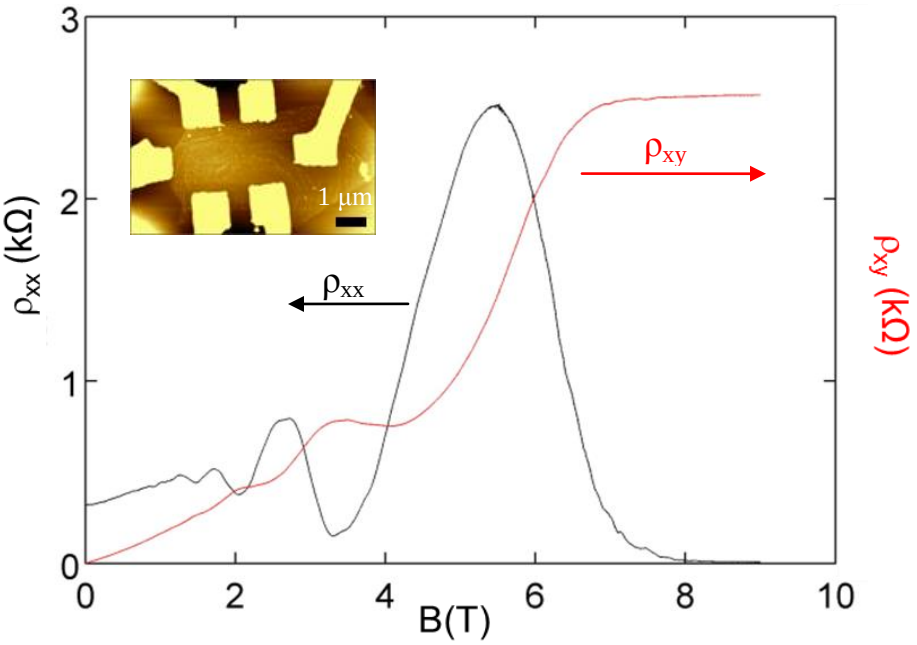

Figure 3.10: QHE in C-face epitaxial graphene for micrometer wide samples. Longitudinal resistivity: black trace, left-hand side label; Hall: red trace, right-hand side label. Hall contacts are deposited to SiC step-free non-patterned single layer graphene. ρ_{xx}=320 Ω, μ = 21100 cm^2 /Vs at charge density n = 0.92 × 10^{12} cm^{-2}. Scale Bar: 1 μm.

CHAPTER 4

FIELD EFFECT TRANSISTOR OF EPITAXIAL GRAPHENE ON THE C-FACE OF SILICON CARBIDE

4.1 Introduction

Graphene is considered to be a promising candidate for a new generation of electronics. Controlling the carrier density and the conductivity is crucial for electronic applications. The thick semi-insulating SiC substrate makes it a natural platform for device electrical measurement since no transferring process is necessary. In contrast to the SiO_2 substrate of exfoliated graphene, it also raises challenges to back gate the epitaxial graphene. Recently an epitaxial graphene transistor with ion implanted SiC back gate has been demonstrated (Waldmann, et al., 2011). This gate device, however, can only operate at temperatures above 50K since the implanted carriers will freeze out at low temperatures. In addition, it requires very high energy (~2 MeV) to implant nitrogen deep into SiC to avoid carrier diffusion to the surface during graphitization. These high energies are not available commercially. The ion implantation method is not compatible with current micro-electronics fabrication technology.

Top gating has provided an alternative method to effectively adjust the material carrier density and carrier type locally (Williams, et al., 2007; Kedzierski, et al.,2008; Li, et al., 2008). Common top gate dielectrics are hafnium oxide (HfO_2), aluminum oxide (Al_2O_3) and silicon dioxide (SiO_2). Top gate dielectric electrodes for individual device can decrease the mobility (Robinson, et al., 2010).

In this chapter, I will discuss how to change the carrier density and carrier type in single layer epitaxial graphene with a local top gate. In our case, the top gated sample

will still maintain a high mobility due to the slow deposition of natural aluminum oxide and the absence of adhesive layer (ξ 4.2.2). The C-face single layer epitaxial graphene has been confirmed to be truly two-dimensional graphene (Wu, et al., 2009). The transport properties of single layer epitaxial graphene with a top gate were measured and analyzed. A novel top gate dielectric boron nitride directly grown on multilayer epitaxial graphene will be discussed.

4.2 Experimental Tools and Methods

4.2.1 Silicon Carbide Alignment Marks

Alignment marks are used to locate the pattern areas in multiple device patterning steps. Cr/Au bi-layer is normally used as alignment mark metals. However, when high temperature (above 1000 ºC) is needed, metal alignment marks would either melt or evaporate. A new method to make alignment marks is necessary for the high temperature device process. Because SiC can be patterned, selectively masked with metal, etched and thoroughly cleaned, alignment marks can be patterned by selective deep etching of SiC below the surface. This method ensures the SiC surface for graphitization is the original CMP epitaxy ready surface. The height contrast between the surface and the alignment marks area can be used to identify the pattern areas in the optical microscope and SEM. The steps to make SiC alignment marks are described and illustrated in Appendix A. Figure 4.1 shows the alignment mark morphology in SEM and AFM.

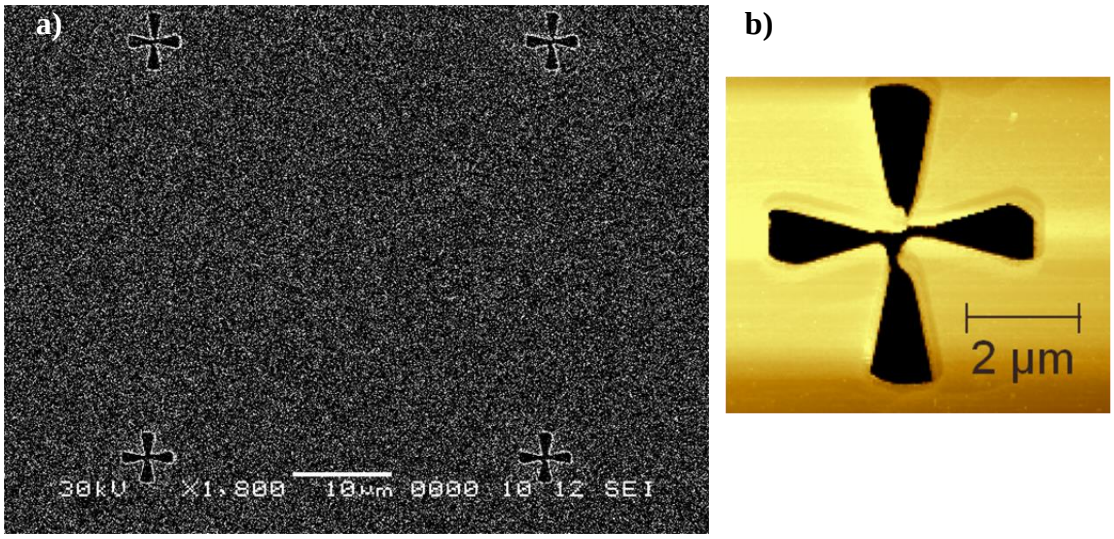

Figure 4.1: a) SEM image of a group of alignment marks at 1,800 magnification. The contrast between the alignment mark area and flat surface makes the alignment mark visible during the EBL process. b) AFM image on one alignment mark. The depth is measured to be 560 nm. Scale Bar: 2 µm.

4.2.2 Gate Dielectric

The FET gate dielectric/gate contact can be made by a one-step metal deposition. It includes deposition of aluminum in e-beam evaporator with different deposition rates. It will create aluminum oxide/ aluminum metal stack as gate dielectric and gate contact respectively. This method is described as follows:

1. Transfer the patterned sample into e-beam evaporator. Deposit aluminum at rate 0.2 Å/s to form natural aluminum oxide as the gate dielectric (10 nm ~ 30 nm).
2. Start the deposition at a base pressure 8 $\times 10^{-6}$ torr. Stop the system pumping once the deposition is finished.
3. Wait for 10 minutes. Then deposit aluminum at a fast rate of 1 Å/s for another 30nm for the gate contact metal.

The high chamber base pressure and slow deposition rate will enhance the formation of natural aluminum oxide as gate dielectric. The dielectric constant was

characterized by measuring the change of the sample carrier density with the gate voltage. A Hall bar sample with 30 nm gate dielectric was measured at B=1 T. The sample carrier density is given by the Hall effect as

$$n = \frac{1}{eR_H}$$

As shown in Figure 4.2, the carrier density coefficient is 2.25×10^{12} cm^{-2} V^{-1} for 10 nm native aluminum oxide.

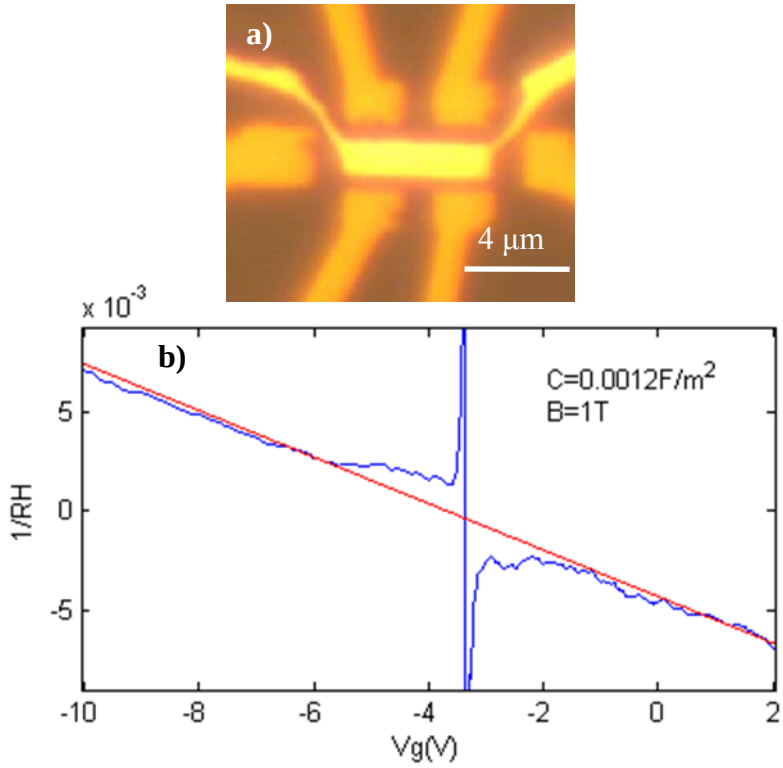

Figure 4.2: Gate dielectric efficiency calculation. 30 nm natural aluminum oxide was deposited as gate dielectric on a graphene Hall bar structure, as shown in a). Applying a perpendicular magnetic field B=1 T to measure the Hall resistance versus gate voltage. $n=\alpha V_g$. By measuring the slope of the linear response of carrier density versus gate voltage, the gate capacitance can be determined. In this case, the carrier density change caused by V_g is 2.25×10^{12} cm^{-2} V^{-1} for aluminum oxide of 10 nm. Scale bar: 4 μm.

4.3 Top Gated Graphene Devices

4.3.1 Resistance vs Vg at B=0 T

A C-face single layer epitaxial graphene Hall bar with a top gate was fabricated. The Hall bar was made with the same method described in Chapter 3. It has a width of 1 μm and a length of 4.3 μm between the voltage contacts. 20 nm aluminum oxide was deposited with the slow deposition method (ξ 4.2.2) as the top gate dielectric. 30nm aluminum was deposited as the top gate metal contact. The longitudinal resistance ρ_{xx} and Hall resistance ρ_{xy} of the top gated Hall bar were measured with lock-in amplifier SR830. The top gate voltage was supplied by Keithley 2400 dc voltage output. The gate leakage current was measured by Keithley to ensure the current was below 5nA and no gate dielectric break-down happened.

Figure 4.3 is the result of resistivity as a function of gate voltage at T = 4 K at zero magnetic field. The resistivity undergoes a maximum at V_g = 0.3 V, clearly showing the conductance modulation by the electrostatic field on both sides of the Dirac point (Figure 4.3 a)). A high to low resistivity ratio $\frac{R_{(Vg=0.3V)}}{R_{\max}} = \frac{I_{off}}{I_{on}} = 13$ is commonly observed for two-dimensional single layer graphene. The dielectric thickness on this sample is 20nm. Based on the gate capacitance calibration results, the gate efficiency to change the charge density is 1.15×10^{12} cm^{-2}/V. The gate voltage V_g = 0.3 V at the Dirac point gives a charge density n_S = 3.45 × 10^{11} cm^{-2} induced by the gate to compensate the natural sample doping. This is very close to the doping density n_S = 3.7×10^{11} cm^{-2} measured from the Hall effect ρ_{xy} at zero gate voltage (will be shown in 4.3.2).

Numerical calculations (Nomura, et al., 2007; Hwang, et al., 2007) show that $\sigma(n)$ changes from a linear dependence to a sub-linear dependence as the scattering mechanism changes from long-range scattering (such as charged impurity scattering) to

short range scattering (such as atomic defects in the lattice). With an empirical conductivity carrier density dependence formula (Dean, et al., 2010),

$$\sigma = \frac{1}{\frac{1}{ne\mu + \sigma_{res}} + \rho_s} \qquad (4\text{-}1)$$

the experiment result can be quantitatively interpreted. Using this equation, the experiment data can be fitted in every region except those close to the Dirac point. Considering the asymmetry between the electron and hole branches, the fitting result is different for positive (electron) and negative (hole) carrier density. For the hole branch, mobility μ= 14,100 cm^2/Vs and short range scattering resistance ρ_s=156 Ω, while for the electron branch, mobility μ= 9160 cm^2/Vs and short range scattering resistance ρ_s=115 Ω.

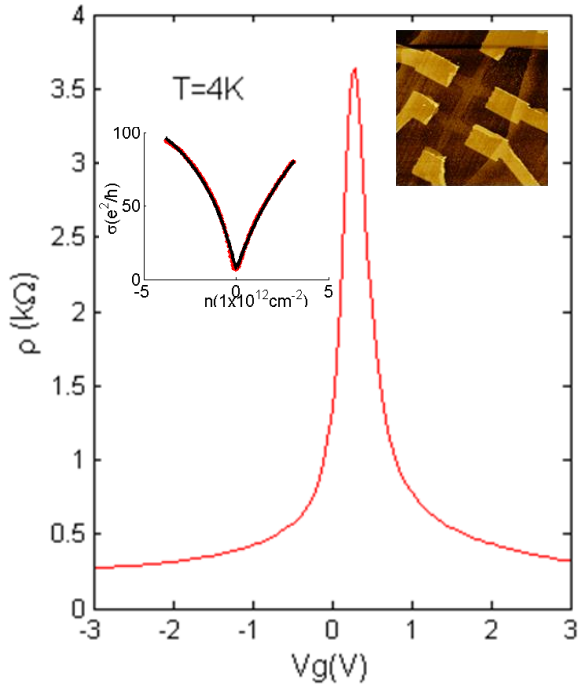

Figure 4.3 Resistance change with top gate voltage for a Hall bar (width=1 μm, length=4.3 μm) at T=4 K. The top gate dielectric is 20 nm thick aluminum oxide. The inset is the fitting result of equation (4-1).

4.3.2 Resistance vs Vg in Magnetic Field

The sample was also measured in a magnetic field. The longitudinal resistance ρ_{xx} and Hall resistance ρ_{xy} were measured with a changing magnetic field at a fixed gate bias. Figure 4.4 a) is the measurement at V_g=0 V and V_g=0.4 V. The sample carrier density is determined by the slope of the linear region of ρ_{xy}. At V_g=0 V, it is hole doped with density of 3.7×10^{11} cm^{-2} and the mobility is 12,200 cm^2/Vs. At V_g=0.4 V, the carrier type changes to electron. The doping density is 4.6×10^{11} cm^{-2} and the mobility is 7,000 cm^2/Vs. As the magnetic field goes above 7T, the system reaches Landau level n=0 and the quantum Hall plateau at ρ_{xy}=12.8 kΩ starts to develop. The longitudinal resistance reaches ρ_{xx}=0. A better way to demonstrate how the top gate voltage affects the graphene transport in the magnetic field is to measure the longitudinal resistance and Hall resistance change with the gate voltage at fixed magnetic field. A gate voltage sweep at B=9 T in figure 4.4 b) reveals the fully developed quantum Hall plateaus at $\sigma_{xy} = \nu \frac{e^2}{h}$ for ν = 2, 6, 10, 14 (σ_{xy} is the transverse conductivity). A vanishing resistivity for the ν = 2 plateau clearly confirms that this is a single layer graphene. The magnetic field sweeps at two different gate voltages, in the p- and n-doped region, show a well resolved ν = 2 plateau that extends into a large field region. In particular, this shows the QHE can be switched from p to n using the top gate. Note that the mobility for n-doping is significantly lower than that for p-doping. This leads to better developed longitudinal resistance oscillations on the hole doping side than the electron doping side.

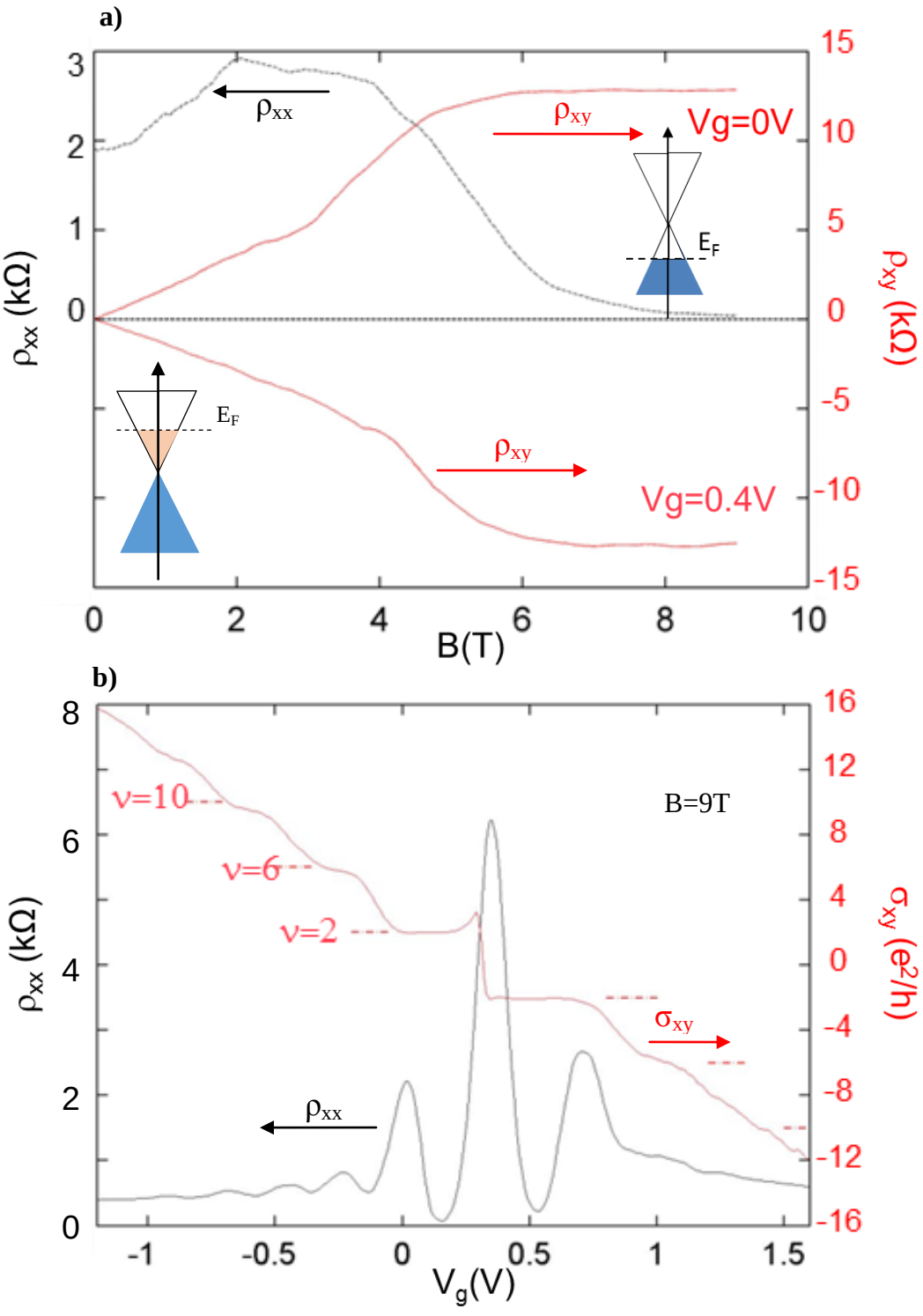

Figure 4.4: a) (red curves) Hall resistance ρ_{xy} versus magnetic field measured at different gate voltages (i) V_g = 0.4 V, n-doping, n= 4.6 × 10^{11} cm^{-2}, μ = 7000 cm^2/Vs, (ii) V_g = 0 V, p-doping, p = 3.7 × 10^{11} cm^{-2}, μ = 12200 cm^2/Vs. b) Resistivity ρ_{xx} (black) and Hall resistance σ_{xy} (red) versus gate voltage at 4 K and 9 T, showing plateaus in the n- and p-doping regions.

4.4 A Novel Dielectric Material: Boron Nitride

4.4.1 Introduction

Hexagonal boron nitride (h-BN) consists of layers of boron and nitrogen atoms bonded by strong covalent bonds that are held together by weak van der Waals forces. Its in-plane lattice mismatch with graphene is less than 2%. Hexagonal boron nitride is an insulator with a band gap 5.2~5.9 eV. Hexagonal boron nitride has a dielectric constant 4.6 compared to 3.9 of SiO_2 and 9.1 of Al_2O_3. Its dielectric breakdown strength is about 8 MV/cm.

With the same mechanical exfoliation method as exfoliated graphene, very thin (1~10 layers) h-BN has been obtained. Because of the flat surface and weak interaction between graphene and h-BN substrate, very high FET mobility up to 275,000 cm^2/Vs at n =$0.8x10^{10}$ cm^{-2} at T=4 K has been observed on such system (Dean, et al., 2010; Zomer, et al., 2011). In addition, the insulator property of h-BN has been utilized as gate dielectric. 2~3 nm h-BN thin film tunneling junction can be used to detect the graphene density of states (Amet, et al., 2012). Graphene-h-BN-Graphene sandwich structures were also proposed as a tunneling transistor (Britnell, et al., 2012).

So far most of the experiments on the graphene–h-BN system are working on the exfoliated h-BN flakes from an h-BN crystal. This method, however, requires very delicate exfoliation method, sample transferring and alignment process. The size of h-BN is limited to tens of micrometer. In order to produce h-BN in a more controllable way, several groups have succeeded to grow h-BN on metals with chemical vapor deposition method (Shi, et al., 2010; Kim, K.K et al., 2012). h-BN characteristics were confirmed by Raman, XPS and HRTEM. A recent attempt was to directly grow h-BN on graphene and HOPG with a similar method (Liu, et al., 2011). The existence of h-BN was confirmed by Raman spectrum after growth. From the AFM image profile in Liu's paper (Liu, et al., 2011), the as-grown h-BN has a surface roughness around 3 nm.

4.4.2 Boron Nitride Characterization

4.4.2.1 Ambient Pressure Chemical Vapor Deposition

The SiC substrate provides the necessary condition for the boron nitride growth on epitaxial graphene since both graphene and SiC can withstand very high temperatures (at least 1200 °C) in an inert gas environment without morphology or chemical properties change. Boron nitride was grown on epitaxial graphene with ambient pressure chemical vapor deposition method. The growth system consists of a two zone furnace and H_2/Ar gas line. Ammonia borane powder is sublimated at T=125 °C in the low temperature zone. The sample is loaded in the high temperature zone and heated up to 1000 °C. The decomposition product NH_2-BH_2 and H_2 are transferred by nitrogen and argon mixing gas to the high temperature zone. Boron nitride is formed directly on the epitaxial graphene surface. The growth process and system schematic is described in Appendix B.

4.4.2.2Boron Nitride Conformity

X-ray photoelectron spectroscopy (XPS) is a non-destructive surface analytical tool to analyze the elemental composition and chemical states of a material. The material surface is irradiated with a monochromatic x-ray beam. For x-ray of high enough energy, core level electrons can be knocked out of the atom. The measured kinetic energy of the escaped electrons is related to the binding energy by

$$KE = h\nu - BE - \phi$$

KE is kinetic energy, measured by an electron spectrometer. $h\nu$ is the x-ray photon energy. ϕ is the spectrometer work function, determined by a separate calibration. BE is the unknown binding energy of the element core level electrons.

One sample with fifteen-layer epitaxial graphene on the C-face was used to grow boron nitride with the method described in ξ 4.3.2.1. Before growth, the sample surface appears to be dark due to the graphene layers. After growth, the sample surface turns

whitish. To determine the elemental composition of the material on the sample, XPS was mapped all over the sample surface with a 50 μm spot size spaced by 600 μm. As shown in Figure 4.5, the B1*s* peak is located at 191.5 eV, and the nitrogen 1*s* peak is located at 398.9 eV, which is consistent with that of boron nitride (Park, et al., 1996). The C1*s* peak is located at 284.7 eV (Mathieu, et al., 2011). No additional peaks other than graphene and SiC C1*s* peak are observed, which confirms no additional carbon compound formed during the BN growth. The shapes, intensities and positions of all peaks were the same across the sample. This confirms the assumption that boron nitride uniformly covers the entire surface. Figure 4.5 a) is an SEM image for an epitaxial graphene sample covered with as grown BN. A scratch was made to show the contrast between graphene and BN. The main feature in the figure is the multilayer graphene characteristic pleat. A continuous thin film across the EG pleats can be seen. This SEM image confirms the boron nitride thin film is conformal to the EG surface morphology.

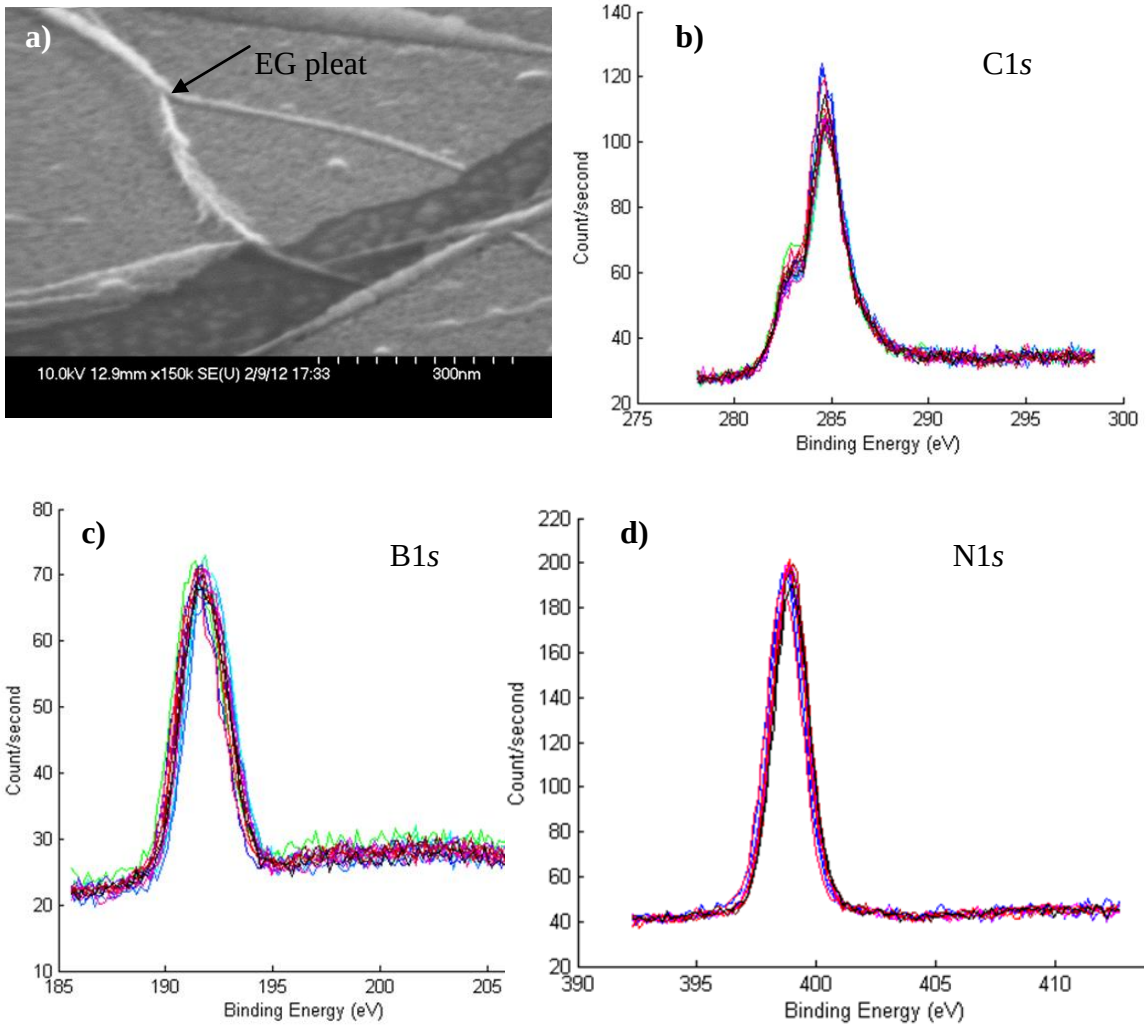

Figure 4.5: Conformal BN thin film growth on top of EG. a) SEM image of a BN thin film covering over graphene pleats. b), c) and d) are C1*s*, B1*s*, and N1*s* XPS peaks collected at 15 different locations across the surface. b) C1*s* peak corresponding to graphene sp^2 bonding and SiC carbon bonding. No extra peaks are visible. c) B1*s* peak centered around binding energy 191.5 eV. d) N1*s* peak centers around binding energy 398.9 eV.

4.4.2.3 Boron Nitride Conductivity

In order to be used as a gate dielectric, the CVD grown boron nitride has to be a very good insulator. I-AFM was used to measure the conductivity difference between graphene and as grown BN on one multilayer epitaxial graphene after BN growth. The sample was placed on a metal chunk with a piece of thin metal clipped on to the sample

surface. The sample surface, metal clip, metal chunk and I-AFM stage were connected as one conduction loop, which applied a dc bias voltage on the sample. The I-AFM conductive tip was scanning on the sample surface and it measured the current flow between the tip and sample. Since the contact resistance between the metal clip and the sample surface and that between the I-AFM tip and the sample surface were unknown, the resistances obtained from I-AFM I-V scan gave information about upper limits of the real material resistance. By scanning across multiple regions on the sample surface, an area where graphene with boron nitride on (EG-BN) and graphene with boron nitride peeled (EG) both existed was chosen to scan carefully. Figure 4.6 is the I-AFM result for a 2 μm × 2 μm area with EG-BN and EG in the same picture. The dc voltage applied on the sample was 100 mV. Figure 4.6 a) is the topography of the entire area. It shows that there are two types of surface material. Figure 4.6 b) is its corresponding conduction map. The thickness for BN was measured to be 5nm. It shows detectable current (~150 nA) on EG area and negligible current (< 30 pA) on EG-BN area. Figure 4.6 c) and e) are the 500 nm scan on EG and EG-BN area respectively, as outlined in Figure 4.6 a). The surface roughness obtained from such topography of EG is 0.09 nm, which is comparable to a newly prepared epitaxial graphene sample. The surface roughness of EG-BN is 0.2 nm, a much smaller value compared to 3 nm reported in another article ((Liu, et al., 2011)). Figure 4.6 d) and f) are the corresponding conduction map. Figure 4.6 f) clearly shows negligibly small current (<30 pA) even at scan area as small as 500 nm. Compared to the good conduction in the graphene region, the resistance on EG-BN area was more than 3 GΩ. Therefore, I-AFM result confirms BN grown on the epitaxial graphene sample is a very good insulator.

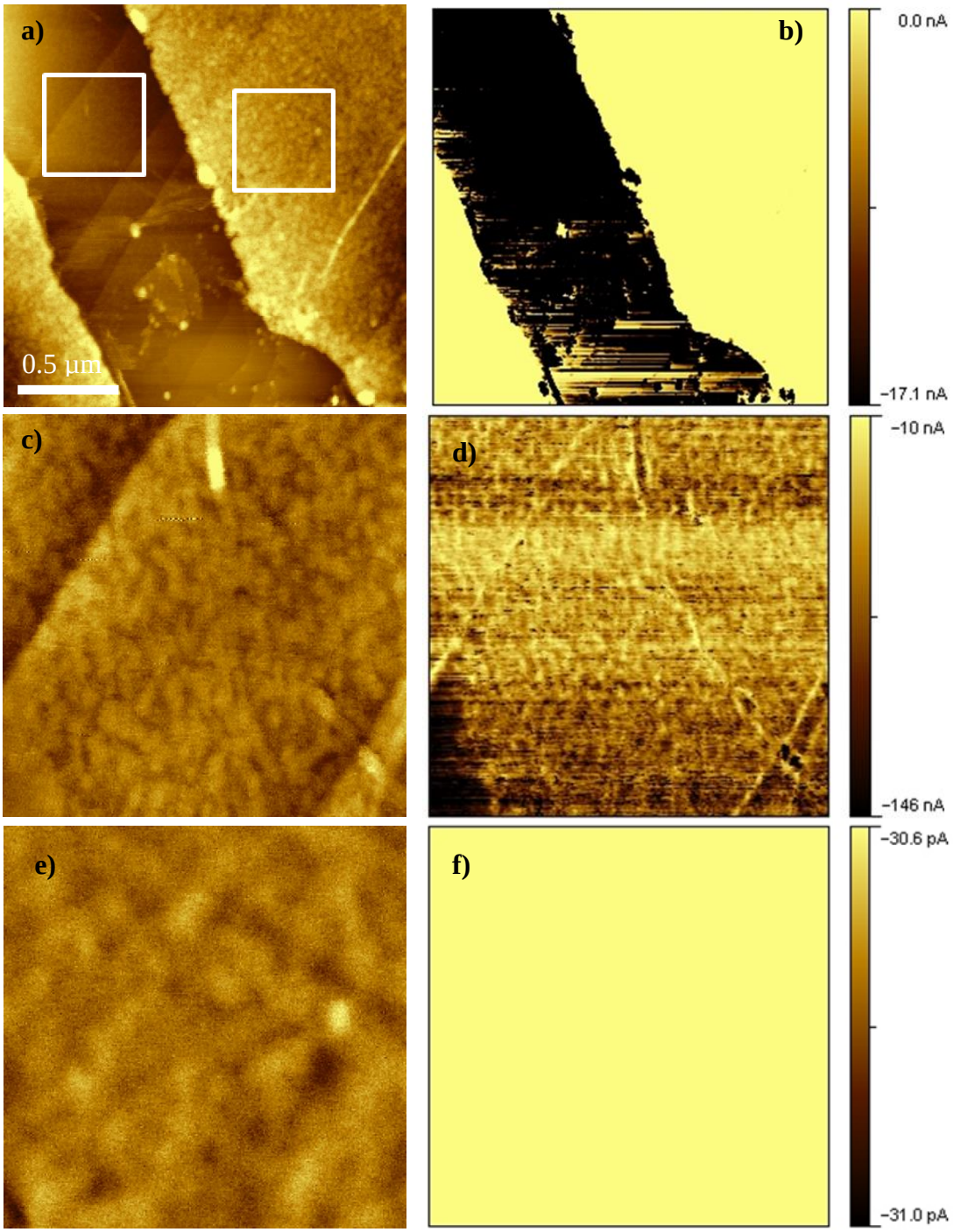

Figure 4.6: I-AFM topography and conduction map for BN on top of epitaxial graphene. V_{ac}=100 mV is being applied to the substrate. a) Surface morphology for BN on EG with partial EG area exposed for comparison. c) 500 nm scan on the graphene region with surface roughness = 0.09 nm. e) 500 nm scan on the BN region surface with surface roughness =0.2nm. V_{dc}=100 mV. b), d) and e) are the corresponding conduction maps. Clearly, the graphene region has very good conduction while the graphene region covered by BN shows no conduction at all. Scale bar: 0.5 µm.

4.4.3 Multilayer Graphene Transistor with a Boron Nitride Dielectric

4.4.3.1 Amorphous Carbon Buffer Layer

After demonstrating that the as-grown BN is insulating enough to potentially work as a gate dielectric, we investigated how to deposit a metallic gate on BN. As grown BN has a thickness of 5 nm. A metallic layer on BN can induce a large tension in boron nitride and may cause dielectric distortion (Park, et al., 2011). In case of pinhole defects in boron nitride, gate leakage current is inevitable. We have deposited an additional layer of amorphous carbon on boron nitride before the metallic gate (Cr/Au (5 nm/40 nm)) deposition to relieve the stress caused by metallic contacts. A carbon coater (Cressington 108A) was used to deposit amorphous carbon. A high current was passed through 2 carbon rods inside the vacuum chamber. An arc occurred at the point where the 2 rods touch and resulted in a sputtering-type deposition of carbon. 8nm amorphous carbon was obtained after 10s deposition. As shown in Figure 4.7 a), the amorphous carbon layer acts as a buffer mesh between the dielectric and metal contact. In the meantime, experiment on using multilayer graphene as a gate electrode to improve gate dielectric reliability has also been reported (Misra, et al., 2012).

I-V characteristics on devices with and without an amorphous carbon buffer layer were measured. Epitaxial graphene on the C-face with boron nitride grown all over surface was prepared. Figure 4.7 b) is the I-V scan between a pair of contacts without carbon buffer. The contacts were 200 μm × 200 μm in size and separated by 300 μm. A linear I-V relationship was observed. The sheet resistivity is 4.5 kΩ/sq, which is comparable to graphene sheet resistivity. This indicates we are actually measuring the graphene resistance underneath BN. The conduction could possibly be through the channel created by the pressure of metal contact on thin dielectric regions. In order to verify this assumption, another device with amorphous carbon buffer was prepared. The contacts were 400 μm × 100 μm in size and separated by 80 μm. Metal contacts made of

Cr/Au were deposited on top of 8 nm amorphous carbon layer. As Fig 4.7 c) showing, the I-V curve is characteristic of a thin dielectric. The resistance between -0.4 V and 0.4 V is about 7 GΩ, consistent with that obtained from I-AFM (3 GΩ).

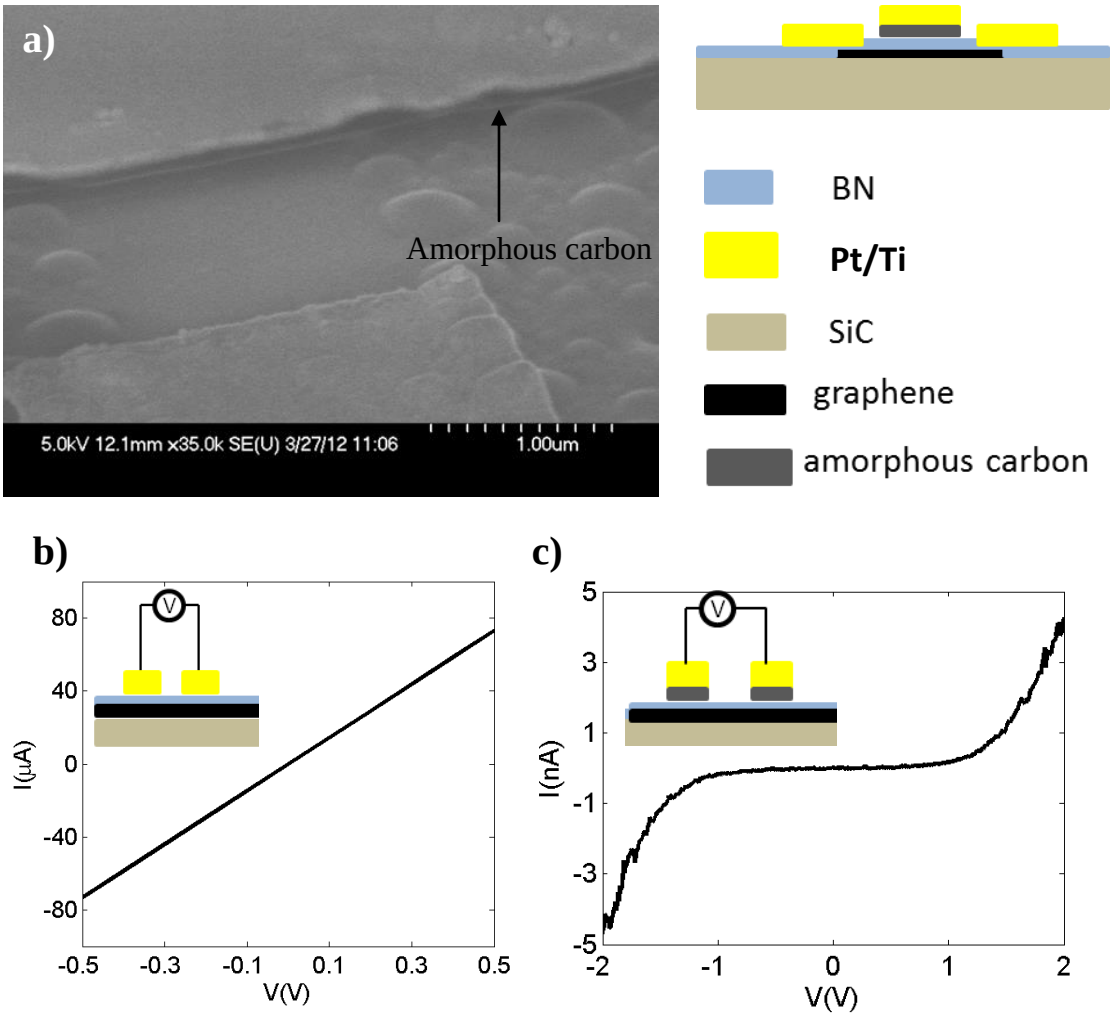

Figure 4.7: Amorphous carbon as a gate dielectric buffer layer. a) SEM image for a few layer graphene FET with amorphous carbon as a gate dielectric buffer layer. b) Linear I-V on metal contact pads on top of the BN-EG stack without an amorphous carbon layer. c) Nonlinear I-V response on metal contact pads on top of BN-EG stack with an amorphous carbon layer in-between.

Note that for metal contact as small as several μm^2, good insulation between contacts without amorphous carbon buffer has been seen on some samples. It is probably because the small contact size reduces the possibility of dielectric defects present underneath metal, however, to improve the yield of working devices and make use of the

strain-relieving property of the amorphous carbon buffer layer, the carbon buffer was kept for all devices.

4.4.3.2 Multilayer Epitaxial Graphene FET

A multilayer epitaxial graphene FET with a boron nitride gate dielectric was made as follows: a) Multilayer graphene was grown on the C-face of SiC with pre-patterned alignment marks; b) a graphene Hall bar structure was fabricated; c) Pt/Ti (30 nm/2.5 nm) was deposited as contact metal; d) Boron nitride was grown on the sample by ambient pressure chemical vapor deposition method; e) Amorphous C/Cr/Au (8 nm/5 nm/40 nm) was deposited as gate contact. Figure 4.8 a) is an optical image for such a device. Pt was chosen as the metal for voltage/current contacts because of its high melting point (1772 °C). A very thin Ti capping layer was used to prevent Pt erosion from gas flow during the BN growth. This metal layer maintained Ohmic contact with graphene after BN growth. Figure 4.8 b) is an I-V scan between a pair of voltage contacts. A linear Ohmic behavior was observed.

Graphene resistance versus gate voltage at room temperature is demonstrated in Figure 4.8 d). Gate voltage was limited in a certain range so that no significant leakage current was detected (below 6 nA), as shown in Figure 4.8 c). A 15% resistance change was observed within the gate working range. The maximum resistance point was found at V_g= - 0.3 V, which indicates the sample is electron doped. Since graphene in ambient environment is usually hole doped due to air, water, and other contaminants. This negative doping supports a clean EG/GN interface. The small resistance change with gate voltage was mostly due to the multilayer graphene (~5 layers) channel. For multilayer graphene, the conduction is dominated by the layer closest to SiC substrate. The top gate voltage cannot change the carrier density of the interface conduction layer because of the graphene layer screening (Kedzierski, 2008; Li, et al., 2009b). In conclusion, the

fabrication of a multilayer epitaxial graphene FET with boron nitride directly grown on MEG as dielectric and its FET operation was demonstrated.

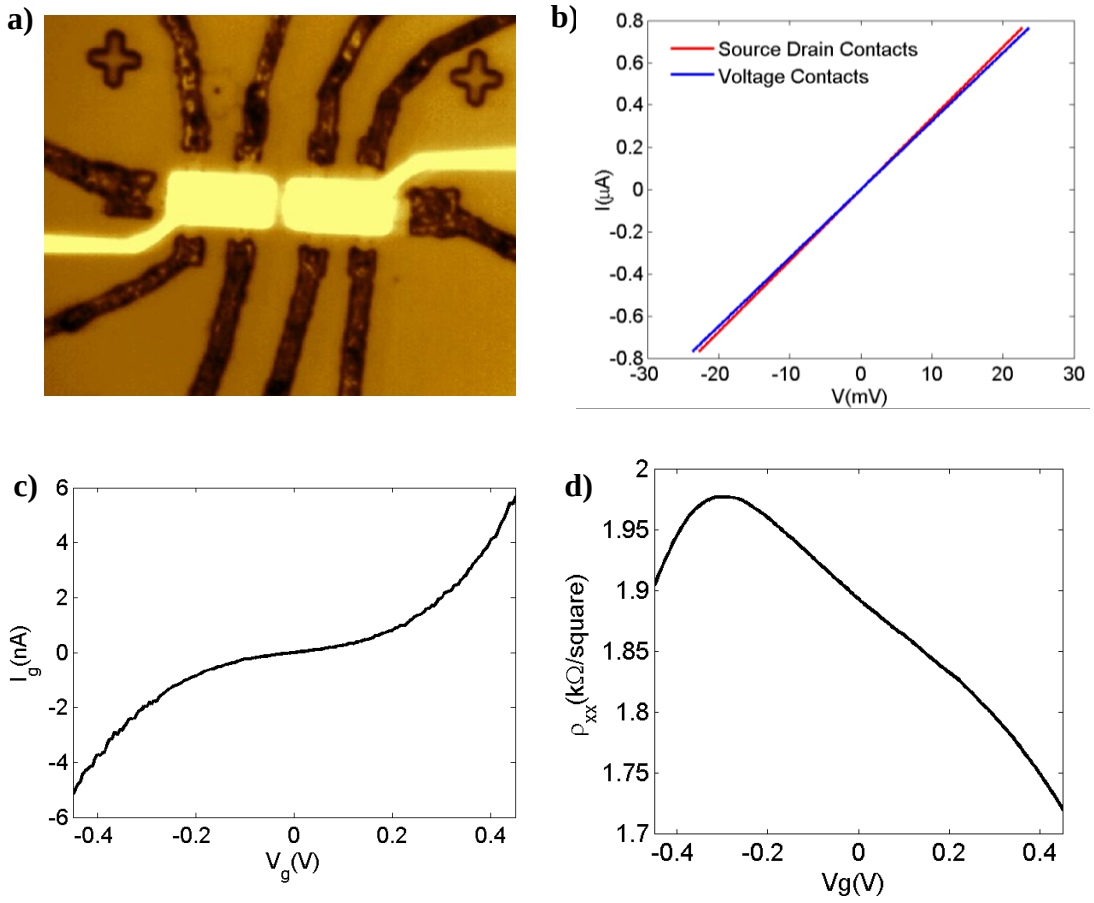

Figure 4.8: Multilayer epitaxial graphene FET characteristics with a BN dielectric. a) Optical image of the final device. Five-layer epitaxial graphene is the conduction channel. The current and voltage contacts were made of Pt/Ti (30 nm/2.5 nm). The top gate was made of amorphous C/Cr/Au (8 nm/5 nm/40 nm) over as-grown boron nitride. b) Ohmic behavior of the contacts after high temperature annealing. c) No significant leakage current within the gate working range is observed. d) FET characteristics. Channel resistivity versus gate voltage measured at room temperature. Within the gate sweeping range, the sample resistance passes the maximum resistance point.

CHAPTER 5

SCHOTTKY BARRIER TRANSISTOR OF 2DEG ON THE C-FACE OF SEMI-INSULATING SILICON CARBIDE

5.1 Introduction

A single layer epitaxial graphene FET has been demonstrated in the previous chapter. It maintains very high carrier mobilities after the top gate deposition and has a current on-off ratio about 13 (Hu, et al., 2012). A FET with excellent switching capacity is desired for logic circuits. One alternative approach is to incorporate the conduction properties of multilayer epitaxial graphene with the SiC substrate to make a Schottky barrier transistor. It is shown that decreasing the semiconductor on insulator and gate oxide thicknesses leads to an increased screening of the potential inside the channel, which in turn yields highly transparent Schottky barriers (Knoch, et al., 2007). An ultrathin body (less than 3nm in thickness) or essentially a two-dimensional electron gas channel material will be ideal to optimize the Schottky barrier MOSFET performance (Knoch, et al., 2002; Knoch, et al., 2006). SiC develops variant surface reconstruction with different properties upon high temperature annealing (Starke, 2002). A Schottky barrier transistor using the silicon oxide/SiC interface as channel and multilayer epitaxial graphene as contacts will be demonstrated in this Chapter. A thin layer of silicon oxide was formed on the high temperature annealed C-face SiC. The accumulating electrons in the interface of SiC/silicate behave as the conduction channel of the Schottky barrier transistor. A back-to-back Schottky diodes model was applied to discuss the I-V.

5.2 High Temperature Annealed C-face SiC

Before reaching graphitization temperature, SiC develops different surface reconstruction depending on the furnace condition and the annealing temperature (Bernhardt, et al., 1999b; Starke, 2002). In this work, the semi-insulating 6H-SiC (II-VI Incorporated, vanadium doped) was annealed in the graphite inset of the high vacuum RF furnace (the same furnace for the epitaxial graphene production) at temperature 1450 °C for 7 minutes. This temperature is below the growth temperature of single layer epitaxial graphene on the C-face of SiC (1490 °C). Raman and EFM confirmed no graphene existed after the high temperature annealing. SiC sample treated by this method is referred as 'high temperature annealed C-face SiC' hereafter. The surface reconstruction was further characterized by LEED and XPS to gain insight about the surface material. Below are the experiment results.

5.2.1 LEED

Figure 5.1 compares the LEED patterns of three type of C-face SiC surface. The SiC (1 × 1) spots were calibrated by the LEED of bare SiC sample from the same wafer, circled in white in Figure 5.1. Figure 5.1 a) is a typical LEED pattern of a C-face multilayer epitaxial graphene sample. Weak (1 × 1) SiC spots are visible while the bright arcs in the sphere indicate the existence of rotationally stacking multilayer graphene. The LEED of the high temperature annealed C-face SiC surface demonstrates a $\sqrt{3}\times\sqrt{3}R30°$ pattern, as seen in Figure 5.1 b) and c). Figure 5.1 b) is the LEED pattern of the C-face SiC annealed at 1450 °C. The sample in Figure 5.1 c) was prepared differently. A C-face multilayer epitaxial graphene sample was grown first. Arrays of MEG were patterned with EBL and etched away by oxygen RIE plasma. Then the sample was annealed at

1450 °C. In the LEED pattern of this sample (Figure 5.1c)), the arc shape from MEG and the $\sqrt{3}\times\sqrt{3}R30°$ pattern are both present. Figure 5.1 d) is the sketch showing how the $\sqrt{3}\times\sqrt{3}R30°$ pattern relates to the SiC (1× 1) spots. Both Figure 5.1 b) and c) confirm the existence of the $\sqrt{3}\times\sqrt{3}R30°$ reconstruction on the C-face of SiC after the high temperature annealing in high vacuum furnace.

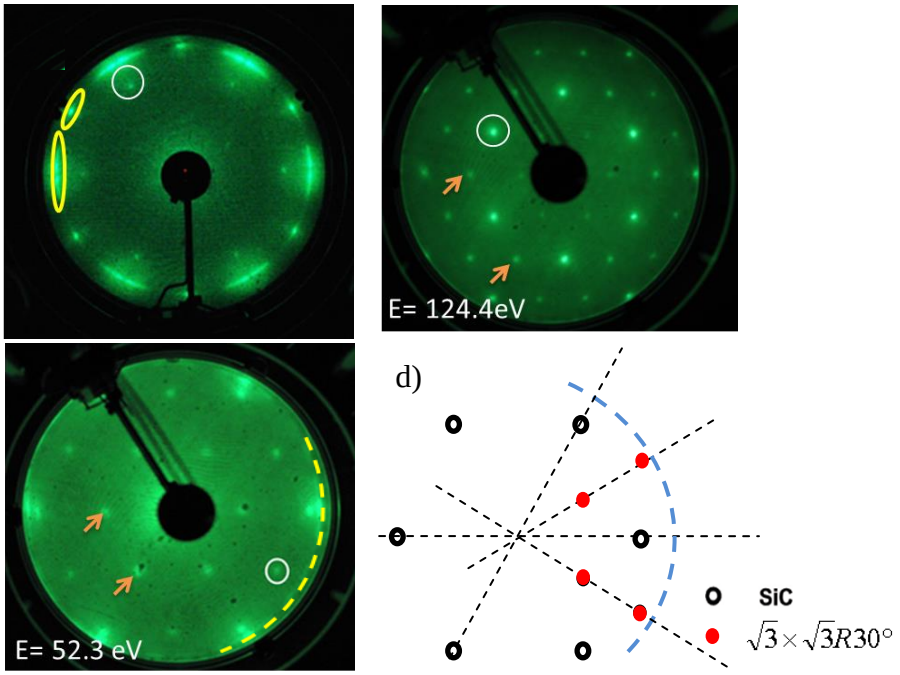

Figure 5.1 LEED pattern of different C-face SiC surface structures. SiC (1×1) spots are circled in white. a) Multilayer epitaxial graphene on C-face. MEG pattern is arc shape. b) C-face SiC annealed at 1450 °C. The $\sqrt{3}\times\sqrt{3}R30°$ pattern is marked by arrows. c) Annealed MEG_SiC arrays. The arcs from MEG and the $\sqrt{3}\times\sqrt{3}R30°$ pattern from the annealed SiC are present. d) Sketch of $\sqrt{3}\times\sqrt{3}R30°$ pattern related to SiC (1×1) spots.

5.2.2 XPS

The chemical elemental composition of the surface material was revealed by the XPS core level spectra. As shown in Figure 5.2 a), the Si2*p* core level spectrum of the annealed C-face SiC with a $\sqrt{3}\times\sqrt{3}R30°$ pattern exhibits an additional peak at 103.6 eV

next to the peak associated with bulk component Si-C bond at 101.8 eV. The energy shift of 103.6-101.8=1.8 eV is consistent with the shift between the Si-C Si2*p* and the oxidation state of the Si atoms in the adlayer Si^{3+} (Hollering, M., et al., 1999). In Figure 5.2 b), the C1*s* spectrum for the high temperature annealed C-face SiC (denoted as SiC/Si_2O_3 in the figure) only has a peak associated with the C-Si bond from SiC. No carbon sp^2 or carbon-oxygen related peak is observed. The XPS spectra confirm the existence of a thin silicon oxide layer (Si_2O_3) on the surface of the high temperature annealed C-face SiC. The $\sqrt{3}\times\sqrt{3}R30°$ pattern corresponds to the SiC/ Si_2O_3 surface.

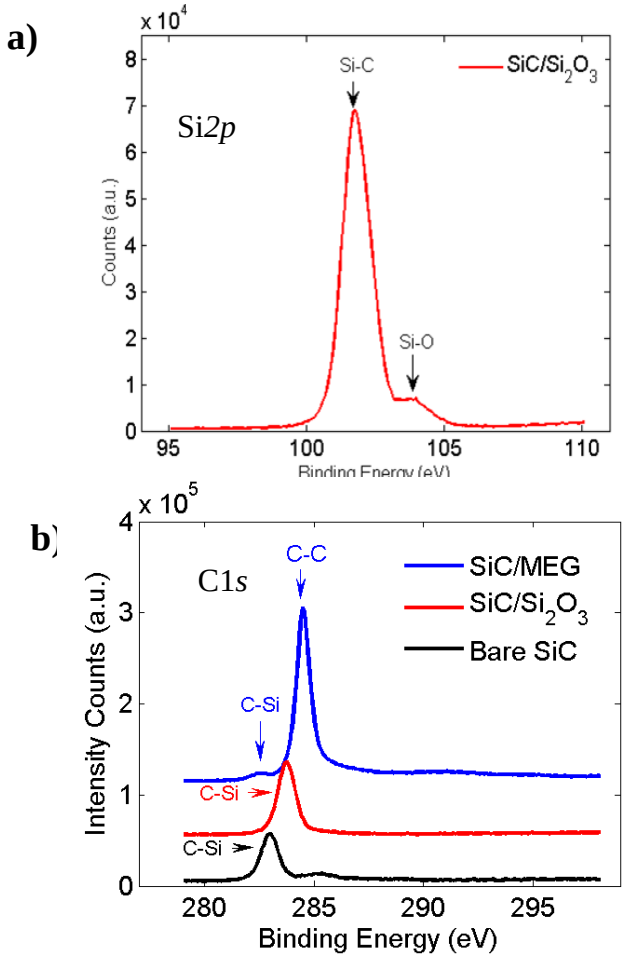

Figure 5.2 a) Si2*p* core level spectrum of high temperaure annealed C-face SiC. The spectrum has two components at 101.8 eV and 103.6 eV associated with bulk Si-C and Si-O. b) C1*s* core level spectra of multilayer epitaxial graphene (up, blue), SiC with Si_2O_3 formation (middle, red), and bare SiC without surface treatment (bottom, black).

5.2.3 Silicate in Literature

A literature search on oxide formed on the C-face of SiC during high temperature thermal treatment yields several papers related to the formation of Si_2O_3 and its surface characterization. A highly ordered ultrathin monolayer silicon oxide was observed on the C-face of SiC by hydrogen plasma or hydrogen flow etching (Starke, et al., 1999; Hoshino, et al., 2004; Bernahardt, et al., 1999). LEED pattern ($\sqrt{3}\times\sqrt{3}R30°$), which was connected to the formation of silicate, was found on the C-face of SiC annealed in 1 atm argon at 1400 °C (Luxmi, 2010, et al.). The silicate is believed to form during the annealing process in Ar (purity 99.999%). The silicate surface was found to be atomically flat and well ordered by STM characterization (Shirasawa, et al., 2007). Refer to Appendix C for more information about silicate in literature.

5.3 SiC/Si_2O_3 Interface

5.3.1 Interface Band Bending

Figure 5.2 b) is the C1*s* core level spectra for Si_2O_3 on the C-face of SiC (SiC/Si_2O_3 for short) (red, middle), MEG on the C-face of SiC (SiC/MEG for short) (blue, up), and bare C-face SiC (only solvent cleaning, no surface treatment, with native disordered oxide) (black, bottom). The C1*s* peaks associated with the bulk C-Si bond clearly locate at different positions for the three type of surface states, which indicates a different band bending at the interface. The C1*s* associated with bulk C-Si bond has a binding energy at 283.8 eV for SiC/Si_2O_3, 282.5 eV for MEG on the C-face, and 282.6 eV for bare C-face SiC.

The band bending voltage in the interface can be derived from the C1*s* binding energy (E_{C1s}) associated with the C-Si bond. The energy difference between the bulk C1*s* core level and the valence band maximum E_v for 6H-SiC was determined to be 281.0±0.1 eV (Seyller, et al., 2006). The binding energies determined by XPS are referenced to the surface Fermi level. The position of the Fermi level at the surface E_F^S with respect to the valence band maximum is given by $E_F^S - E_V^s = E_{C1s} - 281.0eV$.

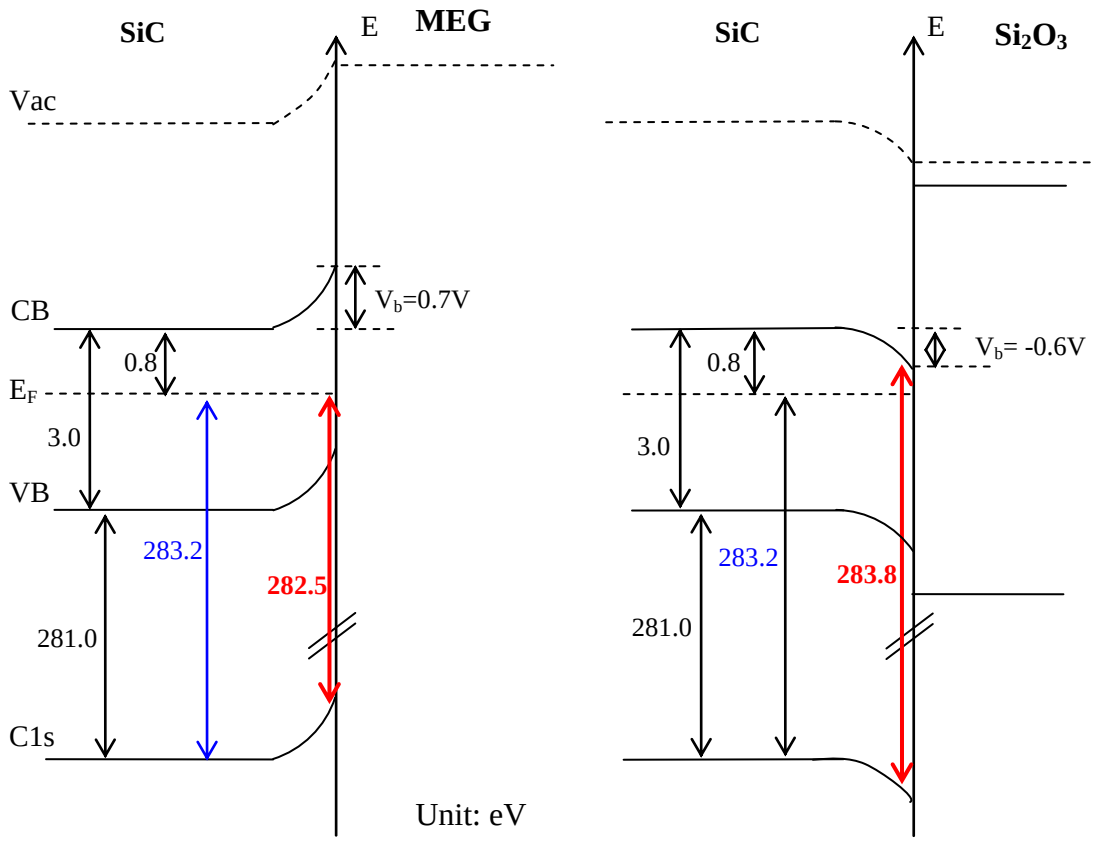

Figure 5.3: Band diagram for SiC/MEG interface and SiC/Si_2O_3 interface. Based on the XPS C1*s* position associated with C-Si bond in XPS, the interface band bending voltage is determined to be upward 0.7 V for 6H-SiC/MEG interface and downward 0.6 V for SiC/Si_2O_3 interface.

The Fermi energy level lies 0.8 eV below conduction band, which can be verified by the supplier's data sheet, the charge neutral condition and the bulk resistivity (Check Appendix D for more details). Considering the 6H-SiC band gap *Eg*=3.0 eV, we have

$E_F^{bulk} - E_V^{bulk} = 2.2eV$. The band bending voltage V_b at the interface is the difference between the bulk and the surface valence band position, *i.e.*, $eV_b = E_V^{S} - E_V^{bulk}$. In the thermal equilibrium state, Fermi level is constant everywhere in the system. The band bending voltage can be derived from

$$eV_b = (E_{C1s} - 281.0) - (E_F^{bulk} - E_V^{bulk}) = (E_{C1s} - 281.0eV) - 2.2eV .$$

Based on the measured binding energy of the C-Si C1*s* peak, the band bending voltage for the semi-insulating 6H-SiC and multilayer graphene interface is 0.7 ± 0.1 V with SiC band bent upwards. The band bending voltage for the semi-insulating 6H-SiC and Si_2O_3 interface is 0.6 ± 0.1 V with SiC band bent downwards. The band bending voltage for the as-received semi-insulating C-face 6H-SiC surface (SiC/disordered oxide interface) is 0.6 ± 0.1 V with SiC band bent upwards. Figure 5.3 is the schematic band bending diagram for the SiC/Si_2O_3 (a) and SiC/MEG (b) interface.

5.3.2 Two-dimensional Electron Gas

This 0.6 V of band bending downward in the SiC/Si_2O_3 interface brings the SiC conduction closer to the Fermi level, which leads to the accumulation of electrons in the conduction band. The band bending voltage in SiC/Si_2O_3 interface obtained from the XPS experiment data can also be reproduced with numerical calculations of the Schrodinger equation and the Poisson equation by adjusting the density of interface states. The calculations with parameters are summarized in Appendix E. Here is a simple picture to explain how the density of interface states can affect the band bending at the SiC/Si_2O_3 interface.

There are five sources of charge at the SiC/Si_2O_3 interface: positive bound charge from the spontaneous polarization $\rho_b = -\nabla \cdot P_0$, positively ionized nitrogen donors ρ_D, negatively charged ionized vanadium acceptors ρ_A, interface states ρ_{gs}, and free carriers ρ_χ. P_0 is inherent to the hexagonal stacking of 6H-SiC (Qteish, et al., 1992; Lu, et al., 2009). This charge is calculated to be 5.9×10^{12} cm^{-2} (Qteish, et al., 1992b) and measured indirectly to be 3×10^{12} cm^{-2} (Lu, et al., 2009). Interface states ρ_{gs} is determined by $D_{gs} \times (E_F\text{-}E_{CNL})$, where D_{gs} is the density of interface states and E_{CNL} is the charge neutrality level (CNL). In the 6H-SiC bulk, the CNL lies 1.57 eV below the conduction band minimum (van Elsbergen, et al., 1996; Brudnyi, et al., 2012), which is 0.77 eV below the Fermi level in our case. The interface states is negatively charged if the surface CNL is below the Fermi level (Robertson, et al., 2006). At the interface, $\rho_{gs} = D_{gs} \times (0.77\ eV\text{-}V_b)$ (V_b is the surface band bending voltage with "+" sign for bending upward). ρ_A, ρ_D, ρ_χ are negligibly small compared to ρ_b and ρ_{gs}. Therefore in the simple picture, $\rho_b = \rho_{gs}$. In the case of band bending downward (0.6 eV), 5.9×10^{12} cm^{-2} $=\rho_b= D_{gs} \times (0.77\ eV\text{-}(-0.6\ eV))$, which gives an approximately $D_{gs}=4.3\times10^{12}$ $eV^{-1}cm^{-2}$. It is close to the numerical calculation result $D_{gs}=3.7\times10^{12}\ eV^{-1}cm^{-2}$ (Appendix E). This explanation also implies the correlation between the density of interface states and band bending voltage (magnitude and direction).

Based on the value of conduction band bending voltage and the Fermi level position, the sheet charge density n_{2D} in the C-face SiC/Si_2O_3 interface is given by

$$n_{2D} = Mc\frac{m_t}{\pi\hbar^2}k_BTIn\left(1+e^{\frac{E_F-E_0}{k_BT}}\right) \cong Mc\frac{m_t}{\pi\hbar^2}k_BTe^{\frac{E_F-E_0}{k_BT}} \qquad (5\text{-}1)$$

where m_t is the in-plane effective mass in SiC (currently taken as m_t = 0.42 m_0, m_0 is the rest mass of electron) and E_0 is the energy of the lowest energy confined interface state. $E_0 = E_C - V_b$ (V_b is the band bending voltage as discussed previously). The approximation holds when $E_0 - E_F >> k_B T$. For a band bending voltage ranging from 0.58 V to 0.64 V, the free charge density in the 2D conduction channel is around 1.0×10^{10} cm^{-2}.

5.4 Schottky Barrier Transistor on C-face 6H-SiC

To use the two-dimensional electron gas properties in the C-face semi-insulating 6H-SiC/Si_2O_3 interface, a metallic-2DEG-metallic Schottky barrier transistor structure was proposed and realized in this dissertation by using a multiple-step annealing process.

5.4.1 Fabrication

The SiC wafer was CMP semi-insulating 6H-SiC purchased from II-VI Incorporated, which was vanadium (V) doped. Different from the semiconducting wafers which use the native defects to reduce conductivity, V doped wafer stays highly insulating after the high temperature annealing. This wafer ensures no conduction is passing though the bulk SiC in device even after multiple steps of high temperature annealing.

The metallic-2DEG-metallic structure was made by multiple patterning, etching and annealing steps. Multilayer epitaxial graphene was grown on the C-face of 6H-SiC. Epitaxial graphene was patterned with the negative e-beam resist maN-2403 to define the areas of graphene contact. The sample was developed in the maN-2403 developer MIF-319. Non-protected area of graphene was etched away with oxygen RIE plasma. The

sample was loaded into the graphite furnace and annealed at a temperature right below graphitization temperature (1450 °C). The sample was characterized with EFM and Raman to confirm that no graphene had grown inside the channel. Then the sample was patterned with maN-2403 again and the area outside the MEG_channel_MEG was etched to define the active device area. After that, the sample was patterned with PMMA for metal contacts deposition. Cr/Au (5 nm/45 nm) was deposited as the extended metal leads on the top of MEG stack. This design creates a clean contact between the multilayer epitaxial graphene and SiC/Si_2O_3. In the end, 20 nm aluminum oxide was deposited on the structure as a gate dielectric with the same method described in Chapter 4.

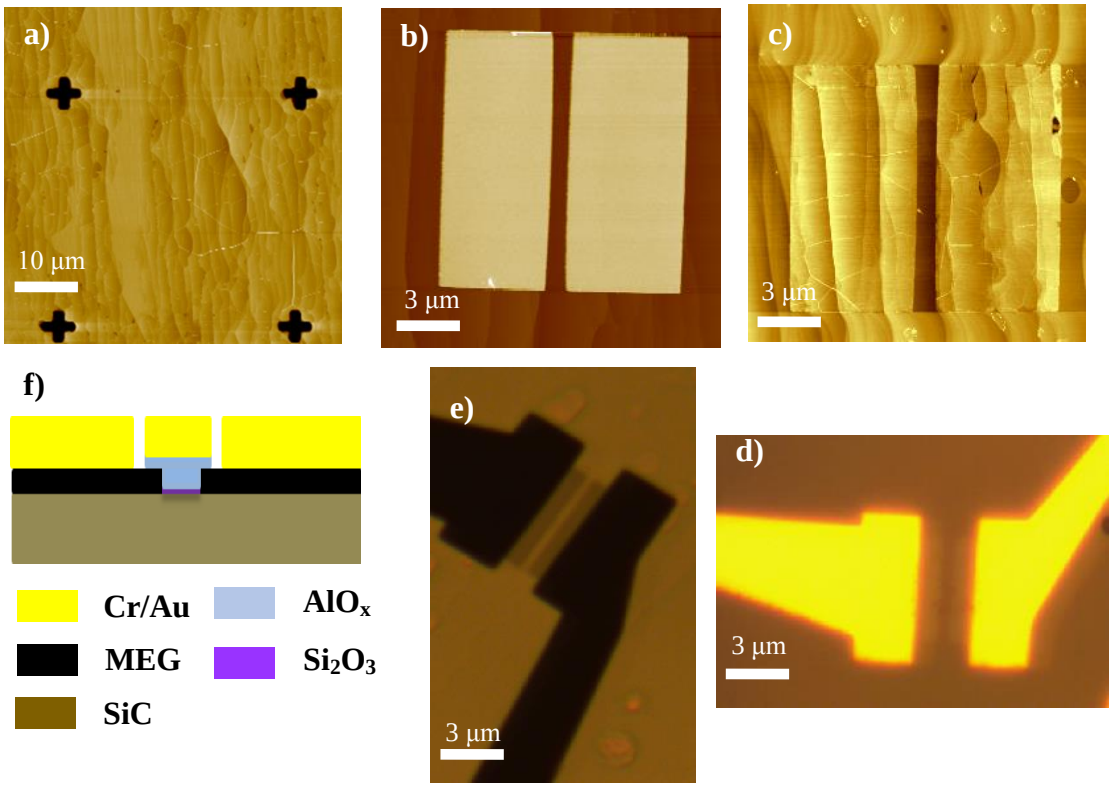

Figure 5.4 Schottky barrier transistor with MEG contacts on the C-face of SiC. Scale bar: a) 10 µm; b), c), d), e) 3 µm. a) AFM topography of MEG on the C-face. b) AFM topography of maN-2403 masks on MEG with the rest of graphene etched by oxygen plasma. c) AFM topography of MEG_channel_MEG structure after high temperature annealing. d) and e) are optical images for the finished devices with Cr/Au metal contact leads on multilayer graphene. f) Schematic side view of the gated device.

Figure 5.4 displays the images corresponding to different stages of the sample preparation. Figure 5.4 a) is the multilayer epitaxial graphene grown on the C-face with the SiC alignment marks. Figure 5.4 b) is the 150 nm thick maN-2403 mask on MEG after the oxygen RIE plasma etching. Graphene remains only underneath the maN-2403. Figure 5.4 c) is the AFM topography for a structure after annealing. Figure 5.4 d) and e) are the optical images for two finished devices with front reflective light and back transmitted light. Figure f) is the schematic side view of the gated device.

5.4.2 Transistor Characteristics

One gated Schottky barrier transistor was fabricated with the same method described in ξ 5.4.1. The channel width was W=10 μm and length was L=900 nm. The device was measured at room temperature. Figure 5.5 a) is the device current-voltage characteristic at zero gate bias. The Figure 5.5 b) is the schematic diagram for the electrical measurement set up. The dc power supply for the source/drain was common-grounded with the dc power supply for the top gate. This circuit wiring induced local gate voltage difference at each diode, i.e., one diode experienced a local gate voltage V_g-$V_{sd,}$ while the other diode experienced a local gate voltage Vg. This asymmetry became significant at high source/drain bias voltage, which led to the asymmetry for the I-V characteristics at high bias voltage. Considering the band bending voltage at the SiC/MEG and SiC/Si_2O_3 interface, the device can be modeled with back-to-back Schottky diodes connected with a conduction channel. The band diagram at different source/drain voltages is depicted in Figure 5.5 c).

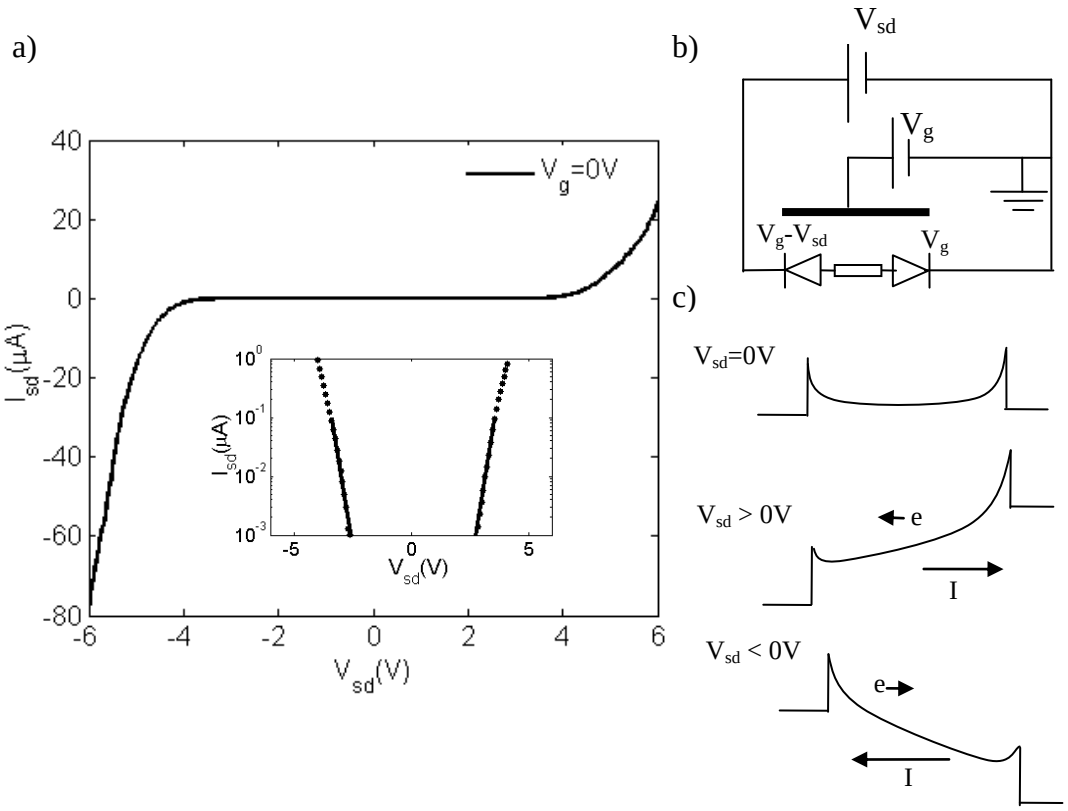

Figure 5.5 a) The current-voltage characteristic at zero gate voltage for the Schottky barrier transistor on the C-face of 6H-SiC. (W=10 μm). The inset is the data fitting at the small source/drain current region with back-to-back Schottky diodes model. b) Schematic diagram for the measurement wiring; c) Band diagram for back-to-back Schottky diodes at different source/drain bias.

Figure 5.6 are the device I-V characteristic at different gate voltage. The gate voltage was varied from 1 V to 6 V at a step of 1 V. The measured current–voltage characteristics show asymmetrical behavior. At the gate voltage of 6 V and the source/drain bias of -6 V, a current of 45 μA/μm was observed. The on-off ratio of the drain current is larger than 10^6. The sub-threshold swing is $S_{s\text{-}th}$=400 mV/*dec* at V_{sd}= -1.2 V.

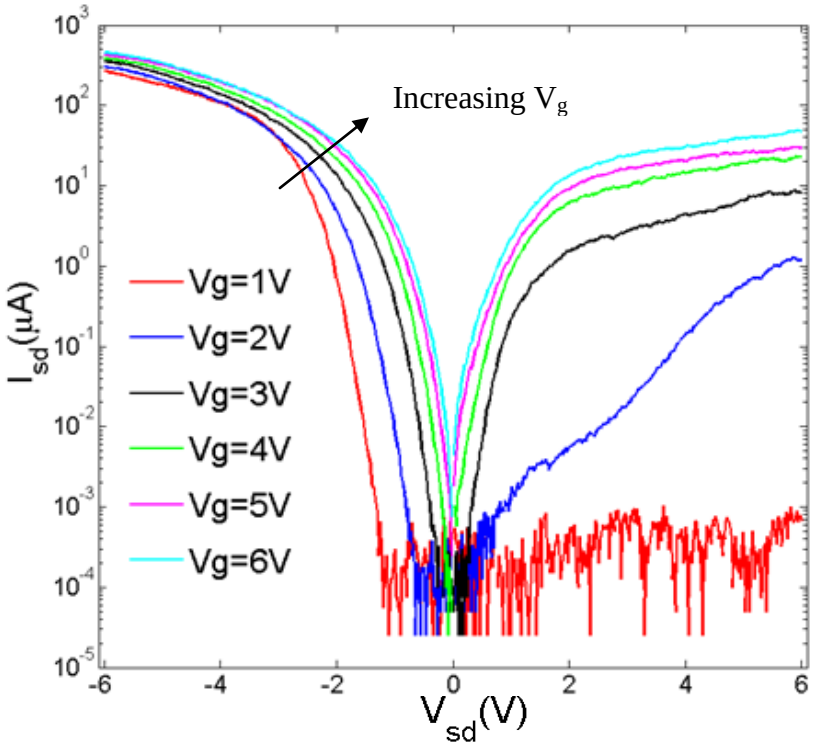

Figure 5.6 Gate dependent current-voltage characteristic for the Schottky barrier transistor on the C-face of semi-insulating 6H-SiC. (L=10 μm). From low to high, the curve represent I-V at a gate voltage equals to 1V, 2 V, 3 V, 4 V, 5 V, 6 V. The arrow indicates the direction of increasing gate voltage.

The analysis of the I-V characteristics of the Schottky barrier transistor requires the thermionic emission model for the Schottky diode. The expression of the I-V characteristic of a single diode by the thermionic-diffusion-theory is (Sze, S.M., 2007)

$$I = A^{*}T^{2}W\exp(-\frac{q\phi_{Bn}}{k_{B}T})\left[\exp(\frac{qV}{k_{B}T})-1\right] \qquad (5\text{-}2)$$

where W is the width of the conduction channel, A^{*} is the 2D effective Richardson constant, q is the electron charge, k_B is the Boltzmann constant, T is temperature, V is the applied voltage, ϕ_{Bn} is the effective barrier height.

For the two-dimensional electron gas, A^{*} can be derived with the same method stated in Sze, S.M., 2007, 3rd, p158, at a fixed temperature,

$$A_{2D}^{*} = \frac{qM_c k_B^{3/2}}{\pi\hbar^2\sqrt{T}}\sqrt{\frac{m_t}{2\pi}} \qquad (5\text{-}3)$$

where Mc is the conduction minima in 6H-SiC, Mc=6, k_B is the Boltzmann constant, $\hbar$ is the reduced Planck constant, m_t is the effective mass in the 2DEG, which is the transverse mass for 6H-SiC, m_t=0.42 m_0, m_0 is the electron rest mass. The 2D-Richardson constant at T=300 K is A_{2D}*=0.02 A/ m K.

When the Schottky diode is not ideal, *e.g*, an ultrathin insulator exists at the metal/semiconductor interface, the I-V characteristic is different from equation (5-2). An ideality factor n taking into account of the insulator influence will be included in the I-V relation. Equation (5-2) need to be replaced with: (Schroder, 2006)

$$I = A^{*}T^{2}W\exp\left(-\frac{q\phi_B^{eff}}{k_B T}\right)\exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \qquad (5\text{-}4)$$

where ϕ_B^{eff} is the effective barrier height at zero source/drain bias voltage.

When the diode is under forward bias, and $qV \geq 3k_B T$, equation (5-4) can be simplified to be

$$I = A^{*}T^{2}W\exp\left(-\frac{q\phi_B^{eff}}{k_B T}\right)\exp\left(\frac{qV}{nkT}\right) \qquad (5\text{-}5)$$

When the diode is under reverse bias, and $q|V| \geq 3k_B T$, equation (5-4) can be simplified to be

$$I = -A^{*}T^{2}W\exp\left(-\frac{q\phi_B^{eff}}{k_B T}\right)\exp\left(\frac{qV}{nkT}\right)\exp\left(-\frac{qV}{kT}\right) \qquad (5\text{-}6)$$

The Schottky barrier transistor is composed of two Schottky diodes and a conduction channel, which satisfies the following relation:

$$V = V_1 + V_2 + V_3 \qquad (5\text{-}7)$$

where V is the total voltage in the circuit, V_1 is the voltage drop on the reverse diode, V_2 is the voltage drop on the forward diode and V_3 is the voltage drop on the channel.

The I-V_1 of the reverse diode satisfies the relation of equation (5-6) with V= -V_1, and the I-V_2 of the forward diode satisfies the relation of equation (5-5) with V= V_2.

Rewriting equation (5-5) and equation (5-6) in terms of current,

$$V_1 = \frac{n_1 kT}{q(n_1 - 1))}\left(LnI - LnI_{10}\right) \qquad (5\text{-}8)$$

$$V_2 = \left(\frac{n_2 kT}{q}\right)\left(LnI - LnI_{20}\right) \qquad (5\text{-}9)$$

where $I_{10} = A^* T^2 W \exp\left(-\frac{q\phi_{B1}{}^{eff}}{k_B T}\right)$, $I_{20} = A^* T^2 W \exp\left(-\frac{q\phi_{B2}{}^{eff}}{k_B T}\right)$

By assuming the same Schottky barrier height and ideality factor for both Schottky diodes, $\phi_{B1}{}^{eff} = \phi_{B2}{}^{eff} = \phi_B{}^{eff}$, $n_1 = n_2 = n$, the total voltage for equation (5-7) can be simplified as

$$V_1 + V_2 = \left(LnI - LnI_0\right)\frac{k_B T}{q}\frac{n^2}{n-1} \qquad (5\text{-}10)$$

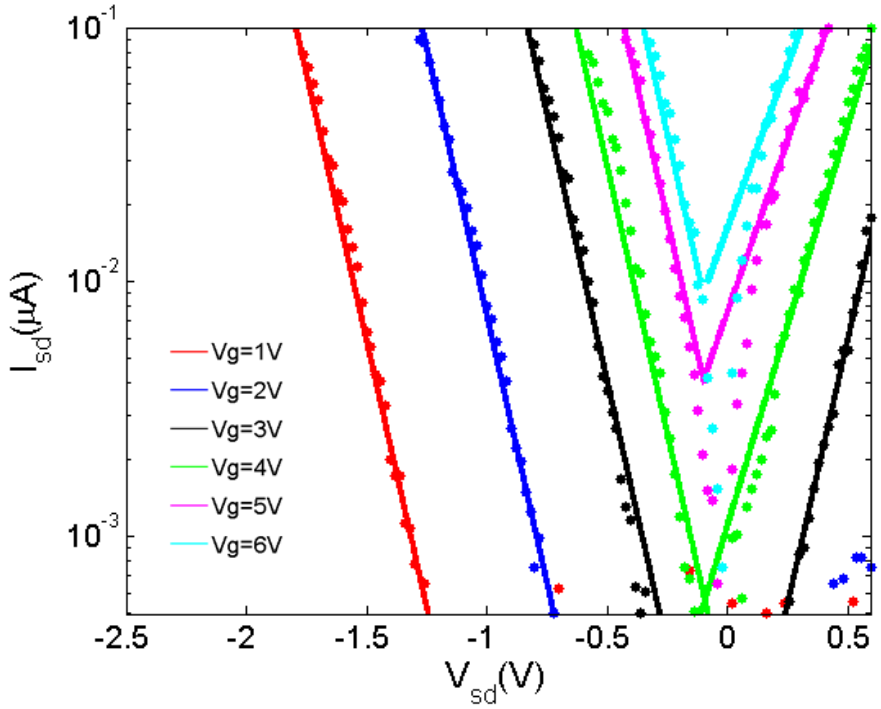

Figure 5.7 Gate dependent current-voltage characteristics curve fitting result (low source/drain current region).

When the current in the channel is small (I < 0.1 μA), the voltage drop across the channel can be neglected. The total voltage in the circuit can be approximately written as:

$$V = V_1 + V_2 \qquad (5\text{-}11)$$

The gate dependent I-V curves in the small source/drain current region can be fitted with the least square method with equation (5-11) at different gate voltages V_g= 0, 1 V, 2 V, 3 V, 4 V, 5 V, 6 V. The fitting parameters are the effective Schottky barrier height at zero source/drain bias ϕ_B^{eff} and the ideality factor *n*. The negative and positive branches were fitted separately considering the asymmetry in the data. Figure 5.5 a) inset and Figure 5.7 are the fitting results versus the experiment data. Table 5.1 lists the Schottky barrier heights at all gate voltages.

Table 5.1 Schottky barrier heights and ideality factors extracted from the data fitting for the current-voltage measurement of small source/drain current region at different gate bias.

Vg	negative bias		positive bias	
	SHB(eV)	Ideality factor	SHB(eV)	Ideality factor
0 V	0.80	1.21	0.84	1.22
1 V	0.76	2.12	N/A	N/A
2 V	0.63	2.00	N/A	N/A
3 V	0.52	2.10	0.51	2.25
4 V	0.47	2.00	0.43	1.33
5 V	0.42	2.01	0.38	1.25
6 V	0.40	2.00	0.36	1.23

There is strong gate dependence with the Schottky barrier height at zero source/drain bias. The barrier lowering effect can be modeled by considering the gate voltage drop across the Schottky barrier and the image force lowering effect. A general form can be used to deduce the reduction in Schottky barrier height (Simmons, 1963)

$$\phi = \phi^0 - \frac{eVx}{s} - \frac{e^2}{16\pi\varepsilon_0\varepsilon_r x} \qquad (5\text{-}12)$$

where ϕ^0 is the zero field Schottky barrier height, s is the Schottky barrier thickness assuming a rectangular barrier shape, V is the external voltage on Schottky barrier(Vg in this case), x is the coordinate inside the barrier. The Schottky barrier height is the minimum value of equation (5-12), which is given by $\left.\frac{d\phi}{dx}\right|_{x_m} = 0$. Therefore the position is

$$x_m = \sqrt{\frac{qs}{16\pi\varepsilon_0\varepsilon_r V}} \qquad (5\text{-}13)$$

Hence the Schottky barrier lowering is given by

$$\phi = \phi^0 - 2\sqrt{\frac{qV}{16\pi\varepsilon_r\varepsilon_0 s}} \qquad (5\text{-}14)$$

By fitting the gate dependence of the effective Schottky barrier height with equation (5-14), the barrier width s and the zero electric field Schottky barrier height ϕ^0 can be obtained. A similar fitting was done by assuming a triangle barrier shape too. Both of the fitting results are shown in Figure 5.8. The fitting assuming a rectangular barrier shape gives a barrier width of 4.2 nm and a barrier height of 0.88 eV. The fitting assuming a triangle barrier shape gives a barrier width of 2 nm and a barrier height of 1.02 eV.

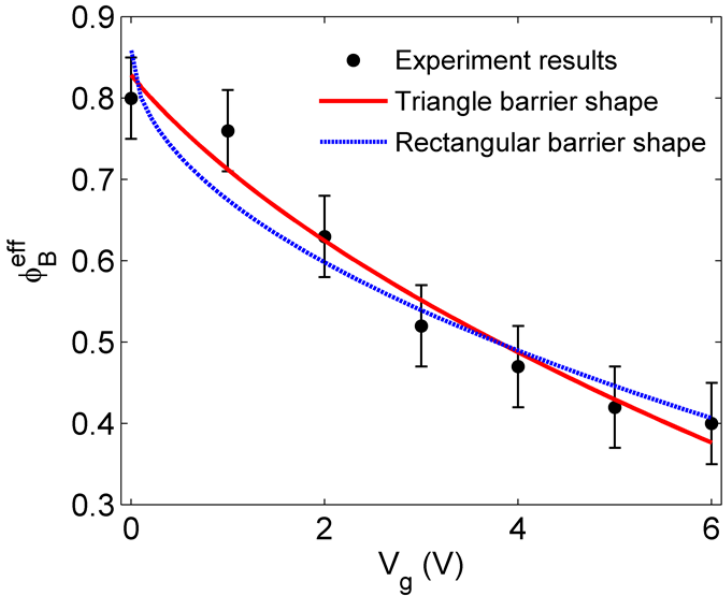

Figure 5.8 The Schottky barrier heights at the zero source/drain bias are lowered by the gate voltage. The experiment data was fitted by assuming a barrier of rectangular shape and a barrier of triangle shape.

To better understand the Schottky barrier height at zero electric field, the electrostatic potential profile across the channel can be calculated with the Poisson equation (Calculated by Jan Kunc)

$$\nabla \varphi = -\rho$$

with boundary condition set as ΔV=0.7 V at the graphene/SiC interface and ΔV= -0.6 V at the Si_2O_3/SiC interface (This was determined by the XPS band bending analysis, as discussed in ξ 5.3.1). A calculated 3D electrostatic potential across the entire channel (MEG_SiC/Si_2O_3 interface_MEG) at zero gate and zero source/drain bias is presented in Figure 5.9 a). A line profile along the current flow is shown in Figure 5.9 b). The line profile reveals a barrier height of 0.87 eV at the junction, where the graphene/SiC edge is connected to the Si_2O_3/SiC plane. If the current flows from graphene into the SiC substrate underneath through the plane, the barrier height is expected to be 0.7+0.8=1.5 eV, where 0.7 V is the band bending between SiC and multilayer graphene and 0.8 V is the distance of SiC Fermi level from the conduction band. This result suggests the current is flowing through the edge of the multilayer epitaxial graphene contacts into the SiC/Si_2O_3 interface.

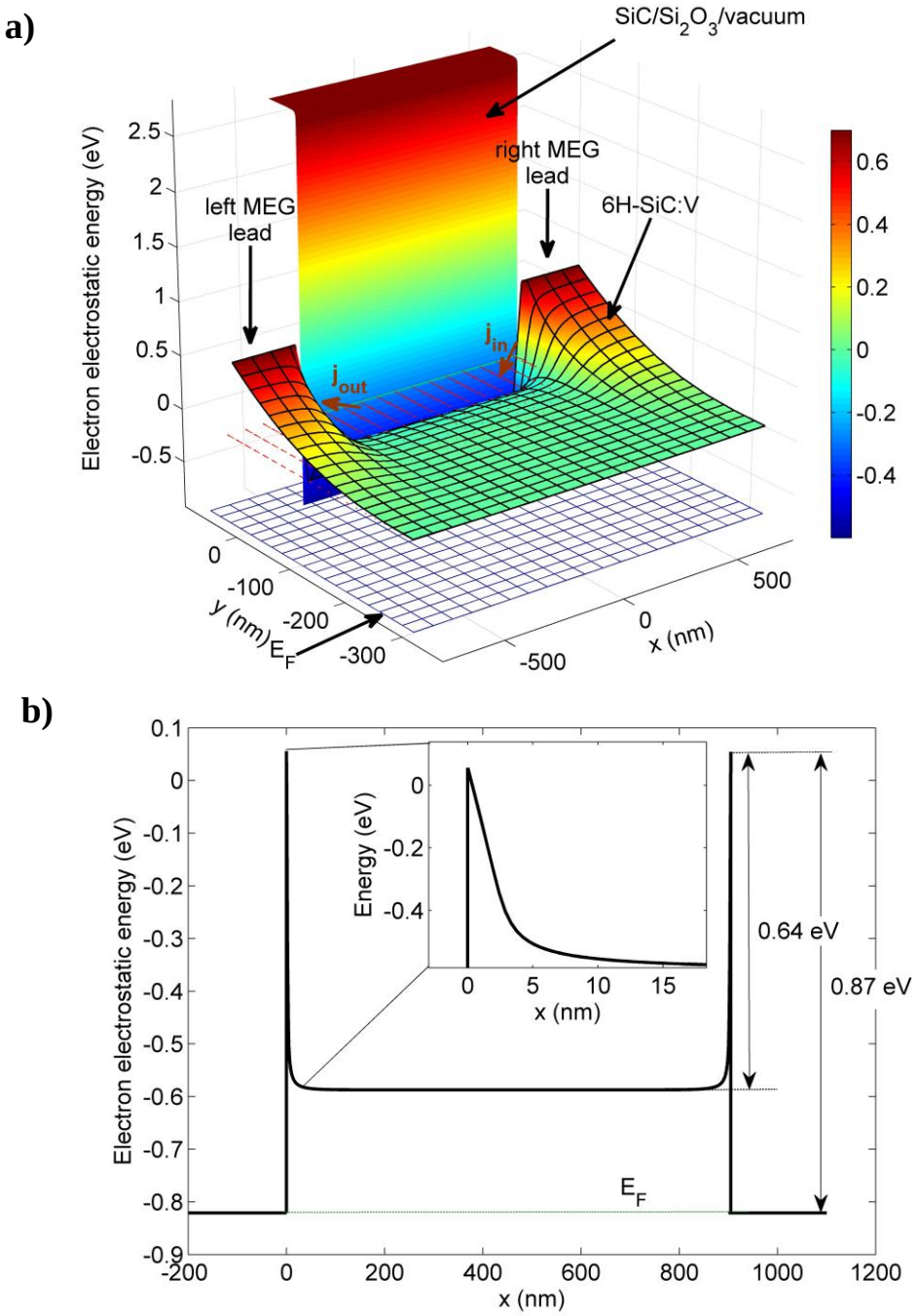

Figure 5.9 a) Numerical calculation result of the electrostatic potential profile across the whole channel (MEG_SiC/Si_2O_3 interface_MEG) at V_g=0 V, V_{sd}=0 V. b) Line profile along the current flow across the channel. A barrier height of 0.87 eV is expected at the zero gate voltage and zero source/drain bias. (Courtesy of Jan Kunc).

At the high source/drain current region, the channel conduction cannot be neglected since the current is significant. To determine the conduction mechanism, I assumed a power law dependence for the channel conduction, which is

$$V_3 = \alpha I^{\beta} \qquad (5\text{-}15)$$

The total voltage drop in the channel is given by equation (5-7). Assuming the voltage-current dependence on diodes and channel as equation (5-8), equation (5-9) and equation (5-15), fit the high source/drain current experiment data with least square method with equation (5-7). With the effective barrier height and ideality factor obtained from the small source/drain current fitting (Table 5.1), the only fitting parameters in the high source/drain current region are α and β. The fitting results are plotted in Figure 5.10 and the fitting parameters are listed in Table 5.2.

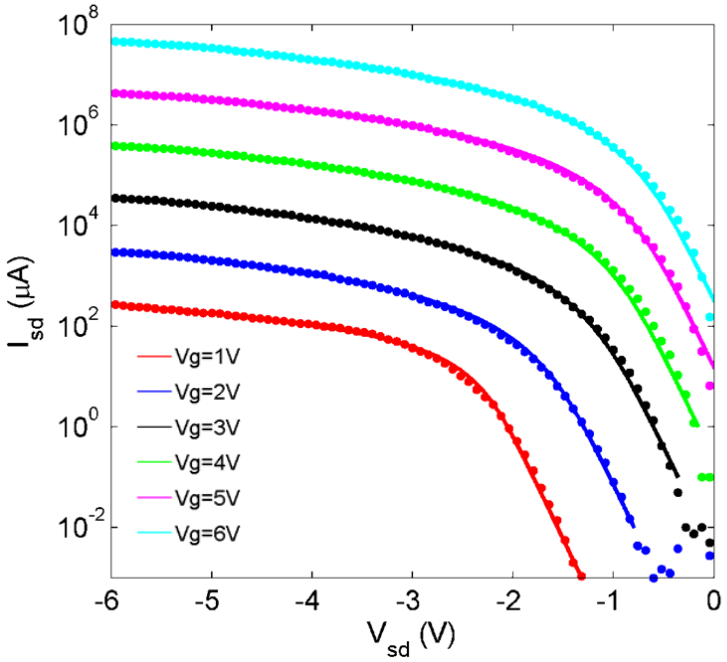

Figure 5.10 Data fitting results for the gate dependent current-voltage characteristics at high source/drain current region. The data are shifted in the y- axis for clarity.

Table 5.2 Fitting parameters for the channel conduction mechanism $V = \alpha I^{\beta}$ for the I-V characteristics of the high source/drain current region at different gate voltages.

Vg	α	β
0V	0.177	0.47
1V	0.020	0.92
2V	0.115	0.61
3V	0.147	0.57
4V	0.130	0.59
5V	0.126	0.59
6V	0.141	0.57

Except for the fitting result of V_g=1 V, which is significantly away from the region of all other data and considered as experimental error, the β value is 0.57±0.05; this corresponds to a current voltage relation $I \propto V^{1.8}$, which is different from a common Ohmic law $I \propto V$. Instead, this indicates a space-charge-limited (SCL) current mechanism.

It is well known that in lightly doped semi-conductor and insulator, SCL current leads to square law I-V characteristics (Rose, 1955). SCL current occurs in situations of mobility dominating transport when the effective carrier concentration is low. The low concentration of carriers creates an extended spatial curvature in electrostatic. By Poisson's equation, a gradient in the electrical field behaves as an additional charge if the thermally generated level of carriers is insufficient, hence a corresponding increase in the current density. When this region extends across the entire current path from source to drain, the device is controlled by SCL current (Wright, 1961). The general approach to solve SCL current is to solve self-consistently Poisson, drift-diffusion and continuity

equations, possibly assuming Shockley-Read-Hall model for trap states. The SCL current in bulk materials assuming carrier scattering has been treated (Mott, et al., 1948), where a square law is present. The I-V characteristic in thin semiconductor layers has been calculated (Geurst, 1966) and an extended analytical analysis was given (Grinberg, et al., 1989).

In the numerical calculation of the I-V characteristics over an extended range of current for the single carrier SCL conduction (Schmidt, et al., 1982), when the carrier concentration over the channel varies slowly, the well-known square law in voltage is not a good approximation. The I-V characteristics depend on the blocking and injecting contact properties, film thickness, trap content and the trap energy level. Power laws from 1.55 to 5.6 are possible based on the trap levels and carrier density distribution over the channel. Hence our fitted result 1.8 is a reasonable value for the SCL conduction.

To estimate the mobility in the channel, the SCL current for a two-dimensional thin film of a lightly doped semiconductor (Grinberg, et al., 1989) is used here.

$$I = \xi \frac{\varepsilon_0 \varepsilon_r \mu}{L^2} W V^2 \qquad (5\text{-}16)$$

where L is the channel length, W is the channel width, ξ is the geometry factor for the contact, which is 0.7 for planar contact configuration, μ is the channel mobility, ε_0 is the vacuum permittivity, and ε_r is the semiconductor permittivity. Using α from the fitting results, the mobilities in this 2DEG channel are in the range of 500~1000 cm^2/Vs. Chandrashekhar (Chandrashekhar, et al., 2007) reported a 2DEG mobility of 700 cm^2/Vs in the interface of C-face 3C/4H-SiC. 3C-SiC has a perfect lattice match to 4H-SiC and the growth is controlled MBE in the case of 3C/4H-SiC interface. The author predicted an increasing mobility of 2DEG to be μ (300 K) = 2000 cm^2/Vs by reducing the

background impurity concentration near the interface to 1×10^{17} cm^{-3}. As for the inversion layer in the C-face of SiC with thermally grown SiO_2, mobilities have been reported around 100 cm^2/Vs (Fukuda, et al., 2004; Harada, et al., 2009; Fronheiser, et al., 2011). The low channel mobility in SiC MOSFET is directly related to the extraordinary high density of interface states in the SiO_2/SiC interface (Ouisse, et al., 1997; Tilak, 2009). A significant increase in channel field effect mobility (284 cm^2/Vs) was observed by the insertion of a 1.2 nm SiO_x in the Al_2O_3/SiC-MOSFET with dry O_2 oxidation (Hino, et al., 2009). Our estimated mobility in the channel lies in the high yet reasonable region of SiC mobilities, which can be attributed to the good interface quality between the semi-insulating SiC and Si_2O_3 after the high temperature annealing.

In conclusion, a Schottky barrier transistor with multilayer epitaxial graphene contacts was fabricated, characterized and analyzed. A two-dimensional electron gas was formed in the interface of SiC and the ordered oxide Si_2O_3 after the high temperature vacuum annealing. It was confirmed by the LEED and XPS experiment and consistent with the numerical calculations based on the SiC semiconductor parameters. Schottky barriers on the edge were observed from the I-V characteristics of the fabricated Schottky barrier transistor with multilayer epitaxial graphene contacts. The change of barrier height can be explained by the source/drain bias voltage and the top gate voltage. The 2DEG in the channel follows a space-charge-limited conduction mechanism. Mobilities in the channel are estimated to be 500 ~ 1000 cm^2/Vs, which corresponds to a good SiC/Si_2O_3 interface.

CHAPTER 6

CONCLUSION

6.1 Summary

To summarize, growth of high quality epitaxial graphene on the C-face of SiC has been demonstrated by the confinement controlled sublimation method. Single layer epitaxial graphene on the C-face was grown and characterized. The single layer characteristic Raman indicator was proposed and evaluated. Unconventional integer quantum Hall effect was observed for the first time on the C-face epitaxial graphene. It unambiguously proved that single layer epitaxial graphene is truly two-dimensional graphene. Exceptionally high mobilities (exceeding 10^4 cm^2/Vs) was measured. It confirms the interaction between graphene and the substrate of C-face SiC does not affect the graphene properties any more than other substrate such as SiO_2.

Field effect transistors based on single layer epitaxial graphene on the C-face of SiC were demonstrated with an on-off ratio more than 10. Electron/hole with high mobility conduction was achieved with a high *k* gate dielectric of aluminum oxide. Quantum Hall effect and Shubnikov de Haas oscillations were observed on both electron and hole branches with a top gate. Boron nitride was successfully grown on epitaxial graphene by ambient pressure chemical vapor deposition. With a boron nitride gate dielectric, a multi-layer epitaxial graphene transistor was fabricated and demonstrated.

A thin layer of silicon oxide (Si_2O_3) was observed on the high temperature high vacuum annealed C-face 6H-SiC. The band alignment at the C-face semi-insulating 6H-SiC/Si_2O_3 interface was analyzed by surface characterization and numerical calculations.

A Schottky barrier transistor using the two-dimensional electron gas in the interface as channel and multilayer epitaxial graphene as contacts was fabricated. The transistor I-V characteristics exhibited over six orders of magnitude change in current. The operation of Schottky barrier transistor can be explained by the interface band alignment (SiC/MEG and SiC/Si_2O_3) and space-charge-limited current in the channel.

6.2 Further Considerations

To continue, the performance of Schottky barrier transistor can be improved by reducing the energy barrier between the 2DEG conduction band and the SiC Fermi level. Therefore, we are approaching the realization of a barrier height tunable tunneling Schottky barrier transistor. Some experimental techniques can be applied achieve this goal. For example, we can increase the band bending voltage in the SiC/Si_2O_3 interface by reducing the density of interface states with a post-annealing in the inter gas environment; or we can engineer the Fermi level position in SiC to move it closer to the conduction band. To make a step further toward the large scale integration of graphene devices on the C-face of SiC, a circuit composed of single layer epitaxial graphene FET/RF transistor and SiC/Si_2O_3 Schottky barrier transistor can be conceived. Since graphene, SiC and boron nitride can withstand very high temperatures (at least 1200 °C) in an inert gas environment, a graphene transistor with a SiC substrate, graphene channel, boron nitride dielectric and high temperature tolerant contacts will also provide a sufficient condition for high temperature electronics application.

APPENDIX A

SILICON CARBIDE ALIGNMENT MARKS FABRICATION PROCESS

SiC alignment marks fabrication process is described as follows:

1. Spin coat e-beam positive resist PMMA (495, A6) on clean SiC chip at 10000 RPM for 60s. Bake the sample on the hot plate for 60 seconds at 90 ºC. Spin coat HSQ (6%) on top of the PMMA coated sample at 4000 PRM for 60 seconds. Bake sample on the hot plate for 4 minutes at 80 ºC.
2. Pattern alignment marks group on the coated sample with HSQ resist dosage and current setup by e-beam lithography. Develop the sample in Tetramethyl Ammonium Hydroxide (TMAH) (25%) for 90 seconds. The designed alignment mark areas were covered by the HSQ/PMMA stacks (150 nm/200 nm).
3. Load the sample in the RIE chamber and etch with oxygen plasma for 90 seconds to fully remove PMMA. After etching, the whole SiC surface was exposed except for the alignment mark areas with the PMMA/HSQ bi-layer stack.
4. Deposit 80 nm Ni on the sample with e-beam evaporator. Lift off metal thin film in acetone. The whole SiC surface is covered by Ni except for the alignment marks region.
5. Transfer the sample to the Plasma Thermal ICP chamber. Etch sample in O_2 and CF_4 (15:5) mixing gas for 5 minutes and obtain 500 nm SiC etching depth.
6. Soak the sample in nitric acid (70%) overnight and sonicate it for one hour in ultrasonicator. Clean the SiC chip with acetone and IPA thoroughly.

The SiC chip with 500 nm deep alignment marks is ready for graphitization. This process is illustrated in Figure A.1.

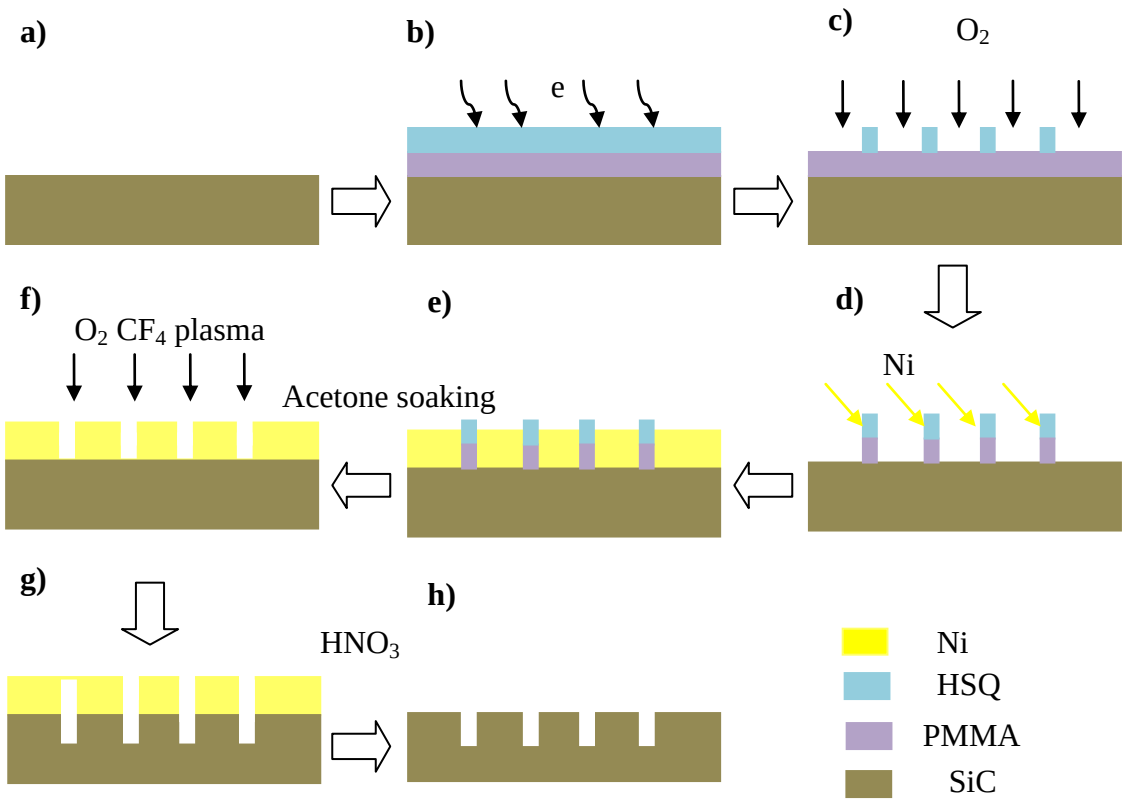

Figure A.1: The SiC alignment mark fabrication process. The SiC alignment mark ensures the alignment marks withstand high temperature treatment. a) SiC (000-1) face; b) Spin coat the SiC surface with PMMA (495, A6)/HSQ(6%) bi-layer and expose the sample in EBL with the alignment mark pattern; c) Develop the pattern in TMAH for 30 seconds and etch sample surface with oxygen plasma for 90 seconds; d) Evaporate 80 nm nickel all over the surface with e-beam evaporator; e) Lift off nickel in acetone overnight; f) Load the sample in Plasma ICP to etch SiC in O_2 and CF_4 gas for 5 minutes. g) Form 500 nm deep SiC surface alignment marks through etching; h) Etch the sample in nitric acid to get rid of nickel, followed by sonicating the SiC in acetone and IPA.

APPENDIX B

BORON NITRIDE GROWTH METHOD

Boron nitride can be grown on the epitaxial graphene with the ambient pressure chemical vapor deposition method in a two-zone furnace (KMT Furnace, SWGL-1600X, MTI Corporation). The method is described as follows:

1. Load the MEG sample with the deposition side facing up in a quartz boat (A) into the center of the high temperature zone (high T zone). Evenly add 5 gram ammonia borane powder in the center of another quartz boat (B). Adjust the thermal couple to be right on top of the chemical powder. Connect the thermal couple to a multi-meter for temperature reading. Load boat B at the end of the low temperature zone (low T zone). Close both ends of the tube furnace.
2. Purge the system with H_2/Ar mixing gas flow at a rate of 540 sccm. Set the target temperature of high T zone to 1000 °C and low T zone to 250 °C. Program the heating step to 10 °C /minute below 800 °C and 5 °C /minute above 800 °C to avoid breaking the furnace inner insulator. After 30 minutes reduce the gas flow rate to 270 sccm and start system heating sequence program.
3. When the high T zone reaches its target temperature, reduce the gas flow rate to 135 sccm. Slowly push the chemical powder boat from the end of the low T zone toward the center of the low T zone. Control the moving speed by reading the temperature rising rate from the thermal couple so that the chemical powder temperature will not increase faster than 1 °C /s.
4. When the thermal couple reads 120 °C, stop moving the sample boat and let the temperature to stabilize. This temperature will stabilize between 120 °C and 130 °C. During the reaction ammonia borane powder turned to white foam and its volume expanded by several times.

5. Stop the reaction after 1hr by pulling the chemical powder boat (B) back to the end of the low T zone. The high T zone starts to cool down in the same time. Pull the epitaxial graphene sample boat (A) to the other end of the high T zone when its temperature drops below 300 °C.
6. Cut off the H_2/A_r mixing gas after the temperature in high T zone drops below 100 °C. Take sample out when the system cools down to room temperature.

The schematic for the growth system and process is depicted in Figure B.1.

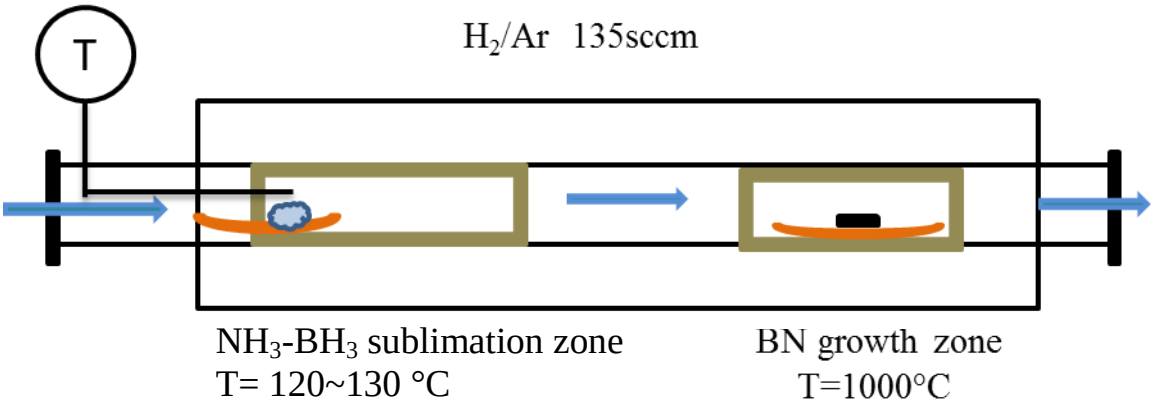

Figure B.1: Schematic for the boron nitride growth chamber. Boron nitride was grown on the epitaxial graphene in a two-zone furnace via the ambient pressure chemical vapor deposition method. Ammonia borane powder was sublimated at T=125 °C in the low temperature zone. The temperature of chemical decomposition was monitored by a thermocouple. The sample was loaded in the high temperature zone and heated up to 1000 °C. The decomposition product NH_2-BH_2 and H_2 were transferred by the hydrogen and argon mixing gas to the high temperature zone. Boron nitride was formed directly on the epitaxial graphene surface.

APPENDIX C

SILICATE ON THE C-FACE OF SILICON CARBIDE

Here I briefly summarize the surface characterization of silicate (Si_2O_3) observed on the C-face of SiC reported in literature. A highly ordered ultrathin monolayer silicon oxide was observed on the C-face of SiC by hydrogen plasma or hydrogen flow etching (Starke, et al., 1999). A well-ordered $\sqrt{3}\times\sqrt{3}R30°$ reconstructed surface was observed by LEED immediately upon introduction into vacuum. The samples contain approximately one layer of oxygen bonded to Si atoms as indicated by Auger electron spectroscopy (AES). This ultrathin monolayer was determined to be silicate Si_2O_3 by full dynamical LEED structure analysis (Bernhardt, et al., 1999) and *in-situ* oxidation experiment (Hoshino, et al., 2004).

Quantitative LEED analysis proposed a Si_2O_3 adlayer model for the C-face SiC treated by hydrogen plasma followed by exposure to air (Bernhardt, et al., 1999). According to this model, the topmost layer has a honeycomb structure in which each Si atom is connected to three oxygen atoms and to an underlying carbon atom, as depicted in Figure C.1 b). Such a model is also confirmed by oxidation kinetic experiment at high temperature (at 500 °C and 900 °C) (Hoshino, et al., 2004) in medium energy ion scattering (MEIS) and angle-resolved ultraviolet photoelectron spectroscopy (PES). The structures maintain their high degree of order even during exposure to ambient air and are stable up to temperatures of 1000 °C in UHV (Bernhardt, et al., 1999).

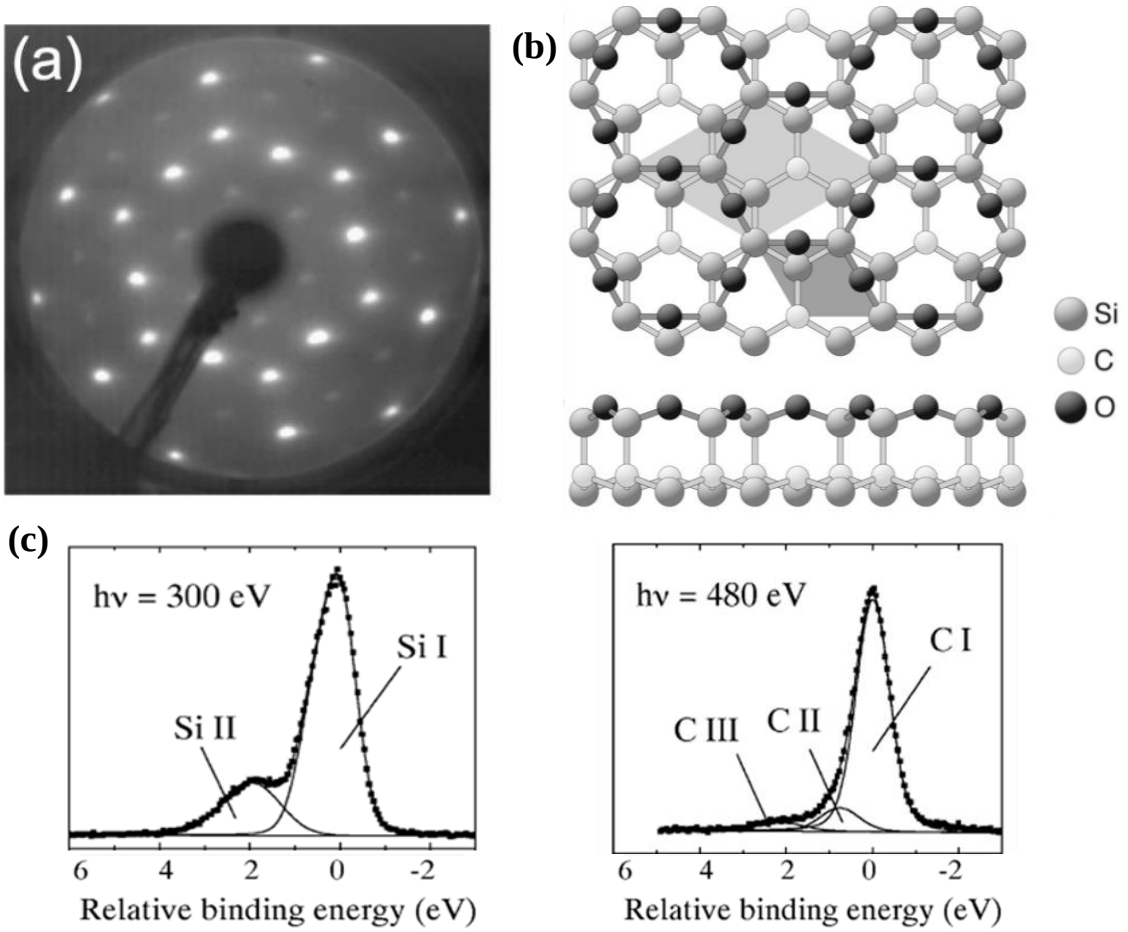

Figure C.1 LEED pattern of the *ex-situ* prepared, as-introduced $\sqrt{3}\times\sqrt{3}R30°$ reconstructed SiC surfaces 6H-SiC (000-1) at 164 eV. b) Top view of the oxide structure on SiC (000-1). The Si_2O_3 silicate adlayer consists of a honeycomb structure with Si–O–Si bonds. In the center of the hexagons one carbon atom of the topmost substrate bilayer is visible (dark shaded area indicates the (1×1) unit cell, light shaded the $\sqrt{3}\times\sqrt{3}R30°$ unit cell). Bottom is the side view projection along the (01-10) direction. c) Si 2*p* and C 1*s* core-level spectra of silicate on SiC (000-1) after being annealed at 650 °C. Si 2*p* has two components at 100.6 eV (Si I) and 102.4 eV (Si II), which are associated with bulk component SiC and surface silicon oxide. C1s has three components at 282.9 eV (CI), 283.7 eV (CII) and 285.0 eV (CIII), which are associated with bulk component SiC, carbon face dangling bond and surface hydrocarbon absorbents.

Another experiment (Shirasawa, et al., 2007) demonstrated the formation of silicon oxynitride (SiON) epitaxial layer on 6H-SiC (0001) by etching the surface with hydrogen and annealing it subsequently in nitrogen atmosphere. The authors claim a

hetero-double-layer structure: a silicate monolayer on a silicon nitride monolayer via Si-O-Si bridge bonds. The STM image revealed the silicate surface on such structure has atomically ordered lattice structure. Additional STM I-V curve shows a surface band gap about 9eV on such oxide layer (Figure C.2) and no midgap states are observed.

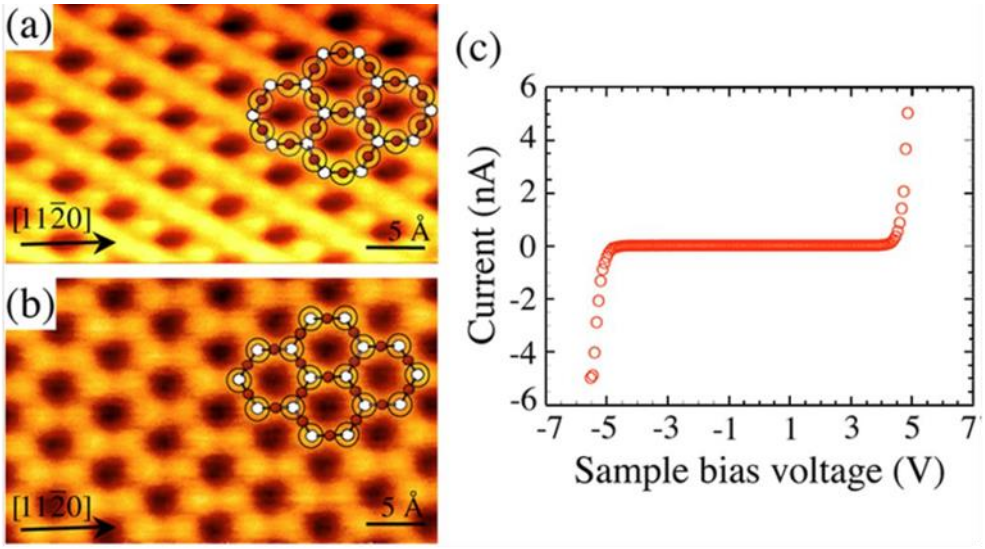

Figure C.2: (a) Filled and (b) empty-state high resolution STM images of the SiON layer taken at V_{ss} of(a) 5.0 and (b) 4.5 V and a tunneling current of 1 nA. Transparent circles indicate the bright protrusions. Ball and stick model of the silicate layer of the SiON is overlaid for comparisons, where solid and empty spheres are O and Si atoms, respectively.(c) A typical STM I-V curve taken on the SiON layer (Shirasawa, et al., 2007)

APPENDIX D

DETERMINATION OF FERMI LEVEL IN VANADIUM DOPED 6H-SIC

The SiC samples used in the Schottky barrier transistor experiment is vanadium doped semi-insulating 6H-SiC (II-VI Corp.). In the wafer data sheet, it states the Fermi level locates at 0.8 eV below the conduction band of 6H-SiC. This number can be further verified by two other methods.

Method 1: Determine E_F by the charge neutrality condition (the amount of positive charges equals to that of negative charges).

$$\frac{N_D}{1+12e^{\frac{E_F-E_D}{k_BT}}} = N_c e^{\frac{E_F}{k_BT}} + \frac{N_A}{1+4e^{\frac{E_A-E_F}{k_bT}}} \qquad \text{(D-1)}$$

where N_D = 5×10^{15} cm^{-3} to1×10^{16} cm^{-3} of nitrogen donors, N_A = 1 × 10^{17} cm^{-3} of vanadium acceptors, N_C = 8.9×10^{19} cm^{-3} is the effective density of states in 6H-SiC, 12 is the number of equivalent conduction band minima in 6H-SiC (6) times spin degeneracy. 4 is the number of valence band maxima (light hole and heavy hole) in 6H-SiC (2) times spin degeneracy. E_c=0 eV, E_D= -0.1 eV. The acceptor level is E_A= -0.8 eV based on a review of vanadium acceptor levels is provided in the work of Mitchel (Mitchel, W. C., et al., 2007).

Due to large amount of vanadium, it can be seen from the neutrality condition that Fermi energy lies few meV's (order of k_BT) below the vanadium acceptor states. Solve equation (E-1), E_F= -0.82 eV.

Method 2: Determine E_F by bulk carrier density and mobility.

The carrier density n_{3D} in the SiC conduction band (Ashcroft, 1976, P574)

$$n_{3D} = 2M_c \frac{(2\pi m_c k_B T)^{3/2}}{h^3} e^{-\frac{(E_c - E_F)}{k_B T}} = N_c e^{-\frac{(E_c - E_F)}{k_B T}} \qquad \text{(D-2)}$$

where M_c is number of equivalent conduction band minima (M_c = 2 in 2H-SiC, M_c = 3 in 4H-SiC, M_c = 6 in 6H-SiC), m_c is the product of the principal values of the SiC conduction band effective mass tensor (i.e., its determinant)

$$m_c = \sqrt{m_x^{\,2} + m_y^{\,2} + m_z^{\,2}} = \sqrt{(0.42m_0)^2 + (0.42m_0)^2 + (0.2m_0)^2} = 0.6m_0$$

and N_C = 8.9×10^{19} cm^{-3} is the effective density of states in 6H-SiC. The charge density at T = 300 K and E_c-E_F = 0.8 eV is n_{3D} = 3.2 × 10^{12} m^{-3}. The value n_{3D} = 3.2 × 10^{12} m^{-3} together with known bulk resistivity of Vanadium doped 6H-SiC ρ = 1 × 10^{11} Ωcm gives carrier mobility $\mu = \frac{1}{e n_{3D} \rho} = 20\,\mathrm{cm}^2/Vs$. The carrier density and mobility is consistent with provider's characterization data (carrier density 10^{12}~10^{13} cm^{-2}, mobility less than 100 cm^2/Vs).

APPENDIX E

NUMERICAL CALCULATION OF BAND ALIGNMENT

The band bending voltage in SiC/Si_2O_3 interface from XPS experiment data can be reproduced with numerical calculations by adjusting the density of interface states. These numerical calculations were done by my collaborator Dr. Jan Kunc. I will briefly introduce the principle of calculations and its result here.

The formation of two-dimensional electron gases (2DEG) at the heterojunction of 4H/3C-SiC and 6H/3C-SiC was investigated by numerical self-consistent solutions of the Schrödinger and Poisson equations (Polyakov, et al., 2005). A similar calculation can be done to the $6H\text{-}SiC/Si_2O_3$ interface too. The Schrödinger equation in effective mass approximation

$$\left(\frac{p^2}{2m_e} + V_H + V_{xc} + V_{conf}\right)\chi(z) = E\chi(z) \qquad \text{(E-1)}$$

has been solved self-consistently with Poisson equation

$$\frac{d}{dx}\left(-\varepsilon_0\varepsilon_r\frac{d\varphi}{dx} + P_0\right) = \rho_D + \rho_A + \rho_{gs} + \rho_\chi \qquad \text{(E-2)}$$

taking into account direct Coulomb (V_H) mean-field exchange and correlation (V_{xc}) electron-electron interaction and confinement energy (V_{conf}) due to band offsets on the interface. The charge in our model has several sources. The first source of charge is the spontaneous polarization P_0. Hexagonal polytypes are expected to have an intrinsic spontaneous polarization (SP) due to the bond to bond charge transfer and ionic relaxation (Qteish, et al., 1992; Lu, et al., 2009). P_0 contributes as a bound charge $\rho_b = -\nabla \cdot P_0$. Other three sources of bound charge are positively ionized nitrogen donors ρ_D, negatively charged ionized vanadium acceptors ρ_A, interface (or gap states) ρ_{gs}. The

gap states are described by metal induced gap states (MIGS) theory and charge neutrality level (CNL) scheme (Tung, 2001; Louie, et al., 1977). The last contribution to charge density is free negative charge $\rho\chi$ due to the occupied quantum levels as determined by the solution of Schrödinger equation.

Based on the XPS data showing bending downward (by 0.6 eV), the CNL model is used with varied density of interface states D_{gs} as an adjustable parameter. This is the crucial parameter which determines band bending after two semiconductors are connected together. The parameters used in the calculation are all extracted from literature except for the density of interface states $D_{gs.}$ The electron effective mass along the SiC c-axis is 2.0 m_0; the electron effective mass in Si_2O_3 is 0.3 m_0; relative permittivity in SiC is 10; conduction band offset SiC/Si_2O_3 is 2.95; spontaneous polarization charge is 9.5 $\times 10^{-3}$ Cm^{-2}; position of conduction band is 2.0 eV; nitrogen donor level E_D=E_C-0.1 eV; vanadium acceptor level E_A=E_C-0.8 eV; Fermi level E_F=E_C-0.8 eV; charge neutrality level E_{CNL}=E_C-1.57 eV; gap states penetration depth: 0.23 nm; density of vanadium acceptor N_A=1.0 $\times 10^{17}$ cm^{-3}; density of nitrogen donor N_D=1.0$\times 10^{16}$ cm^{-3}.

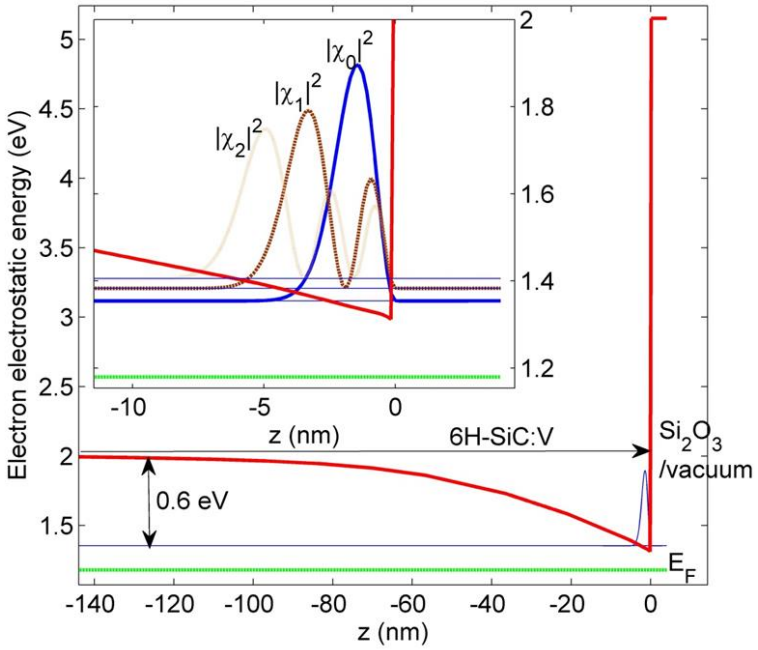

Figure E.1 Interface between semi-insulating C-face 6H-SiC and Si_2O_3 monolayer. Bands are plotted by red solid curves, eigenstates and their eigenenergies are plotted by blue curves and horizontal blue lines, respectively. Dashed green line depicts position of the Fermi energy. Inset shows detail of the interface. (Courtesy of Jan Kunc).

The quality of interface is actually well known to be important for SiC/SiO_2 FETs (Biggerstaff, et al., 2009) and a typical interface states density is 5×10^{11}~1×10^{13} $cm^{-2}eV^{-1}$. To have the first confined energy state from calculation same as XPS band bending voltage, which is 0.6 eV below the conduction band, a density of interface state D_{gs}=3.7 $\times10^{12}$ cm^{-2}/eV was chosen. The interface eigenstates and eigenenergies between C-face 6H-SiC/Si_2O_3 are calculated and shown in Figure E.1.

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