

**ELECTRICAL-THERMAL MODELING AND SIMULATION FOR
THREE-DIMENSIONAL INTEGRATED SYSTEMS**

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The Academic Faculty

by

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**ELECTRICAL-THERMAL MODELING AND SIMULATION FOR
THREE-DIMENSIONAL INTEGRATED SYSTEMS**

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To my family

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CHAPTER 1

INTRODUCTION

1.1 Background

The advancement of through-silicon-via (TSV) fabrication technology makes three-dimensional (3D) integration a promising and key integration technique that can achieve continuous miniaturization of next generation integrated circuits (ICs) and systems. The 3D integration technique provides the capability of integrating multiple dies vertically using TSVs and silicon carriers [1, 2]. A general 3D integrated system consisting of stacked dies, a silicon interposer (or a package), and a printed circuit board (PCB) is shown in Figure 1. Because of the vertical stacking of IC dies, the power density of 3D integrated systems is expected to increase dramatically according to the International Technology Roadmap for Semiconductors [3]. Alleviating the thermal problem for 3D systems requires novel thermal management approaches such as microfluidic cooling using built-in microchannels [4, 5, 6], as shown in Figure 1. Compared to a two-dimensional (2D) integrated system, the design and modeling of a 3D system becomes challenging because of increasing geometry scales and complexities.

1.2 Motivation

Designing a successful 3D integrated system requires efficient numerical modeling and simulation methods that can simultaneously validate electrical performance, thermal integrity, and mechanical reliability. In this regard, the early-design stage modeling and analysis of 3D systems at the system level is important. Modeling includes the extraction of physical parameters and the building of physical or mathematical models that capture electrical, thermal, and mechanical phenomena described by governing equations.

Analysis includes solving problems using numerical solvers to obtain final solutions. As multiple domains such as electrical, thermal, and mechanical domains are included in an integrated system, modeling and analysis become critical. The challenges for the modeling and analysis of 3D systems are discussed in the following subsection.

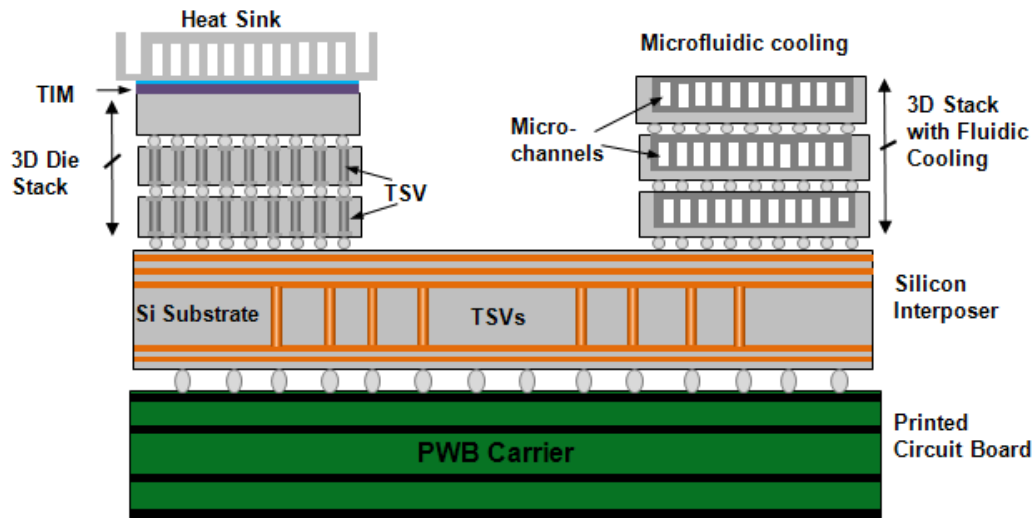


Figure 1. A 3D integrated system.

1.2.1 Major Modeling and Analysis Challenges

The major challenges for the modeling and analysis of a 3D integrated system mainly stem from four aspects: electrical-thermal coupling and interaction, the multiscale nature of 3D systems, the requirement for fast simulation with varying design parameters, and efficient modeling of microfluidic cooling, all explained below:

1. Coupling and interaction between electrical and thermal domains

For an integrated system, since materials such as metal conductors and the silicon substrate usually have temperature-dependent properties, a non-uniform temperature profile can affect electrical performance both in steady state and at high frequencies. The temperature-dependent electrical resistivities of metal conductors such as silver, copper,

and aluminum are shown in Figure 2a while the electrical resistivity of silicon carrier is shown in Figure 2b. In steady state, a power delivery network (PDN), which consists of metal conductors and can be represented using a resistance network, delivers DC voltage and current to IC chips [7, 47]. As the electrical resistivities of metal conductors are temperature-dependent, the effect of temperature on the steady-state voltage drop in a power delivery network needs to be investigated. In addition, because of current flowing in a PDN, generated Joule heating can affect thermal distribution. Thus, the electrical and thermal characteristics interact and form a coupling system in the steady state.

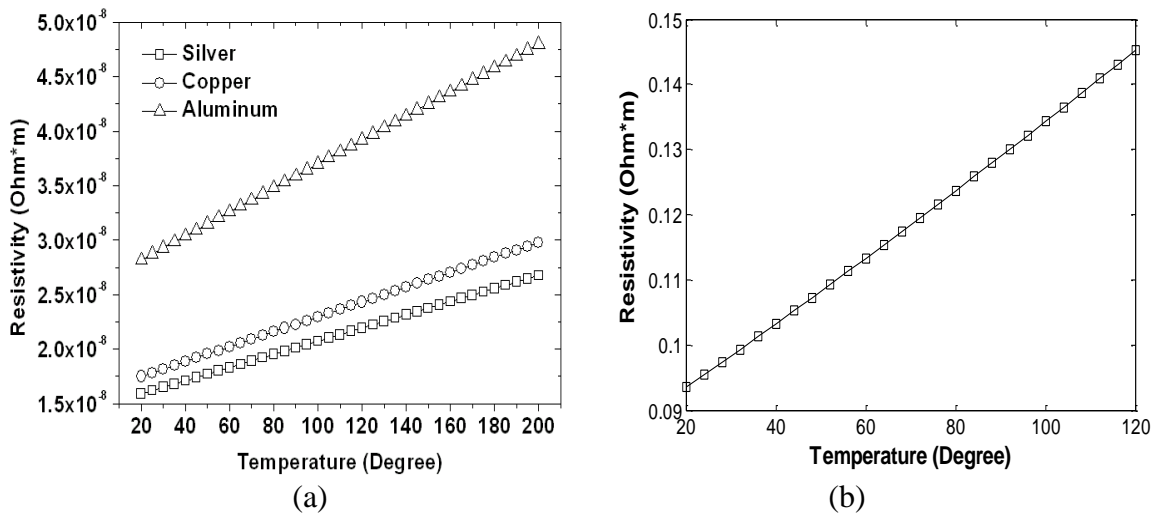


Figure 2. Temperature-dependent resistivities of (a) conductors including silver, copper, and aluminum, and (b) silicon substrate.

At higher frequencies, for the electrical modeling of TSV arrays in a silicon interposer (Figure 1), as the electrical resistivity of silicon substrate is a function of temperature (Figure 2b), the electrical performance of TSV arrays such as insertion loss and crosstalk between neighboring TSVs can be affected by the thermal profile. Therefore, designing and modeling TSV arrays must take into account the effect of

system thermal profile. Addressing the thermal effect on TSVs and facilitating TSV array design requires combined thermal-electrical modeling for TSV arrays.

In summary, the inclusion of simultaneous electrical and thermal phenomena complicates the modeling of 3D systems and requires the development of co-simulation methods. Although thermal and mechanical characteristics also interact because of the mismatch between coefficients of thermal-expansion (CTE) of materials, the co-simulation methods in this dissertation mainly focus on electrical-thermal modeling and analysis.

2. Multiscale nature of 3D systems

For a 3D system shown in Figure 1, the stacked IC region, which has a smaller footprint than the PCB and package, usually contains a great number of small features such as TSVs, vias, and micro-bumps. Consequently, the stacked IC requires finer meshing grids than the package and PCB. Because of the co-existence of both small-sized features and the large-sized package and PCB, the scale difference of features in a 3D system can reach 1:50,000. In addition, as each chip has its own functional blocks, it requires different meshing grids as compared to other chips. The layout difference between stacked chips can cause the mesh grids to propagate from one chip to another with a conformal meshing approach. Therefore, performing thermal or voltage drop modeling of the entire 3D structure requires millions of meshing cells using either conformal finite element or finite volume-based meshing grids. The large number of meshing cells can lead to extensive simulation time and large memory consumption. The multiscale nature of 3D systems poses a critical requirement in terms of fast early-stage modeling and analysis at the system level. Therefore, performing system-level modeling

and achieving fast simulation requires novel multiscale modeling and simulation methods for both DC voltage drop and thermal analysis.

3. The requirement of fast thermal simulation with varying design parameters

Performing fast simulation for a 3D system with varying design parameters becomes challenging when a great number of meshing cells are present. The varying design parameters include power maps of dies, the thermal conductivity of a certain layer, and air convection coefficients on boundaries. To accelerate the thermal simulation with various power maps, model order reduction (MOR) techniques can be utilized. However, because of multiple scales in a 3D system, meshing the entire system can lead to a large number of cells and large thermal capacitance/conductance stiffness matrices. Therefore, for thermal modeling of a 3D system, creating reduced-order models (ROMs) using existing MOR techniques becomes challenging when the size of the system matrix is large and many MOR ports are present. Although iterative matrix-solving techniques can be used to compute projection matrices during the process of MOR, the time consumption increases dramatically because of iterative solving procedures. To circumvent this problem, a new thermal modeling methodology that can handle 3D systems with varying design parameters needs to be developed.

4. Efficient modeling of microfluidic cooling

As the microchannel-based fluidic-cooling technique (Figure 1) has become a promising way of mitigating the thermal problem of 3D systems, the thermal modeling of microfluidic cooling has become a requirement. The inclusion of a large number of microchannels and the fluid velocity complicates the thermal modeling process. Although the computational fluid dynamic (CFD)-based modeling approach can be used to model

one or two microchannels, it becomes computationally intensive when microchannel arrays are used for cooling 3D stacked ICs. Therefore, facilitating early-design stage thermal modeling requires compact thermal models for microchannels that can accurately represent the fluidic cooling behavior and effectively reduce the simulation time using fewer meshed cells/unknowns than that of the CFD approach.

Addressing the aforementioned challenges for the electrical/thermal modeling and analysis of 3D systems requires the development of novel numerical modeling methods, which is the motivation of the research work elaborated in this dissertation.

1.3 Contributions

This dissertation mainly focuses on developing efficient electrical and thermal numerical modeling and co-simulation methods for 3D integrated systems. The research work can be classified into two parts. The first part aims to investigate the interaction between electrical and thermal characteristics for PDNs (power delivery networks) in steady state and the thermal effect on characteristics of TSV arrays at high frequencies. The steady-state electrical-thermal interaction for PDNs is addressed by developing a DC voltage drop-thermal co-simulation method while the thermal effect on TSV characteristics is studied by proposing a thermal-electrical co-analysis approach for TSV arrays. The second part of the research focuses on developing fast numerical methods for (a) multiscale modeling for thermal and voltage drop analysis, (b) compact thermal modeling of microfluidic cooling, and (c) system-level thermal modeling with varying design parameters. As part of the research effort, several numerical methods have been developed. The contributions of the research are listed as follows:

1. The development of a steady-state voltage drop-thermal co-simulation method for PDNs. This co-simulation method ultimately takes into account the temperature effect on electrical resistivity and the Joule heating effect on temperature increases. As a result, accurate voltage drop analysis can be performed considering non-uniform temperature profiles in 3D systems. The developed co-simulation solver also allows identifying hotspots created by Joule heating.
2. The development of a thermal-electrical analysis method for TSV arrays in interposers. The temperature-dependent material properties of silicon substrates and TSV conductors can be taken into account for the modeling of TSV arrays. As a result, the temperature effect on the insertion loss, crosstalk, and noise coupling of TSV arrays can be investigated.
3. The development of a multiscale modeling approach for both thermal and voltage drop analysis. The proposed approach provides the capability of meshing 3D problems containing objects with multiple scales using the domain decomposition approach, which allows independent meshing of subdomains with non-matching grids at interfaces.
4. The development of a compact thermal model for microchannel-based fluidic cooling. The compact thermal model can represent a microchannel using much fewer unknowns/cells than the CFD approach. As a result, the compact thermal model can enable efficient thermal modeling of 3D systems with a large number of micro-channels.
5. The development of a system-level thermal modeling method using domain decomposition and model order reduction. The proposed method can be applied to both steady-state and transient thermal modeling with varying design parameters.

1.4 Organization of the Dissertation

This dissertation consists of eight chapters. In Chapter 1, the background and motivation, contributions, and the organization of this dissertation are introduced. The major challenges for modeling and analysis of 3D systems are discussed. In Chapter 2, the research problems to be addressed and prior art that have been developed in the open literature are investigated. In Chapter 3, the steady-state voltage drop-thermal co-simulation approach for PDNs is presented. In addition, the thermal-electrical analysis for TSV arrays is discussed, and the temperature effect on TSV characteristics is investigated. The multiscale modeling technique for voltage drop and thermal analysis using the non-conformal domain decomposition is introduced in Chapter 4. In Chapter 5, the derivation of a compact thermal model for microfluidic cooling is discussed. The transient thermal analysis using the proposed compact thermal model for microfluidic cooling and domain decomposition is presented. In Chapter 6, a system-level thermal modeling approach using domain decomposition and model order reduction is elaborated. In Chapter 7, the domain decomposition technique for thermal analysis is extended to electromagnetic (EM) modeling, which is the future work. A 2D finite-difference non-conformal domain decomposition method for solving 2D electromagnetic problems is presented. Finally, the summary and conclusion of the research work in this dissertation are shown in Chapter 8.

CHAPTER 2

ORIGIN AND HISTORY OF THE PROBLEM

2.1 Design and Modeling of 3D Integrated Systems

The computer-aided design (CAD) of 3D integrated systems requires modeling and simulation tools that can verify the steady-state and transient performances of components before mass production. The electrical and thermal performances considered in the scope of the research include DC voltage drop, temperature distribution, signal crosstalk and noise coupling between TSVs, and electromagnetic behaviors of plane structures in a power delivery network. For a 3D system with microfluidic cooling, the performance of microchannels also needs to be validated. To reduce the design cycle of today's electronic products, the development of efficient numerical modeling and simulation methods becomes more and more important.

The advancement of 3D integration technology brings in new contents for modeling and simulation. First, as TSVs become key components for chip stacking in 3D integration, capturing the TSV characteristics (e.g., insertion loss and crosstalk) necessitates the development of electrical models for TSV arrays for circuit designers. Second, the vertical integration of IC dies resulting in high power densities in 3D systems makes the temperature an important factor to be considered in real designs. The temperature effects on electrical performances such as voltage drop and the characteristics of TSV arrays need to be investigated through co-simulation or co-analysis approaches. Third, emerging thermal management approaches using microchannel arrays make the thermal modeling of microfluidic cooling very important. As a contrast to the computational fluid dynamic modeling approach, efficient thermal

simulation of a large microchannel array requires developing a compact thermal model for microchannels.

On the other hand, the advancement of 3D integration technology also brings in new challenges for modeling and simulation. The first challenge stems from the requirements of performing the thermal, voltage drop, and electromagnetic modeling of multiscale structures arising in 3D systems. The second challenge comes from the requirement of performing fast thermal modeling with varying design parameters. As a 3D system integrates multiple functional blocks with many tunable design parameters, optimizing a design requires repeating the modeling and simulation process with various design parameters. As usual, numerical modeling and simulation involves solving a matrix equation with a given excitation. As a result, the increase in problem size and modeling complexity can complicate the matrix solving process. The specific challenges are depicted in Figure 3 and elaborated from a numerical modeling standpoint.

Numerical electrical/thermal modeling of 3D structures becomes challenging particularly when the problem scale is large and many unknowns are present. A practical 3D problem usually contains inhomogeneous material stack-ups and both small-sized and large-sized objects such as TSVs, micro-bumps, small apertures and voids, and large planes in PCBs. Using the finite difference method (FDM) or finite element method (FEM), non-uniform meshing grids can be used to reduce the number of meshing cells/unknowns. However, when a problem contains many objects with multiple scales, the large scale difference can still result in a large-scale stiffness matrix (Figure 3) because of extremely dense meshing grids in certain regions using non-uniform meshing. Efficiently modeling multiscale structures requires numerical modeling techniques such

as domain decomposition methods for voltage drop modeling, thermal simulation, and electromagnetic modeling.

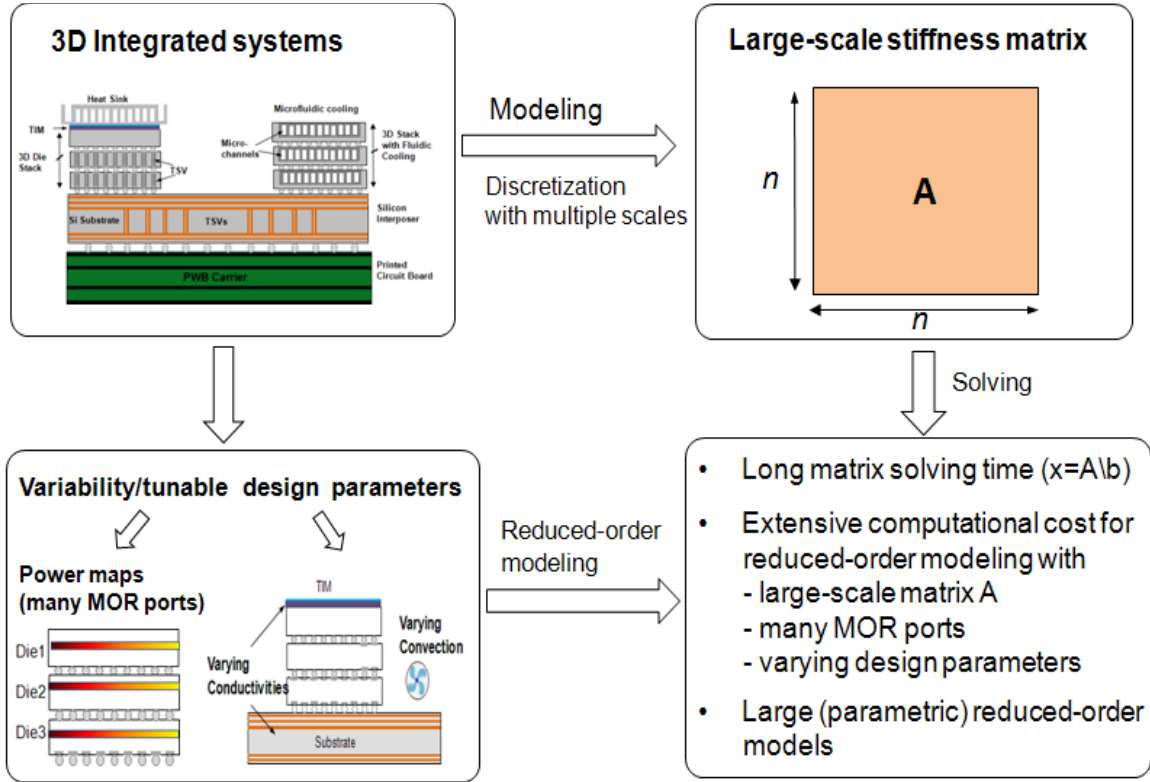


Figure 3. Numerical modeling challenges arising from 3D integration.

In addition to the multiscale nature of 3D problems, difficulties arise in numerical thermal modeling when fast simulation is required with various excitations and many tunable design parameters (Figure 3). As an example, steady-state thermal modeling requires re-solving a matrix equation when the thermal excitation is changed while transient thermal modeling requires repetitively solving a matrix equation at each time step with a dynamic thermal profile. Accelerating the modeling process requires building small-sized reduced-order models that can accurately represent the original large-dimension models using model order reduction techniques. Furthermore, building

reduced-order models for problems containing tunable design parameters requires parameterized model order reduction techniques. Reduced-order modeling using MOR has shown promise when modeling small-sized problems or components such as a MEMS device or a chip. However, as 3D integrated systems consist of many functional blocks (e.g., dies, an interposer, a package, and a PCB), directly creating a reduced-order model using model order reduction becomes challenging because (a) 3D systems usually require a large-scale stiffness matrix and (b) the computational cost of MOR increases dramatically with the size of the stiffness matrix, the number of excitations (e.g., MOR ports), and the number of tunable design parameters.

In the next section, the prior methods for thermal modeling, reduced-order modeling, DC voltage drop simulation, microfluidic cooling modeling, and modeling using domain decomposition are investigated. As investigating the electrical-thermal interaction and coupling for PDNs in steady state and for TSV arrays at high frequencies composes part of the research, the methods for electrical-thermal modeling and the electrical modeling for TSV arrays are also introduced.

2.2 Methods for Modeling and Simulation of Integrated Systems

2.2.1 Methods for Thermal Modeling of Solid Media

In the past decade, a considerable number of approaches have been devoted to both the steady-state and transient thermal modeling of IC chips and packages [8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. These thermal modeling methods can be classified into two categories: (1) differential equation-based methods and (2) integral equation-based methods. The differential equation-based method starts by formulating thermal problems based on differential governing equations and then constructs numerical schemes based

on discretizing entire structures using volumetric mesh grids or cells. Using the constructed numerical schemes, the stiffness matrix can be created, and the original problem is converted to a system matrix equation. Because of the localized finite-element basis functions or finite-difference approximations used to derive the scheme, the coupling between nodes exists for only nearby cells or grids. As a result, the system stiffness matrix is large and sparse.

The differential equation-based thermal modeling methods include the finite difference method and the finite element method. For a finite difference-based solver, a straightforward finite-difference approximation is used to approximate the first- and second-order derivatives of the heat equation. For a finite element-based solver, linear- or high-order basis functions with unknown coefficients are used to approximate the solution. For thermal modeling with conventional heat-sink cooling, the methods in [8, 9, 10] are based on the FEM (finite element method), and the approaches in [11, 12, 13] are based on the FDM (finite difference method). For thermal simulation with a large number of unknowns, iterative solving techniques such as the preconditioned conjugate gradient (PCG) method are required. To alleviate the effect of the increasing problem size on simulation time, thermal modeling using the 3D geometrical multigrid approach has been proposed for the thermal simulation of IC chips in [14, 15]. For transient thermal modeling of IC chips, implicit methods such as the backward Euler method and the Crank–Nicolson (CN) method [16] can be adopted. Because of the implicit formulation, an implicit method requires solving a system matrix equation at each time step. To reduce the computational cost using the implicit scheme, a 3D transient thermal solver based on the alternating direction implicit (ADI) method has been introduced in [17]. Instead of

solving the original stiffness matrix that has a large bandwidth, the ADI method alternately solves three system matrix equations with tri-diagonal stiffness matrices in the x , y , and z directions. Therefore, simulation efficiency greatly improves.

An integral equation-based method formulates the problem using an integral governing equation. The method only discretizes structure surfaces, boundaries, and excitation layers. Therefore, avoiding the volumetric meshing of the entire structure leads to a reduced number of meshing cells and unknowns. However, because of global coupling between cells, the resulting system stiffness matrix is small but dense. The integral equation-based methods include the boundary element method (BEM) [18, 19, 20]. The boundary element-based approach employs a Green's function to estimate the thermal profile. Because of the Green's function, the accuracy can be limited when applied to 3D inhomogeneous problems that contain a complex material stack-up for ICs, packages, and PCBs.

2.2.2 Methods for Thermal Modeling of Microfluidic Cooling

For the modeling of microfluidic cooling, computational fluid dynamic simulation [21], which is based on solving the Navier–Stokes equations, can be applied. However, because of the computationally intensive nature of CFD simulation approaches, simplified compact thermal models that can capture the fluidic cooling behavior using fewer unknowns are preferred. To capture the microfluidic cooling effect, several approaches have been proposed in [5, 6, 22, 23, 24, 25, 26] for steady-state thermal analysis. A one-dimensional (1D) thermal resistance network with constant heat transfer coefficients from all four surfaces of the microchannel has been proposed in [22] to model the microchannel. A similar thermal resistance network-based microchannel model

has been proposed in [23]. The model is combined with a 3D resistance network model for a solid medium to predict the temperature of multi-layered mini-channel heat sinks. In [24], for modeling the convection of boiling water in stacked ICs, an equivalent thermal resistance model has been proposed based on a one-dimensional conservation equation. A thermal-wake function-based model has been proposed in [25] to model microchannel-based fluidic cooling. The thermal-wake function can be extracted using CFD simulations or analytical formulae. The thermal-wake aware microchannel model can be combined with the conventional thermal resistance network for heat conduction to predict the temperature of 3D stacked ICs.

For transient thermal analysis, a compact transient thermal modeling approach based on the FDM has been proposed for stacked ICs with inter-tier liquid cooling in [27]. Instead of using four nodes to represent one microchannel cell as in [25], the proposed model uses only one node per-cell. The modeling method in [27] has demonstrated having higher efficiency than that of the full CFD model.

2.2.3 Methods for DC Voltage Drop Simulation

Because of the finite electrical conductivity of metal conductors, a voltage drop occurs when current flows through a PDN in an integrated system. For a PDN with a regular shape, the voltage drop can be calculated using analytical equations and the method of equivalent resistance. However, in a package or a PCB, a PDN usually contains irregular shapes such as apertures, via arrays, and holes. Estimating the voltage drop in a PDN with complex structures requires numerical simulation. Voltage drop analysis based on an equivalent-circuit approach has been proposed in [28]. A finite volume-based 2D voltage-drop analysis method has been developed for the package-level

voltage-drop analysis in [29]. By meshing PDN conductors and formulating the problem using the finite-volume scheme, the current density and voltage drop can be computed for a 2D irregular power plane structure.

2.2.4 Methods for Electrical-Thermal Co-simulation

In the past, the interaction between electrical and thermal characteristics has been studied. A transistor thermal model that accounts for the self-heating (Joule heating) effect was proposed in [30]. Later on, methods for combined electrical-thermal simulation were proposed for the circuit-level simulations in [31, 32, 33]. Among these methods, an electrothermal simulator that utilizes the coupling between the SPICE circuit simulator and a finite-element thermal solver was proposed in [31] and a similar electrothermal simulation method was discussed in [32]. An electrothermal CAD method was proposed for power devices and circuit analysis in [33]. Unlike the thermal modeling methods in [31, 32], which were based on the finite element method, an analytical thermal model based on a spectral domain decomposition technique has been derived for 3D complex geometries in [33]. For the modeling of passive devices, electrothermal modeling approaches have been proposed for planar transformers in [34], GaAs-based interconnects in [35], and integrated thin-film resistors in [36].

2.2.5 Modeling using Domain Decomposition

Domain decomposition, a divide-and-conquer approach, allows the dividing of a large complex problem into many sub-domains that are smaller and easier to handle. For non-overlapping domain decomposition with geometrical conformal meshing grids at interfaces, the coupling between domains can be captured using the relationship between interface nodes and interior nodes [37]. However, because of the conformal mesh used,

the total number of meshing cells cannot be effectively reduced. Therefore, finite-element non-conformal domain decomposition methods such as the Mortar FEM [41] that uses geometrical non-matching meshing grids at domain interfaces have been proposed. The finite-element non-conformal domain decomposition has been applied to eddy-current calculations in [38] and electromagnetic simulations in [39, 40].

Finite-difference time-domain (FDTD) methods [42, 43] and finite-difference frequency-domain (FDFD) approaches [44, 45, 46, 47] have been proposed for solving a variety of electromagnetic problems. To enhance simulation efficiency, domain decomposition finite-difference methods have been proposed for solving electromagnetic scattering using parallel computing in the time domain [43] and using overlapping grids and virtual boundaries in the frequency domain [48]. However, the methods in [43, 48] are based on conformal meshing grids. Since the finite-difference formulation requires conformal grids at interfaces to approximate derivatives in space, modeling using non-conformal domain decomposition based on finite-difference formulations can become challenging for electromagnetic simulations. A finite-difference domain decomposition approach using characteristic basis functions has been proposed for electrostatic problems [49].

2.2.6 Methods for Reduced-Order Modeling

For the computer-aided design of IC chips, model order reduction techniques, which can create low-dimensional reduced-order models that can reduce simulation time, have been developed. In the past few decades, a considerable number of MOR methods have been devoted to building ROMs for interconnect systems and thermal modeling. Among the MOR approaches for interconnects, asymptotic waveform expansion (AWE) [50],

Padé approximation via the Lanczos process [51], a passive reduced-order interconnect macromodeling algorithm (PRIMA) [52], and efficient nodal order reduction (ENOR) [53] have been proposed. To accommodate the variability arising from interconnect design, several parameterized MOR techniques have been proposed based on matrix perturbation expansion theory [54], multi-parameter moment matching [55, 56], and a two-directional Arnoldi process [57]. For thermal modeling using MOR, since thermal models consist of only thermal resistance and capacitance, MOR approaches such as the block Arnoldi algorithm [58] and PRIMA can also be applied [59, 60, 61]. To handle the variability in thermal modeling, parameterized MOR methods [62, 63] have been proposed based on projection techniques [64] and the multi-series expansion, respectively.

2.2.7 Methods for Electrical Modeling of TSV Arrays

As TSVs provide signal and power supply paths for 3D stacked chips, the electrical modeling and characterization of TSV pairs and TSV arrays becomes important. Several approaches have been devoted to the modeling and characterization of TSV parameters based on measurements [65], closed form formulae [66, 67], and the partial element equivalent circuit method [68]. For the modeling of TSV arrays, the numerical TSV modeling method using cylindrical modal basis functions (CMBFs) has been proposed in [69]. Using a small number of basis functions, the method in [69] can efficiently model large TSV arrays, and the modeling results have been correlated with full-wave solvers and measurements. The modeling method using CMBFs has been used for the coupling analysis of large TSV arrays in both frequency and time domains in [70]. For thermal effects on TSVs, the temperature effect on TSV pair capacitance and conductance has

been studied in [71]. The temperature-dependent modeling of a single TSV capacitance has been proposed and verified with measurements in [72]. However, the thermal effect on characteristics of TSV arrays has not been addressed so far.

2.3 Technical Focus of This Dissertation

The investigation of the aforementioned prior art provides the understanding of the advantages and limitations of existing modeling and simulation techniques. With the evolution of 3D integration technology, novel modeling and simulation methods must be developed to facilitate 3D design. The technical focus of this dissertation is listed as follows:

- The investigation of electrical-thermal interactions through the development of a voltage drop-thermal co-simulation approach for PDNs and the thermal-electrical co-analysis for TSV arrays.
- The development of a multiscale thermal and voltage drop modeling approach to handle 3D problems containing multiple scales.
- The development of a compact thermal model for microfluidic cooling to facilitate the thermal simulation of 3D systems with a large number of microchannels.
- The development of a system-level thermal modeling approach that can achieve fast steady-state and transient thermal modeling with many tunable design parameters and hundreds of MOR ports.
- The development of a finite-difference non-conformal domain decomposition method for 2D electromagnetic modeling.

CHAPTER 3

ELECTRICAL-THERMAL CO-SIMULATION FOR POWER DELIVERY NETWORKS AND TSV ARRAYS

3.1 Introduction

In the past decade, the power supply voltage of IC chips has been continually scaled down to reduce power consumption. Maintaining the functionality of high-speed low-voltage IC circuitry requires ensuring the power integrity and signal integrity of the system. One basic requirement of power integrity is to deliver steady-state power supply voltages and currents to IC chips with less voltage drop via a power delivery network. A power delivery network consists of passive metal conductors: power and ground metal planes, vias, apertures, power and ground bumps, power and ground TSV interconnects, and on-chip power grids, as shown in Figure 4. Because of the finite electrical conductivities of metal conductors, a PDN can be represented using a resistance network. Voltage drops occur when electrical currents flow through a PDN. Because of the temperature-dependent electrical resistivity of metal conductors as shown in Figure 2a, the thermal profile of an electronic system can affect the voltage drop in a PDN. On the other hand, when currents flow in a PDN, the Ohmic loss is converted to Joule heat, which can increase the system temperature. As a result, the electrical characteristics of a PDN interact with the thermal gradient. Capturing the temperature effect on voltage drop and Joule heating effect on temperature necessitates a voltage drop-thermal co-simulation approach.

In addition to maintaining power integrity, ensuring signal integrity requires transmitting clean high-speed signals with less insertion loss, crosstalk, coupled noise,

power and ground bounce, and jitters via signal communication paths [7]. In a 3D system, signal communication paths include on-chip interconnects, package- and PCB-level vias and interconnects, bumps, and TSV arrays. Among a TSV array in a silicon interposer (Figure 4), the pitch between TSVs is usually in the range of 10 - 60 microns, which can result in tight coupling among neighboring TSVs. Most importantly, as the silicon substrate has a temperature-dependent conductivity (Figure 2b), the temperature can affect the insertion loss and crosstalk of TSV arrays. The measurements reported in [87] have shown the effect of temperature variation on the noise coupling of a TSV pair. However, modeling high-density TSV arrays with temperature effects has not been carried out so far. To take the thermal effect into account for TSV arrays, a thermal-electrical analysis method is required.

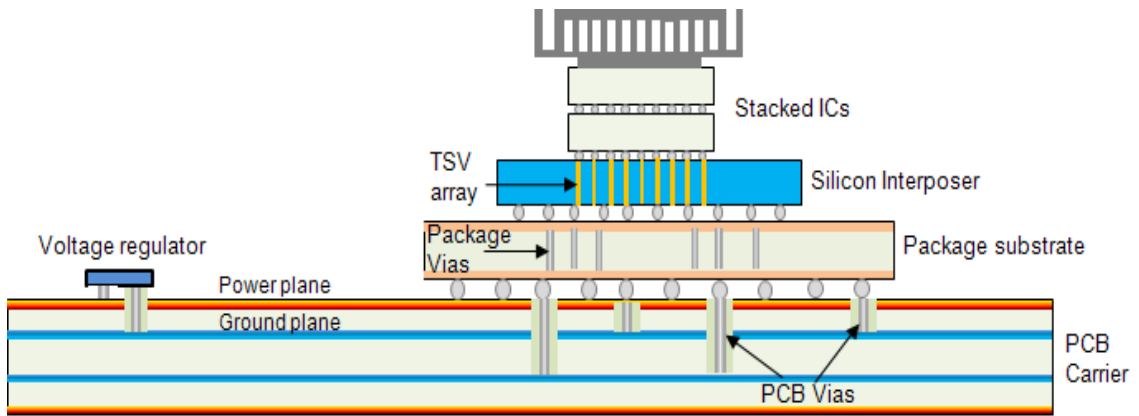


Figure 4. A power delivery network and TSV arrays in a 3D electronic system.

In this chapter, the electrical-thermal modeling is carried out for power delivery networks in steady state and for TSV arrays at high frequencies. To capture the temperature effect on voltage drop in PDNs, a steady-state voltage drop-thermal co-simulation method is presented. This co-simulation approach allows the voltage drop

analysis to take into account the non-uniform temperature distribution in a system, accounting for the temperature effect on electrical resistivities. This approach also provides the capability of performing thermal modeling with Joule heating effects. In addition, to study the thermal effect on TSV characteristics, the thermal-electrical analysis of TSV arrays is carried out. The temperature effect on insertion loss, crosstalk, and coupled noise are discussed.

3.2 DC Voltage Drop-Thermal Co-simulation for PDNs

3.2.1 Co-simulation Flow

In steady state, the governing equation for voltage distribution can be expressed as

$$\nabla \cdot \left(\frac{1}{\rho(x, y, z, T)} \nabla \phi(x, y, z) \right) = 0 \quad (1)$$

where $\rho(x, y, z, T)$ and $\phi(x, y, z)$ represent the temperature-dependent electrical resistivity and voltage distribution, respectively. For the steady-state thermal analysis, the governing heat equations for solid media and fluid flow can be expressed as follows:

$$\nabla \cdot [k(x, y, z) \nabla T(x, y, z)] = -P(x, y, z) \quad (2a)$$

$$\sigma c_p \bar{v}(x, y, z) \cdot \nabla T(x, y, z) = \nabla \cdot (k_f \nabla T(x, y, z)) \quad (2b)$$

where $k(x, y, z)$ and $T(x, y, z)$ represent the thermal conductivity of the solid medium and temperature distribution, respectively; σ , c_p , and $\bar{v}(x, y, z)$ represent the density, heat capacity, and velocity distribution of the fluid, respectively; k_f is the thermal conductivity of the fluid [73, 74]. In Equation (2a), $P(x, y, z)$ is the total heat excitation including the heat source from the chip and the Joule heating converted from the Ohmic loss in a PDN. The Joule heating can be expressed as

$$P_{Joule}(x, y, z) = \vec{J} \cdot \vec{E}(x, y, z) \quad (3)$$

where \vec{J} is the current density and $\vec{E}(x, y, z)$ is the electric field distribution in a PDN. It should be noted that the chip power map (heat source) considered in the simulation is fixed. A temperature-dependent chip power map (e.g., leakage power of chips) can also be used in the formulation presented, which has not been included in the simulation.

The temperature-dependent electrical resistivity can be expressed as

$$\rho = \rho_0[1 + \alpha(T - T_0)] \quad (4)$$

where ρ_0 is the electrical resistivity at T_0 , which is 20 °C, and α is the temperature coefficient of electrical resistance. As shown in Figure 2a, with increasing temperature, the electrical resistivities of conductors increase and can eventually affect the voltage drop in a PDN. Because of the temperature-dependent electrical resistivity $\rho(x, y, z, T)$ and Joule heating generated in a PDN, the electrical and thermal characteristics couple to each other and form a nonlinear system, as shown in Figure 5.

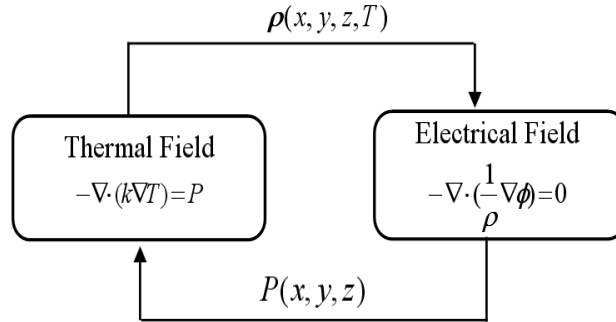


Figure 5. Relationship between electrical and thermal fields.

Obtaining an accurate voltage distribution in a PDN with temperature and Joule heating effects requires simultaneously solving the electrical-thermal equations (1-4). To account for the temperature and Joule heating effects, an iterative voltage drop-thermal co-simulation method has been developed, as shown in Figure 6.

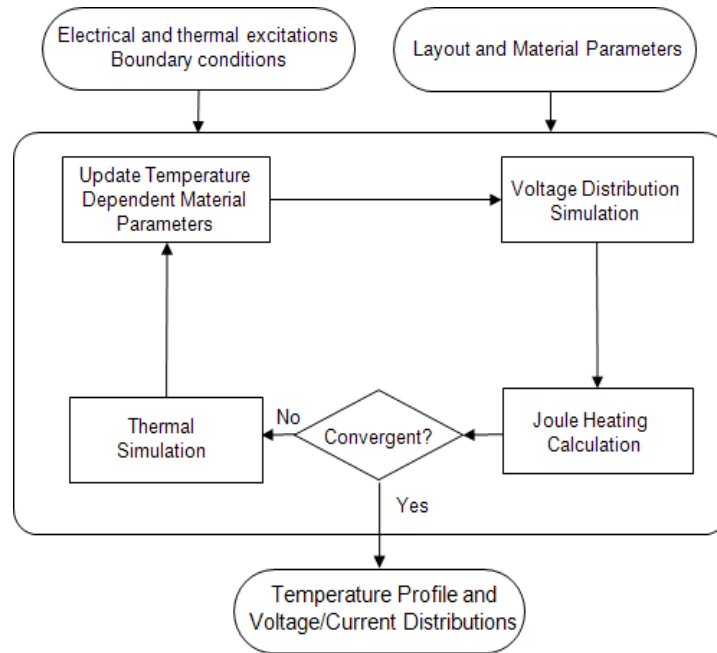


Figure 6. An iterative voltage drop-thermal co-simulation flow.

The iterative simulation technique consists of the following procedures:

1. Setting input information on layout parameters, initial material properties, excitations, and boundary conditions for the steady-state voltage drop and thermal analysis.
2. The steady-state voltage distribution simulation is carried out to obtain voltage and current distributions in a PDN.
3. Heat sources (Joule heat) are calculated from the obtained voltage and current distributions.
4. By updating the Joule heat excitation, the steady-state thermal simulation is carried out to obtain the temperature distribution of the system.
5. Based on the temperature distribution obtained, the electrical resistivities of conductors in a PDN are updated; thereby, the thermal effect on voltage drop is included.

6. The convergence of temperature and voltage distributions is determined. The final thermal and voltage distributions are obtained if convergence is reached; else, the iterations are continued.

For establishing an iterative co-simulation procedure, the voltage-distribution equation (1) with temperature-dependent resistivities and the thermal equations (2a) and (2b) with Joule heating effect need to be solved. In general, the Joule heating generated by the PDN in an electronic system can cause limited temperature increases and convergence can be achieved. However, for designs without careful considerations, the Joule heating can cause sharp temperature increases that lead to non-convergence, which can also be captured using the iterative electrical-thermal co-simulation method. To efficiently update the distributions of temperature, Joule heat, and voltage drop, the same mesh grids need to be used for both the voltage drop and thermal simulations. As a 3D system contains large-sized planes and small-sized structures such as TSVs, C4s, and apertures, 3D nonuniform mesh grids are required to reduce the number of unknowns, to reduce the simulation time, and also to accurately capture all geometries. In the next section, the numerical schemes based on the finite volume method are introduced using nonuniform rectangular grids.

3.2.2 Finite-Volume Schemes

The formulations for solving the DC voltage drop and heat equations are discussed in this section. Although 3D nonuniform rectangular grids are used in the simulation, the finite-volume formulation is explained on 2D nonuniform grids for simplicity.

3.2.2.1 Voltage Distribution Equation

The formulation for solving the voltage-distribution equation (1) is performed using the temperature-dependent resistivity. The 2D rectangular mesh for computing the voltage distribution is shown in Figure 7. In Figure 7, $\phi_{i,j}$ represents the voltage at grid point (i, j) , which is surrounded by four nodes. $\Delta x_1, \Delta x_2, \Delta y_1$, and Δy_2 are the nodal distances between node (i, j) and its adjacent nodes in x and y directions, respectively. It is assumed that the four surrounding cells of node (i, j) have different temperatures T_1, T_2, T_3 , and T_4 , which can be obtained from the thermal simulation.

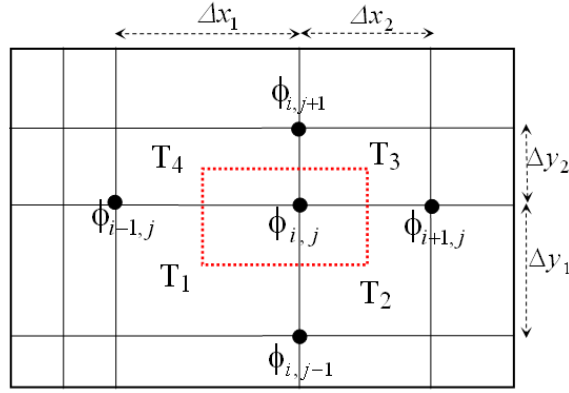


Figure 7. A 2D rectangular mesh for computing voltage distribution.

To apply the finite volume method, node (i, j) is surrounded by a finite-volume cell (dashed line) in Figure 7. The intersection points between the dashed cell and other four cells are the center points of each cell. By integrating Equation (1) over the dashed cell and applying the divergence theorem, we obtain

$$\int_{\text{dashed line}} \frac{1}{\rho(x, y, z, T)} \nabla \phi(x, y, z) \cdot \hat{n} dl = 0 \quad (5)$$

where \hat{n} is the outward pointing unit normal vector at the boundary of the dashed cell.

Initially, the temperature distribution is assumed uniform; thus, the electrical resistivity $\rho(x, y, z, T)$ is a constant. By applying the finite-difference approximation to the first-order derivative of ϕ in Equation (5), the finite-volume scheme at node (i, j) can be obtained as

$$\frac{\phi_{i,j} - \phi_{i-1,j}}{\frac{\rho \Delta x_1}{d}} + \frac{\phi_{i,j} - \phi_{i+1,j}}{\frac{\rho \Delta x_2}{d}} + \frac{\phi_{i,j} - \phi_{i,j-1}}{\frac{\rho \Delta y_1}{w}} + \frac{\phi_{i,j} - \phi_{i,j+1}}{\frac{\rho \Delta y_2}{w}} = 0 \quad (6)$$

where $w = (\Delta x_1 + \Delta x_2)/2$ and $d = (\Delta y_1 + \Delta y_2)/2$. Note that the finite-volume scheme of Equation (6) is analogous to the Kirchhoff's current law.

To include the temperature effect on voltage distribution, the temperature distribution $T_1, T_2, T_3,$ and T_4 in the surrounding cells are considered. Finally, the finite-volume scheme with the temperature-dependent resistivity is generalized as

$$\left(\frac{\Delta y_1}{\rho(T_1) \Delta x_1} + \frac{\Delta y_2}{\rho(T_4) \Delta x_1} \right) (\phi_{i,j} - \phi_{i-1,j}) + \left(\frac{\Delta y_1}{\rho(T_2) \Delta x_2} + \frac{\Delta y_2}{\rho(T_3) \Delta x_2} \right) (\phi_{i,j} - \phi_{i+1,j}) + \left(\frac{\Delta x_1}{\rho(T_1) \Delta y_1} + \frac{\Delta x_2}{\rho(T_2) \Delta y_1} \right) (\phi_{i,j} - \phi_{i,j-1}) + \left(\frac{\Delta x_1}{\rho(T_4) \Delta y_2} + \frac{\Delta x_2}{\rho(T_3) \Delta y_2} \right) (\phi_{i,j} - \phi_{i,j+1}) = 0 \quad (7)$$

3.2.2.2 Heat Equation for Solid Media

In thermal simulation, the thermal conductivity k is considered as a constant. For heat transfer in a solid medium, only heat conduction needs to be considered. As the heat equation (2a) has the same form as Equation (1), the same finite-volume formulation can be applied. The scheme for heat conduction can be obtained as [16]

$$\frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x_1}{kd}} + \frac{T_{i,j} - T_{i+1,j}}{\frac{\Delta x_2}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{kw}} + \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{kw}} = P_{\text{total}} \quad (8)$$

where $P_{total} = \iint_{dashed\ cell} -P(x, y, z)dS$ is the total heat excitation in the dashed cell.

To obtain an accurate temperature distribution of a realistic system, the convection boundary condition

$$k \frac{\partial T}{\partial n} \Big|_{convection} = -h_c(T - T_a) \quad (9)$$

needs to be taken into account. In Equation (9), T_a and h_c represent the ambient temperature and convection coefficient, respectively. The finite-volume formulation procedure can also be applied at the convection boundary with nonuniform mesh grids, as shown in Figure 8. In Figure 8, node (i, j) at the convection boundary is surrounded by a finite-volume cell (dashed line). By integrating Equation (2a) over the dashed cell and applying the divergence theorem, we obtain

$$\int_{dashed\ line} k(x, y, z) \nabla T(x, y, z) \cdot \hat{n} dl = \iint_{dashed\ cell} -P(x, y, z) dS \quad (10)$$

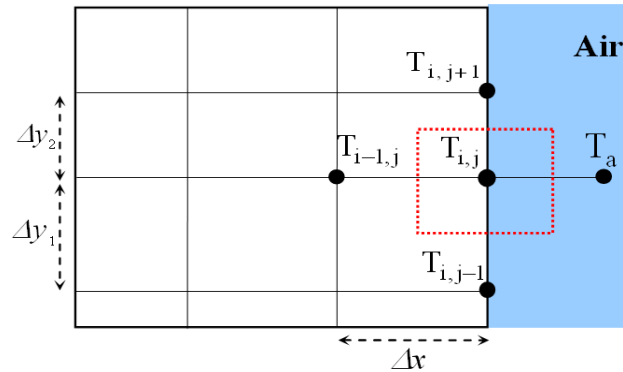


Figure 8. A convection boundary with nonuniform mesh grids.

Then, by applying the finite-difference approximation to the first-order derivative of $T(x, y, z)$ in Equation (10) and incorporating Equation (9), the finite-volume scheme for heat equation with a convection boundary condition at node (i, j) can be expressed as

$$\frac{T_{i,j} - T_a}{\frac{1}{h_c d}} + \frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{k\Delta x/2}} + \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{k\Delta x/2}} = P_{total} \quad (11)$$

where $d = (\Delta y_1 + \Delta y_2) / 2$.

3.2.2.3 Heat Equation for Fluid Flow

For a fluid-cooled integrated system, the modeling of fluidic cooling is required. For fluidic cooling using built-in microchannels (Figure 1), as the cross-sectional dimension of a microchannel is much smaller than its length, the flow velocity along the longitudinal direction is much larger than that in the lateral direction. Therefore, it can be assumed that the fluid only flows in the longitudinal direction and the flow velocity is constant. The 2D nonuniform mesh of a microchannel inside a chip is shown in Figure 9. The average flow velocity ‘ v ’ along the y direction has been used for simulating the fluid flow in microchannels. As a result, Equation (2b) can be converted as

$$\sigma c_p v \frac{\partial T(x, y, z)}{\partial y} = \nabla \cdot (k_f \nabla T(x, y, z)) \quad (12)$$

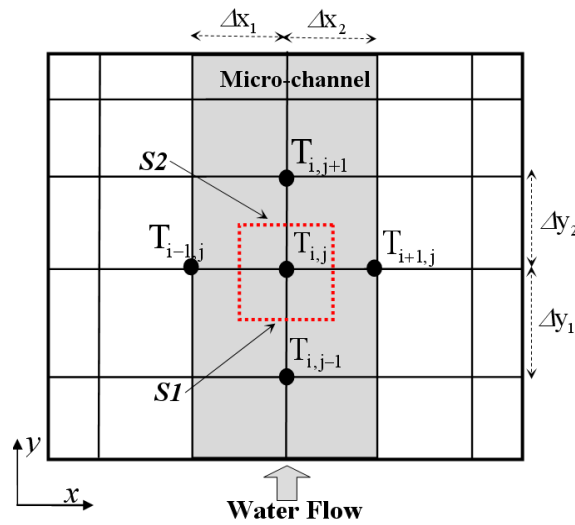


Figure 9. Nonuniform mesh grids for simulating a microchannel in a chip.

By integrating Equation (12) over the dashed cell in Figure 9 and applying the divergence theorem, Equation (12) becomes

$$\int_{S1+S2} \sigma c_p v T \hat{y} \cdot \hat{n} dl = \int_{dashed\ line} k_f \nabla T \cdot \hat{n} dl \quad (13)$$

where $S1$ and $S2$ are the upper and bottom boundaries of the dashed cell, as shown in Figure 9. For the right-hand side of Equation (13), the same formulation for a solid medium can be used. For the left-hand side, since the central finite-difference scheme can generate instability in certain cases [16], the backward difference approximation is used. The finite-volume scheme for fluid flow can be derived as

$$\frac{T_{i,j} - T_{i-1,j}}{\frac{\Delta x_1}{kd}} + \frac{T_{i,j} - T_{i+1,j}}{\frac{\Delta x_2}{kd}} + \frac{T_{i,j} - T_{i,j-1}}{\frac{\Delta y_1}{kw}} + \frac{T_{i,j} - T_{i,j+1}}{\frac{\Delta y_2}{kw}} = \sigma c_p v (T_{i,j} - T_{i,j-1}) \quad (14)$$

where $w = (\Delta x_1 + \Delta x_2)/2$ and $d = (\Delta y_1 + \Delta y_2)/2$.

As the average flow velocity along the longitudinal direction is used in the model, the heat transfer coefficient h needs to be applied at the boundaries of microchannels to model the heat transfer between the solid medium and the fluid flow. The effect of this boundary condition is important since eliminating it can cause incorrect chip temperatures [75]. For water flow in microchannels, the Reynolds number is usually less than 2300; thus, the flow is laminar [77]. For a fully developed laminar flow inside rectangular microchannels with constant heat flux, the Nusselt number can be expressed as [77]

$$Nu = 8.235 \left(1 - \frac{2.0421}{\alpha} + \frac{3.0853}{\alpha^2} - \frac{2.4765}{\alpha^3} + \frac{1.0578}{\alpha^4} - \frac{0.1861}{\alpha^5} \right) \quad (15)$$

where α is the aspect ratio of a rectangular microchannel.

The average heat transfer coefficient h can be obtained analytically from the Nusselt number and expressed as

$$h = Nu \cdot k / D_h \quad (16)$$

where D_h is the hydraulic diameter of a microchannel [76]. The same formulation for air convection boundaries in the last subsection can be used to model the water convection boundary between the solid medium and water flow.

Based on the aforementioned finite-volume schemes for the voltage-distribution equation, heat equation for solid media, and heat equation for fluid flow, a steady-state voltage drop-thermal co-simulation solver “*PowerET*” has been developed. This solver has been used to simulate voltage distribution and thermal distribution with Joule heating, air convection, and fluidic cooling effects. Several numerical test cases are discussed in the following section.

3.2.3 Numerical Test Cases

3.2.3.1 Model-Verification Examples

To verify the correctness and accuracy of the models for heat conduction, air convection, and Joule heating, a PCB example has been simulated. In addition, two examples of microfluidic cooling have been simulated to validate the finite-volume thermal model for microfluidic cooling.

A. A PCB example with Joule heating effect

A two-layer PCB with the size of 10 cm × 5 cm is shown in Figure 10. A 2.5 V voltage source is placed at one end of the top power plane. Uniform current flows from the voltage source to the current sink, which is placed at the other end of the board. The

thicknesses of copper plane and dielectric layer are $36 \mu\text{m}$ and $350 \mu\text{m}$, respectively. Air convection is applied to both the top and bottom surfaces of the board. In this example, the thermal conductivity of the dielectric layer is $0.8 \text{ W}/(\text{mK})$.

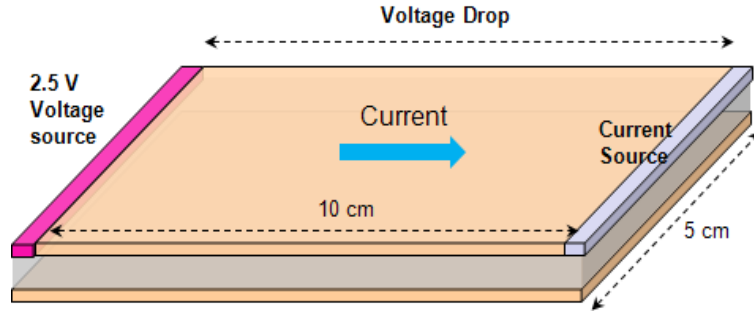


Figure 10. A PCB with rectangular planes.

Because of the rectangular shape of the power plane, the voltage drop across the plane can be calculated using the analytical equation

$$\Delta V = IR = I \frac{\rho L}{S} \quad (17)$$

where L is the length and S is the cross-sectional area of the power plane. Because of Joule heating $P = I \cdot \Delta V$ generated from the Ohmic loss, the temperature of the PCB can increase. The PCB temperature can be obtained by

$$T = T_a + P \cdot R_{total} \quad (18)$$

where T_a is the ambient temperature of $25 \text{ }^\circ\text{C}$ and R_{total} is the total thermal resistance because of heat conduction and air convection.

Without the Joule heating effect, the analytical Equations (17) and (18) can be used to directly calculate the voltage drop and temperature for the power plane. With the Joule heating effect, the iterative classic Newton's method [78] has been used to obtain the voltage drop and temperature. This example has been simulated with and without the

Joule heating effect using the *PowerET* solver. The comparisons of simulated results and the results from the classic Newton's method and analytical equations are shown in Figure 11.

As shown in Figure 11, without the Joule heating effect, the temperature of the power plane is kept at the constant room temperature of 25°C (Figure 11b). Therefore, the voltage drop increases linearly with increasing current, as shown in Figure 11a. However, with the effect of Joule heating under the condition of air convection with a heat transfer coefficient of $5\text{ W}/(\text{m}^2\text{K})$, we observe that the temperature increases nonlinearly with increasing current (Figure 11b). As a result, the voltage drop also increases nonlinearly with increasing current (Figure 11a). In addition, Figure 11 shows that the simulated results match well with the results from the analytical Equations (17-18) and classical Newton's method, indicating the accuracy of the proposed method.

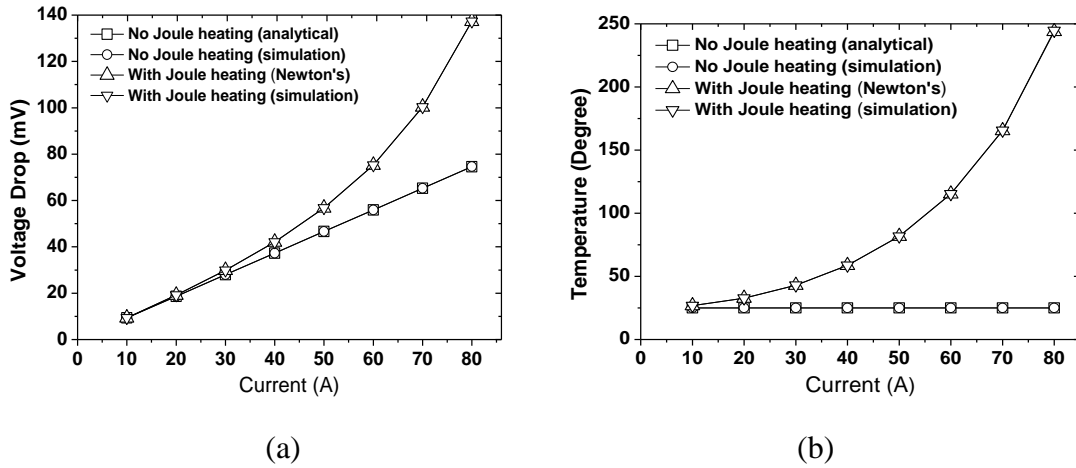


Figure 11. (a) Voltage drop and (b) temperature of the power plane with and without Joule heating effect.

B. An example of microfluidic cooling

To test the accuracy of the model for microfluidic cooling, an example of a single microchannel is simulated first. The microchannel and its cross-sectional view are shown

in Figure 12. The length of the microchannel is 20 mm, and the cross-sectional dimension is 0.12 mm \times 0.24 mm. The thermal conductivity of the bulk silicon is 150 W/(m \cdot K) as in [75]. The thickness of the cover is 0.05 mm, and its thermal conductivity is set to be 0.2 W/(m \cdot K). The heat flux density of 400000 W/m² is applied at the bottom of the silicon substrate. The temperature of the input water is set to be 20 $^{\circ}$ C. To test the convergence of the simulation, the cross-section of the microchannel is meshed with 2 \times 2, 4 \times 4, 8 \times 8, 16 \times 16, and 32 \times 32 cells (mesh level-1 to mesh level-5), respectively.

With a flow rate of 14.4 mg/s (0.864 ml/min), the simulated average outlet temperature of the microchannel and average base temperature of the substrate with different cross-sectional mesh refinements are shown in Figure 13. It shows that both the microchannel outlet temperature and base temperature converge with cross-sectional mesh refinement. As shown in Figure 13, using 4 \times 4 meshed cells (mesh level-2) for the cross-section of the microchannel, the average microchannel outlet temperature and base temperature are 46.070 $^{\circ}$ C and 41.93 $^{\circ}$ C, respectively. Compared to the final converged outlet temperature and base temperature of 46.074 $^{\circ}$ C and 42.17 $^{\circ}$ C, the errors for the average microchannel outlet temperature and base temperature are both less than 1%. Therefore, using 4 \times 4 meshed cells to represent the microchannel cross-section is adequate to obtain accurate results for this example. Using 4 \times 4 meshed cells for the microchannel cross-section, this example is also simulated with different flow rates ranging from 5.76 mg/s (0.3456 ml/min) to 28.8 mg/s (1.728 ml/min). The simulated average base temperatures of the bulk silicon, the CFD simulation results using COMPACTTM, and the analytical results reported in [75] are shown in Figure 14. From Figure 14, we observe that the simulated results from the *PowerET* solver agree well with

the CFD simulation results using COMPACTTM and the analytical results in [75]. Compared to the simulated temperatures using COMPACTTM, the maximum error is less than 6%, showing the accuracy of the presented method.

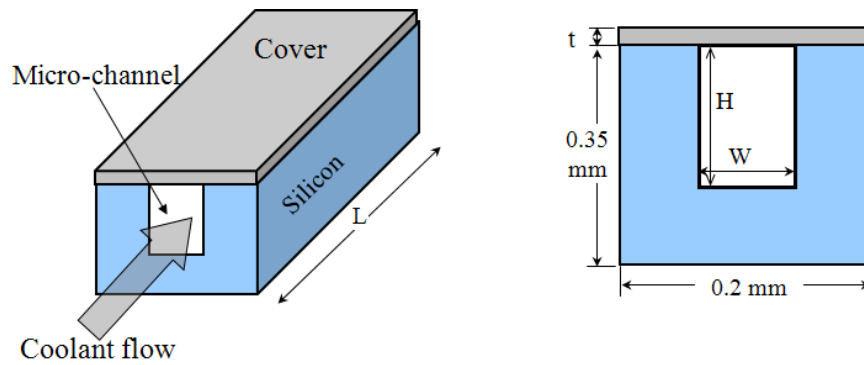


Figure 12. A microchannel and its cross-section.

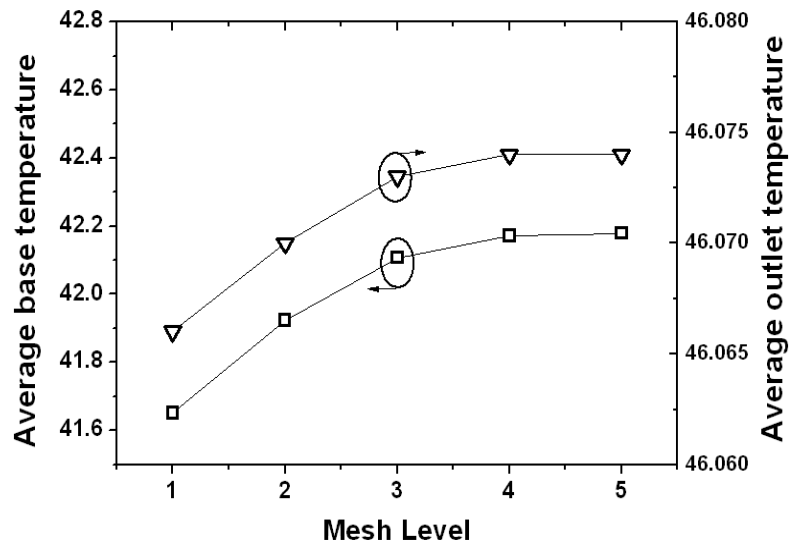


Figure 13. Average outlet temperature of the microchannel and base temperature of the bulk silicon with mesh refinement (unit: Celsius).

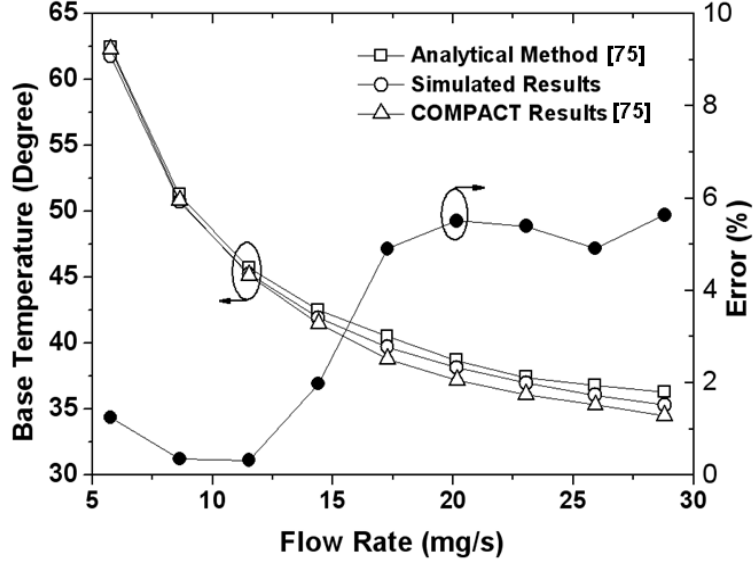


Figure 14. Average base temperatures of the bulk silicon with different flow rates.

C. An experimental example

An experimental test vehicle consisting of a silicon chip with fluidic cooling using microchannels has been described in [4]. To verify the finite-volume model for microfluidic cooling against measured results, the test vehicle of microfluidic cooling in [4] has been simulated. The structure is shown in Figure 15. The chip size is $1 \text{ cm} \times 1 \text{ cm}$, and the power consumption is 45 W . A total of 51 microchannels are uniformly distributed on the chip as described in [4]. The cross-sectional dimension of each microchannel is $0.1 \text{ mm} \times 0.2 \text{ mm}$. A Pyrex glass cover plate is placed on the top of the microchannels. Natural air convection with a convection coefficient of $5 \text{ W}/(\text{m}^2\text{K})$ is applied to both the top and bottom surfaces of the package. The thermal conductivity of the chip is set to be $110 \text{ W}/(\text{mK})$. The temperature of water at the inlets of microchannels is $22 \text{ }^\circ\text{C}$, and the heat capacity of water c_p is set to be $4180 \text{ J}/(\text{Kg} \cdot \text{K})$. The material thicknesses and thermal conductivities are listed in Table 1.

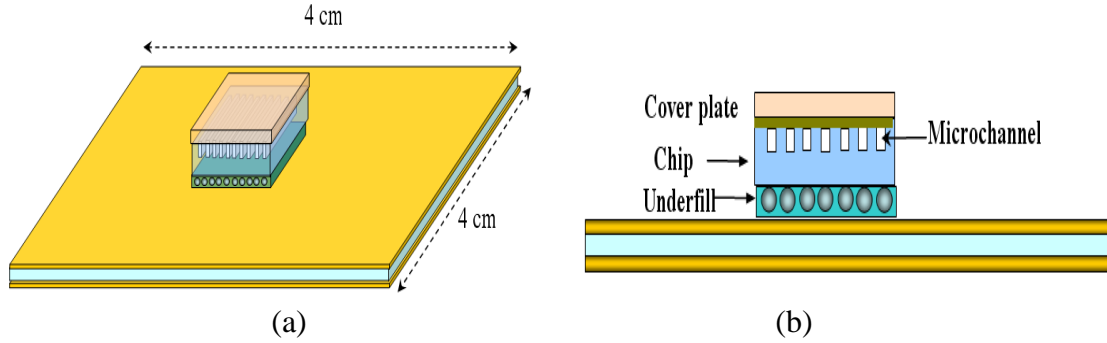


Figure 15. A package with microfluidic cooling, (a) system view, (b) cross-sectional view.

Table 1. Material thicknesses and thermal conductivities for the experimental example.

	Thickness (mm)	Thermal Conductivity (W/mK)
Substrate	0.35	0.8
Copper	0.036	400
Chip	0.3	110
Underfill	0.2	4.3
C4	0.2	60
Microchannel	0.2	0.6
Pyrex glass	0.1	1.1
Channel pitch	0.094	—

A 3D nonuniform mesh has been used to approximate the chip, underfill layer, substrate, and microchannels. For each microchannel, the cross-section is meshed using 4×4 cells, as shown in Figure 16. This test vehicle has been simulated with different water flow rates. The comparisons of the simulated and measured average outlet temperatures of the microchannels and average chip temperatures are plotted in Figure 17. As shown in the figure, with the water flow rates of 65 and 104 ml/min, the differences between the simulated average outlet temperatures and measurements [4] are 0.1 and 0.28 °C, respectively. The relative error is less than 4.5% for the outlet temperature. For the average chip temperature, with water flow rates of 65 and 104

ml/min, the temperature differences between the simulation and measurements are 2.6 and 1.7°C, respectively, as shown in Figure 17. Considering the inlet temperature as the basis, the calculated corresponding errors are 13.7% and 13.9%, respectively. The relative larger error for the average chip temperature may be caused by the average heat transfer coefficient h used in the model for fluidic cooling.

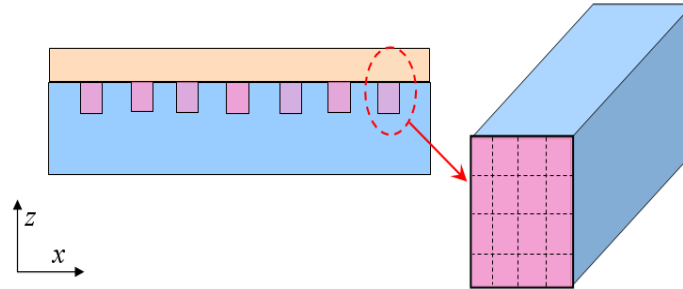


Figure 16. Cross-sectional mesh of a microchannel.

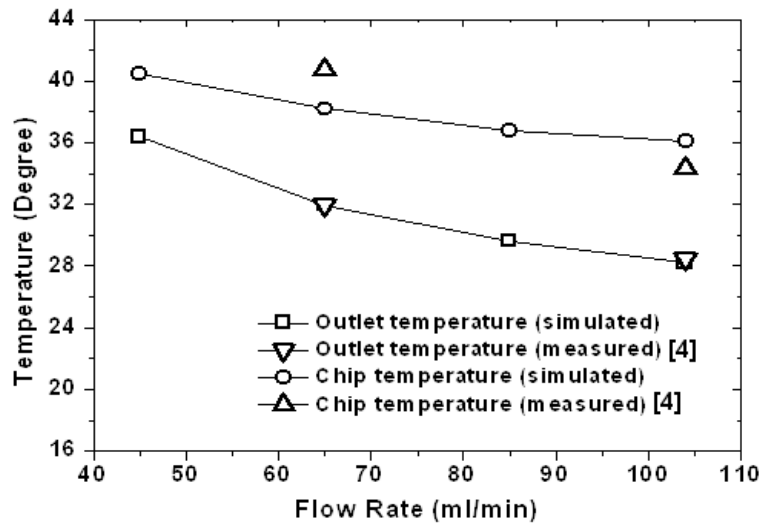
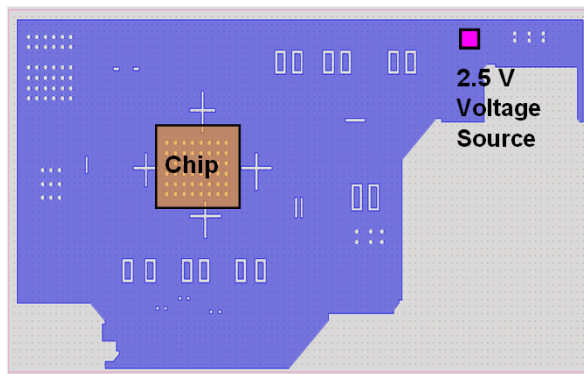


Figure 17. Average outlet temperature and average chip temperature using simulation and measurements.

3.2.3.2 A Practical Design Example

In an IC package or a printed circuit board, a PDN usually has an irregular shape with many voids and apertures. To simulate practical designs, a new interface that can import board and package design files from *Cadence SPB* software into the *PowerET* solver has

been employed. A PCB example is shown in Figure 18a. In Figure 18a, the board dimension is $60 \text{ mm} \times 31 \text{ mm}$, and the chip dimension is $9 \text{ mm} \times 9 \text{ mm}$. The total power consumption of the chip is 50 W , and its nonuniform power map is illustrated in Figure 18b. The thermal conductivity of thermal interface material (TIM) is $2 \text{ W}/(\text{mK})$. The heat sink is modeled as an ideal heat sink with a constant room temperature of $25 \text{ }^\circ\text{C}$. This example has been simulated with a convection coefficient of $5 \text{ W}/(\text{m}^2\text{K})$ on both sides of the board. The voltage drop simulation is carried out first with an initial system temperature of 25 Celsius . The simulated voltage and temperature of the chip with electrical-thermal iterations are shown in Figure 19. It shows that compared to the initial voltage drop of 15 mV , the final voltage drop increases to 18.2 mV . Therefore, the thermal effect on voltage drop is 21.3% . Because of the power density from the chip and Joule heat from the PDN, the final chip temperature increases to $92.1 \text{ }^\circ\text{C}$. It is important to note that in this example, the chip temperature increase is mainly caused by the power density of the chip. Since on-chip power grids are not included in the simulation, the Joule heat generated in the PCB only increases the chip temperature by $0.3 \text{ }^\circ\text{C}$. The final temperature and voltage distributions of the board are shown in Figure 20.



(a)

2.5	3	2.5	2.5
3	4	3.5	3
3	4	4	3
2.5	3.5	3	3

(b)

Figure 18. (a) A board example, (b) a nonuniform chip power map (unit: W).

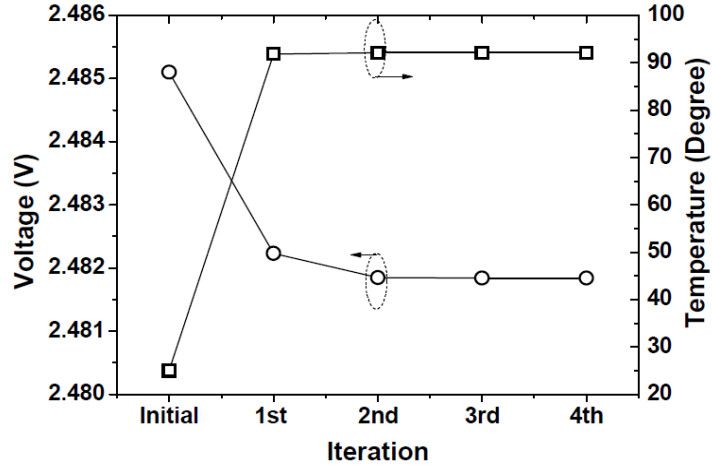


Figure 19. The voltage and temperature of chip with electrical-thermal iterations.

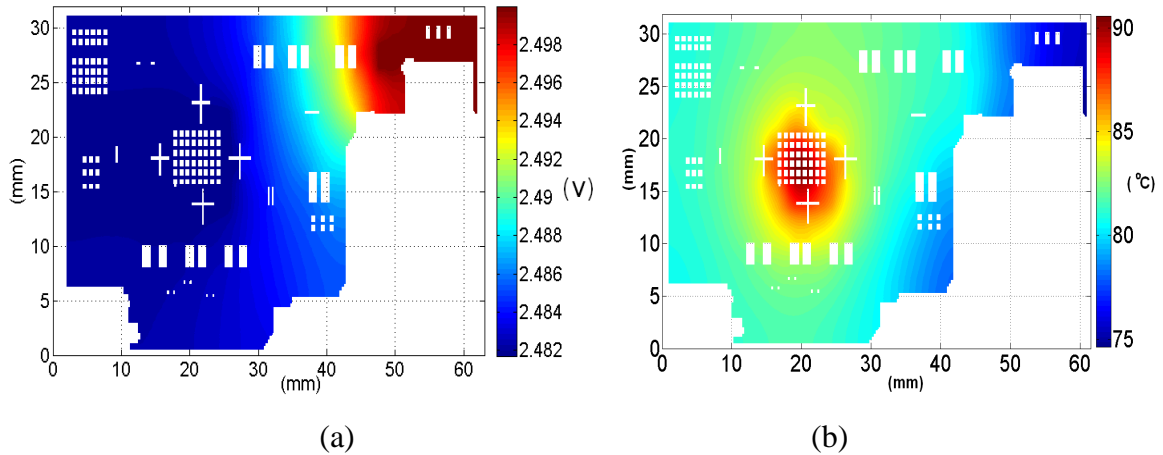


Figure 20. Final voltage and temperature distributions of the board, (a) voltage, (b) temperature.

3.2.3.3 A 3D System with Microfluidic Cooling

A 3D integrated system with microfluidic cooling is also simulated using the *PowerET* solver. The 3D integrated system consists of two sets of stacked chips, 36 microchannels, hundreds of TSVs, C4s, and a package substrate. The structure of the system is shown in Figure 21a. The package has five metal layers: two signal layers, two power plane layers, and one ground plane layer, as shown in Figure 21b. The two power plane layers are shorted together using multiple vias to reduce the voltage drop. A 2.5 V

voltage source is placed at the corner of the package. In each set of stacked chips, the top chip is stacked on the bottom chip using TSVs and micro-bumps. The package size is 20 cm \times 20 cm, and the size of each chip is 1.1 cm \times 1.1 cm.

In this 3D integrated package, the power consumptions for Chip1, Chip2, Chip3, and Chip4 are 100 W, 100 W, 50 W, and 50 W, respectively. Uniform power maps are used for all chips. To efficiently dissipate heat for this high-power 3D system, the method of microfluidic cooling is used with chilled water, as shown in Figure 21. In each chip, nine microchannels with a cross section of 0.6 mm \times 0.2 mm are used. The configuration of microchannels and TSVs of the stacked chips is shown in Figure 22. The geometrical and material parameters are summarized in Table 2.

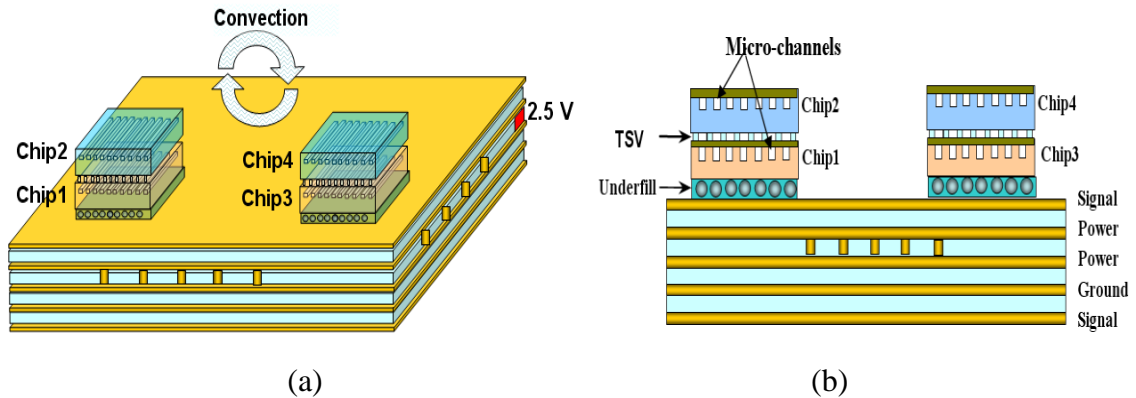


Figure 21. A 3D integrated system with microfluidic cooling, (a) whole system, (b) cross-sectional view.

Air convection with a heat transfer coefficient of $5 \text{ W}/(\text{m}^2\text{K})$ is applied to both the top and bottom surfaces of the package. This example is simulated with both Joule heating and fluidic cooling effects. In the simulation, four chips are supplied with the same water flow rate. The temperature of input water at the inlets of microchannels is 22°C . To validate the effect of fluidic cooling, the traditional cooling method using a heat sink is also simulated for comparison. The thermal conductivity of TIM is $2.4 \text{ W}/(\text{mK})$,

and the heat sink is assumed to be an ideal heat sink with a constant room temperature of 25°C . In the simulation, 3D nonuniform rectangular grids are used, resulting in about 166 K unknowns for the thermal simulation. For the voltage distribution simulation, since only conductor cells are considered as unknowns in the simulation, only 110 K unknowns are used. The simulation took five iterations to converge. The total simulation time was 401.4 seconds.

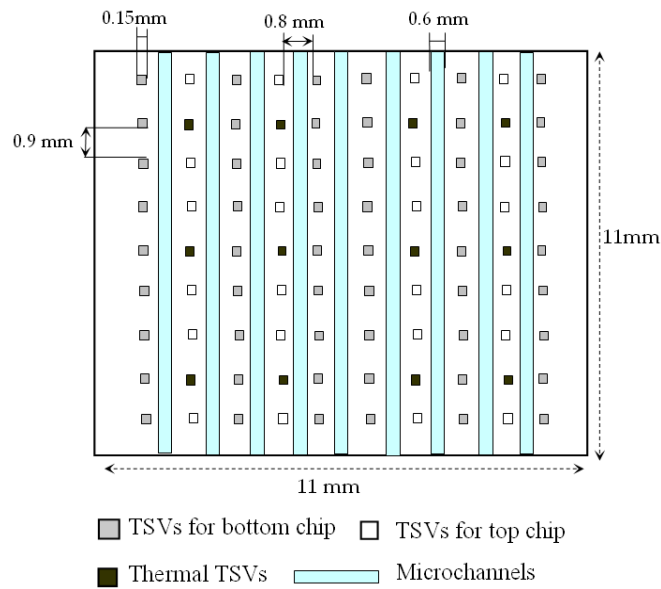


Figure 22. The configuration of microchannels and TSVs for stacked chips.

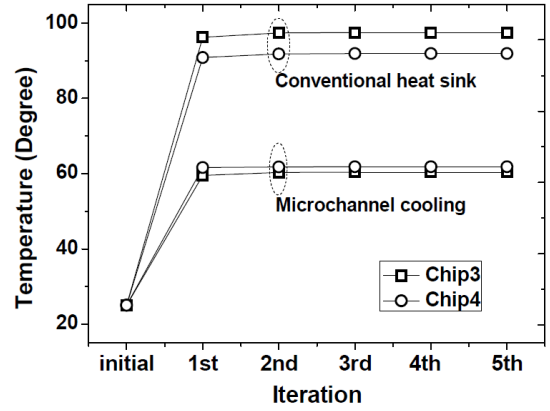
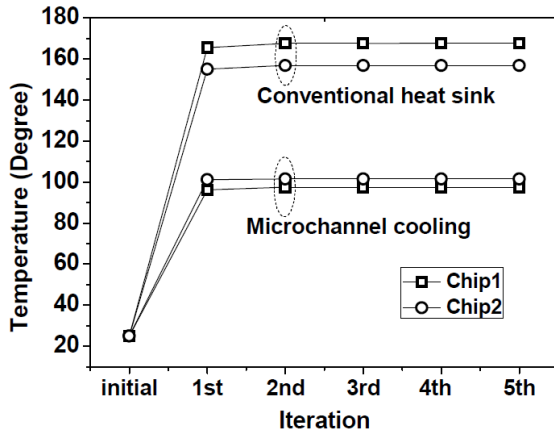
Table 2. Geometrical and material parameters.

	Material Thickness (mm)	Thermal Conductivity (W/mK)
Glass-ceramic	0.35	5
Copper	0.036	400
Chip	0.5	110
Underfill	0.2	4.3
C4	0.2	60
TIM	0.2	2.4
TSV (Tungsten)	0.5	174
Microchannel	0.2	0.6

With a water flow rate of 104 ml/min for each chip, the simulated temperatures using the microfluidic cooling and traditional heat sink are shown in Figure 23. It shows the simulated results converge in five iterations. As can be seen from Figure 23, using the heat sink, the final temperatures of Chip1, Chip2, Chip3, and Chip4 are 167.6°C , 156.8°C , 97.5°C , and 91.9°C , respectively. However, using the microfluidic cooling, their temperatures become 97.5°C , 101.5°C , 60.3°C , and 61.8°C , respectively. Therefore, the microfluidic cooling can greatly reduce the temperature for high-power 3D stacked ICs.

The simulated voltages with the microfluidic cooling and traditional heat sink are shown in Figure 24. The initial voltage drops of Chip1, Chip2, Chip3, and Chip4 are 78.8 mV, 83.2 mV, 60.9 mV, and 63.2 mV, respectively. Using the traditional heat sink, the final voltage drops of Chip1, Chip2, Chip3, and Chip4 are 102.5 mV, 109.6 mV, 75.8 mV, and 78.7 mV, respectively. Therefore, the thermal effect increases the voltage drops of Chip1, Chip2, Chip3, and Chip4 by 30%, 32%, 24%, and 25%, respectively. However, with the microfluidic cooling, the thermal effects only increase the voltage drops of Chip1, Chip2, Chip3, and Chip4 by 20%, 20%, 18%, and 18%, respectively. As the microchannel-based fluidic cooling can reduce the chip temperatures to less than 102°C for Chip1 and Chip2 and less than 62°C for Chip3 and Chip4 (Figure 23), the thermal effect on the voltage drop is dramatically reduced compared to that using heat sink.

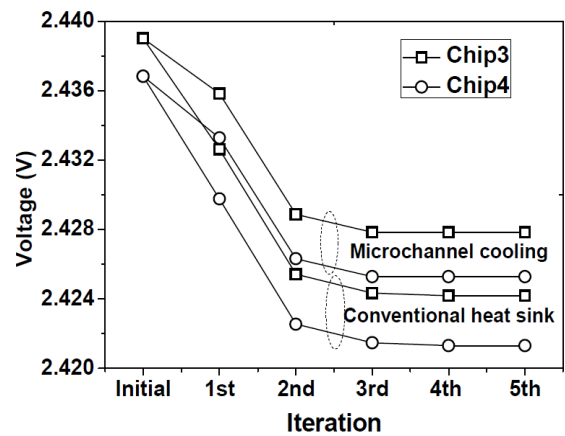
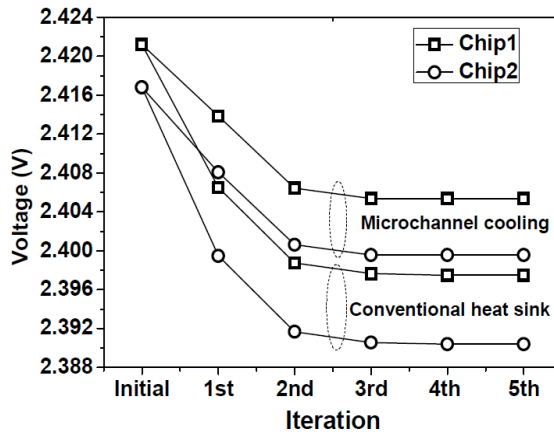
After establishing the convergence of the co-analysis, the final temperature distributions of chips and microchannels are shown in Figure 25. It shows that the chip temperature is much higher than the water temperature inside the microchannel. The large temperature gradient at the boundary is caused by the relative large power density of the chip and small heat transfer coefficient between the liquid water and silicon chip.



(a)

(b)

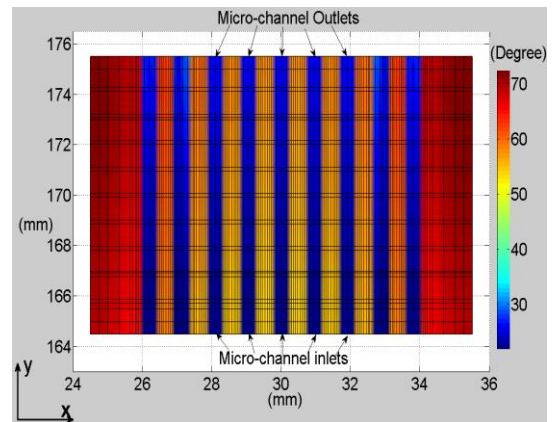
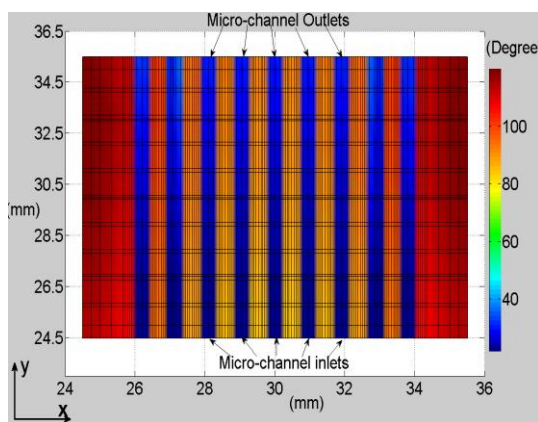
Figure 23. Temperatures of (a) Chip1 and Chip 2, (b) Chip3 and Chip4 with iterations.



(a)

(b)

Figure 24. Voltages of (a) Chip1 and Chip2, (b) Chip3 and Chip4 with iterations.



(a)

(b)

Figure 25. 2D temperature distributions of microchannels and chips, (a) Chip1, (b) Chip3 with a flow rate of 104 ml/min (top view).

3.3 Thermal-Electrical Analysis for TSV Arrays

As TSV interconnects become key components in 3D stacked chips and integrated systems, the modeling and design of TSV arrays becomes important for circuit designers. For the modeling of TSV arrays, the numerical modeling method using CMBFs (cylindrical modal basis functions) [69] has been a promising approach, for large TSV arrays can be efficiently modeled using a small number of basis functions. Because of the temperature-dependent electrical resistivity of silicon substrate and TSV filling materials (e.g., copper and tungsten), modeling TSV arrays in silicon carriers (Figure 1) requires taking into account the thermal effect on TSV characteristics (e.g., crosstalk and insertion loss). In this section, we present a thermal-electrical analysis method for TSV arrays. The proposed approach accounts for the temperature effect on TSV arrays by extending the TSV modeling method in [69] to include temperature-dependent material properties. The objective of the thermal-electrical analysis is to investigate the temperature effect on TSV characteristics such as crosstalk, insertion loss, *RLCG* parameters, and time-domain coupled noise.

3.3.1 Temperature Effects on Silicon Properties

Modeling a TSV array requires taking into account the temperature-dependent material properties of the silicon substrate and TSV filling material. The temperature-dependent electrical resistivity of TSV filling materials (e.g., copper and tungsten) is described by Equation (4). For a silicon interposer, its electrical conductivity is affected by the doping density and temperature T . The temperature-dependent silicon conductivity can be described by [71]

$$\sigma_{si}(T) = 1.602 \times 10^{-17} N_a \mu_p(T) (S/m) \quad (19)$$

where N_a represents the concentration of substrate dopant impurity and $\mu_p(T)$ represents the temperature-dependent carrier mobility [88].

To model a TSV array with temperature effects, the temperature-dependent metal conductivity $\sigma_m(T)$ ($\sigma_m = 1/\rho_m$) and silicon conductivity $\sigma_{si}(T)$ need to be used. In addition, because of the finite conductivity of silicon, which differs from other substrates such as glass ceramic and FR-4 substrates, a complex permittivity of silicon needs to be used and it is described by [89]

$$\varepsilon_{si}(T) = \varepsilon_0 \varepsilon_{si,i} \left(1 - j \tan \delta - j \frac{\sigma_{si}(T)}{\omega \varepsilon_0 \varepsilon_{si,i}} \right) \quad (20)$$

where $\varepsilon_{si,i}$ is the real part of the dielectric constant of silicon and $\tan \delta$ is the intrinsic loss tangent of an intrinsic silicon without doping; ω is the angular frequency.

3.3.2 Thermal-Electrical Analysis Flow for TSV Arrays

Because of the temperature-sensitive material properties, design and modeling of a TSV array requires taking into account the effect of a realistic system thermal profile. Capturing the thermal effect on a TSV array necessitates combined thermal-electrical modeling that consists of thermal modeling of a 3D system and electrical modeling of a TSV array. The thermal modeling enables obtaining the temperature distribution of the TSV array in a silicon interposer. The temperature distribution of the TSV array can be passed to the electrical model of the TSV array, accounting for the temperature effect. Although the thermal modeling can be performed with assumed boundary conditions surrounding the interposer region, the accuracy is limited because of the non-uniform power map and thermal coupling between adjacent regions and stacked dies. Therefore,

accurate temperature estimation requires thermal modeling of the 3D system consisting of the dies, interposer, and package.

The thermal-electrical modeling flow for TSV arrays is shown in Figure 26. The modeling starts with initial design parameters of the TSV array. In general, because of undetermined system layout, the thermal profile or temperature distribution of the system may not be available to circuit/TSV designers at the initial design stage. As a result, thermal analysis is required in the modeling flow. The thermal-electrical modeling procedure for TSV arrays is listed as follows:

- 1) Obtaining initial TSV array design parameters including TSV length, diameter, pitch, oxide liner thickness, material properties, etc.
- 2) Electrical modeling of the TSV array to obtain TSV *RLCG* parameters, crosstalk, and insertion losses at room temperature.
- 3) Deciding whether the crosstalk and insertion loss of the TSV are within the design budget or not. If not, go back to step 1 to adjust the TSV layout parameters. Otherwise, go to next step.
- 4) With updated layout parameters of the TSV array, thermal simulation of the system is carried out to obtain the temperature distribution across the interposer.
- 5) Electrical modeling of TSV array is carried out with updated temperature-dependent material properties. The temperature effect on the characteristics of the TSV array including *RLCG* parameters, crosstalk, and insertion loss can be obtained.
- 6) Deciding whether the new TSV array characteristics meet the design budget or not. If not, go back to step 1 to adjust TSV layout parameters and then go to step 4. Otherwise, multiport S-parameters and a Spice-based macromodel are generated.

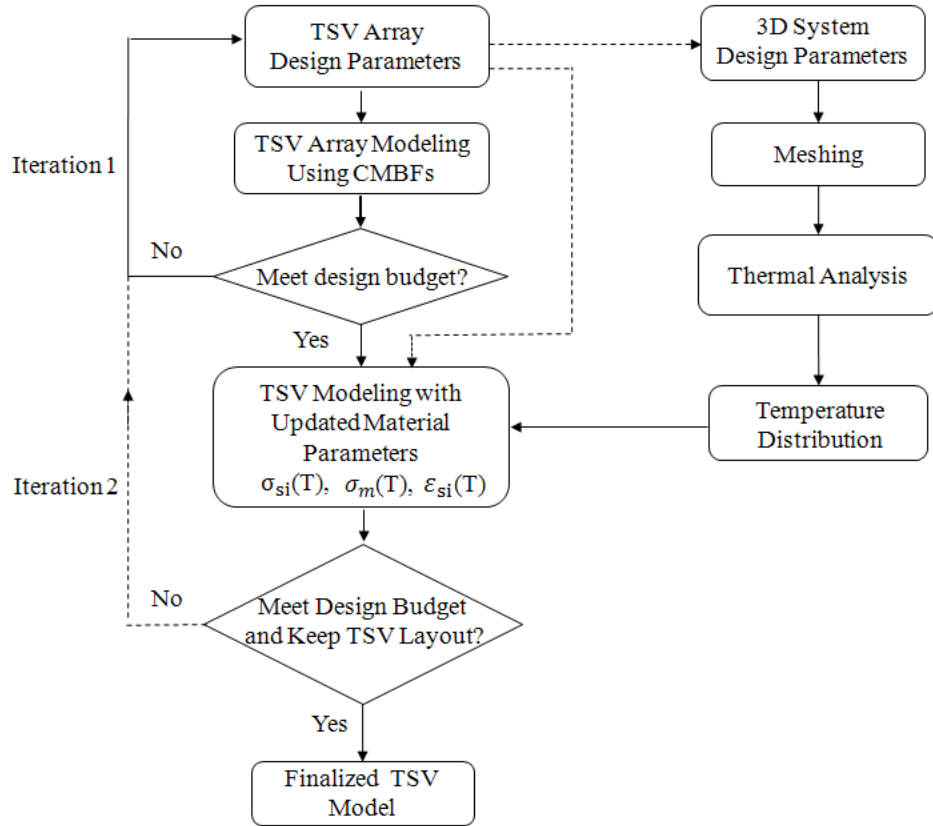


Figure 26. A thermal-electrical modeling flow for TSV arrays.

The conventional TSV array design and modeling consists of only steps 1-3 without considering the thermal profile of the system, which can introduce discrepancy. It is important to note that the thermal profile can also be calculated based on the initial TSV design parameters; thus, Steps 2 and 3 can be bypassed, as shown in Figure 26. However, using the initial design parameters may result in inaccurate temperature estimation. In the second iteration, to reduce the computational cost, the temperature estimation in the first iteration can also be used if limited geometrical modification is made for the TSV array.

The presented thermal-electrical co-analysis approach for TSV arrays is based on the combination of the electrical TSV modeling method using CMBFs and the thermal modeling using the FVM. For the electrical modeling of TSV arrays, we use the

numerical modeling method using cylindrical modal basis functions. As the modeling method using CMBFs has been discussed in detail in [69], the modeling process is omitted here for clarity. The method in [69] is extended to include temperature-dependent material properties by coupling with the thermal modeling.

For the thermal modeling of a 3D system, the aforementioned finite volume-based modeling method is used. The obtained temperature distribution can be passed to the electrical TSV model to update the temperature-sensitive electrical conductivities and permittivities of TSV conductors and the silicon substrate. The temperature effects on the insertion loss, crosstalk, *RLCG* parameters, and time-domain coupled noise of TSV arrays are investigated and shown using numerical test cases.

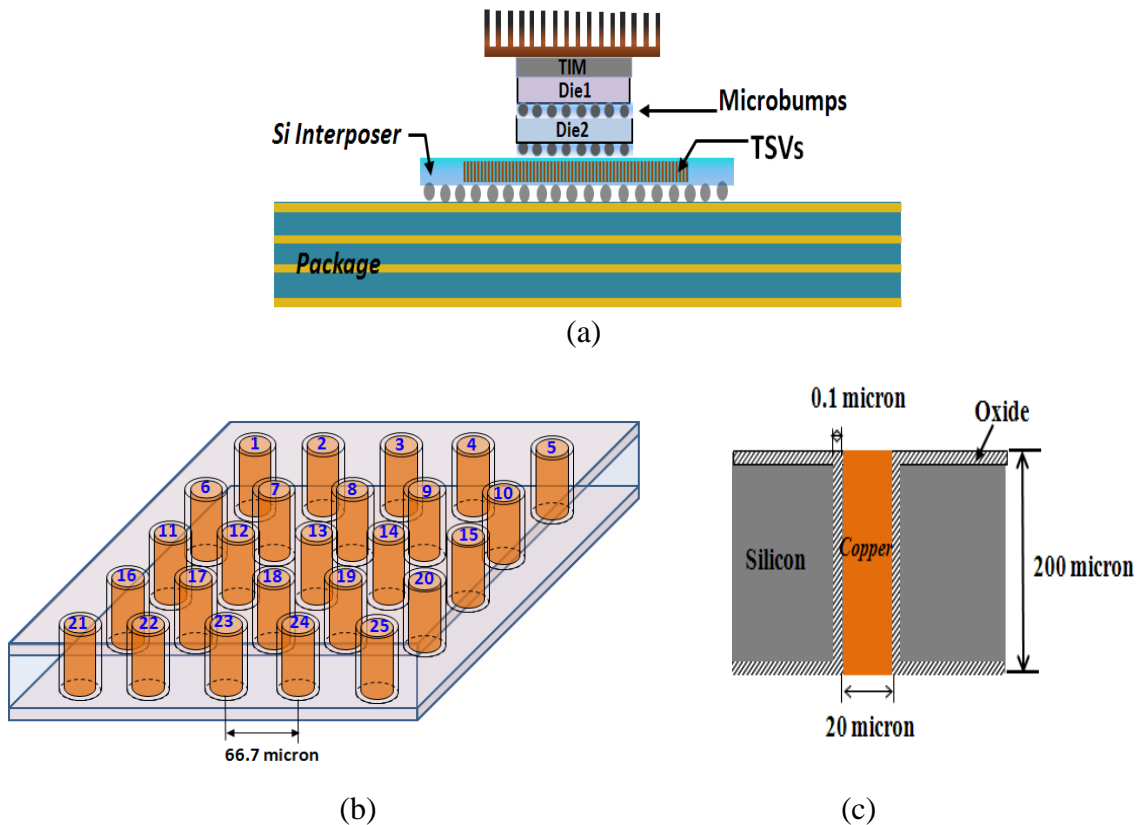


Figure 27. (a) A 3D system with a silicon interposer, (b) a 5 x 5 TSV array structure, (c) TSV cross-section.

3.3.3 Numerical Test Cases

A 3D system consisting of stacked dies, a thermal interface material, a four-layer package, micro-bumps, a silicon interposer, and an under-fill layer is simulated. The 3D system is shown in Figure 27a. The sizes of the stacked dies, silicon interposer, and package are $8\text{ mm} \times 8\text{ mm}$, $30\text{ mm} \times 30\text{ mm}$, and $60\text{ mm} \times 60\text{ mm}$, respectively. In the center of the silicon interposer, a TSV array consisting of 120×120 TSVs is distributed (Figure 27a). Among the 120×120 TSV array, a 5×5 TSV array, which is located at the center of the interposer, is shown in Figure 27b. The TSV diameter is 20 microns, and the pitch between TSVs is 66.7 microns. The cross-sectional view of a TSV is shown in Figure 27c. The TSV filling material is copper. The thicknesses of the interposer and oxide layer are $200\ \mu\text{m}$ and $0.1\ \mu\text{m}$, respectively. The conductivity of the silicon interposer is $10.4\ \text{S/m}$ at room temperature. The doping density of silicon interposer is $1.32 \times 10^{15}\ \text{cm}^{-3}$. The geometrical parameters and material thermal conductivities can be found in [90].

Two design cases are studied. In design Case-1, the power consumptions of die 1 and die 2 are 8 W and 2 W, respectively. In design Case-2, the power consumptions of die 1 and die 2 are 30 W and 12.5 W, respectively. The non-uniform power maps of dies are shown in Figure 28a and Figure 28b, respectively. Air convection with a convection coefficient of $10\ \text{W}/(\text{m}^2\text{K})$ is applied to the top surface of the silicon interposer and both sides of the package. The simulated temperature distributions of the silicon interposer for the two design cases are shown in Figure 29. As seen from Figure 29, because of the non-uniform die power map (Figure 28), the interposer temperature varies from 36.5 to 40.5 Celsius for Case-1 and from 76 to 92 Celsius for Case-2, respectively. Therefore, the

electrical modeling of the TSV array using material properties calculated at the room temperature can introduce discrepancy because of system temperature increases.

In a silicon interposer, the pitch between adjacent TSVs is usually in the range of 50-100 microns, depending on the process used. A 5×5 or 10×10 TSV array covers an area less than 1 mm^2 . Because of the high thermal conductivity of silicon interposer, the temperature variation across the 5×5 TSV array region is usually very small (less than one degree in our simulation). As a result, a single temperature (40 degree for Case-1 and 92 degree for Case-2 for this example) can be used for the 5×5 TSV array region, and the solution accuracy can still be maintained. Although the TSV modeling method using CMBFs [69] is applied to a 5×5 TSV array, the method can also be applied to larger TSV arrays because of the efficiency of the modeling methodology.

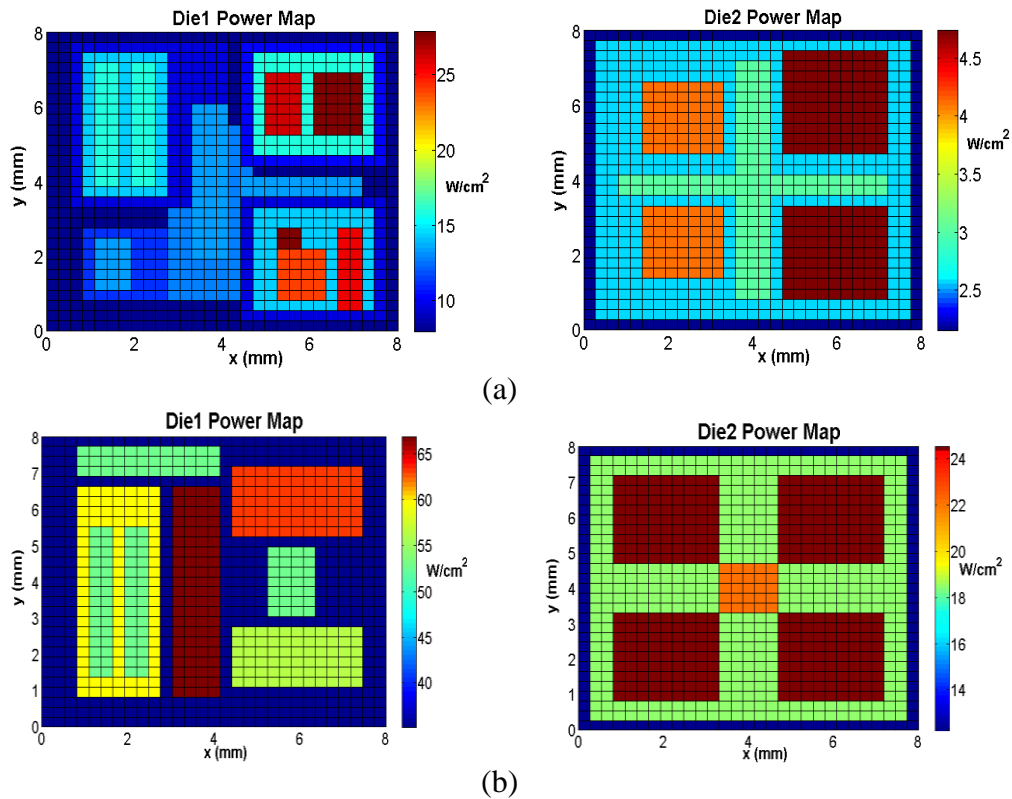


Figure 28. Power maps of dies for (a) Case-1, (b) Case-2.

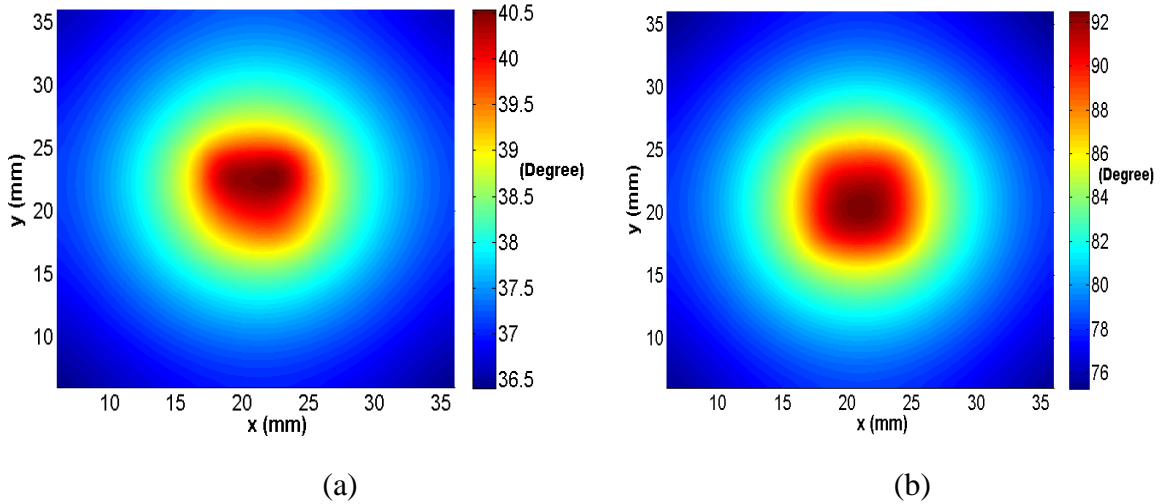


Figure 29. Temperature distribution across the interposer for (a) Case-1 design, (b) Case-2 design.

3.3.3.1 Temperature Effect on TSV Insertion Loss and Crosstalk

Using the initial TSV design parameters, the electrical modeling of the 5×5 TSV array (Figure 27b) is carried out first at room temperature of 25 Celsius. The simulated insertion loss and crosstalk of TSVs are shown in Figure 30 and Figure 31, respectively. As the temperature distribution is already simulated for the two cases, the material properties of the silicon interposer and TSV conductors can be updated, and the electrical modeling of the TSV array is carried out with updated material properties. For comparison purposes, the insertion loss and crosstalk with simulated temperatures (40 Celsius for design Case-1 and 92 Celsius for design Case-2) for the 5×5 TSV array are also shown in Figure 30 and Figure 31, respectively. It is observed that with updated temperatures of 40 and 92 Celsius, the insertion losses of TSV-1 and TSV-7 are reduced and more design budget is gained. As seen from Figure 30, the temperature effect on the insertion loss is not obvious up to 0.2 GHz. From 0.2 - 10 GHz, the insertion loss is

reduced with increasing temperature of the TSV array. This is caused by the reduced conductivity of the silicon interposer because of increasing temperature.

As shown in Figure 31, the temperature effect on TSV coupling shows frequency-dependent behavior regions. In low-frequency range, the near-end coupling between TSV-1 & TSV-2 and TSV-1 & TSV-7 increases with temperature. However, at higher frequencies (from 100 MHz to several GHz), the trend is reversed and better isolation is obtained with increasing temperature, which is due to the fact that the conductivity of the silicon substrate is reduced with increasing temperature, as indicated by Equation (19). As frequency further increases to 10 GHz, the coupling converges and the temperature effect cannot be observed. The same trend has been shown using measurements for a TSV pairs in [87]. The variations of TSV insertion loss and crosstalk caused by the temperature indicate the importance of taking into account the temperature effects on TSV arrays in real designs.

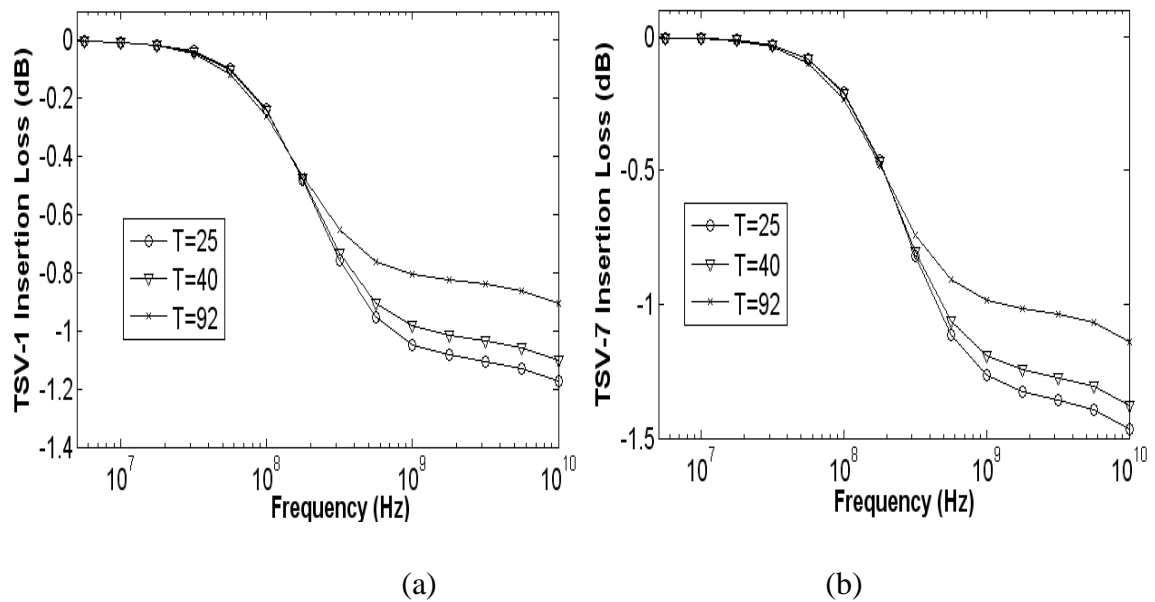
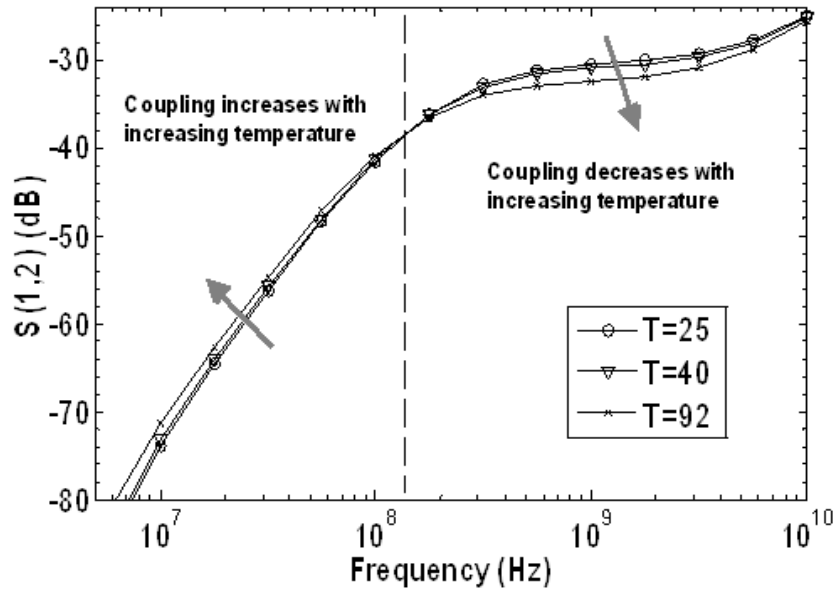
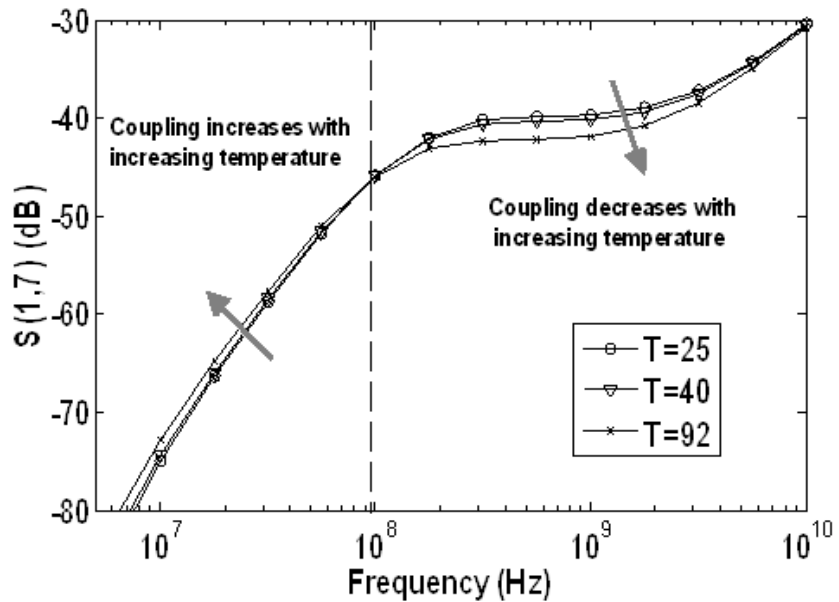


Figure 30. Insertion loss of (a) TSV-1, (b) TSV-7.



(a)



(b)

Figure 31. Near-end crosstalk between (a) TSV-1 & TSV-2, (b) TSV-1 & TSV-7 with initial and simulated temperatures.

3.3.3.2 Temperature Effect on TSV Self-parameters

The self-parameters of TSV-1 including series resistance, series inductance, shunt capacitance, and shunt conductance with initial and simulated temperatures are shown in

Figure 32(a-d), respectively. As shown in Figure 32a, with updated temperatures, the series resistance of TSV-1 increases linearly because of the temperature coefficient of the electrical resistance, which is 0.0039 K^{-1} for copper TSVs in this example. As seen from Figure 32b, at low frequencies, the temperature has no effect on series inductance because of the uniform current distribution inside TSV conductors. At higher frequencies, because of the skin effect that becomes significant around 0.1 GHz, the internal current distribution is affected by the temperature, resulting in a small variation of TSV inductance.

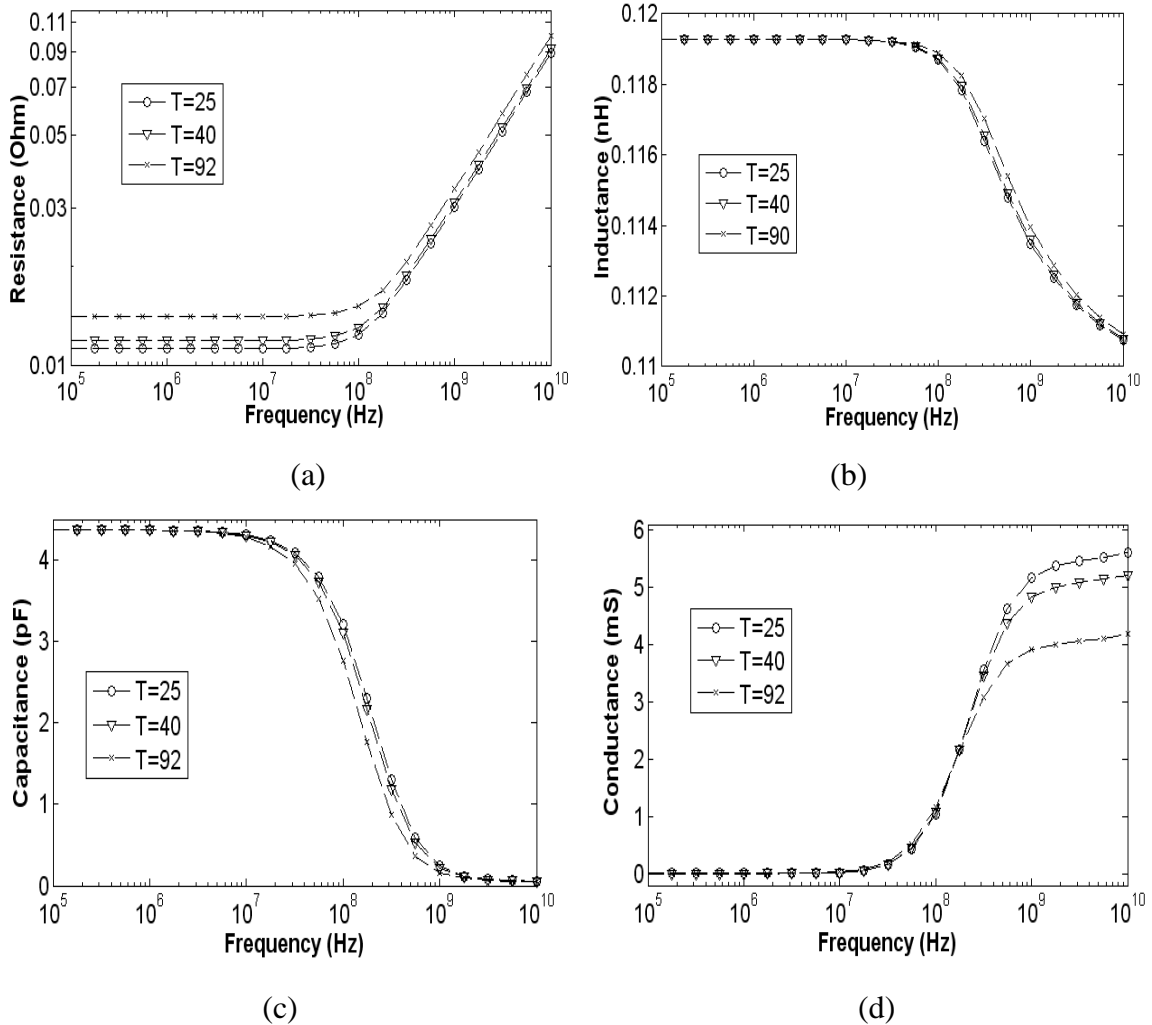


Figure 32. TSV-1 self-RLCG parameters, (a) resistance, (b) inductance, (c) capacitance, (d) conductance.

For the self-capacitance of the TSV, the temperature effect is obvious in the range of 0.05 – 1 GHz, as shown in Figure 32c. With increasing temperature, the equivalent capacitance is reduced. This is because silicon permittivity also depends on the temperature, as indicated by Equation (20). As seen from Figure 32d, in low-frequency range, the conductance does not vary with temperature. However, in frequency range of 0.2 – 10 GHz, the conductance decreases with temperature, which is caused by the decreasing silicon substrate conductivity with increasing temperature. For TSVs, since the series resistance is in the scale of milliohms (Figure 32a) and inductance in the scale of pH (Figure 32b), the insertion loss of TSVs at higher frequencies is mainly caused by the shunt capacitance and conductance.

3.3.3.3 Temperature Effect on Coupled Noise

The temperature effect on time-domain coupled noise of TSVs is also simulated. In the time-domain simulation, a rectangular clock signal with a peak-to-peak amplitude of 2 V is excited at the top ends of four signal TSVs: TSV-1, TSV-3, TSV-11 and TSV-13 (Figure 27b). The bottom ends of the four TSVs are all terminated using 50 Ohm resistors. TSV-7 is the victim TSV used to observe the coupled noise. Since the number of neighboring ground TSVs in the system can affect the signal crosstalk, the effect of ground/signal (G/S) TSV ratio on coupled noise is first examined. Three cases are studied with G/S TSV ratios of 1:4, 2:4, and 4:4, respectively. The ground TSV ID numbers for the three cases are shown in Table 3. Note that the top and bottom ends of all other TSVs in the 5×5 TSV array (Figure 27b) are all terminated with 50 Ohm resistors connecting to ground.

With different G/S TSV ratios, the coupled noise at the top end of TSV-7 with an input clock frequency of 1GHz is shown in Figure 33a. The rise and fall times of the clock signal are both set to 50ps . The peak values of the coupled noise and percentage change with increasing G/S TSV ratio are listed in Table 3. It is observed that by increasing the G/S ratio from 1:4 to 2:4 and 4:4, the coupled noise reduces by 18% and 39%, respectively, indicating the importance of the G/S TSV ratio on crosstalk. With a G/S TSV ratio of 4:4, the coupled noise with temperature effect is also investigated. The coupled waveform is shown in Figure 33b. As seen from Figure 33b, the coupled noise decreases with increasing temperature. The peak values of the coupled noise and percentage change because of the temperature effect are listed in Table 4. As seen from Table 4, by increasing the temperature from 25 to 92 Degrees, the temperature effect can result in a 13% reduction of the coupled noise.

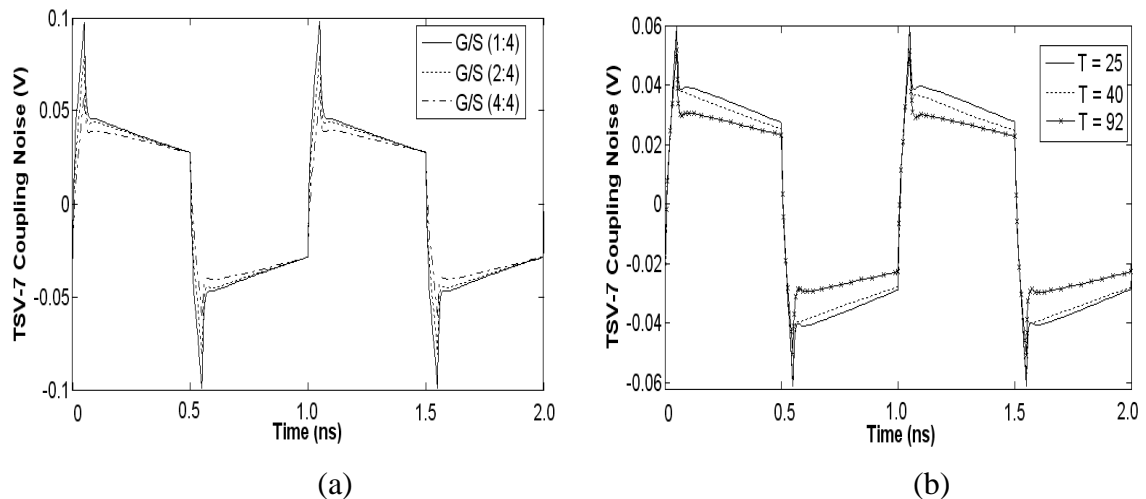


Figure 33. (a) Coupled noise with different G/S TSV ratios, (b) temperature effect on coupled waveforms with a G/S ratio of 4:4.

Table 3. Effect of ground/signal TSV ratio on coupled noise.

G/S TSV Ratio	1:4	2:4	4:4
Ground TSV	TSV-2	TSV-2, TSV-12	TSV-2, TSV-6, TSV-8, TSV-12
Peak Value (mV)	97.6	79.6	59.6
Percentage Change	--	18.4%	38.9%

Table 4. Temperature effect on TSV coupled noise.

Temperature	25 Celsius	40 Celsius	92 Celsius
Peak Value (mV)	59.6	58.3	51.8
Percentage Change	--	2.2%	13.0%

3.4 Summary

In this chapter, the electrical-thermal co-simulation approaches are presented to address the temperature effect on voltage drop and TSV characteristics. The voltage drop-thermal co-simulation method for PDNs is first presented. The finite-volume schemes for the modeling of voltage drop with non-uniform temperature distribution and fluidic cooling are discussed in detail. The correctness and accuracy of the models for heat conduction, air convection, and Joule heating have been verified using a PCB example. In addition, two examples of microfluidic cooling including an experimental example have been simulated to validate the finite-volume model for microfluidic cooling. The temperature effect on voltage drop is demonstrated using several examples. The simulation results show that the temperature effect on voltage drop can be 20-30%. The effectiveness of fluidic cooling is verified using a 3D-system example. The simulation results show that the method of fluidic cooling using microchannels can effectively reduce the temperature of high-power stacked chips, compared to the method using heat sinks.

The thermal-electrical analysis for TSV arrays is also presented to investigate the

temperature effect on TSV characteristics. The presented analysis methodology combines the electrical TSV modeling technique using CMBFs and the thermal modeling using the FVM. We investigated the temperature effect on the insertion loss, crosstalk, *RLGC* parameters, and time-domain coupled noise of TSVs via several numerical test cases. The following conclusions have been drawn. First, the increasing temperature can decrease the insertion loss of TSVs at high frequencies because the conductivity of the silicon interposer decreases with temperature. Second, the temperature increases can cause the variation of the crosstalk between TSVs. The temperature effect on crosstalk demonstrates frequency-dependent behaviors. Third, the self-parameters of TSVs including series resistance, shunt capacitance, and shunt conductance also vary with temperature. Fourth, the temperature can also affect the time-domain coupled noise. With a G/S TSV ratio of 4:4, the temperature increase from 25 to 92 Celsius can reduce the coupled noise by 13% with an input clock frequency of 1GHz in our simulation.

CHAPTER 4

STEADY-STATE VOLTAGE DROP AND THERMAL MODELING USING NON-CONFORMAL DOMAIN DECOMPOSITION

4.1 Introduction

A 3D integrated system contains stacked chips using TSVs and micro-bumps, a package, and a PCB (Figure 1). The small-size features such as TSVs and micro-bumps usually have a dimension in the range of 5-60 microns while the large-size objects (e.g., PCB and planes) have a dimension in the range of 5-20 centimeters. As a result, the scale contrast in a 3D system can reach 1:10000 and beyond. For the thermal and voltage drop modeling of a 3D system, the multiscale nature requires meshing a 3D system using a large number of meshing cells/unknowns, which represents a critical task for simulating the entire system. Simultaneously modeling a 3D system consisting of stacked ICs, packages, and PCBs necessitates the development of multiscale modeling methods that can dramatically reduce the total number of meshing cells/unknowns.

In this chapter, the multiscale modeling method using finite-element non-conformal domain decomposition is presented for steady-state thermal and voltage drop analysis. Using the presented approach, a 3D system can be divided into many individual subdomains. The non-conformal domain decomposition technique also provides the flexibility of gridding each subdomain using independent meshes while maintaining the continuity of heat/current flows across domains by introducing the Lagrange multiplier. The non-conformal domain decomposition approach is also applied for the voltage drop-thermal co-simulation of 3D problems. To accelerate the co-simulation, the cascadic multigrid (CMG) solving approach is applied using hierarchical meshing grids.

4.2 Preliminaries

In this section, the finite-element formulation [79] for steady-state thermal modeling is explained with air convection boundary conditions. By multiplying a testing function N at the both sides of Equation (2a) and integrating over the volume, after using the divergence theorem, the weak form [80] of the heat equation can be obtained as

$$\iint_{\Omega} k \nabla N \cdot \nabla T \, dx dy dz - \int_S k N \frac{\partial T}{\partial n} \, ds = \iint_{\Omega} -NP \, dx dy dz \quad (21)$$

By using the convection boundary condition as in Equation (9), Equation (21) can be converted as

$$\iint_{\Omega} k \nabla N \cdot \nabla T \, dx dy dz + \int_S h_c N T \, ds = \iint_{\Omega} -NP \, dx dy dz + \int_S N h_c T_a \, ds \quad (22)$$

For 3D thermal modeling, the 8-node hexahedral elements with trilinear basis functions are used. The rectangular mesh of an inhomogeneous material stack-up and a hexahedral element with trilinear basis functions are shown in Figure 34. For simplicity, the same basis function can also be used as the testing function. As a result, with n meshed cells, the system equation can be written as

$$\sum_{e=1}^n \left(K_D^{(e)} + K_g^{(e)} \right) \boldsymbol{\varphi} = \sum_{e=1}^n \left(f_P^{(e)} + b^{(e)} \right) \quad (23)$$

where

$$\begin{aligned} K_D^{(e)} &= \iint_e k \nabla N \cdot \nabla N \, dx dy dz & K_g^{(e)} &= \int_{\Gamma_e} h_c N N \, ds \\ f_P^{(e)} &= \iint_e -NP \, dx dy dz & b^{(e)} &= \int_{\Gamma_e} N h_c T_a \, ds \end{aligned} \quad (24)$$

In Equation (23-24), $K_D^{(e)}$ and $K_g^{(e)}$ represent the elementary stiffness matrices for each element because of heat conduction and heat convection, respectively; $f_P^{(e)}$ and $b^{(e)}$ represent the external heat excitation and temperature gradient because of convection,

respectively. For modeling with a homogenous Neumann boundary condition (natural boundary condition) [80], we can simply let $b^{(e)}$ and $K_g^{(e)}$ equal zero in Equation (23).

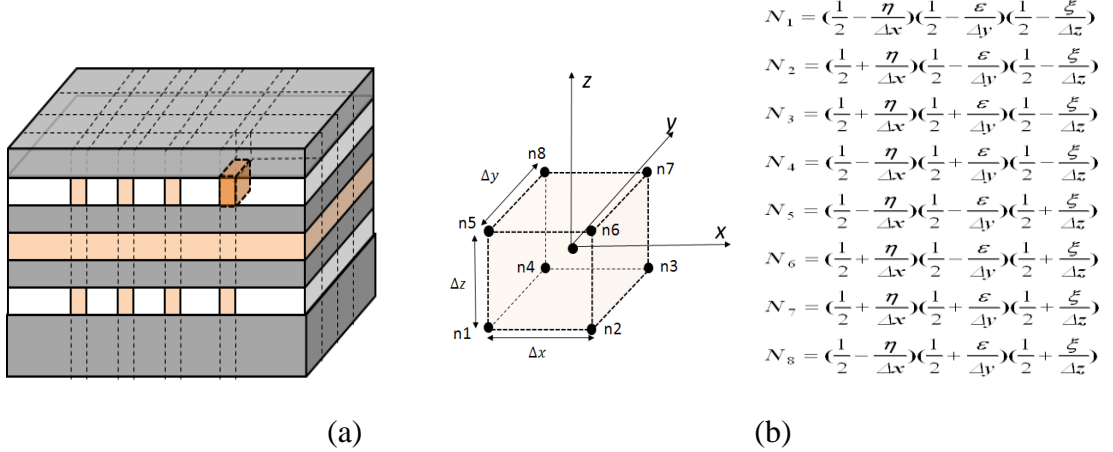


Figure 34. (a) Layer stacking with inhomogeneous materials, (b) an 8-node hexahedral element (cell) and trilinear basis functions.

Since the voltage distribution equation and the heat equation share the same form except the air convection boundary condition, the same finite-element formulation can be used for the modeling of voltage drop. It is noted that the cell-based finite-element formulation can handle the material inhomogeneity as shown in Figure 34a [79].

4.3 Modeling using Non-conformal Domain Decomposition

In this section, the steady-state voltage drop and thermal modeling using the finite-element non-conformal DDM is discussed. The focus is on the modeling of multiscale 3D problems with emphasis on the interposer, package, and PCB using the domain decomposition with non-conformal gridding based on the Mortar FEM [41, 81].

4.3.1 Formulation Based on Mortar FEM

An integrated system consisting of stacked dies, a thermal interface material, micro-bumps, and a package is shown in Figure 35a. Because of the feature scale difference in

the regions of chip and package, large numbers of meshing cells are required when gridding the entire system using the finite-element or finite-volume discretization. To alleviate this problem, the integrated system can be divided into separate subdomains: the chip domain and package domain, as shown in Figure 35b. The chip domain and package domain can be meshed independently using 3D non-uniform grids. As a result, the meshing grids from the chip domain do not overlap with the grids from package domain. Therefore, the required meshing cells are greatly reduced. For simplicity, the thermal analysis using the DDM based on the Mortar finite element formulation [41] is explained with 2D rectangular grids, as shown in Figure 35b.

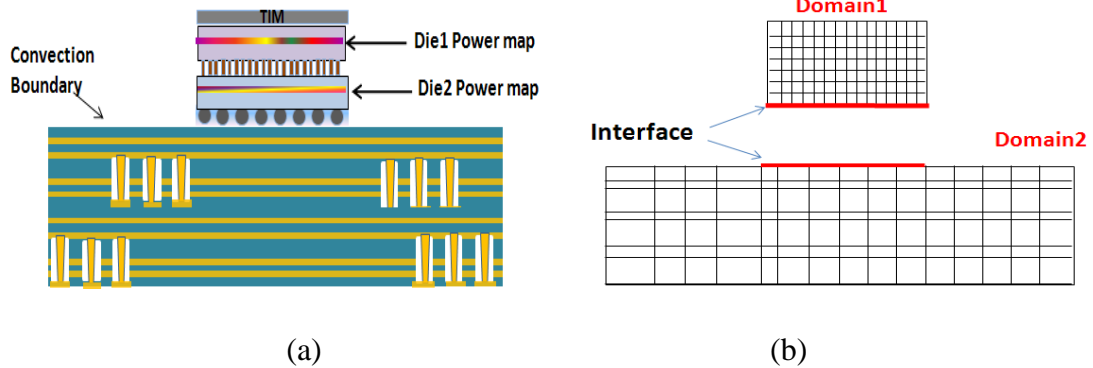


Figure 35. (a) A 3D integrated system, (b) non-conformal gridding of chip and package.

At the interface, the continuity of electrical currents and heat flows needs to be ensured for both the voltage drop and thermal analysis. For two subdomains with a common interface (Figure 35b), by assuming $\lambda^{(i)} = k \partial T^{(i)} / \partial n_i$ ($i = 1, 2$), we have the relationship of $-\lambda^{(1)} = \lambda^{(2)} = \lambda$ [81], where λ is a function from the Lagrange multiplier space. Then the weak continuity for heat or current flows across the interface can be established, and the following equations for domains and interface can be derived as

$$\begin{aligned}
& \iint_{\Omega_1} k \nabla N_1 \cdot \nabla T_1 dx dy - \int_{\Gamma_1} k N_1 \frac{\partial T_1}{\partial n} dt + \int_{\Gamma_{inter}} \lambda N_1 dt = \iint_{\Omega_1} -N_1 P_1 dx dy \\
& \iint_{\Omega_2} k \nabla N_2 \cdot \nabla T_2 dx dy - \int_{\Gamma_2} k N_2 \frac{\partial T_2}{\partial n} dt - \int_{\Gamma_{inter}} \lambda N_2 dt = \iint_{\Omega_2} -N_2 P_2 dx dy \\
& \int_{\Gamma_{inter}} (T_1 - T_2) \psi dt = 0
\end{aligned} \tag{25}$$

where N_1 , N_2 , and ψ represent the basis functions for domain1, domain2, and Lagrange multiplier space, respectively [82]. The temperature T_1 and T_2 can be expressed as a linear combination of basis functions in domain 1 and domain 2, respectively. Similarly, with the Lagrange multiplier λ being expressed as $\lambda = \sum_{i=1}^{n_\lambda} b_i \psi_i$,

the system equation for the problem with two subdomains (Figure 35b) can be written as

$$Kx = \begin{bmatrix} A_1 & 0 & B_1^T \\ 0 & A_2 & -B_2^T \\ B_1 & -B_2 & 0 \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ b \end{bmatrix} = \begin{bmatrix} f_1 \\ f_2 \\ 0 \end{bmatrix} = f \tag{26}$$

where the matrix entries for k -th domain can be expressed as

$$\begin{aligned}
A_{k(ij)} &= \iint_{\Omega_k} k \nabla N_i^{(k)} \cdot \nabla N_j^{(k)} dx dy - \int_{\Gamma_{inter}} k N_i^{(k)} \frac{\partial N_j^{(k)}}{\partial n} dt \\
B_{k(ij)} &= \int_{\Gamma_{inter}} \psi_i N_j^{(k)} dt \quad (k = 1, 2) \\
f_{k(j)} &= \iint_{\Omega_i} -N_j^{(k)} P dx dy
\end{aligned} \tag{27}$$

In Equation (26-27), A_1 , A_2 , f_1 , and f_2 represent the stiffness matrices and excitations for domain 1 and domain 2, respectively; B_1 and B_2 represent the coupling matrices for the two domains. To obtain the stiffness matrix for each domain, the associated boundary conditions need to be used for the corresponding subdomains. In addition, the homogeneous Neumann boundary condition needs to be assigned at the common interface in the process of forming matrices A_1 and A_2 . For a 3D problem, the

interface becomes a surface. As the interfacial surface can have several thousands of nodes, the 4-point Gaussian quadrature for rectangular elements is used to effectively calculate B matrix.

For an integrated system that is divided into N subdomains, the generalized system equation can be written as

$$Kx = \begin{bmatrix} A & B^T \\ B & 0 \end{bmatrix} \begin{bmatrix} x_d \\ x_{inter} \end{bmatrix} = f \quad (28)$$

where A is a block diagonal matrix described by

$$A = \begin{bmatrix} A_1 & & & \\ & A_2 & & \\ & & \ddots & \\ & & & A_N \end{bmatrix} \quad (29)$$

4.3.2 Interface Basis Functions

For the Lagrange multiplier of the interface, the basis functions can be constructed based on the interfacial grids from either side. To reduce the number of unknowns for the interface, the basis functions can be constructed based on the domain with coarse meshing grids. However, to satisfy the inf-sup condition [41, 81] so that the coupling matrix B for the interface has a full rank, the basis functions for the interface cannot be randomly selected. For a 2D problem with 4-node (bilinear) elements (Figure 35b), the interface becomes a line. The interface basis functions can be constructed based on linear shape functions and expressed as

$$\psi_i = \begin{cases} \varphi_1 + \varphi_2 & (i = 1) \\ \varphi_{i+1} & (1 < i < n - 2) \\ \varphi_{n-1} + \varphi_n & (i = n - 2) \end{cases} \quad (30)$$

where φ_i is a linear shape function associated with node i . As an example, the basis functions for the interface in Figure 35b are shown in Figure 36. Therefore, for a one-dimensional interface with n nodes, the total number of basis functions is $n-2$.

For a 3D problem, the interface becomes a surface connecting two subdomains, as shown in Figure 37a. As adjacent domains are usually meshed independently, the meshing grids do not overlap at the common interface. For a 2D interface with $N_x \times N_y$ nodes, the interface basis functions can be obtained based on 2D bilinear shape functions. For a simplified representation, the basis function can be described using 1D basis functions in two directions (Figure 37b) as

$$\psi_{ij} = \psi_{ix} \psi_{jy} \quad (1 \leq ix \leq N_x - 2, 1 \leq jy \leq N_y - 2) \quad (31)$$

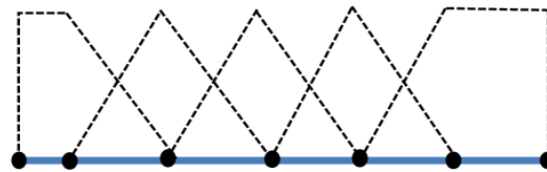


Figure 36. Basis functions for a 1D interface.

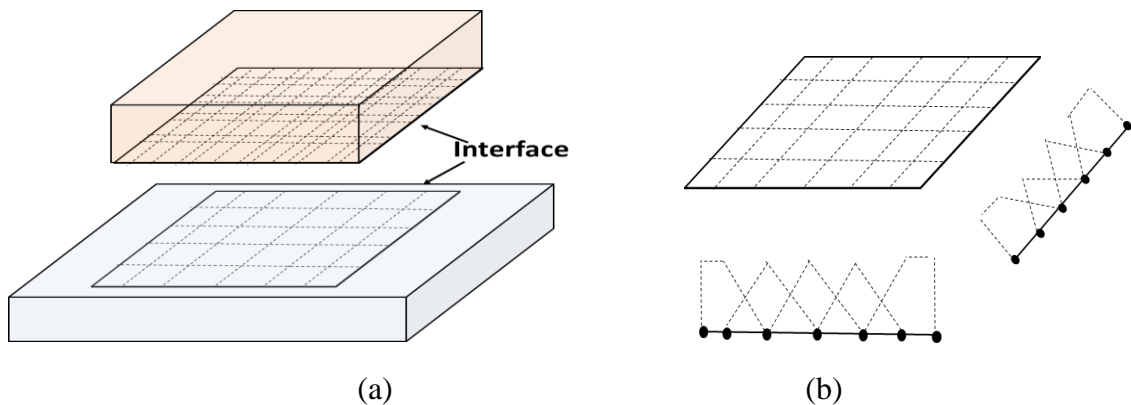


Figure 37. (a) A 2D interface for a 3D problem, (b) interface basis functions in two directions.

For a problem with a total number of n_{inter} interfaces, assuming each interface has M_i basis functions, the dimension of B matrix is $N_B \times N_A$. N_B can be expressed as

$$N_B = \sum_{i=1}^{n_{inter}} M_i \quad (32)$$

Using the non-conformal gridding, the required meshing cells for subdomains can be greatly reduced. However, because of introducing the Lagrange multiplier for interfaces, extra interface unknowns x_{inter} are added to the system (Equation 28). The additional computational cost because of the introduced interface unknowns is explained in Section 4.4.2. It should be noted that for the voltage drop analysis, since a similar formulation using the finite-element non-conformal domain decomposition can be derived as for the thermal analysis, the derivation is omitted here.

4.3.3 Test Cases

To verify the correctness and accuracy of the DC voltage drop and thermal simulation using the non-conformal domain decomposition approach, two verification examples have been simulated first.

A. A Multi-layer PCB Example

A three-layer PCB with a size of 9 cm \times 9 cm is shown in Figure 38a. The thicknesses of the copper plane and dielectric layer are 30 microns and 350 microns, respectively. As shown in Figure 38a, the three-layer copper planes are shunted together using a 40 \times 40 via array. The dimension of via is 0.3 mm \times 0.3 mm. Using the domain decomposition approach, this PCB is divided into nine subdomains, as shown in Figure 38b. The fifth subdomain contains the via array. As the coupling between domains is captured using

Lagrange multipliers, each domain can be meshed independently; thus, the fine mesh grids do not project from the fifth domain to other adjacent domains.

This example is simulated using domain decomposition. The voltage distribution on the first layer of the PCB is shown in Figure 39a. This example is also simulated using the FEM without domain decomposition. For comparison purposes, the maximum mesh size is set to be the same for the two methods. Using the FEM, the voltage distribution on the first layer is shown in Figure 39b. The voltage at the current source location is 2.4811V. Using the domain decomposition approach, the voltage at the current source location is 2.4816 V. The 0.5 mV discrepancy comes from the different meshing grids adopted for the two methods. Because of the mesh projection from the via array, 60 *K* unknowns are required for the FEM. However, only 49.2 *K* domain unknowns and 1.7 *K* interface unknowns are needed for the DDM.

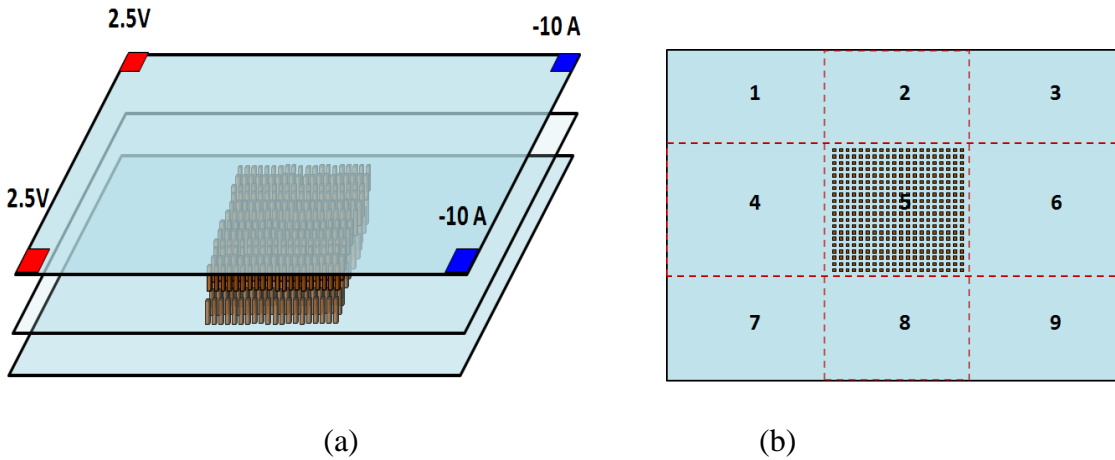


Figure 38. (a) A three-layer PCB, (b) domain decomposition of the PCB.

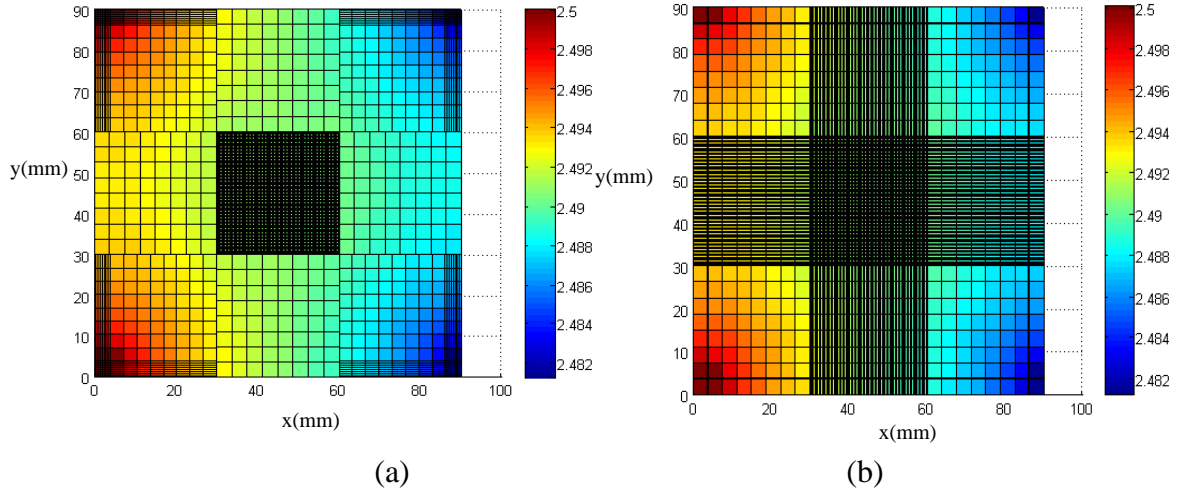


Figure 39. Voltage distribution of the PCB using (a) the domain decomposition method and (b) FEM (Unit: V).

B. A Package Example

To verify the accuracy of the thermal modeling using the domain decomposition approach, a package example, as shown in Figure 40a, is simulated. The package includes five metal layers, a TIM (thermal interface material), 1600 package vias, and a 20×20 micro-bump array. The package size is $30 \text{ mm} \times 30 \text{ mm}$, and the chip size is $10 \text{ mm} \times 10 \text{ mm}$. The total power consumption of the chip is 50 W , and the nonuniform power map of chip is illustrated in Figure 40b. The thermal conductivity of the TIM is $2 \text{ W}/(\text{mK})$. The heat sink is modeled as an ideal heat sink with a constant room temperature of 25°C . This example has been simulated with a convection coefficient of $5 \text{ W}/(\text{m}^2\text{K})$ on both sides of the package. The material thicknesses and thermal conductivities are shown in Table 5.

To effectively simulate this package, this example is divided into two subdomains: the chip domain and package domain. The chip domain has a meshing grid of $70 \times 70 \times 6$, and the package domain has a meshing grid of $80 \times 80 \times 10$. The total number of unknowns is 99.6 K . The total number of interface unknowns is 4.9 K . Compared to the

thermal simulation using the FEM, which requires 183.2 K unknowns, the number of unknowns is greatly reduced because of the non-conformal domain decomposition approach used. The generated system equations for the FEM and DDM are all solved using the direct sparse solver in Matlab. The total solving time for the DDM is 22.3 seconds, about 34% reduction compared to the FEM, which takes 33.6 seconds. The simulated temperature distribution of the chip and package is shown in Figure 41.

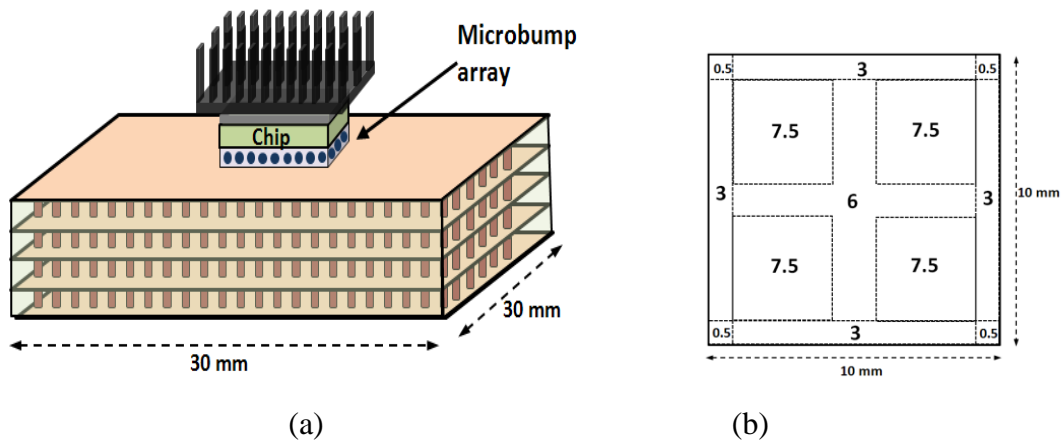


Figure 40. (a) A package example, (b) nonuniform chip power map (unit: W).

Table 5. Material thicknesses and thermal conductivities.

	Material Thickness (mm)	Thermal Conductivity (W/mK)
Package dielectric	0.35	0.8
Copper Plane	0.03	400
Chip	0.3	110
Underfill	0.2	0.4
C4	0.2	174
Package via	0.35	400
TIM	0.2	2.0

The temperature distribution at the location of $y = 12.75$ mm of the chip with and without domain decomposition is shown in Figure 42. The maximum temperature difference is about 0.4 degree, which is due to the different meshing grids used for the

two methods. The good agreement between the results from the two methods validates the accuracy of the thermal simulation using the domain decomposition.

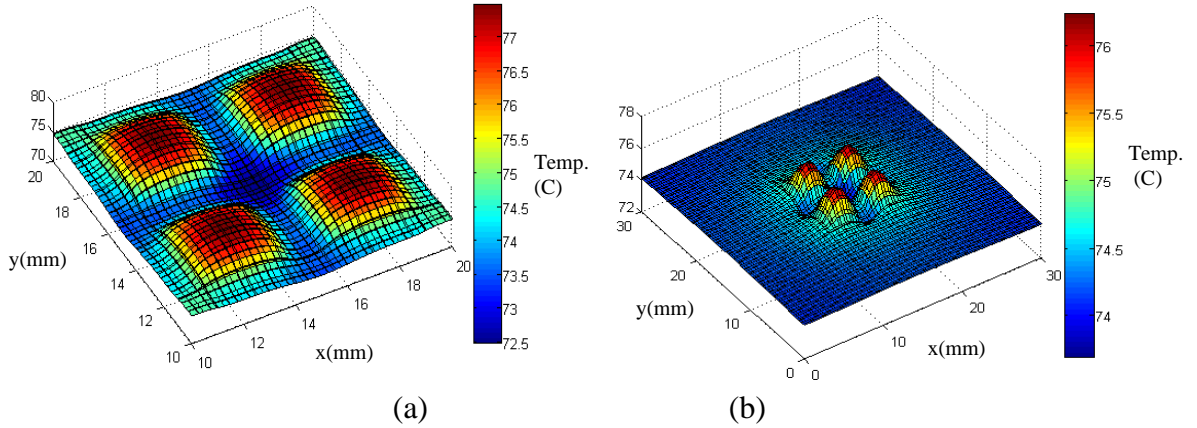


Figure 41. Temperature distributions of (a) chip and (b) package.

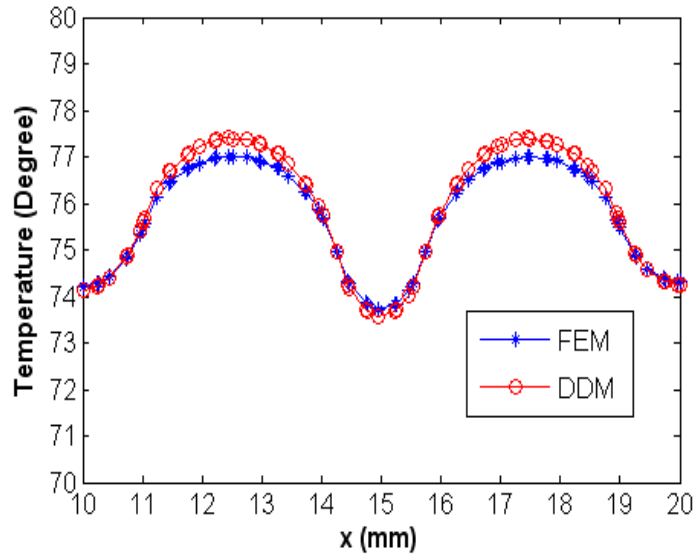


Figure 42. Comparison of on-chip temperature distributions (at $y = 12.75$ mm).

4.4 Co-simulation using Cascadic Multigrid (CMG) Approach

Using the finite-element non-conformal DDM, the system unknowns can be greatly reduced as discussed in the last section. However, for a complex multiscale system, with the size of the sparse stiffness matrix approaching millions, the matrix condition number

can increase dramatically. Therefore, fast iterative methods with a good preconditioner are required. For simulating multiscale systems, in addition to the aforementioned domain decomposition technique, the simulation can be accelerated by making use of hierarchical meshing grids.

For the thermal and voltage drop modeling using the non-conformal DDM, the system matrix K becomes symmetric indefinite. Therefore, standard multigrid methods cannot be directly applied. Instead of using the standard multigrid method as in [14, 91], the CMG method [83] can be used to solve the linear system equation (28). It is important to note that for the CMG to be successfully applied to the voltage drop-thermal co-simulation iteration (Figure 6), because of the coupling between voltage drop and thermal characteristics, special considerations and treatment of the Joule heating and temperature are required considering the multilevel grids, which will be addressed in the next subsection.

4.4.1 Co-simulation using CMG

The cascadic multigrid solving flow with hierarchical non-conformal mesh grids is shown in Figure 43. As shown in Figure 43, the problem on the coarsest mesh grids with fewer unknowns is solved exactly. Then, the solution is interpolated to next level of finer mesh grids. For each mesh level except the initial mesh level, the iterative subspace confined conjugate gradient (CG) method [83] is used as a smoother to accelerate the convergence of the solution before the solution is interpolated to finer grids. Since the initial approximation is interpolated from the previous level, the starting residual is small; thus, the convergence can be efficiently reached. As the non-conformal domain decomposition approach is used, the mesh refinement in one domain does not affect the

gridding of other domains. This feature provides the flexibility to do mesh refinement for only one or two critical domains in the simulation.

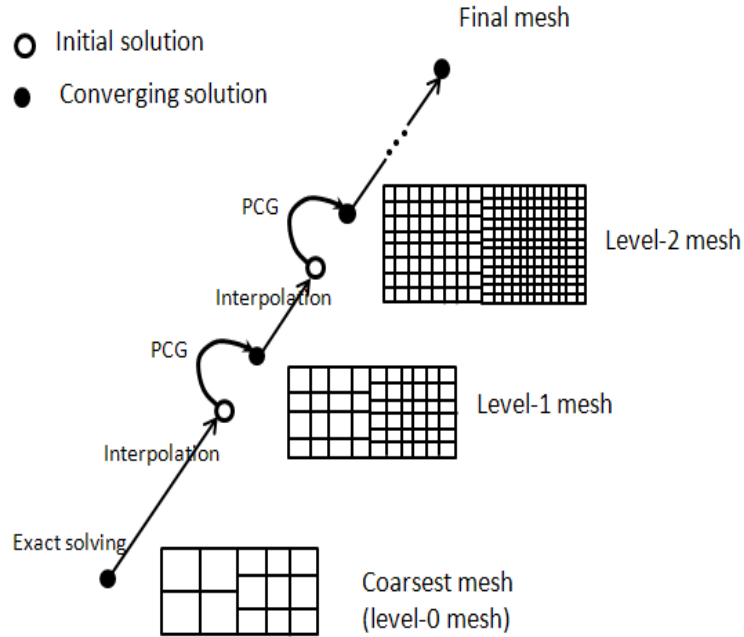


Figure 43. Cascadic multigrid solving flow.

Since the stiffness matrix K is symmetric indefinite, a constraint preconditioner M needs to be used to accelerate the convergence of the CG method [84, 85]. M is given by

$$M = \begin{bmatrix} D & B^T \\ B & 0 \end{bmatrix} \quad (33)$$

where D is a positive definite matrix that satisfies the inequality of $(Dv, v) \geq (Av, v)$.

The pseudo-algorithm of the cascadic multigrid solving method with multiple domains is shown in Figure 44. Since the subspace confined PCG method is used for each mesh level, a stop criterion ε needs to be used to check the convergence. Instead of using the energy norm-based error stop criteria as in [83], the L2 residual norm-based

criterion is used as for the standard PCG method. The iteration stop criterion is described by

$$\|r_{ut}\| < \varepsilon \|r_{u0}\| \quad (34)$$

where $\|r_{u0}\|$ and $\|r_{ut}\|$ represent the L2 norm of the residual for the initial and t -th PCG iterations, respectively. Since the residual is already calculated in each PCG iteration, no extra matrix-vector multiplication is needed. Therefore, the computational cost is reduced.

As matrix M is used as the preconditioner in the PCG iteration, the following equation needs to be solved

$$\begin{bmatrix} D & B^T \\ B & 0 \end{bmatrix} \begin{bmatrix} s_{11} \\ s_{12} \end{bmatrix} = \begin{bmatrix} r_{11} \\ r_{12} \end{bmatrix} \quad (35)$$

Instead of directly solving it, the following algorithm is used:

$$\begin{aligned} 1) & C = -BD^{-1}B^T \\ 2) & s_{12} = C^{-1}(r_{12} - BD^{-1}r_{11}) \\ 3) & s_{11} = D^{-1}(r_{11} - B^T s_{12}) \end{aligned} \quad (36)$$

where C is the Schur complement associated with the Lagrange multiplier variables for interfaces. Since the inverse of D needs to be used to calculate the Schur complement, a D matrix that has a much simpler structure than matrix A is preferred. In the simulation, a diagonal matrix $\alpha \text{diag}(A)$ is used for D matrix, where α is a positive number. As a result, the inverse of D becomes trivial, and C is also a sparse matrix. For the voltage drop simulation and thermal simulation, it is found out that choosing α between 1 and 2 can benefit the convergence.

Because of the interaction between voltage drop and thermal characteristics, Joule heating and temperature become additional variables, which need to be updated in each iteration. For the CMG to be successfully applied to the voltage drop-thermal iteration

with multilevel mesh grids, special considerations and treatment are required. The voltage drop and thermal iteration flow using CMG is shown in Figure 45a.

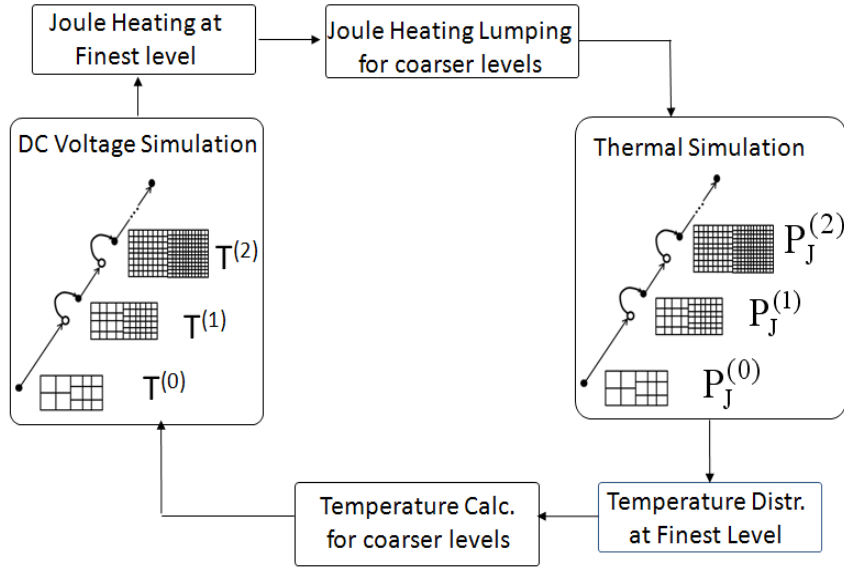
```

Input : K, A, B, f, M of each mesh level,  $\varepsilon, n_{\max}, n_{\text{direct}}$ 
Output : u

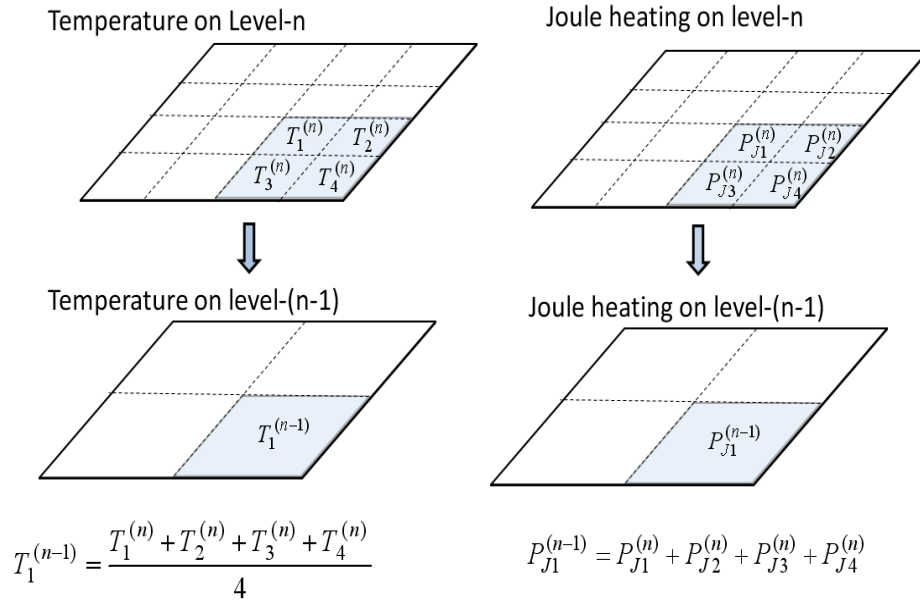
Do i = 0 : levelmax
if (i == 0), solving on coarsest grid
    if size(K) < ndirect
        x = [u0, λ0] = K-1f
    else
        PCG iteration with v0 set to be 0
    end
else
    1) In each domain, interpolate from level (i-1) to level i
         $\tilde{u}^i = I u^{i-1}, \tilde{\lambda}^i = I \lambda^{i-1}, \tilde{v} = [\tilde{u}^i, \tilde{\lambda}^i]$ 
    2) PCG iteration for level i
        v00 = [u00i, λ00i] =  $\tilde{v} + M^{-1}(f - A\tilde{v})$ 
        v0 = [u0i, λ0i] = [u00i, λ00i]
        r0i = [ru0i, rλ0i] = (f - Av0)
        s0i = [su0i, sλ0i] = M-1r0i
        p0i = su0i, σ0 = (s0i, r0i)
        α0 = σ0 / (Ap0i, p0i)
        for(t = 1 : nmax)
            uti = ut-1i + αt-1pt-1i
            λti = λt-1i + sλ(t-1)i-1, vti = [uti, λti]
            rti = [ruti, rλti] = f - Kvti
            sti = [suti, sλti] = M-1rti
            σt = (sti, rti)
            γt-1 = σt / σt-1
            pti = suti + γt-1pt-1i
            αt = σt / (Apti, pti)
            check convergence
            if (||ruti|| < ε ||ru0i||)
                break
            endif
        end for
    end
end
end

```

Figure 44. Pseudocode for the cascadic multigrid method with multiple domains.



(a)



(b)

Figure 45. (a) Voltage drop-thermal iteration flow using CMG, (b) temperature averaging and Joule heat lumping from level-n to level-(n-1).

It is assumed that the thermal simulation is first carried out without considering Joule heating. In each thermal simulation, only the temperature distribution at the finest mesh

level is obtained using the CMG solver. However, because of the multilevel meshing grids used, the temperature profiles at other coarser levels also need to be calculated. The temperature profiles on multilevel grids are used to update the temperature-dependent stiffness matrices for the voltage drop analysis at different meshing levels. On the other side, the Joule heat at the finest mesh level is obtained from the voltage drop simulation. Similarly, Joule heat at other coarser mesh levels also needs to be formed. Thus, the heat excitation vectors at different mesh levels can be accordingly updated for the CMG to be applied to thermal simulation. The calculation of temperature and Joule heat profiles from mesh level- n to level- $(n-1)$ is shown in Figure 45b. The calculation of temperature and Joule heat profiles at coarse level- $(n-1)$ is obtained using cell-based temperature averaging and Joule heat lumping.

In the voltage drop-thermal co-simulation, the stiffness matrices A and B do not change with iterations for thermal simulation. However, for the voltage drop simulation, because of the temperature-dependent resistivity, the stiffness matrix A varies with iterations while B stays the same. To reduce the simulation cost, the stiffness matrices A and B for thermal simulation and B matrix for the voltage drop simulation are only calculated once and stored. The Joule heat for thermal simulation and stiffness matrix A for voltage drop simulation are updated with iterations.

4.4.2 Computational Cost for Interface Unknowns

Using the non-conformal meshing, unknowns for subdomains can be effectively reduced, compared to the conventional FEM. Because of the introduced interface basis functions used to ensure the continuity of heat/current flows across domains, extra nonzero entries of the B matrix and unknowns for interfaces are added to the system. The effect of the

extra unknowns on computational cost needs to be investigated for the CMG method. For modeling a 3D system, assuming the total number of unknowns for domain and interface are N_A and N_B , the simulation can be categorized into two cases based on the size of N_B .

Case A: when N_B is much smaller than N_A , direct solving methods can be used to solve $s_{12} = C^{-1}(r_{12} - BD^{-1}r_{11})$. The total computational cost for each subspace confined PCG iteration is of $O(\alpha N_A + \beta N_B + (N_B)^p)$. Since matrix B is for 2D interfaces, the estimated order p is between 1.5 and 2. α and β are scaling factors for matrix-vector multiplications depending on the matrix nonzero entries. Since N_B is much smaller than N_A , a small fraction of the computational cost is added because of the introduced interface unknowns.

Case B: when N_B is larger and comparable to N_A , direct solving methods cannot be used because of finite computer memory. To solve $s_{12} = C^{-1}(r_{12} - BD^{-1}r_{11})$, iterative solving approaches such as the PCG method are required. For each subspace confined PCG iteration, the estimated computational cost is of $O(\alpha N_A + \beta N_B + N_B \log(N_B))$. As N_B is comparable to N_A , a large amount of computational overhead is added for each iteration. As a result, the system cannot be efficiently solved.

For a 3D system consisting of dies, a package, and a PCB, the system is vertically divided into domains based on feature scale difference. In general, as each domain is meshed using 3D mesh grids and the interface is meshed using 2D grids, the number of interface unknowns is much smaller than that for the subdomains. Thus, the CMG can provide an effective solution in terms of memory and computational complexity. The

efficiency of the non-conformal domain decomposition with the cascadic multigrid solving approach is demonstrated through numerical test cases.

4.4.3 Test Cases

A. A 3D Integration Example

To demonstrate the capability of handling multiscale problems, a 3D integration example, as shown in Figure 46, is simulated. This example includes stacked dies, an 8-layer package, and a 10-layer PCB. The die size is $12 \text{ mm} \times 12 \text{ mm}$, and the package size is $30 \text{ mm} \times 30 \text{ mm}$. The PCB board size is $10 \text{ cm} \times 10 \text{ cm}$. The dies are stacked together using 400 TSVs (a 20×20 array). To reduce the IR drop, two PCB metal layers are shunted together using 100 PCB vias. In this example, the minimum and maximum scales in the lateral direction are 200 microns and 10 cm, respectively. The material layer thicknesses and thermal conductivities are listed in Table 6. Air convection with a convection coefficient of $15 \text{ W}/(\text{m}^2\text{K})$ is applied to both sides of the PCB. In this example, on-chip power grids are not included. The power supply voltage is 1.8 V. The power consumption of stacked dies is 80 W and a uniform power map is used. Note that in a practical design, the power maps of dies need to be extracted using chip CAD tools based on a chip layout design. Because of the scale difference between the die, package and PCB, this example is vertically divided into three domains: the chip domain, package domain, and PCB domain. Therefore, two interfaces are needed to capture the coupling between the chip-package and the package-PCB. In this example, the basis functions for the Lagrange multiplier for the chip-package interface are selected from the package side while the basis functions for the package-PCB interface are selected from the PCB side.

The sub-domains of die, package, and PCB are meshed independently. For the initial (level-0) mesh for thermal simulation, the meshing grid arrays for die, package and PCB domains are $42 \times 42 \times 8$, $44 \times 44 \times 19$ and $24 \times 24 \times 21$, respectively. The total number of domain unknowns is 63.0 K and the number of interface unknowns is 0.4 K, which can be exactly solved using a direct sparse solver in 15.4 s. Without domain decomposition, the meshed cell numbers in the x , y and z directions are 106, 106 and 46, respectively, resulting in about 402 K unknowns using the FEM, which cannot be solved directly. The FEM requires 398.9 s iterative solving time using the conjugate gradient method with a diagonal pre-conditioner.

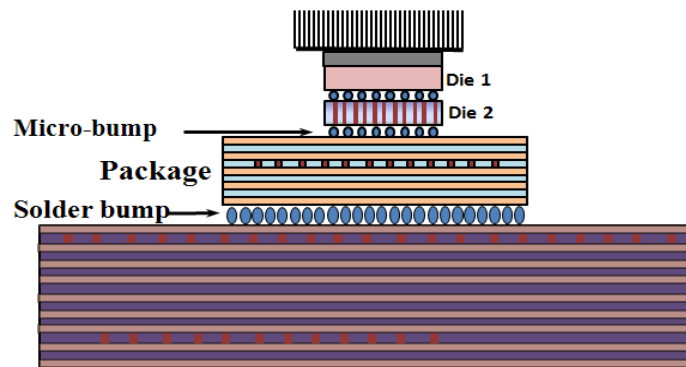


Figure 46. A 3D integration example.

For the level-2 mesh refinement, 968 K unknowns are required for the thermal simulation. However, using the FEM with a similar mesh size, the total number of unknowns is about 6.3 million, which requires a long simulation time using the preconditioned conjugate gradient method. Based on the hierarchical meshing grids using domain decomposition, the cascadic multigrid solving algorithm can be applied. Since the initial solution is interpolated from the previous level, the norm of the initial residual is very small and the stop criterion ε is set to be $1E-2$ for both DC voltage and thermal

simulations. For both the problems with level-1 and level-2 meshes, iterative solving is used for the domain decomposition approach. For the level-1 and level-2 meshes, each IR drop simulation requires 2911 and 5343 iterations while each thermal simulation requires 2217 and 4526 iterations, respectively.

Table 6. Material thicknesses and thermal conductivities.

	Thickness (mm)	Thermal Conductivity (W/mK)
PCB dielectric	0.35	0.8
PCB copper plane	0.03	400
Package dielectric	0.35	5
Package copper plane	0.02	400
Die	0.15	110
Underfill	0.2	0.4
C4	0.2	174
Solder bump	0.3	174
via	0.35	400
TIM	0.2	1.6
TSV	0.15	400

For comparison purposes, this example has also been simulated using the FEM with the conjugate gradient method and a diagonal pre-conditioner. The number of unknowns and solution times using the DDM and FEM with different mesh levels for both DC IR drop and thermal simulations are listed in Table 7. Note that the unknowns for DDM listed in Table 7 denote the number of unknowns for domain and interface. As seen from Table 7, the total number of unknowns using the DDM is reduced by 72-84% for DC IR drop and thermal simulation compared to the FEM. The total simulation time using the DDM is reduced by 64-88% for both DC IR drop and thermal simulations compared to the FEM. For the finite-element thermal simulation with 6.3 million unknowns, it cannot be solved because of finite memory in our simulation.

The simulated voltage and temperature with iterations are shown in Figure 47a and Figure 47b, respectively. The thermal simulation is carried out first in the co-simulation. It shows that the voltage and temperature both converge in four iterations. The total simulation time is 9785 s for four iterations. Note that the calculated chip IR drop is 30.6 mV at room temperature. As shown in Figure 47a, the final IR drop becomes 36.6 mV. Therefore, the thermal effect increases the voltage drop by 19.6%. Since the thermal simulation is carried out first, the temperature increase and extra voltage drop due to the Joule heating effect can be studied. The Joule heating effect on the voltage drop is about 2% in this example because of shunted power planes. As seen from Figure 47b, the Joule heating increases the PCB hotspot temperature about 8 degrees. Since on-chip power grids are not considered, the Joule heating only increases the chip temperature by 0.8 degree. To illustrate the independent meshing grids and scale difference for chip, package and board regions, the top overview of the final temperature distribution of this example is shown in Figure 48.

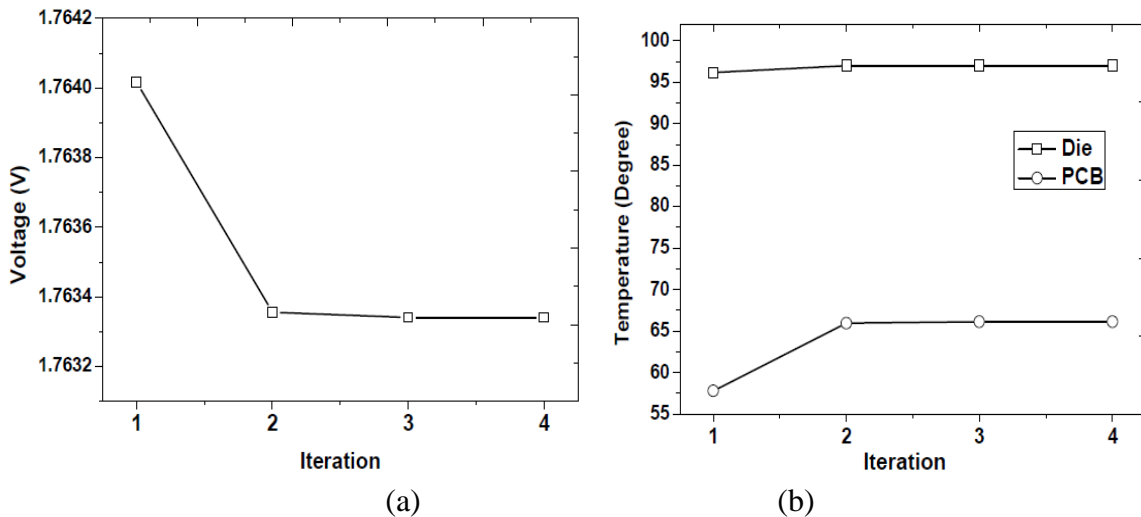
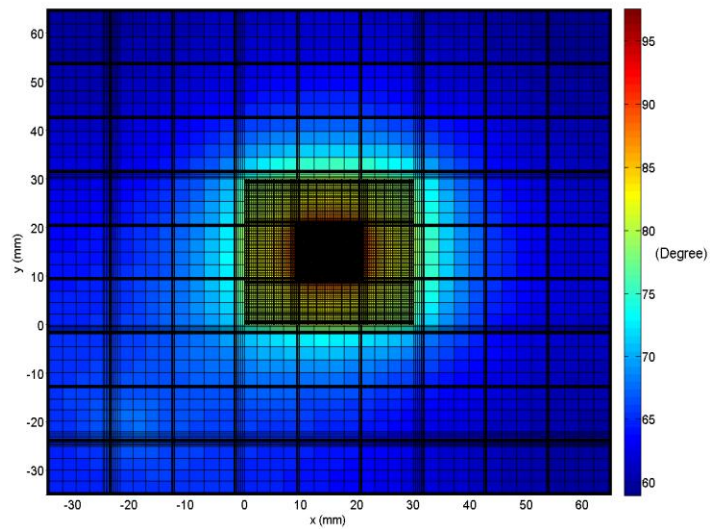


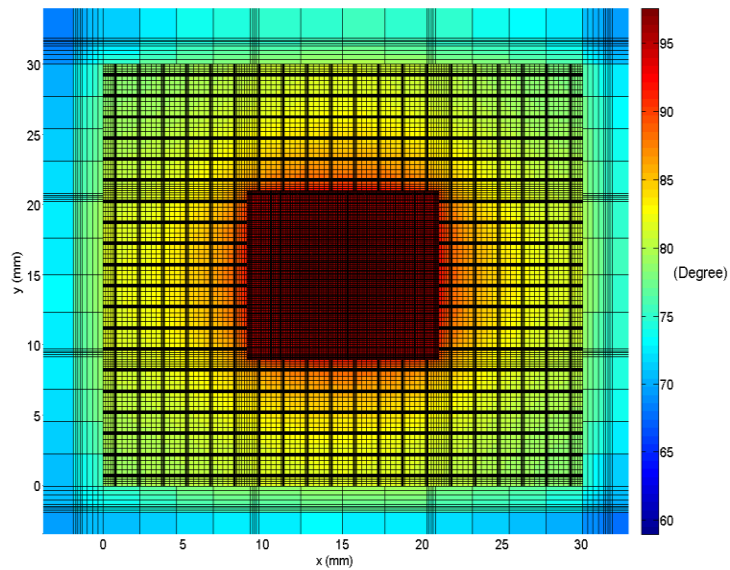
Figure 47. Simulated (a) die voltage, (b) die and PCB temperatures with iterations.

Table 7. Number of unknowns and solving times using the DDM and FEM.

		Level-0	Level-1	Level-2
IR drop (DDM)	unknowns (K)	24.6 (0.4)	80.5 (1.4)	292.1 (5.2)
	time (s)	0.65	166.2	748.6
IR drop (FEM)	unknowns (K)	89.2	336.9	1313.0
	time (s)	5.76	466.5	2122.7
Thermal (DDM)	unknowns (K)	63.0 (0.4)	245.3 (1.4)	968.1 (5.2)
	time (s)	15.4	416.9	1495.5
Thermal (FEM)	unknowns (K)	402.3	1592.1	6334.6
	time (s)	398.9	1599.6	/



(a)



(b)

Figure 48. Top overview of final temperature distributions of (a) chip, package and board, (b) enlarged chip and package domains.

B. A 2D Integration Example

A 2D integrated system with two chips has been simulated. The system is shown in Figure 49a. The PCB size is 10 cm \times 5 cm. As shown in Figure 49b, one metal layer of the PCB is used as the power plane with a 1.8 V voltage supply. In this example, equivalent thermal conductivities are used for the C4 layer and chip. The size of Chip 1 is 12 mm \times 12 mm, and the size of Chip 2 is 10 mm \times 10 mm. The PCB via size is 0.5 mm \times 0.5 mm. In this example, the minimum and maximum scales in the lateral direction are 500 microns and 10 cm, respectively. The geometrical and material parameters are summarized in Table 8. The power consumptions of Chip 1 and Chip 2 are 64 W and 40 W, respectively. Uniform power maps are used for both chips. This example has been simulated with a convection coefficient of 100 W/(m²K) on both sides of the PCB.

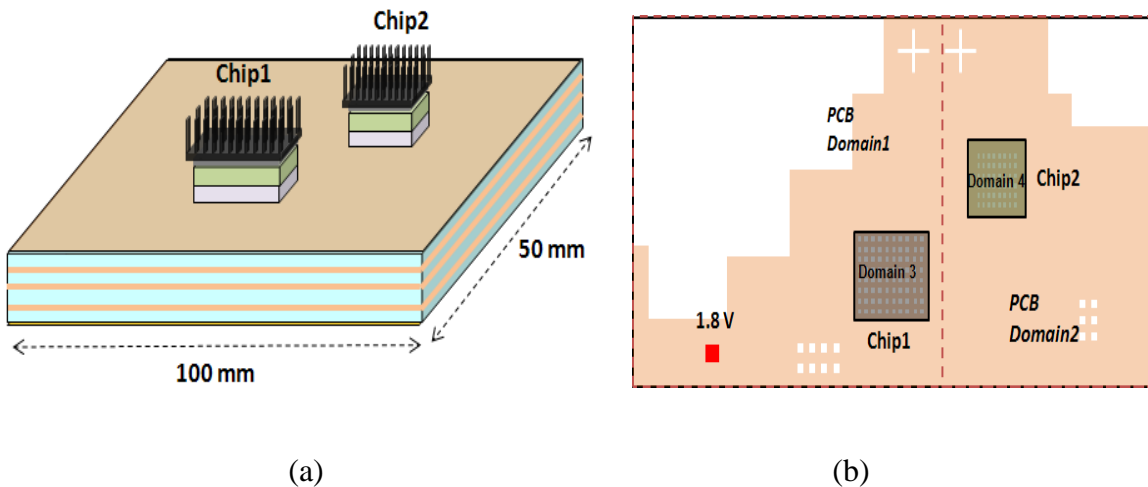


Figure 49. (a) An integrated system and (b) domain decomposition of the system.

This example is divided into four domains: two separate chip domains and two PCB domains, as illustrated in Figure 49b. Since equivalent thermal conductivities are used for the C4 layer and chip, to reduce the number of unknowns for the chip-package interface, the basis functions for the chip-package interface are chosen from the chip side. Because

of the independent meshing grids used for each domain, the total required meshed cells and unknowns are dramatically reduced, compared to the conventional FEM. For the initial mesh without domain decomposition, the FEM requires 121 K unknowns and 22.53 s solving time using a direct solver for each thermal simulation. However, using the domain decomposition approach, only 48 K unknowns are required for domains and 0.6 K unknowns for interfaces. As a result, the matrix equation can be solved using the same direct sparse solver in 3.77 seconds. For both the problems with level-1 and level-2 meshes, iterative solving is used for the domain decomposition approach. For the level-1 and level-2 meshes, each IR drop simulation requires 1644 and 2521 iterations while each thermal simulation requires 869 and 1314 iterations, respectively.

Table 8. Material thicknesses and thermal conductivities.

	Material Thickness (mm)	Thermal Conductivity (W/mK)
PCB dielectric	0.35	0.8
Copper	0.036	400
Chip	0.3	110
C4 layer	0.1	10
PCB via	0.35	400
TIM	0.2	1.0

The number of unknowns and solution times using the DDM and FEM with different mesh levels for both the voltage drop and thermal simulations are listed in Table 9. Note that the unknowns for the DDM listed in Table 9 denote the number of unknowns for domains and interfaces. As seen from Table 9, the total number of unknowns using the non-conformal DDM is reduced by 57% for the voltage drop simulation and 60% for the thermal simulation, compared to the FEM. The total simulation time using the DDM is reduced by 60%-75% for the voltage drop simulation and 42%-83% for the thermal

simulation, compared to the FEM, which uses the PCG method to solve the system equation.

Table 9. Number of unknowns and solving times using the DDM and FEM.

		Level-0	Level-1	Level-2
IR Drop (DDM)	unknowns (K)	22.1 (0.4)	84.4 (1.3)	328.42 (4.6)
	time (s)	0.66	98.9	281.1
IR drop (FEM)	unknowns (K)	52.90	206.01	811.92
	time (s)	1.67	367.5	1162.7
Therm. (DDM)	unknowns (K)	48.5 (0.6)	190.29 (1.7)	754.03 (5.3)
	time (s)	3.77	127.6	284.9
Therm. (FEM)	unknowns (K)	121.05	478.31	1901.55
	time (s)	22.53	223.1	744.2

The simulated voltages and temperatures with iterations are shown in Figure 50a and Figure 50b, respectively. The thermal simulation is first carried out in the co-simulation flow. It shows that the voltage and temperature both converge in four iterations. In the co-simulation, the stop criterion ϵ is set to be 1E-2 for both the voltage drop and thermal simulations. The total simulation time is 2749 s. For Chip 1 and Chip 2, compared to the initial IR drops of 78.8 mV and 86.4 mV at room temperature, the final IR drops become 95.8 mV and 104.1 mV (Figure 50a), respectively. Therefore, the thermal effect increases the IR drop by 21.6% and 20.4%, respectively. Since the thermal simulation is carried out first, the variations of voltage drop and temperature beyond the first iteration are caused by the Joule heating. As seen from Figure 50a, the Joule heating effect causes about 10 mV voltage drop. Therefore, the Joule heat effect on voltage drop is about 11% in this example. As seen from Figure 50b, the Joule heating only increases the temperatures of Chip1 and Chip2 by 1.6 and 0.5 degrees, respectively. However, the Joule heating increases the temperature of hotspot in PCB about 25 degrees (Figure 50b). This is

caused by the current crowding in the irregular power plane (Figure 51). To reduce the effect of Joule heating, more layers of power planes need to be used to reduce the current crowding effect. The final temperature and voltage distributions of the power plane layer are shown in Figure 51.

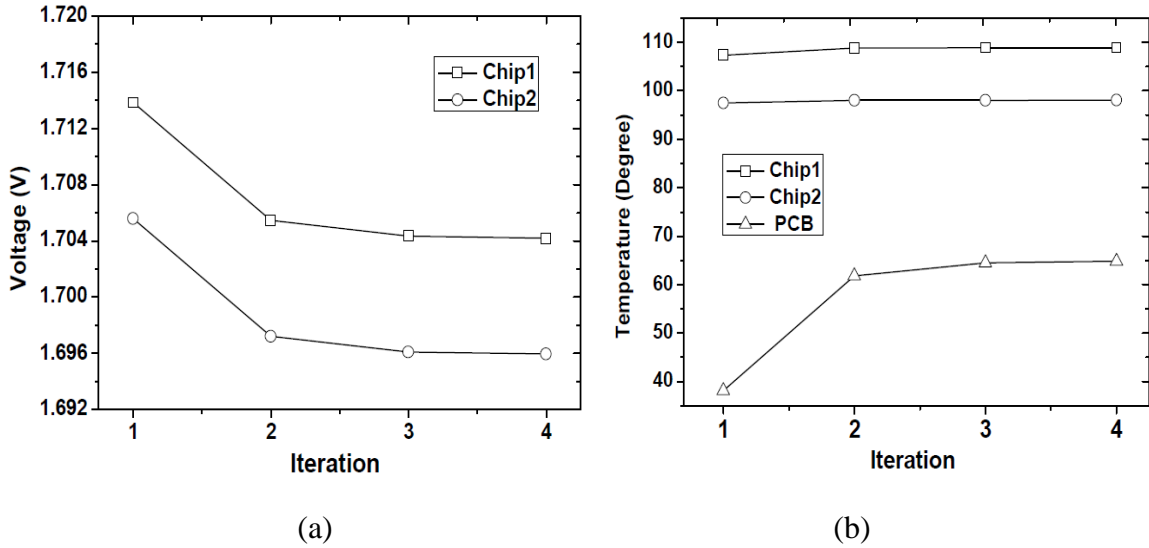


Figure 50. Simulated (a) DC voltage and (b) temperature with iterations.

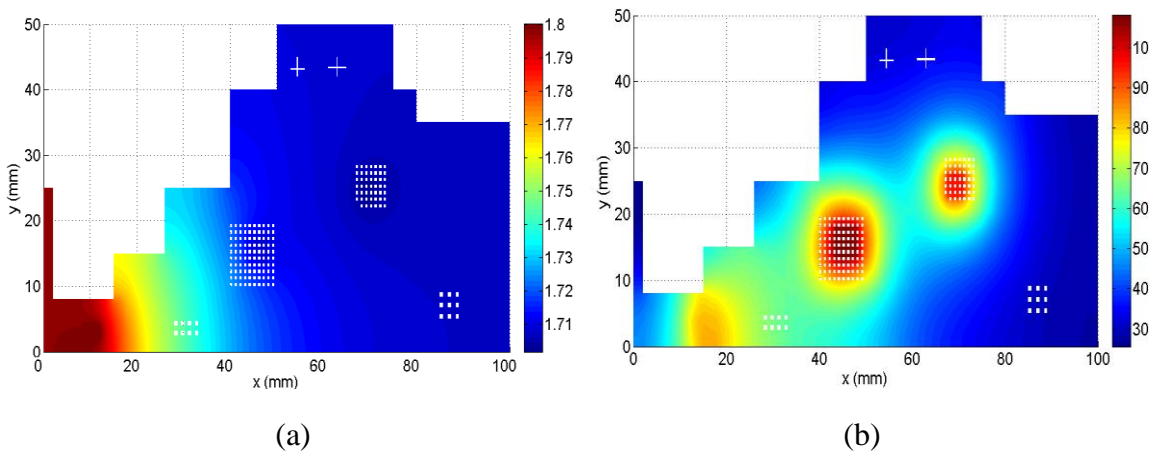


Figure 51. (a) Voltage distribution and (b) temperature distribution of the power plane.

4.5 Summary

In this chapter, multiscale modeling using the finite-element non-conformal domain decomposition is presented for the steady-state thermal and voltage drop analysis. The preliminaries for the finite-element thermal modeling are introduced. The formulation for the thermal modeling using the non-conformal domain decomposition is discussed in detail. In addition, the cascadic multigrid solving approach using hierarchical meshing grids is introduced for the voltage drop-thermal co-simulation with the computational cost discussed. The simulation efficiency of the voltage drop-thermal co-simulation using the non-conformal domain decomposition and CMG solving approach is demonstrated via numerical test cases. The simulation results show that using the finite-element non-conformal domain decomposition, the unknowns and mesh cells can reduce by 57%-84% for the voltage drop and thermal analysis, compared to the FEM. In addition, the simulation results demonstrate that using the domain decomposition and cascadic multigrid method with hierarchical meshing grids, the simulation efficiency can improve by 42%-88% for the voltage drop and thermal simulations, compared to that using the FEM and PCG solving method.

CHAPTER 5

TRANSIENT THERMAL MODELING WITH MICROFLUIDIC COOLING

5.1 Introduction

The estimation of dynamic temperatures for an electronic system requires efficient transient thermal modeling approaches. Transient numerical thermal modeling techniques can be classified into two categories: explicit methods and implicit methods. Explicit thermal modeling techniques recursively update temperatures at grid points at each time step based on the temperature obtained at the previous time step. As explicit techniques do not require solving system matrix equations, the memory requirement is not critical. However, the size of time step is restricted by the grid sizes in x, y, and z directions considering numerical stability [16]. Thus, performing transient thermal analysis over a large time period can require a large number of time steps, which is time consuming. To circumvent this problem, implicit thermal modeling methods such as the Crank–Nicolson method and the backward Euler method [16], which can simulate with large time steps, have been developed. As implicit thermal modeling methods require solving a large sparse matrix equation at each time step, the CPU time and memory consumption increase dramatically with the number of mesh cells/unknowns. For a 3D system with microfluidic cooling, the large number of micro-channels can lead to a greatly increased number of mesh cells, which poses a problem for transient thermal modeling.

In this chapter, an implicit transient thermal modeling approach is presented for thermal modeling with microfluidic cooling. The proposed transient modeling approach

can achieve fast temperature estimations using two techniques. First, to reduce the number of meshing cells for a 3D system, we extend the non-conformal domain decomposition technique to transient thermal modeling. Second, to accelerate the modeling of microfluidic cooling, a compact finite-volume thermal model has been developed for micro-channels. The proposed compact model can represent a microchannel using much fewer mesh cells/unknowns than that using the CFD approach. The transient thermal modeling using the non-conformal domain decomposition technique and the compact model for microfluidic cooling are discussed in the next two sections.

5.2 Transient Thermal Modeling using Domain Decomposition

For the transient thermal modeling of a 3D problem consisting of solid media, the governing transient heat equation is expressed as

$$\rho c_p \frac{\partial T(r,t)}{\partial t} - \nabla \cdot [k(r,T)\nabla T(r,t)] = P(r,t) \quad (37)$$

where $T(r,t)$ and $P(r,t)$ represent the temperature distribution and heat excitation, respectively; $k(r,T)$ is the thermal conductivity; ρ and c_p denote the mass density and heat capacity of the solid medium, respectively. Following the finite-element thermal modeling process, by multiplying a testing function N on both sides of Equation (37) and integrating over the volume, after using the divergence theorem, the new form of the heat equation can be obtained as

$$\iint_{\Omega} \rho c_p N \frac{\partial T}{\partial t} dV + \iint_{\Omega} k \nabla N \cdot \nabla T dV - \int_{\Gamma} k N \frac{\partial T}{\partial n} dS = \iint_{\Omega} N P dV \quad (38)$$

The non-conformal domain decomposition approach can also be applied to transient

thermal modeling. As shown in Figure 52a, in transient thermal modeling, similar to that of steady-state analysis, a 3D system can be divided into separate domains: the domain of chip, package, and PCB. For simplicity, the transient thermal analysis using the domain decomposition technique is explained using 2D rectangular grids shown in Figure 52a.

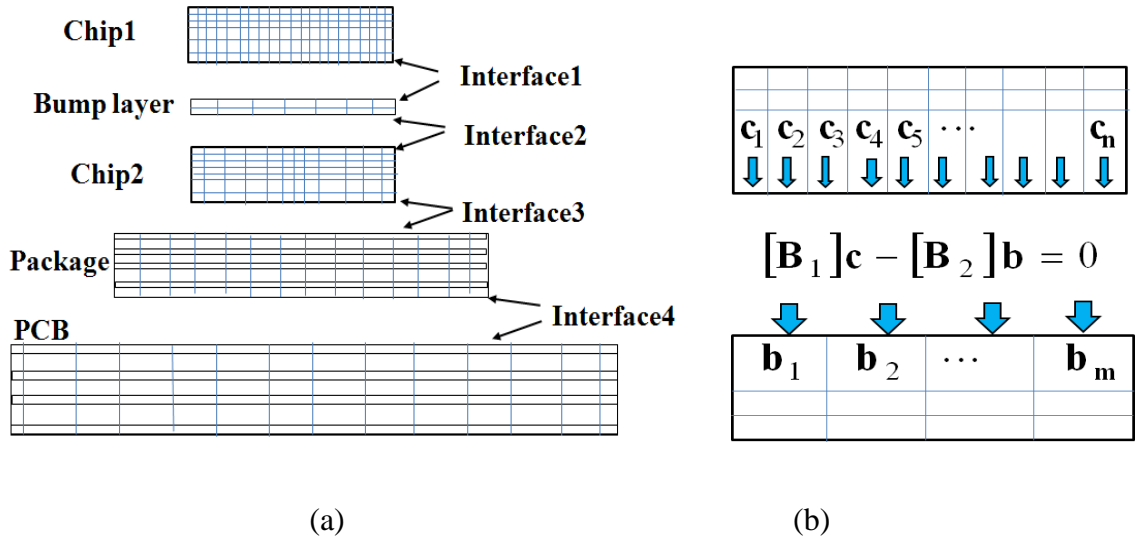


Figure 52. (a) Non-conformal gridding of a 3D system into domains, (b) heat flow continuity illustration. (Vectors c and b represent the coefficient of temperature basis functions.)

In transient thermal modeling, at each time step, the heat transferring out of one domain equals the heat flowing into another domain through the common interface. Two domains with a common interface are shown in Figure 52b. At the interface, the continuity of heat transfer needs to be ensured to capture the coupling between separated domains as in steady-state analysis. For two adjacent subdomains with a common interface (Figure 52b), by assuming $\lambda^{(i)} = k \partial T^{(i)} / \partial n_i$ ($i=1, 2$), we can also obtain the relationship of $-\lambda^{(1)} = \lambda^{(2)} = \lambda$ [41] as for steady-state analysis. Then the weak continuity of heat flow across the interface can be established at each time step. By introducing λ ,

the Lagrange multiplier, for each interface, the coupling between domains can be captured using coupling matrices B_1 and B_2 , as shown in Figure 52b. For simplicity, we can assume the system has only two separated domains.

Based on the introduced Lagrange multiplier and following the Mortar finite-element formulation, the following equations for domains and the interface can be derived from Equation (38) and expressed as

$$\begin{aligned}
& \iint_{\Omega_1} k \nabla N_1 \cdot \nabla T_1 dV - \int_{\Gamma_1} k N_1 \frac{\partial T_1}{\partial n} dt + \int_{\Gamma_{inter}} \lambda N_1 dt + \\
& \iint_{\Omega_1} \rho c_p N_1 \frac{\partial T}{\partial t} dV = \iint_{\Omega_1} N_1 P_1 dV \\
& \iint_{\Omega_2} k \nabla N_2 \cdot \nabla T_2 dx dy - \int_{\Gamma_2} k N_2 \frac{\partial T_2}{\partial n} dt - \int_{\Gamma_{inter}} \lambda N_2 dt + \\
& \iint_{\Omega_2} \rho c_p N_2 \frac{\partial T}{\partial t} dV = \iint_{\Omega_2} N_2 P_2 dx dy \\
& \int_{\Gamma_{inter}} (T_1 - T_2) \psi dt = 0
\end{aligned} \tag{39}$$

where N_1 , N_2 , and ψ represent the basis functions for domain1, domain2, and the Lagrange multiplier, respectively [82, 83]. With temperature T being expressed as a

linear combination of basis functions and $\lambda = \sum_{i=1}^{n_i} b_i \psi_i$, the system equation for the

problem with two subdomains can be written as

$$\begin{bmatrix} C_1 & & \\ & C_2 & \\ & & 0 \end{bmatrix} \dot{T} + \begin{bmatrix} K_1 & & B_1^T \\ & K_2 & -B_2^T \\ B_1 & -B_2 & 0 \end{bmatrix} T = \begin{bmatrix} p_1 \\ p_2 \\ 0 \end{bmatrix} = p \tag{40}$$

where the matrix entries for the k -th domain can be expressed as

$$\begin{aligned}
K_{k(ij)} &= \iint_{\Omega_k} k \nabla N_i^{(k)} \cdot \nabla N_j^{(k)} dV - \int_{\Gamma_k} k N_i^{(k)} \frac{\partial N_j^{(k)}}{\partial n} dt \\
C_{k(ij)} &= \iint_{\Omega_k} \rho c_p N_i^{(k)} N_j^{(k)} dV \\
B_{k(ij)} &= \int_{\Gamma_{inter}} \psi_i N_j^{(k)} dt \quad p_{k(j)} = \iint_{\Omega_k} N_j^{(k)} P dV
\end{aligned} \quad (k = 1, 2) \tag{41}$$

In the above equations, K_k , B_k , and C_k represent the impedance, coupling, and capacitance matrices for the k -th domain, respectively; p_k represents the excitation vector for the k -th domain. By using the backward time-difference approximation

$$\dot{T} = \frac{T^{(n+1)} - T^{(n)}}{\Delta t} \quad (42)$$

Equation (40) can be converted as a linear equation as

$$AT^{(n+1)} = \begin{bmatrix} A_1 & & B_1^T \\ & A_2 & -B_2^T \\ B_1 & -B_2 & 0 \end{bmatrix} \begin{bmatrix} T_1^{(n+1)} \\ T_2^{(n+1)} \\ T_{inter} \end{bmatrix} = \begin{bmatrix} f_1^{(n)} \\ f_2^{(n)} \\ 0 \end{bmatrix} = f^{(n)} \quad (43)$$

where

$$A_i = \frac{C_i}{\Delta t} + K_i, f_i^{(n)} = \frac{C_i}{\Delta t} T_i^{(n)} + p_i \quad (i=1, 2)$$

Here, the superscripts $(n+1)$ and n represent time steps. The matrix A_i represents the stiffness matrix for the i -th domain. $T_i^{(n+1)}$ represents the temperature vector of the i -th domain at time step $(n+1)$. $f_i^{(n)}$ denotes the heat excitation in the i -th domain calculated from time step n . Note that the numerical scheme based on the CN (Crank–Nicolson) method [16], which has second-order accuracy in time, can also be obtained by using $(T^{(n+1)} + T^{(n)})/2$ to approximate the term T in Equation (40). However, the CN scheme has a time step limitation that can result in temperature oscillations when using large time steps [17]. Therefore, the scheme of Equation (43), which is based on the backward Euler method, is employed in our transient simulation. Similarly, for a system with N subdomains, the generalized system equation can be derived and obtained using the superposition rule.

For the efficient simulation of 3D stacked ICs using the DDM, it is important to note that the connection between chip domains is through the transitional subdomain of a bump layer, as shown in Figure 52a. Since the domain of a bump layer can be meshed using much coarser grids than the chip, the required interface basis functions can be greatly reduced. Thus, B matrix has a small dimension. It should be noted that for efficient transient thermal simulation with fluidic cooling, in addition to the non-conformal domain decomposition modeling technique, the compact thermal model for microfluidic cooling needs to be developed, which is discussed in the next section.

5.3 Compact Thermal Modeling for Microfluidic Cooling

Because of the large number of microchannels used for the cooling of 3D ICs, the fast temperature estimation at early-design stage requires compact thermal modeling of microchannels to overcome the simulation inefficiency using CFD approaches. For a coolant flow in the microchannel of IC chips, the Reynolds number is usually less than 2300; thus, the flow is laminar [77]. Since the longitudinal dimension of microchannels is much larger than the lateral dimension, the microfluidic flow can be treated as a fully developed laminar flow, as discussed in Chapter 3. This property allows the development of compact models for microfluidic cooling. The governing heat equation for the transient thermal analysis of microfluidic cooling is expressed as

$$\rho c_p \left(\frac{\partial T(r,t)}{\partial t} + \bar{v} \cdot \nabla T(r,t) \right) = \nabla \cdot (k_f \nabla T(r,t)) + P_f(r,t) \quad (44)$$

where $T(r,t)$ and $P_f(r,t)$ represent the temperature distribution and heat excitation, respectively; k_f and \bar{v} are the thermal conductivity and velocity of the fluid; ρ and c_p denote the mass density and heat capacity of the fluid, respectively. To simplify the

problem, the thermal conductivities of fluid and solid media are both considered without temperature variations in thermal modeling. Compared to the heat equation (37) for solid media, Equation (44) has an extra term related to the coolant flow velocity \bar{v} . For heat transfer using a coolant flow, the process consists of heat conduction because of the finite thermal conductivity and heat transportation because of the flow velocity. In Equation (44), except for the second term on the left-hand side related to flow velocity, other terms can be modeled as a solid medium.

The discretization of a microchannel and a unit cell is shown in Figure 53. For microfluidic cooling as shown in Figure 53, since the microchannel cross-sectional dimension is much smaller than its length, the flow velocity along the longitudinal direction is much larger than that in the lateral direction. Thus, it can be assumed that the coolant only flows in the longitudinal direction. Therefore, the flow velocity is constant. The average flow velocity ‘ v ’ along y direction, as shown in Figure 53, has been used for simulating the fluid flow as for steady-state analysis. As a result, Equation (44) can be transformed as

$$\rho c_p \left(\frac{\partial T(r,t)}{\partial t} + v \frac{\partial T(r,t)}{\partial y} \right) = \nabla \cdot (k_f \nabla T(r,t)) + P_f(r,t) \quad (45)$$

By integrating Equation (45) over the dashed finite volume cell (Figure 53) and applying the divergence theorem, Equation (45) can get rid of the second-order derivative and becomes

$$\int_{cell} \rho c_p \frac{\partial T(r,t)}{\partial t} dV + \int_S \rho c_p v T \hat{y} \cdot \hat{n} dS = \int_S k_f \nabla T \cdot \hat{n} dS + \int_{cell} P_f dV \quad (46)$$

where S is the surface of the finite volume cell. Note that in steady-state analysis, the 4×4 meshing grids, which contain 9 nodes for one fluidic cell, are used for the cross-section

of the microchannel. For efficient transient thermal simulation, instead of using 9 nodes to represent one microchannel cell, the proposed model only uses one node to represent one microchannel cell to reduce the computational cost, as shown in Figure 53.

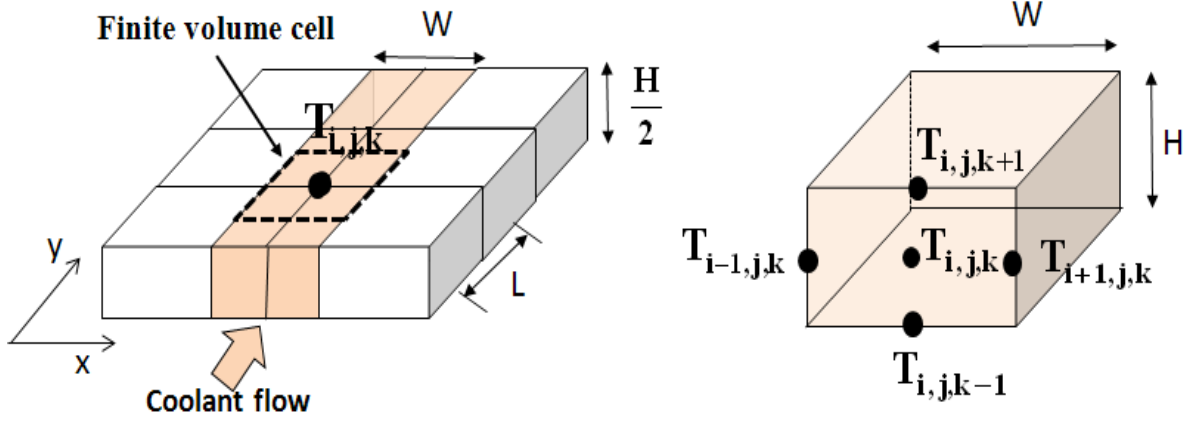


Figure 53. Discretization of a microchannel into cells. (Only bottom half part of the microchannel is shown on the left figure.)

To maintain the numerical stability, the same backward-difference approximation is used to approximate the second term on the left-hand side of Equation (46) as for the steady-state analysis. By applying the finite-difference approximation to Equation (46) and incorporating the convection boundary condition (assuming a convection coefficient of h_s at four sides of the channel), the finite-volume scheme for fluid flow can be derived as

$$\begin{aligned}
 & \frac{T_{i,j,k} - T_{i-1,j,k}}{W/2} + \frac{T_{i,j,k} - T_{i+1,j,k}}{W/2} + \frac{T_{i,j,k} - T_{i,j,k-1}}{H/2} + \frac{T_{i,j,k} - T_{i,j,k+1}}{H/2} + \frac{T_{i,j,k} - T_{i-1,j,k}}{1} + \\
 & \frac{T_{i,j} - T_{i+1,j,k}}{1} + \frac{T_{i,j,k} - T_{i,j,k-1}}{1} + \frac{T_{i,j,k} - T_{i,j,k+1}}{1} + \sigma c_p m (T_{i,j,k} - T_{i,j-1,k}) + \sigma c_p V_c \frac{\partial T}{\partial t} = P_f V_c
 \end{aligned} \quad (47)$$

where $V_c = WHL$ is the cell volume and $m = vWH$ is the volumetric flow rate.

Based on the scheme of Equation (47), an equivalent circuit representation of the fluidic cell is shown in Figure 54a. Since the solid medium is modeled using the FEM and the fluidic cooling is modeled using the FVM, the integration of these two models is required. As shown in Figure 54b, the connection between the finite-element model for solid and finite-volume model for fluid is formed using the forced convection boundary condition. The forced convection is indicated using arrows in Figure 54b. Since the convection boundary effectively captures the heat transfer from the chip to microchannel, the integration of these two models becomes feasible by following the energy conservation rule. The convection strength, the average convection coefficient h_s , at the four sides of the microchannel can be obtained analytically using Equation (16) as in Chapter 3. The Nusselt number can be obtained using Equation (15).

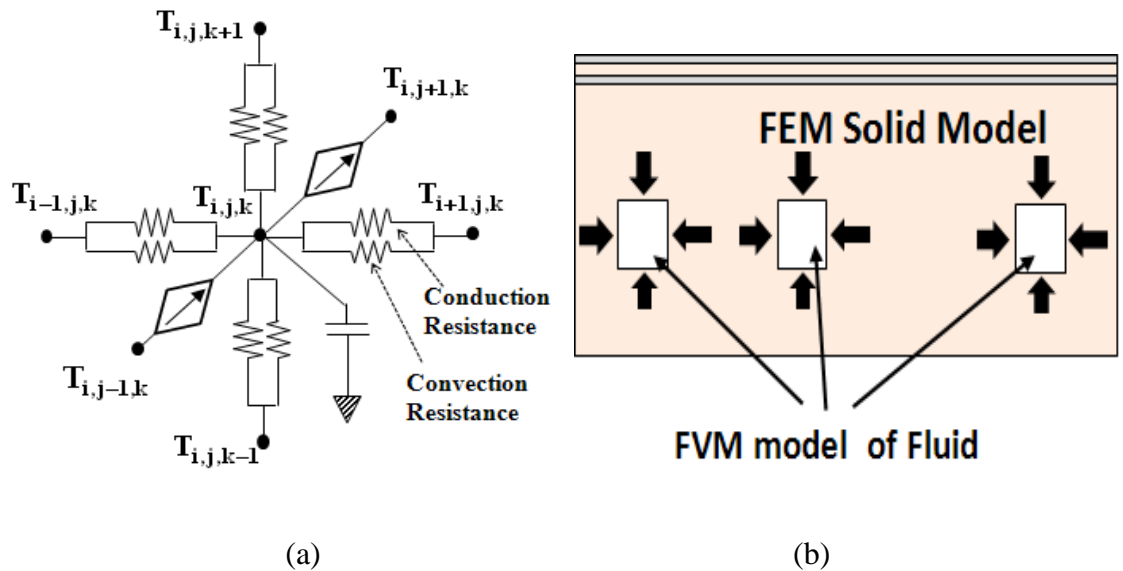


Figure 54. (a) An equivalent circuit model for one fluidic cell, (b) forced convection boundaries between solid and fluid media.

5.4 Test Cases

5.4.1 A Model-Verification Example

To evaluate the accuracy of the proposed method, an experimental example, the test set 1, with both the conventional heat sink and fluidic cooling is simulated. The test set 1 is shown in Figure 55. The test vehicles in Figure 55a and Figure 55b use heat-sink cooling and fluidic cooling, respectively. The chip size is $1\text{ cm} \times 1\text{ cm}$, and the uniform power consumption is 45 W . In the test vehicle shown in Figure 55b, 51 microchannels are uniformly distributed on the chip as described in [4]. The cross-sectional dimension of each micro-channel is $0.1\text{ mm} \times 0.2\text{ mm}$. The temperature of input water at the inlets of microchannels is set to be $22\text{ }^\circ\text{C}$ as in the measurement. Because of the scale difference between the chip and package, the examples in Figure 55a and Figure 55b are both divided into two domains: the chip domain and package domain. The detailed material properties and geometrical information are listed in Table 10. Since the measurement [4] was carried out at the condition of natural convection, a convection coefficient of $5\text{ W}/(\text{m}^2\text{ K})$ is applied to both the top and bottom surfaces of the package in the simulation. The initial system temperature is 25 Celsius.

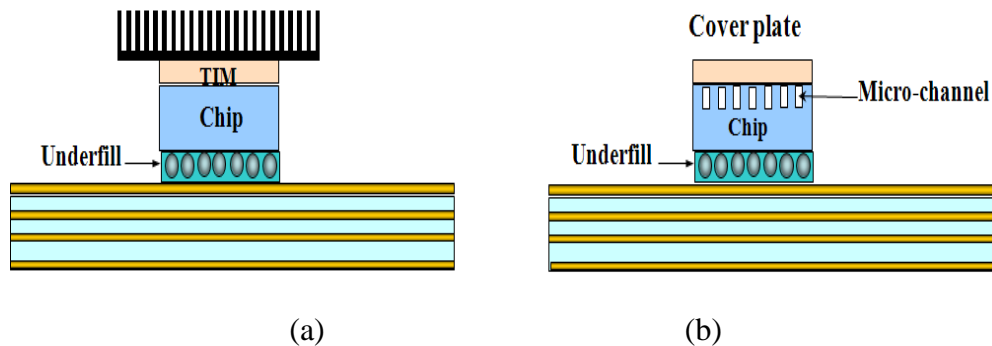


Figure 55. Test set 1 with (a) heat-sink cooling and (b) microfluidic cooling.

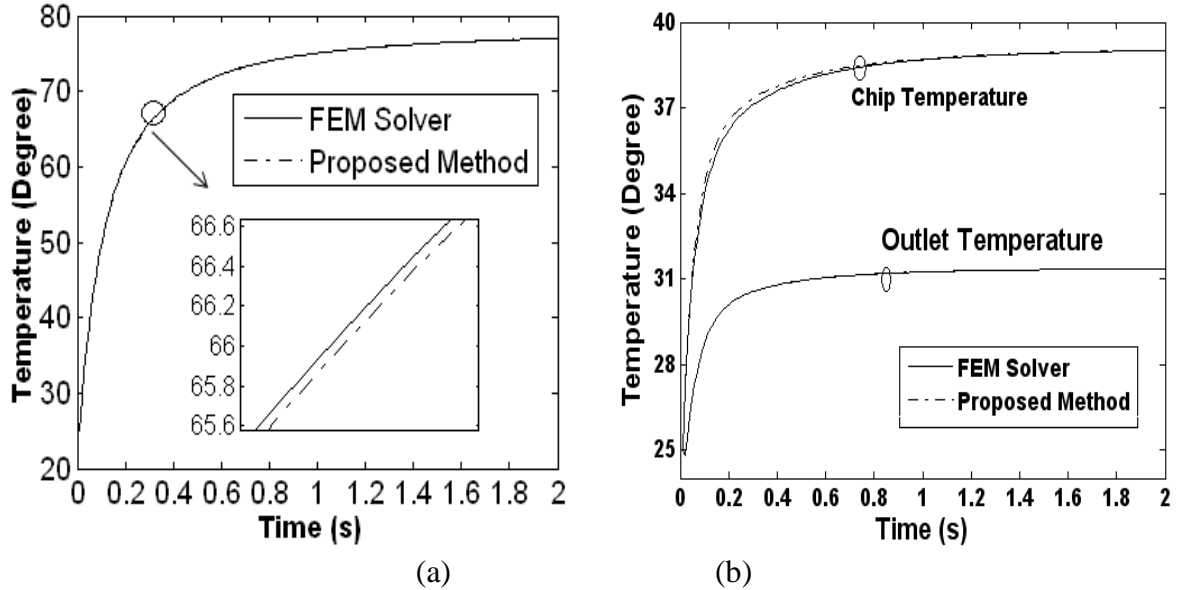


Figure 56. Comparison of temperature waveforms using the proposed method and conventional FEM with (a) heat-sink cooling, (b) fluidic cooling.

This test vehicle with heat-sink cooling and fluidic cooling has been simulated using the proposed method and a conventional FEM solver. The non-conformal and conformal rectangular meshing grids have been used for the proposed method and the FEM solver, respectively. Note that the compact model for microchannels is incorporated into the FEM solver. With heat-sink cooling, the comparison of simulated chip temperatures is shown in Figure 56a. With fluidic cooling, the comparisons of simulated chip temperatures and channel outlet temperatures are shown in Figure 56b. As seen from Figure 56, the results from the proposed model using domain decomposition agree very well with results from the conventional FEM solver. The maximum temperature difference is less than 0.2 and 0.5 degree for the cooling using a heat sink and using microchannels, respectively. For microfluidic cooling, the measured steady-state chip temperature and outlet temperature are 40.8 and 32.2 Celsius in [4]. The difference between the simulated converged chip temperature and measurements [4] is 1.7 Celsius

while the difference between the simulated channel outlet temperature and measurements is 0.4 Celsius. The relative errors are about 4.2% and 1.2% with respect to the measurements, respectively. The unknowns (including the unknowns for interfaces) and simulation times using the proposed method and FEM are shown in Table 11. It shows that the proposed method can reduce unknowns about 2-4 times. Because of the reduced unknowns, the simulation time speed up can reach 35x for the simulation with fluidic cooling.

Table 10. Material properties and geometrical information.

Test set 1	
Number of layers	4 (die: 10 mm x 10 mm) 4 (package: 4 cm x 4 cm)
Channel width * height * length	0.1 mm x 0.2 mm x 10 mm
Channel pitch	196 micron
Bottom and top silicon height	100 micron, 0 micron
Fluid flow rate	65 mL/ min
Pyrex glass heat capacity, thermal conductivity	820 J/Kg-K, 1.1 W/m-K
TIM heat capacity, thermal conductivity	610 J/Kg-K, 1.6 W/m-K
Heat sink boundary temperature	25 Celsius
Test set 2	
Number of layers	4 (die: 10 mm x 10 mm), 4 (package: 3 cm x 3 cm) 10 (board: 10 cm x 10 cm)
Channel width * height * length	0.2 mm x 0.1 mm x 10 mm
Channel pitch	500 micron
Top and bottom silicon height	50, 50 micron
Fluid flow rate (per chip)	26 mL/min
Common Parameters	
Thermal conductivity of fluid, silicon, BEOL	0.6, 110, 2 (W/m-K)
Heat capacity of fluid, silicon, BEOL layer	4187, 700, 520 (J/Kg-K)
Ambient temperature	25 Celsius

Table 11. Comparisons of problem sizes and simulation times.

		DDM Solver		FEM Solver		Time Speed-up
		Size (K)	Time (s)	Size (K)	Time (s)	
Test Set1	Fluidic cooling	50.4	5.59	157.02	201.2	x35
	Heat sink	36.9	6.84	189.1	30.2	x4
Test Set2	3D system	35.1	3.41	206.61	315.1	x91
	3D ICs only	32.2	2.68	107.84	196.2	x72

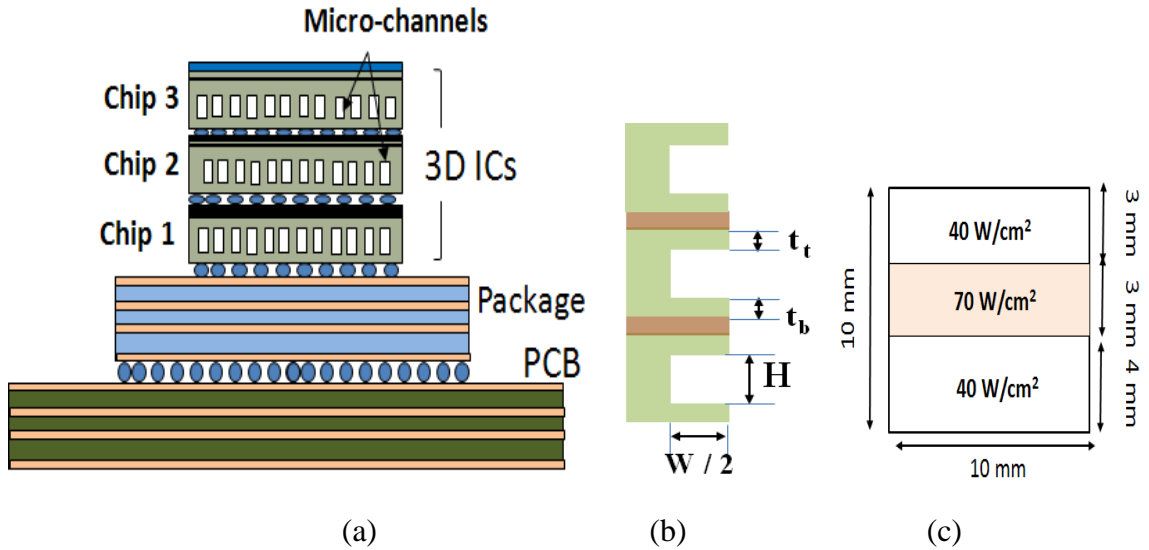


Figure 57. (a) A 3D system with microfluidic cooling, (b) layer cross-section of stacked chips, (c) the power map of chip 2.

5.4.2 A 3D Stacking Example

A 3D stacking example (Test set 2) with inter-tier microfluidic cooling is also simulated using the proposed method. The 3D system consists of three stacked chips, a four-layer package, and a 10-layer PCB, as shown in Figure 57a. Each chip has 20 microchannels. The layer stack-up for the stacked chip and microchannels is shown in Figure 57b. The geometrical and material parameters are summarized in Table 10. Air convection with a heat transfer coefficient of $10 \text{ W}/(\text{m}^2\text{K})$ is applied to the top surface of the package and both sides of the PCB. Three chips are supplied with the same water flow rate. Non-

uniform heat dissipation is used for chip 2, as shown in Figure 57c. A uniform power consumption of 40 W/cm^2 is used for both chip 1 and chip 3.

This test set is divided into seven domains: three chip domains, two domains for micro-bump layers, one package domain, and one PCB domain. The three chips are independently meshed using different mesh sizes. This example is simulated for 2.2 s. In the first second, the three chips operate with a uniform power density of 40 W/cm^2 . From 1.0 s-2.0 s, the 3 mm-wide middle region of chip 2 (Figure 57c) is switched between 70 W/cm^2 and 40 W/cm^2 periodically. The simulated temperatures using the proposed method and conventional FEM are shown in Figure 58. It shows the simulated results using the proposed method agree very well with that using the FEM. The maximum temperature difference is less than 0.5 degree, and the temperature error is about 1%. From Figure 58, it is also observed that because of the convection on the package and PCB, the bottom chip temperature is about 3 Celsius lower than the top chip. To show the capability of simulating only 3D ICs, the example in Figure 57a is also simulated without the IC package and PCB. The comparisons of required unknowns and simulation times are shown in Table 11. As seen from Table 11, the proposed method can reduce unknowns about 2.3-4.9 times for simulating the 3D ICs and 3D system. Because of the reduced unknowns, a simulation speed up to 91x can be achieved, indicating the efficiency of the proposed method. The side view (in yz plane) of the temperature distribution of stacked chips at $t = 1.9 \text{ s}$ is shown in Figure 59 with the non-conformal gridding and hotspot illustrated. The snapshots of temperature distribution (in yz plane) with the evolution of time are shown in Figure 60.

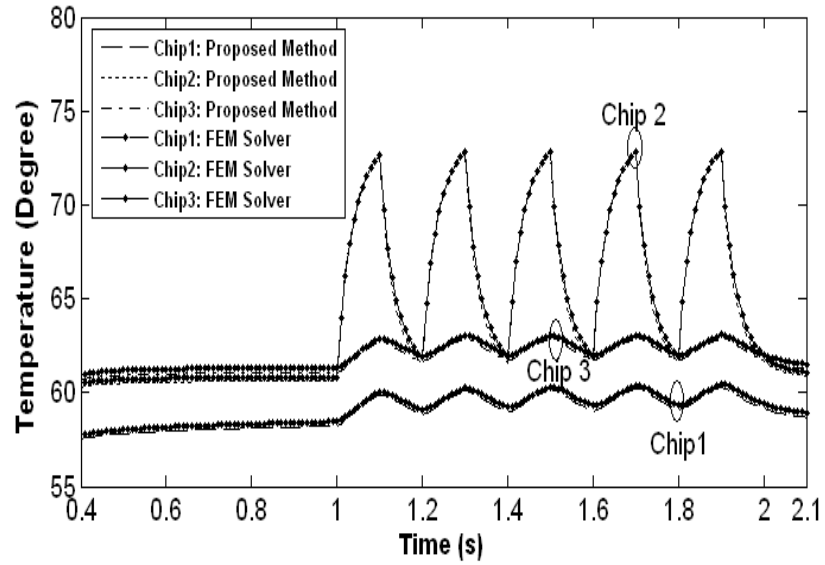


Figure 58. Comparison of temperature waveforms using the proposed method and FEM.

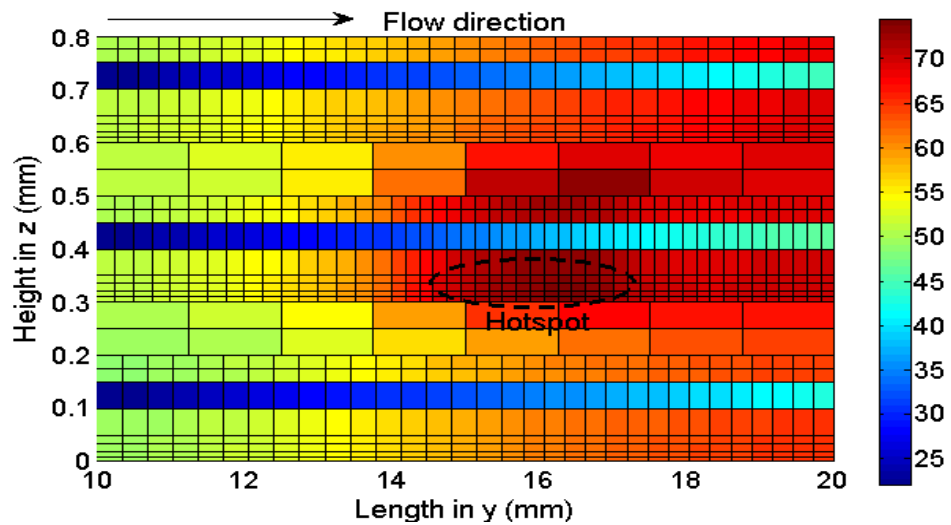


Figure 59. Side view (in yz plane) of temperature distribution at $t = 1.9$ s.

5.5 Summary

In this chapter, the transient thermal modeling using the compact thermal model for microchannels and the non-conformal domain decomposition is proposed. The non-

conformal domain decomposition technique is extended to transient thermal modeling. The derivation of the compact thermal model for microchannels using the finite-volume formulation is discussed in detail with an equivalent circuit model presented. In addition, the formulation also shows that by following the energy conservation rule, the finite-element model for a solid chip and the finite-volume model for microchannels can be integrated together. The efficiency of the proposed transient thermal modeling approach has been validated using several simulation examples.

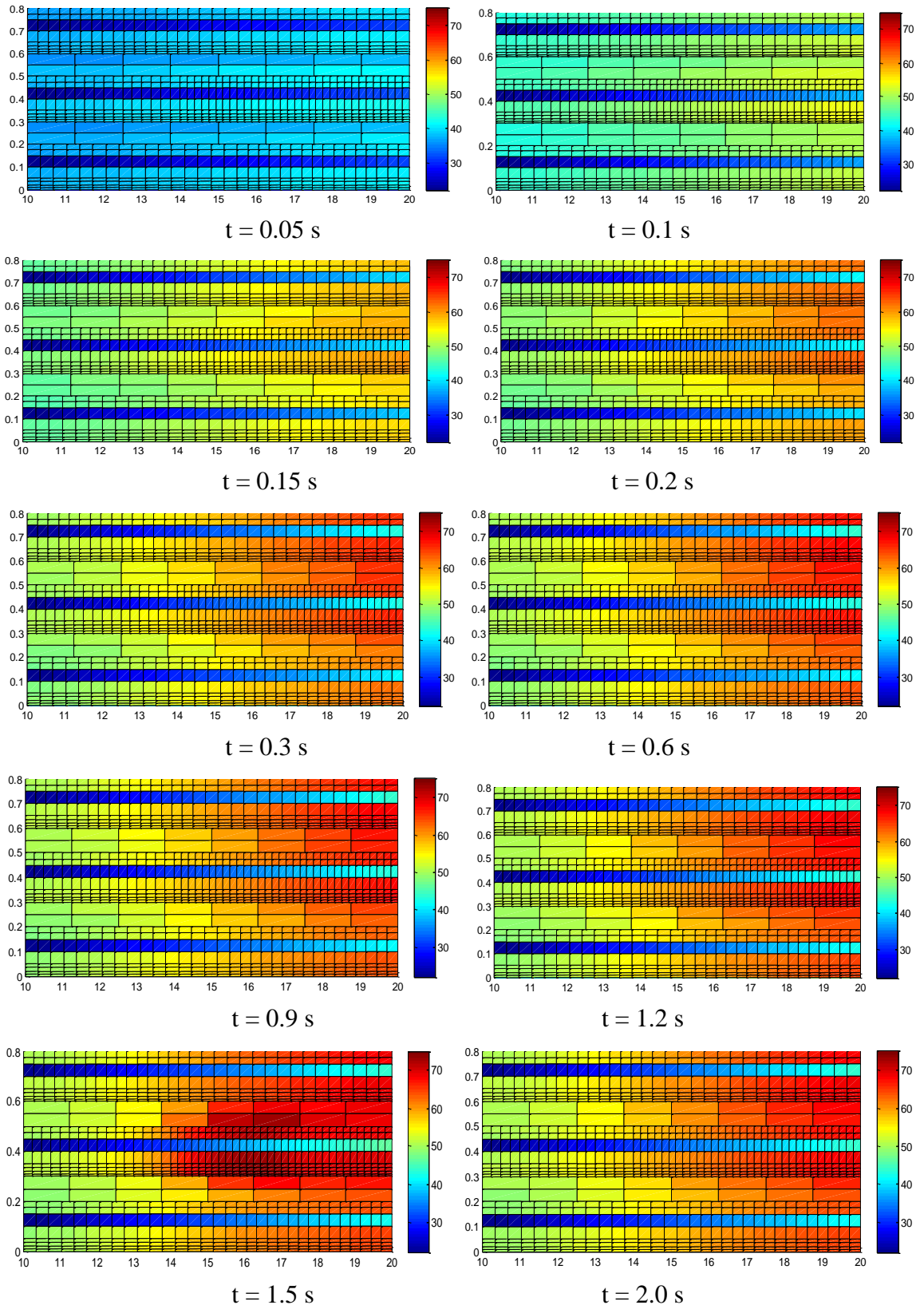


Figure 60. Snapshots of temperature with the evolution of time (unit: Celsius).

CHAPTER 6

SYSTEM-LEVEL THERMAL MODELING USING DOMAIN DECOMPOSITION AND MODEL ORDER REDUCTION

6.1 Introduction

Krylov space-based model order reduction techniques such as the block Arnoldi algorithm [58] and PRIMA [52] can create a low-dimensional reduced-order model to represent a large-dimensional model by constructing the congruence transformation matrix. The general reduced-order modeling process using Krylov space-based model order reduction is shown in Figure 61. These Krylov space-based MOR techniques have been promising for the steady-state and transient thermal modeling of devices and IC chips [59, 60, 61]. As the computation of the congruence transformation matrix requires solving a sparse matrix equation many times to match moments (Figure 61), the computational cost increases dramatically with the number of unknowns and MOR ports. Therefore, MOR techniques are favorable for thermal problems with a small-sized matrix and few MOR ports.

A typical 3D system can consist of several dies, an interposer (or a package), and a PCB, as shown in Figure 1. The total number of unknowns of a 3D problem can vary from 50 K to several million. Because each die can have tens of MOR ports, the whole system can have 100-1000 MOR ports. In addition, an integrated system can have tunable design parameters such as the thermal conductivity of a certain layer (e.g., the layer of TIM or interposer) and the varying air convection coefficients on different sides of package. Therefore, 2-5 degrees of freedom can be added to the system. With a limited

memory (e.g., 2-3 GB), performing MOR for a 3D system with hundreds of ports and 0.1-1.0 million unknowns becomes challenging. Several MOR examples reported in the literature have less than one hundred MOR ports [62, 63]. As the computational complexity of MOR increases dramatically with the number of ports, directly creating a ROM for the entire system using existing MOR techniques such as PRIMA becomes challenging when the size of the system matrix is large and many ports are present. Although Krylov space-based matrix-solving techniques [37, 78, 86] can be used to compute projection matrices during the process of MOR, the time consumption increases dramatically because of iterative solving procedures.

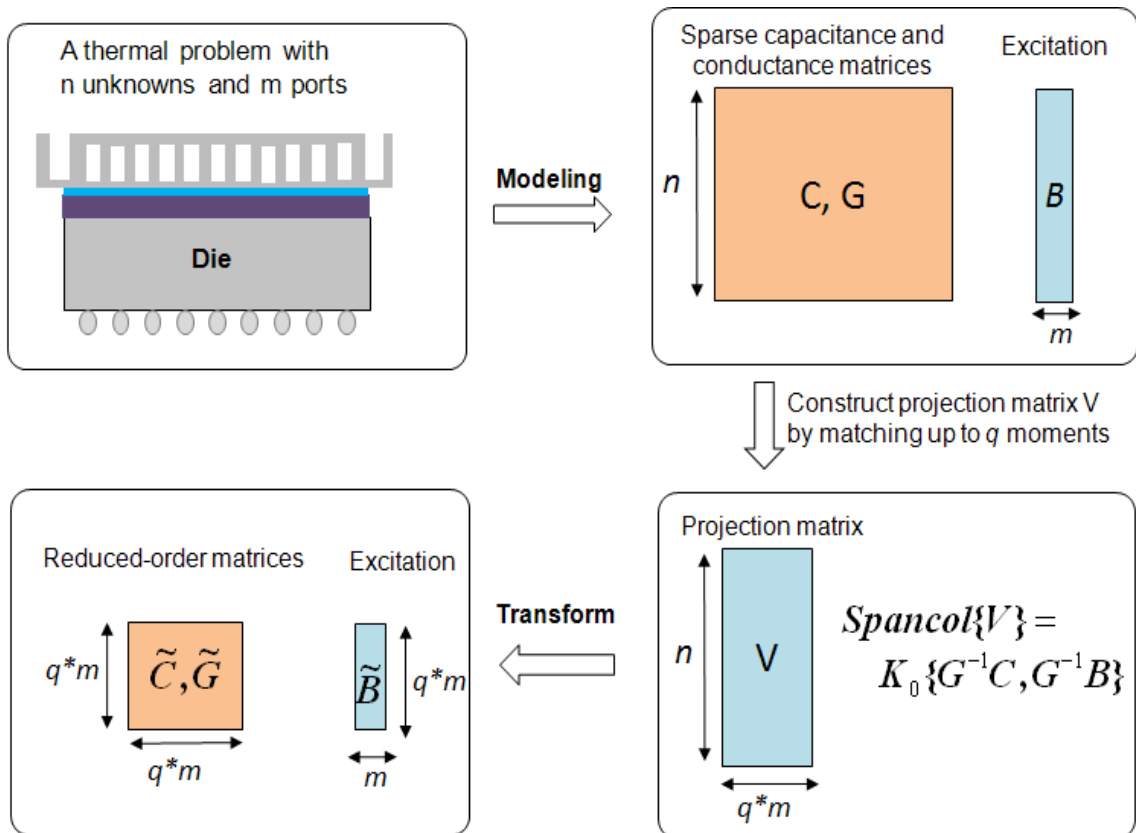


Figure 61. A general reduced-order modeling process using Krylov space-based model order reduction.

In this chapter, the system-level thermal modeling method using the non-conformal domain decomposition and model order reduction is presented. The presented modeling approach can efficiently support both steady-state and transient system-level modeling of 3D systems. To model a 3D system, the system is divided into domains with non-matching grids at interfaces, which helps reduce the system matrix size. Meanwhile, the MOR ports are also divided into groups belonging to different domains (e.g., dies or layers). Therefore, both the matrix size and port number associated with an individual domain are reduced. Thus, reduced-order models for separated domains can be efficiently created using MOR techniques with less computational cost than directly performing MOR for the entire system. The relationship between domains is captured using interfacial coupling matrices via Lagrange multipliers and Schur complements; therefore, interfacial MOR ports are not required. In addition, since individual domains are treated independently, the proposed method can efficiently handle varying parameters such as the thermal conductivities of TIMs and interposers and air convection coefficients when simulating 3D stacked ICs or systems.

6.2 Preliminaries

This section provides a brief summary of the thermal modeling using domain decomposition, which is presented in Chapter 5, with a generalized formulation for n sub-domains for completeness. For transient thermal modeling using the non-conformal DDM, by constructing the finite-element basis functions for each domain and interface, the following matrix equation can be derived for a system divided into n domains:

$$Cx = -Gx + f \quad (48)$$

where

$$C = \begin{bmatrix} C_d & \\ & 0 \end{bmatrix} \quad G = \begin{bmatrix} G_d & E^T \\ E & 0 \end{bmatrix} \quad x = \begin{bmatrix} x_d \\ x_{inter} \end{bmatrix} \quad f = \begin{bmatrix} f_d \\ 0 \end{bmatrix}$$

$$C_d = \begin{bmatrix} C_1 & & & \\ & C_2 & & \\ & & \ddots & \\ & & & C_n \end{bmatrix} \quad G_d = \begin{bmatrix} G_1 & & & \\ & G_2 & & \\ & & \ddots & \\ & & & G_n \end{bmatrix} \quad x_d = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_n \end{bmatrix} \quad f_d = \begin{bmatrix} f_1 \\ f_2 \\ \vdots \\ f_n \end{bmatrix} \quad E^T = \begin{bmatrix} E_1^T \\ E_2^T \\ \vdots \\ E_n^T \end{bmatrix} \quad (49)$$

In the above equation, C_d and G_d represent the block-diagonal thermal capacitance and conductance matrices for domains, respectively; C_i and G_i represent the capacitance and conductance matrices for the i -th domain with homogenous Neumann boundary conditions at interfaces, respectively; x_d and x_{inter} are the temperature of domains and unknowns of interfaces, respectively; x_i denotes the temperature of the i -th domain while matrix E_i represents the coupling matrix between the i -th and other domains; f_i is the thermal excitation for the i -th domain. Note that the finite element method [79] is used to construct the aforementioned capacitance/conductance matrices and excitation vectors, as discussed in Chapter 5.

The dimension of the E matrix is $m \times N$, where N and m are the total numbers of unknowns for domains and interfaces, respectively. Assuming the number of basis functions used for the interface of i -th domain is m_i , m can be expressed as $m = \sum_{i=1}^{n_{inter}} m_i$.

For transient thermal modeling, assuming the backward Euler scheme is used to approximate the time derivative at time step $(q+1)$ as

$$\dot{x} = (x^{(q+1)} - x^{(q)}) / \Delta t \quad (50)$$

the following equation can be obtained:

$$Kx^{(q+1)} = p^{(q)} \quad (51)$$

where

$$K = \begin{bmatrix} K_d & E^T \\ E & 0 \end{bmatrix} = \begin{bmatrix} C_d / \Delta t + G_d & E^T \\ E & 0 \end{bmatrix}$$

$$p^{(q)} = f + \frac{C}{\Delta t} x^{(q)} = \begin{bmatrix} f_d + C / \Delta t \cdot x_d^{(q)} \\ x_{inter}^{(q)} \end{bmatrix}$$

To obtain transient temperature responses, Eqn. (51) needs to be solved using a direct solver or an iterative solver at each time step. Note that for the steady-state thermal modeling, the capacitance matrix can be neglected and $p^{(q)} = f$. Simulating a problem with tunable design parameters (e.g., heat excitations, thermal conductivities, and air convection coefficients) requires repetitively solving Eqn. (51). Consequently, the computational cost is high particularly when the matrix K is large.

6.3 System-Level Thermal Modeling using DDM and MOR

To accelerate thermal simulation, MOR techniques can be utilized. However, since a 3D integrated system contains multiple dies in which many ports are required, the entire 3D system can contain hundreds of MOR ports. Therefore, directly applying MOR techniques to a 3D system can be computationally expensive. To improve the simulation efficiency, a new modeling method using combined domain decomposition and MOR is developed for both the steady-state and transient thermal analysis. The flow of the proposed system-level thermal modeling using domain decomposition and model order reduction without parameter variability is shown in Figure 62.

6.3.1 Problem Formulation

As shown in Figure 62, using the domain decomposition method presented in the last

section, a 3D system can be divided into domains, and the thermal capacitance and conductance matrices can be obtained. With defined MOR ports for each die, the following equation can be formed:

$$C\dot{x} = -Gx + Bu, \quad y = L^T x \quad (52)$$

where u represents the heat excitation including temperature and heat flow at MOR ports; B and L are matrices associated with the temperature and heat flow of MOR ports. In the proposed method that combines domain decomposition and MOR, three main steps are used after forming the system matrix:

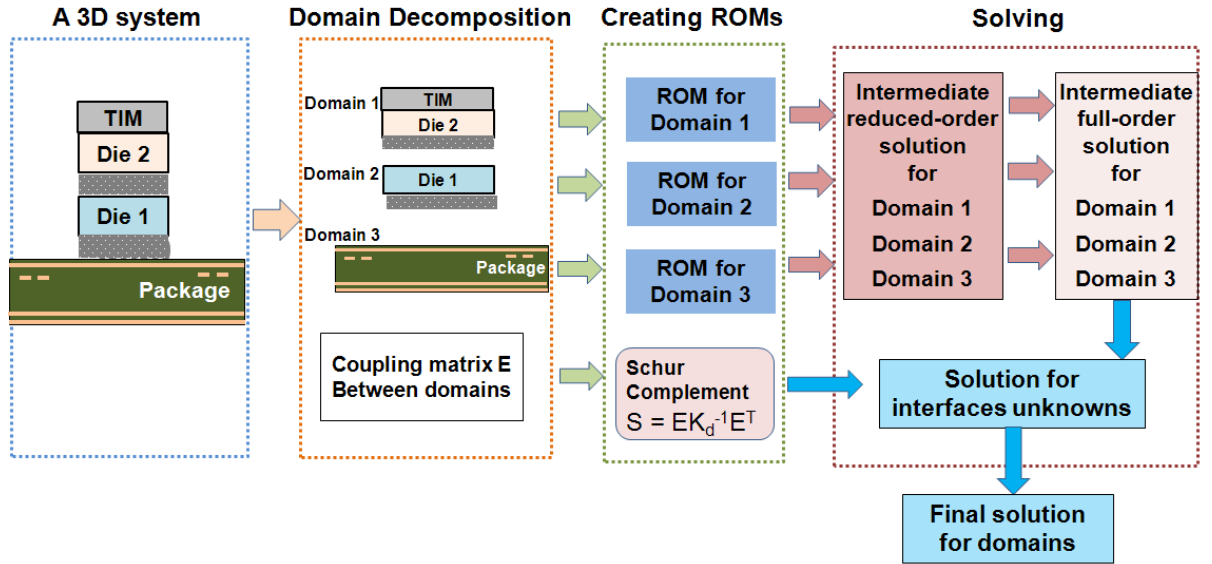


Figure 62. System-level thermal modeling flow using domain decomposition and model order reduction (without parameter variability).

Step 1: As the capacitance and conductance matrices are generated and MOR ports are defined for individual domains, by defining $x_d = \tilde{V}\tilde{x}_d$, the reduced-order model for each domain can be generated using MOR and expressed as

$$\tilde{C}_d \dot{\tilde{x}}_d = -\tilde{G}_d \tilde{x}_d + \tilde{B}\tilde{u} \quad (53)$$

where

$$\tilde{C}_d = \begin{bmatrix} \tilde{C}_1 & & & \\ & \tilde{C}_2 & & \\ & & \ddots & \\ & & & \tilde{C}_n \end{bmatrix}, \tilde{G}_d = \begin{bmatrix} \tilde{G}_1 & & & \\ & \tilde{G}_2 & & \\ & & \ddots & \\ & & & \tilde{G}_n \end{bmatrix}, \tilde{B} = \begin{bmatrix} \tilde{B}_1 \\ \tilde{B}_2 \\ \vdots \\ \tilde{B}_n \end{bmatrix}, \tilde{x}_d = \begin{bmatrix} \tilde{x}_1 \\ \tilde{x}_2 \\ \vdots \\ \tilde{x}_n \end{bmatrix}, V = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}$$

$$\text{and } \tilde{C}_i = V_i^T C_i V_i, \tilde{G}_i = V_i^T G_i V_i, \tilde{B}_i = V_i^T B_i, x_i = V_i \tilde{x}_i \quad (1 \leq i \leq n)$$

In the above equation, V_i , the congruence transformation matrix for the i -th domain, can be obtained using PRIMA [52]. \tilde{C}_i and \tilde{G}_i represent the reduced-order capacitance and conductance matrices for the i -th domain, respectively. As can be seen, the system reduced-order capacitance and conductance matrices \tilde{C}_d and \tilde{G}_d are block-diagonal matrices. It should be noted that if performing MOR for the entire system without domain decomposition, the reduced-order matrices \tilde{C}_d and \tilde{G}_d will be full dense matrices.

Step 2: The connectivity between reduced-order models is maintained via the unknowns at interfaces. As the reduced-order capacitance and conductance matrices do not contain the coupling information for domain interfaces, the unknowns for interfaces need to be calculated using

$$Sx_{inter} = EK_d^{-1}p_d^{(q)} \quad (54)$$

where $p_d^{(q)} = f_d + C/\Delta t \cdot x_d^{(q)}$ and $S = EK_d^{-1}E^T$ is the Schur complement [37]. Since K_d is a block-diagonal matrix, $K_d^{-1}E^T$ and $K_d^{-1}p_d^{(q)}$ can be efficiently obtained as

$$K_d^{-1}E^T = \begin{bmatrix} K_1 & & & \\ & K_2 & & \\ & & \ddots & \\ & & & K_n \end{bmatrix}^{-1} \begin{bmatrix} E_1^T \\ E_2^T \\ \vdots \\ E_n^T \end{bmatrix} = \begin{bmatrix} K_1^{-1}E_1^T \\ K_2^{-1}E_2^T \\ \vdots \\ K_n^{-1}E_n^T \end{bmatrix} \quad (55)$$

$$K_d^{-1}p_d^{(q)} = \begin{bmatrix} K_1 & & & \\ & K_2 & & \\ & & \ddots & \\ & & & K_n \end{bmatrix}^{-1} \begin{bmatrix} p_1^{(q)} \\ p_2^{(q)} \\ \vdots \\ p_n^{(q)} \end{bmatrix} = \begin{bmatrix} K_1^{-1}p_1^{(q)} \\ K_2^{-1}p_2^{(q)} \\ \vdots \\ K_n^{-1}p_n^{(q)} \end{bmatrix} \equiv \begin{bmatrix} \tilde{K}_1^{-1}\tilde{p}_1^{(q)} \\ \tilde{K}_2^{-1}\tilde{p}_2^{(q)} \\ \vdots \\ \tilde{K}_n^{-1}\tilde{p}_n^{(q)} \end{bmatrix} \quad (56)$$

where $K_i = C_i / \Delta t + G_i$ and $\tilde{K}_i = \tilde{C}_i / \Delta t + \tilde{G}_i$.

By constructing the interfacial basis functions based on the domain with coarse mesh grids, the dimension m of E matrix is small. As a result, the Schur complement matrix S can be computed efficiently using Eqn. (55). As the reduced-order thermal model for each domain is obtained in Step 1, $K_i^{-1}p_i^{(q)}$ ($i = 1, 2, \dots, n$) can be computed efficiently using the ROMs, as shown in Eqn. (56). As a result, the interface unknowns at time step $(q+1)$ in Eqn. (54) can be solved efficiently as

$$x_{inter} = S^{-1}EK_d^{-1}p_d^{(q)} = S^{-1}E \sum_{k=1}^n \tilde{K}_k^{-1}\tilde{p}_k^{(q)} \quad (57)$$

Step 3: Based on the obtained interfacial unknowns in Step 2, the temperature for domains can be obtained as

$$x_d = K_d^{-1}p_d^{(q)} - K_d^{-1}E^T x_{inter} \quad (58)$$

Since $K_d^{-1}E^T$ and $K_d^{-1}p_d^{(q)}$ are already calculated using Eqn. (55) and (56) in Step 2, the temperature for domains x_d can be calculated in a quick manner using vector subtraction.

6.3.2 Simulation with Parameter Variability

The creation of ROMs provides the capability of simulating a 3D system with varying

excitations (e.g., temperature and heat flow) at the defined MOR ports. However, simulating with varying parameters (e.g., material conductivities and heat transfer coefficients on boundaries) that are not associated with MOR ports, special consideration and treatment is required.

A. Simulation with Varying Conductivities

As various materials are remedies to optimize the thermal integrity of a 3D system, efficient thermal modeling with varying conductivities is required. To simulate with varying conductivities of TIMs and interposers, the TIM and interposer regions must be treated as separate domains using the domain decomposition method. For other domains with fixed thermal conductivities, since the stiffness matrices stay the same, no re-computation is required.

In steady-state analysis, the capacitance matrix can be ignored ($C_i = 0$), and $p_d = f_d$. As a result, $K_i = G_i$ and $\tilde{K}_i = \tilde{G}_i$. For the domain of TIM or interposer with a varying conductivity k_c , we assume that the initial conductivity is k_0 and the initial system conductance matrix is K_{i0} . First, $K_{i0}^{-1} E_i^T$ and $K_{i0}^{-1} p_i^{(q)}$ can be calculated once and stored. Since the domain conductance matrix K_{ic} scales proportionally with the varying conductivity k_c , the new matrix $K_{ic}^{-1} E_i^T$ and vector $K_{ic}^{-1} p_i^{(q)}$ can be efficiently calculated as

$$K_{ic}^{-1} E_i^T = \frac{k_0}{k_c} K_{i0}^{-1} E_i^T, \quad K_{ic}^{-1} p_i^{(q)} = \frac{k_0}{k_c} K_{i0}^{-1} p_i^{(q)} \quad (59)$$

As shown in Eqn. (59), the new matrix $K_{ic}^{-1} E_i^T$ and vector $K_{ic}^{-1} p_i^{(q)}$ can be calculated by multiplying the original matrix and vector with a scaling factor. Therefore, minimum

extra computational cost is added when simulating with a varying conductivity for steady-state analysis.

In transient analysis, the capacitance matrix C_i needs to be used. Initially, matrices C_{i0} and G_{i0} have been computed once and stored for the i -th domain with an initial conductivity k_0 . With a varied conductivity k_c , K_{ic} and \tilde{K}_{ic} can be computed easily using matrix additions:

$$K_{ic} = \frac{C_{i0}}{\Delta t} + \frac{k_0}{k_c} G_{i0}, \quad \tilde{K}_{ic} = \frac{\tilde{C}_{i0}}{\Delta t} + \frac{k_0}{k_c} \tilde{G}_{i0} \quad (60)$$

Then, $K_{ic}^{-1} E_i^T$ can be computed for the i -th domain. As the excitation term $p_i^{(q)}$ on the right-hand side of Eqn. (56) varies with time step q in transient analysis, $K_{ic}^{-1} p_i^{(q)}$ must be calculated at each time step, which is same for the transient analysis without varying conductivities.

B. Simulation with Varying Convection Coefficients

Real designs require thermal analysis with varying heat transfer coefficients on boundaries. To model an air convection boundary (Equation (9)) with varying convection coefficients, a boundary domain for air convection can be used. A package with a convection boundary at the bottom surface is shown in Figure 63. Using the aforementioned domain decomposition approach, this package can be divided into two separate domains: the domain of the package and the boundary domain with air convection (Figure 63). As shown in Figure 63, as the boundary domain contains a thin layer with the air convection boundary, the boundary domain can be meshed using only 2-layer mesh grids. As a result, the matrix K_i for the boundary domain is a small sparse

matrix with a narrow bandwidth. Therefore, $K_i^{-1}E_i^T$ and $K_i^{-1}p_i^{(q)}$ can be computed efficiently using a direct solver. The only overhead is the computation of $K_i^{-1}E_i^T$ for the neighboring domain because of the introduced interface coupling matrix E_i^T . Since E_i^T does not vary with the convection coefficient h_c , $K_i^{-1}E_i^T$ needs to be computed only once.

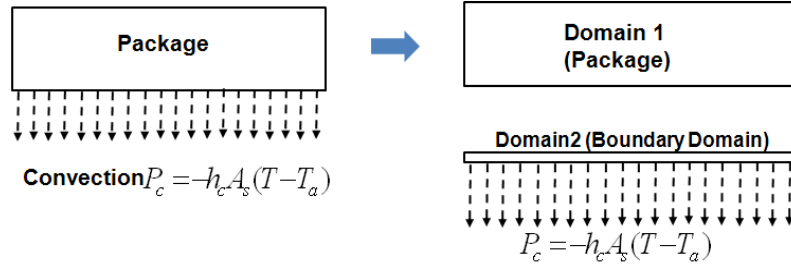


Figure 63. A boundary domain for air convection.

6.3.3 Simulation Flow

The pseudo-algorithm of the proposed system-level thermal modeling method using domain decomposition and MOR is shown in Figure 64. It is important to note that the proposed method can also be applied to steady-state thermal modeling with varying design parameters, as shown in Figure 64. For steady-state thermal modeling, the capacitance matrix is ignored and $p_d = f_d$.

6.3.4 Computational Cost and Complexity

The proposed method allows performing system-level thermal modeling for 3D systems using the divide-and-conquer approach, domain decomposition, and model order reduction. One promising property of the proposed approach is that it allows building ROMs for individual domains and then reconnecting them via the Schur complement. Assuming the system has a total number of n domains and each domain contains N_i

nodes and M_i ports, the total number of unknowns and ports are $N = \sum_{i=1}^n N_i$ and

$$M = \sum_{i=1}^n M_i, \text{ respectively.}$$

Algorithm:

1. Divide a 3D system into n separate domains, and obtain C, G, K, E, B matrices and excitation vectors f and u . Define MOR ports.
2. For each domain, compute the congruence transformation matrix V_i using PRIMA and obtain the reduced-order models \tilde{C}_i, \tilde{G}_i , and \tilde{B}_i :

$$\tilde{C}_i = V_i^T C_i V_i, \tilde{G}_i = V_i^T G_i V_i, \tilde{B}_i = V_i^T B_i, x_i = V_i \tilde{x}_i (i = 1, 2, \dots, n)$$

3. Compute $R = K_d^{-1} E^T$ based on Eqn. (55) and the Schur complement $S = EK_d^{-1} E^T = E \cdot R$
4. If the i -th domain contains varying conductivities, with an initial conductivity k_0 , calculate $K_{i0}^{-1} E_i^T$ and $K_{i0}^{-1} f_i$ for steady-state modeling using Eqn. (55) and (56), and compute K_{i0} and \tilde{K}_{i0} for transient analysis.
5. If (steady-state simulation), then
 - (a) Compute $e = K_d^{-1} f_d$ using the ROMs in Step 2
 - (b) Compute interface unknowns using $x_{inter} = S^{-1} EK_d^{-1} p_d = S^{-1} E \cdot e$
 - (c) Compute domain temperature using $x_d = e - Rx_{inter}$
6. Else if (transient simulation), perform transient simulation for n_t steps with initial system temperature and time step Δt .

First, compute K_{ic} and \tilde{K}_{ic} using Eqn. (60) and $K_{ic}^{-1} E_i^T$ with conductivity of k_c .

Then, for $q = 2$ to n_t

- (a) Map domain temperature x_d to \tilde{x}_d using matrix V
- (b) Compute $e = K_d^{-1} p_d^{(q)}$ using the ROMs in Step 2
- (c) Compute the interface unknowns using $x_{inter} = S^{-1} EK_d^{-1} p_d^{(q)} = S^{-1} E \cdot e$
- (d) Compute domain temperature using $x_d = e - Rx_{inter}$

End

Figure 64. Pseudo-algorithm for system-level steady-state and transient thermal modeling using domain decomposition and MOR.

If directly applying MOR to the entire system represented by Eqn. (52), because the system matrix has a large dimension and M ports, the total computational cost is much higher than the computational cost of performing MOR for n sub-domains particularly when N and M are large. Assuming the system matrix is a large $N \times N$ matrix, directly performing MOR with M ports and matching up to q moments requires an estimated computational cost of $O(qMN \log(N))$ using an iterative solver [37]. However, by building ROMs for n individual domains, the total computational cost is of $\sum_{i=1}^n O(qM_i N_i \log(N_i))$ using an iterative solver. In addition, since the number of unknown N_i for an individual domain is reduced and is much smaller than N , direct solving methods can be applied. Therefore, the computational cost can be reduced dramatically, compared to the cost of direct MOR on the entire structure.

Compared to the computational cost of performing MOR for n sub-domains, the computing of the Schur complement is not the dominant cost. Although the computing of the Schur complement $S = EK_d^{-1}E^T$ requires additional cost using Eqn. (55), since the matrix E is usually constructed based on a coarser-side interface grids, the dimension of E is small; thus, S can be computed efficiently.

Another promising property of the proposed approach is that it allows modeling a 3D system with varying design parameters such as thermal conductivities and convection coefficients without using parameterized MOR techniques. In the simulation algorithm (Figure 64), as the matrix operation for each domain is treated independently, the new system matrix with a varying conductivity in one domain can be obtained efficiently by multiplying a scaling factor using Eqn. (59) for steady-state analysis. For transient

analysis, with a varying conductivity k_c , $K_{ic}^{-1}E_i^T$ needs to be computed for the i -th domain. The variation of air convection can be captured using the introduced boundary domain without performing parameterized MOR. Therefore, minimum extra computational cost is added when modeling with varying parameters.

6.3.5 Implementation

For modeling a 3D problem using the proposed method, to reduce the total number of mesh cell/unknowns, each domain is meshed independently using non-uniform rectangular meshing grids. The capacitance matrix C , conductance matrix G , and coupling matrix E are extracted using the finite element method. The inhomogeneous material stack-up can also be handled using the cell-based finite element formulation, as discussed in Chapter 4.

The reduced-order model for each domain and $R = K_d^{-1}E^T$ are only computed once and stored. For domains that do not contain MOR ports, the original stiffness matrix is used to compute $K_i^{-1}p_i^{(q)}$ in Eqn. (56). It is important to note that the proposed method has high parallelizability because of independent operations for each domain. For the proposed algorithm shown in Figure 64, the operations in each step can be parallelized. The proposed method has been implemented using Matlab and executed on a PC with a 3.2 GHz CPU and 3.0 GB memory. The simulation is executed without using parallelization for the test cases shown in the next section.

6.4 Numerical Test Cases

6.4.1 A Model-Verification Example

To verify the correctness and accuracy of the proposed method, a model-verification example is simulated first. The stack-up is shown in Figure 65. In this example, all the layers have the same lateral dimensions. Equivalent thermal conductivities are used for all the layers. A uniform power consumption of 50 W/cm^2 is used for the die. An air convection boundary is used on the bottom surface of this stack-up to represent the downward heat transfer from the die to the package. This example contains one inner-layer that has a varying thermal conductivity, as shown in Figure 65.

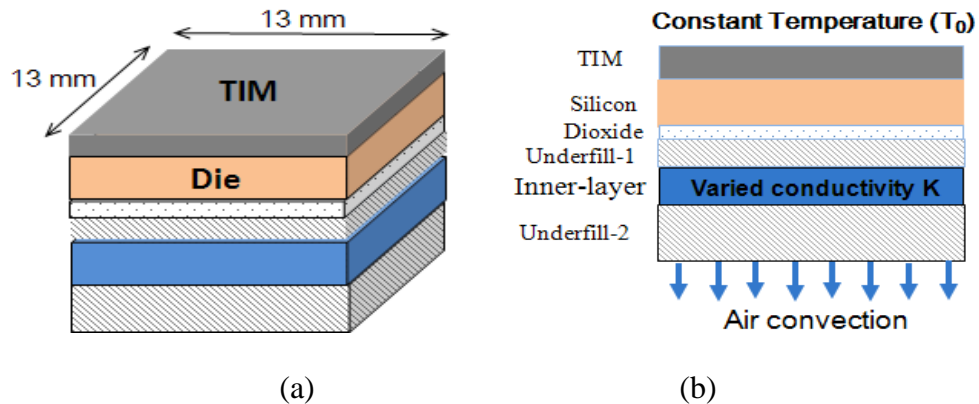


Figure 65. A model-verification example: (a) 3D view and (b) 2D layer stack-up.

The material thicknesses and thermal conductivities are shown in Table 12. As this example comprises layers with a regular shape, a uniform heat source, and a homogeneous conductivity for each layer, an analytical solution can be obtained using the method of equivalent thermal resistance. For comparison purposes, this example is also simulated using the detailed thermal model and the proposed method. In the simulation, various thermal conductivities of the inner-layer and air convection coefficients on the bottom surface are used. Note that the inner-layer can represent a

passive die, an interposer layer, or an under-fill layer in a real design. This example is divided into four domains. The first domain includes the TIM, Die, and underfill-1. The second domain includes the inner-layer, which has a varied conductivity. The third domain contains the layer of underfill-2 while the fourth domain contains the boundary domain with air convection on the bottom surface. The top surface of the TIM is set to 25 Celsius to represent the heat sink.

Table 12. Material thicknesses and thermal conductivities.

Layer	Thickness (mm)	Thermal conductivity (W/(m-K))
TIM	0.15	1.0
Die silicon substrate	0.2	110
Die silicon oxide (total)	0.02	1.4
Underfill-1	0.05	5
Inter-layer	0.10	k
Underfill-2	0.3	2

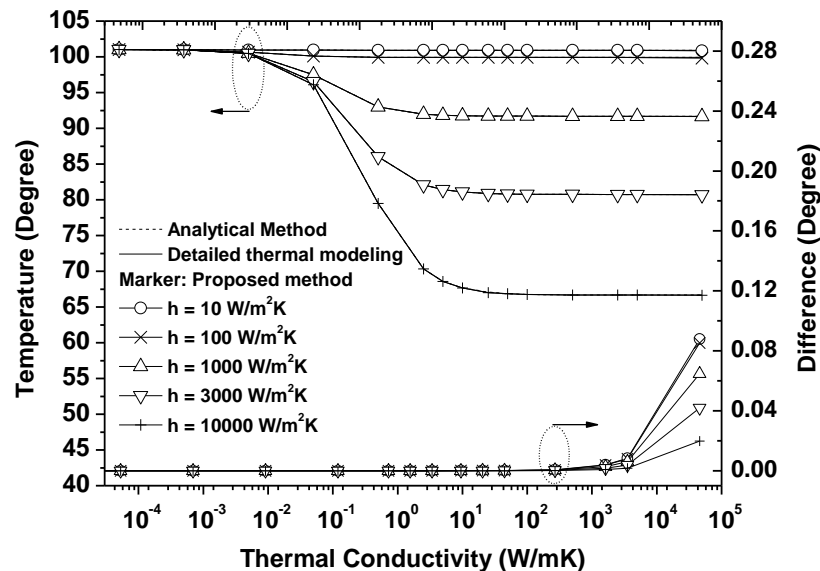


Figure 66. Temperatures of the active layer of die with various thermal conductivities and air convection coefficients.

The simulated temperatures of the die with various thermal conductivities of the inner layer and air convection coefficients are shown in Figure 66. As shown in Figure 66, with the conductivity of the inner-layer varying in the wide range of $5e-4$ to $5e+4$ W/mK and the air convection varying from 10 to $1e+5$ $W/(m^2K)$, the results from the proposed method agree well with results using the finite element-based DDM and analytical method, which validates the accuracy of the proposed method. The temperature difference between the results from the proposed method and the detailed thermal modeling is also shown in Figure 66. The maximum temperature difference is about 0.09 degree. Figure 66 shows that with an extremely low thermal conductivity of the inner-layer, all the heat transfers to the heat sink. Therefore, the die temperature is maintained constant even with high convection at the bottom surface. With a thermal conductivity beyond 0.1 W/mK , the chip temperature decreases with increasing air convection coefficient at the bottom surface.

6.4.2 A 3D Stacked Chip Example

A 3D stacked chip including three dies is shown in Figure 67a. The power consumptions of Die 1, Die 2, and Die 3 are 20, 15, and 12 W, respectively. This test case is divided into four domains, as shown in Figure 67b. The top surface of TIM layer is set to 25 Celsius to represent the effect of heat sink. An air convection boundary with a heat transfer coefficient of 300 W/m^2K is applied at the bottom of Die 1 to represent the effect of air convection on the package and PCB. The initial temperature of this example is set to 25 Celsius. In this example, 81, 81, 81, and 1 MOR ports are used for Domain 1, Domain 2, Domain 3, and Domain 4, respectively. Thus, the total number of MOR ports is 244. In this example, the selected order of the ROMs for domains is 4, and the total

number of unknowns for the 4 domains is 104 K. 9 x 9 meshing grids are used for each domain interface. The layer dimensions and thermal conductivities are shown in Table 13. We first perform MOR using the proposed method with domain decomposition. The simulation times with various problem sizes are shown in Table 14. For comparison purposes, the computational time of performing MOR for the entire system without domain decomposition is also shown in Table 14. Note that a direct solver is used for both cases. Table 14 shows that using the proposed method, the MOR time is greatly reduced, compared to that of performing MOR for the entire system. For the problem with 104 K unknowns, performing MOR for the entire system cannot be completed because of limited memory while the proposed method takes 169.8 seconds. The reduction in the computational time is because using the proposed method, the size of the stiffness matrix and the number of MOR ports are both reduced for each domain, as discussed in Section 6.3.4.

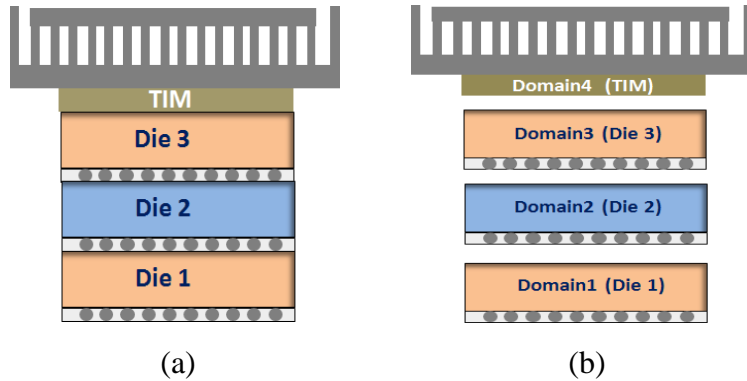


Figure 67. (a) A 3D stacked chip, and (b) its domain decomposition.

Table 13. Material dimensions and thermal conductivities for the examples of 3D stacked chip and 3D integrated system.

Example of 3D Stacked Chip		
Layer	Size (length x width x thickness) (mm)	Thermal conductivity (W/(m-K))
Die 1, Die 2 and Die 3	10 x 10 x 0.2	110
TIM layer	10 x 10 x 0.2	1.4
Microbump layer	10 x 10 x 0.1	5
Example of 3D Integrated System		
Die 1, Die2	10 x 10 x 0.2	110
TIM layer	10 x 10 x 0.2	2.0
Silicon interposer	30 x 30 x 0.3	110
Package	60 x 60 x 1.3	5
Microbump layer	10 x 10 x 0.1	5

Table 14. Comparison of simulation times using the proposed method and the method of performing MOR for the entire system

	Simulation Time (s) for Various Problem Sizes		
	26.2 K	52.1 K	104.0 K
Proposed method	40.9 s	81.6 s	169.8 s
MOR for entire system	184.7 s	371.7 s	/

With 104 K unknowns, the generation of ROMs for four domains takes about 169.8 s, and the computation of the Schur complement takes about 22 s. With a time step of 0.01 s, the simulated transient temperatures of Die 1, Die 2, and Die 3 are shown in Figure 68. Compared to the results obtained using the detailed thermal model with the DDM, the maximum temperature difference is about 0.22 degree. Thus, the error is less than 0.3%. The temperature error comes from the reduced-order models used in the proposed method. For simulating 200 time steps, the comparison of simulation times using the proposed method and the detailed thermal model using the DDM is shown in Table 15. As shown in Table 15, compared to the simulation time using the DDM, a simulation time speed up of 15.7x is obtained for the transient analysis using the proposed method. If considering

the time for generating ROMs and the computation of the Schur complement, the speed-up is about 3.4x for simulating 200 steps. With an increased number of time steps, the speed-up can reach closely to 15x.

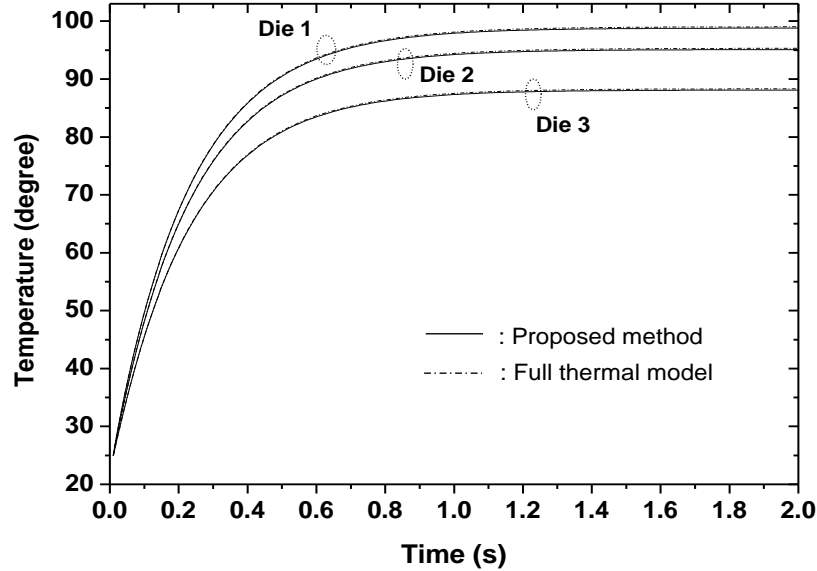


Figure 68. Transient temperatures of Die 1, Die 2, and Die 3 with TIM thermal conductivity of 1.4 W/(m-K).

As the layer of TIM is treated as a separate domain, the temperature of dies with various TIM conductivities can be simulated efficiently. As an example, the steady-state temperature of Die 1, Die 2, and Die 3 with a varying TIM thermal conductivity in the range of 0.5 to 3 W/mK is shown in Figure 69. Compared to the results using the DDM, the maximum temperature difference is 0.02 degree. The time for simulating 400 samples is shown in Table 15. Table 15 shows the proposed method achieves a CPU time speed up of 20.7x, compared to that using the domain decomposition approach.

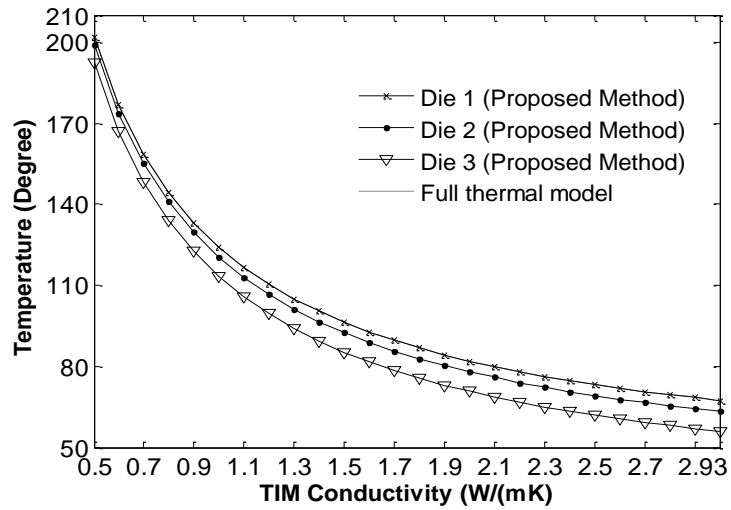


Figure 69. Temperatures of Die 1, Die 2, and Die 3 with a varying TIM conductivity.

Table 15. Comparison of simulation times using the proposed method and the method using detailed thermal model.

		Total Mesh Cells	Detailed Model using DDM (s)	Proposed Method (s)	Time Speed-up
3D IC example	Transient	104 K	806.6	50.7	x15.7
	Steady state	104 K	1600.4	77.4	x20.7
3D system	Transient	79 K	1365.2	110.8	x12.3
	Steady state	79 K	682.6	42.0	x16.2
2.5D example	Steady state	244.4K	2921.3	98.1	x29.8

6.4.3 A 3D Integrated System Example

A 3D integrated system including two stacked dies, a silicon interposer, and a package is shown in Figure 70a. The constant power consumption of Die 1 is 12 W. The transient power consumption of Die 2 is shown in Figure 70b. This example is divided into six domains including the domains for TIM, Die 1, Die 2, interposer, package, and boundary domain for air convection, respectively. In this test case, the domains of Die1, Die2, and TIM contain 81, 81, and 1 MOR ports, respectively. Thus, a total of 163 ports are used.

The layer dimensions and thermal conductivities are shown in Table 13. Note that an average thermal conductivity is used for underfill/microbump layers. The initial system temperature is 25 Celsius. The total number of unknowns for domain 1, 2, 3, 4, 5, and 6 are 11 K, 31 K, 31 K, 2K, 5 K, and 0.2 K, respectively.

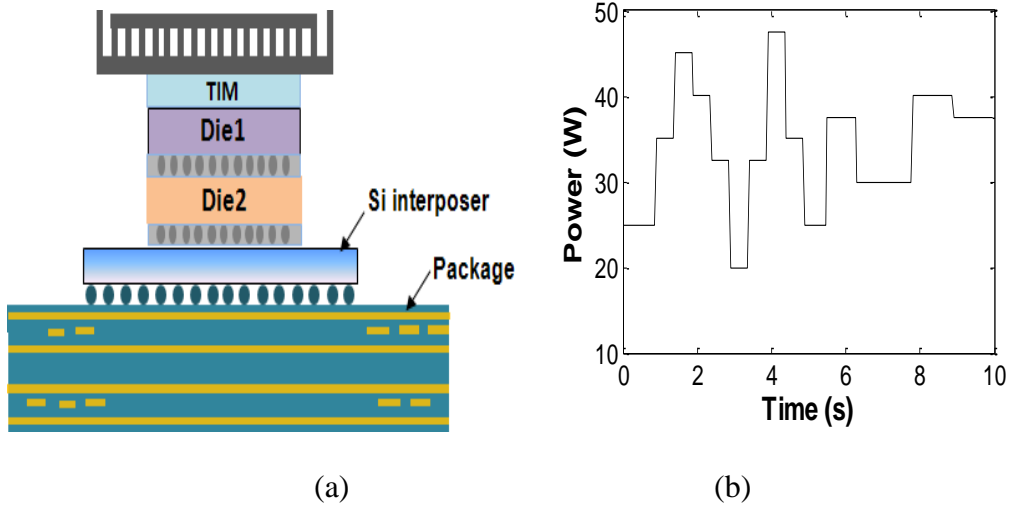


Figure 70. (a) A 3D integrated system with an interposer and a package, (b) transient power of Die 2.

Using the proposed method, the simulated transient temperature of dies with a time step of 25 ms is shown in Figure 71. Compared to the simulation results from the detailed thermal model using the DDM, the maximum temperature difference is less than 0.1 Celsius, which validates the accuracy of the proposed method. The comparison of simulation times for 400 time steps using the proposed method and the method using the DDM is shown in Table 15. Compared to the simulation time using the DDM, the proposed method achieves a simulation time speed up of 12.3x for the transient analysis. In this test case, the selected order of the ROMs for domains containing MOR ports is 5. The generation of ROMs for domains takes about 161.9 s, and the computation of the

Schur complement takes about 23.7 s. If considering the time for generating ROMs and computing the Schur complement, the speed-up is about 4.6x.

To demonstrate the capability of simulating with varying air convection, the steady-state simulation with a varying air convection coefficient in the range of 10 to 5000 $W/(m^2K)$ is also carried out. The simulated temperature of dies is shown in Figure 72. Figure 72 shows that good agreement is obtained between the proposed method and the detailed thermal model using the DDM. As shown in Figure 72, the temperatures of Die 1 and Die 2 decrease with increasing air convection on the package. The comparison of CPU times for steady-state simulation of 200 points is also shown in Table 15. Table 15 shows that the time speed-up is about 16.2x, compared to the thermal modeling using the DDM.

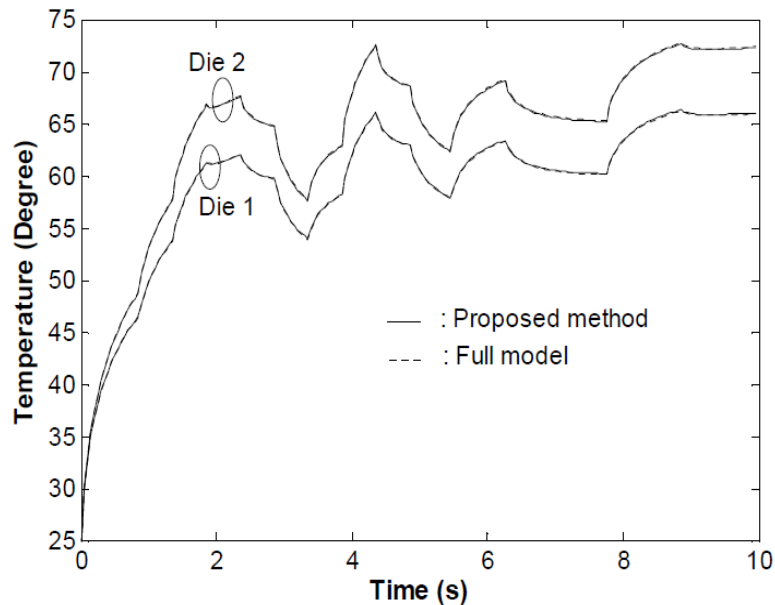


Figure 71. Transient temperature of dies with the TIM conductivity of 2 W/mK and an air convection coefficient of 10 W/m^2K on package.

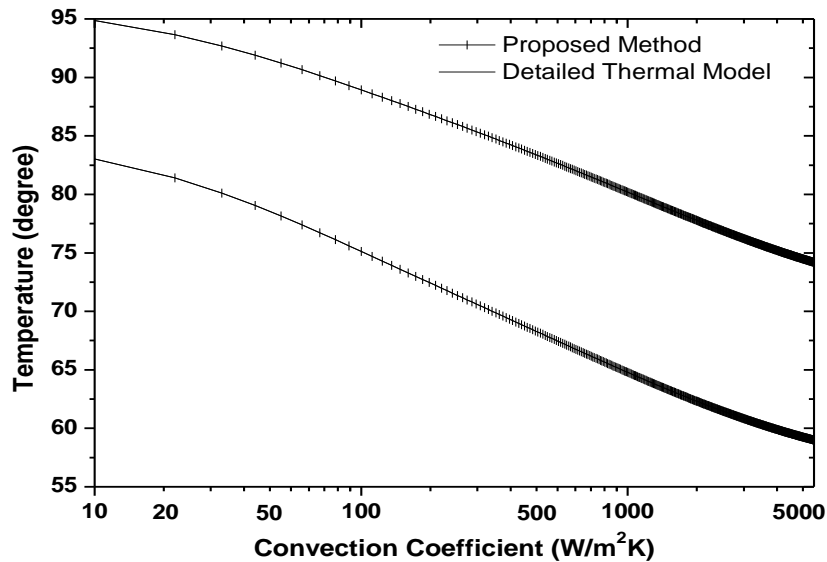


Figure 72. Transient temperature of dies with a varying convection coefficient on package. (The power consumption of Die 2 is set to 50 W.)

6.4.4 A 2.5D Integration Example

A 2.5D integration example is shown in Figure 73. The size of all four dies is 13 x 13 mm², and the size of the interposer is 31 x 31 mm². The package size is 48 x 48 mm². The material thicknesses and thermal conductivities are summarized in Table 16. Note that an average thermal conductivity is used for underfill/microbump layers. An air convection coefficient of 1000 W/m²K is applied to the bottom surface of the package to represent the convection effect on the PCB. In this example, equivalent thermal conductivities are used for both microbump/underfill and bump/underfill layers. The top surface of the TIM is set to 25 Celsius to represent the heat sink. The power consumptions of Die 1, Die 2, Die 3, and Die 4 are 33.8 W, 50.7 W, 59.15 W, and 67.6 W, respectively. This example is divided into seven domains: four domains for dies, one domain for the interposer, one domain for the underfill layer of the interposer, and one domain for the package. In this example, each die contains 154 MOR ports. Therefore, a total of 616 ports are used. Each

die is meshed using 48.9 K meshing cells. The interposer, underfill, and package use 3.4 K, 15.6 K, and 29 K meshing cells, respectively. In this example, the selected order of the ROMs for domains with MOR ports is 4. The generation of ROMs for domains takes about 814.1 s, and the computation of the Schur complement takes about 133.4 s.

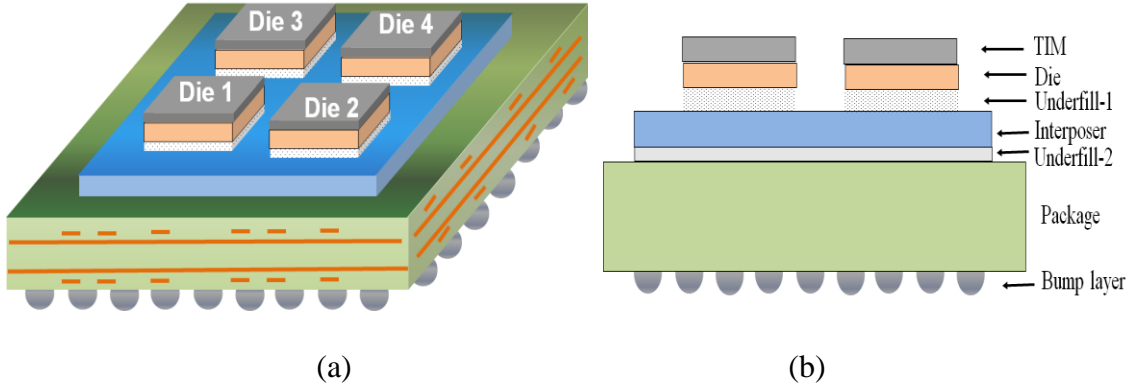


Figure 73. A 2.5D integration example: (a) whole system, (b) cross-sectional view.

Table 16. Material dimensions and thermal conductivities.

Layer	Size (length x width x thickness) (mm)	Thermal conductivity (W/(m-K))
Die 1, 2, 3 and 4	13 x 13 x 0.25	110
TIM	13 x 13 x 0.15	0.8
Underfill-1/microbump	13 x 13 x 0.05	5
Interposer	31 x 31 x 0.10	110
Underfill-2/microbump	31 x 31 x 0.15	5
Package	48 x 48 x 1.47	5
TIM layer	10 x 10 x 0.2	1.4
Bump layer	48 x 48 x 0.3	5

To investigate the effect of the thermal conductivity of interposer on die temperature, this example is simulated with an interposer conductivity over a large range ($k = 5e-4$ to $5e+4$ W/mK). The simulated temperatures of dies using the proposed method and the detailed thermal modeling via the DDM are shown in Figure 74. For comparison purposes, the temperature difference is also shown in Figure 74. With the conductivity

varying from $5e-4$ to $5e+4$ W/mK, the maximum temperature difference is about 0.04 degrees, indicating the accuracy of the simulation. With an extremely low thermal conductivity of interposer, all the power/heat dissipates through the heat sink. With a gradually increased thermal conductivity of interposer from $5e-3$ to 100 W/mK, the temperatures of Die 1, Die 2, Die 3, and Die 4 decrease. However, when the conductivity increases from 100 to $5e+4$ W/mK, the temperature of Die 1 increases. The increasing temperature of Die 1 is because the power consumption of Die 1 is much lower than that of other dies. As a result, the thermal coupling between Die 1 and other dies increases the temperature of Die 1. The simulation times using the proposed method and the detailed thermal modeling are shown in Table 15. Assuming simulating 200 samples of thermal conductivities, the detailed thermal modeling using the DDM requires 2921.3 seconds while the proposed method use only 98.1 seconds. Therefore, a speed-up of 29.8x is achieved.

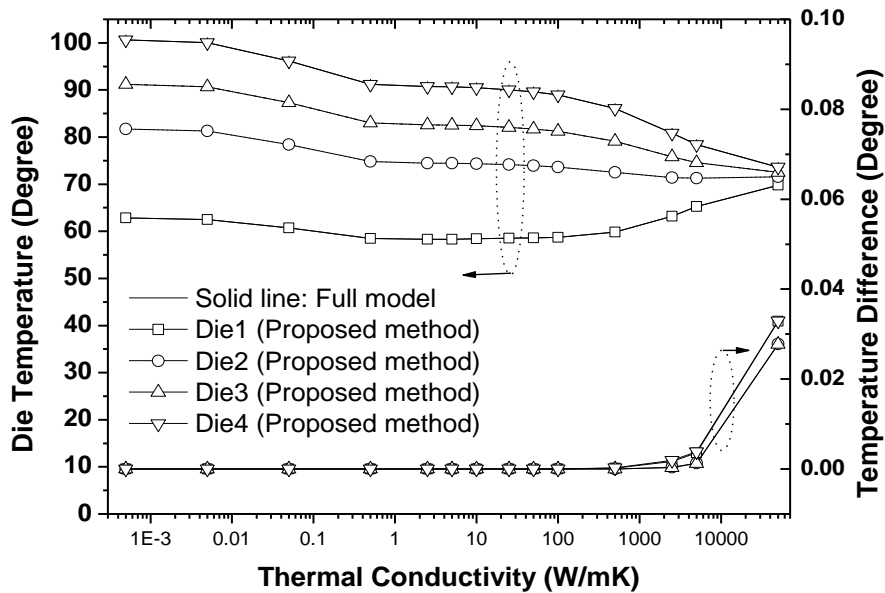


Figure 74. Temperatures of dies and temperature differences with a varying conductivity of interposer.

6.5 Summary

In this chapter, the system-level thermal modeling method using non-conformal domain decomposition and model order reduction is presented for both the steady-state and transient analysis of 3D systems. This thermal modeling approach allows building reduced-order models for separated domains and reconnecting them via the Schur complement. As each domain is treated independently, the proposed method can efficiently handle varying design parameters (e.g., TIM/interposer thermal conductivities and air convection coefficients) without performing parameterized MOR. The modeling process and computational complexity are discussed in detail. The accuracy and simulation efficiency of the approach have been validated against the simulation using the detailed thermal modeling and analytical method. Based on the simulation results, the proposed method shows a maximum temperature error of 0.3%. Because of the combined DDM and MOR approaches, the proposed method can achieve a simulation time speed up of 29x, compared to the thermal modeling using domain decomposition.

CHAPTER 7

FUTURE WORK: EXTENSION TO ELECTROMAGNETIC MODELING USING FINITE-DIFFERENCE NON-CONFORMAL DOMAIN DECOMPOSITION

7.1 Introduction

As material properties such as electrical conductivity and dielectric loss are temperature dependent, a non-uniform temperature distribution can affect the propagation of electromagnetic fields. On the other hand, electromagnetic waves/pulses such as electrostatic discharge pulses propagating on interconnects can result in temperature increases, necessitating coupled thermal-electromagnetics simulation. Facilitating thermal-electromagnetic simulation requires efficient electromagnetic modeling of structures with multiple scales. The aforementioned non-conformal domain decomposition method can also be extended to frequency-domain electromagnetic modeling. Several finite element-based non-conformal domain decomposition techniques have been proposed for eddy-current calculation in [38] and electromagnetic simulations in [39, 40]. A finite-difference domain decomposition approach using characteristic basis functions has been proposed for electrostatic problems [49]. However, the non-conformal domain decomposition technique has not been established in the open literature based on the finite-difference formulation for frequency-domain electromagnetic modeling to the best of our knowledge.

This chapter focuses on two-dimensional electromagnetic modeling using the finite-difference non-conformal domain decomposition, leaving 3D electromagnetic modeling using finite-difference non-conformal domain decomposition as the future work. A finite-

difference non-conformal domain decomposition method is developed for solving 2D electromagnetic problems. The proposed approach allows the formulation of individual domains using the finite difference method with non-matching meshing grids at interfaces. The continuity between domains is maintained by introducing Lagrange multipliers and basis functions at interfaces for the finite-difference formulation. The correctness and accuracy of the proposed method has been validated using a numerical example.

7.2 2D Electromagnetic Modeling using Finite-Difference DDM

7.2.1 Formulation

For a 2D transverse magnetic (TM) electromagnetic problem in a homogeneous medium, the governing equation in frequency domain can be expressed as [45]

$$\begin{aligned}
 j\omega\varepsilon E_z &= \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} - J_z \\
 H_x &= -\frac{1}{j\omega\mu} \frac{\partial E_z}{\partial y} \\
 H_y &= \frac{1}{j\omega\mu} \frac{\partial E_z}{\partial x}
 \end{aligned} \tag{61}$$

where E_z , H_x , and H_y represent the electric (E) and magnetic (H) fields in the z , x , and y directions, respectively; ε and μ represent permittivity and permeability, and ω is the angular frequency; J_z represents the excitation current source in the z direction. By substituting the expression of H_x and H_y into the first equation in Equation (61), the following equation can be derived:

$$\nabla_t^2 E_z + k^2 E_z = j\omega\mu J_z \tag{62}$$

where k is the wavenumber and $k^2 = \omega^2 \mu\varepsilon$. Eqn. (62) can be used to approximate the wave propagation in a parallel plane structure (e.g., PCBs and packages). The losses in

conductors and dielectrics can also be modeled using the finite difference method [46, 47].

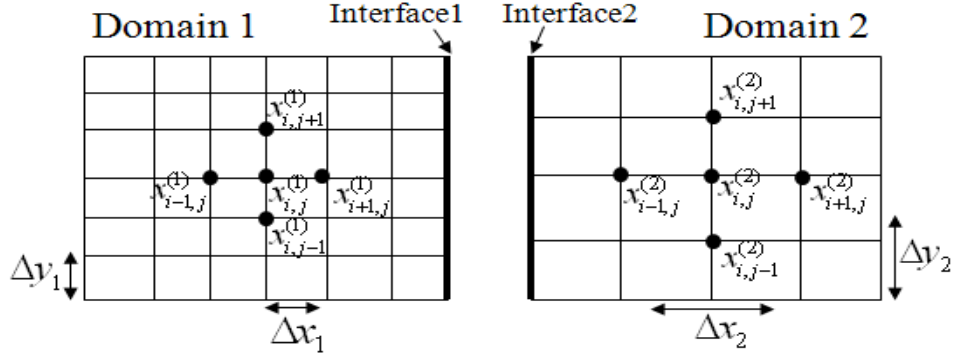


Figure 75. Domain decomposition of a 2D electromagnetic problem.

Using the non-conformal domain decomposition and rectangular meshing grids, a 2D EM problem can be divided into sub-domains. For simplicity, we assume that the problem has a rectangular shape and is divided into two domains with different grid sizes and non-matching grids at interfaces, as shown in Figure 75. Because of the domain decomposition, unknown current densities need to be assigned at interfaces. By introducing the Lagrange multiplier $\lambda^{(k)} = j\omega\mu J_z|_{\Gamma_{inter_k}}$ ($k = 1, 2$), the following equations can be derived for Domain 1 and Domain 2 based on the finite-difference formulation:

$$\frac{x_{i-1,j}^{(1)} + x_{i+1,j}^{(1)} - 2x_{i,j}^{(1)}}{(\Delta x_1)^2} + \frac{x_{i,j-1}^{(1)} + x_{i,j+1}^{(1)} - 2x_{i,j}^{(1)}}{(\Delta y_1)^2} + k^2 x_{i,j}^{(1)} - \lambda_{(i,j)}^{(1)} = 0 \quad (63a)$$

$$\frac{x_{i-1,j}^{(2)} + x_{i+1,j}^{(2)} - 2x_{i,j}^{(2)}}{(\Delta x_2)^2} + \frac{x_{i,j-1}^{(2)} + x_{i,j+1}^{(2)} - 2x_{i,j}^{(2)}}{(\Delta y_2)^2} + k^2 x_{i,j}^{(2)} - \lambda_{(i,j)}^{(2)} = 0 \quad (63b)$$

where $x_{i,j}^{(k)}$ is the electric field at point (i, j) in domain k .

As the pointwise E fields are used in Eqn. 63a and 63b, directly maintaining the continuity of E fields at interfaces becomes challenging for the FDM. Here, we introduce an extra integral equation to maintain the continuity of the E field at interfaces as in the Mortar method [41, 83]:

$$\int_{\Gamma_{inter}} (\tilde{E}^{(1)} - \tilde{E}^{(2)}) \varphi dl = 0 \quad (64)$$

where $\tilde{E}^{(k)}$ is the assumed continuous E field in domain k and φ is a basis function at the interface. Because of the pointwise finite-difference formulation of Eqn. 63a and 63b, continuous representations of φ and the E field are required to compute the integral in Eqn. (64). In this paper, we assume $\varphi_i|_{\Gamma_{inter}} = 1$ ($(i-1)\Delta y \leq y \leq i \cdot \Delta y$) is a piecewise constant basis function, as shown in Figure 76a and

$$\lambda = \sum_{i=1}^{n-1} b_i \varphi_i \quad (65)$$

The basis function φ_i is usually constructed based on a domain with coarse meshing grids to reduce the number of unknowns on interfaces.

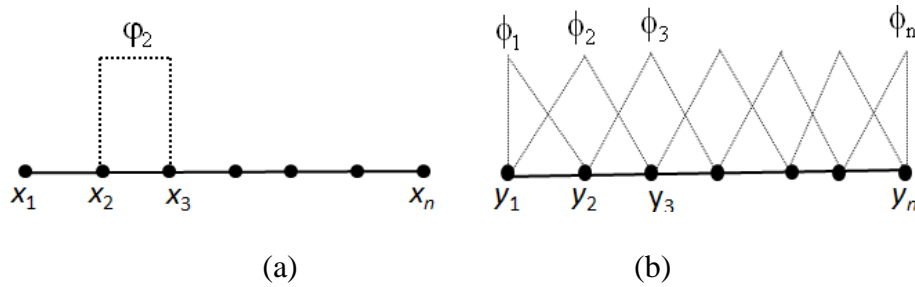


Figure 76. (a) A piecewise constant basis function for the Lagrange multiplier, (b) piecewise linear basis functions for E fields at interfaces.

For the E field in Eqn. 64, we assume

$$\tilde{E}_{i,j}^{(k)} = x_{i,j}^{(k)} \phi_{i,j} \quad (66)$$

where $\phi_{i,j} = \begin{cases} 1 & \text{at point } (i, j) \\ 0 & \text{at other points} \end{cases}$ is the basis function for the E field at point (i, j) . As a result,

the E field at interfaces can be expressed as a linear combination of piecewise linear basis functions, as shown in Figure 76b.

Based on the conservation of currents at the interface, we assume $\lambda = -\lambda^{(1)}\big|_{\Gamma_{inter}} = \lambda^{(2)}\big|_{\Gamma_{inter}}$. By multiplying $\phi_{i,j}$ on both sides of Eqn. 63a and 63b and integrating over the volume, after some mathematical manipulations, the following equations can be obtained:

$$\frac{x_{i-1,j}^{(1)} + x_{i+1,j}^{(1)} - 2x_{i,j}^{(1)}}{(\Delta x_1)^2} + \frac{x_{i,j-1}^{(1)} + x_{i,j+1}^{(1)} - 2x_{i,j}^{(1)}}{(\Delta y_1)^2} + k^2 x_{i,j}^{(1)} + \frac{1}{\Delta x_1 \Delta y_1} \int_{\Gamma_{inter}} b_i \varphi_i \phi_j = 0 \quad (67a)$$

$$\frac{x_{i-1,j}^{(2)} + x_{i+1,j}^{(2)} - 2x_{i,j}^{(2)}}{(\Delta x_2)^2} + \frac{x_{i,j-1}^{(2)} + x_{i,j+1}^{(2)} - 2x_{i,j}^{(2)}}{(\Delta y_2)^2} + k^2 x_{i,j}^{(2)} + \frac{1}{\Delta x_2 \Delta y_2} \int_{\Gamma_{inter}} b_i \varphi_i \phi_j = 0 \quad (67b)$$

With basis functions at interfaces and the Lagrange multiplier, ϕ_j and φ_i , we can derive the following equation from Eqn. 64, 67a, and 67b for the 2D problem with two domains (Figure 75):

$$\begin{bmatrix} K_1 & & \\ & K_2 & \\ B_1 & -B_2 & 0 \end{bmatrix} \begin{bmatrix} x^{(1)} \\ x^{(2)} \\ b \end{bmatrix} = \begin{bmatrix} e^{(1)} \\ e^{(2)} \\ 0 \end{bmatrix} \quad (68)$$

where $\alpha_1 = 1/(\Delta x_1 \cdot \Delta y_1)$ and $\alpha_2 = 1/(\Delta x_2 \cdot \Delta y_2)$ are scaling factors because of the finite-difference approximation; K_1 and K_2 are finite-difference stiffness matrices for Domain 1 and 2 derived based on the first three terms on the left-hand side of Eqn. 63a and 63b, respectively [46]. In Eqn. 68, $e^{(1)}$ and $e^{(2)}$ are excitation vectors associated with port excitations in Domain 1 and 2, respectively. The entries of the B matrix can be expressed as

$$B_{(k)i,j} = \int_{\Gamma_{inter}} \phi_i^{(k)} \cdot \phi_j dl \quad (k=1, 2) \quad (69)$$

Assuming a problem with n subdomains, the generalized matrix equation can be obtained as

$$\begin{bmatrix} K_1 & & & & \alpha_1 B_1^T \\ & K_2 & & & \alpha_2 B_2^T \\ & & \ddots & & \vdots \\ & & & K_n & \alpha_n B_n^T \\ B_1 & B_2 & \cdots & B_n & b \end{bmatrix} \begin{bmatrix} x^{(1)} \\ x^{(2)} \\ \vdots \\ x^{(n)} \\ b \end{bmatrix} = \begin{bmatrix} e^{(1)} \\ e^{(2)} \\ \vdots \\ e^{(n)} \\ 0 \end{bmatrix} \quad (70)$$

Note that the above formulation is derived by assuming uniform meshing grids along x and y directions in each domain. With non-uniform meshing grids in the x and y directions, a similar formulation can be developed following the proposed formulation steps. The only difference is that with non-uniform mesh grids, the matrix K_i ($i = 1, 2, \dots, n$) derived using the finite difference method needs to be multiplied by a diagonal matrix in which the matrix diagonal entries depends on the meshing size at each grid point.

7.2.2 Examples and Discussion

To verify the correctness of the proposed method, a rectangular plane pair structure is simulated. The parallel plane structure is shown in Figure 77. A rectangular structure is selected because the resonant frequencies of the structure can be computed analytically using the formula:

$$f(m, n) = \frac{1}{2\pi\sqrt{\mu\varepsilon}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (71)$$

where a and b are the length and width of the structure. The thicknesses of the dielectric layer and copper plane are $350 \mu m$ and $30 \mu m$, respectively. The dielectric constant is 4, and the copper conductivity is $5.8e+7 S/m$. This structure is divided into two domains as

shown in Figure 77. In the center of each domain, one port is assigned. The losses because of the finite conductivity of the copper plane and skin effect are also included using the method in [46].

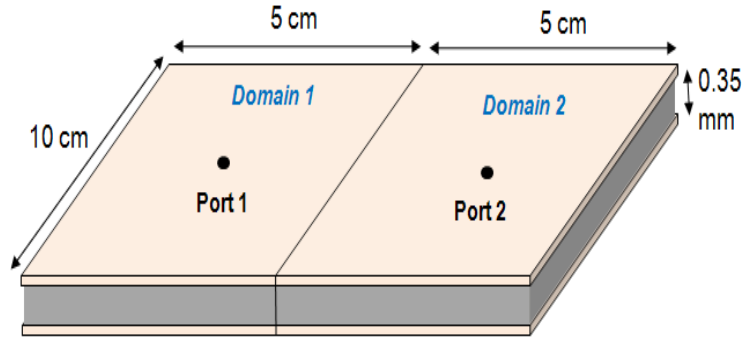


Figure 77. A parallel plane structure.

This structure is simulated using the proposed method with non-matching meshing grids at the interface. With various mesh sizes in each domain, the simulated 2-port S parameters in the frequency ranges of 1.0-3.0 GHz are shown in Figure 78. For comparison purposes, the simulated S parameters using the FDM in [46] without domain decomposition with a 1600×800 mesh are also shown in Figure 78. Figure 78 shows that with different grid size ratios, S parameters agree well with that using the FDM with a conformal mesh. The grid ratio denotes the ratio of grid size in Domain 1 to that in Domain 2. At 2 GHz, the simulated E field distribution with a grid ratio of 1:8 using the proposed method is shown in Figure 79. This shows the continuity of electric field is maintained at the interface. In addition, the comparison of simulated and computed analytical resonance frequencies are shown in Table 17. As shown in Table 17, compared to the computed resonance frequencies using Eqn. (71), the maximum error is 0.7%, indicating the accuracy of the proposed method.

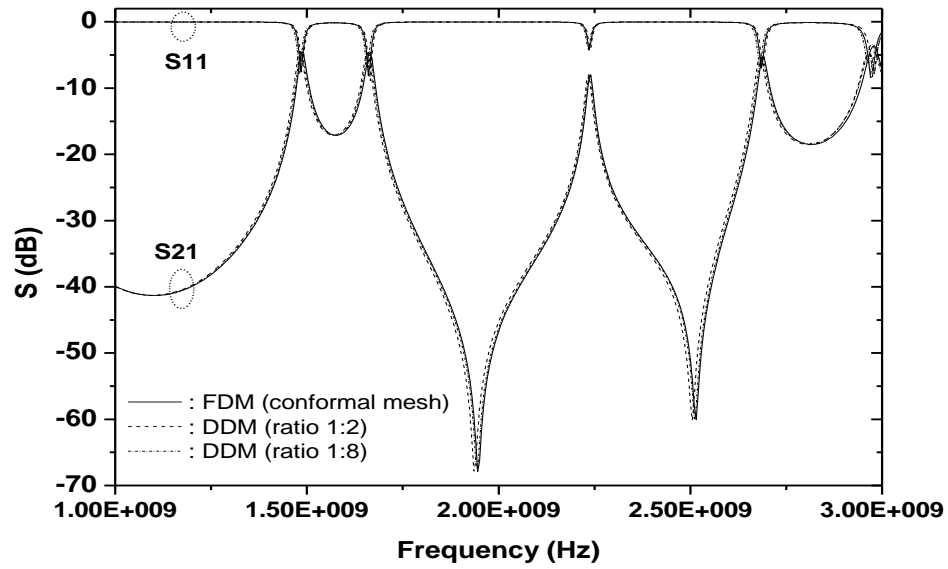


Figure 78. Two-port scattering paramters.

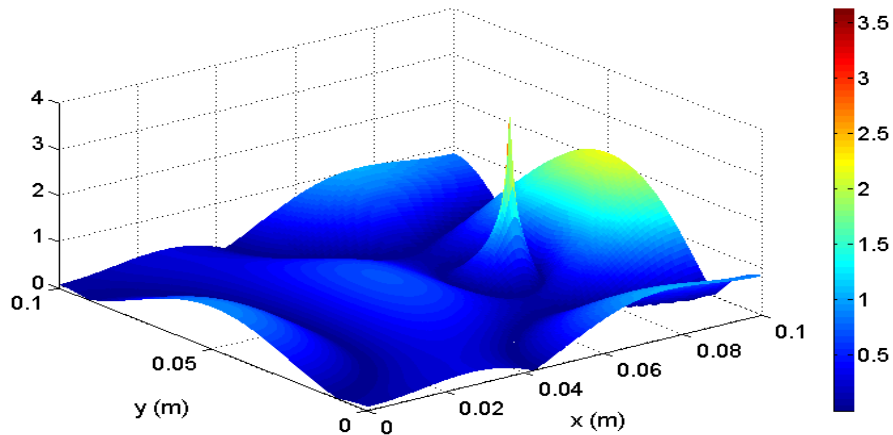


Figure 79. Electric field distribution across the structure with an excitation at port 2.

Table 17. Comparison of resonance frequencies.

Proposed Method (GHz)	FDM (GHz)	Analytical Method (GHz)	Error (%)
0.745	0.745	0.750	0.7
1.490	1.495	1.499	0.6
1.665	1.670	1.676	0.7
2.240	2.245	2.249	0.4
2.690	2.700	2.703	0.5
2.980	2.982	2.999	0.6

7.3 Summary

In this chapter, we presented the finite-difference non-conformal domain decomposition method for solving 2D electromagnetic problems. The formulation of the non-conformal domain decomposition is derived based on the finite difference method. We demonstrated the following: (a) the finite-difference electromagnetic modeling can employ non-matching grids at interfaces, (b) the continuity of pointwise electric fields can be maintained by introducing the Lagrange multiplier, and (c) the entries of the coupling matrices for domains depend on the sizes of grids in domains because of the finite-difference approximation, which differs from the Mortar FEM. In addition, the correctness of the proposed formulation has been verified using a simulation example.

CHAPTER 8

CONCLUSIONS

The continuous miniaturization of electronic systems using the 3D integration technique has brought in new challenges for the computer-aided design and modeling of ICs and integrated systems. As discussed in Chapter 1 and 2, the challenges mainly stem from three aspects: (1) the interaction between the electrical, thermal, and mechanical domains in an integrated system, (2) the increasing modeling complexity arising from 3D systems requires the development of multiscale modeling techniques for the modeling and analysis of DC voltage drop, thermal gradients, and electromagnetic behaviors, and (3) the demands of performing fast simulation with varying design parameters for thermal modeling. To address these challenges, several numerical modeling and simulation techniques are developed and presented in Chapters 3-7. The presented numerical techniques can be classified into three categories: (1) electrical-thermal co-simulation approaches: the voltage drop-thermal co-simulation methodology in steady state and thermal-electrical co-analysis for TSV arrays at high frequencies, (2) multiscale modeling approaches: the voltage drop/thermal modeling using the finite element-based non-conformal domain decomposition approach and 2D electromagnetic modeling using the finite difference-based non-conformal domain decomposition technique, and (3) fast thermal simulation methods using compact models and model order reduction.

8.1 Contributions

The contributions of this thesis are summarized as follows:

1) **DC voltage drop-thermal co-simulation for power delivery networks**

A voltage drop-thermal co-simulation method has been proposed and developed for the steady-state analysis of PDNs. The proposed co-simulation method ultimately takes into account the temperature effect on electrical resistivities and Joule heating effect on temperatures using an iterative simulation procedure. The proposed method allows performing the voltage drop analysis of a PDN considering the non-uniform temperature distribution in a system. This method can also capture the temperature increase because of Joule heating generated in a PDN.

In addition, several finite-volume schemes based on non-uniform rectangular grids have been developed for steady-state thermal and voltage drop modeling. For the modeling of voltage drop, the location-dependent temperatures are included in the formulation. In addition, the finite-volume scheme for microfluidic cooling has also been developed. This scheme enables the thermal modeling with both solid and fluid media in stacked ICs.

2) **The thermal-electrical analysis of TSV arrays in silicon interposers**

The thermal-electrical analysis has been carried out for TSV arrays in silicon interposers. This co-analysis method extends the TSV modeling method using CMBFs [69] to capture the thermal effect on TSV characteristics. By taking into account the temperature effect on material properties in the modeling process, the thermal effect on the insertion loss, crosstalk, RLGC parameters, and coupled noise of TSV arrays has been investigated. This co-analysis method can facilitate the design of TSV arrays considering system thermal profiles.

3) The development of a multiscale modeling method for the steady-state voltage drop and thermal analysis

A multiscale modeling method based on the finite-element non-conformal domain decomposition technique has been proposed for the voltage drop and thermal analysis of 3D systems. The proposed method allows the modeling of a 3D multiscale system using independent mesh grids in sub-domains. As a result, the system unknowns can be greatly reduced. In addition, to improve the simulation efficiency, the CMG solving approach has been adopted for the voltage drop-thermal co-simulation with a large number of unknowns.

4) The development of a compact thermal model for microchannel-based fluidic cooling

To overcome the computational cost using the CFD approach, a finite-volume compact thermal model has been developed for the microchannel-based fluidic cooling. The proposed thermal model uses only one unknown per cell to represent the fluidic cooling behavior. As a result, this compact thermal model enables the fast thermal simulation of 3D ICs with a large number of microchannels for early-stage design. In addition, this compact model can be integrated with the finite-element thermal model for solid media based the energy conservation rule.

5) The development of a fast transient thermal modeling approach

A fast transient thermal simulation approach based on the finite-element non-conformal domain decomposition has been proposed. The combination of the domain decomposition method and the compact thermal model for fluidic cooling enables the fast transient simulation of stacked ICs with fluidic cooling. The

accuracy of the proposed method has been validated by comparing the results from the proposed method with results from the FEM.

6) **The development of a system-level thermal modeling approach using domain decomposition and model order reduction**

A system-level thermal modeling method using domain decomposition and model order reduction is developed for both the steady-state and transient thermal analysis. The proposed approach can efficiently support thermal modeling with varying design parameters (e.g., thermal conductivity of a certain layer and heat transfer coefficients on boundaries) without using parameterized MOR techniques. By dividing a system into subdomains, the reduced-order models for separated domains can be efficiently created using MOR techniques with less computational cost than directly performing MOR for the entire system. The relationship between domains is captured using interfacial coupling matrices via the Lagrange multipliers and Schur complement; therefore, interfacial MOR ports are not required.

7) **The development of a finite-difference non-conformal domain decomposition method for solving 2D electromagnetic problems**

A finite-difference non-conformal domain decomposition method is developed for solving two-dimensional electromagnetic problems in the frequency domain. The proposed method allows the modeling of 2D electromagnetic problems using the finite difference method with non-matching meshing grids at interfaces. Connectivities between domains are maintained by introducing Lagrange multipliers and basis functions for the finite difference formulation.

8.2 Publications

During the dissertation research, the following journal articles and conference papers have been accepted and published.

Journal papers

- [1] D.-C. Yang, **J. Xie**, M. Swaminathan, X.-C. Wei, E.-P. Li, “A rigorous model for through-silicon vias with Ohmic contact in silicon interposer,” *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 8, pp. 385–387, Aug. 2013.
- [2] **J. Xie**, M. Swaminathan, “System-level thermal modeling using non-conformal domain decomposition and model order reduction,” *accepted by IEEE Trans. Compon., Packag. Manuf. Technol.*, 2013.
- [3] **J. Xie**, M. Swaminathan, “Electrical-thermal co-simulation with non-conformal domain decomposition method for multiscale 3D integrated systems,” *accepted by IEEE Trans. Compon., Packag. Manuf. Technol.*, 2013.
- [4] **J. Xie**, M. Swaminathan, “Electrical-thermal modeling of through-silicon-via (TSV) arrays in interposer,” *International Journal of Numerical Modeling*, Sept. 2012.
- [5] **J. Xie**, M. Swaminathan, “Electrical-thermal co-simulation of 3D integrated systems with micro-fluidic cooling and Joule heating effects,” *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 234–246, Feb. 2011.
- [6] M. Swaminathan, D. Chung, S. Grivet-Talocia, K. Bharath, V. Laddha, **J. Xie**, “Designing and modeling for power integrity,” *IEEE Trans. on Electromagnetic Compatibility*, vol. 53, no. 2, pp. 288–310, 2010. (Invited paper)

Conference papers

- [7] R. Bazaz, **J. Xie**, M. Swaminathan, “Electrical and thermal analysis for design exchange formats in three dimensional integrated circuits,” *International Symposium on Quality Electronic Design (ISQED)*, pp. 308–315, 2013.
- [8] R. Bazaz, **J. Xie**, M. Swaminathan, “Optimization of 3D stack for electrical and thermal integrity,” *Electronic Components and Technology Conference (ECTC)*, pp. 22–28, 2013.
- [9] **J. Xie**, M. Swaminathan, “3D transient thermal solver using non-conformal domain decomposition approach,” *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 333–340, 2012.

- [10] **J. Xie**, M. Swaminathan, “Fast electrical-thermal co-simulation using multigrid method for 3D integration,” *Electronic Components and Technology Conference (ECTC)*, pp. 651–657, 2012.
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- [12] B. Xie, M. Swaminathan, K. J. Han, **J. Xie**, “Coupling analysis of through-silicon via arrays in silicon interposers for 3D system,” *IEEE International Symposium on Electromagnetic Compatibility*, pp. 16–21, 2011.
- [13] **J. Xie**, M. Swaminathan, “DC IR drop solver for large scale 3D power delivery networks,” *19th conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, pp. 217–220, Oct. 2010.
- [14] **J. Xie**, M. Swaminathan, “Simulation of power delivery networks with Joule heating effects for 3D integration,” *Electronics System Integration Technology Conferences (ESTC)*, pp. 1–6, Sept. 2010.
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- [16] J. Xie, D. Chung, M. Swaminathan, M. Mcallister, A. Deutsch, L. Jiang, B. J Rubin, “Effect of system components on electrical and thermal characteristics for power delivery networks in 3D system integration,” *18th conference on Electrical Performance of Electronic Packaging and Systems*, pp. 113–116, Oct. 2009.

8.3 Patent Application

- J. Xie, M. Swaminathan, Electrical-Thermal Co-Simulation with Joule Heating and Convection Effects for 3D Systems, US patent application 13/224270, pending, 2011.

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