SIGE BICMOS RF FRONT-ENDS FOR ADAPTIVE WIDEBAND RECEIVERS

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SIGE BICMOS RF FRONT-ENDS FOR ADAPTIVE WIDEBAND RECEIVERS

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To,

my parents,

Kalpana and Ranajit.

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SUMMARY

The pursuit of dense monolithic integration and higher operating speed continues to push the integrated circuit (IC) fabrication technologies to their limits. Transistor dimensions are being scaled down with each passing generation of process technologies to improve performance and increase integration. But reducing transistor size, termed as technology scaling, is also associated with increased variability. In statistical terms, the increase in the mean performance is associated with an increase in the standard deviation. The increasing variation is having a negative impact on circuit yield in current IC technologies, and the problem is likely to become worse in the future. Circuit solutions that are more tolerant of the process-related variations are needed to fully utilize the benefits of technology scaling and improve yield. The primary goal of this research is to develop high-frequency circuits and systems that are capable of delivering consistent performance even under the threat of increasing process variation. These circuits can be used to build "self-healing" systems, which are able to detect process imperfections and compensate accordingly to deliver optimized performance. In addition to improving yield, such adaptive circuits and systems can provide more robust and efficient solutions for a wide range of applications under varying operational and environmental conditions.

Silicon-germanium (SiGe) BiCMOS technology is an ideal platform for highly integrated systems requiring both high-performance analog and radio-frequency (RF) circuits as well as large-scale digital functionality. For monolithic implementation of high-performance complex mixed-signal systems, SiGe BiCMOS offers capabilities not available in any other integrated-circuit platform. Thus, SiGe BiCMOS serves as an ideal platform for developing and demonstrating self-healing circuit solutions. This

research is focused on designing circuit components for a high-frequency wideband self-healing receiver in SiGe BiCMOS technology. The major contributions of this research are summarized as follows:

1. An adaptive wideband (6-20 GHz) image-reject mixer, suitable for use in a self-healing receiver, was designed. Automated simultaneous healing of multiple circuit parameters was demonstrated in measurement [1–3]. A monte-carlo simulation based methodology for verification of healing was developed. Circuits and algorithms were designed to achieve high image rejection ratio (IRR) over a wide bandwidth.

2. A wideband SiGe low-noise amplifier was designed. It was shown that the performance of the resistive feedback LNA can be enhanced by using small reactive elements with little area penalty [4].

3. Low-loss switches were implemented in bulk and silicon-on-insulator (SOI) technologies. The insertion loss of the bulk switches were reduced by using deep trench to isolated the bulk of the devices [5]. The SOI switches, to the best of the author's knowledge, feature lowest loss among all published wideband CMOS switches.

CHAPTER I

INTRODUCTION

1.1 Origin and History of the Problem

Microelectronics is undoubtedly at the forefront of technologies that have shaped our lives in the past few decades. We are now in the middle of a revolution that is making profound and pervasive changes to every sphere of human activity. Most visible changes have taken place in the fields of computing, communication, and consumer electronics. Cellular phones, personal computers, global positioning system (GPS), and internet are some of the many marvels that have become integral parts of our lives. It can be safely said that microelectronics has been the enabler for productivity and growth in virtually all areas of human activities. The revolution, which began with the invention of solid-state transistor by William Shockley in 1947, gained momentum rapidly when planar integrated circuit (IC) was fabricated for the first time by Jack Kilby in 1958. In the early years, the ICs had only a few transistors in them. Since that modest beginning, in a span of mere 50 years, we have now come to a point where billions of transistors are fabricated on ICs measuring less than a square centimeter. Over the years, electronic products have become smaller, cheaper, more powerful, and more reliable. One of the key factors, which made this revolution possible, is the reduction of transistor dimensions.

1.1.1 Technology Scaling

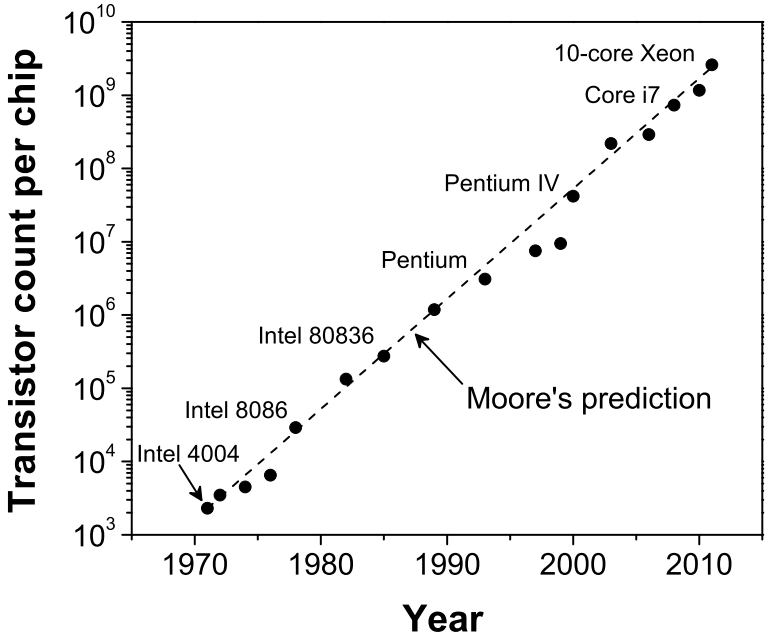
A remarkable trend in the growth of the integrated circuits was first observed by Gordon Moore, one of the co-founders of Intel. In a short paper published in 1965, Moore outlined the trends of growing integration complexity, forming the basis of the legendary Moore's law. Moore pointed out that the number of integrated components

per chip, which minimizes the overall cost of the product, was doubling every year and predicted that this trend would continue in the foreseeable future. The time period for the "doubling of components" was later revised to be 18 months by Moore himself. Nevertheless, his prediction of this exponential growth has been valid for the last 50 years. Moore's law, which was an observation to begin with, subsequently became the trend-setter for increasing integration complexity and has been the basis for the sustained exponential growth in computing power, memory capacity, and the ubiquitous presence of cheap electronics all around us [6]. As an example demonstrating Moore's law, increasing complexity of Intel microprocessors is shown in Figure 1. The number of transistors per chip for Intel microprocessors is plotted in Figure 1a from the date of their introduction in 1971 to 2011. The most important factor behind this phenomenal growth is the reduction of the size of the transistors. The minimum feature size for the Intel microprocessors from 1971 to 2011 is plotted in Figure 1b. Not surprisingly, the rate of change is exponential in nature.

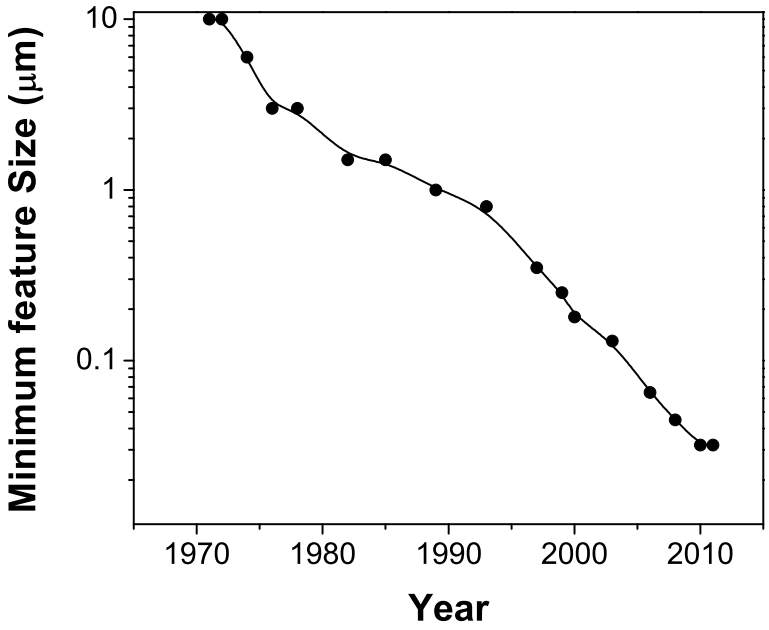
In addition to all the advantages related to Moore's law, a smaller transistor also results in higher intrinsic speed of operation. The current generation of processors has a minimum feature size of 32 nm, which is comparable to the size of viruses. As transistor size continues to approach atomic dimensions, the field of IC manufacturing is ripe with speculations regarding the future of Moore's law [6–8]. The end is inevitable. As Moore himself famously said [9], "No exponential is forever." The question is, what can we do to delay the inevitable?

1.1.2 Process Variation and Impact on Yield

Process variation is the term used to describe the statistical variation in the attributes of the circuit components during fabrication. Transistors with smallest dimensions are most susceptible to process variation. The process variation is characterized in terms of "process corners", which usually represent three-sigma limits of the distribution,



(a) Transistor count over time



(b) Transistor size over time

Figure 1: Exponential change of integration complexity: (a) Transistor count of Intel microprocessors over time (b) Minimum transistor size of Intel microprocessors over time.

and the circuits are designed to be functional within the boundaries of the process corners.

As lithographic limits are being pushed to keep pace with Moore's law, process variations are steadily increasing (Figure 2). As shown in Figure 2, improvement in the worst-case performance is much smaller as compared to that of the nominal case. While relying on the worst-case models will result in over-design and waste of resources, using models based on nominal performance run the risk of taking a significant hit in terms of yield. Moreover, these process corners, although suitable for digital designs, fail to adequately represent effect of process variations on analog circuits. Various techniques are used at present to nullify effects of process variations. But there certainly is room for improvement, especially in the domain of high-frequency design. Post-fabrication trimming using fuses is good for one time adjustment and also occupies lots of area. Common-centroid layout, which is used to reduce mismatch, is difficult to implement at high frequencies due to added parasitic.

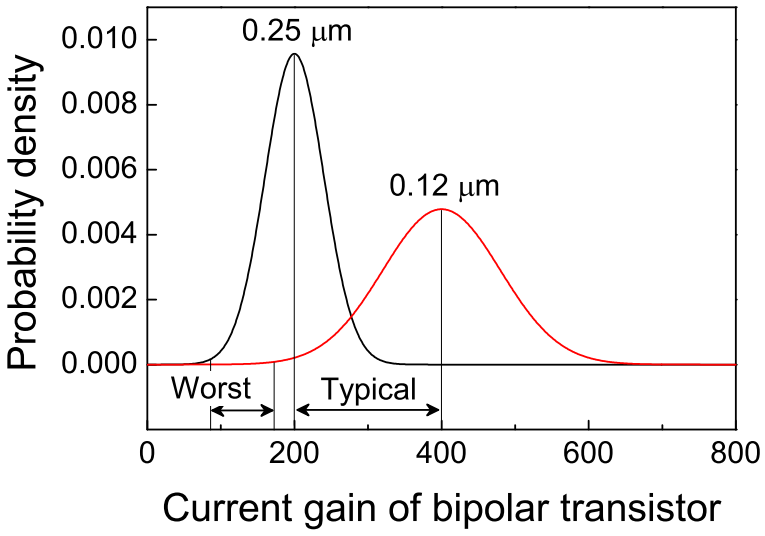


Figure 2: Process variation increases with scaling down of feature size.

One way to nip the problem in the bud is to improve process technologies to reduce process variation itself. Significant amount of effort is spent to achieve better control

over the process of fabrication. But, despite best efforts, process variations have been increasing steadily. The other option is to design circuits that can adapt and function even when process variations are present. Modern microprocessors employ techniques to cope with the evils of process variation [10, 11]. To achieve similar goals for high-frequency systems, design approaches and circuit solutions need to be developed.

1.2 Concept of Self-healing Circuits

One emerging way of dealing with the problem of increasing process variation is to use "self-healing" circuits, which can detect, isolate, and fix its own flaws. The act of self-healing can be partitioned into three functions: sensing, processing, and actuating. Sensors are needed to detect and measure departure from the expected behavior, processing elements are needed to determine what is necessary to fix the problem, and actuators are needed to carry out the actions. Such circuits are partly inspired by biological systems that constantly heal themselves in the presence of random failures.

Ideas similar to self-healing have been tried in the domain of microprocessors [11,12] and memory design [13,14]. The field of high frequency circuits adds an extra layer of complexity to the problem due to increased sensitivity to parastic elements. The idea of self-healing radio-frequency (RF) circuits is being pursued actively at present. Increasing number of recent publications related to this topic [15–19] attests to the growing interest in the problem and the importance of it.

As an example, a block diagram of a self-healing receiver system is shown in Figure 3. The receiver chain consists of a low-noise amplifier (LNA), a mixer, and an analog-to-digital converter (ADC). The response of the system to a known test signal is analyzed by a baseband processor and corrective actions are taken if necessary.

This approach is quite similar to built-in-self-test (BIST) methodology, as far as sensing and processing of information are concerned. But the idea of self-healing also

has the added capability of fixing the problems. For an efficient implementation of this idea of self-healing, the individual circuit blocks need to be capable of adapting their performance in response to control signals, and the processor needs to be aware of the behavioral model of the circuit elements.

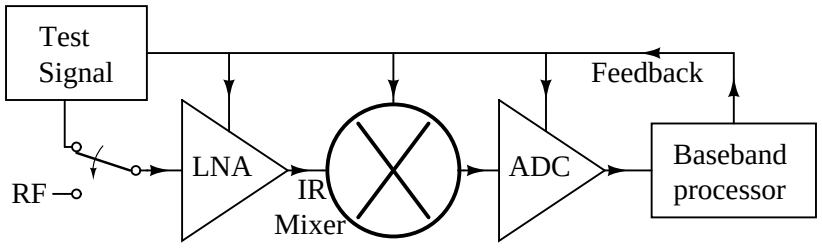


Figure 3: Concept of a self-healing receiver system.

1.3 A Brief Introduction to SiGe HBTs

The heterojunction bipolar transistor (HBT) can be described as an enhanced version of the conventional bipolar junction transistor (BJT). To enhance desired performance aspects, the band diagrams of these devices are modified compared to the band diagram of a conventional BJT. In semiconductor materials, the bandgap can be adjusted by introducing an alloy of another material into a single crystalline growth. The technique of adjusting the bandgap, known as bandgap engineering, is used to produce the highest-performance transistors. A number of different materials are used to build these HBTs, e.g., Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN) etc. However, there is currently only one physically realizable silicon-based heterostructure that combines the performance of bandgap engineering with the processing advantages of silicon: the Silicon-Germanium (SiGe) HBT. Development of the SiGe HBT has spanned many decades. Although the original concept was first considered by William Shockley during development of bipolar device physics, it took over 30 years to produce a working prototype due to limitations in fabrication capability. An excellent history of SiGe process development is given in [20]. When germanium atoms are substituted for silicon atoms in the diamond-lattice crystalline

structure, a narrowing of the bandgap occurs primarily through the valence band. The bandgap narrowing is a function of the amount of germanium in the alloy. A precisely controlled germanium profile, spanning the width of the base, results in controlled modulation of the device bandgap. There are multiple effects that can be achieved by altering the bandgap of a bipolar transistor. A linear-ramped germanium profile and the corresponding band diagram is shown in Figure 4. The start of the neutral base region is set as the origin, x = 0, while the other end of the neutral base is at x = Wb. The bandgap is the difference between the conduction and the valence bands, and is shown for both the Si BJT and SiGe HBT in the band diagram of Figure 4. The bandgap narrows as the germanium content increases across the width of the neutral base, producing the sloped conduction band seen in the SiGe band diagram. The sloped band diagram in the neutral base region corresponds to an electric field that pushes minority carriers through the neutral base according to traditional drift-carrier transport. This electric field has two important effects on static device characteristics. First, it reduces the base transit time of minority carriers, improving the speed of the device. The graded germanium profile also increases the output resistance of the HBT by impeding changes in the depletion region of the base-collector junction.

The germanium profile in the base can be changed to achieve different goals. In Figure 5, the added germanium reduces the bandgap uniformly across the neutral base. Since there is no electric field induced by the sloping bandgap, the transit time improvements are not present here. Instead, the bandgap narrowing reduces the potential barrier at x = 0 in the emitter-base junction, allowing many more minority carriers to diffuse from the emitter into the base at a fixed bias voltage. This effect increases the DC current gain since there is not a significant increase in base recombination, and the base current remains nearly identical to that of a similar Si BJT. A hybrid of the box and linear-ramp profiles can also be used. These hybrids

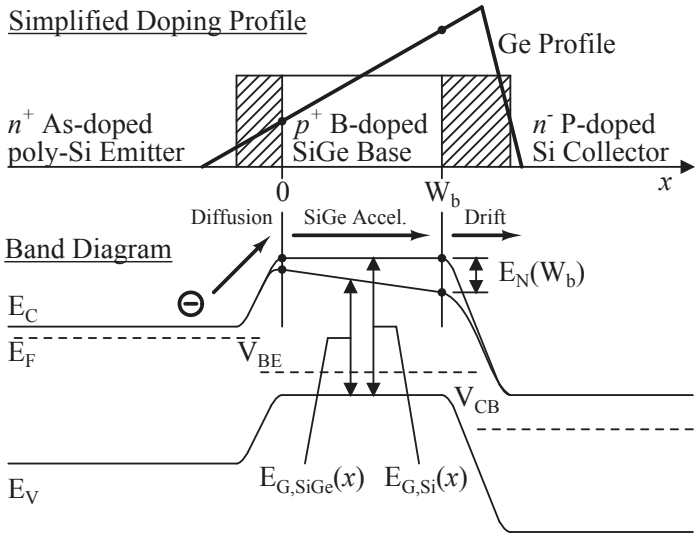


Figure 4: A ramp germanium profile creates an electric field that accelerates minority carriers through the neutral base, improving base transit time and output impedance.

are referred to as trapezoidal profiles and often feature significant germanium content at x = 0 as well as a linear ramp across the neutral base.

Another important feature of the SiGe HBT devices is the exponential current relationship with the thermal voltage (kT). As temperature decreases, the circuit parameters increase proportionally. Leveraging this technique has produced record speeds in silicon-based circuits. With a wide number of profile combinations and a scarce amount of germanium available due to stability limits, germanium profile design is an application-dependent engineering problem with numerous trade-offs to consider. A snapshot of several state-of-the art SiGe processes from 2006 can be found in [20]. More details on SiGe HBT devices can be found in [20] and [21].

Yet another important advantage that SiGe HBT enjoys over other III-V technologies is its integration capability with complementary metal-oxide-semiconductor (CMOS) technology. At present, CMOS is the workhorse of the digital IC world. But CMOS alone is not sufficient to provide solutions for high-performance applications. SiGe HBTs fill that gap nicely, and can be easily integrated in the standard

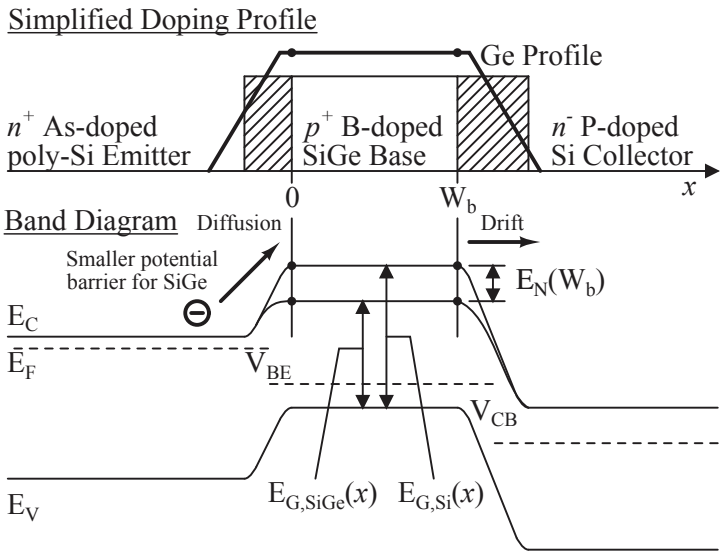


Figure 5: A profile with large germanium content at x = 0 reduces the potential barrier for minority carrier injection into the base, improving DC current gain and small signal transconductance for a fixed bias voltage.

CMOS process flow at a minimal cost overhead. For monolithic implementation of high-performance complex mixed signal systems, SiGe BiCMOS offers capabilities that are not available in any other integrated-circuit platform.

1.4 Research Objectives

The purpose of this research is to develop high-frequency circuits and systems that are capable of delivering consistent performance even under the threat of increasing process variation in aggressively scaled fabrication technologies. The primary focus is on designing circuit components for a high-frequency, wideband, self-healing receiver in SiGe BiCMOS technology. The wideband nature of the circuits adds to the flexibility of the system, making it possible to handle multiple standards and frequency bands. A secondary goal of this research is to improve performance of these wideband circuits. Development of healing algorithms and demonstration of "self-healing" also naturally falls under the purview of this research.

CHAPTER II

WIDEBAND LOW-NOISE AMPLIFIER

A wideband low noise amplifier (LNA) was designed and implemented in a 120-nm SiGe BiCMOS technology. Resistive shunt-shunt feedback is employed to achieve wideband gain and matching characteristics, and it is shown that addition of small reactive elements can extend the bandwidth of the amplifier significantly. Measured data for the LNA show 9.5 dB gain with less than 1.0 dB variation over a frequency range of 3-26 GHz. Input and output reflection coefficients (S_{11} and S_{22}) are better than -10 dB over the entire bandwidth. The measured noise figure (NF) is less than 5 dB below 18 GHz and rises to only 6.5 dB at 24 GHz. In addition, the amplifier exhibits excellent linearity performance, with a input-referred third-order intercept point (IIP3) of 5.8 dBm and input-referred 1 dB compression point (P1dB) of -5.6 dBm. The SiGe amplifier occupies 0.48 mm^2 (including pads) and consumes 33 mW of power while operating on a 3.3 V supply.

Wideband low noise amplifiers are critical components of virtually all broadband communication systems. In recent years, allocation of the 3-10 GHz frequency band for ultra-wide band (UWB) applications has fueled tremendous interest in this domain [22] and resulted in a flurry of publications [23], [24], [25], [26]. Wideband LNAs also find extensive application in instrumentation, optical communication, and software defined radios. An amplifier with good matching and noise performance is essential to all such applications.

Known wideband amplifiers can be categorized into four different topologies. Narrow-band concepts can be extended for broadband applications by having higher-order matching networks at the input and output. But inclusion of a large number

of inductances and capacitances becomes prohibitively costly in terms of chip area, and the inherent low quality-factor (Q) of such passive elements for monolithic implementation in silicon degrades the noise performance. Common-base or common-gate amplifiers provide inherent wideband characteristics but suffer from low gain and high noise figure. Distributed amplifiers, while being the best choice for extremely large bandwidth, suffer from large die area and high power consumption. Resistive-feedback LNAs, on the other hand, provide a compact solution with good wideband noise performance and low power consumption. Several implementations covering the 3-10 GHz UWB band can be readily found in the literature. Traditional inductor-less resistive-feedback LNAs provide a very compact solution, but at the same time limits the achievable maximum operating frequency. In the present paper, we investigate the limits of the resistive-feedback LNA topology and demonstrate how its operating bandwidth can be further extended by using small inductances, with very little area penalty.

There has been some discussion in the literature along similar lines in recent years [27], [28]. In [27], for instance, use of a π-matching network at the input has been shown to improve input matching. In this work, the effects of a matching network on the input matching, gain and noise are analyzed in the context of a SiGe amplifier. A design approach, that exploits the parasitic elements in the circuit to implement the matching network and improves performance, is presented. Theoretical analysis of the impact of reactive matching on resistive-feedback amplifier is presented in section 2.1. In section 2.2, the implementation details of the present LNA are discussed. Measurement results and a comparison with other published data are given in section 2.3, followed by a summary.

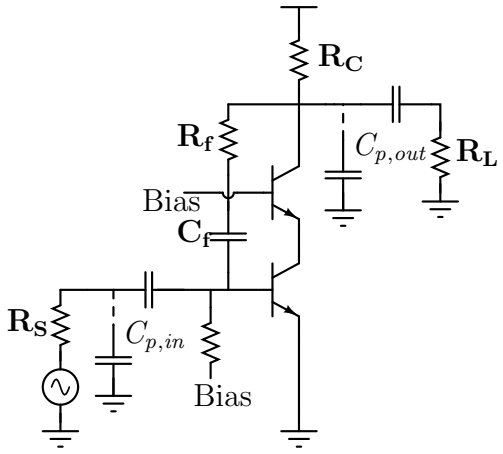


Figure 6: Schematic of a generic shunt-shunt resistive-feedback LNA.

2.1 Analysis of a Resistive-Feedback Amplifier with Reactive Matching

Figure 6 shows a resistive shunt-shunt feedback amplifier in its standard form, with parasitic capacitances added to the input and the output nodes. A small-signal equivalent model is shown in Figure 7, in which the parasitic capacitances are absorbed into the input and output capacitances (C_{in} and C_{out}). At low frequency, under the assumption that the device input impedance is much higher than R_f, straightforward analysis yields expressions for input and output resistances, which can be expressed as

$$R_{in} = \frac{R_f + R_L^{'}}{1 + g_m R_L^{'}} \tag{1}$$

and

$$R_{out} = R_C || (\frac{R_f + R_S}{1 + g_m R_S}), \tag{2}$$

where $R_L^{'} = R_C || R_L$. In the following analysis, we examine how the capacitances cause the impedances to depart from their ideal values and how this situation can be improved by designing a revised matching network. The effects of reactive matching on gain and noise is also considered.

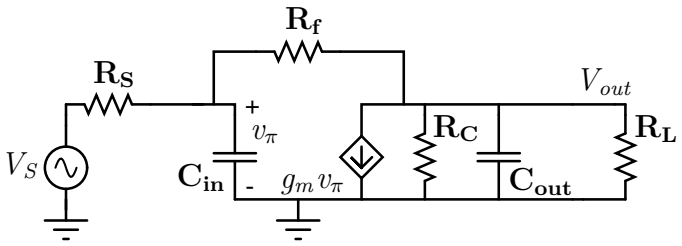


Figure 7: Small-signal model of a resistive-feedback amplifier.

2.1.1 Input Matching

The assumption of very high device input impedance breaks down at high frequencies. Device input capacitance, represented by C_π in the small-signal model, moves the input impedance (Z_{in}) away from its ideal value. Any parasitic capacitance present at the input node, due to DC blocking capacitance or bondpads, adds to the effect and further deteriorates the input matching. The input impedance, including these described effects, can be expressed as

$$Z_{in} = R_{F,in} || (\frac{1}{j\omega C_{in}}), \tag{3}$$

where $R_{F,in} = (R_f + R_L^{'})/(1 + g_m R_L^{'})$ and $C_{in} = C_\pi + C_{p,in}$. The small-signal equivalent circuit is shown in Figure 8.

$R_{F,in}$ is often designed to be equal to R_S, which is usually 50 Ω for most RF systems. Under that assumption, we start from a perfect match at DC and the locus of the reflection coefficient moves along a constant conductance circle, as shown in Figure 8.

The condition of S_{11} being less than 10 dB can be taken as a reasonable measure for good input matching and expressed as

$$20.log \left| \frac{1/R_S - 1/R_F - j\omega C_{in}}{1/R_S - 1/R_F + j\omega C_{in}} \right| < -10, \tag{4}$$

which can be simplified to

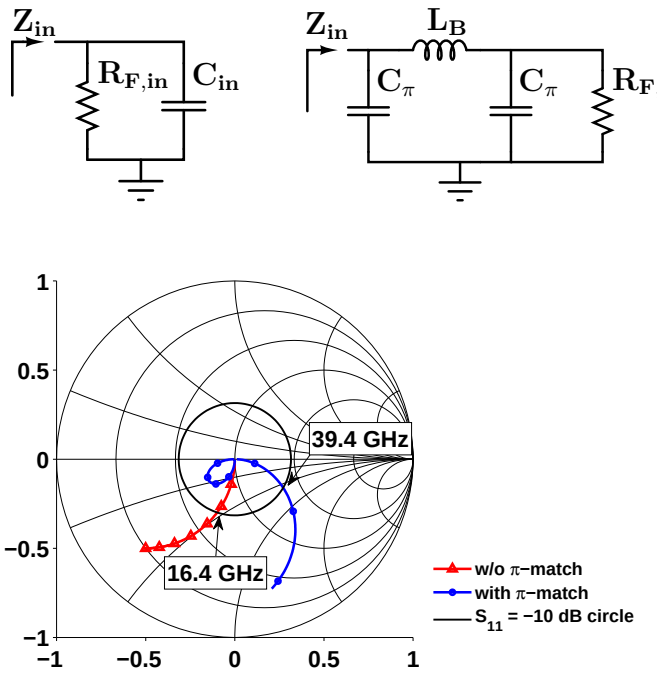


Figure 8: Equivalent small-signal representation of input impedance: (a) without matching and (b) with π-matching network. (c) Loci of S_{11} with and without π-matching network at the input.

$$\omega^2 < (-1 + 3.84/r - 1/r^2).\frac{1}{R_S C_{in}^2}, \tag{5}$$

where $r = R_F/R_S$. From Equation (5), it can be easily found out that the input matching bandwidth is maximized for $r = 0.72$. But a smaller R_F would also mean a higher noise contribution from the feedback resistor and hence will degrade overall amplifier noise figure.

The input matching bandwidth can be extended if an inductor (L_B) is added at the base of the input device. Figure 8 shows the transformed equivalent circuit as far as the input impedance is concerned. L_B separates the device capacitance (C_π) from the parasitic capacitances and forms a π-matching network. For the following analysis, it is assumed that the π network is symmetric. This can be achieved by adding capacitance to the input node if necessary. Figure 8 shows the locus of S_{11} on the Smith Chart and Figure 9 shows how the S_{11} magnitude compares to the

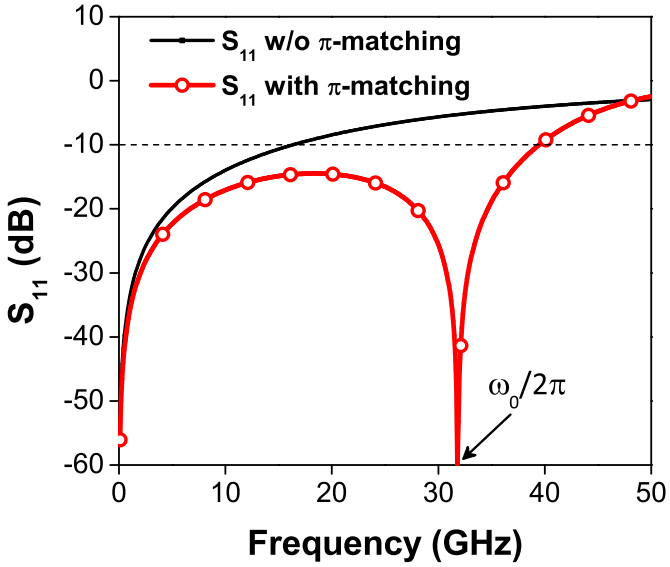


Figure 9: S_{11} with and without the π-matching network at the input.

standard resistive-feedback amplifier. In addition to DC, the π-matching network provides perfect matching at $\omega_0/2\pi$. The frequency ω_0 can be easily found by noting the frequency at which the reactive part of Z_{in} goes to zero and can be expressed as

$$\omega_0 = \sqrt{\frac{2}{L_B C_\pi} - \frac{1}{R_{F,in}^2 C_\pi^2}}. \tag{6}$$

If ω_0 is not too far from DC, S_{11} stays below -10 dB for all intermediate frequencies and the matching bandwidth is thus greatly increased. In [27], it has been shown that a reasonable choice for ω_0 is

$$\omega_0 = \frac{1}{\sqrt{L_B C_\pi}}, \tag{7}$$

and the resultant bandwidth is given by

$$f_{10dB} = \frac{1}{2\pi}\sqrt{\frac{\sqrt{10}+3}{\sqrt{10}+1}}.\frac{1}{\sqrt{L_B C_\pi}}. \tag{8}$$

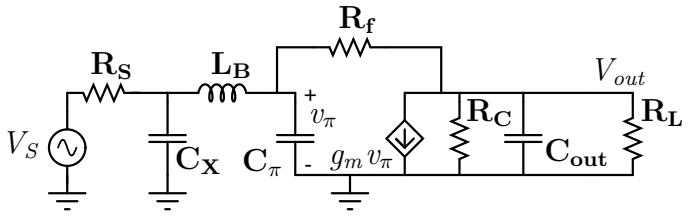


Figure 10: Small-signal model of the resistive-feedback amplifier for use in gain computation.

2.1.2 Gain

The small-signal equivalent circuit for computation of the gain is shown in Figure 10. It can be easily seen that the input matching network forms a third-order low-pass filter and there is another pole at the output. An exact analytical expression for small-signal gain ($A_V = V_{out}/V_S$) is too cumbersome to provide much insight. Under the assumption of $C_X = C_\pi = C$ and $R_S = R_{F,in} = \sqrt{L_B/2C_\pi} = R$ (where $R_{F,in} = (R_f + R_L^{'})/(1 + g_m R_L^{'})$), the small-signal gain can be expressed as

$$A_V = \frac{1/2}{s^3(\frac{LRC^2}{2}) + s^2(LC) + s(\frac{L}{2R} + RC)} . \frac{-g_m(R_F||R_L^{'})}{1 + s(R_F||R_L^{'})C_{out}}, \tag{9}$$

where $R_L^{'} = R_C||R_L$.

The key difference between this result and a purely resistive-feedback amplifier lies in the input matching network. The device input capacitance (C_π) is absorbed in the π section. A first-order pole at the input ($1/(R_S||R_{F,in}||\frac{1}{j\omega C})$) is replaced by a third-order low pass filter with a cut-off frequency ($1/\sqrt{LC/2}$), which is typically higher and thus improves overall frequency response. A comparison of the frequency response of S_{21} with and without the matching network is shown in Figure 11.

2.1.3 Noise

The small-signal model of the LNA including all significant sources of noise is shown in Figure 12. Noise contributions from R_E and r_b are included, although the effect of

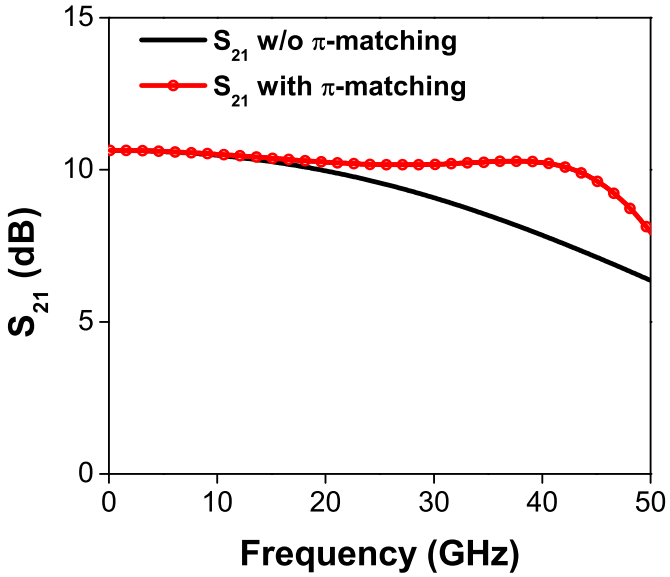


Figure 11: Effect of input-matching network on S_{21}.

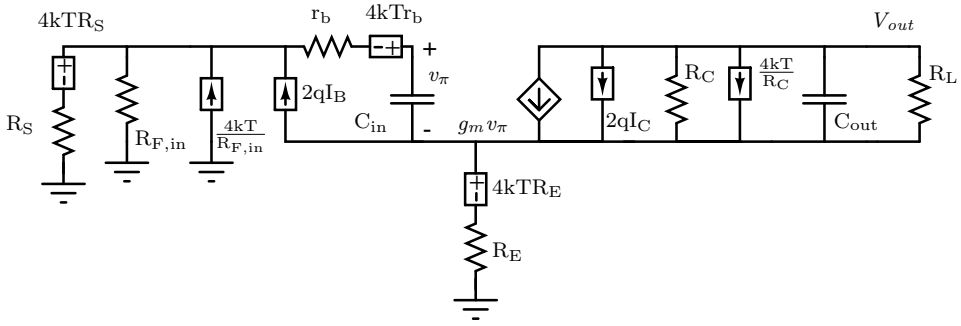


Figure 12: Small-signal model of a generic resistive-feedback amplifier including noise sources.

r_b is excluded from impedance calculations to reduce complexity. Equivalent input referred noise can be expressed as

$$\begin{aligned} v_{ni}^2/\Delta f = \quad & 4kT(R_S + r_b + R_E) + (\tfrac{4kT}{R_{F,in}} + 2qI_B) \\ & .(R_S||R_F)^2 + 2qI_B.R_E^2 \\ & + \tfrac{4kT/R_C + 2qI_C}{g_m'^2} \left|1 + j\omega(R_S||R_{F,in})C_\pi'^2\right|, \end{aligned} \tag{10}$$

where $g_m' = g_m/(1 + g_m R_E)$ and $C_\pi' = C_\pi/(1 + g_m R_E)$. Noise figure can be calculated as $v_{ni}^2/(4kTR_S)$. It can be readily seen from (10) that low frequency noise

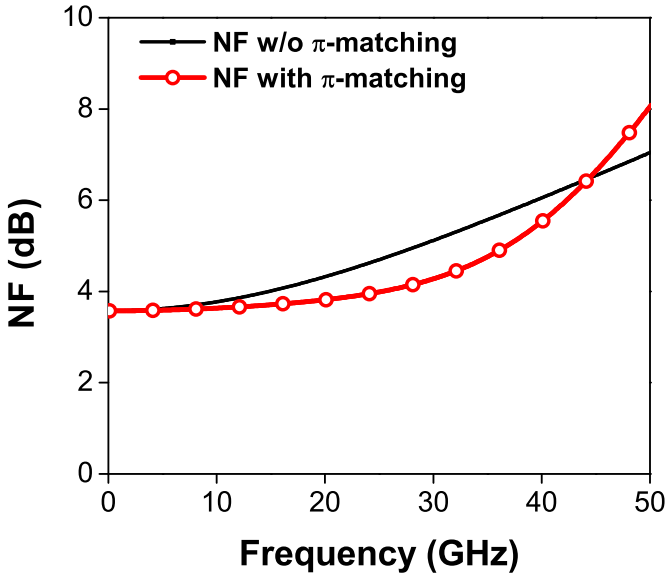


Figure 13: Effect of input-matching network on noise figure.

can be reduced by reducing R_E and increasing $R_{F,in}$, as expected.

With increasing frequency, collector current shot noise and load resistor thermal noise contributions increase, which is captured in the last term of Equation (10). This is due to the pole associated with the input node of the amplifier. Signals traveling through the pole get reduced in magnitude beyond the 3-dB cutoff frequency, but noise originating after the location of the pole ($2qI_C$ and $4kT/R_C$) is not affected, hence degrading the signal-to-noise ratio (SNR).

As discussed above, inclusion of the π matching network moves the input pole to higher frequency and hence increases the frequency at which the noise figure rapidly increases. In other words, the π-matching networks helps to maintain a flat noise figure across frequency, as shown in Figure 13.

2.2 Implementation

An LNA demonstrating this design approach was implemented in a 120-nm SiGe BiCMOS process with 7 metal layers. The SiGe HBTs have a peak f_T of 200 GHz. The devices were biased well below their peak f_T current density to optimize noise

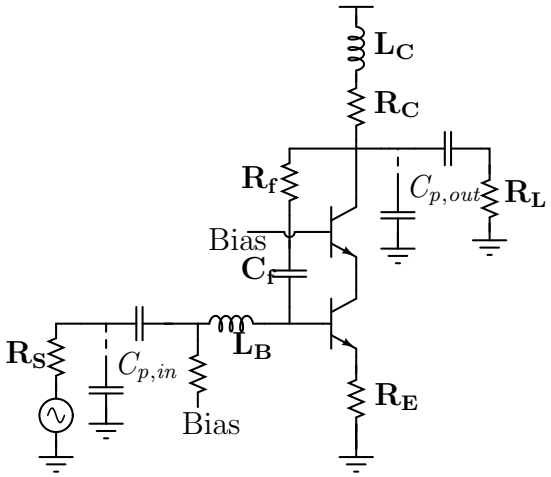


Figure 14: Schematic of the resistive-feedback LNA with reactive components for improved matching.

performance. The schematic is shown in Figure 14. An emitter degeneration resistor (R_E) was included to improve linearity. The effect of emitter degeneration can be easily included in the above analysis on matching performance by simply modifying the transconductance (g_m) and input capacitance of the device (C_π) by the degeneration factor ($1/(1 + g_m R_E)$). Parasitic capacitances at the input node ($C_{p,in}$, due to the bondpad and decoupling capacitor) along with the base inductance (L_B) and the device input capacitance (C_π), forms the input π-matching network. The implemented π network is not perfectly symmetric, but still results in a substantial performance improvement. A gain peaking inductor (L_C) was added to further boost the gain at high frequencies and flatten the gain response across frequency.

A die microphotograph of the LNA is shown in Figure 15. The die area including bondpads is 0.8 μm x 0.6 μm. This LNA is entirely monolithic and does not require any external bias-tee or RF-choke.

2.3 Measurement Results

On-wafer measurements were performed using a VNA for S-parameters and a spectrum analyzer for noise measurements. Measured S-parameters and comparison with

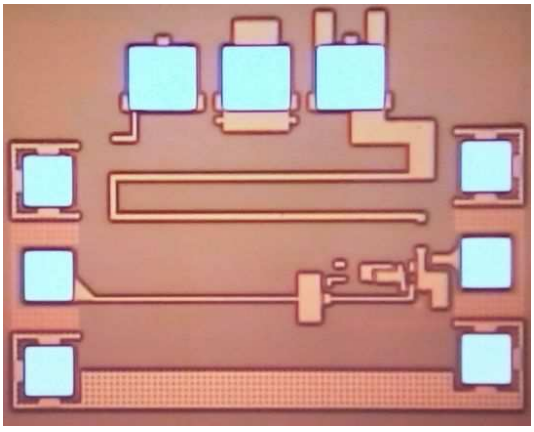


Figure 15: Die microphotograph of the wideband SiGe LNA.

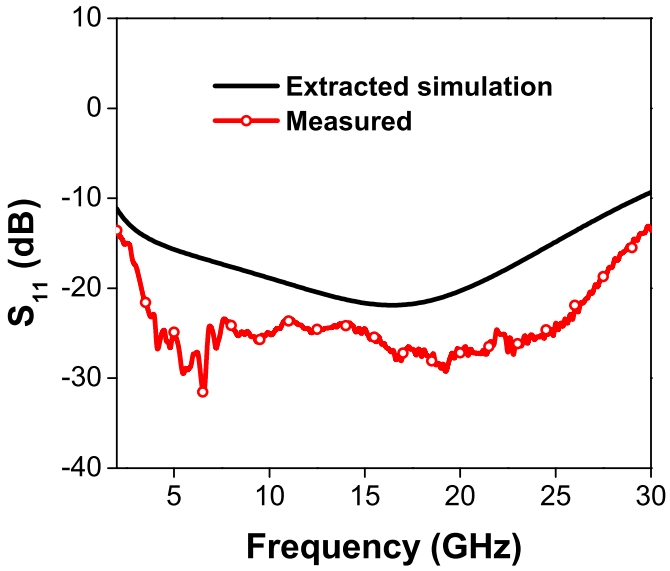


Figure 16: Measured and extracted input return losses (S_{11}) of the wideband SiGe LNA.

simulations are shown in Figure 16, Figure 17 and Figure 18. The measured gain (S_{21}) is nominally 9 dB (Figure 17) and exhibits a very flat frequency response, with less than 1 dB variation over a frequency range of 2-30 GHz. Measured input reflection coefficient (S_{11}) is less than -10 dB over 2-30 GHz. The effect of the input π-matching network can be clearly seen in Figure 16 as the dip in the S_{11} curve around 20 GHz. S_{22}, as shown in Figure 18, is better than -10 dB over 3-26 GHz. It should be noted that the low frequency limit of matching is imposed by the DC blocking networks at the input and the output and can be improved by increasing the size of the DC

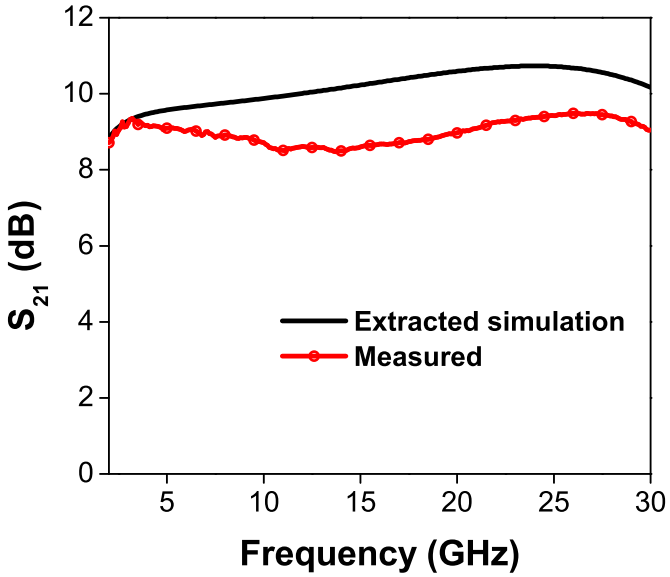


Figure 17: Gain (S_{21}) vs. frequency of the wideband SiGe LNA: comparison of measured and parasitic-extracted simulation results.

blocking capacitors, at the cost of increased die area and parasitic.

Simulated and measured noise figure are shown in Figure 19. The measured noise figure remains below 4.5 dB over 2-14 GHz. Beyond 18 GHz, the measured data did not match simulation very well, but the noise figure was still under 6.5 dB up to 24 GHz. Linearity, as shown in Figure 20, is excellent, with an output IP3 of 15 dBm and 1dB compression point of 1.85 dBm. Emitter degeneration was used to improve linearity, at the cost of increased noise figure. Noise performance of the LNA can be improved for a less stringent linearity requirement. The amplifier draws 10 mA from a 3.3 V supply.

Comparison with other published data are presented in Table 1. The SiGe LNA implemented in this work excels in terms of gain flatness over bandwidth of operation and linearity performance. The noise figure is slightly higher than some of the other designs, but that is due to its inherent trade-off with linearity. It should be noted that this LNA does not require any external component to function. In contrast, [27] requires an external RF choke and thus the present design enjoys an advantage in

Table 1: Performance summary and comparison with other published wideband LNAs

	BW (GHz)	S_{21} (dB)	Gain var. (dB)	NF (dB) (3-10 GHz)	NF (dB)	IIP3 (dBm)	P1dB (dBm)	Power (mW)	Die Size (mm^2)	Technology
This work	3–26	9	< 1	< 4.5	< 6.5	5.8	-5.6	33	0.48	120-nm SiGe BiCMOS
[28]	0.1–14	10.9	3	2.7–3.5	2.7–3.7	-3.8	–	14.4	0.031	130-nm CMOS
[29]	0.1–20	11.2	3	–	3.3–5.5	-2.5	–	20.4	0.35	90-nm CMOS
[27]	1.6–28	9.6	2.2	2.92–3.23	2.92–4.4	4	-9	21.6	0.139	90-nm CMOS
[30]	1.2–11.9	8.73	1.94	4.5–5.1	–	-6.2	–	20	0.59	180-nm CMOS
[31]	0–22.1	9.2	3	–	4.3–6.6 (0.5-15 GHz)	-2.67	–	8.4	0.131	90-nm CMOS
[32]	1–25	11.5	3	–	3.5–4.5	15.5	4.5	900	1.44	200-nm GaN HEMT
[25]	3–10	20	1	3.05–4.5	–	-11.7	–	42.5	0.52	200-nm SiGe BiCMOS
[33]	3–20	19.1	5	–	4.2–5.2 (8-18 GHz)	-6	–	116	0.09	180-nm SiGe

terms of die area, noise figure and gain. It can be inferred that overall performance of this wideband SiGe LNA is competitive with other state-of-the-art designs, in CMOS or III-V platforms, some of which are implemented in more aggressive technology nodes.

2.4 Summary

Analysis and design of a wideband SiGe low-noise amplifier (LNA) was presented. It was shown that by adding small inductors into the scheme of resistive-feedback amplifier design, matching can be greatly improved. The effects of a π-matching network at the input of the LNA on matching, gain, and noise performance were

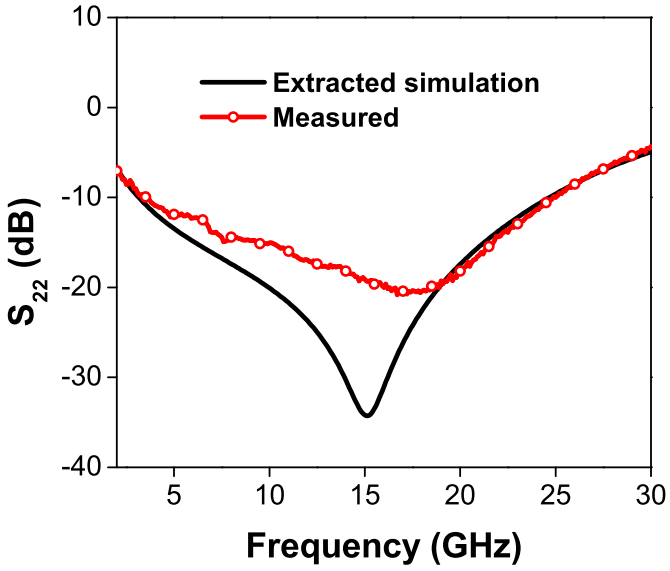


Figure 18: Output matching (S_{22}) across frequency of the wideband SiGe LNA: comparison of measured and parasitic-extracted simulation results.

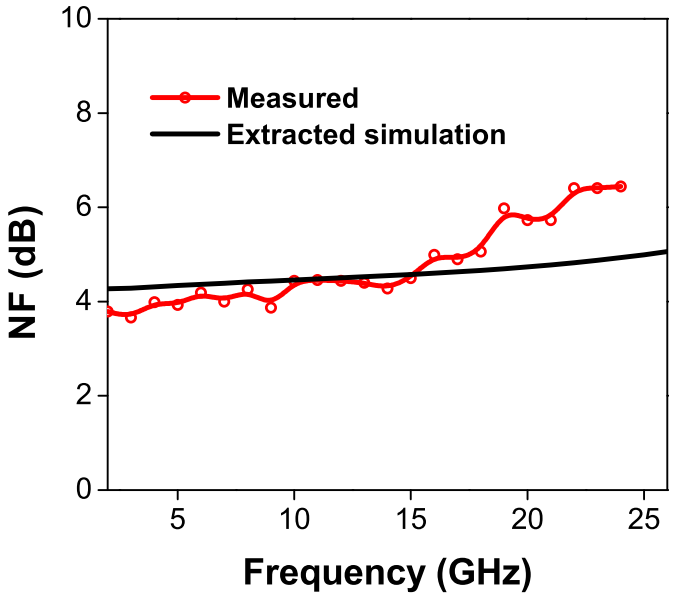


Figure 19: Noise figure vs. frequency: comparison of measured and parasitic-extracted simulation results.

analyzed theoretically. The design approach of combining reactive matching with resistive feedback improves performance as compared to a traditional shunt-shunt resistive-feedback amplifier, at the cost of slightly increased die area.

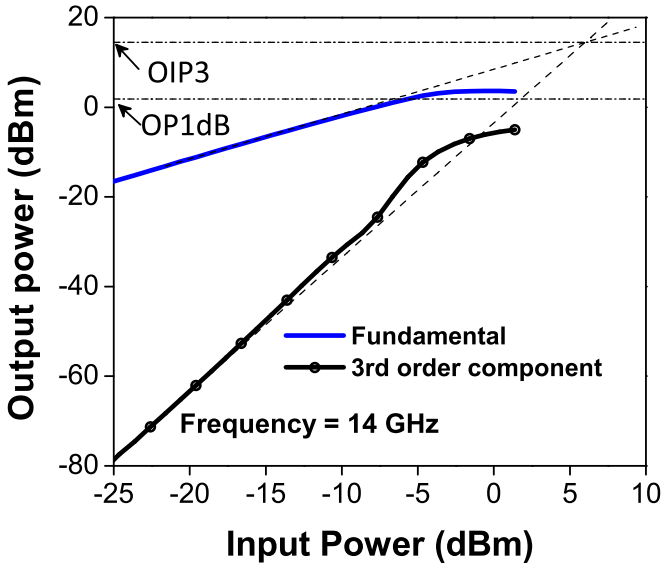


Figure 20: Output power vs. input power for fundamental and 3rd order components showing OIP3 and OP1dB.

CHAPTER III

ADAPTIVE IMAGE-REJECT MIXER

A wideband (6-20 GHz) SiGe adaptive image-reject mixer with an intermediate-frequency (IF) around 1.8 GHz was designed and fabricated in a 200-nm SiGe BiCMOS process with a peak f_T of 150 GHz. The mixer can be automatically healed to deliver consistent performance by nullifying the effects of process variations, environmental changes, and aging. The mixer can also be adapted to different specifications.

The image-rejection ratio (IRR) of quadrature-downconversion based mixer architectures may degrade significantly in the presence of scaling-induced process variations [34]. Complex image-reject architectures are used to reduce sensitivity to process variation at the cost of increased die area and power consumption. Even with the use of complicated architectures, IRR degradation due to mismatch remain a problem [35]. The designed image-reject (IR) mixer corrects for amplitude imbalances in the I and Q paths and consistently delivers high IRR. In addition to that, other key mixer parameters, such as conversion gain and linearity, can also be tuned to meet particular performance requirements.

The self-healing mixer, in its envisioned final form, should be a monolithic entity which can heal itself without any external intervention. In section 3.1, the design of the mixer and results of the healing experiment with external signal sources are described. In the next step, the mixer was integrated with on-chip amplitude locked loops (ALL) and DACs. The ALLs provide test signal sources and the DACs enable digital control. The detailed description and results are in section 3.2. In the final part (section 3.3), a monte-carlo simulation based method to verify effectiveness of healing is described.

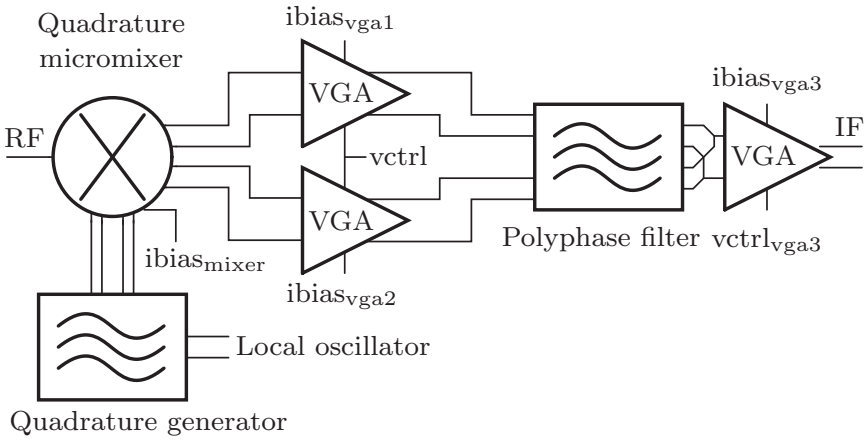


Figure 21: Block diagram of the image-reject mixer. The voltage and current biases are used as control elements to tune different performance metrics.

3.1 Healing using External Sources

3.1.1 System Architecture

A block diagram of the IR mixer is shown in Figure 21. The mixer consists of a quadrature-downconversion stage, two variable gain amplifiers (VGAs) in the in-phase and quadrature (I and Q) paths, a two-stage polyphase filter for image rejection, a three-stage polyphase filter for quadrature signal generation, and another VGA at the output. The overall mixer can be described as a variation of the Hartley architecture using passive *RC* polyphase filters to provide the required phase shift and subsequent summation for image rejection [36].

3.1.1.1 Quadrature Mixer

Quadrature down-conversion is accomplished by a micromixer (Fig. 22), which was chosen for its superior linearity and inherent wideband input matching capability [37]. The input is matched to 50 Ω using a parallel combination of resistor R1 in series with the $1/g_m$ impedance of the Q1 and the impedance looking into diode-connected Q4, which is degenerated by the resistor R2. The class-AB input stage consisting of Q2-Q4 provides excellent linearity, even under large signal condition. Individual currents out of the transistors Q2 and Q4 are nonlinear, but their combination remain linear [37] for

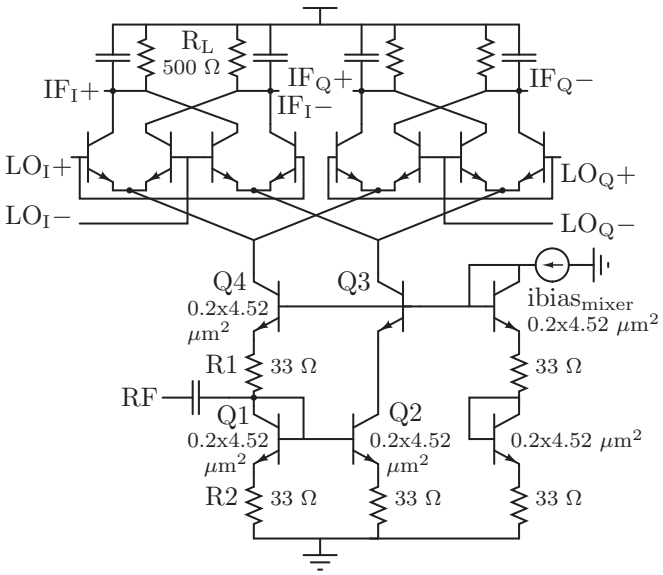


Figure 22: Schematic of the quadrature micromixer.

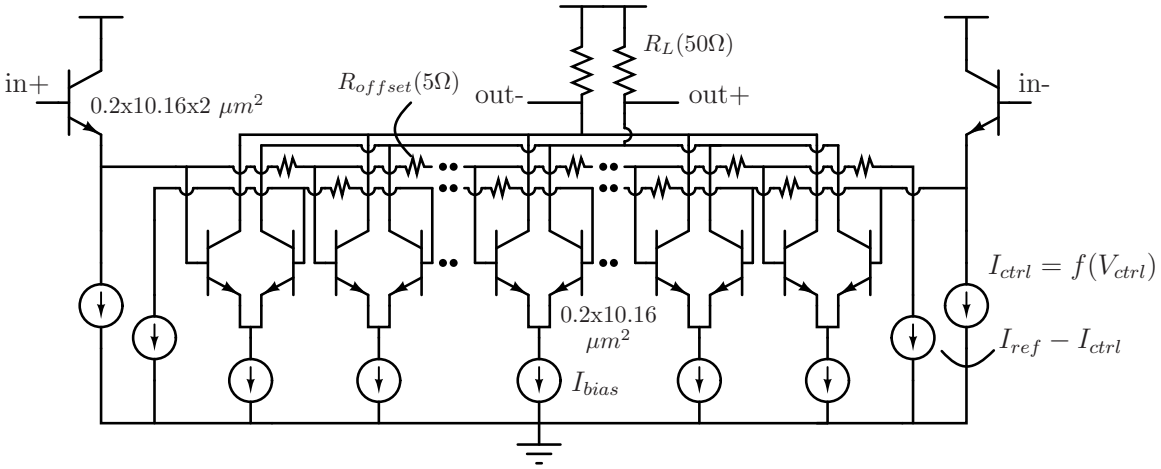


Figure 23: Schematic of the multi-tanh VGA circuit with 'elastic' g_m.

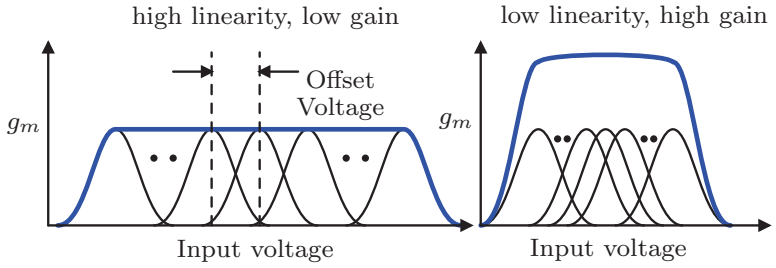


Figure 24: 'Elastic transconductance' of the multi-tanh VGA. The bold curves show the overall transconductance (G_m), which is the superposition of the individual transconductances (g_m). By changing the offset voltage between the individual g_m characteristics, linearity can be traded off for gain and vice-versa.

a wide range of input signal amplitude. Transistor Q3 is added to improve symmetry and balance. The input RF stage is shared between the I and Q paths. Common input transistors have an important advantage from a noise perspective. Noise generated by these transistors in the image frequency band are correlated in the I and Q paths and are canceled along with the image at the IF output. The resulting noise figure can be about 3 dB lower compared to the case when the noise is not correlated.

The wide bandwidth of the mixer can be attributed to two things:

- The down-converter (micromixer) does not use any resonant LC circuit.
- The input matching is implemented by means of a resistance in series with 1/gm of the HBTs.

This wideband nature is a typical characteristic of micromixers that do not use inductors, and comes at the cost of a relatively high noise figure. Small devices (Q1-Q4 in Fig. 22) were used to reduce the device capacitances and extend bandwidth. The use of small devices with high base resistance also adds to the noise figure of the mixer.

3.1.1.2 VGA

The VGAs in the I and Q paths serve the dual purpose of increasing the overall gain and canceling out I-Q imbalances by introducing gain offset. A multi-tanh, 'elastic' g_m based topology [38, 39] was chosen because of the flexibility it offers in terms of controlling gain and linearity. Each VGA consists of 13 differential pairs arranged in parallel (Fig. 23), with two emitter-followers driving their inputs. The overall transconductance (G_m), which results from the superposition of individual g_m's of the differential pairs, is linear over a wider range of input voltage swing. Voltage offsets between individual g_m's is the voltage drop across R_{offset}. These offsets can be varied continuously by changing a control voltage (V_{ctrl}) and thus changing shape of G_m (Fig. 24). R_{offset} and the bias current were chosen to allow offset variation from 0 to 50 mV, which corresponds to high gain and high linearity modes, respectively.

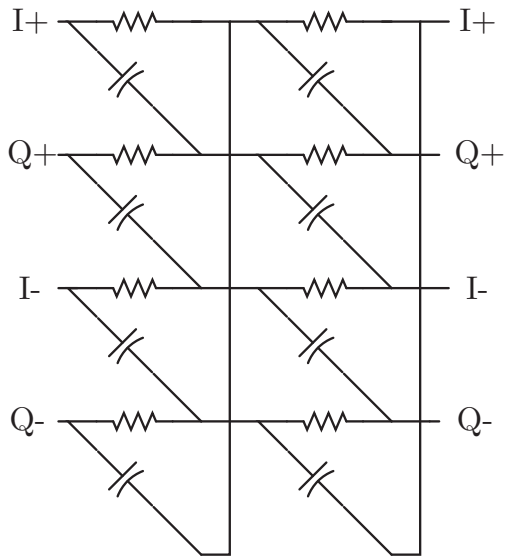


Figure 25: 2-stage complex polyphase filter for image rejection.

Changing the control voltage allows a direct trade-off between gain and input $P1dB$. The VGA's gain can also be varied by changing the tail current of the differential pairs independent of the control voltage.

The VGA at the output acts as a buffer between the image reject polyphase filter and output load. The linearity of this VGA dictates the overall linearity of the complete system. In addition, it also provides an additional degree of freedom for controlling the mixer gain. The load resistance of the VGAs were chosen to be 50 Ω so that the output is matched to differential 100 ohm load.

To avoid unwanted oscillations due to capacitive loading of the emitter-followers, a shunt R-C network (R_S-C_S in Fig. 23) was added to the input. The pole frequency was chosen such that it provides high impedance at the intended operating frequency, and thus does not have significant impact on normal operation. At higher frequencies, however, the shunt resistance compensates for any negative resistance seen at the base, thereby stabilizing the circuit.

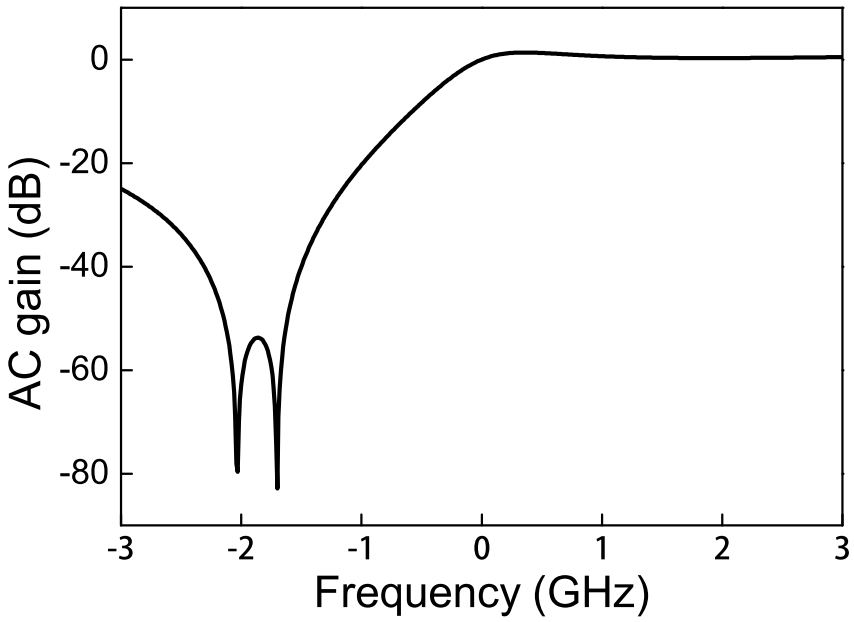


Figure 26: Simulated frequency response of a two-stage complex polyphase filter. The filter pases through positive frequency components while canceling out the negative frequencies where the image is downconverted.

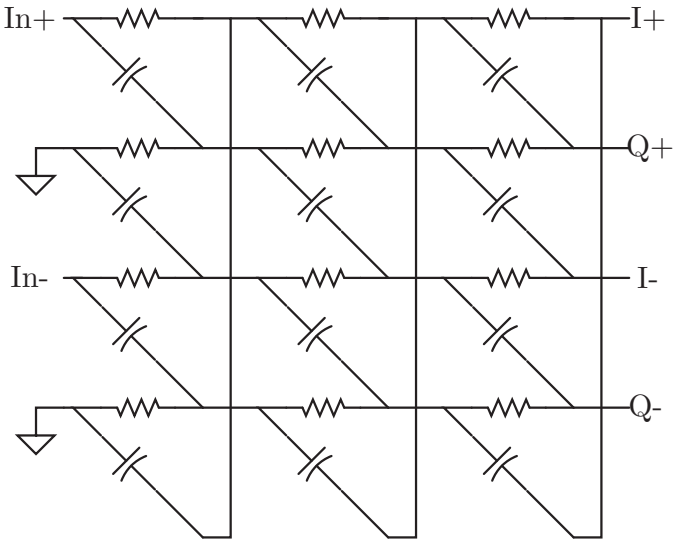


Figure 27: 3-stage complex polyphase filter for quadrature LO generation.

3.1.1.3 Polyphase Filters

The image rejection at IF is provided by a passive *RC* polyphase filter (Fig. 25). Such filters are symmetric (structurally) and can be cascaded to improve IRR over a wider bandwidth. However, cascading a large number of stages can introduce significant

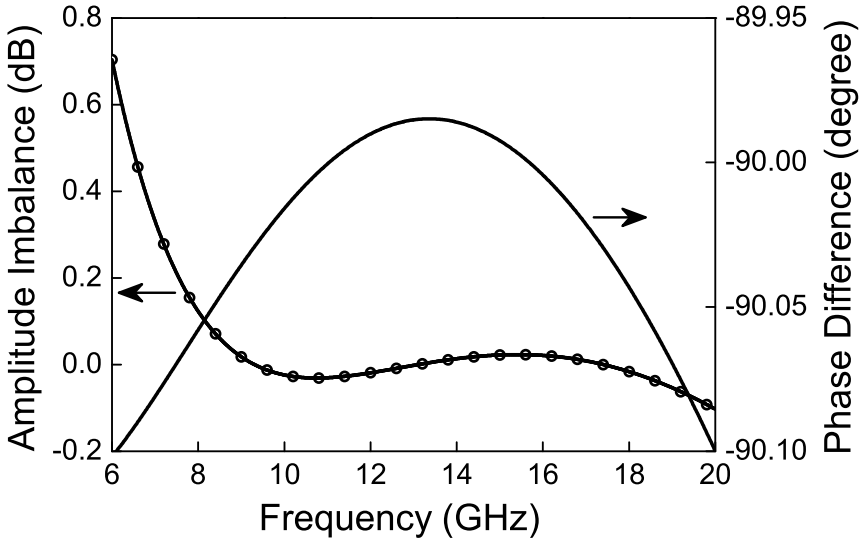


Figure 28: Simulated amplitude and phase error of the quadrature generator based on a three-stage passive polyphase filter.

loss in the signal path, requiring additional amplification stages [40]. A two-stage filter is used in the present implementation. Simulated frequency response of the two-stage polyphase filter is shown in Fig. 26. The filter can differentiate between positive and negative frequencies. In other words, the filter can distinguish between relative phase sequence of the I-Q signals, and hence can be used to pass through down-converted RF signal but cancel the image component.

When driven with differential inputs the polyphase filter works as a quadrature generator [36]. In this implementation, a three stage filter was used. The pole frequencies were chosen so that the phase and amplitude imbalance at the output is minimal over 6 - 20 GHz. For more details regarding polyphase filter design, please refer to [36].

3.1.2 Performance Tuning

This mixer, through the action of its various tuning elements, enables real-time adjustment of its key performance parameters (IRR, conversion gain, and OP1dB). The control elements that we have at our disposal include the current biases and control

voltages of the VGAs ($ibias_{VGA1}$, $ibias_{VGA2}$, $ibias_{VGA3}$, $vctrl$ and $vctrl_{VGA3}$). VGA1 and VGA2 are in the I and Q paths (Fig. 21) and VGA3 is at the output. It has been assumed that the optimum value of LO power is being used. The mixer bias current ($ibias_{mixer}$) has minimal effect on gain or linearity and can rather be governed by noise figure considerations, which is outside the scope of our present discussion. Notable effects and trade-offs are discussed below.

3.1.2.1 Image Rejection

Image rejection depends on the gain and the phase imbalance between the I and Q paths. Phase imbalance can be present in a system due to imperfections in either the quadrature generator or the image reject polyphase filter. Phase accuracies of the polyphase filters depend on relative matching of component values ($< 1\%$ mismatch) and should be minimal under the assumption that the component values are tracking together.

Gain mismatch is attributed to device mismatches in the I and Q paths and shift in R-C pole frequencies of the polyphase filter, which depends on poorly-controlled absolute component values. By introducing a difference between the bias currents of VGA1 and VGA2 ($ibias_{VGA1}$-$ibias_{VGA2}$) and thereby gain offset between the two VGAs, amplitude imbalance can be eliminated and IRR can thus be improved.

3.1.2.2 Gain and linearity

All of the VGA current biases have a linear control over gain, as expected, but only the bias current of VGA3 ($ibias_{VGA3}$) affects the linearity significantly, as it is the last element in the chain and handles larger signals. The nominal value of $ibias_{VGA3}$ is 3 mA, and it can be increased to 4 mA, which corresponds to a gain improvement of about 2.5 dB. The control voltage, on the other hand, alters the shape of G_m by changing the offsets between the individual transconductances. In addition, $vctrl_{VGA3}$ can be used to control the trade-off between gain and linearity and $vctrl$ can be used

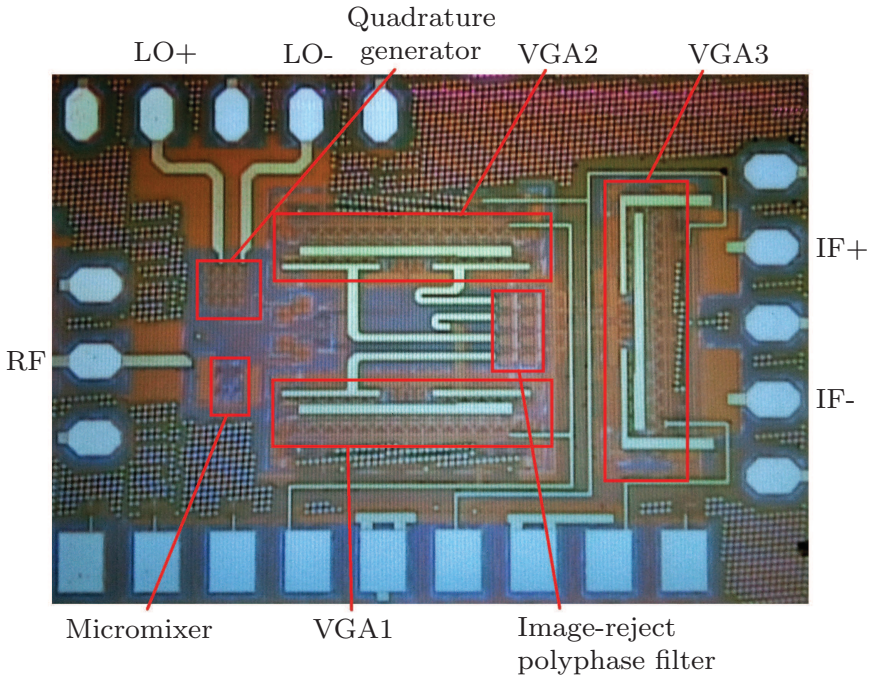


Figure 29: Die photograph of the image-reject mixer. The mixer was fabricated in a 200-nm SiGe BiCMOS process. The chip die area is 1.6 mm x 1.0 mm.

for additional control over gain.

3.1.3 Measurement results

This adaptive mixer was fabricated in a commercially-available, 200 nm, 150 GHz peak f_T SiGe BiCMOS platform. A photograph of the die is shown in Fig. 29. The die area is 1.6 x 1.0 mm^2 (including bondpads) and it consumes 215 mA from a 4.0 V supply rail under nominal settings. The conversion gain across 6-20 GHz is shown in Fig. 30. Gain variation across the entire band is less than 3 dB and it can be varied by more than 10 dB by changing *vctrl* alone. The total gain variation, when all controls are employed, is more than 25 dB.

Different metrics of the mixer can be changed in a variety of ways by different combinations of the control elements. The effects of two important control knobs are considered here. Fig. 31 shows how, in a typical case, IRR is affected by the difference between VGA1 and VGA2 current biases, when other control elements are at their

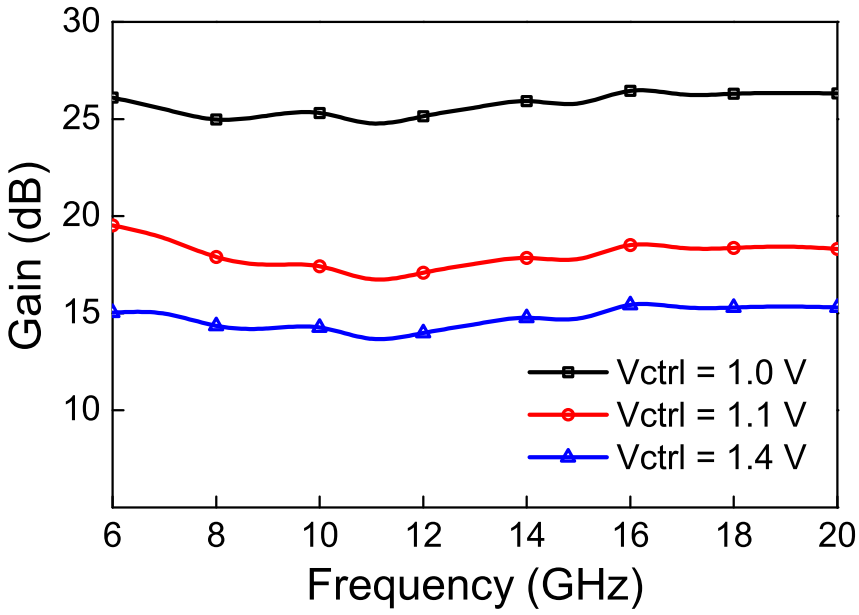


Figure 30: Measured mixer gain across frequency for different VGA control voltages. The gain is quite flat across the entire frequency band and it can be varied by changing the control voltage of the VGAs.

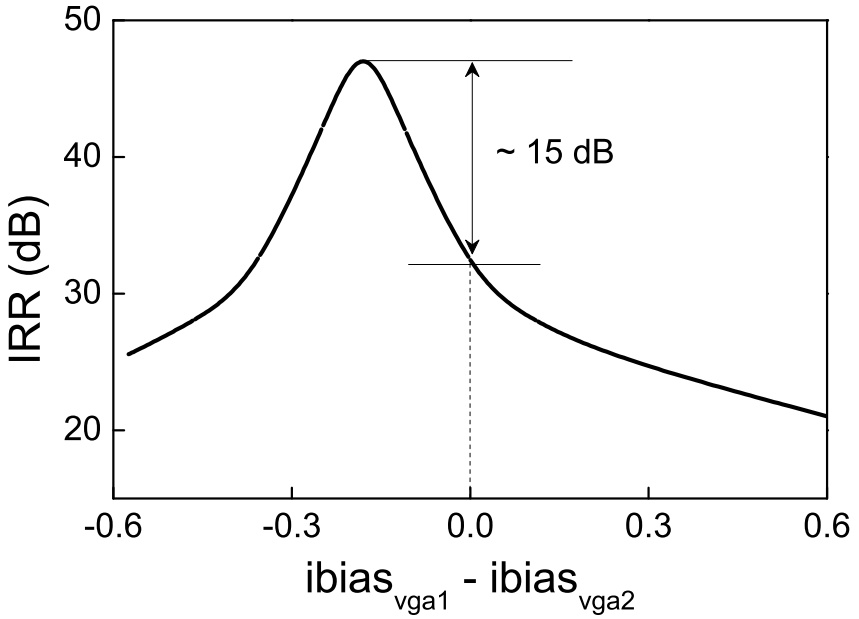


Figure 31: Image rejection ratio (IRR) variation with VGA current biases in a typical case. An improvement of 15 dB was obtained by canceling the gain imbalances in the I and Q paths by introducing offset between the VGA current biases.

nominal values (Table 3). Clearly, the optimum point for best IRR has been shifted from its nominal position and an improvement of about 15 dB can be obtained by

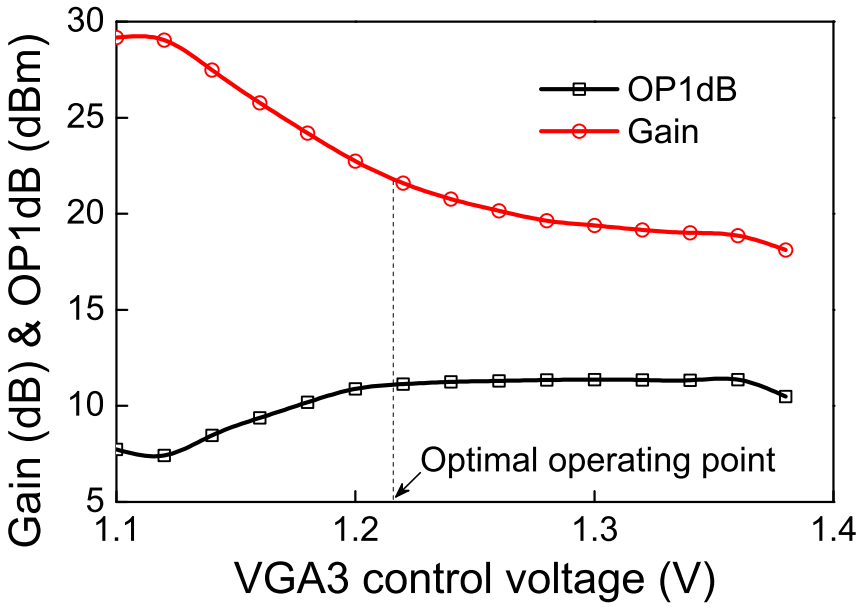


Figure 32: Dependence of gain and 1-dB compression point (OP1dB) on control voltage of VGA3 ($vctrl_{VGA3}$).

changing $ibias_{VGA1}$ and $ibias_{VGA2}$.

The dependence of gain and OP1dB on $vctrl_{VGA3}$ is plotted in Fig. 32. The optimum point of operation is a little less clear in this case. One reasonable definition can be taken as the point where OP1dB saturates, since this gives the best combination of gain and OP1dB. This is again susceptible to process variation, as it depends on R_{offset}, and $vctrl_{VGA3}$ can be changed to restore optimal operation.

The nominal performance of the mixer along with other published works is shown in Table 2. As compared to the other works, the mixer presented here performs well over a much wider range of input frequency and has a relatively higher IF bandwidth but consumes more power.

The noise figure of the mixer is relatively high, primarily due to the wideband nature of the mixer. The absence of reactive matching, use of input matching resistor and small devices (with high base resistance) in the micromixer contribute to a higher noise figure. Primary focus of the work was on conversion gain, linearity and image rejection of the mixer and a little bit of noise performance was traded off for wideband

Table 2: Performance Summary and Comparison with other Published Image-Reject Mixers

	RF (GHz)	IF	Gain (dB)	NF (dB)	IRR (dB)	IIP3 (dBm)	OP1dB (dBm)	Power	Technology
This work	6–20	1.8 GHz	15	14-16*	30	3	10	215mA @ 4V	180 nm SiGe BiCMOS
[17]	2.1	100 KHz	1.4	13.9	20	5.5	–	42.6 mW	50 GHz SiGe
[41]	17.2	75 MHz	13.9	7.4	74 (max)	-4.7	–	63 mW	180 nm SiGe BiCMOS
[42]	1.2	44 MHz	26.2	4.1-5.6	31.3	5.7	–	119mA @ 3.3V	0.35 μm SOI BiCMOS
[43]	5-6 9.8-11.8	3 GHz	5-12	8.7-10.9	NA	–	-5	68 mW	0.13 μm CMOS
[44]	20-32	12 GHz	3	10.5-13	NA	0.5-2.6	–	18 mW	0.18 μm BiCMOS

* Simulated with extracted parasitic

operation. Still, a noise figure of 14-16 dB across 6-20 GHz is certainly useful for receivers that do not have stringent noise requirements.

The mixer burns quite a bit of power to achieve high linearity at an IF of 1.8 GHz. A OP1dB of 10 dBm, while driving 100 Ω differential load at 1.8 GHz, is considerably higher as compared to the other published data in Table 2. The property of image rejection and having I-Q paths also contribute to power consumption substantially.

3.1.4 Automated healing in measurement

This SiGe mixer was put into an automated healing loop to demonstrate its full adaptive capabilities. The setup is shown in Fig. 33. External signal sources were used to provide RF and LO signals, and a spectrum analyzer was used to measure the output of the mixer. All of the instruments, including the DC supplies, were connected using GPIB and controlled through a MATLAB program running on a computer. The program measures IRR, gain and gain compression and based on that measurement changes the biases autonomously to achieve the desired mixer specifications. Measurement of gain involves feeding in an RF signal of known amplitude,

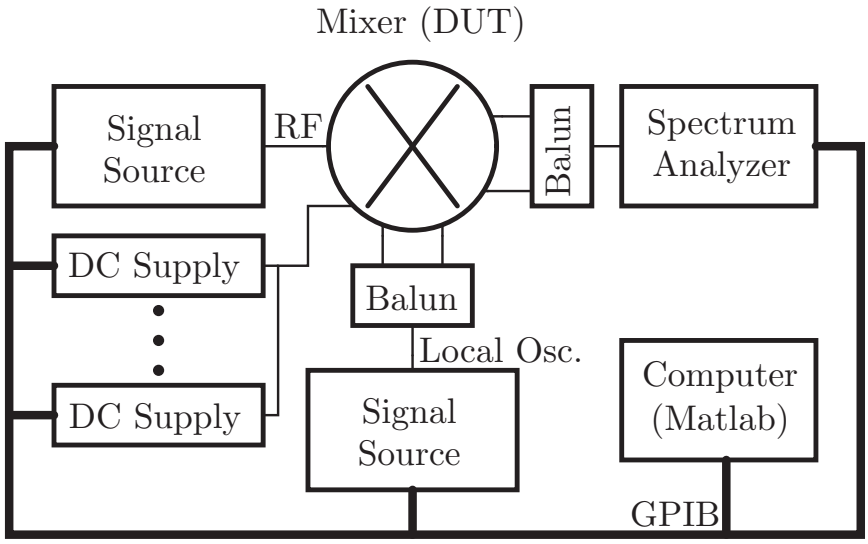


Figure 33: Automated healing setup. All the instruments are connected using a GPIB interface. A Matlab program running on the computer iteratively measures performance and tunes bias values to adapt the performance of the mixer.

which should be low enough so that the mixer not driven into saturation, and measuring the corresponding IF power at the output using the spectrum analyzer. To measure IRR, the input signal frequency is changed to the image frequency and gain corresponding to the image is measured. The ratio of gain numbers corresponding to RF and image signals gives IRR. Measuring the output referred 1-dB compression point requires a power sweep of the input RF source. Instead of measuring the exact 1-dB compression point, gain compression at an output power level of 10 dBm was measured to reduce the number of required iterations. The compression point test was performed as follows:

1. Set input power (P_{in}) to ($OP1dB_{goal} - gain$) to start with.

2. Measure output power (P_{out}).

3. Calculate gain compression ($gain_{comp} = gain - (P_{out} - P_{in})$.

4. Update input power to ($P_{IN} + OP1dB_{goal} - P_{out} + \epsilon$), where ϵ is a small number which cntrols the tradeoff between number of iterations and accuracy of the

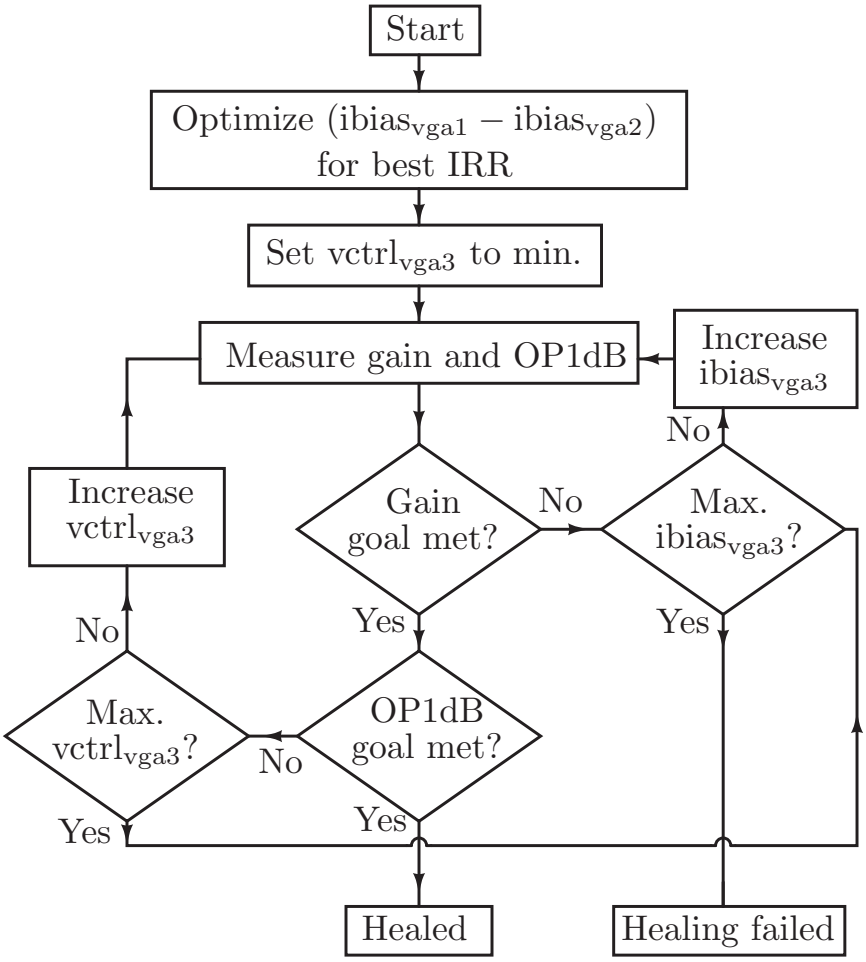


Figure 34: Steps of the algorithm used in the automated healing procedure. IRR is healed first as it is independent of the rest of the parameters, and then the iterative loop measures gain and compression, and sets the biases accordingly.

measurement. Smaller the value of ϵ smaller will be the error between the final output power and the target OP1dB, but a larger number of iterations will be required. In our measurements, a value of 0.1 was used.

5. Carry out steps 2 - 4 until $P_{out} > OP1dB_{goal}$.

Using this method reduces the number of iterations required to find out if the DUT is meeting target specification for gain compression as compared to a linear power sweep.

The steps of the healing algorithm is outlined in Fig. 34. IRR is optimized first, since it can be done independent of the other two parameters of interest. The goal

is to find out the optimum offset between the VGA bias currents that maximizes IRR (Fig.31). This is done by measuring the IRR at the end point of the interval of interest and bisecting the interval iteratively based on those measurements. The algorithm can be detailed as:

1. Measure IRR at the extreme points of the search interval. Say, IRR_{left} corresponds to maximum $ibias_{vga1}$ and minimum $ibias_{vga2}$, and IRR_{right} corresponds to the opposite, i.e., minimum $ibias_{vga1}$ and maximum $ibias_{vga2}$.

2. If IRR_{left} is larger than IRR_{right}, then the peak lies in the left half portion of the search interval and vice versa. The end points of the search interval is then modified accordingly.

3. Steps 1 - 2 are performed repeatedly until the search interval shrinks down to the desired accuracy level.

The IRR curve falls monotonically at the same rate on both sides of the peak. It is the nature of the IRR curve that allows us to do the search in this fashion, which is much more efficient than sweeping linearly across the whole interval.

After IRR optimization is done, the routine then proceeds to find the optimum values of $vctrl_{vga3}$ and $ibias_{vga3}$, which meets the linearity requirement with highest possible gain. The goal of the algorithm is to find an operating point which just about meets the linearity specification with as much gain left in the system as possible. The algorithm starts from the minimum value for $vctrl_{vga3}$, which corresponds to maximum gain and minimum linearity, and increase it from there. If any point during that procedure the gain falls below the specification, $ibias_{vga3}$ is increased to boost the gain. Power consumption is increased only if bias current of the VGA3 is increased during the routine and even then it goes up only by as much as needed to meet the desired specifications.

Table 3: Values of control elements

	Min.	Nom.	Max.
$ibias_{vga1,2}$ (mA)	2.5	3	3.5
$ibias_{vga3}$ (mA)	3	3	4
$vctrl_{vga3}$ (V)	1.1	1.25	1.4

Table 4: Simulation results of the mixer at nominal settings in different process corners

	Fast	Nominal	Slow
Gain (dB)	16.32	18.99	18.7
OP1dB (dBm)	9.74	10.02	9.84
IRR (dB)	24.6	44.3	30.8

Table 5: Target Specifications

IRR (dB)	Gain (dB)	OP1dB (dBm)
30	15	10

Table 6: Measured performance of the mixer before and after healing for 5 different dies

	Nominal			Healed		
Die #	IRR (dB)	Gain (dB)	Comp. (dB)	IRR (dB)	Gain (dB)	Comp. (dB)
1	31.3	15.9	0.74	45.6	15.8	0.76
2	24.8	13.9	1.86	34.2	15.1	0.85
3	31.8	18.3	0.75	44.6	18.0	0.64
4	26.7	16.1	0.90	38.2	16.1	0.82
5	38.4	17.7	2.02	42.1	17.4	0.78
Mean	30.6	16.38	1.25	40.94	16.48	0.77
Std. dev.	4.72	1.54	0.57	4.23	1.06	0.07

The range of control biases and their nominal values are given in Table 3. Simulated performance of the mixer in different process corners under nominal bias settings is shown in Table 4. The simulations were carried out with RC-extracted parasitic values. Measured conversion gain of the mixer, as shown in Table 6 was consistently

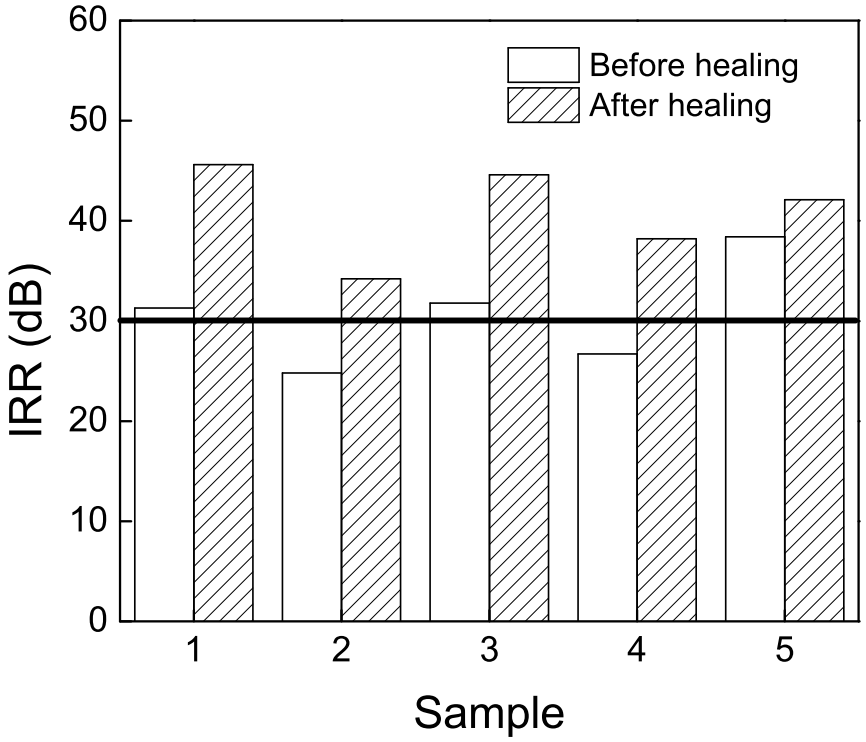


Figure 35: Measured IRR of the mixer before and after healing for 5 different mixer die.

quite a bit lower than the simulated values. In fact, in most cases, the measured values of the gain before healing fell outside the range of corner simulations. This discrepancy between simulated and measured data can be due to parasitic effects that were not accounted for in simulation, like parasitic inductance or imperfections of the measurement setup, like imperfect LO drive. Due to these factors, the healing procedure was not able to achieve nominal simulated performance of the mixer. Instead, the target specifications of the healing procedure were slightly altered. The target specifications for this demonstration are shown in Table 5. The goal was to show that the healing algorithm is effective in reducing the effects of process variation in measurement.

The results of the self-healing procedure using this approach for 5 different die are tabulated in Table 6 and also plotted in Fig. 35-37. In all cases, the healed mixer met all required specifications and are significantly better than the nominal measured

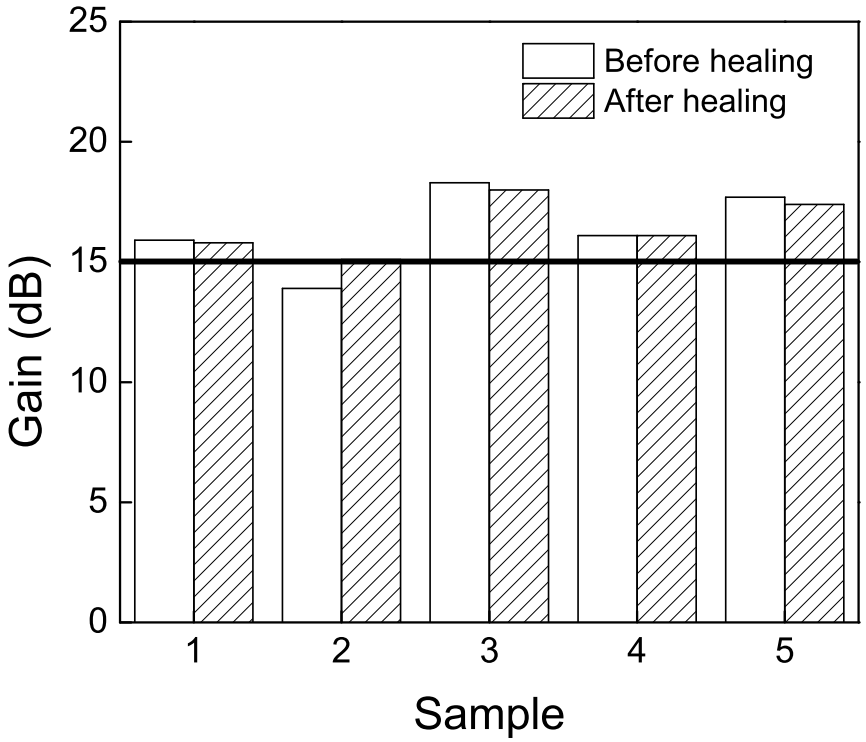


Figure 36: Measured gain of the mixer before and after healing for 5 different mixer die.

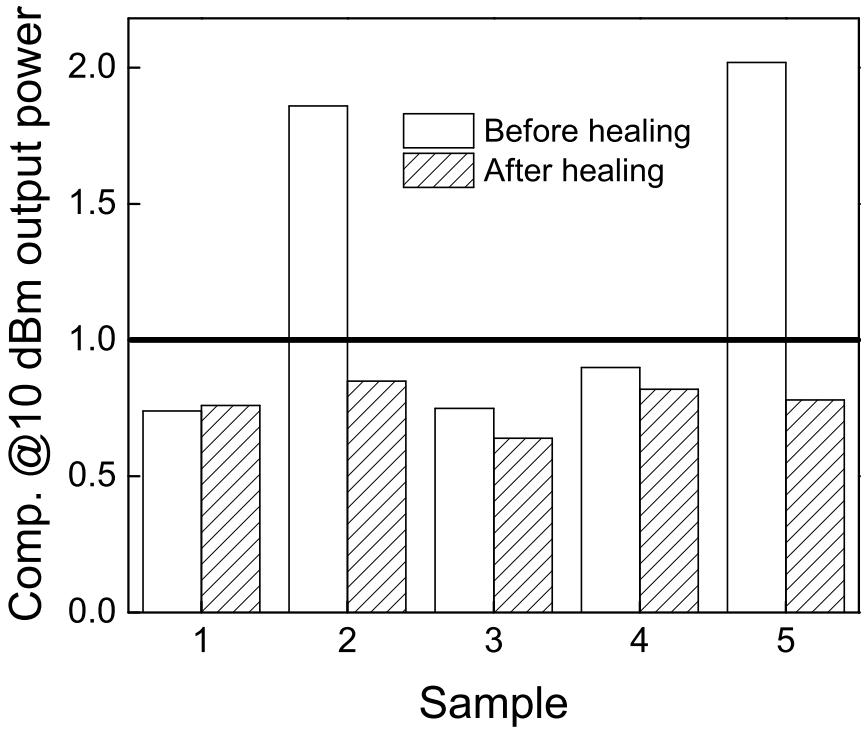


Figure 37: Measured OP1dB of the mixer before and after healing for 5 different mixer die.

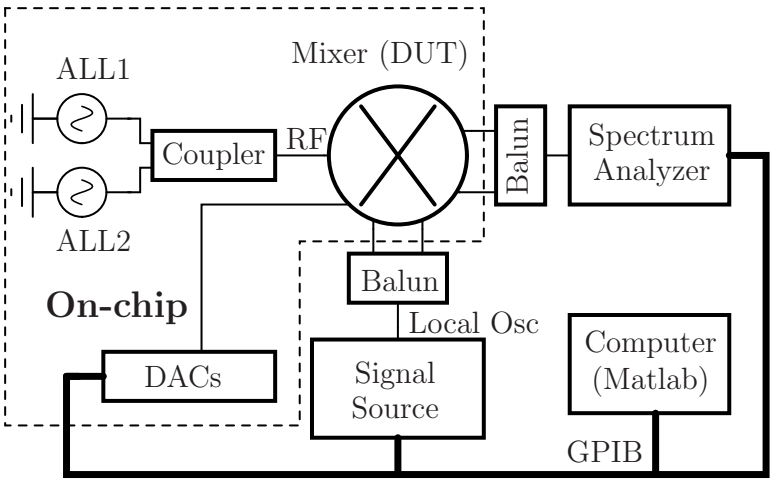


Figure 38: Healing setup of the image-reject mixer using ALLs and DACs.

performance. Table 6 also shows the mean and variance of IRR, gain and OP1dB before and after healing. Clearly, die to die variation is reduced significantly after healing.

Depending on the goal of the optimization process, the algorithm can be modified in various ways and made more sophisticated. Average execution time for this particular healing routine was around 25 seconds. The time to execute the code is largely limited by the GPIB requirements. The code will execute much faster when running on an on-chip processor. It should be noted that success of this simple algorithm is largely due to the fact that the circuit allows relatively independent control of the metrics IRR, gain and OP1dB.

3.2 Integration of signal sources and digital control on-chip

The final vision of the idea of "self-healing" is to be able to perform the healing without any intervention from outside the chip. In the next iteration of the chip, test signal sources and DACs were integrated on-chip. The healing setup is shown in Figure 38. Two amplitude locked loops (ALLs) were integrated on-chip to provide test signals for healing and DACs were used to control the mixer digitally. The ALLs and DACs were designed by others as part of a larger project. At the heart of the

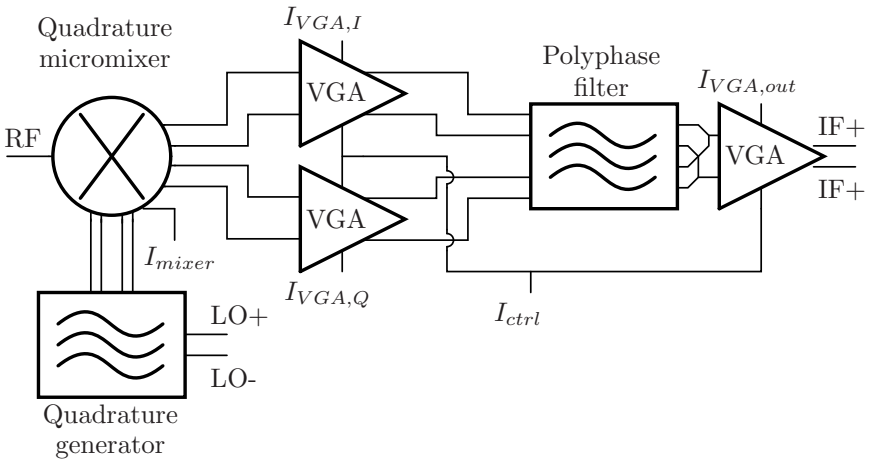


Figure 39: Block diagram of the revised Image-reject mixer.

ALL there is a voltage controlled oscillator. Since phase noise requirement of the test signals were not very stringent, a ring oscillator was chosen to keep the area overhead to a minimum. The amplitude locking mechanism works by sensing the output amplitude using a peak detector and then using that information to control a VGA in a feedback loop. The 8-bit DACs are serially connected and fed with a single bitstream. The bitstream was generated within the MATLAB code and fed to the DACs using a digital pattern generator.

The revised block diagram of the mixer is shown in Figure 39. The voltage controlling the shape of the transconductance (G_m) of the VGAs was replaced with a current based control (I_{ctrl}) to have more linear and precise variation of the VGA gain. One other important change was the measure of linearity for healing. Since the ALLs are designed to produce a fixed amplitude, it is easier to measure third-order intercept point (IP3) rather than sweeping power to measure compression point (P1dB). Two ALLs were used to generate two tones spaced about 100 MHz apart and those tones were combined using a resistive coupler and fed to the input of the mixer. The number of parallel g_m stages in the multi-tanh VGAs were reduced to 9 to save power consumption without hurting the small signal linearity performance.

A die photograph of the HEALICs (Heal ICs) receiver chain is shown in Fig. 40.

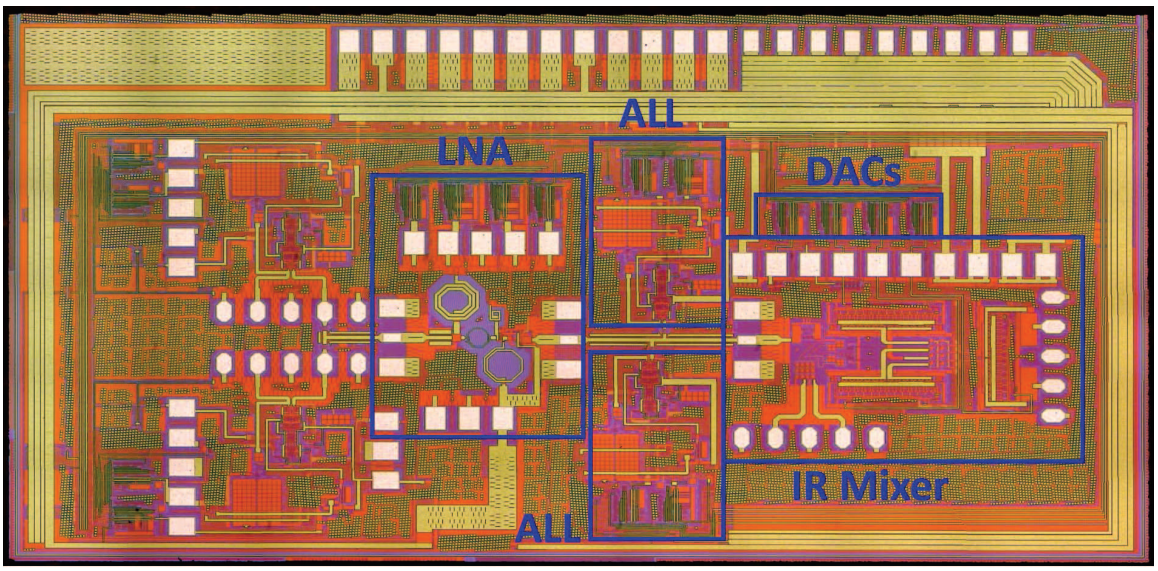


Figure 40: Die photograph of the mixer with other components of the HEALICs receiver chain.

Table 7: Healing performance of the IR mixer with ALLs and DACs

Parameters	Target	Pre-healing	Post-healing
Gain (dB)	23	18.6	23.1
IRR (dB)	40	26.2	37.1
OIP3 (dBm)	20	16.9	21.1
Power Consumption (mW)	$< 5\%$ increase	760	792

The output of the healing procedure for one die is tabulated in Table 7. Post-healing gain and OIP3 numbers meet required specifications. The IRR was improved as a result of healing, but it just fell short of the target (40 dB).

The gain and IRR variation with IF before and after healing is shown in Figure 41 and Figure 42 respectvely.

3.3 Monte-carlo Based Verification of Healing

In the preceding sections, self-healing capabilities of the IR mixer was demonstrated with measured data. However, there is one limitation of that approach. It is difficult

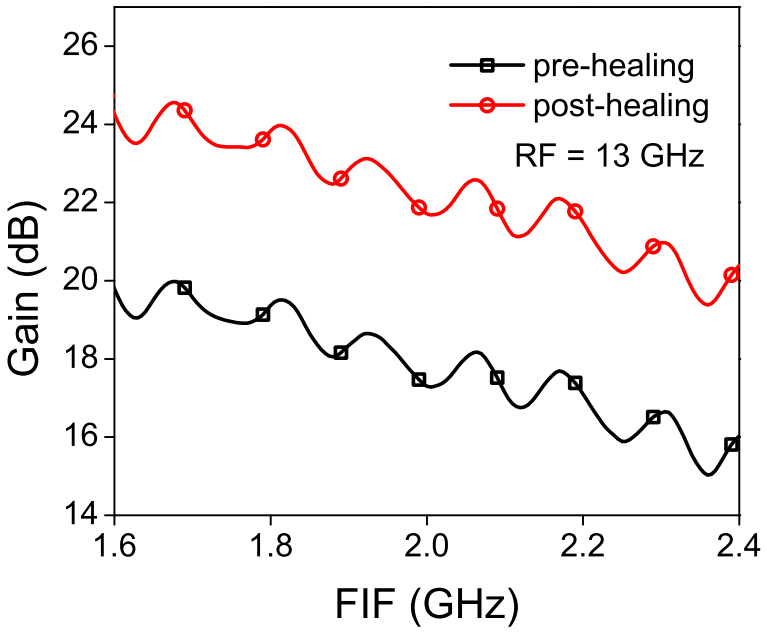


Figure 41: Gain vs. IF before and after healing using ALLs.

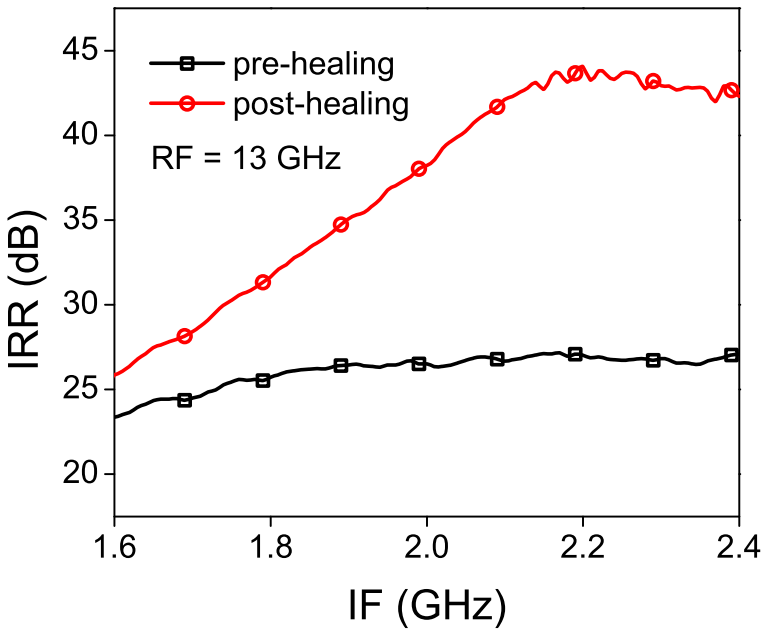


Figure 42: IRR vs. IF before and after healing using ALLs.

to measure a sufficiently large number of dies to obtain data that is statistically significant. Even measuring multiple dies from the same wafer is not sufficient because the in-wafer variations do not represent the full gamut of possible process variations. To really measure effectiveness of the self-healing procedure, a large number of dies spanning a large number of wafers need to characterized. That is prohibitively costly, both in terms of money and labor. To solve the problem, a monte-carlo simulation based approach was adopted.

Monte-carlo is used to simulate the effects of process variations and mismatch by running multiple simulations with randomly varying process, model, and component parameters. The variations are controlled by the probability distributions specified by the foundry. Larger the number of simulations, greater is the coverage of the variations. The sample size used in this work is 250, which is large enough to cover 3σ limits of the distributions. In this simulation-based healing procedure, the design variables defined for currents and voltages serve as the tuning knobs. For each combination of model and component parameters, generated by monte-carlo, simulations were run repeatedly with changing variable values. The variables were updated at each iteration according to the healing rules and the results obtained from the previous simulations. The iterations go on until either the results meet the specifications or the variables go out of their allowed range, in which case the best possible values are returned. This healing procedure was run on 250 monte-carlo simulations. The entire procedure was coded using Ocean and little bit of PERL.

3.3.1 Circuit improvements

The changes at the circuit level were mainly aimed at improving the IRR. In the previous versions of the design, which is described in the preceding sections, the IRR healing only involved compensating for gain imbalances in the I and Q paths. While that was sufficient to demonstrate the healing procedure, a better IRR requires phase

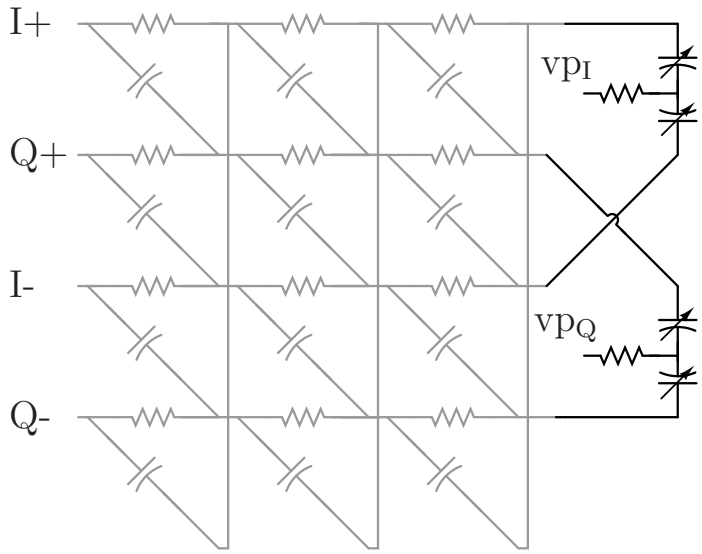


Figure 43: Schematic of the quadrature LO generator with varactors at the output.

compensation along with gain.

Phase compensation can be introduced either before or after downconversion. In this implementation, the LO inputs were chosen to introduce the compensating phase in the circuit. The primary advantage of choosing the LO input over IF for introducing phase tuning is the fact that the mixer gain is much less sensitive to LO amplitude variation as compared to that of the IF. Hence, even if some amplitude imbalance were introduced in the course of compensating the phase, that would not have a great effect on the gain imbalance; helping to decouple the tuning process of gain and phase.

Phase compensation was implemented by adding varactors at the output of the polyphase filter that generates the quadrature LO signals (Figure 43). The varactors are accumulation mode MOS devices. The size of each device is 12 μm x 0.36 μm. The difference between vp_I and vp_Q, referred to as vp_d from now on, controls the phase difference between the I and Q paths. As shown in Figure 44, by changing vp_d, the phase difference can be varied by ± 1 degree.

Changing the LO phase in this fashion also affects the LO amplitude and introduces gain imbalance in the circuit (Figure 44). The magnitude of that change is

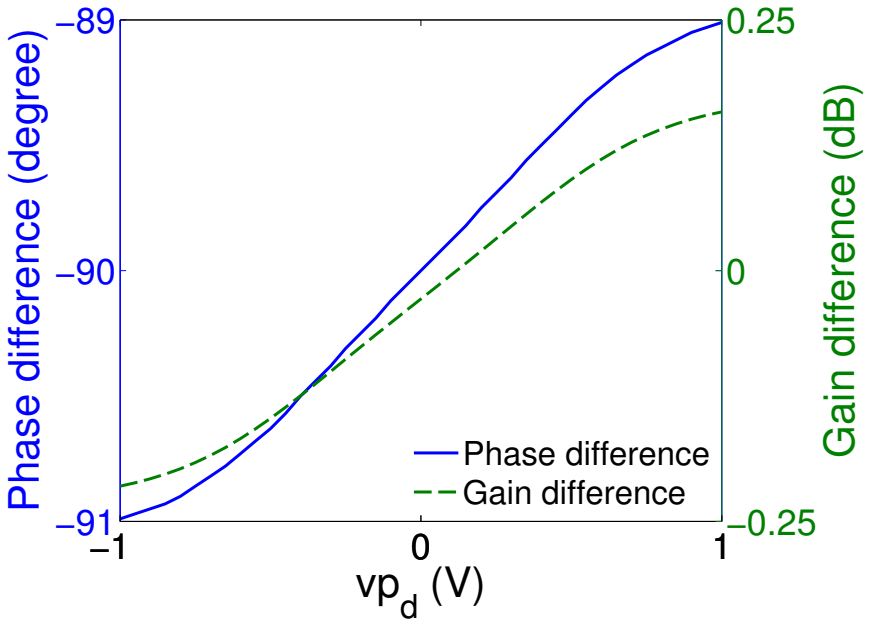


Figure 44: Phase tuning of I and Q LO signals using varactors: the difference between vp_I and vp_Q (vp_d) controls the phase difference between I and Q signals.

small; and despite the fact that the IF output is not very sensitive to the LO amplitude variation, it was found that the resulting gain imbalance was enough to have a significant effect on IRR. To solve this problem and decouple the tuning of gain and phase, two limiting amplifiers were added at the LO output. The limiting amplifiers provide a fixed amplitude at the output despite variations in the input amplitude. The limiting amplifier essentially consists of two differential amplifiers (Figure 45). The first stage is designed to have high gain so that its output drives the second stage into saturation. The outputs coming out of the second stage are shaped like square waves. The tail current and the load resistor of the second stage was chosen to set the differential output amplitude to about 360 mV peak-to-peak. The input and output waveforms for two different LO powers are shown in Figure 46. Clearly, the output amplitude is independent of small variations in the input amplitude. Any gain imbalance caused by an attempt to tune the phase does not propagate through the limiting amplifiers and hence allows independent tuning of gain and phase.

The limiting amplifiers also provide gain and reduces the LO power requirements

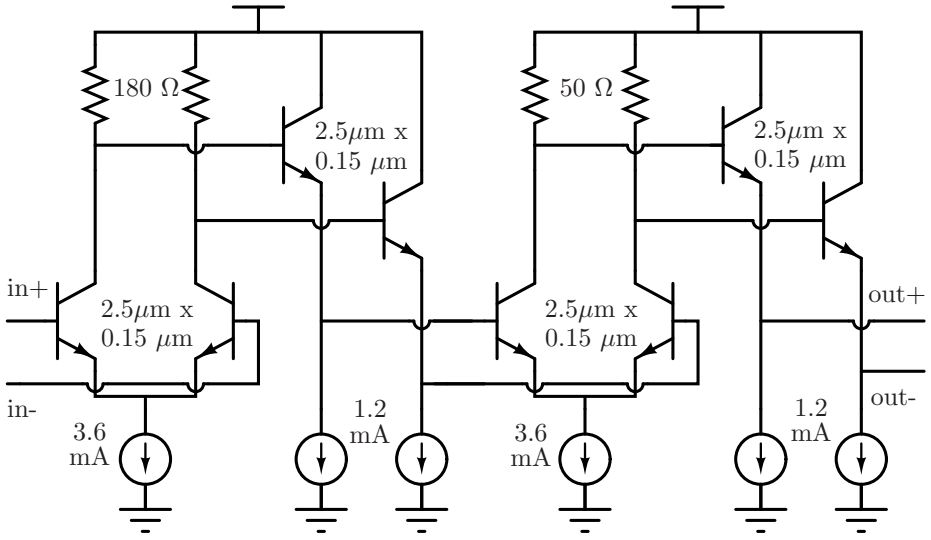


Figure 45: Schematic of the LO limiting amplifier.

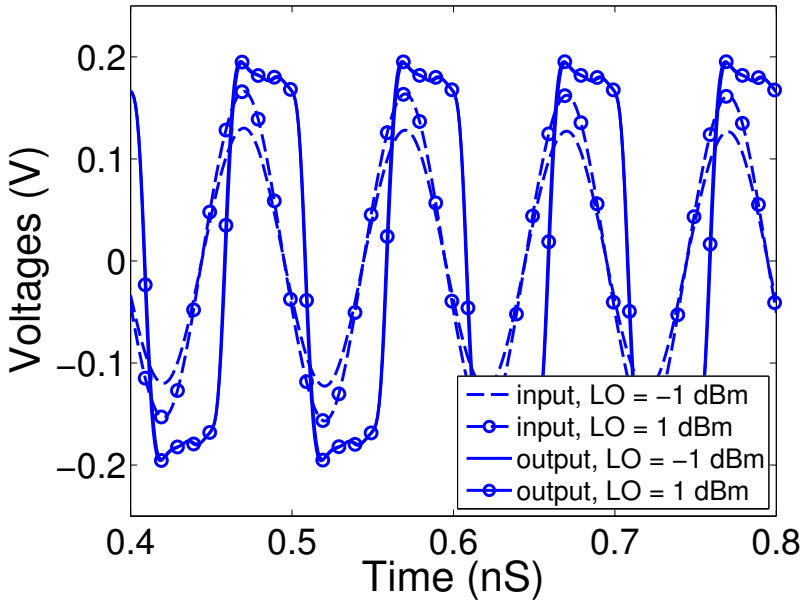


Figure 46: Transient waveforms in and out of the LO limiting amplifier. The variaiton in input amplitude, within a certain range, does not affect the output amplitude.

from off-chip sources. Only 0 dBm of external LO power is sufficient to drive the quadrature mixer throughout 6 to 20 GHz. The square waveform coming out of the limiting amplifiers, due to the sharp zero-crossing of the differential LO drive, also helps to reduce noise contributions of the switching transistors.

3.3.1.1 Compensating for component variations of the polyphase filter

One of the major sources of IRR degradation in this mixer if the RC pole shift of the polyphase filter at the IF. The absolute values of the components (R and C) can vary by as much as 20% and that results in a shift in the frequency at which image rejection takes place.

Traditional treatments of image reject architectures only talk about gain and phase imbalance and their compensation. But for circuits using polyphase filters with two or more stages, the point of origin of the imbalances also become important. As will be shown in the following discussion, the imbalances originating within the polyphase filter have unique characteristics and cannot be compensated for by either gain or phase tuning outside the filters.

In this discussion, it is assumed that the all the component values in the polyphase filter are well-matched and hence, their values track together. In other words, the secondary effects of mismatch in between the components of the filter are ignored.

The basic building block of the polyphase filter is one single RC network, as shown in Figure 47. The circuit is fed with two signals that are in quadrature. They are denoted as I and Q. The input signals are also named according to the frequency response they see looking into the RC network: the signal driving the RC branch is named S_{LP}, and the one driving the CR branch is named S_{HP}. This naming convention will be useful in the following discussion. The output can be thought of as the superposition of individual responses to S_{LP} and S_{HP}. It should be noted that for image cancellation to take place, S_{HP} should lead S_{LP} by 90°. In Figure 47, if the phase of S_{HP} was -90° instead of 90°, the I and Q signals would still be in quadrature. But, they would add at the output rather than canceling each other.

The phase difference between the low-pass (RC) and high-pass (CR) transfer functions remain 90° at all frequencies. But, the magnitude of the two transfer functions are equal only at the pole frequency ($f_p = 1/(2\pi\text{RC})$), and hence, image rejection is

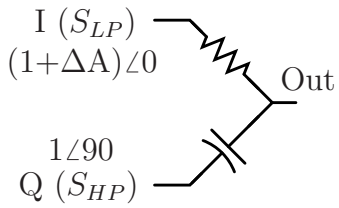


Figure 47: Bulding block of the polyphase filter: one single RC network.

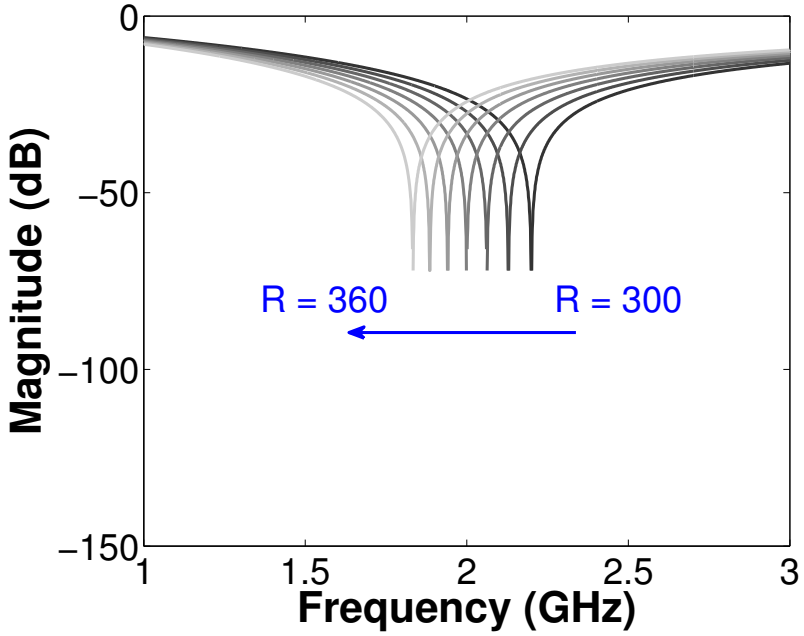


Figure 48: Magnitude response of the RC-CR combination with changing resistor value, simulating the effect of process variation.

only effective in a small bandwidth around f_p. The RC values were chosen to place f_p at 2 GHz.

The magnitude response of the RC-CR network, which is the gain of the image signal, is shown in Figure 48. Sweeping the resistor (R) simulates the effect of process variation. The change in the pole frequency (f_p) brings about a corresponding shift in the IRR response.

To analyze the effect of amplitude imbalance, an error term (ΔA) was applied to the low-pass input (S_{LP}). Figure 49 shows how the RC network responds to the applied amplitude imbalance. The amplitude imbalance can be represented graphically by moving the low-pass magnitude response up or down, depending on the sign

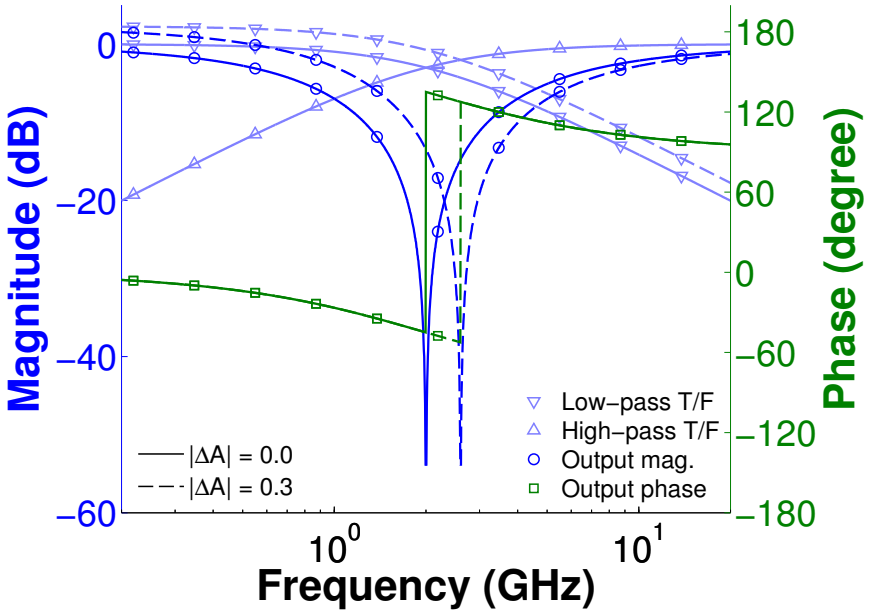


Figure 49: Magnitude and phase response of an RC section with varying gain imbalance.

of ΔA. Best image rejection is achieved at the frequency where the low-pass and high-pass magnitude responses meet. Consequently, moving the low-pass response up results in the notch in the combined magnitude response to shift to a higher frequency. Similarly, for a negative ΔA the notch shifts down in frequency. Another important property of this RC network is the fact that the output phase changes by 180° at the point where the low-pass and high-pass magnitude responses meet (f_{GZ}). The output phase follows the phase of the low-pass response before f_{GZ} and moves to the high-pass response after that.

Magnitude response of the RC network for varying ΔA is plotted in Figure 50. A comparison of Figure 48 and Figure 50 shows that changing ΔA (amplitude imbalance) and changing the f_p (pole frequency) have similar effect on the output, both manifests as a gain imbalance in the overall response, and one can be used to compensate for the other.

The polyphase filter builds on the simple RC network and retains most of its properties. The major advantage of using a polyphase filter is that multiple stages

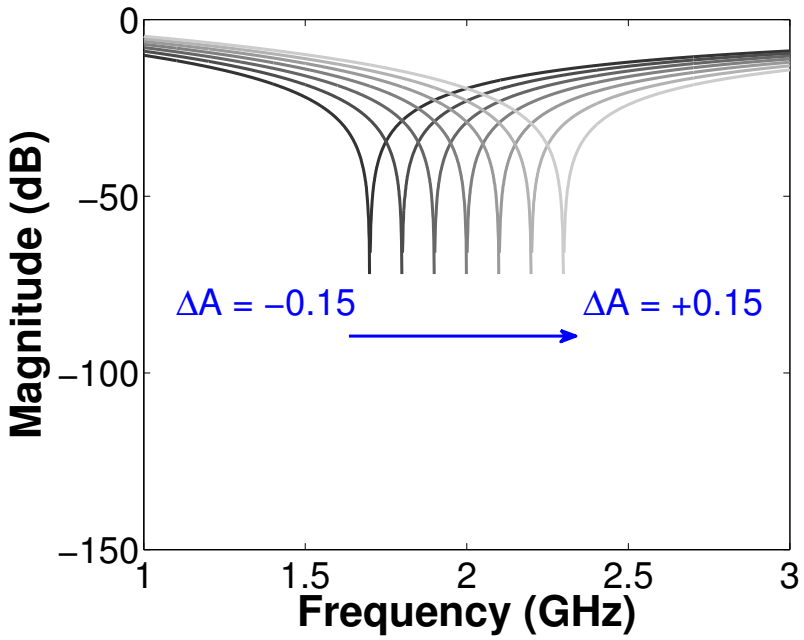


Figure 50: Magnitude response of the RC-CR combination with changing gain imbalance at the input.The effect has the same signature as changing R or C values, and hence, can be used to tune out those effects.

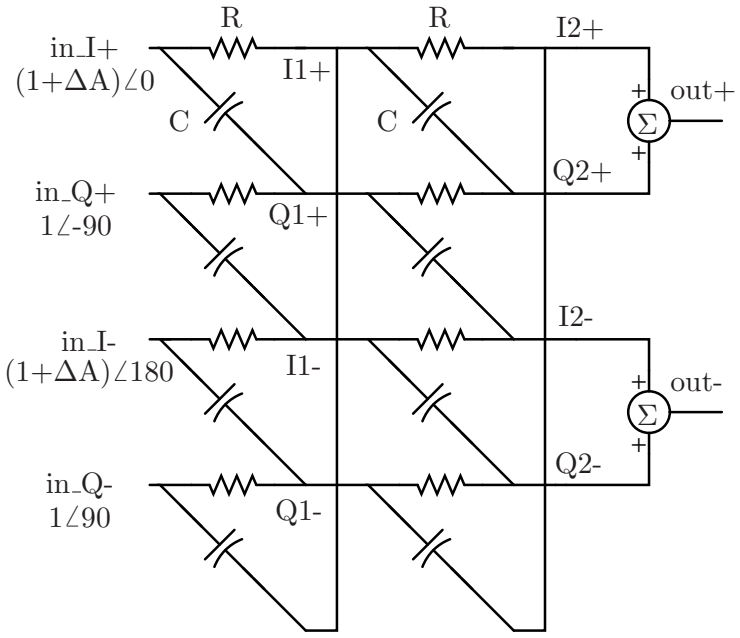


Figure 51: Schematic of two-stage polyphase filter.

can be cascaded to improve the image rejection over a wider bandwidth. A two-stage polyphase filter is shown in Figure 51. In this particular example, the pole frequency of both stages have been set to 2 GHz. The input signals to the polyphase filter are

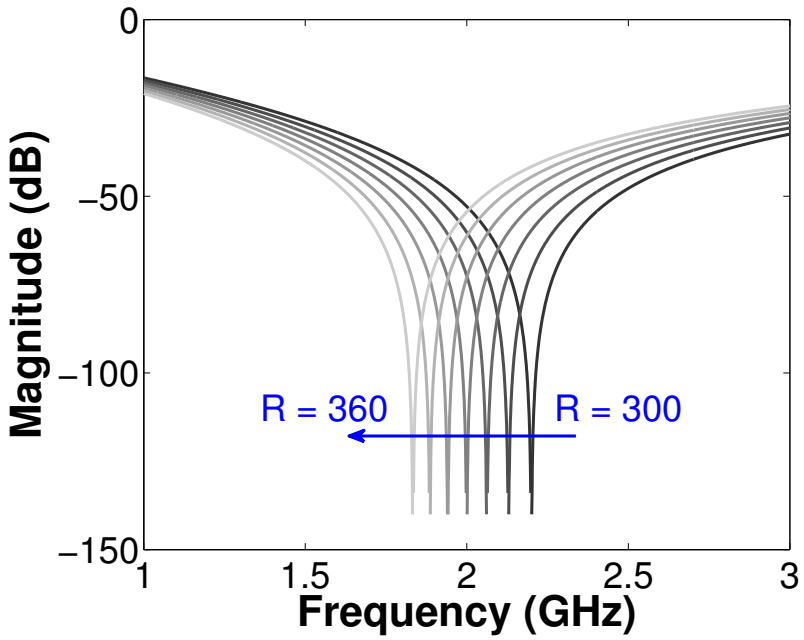


Figure 52: Magnitude response of the two-stage polyphase filter with changing resistor value, simulating the effect of process variation.

at quadrature and the phase sequence is such that the signal driving the high-pass combination (S_{HP}) leads the signal driving the low-pass combination (S_{LP}) by 90°. The quadrature outputs are summed at the output to provide differential signal. The magnitude response of the filter under these conditions is shown in Figure 52 with varying resistor values (R). The advantage of using two stages is evident from the plot. Better image rejection is achieved over a wider bandwidth as compared to the single RC circuit (Figure 48). The magnitude response behaves in exactly the same fashion as that of the RC-CR network. The location of the notch in the magnitude response is determined by the pole frequency (f_p).

The polyphase filter responds quite differently to an amplitude imbalance at its input. The magnitude response of the filter for varying amplitude imbalance (ΔA) is shown in Figure 53. The amplitude imbalance does not, unfortunately, shift the response up or down in frequency as was the case for the single RC-CR network. Rather, any amplitude error on either side of perfect balance degrades the image rejection performance for all frequencies. This means that the effect of the pole shift

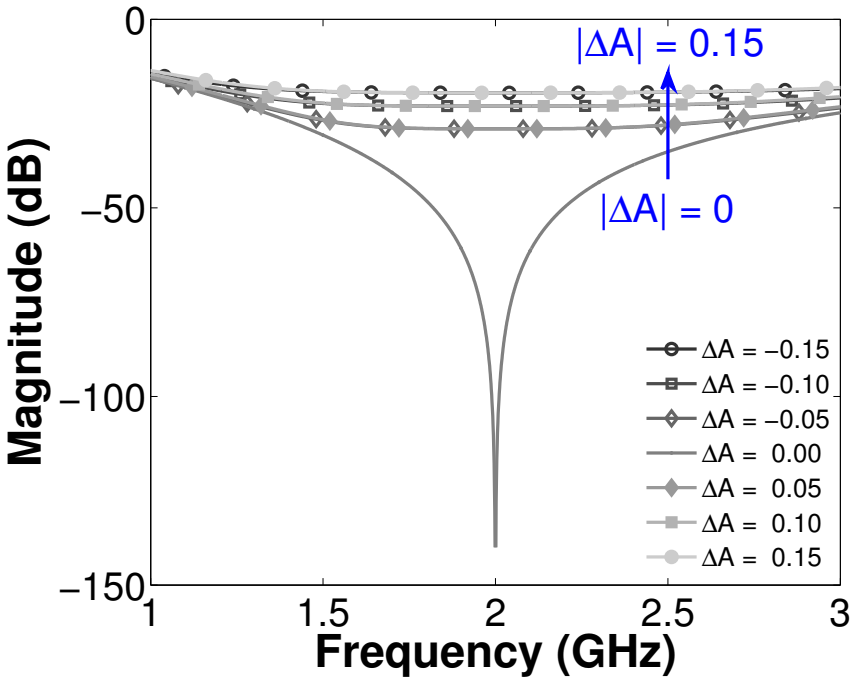


Figure 53: Magnitude response of the two-stage polyphase filter with changing gain imbalance at the input. It has a completely different signature as compared to that of varying R or C, and hence, it cannot use to compensate for drifting component values within the polyphase filter.

of the polyphase filter, which can be caused by process variation, is entirely different from the response of the filter to amplitude imbalance, and the effect of process variation on the polyphase filter cannot be compensated for by changing gain balance outside of the filter.

The polyphase filter behaves differently as compared to the RC-CR network because each input of the polyphase filter drives both a low-pass branch and a high-pass branch, which react differently to the applied amplitude imbalance. The response of an RC network was discussed before (Figure 49). The response of a CR network (Figure 54) to the same input amplitude imbalance is shown in Figure 55. In the case of the CR network, the high-pass response is moved up, and consequently, the notch in the magnitude response shifts down in frequency. To reiterate, for the same amplitude imbalance between the I and Q signals, image cancellation takes place at different frequencies for the high-pass and low-pass combinations, creating a frequency-dependent

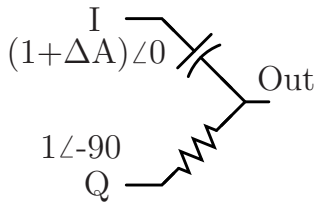


Figure 54: Response of an CR branch to gain imbalance. schematic

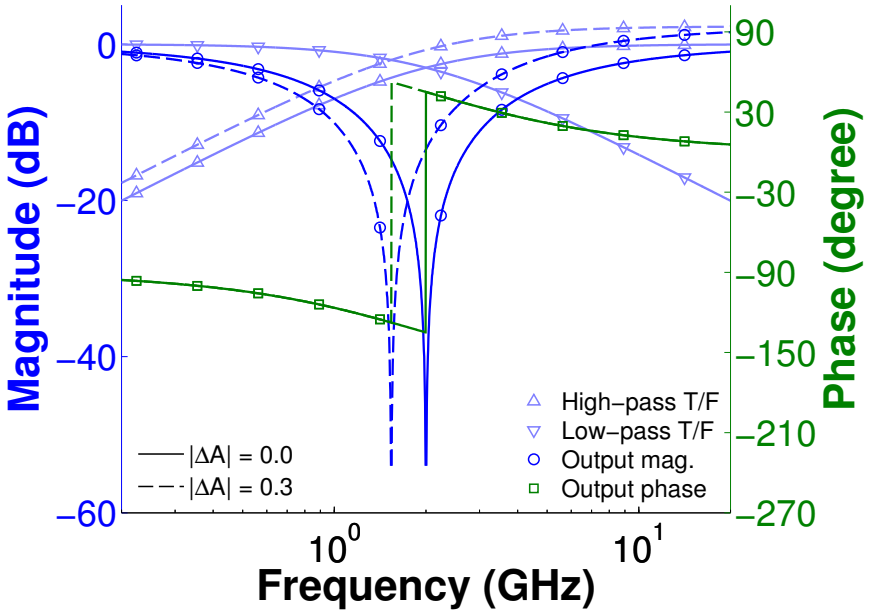


Figure 55: Magnitude and phase response of an CR section with varying gain imbalance.

amplitude imbalance at the output. For a multi-stage polyphase filter this imbalance then cascades down the chain to degrade the IRR.

The magnitude and phase of I1+ (Figure 51) and the corresponding input amplitude and phase differences are plotted in Figure 56. The image is perfectly canceled at the frequency at which the difference in magnitude between the RC and CR response become equal to the input amplitude imbalance. This is convenient way of keeping track of the notch in the image response. In Figure 56, both the magnitude difference between the high-pass and low-pass responses and the input amplitude imbalance are plotted. Their point of intersection determines the location of the notch. In this case, the notch moves up in frequency. The case of the signal Q1+ is shown in Figure 57.

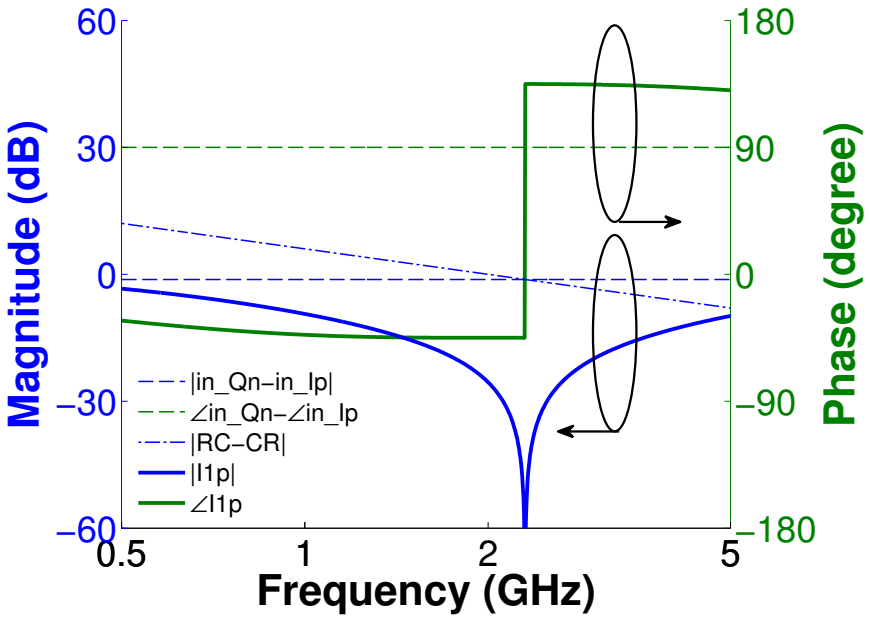


Figure 56: Magnitude and phase response of an CR section with varying gain imbalance.

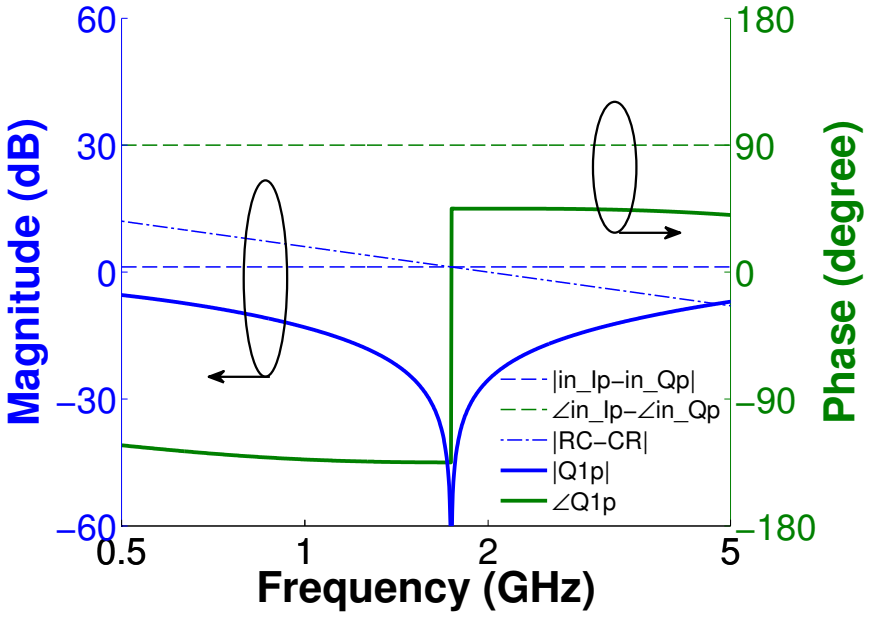


Figure 57: Magnitude and phase response of an CR section with varying gain imbalance.

The notch in this case moves down in frequency.

Figure 58 and Figure 59 plots the responses for the outputs of the second stage I2+

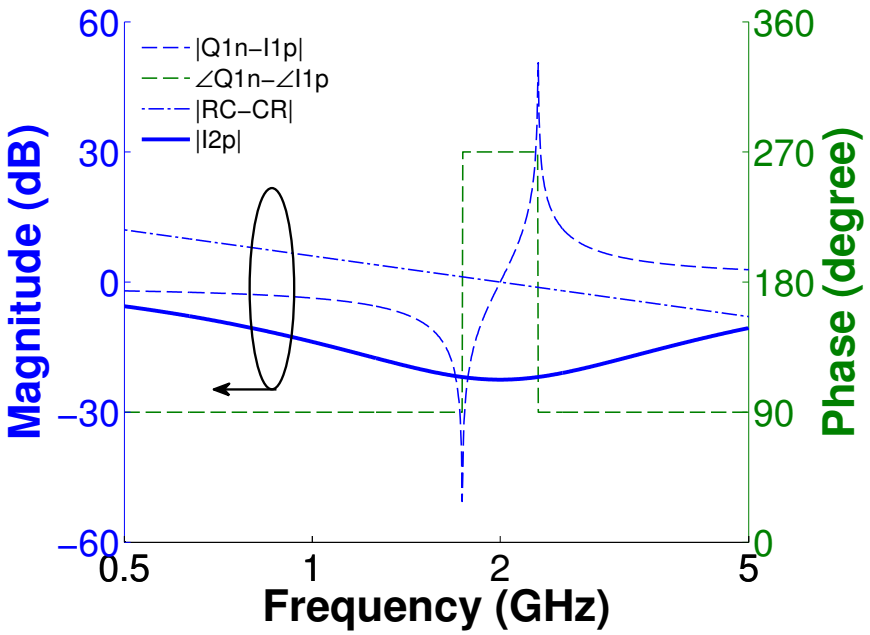


Figure 58: Magnitude and phase response of an CR section with varying gain imbalance.

and Q2+. The conditions for obtaining exact image cancellation can be summarized as:

- The signal driving the high-pass network (S_{HP}) has to lead the signal driving the low-pass network (S_{LP}) by 90°.
- The input amplitude imbalance has to cancel out the difference in magnitude response of the low-pass (RC) and high-pass (HP) networks.

It is interesting to note that the phase difference of the input signals being fed to the second stage of the polyphase filter changes abruptly by 180° in between the frequencies at which the I and Q outputs of the first stage goes to zero; and in that region, the input signals add in phase at the output rather than canceling out, which explains why the output does not go to zero at 2 GHz (Figure 59) despite the condition of gain being satisfied.

The I and Q output of the second stage of the polyphase filter, shown in Figure 58

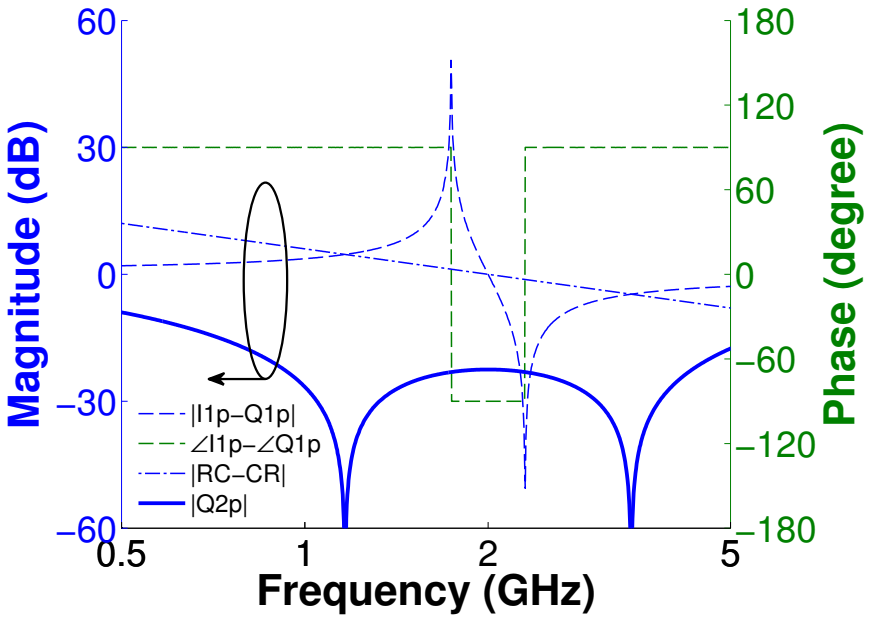


Figure 59: Magnitude and phase response of an CR section with varying gain imbalance.

and Figure 59, when summed together produces the overall image response that was shown in Figure 53. The foregoing analysis reveals the the fact that the imbalances within the polyphase filter have different characteristics as compared to gain or phase imbalances arising from outside the filter and has to be compensated for within the filter to achieve better image rejection.

One way to get around the problem of the pole shift of the polyphase filter is to make the bandwidth of image rejection so wide that even after process variation, the filter covers the required bandwidth of operation. But this approach requires many cascaded stages, each stage adding extra loss to the chain. A better way to deal with the problem of pole shift is to make the polyphase filter tunable. Either R or C can be changed to tune the pole frequency. It is difficult to implement a variable resistor at high frequency without significant penalty in terms of linearity. For this reason, varactors were chosen to vary the capacitors. A schematic of the tunable polyphase filter is shown in Figure . All the voltages controlling the bank of varactors are tied

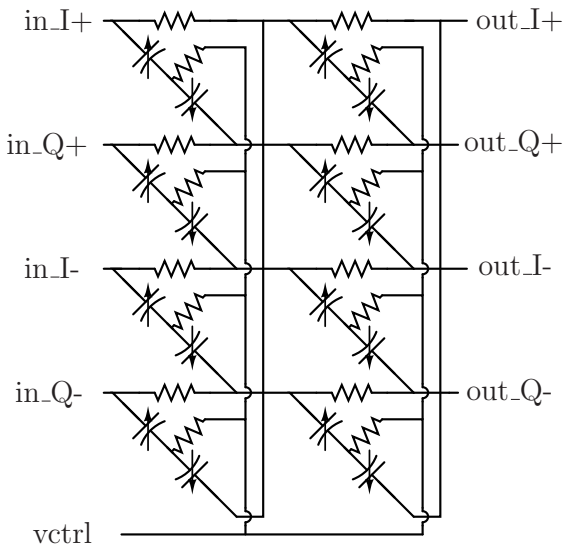


Figure 60: Tunable polyphase filter.

together. This approach allows us to compensate for variations assuming there is no mismatch between the elements. In the presence of mismatches, the IRR can degrade. Also, the quality factor of the varactors limit the achievable level of image rejection. But, as will be shown later, by targeting the major source of variation, which is the variation in the absolute values of the components, excellent IRR was achieved.

3.3.2 Detailed descriptions of the healing algorithms

The goal of the healing algorithm is to find out the right combination of variables that produces optimum performance. The method adopted can be broken down into the following steps:

- Study the relationships between the performance metrics and the tuning knobs.
- Define goals of the healing algorithm.
- Build rules that are necessary and sufficient to achieve the defined goals.
- Combine and translate the rules into codes.

In the ideal scenario, there would be a one to one relation between the performance metrics and the tuning knobs; each tuning knob controlling one output parameter

Table 8: Dependence matrix of tuning knobs and performance metrics

	IRR (dB)	Gain (dB)	OIP3 (dBm)
$\Delta I_{VGA,I-Q}$	strong	very low	very low
$V_{P,I-Q}$	strong	very low	very low
V_{PPF}	strong	very low	very low
I_{ctrl}	low	strong	strong
$I_{VGA,out}$	very low	strong	strong

and having no effect on the others. That would greatly simplify the design of the algorithm. But, unfortunately, that is rarely the case. In reality, each tuning knob affects more than one parameters. In this implementation, circuit topologies and architectures were chosen or to preserve the desired orthogonality as much as possible.

The subset of output parameters and tuning knobs that satisfy the condition of one to one relationship, can be tuned independently in a completely separate step in the healing process. Other parameters, whose dependence on the tuning knobs do not follow the condition of one to one relationship, should be healed together to ensure that the global optimum point is achieved.

The healing rules can sometimes be implemented conveniently in the form of equations. When that is not possible, we may take resort to look up tables. The baseband processor must be aware of the behavioral model of the DUT and its response to the tuning knobs, which are condensed into the healing rules, to be able to efficiently drive the system towards the optimum operating point.

The relative degree of dependence of the performance metrics on the tuning knobs are shown in Table 8. The IRR healing is relatively independent of the OIP3 or gain healing. Hence, the total healing process is divided into two steps. Figure shows the overall flow of the healing process. In the first step, gain and OIP3 are healed simultaneously using I_{ctrl} and $I_{VGA,out}$, and IRR is healed using $\Delta I_{VGA,I-Q}$, $V_{P,I-Q}$, and V_{PPF} in the second step. IRR healing was done at the end because the IRR is

affected by I_{ctrl} when $\Delta I_{VGA,I-Q}$ is not zero. Although I_{ctrl} has only a weak influence on the relative gain between I and Q, IRR, being very sensitive to such changes, may degrade to some extent. In the following sections the details of the healing algorithms are discussed.

3.3.2.1 Gain and OIP3 healing

Gain and OIP3 both depend on I_{ctrl} and $I_{VGA,out}$. Hence, they were healed simultaneously. The dependence of gain and OIP3 on $I_{VGA,out}$ and I_{ctrl} are shown in Figure 61 and Figure 62 respectively. Increasing $I_{VGA,out}$ increases gain of the final VGA stage and increases OIP3 proportionately. I_{ctrl} affects OIP3 in a more complex fashion. Increasing I_{ctrl} decreases the voltage offset between the individual g_m curves of the multi-tanh circuit. There exists an optimum value of I_{ctrl} for which the overall transconductance (G_m) of the VGA achieves maximum flatness. At that optimum value OIP3 of the VGAs become very high and the OIP3 of the micromixer dominates the overall linearity. The plateau at the center of the OIP3 plot (Figure 62) corresponds to the range of I_{ctrl} for which the micromixer linearity becomes the limiting factor. On either side of the plateau, the overall OIP3 is determined by that of the VGAs and starts degrading as we move away from the optimum I_{ctrl} value. Gain increases with I_{ctrl} as increasing I_{ctrl} reduces the offset voltage between the g_m curves, which add to give higher overall transconductance (G_m).

The goals of the algorithm were defined as:

- Try to achieve both gain and OIP3 targets with minimal increase in power consumption.
- If both goals cannot be met, exit with the best possible combination of gain and OIP3.

Based on the plots and the goals, the following rules were developed to find the optimum value of I_{ctrl} and $I_{VGA,out}$:

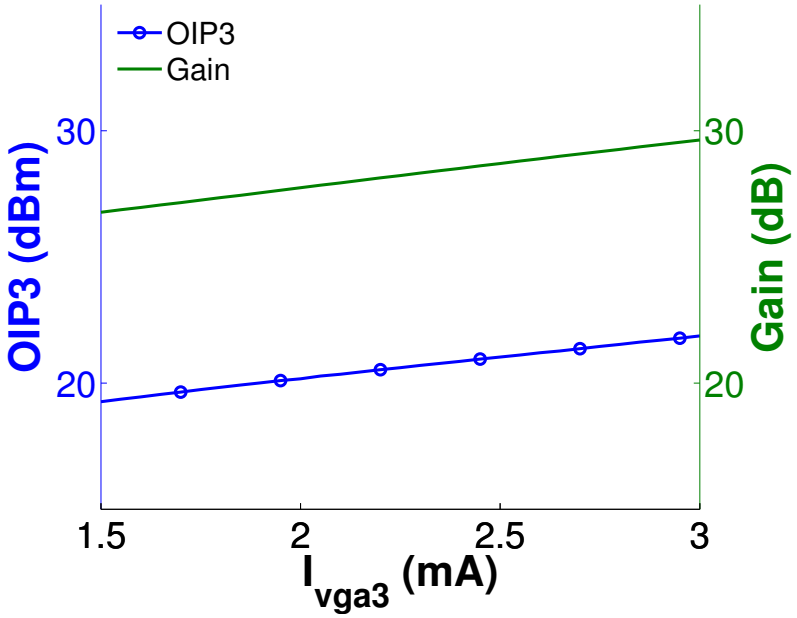


Figure 61: Dependence of gain and OIP3 on $I_{VGA,out}$.

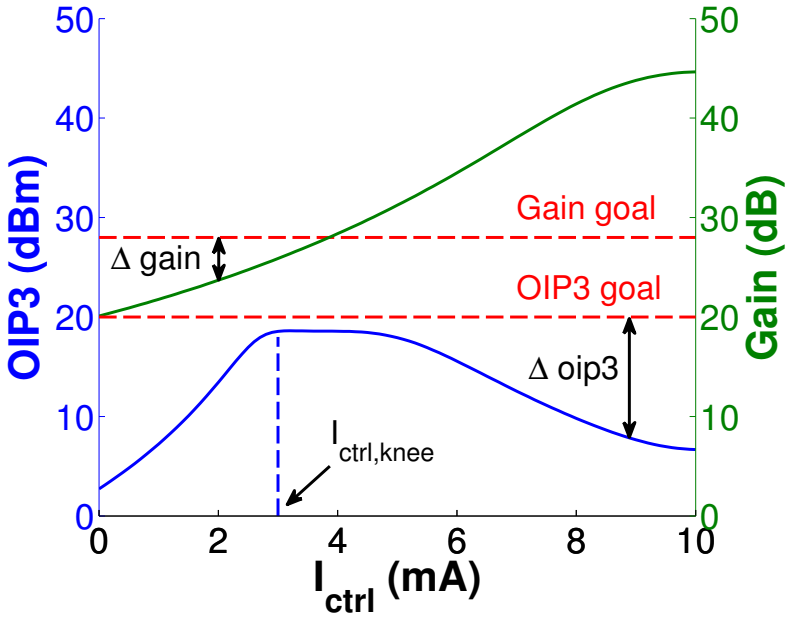


Figure 62: Dependence of gain and OIP3 on I_{ctrl}.

- I_{ctrl} is optimized first as that does involves very little power penalty. If optimization of I_{ctrl} fails to meet the goals, only then I_{VGA3} is increased.

- As shown in Figure 62, below a certain value of I_{ctrl}, named $I_{ctrl,knee}$, both gain

and OIP3 decreases. Hence, it is desirable to operate above $I_{ctrl,knee}$ ($I_{ctrl} > I_{ctrl,knee}$). Since, the position of $I_{ctrl,knee}$ depends on process variation, a more practical way to implement the rule is to make sure that the slope of the OIP3 curve is negative ($\frac{\partial OIP3}{\partial I_{ctrl}} < 0$).

- The optimum value of I_{ctrl} is defined as the point for which gain and OIP3 are equidistant from their respective goals ($\Delta gain = \Delta OIP3$). This rule enables the trade-off between gain and OIP3, if needed. Also, the fact that $I_{VGA,out}$ changes both gain and OIP3 approximately by the same amount, fits perfectly with this approach. The optimization of I_{ctrl} can be followed by an increase in $I_{VGA,out}$ if needed.

Figure 63 shows the flow of the algorithm, which starts by making sure that the OIP3 slope is negative ($\frac{\partial OIP3}{\partial I_{ctrl}} < 0$). Once on the negative slope of the OIP3 hill, the value of I_{ctrl} is updated based on the following equations:

$$I_{ctrl} = I_{ctrl} + I_{ctrl,step,sign}.I_{ctrl,step,mag} \tag{11}$$

where,

$$I_{ctrl,step,sign} = \frac{\Delta gain - \Delta OIP3}{|\Delta gain - \Delta OIP3|} \tag{12}$$

and

$$I_{ctrl,step,mag} = \epsilon' + k.log\,[1 + |\Delta gain - \Delta OIP3|] \tag{13}$$

The step size is adaptive. Farther the operating point from the optimum point, greater is the difference between $\Delta gain$ and $\Delta OIP3$, and larger is the step size; and, as I_{ctrl} gets closer to the optimum value, the step size gets smaller. k is a scaling factor for the step size and affects the convergence characteristics. A large k results in "ringing" and a small k results in a "over-damped" response. For a very large k, the algorithm may not converge at all. The value of k was chosen carefully to ensure fast convergence. The variable ϵ' is used to ensure that the step size does not get too

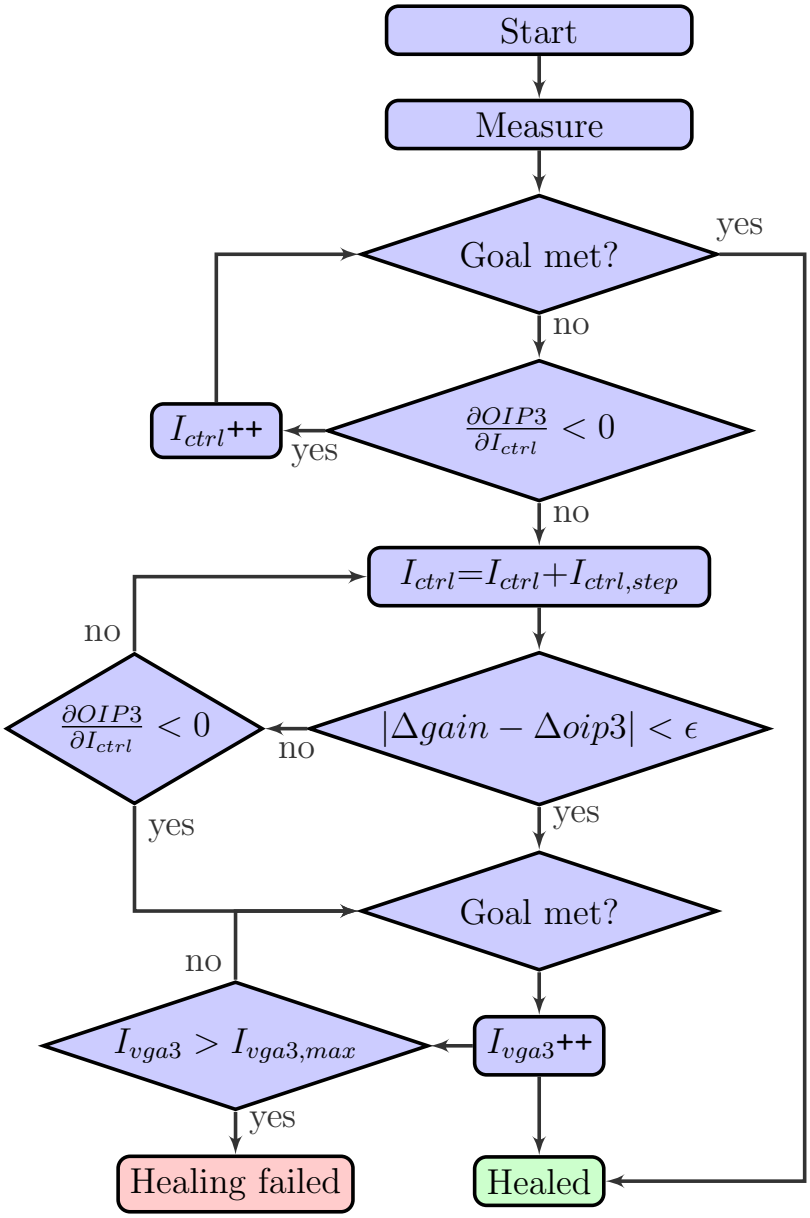


Figure 63: Algorithm for healing gain and OIP3.

small when I_{ctrl} is close to the optimum point; and its value provides a way to control the trade-off between accuracy and speed.

The iterative process continues till the difference between $\Delta gain$ and $\Delta OIP3$ falls below an error bar (ϵ), which provides another control over speed and accuracy of the procedure. At each iteration of updating the value of I_{ctrl}, the slope of OIP3 is checked to make sure that the operating point is above $I_{ctrl,knee}$. If the goals are not

met after determining the optimum value of I_{ctrl}, $I_{VGA,out}$ is increased till the goal a is achieved or the maximum allowed value of $I_{VGA,out}$ is reached.

3.3.2.2 IRR healing

IRR healing consists of three steps: gain compensation, phase compensation, and centering the frequency response of the polyphase filter. The relationship between IRR and the gain and phase imbalances can be approximated as

$$IRR \approx \frac{\Delta A^2 + \Delta\theta^2}{4}, \tag{14}$$

where ΔA is the gain imbalance and $\Delta\theta$ is the phase imbalance between the I and Q paths. As (14) suggests, The optimum points for gain and phase imbalances that minimizes IRR are quite independent of one another and hence, the optimum value of one can be found irrespective of what the other is set to. The same holds true for gain imbalance and the pole shift of the polyphase filter. The optimum value of phase imbalance though depends on the location of the RC pole of the filter. It is not possible to find the optimum phase without first centering the polyphase filter. The IRR healing was implemented by compensating for gain imbalance, centering the polyphase filter, and compensating for phase imbalance, in that order.

Compensation for gain imbalances was done by introducing a difference between the gain of the I and Q VGAs. The dependence of the image gain on the difference of bias currents of the VGAs ($\Delta I_{VGA,I-Q}$) is shown in Figure 64. The notch in the image gain response corresponds to the peak in the IRR response. The location of the notch changes with process variation and the goal was to find $\Delta I_{VGA,I-Q}$ that minimizes image gain. The flow of the algorithm is shown in Figure 65. The algorithm starts by measuring the image gain at the two extremes points of the $\Delta I_{VGA,I-Q}$ interval. Depending on which value is greater, the corresponding $\Delta I_{VGA,I-Q}$ value is updated to the middle of the interval; thus shrinking the search interval in half. This process continues till the search interval shrinks down to the desired accuracy level.

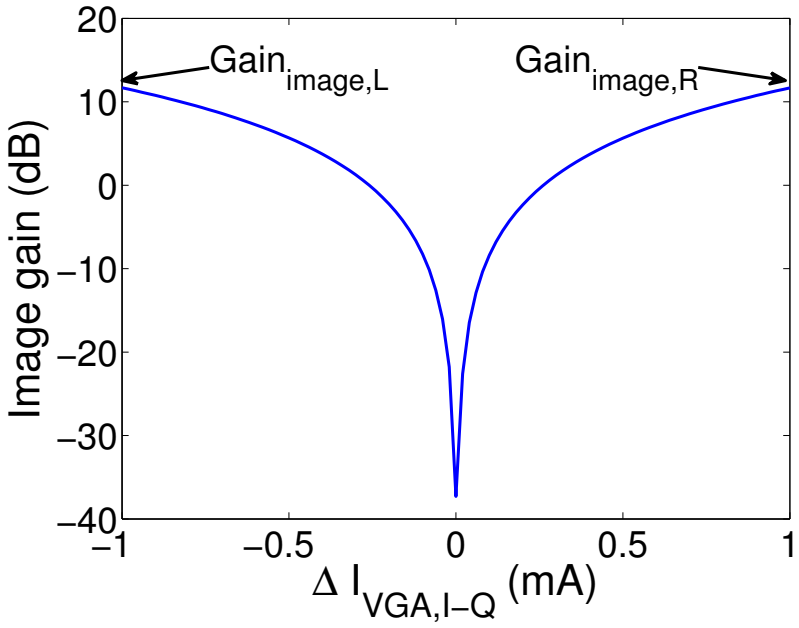


Figure 64: Dependence of image gain on $I_{VGA,I} - I_{VGA,Q}$.

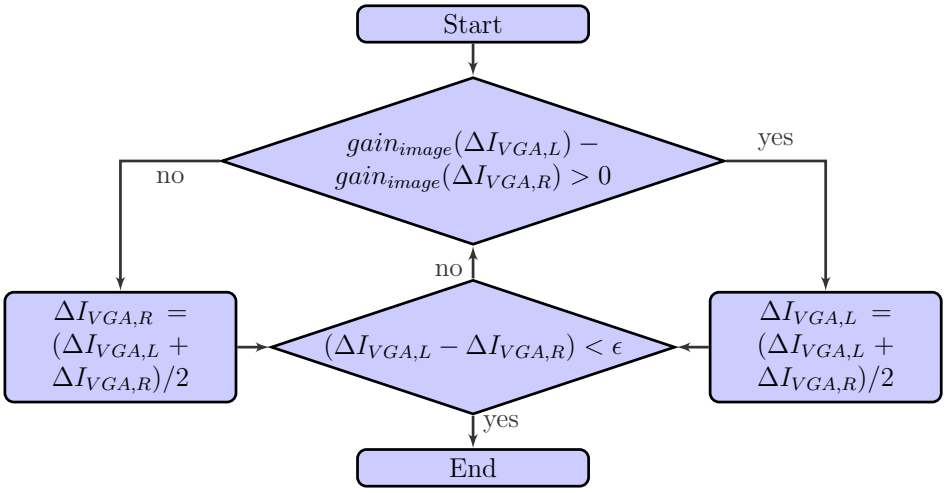


Figure 65: Algorithm to find out optimum ΔI_{VGA} for gain compensation.

The effect of phase imbalance on image gain has the same signature, and the optimum value of $\Delta V_{P,I-Q}$ that minimizes image gain was determined in a similar fashion.

The effect of V_{PPF} on image gain is shown in Figure 66. The location of notch was estimated by the difference in the image gain values ($\Delta gain_{image}$) at 1GHz and 3 GHz. The variation of $\Delta gain_{image}$ with V_{PPF} is shown in Figure 67. Under nominal

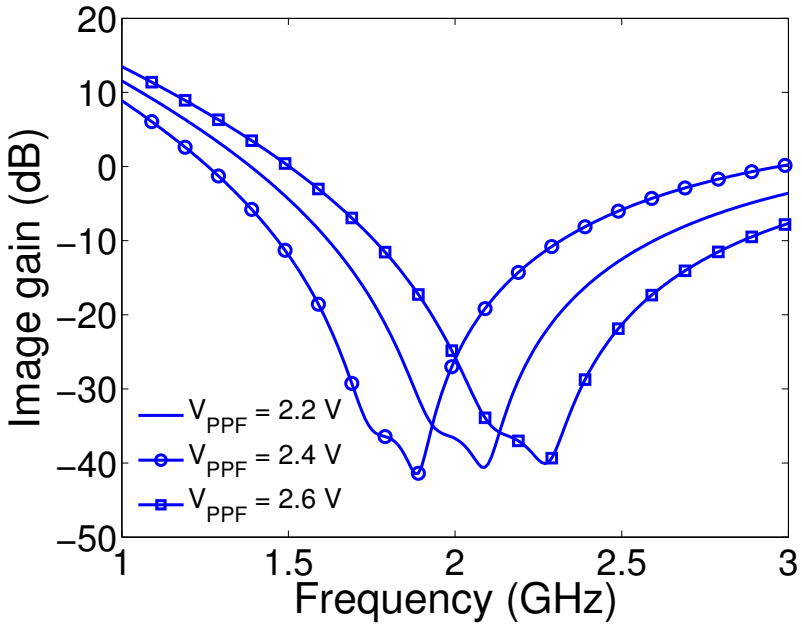


Figure 66: Change in image gain frequency response with V_{PPF}.

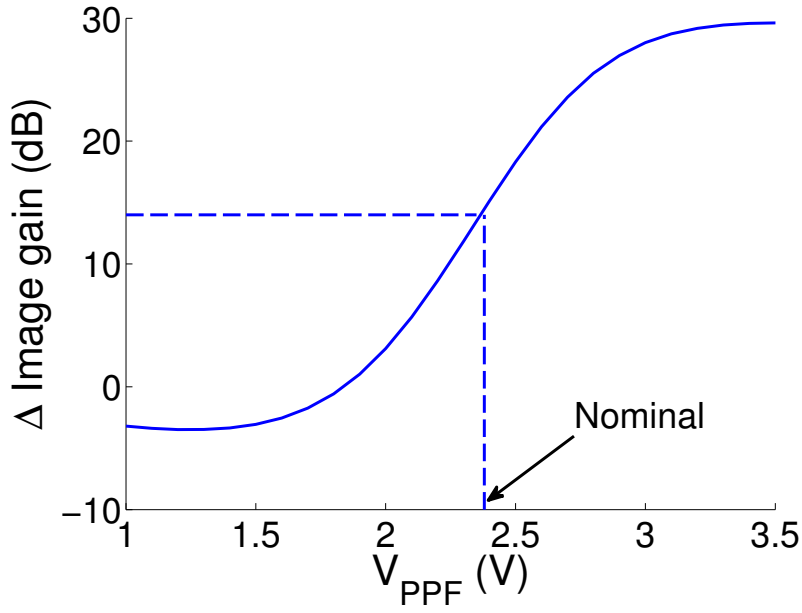


Figure 67: Difference in image gain at upper and lower edge of the frequency band vs. V_{PPF}.

conditions, the value of $\Delta gain_{image}$ is about 14. Process variation can cause the operating point to move from that nominal value and the goal of the algorithm is to bring the value of $\Delta gain_{image}$ to its nominal value ($\Delta gain_{image,nom}$). An empirical

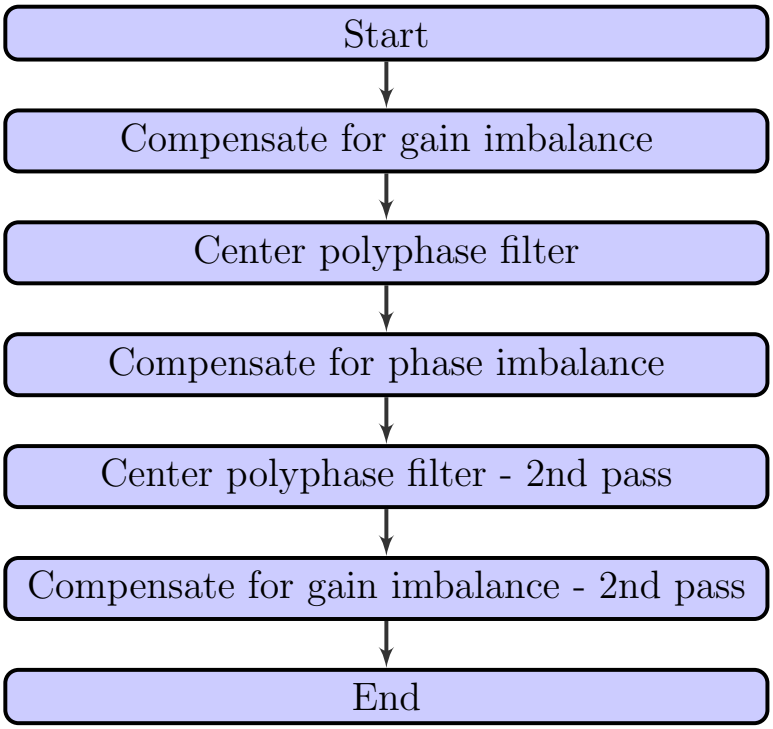


Figure 68: Flow of IRR healing algorithm.

equation was developed based on an straight-line approximation of the curve in Figure 67. The equation, shown in (15), was used to update the value of V_{PPF} at each iteration until the value of $\Delta gain_{image}$ ended up within an specified error bar of the nominal value ($\Delta gain_{image,nom}$).

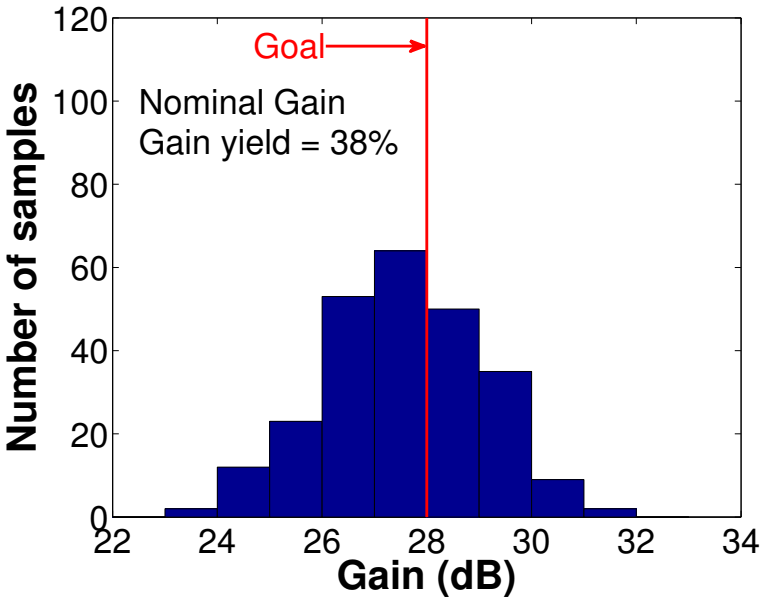
$$V_{PPF} = V_{PPF} + \left(\Delta gain_{image} - \Delta gain_{image,nom}\right)/33 \tag{15}$$

The complete IRR healing algorithm is shown in Figure 68. A second round of gain compensation and centering was used to improve accuracy.

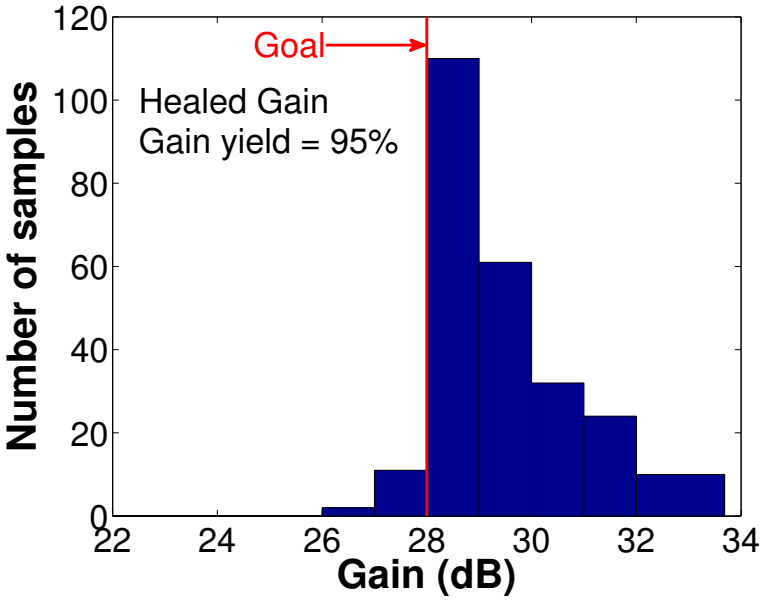
3.3.3 Results

The healing procedure, outlined in the previous section, was applied to 250 monte-carlo runs at 13 GHz RF and 2 GHz IF. The resulting histograms for gain, OIP3, and IRR are shown in Figure 69, Figure 70, and Figure 71. The healing procedure improves the yield in each case significantly.

To verify how the IRR healing at a single frequency translates over a bandwidth

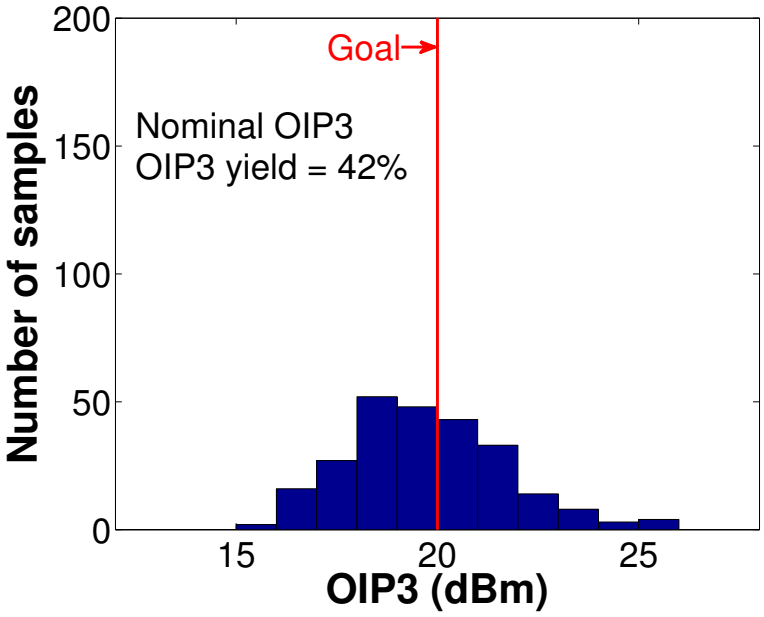


(a) Pre-healing gain

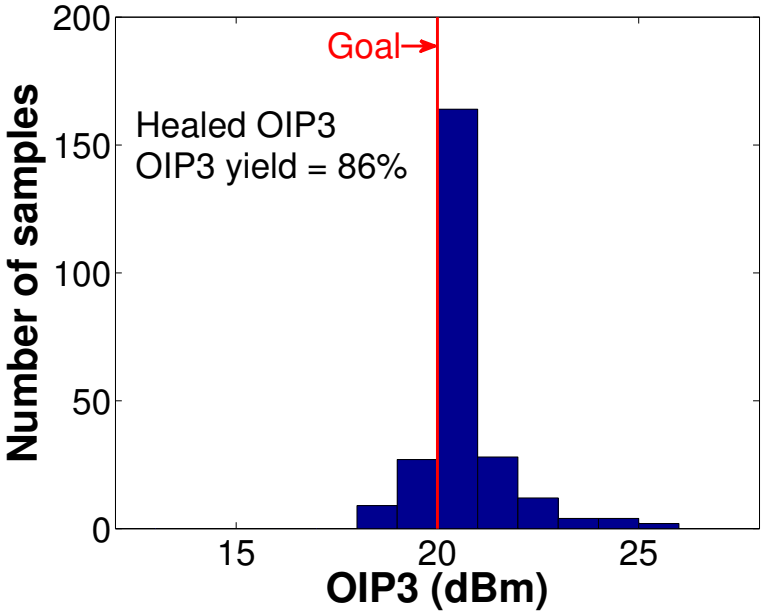


(b) Post-healing gain

Figure 69: Histogram of gain before and after healing for 250 monte-carlo runs.

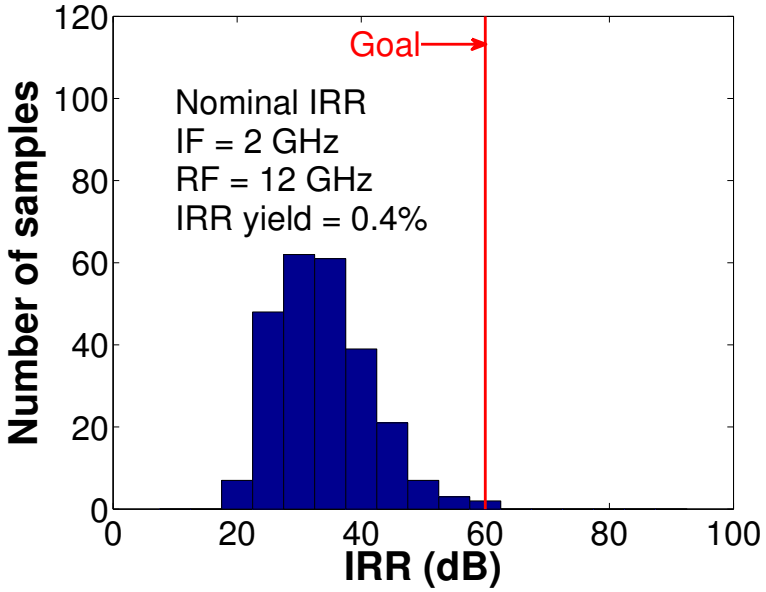


(a) Pre-healing OIP3

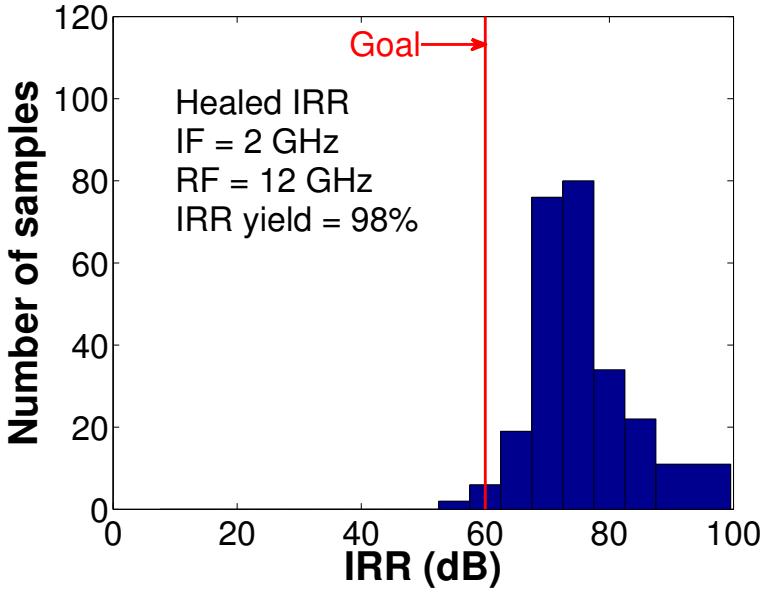


(b) Post-healing OIP3

Figure 70: Histogram of OIP3 before and after healing for 250 monte-carlo runs.



(a) Pre-healing IRR



(b) Post-healing IRR

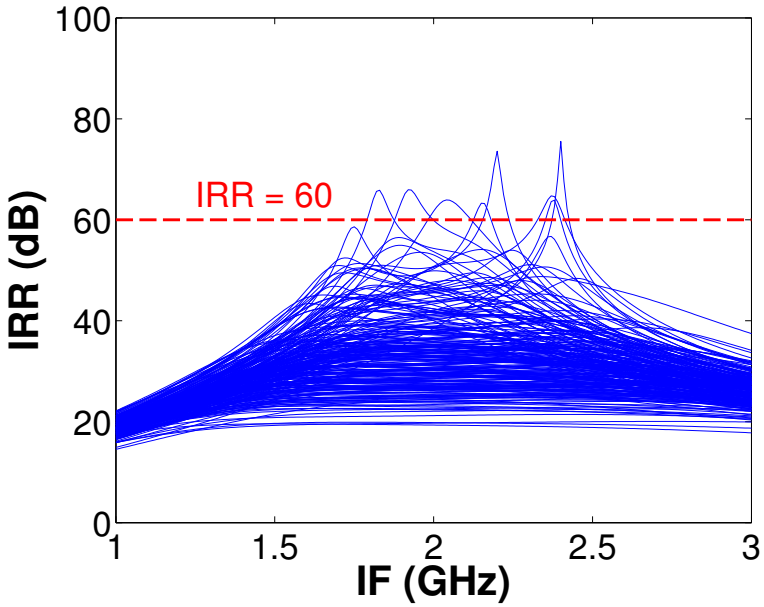
Figure 71: Histogram of IRR before and after healing for 250 monte-carlo runs.

around the center frequency, the IRR was simulated over a wide bandwidth before and after healing. The plots are shown in Figure 72. The healed IRR is better than 60 dB over a bandwidth of 140 MHz for most of the monte carlo runs. For an IRR requirement of 50 dB, the bandwidth increases to 380 MHz.

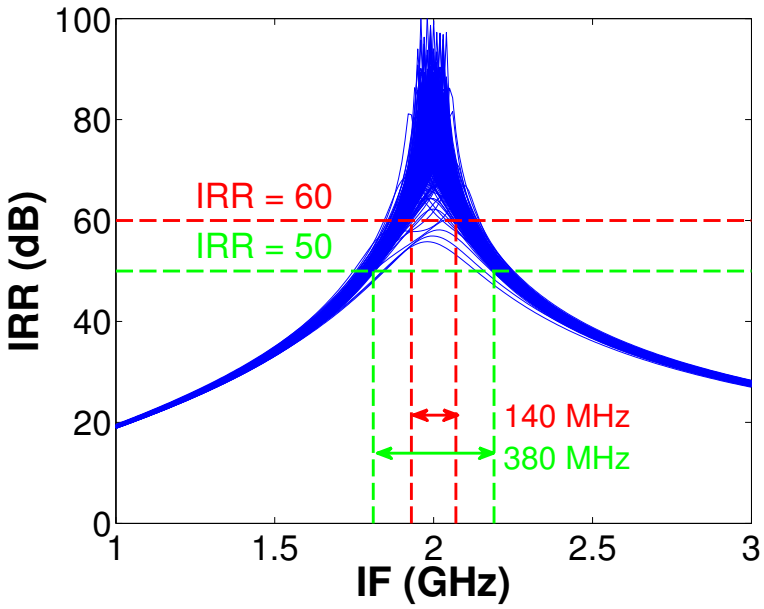
Healing of gain and OIP3 involves increasing the power consumption in some cases. The histograms for power consumption before and after healing are shown in Figure 73. After healing the power consumption increases only by 1.57%, while the overall yield for gain, OIP3, and IRR goes up from 0% to 82.4%.

3.4 Summary

An adaptive 6-20 GHz image-reject mixer was implemented in a 200-nm SiGe BiCMOS process. Tunability of various performance metrics was explored with different bias voltages and currents as control elements. Automated self-healing of IRR, gain, and linearity was demonstrated in measurement with on-chip signal sources and DACs. The IRR performance of the mixer was analyzed and improved. A monte-carlo based methodology was developed to verify the effectiveness of the healing procedure. The flexible nature of this "self-healing" mixer makes it suitable for an RF receiver that can adapt to varying performance requirements or can deliver consistent performance despite process variations.

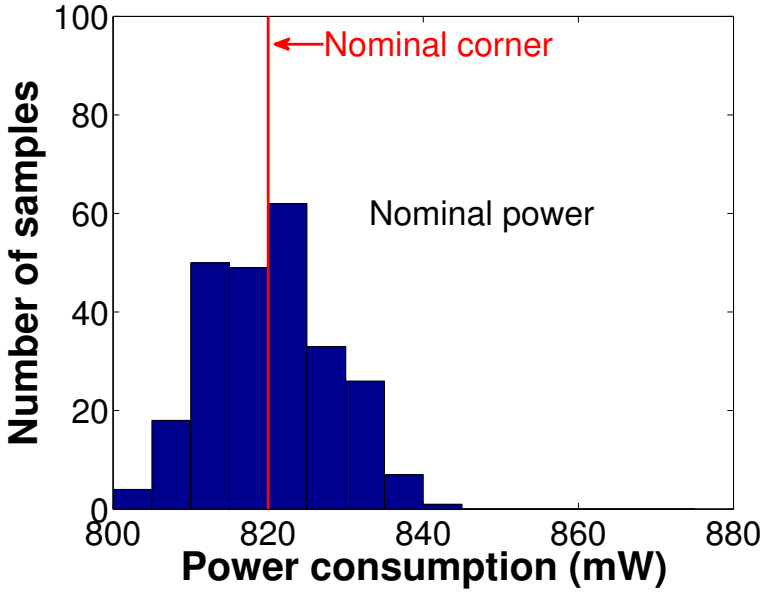


(a) Pre-healing IRR vs. IF

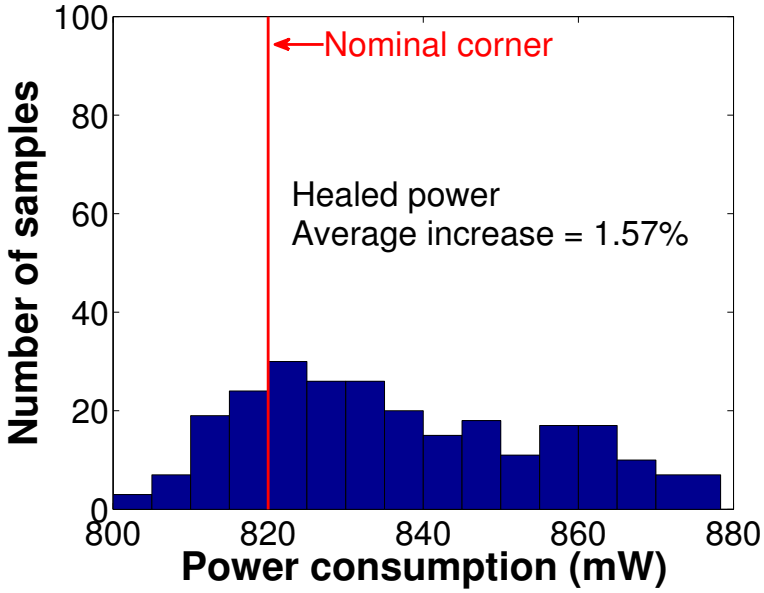


(b) Post-healing IRR vs. IF

Figure 72: IRR vs. IF before and after healing for 250 monte-carlo runs.



(a) Pre-healing power consumption



(b) Post-healing power consumption

Figure 73: Power consumption before and after healing for 250 monte-carlo runs.

CHAPTER IV

LOW-LOSS SWITCHES

RF switches find widespread application in a variety of electronic systems. Switched-line phase shifters, transmit-receive (T/R) switches, multi-mode and multi-band transceivers, phased arrays, reconfigurable and self-healing systems are a few applications that require high-performance RF switches. In many of these applications, the insertion loss of the switch greatly impacts the performance of the system, and hence, it is desirable to minimize the loss of the switch.

Minimizing insertion loss inevitably involves a trade-off with other switch performance metrics such as isolation, bandwidth, and signal handling capacity [45]. In narrow-band designs, it is possible to take advantage of LC resonance to reduce loss [46]. For wide-band high-frequency switches, the options to reduce loss are much more limited. The primary means of achieving low loss is to reduce the loss through the gate and substrate of the component transistors [5, 47]. A large resistor added to the gate prevents high-frequency signal from leaking through the gate, but limits the switching speed of the switch. In bulk CMOS technologies, loss through the substrate can be minimized by increasing the substrate resistance, isolating the substrate using deep-trench, or using triple-well technologies.

Phase shifters are crucial components for phased-array communication and radar systems. Low-loss and inexpensive phase shifters are required for improved performance and widespread application. Many phase shifter architectures, such as the high-pass/low-pass and switched line topologies, require RF switches for their operation. In such cases, the RF performance of the switch, and especially its insertion loss, dominates the overall phase shifter performance. For this reason, microwave

and millimeter-wave phase shifters are typically implemented using ferrite materials [48], p-i-n diodes [49], III-V FET switches [50] and more recently MEMS [51]. Silicon FET-based phase shifters, however, consume virtually no DC power and are amenable to better integration with on-chip low noise amplifiers or power amplifiers, and thus have emerged as an active research topic.

In this chapter, design of low-loss switches in both bulk and silicon-on-insulator (SOI) technologies are discussed.

4.1 Low-loss switch in bulk technology

Recently, there has been significant work on MOSFET-based single-pole, double-throw (SPDT) switches for various microwave applications [52]– [55]. In most SiGe BiCMOS technologies, the CMOS devices are typically fabricated on a medium-resistivity (5 – 20 Ω-cm) p-type bulk substrate, as opposed to a lower-resistivity (< 1 Ω-cm) substrate typically used in a pure CMOS technology. It has been previously shown that by either significantly increasing [54] or significantly decreasing [55] the substrate resistance for a series-shunt SPDT switch design, the insertion loss of the switch can be improved. In a previous work [56], the effects of substrate and additional gate impedance on insertion loss, isolation, bandwidth and linearity of series-shunt SPDT switches targeted for X-band radar applications were studied in detail. The present work extends this to K-band, performs additional optimization for loss, and implements a 20 GHz 1-bit phase shifter using deep-trench isolated switches with low insertion loss, demonstrating the feasibility of building highly integrated low loss K-band phase shifters in commercially-available SiGe technology.

In this section, design of wideband high-frequency (K-band) nMOS SPDT switches and a switched-line 180° single-bit phase shifter using bulk technology is discussed. The design of the phase shifter demonstrates the use of low insertion loss nMOSFET switches in 130-nm silicon-germanium (SiGe) BiCMOS technology. Design and layout

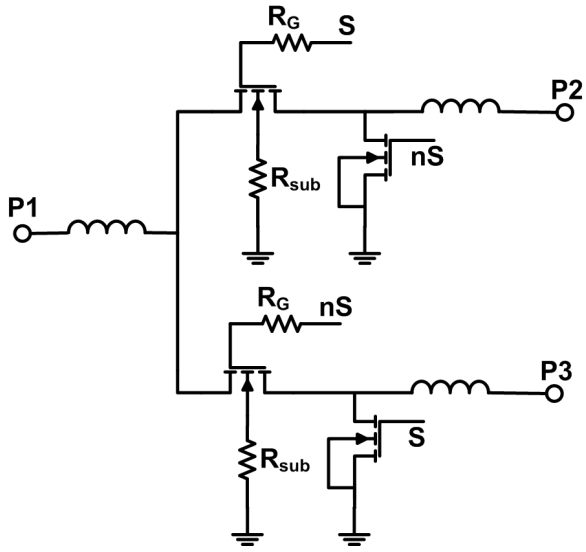


Figure 74: nMOS series-shunt SPDT switch topology.

optimization approaches for MOSFET based series-shunt, single-pole double-throw (SPDT) switches were investigated. The switches were designed to use deep trench substrate isolation to reduce losses. An insertion loss of 2 dB and a isolation better than 15 dB up to 20 GHz were obtained in measurement. The single-bit phase shifter, built from these switches and delay lines has an insertion loss of 4.5±0.5 dB at 20 GHz while maintaining input and output return losses better than -15 dB.

4.1.1 Technology

The technology utilized for this work is the commercially-available IBM 8HP SiGe HBT BiCMOS technology [57]. This 130 nm SiGe technology offers standard Si CMOS, 200 GHz SiGe HBTs, various types of resistors, shallow-trench and deep-trench isolation, low-loss MIM capacitors, low-loss spiral inductors, and on-chip microstrip transmission lines. This SiGe platform is fabricated on a conventional 8 – 10 Ω-cm p-type bulk substrate, and contains no additional buried epi-layer.

4.1.2 nMOS switch design

A standard series-shunt nMOS SPDT switch (Figure 74) utilizes nMOS transistors acting as pass-gates and shunt terminations. The switch performance is mostly determined by the electrical characteristics and parasitics associated with the series (or pass-gate) device. Devices with higher W/L ratio decrease the on-resistance and hence insertion loss at low frequency. At the same time, however, the larger parasitic capacitances of these bigger devices degrade their high frequency performance. Various nMOS design and layout optimizations were studied for the series device, to determine their transmission and isolation properties in both the "on" and "off" state. These design and layout changes attempt to significantly increase or decrease the series devices substrate resistance (R_{sub}) and gate resistance (R_G) by incorporating on-chip polysilicon-based resistors, additional substrate contacts, and deep-trench isolation structures in the switch design. All the design variations consist of the same core design, which utilize 6 parallel nMOS devices for the series device, with four gate fingers, each 2μm wide. To alter the impedance seen by the bulk of the series devices, three different layouts (Figure 75) were examined, a "high-substrate" (HS) resistance design, a "medium-substrate" (MS) resistance design, and a "low-substrate" resistance design (LS). The HS design incorporates a ring of deep-trench isolation (approximately 10 μm deep and 1 μm wide) around the 6 nMOS devices to increase impedance to the substrate. The MS design incorporates a single ring of substrate contacts (approximately 2 μm from the devices and 1 μm wide), to obtain an intermediate impedance to the substrate. The LS design incorporates additional substrate contacts adjacent to the initial ring, providing low-impedance substrate connection.

Similarly, a 21 kΩ polysilicon resistor was placed in series with the gate of the nMOS device to create a high gate resistance connection. With these variations, 5 different series nMOS devices were experimentally investigated: a high substrate

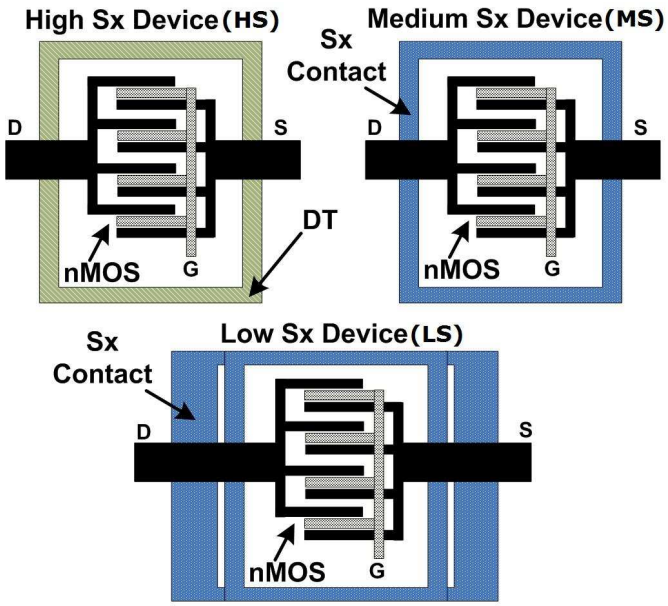


Figure 75: Various layout configurations of the nMOS devices investigated.

resistance, high gate resistance device (HSHG), a high substrate resistance, low gate resistance device (HSLG), a medium substrate resistance, low gate resistance device (MSLG), and a low substrate resistance, low gate resistance device (LSLG).

4.1.3 Measured Results for nMOS device

The S-parameters of the series nMOS devices were measured at wafer-level, with the pad parasitics de-embedded using standard open-short de-embedding. The S_{21} of these devices can be seen in Figure 76, with the gate-source voltage (V_{GS}) biased at 0 V and 1.2 V to evaluate their transmission and isolation capabilities. As seen in Figure 76, the HSHG device demonstrates the best transmission performance, with minimum degradation at higher operational frequencies. The HSLG device has the second best transmission performance, and the MSLG and LSLG devices have nearly identical (and the worst) performance. Not surprisingly, the exact opposite performance trends occurred for the isolation capabilities of the devices.

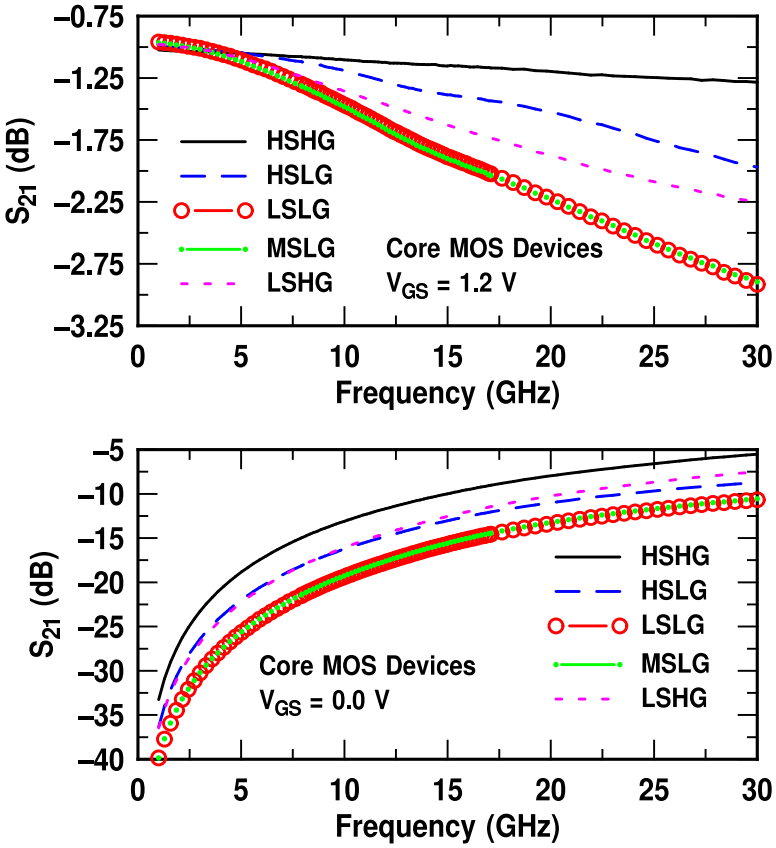


Figure 76: Measured S_{21} of various nMOS layouts for both on and off states.

These results highlight the impact of the deep-trench isolation ring on the high-substrate (HS) devices. This ring increases the nMOS substrate resistance, minimizing loss through the parasitic drain-substrate and source-substrate capacitances. However, in doing this, the parasitic coupling path between the drain and source (via the substrate) is increased, degrading the isolation. The incorporation of an external gate resistance has a similar effect, by reducing the loading effect of the gate-source and gate-drain capacitances. Interestingly, the medium-substrate (MS) and low-substrate (LS) devices have essentially identical S-parameter performance, indicating that (at least for this technology) the incorporation of additional substrate contacts has no effect in reducing the effective nMOS substrate impedance.

4.1.4 SPDT Switch Design

The SPDT switch was designed based on the familiar series-shunt topology (Figure 74). nMOS devices with isolated substrate and high gate resistance (HSHG) were used in the design to minimize insertion loss at high frequency. Inductors and device parasitic capacitances were used to match the ports to 50 Ω. Due to the small amount of required inductance RF line inductors were used in this case. The RF line component is essentially a metal trace over a deep trench isolated ground plane, emulating a microstrip line with very high characteristic impedance. The design incorporated a 5 finger nMOS device with a gate width of 3.2μm for the shunt switch. CMOS inverters were used to drive the gates of the devices. All of the switches are 0.93 X 0.85 mm^2 in size (0.48 X 0.60 mm^2 not including the pads), operate off a 1.2 V supply, dissipate < 1 μW of dc power, and incorporate on-chip microstrip transmission lines for signal routing.

4.1.5 SPDT Measured Results

The measured insertion loss and isolation performance of the HSHG SPDT switch is shown in Figure 77 and Figure 78. Due to the absence of any resonance network,

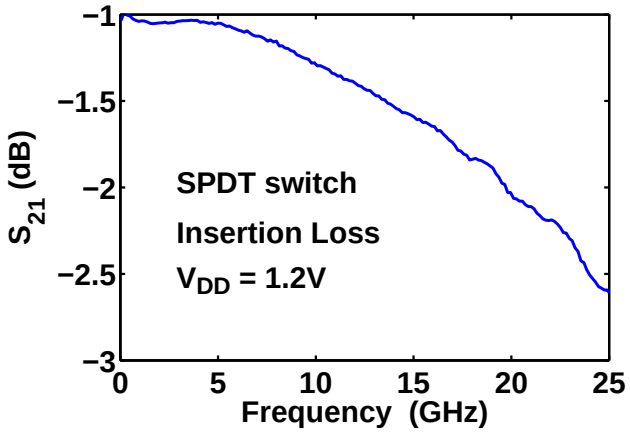


Figure 77: Measured insertion loss of the SPDT switch.

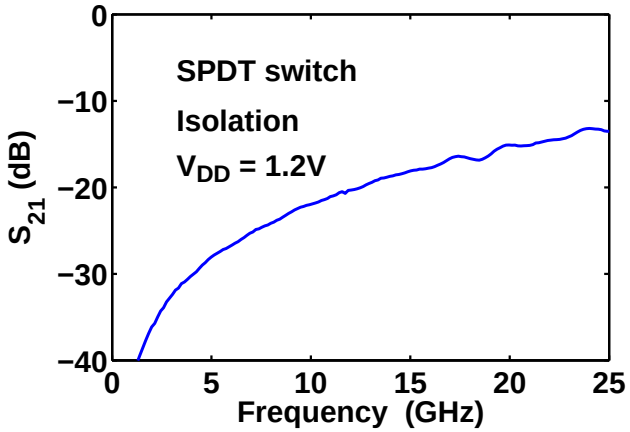


Figure 78: Measured isolation of the SPDT switch.

the switch has broadband characteristics, as expected. The switch demonstrates low insertion loss performance, with an S_{21} of -1.4 dB at 10 GHz, -1.7 dB at 15 GHz, and -2.0 dB at 20 GHz. The isolation between the ports is better than 15 dB upto 20 GHz (Figure 78). The ports are well-matched from 1 GHz to 25 GHz (Figure 79), with S_{11} and S_{22} below -15 dB from 1 to 20 GHz. IIP_3 and $P1dB$ of the switch was measured to be 22.5 dBm and 12.5 dBm respectively at 20 GHz.

4.1.6 Phase Shifter design

The K-band phase shifter design is based on two microstrip lines whose phase delay differ by 180° at 20 GHz. SPDT switches are used to switch between the reference

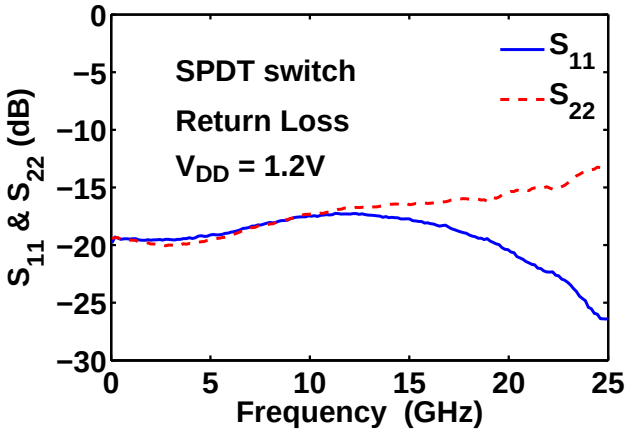


Figure 79: S_{11} and S_{22} of the SPDT switch.

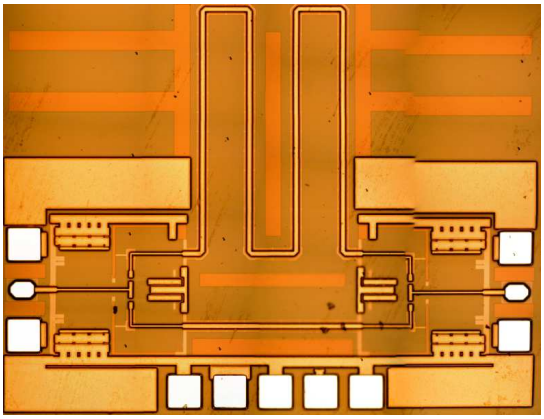


Figure 80: Die micrograph of the K-band phase shifter.

arm and the delay arm. The delay lines are implemented as microstrip lines with 50 Ω characteristic impedance. The phase shifter is bi-directional in nature and consumes virtually no DC power. Die micrograph of the phase shifter is shown in Figure 80. The phase shifter occupies 1.46 X 1.18 mm^2 without pads.

4.1.7 Phase Shifter Measured Result

Insertion loss and matching at the ports of the phase shifter are shown in Figure 81 and Figure 82, respectively. Insertion loss at 20 GHz is below 4.75 dB with gain mismatch between the two arms being below 0.5 dB. It is well-matched at the ports, with S_{11} below -15 dB from 1 GHz to 25 GHz. Phase variation with frequency is shown in Figure 83. A 180° phase difference was obtained at around 24 GHz, and

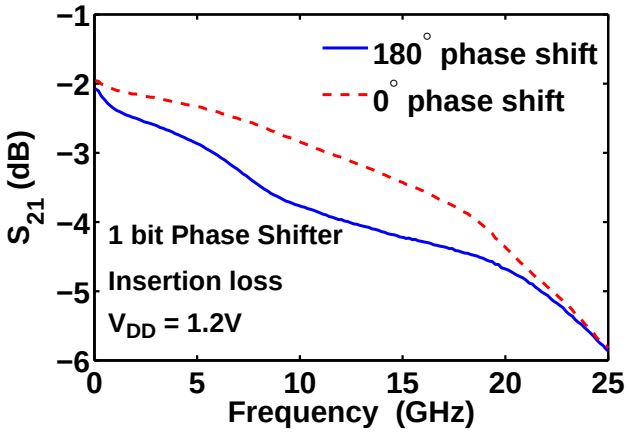


Figure 81: Insertion loss of K-band phase shifter.

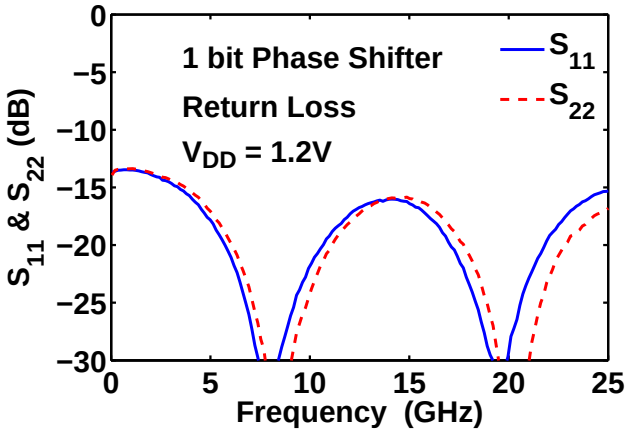


Figure 82: S_{11} and S_{22} of the K-band phase shifter.

the measured bandwidth is about 2 GHz with 10° phase error.

4.1.8 Benchmarking

The performance of this HSHG SPDT switch is compared with other published results in Table 9. [55] and [53] are based on a 0.13 μm CMOS technologies and [58] uses GaAs MESFETs. It should be noted that the work presented in [52] utilizes three supply lines (GND, VDD, and VSS) to apply dc bias to the RF signal path, which reduces the parasitic capacitances of the device as well as increasing the transient voltage capabilities of the switch. The HSHG switch presented here is competitive with all of the previously published work, in terms of insertion loss and bandwidth

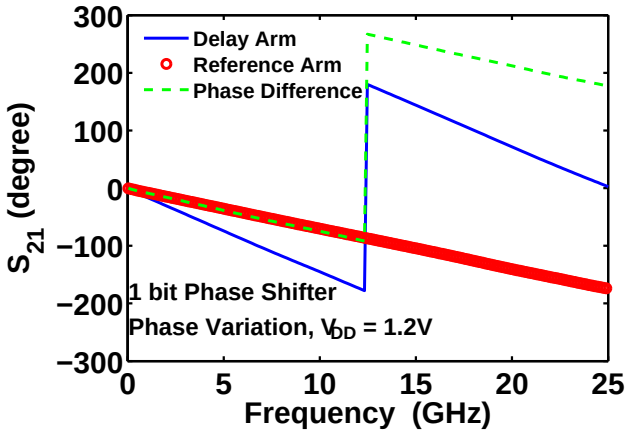


Figure 83: Variation of phase with frequency.

Table 9: Comparison of SPDT switches

Lit.	IL (dB)			Iso. (dB)	IIP_3 (dBm)
	10 GHz	15 GHz	20 GHz		
HSHG	1.4	1.7	2	>15	22.5
[53]	2.25	N/A	N/A	23	28
[52]	N/A	1.8	N/A	17.8	34.5[a]
[58]	N/A	N/A	2.5	47	N/A

[a]Uses 3 supply lines

Table 10: Comparison of phase shifters

Literature	Frequency	No. of bits	IL (dB)
This Work	19-21 GHz	1	4.5
[59]	9-15 GHz	5	15
[60]	33-35 GHz	4	14.2

capabilities, highlighting the effectiveness of the deep-trench shielding and its ability to reduce the loss of the series nMOS device.

The performance of the 1 bit phase shifter is compared to other relevant published results in Table 10. It should be noted that [59] uses nMOS with a shorted Bulk-Source connection, necessitating the use of deep NWELL and thus an extra processing step (higher cost). In addition, [60] is based on heterojunction FETs (HJFETs) for the switch elements consisting of an InGaAs channel layer sandwiched between Si-doped AlGaAs layers. This comparison shows the feasibility of building competitive K-band phase shifters with low insertion loss using MOS switches in SiGe BiCMOS technology.

4.2 SOI switch

Silicon on insulator (SOI) CMOS technologies are naturally suited for low-loss FET switches, since the isolated bulk greatly reduces the loss through the substrate. In this section, SOI CMOS switches focused on low-loss and wide bandwidth are presented. The design details and relevant trade-offs are discussed in section 4.2.1, and the measured data are presented in section 4.2.2.

4.2.1 Switch design

The designed SPDT RF switches are based on the simple series-shunt topology, as shown in Fig. 84. The transistor dimensions are chosen based on the competing requirements of insertion loss, bandwidth, and isolation. Large series devices (M1,

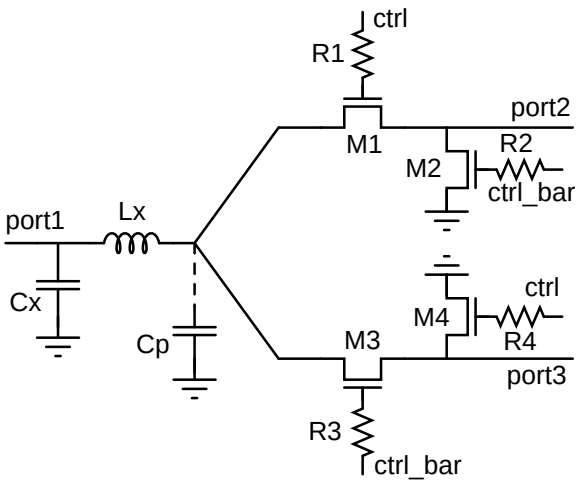


Figure 84: Schematic of the SPDT RF switch.

M3) reduce their on-resistance, and hence, insertion loss at low frequency. However, at the same time, increased parasitic capacitances due to the large devices limits the bandwidth of operation and degrades isolation. Increasing the size of the shunt devices (M2, M4) improves isolation at the cost of a slight decrease in insertion loss due to added parasitic capacitance. Two versions of the switch using low (1.5 V) and high-voltage (2.5 V) FETs were designed. For the 1.5 V design, the sizes of M1, M3 and M2, M4 are 125 μm X 0.18 μm and 40 μm X 0.18 μm, respectively. For the 2.5 V design, larger devices were used; the size of M1, M2 is 260 μm X 0.32 μm and that of M2, M4 is 105 μm X 0.32 μm. Large gate resistances (R1, R3 = 17.5 kΩ and R2,R4 = 13 kΩ) were chosen to minimize leakage through the gate.

The matching network consists of L_x and C_x (Fig. 84). The parasitic capacitances (C_p), together with the matching network, form a π-match, which improves matching and insertion loss at the higher end of the intended bandwidth (Fig. 85). The switch has perfect matching at DC, assuming all the ports are terminated with 50 Ω resistances. The matching network introduces a notch in the S_{11} response. The location of the notch depends on the values of L_x and C_x, and it should be placed such that the S_{11} stays below the required value throughout the desired range of frequencies. To maximize the matching bandwidth, the π-network was made symmetrical by setting

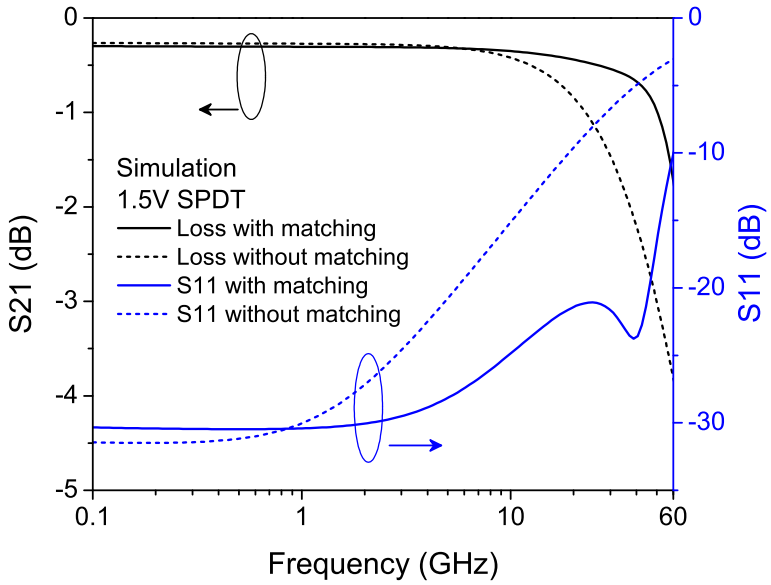


Figure 85: Simulation results showing effects of matching network on insertion loss and matching.

$C_x = C_p$. The value of the inductor (L_x) was selected based on the cut-off frequency ($1/(2\pi\sqrt{L_x C_x})$) and the location of the notch in the S_{11} response.

The P1dB of this series-shunt topology is limited by the shunt devices under negative voltage swing [46]. The simulated input P1dB of the 1.5 V switch is 11 dBm, which can prove to be insufficient for some applications. The signal handling capacity can be improved by using higher-voltage FETs, at the cost of degrading loss and reducing bandwidth. Additionally, the P1dB of this switch topology can be changed simply by changing the DC bias of the RF signal. As shown in Fig. 86, increasing the DC bias improves P1dB up to a certain point, with a corresponding increase in loss. Importantly, the DC bias can be used to change the performance of the switch post fabrication. Reconfigurable, adaptive or self-healing systems [3] can make use of such low-loss adaptive switches. For example, when used as a T/R switch, the nominal low-loss bias setting can be used in receive mode and a high-P1dB setting can be turned on in transmit mode, enabling much greater design flexibility.

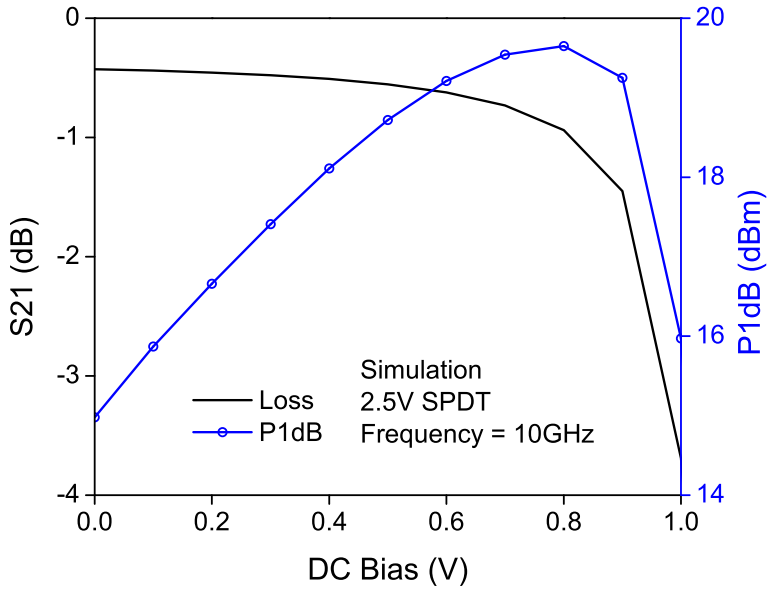


Figure 86: Simulation results showing effects of DC bias variation on insertion and signal handling capacity (P1dB).

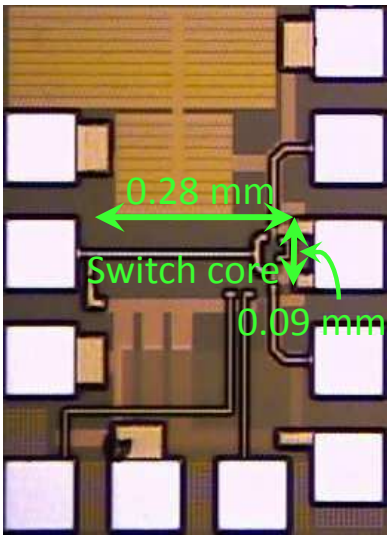


Figure 87: Die photograph of the 1.5 V SPDT RF switch.

4.2.2 Measured data

The switches were fabricated in a commercially available twin-well SOI CMOS process (IBM 7RF-SOI) on a high-resistivity (1000 Ω-cm) SOI substrate with 3 metal layers. A die photograph of the 1.5 V switch is shown in Fig. 87. The core of the chip measures 0.28 x 0.09 mm^2.

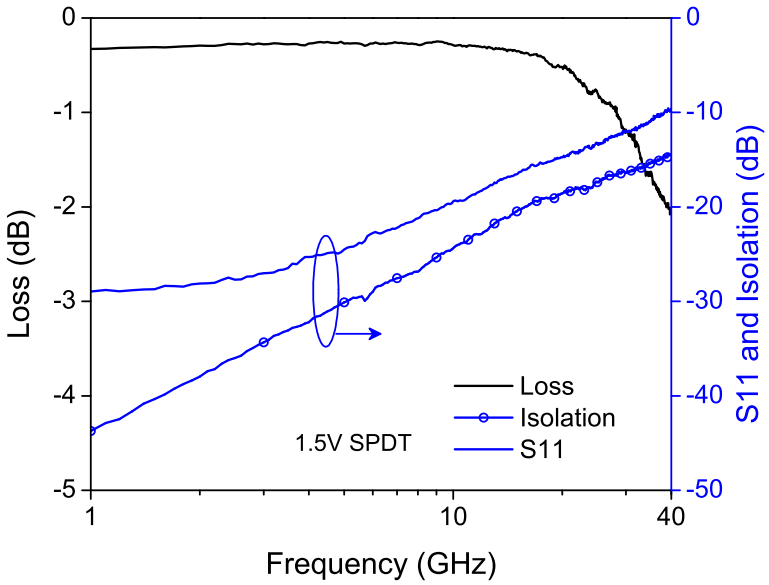


Figure 88: Measured S-parameters of the 1.5 V SPDT RF switch.

The S-parameters of the switches were measured using a VNA and de-embedded using open-short structures on wafer. Measured data of the switches under nominal conditions are plotted in Fig. 88 and Fig. 89. Loss of the 1.5 V switch is less than 0.5 dB up to 20 GHz and below 2.0 dB at 40 GHz. To the best of our knowledge, this is the best reported loss performance of any wide-band CMOS switch in this range of frequencies. The matching is better than -10 dB and the isolation is greater than 15 dB.

These SPDT RF switches are compared with other published data in Table 11. It is worth noting that some of the prior work employ additional techniques to improve certain performance metrics, requiring extra resources. For example, [61] uses a negative body bias to improve P1dB, while [46] uses LC resonance and the reported values are valid at only 35 GHz.

As an application of the switches, a one-bit, 180° switched-line phase shifter was designed at 20 GHz. The die photograph of the phase shifter is shown in Fig. 90 and the measured results are plotted in Fig. 91. As a result of the high-performance switches, the phase shifter has very low loss combined with good matching.

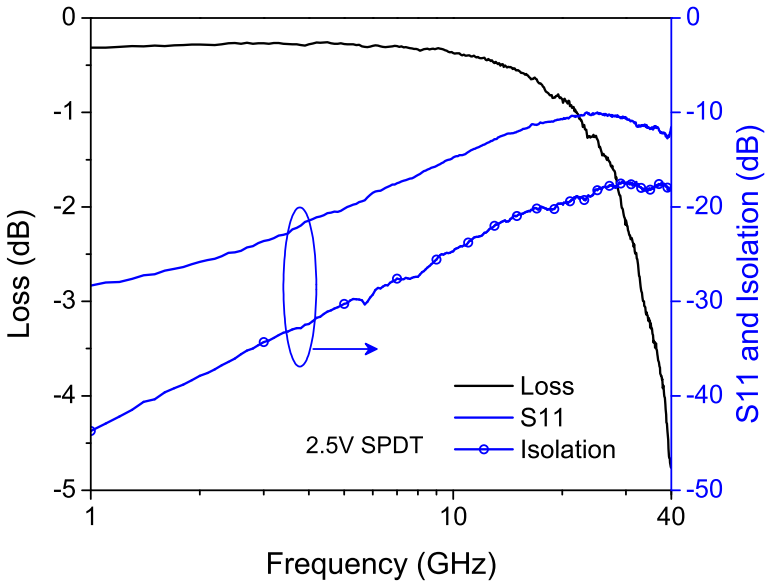


Figure 89: Measured S-parameters of the 2.5 V SPDT RF switch.

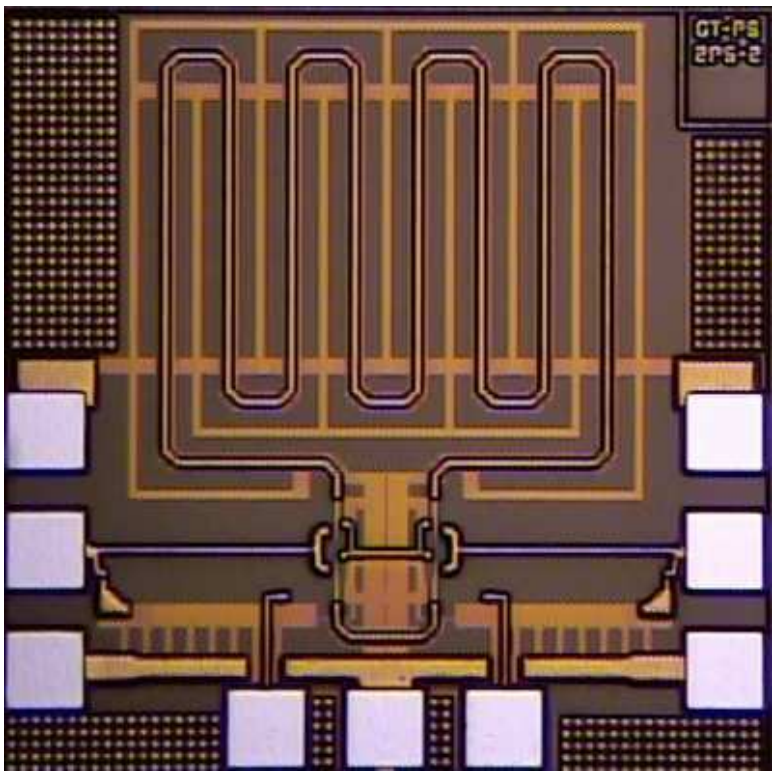


Figure 90: Die photograph of the switched-line phase shifter.

4.3 Summary

Design of low-loss switches and switched-line phase shifters were discussed in both bulk and SOI technologies.

Table 11: Comparison of SPDT switches

Ref.		BW (GHz)	Loss (dB)		Isolation (dB)	P1dB (dBm)	Technology
			DC-20 GHz	20-40 GHz			
[61]		DC-60	<2.5	<3.0	>48	17	90 nm CMOS
[46]		26-40	N/A	2.6	27	12	130 nm CMOS
[62]		DC-28	<2.0	N/A	>15	26.5	130 nm CMOS
[5]		DC-20	<2.0	N/A	>15	N/A	130 nm SiGe BiCMOS
This work	1.5 V	DC-40	<0.5	<2.0	>15	11	180 nm SOI CMOS
	2.5 V	DC-40	<1.0	<5.0	>17	15	180 nm SOI CMOS

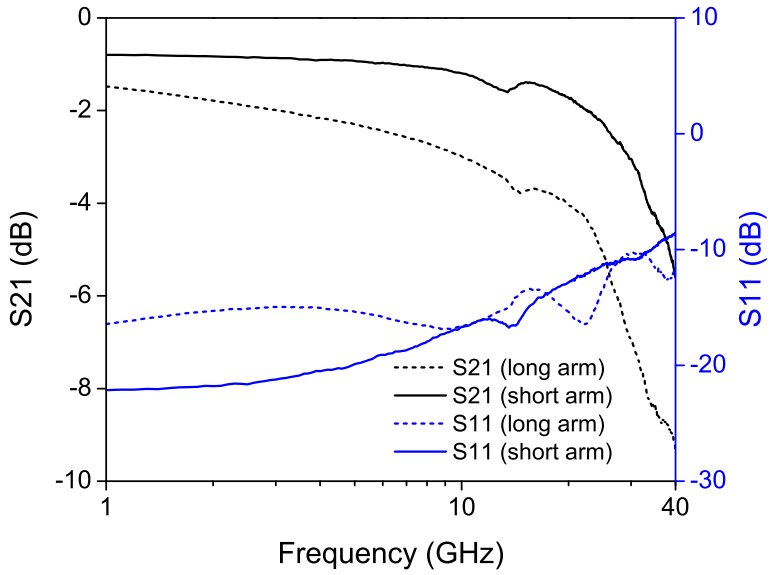


Figure 91: Measured S-parameters of the one-bit switched-line 180° phase shifter using the 1.5 V switches. The phase shifter produces 180° phase shift at 20 GHz.

For the bulk technology, various design and layout optimizations for K-band nMOS series-shunt SPDT switches were investigated. It was demonstrated that the incorporation of a deep-trench isolation ring around the series nMOS device can significantly

improve switch bandwidth and insertion loss capability. The use of an additional gate resistor also results in a modest improvement in bandwidth and insertion loss. A series-shunt SPDT switch based on these two design techniques has been investigated, demonstrating an insertion loss of -2 dB at 20 GHz, and a return loss $<$ -15 dB over the entire band of interest. A 1-bit 180° 20 GHz switched line phase shifter was designed, demonstrating the possibility of implementing high performance monolithic phased arrays in SiGe BiCMOS technology.

Two low-loss SPDT RF switches and a one-bit 180° switched-line phase shifter, implemented in a 180 nm SOI CMOS, were presented. A π-matching network was used to extend the bandwidth and reduce insertion loss. It was demonstrated that P1dB can be improved using different biasing schemes. The switches combine best-in-class loss performance with good matching, and moderate isolation.

CHAPTER V

COMPLEMENTARY SIGE OSCILLATOR

A comparison of LC cross-coupled oscillators implemented in a high-speed, complementary SiGe BiCMOS platform with matched *npn* and *pnp* performance was performed. Three oscillators (*npn*-only, *pnp*-only and complementary – *npn* + *pnp*) with the same *LC* resonant tank were designed, fabricated and tested. Results show that the complementary oscillator provides a more efficient circuit solution than its *npn*-only or *pnp*-only counterparts in terms of phase noise and power consumption. The fully monolithic complementary oscillator operating at 1.15 GHz exhibits a phase noise of -114.8 dBc/Hz at 1 MHz offset, with a corresponding FoM of 171.5, while drawing only 0.9 mA from a 3.3 V supply. The FoM of the complementary design is 5.7 dB better than that of the *npn*-only design at 1 MHz offset. The complementary SiGe oscillator also features excellent close-in phase noise performance.

Majority of the SiGe platforms offer only a high-performance *npn* SiGe HBT. Fabricating an equivalent high-performance *pnp* SiGe HBT is difficult for a number of reasons, including the lower carrier mobility of holes relative to electrons. However, having an *npn-pnp* pair with matched performance can be advantageous in many circuit contexts [63]. In low frequency analog applications, for instance, use of both *npn* and *pnp* is ubiquitous. Push-pull drivers, folded amplifier topologies, current sinks and sources, all depend on *npn-pnp* pairs. Due to the fundamental physical limitations of hole mobility and n-type valence band offsets in the *pnp* HBT, matching device performance typically requires sacrificing *npn* performance. In SiGe HBTs, matched performance is achieved by fine-tuning the germanium and doping profiles [64]. Complementary SiGe platforms are typically a generation behind leading edge *npn*-only

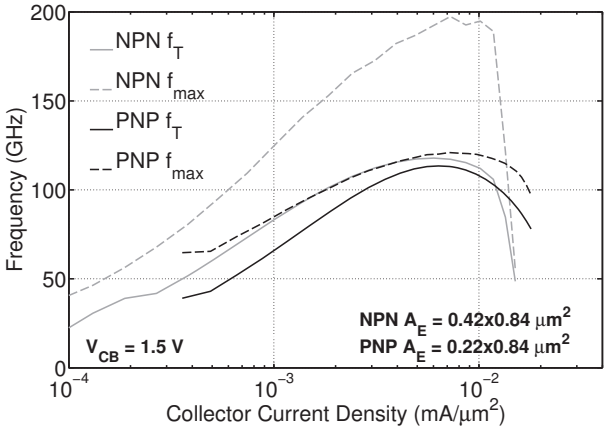


Figure 92: AC characteristics of the *npn* and *pnp* high-speed complementary SiGe HBTs.

SiGe platforms. However, with the most recent complementary SiGe platforms having matched f_T performance of around 100 GHz [65], RF applications exceeding 10 GHz are certainly well within reach.

The availability of matched SiGe *npn*-*pnp* pairs opens up new possibilities in the field of bipolar RF circuit design. In the present paper, we focus on voltage controlled oscillators (VCO), which form the core of frequency synthesizers and are thus integral parts of all communications systems. Complementary cross-coupled oscillators are common in the CMOS world [66, 67] but bipolar cross-coupled oscillators are implemented using *npn* devices [68]. In this work, three oscillators (*npn*-only, *pnp*-only and complementary) were designed and compared. The results show that the complementary design indeed offers new possibilities, delivers good phase noise performance at very low power consumption, and outperforms *npn*-only designs in terms of common oscillator figures-of-merit (FoM). Section 5.1 briefly outlines the complementary SiGe technology used for this work. A detailed circuit description can be found in section 5.2. Measured data and discussions are contained in section 5.3, followed by a summary.

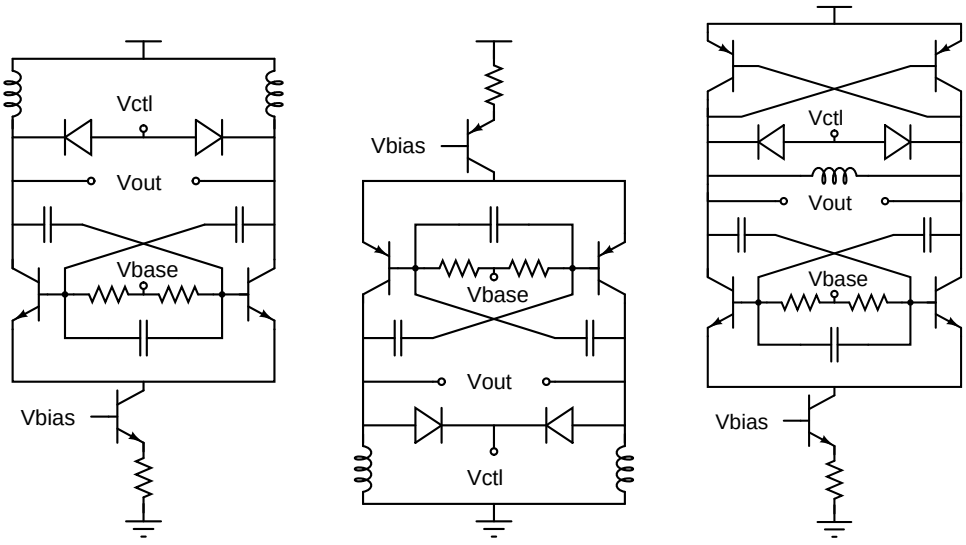


Figure 93: Schematics of the VCOs (a) *npn*-only, (b) *pnp*-only and (c) complementary.

5.1 Technology Platform

The circuits were implemented in a complementary SiGe:C BiCMOS process technology from IHP [65]. The 90 GHz f_T *pnp* and 100 GHz f_T *npn* devices were mapped onto a 0.25 μm third-generation SiGe BiCMOS platform also featuring a 200 GHz f_T high-speed *npn* SiGe HBT.

The AC performance of the *npn* and *pnp* devices is shown in Figure 92, and demonstrates their matched performance. This technology engineers the base and collector doping profile in the *pnp* to optimize heterojunction barrier effects. A novel collector design without deep trench isolation reduces parasitic capacitance and increases the overall speed of the vertical *pnp* [69]. As shown in Figure 92, while the unity current gain (f_T) is matched fairly well between the *npn* and *pnp*, the *npn* still exhibits a noticeably higher maximum oscillation frequency, f_{max}. In addition, the complementary devices have almost identical output impedances at a fixed collector current. The fixed output impedance ensures that the loaded Q of the resonators remains comparable for both the *npn* and *pnp* oscillators. The *pnp* SiGe HBT has a significantly higher $1/f$ corner frequency than the *npn* HBT. Beyond the $1/f$ noise

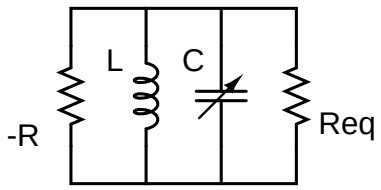


Figure 94: Conceptual model of LC cross-coupled oscillators.

corner where thermal noise dominates, an S-parameter extraction of the base resistance shows that the *pnp* resistance is around 250 Ω. while the *npn* base resistance is around 170 Ω. In terms of noise power, this is a difference of 1.7 dB in favor of the *npn* SiGe HBT. Another critical difference lies in the DC current gain of the devices. The *pnp* HBT has a peak β of 100 versus 200 for the matched *npn* HBT.

5.2 Circuit Description

Three oscillator designs were implemented in this C-SiGe platform, with schematics shown in Figure 93. The cross-coupled oscillator topology is a common integrated circuit design and allows direct bias control of the oscillating devices via the collector current. All three oscillators were designed to have identical *LC* resonators and device sizes to facilitate meaningful comparisons of the device performances. All of the oscillators use monolithically integrated resonators with an unloaded Q of 10.7. The emitter area of the *npn* and *pnp* devices used in the design are 8X(0.42X0.84) μm^2 and 8X(0.22X0.84) μm^2, respectively. Both devices have a peak f_T of about 90 GHz at a collector current of 8 mA.

A conceptual model of the LC cross-coupled oscillator is shown in Figure 94. The loss resistance of the *LC* resonator is modeled as R_{eq}. The negative resistance represents the energy put into the circuit by the active devices (i.e., the cross-coupled pair) and is given by

$$-R = \frac{2}{g_m}. \tag{16}$$

The start-up condition can be expressed as $|-R| < R_{eq}$. Since the complementary

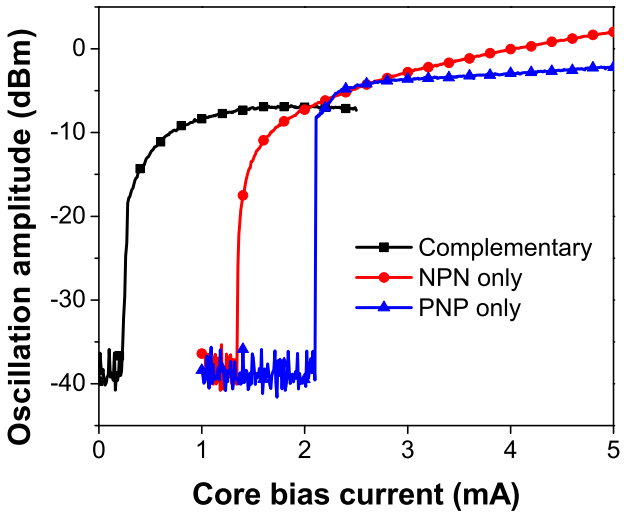


Figure 95: Power characteristics of the complementary, *npn*, and *pnp* VCOs across bias current.

topology reuses the same current and provides more transconductance compared to the *npn*-only or *pnp*-only designs, it should be more efficient in terms of power consumption.

5.3 Measurement results

A die photograph of the complementary SiGe VCO is shown in Figure 96. Frequency and power characteristics of the oscillators were measured using a spectrum analyzer. Phase noise was measured using a custom-designed setup using the delay line techniques. This technique is ideal for free-running oscillator measurements because it nullifies the effects of frequency bounce, allowing close-in phase noise measurements.

The power characteristics across bias current are plotted in Figure 95. As expected, the complementary VCO starts oscillating and reaches its peak amplitude at a much lower current compared to the others. The maximum amplitude of oscillation for the complementary VCO is less than its *npn*-only or *pnp*-only counterparts as it is limited by two cross-coupled pairs at both rails (Figure 93), whereas for the other two, the oscillation is allowed to grow beyond the rail.

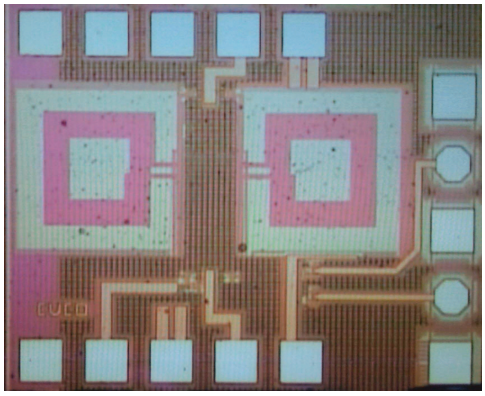


Figure 96: Die photograph of the complementary SiGe VCO.

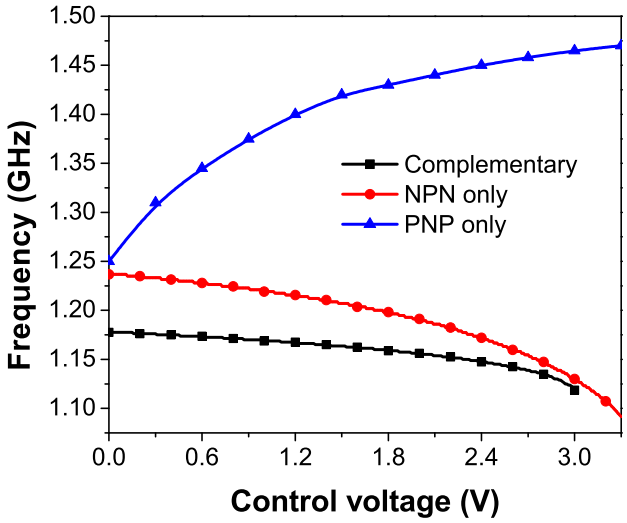


Figure 97: Frequency characteristics of the complementary, *npn*, and *pnp* VCOs for different control voltages.

Frequency characteristics of the VCOs across control voltages are plotted in Figure 97. The *npn* and *pnp* VCOs have a tuning range of about 150 MHz and 200 MHz, respectively. The tuning range of the complementary VCO is about 60 MHz. The reduced tuning range for the complementary design, despite using an identical resonators and varactors, can be attributed to the larger capacitance contributed by the cross-coupled pairs.

5.3.1 Phase Noise Performance

Figure 98 compares the SSB phase noise of the VCOs at a constant control voltage of 0 V. The core bias currents for each VCO were chosen to minimize the phase noise. The complementary VCO was biased at 0.9 mA and the other two were operating at 5 mA. Despite operating at a much lower current level and lower oscillation amplitude (Figure 95), the phase noise of the complementary VCO is close to the *npn*-only and *pnp*-only in the $1/f^2$ region of the phase noise plot. At 1 MHz offset, the phase noise for the complementary, *npn* and *pnp* VCOs are -114.8, -116.2 and -118.9 dBc/Hz, respectively. In this white noise region, the *pnp*-only VCO has the best phase noise performance. This is counter-intuitive, given the superiority of *npn* over *pnp* devices. The reason behind this unusual result can be explained by lower current gain (β) of the *pnp*s compared to the *npn*s. Lower β results in lower total output referred noise at the collector, which translates into phase noise. More detail about the improved phase noise performance of the *pnp*-only design in the white noise region can be found in [70].

At close-in offsets, however, the phase noise of the *pnp*-only VCO is markedly worse due to higher flicker noise contribution from the *pnp* devices. The complementary design, despite having a *pnp* cross-coupled pair, performs as well as the *npn*-only design and is actually better at offsets less than 10 kHz. This is due to better symmetry of the oscillating waveform for the complementary design. As explained in [71] using impulse sensitivity function (ISF), symmetry of the waveform affects phase noise performance in the flicker noise dominated region and hence the complementary VCOs perform better than unbalanced topologies. In this case, the effect of symmetry was enough to more than compensate for the inherently higher flicker noise of the *pnp* devices.

The complementary SiGe VCO delivers good phase noise performance while consuming 5 times less current than the *npn*-only or *pnp*-only designs. To underscore the

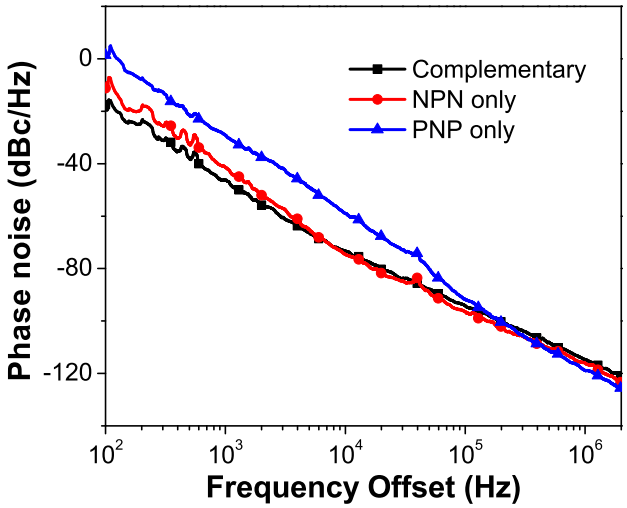


Figure 98: Measured phase noise of the VCOs at constant control voltage ($V_{ctl} = 0V$). The complementary VCO, despite operating at much lower bias current (0.9 mA) as compared to the *npn*-only and *pnp*-only VCOs (5 mA), has comparable phase noise in the $1/f^2$ region and performs better at close-in offsets.

importance of this point, the VCOs were compared based on a figure-of-merit (FoM) that combines phase noise and power consumption and compensates for variations in oscillation frequency [72]. The FoM is defined as

$$FoM = \left(\frac{f_0}{f_m}\right)^2 . \frac{1}{L(f_m).V_{CC}.I(mA)}, \tag{17}$$

where f_0 is the frequency of oscillation, f_m is the offset frequency, $L(f_m)$ is the phase noise at the specified offset, V_{CC} is the supply voltage, and I is the current drawn from the supply.

The FoMs of the VCOs at 1 MHz offset across bias currents are plotted in Figure 99. Clearly, the complementary design achieves the best figure-of-merit while consuming much lower power. The complementary VCO FoM is better than the *npn*-only design by about 5.7 dB. At lower offset frequencies, the gap between the two will widen even more.

These results successfully demonstrate the advantages of complementary bipolar VCOs. It should be noted that in this work our focus was on comparing different VCO

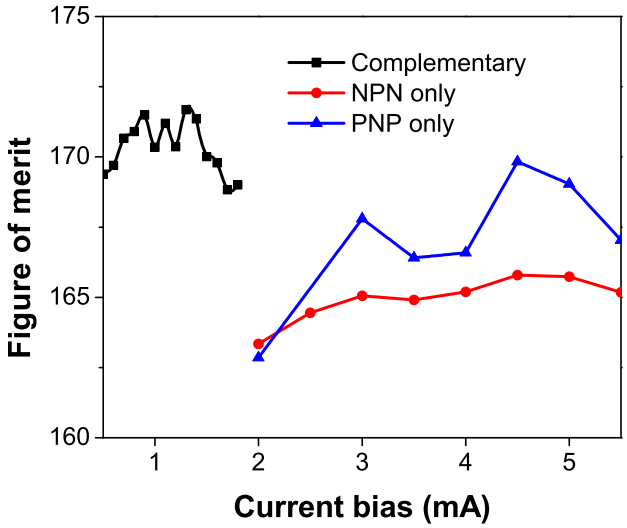


Figure 99: Comparison of FoM (Eqn.17) of the VCOs based on phase noise at 1 MHz offset. The complementary VCO outperforms both the *npn*-only and *pnp*-only designs while operating at much lower power.

topologies and there are additional opportunities for further improving this complementary VCO design. The *pnp* pair was directly cross-coupled as opposed to normal capacitive coupling used in bipolar oscillators to ensure a stable DC operating point. Direct cross-coupling results in the entire output amplitude appearing across the base-emitter junction and limits the signal amplitude. A way around this limitation would be to use capacitive coupling while implementing a separate common-mode feedback (CMFB) loop to take care of the DC operating point, as demonstrated in [73]. In addition, optimizing the design of the inductor [72] and the use of noise suppression techniques [66] can further improve overall performance of the C-SiGe oscillator.

5.4 Summary

A comparison of cross-coupled VCO designs in a high-speed C-SiGe process has shown that the phase noise performance of the complementary VCO is comparable to the *npn*-only or *pnp*-only implementations while consuming much less power. Based on a figure-of-merit which combines phase noise performance with power consumption, the complementary design significantly outperforms the unbalanced designs. The

complementary design has lower output power and tuning range; however, in many applications the lower power consumption and better close-in phase noise are expected to provide signficant advantages.

CHAPTER VI

CONCLUSION

6.1 Summary of Contributions

The purpose of this research is to develop high-frequency circuits and systems that are capable of delivering consistent performance even under the threat of increasing process variation in aggressively scaled fabrication technologies. The research is aimed at the emerging class of "self-healing" high-frequency circuits. The primary goal of the "self-healing" circuits is to mitigate the effects of process variations and increase yield. But the scope of application of this type of intelligent, adaptive circuits is much broader. The long-term vision is to design circuits that are flexible and intelligent enough to adapt to the effects of process variation, changing environments, and multiple standards on their own in a monolithically integrated form.

The approach adopted here is to combine high-performance tunable circuits with digital processing to achieve the desired flexibility. Tunable circuit solutions and healing algorithms that work harmoniously to improve performance were developed and demonstrated. The specific contributions of this research are summarized as follows:

1. An adaptive wideband (6-20 GHz) image-reject mixer, suitable for use in a self-healing receiver, was designed. Automated simultaneous healing of multiple circuit parameters (gain, IRR, and linearity) was demonstrated in measurement [1–3].

2. A monte-carlo simulation based methodology for verification of healing was developed. Using this method, a custom healing algorithm can be applied to a circuit and its success rate and efficiency can be determined in a statistically

significant way. The method was applied to the image-reject mixer and it was shown that the healing methods were able to improve yield significantly.

3. Circuits and algorithms were designed to achieve high image rejection ratio (IRR) over a wide bandwidth. It was shown that for image reject architectures using polyphase filters, the effect of pole shift within the filter on the IRR has unique properties and cannot be healed by gain or phase compensation outside the filter. A tunable polyphase filter was designed to compensate for the pole shift. An IRR of 60 dB over 140 MHz of bandwidth with an yield of 98% was achieved after healing using the monte-carlo based method.

4. A wideband (3-26 GHz) SiGe low-noise amplifier was designed. It was shown that the performance of the resistive feedback LNA can be enhanced by using small reactive elements with little area penalty [4].

5. Low-loss switches were implemented in bulk and silicon-on-insulator (SOI) technologies. The insertion loss of the bulk switches were reduced by using deep trench to isolated the bulk of the devices [5].

6. SPDT switches were designed in SOI CMOS technology. The insertion loss of the SOI switch with an operating voltage of 1.5V was measured to be less than 0.5 dB upto frequency of 20 GHz. To the best of the author's knowledge, this is the lowest among all published wideband CMOS switches.

6.2 Future Work

The field of self-healing circuits is very young. Although concepts related to process variation tolerance has always been a part of robust circuit design, the applications in the field of high-frequency designs have been limited. Great things are to be expected as we continue to explore the horizons of intelligent circuits.

The mixed signal approach of integrating the flexibility of digital processing with high-frequency circuits has a lot of potential for a variety of applications.

The interaction between circuits and the healing algorithms can be explored in depth. In this work, algorithms specific to the circuits were used with success. But such algorithms cannot be readily applied to other circuits and may have to be developed from scratch for another circuit topology. On the other hand, a more generic algorithm may suffer from lower success rate and less efficiency. The question of optimum co-design of circuits and healing algorithms needs more exploration.

The IRR healing of the mixer in this work ignores the mismatch of components within the polyphase filter. IRR can be improved further if those mismatches can be nullified.

REFERENCES

[1] P. K. Saha and J. D. Cressler, "A tunable, SiGe X-band image reject mixer," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Oct. 2010, pp. 196–199.

[2] P. K. Saha, D. Howard, S. Shankar, R. Diestelhorst, T. England, and J. D. Cressler, "An adaptive, wideband SiGe image reject mixer for a self-healing receiver," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2011, pp. 99–102.

[3] P. K. Saha, D. C. Howard, S. Shankar, R. Diestelhorst, T. England, and J. D. Cressler, "A 6-20 GHz adaptive SiGe image reject mixer for a self-healing receiver," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1998–2006, 2012.

[4] P. K. Saha, S. Shankar, R. Schmid, R. Mills, and J. D. Cressler, "Analysis and design of a 3-26 GHz low-noise amplifier in SiGe HBT technology," in *IEEE Radio and Wireless Symposium Digest*, 2012, pp. 203–206.

[5] P. K. Saha, J. P. Comeau, W. M. Kuo, and J. D. Cressler, "A K-band nMOS SPDT switch and phase shifter implemented in 130 nm SiGe BiCMOS technology," in *Proc. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2009, pp. 1–4.

[6] C. A. Mack, "Fifty years of Moore's law," *IEEE Transactions on Semiconductor Manufacturing*, vol. 24, no. 2, pp. 202–207, May 2011.

[7] R. Schaller, "Moore's law: past, present and future," *IEEE Spectrum*, vol. 34, no. 6, pp. 52–59, Jun. 1997. [Online]. Available: http://ieeexplore.ieee.org.www.library.gatech.edu:2048/xpl/downloadCitations

[8] G. Moore, "Lithography and the future of Moore's law," in *Proc. of SPIE*, vol. 2438, 1995, p. 2.

[9] G. E. Moore, "No exponential is forever: but forever can be delayed! [semiconductor industry]," in *IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers*, 2003, pp. 20– 23 vol.1.

[10] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, and V. De, "Parameter variations and impact on circuits and microarchitecture," in *Proc. Design Automation Conference*, 2003, pp. 338–42.

[11] D. Sylvester, D. Blaauw, and E. Karl, "ElastIC: an adaptive Self-Healing architecture for unpredictable silicon," *IEEE Design & Test of Computers*, vol. 23, no. 6, pp. 484–490, Jun. 2006.

[12] E. Fetzer, "Using adaptive circuits to mitigate process variations in a microprocessor design," *IEEE Design and Test of Computers*, vol. 23, no. 6, pp. 476–483, Jun. 2006.

[13] S. Mukhopadhyay, K. Kim, H. Mahmoodi, and K. Roy, "Design of a process variation tolerant Self-Repairing SRAM for yield enhancement in nanoscaled CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1370–1382, Jun. 2007.

[14] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "90-nm Process-Variation adaptive embedded SRAM modules with Power-Line-Floating write technique," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 705–711, Mar. 2006.

[15] S. K. Devarakond, V. Natarajan, S. Sen, and A. Chatterjee, "BIST-assisted power aware self healing RF circuits," in *Proc. IEEE 15th International Mixed-Signals, Sensors, and Systems Test Workshop*, Jun. 2009, pp. 1–4.

[16] S. Sen and A. Chatterjee, "Design of process variation tolerant radio frequency low noise amplifier," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008, pp. 392–395.

[17] A. Tasic, S. Lim, W. A. Serdijn, and J. R. Long, "Design of adaptive multimode RF Front-End circuits," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 2, pp. 313–322, Feb. 2007.

[18] A. Goyal, M. Swaminathan, and A. Chatterjee, "Self-correcting, self-testing circuits and systems for post-manufacturing yield improvement," in *Proc. IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2011, pp. 7–10.

[19] ——, "Self-calibrating embedded RF down-conversion mixers," in *Proc. Asian Test Symposium*, Nov. 2009, pp. 249–254.

[20] J. D. Cressler, *Silicon heterostructure handbook: materials, fabrication, devices, circuits, and applications of SiGe and Si strained-layer epitaxy.* CRC Press, 2006.

[21] J. D. Cressler and G. Niu, *Silicon-germanium heterojunction bipolar transistors.* Artech House, Jun. 2003.

[22] D. Porcino and W. Hirt, "Ultra-wideband radio technology: potential and challenges ahead," *IEEE Communications Mag.*, vol. 41, no. 7, pp. 66–74, Jul. 2003.

[23] Y. Park, C. Lee, J. Cressler, J. Laskar, and A. Joseph, "A very low power SiGe LNA for UWB application," in *Tech. Dig. IEEE MTT-S Int. Microwave Symp.*, Jun. 2005, pp. 1041–1044.

[24] Y. Lu, R. Krithivasan, W. L. Kuo, and J. Cressler, "A 1.8–3.1 dB noise figure (3–10 GHz) SiGe HBT LNA for UWB applications," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2006, pp. 45–49.

[25] J. Lee and J. Cressler, "Analysis and design of an ultra-wideband low-noise amplifier using resistive feedback in SiGe HBT technology," *IEEE Trans. on Microwave Theory and Tech.*, vol. 54, no. 3, pp. 1262–1268, Mar. 2006.

[26] Y. Lin, H. Chen, T. Wang, Y. Lin, and S. Lu, "3–10-GHz Ultra-Wideband Low-Noise amplifier utilizing miller effect and inductive Shunt–Shunt feedback technique," *IEEE Trans. on Microwave Theory and Tech.*, vol. 55, no. 9, pp. 1832–1843, Sep. 2007.

[27] H. Chen, Y. Lin, and S. Lu, "Analysis and design of a 1.6–28-GHz compact wideband LNA in 90-nm CMOS using a π-Match input network," *IEEE Trans. on Microwave Theory and Tech.*, vol. 58, no. 8, pp. 2092–2104, Aug. 2010.

[28] P. Chang and S. Hsu, "A compact 0.1–14-GHz Ultra-Wideband Low-Noise amplifier in 0.13- μm CMOS," *IEEE Trans. on Microwave Theory and Tech.*, vol. 58, no. 10, pp. 2575–2581, Oct. 2010.

[29] M. Chen and J. Lin, "A 0.1–20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm digital CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 5, pp. 323–325, May 2009.

[30] C. Liao and S. Liu, "A broadband Noise-Canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[31] M. Okushima, J. Borremans, D. Linten, and G. Groeseneken, "A DC-to-22 GHz 8.4mW compact dual-feedback wideband LNA in 90 nm digital CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2009, pp. 295–298.

[32] M. Chen, W. Sutton, I. Smorchkova, B. Heying, W. Luo, V. Gambin, F. Oshita, R. Tsai, M. Wojtowicz, R. Kagiwada, A. Oki, and J. Lin, "A 1–25 GHz GaN HEMT MMIC Low-Noise amplifier," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 10, pp. 563–565, Oct. 2010.

[33] D. Howard, J. Poh, T. Mukerjee, and J. Cressler, "A 3–20 GHz SiGe HBT ultra-wideband LNA with gain and return loss control for multiband wireless applications," in *Proc. 53rd IEEE Int. Midwest Symp. on Circuits and Systems*, Aug. 2010, pp. 445–448.

[34] B. Razavi, *RF microelectronics*. Prentice Hall, 1998.

[35] J. Crois and M. Steyaert, "A fully integrated 900 MHz CMOS double quadrature downconverter," in *Proceedings ISSCC*, 1995, pp. 136–137.

[36] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.

[37] B. Gilbert, "The MICROMIXER: a highly linear variant of the gilbert mixer using a bisymmetric class-ab input stage," *IEEE Journal of Solid-State Circuits,*, vol. 32, no. 9, pp. 1412–1423, 1997.

[38] ——, "The multi-tanh principle: a tutorial overview," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 2–17, 1998.

[39] P. van Lieshout and R. van de Plassche, "A monolithic wideband variable gain amplifier with a high gain range and low distortion," in *Digest of Technical Papers, IEEE International Solids-State Circuits Conference*, 1997, pp. 358–359.

[40] S. Galal, H. Ragaie, and M. Tawfik, "RC sequence asymmetric polyphase networks for RF integrated transceivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 1, pp. 18–27, 2000.

[41] S. Yue, D. Ma, and J. Long, "A 17.1-17.3-GHz image-reject downconverter with phase-tunable LO using 3 times; subharmonic injection locking," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2321 – 2332, Dec. 2004.

[42] R. Montemayor, "A 410-mW 1.22-GHz downconverter in a dual-conversion tuner IC for OpenCable applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 714 – 718, April 2004.

[43] B. Jackson and C. Saavedra, "A dual-band self-oscillating mixer for C-band and X-band applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 58, no. 2, pp. 318 –323, Feb. 2010.

[44] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A 20-32-GHz wideband mixer with 12-GHz IF bandwidth in 0.18-μm SiGe process," *IEEE Trans. Microwave Theory and Techniques*, vol. 58, no. 11, pp. 2731 –2740, Nov. 2010.

[45] X. J. Li and Y. P. Zhang, "Flipping the CMOS switch," *IEEE Microw. Mag.*, vol. 11, no. 1, pp. 86–96, 2010.

[46] B.-W. Min and G. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 6, pp. 1364–1371, 2008.

[47] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 31–39, 2006.

[48] Z. Zhao et al., "Ferroelectric phase shifters at 20 and 30 ghz," *IEEE Trans. on MTT-S*, vol. 55, no. 2, pp. 430–437, Feb. 2007.

[49] Y. Yue et al., "A millimeter-wave 4-bit digital phase shifter," *Asia-Pacific Microwave Conference Proceedings*, vol. 2, pp. pp. 4–7, Dec. 2005.

[50] V. Sokolov et al., "A Ka-band GaAs monolithic phase shifter," *IEEE Trans. on Elec. Devices*, vol. 30, no. 12, pp. 1855–1861, Dec 1983.

[51] G. Rebeiz, G.-L. Tan, and J. S. Hayden, "RF MEMS phase shifters: design and applications," *IEEE Microwave Magazine*, vol. 3, no. 2, pp. 72–81, Jun 2002.

[52] Z. Li and K. K. O, "15-GHz fully integrated nMOS switches in a 0.13 μm CMOS process," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2323–2328, Nov. 2005.

[53] W. M. Kuo, J. P. Comeau, J. M. Andrews, J. D. Cressler, and M. A. Mitchell, "Comparison of shunt and series/shunt nMOS single-pole double-throw switches for X-band phased array T/R modules," in *Proc. Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 2007, pp. 249–252.

[54] M.-C. Yeh, R.-C. Liu, Z.-M. Tsai, and H. Wang, "A miniature low-insertion-loss, high-power CMOS SPDT switch using floating-body technique for 2.4- and 5.8-GHz applications," in *in IEEE RFIC Symposium Dig. Papers*, June 2005, pp. 451–454.

[55] Z. Li, H. Yoon, F.-J. Huang, and K. O, "5.8-GHz CMOS T/R switches with high and low substrate resistances in a 0.18-μm CMOS process," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 1, pp. 1–3, Jan 2003.

[56] J. Comeau, J. Cressler, and M. Mitchell, "Design and layout techniques for the optimization of nMOS SPDT series-shunt switches in a 130 nm SiGe BiCMOS technology," in *IEEE RFIC Symposium Dig. Papers*, June 2007, pp. 457–460.

[57] B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. Greenberg, R. Groves, S. Jeng, J. Johnson, E. Mengistu, K. Schonenberg, C. Schnabel, P. Smith, A. Stricker, D. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{MAX} and 207 GHz f_t in a manufacturable technology," *IEEE Electron Device Letters*, vol. 23, no. 5, pp. 258–260, May 2002.

[58] D. Yongsheng, X. Chen, C. Tangsheng, Y. Lijie, L. Lin, G. Shuping, L. Hui, and L. Jinting, "Reflect type DC-20 GHz MMIC high performance SPST and SPDT switches," in *2nd International Conference on Microwave and Millimeter Wave Technology*, 2000, pp. 211–214.

[59] D.-W. Kang, H. D. Lee, C.-H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Trans. on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 294–301, Jan. 2006.

[60] K. Maruhashi, H. Mizutani, and K. Ohata, "A Ka-band 4-bit monolithic phase shifter using unresonated FET switches," in *IEEE RFIC Symposium Dig. Papers*, Jun 1998, pp. 191–194.

[61] H.-Y. Chang and C.-Y. Chan, "A low loss high isolation DC-60 GHz SPDT traveling-wave switch with a body bias technique in 90 nm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 82–84, 2010.

[62] Q. Li, Y.-P. Zhang, K.-S. Yeo, and W. M. Lim, "16.6- and 28-GHz fully integrated CMOS RF switches with improved body floating," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 2, pp. 339–345, 2008.

[63] J. D. Cressler, "Issues and opportunities for complementary SiGe HBT technology," in *Proceedings of the 2006 Electrochemical Society Symposium on SiGe and Ge: Materials, Processing, and Devices*, 2006, pp. 893–912.

[64] G. Zhang, J. D. Cressler, G. Niu, and A. Pinto, "A comparison of npn and pnp profile design tradeoffs for complementary SiGe HBT technology," *Solid-State Electronics*, vol. 44, no. 11, pp. 1949–1954, Nov. 2000.

[65] B. Heinemann, R. Barth, D. Bolze, J. Drews, P. Formanek, O. Fursenko, M. Glante, K. Glowatzki, A. Gregor, U. Haak, W. Hoppner, D. Knoll, R. Kurps, S. Marschmeyer, S. Orlowski, H. Rucker, P. Schley, D. Schmidt, R. Scholz, W. Winkler, and Y. Yamamoto, "A complementary BiCMOS technology with high speed npn and pnp SiGe:C HBTs," in *Technical Digest of IEEE International Electron Devices Meeting*, Dec. 2003, pp. 5.2.1– 5.2.4.

[66] A. Ismail and A. A. Abidi, "CMOS differential LC oscillator with suppressed up-converted flicker noise," in *Digest of Technical Papers. IEEE International Solid-State Circuits Conference (ISSCC)*, 2003, pp. 98– 99 vol.1.

[67] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[68] J. H. Zhan, K. Maurice, J. Duster, and K. T. Kornegay, "Analysis and design of negative impedance LC oscillators using bipolar transistors," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 11, pp. 1461– 1464, Nov. 2003.

[69] B. Heinemann, H. Rucker, R. Barth, J. Bauer, D. Bolze, E. Bugiel, J. Drews, K. E. Ehwald, T. Grabolla, U. Haak, W. Hoppner, D. Knoll, D. Kruger, B. Kuck, R. Kurps, M. Marschmeyer, H. H. Richter, P. Schley, D. Schmidt, R. Scholz, B. Tillack, W. Winkler, D. Wolnsky, H. E. Wulf, Y. Yamamoto, and P. Zaumseil, "Novel collector design for high-speed SiGe:C HBTs," in *Digest of International Electron Devices Meeting*, 2002, pp. 775– 778.

[70] S. J. Horst, P. Chakraborty, P. Saha, J. D. Cressler, H. Gustat, B. Heinemann, G. G. Fischer, D. Knoll, and B. Tillack, "A comparison of npn vs. pnp SiGe

HBT oscillator phase noise performance in a complementary SiGe platform," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 2010, pp. 13–16.

[71] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[72] M. Tiebout, "A fully integrated 1.3 GHz VCO for GSM in 0.25 μm standard CMOS with a phase noise of –142 dBc/Hz at 3 MHz offset," in *30th European Microwave Conference*. IEEE, Oct. 2000, pp. 1–4.

[73] P. K. Saha, A. Dutta, A. Patra, and T. K. Bhattacharyya, "Design of a 1 V low power 900 MHz QVCO," in *IEEE 19th International Conference on VLSI Design*, Jan. 2006.

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