FABRICATION TECHNOLOGY AND DESIGN FOR CMUTS ON CMOS FOR IVUS CATHETERS

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FABRICATION TECHNOLOGY AND DESIGN FOR CMUTS ON CMOS FOR IVUS CATHETERS

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1. ASIC – Application-specific integrated circuit
2. BEM – Boundary element method
3. CMOS – Complementary metal oxide semiconductor
4. CMUT – Capacitive micromachined ultrasonic transducer
5. CTO – Chronic total occlusion
6. DEMUX – Demultiplexer
7. DOF – Depth of field
8. DRA – Dual ring array
9. FEA – Finite element analysis
10. FL – Forward looking
11. FPGA – Field-programmable gate array
12. ICE – Intracardiac echocardiography
13. IVUS – Intravascular ultrasound
14. LPCVD – Low pressure chemical vapor depostion
15. MIMO – Multiple-input multiple-output
16. MISO – Multiple-input single-output
17. MUX – Multiplexer
18. NDE – Non-destructive evaluation
19. PCB – Printed circuit board
20. PECVD – Plasma enhanced chemical vapor deposition
21. PZT – Lead zirconate titanate
22. SL – Side looking
23. SMA – SubMiniature version A (connector)
24. SNR – Signal-to-noise ratio

25. TAVI – Transcatheter aortic valve implantation
26. TIA – Transimpedance amplifier
27. TSMC – Taiwan Semiconductor Manufacturing Company Limited
28. TSV – Through silicon via
29. RIE – Reactive ion etching
30. Rx – Receive
31. Tx – Transmit

SUMMARY

The objective of this research is to develop novel capacitive micromachined ultrasonic transducer (CMUT) arrays for intravascular ultrasonic (IVUS) imaging along with the fabrication processes to allow for monolithic integration of CMUTs with custom CMOS electronics for improved performance. The IVUS imaging arrays include dual-ring arrays for forward-looking volumetric imaging in coronary arteries and annular-ring arrays with dynamic focusing capabilities for side-looking cross sectional imaging applications. Both are capable of integration into an IVUS catheter 1-2 mm in diameter.

The research aim of monolithic integration of CMUTs with custom CMOS electronics has been realized mainly through the use of sloped sidewall vias less than 5 μm in diameter, with only one additional masking layer as compared to regular CMUT fabrication. Fabrication of CMUTs has been accomplished with a copper sacrificial layer reducing isolation layers by 50%.

Modeling techniques for computational efficient analysis of CMUT arrays were developed for arbitrary geometries and further expanded for use with larger signal analysis.

Dual-ring CMUT arrays for forward-looking volumetric imaging have been fabricated with diameters of less than 2 mm with center frequencies at 10 MHz and 20 MHz, respectively, for an imaging range from 1 mm to 1 cm. These arrays, successfully integrated with custom CMOS electronics, have generated 3D volumetric images with only 13 cables necessary. Performance from optimized fabrication has reduced the bias required for a dual-ring array element from 80 V to 42 V and in conjunction with a full electrode transmit array, it was shown that the SNR can be improved by 14 dB. Simulations were shown to be in agreement with experimental characterization indicated transmit surface pressure in excess of 8 MPa.

For side-looking IVUS, three versions of annular CMUT arrays with dynamic focusing capabilities have been fabricated for imaging 1 mm to 6 mm in tissue. These arrays are 840 μm in diameter membranes linked to form 8 ring elements with areas that deviate by less than 25 %. Through modeling and simulation undesirable acoustic cross between ring elements was reduced from -13 dB to -22 dB.

CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1. Motivation

Heart disease in its various forms is the leading cause of death in developed countries, and as such, the diagnosis and treatment with non-invasive techniques is of particular interest [1]. Based on 2007 mortality statistics in the United States, 2200 people die each day from cardiovascular disease claiming more lives than cancer, chronic lower respiratory disease, and all accidents combined [2].

Angiography remains a standard medical imaging technique for the diagnosis of heart disease through where an X-ray absorbing contrast agent is inserted into the blood vessel while X-ray imaging techniques such as fluoroscopy are used to evaluate the flow of blood [3, 4]. Figure 1 shows two example angiograms with normal blood flow on the left and a clogged coronary artery indicated in the image on the right [5, 6]. While this method accurately shows the flow inside of the vessel, it fails to show any information about the arterial wall itself, and it subjects the patients to potentially harmful radiation [7].

To assist in the diagnosis and treatment of heart disease where the angiogram is unclear, specialized catheters with ultrasonic imaging capabilities were developed with the ability to provide a cross-sectional image equating to a plane perpendicular to the catheter tip [3, 8]. The following summarizes current intravascular ultrasound (IVUS) technology, discusses common medical interventions assisted by IVUS and identifies physical catheter constraints.

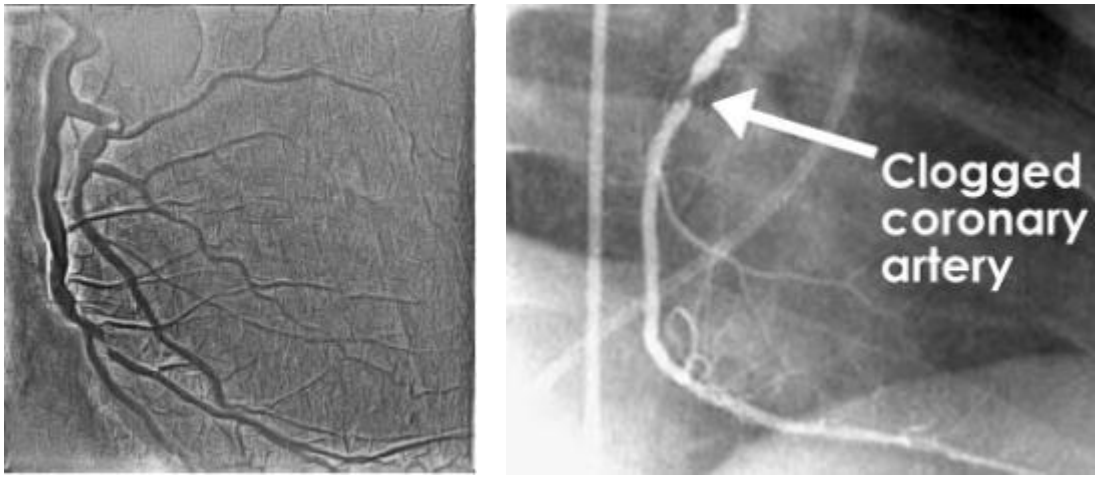


Figure 1. Sample angiograms from a fluoroscopic procedure showing the blood flow through the vessels (left) and a clogged coronary artery (right) [5, 6].

1.2. IVUS Catheters

Since their first appearance in the late 1990's, piezoelectric based IVUS has become an accepted tool for coronary and vascular imaging to assist in the diagnosis and treatment of heart disease with a single mechanically scanned transducer or a multi-element electronically steerable assembly as shown in Figure 2 [9]. To date, all commercially available ultrasonic imaging catheters are based upon piezoelectric transducer technology with fabrication techniques that typically require thinning of a piezoelectric substrate and subsequent dicing. The shapes and sizes producible are limited by the capabilities of the dicing and handling. The ability to process and handle smaller piezoelectric samples is a major avenue of current research including such process as thin film deposition and laser dicing [10, 11].

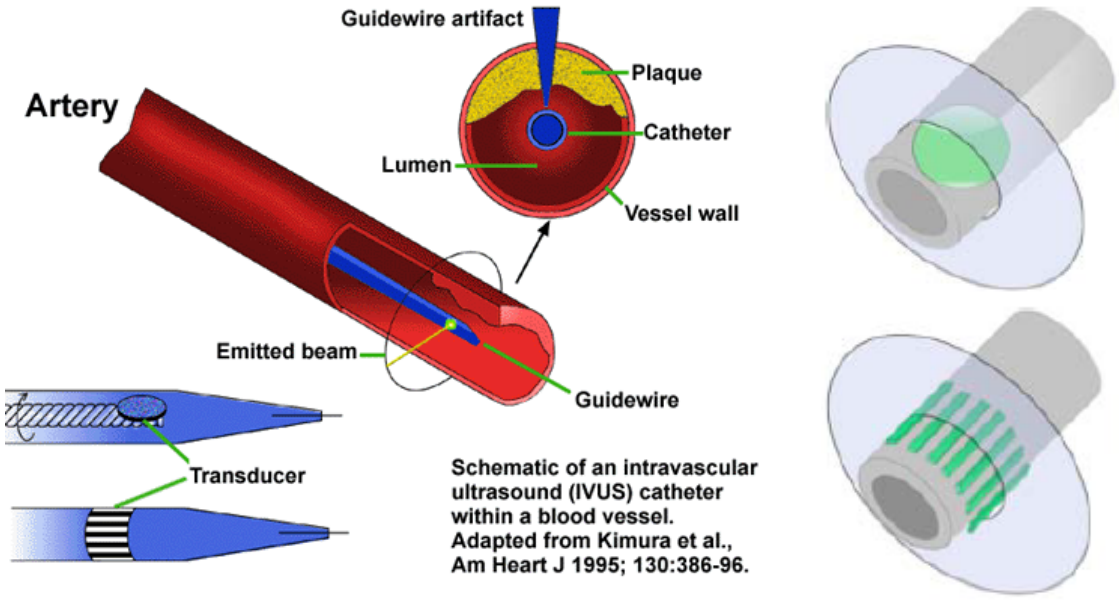


Figure 2. Examples of single-element and multi-element transducer configurations with imaging planes shown on the right [9].

Catheters are available in a variety of sizes from 3 French to 15 French which corresponds to diameters of one to five mm respectively with a central guide wire on many of the designs. The smaller sized catheters, on the order of 1-2 mm in diameter, are used for IVUS while larger catheters on the order of 3-5 mm are useful for intracardiac echocardiography, ICE. As such, piezoelectric transducer fabrication is better suited for larger transducers or transducer arrays, and it is not ideal for small scale transducer elements required for IVUS applications. The standard frequency range of operation varies from 5 MHz up to 45 MHz depending upon the application and imaging resolution desired. Additional research includes higher frequency transducers beyond 45 MHz for harmonic imaging modalities and/or increased resolution [12-14].

Standard IVUS catheters can be divided into two main categories depending upon whether they utilize a single-element or multi-element array as shown in Figure 2. The single-element catheter is relatively simple in design requiring minimal electronics integration, but it requires 360 degree mechanical rotation to form an image. Conversely,

the multi-element catheters, which can have up to 64 elements wrapped around the catheter, require complex electronics but don't necessarily require constant rotation. By retracting the catheter at a known rate, the tissue can be imaged in a 3D manner through the acquisition of multiple cross-sectional images. Sample cross-sectional images are shown in Figure 3 and show a normal vessel, left, and a vessel with plaque and calcification, right [15]. Although current commercial IVUS catheters are predominantly side-looking with the inability to image directly in front of the catheter, Volcano has introduced a "forward-looking" catheter with RF ablation capabilities. This catheter requires rotation and only produces an image over a conical surface but not a full 3D volumetric image in front of the catheter and it doesn't appear to be for sale as of August 2012 [16].

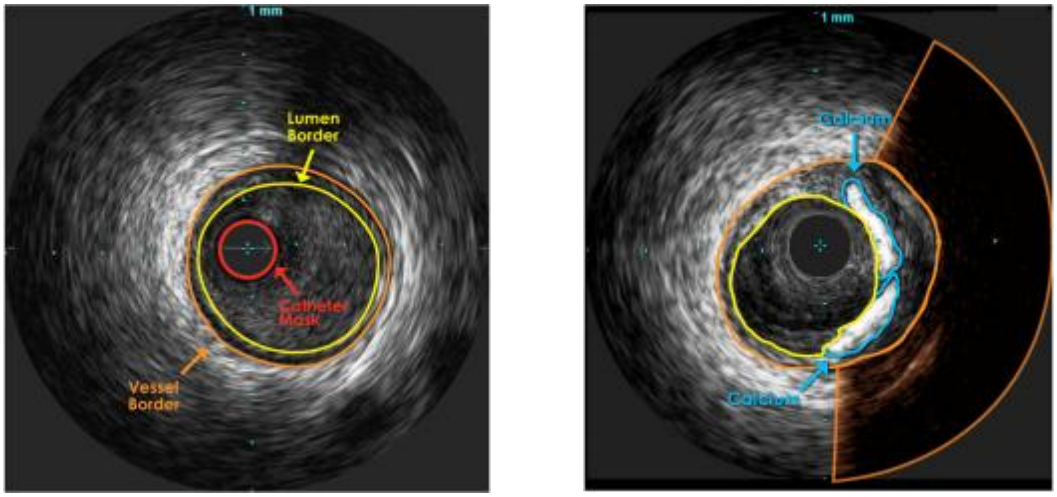


Figure 3. IVUS cross-sectional images of a normal vessel (left) and with calcification (right) [15].

1.3. Angioplasty and Stent Placement

IVUS procedures of particular interest for the treatment of heart disease requiring accurate non-destructive evaluation (NDE) of the vascular system include, but are not limited to, angioplasty and stent placement. Angioplasty is a procedure to unblock or

expand occluded arteries where an inflatable balloon on the end of a catheter is used to compress the plaque buildup through repeated inflation and deflation, Figure 4-left [17]. Following the angioplasty, and depending upon the situation, a stent can be permanently placed and expanded to support the arterial wall helping it to remain open for a longer period of time, Figure 4-right. This stent, which is commonly a wire mesh, can also be coated with medicines to prevent the artery from becoming clogged. Currently, accurate stent placement is difficult, with the stent often being completely misplaced altogether. There is also a desire for high-resolution imaging capable of evaluating how the stent is interacting with the surround tissue just after placement, and for reevaluation after an extended period of time.

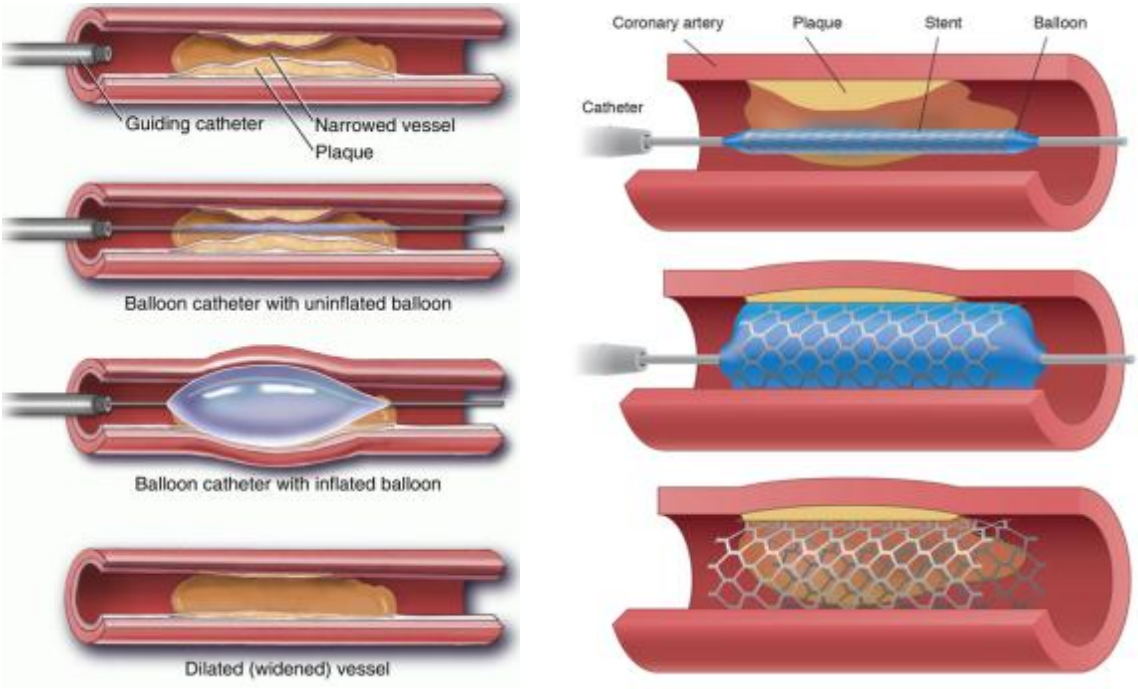


Figure 4. A pictorial diagram of the angioplasty procedure (left) and the stent placement procedure (right) [17].

Because of the limited imaging capabilities of current IVUS catheters, namely the imaging plane perpendicular to the catheter axis, physicians and other clinical personnel often have difficulty guiding the catheter through the many vascular branches before it is retracted for 3D imaging. These procedures would directly benefit from the inclusion of

forward-looking capabilities on the catheter to evaluate the effectiveness of the vessel dilation and proper stent placement and expansion.

1.4. Chronic Total Occlusions

Complications also arise with chronic total occlusions (CTOs), defined as when the artery has been completely blocked for more than 30 days. Blood flow from stenosed vessels can be decreased to such an extent as to be clinically significant. In Figure 5 the vessel is completely occluded, and the guide wire is used to push through the plaque. This situation occurs in approximately 30% of patients suffering from coronary disease [3, 18]. Occluding plaque can be divided into two categories based on the physical properties, hard and soft, Figure 6. The hard plaque is fibrocalcific, more than 50% collagen and calcium while the soft plaque is cholesterol, macrophages, and loose fibrous tissue. Treatment options include medication, ~22%, surgery, ~31%, and angioplasty ~47% [18]. Unfortunately, angioplasty for these patients is more resource intensive in terms of device utilization, catheter lab time, and fluoroscopy exposure which also leads to greater exposure to radiation. For these situations, advancing catheters are unable to image in front of them, and in more severe situations, the catheter can rupture the vessel wall while attempting to pass an occlusion as the guide wire progresses as depicted in Figure 5-right. For this scenario, the forward-looking IVUS catheter would be beneficial to evaluate the blockage and reduce procedure time along with associated catheter lab resources.

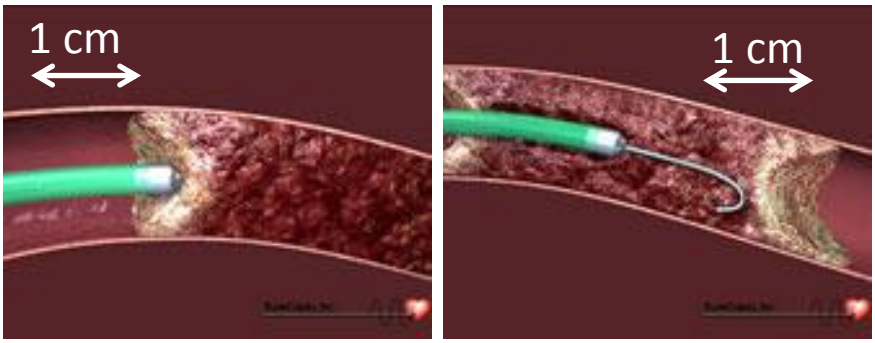


Figure 5. CTO imaging demonstrating the two imaging scenarios. The catheter approaches the CTO through the blood (left) and the catheter is pushing through the occlusion (right) [18].

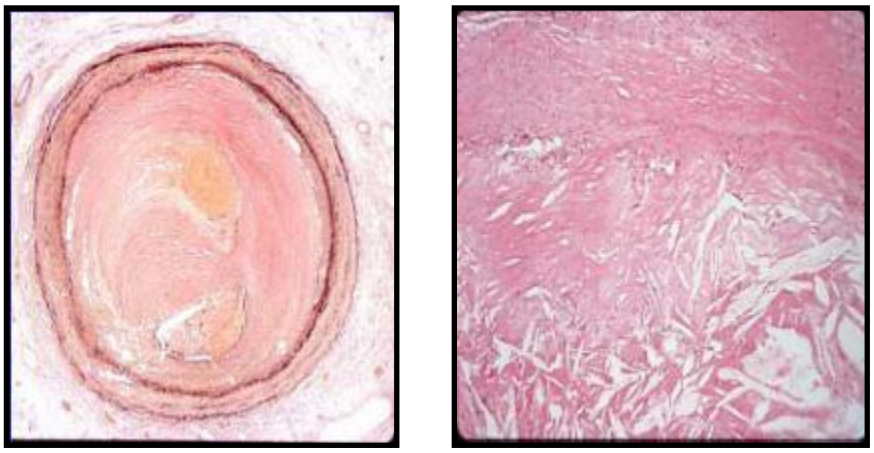


Figure 6. Hard plaque (left) and soft plaque (right) [18].

1.5. Heart Valve Replacement

Heart surgery is routinely performed to repair or replace diseased heart valves through open heart surgery or less invasive procedures with a catheter inserted through a smaller incision. Recent developments have focused on the use of intracardiac echocardiography (ICE) catheters to replace heart valves without the need for invasive open heart surgery. The transcatheter aortic valve implantation (TAVI) depicted in

Figure 7 uses a catheter inserted in the groin area to deploy a prosthetic heart valve [19, 20]. The valve shown is comprised of three bovine pericardial tissue leaflets integrated with stainless steel expandable stent which remains compressed until it reaches the aortic valve. A balloon on the catheter is used to expand the valve within the current diseased valve to act as a direct replacement. Candidates for these percutaneous procedures include patients deemed to be inoperable as defined as a patient who faces more than a 50% risk of death following the standard surgical procedure. Patients in this category include those of advanced age or previous heart surgery. The TAVI and other procedures requiring soft tissue imaging of the heart benefit from forward-looking improved imaging capabilities for accurate valve deployment/evaluation or other repair procedure.

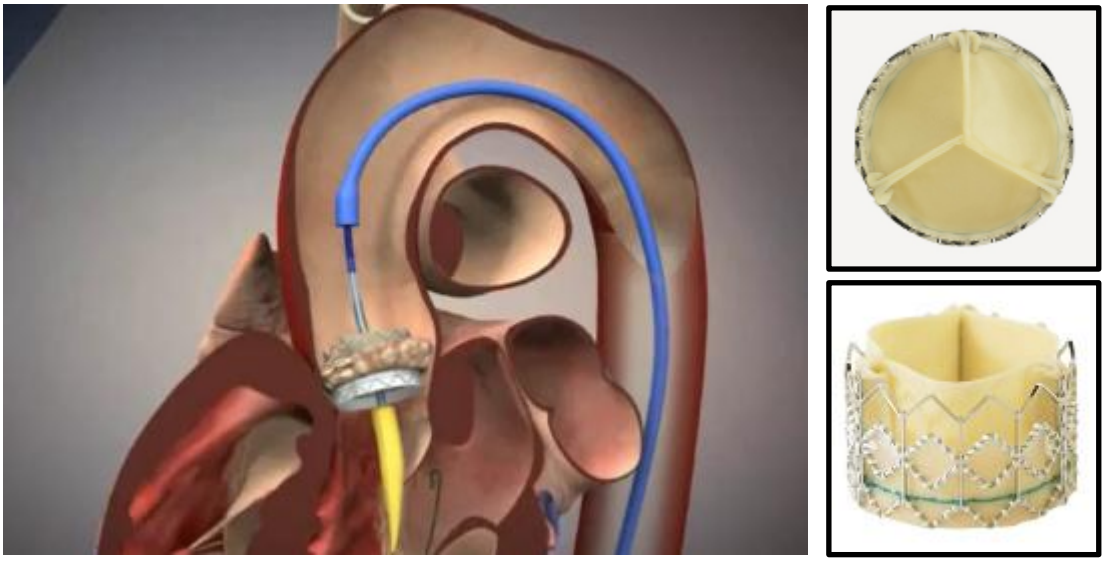


Figure 7. A TAVI procedure is shown placing a prosthetic aortic valve through the use of a catheter inserted through the groin area (left) and a prosthetic heart valve based on an expandable stent mesh (right) [19, 20].

1.6. Catheter Constraints

Intravascular catheters, by their very nature, have certain limitations as they are inserted into the human body. They are inserted and guided through the vascular system around corners and through various branches. The whole assembly including tip with transducers and associated electronics must be flexible enough to reach the affected area. The number of cables for powering electronics and signal transmission are limited, on the order of 25 cables/mm^2, which translates to ~ 20 cables for a 3 French/1mm diameter catheter based on Tyco Electronics 48 AWG coax cable documentation [21]. Additionally, within the body, there are voltage limitations to prevent accidental shocking of the patient, which can lead to fibrillation and other complications.

With these constraints in mind, the transducer arrays for forward-looking IVUS and ICE capabilities need to be small in diameter to fit on the tip of the catheter while incorporating a center hole for a guide wire as shown in Figure 8. The element sizes for the ring array also need to be small in the radial and lateral dimensions to reduce side lobes which adversely affect imaging performance. To generate the volumetric image with sufficient SNR, the array area would also completely cover the doughnut shape tip real-estate. Therefore with a larger number of small transducer elements there is an inherent desire for direct electronics integration at the tip for signal amplification and to multiplex the output as constrained by the limited cable count.

The capacitive micromachined ultrasonic transducer (CMUT) has been introduced to address the limitations of piezoelectric transducer technology, namely the difficulty in fabrication of small, thin elements and the ability to integrate with electronics [22]. The following chapter will introduce the CMUT technology that will be investigated for use in developing ring arrays for real-time volumetric imaging capable of integration on the tips of IVUS catheters similar to the depiction of Figure 8.

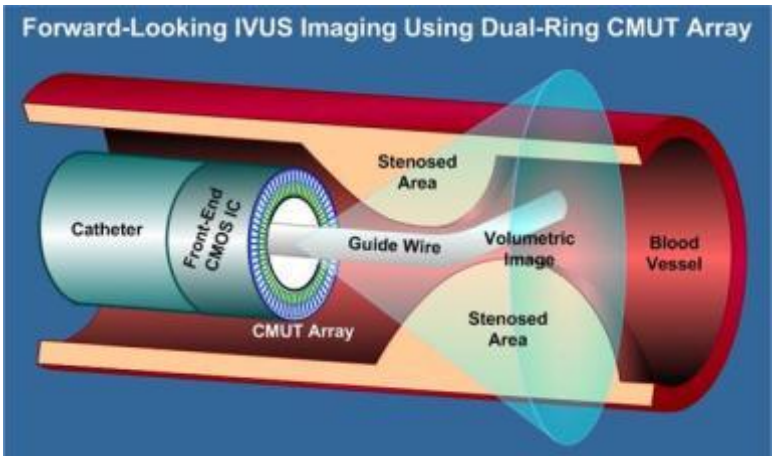


Figure 8. A depiction of a forward-looking ultrasonic catheter with guide wire.

CHAPTER 2

CMUTs: BASIC MODEL, DESIGN CRITERIA AND FABRICATION BACKGROUND WITH INTEGRATED ELECTRONICS

Although theorized in the late 1800's it wasn't until the 1990's that it was possible to micromachine CMUTs capable of competing with piezoelectric transducers in terms of performance [22]. These CMUTs offer an attractive alternative to the piezoelectric transducers, (mostly lead zirconium titanate PZT based), technology, especially while attempting to fabricate and integrate both forward-looking (FL) and side-looking (SL) arrays into a single IVUS catheter. This chapter will introduce the basics of CMUTs as well as the specific design requirements for FL and SL arrays with improved performance as compared to the currently available commercial IVUS catheters.

2.1. Introduction to CMUTs

2.1.1. CMUT Operation

In its most basic form, a CMUT is comprised of two electrodes with a vacuum gap between. One electrode is fixed, the bottom electrode, and the other electrode is buried inside or affixed to a top, movable membrane. Figure 9 shows a cross-sectional diagram of such a CMUT with silicon nitride as the membrane material and buried top electrode above a vacuum gap. Appendix A describes the standard CMUT fabrication used for this research. A DC bias is applied to provide charge to the top electrode which in turn deflects the membrane closer to the bottom electrode setting up an electric field in the GV/m range. Additionally, this increases the linearity of the response. This is similar to the standard capacitive electret type microphones which utilizes a permanently trapped

charge in a material such as Teflon^{TM} as opposed to an external DC bias [23]. In the transmit mode of operation, an AC signal is also applied to induce membrane motion which couples to the surrounding fluid generating the ultrasound for imaging. In the receive mode of operation, incoming ultrasonic waves impinge upon the membrane causing it to deflect which in turn changes the capacitance of the transducer generating a detectible current.

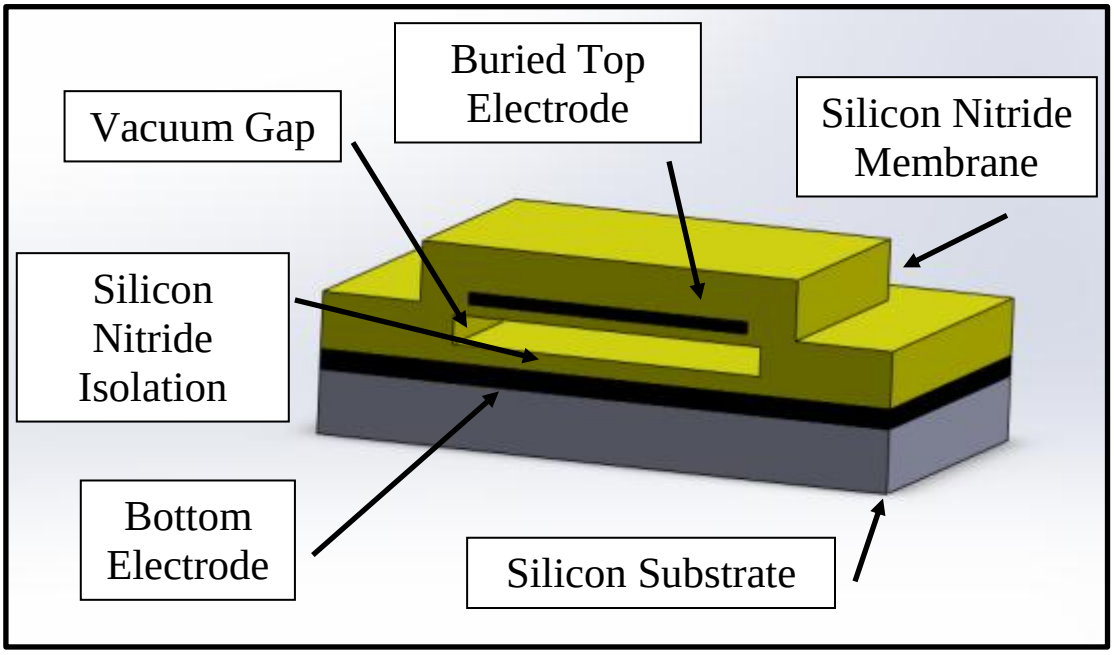


Figure 9. Cross-sectional image of a CMUT, primarily made from silicon nitride.

2.1.2. Static Parallel Plate CMUT Analysis

A CMUT has a compliant membrane typically with an electrode gap separation much smaller than the lateral dimensions, aspect ratios >> 100. Neglecting the deflected membrane shape, a simple parallel plate actuator can be used to develop analytical models to better understand the operation of a CMUT. Figure 10 shows a first order model with a spring-mass-dashpot mechanical system with an applied potential between the top and bottom electrodes. For a static analysis, the mass associated with membrane

and the force from the dashpot can be ignored, and the force balance between the membrane stiffness, k, and the electrostatic force can be evaluated.

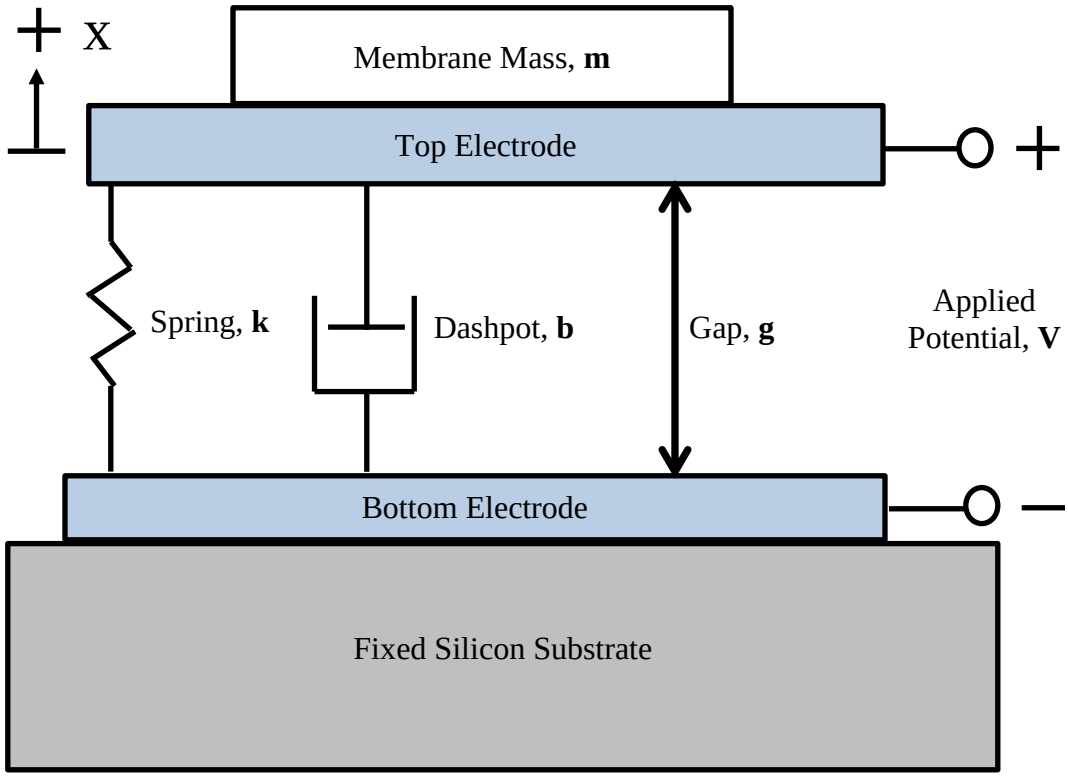


Figure 10. An illustration of a parallel plate CMUT model of the first-order.

The mechanical force from the spring can be described by equation (1) where k is the spring constant associated with the membrane stiffness, g_0 is the initial gap, and g is the instantaneous gap. The electrostatic force is given by equation (2) where A is the electrode surface area, ε_0 is the permittivity of the space between the electrodes, and V_0 is the applied potential. When the mechanical force and electrostatic force are in equilibrium, the net force on the membrane is zero. By mathematically setting the electrostatic force equal to the mechanical force it can be shown that after a certain potential, $V_0=V_{collapse}$, the electrostatic force will always be greater than the mechanical force, equation (3) leading to a condition where the membrane will completely deflect

leading to a collapsed condition. By plugging equation (3) into the force balance, the membrane displacement at collapse, $x_{collapse}$, can be simplified and is found to be 1/3 of the original gap, equation (4). Figure 11 shows the static mechanical and electrostatic forces as a function of the normalized membrane displacements at collapse and after collapse. It can be seen that as the collapse is approached, the static equilibrium occurs at 1/3 of the gap, whereas the electrostatic force is always greater than the mechanical force after collapse [24].

$$F_s = k(g_0 - g) \tag{1}$$

$$F_{es} = -\frac{\varepsilon_0 A V_0^2}{2g^2} \tag{2}$$

$$V_{collapse} = \sqrt{\frac{8kg_0^3}{27\varepsilon_0 A}} \tag{3}$$

$$x_{collapse} = \frac{g_0}{3} \tag{4}$$

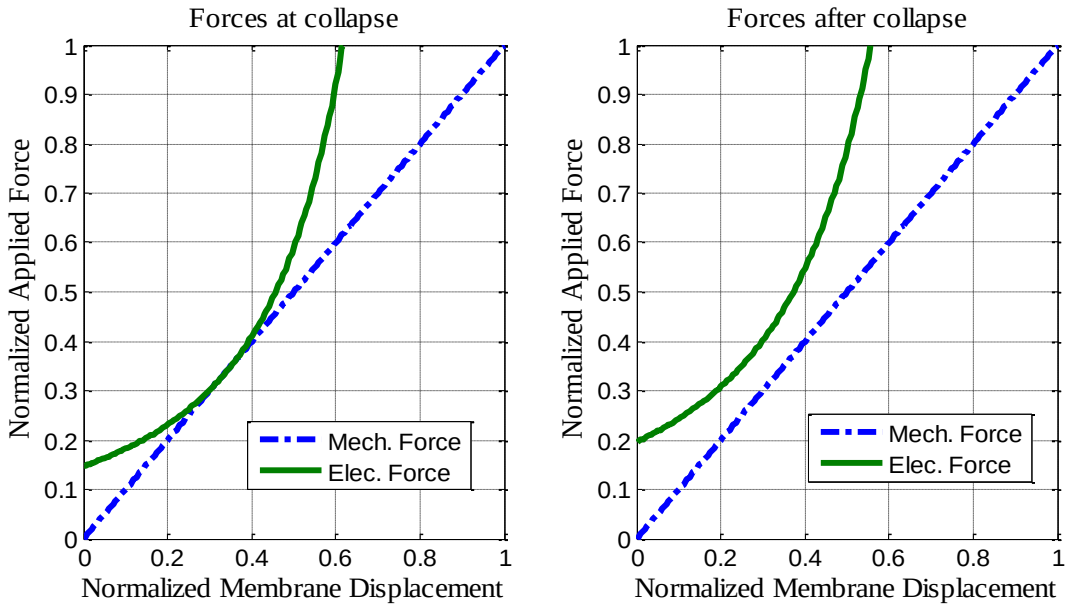


Figure 11. Mechanical and electrostatic forces at collapse (left) and after collapse (right) for a parallel plate actuator with k = 1 kN/m and g_0 = 0.1 µm [24].

2.1.3. Small Signal AC Mason Equivalent Circuit Model

The CMUT is a reciprocal transducer converting electrical energy into mechanical in the transmit (Tx) mode of operation and mechanical to electrical in the receive (Rx) mode of operation. The Mason Equivalent circuit can be used to investigate CMUT operation in fluid assuming linear, small-signal analysis with parallel plate operation [25]. The deformed membrane profile is again neglected for the parallel plate, and it is assumed that the dynamic voltage and displacements are much smaller than their associated static components. Figure 12 shows the circuit with an electrical mesh consisting of an AC signal with parasitic capacitor, C_p, and membrane capacitance with DC bias, C_0. The mechanical mesh includes complex impedances for the membrane and fluid, Z_m and Z_f, respectively. The two meshes are connected via a transformer with ratio 1:n, where the current in the electrical domain is equivalent to the velocity in the mechanical domain. Through algebraic manipulation and circuit analysis, it can be

shown that the transformer ratio, *n*, is inversely proportional to the square of the effective gap of the CMUT, equation (5). In this equation ε_r is the relative permittivity of the isolation material between the electrodes, 6.7 for silicon nitride, and t_{nit} is the thickness of the isolation [26]. As the DC bias is increased, the gap is reduced up to the point of collapse, 1/3 of the equivalent gap, to yield the greatest transformer ratio. It can be shown that at collapse, the transformer ratio is only dependent up on the initial gap, equation (6). Therefore one would like to fabricate CMUTs with the smallest possible gap for highest Rx mode sensitivity. A more complete derivation and evaluation of the Mason equivalent circuit can be found in [24, 27].

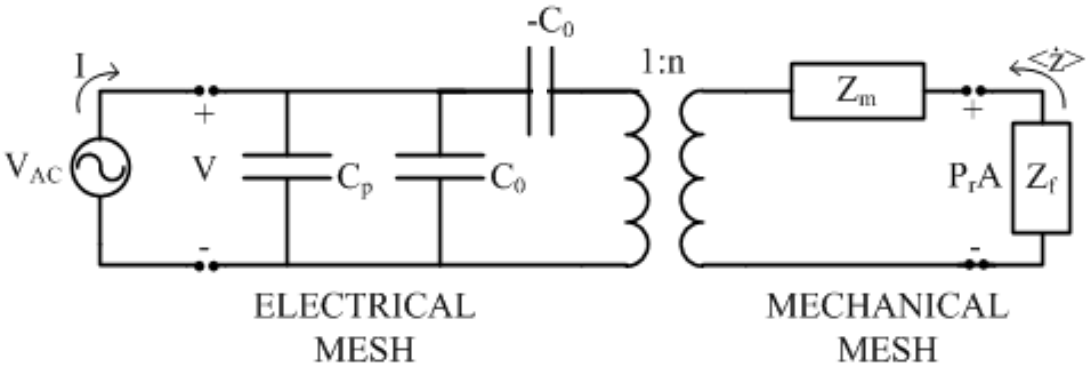


Figure 12. Mason equivalent circuit.

$$n = \frac{F_{es,AC}}{V_{AC}} = -\frac{\varepsilon_0 A}{\left(g + \frac{t_{nit}}{\varepsilon_r}\right)} \frac{V_{DC}}{\left(g + \frac{t_{nit}}{\varepsilon_r}\right)} = C_0 E \tag{5}$$

$$n_{collapse} = \sqrt{\frac{3kA\varepsilon_0}{2g_0}} \tag{6}$$

2.1.4. CMUTs in Comparison to Piezoelectric Transducers

Two distinct advantages are easily identifiable when comparing CMUTs to their piezoelectric counterparts within the context of catheter integration. For IVUS imaging arrays, dicing of the brittle piezoelectric materials as the element sizes drop below 200 μm is expensive and difficult, a significant drawback. Alternatively, CMUT technology is based on micromachining principles which allow for batch fabrication of transducer arrays of arbitrary shapes and sizes well below 20 μm. The bulk fabrication and ability to define curved, micron scale, features are a significant advantage when working with circular arrays for catheters. The processes used in the fabrication are well defined and characterized having been originally developed for the semiconductor industry.

Secondly, the fabrication processes involved with CMUTs are compatible with CMOS technology. This key feature allows for the transducer-electronics necessary to achieve compact assemblies with reduced cable counts as well as improved SNR associated with the direct connection of CMUT elements to amplifier electronics with details to be further discussed in the following sections.

To determine the resonant frequency, the standard piezoelectric transducer element is thinned to an appropriate thickness, with additional matching layers as the impedance of the transducer material can be significantly greater than that of water. In the case of lead titanate, PbTiO3, the impedance is 36 MRayls, 24 times that of water, 1.5 MRayls [28]. These matching layers are difficult to realize and reduce the bandwidth which is detrimental to the axial resolution. In terms of performance, previously fabricated CMUTs show greater fractional bandwidth than comparable PZTs [27, 29-32]. The impedance of a CMUT is lower than that of water leading to an over-damped system. This in turn leads to the larger bandwidth and improved transmission into water [33].

To illustrate, the mechanical mesh in Figure 12 can be evaluated for a simplified CMUT. In this case the impedance of the membrane is modeled as a simple spring and

mass system to produce $Z_m(f)$ which is equivalent to a band pass filter from a series capacitor and inductor with a resonance is set to 20 MHz which is shown when $|Z_m| = 0$ in Figure 13. Assuming the CMUT membrane surface is larger in comparison to the wavelength, the impedance of the fluid is assumed to be real and $Z_f = \rho_0 c_0 = 1.5\ Mrayls$ for the case of water [34]. The -6 dB pressure bandwidth is calculated from the crossing of $Z_m(f)$ with Z_f which is approximately 14 MHz to 29 MHz as shown in Figure 13 for a 70% fractional bandwidth (FBW).

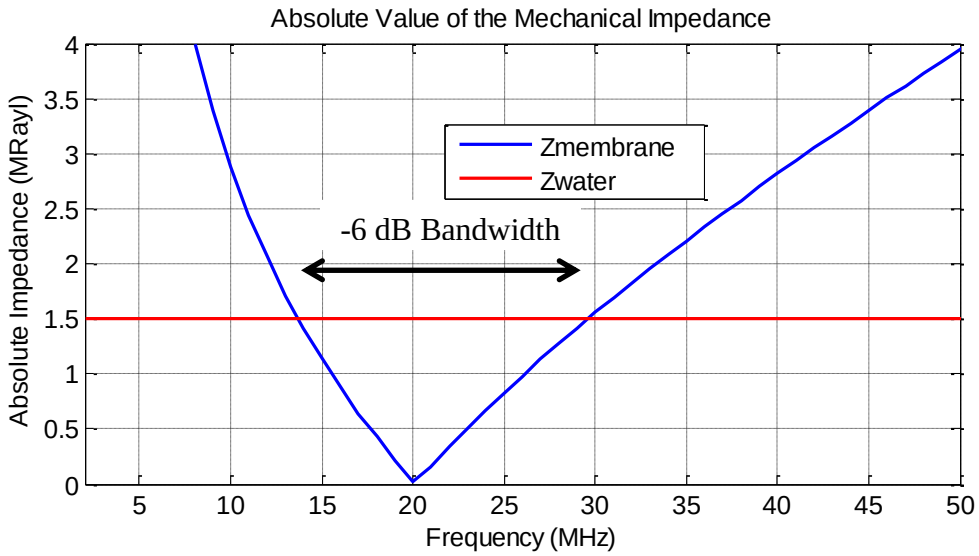


Figure 13. Mechanical mesh impedance analysis of a simple parallel plate CMUT with a spring constant, K, and mass, m, in comparison to water.

Unfortunately, CMUTs suffer in the performance area when evaluating the peak output pressure as compared to their piezoelectric counterparts. For the CMUT, the maximum membrane displacement is physically limited to the fabricated vacuum gap, and the peak pressure is proportional to the displacement. For a simplified piston type transducer with uniform harmonic surface displacement in fluid, the surface pressure can be described by $P_{surface} = \rho c \pi f u$ where ρ is the density and c is the speed of sound in fluid, u is the piston displacement, and f is the frequency of operation. From this basic

analysis, is can be observed that the surface pressure is proportional to the frequency of operation, and the transmit pressure for CMUTs designed for low frequency applications, ~ 10 MHz, require 4 x the displacement of a 40 MHz transducer for the same desired output pressure. Certain techniques to improve the pressure in the Tx mode have been shown to be effective through geometric and biasing optimization [27, 31, 35, 36].

However in general, from the basic analysis, the optimization of the CMUT for receive operation is based on reduction of the vacuum gap, but this reduction reduces the transmit pressure capability. As such, for the ring array design for forward looking applications, it has been proposed that that the single ring can be divided into two separate rings, one for transmit and one for receive as shown in Figure 14. This allows for separate optimization of the Tx/Rx CMUT elements and additionally allows for electrical separation when integrated with electronics.

Although the models used for comparison purposes are simple, ignoring many realistic factors, it provides initial insight. Therefore, a better model is needed to predict the behavior of both Tx and Rx elements.

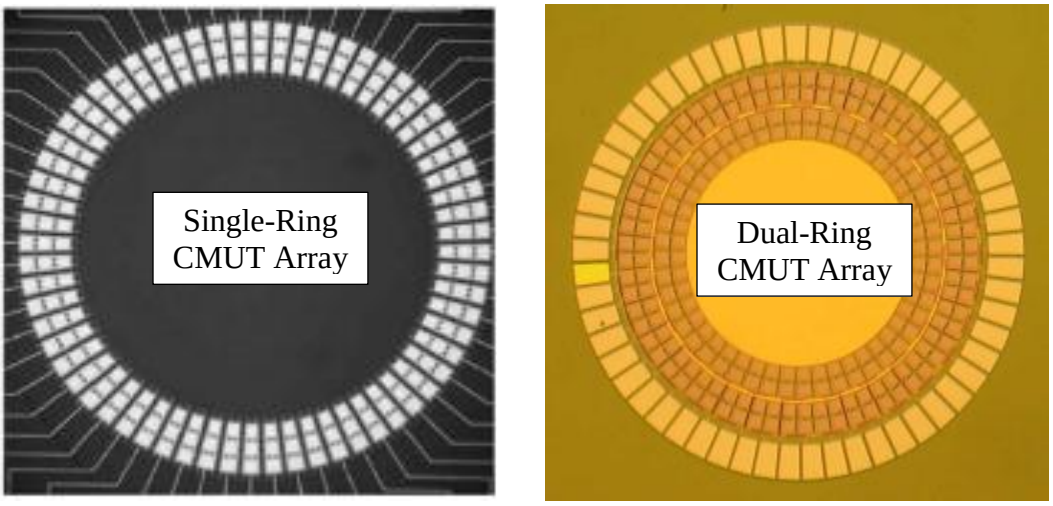


Figure 14. Fabricated CMUT arrays with a single-ring of elements, 1.2 mm outer diameter (left) [37] and dual-ring of elements, 0.8 mm outer diameter (right).

2.2. CMUT-Electronics Integration

One of the primary benefits of CMUT technology is the promise of simplified integration with CMOS electronics for improved performance and real estate optimization [38, 39]. By connecting the CMUTs directly to the CMOS electronics, the parasitic capacitance can be significantly reduced to improve the overall SNR, and with front end multiplexing electronics, the number of cables necessary to connect the front end of the catheter to the backside imaging system can be significantly reduced. Further, real estate optimization is extremely important when dealing with forward-looking arrays found on the tip of a catheter. Arrays for side-looking capabilities are not as constrained since they can utilize the lateral dimension, but still require electronics integration for SNR improvement. Multiple integration methods have been proposed and implement with varied strengths and weakness. The following sections describe previous work along with the method of integration developed as part of this dissertation.

2.2.1. CMUT-in-CMOS

Processing of the CMUTs can be simultaneously accomplished with the fabrication of electronics utilizing reliable and well-established CMOS processing techniques [40]. Due to the parallel processing, the overall fabrication time and processing costs are reduced. However, the design space for the CMUTs suffers from the limited CMOS fabrication options in terms of material types, material properties, and layer thicknesses. Total device area also increases as the electronics and CMUTs must be positioned side-by-side. Therefore, this is not an ideal scheme for FL-IVUS applications where available space is limited. Figure 15 shows a single CMUT membrane fabricated during the CMOS processing with associated electronics above and to the right [40].

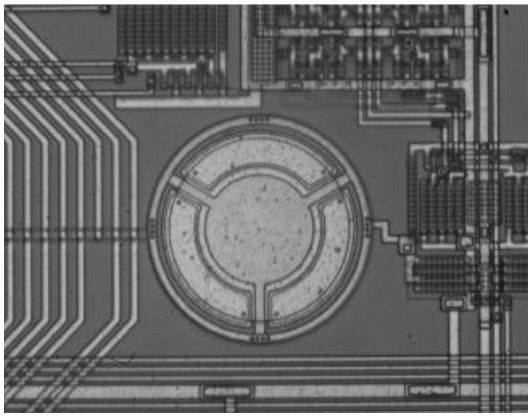


Figure 15. A single CMUT element, center, with surrounding CMOS electronics [40].

2.2.2. Interleaved CMUT-CMOS

To improve upon the CMUT design space, it is possible to interrupt the electronics fabrication for outside processing [41, 42]. This method has been utilized to generate smaller gap heights as compared to the aforementioned CMUT-in-CMOS processing. This technique increases cost and fabrication complexity and may experience resistance from commercial CMOS foundries due to contamination concerns. In addition, even though CMUT performance can be improved, this process is still similar to the standard CMUT-in-CMOS technique outlined above, in which available area is not optimally utilized.

2.2.3. Flip Chip Bonding

To improve on the utilization of available device area, and to allow for better optimization of CMUT material properties, separately fabricated CMOS and CMUT chips can be electrically connected through flip chip bonding [43-48]. In this case, the CMUTs are not limited to low temperature, CMOS-compatible fabrication processes, nor are they limited to the materials and layer thicknesses designated by standardized foundry processes. However, this interconnect method requires a number of additional fabrication steps that include deep reactive ion etching, conformal metal and dielectric

depositions, backside patterning, and the final wafer bonding step [49]. Furthermore, the packaging techniques associated with this technology are complex in nature adding to the overall cost. This technique is attractive for larger CMUT arrays [50], but may not be ideal for FL-IVUS applications as the minimum solder bump pitch approaches the CMUT element pitch. Figure 16 shows a schematic of a 2D CMUT array which is flip chip bonded to a front-end IC for 3D volumetric imaging [49].

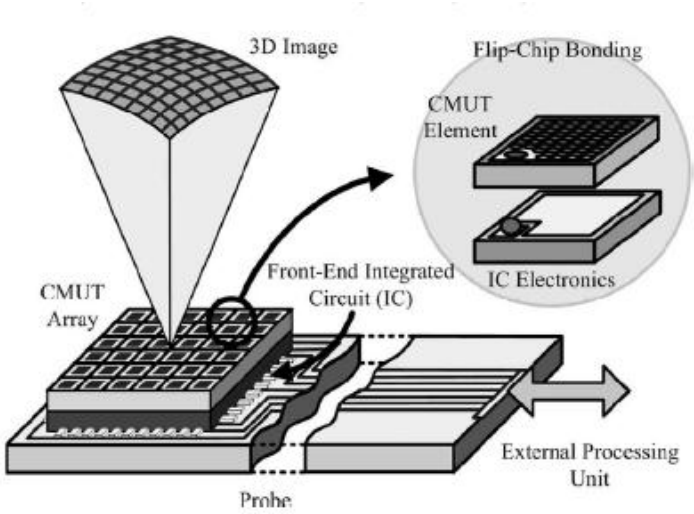


Figure 16. Schematic of a 2D CMUT array bonded to electronics through flip chip bonding methods [49].

2.2.4. CMUT-on-CMOS

To address the real-estate optimization and vacuum gap fabrication flexibility for forward-looking array optimization, a CMUT-on-CMOS process, has been pursued as an integration scheme where the CMUTs are directly fabricated above associated electronics as depicted in

Figure 17. This interconnect approach minimizes parasitic capacitances associated with connection lines while introducing only one additional masking step as will be described in CHAPTER 3. Total occupied area is minimized as the CMUTs can be located over CMOS metal layers, similar to the flip-chip bonding method, but without the complexity and spacing requirements associated with solder bump technology. In addition, the

CMUTs are not constrained by the CMOS processing steps, so it is possible to optimize material properties and produce thinner vacuum gaps for low voltage operation and increased electromechanical coupling efficiency. A drawback to this method is that fabrication is limited to processes under 400 °C so as not to damage the CMOS. However, it has been shown that the performance of CMUTs fabricated with such low temperature PECVD silicon nitride and oxide are not significantly affected.

The main design trade-offs associated with the different CMOS integration approaches is summarized in Table 1. Again, for the design constraints associated with FL-IVUS, this CMUT-on-CMOS fabrication was developed as a good compromise with advantages in optimal space utilization, minimal parasitic capacitances, and relative ease of fabrication and final assembly. Details of this fabrication will be discussed in CHAPTER 3.

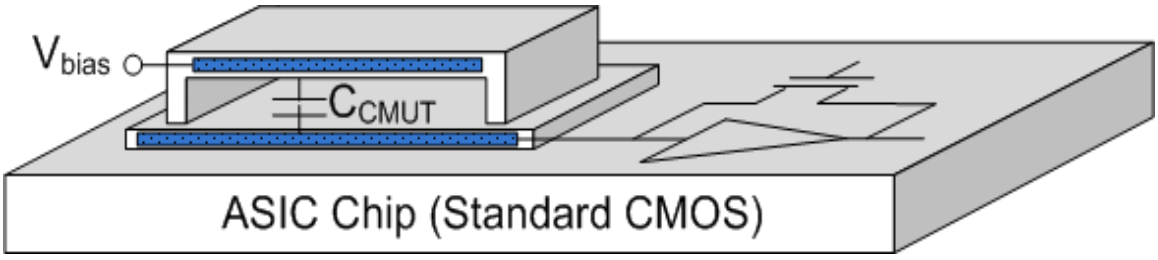


Figure 17. A simplified depiction of a CMUT on a CMOS substrate connected to an amplifier.

Table 1. CMUT-CMOS Integration Comparison

	CMUT-in-CMOS	Interleaved	Flip Chip	CMUT-on-CMOS
Number of Processing Steps	+	+	-	-
Active CMUT Area Optimization	-	-	+	+
Processing Temperature	n/a	-	+	-
Gap Height Control	-	+	+	+
CMUT to CMOS Interconnect Assembly	+	+	-	+
Foundry Compatibility	+	-	n/a	n/a

2.3. Array Design Requirements

The objective of this research is to improve upon the imaging capabilities of IVUS catheters through the use of novel CMUT arrays integrated with CMOS electronics. These CMUT-on-CMOS arrays can be divided into two distinct categories based on the imaging direction, forward-looking and side looking. The requirements for each are unique in terms of operational frequency, array design, electronics, and SNR. A preliminary breakdown of the design objectives will be discussed in this section.

2.3.1. FL-IVUS Dual-Ring Array

Forward-looking arrays for generating 3-D forward-looking volumetric images can also be utilized for Doppler blood flow imaging through the investigation of the frequency shift in the received signal as a further assessment tool. In the context of IVUS catheters, the available transducer space is limited to a doughnut shaped region as the guide wire passes through the center, as previously introduced. With such a limited

surface area to work with, fabrication with piezoelectric based transducers becomes increasingly difficult and hence is an ideal candidate for the CMUT-on-CMOS technology.

An experimental forward-looking PZT array for 3-D imaging can be seen in Figure 18 where a rectangular PZT slab was diced and wrapped around a catheter tube with a final outer diameter of 4.3 mm, 13 French [51]. Although too large for many IVUS applications, this is an excellent example of a single-ring array using PZT technology for volumetric imaging.

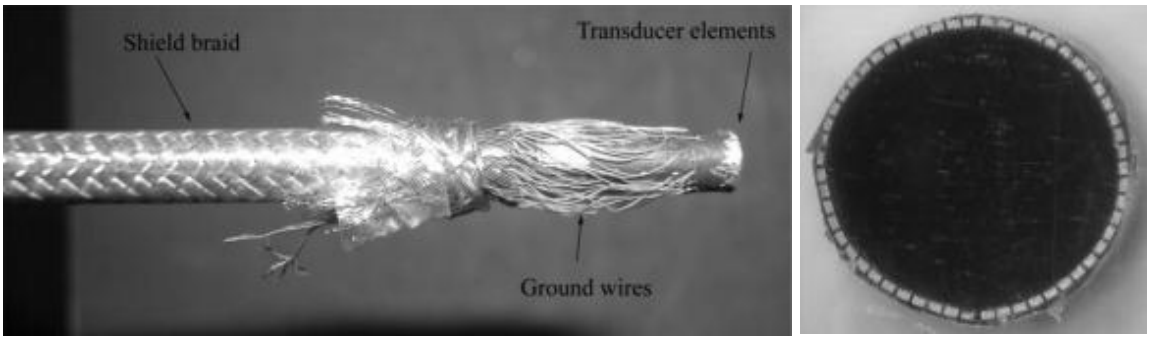


Figure 18. A single ring PZT based forward looking array [51].

Single-ring CMUT arrays have been previously fabricated as shown in Figure 19-left [37, 52, 53]. These designs work well with the doughnut shaped real estate available, but just as in the PZT array in Figure 18, each element is used for both Tx and Rx operations. For the CMUT, this means that the DC bias used is the same for both Tx and Rx operation and requires protection circuitry for the electronics integration. This additional circuitry increases the complexity of the electronics and the noise in the system. Figure 19-right shows a previously proposed integration scheme where the

CMUT array on the front of the catheter is connected to associated electronics on the sides via wire bonding.

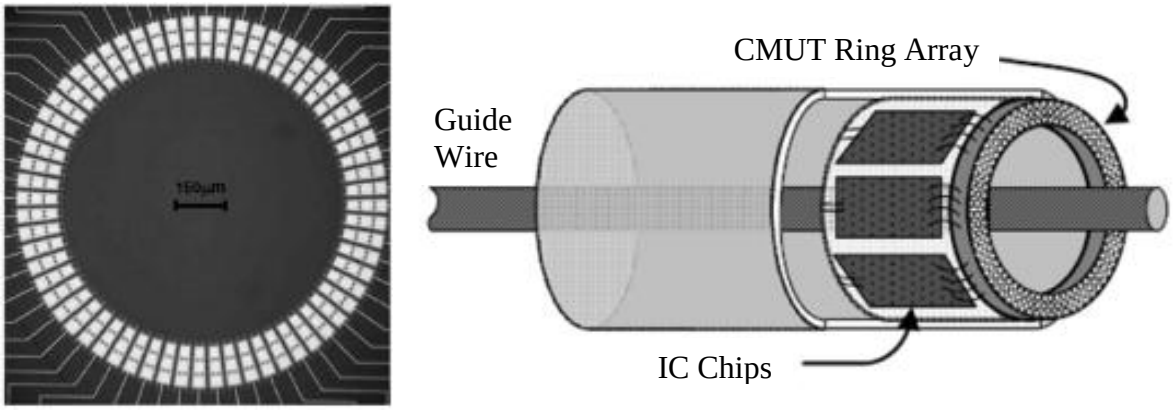


Figure 19. A fabricated single-ring CMUT array (left) and a diagram of a catheter with a single-ring array for forward-looking imaging with guide wire (right).

Dual-ring CMUT arrays have also been fabricated, Figure 20, to improve upon the single-ring CMUT design [29, 54]. With two rings of CMUTs, the Tx and Rx elements can be separated and optimized independently. For example, the vacuum gaps for the Rx elements can be minimized to increase the transformer ratio and increased for the Tx elements as necessary to allow for sufficient membrane displacement and corresponding Tx pressure. With this dual-ring design, there is a small loss in resolution from the reduced inside diameter, but with separate Tx-Rx elements, protection circuitry is no longer required which also reduces the associated noise from such circuitry. This in turn allows for easier CMOS integration as the Rx elements can be directly connected to amplifiers and Tx elements can be directly connected to pulser circuitry.

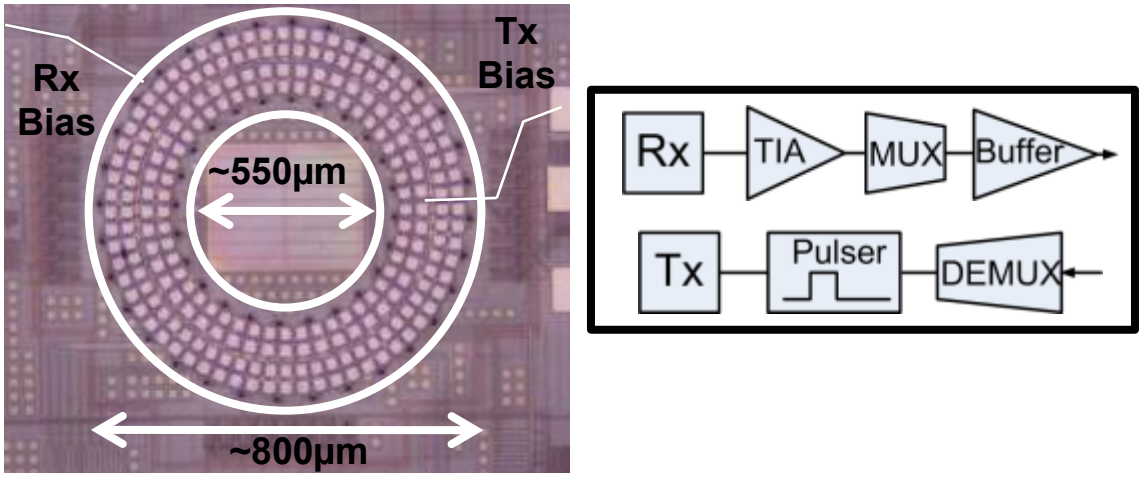


Figure 20. A fabricated dual-ring CMUT design with separate Tx and Rx bias capabilites (left) and flow chart for Tx-Rx integration with electronics (right).

2.3.2. SL-IVUS Annular Ring Arrays

Side-looking, SL, arrays are useful for interrogation and investigation of the arterial walls and are a proven technology with PZT based catheters with the ability to generate 3D vessel images through rotation and extraction at known rates. Recent interest in ultrasonic imaging is in higher frequency ranges, above 20 MHz for increased imaging resolution [10, 28, 55-57]. However, high frequency ultrasound 35-70 MHz, in general, can be problematic as the attenuation of blood and tissue increases with frequency, and as the wavelength approaches the size of blood cells, scattering becomes more of an issue in terms of attenuation [58-61]. Therefore, the ability to focus the side-looking array at these higher frequencies will be useful for improved SNR.

Transducers, circular in shape, have been previously fabricated with center frequencies greater than 20 MHz down to the mm diameter range [11, 62-64]. During the fabrication process, a PZT element can be given a curvature, and hence geometric focal point, by pressing a spherical object into the surface while the backing material is cured or dried, as depicted in Figure 21 [65]. With a single element transducer, there is an

inherent tradeoff between the depth of field, DOF, and resolution. For the case of the flat transducer, the lateral resolution achievable is determined by the size of the transducer, the operational frequency, defined by equation

(7**)** multiplied by the wavelength, Figure 22-left. The axial resolution is determined in the same way as for the ring above, equation

(8**)**. If the bandwidth is doubled, the axial resolution is increased two fold, Figure 22-right. The graphs in Figure 23 plot the lateral resolution vs. center frequency for F# 2.9 and F# 0.7 and the axial resolution versus bandwidth up to 150 MHz [66].

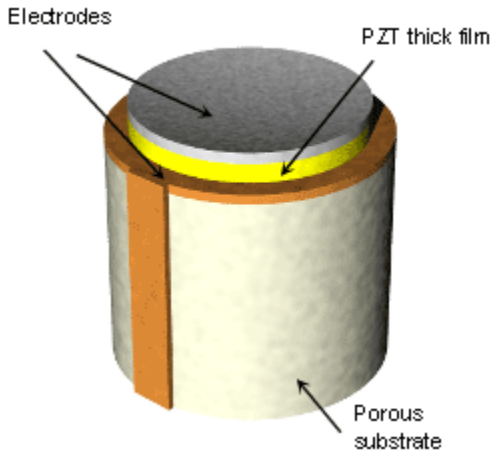


Figure 21. A depiction of a single element annular array with a geometric focus [65].

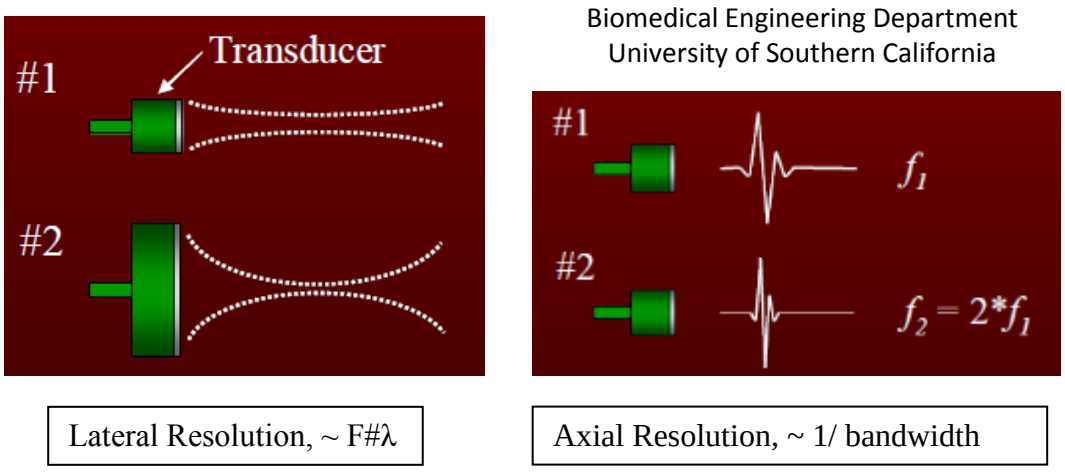


Figure 22. An illustration of lateral resolution (left) and axial resolution (right) [66].

$$Laterial\ Resolution \sim F\# \cdot \lambda = \frac{f}{D} \cdot \lambda \tag{7}$$

$$Axial\ Resolution \sim \frac{c}{2 \cdot BW} \tag{8}$$

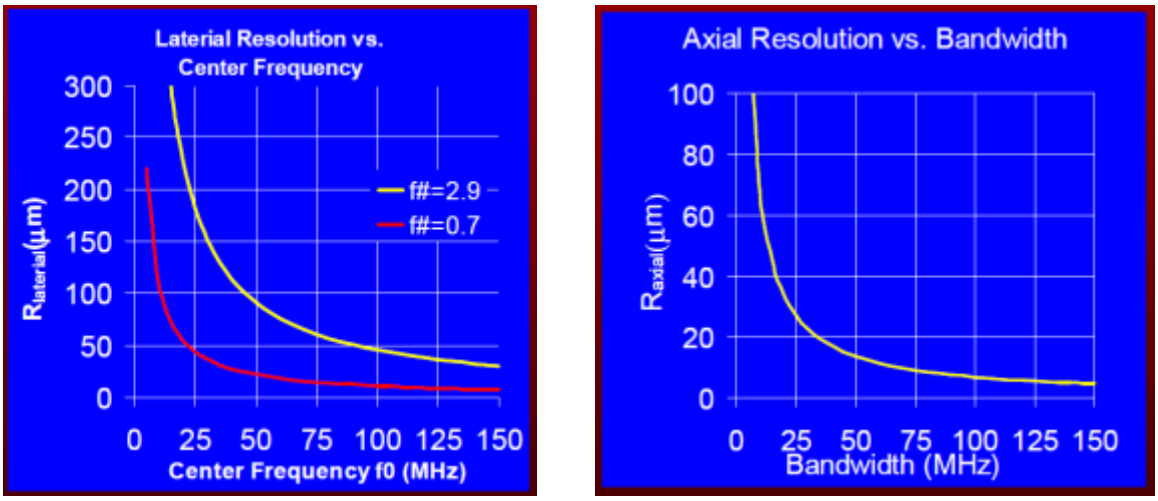


Figure 23. Graphs of: lateral resolution versus center frequency (left) and axial resolution versus bandwidth (right) [66].

Annular arrays have also been designed, Figure 24, to address the DOF-resolution tradeoff found with single element transducers [57, 65, 67-72]. With electronic focusing, time delays can be introduced in the Tx mode of operation to synthesize a curved surface effecting a change in the focal point of the transducer [56, 64, 73-75]. With an element radius, a_n, geometric focus, R, speed of sound in the fluid, c, and focal distance, f, equation (9) can be used to calculate appropriate time delays. For a flat transducer with no geometric focus, it can be seen that time delays between elements are the same when the areas of the individual ring elements are of equal surface area, which yields the greatest on-axis pressure. In the same way, when the received signals are combined, they can be delayed for receive focusing. Ideally, both Tx and Rx dynamic delay capabilities would be integrated with the transducer to minimize the cables necessary in the catheter.

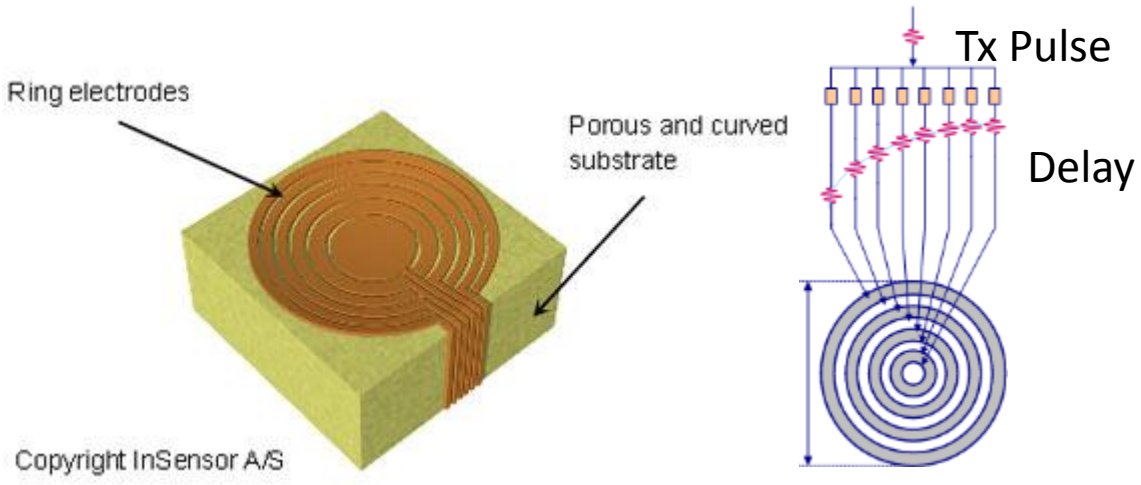


Figure 24. A depiction of an annular array (left) and illustration showing relative pulse delays for focusing (right) [65].

$$t_n = \frac{{a_n}^2(1/R - 1/f)}{2c} \tag{9}$$

Annular-ring arrays have been previously fabricated from piezoelectric materials, but to date, they are not suitable for IVUS applications due to the mm range diameters [63, 76]. Additionally, there are issues making electrical connections to all rings as the substrate is the common electrode requiring the top of each ring to be connected separately. Figure 25 shows an eight element piezoelectric annular array with wire bonded electrical connections to the surface of each ring [77].

CMUT technology offers an excellent alternative for the fabrication of annular arrays primarily associated with the ability to fabricate arbitrary array configurations. In addition, the interconnect between elements and associated electronics can be accomplished without the need for wire bonding. The development of these arrays will benefit from the same fabrication and electronics interconnect technology developed in this dissertation for the forward-looking dual-ring arrays.

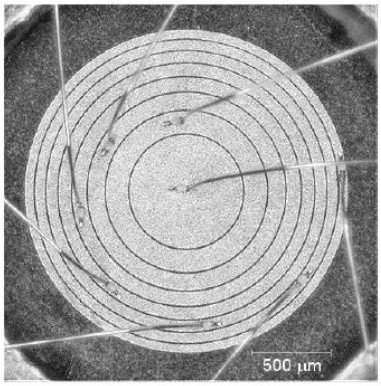


Figure 25. An eight element PZT annular array with surface wire bonding [77].

2.4. Summary

In this chapter CMUTs were introduced as a technology platform to address limitations associated with the prevalent piezoelectric transducer technology, micron scale fabrication and CMOS integration. The parallel plate model was evaluated to describe the basic operation of a CMUT under static conditions. It was shown that the collapse condition occurs when the electrostatic force no longer balances the mechanical spring force associated with the clamped membrane, when the membrane deflects to 1/3 of the original gap. The small signal Mason's equivalent circuit was also introduced to describe the electro-mechanical interaction of a CMUT in a fluidic environment. It was shown that the transformer ratio, *n*, can be used to describe how the mechanical response couples to the electrical mesh to generate a detectable signal and is proportional to the initial gap when biased close to the collapse voltage. Therefore desired fabrication includes reduction of the vacuum gap for increased Rx sensitivity. Additionally, based on the mechanical mesh of the Mason circuit, it was shown that the CMUT is inherently a broad-band device with improved transmission into water as the impedance of the CMUT is lower than that of water leading to an over-damped system.

Previous CMUT-CMOS integration efforts were described with various strengths and weaknesses. The CMUT-on-CMOS integration was identified as the optimal solution for the purposes of intravascular ultrasound to address minimization of parasitic capacitance and real estate constraints.

Finally, CMUT arrays for forward-looking and side-looking capabilities under investigation were introduced with the dual-ring and annular-ring configurations respectively.

CHAPTER 3

OPTIMIZED CMUT FABRICATION AND MONOLITHIC CMOS INTEGRATION

The bulk microfabrication techniques used for CMUT fabrication routinely suffer in terms of overall yield from such issues as contamination and misalignment similar to semiconductor electronics fabricated in a clean room facility. Traditionally, yield was considered a fabrication-only issue, however as design features and spacing rules become smaller, what is designed may not actually be fabricated. Therefore the layout becomes increasingly more important, and in industry this is beginning to be called "yield-driven-layout" [78]. Similarly, as the constraints become tighter for optimized CMUT fabrication, the layout becomes more important for optimizing the yield.

Additionally, one of the most important promises of capacitive micromachined ultrasonic transducer (CMUT) technology is integration with electronics. This approach is required to minimize the parasitic capacitances in the receive mode, especially in catheter based volumetric imaging arrays where the elements need to be small. Furthermore, optimization of the available silicon area and minimized number of connections occurs when the CMUTs are fabricated directly above the associated electronics.

The following section describes the process and fabrication methods used for efficient and reliable CMUT fabrication for Tx-Rx optimization as well as CMUT-on-CMOS fabrication along with modifications to allow for improved catheter integration.

3.1. Motivation for Fabrication for Optimized CMUT Tx-Rx Performance

Motivation for the fabrication optimization is driven not only by the improvement in yield but by the desire to decrease the minimum vacuum gap that can be fabricated for the improvement in performance. Therefore a preliminary evaluation of the benefits for a reduced vacuum gap and minimum isolation layers will be discussed.

The microfabrication techniques used for CMUT fabrication as described in Appendix A, utilize low temperature, 250° C, PECVD silicon nitride for the bulk membrane material and electrode isolation with metal layers for the bottom electrode, sacrificial layer, and top electrode as shown in Figure 26-left. Lateral dimensions for individual CMUT membranes and array spacing are set by the masks used for fabrication as shown in Figure 26-right for an example 10 MHz dual-ring array element. Table 2 lists typical layer thickness and dimensions for the 10 MHz CMUT membranes.

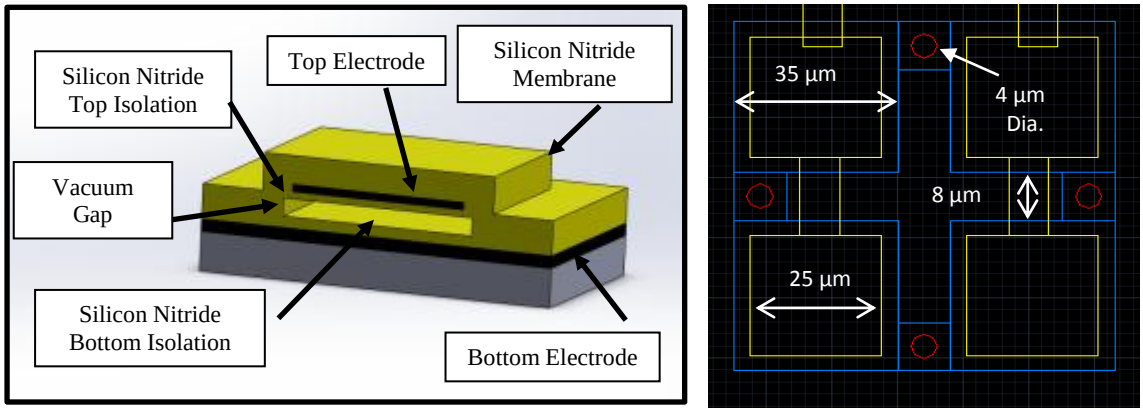


Figure 26. CMUT cross-section showing the silicon nitride top and bottom isolation as well as top and bottom electrodes (left). A sample 10 MHz dual-ring array element with four individual membranes electrically linked (right).

The layer thickness, predominantly, the isolation layers and vacuum gap directly affect the performance of the CMUT in Tx and Rx modes of operation. In the Tx mode, a larger vacuum gap allows for a greater membrane displacement. The linear relationship between displacement, u, and surface pressure, p, is described by equation (10) where f is the frequency, ρ and c are the density and speed of sound of the fluid respectively. Therefore a doubling of the surface displacement equates to a doubling of the surface pressure. In the Rx mode of operation, it was previously shown that the electromechanical coupling coefficient, $n_{collapse}$, of a CMUT is maximized when it is biased close to collapse as described previously by equation (6). In this equation, $n_{collapse}$, is proportional to $1/\sqrt{g_0}$, where g_0 is calculated from the silicon nitride isolation layer thickness, $t_{isolation}$ with its relative permittivity, 6.7, and the vacuum gap thickness with no bias applied, t_{gap}, equation (11). It is important to note that the resonant frequency of the CMUT membrane is tied to the thickness of the membrane. Therefore any adjustment of the bottom isolation or vacuum gap will have no effect on the operational frequency.

Table 2. Typical dimensions for a 10 MHz membrane.

Parameter	**Dimension**
Bottom isolation	0.15 μm
Top isolation	0.15 μm
Membrane	2.5 μm
Top Electrode	0.12 μm
Bottom Electrode	0.12 μm
Gap thickness	0.1 μm
Membrane width	35 μm
Electrode width	25 μm

$$p = u \cdot 2\pi \cdot f \cdot \rho \cdot c \tag{10}$$

$$g_0 = t_{gap} + \frac{t_{isolation}}{6.7} \tag{11}$$

Without the introduction of additional masking layers, which increases the fabrication complexity, the isolation and vacuum gap are identical for the Tx and Rx membranes. Therefore it is desirable to optimize the vacuum gap and isolation to allow for an optimal combination of Tx pressure and Rx sensitivity. Additionally, as the effective gap is reduced, the collapse bias is also reduced proportional to $\sqrt{g_0^3}$ as described in equation (3). This is beneficial for preventative electrical isolation purposes and integration with electronics. It is important to note that for practical purposes, a minimum amount of isolation is necessary to separate the bottom electrode layer from the top electrode layer due to the electrical connections between membranes that utilize the top electrode metal. Reported dielectric breakdown strength for PECVD silicon nitride varies from 915 V/μm at a deposition pressure of 400 mTorr to 410 V/μm at 700 mTorr [79]. The dielectric breakdown strength for PECVD silicon nitride used for the experimental devices fabricated was measured to be ~ 700 V/μm.

With the design parameters from Table 2, devices were fabricated with a measured collapse of 120 V. The transformer ratio for this case, Table 3 (a), was set to 1 for comparison purposes. In case (b) a reduction in the vacuum gap by 1/3 leads to an increase in the transformer ratio by 8% in case (c) with an additional removal of one isolation layer, the transformer ratio is increased by 18%. In case (d) the vacuum gap is further reduced to 0.05 μm, increasing the transformer ratio by 41% as compared to case (a). It is also important to note with this reduced gap and no bottom isolation, the

maximum field strength that the silicon nitride isolation is subject to is reduced by 30% as compared case (a) with full isolation and gap.

Based on this preliminary analysis and the calculations it can be seen that the desirable fabrication includes reducing the vacuum gap, and the overall isolation layer should be reduced to a minimum within the limitation of preventing dielectric breakdown through the isolation layer. For CMUT membranes at frequencies greater than 10 MHz, the vacuum gap may be further reduced for both Tx and Rx elements as indicated by modeling and simulation.

Table 3. Design Parameters for Optimization

	(a)	(b)	(c)	(d)
Parameter	**Fabricated Device**	**Reduced Gap**	**No Bottom Isolation**	**No Bottom Isolation & Further Reduced Gap**
Vacuum Gap	0.12 μm	0.08 μm	0.08 μm	0.05 μm
Total Isolation	0.30 μm	0.30 μm	0.15 μm	0.15 μm
Effective Gap	0.145 μm	0.125 μm	0.102 μm	0.072 μm
Collapse Voltage	120V	95V	72V	42V
Transformer Ratio	1	1.08	1.18	1.41
Nitride Field Strength	400 V/μm	320 V/μm	480 V/μm	280 V/μm

3.2. Robust CMUT Layout Design Considerations

For any microfabrication process, it is desirable that the process flow be as simple and robust as possible to preserve the overall yield and reduce the cost per unit fabricated. In general, the μm lateral dimensions of the CMUTs under investigation, do not pose a technological challenge. The use of contact lithography with photoresist exposed at 405 nm is capable of resolving feature sizes smaller than 3 μm, the minimum feature size associated with the sacrificial etch holes. However, optimization of the CMUT layout on the masking layers is tied directly to the processing and materials used for fabrication. In

particular, isolation is important if the metal layers used for the top and bottom electrode are susceptible to the etchant used during the sacrificial release.

For the case of CMUTs monolithically integrated with CMOS electronics, there are additional distinct fabrication limitations; predominantly the process temperature is limited to 400 °C so as to not adversely affect the CMOS substrate. This prohibits the use of thermal oxide/nitride growth techniques or low pressure PECVD which deposits above 700 °C [26]. Therefore, PECVD nitride at 250 °C is used for the isolation and bulk membrane material. Although, CMUTs have been previously fabricated with PECVD nitride, the quality suffers in terms of porosity. This can be an issue during the release process if the etchant used for the sacrificial layer seeps thought the nitride and etches the electrode material. Figure 27 shows a top electrode segment that has been etched during the sacrificial release process through the silicon nitride isolation. In addition to direct etching through the silicon nitride, misalignment during the etching of the sacrificial release holes can lead to an accidental opening to the bottom electrode as shown in Figure 28. For both cases, the top and bottom electrodes were aluminum, 0.11 μm with chromium, 0.01 μm, as a smoothing layer, and the sacrificial layer utilized was 0.12 μm of chromium.

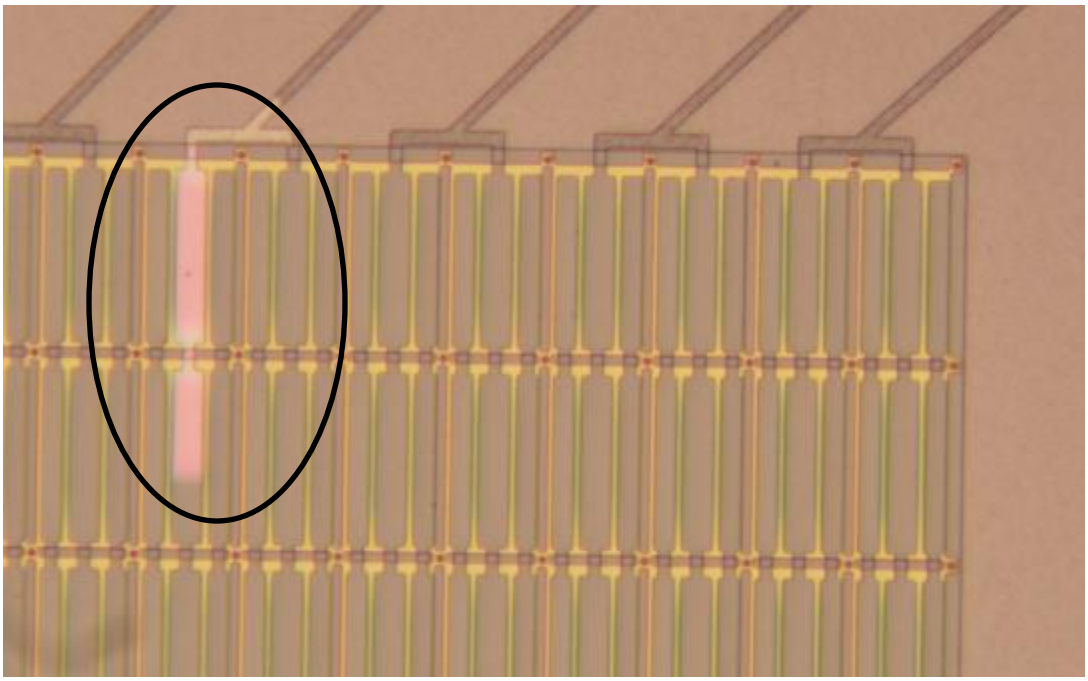


Figure 27. The top center electrode has been etched by the sacrificial etchant through the silicon nitride during the release process.

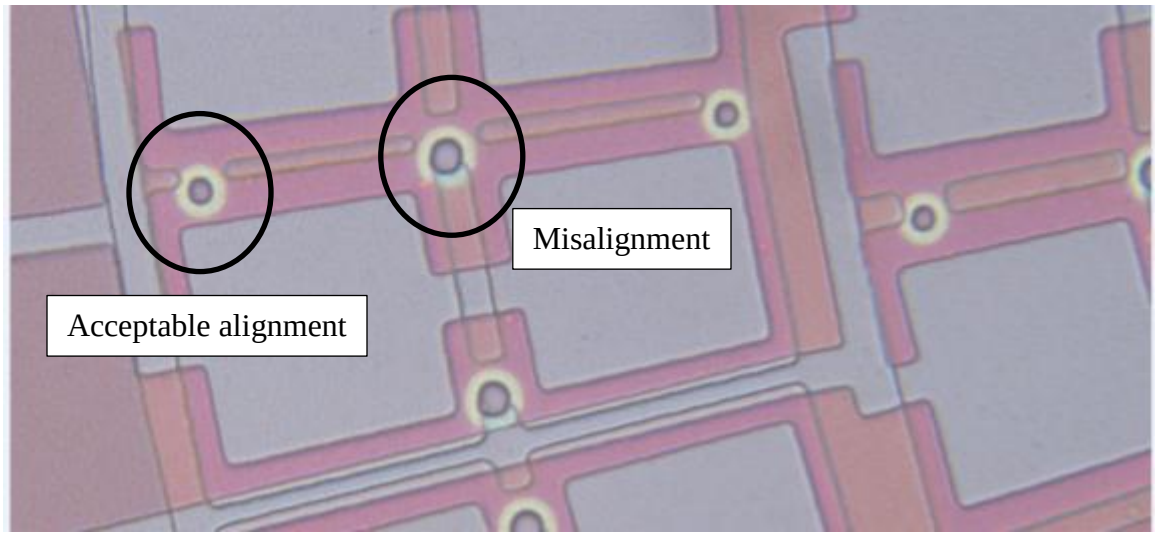


Figure 28. The start of the sacrificial release with acceptable alignment on the left and misalignment on the right.

Both modes of failure associated with improper sacrificial release can be minimized though judicious planning and layout of the sacrificial layer and associated release holes. To fully understand the layout considerations that can be implemented, it is important to think of CMUTs as being fabricated not only in the three physical dimensions but also in time. In particular, excessive time necessary for complete release of CMUTs leads to contamination of the isolation nitride and increases the probability of accidental etching of the electrodes through the isolation nitride.

Two easily implementable layout improvements are an increase in the sacrificial area surrounding the etch holes and the addition of extra sacrificial etch locations. As a design example, Figure 29 (a) depicts a sacrificial layer in blue with etch holes in red. The etchant removes the sacrificial layer in the direction as indicated by the arrows. For the case of a 50 μm x 100μm x 0.12 μm sacrificial layer, and etch holes on the corner, the release using CR-7s chromium etchant requires ~ 12 h. In Figure 29 (b), the sacrificial layer dimensions in the vicinity of the etch holes has been increased to allow for possible misalignment. It is important to note that the metal sacrificial layer acts as an etch stop for the reactive ion etch (RIE) of the nitride material, and with the larger sacrificial region surround etch holes, it is possible to over etch to ensure proper opening. Additionally, two more etch locations were included to decrease the time necessary for the etchant to release the membrane. The membrane thickening step that follows the release, fills the etch holes and mechanically pins the membrane at that location. Therefore, the addition of extra release holes and the slight increase in the size of the associated sacrificial region doesn't adversely affect the membrane dynamics. For a similar membrane sacrificial area, 50 μm x 100μm x 0.12 μm, the time for complete release is reduced to ~ 4 h.

Previous fabrication relied upon the use of 0.3 μm of nitride isolation for both top and bottom electrodes for a total of 0.6 μm silicon nitride between electrodes to prevent accidental seepage through any pin holes. With the reduced time required for release, the exposure of the top and bottom electrodes to the release etchant through the isolation

nitride is significantly reduced. In addition, it was possible to reduce the isolation nitride by 50% to 0.15 μm for each layer without detrimental effect. It should be noted that for the isolation deposition, to reduce pin-hole effects, the wafers were exposed to atmosphere and rotated twice dividing the deposition into three consecutive segments. This reduction in isolation nitride affects the performance of the CMUT as will be discussed in CHAPTER 5.

Although, judicious layout can be used to improve the yield and reduce the necessary silicon nitride isolation, it was desired to further reduce the equivalent vacuum gap for reduced collapse voltage. In the following section the materials used for the top and bottom electrodes as well as sacrificial layer are investigated to meet the desired goal of reduced isolation layers.

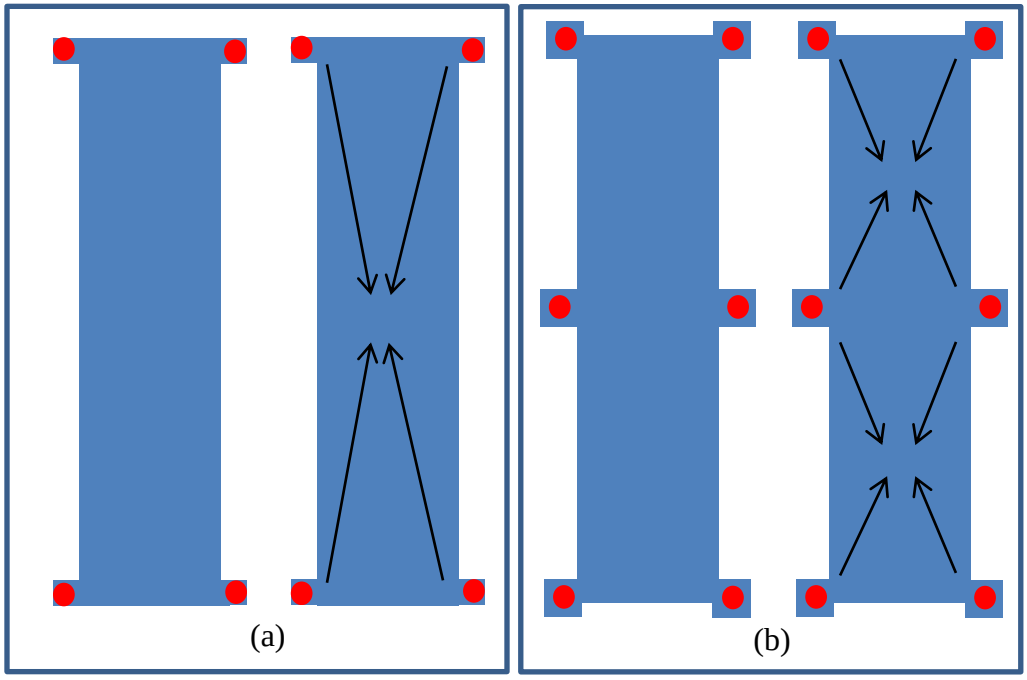


Figure 29. Sacrificial layer and etch directions. Previous sacrificial layout and release etch holes (a) and modified layout (b) to reduce overall time required for release.

3.3. Electrode Optimization with Copper Sacrificial Layer

Further optimization efforts to meet the reduced isolation layer design goals focused on the layers used for the top, bottom, and sacrificial layers, APPENDIX B. Additionally, thorough judicious metal selection, the fabrication robustness is improved.

The exposure to 250 °C temperatures during the PECVD deposition proved to be problematic in the past for the gold and aluminum electrodes for two distinct reasons. For the gold electrode a titanium stiction layer was necessary and the sacrificial layer used was chromium. With this fabrication, three separate metal etch solutions were required, GE-8141 gold etch, hydrofluoric acid diluted in water for titanium, and CR-7s for the chromium layer. The opaque gold etchant proved to be especially problematic for electrode definition as it was not possible to visually verify the state of the process often leading to an over-etching condition. Additionally, fabricated devices were found to be susceptible to detrimental charging effects, limiting the useful lifecycle of the CMUTs to minutes of continuous operation before failure.

Fabrication was modified to use aluminum for the top and bottom electrodes with the same chromium sacrificial layer. This process flow virtually eliminated the charging effect, but the surface roughness increased to as much as 50 nm which led to problematic sacrificial release as it would seep through the isolation to etch the top and bottom electrodes. Therefore, isolation nitride was increased to prevent accidental etching of the electrode material during the sacrificial release. The roughness from the bottom electrode deposition also increased the minimum practical vacuum gap, > 100 nm, and in conjunction with the additional nitride, the collapse voltage increased.

The desired electrode and sacrificial material would meet three criteria: minimal contamination of isolation nitride to prevent charging effects, surface roughness less than 10 nm for smaller vacuum gap fabrication and improved selectivity in that the sacrificial release would not etch the electrode material. Ideally, with these properties, it should be

possible to fabricate devices with a single isolation layer and vacuum gap on the order of 50 nm for improved performance in terms of increased sensitivity, reduced DC bias, and AC actuation.

Further modification of the process flow substituted the top and bottom electrode aluminum for chromium. This mitigated the surface roughness issues but a minimum of 150 nm isolation was still necessary to prevent etching of the electrodes during the sacrificial release.

To meet all three criteria, a process flow was developed using a chromium bottom electrode, copper sacrificial layer, and aluminum silicon top electrode. The sacrificial copper layer was chosen for its ability to be etched with APS-100 which is highly selective against chromium and aluminum,

Table 4 [80]. Additionally, an important feature is its ability to withstand solvents such as acetone and isopropanol that are used during processing for photoresist removal. The bottom electrode, chromium, was selected as a stiction layer for the copper, and it was determined that the subsequent silicon nitride isolation deposition did not adversely affect the surface roughness. The top electrode material, aluminum, was found to be superior to chromium. It was observed that if chromium was used as a top electrode, it would delaminate for certain electrode configurations. This is most likely due to a combination of material properties such as the thermal expansion mismatch during the 250 °C nitride deposition, Table 5.

Table 4. Etch rates for Cr, Al, Cu

Metal	**CR-7s**	**Al-Etch Type A**	**APS-100**
Chromium	150 nm/min	-	0 nm/min
Aluminum	3.8 nm/min	530 nm/min	<0.3 nm/min
Copper	280 nm/min	>2900 nm/min	2500 nm/min

Table 5. Material Properties of Cr, Al, Cu, Si

Metal	Linear Coefficient of Thermal Expansion	Modulus of Elasticity	Electrical Resistivity
Chromium	4.9×10^{-6}/C	279 GPa	125 nOhm/m
Aluminum	23×10^{-6}/C	70 GPa	28.2 nOhm/m
Copper	17×10^{-6}/C	115 GPa	16.78 nOhm/m
Silicon	3×10^{-6}/C	150 GPa	-

For improved adhesion the chromium and copper layers are deposited in the same run under vacuum, and as such the process flow order was modified as the chromium etchant, CR-7s, aggressively etches copper. A detailed process flow can be found in APPENDIX B and a summary of the modified process is listed in Figure 30. It is important to note the reversal of the bottom electrode definition and sacrificial layer definition. By defining the sacrificial layer first, the following bottom electrode masking protects the sacrificial copper from the CR-7s. As long as the bottom electrode is larger than the sacrificial regions, as is the case for typical CMUT fabrication, this process is acceptable. Figure 31 shows a patterned bottom electrode and sacrificial layer where the bottom electrode has been modified with an increase in size, radially ~ 3 μm, to ensure proper protection. Figure 32 shows top electrode aluminum definition without detrimental etching of the copper sacrificial layer which is important to note as the Al-Etch Type A is not selective to copper as listed in
Table 4.

An additional advantage to using the copper sacrificial is the tolerance to misalignment of the sacrificial release holes which leads to an improvement in the yield. Figure 33 shows a linear array with dual top electrode structure where the release holes are misaligned by ~ 2 μm in the horizontal direction. Previous fabrication would not be tolerant to such misalignment. For this fabrication with misalignment, the bottom chromium electrode also acts as an etch stop preventing accidental etching of the substrate.

A 40 MHz test array comprised of 20 µm x 20 µm membranes was fabricated with 50 nm gap and 120 nm of silicon nitride isolation using the copper sacrificial process. The measured collapse voltage was found to be 70 V DC which is a reduction from the previously measured figure of 180 V DC from a fabrication with 100 nm gap and 300 nm gap using the chromium sacrificial layer. The surface roughness was measured to be on the order of 10 Å after isolation deposition, and measurement taken with a network analyzer, Agilent 8753ES, showed minimal performance degradation over time. Figure 34 shows the real and imaginary parts of the electrical impedance measurements of the CMUT array element with an initial measurement and after 12 h with a constant 60 V DC bias applied.

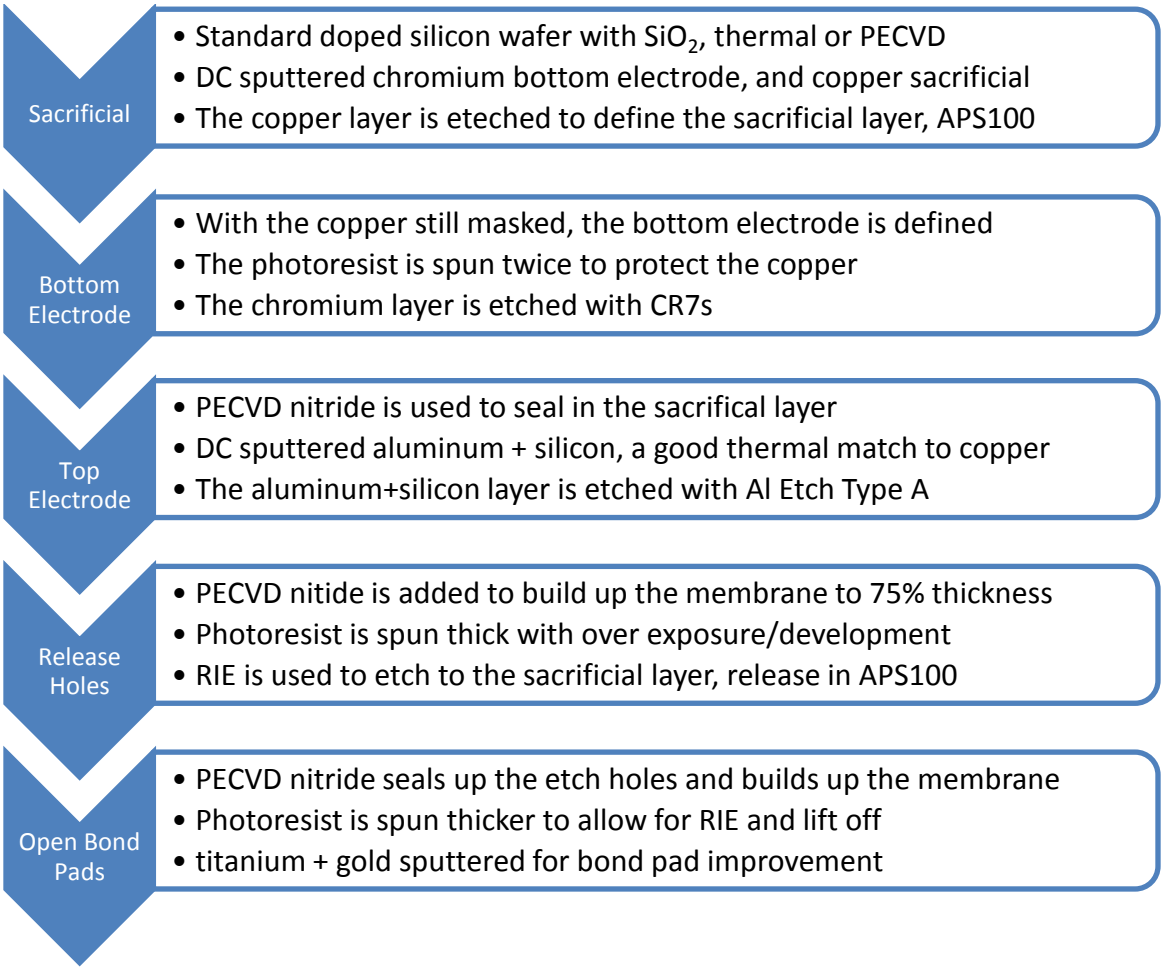


Figure 30. Modified process flow using the copper sacrificial layer.

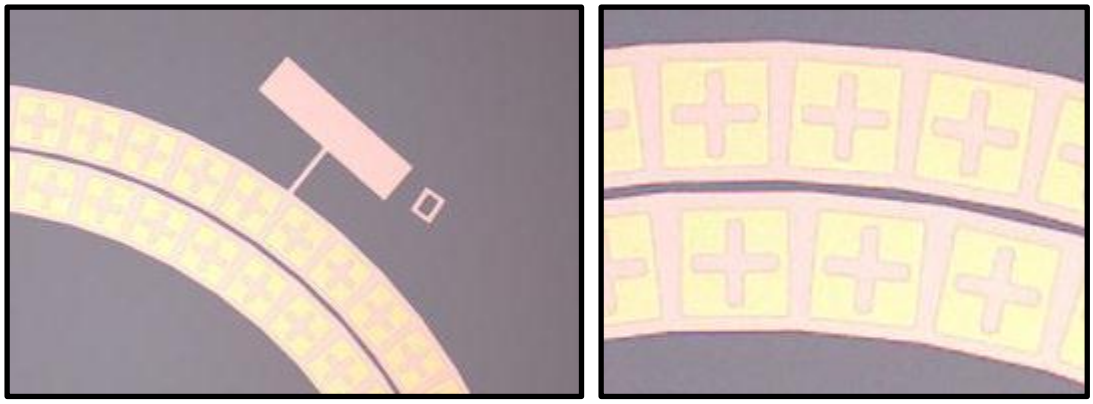


Figure 31. The chromium bottom electrode and copper sacrificial layer are shown where the bottom electrode has been enlarged by ~ 3 µm radially to protect the sacrificial copper during the wet etch definition.

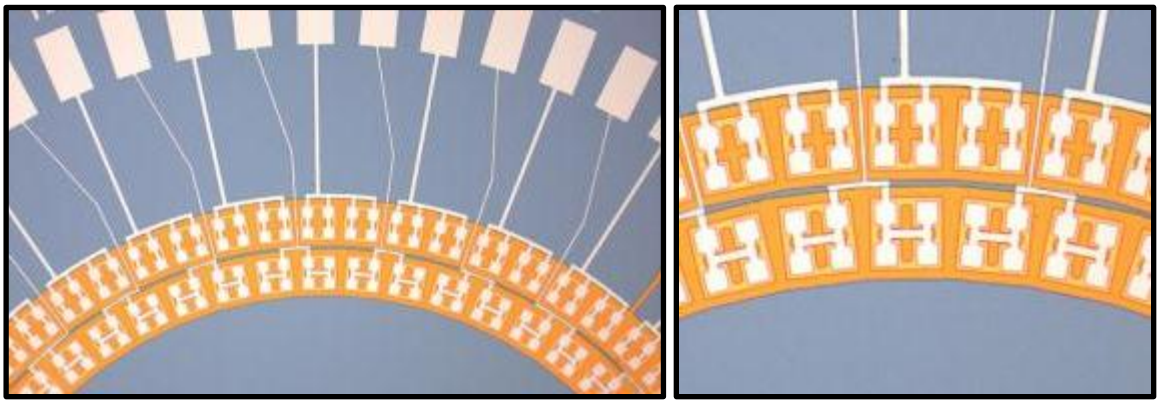


Figure 32. Aluminum top electrode definition shows no delamination and the patterning is shown to not affect the sacrificial layer.

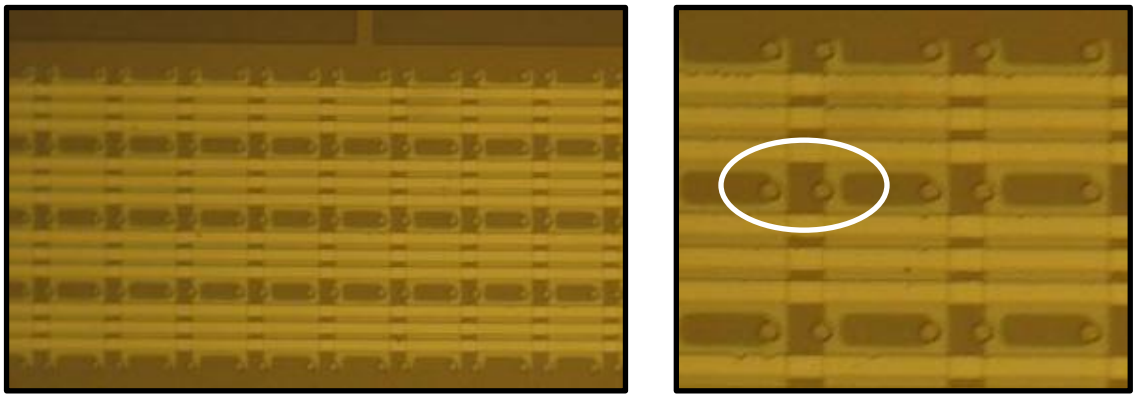


Figure 33. A functional released CMUT linear array employing a dual top electrode is shown with sacrificial release hole etch locations misaligned in the horizontal direction by ~2 µm without detrimental effect.

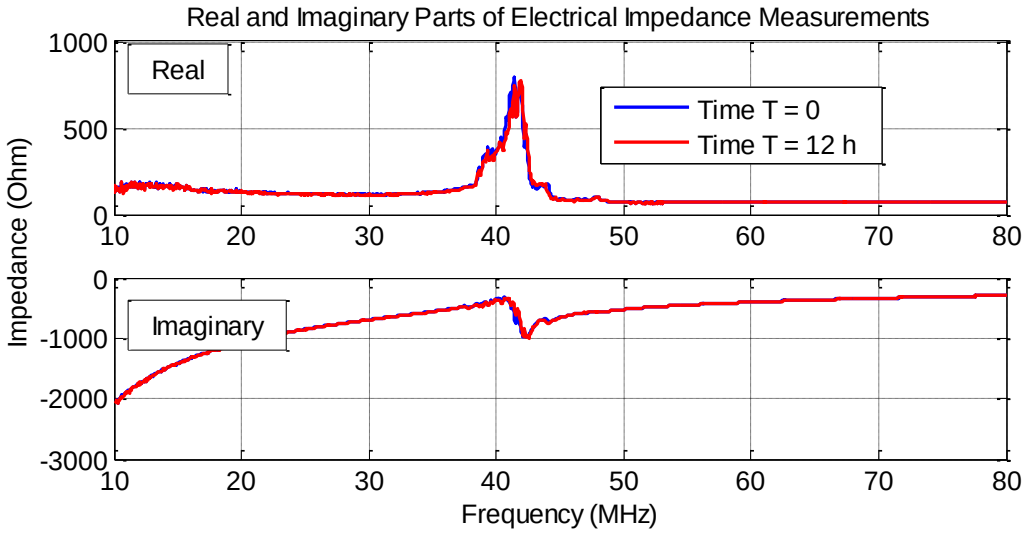


Figure 34. Real and imaginary impedance measurements of a 40 MHz CMUT array in air with a 60 V DC bias over time show no deviation in magnitude or resonance indicating minimal charging effects.

3.4. CMUTs on CMOS Fabrication

One of the most important promises of capacitive micromachined ultrasonic transducer (CMUT) technology is integration with electronics. This approach is required to minimize the parasitic capacitances in the receive mode, especially in catheter based volumetric imaging arrays where the elements need to be small. Direct integration with electronics not only increases the signal-to-noise (SNR) of CMUTs by decreasing parasitic capacitances but also significantly reduces the complexity of design while optimizing the use of catheter tip real estate. Furthermore, optimization of the available silicon area and minimized number of connections occurs when the CMUTs are fabricated directly above the associated electronics. For an ideal case, the electronic and CMUT design parameters should not significantly affect the other. Additionally, the process flow for the post processing of CMUTs on electronics should keep additional steps to a minimum so as to preserve the yield. The CMUT-on-CMOS approach developed attempts to meet these criteria.

3.4.1. CMUT-on-CMOS Integration

A CMUT-on-CMOS process, described in the following section, has been pursued as an integration scheme where the CMUTs are directly fabricated above associated electronics as depicted in Figure 35 as a good compromise with advantages in optimal space utilization, minimal parasitic capacitances, and relative ease of fabrication and final assembly. This interconnect approach minimizes parasitic capacitances associated with connection lines while introducing only one additional masking step. As mentioned previously, the real estate is optimized as the CMUTs are located directly over CMOS and the fabrication modifications can be easily implemented as the fabrication is not constrained by the CMOS processing with the exceptions of the 400 °C thermal process limit.

The following considers CMOS integration with dual-ring CMUT ring arrays for forward-looking intravascular ultrasound (FL-IVUS) which have a small element size, 70 µm x 70 µm, comprised of four individual membranes 35 µm x 35 µm. Estimated parasitic capacitances associated with a single Rx element up to the point of connection to an amplifier, shown in Figure 35, are reduced by more than a factor of 200 as compared to wire bonding by monolithic integration as numerically calculated, Table 6. The TIA input capacitance, which was used in this study, was simulated to be 400 fF.

Table 6. Array Element Connection Capacitance Comparison

Parameter	**DRA Wire Bond Connections**	**DRA CMOS Connections**
Receiver Element (CMUT)	114 fF	114 fF
Connection Line	42 fF	11 fF
Bond Pad	239 fF	-
Wire bond	2 pF	-
Total Parasitic Capacitance	2.281 pF	11 fF
Parasitic to CMUT Ratio	20:1	1:11

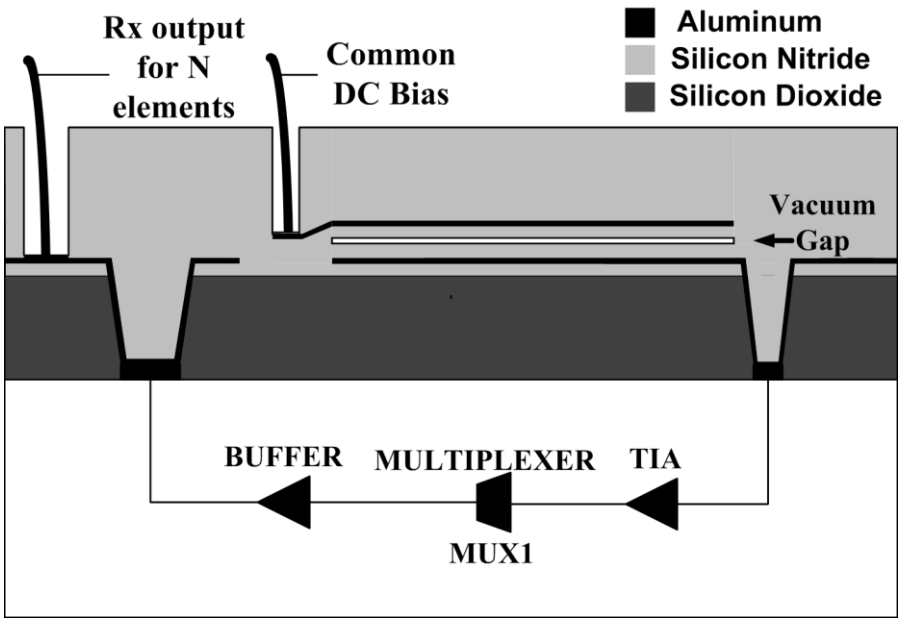


Figure 35. Cross-section schematic of the CMUT on CMOS membrane and the critical metal interconnections made to CMOS electronics. Receive elements are connected and divided between multiplexers for receiver output signals and all receive elements are connected to a common DC bias. Dual ring arrays use four multiplexers, MUX1-4, to route one output from a group of 8 or 16 receive channels for parallel output.

3.4.2. CMOS Wafer Substrate

The CMUT-on-CMOS approach developed begins with the custom CMOS electronics fabricated through the TSMC's 0.35 μm processing technology on 200 mm silicon wafers with 48 repeated squares per wafer as shown in Figure 36 (a). Each square contained many die with a variety of designs with multiplexers and trans-impedance amplifiers (TIAs) for the different CMUT designs.

These wafers were subsequently diced yielding 6 rectangular blocks approximately 4 cm x 7 cm (3 x 2 die) to allow for CMUT fabrication using standard micromachining tools designed for 100 mm (4 inch) wafers as shown in Figure 36 (b). No carrier wafers were used as the lithography tools utilized accepted rectangular samples. However, due to its rectangular shape, processing uniformity is adversely affected in the upper right and lower left corners of the CMOS block as indicated in

Figure 36 (b). This result was attributed to the pooling of photoresist in the corners of the rectangular blocks during the photoresist spinning process.

Through profilometer scans, it was found that layers from the CMOS can protrude as much as 1 μm in critical regions where CMUTs are fabricated. Subsequent CMUT processing on such topography lead to problems such as open circuitry in the CMUT metallization layers as well as non-uniformity in CMUT geometry as shown in Figure 37.

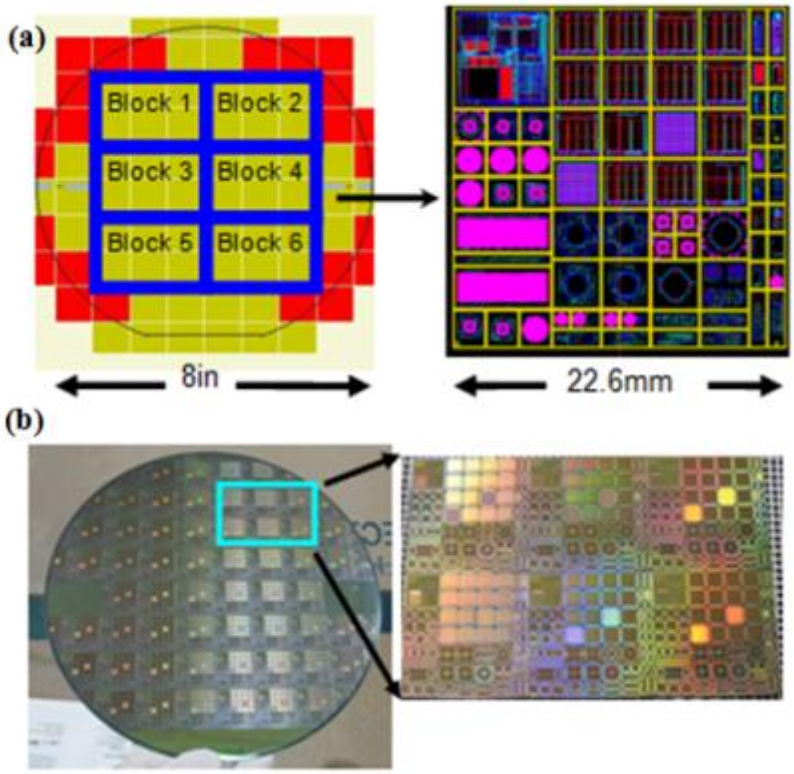


Figure 36. The repeated squares and block dicing lines are shown on the left with a magnified view of an individual square with die on the right, (a). The custom 200 mm CMOS wafer is shown on the left with a diced block on the right, (b).

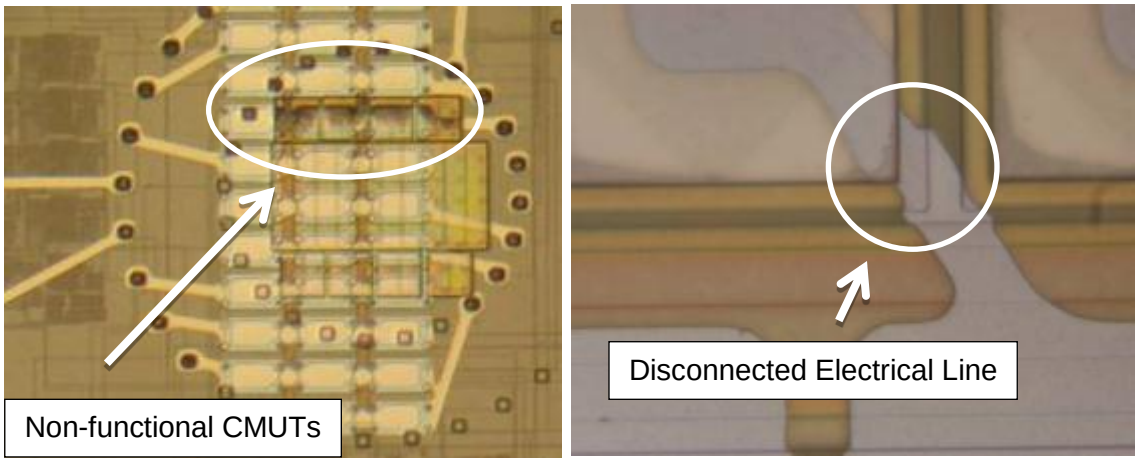


Figure 37. Topography of the CMOS electronics. CMUTs fabricated with non-functional elements on the left and a failed electrical connection on the right.

3.4.3. Polishing

To address the CMOS topography, planarization through mechanical polishing was pursued. A 3 µm layer of PECVD silicon dioxide (SiO_2) was deposited to electrically isolate the bottom electrodes of the CMUT devices from the CMOS electronics beneath while providing extra base surface material to be removed during polishing. Figure 38 (b) displays the profilometer scan of the CMOS surface taken after the oxide deposition. The oxide layer was then planarized using a Logitech PM5 automated polisher with Leeco 1 µm aluminum oxide slurry for approximately 3 h. Profilometer scans showed that the surface topography had been significantly reduced, and all previously observed steep slopes had been polished down to very gradual inclines of less than 0.5 degrees from the horizontal, Figure 38 (c). Residual slurry contamination from the polishing process was removed in an ultrasonic cleaner in acetone and if necessary, a dip in Aluminum Etch Type A which attacks aluminum oxide but not the SiO_2 layer. Further surface preparation included 0.2 µm of PECVD silicon nitride deposition after polishing to improve stiction with the first aluminum layer in the CMUT process which also forms bond pad regions. In previous fabrication, the bottom electrode

metal layer would often delaminate from the polished oxide surface during wire bonding. This approach improved the wire bond success rate from approximately 10% to near 100%. The silicon nitride addition was preferred to oxide as previous testing revealed that it exhibited better bond pad adhesion, while etching twice as fast as oxide in subsequent processing.

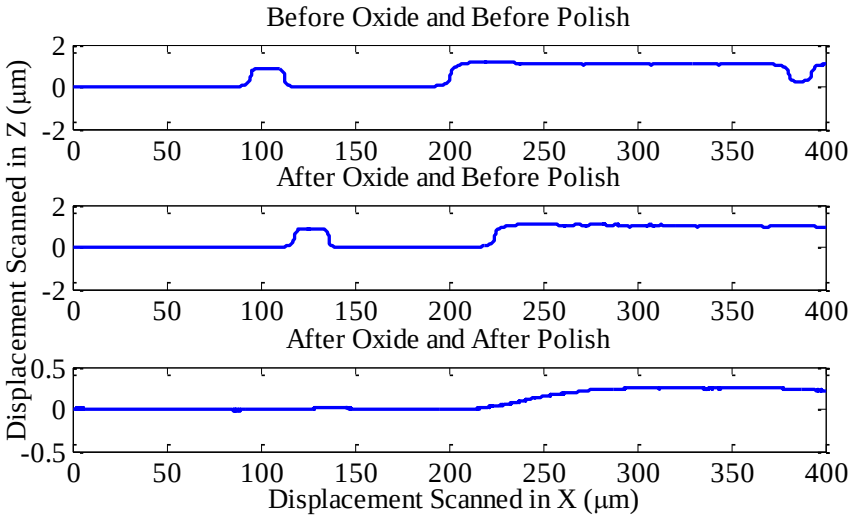


Figure 38. Profilometer scans of the same region shown, (from top to bottom): (a) the initial topography, (b) after 3 μm of PECVD silicon dioxide passivation, (c) after 3 h of polishing.

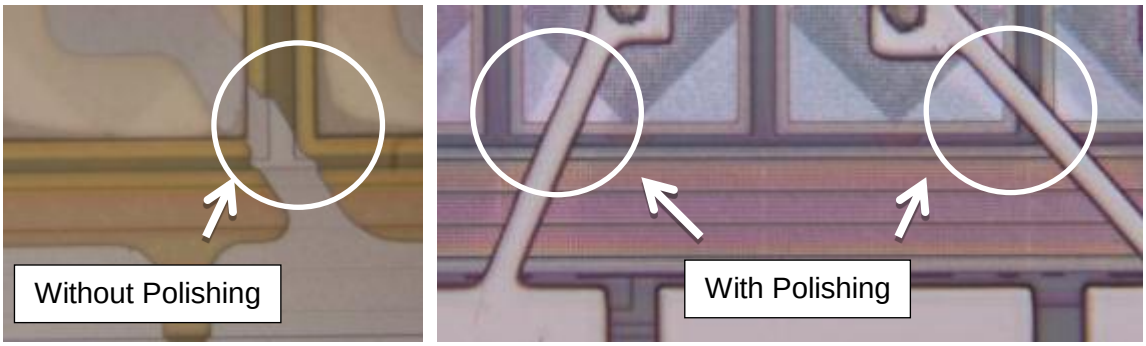


Figure 39. Similar electronics without polishing (left) and with polishing (right). The discontinuity of the connection line has been mitigated through the addition of silicon oxide and subsequent polishing.

3.4.4. CMUT-on-CMOS Via Interconnect

The interconnect scheme developed uses sloped sidewall vias with conformal metal sputtering to connect the CMOS electronics with their respective CMUT elements. The aforementioned custom CMOS wafers were designed with metal posts and bond pads for electrical connection. Figure 40 shows the CMOS electronics for a DRA device with metal connection posts 25 μm x 25 μm for the outer Tx electronics, middle Rx electronics, and inner electronic connection ring. The bond pads on the outside are electrically connected to the inner ring connection posts for testing purposes.

With the CMOS substrate prepared, removal of topography, the CMUT fabrication utilizes the previously described processes. Following the sacrificial layer metallization and subsequent silicon nitride isolation, connection vias are etched into the dielectric layer over the inputs to the CMOS electronics. This is accomplished with a specialized recipe using the Advanced Vacuum Vision 320 reactive ion etch (RIE) so as to produce sloped sidewall vias, Figure 41. Figure 42-left shows etched silicon oxide after 140 minutes and the right shows an amplifier connection post after 160 minutes of etching, right. The following metal deposition, for the CMUT top electrode, is extremely conformal making electrical connection to the CMOS metal layer as shown in Figure 43. This metal layer is patterned accordingly with each CMUT now connected to their respective CMOS electronics. Figure 43-right, shows these vias used for Rx CMUT-CMOS interconnection. Electrical tests were performed with point probes verifying the continuity through two vias with deposited aluminum bond pads connected through a metal CMOS layer. The thickness of the metal trace on the CMOS layer was not known, but with a width of 25 μm and utilizing all metal layers, it was assumed that the internal resistance of the trace would be small. A total resistance on the order of 10 Ohms was measured across multiple samples indicating electrical connections were established through two separate vias simultaneously.

Pulse-echo experiments with devices using this integration scheme have shown a 41 dB SNR which is an improvement from the measured 21 dB SNR from similar experiments which utilized separate, wire bonded, CMOS electronics [54].

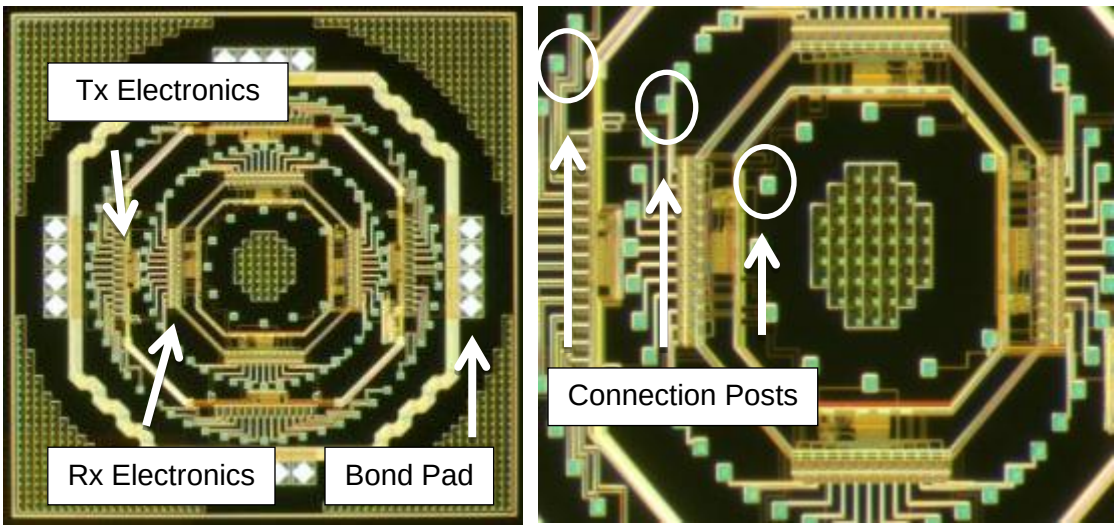


Figure 40. CMOS electronics block for a DRA with Tx and Rx electronics. Bond pads on the outer ring for power, signal, and clock connections.

Table 7. RIE Parameters for Via Interconnect

Parameter	**Set Point**
RF Power	300 W
Pressure	22 mTorr
O_2	6 SCCM
CHF_3	40 SCCM
Etch Rate for PECVD SiO_2	300 Å/min

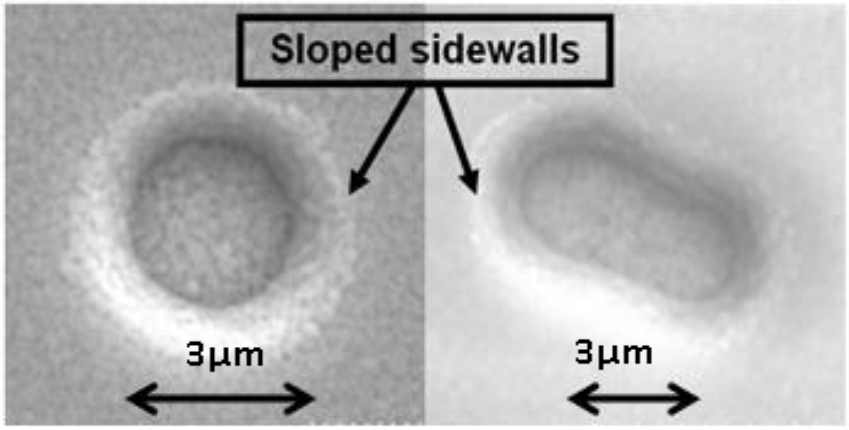


Figure 41. Test connection vias through ~3 µm of silicon oxide using a 5 µm circular mask feature.

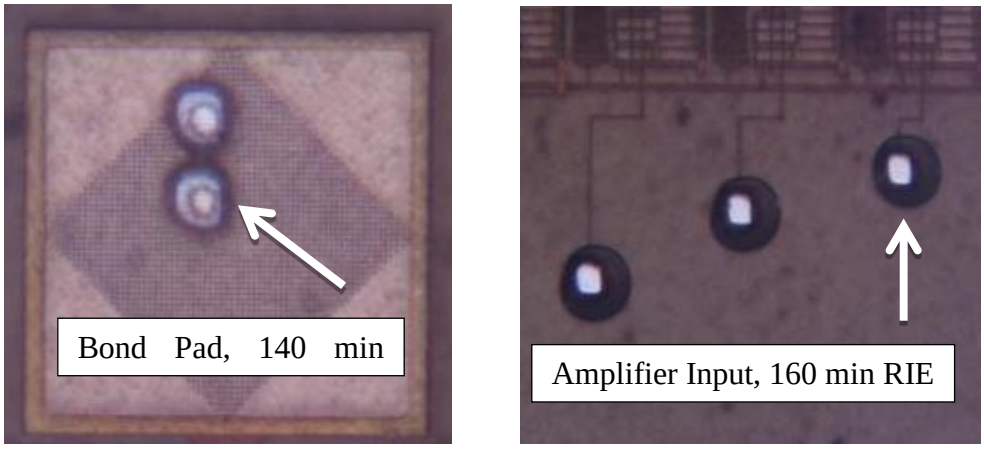


Figure 42. Etched vias over a bond pad location with 140 min of RIE with visible sloped side wall (left) and a via with slight over etching at 160 min at an amplifier input location (right).

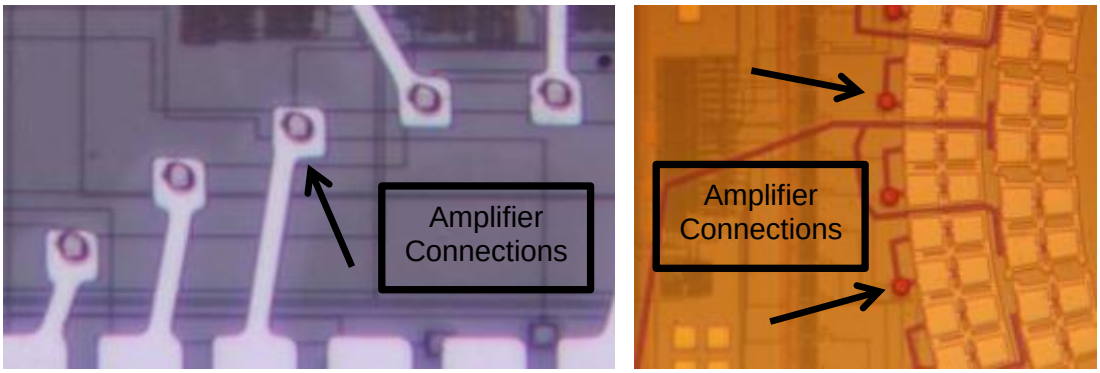


Figure 43. Metal connection to amplifier connections on the CMOS electronics through the use of a connection via.

3.4.5. CMUT-on-CMOS Design and Processing Considerations

During the design phase of the CMOS electronics and associated CMUT masks, certain considerations were kept in mind to ensure reliable integration. First, alignment marks in the shape of crosshairs, were included in the CMOS metal layers that could be observed on the finished electronics for CMUT mask alignment. Secondly, the CMOS electronic connection studs where the CMUT connects to the associated electronic input were defined to be on the top metal layer. The 25 μm x 25 μm studs were larger than the connection etch holes 15 μm in diameter to act as an etch stop during the via opening so that other CMOS layers would not be accidentally etched. The stud and via locations were placed to the sides of the CMUTs as it introduced topography on the order of microns. If the CMUT membrane were to be directly above a via, it could interfere with the membrane performance. The CMUT mask for the metal layer following the via etching, which connected the CMUTs to the electronics, masked the entire via location with ~ 30% additional coverage to prevent accidental etching of the metal studs if misaligned. Additionally, the SiO2 isolation layer thickness should be greater than 1 μm to ensure that there is no dielectric breakdown between the high voltage (100-200 V) bias lines and the underlying low voltage CMOS and ground lines.

Due to the rectangular shape of the CMOS samples, as shown in Figure 36, spun-on photoresists was found to collect at opposing corners forming a thicker region and in crevices formed by the remaining CMOS topography. Therefore it was necessary to over expose and over development ensured proper via opening across the entire sample. Table 8 lists the processing parameters for the positive photoresist Shipley 1827 as modified for via etching. In all lithography steps following the opening of the CMOS connections, Shipley 1813 was used instead of Shipley 1827 with similar over exposure and development. The thinner photoresist coupled with increased exposure and development helped to prevent residual photoresist from collecting in the crevices of the

remaining CMOS topography and preventing shorting of the metal layers. Some of the finer features of the CMUTs suffer from the over-developing in that the sharp corners of the square areas became slightly rounded similar to a chamfered corner. However, testing indicated no significant adverse effects to CMUT performance. As mentioned previously, all processing steps were limited to temperatures no greater 250 °C, so as not to adversely affect the CMOS electronics. Outside of these considerations, standard CMOS and CMUT design rules were adhered to.

Table 8. Shipley 1827 Processing

Photoresist	Spin Rate (RPM)	Ramp Speed (R/s)	Time (s)
SC-1827	2500	500	40
	Pre-Bake	Temperature (°C)	Time (min)
	Lindberg Oven	110	6-8
Exposure	UV Wavelength (nm)	Dose (mJ/cm^2)	
Karl Suss MA-6	405	250-300	
Developer MF-319	Time (s) 110-120	Agitation yes	

3.5. Catheter Interconnect Development

Catheter integration benefits from CMUT-on-CMOS fabrication through batch fabrication, but still requires integration into a catheter with electrical connections to external hardware. The assembly and packaging of electronic components, integrated circuits, and sensors has become an important issue with the associated cost often superseding the actual cost of the components to be integrated [81]. The motivation for this interconnect development is to achieve simple, reliable, integration of the CMUT-on-CMOS array on the tip of the catheter.

Wire bonding methods, first developed by Bell Labs in the 1950's, have been used in the manufacturing of the IVUS catheters where the transducer assembly can be wire bonded to associated electronics with subsequent communication and power cables attached or bonded to the electronics as depicted in Figure 44. Bonding methods fall into three categories, thermocompression, ultrasonic, or a combination of the two, thermosonic. Wire bonding has proven to be a reliable technology used with billons of devices each year. However, electronics failure is still commonly attributed to a failure in wire bonding. Wires used for bonding, typically aluminum and gold, start at 15 μm but continue up to hundreds of micrometers for power applications [81]. Wire bonding affords a certain amount of flexibility during the integration as the wires can be bent into an appropriate configuration. However, dedicated bonding locations are necessary on both the transducer and electronics which can consume valuable real estate especially with respect to FL-IVUS where the size of the bond pad approaches the size of the actual transducer.

Another technology for electronics integration, was theorized more than a century ago with patents issued as early as 1903 describing flat metal conductors on paraffin coated paper [82]. This flexible circuit technology, often referred to as flexible printed circuit boards, are prevalent in a variety of products commonly made from conductive filled polymers or metals on a dielectric film and can be manufactured with multiple layers and with plated through hole connections [83].

The following section will briefly discuss integration efforts utilizing both wire bonding and flexible circuitry to meet the objective of CMUTs-on-CMOS catheter integration.

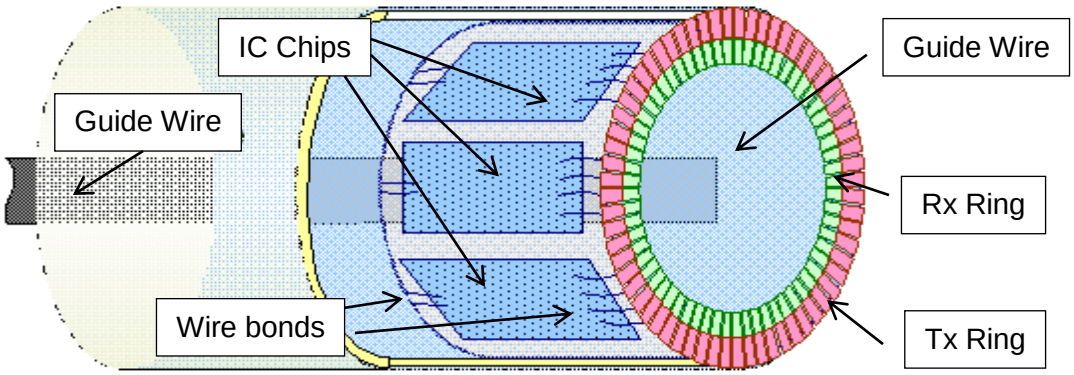


Figure 44. Diagram of FL DRA arrays wire bonded to IC chips and additional signal lines.

3.5.1. Flex Tape Integration

Flexible circuitry, also compatible with industry standard wire bonding techniques, is a promising technology to alleviate a portion of the catheter integration complexity. Through careful design of the electronics, transducer arrays, and flexible integration circuitry, an optimal combination should be achievable to reduce the overall cost and time necessary to produce IVUS catheters.

The use of flexible circuit technology to integrate electronics with transducers has been previously reported, and an example of a CMUT ring array integrated with electronics is shown in Figure 45-left [50, 53, 84, 85]. This array uses through silicon vias to establish electrical connection through the backside of the CMUT array with the flex circuit. Respective electronics are also bonded to the flexible circuit along each of the 8 radial strips. Also shown in Figure 45-right is a test CMUT array fabricated for testing purposes, and using top side bond pads, connections were established to a flex circuit manufactured by RWTH Aachen University, Germany comprised of Polyimide and gold. The CMUT array consisted of three separate elements, an inner center CMUT, middle ring of 6 CMUTs and outer ring of 12 CMUTs. The wire bond pads at the termination measured 150 µm x 150 µm with traces 40 µm in width using solder bump technology for interconnection. The resonant frequency measured in air, for the wire

bonded case, was measured to be 13.8 MHz, 13.9 MHz, and 13.9 MHz for the elements center to outer respectively with a 50 V DC bias well below the collapse of 100 V DC. The array with flex tape was measured and found to have similar resonances +/- 0.1 MHz, most likely due to processing variation as shown in Figure 46-top. The array as shown in Figure 45-right was found to be functional during pulse-echo operation in oil with no difference in amplitude or frequency response from a similar array tested via direct wire bonding, Figure 46-bottom.

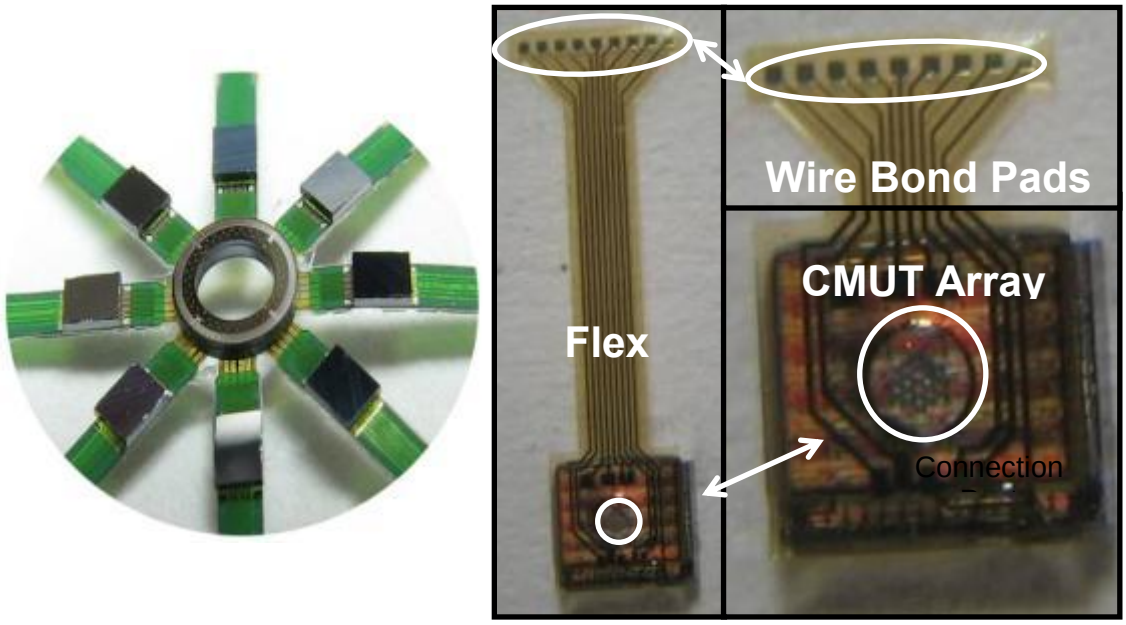


Figure 45. Flexible interconnect technology showing a CMUT ring array integrated with electronics via TSV and flexible circuitry [50] (left) and a test CMUT array connected to flexible circuitry via top side bond pads (right).

A second generation of flexible circuit was designed for topside connection to the custom CMOS electronics via pad locations on the inner ring electronics posts as shown in Figure 47 The electronics connection on the flex tape are ~ 40 µm in diameter with 20 µm traces. Bond pad locations were staggered to allow for a larger connection area, 550 µm square, Figure 47 (c). A sample CMUT array is shown in Figure 48 where select regions in the CMOS electronics were etched completely to allow for pass through of the flex tape to the back side. However, electrical connections to the front side are not ideal

in so far that the bond locations for the flex tape require significant real estate. Additionally, the flex connections may interfere with the operation of the transducer from adhesive glue spreading and possible flex tape overlap.

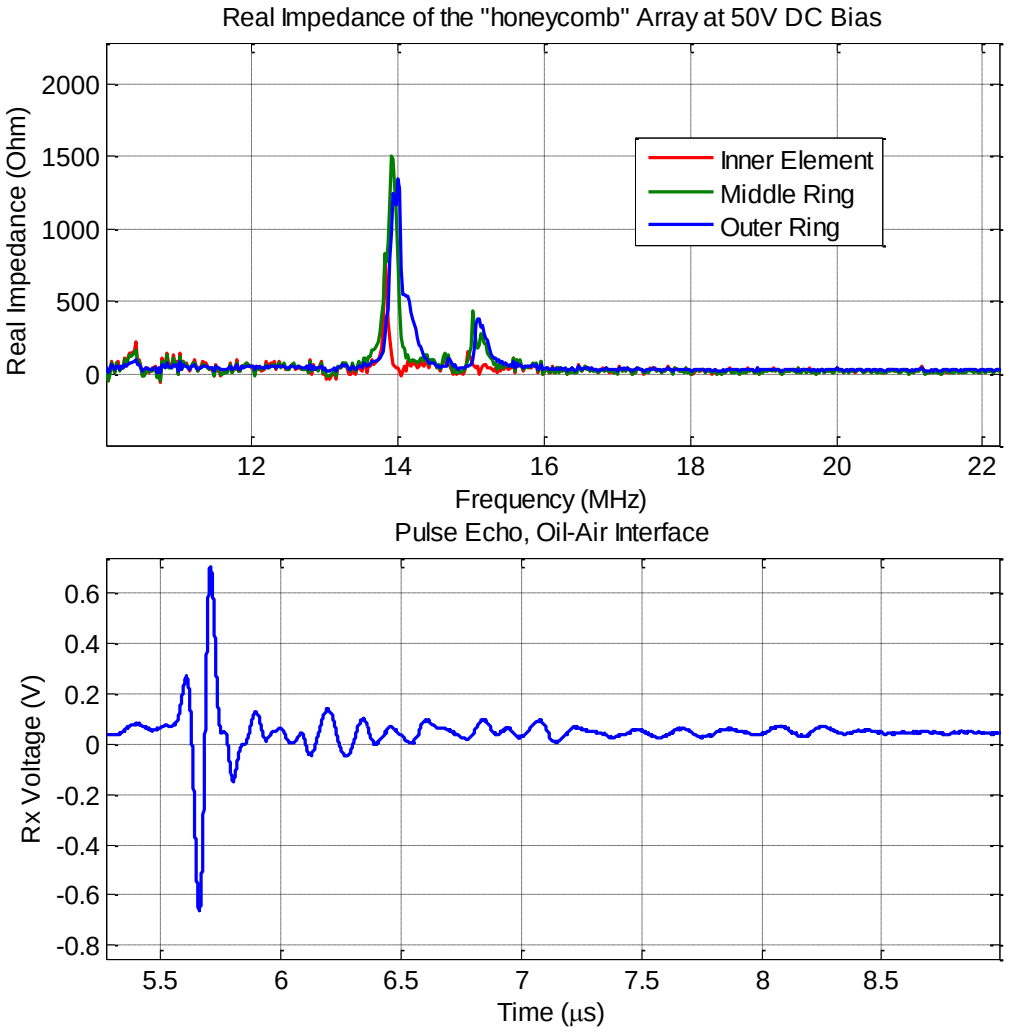
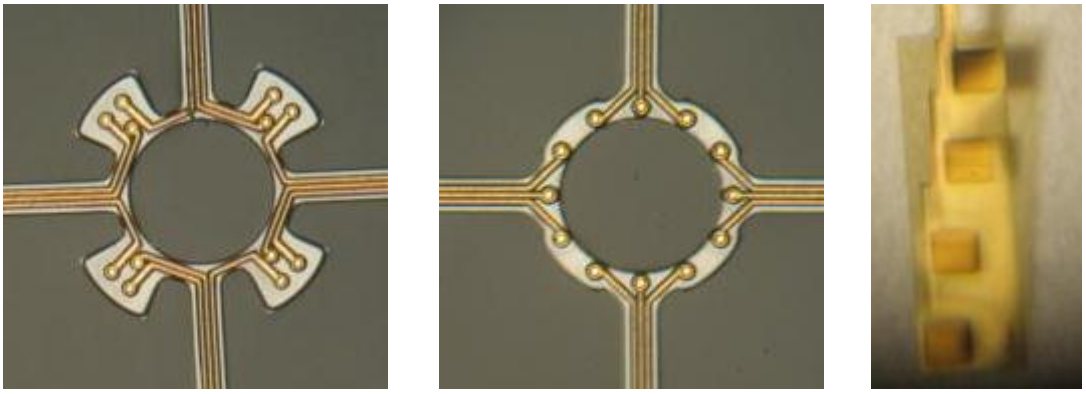


Figure 46. The resonances in air for the three elements of the "honeycomb" type CMUT array with the flexible circuit attached are shown indicating functional devices (top). A pulse echo from an oil-air interface from the same array with the flexible circuit connected (bottom).

To improve upon the initial top side connection scheme, it was proposed that through silicon vias (TSVs) would allow for flex tape connections on the backside of the CMOS eliminating any issue with adhesive contamination while minimizing the topside real estate used for integration. Figure 49 depicts a possible optimized flex circuit as

idealized in Figure 49 (a). A forward-looking dual-ring array is integrated with side-looking annular-ring arrays utilizing the TSV back side connections, Figure 49 (b). With an additional switching circuit, the forward-looking mode of operation can toggled to a side-looking mode of operation to preserve the reduced cable count. With the arrays in place, the flex circuitry can be folded in place around the tip of the catheter, Figure 49 (c) and wrapped as necessary, Figure 49 (d). Therefore, integration development was expanded to include the addition of TSVs in the CMOS substrate.



(a) (b) (c)

Figure 47. Two flexible tape rings designed for front side connection to FL-DRA CMOS electronics, (a) and (b) with bond pads for wire bonding (c).

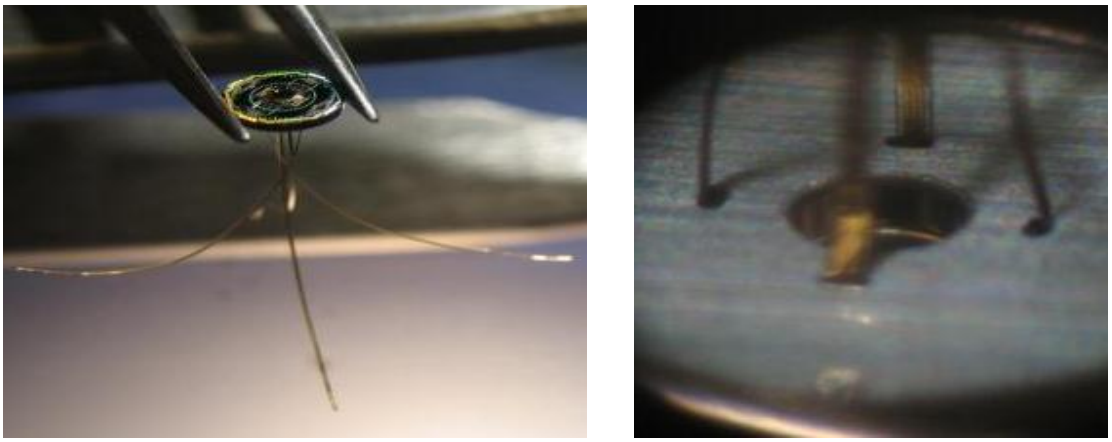


Figure 48. Doughnut shaped CMUT array with flex tape connections to the front of the array and passed through the silicon to the back side for connection to electrical lines.

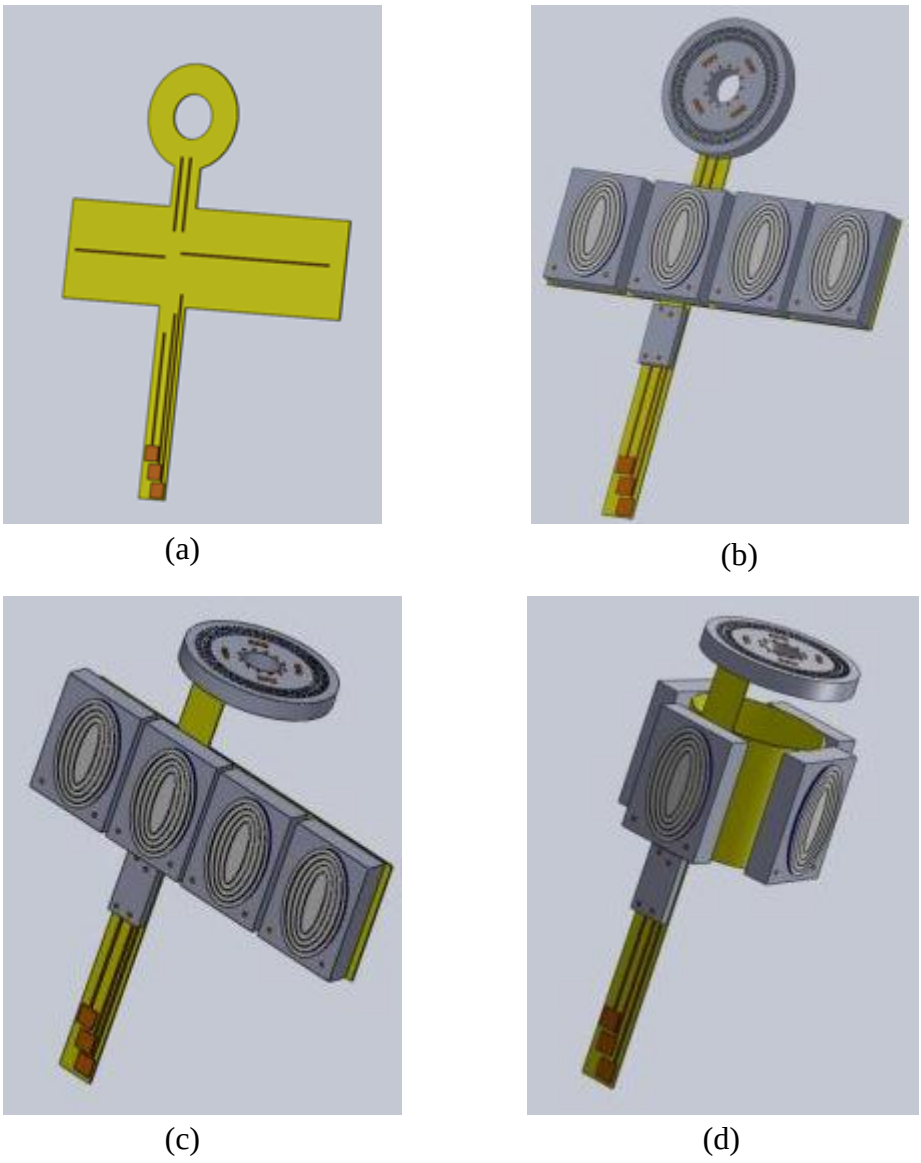


Figure 49. A proposed flexible interconnect method for catheter integration. The flexible tape in (a) is designed for forward looking and side looking arrays. Five CMUT arrays and one CMOS switch circuit attached to the flex tape (b) with a fold (c) and wrap (d).

3.5.2. Through Silicon Via Approach

The use of through silicon via (TSV) technology for CMUT integration had been previously reported where the CMUT's were directly connected to TSVs for back side connection as shown previously in Figure 45. For this configuration, extra parasitic capacitances are introduced between the CMUTs and electronics which can be especially

detrimental when working with DRA devices where the individual transducer capacitances are sub pF as previously described in Table 6.

Therefore, with the ability to fabricate CMUTs on custom CMOS directly, it is desirable to implement TSV's within the CMOS wafer before CMUT fabrication to provide connection to the top side electronics so that the associated parasitic capacitance is inserted after signal amplification and buffering, and therefore its effect is negligible. The second generation of CMOS electronics developed for DRA applications included regions free of electronic traces to allow for flex tape as shown in Figure 48. A forward-looking dual-ring array silicon doughnut is shown in Figure 50-left where the rectangular slots for flex tape, left, are exchanged for three TSV's, Figure 50-right.

To date, TSV's have been integrated with the CMOS electronics pre-CMUT fabrication in regions free of metal traces as shown in Figure 50. The TSV fabrication was accomplished at Georgia Tech by Mr. James Yang of Dr. Muhannad Bakir's research group. The TSV fabrication process is specifically designed to be CMOS compatible with minimal surface topography. This method as described in Yang *et al.* [86] utilizes inductively coupled plasma (ICP) etching to produce high aspect ratio holes through the silicon substrate, on the order of 60 μm in diameter with PECVD silicon oxide for electrical isolation. The fabricated TSV's in Figure 50 were tested electrically with no dielectric breakdown through the substrate up to 200 V DC. Testing of the CMOS electronics, post TSV processing, measured the current draw of the CMOS electronics showing no degradation in performance across multiple samples. Current efforts are focused on optimization of the TSV process in terms of yield and reduction of TSV diameter for compact integration.

With TSV's in the CMOS, it is possible to utilize the same mask set and processing for the CMUT-on-CMOS fabrication. Additional via locations are added to the mask over the TSV locations as well as electrical connection posts as indicated in the AutoCAD mask drawing of Figure 52-left. Electrical connection is accomplished though

the CMUT top electrode metallization. Therefore it is possible to connect the electronics and TSVs within a degree of flexibility. Figure 52-right shows a fabricated DRA with TSV connections. Because of the limited CMOS regions available for TSV fabrication, electrical connections were split between the inner electronics ring and the external bond pad connections which are duplicated connection locations.

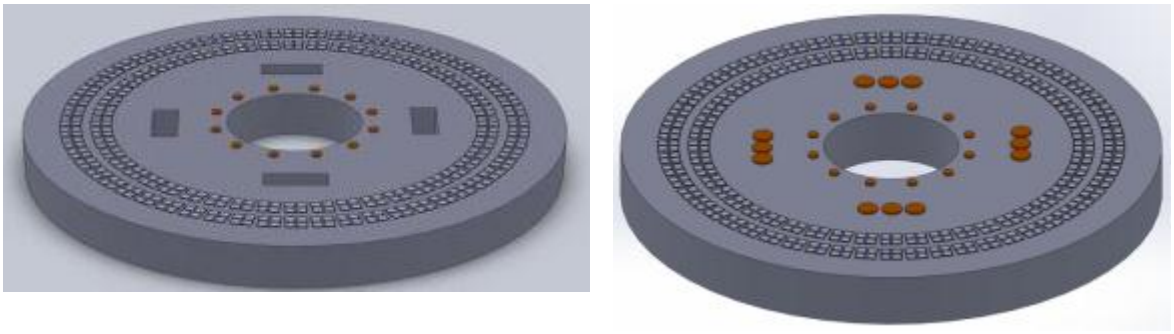


Figure 50. Depictions of DRA's with openings for flex tape (left) and with copper TSV's at the same locations (right).

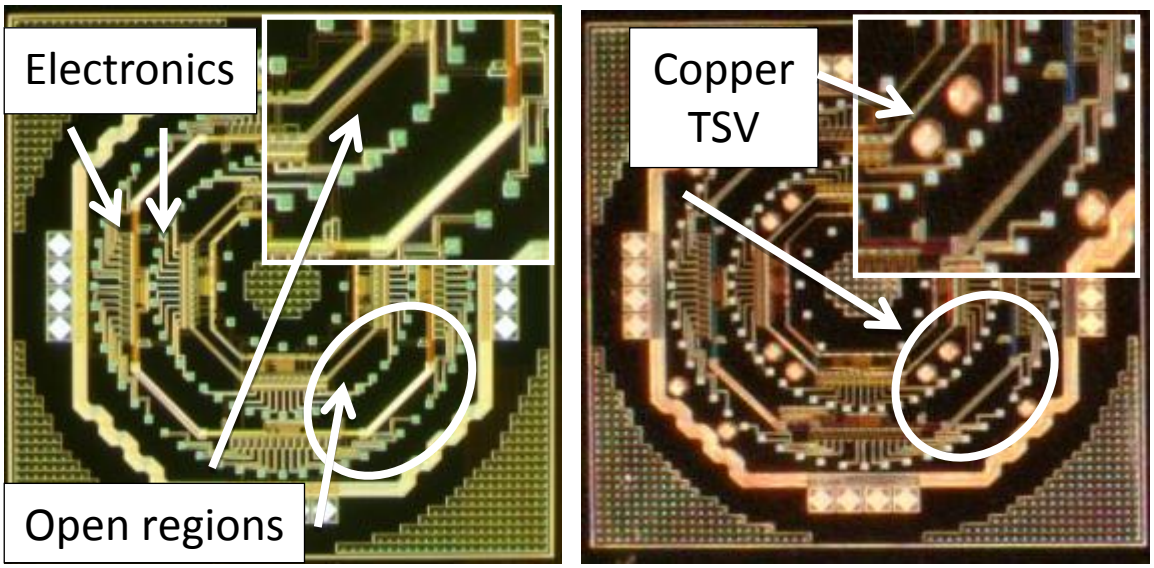


Figure 51. Second generation DRA CMOS electronics with both Tx and Rx capibilities and open regions for through wafer etching.

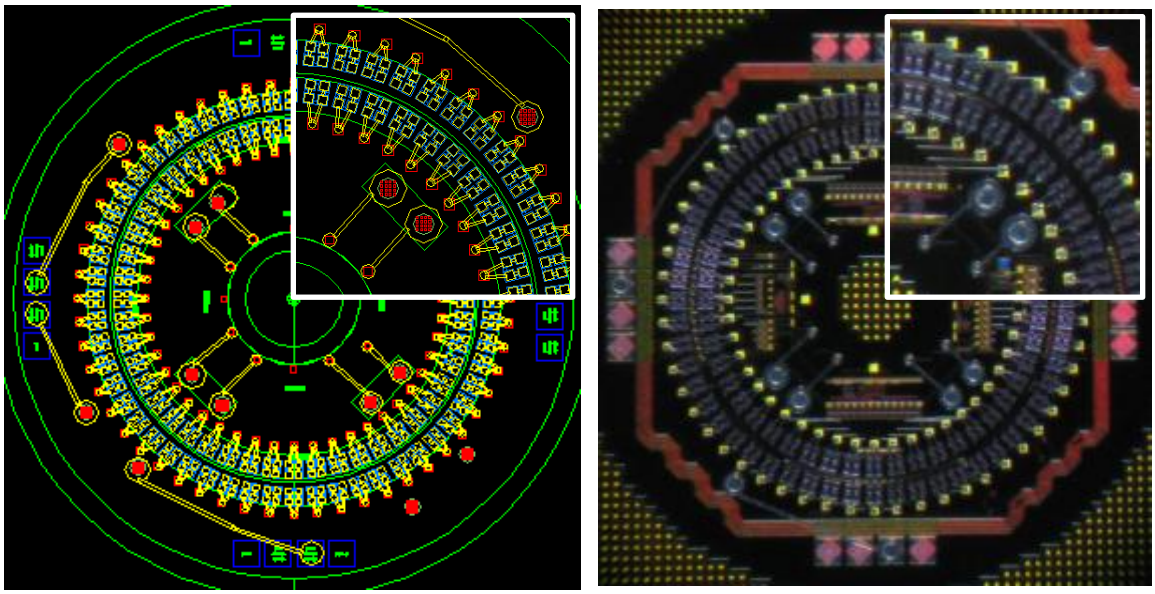


Figure 52. An AutoCAD drawing with via interconnection layer and top electrode metal layer used for connections between electronics and TSVs for back side connection (left) and fabricated array (right).

3.6. Summary

In this chapter the motivation for a reduced vacuum gap and minimal isolation layers was investigated for the purpose of increasing electro-mechanical coupling and reducing the operational voltage. For the dual-ring array element, it was calculated that the collapse voltage can be reduced from 120 V to 42 V with a reduction in the field strength at collapse from 400 V/μm to 280 V/μm by reducing the vacuum gap and silicon nitride isolation.

To achieve the desired fabrication for reduced voltage operation, materials used for the bottom, top, and sacrificial layers were investigated, and it was found that using chromium for all three layers supported robust fabrication with smooth surfaces when two isolation layers are used for protection during the sacrificial release. However this processing required two isolation layers, 300 nm total. Modification of this process substituted the copper for the sacrificial layer and aluminum for the top electrode to allow for the removal of the bottom isolation layer allowing for total isolation of 120 nm.

The CMUT-on-CMOS process presented, allowed for monolithic integration above CMOS electronics using a sloped side-wall vias for efficient and reliable interconnection. This allows for the dual-ring array to be fabricated with reduced parasitic capacitances by a factor of 200. The process developed required only a single additional masking step and is compatible with both CMUT processing fabrication process flows.

For catheter integration purposes, flex tape was fabricated and implemented on standard CMUT test arrays which were shown to be functional with no degradation in performance, signal strength and frequency. The custom CMOS electronics were designed with electrical connections for the express purpose of flex tape integration including regions free of metal traces for through silicon etching to allow for the flex tape to pass through. The flex tape for the dual-ring array was successfully fabricated for multiple designs.

In conjunction with the flex tape, initial development of through silicon vias was accomplished to allow for backside connection. Preliminary results of the TSV fabrication in the regions previously designated for flex tape were shown to not adversely affect the CMOS electronics and were shown to be electrically isolated up to 200 V.

CHAPTER 4

IMPROVED CMUT MODELING

CMUT design optimization based on the desired application such as frequency, bandwidth, and SNR, without the cost associated with fabrication and testing is important for commercialization. Therefore the capability to accurately model and simulate CMUT arrays is an important tool to predict the imaging capabilities and limitations. With the fabrication capabilities improved to allow for reduced silicon nitride isolation and integration with CMOS electronics, the design space can be further explored for optimization.

Ideally the modeling and simulation capabilities need to robust in terms of varied cross-sectional geometry, as well as small signal and large signal analysis in array configurations. Finite element analysis (FEA) of CMUTs meets these requirements with the ability to perform harmonic, transient, and electrostatic simulation. However it can be computationally expensive especially when investigating the effect of array interactions such as acoustic cross-talk and mutual impedance. Therefore, as part of this dissertation, a computationally efficient method of array simulation with the ability to evaluate CMUTs with arbitrary cross-sections, was pursued to assist in the design and layout of the forward-looking and side-looking arrays and will be discussed in the following chapter.

4.1. CMUT Design Space

The design space for CMUT array fabrication includes, but is not limited to, the bulk membrane material and processes used for deposition, the CMUT array surface spacing, and the CMUT cross-section. This allows for many optimizations, some of

which are necessary for compatibility with the electronics integration scheme pursued as described in CHAPTER 3.

Previously fabricated CMUT arrays have utilized high-temperature low-pressure chemical vapor deposition (LPCVD) to produces high quality films. However, it is not compatible with direct, monolithic, electronics integration. LPCVD is an excellent choice for CMUT arrays that are fabricated and then subsequently integrated with electronics via such methods as flip chip bonding. As an alternative, low-temperature plasma enhanced chemical vapor deposition (PECVD) has been used for CMUT fabrication for CMOS integration.

The location and relative placement of the individual CMUT membranes for a transducer array can significantly impact the frequency response, radiation pattern, and cross-talk effects. Recent research has also investigated sparsely filled arrays to reduce the image acquisition time while maintaining the SNR of a fully populated array [87, 88]. And, with the ability to incorporate separate transmit, Tx, and receive, Rx, elements, it's possible to optimize each independently. Real estate is still very much limited when dealing with catheters, so CMUT elements must fit within the allowable area, and separation of Tx-Rx elements may not be ideal.

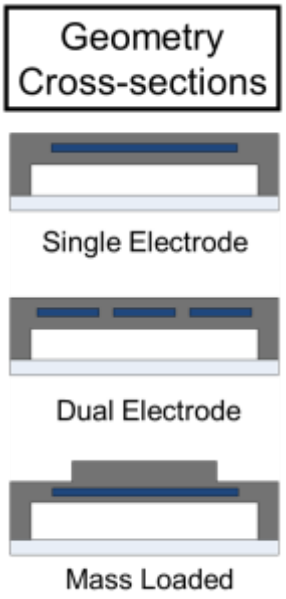
The easiest design optimizations to effect during the fabrication involve adjusting the placement and areas of the different layers such as providing full-electrode or partial-electrode coverage. Geometric cross-sectional changes typically involve separate masking steps, such as the addition of extra mass to the top of a membrane, which increases the fabrication complexity [36]. Table 9 lists easily identifiable parameters useful for optimization. For example, to improve the receive sensitivity, it is desirable to have a small vacuum gap, but not necessarily to improve the transmit pressure [89]. Studies have been performed to optimize the size of the top electrode for a given geometry showing that a full top electrode is not an optimal solution [90, 91]. However,

when the CMUTs for transmit and receive are of the same geometry, optimization is limited to electrical biasing and actuation.

Previously reported optimizations include a dual top electrode structure for linear arrays where the side electrodes can be used for transmit operation for piston like actuation or to pull the center receive electrode closer than 1/3 of the gap for greater sensitivity [32]. CMUTs have also been fabricated with concave bottom electrodes to increase the active area for reduced DC bias and increased bandwidth [92]. CMUTs with mass loading have also been fabricated yielding increased fractional bandwidth along with an improved transformer ratio and coupling coefficients [93, 94].

Table 9. CMUT design matrix with example geometric cross-sections

Parameter	Tx	Rx
Single Electrode, 100% coverage	+	–
Single Electrode, 75% coverage	–	+
Dual Electrode, Side bias only	–	+
Dual Electrode, Side actuation	+	–
Mass Loading	+	+
Small Gap	–	+
Large Gap	+	–
DC Bias ~close to $V_{collapse}$	–	+
DC Bias ~50% $V_{collapse}$	+	–
No DC Bias	+	–



Finite element analysis (FEA) using multi-physics software such as COMSOL or ANSYS has become a well-accepted method used to simulate CMUTs and CMUT arrays. To evaluate CMUT design options, FEA can be used for modal, harmonic, and fully coupled electrostatic analysis in a fluidic environment. As listed above, CMUT

options such as material properties and mass loading can be implemented with relative ease.

To reduce the complexity and computation time of the FEA, symmetry boundary conditions can be applied where appropriate and if appropriate the geometry under investigation can be simplified to a 2D cross-sectional analysis. This 2D analysis can significantly reduce the number of nodes and associated computation time, but it is primarily limited to membranes where the length of the membrane is much larger than the width. Additionally, axisymmetric 2D models can be used for ring type arrays.

However, certain membrane dynamics are not accurately captured using these FEA optimizations that can be detrimental to CMUT array performance evaluation. As CMUT arrays become larger and more complex within the context of optimizing the placement and configuration of CMUT membranes, the use of 3D simulation becomes a necessity.

The following section will describe the development of modeling and simulation efforts to improve upon FEA with the ability to evaluate arrays of CMUTs with arbitrary cross-sections in a more computationally efficient manner.

4.2. Fabricated CMUT Geometry and Array Option Examples

A brief description of previously fabricated CMUT arrays would be beneficial to understand the realistic modeling and simulation parameters for arrays of CMUT membranes. Figure 53 (a) shows a 16 element linear array with overall dimensions of 1.05 mm by 1.7 mm utilizing a dual electrode structure where two columns of membranes are connected in parallel for each element. The individual membranes in Figure 53 (b), 50 μm x 100 μm, are connected in series along each column showing the dual electrode structure with a 15 μm center electrode and 10 μm side electrodes. Figure

53 (c) shows a SEM of linear array with 15 µm x 45 µm silicon nitride mass blocks 1.5 µm thick added to the center of each membrane.

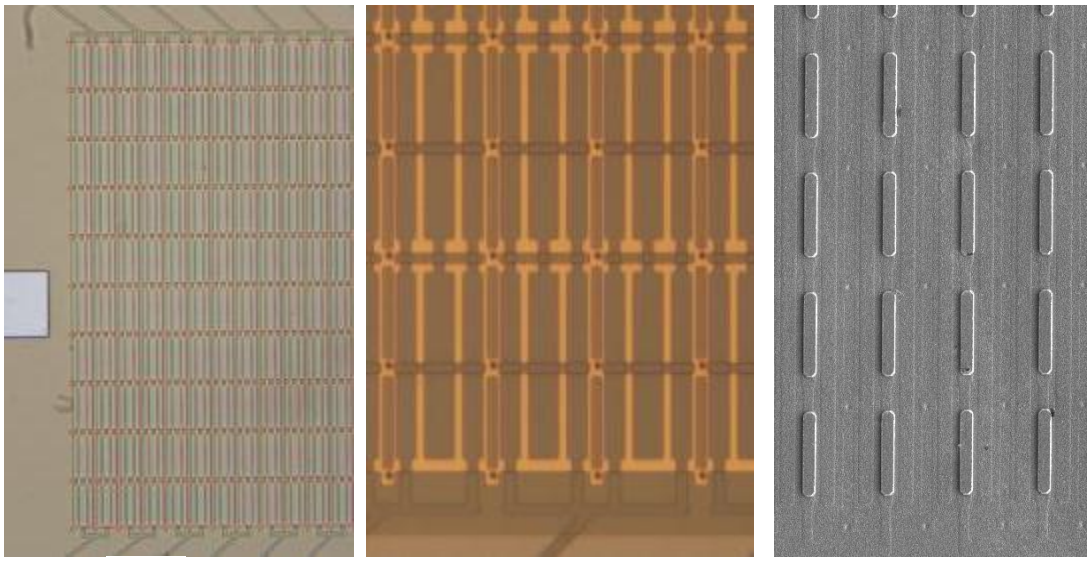


Figure 53. Dual electrode linear array with two rows connected in parallel, (a), individual membranes with side electrodes 10 µm and center electrode 15 µm, (b) and SEM view with additional mass loading (c).

Figure 54 shows a dual-ring array with 800 µm outer diameter and 500 µm inner diameter. It can be seen that the inner Tx ring, 24 elements, is divided into four regions with different electrode configurations. The trapezoidal shape of the membrane transitions from 61 µm in width to 79 µm over 70 µm in the radial direction.

The annular ring array shown in Figure 55 is 840 µm in diameter with 21 separate rings combined to form eight distinct elements. For each ring, curved membranes 28 µm x 60 µm are connected in series as shown on the right side of Figure 55.

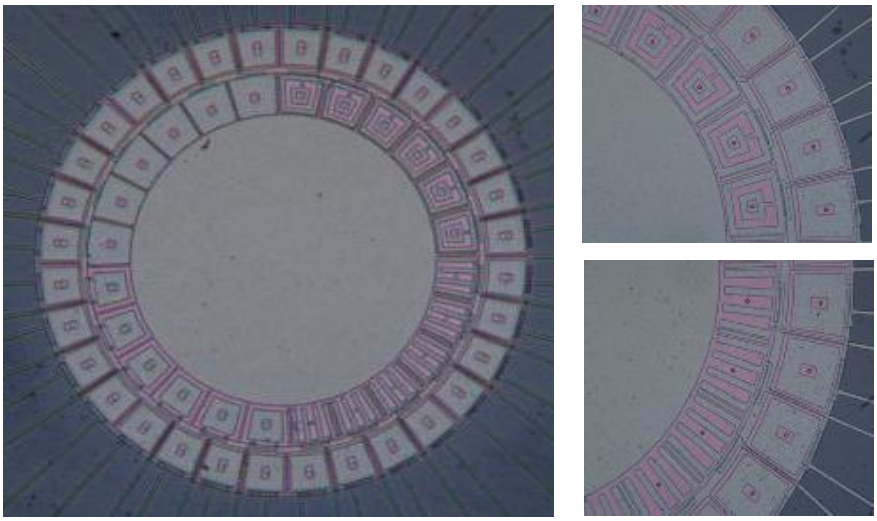


Figure 54. Dual ring array with separate Tx and Rx rings. The transmitter inner ring is shown with experimental electrode configurations.

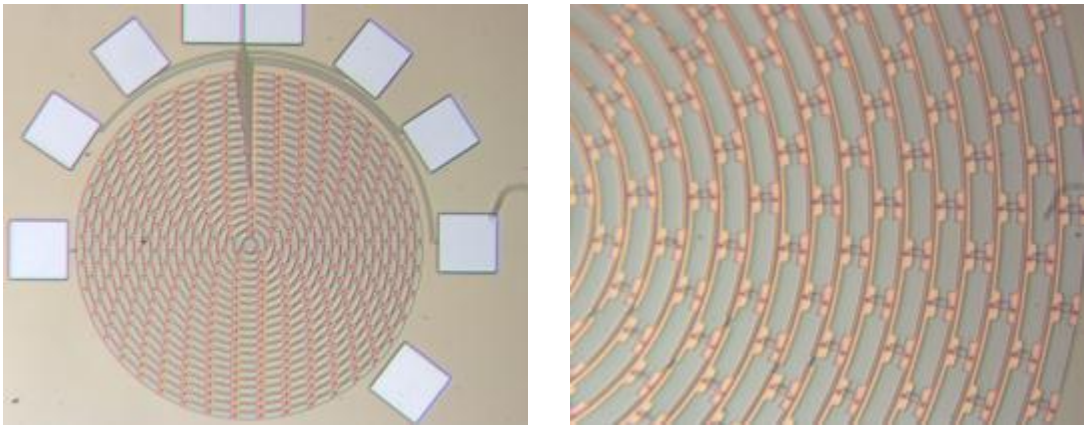


Figure 55. Annular ring array with eight electrically linked rings (left). Individual curved membranes that make up the 21 rings of the eight element annular array (right).

The CMUT arrays described above illustrate the diversity of the surface configurations capable with the micromachining technology used for fabrication. Shapes are not limited to squares or rectangles as in the linear array but can be arbitrary curved shapes as demonstrated by the annular array membranes. For all three configurations, the fabricated vacuum gap was 0.12 μm with 0.6 μm of isolation and membrane thickness 2-

3 μm. The mass loaded array demonstrates the ability to fabricate CMUTs with varied cross-sections.

4.3. Finite Difference Boundary Element Modeling

As an alternative to previous equivalent circuit analysis efforts, finite element analysis (FEA) of CMUTs has been used for analysis in a 3D fluidic environment [95, 96]. Benefits of FEA over equivalent circuit methods include the ability to model complex CMUT shapes and geometries as well as capture higher order modes [27, 32, 93, 97]. Although FEA is well suited for arbitrary configurations, array analysis becomes computationally expensive, predominately associated with the increased number of nodes required to mesh the fluidic environment.

The numerical approach pursued by Meynier *et al*. utilizes finite difference (FD) approximations of Timoshenko's thin plate equations to model the CMUT membranes with fluidic loading accomplished through the use of the boundary element method (BEM) [98, 99]. This method only requires meshing of the CMUT array's vibrating surface area [100]. As this is a 2D surface mesh over the CMUT membranes, the computational load is significantly reduced as compared to 3D FEA. For small signal analysis of CMUT arrays, this model has been shown to be accurate as in the case of thermal mechanical noise modeling of CMUT arrays as presented in [101].

In the following section an alternate method to calculate the stiffness of a CMUT membrane based on static FEA that is used with the BEM. A number of static simulations for an arbitrary CMUT membrane are performed which are equal to the number of nodes used in the BEM matrix. This analysis allows for the modeling of varied edge boundary conditions as well as arbitrary cross-sectional geometry with multiple layers. Additionally, as the stiffness matrix calculated is reused for any similar membrane modeled in the array the computational load associated with the FEA is minimized.

4.3.1. Acoustic Response

This computationally efficient boundary element method to simulate CMUTs in a fluidic environment is based on the force balance in equation (12), where the external applied pressure, p_{ext}, electrostatic pressure in the case of a CMUT, is balanced by the membrane dynamics and fluidic loading, p_{fluid} [98]. In this equation the forces are normalized by the surface area, m is the mass, k is the stiffness, and u is the displacement.

$$p_{ext} = m\ddot{u} + ku + p_{fluid} \tag{12}$$

The pressure associated with the fluidic loading is accomplished through the use of the BEM matrix described below. As such, the transducer surface is divided into a grid with a total of *N* nodes each with an associated elemental surface area, *dx* x *dy*, as shown in Figure 56.

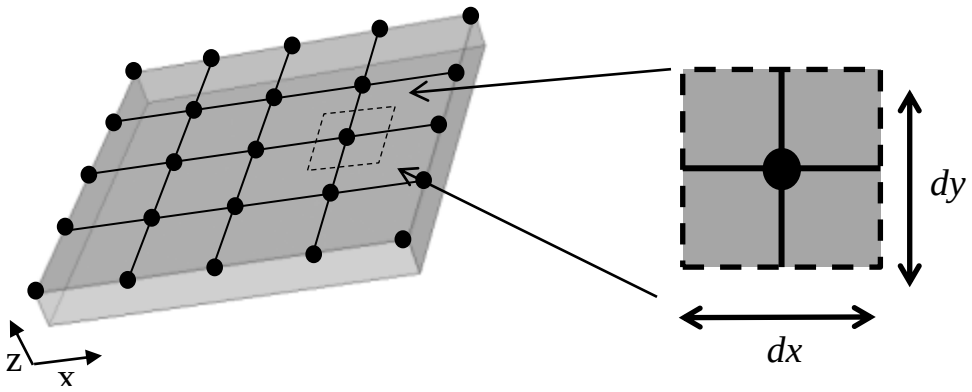


Figure 56. A CMUT membrane divided into a 5 x 5 matrix of nodes, N=25, with corresponding areas *dx* x *dy*.

The linear acoustic response of the CMUT array is calculated with this BEM method by applying a harmonic pressure load on the active electrodes of array elements, and given the membrane and array geometries, the nodal response to the applied pressure can be calculated as:

$$\boldsymbol{u}(\omega) = p_{app}(\omega)\boldsymbol{G}(\omega)^{-1}\boldsymbol{\delta}^{el}. \tag{13}$$

Here $\boldsymbol{G}(\omega)$ is the force balance matrix which is calculated from the stiffness, $\boldsymbol{K}$, mass, $\boldsymbol{M}$, and fluid coupling, $\boldsymbol{Z}_r(\omega)$ matrices such that:

$$\boldsymbol{G}(\omega) = \boldsymbol{K} - \omega^2\boldsymbol{M} + j\omega\boldsymbol{Z}_r(\omega). \tag{14}$$

The sifting vector, $\boldsymbol{\delta}^{el}$, specifies the nodes of the active electrode such that

$$\boldsymbol{\delta}^{el} = [\delta_1; \delta_2; \dots; \delta_n; \dots; \delta_N] \tag{15}$$

and

$$\delta_n = \begin{cases} 1 \text{ if node } n \in \text{active electrode} \\ 0 \; else \end{cases}. \tag{16}$$

The stiffness matrix,$\boldsymbol{K}$, describes how the normal force at a given elemental area influences the displacement of the entire membrane surface. For static loading of the membrane, assuming that the lateral dimensions are much larger than the thickness, the stiffness can be approximated by the thin plate equation:

$$P(x,y) = K * u(x,y) = \frac{\partial^2 M_x}{\partial x^2} + \frac{\partial^2 M_y}{\partial y^2} + \frac{\partial^2 M_{xy}}{\partial x \partial y} \tag{17}$$

where $P(x,y)$ is the distribution of pressure acting on the CMUT membrane. This is given as the flexural plate operator where M_x, M_y, and M_{xy} are the bending moments on an element volume of the membrane where v is Poisson's ratio, E is the modulus of elasticity and h is the membrane thickness equations (18) and equations (19) [99].

$$M_x = D\left(\frac{d^2u}{dx^2} + v\frac{d^2u}{dy^2}\right), M_y = D(\frac{d^2u}{dy^2} + v\frac{d^2u}{dx^2}) \tag{18}$$

$$M_{xy} = D(1-v)\frac{d^2u}{dxdy} \text{ where } D = \frac{Eh^3}{12(1-v^2)} \tag{19}$$

This equation can be written in vector form for a meshed membrane in discrete form

$$\boldsymbol{p} = \boldsymbol{K}\boldsymbol{u} \tag{20}$$

where $\boldsymbol{u}$ is the displacement vector of the surface nodes and $\boldsymbol{K}$ is the stiffness describing the return stresses in an elemental area of the plate [98]:

$$\boldsymbol{K} = \begin{bmatrix} K^{11} & K^{12} & \cdots & K^{1N} \\ K^{21} & K^{22} & \cdots & K^{2N} \\ \vdots & \vdots & \ddots & \vdots \\ K^{N1} & K^{N2} & \cdots & K^{NN} \end{bmatrix} \tag{21}$$

The unique $\boldsymbol{K}$ expression for the force balance at a node is generated through finite difference (FD) approximations to estimate the derivatives used to describe the three bending moments. Each node is a linear function of the nodal displacement values from surrounding nodes and the distance between nodes resulting in a system of force balance equations equal to the total number of nodes, *N*, in the membrane. Therefore in matrix form, the membrane stiffness can be described as an *N* x *N* matrix. The fixed boundary condition sets nodal displacements at the edge and beyond to zero. The stiffness matrix generated using this approach is a sparse matrix containing information that relates one node and its immediate surrounding nodes.

The mass matrix, $\boldsymbol{M}$, is a diagonal *N* x *N* matrix consisting of the local surface density and thickness at each node. For an array with arbitrary membrane geometries the mass matrix is:

$$\boldsymbol{M} = \begin{bmatrix} \rho_1 h_1 & 0 & \cdots & 0 \\ 0 & \rho_2 h_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \rho_N h_N \end{bmatrix}, \tag{22}$$

where $\rho_n$and h_n are the local density and membrane thickness at node n respectively.

The last matrix in eq. (14) is the fluid coupling matrix which couples the nodal displacements through acoustic propagation. The fluid loading on node q due to the

displacement of node p can be expressed as $j\omega Z_r^{pq}(\omega)u_p$ where k is the wavenumber and r_{pq} is the distance between node p and node q.

$$Z_r^{pq}(\omega) = \frac{j\rho_{fl}\omega S}{2\pi}\frac{e^{-j\mathrm{r_{pq}}k}}{\mathrm{r_{pq}}}, \tag{23}$$

This formulation is based on the Green's function of a baffled radiator in a semi-infinite fluid. It assumes that meshing is fine enough that the normal velocity is approximately uniform over the nodal area. Since the Green's function accounts for the radiation boundary conditions of the acoustics problem, the fluid is not meshed in the BEM, which allows for the significant reduction in computational time as compared to FEA [98]. The formulated fluid coupling is included in the force balance matrix in equation (14) as:

$$\boldsymbol{Z}_r(\omega) = \begin{bmatrix} Z_r^{11} & Z_r^{21} & \cdots & Z_r^{N1} \\ Z_r^{12} & Z_r^{22} & \cdots & Z_r^{N2} \\ \vdots & \vdots & \ddots & \vdots \\ Z_r^{1N} & Z_r^{2N} & \cdots & Z_r^{NN} \end{bmatrix} \tag{24}$$

It should be noted that the fluid coupling matrix $\boldsymbol{Z}_r(\omega)$ is symmetric, such that $Z_r^{ij} = Z_r^{ji}$.

As the force balance matrix $\boldsymbol{G}(\omega)$ is calculated, equation (13) can be solved for nodal displacements when the active electrode nodes are excited with the harmonic load $p_{app}e^{j\omega t}$.

4.3.2. Limitations of The Thin Plate Approximation

The thin plate equations used to generate the **K** matrix above inherently limit the numerical modeling capabilities of the FD-BEM approach. For high frequency applications, > 40 MHz, CMUT imaging arrays comprised of membranes 18 μm wide and 3 μm thick, have been fabricated and tested, but are not accurately described by the thin plate equations [99]. Additionally, the interaction with neighboring membranes and attachment to substrate is not accurately reflected in the fixed edge boundary conditions

imposed by the FD approximation. Fabricated CMUT membranes also incorporate a buried metal electrode with thickness typically on the order of 0.1 - 0.3 μm as compared to the bulk membrane material 2 - 5 μm. This is difficult to include in the FD approximation of the thin plate equation as well as any non-uniform membrane geometry such as mass loaded or stiffened membranes [32, 93]. Figure 57 shows a simple square membrane with fixed edge as compared to a CMUT with mass loading, electrode material, and alternate fixed boundary.

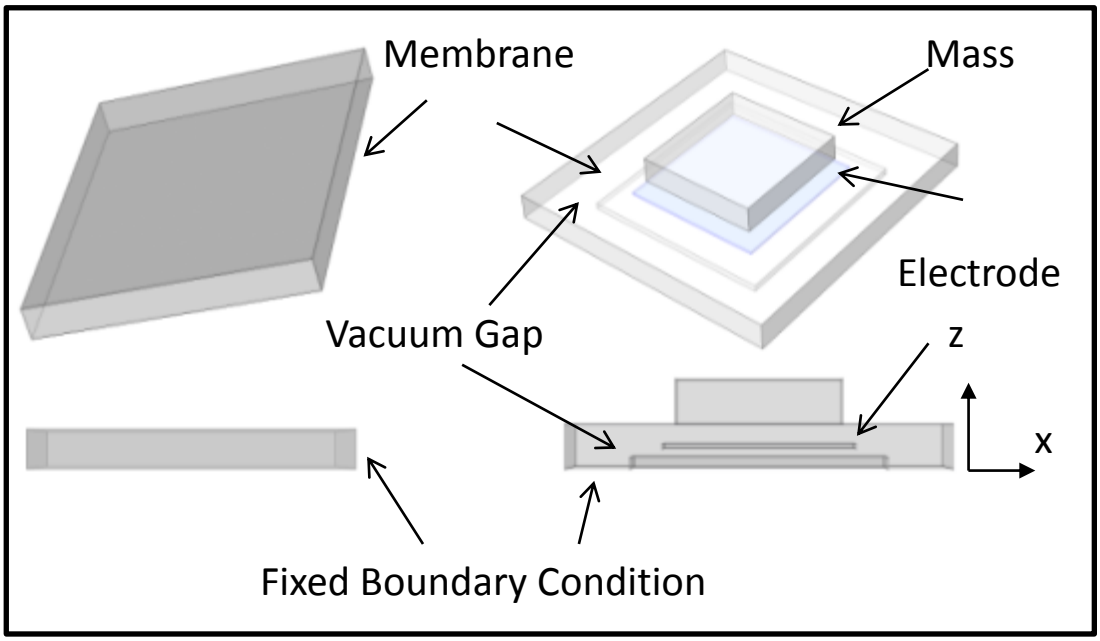


Figure 57. CMUT membrane used for the finite difference calculation (left) and the CMUT membrane used for FEA stiffness calculations (right).

4.3.3. Static FEA for K Matrix Evaluation

To address the main limitations described above, static FEA is used to generate an equivalent stiffness matrix, $\boldsymbol{K}$. For this purpose, FEA is implemented using the BEM nodal locations over the *dx* x *dy* areas associated with the BEM meshing density. For each finite area, *dx* x *dy*, centered on each node of the 2D membrane surface, a uniform pressure force is applied, and the resulting displacement for each nodal location is calculated with FEA. Figure 58 shows an example FEA mesh with boxed region for

pressure application. Each FEA simulation associated produces displacement information over the entire membrane where $u^{i,j}$ is the displacement of node j when pressure is applied to node i. With all N FEA simulations, the displacement matrix is fully populated, and the stiffness matrix can be calculated by equation (25). Through this formulation, the $\boldsymbol{K}$ matrix is completely populated with information as to how each node affects all other nodes on the surface. Note that, with this approach, thin plate approximations are removed, realistic edge boundary conditions can be applied, and complex geometries can be evaluated for a CMUT as shown in Figure 57-right.

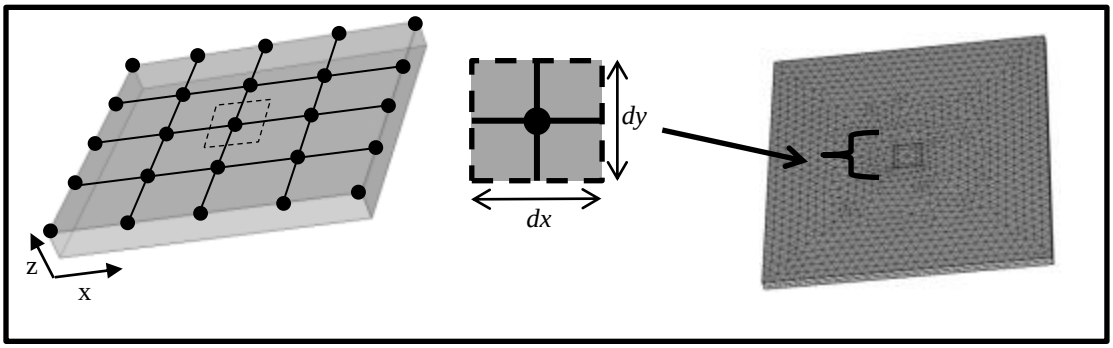


Figure 58. CMUT nodal spacing and a meshed membrane in COMSOL used for $\boldsymbol{K}$ matrix calculations.

$$\boldsymbol{K} = \begin{bmatrix} P_{app} & 0 & \cdots & 0 \\ 0 & P_{app} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & P_{app} \end{bmatrix} \begin{bmatrix} u^{1,1} & u^{2,1} & \cdots & u^{N,1} \\ u^{1,2} & u^{2,2} & \cdots & u^{N,2} \\ \vdots & \vdots & \ddots & \vdots \\ u^{1,N} & u^{2,N} & \cdots & u^{N,N} \end{bmatrix}^{-1} \tag{25}$$

Also, for a given geometry and mesh density, the FEA need only be performed once as it can be reused for an array of similar membranes. Membrane symmetry may also be exploited to reduce computation time. The resulting $\boldsymbol{K}$ matrix is directly combined with the BEM formulation for fluid loading to implement an efficient hybrid computation of linear CMUT dynamics. Simulations were performed in COMSOL using the Matlab interface with example code in APPENDIX D.

4.3.4. FEA K Matrix Validation

To validate the stiffness matrix calculations for harmonic simulations in vacuum to predict the high Q > 50, first mode resonance was calculated in COMSOL 4.2a and compared to both the numerical method with the stiffness matrix based on thin plate approximations and the hybrid FEA-numerical method. The bulk membrane material chosen for simulation, silicon nitride, as deposited by plasma enhanced chemical vapor deposition (PECVD) has been previously used for CMUT fabrication with properties listed in Table 10 [32, 101]. The FEA meshing was set to "Extra Fine" for all simulations. The square CMUT membrane thickness was fixed at 2 μm with electrode coverage dimensions were fixed to 75 % of the edge dimensions which were adjusted from 40 μm to 10 μm, aspect ratios 20 to 5. These dimensions were chosen to be consistent with CMUT membranes previous fabricated for ultrasonic imaging [32, 101]. For all cases the hybrid method and FEA simulation are in good agreement for all aspect ratios deviating by less than 1.5% for 2 μm nodal meshing in the BEM domain. Figure 59 shows a comparison of the hybrid method to finite difference approximation as a percent difference from full FEA analysis. The meshing for the FD simulations was below 0.5 μm based on convergence criteria of less than 5%. With the low aspect ratio of 5, the thin plate approximation deviates by 25% from FEA while the hybrid method deviates by less than 2%.

Table 10. Simulation material properties

Simulation Properties	**PECVD SiN**	**Al**
Young's Modulus, GPa	110	70
Poison's Ratio	0.22	0.35
Density, kg/m^3	2040	2700

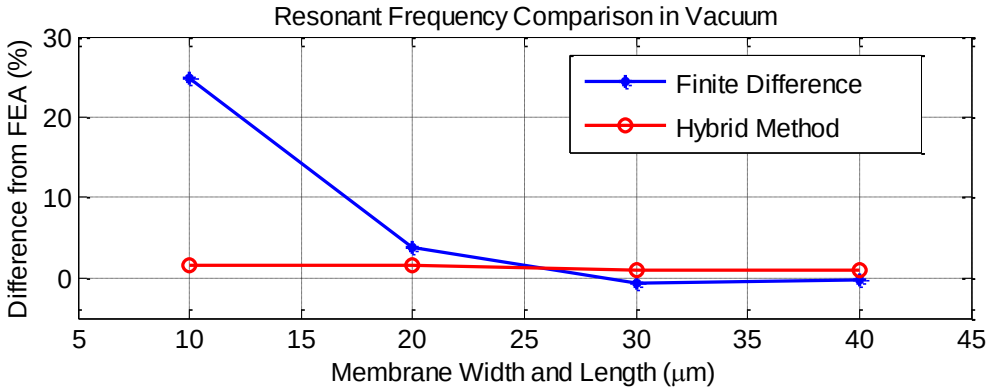


Figure 59. A comparison of a square membrane in vacuum. The finite difference and hybrid methods are compared to FEA.

To further validate the hybrid method, a single mass loaded membrane, as shown in Figure 60 with buried electrode was simulated in water with material properties listed in Table 10 and dimensions listed in Table 11. The frequency response using the hybrid method was compared to FEA utilizing symmetry in a quarter of a sphere with an outer matched layer to simulate an infinite fluidic space. For the single membrane case, meshing of the membrane and electrode was accomplished via the automatic meshing set to "Extra Fine" with the nodal meshing into the fluid set at a maximum growth rate of 1.08 and maximum element size of 18 μm. For the hybrid numerical method, the stiffness matrix was calculated using 1 μm x 1 μm meshing. For each node, the mass matrix was calculated based on the average thickness and known density of the materials in the 1 μm x 1 μm regions. Figure 61-top, shows the FEA results with 1 MHz resolution from 20 - 70 MHz, along with the hybrid method, 1 MHz resolution from 5 - 80 MHz, showing good agreement in center frequency and bandwidth with 0.2 MHz difference in center frequency. It can also be seen that the FEA above 45 MHz oscillates which is a known issues with insufficient fluid meshing. To expand upon the single membrane comparisons, the same membrane geometry was simulated using quarter symmetry to simulate a 2 x 2 array of complete membranes with 24 μm pitch. Because of the

limitations of the computer used to run the FEA simulation, the membrane meshing was reduced from Extra Fine to Fine with limited frequency range, 20 - 45 MHz at 1 MHz resolution. With all other simulation parameters the same, it can be seen, Figure 61-bottom, that the center frequency and bandwidth are in good agreement with a maximum 1.1 dB difference in the region where FEA is accurate. The effect of multiple membranes in close proximity is shown by the increased center frequency, 32 MHz to 37 MHz, and corresponding -3 dB fractional bandwidth reduction from 37% to 21%.

With the same mass-loaded membranes, the array was further increased to a 3 x 3 array configuration. Three active membrane configurations were chosen to further demonstrate the importance array simulation. Figure 62 shows the simulated frequency response for all membranes active, top, center column of 3 membranes active, and outer two columns active, bottom. It is important to note that all three simulated configurations produce distinct frequency response based solely on which membranes are active. This simulation would not be possible in FEA using symmetry boundary conditions.

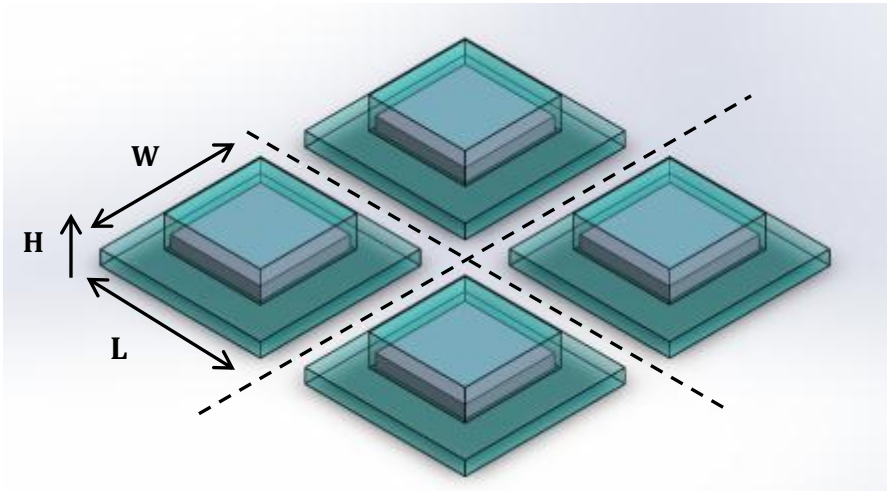


Figure 60. Mass loaded CMUTs with aluminum electrodes. Dashed lines indicate symmetry for the 2 x 2 array simulated using FEA.

Table 11. Mass loaded geometry dimensions

Geometry	L x W x H, μm	Material
Base Membrane	20 x 20 x 1	SiN
Top Mass	15 x 15 x 2	SiN
Buried Electrode	14 x 14 x 1	Al

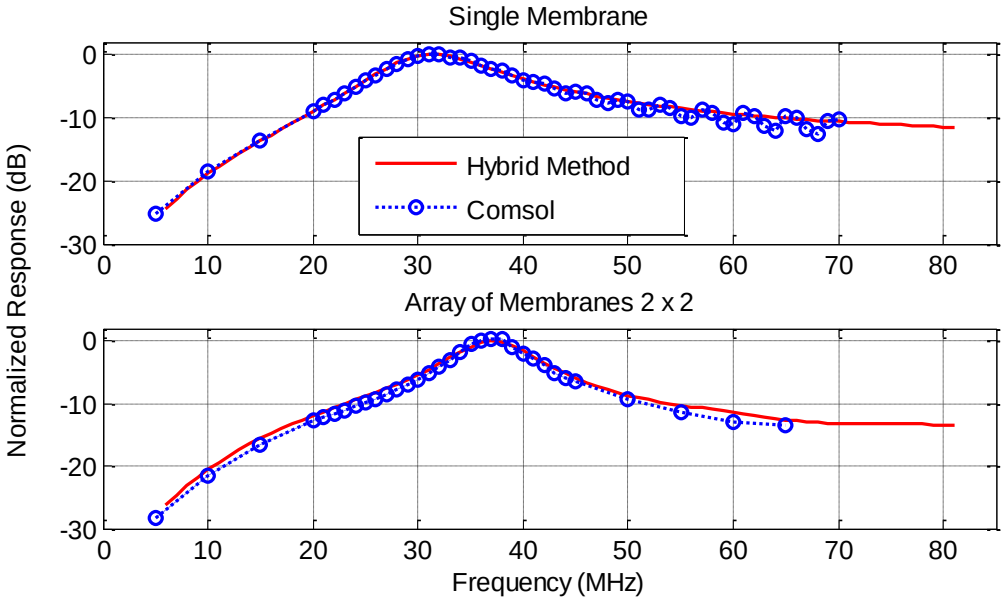


Figure 61. FEA simulation of a single mass-loaded membrane compared to simulation using the hybrid method (top). A 2 x2 array of mass-loaded membranes (bottom).

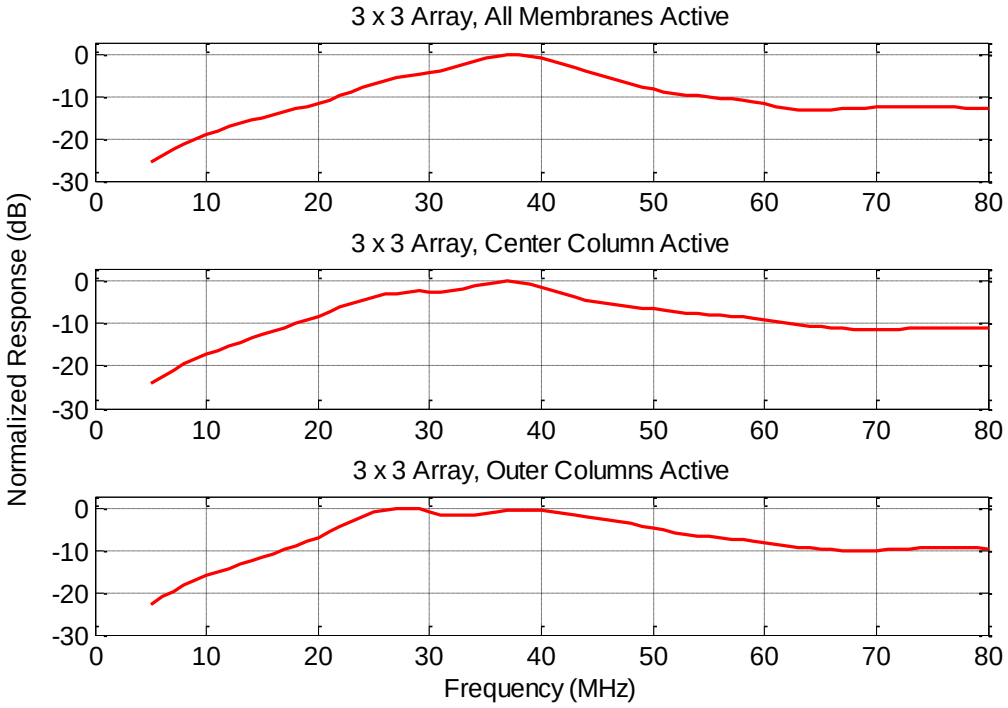


Figure 62. Simulations of a 3 x 3 matrix of mass-loaded membranes with all membranes active, top, center column active, middle, and outer two columns active bottom. All three cases show distinct frequency responses.

4.3.5. Computation Time Reduction

For comparison purposes, a computer with an Intel i5 processor running at 2.67 GHz and 4 GB of RAM was utilized. For FEA, the simulation required approximately 10 h for the single membrane and approximately 16 h for the 2 x 2 array of membranes. The stiffness matrix required approximately 30 minutes to compute. Once the stiffness matrix was calculated, the frequency analysis required less than a minute to for the single membrane and less than 2 additional minutes for the array. Simulations for the 3 x 3 array required less than 10 minutes with the pre-calculated stiffness matrix further demonstrating the computational effectiveness of the hybrid method. It should also be noted that the FEA analysis relied upon quarter symmetry resulting in all membranes being active which is not a limitation of the hybrid method.

The hybrid analysis presented has been shown to overcome the limitations of the thin plate approximation for modeling CMUT membranes, which have large variations in geometry. The results of the hybrid model match well to FEA simulations for both low aspect ratio and varied geometry membranes while significantly reducing overall computation time.

4.3.6. Large Signal Expansion

To improve upon the small signal analysis capabilities of the aforementioned FD/hybrid BEM, a transient model for larger signal analysis of CMUT arrays with arbitrary configurations was concurrently developed by Mr. Sarp Satir. This model describes every electrode in the array as a lumped system resulting in a multi-input multi-output (MIMO) model which is based on the separation of the linear acoustic problem and the nonlinear electrostatic force. This model utilizes the linear acoustic response as calculated through the BEM as described previously.

The larger signal model developed can be divided into three main sections as described by the three general blocks of Figure 63 with voltage input and pressure output. In block A, the drive signals are the voltages applied to each of the CMUT electrodes as a function of time. Figure 63 also shows an example array with four CMUT transducers where each of the top electrodes, which covers a portion of the transducer membrane, are divided into two distinct electrostatic patches and as such, the drive signal can be applied independently to each patch. Based on static loading conditions, the center patch is set to be over the region of maximum deflection, while the outer doughnut patch undergoes deflection one half of the maximum. In this figure, the inner two membranes are active Tx elements with a DC bias and an AC signal. The outer two CMUTs in this figure are subject to a DC bias only, as in the case of a non-actuated neighbor element in the Rx mode of operation.

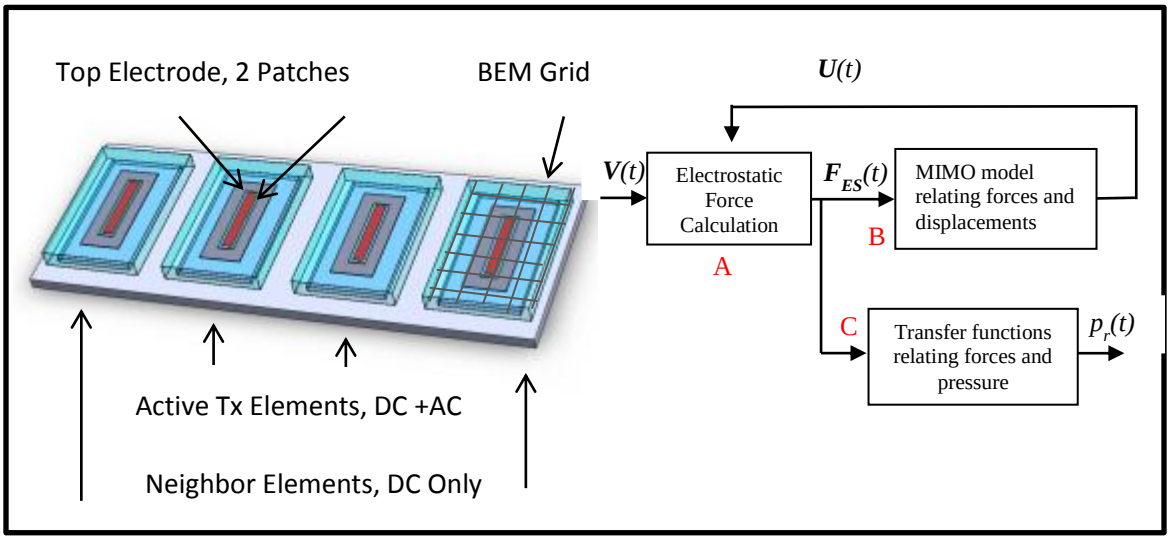


Figure 63. An array of four CMUT membranes each with two electrostatic patches where the center two CMUTs are actuated with both a DC and AC signal for the Tx mode of operation. The outer two CMUTs are subject to only a DC bias as in the Rx mode. The right most CMUT is shown with an example BEM grid. A block diagram describing the transient model with arbitrary voltage input and pressure output.

The voltage input of block A together with the average electrode displacement feedback is used to calculate the total electrostatic force for each electrode patch in the array. This block takes care of sources of nonlinearity in large signal CMUT modeling, within the constraint that the mechanical behavior is assumed to be linear as the vacuum gaps are much smaller than the lateral dimensions and the induced strain will be small even under full deflection [102]. The sources of the nonlinearity in CMUT operation are the inverse gap square dependence of the electrostatic force acting on the electrodes as explored in Satir *et al.* [103], and the change in force distribution on the electrodes as the CMUT membrane deflects [94]. Therefore block A models the electrostatic force generation for each electrode patch in the array.

Block B describes the vibroacoustic behavior of the array as a linear MIMO system relating the total electrostatic forces acting on each electrode patch and their respective average displacements. This block is derived from the linear acoustic analysis of the CMUT array using the boundary element method presented in Meynier *et al.* [98].

The rightmost CMUT membrane in Figure 63 shows a representative surface grid used for BEM calculation where each intersection is a nodal location with grid endpoints fixed nodes for the ridged edge boundary condition. Using the BEM, nodal displacements are calculated as a function of frequency for multiple cases where each electrode patch is excited individually with unit pressure applied to the electrodes. As the mechanical dynamics of the CMUT array are linear, the superposition of the individual solutions can be used for the solution of arbitrary excitation configurations. To reduce the order of the distributed model, the nodal frequency response data is lumped into transfer functions from total forces acting on electrodes to the average displacement of each electrode patch. A MIMO state space model is then fit to the calculated frequency response data. This linear MIMO model block couples the dynamics of individual electrode patches through acoustic interaction, and therefore it models the linear mechanical behavior of the array, including crosstalk and higher order membrane shapes.

Electrostatic force (block A) and membrane displacement (block B) calculations completely define the electromechanical behavior of the modeled CMUT array. The solution of the transient model is then used to calculate the time domain pressure signal at an arbitrary point of interest. As the linear acoustic problem is solved via BEM, a transfer function is calculated which relates the total force acting on each electrode patch and the pressure at the point of interest. Block C can be considered as a multi-input single-output (MISO) system where the block inputs are the total electrostatic forces acting on array electrode patches and the output is the pressure at the desired point in the immersion fluid.

Single or multiple membrane geometries, each with a separate **K** matrix, can be arranged into an array with subsequent analysis using the BEM. With the MIMO and MISO blocks derived from these calculations, SIMULINK is used with voltage signals to compute the output pressure [104]. To demonstrate the capability of this model CMUT membranes, 2 μm x 40 μm x 40 μm with a 50 μm pitch were modeled in a 2 x 2 array

configuration for large signal transient analysis. The simulation is set up such that all 4 array elements are excited with the same drive signal and the pressure at the array surface in the middle of the array is calculated both with COMSOL and the model. The actuation signal is a 20 ns long, 70 V pulse without DC bias which results in a full gap membrane swing. The time domain pressure signals and their spectrums for both FEA and the SIMULINK model are presented in Figure 64. The two are in excellent agreement, with 1 dB max difference up to 30 MHz for the 10 MHz CMUT, which demonstrates the larger signal simulation capability.

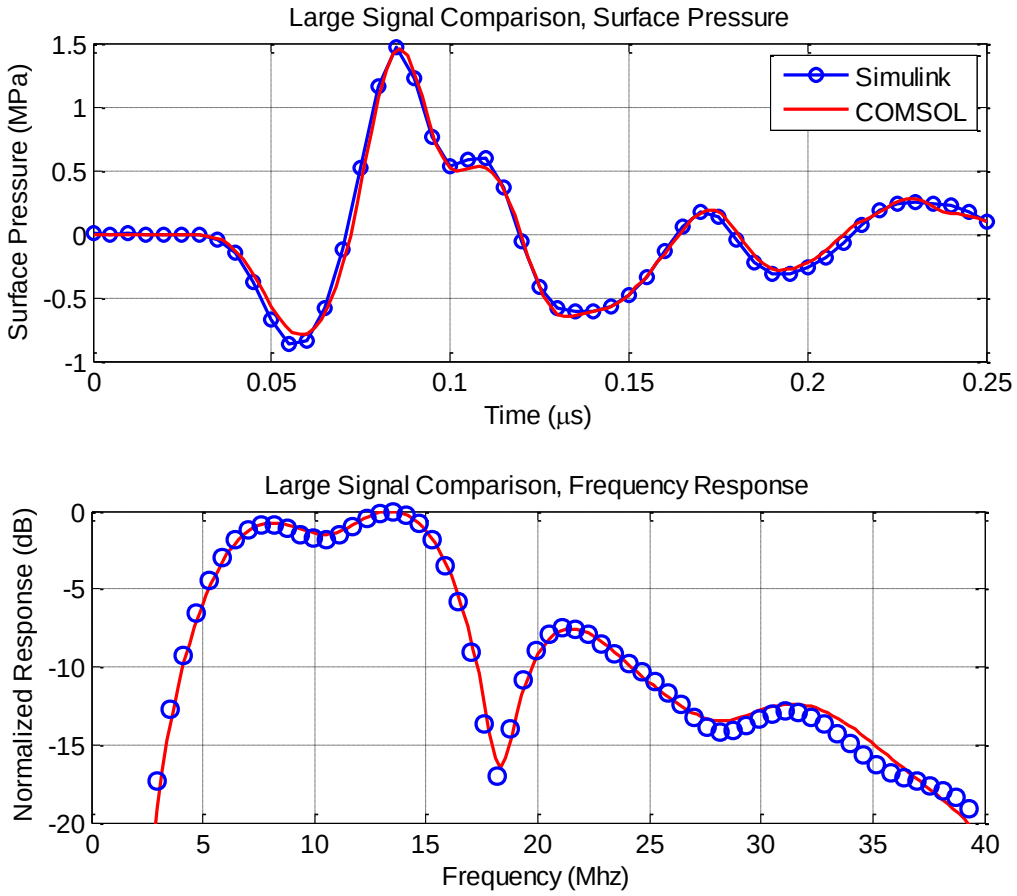


Figure 64. Simulated surface pressure and corresponding frequency response, of a 2 x 2 array of CMUT membranes for a high amplitude, short pulse resulting in full gap swing.

4.3.7. CMUT and Array Optimization Algorithm

As the model is generated in discrete steps, optimization or modification can be more or less computationally expensive depending upon the parameter modified such as mass loading, array spacing, and applied signal as described by the feedback. Figure 65 describes the general process flow of the model along with main computational methods and blocks. For an initial set of parameters, and based on the individual membrane geometry, either the finite difference method or the hybrid-FEA method can be used to generate the stiffness matrix. Single or multiple membrane geometries, each with a separate $\boldsymbol{K}$ matrix, can be arranged into an array with subsequent analysis using the BEM. With the MIMO and MISO blocks derived from these calculations, SIMULINK is used with voltage actuation signals to compute the output pressure at any arbitrary point in space.

To illustrate the optimization flow, the gap thickness can be examined. In general, the gap has minimal influence on the frequency response; therefore that parameter can be iterated quickly without modifying the MIMO and MISO blocks. This doesn't change the array geometry and would not normally require recalculation of the $\boldsymbol{K}$ matrix. However, if the gap were to be adjusted significantly, there is a possibility that it could affect the stiffness, and the $\boldsymbol{K}$ matrix would then require recalculation. Since iterative optimization is an important feature, overall this model is well suited for rapid and accurate design of CMUT arrays.

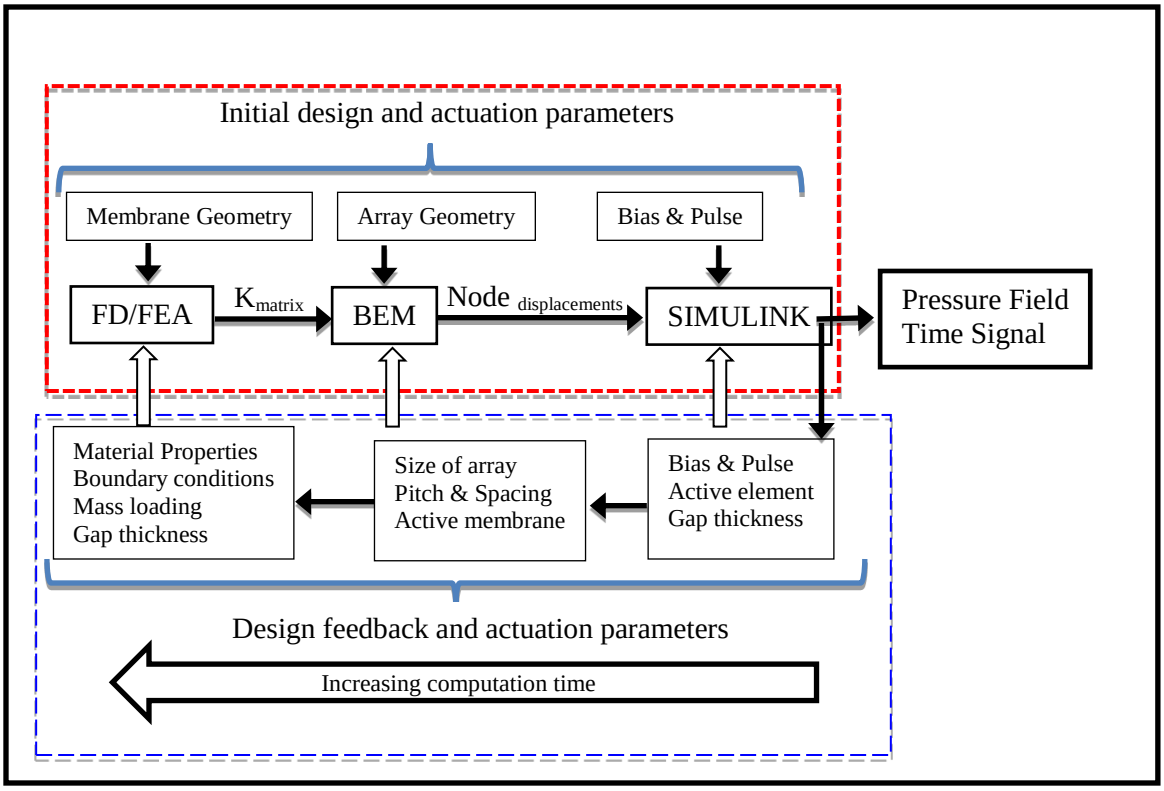


Figure 65. A block diagram describing the modeling process and design feedback parameters that can be modified at each stage of the modeling

4.4. Summary

A key benefit of the modeling and simulation approach presented in this chapter is its generality in terms of individual CMUT geometry, CMUT placement in an array, and large signal actuation capability. With this approach, it is possible to investigate the interaction of arrays of CMUTs with arbitrary geometry and actuation for expedited iterative design optimization.

It was shown that the limitations associated with the thin plate can be removed by generating an alternative stiffness matrix through the use of FEA. As a test case, mass loaded CMUT geometries were compared using the hybrid-BEM and FEA, showing excellent agreement in center frequency and bandwidth. As the model is based on a 2D

surface mesh, increasing the array size has been shown to be computationally less expensive than using 3D transient FEA. It is important to note that for a given CMUT geometry, the stiffness matrix need only be generated once while the array placement can be modified for optimization purposes.

The larger signal expansion was also summarized which uses arbitrary voltage drive signals as the input with pressure in the field as the output. Since, the SIMULINK model blocks are pre-calculated for a given array geometry, the transient SIMULINK model was shown to takes less than a second to run [104]. This is a significant advantage over FEM, as the model can be simulated for different drive signals for individual array elements iteratively in a significantly reduced computation time.

CHAPTER 5

FORWARD-LOOKING DUAL-RING ARRAY

As discussed previously, the ring type doughnut shaped transducer array has been proposed to be fit on the front tip of the catheter to allow for forward-looking looking imaging capabilities. For FL-IVUS applications, the element sizes need to be small in both the radial and lateral dimensions to avoid grating lobes, and in the ring configuration, the center is free to allow for passage of a guide wire.

With these considerations in mind, CMUTs have been found especially suitable for catheter bussed FL imaging applications due to the flexibility of different array structures at this small scale. With the design space improvement based on the fabrication with a copper sacrificial layer, and the ability to perform large signal transmit array simulations, the dual-ring array is investigated for optimized 3D volumetric imaging when integrated with the custom CMOS electronics.

The following section describes the develop of the dual-ring CMUT arrays on the order of 1 - 2 mm in diameter for FL-IVUS applications in the frequency range of 10 - 20 MHz integrated with CMOS electronics capable of real time 3D volumetric imaging. In particular, of primary interest, associated with the small CMUT elements of the DRA, is the increase in transmit pressure and receive sensitivity while reducing the maximum DC bias necessary for operation.

5.1. Physical Depiction of an Ideal FL-DRA Catheter Implementation

The catheter integration design objective of the forward-looking ring array is shown in Figure 66. In this depiction the CMUT array is monolithically integrated with CMOS electronics utilizing backside flex-circuit technology as made possible through

TSV electrical connection to the front side CMOS. Also shown is the central guide wire passing through the center of the CMOS substrate, and a backing layer included for damping of substrate ringing which can adversely affect the frequency response of the transducer array.

The integration with the electronics is not only used for improved performance in terms of SNR from reduced parasitic capacitances as previously discussed in CHAPTER 3, but also to reduce the number of cables necessary for power, bias, and Rx signal etc. For catheters on the order of 1 mm in diameter, the available space to pass power and signal cables is limited, 10 - 20, and with the desire for both side-looking and forward-looking capabilities this becomes an important design limitation. This integration scheme, in part, drives the development of the forward-looking dual ring array design.

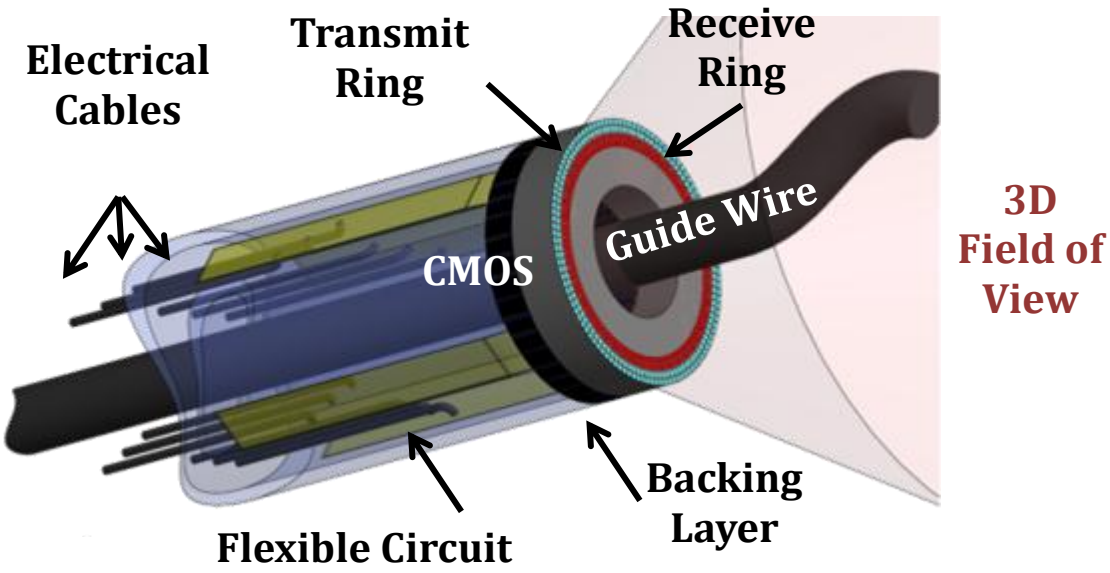


Figure 66. A depiction of a dual-ring CMUT array with backside flexible circuit interconnect technology. The doughnut CMOS with monolithically integrated CMUTs allows for the passage of the central guide wire.

5.2. FL-DRA Specifications

For IVUS imaging, the array diameters under investigation are on the order of 1-2 mm in diameter with desired imaging capabilities 1 mm to 1 cm into the tissue for CTO evaluation. With these diameters, center frequencies chosen were set to be 10 MHz and 20 MHz with associated parameters in Table 12. The axial resolution is approximated using the speed of sound, c = 1500 m/s, and bandwidth, BW, set to 100% FBW, equation (26). The lateral resolution is approximated using the focal length, *f*, diameter of array, *D*, and the wavelength based on the center frequency, λ, equation (27).

$$Axial\ Resolution \sim \frac{c}{2 \cdot BW} \tag{26}$$

$$Laterial\ Resolution \sim F\# \cdot \lambda = \frac{f}{D} \cdot \lambda \tag{27}$$

Table 12. FL-DRA parameters

Diameter	**2 mm**	**1 mm**
Center Frequency	10 MHz	20 MHz
Wavelength	150 µm	75 µm
Axial Resolution	75 µm	38 µm
Lateral Resolution at 1 mm	75 µm	75 µm
Lateral Resolution at 1cm	750 µm	750 µm
Element size	75 µm	38 µm

Further requirements are based upon the two cases reshown in Figure 67 where the IVUS catheter approaches an occlusion, left, and when the catheter is passing through the occlusion, right. For real time volumetric imaging at 30 FPS, it is only possible to collect 2500 data sets based upon the two way acoustic propagation in tissue at an imaging depth of 1cm. To estimate the on axis transmit pressure required to image the interface for the 10MHz device, attenuation, reflection, and the number of Tx-Rx

combinations need to be accounted for. Material properties for blood and fatty tissue are listed in Table 13 [105]. Noise characterization from previous CMUT-CMOS integration of a FL-DRA element was found to be 3mPa/√Hz. With the specified element sizes from Table 12, it is possible to fabricate dual rings with 64 Tx and 56 Rx elements for a total of 3584 combinations. This exceeds the 2500 data set limitation for volumetric imaging, but with 4 multiplexed output lines, the equivalent data collections per image reduces to 896, well below the limit. Taking the aforementioned into account along with the desire to have an overall 30 dB SNR, the Rayleigh Integral equation

(28**)** was used to approximate the radiated pressure from square CMUT membranes. With a wavelength of 150 µm at 10MHz, the surface resolution, *dS*, for integration was set to 3.5 µm x 3.5 µm.

$$p(x,y,z,t) = \frac{jk\rho_0 c_0 u_0 e^{j\omega t}}{2\pi} \int_S \frac{e^{jkR}}{R} dS \tag{28}$$

Figure 68 shows that at 10 MHz for the first case, the transmit pressure would need to be 2 MPa whereas for the second case the pressure would need to be 3.6 MPa. This translates to a minimum average membrane displacement of 21 nm and 38 nm at 10 MHz, which is smaller than previously fabricated vacuum gaps for CMUT membranes.

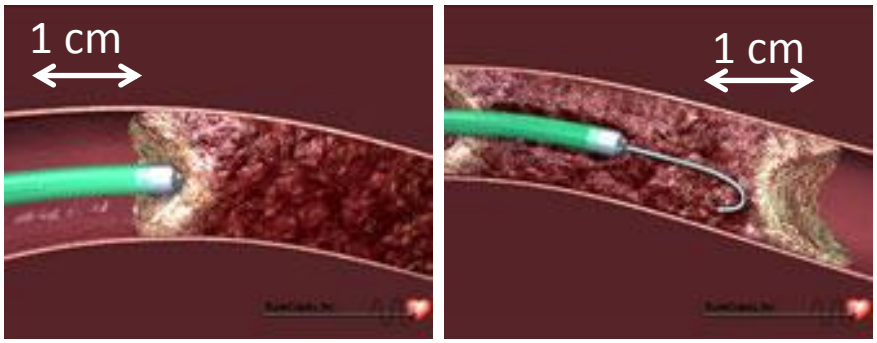


Figure 67. CTO imaging demonstrating the two imaging scenarios. The catheter approaches the CTO through the blood (left) and the catheter is pushing through the occlusion (right) [18].

Table 13. Tissue properties

Property	**Blood**	**Fat Tissue**
Attenuation db/MHz-cm	0.2	0.48
Acoustic Impedance Mrayl	1.51	1.38

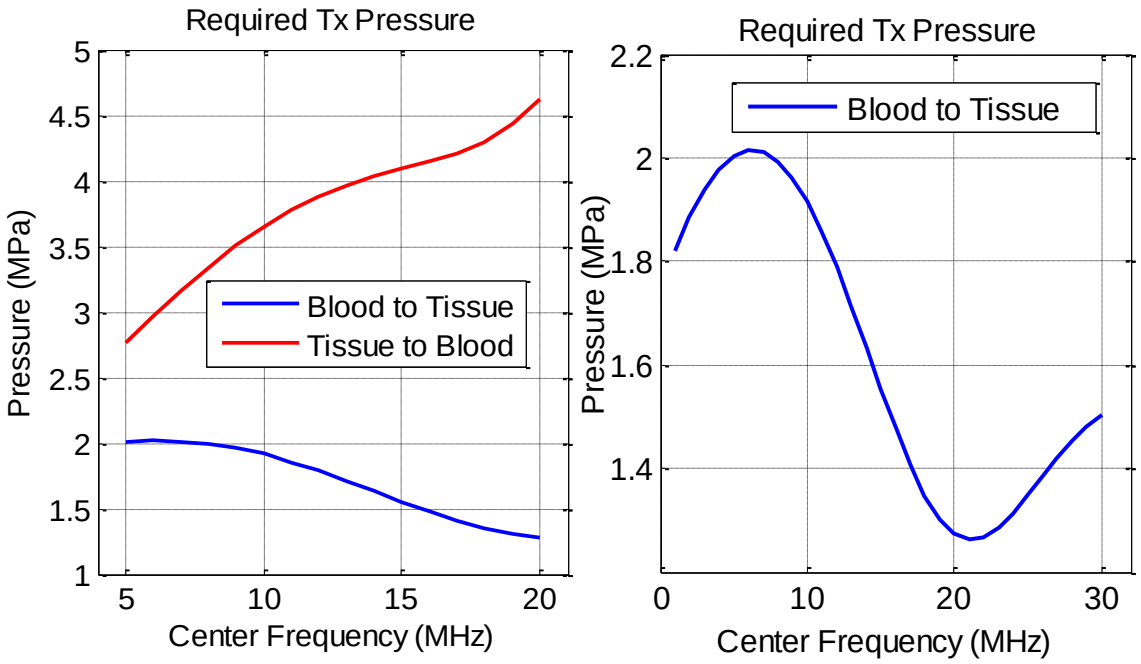


Figure 68. Required transmit pressure for a fixed bandwidth of 10 MHz at a distance of 1 cm as a function of the center frequency for 30 dB SNR.

5.3. Initial DRA Fabrication with External CMOS

As a proof of concept, a dual ring array with 24 Tx and 32 Rx elements was fabricated with an overall array diameter of 800 µm as shown in Figure 69. The trapezoidal membranes are approximately 35 µm x 35 µm with four membranes electrically connected to for each Tx/Rx element.

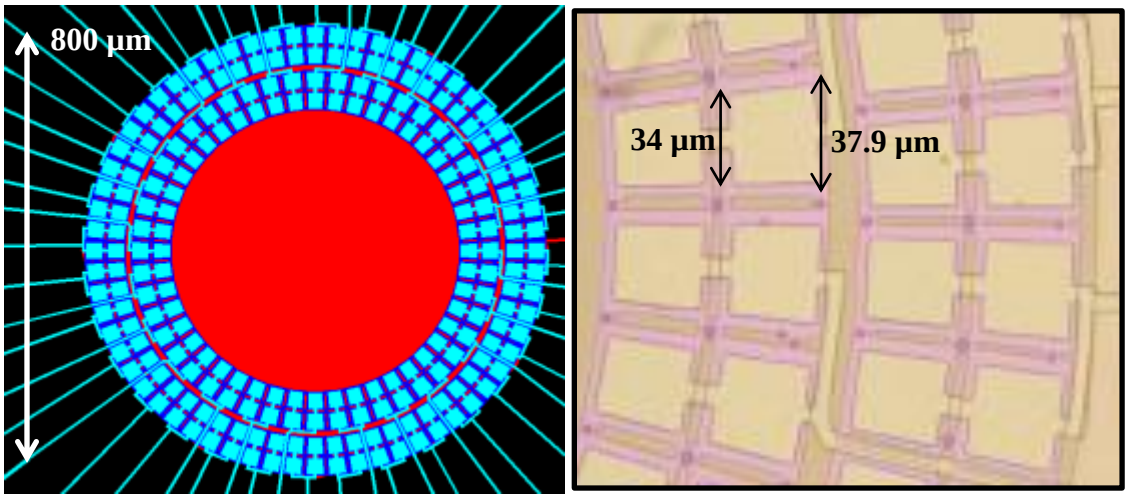


Figure 69. An AutoCAD drawing of a dual-ring array (left) and close up view of fabricated CMUT membranes (right).

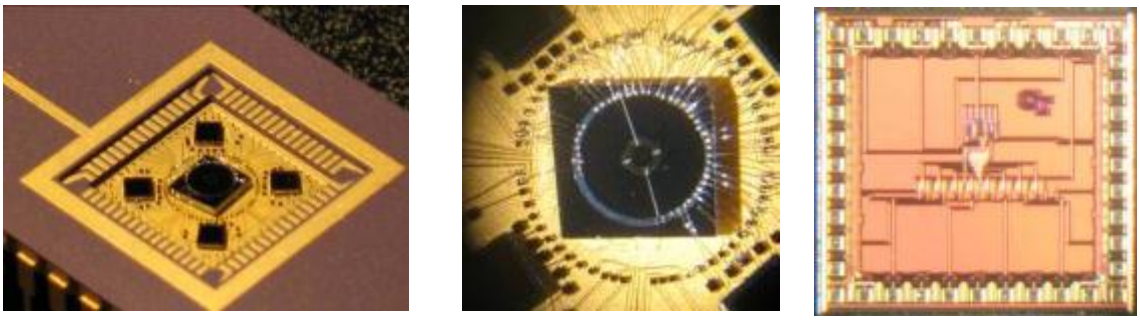
Custom ICs using a standard 0.5 µm CMOS process available through MOSIS were fabricated with an 8 x 1 multiplexer and buffer amplifier, Additionally, for each channel there is also 20k gain common source transimpedance amplifier (TIA) with a 50 MHz bandwidth with 5 pF input capacitance. The CMUT dual-ring array was integrated using a glass slide with custom fan out traces in a 64 pin ceramic DIP package. Around the CMUT array, 4 of the 1.5 mm^2 IC chips were integrated with the array via wire bonding to the Rx elements. A picture of electronic chips and CMUT array on the chip carrier is shown in Figure 70.

Pulse-echo experiments in oil were performed with A-scan data collected with 8 bits at 250 MS/s. The frequency response from a single Tx-Rx combination from the air oil interface at 6 mm was measured to have a center frequency of 11 MHz with a 95 % -

6 dB FBW. The SNR for this pulse-echo, using a DC bias of 170 V DC, ~ 90% of the collapse voltage, with a pulse of 160 V, was measured to be 24 dB with no averaging.

Imaging experiments were performed using a 3 wire target comprised of 250 µm aluminum wires as depicted in Figure 71-left. Data was collected from 19 Tx elements and 30 Rx elements as 5 Tx and 2 Rx channels were found to be non-functional. The reconstructed B-scan image was post-processed first using a digital filter, 1-30 MHz, over the raw RF data. The image was reconstructed through synthetic phased array RF beamforming with dynamic transmit and receive focusing along with envelope detection and logarithmic compression. The cross-sectional B-scan of the volumetric image with 20 dB dynamic range is shown Figure 71-right with the three wire targets clearly visible. The lateral resolution of the second and third targets are in agreement with theoretical values at 1.4 mm and 2.25 mm respectively. And, the axial resolution was measured to be 90 µm at the 3rd target in agreement with the theoretical value of 95 µm.

This implementation suffered in terms of SNR, limiting the dynamic range, from the parasitic capacitance associated with the wire bonding, bond pads, and associated connection lines from individual Rx elements to associated electronics. Therefore, to reduce the parasitic capacitance, there needs to be a more efficient method of CMUT-CMOS integration.



(a) (b) (c)

Figure 70. A dual-ring array in a 64 pin DIP surrounded by 4 custom IC chips (a), Close up view of the array and fan out chip (b). Magnified view of the custom IC chip (c).

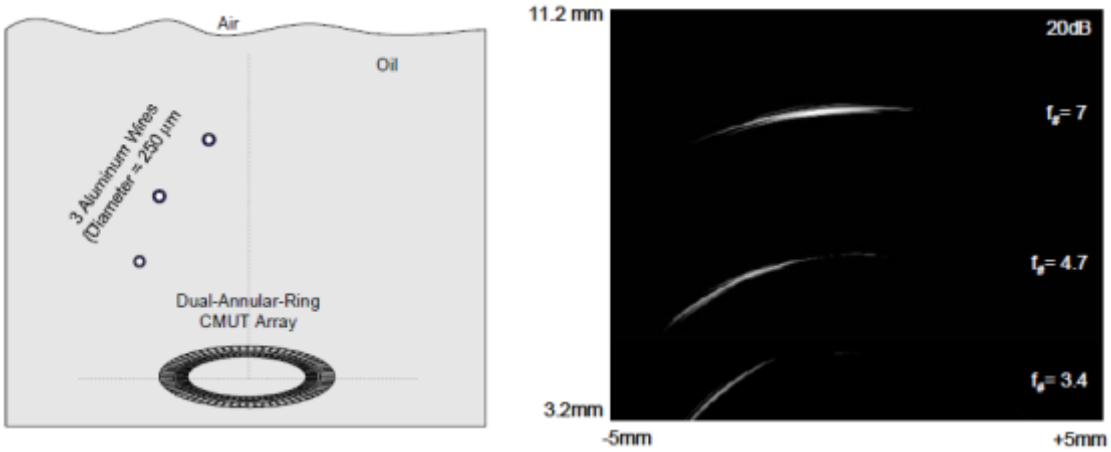


Figure 71. A depiction of a 3 wire target above the CMUT array (left) and cross-sectional image with 20 dB dynamic range (right).

5.4. DRA integration with CMOS

Based on the initial CMUT-CMOS results with wire bonding connections, custom CMOS substrates were fabricated and prepared as described in CHAPTER 3. Utilizing the developed interconnect fabrication processing, dual-ring CMUT arrays were successfully integrated with the CMOS electronics as the processing substrate as shown in shown in Figure 72. Dimensions for the layer thicknesses can be found in Table 14.

Of the two fabricated arrays shown, the 1.6 mm diameter dual-ring FL-IVUS array on the left consists of 64 receiver elements on the outer ring and 24 transmitters in the inner ring. The CMOS electronics contain one transimpedance amplifier (TIA) for each receiver, and four 16 x 1 multiplexers to route 4 receiver channels to the 4 output buffers. The electronics also include the digital decoding and control lines to collect data in a sequential manner from all transmit-receive combinations. In this version of the electronics the transmitters are driven by outside pulsers, but are integrated into the same chip in future versions. In the FL-IVUS array shown in Figure 72 (a), the electronics are

not located directly beneath the CMUTs as this was a proof of concept design. Concurrently, other FL-IVUS arrays with smaller dimensions were also fabricated with electronics directly below CMUT arrays without complication, Figure 72 (b). These devices have Tx elements connected to external bond pads for wire bonding and testing purposes.

For electrical and acoustical characterization of the CMUT on CMOS devices, the dual-ring FL-IVUS array shown in Figure 72-left was used since this array has larger area and larger number of array elements than the other FL-IVUS arrays concurrently fabricated. Each element consists of 4 rectangular CMUT membranes as seen in Figure 73. As shown, there are two different sized membranes that are electrically connected to form each element. The motivation behind this design was to maximize the active transducer area in the circular transducer region available, but the measured deflection of the membrane was found to be non-uniform under an applied bias with one side collapsing before the other. Smaller ring arrays for FL-IVUS with CMOS directly beneath CMUTs, Figure 72-right, have also been successfully tested as reported in G. Gurun *et al*. [106], but they were designed with fewer elements and were not as ideal to demonstrate volumetric imaging in the 10 MHz frequency range.

Due to the small membrane sizes and the number of Tx and Rx elements, it is possible for misalignment and process variation to decrease the uniformity across an array. As a figure of merit, we investigated the uniformity of a CMUT on CMOS array as well as an array with identical mask design fabricated on a standard silicon wafer for comparison. Additional experimental characterization included pulse echo experiments to evaluate the frequency response and finally initial volumetric images obtained by the FL-IVUS arrays.

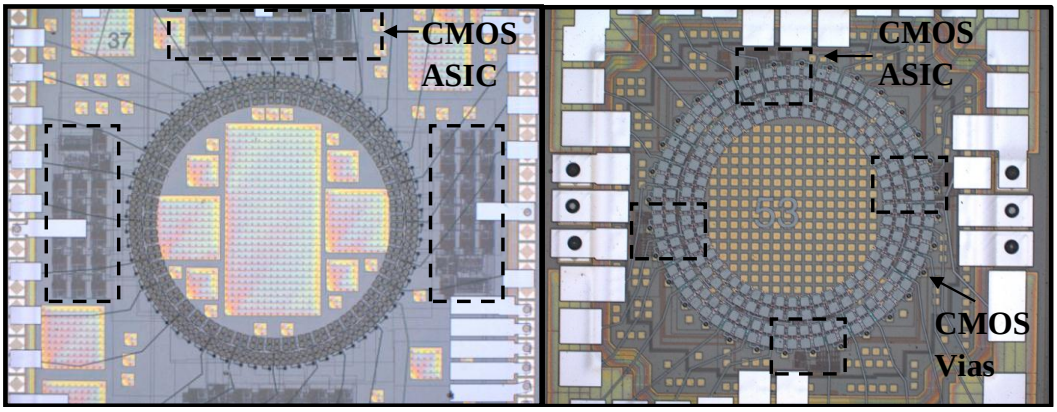


Figure 72.A fully fabricated CMUT on CMOS dual ring array with a 1.6 mm diameter array (left) and a 840 µm diameter array fabricated directly on top of the CMOS ASIC for FL-IVUS application (right).

Table 14. DRA Dimension for CMOS Integration

Layer	**Thickness**
SiO_2 planarization layer (before polishing)	3µm
Nitride layer for stiction improvement	0.2µm
Bottom and top electrode (Al / Cr)	0.12µm / 0.02µm
Nitride isolation layers (x2)	0.2µm
Chromium sacrificial layer	0.12µm
Nitride membrane thickness	1.5 – 3µm

5.4.1. Electrical Characterization

To characterize uniformity, a CMUT on CMOS FL-IVUS array was attached to a custom PCB with each of the 24 Tx CMUT elements wire bonded to a separate connection pad. An Agilent 8753ES network analyzer was used to measure the resonant frequency of the Tx elements at 70 V DC bias, well below the average collapse voltage of 96 V. It was not possible to directly test the Rx elements as they were only connected to the CMOS with no external testing connections. Testing in air is beneficial for uniformity characterization as the differences in resonances are more apparent with the higher quality factor as opposed to operation in a fluid medium. Because of the two

different membrane sizes within a CMUT element, two distinct resonance peaks are seen in the real part of the electrical impedance for a single Tx element as shown in Figure 73. For uniformity evaluation, impedance data were collected for each Tx element of the integrated CMUT on CMOS dual-ring array. The two distinct resonant peak frequencies for each Tx element across the 24 element array were measured with average resonances calculated as 13.7 MHz and 16.7 MHz. Numerical methods previously described in CHAPTER 4 were used to calculate the resonances in air of the two different sized membranes which were found to be 13.7 MHz and 16.7 MHz, in excellent agreement with measurements. The percent difference for each Tx element from the average resonance frequency does not exceed 6% implying acceptable uniformity from the fabrication. Most of this variation is likely due to the pre-process polishing and geometrical variation introduced while working with rectangular CMOS samples including the associated misalignment errors. Any non-uniformity in mechanical behavior due to the PECVD silicon nitride depositions should be minimal considering a given device occupies such a relatively small space on the wafer.

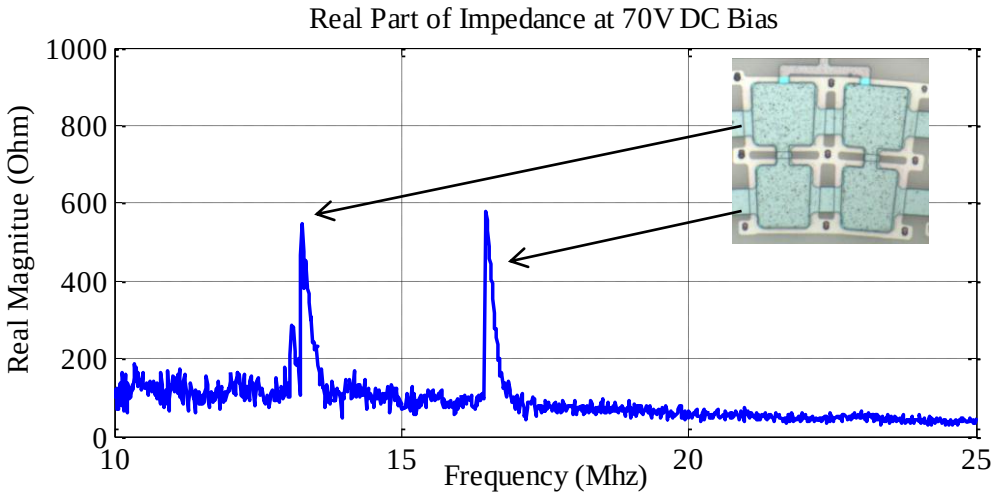


Figure 73.Agilent network analyzer measurement of real electrical impedance of fabricated CMUT on CMOS device showing 2 distinct resonant peaks due to membrane geometry differences. The peaks of this transmitter are measured at 13.3 MHz and 16.5 MHz

Similar data were obtained on CMUT arrays fabricated on a blank 100 mm silicon wafer using the CMUT-on-CMOS mask set. The resonances in air were measured to be on average 14.7 MHz and 17.1 MHz with the percent difference of each Tx element not exceeding 6%. The calculated resonances were 14.4 MHz and 17.2 MHz. The higher resonances are attributed to a slight increase in the membrane thickness, ~ 0.1 μm, which occurred during fabrication. This indicates that the CMUT on CMOS fabrication techniques implemented do not significantly affect uniformity of the CMUT operation from element to element. It should be noted that in a more recent CMUT on CMOS fabrication, with better alignment and reduced surface roughness from improved polishing and optimized metal depositions, uniformity was measured to be within 1.5% of the mean. This validates the assumption that PECVD nitride should exhibit minimal variation over the elements of a single device.

5.4.2. Acoustic Characterization

A completed 1.6 mm diameter CMUT on CMOS array, as shown in Figure 74, was wire bonded in a ceramic dual inline package (DIP, Spectrum CSB04075) and coated with 3 μm of Parylene C for electrical isolation in water. A 60 mm diameter, 15 mm tall polystyrene Petri dish was modified by milling a square opening in the base and then using epoxy to attach it to the ceramic DIP. This formed a cavity that could then be filled with water. External pulsers were connected to the Tx elements and the reflections from the air-water interface were received by Rx elements integrated with CMOS amplifiers and multiplexers. The DC bias for the Tx and Rx elements was set to 80 V, below the typical 95% of collapse voltage to avoid premature failure. A sample pulse echo signal from water-air interface at 5 mm is shown in Figure 75 with the corresponding frequency response which was filtered from 5-30 MHz during post processing. The center frequency of the array elements is around 15 MHz as desired.

There are significant spurious features in the frequency response including a dip at 7.5 MHz which is due to standing waves in the 550 μm thick silicon substrate [32, 107]. Acoustic crosstalk in the array resulting from the initial transmit pulse is also significant and corrupts the echo signal with features occurring before the target echo signal. This issue needs to be considered in the future designs with realistic donut shaped geometries, but for the purposes of acoustic characterization, the pulse echo response shows that the signal levels from single Tx-Rx pairs are strong and uniform. The standard deviation in the pulse echo peak to peak amplitudes was 1.3 dB, when the output for all active receiver elements were analyzed while using the same single transmitter. A simple geometric analysis of the Tx-Rx distance combinations shows that the difference in the distance varies by not more than 5% for an acceptance angle deviation less than 18 degrees from the vertical. Considering the small magnitude of these distance variations, the results from scanning all Rx channels demonstrate consistent and uniform acoustic response in the receiver side.

To have an estimate of the achievable pulse echo SNR, the receive bias was increased to 86 V, the water-air interface distance was set to 1 cm and the Tx element was driven with a 160 V_{pp} bipolar pulse centered at 15 MHz. The resultant SNR was calculated to be 41 dB using the RMS value of the received pulse divided by the RMS of the received signal without transmission, i.e. background CMOS electronic noise. The measurement bandwidth was 40 MHz, limited by the CMOS amplifiers. To evaluate the feasibility of imaging CTOs with this SNR level, we performed a calculation including diffraction losses and attenuation in blood at 15 MHz with 0.14 dB/MHz-cm frequency dependence. Considering an acoustical impedance of 1.68 MRayl for blood and reflection from a typical fat tissue with impedance of 1.33 MRayl, the SNR with 48 Tx elements and 64 Rx elements at a distance of 1 cm was calculated to be 34 dB SNR, suitable for detecting CTOs in front of a catheter [105]. Simulations and measurements on a noise

optimized TIA implemented in CMUT on CMOS shows that the SNR can be further improved by 15 dB [106].

To demonstrate that real time imaging data can be acquired with the FL-IVUS dual ring arrays, a custom data collection setup was constructed. It consisted of a custom high voltage pulser board to actuate the Tx elements, an FPGA board (Xilinx Virtex 5) for Tx element selection and multiplexing of the on-chip Rx elements, and a PC with 2 digitizer cards (UltraFast M3i.4142) for data collection and storage. The synthetic phased array method was used for image processing. The pulse-echo data for every Tx-Rx element pair were acquired for 20 μs (~ 1.5 cm imaging depth) without any time gain compensation or averaging. This results in a real time data acquisition rate of 130 frames/s considering 1536 Tx-Rx combinations and 4 parallel receive channels, which is suitable for FL-IVUS imaging. Delay and sum algorithms are then used to create a volumetric images using synthetic phased array image reconstruction. A more detailed description of the imaging setup with sample images can be found in [101, 108].

Figure 76 shows an imaged target comprised of four 150 μm diameter wires with a 15 dB dynamic range. The side, front, and isometric views are shown for the imaging volume of 2 mm x 2 mm x 6 mm starting 2 mm above the CMUT array. The bias for the Rx elements was set to 78 V and the Tx elements was biased to 70 V with a 140 V peak-to-peak bipolar pulse. Using the same setup, a tissue phantom using a corner section of the Three Vessel Training Ultrasound Phantom ATS VES-3 with embedded wire was imaged as shown in Figure 77. The front and isometric views are shown with a 15 dB dynamic range for a 4 mm x 4 mm x 9 mm volume starting 3 mm above the array. Data was collected at 130 frames/s and the phantom interface, top and bottom, as well as embedded wire can be seen in the image. This demonstrates the real-time imaging capabilities of the system for CTO applications but also indicates the need for improved performance with the limited on-chip pulse capability.

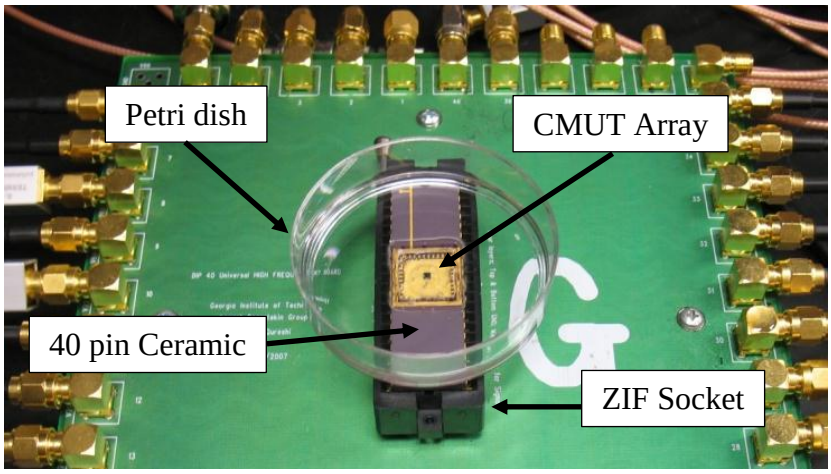


Figure 74. Experimental set up of wire-bonded 1.6 mm dual-ring CMUT array in a ceramic package combined with a modified Petri dish. The custom PCB board interfaces the ceramic package to external pulsers, FPGA board, high voltage bias lines, and signal output line to the digitizer card via SMA connections.

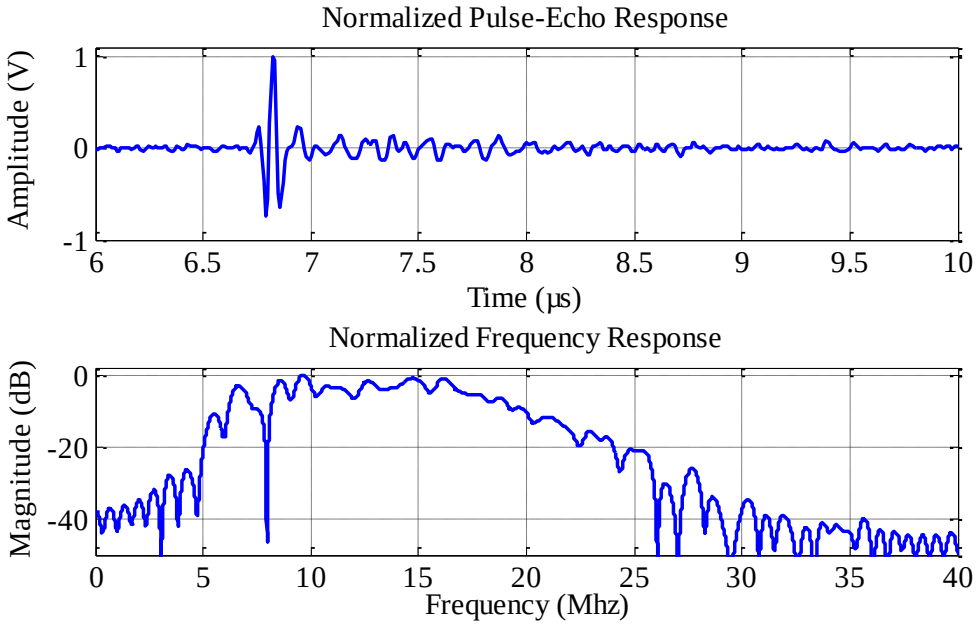


Figure 75. Pulse-echo response from a single pair of transmit and receive elements, showing functioning CMUT on CMOS array element, top. Frequency response from a dual ring array element in water shows that the CMUT on CMOS fabrication was successful and frequency response has enough bandwidth for imaging capabilities, bottom.

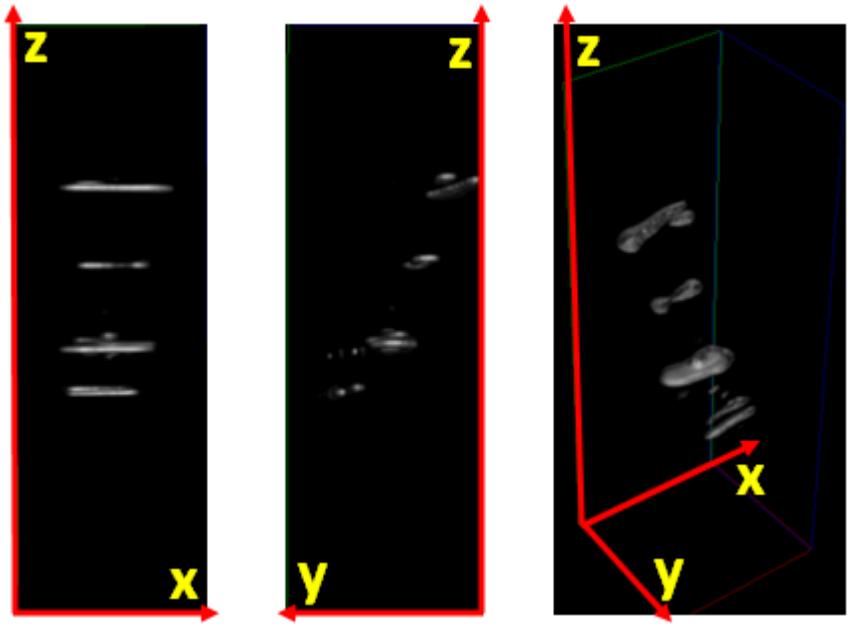


Figure 76. Side, front, and isometric views of a volume 2 mm x 2 mm x 6 mm of a 4 wire target, 15 dB dynamic range.

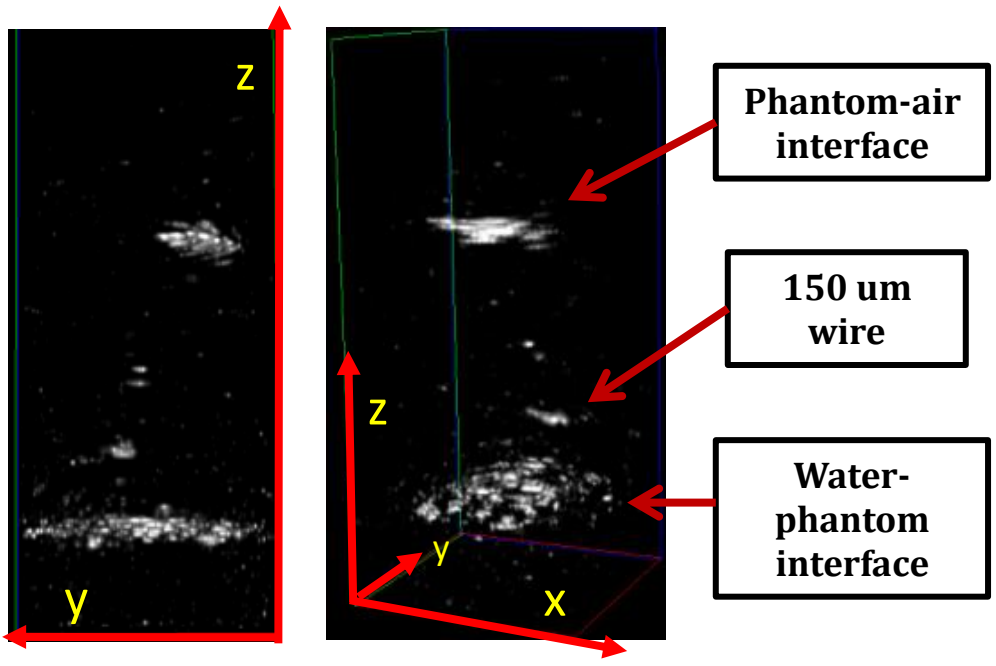


Figure 77. Tissue-like phantom with scattering and embedded wire target of a 4 mm x 4 mm x 9 mm volume, front and isometric view with 15 dB dynamic range.

5.5. CMUT-on-CMOS Imaging with Integrated Pulsers

Similar to the previous CMUT-on-CMOS integration, a second generation of custom CMOS electronics was fabricated with 56 Tx elements and 48 Rx elements with an overall diameter of 1.4 mm. Layer dimensions are the same as listed in Table 14 with square CMUT membranes 25 μm x 25 μm in a 2 x 2 configuration for each Tx-Rx element. The transition from the previous trapezoidal shape to a square CMUT membrane allowed for uniform deflection with applied bias. The second generation of electronics focused on CMOS layout optimization to allow for through silicon etching to form the circular doughnut shapes and passages for flex tape as previously described. Integrated pulser circuitry allowed for a 25 V pulse on top of a DC bias. For the fabricated devices, the collapse voltage was measured to be 160 V with a 21 MHz center frequency and 50 % fractional bandwidth. From a sample A-scan, the SNR was found to 20 dB as primarily limited by the 25 V pulse limitation which was not an issue with the external pulser circuitry previously implemented.

A four wire target immersed in oil was imaged and a 3D volume was reconstructed with a cross section shown in Figure 78. The lateral resolution was measured to be 251 μm from the second wire target, and axial resolution 92 μm. Additionally, to demonstrate the imaging capabilities of the CMUT-on-CMOS array, a chicken heart was suspended ~ 2.5 mm above the array as shown in Figure 79. The 3D volumetric image utilizing GE Microview software is shown in Figure 80 with a 40 dB dynamic range.

With the CMUT-on-CMOS array shown to be functional and capable of generating real-time 3D images while meeting the cable count limitation, 13 connections, the focus of the DRA development becomes improved SNR through optimized Tx-Rx fabrication as made possible through the fabrication optimization.

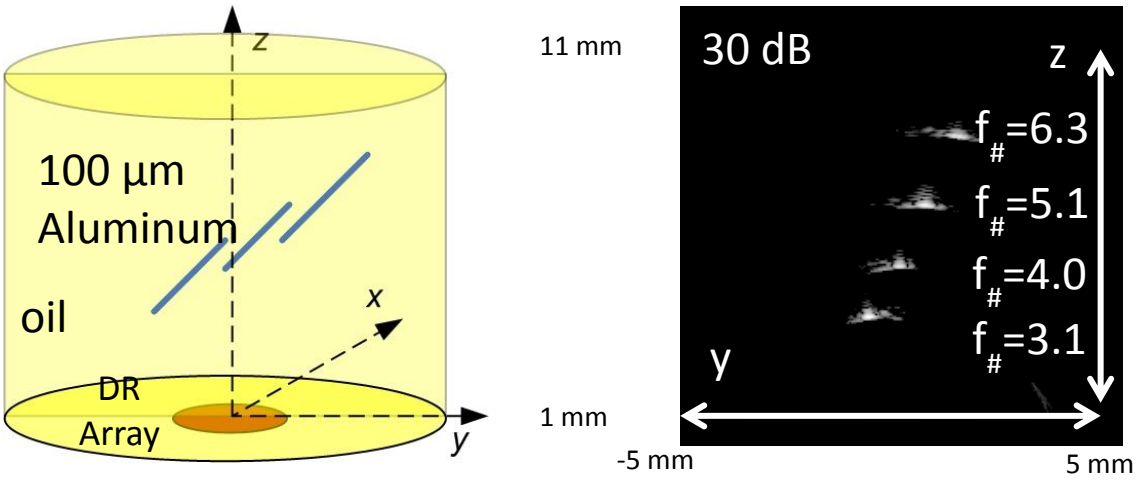


Figure 78. A depiction of a wire target in oil (left) and cross-section of a reconstructed volume with 30 dB SNR (right).

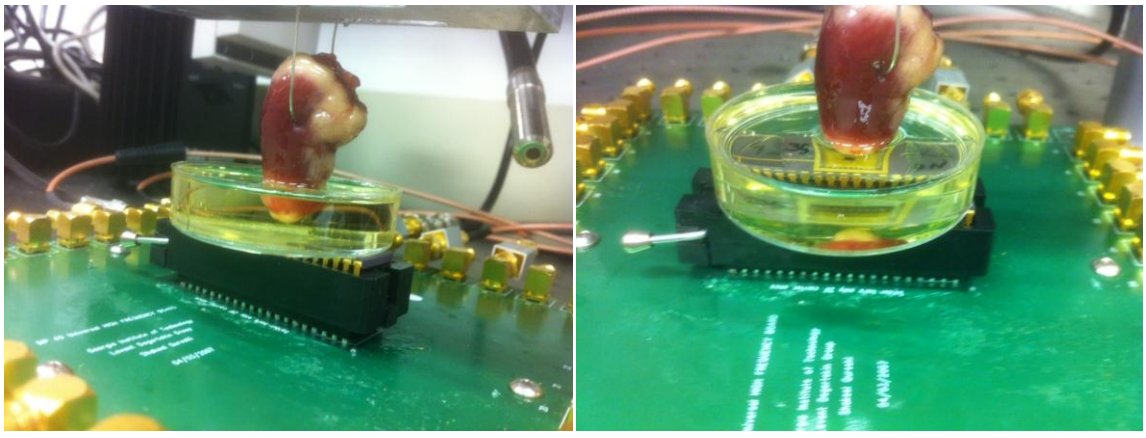


Figure 79. A chicken heart suspended 2.5 mm above a CMUT-on-CMOS array in oil.

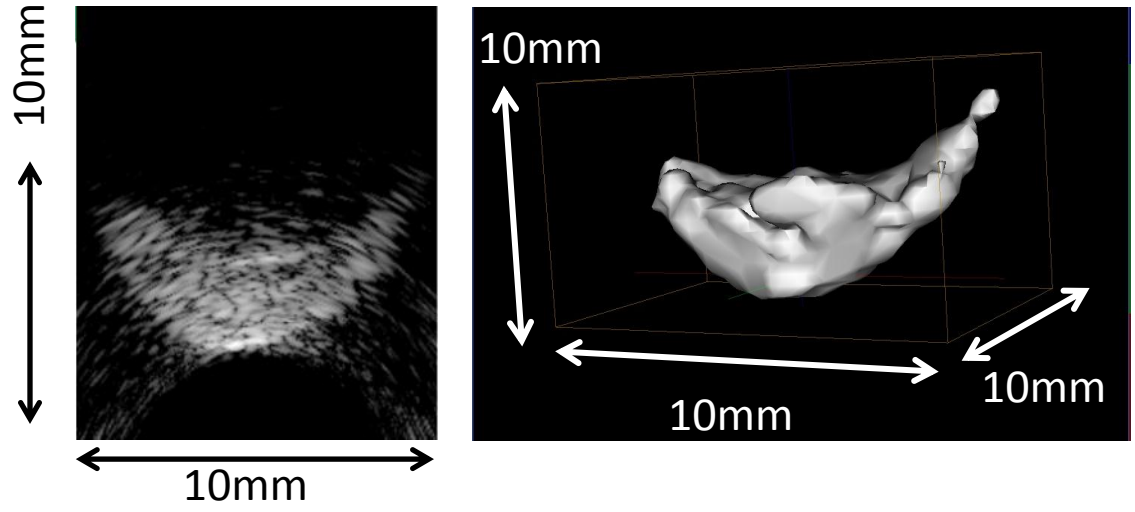


Figure 80. A cross-sectional view and isometric 3D image of a chicken heart using GE Microview with a 40 dB dynamic range.

5.6. Fabrication Optimization of DRA Elements

The use of a copper sacrificial layer and reduction of isolation nitride is primarily driven by the desire to optimize dual-ring array elements for improved SNR and lower operational voltages. As mentioned previously, in the Rx mode of operation SNR improvement is driven through gap reduction to increase the initial capacitance. In the Tx mode of operation, the improvement in SNR is derived from an increase in the Tx pressure which is linked to pulse and bias capability of the electronics used for integration. In general, the ability to reduce the operational voltage is important for ease of integration with electronics and to prevent dielectric breakdown on the cables passed through the body.

Test arrays of CMUT membranes 35 μm x 35μm for DRA application were configured in a 4 x 4 array with 45 μm pitch as shown in Figure 85-top. All membranes were electrically linked together with a common bottom electrode and 25 μm x 25μm top electrodes. Bond pads for testing purposes were fabricated with connection lines 10 μm

x 350 µm. For comparison purposes, two initial sets of devices were fabricated, one with a copper sacrificial layer and another with the chromium sacrificial layer. Measured layer thickness and measured collapse voltages are listed in Table 15. The membrane thickness which determines the resonant frequency was fabricated to be 2.2 µm for all cases. The collapse voltage was measured on a network analyzer, Agilent 8753ES.

Table 15. Layers and Collapse Voltages for DRA Test Arrays

Sacrificial Material	**Bottom Electrode**	**Sacrificial Thickness**	**Electrical Isolation**	**Top Electrode**	**$V_{collapse}$**	**Tx35/ Tx25**
Cr	Cr 30 nm	100 nm	244 nm	Cr 100 nm	88 V	1.3
Cu1	Cr 30 nm	65 nm	119 nm	AlSi 70 nm	45 V	0.94
Cu2	Cr 60 nm	70 nm	124 nm	AlSi 140nm	55 V	1.45

For the initial Rx testing, a 15 MHz Valpey Fisher piezoelectric transducer, part number IS1502HR, was placed 1.1 cm from the test arrays in vegetable oil. The bias was increased up to the collapse voltage and the received signal was amplified, 20 dB gain, and recorded on a Tektronix TDS 5054 oscilloscope. As predicted, the maximum sensitivity occurred when the CMUT array was biased close to the measured collapse. Table 16 lists the received signal for the bias conditions 50%, 80%, and 95% of the collapse voltage. For the bias condition 95% of the collapse voltage, the chromium fabrication measured Rx signal was 4.2 mV with an 80 V bias, and for the copper fabrication with 65 nm gap, the Rx signal was 6.3 mV with a 42 V bias. This experimental characterization is in agreement with theory in that the reduction in gap and isolation allows for greater Rx sensitivity with a reduced DC bias.

Table 16. Receive Sensitivity at 15 MHz for DRA Test Arrays

Sacrificial Material	**Sacrificial Thickness**	**$V_{collapse}$**	**0.5 x V_c (mV)**	**0.8 x V_c (mV)**	**0.95 x V_c (mV)**
Cr	100 nm	88 V	1.5 @ 43V	3.1 @ 68V	4.2 @ 80V
Cu1	65 nm	45 V	1.7 @ 23V	3.6 @ 36V	6.3 @ 42V

Tx measurements using an ONDA GL-0085 hydrophone, in oil were performed with a positive 25 V, 20 ns pulse with a negative bias set to ~ 90% of the collapse voltage. The pulse and bias were set to match the previously fabricated CMOS on chip pulser capability, 25 V peak, and bias configuration. The Tx pressure at 2.2 mm in vegetable oil was measured to be 22 kPa for the chrome sacrificial layer and 56 kPa for the lower voltage copper device. The 2.5x increase in Tx pressure indicates that the CMUT-on-CMOS DRA benefits from the reduced gap and isolation combination.

Utilizing the same hydrophone setup, the 20 ns pulse was varied from 15 V to 80 V and the DC bias was varied over the operational range of the CMUT. Figure 81 shows the received peak to peak pressure from the hydrophone for the CMUT with chromium fabrication, 100 nm. It can be observed that the maximum pressure occurs when the DC bias and pulse are the same polarity when the device is biased close to collapse with a high voltage pulse pulling it towards the bottom electrode.

Figure 82 shows the received pressure for the CMUT with 70 nm gap from the copper fabrication. Similar trends to the chromium fabrication can be observed and comparable pressures are generated but with approximately 50% of the DC bias applied for the chromium CMUT. The maximum pressure is observed to be, for both CMUT's, when a positive pulse is applied with a positive DC bias, with the peak applied voltage greater than the measured collapse. Therefore, simulations were performed using the SIMULINK model previously described to evaluate at which conditions the membrane completely deflects.

Figure 83 and Figure 84 show simulated results including attenuation in vegetable oil with a 20 ns Gaussian pulse under similar DC bias conditions. The SIMULINK implementation was not configured to deal with situations where the CMUT membrane touches the bottom substrate and as such would return a zero pressure condition. The trends in the simulated data match well with the experimental data, and it can be observed that the maximum pressure occurs with the 80 V pulse and positive DC bias. The

maximum simulated pressure was found to be 170 kPa and 230 kPa for the two cases respectively. Simulation and experimental characterization did not explore pulse width adjustment which may further improve the Tx pressure.

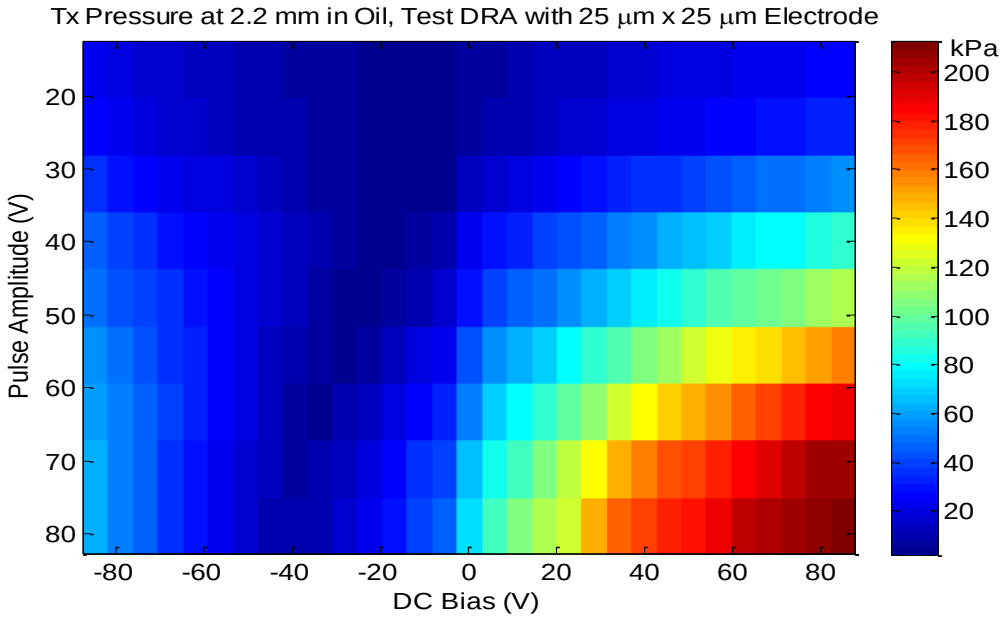


Figure 81. Transmit pressure for the chromium CMUT with 100 nm gap.

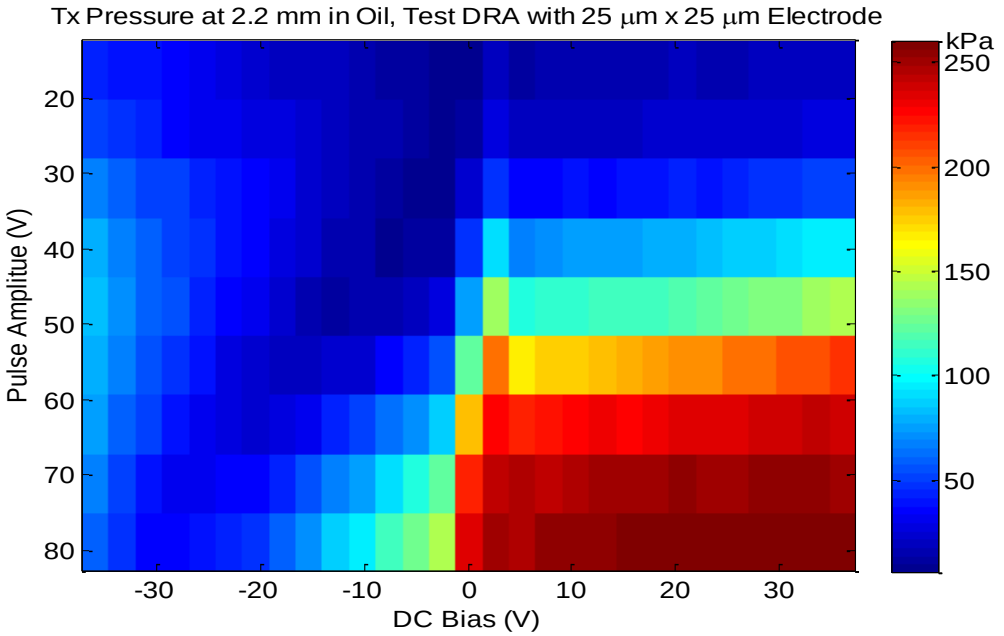


Figure 82. Transmit pressure for the copper CMUT with 70 nm gap.

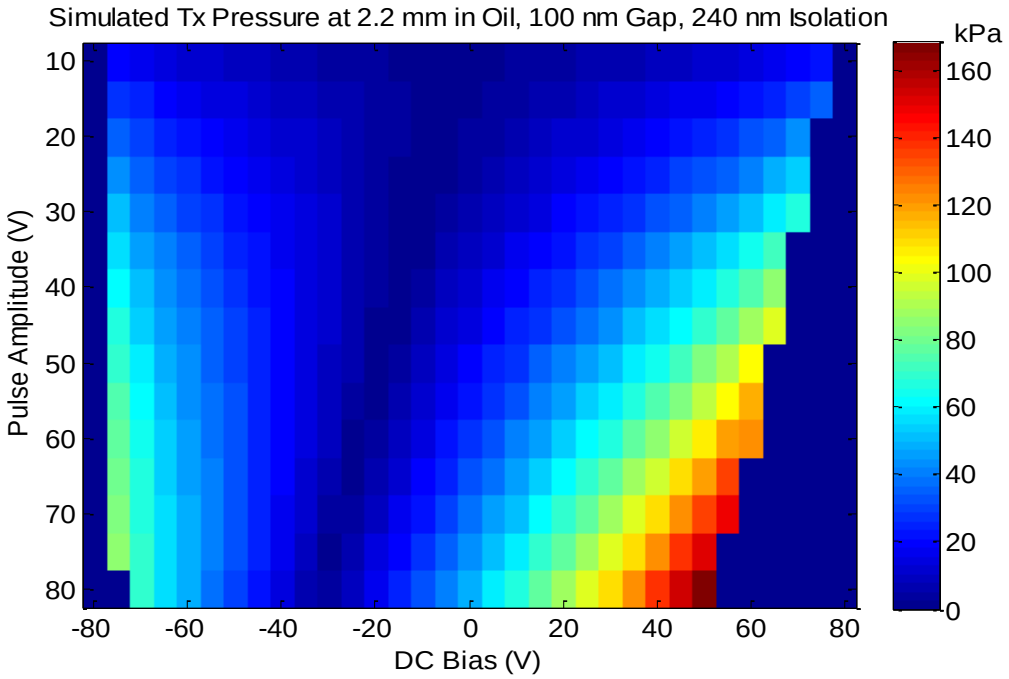


Figure 83. Simulated transmit pressure for the CMUT with 100 nm gap and 240 nm of silicon nitride isolation.

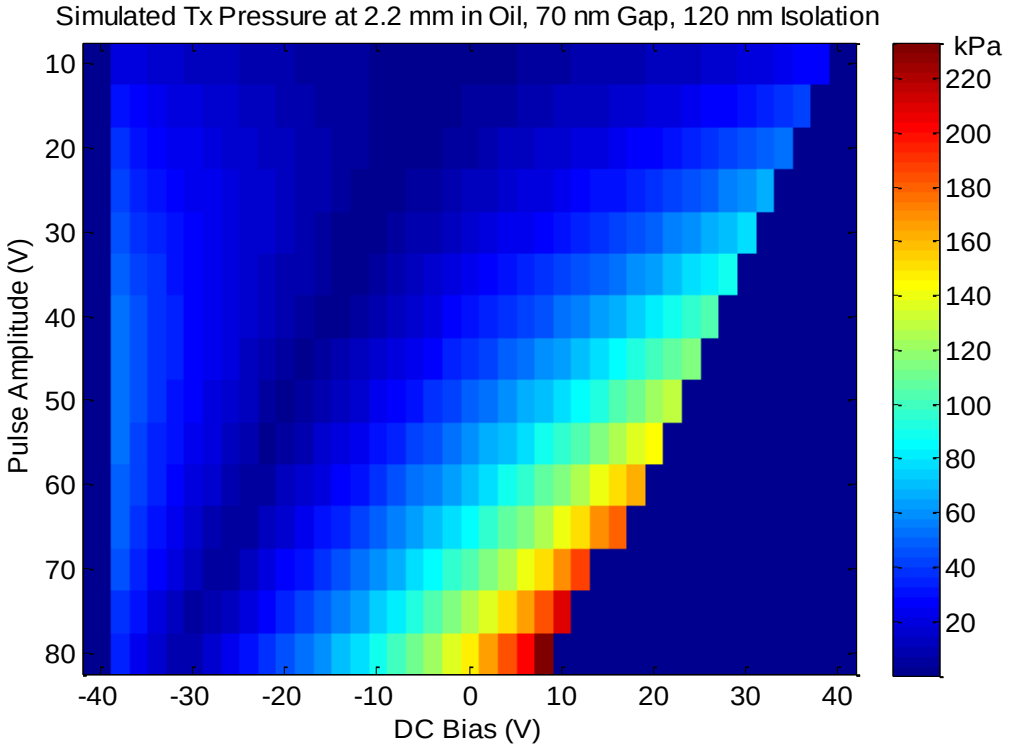


Figure 84. Simulated transmit pressure for the CMUT with 70 nm gap and 120 nm of silicon nitride isolation.

Test arrays with 100% electrode coverage, 35 µm x 35µm, as shown in Figure 85 bottom, were concurrently fabricated for transmit optimization. With an increased active electrode area, the transmit pressure is theorized to increase at the cost of overall reduced electromechanical coupling efficiency and hence increased power. Preliminary transient finite element analysis in COMSOL with a 30 V 20 ns pulse indicated an increased Tx pressure from the full electrode configuration. As a figure of merit, the ratio of the Tx pressure for the 35 µm x 35µm electrode is divided by the transmit pressure for the 25 µm x 25µm electrode. Both devices were tested in vegetable oil with a hydrophone using a 20 ns pulse with no DC bias. For the chrome sacrificial CMUTs, the ratio was measured to be 1.3 for the 80 V peak pulse. For the 65 nm copper sacrificial CMUT, the ratio was found to be 0.94 for the same 80 V pulse which does support theory. However, it was observed that the bottom and top electrode layers were fabricated with layer thickness ~ 1/3 of previously reported devices [108, 109]. As these devices were tested using bond pads, it was theorized that the thinner electrode layers introduced a series resistance associated with the 10 µm x 350µm connection lines that was previously neglected. Additional devices fabricated on the same substrate contained multiple bottom electrodes and the electrode electrical resistance was measured to be 5.35 kΩ/mm for the 30 nm bottom electrode. Therefore a second fabrication with double the electrode thickness was used for comparison purposes. The bottom electrode resistance was measured to be 1.2 kΩ/mm, a 4.5x reduction. The Tx pressure ratio was measured to be 1.45 in agreement with the chromium fabrication.

The use of thinner electrode layers was originally implemented as a fabrication optimization as the time required for the wet etch used to define the electrode is reduced. This is of particular importance as the bottom electrode etchant, CR-7s, attacks the copper sacrificial layer. Further, as the silicon nitride isolation is used to prevent shorting of the top and bottom electrodes, a reduction in the bottom electrode thickness allows for thinner silicon nitride isolation layers to prevent shorting at the sharp electrode corners

and edges. As observed, the electrical resistance of the electrodes may interfere with the performance of a CMUT array. For the case of a linear array, the electrodes can be of similar size as the connection lines used for the DRA elements tested. Possible issues include non-uniform actuation across an array as well as reduced imaging SNR.

Utilizing the reduced gap and isolation fabrication for improved Rx sensitivity as well as increased Tx pressure, the SNR increase for the dual-ring array CMUT configuration would be 11.4 dB. With the modification of the top electrode to full coverage for the Tx elements, the SNR would be further increased by 2.9 dB for a total improvement of 14.3 dB. With this improvement in overall SNR, alternate dual-ring array designs with fewer elements for an increased volumetric frame rate can be investigated.

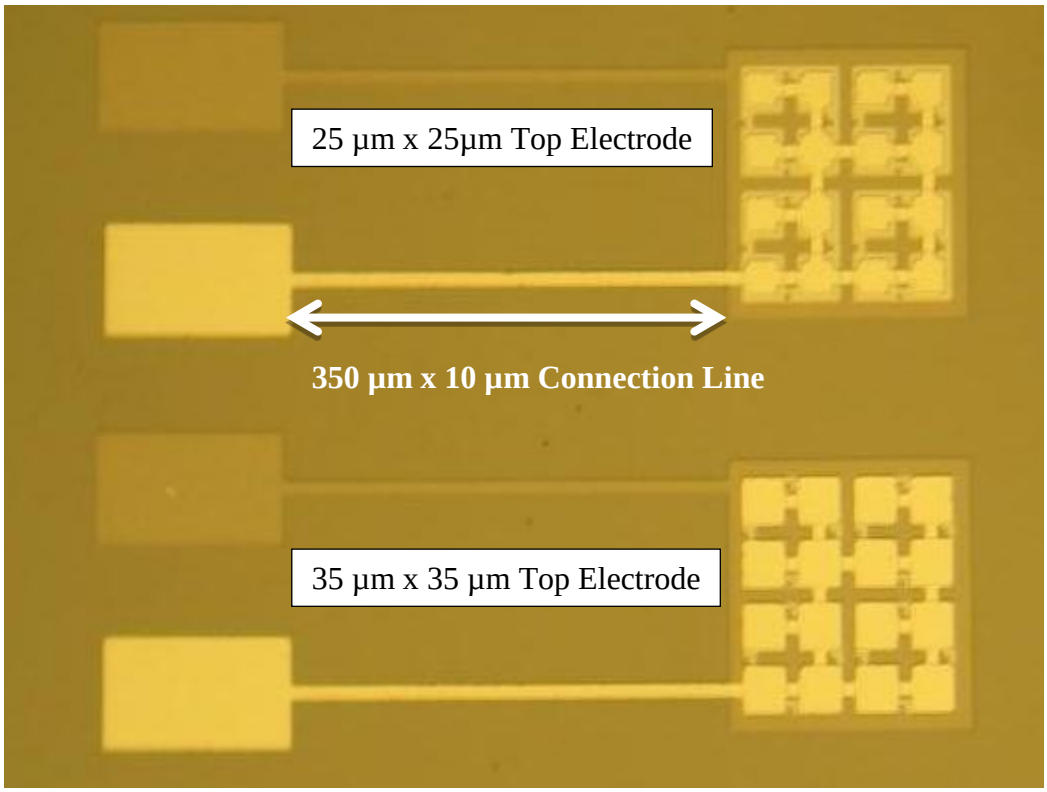


Figure 85. Sample DRA test elements using 35 µm x 35 µm membranes in a 4 x 4 configuration with bond pads for electrical connection. Two options include 25 µm x 25 µm top electrode coverage (top) and full electrode 35 µm x 35 µm coverage (bottom).

5.7. Summary

The development of the dual-ring array for forward-looking IVUS integration has been described. Monolithic integration with custom CMOS electronics has been achieved with an overall cable count of 13, meeting the design criteria for catheter integration. Imaging experiments using a wire target in oil with integrated pulsers were found to have 20 dB SNR from the A-scan data and imaging of a chicken heart with 40 dB dynamic range was achieved. Imaging 1 cm into the tissue was possible, demonstrating the ability to image a CTO, meeting the design goal.

Based on the electronics limitations, specifically the 25 V pulse generation, experimental test arrays were fabricated using both the chromium and copper sacrificial fabrication techniques as described in CHAPTER 3. Experimental results show that with a reduction in vacuum gap, 100 nm to 70 nm, and reduction in isolation layer, 240 nm to 119 nm, the transmit pressure and receive sensitivity can be increased by 7.9 dB and 3.5 dB respectively. Large signal simulation trends were shown to be in agreement with the experimental measurements indicating full gap swing was achieved for maximum transmit pressure, 230 kPa at 2.2 mm in oil. Simulations indicate that surface pressure at the same maximum operational point is in excess of 8 MPa as identified as a performance goal for CTO imaging. Additional characterization of test arrays with full electrode coverage indicate increased transmit pressure by 2.9 dB for a total of 14.3 dB improvement.

CHAPTER 6

ANNULAR CMUT ARRAYS FOR SL-IVUS

Side-looking (SL) arrays are useful for interrogation and investigation of the arterial walls and are a proven technology with PZT based catheters with the ability to generate 3D images through mechanical scanning techniques. Most recent interest in ultrasonic imaging is in higher frequency ranges, above 20 MHz for increased imaging resolution [10, 14, 55, 56, 72]. IVUS is well suited for such high frequency imaging as it has direct access to the regions of interest as compared to external ultrasonic imaging methods where acoustic attenuation in the body becomes significant [105].

In conjunction with the forward-looking dual-ring array, a multi-element annular array for side-looking applications is desired for dynamic focusing capabilities. As discussed in CHAPTER 2, the advantage of the annular array design is the ability to adjust the focal point through a time delay introduced between annular ring elements. For real time imaging, these annular-arrays can employ a nominally fixed focus in the transmit mode with dynamic focusing in the receive mode. With this configuration, the transmit focus can be adjusted for each frame as necessary [110, 111].

In comparison to the dual-ring array, the annular-ring array is completely filled with CMUT membranes, significantly increasing the active area. Therefore, the pressure in transmit is of secondary concern, but the acoustic cross-talk becomes a significant issue as it affects the imaging resolution. Therefore the modeling tools developed in CHAPTER 4 were used to evaluate arrays of CMUT membranes for the purpose of acoustic cross-talk reduction.

The following sections describe the development of an eight element CMUT annular array suitable for operation at 40 MHz with an overall diameter less than 1 mm

for side-looking IVUS applications with the objective of acoustic cross-talk reduction between elements to less than 20 dB.

6.1. Physical Description of a Side-Looking Annular Ring Array

The side-looking array as shown in Figure 86 is comprised of 8 equal area rings with an outer diameter of 840 µm. In this figure, the electronics are wire bonded to the annular array along with signal/power cables. With the rotation and pull back, the vessel wall can be imaged in the same manner as the current mechanically rotated IVUS catheters.

Figure 87-left shows these annular arrays placed on the four sides of the catheter, and therefore an image can be produced for each 90° rotation. With this configuration the catheter frame rate is increased fourfold. Utilizing the CMUT-on-CMOS processing, the arrays would avoid the need for wire bonding to the front end IC's, Figure 87-right, and with the addition of TSV's, the flexible tape circuitry can be used to integrate the side looking arrays with a minimum cable count.

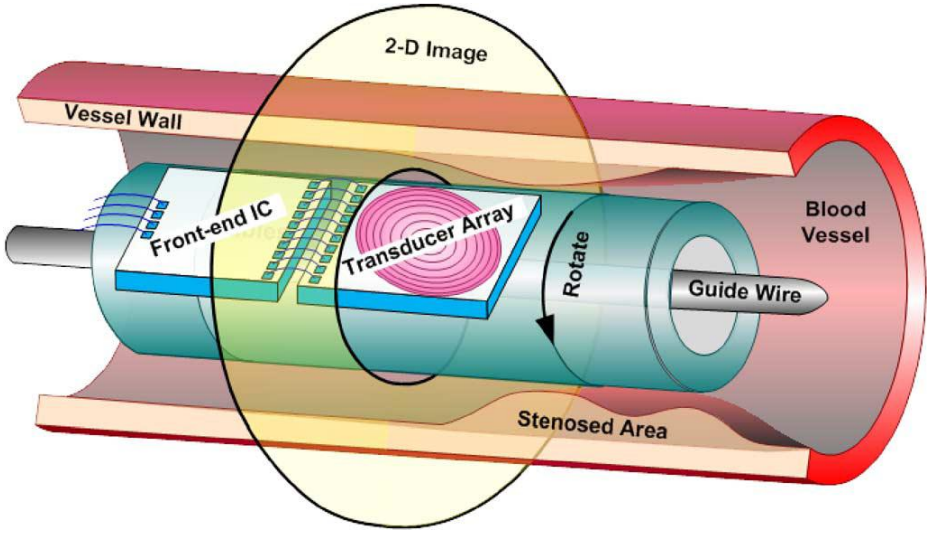


Figure 86. An annular array on the side of an IVUS catheter wire bonded to associated electronics which is rotated to generated a 2D cross-sectional image.

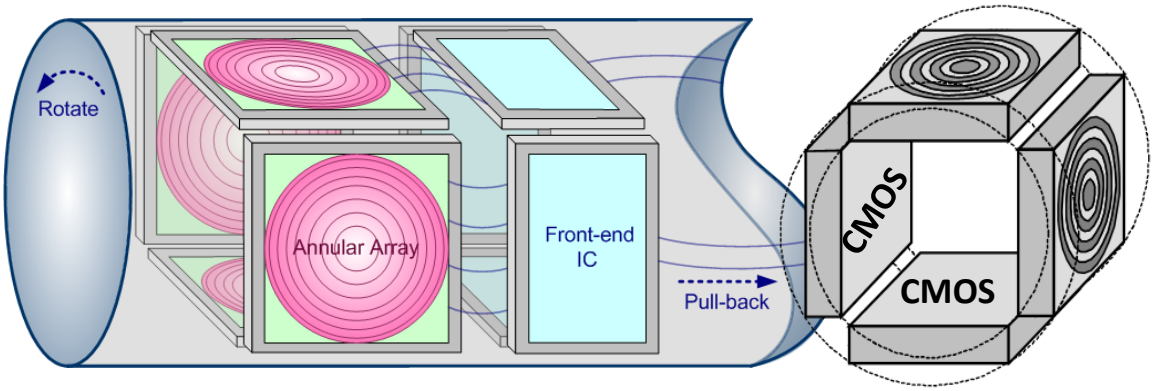


Figure 87. Four annular array devices placed on the outside of a catheter and wire bonded to electronics (left) and four annular arrays integrated with custom electronics to eliminate wire bonding (right).

6.2. Annular Array Specifications

For the aforementioned IVUS integration, the side looking arrays under investigation are sub mm in diameter with multiple rings for focusing capabilities at 40 MHz for high resolution imaging from 1 mm to 6 mm perpendicular to the catheter axis. With a 40 MHz center frequency, the axial resolution is calculated to be 19 µm. Physically to fit on the side of a 1 mm diameter catheter, the initial annular array configuration chosen was on the order of 800 µm in diameter. With equal area rings, the outer ring becomes the limiting factor in terms of minimum CMUT membrane size, and for an 8 element array configuration, the width of the outer ring can be calculate and was found to be 25.8 µm.

Initial calculations for desired transmit pressure were based on a circular piston transducer of radius *a*. The on axis pressure can be simplified from the Rayleigh Integral, equation

(28), assuming uniform surface displacement to equation (29). As depicted in Figure 88, left, the circular piston can be expanded further to include a geometric focus as described by equation (30) with r_e and h as described by equations (31) and (32) .

$$p(z,\omega) = \rho_0 c_0 u_0 [e^{jkz} - e^{(jk\sqrt{a^2+z^2}}] \tag{29}$$

$$p(z,\omega) = \frac{\rho_0 c_0 u_0}{q_0} [e^{jkz} - e^{-jkr_e}] \tag{30}$$

$$r_e = \sqrt{(z-h)^2 + a^2} \tag{31}$$

$$h = R_0 - \sqrt{R_0^2 - a^2} \tag{32}$$

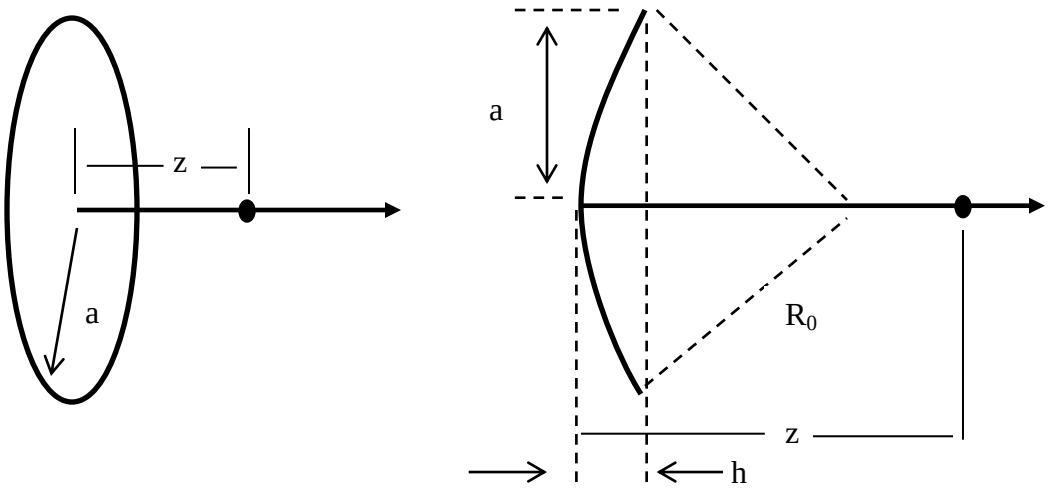


Figure 88. Circular piston (left) and circular piston with fixed curvature (right).

The ratio of the on axis transmit pressure to surface pressure is shown in Figure 89 over the region of interest for the case with no focus and with geometric focus from 6 mm to 1mm. Using equation (9) from CHAPTER 2 the equivalent time delay between elements to simulate a 6 mm focus would be 1.2 ns and for the 1 mm focus, 7.35 ns. In conjunction with the CMUT annular array, custom analog CMOS electronics for the receive mode have been fabricated and tested capable of achieving the desired 1-10 ns delays between all eight elements utilizing a single voltage control signal[112].

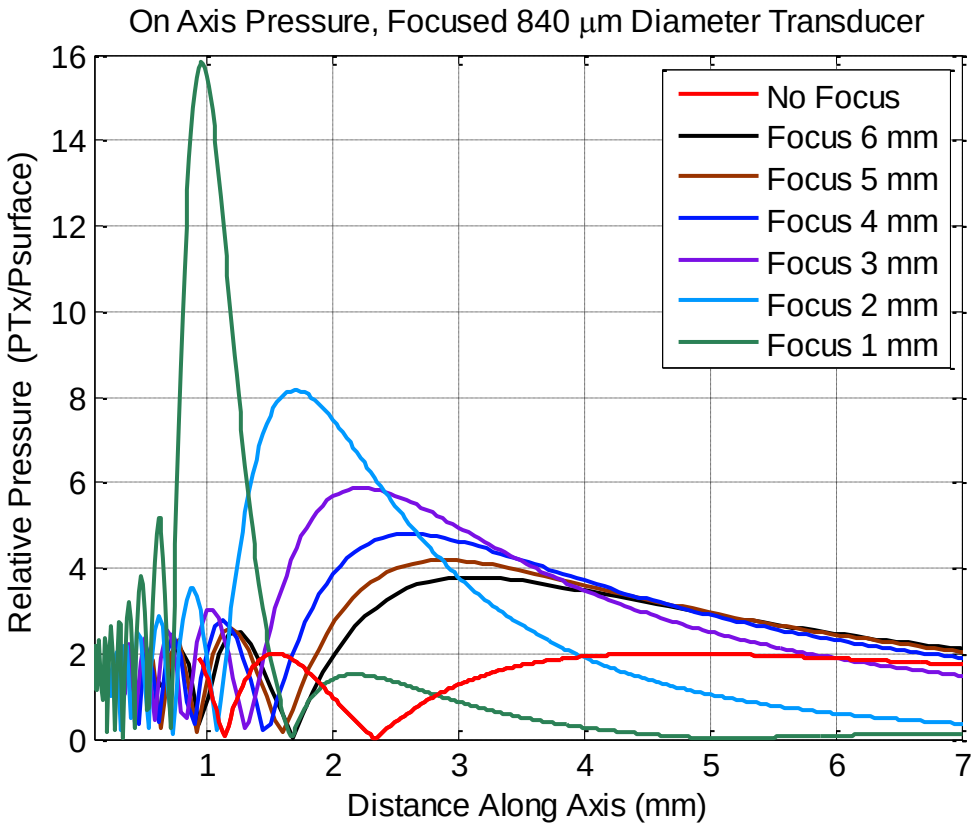


Figure 89. On axis pressure for a piston transducer without focus and with focusing from 6 mm to 1 mm.

Previous numerical simulations as described in [110] calculate the 2-way point spread function (PSF) for four different array structures for side-looking IVUS transducer arrays at 20 MHz with a 25 % FBW. The different structures shown in Figure 90, from left to right, are a single circular transducer, single rectangular transducer, solid-state array, and phased annular array. The radius of the circular transducers was set to 420 μm to be consistent with the CMUT annual array, and the phased annular array was divided into 8 elements. The rectangular array was set to be 840 μm x 560 μm while the 64 element solid state array utilized 38 μm x 560 μm elements. The PSF simulations show

that the annular array has the best performance in the lateral dimension as well as in the axial direction.

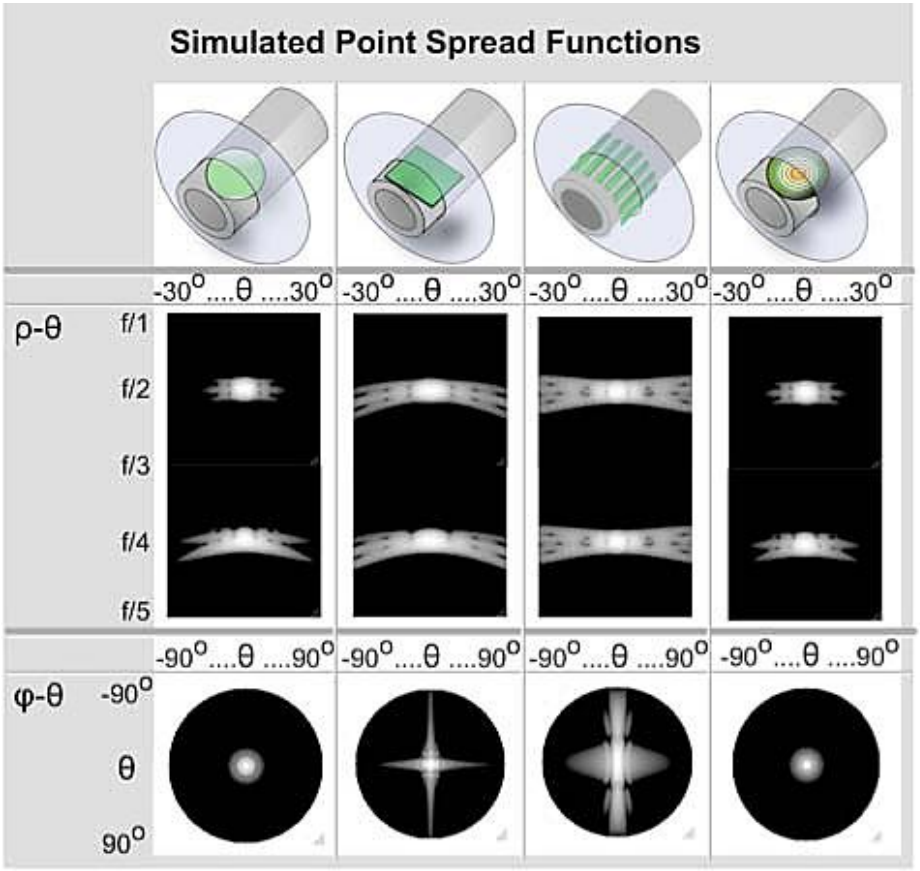


Figure 90. Simulated 2D PSFs for different probe types for an image depth of 3.36 mm. The transducer with imaging plane is shown (top) cross-section at f/2 and f/4 (middle) and surface cross section at f/2 (bottom) [110].

For the case of the side looking annular array, a similar analysis to that of the dual-ring array can be performed for imaging of the vessel wall through blood and imaging into the tissue. The center frequency was set to 40 MHz with a 40 MHz bandwidth. The membrane population density over the surface of the array was set to 80% to account for the connection lines and non-active space between membranes. The noise estimate was based on the ratio of the surface area of the annular array, 0.55 mm^2, to the 70 μm x 70 μm membrane where 3 mPa/√Hz was measured. This estimate effectively lowers the noise floor from the increased active CMUT area. The required

surface pressure to image a vessel wall through blood with 30 dB SNR was previously calculated to be 50 kPa and to image through tissue was 175 kPa. Transmitting through blood and tissue interface twice requires 880 kPa. At the 40 MHz center frequency set point, 880 kPa translates to a piston displacement of 2.3 nm. With noise introduced from switching electronics and analog delay circuitry, the required surface pressure to achieve an overall 30 dB SNR will increase. However, at the desired frequency, 40 MHz, the necessary displacement to produce appropriate pressure levels, 2.3 nm, is significantly smaller than previously fabricated CMUT vacuum gaps, 100 nm, and should not pose a fabrication challenge.

6.3. Fabricated Annular Arrays

Based on the physical size limitations and imaging requirements, CMUT annular arrays with eight ring elements were designed with an overall diameter of 840 μm. Through the development process, three iterations of devices with distinct array patterns and membrane shapes were successfully fabricated and tested.

6.3.1. Initial Annular Array

Figure 89-left shows the first test array with 8 top electrode bond pads and one bottom electrode bond pad. This array is comprised of 18 μm x 60 μm membranes linked to form 21separate concentric rings with a pitch of 20 μm, Figure 91-right[110].The individual rings were electrically linked to approximate equal area elements as listed in Table 17 with an overall 82% active area. The annular ring array shown was designed to operate at a center frequency of 40 MHz with a membrane thickness of ~2.5 μm.

It is important to note that this initial annular array did not meet the equal area design requirement as each of the eight elements was limited to a finite number of rings

as listed in second column of Table 17. The largest element was nearly three times the size of the smallest.

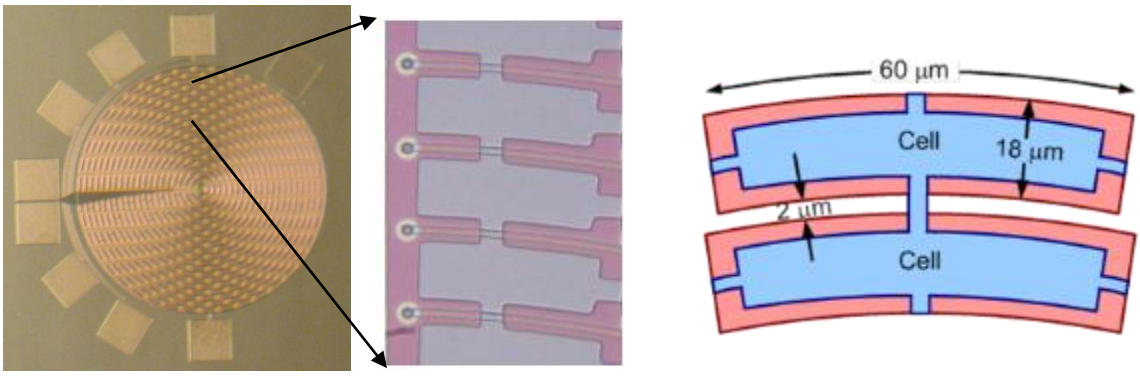


Figure 91. Fabricated 8 element CMUT annular array (left) with membrane dimensions (right).

Table 17. First Generation Annular Array Areas

Element #	# of rings	# of membranes	Area µm^{2}x 1000
1	5	25	26.0
2	3	39	40.5
3	3	57	59.2
4	3	75	77.9
5	2	60	62.3
6	2	66	68.5
7	2	75	77.9
8	1	41	42.1

6.3.2. Second Generation Annular Array

In the second iteration, the individual CMUT membrane shape was modified to be 20 µm x 45 µm with 15 µm x 37.5 µm top electrodes to allow for equal area elements. Figure 92 shows a fabricated device with bond pads including an extra ground electrode connection. The CMUT membranes were placed in an alternating pattern to break up the radial periodicity in an attempt to reduce acoustic cross talk. Although the elemental areas deviate by less than 5%, in this configuration, the active area is reduced to 53%,

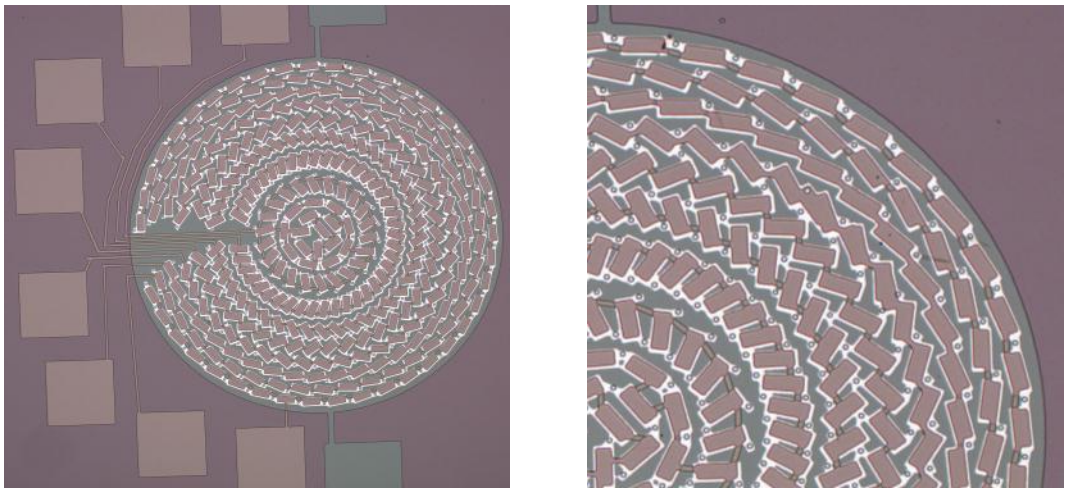


Figure 92. Second generation of annual array with equal area elements along with varied periodicity in the radial direction.

Table 18. Second Generation Annular Array Areas

Element #	# of rings	# of membranes	Area μm^2 x 1000
1	1	38	34.2
2	1	41	36.9
3	1	42	37.8
4	1	41	36.9
5	1	41	36.9
6	1	41	36.9
7	1	41	36.9
8	1	41	36.9

6.3.3. Third Generation Annular Array

For the third design, the individual CMUT membrane shape was further modified to be 20 µm x 20 µm with 15 µm x 15 µm top electrodes. This configuration was chosen in an attempt to reduce higher order modes that may be present in the longer dimension of the previous design. Figure 93 shows the fabricated devices which also includes the extra bottom electrode pad. From the smaller CMUT membrane implementation, it was found to be more difficult to combine the CMUTs electrically into equal area elements,

Table 19. The deviation from one element to the next did not exceed 25% and the active area was found to be 50%.

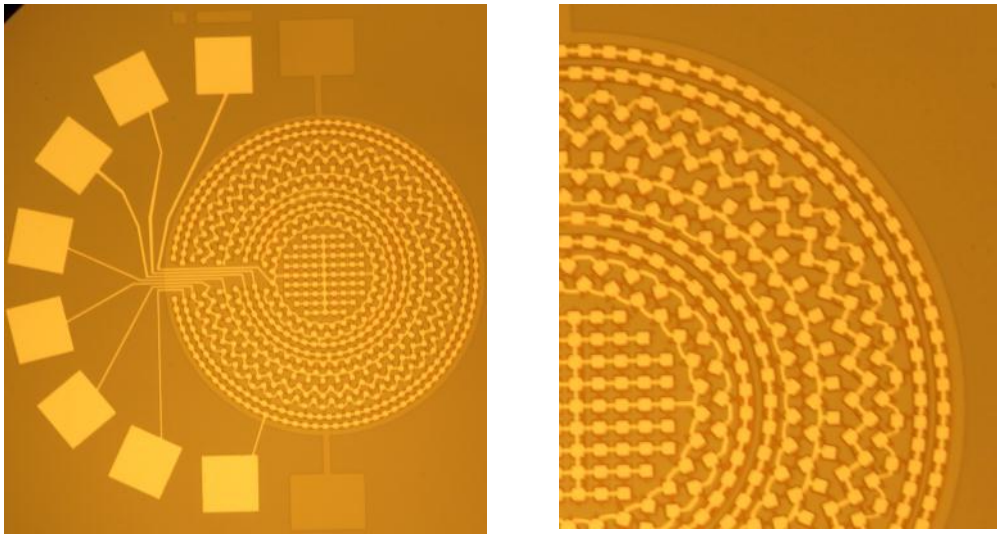


Figure 93. A third generation annular array with square membranes for reduced acoustic cross talk.

Table 19. Third Generation Annular Array Areas

Element #	# of rings	# of membranes	Area μm^2x 1000
1	~5	97	38.8
2	2	72	28.8
3	2	86	34.4
4	2	77	30.8
5	2	87	34.8
6	2	86	34.4
7	1	91	36.4
8	1	90	36.0

6.3.4. Initial Annular Array Testing in Water

To evaluate the transmit pressure, radiation pattern, and frequency response, experiment were performed in water using an ONDA HGL-0085 hydrophone and data collection through the use of a Tektronix TDS 5054 oscilloscope. Annular arrays were wired bonded to custom PCB's and coated with 3 µm of Parylene C using a SCS Labcoater PDS 2010 for electrical isolation while submerged in water. The test setup, as

shown in Figure 94 shows the hydrophone placement with respect to the submerged array as well as the mechanical scan direction of the hydrophone.

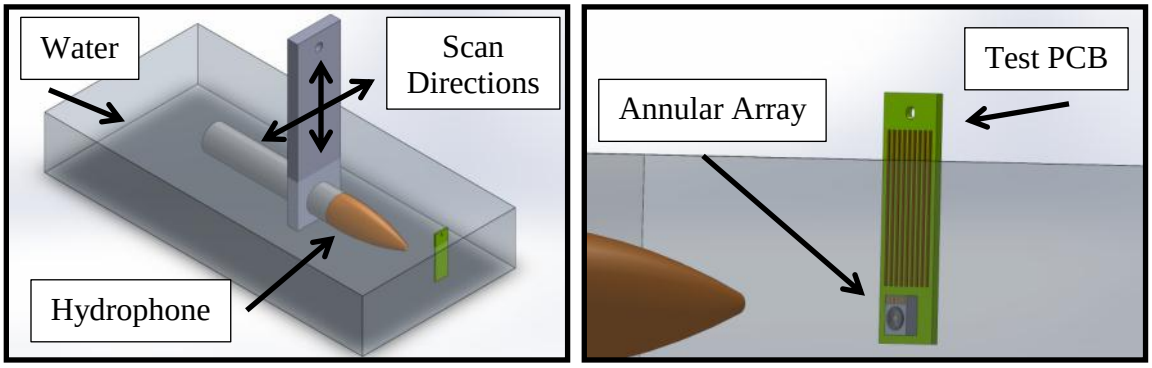


Figure 94. The test setup used for annual array evaluation in a water bath using a hydrophone with xyz stage.

Data was collected 6mm from the array surface with a 180V DC bias and 90V pulse from a Panametrics pulser/receiver model 5072PR. A sample time domain signal from the inner annular array element with corresponding frequency response is shown in Figure 95. The peak to peak pressure from this element was measured to be 140 kPa indicating surface pressure in excess of 1 MPa and therefore suitable for imaging applications. From this element, undesirable ringing in the time domain can be observed at 4.2 μs.

Two dimensional scans were also performed to evaluate the radiation pattern. Data was collected over a 2 mm by 2 mm area at a distance of 3 mm with spatial resolution of 0.05 mm. Figure 96 shows the measured radiation pattern from the fourth element with narrow band filtering at 38 MHz as compared to a piston ring approximation, showing good agreement. However, at 32 MHz, Figure 96, the piston ring approximation deviates from the measured response as indicated by the two lobes on the vertical axis above and below the main lobe.

As a further example, a pitch catch experiment was performed in water using two identical annular arrays. Figure 98 shows the time domain signal from the receive annular array which was separated by 4.5 mm. All eight ring elements were used simultaneously

for transmit and receive without any focusing. Ringing in the time domain can be seen after the main pulse, 3 μs, from 3.1 μs up to 4.2 μs.

To guide further development, finite element analysis was pursued to simulate the ringing in the time domain as well as the measured additional side lobes not predicted by the piston approximation.

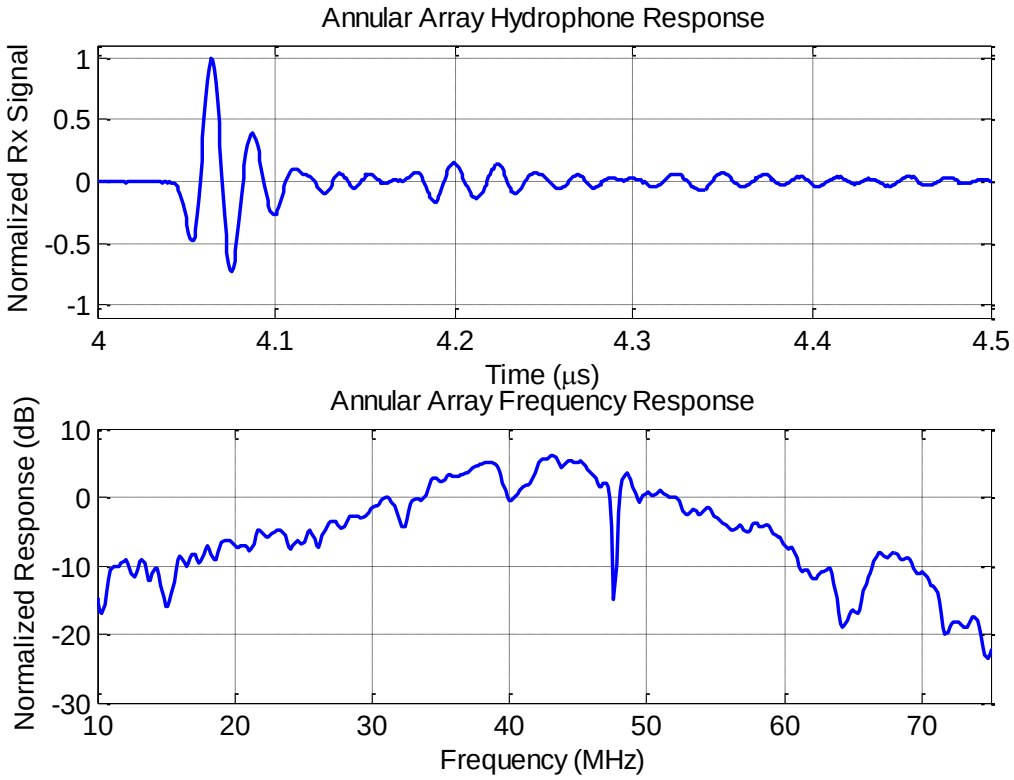


Figure 95. A sample time domain normalized receive signal from the center annular array element with corresponding frequency response.

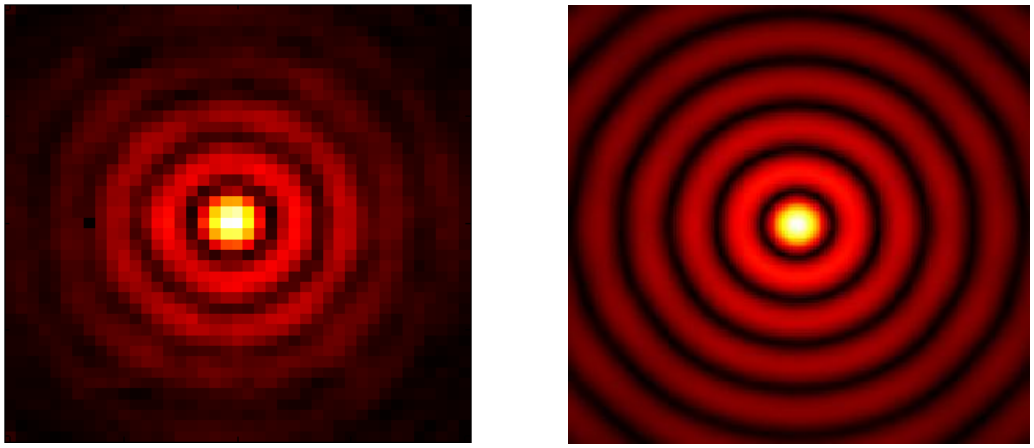


Figure 96. Radiation pattern from the 4th element filtered at 38MHz, measured versus piston approximation.

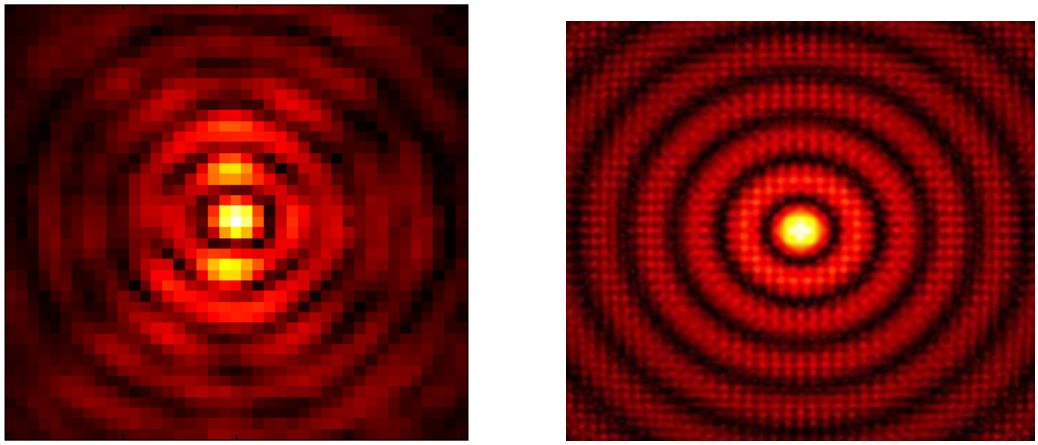


Figure 97. Radiation pattern from the 6th element filtered at 32 MHz, measured versus piston approximation.

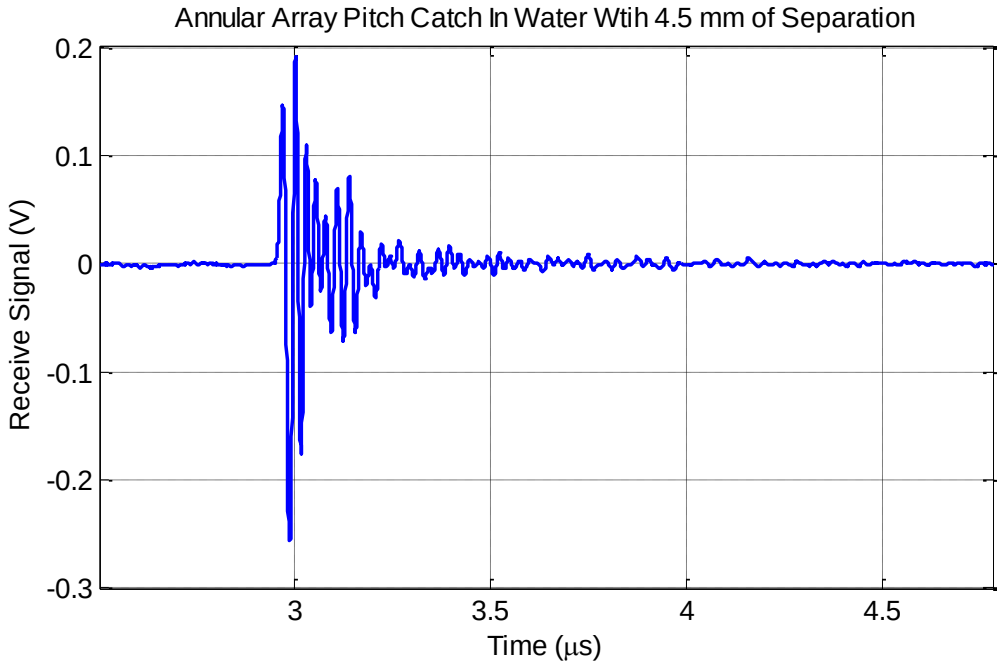


Figure 98. Initial annular array pitch catch experiment in water.

6.3.5. Initial Annular Array Imaging

A fabricated CMUT annular array used for experimental testing were found to have center frequencies of 20 MHz and 50 MHz with a 6 dB FBW of 105 % and 40 % respectively [110]. Each array was wire bonded into ceramic DIP package, Spectrum Semiconductor Material Inc. part CSB06426, and inserted into a ZIF socket on a custom PCB. Pitch-catch experiments were performed using pairs of neighbor elements due to the limitations of the electronics for a total of 7 combinations. The experimental setups with wire target locations are shown in Figure 99. SNR calculations were made using the RMS value of the noise from a section of data without any acoustic signal, and the signal amplitude was taken from the RMS of the signal in the time window containing the echo pulse. For the 50 MHz device the SNR was found to vary from 12 dB - 22 dB, and for the 20 MHz device, 21 dB - 33 dB. The variation is mostly due to the significant difference in the elemental areas, Table 17. Reconstructed B-scan images are shown in Figure 100 along with simulated point spread functions. These results demonstrate the

imaging capabilities with acceptable pressure, center frequency, and bandwidth. However, the acoustic cross talk is an issue as is found in other arrays reducing the image quality as indicated by the image artifacts as show in the reconstructed images in Figure 100 [113].

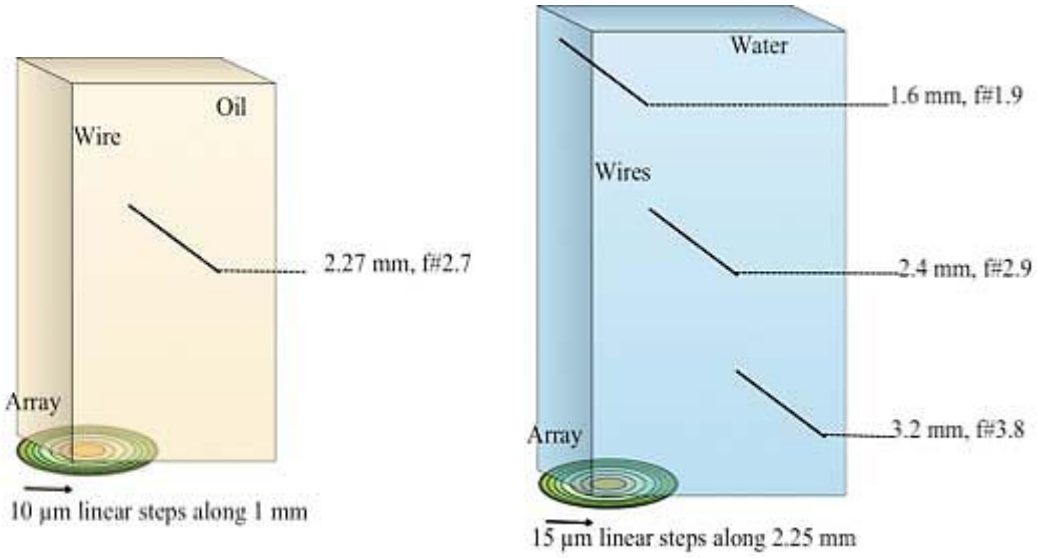


Figure 99. Experimental setups used for evaluation of the 20 MHz array (left) and 50 MHz array (right) [110].

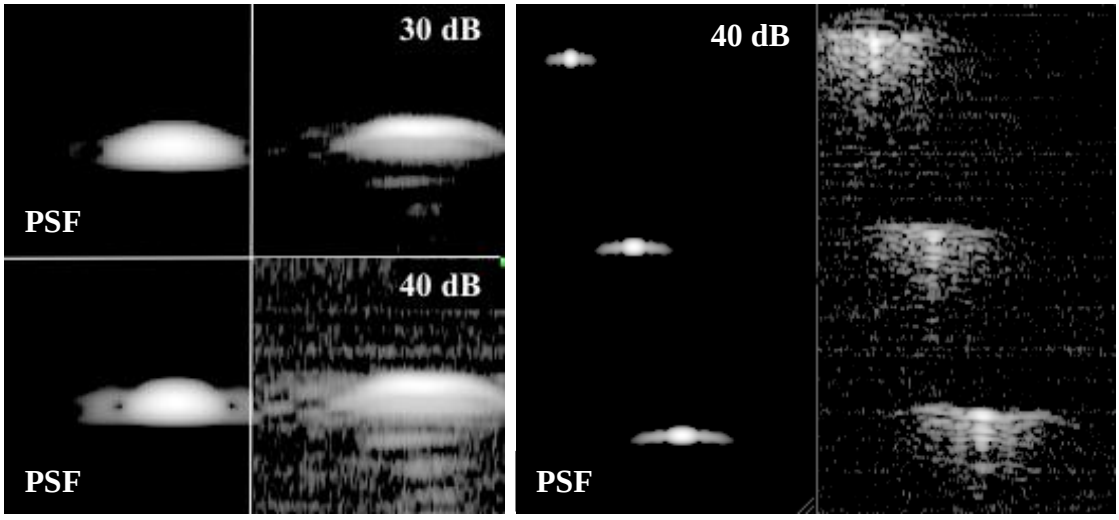


Figure 100. Imaging results are compared to the theoretical point spread functions for the 20 MHz experiment (left) and 50 MHz experiment (right) [110].

6.4. Finite Element Analysis for Crosstalk Evaluation

With respect to the annular arrays under investigation, crosstalk reduction is an important optimization which can be influenced by the element size, cross-section, and spacing. This acoustic crosstalk can manifest as a sharp resonance in the frequency response of the transducer which translates to a ringing in the time domain. This in turn directly affects the imaging capability from the introduced image artifacts. Standard acceptable isolation would be more than -20 dB from one element to another at the frequencies being utilized which is a specific design goal for the annual array design.

To evaluate the acoustic crosstalk, evaluation of the annular ring array design using FEA was performed with the multi-physics software ANSYS 12.0. Because of the ring nature of the CMUT annular array evaluated, it was possible to set up an axi-symmetric model to evaluate the 21 ring 3D array in a 2D simulation. The structural materials were modeled with PLANE183 elements and the fluid was modeled with FLUID29 elements, and an absorbing boundary was modeled with FLUID129 to simulate an infinite fluid medium. Sample code can be found in APPENDIX C. A view of the geometry modeled with a close up view of a single ring cross section is shown in Figure 101. The same geometry is shown meshed in Figure 102 with the solid-fluid interface flagged in red, boundary conditions shown with triangles, and loads shown as red arrows. Harmonic simulations were performed at discrete frequencies where a pressure load was applied to specific rings corresponding to each of the eight elements. With the frequency and membrane displacement known, the normal surface velocity can be calculated and plotted to give the frequency response of the transducer.

As each element is activated in turn over a given frequency range, data is simultaneously collected for the other seven elements to measure acoustic cross talk. Figure 103 shows the frequency response of the fifth element, E5, in red, along with the response from the neighboring elements for a device with a 2.5 μm membrane thickness.

It can be seen that at 25 MHz and 65 MHz, there is significant undesirable coupling to neighboring elements. The average separation from the 5th element to neighboring elements, 4 and 6, was found to be -13 dB over the operational frequency range of the device, 20 - 60 MHz.

Two frequencies of particular interest where the cross talk is substantial are at 25 MHz and 65 MHz. Investigation of the finite element analysis in ANSYS indicates that the period of the rings and width of the membranes influences the frequency of the cross talk. Figure 104 shows the surface displacement, not to scale, for the harmonic simulation at 25 MHz. It can be observed that at this operational point, the surface displacement is associated with the pitch of the rings. It was also observed that at 65 MHz, the membrane exhibited the second mode shape effectively reducing the average displacement across each individual membrane.

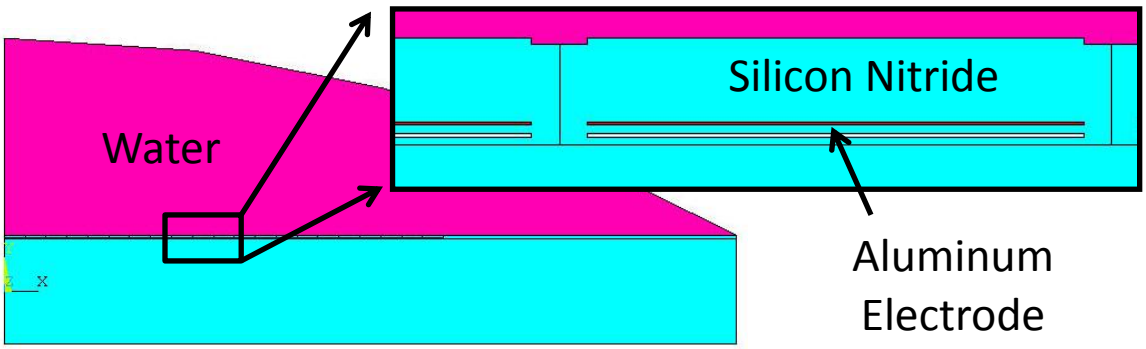


Figure 101. Annular array geometry modeled in ANSYS.

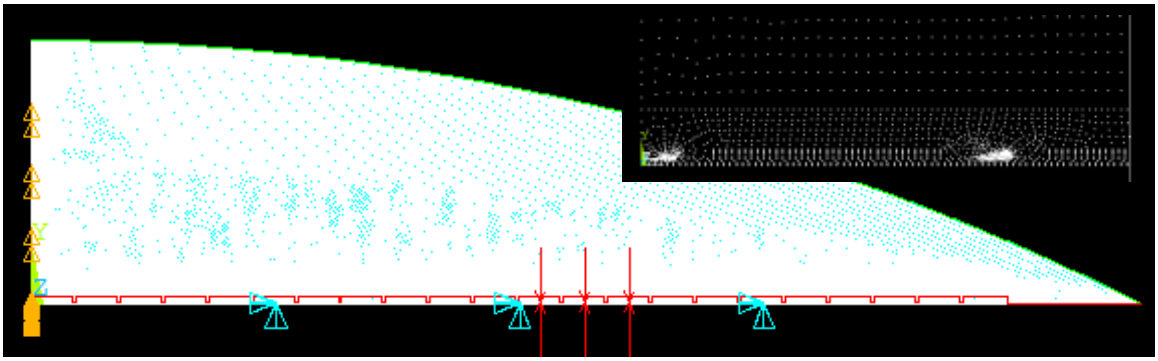


Figure 102. Annular array geometry meshed with boundary conditions shown as triangles and loads as arrows.

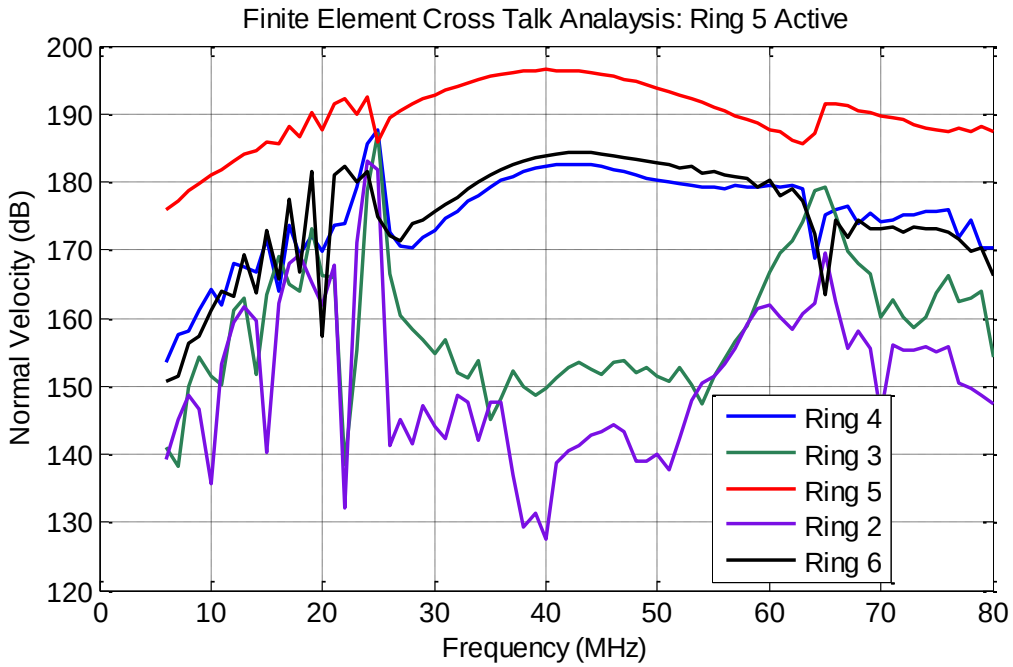


Figure 103. Finite element analysis shows the frequency response of a CMUT element, 5th ring, and crosstalk to neighboring elements.

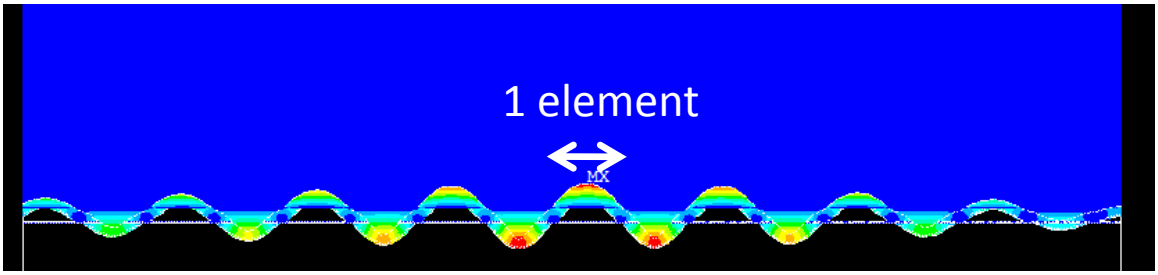


Figure 104. Surface displacement at 25 MHz with the 5th element active.

This analysis can be used to explain some of the dips in the measured frequency response; however it was also observed that the fabricated annular array exhibited a varied periodicity in the radial direction as indicated in Figure 105. The previous simulation assumed direction 1 where all elements are parallel, but in direction 2, the pitch is essentially doubled as every other membrane is mechanically constrained from the sacrificial release hole sealing. Therefore, three simulations were performed, one in direction 1, and two in direction 2. In direction 2, every other membrane was mechanically clamped and then switched. Figure 106 shows the measured radiation pattern at 32 MHz along with the initial FEA simulation results as well as the expanded FEA simulation. In can be seen that the secondary lobes are present in the expanded FEA, matching the experimental measurements. This result indicates the significance of the array placement and the need for a more complete array analysis.

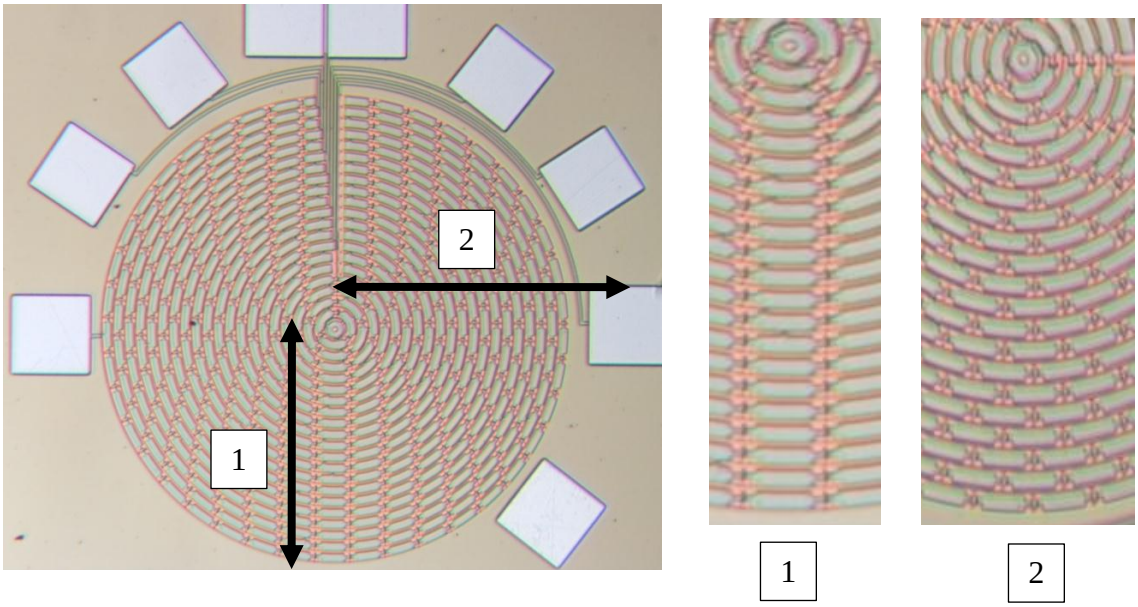


Figure 105. Annular array with varied periodicity in the two directions 90 degrees apart.

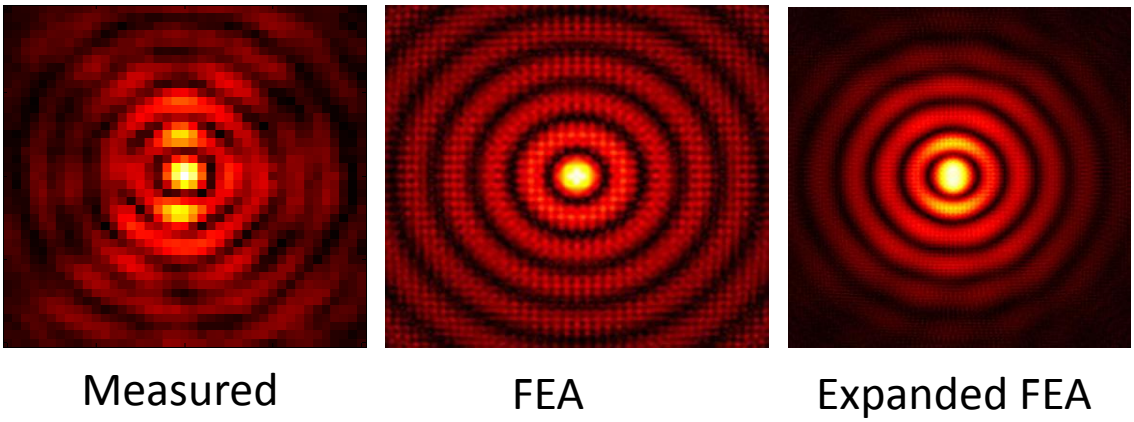


Figure 106. Measured radiation pattern versus a single FEA simulation versus the expanded FEA simulation.

6.5. Boundary Element Method Simulation

FEA was found to be difficult for full 3-D evaluation of the annular arrays due to excessive nodal count and associated computation time. Therefore, the BEM technique as described in CHAPTER 4 was used to assist in the evaluation of cross talk effects from the three annular array configurations. The meshing density for all three simulations was increased with minimum of 5% convergence. To reduce the overall computation time, simulations in this section use the small signal implementation with a 1 V AC excitation. Modeled arrays are shown of the left hand side with for Figure 107 through Figure 115 with corresponding normalized frequency spectra on the right hand side. The modeled array membranes are shown in blue, with active top electrode areas indicated in dark red.

6.5.1. Annular Array Design 1

Figure 107 simulates a 4 x 8 membrane section of the first annular array design using direction 1 as indicated in Figure 105. Figure 108 simulates the similar membrane configuration but using direction 2 as indicated in Figure 105 which is not possible using the axisymmetric FEA model. The three active ring simulation corresponds to elements 2 - 4 as listed in Table 17. These two simulations are similar to the axisymmetric FEA

simulations previously performed, but it is possible to observe a more complete interaction in the array configuration. The combined frequency response from both BEM simulations is in better agreement with the experimental results as compared to the previous FEA. The BEM simulations compare well with FEA when evaluating the crosstalk features, but the BEM requires significantly less computational resources which are a significant advantage.

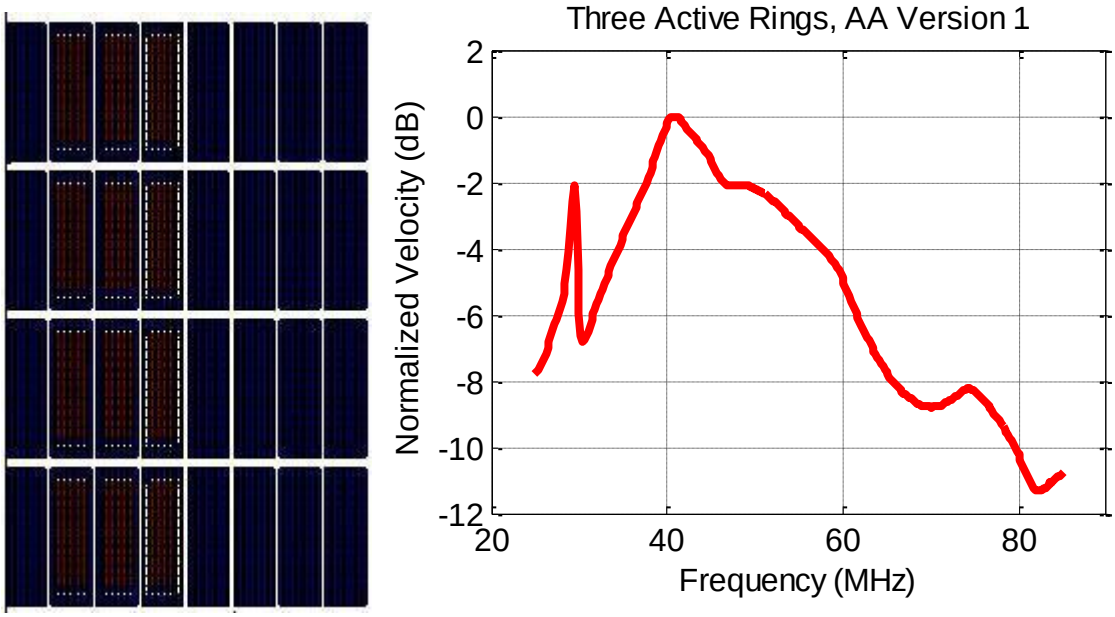


Figure 107. Annular array version 1 simulation with 3 active rings in a 4 by 8 membrane simulation.

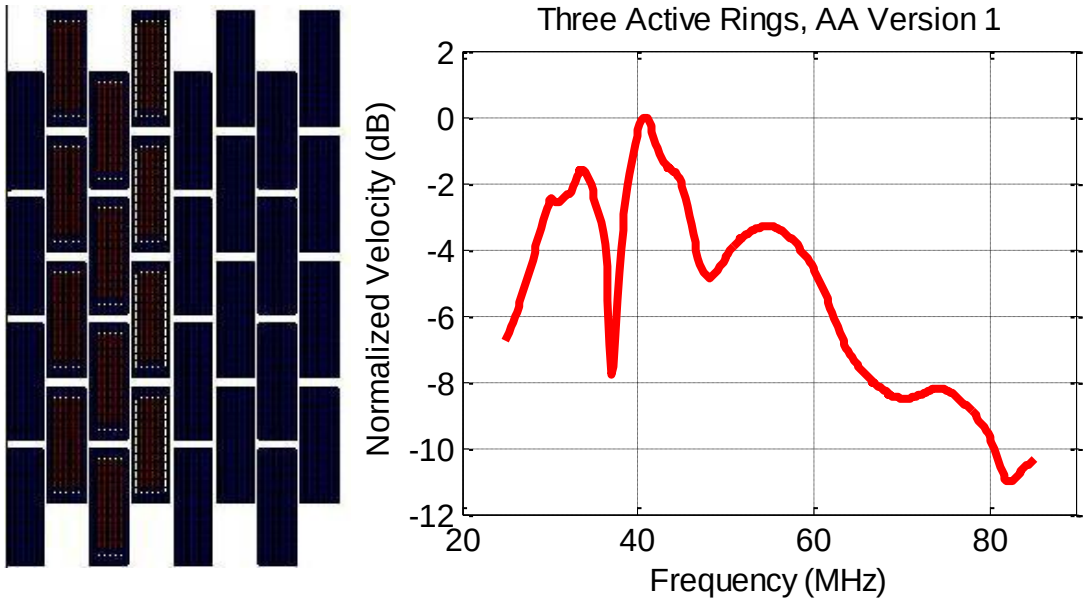


Figure 108. Annular array version 1 simulation with 3 active rings in a 4 by 8 membrane simulation offset to simulate the alternate radial periodicity.

6.5.2. Annular Array Design 2

For the second generation of annual array designs, segments of the third and fifth element were simulated. Figure 109 simulates the third ring element with five active membranes surrounded by four neighbor membranes on either side. For this element, the frequency spectrum does not show significant dips in the frequency response, but the center frequency was found to be lower than originally predicted for a single membrane. Figure 110 shows a simulation for the fifth element with three active membranes. The frequency response for this simulation is not ideal with a notch at 40 MHz. Nominally, the center frequency can be increased through the use of a thicker membrane. However, the other six rings all exhibited different frequency responses, which is not ideal for imaging purposes. It is important to note that the BEM simulation capability was under development when the second generation annular array was designed and it was assumed that varying the radial periodicity would significantly reduce the acoustic crosstalk.

Figure 111 shows the relative displacement of the array surface at 30 MHz and 41 MHz for the array shown in Figure 110. At 30 MHz it can be seen that the active

membranes are operating in the first mode which is associated with the center frequency of the ring element. However, at the 41 MHz dip in the frequency response, a higher order mode is observed where the average displacement of the active membranes is significantly reduced. This phenomenon was also observed at 48 MHz and 54 MHz.

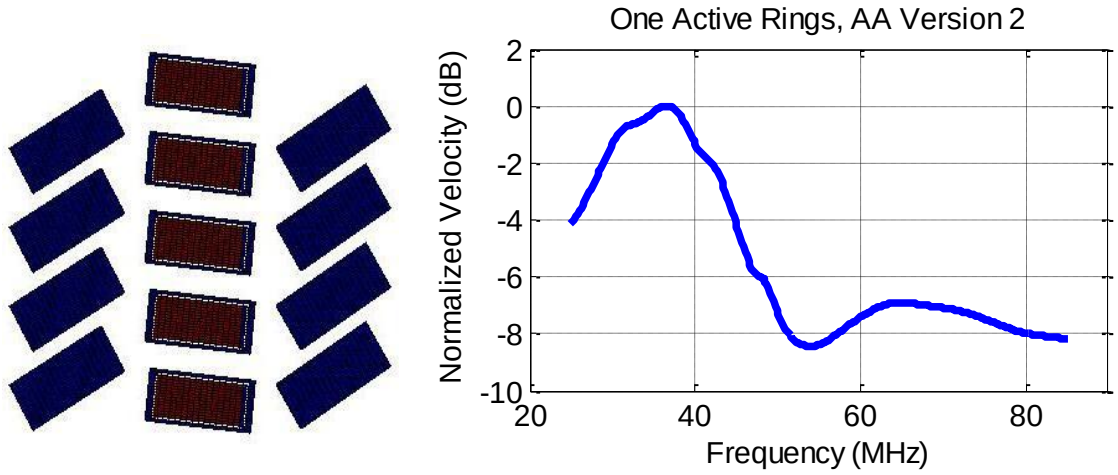


Figure 109. Annular array version 2 simulation with 1 active ring to simulate the third element.

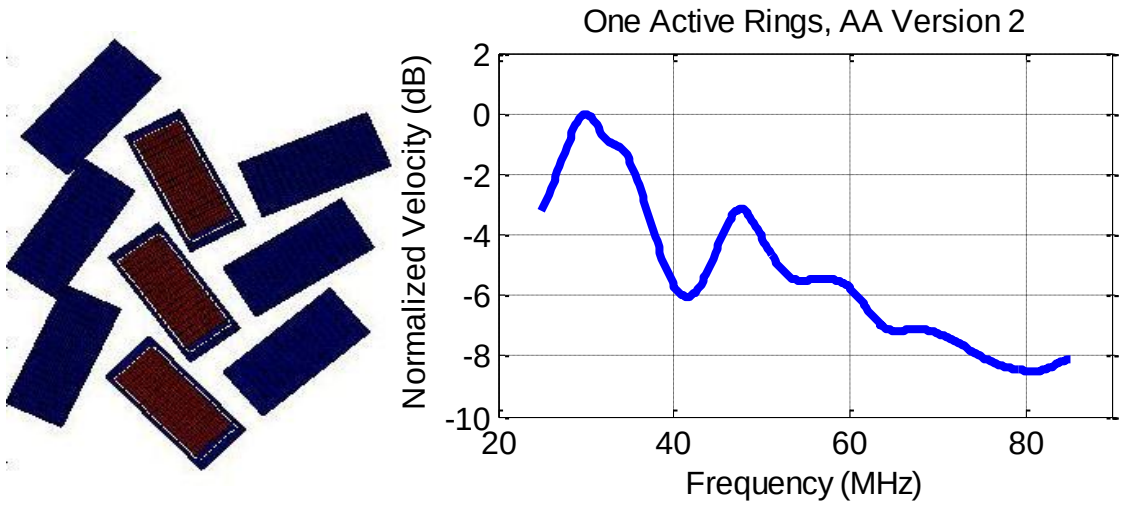


Figure 110. Annular array version 2 simulation with 1 active ring to simulate the fifth element.

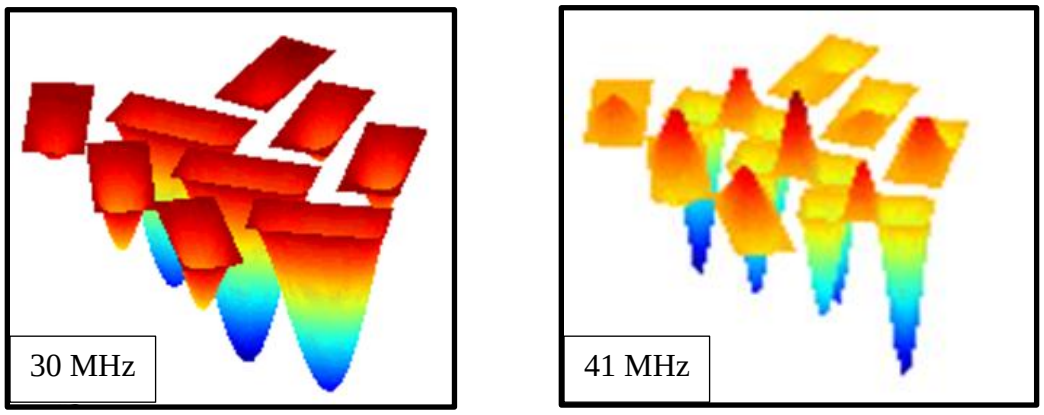


Figure 111. Mode shapes at 30 MHz and 41 MHz for the array configuration shown in the figure above.

6.5.3. Annular Array Design 3

The third annual array design with square membranes to suppress higher order mode shapes over the frequency range of interest. First, simulations were performed to approximate the first design array criteria with all membranes aligned and subsequently offset. Figure 112 shows the first array configuration, 7 x 4 membranes, with three rows active along with corresponding frequency response. Between 30 MHz and 60 MHz, the frequency response does not show sharp resonances over the frequency range of interest. Figure 113 shows the same array with offset, and it is important to note that the frequency response is similar to the non-shifted simulation with only minor variation. For the array configuration in Figure 113 the mode shapes at 28 MHz and 57 MHz are shown in Figure 114. It can be seen that at 28 MHz active membrane elements are out of phase leading to a reduced average displacement and at 57 MHz it can be seen that individual membranes experience a higher order mode where the average displacement of an individual membrane is reduced.

In the final simulation, Figure 115, quarter symmetry was utilized to increase the simulation with two columns of active membranes indicated by the light blue and red

electrode areas. The array membranes were rotated to simulate a fabricated array with varied periodicity. Additionally, the frequency response of the neighbor elements was calculated showing an average of -22 dB of separation over the frequency range of interest, 20 MHz to 60 MHz.

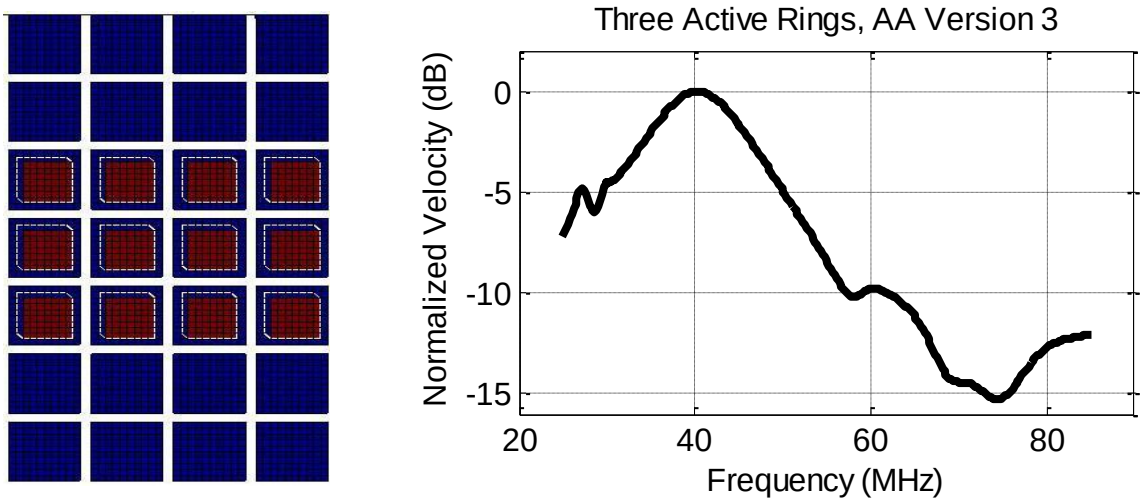


Figure 112. Annular array version 3 simulation with 1 active ring from three rows combined.

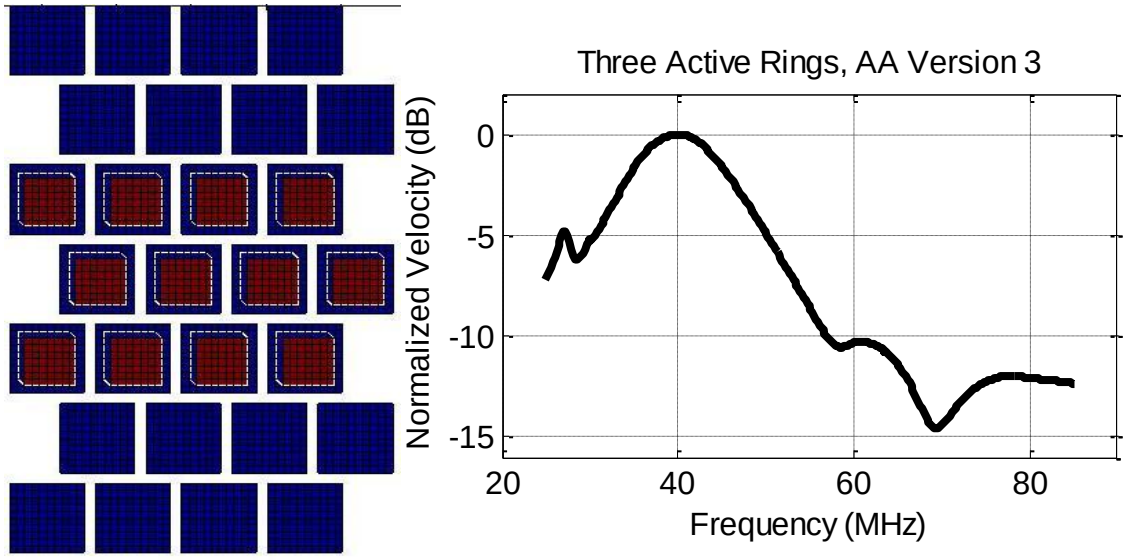


Figure 113. Annular array version 3 simulation with 1 active ring from three shifted rows combined.

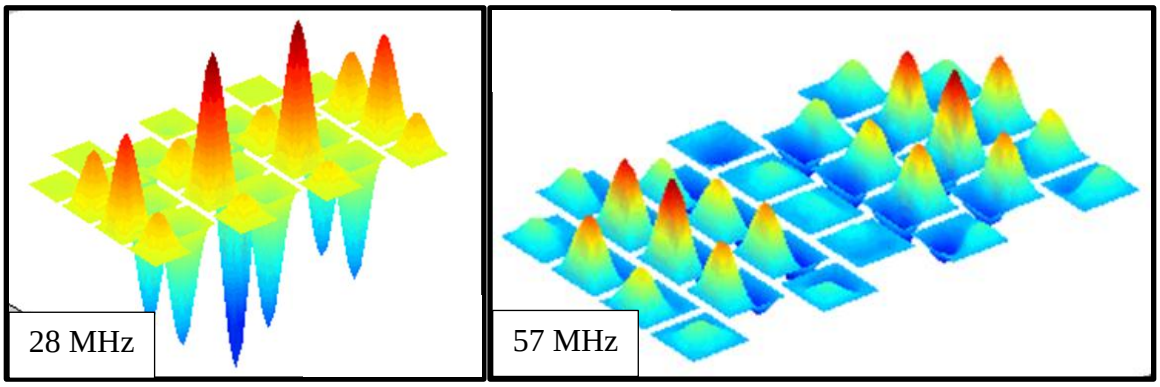


Figure 114. Mode shapes at 28 MHz and 57 MHz for the array configuration shown in the figure above.

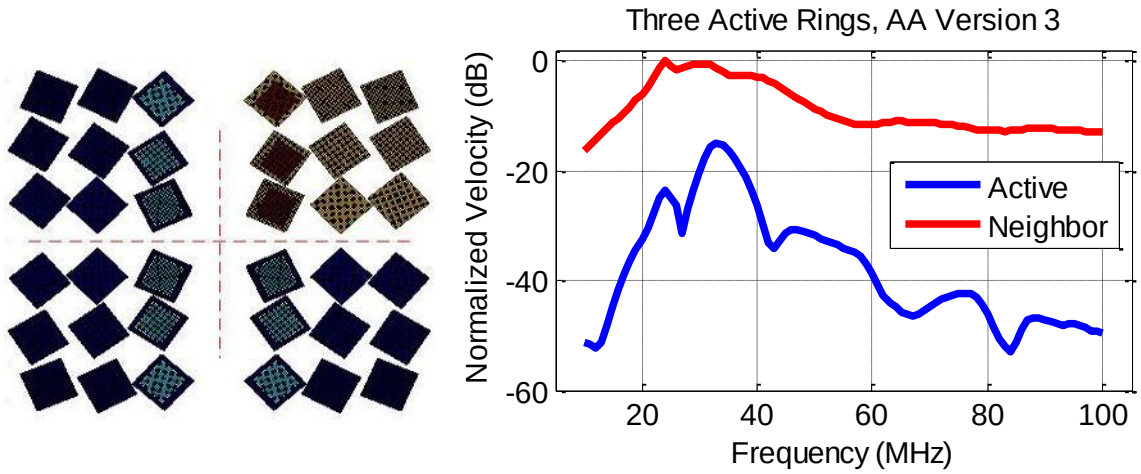


Figure 115. Annular array version 3 simulation with membrane rotation to remove periodicity.

6.6. Testing of the Second and Third Generation of Annular Arrays

For comparison purposes, the second and third generation of devices was fabricated on the same wafer with a membrane thickness of 2.2 µm, total isolation 0.3 µm, and vacuum gap of 0.1 µm. Devices were coated in 3 µm of Parylene C for hydrophone, ONDA HGL0085, testing. The DC bias was set to 120 V, for both devices, below the collapse voltage, and a 90 V broad band pulse was applied, Parametrics model 5072PR. Scan data was collected using an automated stage to move the hydrophone

parallel to the array surface over a distance of 6 mm with a spatial resolution of 0.08 mm. All data was collected at a distance of 6 mm in water. It should be noted that this characterization was not focused on optimal transmit pressure as the devices were not biased close to collapse, and with the same membrane thickness, the second generation device was shown to transmit more pressure as it was closer to the optimal operational point. An evaluation of all eight rings was performed for both devices and it was observed that the second generation devices, suffered from acoustic cross talk issues as predicted by the BEM modeling. The location of the dips in the frequency response varied depending upon the array orientation for a specific element. The third generation of annular arrays was found to be narrowband but the uniform across all elements was significantly improved as compared to the second generation.

For comparison purposes, Figure 116 and Figure 117 show the radiation pattern, time domain signal at the peak pressure location, as well as the FFT of the signal for the 4^{th} element of both devices respectively. From the radiation pattern in Figure 116, the -3 and -6 dB main lobe beam width was measured to be 0.34 mm and 0.5 mm respectively. The secondary lobes were measured to be 0.9 mm from the main lobe. The time domain signal was shown to contain ringing in the system past 4.6 µs, and the FFT of this signal shows a strong dip in the frequency response at 34 MHz. These results are in agreement with previous simulations.

From the radiation pattern in Figure 117, the -3 and -6 dB main lobe beam width was measured to be 0.3 mm and 0.6 mm respectively. The secondary lobes were measured to be 0.45 mm from the main lobe. As predicted, the time domain signal shows minimal ringing after 4.3 µs, and the corresponding FFT shows no significant sharp resonances around the operational frequency range. Although the third generation annular array design is more narrowband in comparison to the second generation, the 30 dB ring down time is reduced by ~ 0.3 µs. Further imaging with such devices should be performed for true comparison purposes.

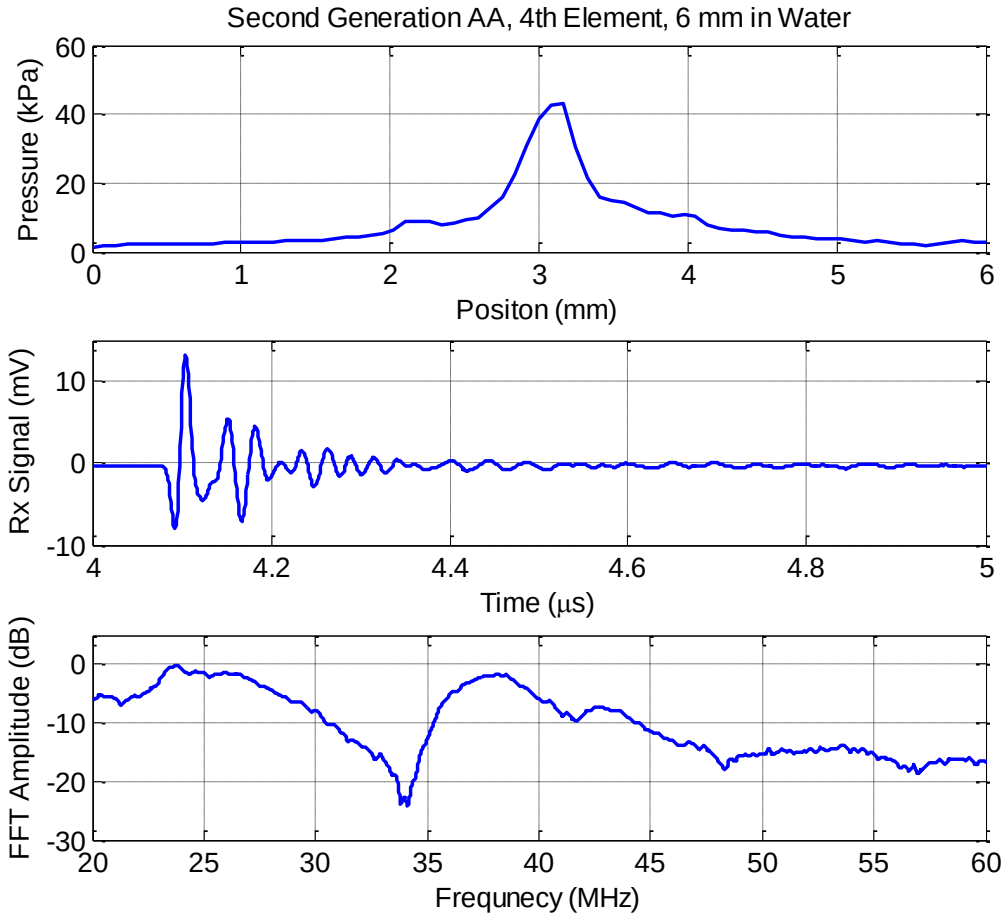


Figure 116. Annular Array, second generation radiation pattern at 6 mm, received hydrophone signal, and FFT of the time domain signal.

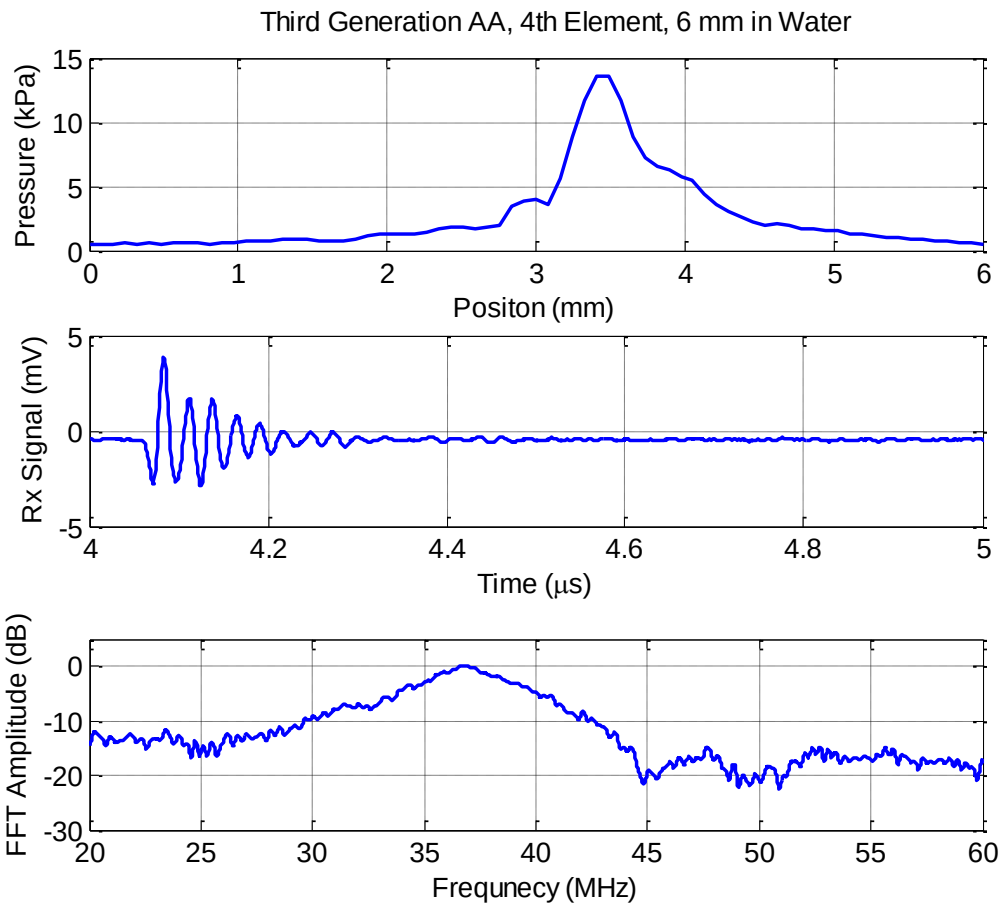


Figure 117. Annular Array, third generation radiation pattern at 6 mm, received hydrophone signal, and FFT of the time domain signal.

6.7. Summary

For side-looking IVUS applications, eight element annular ring arrays with a 420 μm radius have been fabricated and tested. For dynamic focusing applications, it was desired to fabricate arrays with equal area elements for unit time delays. The first generation of annular ring arrays did not have equal areas and although imaging was performed with focusing, it was found that the SNR for different ring combinations deviated by more than 10 dB due to the deviation in active area. FEA simulation also indicated significant acoustic cross talk between elements, simulated to be around -13 dB.

The second generation annular-ring array was designed with equal area ring elements and varied radial periodicity in an attempt to reduce acoustic crosstalk and address the SNR deviation. However, further 3D simulation using the BEM showed variation in the frequency response for each of the ring elements. It was observed that undesired mode shapes occurred at specific frequencies over the 20 MHz - 60MHz band of operation, reducing the average displacement CMUT element.

In the third generation of annular array design, the membrane shape was modified to a square design, 20 μm x 20 μm to minimize higher order mode shapes. Simulations indicated reduced acoustic cross-talk and with varied array placement, the cross-talk was calculated to be -22 dB over the 20 MHz – 60 MHz band. Additionally, the frequency response did not contain sharp resonances as predicted by simulation.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

The objective of this research is to develop the fabrication processes for monolithic integration of CMUTs with custom CMOS electronics as well as to improve the CMUT fabrication design space to allow for reduced isolation layers and vacuum gap. These processes are developed within the context of IVUS imaging arrays which include dual-ring arrays for forward-looking volumetric imaging in coronary arteries and annular-ring arrays with dynamic focusing capabilities for side-looking cross-sectional imaging applications. Both are designed for integration into an IVUS catheter 1-2 mm in diameter.

7.2. Contributions

7.2.1. CMUT-CMOS Integration Processing

Monolithic integration of CMUTs with custom CMOS electronics, has been developed and realized thought the use of top side connections through sloped sidewall vias less than 5 μm in diameter, allowing for simplified integration with only one additional masking layer for the CMUT fabrication, Figure 43. For the smaller elements associated with forward-looking dual-ring array it was shown experimentally that the detection is limited dominantly by thermomechanical noise of the CMUT, to 3 mPa/√Hz with this CMUT-on-CMOS integration scheme. [106]

The second generation of CMOS electronics has been fabricated with both transmit and receive electronics allowing for complete transducer integration reducing the

overall cable count to 13 as shown in Figure 118 which is a specific objective attainable through the developed fabrication processes. Integrated CMUT arrays with the CMOS electronics have generated 3D images in a test setup, demonstrating the real time imaging capabilities of the system, Figure 80.

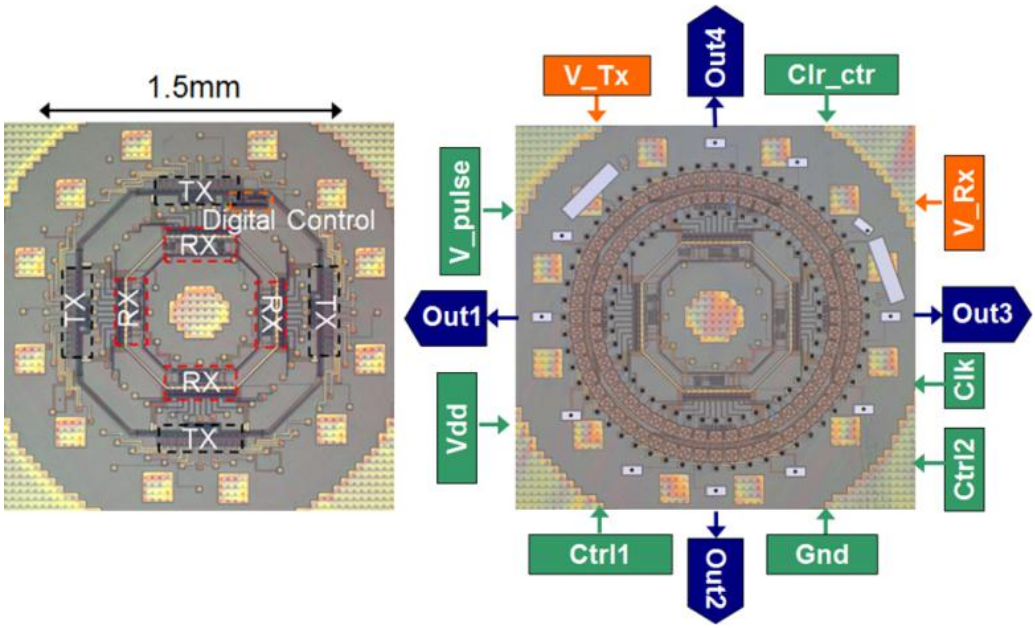


Figure 118. CMOS electronics for a 1.4 mm diameter FL-IVUS array (left) and the same silicon array with CMUTs fabricated above electronics with 13 electrical connections (right).

Additionally, catheter integration technology, flex-tape circuits and through silicon vias, have been tested in conjunction with the CMUT-on-CMOS processing. Etching of the silicon substrate over regions specifically designed to be free of CMOS electronics has allowed for the fabrication of circular doughnuts as well as slits for the flex tape to pass through. Arrays with flex-tape connections to the topside, Figure 119-left, have also been shown to be functional and capable of 3D imaging as shown by the image of a suspended wire target, Figure 119-right.

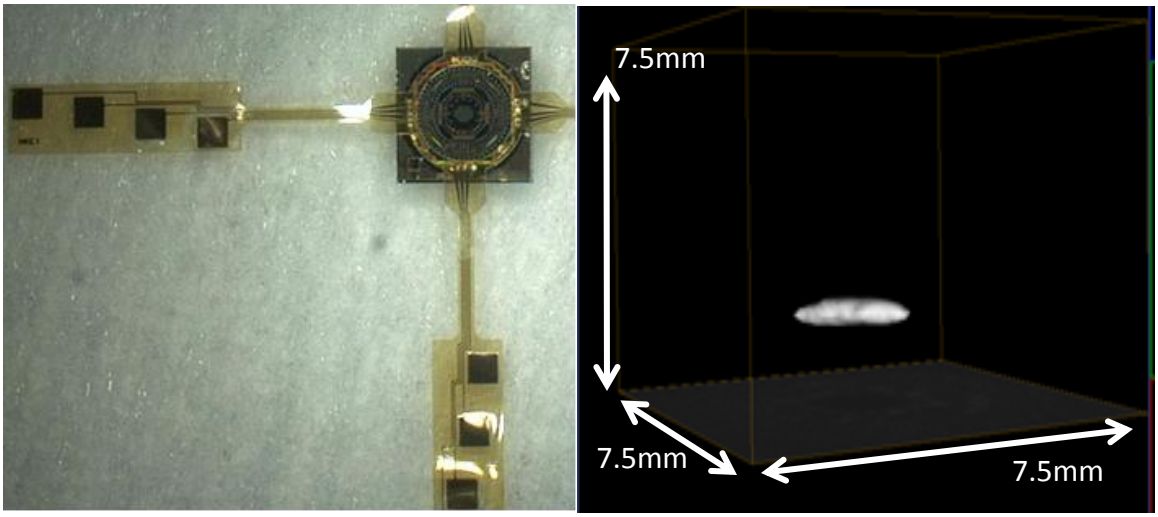


Figure 119. Flex tape integrated via top side connection (left) and reconstructed image of a 0.5 mm wire target 3.5 mm above the array with a 40 dB dynamic range (right).

Through silicon vias have also been fabricated in the CMOS substrates prior to the CMUT addition by Mr. James Yang with successful CMOS electronics testing showing functional electronics and electrical isolation up to 200 V DC. This will allow for future flex tape integration from the backside of the doughnut array to prevent interference with the topside CMUT array which will be important for the smaller IVUS catheters less than 1 mm in diameter, Figure 51.

Relevant publications with further specific details from the CMUT-on-CMOS fabrication development presented include [106, 108, 114, 115]

7.2.2. Optimization of CMUT Processing

To reduce the operational voltage of the CMUTs and to increase the transmit pressure with lower voltage actuation drive signals, it was desired to reduce the vacuum gap and isolation silicon nitride. To accomplish this, the materials used for the top, bottom, and sacrificial layers were investigated.

A process flow was developed using chromium metal for all three layers which allowed for a reduction in the silicon nitride isolation from the reduced surface roughness

previously associated with the aluminum hillock formation. Additionally, copper was implemented for the sacrificial layer in conjunction with chromium and aluminum for the bottom and top electrode layers respectively, Figure 30. With this process it was possible to completely eliminate one silicon nitride isolation layer allowing for a reduction from 100 nm vacuum gap and 300 nm of silicon nitride isolation to 45 nm vacuum gap and 120 nm of silicon nitride isolation allowing for a reduction in collapse voltage from 88 V to 45 V for a dual-ring array test element. This is significant given the current 25 V pulse limitation.

Additionally, the release of the copper layer using dilute APS-100 was found to be extremely selective against the chromium and aluminum layers allowing for improved fabrication reliability previously associated with the misalignment of the sacrificial release hole as well as seepage through pinholes in the silicon nitride isolation, Figure 33.

7.2.3. Improved Modeling

As part of the array development process, it was desired to accurately simulate CMUTs in array configurations, but FEA was found to be computationally expensive. Therefore, the Boundary Element Method was investigated which was successfully implemented, modeling CMUT membranes based on thin plate approximations.

A method to generate an alternate stiffness matrix was developed utilizing static FEA analysis to address the limitations associated with the thin plate approximation, low aspect ratio membranes, varied cross-sectional geometry, and varied boundary conditions, Figure 57. Test cases were shown to be in agreement with FEA in a computationally less expensive manner.

The larger signal expansion was also summarized, which uses arbitrary voltage drive signals as the input with pressure in the field as the output. Since, the SIMULINK model blocks are pre-calculated for a given array geometry, the transient SIMULINK model was shown to takes less than a second to run.

This BEM model was used to simulate segments of annular array designs for acoustic cross talk reduction and the larger signal model was used for dual-ring test arrays for transmit optimization, Figure 61.

Publications describing the model developed in this dissertation along with large signal capabilities can be found in [104, 116, 117].

7.2.4. Forward-Looking Dual-Ring Array

For forward-looking IVUS, the dual-ring array was developed and successfully integrated with custom CMOS electronics with a total of 13 connections meeting the criteria for catheter integration, Figure 118. Current designs for 10 MHz and 20 MHz with outer diameters of 2 mm and 1.4 mm include separate bottom electrodes for the Tx and Rx elements.

Imaging experiments showed 20 dB SNR from A-scan data and volumetric images were achieved with a 40 dB dynamic range 1 cm into tissue. These are the first images produced with a dual-ring CMUT-on-CMOS array with limited cable count, demonstrating the feasibility of CTO imaging meeting the design goal.

Based on the current 25 V pulse generation with the CMOS fabrication, test array were fabricated with reduced vacuum gap and isolation. For the two fabricated samples it was shown that the transmit pressure could be increased by 7.9 dB and the receive sensitivity by 2.9 dB with a reduction in the bias voltage from 80 V to 40 V using a 25 V pulse. Simulation was shown to be in agreement with experimental results with full gap swing achieved, and for the low voltage device, the maxim pressure was found to be 230 kPa at 2.2 mm in oil with an associated surface pressure in excess of 8 MPa, meeting the design criteria, Figure 82. Experimental characterization showed that the transmit pressure could be improved by a further 2.9 dB if the Tx elements were fabricated with full electrode coverage, Figure 85. Therefore it should be possible to increase the SNR of

the forward-looking dual-ring array by 14.3 dB though fabrication and layout modification.

Relevant publications from the dual-ring array development, fabrication, and imaging results include [29, 54, 118-120]

7.2.5. Side-Looking Annular-Ring Array

Annular ring arrays were successfully fabricated and tested with eight elements with a 420 µm radius, suitable for side-looking applications over the 20 MHz to 60 MHz band. First generation arrays did not have equal area elements as desired for unit time delay focusing. It was experimentally determined that the SNR from pulse-echo combinations deviated by more than 10 dB from the deviation in ring element areas. FEA simulations indicated -13 dB of acoustic separation between elements over the 20 MHz to 60 MHz band.

For the second generation design, the equal area issue was addressed, and the CMUT membranes were varied to reduce cross talk associated with the radial periodicity of the first design. Simulations of select array segments using the developed model in CHAPTER 4 indicated a reduction in average displacement of the active ring from undesirable mode shapes at specific frequencies, adversely affecting the overall frequency response.

In the third generation design, the CMUT membrane shape was simulated and modified to minimize higher order mode shapes. A square design, 20µm x 20µm was found to be suitable, and as before the array placement was varied to reduce radial periodicity. Simulations indicated reduced acoustic cross-talk -22 dB over the 20 MHz – 60 MHz band to meet the separation criteria, Figure 115. Experimental measurements indicate surface pressure in excess of 1 MPa, meeting the previously identified performance criteria.

For the dynamic receive mode, custom electronics have also been developed and tested. Utilizing a single voltage control signal, unit time delays were achieved over the 1-10 ns range as desired.

Publications from the annular-ring array development and fabrication along with further details on the array designs include [110, 112, 121, 122]

7.3. Future Work

The research presented in this dissertation establishes a solid processing method for producing CMUT's with minimal isolation and reduced vacuum gap as well as the ability to monolithically integrate CMUT's on CMOS electronics. Further modeling of the CMUT arrays for the dual-ring array applications should be performed to determine the optimal bias and pulse conditions for maximum transmit pressure. Additionally, current designs which utilize a uniform electrode size for both Tx and Rx elements should be modified to increase the electrode coverage for Tx elements and possibly reduce the electrode coverage for Rx elements.

Initial results from the through silicon via addition are promising, and future samples should be fabricated with fully functional CMUT arrays for proof of concept. Additional custom CMOS fabrication can be modified to include open regions specifically designated for TSV addition. Utilizing the CMOS electronics layers, it should be possible to assist in the TSV fabrication through the addition of a metal framework to act as a masking layer during the critical etching process of the silicon dioxide top layer.

Based on the successful annular array fabrication, arrays should be monolithically integrated with the custom CMOS delay circuitry. Combined with the improved processing capabilities, the vacuum gap can be reduced for a decrease in the DC bias required for operation. As with the dual-ring array electronics, TSV's should be included in the delay electronics for back side flex tape connection. Designs that include mass-

loading or additional stiffening members should be investigated to increase the bandwidth and/or suppress higher order membrane modes that adversely affect the frequency response.

Further fabrication optimization can be explored for performance improvement and robust fabrication. Possible improvements include the use of atomic layer deposition for conformal isolation layers with relative dielectric constants greater than that of the current PECVD. Also, the use of low temperature PECVD silicon nitride, 100 °C, can be investigated to avoid delamination issues.

APPENDIX A LOW TEMPERATURE CMUT FABRICATION

CMUT technology is based on well-defined micromachining technology used to achieve batch fabrication as shown in

Figure 120. The following is a summary of the processes and equipment used for CMUT fabrication which is also compatible with monolithic CMOS integration in terms of the processing and equipment.

When processing CMUTs on bare, doped silicon wafers, a dielectric layer of silicon oxide is first deposited through plasma enhanced chemical vapor deposition, PECVD, to form an isolation layer (a). All PECVD depositions for CMUT fabrication occur at 250 °C, compatible with professionally manufactured CMOS electronics which can be substituted for the bare wafers as the processing substrate. Five masks for lithography are then used in the processing of standard CMUTs which use wire bonding for electrical connections. These masks define the surface areas of the CMUT membranes and their locations, with deposited layer thickness determining the CMUT cross-section. A DC metal sputtering tool is used to deposit conformal metal layers, the first being the bottom electrode, aluminum with a thin chromium smoothing layer (b). Through lithography, the bottom electrode is masked, and the excess metal is removed via a wet etch as is the case with the sacrificial and top electrode metal layers. Silicon nitride is use as the bulk material for its material properties, namely stiffness, density, and low-stress. Following the bottom electrode, a thin layer of silicon nitrite is deposited via PECVD to protect the bottom electrode during the release process. A layer of chromium is then deposited and patterned to act as the sacrificial layer (c). Silicon nitride is again deposited, (d), to protect the following top electrode (e). Before the release, the membrane is built up with more silicon nitride, (f), to provide structural support to

prevent stiction during the release in the wet chrome etch. A reactive ion etch, RIE, tool drills holes through the silicon nitride down to the chromium sacrificial layer to allow access for the wet etchant (g). After the membranes are completely released, (h), the final silicon nitride is deposited to build up the membrane and fill the etch holes preserving the vacuum in the gap (i). In the final process step, the RIE removes any silicon nitride material above the top and bottom electrode bond pads to allow for electrical connection (j).

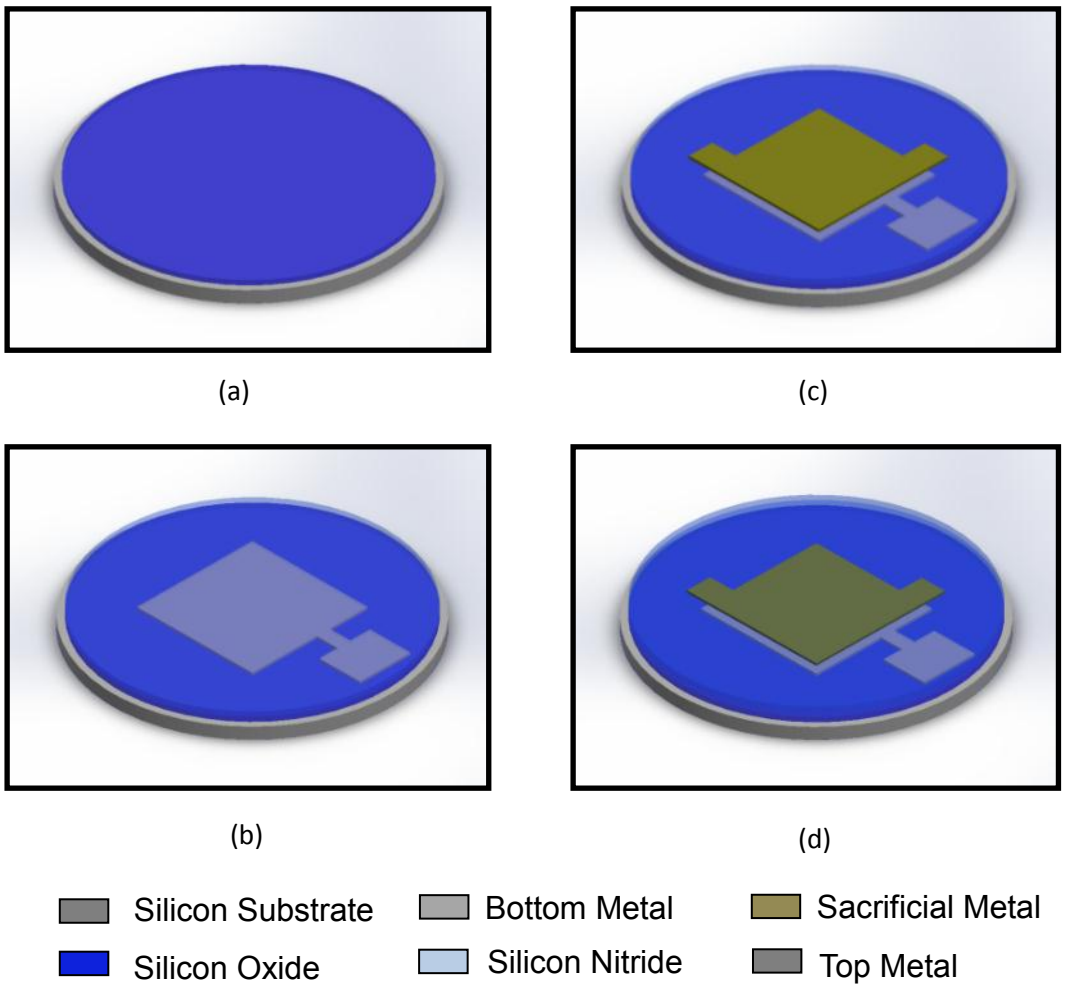
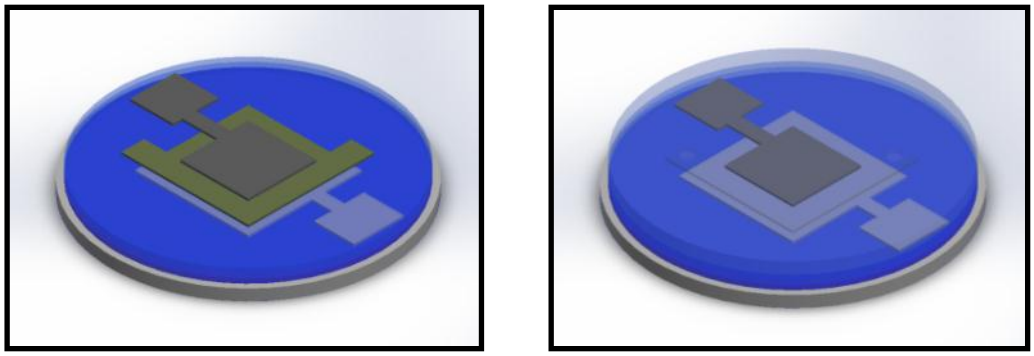
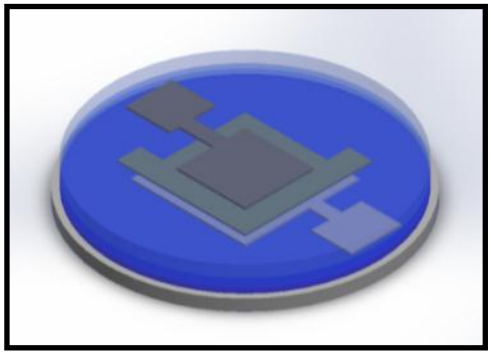


Figure 120. CMUT fabrication process steps.

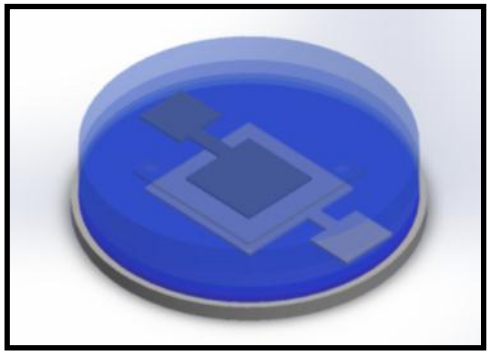


(e)

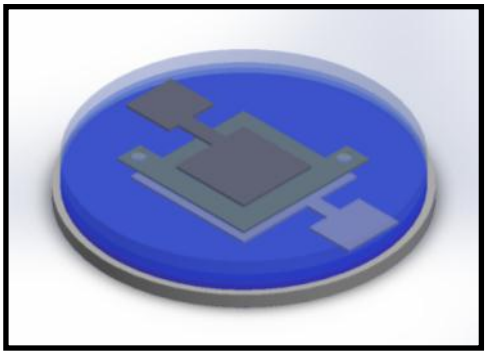
(h)



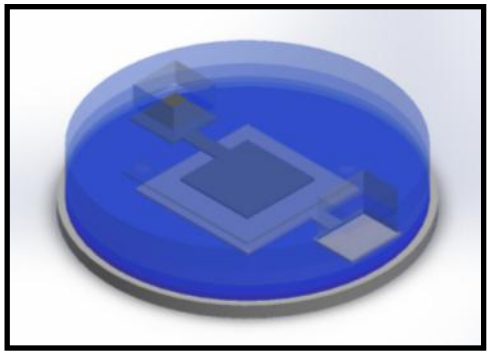
(f)



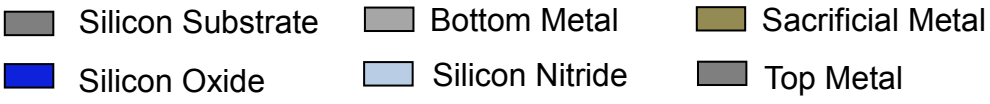
(i)



(g)



(j)


Silicon Substrate
Bottom Metal
Sacrificial Metal
Silicon Oxide
Silicon Nitride
Top Metal

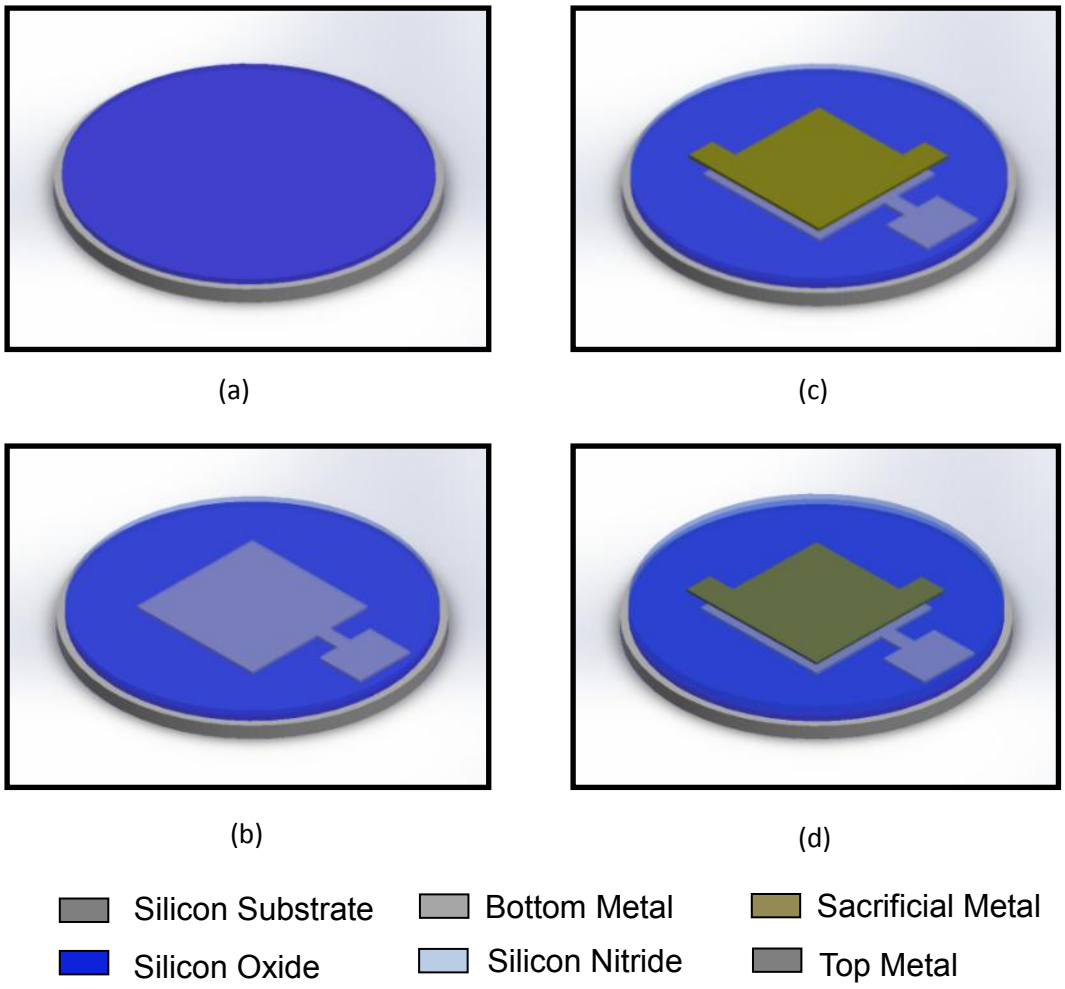


Figure 120 Continued

APPENDIX B COPPER SACRIFICIAL CMUT FABRICATION

The following details describe how to fabricate CMUT's with minimal electrical isolation, one layer 100 nm, and a vacuum gap 50 nm thick. The same 5 masks are used as in standard CMUT fabrication, but the order is modified to allow for protection of the sacrificial material, copper, while the bottom electrode, chromium, is etched.

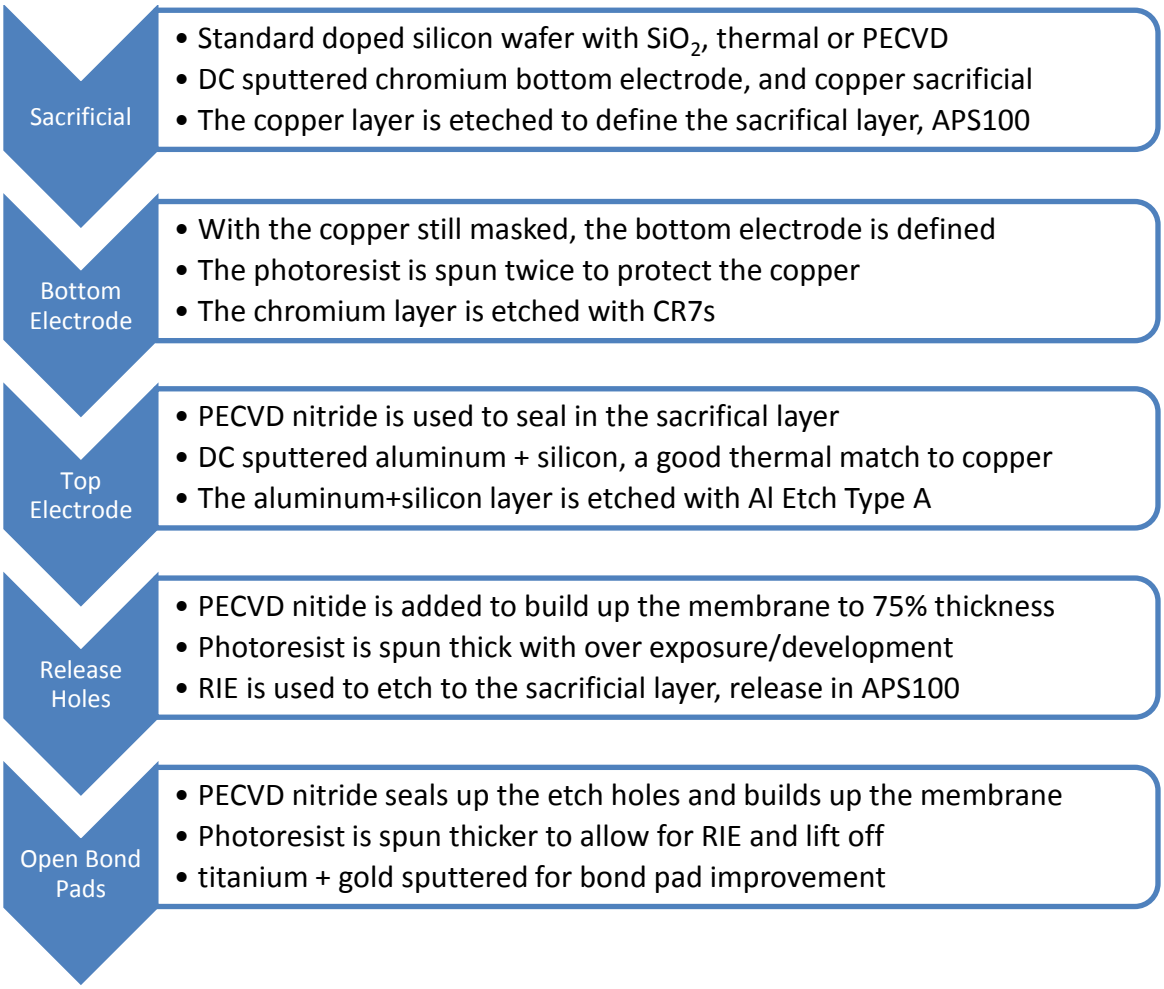


Figure 121. Process flow for the use of copper as a sacrificial layer.

Sample Preparation:

With standard 4 in diameter doped silicon wafers as the substrate, it is possible to use the substrate as the common electrode, but to reduce the parasitic capacitance it is necessary to electrically passivate the surface. High temperature, 1200 °C, thermal oxidation is desirable for its low surface roughness, but is not compatible with CMOS electronics. PECVD silicon dioxide or silicon nitride, on the order of 1 to 3 μm, is also possible and with a deposition temperature of 250 °C, CMOS compatible. PECVD oxide is typically used for its rapid deposition rate, ~ 500 Å /min.

Metal Deposition 1:

The first metal deposition is a combination of chromium and then copper to form the bottom electrode and copper sacrificial layers. The chromium acts as an adhesion layer for the copper, and both are deposited via DC metal sputtering for conformal coverage in the same run. As such, there is no isolation between the bottom electrode and the sacrificial layer.

Sacrificial Definition:

The positive photoresist Shipley 1813 is spun at 3000 RPM for 60 s with a 500 RPS ramp up. It is cured in a 100 °C oven for 5 minutes. This bakes the photoresist from the outside in preventing excessive residue during subsequent removal. Additionally, baking helps to cure the photoresist on the top surface so that the wafer won't stick to the mask during alignment. After baking the wafer is allowed to cool for 3-5 minutes before insertion into the Karl Suss MA6 mask aligner. The dose is set to 200 mJ/cm^2. Development in MF319 requires approximately 60 s with a gentle sloshing forward/backward and left/right once every 15 s. To ensure uniform sloshing, the MF319 is poured to a depth of 1 cm in a 5 cm deep plastic container.

The etch for this process is APS-100 copper etch mixed with water in a ratio of 1:30 as the listed etch rate is 80 Å/s which is too fast for the thin sacrificial layer. APS-100 is a mix of primarily ammonium peroxydisulfate 15 - 20% with water 80 - 85% with a pH <1. During the copper etch, gas bubbles, hydrogen, form on the surface of the wafer and prevent the APS-100/water mix from attacking the underlying copper. This was found to be especially problematic between features with less than 10 µm spacing. Therefore immediately after the wafer is submerged in the etchant, rapid tapping is performed on the sides of the container to promote the release of bubbles from the surface. Sloshing from side to side was found to be insufficient and tended to produce results where one direction along the wafer was over etched.

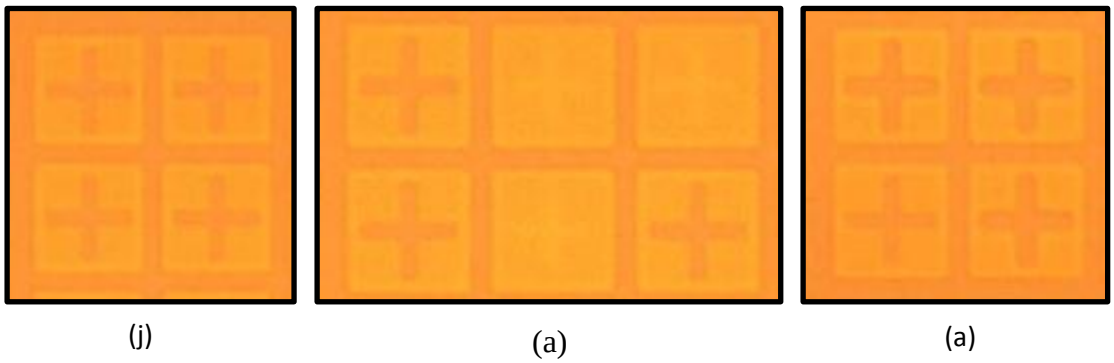


Figure 122.The sacrificial layer in (a) is properly etched with clean, sharp definition. The sacrificial layer in the center of (b) shows failed sacrificial etching from the formation of bubbles on the surface. The sacrificial layer on the right side of (c) shows over etching from excessive sloshing.

Bottom Electrode Definition:

Without removing the photoresist from the sacrificial layer, Shipley 1813 was spun on at 3000 RPM for 60 s with a 500 RPS ramp up which did not uniformly coat the sample. Without removal from the spin coater, Shipley 1813 was spun a second time for a more conformal coverage. The sample was then baked for 5 minutes at 100 °C. After baking the wafer is allowed to cool for 3-5 minutes before insertion into the MA6 mask

aligner. The dose is set to 300 mJ/cm^2 as the resist is thicker than normal and the feature sizes for the bottom electrode are not as critical. The wet etch for the chromium, CR7S, is not diluted and is very aggressive towards copper. Therefore it is critical that the photoresist for the bottom electrode completely cover the sacrificial layer.

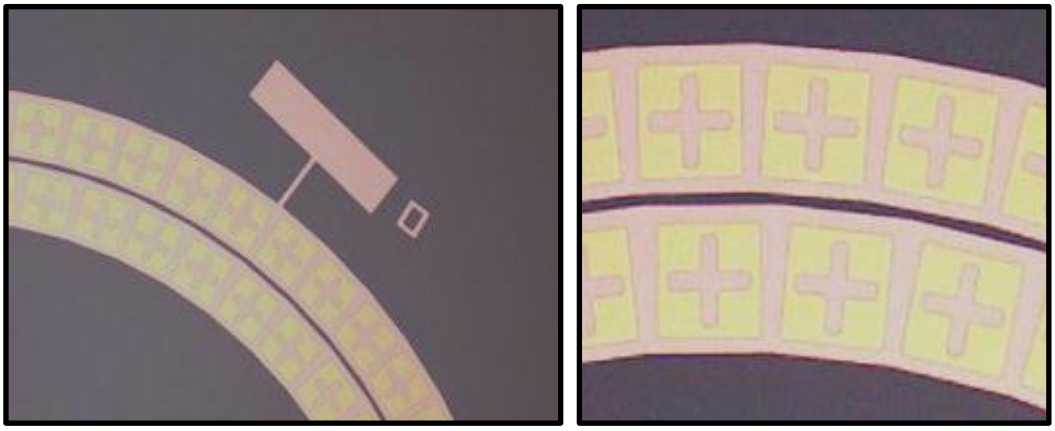


Figure 123.The chromium bottom electrode is larger than the sacrificial copper as a protection measure against the CR7S. For this device, the distance in the radial direction from the sacrificial layer to the bottom electrode is approximately 7 μm.

Cleaning:

After the sacrificial and bottom definition, the wafer or CMOS sample is rinsed with acetone to remove the bulk of the photoresist. It is then soaked in acetone for 5 minutes. The sample can also be placed in an ultrasonic cleaner in the acetone for complete removal of residue. The photoresist stripper 1165, is a base and doesn't attack the two metal layers. It can be used at room temperature as the photoresist did not exceed 100 °C during the baking cycles. After the acetone batch, it is rinsed with methanol, isopropyl alcohol, and rinsed with DI water.

Isolation:

PECVD or ICP PECVD silicon nitride is added to the surface for isolation. This layer will determine the maximum electric field strength that can be applied before electrical shorting between the top and bottom electrode. It also provides a protective layer for the copper sacrificial layer when the top electrode is etched. As such, the pinhole effects in the silicon nitride are extremely detrimental as the sacrificial layer will be accidentally etched if the metal etch for the top electrode seeps through. Typically isolation is on the order of 100 - 300 nm and can be based on two factors. First the dielectric strength is on the order of 800 V/μm and with a desired collapse voltage from simulation, the thickness can be approximated.

Top Electrode Deposition and Definition:

The top electrode is made of Aluminum and Silicon on the order of 100 nm and is deposited with the conformal DC sputterer. The top electrode was first fabricated with Chromium to match the bottom electrode stiction layer. However, it was found that the Chromium layer would delaminate during subsequent processing. The Aluminum/Silicon mix offers better adhesion to the silicon nitride isolation and is a better match to the underlying Copper layer in terms of thermal expansion.

Shipley 1813 is used for the masking of the top electrode and is processed similar to the bottom electrode. The wet etch used is Al Etch Type A, which at room temperature has a viscosity similar to Maple syrup. Often this etch is heated, but in its more viscous room temperature form, the undercut is minimized. This container is lightly agitated during the etch process. Additionally, it is often possible to visualize streaks of Aluminum on the wafer in random regions. An extended etch will often remove such streaks without detriment to the masked regions. The sample is cleaned as before.

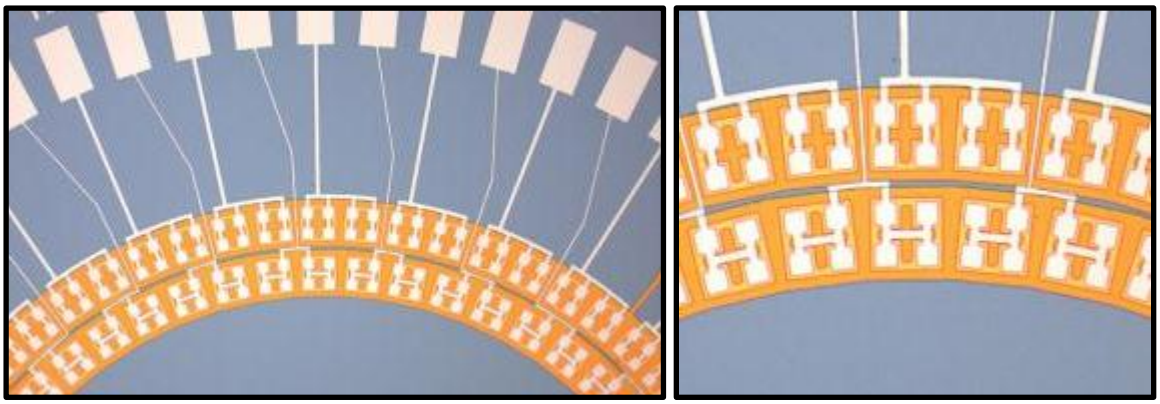


Figure 124.The top electrode is clearly defined with no degradation of the underlying sacrificial copper layer. The corners of the membranes are slightly rounded from the over etching to remove streaking.

Membrane Build Up:

With the three metal layers defining the CMUT areas, the membrane can now be built up. Silicon nitride is the material of choice for its mechanical properties and ease of etching, twice that of PECVD oxide with RIE. Typical CMUT membrane thicknesses are from 2 - 4 µm depending up the design requirements. During the release process, the membrane needs to be thick enough to prevent collapse from surface tension etc. Therefore, for a 2 µm thick membrane, 1.5 µm can be deposited before release. Nitride is deposited in multiple runs based on the cycling capability of the tool used.

Sacrificial Etch Holes:

For the definition of the vacuum gap, the copper sacrificial layer needs to be removed via a wet etch. Holes to reach the copper need to be defined that drill through the deposited membrane nitride. Shipley 1827 is spun at 3000RPM with a 500 RPS ramp up and is cured at 100 °C in the oven for 5 minutes. It is allowed to cool for 5 - 10 minutes before insertion in to the mask aligner. The dose was set to ~ 350 mJ/cm^2 as the feature sizes are on the order of 3 - 5 µm. Development in MF-319 for 120 s ensures that

the developing removes all of the material in the holes with sloshing every 30 s. The RIE recipe with argon drills the holes to the copper layer with vertical side walls. The copper acts as an etch stop so it is possible to over etch without detrimental effects. The etch rate for the RIE is also reduced as compared to bulk etching from the small feature sizes. Before removal of the resist, the sample is placed in the wet release etch of APS100 and water in a ratio of 1:15 for 15 minutes. It is inspected to verify that the RIE etched completely to the sacrificial layer. If necessary, the sample can be etched further in the RIE. If the Copper layer is seen to be etching, then the photoresist can be removed and the sample placed in the APS100/water mix for 2-10 hours as necessary. It is important to note that APS100 does not etch either chromium or aluminum in during the release process and any small pinholes in the isolation nitride are no longer an issue.

Release:

The release process is very important to prevent collapse of the membrane and to minimize contamination of the silicon nitride with metal etch. Previous samples with minimal cleaning, exhibited charging effects. The sample is removed from metal etch and rinsed with DI water for 5 minutes. As an alternative to the multiple baths of water, it is also possible to use a continuous water rinse for 10-15 minutes. Following it is placed in sample containers of DI water changed every 5 minutes for 20 minutes. The sample is then moved to isopropyl alcohol containers to displace the water. The surface tension of water is 72 mN/m as compared to 22 mN/m for isopropyl alcohol. At 100 °C the vapor pressure of water is 101 kPa as compared to 200 kPa for isopropyl alcohol. The wafer is allowed to soak for the last bath in the isopropyl alcohol for 5-12 hrs. The oven is set between 80 °C and 100 °C. The sample is removed from the final bath and without drying, the sample immediately placed in the oven. If the temperature of the oven is too high, the isopropyl alcohol will vaporize rapidly and the membranes will bubble/explode.

Final Membrane Deposition and Bond pad Opening:

The final membrane material is deposited to seal the release holes used for the release and to provide the remaining structural material. After completion, the bond pad regions need to be opened for external connections. Shipley 1827 is spun at 2000 RPM with a 500 RPS ramp up. The bake at 100 °C for 5 minutes is still sufficient for the thicker photo resist. Again, it is allowed to cool before exposure, ~500 mJ/cm^2. Development in MF319 needs to be longer, 120 – 180 s, to ensure proper opening. The RIE is then used to open the bond pads and optically measured using a spectroscopic reflectometer to ensure complete nitride removal.

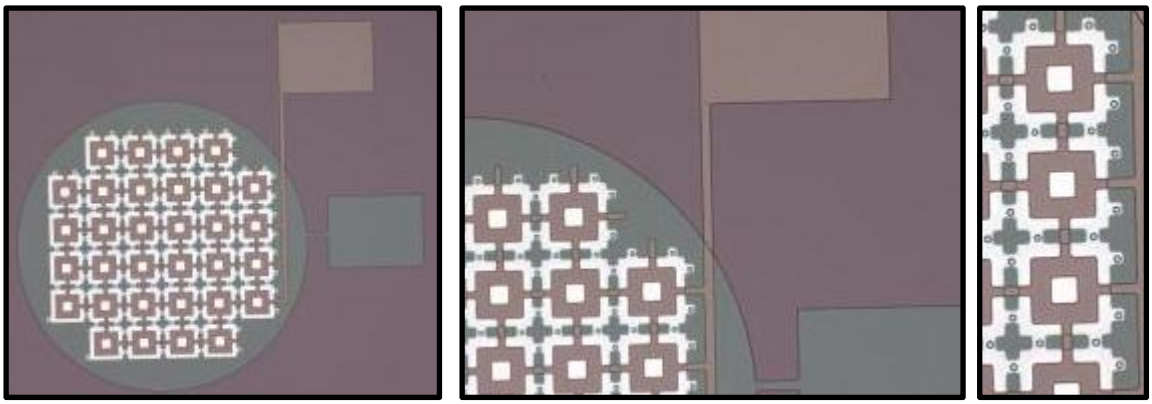


Figure 125.The copper sacrificial layer is completely removed and the etch hole features are still visible after membrane sealing. There is no pealing of the top electrode, and profilometer scans show no collapse from the release process which can be problematic with lower frequency arrays such as the 6 MHz device above, 50 µm wide membrane.

Bond Pad Thickening:

If the metal layers used for the bottom and top electrode are less than 100 nm, it may be beneficial to add additional material for the wire bonding process or flexible interconnect assembly. With the bond pads still masked from the RIE opening, a lift off process may be utilized with the DC sputterer. An adhesion layer of Titanium, 10 - 20 nm, is deposited followed by 2000 - 3000 nm of Gold. The wafer is placed in an acetone

bath for 1hr. If necessary, ultrasonic agitation may be required to assist in the lift off process. A second acetone bath is also used for a final cleaning.

APPENDIX C ANSYS SAMPLE CODE

```
finish
/clear,nostart

/filename,aa1,1
this if for looping the entire program
!*do,iti,0,0,1 !do iti from 0 to .2 in 0.1 increments
!parsav,scalar,iti        ! save the variable iti

/clear,nostart
/filename,aa1,1

!parres,new,iti           ! reopen the variable iti

/prep7

!Gemetry constants uMKSV units
!numbers are in um
!*************************************************

beth=0.15       !Bottom Electrode
biso=0.25       !Bottom Isololation
sac=0.12        !Sacrifical Layer
tiso=0.25       !Top Isolation
teth=0.15       !Top electrode
tnit=2.7   !+iti*0.1              !Nitride thickness above Top Electrode

wm=18                   !Width of membrane
pitch=20        !pitch
we=13.5                 !Width of Top Electrode

PL=5   !+iti*5          !parylene Thickness
!Initial Offset from center(axial)
offset=11
!silicon width
siw=700

!silicon height
sih=700
!Number to array
arn=21
```

```
!initial fluid thickness
FT=500                  !approximate look at the radius issue with 129

!*************************************************
minf=5 000 000          !start frequency of sweep (Hz)
maxf=80 000 000         !end of frequency of sweep (Hz)
nsteps=2        !number of solution steps in between
f_min=minf
f_max=maxf

c_fluid=1500 000 000            !speed of sound in the fluid, material 5
lamda_max=c_fluid/minf                  !max wavelength in range of sweep
lamda_min=c_fluid/maxf
radius=lamda_max                !radius of fluid space
*set,d_fluid,1000/(1 000 000 000 000 000 000)

neplamda=5                      !this is the number of elements per wavelength.


Create the Geometry
!*************************************************

!RECTNG, X1, X2, Y1, Y2

!Silicon
rectng,0,siw,0,-sih

!bottom Electode
rectng,0,pitch*(arn+2),0,beth

!Bottom Isolation
rectng,0,pitch*(arn+2),beth,beth+biso

!Silicon Nitride bulk
rectng,0,pitch*(arn+2),beth+biso,beth+biso+tiso+teth+tnit

!Sacrifical Layer
rectng,offset-wm/2,offset+wm/2,beth+biso,beth+biso+sac

!Top Electrode
rectng,offset-we/2,offset+we/2,beth+biso+sac+tiso,beth+biso+sac+tiso+teth

agen,arn,5,,,pitch,0,0,0
agen,arn,6,,,pitch,0,0,0
asel,s,area,,5,46
```

```
asel,a,area,,4
!generate the sin area
asba,4,all,,delete,keep

allsel,all
aglue,all

!*****************************************************************

!Silicon Nitride bulk
rectng,0,pitch*(arn+2),beth+biso+tiso+teth+tnit,beth+biso+tiso+teth+tnit+PL

!set the fluid layer
fb=1.0*siw
R1=sqrt(fb*fb+siw*siw)
FT=R1-fb

k,7001,0,FT,0

!larc,7001,3,1,5*FT+sih
larc,7001,3,1,R1
l,7001,13

!ldiv,3,1-pitch*(arn+1)/siw

allsel,all
aglue,all

lsel,s,line,,208,209
lsel,a,line,,8
lsel,a,line,,6
lsel,a,line,,6
lsel,a,line,,14
lsel,a,line,,5
lsel,a,line,,10,11
al,all

allsel,all
aglue,all

!*************************************************************
!break the sacrifical lines to allow for pressure application
!divided into the 21 rings

pct=we/wm
rs=.5*(1-pct)
```

```
ls=pct/(pct+rs)
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!   first 5
ldiv,19,rs
ldiv,15,ls

ldiv,27,rs
ldiv,185,ls

ldiv,31,rs
ldiv,213,ls

ldiv,35,rs
ldiv,215,ls

ldiv,39,rs
ldiv,217,ls

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!   6 to 10

ldiv,43,rs
ldiv,219,ls

ldiv,47,rs
ldiv,221,ls

ldiv,51,rs
ldiv,223,ls

ldiv,55,rs
ldiv,225,ls

ldiv,59,rs
ldiv,227,ls

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!   11 to 15

ldiv,63,rs
ldiv,229,ls

ldiv,67,rs
ldiv,231,ls

ldiv,71,rs
ldiv,233,ls

ldiv,75,rs
```

```
ldiv,235,ls

ldiv,79,rs
ldiv,237,ls

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!   16 to 21

ldiv,83,rs
ldiv,239,ls

ldiv,87,rs
ldiv,241,ls

ldiv,91,rs
ldiv,243,ls

ldiv,95,rs
ldiv,245,ls

ldiv,99,rs
ldiv,247,ls

ldiv,103,rs
ldiv,249,ls


!*************************************************

!Set the material poperties use uMKSV
!! #1  material properties of SiN!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
et,1,183                    !2D 8-node or 6 node struct. solid

mp,ex,1,110000              !Young's modulus of structural material 1 (membrane)
mp,prxy,1,.22               !minor poison's ratio of structural material 1
mp,dens,1,2200/1 000 000 000 000 000 000 000  !density of structural material 1
!mp,pery,1,6.7*8.85e-12*e6  !electrical permutivity
!mp,perx,1,6.7*8.85e-12*e6  !electrical permutivity

!! #2  Material properties of Si!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

mp,ex,2,150000              !Young's modulus of structural material 1 (silcion
substrate)
mp,prxy,2,.28               !major poison's ratio of structural material 1
mp,dens,2,2329/1 000 000 000 000 000 000 000          !density of structural material 1

!! #3  material properties of aluminum!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
```

```
mp,ex,3,70000          !Young's modulus of structural material 3 (electrode)
mp,dens,3,2700/1 000 000 000 000 000 000          !density of structural material 3
mp,prxy,3,.35                    !major poison's ratio of structural material 3

!! #4  material properties of parylene c!!!!!!!!!!!!!!!!!!!!!!!!!!!!

!mp,ex,10,1391.6               !Young's modulus of structural material 3 (electrode)
!mp,dens,10,1020/1 000 000 000 000 000 000                !density of structural material
3
!mp,prxy,10,.49                  !major poison's ratio of structural material 3
et,10,79
!mp,ex,10,2250 bulk modulus of water c^2rho

dRTV=1020*1e-18
cRTV=1080e6
mp,ex,10,cRTV*cRTV*dRTV
mp,dens,10,dRTV               !density of structural material 3
mp,damp,10,0
!zparylene=dparylene*cparylene
!Set the keyoption for axisymetry
!*************************************************
KEYOPT,1,3,1         !axisymetric keyoption for plane 183, keyoption 3 is set to 1
KEYOPT,2,3,1                 !axisymetric
KEYOPT,3,3,1                 !axisymetric
KEYOPT,4,3,1                 !axisymetric
kEYOPT,10,3,1                !axisymetric

!*************************************************
!!!!!!Acoustic elements!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
et,4,29          !2D acoustic element in contact with structure (interface)
keyopt,4,2,0    !DOF is ux,uy, and P (all 3 needed for interface elements)
keyopt,4,3,1    !planar option ( axisymetric)
r,4,20/1 000 000 000 000      !reference pressure is 20 uPa use the e-12 for the
conversion to uMKSV
et,5,29          !2D acoustic element not in contact with structure
keyopt,5,2,1    !DOF is P only
keyopt,5,3,1    !planar option ( axisymmetric)
et,6,129         !absorbing acoustic element (line element)
keyopt,6,3,1    !planar option ( axisymetric)
mp,dens,7,d_fluid               !density of material 7 (fluid)
mp,sonc,7,c_fluid       !speed of sound of material 5 (fluid)
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!Assign attibutes

!Fluid Region
```

```
asel,s,area,,3
aatt,7,5,5
!top and bottom electrodes
asel,s,area,,6
asel,a,area,,27,46
asel,a,area,,4
aatt,3,,1

!silicon nitride
asel,s,area,,2
asel,a,area,,49
aatt,1,,1

!block above the transducer rtv if selected
asel,s,area,,1
aatt,10,,10


!*************************************************************************
!mesh the areas, solids

asel,all
lesize,all,lamda_min/neplamda*.2

!lesize,all,0.2
!top and bottom electrodes
asel,s,area,,6
asel,a,area,,2
asel,a,area,,27,46
!asel,a,area,,4
asel,a,area,,49
asel,a,area,,1
mshape,0,2D             !set to quads
smartsize,2
amesh,all

asel,s,area,,3    !Mesh the fluid
aatt,7,5,5
aesize,all,lamda_min/neplamda*0.3
!asel,a,area,,1

mshape,0,2D             !set to quads
mopt,trans,1.5          !this to prevent rapid changes in elements
amesh,all

!!!!! CHANGE FLUID ELEMENT TYPE FOR THOSE TOUCHING STRUCTURE !!!
```

```
!silicon nitride
lsel,s,line,,8
lsel,a,line,,5
lsel,a,line,,14
lsel,a,line,,208,209
lsel,a,line,,6

!Optional rings
!lsel,s,line,,3
!lsel,a,line,,4
!lsel,a,line,,209
!lsel,a,line,,6

nsll,s,1          !Select nodes associated with lines
esln,s,0,all              !select elements attached to selected nodes
esel,r,type,,5            !select a subset of elements
emodif,all,type,4         !modify previously defined element
allsel,all

!!!!! FLAG FLUID / STRUCTURE INTERFACE NODES !!!!
!silicon nitride
lsel,s,line,,8
lsel,a,line,,5
lsel,a,line,,14
lsel,a,line,,208,209
lsel,a,line,,6

!Optional rings
!lsel,s,line,,3
!lsel,a,line,,4
!lsel,a,line,,209
!lsel,a,line,,6


nsll,s,1
esel,s,type,,4   !applying flag to nodes, but fluid elements should be selected too
sf,all,fsi,1       !speficies surface loades, fsi=fluid structure interface
allsel,all

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!! ADD ABSORBING ACOUSTIC ELEMENTS !!!!!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
!radius,xo, and yo of the center of the radius for absorbing boundary real constant 6
r,6,R1,0,-fb
lsel,s,line,,10
nsll,s,1
type,6            !Sets the element type attribute pointer
```

```
real,6          !Sets the element real constant set attribute pointer
mat,7
esurf
!esln,s,0,all          !select elements attached to selected nodes
!esel,r,type,,5        !select a subset of elements
!emodif,all,type,6     !modify previously defined element
allsel,all
finish
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
! RTV if selected
*do,iti,10,80,.25 !do iti from 0 to .2 in 0.1 increments
/prep7
frq=1e6*iti
nsteps=1
k=(2*3.14*frq)/cRTV
n=.95629
B=2.135e-4
alpha=B*exp(n*log(frq))*1e-6

zeta=alpha/(k)
mp,damp,10,zeta

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
/solu                  !enter solution processor

assopt,,front          !command uses matrix assembly method from version 5.7
antype,harmic,new      !select a new harmonic analysis
hropt,full             !use full solution option
hrout,on               !print the complex results as real and imaginary

!!!!! APPLY STRUCTURAL BCS AND LOADING !!!!!!
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!

lsel,s,line,,7
!lsel,a,line,,208

dl,all,,ux,0
dl,all,,uy,0
allsel,all

lsel,s,line,,11,12
lsel,a,line,,9
lsel,a,line,,207,,210,3
dl,all,symm,roty

!*************************************************************************
```

```
p_act=1                 !This is the pressure, really its 1E7*1e-6

                !1 5 rings for 1st element
lsel,s,line,,15
lsel,a,line,,185
lsel,a,line,,213,217,2
sfl,all,pres,p_act      !This is the application of pressure
allsel,all

!*****************************************************************************
****
harfrq,frq

!nsubst,nsteps          !number of substeps in frequency sweep
kbc,1                   !Ramped loading (seems arbitrary)
allsel,all
save,harcmut,db             !save the database before solving the model
solve
finish

!!!!!!!!!!!!! Use this go t0 grab the Displacement real and imaginary
*use,mac1\U_rmac.txt
*use,mac1\U_imac.txt
*use,mac1\U_rmac2.txt
*use,mac1\U_imac2.txt
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
*enddo


!!!!!!!!!!!!!U_rmac!!!!!!!!!! (separate code file)
/post1
*cfopen,U_real1e1,txt,,append
*do,step,1,nsteps,1     ! repeat for each frequency solved
set,1,step,,0               ! read real part of the results from the results file
path_division=441
path,press1,2,20,path_division
ppath,1,,0,beth+biso+sac+tiso,0
ppath,2,,440,beth+biso+sac+tiso,0
pdef,P1,U,Y
*do,k,1,path_division
PSEL,s,press1
*get,variable,PATH,0,ITEM,P1,pathpt,k
*vwrite,variable
(e24.18)
*enddo
*enddo
*cfclose
```

```
finish

!!!!!!!!!!!!!U_imac!!!!!!!!!! (separate code file)
/post1
*cfopen,U_imiginary1e1,txt,,append      !set the file to save the data
*do,step,1,nsteps,1       ! repeat for each frequency solved
set,1,step,,1               ! read the imaginary part of the results
path_division=441      !set the number of data points to collect
path,press1,2,20,path_division
ppath,1,,0,beth+biso+sac+tiso,0
ppath,2,,440,beth+biso+sac+tiso,0
pdef,P1,U,Y
*do,k,1,path_division
PSEL,s,press1
*get,variable,PATH,0,ITEM,P1,pathpt,k

*vwrite,variable
(e24.18)
*enddo
*enddo
*cfclose

finish
```

APPENDIX D COMSOL SAMPLE CODE FOR K MATRIX CALCULATION

```
%COMSOL CODE FOR K MATRIX CALCULATION IN MATLAB

%% Membrane dimensions and BEM mesh nodal spacing
Membrane_Xwidth = 20e-6;      %[um]
Membrane_Ywidth = 20e-6;      %[um]
Membrane_thick = 1e-6;        %[um]

NodesX = 21;              %Number of nodes in X direction
NodesY = 21;              %Number of nodes in X direction

dx=Membrane_Xwidth/(NodesX-1);
dy=Membrane_Ywidth/(NodesY-1);

% sets up the interpolation grid
x0=dx:dx:dx*(NodesX-2);
y0=dy:dy:dy*(NodesY-2);
z0=[1e-6];
[x,y,z]=meshgrid(x0,y0,z0);
xx=[x(:),y(:),z(:)]';

%% Start COMSOL model

import com.comsol.model.*
import com.comsol.model.util.*
model = ModelUtil.create('Model');
model.modelPath('C:\Users\Administrator\Desktop\MassL');
model.modelNode.create('mod1');
model.geom.create('geom1', 3);
model.mesh.create('mesh1', 'geom1');
model.physics.create('solid', 'SolidMechanics', 'geom1');
model.study.create('std1');
model.study('std1').feature.create('stat', 'Stationary');
%% create initial geometry
model.geom('geom1').feature.create('blk1', 'Block');
model.geom('geom1').feature('blk1').setIndex('size', '20e-6', 0);
model.geom('geom1').feature('blk1').setIndex('size', '20e-6', 1);
model.geom('geom1').feature('blk1').setIndex('size', '1e-6', 2);
model.geom('geom1').run('blk1');
model.geom('geom1').feature.create('blk2', 'Block');
model.geom('geom1').feature('blk2').setIndex('size', '1e-6', 0);
model.geom('geom1').feature('blk2').setIndex('size', '1e-6', 1);
model.geom('geom1').feature('blk2').setIndex('size', '1e-6', 2);
model.geom('geom1').feature('blk2').setIndex('pos', '5e-6', 0);
model.geom('geom1').feature('blk2').setIndex('pos', '5e-6', 1);
model.geom('geom1').run('blk2');
model.geom('geom1').feature.create('blk3', 'Block');
model.geom('geom1').feature('blk3').setIndex('size', '15e-6', 0);
model.geom('geom1').feature('blk3').setIndex('size', '15e-6', 1);
```

```
model.geom('geom1').feature('blk3').setIndex('size', '2e-6', 2);
model.geom('geom1').feature('blk3').setIndex('pos', '2.5e-6', 0);
model.geom('geom1').feature('blk3').setIndex('pos', '2.5e-6', 1);
model.geom('geom1').feature('blk3').setIndex('pos', '1e-6', 2);
model.geom('geom1').run('blk3');
model.geom('geom1').feature.create('blk4', 'Block');
model.geom('geom1').feature('blk4').setIndex('size', '14e-6', 0);
model.geom('geom1').feature('blk4').setIndex('size', '14e-6', 1);
model.geom('geom1').feature('blk4').setIndex('size', '1e-6', 2);
model.geom('geom1').feature('blk4').setIndex('pos', '3e-6', 0);
model.geom('geom1').feature('blk4').setIndex('pos', '3e-6', 1);
model.geom('geom1').feature('blk4').setIndex('pos', '1e-6', 2);
model.geom('geom1').run;

model.view('view1').set('renderwireframe', true);
%% Set material properties
model.material.create('mat1');
model.material('mat1').propertyGroup('def').set('youngsmodulus',
{'110e9'});
model.material('mat1').propertyGroup('def').set('poissonsratio',
{'0.22'});
model.material('mat1').propertyGroup('def').set('density', {'2200'});
model.material('mat1').selection.set([1 2 4]);
model.material.create('mat2');
model.material('mat2').selection.set([3]);
model.material('mat2').propertyGroup('def').set('youngsmodulus',
{'70e9'});
model.material('mat2').propertyGroup('def').set('poissonsratio',
{'0.35'});
model.material('mat2').propertyGroup('def').set('density', {'2700'});
%% Set Boundary loads
model.physics('solid').feature.create('fix1', 'Fixed', 2);
model.physics('solid').feature('fix1').selection.set([1 2 5 24]);
model.physics('solid').feature.create('bndl1', 'BoundaryLoad', 2);
model.physics('solid').feature('bndl1').selection.set([19]);
model.physics('solid').feature('bndl1').set('FperArea', {'0''0''1'});

model.mesh('mesh1').autoMeshSize(2);
model.mesh('mesh1').run;
%% Set study
model.sol.create('sol1');
model.sol('sol1').study('std1');
model.sol('sol1').feature.create('st1', 'StudyStep');
model.sol('sol1').feature('st1').set('study', 'std1');
model.sol('sol1').feature('st1').set('studystep', 'stat');
model.sol('sol1').feature.create('v1', 'Variables');
model.sol('sol1').feature.create('s1', 'Stationary');
model.sol('sol1').feature('s1').feature.create('fc1', 'FullyCoupled');
model.sol('sol1').feature('s1').feature.remove('fcDef');
model.sol('sol1').attach('std1');

model.result.create('pg1', 3);
model.result('pg1').set('data', 'dset1');
model.result('pg1').feature.create('surf1', 'Surface');
model.result('pg1').feature('surf1').set('expr', {'solid.mises'});
model.result('pg1').name('Stress (solid)');
```

```
model.result('pg1').feature('surf1').feature.create('def', 'Deform');
model.result('pg1').feature('surf1').feature('def').set('expr',
{'u''v''w'});
model.result('pg1').feature('surf1').feature('def').set('descr',
'Displacement field (Material)');
%% Remesh
model.mesh('mesh1').autoMeshSize(3);
model.mesh('mesh1').run;

model.sol('sol1').study('std1');
model.sol('sol1').feature.remove('s1');
model.sol('sol1').feature.remove('v1');
model.sol('sol1').feature.remove('st1');
model.sol('sol1').feature.create('st1', 'StudyStep');
model.sol('sol1').feature('st1').set('study', 'std1');
model.sol('sol1').feature('st1').set('studystep', 'stat');
model.sol('sol1').feature.create('v1', 'Variables');
model.sol('sol1').feature.create('s1', 'Stationary');
model.sol('sol1').feature('s1').feature.create('fc1', 'FullyCoupled');
model.sol('sol1').feature('s1').feature.remove('fcDef');
model.sol('sol1').attach('std1');
model.sol('sol1').runAll;

model.result('pg1').run;

model.name('mass20by20withaluminum.mph');
%% Run mdel to verify
model.result('pg1').run;
model.geom('geom1').feature('blk2').set('base', 'center');
model.geom('geom1').feature('blk2').setIndex('pos', '1e-6', 0);
model.geom('geom1').feature('blk2').setIndex('pos', '1e-6', 1);
model.geom('geom1').feature('blk2').setIndex('pos', '0.5e-6', 2);
model.geom('geom1').runAll;
model.geom('geom1').run;
model.physics('solid').feature('bndl1').selection.set([9]);
model.mesh('mesh1').run;
%% Set up final block size for actuation
model.sol('sol1').study('std1');
model.sol('sol1').feature.remove('s1');
model.sol('sol1').feature.remove('v1');
model.sol('sol1').feature.remove('st1');
model.sol('sol1').feature.create('st1', 'StudyStep');
model.sol('sol1').feature('st1').set('study', 'std1');
model.sol('sol1').feature('st1').set('studystep', 'stat');
model.sol('sol1').feature.create('v1', 'Variables');
model.sol('sol1').feature.create('s1', 'Stationary');
model.sol('sol1').feature('s1').feature.create('fc1', 'FullyCoupled');
model.sol('sol1').feature('s1').feature.remove('fcDef');
model.sol('sol1').attach('std1');
model.sol('sol1').runAll;
model.result('pg1').run;
model.geom('geom1').feature('blk2').setIndex('size', '0.5e-6', 2);
model.geom('geom1').feature('blk2').setIndex('pos', '0.25e-6', 2);
model.geom('geom1').runAll;
model.geom('geom1').run;
```

```
%% set the loop to iterate over all BEM nodes
in=1;
for lx=1:1:NodesX-2
for ly=1:1:NodesY-2
       locx=dx*lx;
       locy=dy*ly;

model.geom('geom1').feature('blk2').setIndex('pos', num2str(locx), 0);
model.geom('geom1').feature('blk2').setIndex('pos', num2str(locy), 1);
model.sol('sol1').study('std1');
model.sol('sol1').feature.remove('s1');
model.sol('sol1').feature.remove('v1');
model.sol('sol1').feature.remove('st1');
model.sol('sol1').feature.create('st1', 'StudyStep');
model.sol('sol1').feature('st1').set('study', 'std1');
model.sol('sol1').feature('st1').set('studystep', 'stat');
model.sol('sol1').feature.create('v1', 'Variables');
model.sol('sol1').feature.create('s1', 'Stationary');
model.sol('sol1').feature('s1').feature.create('fc1', 'FullyCoupled');
model.sol('sol1').feature('s1').feature.remove('fcDef');
model.sol('sol1').attach('std1');
model.sol('sol1').runAll;
model.result('pg1').run;

data = mpheval(model,'w')
mem_disp = mphinterp(model,'w','coord',xx);

     disp(in,:)=mem_disp;

save('C:\Users\Administrator\Desktop\MassL\MLal20by20v4_smallerblock','
disp');
     in=in+1

end
end
```

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