Transparent Oxide Semiconductors for Emerging Electronics

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ABSTRACT

Transparent Oxide Semiconductors for Emerging Electronics

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Transparent oxide electronics have emerged as promising materials to shape the future of electronics. While several n-type oxides have been already studied and demonstrated feasibility to be used as active materials in thin film transistors, high performance p-type oxides have remained elusive. This dissertation is devoted to the study of transparent p-type oxide semiconductor tin monoxide and its use in the fabrication of field effect devices.

A complete study on the deposition of tin monoxide thin films by direct current reactive magnetron sputtering is performed. Carrier density, carrier mobility and conductivity are studied over a set of deposition conditions where p-type conduction is observed. Density functional theory simulations are performed in order to elucidate the effect of native defects on carrier mobility.

The findings on the electrical properties of SnO thin films are then translated to the fabrication of thin films transistors. The low processing temperature of tin monoxide thin films below 200 °C is shown advantageous for the fabrication of fully transparent and flexible thin film transistors. After careful device engineering, including post deposition annealing temperature, gate dielectric material, semiconductor thickness and source and drain electrodes material, thin film transistors with record device performance are demonstrated, achieving a field effect mobility >6.7 $cm^2V^{-1}s^{-1}$.

Device performance is further improved to reach a field effect mobility of 10.8 $cm^2V^{-1}s^{-1}$ in SnO nanowire field effect transistors fabricated from the sputtered SnO thin films and patterned by electron beam lithography. Downscaling device dimension to nano scale is shown beneficial for SnO field effect devices not only by achieving a higher hole mobility but enhancing the overall device performance including better threshold voltage, subthreshold swing and lower number of interfacial defects.

Use of p-type semiconductors in nonvolatile memory applications is then demonstrated by the fabrication of hybrid ferroelectric field effect transistors composed of organic ferroelectric layer polyvinylidene fluoride trifluoroethylene and inorganic p-type semiconductor tin monoxide. Both rigid and flexible devices are demonstrated, showing the advantages of low temperature oxides over polymer semiconductors by achieving much better performance, such as order of magnitude higher hole mobility.

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LIST OF ABBREVIATIONS

AFM – atomic force microscopy

ALD - atomic layer deposition

AMOLED- active matrix organic light emitting diode

ATO- aluminum titanium oxide

AZO- aluminum doped zinc oxide

CB- conduction band

CBM- conduction band minimum

CMOS- complementary metal oxide semiconductor

CVD- chemical vapor deposition

DC -direct current

DFT- density functional theory

DI- de-ionized water

DOS- density of states

EBL- electron beam lithography

FeFET- ferroelectric field effect transistor

FET- field effect transistor

FFT- fast Fourier transformation

FPD- flat panel display

FTO- fluorine doped tin dioxide

HRTEM- high-resolution transmission electron microscopy

IGZO- indium gallium zinc oxide

IPA- isopropyl alcohol

ITO- indium tin oxide

IUPAC- International Union of Pure and Applied Chemistry

IZO- indium zinc oxide

KAUST- King Abdullah University of Science and Technology

LCD- liquid crystal display

MIBK- methyl isobutyl ketone

MOS- metal oxide semiconductor

MOSFET- metal oxide semiconductor field effect transistor

NW- nanowire

NWFET- nanowire field effect transistor

OLED- organic light emitting device

P(VDF-TrFE)- polyvinylidene fluoride trifluoroethylene

PDA- post deposition annealing

PECVD- plasma enhanced chemical vapor deposition

PLD- pulsed laser deposition

PMMA- polymethyl-methacrylate

PPMS- physical properties measurement system

PV- photovoltaic

PVD- physical vapor deposition

rf- radio frequency

sccm- standard cubic centimeters per minute

SEM- scanning electron microscopy

TCO- transparent conducting oxide

TEM- transmission electron microscopy

TFT- thin film transistor

TSO- transparent semiconducting oxide

UPS- ultra violet photoelectron spectroscopy

UV- ultra violet

VB- valence band

VBM- valence band maximum

XPS- x-ray photoelectron spectroscopy

XRD- x-ray diffraction

ZTO- zinc tin oxide

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Chapter 1

Motivation, Objective and Structure of the Dissertation

Transparent electronics have been envisioned many years ago; but just recently, thanks to the development of transparent conducting and semiconducting oxides, they are becoming a reality. Transparent electronics is an emerging field of great importance that will allow the development of innovative and disruptive technology away from conventional silicon-based technology. The use of transparent metal oxide semiconductors as the active material in the thin film transistors used in liquid crystal displays and active matrix organic light emitting diode displays have been proved advantageous. Several display companies are moving towards the replacement of traditional amorphous silicon for the more advanced transparent metal oxides. The realization of fully transparent displays is no longer a dream, but close to reality in the years to come.

As an emerging field, nevertheless, there are certain materials requirements that need to be assessed to broaden the applications of transparent oxide electronics. The viability of this technology greatly depends on the suitability of transparent transistors. While several transparent n-type oxide semiconductors have been demonstrated feasible and useful for the fabrication of thin film transistors, a viable p-type oxide remains elusive. Both n- and p-type oxides with comparable performance are required for the fabrication of technologies based on the complementary metal oxide semiconductor (CMOS) logic, which is preferable for low power consumption circuits. In the other hand, several of the envisioned applications are flexible circuits on inexpensive plastic substrates, so for oxide semiconductors to make it

into practical applications, other material requirements are large area scalability, mechanical flexibility and low temperature processing.

Even though oxide semiconductors are on the early development stage, they have arrived to stay, not to replace silicon, but to complement it and allow the design and fabrication of innovative and creative see-trough applications that have existed only in our dreams.

The main objective of this research work is to develop, study and optimize a thin film deposition process for transparent p-type oxide semiconductor, tin monoxide, and the fabrication, characterization and optimization of field effect devices. Reactive direct current magnetron sputtering is selected as the deposition technique, while thin film transistors are the main devices used to demonstrate the feasibility of this material for its use on the fields of transparent and flexible electronics.

This dissertation is organized as follows:

Chapter 2. Literature review and fundamental background is presented in chapter 2. Basics of transparent conducting oxides (TCO) and transparent semiconducting oxides (TSO) are discussed here, along with actual and emerging applications. Fundamentals of p-type oxide semiconductor tin monoxide are then discussed, followed by a summary on the state of the art of p-type oxides. Finally, structure, fabrication and operation of thin film transistors (TFTs) are presented.

Chapter 3. This chapter presents the experimental techniques used for the processing and characterization of thin films as well as the experimental details for the fabrication and characterization of field effect devices, mainly focused on TFTs. Important parameters typically used to quantify the performance of field effect devices are also summarized, along with the protocol used for effective electrical characterization of metal oxide field effect devices.

Chapter 4. The main results obtained in the development of high performance p-type oxide thin films and TFTs are discussed in this chapter. A detailed film characterization is first presented, followed by density functional theory simulations performed to explain the enhanced carrier mobility observed in the tin monoxide films. TFT fabrication on both rigid and flexible substrates is discussed, including the device engineering performed in order to achieve the high mobility values presented.

Chapter 5. This chapter focuses on the fabrication and characterization of nanowire field effect transistors using the optimized tin monoxide films and electron beam lithography to achieve even better performance when compared to thin film transistors. This chapter shows experimental evidence of the advantages of reducing device dimensions, taking them to the nanoscale, to boost device performance in p-type SnO-based field effect devices.

Chapter 6. This chapter discusses the fabrication and characterization of ferroelectric field effect transistors combining the inorganic p-type semiconductor, SnO, with an organic ferroelectric material, to demonstrate the first ever p-type oxide ferroelectric field effect transistor for applications in non-volatile memories. Both rigid and flexible devices are

presented, exhibiting an order of magnitude improvement on carrier mobility when compared to organic p-type semiconductors.

Chapter 7. The main conclusions of this dissertation, future work, remaining challenges, and prospects for p-type oxide semiconductor-based field effect devices are discussed on chapter 7.

Chapter 2

Literature Review and Technical Background

Chapter 2 provides an introductory background to the topics discussed in this dissertation. Principles of transparent conducting and semiconducting oxides are first discussed, followed by their current and emerging applications. A section of this chapter is then dedicated to p-type oxide semiconductor tin monoxide, as it is the main material analyzed throughout this research work. The relevance of tin monoxide is analyzed in the state of art in p-type oxide semiconductors. Since thin film transistors are the key field effect devices fabricated for this research work, device structure, fabrication, and operation is covered in this chapter.

2.1 Transparent Conducting and Semiconducting Oxides

This section provides an introduction to the basics of transparent semiconducting oxides (TSOs) by analyzing the generic properties and applications of transparent conducting oxides (TCOs). The definition of TCO is briefly presented analyzed from a band structure point of view, followed by actual and emerging applications of both TCOs and TSOs.

2.1.1 Basics of Transparent Conducting Oxides

Transparent conducting oxides are unique materials combining optical transparency in the visible region of the electromagnetic spectrum and electrical conductivity[1]. If analyzed from a band structure point of view these properties are contradictory: metallic conductors have a large density of states in the band where the Fermi level is located, giving rise to a high concentration of free carriers, whereas transparent materials are typically insulators with empty conduction bands and totally filled valence bands[2].

The combination of these two properties is achieved by degenerately doping a host material displacing the Fermi level (E_F) to lie within the conduction band. Common host materials include CdO, ZnO, SnO_2 and In_2O_3, which are typical insulators in their undoped, stoichiometric state with an optical band gap (E_G) > 3 eV[2-6]. These typical host materials have a conduction band formed by the interactions of the metal *s* and oxygen *p* orbitals, exhibiting a highly dispersed, single-electron-like parabolic conduction band due to the *s* orbitals, and a flat valence band composed of the oxygen *p* orbitals[7-10]. Figure 2.1 illustrates the band structure of the typical host materials. Degenerate doping, achieved either by substitution or defect formation, displaces the E_F via a Burstein-Moss shift, allowing the material to be conductive. The degenerate doping provides the additional extra carriers that exhibit high mobility as a result of their small electron effective masses, as well as preserving the optical transparency of the host material since the increase in the optical absorption is quite low because of the low density of states in the conduction band[2]. In Burstein-Moss shift, the free electrons in the dispersed conduction band (lowest energy) do not shift to the conduction band minimum, but to unoccupied states of higher energies, increasing the energy of the lowest optical transition[11]. A schematic representation of this description is shown in Figure 2.2.

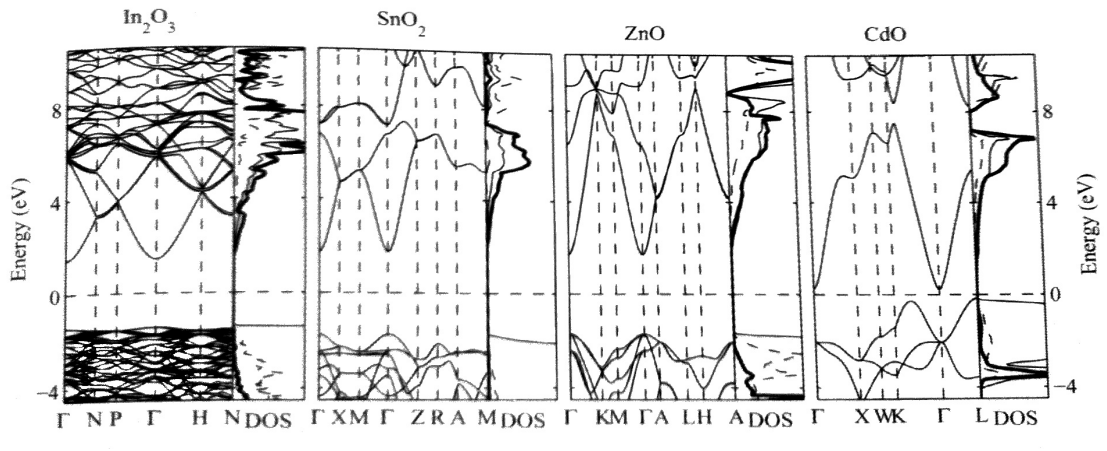

Figure 2.1. Band structure of conventional TCO host materials. Electronic band structure and partial density of states (DOS) of **a,** In_2O_3; **b,** SnO_2; **c,** ZnO; **d,** CdO. In the DOS plots, the thick, dashed, and the thin lines represent metal *s*, metal *p* and oxygen *p* states, respectively. *From Facchetti and Marks*[2].

Having the ability to be electrically conductive, while preserving optical transparency is challenging due to the close relation between optical and electronic properties[12,13]. The high carrier concentration needed for electrical conductivity may decrease the optical transparency by increasing the optical absorption caused by inter-band and intra-band transitions at short and long wavelengths, respectively. Furthermore, the degenerate doping achieved either by point defects or substitutional dopants can seriously affect charge transport by ionized impurity scattering mechanism[2].

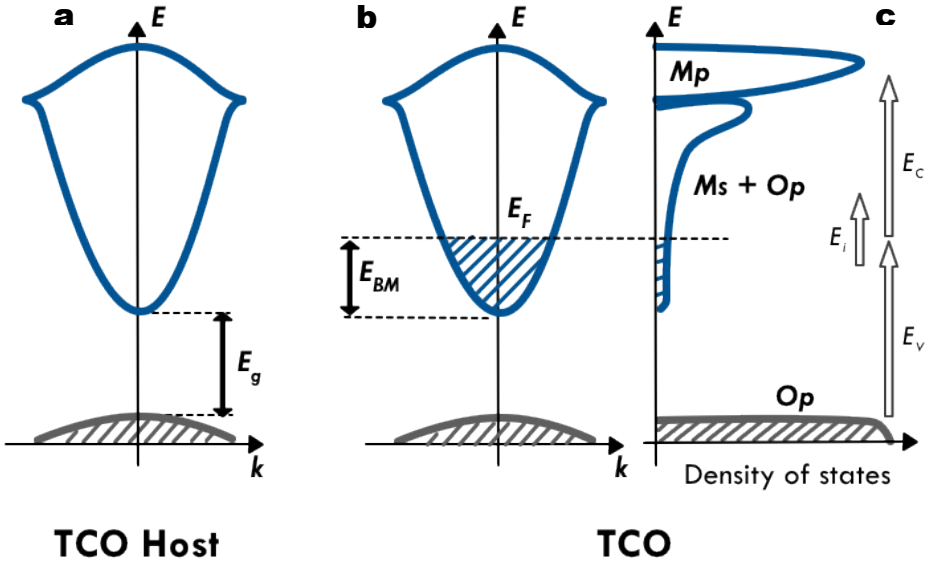

Figure 2.2. Schematics of the TCO band structure. a, an insulating TCO host with a band gap E_g > 3 eV. **b,** Degenerate doping displaces the Fermi level (E_F) via a Burstein-Moss shift (E_{BM}) making the TCO host conductive. **c,** Density of states of a typical TCO. The shift broadens the optical transparency window, while the intraband absorption is minimized as the next empty conduction band is far above the *Ms+Op* single band. *Adapted from Facchetti and Marks*[2].

Conventional TCO materials are those formed by the oxides of Zn, Sn, In, Ga and Cd, which combined with possible dopants as listed in Table 2.1, form most of the known TCOs and TSOs materials[1]. TSOs share the same principles of TCOs, but showing a lower free carrier concentration, N, ($N \approx 10^{14\text{-}18}$ cm^{-3}) not enough to shift E_F to lie within the conduction band, that allows them to be used as active components for several applications. Sn-doped In_2O_3 (ITO), Al-doped ZnO (AZO) and F-doped SnO_2 (SnO_2:F) constitute the most well-known TCO materials, in which the extrinsic doping is used to enhance the electrical conductivity.

TCOs and TSOs are predominantly n-type materials, as it is easier to form donor-like defects (oxygen vacancies and cation interstitials) in conventional host materials, being the binary oxides ZnO, In_2O_3, SnO_2 and the more complex systems $InGaO_3(ZnO)_5$ (IGZO)[14-18], In-Zn-O (IZO)[19-22], and Zn-Sn-O (ZTO)[23-26] the most widely studied.

Nevertheless, p-type TSOs are needed for the fabrication of more complex transparent electronics like complementary-metal-oxide-semiconductor (CMOS)-based circuitry. A more detailed discussion on the challenges and state of the art in p-type oxides is presented in section 2.2, where the most promising p-type material, tin monoxide, is analyzed.

Material	Dopant or compound
SnO_2	Sb, F, As, Nb, Ta
In_2O_3	Sn, Ge, Mo, F, Ti, Zr, Hf, Nb, Ta, W, Te
ZnO	Al, Ga, B, In, Y, Sc, F, V, Si, Ge, Ti, Zr, Hf
CdO	In, Sn
$ZnO\text{-}SnO_2$	Zn_2SnO_4, $ZnSnO_3$
$ZnO\text{-}In_2O_3$	$Zn_2In_2O_5$, $Zn_3In_2O_6$
$In_2O_3\text{-}SnO_2$	$In_4Sn_3O_{12}$
$CdO\text{-}SnO_2$	Cd_2SnO_4, $CdSnO_3$
$CdO\text{-}In_2O_3$	$CdIn_2O_4$
$MgIn_2O_4$	
$GaInO_3$, $(Ga, In)_2O_3$	Sn, Ge
$CdSb_2O_6$	Y
$ZnO\text{-}In_2O_3\text{-}SnO_2$	$Zn_2In_2O_5$ - $In_4Sn_3O_{12}$
$CdO\text{-}In_2O_3\text{-}SnO_2$	$CdIn_2O_4$ - Cd_2SnO_4
$ZnO\text{-}CdO\text{-}In_2O_3\text{-}SnO_2$	

Table 2.1. Dopants for TCO and TSO materials. *From Tadatsugu Minami*[27].

2.1.2 Applications of TCOs

Industrial uses of TCOs are mainly dominated by three areas: architectural window applications, flat panel displays (FPDs) and photovoltaic cells, and limited to few materials: SnO_2, ITO, IZO and just recently IGZO[1,28]. Nevertheless, emerging applications based on the spectral selectivity, solar control coatings, and transparent and flexible electronics offer a huge market potential for existing TCOs as well as a growing demand for new materials, such as a high performance p-type oxide semiconductor.

Among energy efficient windows, known as low emittance (low-e) windows, SnO_2:F is the most widely used material[29,30]. The energy efficiency concept behind the low-e windows is the use of the tin oxide coating to prevent radiative heat loss taking advantage of the low thermal emmittance of SnO_2:F: around 0.15 in contrast to 0.84 for common glass[31]. Tin oxide coated glass is also used for heated glass freezer doors, on which a small current is circulated on the TCO coating to defrost the glass door[1]. The demand for low-e coating glass in the European Union in 2010 was around 100 millions m^2, and rapidly increasing over the years[32]. Demand in China grew from 3 millions m^2 in 2004 to 97 millions m^2 in 2010[33], which gives an indication of the huge market demand for low-e coatings.

The second biggest market for TCOs is FPDs. ITO and in some extent IZO, are the most common materials, being used as passive elements (electrodes) in liquid crystal displays (LCDs), touch screens, plasma displays, and organic light emitting diode (OLED) displays. Market revenue on FPDs grew from US$65.25 billions in 2005 to US$125 billion in 2012[34,35], due to the worldwide adoption of FPDs and increasing demand in portable electronics.

Photovoltaic (PV) cells are currently the third, but fastest growing market for TCOs. With a sustained growth rate of about 40% since 2007 PV modules represent a huge market for TCOs. Being used as a transparent current collector, TCOs are critical components of silicon-based as well as thin film-based solar cells[1,2]. Figure 2.3 shows some of the current applications of TCOs.

Figure 2.3. Applications of TCOs. a, Architectural applications (low e-glass). *From gravinawindows.com*; **b,** Flat panel displays. *From apple.com*; **c,** Photovoltaic cells. *From bubblews.com*

2.1.3 Emerging Applications

TCOs are predominantly used as passive elements in the applications described previously. Emerging applications take advantage of TCOs and specially TSOs as active elements for the fabrication of technologies than can be summarized in two main areas: transparent electronics and applications based on temporal variability.

Transparent electronics is a high profile and very advanced topic for a wide range of device applications, with transparent semiconducting materials being the key element for the development of this area. Passive uses of TCOs can be combined with oxide-based transparent thin film transistors (TFTs) to fabricate a wide range of new and disruptive technology: transparent electronics. If fabricated at low temperatures, these transparent devices can be even made on plastic substrate for the fabrication of flexible electronics. Figure 2.4 illustrates some of the envisioned applications of TSOs.

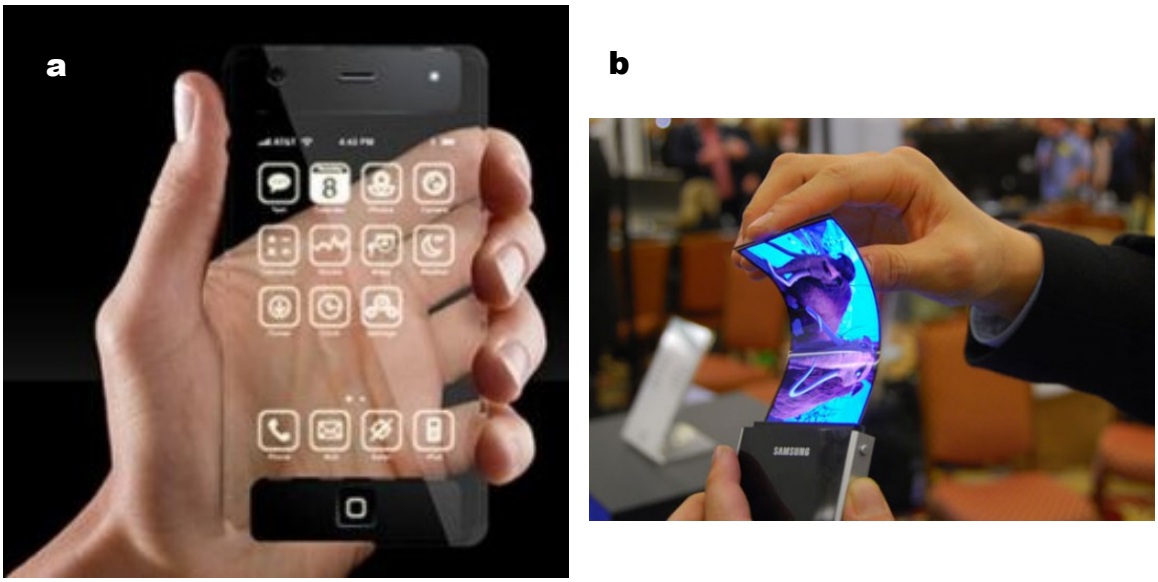

Figure 2.4. Emerging Applications. a, Transparent electronics. *From troxel.com*; **b,** Flexible displays. *From Samsung.com*

According to the most recent display market forecast from the market research firm Dsiplaybank, transparent display technologies will dominate the market by 2030 with a projected market around US$150 billions[35], as shown in Figure 2.5. Beginning in 2010, display companies like Samsung Electronics, LG Electronics and Sharp Electronics, among others, have demonstrated oxide-based displays with enhanced performance when compared with conventional silicon-based ones[28,36]. The key parameter for improved display performance has been the replacement of a-Si:H for TSOs materials, specifically IGZO, as the active element in the thin film transistors used as the switching/driving current elements for pixel control. Just recently in 2012 Samsung announced for the first time the production of a fully transparent LCD with 90% energy consumption reduction when compared with a conventional LCD[37]. The improved energy efficiency arises from the elimination of the backlight required in the conventional LCD, as the fully transparent display uses the ambient light, significantly reducing the power consumption.

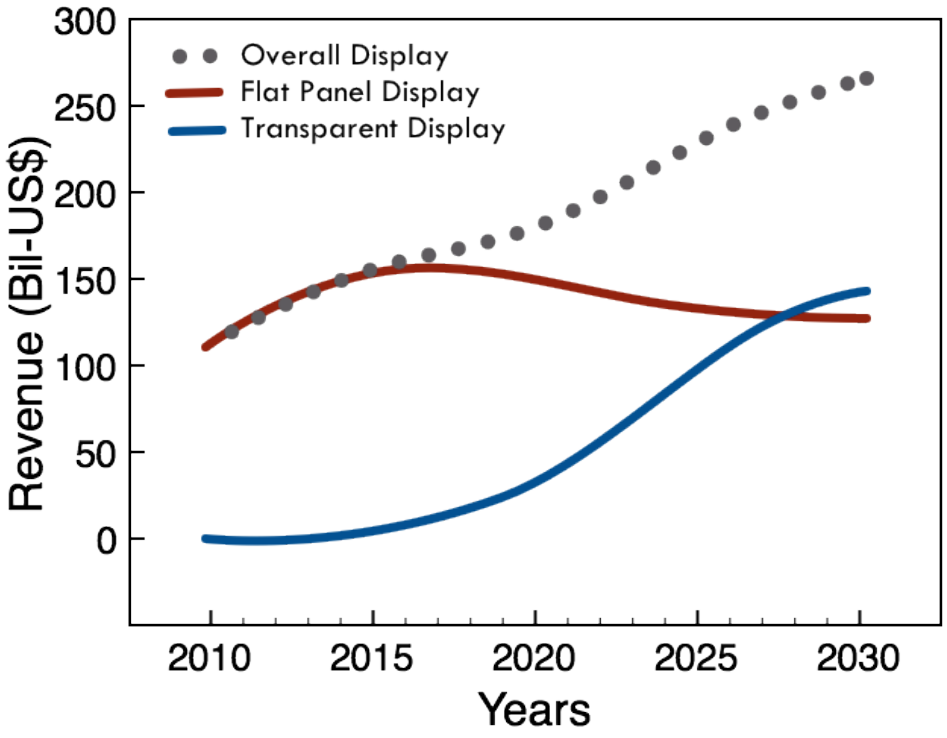

Figure 2.5. Display market revenue evolution and forecast. *Adapted from Displaybank*[35].

Display market is still dominated by a-Si:H and poly-Si used as the active TFT material . Table 2.2 shows a comparison between the available materials for the development of transparent electronics.

TFT Properties	a-Si:H	Low-T poly-Si	Oxide semiconductors*	Organic semiconductors
Carrier mobility ($cm^2V^{-1}s^{-1}$)	1 max	50 to 100	1 to 100	0.1 to 10
Switching ($V\ dec^{-1}$)**	0.4-0.5	0.2-0.3	0.1-0.6	0.1-1.0
Leakage current (A)**	$\sim10^{-12}$	$\sim10^{-12}$	$\sim10^{-13}$	$\sim10^{-12}$
Manufacturing cost	Low	High	Low	Low
Long term TFT reliability	Low	High	High^{+}	Low in air
Yield	High	Medium	High	High
Process Temperature (^oC)	~250	<500	RT to 350	RT

Table 2.2. Comparison between available materials for the development of transparent electronics. *From Fortunato et al*[36]. *Based on n-type oxides. **Highly dependent on dielectric. $^{+}$Forecast.

Applications based on temporal variability have been recently demonstrated, and emerged as a commercial reality in the form of electrochromic windows[1]. An electrochromic device, as the one depicted in Figure 2.6a, is a multicomponent device in which an electrochomic film changes its transmittance in response to an electrical stimulus applied across the TCOs[38]. Smart windows with electronically adjustable transparency can be found in automotive applications[38,39] and more recently as part of the highly efficient Boeing 787 Dreamliner[40]. Other emerging applications include photochromic and thermochromic devices, which change their transparency in response to light and thermal stimulus respectively[30].

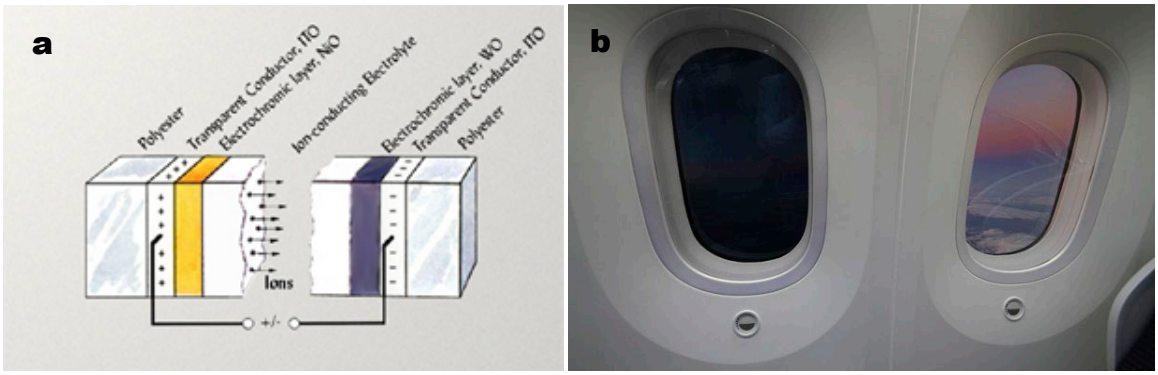

Figure 2.6. Electrochromic device. a, Basic device structure. *From Granqvist et al*[41]; **b,** Electronically adjustable windows in the Boeing 787 Dreamliner. *From theplaneblog.wordpress.com.*

Undoubtedly, transparent oxides have a promising future to be used in a wide range of applications, especially as the active elements in the development of transparent electronics. From the comparison shown in Table 2.2, it is possible to conclude that oxide semiconductors are the most promising candidate materials for transparent and flexible electronics, based in high carrier mobility, low processing temperature, low manufacturing cost and long term reliability. Nevertheless, a key challenge remains: the development of a p-type oxide semiconductor with performance comparable to that of the n-type oxides.

2.2 Tin Monoxide

This section describes the general properties of Tin Monoxide. A brief introduction to the formation mechanism and thermodynamics of SnO is presented, followed by an introduction to its crystal and electronic structure. The relevance of tin monoxide as a p-type TSO is discussed in the analysis of state of the art in p-type oxides semiconductors.

2.2.1 Introduction to Tin Monoxide

Tin oxides are found in two forms: tin monoxide (SnO) or stannous oxide, and tin dioxide (SnO_2) or stannic oxide. This two forms results from the dual valence of tin, 2+ and 4+, respectively. Tin dioxide is a functional material that has been extensively studied and characterized, mainly due to its multiple applications of technological significance[36,42]. As mentioned previously, SnO_2:F (also known as FTO) is of very high industrial importance as it is extensively used in low-e windows and as a TCO in solar cell applications[1,43,44], while in its pure state is the active material in solid-state gas sensing devices[44] and oxidation catalysis[42]. Non-stoichiometric tin dioxide is an intrinsic n-type semiconductor in which structural defects, such as the oxygen vacancies and tin interstitials, generate free electrons raising the Fermi level close to the conduction band[36].

Tin monoxide is in contrast, much less characterized than tin dioxide, as well as the less abundant form of tin oxide. The lack of SnO single crystals has prevented a more extensive characterization of the properties of this material. Previously, SnO has been used as anode material in lithium ion batteries[45,46], catalyst for oxygen reduction in acid electrolytes[47] and as a precursor for the production of SnO_2[48]. Nevertheless, being an

intrinsic p-type semiconductor has attracted attention to be used as a transparent oxide semiconductor.

Figure 2.7 shows the Sn-O phase diagram at atmospheric pressure[49]. SnO is observed in the phase diagram as a stoichiometric compound having a single, well-defined composition occurring at temperatures below 543±20 K. Some intermediate phases between SnO and SnO_2 can be observed. These intermediate phases, identified as Sn_3O_4 and Sn_2O_3, are normally assigned by its composition with Sn existing in a combination of Sn(II) and Sn(IV)[50,51]. SnO has a heat of formation at 298 K of ΔH=-68 cal/mol compared to the ΔH=-138 cal/mol of SnO_2[52], resulting in a reaction

$$SnO + \frac{1}{2}O_2 \rightarrow SnO_2 \tag{2.1}$$

also the disproportionation reaction given by

$$xSnO \rightarrow Sn_xO_y + (x-1)Sn \tag{2.2}$$

can occur via the intermediate oxide phases and started by the internal displacement of oxygen even at low temperatures[53]. SnO_2, the more thermodynamically stable form of tin oxide, is then formed at higher temperatures as a result of the external oxygen diffusion that oxidizes the metallic tin and intermediate oxide:

$$Sn_xO_y + (x-1)Sn + O_2 \rightarrow SnO_2 \tag{2.3}$$

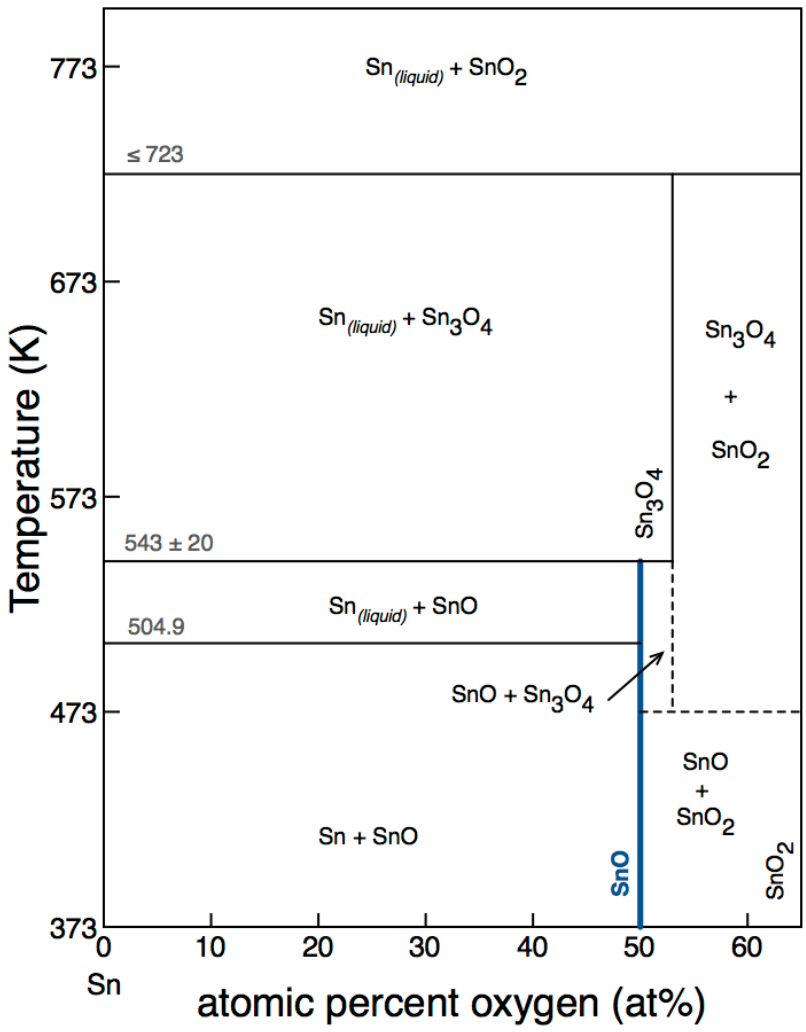

Figure 2.7. Sn-O phase diagram. Tin monoxide is observed as stoichiometric compound with a single, well-defined composition (highlighted in blue).

Table 2.3 summarizes the properties of tin monoxide

Properties of Tin Monoxide	
IUPAC Name	Tin(II) oxide
Other names	Stannous oxide, tin monoxide
Molecular formula	SnO
Molar mass (g/mol)	134.709
Density (g/cm^3)	6.45
Melting point	1080 °C (decomposes)
Solubility in water	Insoluble

Table 2.3. General properties of SnO. *Adapted from webelements.com.*

2.2.2 Crystal Structure of Tin Monoxide

SnO has the litharge structure, isostructural to PbO, with a tetragonal unit cell described by the symmetry space group P4/nmm[42,54]. Lattice constants of SnO are typically a = b = 3.8029 Å and c = 4.8382 Å[54]. The unit cell is composed of two tin atoms and two oxygen atoms in the positions Sn (0, ½,u; ½, 0, -u) and O (0,0,0; ½, ½, 0) with u=0.244[55]. SnO has a layered structured in the [001] direction with a $Sn_{1/2}$-O-$Sn_{1/2}$ sequence and van der Waals gap between the Sn layers of 2.52 Å. Each Sn and O atoms has a fourfold coordination and O is tetrahedrally bonded to Sn, with a bond length of 2.23 Å[54]. Figure 2.8 depicts the crystal structure of SnO. Tin monoxide exists in a stable blue-black form and a metastable red form[56]. The stable black form is rarely found in nature as the mineral romarchite[56], shown in Figure 2.8c.

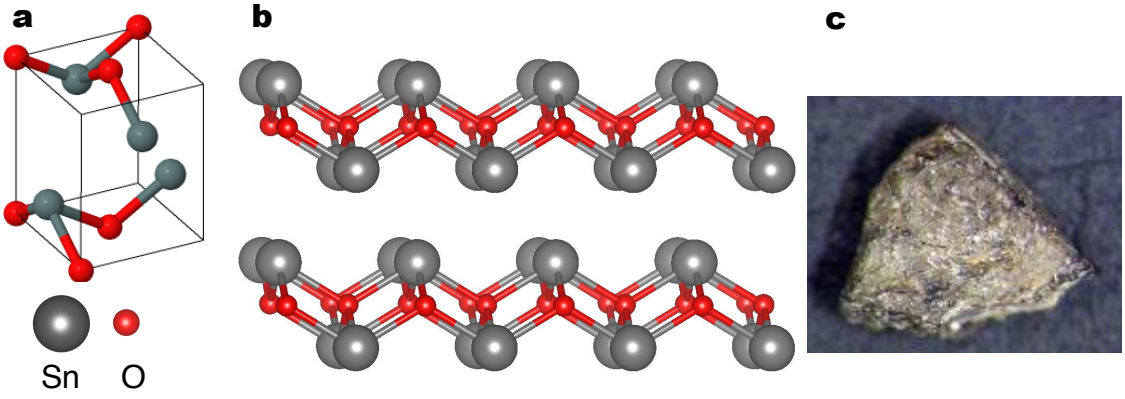

Figure 2.8. Crystal structure of SnO. **a,** Unit Cell; **b,** layered structure in the [001] crystallographic direction; **c**, Romarchite mineral, *from mindat.org.*

2.2.3 Electronic Structure of Tin Monoxide

In typical metal oxides the conduction band (CB) is formed by the spatially spread *s* orbitals of the metal while the valence band (VB) is dominated by the very localized and anisotropic oxygen *2p* states. This typical configuration (localized O 2*p* orbitals in the VB) reduces hole mobility because the holes are trapped in the localized oxygen states. The electronic structure of tin monoxide is different from typical n-type oxide semiconductors. The VB region at high energy of tin monoxide has contributions of the Sn *5s*, Sn *5p,* and O *2p* orbitals, but close to the valence band maximum (VBM), Sn *5s* and O *2p* have almost equal contributions, slightly dominated by the Sn *5s* orbitals[57], as shown in Figure 2.9.

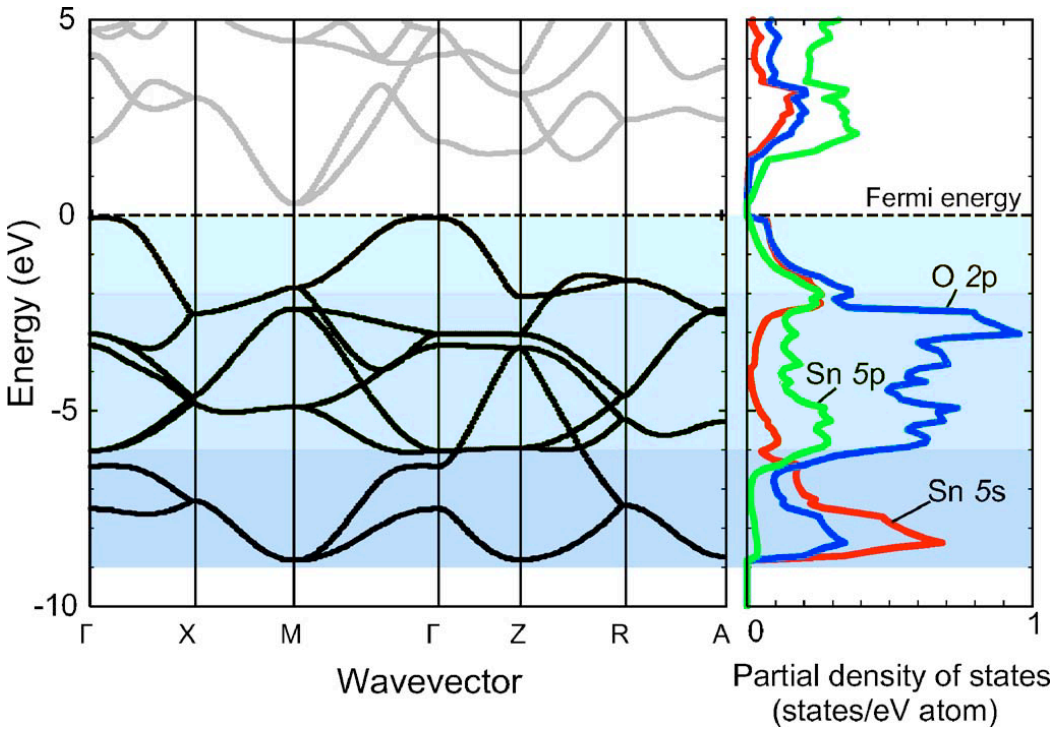

Figure 2.9. Band structure of SnO. *From Togo et al*[57].

Nearly equal contributions of the Sn *5s* and O *2p* orbitals at the VBM are advantageous to reduce the VB edge localization, leading to an enhancement on hole

mobility and giving SnO its p-type character[57-60]. Figure 2.10 depicts a comparison between the band structure of SnO and SnO_2, showing the VBM hybridization in SnO arising from the nearly equal contributions of Sn *5s* and O *2p* orbitals. The conduction band minimum (CBM) of tin monoxide is mainly formed by contributions of Sn *5p*. The band structure of SnO is in good contrast to n-type SnO_2 that has a VBM formed of O *2p* orbitals and CBM of Sn *5s* orbitals[42,57].

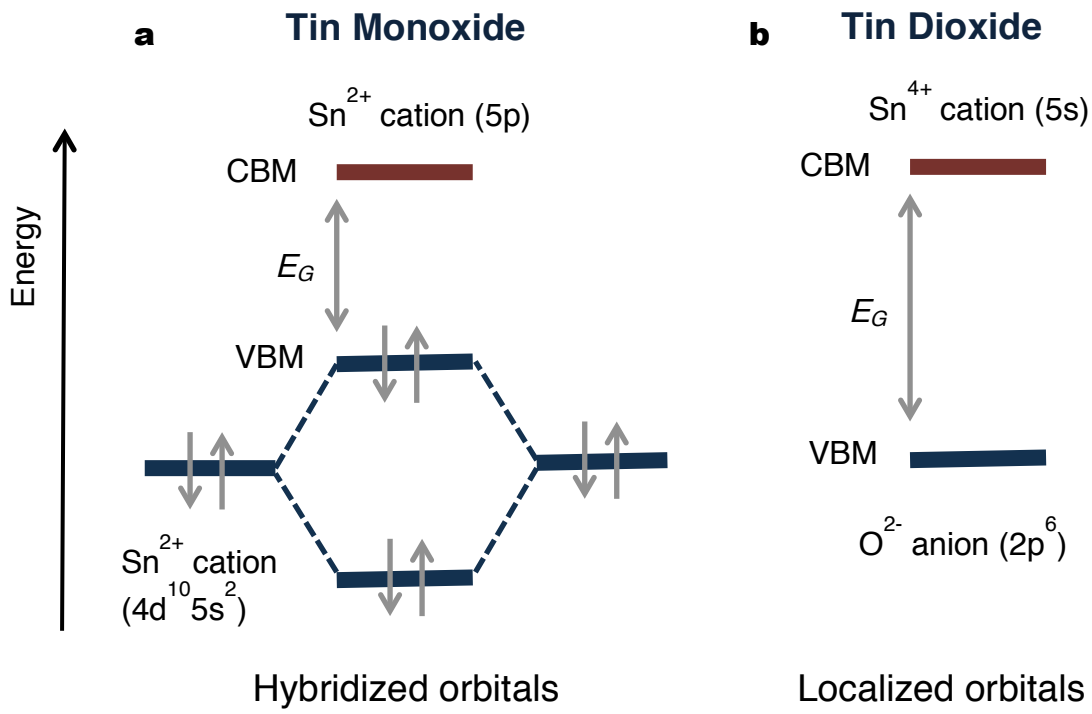

Figure 2.10. Band structure comparison. a, SnO **b,** SnO_2. SnO shows orbital hybridization at the VBM while SnO_2 shows localized O *2p* orbitals, characteristics of conventional n-type oxides.

p-type conductivity can be attributed to Sn vacancies (V_{Sn}) and O interstitials (O_i) that when fully ionized can give rise to the formation of acceptor like band states. Nevertheless, Togo *et al.* have demonstrated by first principles calculations that Sn vacancies give SnO its p-type character based on their calculations on the defect formation energies and defect concentrations (Figure 2.11)[57]. They also demonstrated that the O_i equilibrium

defect concentration is comparable to that of the Sn vacancy, but it is hardly ionized, therefore not contributing to the conductivity. Furthermore, the donor-like defects Sn interstitial (Sn_i) and Oxygen vacancy (V_O) have a very small concentration, not enough to cancel the holes generated by the V_{Sn}[57].

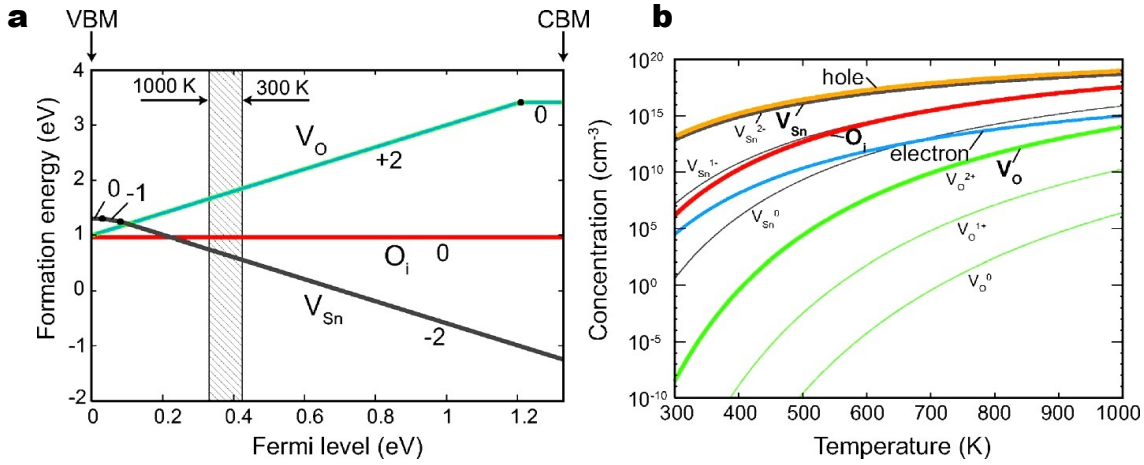

Figure 2.11. Defect formation energy. a, Defect formation energies as a function of the Fermi level. **b,** Defect concentrations as function of temperature**.** *From Togo et al*[57]**.**

The hole formation as a result of an ionized Sn vacancy can be described by the defect reaction using the Kröger-Vink notation with or without the formation of an oxygen vacancy:

$$SnO \Leftrightarrow Sn_{Sn}^{x} + O_{O}^{x} + V_{Sn}^{2-} + 2h^{+} \tag{2.4}$$

$$SnO \Leftrightarrow Sn_{Sn}^{x} + O_{O}^{x} + V_{Sn}^{2-} + O_{i}^{2-} + V_{O}^{2+} + 2h^{+} \tag{2.5}$$

Ogo *et al.* have estimated the ionization potential of SnO from ultra violet photoelectron spectroscopy (UPS) measurements of SnO_2 as they couldn't obtain reliable UPS data for bulk or thin-film samples of SnO[59]. They have estimated the VBM to be 5.8 eV, with an indirect fundamental band gap of 0.7 eV. CBM is then estimated to be around

2.7 to 2.9 eV above VBM based on the optical determination of the band gap. Figure 2.12, shows the estimated band structure of SnO.

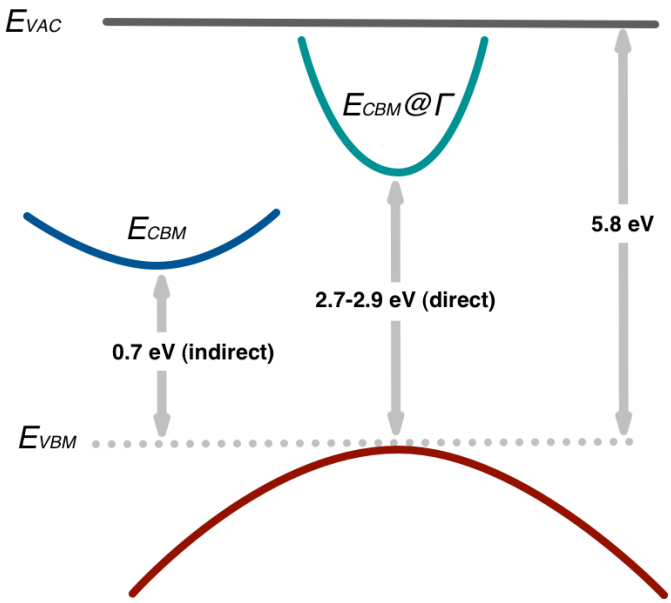

Figure 2.12. Schematic illustration of the band structure of SnO. *Adapted from Nomura et al*[61].

2.2.4 State of the art of p-type oxides

In this section a brief description of the state of the art of p-type oxide TFTs is presented. Three main metal oxides have been reported to show p-type conductivity: NiO, Cu-based oxides and SnO. Among them, Cu based semiconductors, especially those with the delafossite structure $CuMO_2$ (M=Al, Ga, In, Y, Sc, La, etc.) have been extensively studied being $CuAlO_2$ the first to exhibit p-type conductivity[62]. NiO oxide has been studied as well[63], nevertheless, as with the delafossite Cu-based oxides only poor TFT performance has been reported.

Binary copper oxides, Cu_2O and CuO are both p-type semiconductors, with Cu_2O being know as a p-type semiconductor since 1917, when Kennard et al. demonstrated its semiconductor properties[64]. As previously described, hole conduction in oxides is difficult as most of them have a VB mainly composed of O *2p* orbitals[65]. Cu_2O and SnO are the most promising materials to be used as p-type semiconductors, based on the fact that they both show orbital hybridization in the VBM. The orbital hybridization in Cu_2O and CuO arises from the equal contributions of the Cu *3d* and O *2p* orbitals at the VBM[66-68], while its p-type character is attributed to the copper vacancies[69]. Cupric oxide (CuO), which is also a p-type semiconductor, has a monoclinic crystal structure and a band gap of 1.91 to 2.1 eV. Cuprous oxide (Cu_2O) shows the cubic crystal structure and a band gap of 2.1 to 2.6 eV[67,70,71].

Thin films of copper oxides have been reported to exhibit very high Hall mobility, exceeding 100 $cm^2V^{-1}s^{-1}$ [67,71]. Nevertheless, TFTs with high mobility remains elusive, as control of the high carrier density has been shown to be difficult[72]. Furthermore, relative good performance on Cu_xO TFTs has been only achieved at high processing temperatures, which posses a serious challenge for devices to be fabricated in plastic substrates.

Tin monoxide, in contrast, has been reported to show good TFT performance at low processing temperatures and even flexible devices have been demonstrated[73]. A more detailed discussion on high mobility on both SnO films and devices is presented in Chapters 4 to 6. Table 2.4 summarizes the state of the art on p-type oxide thin films and TFTs, showing selected reports on the most promising p-type oxides: SnO and Cu_xO.

	Technique	T_{dep} (°C)	T_{post} (°C)	Substrate	Dielectric	Mobility ($cm^2V^{-1}s^{-1}$)		I_{ON}/I_{OFF}	Reference	Year
						Hall	Field-effect			
SnO_x	PLD[a]	575	200	YSZ	Al_2O_x	2.6	1.3	10^2	Ogo *et al.*[58]	2008
	rf sputtering	RT	400	Si	SiN_x		0.24	10^2	Yabuta *et al.*[74]	2010
	evaporation	RT	400	Si	SiO_2		0.87	10^2	Liang *et al.*[75]	2010
	rf sputtering	RT	200	Glass	ATO[b]	4.8	1.2	10^3	Fortunato *et al.*[60]	2010
	rf sputtering	RT	200	Glass	ATO	4.8	4.6	10^4	Fortunato *et al.*[76]	2011
	solution processed	RT	500	Si	SiO_2		0.13	85	Okamura *et al.*[77]	2012
	dc sputtering	RT	180	Glass	HfO_2	18.71	6.75	10^4	Caraveo-Frescas *et al.*[73]	2013
	dc sputtering	RT	180	Polyimide	HfO_2	18.71	5.87	10^3	Caraveo-Frescas *et al.*[73]	2013
Cu_xO	PLD	700		MgO	Al_2O_x	100	0.26	6	Matsuzaki *et al.*[67]	2008
	rf sputtering	RT	200	Si	SiO_2		0.4	10^4	Sung *et al.*[68]	2010
	PLD	500		Si-SiO_2	HfON	107	4.3	10^6	Zou *et al.*[78]	2010
	rf sputtering	RT	200	Glass	ATO	18.47	0.0012	10^2	Fortunato *et al.*[72]	2010
	PLD	500		Si-SiO_2	HfO_2		2.7	10^6	Zou *et al.*[79]	2011

Table 2.4. State of the art on p-type oxides. [a]Pulsed laser deposition. [b]Bilayer of TiO_2 and Al_2O_3. *Adapted from Fortunato et al*[36].

2.3 Thin-Film Transistors

Display technology is the main area of application for thin-film transistors (TFTs), specifically as switching/driving current elements in backplanes of flat panel displays, such as liquid crystal displays (LCD) or active matrix organic light-emitting diode (AMOLED) screens[1,2]. Nevertheless, TFTs may constitute the building blocks for the development of a wide range of applications on the emerging field of transparent electronics. In this section, TFT structure and fabrication is briefly described, followed by the basis of TFT operation. Basic device physics are also introduced and the operation of TFTs is compared with that of the well-known metal-oxide-semiconductor field-effect transistors (MOSFETs). As most of this research work is focused on p-type oxide semiconductors, the description of device physics in done for a p-channel TFT.

2.3.1 Device Structure and Fabrication

A thin-film transistor is a field-effect device comprised of thin-film layers of amorphous or polycrystalline materials. The basic structure of a TFT consists of a semiconducting layer connected by conducting source and drain electrodes with a dielectric material between the gate electrode and the semiconductor. Figure 2.13 illustrates the conventional structures used for TFT fabrication[80]. In a coplanar structure the source and drain electrodes and the dielectric are on the same side of the channel (the channel is in direct contact to source and drain electrodes, allowing current to flow horizontally in a single plane). In a staggered configuration, source and drain electrodes are on the opposite side of the channel from the insulator (current first flows in two planes: first vertically to the

channel then horizontally from source to drain). The position of the gate electrode defines the top-gate (normal) or bottom-gate (inverted) configuration.

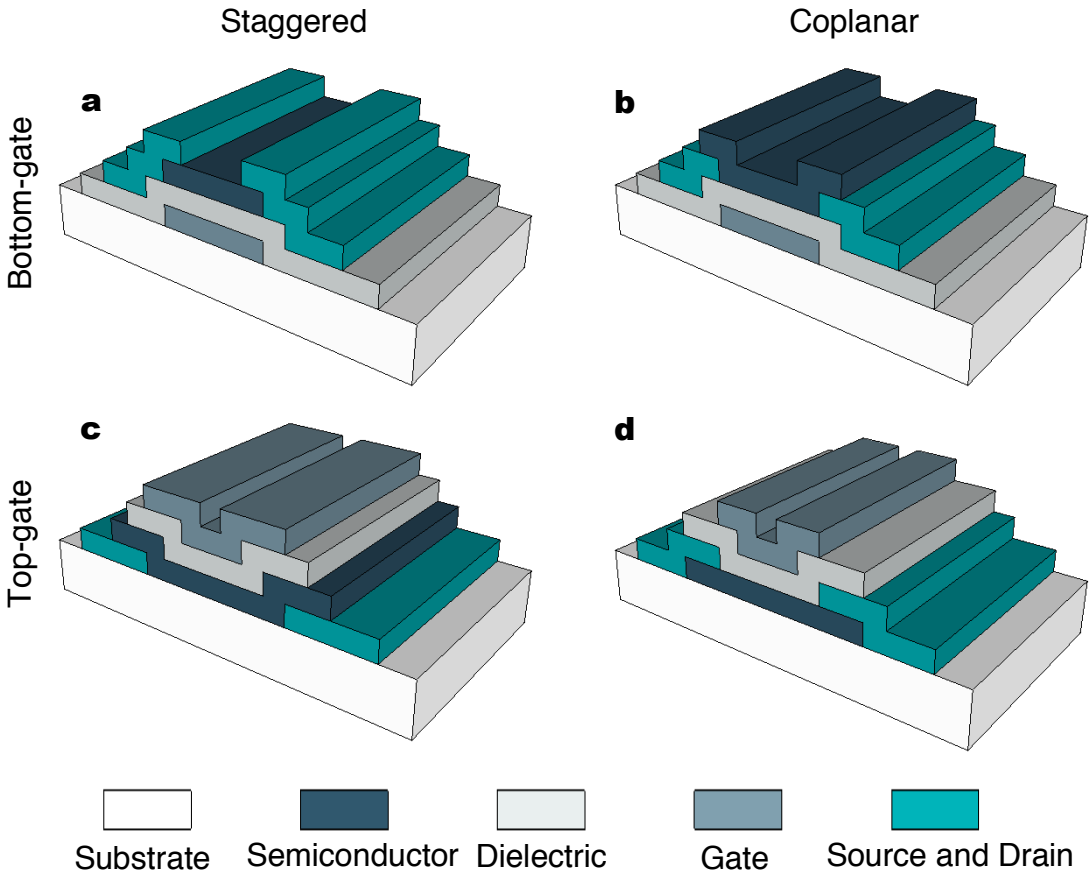

Figure 2.13 Conventional TFT structures. a, Staggered bottom-gate; **b,** coplanar bottom-gate; **c,** staggered top-gate. **d,** coplanar top-gate.

Each structure presents advantages and disadvantages mainly depending on the materials involved in the TFT fabrication. Top-gate structures, are normally preferred when a given material (*e.g.* semiconductor) requires high processing temperatures that may damage the previously deposited layers (*e.g.* dielectric and/or source and drain electrodes). Top-gate configuration is also preferred when a flat, continuous layer (normally with low surface

roughness) without any layer underneath is desired. For instance, coplanar top-gate configuration is the standard structure for the fabrication of TFTs based on poly-Si as the active layer (semiconductor). The processing temperature of poly-Si could be as high as 1000 ^{o}C that requires to be the first deposited layer in order to prevent damage to the remaining layers[81]. In contrast, TFTs based on a-Si:H are fabricated with the staggered bottom-gate configuration. The lower processing temperatures of a-Si:H allows the fabrication of TFTs with this structure that allows better device performance for a-Si:H[81]. This structure is also advantageous to protect the light-sensitive a-Si:H layer from backlight exposure when used in displays, as the gate electrode protects a-Si:H blocking the light. In the bottom gate structures, having the semiconductor surface exposed to air is either advantageous or disadvantageous depending on the material itself. This structure is therefore preferred when further processing (*e.g.* post-annealing in a suitable atmosphere) is used to modify the semiconductor properties[82].

TFTs are deposited in a substrate (typically insulating such as glass) that acts as a supporting element, but that is not an active part of the device as it is in high performance applications using bulk crystalline materials (*e.g.* Si CMOS technology). Figure 2.14 shows the typical structures of TFTs and metal-oxide-semiconductor field-effect transistors (MOSFETs).

The performance of TFTs is inferior compared to MOSFETs primarily due to a larger number of defects in the semiconducting layer in TFTs. In MOSFETs, carriers flow in a single crystalline semiconductor while in TFTs flow in either polycrystalline or amorphous layers. Higher carrier scattering is therefore present in TFTs. Surface defects are extremely

detrimental to device performance[83,84]. In TFTs, the semiconductor layer is so thin than surface defects might extend across the entire film layer. On TFTs, two surfaces (top and bottom) influence the device performance while in bulk devices, there is only one surface (semiconductor/dielectric) influencing it.

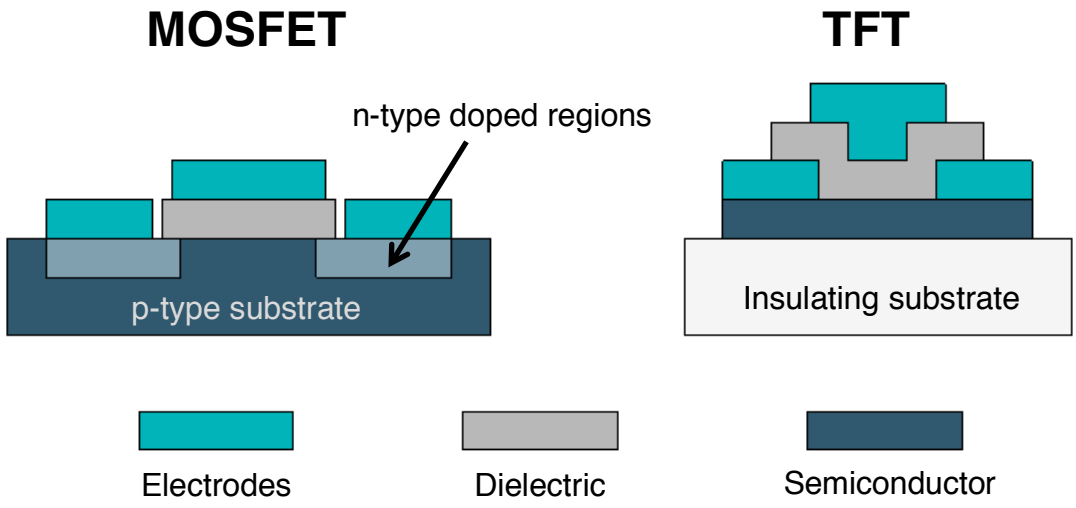

Figure 2.14. Comparison between typical structures of TFTs and MOSFETs. The single crystal Si wafer used in MOSFETs is both the substrate and the semiconductor.

Fabrication temperature is another difference between TFTs and MOSFETs. While in MOSFETs processing temperatures may exceed 1000 °C, in TFTs processing temperatures are restricted to substrate softening temperature[80]. TFTs are commonly fabricated on glass substrates, which can normally withstand temperatures as high as 600-650 °C. Nevertheless, if flexible plastic substrates are used, the maximum processing temperature drops to around 140-200 °C.

2.3.2 Device Operation

The basic principle of a field-effect device is to control the flow of electrons (or holes) from source to drain by the modulation of a conductive channel. This modulation is achieved by the injection of carriers near the semiconductor/dielectric interface[85], through the voltage applied on the gate electrode that forms a parallel plate capacitor structure along with the gate dielectric and semiconductor.

Channel modulation in TFTs is achieved by the formation of *accumulation* layer (*i.e.* holes accumulated at the p-type semiconductor/dielectric interface), while in MOSFETs, which have p-n junctions, is achieved by the formation of on an *inversion* layer, that is, electron-conduction (n-type channel) in a p-type semiconductor.

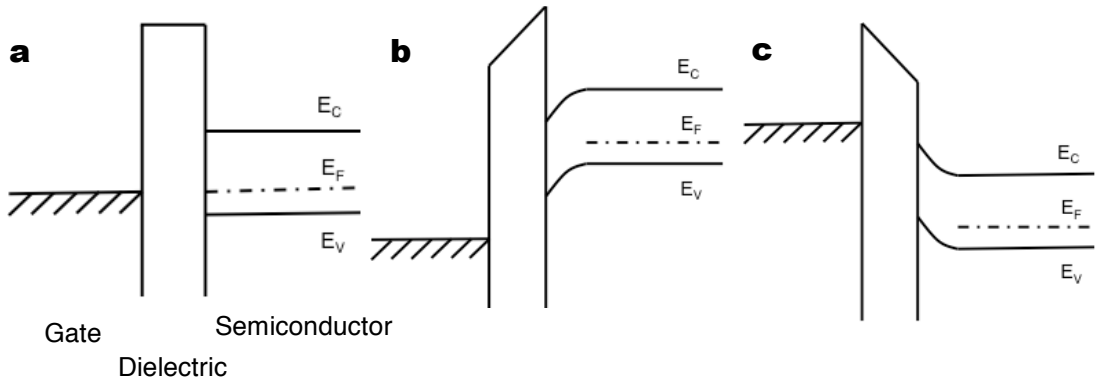

Figure 2.15 Energy band diagrams. A MOS capacitor with a p-type semiconductor under different gate bias**: a,** equilibrium (V_{GS}=0 V); **b,** depletion (V_{GS}>0 V); **c,** accumulation (V_{GS}<0 V).

The energy band diagram of the metal-oxide-semiconductor (MOS) capacitor formed by the gate electrode, the gate dielectric and the semiconductor is useful to describe the basic operation of a TFT. The following analysis presents the ideal case for a p-type semiconductor. Figure 2.15a shows the energy band diagram under 0 V applied to the gate

electrode (equilibrium), while in Figure 2.15b a positive gate-source voltage (V_{GS}) is applied (depletion). When V_{GS}>0 V (depletion) the positive bias repels the mobile holes in the semiconductor, giving rise to a depletion region near the semiconductor/dielectric interface. If V_{GS} >> 0 V the depletion region can extend through the whole semiconductor. Under positive bias, there are few mobile holes in the semiconductor, resulting in a channel with very low conductance. For the situations illustrated in Figs. 2.15a and 2.15b, if drain-source voltage (V_{DS}) is applied, only a very low drain-source current (I_{DS} or simply I_D) will flow. The lack of current flow is the *OFF*-state of the transistor. In contrast, Figure 2.15c shows an energy band diagram at accumulation, that is, a negative V_{GS}. The applied negative bias attracts mobile holes giving rise to an accumulation region near the semiconductor/dielectric interface, and leading to an increase in the channel conductance. Under this condition, when a V_{DS} is applied, a considerable I_{DS} flows (*ON*-state). In the ideal case, a very small negative $|V_{GS}|$ is enough to form a conductive channel. However, in the real case the V_{GS} required to form a conductive channel, defined as the threshold voltage (V_T) deviates from the ideal value of zero and its magnitude largely depends on the difference between the work functions of the gate and the semiconductor; semiconductor background carrier concentration; and the density of trapped charges in the dielectric, the semiconductor and the dielectric/semiconductor interface[82,86].

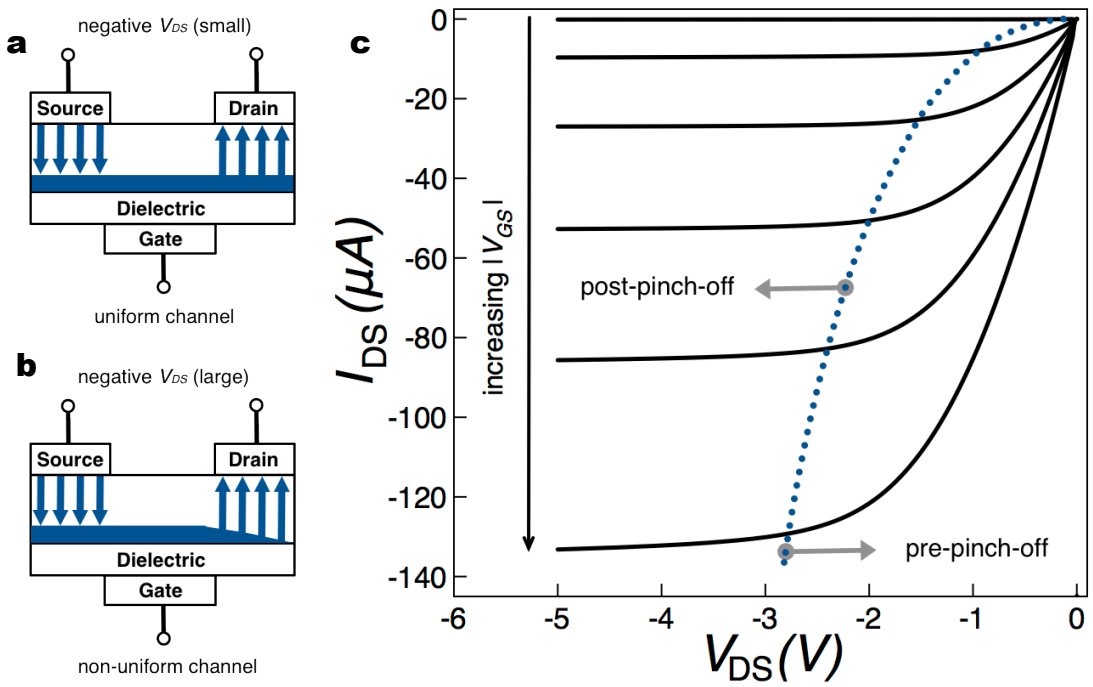

Figure 2.16 Channel in the *ON*-state. Schematics of TFT operation regions in the *ON*-state. **a,** Linear region, pre-pinch-off ($-V_{DS} \leq -V_{GS} + V_T$); **b,** saturation region, post-pinch-off ($-V_{DS} > -V_{GS} + V_T$). **c,** plot of I_{DS} versus V_{DS} for different V_{GS}.

The *ON*-state of the transistor can be described in two regimes according to the value of the drain-source voltage (V_{DS}):

1. **Linear region.** A conductive channel formed and current flows between the drain and source. In this regime, the accumulated charges are uniformly distributed throughout the channel (Fig. 2.16a) and it is also known as the pre-pinch-off regime. The TFT behaves as a resistor, with a linear increment in the current with respect to V_{DS}.

   This regime occurs when $-V_{DS} \leq -V_{GS} + V_T$ and the drain to source current is modeled as:

$$I_{DS} = -\mu_{FE} C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \quad (2.6)$$

Where μ_{FE} is the field-effect mobility, C_{ox} is the gate dielectric capacitance per unit area, W is the channel width and L is the channel length.

2. **Saturation region.** In this regime, the drain voltage is higher than the gate voltage causing the carriers to spread out from the narrow channel created during the linear regime. Current flows in a broader region than just the semiconductor/dielectric interface. Near the drain electrode a lack of channel region (Fig. 2.16b) results from the depletion of the charges in the accumulation layer near this electrode, and is defined as pinch-off.

   This regime occurs when $-V_{DS} > -V_{GS} + V_T$. I_{DS} saturates (also defined as the post-pinch-off regime) being now primarily controlled by the gate-source voltage, and described approximately by:

$$I_{DS} = -\mu_{sat} C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \quad (2.7)$$

where μ_{sat} is the saturation mobility. Figure 2.16c illustrates the ON-state regimes of a p-type TFT in a plot of I_{DS} versus V_{DS} for different V_{GS}.

The equations used to describe the operation of TFTs are based in the ideal square-law model[82,87], which relies on the three major assumptions:

1. The electric field perpendicular to the channel is much greater than the electric field parallel to the channel, that is, the channel is seen as one-dimensional[88] also known as the gradual channel approximation[89].
2. Linear variation of the charge in the channel with respect to applied gate bias.
3. All induced charge is due to free carries having a uniform mobility.

Even though the first assumption is not valid during saturation near the drain region, equations 2.6 and 2.7 are the standard ones used to describe the operation of TFTs given that the device has channel L much larger than the dielectric thickness[90].

TFTs, just like MOSFETs can operate as *enhancement*-mode or *depletion*-mode devices. The former is defined as normally off device, that is, negligible I_{DS} flows at V_{GS}=0 V; while the last is defined as normally on device, where some I_{DS} flows at V_{GS}=0. Turning off a depletion-mode device can be done by applying a V_{GS} of the opposite polarity (i.e. positive V_{GS} for p-type TFTs). While both operation modes are useful for certain applications, enhancement-mode is preferred, as it doesn't require power to turn off facilitating circuit design and dissipating less power when in a standby mode[84,91].

2.4 References

1 Ginley, D. S., Hosono, H. & Paine, D. C. *Handbook of Transparent Conductors* (Springer, 2010).

2 Facchetti, A. & Marks, T. J. *Transparent electronics: from synthesis to applications*. (John Wiley & Sons, 2010).

3 Chopra, K. L., Major, S. & Pandya, D. K. Transparent conductors -a status review. *Thin Solid Films* **102**, 1-46 (1983).

4 Dawar, A. L. & Joshi, J. C. Semiconducting transparent thin films: their properties and applications. *Journal of Materials Science* **19**, 1-23 (1984).

5 Fortunato, E., Ginley, D., Hosono, H. & Paine, D. C. Transparent conducting oxides for photovoltaics. *MRS Bulletin* **32**, 242-247 (2007).

6 Exarhos, G. J. & Zhou, X.-D. Discovery-based design of transparent conducting oxide films. *Thin Solid Films* **515**, 7025-7052 (2007).

7 Freeman, A. J., Poeppelmeier, K. R., Mason, T. O., Chang, R. P. H. & Marks, T. J. Chemical and thin-film strategies for new transparent condcuting oxides. *MRS Bulletin* **25**, 45-51 (2000).

8 Mryasov, O. N. & Freeman, A. J. Electronic band structure of indium tin oxide and criteria for transparent conducting behavior. *Physical Review B* **63**, 233 111 (2001).

9 Mizoguchi, H. & Woodward, P. M. Electronic structure studies of main group oxides possessing edge-sharing octahedra: implications for the design of transparent conducting oxides. *Chemistry of Materials* **16**, 5233-5248 (2004).

10 Medvedeva, J. E. Unconventional approaches to combine optical transparency with electrical conductivity. *Applied Physics A* **89**, 43-47 (2007).

11 Hamberg, I. & Granqvist, C. G. Evaporated Sn-doped In2O3 films: Basic optical properties and applications to energy-efficient windows. *Journal of Applied Physics* **60**, R123 (1986).

12 Bellingham, J. R., Phillips, W. A. & Adkins, C. J. Intrinsic performance limits in transparent conducting oxides. *Journal of Materials Science Letters* **11**, 263-265 (1992).

13 Coutts, T. J., Young, D. L. & Li, X. Characterization of transparent conducting oxides. *MRS Bulletin* **25**, 58-65 (2000).

14 Barquinha, P., Pereira, L., Gonçalves, G., Martins, R. & Fortunato, E. The Effect of Deposition Conditions and Annealing on the Performance of High-Mobility GIZO TFTs. *Electrochemical and Solid-State Letters* **11**, H248-H251 (2008).

15 Suresh, A., Wellenius, P., Dhawan, A. & Muth, J. Room temperature pulsed laser deposition indium gallium zinc oxide channel based transparent thin film transistors. *Applied Physics Letters* **90**, 123512 (2007).

16 Kang, D. *et al.* Effect of Ga/In ratio on the optical and electrical properties of GaInZnO thin films grown on SiO2/Si substrates. *Applied Physics Letters* **91**, 091910 (2007).

17 Hosono, H., Nomura, K., Ogo, Y., Uruga, T. & Kamiya, T. Factors controlling electron transport properties in transparent amorphous oxide semiconductors. *Journal of Non-Crystalline Solids* **354**, 2796-2800 (2008).

18 Iwasaki, T. *et al.* Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: An application to amorphous oxide semiconductors in In-Ga-Zn-O system. *Applied Physics Letters* **90**, 242114 (2007).

19 Dehuff, N. L. *et al.* Transparent thin-film transistors with zinc indium oxide channel layer. *Journal of Applied Physics* **97**, 064505 (2005).

20 Barquinha, P. *et al.* Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide. *Journal of Non-Crystalline Solids* **352**, 1749-1752 (2006).

21 Yagiloglu, B., Yeom, H. Y., Beresford, R. & Paine, D. C. High-mobility amorphous In2O3-10 wt%ZnO thin film transistors. *Applied Physics Letters* **89**, 062103 (2006).

22 Paine, D. C., Yaglioglu, B., Beiley, Z. & Lee, S. Amorphous IZO-based transparent thin film transistors. *Thin Solid Films* **516** (2008).

23 Chiang, H. Q., Wager, J. F., Hoffman, R. L., Jeong, J. & Keszler, D. A. High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer. *Applied Physics Letters* **86**, 013503 (2005).

24 Hoffman, R. L. Effects of channel stoichiometry and processing temperature on the electrical characteristics of zinc tin oxide thin-film transistors. *Solid-State Electronics* **50**, 784-787 (2006).

25 Gorn, P. *et al.* Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes. *Advanced Materials* **18**, 738 (2006).

26 Jackson, W. B., Hoffman, R. L. & Herman, G. S. High-performance flexible zinc tin oxide field-effect transistors. *Applied Physics Letters* **87**, 193503 (2005).

27 Minami, T. Transparent conducting oxide semiconductors for transparent electrodes. *Semiconductor Science and Technology* **20**, S35-S44 (2005).

28 SharpCorporation. Sharp announces production of world's first IGZO LCD panels. http://www.macdailynews.com (2012).

29 Gordon, R. G. Criteria for choosing transparent conductors. *MRS Bulletin* **25** (2000).

30 Granqvist, C. G. Transparent conductors as solar energy materials: a panoramic review. *Solar Energy Materials and Solar Cells* **91**, 1529-1598 (2007).

31 Karlsson, J. & Roos, A. Annual energy window performance vs. glazing thermal emittance -the relevance of very low emittance values. *Thin Solid Films* **392**, 345-348 (2001).

32 Pilkington Group Limited, S. H., UK WA10 3TT. Pilkington and the flat glass industry. http://www.pilkington.com (2010).

33 Research and Markets, G. C., Taylors Lane, Dublin 8, Ireland. China Low-e Glass Market Report. http://www.researchandmarkets.com/reports (2010).

34 Frost & Sullivan. World Flat Panel Display Markets. http://www.electronics.frost.com (2012).

35 Displaybank. Display Market Forecast. http://www.displaybank.com (2012).

36 Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **24**, 2945-2986 (2012).

37 Phys.org/news. *Samsung shows transparent 46-inch LCD panel*, 2012).

38 Granqvist, C. G., Azens, A., Heszler, P., Kish, L. B. & Osterlund, L. Nanomaterials for bening indoor environments: Electrochromics for "smart windows" sensors for air quality, and photo-catalysts for air cleaning. *Solar Energy Materials and Solar Cells* **91**, 355-365 (2007).

39 Granqvist, C. G. *Handbook of Inorganic Electrochromic Materials*. (Elsevier, 1995).

40 Newswire, P. PPG Aerospace Awarded Boeing Contract for Electrochromic Cabin Window Systems. http://www.prnewswire.com/news (2010).

41 Granqvist, C. G., Avendaño, E. & Azens, A. Electrochromic coatings and devices: survey of some recent advances. *Thin Solid Films* **442**, 201-211 (2003).

42 Batzill, M. & Diebold, U. The surface and materials science of tin oxide. *Prog. Surf. Sci.* **79**, 47-154 (2005).

43 Zhao, G. Y., Zhi, X., Ren, Y. & Zhu, T. in *Eco-materials processing and design X* Vol. 620-622 (eds H. Kim, J. F. Yang, T. Sekino, & S. W. See) 5 (Trans Tech Publications, 2009).

44 Ihokura, K. & Watson, J. *The Stannic Oxide Gas Sensor: Principles and Applications*. (CRC Press, 1994).

45 Li, H., Huang, X. & Chen, L. Direct Imaging of the Passivating Film and Microstructure of Nanometer-Scale SnO Anodes in Lithium Rechargeable Batteries. *Electrochemical and Solid-State Letters* **1**, 241-243 (1998).

46 Aurbach, D. *et al.* Nanoparticles of SnO Produced by Sonochemistry as Anode Materials for Rechargeable Lithium Batteries. *Chemistry of Materials* **10**, 4155-4163 (2002).

47 Baker, W. S. *et al.* Enhanced Oxygen Reduction Activity in Acid by Tin-Oxide Supported Au Nanoparticle Catalyst. *Journal of The Electrochemical Society* **153**, A1702-A1707 (2006).

48 Ifeacho, P., Huelser, T., Wiggers, H., Schulz, C. & Roth, P. Synthesis of SnO2-x nanoparticles tuned between $0 \leq x \leq 1$ in a premixed los pressure H2/O2/Ar flame. *Proceedings of the Combustion Institute* **31**, 1805-1812 (2007).

49 Luxmann, L. & Dobner, R. *Metallurgy* **34**, 821 (1980).

50 Lawson, F. Tin Oxide - Sn3O4. *Nature* **215**, 955-956 (1967).

51 Murken, G. & Trömel, M. Ueber das bei der Disproportionierung von SnO entstehende Zinnoxid, Sn2O3. *Journal of Inorganic and General Chemistry* **397**, 117-126 (1973).

52 Rossini, F. D., Wagman, D. D., Evans, W. H., Levin, S. & Jaffe, I. (ed Circular of the National Bureau of Standards 500) (U.S. Government Printing Office, Washington, DC, 1952).

53 Geurts, J., Rau, S., Richter, W. & Schmitte, F. J. SnO films and their oxidation to SnO2: Raman scattering, IR reflectivity and X-ray diffraction studies. *Thin Solid Films* **121**, 217-225 (1984).

54 Pannetier, J. & Denes, G. Tin(II) Oxide: structure Refinement and Thermal Expansion. *Acta Crystallographica Section B: Strcutural Crystallography and Crystal Chemistry* **36**, 2763-2765 (1980).

55 Meyer, M., Onida, G., Palummo, M. & Reining, L. Ab initio pseudopotential calculation of the equilibrium strucuture of tin monoxide. *Physical Review B* **64**, 45119-45111-45119-45119 (2001).

56 Ramik, R. A., Organ, R. M. & Mandarino, J. A. On type of romarchite and hydroromarchite from Boundary Falls, Ontario, and notes on other ocurrences. *The Canadian Mineralogist* **41**, 649-657 (2003).

57 Togo, A., Oba, F., Tanaka, I. & Tatsumi, K. First-principles calculations of native defects in tin monoxide. *Phys. Rev. B* **74**, 195128 (2006).

58 Ogo, Y. *et al.* p-channel thin-film transistor using p-type oxide semiconductor, SnO. *Appl. Phys. Lett.* **93**, 032113 (2008).

59 Ogo, Y. *et al.* Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application. *Phys. Status Solidi A* **206**, 2187-2191 (2009).

60 Fortunato, E. *et al.* Transparent p-type SnO[sub x] thin film transistors produced by reactive rf magnetron sputtering followed by low temperature annealing. *Appl. Phys. Lett.* **97**, 052105 (2010).
61 Nomura, K., Kamiya, T. & Hosono, H. Ambipolar Oxide Thin-Film Transistor. *Adv. Mater.* **23**, 3431-3434 (2011).
62 Kawazoe, H. *et al.* P-type electrical conduction in transparent thin films of CuAlO2. *Nature* **389**, 939-942 (1997).
63 Shimotani, H., Suzuki, H., Ueno, K., Kawasaki, M. & Iwasa, Y. p-type field-effect transistor of NiO with electric double-layer gating. *Applied Physics Letters* **92**, 242127 (2008).
64 Kennard, E. H. & Dieterich, E. O. An Effect of Light upon the Contact Potential of Selenium and Cuprous Oxide. *Physical Review* **9**, 58-63 (1917).
65 Yanagi, H., Kawazoe, H., Kudo, A., Yasukawa, M. & Hosono, H. Chemical Design and Thin Film Preparation of p-Type Conductive Transparent Oxides. *J. Electroceram.* **4**, 407-414 (2000).
66 Raebiger, H., Lany, S. & Zunger, A. Origins of the p-type nature and cation deficiency in Cu2O and related materials. *Physical Review B* **76**, 045209 (2007).
67 Matsuzaki, K. *et al.* Epitaxial growth of high mobility Cu2O thin films and application to p-channel thin film transistor. *Appl. Phys. Lett.* **93**, 202107 (2008).
68 Sung, S.-Y. *et al.* Fabrication of p-channel thin-film transistors using CuO active layers deposited at low temperature. *Appl. Phys. Lett.* **97**, 222109 (2010).
69 Raebiger, H., Lany, S. & Zunger, A. Origins of p-type nature and cation deficiency in Cu2O and related materials. *Phys. Rev. B* **76**, 045209 (2007).
70 Li, B. S., Akimoto, K. & Shen, A. Growth of Cu2O thin films with high hole mobility by introducing a low-temperature buffer layer. *Journal of Crystal Growth* **311**, 1102-1105 (2009).
71 Fortin, E. & Weichman, F. L. Hall Effect and Electrical Conductivity of Cu2O Monocrystals. *Canadian Journal of Physics* **44**, 1551-1561 (1966).
72 Fortunato, E. *et al.* Thin-film transistors based on p-type Cu[sub 2]O thin films produced at room temperature. *Appl. Phys. Lett.* **96**, 192102 (2010).
73 Caraveo-Frescas, J. A. *et al.* Record Mobility in Transparent p-Type Tin Monoxide Films and Devices by Phase Engineering. *ACS Nano* **7**, 5160-5167 (2013).
74 Yabuta, H. *et al.* Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits. *Appl. Phys. Lett.* **97**, 072111(2010).
75 Liang, L. Y. *et al.* Phase and Optical Characterizations of Annealed SnO Thin Films and Their p-Type TFT Application. *Journal of The Electrochemical Society* **157**, H598-H602 (2010).
76 Fortunato, E. & Martins, R. Where science fiction meets reality? With oxide semiconductors! *Physica Status Solidi Rapid Research Letters* **5**, 336-339 (2011).
77 Okamura, K., Nasr, B., Brand, R. A. & Hahn, H. Solution-processed oxide semiconductor SnO in p-channel thin-film transistors. *Journal of Materials Chemistry* **22**, 4607-4610 (2012).
78 Zou, X. *et al.* Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-k HfON Gate Dielectric. *Electron Device Letters, IEEE* **31**, 827-829 (2010).
79 Zou, X. *et al.* Improved subthreshold swing and gate-bias stressing stability of p-type Cu2O thin-film transistors using a HfO2 high-k gate dielectric grown on a SiO2/Si

substrate by pulsed laser ablation. *IEEE Transactions on Electron Devices* **58**, 2003-2007 (2011).
80 Kagan, C. R. & Andry, P. *Thin-Film Transistors*. (Marcel Dekker, Inc., 2003).
81 Lee, J.-H., Liu, D. N. & Wu, S.-T. *Introduction to Flat Panel Displays*. (John Wiley & Sons Ltd., 2008).
82 Tickle, A. C. *Thin-Film Transistors -A New Approach to Microelectronics*. . (Wiley, 1969).
83 Hoffman, R. L. *Development, Fabrication, and Characterization of Transparent Electronic Devices* Masters thesis, Oregon State University, (2002).
84 Hong, D., Yerubandi, G., Chiang, H. Q., Spiegelberg, M. C. & Wager, J. F. Electrical Modeling of Thin-Film Transistors. *Critical Reviews in Solid State and Materials Sciences* **33:2**, 101-132 (2008).
85 Barquinha, P. M. C. *Transparent Oxide Thin-Film Transistors: production, characterization and integration* PhD thesis, Universidade Nova de Lisboa, (2010).
86 Yang, E. S. *Microelectronic Devices*. (McGraw Hill, 1988).
87 Pierret, R. F. *Semicondcutor Fundamentals*. (Addison-Wesley, 1996).
88 Sze, S. M. *Physics of Semiconductor Devices*. 2nd edn, (John Wiley & Sons, Inc., 1981).
89 Weimer, P. K. in *Field-Effect Transistors: Physics, Technology, and Applications* (eds J.T. Wallmark & H. Johnson) 216-252 (Prentice-Hall, 1966).
90 Ytterdal, T., Cheng, Y. & Fjeldly, T. A. *Device Modeling for Analog and RF CMOS Circuit Design*. (John Willey & Sons, Ltd., 2003).
91 Hoffman, R. L., Norris, B. J. & Wager, J. F. ZnO-based transparent thin-film transistors. *Applied Physics Letters* **82**, 733 (2003).

Chapter 3

Experimental Techniques

Chapter 3 describes the experimental techniques used for the deposition and characterization of thin films, as well as techniques employed for the fabrication of field effect devices. As this dissertation is mainly focus on the fabrication of thin film transistors, the final section of this chapter is dedicated to discuss the adequate device characterization protocol for oxide-based TFTs.

3.1 Thin-film Processing

This section describes the thin-film deposition and post deposition techniques used throughout this research work. Reactive sputtering is the central technique used for the deposition of p-type oxide semiconductors. Electron-beam evaporation, atomic layer deposition and plasma-enhanced chemical vapor deposition are used to fabricate the different layers of field-effect devices and are briefly described along with post deposition annealing.

3.1.1 Magnetron Sputtering

Sputtering is a physical vapor deposition (PVD) technique that utilizes ion bombardment to eject atoms from a solid material. Atoms or molecules are physically removed from a source material, known as the target, to be deposited in a substrate after

being transported through the vacuum. The atoms are ejected from the surface of the target as a result collisions and momentum transfer from the impinging highly energetic particles created during the ionization of a gaseous species. The sputtered atoms are directed to the substrate by an electric field, where they form a thin-film[1,2].

The process begins in a vacuum chamber having two electrodes, the cathode (target) and the anode (substrate). An inert gas (usually Argon) is then flown to the chamber and an electric field applied to the electrodes. Under the applied electric field, electrons are accelerated towards the anode (+) colliding with the atoms of the gas, giving rise to two main reactions, which depend on the transferred energy during the collision[1,3]:

1. Electronic excitation: $e^- + Ar \rightarrow Ar^* + e^-$
2. Ionization: $e^- + Ar \rightarrow Ar^+ + 2e^-$

The ionization reaction creates additional electrons that may create subsequent electronic excitation and ionization reactions leading to the formation of a glow discharge (the plasma region in which a degree of ionization is sustained by the presence of energetic electrons[4]). Ions are accelerated towards the cathode leading to the ejection of atoms from the source material (target). Secondary electrons are emitted from the surface, allowing the glow discharge to be sustained, as a result of the ions striking the cathode. The ejected atoms travel through vacuum to the anode, where they condense giving rise to the thin film. A heated substrate may be used to improve/modify the properties of the film. Secondary electrons may reach the substrate causing structural damage to the growing film[4]. In order to avoid that, magnets are placed behind the target, which confine the electrons near the target surface. The presence of the magnetic field not only prevents damage to the substrate, but

also helps increasing the probability of ionization of the inert gas, resulting in higher deposition rates[1]. Figure 3.1a summarizes the description of magnetron sputtering.

Thin films can also be deposited by reactive magnetron sputtering, in which a reactive gas, in addition or substitution of the inert one, is flown to the chamber. For instance, thin films of transparent p-type oxide semiconductors described in this work, are deposited by sputtering metallic targets in an oxidizing atmosphere. Figure 3.1b illustrates the concept of reactive sputtering, in which the ejected atoms react with the oxygen-containing atmosphere to form a thin film of metal oxide. Reactive sputtering is very useful for stoichiometry control of the deposited films as well as for the deposition of different oxide phases as will be presented later.

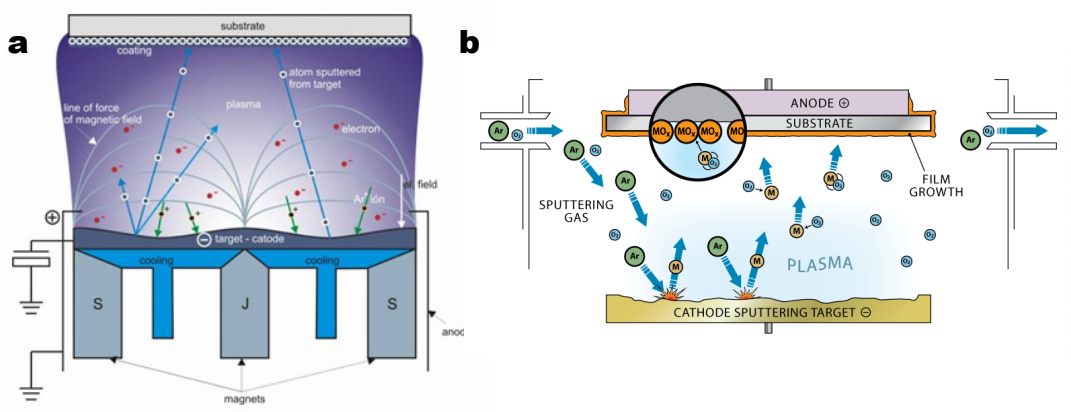

Figure 3.1. Magnetron Sputtering. a, Phenomena occurring during the sputtering process. *From Arzuffi SRL*[5]; **b,** Schematic of reactive sputtering. *From clear metals Inc.*[6]

When a direct current (dc) electrical excitation is used, the process is known as a dc magnetron sputtering. It is the simplest method, as a dc voltage is applied between the cathode and the anode, nevertheless it is restricted to conductive materials, as insulating materials are not able to supply enough secondary electrons to sustain the glow discharge[1,7]. To overcome this issue, radio frequency (rf) magnetron sputtering is employed. In this

process a high frequency (13.56 MHz) voltage is supplied to the target to attract electrons from the glow discharge during the positive pulse of the rf signal. Both conductive and insulating materials can be deposited by rf magnetron sputtering.

Sputtering deposition is a complex function of gas flow, deposition pressure, sputtering power, target to substrate distance, and deposition temperature, as shown later in this dissertation.

At the *Functional Nanomaterials and Devices Laboratory*, sputtering is performed in a custom-made AMOD-model system form Angstrom Engineering[8]. The system is a semi-cylindrical, stainless steel chamber equipped with a load lock chamber. High vacuum ($<1\times10^{-7}$ Torr) is achieved by a turbo pump. The system is equipped with four 2" sputtering guns, two *dc* and 2 *rf* with maximum 1000 Watts dc power and 300 Watts rf power. Three independent mass flow controllers allow flowing gas to the chamber with a maximum flow rate of 50 sccm (standard cubic centimeters per second) of Ar, 20 sccm Oxygen, and 20 sccm Nitrogen. All the films are deposited at room temperature with a substrate to target distance of 21 cm and under substrate rotation at 30 rpm (revolutions per minute) to ensure uniformity up to 12cmX12cm substrates.

p-type materials on this study are deposited by *dc* reactive sputtering using a metal target of the appropriate material under different conditions given by

- Relative oxygen partial pressure (O_{PP}). In a mixture of argon and oxygen gasses, where $O_{PP} = P_{O_2}/(P_{O_2} + P_{Ar})$.
- Deposition pressure (P). Ranging from 1 mTorr to 10 mTorr

- dc/rf power. 1000 watts maximum dc power, 300 watts maximum rf power

Indium tin oxide (ITO) layers are deposited by rf sputtering in an argon atmosphere under the following conditions:

Parameter	Value
rf power (W)	80
Deposition pressure (mTorr)	2
Argon flow rate (sccm)	15
Temperature (°C)	25
Deposition rate (nm/min)	2

Table 3.1. ITO sputtering deposition conditions.

3.1.2 Electron-beam Evaporation

Electron-beam evaporation (e-beam for short) is a PVD technique widely used for the thin-film deposition of a variety of materials[7,9]. E-beam evaporation heats up a material up to its vaporization point by using a high-energy (5-30 kV) electron beam. The evaporated material condenses back to a solid thin film in the substrate[10]. The source material begins as a solid, but after being heated by the e-beam transform to solid phase, either by direct via (solid-vapor transition) known as sublimation, or by and indirect one (solid-liquid-vapor) known as vaporization, greatly depending on the properties of the source material. E-beam evaporation is done under high vacuum to increase the mean free path of vaporized molecules, as well as to reduce contamination of deposited films. In a conventional e-beam evaporation tool, the source material is placed in a water-cooled crucible and the electron beam is generated by thermionic emission from an incandescent filament. The e-beam is directed to the surface of the source material by applying a magnetic field. As the e-beam is

very localized, it allows the evaporation of materials with very high melting points[7,10]. Figure 3.2 illustrates the e-beam evaporation process.

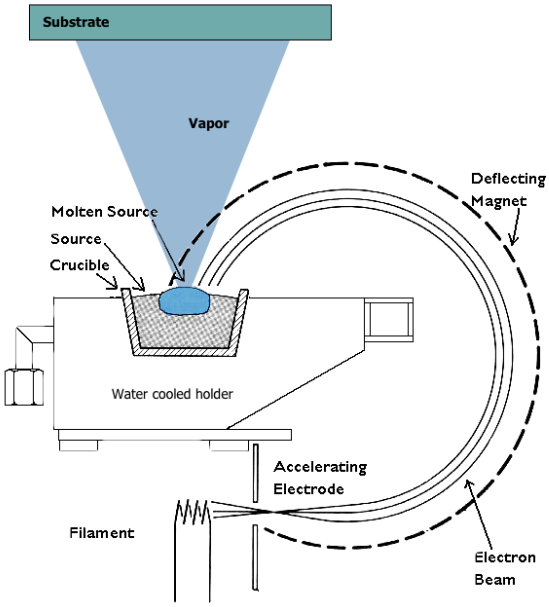

Figure 3.2. E-beam evaporation. Thin-film deposition by e-beam evaporation. *Adapted from http://www.cleanroom.byu.edu/metal.phtml*

E-beam evaporation is the main technique used in this research work to deposit metal contacts for electrical characterization of both films and devices. Table 3.2 summarizes the deposition conditions for metals used in this dissertation.

	Titanium	Gold	Nickel	Platinum
Base pressure (mTorr)	$< 5 \times 10^{-7}$	$< 5 \times 10^{-7}$	$< 5 \times 10^{-7}$	$< 5 \times 10^{-7}$
Power ramping rate (W/s)	90 sec	170	100	120
Soaking time (sec)	350	600	400	300
Deposition power* (W)	7-9%	20-30%	18-24%	30-35
Deposition temperature (^{o}C)	RT	RT	RT	RT
Substrate rotation (rpm)	30	30	30	30
Deposition rate (Å/s)	0.5	1.0	0.5	0.5

Table 3.2. E-beam evaporation deposition conditions for different metals used in this study. *Maximum deposition power, as it automatically adjusts to maintain a constant deposition rate.

3.1.3 Atomic Layer Deposition

Atomic layer deposition (ALD) is a self-limiting chemical deposition technique that uses gaseous chemicals, typically referred as precursors, in a sequential way to form monolayers of a given material[11-13]. The growth of thin-films by ALD can be described by a repetition of cycles, each of them consisting on four major steps (Fig. 3.3):

1. *Exposure of the first precursor*. The first precursor (the cationic precursor) is introduced leading to the adsorption of several monolayers onto the substrate surface.
2. *Purge of the reaction chamber*. An inert gas is flown to the reaction chamber causing desorption of the weekly bonded atoms, leaving a single monolayer on the substrate surface.
3. *Exposure of the second precursor*. The second precursor (anionic species), or another treatment to activate the surface (*e.g.* plasma), is introduced reacting with the adsorbed cationic monolayer.
4. *Purge or evacuation of the reaction chamber*. Second purge or evacuation completes the cycle.

ALD allows the conformal deposition of thin films with very good quality. For instance, high-*k* (high permittivity) oxides deposited by ALD have superior insulating properties compared to films deposited by other common deposition technique such as physical vapor deposition[13].

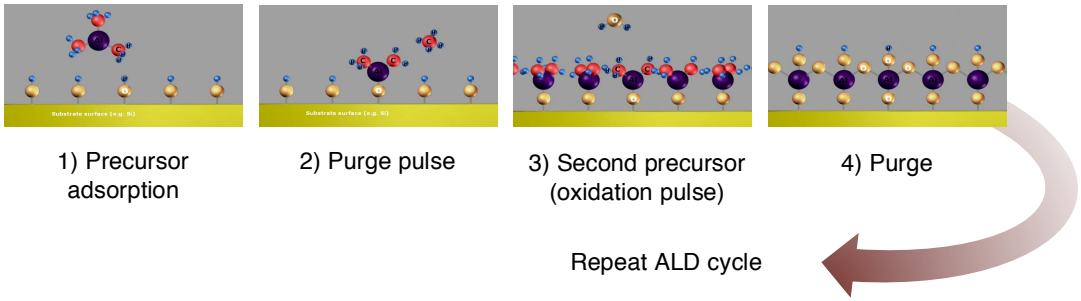

Figure 3.3. ALD. Four major steps in each cycle. *Adapted from www.laserwort.com*

Films of HfO_2 and Al_2O_3 used in this study were deposited by ALD in a Cambridge Nanotech system under the conditions given in Table 3.3.

	HfO_2	Al_2O_3
First precursor	Tetrakis(dimethylamido)hafnium (IV) ($Hf(NMe_2)_4$)	Trimethylaluminum (TMA)
Second precursor	Ozone (O_3)	H_2O
Substrate temperature	200 °C	200 °C
Growth rate	1.1 Å/cycle	1.01 Å/cycle

Table 3.3. ALD deposition conditions for different high-*k* oxides used in this study.

3.1.4 Plasma Enhanced Chemical Vapor Deposition

In chemical vapor deposition (CVD) processes a thin-film is deposited in a substrate by the thermal reaction of gas precursors[9,14]. Gaseous species are introduced to the chamber where the reaction occurs resulting in the thin film deposition. In typical CVD systems the reaction is due only to applied heat, in plasma-enhanced CVD system, both heat and a glow discharge are used to drive the chemical reaction[9]. The main advantage of PECVD is that the glow discharge allows deposition at lower temperatures when compared with conventional CVD.

PECVD is used in this work to deposit silicon nitride (Si_3N_4) to be used as a gate dielectric for TFT fabrication. The precursors used are SiH_4 and NH_3 giving rise to Si_3N_4 formation via the following reaction:

$$3SiH_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12H_2(g) \quad (3.1)$$

The process is done in the PECVD system from Oxford Instruments inside KAUST NanoFab Facilities (cleanroom) using the deposition conditions given in Table 3.4.

Parameter	Value
SiH_4 flow rate	20 sccm
NH_3 flow rate	20 sccm
N_2 flow rate	980 sccm
RF Power (low frequency)	20 W 6 seconds
RF Power (high frequency)	20 W 14 seconds
Pressure	650 mTorr
Temperature	300 °C
Deposition rate	10.76 nm/min

Table 3.4. PECVD deposition conditions for low stress Si_3N_4.

3.1.5 Post Deposition Annealing

Post deposition treatments are known to modify the material's properties [9,15]. Electrical properties of TSO are especially sensitive to post annealing treatments[15]. Control over the properties of TSO can be tuned by controlling the thermal budget (the combination of the temperature and annealing time) and the annealing atmosphere. If the films are amorphous, they can undergo crystallization during the treatment. The effect of the thermal treatment on the electrical properties of p-type SnO thin films and devices will be discussed later in this thesis, as it is a crucial parameter for achieving high mobility.

Thermoscientific tubular furnaces are used for the post annealing treatments. Temperatures range from 100 °C to 300 °C, with ramping time of 6 °C/min, holding the annealing temperature for 30 min, and then cooling down to room temperature. A single-zone tubular furnace is used for the annealing treatments done in an air atmosphere, while a three-zone furnace equipped with three independent mass flow controllers is used for annealing in nitrogen, oxygen and argon atmospheres. The tube used for annealing has a diameter of 1" and samples are placed in a quartz boat.

3.2 Thin-film Characterization

This section describes the thin-film characterization techniques used throughout this research work. A brief introduction to structural and morphological, compositional, electrical, and optical characterization techniques is presented, along with the methods used to extract the important parameters of every technique.

3.2.1 X-ray diffraction

X-ray diffraction (XRD) is a fundamental structural characterization technique widely used by material's scientists. It provides important information about solid matter: whether it is amorphous or crystalline, the crystal structure of a material, which phases are present, determine any preferential orientation, and measure the size, shape and internal

stress of small crystalline regions in the material[16-18]. Briefly, the principle of XRD is that when a monochromatic x-ray beam is directed to a solid material and constructive interference (electrons in the material oscillating at the same frequency as the incident beam) occurs, a diffractogram is obtained, which is unique to every material. Constructive interference (waves in phase) is described by well-known Bragg's law:

$$n\lambda = 2dsin\theta \tag{3.2}$$

where n is an integer, λ is the x-ray wavelength, d is the distance between atomic layers in a crystal, and θ is the x-ray angle of incidence.

The position and intensity of the peaks observed in the XRD pattern are then compared with a database to identify the material under observation, as well as the phase or phases present.

X-ray diffraction patterns in this study are obtained using a high-resolution XRD Bruker D8 Discover diffractometer using CuKα_1 (λ=1.5406 Å) radiation. XRD is primarily used to identify the phase(s) of the oxide materials used in this dissertation and to obtain the degree of preferential orientation, the crystallite size (D) and lattice strain (ε) of tin monoxide films.

Crystallite size and lattice strain are simultaneously calculated on the basis of the integral breadth (β) of the diffraction patterns (Fig. 3.4a) by using a least-squares method to account for the β of all diffraction conditions according to[16]:

$$\beta_t \approx \left(\frac{0.9\,\lambda}{D cos\theta}\right)^2 + (4\varepsilon tan\theta)^2 + \beta_o^2\,, \tag{3.3}$$

where λ is the CuKα_1 line and β_o is the instrumental broadening.

Using a MATLAB routine, the integral breadth, defined as the total area under the peak divided by the peak height (Fig. 3.4b), is obtained for every observed diffraction peak. With the obtained values and using equation (3.3), equal number of equations (seven for SnO films) with three unknowns (D, ε and β_o) are formed and solved using the least-squares method in MATLAB.

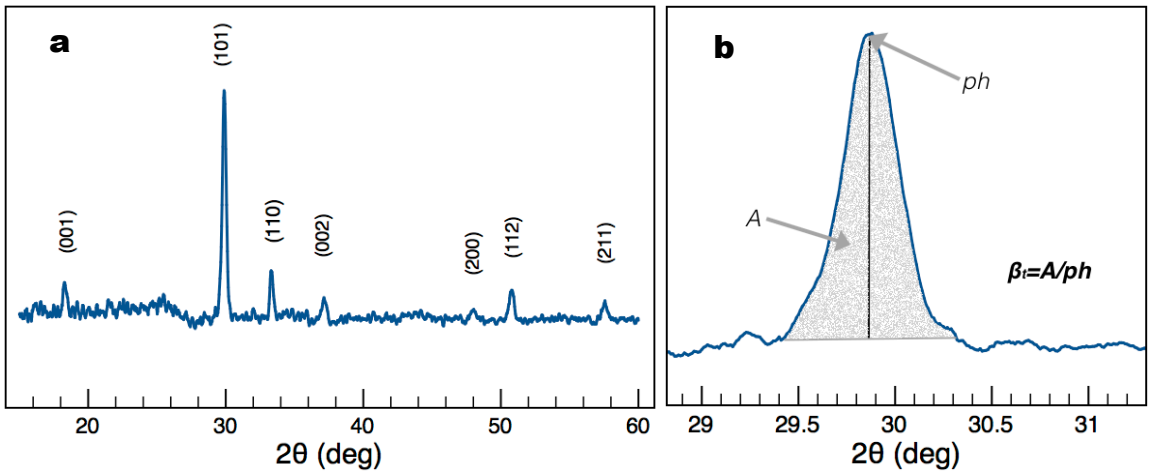

Figure 3.4. XRD Pattern. a, XRD pattern of single phase SnO, showing seven diffraction conditions. **b,** The integral breadth (β_t) defined as the total area under the peak (A) divided by the peak height (ph), was obtained for every observed diffraction condition.

3.2.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a compositional surface characterization technique. It is useful to obtain elemental composition, empirical formula, and the chemical and electronic states of elements within a material[19-21].

The basic operation principle consist of a monochromatic x-ray beam directed to a film, which causes emission of photoelectrons from the top 0.5 to 10 nm of the film. The XPS tool measures the kinetic energy of emitted electrons, $E_{kinetic}$, under ultra-high vacuum conditions, allowing the determination of the electron binding energy, $E_{binding}$, of emitted electrons according to:

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \tag{3.4}$$

where E_{photon} is the energy of the x-ray beam and ϕ is the work function of the spectrometer.

Compositional analysis is then performed from the obtained XPS spectrum (a plot of number of electrons detected versus $E_{binding}$). Each element present in the material produces a set of peaks at specific $E_{binding}$, which can be related to the existing database for identification. The relative intensity of each XPS peak, in the other hand, allows the estimation of atomic percentage values of every element present in the irradiated surface[21].

XPS spectra are recorded with an Axis Ultra DLD spectrometer (Kratos Analytical, UK), using a monochromatic Al-K_α source ($h\nu$=1486.6 eV) operating at 150 W. The spectrum analysis is done using the CASA XPS software. Shirley background subtraction and peak fitting with Gaussian–Lorentzian shaped profiles are performed for all considered photoelectron peaks.

3.2.3 Hall Effect Measurements

Hall effect is commonly used to determine the resistivity, majority carrier polarity, carrier concentration, and mobility[19,22]. The Hall effect reflects the behavior of charged particles in the presence of magnetic and electric fields (Lorentz force) given by the relation:

$$F = q(\vec{v}\times\vec{B}) \tag{3.5}$$

where q is the charge of the electron, $\vec{v}$ is the velocity vector and $\vec{B}$ is the magnetic field vector. In a Hall effect measurement four electrodes are connected to the sample in the Van der Pauw configuration[23,24], current $\vec{I}$ is injected to the sample perpendicular to the applied magnetic field by two non-adjacent electrodes (Fig. 3.5). The Lorentz force deflects the carriers toward one side of the sample, creating an electric field in the remaining electrodes that is perpendicular to both $\vec{B}$ and $\vec{I}$. At equilibrium, magnetic and electrostatic forces are balanced:

$$q(\vec{v}\times\vec{B}) = q\vec{E} \tag{3.6}$$

since $\vec{B}$, $\vec{v}$ and $\vec{I}$ are perpendicular, they can be treated as scalars and given that I is defined as

$$I = qwtNv \tag{3.7}$$

where w is the distance between the electrodes, t is the sample thickness and N is the carrier concentration. Substituting equation 3.7 in 3.6 and given that $E = V_H/w$, where V_H is defined as the Hall voltage:

$$V_H = \frac{BI}{qNt} \tag{3.8}$$

additionally, the Hall effect coefficient, R_H, can be defined as

$$R_H = \frac{tV_H}{BI} \tag{3.9}$$

The sign of the Hall effect coefficient indicates the polarity of the majority carriers[19,24]. A positive R_H indicates holes are the dominant carriers. From the Hall effect coefficient, the carrier concentration can be determined according to

$$N = \frac{1}{qR_H} \quad [\text{cm}^{-3}] \tag{3.10}$$

if the resistivity, ρ, is known the Hall mobility can be obtained from

$$\mu_{Hall} = \frac{R_H}{\rho} \quad [\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}] \tag{3.11}$$

Hall mobility is related to conductivity mobility by

$$\mu_{Hall} = r\mu \tag{3.12}$$

where *r* is the scattering factor defined as

$$r = \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \tag{3.13}$$

and τ is the scattering factor defined as the mean time between scattering events. R has a value of 1.18 for lattice scattering and 1.93 for impurity scattering[19].

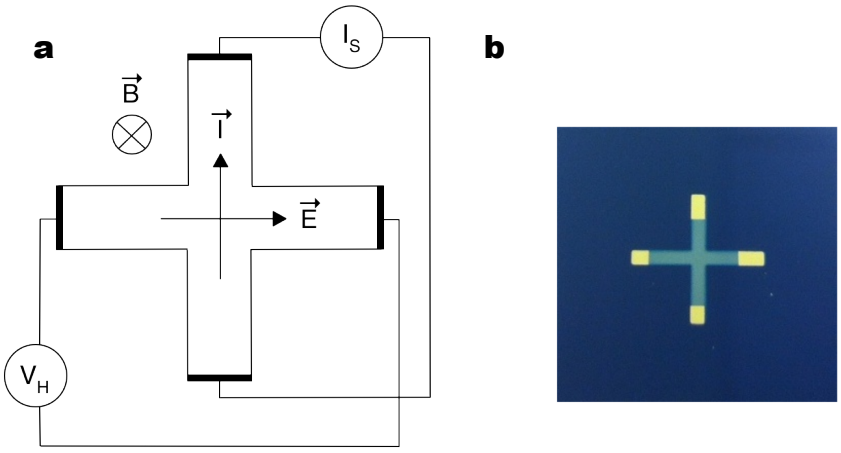

Figure 3.5. Hall Effect. a, Greek cross configuration used for measurements. **b,** Fabricated sample for Hall effect measurement.

All the Hall effect measurements shown in this work are performed in a physical properties measurement system (PPMS) from Quantum Design in the thin film laboratory at KAUST. Samples are patterned in the Greek cross configuration shown in Figure 3.5 connected in the Van der Pauw configuration following the specifications given by David and Beuhler[25]. The e-beam evaporated gold contacts are used as electrodes. Each sample is measured in a magnetic field from -5 to +5 Tesla at room temperature in the dark. The reported values are the average of measurements in three samples and after magnetoresistance correction (the increase in the resistivity under the presence of a magnetic field) by performing dual sweeps of the magnetic field (positive-going and negative-going scans). Resistivity measurements were performed in a CMT four-point probe system from Advanced Instrument Technology.

3.2.4 Optical Characterization

Optical transmittance is used to determine the transparency and the optical band gap of transparent materials[26]. In order to determine these values, the absorption coefficient, α, needs to be obtained from the transmittance, T, measured across a wavelength range, λ, by using a spectrophotometer. The absorption coefficient can be determined by:

$$\alpha = \frac{1}{t} ln \left[\frac{1}{1-A}\right] \tag{3.14}$$

where t is the film thickness, and A is the absorption spectrum given by $A=1-T$[26]. As α is a function of photon energy, $E = hv$, given by

$$\alpha^x \propto (hv - E_{opt}) \tag{3.15}$$

where x is a value related to the transition type of the fundamental absorption process (excitation of a valence electron to a higher energy level) with values of 2 for an allowed direct transition, and ½ for an allowed indirect transition. E_{opt} can be then determined by a linear fit of $(\alpha h\nu)^X$ versus $h\nu$ [26].

The transmittance measurements in this dissertation are obtained by using an evolution 600 UV-vis spectrophotometer in the wavelength range from 300 to 900 nm. The samples are deposited on glass and the transmittance of the films is measured with respect to the glass substrate. Since the discussion in this dissertation is focused on transparent materials, an average optical transparency is obtained by averaging the transmittance in the visible region (λ from 400 nm to 700 nm).

3.2.5 Supplementary Structural and Morphological Characterization Techniques

The following techniques are used in this study as supplementary structural and morphological characterization techniques. A detail description of the principles of these techniques can be found elsewhere[21].

3.2.5.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is used in this work to analyze the structural and morphological properties of oxide films and devices. It is primarily used for imagining the nanowire field-effect transistors described in chapter 5, as well as to determine TFT

device dimensions. Top view imagining is performed using a FEI Helios NanoLab 400S SEM.

3.2.5.2 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is used to accurately determine the thickness of the films and grain size of the polycrystalline oxide films used in this study. High-resolution TEM (HRTEM) and fast Fourier transformation (FFT) are used to accurately analyze the structural and morphological characteristics of the SnO films and patterned nanowire structures. TEM analysis is preformed with a FEI Titan ST. Data analysis is performed using the DigitalMicrograph™ software from the Gatan Microscopy Suite.

3.2.5.3 Atomic Force Microscopy

Atomic force microscopy (AFM) is used for imagining surface morphology of oxide films, especially to determine surface roughness. Analysis is performed with an Agilent 5400 SPM AFM system.

3.3 Patterning Techniques

As described later in this dissertation, having devices with well-defined geometries is crucial for electrical characterization. This section briefly describes the main patterning techniques used for the fabrication devices within this research work.

3.3.1 Photolithography

Photolithography or optical lithography is a microfabrication process used to transfer a pattern from a mask to a substrate. A light-sensitive chemical known as photoresist is used for transferring the geometric patter on the photomask to the substrate[9,27]. Figure 3.6a shows a conventional photolithography process flows, which consists in the following basic steps:

1. Substrate preparation. This step includes substrate cleaning to remove organic and inorganic contaminants from the surface as well as the deposition of the thin-film to be patterned.
2. Photoresist application. The sample is covered with the photoresist by spin coating. The thickness of the photoresist depends on the viscosity and the spin speed used to coat the sample. The substrate is then soft-baked to remove the excess solvent from the resist as well as to improve its adhesion.
3. Exposure and developing. The substrate is then taken for mask alignment, if required, and UV exposure. In a positive photoresist, the area exposed to UV light causes a chemical change in the resist that allows it to be removed by a chemical solution known as the developer. In negative resist the unexposed areas are soluble in the developer. After developing, the substrate may be hard-baked to solidify the remaining resist.
4. Etching. The areas of the substrate that are not protected by the photoresist are removed by either a liquid (wet) or plasma (dry) chemical attack.
5. Photoresist removal. After the removal of the unwanted portion of the thin film, the resist needs to be removed to uncover the wanted portions. This process is also known as photoresist stripping, usually done by liquid stripper such as acetone or by an oxygen plasma process referred as ashing.

Figure 3.6b depicts a variation of the process described above and is known as lift-off. In this process, the photoresist is spin-coated in the substrate prior to the thin-film deposition. The desired pattern (typically in a negative mask) is then exposed and developed as described before. The thin-film is deposited on the photoresist-coated substrate and taken directly to photoresist stripping in a liquid solvent. In this way, the thin-film deposited on the uncovered areas remains after stripping, and removed from the photoresist-coated areas along with the resist. The use of lift-off technique is limited to be used in low temperature deposition processes as most of the conventional resist only withstand temperatures below 200 ^{o}C. Nevertheless, it is advantageous in the way that no chemicals, besides the developer, are involved in the patterning process[27].

In this work, lift-off is the preferred patterning technique. Substrates are first cleaned in acetone, followed by isopropyl alcohol (IPA) and lastly in de-ionized (DI) water, under sonication for five minutes in each solution. Photoresist application is performed in a JST spin-coater system using the resists and process conditions shown in Table 3.5. Mask alignment and exposure is performed in an EVG-6200 mask aligner system equipped with a 1000 W mercury arc lamp source (broadband UV wavelength and SU-8 and i-line filter). Developing is done using metal ion free (tetramethylammonium hydroxide)-based developer AZ 726 MIF. Photoresist stripping is done using acetone or methanol when an organic layer is involved in the stack, like the device structure described in chapter 6.

Photoresist	AZ ECI3027	AZ1512 HS	AZ5214
Spin speed (rpm)	1750	3000	3000
Thickness (μm)	4	1.4	1.6
Soft bake temperature (°C)	100	100	110
Soft bake time (s)	60	60	50
Exposure dose (mJ/cm^2)	200	40	100
Developing time (s)	60	20	60

Table 3.5. Photoresist application. Spin-coating conditions for photoresist used in this dissertation.

Photomasks used for the fabrication of devices described later in this dissertation were designed using L-Edit layout editor from Tanner EDA and fabricated in a μPG101 mask writer system equipped with a 405 nm laser diode. All the photolithography steps are performed in KAUST advanced nanofabrication core facility (class-100 cleanroom).

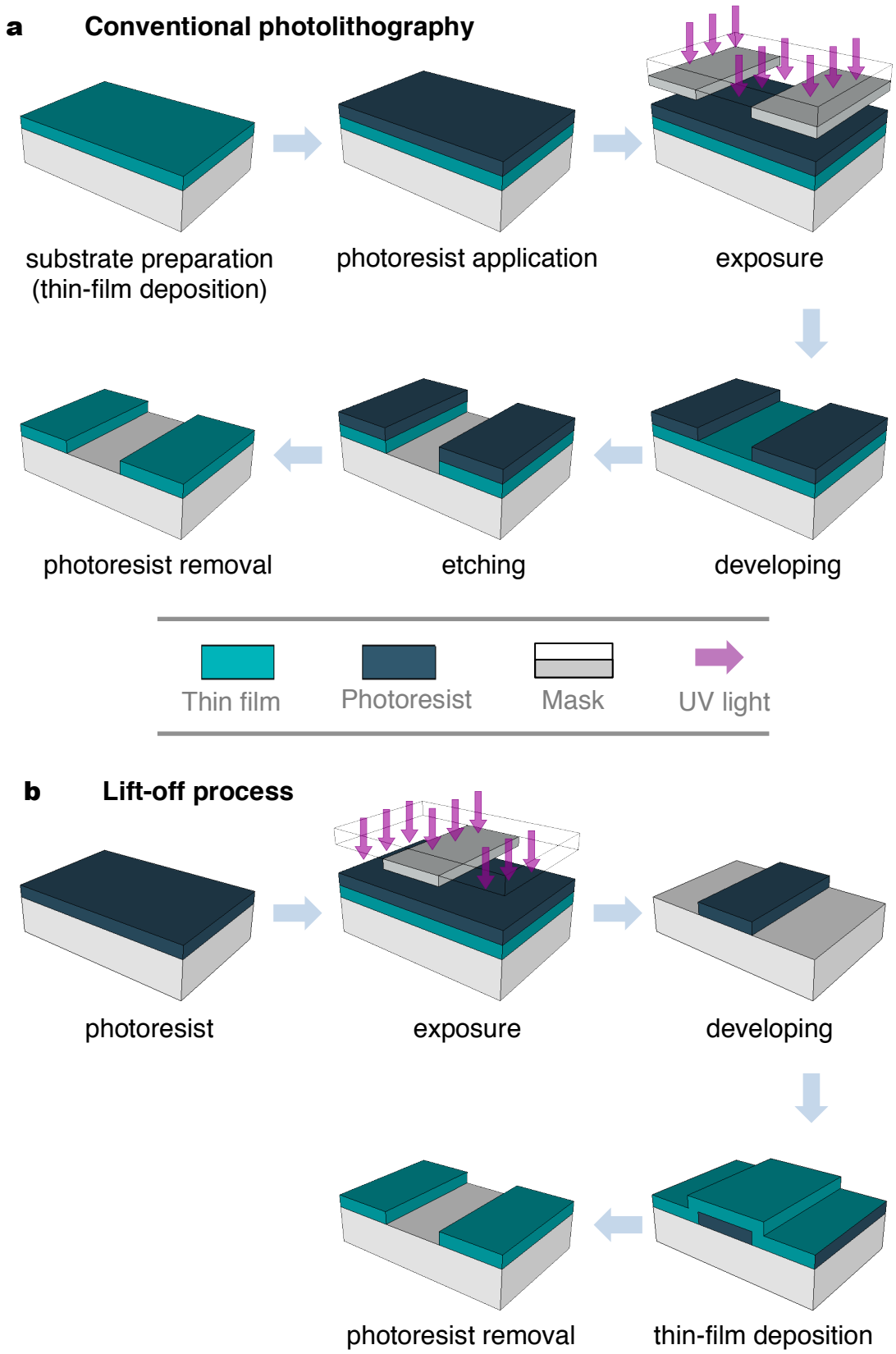

Figure 3.6. Photolithography processes. a, Conventional process flow. **b,** Lift-off process

3.3.2 Electron Beam Lithography

Electron beam lithography (EBL) is a direct-write patterning technique that uses a focused beam of electrons instead of an UV light as in photolithography[28]. The main advantage of EBL is the ability to pattern structures in the nanometer regime (even sub-10 nm[29]) due to its small wavelength, which is smaller than the diffraction limit of light in optical lithography. In contrast to photolithography, EBL doesn't require a mask, as the e-beam directly exposes a photoresist-coated substrate. Despite the advantage of patterning features in the nanoscale, the main disadvantage of EBL is the very long exposure time[28,29].

EBL has been used in this research work to pattern SnO nanowire-like structures from a thin-film deposited in a glass substrate. A 70 nm single layer of 950 K molecular weight polymethyl-methacrylate (PMMA A2) organic resist is spin coated onto a ITO/dielectric coated 1"×1" glass followed by a soft bake processing at 180 ^{o}C for 90 s to bake out the casting solvent. EBL is performed in a CRESTEC CABL-9520C high-resolution electron beam lithography system. The adjustment of the focus was primarily done by the observation with secondary electrons of a mark in the resist at high magnification. Fine focusing and correction of astigmatism is performed on gold nanoparticles placed in the substrate holder at a magnification of 300 000. Pattern is then exposed in a vector scan mode with an e-beam exposure dose of 0.84 μsec/dot and a field size setting of 1200 μm/60000 dots at a beam current of 500 pA (resist sensitivity of 80 μCcm^{-2}). 1:1 methyl isobutyl ketone: isopropanol (MIBK:IPA) is used as the developer. EBL patterning is performed in KAUST advanced nanofabrication core facility.

3.4 Device Characterization

This section describes the *I-V* characterization of p-type thin film transistors. Typical figures of merit are summarized with special emphasis on mobility extraction. A procedure for accurate electrical characterization of oxide-based TFTs is introduced and it was used as the standard procedure for all the measurements of field-effect devices described in this dissertation.

3.4.1 Current-voltage Measurements

The static characteristics of thin-film transistors can be evaluated by their output and transfer characteristics.

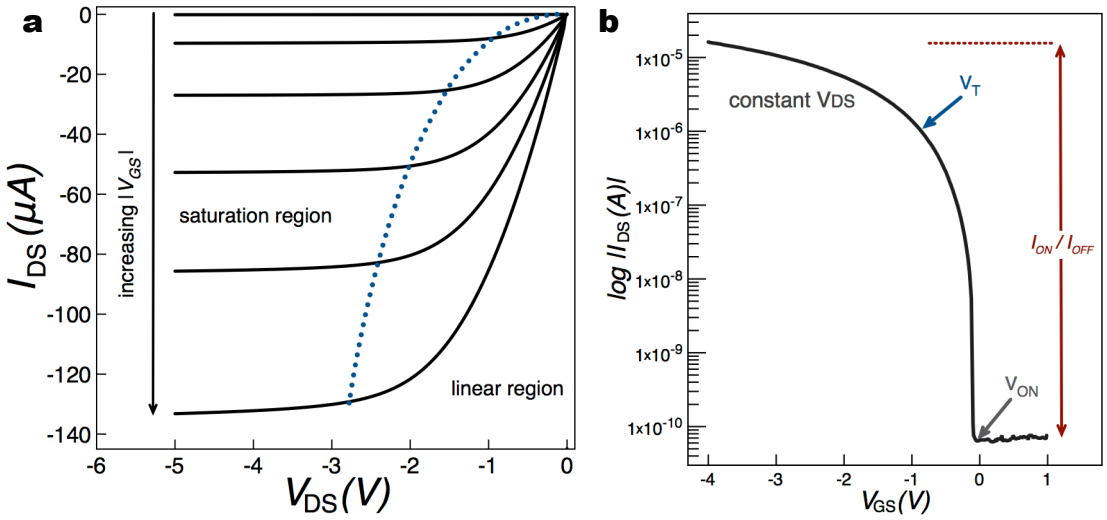

Figure 3.7. Typical curves of a p-type TFT. a, Output characteristics. **b,** Transfer characteristics.

The output characteristics are obtained by measuring the drain current (I_D) as a function of drain-source voltage (V_{DS}) for various gate-source voltages (V_{GS}), as shown in Figure 3.7a

allowing observing both the linear and saturation regimes. The output curves provide important **qualitative** information, in particular:

a) *Mode of operation.* Whether the TFT operates as a depletion-mode ($I_D \neq 0$ at $V_{GS}=0$) or enhancement-mode ($I_D \approx 0$ at $V_{GS}=0$) device.

b) *Formation of a depletion region.* The flatness of the output curve in saturation region (post-pinch-off) indicates if full carrier depletion (near the drain electrode) can be achieved in the active material. Achieving good saturation is of crucial importance particularly if the TFT is going to be used a current limiter[30].

c) *Presence of series resistance.* If non-linear behavior is observed at low V_{DS} voltages.

d) *Excessive gate leakage.* Present if near the origin the I_D-V_{DS} curves at different V_{GS} overlap with each other at do not begin at the origin.

e) *Estimation of threshold voltage.* Obtained based on the V_{GS} value at which I_D reaches the off state.

f) *Mobility degradation.* If a decreasing separation between the I_D-V_{DS} curves for increasing V_{GS} is observed at a given V_{GS} range.

Transfer characteristics are obtained by sweeping V_{GS} at a constant V_{DS}, as shown in the semi-logarithmic plot in Figure 3.7b. Depending on the value of V_{DS}, the transfer curve will show the performance at the linear or saturation region.

In contrast to output curves, transfer characteristics permit assessment of a large number of important **quantitative** parameters of the TFT performance:

1. <u>On-to-off current ratio (I_{ON}/I_{OFF}).</u> It is defined as the ratio of drain current in the on state (I_{ON}) to current in the off state (I_{OFF}). The maximum I_{ON} current depends on the

properties of the semiconductor material as well as the effectiveness of field-effect achieved by the capacitive injection from the gate electrode. The maximum gate current (I_{GS}) and/or the noise level of the characterization equipment typically determine I_{OFF}. High on-to-off current ratios (>10^6) are commonly required for TFTs to be used as electronic switches[31].

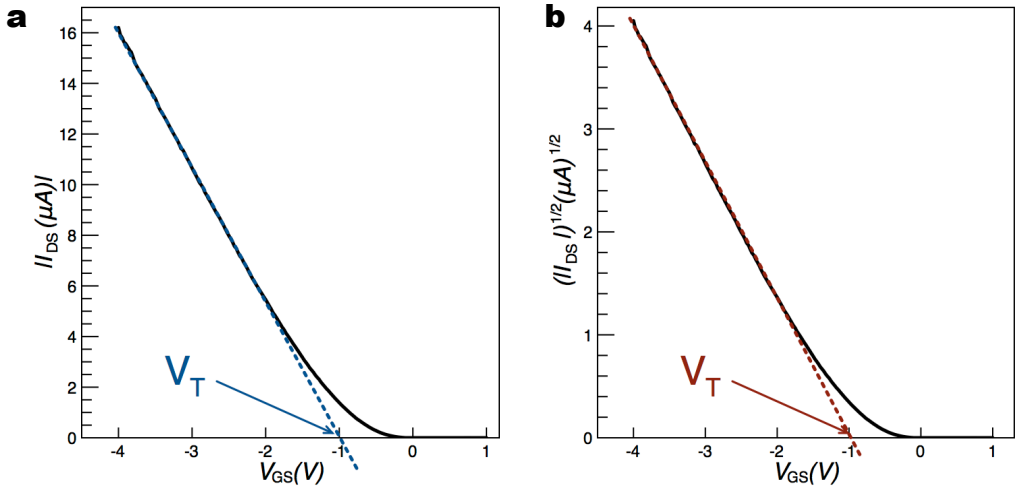

Figure 3.8. Threshold Voltage (V_T) extraction by linear extrapolation. a, Linear region from I_{DS}-V_{GS} curve. **b,** Saturation region from $(I_{DS})^{1/2}$-V_{GS} curve.

2. Threshold voltage (V_T). It is defined as the value of V_{GS} when the conductive channel (or an accumulation layer near the dielectric/semiconductor interface) just begins to connect the source and drain electrodes. As previously discussed, in an ideal case, the channel readily forms on the presence of a very small V_{GS}. In the real case, V_T deviates from the ideal value (close to 0 V) caused by the gate-semiconductor work function difference, semiconductor background carrier concentration and the density of trapped charges in the dielectric, the semiconductor and the dielectric/semiconductor interface. V_T can be estimated by different

methodologies[32], being linear extrapolation the most widely used. Figure 3.8a shows V_T extraction using the I_D-V_{GS} curve at low V_{DS} value (linear region), where V_T is estimated from the x-axis V_{GS} intercept of a straight-line fit. Figure 3.8b shows V_T estimation from a $(I_D)^{1/2}$-V_{GS} plot for high V_{DS} (saturation region)[19,32]. V_T estimation in the linear region is preferred as series resistance is usually negligible at low drain currents (obtained at low V_{DS})[19].

3. Turn-on voltage (V_{ON}). To avoid some ambiguity on the V_T extraction, the V_{ON} concept has been introduced[33,34] and is widely used in literature. As shown in Figure 3.7b, V_{ON} is simply defined as the V_{GS} for drain current conduction onset, or in other words, the V_{GS} at which the drain current rises.
4. Subthreshold swing (SS). It is defined as the gate voltage necessary to increase the drain current by one decade. SS is obtained by the inverse of the maximum slope of the transfer characteristics in the subthreshold region ($|V_{GS}|<|V_T|$).

$$SS = \left(\frac{d(logI_{DS})}{dV_{GS}}\Big|_{max}\right)^{-1} = \frac{\ln(10)nkT}{q} \quad \text{[V/decade]} \tag{3.16}$$

Low values of SS results in high operating speed and low power consumption[31].

5. Interface trap density (D_{it}). Can be obtained from the SS and is given by

$$D_{it} = \frac{1}{q}\left(\frac{q\,SS}{2.3kT} - 1\right)C_{ox} \quad [\text{cm}^{-2}\ \text{eV}^{-1}] \tag{3.17}$$

where q is the magnitude of electron charge (1.6×10^{-19} C), k is the Boltzmann's constant (8.617×10^{-5} eV K^{-1}) and T is Temperature (K).

6. Mobility (μ). Defined as the efficiency of majority carrier transport in a semiconducting material[19]. A more detailed discussion on mobility calculation is presented in the following section.

3.4.2 Mobility

Mobility, μ, is in the most general scenario is a linear proportionality constant relating the carrier drift velocity (v_d) to the applied electric field (ξ)[19]:

$$v_d = \mu\xi \quad [\text{cm s}^{-1}] \tag{3.18}$$

As described before in section 3.2.3 different types of mobility are in use. From a device point of view, the relevant mobility is *drift mobility*, which measures the efficiency of majority carrier transport in a semiconducting material and is obtained from a field-effect measurement.

In an ideal TFT, mobility is assumed to be constant and doesn't vary with V_{GS}. In a real TFT, the channel mobility may not be constant and can vary with V_{DS} and V_{GS}[19,35,36]. Several scattering mechanisms (lattice vibrations, ionized impurities, grain boundaries, interface surface roughness, lattice strain and other structural defects[19,37]), velocity saturation, and electron trapping affects the mobility of field-effect devices. In a real TFT an increment

of mobility is observed above threshold voltage, reaching a maximum value at a saturation peak, to finally decrease as the gate-source voltage increases[33].

The voltage dependence of mobility requires the definition of several types of mobility to account for it. The most common ones used in the TFT community are effective mobility, field-effect mobility and saturation mobility. The last two were previously introduced in section 2.3.

Effective mobility (μ_{eff}). The ideal drain current equation in the linear region for a TFT is given by:

$$I_D = -\mu_{eff}\, C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{3.19}$$

the very precise definition of the linear region is that given by $-V_{DS} \ll -V_{GS} + V_T$ (recall analysis is done for a p-channel TFT), and as V_{DS} is very small, I_D can be approximated as

$$I_D \approx -\mu_{eff}\, C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS}\right] \tag{3.20}$$

output conductance, g_d, defined as the change in I_D for a change in V_{DS} at a constant V_{GS} in the linear region yields,

$$g_d = \frac{\partial I_D}{\partial V_{DS}}\bigg|_{V_{GS}=constant} \approx \mu_{eff} C_{ox} \frac{W}{L}(V_{GS} - V_T) \tag{3.21}$$

solving equation 3.21 for mobility yields,

$$\mu_{eff} = \frac{g_d L}{W C_{ox}(V_{GS}-V_T)} \qquad [\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}] \tag{3.22}$$

μ_{eff} may be found using the measured linear region output conductance. Effective mobility is normally considered the most accurate estimation of mobility as it includes the effect of V_{GS}[19]. Nevertheless, errors on the threshold voltage determination can lead to effective mobility inaccuracies.

Field-effect mobility (μ_{FE}). It is the most commonly used mobility to describe the performance of a TFT. It is also obtained at a low V_{DS} but it does not depend on V_T determination, as it is extracted from the transconductance, g_m, defined as the change in I_D for a change in V_{GS} at a constant V_{DS}

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=constant} \approx \mu_{FE} C_{ox} \frac{W}{L} V_{DS} \tag{3.23}$$

solving equation 3.23 for mobility yields,

$$\mu_{FE} = \frac{g_m L}{W C_{ox} V_{DS}} \tag{3.24}$$

μ_{FE} is generally lower than μ_{eff} because in the transconductance derivation the electric field dependence of mobility is neglected, that is $\mu_{eff} = f[V_{GS}, g_d(V_{GS})]$ and $\mu_{FE} = f[\, g_m(V_{DS})]$.

Saturation mobility (μ_{sat}). The ideal drain current equation in the saturation region for a TFT is given by

$$I_D = -\mu_{sat} C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \tag{3.25}$$

μ_{sat} may be obtained using the measured saturation region transconductance (at high V_{DS}) according to

$$\mu_{sat} = \frac{2L}{WC_{ox}} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2 \tag{3.26}$$

Saturation mobility is also commonly used to describe TFTs, however it is not physically accurate as it is extracted from measurements in the post-pinch-off region (saturation) where the effective channel length is smaller than the defined L due to the depletion region formed near the drain electrode, as previously explained in section 2.3.2.

Other definitions of mobility include the ones proposed by Hoffman[38], defined as average and incremental mobility, μ_{AVG} and μ_{INC}, respectively. μ_{AVG} indicates the average mobility of the total number of carriers in the channel, while μ_{INC} reflects the mobility of the carriers added to the channel as $|V_{GS}|$ increases. Besides the more physical significance of the average and incremental mobility, field-effect mobility is used throughout this dissertation, as it is the most commonly used in the TFT literature.

3.4.3 Procedure for Electrical Characterization of Oxide TFTs

In order to avoid measurement artifacts during the TFT characterization, the procedure for electrical characterization proposed by Wager[34] has been followed during the characterization of field-effect devices and can be summarized as follows:

a) Only devices with a patterned channel, with well-defined channel width and channel length are considered. The width-to-length ratio (W/L) of a TFT is a key parameter when determining the electrical properties. In the case of an unpatterned channel, or a channel width much larger than the width of the source and drain electrodes, fringing current flows outside the drawn width and length, as illustrated in Figure 3.9, leading to an overestimation of mobility as a result of the underestimation of the effective channel width. In other words, in an unpatterned channel the effective W/L is much larger than the drawn channel width and length. Devices with $W/L>10$ are preferred for accurate characterization.

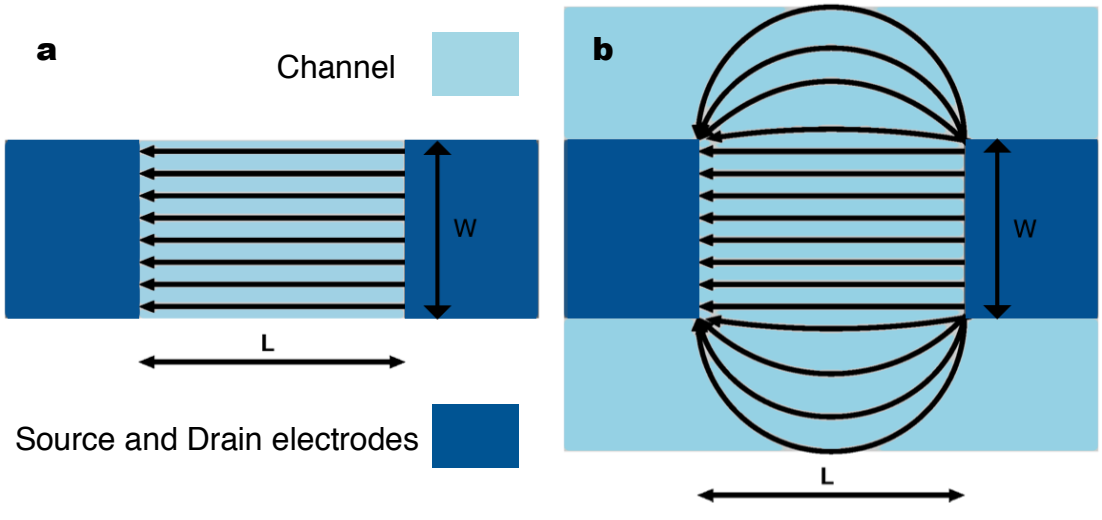

Figure 3.9. Current pathways in TFTs with identical drawn width (W) and length (L). a, Patterned channel. **b,** Unpatterned channel. *Adapted from Hong et al.*[33]

b) Acquire multiple dual-sweep (from positive V_{GS} to negative V_{GS} and vice versa) $\log(I_D)$-V_{GS} transfer curves at low V_{DS} making sure the V_{DS} is small enough that the device operates in the linear region. Sweep the gate voltage in the range $|V_{GS}/t_{ox}| \geq$ 2 MV cm^{-1} as a stress test for the gate dielectric, which truly reflects its insulating properties, where t_{ox} is the gate dielectric thickness.

c) From multiple dual-sweep transfer curves classify the TFT behavior as follows:

1. Equilibrium: Transfer characteristics free of hysteresis. Positive-going ($-V_{GS}$ to $+V_{GS}$) and negative-going ($+V_{GS}$ to $-V_{GS}$) transfer curves retrace one another (Figure 3.10a). This is the ideal case. If the transfer curves behave in this way, assessment is simple and straightforward. Include the gate current in the transfer characteristics plot.
2. Non-equilibrium, steady-sate: Hysteresis is present. Scans in the same direction retrace themselves. (Figure 3.10b). The presence of hysteresis indicates the presence of traps in the TFT and that the device operates in non-equilibrium. The fact that positive-going scans and negative-going scans retrace themselves means the TFT measurement has achieved a steady state. Both effective hysteresis density, N_{HYS}, defined as

$$N_{HYS} = \Delta V_{ON} \frac{C_{ox}}{q} \quad [\text{cm}^{-2}] \tag{3.27}$$

and V_{GS} scan rate, SR

$$SR = \frac{[V_{GS}(\max) - V_{GS}(\min)]}{t_{scan}} \quad [\text{mV sec}^{-1}] \tag{3.28}$$

should be specified along with the important TFT parameters described in section 3.4.1. ΔV_{ON} is the difference in V_{ON} between positive-going and negative-going scans and t_{scan} is the time required to accomplish one positive- or negative-going scan. Include the gate current in the transfer characteristics plot.

3. Non-equilibrium, non-steady-state: Hysteresis is present and scans in the same direction do not follow each other (Figure 3.10c). Non-steady state is commonly a consequence of high gate leakage, mobile ion migration, or excessive density of trap states in the dielectric. If this behavior is observed, quantitative characterization should be avoided as nothing meaningful can be extracted of a device operating in this category.

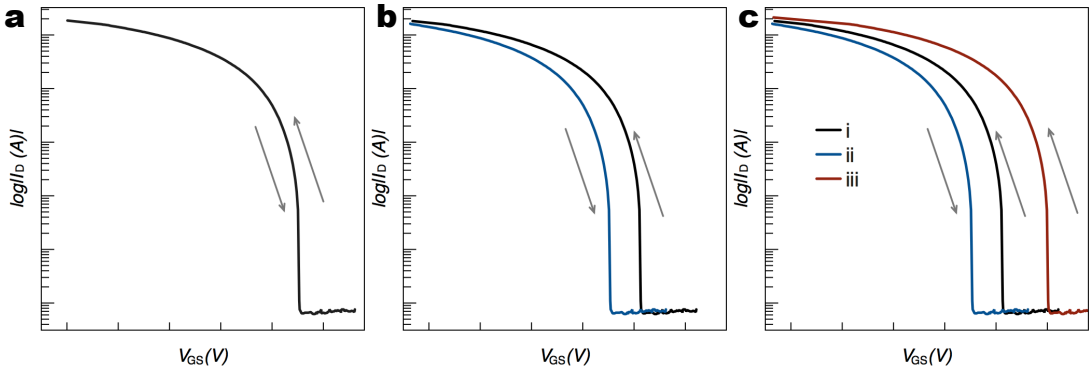

Figure 3.10. TFT behavior. Multiple dual-sweep transfer curves for **a,** equilibrium; **b,** non-equilibrium, steady-state; **c,** non-equilibrium, non-steady-state TFT operation. Adapted from Wager[34].

All the field-effect devices fabricated for this dissertation were characterized using a 4200-SCS Keithley semiconductor parameter analyzer connected to a Cascade Microtech probe station. Measurements were made at room temperature, in the dark, at a relative humidity of 30-50%.

3.5 References

1 Wasa, K., Kitabakate, M. & Adachi, H. *Thin Film Materials Technology: Sputtering of Compound Materials*. (William Andrew, Inc., 2004).

2 Vossen, J. L. & Cuomo, J. J. *Thin Film Processes*. (Academic Press, Inc., 1978).

3 Chiang, H. Q. *Development of Oxide Semiconductors: Materials, Devices, and Integration* PhD thesis, Oregon State University, (2007).

4 Thornton, J. A. Magnetron sputtering: basic physics and application to cylindrical magnetrons. *Journal of Vacuum Science and Technology* **15**, 171-177 (1978).

5 http://www.arzuffisrl.it/eng/sputtering.htm.

6 http://clearmetalsinc.com/technology/.

7 Hartnagel, H., Dawar, A., Jain, A. & Jagadish, C. *Semiconducting Transparent Thin Films*. (IOP Publishing, 1995).

8 http://www.angstromengineering.com/amod.html.

9 Jaeger, R. C. *Introduction to Microelectronic Fabrication*. (Adisson-Wesley Publishing Company, 1988).

10 Smith, D. L. *Thin-Film Deposition Principle and Practice*. (McGraw Hill, 1995).

11 Suntola, T. & Hyvärinen, J. Atomic Layer Epitaxy. *Ann. Rev. Mater. Sci.* **15**, 177-195 (1985).

12 Ritala, M. & Leskelä, M. Atomic Layer Epitaxy- a valuable tool for nanotechnology? *Nanotechnology* **10**, 19-24 (1999).

13 George, S. M. Atomic Layer Deposition: An Overview. *Chemical Reviews* **110**, 111-131 (2010).

14 Wolf, S. & Tauber, R. *Silicon Processing for the VLSI Era: Volume 1-Process Technology*. (Lattice Press, 2000).

15 Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Advanced Materials* **24**, 2945-2986 (2012).

16 Birkholz, M. *Thin-film analysis by x-ray scattering*. 1-37, 200-265 (WILEY-VCH, 2006).

17 Ramadan, A. A. *et al.* Addressing difficulties in using XRD intensity for structural study of thin films. *Crys. Res. Technol.* **44**, 111-116 (2009).

18 Delhez, R., Keijser, T. H. & Mittemeijer, E. J. Determination of crystallite size and lattice distortions through X-ray diffraction line profile analysis. *Fresenius Z. Anal. Chem.* **312**, 1-16 (1982).

19 Schroder, D. *Semiconductor Material and Device Characterization*. 2nd edn, (John Willey & Sons, 1998).

20 Brundle, C. R., Jr., C. A. E. & Wilson, S. *Encyclopedia of materials characterization -surfaces, interfaces, thin films.*, (Manning, 1992).

21 Leng, Y. *Materials Characterization: Introduction to Microscopic and Spectroscopic Methods*. (John Wiley & Sons, 2009).

22 Putley, E. *The Hall Effect and Related Phenomena*. (Butterworth, 1960).

23 Pauw, L. J. v. d. A method of measuring specific resistivity and Hall effect of discs of arbitrary shape. *Philips Research Reports* **13**, 1-9 (1958).

24 Pauw, L. J. v. d. A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shaper. *Philips Technical Review* **20**, 220-224 (1958).

25 David, J. M. & Beuhler, M. G. A numerical analysis of various cross sheet resistor test structures. *Solid-State Electronics* **20**, 539-543 (1977).

26 Pankove, J. I. *Optical Processes in Semiconductors*. (Dover Publications, 1971).
27 Koch, C. & Rinke, T. Lithography: Theory and Application of Photoresists, Developers, Solvents and Etchants. *Microchemicals Company Manual* (2006).
28 Broers, A. N., Hoole, A. C. F. & Ryan, J. M. Electron beam lithography—Resolution limits. *Microelectronic Engineering* **32**, 131-142 (1996).
29 http://anicbooking.kaust.edu.sa/Lithography/litho-ebeam.html.
30 Tickle, A. C. *Thin-Film Transistors -A New Approach to Microelectronics*. . (Wiley, 1969).
31 Lee, J.-H., Liu, D. N. & Wu, S.-T. *Introduction to Flat Panel Displays*. (John Wiley & Sons Ltd., 2008).
32 Ortiz-Conde, A. *et al.* A review of recent MOSFET threshold voltage extraction methods. *Microelectronics Reliability* **42**, 583-596 (2002).
33 Hong, D., Yerubandi, G., Chiang, H. Q., Spiegelberg, M. C. & Wager, J. F. Electrical Modeling of Thin-Film Transistors. *Critical Reviews in Solid State and Materials Sciences* **33:2**, 101-132 (2008).
34 Wager, J. F. Transfer-curve assessment of oxide thin-film transistors. *Journal of the Society for Information Display* **18**, 749-752 (2010).
35 Kang, J. S., Schroder, D. K. & Alvarez, A. R. Effective and field-effect mobilities in Si MOSFETs. *Solid-State Electronics* **32**, 679-681 (1989).
36 Sun, S. C. & Plummer, J. Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces. *IEEE Transactions. Electron Devices* **27**, 1497-1508 (1980).
37 Yang, E. S. *Microelectronic Devices*. (McGraw Hill, 1988).
38 Hoffman, R. L. ZnO-channel thin-film transistors: Channel mobility. *Jounal of Applied Physics* **95**, 5813-5819 (2004).

Chapter 4

Record Mobility in Transparent p-Type Tin Monoxide Films and Devices

Transparent oxide semiconductors hold great promise as materials for the development of a variety of emerging electronic devices. While several high-performing n-type oxide semiconductors have been demonstrated, equally well performing p-type oxide semiconductors remain elusive. This fact has limited the development of complex electronic circuitry based on transparent oxides. This is because low power applications as well as many types of circuit elements require both n and p-type semiconductors. High mobility, p-type oxide semiconductors processed at low-temperature are crucial for realizing cost-effective, large-area, transparent electronic and display applications. Here, we report the fabrication of nanoscale fully transparent p-type SnO thin film transistors (TFT) at temperatures as low as 180 ^{o}C with record device performance. Specifically, by carefully controlling the process conditions, we have developed SnO thin films with a Hall mobility of 18.71 $cm^2V^{-1}s^{-1}$ and fabricated TFT devices with a linear field-effect mobility of 6.75 $cm^2V^{-1}s^{-1}$ and 5.87 $cm^2V^{-1}s^{-1}$ on transparent rigid and translucent flexible substrates, respectively. These values of mobility are the highest reported to date for any p-type oxide processed at this low temperature. We further demonstrate that this high mobility is realized by careful phase engineering. Specifically, we show that phase-pure SnO is not necessarily the highest mobility phase; instead, well-controlled amounts of residual metallic tin are shown to substantially increase the hole mobility. A detailed phase stability map for physical vapor deposition of nanoscale SnO is constructed for the first time for this p-type oxide.

4.1 Introduction

Oxide semiconductors hold great promise as materials for use in many emerging electronic applications. Such applications include transparent and flexible displays, sensor arrays, flexible solar cells, and logic circuitry for so-called invisible electronics.[1-3] The use of oxide-based thin-film transistors (TFT) has already been shown as a good solution to the increasingly demanding requirements of better display technologies.[4,5] For example, transparent amorphous In-Ga-Zn-O with a mobility of 10 $cm^2V^{-1}s^{-1}$ has been demonstrated to be useful in switching/driving TFTs in the next generation of flat panel and flexible displays.[2] Outstanding TFT results have been reported for display applications based on various oxide-based semiconducting films,[6] although all such materials are based on n-type semiconductors. A p-type oxide with comparable performance (mobility, current-carrying capacity, optical transparency and mechanical flexibility) to that of previously developed n-type transparent semiconducting oxides will allow the realization of not only better display technologies, but it will usher in a new era of transparent electronics.

Electronic circuits based on single crystalline silicon substrates have limited potential applications in large-area electronics because of their opaqueness, high processing temperatures and rigidity especially when mechanical flexibility is desired. The use of amorphous silicon has partially addressed this issue, but its field-effect mobility of $\mu_{FE} \leq 1$ $cm^2V^{-1}s^{-1}$ limits its performance[7]. Moreover, low-temperature processing is essential to fabricating flexible devices on inexpensive plastic substrates.[8] One group of candidate materials to satisfy this requirement is organic semiconductors, but their μ_{FE} is barely different from that of amorphous silicon.[9] Recently, n-type oxide semiconductors, with high

optical transparency, low-temperature processing and performance comparable to that of polycrystalline silicon, have been demonstrated using a variety of deposition methods[10-12].

The limiting factor for the full integration of oxide-based devices, however, continues to be the development of a p-type oxide material with performance comparable to that of the n-type oxides. Cu-based oxides have been demonstrated to exhibit p-type behavior[13,14]. The best performance (μ_{FE}= 4.3 $cm^2V^{-1}s^{-1}$)[15] has been exhibited when Cu_2O is deposited at 500 °C. Despite their high hole mobility, Cu_2O-based oxides are of limited use because its optical transparency is hindered by their low optical bandgap of 2.2 eV[16,17]. If plastic and other flexible substrates are the ultimate goal, low processing temperatures are essential. Recently, devices based on p-type tin monoxide (SnO) have been developed, but again their use is limited by either high deposition temperatures or low μ_{FE} similar to a-Si:H[18-23]. Not even Hall-effect mobility (μ_{Hall}) in the range of n-type amorphous oxide semiconductors[2] (10 $cm^2V^{-1}s^{-1}$) has been reported for SnO, preventing its use in practical applications.

4.2 Film Characterization

The pathway to achieve high mobility involved a large number of experimental studies, each repeated several times, in which we carefully mapped out a very wide process window in our reactive DC magnetron sputtering process. It is known that Sn metal occurs in two possible oxidation states (2^+ and 4^+), with SnO_2 (4^+) being the most thermodynamically stable phase[24]. SnO easily oxidizes to n-type SnO_2 via the reactions presented in section 2.2. It is also known that depositing the correct p-type phase of SnO by

physical vapor deposition is challenging due to the required fine control of oxygen pressure to prevent the formation of SnO_2 or any other intermediate phases such as Sn_2O_3 or Sn_3O_4 with n-type characteristics[24]. In our extensive experimental studies, we have found that the p-type transport in tin monoxide occurs only in a very narrow window of deposition conditions. This window occurs when the relative oxygen partial pressure (O_{PP}) [where $O_{PP} = P_{O2}/(P_{O2}+P_{Ar})$] and deposition pressure (P) lie within the process boundaries illustrated by the bold black lines in Figure 4.1a. Specifically, p-type tin monoxide transport occurs in the process regime where $7\% \leq O_{PP} \leq 15\%$ and 1.5 mTorr $\leq P \leq$ 2 mTorr. For the case where P is > 2.0 mTorr or $O_{PP}>15\%$, either amorphous phase or SnO_2 is formed. Pan and Fu have shown that in the presence of excess oxygen (and temperature), the metastable SnO phase transforms to SnO_2 via a process initiated by the local disproportionate redistribution of internal oxygen[25], known as the disproportionation mechanism[26]. In the first step of the oxidation process the metastable SnO phase coexist with intermediate products such as Sn_3O_4 and Sn, then the inward diffusion of external oxygen causes the full oxidation into the thermodynamically stable SnO_2 phase[24-26]. In our films, the observation of an amorphous phase when P > 2.0 mTorr and $15\% \leq O_{PP} < 20\%$ indicates that at these conditions the oxygen concentration is high enough not to form p-type SnO, but the thermal budget is not enough to crystallize the intermediate product (Sn_3O_4), or its diffraction intensity is too low to be detected by our tool. At higher O_{PP} (> 20%) oxygen content is enough to directly crystallize the films into SnO_2 phase after annealing. When $O_{PP}<7\%$ and/or $P<1.5$ mTorr, metallic tin (β-Sn) is the dominant phase and the films exhibit either metallic or weak n-type conduction. In this study, all the samples were deposited at room temperature following a post annealing treatment in air, in a tube furnace at 180 ^{o}C for 30 min.

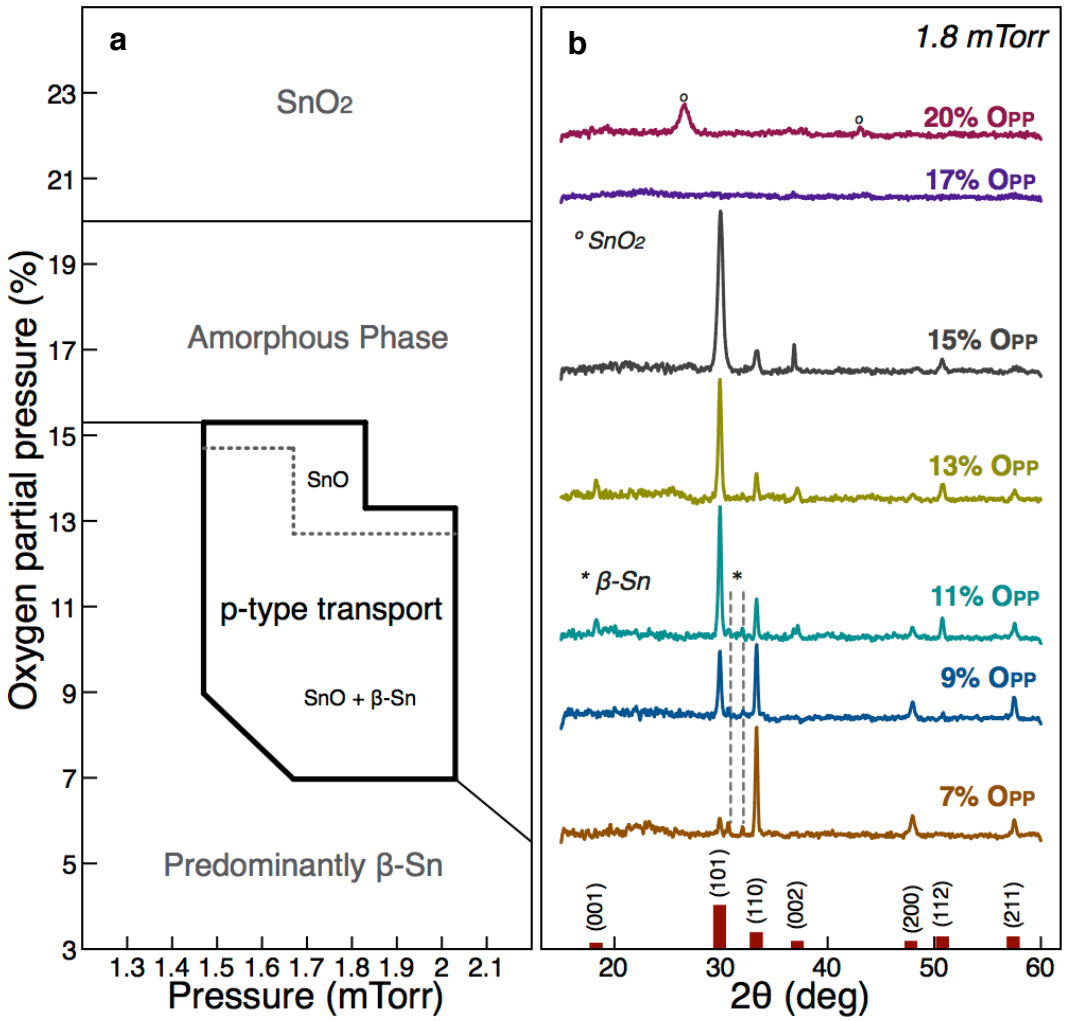

Figure 4.1. SnO deposition map and XRD patterns. a, phase stability map to obtain p-type tin moxide, which occurs in a very narrow window of deposition conditions. **b**, Phase formation dependence on the oxygen partial pressure (O_{PP}) at a deposition pressure of 1.8 mTorr.

The x-ray diffraction (XRD) patterns in Figure 4.1b show the dependence of phase formation on the oxygen partial pressure (O_{PP}) at a deposition pressure *(P)* of 1.8 mTorr, as an example (in fact, similar XRD analysis was done for many deposition pressures to construct the phase map in Fig. 4.1a). As indicated in Fig. 1b, films deposited at $7\% \leq O_{PP} \leq 11\%$ show the presence of small traces of β-Sn in a matrix of SnO (this mixture is henceforth referred to as mixed phase SnO or **mp-SnO**), while films deposited at

$13\% \leq O_{PP} \leq 15\%$ are comprised of pure tetragonal SnO. The Sn metal was uniformly distributed in the SnO matrix as seen in plane view transmission electron microscopy and as reflected by the excellent device uniformity, which will be discussed later on. Films deposited at higher O_{PP} form either amorphous SnO phase (*a*-SnO) (e.g.,17% O_{PP}) or SnO_2 (e.g., 20% O_{PP}). Further, we found that the tin oxide phase formation (SnO, mp-SnO, *a*-SnO or SnO_2) is *extremely sensitive* to the deposition pressure. Figure 4.2a shows the influence of the deposition pressure on the SnO phase formation at 13% O_{PP}. A pure polycrystalline SnO phase is obtained in the deposition pressure range of 1.7 mTorr to 2.0 mTorr. As the deposition pressure increases, the intensity of the SnO diffraction peaks increases up to P=1.8 mTorr and then decreases at P=1.9 mTorr to completely vanish at $P \geq$ 2.0mTorr, indicating the formation of amorphous films. The O_{PP} is not only crucial to controlling which oxide phase will form, but also to controlling the amount of metallic tin present in the films. Figure 4.2b shows XRD patterns in a narrower 2θ range to clarify how the diffraction intensity of the β-Sn decreases as a function of O_{PP} at 1.8 mTorr, which turned out to be the optimal deposition pressure for device performance as discussed below. X-ray photoelectron spectroscopy (XPS) analysis was used to estimate the metallic tin content in the mp-SnO films. Figure 4.3 shows the XPS analysis of selected films deposited at P=1.8 mTorr after the post deposition annealing (PDA) at 180 ^{o}C. Figure 4.3a shows the XPS curves for films deposited at 3% O_{PP} and 9% O_{PP}, showing the predominant metallic phase (3% O_{PP}) and the mp-SnO (highest μ condition). The 3% O_{PP} films show a predominant metallic content, as seen on the peaks centered at 484.9 eV and 493.5 eV, which correspond to Sn^0 $3d_{5/2}$ and Sn^0 $3d_{3/2}$, respectively. The SnO phase is present in a small amount on this film, which can be identified by the peaks at 486.5 eV (Sn^{2+} $3d_{5/2}$) and 495.1 eV (Sn^{2+} $3d_{3/2}$)[24]. The 9% O_{PP} sample has in contrast a predominant SnO phase with some traces of metallic phase, which

has been calculated to be around 3 at% for this deposition condition, and confirms the mixed phase composition of this film. Figure 4.3b compares two films deposited at *P*=1.8 mTorr but different O_{pp} and after PDA treatment. The film deposited at 13% O_{pp} clearly shows the presence of phase-pure SnO as only XPS peaks for Sn^{2+} are detected, in contrast with the 9% O_{pp} where small shoulders near the Sn^{2+} peaks can be observed and correspond to the presence of metallic β-Sn (Sn^0). For the 1.8 mTorr deposition pressure, as the relative oxygen partial pressure (O_{pp}) was reduced from 15% to 7%, the amount of metallic tin in the films increased from undetectable by XPS to nearly 5 at% for the region where p-type behavior is observed.

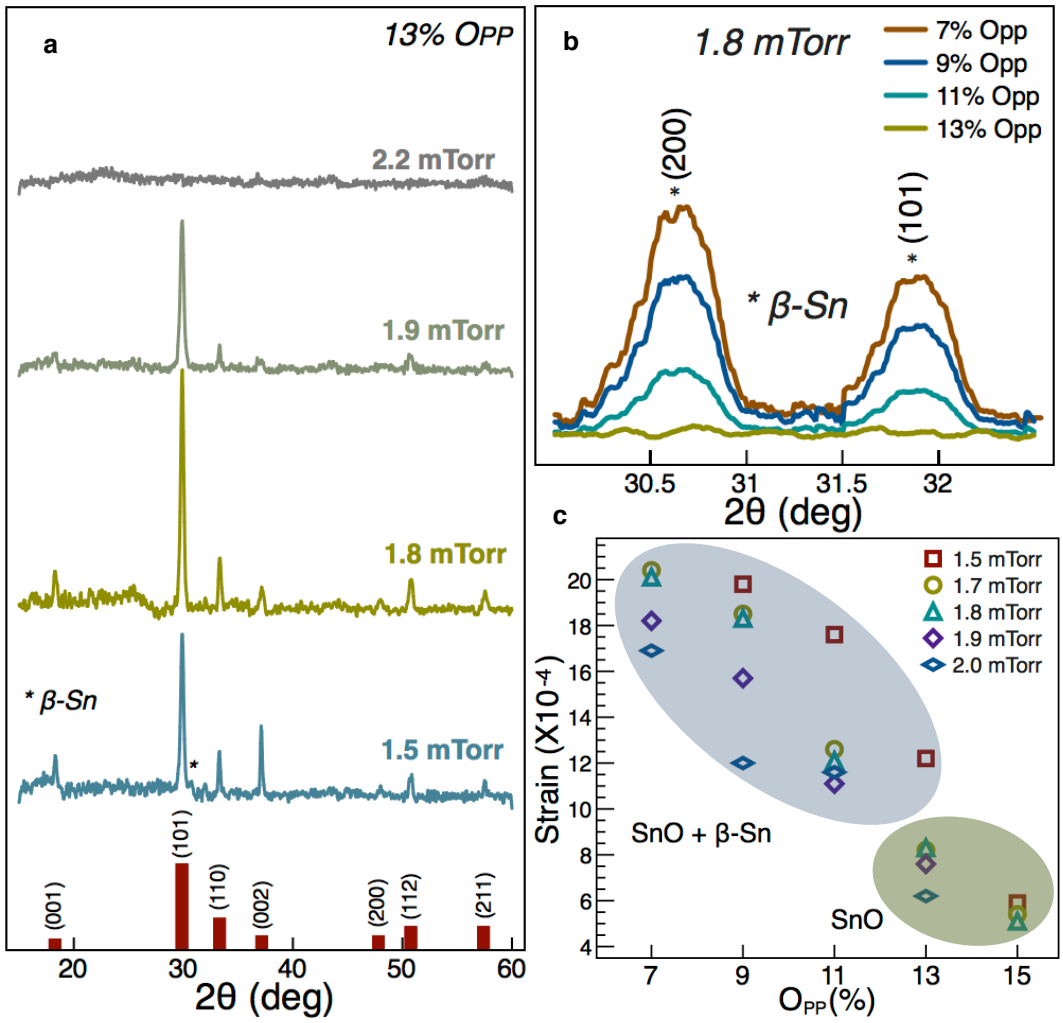

Figure 4.2. XRD patterns and strain analysis. **a,** Deposition pressure dependence of the SnO phase at 13% O_{PP}. The red lines at the bottom show the diffraction pattern (JCPDS card No. 06-0395) of tetragonal SnO. **b**, The β-Sn phase decreases as the O_{PP} increases. Pure SnO is obtained at 13% O_{PP}. **c**, Lattice strain for all deposition conditions calculated from the XRD patterns. Higher strain values are observed for the SnO_x phase (β-Sn + SnO), indicating the presence of lattice impurities.

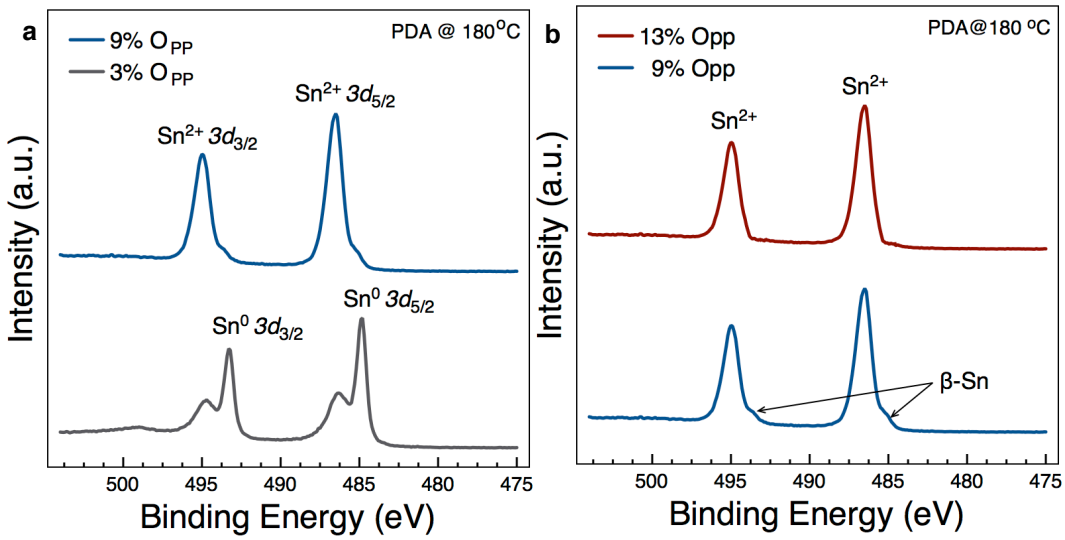

Figure 4.3. XPS Analysis. a, Films deposited at 3% O_{PP} and 9% O_{PP} and *P*=1.8 mTorr after PDA at 180 °C. **b,** Post annealed films deposited at different O_{PP} showing the mixed phase condition (9% O_{PP}, 3 at% Sn) and single phase SnO (13% O_{PP})

Noticeable differences in the intensities of the (101) and (110) diffraction peaks are observed with increasing O_{PP} (Fig. 4.1b). The difference in intensities of the XRD peaks can have many origins, such as crystallite size, lattice defects, and preferential crystallite orientation[27-29]. We have identified preferential crystallite orientation (by pole density calculations) as well as lattice defects (by strain analysis) to be the main causes of the intensity differences. Nevertheless the impact of the preferential orientation yields no clear relation with the observed mobility enhancement, as most of the films are preferentially oriented in the [101] or [110] directions and none of them in the direction of the lowest hole effective mass ([001]), where higher mobility is expected. The crystallite size and strain were extracted for all deposition conditions and we found out that the lattice strain increases with the amount of metallic tin present in the films, as observed in Figure 4.2c. This analysis was done by simultaneously calculating crystallite size (D) and lattice strain (ε) on the basis of the integral breadth (β) of the diffraction peaks by using a least-squares method to account for the β of all diffraction conditions, as explained in section 3.2.1. The films deposited at 7%

O_{PP}, where maximum metallic tin was present (~ 5 at%), had nearly one order of magnitude higher strain values (10^{-3}) than those of pure SnO (10^{-4}). The peak shift of around 0.2° on the (200) and (211) diffraction peaks of the Sn-rich films is an indication of the strain-related intensity difference. The extracted crystallite size is about 10-15 nm for all deposition conditions tested, as confirmed by the transmission electron microscopy analysis. The higher strain values of the mixed phase films (mp-SnO) when compared to pure SnO indicate the presence of more lattice defects, which can act as potential scattering centers in the former case.

Room-temperature Hall effect measurements are summarized in the three-dimensional plot depicted in Figure 4.4. The plot summarizes the effect of the process parameters discussed above on the Hall mobility of the films. As shown in the figure, films deposited in the range of $7\% \leq O_{PP} \leq 15\%$ and a deposition pressure of 1.5 to 2.0 mTorr exhibit *p*-type behavior (a positive Hall effect coefficient). Films processed using conditions outside this window showed n-type or metallic behavior in accordance with the phase map in Fig. 4.1a. According to Fig. 4.4, a maximum Hall mobility (μ_{Hall}) of 18.7 $cm^2V^{-1}s^{-1}$ is obtained for the films deposited at 1.8 mTorr and 9% O_{PP}, which surprisingly does not correspond to pure SnO films, but to the mixed phase ones (mp-SnO). The maximum μ_{Hall} obtained in this study is 8 times higher than the value reported for single-phase (00*l*) epitaxial SnO[22] and is of sufficiently large value that practical applications can be realized. The measured carrier density ranges from 4.83×10^{16} cm^{-3} to 3.33×10^{17} cm^{-3}, which is in the range of previously observed p-type SnO[18,20,22]. Details of the Hall mobility, carrier density, and film conductivity are shown in Table 4.1.

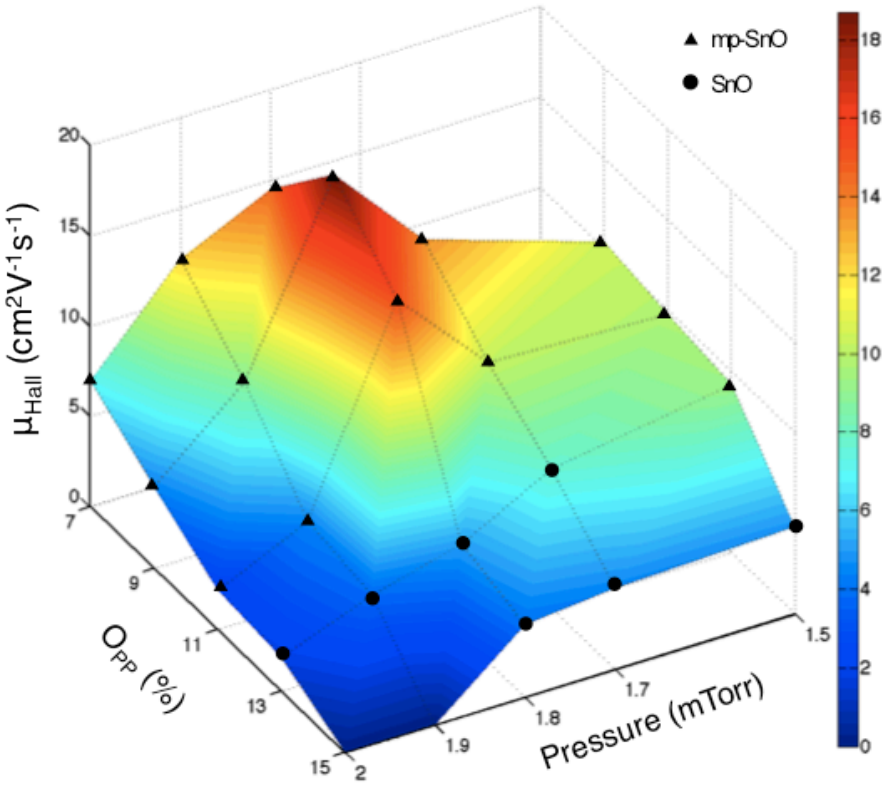

Figure 4.4. Hall Mobility. Room temperature Hall mobility of the films deposited in the pressure range from 1.5 mTorr to 2.0 mTorr and 7% O_{PP} to 15% O_{PP}. The point at 7% O_{PP}, 1.5 mTorr showing n-type conduction as well as the 15% O_{PP} at 1.9 mTorr and 2.0 mTorr showing unreliable measurements, are set to zero. A maximum Hall mobility of 18.7 $cm^2V^{-1}s^{-1}$ is obtained at 1.8 mTorr, 9% O_{PP}.

O_{PP} \ Dep. Pressure		1.5 mTorr	1.7 mTorr	1.8 mTorr	1.9 mTorr	2.0 mTorr
7%	**Mobility (cm^2/Vs)**	**n**	**9.60**	**14.48**	**12.22**	**7.01**
	Carrier Density (cm^{-3})	n	2.42E+17	2.57E+17	3.12E+17	3.33E+17
	Conductivity (S/cm)	n	0.3738	0.5986	0.6133	0.3757
9%	**Mobility (cm^2/Vs)**	**10.43**	**13.57**	**18.71**	**8.78**	**4.45**
	Carrier Density (cm^{-3})	2.29E+17	2.38E+17	2.18E+17	2.37E+17	3.33E+17
	Conductivity (S/cm)	0.3838	0.5198	0.6560	0.3350	0.2386
11%	**Mobility (cm^2/Vs)**	**9.83**	**10.16**	**15.21**	**4.45**	**2.25**
	Carrier Density (cm^{-3})	7.55E+16	1.44E+17	7.62E+16	5.11E+16	2.31E+17
	Conductivity (S/cm)	0.1195	0.2363	0.1865	0.0366	0.0836
13%	**Mobility (cm^2/Vs)**	**9.33**	**7.68**	**5.08**	**3.82**	**1.95**
	Carrier Density (cm^{-3})	7.62E+16	1.91E+17	4.83E+16	9.77E+16	6.88E+16
	Conductivity (S/cm)	0.1144	0.2359	0.0395	0.0601	0.0216
15%	**Mobility (cm^2/Vs)**	**4.82**	**4.50**	**4.00**	**X**	**X**
	Carrier Density (cm^{-3})	7.83E+16	6.23E+16	5.90E+16	X	X
	Conductivity (S/cm)	0.0607	0.0451	0.0380	X	X

Pure phase SnO

n - n-type conduction

X - high resistance

Table 4.1. Hall mobility, carrier density and film conductivity as extracted from room temperature Hall effect measurements. The reported value is the average of 3 measurements performed on different samples of every deposition condition. A maximum Hall mobility of 18.7 $cm^2V^{-1}s^{-1}$ is obtained at 1.8 mTorr, 9% O_{PP}.

Fig. 4.4 also shows that within the p-type transport process window (Fig. 4.1a), the mobility increases as O_{PP} drops (and Sn levels increase) for several pressure values. This mobility increase occurs up to a point then begins to decrease. The O_{PP} value at which the mobility peaks depends on process pressure as shown in Fig. 4.4. An important question to answer is how the excess metallic tin, present in the mp-SnO films, affects the hole mobility. According to our phase map (Fig. 4.1a), a pure SnO phase is obtained with 15% O_{PP} at a deposition pressure of 1.5 mTorr and with $O_{PP} \geq 13\%$ for the other pressures. It is important to note that the films deposited under these conditions exhibit rather low μ_{Hall} values as shown in Fig. 4.4. The role of additional metallic tin becomes clearer if we compare two films with and without detectable metal content (XRD shown in Fig. 4.2a): (i) 13% O_{PP}, 1.5 mTorr and (ii) 13% O_{PP}, 1.9 mTorr. In the former case, $\mu_{Hall} = 9.3$ $cm^2V^{-1}s^{-1}$, while for pure SnO, μ_{Hall} drops to 3.8 $cm^2V^{-1}s^{-1}$. A similar trend is observed at 1.8 mTorr process pressure for 11% O_{PP} and 13% O_{PP}, where the presence of metallic tin (Fig. 4.1b) boosts the mobility in the 11% O_{PP} film ($\mu_{Hall} = 15.2$ $cm^2V^{-1}s^{-1}$). When metallic tin becomes the dominant phase, the films show n-type conduction as observed under the 7% O_{PP}, 1.5 mTorr condition (back of Fig. 4.4). Thus, the amount of embedded Sn must be precisely controlled to obtain the high mobility. As mentioned previously, at 1.8 mTorr deposition pressure, the amount of excess Sn increased from undetectable by XPS to nearly 5 at% as the oxygen partial pressure (O_{PP}) was reduced from 15% to 7%. At the optimum mobility point (P = 1.8 m Torr, O_{PP} = 9%), the Sn metal content was around 3 at%. Finally, the phase map in Fig. 4.1a shows that the films deposited at O_{PP} of 15% and 2 mTorr are amorphous. These films were in fact too resistive to measure and we assumed mobility to be essentially zero.

4.3 Density Functional Theory Simulations

Since the mixed phase tin monoxide films (mp-SnO) exhibit the highest Hall mobility, it is important to understand how this mixture of phases results in mobility improvement. The conduction band minima (CBM) of n-type metal oxide semiconductors are mainly formed of spatially spread s orbitals of the metal cations exhibiting large electron mobility[18,22], while the valence band maxima (VBM) is mainly formed of localized and anisotropic O *2p* orbitals, which results in low hole mobility[3], as previously discussed in Chapter 2. SnO has a larger and better hole mobility owing to its hybridized orbitals, as the VBM has nearly equal contributions of the Sn *5s* and O *2p* orbitals[30,31]. We believe that small traces of metal cations are advantageous to further reduce the valence band edge localization of the SnO matrix in which the VBM is made of pseudoclosed ns^2 orbitals[22,32].

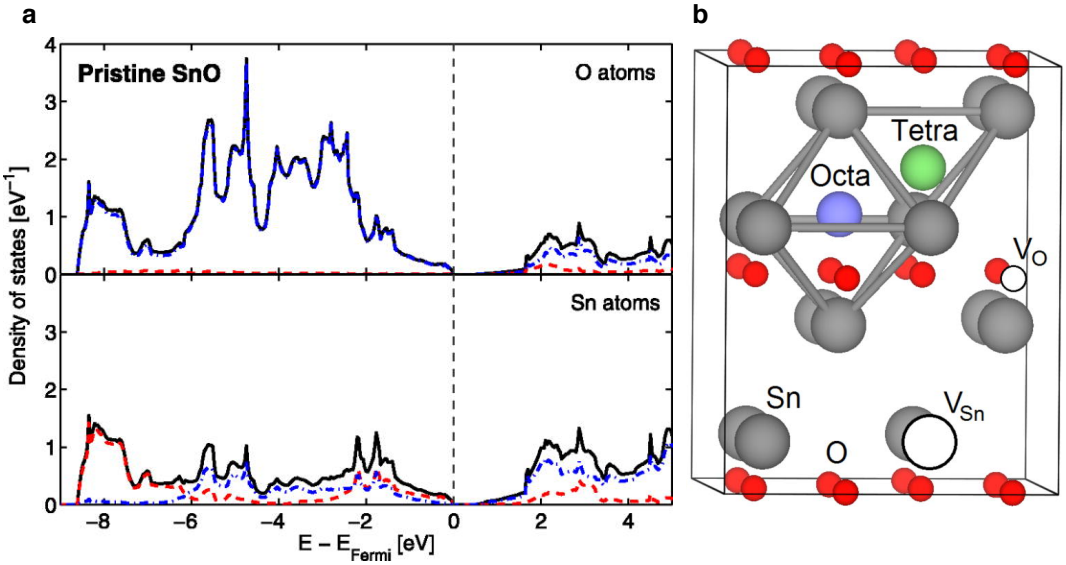

Figure 4.5. Partial density of states of SnO and native defects. a, Pure phase SnO**.** Black solid line: summed valence states (O *2s+2p* and Sn *5s+5p+4d*), red dashed line: summed *s* states (O *2s* and Sn *5s*), blue dashed-doted line: summed *p* states (O 2p and Sn *5p*).Fermi energy is set to the top of the valence band. **b,** Native defects in SnO. *From Granato et al.*[33]

Density functional theory (DFT) simulation studies, suggest that defects generated under Sn-rich growth conditions (Sn interstitial and O vacancy), give a more metallic character to the valence band of SnO. Due to the relatively large amounts of Sn metal second phase, we presume that some point defects, particularly Sn metal interstitials, will also exist in the lattice of SnO. Thus, we have studied the changes in the density of states near the valence band maximum in pure SnO films and compared the results to SnO films in which interstitial tin atoms have been introduced into the SnO lattice. Figure 4.5a shows the averaged partial density of states (DOS) of the orbitals of the lattice atoms in pure SnO: Sn_{latt} 5*s*, Sn_{latt} 5*p*, and O_{latt} 2*p*. In comparison, Figure 4.6 shows the density of states of SnO with tin vacancy (V_{Sn}), oxygen interstitial (O_i), oxygen vacancy (V_O), and tin interstitial (Sn_i) defects (depicted in Figure 4.5b). Only interstitial defects in the octahedral site have been considered for analysis, as it has been shown to be the most stable site[30]. For the V_{Sn} defect, a lowering of the Fermi level is observed (Fig.4.6a), indicating an acceptor behavior, consistent with the analysis done by Togo *et al.*[30] and previously discussed in section 2.2. Nevertheless, along with the Oi defect (Fig. 4.6b), there is no significant change to the VB edge compared to the pure phase SnO in Figure 4.5a. As hole transport mainly occurs in the VBM, these defects do not show any significant impact to improve the hole mobility. In contrast, V_O and Sn_i defects show a strong modification of the VBM. For the V_O the Sn *5p* states increase considerably, and the contribution of the metal cation orbitals (Sn *5s* + Sn *5p*) is now around twice the contribution of the O *2p* orbitals (Fig. 4.6c). Similar effect is observed on the case of Sn_i, with additional *5p* orbitals near the VBM introduced by the Sn_i defect (Fig. 4.6d), resulting in a metal dominated region near the VBM, which results advantageous for enhancing the hole transport due to the more disperse character of the metallic bands[18,22,32,34].

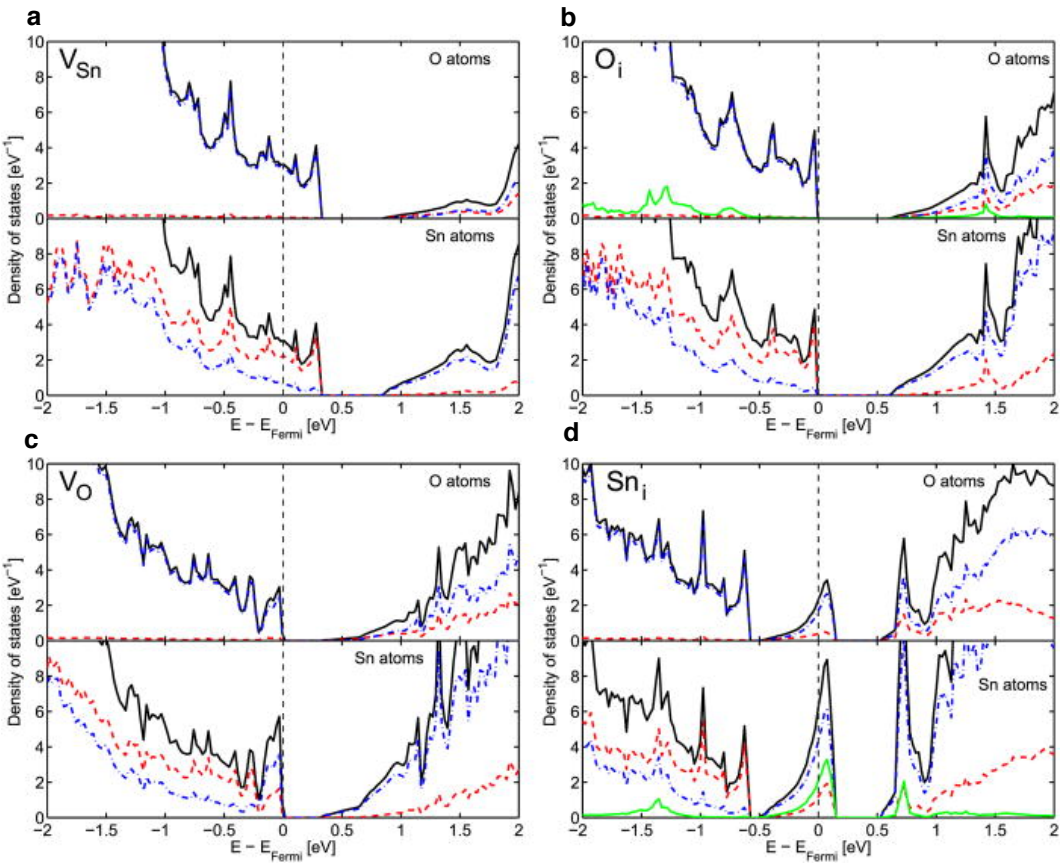

Figure 4.6. Partial density of states of defective SnO supercell. a,Tin vacancy; **b,** Oxygen interstitial; **c,** Oxygen vacancy; **d,** Tin interstitial. Black solid line: summed valence states (O *2s+2p* and Sn *5s+5p+4d*), red dashed line: summed *s* states (O *2s* and Sn *5s*), blue dashed-doted line: summed *p* states (O 2p and Sn *5p*). The green solid line represents the *p* states of the corresponding interstitial atom. The energy is measured in relation to the Fermi level (vertical dashed line). *From Granato et al.*[33]

The concentration of the interstitial Sn atoms used in the simulation is 2.8 at%, which corresponds to introducing one interstitial Sn atom to the supercell used in the DFT simulations. Looking first at the pure SnO case, the DOS in Fig. 4.5 shows that the conduction band (CB) above 0.5 eV is dominated by the Sn_{latt} 5*p* orbitals, while the edge of the valence band (VB) around 0 eV has similar contributions of the O_{latt} *2p* and Sn_{latt} *5s* states, resulting in hybridized orbitals that reduce the O_{latt} *2p* orbital localization, as observed in previous works[30,31]. This is different from typical metal oxides, in which the CB is formed by the spatially spread *s* orbitals of the metal while the VB is dominated by the very localized

O_{latt} 2*p* states. This typical configuration (localized O 2*p* orbitals in the VB) reduces hole mobility because the holes are trapped in the localized oxygen states. However, the Sn_{latt} 5*s* mixing at the edge of the VB at 0 eV gives the holes a more delocalized character in SnO, improving its p-type mobility[32,34,35]. In other words, the p-type character of SnO arises from its hybridized orbitals at the VB, which gives the O 2*p* orbitals a more delocalized character as compared with typical metal oxides. We can therefore conclude that the SnO+Sn_i (Fig. 4.6d) case has substantially more delocalized O_{latt} 2*p* orbitals (less holes trapped) when compared to pure SnO (hybridized Sn_{latt} 5*s* O_{latt} 2*p* orbitals) due to the higher contribution of the delocalized Sn_i 5*p* states to the VB. Thus higher hole mobility can be expected in mp-SnO films, which is what we observe experimentally.

The contribution of the metal cation orbitals (particularly Sn *5p* orbitals) is increased near the VBM under the presence of Sn interstitial. Nevertheless, the amount of additional metal must be carefully controlled not to compensate the holes generated by the Sn vacancies, which give SnO its p-type character. Mobility improvement by incorporating excess Sn occurs only up to a point determined by the process conditions used, as clearly shown in Fig. 4.4. In fact, we observe that increasing Sn metal content beyond a certain point in the mp-SnO films degrades both the Hall and field-effect mobility (*e.g.* 7% O_{PP} films). We believe that this result is due to the fact that further increasing the Sn metal concentration increases carrier scattering and therefore reduces hole mobility. The presence of metallic tin can contribute to carrier scattering in several ways. For instance, too much tin can introduce additional point defects (*e.g.* additional Sn interstitials in the SnO lattice, free Sn atoms and clusters in the grain boundaries, or dislocations) that act to scatter the charge carriers. It is evident that more defects are introduced in mixed phase films with higher

content of metallic Sn as presented in the lattice strain analysis (Fig. 4.2c). Basically, we find that the pure phase SnO films (lower right-hand side of Fig. 4.2c) exhibited lower strain compared to mp-SnO films. In contrast, mp-SnO films with high levels of metallic tin (upper left-hand side of Fig. 4.2c) exhibit higher strain levels, indicating larger concentration of defects in the films (*e.g.* Sn interstitials in the SnO lattice, free Sn atoms and clusters in the grain boundaries, dislocations). These defects, if present in significant amounts, can enhance carrier scattering, leading to a decrease in hole mobility. Therefore, the optimum mobility in our tin monoxide films is determined by a trade-off between: **(i)** the extent of valence band modulation caused by additional metal cations, and **(ii)** the amount of charge carrier scattering from defects induced by the presence of increasing amounts of metallic tin in the mp-SnO films.

4.4 Device Characterization

This section describes the characterization of the fabricated fully transparent and flexible devices showing record performance followed by a brief description of the device engineering done to achieve this performance.

4.4.1 Transparent Rigid and Flexible TFTs

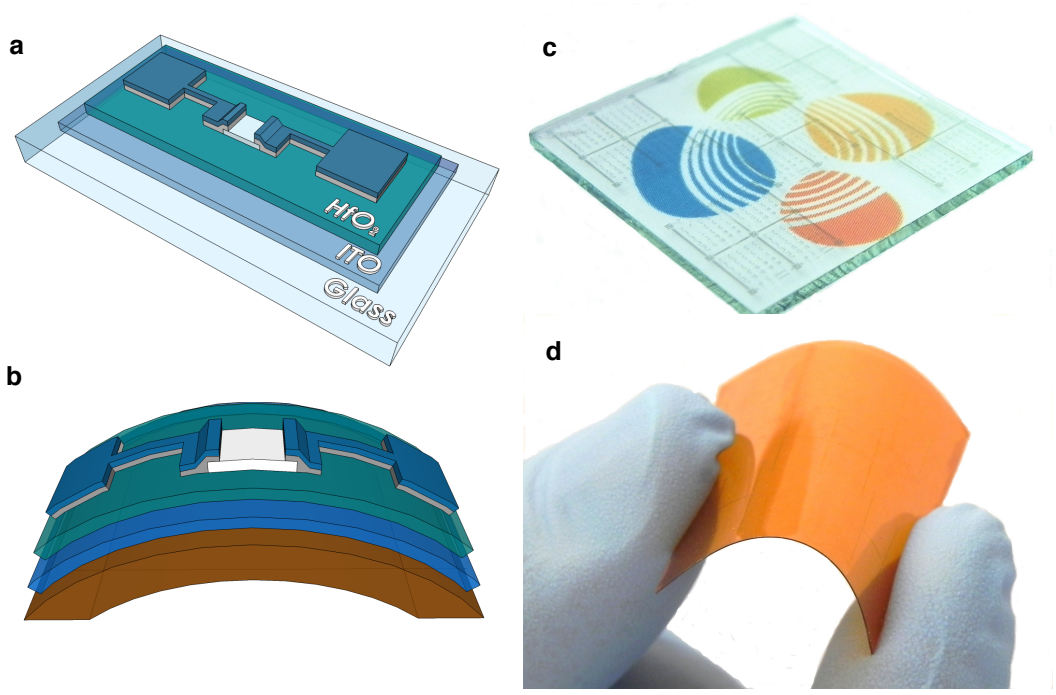

Figure 4.7. Device structure. Conceptual designs of the fabricated devices. **a**, fully transparent devices on glass and **b**, flexible devices on translucent polyimide (150 nm ITO gate electrode/220 nm HfO_2 gate dielectric/15 nm SnO_x active channel/8 nm Ti, 90 nm ITO source and drain electrodes). Photograph of **c**, a fully transparent device and **d**, a flexible one.

The conceptual design of the fully transparent and flexible devices is depicted in Figures 4.7a and 4.7b, whereas Figures 4.7c and 4.7d show the actual fabricated devices. Figs. 4.8a and 4.8b depict the output characteristics of fully transparent and flexible devices produced at 9% O_{PP}, P=1.8 mTorr, respectively, in which clear linear and saturation regions can be observed. The absence of current crowding at low source-to-drain voltages (V_{DS}) indicates an Ohmic contact of Ti/ITO with SnO. Figures 4.8c and 4.8d present the transfer characteristics with V_{DS}=-1V for devices produced at 1.8 mTorr with different O_{PP}. In all cases, p-type behavior is observed, since the holes are generated at negative gate voltages (V_{GS}). Fig. 4.8c and Fig. 4d also show that the gate leakage currents are very low and are around 10^{-12} Amps. Linear-region field-effect mobility (μ_{FE}) and threshold voltage (V_T) were

calculated from the transfer characteristics and the obtained values are shown in Figs. 4.9a and 4.9b, respectively. To rule out any artifacts in the TFT measurements, all the devices were characterized following the procedure recommended by J.F. Wager[36] (discussed in section 3.4.3) with multiple W/L ratios. The mobility data shown in Fig. 4.9a were extracted from devices with W/L =1, but W/L ratios from 1 to 10 were tested and gave very similar results as shown in Figure 4.9c for the set of fully transparent devices. Multiple, dual sweep I_{DS} vs V_{GS} scans were performed and it has been found that the devices belong to type II in Wager's classification[36] which is *non-equilibrium*, *steady-state behavior*. An effective hysteresis density of $N_{HYS}=1.8645\times10^{12}$ cm^{-2} with a threshold voltage shift of 3.67 V at a V_{GS} scan rate SR=366 mV sec^{-1} is observed for the best performance device (9% O_{PP}, 1.8mTorr) as shown in Fig. 4.9d with a W/L ratio of 10. The transparent TFTs on glass have a maximum μ_{FE} of 6.75 $cm^2V^{-1}s^{-1}$ while the mobility is nearly 20% lower for the TFTs made on flexible substrates. Results of SnO surface inspection by atomic force microscopy using the same area as in actual devices (50 μm X 50 μm) are presented in Figs. 4.9e and 4.9f for glass and plastic substrates, respectively. It is evident that the mixed phase (mp-SnO) films deposited on flexible substrates have a higher surface roughness. The lower mobility of devices on flexible polyimide substrate can thus be attributed to the higher surface roughness of this substrate, which increases carrier scattering and hence reduces the mobility. The threshold voltage (V_T) of the flexible devices matches well with the V_T of the rigid ones. The gate leakage current in the on state was measured in the pA range, indicating good insulating properties of the dielectric layer. For all O_{PP} conditions, the I_{ON}/I_{OFF} ratio is around 10^3, leading to a maximum of $6x10^3$ for the highest mobility device.

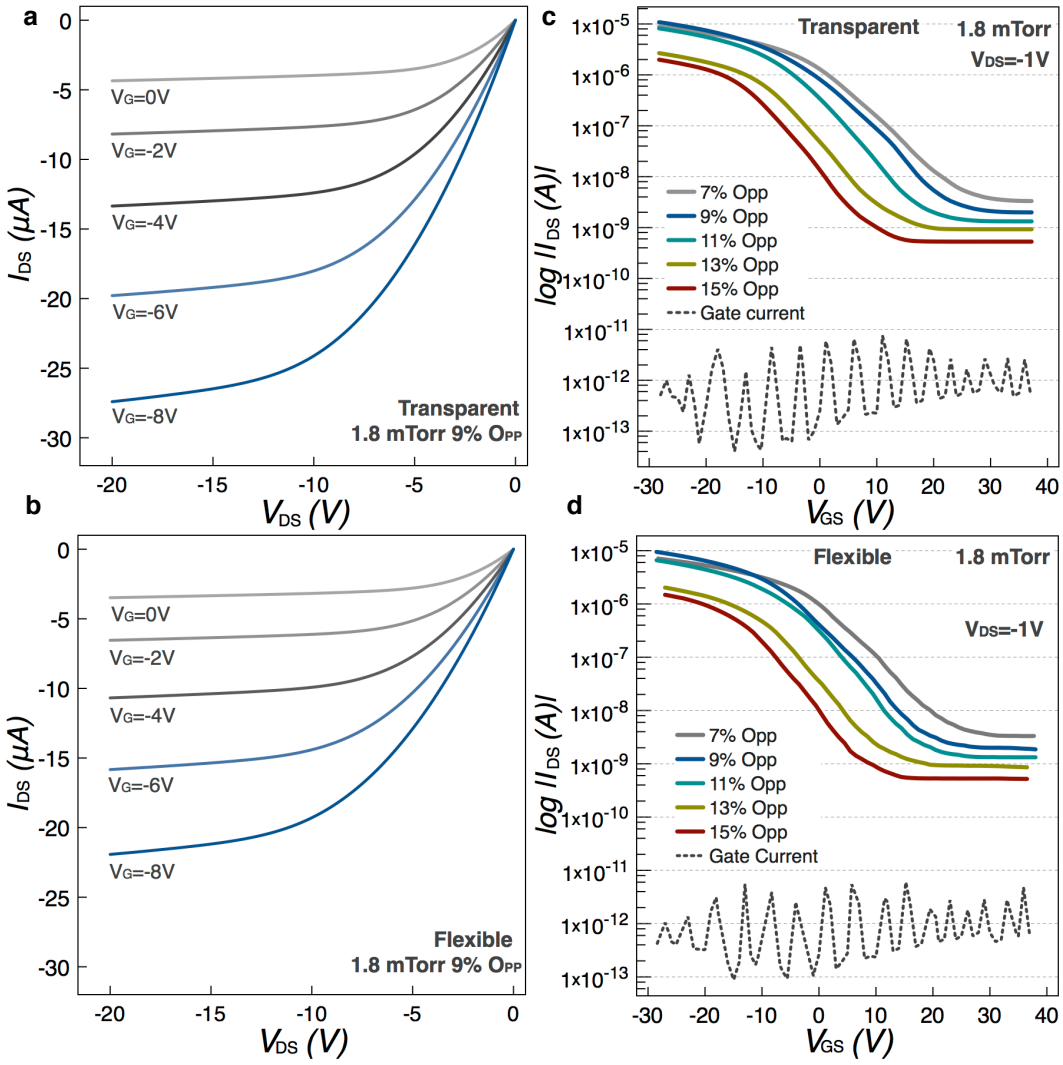

Figure 4.8. Transfer and output characteristics. a,b, Output and transfer characteristics of devices fabricated on glass (fully transparent) and **c,d**, devices fabricated on polyimide (flexible) with a channel width of 50 μm and length of 50 μm.

As expected, devices produced at different O_{PP} exhibit different behaviors. μ_{FE} follows a similar trend to that of μ_{Hall} shown in Fig. 4.4. The hole mobility reaches its maximum in devices (and films) deposited at 9% O_{PP}, 1.8 mTorr, which corresponds to the mp-SnO films with ~3 at% Sn. Competing contributions of metal cations are also observed in our devices: TFTs fabricated with mp-SnO films have higher mobility than those

fabricated with pure SnO. It is obvious that the presence of small amounts of Sn enhances hole mobility by promoting orbital delocalization in the valence band, but this delocalization has to be controlled so that the scattering effects do not cancel out the mobility enhancement. The shift of V_T as a function of O_{PP} also gives an indication of the crucial role of the embedded metallic Sn. V_T is positive for 7% O_{PP}, then becomes negative and further decreases as the Sn concentration decreases (or the SnO phase becomes dominant) with a value of -1V for the best-performing device. TFTs fabricated at 7% O_{PP}, when more metallic Sn is present, exhibit a positive V_T, indicating the presence of large number of free carriers. As O_{PP} increases from 9% to 15%, a significant decrease in I_{DS} is observed, indicating a decrease in carrier concentration (as seen in Table 4.1), as is also evident from the shifting of V_T *in negative direction*.

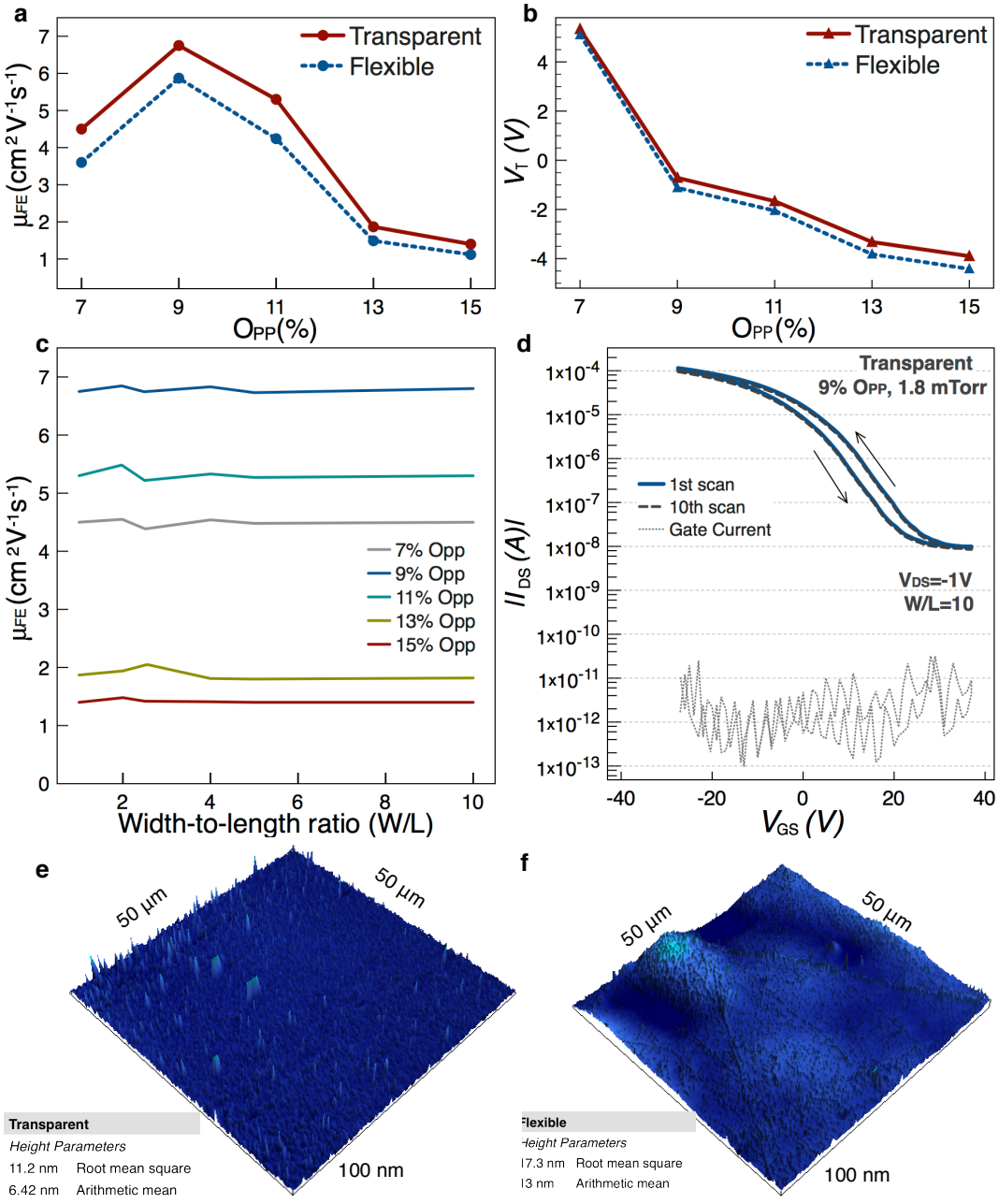

Figure 4.9. TFT parameters and surface morphologies. a, Linear field-effect mobility (μ_{FE}) as a function of O_{PP} for the devices fabricated for this study. **b**, Threshold voltage (V_T) comparison of the fully transparent and flexible devices. **c,** Linear field-effect mobility as a function of width-to-length ratio for the transparent samples. **d**, Multiple, dual-sweep transfer curves for a device with a W/L=10 at the best performance condition (9% O_{PP}, 1.8 mTorr). **e,f**, AFM surface profiles for the mp-SnO films deposited on glass and polyimide substrates, respectively.

The TFT data correlates very well with the Hall mobility data, although the actual μ_{FE} is smaller than μ_{Hall} regardless of the deposition conditions. This is typical behavior for oxide semiconductors and likely arises from defects near the valence band maximum and/or hole traps at the semiconductor-dielectric interface. Extracted sub-threshold swing data in the range from 7.63 $Vdec^{-1}$ to 10 $Vdec^{-1}$ indicate that there is a high density of trap states in the semiconductor and/or at the interface with the dielectric. Optimization of the semiconductor-dielectric interface has been shown to play a crucial role in maximizing device performance[37]. Better device engineering to decrease the number of trap states should allow the μ_{FE} to approach μ_{Hall} more closely. We note here that our field-effect mobility stands out as the highest reported up-to-date for any p-type transparent oxide semiconductor, as shown in Figure 4.10a where the two most promising p-type oxides are compared.

Devices deposited at the same conditions show very stable and reproducible behavior. Table 4.2 shows the mobility, threshold voltage, and on-to-off current ratio values for devices fabricated on glass for the different O_{PP} at a fixed deposition pressure of 1.8 mTorr and as function of different width-to-length ratio. All devices show consistent results regardless of the channel dimension. Devices fabricated at different deposition conditions show different V_T values. We attribute this behavior to the difference in carrier density observed in our Hall effect measurements (Table 4.1) but also to the density of trap states at the semiconductor/dielectric interface (qualitatively estimated from the subthreshold swing) that significantly varies with varying the deposition conditions. Nevertheless, further investigation of the SnO/HfO_2 interface is required to accurately determine the number of trap states and its influence on V_T. We believe that modulation of the carrier density, via

adequate doping to reduce the number of free carriers, is the method to go for V_T optimization, as well as to decrease the off current to improve the I_{ON}/I_{OFF}.

O_{PP}	W/L	1	2	2.5	4	5	10	Average	Max	Min
7%	μ_{FE}	**4.50**	**4.73**	**4.32**	**4.54**	**4.48**	**4.50**	**4.51**	**4.73**	**4.32**
	V_T	5.01	5.02	5.00	4.89	5.02	5.02	4.99	5.02	4.89
	I_{ON}/I_{OFF}	2.71E+03	2.35E+03	2.36E+03	2.34E+03	4.68E+03	4.69E+03		4.69E+03	2.34E+03
9%	μ_{FE}	**6.75**	**7.08**	**6.53**	**6.83**	**6.73**	**6.80**	**6.79**	**7.08**	**6.53**
	V_T	-1.05	-1.04	-1.20	-1.20	-1.20	-1.05	-1.12	-1.04	-1.20
	I_{ON}/I_{OFF}	6.46E+03	6.60E+03	6.61E+03	6.63E+03	1.31E+04	1.32E+04		1.32E+04	6.46E+03
11%	μ_{FE}	**5.30**	**5.57**	**5.09**	**5.33**	**5.27**	**5.30**	**5.31**	**5.57**	**5.09**
	V_T	-2.01	-2.01	-1.99	-2.02	-1.88	-2.03	-1.99	-1.88	-2.03
	I_{ON}/I_{OFF}	5.96E+03	5.81E+03	5.82E+03	5.80E+03	1.15E+04	1.16E+04		1.16E+04	5.80E+03
13%	μ_{FE}	**1.87**	**1.94**	**1.73**	**1.81**	**1.80**	**1.82**	**1.83**	**1.94**	**1.73**
	V_T	-3.66	-3.49	-2.99	-2.99	-3.03	-3.17	-3.22	-2.99	-3.66
	I_{ON}/I_{OFF}	3.09E+03	3.33E+03	3.34E+03	3.37E+03	6.64E+03	6.65E+03		6.65E+03	3.09E+03
15%	μ_{FE}	**1.40**	**1.48**	**1.35**	**1.41**	**1.40**	**1.40**	**1.41**	**1.48**	**1.35**
	V_T	-4.23	-4.29	-4.27	-4.25	-4.28	-4.25	-4.26	-4.23	-4.29
	I_{ON}/I_{OFF}	4.03E+03	4.04E+03	4.06E+03	4.03E+03	8.04E+03	8.05E+03		8.05E+03	4.03E+03

Table 4.2 Linear region field effect mobility (cm^2/Vs), threshold voltage (V) and on-to-off current ratio of devices as a function of the O_{PP} at a deposition pressure P=1.8 mTorr for different W/L ratios.

The transmittance spectra of the gate electrode and the gate dielectric, the mp-SnO layer, and the final stack are shown in Fig. 4.10b. The average optical transmission of the 15 nm mp-SnO layer in the visible region (400 to 700 nm) is 92%, while it is 63% for the entire device, mainly limited by the Ti layer. The use of the Ti source and drain contact interlayer results from the observation of enhanced device performance over some other contacts like Au, Ni, Pt and ITO (discussed in the next section). The optical bandgap, E_G, has been estimated from the absorption coefficient, α, calculated as a function of the incident photon energy, $h\nu$. E_G was obtained by extrapolating the linear portion in the $(\alpha h\nu)^2$ vs $h\nu$ plot, as shown in Fig. 4.10c by the dotted lines, in accordance with the principles described in section 3.2.4. The estimated E_G ranges from 2.65 eV for 7% O_{PP} to 2.92 eV for 15% $O_{PP,}$ matching well with that of pure SnO[19,22].

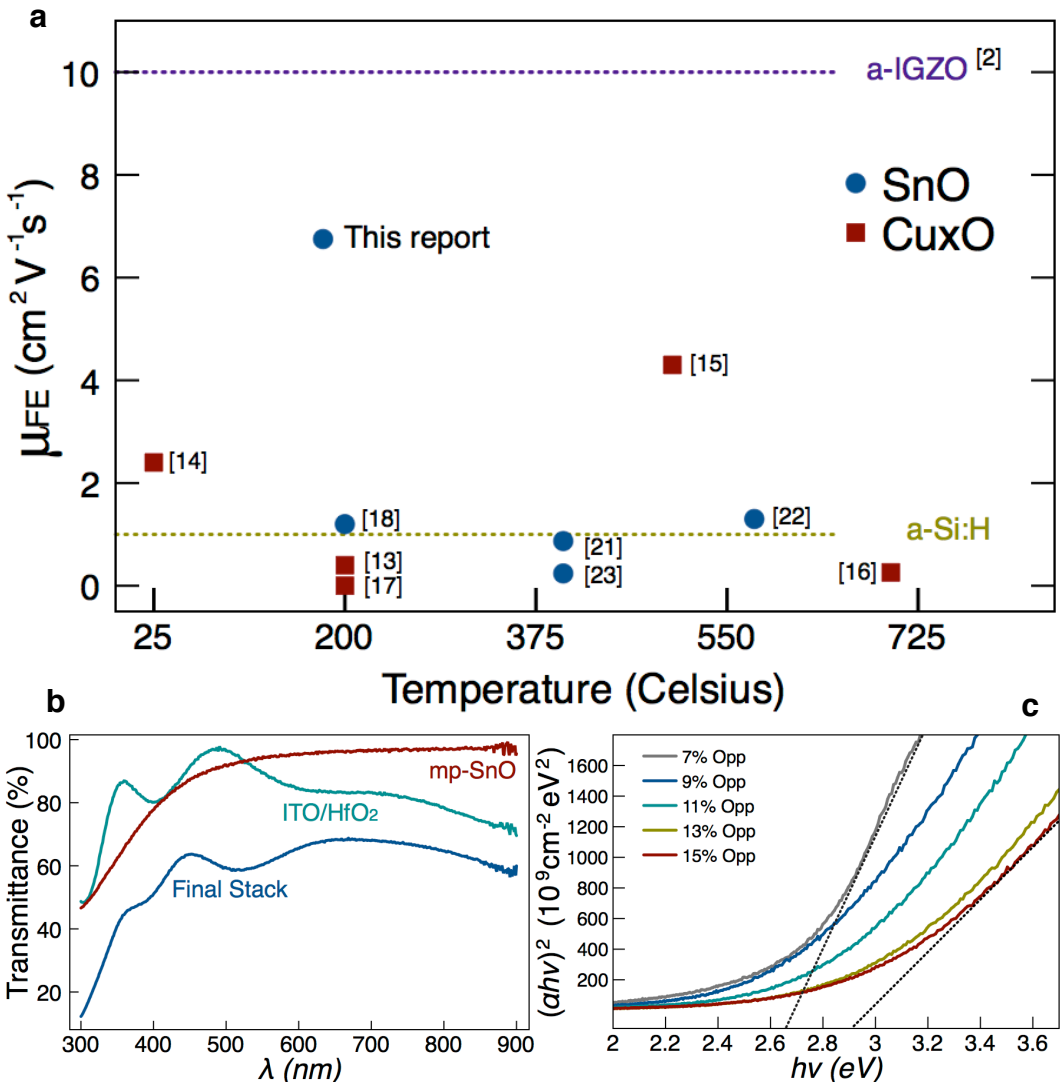

Figure 4.10. Field effect mobility vs temperature and optical characterization. a, Comparison of reported field effect mobility versus maximum processing temperature (either deposition or post annealing) for leading p-type oxides. The reference is indicated in square brackets. Mobility of a-IGZO (n-type) and a-Si:H are not plotted as a function of the temperature and are used just for comparison. **b**, Transmission spectra of the components of the TFT. **c**, Tauc plot of the optical band gap extraction (indicated by the dotted line) of the films deposited at 1.8 mTorr.

4.4.2 Device Engineering

Source and drain contacts, thicknesses of the active channel, and the type of gate dielectric have been analyzed in order to maximize the device performance. Having ohmic contact between the source and drain (S&D) electrodes and the active channel is very

important to maximize the drain current. This is achieved by having contacts with a work function close to the Fermi level of SnO. In the estimated band diagram of SnO discussed in section 2.2, the VBM is located around 5.8 eV, so it was expected that metals with high work function are advantageous to be used as S&D electrodes. In our experiments, we have fabricated devices with S&D contacts of ITO (4.6-4.8 eV), platinum (5.12 – 5.93), nickel (5.04 – 5.35), and titanium (4.3 – 4.4 eV), but observed higher mobility (and higher I_{ON}) when using Ti, as shown in transfer characteristics of Figure 4.11a. μ_{FE} and V_T of these devices are shown in the inset of Fig. 4.11a. Due to the relative lower work function of Ti, it is very unlikely to have band alignment with SnO, nevertheless it is very likely the Ti layer is getting oxidized at the SnO/Ti interface as we perform the thermal treatment after source and drain deposition. The oxidation of the Ti layer causes the Ti effective work function to go to a deeper energy level[38] thus a better band alignment is observed between the SnO VBM and the Ti S&D contacts.

As the use of Ti S&D contacts has been shown to be advantageous to maximize device performance, a very thin layer (8 nm) of this material is deposited followed by a thicker layer of ITO to render the device transparent. Using only ITO as S&D electrode showed to supply additional oxygen to the SnO layer facilitating the phase transformation to SnO_2. The enhanced device performance when using Ti/ITO electrodes results from the oxidation of the Ti layer, modifying its effective work function to a deeper energy level, which is closer to the VBM of the mp-SnO films, while recognizing some degree of uncertainty on the estimated band structure of SnO. Nevertheless, further investigation of the band structure of SnO, and particularly of our mixed phase films is required for further enhancement of the device performance.

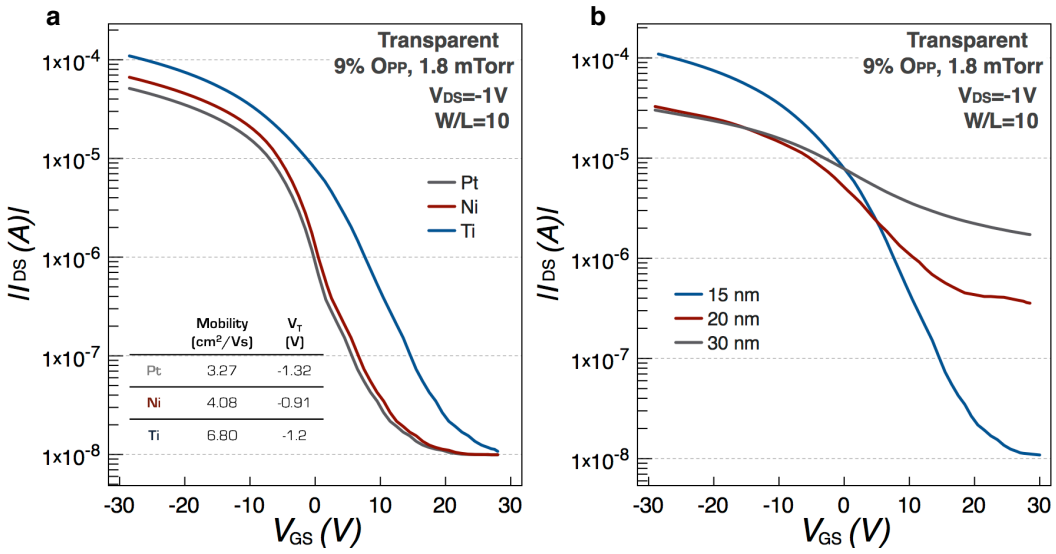

Figure 4.11. Transfer characteristics for different conditions. a, Different source and drain contacts **b**, Different thicknesses of the SnO active layer. All devices using HfO_2 as the gate dielectric and deposited on glass substrates.

We have studied the device performance as a function of active thickness ranging from 40 nm down to 15 nm in 5 nm steps. The best device performance is observed when using a 15 nm thick SnO layer. Figure 4.11b shows the transfer characteristic of devices fabricated at the deposition conditions showing the best mobility (9% O_{PP},1.8 mTorr). We couldn't find working devices with a channel thickness below 15 nm, mainly attributed to the surface roughness of the substrate (measured to be 11.2 nm after ITO and HfO_2 deposition, as shown in Figure 4.9e) which may prevent from having a continuous channel. Improving the surface roughness, by choosing a flatter substrate (*e.g.* Si wafer) may help to go further down and continue with the trend shown in the Figure 4.11b. By decreasing the SnO channel thickness we observe lower off current and more stable TFT performance. The effect of the channel thickness in the TFT performance is a commonly observed phenomenon, but the mechanisms behind, remain on debate and seems to be material dependent.[39] In our devices we surmise the thicker the channel the higher the number of

defects, specially the surface defects that respond to the applied gate bias. In the 30 nm TFT the I_{ON}/I_{OFF} ratio is very low and mainly limited by the large off current. The off current significantly decreases by decreasing the channel thickness, as shown in the transfer characteristics in Fig. 4.11b. Furthermore, the repeatability and consistency of measurement is much better for the 15 nm thick devices, indicating non-steady-state behavior of thicker devices annealed at the optimized temperature of 180 °C.

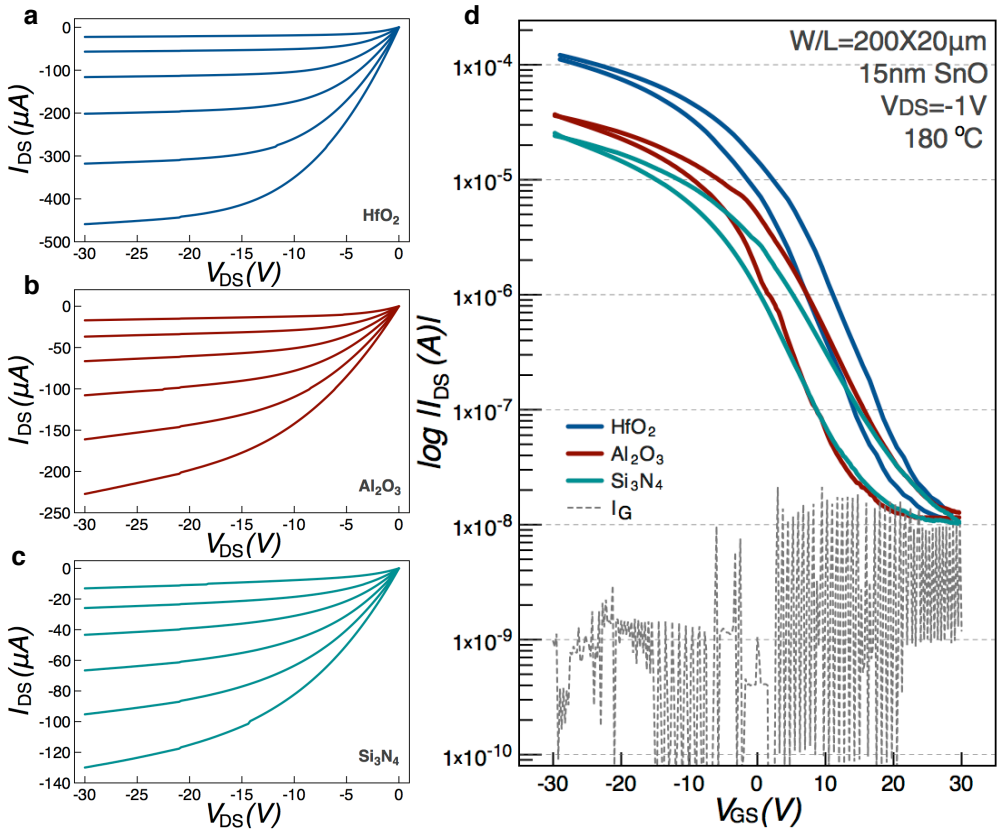

Figure 4.12. Output and transfer characteristics for different gate dielectrics. Output characteristics (V_G from 0 to -15 V at -3 V steps) for **a**, HfO_2; **b**, Al_2O_3; **c,** Si_3N_4; **d,** Transfer characteristics as a function of gate dielectric. All devices using ITO as gate electrode, 15 nm thick SnO, Ti/ITO source and drain electrodes and deposited on glass substrates.

Figure 4.12 shows the output and transfer characteristics of devices with three different gate dielectric materials (~220 nm thick): HfO_2 (ε≈14.4), Al_2O_3 (ε≈8.1) and Si_3N_4

(ε≈ 7.2) using the optimized channel thickness of 15 nm SnO, Ti/ITO S&D electrodes, and post deposition annealing temperature of 180 °C. Good saturation and *depletion-mode* operation is observed in the output characteristics regardless of the gate dielectric being used. Transfer characteristics show higher I_{ON} for HfO_2 device as well as lower hysteresis between the positive-going and negative-going scans. Table 4.3 summarizes the important device parameters for the three different dielectrics at the optimized post deposition annealing temperature of 180 °C. As thin film transistors are capacitance-operated devices it is expected higher dielectric constant materials to be beneficial for achieving higher drain current and higher mobility.[40,41] In our devices, the higher the dielectric constant of the gate dielectric, the higher the mobility. $\mu_{FE} \approx 2.9$ $cm^2V^{-1}s^{-1}$ is observed for Si_3N_4, increasing to 4.3 $cm^2V^{-1}s^{-1}$ for Al_2O_3 devices, and reaching a maximum of 6.8 $cm^2V^{-1}s^{-1}$ for HfO_2. Threshold voltage reduces with increasing dielectric constant, but there is no clear relation with the density of interfacial trap states (D_{it}) or the effective hysteresis density (N_{HYS}), as both parameters remain high regardless of the gate dielectric material being used. The advantage of using HfO_2 is that it yields higher I_{ON} and higher μ_{FE}, lower threshold difference between the positive- and negative-going scans (ΔV_T), and lower subthreshold swing (SS). Nevertheless, the high number of interfacial trap states indicates a lot of room for improvement, perhaps by using gate dielectrics of higher dielectric constants, or by improving the gate dielectric/semiconductor interface.

		W/L					
		1	2	2.5	4	5	10
HfO_2	μ_{FE} (cm^2/Vs)	**6.75**	**7.08**	**6.53**	**6.83**	**6.73**	**6.80**
	V_T (V)	-1.05	-1.04	-1.20	-1.20	-1.19	-1.20
	I_{ON}/I_{OFF}	6.46×10^3	6.60×10^3	6.61×10^3	6.63×10^3	1.31×10^4	1.19×10^4
	ΔV_T (V)	3.58	3.60	3.59	3.62	3.61	3.63
	SS (V/dec)	7.12	7.18	7.30	6.98	7.38	7.41
	D_{it} (#/eV cm^2)	4.48×10^{13}	4.52×10^{13}	4.59×10^{13}	4.39×10^{13}	4.64×10^{13}	4.66×10^{13}
	N_{HYS} (#/cm^2)	1.33×10^{12}	1.34×10^{12}	1.34×10^{12}	1.35×10^{12}	1.35×10^{12}	1.35×10^{12}

		W/L					
		1	2	2.5	4	5	10
Al_2O_3	μ_{FE} (cm^2/Vs)	**4.26**	**4.23**	**4.22**	**4.27**	**4.28**	**4.30**
	V_T (V)	-1.39	-1.37	-1.43	-1.67	-1.48	-1.58
	I_{ON}/I_{OFF}	1.28×10^3	3.07×10^3	3.22×10^3	3.34×10^3	3.48×10^3	3.50×10^3
	ΔV_T (V)	4.82	4.85	4.87	4.94	4.98	5.05
	SS (V/dec)	8.01	8.05	8.07	8.13	8.15	8.18
	D_{it} (#/eV cm^2)	2.54×10^{13}	2.55×10^{13}	2.56×10^{13}	2.58×10^{13}	2.58×10^{13}	2.59×10^{13}
	N_{HYS} (#/cm^2)	9.05×10^{11}	9.10×10^{11}	9.14×10^{11}	9.27×10^{11}	9.35×10^{11}	9.48×10^{11}

		W/L					
		1	2	2.5	4	5	10
Si_3N_4	μ_{FE} (cm^2/Vs)	**2.92**	**2.86**	**2.89**	**2.91**	**2.92**	**2.94**
	V_T (V)	-3.05	-3.05	-3.13	-3.19	-3.21	-3.27
	I_{ON}/I_{OFF}	2.47×10^3	2.49×10^3	2.54×10^3	2.66×10^3	2.68×10^3	2.63×10^3
	ΔV_T (V)	5.12	5.14	5.16	5.24	5.22	5.28
	SS (V/dec)	8.98	9.05	9.11	9.14	9.16	9.17
	D_{it} (#/eV cm^2)	3.02×10^{13}	3.04×10^{13}	3.06×10^{13}	3.07×10^{13}	3.08×10^{13}	3.08×10^{13}
	N_{HYS} (#/cm^2)	1.02×10^{12}	1.02×10^{12}	1.03×10^{12}	1.04×10^{12}	1.04×10^{12}	1.05×10^{12}

Table 4.3 Important TFT parameters for the different gate dielectrics used in this study as a function of W/L ratios.

4.5 Conclusions

In conclusion, we have demonstrated the highest hole mobility reported to date for a p-type oxide processed at low temperature by careful process control. A detailed phase map for nanoscale physical vapor deposition of tin monoxide has been developed for the first

time. We have shown that control of the phase formation of tin monoxide films greatly enhances the carrier mobility yielding μ_{Hall} = 18.7 $cm^2V^{-1}s^{-1}$. Residual second phases must be carefully optimized to obtain maximum hole mobility. Furthermore, we have demonstrated record device performance for a transparent p-type oxide semiconductor on both rigid and flexible substrates, with a linear-region field-effect mobility of 6.75 $cm^2V^{-1}s^{-1}$ and 5.87 $cm^2V^{-1}s^{-1}$, respectively, a threshold voltage of -1V and a maximum I_{ON}/I_{OFF} ratio of 10^4.

4.6 Methods

4.6.1 Film Fabrication and Characterization

Pure SnO and mixed phase (mp-SnO) films were deposited onto soda-lime glass substrates by direct current (DC) reactive magnetron sputtering using a 2 in (5.08 cm) Tin metal target from Angstrom Science, Canada with a purity of 99.99%. The reactive sputtering was performed at room temperature in a mixture of argon and oxygen gasses, in an AMOD-model thin film deposition tool designed by Angstrom Engineering. To determine optimal deposition conditions, the oxygen partial pressure was varied from 3% to 50%. The deposition pressure was scanned from 1 to 4 mTorr while the DC power was held at 30 watts (9.55 W/in^2 power density). The distance between the target and the substrate was 20 cm, while the gun is located at 160° with respect to the horizon, achieving a deposition rate of 0.8 Å/s. Post annealing in air was performed in a tube furnace at 180 °C for 30 min. The film thicknesses were measured using a Veeco Dektak 150 surface profilometer and confirmed by cross-sectional transmission electron microscopy (TEM) analysis performed with a FEI Titan ST. High-resolution X-ray diffraction patterns were obtained at room temperature in air by a Bruker D8 Discover diffractometer using the $CuK\alpha_1$ (1.5406 Å) radiation. Carrier density and Hall mobility were extracted from room

temperature Hall effect measurements conducted using a physical property measurement system (PPMS®) from Quantum Design in a Greek-cross patterned film with the Van der Pauw configuration and after magnetoresistance correction. The optical properties were obtained using an evolution 600 UV-VIS spectrophotometer in the wavelength range from 300 nm to 900 nm. Surface morphologies were imaged by an Agilent 5400 SPM AFM system and FEI Helios NanoLab 400S SEM. Crystallite size (D) and lattice strain (ε) were simultaneously calculated using the procedure described in section 3.2.1.

4.6.2 DFT Simulations

Performed by Danilo Granato under the supervision of Prof. Udo Schwingenschlögl (ref. 33)

The electronic structures were calculated by density functional theory using the projector-augmented wave method[42] as implemented in VASP code[43,44]. The electron-electron interaction was treated in the generalized-gradient approximation as parameterized by Perdew, Burke, and Ernzerhof[45]. The supercell considered in the calculations contained 72 atoms (a 3x3x2 supercell). A Sn atom was inserted in the most stable interstitial site which was surrounded by five Sn atoms. This simulated a 2.8 at% concentration of excess Sn. Our optimized lattice parameters of pristine SnO were a = b = 11.60 Å and c = 10.12 Å. In the super cell with the extra Sn atom, the lattice parameters were kept fixed at these values and the atomic positions were optimized. Sn 5s and 5p as well as O 2s and 2p orbitals were considered as valence states. All other orbitals were treated as core states. The energy cut-off was set to be 600 eV and the Brillouin zone was sampled using the Monkhorst-Pack method[46] with a 3x3x3 k-mesh in the self-consistency cycle and a 7x7x7 k-mesh in the calculation of the density of states (DOS). The atomic forces and total energy converged to

less than 0.02 eVÅ^{-1} and 10^{-5} eV, respectively. All numerical parameters were selected after a careful convergence analysis.

4.6.3 TFT Fabrication and Characterization

The bottom gate indium tin oxide (ITO) layers were deposited by radio frequency magnetron sputtering at room temperature. The HfO_2 and Al_2O_3 gate dielectrics (~220nm thick) were deposited on top of 150 nm ITO-coated glass/polyimide substrates by atomic layer deposition using a Cambridge Nanotech system; while the 200 nm thick Si_3N_4 layer was deposited by plasma enhanced chemical vapor deposition. The active layer consisted of 15 nm of SnO deposited at different oxygen partial pressures. The stack was completed with 8 nm electron-beam evaporated Ti and 90 nm sputtered ITO source and drain contacts followed by thermal treatment at 180 °C in air, for 30 min, to crystallize both the SnO and ITO layers. The devices were patterned by photolithography and lift-off technique as described in section 3.3 and measured as indicated in section 3.4. The performance of the TFTs was evaluated on devices with a width-to-length ratio (W/L) of 1 with W and L 50 μm, respectively. TFT parameters were evaluated with the conventional metal-oxide-semiconductor field effect transistor model described section 3.4. The capacitance per unit area of the gate insulator (C_{ox}) was measured to be 60 nFcm^{-2} for HfO_2, 30.2 nFcm^{-2} for Al_2O_3 and 32 nFcm^{-2} for Si_3N_4 with no more than 3% variation in the frequency range from 1 kHz to 1 MHz and an extracted dielectric constants of ~14.4, 8.12 and 7.22 respectively.

4.7 References and Notes

1 Sun, Y. & Rogers, J. A. Inorganic Semiconductors for Flexible Electronics. *Adv. Mater.* **19**, 1897-1916 (2007).

2 Nomura, K. *et al.* Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488-492 (2004).

3 Ginley, D. S., Hosono, H. & Paine, D. C. *Handbook of Transparent Conductors* (Springer, 2010).

4 Kim, B. *et al.* Highly Reliable Depletion-Mode a-IGZO TFT Gate Driver Circuits for High-Frequency Display Applications Under Light Illumination. *Electron Device Letters, IEEE* **33**, 528-530 (2012).

5 Kim, K. M. *et al.* Competitive device performance of low-temperature and all-solution-processed metal-oxide thin-film transistors. *Appl. Phys. Lett.* **99**, 242109-242103 (2011).

6 Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **24**, 2945-2986 (2012).

7 Reuss, R. H. *et al.* Macroelectronics: Perspectives on Technology and Applications. *Proceedings of the IEEE* **93**, 1239-1256 (2005).

8 Kim, M.-G., Kanatzidis, M. G., Facchetti, A. & Marks, T. J. Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing. *Nat Mater* **10**, 382-388 (2011).

9 Arias, A. C., MacKenzie, D. J., McCulloch, I., Rivnay, J. & Salleo, A. Materials and Applications for Large Area Electronics: Solution-BasedApproaches. *Chem. Rev.* **110**, 3-24 (2010).

10 Fortunato, E. M. C. *et al.* Fully Transparent ZnO Thin-Film Transistor Produced at Room Temperature. *Adv. Mater.* **17**, 590-594 (2005).

11 Kim, H. S., Byrne, P. D., Facchetti, A. & Marks, T. J. High performance solution-processed indium oxide thin-film transistors. *J. Am. Chem. Soc.* **130**, 12580-12581 (2008).

12 Nayak, P. K., Hedhili, M. N., Cha, D. K. & Alshareef, H. N. High performance solution-deposited amorphous indium gallium zinc oxide thin film transistors by oxygen plasma treatment. *Appl. Phys. Lett.* **100**, 202106 (2012).

13 Sung, S.-Y. *et al.* Fabrication of p-channel thin-film transistors using CuO active layers deposited at low temperature. *Appl. Phys. Lett.* **97**, 222109 (2010).

14 Yao, Z. Q. *et al.* Room temperature fabrication of p-channel Cu2O thin-film transistors on flexible polyethylene terephthalate substrates. *Appl. Phys. Lett.* **101**, 042114 (2012).

15 Zou, X. *et al.* Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-k HfON Gate Dielectric. *Electron Device Letters, IEEE* **31**, 827-829 (2010).

16 Matsuzaki, K. *et al.* Epitaxial growth of high mobility Cu2O thin films and application to p-channel thin film transistor. *Appl. Phys. Lett.* **93**, 202107 (2008).

17 Fortunato, E. *et al.* Thin-film transistors based on p-type Cu2O thin films produced at room temperature. *Appl. Phys. Lett.* **96**, 192102 (2010).

18 Fortunato, E. *et al.* Transparent p-type SnOx thin film transistors produced by reactive rf magnetron sputtering followed by low temperature annealing. *Appl. Phys. Lett.* **97**, 052105 (2010).
19 Guo, W. *et al.* Microstructure, optical, and electrical properties of p-type SnO thin films. *Appl. Phys. Lett.* **96**, 042113 (2010).
20 Lee, H.-N., Kim, H.-J. & Kim, C.-K. p-Channel Tin Monoxide Thin Film Transistor Fabricated by Vacuum Thermal Evaporation. *Jpn. J. Appl. Phys.* **49** (2010).
21 Liang, L. Y. *et al.* The structural, optical and electrical properties of Y-doped SnO thin films and their p-type TFT application. *J. Phys. D: Appl. Phys.* **45**, 085101 (2012).
22 Ogo, Y. *et al.* p-channel thin-film transistor using p-type oxide semiconductor, SnO. *Appl. Phys. Lett.* **93**, 032113 (2008).
23 Yabuta, H. *et al.* Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits. *Appl. Phys. Lett.* **97**, 072111 (2010).
24 Batzill, M. & Diebold, U. The surface and materials science of tin oxide. *Prog. Surf. Sci.* **79**, 47-154 (2005).
25 Pan, X. Q. & Fu, L. Oxidation and phase transitions of epitaxial tin oxide thin films on (1-bar 012) sapphire. *J. Appl. Phys.* **89**, 6048-6055 (2001).
26 Geurts, J., Rau, S., Richter, W. & Schmitte, F. J. SnO films and their oxidation to SnO2: Raman scattering, IR reflectivity and X-ray diffraction studies. *Thin Solid Films* **121**, 217-225 (1984).
27 Birkholz, M. *Thin-film analysis by x-ray scattering.* 1-37, 200-265 (WILEY-VCH, 2006).
28 Ramadan, A. A. *et al.* Addressing difficulties in using XRD intensity for structural study of thin films. *Crys. Res. Technol.* **44**, 111-116 (2009).
29 Delhez, R., Keijser, T. H. & Mittemeijer, E. J. Determination of crystallite size and lattice distortions through X-ray diffraction line profile analysis. *Fresenius Z. Anal. Chem.* **312**, 1-16 (1982).
30 Togo, A., Oba, F., Tanaka, I. & Tatsumi, K. First-principles calculations of native defects in tin monoxide. *Phys. Rev. B* **74**, 195128 (2006).
31 Watson, G. W. The origin of the electron distribution in SnO. *J. Chem. Phys.* **114**, 758-763 (2001).
32 Ogo, Y. *et al.* Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application. *Phys. Status Solidi A* **206**, 2187-2191 (2009).
33 Granato, D. B., Caraveo-Frescas, J. A., Alshareef, H. N. & Schwingenschlögl, U. Enhancement of p-type mobility in tin moxide by native defects. *Applied Physics Letters* **102**, 212105 (2013).
34 Kawazoe, H. *et al.* P-type electrical conduction in transparent thin films of CuAlO2. *Nature* **389**, 939-942 (1997).
35 Yanagi, H., Kawazoe, H., Kudo, A., Yasukawa, M. & Hosono, H. Chemical Design and Thin Film Preparation of p-Type Conductive Transparent Oxides. *J. Electroceram.* **4**, 407-414 (2000).
36 Wager, J. F. Transfer-curve assessment of oxide thin-film transistors. *Journal of the Society for Information Display* **18**, 749-752 (2010).
37 Lee, C.-G. & Dodabalapur, A. Solution-processed zinc-tin oxide thin-film transistors with low interfacial trap density and improved performance. *Appl. Phys. Lett.* **96**, 243501 (2010).
38 Azoulay, A., Shamir, N., Fromm, E. & Mintz, M. H. The initial interactions of oxygen with polycrystalline titanium surfaces. *Surface Science* **370**, 1-16 (1997).

39 Barquinha, P. *et al.* Influence of the semicondcutor thickness on the electrical properties of transparent TFTs based on indium zinc oxide. *Journal of Non-Crystalline Solids* **352**, 1749-1752 (2006).
40 Robertson, J. High dielectric constant oxides. *The European Physical Journal Applied Physics* **28**, 265-291 (2004).
41 Houssa, M. *High k Gate Dielectrics*. (Taylor & Francis, 2003).
42 Blöchl, P. E. Projector augmented-wave method. *Phys. Rev. B* **50**, 17953-17979 (1994).
43 Kresse, G. & Hafner, J. Ab initio molecular-dynamics simulation of the liquid-metal-amorphous-semiconductor transition in germanium. *Phys. Rev. B* **49**, 14251-14269 (1994).
44 Kresse, G. & Furthmüller, J. Efficient iterative schemes for ab-initio total energy calculations using a plane-wave basis set. *Phys. Rev. B* **54**, 11169-11186 (1996).
45 Perdew, J. P., Burke, K. & Ernzerhof, M. Generalized Gradient Approximation Made Simple. *Phys. Rev. Lett.* **77**, 3865-3868 (1996).
46 Monkhorst, H. J. & Pack, J. D. Special points for Brillouin-zone integrations. *Phys. Rev. B* **13**, 5188-5192 (1976).

A summary of the electrical characterization of SnO thin films and TFTs can be found in

Caraveo-Frescas, J. A.; Nayak, P. K.; Al-Jawhari, H. A.; Granato, D. B.; Schwingenschlögl, U.; Alshareef, H. N., Record Mobility in Transparent p-Type Tin Monoxide Films and Devices by Phase Engineering. *ACS Nano* **7**, 5160-5167 (2013)

Density Functional Theory simulations are further discussed in

Granato, D. B., Caraveo-Frescas, J. A., Alshareef, H. N. & Schwingenschlögl, U. Enhancement of p-type mobility in tin moxide by native defects. *Applied Physics Letters* **102**, 212105 (2013)

Chapter 5

SnO Nanowire Field Effect Transistors

In this chapter we report the fabrication of transparent p-type tin monoxide (SnO) nanowire field-effect transistors (NW-FETs). The nanowire devices show very stable and well-behaved enhancement mode p-type behavior, with record performance at low process temperature (160°C). The SnO nanowire FETs exhibit the highest reported field-effect hole mobility ($10.83 cm^2V^{-1}s^{-1}$) of any p-type oxide semiconductor processed at such low temperature. Compared to thin film transistors (TFTs) using the same SnO film, the NW-FETs exhibit five times higher mobility, and one order of magnitude lower subthreshold slope, clearly demonstrating the effectiveness of device nanoscaling. In addition, the SnO nanowire FETs show exceptionally low threshold voltages (~ -1 Volt), which is three times lower than the best reported SnO TFT devices, and fifteen times smaller than the only other reported p-type oxide nanowire transistors (based on Cu_2O). Besides quantum confinement effects, which are known to increase mobility in 1-D nanostructures,[1,2] gate dielectric choice and process temperature are shown to be critical parameters for achieving this record performance.

5.1 Introduction

Among field-effect transistors (FET), thin-film transistors (TFTs), which employ a thin film layer of a semiconducting material as the active layer, have been used for decades as a crucial component in commercial displays.[3-6] Polycrystalline silicon (poly-Si) and

amorphous silicon (a-Si) are widely used materials to fabricate the switching/driving TFTs for active matrix organic light emitting diode displays (AMOLED) and liquid-crystal displays (LCD) respectively.[2-4] Nevertheless, there are intrinsic properties like their lack of transparency, rigidity, low mobility (~1 $cm^2V^{-1}s^{-1}$ for a-Si), or high processing temperature (poly-Si), that rules them out as alternatives for future display technologies, especially for the emerging transparent and flexible electronics.[7, 8] Great efforts have been exerted recently in transparent transistor research to find semiconducting materials that can replace a-Si in backplane TFTs. With transparent TFTs being the fundamental building blocks of potential transparent electronics,[9, 10] the suitable candidate(s) must have good optical transparency (>90% in the visible range); high material stability; excellent device performance (high carrier mobility, high on-to-off current ratio, moderate carrier density, low threshold voltage, low sub-threshold slope); and compatibility with existing TFT fabrication technologies.

Semiconducting metal oxides stand out as the most promising candidates for future display technologies and emerging transparent electronics owing to their wide optical band gap (E_g), chemical and mechanical stability, low temperature processing and excellent device performance. Fully transparent and flexible TFTs with excellent device performance have been reported for different metal oxide semiconducting films.[8, 9, 11-13] Furthermore, nanowire (NW) field-effect transistors based on n-type oxides such as ZnO, SnO_2, In_2O_3 or other binary and ternary oxides have been also demonstrated to show even higher field-effect mobility (μ_{FE}) to that of poly-Si (150 $cm^2V^{-1}s^{-1}$) [2, 10, 14-17] preserving the high optical transparency and material stability. The high mobility values reported for nanowire field effect transistors of different materials have been attributed to confinement-induced effects. Even though the exact mechanisms that produce higher mobility in nanowire FETs are not

completely clear, Trivedi *et al.* have shown how increased quantum confinement results in high mobility p-Si nanobelts and nanowire transistors.[1] They have attributed their higher mobility values to a lower hole effective mass dispersion as the channel shrinks in dimension, *i.e.* holes with closer values of effective mass form the channel. Ju *et al.* have also suggested that a reduction in low-angle carrier scattering by the use of quasi-one dimensional structures might be an important mechanism for mobility enhancement.[2]

Among the promising p-type candidates are cuprous oxide (Cu_2O) and stannous oxide (SnO), which have been demonstrated as p-type active channel materials in TFTs fabricated by several methods[18-26] with the physical vapor deposited films exhibiting the best performance.[19] The PbO-type layered structure tin monoxide is now well known to be a transparent p-type semiconductor[27] with an indirect E_g ~ 2.7 to 2.9 eV.[25, 26, 28] Its intrinsic p-type character originates from the Sn^{2+} vacancy and with relatively high hole mobility attributed to the hybridized Sn *5s* and O *2p* orbitals near the valence band maxima.[27, 28] The best reported mobility for TFTs fabricated with pure SnO is 1.3 $cm^2V^{-1}s^{-1}$,[25] but it has recently been demonstrated that excess Sn metal in the SnO films can increase the mobility to above 6.0 $cm^2V^{-1}s^{-1}$.[29]

Liao *et al.* have demonstrated p-type behavior in CuO and poly crystalline Cu_2O single NW-FETs grown by thermal oxidation of copper foils at 500 ^oC (for CuO)[30] and further reduction in hydrogen gas for Cu_2O conversion.[31] Their devices exhibited field-effect mobility around 5 and 95 $cm^2V^{-1}s^{-1}$, respectively. Despite the impressive μ_{FE} of polycrystalline Cu_2O NW-FET, its high threshold voltage (V_T) ~15V, low E_g=2.17 eV, high processing temperature make it less attractive for future applications. In contrast, the

fabrication of field-effect functional devices using SnO nanoscale structures has not been yet demonstrated, even though synthesis of SnO structures like nanosheets[32], nanobelts[33], and nano-rectangle strips[34] have been reported.

5.2 Results and Discussion

Here we demonstrate for the first time the fabrication of transparent SnO nanowire field-effect transistors with stable and well-behaved enhancement-mode p-type behavior, and a maximum linear μ_{FE}=10.83 $cm^2V^{-1}s^{-1}$, V_T ~ -1V, I_{ON}/I_{OFF} ratio >10^3 at a record low temperature for active channel crystallization of 160 °C.

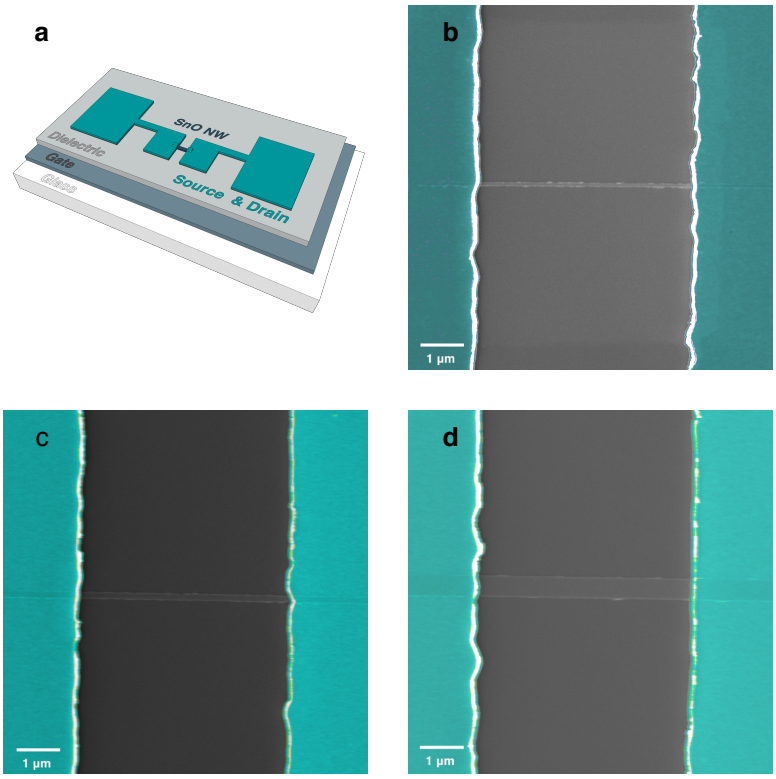

Figure 5.1.Conceptual design and SEM images. a, Conceptual design of the fabricated devices (150 nm ITO gate electrode/220 nm HfO_2/ATO gate dielectric/ EBL-patterned SnO nanowire channel/8 nm Ti, 80 nm Au source and drain electrodes); Top view scanning electron microscopy image of fabricated device with channel length of 5 µm and channel width defined by the nanowire planar width of **b,**100 nm; **c,** 200 nm; and **d,** 500 nm.

The single NW back-gate FET structure is depicted in Figure 5.1a. Indium tin oxide (ITO)-coated glass is used as transparent substrate, while the ITO layer is used as a global gate. Atomic layer deposition (ALD)-derived high-k HfO_2 and ATO (a stacked multilayer of Al_2O_3 and TiO_2) are used as gate dielectrics. Electron beam lithography (EBL)-patterned SnO NW are used as a p-type semiconducting active and the stack is completed by Ti/Au source and drain (S&D) electrodes. The SnO films used as starting point for nanowire formation were deposited under previously optimized process conditions (Chapter 4) that included deposition pressure (*P*) of 1.8 mTorr and relative oxygen partial pressure (O_{PP}) of 13% where single phase SnO occurs.[29] The whole stack followed a post-annealing treatment in a tube furnace in air, in order to crystallize the SnO NWs as well as to improve the S&D contact to SnO. Top view scanning electron microscopy (SEM) images of a NW-FETs are shown in Figure 5.1b-d of a device with an effective channel length (L) of 5 μm and channel width (W) defined by the planar NW width of 100 nm, 200nm and 500 nm, respectively. The as-deposited films are amorphous, but do crystalize after a post-annealing treatment in air, in a tube furnace at temperatures as low as 160 ^{o}C. Figure 5.2a shows X-ray diffraction (XRD) patterns of as-deposited amorphous and crystallized SnO films showing the presence of single-phase tetragonal SnO. The optimized tin monoxide layer is polycrystalline with a crystallite size ranging from 10 to 15 nm as extracted from transmission electron microscopy (TEM) analysis. The SnO films themselves are transparent with an average optical transmission of 92% in the visible region of the electromagnetic spectrum (400 nm-700 nm), as previously described in Chapter 4. Figure 5.2b shows a cross-sectional TEM image of the stack, showing the rectangular cross-sectional area of a 100 nm wide EBL-patterned structure. Figure 5.2c corresponds to a high-resolution TEM (HRTEM) image showing the polycrystalline nature of the nanowire. Figures 5.2d-e show the fast Fourier transformation

(FFT) analysis of the SnO grains observed in the HRTEM image showing the interplanar distance of 2.64 Å and 2.95 Å, consistent with the (110) and (101) lattices of the tetragonal SnO phase.

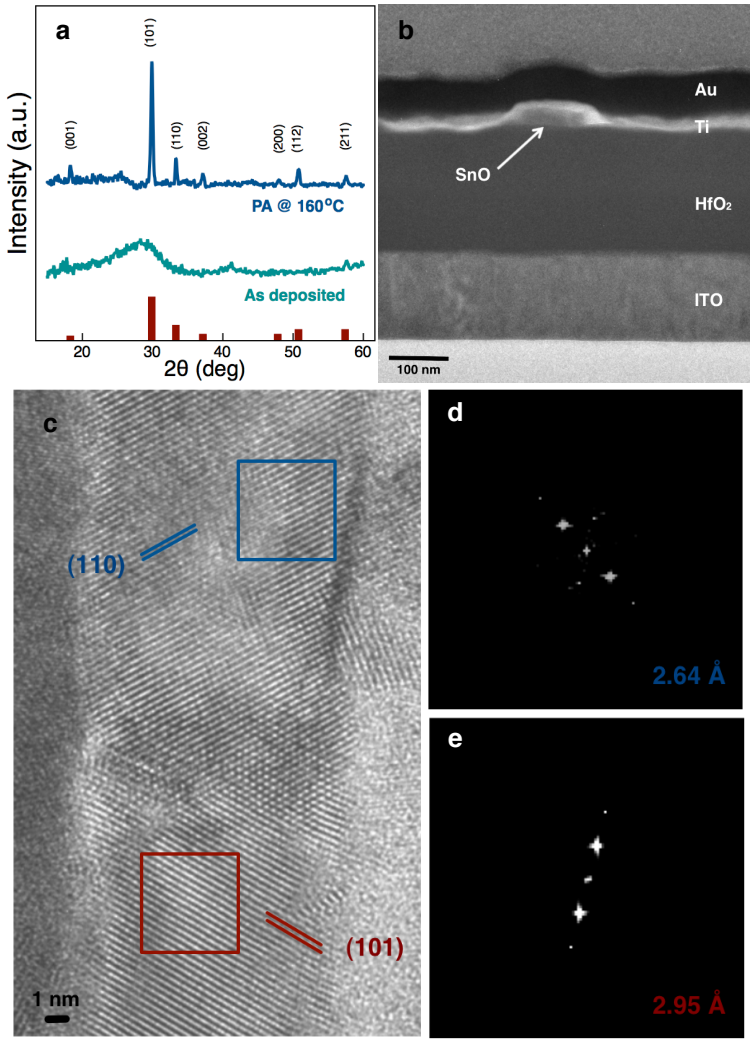

Figure 5.2 NW Characterization. a, X-ray diffraction patterns of amorphous as-deposited SnO films and crystalline SnO films after annealing in air at 160 °C. The diffraction pattern of tetragonal SnO (JCPDS card No. 06-0395) is shown by the red bars; **b,** Cross-sectional TEM image of the stack, showing the rectangular cross-sectional area of a 100 nm wide EBL-patterned structure; **c,** HRTEM image of the SnO nanowire, viewed vertically. FFT analysis of the grains observed in the HRTEM image showing the interplanar spacing of the **d,** (110) and **e,** (101) lattices of tetragonal phase SnO.

Figure 5.3 shows the characteristic transistor curves for the best performing devices, which correspond to FETs fabricated using HfO_2 as the gate dielectric and post-annealed at

160 °C. Figure 5.3a-5.3c shows the output characteristics of the 100 nm, 200 nm and 500 nm NW-FET, respectively. No current crowding at low drain-source voltage (V_{DS}) is observed, showing Ohmic contact with the Ti/Au source and drain contacts. The well-behaved output curves exhibit a clear pinch-off and current saturation for all the FETs when operating in the negative V_{DS} region. p-channel operation is confirmed by the transfer characteristics shown in Figure 5.3d, since drain-source current (I_{DS}) increased in all the tested devices when a negative gate-source voltage (V_{GS}) was applied at a fixed V_{DS}=-1V. Multiple dual-sweep I_{DS}-V_{GS} were obtained for several devices for each channel geometry and all curves show comparable behavior, with consistent on-off current ratio (I_{ON}/I_{OFF}), sub-threshold swing (SS), linear-region field-effect mobility (μ_{FE}) and threshold voltage (V_T) values.

Multiple dual-sweep characterization was performed following the recommendations by J. Wager[35] (described in section 3.4.3) and it was found that all the measured devices exhibit *non-equilibrium, steady state behavior*: dual-sweep log (I_{DS})-V_{GS} transfer characteristics show hysteresis and retraceable positive-going and negative-going behavior after multiple scans. I_{DS}-V_{GS} scans were performed at a V_{GS} scan rate of SR=1.09 $Vsec^{-1}$. I_{DS} increased for all FETs when a negative V_{GS} was applied, exhibiting enhancement-mode operation ($I_{DS}\approx 0$ at V_{GS}=0) as shown in the output characteristics of Figure 5.3. The off-current is $<4\times10^{-10}$ A for all devices, while the gate leakage is $<3\times10^{-10}$ A reflecting the good insulating properties of the HfO_2 gate dielectric. A maximum μ_{FE} of 10.83 $cm^2V^{-1}s^{-1}$, 10.58 $cm^2V^{-1}s^{-1}$ and 10.30 $cm^2V^{-1}s^{-1}$ for the 100 nm, 200 nm and 500 nm devices respectively, with $V_T \sim$ -1V, SS≈0.74 $Vdec^{-1}$ and effective hysteresis density of $N_{HYS} \approx 7.5\times10^{11}$ cm^{-2} was achieved for FETs annealed at 160 °C as extracted from the transfer characteristics displayed in Figure 5.3d.

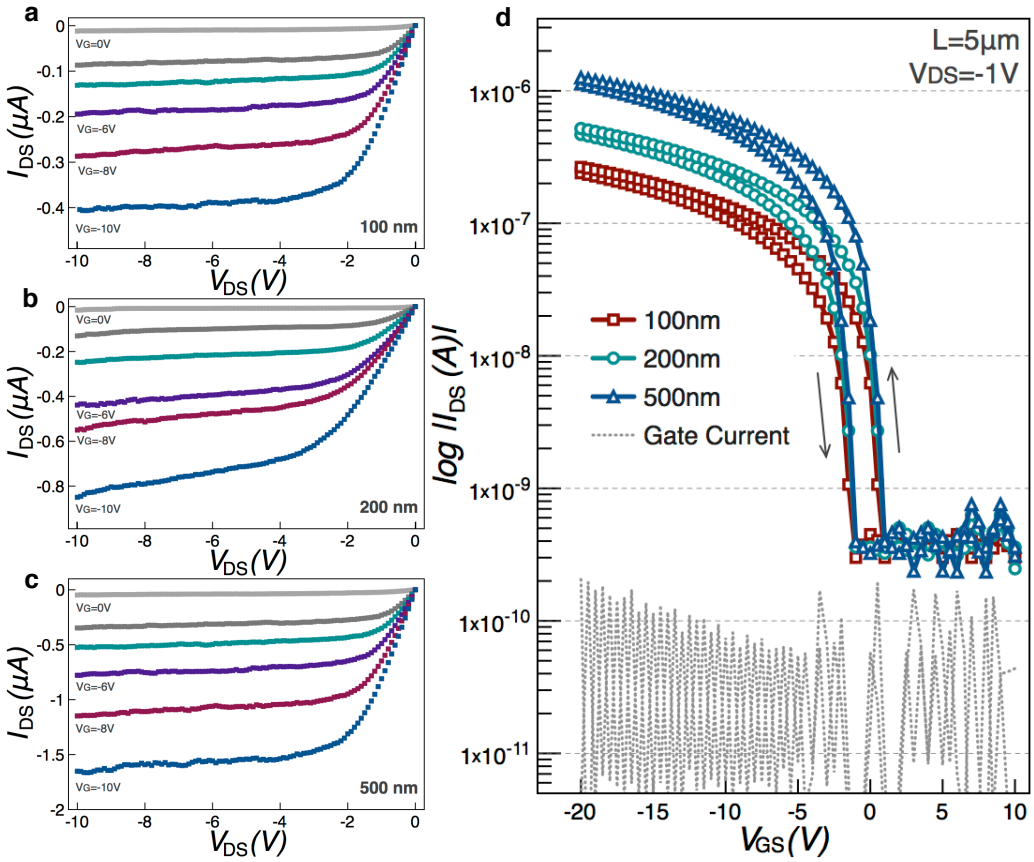

Figure 5.3. Output and transfer characteristics of devices annealed at 160 °C. Output characteristics of devices **a,** 100 nm; **b,** 200 nm; and **c,** 500 nm nanowire transistors (NW-FETs) respectively; **d,** Transfer characteristics of NW-FETs as a function of nanowire width when using HfO_2 as the gate dielectric.

The single phase SnO TFTs deposited at *P*=1.8 mTorr and 13% O_{PP} showed more inferior performance compared to the nanowire FET (μ_{FE} of 1.87 *vs* 10.83 $cm^2V^{-1}s^{-1}$), clearly demonstrating the effectiveness of nanoscaling. Table 5.1 shows the important device parameters comparing the NW FET and TFT devices fabricated with 15 nm thick of the same single-phase SnO film. It is clear from the data in Table 1 that the 1-D structure (nanowire) results in substantially improved device performance. The NW-FET has 5 times higher mobility, three time smaller threshold voltage, which is also closer to zero (-3.66 V for TFT to around -1 V for NW-FET), lower I_{OFF}, and lower density of interfacial trap states

(D_{it}) extracted from the SS. Furthermore, the NW devices show enhancement-mode operation in contrast to depletion-mode behavior of TFTs. It is important to highlight that the SS for the nanowire FET is one order of magnitude lower than the thin film device (7.65 V/dec for the TFT and 0.70 V/dec for the NW-FET), which gives a clear indication of the dramatic reduction in the density of interfacial trap states for nanoscale channel dimensions. The reduction in the I_{OFF} when compared to the TFTs indicates the reduction of the surface defects (*e.g.* additional oxygen), which is advantageous to maximize device performance. Our optimized post annealing temperature for the best TFT performance is 180 ^{o}C, but for the NW-FET, the best performance is observed at 160 ^{o}C. This small temperature difference is crucial to avoid additional oxygen incorporation into the film and hence we get a better mobility. TFTs annealed at 160 ^{o}C show very poor performance, most likely attributed to the incomplete crystallization of the SnO channel. The higher annealing temperature of TFTs allows additional oxygen to go into the exposed SnO surface contributing to an oxygen-rich surface and hence a higher off current. The smaller dimensions of the SnO nanowires allow their complete crystallization at lower temperature, which in turn reduces the likelihood of an oxygen-rich surface formation. The transfer characteristics of TFT and the 500 nm NW-FET are depicted in Figure 5.4a. In order to rule out narrow and short channel effects in the nanowire FETs, at least 10 devices of each NW width were tested showing consistent results. The data in Fig. 5.4a clearly demonstrate the advantages of our nanoscale nanowire devices over one of the best-reported performance for single-phase SnO TFT devices.

For consistency with the TFT devices described in Chapter 4, NW FET with Ti/ITO source and drain contacts were fabricated. The transfer characteristics of these devices are shown in Figure 5.4b for devices annealed at 160 ^{o}C. The use of ITO in the

source and drain electrodes negatively impacts the on current of the devices, decreasing the mobility down to 7.1 $cm^2V^{-1}s^{-1}$. The reason behind the degradation of the SnO mobility when using ITO requires further investigation, but a possible reason might be additional oxygen being supplied to the pure phase SnO making it an oxygen rich SnO phase instead. A similar behavior is observed when the post annealing temperature is increased and is discussed below.

	NW FET			TFT
	100 nm	200 nm	500 nm	W/L=50X50µm
μ_{FE} (cm^2/Vs)	10.83	10.58	10.30	1.87
V_T (V)	-1.06	-1.08	-1.20	-3.66
I_{OFF} (A)	4×10^{-10}	4×10^{-10}	4×10^{-10}	1×10^{-9}
ΔV_{ON} (V)	1.99	2.07	2.03	3.61
SS (V/dec)	0.76	0.69	0.60	7.65
D_{it} (#/eV cm^2)	4.45×10^{12}	4.00×10^{12}	3.43×10^{12}	4.82×10^{13}
N_{HYS} (#/cm^2)	7.42×10^{11}	7.72×10^{11}	7.57×10^{11}	1.35×10^{12}

Table 5.1. Performance comparison of NW-FET and TFT devices fabricated using the same single-phase SnO material.

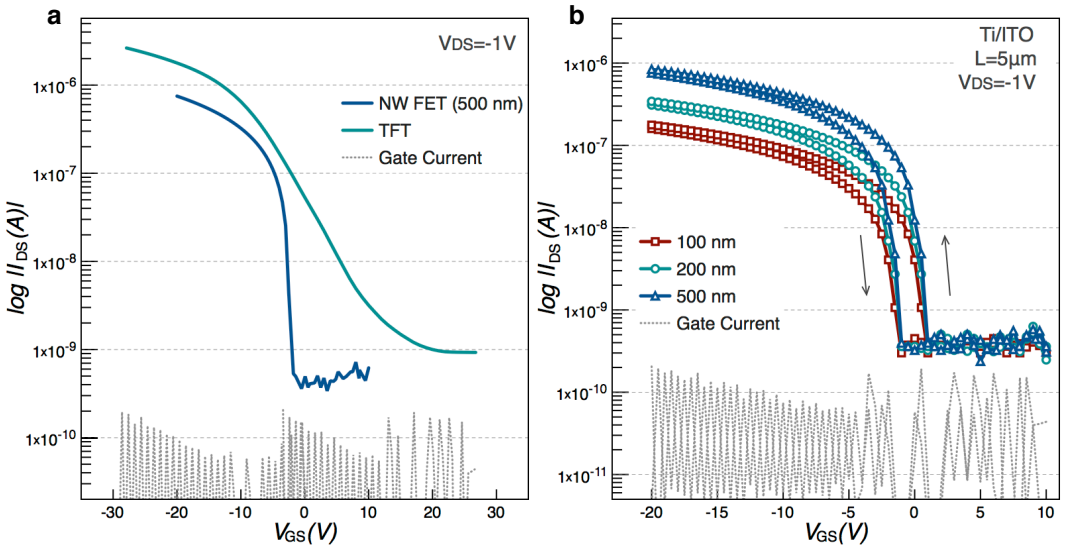

Figure 5.4. Transfer characteristics comparison. **a,** Thin film transistor versus nanowire FET (500 nm); **b,** Transfer characteristics of NW-FETs as a function of nanowire width when using HfO_2 as the gate dielectric, annealed at 160 °C using Ti/ITO source and drain contacts.

Figure 5.5 shows the response of the 100 nm width FETs at three different temperatures where p-type behavior is observed. Figure 5.5a shows weak gate response without hard saturation, which is attributed to the incomplete crystallization of the active layer at this temperature. Hard saturation is observed on well-behaved curves shown in Fig. 5.5b and 5.5c that correspond to devices annealed at 160 °C and 170 °C, respectively. Transfer characteristics of these devices are depicted in Figure 5.5d showing the best performance at 160 °C. The important FETs parameters are summarized in Figure 5.6 as a function of NW width and post-annealing temperature for devices fabricated using HfO_2 as gate dielectric. At 150 °C SnO is not completely crystallized so the devices show a rather modest μ_{FE} (Fig. 5.6a), positive V_T (Fig. 5.6b), large SS (Fig. 5.6c), and high N_{HYS} (Fig. 5.6d). The last two parameters reflect a high density of trap states in the SnO channel (SS) and the SnO/HfO_2 interface (N_{HYS}), which significantly reduces as the annealing temperature increases. At 160 °C and 170 °C, SS reduces from around 11 $Vdec^{-1}$ at 150 °C to an average of 0.74 $Vdec^{-1}$ (Fig 5.6c), showing that once the active layer is completely crystallized the SnO/HfO_2 interface is of relatively high quality. This statement is confirmed in Fig. 5.6d, where the N_{HYS} is nearly the same for all devices annealed at 160 °C and 170 °C. Nevertheless, the mobility and threshold voltage degrades at temperatures higher than 160 °C, as observed for devices annealed at 170 °C. The devices convert to weak n-type conduction when annealed at 180 °C and mainly attributed to the oxygen disproportionation mechanism[36] in which the incorporation of excess oxygen into SnO causes a transformation to an oxygen-deficient SnO_2 phase. In summary, at 150 °C the SnO NWs are not completely crystallized, at 160 °C they show the best p-type performance, at 170 °C they are affected by additional oxygen incorporation, and at 180 °C they exhibit weak n-type conduction as summarized in Figure 5.6e.

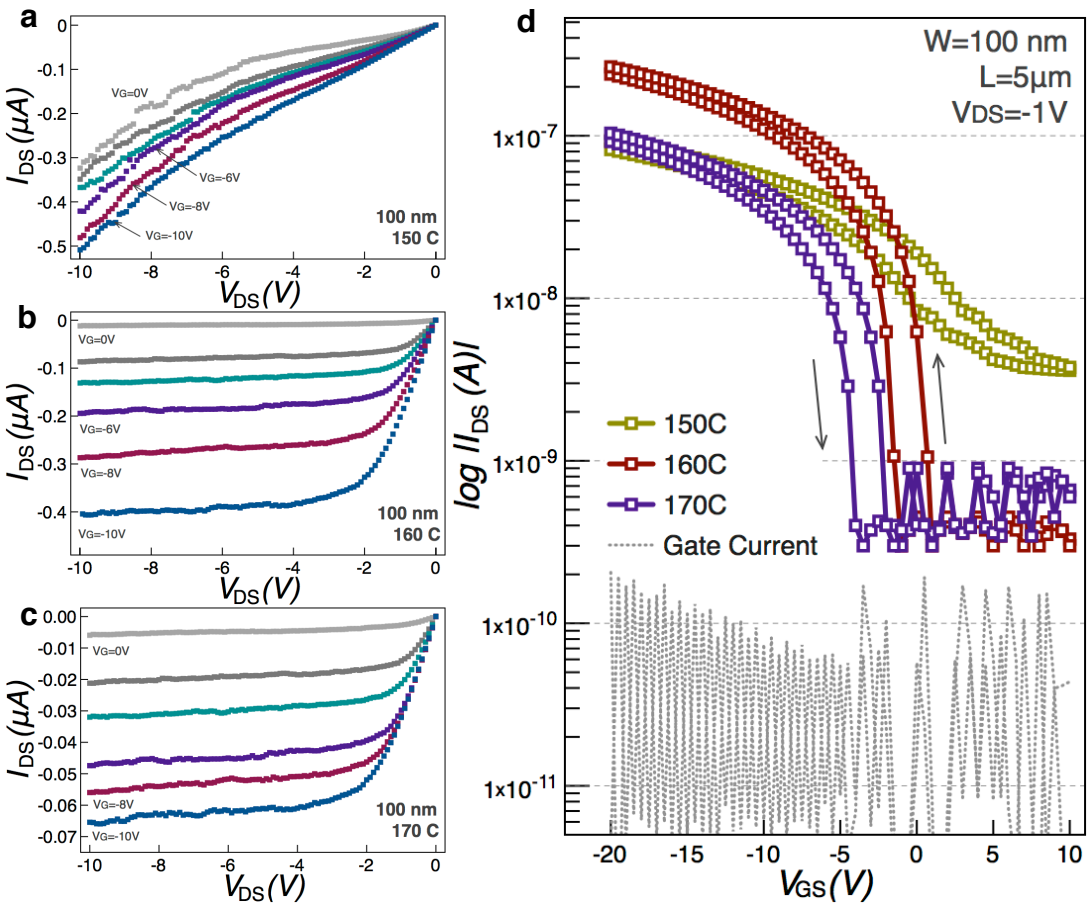

Figure 5.5. Output and transfer characteristics as a function of post annealing temperature. Output characteristics of the 100 nm NW-FETs annealed at **a,** 150 °C; **b,** 160 °C; **c,** 170 °C; **d,** Transfer characteristics of 100 nm width NW-FETs as a function of annealing temperature. The best performance is observed at an annealing temperature of 160 °C showing a field-effect mobility of 10.83 $cm^2V^{-1}s^{-1}$ when using HfO_2 as the gate dielectric.

Figure 5.7 compares the important FET parameters for devices fabricated at the best performance condition when using HfO_2 and ATO as gate dielectric. μ_{FE} on ATO is around half of the μ_{FE} on HfO_2, while there is no clear trend on V_T as shown in Fig. 5.7a. The I_{ON}/I_{OFF} ratio is in general one order of magnitude higher on HfO_2 (10^3) as shown in Fig. 5.7b. The gate leakage current of ATO is as high as 3×10^{-9} A, which significantly affects the device off current, thus reducing the I_{ON}/I_{OFF} ratio. Figure 5.7c shows the huge difference in the SS for both dielectrics, indicating a much better interface formation between the SnO

and HfO_2, which is also confirmed by the lower N_{HYS} (Fig. 5.7d) extracted from devices fabricated on HfO_2. Despite the fact that these two high-k oxides have comparable dielectric constant (and similar C_{ox} was used), the low V_T, SS and N_{HYS} of devices fabricated on HfO_2 compared to the higher variability of V_T as a function of NW width, higher SS, N_{HYS} and gate leakage current of devices on ATO shows that SnO/HfO_2 interface is more suitable for maximizing device performance. The relatively poorer performance on ATO seems to arise from the higher density of trap states at the SnO/ATO interface as well as from the degradation of ATO during the fabrication process caused mainly by e-beam exposure during the active patterning.

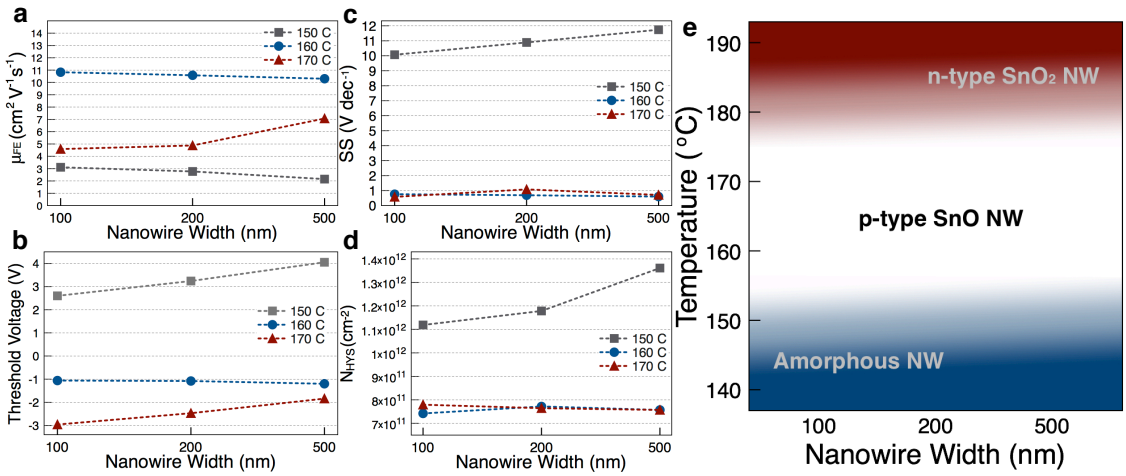

Figure 5.6. Important NW-FET parameters measured as a function of nanowire width and anneal temperature. a, field-effect mobility (μ_{FE}); **b,** threshold voltage (V_T); **c,** subthreshold swing (SS); **c,** effective hysteresis density (N_{HYS}). All devices shown here were fabricated using HfO_2 gate dielectric. **e,** Process map depicting process conditions where p-type conduction is observed in SnO NW FETs.

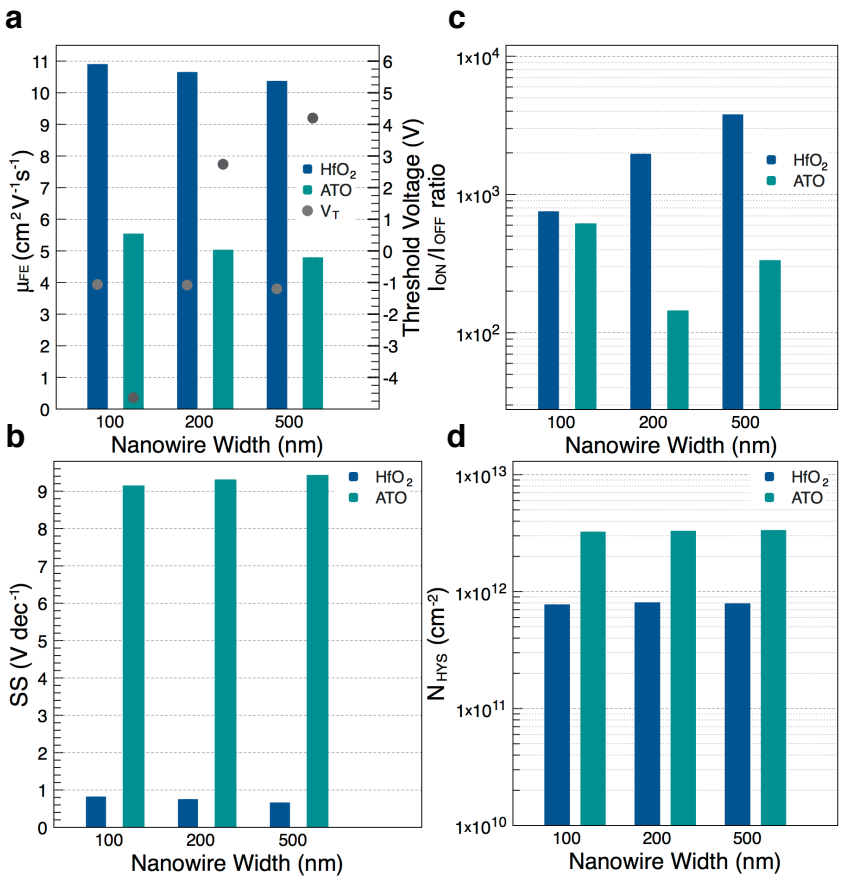

Figure 5.7. Effect of gate dielectric material on the performance of NW-FETs fabricated at the optimum anneal temperature (160 °C). a, field-effect mobility (μ_{FE}) and threshold voltage (V_T); **b,** subthreshold swing (SS); **c,** on-to-off current ratio (I_{ON}/I_{OFF}); **d,** effective hysteresis density (N_{HYS}).

5.3 Conclusions

We have demonstrated for the first time the fabrication of transparent p-type SnO nanowire field-effect transistors (NW-FETs) with unprecedented performance at low process temperatures (160°C). The SnO NW-FETs exhibit the highest reported field-effect hole mobility (10.83$cm^2V^{-1}s^{-1}$) of any p-type oxide semiconductor processed at such low temperature. Compared to thin film transistors (TFTs) using the same SnO film, the NW-FETs exhibit five times higher mobility and one order magnitude lower subthreshold slope. In addition, the SnO nanowire FETs show exceptionally low threshold voltages (~ -1 Volt),

which is nearly three times smaller than the thin film device. We have also shown that the use of HfO_2 as gate dielectric increases SnO nanowire device mobility due to a better dielectric/semiconductor interface with reduced trap states.

5.4 Methods

5.4.1 Device Fabrication

Indium tin oxide (ITO)-coated glass is used as transparent substrate, while the ITO layer is used as a global gate. The high-k HfO_2 (220 nm) gate dielectric was deposited by atomic layer deposition at 200 °C in a Cambridge Nanotech system while the ITO/ATO (a stacked multilayer of Al_2O_3 and TiO_2) substrates were obtained from Planar Systems, I. E., Finland. A 70 nm single layer of 950 K molecular weight polymethyl-methacrylate (PMMA A2) organic resist was spin coated onto a ITO/dielectric coated 1"×1" glass followed by a soft bake processing at 180 °C for 90 s to bake out the casting solvent. Electron beam lithography (EBL) was performed in a CRESTEC CABL-9520C high-resolution EBL system. The adjustment of the focus was primarily done by the observation with secondary electrons of a mark in the resist at high magnification. Fine focusing and correction of astigmatism were performed on gold nanoparticles placed in the substrate holder at a magnification of 300 000. Rectangular shapes with a width of 100 nm, 200 nm and 500nm, and a length of 9 μm were exposed in a vector scan mode with an e-beam exposure dose of 0.84 μsec/dot and a field size setting of 1200 μm/60000 dots at a beam current of 500 pA (resist sensitivity of 80 μCcm^{-2}). 1:1 methyl isobutyl ketone: isopropanol (MIBK:IPA) was used as developer. A 15 nm thick layer of single phase SnO was deposited at room temperature on the PMMA coated substrate by reactive DC magnetron sputtering. SnO

films were deposited from a 2" metal Tin target (99.99% purity) at an oxygen partial pressure (P_{O2}) of 3.12×10^{-2} Pa in an mixture of oxygen and argon gasses and a DC constant power of 30 watts achieving a deposition rate of 0.8 $Å s^{-1}$. After a conventional lift-off technique, well-defined SnO nanowire-like structures were obtained. In order to complete the stack, 8nm Ti/ 80nm Au source and drain (S&D) electrodes were e-beam evaporated and patterned by conventional photolithography and lift-off techniques. The single post-annealing treatment (150 °C, 160 °C, 170 °C) was performed after source and drain fabrication, in a tube furnace in air, in order to crystallize the SnO NWs as well as to improve the S&D contact to SnO.

5.4.2 Device Characterization

Device dimensions were analyzed by a FEI Helios NanoLab 400S scanning electron microscope (SEM). Film thicknesses were measured using a Veeco Dektak 150 surface profilometer and confirmed by cross-sectional transmission electron microscopy (TEM) analysis performed with a FEI Titan ST. High-resolution TEM (HRTEM) and fast Fourier transformation (FFT) analysis were performed in order to confirm the presence of single phase SnO. High-resolution X-ray diffraction patterns were obtained at room temperature in air by a Bruker D8 Discover diffractometer using the CuKα_1 (1.5406 Å) radiation. The electrical properties of the devices were measured on a probe station in air using a Keithley 4200-SCS semiconductor parameter analyzer at room temperature in the dark. The performance of the NW FETs was evaluated on devices with a fixed channel length (L) of 5 μm, and channel width (W) determined by the planar nanowire width of 100 nm, 200 nm and 500 nm. Linear-region field-effect mobility (μ_{FE}), threshold voltage (V_T) and sub-threshold swing (SS) were evaluated with the conventional metal-oxide-semiconductor field effect transistor model described in equations (5.1) and (5.2).

$$I_{DS} = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \; for \; V_{DS} < V_{GS} - V_T \tag{5.1}$$

where C_{ox} is the capacitance per unit area of the gate insulator.

$$SS = \frac{dV_{GS}}{d(logI_{DS})} \tag{5.2}$$

μ_{FE} was calculated starting from equation 1 by transconductance, g_m, in the linear regime according to equation (5.3)

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \approx \frac{W\mu_{FE}C_{ox}}{L} V_{DS} \tag{5.3}$$

As the geometry of the patterned nanowire has a well-defined belt-like shape and the device structure is in a global back-gate configuration, the gate capacitor can be described as equation (5.4) using the well-known parallel plate model.[10]

$$C = \frac{\varepsilon_r \varepsilon_o}{t} A \tag{5.4}$$

where A is the gate capacitor area and t the dielectric thickness.

C_{ox} of the 220 nm thick HfO_2 was measured to be 60 nFcm^{-2} with no more than 3% variation in the frequency range from 1 kHz to 1 MHz and an extracted dielectric constant of ~14, while for the 220 nm thick ATO it was found to be 55 nFcm^{-2} with around 10% frequency variation and extracted dielectric constant of ~15. All devices were swept from negative gate voltage (V_{GS} (-)) to positive gate voltage (V_{GS} (+)) and back to V_{GS} (-) in order to evaluate the effective hysteresis density N_{HYS} defined in equation (5.5) and which is an indication of the trapped states at the semiconductor-dielectric interface.

$$N_{HYS} = \frac{\Delta V_{ON} C_{ox}}{q} \tag{5.5}$$

where ΔV_{ON} is the difference between the ON voltage (V_{ON}) of the V_{GS}(-)-V_{GS}(+) and V_{GS}(+)-V_{GS}(-) scans and q is the elementary charge.

5.5 References and Notes

1 Trivedi, K., Yuk, H., Floresca, H. C., Kim, M. J. & Hu, W. Quantum Confinement Induced Performance Enhancement in Sub-5-nm Lithographic Si Nanowire Transistors. *Nano Lett.* **11**, 1412-1417(2011).

2 Ju, S. *et al.* Fabrication of fully transparent nanowire transistors for transparent and flexible electronics. *Nat. Nano.* **2**, 378-384 (2007).

3 Madelung, O. e. *Technology and Applications of Amorphous Silicon*. (Springer, 2000).

4 Ucjikoga, S. Low-temperature polycrystalline silicon thin-film transistor technologies for system-onglass displays. *MRS Bull.* **27**, 881-886 (2002).

5 Mentley, D. E. State of flat-panel display technology and future trends. *Proc. IEEE* **90**, 453 - 459 (2002).

6 Brody, T. P. The thin film transistor—A late flowering bloom. *IEEE Trans. Electron Devices* **31**, 1614 - 1628 (1984).

7 Reuss, R. H. *et al.* Macroelectronics: Perspectives on Technology and Applications. *Proceedings of the IEEE* **93**, 1239-1256 (2005).

8 Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **24**, 2945-2986 (2012).

9 Nomura, K. *et al.* Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488-492 (2004).

10 Huang, H. *et al.* Metal oxide nanowire transistors. *J. Mater. Chem* **22**, 13428-13445 (2012).

11 Ginley, D. S., Hosono, H. & Paine, D. C. *Handbook of Transparent Conductors* (Springer, 2010).

12 Kim, B. *et al.* Highly Reliable Depletion-Mode a-IGZO TFT Gate Driver Circuits for High-Frequency Display Applications Under Light Illumination. *Electron Device Letters, IEEE* **33**, 528-530 (2012).

13 Kim, K. M. *et al.* Competitive device performance of low-temperature and all-solution-processed metal-oxide thin-film transistors. *Appl. Phys. Lett.* **99**, 242109 (2011).

14 Cha, S. N. *et al.* High performance ZnO nanowire field effect transistor using self-aligned nanogap gate electrodes. *Appl. Phys. Lett.* **89**, 263102 (2006).

15 Chen, P.-C. *et al.* High-Performance Single-Crystalline Arsenic-Doped Indium Oxide Nanowires for Transparent Thin-Film Transistors and Active Matrix Organic Light-Emitting Diode Displays. *ACS Nano* **3**, 3383-3390 (2009).

16 Shen, G., Xu, J., Wang, X., Huang, H. & Chen, D. Growth of Directly Transferable In2O3 Nanowire Mats for Transparent Thin-film Transistor Applications. *Adv. Mater.* **23**, 771-775 (2011).

17 Chen, D., Liu, Z., Liang, B., Wang, X. & Shen, G. Transparent metal oxide nanowire transistors. *Nanoscale* **4**, 3001-3012 (2012).

18 Yao, Z. Q. *et al.* Room temperature fabrication of p-channel Cu2O thin-film transistors on flexible polyethylene terephthalate substrates. *Appl. Phys. Lett.* **101**, 042114 (2012).

19 Zou, X. *et al.* Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-k HfON Gate Dielectric. *Electron Devic. Lett.* **31**, 827-829 (2010).

20 Matsuzaki, K. *et al.* Epitaxial growth of high mobility Cu[sub 2]O thin films and application to p-channel thin film transistor. *Appl. Phys. Lett.* **93**, 202107 (2008).
21 Fortunato, E. *et al.* Thin-film transistors based on p-type Cu2O thin films produced at room temperature. *Appl. Phys. Lett.* **96**, 192102 (2010).
22 Fortunato, E. *et al.* Transparent p-type SnOx thin film transistors produced by reactive rf magnetron sputtering followed by low temperature annealing. *Appl. Phys. Lett.* **97**, 052105 (2010).
23 Lee, H.-N., Kim, H.-J. & Kim, C.-K. p-Channel Tin Monoxide Thin Film Transistor Fabricated by Vacuum Thermal Evaporation. *Jpn. J. Appl. Phys.* **49**, 020202 (2010).
24 Liang, L. Y. *et al.* The structural, optical and electrical properties of Y-doped SnO thin films and their p-type TFT application. *J. Phys. D: Appl. Phys.* **45**, 085101 (2012).
25 Ogo, Y. *et al.* p-channel thin-film transistor using p-type oxide semiconductor, SnO. *Appl. Phys. Lett.* **93**, 032113 (2008).
26 Yabuta, H. *et al.* Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits. *Appl. Phys. Lett.* **97**, 072111 (2010).
27 Togo, A., Oba, F., Tanaka, I. & Tatsumi, K. First-principles calculations of native defects in tin monoxide. *Phys. Rev. B* **74**, 195128 (2006).
28 Ogo, Y. *et al.* Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application. *Phys. Status Solidi A* **206**, 2187-2191 (2009).
29 Caraveo-Frescas, J. A. *et al.* Record Mobility in Transparent p-Type Tin Monoxide Films and Devices by Phase Engineering. *ACS Nano* **7**, 5160-5167 (2013).
30 Liao, L. *et al.* Multifunctional CuO nanowire devices: p-type field effect transistors and CO gas sensors. *Nanotechnology* **20**, 085203 (2009).
31 Liao, L. *et al.* p-type electrical, photoconductive, and anomalous ferromagnetic properties of Cu2O nanowires. *Appl. Phys. Lett.* **94**, 113106 (2009).
32 Kumar, B. *et al.* General Route to Single-Crystalline SnO Nanosheets on Arbitrary Substrates. *J. Phys. Chem. C* **114**, 11050-11055 (2010).
33 Orlandi, M. O., Leite, E. R., Aguiar, R., Bettini, J. & Longo, E. Growth of SnO Nanobelts and Dendrites by a Self-Catalytic VLS Process. *J. Phys. Chem. B* **110**, 6621-6625 (2006).
34 Iqbal, M. Z. *et al.* Preparation, characterization and optical properties of tin monoxide micro-nano structure via hydrothermal synthesis. *Mater. Lett.* **68**, 409-412 (2012).
35 Wager, J. F. Transfer-curve assessment of oxide thin-film transistors. *J. Soc. Inf. Display* **18**, 749-752 (2010).
36 Geurts, J., Rau, S., Richter, W. & Schmitte, F. J. SnO films and their oxidation to SnO2: Raman scattering, IR reflectivity and X-ray diffraction studies. *Thin Solid Films* **121**, 217-225 (1984).

A summary of the electrical characterization of NW FETs can be found in

J. A. Caraveo-Frescas and H. N. Alshareef. Transparent p-type SnO Nanowires with Unprecedented Hole Mobility among Oxide Semiconductors. *Applied Physics Letters (accepted)*

Chapter 6

Hybrid Organic/Inorganic Ferroelectric Field Effect Transistor

In this chapter, we report for the first time a hybrid organic/inorganic ferroelectric transistor based on transparent p-type oxide semiconductor tin monoxide and using P(VDF-TrFE) as the gate dielectric. A record mobility of 3.3 $cm^2V^{-1}s^{-1}$, large memory window (~ 16 V), low subthreshold swing (~ −4 $Vdec^{-1}$) and excellent retention characteristics up to 5000 sec have been achieved on both rigid and flexible devices fabricated at low temperatures (200 °C). The mobility achieved in our devices is 10 times higher than previous reports on polymer-based p-type ferroelectric field effect transistors (FeFETs). The demonstration here of high performance hybrid memory using transparent p-type SnO at low temperatures opens the door for the development of CMOS-based non-volatile memory devices for the emerging transparent and flexible applications.

6.1 Introduction

Flexible electronics research has made tremendous progress during the past 15 years, specifically in the area of thin film transistors (TFTs), organic light emitting diodes (OLEDs) and sensors[1, 2]. An integral part of any flexible electronic circuits is a non-volatile memory component, preferably transparent, that can be used to store and retrieve information as required[3]. Traditional memory circuits based on silicon technology are difficult to integrate with flexible and transparent plastic substrates due to the required high-temperature processing and limited flexibility of silicon. These problems can be overcome by using polymer ferroelectric memories, which are attractive due to their transparency, non-volatility,

large spontaneous polarization, excellent chemical stability, and low processing temperature[3-5]. Among the organic ferroelectric materials, Poly(vinylidene fluoride) [P(VDF)] and its copolymer with trifluoroethylene [P(VDF-TrFE)] are the most widely used materials due to their large remnant polarization, low leakage, short switching time, superior chemical stability and low temperature processability[3, 6].

Ferroelectric capacitor memories make use of the hysteresis behavior by associating +Pr and –Pr states with Boolean 1 and 0 logic states. The problem with using ferroelectric capacitors is that they suffer from destructive read-out, as the voltage applied to read the information can erase it as well. Ferroelectric transistor (FeFETs) memories solve this problem as they provide resistive switching that can be sampled at low voltages without affecting the ferroelectric polarization. Historically, polymer FeFETs have suffered from poor performance due to inherent low carrier mobility, low on-to-off current ratios, poor data retention characteristics and high operating voltages.

Most of the scientific reports regarding organic ferroelectric field effect transistors use p-type pentacene as the semiconducting material[4, 7]. Several authors have demonstrated that device performance when combining pentacene with P(VDF-TrFE) is rather modest due to the high surface roughness of P(VDF-TrFE) films[5]. Reversing the layer order, i.e., depositing the P(VDF-TrFE) on top of the pentacene, even when thought to be beneficial to avoid interfacial roughness has not been demonstrated satisfactory. This interfacial roughness problem arises from the fact that organic solvents required for the deposition of P(VDF-TrFE) cause severe damage to the surface of pentacene. In consequence, the reported mobility values are quite low. So far, the highest mobility reported for pentacene

based FeFETs is about 0.1 $cm^2V^{-1}s^{-1}$ [8-10]. Similarly even upon using other p-type polymeric semiconductors like MEH-PPV[11], TIPS pentacene[12], and rr-P3HT[13] the mobility in FeFETs is usually << 1 $cm^2V^{-1}s^{-1}$, with a maximum mobility value of 0.36 $cm^2V^{-1}s^{-1}$ achieved when using TIPS pentacene as the channel material[12].

Recently the community has adopted organic–inorganic hybrid-type nonvolatile memory thin-film transistors using an oxide semiconductor as the active material and an organic ferroelectric gate insulator[3, 9, 14]. This hybrid organic/inorganic device structure is a promising approach for the fabrication of high performance memory devices that will be needed in the development of next generation transparent and flexible electronics. n-type oxide based TFTs have already been demonstrated useful to be used in the active matrix (AM) backplane of liquid-crystal displays (LCD) and organic light-emitting diode (OLED) displays[1]. TFTs having an oxide semiconductor channel show very attractive features like high field-effect mobility, excellent uniformity, robust device stability, excellent transparency and can be deposited at low temperatures on plastic substrates for flexible electronic applications[2, 15].

Thus it seems reasonable to try hybrid organic-inorganic approach using oxide semiconductors and ferroelectric polymers to fabricate high performance and low cost non-volatile memory. There have been a few studies reporting hybrid ferroelectric memory with much improved performance compared to their polymer counterparts[3]. Field effect mobility > 30 $cm^2V^{-1}s^{-1}$ has been achieved in both rigid and flexible devices using ZnO-based semiconductors[14, 16]. Nevertheless, all reports on oxide semiconductor/organic ferroelectrics exhibit unipolar n-type conduction. Complementary metal oxide semiconductor (CMOS)

logic is of paramount importance if good circuit performance is desired. The advantages of CMOS logic compared to unipolar logic are low power consumption and dissipation, higher operating frequencies, good noise margin, and robust operation. Thus the development of high performance memory with both n and p-type conduction is critical to fabrication of CMOS-based circuitry.

Stannous oxide (SnO) and cuprous oxide (Cu_2O) have been recently shown as promising transparent p-type oxide semiconductors by the fabrication of TFTs by different methods[17-25]. Fully transparent and flexible TFTs based on SnO processed at low temperatures (180 ^oC) have been already demonstrated exhibiting higher mobility than Cu_2O based TFTs[26]. The p-type character of SnO originates from the Sn^{2+} vacancies while its high hole mobility is attributed to the hybridized Sn *5s* and O *2p* orbitals near the valence band maxima[27, 28]. With an optical band gap, E_G, of ~ 2.7 to 2.9 eV[24-26, 28] (compared to E_G ~2.1 of Cu_2O)[19, 20] and demonstrated field effect mobility as high as 6.75 $cm^2V^{-1}s^{-1}$, SnO is advantageous to be used as p-type semiconductor in the emerging field of transparent electronics[26].

In this study we report high performance rigid and flexible non-volatile memory devices using transparent p-type SnO. Our hybrid non-volatile ferroelectric memory devices consists of p-type SnO as the oxide channel and P(VDF-TrFE) as the gate dielectric. To the best of our knowledge this is the first report of p-type oxide ferroelectric memory transistor. We have fabricated the memory devices at low temperatures (~200 ^oC) on both rigid and flexible substrates. Our devices show very high mobility (~ 3.3 $cm^2V^{-1}s^{-1}$), large memory window (~ 16 V), low SS (~ −4 $Vdec^{-1}$), low operating (after switching) voltages (~ -1 V)

and excellent retention characteristics up to 5000 sec. Our hybrid devices show mobility which is an order of magnitude (10 times) higher than previous reports on p-type FeFETs.

6.2 Results and Discussion

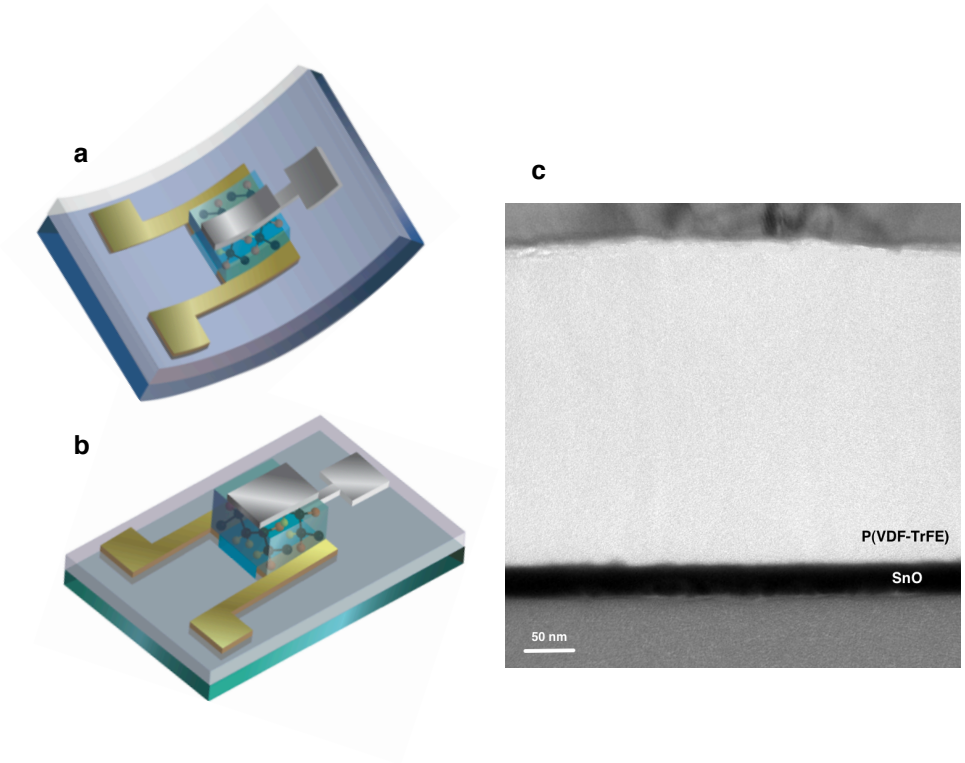

Figure 6.1. Conceptual design of the devices. a, polyimide substrate; **b,** glass substrate; **c,** TEM image of the SnO/P(VDF-TrFE) interface.

Figure 6.1a and 6.1b show the conceptual design of the top gate/top contact FeFETs on the flexible and rigid substrates, respectively. Bottom gate devices could not be fabricated, as the sputtering process and annealing process required for the oxide channel would be detrimental to the polymer ferroelectric dielectric. The active channel was a 30 nm thick layer of p-type SnO semiconductor deposited by sputtering which was then patterned by optical lithography. Next 10 nm Ti/40 nm Au thick source and drain electrodes were deposited as top contacts by thermal evaporation. After this 300 nm thick layer of

ferroelectric P(VDF-TrFE) was spin coated on top as the dielectric. Finally 80 nm thick aluminum metal was thermally evaporated and patterned to form the top gate of the memory transistor. The entire fabrication process was carried out at low temperatures of 200 ^{o}C, compatible with flexible substrates. Figure 1c shows a cross-sectional transmission electron microscopy (TEM) of the semiconductor/ferroelectric interface. P(VDF-TrFE) grows nicely on the flat surface of SnO without causing any damage to the oxide layer, and what is achieved by the use of dimethyl-formamide (DMF) as the P(VDF-TrFE) solvent instead of Methyl-Ethyl-Ketone (MEK) which damaged the SnO preventing the fabrication of working devices.

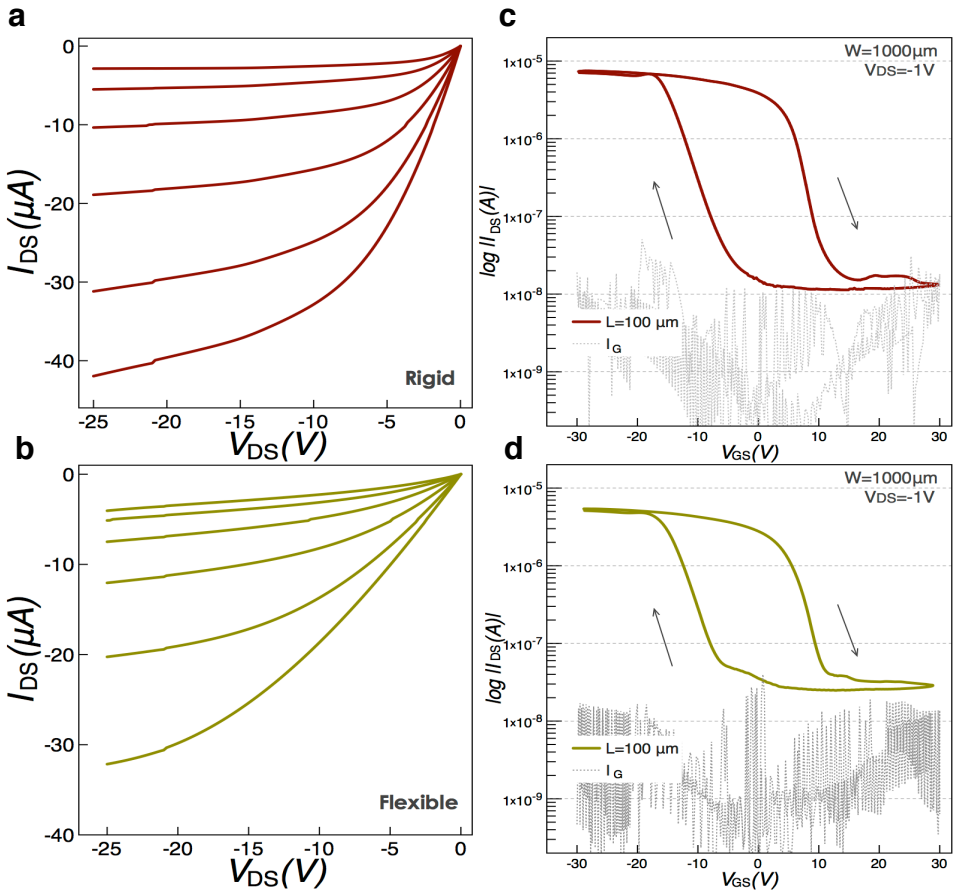

Figure 6.2. FeFET static characteristics. Output characteristics from V_{GS}=0 V to -15 V at -3V steps of **a,** glass substrate; **b,** polyimide substrate; Transfer characteristics at V_{DS}=-1V of **c,** rigid device; **d,** flexible device.

Figure 6.2 shows the static characteristics of the rigid and flexible devices with a width-to-length ratio (W/L) of 10 and a channel length, L=100 μm. Clear linear and saturation regions can be observed in the output characteristics shown in Fig. 6.2a and 6.2b for the rigid and flexible devices, respectively. Figures 6.2c and 6.2d show the transfer characteristics measured in the linear region at V_{DS}=-1V. The p-type conduction is observed for both devices since holes are generated when a negative gate voltage (V_{GS}) is applied. The arrows in the transfer characteristics show the clockwise hysteresis of the drain current (I_{DS}) originated from the ferroelectric nature of the P(VDF-TrFE) and not arising from the charge trapping mechanism[10]. Field effect mobility (μ_{FE}), calculated in the linear regime, of 3.3 $cm^2V^{-1}s^{-1}$ and 2.5 $cm^2V^{-1}s^{-1}$ were obtained for the rigid and flexible devices respectively, which to our knowledge, are the highest mobility values reported for any transparent p-type semiconductor and which are one order of magnitude higher than previously reported FeFETs based on p-type organic semiconductors[8-10]. On-to-off current ratio (I_{ON}/I_{OFF}) measured at V_{GS}=0 V was found to be around 10^2 and mainly limited by the relatively high gate current (I_G) of 10^{-8} A, seriously impacting the FeFETs off current. In the other hand, subthreshold swing (SS) of 4 V dec^{-1} is obtained, which is relatively lower to reported SnO TFTs using an oxide gate dielectric[21, 26]. A memory window, calculated from the shift in the on voltage (V_{ON}) of the negative-going scan (accumulation mode) and the positive-going scan (depletion mode) of 16 V is observed for FeFETs on both substrates.

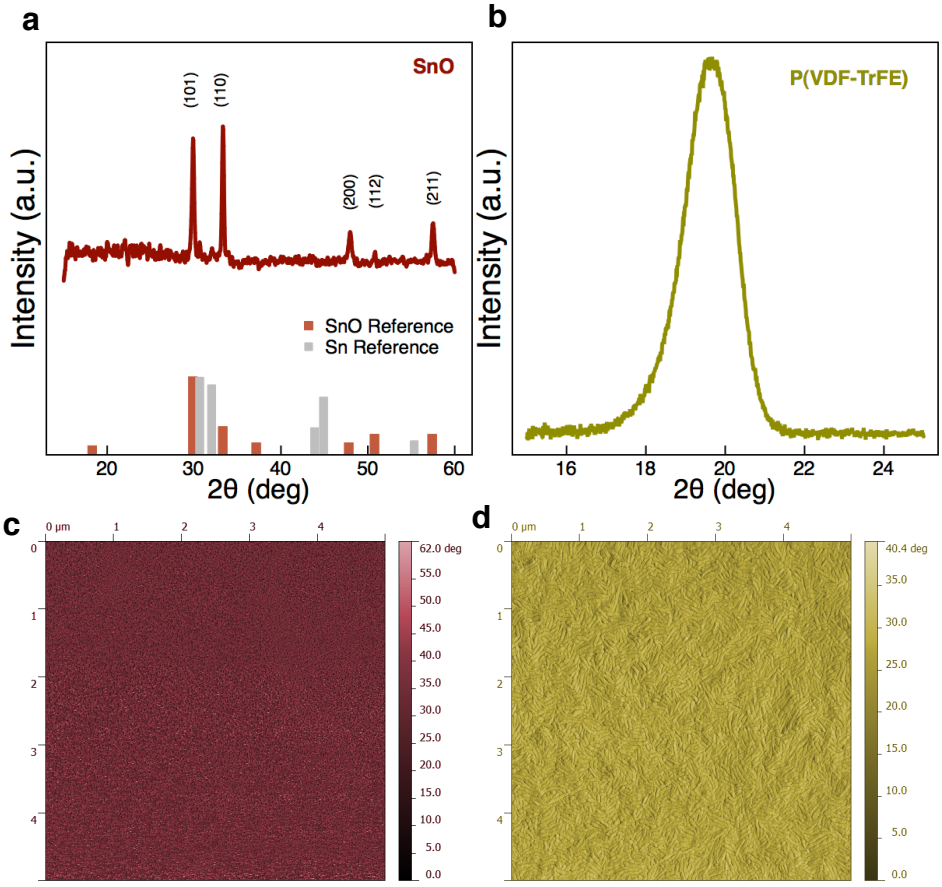

Figure 6.3. Materials characterization. a, XRD pattern of SnO thin films. The lines at the bottom show the diffraction patterns of tetragonal SnO (JCPDS card No. 06-0395) and tetragonal Sn (JCPDS card No. 04-0673); **b,** GIXRD pattern of P(VDF-TrFE) layer; **c,** AFM image of the SnO surface; **d,** AFM image of the P(VDF-TrFE) surface morphology.

Figure 6.3 shows the material characterization of both the SnO active layer as well as the ferroelectric P(VDF-TrFE) layer. Figure 6.3a shows the x-ray diffraction (XRD) pattern of SnO where mixed phase tin monoxide is shown. It has been previously demonstrated that the presence of metallic phase in a SnO matrix enhances mobility by promoting orbital delocalization in the valence band of SnO[26, 29]. We have used our previously optimized deposition conditions of SnO, where the highest mobility occurs, to fabricate the FeFETs devices. The deposition conditions where maximum mobility is observed were found to be

at a deposition pressure of 1.8 mTorr and relative oxygen partial pressure (O_{PP}) of 9%, where around 3 at% metallic tin is present[26]. The SnO film is polycrystalline with an extracted crystallite size of around 12 nm. The grazing incidence (GI) XRD pattern shown in Figure 6.3b shows the presence of the ferroelectric β phase of P(VDF-TrFE). The peak centered at $2\theta=19.7^{o}$ is consistent with the (100) and (200) planes yielding an inter planar distance of 4.5 Å consistent with earlier reports[30, 31]. Figure 6.3c and 6.3d show the 5μm × 5μm atomic force microscope (AFM) phase diagrams of SnO and P(VDF-TrFE) layers respectively, deposited in the rigid substrate. The SnO films show very smooth surfaces with a root mean square roughness of ~ 1.4 nm. It's very critical to have a smooth interface to achieve high performance devices. Previous report on bottom gate polymer FeFETs have reported poor mobility of the charge carriers due to the high surface roughness of P(VDF-TrFE) thin films[4, 5]. Inverting the stack by fabricating top gate devices can help but it's difficult to fabricate in all polymer structures. This is because the solvent used for spin coating P(VDF-TrFE) can be detrimental to a lot of organic semiconductors[5]. This can be solved using hybrid organic/inorganic structures for achieving high mobility in FeFETs[3]. P(VDF-TrFE) grows nicely on the relatively flat SnO surface (rms surface roughness ~ 6.18 nm) with an average grain size of ~ 160 nm, which can be clearly observed on the AFM image, consistent with earlier reports[32]. The large grains are important to get maximum polarization from the ferroelectric layer. Flexible devices show a higher surface roughness of ~ 9.77 nm mainly attributed to the higher substrate roughness of the polyimide when compared to glass. This difference in the surface roughness is of particular importance when comparing devices on both substrates, as it is known that large surface roughness degrades performance[4, 5, 8].

W=1000 μm	L (μm)		
Rigid Substrate	100	200	500
Mobility ($cm^2V^{-1}s^{-1}$)	**3.30**	**3.24**	**3.28**
Threshold Voltage (V)	-11.60	-11.61	-11.64
I_{ON}/I_{OFF}	2.51×10^2	2.40×10^2	2.62×10^2
SS ($Vdec^{-1}$)	4.29	4.33	4.35
Memory Window (V)	15.97	16.1	16.37

	L (μm)		
Flexible Substrate	100	200	500
Mobility ($cm^2V^{-1}s^{-1}$)	**2.53**	**2.48**	**2.51**
Threshold Voltage (V)	-11.74	-11.76	-11.72
I_{ON}/I_{OFF}	0.94×10^2	0.92×10^2	0.90×10^2
SS ($Vdec^{-1}$)	4.35	4.42	4.49
Memory Window (V)	16.26	14.21	14.64

Table 6.1. Important transistor parameters for devices fabricated on both rigid and flexible devices for three different W/L ratios.

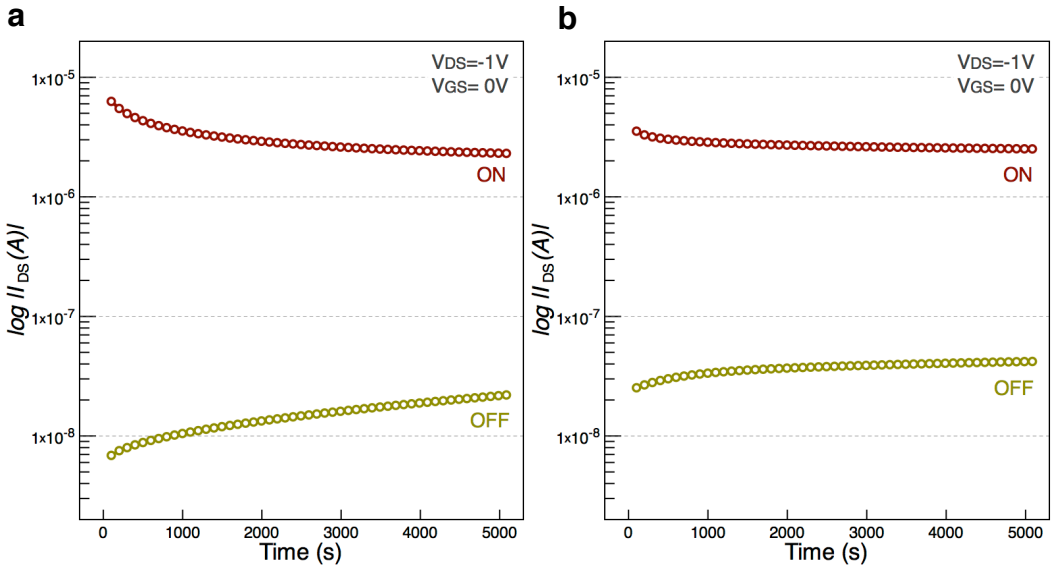

Figure 6.4. Retention characteristics. a, Rigid device; **b,** Flexible device. The ON/OFF states were produced at gate voltages of -30/+30 V with a 1 sec pulse and the retention was measured at zero gate bias condition.

Table 6.1 summarizes the important transistor parameters of devices with W/L ratios of 10, 5 and 2 in both the rigid and flexible devices. Comparable performance is

observed on the devices regardless of the channel dimensions. Furthermore, several measurements performed on each device, showing similar behavior prove their stability and reliability. Rigid devices exhibit higher mobility and I_{ON}/I_{OFF}. From the transfer characteristics on Figure 6.2, a higher I_G can be observed for the flexible devices, which in turn increases the device off current. Carrier scattering arising from higher surface roughness on the flexible devices seems to be the reason for the lower device performance when compared to the rigid ones. The higher surface roughness also makes the spin coating process of the ferroelectric layer less uniform giving rise to a higher probability of leakage paths due to a non-uniform electric field distribution on the dielectric as a result of the thickness differences. The use of an interfacial layer might be required to help decreasing the gate current, as it has been demonstrated when using n-type oxide semiconductors[33, 34]. From a memory point of view, data retention characteristics are of paramount importance. Figure 6.4 a and b shows the retention characteristics obtained by measuring the remnant I_{DS} as a function of time for rigid and flexible devices, respectively. The ON/OFF states were produced at gate voltages of -30/+30 V with a 1 sec pulse and the retention was measured at zero gate bias condition. Excellent retention characteristics are observed for these devices, as they keep an I_{ON}/I_{OFF} of around two orders of magnitude even after 5000 seconds.

6.3 Conclusions

We have demonstrated the first p-type oxide FeFET on both rigid and plastic substrates using the P(VDF-TrFE) as the ferroelectric material. The top gate devices exhibit a field effect mobility of 3.3 $cm^2V^{-1}s^{-1}$ and 2.5 $cm^2V^{-1}s^{-1}$ on the rigid and flexible substrates,

respectively. Furthermore a high memory window of 16 V has been achieved along with excellent retention characteristics of more than 5000 seconds. Further device engineering, such as semiconductor thickness optimization and the use of interfacial layer are required to enhance the device performance. The demonstration here of the first p-type oxide semiconductor/organic ferroelectric thin film transistor with superior device performance and low process temperature, opens the door for the development of CMOS-based non-volatile memory devices for the emerging transparent and flexible applications.

6.4 Methods

The top gate structure was fabricated in a rigid glass substrate and a flexible polyimide films. In order to decrease the surface roughness of the polyimide film a 200 nm thick Si_3N_4 layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The SnO active layer was deposited by DC reactive magnetron sputtering from a 2" metal target, at room temperature, at a deposition pressure of 1.8 mTorr, relative oxygen partial pressure of 9%, and power density of 9.55 W/in^2. Source and drain electrodes (10nm Ti, 40 nm Au) were electron-beam evaporated. The stack was annealed at 200 ^oC after source and drain deposition in order to crystallize the SnO active layer. P(VDF-TrFE) copolymer (70-30 mol %) powder was dissolved in Dimethyl Formamide (DMF) to get a 4 wt.% solution. The filtered solution was then spun on the PEDOT:PSS film at 4000 rpm for 60 s followed by a soft bake for 30 min at 80 ^oC. The films were then annealed in vacuum at 130 ^oC for 2 h to improve the crystallinity. The resulting P(VDF-TrFE) film thickness was approx. ~300 nm. Aluminum top gate electrodes were thermally evaporated to complete the stack. Layers of the device were patterned by conventional photolithography technique and lift-off process.

In order to prevent damage to the ferroelectric layer, methanol was used for lift-off. Devices were measures on a probe station at ambient conditions, in the dark, using a Keithley 4200 semiconductor parameter analyzer. The performance of the FeTFTs was evaluated from devices with width-to-length (W/L) ratios ranging from 2 to 10 at a fixed width W=1000 μm. Field-effect mobility (μ_{FE}) was extracted using the conventional metal-oxide-semiconductor field effect transistor model described in section 3.4. The capacitance density of the ferroelectric layer was measured by the well-known parallel plate capacitor method using Ti/Au as the bottom electrode and Al as top electrode for consistency, yielding a C_{ox}=40 nF cm^{-2} at a frequency of 100 Hz. The on-to-off current ratio was calculated at V_{GS}=0 V and the memory window as the difference in the on voltage of the positive-going and negative-going scans. Thicknesses of the different layers were obtained using surface profilometer (Veeco Dektak 150) and confirmed by cross-sectional TEM analysis (FEI Titan ST). High-resolution X-ray diffraction analysis was performed following the procedure described in section 3.2.1.

6.5 References and Notes

1 Ginley, D. S., Hosono, H. & Paine, D. C. *Handbook of Transparent Conductors* (Springer, 2010).

2 Fortunato, E., Barquinha, P. & Martins, R. Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances. *Adv. Mater.* **24**, 2945-2986 (2012).

3 Yoon, S.-M. *et al.* Nonvolatile memory thin-film transistors using an organic ferroelectric gate insulator and an oxide semiconducting channel. *Semicond. Sci. Technol.* **26**, 034007+034025 (2011).

4 Park, Y. J., Bae, I.-S., Kang, S. J., Chang, J. & Park, C. Control of Thin Ferroelectric Polymer Films for Non-volatile Memory Applications. *IEEE. T. Dielect. El. In.* **17**, 1135-1163 (2010).

5 Naber, R. C. G., Asadi, K., Blom, P. W. M., Leeuw, D. M. d. & Boer, B. d. Organic Nonvolatile Memory Devices Based on Ferroelectricity. *Adv. Mater.* **22**, 933-945 (2010).

6 Ling, Q.-D. *et al.* Polymer electronic memories: Materials, devices and mechanisms. *Prog. Polym. Sci.* **33**, 917-978 (2008).

7 Naber, R. C. G., Asadi, K., Blom, P. W. M., Leeuw, D. M. d. & Boer, B. d. Organic Nonvolatile Memory Devices Based on Ferroelectricity. *Adv. Mater.* **22**, 933-945 (2010).

8 Khan, M. A., Bhansali, U. S. & Alshareef, H. N. High-Performance Non-Volatile Organic Ferroelectric Memory on Banknotes. *Adv. Mater.* **24**, 2165-2170 (2012).

9 Lee, K. H. *et al.* High-Mobility Nonvolatile Memory Thin-Film Transistors with a Ferroelectric Polymer Interfacing ZnO and Pentacene Channels. *Adv. Mater.* **21**, 4287-4291 (2009).

10 Nguyen, C. A., Mhaisalkar, S. G., Ma, J. & Lee, P. S. Enhanced organic ferroelectric field effect transistor characteristics with strained poly(vinylidene fluoride-trifluoroethylene) dielectric. *Org. Electron.* **9**, 1087-1092 (2008).

11 Naber, R. C. G. *et al.* High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Mater.* **4**, 243-248 (2005).

12 Kang, S. J. *et al.* Non-volatile Ferroelectric Poly(vinylidene fluoride-co-trifluoroethylene) Memory Based on a Single-Crystalline Tri-isopropylsilylethynyl Pentacene Field-Effect Transistor. *Adv. Mater.* **19**, 1609-1616 (2009).

13 Naber, R. C., Boer, B. d., Blom, P. W. & Leeuw, D. M. d. Low-voltage polymer field-effect transistors for nonvolatile memories. *Appl. Phys. Lett.* **87**, 2035509 (2005).

14 Yoon, S.-M. *et al.* Fully Transparent Non-volatile Memory Thin-Film Transistors Using an Organic Ferroelectric and Oxide Semiconductor Below 200 oC. *Adv. Funct. Mater.* **20**, 921-926 (2010).

15 Wong, W. S. & Salleo, A. (Springer, 2009).

16 Yoon, S.-M., Yang, S. & Park, S.-H. K. Flexible Nonvolatile Memory Thin-Film Transistor Using Ferroelectric Copolymer Gate Insulator and Oxide Semiconducting Channel. *J. Electrochem. Soc.* **158**, H892-H896 (2011).

17 Yao, Z. Q. *et al.* Room temperature fabrication of p-channel Cu2O thin-film transistors on flexible polyethylene terephthalate substrates. *Appl. Phys. Lett.* **101**, 042114 (2012).

18 Zou, X. *et al.* Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-k HfON Gate Dielectric. *Electron Devic. Lett.* **31**, 827-829 (2010).

19 Matsuzaki, K. *et al.* Epitaxial growth of high mobility Cu[sub 2]O thin films and application to p-channel thin film transistor. *Appl. Phys. Lett.* **93**, 202107 (2008).

20 Fortunato, E. *et al.* Thin-film transistors based on p-type Cu2O thin films produced at room temperature. *Appl. Phys. Lett.* **96**, 192102 (2010).

21 Fortunato, E. *et al.* Transparent p-type SnOx thin film transistors produced by reactive rf magnetron sputtering followed by low temperature annealing. *Appl. Phys. Lett.* **97**, 052105 (2010).

22 Lee, H.-N., Kim, H.-J. & Kim, C.-K. p-Channel Tin Monoxide Thin Film Transistor Fabricated by Vacuum Thermal Evaporation. *Jpn. J. Appl. Phys.* **49**, 020202 (2010).

23 Liang, L. Y. *et al.* The structural, optical and electrical properties of Y-doped SnO thin films and their p-type TFT application. *J. Phys. D: Appl. Phys.* **45**, 085101 (2012).

24 Ogo, Y. *et al.* p-channel thin-film transistor using p-type oxide semiconductor, SnO. *Appl. Phys. Lett.* **93**, 032113 (2008).

25 Yabuta, H. *et al.* Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits. *Appl. Phys. Lett.* **97**, 072111 (2010).

26 Caraveo-Frescas, J. A. *et al.* Record Mobility in Transparent p-Type Tin Monoxide Films and Devices by Phase Engineering. *ACS Nano* **7**, 5160-5167 (2013).

27 Togo, A., Oba, F., Tanaka, I. & Tatsumi, K. First-principles calculations of native defects in tin monoxide. *Phys. Rev. B* **74**, 195128 (2006).

28 Ogo, Y. *et al.* Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application. *Phys. Status Solidi A* **206**, 2187-2191 (2009).

29 Granato, D. B., Caraveo-Frescas, J. A., Alshareef, H. N. & Schwingenschlögl, U. Enhancement of p-type mobility in tin monoxide by native defects. *Appl. Phys. Lett.* **102**, 212105 (2013).

30 Bhansali, U. S., Khan, M. A. & Alshareef, H. N. Electrical performance of polymer ferroelectric capacitors fabricated on plastic substrate using transparent electrodes. *Org. Electron.* **13**, 1541-1545 (2012).

31 Mao, D., Quevedo-Lopez, M. A., Stiegler, H., Gnade, B. E. & Alshareef, H. N. Optimization of poly(vinylidene fluoride-trifluoroethylene) films as non-volatile memory for flexible electronics. *Org. Electron.* **11**, 925-932 (2010).

32 Khan, M. A., Bhansali, U. S., Cha, D. & Alshareef, H. N. All-Polymer Bistable Resistive Memory Device Based on Nanoscale Phase-Separated PCBM-Ferroelectric Blends. *Adv. Funct. Mater.* **23**, 2145-2152 (2013).

33 Park, C. H., Lee, K. H., Lee, B. H., Sung, M. M. & Im, S. Channel/ferroelectric interface modification in ZnO non-volatile memory TFT with P(VDF-TrFE) polymer. *J. Mater. Chem.* **20**, 2638-2643 (2010).

34 Yoon, S. M. *et al.* Impact of interface controlling layer of Al2O3 for improving the retention behaviors of In-Ga-Zn oxide-based ferroelectric memory transistor. *Appl. Phys. Lett.* **96**, 232903 (2010).

The research work described in this chapter was done in collaboration with PhD student Mohd Adnan Khan. A summary of this chapter can be found in

J. A. Caraveo-Frescas, M.A. Khan, and H. N. Alshareef. High Performance Nonvolatile Memory Using Transparent p-type Oxide Semiconductor SnO and Organic Ferroelectric Layer. (*to be submitted*)

Chapter 7

Summary and Future Perspectives

This chapter summarizes the most relevant findings and achievements of this research work and gives an overview of future research perspectives. General conclusions of the four major topics discussed in this dissertation are presented followed by a brief summary of the remaining challenges of tin monoxide thin films and devices.

7.1 Summary

The main conclusion of this research work is that tin monoxide can be used as a transparent p-type oxide semiconductor for the fabrication of transparent and flexible electronics at temperatures below 200 °C. Thin films of SnO can be deposited by dc reactive magnetron sputtering that can be used for the subsequent fabrication of field effect devices.

A comprehensive study of the deposition condition of SnO has been performed in order to optimize the conditions to obtain high mobility p-type oxide. The feasibility of SnO as a p-type semiconductor has been demonstrated by the fabrication of high performance field effect devices such as thin film transistors, nanowire transistors and ferroelectric transistors. The following paragraphs summarize the most relevant achievements of this research work.

7.1.1 SnO Thin Films

- P-type SnO can be successfully deposited by a DC reactive magnetron sputtering at room temperature, following a post deposition annealing procedure in air in order to crystallize it.
- Careful deposition control is required to achieve high mobility SnO thin films, exhibiting Hall mobility as high as 18.7 $cm^2V^{-1}s^{-1}$.
- High mobility SnO thin films can be deposited at a relative oxygen partial pressure of 9%, deposition pressure of 1.8 mTorr and DC power of 30 watts in a reactive sputtering process from a metal tin target.
- Presence of around 3 at% metal phase in a matrix of SnO is beneficial to achieve high mobility p-type SnO films.

7.1.2 Thin Film Transistors

- High performance thin film transistors can be fabricated with SnO in both rigid and flexible devices at temperatures as low as 180 °C.
- Device engineering is of special importance to achieve high performance TFTs: ITO gate electrodes, HfO_2 gate dielectric and Ti/ITO source and drain electrodes showed to be the best combination for enhanced device performance.
- A field effect mobility of 6.75 $cm^2V^{-1}s^{-1}$ demonstrated here stands out as the highest mobility value reported so far for any p-type oxide semiconductor field effect device.

7.1.3 Nanowire Field Effect Transistors

- Nanowire field effect devices based on p-type SnO have been demonstrated for the first time.
- Device nanoscaling has been shown advantageous to further increase the carrier mobility of p-type SnO devices to a field effect mobility >10 $cm^2V^{-1}s^{-1}$, at a maximum fabrication temperature of 160 ^oC.
- SnO nanowire transistors show superior device performance when compared to thin film transistors.

7.1.4 Ferroelectric Field Effect Transistors

- FeFETs based on p-type oxide semiconductor has been demonstrated for the first time, expanding the applications of oxide semiconductors to nonvolatile memory applications.
- The superior intrinsic electrical properties of SnO have yielded FeFETs with one order of magnitude higher mobility when compared to polymer-based FeFETs.

7.2 Future Perspectives

As expected with any research work, only a partial understanding is achieved at the end of the endeavor and many questions remain unanswered. Some future research paths for the full understanding of tin monoxide thin films and devices are presented in this section.

1. Electrical characterization as a function of film thickness and post annealing temperature. In order to better understand the electrical properties of SnO films, Hall effect measurements, as function of film thickness and post deposition annealing, are recommended to better understand the relevance of this two variables in carrier density and carrier mobility.
2. Carrier density modulation. An important challenge remaining for SnO, and other p-type oxides such as Cu_2O, is its relatively high carrier density. While some device engineering, such as double gated structures may be beneficial, finding adequate dopants is of paramount importance. Dopants and doping mechanisms should be explored to further enhance the electrical properties of SnO without compromising its transparency. Density functional theory simulations to find candidate dopants are recommended prior to any experimental effort.
3. Device Engineering. From a device perspective, several issues need to be addressed before SnO can be used as an active material in real-life applications. The most important parameter to be improved is the on-to-off current ratio. The relatively high off current of thin film and ferroelectric transistors likely arises from the high background carrier concentration of SnO as well as from a high number of surface defects in the active channel. The systematic investigation of surface treatments and

passivation layers is strongly recommended. Another suggested approach is the use of a different device structure such as the top gate configuration to prevent the semiconductor surface from atmosphere exposure.

4. Device Stability Characterization. Current and voltage stress measurements needs to be performed in order to assess the stability of SnO-based TFTs. Light stability is another important study to be performed on the transparent devices in order to asses their performance under light exposure.
5. Fabrication of CMOS structures. The main purpose of a high performance p-type oxide semiconductor is to allow the fabrication of CMOS devices. With several n-type oxides already well characterized, combinations of p-type SnO with the best performing n-type oxides (e.g. IGZO or IZO) must be fabricated. As SnO easily oxidizes to form n-type SnO_2, CMOS structures combining these two materials need to be explored.
6. Nanowire Transistors Downscaling. Further downscaling device dimensions, below 100 nm, is crucial to get a better understanding of the transport mechanism in SnO nanowires (quantum confinement, hole effective mass distribution, etc.).
7. FeFET device engineering and ferroelectric CMOS. Fully transparent devices need to be explored, as well as the subsequent fabrication of CMOS-based nonvolatile memory elements combining p-type SnO with a suitable n-type oxide.
8. Other techniques for material deposition. Even though magnetron sputtering is widely used in semiconductor industry, other deposition techniques should be explored. If low cost devices and large area processing is desired, non-vacuum based techniques must be explored. Solution based deposition techniques such as spin

coating and ink jet printing are particularly relevant if hybrid organic/inorganic devices are foreseen.

Even though transparent oxide electronics is an emerging field, it has already revolutionized the electronics industry. Wide gap semiconductors are extensively used as dielectrics in several electronic devices. Transparent conductors are being used in a wide range of optoelectronic applications such as displays, solar cells, and optical sensors, to mention a few. Oxide semiconductors have made impressive progress in the display industry allowing the fabrication of better, brighter, thinner and larger displays. The fully transparent display or some other see-through applications like the ones shown in Figure 7.1 are becoming close to reality. Transparent oxide electronics have arrived to complement existing technologies in the development of the next generation electronics. A very promising future is foreseen for this amazing technology.

Figure 7.1. Future Applications of Transparent Electronics. **a,** Transparent display concept. *From engadget.com*; **b,** Transparent smartphones. *From engadget.com*; **c,** Transparent office. *From microsoft.com*; **d,** See-trough portable devices. *From invisibleerc.eu.* **e,** Flexible displays. *From designbuzz.com*; **f,** Wearable electronics. *From ihealthtran.com*