Polymer Ferroelectric Memory for Flexible Electronics

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ABSTRACT

Polymer Ferroelectric memory for Flexible Electronics

Mohd Adnan Khan

With the projected growth of the flexible and plastic electronics industry, there is renewed interest in the research community to develop high performance all-polymeric memory which will be an essential component of any electronic circuit. Some of the efforts in polymer memories are based on different mechanisms such as filamentary conduction, charge trapping effects, dipole alignment, and reduction-oxidation to name a few. Among these the leading candidate are those based on the mechanism of ferroelectricity. Polymer ferroelectric memory can be used in niche applications like smart cards, RFID tags, sensors etc. This dissertation will focus on novel material and device engineering to fabricate high performance low temperature polymeric ferroelectric memory for flexible electronics. We address and find solutions to some fundamental problems affecting all polymer ferroelectric memory like high coercive fields, fatigue and thermal stability issues, poor breakdown strength and poor p-type hole mobilities. Some of the strategies adopted in this dissertation are: Use of different flexible substrates, electrode engineering to improve charge injection and fatigue properties of ferroelectric polymers, large area ink jet printing of ferroelectric memory devices, use of polymer blends to improve insulating properties of ferroelectric polymers and use of oxide semiconductors to fabricate high mobility p-type ferroelectric memory. During the course of this dissertation we have fabricated: the first all-polymer

ferroelectric capacitors with solvent modified highly conducting polymeric poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) [PEDOT:PSS] electrodes on plastic substrates with performance as good as devices with metallic Platinum-Gold electrodes on silicon substrates; the first all-polymer high performance ferroelectric memory on banknotes for security applications; novel ferroelectric capacitors based on blends of ferroelectric poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] and highly insulating dielectric poly(p-phenylene oxide) [PPO] with drastically improved fatigue and thermal stability; novel all-polymer ferroelectric diodes based on blends of ferroelectric [P(VDF-TrFE)] and n-type semiconducting [6,6]-phenyl-C61-butyric acid methyl ester [PCBM] with resistive switching properties and the first hybrid p-type ferroelectric memory with transparent tin monoxide [SnO] on plastic substrates with record mobilities.

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LIST OF ABBREVIATIONS

(Entries are listed alphabetically)

AFM	Atomic Force Microscopy
DMSO	Dimethyl sulfoxide
DMF	Dimethyl Formamide
DFT	Density Functional theory
FeFET	Ferroelectric field effect transistor
IC	Integrated circuit
MEK	Methyl-Ethyl-Ketone
PPO	poly(p-phenylene oxide)
PVDF	poly(vinylidene difluoride)
P(VDF-TrFE)	poly[(vinylidene-difluoride-trifluoroethylene]
PEDOT:PSS	poly (3,4-ethylenedioxythiophene)-poly(styrenesulfonate)
RFID	Radio Frequency Identification
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
TFT	Thin film transistor
WORM	Write Once Read many
XRD	X-ray diffraction

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CHAPTER 1

INTRODUCTION

1. Motivation and Background

Flexible electronics has made remarkable progress during the last 15 years, especially in the field of organic/polymer thin film transistors (OTFTs), organic light emitting diodes (OLEDs), polymer memory, and sensors. The large-area, flexible electronics market is currently a 2 billion US $ market and expected to grow to about US $250 Billion by 2025 (Fig. 1.1(a)) [1]. An essential part of most flexible electronic circuits is a non-volatile memory that can be used to store and retrieve information when required. In fact logic/memory is expected to be the leading technology in flexible electronics, capturing 32 % of the market share (Fig. 1.1(b)) [1].

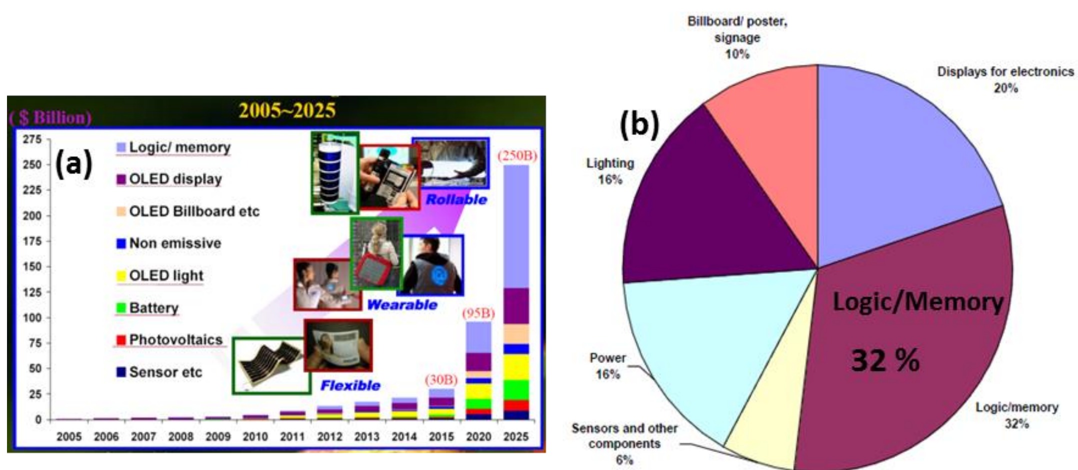

Figure. 1.1. (a) Projected growth for flexible electronics market. (b) Projected market share of different technologies in flexible electronics by 2020. [1]

Traditional memory circuits based on silicon are difficult to integrate with plastic substrates due to the high processing temperature for silicon and its poor flexibility. Polymeric memories are a promising alternative due to their simple device structure, low temperature processability, low cost, large information storage capacity and multi-layer stacking possibility [2]. Polymeric materials possess unique advantages, like good mechanical strength, high flexibility and most importantly ease of processability. A variety of deposition techniques such as spin-coating, spray-coating, dip-coating, roller-coating and ink-jet printing can be used to deposit polymers on a variety of substrates (plastics, silicon wafers, paper, glass etc.) for large scale low cost fabrication of memory devices (Fig. 1.2(a) and (b)).

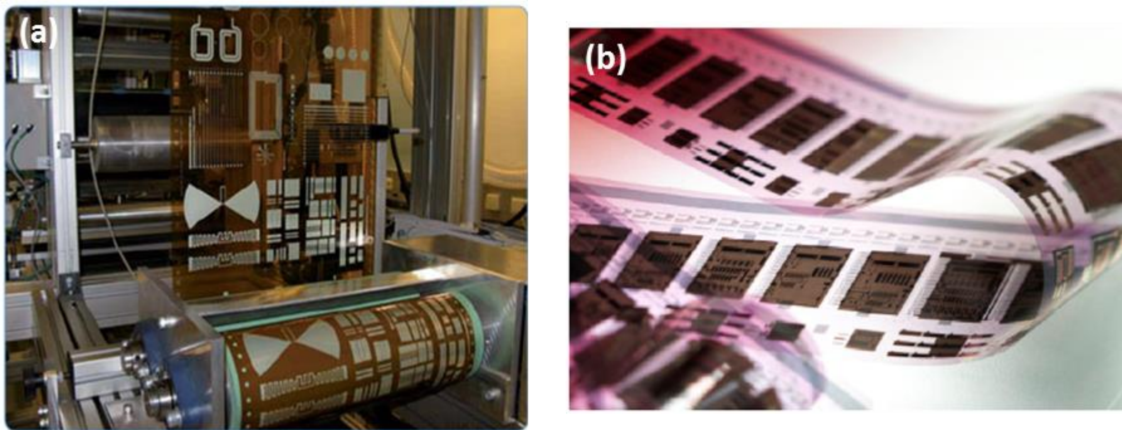

Figure. 1.2 (a) Roll to roll processing on plastic substrates (b) Large area printed, flexible polymeric circuits for RFID application [2].

One of the major markets that one can think for the use of polymer memory would be low cost mass data storage. In this market, it would have to compete with

Flash memory (a multi-billion dollar market) by lowering the fabrication costs [3]. Integrated memory circuits (IC's) for niche applications would be another potential market for polymer memory. A popular example is the RFID tag (radio-frequency identification) [3]. These tags are small ICs that communicate data stored in its memory via radio. The RFID tags can potentially replace bar codes. RFID tags fabricated by using silicon, cost around $ 0.35 per tag. Thus to compete in this market the cost price of the RFID tags must be only a few cents [3]. This might not be possible using RFID tags fabricated with silicon, but may be possible by using polymeric/organic materials that are cheaper to synthesize, can be solution processed and deposited over large areas using different techniques.

Many efforts are ongoing towards the fabrication of a fully polymer based nonvolatile-rewritable electronic memory device that can be used for a wide range of applications. Generally, electronic memories can be categorized into: Volatile and Nonvolatile memories (Fig. 1.3) [2]. Volatile memory loses the stored information as soon as it loses its power. They require a continuous power source so they don't lose the stored data. On the other hand non-volatile memory will retain the stored information or data even when it loses its power supply. Among volatile memories, DRAM (random access memory) is the most popular and is mainly used for computers/laptops today. It stores each bit i.e. "1" or "0" in a separate capacitor, but is volatile as the stored charge leaks away with time. Thus it loses its data when the power supply is turned off. Volatile memories such as these are unsuitable for applications like

RFID tags, where the stored information in the tag is sent via a radio signal. RFID tags get their power from the radio signal that they use to communicate; thus there is no constantly available power source [3]. Therefore, they cannot perform a memory refresh operation whenever necessary to prevent loss of information. A nonvolatile memory, where the information is preserved after removing the external power, is ideal for such applications.

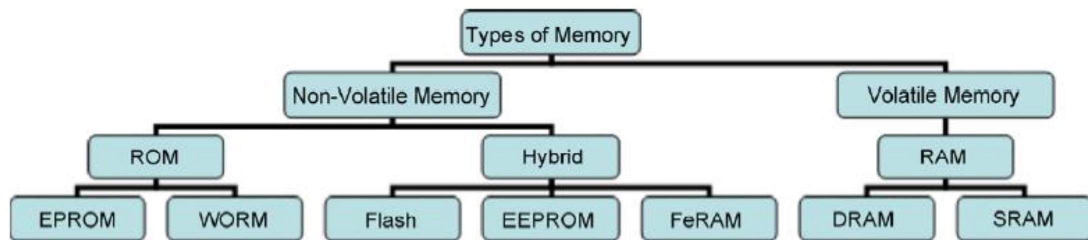

Figure. 1.3 Classification of different types of memory [2].

Non-volatile memories can be classified into read only memories and rewritable memories. Among read only category the WORM i.e. Write-Once-Read-Many is the most widely studied and reported. WORM memory with its non-volatile character can store data permanently and be read repeatedly. It can be written onto just once and thereafter the data cannot be modified. WORM memory can be used for archives, databases where large information has to be kept reliably and made available for a long time. Examples of WORM memory in daily life are digital optical disc storage devices such as Compact disc (CD) drives, Digital Versatile Disc (DVD-R) drives or Programmable Read only memories (PROMs). In the rewritable category, Flash memory is the most

widely used. It is possible to electrically reprogram the stored data and thus, it is non-volatile and rewritable. Flash memory is used in a number of systems such as Personal digital assistors (PDA's), laptops, MP3 players, digital cameras, smartphones and tablets. The current technology for flash memory is based on metal-oxide-semiconductor field-effect transistors (MOSFET) with a floating gate [2]. The problem with using flash memory is that the voltage during the write or erase process is very high and thus requires a charge pump. Furthermore the writing speed of flash memory is not fast enough (several milliseconds) and it suffers from poor endurance (up to 10^6 cycles) [2].

To store data, memory materials use a physical property that displays hysteresis in response to an external stimulus. By measuring the current state of the hysteresis one can retrieve the stored data. Many different physical properties can be used to obtain a memory effect. Some of the efforts in polymer memories are based on different mechanisms such as filamentary conduction, charge trapping effects, dipole alignment, and reduction-oxidation to name a few [4]. In this dissertation, the aim is to fabricate all-polymer non-volatile memory devices focused on one particular mechanism, i.e., those based on ferroelectricity particularly for flexible electronics applications. To provide the basic knowledge on materials, physical properties and concepts employed in the rest of this dissertation, this chapter is dedicated to an introduction. We first introduce ferroelectricity and ferroelectric polymers. This is followed by a discussion on the working principle of ferroelectric memory devices; in particular ferroelectric capacitors and transistors. After this we have a review on the current state of research

for ferroelectric memory devices. Lastly we end with a short summary or outlook of the field.

2. Ferroelectricity and Ferroelectric polymers

Ferroelectric memory (FeRAM) is gaining a lot of popularity due to its non-volatile and rewritable property. Ferroelectric materials have a spontaneous electric polarization which is reversible upon the application of an external electric field (EF) and more importantly they retain the polarization state even upon removal of the electric field [4]. When dielectrics are placed in a uniform external electric field, a displacement of positive and negative charges leads to the polarization of the dielectric material. This induced polarization creates a so-called depolarization field; an EF in the opposite direction, which tends to bring the displaced charges back to their equilibrium position after removing the external field. For most materials, “the polarization P”, is a linear function of the “applied external electric field: EF” (Fig. 1.4(a)) [5].

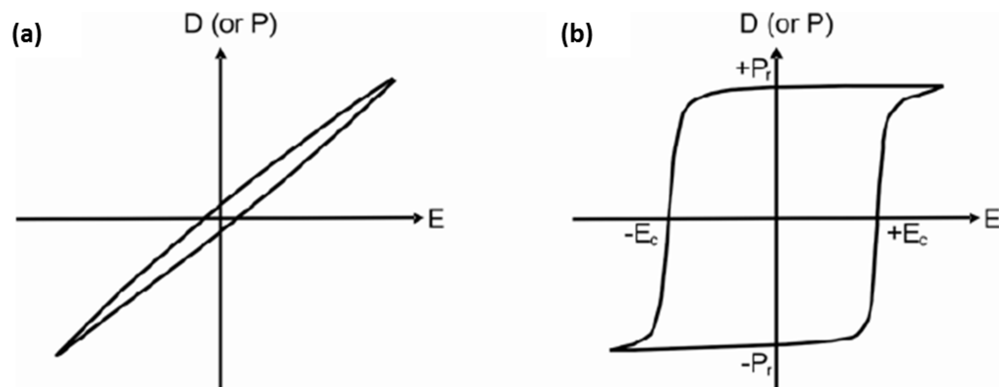

Figure. 1.4 (a) Polarization loop in a normal dielectric (b) Polarization (Hysteresis) loop in a ferroelectric dielectric [5].

This is called dielectric polarization. For most dielectric materials the plot of charge displacement (or polarization) versus electric field, does not show any significant hysteresis upon applying an external electric field (Fig. 1.4(a)).

In 1921 a new property, called ferroelectricity, was discovered in Rochelle salt ($KNa(C_4H_4O_6)\cdot 4H_2O$) by Valasek [3]. Ferroelectric dielectric materials show a non-linear polarization as a function of applied electric field. They show an electric hysteresis with a remnant polarization P_r; polarization that is retained by the material even when the field is removed (Fig. 1.4(b)). The term ferroelectricity comes from the similarity between ferroelectrics and ferromagnets. The way the hysteresis curve of P versus EF of ferroelectrics varies is the same as M versus H for ferromagnets [3]. The hysteresis loop of polarization versus applied field of ferroelectric materials can be used for non-volatile data storage. The polarization states ($\pm P_r$) up and down can be used to store “1” and “0”, respectively. When the external electric field is removed, the polarization state remains unchanged. As a result, ferroelectric materials are ideal for non-volatile memory applications.

Ferroelectricity remained a theoretical curiosity for long until ceramics were discovered. It started with the discovery of ceramics such as barium titanate ($BaTiO_3$) in 1944 and most notably lead zirconate titanate ($Pb(Zr,Ti)O_3$, PZT). The most widely used ferroelectric materials is $Pb(Zr,Ti)O_3$ (PZT) which is a perovskite, and $Sr(Bi,Ta)_2O_9$ (SBT) which is a layered material. The issue with these perovskite materials is the high

processing temperature requirements and their brittle nature which makes them unsuitable for flexible electronic applications.

Alternatively, ferroelectric polymers can be used for memory applications. Polymers have many attractive features: They can be solution processed and deposited at low temperatures on a wide different substrates using low cost techniques like gravure printing, ink jet printing, spin coating etc. [2]. Many polymers display polarization hysteresis due to charge injection or induced polarization. These mechanisms produce electrets, which display unstable piezoelectric and pyroelectric effects on a time scale of few hours to few days. However, the true definition of a polymer ferroelectric material is one which has a polar unit cell and an electric field can reverse the direction of the polarization/dipole moment [2,3,4]. Some polymers which exhibit ferroelectric properties are: (i) poly(vinylidene fluoride) (PVDF) and its copolymers, (ii) odd nylons, (iii) polyacrylonitrile, (iv) polyureas and polythioureas, and (v) ferroelectric liquid-crystalline (FLC) polymers (from attaching ferroelectric liquid-crystal molecules as side chains or pendant groups to polymer backbones) [2].

Among them, PVDF and its copolymer are the most widely used for FeRAMs. Poly(vinylidene fluoride) P(VDF) is very attractive for memory applications due to its large spontaneous polarization, short switching times, low leakage, excellent chemical stability, transparency and low temperature processability [4]. PVDF was discovered in the early 1970s to be ferroelectric. It has a simple chemical structure with a monomer unit of $–CH_2$-CF_2 (Fig. 1.5(a)). PVDF is used for a wide variety of applications, ranging

from protective coatings to ultrasound transducers. The highly electronegative fluorine atoms with a van der Waals radius of 1.35 Å, along with electropositive Hydrogen (1.2 Å) form polar bonds with the main chain, resulting in a very high dipole moment of 6.4×10^{-30} Cm [2,4]. This simple structure makes it highly flexible (like Polyethylene) but at the same time gives some stereo-chemical constraints (like Polytetraflouroethylene) to PVDF. The PVDF chains usually have head-to-tail configuration, but head-to-head and tail-to-tail defects can also occur (Fig. 1.5(b)).

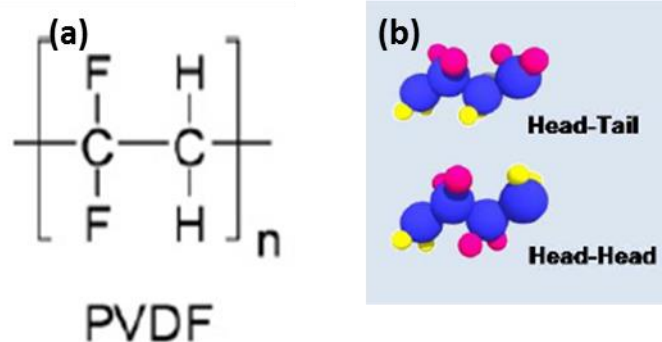

Figure. 1.5 (a) Chemical Structure of PVDF monomer (b) Molecular configuration in PVDF. (Fluorine atoms in Red and Hydrogen in Yellow and Carbon in Blue) [4].

PVDF can exist in at least three different stereo-chemical conformations: alternating trans (T) and gauche (G) (TGTG), all-trans (TTTT), and TTTG (Fig 1.6(a)). A major difference between these conformations is that the C-F and C-H bonds take different directions. Since the net dipole moment of the chain is the vectorial sum of dipole moment carried by individual segments, the different conformations exhibit

different net dipole moments. The all-trans conformation (TTTT) is the most polar one with dipole moment of 7.0×10^{-30} Cm per repeat unit perpendicular to the chain axis.

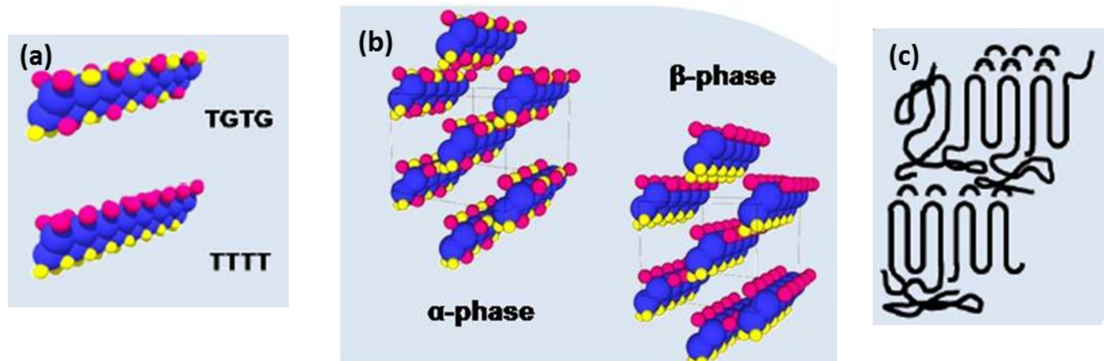

Figure. 1.6 (a) Conformation like TFTG and TTTT in ferroelectric polymers. (b) Different packing modes leads to different crystalline structures like the α and β phase (c) Typical nature of a semicrystalline polymer with crystalline and amorphous regions. (Fluorine atoms in Red and Hydrogen in Yellow and Carbon in Blue) [4].

PVDF is a semi-crystalline polymer, which means there are both crystalline and amorphous regions (Fig. 1.6(c)). In its crystalline region the polymer chains are packed into different crystalline forms, depending not only on the conformation of each individual chain but also the way of packing. The difference in packing of the polymer chains in the unit cell leads to four polymorphic crystals, referring to as α, β, γ and ϕ [2,3,4]. The non-polar α phase, with its TGTG conformation has chains are packed in a way that their dipole moments cancel each other, resulting in zero net polarization.(Fig. 1.6(b)) The most useful and interesting phase is the polar β phase in which has the all Trans (TTTT) conformation. Since the fluorine atoms are all positioned on one side of a unit cell, the β phase is a polar phase (Fig 1.6(b)). Thus the β phase is ferroelectric, due

to an optimal alignment of fluorine and hydrogen atoms in the chain. The unit cell in the β phase is orthorhombic, space group C_m2_m, and with lattice constants a = 8.58, b = 4.91, and c (chain axis) = 2.56 Å [5,6]. (Fig. 1.7(b)) When PVDF polymer is melted and subsequently cooled, the crystalline packing usually forms the non-polar α phase. But by annealing, poling or stretching the packing of ferroelectric chains can be modified to have a polar configuration i.e. α phase can be changed to the other three phases [2,4].

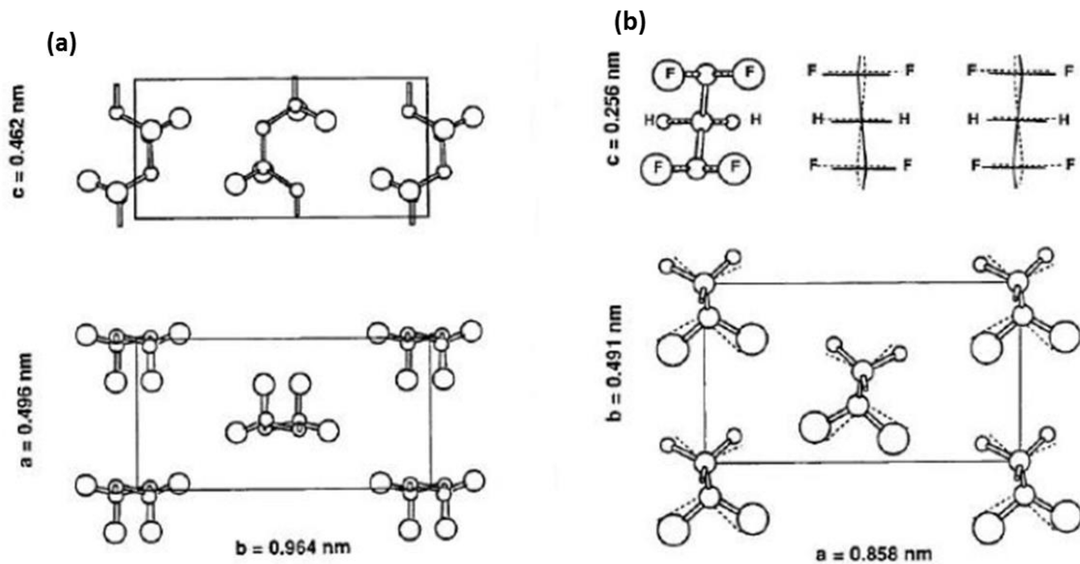

Figure. 1.7 (a) α phase of PVDF (b) β phase of PVDF. [5]

Getting the ferroelectric phase in PVDF can be tricky. Another option is to copolymerize VDF with TrFE ($CHFCF_2$) (Fig. 1.8(a)). The fluorine atoms which are larger than hydrogen, impart more steric hindrance. With the addition of TrFE into the VDF chain the unit cell size increases and easily allows the formation of the β phase with

TTTT conformation [2]. The copolymerization of PVDF with TrFE also helps to improve the crystallinity of the semicrystalline polymer ferroelectric film which is important as only the crystalline regions give rise to ferroelectricity. The dipole moments in amorphous regions have random directions and will cancel out each other leading to a net zero polarization. Also the addition of TrFE lowers the ferroelectric–paraelectric phase transition temperature or the Curie temperature (T_c) below the melting point. P(VDF-TrFE) is the only known ferroelectric polymer that has a measurable Curie temperature T_C which increases with increasing VDF content from 70 °C (50 mol%) to 140 °C (80 mol%) (Fig. 1.8) [6]. In PVDF homo-polymer the energy barrier for such transition is so large that no phase transition could be observed up to the melting temperature. Thus with a simple annealing step below the melting temperature and above the curie temperature, it is possible to fabricate high quality ferroelectric P(VDF-TrFE) thin films [6].

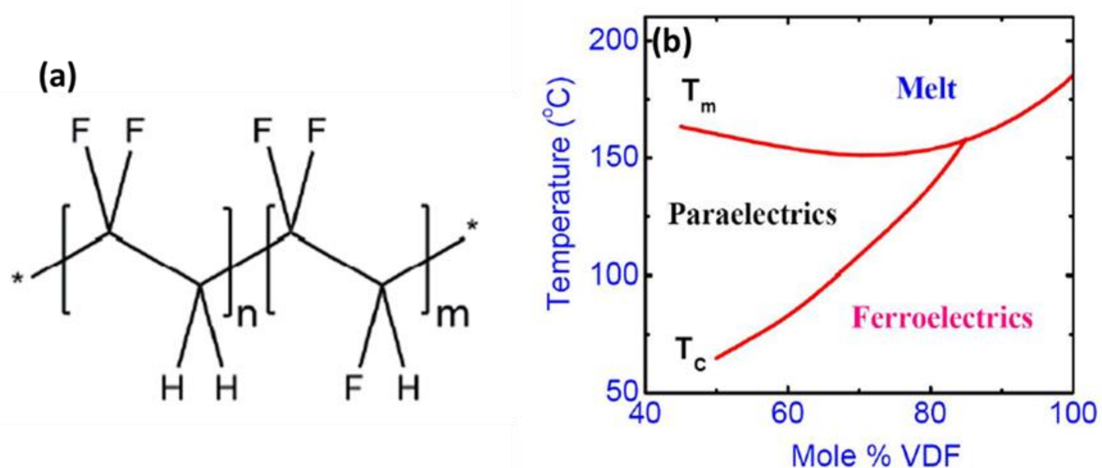

Figure. 1.8 (a) Chemical structure of P(VDF-TrFE) (b) Phase diagram of P(VDF-TrFE) [6].

P(VDF-TrFE) polymer chains have a net dipole moment pointing from the electronegative F to electropositive H (Fig. 1.9(a)). Figs. 1.9(a) and (b) show the dipole switching mechanism. The direction of the dipole is changed by a rotation of the polymer chain or molecule. This is possible due to the single C-C bonds that allow for some flexibility. The dipole switching is achieved by a large external EF opposite to the direction of polarization. “The reorientation of dipoles is not a simple 180◦ rotation but may progress through successive 60◦ rotations of the dipoles, which is consistent with the experimental observations and theoretical investigation at the molecular level” (Fig. 1.9(b)). [2,4]

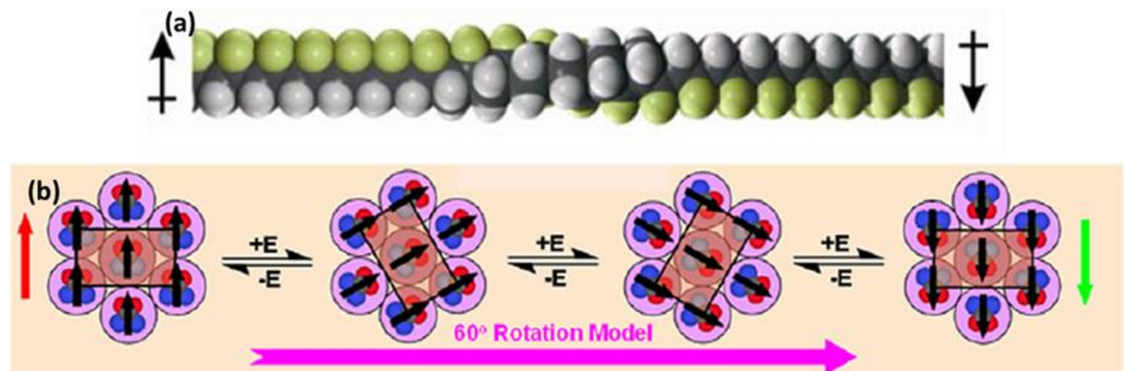

Figure. 1.9 (a) Illustration of the dipole switching in PVDF. (b) Dipole switching of fluorine-hydrogen dipoles based on 60° rotation model [2, 3].

3. Ferroelectric memory devices

a. Ferroelectric capacitors

The simplest ferroelectric memory device is a MFM structure i.e. Metal-Ferroelectric-Metal structure (Fig. 1.10(a)).

If we consider putting two conducting plates close to each other with vacuum in between and if we apply a voltage V across the plates, it generates an electric field E in the vacuum:

$$E = -\frac{V}{d} \qquad (1.1)$$

where d is the distance between the plates.

A charge of ±Q accumulates on both plates. The charge per unit area is:

$$D = \epsilon_0 E \qquad (1.2)$$

Also known as "charge displacement D", with ε_0 the dielectric permittivity of free space.

If a dielectric material is used instead of vacuum, then ε_0 is increased to the permittivity ε_{di} of this dielectric, also known as the relative permittivity (ε_r) or dielectric constant [7].

$$k = \frac{\epsilon_{di}}{\epsilon_0} \qquad (1.3)$$

If the Electric Field is kept constant then upon introducing a dielectric the charge displacement would increase (Eq. (1.2)). When a dielectric material is placed in an EF, it polarizes in the direction opposite to the field. This creates a small internal depolarizing field which opposed the applied external EF. This requires extra charges on the electrodes to maintain the same EF. For a ferroelectric MFM capacitor, Equation 1.2 becomes

$$D = \epsilon_{di} E + P \qquad (1.4)$$

with an additional polarization P. The theoretical polarization depends on the size and direction of the dipoles and their density. Polarization P depends on the history of the applied EF or in other words its last state and not just the instantaneous applied field. The most well-known technique for measuring P is with a Sawyer-Tower circuit, shown in Fig. 1.10(a). “A sinusoidal voltage signal is applied to one of the electrodes of the ferroelectric capacitor and the amount of charge displacement in the other electrode is measured using the voltage it creates over a reference capacitor connected in series. The voltage drop over the reference capacitor is minimized by using a large reference capacitor [7].”

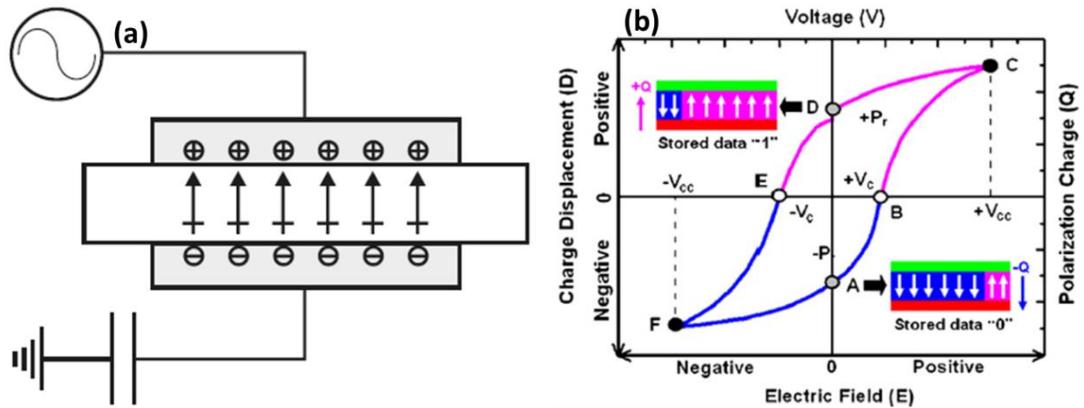

Figure. 1.10 (a) Sawyer-Tower circuit to measure polarization hysteresis in a ferroelectric capacitor (b) Polarization or Charge displacement versus Electric field curved for a typical ferroelectric capacitor [2,7].

Fig. 1.10(b) shows a typical hysteresis measurement of a ferroelectric capacitor. As the Electric field/Voltage is increased from 0 to $+V_{cc,}$ the polarization changes from A → B → C. Point C represents the maximum or saturation polarization of the capacitor (P_s) at max fields (V_{cc}). Upon decreasing the field to zero the polarization decreases to point D. Point D represents remanent or remaining polarization (P_r) at zero fields. It is slightly lower than saturation polarization due to relaxation of some dipoles (without reversing their direction). The minimum field necessary to switch or reverse the dipoles is known as the coercive field (V_c). To apply ferroelectric materials in memory devices, the two net stable states, “upward polarization $+P_r$” and “downward polarization $-P_r$”, can be defined as “1” and “0” signals.

To read the data one applies a field greater than the coercive voltage to detect a high/low charge displacement current depending on whether the dipoles/polarization were aligned or not with the direction of the external EF. Therefore ferroelectric capacitors suffer from “destructive read-out” since the read-out operation can erase the stored data. Thus we need a reset voltage to rewrite the erased data after every read operation [3]. The important property is the retention of polarization (remanent polarization-P_r) by the ferroelectric material even after the field is removed. In addition to the hysteresis curves, ferroelectric capacitors are characterized using leakage current, switching current, fatigue endurance, and dielectric dispersion properties.

b. Ferroelectric Field effect Transistors (FeFET’s)

The organic thin film transistor (OTFT) is composed of: (i) substrate which can be glass, silicon, plastic etc. (ii) Gate electrode (iii) source (S) and drain (D) electrodes, (iv) a dielectric, and (v) a semiconductor channel layer, as shown in Fig. 1.11. The channel length can be defined as the distance between the S and D (10 to 100 μm) and the channel width (W) is the actual width of the electrodes (100 μm to 1mm) [2]. Thin film transistors can be in two different configurations: (i) top contact (ii) bottom contact (Fig. 1.11). In a top contact device the S&D electrodes are deposited onto the semiconductor and in a bottom contact device the semiconductor is deposited onto the S&D

electrodes. Different conducting materials such as Al, Pt, Au, Ag, ITO, highly doped Si, PEDOT:PSS can be used as the electrode. In an OTFT the active channel layer is usually a conjugated molecule or polymeric semiconductor.

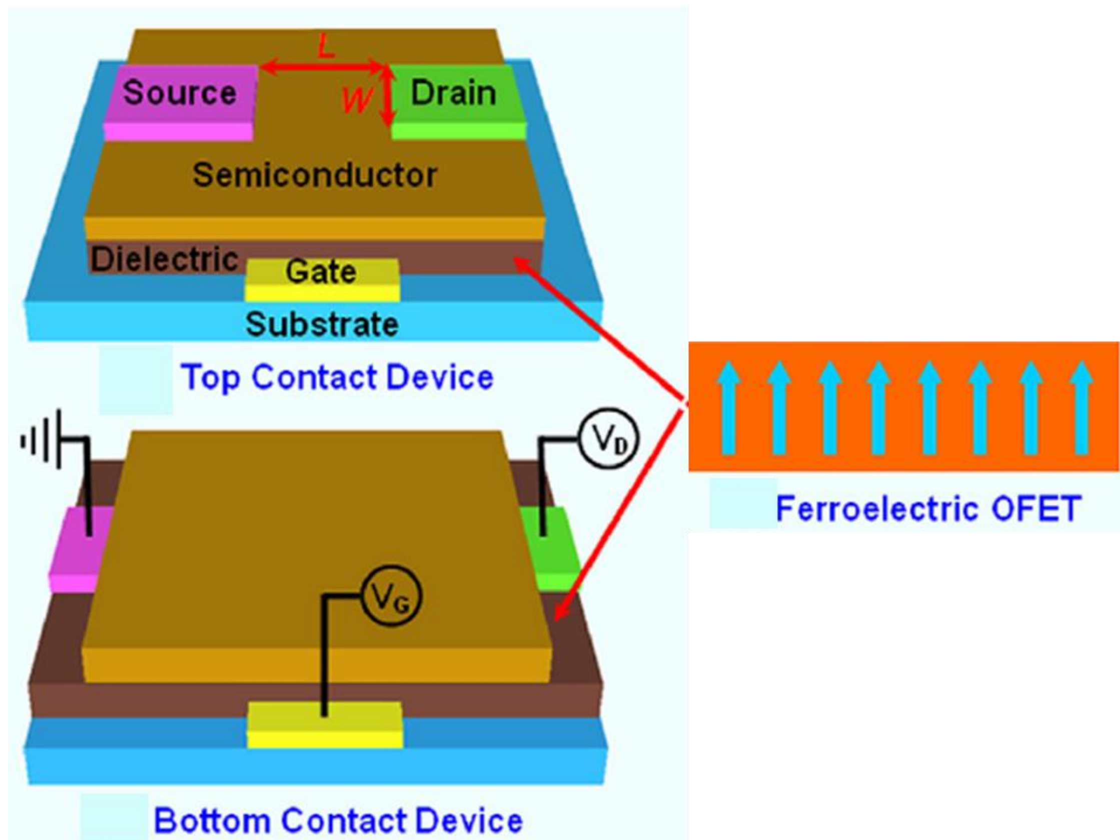

Figure. 1.11. OTFT in top and bottom contact configuration. If a ferroelectric polymer is used as the gate dielectric then it becomes a Ferroelectric Field Effect Transistor (FeFET) [2].

In 1963 the first FeFET was fabricated by Moll and Tarui, with triglycine sulphate (TGS) on a CdS substrate [7]. In a FeFET, a ferroelectric material is used as the gate dielectric layer and is in contact with active SC layer (Fig. 1.11). To read the current in the channel layer (I_d) one needs to apply a voltage between the S and D electrodes (V_d) so the charges can flow from Source to drain and one can detect the current (Fig. 1.12(a)). The drain current (I_d) depends strongly on the gate voltage (V_g) (Fig. 1.12(b)).

When we apply a voltage to the gate it can align the dipoles in the ferroelectric layer and induce surface polarization. This attracts charge carriers in the semiconducting channel and can induce either a high or a low drain current depending on the direction of polarization. This current remains high/low even after removing the gate bias (Fig. 1.12(b)). On the contrary, the OFETs lose the accumulated charges when the gate bias is removed and the device turns OFF. Thus they are volatile, which means that they can't be used for non-volatile memory. In contrast in a FeFET, the dipoles maintain their polarization state even after removal of the field. Therefore the I_d-V_g characteristics in a FeFET show a hysteresis effect with two stable states of high and low current (I_d) that can be related to a 1 or 0 required for memory applications.

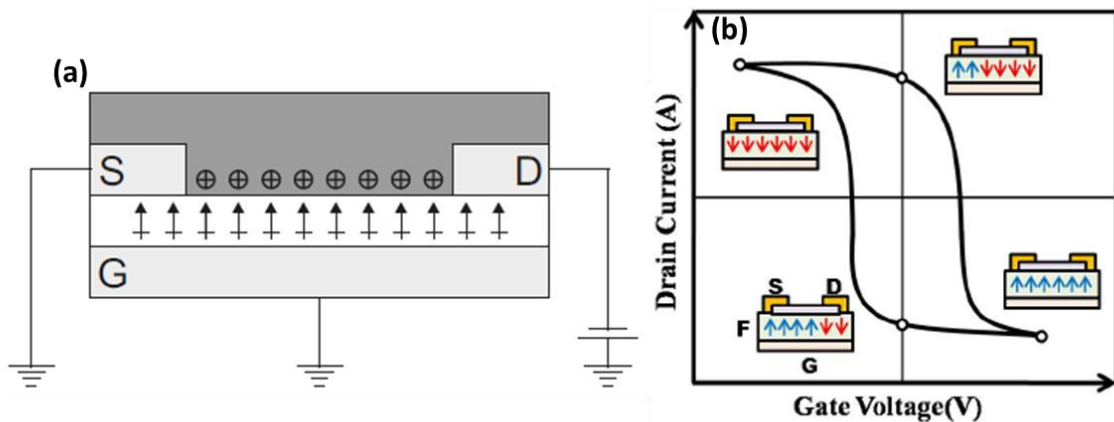

Figure. 1.12 (a) Layout of typical thin film transistor showing source, drain and gate contacts. (b) I_d-V_g characteristics of a FeFET

Thus the way a FeFET works is due to attenuation of charge carriers in the SC by the remanent polarization (P_r) of the ferroelectric layer. The major advantage of FeFET

over Ferroelectric capacitors is their non-destructive read out property. The drain current (I_d) which represents “1” or “0” can be sampled for long times using a low V_d and at zero V_g. This does not disturb the dipoles/polarization in the ferroelectric dielectric. Thus, we get combined non-volatile and non-destructive read out property by using FeFETs [2,3,4]. Another added advantage of using FeFET is that they are highly scalable. In a capacitor reduction of the electrode area is highly desirable because it increases the memory density. “The switching current during a dipole switching event scales with the electrode area A, remanent polarization P_r and switching time t_{sw} as:

$$I \ \alpha \ \frac{AP_r}{t_{sw}} \qquad (1.5)$$

An area reduction therefore reduces the signal. By contrast, the drain current of a FeFET working in the linear regime scales with

$$I \ \alpha \ \frac{V_d W \mu}{L} \qquad (1.6)$$

It will also increase with the charge density in the semiconductor induced by the ferroelectric. According to Eq. 1.6, if L and W are reduced by the same factor, the readout signal (I_d) is unaffected by scaling” [7]. Other important parameters for Ferroelectric transistors are the ON/OFF ratio, mobility, memory window, operating voltages and retention times.

4. Review on polymer ferroelectric memories

a. Ferroelectric capacitors

In the past, majority of the research on ferroelectric memory has focused on ferroelectric capacitors for potential use in 1T-1C memory cells. The two polarization states (+P_r and –P_r) of a ferroelectric capacitor are used to store “1” and “0” and can be written via an external electric field. To read the data one applies a field voltage greater than coercive voltage to obtain a high or a low switching current response (1 or 0). Some of the fundamental issues that need to be studied and resolved for polymer ferroelectric capacitors are: Reducing operating voltages, improving endurance or fatigue, improving thermal stability, decreasing switching speed and improving data retention properties.

Most of the literature available in the 80s and 90s has reported high operating voltages (50-100 V), low switching currents and poor fatigue behavior for ferroelectric capacitors. P(VDF-TrFE) has a high intrinsic coercive field of 50 MV/m, which leads to high operating voltages and thus are applicable for commercial memory devices. To reduce the operating voltage once needs to use thinner films. There are two reports 1986 and 1995 which tried spin coated P(VDF-TrFE) films with thickness below 200 nm; but these studies reported a poor ferroelectric response of the films [3]. In 1998 a study reported very thin P(VDF-TrFE) films (~15 nm) fabricated using the Langmuir–Blodgett technique. But these films could not be used for practical applications due to very high switching fields (500 MV/m), long switching times (3 orders of magnitude longer). An

important discovery was published in 2004 by Naber et. al. which showed good ferroelectric response from films with thicknesses down to 65 nm [8]. This report showed that it's possible to have operating voltages of ~ 10-12 V while retaining the P_r and t_{sw} of the bulk ferroelectric film. The trick was by using an interfacial layer of conducting polymer PEDOT:PSS between the bottom metal electrode and ferroelectric P(VDF-TrFE). Previously most reports have used Al electrodes, which was shown to react with the P(VDF-TrFE) and form a non-ferroelectric "dead" layer. Use of an interfacial layer of PEDOT:PSS helps prevent any such unwanted reactions [4].

Another major issue for ferroelectric capacitors is their fatigue endurance. Fatigue is the primary damage mechanism for ferroelectric capacitors. It is the drop in available remnant polarization upon repeated switching or stress cycles. Fatigue has been studied extensively in P(VDF-TrFE) based ferroelectric capacitors. Zhu et. al. studied fatigue and found it to vary with the frequency and field of fatigue [9]. Electric field profiles with lower frequency and higher voltages lead to more fatigue and they proposed that it is due to trapped charges, injected from electrodes into the ferroelectric film [9]. There are other studies showing the effect of different electrodes, annealing conditions and frequency on the fatigue performance of ferroelectric capacitors. Regardless majority of the literature still suggests that fatigue is a major issue for polymer ferroelectric memory. Recently it was shown that a conducting polymeric interlayer between the bottom electrode and ferroelectric layer improved the

fatigue properties. Using a PEDOT:PSS film or Polypyrole film between the bottom metal and P(VDF-TrFE), prevented any unwanted reactions and dead layers to form [2, 4].

The existence of the above literature suggested that conducting polymers can enable memory devices based on ferroelectric polymers. The findings suggested that it would be possible to fabricate all-polymer ferroelectric capacitors for flexible electronic applications. All-polymer devices would be ideal for flexible electronics because of their low cost, flexibility and low temperature requirements. Further polymers are more compatible with low cost large area deposition techniques such as ink-jet printing, micro imprinting, and contact printing on plastic substrates. Recently there was a study on all polymer ferroelectric capacitors on but reported very limited data with poor ferroelectric response [11]. To the best of our knowledge, there are no reports on high performance all polymer ferroelectric capacitors on flexible substrates.

b. Ferroelectric Field effect Transistors (FeFET’s)

Inorganic FeFETs based on PZT, SBT etc. have been studied for a very long time but still have not been implemented on a large scale for commercial products. They suffer from charge trapping at the FE-SC interface and poor thermal stability. In contrast polymer based Ferroelectric transistors don’t have such issues at the interface. The surface of organic materials does not experience strong columbic forces as organic

materials are mainly held together by relatively weak Van-der-Waals and/or hydrogen bonding. However, polymer based FeFETs have their own problems and challenges [3].

The initial work on polymer FeFET's mainly started with the use of small molecule pentacene as the semiconducting active channel. The mobility of FeFET's depends a lot on the quality of the interface between the ferroelectric and semiconducting layers. Historically as mentioned by several studies, pentacene based polymer FeFET's suffer from low mobility and low yield due to the high surface roughness of P(VDF-TrFE) thin films [3]. P(VDF-TrFE) with its semicrystalline nature and needle like morphology leads to rough thin films. Pentacene needs to be highly crystalline to attain high charge carrier (hole) mobility. This is done by optimizing the crystal growth of pentacene and to achieve this it is a must to have smooth surfaces. One can think about reversing the structure and fabricating top gate FeFET's so that we have the pentacene layer deposited first. This is also detrimental to the performance of the FeFET's as the solvents used to dissolve P(VDF-TrFE) cause damage to the pentacene layer. Thus as a result, the performance and yield of pentacene based FeFET's is poor and mobilities are relatively low. The record mobility for pentacene based FeFET's is ~ 0.1 $cm^2V^{-1}s^{-1}$, which was achieved by stretching of P(VDF-TrFE) thin films in order to make them smooth. There are a few other reports for pentacene based FeFET's. Matsuo et. al. used TGS [tri-glycine-sulphate] as the ferroelectric layer and Schroeder et al. used amorphous nylon as the ferroelectric layer to fabricate pentacene based FeFET's [3]. TGS and Nylon do not suffer from high surface roughness as P(VDF-TrFE). The devices

showed decent performance with good ON/OFF ratios and low operating voltages. However, the poor ferroelectric properties of TGS and Nylon lead to other issues. FeFETs based on TGS and Pentacene had poor retention i.e. The ON/OFF ratio decreases dramatically with time leading to poor non-volatile property. FeFET's based on Nylon ferroelectric layer suffered from very slow switching speeds (~ seconds) which is much slower than P(VDF-TrFE) based FeFET's (~ milliseconds). With a lot of major problems as mentioned above, it's difficult to see the commercialization of FeFET's based on organic small molecules.

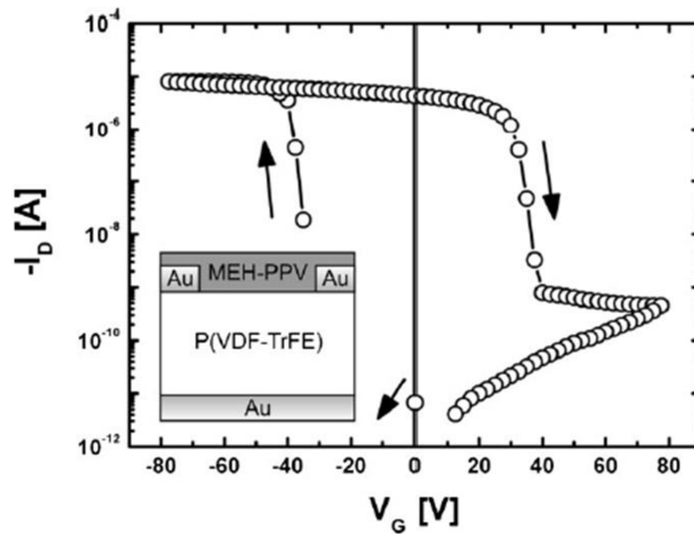

Figure. 1.13 (a) Transfer curve (I_d-V_G) of the first FeFET with a polymeric semiconductor (MEH-PPV) [3].

It was only as recent as 2005 that FeFET's based on polymeric semiconductors were fabricated. Fig 1.13 shows the transfer curve of the FeFET fabricated using P(VDF-

TrFE) as the ferroelectric layer and amorphous polymer MEH-PPV as the polymeric semiconductor [10]. The I_d-V_G curve demonstrates the non-volatile memory functionality and non-destructive read out property achieved. At positive bias the drain current is low in the p-type semiconducting MEH-PPV. By applying a negative gate bias, the drain current increases dramatically i.e. the device turn ON close to the coercive voltage of the ferroelectric gate dielectric. Even after the bias is removed the drain current remains high. This is because the dipoles in the P(VDF-TrFE) remain in the same direction even after the field is removed i.e. the ferroelectric dielectric remains polarized. This maintains the hole accumulation in the semiconducting MEH-PPV channel and thus the current remains high. This gives the FeFET its non-volatile characteristics. By applying a positive gate bias the device can be turned OFF. At zero gate bias it can be seen the drain current can vary by four orders of magnitude giving the device a high on/off ratio. This current can be read without applying a gate bias and at low drain voltages which does not disturb the ferroelectric polarization. Thus we can safely read the data stored non-destructively. To confirm that the bistable and nonvolatile behavior is coming from the ferroelectric property of P(VDF-TrFE) the authors fabricated transistors by replacing the P(VDF-TrFE) with PTrFE [10]. PTrFE is also a semicrystalline polymer and highly polar just like P(VDF-TrFE) but with negligible ferroelectricity. Transistor devices made with PTrFE as the dielectric displayed very little or negligible hysteresis in the transfer measurement. This confirmed that bistability and non-volatility in the earlier devices was due to the ferroelectric properties of P(VDF-TrFE). Later there were a few studies showing memory transistors with rr-P3HT and TIPS

pentacene transistors. But all these studies of polymer FeFET's have reported poor performance with low mobilities, high leakage, poor retention characteristics and high operating voltages. Surface roughness, use of thick gate dielectric layers, leakage through the un-patterned channel layers are some of the reasons for the poor performance.

5. Dissertation Outlook

The potential and advantages of PVDF based ferroelectric polymers was realized in the 80's. Nonetheless the drive to commercialize polymer ferroelectric memory died in the mid 90's to early 2000's. This technology might have been pre mature for the market at the time as the flexible and plastic electronics industry was only taking its first steps. In contrast, memory technologies using silicon, oxides and other inorganic ferroelectric materials have been commercially available for a long time. However, there is renewed interest in the research community to improve the performance of polymer ferroelectric memory. In the last decade the organic LED and display industry has seen an exponential growth. The research and industry is realizing the plastic electronics will be the future. Hence it is critical to fabricate high performance polymer based memory which will be a critical and necessary component of any electrical circuit. Currently there are several media reports and patents suggesting that memory devices based on polymer ferroelectric capacitors are on the verge of commercialization. This confirms the large market potential for all polymer non-volatile ferroelectric memory. This

dissertation will focus on novel material and device engineering to fabricate high performance low temperature polymeric ferroelectric memory for flexible electronics. We will address some of the major limitations and problems for polymer ferroelectric memory like fatigue performance, thermal stability, breakdown strength and mobility in ferroelectric memory. Some of the strategies adopted in this dissertation but not limited to are: (1) Use of different flexible substrates (2) Electrode engineering to improve performance (3) Large area printing of ferroelectric memory (4) Use of polymer blends to fabricate novel ferroelectric devices (5) Use of oxide semiconductors to fabricate novel hybrid high performance ferroelectric memory.

Chapter 2: Fabrication and characterization of all polymer flexible and transparent ferroelectric capacitors (Organic Electronics 12 (2011))

“All-polymer, transparent ferroelectric devices have been fabricated on flexible PEN substrates. Specifically, the effect of polymeric and metal electrodes on the growth, morphology, crystallinity and orientation of P(VDF-TrFE) films was systematically characterized. The all polymer devices showed a big improvement in performance to previous reports on all polymer ferroelectric capacitors on flexible substrates.”

Chapter 3: Series Resistance effects of high performance polymer ferroelectric capacitors (Applied Physics Letters 101 (2012))

"Flexible ferroelectric capacitors with highly conducting modified polymer electrodes have been fabricated on plastic substrates with performance as good as metal electrodes on silicon substrates. It is shown that the polymer electrodes follow classical ferroelectric and dielectric responses, including series resistance effects. The improved device characteristics obtained using highly conducting doped PEDOT:PSS suggest that it may be used both as an electrode and as global interconnect for all-polymer transparent circuits on flexible substrates."

Chapter 4: Large area ink-jet printed all polymer ferroelectric memory (Microelectronic Engineering 105 (2013))

"Drop-on-demand piezoelectric inkjet-printing technique has been used to fabricate a functional cross-bar array of all-polymer ferroelectric memory devices. The polymer-ferroelectric-polymer device consists of a ferroelectric copolymer P(VDF-TrFE) film sandwiched between inkjet-patterned, continuous, orthogonal lines of PEDOT:PSS polymer as the bottom and top electrodes. The overall performance and polarization retention characteristics of these printed ferroelectric capacitors are comparable to metal and spin-cast polymer electrodes suggesting their potential use in large-area flexible electronics."

Chapter 5: Characterization of current transport in polymer ferroelectric devices (Organic Electronics (2013))

"In this study we report the charge injection characteristics in poly(vinylidene fluoride-trifluoroethylene), P(VDF-TrFE), as a function of electrode material in metal/ferroelectric/metal device structures. Symmetric and asymmetric devices with Al, Ag, Au and Pt electrodes were fabricated to determine the dominant carrier type, injection current density, and to propose transport mechanisms in the ferroelectric polymer. Implication of these results for degradation in P(VDF-TrFE) memory performance are discussed."

Chapter 6: Electrode engineering to fabricate fatigue free polymeric ferroelectric memory (Organic Electronics 13 (2012))

"Polymeric flexible ferroelectric capacitors have been fabricated using a transparent conducting oxide (ITO) and a transparent conducting polymer (PEDOT:PSS) electrodes. It is found that the polarization fatigue performance with transparent oxide and polymer electrodes exhibits a significant improvement over the polymer electrodes (20% vs 70% drop in polarization after 10^6 cycles). This result can be explained based on a charge injection model that is controlled by interfacial band-offsets, and subsequent pinning of ferroelectric domain walls by the injected carriers."

Chapter 7: High performance non-volatile ferroelectric memory on banknotes (Advanced Materials 24 (2012))

“Here, we demonstrate the first ever polymer ferroelectric memory fabricated on rough banknotes. These memory devices have great potential to be used in anti-counterfeiting circuitry for banknotes and along with RFID tags for tracking purposes. Our all-polymer devices show excellent performance with a maximum remnant polarization ~ 8.2 $\mu C/cm^2$, low coercive fields (50 MV/m), low leakage (~ 10^{-6} A/cm^2), record mobilities (~ 0.12 $cm^2/V.s$), high I_{on}/I_{off} ratio (~ $5x10^3$), large memory window (~ 8 V), low turn on voltages (~ −0.5 V), low operating (after switching) voltages (~ 4 V) and excellent retention characteristics upto 10000 sec.”

Chapter 8: All polymer memory based on phase separated ferroelectric-fullerene blends with resistive switching behavior (Advanced Functional Materials 23 (2013))

“Here we report the fabrication of the first ever all polymer ferroelectric diode. The ferroelectric diode is a simple two terminal device that shows resistive switching like the FeFET with non-destructive read out capability. Our diodes are fabricated from blends of ferroelectric P(VDF-TrFE) and n-type semiconducting PCBM. With careful optimization of the solvent and processing conditions, it is possible to spin cast very smooth blend films (R_{rms}~ 7.94 nm) and with good reproducibility. The devices exhibit high I_{on}/I_{off} ratios

($\sim 3x10^3$), low read voltages (~5 V), excellent dielectric response at high frequencies ($\varepsilon_r \sim 8.3$ at 1 MHz) and excellent retention characteristics upto 10,000 seconds."

Chapter 9: High performance ferroelectric memory based on phase separated PPO blends (Advanced Functional Materials (2013))

"High performance polymer memory is fabricated using blends of ferroelectric poly(vinylidene-fluoride-trifluoroethylene) (P(VDF-TrFE)) and highly insulating Poly(p-phenylene Oxide) (PPO). These blend devices display highly improved ferroelectric and dielectric performance with low dielectric losses (< 0.2 up to 1 MHz), enhanced thermal stability (~ upto 353 K), excellent fatigue endurance (80 % retention after 10^6 cycles at 1 KHz) and high dielectric breakdown fields (~360 MV/m)."

Chapter 10: High performance low temperature flexible hybrid p-type ferroelectric memory (Advanced Materials 24 (2012))

"Here, we report for the first time a hybrid organic/inorganic ferroelectric transistor based on transparent p-type oxide semiconductor tin monoxide and using P(VDF-TrFE) as the gate dielectric. A record mobility of 3.3 $cm^2V^{-1}s^{-1}$, large memory window (~ 16 V), low subthreshold swing (~ −4 $Vdec^{-1}$) and excellent retention characteristics up to 5000 sec have been achieved on both rigid and flexible devices fabricated at low temperatures (200 ^oC). The mobility achieved in our devices is 10 times higher than

previous reports on polymer-based p-type ferroelectric field effect transistors (FeFETs). The demonstration here of high performance hybrid memory using transparent p-type SnO at low temperatures opens the door for the development of CMOS-based non-volatile memory devices for the emerging transparent and flexible applications."

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CHAPTER 2

Fabrication and Characterization of All Polymer Flexible and Transparent Ferroelectric Capacitors

M.A. Khan, Unnat S. Bhansali, and H. N. Alshareef (Organic Electronics 12 (2011) 2225)

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Abstract

All-polymer, transparent ferroelectric devices, based on the functional polymer poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)], have been fabricated on flexible substrates. The performance of the all-polymer devices was studied and compared to devices with metal electrodes. Specifically, poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) [PEDOT:PSS] and Platinum (Pt) electrode effects on the morphology, crystallinity and orientation of P(VDF-TrFE) films were investigated. The devices with PEDOT:PSS electrodes showed similar hysteresis and switching current response compared to Pt electrodes. Furthermore, the devices with PEDOT:PSS electrodes showed higher polarization and lower coercive fields than values reported for other polymer electrodes used with P(VDF-TrFE) on flexible substrates.

1. Introduction

Polymer memories are promising circuit elements in the field of organic electronics due to simplicity in device structure, easy processability, low cost, large data storage capacity and potential 3D stacking possibility [1-4]. Among organic memories, ferroelectric memories based on P(VDF-TrFE) are of particular interest to the flexible and organic electronics community due to its sufficiently large spontaneous polarization, non-volatility, low leakage, excellent chemical stability and low temperature processability [1, 5, 6] .

The simplest P(VDF-TrFE) ferroelectric memory device is a thin film capacitor. Ferroelectric capacitor memories make use of the hysteresis behavior by associating +Pr and –Pr states with Boolean 1 and 0 logic states. To read data, one needs to apply a switching voltage to obtain a high or low current response. The problem with using P(VDF-TrFE) is its high coercive field of 50 MV/m, which has been a factor in preventing organic ferroelectric capacitors from being used on a commercial scale [7-9] . Using thinner films was considered as the solution to getting lower operation voltage. Recent studies have shown that as thickness is reduced there is a reduction in polarization, increase in switching field, increase in switching times and increase in leakage current [9-12]. One of the promising solutions is to use conducting polymers as interface layers or as electrodes to improve the ferroelectric device properties. This is because using all-polymer devices is more compatible with cost-effective processing techniques such as spin coating, ink-jet printing, micro imprinting, and contact printing on plastic

substrates. Although some studies have been reported on P(VDF-TrFE) with polymer interfacial layers [13-15], very limited studies have been reported on P(VDF-TrFE) capacitors with polymer electrodes on flexible plastic substrates [16]. In this work, we systematically characterize the growth of P(VDF-TrFE) film on polymer electrodes and compare the device properties to metal electrodes on plastic substrates.

2. Experimental

Polyethylene naphthalate (PEN) was used as the substrate. Prior to device fabrication, the substrate was cleaned by a sequence of ultra-sonication in acetone, isopropanol followed by DI water. The bottom PEDOT:PSS electrode was spin coated onto the plastic substrate at 1500 rpm for 30 sec followed by 5000 rpm for 30 sec to get a smooth film. The film was dried at 110 °C for 30 min in air. P(VDF-TrFE) copolymer powder was dissolved in methyl ethyl ketone (MEK) to get a 2 wt. % solution. The filtered solution was then spun on the PEDOT:PSS film at 6000 rpm for 60 seconds followed by a soft bake for 30 min at 80 °C. The films were then annealed in vacuum at 140 °C for 4 hours to improve the crystallanity [2, 13, 16]. The PEDOT:PSS electrodes were approximately 110 ± 10 nm thick and P(VDF-TrFE) film was ~100 ± 10 nm thick, measured using a Dektak profilometer. Finally, the top PEDOT:PSS electrode was spun and etched using RF oxygen plasma with patterned gold (Au) layer as a hard mask. For comparison, a sample with Au and Pt as top and bottom electrodes, respectively was also made with the same P(VDF-TrFE) thickness.

Surface morphology was studied using Atomic Force Microscopy (Agilent 5400) and Scanning Electron Microscopy (Nova NanoSEM 630 FESEM). The crystallinity and inter-planar distance of polymer chains was evaluated using Grazing Incidence X-ray Diffraction (Bruker D8 Discover) while the bonding and dipole orientation was analyzed using Fourier-transform infrared spectroscopy (FT-IR, Thermo-Scientific Nicolet iS10). The electrical characterization was performed using the Keithley 4200 semiconductor analyzer while Polarization-Voltage and fatigue tests were done using the Premier Precision II ferroelectric tester (Radiant Technologies Inc.).

3. Results and discussion

Fig. 2.1(a) and (b) show the surface morphology of platinum and PEDOT:PSS surfaces, respectively. The root mean square (R_{rms}) roughness values for Pt and PEDOT:PSS over 1 μm^2 area are comparable and are 0.44 nm and 0.55 nm, respectively. Fig. 2.1(c) and (d) show P(VDF-TrFE) films grown on Pt and PEDOT:PSS surfaces, respectively. The data shows that the P(VDF-TrFE) film grown on the polymer surface is smoother than on the Pt surface with a roughness value of 1.28 nm versus 2.3 nm. Fig. 2.1(e) and (f) show scanning electron microscopy (SEM) images of P(VDF-TrFE) films grown on Pt and PEDOT:PSS. The figure indicates a difference in the nucleation and grain growth rates of the films on the two respective electrodes. The average grain size of P(VDF-TrFE) is much smaller (~75-80 nm) when grown on a polymer, compared to a metal surface (~160-170 nm).

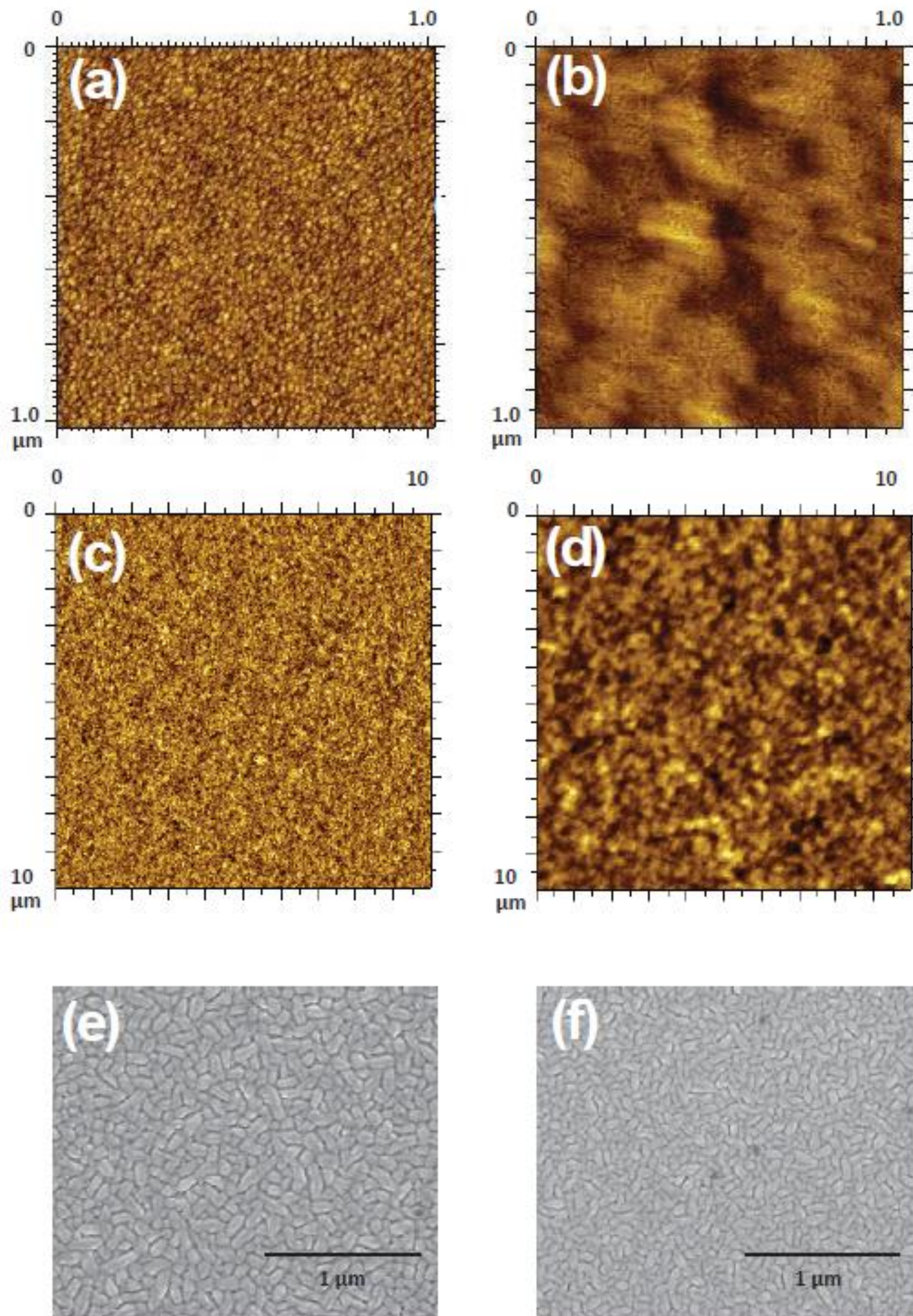

Figure. 2.1 AFM topography images of (a) Pt surface (b) PEDOT:PSS surface (c) P(VDF-TrFE) grown on Pt surface (d) P(VDF-TrFE) grown on PEDOT:PSS surface. SEM images of (e) P(VDF-TrFE) grown on Pt surface (f) P(VDF-TrFE) grown on PEDOT:PSS surface.

This result should not be surprising since the surface roughness of the bottom electrode has an effect on nucleation rate of the P(VDF-TrFE) film, with rougher surface leading to higher nucleation rate [17]. The higher nucleation rate limits the grain growth leading to smaller grains, as observed in our films. Additionally the higher nucleation rate and smaller grain size leads to a smoother P(VDF-TrFE) film on PEDOT:PSS as suggested by the AFM data.

Grazing Incidence XRD (GIXRD) was used to compare the phase and orientation of the P(VDF-TrFE) films on the resp. electrodes. Fig. 2.2 shows that P(VDF-TrFE) films on Pt substrate exhibit a peak centered at 2θ ~ 19.95°, characteristic of the ferroelectric β phase and reflection from the (110) and (200) planes. The inter-planar distance was calculated to be approximately 4.44 Å and is consistent with earlier studies [16].

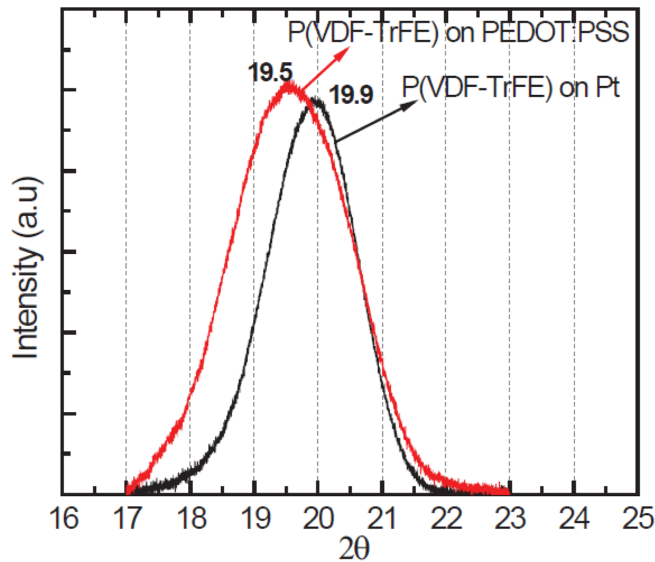

Figure. 2.2 Grazing Incidence XRD spectra of P(VDF-TrFE) films on Pt and PEDOT:PSS electrodes.

In comparison, the P(VDF-TrFE) films grown on PEDOT:PSS exhibit a peak at 2θ ~ 19.53°, indicating a larger inter-planar distance. The XRD peaks indicate that the P(VDF-TrFE) films on Pt electrodes have larger crystallite size than films on PEDOT:PSS electrodes, with a full-width-half-maxima (FWHM) of 1.67° and 2.2°, respectively, as confirmed by the SEM images.

In P(VDF-TrFE) films, it is important that the chain direction (c axis) is oriented parallel to the film surface because polarization is induced in the b-axis direction, perpendicular to the chain axis [18-20] . There have been some studies on techniques to control the preferential orientation of P(VDF-TrFE) chains by nano-imprint lithography and using nanostructured electrodes [20, 21] . We have analyzed the orientation of the P(VDF-TrFE) films as a function of growth on polymer and metal electrodes under identical annealing temperatures (140 °C) and thickness (100 nm). The dipoles in P(VDF-TrFE) strongly interact with the applied field, when it is perpendicular to the dipole direction. We used p-polarized FTIR analysis of the ferroelectric polymer films, which has an electric field component parallel to the plane of the substrate. It has been reported that the FTIR bands at 1288 cm^{-1} and 850 cm^{-1} are associated with CF_2 symmetric stretching vibration and are characteristic bands of the trans-zigzag formation (β phase)- indicating dipole moments parallel to the b axis [16, 18, 19] . It can be easily seen from Fig. 2.3 that 1288 cm^{-1} peak is relatively stronger on the film grown on Pt, therefore b axis (and dipoles) of the polymer is perpendicular to the film. The 1400 cm^{-1} band which is characteristic of the CH_2 wagging vibration has dipoles parallel

to the polymer chain c axis. For a baseline region of 1417.48 -1378.43 cm^{-1}, the area under the 1400 cm^{-1} band shows that this peak is relatively stronger on PEDOT:PSS (Area of 0.2074) compared to Pt (Area of 0.1431). This indicates that for P(VDF-TrFE) film grown on PEDOT:PSS a significant portion of the copolymer chain tilts vertically, which is undesirable for vertical polarization as most dipoles are parallel to substrate. All other peaks in the FTIR pattern of P(VDF-TrFE) film grown on PEDOT:PSS can be attributed to the PEDOT:PSS layer itself as can be seen from the IR spectra of the PEDOT:PSS at the bottom of Fig 2.3.

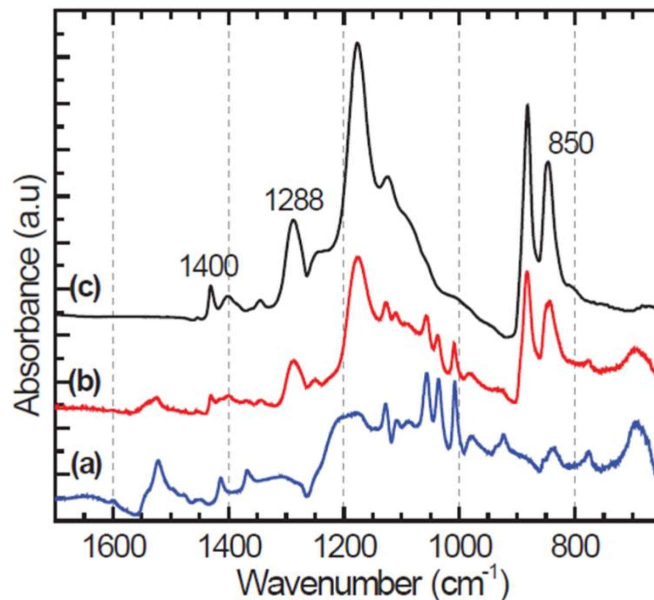

Figure. 2.3 p polarized FT-IR spectra of (a) spin coated PEDOT:PSS b) P(VDF-TrFE) film (~110±10 nm) on PEDOT:PSS and (c) P(VDF-TrFE) film on a Pt substrate

Ferroelectric behavior of our capacitors was tested using polarization-electric field hysteresis measurements. In Fig. 2.4, the hysteresis loops for the all-polymer

device show a remnant polarization (P_r) of 7.5 μC/cm^2 and coercive field (E_c) of 60 ± 5 MV/m. These values show a remarkable improvement compared to earlier studies using polymer electrodes on plastic substrates. Xu et al had earlier reported a P_r of 7.6 μC/cm^2 and an E_c of 130 MV/m with an all polymer capacitor with Polyaniline and PEDOT:PSS as top and bottom electrodes, respectively on a plastic substrate [22]. Our all polymer, flexible and transparent device also compares well with the device with metal electrodes which show a Pr of 7.5 μC/cm^2 and E_c of 54 ± 5 MV/m. The slightly higher coercive field could be attributed to the smaller grain size as well as the unfavorable orientation of P(VDF-TrFE) chains on the polymer electrode as seen from the FTIR data.

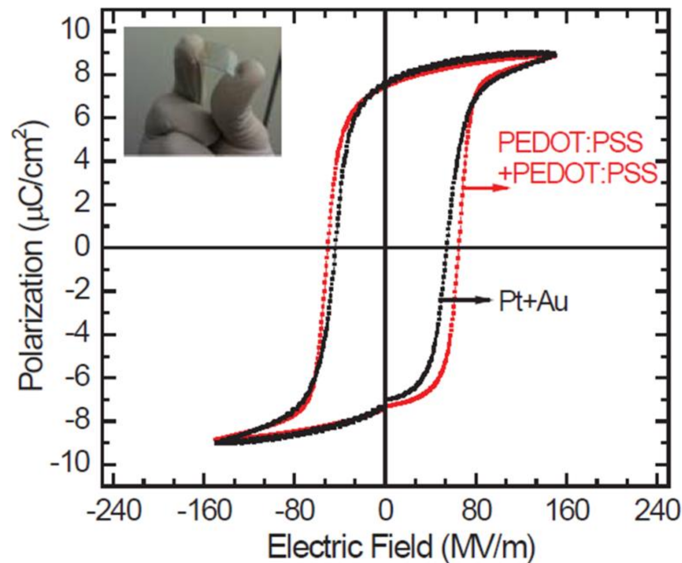

Figure. 2.4 Hysteresis loops at a frequency of 1 Hz and Electric Field of 150 MV/m from devices with Platinum/Gold electrodes and with PEDOT:PSS top and bottom electrodes

Fig. 2.5(a) shows that the switching current response of the all polymer devices is almost identical to the device with metal electrodes with a peak switching current

density ~20μA/cm^2. Leakage current mechanisms in dielectric films are usually controlled by space charge limited current (SCLC), interface limited Schottky emission (SE) or bulk limited Frenkel-Poole (FP) emission. SE involve carrier injection from the electrodes into the conduction band of the dielectric over a barrier height while FP emissions involves field-assisted thermionic emission of carriers trapped in the dielectric film [23, 24]. The best fit of I-V response for the all-polymer device is plotted for ln(J) versus $V^{1/2}$ as seen in the inset in Fig. 2.5(b). Linear behavior of this plot suggests that leakage current is controlled either by Schottky or Frenkel Poole emission. FP emissions are independent of the work functions of the electrodes and display symmetric I-V characteristics [23, 25]. A look at Fig. 2.5(b), shows the asymmetry of the leakage current response which confirms that FP emission is likely not possible in our devices.

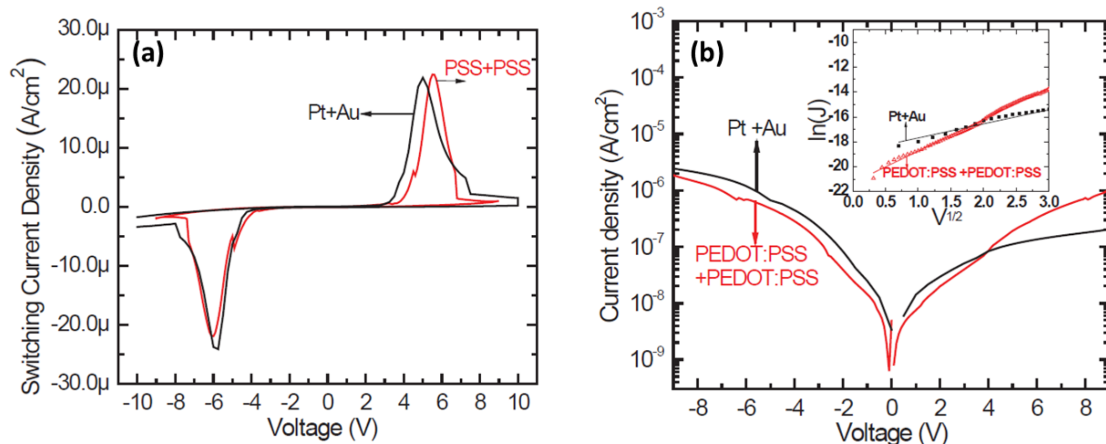

Figure. 2.5 (a) Switching current response from devices with Platinum/ Gold electrodes and with PEDOT:PSS top and bottom electrodes (b) I-V characteristics of devices with Platinum/Gold electrodes and PEDOT:PSS electrodes. The inset shows a plot of Current density versus Voltage$^{0.5}$ measured at room temperature.

The Schottky controlled leakage current is given by:

$$J = AT^2 exp\left(\frac{aE^{0.5} - \phi_B}{kT}\right) \quad (2.1)$$

where A is the effective Richardson's constant, T is temperature, E is applied electric Field, ϕ_B is barrier height and a is a constant [23] .

According to Fig. 2.5(b), the current response in our devices shows dependence on the work functions of the electrodes, confirming an interface limited Schottky emission process. The device with metal electrodes shows lower leakage current in the forward bias regime because of the higher work function of bottom Pt electrode (5.65 eV) compared to the top Au electrode (5.1 eV). The devices with PEDOT:PSS top and bottom electrodes show symmetric I-V curves. The work function for PEDOT:PSS is 5.2 eV which explains the slightly lower leakage current compared to the Au top electrode devices in the reverse bias regime.

4. Conclusions

In summary, we have fabricated all-polymer, flexible and transparent ferroelectric capacitors on PEN substrate. Electrical characterization showed that the all-polymer capacitors showed comparable ferroelectric properties (P_r ~ 7.5 μC/cm^2, E_c ~ 60 ± 5 MV/m) and I-V characteristics to capacitors with metal electrodes.

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CHAPTER 3

Series Resistance Effects of High Performance Polymer Ferroelectric Capacitors

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Abstract

Flexible ferroelectric capacitors with doped polymer electrodes have been fabricated on plastic substrates with performance as good as metal electrodes. The effect of doping on the morphology of polymer electrodes and its impact on device performance has been studied. Improved fatigue characteristics using doped and undoped poly (3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) electrodes versus metal electrodes are observed. It is shown that the polymer electrodes follow classical ferroelectric and dielectric responses, including series resistance effects. The improved device characteristics obtained using highly conducting doped PEDOT:PSS suggest that it may be used both as an electrode and as global interconnect for all-polymer transparent circuits on flexible substrates.

1. Introduction

Organic electronics targeting next generation transparent and flexible electronics applications continues to be heavily investigated. An integral part of most flexible electronic circuits is a non-volatile memory component, preferably transparent, that can be used to store and retrieve information as required. Traditional memory circuits based on silicon technology are difficult to integrate with flexible and transparent plastic substrates due to the required high-temperature processing and limited flexibility of silicon. These problems can be overcome by using polymer ferroelectric memories. A promising candidate material is poly(vinylidene fluoride- trifluoroethylene) P(VDF-TrFE) due to its transparency, non-volatility, large spontaneous polarization, excellent chemical stability, and low temperature processability [1-3]. Moreover, the use of easily patternable, spin-cast films of conducting polymer electrodes opens the possibility of large scale fabrication of flexible and transparent ferroelectric memory. The use of polymer electrodes presents unique challenges for the fabrication of electronic devices. In contrast to metal electrodes, the morphology and processing conditions of these conducting polymer electrodes can affect their properties and the electronic devices made thereof. There have been limited reports on the use of conducting polymers as electrodes and interfacial layers for ferroelectric capacitors [4-6] but there are no studies reporting on how the morphology and conductivity of the underlying polymer electrodes affects the dielectric and ferroelectric properties of the memory devices.

A variety of polymers such as Polypyrrole, Polyaniline and Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) offer a unique combination of properties that make them attractive for transparent electronics. These polymers are made conducting by the reaction of the conjugated semiconducting polymer with an oxidizing agent, a reducing agent, or a protonic acid. The conductivity of these materials can be modified by the nature and degree of doping [7]. The easily tunable optical, chemical and electrical properties of PEDOT:PSS make it the most widely used conducting polymer for numerous applications such as organic light-emitting diodes (OLEDs), organic photovoltaic (OPVs), organic thin film transistors (OTFTs), hybrid nanocomposites for thermoelectrics etc [8-10]. In this study, we analyze and compare the performance and reliability of capacitors fabricated using doped/undoped PEDOT:PSS polymer electrodes to metal electrodes. The device performance is characterized using polarization-electric Field (P-E) curves, capacitance-voltage (C-V) curves, dielectric spectroscopy and fatigue analysis.

2. Experimental

High performance thermoplastic Polyetherimide sheets (Ultem 1000B) supplied by Saudi Basic Industries Corporation (SABIC), were used as the substrate. Prior to device fabrication, the substrates were cleaned by ultra-sonication in acetone and isopropanol and de-ionized water. To study the effect of series resistance from polymer electrodes in a metal-ferroelectric-metal device architecture, a broad range of

conductivity is essential and hence PEDOT:PSS from Sigma Aldrich was used without modification with a conductivity of ~ 1 S/cm. In contrast, PEDOT:PSS in the form of Clevios PH-1000 from Heraeus was chemically doped to control its conductivity. We found that a maximum conductivity of ~ 915 S/cm could be achieved by doping the PH-1000 with ~ 4% Dimethylsulfoxide (DMSO). The thickness, sheet resistance and conductivity of spin-cast films of different kinds of PEDOT:PSS used in this study are summarized in Table 3.1. The thicknesses were measured using a Dektak profilometer and the sheet resistance values were measured with a 4-point probe system. The inherently hydrophobic Polyetherimide substrates were treated with O_2 plasma for 2 minutes, rendering the surface hydrophilic, essential for spin-casting uniform, thin films. Bottom electrodes were formed by spinning the PEDOT:PSS solutions at 1500 rpm for 30 seconds followed by annealing on a hotplate at 120 °C for 30 minutes. A 2 wt.% solution of P(VDF-TrFE) (70 – 30 mol%) dissolved in methyl ethyl ketone (MEK) was then spun on the PEDOT:PSS film at 3000 rpm for 60 s, followed by a soft bake for 30 min at 80 °C. The films were then annealed in vacuum at 135 °C for 4 hours to improve the crystallinity and obtain the ferroelectric phase. The P(VDF-TrFE) layer was ~ 120 ± 5 nm thick, as measured by a Dektak profilometer. Gold (Au) was thermally evaporated through a shadow mask to define the top electrodes. For comparison, a capacitor with Au and Pt as top and bottom electrodes, respectively, was also made with the same P(VDF-TrFE) thickness. Different bottom electrodes of Platinum, undoped PEDOT:PSS, and doped PEDOT:PSS are referred to as Pt, PSS and PH1000 respectively in all figures.

3. Results and Discussion

The morphology of PEDOT: PSS films spun on plastic Polyetherimide substrates was studied using Atomic Force Microscopy (AFM). Fig. 3.1 shows the phase image of doped (top) and undoped PEDOT:PSS (bottom) films. The phase image of PEDOT:PSS doped with approx. 4 % DMSO shows a fibrous morphology with connecting PEDOT chains (bright regions) in a matrix of PSS (dark).

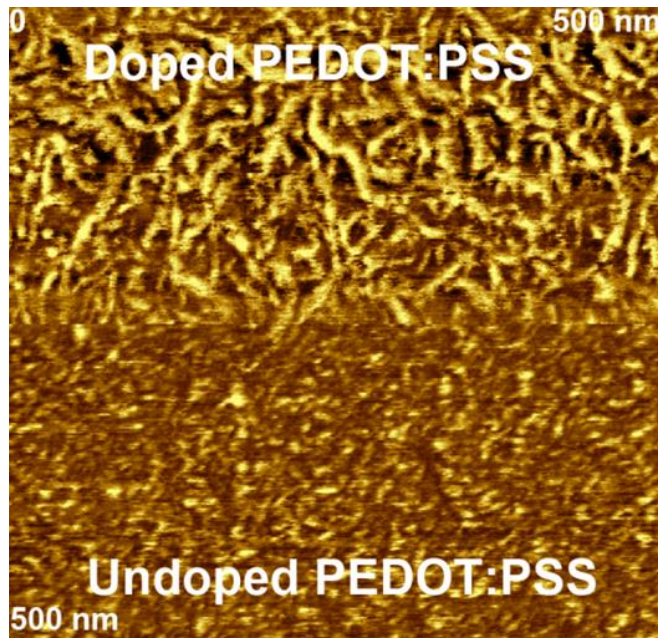

Figure. 3.1 AFM phase image of a 0.5 x 0.5 μm^2 area with top half showing morphology of doped PEDOT:PSS and bottom half of undoped PEDOT:PSS film.

It is well known that the addition of solvents like DMSO, Ethylene Glycol (EG) induces phase segregation at the nanometer level in PEDOT:PSS films [11]. Due to a thermodynamically driven rearrangement, the PSS phase segregates into insulating

domains (dark regions in phase image), while highly conducting PEDOT grains merge together to form a three dimensional conducting network (bright fibers in phase image). The presence of conducting PEDOT chains through which charge carriers can move freely, leads to the high conductivity seen in doped PEDOT:PSS films. On the other hand undoped PEDOT:PSS films show a granular morphology with the presence of isolated PEDOT domains in a matrix of insulating PSS phase. This leads to an increase in sheet resistance of undoped PEDOT: PSS films as seen from Table 3.1.

PEDOT:PSS Grade	PSS	PH500	PH1000
Thickness (nm)	95 ± 5	45 ± 5	65 ± 5
Sheet Resistance (Ω/sq)	~1.37 x10^5	~4.3 x10^2	~1.7 x10^2
Conductivity (S/cm)	~0.768	~520	~915

Table 3.1. Conductivities of different PEDOT: PSS grades, characterized using a four probe measurement system. Clevios PH500 and PH1000 were doped with 4 % Dimethyl Sulfoxide (DMSO). All films were spun at 1500 rpm for 30 seconds.

Typical hysteresis loops for 120 nm thick P(VDF-TrFE) films measured at a frequency of 10 Hz are shown in Fig. 3.2 (a). The figure shows well-saturated loops with a saturation polarization ($\pm P_s$) of 9 μC/cm^2 and remnant polarization ($\pm P_r$) of 7.4 μC/cm^2, indicating good crystallinity of the P(VDF-TrFE) film irrespective of the electrodes used. A significant and consistent increase in the positive and negative switching fields is observed for devices with bottom PEDOT: PSS electrodes, compared to metal electrodes. The unfavorable increase in coercive fields ($+E_c/-E_c$) is from [+58/−53] MV/m using metal electrodes to [+70/−65 MV/m] using PEDOT:PSS bottom electrodes. We

believe this can be attributed to the poor conductivity of the undoped PEDOT:PSS which leads to a large voltage drop across the unpatterned bottom electrode. The undoped and poorly conducting PEDOT:PSS film acts as a large resistor connected in series with the ferroelectric capacitor. This is also indicated by the AFM image of undoped PEDOT:PSS films shown above, which shows the presence of excess insulating PSS leading to resistor like behavior from these unpatterned films. The intrinsic coercive field of the ferroelectric film itself does not change. Instead, a higher voltage is needed to reach the required coercive field to switch the dipoles in the ferroelectric copolymer film. To further confirm this effect, we fabricated a device with bottom Pt electrodes and a thin interfacial layer of undoped PEDOT:PSS (~ 20 nm), referred to as Pt-PSS in all figures. The devices with an interfacial layer of undoped, poorly conducting PEDOT:PSS exhibit coercive fields of +58 MV/m and -50 MV/m, similar to devices with metal electrodes. This result confirms the fact that the apparent high coercive voltage measured in devices using undoped PEDOT:PSS as a standard electrode is not intrinsic. Instead, it is related to an extrinsic voltage drop due to the large resistance of the electrode. This result may also explain some of the high coercive voltages reported for P(VDF-TrFE) devices with polymer electrodes that have been reported in literature [12].

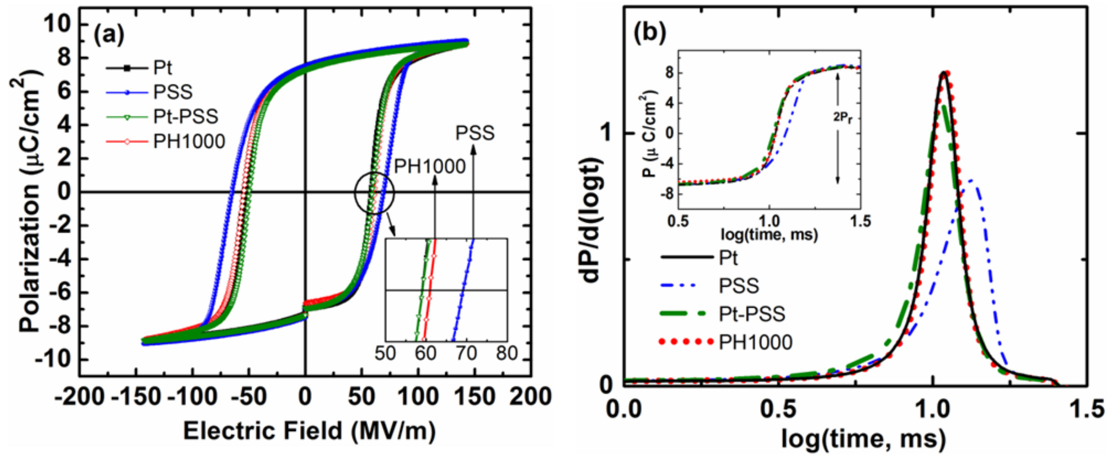

Figure. 3.2 (a) Polarization (P) vs Electric Field (E) hysteresis loop measurements at a frequency of 10 Hz. Inset shows a magnified image of coercive fields for devices with different bottom electrodes i.e. (b) Switching characteristics for ferroelectric capacitors at 120 MV/m, with peak of dP/d(log t) vs. log t representing respective switching times. Inset shows a switching event with sharp increase in polarization at corresponding switching times.

In parallel, we have fabricated devices with highly conducting, doped PEDOT:PSS electrodes. Devices with highly conducting, doped PEDOT:PSS electrodes displayed coercive fields similar to devices with metal electrodes (+60 MV/m and −54 MV/m). The presence of highly conducting network of PEDOT chains as seen from the AFM characterization shown above ensures minimal voltage drop across the unpatterned bottom electrode. This substantial improvement in coercive fields compared to the low-conductivity PEDOT:PSS suggests the possibility of using doped PEDOT:PSS for fabrication of low-voltage, transparent and flexible ferroelectric memory.

Switching characteristics of our P(VDF-TrFE) copolymer films are shown in Fig. 3.2 (b), which can be obtained by a time domain measurement of the charge density or polarization (P) response. As seen from the inset of Fig. 3.2 (b), polarization plotted against logarithmic time (log t) exhibits a rapidly increasing curve during dipole switching. Switching times (τ_s) are estimated from the time of the maximum of dP/d(logt) vs. log (t) plot [13]. At applied fields of 120 MV/m, devices with Pt electrodes exhibit switching times of 10.7 ms while devices with bottom PEDOT:PSS electrodes have increased switching times of 13.35 ms. This can be explained based on the dependence of switching time, τ_s on applied electric field [13], given by equation 3.1:

$$\tau_S = \tau_{S\infty}\, e^{E_a/E} \qquad (3.1)$$

where $\tau_{s\infty}$ is the limited switching time, E_a is the activation field and E is applied electric field. Thus, the switching time increases for lower applied fields in ferroelectric capacitors. For undoped (poorly conducting) PEDOT:PSS electrodes, the voltage drop across the bottom electrode leads to lower applied fields across the ferroelectric film, leading to increased switching times. However, devices with an interfacial layer of undoped PEDOT:PSS and doped PEDOT: PSS electrodes have lower switching times of ~ 10.7 ms, identical to devices with metal electrodes.

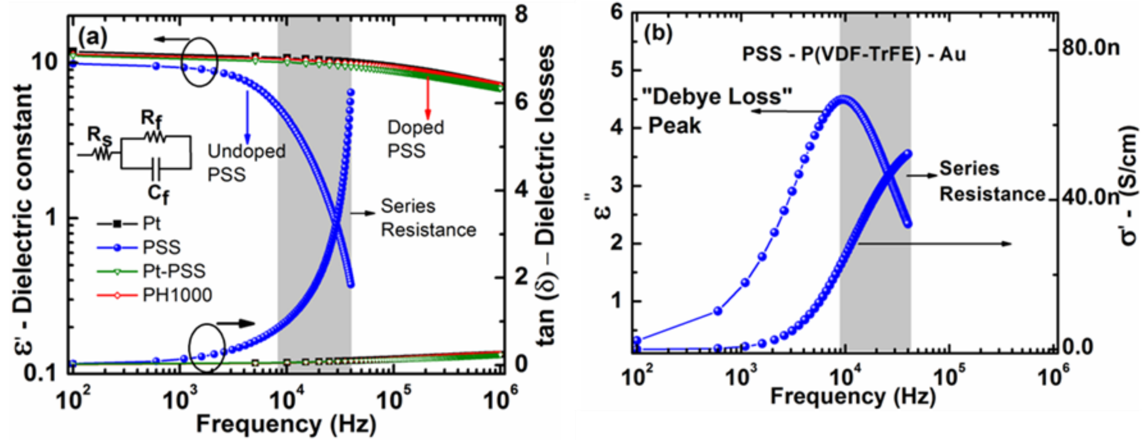

Figure. 3.3 (a) Dielectric spectroscopy study with dielectric constant (left axis) and dielectric losses (right axis) for all the devices studied. Equivalent circuit model is represented in the inset where R_s is series resistance from electrodes, R_f and C_f is resistance and capacitance of dielectric film, respectively. (b) Imaginary part of the complex permittivity (ε'') (left axis) indicating a "debye-loss" peak at ~ 7 kHz and conductivity (σ') (right axis) of the ferroelectric co-polymer with increasing frequency.

Fig. 3.3 (a) shows the dielectric dispersion and the loss factor (tan δ) of P(VDF-TrFE) ferroelectric capacitors. A decay of the dielectric constant is seen, consistent with the dielectric response of ferroelectric thin films [14-17]. Our P(VDF-TrFE) copolymer films exhibit a dielectric constants of ~ 11.5 at 100 Hz, comparable to other reports in literature [3]. Devices with Pt bottom electrodes have excellent dielectric performance even at a high frequency of 1 MHz, with a negligible drop in permittivity and low losses. Devices with poorly conducting PEDOT: PSS electrodes show a step-like decrease of the permittivity upto a frequency of ~ 7 kHz. This reduction is mainly caused due to loss of interfacial polarization at the dielectric-electrode interface, indicated by a peak in the imaginary part of the permittivity, ε'' (Fig. 3.3 b) resembling a Debye-like dipolar

relaxation process [15,18,19]. Further drop in the permittivity beyond 7 kHz can be attributed to the series resistance from the undoped PEDOT:PSS electrodes, absent in the devices with doped PEDOT:PSS bottom electrode. The dielectric response of ferroelectric capacitors can be represented with an equivalent circuit, consisting of a resistor in series with a parallel RC circuit [14,16]. The capacitor shows an RC time constant behavior determined by $\tau = R_sC_f$, where R_s is the series resistance from the electrode and C_f is the film capacitance. Higher series resistance from the electrodes indicates that the fall-off would occur at lower frequencies, which in our case is attributed to the poor conductivity of undoped PEDOT: PSS. This limits the use of poorly conducting PEDOT:PSS electrodes to low frequency applications.

Fig. 3.3 (a) also shows the dielectric losses (tan δ) calculated from the ratio of the imaginary and real part of the dielectric constant (Equation 3.2). For undoped, poorly conducting PEDOT: PSS electrodes, the increase in losses upto ~ 7 kHz can be contributed to an increase in the imaginary part of the permittivity, ε'' that is the Debye loss peak. Beyond this, the series resistance effect dominates manifested by a sharp increase in losses (Fig. 3.3 a) and the real part of conductivity (σ') (Fig. 3.2 (b)): [14,15]

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{\sigma'}{\varepsilon'\varepsilon_0\omega} \qquad (3.2)$$

More importantly, here we demonstrate that upon using highly conducting doped PEDOT:PSS electrodes, it is possible to get devices with excellent dielectric response and low losses up to 1 MHz, frequencies applicable to many basic logic and memory operations.

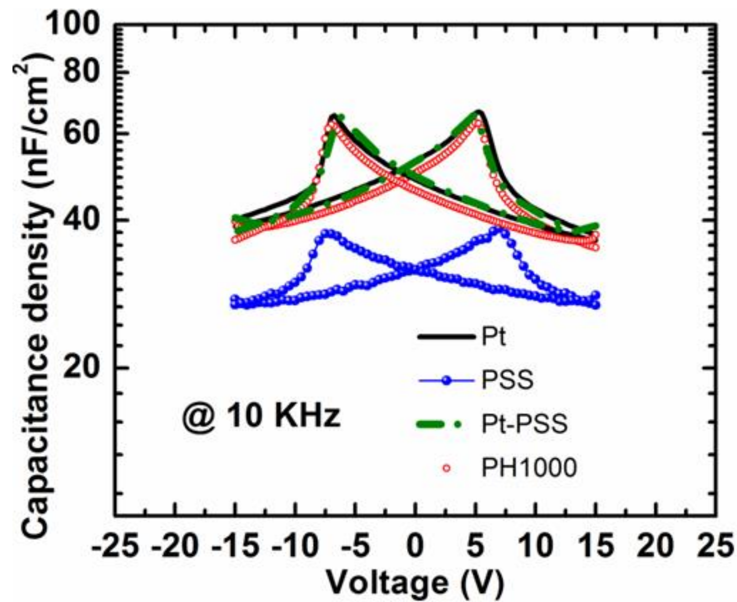

Figure. 3.4 Capacitance density plotted as a function of voltage from −15 to +15 V for different electrodes. The C-V (“butterfly”) curves were measured at 10 kHz.

Fig. 3.4 shows the small signal capacitance measured by superimposing a small AC electric field (50 mV, 10 KHz) over DC field sweep from −15 to +15 V. The characteristic “butterfly” shape of the C-V curve indicates ferroelectric switching phenomenon with the two peaks corresponding to dipole reversal. The 120 nm thick P(VDF-TrFE) films on metal electrodes display a peak capacitance of ~ 65 nF/cm^2. This is identical to devices with undoped interfacial PEDOT:PSS layer and doped highly

conducting PEDOT:PSS electrodes. In contrast, there is an approximate 40 % drop in capacitance density to ~ 37 nF/cm^2 upon using undoped PEDOT:PSS electrodes. The drop in capacitance confirms the series resistance effect, as discussed using dielectric spectroscopy in Fig. 3.3.

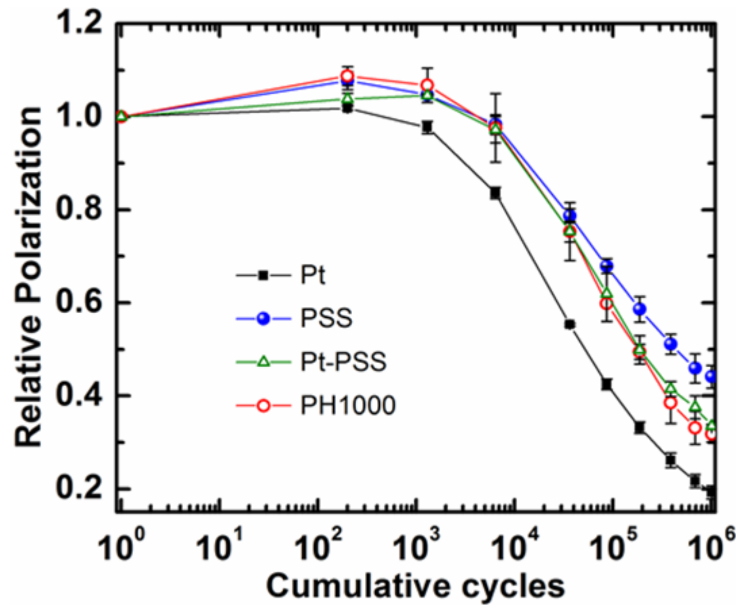

Figure. 3.5 Electrical fatigue properties showing relative polarization of P(VDF-TrFE) films stressed at 80 MV/m and a frequency of 100 Hz. The PUND measurements were done at saturation fields of 125 MV/m.

The fatigue behavior of ferroelectric capacitors with metal and polymer electrodes is compared in Fig. 3.5. A bipolar triangular waveform with amplitude of 10 V and 10 ms pulse width was applied during fatigue and the devices were characterized periodically with a Positive-Up-Negative-Down (PUND) measurement at 15 V at the same frequency. Devices with metal electrodes display significant fatigue with only 20 %

retention after 10^6 cycles. Fatigue in P(VDF-TrFE) is very sensitive to applied field and frequency of stress cycles, with increased fatigue at high field and low frequencies [20,21]. Fatigue performance of our devices with metal electrodes is consistent with other reports in literature at similar frequency [20,22]. Devices with bottom polymer electrodes show a slight improvement with 31 % and 44 % retention for highly and poorly conducting PEDOT: PSS electrodes, respectively. There have been various studies published on the effect of applied voltage profile, frequency, crystallinity and operating temperature on polarization fatigue, but most of these studies were done using metal electrodes on silicon substrates [21, 23, 24]. In contrast, there have been very limited reports on fatigue using polymer electrodes [12]. It has been proposed that fatigue in P(VDF-TrFE) film is related to the injection of charges from electrodes which are subsequently trapped at crystallite boundaries and defects, inhibiting ferroelectric switching and leading to higher fatigue rates [5,21]. Our fatigue data shows that after 10^5 cycles, devices with bottom Pt electrodes retain about 42 %, doped PEDOT:PSS devices retain 60 % while undoped PEDOT:PSS devices retain as much as 68 % of the initial polarization. We believe that the use of poorly conducting polymer electrodes reduces charge injection into the P(VDF-TrFE), resulting in less trapped charges, therefore lower fatigue rates. Thus it is evident that while the devices made from the undoped, poorly conducting PEDOT:PSS exhibit inferior performance, their fatigue characteristics are greatly improved. Based on the data, using doped PEDOT:PSS with high conductivity appears to be a promising material for use as local and global

interconnect in flexible, transparent electronics applications. It exhibits metal-like behavior and with improved fatigue retention properties.

4. Conclusions

In summary, we have demonstrated that by using highly conducting doped polymer electrodes (PEDOT:PSS with 4 % DMSO), we can fabricate ferroelectric devices with good polarization, low coercive fields, low dielectric losses, comparable to devices with metal electrodes. Furthermore we have shown the added advantage of using polymer electrodes, in the improved fatigue performance of ferroelectric capacitors. This is a major advancement in the performance and opens the possibility of fabricating all-polymer ferroelectric memory devices for plastic electronics.

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CHAPTER 4

Large Area Ink-Jet Printed All Polymer Ferroelectric Memory

Unnat S. Bhansali, M.A. Khan and H. N. Alshareef (Microelectronic Engineering 105 (2013) 68)

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Abstract

Drop-on-demand piezoelectric inkjet-printing technique has been used to fabricate a functional cross-bar array of all-organic ferroelectric memory devices. The devices consists of a ferroelectric copolymer P(VDF-TrFE) film sandwiched between inkjet-patterned, continuous, orthogonal lines of PEDOT:PSS polymer as the bottom and top electrodes. These devices exhibit well-saturated hysteresis curves with a maximum remnant polarization (P_r) = 6.7 μC/cm^2, coercive field (E_c)= 55 MV/m and a peak capacitance density of 45 nF/cm^2. The overall performance and polarization retention characteristics of these ferroelectric capacitors with inkjet-printed polymer electrodes are comparable to metal and spin-cast polymer electrodes suggesting their potential use in large-area flexible electronics.

Contribution of Author M.A. Khan:

Optimizing the ink jet printing process to print PEDOT:PSS electrodes.

1. Introduction

The tremendous growth of organic electronics in the last two decades has stimulated the use of drop-on demand inkjet-printing (IJP) for numerous applications such as organic electronic devices and components [1-6], nano-biosensors [7], ceramic component manufacture [8] etc. IJP is a material-conserving, cost-effective, high precision, non-contact deposition technique suitable for a wide variety of functional inks and substrates. Inkjet-printed metal nanoparticle inks and semiconducting polymers such as poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) have been extensively used as electrodes for polymer light emitting diodes, organic solar cells, organic transistors, capacitors and ferroelectric transistors [2,4-6,9,10]. Polymer/inorganic nanocomposites and polymer-fullerene blends have also been inkjet-printed for displays and solar cells applications [11,12]. While IJP's versatility seems attractive for flexible electronics, a lot of attention has to be paid toward formulating the ink to suit the application in mind. Ink viscosity, surface free energy, interaction at the drop-substrate interface and solvent stability are some of the key considerations [13,14]. Inkjet-printing polymer solutions with high molecular weight such as poly(vinylidenefluoride–trifluoroethylene) P(VDF-TrFE) is a challenging task mainly because of its non-Newtonian behavior causing tail elongation and satellite drops following droplet rupture. The viscoelastic properties of the polymer are thought to be due to the elastic stresses associated with the extensional flow in the nozzle [15]. However, Zhang et. al.[16] demonstrated inkjet-printed P(VDF-TrFE) microdots using a

mixed solvent system, consisting of a good solvent with low boiling point and a poor solvent with high boiling point on a hydrophobic surface.

In this paper, we demonstrate all-polymer ferroelectric capacitors using inkjet-printed PEDOT:PSS as bottom and top electrodes. The ink formulation and jetting conditions are optimized to obtain continuous lines of PEDOT:PSS electrodes sandwiching the spin-cast organic ferroelectric film. We have also characterized the performance and long-term reliability of the ferroelectric capacitors thus fabricated and found them comparable to devices with spin-coated polymer electrodes or conventionally deposited metal electrodes.

2. Experimental

The flexible and transparent substrate, ULTEM 1000B® (SABIC) was cleaned in an ultrasonicator with acetone and isopropanol followed by de-ionized (DI) water for 10 min. each, in that particular sequence. The semiconducting polymer, PEDOT:PSS (from Sigma Aldrich, 1.3 wt.% dispersion in water), was diluted with ethylene glycol (EG) and Dimethylsulfoxide (DMSO) in a 5:2:1 volume ratio, respectively, referred to as PEDOT:PSS ink hereafter. The ferroelectric copolymer P(VDF-TrFE) (70–30 mol%) obtained from Piezotech S.A, France was dissolved in anhydrous methyl ethyl ketone (MEK) at a concentration of 30 mg/mL and stirred overnight at room temperature inside a N_2 purged glove-box.

A Jetlab® II Precision Printing Platform (Microfab Technologies Inc.) was used for inkjet-printing PEDOT:PSS lines. The dispensing head consists of an ink reservoir, an integrated filter and a nozzle with a 60 µm orifice. The reservoir is filled with PEDOT:PSS ink filtered through a 0.45 µm PTFE syringe filter. The input voltage signal to the piezoelectric printhead was optimized in amplitude, rise/dwell times and frequency to consistently eject drops of diameter (55 µm), approximately similar to the nozzle orifice and a volume of ~ 90 pL at an average velocity of 1.2 m/s. The stage speed, drop-spacing and the base drop frequency were adjusted to 2 mm/s, 40 µm and 50 Hz, respectively, while the temperature of the substrate was fixed at 60 °C. The dimensions of the printed PEDOT:PSS lines are approximately 2 cm x 60 µm x 500 nm (length x width x thickness). The ferroelectric polymer P(VDF-TrFE) was spin-coated on top of the printed bottom electrodes, followed by a soft bake for 30 min at 80 °C. The films were then annealed in vacuum at 135 °C for 4 hours to obtain the ferroelectric β-phase. For the top electrodes, PEDOT:PSS lines were inkjet-printed orthogonal to the bottom electrodes, forming a cross-bar array of ferroelectric capacitors. The devices were finally annealed on a hot-pate at 80 °C for 30 min. prior to electrical characterization.

The 3D surface profile was taken using a Zygo white light interferometer system. The surface roughness (R_{rms}) of the substrate and printed lines was measured using an Atomic Force Microscope (AFM, Agilent 5400). The thickness of the ferroelectric layer and the PEDOT:PSS lines was measured by a Dektak Profilometer and verified by AFM.

The capacitors were characterized using a Premier Precision II ferroelectric tester (Radiant Technologies Inc.) and Keithley 4200 Semiconductor Parameter Analyzer.

3. Results and Discussion

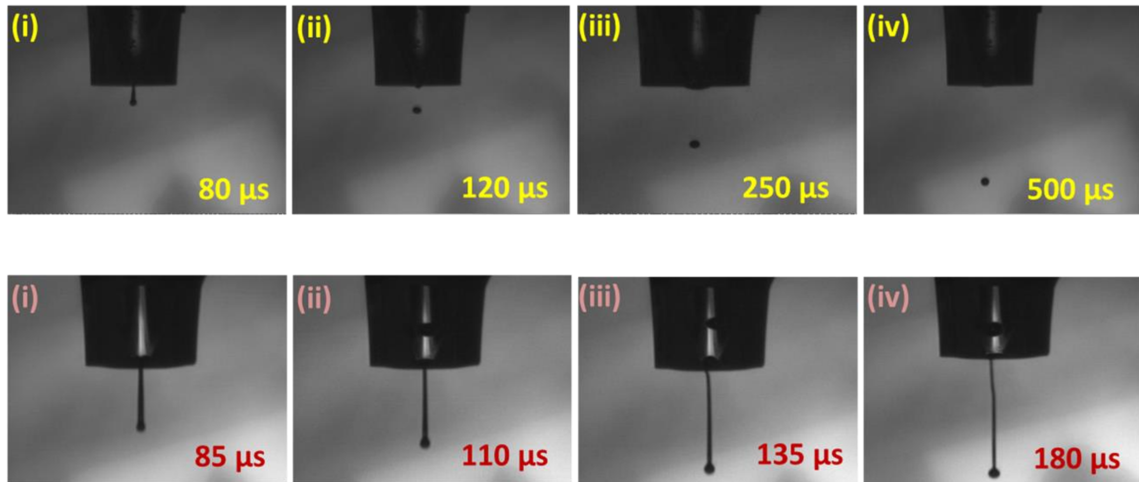

Figure. 4.1 Stroboscopic in-flight images of: PEDOT:PSS single-drop formation and release (top) and tail elongation of P(VDF-TrFE) and no break-off even after 180 μs.

A steady stream of single drops consistent in size, velocity and volume is essential for achieving well-defined printed features on any substrate. For an aqueous polymer dispersion such as PEDOT:PSS, the viscosity and surface tension can be adjusted through additives to obtain individual drops [6]. Fig. 4.1(top) (i-iv) shows a series of stroboscopic in-flight images of PEDOT:PSS drop formation and release at various time delays, captured by a CCD camera mounted in line with the nozzle. The

single drop ejection was also maintained at frequencies as low as 30 Hz, indicating good stability and jet reliability. P(VDF-TrFE) solution, on the other hand, behaves like a viscoelastic fluid that forms a droplet and a following tail or ligament that elongates before rupturing into multiple, small satellite drops at very high voltages. These drops could either merge with the leading drop in flight, prior to impact and form a huge drop with excess volume or form multiple stray drops resulting in poor definition of printed patterns. The drop elongation of P(VDF-TrFE) dissolved in Dimethylformamide (DMF) with a concentration of 10 mg/mL is shown in Fig. 4.1(bottom) (i-iv). Even at concentrations as low as 0.1 wt.%, the elongated tail would not break off at 40 V and this can be attributed to the high molecular weight and surface tension of the solution [17].

Fig. 4.2 (a) shows an optical microscope image of the printed columns of PEDOT:PSS lines on ULTEM 1000B substrates. The lines with smooth edges are obtained by optimizing the drop spacing, jetting frequency and the applied voltage signal. A typical voltage pulse with an amplitude of ± 22 V, rise/fall time = 3 µs, dwell time = 18 µs and a drop frequency = 600 Hz was applied to print uniform, continuous PEDOT:PSS lines, as illustrated in Fig. 4.2 (b).

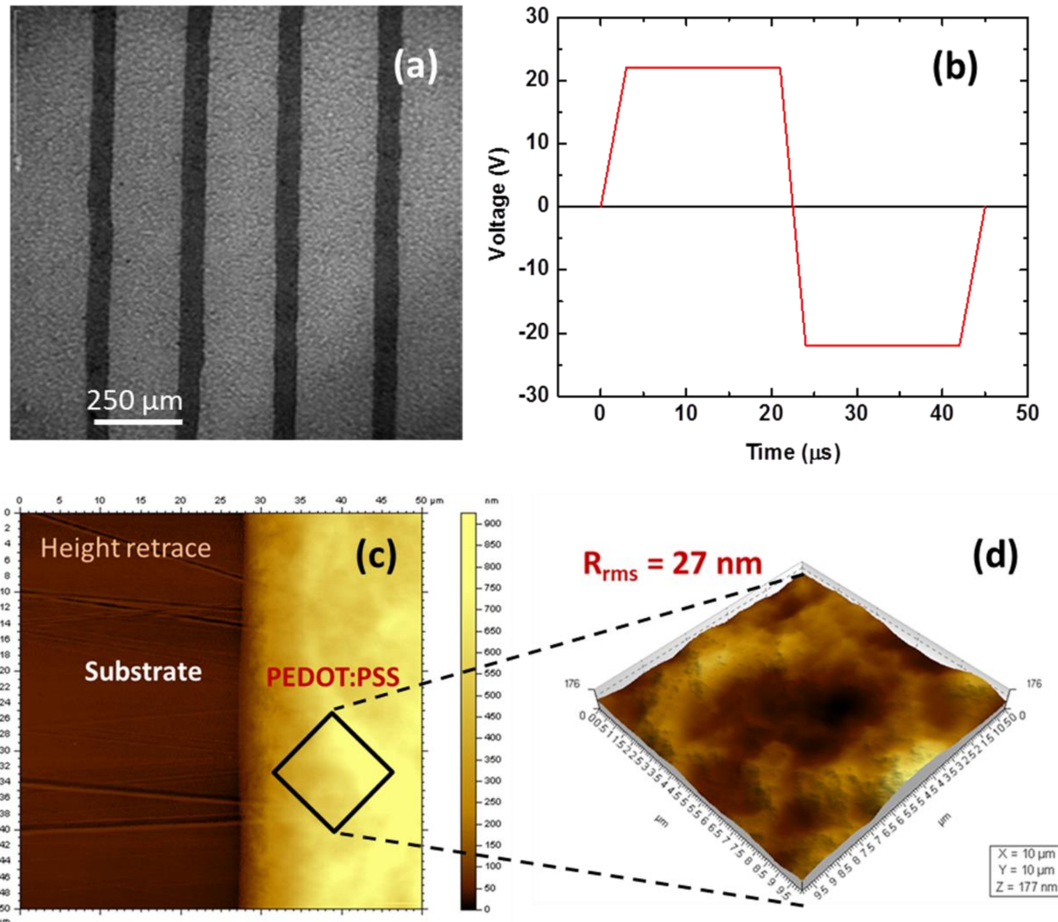

Figure. 4.2 (a) An optical microscope image of the printed PEDOT:PSS lines on plastic substrate. The pitch spacing is set at 250 µm. (b) A typical voltage pulse applied to the piezoelectric print head for stable ejection of PEDOT:PSS ink. (c) Height retrace AFM image showing the PEDOT:PSS line edge and (d) surface morphology of printed PEDOT:PSS features showing a roughness (R_{rms}) ~ 27 nm. The scan area is 10 µm x 10 µm.

At V > 25 V, satellite drops were observed causing stray-jetting which adversely affected the line definition. Fig. 4.2 (c) shows an AFM image of the printed PEDOT:PSS line edge on a plastic substrate. The step height measured across the PEDOT:PSS line was ~ 500 nm, consistent with the Dektak profiler measurement. The roughness value

(R_{rms} = 27 nm) measured by AFM over a 10 µm x 10 µm scan area, shown in Fig. 4.2 (d), is significantly higher compared to spin-coated films. This can be attributed to: (a) the high substrate temperatures ~ 60 °C causing solute movement and (b) overlapping of individual adjacent drops due to reduced drop spacing to form a continuous line.

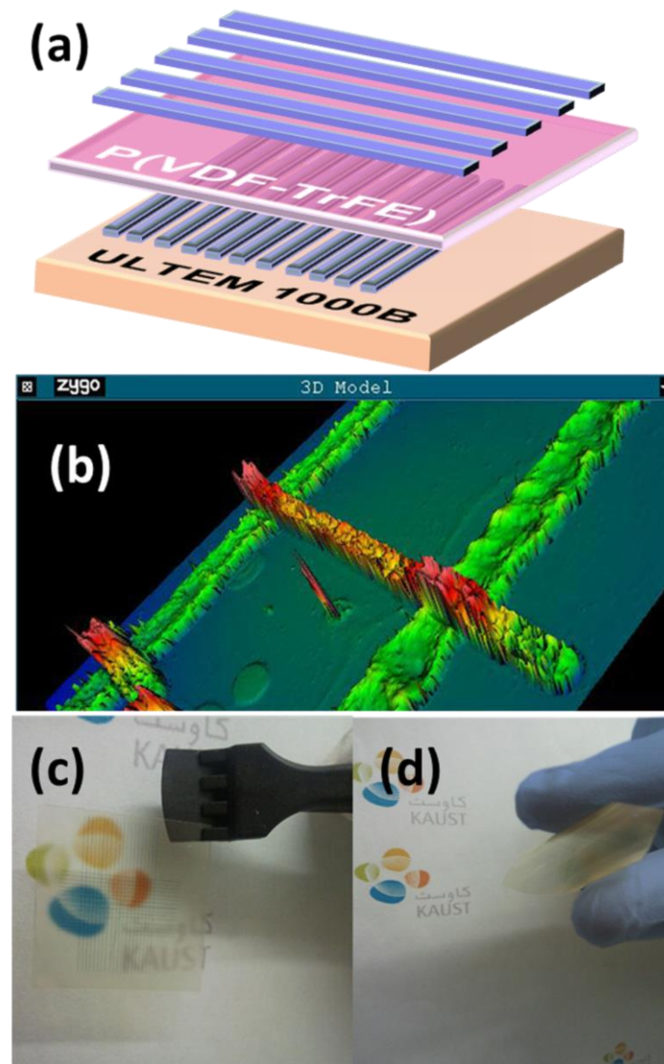

Figure. 4.3 (a) Schematic of the device structure showing a transparent substrate, orthogonal lines of inkjet-printed PEDOT:PSS and a spin-cast P(VDF-TrFE) layer, (b) a white light interferometry image of the device showing the concave profile of the inkjet-printed PEDOT:PSS lines. Photographs of the actual device on ULTEM 1000B where the transparency and flexibility can be discerned in (c) and (d), respectively.

An approximately 250 nm thick P(VDF-TrFE) layer was spin-coated from a 3 wt.% solution to prevent the electrical shorting of devices due to the high roughness of the underlying PEDOT:PSS electrodes. After annealing the ferroelectric layer, another set of PEDOT:PSS lines as top electrodes were inkjet-printed orthogonally to the bottom electrode. A schematic of the device is shown in Fig. 4.3 (a). A surface profile captured using a Zygo interferometer, is shown in Fig. 4.3 (b).

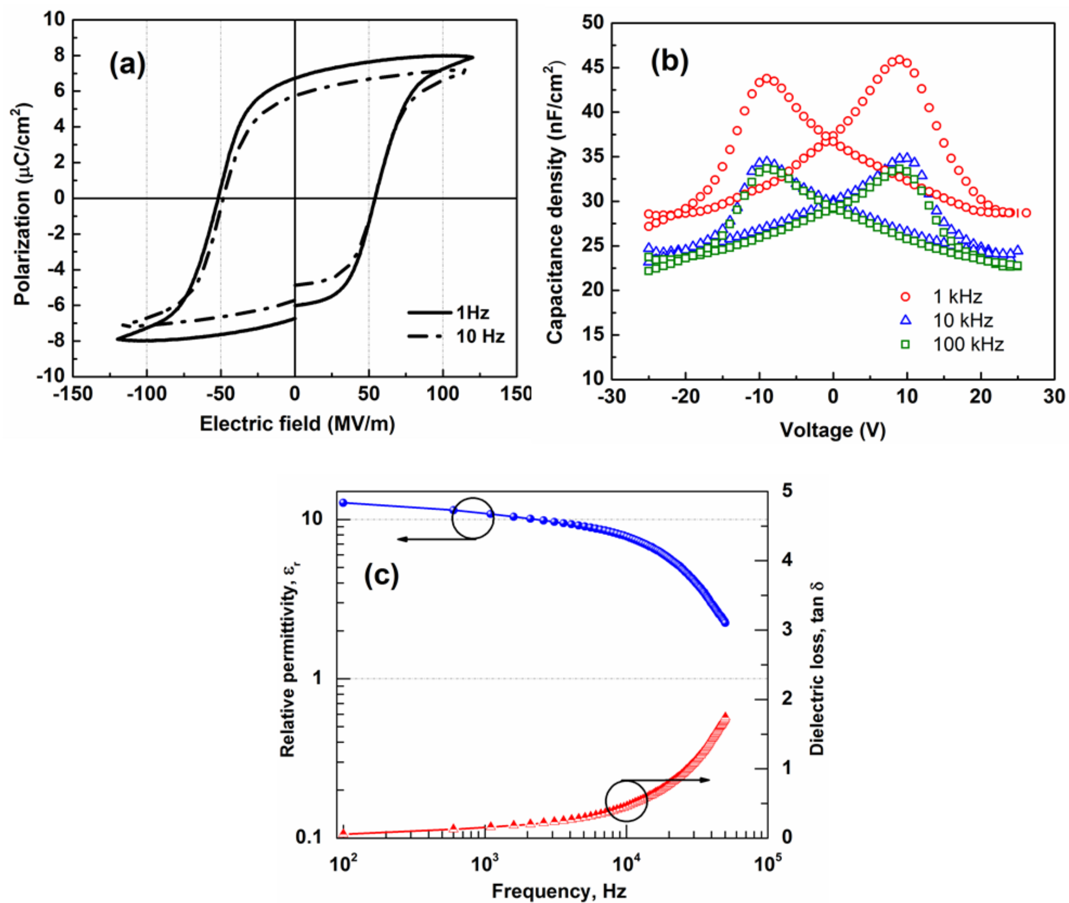

Figure. 4.4 (a) Hysteresis loops of ferroelectric capacitors measured at 1 Hz and 10 Hz under an electric field of 120 MV/m (b) Capacitance - Voltage curves measured for frequencies upto 100 kHz and (c) dielectric constant (left axis) and dielectric losses (right axis) measured at room temperature from 100 Hz to 50 kHz.

It can be clearly seen that the PEDOT:PSS lines have a concave profile when printed at high substrate temperatures. Soltman et. al.[18] obtained similar drop profiles for PEDOT:PSS at substrate temperature, ~ 60 °C. This can be explained based on the “coffee-ring effect” which occurs due to a combination of increased solvent evaporation rate at the edges of a droplet and contact line pinning due to solute deposition [19,20]. A capillary-driven flow from the center of the drop towards the edges compensates for the evaporative losses and transports solute toward the contact line, causing a concave profile. An actual photograph of devices on plastic substrate illustrating the transparency and flexibility is shown in Figs. 4.3 (c) and (d) respectively.

Well-saturated and symmetric hysteresis curves for a P(VDF-TrFE) film on inkjet-printed PEDOT:PSS bottom electrodes, measured at 1 Hz and 10 Hz for a virgin device are shown in Fig. 4.4(a). The ferroelectric capacitors exhibit remanent polarization (P_r) and an average low coercive field (E_c) ~ 6.5 μC/cm^2 and 55 MV/m, respectively. The low coercive fields could be attributed to the increased conductivity of the printed PEDOT:PSS electrode by addition of a high boiling-point solvent such as DMSO [21]. Addition of DMSO also improves the wetting properties and interfacial stability of the electrode with the dielectric [9]. The ferroelectric behavior of these devices is further confirmed by the Capacitance-Voltage (C-V) or the “butterfly” curves measured up to 100 kHz. Fig. 4.4 (b) shows the peak capacitance density ~45 nF/cm^2 measured at 1 kHz which drops to ~35 nF/cm^2 at 100 kHz. These values are slightly lower compared to metal electrodes but comparable to other spin-cast polymer electrodes such as

Polyaniline (PANI) or Polypyrrole (Ppy) [22]. The dielectric constant (ε_r) and losses (tan δ) measured at room temperature are 12.7 and 0.05, respectively, at 100 Hz. Fig. 4.4 (c) shows a plot of relative permittivity and dielectric losses vs. frequency for these devices at room temperature. The drop in the dielectric constant to 7.8 and 2.2 at 10 kHz and 50 kHz, respectively, could be attributed to the high series resistance across the electrode. This problem can be alleviated by increasing the conductivity of PEDOT:PSS inks [23]. Nonetheless, our values are comparable to other reported devices with spin-cast polymer or metal electrodes for similar P(VDF-TrFE) thicknesses.

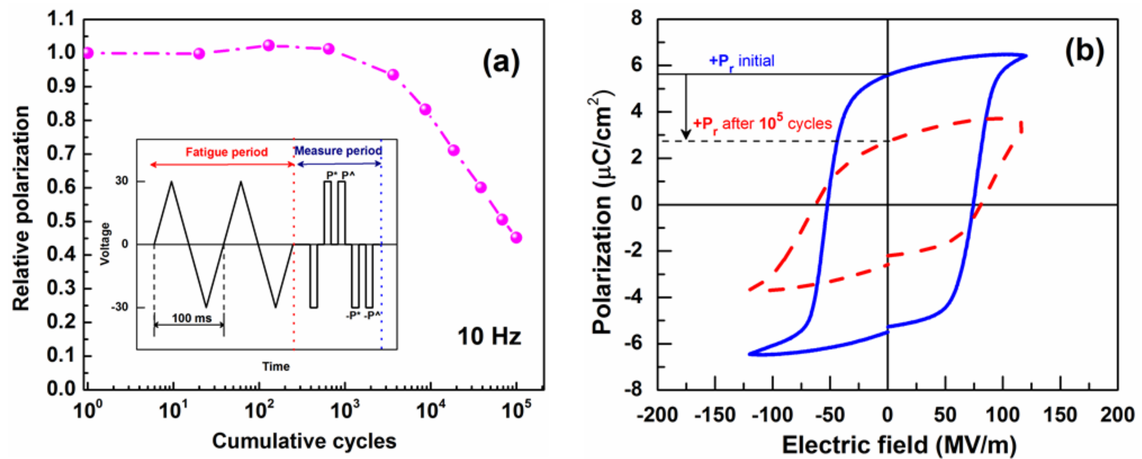

Figure. 4.5 (a) Normalized fatigue behavior for inkjet-printed PEDOT:PSS electrode capacitors showing dP (=P*− P^) vs. frequency, where P* is the (remanent + non-remanent polarization) and P^ is the non-remanent polarization from a PUND measurement. The devices were stressed at a switching frequency of 10 Hz and 120 MV/m. Inset shows the voltage profile and the measurement protocol used for this study and (b) a comparison of hysteresis curves before and after electrical fatigue, indicating that P_r drops to 45% of the initial value.

For organic ferroelectric capacitors to be used in non-volatile memory applications, it is important that they have long operational lifetime. The long-term device reliability is determined by polarization fatigue and data retention. Polarization fatigue is defined as the reduction in the amount of remanent polarization (P_r) with repeated switching or usage cycles. The fatigue behavior of devices with inkjet-printed bottom and top PEDOT:PSS electrodes is shown in Fig. 4.5 (a). The devices are stressed at a frequency of 10 Hz and ± 30 V which corresponds to an electric field ~ 120 MV/m, high enough to cause dipole switching in every fatigue cycle, followed by a Positive-Up-Negative-Down (PUND) measurement with a 10 ms pulse width. The inset of Fig. 4.5(a) demonstrates the voltage profile for the fatigue and PUND measurement used in this study. It can be seen from Fig. 4.5 (a) that after 10^5 cycles, P(VDF-TrFE) capacitors retain ~45% of the initial polarization. This is consistent with the drop in the remanent polarization seen from the polarization loops measured at 10 Hz before and after fatigue, shown in Fig. 4.5 (b). These data are consistent with previously reported fatigue behavior of spin-coated PEDOT:PSS bottom and top electrodes [24]. There is only a slight increase in the coercive field (<10%) which can be attributed to the defects caused by charge injection in the ferroelectric film. An internal electric field created by the trapped charges acts opposite to the external electric field, causing an apparent increase in the switching voltage for the ferroelectric domains in P(VDF-TrFE).

4. Conclusions

In summary, we have demonstrated functional cross-bar arrays of polymer ferroelectric capacitors with inkjet-printed polymer electrodes on flexible and transparent substrates. Uniform, continuous lines of PEDOT:PSS as electrodes were inkjet-printed by optimizing the substrate, ink formulation and jetting conditions. We have also shown that the inkjet-printed devices exhibit comparable remanent polarization, low coercive fields, low frequency dispersion and fatigue behavior similar to spin-cast PEDOT:PSS electrodes. Our results suggest that inkjet-printing is a useful technique to fabricate ferroelectric capacitors on flexible substrates without compromising performance and reliability.

CHAPTER 4 REFERENCES

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CHAPTER 5

Characterization of Current Transport in Polymer Ferroelectric Devices

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Abstract

In this chapter we report the charge injection characteristics in P(VDF-TrFE), as a function of the electrode. Symmetric and asymmetric devices with Al, Ag, Au and Pt electrodes were fabricated to determine the dominant carrier type, injection current density, and to propose transport mechanisms in the ferroelectric polymer. Higher work function metals such as Pt are found to inject less charges compared to lower work function metals, implying n-type conduction behavior for P(VDF-TrFE) with electrons as the dominant injected carrier. Two distinct charge transport regimes were identified in the P(VDF-TrFE) devices; a Schottky-limited conduction regime for low to intermediate fields ($E< 20$ MV/m), and a Space-charge limited conduction (SCLC) regime for high fields ($20<E<120$ MV/m).

Contribution of Author M.A. Khan:

Fabrication of the capacitors and characterizing the morphology of P(VDF-TrFE) thin films.

1. Introduction

P(VDF-TrFE) is a promising material for flexible organic non-volatile memory applications [1]. Nonvolatile ferroelectric random access memories' (FRAM) operation is based on the polarization reversal of electric dipoles in this polymer by an external applied electric field. The computational "0" and "1" are represented by the nonvolatile storage of negative or positive remnant polarization state, respectively, in the polymer material. Reading of the memory state is done by measuring the current through the ferroelectric material, which exhibits either a high conductance state or a low conductance state [2]. Despite easy operation and fabrication, the two major problems facing this type of memory are (a) polarization fatigue, defined as the reduction or the loss of remnant polarization under electric field cycling and (b) data retention. Both of these phenomena determine the long-term reliability of memory devices and are known to be affected mainly by two factors: (i) the depolarization field inside the film and (ii) the charge injection into the film [3]. Hence, it becomes critically important to identify and thoroughly understand the charge injection and transport mechanisms in these polymer ferroelectric thin films.

For inorganic ferroelectrics such as $Pb(Zr_x,Ti_{1-x})O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT), polarization fatigue is a well-studied phenomenon believed to depend strongly on charge injection into the ferroelectric film [4,5]. However, in the case of organic ferroelectrics such as P(VDF-TrFE), charge transport and the role of charge injection in device performance has not been thoroughly characterized. Bihler et al. reported that

charge injection and trapping at polarized crystallite surfaces is essential to stabilize the remnant polarization [6], but no comments were made on the fatigue performance due to charge injection. Xia et al. reported that charge injection in P(VDF-TrFE) is interface-controlled and a Schottky barrier forms at the metal-polymer interface [7]. He also reported that higher work function metals have lower injection barrier compared to lower work function metals, suggesting a p-type behavior for charge transport. Other reports in the literature have also suggested Schottky emission as the limiting leakage mechanism in P(VDF-TrFE) capacitors [8]. However, our data suggests n-type transport behavior in P(VDF-TrFE) thin films contrary to what has been reported earlier by Xia et al.[7]. Clearly, there seems to be a lack of complete characterization of the leakage behavior, charge injection and transport mechanisms in P(VDF-TrFE), specifically as a function of electrodes and temperature. Therefore, we have conducted a detailed study to characterize the leakage current behavior of P(VDF-TrFE) films sandwiched between electrodes of similar or dissimilar work functions, and propose charge transport mechanisms in P(VDF-TrFE) over a range of conditions.

2. Experimental

Prior to fabrication, Si substrates coated with 100 nm SiO_2 were cleaned by ultra-sonication in acetone, isopropanol and de-ionized (DI) water for 10 minutes each. The substrates were then cleaned in Oxygen plasma for 5 min. prior to depositing the bottom electrode. Bottom Au and Ag electrodes, ~ 100 nm thick were deposited by

thermal evaporation. The P(VDF-TrFE) (70–30 mol.%) was dissolved in anhydrous methyl ethyl ketone (MEK) at a concentration of 30 mg/mL to get a 3 wt.% solution. Thin films of P(VDF-TrFE) were spin-coated on all substrates at 6000 rpm for 60 secs and baked on a hotplate at 80 °C for 30 minutes followed by annealing in vacuum at 140 °C for 4 hours. The samples were allowed to cool down in vacuum to room temperature to facilitate the ferroelectric β phase growth. The thickness of the films was measured to be 200 + 10 nm, using a Dektak profilometer. Top Au, Ag and Al electrodes were deposited by thermal evaporation through a shadow mask. The electrical characterization was done using the Keithley 4200 Semiconductor Parameter Analyzer. The temperature-dependent current-voltage (I-V) characteristics of the devices were measured by heating the sample holder from 25-65 ^{o}C. All the I-V data shown represent averages of five devices of similar area. The I-V curves are reported after two initial sweeps, to make sure that steady state I-V curves are obtained.

3. Results and Discussion

Fig. 5.1 (a) and (b) show a schematic of the device structures used in this study with symmetric top and bottom metal electrodes, Ag and Au, respectively. The naming convention followed throughout this paper for any device structure is: Top electrode (TE)/P(VDF-TrFE)/Bottom electrode (BE). The plot in Fig. 5.1 (c) shows symmetric current density-electric field (J-E) curves for devices with Ag/P(VDF-TrFE)/Ag and Au/P(VDF-TrFE)/Au structure. It can be seen that the leakage current density for devices with Ag

as the top/bottom electrode at any given electric field is higher compared to Au electrodes, indicating a lower injection barrier for the lower work function Ag contacts to P(VDF-TrFE).

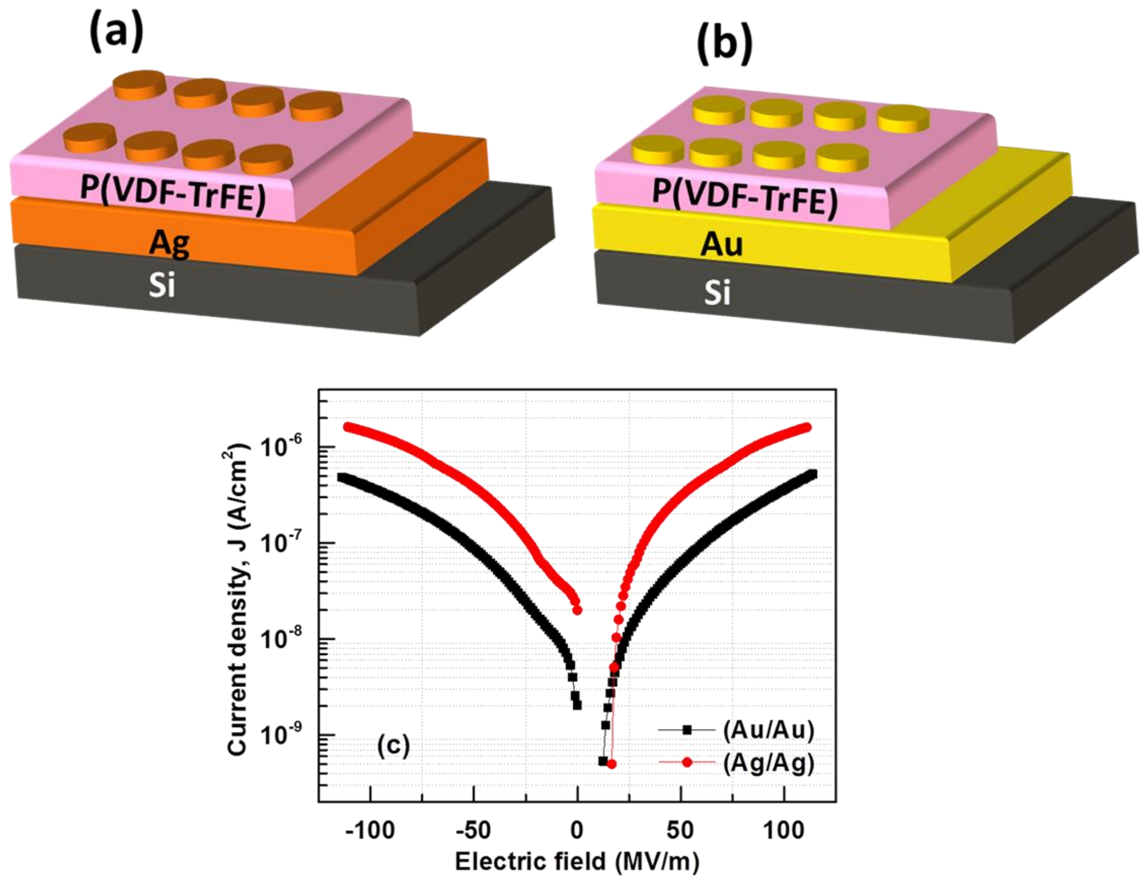

Figure. 5.1 A schematic of devices with symmetric electrodes, (a) Ag and (b) Au, as top and bottom metal contacts to P(VDF-TrFE) used for this study and (c) J-E curves for metal-ferroelectric-metal structures with Ag and Au top/bottom electrodes.

A schematic of the proposed band diagram for our devices, assuming β-phase P(VDF-TrFE) has a band gap of 7.7 eV and electron affinity of ≈ 4 eV, based on a density functional theory (DFT) study [9] is shown in Fig. 5.2(a). Previously reported work function values of 5.6, 5.1, 4.25 and 4.1 eV for Pt, Au, Ag and Al metals, respectively [10,11] are also indicated.

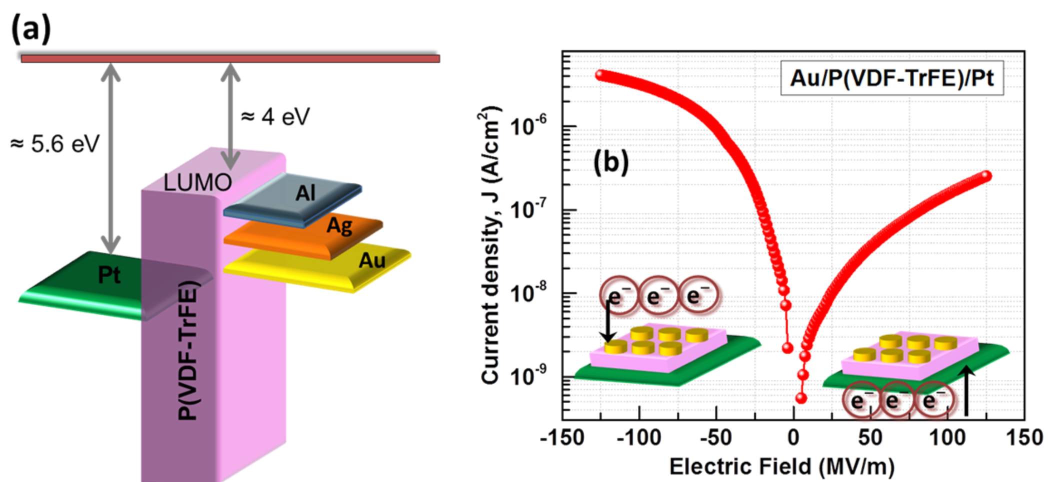

Figure. 5.2 (a) Proposed band diagram with the P(VDF-TrFE) energy levels and the work functions of metals used in this study w.r.t. vacuum. (b) Typical J-E plot of a Au/P(VDF-TrFE)/Pt device showing higher leakage when injecting electrons from Au (negative bias) compared to Pt (positive bias). The insets show the direction of electron injection corresponding to the polarity.

The J-E curves, shown in Fig. 5.1 (c) and the proposed band diagram suggest that conduction occurs through the Lowest Unoccupied Molecular level (LUMO) of P(VDF-TrFE) and that the leakage is interface-limited by an energy barrier that exists between the Fermi level of the metal and the LUMO level of the copolymer. The energy barrier is higher for the higher work function metal (Au) compared to the lower work function

metal (Ag). This interface-limited leakage current behavior was confirmed in the J-E plot of (Au/P(VDF-TrFE)/Pt) device shown in Fig. 5.2 (b), where the leakage current measured for positively biased Au top electrode is almost an order of magnitude lower than when it is negatively biased (here bias is defined with respect to the bottom Pt electrode), consistent with J-E characteristics of thinner P(VDF-TrFE) films [12,13]. The insets in Fig. 5.2 (b) show the device cross section with arrows indicating the direction of electron injection for both positive and negative bias applied to the Au electrode. These results indicate that an n-type conduction behavior occurs in P(VDF-TrFE) and that electrons are the dominant type of injected charges, consistent with previous report in the literature for 70-30 mol. % P(VDF-TrFE) films [14].

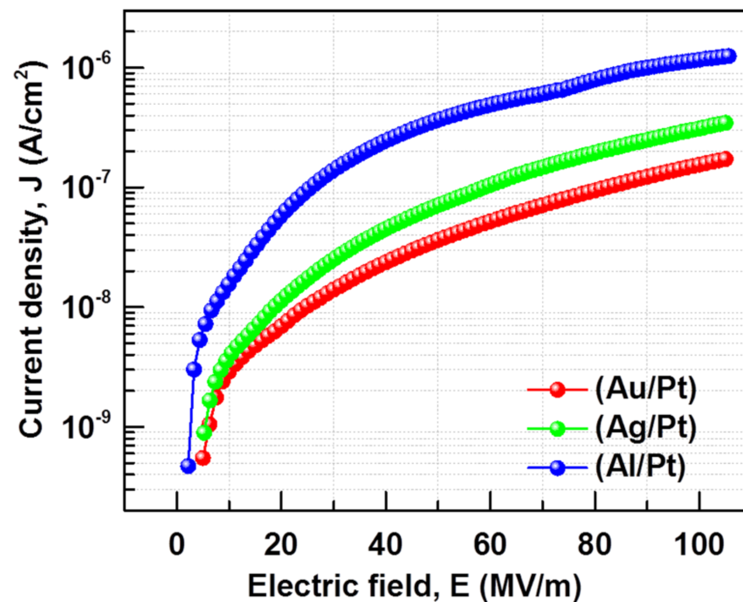

Figure. 5.3 J-E plots for asymmetric devices showing highest leakage current for Al/(P(VDF)-TrFE)/Pt compared to Ag/(P(VDF)-TrFE)/Pt and Au/(P(VDF)-TrFE)/Pt.

Fig. 5.3 shows a comparison of leakage behavior between asymmetric devices based on electron injection from a high work function bottom electrode, Pt, into different top electrodes such as Au, Ag and Al. The current density at any given electric field is the highest for devices with Al top electrode and least for Au electrodes. This can be attributed to a smaller band offset between Al and the LUMO level of the β-phase P(VDF-TrFE) which enhances carrier collection at the top electrode. This explanation is based on the assumption that the charge transport occurs primarily through the ferroelectric β-phase.

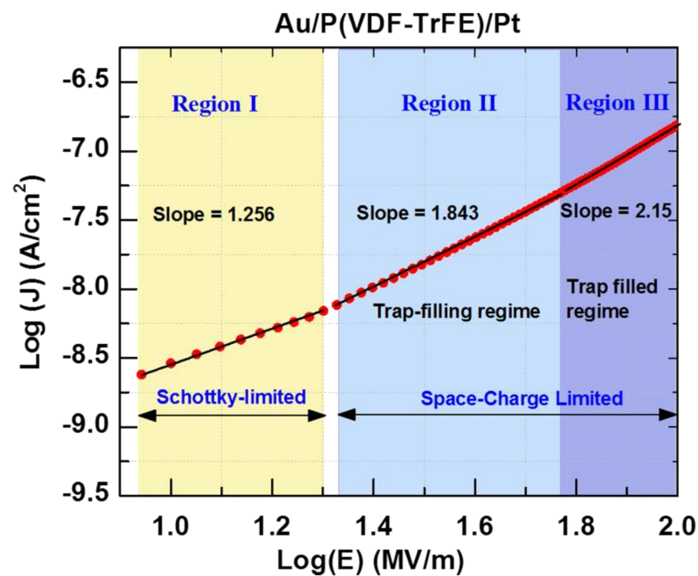

Figure. 5.4 A log-log plot of the J-E curve for Au/(P(VDF)-TrFE)/Pt device. Three regions with distinct slopes indicating different transport mechanisms are depicted. The slope values are calculated from a linear fit to the J-E curve and the adjusted R2 values are > 0.993.

For a clear understanding of charge transport mechanisms in P(VDF-TrFE), a representative log-log plot of the leakage current density versus electric field (J-E) curve for a Au/P(VDF-TrFE)/Pt device will be discussed in detail. The low field region starting from 0 to 8 MV/m (corresponding to 0.9 MV/m on the log x-axis) was excluded in this study since the data were very noisy.

Fig. 5.4 shows a region with a slope of 1.25 that extends from about 9 to 20 MV/m, corresponding to 0.9 - 1.3 MV/m on the log scale, defined here as region I. A linear relationship between log (current density) and log (voltage) suggests a possible Ohmic conduction as the transport mechanism in this regime. Although it is tempting to assume that Ohmic behavior dominates here since the slope of the log-log plot is close to 1, we found that the magnitude of the leakage current depends strongly on the work function value of the top metal electrode, ruling out the possibility of Ohmic conduction. Instead, an injection-limited transport mechanism that controls the leakage current levels in this regime such as Schottky-limited conduction is more likely, keeping in mind that P(VDF-TrFE) is a large band gap insulator and expected to form a Schottky contact with the used metals, as illustrated in Fig. 5.2 (a). The field dependence of Schottky-limited conduction current density, J, is expressed in equation (5.1) [15]:

$$J = A\,T^2 \exp\left[\frac{-q\left(\Phi_{b-}\sqrt{\dfrac{q\,E}{4\,\pi\,\varepsilon_i}}\right)}{KT}\right] \quad (5.1)$$

where, J is the current density, A is Richardson's constant, T is the absolute temperature in K, Φ_b is the injection barrier height, K is the Boltzmann constant, ε_i is dielectric

constant of the material, and $\varepsilon_i = \varepsilon_o \varepsilon_r$, where ε_o is the permittivity of free space, and ε_r is the relative permittivity of P(VDF-TrFE), E is electric field applied across the sample and q is the electron charge.

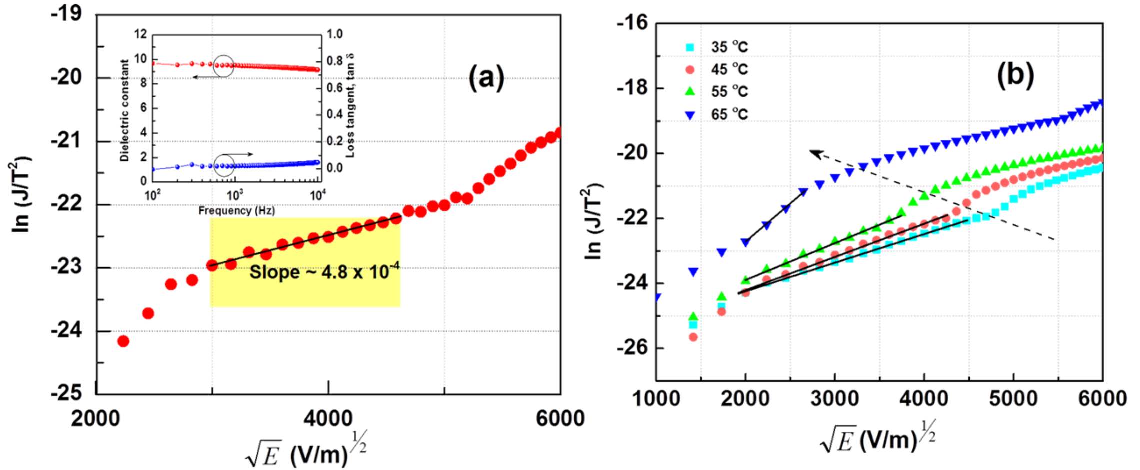

Figure. 5.5 (a) A plot of ln J/T^2 vs. √E for a Au/(P(VDF)-TrFE)/Pt device measured at room temperature. Inset shows the measured experimental relative permittivity and dielectric losses as a function of frequency. (b) Temperature dependent current-voltage dependence of Au/P(VDF-TrFE)/Pt device from T=25 - 65 °C. The direction of the arrow indicates a reducing electric field for the onset of the SCLC transport behavior.

Based on equation 5.1, the slope of ln (J/T^2) vs. √E curve can be represented by equation 5.2 and for the case of Schottky-limited conduction, a linear relationship is expected if one makes a plot of ln (J/T^2) vs. √E. Fig. 5.5a shows a ln (J/T^2) vs. √E curve for a Au/P(VDF-TrFE)/Pt device at T= 25 °C exhibiting a linear fit in Region I (corresponding to 3000 – 4472 $V/m^{1/2}$) and the slope is approximately ~ 4.8 x 10^{-4}. The calculated relative permittivity of P(VDF-TrFE) thin film using this slope value in equation 5.2 was

determined to be ~ 9, comparable to the experimental values measured by dielectric spectroscopy, shown as an inset of Fig. 5.5(a). A good correlation between the measured and calculated values of relative permittivity leads us to believe that charge transport in Region I can be attributed to a Schottky-limited mechanism. For Schottky-limited conduction, the slope of ln (J/T^2) vs √E should be equal to:

$$Slope = \frac{(\frac{q^3}{4\pi\ \varepsilon_o \varepsilon_r})^{\frac{1}{2}}}{KT} \quad (5.2)$$

To further confirm the Schottky-limited carrier transport mechanism in Region I, the I-V behavior of these devices was measured as a function of increasing temperature from 25 °C to 65 °C at 10 °C intervals, as shown in Fig. 5.5(b). The dielectric constant calculated from the current-voltage-temperature dependence was similar to experimentally measured values. Linear fits for the ln (J/T^2) vs. √E relationship were also found for the rest of the temperatures in Region I, indicating a Schottky-limited transport behavior. It should also be noticed that the electric field at which the Schottky-limited transport regime ends monotonically decreases as the temperature is increased, marked by the arrow in Fig. 5.5(b). This is also consistent with the Schottky-limited injection mechanism behavior where carriers can be excited over the energy barrier at lower fields because of the externally applied higher thermal energy.

The Au/P(VDF-TrFE)/Pt device exhibits regions with slope values 1.84 and 2.15 in the high field regime (E>20 MV/m) (labeled as Regions II and III on Fig. 5.4), which can

be attributed to the trap-filling and traps-filled-limit transport phenomena, respectively. Slope values between 1 and 2 are characteristic of the trap-filling region for an insulator with shallow traps, followed by a region with slope values of ≥ 2 representing the traps-filled limit behavior or the trap-free square law dependence [16].

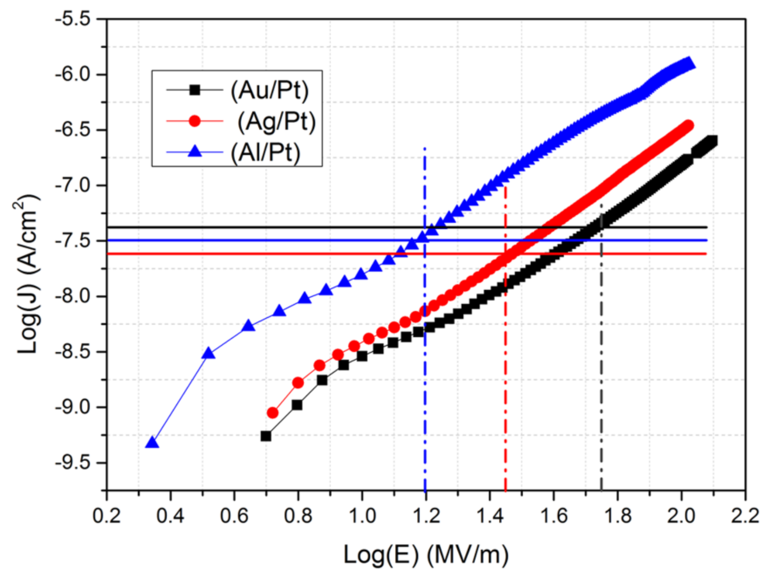

Figure. 5.6 Log (J) vs. Log (E) plots for Au/P(VDF-TrFE)/Pt, Ag/(P(VDF-TrFE)/Pt and Al/(P(VDF-TrFE)/Pt devices. The field values at which the slope of the J-E curve is ≥ 2 are marked as x-axis intercepts and the current density ≈ 3×10^{-8} A/cm^2, indicating bulk-limited SCLC transport.

Space-charge limited conduction (SCLC) transport mechanism commonly occurs in insulators with extremely low intrinsic carrier concentration, such as P(VDF-TrFE), which is known to be a wide band-gap insulator. SCLC mechanism also assumes one of the contacts to be Ohmic [17]. We have observed SCLC behavior in our devices beyond

the Schottky-limited regime (Region I) where the current is expected to be non-injection limited, as shown in the log (J) - log (E) plots of devices with Au, Ag and Al as the top electrode metal and Pt as the bottom electrode metal in Fig. 5.6. The trap-filling region (Region II) and the traps-filled limit regime (Region III) for Al/Pt device was observed at much lower field values compared to Au/Pt and Ag/Pt, which can be attributed to a lower Schottky barrier for Al into the LUMO (Lowest Unoccupied Molecular Orbital) of P(VDF-TrFE), as illustrated in Fig. 5.2(a). Furthermore, SCLC is a bulk-limited transport mechanism and hence the current density at the traps-filled limit field should be independent of the electrode metal [18]. For all the devices shown in Fig. 5.6, we observed that the field at which the slope of the J-E curve is > 2 for Au/Pt, Ag/Pt and Al/Pt electrodes are 59 MV/m, 28 MV/m and 16 MV/m, respectively. It is also observed that all these field values correspond to a current density of ≈ 3×10^{-8} A/cm^2 (−7.5 A/cm^2 in the log-scale), beyond which we observe a trap-free square law dependence, described by the following relationship.

$$J = \frac{9\varepsilon\mu V^2}{8L^3} \qquad (5.3)$$

where J is the current density, ε is the permittivity of the material, μ is the mobility of the dominant carrier, and L is the thickness of the dielectric film. As for the trap-filling region, the slope value 1.84 is characteristic of the trap-filling region for an insulator with shallow traps as the slope value would be between 1 and 2. This is in contrast to insulators with deep trap energy levels, where transition from the trap-filling to the trap-filled regions is much steeper giving rise to higher slope values [16,18,19]. This

behavior confirms the presence of bulk-limited SCLC transport mechanism in P(VDF-TrFE) capacitors modeled as an insulator with shallow trap levels. So, our data strongly suggest the presence of SCLC behavior in P(VDF-TrFE) metal-ferroelectric-metal capacitors at high fields with distinct regions for trap-filling and trap-filled limit conduction mechanisms.

4. Conclusions

In summary, we have performed detailed analysis of the electrical transport mechanism in thin films of the ferroelectric copolymer, P(VDF-TrFE). The lower work function metals as top electrodes have a lower energy barrier and hence the highest leakage current density, suggesting a n-type behavior of P(VDF-TrFE) in metal-ferroelectric-metal capacitor structures. Two distinct transport regimes were identified through the current density- electric field plots. At fields below 20 MV/m, the transport is mainly Schottky limited by barriers at the metal/ferroelectric interface. In contrast, at higher fields (E>20 MV/m) space-charge-limited current (SCLC) conduction dominates.

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CHAPTER 6

Electrodes Engineering to Fabricate Fatigue Free Polymeric Ferroelectric Memory

Unnat S. Bhansali, M.A. Khan and H. N. Alshareef (Organic Electronics 13 (2012) 1541)

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Abstract

Fully transparent and flexible ferroelectric capacitors have been fabricated using a transparent conducting oxide (ITO) and a transparent conducting polymer (PEDOT:PSS). By understanding the charge injection mechanism and by appropriate electrode engineering we were able to fabricate capacitors with tremendous improvement in fatigue. It is found that the polarization fatigue performance with transparent oxide electrodes exhibits a significant improvement over the polymer electrodes (20% vs 70% drop in polarization after 10^6 cycles). This result can be explained based on a charge injection model that is controlled by interfacial band-offsets, and subsequent pinning of ferroelectric domain walls by the injected carriers.

Contribution of Author M.A. Khan:

Characterization of the fatigue performance of the devices and measuring the curie temperature of the P(VDF-TrFE) as function of electrode.

1. Introduction

The flexible electronics industry is experiencing significant growth especially in the use of organic electronic materials including small molecules and polymers. One of the potential applications of such multifunctional polymers is ferroelectric non-volatile random access memories using the copolymer poly(vinylidene-fluoride-trifluoroethylene) or P(VDF-TrFE) [1]. Several properties of P(VDF-TrFE) make it nearly an ideal polymer non-volatile memory compared to other types of reported organic ferroelectric materials [2-5]. These include ease of device fabrication using solution processing, nonvolatility, sufficiently large remanent polarization, fast switching speeds, and thermal stability. Several reports on high performance, spin-cast films of P(VDF-TrFE) have been demonstrated, [1,6,7] but very few reports have been published using transparent electrodes .

In this study, we report the fabrication of polymer ferroelectric capacitors using P(VDF-TrFE) and two types of transparent electrodes on flexible, optically transparent polyethylene napthalate (PEN) substrates. Specifically, we compare the performance and reliability of these ferroelectric capacitors with a transparent conducting oxide and a transparent conducting polymer (Indium-Tin Oxide (ITO) and poly(3,4-ethylenedioxythiophene):polystyrenesulfonate, PEDOT:PSS)) and offer an explanation for the observed results.

2. Experimental

The devices with transparent polymer electrodes were fabricated by first spinning PEDOT:PSS (Sigma Aldrich, conductivity ca. 1 S/cm) on a cleaned PEN substrate at 3000 rpm for 30 seconds and drying on a hotplate in air at 110 °C for 30 mins, resulting in a ~100 nm thick film. For comparison, a thin film of transparent conducting oxide (ITO, R_s ~ 50 Ω/sq.) as the bottom electrode was sputtered on PEN. The P(VDF-TrFE) (70 – 30 mol%) obtained from Piezotech S.A, France was dissolved in anhydrous methyl ethyl ketone (MEK) at a concentration of 20 mg/mL to get a 2 wt.% solution. P(VDF-TrFE) films were spin-coated on ITO and PEDOT:PSS coated PEN substrates at 6000 rpm for 60 secs and baked on a hotplate at 80 °C for 1 hour. The films were then annealed in vacuum at 140 °C for 4 h. The samples were allowed to slowly cool down to room temperature to facilitate grain growth [8]. All layer thicknesses were measured using a Dektak profilometer. Finally, the top PEDOT:PSS electrode was spun under similar conditions as the bottom electrode and patterned by an optimized reactive ion etch (RIE) process in oxygen plasma. The etching was carried out at an RF power of 10 W, 13 mTorr of O_2 for 20 s using evaporated (patterned) Au as a hard mask.

The ferroelectric capacitors were characterized using a Premier Precision II ferroelectric tester, from Radiant Technologies Inc. Surface morphology was studied using a Nova NanoSEM 630 FESEM for Scanning Electron Microscope (SEM) images. The crystallinity and inter-planar spacing was evaluated using Grazing Incidence X Ray

Diffraction (Bruker D8 Discover). The electrical characterization was done using the Keithley 4200 Semiconductor Parameter Analyzer.

3. Results and Discussion

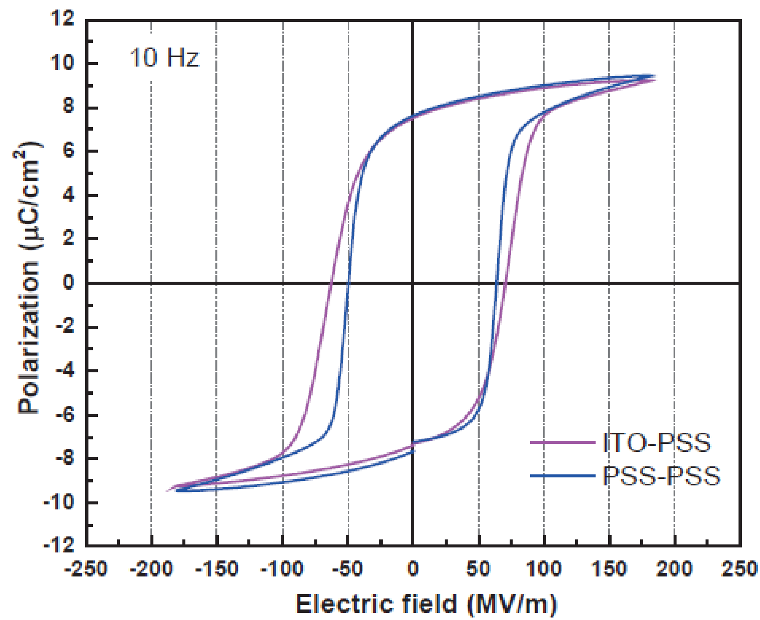

Figure. 6.1 Polarization-Electric field (P-E) hysteresis curves measured at ± 15V and 10 Hz. The device structures are PEN/ITO/P(VDF-TrFE)/PEDOT:PSS and PEN/PEDOT:PSS/P(VDF-TrFE)/PEDOT:PSS.

Typical hysteresis loops for a 100 nm thick P(VDF-TrFE) film on ITO and PEDOT:PSS bottom electrodes, measured at 10 Hz are shown in Fig. 6.1. The two types of capacitors exhibit comparable remanent polarization (P_r) and average coercive field (E_c) ~ 6.5 μC/cm^2 and 72 MV/m, respectively. Our remanent polarization values are

comparable to typically reported capacitors using P(VDF-TrFE) as the ferroelectric copolymer. Recently, Xu et al.[9] reported solution processed ferroelectric capacitors using PEDOT:PSS and Polyaniline (PANI) as bottom and top electrodes, respectively with E_c ~ 130 MV/m. In comparison, our devices exhibit much lower coercive voltages of 72 MV/m. We believe that patterning the top PEDOT:PSS electrode with an oxygen plasma process reduces the coercive voltage, probably because of defects and charges induced by the oxygen plasma at the polymer-ferroelectric interface.

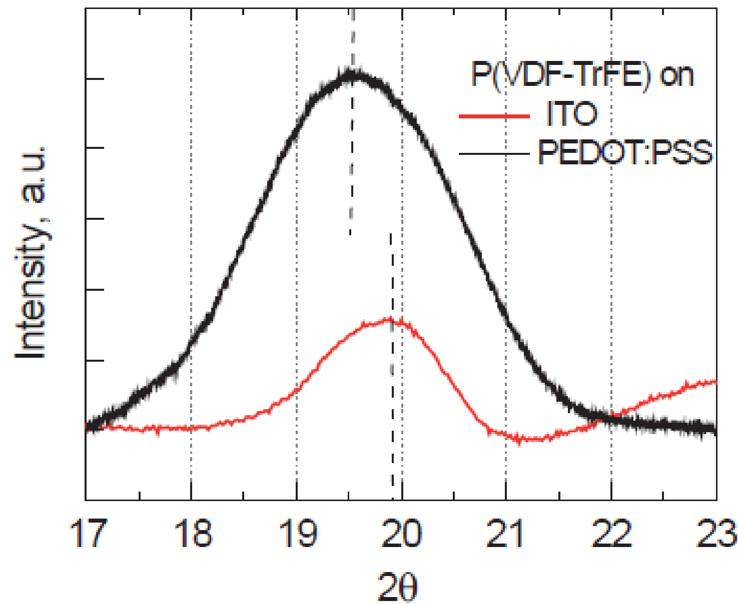

Figure. 6.2 Grazing Incidence X Ray Diffraction spectra for 100 nm P(VDF-TrFE) films grown on ITO and PEDOT:PSS. The incidence angle was set at 0.5°

The microstructure and crystallinity of P(VDF-TrFE) films depend on the processing conditions and the substrate [10]. Fig. 6.2 compares the Grazing Incidence X-Ray Diffraction (GIXRD) spectrum of 100 nm thin P(VDF-TrFE) films deposited on ITO and

PEDOT:PSS. The films on ITO substrate exhibit a broad peak at a 2θ ~ 19.9°, indicating the presence of polar, ferroelectric β phase in the all-trans (TTTT) configuration. The calculated inter-planar spacing is ca. 4.44 Å. The broadness arises due to the two close lying peaks corresponding to the Bragg diffraction of (110) and (200) planes. On the other hand, the GIXRD of P(VDF-TrFE) films grown on PEDOT:PSS peak at a 2θ ~ 19.5°, indicating a larger inter-planar distance ca. 4.55 Å and a FWHM ~ 2.27 °.

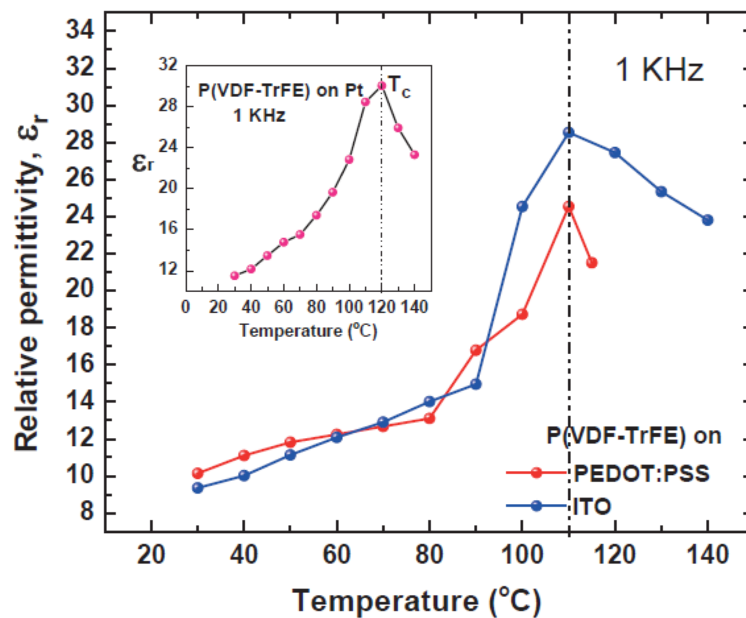

Figure. 6.3 Temperature characteristics of dielectric constant of P(VDF-TrFE) films on ITO and PEDOT:PSS measured at 1 KHz. Inset shows a higher Curie transition (T_c) temperature of P(VDF-TrFE) on Pt.

When subjected to a heating-cooling cycle, P(VDF-TrFE) thin films undergo a ferroelectric-paraelectric (F-P) phase transition. The phase transition, on cooling, involves rotational motion of the bonds to form a polar, ferroelectric, all-trans (TTTT) conformation where all the monomer units are aligned normal to the polymer chain [11]. The Curie transition temperature (T_c) for the copolymer P(VDF-TrFE) decreases with increasing TrFE content [12]. The reported T_c value for 70-30 mol.% P(VDF-TrFE) grown on metal electrodes with an average grain size of ~180 nm is 118 °C [8]. Typically, T_c is defined as the temperature where the dielectric constant reaches a maximum.

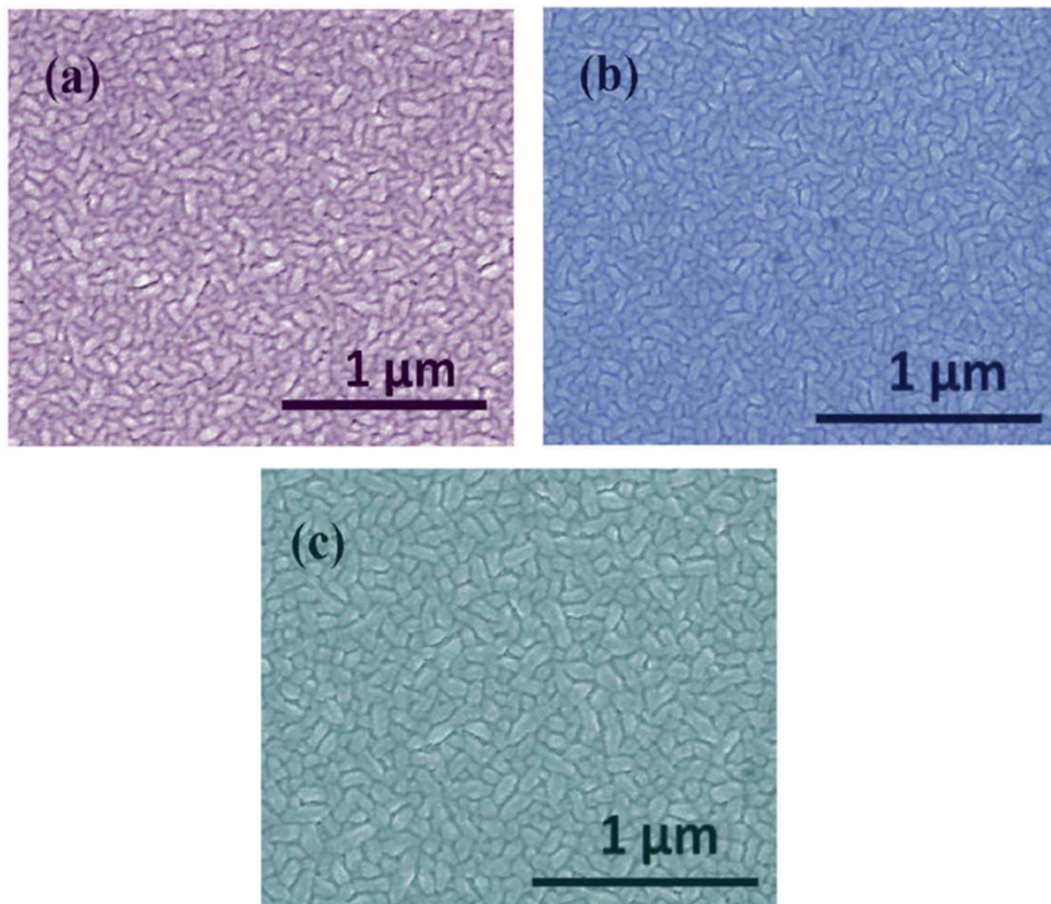

Figure. 6.4 SEM images of P(VDF-TrFE) grown on (a) ITO, (b) PEDOT:PSS and (c) Pt substrate.

The temperature dependence of dielectric constant of P(VDF-TrFE) thin films grown on various substrates, at 1 KHz over a temperature range between 30 °C and 140 °C is shown in Fig. 6.3. The P(VDF-TrFE) films grown on ITO and PEDOT:PSS electrodes exhibit a ferroelectric-to-paraelectric transition at a lower temperature compared to the films grown on Pt surface (inset). To help understand the origin of this effect, Fig. 6.4 shows SEM images of P(VDF-TrFE) films grown on these substrates, and indicates that the T_c shifts to lower temperatures with decreasing grain-size.. The average grain size of films grown on ITO, PEDOT:PSS and Pt is 70 ± 5 nm, 65 ± 5 nm and 160 ± 10 nm, respectively. The dependence of T_c on grain size could be related to internal stresses induced in the smaller grains. It is well-known that the introduction of stress and defects can reduce the activation energy barrier for the phase transition in ferroelectric polymers, thus reducing the Curie temperature [12]. Internal stresses are higher in P(VDF-TrFE) films with smaller grains due to the higher concentration of grain boundaries resulting in a reduced T_c, as shown in Fig. 6.3. In addition, we have also observed that the maximum dielectric constant decreases with decreasing grain size which could be attributed to the presence of more defects and trap states at the grain boundaries.

Polarization fatigue, the reduction in the amount of switchable polarization with repeated switching, is shown in Fig. 6.5. The figure compares the fatigue behavior of devices with ITO and PEDOT:PSS electrodes. The devices are stressed and measured at a frequency of 100 Hz to ensure complete dipole switching in every fatigue cycle.

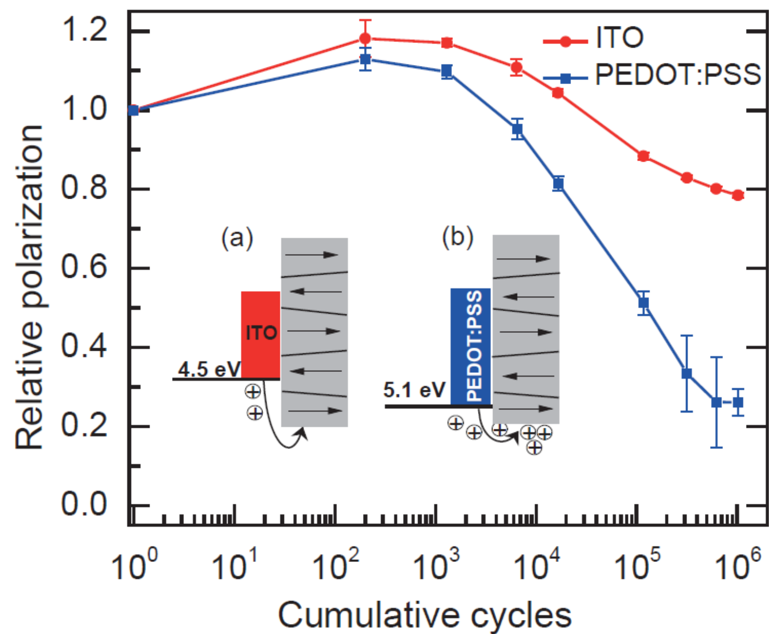

Figure. 6.5 Normalized fatigue behavior for ITO and PEDOT:PSS bottom electrode capacitors showing dP (=P*− P^) vs. frequency, where P* is the (remanent + non-remanent polarization) and P^ is the non-remanent polarization from a PUND measurement. The devices were stressed at a switching frequency of 100 Hz. Insets (a) and (b) illustrate the charge injection mechanism in oxide and polymer electrodes.

It can be seen from Fig. 6.5 that after 10^6 cycles, P(VDF-TrFE) capacitors on ITO retain ~78% of their original polarization values, whereas P(VDF-TrFE) capacitors on polymer electrodes retain only ~20% of the initial polarization. This is a significant result and can be explained based on a charge injection model as shown in the inset of Fig. 6.5.

It is known that the work function of solvent-cleaned ITO is 4.5 ± 0.1 eV [13] and the Highest Occupied Molecular Orbital (HOMO) of PEDOT:PSS is 5.1 ± 0.1 eV [14]. This difference in the work function of the two electrode materials results in band-offsets at the interface between the electrode and ferroelectric as illustrated in insets of Fig. 6.5. In order to confirm the difference in the charge injection model, the J-V characteristics (leakage current density – applied voltage) for both structures, ITO/P(VDF-TrFE)/PEDOT:PSS and PEDOT:PSS/P(VDF-TrFE)/PEDOT:PSS were measured and are shown in Fig. 6.6. The bottom electrode was swept from -15 V to +15 V for the measurement. In this configuration, holes are injected from the bottom electrode into the P(VDF-TrFE) layer under positive bias (0 to +15 V) and from the top electrode under negative bias (0 to -15 V).

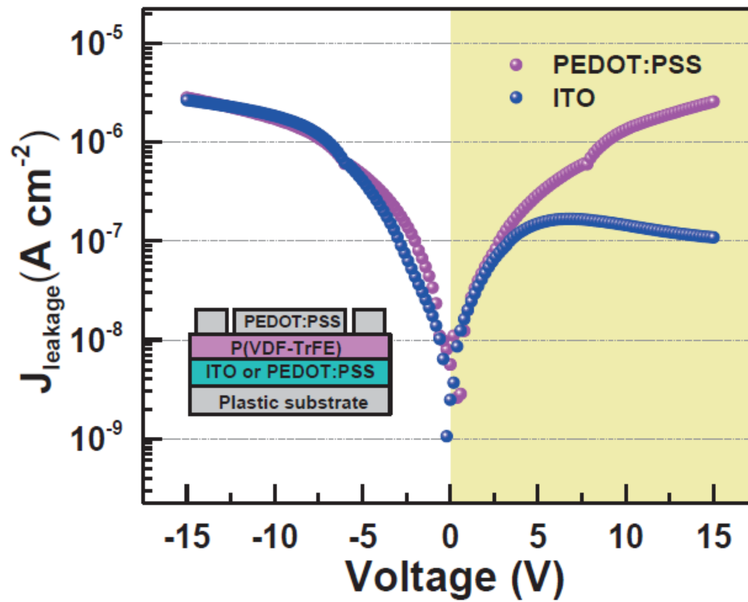

Figure. 6.6 A comparison of J-V (leakage current density vs. voltage) characteristics of ferroelectric capacitors; ITO/P(VDF-TrFE)/PEDOT:PSS and PEDOT:PSS/P(VDF-TrFE)/PEDOT:PSS. The bottom electrode was swept from -15 V to +15 V while the top electrode was at 0 V. Inset shows the device cross-section on a plastic substrate.

It can be seen that under positive bias a significantly higher hole injection current is observed from the PEDOT:PSS electrode as compared to ITO, which can be attributed to the smaller band offset and smaller energy barrier for hole injection. The leakage current for both structures overlaps under negative bias since the top electrode is similar, i.e. PEDOT:PSS. A well-known model for polarization fatigue in inorganic ferroelectrics has been demonstrated where injected electronic pined the domain walls leading to the suppression of ferroelectric polarization [15]. Our results indicate that

polarization fatigue in organic ferroelectrics appears to have the same origin as polarization fatigue in inorganic ferroelectrics.

4. Conclusions

In summary, we have demonstrated functional flexible and transparent polymer ferroelectric capacitors with transparent electrodes. The polymer electrodes exhibit lower coercive voltages identical to those reported on metal electrodes, but still show substantial fatigue. The conducting oxide electrodes dramatically improve the fatigue performance of the ferroelectric polymer. The difference in fatigue behavior of devices with different transparent electrodes is explained using a charge injection model based on domain wall pinning by injected electronic charges.

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CHAPTER 7

High Performance Non-Volatile Ferroelectric Memory on Banknotes

M.A. Khan, Unnat S. Bhansali, and H. N. Alshareef (Advanced Materials 24 (2012) 2165)

Abstract

Here, we demonstrate the first ever polymer ferroelectric memory on banknotes. Our all-polymer devices show excellent performance with a maximum remnant polarization ~ 8.2 μC/cm^2, low coercive fields (50 MV/m), low leakage (~ 10^{-6} A/cm^2), record mobilities (~ 0.12 cm^2/V.s), high I_{on}/I_{off} ratio (~ 5x10^3), large memory window (~ 8 V), low turn on voltages (~ −0.5 V), low operating (after switching) voltages (~ 4 V) and excellent retention characteristics upto 10000 sec.

1. Introduction

There has been an increased interest recently in using active electronic components and RFID tags to determine the authenticity of money and stop counterfeiting [1-3]. Electronic features in the form of integrated silicon circuits are difficult to fabricate on banknotes due to the required high-temperature processing and limited flexibility of silicon. Organic electronics has emerged as a promising alternative that allows the fabrication of electronic circuits on a variety of substrates such as glass, fabric, plastics and paper [4-7]. The advantages of using organic electronics are their flexibility, transparency, low-temperature process requirements, and the potential they offer for large-area and low-cost deposition techniques such as spin coating and ink jet printing.

An essential element for realizing anti-counterfeiting organic electronic circuits and RFID tags is a reliable non-volatile organic memory technology that can effectively complement logic and sensing circuit elements to provide the desired circuit functionality. Volatile memories can increase the complexity of circuit and are unsuitable for applications such as RFID tags as they do not have a constantly available power source. They derive power from the radio signal that they receive which means that they cannot always perform a memory refresh operation. Recently, Zschieschang et. al.[1] reported the successful demonstration of organic-electronic logic devices on paper and banknotes, but there is, to our knowledge, no existing reports on non-volatile organic memories fabricated on banknotes. Among polymer memories, ferroelectric

devices based on poly(vinylidene fluoride trifluoroethylene) [P(VDF-TrFE)] is of particular interest due to its sufficiently large spontaneous polarization, non-volatility, low leakage, excellent chemical stability and low temperature processability [8, 9]. Here, we demonstrate two types of all-polymer ferroelectric memories fabricated on a banknote: (1) ferroelectric capacitor memory device and (2) ferroelectric transistor memory device (FeFET), both of which are based on P(VDF-TrFE). A major challenge with using banknotes is their rough fibrous surface, which necessitates adding a planarization layer to render the surface amenable to electrode and active layer deposition. We show that this can be accomplished by using a spin-cast film of Polydimethylsiloxane (PDMS) as the planarizing layer because of its reported excellent adhesion, flexibility, transparency and impermeability to moisture and organic solvents [5, 6]. Apart from acting as the planarizing layer PDMS provides other important roles such as providing adhesion and strain isolation for the devices above. A key feature of PDMS layer is that it penetrates deep into the fibers of substrates such as banknotes, thus providing strong adhesion without chemical bonding. PDMS has been used as a strain isolation layer for silicon circuits fabricated on substrates like fabric, paper and leather [6]. PDMS has a low elastic modulus when compared to underlying substrates like paper (banknote), silicon and plastic. Because of this the underlying substrates are only weakly mechanically coupled to the electronic devices fabricated on our PDMS surface. Thus bending of the substrates leads to only a small bending of the electronic circuits above, thereby providing strain isolation.

Our all-polymer devices show excellent performance with a maximum remnant polarization ~ 8.2 μC/cm^2, low coercive fields (50 MV/m), low leakage (~ 10^{-6} A/cm^2), high mobility (~ 0.12 cm^2/V.s), high I_{on}/I_{off} ratio (~ 5x10^3), large memory window (~ 8 V), low turn on voltages (~ −0.5 V), low operating (after switching) voltages (~ 4 V) and excellent retention characteristics upto 10000 sec.

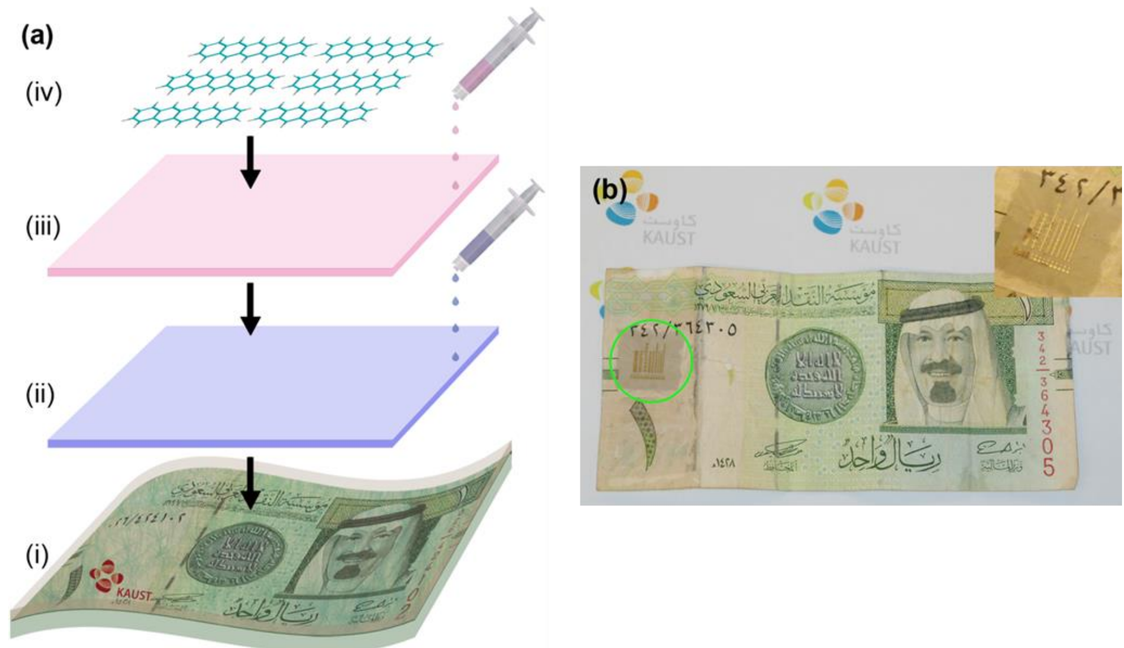

Figure. 7.1 (a) Fabrication of polymer ferroelectric memory devices on banknotes :(i) PDMS coated banknote (ii) spin-coating PEDOT:PSS bottom electrodes (iii) spin-coating P(VDF-TrFE) ferrolectric layer ~ 140 nm (iv) thermally evaporated pentacene thin film (~60 nm) and (b) Photograph of a 1-Saudi Riyal note covered with arrays of polymer ferroelectric memory devices.

2. Experimental

The fabrication steps of ferroelectric memory on banknote are illustrated in Fig. 7.1(a). Prior to device fabrication, the banknote was cleaned with acetone and DI water

and dried at 80 °C for 5 minutes. PDMS (Dow Corning Sylgard 184) was mixed in a 10:1 ratio with the curing agent and then spun onto the banknote at 1000 rpm for 30 seconds to get a 40 µm thick layer. It was left to cure at room temperature for 24 hours to minimize bubbles and pinholes formed on the surface. Once cured, the PDMS film was pre-annealed at 135 °C for 2 hours to minimize the stress in the subsequent layers due to a large thermal expansion coefficient mismatch (PDMS coefficient of thermal expansion of 310 ppm/°C) [10]. The inherently hydrophobic surface of PDMS was treated with O_2 plasma at a low RF power (~ 10 W) for 2 minutes using O_2 as the process gas and at a pressure of 150 mTorr. Previous studies have shown that the use of high RF powers (> 20 W) and long exposure times of O_2 plasma (> 20 minutes) can cause formation of a brittle silica layer on the surface which can lead to cracks in the surface [11]. The low power, short duration O_2 plasma treatment can help minimize the damage to the PDMS surface and the same time leaves silanol (SiOH) groups on the surface, rendering the surface hydrophilic. PEDOT: PSS in the form of Clevios PH-500 (Heraeus) was doped with ~ 4% Dimethylsulfoxide (DMSO) to increase its conductivity by more than two orders of magnitude (σ ~ 500 S/cm). Bottom gate electrodes of conducting PEDOT:PSS were spun at 1500 rpm for 30 sec and dried at 120 °C for 1 hr on a hotplate. A 2 wt.% solution of P(VDF-TrFE) dissolved in methyl ethyl ketone (MEK) was then spun on the PEDOT:PSS film at 3000 rpm for 60 s, followed by a soft bake for 30 min at 80 °C. The films were then annealed in vacuum at 135 °C for 4 hours to improve the crystallinity. The PEDOT: PSS and P(VDF-TrFE) layer were 50 ± 5 nm and 140 ± 5 nm thick respectively, as measured by a Dektak profilometer. A 60 nm pentacene (Sigma

Aldrich, 99 % purity) active channel layer was thermally evaporated at a deposition rate at 0.4 A°/s, monitored by a quartz crystal monitor. Finally gold (Au) was thermally evaporated through a shadow mask to define the source and drain electrodes. A photograph of the completed device on a 1-Saudi Riyal banknote, with arrays of transparent ferroelectric capacitors and transistors is shown in Fig. 7.1(b).

3. Results and Discussion

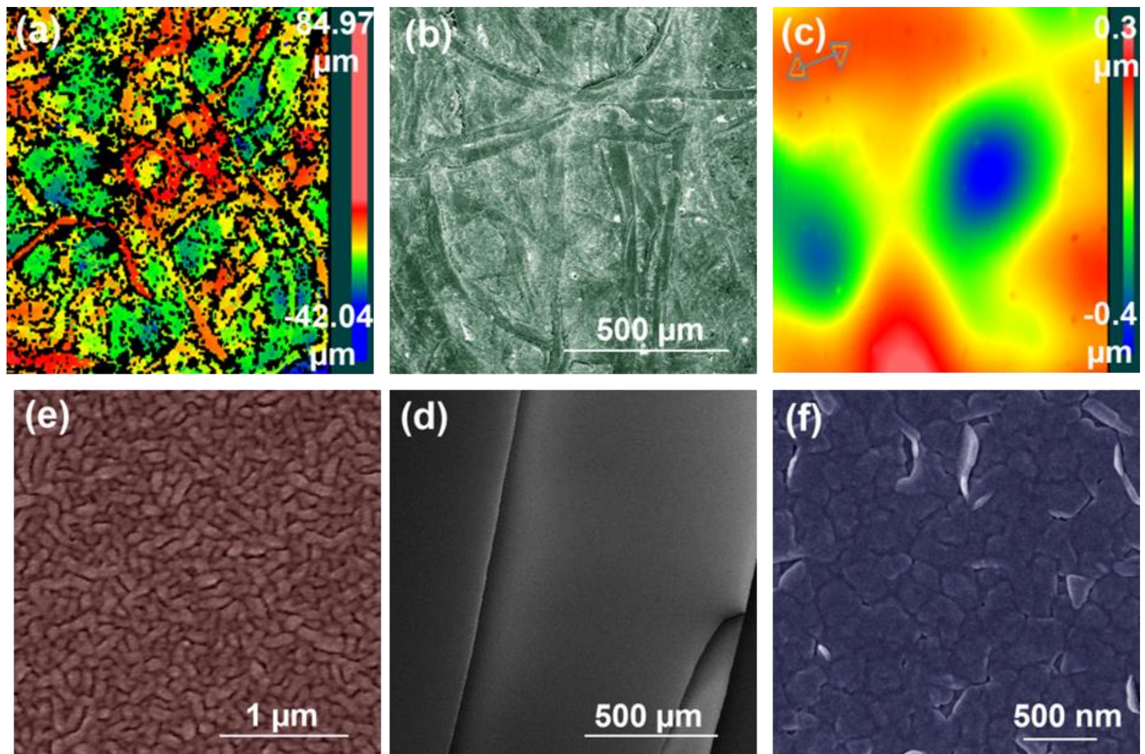

Figure. 7.2 3D surface profiles of untreated and PDMS coated banknote (a & c) and their corresponding SEM images (b & d). Top view SEM images of P(VDF-TrFE) grains grown on PEDOT:PSS electrodes (e) and pentacene grains grown on P(VDF-TrFE) (f). 10 µm x 10 µm 3-D AFM images of P(VDF-TrFE)grown on PEDOT:PSS and Pt (g) and (h), respectively.

Fig. 7.2 shows the surface characterization of the different layers in the ferroelectric memory devices. Fig. 7.2(a) and 7.2(b) show a 3D surface profile measurement and SEM image, respectively, of the rough fibrous surface of a banknote. The 3D surface profile was taken using a Zygo white light interferometer system and shows the rough surface of the banknote with an average roughness (R_{rms}) of ~ 7 µm and peak fibers approximately 80 µm in height. Fig. 7.2(c) and 7.2(d) show the smooth, nearly-featureless PDMS surface. The 3D surface profile illustrates significantly less light scattering compare to the banknote, reflecting the smooth nature of PDMS surface with average roughness (R_{rms}) of ~ 1.3 nm, as confirmed by atomic force microscopy (AFM). It is very important to have a smooth P(VDF-TrFE) surface when fabricating FeFETs, as the large surface roughness significantly degrades the performance of the device [9, 12]. Fig. 7.2(e) shows an SEM image of P(VDF-TrFE) grains grown on the PEDOT:PSS electrodes with an average grain size of ~ 80-90 nm. Fig. 7.2(f) shows pentacene grains grown on the hydrophobic surface of P(VDF-TrFE). The smooth and hydrophobic surface of P(VDF-TrFE) plays an important role in the growth of pentacene resulting in large grains of ~150 nm in size and consequently good FeFET performance. Furthermore we fabricated devices on Platinum (Pt) /Silicon (Si) substrates for comparison with devices using polymeric PEDOT:PSS electrodes. Fig. 7.2(g) and 7.2(h) show the AFM images of the surface of P(VDF-TrFE) grown on PEDOT:PSS and Pt electrodes with R_{rms} values of 1.16 nm and 2.37 nm respectively, indicating improved film roughness on polymer electrodes.

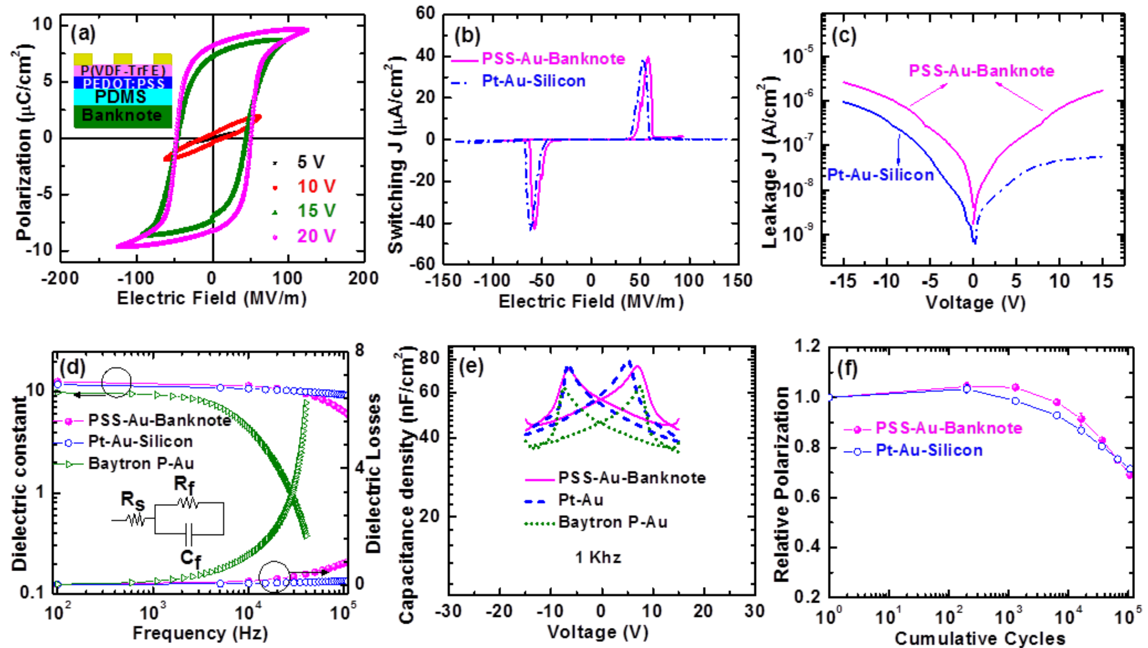

Figure. 7.3 (a) Hysteresis curves measured at different fields at 1 Hz for devices on banknotes Inset shows the device cross-section. (b) Switching current density versus electric field for devices on banknotes and Pt coated silicon substrates (c) J-V curves showing leakage current measured from −15 to +15 V. (d) Dielectric spectroscopy study with dielectric constant (left axis) and dielectric losses (right axis) for poorly conducting PEDOT:PSS (Baytron P), highly conducting PEDOT: PSS (PSS) and Pt electrodes. Equivalent circuit model is represented in the inset where R_s is series resistance from electrodes, R_f and C_f is resistance and capacitance of the film, respectively. (e) Capacitance –Voltage (Buttefly loops) at 1 KHz and reverse voltage sweep from −15 to +15 V. (f) Fatigue performance of capacitors at 100 Hz and stressed at 15 V for 100,000 cycles.

Fig. 7.3(a) shows the ferroelectric performance of our all-polymer ferroelectric capacitors on banknotes in comparison to devices with metal electrodes fabricated on silicon substrates. Our ferroelectric capacitors on banknotes show a maximum remnant polarization (P_r) of 8.2 μC/cm^2 and low coercive fields (E_c) of 50 MV/m, indicating highly crystalline P(VDF-TrFE) films. Our low coercive fields show a remarkable improvement in performance of polymer ferroelectric capacitors, mainly due to the high conductivity of

our PEDOT:PSS electrodes as compared to earlier studies using polymer electrodes. Recently, Xu et al.[13] reported ferroelectric capacitors using polymer electrodes, with E_c of ~ 130 MV/m. We believe this can be attributed to the poor conductivity of the polymer electrodes used in the study which leads to a large voltage drop across the electrode. The poorly conducting polymer electrode acts as a large resistor connected in series with the ferroelectric capacitor. The intrinsic coercive field of the ferroelectric film itself does not change. Instead, a higher voltage is needed to reach the required applied field to switch the ferroelectric copolymer film. More importantly, our devices on banknotes with highly conducting PEDOT: PSS electrodes displayed low coercive fields comparable to devices with metal electrodes. In ferroelectric capacitors, it is critical that the difference between switching and non-switching current is maximized to be able to distinguish the "0" from "1" stored memory state. Fig. 7.3(b) shows that our polymer capacitors on banknotes display peak switching current density ~ 40 $\mu A/cm^2$; at a coercive field of 55 MV/m. This is comparable to our devices on silicon substrates and an improvement from reported devices in literature [14, 15]. Fig. 7.3(c) displays the low leakage current densities (~10^{-6} A/cm^2) on our banknote capacitors. In an earlier study we showed that the leakage current mechanism in P(VDF-TrFE) dielectric is Schottky controlled and therefore involves charge carrier injection from the electrodes into the conduction band of the dielectric over a barrier height dependent on the work function of the respective electrodes [16]. The Schottky controlled leakage current is given by: [17]

$$J = AT^2 exp\left(\frac{aE^{0.5} - \phi_B}{kT}\right) \qquad (7.1)$$

where A is the effective Richardson's constant, T is temperature, E is applied electric Field, ϕ_B is barrier height and a is a constant. The devices on banknotes with PEDOT: PSS and Au electrodes show symmetric I–V curves as shown in Fig. 7.3(c). This is because of similar Highest Occupied Molecular Orbital (HOMO) level for PEDOT:PSS ~5.2 eV [18] and work function of Au of ~ 5.1 eV. The devices with metal electrodes show lower leakage current in the forward bias regime which can be explained based on the higher work function of bottom Pt electrode (5.65 eV) compared to the top Au electrode (5.1 eV).

Fig. 7.3(d) shows the complex relative permittivity (dielectric constant) and the loss factor (tan δ) of polymer capacitors on banknotes compared to capacitors with metal electrodes fabricated on silicon substrates. All device areas were fixed at 0.0001875 cm^2. A step-like decay of the dielectric constant is seen, consistent to the dielectric response of ferroelectric thin films. The dielectric response of ferroelectric capacitors can be modeled as an equivalent circuit consisting of a resistor in series with a parallel RC circuit. The capacitor shows an RC time constant behavior determined by $\tau = R_sC_f$, where R_s is the series resistance and C_f is the film capacitance [19-21]. Using poorly conducting electrodes will lead to a significant degradation in dielectric

performance at high frequencies because of high series resistance across the electrode. Devices with poorly conducting PEDOT: PSS (Baytron P) electrodes (σ ~ 1 S/cm) show a poor dielectric response with significant drop in permittivity which goes to ~ 0.2 at 40 kHz. This limits the use of the poorly conducting PEDOT: PSS electrodes to low frequency applications. In contrast we can see that upon using highly conducting PEDOT: PSS using same device area, it is possible to get devices with low losses and excellent dielectric response up to 10^5 Hz, frequencies applicable to relevant applications of these memory devices on banknotes such as RFID circuits. This is further emphasized in Fig. 7.3(e); Capacitance-Voltage (CV) measurements of the devices on banknotes show that at frequencies of 1 KHz the devices show capacitance of 75 nF/cm^2, similar to devices on silicon substrates.

Polarization fatigue behavior of ferroelectric capacitors with polymer and metal electrodes is compared in Fig. 7.3(f). The devices on banknotes show good fatigue performance comparable to metal electrodes retaining 80 % of the polarization after 10^4 cycles. The results represent fatigue measurements from 5 different devices on the sample, showing the consistency in polarization degradation. A bipolar triangular waveform with amplitude of 15 V and 10 ms pulse width was applied to assess the fatigue behavior.

To evaluate the reliability of these devices, we tested 30 devices with different device areas of 0.002 cm^2, 0.0007 cm^2 and 0.0000785 cm^2 corresponding to circles with diameters of 500 µm, 300 µm and 100 µm respectively. Fig. 7.4(a) shows an actual

layout of the capacitors with an average remnant polarization (P_r) ~ 7.65 ± 0.4 μC/cm^2 and an average coercive voltage ~7.62 ± 0.28 V (~55 MV/m). Our capacitors on banknotes show similar polarization when compared to devices fabricated on silicon substrates using Pt electrodes which show an average P_r~ 7.6 μC/cm^2 (not shown here). We had 27 functional devices giving a yield of 90%, emphasizing the reliability and reproducibility of the process. Devices E300, E100 and J500 were not functional. A closer look at these devices revealed scratches and holes in these areas as seen from the optical microscope images in Fig. 7.4(c) and 7.4(d). This can be attributed to bubble/pinholes and defects in the PDMS film underneath which can occur during the curing process. In contrast, Fig. 7.4(b) shows optical microscope images of some functional devices.

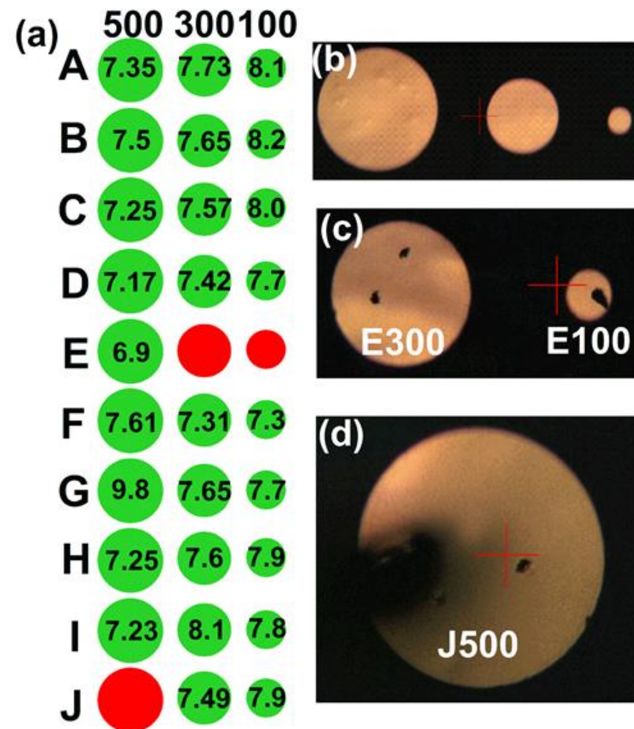

Figure. 7.4 (a) Schematic of device layout on banknotes with different diameters of 500, 300 and 100 µm (left to right). (b) Optical microscope images of working devices. (c) and (d) defects and irregularities in non-functional devices E300, E100 and J500.

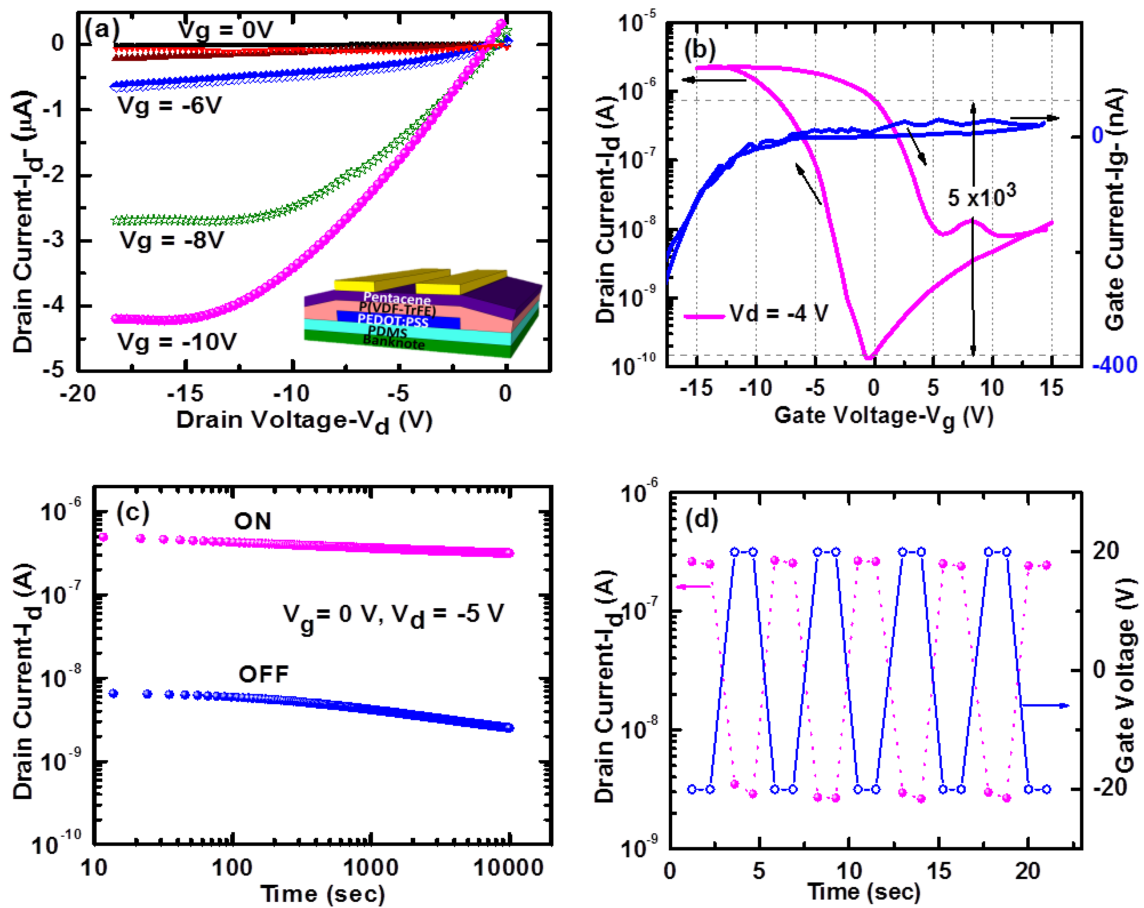

Figure. 7.5 (a) Source-drain (I_d-V_d) characteristics of a p-channel transistor on banknote with W/L ratio = 1000/60. Inset shows the device cross section. (b) Transfer characteristics (I_d-V_g) [left axis] and gate current (I_g-V_g) [right axis] of FeFETs on banknote measured at V_d = −4V. (c) Retention characteristics of FeFETs measured at V_g= 0 V and V_d = −5 V. A 3 sec. gate voltage pulse of −20 V and +20 V was applied to turn the transistor ON or OFF before the test. (d) Dynamic retention (Id versus time) plot obtained using a pulse width of 1 sec at V_d = −5 V.

One of the disadvantages of ferroelectric capacitors for memory applications is that they suffer from destructive read-out. In contrast, ferroelectric field effect transistors (FeFETs) are more suitable for non-volatile memory applications because of

their non-destructive read out and low power consumption. Several reports on FeFETs with different semiconductors like TIPS pentacene, P3HT, MEH-PPV exist, but most of these devices suffer from high operating voltages and low mobilities due to thick and rough P(VDF-TrFE) films [22-24]. A cross section of our device structure is shown in the inset of Fig. 7.5(a). PDMS coated banknotes act as substrates, with PEDOT:PSS polymer gate electrodes, P(VDF-TrFE) dielectric layer and pentacene as the active channel semiconductor. The thickness of the P(VDF-TrFE) and pentacene layers were 140 nm and 60 nm respectively and width and length of the channel was 1000 µm and 60 µm, respectively. Fig. 7.5(a) shows typical drain current-drain voltage (I_d-V_d) transistor characteristics of our polymer FeFET, measured using a Keithley 4200 semiconductor analyzer. The p-type FET works in the accumulation enhancement mode where holes are the majority charge carriers. The drain current-gate voltage (I_d -V_g) transfer curves and leakage (I_g -V_g) curves are shown in Fig. 7.5(b). The gate voltage was swept from +15V to −15V and back, keeping the drain voltage fixed at −4 V. The copolymer P(VDF-TrFE) film is seen to act as a good dielectric with low leakage current (I_g) in the order of 30 nA even at saturation voltages of 15 V. The arrows show the clockwise hysteresis of the drain current (I_d) consistent with the accumulation and depletion of p-type charge carriers. It indicates that the current retention behavior is due to the dipolar polarization by the ferroelectric rather than charge trapping mechanism [25]. The transistor behaves as a bi-stable memory; at 0 V gate bias the current in the off state and on-state differ by more than 3 orders of magnitude (I_{on}/I_{off} ~ $5x10^3$) .The p-type

FeFET working in the accumulation mode also shows low turn on voltage of ~ −0.5 V. The saturation mobility of our devices was determined using the following equation:

$$I_{d,sat} = \frac{W}{2L} C_i \, \mu_{sat} \, (V_g - V_{th})^2 \qquad (7.2)$$

The saturation mobility (μ_{sat}) of our devices was determined to be 0.12 cm^2/Vs, which matches previous records of pentacene/P(VDF-TrFE) FeFETs [23, 26].

Data retention charac. of our devices were examined by a measurement of the remnant drain current as a function of time. Fig. 7.5(c) shows the value of I_d in the ON and OFF states as a function of retention time, measured at V_d = −5 V. The ON and OFF states were produced at gate voltages of −20 and +20 V with a 3 sec pulse, respectively. The memory retention is excellent for these polymer FeFETs on banknotes with the ON/OFF ratio more than two orders of magnitude even after 10000 seconds. The ON current decreases slightly to 62 % of its initial value but the OFF current remains constant and even decreases slightly. The dynamic retention properties of our non-volatile FeFETs is shown in Fig. 7.5(d). An alternating and repetitive ±20 V pulse (1 sec in width) was applied for switching the transistor ON and OFF. Fig. 7.5(d) clearly differentiates the ON and OFF states, with a good distinguishable dynamic retention ratio of approximately ~ 80. This is slightly smaller than the ON/OFF ratio during the measurement of the static retention, which may be due to lower polarization of the ferroelectric under a 1 sec pulse versus a 3 sec pulse. This memory retention behavior show an improvement compared to previous reports of pentacene/P(VDF-TrFE) FeFETs [22, 24, 26].

4. Conclusions

In summary, we have fabricated the first polymer ferroelectric memory on banknotes. Our devices demonstrate low operating voltage (~ 4 V), high mobility (~ 0.12 cm^2/Vs), large memory window (~ 8 V) and long retention times of more than 10000 sec. The performance is comparable to previous records of low voltage pentacene FeFETs on other substrates [23, 26]. These reports used strain-annealing and quenching of P(VDF-TrFE) grown on Al electrodes to obtain small grain morphology and reduce the roughness. The excellent performance of our FeFETs can be attributed to the growth of thin P(VDF-TrFE) films (~140 nm) on polymeric PEDOT:PSS electrodes which leads to a smooth film (R_{rms} ~ 1.16 nm) and small grains (size ~ 80 nm) as seen from Fig. 7.2. Furthermore we demonstrate that by using conducting polymer electrodes, it is possible to get high performance devices with low E_c (50 MV/m), high P_r (~ 8.2 $\mu C/cm^2$) and high J (~ 40 $\mu A/cm^2$). The polymer electrodes perform well under frequencies of a few kiloHertz which is already sufficient for basic logic operations. The high performance, ease of fabrication and excellent compatibility suggests that conducting polymer electrodes can be used as cheap, flexible and transparent global interconnects without compromising on the device performance. Thus these results suggest that the fabrication of high performance non-volatile polymer memories on banknotes is possible. However to make these devices commercially viable, much work still needs to be done in optimizing printing techniques, improving mechanical integrity, devising appropriate encapsulation layers.

CHAPTER 7 REFERENCES

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CHAPTER 8

All Polymer Memory Based on Phase Separated Ferroelectric-Fullerene Blends with Resistive Switching Behavior

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Abstract

All polymer non-volatile bistable memory devices are fabricated from blends of ferroelectric P(VDF-TrFE) and n-type semiconducting PCBM. The nanoscale phase separated films consist of PCBM domains that extend from bottom to top electrode, surrounded by a ferroelectric P(VDF-TrFE) matrix. Highly conducting PEDOT:PSS polymer electrodes are used to engineer band offsets at the interfaces. The devices display resistive switching behavior due to modulation of this injection barrier. With careful optimization of the solvent and processing conditions, it is possible to spin cast very smooth blend films (R_{rms}~ 7.94 nm) and with good reproducibility. The devices exhibit high I_{on}/I_{off} ratios (~$3x10^3$), low read voltages (~5 V), excellent dielectric response at high frequencies (ε_r~8.3 at 1 MHz) and excellent retention characteristics upto 10,000 secs.

1. Introduction

Polymer-based resistive memories targeting next generation transparent and flexible electronics are experiencing unprecedented levels of research activity. They are promising circuit elements due to their simple device structure, easy processability, high storage density, and the potential they offer for large-area and low-cost, large-area deposition techniques such as spin coating, roll-to-roll processing, and ink jet printing [1]. Among polymer memories, fullerene-based composites have been studied for their Write- Once- Read- Many- times (WORM) memory behavior. Most of these systems are reported to work by either charge trapping or charge transfer mechanism [2-5]. Aggregation of fullerene leading to electrical shorts and unstable memory behavior remains a significant problem. Therefore, the development of fullerene-based nonvolatile memory devices is still in its early stages. On the other hand, ferroelectric memories based on the copolymer poly(vinylidene-fluoride–trifluoroethylene) [P(VDF-TrFE)] have been widely studied and are of particular interest to the organic electronics community due to its non-volatility, large spontaneous polarization, excellent chemical stability, and low temperature processability [6].

Ferroelectric capacitor memories make use of the hysteresis behavior by associating $+P_r$ and $–P_r$ states with Boolean 1 and 0 logic states. The problem with using ferroelectric capacitors is that they suffer from destructive read-out, as the voltage applied to read the information can erase it as well [7]. Ferroelectric transistor (FeFETs) memories solve this problem as they provide resistive switching that can be sampled at

low voltages without affecting the ferroelectric polarization. Historically, polymer FeFETs have suffered from poor performance due to low mobilities, low ON/OFF ratios, poor retention characteristics and high operating voltages. Surface roughness, defects and leakage through the P(VDF-TrFE) film are some of the reasons for the poor performance [6, 7]. Further, FeFETs are a complicated three terminal device making it difficult to scale upto an integrated memory circuit. Recently Asadi et. al demonstrated a breakthrough device using phase-separated films of P(VDF-TrFE) and the p-type polymer semiconductor rir-P3HT [regio-irregular poly(3-hexylthiophene)] [8]. The proposed working principle in these devices is that the dipole alignment in the ferroelectric component of the blend modulates the injection barrier at the semiconductor–electrode interface. These polymer blend devices, which used only metal electrodes, have a simple two terminal structure like a capacitor and at the same time provide resistive switching like the FeFETs. The choice of semiconductor material and electrode becomes very critical in order to engineer an injection barrier at the interface. This is necessary to achieve current modulation in these devices. p-type semiconductors like rir-P3HT and phenyl-substituted poly(phenylene-vinylene) (SY) with HOMO levels of 5.1 and 5.4 eV, respectively form an injection barrier with metal electrodes like Ag and Al with work functions of 4.3 eV and 4.2 eV, respectively [9]. On the other hand, they form ohmic contacts with polymer electrodes like PEDOT: PSS (work function of 5.1 eV), which is undesirable to obtain resistive switching. Furthermore, blends of these p-type semiconductors and ferroelectric P(VDF-TrFE)

suffer from coarse phase separation resulting in high surface roughness leading to electrical shorts and low device yields as reported in the work by Asadi et al [10].

In this study, we have fabricated the first resistive memory devices based on n-type semiconductor-ferroelectric polymer blends and optimized their performance. Our devices are all-polymer, non-volatile, bi-stable, resistively switched, and incorporate nanoscale phase separated blends of a ferroelectric and semiconducting material. Highly conducting PEDOT:PSS polymer electrodes are used to engineer the band offsets at the interfaces. By carefully optimizing the solvent and processing conditions we achieved very smooth films with low surface roughness (R_{rms}~ 7.94 nm) and good reproducibility. The devices exhibit high I_{on}/I_{off} ratios (~$3x10^3$), low read voltages (~5 V), excellent dielectric response at high frequencies (ε_r~8.3 at 1 MHz) and excellent retention characteristics upto 10,000 secs.

2. Experimental

A. Sample Preparation

The resistive memory devices with P(VDF-TrFE):PCBM blend films were fabricated on transparent glass substrates. Prior to device fabrication, the substrate was cleaned by a sequence of ultra-sonication in acetone, isopropanol followed by DI water. The glass substrates were then treated with O_2 plasma at a low RF power (~ 10 W) and pressure of 150 mTorr for 2 minutes, rendering the surface hydrophilic. PEDOT:PSS in

the form of Clevios PH-1000 from Heraeus was chemically doped with ~ 4% Dimethylsulfoxide (DMSO) to achieve maximum conductivity of ~ 900 S/cm. Bottom electrodes were formed by spinning the doped PEDOT:PSS solutions at 1500 rpm for 30 seconds followed by annealing on a hotplate at 120 °C for 30 minutes. Simultaneously as bottom electrode 80 nm Au was evaporated using e-beam onto silicon substrates, with a 8 nm Ti adhesion layer.

High purity (99.8 %) Cyclohexanone (Acros) was used as the common solvent for both the ferroelectric copolymer P(VDF–TrFE) and the n-type organic semiconductor PCBM. P(VDF-TrFE) (70–30 mol%) obtained from Piezotech S.A, France was dissolved in Cyclohexanone at a concentration of 30 mg/mL of P(VDF–TrFE) for a pure ferroelectric layer. A 5 % PCBM solution was prepared by adding 15.78 mg of PCBM to 300 mg P(VDF-TrFE) and dissolved at 50 °C for 24 hours. Similarly solutions with different concentrations of PCBM (3 %, 7%, 10% and 15%) were prepared by varying the amount of PCBM (9.27 mg, 22.58 mg, 33.33 mg and 52.94 mg), added to 300 mg of P(VDF-TrFE). All the different concentrations of PCBM formed clear homogenous solutions stable even after a few weeks. The filtered polymer blend films were spun in a nitrogen filled glove box, at 3000 rpm for 60 seconds followed by a soft bake for 30 min at 90 °C. The films were then annealed in vacuum at 135 °C for 4 hours to improve the crystallinity of the P(VDF-TrFE) phase. The thickness of the films was ~ 200 ± 20 nm as measured by a Dektak profilometer, and did not change with increasing PCBM concentrations. Finally a drop-on-demand piezoelectric inkjet-printing technique using a Jetlab® II Precision

Printing Platform (Microfab Technologies Inc.) was used to print the top PEDOT:PSS electrodes. Devices with Au top electrodes were completed by thermally evaporating ~60 nm Au through a shadow mask.

B. Characterization

All current-voltage measurements were carried out in air ambient using Keithley 4200 semiconductor characterization system. Transmission data for the polymer blend films were obtained using UV-Vis optical absorption spectra (ThermoScientific Evolution 600) .Surface morphology and roughness for films was studied using Atomic Force Microscopy (Agilent 5400). Cross section morphology of the devices was studied using Transmission Electron Microscopy (Titan ST) and operated at an accelerating voltage of 300 kV. Energy Filtered TEM analysis was done to elementally map fluorine in the polymer blend films. The crystallinity and inter-planar distance of polymer chains was evaluated using Grazing Incidence X-ray Diffraction (Bruker D8 Discover) while the bonding and dipole orientation was analyzed using Fourier-transform infrared spectroscopy (FT-IR, ThermoScientific Nicolet iS10).

3. Results and Discussion

A. Switching behavior of blend films

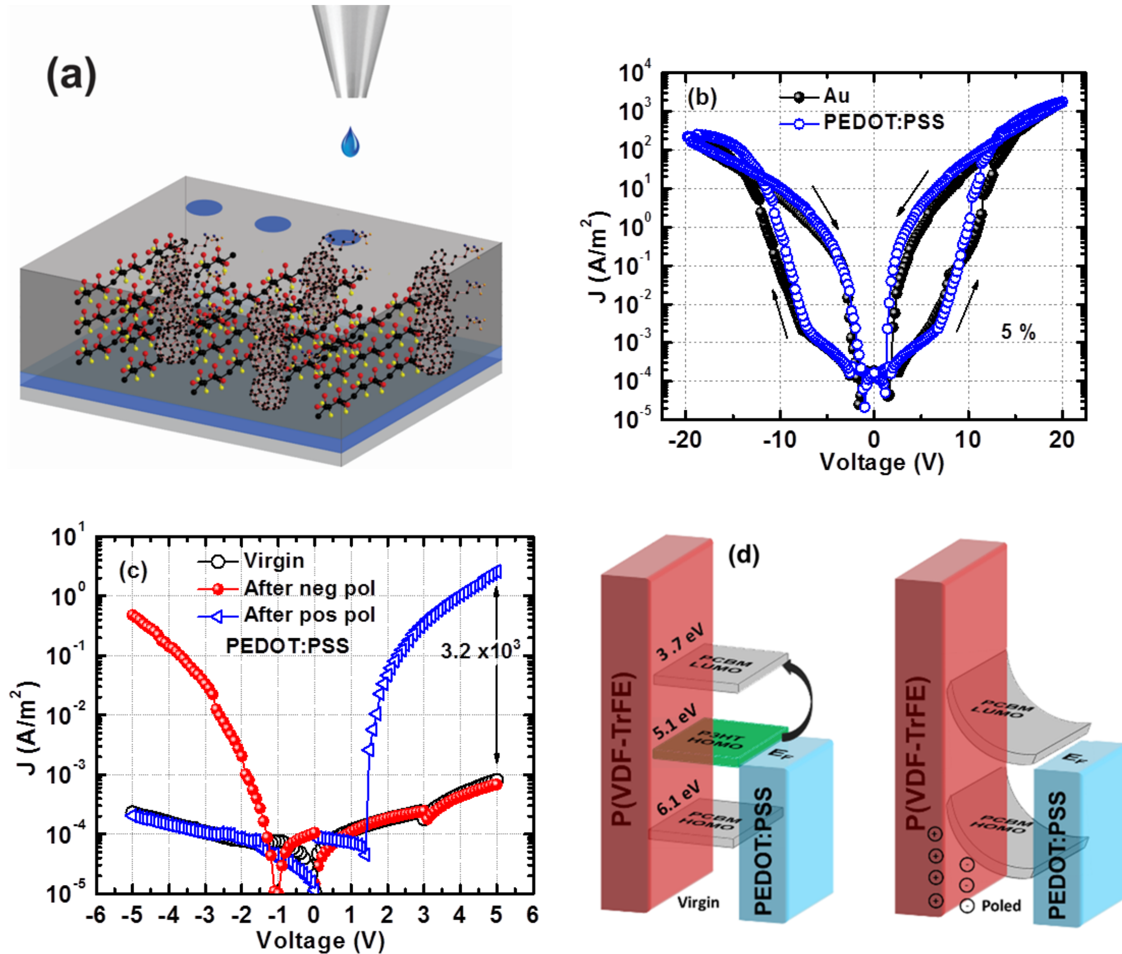

Figure. 8.1 (a) Schematic 3-D cross section of all polymer memory devices with phase separated network of P(VDF-TrFE) and PCBM polymers. PEDOT:PSS was ink-jet printed as the top electrode. (b) Current density (J) –Voltage (V) sweeps of P(VDF-TrFE)-PCBM blend (95:5) devices with Au and PEDOT:PSS electrodes showing resistive memory behavior. (c) J-V memory performance of virgin polymer P(VDF-TrFE)-PCBM blends (95:5) and after positive and negative poling. (d) Band diagram at the interface between PCBM phase and bottom PEDOT:PSS electrode for virgin and poled devices.

A schematic of the all-polymer resistive memory device with highly conducting top and bottom PEDOT:PSS electrodes (σ ~ 900 S/cm) is shown in Fig. 8.1(a). The active single-layer consists of a film spin cast from a blend of ferroelectric P(VDF-TrFE) and n-type semiconducting PCBM from a common solvent - cyclohexanone. The active layer consists of an interpenetrating network of the P(VDF-TrFE) matrix [70-30 molar ratio] with the semiconducting PCBM phase forming continuous channels between the two polymer electrodes, a feature that is essential for the operation of these devices. Device fabrication details are discussed in the experimental section of the manuscript. Highly conducting doped PEDOT: PSS top electrodes (σ ~ 900 S/cm) with an area of approx. 7.85 x 10^{-5} cm^2, were ink-jet printed on top of the phase separated blend films. The processing was optimized for different blend ratios from 1 wt % to 15 wt% PCBM. Devices with 10 wt % and higher PCBM content suffered from high leakage leading to low device yields. The best performance and yield were achieved using devices with 5 wt% PCBM content.

Fig. 8.1(b) shows the current density (J) - voltage (V) characteristics of 200 nm thick blend films of ferroelectric P(VDF-TrFE) containing 5 wt % n-type semiconductor (PCBM). The J-V curves of the devices show a current hysteresis on both positive and negative sweeps from 0 to 20 V and 0 to -20 V, indicative of a bistable nonvolatile resistive memory device. The device can be programmed into high and low resistance states (OFF/ON) by applying a voltage pulse larger than the coercive field of the ferroelectric (~ ± 20 V). These nonvolatile memory devices can be read out non-

destructively at low bias unlike ferroelectric capacitors which suffer from a destructive read-out. Devices fabricated on both Au and PEDOT: PSS electrodes showed similar hysteresis loops. This is expected due to the similar work function of Au (~5.1 eV) and HOMO level of PEDOT: PSS (~5 eV) [11]. Switching behavior for P(VDF-TrFE) - 5 wt. % PCBM blends sandwiched between polymeric PEDOT:PSS electrodes is shown in Fig. 8.1(c). For all switching characterization, the bottom electrode was grounded and the bias applied to the top electrode. At low positive biases (0 to 5 V) less than the coercive field of the P(VDF-TrFE), the charge injection is from the bottom electrode interface. In the virgin unpoled state, the current is low (~ 10^{-3} A/m^2) due to the large injection barrier between the PEDOT: PSS and the PCBM. Fig. 8.1(d) shows the band diagram at the bottom interface between the bottom PEDOT:PSS electrode, ferroelectric P(VDF-TrFE) and semiconducting PCBM. The mismatch of HOMO of PEDOT: PSS (~ 5 eV) and the LUMO level of n-type PCBM (3.7 eV) forms a large injection barrier (~1.3 eV) for charge carriers [12]. Thus, there is poor charge injection and the current is low. This is unlike previously reported p-type semiconductors like P3HT which form an ohmic contact with PEDOT: PSS [9]. Without having the injection barrier between the electrode and semiconducting phase, the device is always in a low resistance state (ON) and cannot be turned OFF. Subsequently, the ferroelectric is poled with a positive bias (+20V) at the top electrode as shown in the poled band diagram on the right in Fig. 8.1(d). The dipoles in the ferroelectric phase rotate and align with the electric field. Due to the alignment of dipoles, negative polarization charge is built up in the P(VDF-TrFE) phase at the interface with the top electrode, while positive polarization charge

accumulates at the interface with bottom electrode. To neutralize the positive polarization charge, negative charges accumulate in the n-type PCBM semiconductor at the interface with the bottom electrode. The accumulated charge leads to a strong band bending in the PCBM phase, effectively reducing the injection barrier at the bottom electrode. This is indicated by poled band diagram in Fig. 8.1(d) (positively poled case), showing the lowering of the injection barrier. Subsequent sweeps up to a low bias, + 5 V see efficient injection of charges due to lack of an injection barrier. This current density is more than 3 orders of magnitude larger than the virgin unpoled junction, thus turning the device ON. When the device is poled with an opposite polarity i.e. negative bias (-20 V) applied at the top electrode, the negative polarization charge in P(VDF-TrFE) at the bottom interface builds up. The negative charge polarization cannot be compensated by the n-type PCBM. Thus injection barrier remains constant at bottom interface and the device goes back to an OFF state like the virgin unpoled state. Thus the interface is bistable and can be switched to an ON and OFF state by poling with opposite polarity voltage pulses. Similarly at reverse bias, where charges have to be injected at the top interface the device can be turned into ON and OFF states, as seen in Fig. 8.1(c). Thus the devices exhibit non-volatile bistable resistive memory behavior with excellent yields and a small spread in current densities.

B. Physical Characterization of the films

i. Morphology

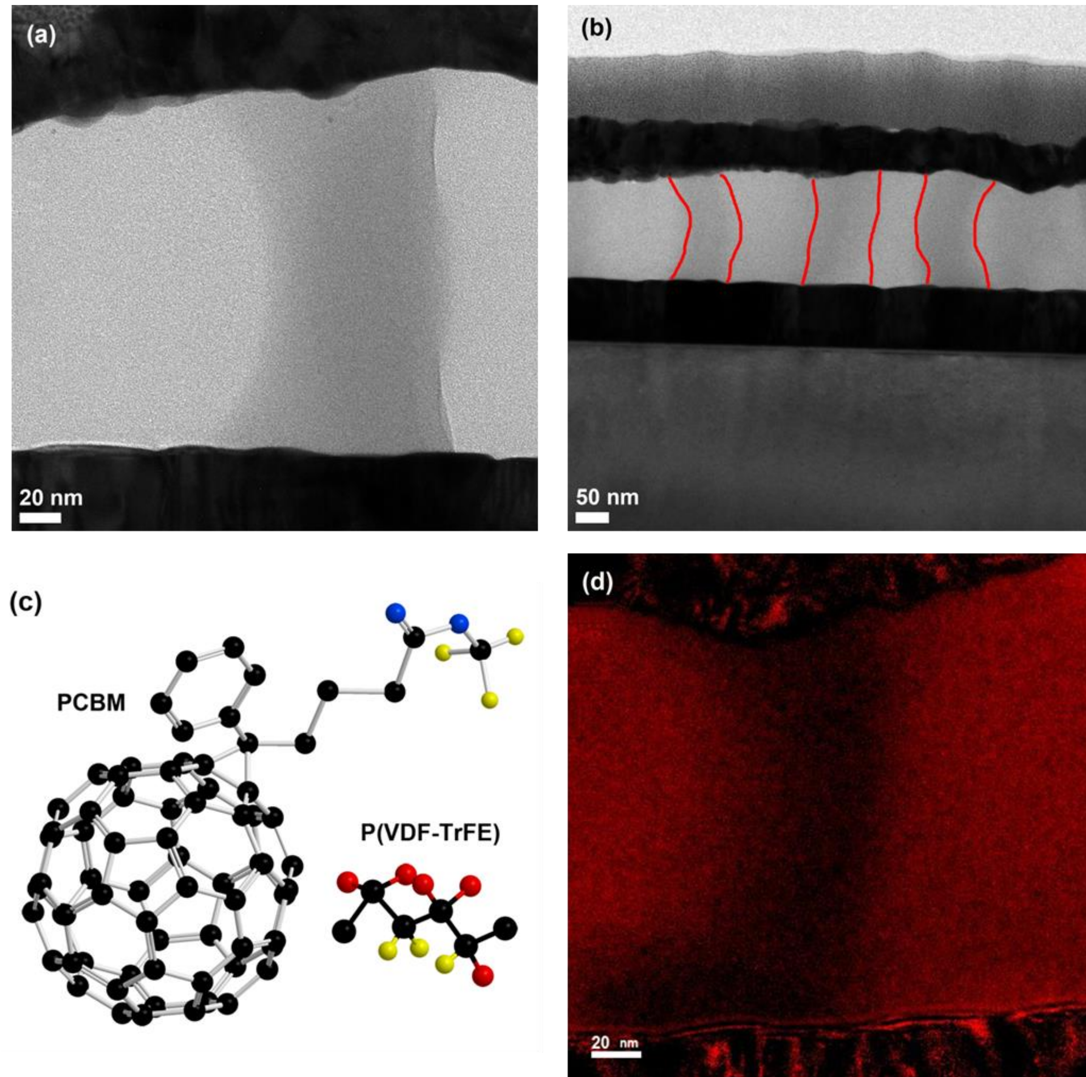

Figure. 8.2 (a) Cross section TEM showing nano-scale phase separated PCBM continuous between the gold electrodes (b) Cross section TEM showing multiple phase-separated PCBM columns throughout the thin film with an average domain width of ~ 80 nm. The red lines are a visual aid for delineation of the PCBM phase in the PVDF TrFE matrix. (c) Molecular structures of semiconducting PCBM (left) and ferroelectric P(VDF-TrFE) (right). (d) X-ray elemental mapping of the polymer blend film using EFTEM showing the fluorine (red) in the P(VDF-TrFE) phase.

The morphology of the blend films is very critical to achieving nonvolatile resistive switching memory behavior in these devices as explained above. Fig. 8.2(a) is a TEM cross section that shows the morphology of these polymer blend films with 5 wt% PCBM sandwiched between gold electrodes. The morphology of these blend films consists of phase separated semiconducting PCBM domains that extend from bottom to top electrode, surrounded by a ferroelectric P(VDF-TrFE) matrix. The observed phase separation was seen in multiple locations throughout the film, as shown in Fig. 8.2(b) with an average width of the PCBM phase between 80-90 nm. Fig. 8.2(c) shows the chemical structure of ferroelectric copolymer, P(VDF-TrFE) [$(-CH_2-CF_2-)_n-(CHFCF_2)_m$] and n-type semiconducting PCBM [$C_{72}H_{14}O_2$]. The ferroelectricity of PVDF stems from the dipole moments in the molecule that can be aligned with the applied field by rotation of the polymer chain. The dipole moments originate predominantly from the presence of the strongly electronegative fluorine atoms and electropositive hydrogen [1]. Fig. 8.2(d) shows high resolution X-ray elemental mapping of the polymer blend film using EFTEM (Energy filtered TEM). Based on the presence of fluorine in P(VDF-TrFE), the images clearly distinguish the phase separated P(VDF-TrFE) matrix (red) with the semiconducting PCBM phase (black) which is continuous between the two electrodes.

The surface morphology and grain growth of 200 nm thick polymer blend films annealed at 135 ºC was characterized using atomic force microscopy (AFM). The surface topography images of pure ferroelectric P(VDF-TrFE) i.e. 0 wt % PCBM and blends with 5 wt% PCBM and 10 wt% PCBM are shown in Fig. 8.3(a), 8.3(b) and 8.3(c) respectively.

The measured surface roughness of our PCBM blend films surprisingly shows very smooth films with R_{rms} of ~ 7.94 nm and 11.5 nm for 5 wt % and 10 wt % films, respectively. The surface roughness is comparable to the pure P(VDF-TrFE) films which have an average R_{rms} ~ 6.9 nm.

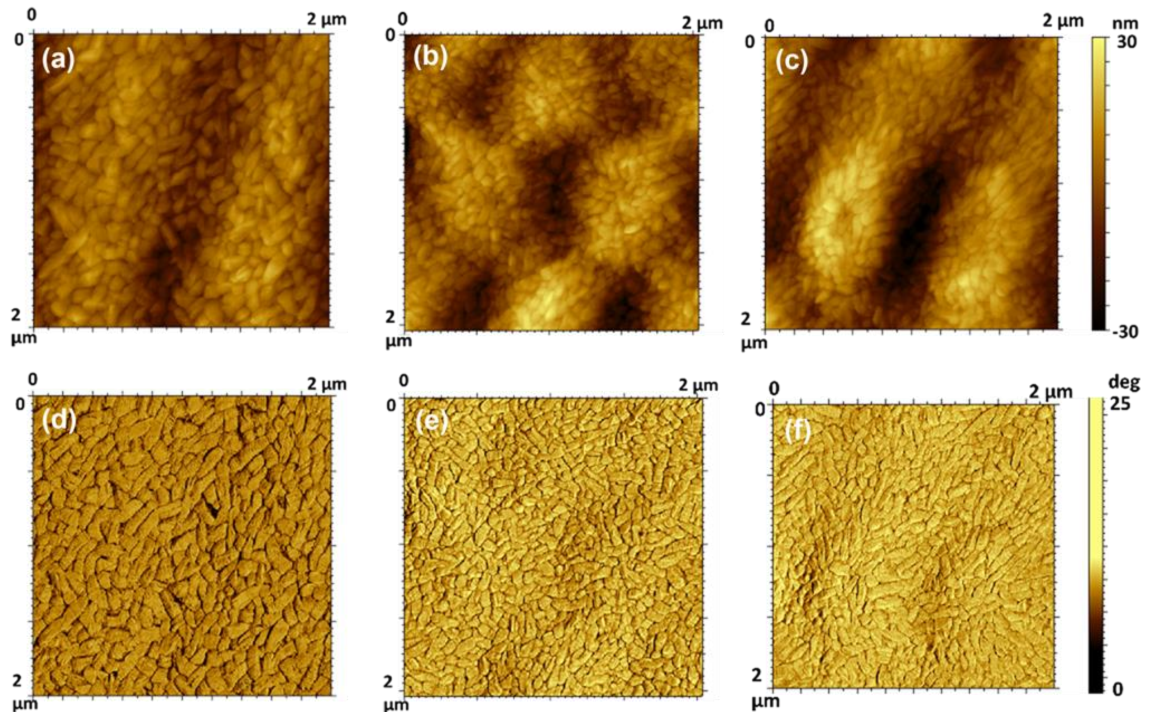

Figure. 8.3 AFM images showing topography (a,b,c) and phase (d,e,f) images of a blend with 0 wt %. 5 wt % and 10 wt% PCBM respectively.Surface roughness (R_{rms}) ~ 6.9, 7.94 and 11.5 nm for 0, 5 and 10 wt% PCBM films.

This is a remarkable improvement from previous reports on ferroelectric-semiconductor blend films of P(VDF-TrFE) and rir-P3HT where the coarse phase separation leads to surface roughness ~ 100 nm comparable to film thickness [9, 10]. High surface roughness leads to non-uniform electrical field across the active layer and

possibly poor yield and reproducibility. Previous studies have used tetrahydrofuran (THF) as a common solvent for both P(VDF-TrFE) and P3HT[10] ,but is a poor solvent for both. P3HT has poor solubility in THF while its low viscosity (0.456 mPa s @ 25ºC), low boiling point (66 ºC) and high vapor pressure (143 mmHg @ 20 ºC) are detrimental to P(VDF-TrFE) film forming characteristics. The use of cyclohexanone, a common solvent that dissolves the ferroelectric and semiconductor material is key to obtaining extremely smooth films resulting in high performance and yields for our devices. Cyclohexanone has recently been reported in spin-cast ultra-thin and smooth P(VDF-TrFE) films [13]. It has a high solubility for P(VDF-TrFE) and its high boiling point (156 ºC) , viscosity (2 mPa s@ 25ºC) and vapor pressure (5 mmHg @ 25 ºC) make it an excellent solvent for spin casting ferroelectric P(VDF-TrFE) thin films. At the same time it also has an excellent solubility for PCBM (> 91 %) [14]. Using cyclohexanone we were able to make clear homogeneous solutions of P(VDF-TrFE) and PCBM even at high concentrations of PCBM (>10 wt%), as seen from the photograph in Fig. 8.4(a). Thus we were able to fabricate very smooth blend films, with a drastic improvement in roughness to previous reports. Any small fluctuations in the homogeneity of the solution will lead to coarse phase separation and rough films.

The AFM phase images in Fig. 8.3(d), 8.3(e) and 8.3(f) show the P(VDF-TrFE) grains in a pure ferroelectric film, 5 wt% PCBM and 10 wt% PCBM, respectively. The average grain size of pure P(VDF-TrFE) is approximately 200 nm, consistent with previous reports in literature and indicating high crystallinity [1, 6]. Polymer blend films

with 5 wt % and 10 wt% PCBM also show well crystallized P(VDF-TrFE) grains with an average grain size of ~ 160 nm and 150 nm respectively. We believe the addition of PCBM leads to an increase in nucleation site density leading to smaller grain size observed for P(VDF-TrFE).

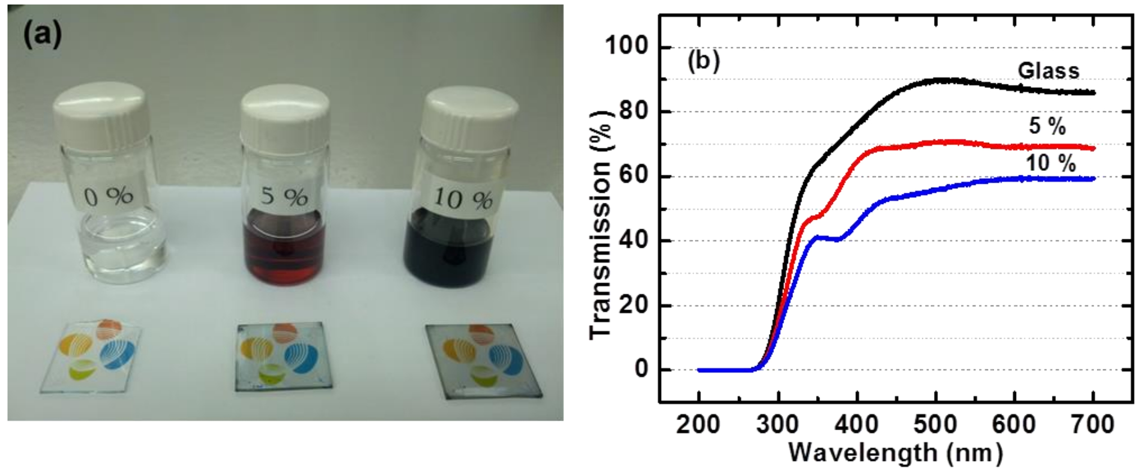

Figure. 8.4 (a) Photographs of the all-polymer transparent non-volatile resistive memory fabricated on glass substrates. The corresponding solutions with 0 wt%, 5 wt% and 10 wt% PCBM (Left to Right) showing a homogenous solution. (b) UV-Vis transmission spectra for devices with 5 wt% and 10 wt% PCBM blend films.

A photograph of the solutions and the all polymer memory devices with 0 wt%, 5 wt% and 10 wt% PCBM composition is shown in Fig. 8.4(a). Cyclohexanone forms a clear homogenous viscous solution with P(VDF-TrFE) and PCBM even at high concentrations. This is very critical in getting smooth polymer blend films essential for good device performance, as explained above. Fig. 8.4(b) shows the UV-Vis optical transmission spectra of P(VDF-TrFE)-PCBM blends films spun on glass substrates. At approximately λ =

600 nm, bare glass substrates have transmission upto ~ 87% and the transmission drops to ~70 and 60 % for 5 wt% and 10 wt% PCBM devices, respectively.

ii. Crystal Structure and Orientation

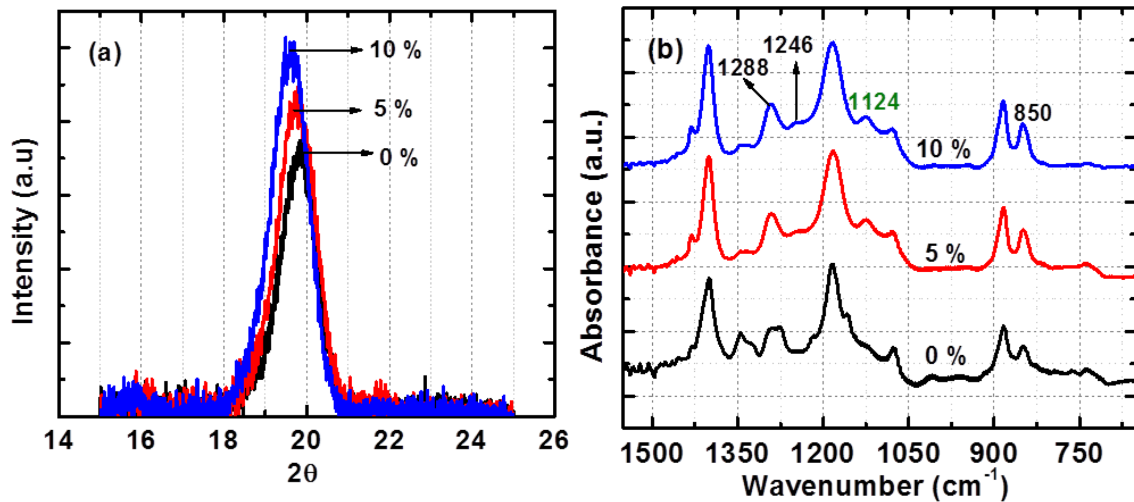

Figure. 8.5 (a) Grazing incidence XRD spectra for pure ferroelectric P(VDF-TrFE) and blend films with 5 wt% and 10 wt% PCBM. (b) FT-IR spectra of pure ferroelectric P(VDF-TrFE) and 5 wt% and 10 wt% PCBM blend thin flms.

Fig. 8.5(a) shows the Grazing Incidence X-ray diffraction (GIXRD) spectra which was used to study the crystal structure of pure ferroelectric P(VDF-TrFE) and the polymer blends with PCBM. Pristine P(VDF-TrFE) films spun on PEDOT:PSS electrodes and annealed at 135 ºC exhibit a peak centered at 2θ ~ 19.85°, characteristic of the ferroelectric β phase and reflection from the (110) and (200) planes. The inter-planar distance was calculated to be approximately 4.46 Å and is consistent with earlier

reports [15]. In comparison, the blend films exhibit a peak slightly shifted to the left at $2\theta \sim 19.75°$ and 19.6° for 5 wt % and 10 wt % PCBM films, respectively indicating a larger inter-planar distance. It is possible that with increasing PCBM content, some of the PCBM molecules are intercalating between the P(VDF-TrFE) polymer chains leading to larger inter-planar distance. Furthermore, the XRD peaks indicate that the polymer blend films have smaller crystallite size compared to the pristine P(VDF-TrFE) films with a larger full-width-half-maxima (FWHM), as confirmed by the AFM images above.

The presence of PCBM in thin films of the polymer blend was verified using transmission mode Fourier Transform Infra-Red (FTIR) spectroscopy. Fig. 8.5(b) shows the absorbance bands at 1288 cm^{-1} and 850 cm^{-1} associated with CF_2 symmetric stretching vibration and are characteristic bands of the trans-zigzag formation (β phase) [15-17]. Other major peaks identified are the 1400 cm^{-1} band characteristic of the CH_2 wagging vibrations, 1186 cm^{-1} band characteristic of asymmetric stretching of CF_2 and the 880 cm^{-1} band related to the rocking CH_2 vibration [16]. All these peaks were common in both pristine P(VDF-TrFE) and PCBM blended films. A couple of extra peaks were identified in the blend films at 1246 cm^{-1} characteristic of O=C-O-C stretching and at 1124 cm^{-1} from C-O-C stretching from the methyl ester group in the PCBM [18]. FTIR analysis proves the presence of PCBM in these polymer blend films but does not suggest any interaction or bonding between the PCBM and P(VDF-TrFE) chains.

C. Device Characterization of blend films

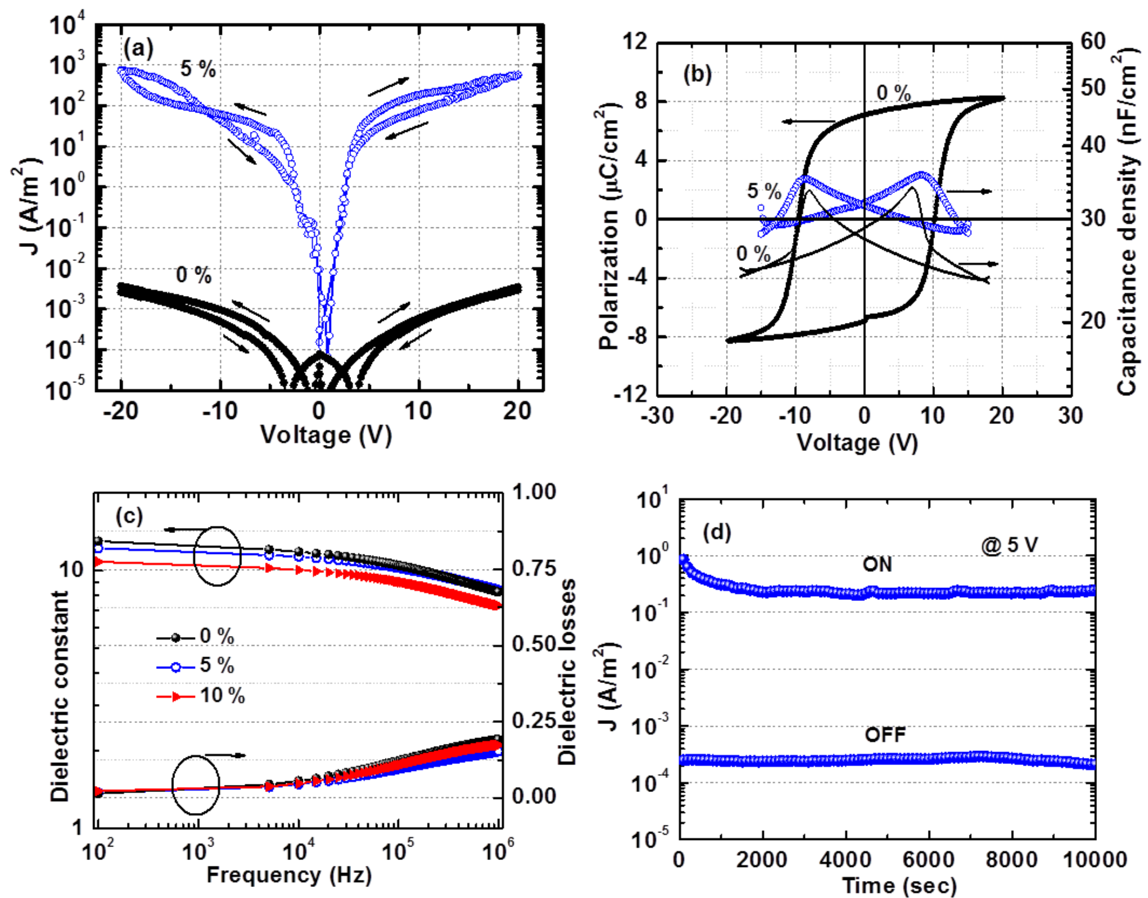

Figure. 8.6 (a) Current density (J)- Voltage (V) characteristics of 200 nm pure P(VDF-TrFE) films showing no current hysteresis. Un-annealed 5 wt % polymer blend films show an increase in current by 5 orders but no memory behavior. (b) Polarization-Voltage Hysteresis curve for 200 nm pure ferroelectric films at 10 Hz (Left Axis). Small signal Capacitance –Voltage (Butterfly loops) at (100 mV,1 MHz) for pure P(VDF-TrFE) films and blends with 5 wt% PCBM (Right axis). (c) Dielectric spectroscopy study with dielectric constant (left axis) and dielectric losses (right axis) for pure ferroelectric P(VDF-TrFE) (0 wt% PCBM) and polymer blend films with 5 wt% and 10 wt% PCBM content. (d) Retention characteristics of non-volatile resistive memory with 5 wt% PCBM measured at V = +5 V showing an ON/OFF ratio of ~10^3. A voltage pulse of +20 V and -20 V was applied to turn the device ON or OFF, respectively before the test.

Fig. 8.6(a) shows the current density (J) - voltage (V) characteristics of 200 nm thick pure ferroelectric P(VDF-TrFE) film. The J-V curves of pre-poled devices show no current hysteresis on either positive or negative bias sweeps and is consistent with the leakage current behavior of P(VDF-TrFE). At the same time J-V loops for un-annealed blend films with 5 wt % PCBM, show negligible hysteresis. This indicates that the current hysteresis and the resistive switching in blend films arise due to the ferroelectric polarization which modulates the current injection into the PCBM phase.

Ferroelectric hysteresis of pure P(VDF-TrFE) capacitors with a remnant polarization (P_r) of 7.1 μC/cm^2 and coercive field (E_c) of ~ 50 MV/m is shown in Fig. 8.6(b). The polarization could not be measured for P(VDF-TrFE) and PCBM blends even though FTIR and XRD analysis indicate the presence of ferroelectric β phase. This might be due to the high leakage current through the PCBM phase at high fields used for the P-V measurement. Small signal capacitance (C) - voltage (V) curves measured by superimposing a small AC electric field (100 mV, 1 MHz) over DC field sweep are also shown in Fig. 8.6(b). It is a measure of the modulation of dielectric constant by the remanent polarization state. The 200 nm thick P(VDF-TrFE)-PCBM blend films display a peak capacitance of ~ 35 nF/cm^2, comparable to pure P(VDF-TrFE) devices. A characteristic “butterfly” shape of the C-V curve is seen for blends with 5 wt% PCBM content, typical for ferroelectric materials. Fig. 8.6(c) shows the dielectric dispersion and the loss factor (tan δ) of pure P(VDF-TrFE) and blend memory devices. A gradual decay of the dielectric constant is observed, consistent with the dielectric response of

ferroelectric thin films. Our P(VDF-TrFE) copolymer films exhibit a dielectric constant of ~ 12.9 at 100 Hz, comparable to other reports in literature [19]. Upon adding PCBM the dielectric permittivity does not change as the response is dominated by the ferroelectric phase in the blend films. Devices with 5 wt% PCBM and 10 wt% PCBM also show excellent frequency dispersion upto frequencies of 1 MHz, with a negligible drop in permittivity and low losses.

Data retention characteristics of our devices were examined by a measurement of the current as a function of time. Fig. 8.6(d) shows the value of current density in the ON and OFF states as a function of retention time, measured at 5 V. The ON and OFF states were produced at by poling the device at +20 and -20 V, respectively. The all-polymer nonvolatile bistable resistive memory devices show excellent retention with the ON/OFF ratio of three orders of magnitude even after 10000 seconds, with almost no change in current modulation.

4. Conclusions

In summary, we have fabricated all-polymer nonvolatile bistable resistive memory devices made from phase separated blends of ferroelectric P(VDF-TrFE) and n-type semiconducting PCBM. The ferroelectric polarization modulated the current injection into the semiconducting phase, thus controlling the resistive switching behavior. The use of an n-type semiconductor helps us to fabricate an all-polymer device. Coarse phase separation of such polymer blend films has been an issue in the

past. This leads to large surface roughness and low device yields. The use of a cyclohexanone as a common solvent which has excellent solubility to both P(VDF-TrFE) and PCBM helped us fabricate devices with very low surface roughness (R_{rms} ~ 7.94 nm) leading to good device yields. Our devices demonstrate excellent performance with low read voltages (~ 5 V), good ON/OFF ratio (~ $3x10^3$), low frequency dispersion (upto 10^6 Hz) and long retention times of more than 10000 sec. The all-polymer, cost effective, solution processed devices are fabricated at low temperatures and have excellent performance comparable to devices with metal electrodes. This opens up the possibility of large scale fabrication of these resistive memory devices for flexible and transparent electronic applications.

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CHAPTER 9

High Performance Ferroelectric Memory Based on Phase Separated PPO Blends

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Abstract

High performance polymer memory is fabricated using blends of ferroelectric poly(vinylidene-fluoride-trifluoroethylene) (P(VDF-TrFE)) and highly insulating Poly(p-phenylene Oxide) (PPO). The blend films spontaneously phase separate into amorphous PPO nanospheres embedded in a semicrystalline P(VDF-TrFE) matrix. Using low molecular weight PPO with high miscibility in a common solvent i.e. Methyl Ethyl Ketone, we were able to spin cast blend films with extremely low roughness (R_{rms}~ 4.92 nm) and achieve nano-scale phase separation (PPO domain size < 200 nm). These blend devices display highly improved ferroelectric and dielectric performance with low dielectric losses (< 0.2 up to 1 MHz), enhanced thermal stability (~ upto 353 K), excellent fatigue endurance (80 % retention after 10^6 cycles at 1 KHz) and high dielectric breakdown fields (~360 MV/m).

1. Introduction

Flexible electronics research has made tremendous progress during the past 15 years, specifically in the area of organic thin film transistors (OTFT's), organic light emitting diodes OLED's) and sensors. An integral part of any flexible electronic circuits is a non-volatile memory component that can be used to store and retrieve information as required. Polymer memories continue to be the biggest hurdle in the development of polymer-based flexible electronics. Among polymer memories, ferroelectric memories based on P(VDF-TrFE) are one of the leading candidates in the flexible and organic electronics community due to its easy low -temperature processability, excellent chemical stability, sufficiently large spontaneous polarization, non-volatility, and short switching times [1, 2].

The potential of polymer ferroelectric memory was realized more than two decades ago but has not lead to any major commercial products. Some of the important limitations include poor leakage, high surface roughness, poor thermal stability, poor fatigue/retention endurance and low breakdown strength of thin film P(VDF-TrFE) ferroelectric memory devices [1]. In particular, the poor thermal stability and poor fatigue performance of the P(VDF-TrFE) thin films remains a major hurdle for commercialization of polymer ferroelectric memory [1, 3]. In recent years there have been numerous studies on the effect of different electrodes and interlayers on charge injection and fatigue performance of ferroelectric memory [4-6]. Nonetheless fatigue continues to be a big issue when characterized at a frequency low enough at which the

dipoles in the copolymer can switch and at an applied field close to saturation field of the ferroelectric thin film [7, 8]. Furthermore there are very few limited studies on the issue of thermal stability and poor breakdown strength of thin film P(VDF-TrFE) ferroelectric capacitors [9, 10]. In contrast to the strategy of modifying electrodes and interfaces to improve performance of polymer ferroelectric capacitors, one can look at modifying and optimizing the properties of ferroelectric thin films. One very promising and interesting approach is to blend ferroelectric polymers with low-k dielectrics to improve their properties. PVDF and P(VDF-TrFE) blend films have primarily been studied with PMMA which shows excellent solubility up to 40 wt% [11]. PVDF and PMMA blend systems have been studied, to observe effect of PMMA on the crystallization of PVDF and growth of nanocrystalline ferroelectric β phase in PVDF. These systems are complicated to fabricate as the blend films have to be melted, quenched in ice water and further annealed to get the desired ferroelectric properties [10, 12]. P(VDF-TrFE) copolymer also has good miscibility with PMMA up to 40 wt%. Earlier studies have characterized the morphology, dielectric and ferroelectric properties of P(VDF-TrFE)/PMMA blends and shown an improvement in performance [13-15]. Apart from PMMA, there are almost no reports of P(VDF-TrFE) blends with other insulating polymers for ferroelectric memory applications.

In this study we report the fabrication of thin film ferroelectric capacitors using blends of P(VDF-TrFE) with PPO. PPO is an amorphous high performance polymer dielectric with excellent electrical properties (good insulator, low dielectric losses), high

temperature stability, good chemical resistance, low moisture absorption, and high mechanical and dielectric strength [16, 17]. To our knowledge this is the first exhaustive study of P(VDF-TrFE)-PPO blend system for ferroelectric memory applications. We characterize the morphology and nanoscale phase separation of these blends using Atomic force Microscopy (AFM) and cross-section Transmission Electron Microscopy (TEM) imaging. The crystallinity and inter-planar distance of polymer chains was evaluated using Grazing Incidence X-ray Diffraction (GIXRD) while the bonding and dipole orientation was analyzed using Fourier-transform infrared spectroscopy. Furthermore, we report an exhaustive electrical and ferroelectric characterization of these blend films in a metal-insulator-metal (MIM) capacitor structure using Polarization-Voltage, Current-Voltage, dielectric spectroscopy and switching time studies. We have also characterized the thermal stability, fatigue endurance and breakdown strength of these films and report a tremendous improvement in the performance of these blend devices compared to unblended ferroelectric devices.

2. Experimental

The polymer blend thin films were fabricated on Platinum coated silicon substrates. Prior to device fabrication, the substrates were cleaned by ultra-sonication in Acetone, Isopropanol and DI water respectively. P(VDF-TrFE) (70/30 mol. %) obtained from Piezotech S.A, France was dissolved in anhydrous Methyl Ethyl Ketone (MEK) at a concentration of 20 mg/mL to make a 2 wt % solution. High purity low molecular weight

Polyphenylene Oxide (Noryl SA90 PPO) (M_n ~ 1800) obtained from Saudi Basic Industries Corporation (SABIC) was dissolved in 10 mL P(VDF-TrFE) solutions by varying the amounts (4.08 mg, 8.22 mg, 12.76mg, 17.39 mg, 27.27 mg) to make 2 wt % to 8 wt % P(VDF-TrFE)-PPO blend solutions. All the different concentrations of PPO formed clear homogenous solutions stable even after a few weeks. The filtered polymer blend films were spun in a nitrogen filled glove box, at 4000 rpm for 60 seconds followed by a soft bake for 20 min at 70 °C. The films were then annealed in vacuum at 135 °C for 4 hours to improve the crystallinity of the P(VDF-TrFE) phase. The thickness of the blend films was ~ 120 ± 10 nm as measured by a Dektak profilometer, and did not change much with increasing PPO concentrations. To complete the device, ~ 80 nm Gold (Au) was thermally evaporated through a shadow mask to define the top electrodes.

All current-voltage measurements were carried out in air ambient using Keithley 4200 semiconductor characterization system, while Polarization-Voltage and fatigue tests were done using the Premier Precision II ferroelectric tester (Radiant Technologies Inc.). Surface morphology and roughness for the blend films was studied using Atomic Force Microscopy (Agilent 5400). Cross section morphology of the devices was studied using Transmission Electron Microscopy (Titan ST) and operated at an accelerating voltage of 300 kV. Energy Filtered TEM analysis was done to elementally map carbon in the polymer blend films. The crystallinity and inter-planar spacing of polymer chains was evaluated using Grazing Incidence X-ray Diffraction (Bruker D8 Discover) while the

bonding and dipole orientation was analyzed using Fourier-transform infrared spectroscopy (FT-IR, ThermoScientific Nicolet iS10).

3. Results and Discussion

A. Physical Characterization of blend films

i. Morphology

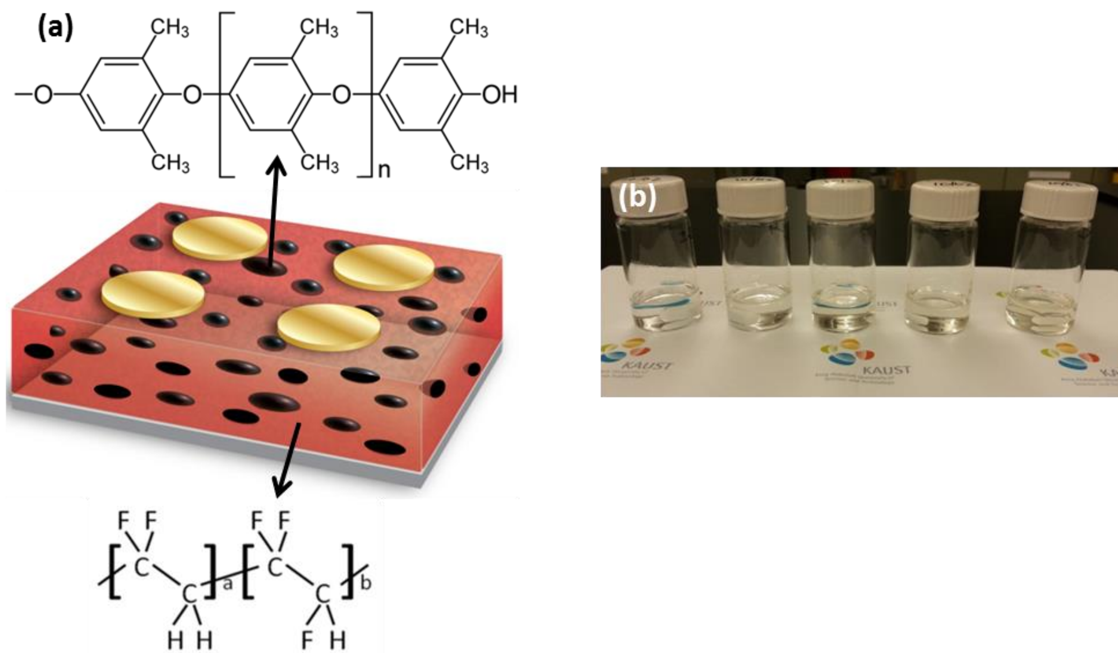

Figure. 9.1 (a) Schematic 3-D cross section of ferroelectric capacitors with phase seperated blends of P(VDF-TrFE)-PPO sandwiched between Pt and Au electrodes. The morphology consists of phase separated nanospheres of amorphous PPO, surrounded by P(VDF-TrFE) matrix. (b) Solutions with 0 wt%, 2 wt%, 4 wt %, 6 wt % and 8 wt% PPO (Left to Right) showing clear, homogenous and stable solutions.

A schematic of the nanoscale phase-separated blend devices is shown in Fig. 9.1(a). The active single-layer consists of a blend film spin-cast from a solution of ferroelectric P(VDF-TrFE) and insulating PPO from a common solvent: Methyl Ethyl Ketone. The morphology of these blend films consists of phase separated nanospheres of amorphous PPO, embedded in a semicrystalline P(VDF-TrFE) matrix. Polymers in general don't tend to mix with each other. Due to their highly disordered nature, they are in a state of high entropy. Thus when two polymers are blended together, mixing is generally disfavored due to the 2nd law of thermodynamics as they don't gain anything in entropy. Upon evaporation of a common solvent, polymers due to their long chain nature generally tend to phase separate leading to unstable nanostructures. However polymers with high miscibility in a common solvent and strongly correlated chains due to hydrogen bonding and dipole-dipole interactions can lead to stable nanoscale phase separation [10, 18]. P(VDF-TrFE) and PPO are highly miscible in MEK, and stable in a large range of compos. from 0 to 25 wt % of PPO content. Fig. 9.1(b) shows clear homogenous solutions from 2 wt % to 8 wt %. Solutions with up to 25 wt % PPO were made and remained stable even after a few weeks. Fig. 9.1(a) also shows the chemical structure of P(VDF-TrFE) and PPO. PPO i.e. Poly(p-phenylene oxide) is an aromatic polyether with oxygen connected to aromatic aryl groups. Ethers are slightly polar in nature as the C-O-C bond angle in the functional group is about 110°, and the C-O dipole does not cancel out. The presence of two lone pairs of electrons on the O atoms makes H-bonding with water and other polar molecules possible. We believe hydrogen bonding between the electronegative O in PPO and electropositive hydrogen in P(VDF-

TrFE) and the electropositive H in the methyl group of PPO and electronegative F in P(VDF-TrFE) leads to stable, repeatable nanoscale phase separation of the polymers.

The surface morphology and phase separation of 120 nm thick polymer blend films spun on Pt/Si substrates was characterized using AFM as shown in Fig. 9.2. Fig. 9.2(a) shows the morphology of P(VDF-TrFE) thin films annealed at 135 °C, with crystalline grains about 80-100 nm in size.

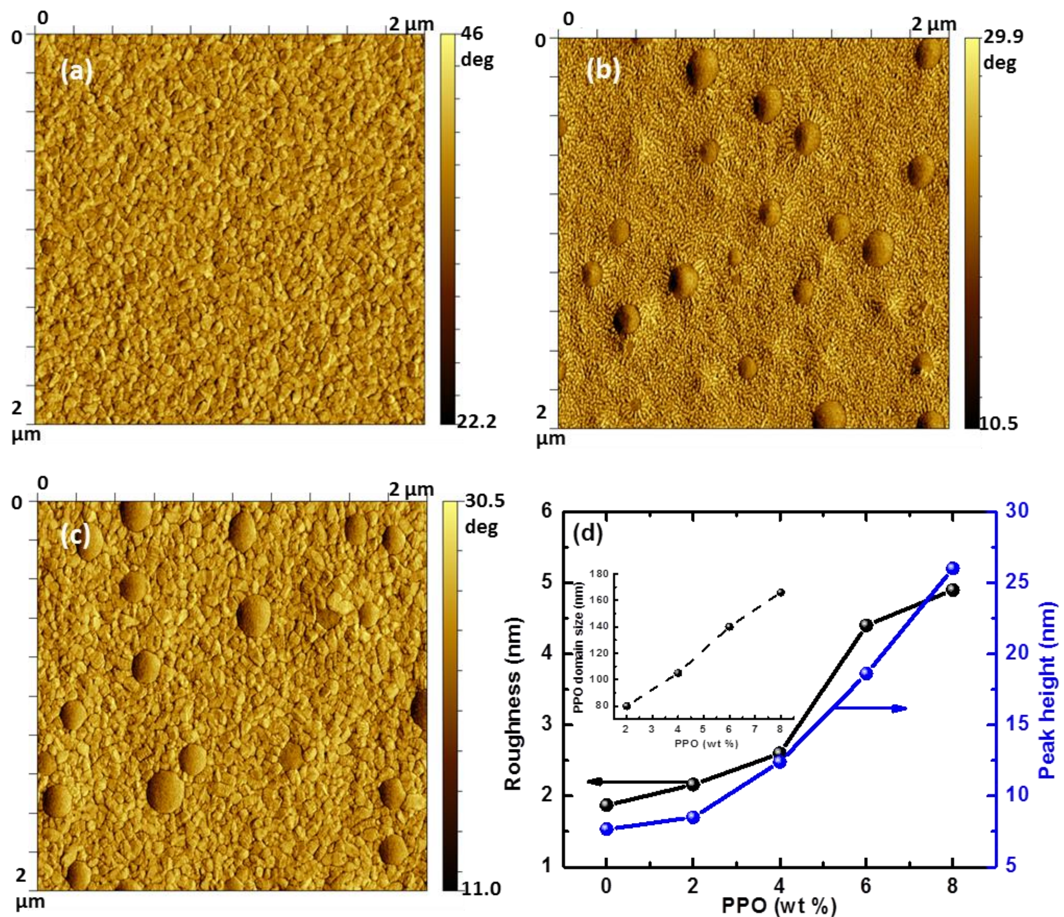

Figure. 9.2 (a) AFM phase image of pure P(VDF-TrFE) film showing island like grains in the film. (b) AFM phase image of as spun blend films with 6 wt % PPO without annealing. (c) AFM phase image of blend films with 6 wt % PPO after annealing at 135 °C, with increase in grain size of P(VDF-TrFE). (d) R_{rms} (Left) and peak height (Right) of blend films as a function of PPO loading. The inset shows average size of the PPO nanospheres as calculated from the AFM phase images.

Fig. 9.2(b) shows spun cast blend films with 6 wt % PPO. These films were not subjected to any annealing process. The blends phase separate into amorphous PPO nanospheres (~140 nm in size) randomly distributed throughout the films surrounded by the semi crystalline P(VDF-TrFE) matrix. The AFM study confirmed that phase separation for these blends was spontaneous and not thermally stimulated. Fig. 9.2(c) shows the phase image of the same blend film after annealing at 135 ºC for 4 hours. After annealing, we observe an increase in grain size of the semi crystalline P(VDF-TrFE) indicative of higher crystallinity but there is no significant change in the microstructure of PPO nanospheres or the roughness of the blend films. AFM measurements were performed as a function of blending ratio from 0 to 8 wt % PPO content. With increasing amount of PPO the average lateral size of PPO nanospheres increases in a linear fashion from ~ 80 nm in a 2 wt % films, ~ 105 nm (4 wt%), ~ 140 nm(6 wt%) and ~ 165 nm for 8 wt % film as depicted in the inset of Fig. 9.2(d). This was calculated from the AFM phase images of blend films with different PPO loadings. Furthermore the number of PPO nanospheres decreases with increasing PPO content i.e. the phase separation coarsens with increasing PPO content. These observations seem to rule out that the solidification process is due to nucleation and growth. This leads us to believe that the phase separation might be due to spinodal decomposition in which the separation occurs uniformly throughout the film and not at distinct nucleation sites. Similar observation has been made for P(VDF-TrFE) blends with other polymers [19]. Spinodal decomposition can be contrasted with nucleation and growth. There the initial formation of the microscopic clusters involves a large free energy barrier, and so can be

very slow, and may occur as little as once in the initial phase, not throughout the phase, as happens in spinodal decomposition. In the spinodal region there is no thermodynamic barrier to the reaction, thus the decomposition or phase separation is determined solely by diffusion [19]. Thus when dealing with polymer blends various factors like their molecular weight, isotropy, temperature, composition, solvent properties etc. can affect the evolution and shape of the microstructures. From a practical standpoint, spinodal decomposition provides a means of producing a very finely dispersed microstructure that can significantly enhance the physical properties of the material.

The surface roughness of ferroelectric thin films is a very critical parameter when fabricating ferroelectric memory. High surface roughness leads to non-uniform electrical field across the active layer and possibly poor yield and reproducibility for ferroelectric capacitors and low mobility and low ON/OFF ratios in ferroelectric transistors [2, 19, 20]. The measured surface roughness from the topography images (See Supplementary) of these blend films annealed at 135 ºC for 4 hours, show relatively smooth films with an increase in roughness from ~ 2 nm for pure P(VDF-TrFE) films to ~ 5 nm for a blend film with 8 wt % PPO. As seen from Fig. 9.2(d), with increasing amounts of PPO the peak height of the amorphous PPO nanospheres increases hence leading to increase in roughness. This can be further optimized and improved using techniques like temperature assisted wire-bar coating which has recently been used to fabricate smooth, polymer blend thin films [10, 21].

The cross section morphology and phase separation was characterized through transmission electron microscopy (TEM) as seen in Fig. 9.3. Fig. 9.3(a) shows the cross section TEM image of a 120 nm thick pure P(VDF-TrFE) thin film. Fig. 9.3(b)-(d) show the cross sections of 6 wt % PPO blend film sandwiched between Pt and Au electrodes at different locations. The TEM images confirm the morphology of these blend films consists of phase separated nanospheres of amorphous PPO, surrounded by a ferroelectric P(VDF-TrFE) matrix as seen by AFM. The observed phase separation was seen in multiple locations throughout the film, as shown in Fig. 9.3(c) and 9.3(d).

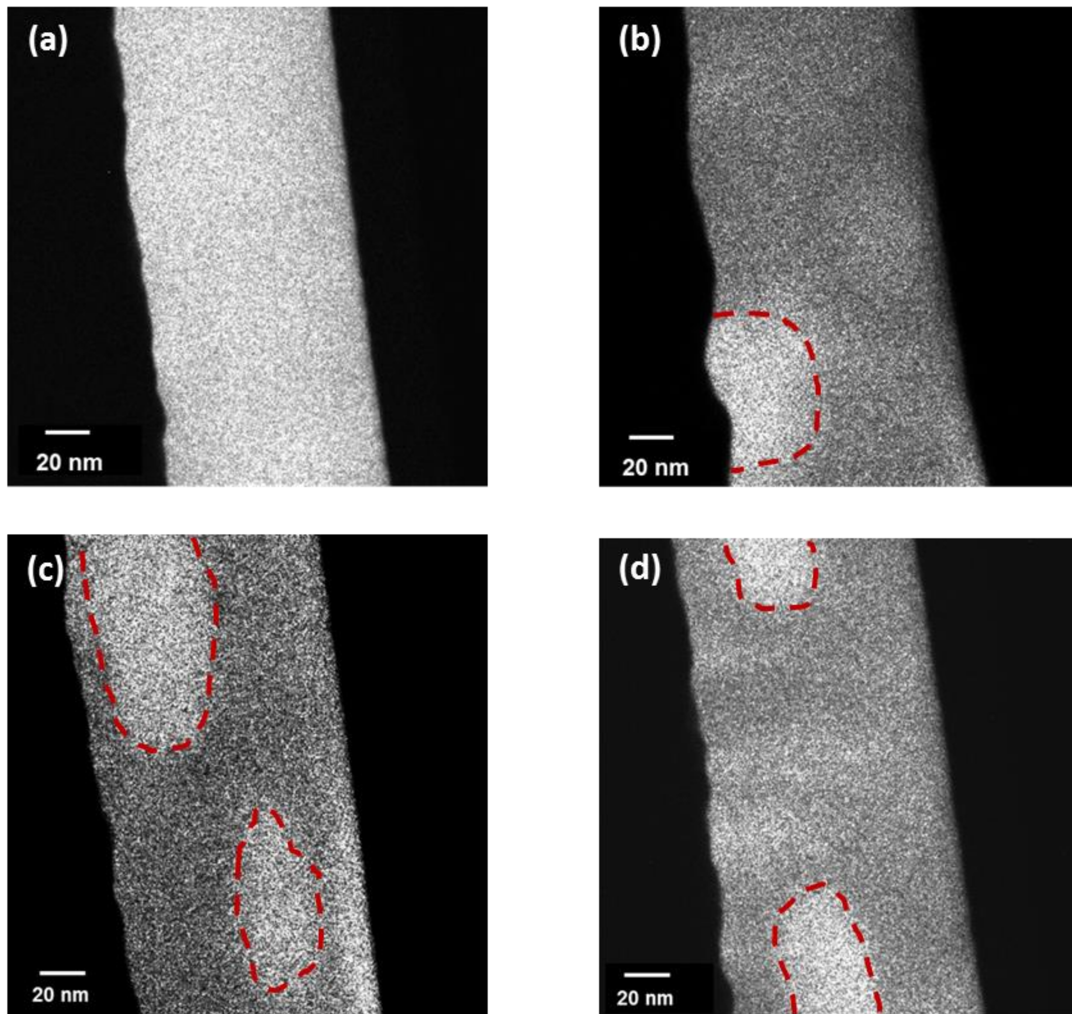

Figure. 9.3 Cross section TEM images of pure P(VDF-TrFE) films (a) and blend films with 6 wt % PPO (b,c,d) .

ii. Crystal Structure and Orientation

Fig. 9.4(a) shows the Grazing Incidence X-ray diffraction (GIXRD) spectra which was used to study the crystal structure of pure ferroelectric P(VDF-TrFE) and the polymer blends with PPO. Pristine P(VDF-TrFE) films spun on Pt electrodes and

annealed at 135 ºC exhibit a peak centered at 2θ ~ 19.78°, characteristic of the ferroelectric β phase and reflection from the (110) and (200) planes [1, 22, 23]. The inter-planar distance was calculated to be approximately 4.48 Å and is consistent with earlier reports [22, 24]. The broad peak is typical of a semicrystalline polymer like P(VDF-TrFE) comprising of crystalline lamella and amorphous regions. It's very important to have highly crystalline ferroelectric thin films as only the β-crystalline regions in the films give rise to ferroelectricity because the dipole moments in the amorphous regions will be random and cancel out each other [2]. X-ray diffraction is the primary technique to determine crystallinity of semicrystalline polymers and has been previously used for P(VDF-TrFE) thin films [23]. The determination of the degree of crystallinity implies use of a two-phase model, i.e. the sample is composed of crystals and amorphous regions and no regions of semi-crystalline organization. The diffraction peak observed could be well resolved into two peaks, C (Crystalline) and NC (Non crystalline). We used a Gaussian function to get the best fitting. The degree of crystallinity can be calculated from the ratio of area under C to total area under C+N. The calculated degree of crystallinity for pure P(VDF-TrFE) was ~ 74 %, typical of very thin (~100-200 nm) P(VDF-TrFE) films [25]. Fig. 9.4(b) shows the XRD peak for blend films with 8 % PPO content. The blend films with PPO exhibit a peak slightly shifted to the right at 2θ ~ 19.9° for 8 wt % PPO films, indicating a smaller polymer chain inter-planar distance of ~ 4.45 A°. The polymer blend films phase separate and thus it is possible that with increasing PPO content there is more stress on the P(VDF-TrFE) phase leading to closer chain packing or smaller inter-planar distance. Furthermore, the XRD

peaks indicate that the polymer blend films have smaller crystallite size compared to the pristine P(VDF-TrFE) films with a larger FWHM~2°. We noticed lower crystallinity for blend films with increasing PPO content, and was approx. ~ 62 % for 8 wt% PPO films. This is typical for blend films and has been observed for P(VDF-TrFE)-PMMA blend systems as well [11, 26].

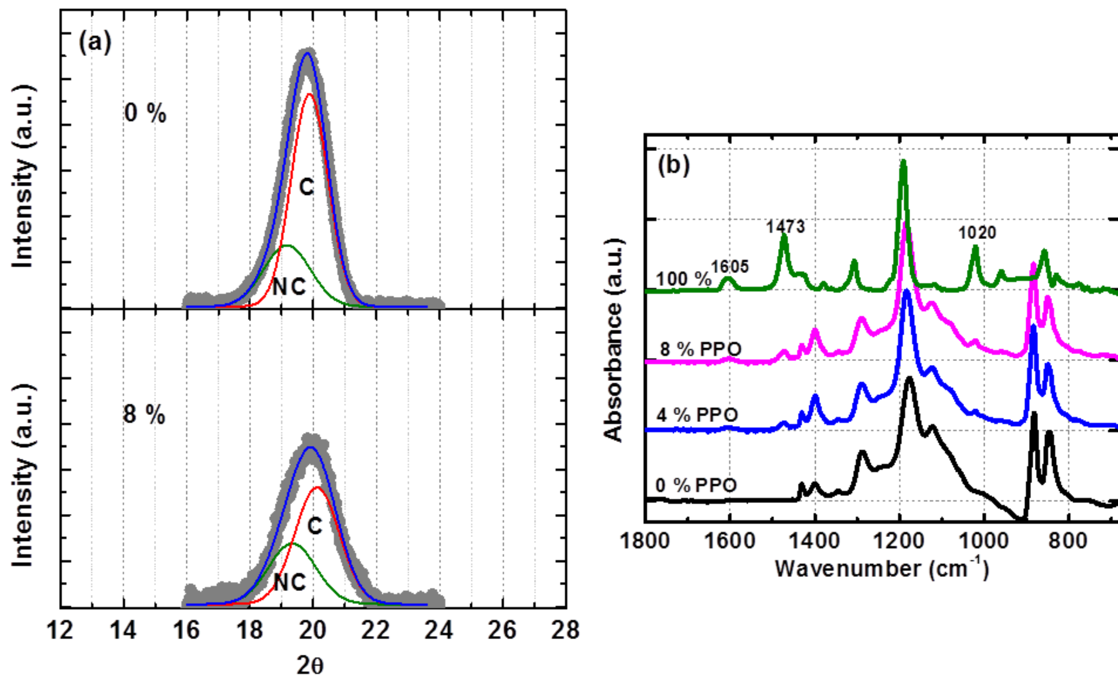

Figure. 9.4 (a) Grazing incidence XRD spectra for pure ferroelectric P(VDF-TrFE) films and blend films with 8 wt% PPO. (b) FT-IR spectra of pure ferroelectric P(VDF-TrFE) thin film, pure PPO thin film and blend films with 4 wt% and 8 wt% PPO.

The presence of PPO in thin films of the polymer blend was verified using transmission mode Fourier Transform Infra-Red (FTIR) spectroscopy. Fig. 9.4(b) shows

the absorbance bands at 1288 cm^{-1} and 850 cm^{-1} associated with CF_2 symmetric stretching vibration and are characteristic bands of the trans-zigzag formation (β phase) [22, 27, 28]. Other major peaks identified are the 1400 cm^{-1} band characteristic of the CH_2 wagging vibrations, 1186 cm^{-1} band characteristic of asymmetric stretching of CF_2 and the 880 cm^{-1} band related to the rocking CH_2 vibration [22, 27, 28]. All these peaks were common in both pristine P(VDF-TrFE) and P(VDF-TrFE)-PPO blended films. A few additional peaks were identified in the blend films at 1605 cm^{-1} characteristic of C-C=C symmetric stretching in the benzene ring, 1473 cm^{-1} from C-C=C asymmetric stretching and 1020 cm^{-1} from C-O stretching confirming the presence of ether group in PPO [17, 29, 30]. It's important to mention here that we could not detect the methyl functional groups in FTIR spectra which might be due to some overlapping with other peaks or due to the poor resolution of the FTIR equipment. FTIR analysis proves the presence of PPO in these polymer blend films but does not suggest any interaction or bonding between the PPO and P(VDF-TrFE) chains.

B. Ferroelectric and Dielectric performance of blend films

Fig. 9.5(a) shows the polarization-electric field hysteresis loops for P(VDF-TrFE)-PPO blend devices. The devices measured at 10 Hz exhibit well-saturated hysteresis curves and pure P(VDF-TrFE) capacitors show a remnant polarization ($\pm P_r$) of 7.3 $\mu C/cm^2$ and coercive field of ~ 62 ± 5 MV/m. With increasing PPO content, a monotonic decrease in remnant polarization and increase in coercive fields is observed. Blend films

with 8 wt % PPO exhibit a remnant polarization ($\pm P_r$) of 4.93 μC/cm^2 and coercive field of ~ 67 ± 5 MV/m. This effect can be attributed to the decrease in crystallinity of the films upon adding PPO, as seen from the x-ray diffraction peaks in Fig. 9.4(a).

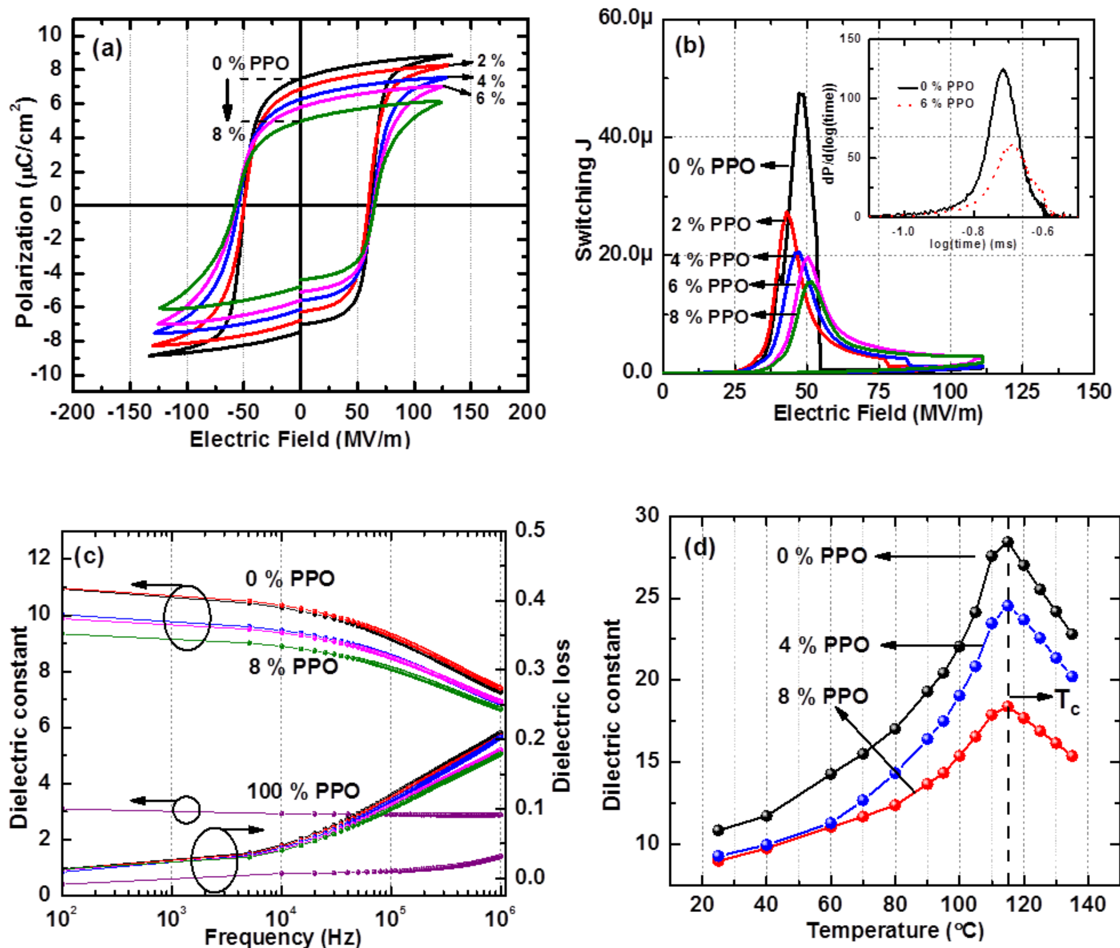

Figure. 9.5 (a) Polarization-Electric Field hysteresis loop measurements for blend films at 10 Hz as a function of amount of PPO. (b) Switching current response from blend films with 0 to 8 wt % PPO and with Platinum/ Gold electrodes. The inset shows switching characteristics for blend film at 125 MV/m, with peak of dP/d(log(t)) vs. log(t) representing respective switching times. (c) Dielectric spectroscopy study with dielectric constant (left axis) and dielectric losses (right axis) for blend films with 0 to 8 wt % PPO and pure PPO films. (d) Temperature dependence of dielectric permittivity for devices with 0, 4 and 8 wt % PPO at 1 KHz.

In ferroelectric capacitors, it is critical that the difference between switching and non-switching current is maximized to be able to distinguish the “0” from “1” memory state. Fig. 9.5(b) shows that with increasing PPO content the switching current gradually decreases. But even with high amounts of PPO content upto 8 wt %, our blend capacitors display good switching current density ~ 15 $\mu A/cm^2$; comparable to reports of pure P(VDF-TrFE) based ferroelectric capacitors [31, 32]. At the same time we measured the switching time characteristics of our P(VDF-TrFE)-PPO blend films, which can be obtained by a time domain measurement of the charge density or polarization (P) response. Switching times (τ_s) are estimated from the time of the maximum of dP/d(logt) vs. log (t) plot and are plotted in the inset of Fig. 9.5(b) [33]. At applied fields of 125 MV/m, pure P(VDF-TrFE) capacitors devices exhibit switching times of 0.19 ms while devices with 8 wt % PPO have similar switching times of ~ 0.21 ms. Thus switching times do not vary significantly with increase in PPO content, another important requirement for ferroelectric memories.

One of the biggest advantages of using PVDF-based ferroelectric polymers is their high capacitance or high permittivity coming from their ability to polarize under an applied electric field. This makes it possible to fabricate devices with low operating voltages using them as a dielectric layer. A gate dielectric with high permittivity reduces the operating voltage of OTFTs effectively without the need for thickness reduction [26]. Thus, it is important to characterize the effect of PPO on dielectric dispersion of these

blend films. Fig. 9.5(c) shows the dielectric dispersion and the loss factor (tan δ) of pure P(VDF-TrFE), pure PPO and blend ferroelectric capacitors. Our P(VDF-TrFE) copolymer films exhibit a dielectric constant of ~ 11 at 100 Hz, comparable to other reports in literature [34]. A gradual decay of the dielectric permittivity (ε_r) is observed for pure P(VDF-TrFE) capacitors, consistent with the dielectric response of a polar polymer dielectric where the dipoles cannot respond to the applied field at high frequencies. On the other hand PPO exhibits a dielectric constant of ~ 3 and a dielectric response which is independent of frequency, typical of low dielectric constant polymer dielectrics. In such materials the electronic polarization is the majority contributor to the overall permittivity and its response to the frequency of the applied field is almost instantaneous. Fig. 9.5(c) also shows the dielectric dispersion of our blend capacitors. With increasing amounts of PPO, the permittivity gradually drops but is relatively high for low voltage electronic applications; an 8 wt % blend film has a ε_r ~ 9.3. Fig. 9.5(c) also shows the dielectric losses (tan δ) calculated from the ratio of the imaginary and real part of the dielectric constant indicating power dissipation from the dielectric layer. An ideal dielectric would be one with high permittivity and low losses for electronic applications. Our blend films with 8 wt % PPO show lower dielectric losses (0.17 at 1 MHz) compared with the baseline pure P(VDF-TrFE) films (0.21 at 1 MHz) resulting from the excellent insulating and low power dissipation properties of the PPO phase. Thus with small amounts of PPO, it is possible to maintain relatively high permittivity in the blend films and at the same time lower the dielectric losses.

Fig. 9.5(d) shows the temp. dependence of the dielectric permittivity of our blend films. The dielectric permittivity of our ferroelectric capacitors increases with T, reaches a maximum, then decreases. This behavior is typical of ferroelectric materials which when subjected to heating–cooling cycle undergo a ferroelectric-to-paraelectric phase transition at the Curie temperature (T_c). The curie temperature for our pure P(VDF-TrFE) films is approx. ~ 115 °C, consistent with reports in literature [24, 35]. Interestingly blend films with increasing amount of PPO don't show any change curie temperature. This is typical of phase separated thin films and has been observed for P(VDF-TrFE) and PMMA blend system as well [11, 14].

C. Thermal stability of blend films

Large scale integration of ferroelectric memory based on the copolymer P(VDF-TrFE) remains a big challenge due to its poor thermal stability [3]. We have studied the thermal stability of our pure and blend capacitors with 8 wt % PPO content. The devices were evaluated based on their ability to switch polarization at an applied field of 125 MV/m and a frequency of 10 Hz. Fig. 9.6(a) shows the measured remnant polarization and coercive field vs. temperature. In general, a slight increase in polarization and decrease in E_c is observed with increasing T, since the elevated temperatures supply some the required energy to switch the dipoles [36]. Thermal stability of PVDF and PVDF based ferroelectric polymers is directly related to the Curie temperature of these polymers as these polymer undergo a ferroelectric-paraelectric transition at the Curie

temperature [24]. Interestingly we noticed a rapid deterioration in stability of our pure P(VDF-TrFE) thin film capacitors at only 50 °C. This is consistent with other reports for thin film P(VDF-TrFE) capacitors that the P_r decreases notably at 50 °C and rapidly deteriorates at even higher temperatures [3]. This was surprising as it is still way below the curie temperature of ~ 110-120 °C for a 70/30 molar ratio copolymer [35, 36].

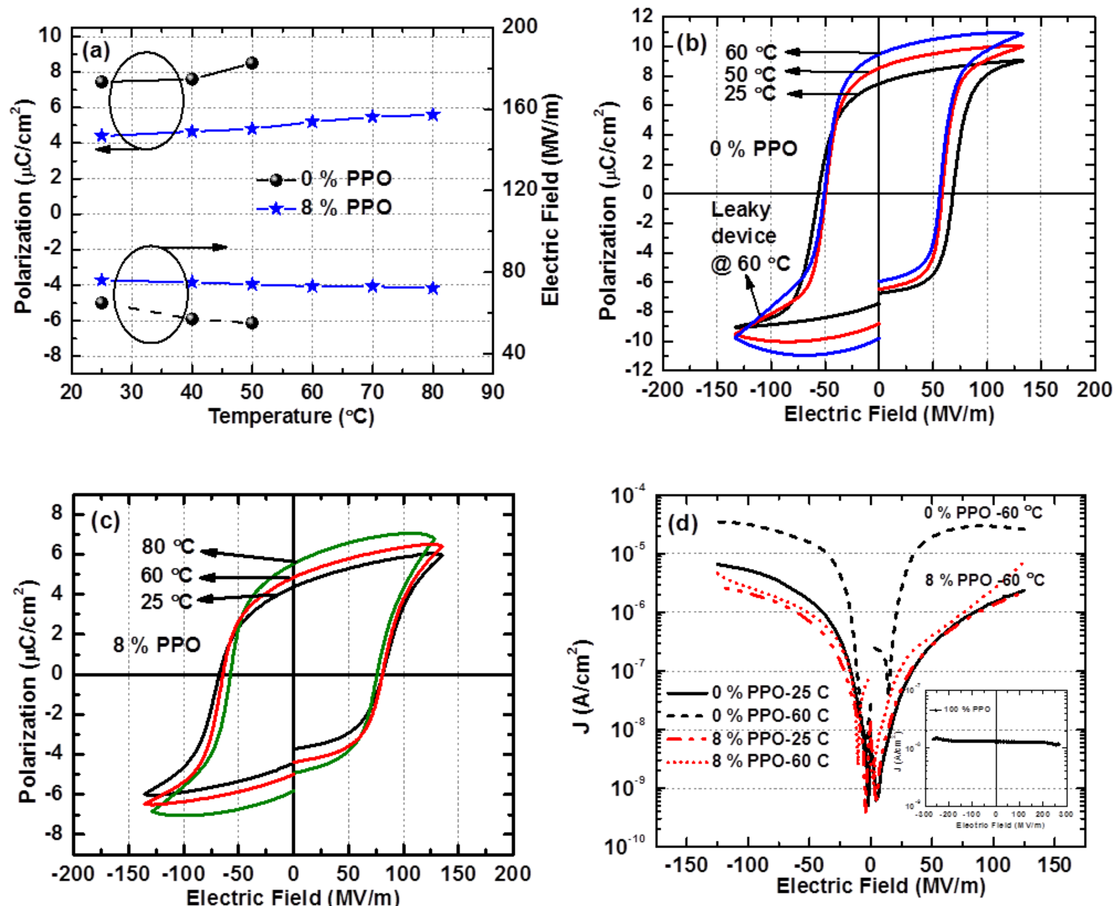

Figure. 9.6 (a) P_r and E_c as a function of temperature for pure P(VDF-TrFE) films and blend films with 8 wt % PPO. (b) P-EF hysteresis loop measurements for pure P(VDF-TrFE) films at 10 Hz as a function of T. (c) P-EF hysteresis loop measurements for blend films with 8 wt % PPO at 10 Hz as a function of T (d) Current density-Electric Field measurements of blend films (0, 8 wt % PPO) at 0 °C and 60 °C. The inset shows the leakage J of pure PPO device with Pt-Au electrodes.

In contrast, blend films with 8 wt % PPO, showed much better thermal stability compared to pure P(VDF-TrFE) capacitors. The devices perform well upto 80 °C which are closer to curie temperature of the copolymer. The improvement in thermal stability cannot come from change or increase in curie temperature of the blend films as seen in Fig. 9.5(d). Fig. 9.6(b) show the hysteresis loops for pure P(VDF-TrFE) capacitors at different temperatures. We observed that at temperatures of 60 °C or above, the hysteresis loops displayed a resistive leaky behavior making it impossible to accurately determine polarization in these films. At higher temperatures we noticed very leaky curves especially in the negative bias regime, indicative of surface breakdown at one of the electrode/ferroelectric interfaces. In contrast the blend films with PPO show better saturated curves at high temperatures as can be seen in Fig. 9.6(c).

To further understand this we studied the leakage current of pure P(VDF-TrFE) films and blend films as a function of temperature. Leakage of ferroelectric capacitors based on the copolymer has been well studied and shows a relatively high leakage for thin films around 100 nm [22, 37]. The introduction of TrFE is very effective in obtaining the ferroelectric β phase in the copolymer but also leads to larger leakage current. If we apply an electric field to switch polarization, current leakage occurs easily at the TrFE monomer because two fluorine atoms opposite from the carbon atoms of the TrFE monomer cause a current leak path [37]. This is very evident for thin films P(VDF-TrFE) capacitors with high TrFE content and several studies have reported large leakage

issues. Fig. 9.6(d) shows that at saturation fields of ~ 125 MV/m pure P(VDF-TrFE) capacitors show leakage current density in excess of 10^{-6} A/cm^2 at room temperature. On the other hand pure PPO films display low leakage current of ~10^{-8} A/cm^2 even at high fields ~ 300 MV/m further highlighting the excellent insulating properties of PPO. The blend devices with 8 wt % PPO show similar leakage currents with slightly lower currents on the negative bias. We believe its because of current conduction through the more leaky majority ferroelectric phase. More importantly what we noticed a drastic improvement in leakage current of the blend films compared to pristine P(VDF-TrFE) films at higher temperatures of 60 °C. This leakage current density of the blend films does not change much with temperature and is an order of magnitude lower than P(VDF-TrFE) films at 60 °C. We believe that the highly insulating amorphous nanospheres of PPO in the blend films acts as good charge trap regions and do not allow charge carriers to move freely through the film. This directly affects thermal stability of these blend films leading us to reliably switch the polarization even at elevated temperatures.

D. Fatigue endurance and breakdown strength of blend films

Polarization fatigue is the reduction of amount of switchable polarization with repeated switching cycles and still remains an elusive problem for the ferroelectric copolymer. The fatigue characterization of the copolymer is rather complicated since it depends on many parameters such as the thickness of film, molar ratio of the

copolymer, frequency of stress waveform, applied field, temperature and electrodes of the capacitor [5].

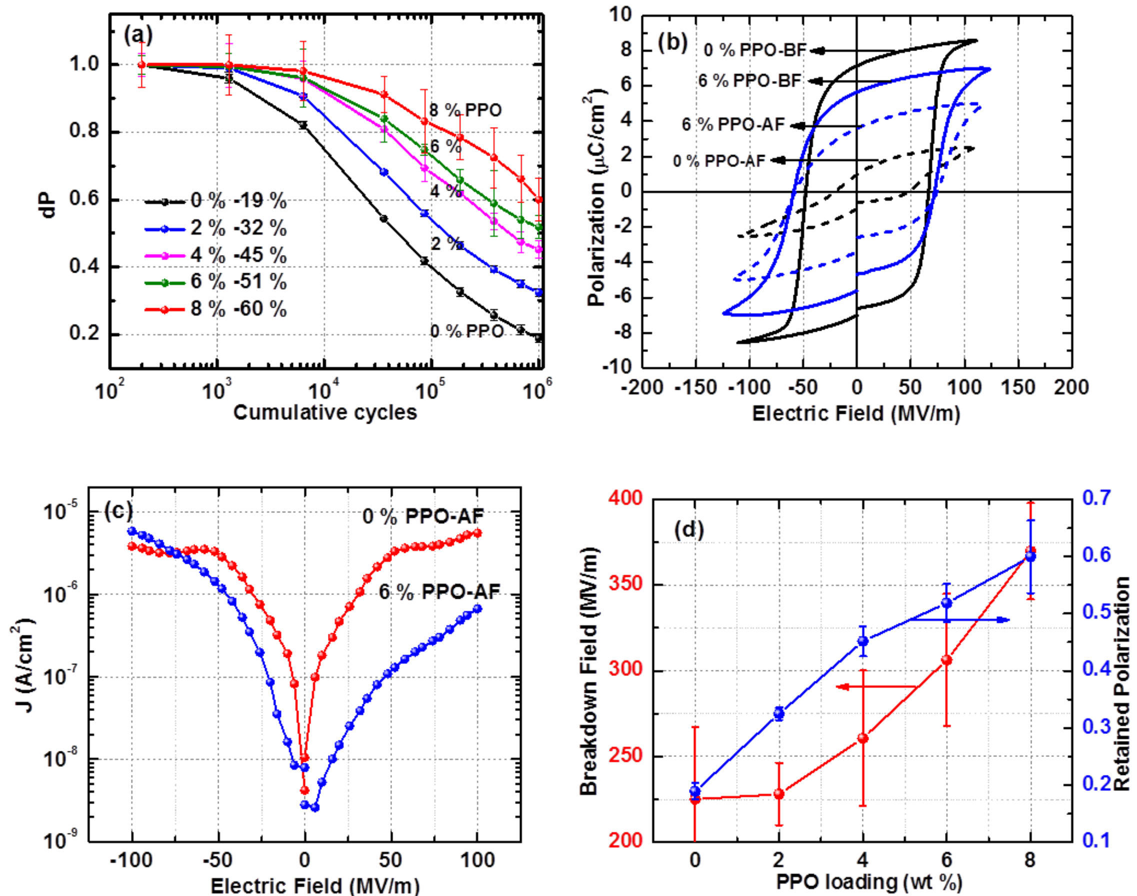

Figure. 9.7 (a) Electrical fatigue properties showing relative polarization of blend films with 0 to 8 wt % PPO. The films were stressed at 100 MV/m and a frequency of 100 Hz and the PUND measurements were done at saturation fields of 125 MV/m and 100 Hz. (b) Polarization-Electric Field hysteresis loop measurements for pure P(VDF-TrFE) films and 6 wt % PPO films before (BF) and after fatigue (AF), characterized also at 100 Hz. (c) Current density-Electric Field measurements of pure P(VDF-TrFE) films and 6 wt % PPO films after fatigue upto 106 cycles at 100 Hz (d) Dielectric breakdown strength (Left) and Fatigue or polarization retention after 10^6 cycles (Right) as a function of amount of PPO in blend films.

Here we report the fatigue performance of our capacitors with common Pt and Au electrodes under relevant and correct conditions [5, 8]. Fig. 9.7(a) shows the fatigue performance of our P(VDF-TrFE)-PPO blend film capacitors upto a million (10^6) cycles. A bipolar triangular waveform with an electric field of 100 MV/m and 10 ms pulse width (100 Hz) was applied to fatigue the devices. The polarization was characterized periodically with a Positive-Up-Negative-Down (PUND) measurement at 125 MV/m at the same frequency. We observed a gradual improvement in the fatigue performance of our blend devices with increasing PPO content. With approx. 8 wt % PPO, the devices retain ~ 60 % of the polarization after 10^6 cycles, which is a tremendous improvement from pure P(VDF-TrFE) capacitors which only retain ~ 20 % of the polarization. Fig. 7(b) shows the hysteresis curves at 100 Hz measured before and after fatigue cycles. We can see that the polarization decreases sharply from ~ 7 $\mu C/cm^2$ to only 1 $\mu C/cm^2$ for pure P(VDF-TrFE), while for 6 wt % PPO films the polarizations drops marginally from ~ 5.6 $\mu C/cm^2$ to ~ 3.6 $\mu C/cm^2$. The devices were also fatigued at a higher frequency of 1 KHz which is close to the maximum frequency at which we can switch the polarization of our copolymer films. Even at higher frequencies the films with 8 wt % PPO show excellent polarization retention of ~ 80 % after 10^6 cycles compared to 54 % for pure P(VDF-TrFE) films. The frequency dependence of fatigue performance for ferroelectric memory has been well studied before with devices showing better fatigue performance at higher frequencies [5]. It has been proposed that fatigue in P(VDF-TrFE) film is related to the injection of charges from electrodes which are subsequently trapped at crystallite boundaries and defects, inhibiting ferroelectric switching and leading to higher fatigue

rates [5, 8]. To further understand the fatigue mechanism we compared the current-voltage (leakage) characteristics of the pure and blend film devices after fatigue. Fig. 9.7(c) shows high leakage current through fatigued P(VDF-TrFE) film while the films with 6 wt % PPO content show much lower leakage after fatigue. This suggests that the high number of trapped charges in pure P(VDF-TrFE) films causes poor fatigue performance. The leakage current of the P(VDF-TrFE) thin films also shows an S shaped behavior at high fields, exhibiting small negative differential resistance. This phenomena has been well observed in breakdown studies of polymer dielectrics [38]. This indicates current instability in the film; a situation in which a homogeneous current distribution becomes unstable and decays into filaments [38]. The local charge and current densities are larger; leading to electrical thinning of the film. This is the reason for the lower coercive fields seen for our films after fatigue (Fig. 9.7(b)). This can also lead to a vastly increased thermal stress leading to electrode delamination also reported in literature especially with the use of unreactive metals such as Au [36]. We have also observed this during the fatigue of our pure P(VDF-TrFE) capacitors, where in some devices the top Au electrode delaminates due to the high thermal stress. Thus continuous fatigue of thin film P(VDF-TrFE) ferroelectric capacitors leads to dielectric aging and a film close to breakdown. In contrast, blend films with PPO show only a slight increase in leakage current after fatigue, due to the good insulating and charge trapping properties of the PPO nanospheres which results in better fatigue endurance. These highly insulating nanospheres in the blend films act as good charge trap regions and do not allow charges to get trapped in the ferroelectric film, thereby improving fatigue performance. In a

follow up study we also measured the dielectric breakdown strength of the blend films. Dielectric breakdown strength using short time tests where the sweeping DC voltage was applied at a ramp rate of 3 V/s to reach device failure between 10-20 seconds was performed. Fig. 9.7(d) shows that with increasing PPO content , the breakdown strength of these films improves from ~ 225 MV/m to ~ 360 MV/m for 0% PPO to 8 wt % PPO content, respectively [39]. The PPO in the blend films with its good insulating properties as well as its inherently high dielectric breakdown strength helps improve the breakdown strength of these P(VDF-TrFE)-PPO blend ferroelectric memory devices.

4. Conclusions

In summary, we have fabricated ferroelectric memory from polymer blends consisting of phase-separated ferroelectric P(VDF-TrFE) and highly insulating amorphous Polyphenylene oxide (PPO). The morphology of these blend films consists of phase separated nanospheres of amorphous PPO, surrounded by a crystalline ferroelectric P(VDF-TrFE) matrix. The highly insulating amorphous nanospheres of PPO in the blend films acts as good charge trap regions and do not allow charge carriers to move freely through the film. This directly affects the ferroelectric and dielectric performance of the devices. The blend devices display highly improved ferroelectric and dielectric performance with low dielectric losses (< 0.2 up to 1 MHz), enhanced thermal stability (~ up to 353 K), excellent fatigue endurance (80 % retention after 10^6 cycles at 1 KHz) and high dielectric breakdown fields (~360 MV/m). The blend devices provide a solution

to some of the important limitations of ferroelectric memory based on the copolymer, making ferroelectric memory devices based on these blends more suitable for flexible and transparent electronic applications.

CHAPTER 9 REFERENCES

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CHAPTER 10

High Performance Low Temperature Flexible Single and Dual Gate Hybrid p-type Ferroelectric Memory

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Abstract

Here, we report for the first time a hybrid organic/inorganic flexible ferroelectric memory transistor using transparent p-type SnO and P(VDF-TrFE). A record mobility of 2.7 $cm^2V^{-1}s^{-1}$, large memory window (~ 18 V), low sub threshold swing (~ −4 $Vdec^{-1}$) and excellent retention characteristics up to 3500 sec have been achieved with devices fabricated at low temperatures (200 ^oC). The mobility achieved in our devices is 10 times higher than previous reports on polymer-based p-type ferroelectric field effect transistors (FeFETs). Furthermore dual gate FeFET's were fabricated for controlling the threshold voltage and with lower gate leakage currents.

1. Introduction

Ferroelectric capacitor memories make use of the hysteresis behavior by associating $+P_r$ and $–P_r$ states with Boolean 1 and 0 logic states. The problem with using ferroelectric capacitors is that they suffer from destructive read-out, as the voltage applied to read the information can erase it as well [1-3]. Ferroelectric transistor (FeFETs) memories solve this problem as they provide resistive switching that can be sampled at low voltages without affecting the ferroelectric polarization. Historically, polymer FeFETs have suffered from poor performance due to inherent low carrier mobility, low on-to-off current ratios, poor data retention characteristics and high operating voltages [4-6].

Almost all previous reports about organic FeFETs based on small molecule semiconductors have used p-type pentacene [4, 7]. As noted by several authors, combining pentacene with P(VDF-TrFE) is problematic due to the high surface roughness of P(VDF-TrFE) thin films [5]. It is deemed impossible to avoid this interface roughness problem by reversing the layer order, i.e., by depositing the P(VDF-TrFE) on top of the pentacene. The organic solvents that would be required for the deposition of P(VDF-TrFE) onto pentacene are known to be detrimental to the pentacene surface. As a result, the reported mobilities are relatively low. The highest mobility attained thus far in pentacene based FeFETs is about 0.1 $cm^2V^{-1}s^{-1}$ [8-10]. Similarly even upon using other p-type polymeric semiconductors like MEH-PPV [11], TIPS pentacene [12], and rr-P3HT [13] the mobility in FeFETs is usually $<< 1$ $cm^2V^{-1}s^{-1}$. The weaknesses of a low field-effect

mobility, an unsatisfactory ambient stability and a difficult device integration with the polymer based FeFETs seriously restricts the real application within narrow limits.

Recently the community has adopted organic–inorganic hybrid-type nonvolatile memory thin-film transistors using an organic ferroelectric gate insulator and an oxide semiconducting active channel [3, 9, 14]. This is a very promising solution to the memory devices having both features of low-cost and high-performance, which can be embedded into the next-generation flexible and transparent electronics. Actually, oxide channel TFTs have recently attracted huge interest for use in the active matrix (AM) backplane of liquid-crystal display (LCD) and organic light-emitting diode (OLED) display [1]. TFTs employing the oxide semiconductor channel show such beneficial features as high field-effect mobility, excellent uniformity, robust device stability, transparency and can be deposited at low temperatures on plastic substrates for flexible electronic applications [2, 15].

Thus it seems reasonable to try hybrid organic-inorganic approach using oxide semiconductors and ferroelectric polymers to fabricate high performance and low cost non-volatile memory. There have been a few studies reporting hybrid ferroelectric memory with much improved performance compared to their polymer counterparts [3]. Field effect mobility > 30 $cm^2V^{-1}s^{-1}$ has been achieved in both rigid and flexible devices using ZnO-based semiconductors [14, 16]. Nevertheless, all reports on oxide semiconductor/organic ferroelectrics exhibit unipolar n-type conduction. From a performance point of view, however, complementary metal oxide semiconductor

(CMOS) logic is crucial. The advantages compared with unipolar logic are low power consumption and dissipation, higher operating frequencies, good noise margin, and robust operation. Thus the development of high performance memory with both n and p-type conduction is critical to fabrication of CMOS-based circuitry.

Stannous oxide (SnO) and cuprous oxide (Cu_2O) have been recently shown as promising transparent p-type oxide semiconductors by the fabrication of TFTs by different methods [17-25]. Fully transparent and flexible TFTs based on SnO processed at low temperatures (180 ^oC) have been already demonstrated exhibiting higher mobility than Cu_2O based TFTs [26]. The p-type character of SnO originates from the Sn2+ vacancies while its high hole mobility is attributed to the hybridized Sn 5s and O 2p orbitals near the valence band maxima [27, 28]. With an optical band gap, E_G, ~ 2.7 to 2.9 eV [24-26, 28] (compared to E_G ~2.1 of Cu_2O) [19, 20] and demonstrated field effect mobility as high as 6.75 $cm^2V^{-1}s^{-1}$, SnO is advantageous to be used as p-type semiconductor in the emerging field of transparent electronics [26].

In this study we report high performance flexible non-volatile memory devices using transparent p-type SnO. Our hybrid non-volatile ferroelectric memory devices fabricated on polyimide substrates consists of p-type SnO as the oxide channel and P(VDF-TrFE) as the gate dielectric, as shown in Fig. 10.1(a). To the best of our knowledge this is the first report of p-type oxide ferroelectric memory transistor. We have fabricated the memory devices at low temperatures (~200 ^oC) on both rigid and flexible substrates. Our devices show very high mobility (~ 2.7 $cm^2V^{-1}s^{-1}$), large memory window

(~ 18 V), low SS (~ −4 $Vdec^{-1}$), low operating (after switching) voltages (~ -1 V) and excellent retention characteristics up to 3500 sec. Our hybrid devices show mobility which is an order of magnitude (10 times) higher than previous reports on p-type FeFETs.

Furthermore we have also fabricated dual gate FeFET's using SnO as the active channel layer and with Si_3N_4 as the bottom dielectric, as shown in Fig. 10.1(b). Using a dual gate structure it is possible to control the threshold voltage (V_{th}) and with lower gate leakage current (I_g). For any envisioned application, control of the threshold voltage is essential. For logic gates, the threshold voltage determines the trip point, which is the input bias at which the gate inverts the output signal. For sensing applications, the threshold voltage signifies the bias at which the largest change in current occurs, i.e. the point of the highest sensitivity. We were able to shift the V_{th} from 6 V to 12 V and lower the gate leakage current from 30 nA to 2 nA.

2. Experimental

The hybrid FeFET's were fabricated in a top gate structure on flexible polyimide films. The 30 nm thick SnO active layer was deposited by DC reactive magnetron sputtering from a 2" metal target, at room temperature, at a deposition pressure of 1.8 mTorr, relative oxygen partial pressure of 9%, and power density of 9.55 W/in^2. Source and drain electrodes (10nm Ti, 40 nm Au) were electron-beam evaporated. The stack

was annealed at 200 ^{o}C after source and drain deposition in order to crystallize the SnO active layer. P(VDF-TrFE) copolymer (70-30 mol %) powder was dissolved in Dimethyl Formamide (DMF) to get a 4 wt.% solution. The filtered solution was then spun on the PEDOT:PSS film at 4000 rpm for 60 s followed by a soft bake for 30 min at 80 ^{o}C. The films were then annealed in vacuum at 130 ^{o}C for 2 h to improve the crystallinity. The resulting P(VDF-TrFE) film thickness was approx. ~280 nm. Aluminum top gate electrodes were thermally evaporated to complete the stack. Layers of the device were patterned by conventional photolithography technique and lift-off process. In order to prevent damage to the ferroelectric layer, methanol was used for lift-off. The dual gate FeFET's were fabricated with the same process but on Si_3N_4 coated Si substrates for the bottom dielectric and gate respectively.

Devices were measures on a probe station at ambient conditions, in the dark, using a Keithley 4200 semiconductor parameter analyzer. The performance of the FeFET's was evaluated from devices with different width-to-length (W/L) ratios. Field-effect mobility (μ_{FE}) was extracted using the conventional metal-oxide-semiconductor field effect transistor model described in equation 10.1, by the trans-conductance, g_m, in the linear regime according to equation 10.2.

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \text{ for } V_{DS} < V_{GS} - V_T \qquad (10.1)$$

where C_{ox} is the capacitance per unit area of the gate insulator

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \approx \frac{W \mu_{FE} C_{ox}}{L} V_{DS} \quad (10.2)$$

The subthreshold swing (SS) was calculated by the inverse of the maximum slope of the transfer characteristics in the subthreshold region according to equation 10.3.

$$\mathrm{SS} = \left(\frac{\mathrm{d(logI_{DS})}}{\mathrm{dV_{GS}}} \bigg|_{\mathrm{max}} \right)^{-1} = \frac{\mathrm{ln(10)nkT}}{\mathrm{q}} \quad (10.3)$$

The capacitance density of the ferroelectric layer was measured by the well-known parallel plate capacitor method using Ti/Au as the bottom electrode and Al as top electrode for consistency, yielding a C_{ox}=40 nF cm^{-2} at a frequency of 100 Hz. The on-to-off current ratio was calculated at V_{GS}=0 V and the memory window as the difference in the on voltage of the positive-going and negative-going scans. The film thicknesses were measured using a Veeco Dektak 150 surface profilometer and confirmed by cross-sectional transmission electron microscopy (TEM) analysis performed with a FEI Titan ST. High-resolution X-ray diffraction patterns were obtained at room temperature in air by a Bruker D8 Discover diffractometer using the $CuK_{\alpha 1}$ (1.5406 Å) radiation. Surface morphologies were imagined by an Agilent 5400 SPM AFM system.

3. Results and Discussion

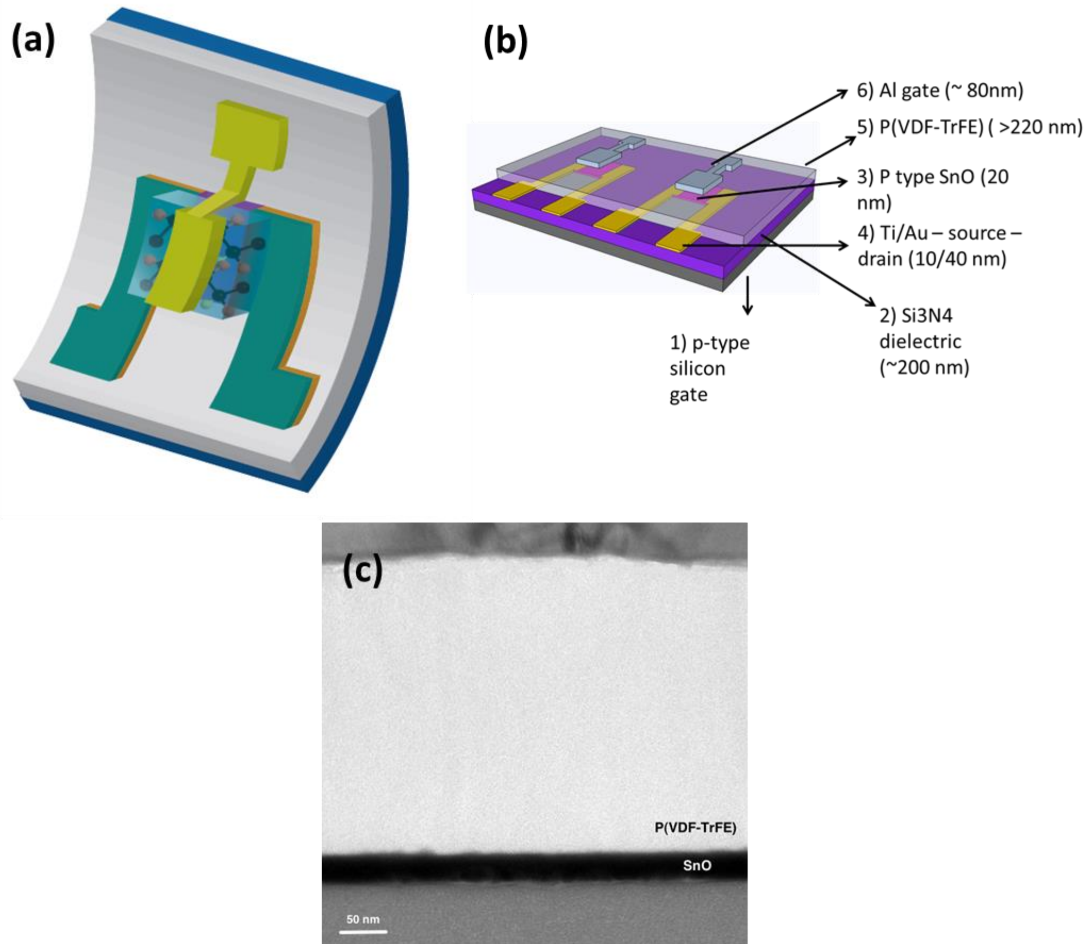

Figure. 10.1 (a) Top gate SnO-P(VDF-TrFE) FeFET on polyimide (b) Dual gate FeFET's with Si_3N_4 and p-type Silicon as bottom dielectric and gate. (c) TEM image of the SnO/P(VDF-TrFE) interface.

Fig. 10.1(a) show the conceptual design of the top gate/top contact FeFETs on polyimide films. Bottom gate devices could not be fabricated, as the sputtering process and annealing process required for the oxide channel would be detrimental to the polymer ferroelectric dielectric. The entire fabrication process was carried out at low temperatures of 200 ^{o}C, compatible with flexible substrates. The detailed fabrication steps are described in the experimental section above. Dual gate FeFET's were also fabricated on Si_3N_4 coated p-type Si substrates, as shown in Fig. 10.1(b). Fig. 10.1(c) shows a cross-sectional transmission electron microscopy (TEM) of the semiconductor/ferroelectric interface. P(VDF-TrFE) grows nicely on the flat surface of SnO without causing any damage to the oxide layer, and what is achieved by the use of dimethyl-formamide (DMF) as the P(VDF-TrFE) solvent instead of Methyl-Ethyl-Ketone (MEK) which damaged the SnO preventing the fabrication of working devices.

Fig. 10.2 shows the characteristics of the flexible top gate FeFET with a width-to-length ratio (W/L) of 5 and a channel length, L=100 µm. Fig. 10.2(a) shows the transfer characteristic of the FeFET at V_{ds} = -1 V (Linear regime) while Fig 10.2(b) shows transfer curves at different V_{ds}. P-type conduction is observed since holes are generated when a negative gate voltage (V_{GS}) is applied. The arrows in the transfer characteristics show the clockwise hysteresis of the drain current (I_{DS}) originated from the ferroelectric nature of the P(VDF-TrFE) and not arising from the charge trapping mechanism [10].

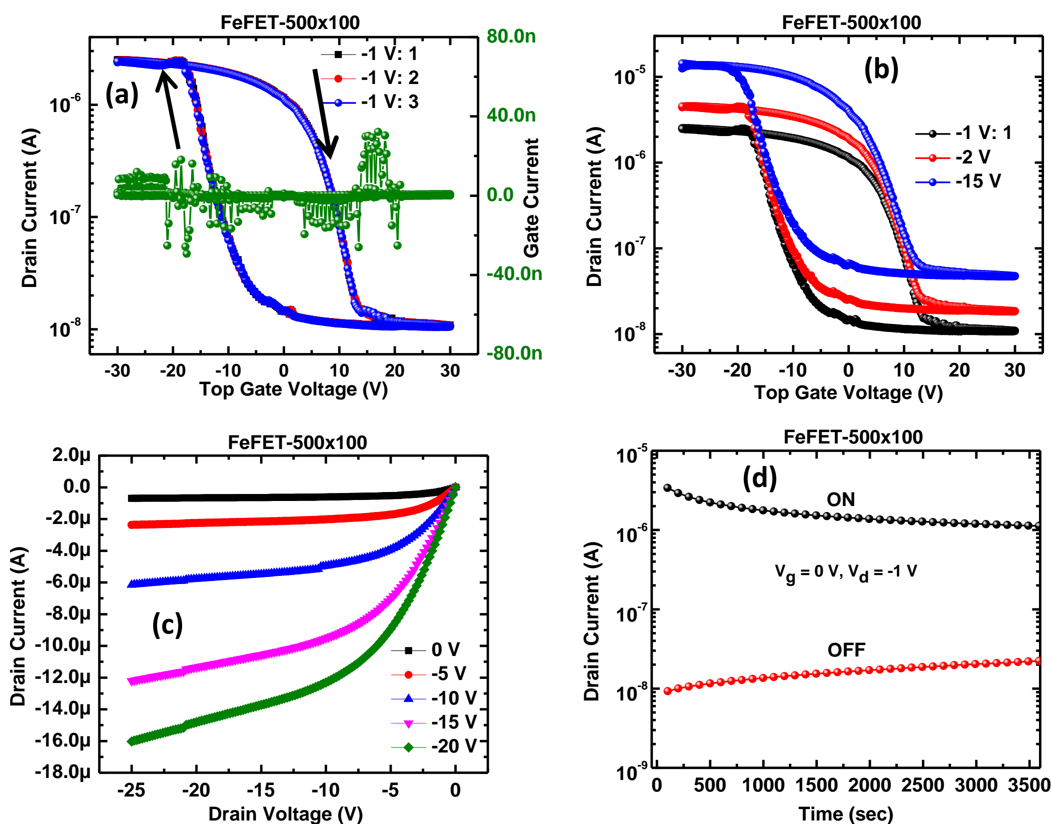

Figure. 10.2 SnO/P(VDF-TrFE) FeFET characteristics on polyimide. (a) Transfer characteristics at V_{DS}=-1V (Linear) and gate leakage current (Right Axis) (b) Transfer characteristics at different V_{DS}= -1 V (Linear) to -15 V (Saturation) (c) Output characteristics from V_{GS}=0 V to -20 V at -5V steps (c) Retention Characteristics. The ON/OFF states were produced at gate voltages of -30/+30 V with a 1 sec pulse and the retention was measured at zero gate bias condition.

Field effect mobility (μ_{FE}), calculated in the linear regime, of 2.7 $cm^2V^{-1}s^{-1}$ was obtained, which to our knowledge, are the highest mobility values reported for any transparent p-type semiconductor and which are one order of magnitude higher than previously reported FeFETs based on p-type organic semiconductors [8-10]. On-to-off

current ratio (I_{ON}/I_{OFF}) measured at V_{GS}=0 V was found to be ~ 10^2 and mainly limited by the relatively high gate current (I_G) of 10^{-8} amps (Right axis of Fig. 10.2(a)), seriously impacting the FeFETs off current. On the other hand, subthreshold swing (SS) of 4 V dec^{-1} is obtained, which is relatively lower to reported SnO TFTs using an oxide gate dielectric [21, 26]. A memory window, calculated from the shift in the on voltage (V_{ON}) of the negative-going scan (accumulation mode) and the positive-going scan (depletion mode) of 18 V is observed for the FeFETs. Clear linear and saturation regions can be observed in the output characteristics shown in Fig. 10.2 (c). The absence of current crowding at low source-to-drain voltage (V_{DS}) indicates a good ohmic contact between the SnO and the source and drain electrodes. From a memory point of view, data retention characteristics are of paramount importance. Fig. 10.2(d) shows the retention characteristics obtained by measuring the remnant I_{DS} as a function of time for the flexible hybrid FeFET devices, respectively. The ON/OFF states were produced at gate voltages of -30/+30 V with a 1 sec pulse and the retention was measured at zero gate bias condition. Good retention characteristics are observed for these devices, as they keep an I_{ON}/I_{OFF} of around two orders of magnitude even after 3500 seconds.

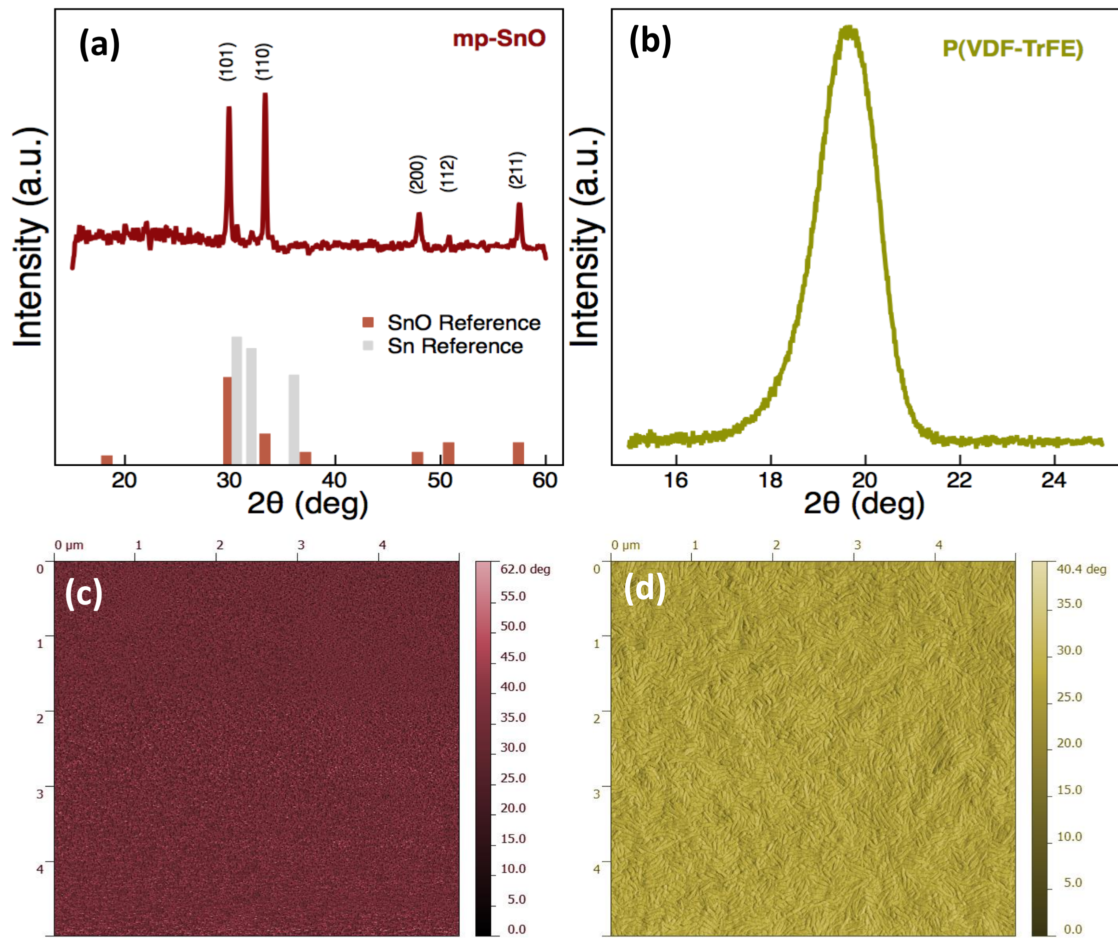

Figure. 10.3 Materials characterization. (a) XRD pattern of SnO thin films. The lines at the bottom show the diffraction patterns of tetragonal SnO (JCPDS card No. 06-0395) and tetragonal Sn (JCPDS card No. 04-0673); (b) GIXRD pattern of P(VDF-TrFE) layer (c) AFM image of the SnO surface; (d) AFM image of the P(VDF-TrFE) surface morphology.

Fig. 10.3 shows the material characterization of both the SnO active layer as well as the ferroelectric P(VDF-TrFE) layer. Fig. 10.3(a) shows the x-ray diffraction (XRD) pattern of SnO where mixed phase tin monoxide is shown. It has been previously demonstrated that the presence of metallic phase in a SnO matrix enhances mobility by promoting orbital delocalization in the valence band of SnO [26, 29]. We have used our

previously optimized deposition conditions of SnO, where the highest mobility occurs, to fabricate the FeFETs devices. The deposition conditions where maximum mobility is observed were found to be at a deposition pressure of 1.8 mTorr and relative oxygen partial pressure (OPP) of 9%, where around 3 at% metallic tin is present [26]. The SnO film is polycrystalline with an extracted crystallite size of around 12 nm. The grazing incidence (GI) XRD pattern shown in Fig. 10.3(b) shows the presence of the ferroelectric β phase of P(VDF-TrFE). The peak centered at $2\theta=19.7^{o}$ is consistent with the (100) and (200) planes yielding an inter planar distance of 4.5 Å consistent with earlier reports [30, 31]. Fig. 10.3(c) and 10.3(d) show the 5µm × 5µm atomic force microscope (AFM) phase diagrams of SnO and P(VDF-TrFE) layers respectively, deposited in the rigid substrate. The SnO films show very smooth surfaces with a root mean square roughness of ~ 1.4 nm. It’s very critical to have a smooth interface to achieve high performance devices. Previous report on bottom gate polymer FeFETs have reported poor mobility of the charge carriers due to the high surface roughness of P(VDF-TrFE) thin films [4, 5]. Inverting the stack by fabricating top gate devices can help but it’s difficult to fabricate in all polymer structures. This is because the solvent used for spin coating P(VDF-TrFE) can be detrimental to a lot of organic semiconductors [5]. This can be solved using hybrid organic/inorganic structures for achieving high mobility in FeFETs [3]. P(VDF-TrFE) grows nicely on the relatively flat SnO surface (Rms surface roughness ~ 6.18 nm) with an average grain size of ~ 160 nm, which can be clearly observed on the AFM image, consistent with earlier reports [32]. The large grains are important to get maximum polarization from the ferroelectric layer. Flexible devices show a higher surface

roughness of ~ 9.77 nm mainly attributed to the higher substrate roughness of the polyimide when compared to silicon. This difference in the surface roughness is of particular importance when comparing devices on both substrates, as it is known that large surface roughness degrades performance [4, 5, 8].

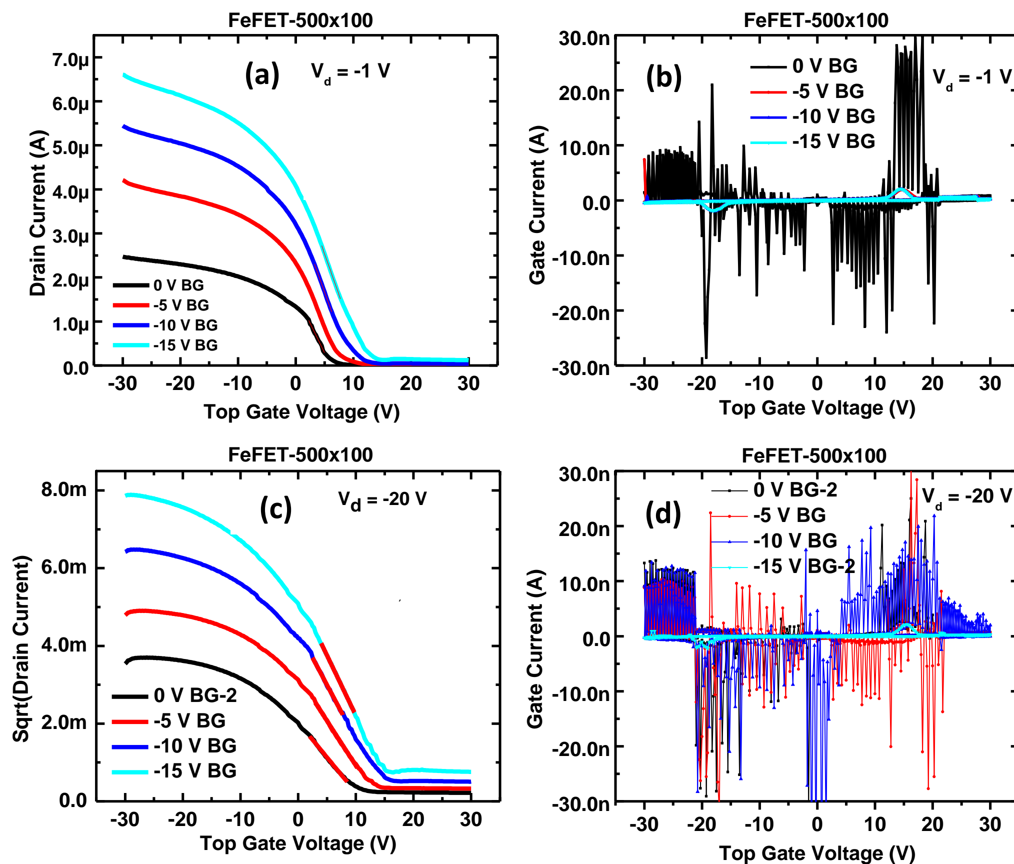

Figure. 10.4 Dual Gate FeFET characteristics. (a) Dual gate FeFET transfer curves in Linear regime (V_d= -1 V) with bottom gate (BG) negatively biased (b) Top Gate leakage curves in Linear regime (V_d= -1 V) with bottom gate (BG) negatively biased (c) Dual gate FeFET transfer curves in saturation regime (V_d= -20 V) with bottom gate (BG) negatively biased (d) Top Gate leakage curves in saturation regime (V_d= -20 V) with bottom gate (BG) negatively biased

Fig. 10.4 shows the dual gate behavior of our FeFET's. The dual gate behavior is realized by biasing both the top and bottom gate i.e. Al and p-type silicon. The linear transfer curves are shown in Fig. 10.4(a) at a drain bias of -1V. The top gate bias is swept while the bottom gate is kept at different constant negative biases. We see a shift in threshold voltages towards the positive bias side from ~ 6 V in floating gate mode to +12 V with -15 V applied at the bottom gate. Similarly with positive bottom gate bias the threshold voltages shifted to negative bias side. The data is summarized in Table 10.1 below. Fig. 10.4(b) shows the gate leakage current of the FeFET's in dual gate mode operation. The gate leakage current decreases 10 times from a max of 30 nA in floating gate mode to 3 nA with -15 V applied at the bottom gate. Similarly with positive bottom gate bias the gate current leakage decreased. The same trend is also seen in the saturation regime as seen from Fig. 10.4(c) and (d).

SnO behaves as a unipolar p-type semiconductor. The stack shown in Fig. 10.1(b) contains a bottom and a top channel as the semiconductor thickness is greater than 10 nm. When the bottom gate is negative, holes are also accumulated in the bottom channel and both channels carry current. With a positive bottom gate bias, the bottom channel is depleted of holes and only the top channel contributes. The IV characteristics then depend on the coupling between the linear bottom capacitance and the ferroelectric top capacitance.

When we apply a negative bias on the bottom gate, a bottom gate channel is formed. The bottom gate bias is fixed, so an additional constant drain current is added

to the transfer curve of the top FeFET. The bottom channel is only depleted by the top gate at a positive bias beyond the threshold voltage of the top channel. Effectively, the entire transfer curve is shifted to the right.

For a positive bottom gate bias, the curves shift to left. SnO is a unipolar p -type semiconductor, hence electrons cannot be accumulated. The net effect is that the accumulated charges in the bottom channel are depleted. Mobile charge carriers in the top channel are accumulated by the top gate, but depleted by the bottom gate when biased positively. To compensate for the bottom gate bias and to attain the original drain current at 0 V bottom gate bias, the top gate bias needs to be increased. Thus the transfer curve shifts to the left. The exact shift can be calculated using the capacitances of the two dielectrics. A detailed investigation is beyond the scope of this chapter and dissertation. The measurements are included to demonstrate the feasibility of fabricating a hybrid ferroelectric dual-gate transistor with the capability to control the threshold voltage and lower gate leakage current.

BG bias	V_{th}	Memory window	ON/OFF ratio	SS (V/dec)
-15 V	+11.8 V	21.6 V	9.2	6.84
-10 V	+9.6 V	19.6 V	$1.97E^1$	5.58
-5 V	+7.5 V	17.7 V	$5.8E^1$	5.05
0 V	+6.1 V	18.1 V	$1.08E^2$	4.0
+ 5V	+5.0 V	18.4 V	$1.5E^2$	4.25
+10 V	+4.0 V	18.0 V	$1.08E^2$	4.65
+15 V	+0.3 V	17.3 V	$7.3E^1$	4.9

Table 10.2. Important parameters for our dual gate FeFET's as a function of different bottom gate bias.

4. Conclusions

We have demonstrated the first p-type hybrid polymer/oxide FeFET on plastic substrates using P(VDF-TrFE) as the ferroelectric material. The top gate devices exhibit a high field effect mobility of 2.7 $cm^2V^{-1}s^{-1}$. Furthermore a high memory window of 18 V has been achieved along with good retention characteristics of more than 3500 seconds. Furthermore we have also demonstrated dual gate FeFETs where we can control the threshold voltages and reduce gate leakage current. These dual gate devices are very attractive in ring oscillators and 64 bit RFID transponder chips and biosensors. Further

device engineering, such as semiconductor thickness optimization and the use of interfacial layer are required to enhance the device performance. The demonstration here of the first p-type oxide SC/organic ferroelectric thin film transistor with superior device performance and low process temperature, opens the door for the development of CMOS-based non-volatile memory devices for the emerging transparent and flexible applications.

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CHAPTER 11

Summary of Dissertation

The work done during the course of this dissertation highlights the potential of polymer ferroelectric memory for flexible electronics applications. There is market opportunity for polymer ferroelectric memory to be used in niche applications like smart cards, RFID tags, sensors etc. Using novel materials and device engineering we have fabricated high performance polymeric ferroelectric memory and find solutions to some of the critical problems with ferroelectric memory hindering their commercialization.

In Chapters 2-4 we fabricated solution processed all polymeric flexible and transparent ferroelectric capacitors on plastic substrates. In chapter 2 we systematically characterized the effect of polymeric electrodes on the growth, morphology, crystallinity and orientation of the P(VDF-TrFE) ferroelectric polymer versus metallic electrodes. We identified the key growth requirements and processing conditions to get the best performance out of the ferroelectric polymer. In chapter 3 we demonstrate the first ever all polymeric ferroelectric capacitors with performance as good as metal electrodes. We identify the series resistance problem when using polymeric electrodes and find by using solvent modified highly conducting electrodes it’s possible to achieve excellent dielectric and ferroelectric performance with low coercive fields, high

polarization and good dielectric frequency response. Lastly in chapter 4 we demonstrate large array of ink-jet printed polymeric ferroelectric capacitors in a cross bar geometry.

In Chapters 5 and 6 we investigated current transport mechanism in ferroelectric polymers based on an electrode study and discuss the implication of this on the degradation of the memory performance. Earlier, there have been multiple studies reporting different ferroelectric, dielectric and endurance performance of ferroelectric capacitors. Most of these studies used different electrodes such as Pt, Au, Al and ITO. In Chapter 5 we systematically attempt to characterize the charge injection characteristics and transport mechanism in P(VDF-TrFE) capacitors as a function of different electrodes such as Pt, Ag, Au and Al. Following up on our results, In Chapter 6 we demonstrate how by using electrode engineering it's possible to fabricate ferroelectric capacitors with highly improved fatigue characteristics.

In Chapters 7 and 10 we demonstrate high performance p-type FeFET's with record mobilites. In Chapter 7 we demonstrate the first ever polymeric FeFETs fabricated on banknotes for potential use in anti-counterfeiting circuits along with RFID technology. We demonstrate that by using planarizing layers and smooth polymeric gate electrodes it's possible to fabricate high performance pentacene based FeFET's with high P_r, low E_c, high mobility, low leakage, large memory window and high yields. In Chapter 10 we demonstrate novel hybrid oxide-polymer FeFET's using p type SnO and P(VDF-TrFE) as the ferroelectric gate dielectric. The devices were fabricated at low temperatures on both rigid and plastic substrates. The devices showed high

performance with record hole mobility of ~ 3.3 $cm^2V^{-1}s^{-1}$ which is an order of magnitude higher than previous reports.

Last but not the least in Chapters 8 and 9 we demonstrate the potential of using polymer blends for fabricating high performance ferroelectric memory. In Chapter 8 we demonstrate novel ferroelectric-semiconducting blends to fabricate the first ever all polymer ferroelectric diode. We fabricated diodes using ferroelectric P(VDF-TrFE)-n type PCBM and PEDOT:PSS electrodes. With careful solvent optimization it's possible to make high performance devices with low roughness, high on/off ratios, low read voltages and excellent retention. In Chapter 9 we fabricated high performance ferroelectric memory using novel ferroelectric-dielectric blends. By using blends with highly insulating Poly(p-phenylene oxide) it's possible to drastically improve the thermal stability, fatigue endurance and breakdown fields of ferroelectric memory.

In summary, we have used materials and device engineering to find novel solutions to some critical issues for polymer based ferroelectric memory devices. Further work needs to be done on fabricating high performance ferroelectric memory with polymeric semiconductors, decreasing the operating voltages, improving the thermal stability and large area printing of these devices. This can lead to the commercialization of polymer ferroelectric memory for applications such as RFID tags, smart cards, interactive toys and sensors.

LIST OF PUBLICATIONS

1. M.A. Khan et al., “High performance non-volatile organic ferroelectric memory on banknotes”, *Advanced Materials (2012) (IF: 14.8)*
2. M.A. Khan et al., “All-polymer bistable resistive memory device based on nanoscale phase-separated PCBM-ferroelectric blends”, *Advanced Functional Materials (2012) (IF: 9.8)*
3. M.A. Khan et al., “High performance polymeric memory based on phase-separated films of ferroelectric poly(vinylidene-fluoride-trifluoroethylene) and highly insulating poly(p-phenylene oxide)”, *Advanced Functional Materials (2013) (IF: 9.8)*
4. M.A. Khan et al., “Doped polymer electrodes for high performance ferroelectric capacitors on plastic substrates”, *Applied Physics Letters (2012) (IF: 3.8)*
5. M.A. Khan et al., “Fabrication and Characterization of all-polymer, transparent ferroelectric capacitors on flexible substrates”, *Organic Electronics (2011) (IF: 4.0)*
6. M.A. Khan, et al., “Buckled graphene: A model study based on density functional theory”, *Chemical Physics Letters (2010) (IF: 2.3)*
7. Unnat S. Bhansali, *M.A. Khan* and H. N. Alshareef, “Electrical performance of polymer ferroelectric capacitors fabricated on plastic substrate using transparent electrodes”, *Organic Electronics (2012) (IF: 4.0)*
8. Unnat S. Bhansali, *M.A. Khan* and H. N. Alshareef, “Organic ferroelectric memory devices with inkjet-printed polymer electrodes on flexible substrates”, *Microelectronics Engineering (2012) (IF: 1.5)*
9. Unnat S. Bhansali, *M.A. Khan* and H. N. Alshareef, “Metal-free, single-polymer resistive memory devices on flexible substrates”, *ACS Nano (2013) (IF: 12)*
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LIST OF PATENTS

1. M.A. Khan et al., “Use of Doped Polymer Electrodes for fabrication of high Performance Ferroelectric memory”, 12T&I0018-US-PSP2 (SB40004US2), *(Serial Number 61/705782)*
2. M.A. Khan et al., “Use of single polymer to fabricate a resistive memory device” , 12T&I0025-US-PSP *(Serial # 61/711281)*
3. M.A. Khan et al., “Use of Blends of Ferroelectric P(VDF-TrFE) and SABIC Noryl resin to fabricate ferroelectric capacitors with improved fatigue properties. (*Serial Number 61/784,011)*