Mode Matching Analysis and Design of Substrate Integrated Waveguide Components

by

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B.Sc., Iran University of Science and Technology, Tehran, Iran 2005
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ABSTRACT

The advent of Substrate Integrated Circuit (SIC) technology, and specifically Substrate Integrated Waveguide (SIW) technology has made it feasible to design and fabricate low loss and high quality factor (Q-factor) microwave and millimeter wave structures on a compact and integrable layout and at a low cost. The SIW structure is the planar realization of the conventional rectangular waveguide (RWG). In this technology, the side walls of the waveguide are replaced with two rows of metallic vias, which are connecting two conductor sheets, located at the top and bottom of a dielectric slab. The motivation for this thesis has been to develop an analytical method to efficiently analyze SIW structures, and also design different types of passive microwave components based on this technology.

As SIW structures are imitating waveguide structures in a planar format, the field distributions inside these structures are very close to those in waveguides. However, due to the very small substrate height in conventional planar technologies, and also the existence of a row of vias, instead of a solid metallic wall, there is a reduced set of modes in SIW compared to regular waveguide. This fact has given us an opportunity to deploy efficient modal analysis techniques to analyze these structures. In this thesis, we present a Mode Matching Techniques (MMT) approach for the analysis of H-plane SIW structures.

One of the areas of application, which can significantly benefit from having an efficient analytical method, is designing and optimizing new circuits. Having such an analytical tool, which is faster than commercially available field solvers by an order of magnitude, new components can be designed, analyzed and optimized in a fast and inexpensive manner. Based on this technique, various types of passive microwave components including filters, diplexers, power dividers and couplers, some of which are among the first to be reported in SIW technology, are designed and analyzed in this thesis. Also based on this technique, the most accurate formula for the effective waveguide width of the SIW is presented in this thesis.

In order to provide means to excite and measure SIW components, transitions between these structures and other planar topologies like microstrip and coplanar waveguide (CPW) are needed. More importantly, low-reflection transitions to microstrip are required to integrate SIW circuits with active components, and therefore it is vital to provide low-reflection transitions so that the component design is independent of the influences of the transitions. In this thesis, a new wideband microstrip-to-SIW transition, with the lowest reported reflection coefficient, is also introduced.

Preface

Some of the methods and results presented in this thesis have been published or have been submitted for publication as journal or conference proceedings articles. The list of the publications can be found below.

The material in Chapter 2 was published with preliminary results in *Frequenz-Journal of RF/Microwave Engineering, Photonics and Communications* in 2011 [1]. A part of the material presented in Chapter 3 is published in *IEEE Microwave and Wireless Components Letters* in 2013 [2] and the other part is in press for publication in *IEEE Transactions on Microwave Theory and Techniques* in 2014 [3]. A part of theoretical material presented in Chapter 2 with results presented in Chapter 4 is also in press for publication in the *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* in 2014 [4]. The material presented in Chapter 4 is mainly published in the Proceedings of the *Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC) Conference* in 2012 [5], the Proceedings of the *42nd European Microwave Conference (EuMC)* in 2012 [6], the Proceedings of the *7th European Conference on Antennas and Propagation (EuCAP)* in 2013 [7], [8] and in the *IEEE MTT-S International Microwave Symposium (IMS) Digest* in 2013 [9]. Also, a part of the material presented in Chapter 4 is submitted for publication to *IEEE Microwave and Wireless Components Letters*, and a part is accepted for presentation in *Asia-Pacific Microwave Conference (APMC)* in November 2014 [10].

The publications resulting from this thesis are as follows:

Journal Articles

- J. Bornemann, F. Taringou, and Z. Kordiboroujeni. A mode-matching approach for the analysis and design of substrate-integrated waveguide components. *Frequenz - J. of RF/Microwave Engr., Photonics and Communications*, 65:287-292, September 2011. ([1])

- Z. Kordiboroujeni and J. Bornemann. Designing the width of substrate integrated waveguide structures. *IEEE Microwave and Wireless Components Letters*, 23(10):518-520, October 2013. ([2])

- Z. Kordiboroujeni and J. Bornemann. New wideband transition from microstrip line to substrate integrated waveguide. *IEEE Transactions on Microwave Theory and Techniques*, 2014, In press. ([3])

- Z. Kordiboroujeni and J. Bornemann. Mode-matching analysis and design of substrate integrated waveguide T-junction diplexer and corner filter. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 2014, In press. ([4])

- Z. Kordiboroujeni and J. Bornemann. Design and analysis of a novel K-band backward substrate integrated waveguide diplexer . *IEEE Microwave and Wireless Components Letters*, 2014, Under revision.

Refereed Conference Papers

- Z. Kordiboroujeni, J. Bornemann, and T. Sieverding. Mode-matching design of substrate-integrated waveguide couplers. *Proceedings of Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC)*, pages 701-704, Singapore, May 2012. ([5])

- Z. Kordiboroujeni, F. Taringou, and J. Bornemann. Efficient mode-matching design of substrate-integrated waveguide filters. *Proceedings of 42nd European Microwave Conference (EuMC)*, pages 253-256, Amsterdam, The Netherlands, Oct./ Nov. 2012. ([6])

- Z. Kordiboroujeni and J. Bornemann. Efficient design of substrate integrated waveguide power dividers for antenna feed systems. *Proceedings of 7th European Conference on Antennas and Propagation (EuCAP)*, pages 352-356, Gothenburg, Sweden, April 2013. ([7])

- L. Locke, Z. Kordiboroujeni, J. Bornemann, and S. Claude. Substrate integrated waveguide couplers for tapered slot antennas in adaptive receiver applications. *Proceedings of 7th European Conference on Antennas and Propagation (EuCAP)*, pages 2865-2869, Gothenburg, Sweden, April 2013. ([8])

- Z. Kordiboroujeni and J. Bornemann. Mode matching design of substrate integrated waveguide diplexers. *IEEE MTT-S International Microwave Symposium (IMS) Digest*, pages 1-3, Seattle, WA, USA, June 2013. ([9])

- Z. Kordiboroujeni, J. Bornemann and T. Sieverding. K-Band substrate integrated waveguide T-junction diplexer design by mode-matching techniques. *Asia-Pacific Microwave Conference (APMC)*, Sendai, Japan, Nov. 2014. ([10])

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List of Abbreviations

2D	two-dimensional
3D	three-dimensional
AGC	Automatic Gain Control
ATSA	antipodal tapered slot antenna
BEM	Boundary Element Method
BI	Boundary Integrals
BI-RME	Boundary Integral-Resonant Mode Expansion
CPW	coplanar waveguide
DD-FDTD	Domain Decomposition Finite-Difference Time-Domain
EM	electromagnetic
EBG	Electromagnetic Bandgap
FDFD	Finite-Difference Frequency-Domain
FDTD	Finite-Difference Time-Domain
FEM	Finite Element Method
FETD	Finite-Element Time-Domain
FHMSIW	Folded HMSIW
HMSIW	half-mode SIW

LTCC	Low-Temperature Co-fired Ceramic
LRL	line-reflect-line
MMT	Mode Matching Techniques
MoM	Method of Moments
PCB	printed circuit board
PEC	perfect electric conductor
PMC	perfect magnetic conductor
PML	perfectly matched layer
Q-factor	quality factor
RL	return loss
RME	Resonant Mode Expansion
RWG	rectangular waveguide
S-parameters	scattering parameters
SIC	Substrate Integrated Circuit
SIFW	Substrate Integrated Folded Waveguide
SIIDG	Substrate Integrated Image Dielectric Guide
SIIG	Substrate Integrated Insular Guide
SIINDG	Substrate Integrated Inset Dielectric Guide
SINRD	Substrate Integrated Non-Radiating Dielectric
SISW	Substrate Integrated Slab-Waveguide
SIW	Substrate Integrated Waveguide
TE	transverse electric
TEM	transverse electromagnetic

TI	Tearing and Interconnecting
TL	thru-line
TM	transverse magnetic

Acknowledgment

During the last few years as a Ph.D. student, I was fortunate to benefit from the insight, encouragement, and support of mentors, colleagues, family members, and many dear friends.

First and foremost, I would like to express my sincere appreciation to my advisor, Prof. Jens Bornemann, for his continuous supports, insightful comments and advice throughout my Ph.D. studies. I consider myself very lucky for having him as my supervisor and I feel very fortunate to have worked with an advisor who was so involved with my research.

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To ...
my lovely mother, for her lifetime kindness and sacrifice,
my precious father, whose way of life defines honesty,
and my lovely husband, whose love makes me feel alive.

Chapter 1

Introduction

As starting point in the integration of microwave components and circuits, planar structure topologies are widely used in the design of passive microwave circuits due to their compact size, integrability and also capability of mass production. However, in such structures like microstrip lines, CPW and slot lines, due to the high current density along the open edges of the line, the conductor loss is high. Moreover, the developed circuits consist of line discontinuities which may cause radiation loss and element-to-element parasitic cross coupling [11]. In addition, as open structures, their radiation loss increases with increasing frequency [12].

In contrast, the traditional low loss waveguide structures have minimum radiation loss as they are completely shielded and the wave is totally bound inside the structure. Waveguide structures are the inevitable choice in designing high Q-factor, low loss and interference free circuits. By increasing the frequency, the physical dimensions of the waveguide decrease, but still the integration of waveguide circuits is not as easy as that of microstrip circuits and requires transitions from planar to non-planar circuits [13].

In order to integrate planar and non-planar structures, difficulties like electrical problems related to matching and bandwidth, thermal problems due to different thermal expansion coefficients between them and also mechanical problems associated with assembling and packaging aspects should be considered [11]. Therefore, hybrid methods were introduced in the early 2000 to integrate planar and non-planar structures on a same substrate [14]. Figure 1.1 shows some of these integrations, including SIW, Substrate Integrated Slab-Waveguide (SISW), Substrate Integrated Non-Radiating Dielectric (SINRD) guide, Substrate Integrated Image Dielectric Guide (SIIDG), Substrate Integrated Inset Dielectric Guide (SIINDG), and

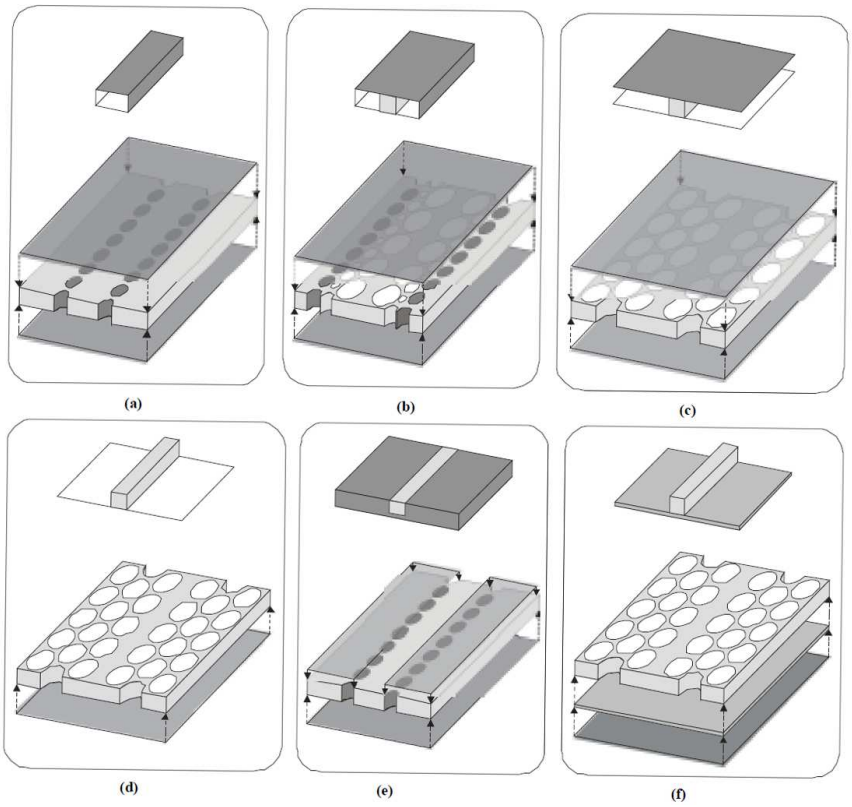


Figure 1.1: Topologies of different non-planar SIC structures: (a) SIW, (b) SISW, (c) SINRD guide, (d) SIIDG, (e) SIINDG, and (f) SIIG. Note that white circles stand for air holes and dark circles for metalized via holes. Dielectric material is colored as light gray [15] (Reprinted from ©2003 IEEE, Wu K. et al., The substrate integrated circuits - a new concept for high-frequency electronics and optoelectronics. Page 2, Copyright ©2003 IEEE, with permission from IEEE).

Substrate Integrated Insular Guide (SIIG). Our focus is on SIW structures and their MMT analysis in this thesis. Please note that among different structures presented in Figure 1.1, SIW is the best choice to apply MMT. SINRD guides can also be analyzed with MMT, however these structures are not discussed in this thesis.

1.1 Substrate Integrated Waveguide

One of the integration techniques between planar structures and waveguide structures, which has received considerable attention among microwave engineers, is SIW technology. SIW, also called laminated waveguide [16] or post-wall waveguide [17], is a terminology of a type of transmission line first introduced in 2001 [14]. In this

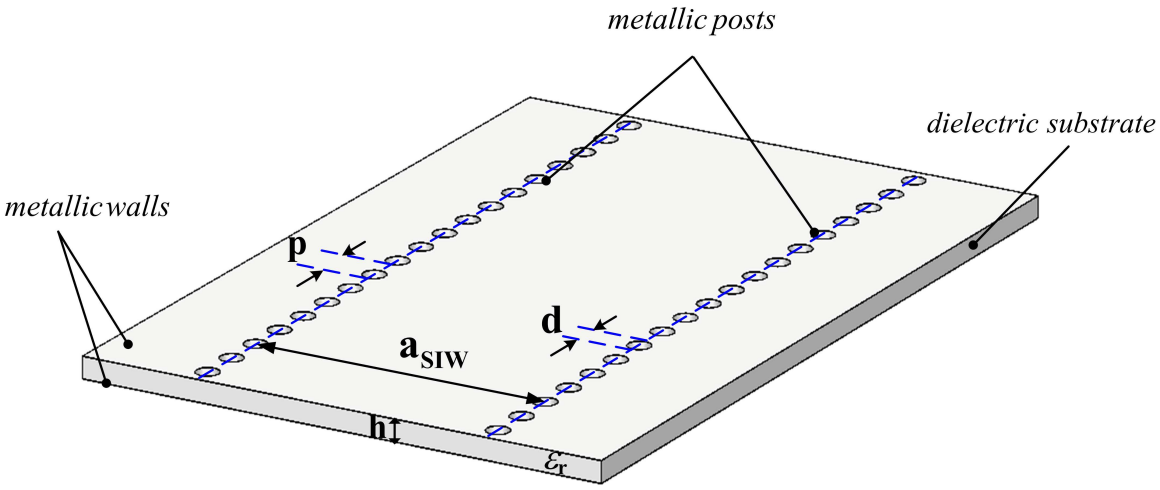
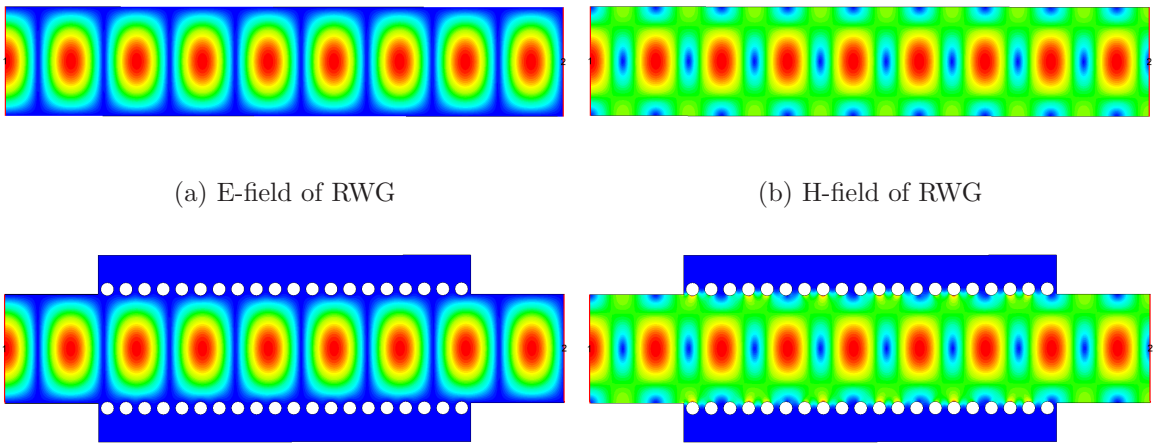


Figure 1.2: SIW topology with its structural parameters.

evolving technology, a waveguide structure is implemented on a piece of printed circuit board (PCB) and its side walls are replaced by two rows of metal posts [13]. Inheriting low radiation loss, acceptable Q-factor and high power handling capability from traditional RWG structures, SIW also utilizes low cost, low profile and easy integration capabilities of planar structures [13]. SIW presents a widely accepted circuit compromise in the lower millimeter-wave regime where microstrip components are increasingly lossy and waveguides too bulky and too expensive. Thus, the SIW technology offers a new layout in which microwave circuits can be effectively designed and integrated at a low cost and with low radiation loss. SIW structures can be fabricated with existing manufacturing capabilities like PCB and Low-Temperature Co-fired Ceramic (LTCC) technologies [13]. Figure 1.2 shows the SIW topology with its structural parameters. On a specific dielectric with h as the substrate height and ϵ_r as substrate relative permittivity, the main structural parameters of an SIW structure are the diameter of the metal posts (d), the space between them in a row (via pitch p), and the SIW width, a_{SIW}, which is the spacing between two rows of vias (center-to-center).



(a) E-field of RWG

(b) H-field of RWG

(c) E-field of SIW

(d) H-field of SIW

Figure 1.3: Comparison between electric field patterns (left) and magnetic field patterns (right) of the dominant TE_{10} mode inside RWG (top) and SIW (bottom).

1.2 Design Considerations and Limitations of SIW Structures

As SIW structures are planar realizations of traditional RWGs, the electrical behavior of these structures is very similar to that of RWGs. Figure 1.3 compares the electric and magnetic field patterns of the dominant TE_{10} mode inside the two structures. It is observed that the field patterns are almost identical. Based on this similarity between SIW and RWG, there exists an equivalent waveguide width (W_{equi}) for the SIW structure (Figure 1.4). W_{equi} of the SIW is of fundamental design importance as the design of any SIW structure usually starts with specifying the waveguide width for the desired frequency band and substrate material. A complete review on different proposed relations between a_{SIW} and W_{equi} in the literature, along with a new relation introduced in this thesis will be presented in Chapter 3.

However, beside the similarities between SIW and RWG, there are two major differences. First, SIW is a periodic guided wave structure which may result in electromagnetic bandstop properties and second, there might be some leakage through the space between via holes [18].

In designing SIW structures, after specifying W_{equi} and a_{SIW}, the next step is to carefully choose d and p in order to achieve the desired propagation constant,

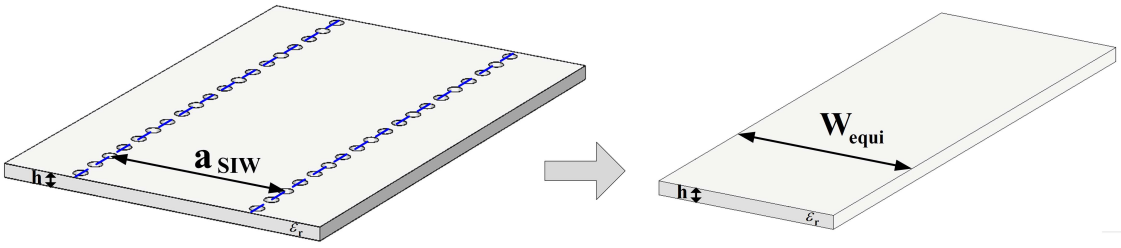
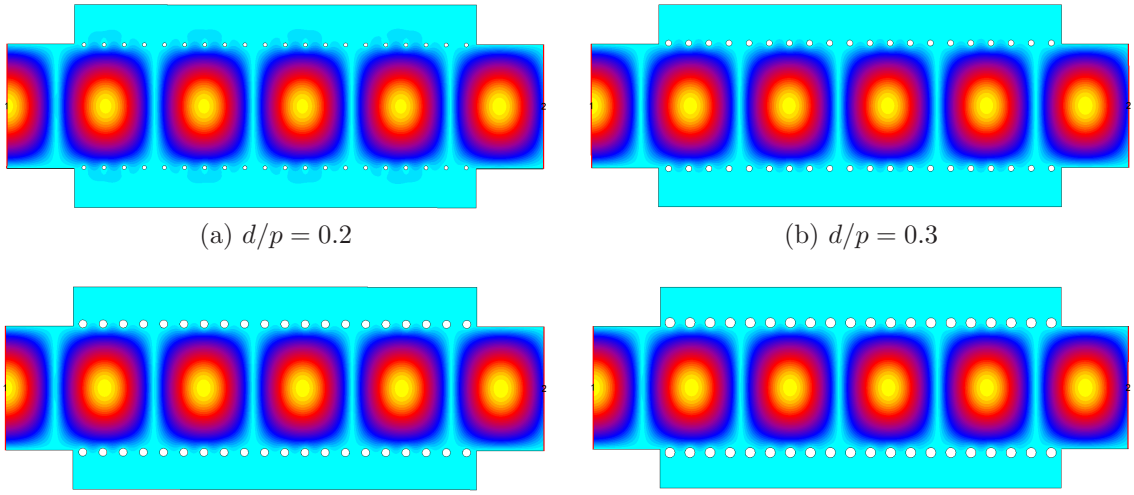


Figure 1.4: Effective waveguide width of an SIW structure. a_{SIW} is the SIW width and W_{equi} is its equivalent waveguide width.

reduce the wave leakage, and also meet the fabrication limitations. The via pitch p is usually chosen such that we have around ten vias per guided wavelength in the structure. With such a p, the frequency of the stopband of the SIW acting as a periodic structure would be much higher than our desired operating frequency. Therefore, there is usually no need to consider that bandgap effect when dealing with SIW structures.

The ratio of via diameter d to the via pitch p, d/p, is an important parameter in designing SIW structures. d/p should be chosen large enough so that we have minimum amount of leakage. On the other hand, it should be small enough so that the fabrication process including drilling these vias become feasible. Figure 1.5 shows the electrical field pattern inside an SIW structure for different d/p ratios. SIW circuits with d/p between 0.4 and 0.8 have been published in the literature. However, in order to minimize leakage losses, $d/p > 0.5$ is recommended. The practical range of the d/p ratio in SIW applications is $0.5 < d/p < 0.8$ according to [19].

There are three major sources of loss in the SIW circuitry. Similar to dielectric filled waveguide structures, the conductor loss due to the finite conductivity of the conductors, and also dielectric loss of the substrate should be taken into account. In addition, due to the gap between vias in the side wall of the SIW, there might be some radiation losses as well. However, proper selection of the d/p, as it is discussed above, would result to a negligible radiation loss. In [20] the effect of structural parameters of the SIW on the conductor and dielectric losses have been investigated. It is shown that increasing the dielectric height would result in a lower conductor loss. Also, the contribution of other structural parameters in the ohmic loss is not significant. On the other hand, dielectric loss does not depend on the SIW structural parameters,



(a) $d/p = 0.2$ (b) $d/p = 0.3$

(c) $d/p = 0.4$ (d) $d/p = 0.5$

Figure 1.5: Electric field pattern inside an SIW structure for different d/p values plotted at $f = 15.2GHz$. In all structures, dielectric is RT/duroid 6002 with relative permittivity $\epsilon_r = 2.94$ and height $h = 0.508mm$. The width of the waveguide port is $9.2139mm$ and $p = 1.5mm$. For different values of d, a_{SIW} has been calculated accordingly based on [2]. (a) $d/p = 0.2$, (b) $d/p = 0.3$, (c) $d/p = 0.4$ and (d) $d/p = 0.5$.

and it is merely determined based on the chosen substrate. In the millimeter wave region, with the commercially available dielectrics and standard dielectric thicknesses, dielectric loss is dominant in SIW structures [20].

As it is stated in the beginning of this section, a_{SIW} is mainly determined based on the chosen dielectric, desired frequency band and d/p ratio. However, some attempts have been reported in the literature in order to reduce the SIW size. A Substrate Integrated Folded Waveguide (SIFW) topology, proposed in [21], decreases the size of the SIW by almost half, while increases the loss. Also close to 50% size reduction is achieved by introducing half-mode SIW (HMSIW) [22]. A combination of these two techniques, Folded HMSIW (FHMSIW), is also reported [23], which results in even more size reduction [24].

It is worth mentioning that although SIW components have acceptable Q-factor (around a few hundreds), in the applications with demand for lowest possible losses (like satellites), waveguide structures are still an inevitable choice. SIW components have limitations to reach that level of Q-factors of about a few thousands due to the dielectric loss and higher conductor loss relative to waveguide circuitry. Also, due to the lower power-handling capability of SIW structures compared to waveguide

ones, in high-power designs waveguides are still preferable. However, despite all these limitations, recently the number of industry papers on SIW is increasing, which shows the real world demand for this evolving technology.

1.3 Motivation for This Thesis

One factor that has to be dealt with in designing SIW structures is their complexity. Due to the large amount of via holes required, designing and optimizing SIW components with commercially available field solvers is a tedious and cumbersome task. Therefore, the need for an efficient analytical tool, which can model SIW components in a fast and accurate manner, is crucial. Developing an effective and efficient analytical technique for time efficient and accurate analysis of SIW structures is one of the major motivations for this thesis.

In addition, SIW as an evolving technology has attracted much interest in designing different types of microwave components based on this layout. Numerous publications have been reported in this area. However, still some types of components have not been designed in this technology. In this thesis, some new SIW passive component designs are presented for the first time.

The waveguide width of the SIW is of fundamental importance in designing SIW circuits. However, the accuracies of the different reported formulations for the relation between a_{SIW} and W_{equi} vary depending on the d/p ratio. The need for a simple, yet accurate formulation, which is applicable in all practical ranges of d/p, was obvious. In this thesis, such a formulation based on the MMT is presented.

One the other hand, in order to integrate and provide means for the excitation and measurement of SIW structures, transitions between SIW and other planar topologies are required. It is vital to provide low-reflection transitions so that the component design is independent of the influences of the transitions. One of the most common types of these transitions is the transition between a microstrip line and SIW. Different configurations for the microstrip-SIW-transition have been reported. However, all of those transitions are either narrow band, or provide return loss not better than $20dB$. Presenting a low reflection transition topology, which can operate on the full waveguide bandwidth, has been one of the main motivations for this thesis.

1.4 Thesis Contributions

The major contributions of this thesis are summarized in this section. This thesis

- utilizes a duality between circular vias and square vias and introduces an MMT analytical approach to analyze SIW structures with equivalent square vias. This MMT is faster than commercially available field solvers by an order of magnitude, and still can efficiently model complex SIW structures.
- introduces a new relation between SIW width and its equivalent waveguide width. The presented equation is derived by the MMT and proves to be the most accurate formulation available.
- presents a new transition between the microstrip line and the SIW structure. This transition is capable of operating over the full waveguide bandwidth for microwave bands from X to E, and yields the minimum reported reflection coefficient among previously reported microstrip-SIW-transitions.
- presents different types of passive microwave structures designed in SIW technology using the MMT. Some of these components are among the first reported in SIW technology, e.g. the backward diplexer.

1.5 Thesis Outline

The outlines of each chapter are described as follows.

Chapter 1 contains an overall introduction and overview of SIW technology, its applications, potentials and limitations. Thesis contributions and overall motivations of this thesis are also presented in this chapter.

Chapter 2 provides an overview of the analytical techniques available for analyzing SIW structures and then describes in details the analytical approach of this dissertation which is based on the MMT. Performances of the presented techniques are validated for different configurations of vias in the structure and also different excitation methods.

Chapter 3 investigates excitation of SIW structures with waveguide ports and microstrip ports and gives a new formulation for the calculation of the effective

waveguide width of the SIW, which is used in exciting SIW structures with waveguide ports. Also, a new configuration for the transition between microstrip line and SIW is proposed in this chapter. The presented transition proves to be the most wideband microstrip-SIW-transition available with minimum reflection coefficient.

Chapter 4 includes the passive SIW components designed and analyzed with the MMT. Various types of SIW components including filters, couplers, power dividers and diplexers are designed. The literature review of each passive component is provided and the designed SIW structures based on the MMT approach are presented afterward. The analytical data are validated with simulation data and in some cases with measurement data.

Chapter 5 summarizes the results and findings presented in this thesis and presents some of the possible future directions of the analysis and design of SIW structures and their applications.

Chapter 2

Analysis of SIW Structures

As vias in SIW structures can be considered as inductive obstacles in RWG, in the first section, we present the analytical works on inductive obstacles in terms of historical trend, followed by SIW analysis methods. The MMT analysis of H-plane SIW structures is presented in the subsequent section.

2.1 Inductive Obstacles in Rectangular Waveguide

The scattering of a plane electromagnetic wave by an inductive obstacle placed in an RWG parallel to the electric field of the dominant mode has received considerable attention in microwave theory. In one of the earliest works, during World War II Julian Schwinger [25] had originally solved the single-post problem by a variational principle. His solution was for small posts, and his data is presented in Marcuvitz's Waveguide Handbook [26]. The inductive post problem can simply be considered in terms of current which is induced on the post. This current is longitudinally directed along the post axis and varies circumferentially with radius. The variation of current density on the surface of the obstacle may be represented by a Fourier series:

$$K(r) = \sum A_n f_n(r)$$

where $f_n(r)$ form a function set, and A_n are expansion coefficients to be determined. Schwinger had taken into account the zeroth and first-order terms of the series. This simplification is valid for posts which were of moderate size and were distant from the walls and from each other. However, his results are very accurate within those limitations [25].

In 1951, Marcuvitz calculated by variational methods the parameters of the equivalent circuit for the RWG containing a discontinuity which may be a dielectric or metallic cylinder (Figure 2.1). The results are obtained by employing a constant, a cosine, and a sine term in the expression for the obstacle current and are accurate to within a few percent, but only for cylinders of diameter less than 0.1 of the waveguide width, and $0.2 < \frac{x}{a} < 0.8$ (Figure 2.1), provided that neither of the equivalent circuit parameters was close to resonance [26].

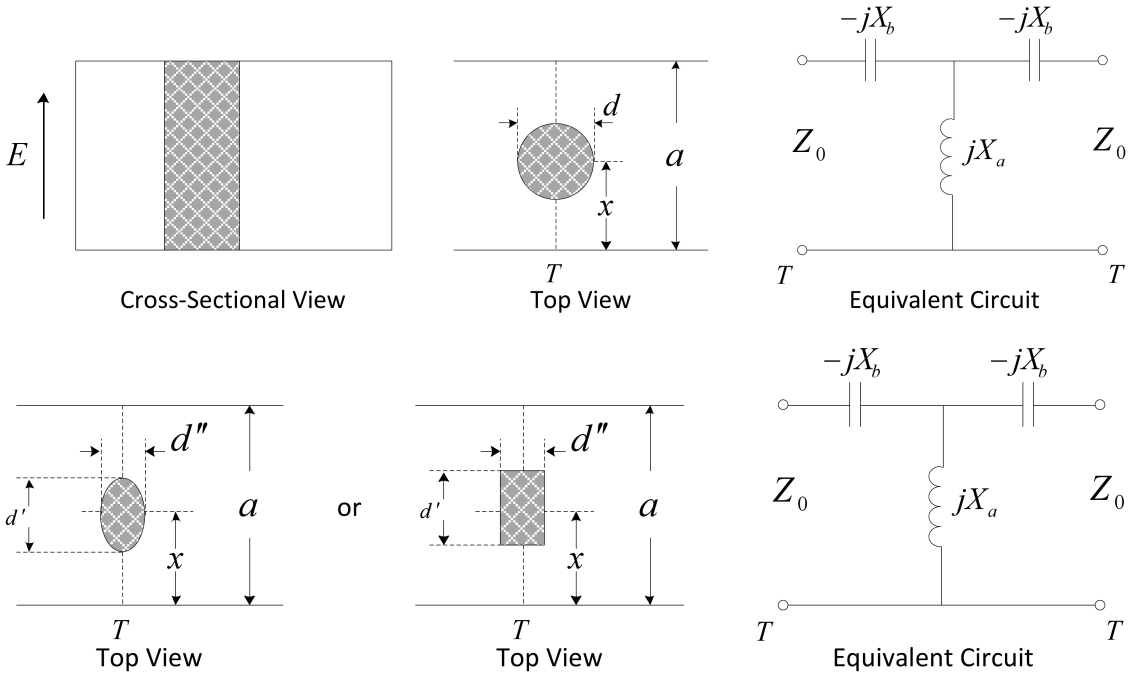


Figure 2.1: Equivalent circuit for small inductive post in RWG presented by Marcuvitz [26].

Also in 1951, Lewin set up a theory for calculating the reactance of the post and the reflection from a metallic, cylindrical post placed across the narrow side of an RWG. The method used is to find a configuration of dipoles, doublets, etc., which, if present along the axis of the post, would give a field that would cancel the tangential component of an incident electric field at the surface of the post. However, the results are approximate, based upon the assumption of a cylinder of radius r which is small compared to the waveguide dimensions, allowing powers of r higher than the second to be neglected [27].

In 1956, Craven and Lewin [28] pointed out the advantages of triple-post configurations in designing band-pass filters such as the one presented in Figure 2.2. The

construction is such that some cancellation of higher order modes occurs.

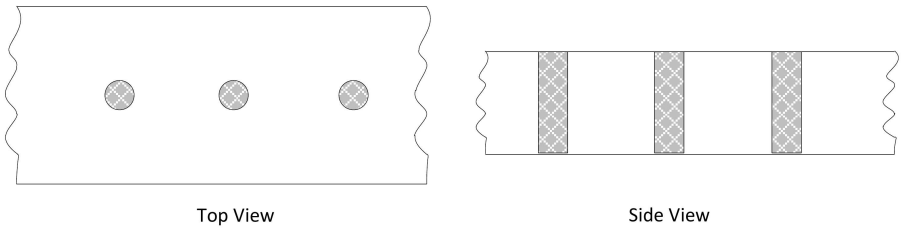


Figure 2.2: Triple-post configuration in RWG considered by Craven and Lewin [28].

However, in microwave filter design, larger posts were needed when narrow band-pass filters were desired. Mariani [29], in 1965, recognized the need for larger posts, but due to the lack of data, decided to analyze the triple-post configuration consisting of three small posts, each within the range of Schwinger's analysis [30]. He found it necessary to add experimentally determined correction factors to his analysis.

In 1969, Nielsen [31] presented a solution for a circular cylindrical post of arbitrary complex permittivity centered in an RWG with its axis parallel to the electric field of the dominant mode. The method used by Nielsen divided the waveguide into three different parts by introducing two imaginary walls perpendicular to the waveguide walls. The cylindrical post is placed in the center region, where the electromagnetic field is expanded in cylindrical waves. In the outer regions, the field is expanded in waveguide modes. By applying the boundary conditions at all discontinuity surfaces and matching the fields at the two imaginary walls, a system of linear equations determining the coefficients of reflection, transmission, and absorption of the field due to the cylindrical post was found [31] (Figure 2.3). His method is extended to posts of any size and complex permittivity; however, it is applicable only to circular centered posts. Nielsen's work also improved the results near resonance [31].

Also in 1969, Green [32] presented a Green's function for a line current in RWG in terms of a rapidly converging series. This representation of Green's function consists of two parts. The first part is a finite series which yields the field due to the original source and its nearest neighboring images (Figure 2.4). The second part is an infinite series which gives the contribution to the field due to the remaining images. With the aid of the Method of Moments (MoM), he computed the reflection coefficient for a perfectly conducting circular post in a waveguide with its axis parallel to the electric field. The current distribution on the cylinders were approximated by pulses for use with MoM [32].

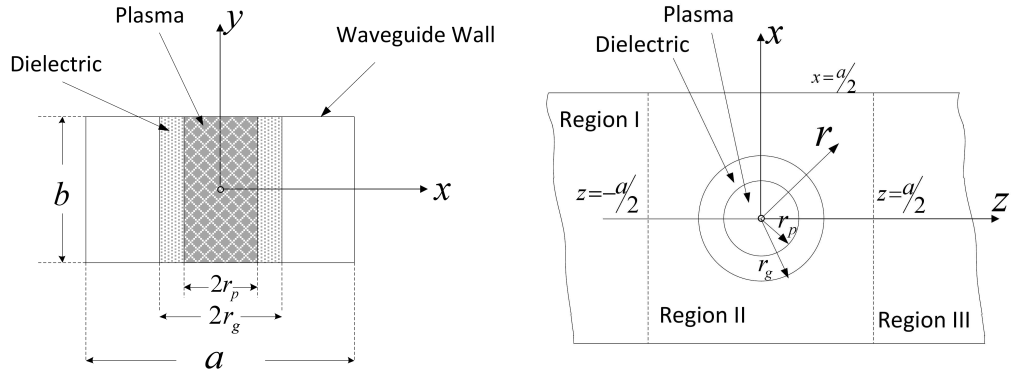


Figure 2.3: Cross section (left) and top view showing the imaginary walls (right) of the structure considered by Nielsen [31].

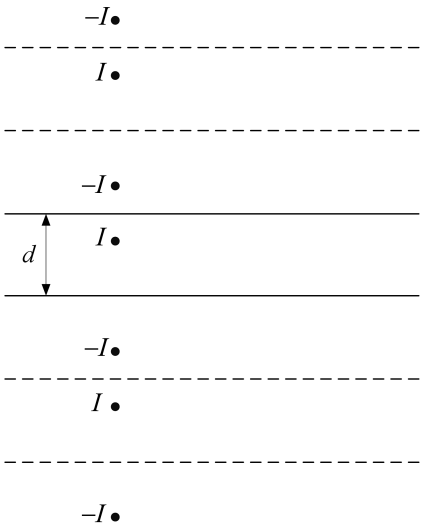


Figure 2.4: Images for a current line in rectangular guide presented by Green [32].

In 1978, Abele [33] obtained precise data for equivalent circuits of symmetric inductive post arrays in RWG by the MMT. However, he did not consider higher order mode interactions.

Leviatan and his group published multiple papers on inductive obstacles in RWG including a single-post inductive obstacle in 1983 [30], multiple-post inductive obstacle in 1984 [34], numerical study of the current distribution on the post in 1984 [35], inductive dielectric posts in 1987 [36] and composite inductive posts in 1988 [37]. Their general approach is to use a multi-filament representation of the current (Figure 2.5). The field due to each filament is then expanded in terms of waveguide modes. However, this results in a slowly converging series which is not suitable for

computation. They solved this drawback by converting the series to a rapidly converging one. Subsequently, a multiple point-matching of the boundary condition is applied and the unknown filamentary currents are obtained [30].

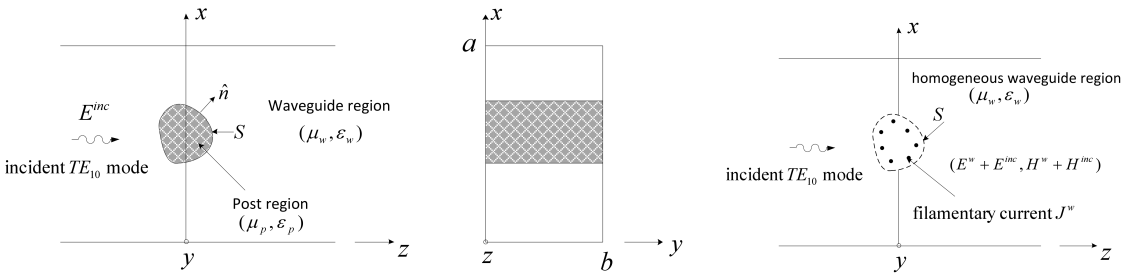


Figure 2.5: Filamentary current element used in the work of Leviatan *et al.* [36].

X.-H. Jiang and S.-F. Li in 1991 proposed a three-dimensional (3D) analysis for calculating the equivalent network of arbitrarily shaped inductive posts in RWG based on the method of lines [38].

Also some works have used the Finite Element Method (FEM) and the Boundary Element Method (BEM) for dividing the arbitrarily shaped inductive obstacle into meshes and calculate S-parameters of the structure [39], [40].

In [41], Buchta and Heinrich investigated the equivalence between cylindrical and square via holes in a RWG. Among their four proposed equivalences, the one that showed most accurate equivalence in our simulations has been used in our further studies presented in Chapter 3 and Chapter 4.

2.2 Review on SIW Analysis Techniques

In most single layer SIW circuits, the conductor sheets on the top and bottom are intact. Therefore, these kinds of structures are excited by transverse electric (TE)-like waves. With no field variation normal to the substrate, this type of SIW circuits is mainly a two-dimensional (2D) problem [13]. Modes that can be preserved in these H-plane SIW structures are discussed in Section 2.3.2.

It should be mentioned that SIW technology can also be deployed in the antennas design. Electromagnetic energy radiation can be achieved by cutting slots in the conductor planes on the top or bottom of the substrate, or leaving the end of an SIW open, i.e., not closed by a post wall. For these structures, the electromagnetic field is not constant in the normal direction of the substrate anymore and a 3D

electromagnetic solver must be used in order to analyze these circuits [13].

Different numerical techniques have been used to analyze SIW configurations, mostly the H-plane ones. Specifically for SIW interconnections, which consist of just two rows of vias, some approaches have been introduced for the study of their wave propagation characteristics. The SIW interconnect (not SIW components) is treated as a periodic structure, and in some cases by using Floquet's theorem, the computational domain is restricted to just one cell.

In one of the earliest works in this area, a Galerkin's MoM is used for the analysis of a unit cell of a post-wall waveguide used to excite a plane transverse electromagnetic (TEM) wave, and then Floquet's theorem is applied to calculate the propagation constant of the periodic post-wall waveguide [17]. Xu *et al.* in 2003 combined a Finite-Difference Frequency-Domain (FDFD) algorithm with a perfectly matched layer (PML) and Floquet's theorem for the analysis of SIW guided-wave problems [42]. The desegmentation method is deployed in [43] in order to calculate the impedance matrix of a unit cell of SIW. Then, the propagation constant of the fundamental mode of SIW is obtained by applying Floquet's theorem on the impedance matrix of the unit cell [43]. Also, in 2005, leakage characteristics of SIW structures and complex propagation constants of SIW modes have been investigated by using a multi-mode calibration technique which is developed and integrated with a full wave simulator based on the FEM [18]. Again, Floquet's theorem is deployed in [44] in order to study the dispersion characteristics of SIW. The unit cell of the SIW is analyzed with the MMT [44]. The periodic guided-wave problem of SIW is turned into an equivalent resonator problem in [45], and then the Finite-Difference Time-Domain (FDTD) technique is deployed to simulate periodic guided-wave structures. The application of this technique for the analysis of SINRD guides is investigated [45]. The concept of surface impedance is used in [19] in order to model the rows of conducting cylinders and determination of complex propagation constants in SIWs. The model is then solved by combining an MoM and a transverse resonance procedure [19].

However, for the analysis and modeling of complete SIW components and circuits, some full-wave analytical techniques are required. In the following sections, some of the main analytical works will be reviewed.

2.2.1 Finite-Difference and Finite-Element Methods for Analysis of SIW

Xu *et al.* utilized a Domain Decomposition Finite-Difference Time-Domain (DD-FDTD) method combined with a numerical thru-line (TL) calibration technique in order to extract parameters of microwave circuits and structures like SIW components [46]. By combining the numerical TL calibration techniques with the FDTD method, not only the accuracy of the simulation increases, but also the computational efficiency is improved. In addition, the hybrid algorithm can be extended to the applications that the FDTD method alone is not capable of, such as extracting parameters for non-continuous or discrete structures [47].

Also, based on a high order hierarchical vector function, higher order Finite-Element Time-Domain (FETD) methods combined with a Tearing and Interconnecting (TI) algorithm is presented in [48] in order to analyze SIW structures. By means of the high order hierarchical vector function, the accuracy and ability of FETD simulations of complicated SIW problems are improved [48].

2.2.2 Method of Moments for Analysis of SIW

In [49] and [50], the MoM is used in the analysis of SIW circuits and also SIW slot arrays. The field inside the SIW structure is computed by considering the dyadic Green's function expressed as an expansion in terms of vectorial cylindrical eigenfunctions and considering the scattering from the conducting posts. Coaxial or waveguide ports are included in the analysis as equivalent magnetic current distributions [49]. The slots in the array are modeled as unknown equivalent magnetic current distributions [50].

Another MoM based method for analyzing SIW structures is presented in [51], [52] and [13]. In this method, the field due to a cylinder is written in a series of cylindrical eigenfunctions assuming no variation of the field along the cylinders, which makes the problem of 2D type, while the waveguide ports are treated in MoM manner (Figure 2.6). There is no geometry discretization for the cylinders, and the boundary conditions at the entire surface of a cylinder are forced intrinsically [13].

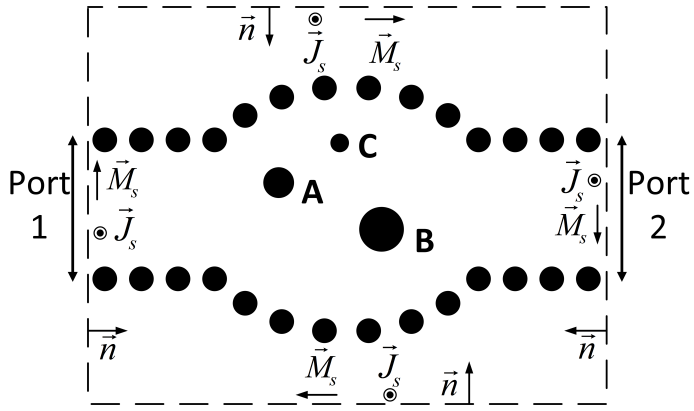


Figure 2.6: Equivalent problems of SIW circuits with metallic post presented in [13].

2.2.3 Boundary Integral-Resonant Mode Expansion Method for Analysis of SIW

Among analytical approaches of investigating SIW structures, one of the recent and most popular contributions are based on the Boundary Integral-Resonant Mode Expansion (BI-RME) method [53], [54] and [55]. In this method, the hybrid representation, consisting of Boundary Integrals (BI) and a rapidly converging Resonant Mode Expansion (RME), permits to transform the non-linear eigenvalue problem resulting from a standard boundary integral approach into a linear one. This transformation is done by introducing a limited number of auxiliary variables. However, the disadvantage of increasing the number of unknowns is compensated by the advantage of avoiding unreliable numerical solutions of the non-linear eigenvalue problem arising from conventional BEM [56]. The BI-RME method yields the admittance matrix Y of a lossless and shielded waveguide component in the form of a pole expansion in the frequency domain [57]. In this method, the domain of the eigenfunctions is extended from S, which is the actual cross-section of the structure, to a rectangular or circular domain Ω, embedding S (Figure 2.7). The method yields the solution of *enlarged* eigenvalue problems [56]. The BI-RME method also allows to derive multimodal equivalent circuit models of SIW discontinuities [58]. The method can be extended to model the losses in SIW circuits as well [54].

2.2.4 Hybrid MMT and MoM for Analysis of SIW

A hybrid MMT and MoM is deployed in [59] in order to analyze SIW components. Each via is approximated by discrete filaments carrying uniform currents. The dyadic

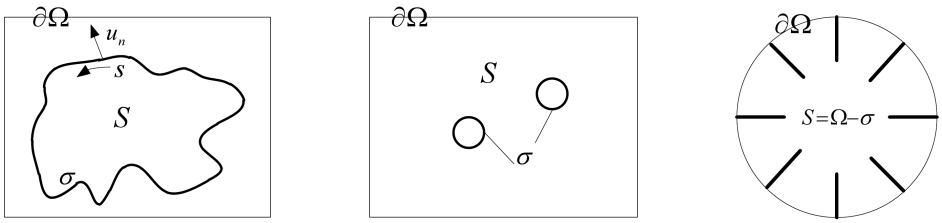


Figure 2.7: The domain S is embedded in a rectangular or circular domain Ω in the BI-RME method [56].

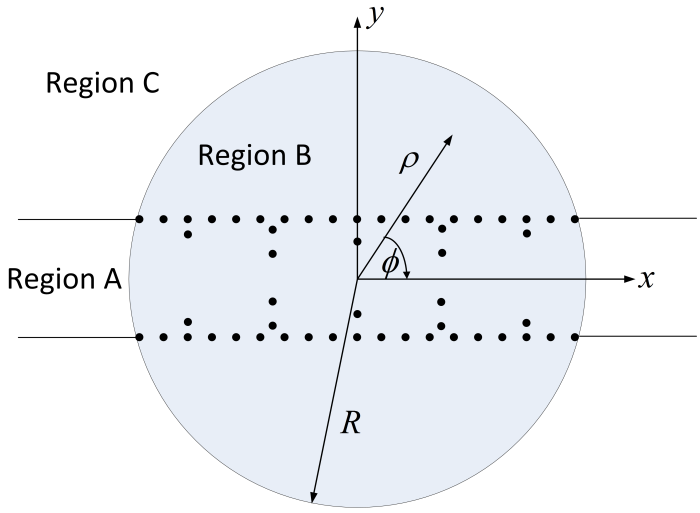


Figure 2.8: General layout of the SIW problem with coordinate systems of regions A, B and C considered in the work of Diaz *et al.*. Region A includes all the guided ports accessing the SIW device. Region B, containing the SIW device, can be seen as a multiple scattering problem with N scattering objects and in Region C, as the field leakage from the post walls is very weak, the field can be neglected [62].

Green's function of the structure is calculated and MMT is applied in order to assure the continuity of fields on waveguide ports. The MoM approach completes the analysis and S-parameters of the structure along with the field patterns inside the structure are determined [59].

Another hybrid MMT/MoM formulation is proposed in [60]. The advantage of this approach is that in this method, the port characterization is based only on a single electric current density rather than the conventional two equivalent sources. This results in decreased computational time, and makes it possible to utilize a fast sweep scheme that can be used to accelerate the solution [61].

2.2.5 Hybrid MMT and Spectral Method for Analysis of SIW

In a work published in 2012 [62], the multiple 2D scattering analysis described in [63], a method that solves the matching between cylindrical and guided waves, has been adopted to analyze SIW circuits with multiple ports (Figure 2.8). In this work, the electromagnetic coupling among all scatterers is solved by means of scattered cylindrical modes and spectrum translation, instead of using MoM [62] as in [60, 61].

Based on the method presented in [62], for analyzing SIW structures, firstly the whole SIW device is enclosed in a circumference as small as possible. This circular region is completely characterized through a global transfer function. In the next step, the continuity of electric and magnetic fields particularized in the circular boundary are projected over the cylindrical and guided modes [62].

A review of different presented methods deployed to analyze SIW interconnects and SIW components can be found in Table 2.1.

Analytical Approaches for SIW Interconnects					
FDFD+PML +Floquet [42]	desegmentation +Floquet [43]	multi-mode calib.+ FEM simulator [18]	MMT+ Floquet [44]	equivalent resonator +FDTD [45]	MoM+transverse resonance [19]
Analytical Approaches for SIW Components					
DD-FDTD+ TL calib. [46]	FETD+ TI [48]	MoM [49] and [13]	BI-RME [53] and [55]	MMT+MoM [59] and [60]	MMT+spectral method [62]

Table 2.1: Different analytical methods for analyzing SIW interconnects and SIW components.

2.3 Modes in SIW Structures

As SIW structures are imitating RWGs in the planar format, different modes in RWG structures are investigated first. For each mode, electric and magnetic fields are calculated from respective vector potentials. Please note that the time dependence of $e^{(j\omega t)}$ is assumed in all vector potentials, in which ω is the angular frequency.

2.3.1 Modes in RWGs

Figure 2.9 shows the discontinuity between two RWGs. The field in each waveguide is expanded as a superposition of z-directed eigenmodes. The fields for TE and transverse magnetic (TM) modes are presented in the following.

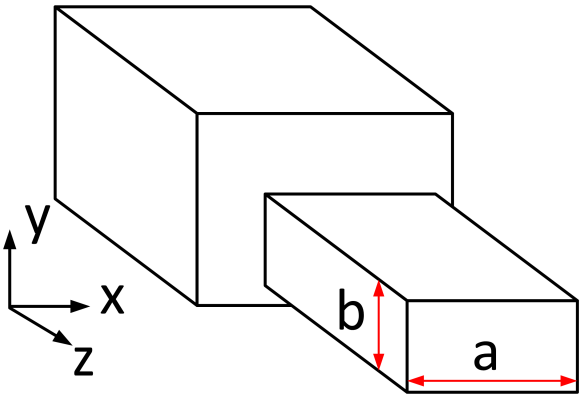


Figure 2.9: Discontinuity between two RWG structures.

TE Modes

For the TE_{mn} set of modes, the vector potential can be expressed as (suppose that the cross-section of the structure is in x-y plane, cf. Figure 2.9):

$$\vec{A_h} = A_{hz}\vec{a_z} = \sum_m \sum_n \sqrt{Z_{hmn}} T_{hmn}(x,y)[F_{hmn}e^{-jk_{zhmn}.z} + B_{hmn}e^{+jk_{zhmn}.z}]\vec{a_z} \quad (2.1)$$

in which Z_{hmn} is the wave impedance of the TE_{mn} mode and is equal to:

$$Z_{hmn} = \frac{\omega\mu}{k_{zhmn}} = \frac{1}{Y_{hmn}} \quad (2.2)$$

μ is the permeability of free space, a is the width of the waveguide and k_{zhmn} is the wave propagation constant for the TE_{mn} propagating wave in the z-direction and is given by:

$$k_{zhmn} = \sqrt{k^2 - k_{chmn}^2} = \sqrt{(\frac{\omega}{v_c})^2\epsilon_r - (\frac{m\pi}{a})^2 - (\frac{n\pi}{b})^2} \quad (2.3)$$

in which $k = \omega\sqrt{\mu\epsilon}$ is the wavenumber of the material filling the waveguide, v_c is the speed of light in free space and ϵ_r is the relative permittivity of the filling material of the waveguide. b is also the height of the waveguide. F and B are the amplitudes of forward and backward traveling waves in the structure (see Figure 2.14), and T_{hmn} represents the dependence of the potential on cross-sectional coordinates.

From this vector potential, the electric and magnetic fields can be calculated as:

$$\vec{E} = -\nabla \times (A_{hz}\hat{a_z}) = -\sum_m \sum_n \sqrt{Z_{hmn}}[\nabla T_{hmn}(x,y) \times \hat{a_z}]$$
$$[F_{hmn}e^{-jk_{zhmn}.z} + B_{hmn}e^{+jk_{zhmn}.z}] \quad (2.4)$$

and

$$\vec{H} = \tfrac{1}{j\omega\mu}\nabla \times \nabla \times (A_{hz}\hat{a_z}) = -\sum_m \sum_n \sqrt{Y_{hmn}}(\nabla T_{hmn}[F_{hmn}e^{-jk_{zhmn}.z} -$$
$$B_{hmn}e^{+jk_{zhmn}.z}] + j\tfrac{k^2_{chmn}}{k_{zhmn}}T_{hmn}(x,y)\hat{a_z}[F_{hmn}e^{-jk_{zhmn}.z} + B_{hmn}e^{+jk_{zhmn}.z}]) \quad (2.5)$$

TM Modes

For the TM_{mn} set of modes, the vector potential can be expressed as (again suppose that the cross-section of the structure is in x-y plane, cf. Figure 2.9):

$$\vec{A_e} = A_{ez}\vec{a_z} = \sum_m \sum_n \sqrt{Y_{emn}}T_{emn}(x,y)[F_{emn}e^{-jk_{zemn}.z} - B_{emn}e^{+jk_{zemn}.z}]\vec{a_z} \quad (2.6)$$

in which Z_{emn} is the wave impedance of the TM_{mn} mode and is equal to:

$$Z_{emn} = \frac{k_{zemn}}{\omega\epsilon} = \frac{1}{Y_{emn}} \quad (2.7)$$

k_{zemn} is the wave propagation constant for the TM_{mn} propagating wave in the z-direction and is given by:

$$k_{zemn} = \sqrt{k^2 - k^2_{cemn}} \quad (2.8)$$

T_{emn} represents the dependence of the potential on cross-sectional coordinates.

From this vector potential, the electric and magnetic fields can be calculated as:

$$\vec{E} = \tfrac{1}{j\omega\epsilon}\nabla \times \nabla \times (A_{ez}\hat{a_z}) = -\sum_m \sum_n \sqrt{Z_{emn}}(\nabla T_{emn}[F_{emn}e^{-jk_{zemn}.z} +$$
$$B_{emn}e^{+jk_{zemn}.z}] + j\tfrac{k^2_{cemn}}{k_{zemn}}T_{emn}\hat{a_z}[F_{emn}e^{-jk_{zemn}.z} - B_{emn}e^{+jk_{zemn}.z}]) \quad (2.9)$$

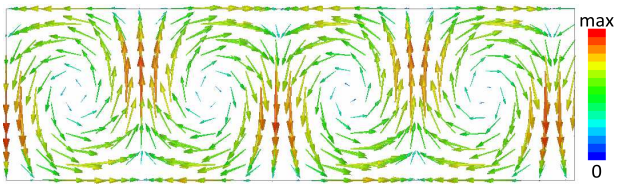
and

$$\vec{H} = \nabla \times (A_{ez}\hat{a_z}) = \sum_m \sum_n \sqrt{Y_{emn}}[\nabla T_{emn}(x,y) \times \hat{a_z}]$$
$$[F_{emn}e^{-jk_{zemn}.z} - B_{emn}e^{+jk_{zemn}.z}] \tag{2.10}$$

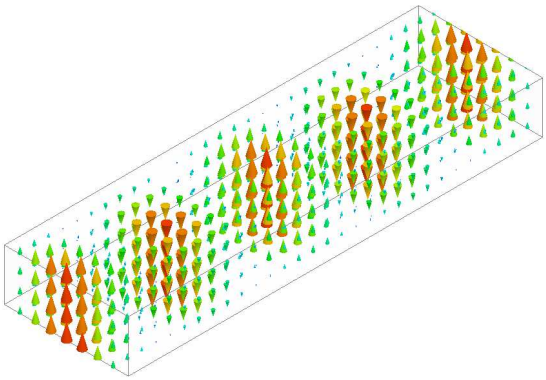
Please also note that in waveguide structures with perfect magnetic conductor (PMC) side walls, like the waveguide model of microstrip structures, TEM modes are also present. In this case, TEM mode can be treated as the zero-th mode of TM waves ($k_{cemn} = 0$ in Equation 2.8, cf. Section 2.4.2).

2.3.2 Modes in SIW

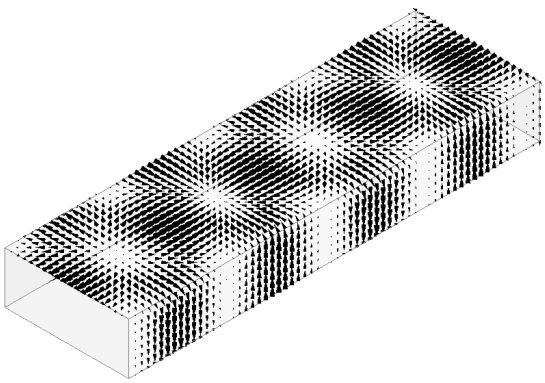
TE_{m0} modes are the only modes that can propagate in H-plane SIW structures. For justifying this statement, let us consider the different types of modes that can exist in an RWG and the pattern of the surface current each mode creates on the waveguide walls.



(a) Top view of the magnetic field pattern.



(b) Electric field pattern.



(c) Currents on the side walls.

Figure 2.10: Fields and current patterns for TE_{10} mode in a rectangular waveguide: (a) top view of the magnetic field pattern, (b) the electric field pattern, and (c) currents on the side walls.

Figure 2.10 shows the fields and surface current pattern of a TE_{10} mode on the

conducting walls of the rectangular waveguide. As it can be seen, there is no longitudinal current on the side walls of the rectangular waveguide. Therefore, if we create some vertical slots in these side walls, the currents of this dominant mode still can find its way along the conductor parts of the side wall and will produce no radiation. Figure 2.11 represents these current patterns.

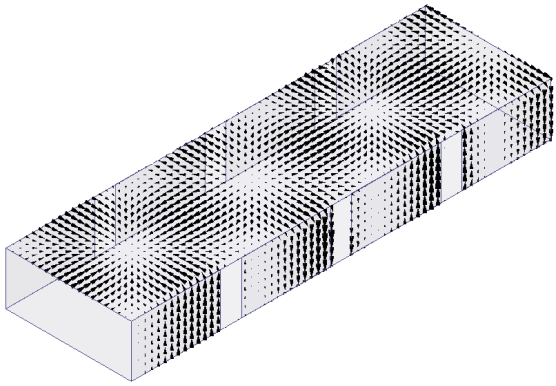


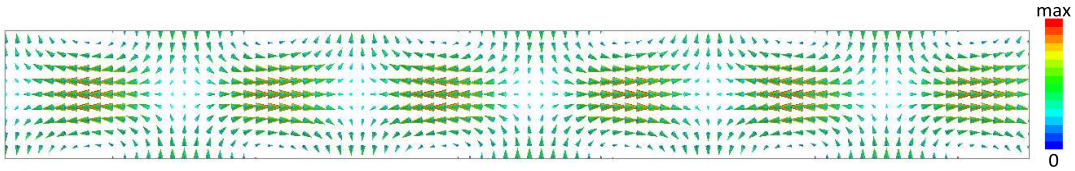
Figure 2.11: Vertical slots on the side walls of a rectangular waveguide and the surface current pattern in this structure.

As there is no longitudinal current on the side walls in the current patterns of all TE_{m0} modes, by having some vertical slots in the side wall of the rectangular waveguide (like in the case of SIW structures), the current pattern remains almost the same, and these kind of modes can be preserved in these defected structures.

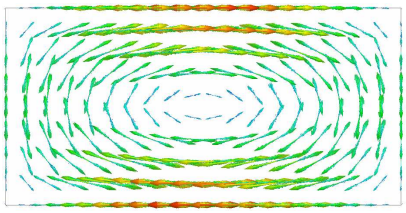
On the other hand, for TM modes, the transverse magnetic field produces longitudinal currents on the side walls of the rectangular waveguide. Figure 2.12 presents the fields and surface current patterns for a TM_{11} mode in a rectangular waveguide.

Now, if we create any vertical slot or defect on the side wall, these defects would cut the current and introduce enormous amounts of radiation. That is the reason why this class of modes can not be preserved in SIW structures [18].

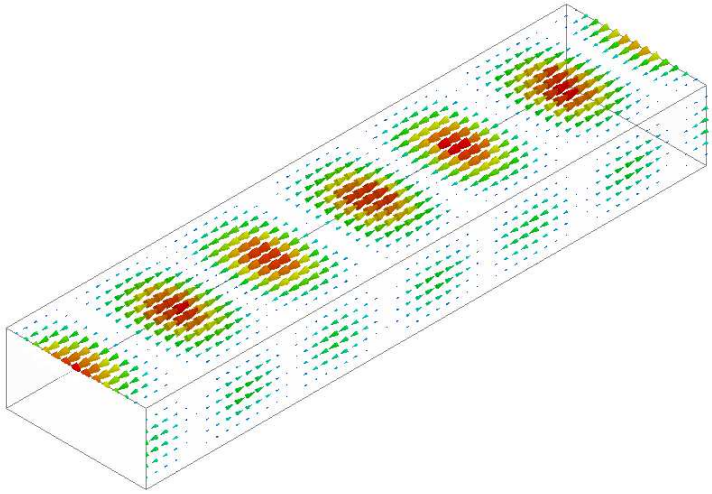
Also, as in the conventional PCB technology, the substrate height is too small compared to the SIW width, TE_{mn} modes with n greater than zero would appear at frequencies much higher than the desired operating frequency band (about ten times of the cut-off frequency of the working frequency band). Thus, these types of modes cannot be preserved in SIW structures either. Please note that in waveguide technology increasing the height of the waveguide results to a higher Q-factor, whereas in SIW technology we try to keep the height small, to have lower substrate loss and be compatible with standard planar technologies.



(a) The side view of the electric field pattern.



(b) The front view of the magnetic field.



(c) Surface currents.

Figure 2.12: Fields and current patterns for TM_{11} mode in rectangular waveguide: (a) the side view of the electric field pattern, (b) front view of the magnetic field, and (c) surface currents.

In conclusion, only TE_{m0} modes need to be considered in H-plane SIW structures. As there is a reduced set of modes in SIW structures, modal analysis techniques are proper candidates to analyze SIW structures. However, in order to apply any modal analysis like the MMT, the fundamental modes on each side of a discontinuity must be known. In this thesis, an MMT technique for the analysis of SIW structures with rectangular/square vias is presented. The method will be presented in detail in the next section. However, circular vias in SIW structures are most popular due to standard fabrication. Therefore, the analysis of the SIW structures with circular vias is more desirable. For analysis of SIW structures with circular vias, which is the case in most SIW structures, these modal analysis techniques should be combined with other techniques, or as presented in this thesis, a proper equivalence between square vias and circular ones must be established.

2.4 MMT for Analysis of H-plane SIW Structures

It is discussed in Section 1.2 that the ratio of $\frac{d}{p}$ in SIW structures is chosen so that the electromagnetic field is completely bound inside the structure and minimum leakage occurs. As a result of that, we bound our SIW structure inside a larger RWG with the same height as the SIW structure, in order to be able to apply the MMT. In this larger RWG surrounding the SIW structure, fundamental modes are known, which enables us to apply MMT for any via configurations in the SIW.

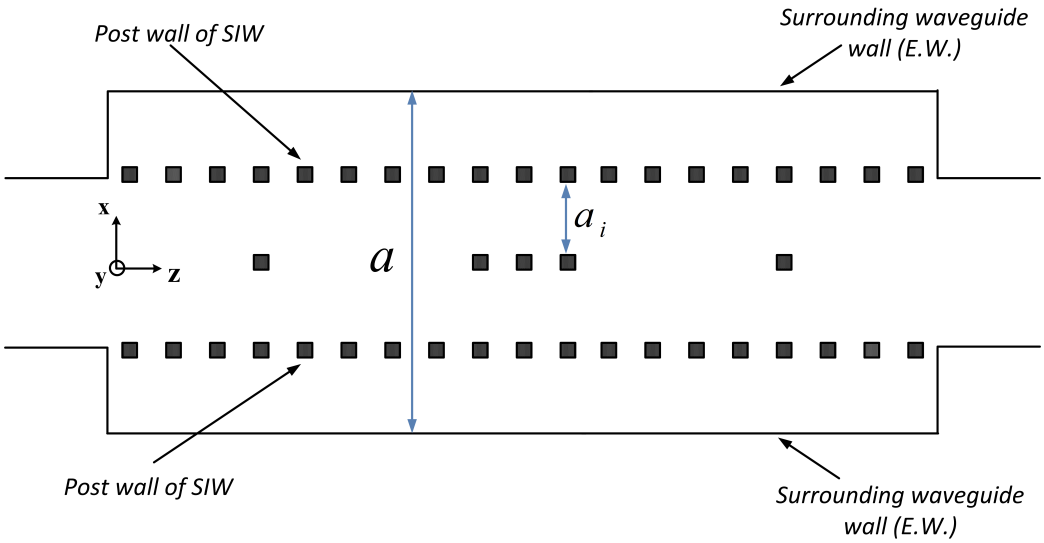


Figure 2.13: Typical SIW structure surrounded by a larger RWG.

Figure 2.13 presents a typical SIW structure surrounded by a larger RWG. In the ideal situation that the leakage from the SIW structure is absolutely zero, the width of this circumferential waveguide could be equal to $a_{SIW} + d$ (see Figure 1.2), but in reality, in order to accurately model the structure, we need to choose this width slightly larger than $a_{SIW} + d$.

In the following sections, the application of MMT in the analysis of different types of discontinuities encountered in SIW structures will be presented in detail. Please note that loss-less SIW structures are considered first in order to present our MMT approach. The dielectric and conductor losses of SIW can be easily incorporated in the MMT analysis, as it will be discussed in Section 2.6.

2.4.1 Modes in Waveguide with Electric Walls

For the TE_{m0} set of modes (n is set to zero in all equations presented for TE_{mn} modes in RWG, cf. Section 2.3.1), the vector potential can be expressed as (suppose that the cross-section of the structure is in x-y plane, cf. Figure 1.2):

$$\vec{A_h} = A_{hz}\vec{a_z} = \sum_m \sqrt{Z_{hm}} T_{hm}(x)[F_m e^{-jk_{zm}.z} + B_m e^{+jk_{zm}.z}] \tag{2.11}$$

in which Z_{hm} is the wave impedance of the TE_{m0} mode and is equal to

$$\sqrt{Z_{hm}} = \sqrt{\frac{\omega\mu}{k_{zm}}} \tag{2.12}$$

k_{zm} is the wave propagation constant for the TE_{m0} propagating wave in the z-direction and is given by:

$$k_{zm} = \sqrt{k^2 - k_c^2} = \sqrt{(\frac{\omega}{v_c})^2\epsilon_r - (\frac{m\pi}{a})^2} \tag{2.13}$$

in which $k = \omega\sqrt{\mu\epsilon}$ is the wavenumber of the dielectric, v_c is the speed of light in free space and ϵ_r is the relative permittivity of the substrate. F and B are the amplitudes of forward and backward traveling waves in the structure (see Figure 2.14), and T_h represents the dependence of the potential on cross-sectional coordinates; for TE_{m0} modes, we only have x dependence of T_h. T_h can be expressed as: (note that the origin has been placed in the middle of the cross-section)

$$T_{hm}(x) = A_m cos\frac{m\pi}{a}(x + \frac{a}{2}) \tag{2.14}$$

This equation holds for the waveguide of width a as presented in Figure 2.13 or any sub-regions of width a_i. Since in MMT all modes have to be normalized to the same power, e.g. $1W$ in each region, we have:

$$A_m = \frac{a}{m\pi}\sqrt{\frac{2}{ab}} \tag{2.15}$$

For the electric and magnetic fields in this region, we have:

$$\vec{E} = -\nabla \times (A_{hz}\hat{a_z}) \Longrightarrow E_y = \frac{\partial A_{hz}}{\partial x} \tag{2.16}$$

and

$$\vec{H} = \frac{-1}{j\omega\mu}\frac{\partial^2 A_{hz}}{\partial x \partial z}\hat{a_x} + \frac{j}{\omega\mu}\frac{\partial^2 A_{hz}}{\partial x^2}\hat{a_z} \tag{2.17}$$

For completing MMT, subject to the boundary conditions at the discontinuity, electric and magnetic fields at both sides of a discontinuity relate to each other and form the scattering parameters (S-parameters) of the junction. The procedure will be expressed in the next sections.

2.4.2 Modes in Waveguide with Magnetic Walls

A microstrip line can be modeled as a waveguide with perfect magnetic walls. In order to investigate microstrip feed ports in SIW structures, we need to express the field in such a region as well (see Figure 2.18). For information about the equivalent waveguide width of a microstrip line and its effective permittivity, the reader is referred to [64]. As any microstrip structure supports a quasi-TEM mode, and as the TEM mode can be considered as the zero-th TM wave, we have two sets of vector potentials here. For the TEM wave we have:

$$A_{el} = \sqrt{\frac{\epsilon_0 \epsilon_r a}{k_{ze}}} T_{el}(y)[F_e e^{-jk_{ze}.z} - B_e e^{+jk_{ze}.z}] \tag{2.18}$$

in which $T_{el} = V_0 \frac{y}{b}$, $k_{ze} = \frac{\omega\sqrt{\epsilon_r}}{v_c}$ and $V_0 = \sqrt{\frac{b}{a}}$. For TE modes, the vector potential is:

$$\vec{A_h} = A_{hz}\vec{a_z} = \sum_m \sqrt{\frac{\omega\mu}{k_{zm}}} T_{hm}(x)[F_m e^{-jk_{zm}.z} + B_m e^{+jk_{zm}.z}]\vec{a_z} \tag{2.19}$$

and for $T_{hm}(x)$ we have:

$$T_{hm}(x) = A_m sin\frac{m\pi}{a}(x + \frac{a}{2}) \tag{2.20}$$

in which A_m and k_{zm} are the same as in the previous section: $A_m = \frac{a}{m\pi}\sqrt{\frac{2}{ab}}$ and $k_{zm} = \sqrt{(\frac{\omega}{v_c})^2\epsilon_r - (\frac{m\pi}{a})^2}$.

2.4.3 Discontinuity Between an All-dielectric Waveguide and an N-furcated Waveguide

Figure 2.14 presents the discontinuity between an all-dielectric waveguide and an N-furcated waveguide with N-1 via holes. Please note that we apply MMT for the analysis of SIW structures with rectangular/square vias. The size of the vias in Figure 2.14 is exaggerated in order to demonstrate forward and backward traveling waves in each region.

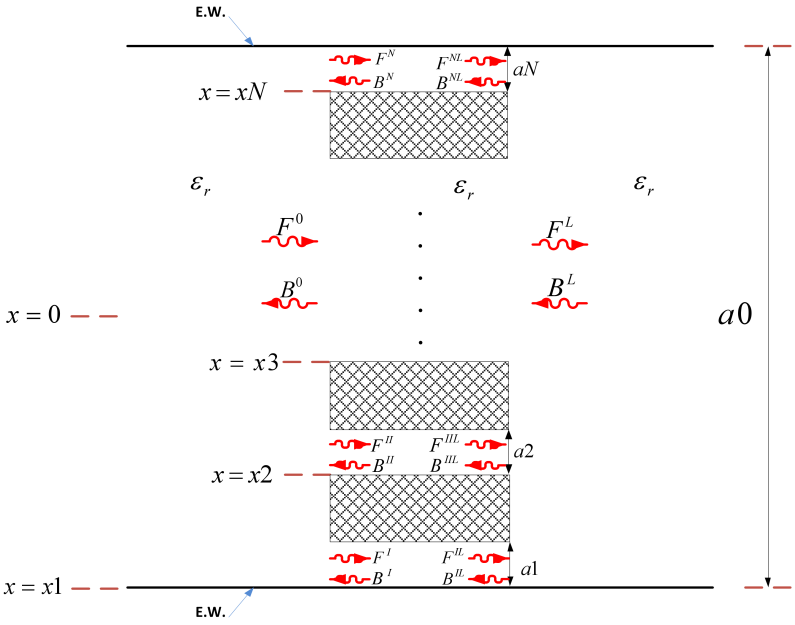


Figure 2.14: Discontinuities between an all-dielectric waveguide and an N-furcated waveguide formed by N-1 via holes.

For this type of discontinuity, $\vec{E}$ and $\vec{H}$ are calculated by Equation 2.16 and Equation 2.17 and at the discontinuity, the boundary condition of perfect electric conducting vias is applied. By matching E_y over the entire discontinuity, knowing that E_y is zero on PEC walls (suppose that it is placed at $z = 0$), we have:

$$\begin{aligned} & \sum_m \sqrt{\frac{\omega\mu}{k_{zm}^0}} A_m^0 \frac{m\pi}{a_0} (-sin\frac{m\pi}{a_0}(x + \frac{a_0}{2}))[F_m^0 + B_m^0] \\ = & \sum_{n=1}^{N} \sum_k \sqrt{\frac{\omega\mu}{k_{zk}^n}} A_k^n \frac{k\pi}{a_n} (-sin\frac{k\pi}{a_n}(x - x_n))[F_k^n + B_k^n] \end{aligned} \tag{2.21}$$

and by matching H_x in each individual region (e.g., region n), we obtain:

$$\begin{aligned} & \sum_m \frac{k^0_{zm}}{\omega\mu}\sqrt{\frac{\omega\mu}{k^0_{zm}}}A^0_m \frac{m\pi}{a_0}(-sin\frac{m\pi}{a_0}(x+\frac{a_0}{2}))[-F^0_m + B^0_m] \\ = & \sum_k \frac{k^n_{zk}}{\omega\mu}\sqrt{\frac{\omega\mu}{k^n_{zk}}}A^n_k \frac{k\pi}{a_n}(-sin\frac{k\pi}{a_n}(x-x_n))[-F^n_k + B^n_k] \end{aligned} \tag{2.22}$$

We multiply both sides of Equation 2.21 by $sin\frac{m'\pi}{a_0}(x+\frac{a_0}{2})$ and integrate from $-\frac{a_0}{2}$ to $\frac{a_0}{2}$. This results in the following equation:

$$F^0 + B^0 = \sum_n M^n[F^n + B^n] \tag{2.23}$$

or in the matrix format:

$$\left[F^0 + B^0\right] = \left[\begin{array}{cccc} M^1 & M^2 & \cdots & M^N \end{array}\right] \left[\begin{array}{c} F^1 + B^1 \\ \cdots \\ \vdots \\ \cdots \\ F^N + B^N \end{array}\right]$$

in which $M = \left[\begin{array}{cccc} M^1 & M^2 & \cdots & M^N \end{array}\right]$. Also we multiply both sides of Equation 2.22 by $sin\frac{k'\pi}{a_n}(x-x_n)$ and integrate from x_n to $x_n + a_n$, leading to the following equation:

$$(M^n)^T[F^0 - B^0] = F^n - B^n \qquad (N - times) \tag{2.24}$$

or in the matrix format:

$$\left[\begin{array}{c} (M^1)^T \\ \cdots \\ (M^2)^T \\ \cdots \\ \vdots \\ \cdots \\ (M^N)^T \end{array}\right] . \left[F^0 - B^0\right] = \left[\begin{array}{c} F^1 - B^1 \\ \cdots \\ \vdots \\ \cdots \\ F^N - B^N \end{array}\right]$$

M^T is the transpose of M. In the above equations, matrix M^n is related to the impedance matrix Z_k^n, admittance matrix Y_m^0 and coupling integral $(J^n)_{mk}$ by:

$$M^n = Diag\sqrt{Y_m^0} \cdot J^n \cdot Diag\sqrt{Z_k^n} \tag{2.25}$$

for each discontinuity, and the coupling integral is:

$$(J^n)_{mk} = \frac{2}{\sqrt{a_0 a_n}} \int_{x_n}^{x_n+a_n} sin\frac{m\pi}{a_0}(x + \frac{a_0}{2}) sin\frac{k\pi}{a_n}(x - x_n)dx \tag{2.26}$$

From this M matrix, S-parameters, which relate incident and reflected wave amplitudes as:

$$\begin{bmatrix} B^0 \\ F^I \\ \vdots \\ F^N \end{bmatrix} = [S] \begin{bmatrix} F^0 \\ B^I \\ \vdots \\ B^N \end{bmatrix}$$

can be derived by:

$$\begin{aligned} S_{11} &= [MM^T + I]^{-1}.[MM^T - I] \\ S_{12} &= 2[MM^T + I]^{-1}.M = S_{21}^T \\ S_{21} &= M^T(I - S_{11}) \\ S_{22} &= I - M^T S_{12} \end{aligned} \tag{2.27}$$

where I denotes the unit matrix.

Also, please note that some SIW components have some vias that are not completely aligned with each other (cf. Figure 2.15). In this case, according to the previous procedure, S-parameters of the discontinuity from an N-furcated waveguide to an all-dielectric waveguide are calculated. The difference from before is that, in both SIW slices number one and two in Figure 2.15, we do not have any all-dielectric waveguide after the discontinuity and thus we set the length of the all-dielectric waveguide equal to zero in our calculations.

2.4.4 SIW Structures with Waveguide Ports

Figure 2.16 represents the discontinuity from a waveguide port to an SIW structure. The boundary between two structures is treated as a PMC. In our first investigations, we considered the chance of the existence of some electric fields at this boundary, and

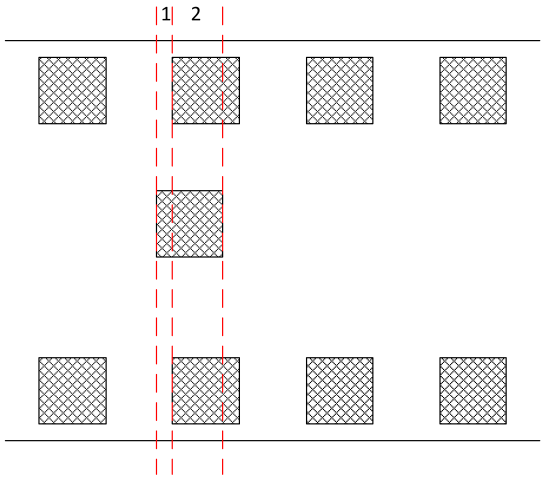


Figure 2.15: Longitudinally overlapping vias in SIW components.

thus we chose the boundary as a PMC. However, in SIW components there is hardly any field at this discontinuity, and choosing that as a PMC or a perfect electric conductor (PEC) produces differences within the plotting accuracy. In this case, $\vec{E}$ and $\vec{H}$ are calculated by Equation 2.16 and Equation 2.17. However, as the boundary condition is a PMC, for matching we have to multiply both sides of the equation for E_y by $sin\frac{m'\pi}{a_0}(x+\frac{a_0}{2})$ and integrate from $-\frac{a_0}{2}$ to $\frac{a_0}{2}$ (see Figure 2.16) and for H_x by $sin\frac{k'\pi}{a_1}(x+\frac{a_1}{2})$ and integrate from $-\frac{a_1}{2}$ to $\frac{a_1}{2}$. In this case the coupling integral is:

$$(J)_{mk} = \frac{2}{\sqrt{a_0 a_1}} \int_{-\frac{a_0}{2}}^{\frac{a_0}{2}} sin\frac{m\pi}{a_0}(x+\frac{a_0}{2}) sin\frac{k\pi}{a_1}(x+\frac{a_1}{2})dx \tag{2.28}$$

The M matrix and S-parameters are calculated as in Equation 2.25 and Equation 2.27.

2.4.5 SIW Structures with Microstrip Ports

It is known that a simple microstrip line can be modeled as an equivalent waveguide with perfect magnetic walls. Different formulations for the effective dielectric constant and effective width of this equivalent waveguide presented in the literature have different validity limits. In this case, the fields are calculated from vector potentials represented in Equation 2.18 and Equation 2.19. Note that the equivalent waveguide width of microstrip and effective permittivity of this equivalent waveguide are frequency dependent values. For details on microstrip transmission line parameters, the reader is referred to [64].

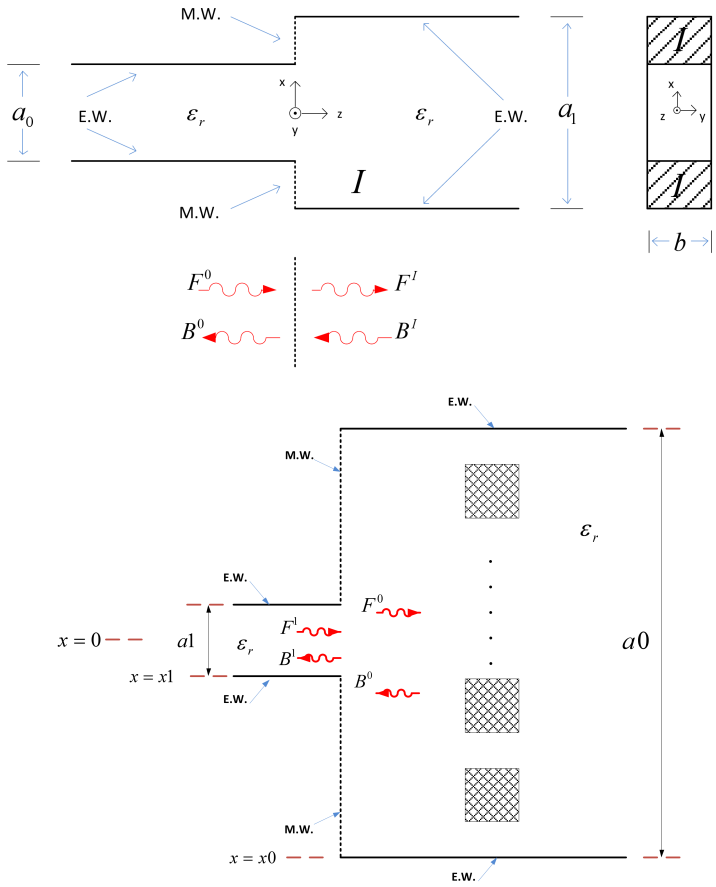


Figure 2.16: Discontinuity between waveguide port and SIW structure.

For matching purposes, a transition is needed from the microstrip line to an SIW structure. Such transition is presented in Figure 2.17. In order to analyze this transition, we approximate it by several steps. So we need to evaluate the discontinuity between two microstrip lines. Also, the discontinuity between the microstrip line (taper) and an SIW structure will be presented.

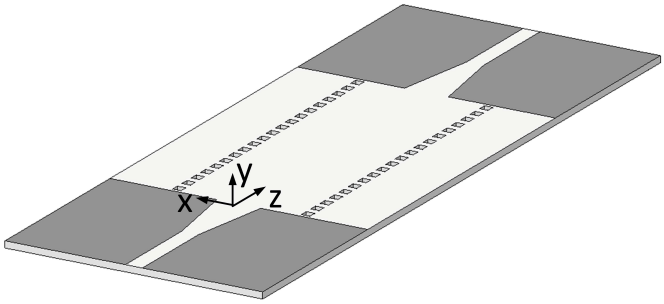


Figure 2.17: Transition from microstrip line to SIW structure. Light gray represents PEC and darker gray shows dielectric material.

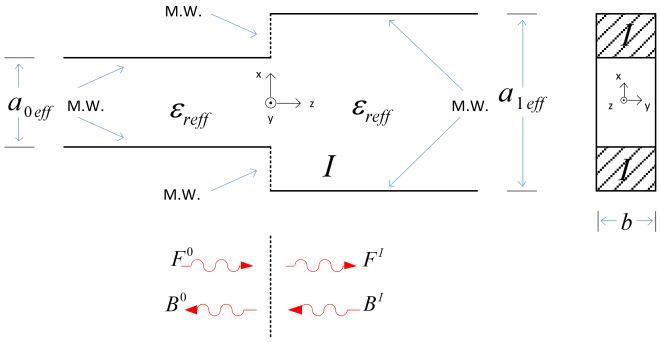


Figure 2.18: Discontinuity between two microstrip guides.

Discontinuity Between two Microstrip Lines

The discontinuity between two microstrip lines is depicted in Figure 2.18. In this case, the coupling integrals are:

$$
\begin{aligned}
(J_{ll})_{0,0} &= \int_{A_0} (\nabla T^0_{el})(\nabla T^I_{el}) da = \sqrt{\tfrac{a_0}{a_1}} \\
(J_{lh})_{0,k} &= \int_{A_0} (\nabla T^0_{el})(\nabla T^I_{hk} \times \vec{a_z}) da = \tfrac{2}{\sqrt{a_0 a_1}} \int_{-\frac{a_0}{2}}^{\frac{a_0}{2}} cos\tfrac{k\pi}{a_1}(x + \tfrac{a_1}{2}) dx \\
(J_{hl})_{m,0} &= \int_{A_0} (\nabla T^0_{hm} \times \vec{a_z})(\nabla T^I_{el}) da = 0 \\
(J_{hh})_{m,k} &= \int_{A_0} (\nabla T^0_{hm})(\nabla T^I_{hk}) da = \tfrac{2}{\sqrt{a_0 a_1}} \int_{-\frac{a_0}{2}}^{\frac{a_0}{2}} cos\tfrac{m\pi}{a_0}(x + \tfrac{a_0}{2}) cos\tfrac{k\pi}{a_1}(x + \tfrac{a_1}{2}) dx
\end{aligned}
\tag{2.29}
$$

Again, the M matrix and S-parameters can be calculated according to Equation 2.25 and Equation 2.27.

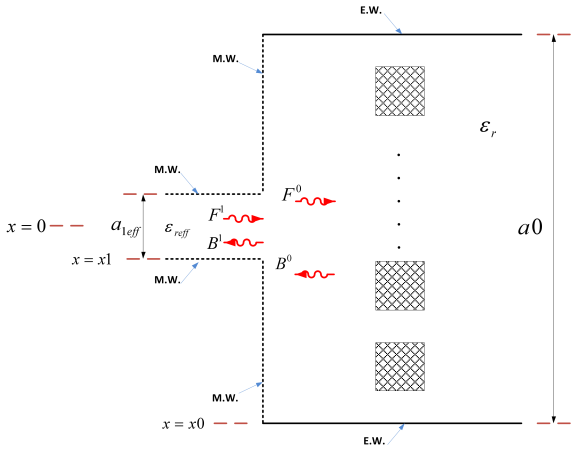


Figure 2.19: Discontinuity between microstrip line and SIW structure.

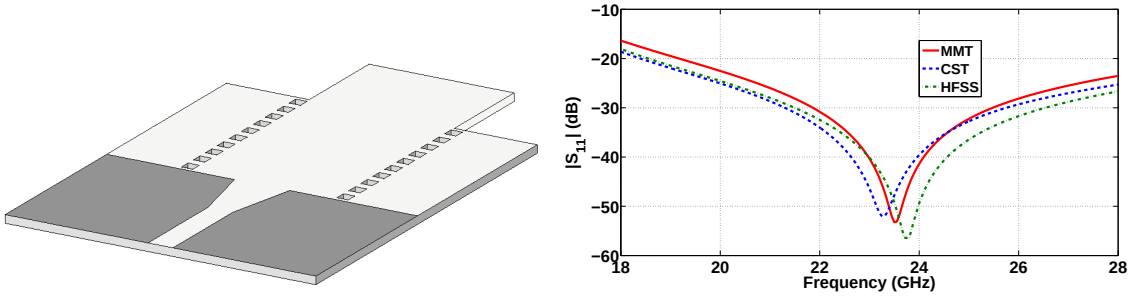


Figure 2.20: Comparison between results obtained with this method (MMT), HFSS and CST.

Discontinuity Between Microstrip Line and SIW Structure

The discontinuity between a microstrip line and an SIW structure is depicted in Figure 2.19. The coupling integrals in this case are:

$$\begin{aligned}(J_{lh})_{0,k} &= \frac{2}{\sqrt{a_1 a_0}} \int_{-\frac{a_1}{2}}^{\frac{a_1}{2}} sin\frac{k\pi}{a_0}(x + \frac{a_0}{2})dx \\ (J_{hh})_{m,k} &= \frac{-2}{\sqrt{a_0 a_1}} \int_{-\frac{a_1}{2}}^{\frac{a_1}{2}} cos\frac{m\pi}{a_1}(x + \frac{a_1}{2}) sin\frac{k\pi}{a_0}(x + \frac{a_0}{2})dx\end{aligned} \tag{2.30}$$

and the M matrix and S-parameters can be calculated as before.

Figure 2.20 shows an analysis of 10 equally spaced via-hole pairs with microstrip input and all-dielectric waveguide output. The substrate is chosen as RT/duroid 5880 with $\epsilon_r = 2.2$, substrate height $h = 0.508mm$ and metallization thickness $th = 0.0175mm$. In the mode-matching approach, the microstrip transformer at the input is approximated by five individual sections, whereas in CST and HFSS, it is

modeled as shown. Very good agreement is observed between this approach (MMT) and HFSS and CST, with the MMT minimum located between those of CST and HFSS. It should be noted that the difference between results from the three solvers results from different analytical approaches deployed by each solver, which result in slight differences below $-20dB$. Also, although increasing the number of steps in the stair-case approximation of microstrip taper results in more accurate results, with a compromise between accuracy and CPU time, we usually use 3-7 microstrip steps in our approximation.

2.4.6 Number of Modes in MMT Calculations

The number of modes in each individual section is set by a maximum frequency. With this maximum frequency, f_{max}, the number of modes in a waveguide section with width a_N is determined as:

$$m_{max} = ceiling(\frac{2a_N f_{max}}{v_p}) \tag{2.31}$$

In which v_p is the wave propagation speed in the dielectric, and the ceiling function maps a real number to the smallest following integer.

According to our investigations, setting this f_{max} equal to 40 times the cut-off frequency of the input/output ports, f_c, results in an acceptable accuracy. f_c is specified at the beginning of the design and determines the operation frequency band. For example, the convergence analysis is done for the S-parameters of the SIW structure presented in Figure 2.21 and the results are presented in Figure 2.22. Figure 2.21 is an SIW structure with 10 pairs of square via holes excited by waveguide ports. $|S_{11}|$ of this structure is compared in Figure 2.22 for different values of f_{max}. In this structure, the dielectric is chosen as RT/duroid 6002 substrate with $\epsilon_r = 2.94$ and height $h = 0.508mm$. Choosing $f_c = 14.051GHz$, which is the cut-off frequency of K-band operation, results in the waveguide port width $W_{equi} = 6.2217mm$. With $p = 1mm$ and $d = 0.6444mm$, the SIW width is $a_{SIW} = 6.7064mm$ (cf. Equation 3.6). With this d, the side length of the square via is $l_{square} = 0.55mm$ (cf. Equation 2.45). As it can be seen in Figure 2.22, increasing the number of modes more than what is suggested by $f_{max} = 40f_c$ does not change the S-parameters significantly. Thus, we choose $f_{max} = 40f_c$ in most of our calculations.

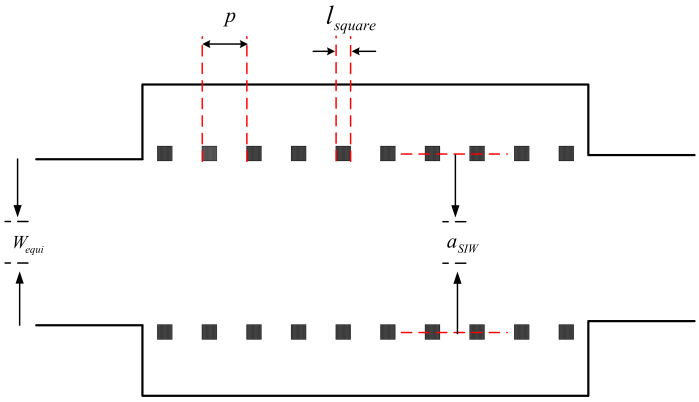


Figure 2.21: SIW structure with square via holes.

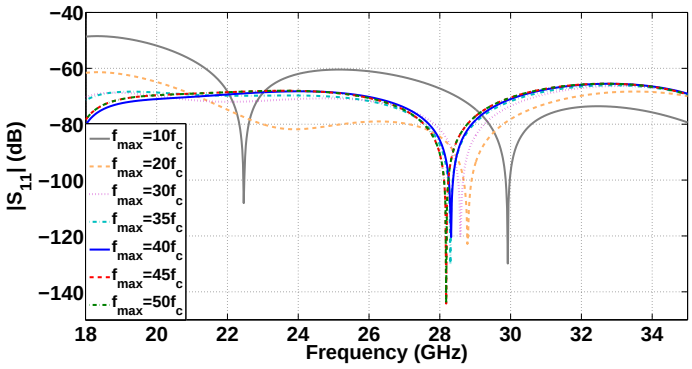


Figure 2.22: Convergence Analysis of the S-parameters calculated with the MMT approach.

2.4.7 Discontinuity Between Multiple Input/Output Ports and SIW Structure

If there is more than one waveguide port at the input or output of the structure (like SIW couplers, Figure 2.23), the procedure of calculating the S matrix is predominantly based on the method presented above for two-port SIW structures. After calculation of the total modal S matrix of the discontinuities involved (same procedure as that presented for two-port structures), the desired S-parameters of the multiple port structure ($M + N$ port structure) with M input ports and N output ports, S_{ij}, are extracted from the computed overall modal two-port scattering matrix

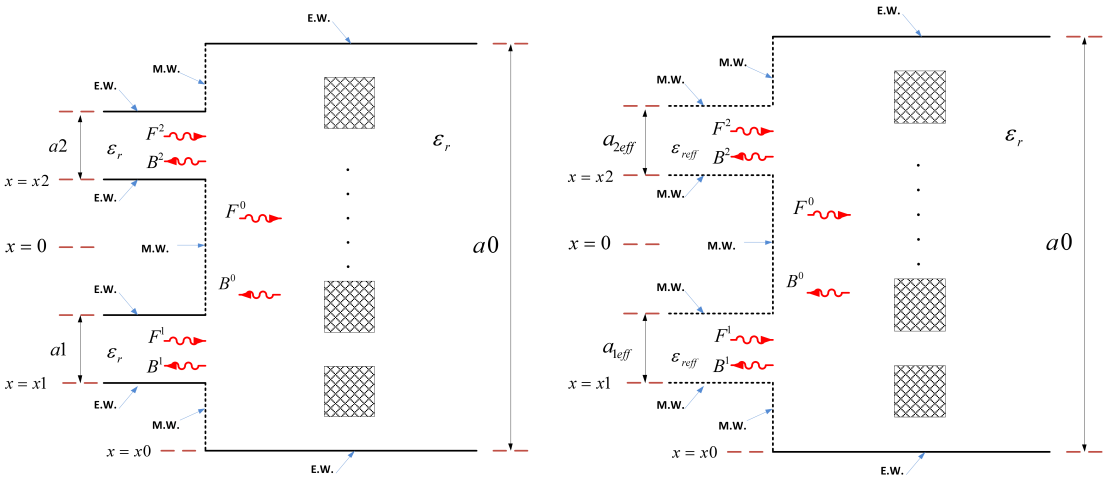


Figure 2.23: SIW couplers with waveguide ports (left) and microstrip ports (right).

as:

$$S^{total} = \left[\begin{array}{c|c} S_{11}^{2-port} & S_{12}^{2-port} \\ \hline S_{21}^{2-port} & S_{22}^{2-port} \end{array}\right]$$

$$= \left[\begin{array}{ccc|ccc} S_{11} & \cdots & S_{1M} & S_{1(M+1)} & \cdots & S_{1(M+N)} \\ S_{21} & \cdots & S_{2M} & S_{2(M+1)} & \cdots & S_{2(M+N)} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ S_{M1} & \cdots & S_{MM} & S_{M(M+1)} & \cdots & S_{M(M+N)} \\ \hline S_{(M+1)1} & \cdots & S_{(M+1)M} & S_{(M+1)(M+1)} & \cdots & S_{(M+1)(M+N)} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ S_{(M+N)1} & \cdots & S_{(M+N)M} & S_{(M+N)(M+1)} & \cdots & S_{(M+N)(M+N)} \end{array}\right] \tag{2.32}$$

2.5 MMT Analysis of SIW T-junction

In the analysis presented in Section 2.4, calculations of the S-parameters of an SIW structure with M input ports and N output ports are presented. Now, for the analysis of an SIW structure including a T-junction, as presented in Figure 2.24, we will deploy that method along with the S-parameter calculations for the waveguide corner [65].

For the S-parameters calculations of the SIW T-junction (Figure 2.25(c)), we first add a waveguide corner (Figure 2.25(b)) to this T-junction, and then calculate the

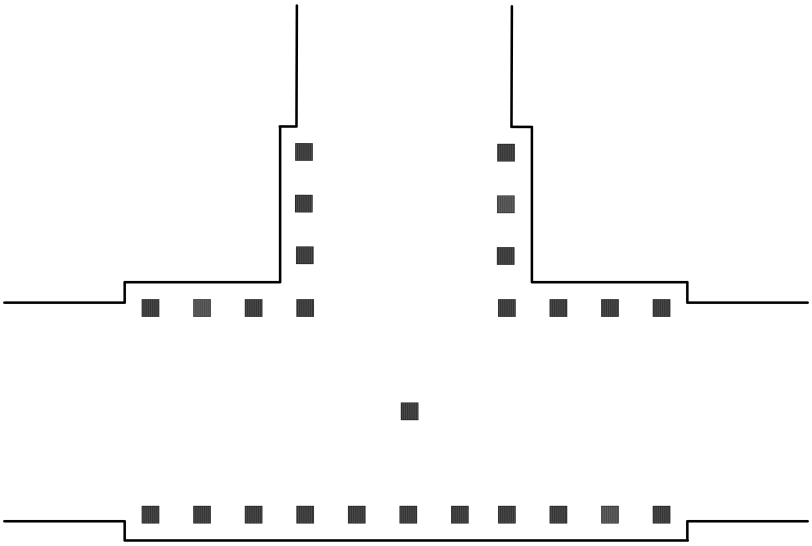


Figure 2.24: T-junction SIW structure with square vias.

S-parameters of this new SIW structure with one input port and two output ports (Figure 2.25(a)) from the theory presented in Section 2.4. Now, we subtract the S-parameters of the waveguide corner [65] from that calculated S-parameters in order to achieve the desired S-parameter of the SIW T-junction in Figure 2.25(c) [66].

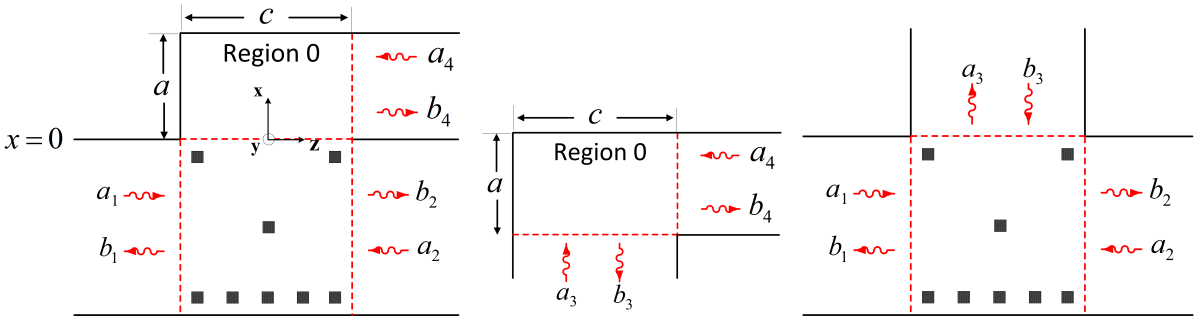
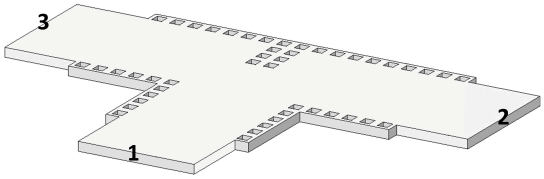


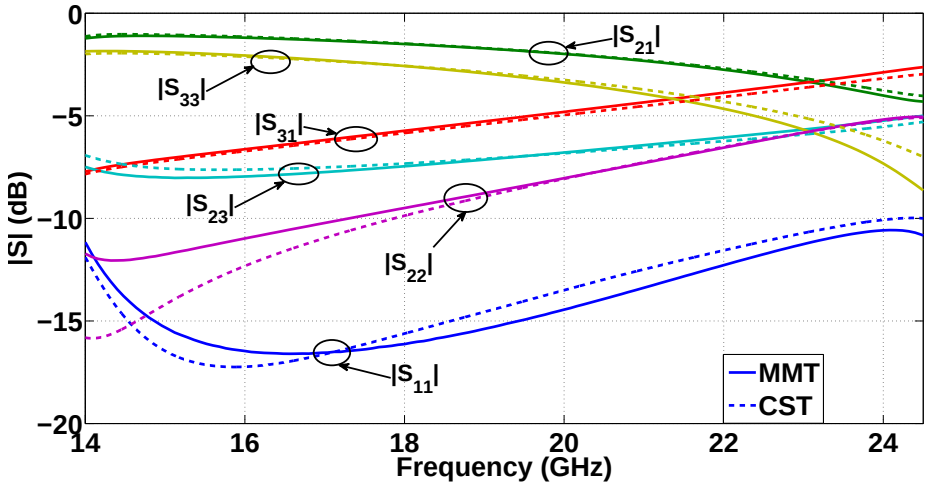
Figure 2.25: S-parameter calculation of an SIW T-junction (c) based on subtraction of the S-parameters of the waveguide corner (b) from the S-parameters of an SIW structure with one input port and two output ports (a).

The details of the theory are as follows: For the structure in Figure 2.25(a) we have:

$$\begin{aligned} b_1 &= S^I_{11}a_1 + S^I_{12}a_2 + S^I_{14}a_4 \\ b_2 &= S^I_{21}a_1 + S^I_{22}a_2 + S^I_{24}a_4 \\ b_1 &= S^I_{41}a_1 + S^I_{42}a_2 + S^I_{44}a_4 \end{aligned} \tag{2.33}$$



(a)



(b)

Figure 2.26: SIW T-junction with square vias. The structure is analyzed with MMT (solid line), and the results are compared with the CST data (dashed line).

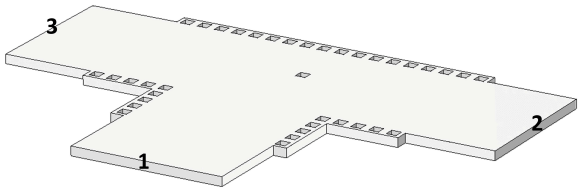
The S-parameter of Figure 2.25(b) can be written as:

$$\begin{aligned} b_3 &= S_{33}^{II} a_3 + S_{34}^{II} a_4 \\ b_4 &= S_{43}^{II} a_3 + S_{44}^{II} a_4 \end{aligned} \tag{2.34}$$

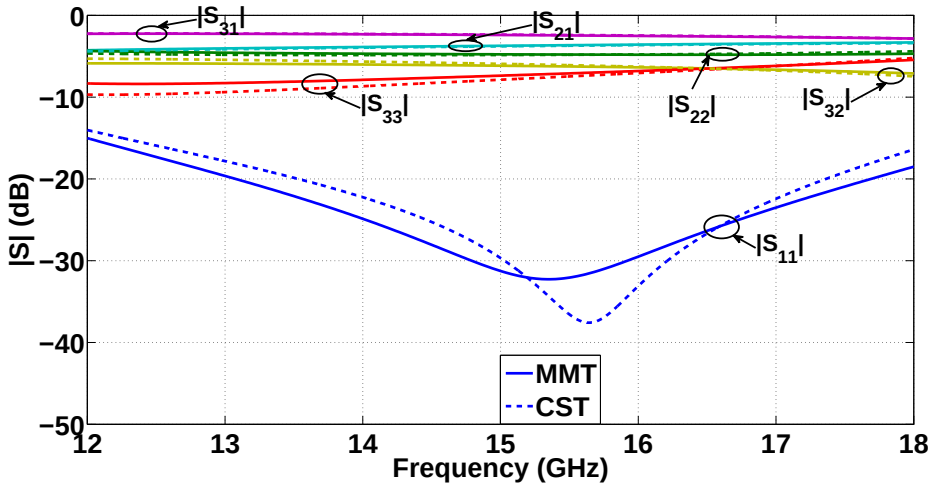
And finally for the S-parameters of our T-junction SIW structure in Figure 2.25(c) we have:

$$\begin{aligned} b_1 &= S_{11}^{III} a_1 + S_{12}^{III} a_2 + S_{13}^{III} b_3 \\ b_2 &= S_{21}^{III} a_1 + S_{22}^{III} a_2 + S_{23}^{III} b_3 \\ a_3 &= S_{31}^{III} a_1 + S_{32}^{III} a_2 + S_{33}^{III} b_3 \end{aligned} \tag{2.35}$$

With some calculations, the final S-parameters of the SIW T-junction are extracted as follows:



(a)



(b)

Figure 2.27: SIW T-junction with square vias in Ku-band. The structure is analyzed with MMT (solid line), and the results are compared with CST data (dashed line).

$$
\begin{aligned}
S_{11}^{III} &= S_{11}^{I} - S_{14}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{41}^{I} \\
S_{12}^{III} &= S_{12}^{I} - S_{14}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{42}^{I} = (S_{21}^{III})^{T} \\
S_{13}^{III} &= S_{14}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{43}^{II} (S_{33}^{II})^{-1} = (S_{31}^{III})^{T}
\end{aligned}
$$

$$
\begin{aligned}
S_{21}^{III} &= S_{21}^{I} - S_{24}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{41}^{I} = (S_{12}^{III})^{T} \\
S_{22}^{III} &= S_{22}^{I} - S_{24}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{42}^{I} \\
S_{23}^{III} &= S_{24}^{I} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{43}^{II} (S_{33}^{II})^{-1} = (S_{32}^{III})^{T}
\end{aligned}
\tag{2.36}
$$

$$
\begin{aligned}
S_{31}^{III} &= (S_{33}^{II})^{-1} S_{34}^{II} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{41}^{I} = (S_{13}^{III})^{T} \\
S_{32}^{III} &= (S_{33}^{II})^{-1} S_{34}^{II} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{42}^{I} = (S_{23}^{III})^{T} \\
S_{33}^{III} &= (S_{33}^{II})^{-1} - (S_{43}^{II} (S_{33}^{II})^{-1})^{T} W (S_{44}^{I} - S_{44}^{II})^{-1} S_{43}^{II} (S_{33}^{II})^{-1}
\end{aligned}
$$

where

$$
W (S_{44}^{I} - S_{44}^{II})^{-1} = [S_{44}^{I} - S_{44}^{II} + S_{43}^{II} (S_{33}^{II})^{-1} S_{34}^{II}]^{-1} \tag{2.37}
$$

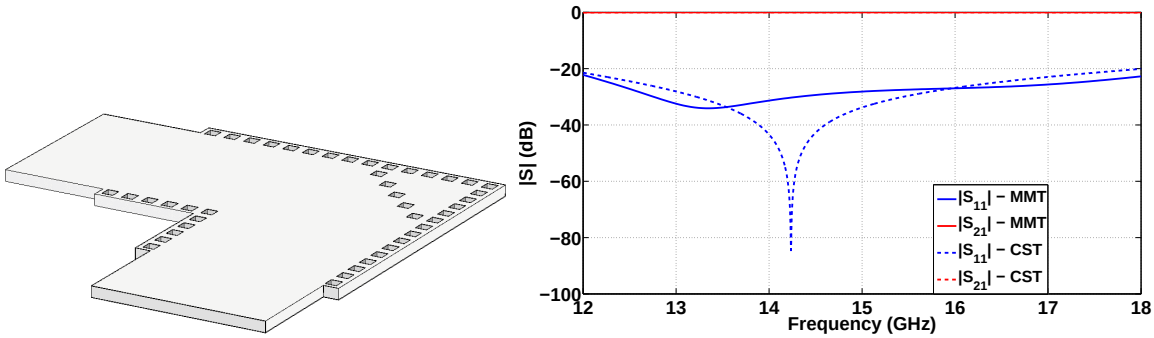


Figure 2.28: Layout and performance of an SIW corner. MMT data (solid line) has been compared with CST data (dashed line).

Based on the above theory, two SIW T-junctions have been designed and analyzed (Figure 2.26(a) and Figure 2.27(a)). The MMT has been compared with CST data in Figure 2.26(b) and Figure 2.27(b). The good agreement validates the accuracy of the proposed analytical method.

2.5.1 MMT Analysis of SIW Corner

For the analysis of SIW corners, one of the branching ports of the SIW T-junction is short-circuited (e.g., port 2 in Figure 2.25(c)), and the final S-parameters of the SIW corner can be extracted from the S-parameters presented in Equation 2.36 as:

$$\begin{bmatrix} b_1 \\ a_3 \end{bmatrix} = \begin{bmatrix} S_{11}^{corner} & S_{12}^{corner} \\ S_{21}^{corner} & S_{22}^{corner} \end{bmatrix} = \begin{bmatrix} a_1 \\ b_3 \end{bmatrix};$$

$$\begin{aligned} S_{11}^{corner} &= S_{11}^{III} + S_{12}^{III}.(-I - S_{22}^{III})^{-1}.S_{21}^{III} \\ S_{12}^{corner} &= S_{13}^{III} + S_{12}^{III}.(-I - S_{22}^{III})^{-1}.S_{23}^{III} \\ S_{21}^{corner} &= S_{31}^{III} + S_{32}^{III}.(-I - S_{22}^{III})^{-1}.S_{21}^{III} \\ S_{22}^{corner} &= S_{33}^{III} + S_{32}^{III}.(-I - S_{22}^{III})^{-1}.S_{23}^{III} \end{aligned} \tag{2.38}$$

The SIW corner layout along with its performance is presented in Figure 2.28. Again, it can be seen that good agreement between CST and MMT results has been achieved.

2.6 MMT Analysis of Lossy SIW Structures

It is stated in Section 1.2 that the mechanism of dielectric and conductor losses in the SIW circuitry is similar to that of in a dielectric filled waveguide. Note that losses can be easily incorporated in the MMT approach by considering the loss tangent of the dielectric, $tan\delta$, and the conductivity of the metal, σ, for propagating modes in all individual waveguide and microstrip sections. In order to consider dielectric losses in our MMT approach, k in Equation 2.13 for TE_{m0} modes should be written as:

$$k = \omega\sqrt{\mu\epsilon} = \omega\sqrt{\mu\epsilon_0\epsilon_r(1 - j\tan\delta)} \tag{2.39}$$

Thus, instead of Equation 2.13, k_{zm} is calculated as below :

$$k_{zm} = j\gamma = j(\alpha_d + j\beta) = \sqrt{\omega^2\mu\epsilon_0\epsilon_r(1 - j\tan\delta) - (m\pi/a)^2} \tag{2.40}$$

For considering conductor losses, α_c is added to α_d in Equation 2.40. For TE_{m0} modes in an RWG, we have [26]:

$$\alpha_c = \frac{R_s}{h\eta\sqrt{1 - \left(\frac{f_c}{f}\right)^2}}\left[1 + \frac{2h}{a}\left(\frac{f_c}{f}\right)^2\right] \tag{2.41}$$

in which $R_s = \sqrt{\frac{\pi f\mu_0}{\sigma}}$ is the surface resistance of conductors, and $\eta = \sqrt{\frac{\mu_0}{\epsilon_0\epsilon_r}}$ is the intrinsic impedance of the medium. For TE_{m0} modes in the microstrip section, α_c is also calculated from Equation 2.41.

For the TEM case in microstrip, dielectric and conductor losses can be calculated as [67]:

$$\begin{aligned} \alpha_d &= \tfrac{k_0\epsilon_r(\epsilon_e - 1)\tan\delta}{2\sqrt{\epsilon_e}(\epsilon_r - 1)} \\ \alpha_c &= \tfrac{R_s}{Z_0 W} \end{aligned} \tag{2.42}$$

in which ϵ_e is the effective permittivity, Z_0 is the characteristic impedance and W is the width of the microstrip line.

It is worth mentioning that after S-parameters calculations for different types of discontinuities in SIW structures, a toolbox can be designated to each individual discontinuity with certain structural parameters, and then the calculated S-parameters can be deployed in future calculations.

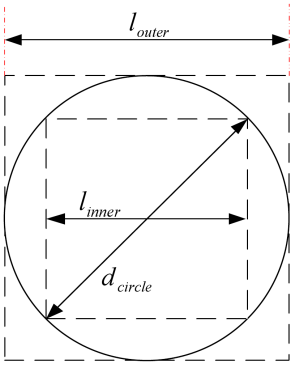


Figure 2.29: The circle with diameter d_{circle} and its inscribed and circumscribed squares with length l_{inner} and l_{outer}, respectively [41].

2.7 Equivalence Between Circular and Square Vias

In [41], Buchta and Heinrich investigated the equivalence between cylindrical and rectangular via holes in an RWG in electromagnetic modeling. The investigation is for $d/p < 0.5$, and for frequencies up to $140GHz$. According to this paper, among four different approaches, cases 3 and 4 are best choices for dimensions of rectangular vias to replace cylindrical vias. If l is the side length of the square via and d the diameter of the cylindrical via, the four approaches are as follows.

1. The most simple approach is to use the same side length as the cylindrical diameter:

$$l_{same} = d_{circle} \tag{2.43}$$

2. Another approach is to equal the cross-sectional area of the rectangular and cylindrical vias:

$$l_{cross} = d_{circle}\frac{\sqrt{\pi}}{2} \tag{2.44}$$

Two further variants are approximating the cylindrical cross-section using as side length the arithmetic or geometric means of the inscribed l_{inner} and circumscribed square l_{outer} as shown in Figure 2.29.

3.

$$l_{arith} = (l_{inner} + l_{outer})/2 = d_{circle}(1/\sqrt{2} + 1)/2 \tag{2.45}$$

4.

$$l_{geo} = \sqrt{(l_{inner}.l_{outer})} = \sqrt{1/\sqrt{2}}.d_{circle} \tag{2.46}$$

l_{inner} and l_{outer} are depicted in Figure 2.29.

Of these four methods, the third one turned out to give consistently the best results even for advanced SIW configurations (for the practical range of the d/p ratio in SIW applications, which is $0.5 < d/p < 0.8$ according to [19]). Thus, this equivalence, which is based on S-parameters equivalence for both reflection and transmission, has been chosen in our studies. With this simple relationship, an SIW device can now be designed with either circular or square via holes and can then be translated to the respective other via shape.

In Chapter 4, different SIW components with circular vias, analyzed by the MMT method with square vias as presented in this chapter, will be presented.

Chapter 3

Excitation of SIW Structures

As it is mentioned in Chapter 1, SIW technology has proven to be a promising alternative to conventional waveguides for the design of microwave and millimeter-wave circuits compatible with planar technologies. As the field patterns inside the SIW are similar to that of rectangular waveguides, the design of any SIW structure starts with specifying the waveguide width for the desired frequency band and substrate material. Therefore, the equivalent waveguide width (W_{equi}) of the SIW is of fundamental design importance.

In addition, transitions between SIW and other planar topologies like microstrip and CPW are needed in order to provide means to excite and measure these components. More importantly, low-reflection transitions to microstrip are required to integrate and combine SIW circuits with active components such as amplifiers [68].

In the first section of this chapter, a review of previous formulations for calculating W_{equi} is presented, and then a new analytical formula for calculating the equivalent waveguide width of the SIW based on the MMT analysis presented in Chapter 2 will be introduced. In the second section, different transition topologies between microstrip and SIW are reviewed, and then a new wideband microstrip-to-SIW transition with minimum return loss is presented.

3.1 Equivalent Waveguide Width of SIW

3.1.1 Literature Review

The first and most simple relationship between the SIW width a_{SIW} and its effective waveguide width W_{equi} (cf. Figure 3.1) was reported in 2002 [69]. Via diameter d

and via pitch p are shown in Figure 3.1. In [69], dispersion properties of the SIW are investigated using the BI-RME method combined with the Floquets theorem. From that method, the cutoff frequencies of the first two modes of the SIW are approximated and by comparison with the equivalent waveguide, a formula for the effective waveguide width of the SIW is reported (Equation 3.1).

$$W_{equi} = a_{SIW} - \frac{d^2}{0.95p} \tag{3.1}$$

However, it is stated in [18] that the formula presented in Equation 3.1 does not take into account the effect of $\frac{d}{a_{SIW}}$, and when d increases, a small error will appear [18]. The formula was slightly modified empirically in 2005 [18] as:

$$W_{equi} = a_{SIW} - 1.08\frac{d^2}{p} + 0.1\frac{d^2}{a_{SIW}} \tag{3.2}$$

In 2004, an empirical formula for the normalized equivalent SIW width, $\overline{a} = \frac{W_{equi}}{a_{SIW}}$, was presented [70]. The formulation is presented in Equation 3.3.

$$\overline{a} = \zeta_1 + \frac{\zeta_2}{\frac{p}{d} + \frac{\zeta_1+\zeta_2-\zeta_3}{\zeta_3-\zeta_1}} \tag{3.3}$$

where

$$\zeta_1 = 1.0198 + \frac{0.3465}{\frac{a_{SIW}}{p} - 1.0684}$$
$$\zeta_2 = -0.1183 - \frac{1.2729}{\frac{a_{SIW}}{p} - 1.2010}$$
$$\zeta_3 = 1.0082 - \frac{0.9163}{\frac{a_{SIW}}{p} + 0.2165}$$

In 2006, the frequency-dependent W_{equi} was obtained from experimental data [71], but a direct design equation is not provided.

In [72], an MoM approach was used to calculate a_{SIW} in terms of W_{equi}. The equivalence between SIW structure and rectangular waveguide is established based on comparing the surface impedances along the side walls of the SIW and of a rectangular waveguide, and the relation is:

$$a_{SIW} = \frac{2W_{equi}}{\pi} cot^{-1}\left(\frac{p\pi}{4W_{equi}} \ln\frac{p}{2d}\right) \tag{3.4}$$

Equation 3.4 implies that when via diameter d is less than half of the via-spacing p, width W_{equi} is larger than a_{SIW}, and vice versa. When via diameter d is equal to half of the via-spacing p, W_{equi} equals a_{SIW}. This means that the row of vias becomes a solid conductive plane causing a total reflection of the electromagnetic waves with a 180° phase shift [72]. In order to calculate W_{equi} in terms of SIW structural parameters based on Equation 3.4, one should utilize recursive algorithms.

Finally, in [73] the unit cell of a via hole and the dielectric space to its neighbour was approximated by electric walls and solved as a rectangular waveguide discontinuity. The SIW's effective waveguide width W_{equi} was then calculated and a correction term was added for more accurate results (Equation 3.5).

$$W_{equi} \cong \frac{a_{SIW}}{\sqrt{1+(\frac{2a_{SIW}}{p})(\frac{d}{a_{SIW}-d})^2-\frac{4a_{SIW}}{5p^4}(\frac{d^2}{a_{SIW}-d})^3}} \tag{3.5}$$

These five different models [69, 18, 70, 72, 73] have been compared in [74] for different ratios of via diameter to via pitch, d/p (Figure 3.1). It was found that the accuracies of such formulas vary depending on the d/p ratio. Therefore, the design of an SIW would often proceed using an inferior equivalent-width formula. However, no new design formulas are presented in [74].

For the design engineer, the use of such equations (with the exception of the simplest one in [69]) is not straightforward as the design parameter a_{SIW} is embedded in the computation of equivalent width W_{equi}. For the equation that so far provides the best design based on our investigation [70], an iterative process or the solution of a fifth-order polynomial would be required to design the actual SIW parameter a_{SIW}. Similar complexity is involved using [73]. Only [72] presents a_{SIW} as a function of W_{equi}. However, the approach in [72] is found to be far less accurate than the models presented in [69, 18, 70, 73].

3.1.2 New Relation Between SIW Width and Equivalent Waveguide Width Based on the MMT

In this section, a new formula based on the MMT is presented for the design of the actual SIW width a_{SIW} in terms of the equivalent waveguide width W_{equi}, which determines the frequency range and bandwidth of the SIW. The formula is based on the reflection from an all-dielectric waveguide of width W_{equi} to an SIW of width a_{SIW}. If that reflection is the lowest, then the actual SIW width is best adjusted to

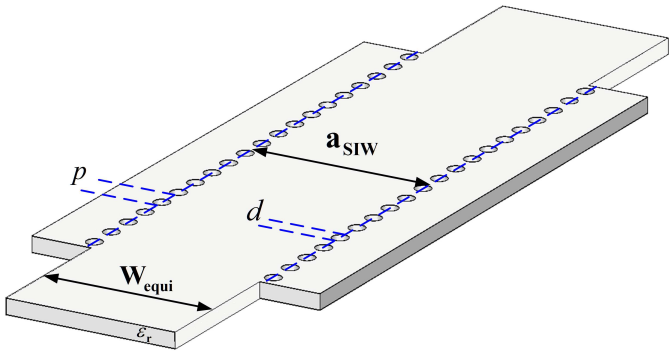


Figure 3.1: Structural parameters of the discontinuity between an all dielectric waveguide and the SIW structure.

the equivalent width.

Figure 3.1 shows the structural parameters of an SIW structure with width a_{SIW}, consisting of 20 pairs of via holes with diameter d and via pitch p, and with all-dielectric waveguide ports of width W_{equi}. This structure is analyzed with the MMT method presented in Chapter 2 ([1]) that uses a circular-to-square via conversion such that the square vias' side lengths are equal to the arithmetic mean of the side lengths of the inscribed and circumscribed squares of the circular via [5].

In order to obtain the best value for a_{SIW}, with W_{equi}, d and p given, the input reflection coefficient of the transition is minimized by varying a_{SIW}. Note that during this process, the number of via-hole pairs in Figure 3.1 was changed a few times by approximately a quarter wavelength to make certain that the low reflection coefficient was not influenced by the combination of the two (input and output) discontinuities of the structure (cf. Figure 3.4). This entire procedure was repeated for the practical range of different d/p ratios which, in order to avoid leakage loss in SIW structures and make fabrication realizable, should lie between 0.5 and 0.8 [19].

Figure 3.2 shows the obtained a_{SIW}/W_{equi} ratios versus d/p and compares them to those values found in the literature [69, 18, 70, 72, 73]. It is observed that our results based on the MMT are closest to that of [70], but the empirical formula in [70] does not allow a direct design of a_{SIW}. It is also observed that the values reported in [69, 18, 73] are in relatively close vicinity. However, the results based on [72] are far from the other methods. Based on the optimum width a_{SIW} obtained from the investigation described above, the nonlinear least squares technique is used to obtain

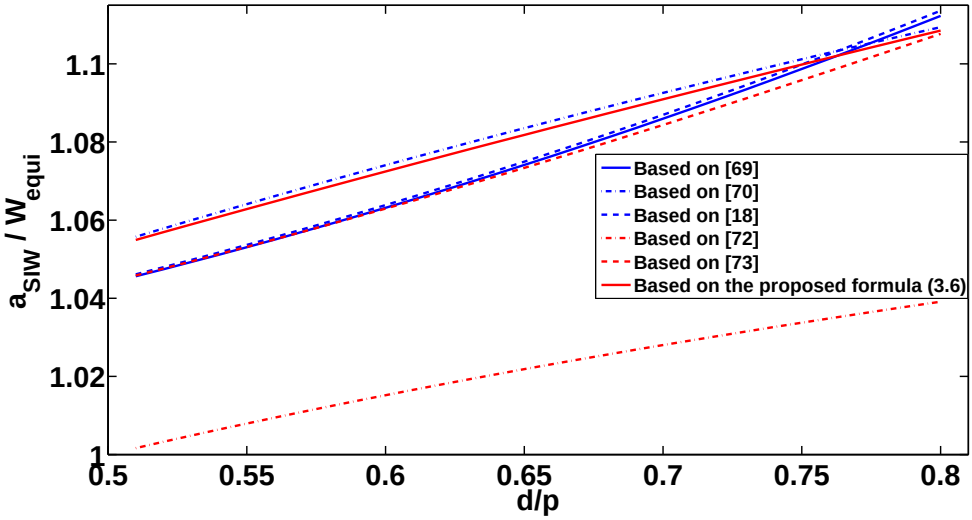


Figure 3.2: a_{SIW}/W_{equi} ratios of different formulas reported in the literature for $W_{equi} = 5.828mm$, $p = 1mm$, on a substrate with $\epsilon_r = 2.94$.

the final formula for the design of a_{SIW}.

$$a_{SIW} = W_{equi} + p(0.766e^{(0.4482d/p)} - 1.176e^{(-1.214d/p)}) \tag{3.6}$$

The error of this equation is within 1.2×10^{-3} percent of the original data. Note that due to the normalization, this formula is independent of the relative permittivity of the substrate and frequency. The applicable range of Equation 3.6 covers all practical SIW applications for which $0.5 < d/p < 0.8$ [19]. For these limits, $a_{SIW} - W_{equi}$ varies between $0.318p$ and $0.651p$ which is consistent with the fact that a_{SIW} is always larger than W_{equi} and that larger vias require more lateral spacing (Figure 3.1) to match the same equivalent width W_{equi}. For the design of an SIW, the cutoff frequency f_c, substrate permittivity ϵ_r and d/p ratio ($0.5 < d/p < 0.8$) are specified. Then the SIW width a_{SIW} is immediately obtained from Equation 3.6 once the effective width W_{equi} is calculated from Equation 3.7, where c is the speed of light.

$$W_{equi} = \frac{c}{2f_c\sqrt{\epsilon_r}} \tag{3.7}$$

3.1.3 Validation of the Proposed Formula

Three different design examples illustrate the usefulness of the proposed formula Equation 3.6. For different substrates, frequency bands and d/p ratios, the in-

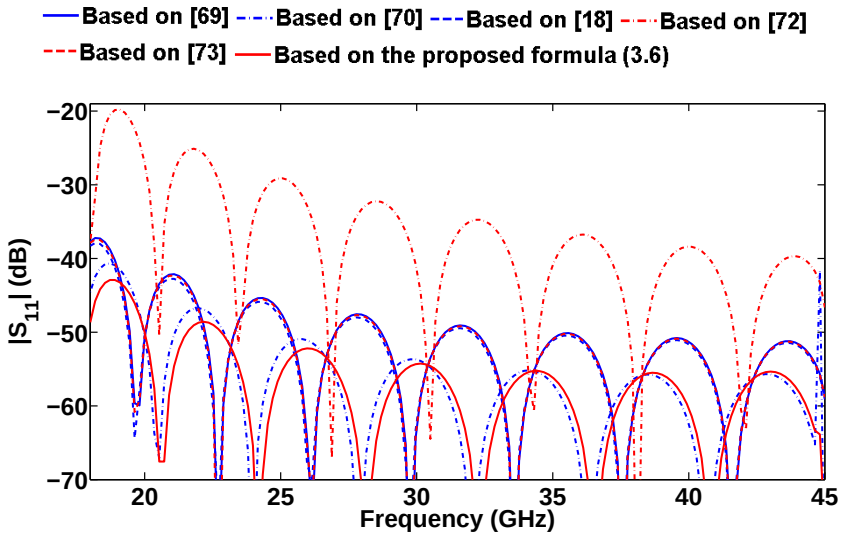
put reflection coefficient of the structure in Figure 3.1 is calculated using the μWaveWizard and presented in Figure 3.3. In each example, the result based on a_{SIW} of Equation 3.6 is compared to those of [69, 18, 70, 72, 73].

As the first example, we are considering an RT/duroid 6002 substrate with $\epsilon_r = 2.94$, height $h = 0.508mm$ and $f_c = 15GHz$, resulting in $W_{equi} = 5.828mm$ according to Equation 3.7. The via pitch is chosen such that we have at least twelve vias per guided wavelength. Thus $p = 1mm$ and $d = 0.55mm$ are selected ($d/p = 0.55$). Figure 3.3(a) shows input reflection results for different a_{SIW} obtained from different formulas reported in the literature and Equation 3.6. It is observed that the a_{SIW} calculated with the proposed formula Equation 3.6 yields the best return loss. (Note that due to symmetry reasons, the theoretical bandwidth is extended to $3f_c$).

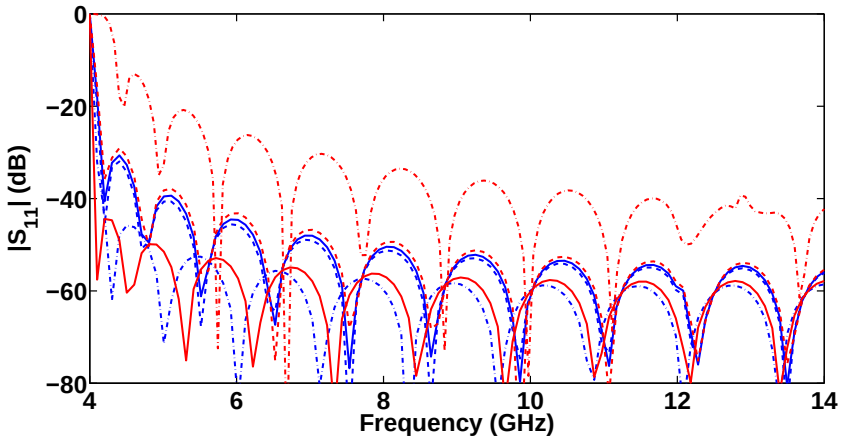
As the second example, we are using RT/duroid 6010 with $\epsilon_r = 10.2$ and height $h = 1.27mm$. We are interested to work in the C-band so that Equation 3.7 yields $W_{equi} = 11.7336mm$ for $f_c = 4GHz$. $p = 2mm$ and $d = 1.36mm$ are chosen so that $d/p = 0.68$. Figure 3.3(b) shows the reflection coefficients for different a_{SIW} obtained from the literature and from Equation 3.6. As it can be seen, the calculated a_{SIW} based on the proposed formula Equation 3.6 yields the minimum return loss when the entire frequency band is considered.

The third example uses RT/duroid 6006 with $\epsilon_r = 6.15$ and substrate height $h = 0.508mm$. The frequency range is X-band, and we obtain $W_{equi} = 8mm$ for $f_c = 7.56GHz$. The via dimensions are selected as $p = 1.2mm$ and $d = 0.96mm$ ($d/p = 0.8$). Figure 3.3(c) shows the input reflection coefficients for different a_{SIW} obtained from [69, 18, 70, 72, 73] and from Equation 3.6. As can be expected from Figure 3.2 ($d/p = 0.8$), the calculated a_{SIW} based on the different formulas (except for [72]) are really close which is confirmed in Figure 3.3(c). Note that at such a high d/p ratio, which is not often used in practice, the simplest formula [69] provides slightly better results.

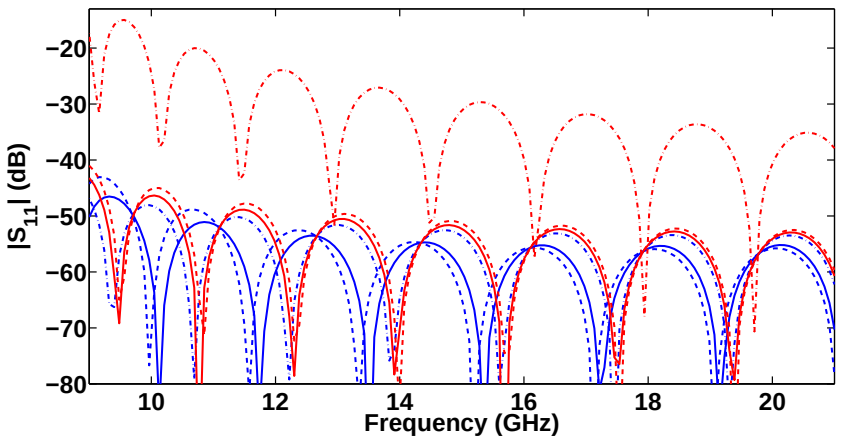
From the plots presented in Figure 3.3, the reflection coefficient of the SIW structure with all-dielectric waveguide ports with SIW width based on [72] are between $-20dB$ to $-30dB$ for all three cases. Those based on the [69, 18, 73] are between $-40dB$ to $-50dB$. The best return loss of the structure for $d/p < 0.75$ is obtained with the empirical width from [70] and the width proposed in Equation 3.6 with a few dB improvement compared to [70]. However, in order to calculate a_{SIW} according to [70], the roots of a fifth-order polynomial need to be calculated. In all different structures, the SIW widths calculated based on these two formulations, lead to the



(a)



(b)



(c)

Figure 3.3: Return loss investigation of an SIW structure with waveguide ports with μWaveWizard for different formulations. The structural parameters are: (a) RT/duroid 6002 ($\epsilon_r = 2.94$), $W_{equi} = 5.828mm$, $d = 0.55mm$, $p = 1mm$; (b) RT/duroid 6010 ($\epsilon_r = 10.2$), $W_{equi} = 11.734mm$, $d = 1.36mm$, $p = 2mm$; (c) RT/duroid 6006 ($\epsilon_r = 6.15$), $W_{equi} = 8mm$, $d = 0.96mm$, $p = 1.2mm$.

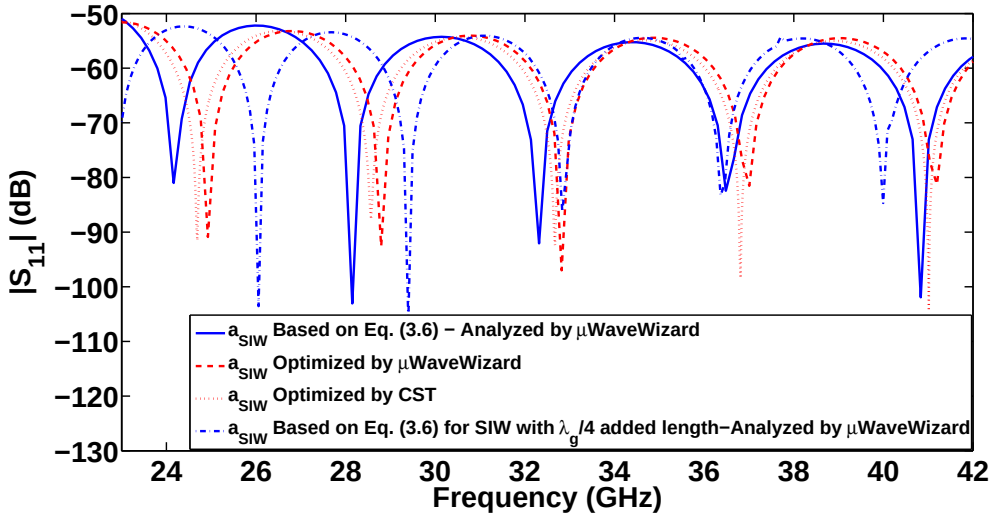


Figure 3.4: Comparison between reflection coefficients of an SIW structure with waveguide ports, for three different values of a_{SIW}: a_{SIW} based on Equation 3.6 (solid line), a_{SIW} based on Equation 3.6 for SIW with quarter of wavelength added line (dashed-dotted line),optimized a_{SIW} with μWaveWizard (dashed line) and CST (dotted line). The structural parameters are: RT/duroid 6002 ($\epsilon_r = 2.94$), $W_{equi} = 5.828mm$, $d = 0.55mm$, $p = 1mm$.

reflection coefficient between $-50dB$ and $-60dB$. For $d/p > 0.75$, all different formulations (except for [72]) result in almost the same value for a_{SIW}, as it can be seen in Figure 3.2.

In Figure 3.4, we are demonstrating that once a_{SIW} is obtained from Equation 3.6, further attempts by optimization to find an a_{SIW}, which might provide better return loss than that given by Equation 3.6, either in μWaveWizard or in CST, will not result in better performance. This confirms the robustness of the formula presented in Equation 3.6. Note that in this and previous figures, the ripples are related to the length of 20 via-hole pairs between the two discontinuities at the input and output (Figure 3.1). Of course, the number of minima changes with the SIW length or number of via-hole pairs. It is important to observe though that the levels of the maxima do not change; in other words, the level of reflection is independent of the interaction between the input and output discontinuities. This is demonstrated in Figure 3.4 by adding three SIW pairs which corresponds to an additional line length of approximately a quarter-wavelength.

Therefore, that proves that the formula for the design of SIW components presented in Equation 3.6 allows the design engineer to directly obtain the optimum

SIW width without solving more complicated formulas presented in the literature. Moreover, it is demonstrated that further optimization of the SIW width does not improve the excellent performance obtained with the new formula.

3.2 Microstrip to SIW Transition

As discussed earlier, transitions between SIW and other planar topologies like microstrip and CPW are needed in order to provide means to excite and measure these structures. More importantly, low-reflection transitions to microstrip are required to integrate and combine SIW circuits with active components such as amplifiers, e.g., [68]. In such applications, it is vital to provide low-reflection transitions so that the component design is independent of the influences of the transitions.

3.2.1 Literature Review

The first interconnect introduced is the microstrip taper [75], and it is still the most widely used type of microstrip-to-SIW transition in single-layered circuits. In [76], the design formula for this type of transition is presented and it is stated that it is generally possible to obtain a return loss (RL) better than $20dB$ over the full waveguide bandwidth [76]. A microstrip-to-SIW transition with bandwidth of about 24% and with return loss of about $15dB$ for a back-to-back transition in Ku-band is presented in [77]. Another narrow band microstrip-to-SIW transition at $60GHz$ in LTCC technology is presented in [78]. A return loss of about $15dB$ in the $58-64GHz$ range (about 10% bandwidth) is reported. In [79], a microstrip-to-SIW transition within a multilayered substrate is introduced. With this transition, a bandwidth of 14.5% ($23.2-27.1GHz$) at $15dB$ return loss is obtained. A single-layer DC-coupled microstrip-to-SIW transition using an interdigital configuration is reported in [80]. A return loss about $15dB$ is achieved within a 25% bandwidth centered at $12.5GHz$.

Also in 2007, another microstrip-to-SIW transition on LTCC substrate is presented [81]. The return loss for a single transition is reported as $15dB$ within a 30% bandwidth. A microstrip-to-SIW transition based on an exponential instead of a linear taper is presented in [82]. The return loss is about $20dB$ over a 15% bandwidth at $18GHz$. A transition between SIW and a differential microstrip line in multilayered substrate is presented in [83]. Over a $10GHz$ bandwidth at $35GHz$ (28%), a return loss of $10dB$ is achieved. In [84], different types of microstrip tapers

in microstrip-to-SIW transitions are investigated and a new design approach based on electromagnetic (EM) simulation is presented. Although the resulting transitions yield return losses better than $30dB$, the structures are very narrow band (5.5% at $11GHz$). The parallel HMSIW is suggested as transition between microstrip line and SIW structure in [85]. This transition relies on the suppression of the dominant higher order TE_{20} mode, and hence has enhanced bandwidth compared to the conventional microstrip taper. It is stated that the proposed transition has a return loss better than $25dB$ for $1.25f_c - 1.9f_c$ with $f_c = 8.6GHz$ [85].

And finally, another narrow band microstrip-to-SIW transition is presented in [86]. According to [86], and for relatively thick substrates, when the characteristic impedance of the SIW is greater than that of the microstrip, the presented transition has better performance compared to the regular microstrip taper. However, except for one case which has a return loss of about $20dB$ between $15GHz$ and $40GHz$, other presented examples in [86] are narrow band.

3.2.2 New Microstrip-to-SIW Transition

The most common type of microstrip-to-SIW transition in single-layered circuits is the microstrip taper. It not only provides acceptable return loss but is also wideband and operates over a full waveguide bandwidth [76]. In this section, we first investigate the effect of the substrate height h (Figure 3.5) on the tapering topology and then present our new transition which improves the return loss significantly compared to the regular microstrip taper. The new transition, which consists of a microstrip taper plus two added vias, proves to be the most wideband microstrip-SIW transition available with minimum return loss.

Effect of Substrate Height on Microstrip Taper

Figure 3.5 presents a single microstrip taper transition from microstrip line to the SIW. The other port is terminated with a regular waveguide port.

In this figure, a_{SIW} is the SIW width, d is the diameter of the vias, p is the via pitch, w_m is the width of the microstrip line, W_{equi} is width of the waveguide port, w_t is the taper width, L_t is the taper length, h is the substrate height, and ϵ_r is the relative permittivity of the substrate.

For the design of an SIW structure, the cutoff frequency f_c of the dominant mode TE_{10}, substrate permittivity ϵ_r and d/p ratio (which should be in the practical range

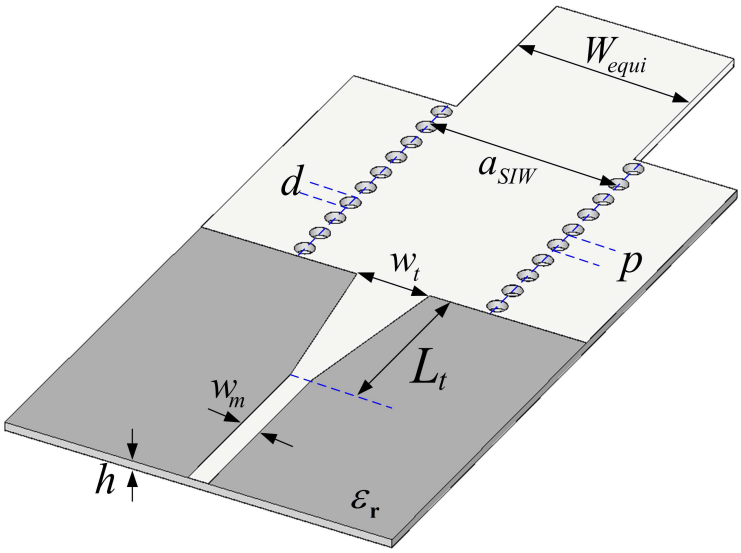


Figure 3.5: Structural parameters of a single microstrip taper transition between a microstrip line and an SIW.

of d/p ratios, i.e., $0.5 < d/p < 0.8$ [19]) are specified. The via pitch is usually chosen such that at least ten vias per guided wavelength are obtained at center frequency. The substrate thickness h is selected based on availability from manufacturers. The cutoff frequencies for the standard waveguide operating frequency bands are presented in [15]. Then the SIW width a_{SIW} is immediately obtained from Equation 3.6, once the effective width W_{equi} is calculated from Equation 3.7.

In order to excite and integrate an SIW structure with a microstrip port, the first step is to choose w_m so that the characteristic impedance of the microstrip line, Z_0^{MS}, becomes 50Ω at the center frequency of the desired frequency band. Also, it should be noted that depending on the chosen h, the characteristic impedance of the SIW structure, Z_0^{SIW}, differs from 50Ω, and so different tapering topologies between microstrip line and SIW structure appear. In most SIW structures, h is small enough so that the characteristic impedance of the SIW structure Z_0^{SIW} is less than 50Ω. This situation results for the microstrip taper to taper out ($w_m < w_t$) which is the most common type of transition (Figure 3.5). A typical example of such a transition and its performance in Ku-band ($12.4 - 18GHz$) is shown in Figure 3.6(a).

Depending on application, however, higher values of h are sometimes required. In this case, the impedance Z_0^{SIW} of the SIW is greater than 50Ω, and a microstrip taper design results in a taper-in transition ($w_m > w_t$) as shown in Figure 3.6(b). This latter case, in which $Z_0^{SIW} > Z_0^{MS}$, is considered in [86]. (Note that the results of our

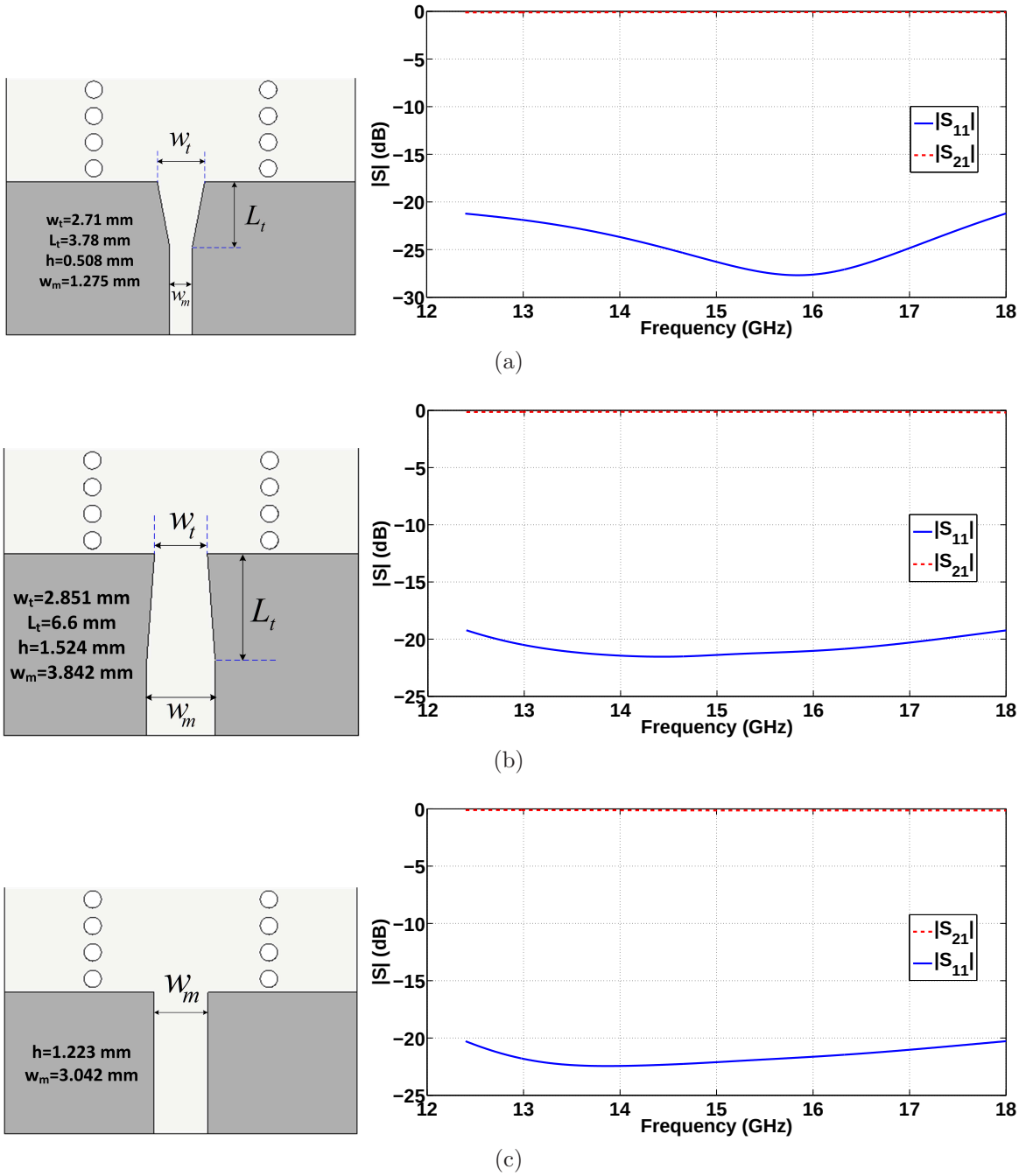


Figure 3.6: Effect of substrate height h on the microstrip taper topology; Ku-band designs and performances: (a) taper-out, (b) taper-in and (c) no-taper topologies.

new microstrip-to-SIW transition have been compared with a taper-out transition (not shown here). It is concluded that the taper-out configuration does not provide the best possible performance in this situation.)

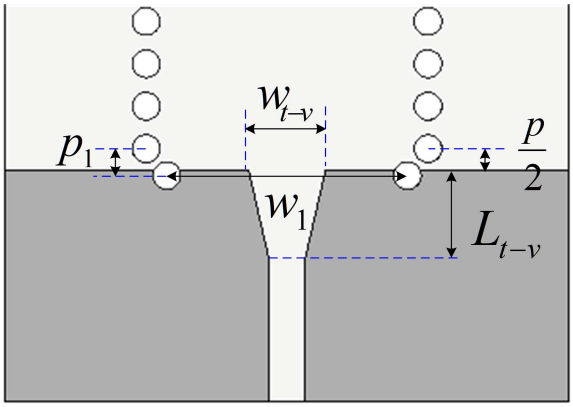


Figure 3.7: Structural parameters of the new taper-via transition between microstrip line and SIW.

Since for some values of h we have taper-in transitions and for some other values taper-out transitions, there should be an h at which no microstrip taper is needed ($w_m = w_t$) as $Z_0^{SIW} = Z_0^{MS}$ for exactly that substrate height. The corresponding example is demonstrated in Figure 3.6(c). This value of h can be found by deploying full-wave software optimizers. In the optimizer, we set $w_m = w_t$, and try to find h and w_m such that the $|S_{11}|$ is minimum for $Z_0^{MS} = 50\Omega$ at center frequency. Figure 3.6(c) presents such a h_{nt} (no-taper h), where no taper between the microstrip line and the SIW is required. This height h_{nt}, is listed in Table 3.1 for all investigated frequency bands in this paper. It basically provides guidance to the design engineer for choosing an appropriate substrate height.

Taper-Via Transition

The new microstrip-to-SIW transition, termed taper-via transition, is presented in Figure 3.7. This transition adds two vias to the conventional microstrip taper. The inserted vias are placed symmetrically at both sides of the taper and have the same dimensions as the SIW vias, so there is no need to use a different drill size in the fabrication process. In this figure, p_1 is the distance between the inserted via and the first via in the side wall of the SIW, and w_1 is the distance between the inserted vias. L_{t-v} and w_{t-v} are the length and width of the microstrip taper, respectively.

The advantage of the new configuration compared to the microstrip taper alone is that the field is more confined in lateral direction, and thus a better match from the microstrip to SIW is provided.

The variations of the normalized input impedance, $z_{in} = Z_{in}/Z_0^{MS} = r_{in} + jx_{in}$,

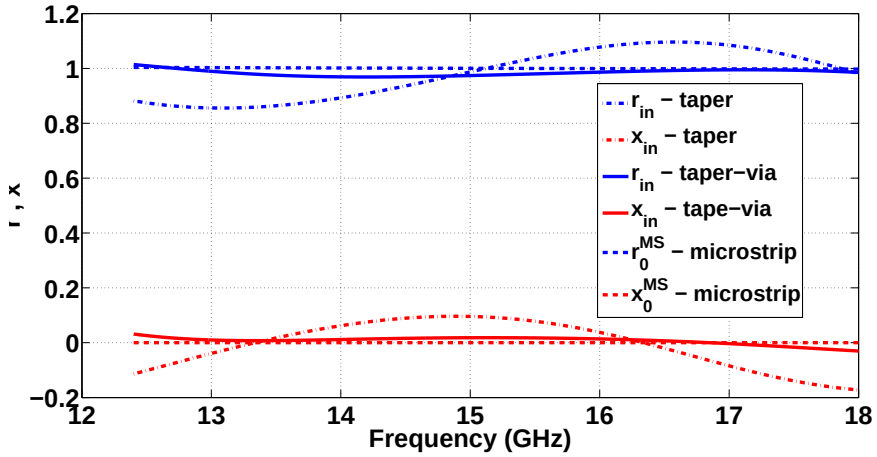


Figure 3.8: Comparison between real (blue) and imaginary (red) parts of the input impedance for three different cases: structure with taper transition (dotted-dashed line), structure with taper-via transition (solid line), microstrip line (dashed line).

with frequency are plotted Figure 3.8 for both taper and taper-via transitions and are compared with the normalized characteristic impedance of the microstrip line. It is observed that the taper-via transition provides an input impedance closer to Z_0^{MS}, compared to the conventional taper transition, which proves that better matching between the microstrip line and the SIW structure is achieved.

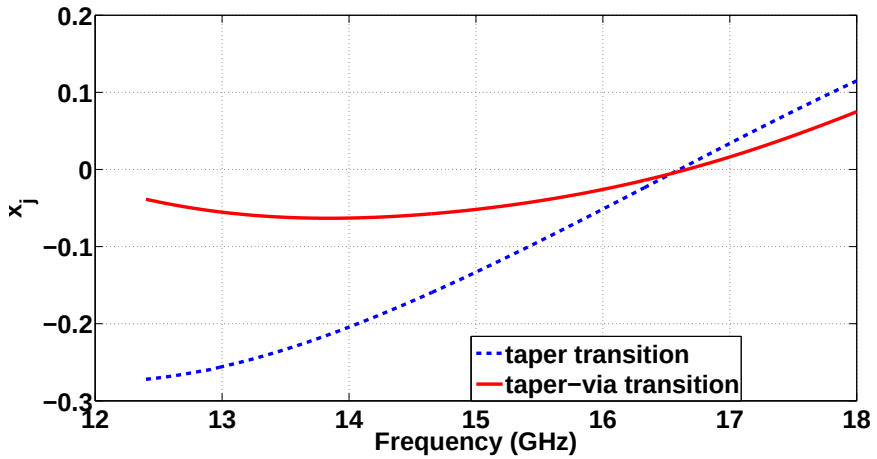
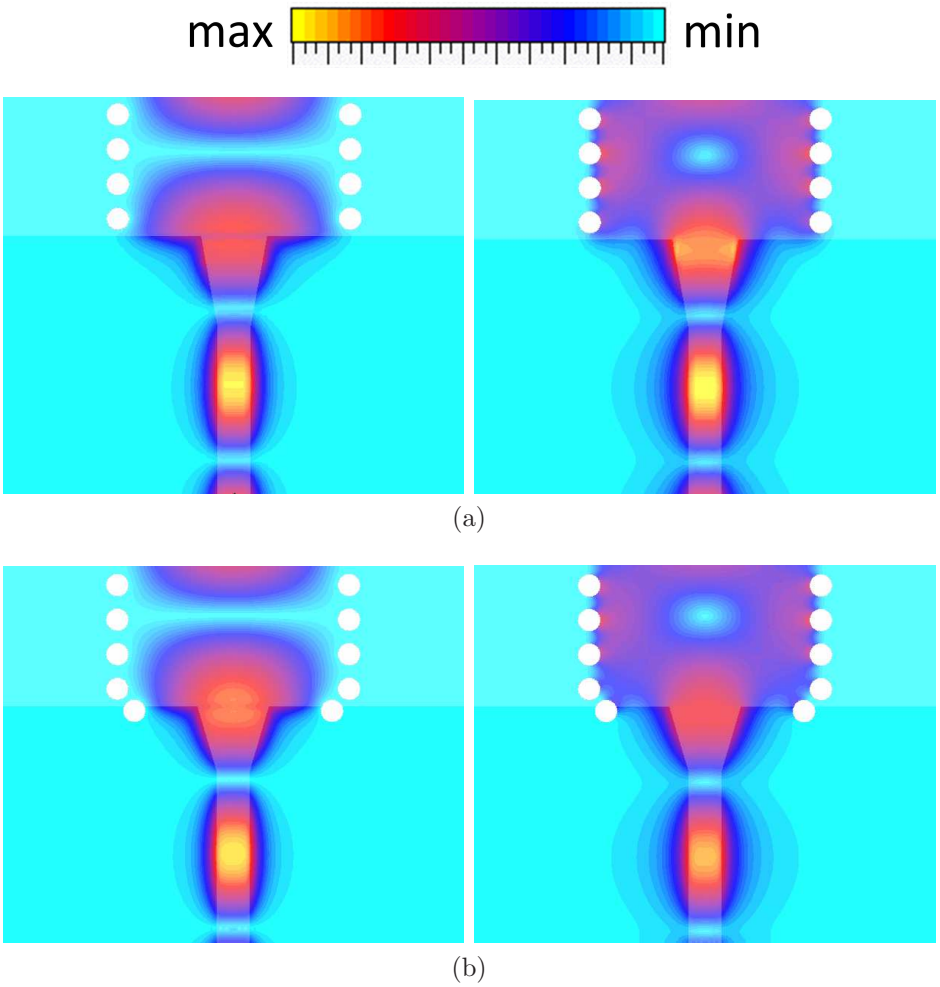


Figure 3.9: Normalized reactance comparison in the microstrip-to-SIW junction plane for both taper (dashed line) and taper-via (solid line) transitions.

In order to investigate the nature of this improved performance achieved by the proposed transition, the normalized reactance of the microstrip-to-SIW junction (x_j) is compared for both taper and taper-via transitions. As shown in Figure 3.9, the

added vias to the taper transition compensate the reactance effect of the microstrip taper-to-SIW transition in the junction plane and provide an overall reactance that is, over the entire bandwidth, smaller than that of the regular transition.



(a)

(b)

Figure 3.10: Electric (left) and magnetic (right) field patterns of transitions between a microstrip line and an SIW: (a) conventional taper, (b) new transition.

The field patterns in the new transition are also compared to those of the conventional microstrip taper and presented in Figure 3.10. In all four cases in Figure 3.10, the same scaling has been adopted so that the a_{SIW} and d are exactly the same. Also, the phase of the incident wave has been chosen so that for both transitions, the maximum E-field occurs at the beginning of the SIW structure. The H-fields are plotted at the same phase. As it is observed, by confining the field better, the new transition results in better matching between microstrip and SIW and thus has lower return loss. When the proposed transition is deployed, the electromagnetic field of

the microstrip line attaches itself better, e.g., with lower fringing fields, thus reduced lateral field extension, at the SIW interface, to the vias (Figure 3.10(b)) compared to the traditional taper (Figure 3.10(a)).

Based on the new configuration in Figure 3.7, transitions in different microwave frequency bands from $8.2GHz$ to $90GHz$ have been designed. In all cases, the performance of the new transition is compared with that of the conventional microstrip taper. The substrate material in this investigation is chosen as RT/duroid 6002 with effective permittivity $\epsilon_r = 2.94$ for both taper and taper-via transitions. (Note that design formulas that will be introduced in Section 3.2.3 can be applied to other substrates.) The SIW structure consists of ten rows of vias. Taper-via transition parameters w_{t-v}, L_{t-v}, p_1, w_1 (cf. Figure 3.7) are optimized in the frequency-domain solver of CST Microwave Studio in order to maximize the return loss of a single transition over the entire waveguide band. The optimized parameters are presented in Table 3.1.

Optimized parameters of conventional tapers (w_t, L_t) are also presented in Table 3.1. It is worth mentioning that the optimized parameters of the conventional tapers differ from values obtained from the formulation presented in [76]. In each frequency band, the substrate height h is chosen so that we have taper-out microstrip-SIW transitions ($h < h_{nt}$) as they are much more common than taper-in transitions. For this height (h), w_m is calculated so that we have $Z_0^{MS} = 50\Omega$ at the center frequency.

In Figure 3.11, the reflection coefficients of the new transitions are compared with those of the conventional microstrip taper in each frequency band. It is observed that the new transitions show return losses better than $30dB$ within each frequency band if the dielectric height is chosen properly (cf. Table 3.1). (Note that a direct scaling process of the new transition to other bands would involve the height of the substrate material and will result in substrate heights that are not readily available from suppliers.) The new transition has significantly improved performance compared to the conventional taper transition. For the E-band, the $5mil$ ($0.127mm$) substrate is the only option provided by the manufacturer for maintaining $h < h_{nt}$. The new E-band transition (Figure 3.11(f)) still outperforms the conventional taper transition by close to $6dB$ in this case. However, if a thinner substrate is available (cf. Figure 3.12), for example, PTFE-glass dielectrics; TLT: $\epsilon_r = 2.45 - 2.65$, $h = 2mil = 0.0508mm$, TLX: $\epsilon_r = 2.45 - 2.65$, $h = 2mil = 0.0508mm$, TLE: $\epsilon_r = 2.95 - 3$, $h = 1.5mil = 0.0381mm$ [87], the performance improvement of the new transition is more significant

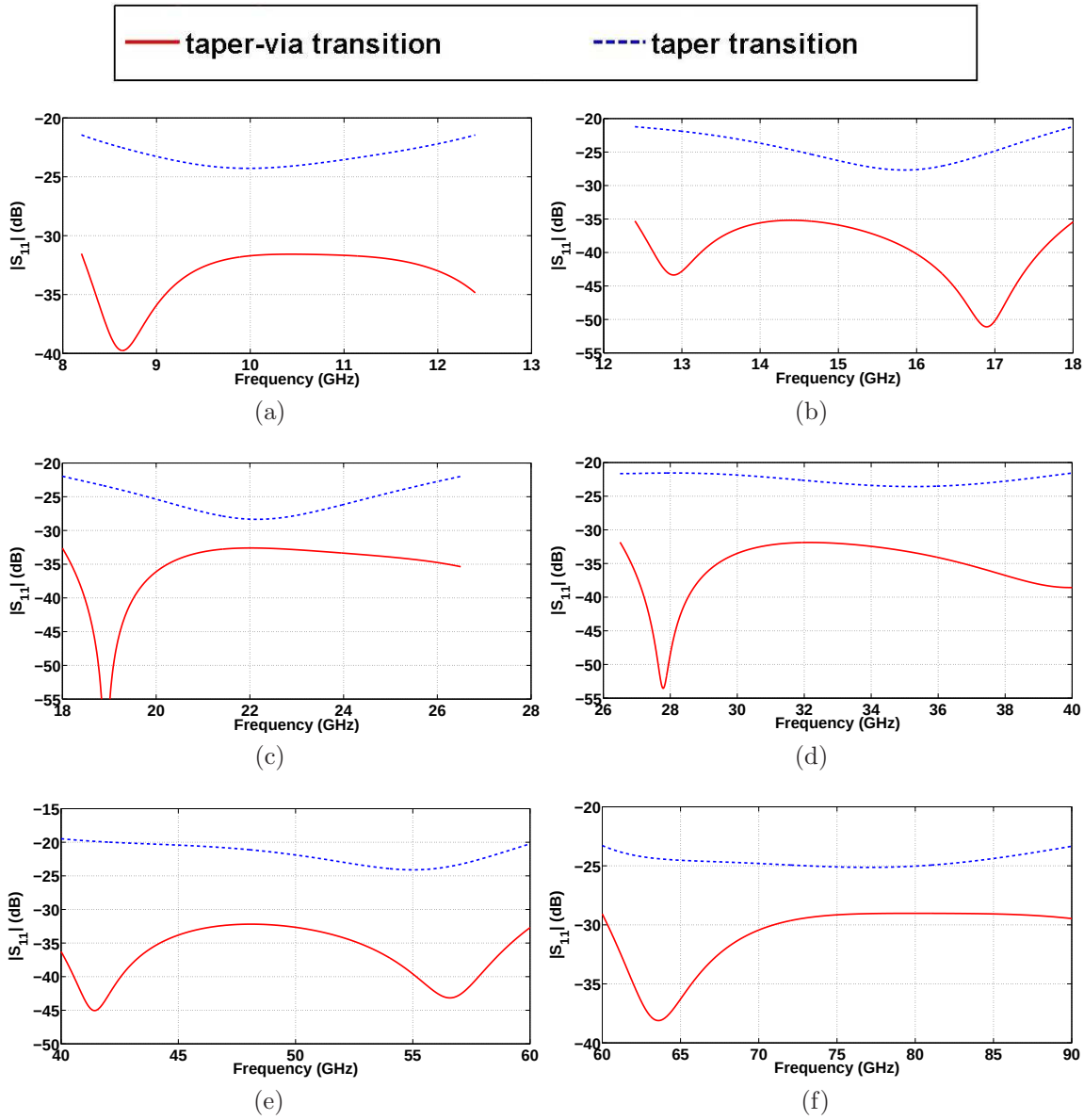


Figure 3.11: Comparison between reflection coefficients of the conventional microstrip transition (taper transition - dashed line) and the new transition (taper-via transition - solid line) for different frequency bands: (a) X-band, (b) Ku-band, (c) K-band, (d) Ka-band, (e) U-band, and (f) E-band; transition parameters according to Table 3.1.

compared to the taper alone. The minimum return loss values of all transitions in Figure 3.11 are also presented in Table 3.1.

Freq. band (GHz)	**X-band 8.2-12.4**	**Ku-band 12.4-18**	**K-band 18-26.5**	**Ka-band 26.5-40**	**U-band 40-60**	**E-band 60-90**
$f_c(GHz)$	6.557	9.488	14.051	21.077	31.391	48.373
$p(mm)$	2.2	1.5	1	0.7	0.45	0.3
$d(mm)$	1.43	0.975	0.65	0.455	0.2925	0.195
$a_{SIW}(mm)$	14.4124	9.9502	6.7126	4.4913	3.0058	1.9545
$h_{nt}(mm)$	1.6623	1.2233	0.7990	0.5298	0.3616	0.2210
$h(mm)$	0.762	0.508	0.381	0.254	0.127	0.127
$w_m(mm)$	1.9161	1.2754	0.9520	0.6358	0.3213	0.3165
$w_t(mm)$	3.8868	2.7142	1.8881	1.2476	0.7647	0.5739
$L_t(mm)$	5.2611	3.7760	2.5375	1.5357	1.1104	0.6667
$RL(dB)$	**21.46**	**21.20**	**21.97**	**21.56**	**19.47**	**23.28**
$w_{t-v}(mm)$	4.1697	2.7533	2.0365	1.3252	0.7784	0.6275
$L_{t-v}(mm)$	4.2722	3.1088	1.8908	1.3168	0.9630	0.5458
$w_1(mm)$	12.3678	8.4486	5.7314	3.9182	2.5078	1.7016
$p_1(mm)$	1.4791	0.9494	0.6357	0.4387	0.2840	0.2417
$RL(dB)$	**31.53**	**35.2**	**32.6**	**31.84**	**32.19**	**29.02**

Table 3.1: Structural parameters of the taper transition and taper-via transition between microstrip line and SIW structure at different frequency bands.

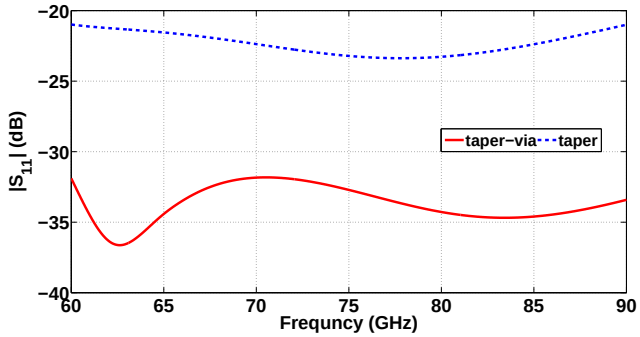


Figure 3.12: Comparison between reflection coefficients of the conventional microstrip transition (taper transition - dashed line) and the new transition (taper-via transition - solid line) for E-band and smaller height. The dielectric is RT/duroid 6002 with height $0.1mm$. The microstrip port width is $0.2512mm$.

3.2.3 Design Formulation

Based on the values presented in Table 3.1, we extract formulas for the direct design of the new transition in Figure 3.7. After calculation of SIW and microstrip parameters for the desired frequency band, the next step for designing a taper-via transition is to calculate the transition parameters w_{t-v}, L_{t-v}, p_1, w_1 based on the following simple formulations:

$$L_{t-v} = 0.2368\lambda_{g-ms} \tag{3.8a}$$

$$w_{t-v} = 0.1547a_{SIW} + w_m \tag{3.8b}$$

$$p_1 = 0.6561p \tag{3.9a}$$

$$w_1 = 0.8556a_{SIW} \tag{3.9b}$$

in which λ_{g-ms} is the guided wavelength of the microstrip line calculated at the center frequency:

$$\lambda_{g-ms} = \frac{\lambda_{g0}}{\sqrt{\epsilon_{reff}}} \tag{3.10}$$

λ_{g0} is the wavelength in free space, and ϵ_{reff} is the effective dielectric constant of the microstrip line, both calculated at the center frequency. As it can be seen from Equation 3.8, L_{t-v} is always close to a quarter of λ_{g-ms}. Also, the difference between w_{t-v} and w_m is approximately about one-eighth of a_{SIW}. The placement of the two added vias is also related to SIW parameters p and a_{SIW} (cf. Figure 3.5). Based on Equation 3.8 and Equation 3.9, the normalized root-mean-square errors of L_{t-v}, w_{t-v}, p_1 and w_1 to the original data in Table 3.1 are 3, 1.2, 3 and 0.6 percent , respectively.

Based on the proposed formulas, three examples have been investigated. Example 1 presents the new taper-via transition in V-band. The d/p ratio and the substrate are chosen as in the previous structures. Examples 2 and 3 present the performances of the two new taper-via transitions at an arbitrary frequency band of between $43.75GHz$ and $66.5GHz$ where the waveguide cut-off frequency is $35GHz$. In Example 2, the dielectric is chosen as RT/duroid 6006 with $\epsilon_r = 6.15$ and $d/p = 0.75$, and in Example 3, the dielectric is chosen as RT/duroid 5580 with $\epsilon_r = 2.2$ and $d/p = 0.55$. In each case, the performances of the new transitions (designed from Equation 3.8 and Equation 3.9) are compared with those of optimized transitions in CST.

The results are presented in Figure 3.13 with structural parameters given in Table 3.2. The structural parameters of the optimized structure by CST are pre-

sented by superscript CST, while the values obtained from the design formulas are presented by superscript design. It is observed that the presented design formulas result in transitions that perform close to the optimized performance (Figure 3.13(a), Figure 3.13(b)). In some cases, however, the performance of the transition based on the design formulas is not the best possible performance (RL around 27 dB in Figure 3.13(c) - solid line). A few optimization steps towards adjusting just one parameter (here w_1) will bring $|S_{11}|$ below $-30dB$ (dashed line in Figure 3.13(c)). Nevertheless, the examples presented in Figure 3.13 validate the simple design formulations presented in Equation 3.8 and Equation 3.9.

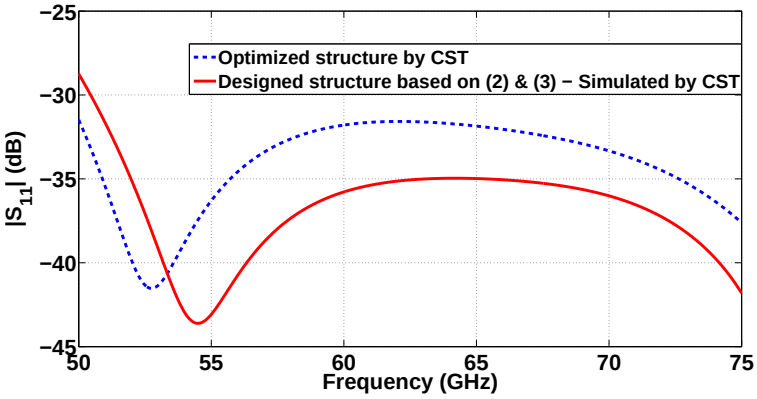
3.2.4 Measurement Results

A back-to-back version of the new taper-via transition in Ku-band has been prototyped. Figure 3.14 shows the fabricated structure under test. For measurements, a line-reflect-line (LRL) (here thru-short-line) calibration is used to de-embed the influences of the test fixture and its coaxial connectors. The calibration planes are located in the feeding microstrip lines as shown in Figure 3.14.

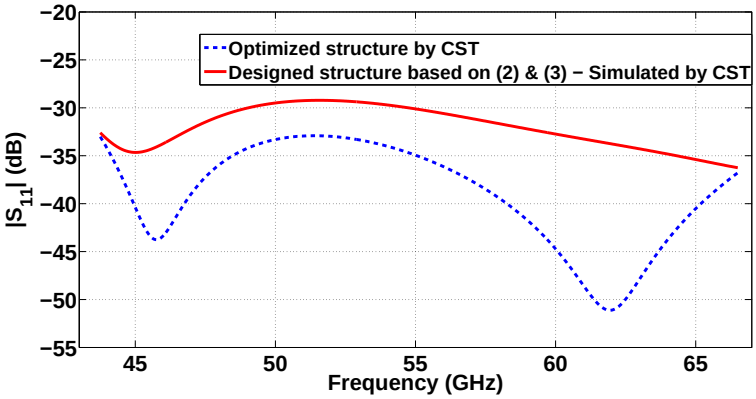
The back-to-back transition was originally designed and optimized in CST con-

Frequency band (GHz)	Example 1 50-75	Example 2 43.75-66.5	Example 3 43.75-66.5
$f_c(GHz)$	39.875	35	35
ϵ_r	2.94	6.15	2.2
$p(mm)$	0.36	0.28	0.47
$d(mm)$	0.234	0.21	0.2585
$a_{SIW}(mm)$	2.3691	1.8947	3.0646
$h(mm)$	0.127	0.127	0.127
$w_m(mm)$	0.3184	0.1815	0.3894
$L_{t-v}^{design}(mm)$	0.7126	0.5980	0.9141
$L_{t-v}^{CST}(mm)$	0.7134	0.6194	0.9141
$w_{t-v}^{design}(mm)$	0.6849	0.4747	0.8635
$w_{t-v}^{CST}(mm)$	0.6844	0.4782	0.8635
$p_1^{design}(mm)$	0.2362	0.1837	0.3084
$p_1^{CST}(mm)$	0.2599	0.1854	0.3084
$w_1^{design}(mm)$	2.0269	1.6211	2.6221
$w_1^{CST}(mm)$	2.0173	1.6146	2.5168

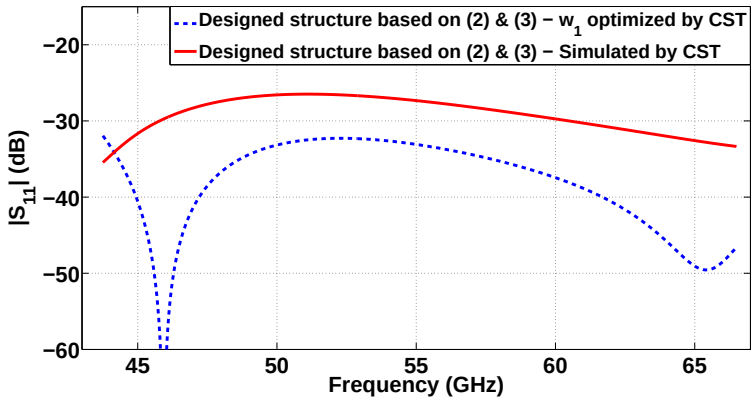
Table 3.2: Structural parameters of the taper-via transition between microstrip line and SIW structure for different examples.



(a)



(b)



(c)

Figure 3.13: Examples showing comparison between the reflection coefficient of the transition optimized in CST (blue - dashed line), and the performance of the transition designed based on Equation 3.8 and Equation 3.9 (red - solid line), cf. Table II: (a) Example 1, (b) Example 2, and (c) Example 3.

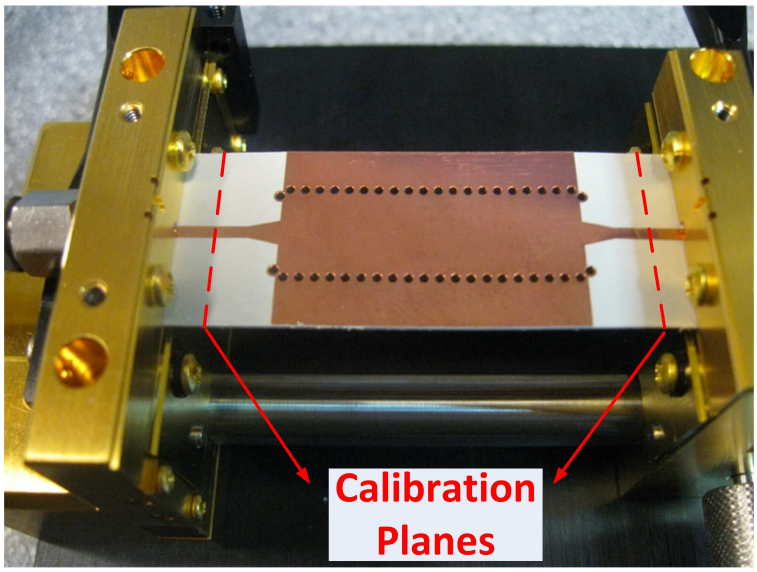


Figure 3.14: Back-to-back fabricated taper-via transition in Ku-band and indication of calibration planes.

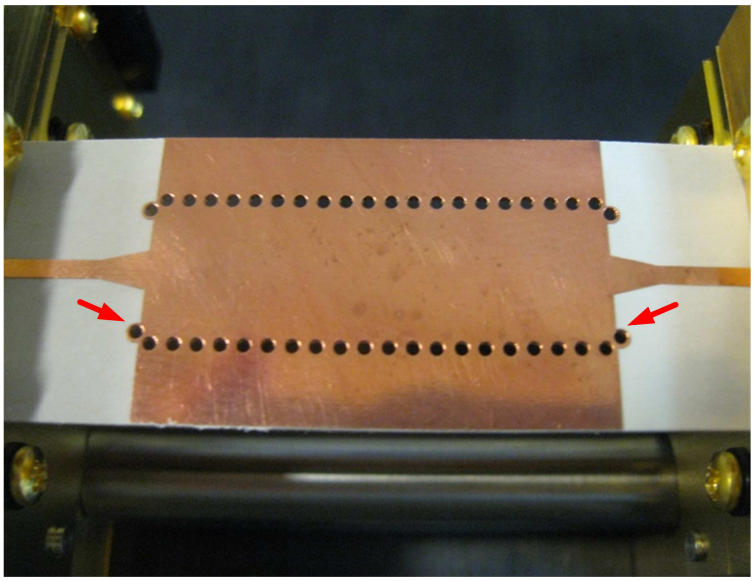
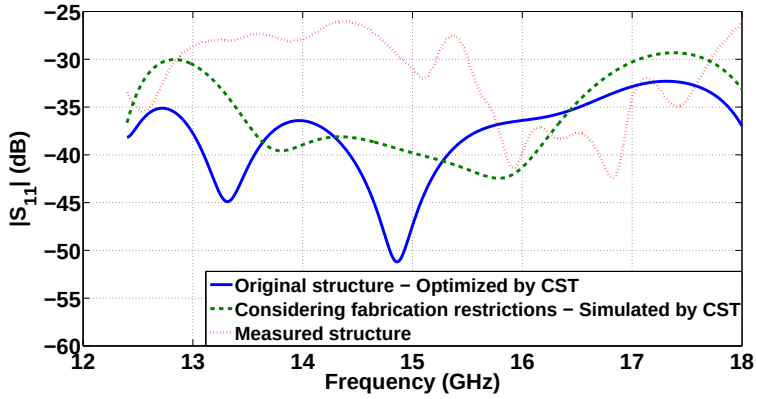


Figure 3.15: Fabricared back-to-back taper-via transition. The red arrows are pointing to the asymmetric conductor plating around outside vias.

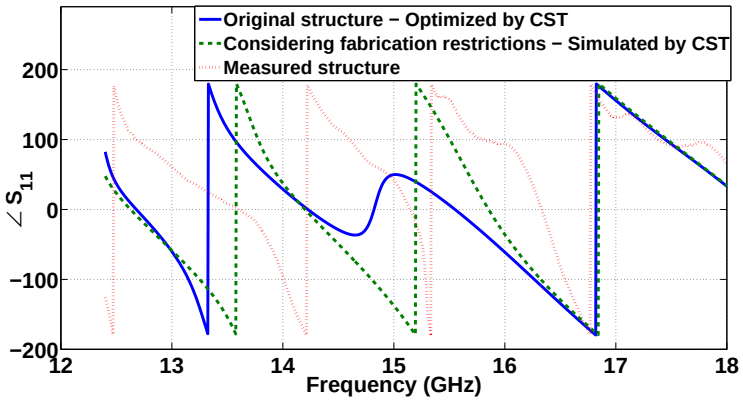
sidering dielectric and conductor losses ($tan\delta = 0.0012$, $\sigma_c = 5.8 \times 10^7 S/m$). In Figure 3.16, the performance of the originally optimized structure (solid lines) is presented. In the manufacturing process, however, a minimum amount of conductor plating was necessary around the top of the left- and right-most vias.

Also, the original via diameter of the Ku-band structure (cf. Table 3.1) was

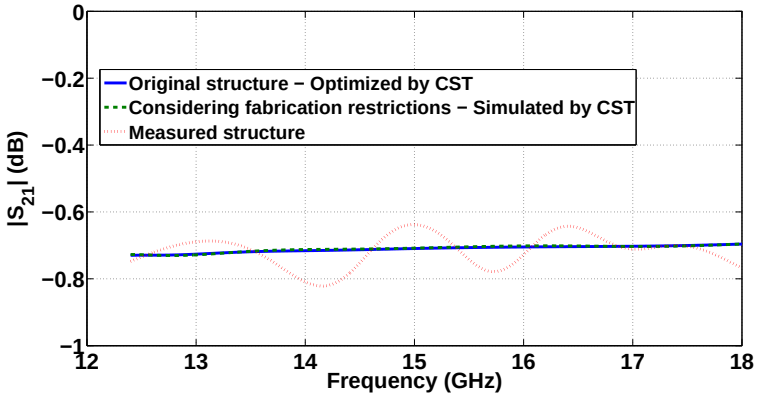
changed from $0.975mm$ to $0.965mm$ due to drill size restrictions. The structure is again simulated in CST including the fabrication restrictions, and its performance is presented in Figure 3.16 as dashed lines for comparison with measured data (dotted lines). It is worth mentioning that symmetric conductor plating around outside vias is considered in the simulation, whereas the actual plated metals in the fabricated prototype are asymmetric (cf. Figure 3.15). This is the main reason for the difference between simulated and measured results. However, the measured return loss (Figure 3.16(a), dotted line) is better than $26.05dB$ in the entire Ku-band which, to the best of the my knowledge, is the lowest measured back-to-back return loss over a full waveguide band for microstrip-to-SIW transitions reported in the literature. Also, it is worth mentioning that considering the level of the $|S_{11}|$, which is below $-25dB$, the accuracy of the measured data is adequate enough for prototyping purposes and proves the design concept. In addition, the difference between the phases of the structures (Fig. 8b) is due to the different added metal plating, as it plays significant roles in the phase response (compare the data for two simulated structures, solid line and dashed line data, in Figure 3.16(b)). Other than that, the phases have similar patterns. The maximum measured insertion loss of the fabricated back-to-back transition is $0.821dB$ (Figure 3.16(c)) and is about $0.1dB$ lower than the prediction by CST.



(a)



(b)



(c)

Figure 3.16: Comparison between the S-parameters of the original transition optimized in CST (solid lines), the structure considering manufacturing restrictions, simulated in CST (dashed lines), and the measurement data (dotted lines); a) reflection coefficient (amplitude), (b) reflection coefficient (phase), (c) transmission coefficient (amplitude).

Chapter 4

MMT Analysis and Design of SIW Passive Components

The fastest approach for designing SIW structures is to apply design procedures known for all-dielectric-filled waveguide components and then fine-optimize the structure in order to obtain a desired performance. However, optimization and sensitivity analysis of SIW structures is mostly carried out with commercially available field solvers such as CST Microwave Studio and ANSYS HFSS. Considering the large number of vias in SIW components, which results in numerous optimization parameters, it can be a cumbersome process. In order to overcome this difficulty, analytical approaches, like the proposed MMT in Chapter 2, should be adopted for the fast and efficient design of SIW components.

We have presented the S-parameter calculations of different kinds of discontinuities encountered in H-plane SIW structures. Thus, the total S-parameters of an SIW structure with square vias can be easily found. In this chapter, we present the design and analysis of passive H-plane SIW components such as filters, diplexers, couplers, and power dividers. A brief literature review on each SIW component will be presented at the beginning of each section.

4.1 SIW Filters

Filters are among the first passive components designed based on SIW technology. SIW filter design has attracted significant attention over the last few years, e.g., a three-resonator filter with off-center posts in Ka-band in 2003 [88], a four-pole direct

coupled cavity SIFW filter in X-band in 2005 [89], two four-pole iris filters at X- and V-bands in 2007 [90], also in 2007, an SIW filter based on complementary split ring resonators in X-band [91], a three-pole LTCC based SIW filter at $35GHz$ in 2009 [92], a four-resonator post filter in X-band in 2010 [93], a three-resonator iris filter at C-band in 2011 [94], and a three-resonator filter which is formed by etching slots on the top metal plane of the single SIW cavity at $140GHz$ in 2014 [95] are some examples of the reported filters based on SIW technology. Although it is well established that a reduction of one order of magnitude in unloaded Q has to be accepted in SIW filters when compared to all-metal waveguide filters, the benefits of size reduction and planar fabrication techniques in SIW outweigh the increased losses in quite a number of applications.

In this section, some filters have been designed and analyzed with the MMT method of Chapter 2. The results are verified by commercially available electromagnetic field solvers, and in some cases by measurement data.

4.1.1 Analysis of SIW Filters by MMT

For given SIW dimensions such as via diameter, spacing, substrate permittivity and height, an equivalent waveguide filter model is designed and optimized with the MMT, as available in in-house codes, or the commercial software package μWaveWizard. The dimensions of the square via holes, as derived from Equation 2.45 for a given via diameter, can be incorporated from the onset in the all-dielectric waveguide design as, e.g., post thickness, aperture thickness, etc. Such an all-dielectric waveguide prototype is then translated to an SIW structure with square via holes. Fine optimization with square vias completes the design. In this step, the MMT procedure displays its full advantage as a single analysis over a given set of frequency points is at least, depending on code implementation, ten times faster than HFSS or CST (e.g., CPU time for the MMT analysis of the filter presented in Figure 4.1 is 67 seconds, whereas it is 720 and 811 seconds for CST and HFSS simulations, respectively). Thus a simple fine-tuning run with n optimization steps will be at least $10n$ times faster than a comparable optimization in HFSS or CST. Finally, the square-via design is translated to one with circular vias, and the performance is verified with an independent numerical technique provided by commercially available software packages.

Some SIW filters have been designed ([96], [88]), based on waveguide design principles [97], with circular vias and simulated with μWaveWizard and full-wave elec-

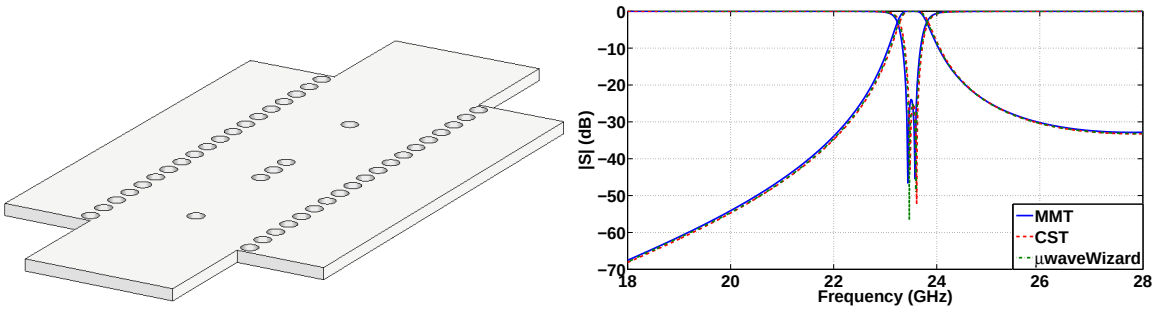


Figure 4.1: Performance comparison between square via holes (MMT) and circular vias (CST and μWaveWizard) at the example of a two-resonator post filter in SIW technology.

tromagnetic simulation packages like CST. The circular vias have been translated to proper square ones, with equivalence presented in Equation 2.45, and the structures have been analyzed with MMT.

Figure 4.1 shows a two-resonator post filter in SIW technology which has been designed by using the procedure outlined above. Note that all-dielectric waveguide I/O ports are used here as they eliminate additional influences, e.g., of microstrip feeds which are commonly used for measurement purposes. It is seen in Figure 4.1 that both the CST and μWaveWizard simulations of the filter with circular vias are in excellent agreement with the MMT design using square vias according to Equation 2.45.

Figure 4.2 shows a comparison between circular and square vias for a three-resonator dual-post filter in which the dual-post arrangements resemble inductive-iris sections as the main coupling between resonators is obtained through the centered apertures. This design was originally proposed in [96] and obtained using repeated parametric analysis in Ansoft HFSS. We recomputed the design in CST and addition-

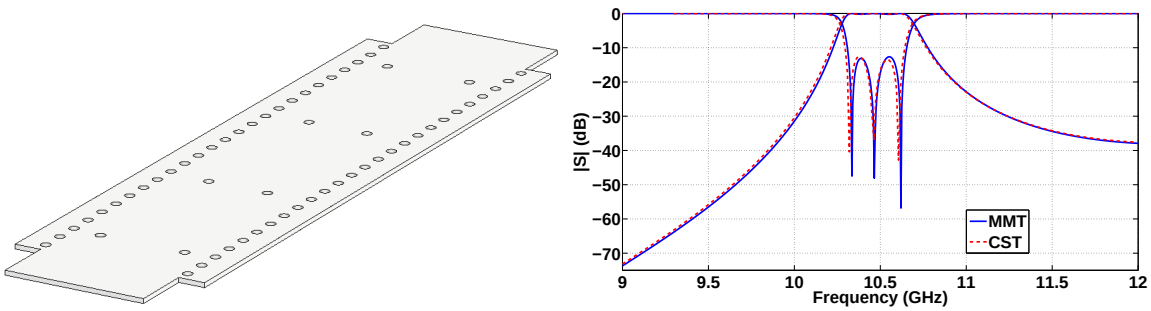


Figure 4.2: Performance comparison of square via-hole geometries (MMT) with circular vias (CST) at the example of a three-resonator post filter in SIW technology [96].

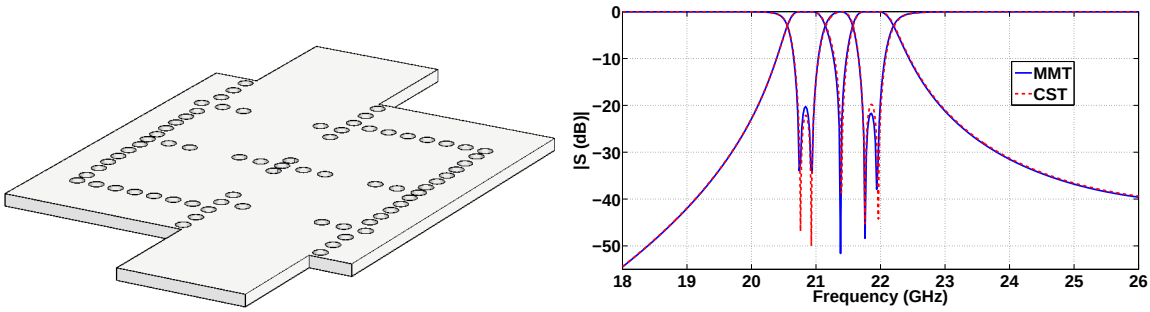
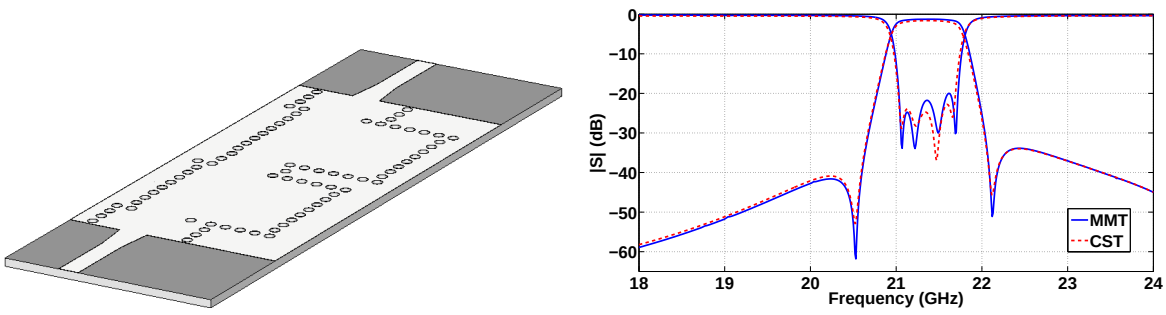


Figure 4.3: Performance comparison between square (MMT) and circular vias (CST) at the example of a four-resonator (dual-band) SIW filter with a transmission zero at midband frequency.

ally, converted the circular vias to square ones for comparison with the MMT routine. Excellent agreement between square (MMT) and circular (CST) vias is observed in Figure 4.2.

A quasi-elliptic filter design example is shown in Figure 4.3. The filter was designed with square via holes in MMT and then translated to circular vias using Equation 2.45. It is easily verified that the four-resonator routine scheme can support a single transmission zero, which, when the filter is symmetric with respect to its center, will be positioned in the center of the pass-band. Thus a dual-band filter performance with two poles in each band is obtained as shown in Figure 4.3. Note that we observe excellent agreement between the responses using square and circular via holes.

For measurement purposes or connection to other circuitry, SIW components are often equipped with microstrip transitions. Therefore, a dual-mode filter with mi-



(a) (b)

Figure 4.4: Comparison between square (MMT) and circular vias (CST) at the example of a four-pole SIW dual-mode filter.

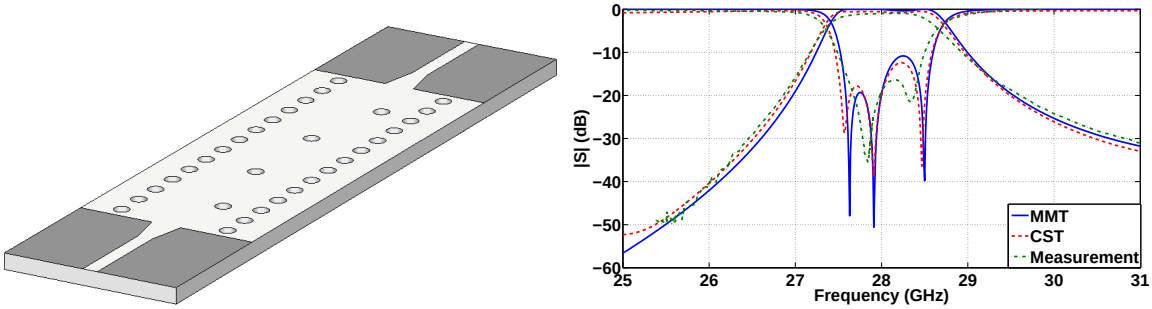


Figure 4.5: Comparison between square (MMT) and circular vias (measured [88] and CST) at the example of a three-resonator SIW filter with off-center posts.

crostrip ports is shown in Figure 4.4(a). (For the original all-metal waveguide filter design, the reader is referred to [98].) In the MMT computation, the microstrip tapers have been approximated by a three-step staircase function. The MMT performance shown in Figure 4.4(b) is that of the filter with square via holes. Dielectric and metallic losses are added by considering the respective losses of all propagating modes in waveguide and microstrip sections. The comparison with results obtained with circular via holes in CST is very good (Figure 4.4(b)). The slight discrepancies in the return loss are due to the modeling of the microstrip tapers (stair-cased in MMT and continuous in CST).

Also, Figure 4.5 shows the responses of the MMT with square vias and prototype measurements with circular vias presented in [88] for the example of a three-resonator filter with off-center posts. In the MMT computation, the microstrip tapers at each end have been approximated by a three-step staircase function. Moreover, the first set of vias at the input and output, which have been moved partly outside the bottom and top metallization in the prototype (Figure 6 in [88]) are modeled slightly differently as shown in Figure 4.5. Dielectric and metallic losses are included in the MMT simulation by considering the respective losses of all propagating modes in waveguide and microstrip sections.

The overall agreement for the filter at $28GHz$ is very good and thus demonstrates the applicability of the faster SIW filter design procedure using the MMT. The slight differences between the CST and MMT results, as compared to the previous design examples, are due to the fact that the microstrip transformers are modeled by a staircase approximation of three steps in the MMT whereas it is a continuous transformer in CST.

Also, based on the theory presented in Section 2.5.1, an SIW corner filter, which

is a four-pole iris filter, is designed and its S-parameters are presented in Figure 4.6. Please note that the discrepancy observed between MMT data and simulation data in Figure 4.6 is due to the fact that the matrix inversion in Equation 2.38 limits the number of modes considered in the MMT analysis. Other than that, for both SIW corner and SIW corner filter, the analytical data is in good agreement with the simulated data, which proves the validity of the analytical method.

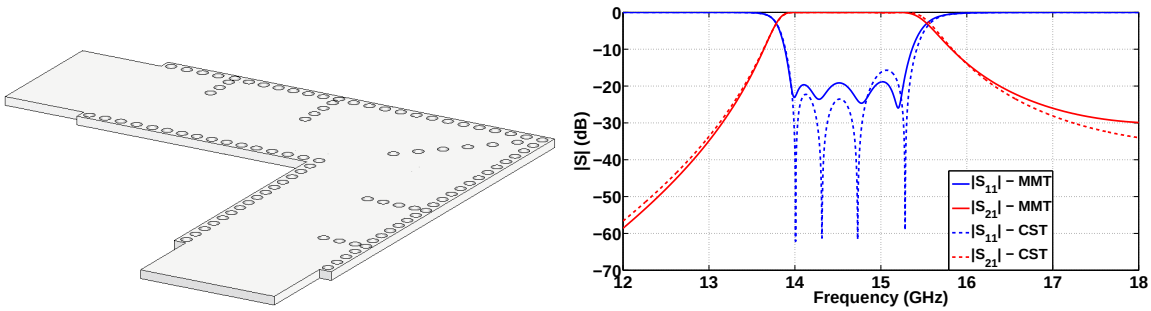


Figure 4.6: Layout and performance of an SIW corner filter. MMT data (square vias, solid line) has been compared with CST data (circular vias, dashed line).

4.2 SIW Diplexers

One of the essential passive components in front-end systems is the diplexer, which provides needed separation between transmit and receive bands. The first diplexers based on SIW technology are reported in 2005 [99, 100]. An X-band SIW diplexer using asymmetric dual-mode iris filters in a branching-port configuration is proposed in [99]. The bands of the diplexer are located at $9.7GHz$ and $10.3GHz$, respectively, and three-pole in-band filters are used at each branch [99]. A similar configuration with single-mode iris filters operates at C-band [100]. The bands of this diplexer are located at $5.42GHz$ and $5.96GHz$ using five-pole and four-pole channel filters, respectively [100]. In 2007, a diplexer designed with triplet technology is presented [101]. The diplexer has input and output ports on opposite sides of the substrate and uses iris filters, including a tri-section, at $12.1GHz$ and $11.55GHz$, respectively [101]. Also in 2007, a diplexer operating at K-band uses dual-mode SIW filters with circular and elliptic cavities [102]. The diplexer bands are located at $25GHz$ and $26GHz$, respectively [102]. An SIW triplexer with bands located at $1.9GHz$, $2.018GHz$ and $2.35GHz$ is reported in 2009 [103], but the insertion loss in one of the channels is in the order of $7dB$. In 2011, a T-junction diplexer with iris filters is presented in [104]

with bands located at $59.8GHz$ and $62.2GHz$, respectively; however, the performance is not verified by measurements. Also in 2011, the T-junction SIW diplexer in [105] uses complementary split-ring resonators at C-band. The channels of this C-band diplexer are located at $4.7GHz$ and $5.8GHz$.

In all SIW diplexers mentioned above, the optimization and tuning steps of the SIW diplexer design are carried out using full-wave commercial simulators. This is a tedious and cumbersome task, considering the large number of optimization parameters present in SIW diplexer designs. In contrast, the MMT approach adopted in this thesis is utilized for designing SIW diplexers is an order of magnitude faster than commercially available filed solvers.

The first diplexer presented in the next section is a K-band in-line SIW diplexer with bands located at $18.15GHz$ and $19GHz$, which is introduced in 2013 [9]. The SIW diplexer is similar in configuration to [101] and [103], but operates at a significantly higher frequency. Two SIW T-junction diplexers are presented afterward. One is a Ku-band T-junction SIW diplexer which its bands are placed at $14.55GHz$ and $15.85GHz$. The other T-junction diplexer is a K-band SIW diplexer with bands at $18.15GHz$ and $19GHz$. A K-band backward diplexer with bands located at $20GHz$ and $21GHz$ is also presented at the end of this section.

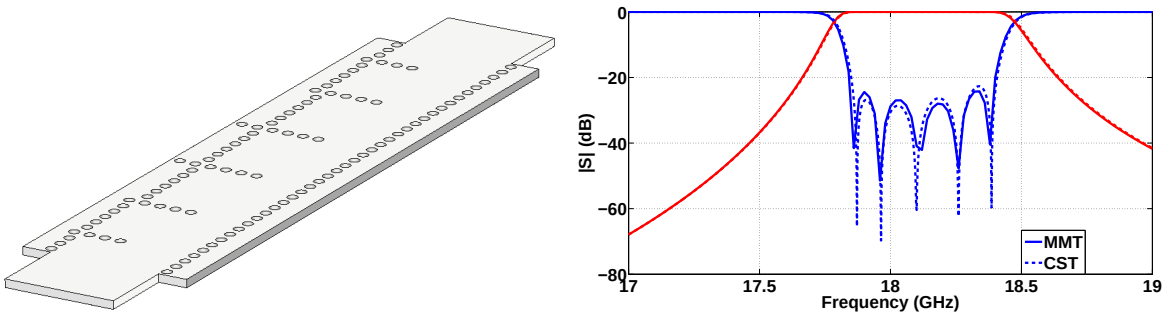
As the first step in the diplexer design, direct coupled all-dielectric waveguide iris filters are synthesized [97] using the MMT. The next step is fine optimization of the diplexer in waveguide. Then, the structure is translated to SIW technology and optimization steps using the MMT approach with square vias completes the SIW diplexer design.

4.2.1 In-line K-band SIW diplexer

A K-band diplexer based on SIW technology is presented in this section. The diplexer has input and output ports on opposite sides and bandwidths of 2.75% and 2.11% at $18.15GHz$ and $19GHz$, respectively.

During the step of fine optimization of the waveguide diplexer, the lengths of the resonators are fixed so that their equivalent lengths according to Equation 3.6 fall within the given via-diameter-to-spacing ratio of the later to be implemented SIW structure. This limits the number of optimization parameters for the SIW diplexer as only cavity widths and aperture widths need to be optimized.

The second step consists in translating the entire all-dielectric waveguide diplexer



(a) (b)

Figure 4.7: SIW filter for the lower channel of the SIW K-band diplexer. The structure is analyzed with the MMT (square vias, solid line), and the results are compared with CST data (circular vias, dashed line).

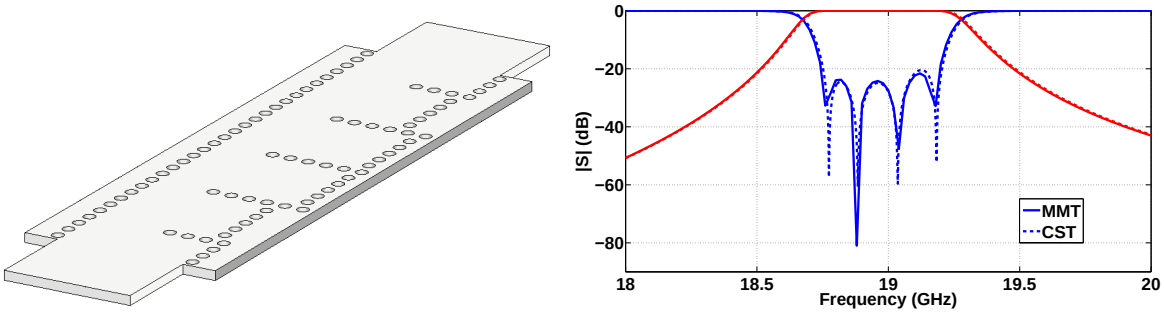
into SIW technology. A fine optimization with the MMT varies the transverse position of all via holes until a given return loss and attenuation has been reached. Note that this might not necessarily lead to a performance where all possible reflection zeros are shown. Also, the maximum number of resonators was kept to five in order to keep the prototype short enough to fit into a universal test fixture for prototype measurement purposes.

For the design of the K-band diplexer, RT/duroid 6002 with $\epsilon_r = 2.94$ is chosen as substrate. Its height is $0.508mm$ and metallization thickness is $17.5m$. The loss factors are $tan\delta = 0.0012$ for the dielectric and $\sigma = 5.8 \times 10^7 S/m$ for the copper layers and vias. The longitudinal center-to-center spacing of via holes is set to $p = 1mm$.

The channel filters of this diplexer are shown in Figure 4.7(a) and Figure 4.8(a). The channel filter at the lower band is a five-resonator filter and has a 2.75% bandwidth at $18.15GHz$, while the bandwidth for the channel filter at the higher band, which is a four-resonator filter, is 2.11% at $19GHz$. For both filters, great agreement between MMT data with square vias and CST data with circular vias has been achieved (Figure 4.7(b), Figure 4.8(b)).

After having both channel filters, as the first step we put two filters side-by-side to investigate if one row of vias can provide enough isolation between the two channels. The structure, along with its S-parameters, are presented in Figure 4.9. As it can be seen, isolation better that $50dB$ is achieved between the two channel filters.

Figure 4.10(a) depicts the layout, with five and four resonators in the lower and upper channels, and Figure 4.10(b) presents the performance of the diplexer with waveguide ports. This is an inline diplexer similar to [101], where input and output



(a) (b)

Figure 4.8: SIW filter for the higher channel of the SIW K-band diplexer. The structure is analyzed with the MMT (square vias, solid line), and the results are compared with CST data (circular vias, dashed line).

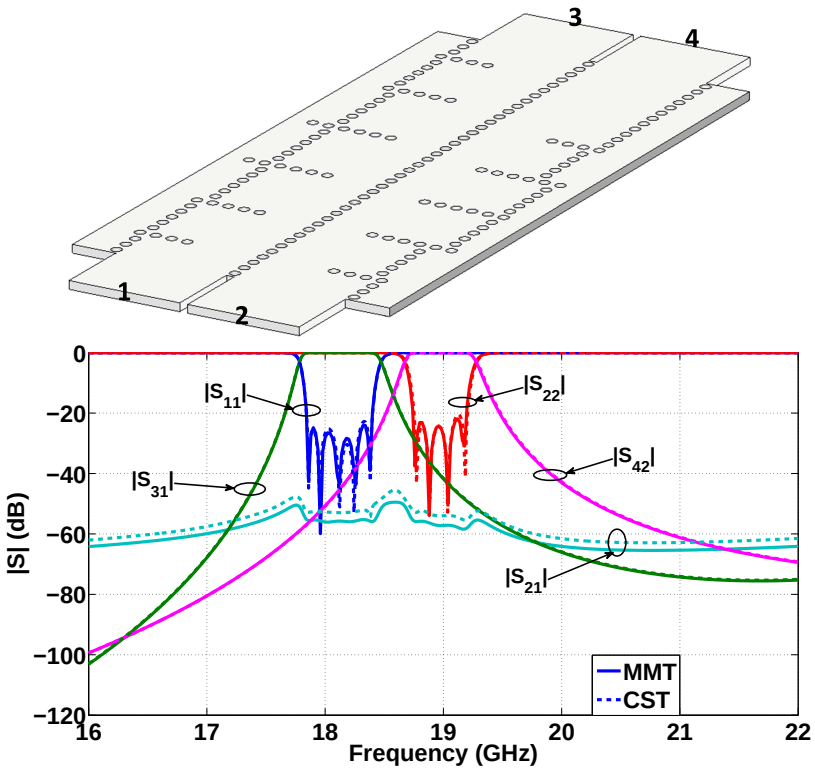
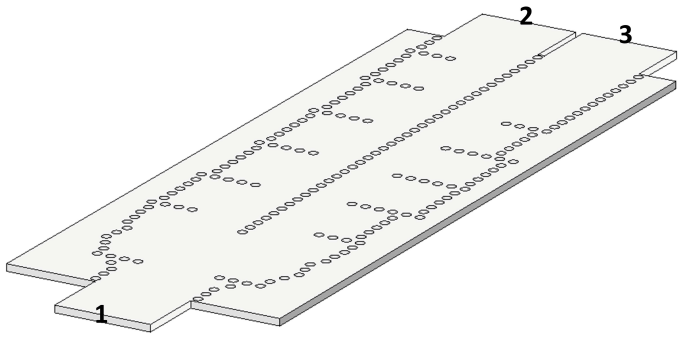
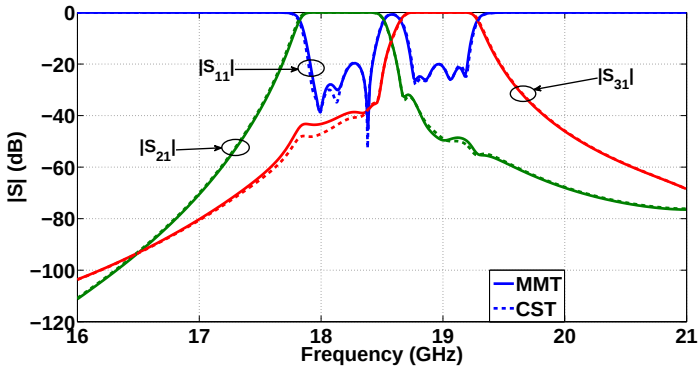


Figure 4.9: Layout and performance of a structure consist of the two channel filters side by side. The structure is analyzed with the MMT (square vias, solid line), and the results are compared with CST data (circular vias, dashed line).

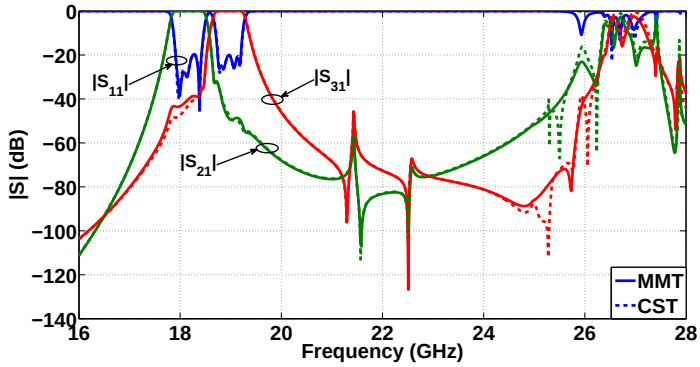
ports are located on opposite sides of the substrate. For the design with the MMT, the square vias were chosen to have side lengths of $0.55mm$ so that the equivalent circular via diameters are $d = 0.644mm$. This diplexer is designed for bandwidths of



(a)



(b)



(c)

Figure 4.10: (a) Layout of the diplexer and (b) comparison between the MMT data with square vias and CST data with circular vias for the K-band SIW diplexer with waveguide ports; (c) extended frequency range.

17.9GHz to 18.4GHz and 18.8GHz to 19.2GHz, respectively, which resemble those of 19GHz satellite specifications. The comparison between the MMT design using square vias and the CST results with circular vias is excellent.

Note that the performances shown in Figure 4.10 are calculated without the con-

sideration of losses in order to demonstrate the concept. Losses can easily be implemented as shown in Section 2.6. In order to demonstrate attenuation properties towards higher frequencies, Figure 4.10(c) shows the performance over an extended frequency range up to $26GHz$. It is observed that the attenuation is better than $40dB$ up to $25GHz$ where the harmonic filter responses start to appear.

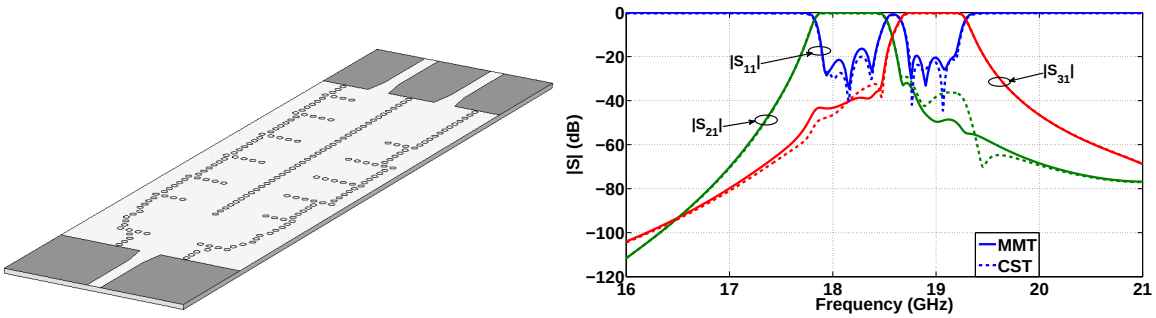


Figure 4.11: Comparison between the MMT data with square vias (solid line) and CST data with circular vias (dashed line) for the K-band SIW diplexer with microstrip ports.

In Figure 4.11, the same structure but with SIW-to-microstrip transitions at all ports is shown. The width of the microstrip ports is $w_m = 1.523mm$, and the widths and lengths of the tapers after optimization are $2.321mm$ and $2.729mm$, respectively. In the MMT analysis, the taper is approximated by small microstrip step discontinuities. That is the reason for the fact that the agreement between the MMT and CST is not as good as in Figure 4.10 where waveguide ports are used.

In order to measure the diplexer prototype, SIW ports are fitted with an SIW-to-microstrip taper. The initial parameters of the taper are chosen according to [76] and are then optimized to reach the best performance. As the two output ports of the diplexer are located close to each other, two separate structures were built. In each of the two structures, one of the output ports is curved in order to provide access with measurement equipment to the respective other port. The parameters of the bent microstrip ports, $R_c = 2w_m$, $\alpha = \pi/2$, are based on the data presented in [106], where R_c is the radius of the bend and α the curve angle. Figure 4.12 shows the layout of these two structures.

Photographs of the fabricated diplexer prototypes are shown in Figure 4.13. Although the taper can be included in the MMT analysis, the microstrip-to-SIW transitions have been deembedded in the measurements. As pointed out earlier, the two circuits are necessary to gain access to the respective ports by a universal test fixture.

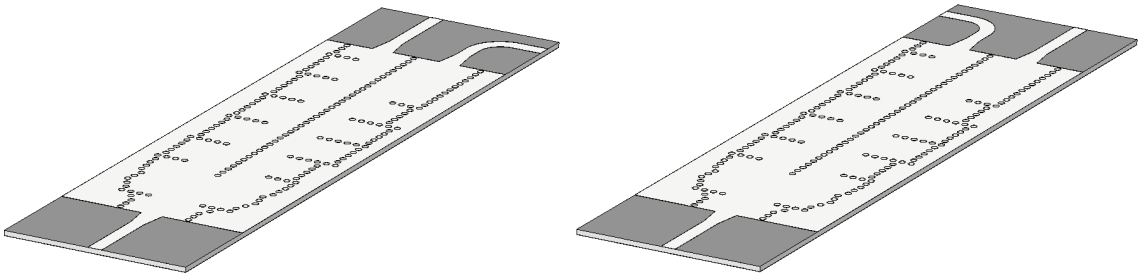


Figure 4.12: Layouts of the two K-band SIW diplexers with curved output ports.

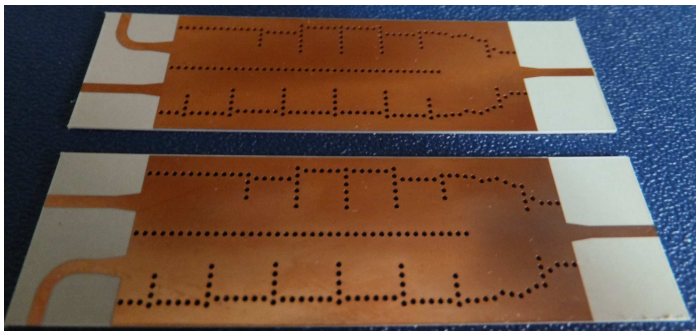


Figure 4.13: Photograph of the two fabricated diplexer prototypes with microstrip ports.

During transmission measurements, the curved ports were terminated by absorbing material.

Figure 4.14 shows a comparison between measurements and the MMT and CST predictions. Measured in-band insertion losses are $3.05dB$ and $2.3dB$ compared with $2.0dB$ and $1.8dB$, respectively, in the MMT analysis. The minimum measured return loss in the two bands is $18dB$ and $15dB$, respectively, compared to about $20dB$ in the simulation. This difference is explained by the absorbing material used for the curved ports in the measurements (Figure 4.13). This material, when placed on top of the curved microstrip ports, does not represent a matched load. Moreover, these ports could not be de-embedded from the measurements so that the SIW-to microstrip taper contributes to the reflection of such ports. Also a slight shift of the measurements towards higher frequencies is observed. This is due to the fact that the via holes of designed diameter $d = 0.644mm$ have been manufactured with an actual drill size of $0.65mm$.

The general transmission curves are also reproduced but differences in the slopes of the respective pass-bands are observed. We can only attribute these discrepancies to the measurement procedure. The actual positions and sizes of via holes have not

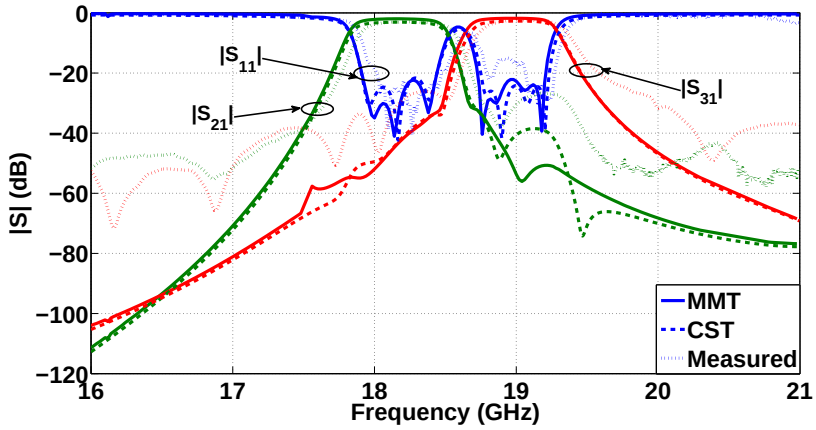


Figure 4.14: Comparison between measurements and simulation (MMT and CST) for the diplexer prototypes shown in Figure 4.13.

been measured. However, the measurements confirm in principle the simulations and the design procedure.

4.2.2 T-junction SIW Diplexer at Ku-band

In this section, the MMT approach presented in [1, 5], in conjunction with the approach for deploying MMT in analyzing SIW T-junctions Section 2.5, are adopted in order to design and analyze SIW T-junction structures, like an SIW T-junction diplexer operating at Ku-band. The diplexer bands are placed at $14.55GHz$ and $15.85GHz$, using five-pole and four-pole filters, respectively. The design of the T-junction diplexer starts with the design of two channel filters. The first channel filter with the bandpass located at the lower frequency band is a 5-pole filter and has 4.12 percent bandwidth at $14.55GHz$. This SIW filter is designed and analyzed based on the MMT for SIW structures with square vias, and the analytical data is compared with simulated data with circular vias from CST in Figure 4.15.

The other filter operating at the higher frequency band is a 4-pole filter and has 3.79% of bandwidth at $15.85GHz$. Figure 4.16 shows the layout of the filter along with the comparison between MMT and CST data.

Now, the diplexer is formed based on the two presented channel filters. The diplexer is optimized with the MMT, which saves us significant amount of time. The layout of the final optimized diplexer is presented in Figure 4.17(a). The designed diplexer is simulated in CST Microwave Studio and also ANSYS HFSS, and the agreement between the MMT and simulated data validates the presented mode-

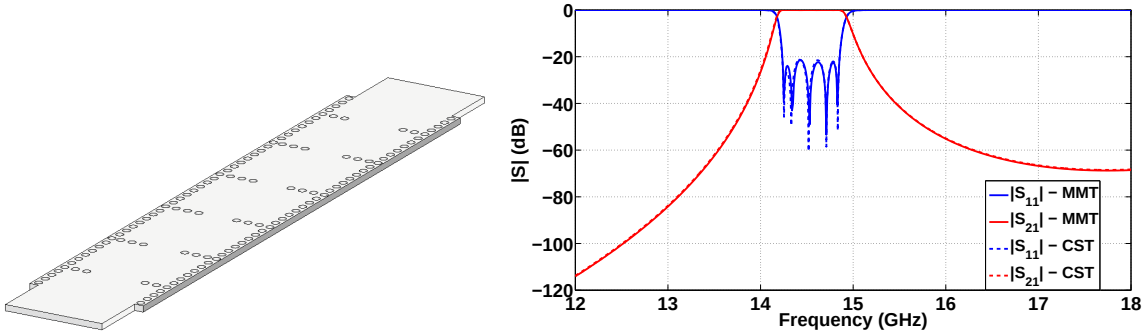


Figure 4.15: SIW filter for the lower channel of the SIW T-junction diplexer. The structure is analyzed with MMT (square vias, solid line), and the results are compared with CST data (circular vias, dashed line).

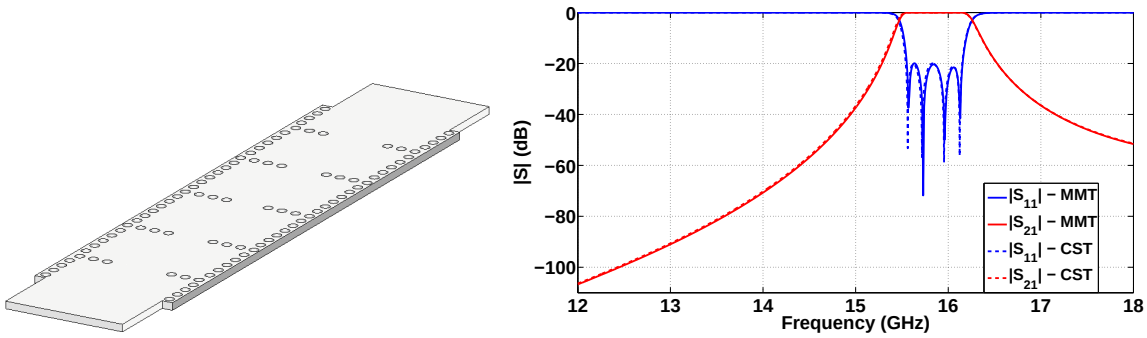


Figure 4.16: SIW filter for the higher channel of the SIW T-junction diplexer. The structure is analyzed with MMT (square vias, solid line), and the results are compared with CST data (circular vias, dashed line).

matching based technique for the analysis of SIW components including a T-junction (Figure 4.17(b)).

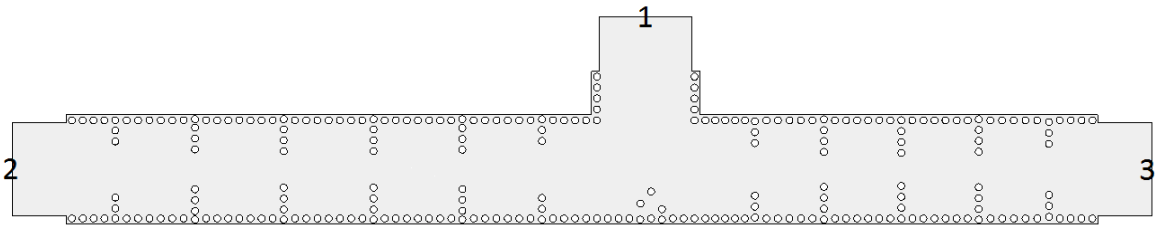
4.2.3 T-junction SIW Diplexer at K-band

The diplexer design starts with the design of the two channel filters. In both channels, five-pole SIW Chebyshev filters are designed with the goal of having $|S_{11}| < -25dB$ in the pass-band. The bandwidths of both filters are $0.5GHz$.

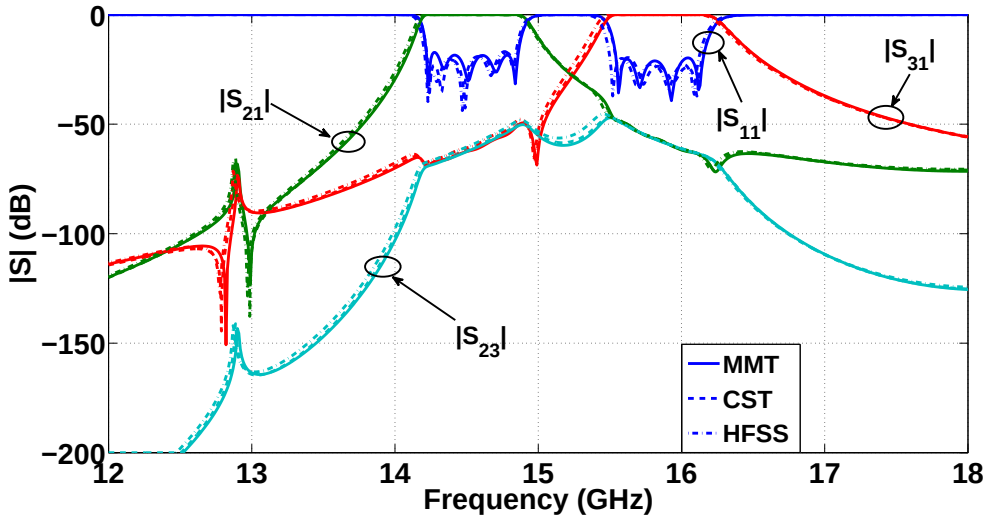
The layout and S-parameters of the channel filter for the lower band are presented in Figure 4.18. This filter has 2.75% bandwidth at $18.15GHz$.

Also, the layout and S-parameters of the channel filter for the higher band are presented in Figure 4.19. This filter is designed for 2.63% bandwidth at $19GHz$. For both filters, the MMT results of the SIW structures with square vias are verified by simulation data for the same structures with circular vias.

After designing two channel filters, the final K-band T-junction diplexer is designed and analyzed. The optimization steps in the design of the SIW T-junction



(a)



(b)

Figure 4.17: Diplexer T-junction layout (a) along with S-parameters (b). The structure in analyzed with MMT (square vias, solid line), and the data is compared with simulated data from CST (circular vias, dashed line) and also HFSS (circular vias, dash-dotted line).

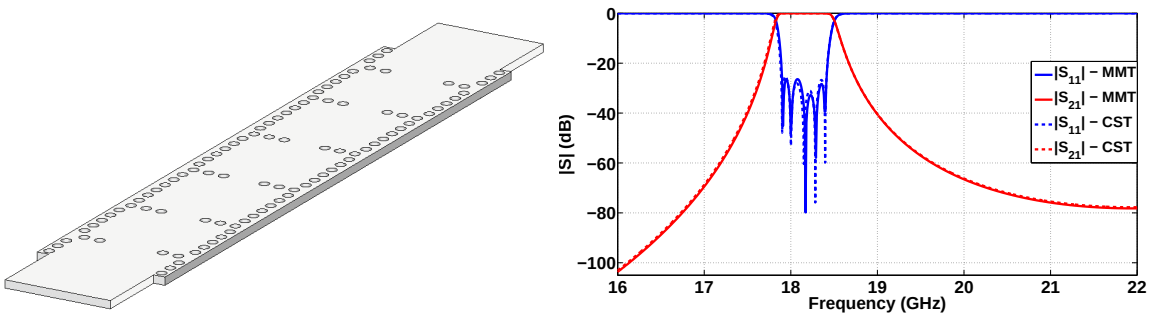


Figure 4.18: Layout and performance comparison between MMT (square vias, solid lines) and CST (circular vias, dashed lines) for the channel filter in the lower band.

diplexer are carried out by employing the MMT approach.

Figure 4.20 depicts the layout and performance of the final diplexer with waveguide ports. The MMT data for the structure with square vias are compared with simulated data obtained from CST, μWave Wizard and HFSS. Excellent agreement is again observed between the MMT results with square vias and simulated responses with circular vias.

Figure 4.21 shows the fabricated prototype of the diplexer along with the S-parameter results from measurements, simulations, and also MMT. Measured in-band insertion losses are $3.88dB$ and $4.28dB$ compared with $2.39dB$ and $2.46dB$, respectively, in the CST simulations. The minimum measured return loss in the two bands is $18.13dB$ and $16.9dB$, respectively, compared to $23.4dB$ and $21.3dB$ in the simulation. Due to fabrication restrictions, the via diameter has been changed to $d = 0.65mm$, which causes the measured data to have a slight frequency shift towards higher frequencies compared to the MMT and simulated data. Otherwise, the measured data confirms the validity of the proposed MMT approach for the analysis and design of SIW components involving T-junctions.

4.2.4 Backward Diplexer

In this section, we present a new design for SIW diplexers in which all three ports are located at the same edge of the substrate thus allowing for a more compact design. In addition, having input/output ports at the same interface is desirable in some applications. Due to the orientation of ports, this component is named backward diplexer.

The diplexer is designed at K-band, with $15dB$ return loss in bandwidths of

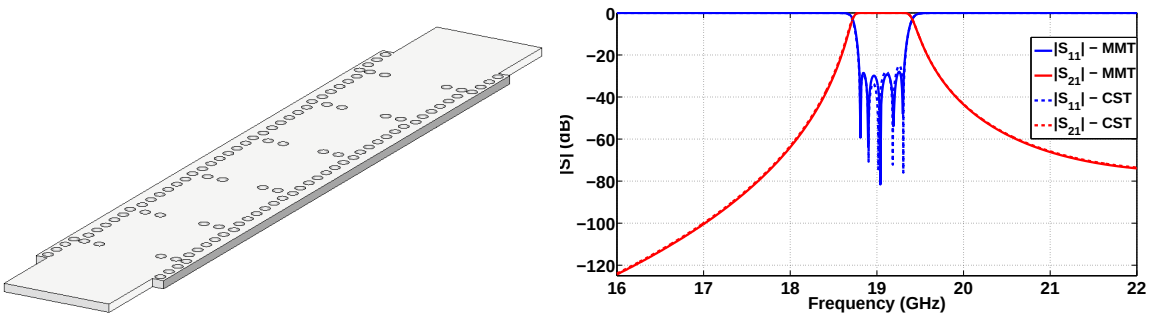


Figure 4.19: Layout and performance comparison between MMT (square vias, solid lines) and CST (circular vias, dashed lines) for the channel filter in the upper band.

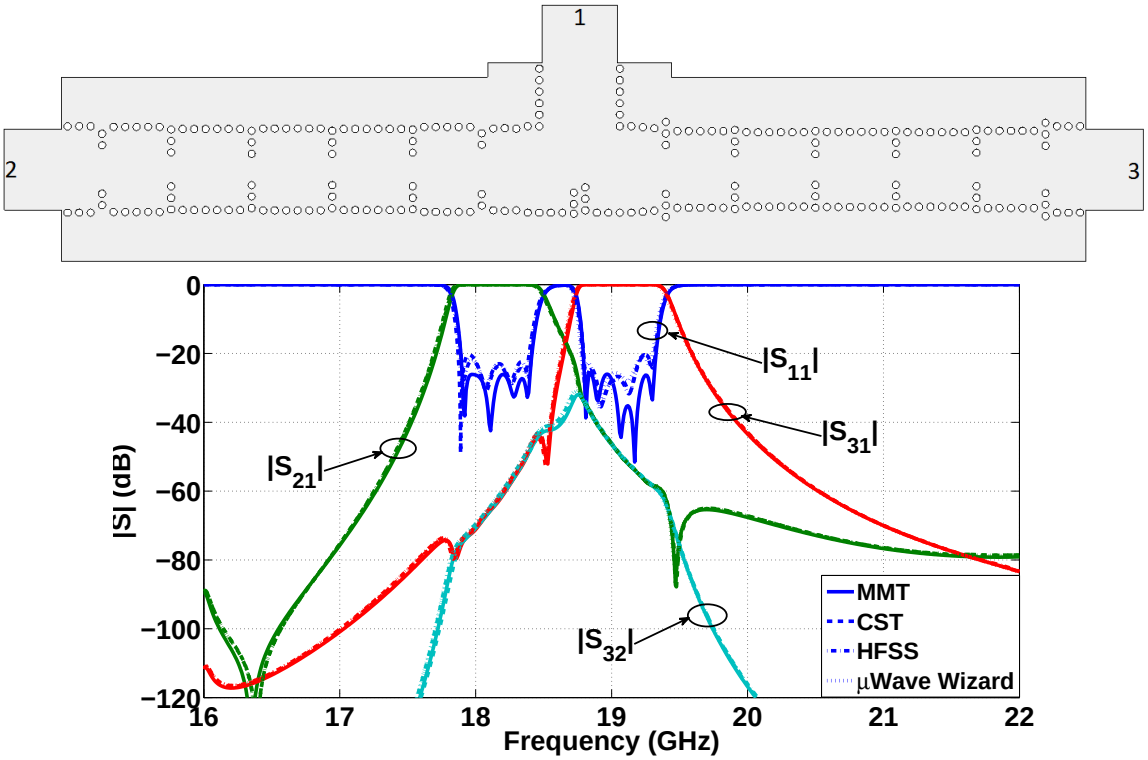


Figure 4.20: Layout of the simulated K-band SIW T-junction diplexer with waveguide ports and performance comparison between MMT (square vias, solid lines), CST (circular vias, dashed lines), μWave Wizard (circular vias, dotted lines) and HFSS (circular vias, dash-dotted lines).

$0.4GHz$ located at $20GHz$ and $21GHz$. The backward diplexer is originally designed in dielectric-filled waveguide technology [97]. The diplexer is then translated to SIW technology using the relation between SIW width and its effective waveguide width Equation 3.6. Optimization steps using the MMT approach (Chapter 2) completes the design.

The design of the diplexer begins with synthesizing the two channel filters in waveguide technology [97]. For this design, the substrate is chosen as RT/duroid 6002 with $\epsilon_r = 2.94$ and height $h = 0.254mm$ with loss factors $tan\delta = 0.0012$ for the dielectric and $\sigma = 5.8 \times 10^7 S/m$ for copper layers and vias. The equivalent waveguide width is set to be $W_{equi} = 5mm$. Two five-pole Chebyshev iris filters with bandwidths of $0.4GHz$ at $20GHz$ and $21GHz$ are designed with the MMT approach [97]. The thicknesses of apertures in the waveguide design are chosen as $l_{iris} = 0.55mm$, which is the same as the side length of the square via in the SIW structure. This results in via diameters of $d = 0.6444mm$ in SIW diplexer (Equation 2.45). Figure 4.22 shows

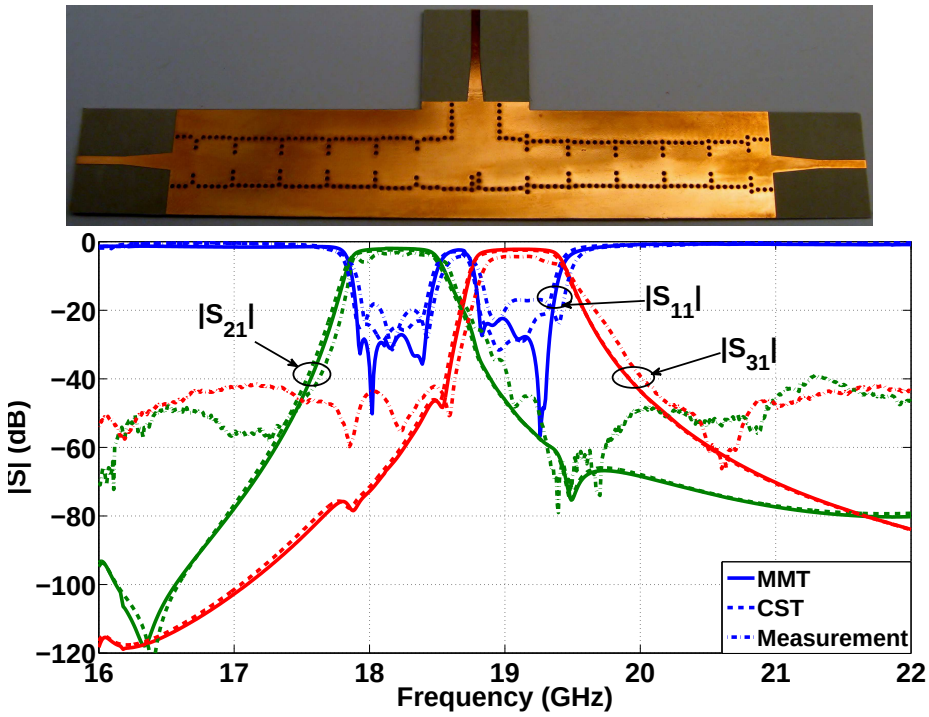


Figure 4.21: Layout of the fabricated K-band SIW T-junction diplexer and performance comparison between MMT (square vias, solid lines), CST (circular vias, dashed lines) and measurements (circular vias, dash-dotted lines).

the performance of the two channel filters where the MMT data is also verified by simulation data obtained from CST Microwave Studio.

The backward waveguide diplexer is then constructed from the channel filters. Optimizing the diplexer using an MMT approach results in a backward waveguide diplexer with return loss better than $25dB$ in each band. The isolation between two channels is better than $50dB$. Note that a via is added at the center of the structure, close to the short circuit at the far end (Figure 4.23(a)), in order to provide a better return loss. The layout and performance of the waveguide diplexer are presented in Figure 4.23(a) and Figure 4.23(b), respectively. In Figure 4.23(a), all structural parameters (in mm) of the all-dielectric waveguide diplexer are presented. Also in Figure 4.23(b), the MMT data is verified by simulations with CST.

The diplexer is then translated to SIW technology using the relation presented in Equation 3.6. The side length of the square vias and via pitch are $l_{square} = 0.55mm$ and $p = 1mm$, respectively. Deploying the MMT approach (Chapter 2), the SIW diplexer with square vias is optimized for the best performance in each band. The square-to-circular conversion relation adopted in Equation 2.45 is deployed to replace

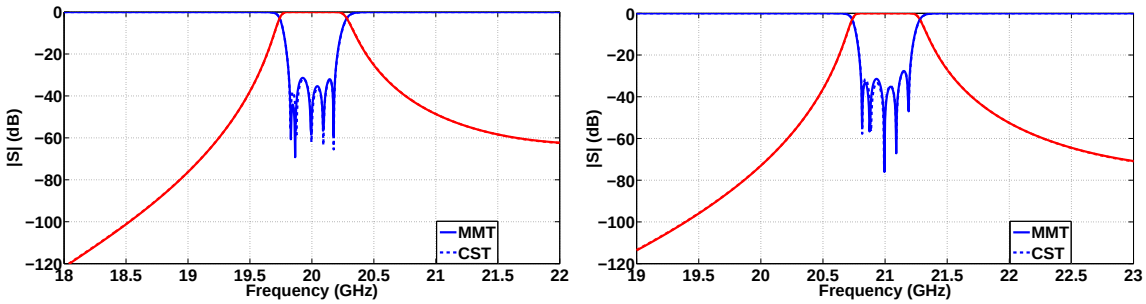
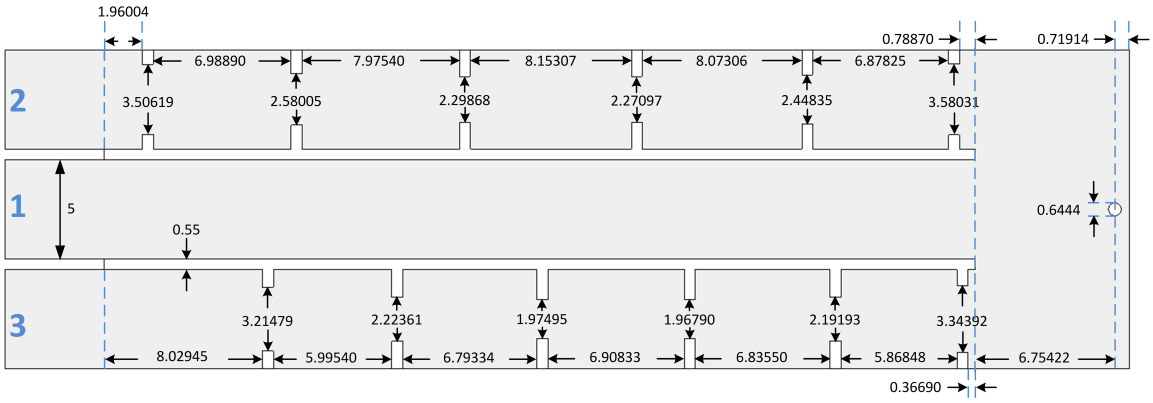


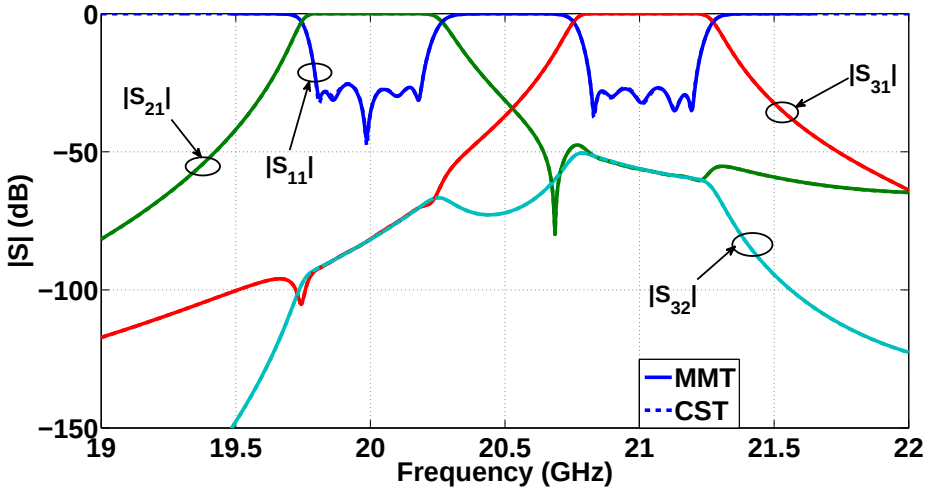
Figure 4.22: (a) Lower and (b) higher channel filters of the backward waveguide diplexer. The filters are designed with the MMT (solid line) approach, and verified in CST (dashed line).

square vias with circular vias with diameter of $d = 0.6444mm$. $15dB$ return loss in each band and isolation better than $53dB$ between the two channels are achieved. The layout and performance of the optimized SIW backward diplexer with circular vias and with waveguide ports are presented in Figure 4.24. In this figure, the MMT data for square vias is compared with the CST data for the diplexer with circular vias. Good agreement is achieved.

It should be noted that for the SIW diplexer, the return loss at each band is better than $15dB$ (for same bandwidths as those in waveguide design), which is inferior to the $25dB$ return loss achieved in the all-dielectric waveguide component of Figure 4.23. One of the main reasons is that in the SIW technology the spacing between vias is restricted by manufacturing limitations. In this case, according to our manufacturer, the separation between vias should be at least $0.2mm$ for a via diameter of $d = 0.65mm$, in order to properly drill the vias. This restriction prevents us from realizing some of the iris widths obtained in the waveguide design, and thus the vias around those irises should be displaced as well (c.f. the adjusted vias around irises in the layout of Figure 4.24). This backward diplexer, due to the presence of a short at the far end, is very susceptible to these structural changes compared to regular types of diplexers (c.f. our other SIW diplexers presented in Section 4.2.1, Section 4.2.2 and Section 4.2.3). As a result, optimizing such a structure is a more cumbersome task. Nevertheless, the designed SIW backward diplexer still outperforms most of the previously designed diplexers reported in the literature in terms of the return loss (e.g., $12dB$ RL in [100], $11dB$ RL in [99], $13dB$ RL in [105] and RL about $9dB$ in [104]).



(a)



(b)

Figure 4.23: (a) Layout of the backward diplexer in dielectric-filled waveguide technology (dimensions in mm), and (b) its performance. The MMT data (solid line) is compared with CST data (dashed line).

The fabricated prototype of the SIW backward diplexer, along with its simulated and measured performances, are presented in Figure 4.25. Please note that the structure with microstrip port has a slightly better in-band RL (RL better than $-16.5dB$) on a slightly narrower bandwidth ($395MHz$) at the first band. The width of the 50Ω microstrip port is $w_m = 0.6442mm$, and the widths and lengths of the tapers after optimization are $1.0019mm$ and $2.3058mm$, respectively. In order to be able to use a test fixture in our measurement for at least one of the ports, two output ports are curved. The parameters of the bent microstrip ports, $R_c = 2w_m$, $\alpha = \pi/2$, are based on the data presented in [106], where R_c is the radius of the bend and α is the curve angle. The position of the microstrip bend is chosen so that the bent ports have

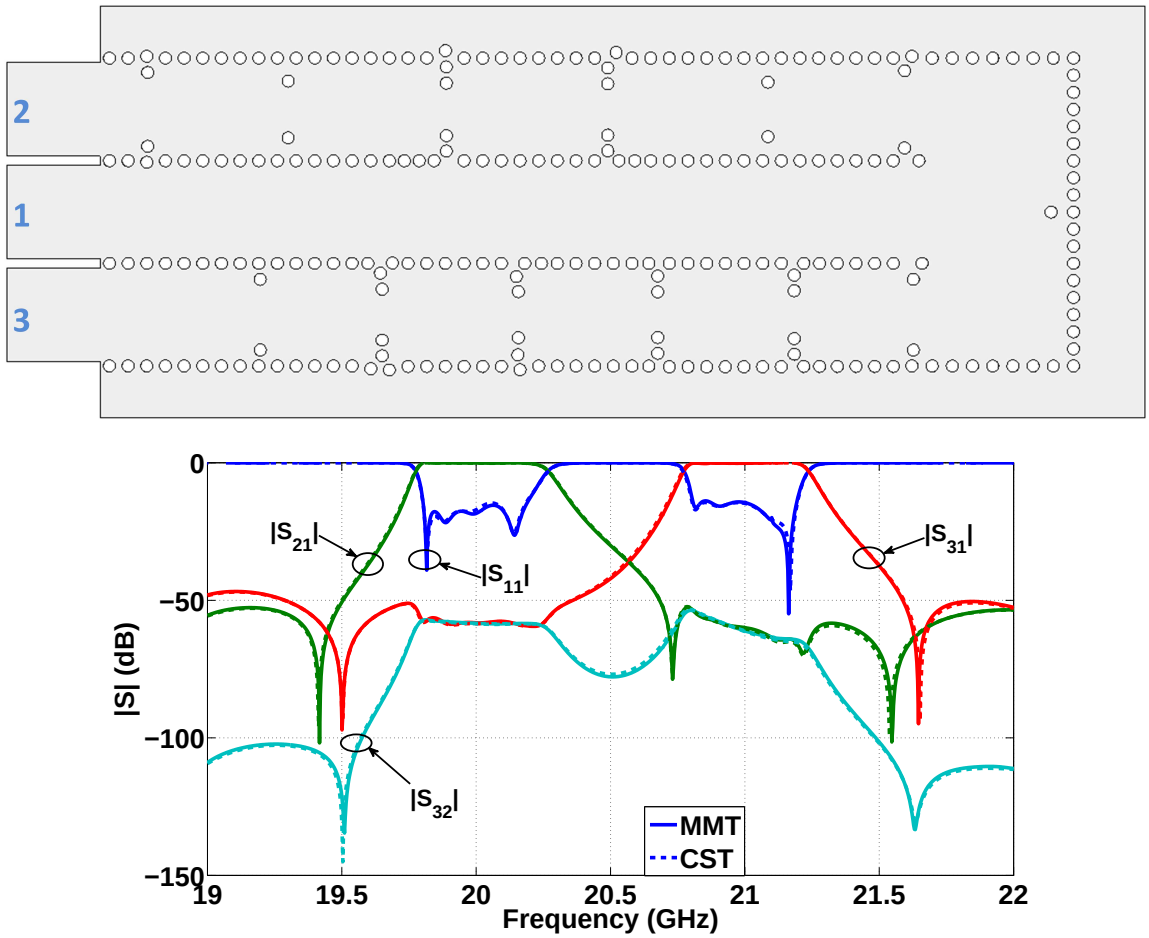


Figure 4.24: Backward SIW diplexer (top) and its performance (bottom). The MMT data for square vias (solid line) has been compared with the CST data for circular vias (dashed line).

same lengths as the input port. The via diameter has changed to $d = 0.65mm$ due to fabrication restrictions. The overall agreement between measured data and MMT and CST data is good. The in-band measured RLs are $14.65dB$ and $13dB$, compared to the simulated RLs of $16.5dB$ and $15dB$. The in-band measured insertion losses are $2.75dB$ and $3.05dB$ compared to simulated $2.53dB$ and $2.76dB$. The measured isolation between two channels is better than $36.7dB$, compared to $38.4dB$ from the simulation.

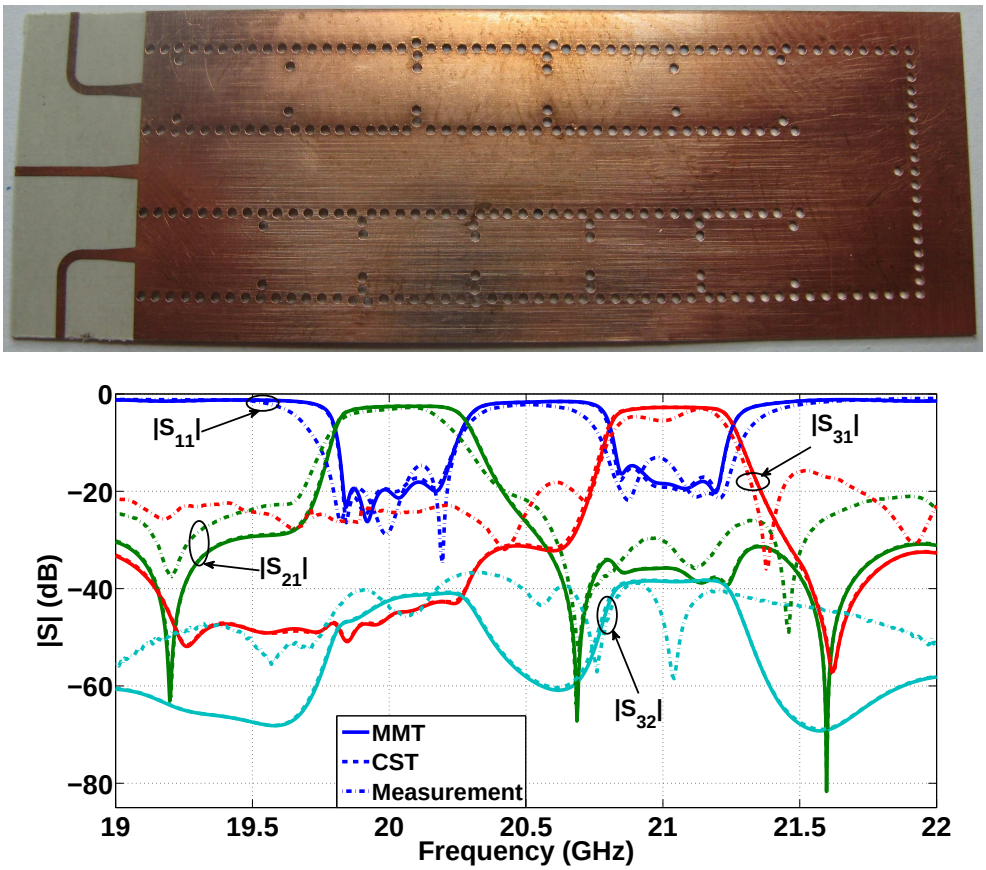


Figure 4.25: Photograph (top) and performance (bottom) of the fabricated prototype. The MMT data for square vias (solid line) is compared with the CST data for circular vias (dashed line) and measured data (dash-dotted line).

4.3 SIW Couplers

The first directional coupler designed based on SIW technology was reported in 2002 [107]. $3dB$ and $10dB$ H-plane SIW couplers in $20-34GHz$ and $28-32GHz$ frequency ranges, respectively, along with $3dB$ and $20dB$ E-plane SIW couplers in $20-39GHz$ frequency range, are the couplers designed by Cassivi *et al.* [107]. Since then, different SIW couplers at different frequency bands have been reported in the literature. In 2005, a $20dB$ SIW coupler in X-band was reported in [108]. $3dB$, $6dB$ and $10dB$ single layer SIW couplers in the $22-28GHz$ frequency range are reported in 2006 [109]. Also in 2006, a 90 degree $3dB$ SIW coupler in the $6-15GHz$ frequency range was reported by Chen *et al.* [110]. Half-mode $3dB$ SIW couplers operating at C-, X-, Ku-, and Ka-bands are presented in [111] in 2007. $3dB$ and $10dB$ E-plane SIW couplers at Ka-band are designed in [112] in 2008. Again in 2008, a FHMSIW $3dB$

coupler operating at X-band is reported in [23]. In 2009, a guideline for designing dual-band E-plane SIW couplers was presented in [113]. Dual-band rat-race couplers based on the composite right/left-handed HMSIW are introduced in [114] in 2010. A hybrid-ring coupler using Electromagnetic Bandgap (EBG) loaded ridge SIW in the $7-9GHz$ frequency range in 2011 [115] is another examples of the different couplers designed based on SIW technology.

In the next section, some SIW couplers designed and analyzed by the MMT will be presented.

4.3.1 Analysis of SIW Couplers by MMT

Some waveguide couplers have been designed [97], translated to SIW technology and analyzed with the MMT technique. The theoretical results of respective SIW couplers are verified with simulations from CST and μWaveWizard and measured results.

The inset of Figure 4.26 shows a $3dB$ K-band H-plane SIW directional coupler with waveguide ports which is designed with the μWaveWizard with circular via holes and analyzed with the MMT (square vias) and simulated with CST Microwave Studio (circular vias). The substrate is chosen as RT/duroid 6002 with $\epsilon_r = 2.94$, substrate height $h = 0.508mm$ and metallization thickness $th = 17.5\mu m$. The diameters of the circular vias are chosen as $d = 0.71mm$ so that the side lengths of the equivalent square vias are $l_{square} = 0.606mm$ according to Equation 2.45. The results of the MMT approach with square vias and CST and μWaveWizard simulations, both with circular vias, are compared in Figure 4.26. Excellent agreement is obtained.

Figure 4.27 shows another $3dB$ K-band H-plane SIW directional coupler with waveguide ports. The substrate is the same as that of the coupler in Figure 4.26. The

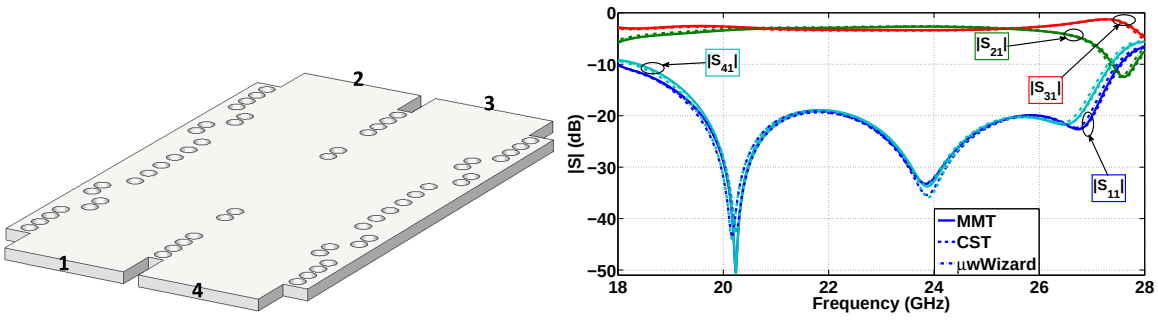


Figure 4.26: Comparison between results obtained with MMT (square via holes, solid lines), CST (circular via holes, dotted lines) and the μWaveWizard (circular via holes, dashed lines) for a $3dB$ K-band SIW coupler.

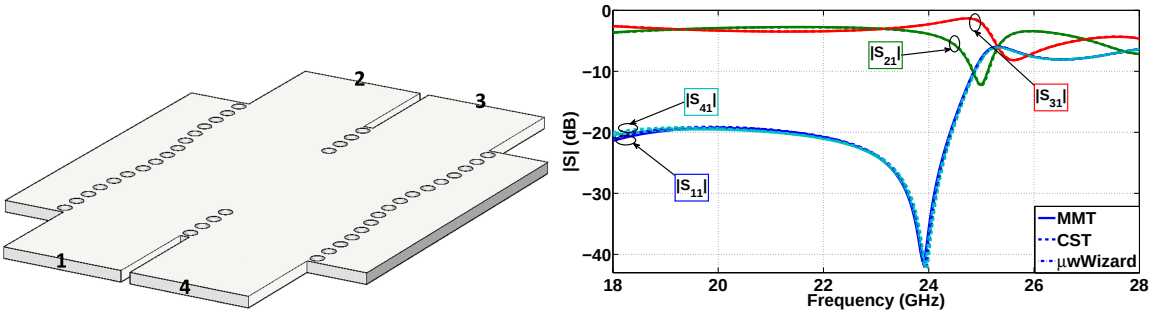


Figure 4.27: Comparison between results obtained with MMT (square via holes, solid lines), CST (circular via holes, dotted lines) and the μWaveWizard (circular via holes, dashed lines) for another $3dB$ K-band SIW coupler.

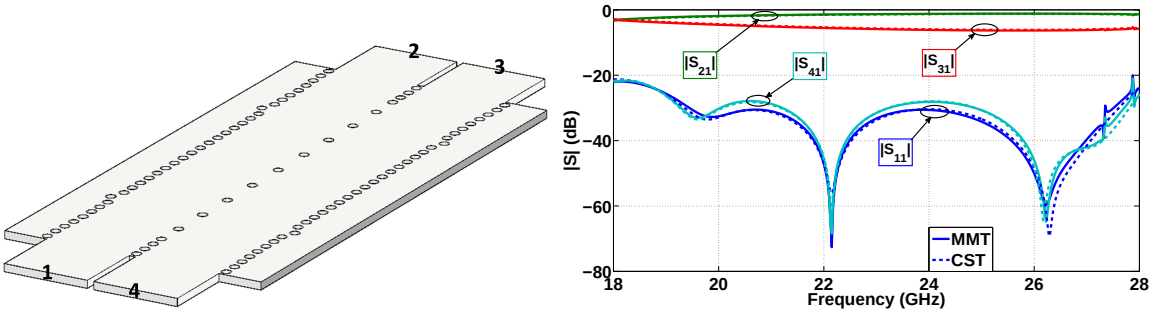


Figure 4.28: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $6dB$ K-band multi-aperture SIW coupler.

diameters of the circular vias are chosen as $d = 0.6444mm$ so that the side lengths of the equivalent square vias are $l_{square} = 0.55mm$ according to Equation 2.45. The results of the MMT approach with square vias and CST and μWaveWizard simulations, both with circular vias, are compared in Figure 4.27. Excellent agreement is obtained.

Figure 4.28 shows the layout (left) and performance (right) of a multi-aperture $6dB$ H-plane coupler in SIW technology on RT/duroid 6002. Due to the SIW width and the relatively large coupling sections, higher-order mode effects come into play beyond $27GHz$. Excellent agreements are again observed between results obtained with the MMT with square via holes and CST with circular via holes.

Figure 4.29 shows the performance of a $20dB$ SIW coupler. The substrate selected for this coupler is RT/duroid 6002 with $\epsilon_r = 2.94$, $tan\delta = 0.0012$, substrate thickness $h = 0.508mm$, metallization thickness $th = 17.5\mu m$, and conductivity $\sigma = 5.8 \times$

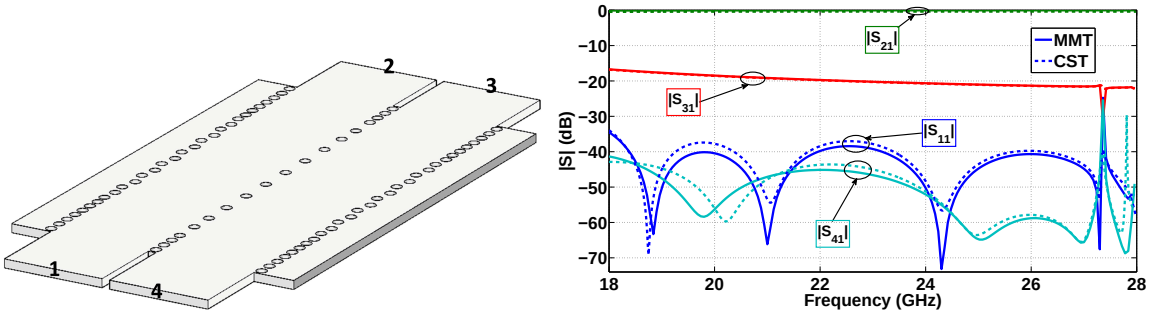


Figure 4.29: Performance of $20dB$ SIW coupler and comparison between MMT (square via holes) and CST (circular via holes).

$10^7 S/m$. For the design of the coupler, the following parameters are used: via-hole diameters and center-to-center spacings are $642\mu m$ and $866\mu m$, respectively. For a cutoff frequency of $14.05GHz$, the equivalent waveguide width is $6.22mm$ and the SIW width $6.714mm$. The initial coupler design is accomplished in an all-dielectric waveguide environment by using well-known design procedures, e.g. [97]. In this step, certain dimensions pertaining to the SIW geometry are already fixed. They include parameters such as wall thickness, aperture width versus waveguide sections in the coupler, etc. This design is translated into an SIW coupler with square via holes which is analyzed and optimized by applying the MMT. After design specifications are met, the square vias are converted to circular ones (Equation 2.45) and designs verified by either CST Microwave Studio or HFSS.

The coupler has return loss and isolation better than $34dB$ between $18GHz$ and $27.3GHz$. Beyond this upper frequency, excitations of higher order modes in the coupler aperture sections limit the operation of the device. This behavior is also known from H-plane waveguide couplers [97]. Narrowing the SIW guides would push the spikes beyond 28 GHz, but at the expense of increasing coupling values between $18GHz$ and $21GHz$. The comparison between the results obtained with the MMT and CST are very good, with CST predicting about $0.35dB$ more loss in the through port ($|S_{21}|$).

For a $3dB$ multi-aperture W-band SIW coupler, the wide bandwidth specification and fabrication restrictions on minimum via dimensions and distances do not allow a straight-forward synthesis using standard coupler theory. Thus such a coupler is realized as a tandem connection of two $8.34dB$ couplers. The substrate is RT/duroid 6002 with a substrate height of $h = 0.254mm$. The diameters of circular vias are chosen as $d_{circular} = 0.2929mm$ so that the side lengths of the equivalent square vias

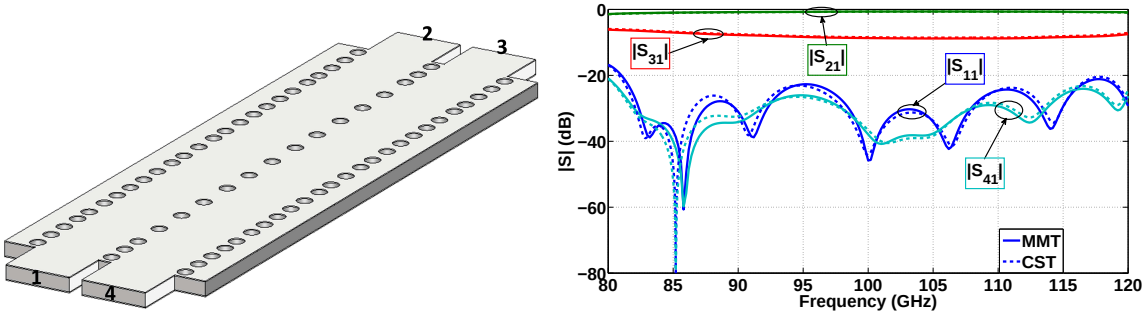


Figure 4.30: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $8.34dB$ W-band 12-aperture SIW coupler.

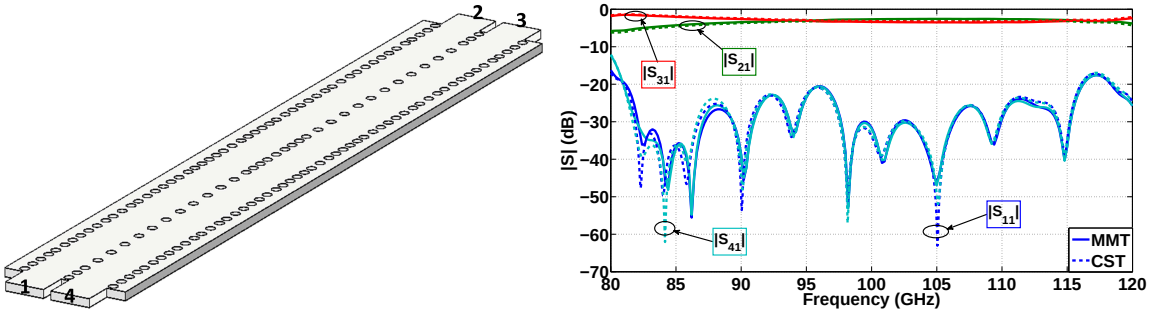


Figure 4.31: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $3dB$ W-band 24-aperture SIW coupler.

are $l_{square} = 0.25mm$.

Figure 4.30 shows the layout and performance of the $8.34dB$ coupler with 12 apertures and Figure 4.31 those of the tandem connection with 24 apertures. Excellent agreement is observed.

Figure 4.32 compares the MMT results with measurements of a Ka-band $3dB$ H-plane SIW coupler with microstrip ports as presented in [107]. While the agreement is not as good as compared to previous results, the agreement between measurements with circular via holes and MMT computations with square via holes is deemed acceptable in many technical applications and thus verifies the MMT analysis procedure using square via holes.

A comparison for a $3dB$ coupler with microstrip ports is presented in Figure 4.33. The measured data in [110] is obtained with microstrip-to-coaxial end launchers which are not included in the simulations. Nevertheless, the agreement between experimental and simulated results is quite good with simulations and measurements showing

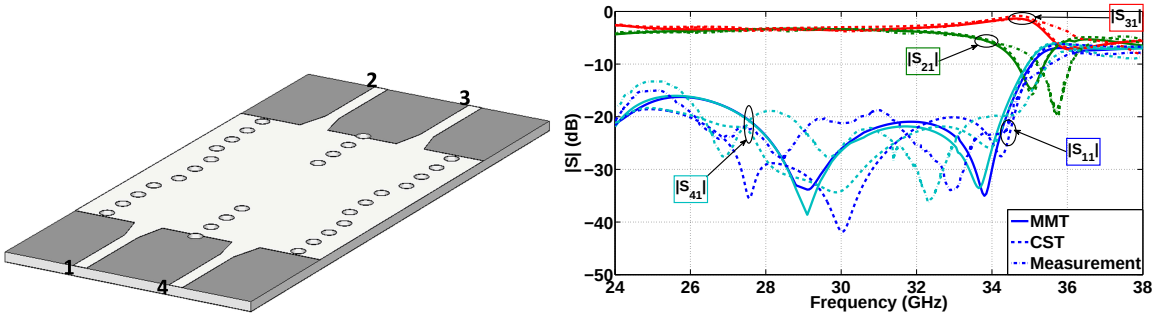


Figure 4.32: Layout and performance comparison between results obtained with MMT (square via holes, solid lines), CST (circular via holes, dashed lines), and measurements (circular via holes, dash-dotted lines) for a $3dB$ Ka-band SIW coupler according to [107].

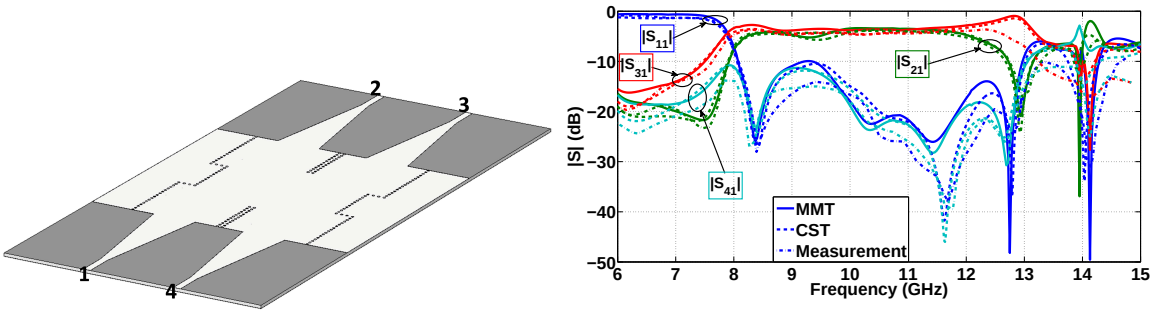


Figure 4.33: Performance comparison between results obtained with MMT (square via holes, solid lines), CST (circular via holes, dashed lines) and measurements (circular via holes, dash-dotted lines) for a $3dB$ Ka-band SIW coupler according to [110].

input return loss and isolation values better than $10dB$ between $8GHz$ and $12.5GHz$. The differences between MMT (square vias) and CST (circular vias) results are attributed to the modeling of the SIW-to-microstrip transitions. While CST models the microstrip taper as seen in Figure 4.33, the MMT code uses a staircase approximation of ten steps in this case.

4.4 SIW Power Dividers

Power dividers designed based on SIW technology have first been reported in [16]. Y- and T-junction SIW power dividers integrated with microstrip ports are proposed in [116]. A multi-way broadband SIW power divider [117], broadband and compact half-mode SIW (HMSIW) Wilkinson power divider [118], [119], wideband SIW power splitter with high isolation [120] and folded E-plane SIW power divider [121], are

other examples of SIW power dividers proposed within the past few years.

With the MMT analysis framework in place, the design of a power divider proceeds as follows. First, the frequency range determines the width of the all-dielectric waveguides ports. The power divider in question is then designed and optimized in all-dielectric waveguide technology using MMT procedures and well-known waveguide design guidelines, e.g., [97]. In this step, the wall thickness between ports or between adjacent waveguides is already confirming to the via hole dimensions of the later-to-be-realized SIW component.

SIW or H-plane waveguide power dividers can be designed according to two basic principles. First, a waveguide N-furcation divides the input power into N output waveguides. However, the N-furcation usually represents a significant discontinuity which can be compensated only over a limited bandwidth. Therefore, power dividers based on waveguide bifurcation are not, under normal circumstances, capable of operating over an entire waveguide band. The second divider type employs waveguide coupler principles where an incoming guide couples to two or more adjacent guides. If the number of coupling sections is large enough, and this is certainly possible in SIW technology, then the bandwidth of such a power divider is much larger than that of an N-furcated divider and can cover an entire waveguide band.

Once the waveguide power dividers performance is found to conform to specifications, the individual waveguide sections are translated to SIW circuits with square via holes by considering the equivalent width of the SIW, e.g., Equation 3.6.

The so-obtained SIW power divider is analyzed and fine-optimized with the MMT algorithm. With the positions and locations of all via holes known, the final step consists in translating the square via holes into circular ones which are more amenable to standard printed-circuit fabrication techniques (Equation 2.45).

4.4.1 Analysis of SIW Power Dividers by MMT

Five K-band power dividers with waveguide ports have been designed and analyzed using the MMT procedure with square via holes. The final configurations are then recomputed with CST Microwave Studio employing circular via holes. The substrate is chosen as RT/duroid 6002 with $\epsilon_r = 2.94$, substrate height $h = 0.508mm$ and metallization thickness $th = 17.5m$. The diameters of the circular vias are chosen as $d_{circular} = 0.644mm$ so that the side lengths of the equivalent square vias are $l_{square} = 0.55mm$ according to Equation 2.45. The ports are set for a cutoff frequency

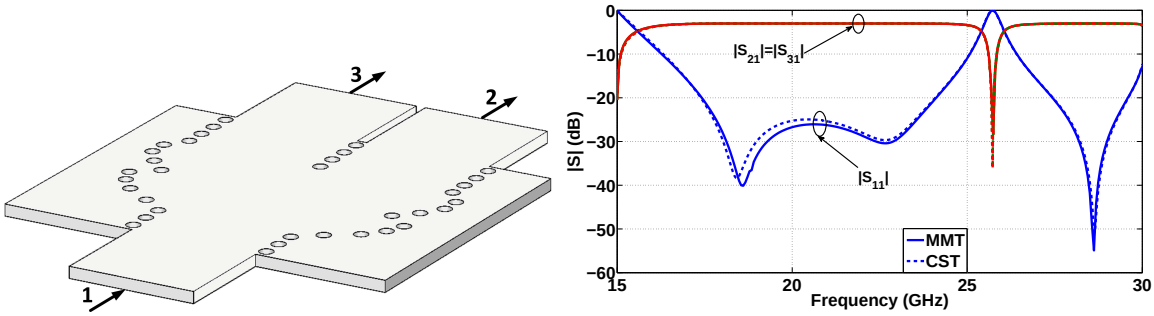


Figure 4.34: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $3dB$ K-band SIW bifurcation power divider.

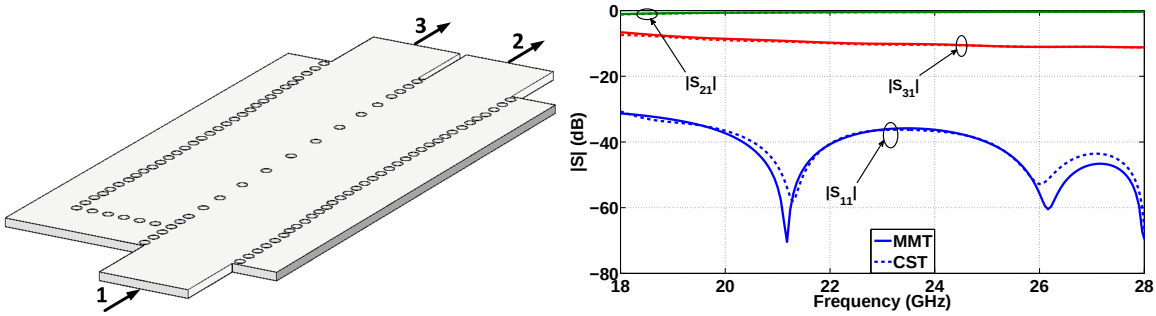


Figure 4.35: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $10dB$ K-band SIW power divider based on 10 coupling sections.

of $15GHz$ with a normal operating band between $18GHz$ and $28GHz$.

Figure 4.34 shows a $3dB$ H-plane SIW bifurcation power divider with all-dielectric waveguide ports. First of all, excellent agreement is observed between results obtained with the MMT using square via holes and CST with circular via holes. Secondly, this being a divider based on SIW bifurcation, the $15dB$ return loss bandwidth covers a frequency range between $17GHz$ and $24.6GHz$. Thus the fractional bandwidth is 36.5%.

Figure 4.35 depicts the layout and performance of an asymmetric K-band SIW power divider which is designed for $10dB$ power division using H-plane coupler principles. Due to ten coupling sections, the return loss of this divider is below $30dB$ over the entire $18-28GHz$ range (43.5%). As is typical for H-plane waveguide couplers, e.g. [97], the signal to the coupled port varies between $-6.6dB$ at $18GHz$ and $-11.2dB$ at $28GHz$. Excellent agreement is again observed between the MMT results with square via holes and the ones from CST with circular vias.

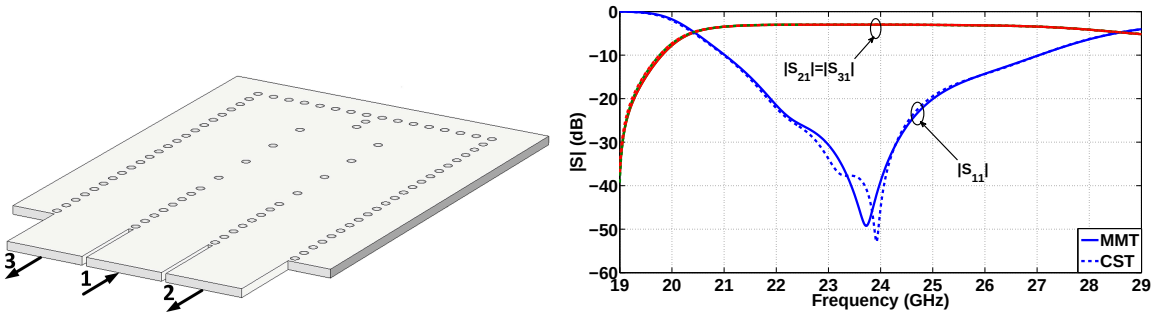


Figure 4.36: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a $3dB$ K-band backward-coupled SIW power divider.

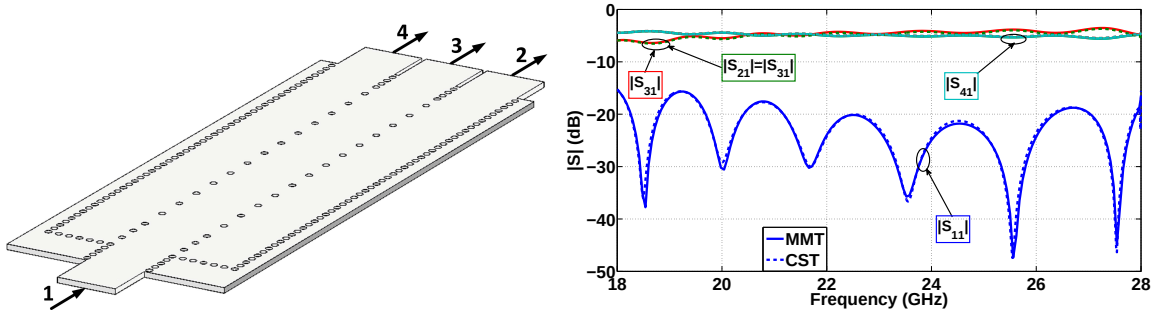


Figure 4.37: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a 3-way ($4.77dB$) K-band SIW power divider based on 17 coupling sections.

In some applications, input and output ports of a power divider have to be accessible at the same interface. Such a so-called backward-coupled divider in SIW technology is presented in Figure 4.36. However, since the backward coupling is achieved by placing a short at the far end of the divider, it is more susceptible to frequency changes. Thus the $15dB$ return loss bandwidth is only 18.2% ($21.5 - 25.8GHz$). Note again the excellent agreement between results with the MMT and CST. As in previous comparisons, differences are observed only below the $-20dB$ value.

The coupled guide principle is now applied to a 3-way ($4.77dB$) SIW power divider as shown in Figure 4.37. The return loss is better than $15dB$ over the entire $18 - 28GHz$ range (43.5%), but the coupling varies slightly between the through port (port 3) and the coupled ports (ports 2 and 4) as expected from typical H-plane waveguide couplers.

The individual dividers presented above can now be combined to, for example, create an entire antenna array feed network in SIW technology. However, as more of

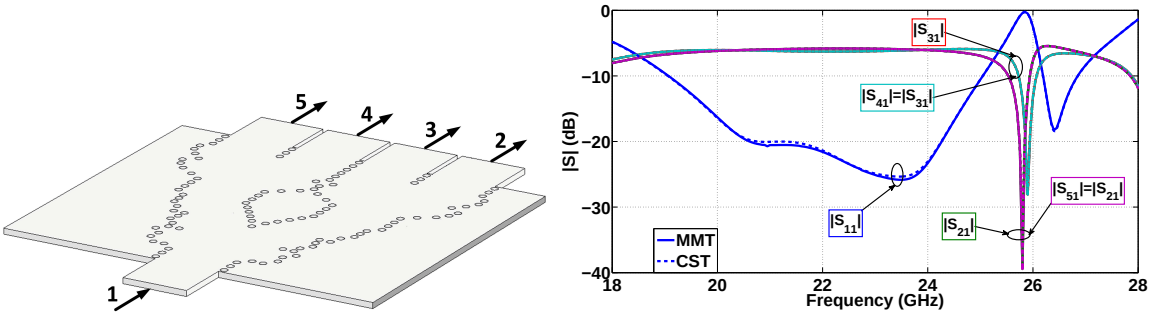


Figure 4.38: Layout and performance comparison between results obtained with MMT (square via holes, solid lines) and CST (circular via holes, dashed lines) for a 4-way ($6dB$) K-band SIW bifurcation power divider.

them are combined, especially those based on the bifurcation principle, the bandwidth will be reduced due to the limited bandwidths of the individual dividers. This is demonstrated in Figure 4.38 for a 4-way ($6dB$) divider based on three individual 2-way bifurcation dividers. The return loss is $15dB$ between $19.8GHz$ and $24.6GHz$ (21.6%) which is a 14.9% bandwidth reduction compared to the individual SIW 2-way divider presented in Figure 4.34. Again note the excellent agreement between the MMT and CST for this power divider with a rather complex arrangement and locations of via holes.

For an application in a receiver module, the isolated port of a coupler, like the one presented in Figure 4.29, should ideally be matched. However, producing a match in SIW is not straightforward and would require fabrication steps in addition to the simple PCB process to fabricate the coupler, that is used in adaptive receiver systems and should be connected to a planar antenna like the antipodal tapered slot antenna (ATSA). Therefore, it is more appropriate in SIW to short the isolated port, which results to a power divider. The layout and performance of such a power divider is shown in Figure 4.39. Very good agreement between the MMT and CST is observed, thus validating the design. In comparison with Figure 4.29, it is obvious that the short reduces the level of spikes at around $27.3GHz$. However, it comes with the price of a poor match at the coupled port. This is of no concern as long as it can be accommodated by for example an Automatic Gain Control (AGC) circuit that is connected to that port. For comparison, the individual $3dB$ power dividers in SIW technology as used in, e.g., [122] have an output return loss in the order of $6dB$ and operate well in a feed network for eight ATSAs.

Figure 4.40 compares the MMT results with measurements of a Ka-band $3dB$ H-

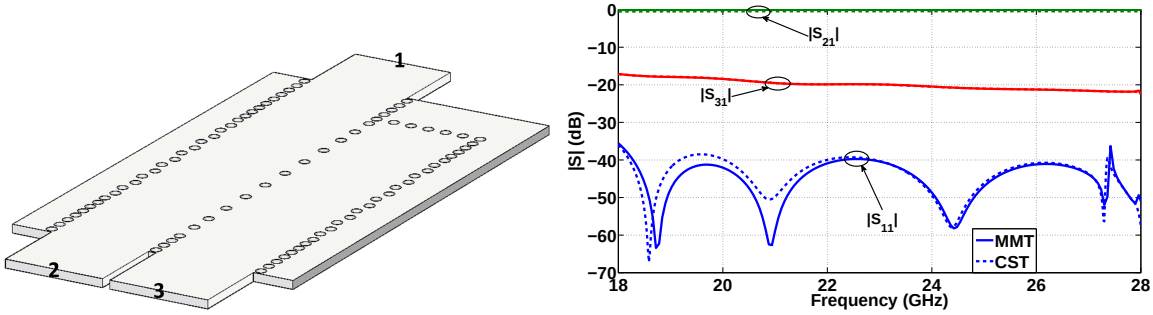
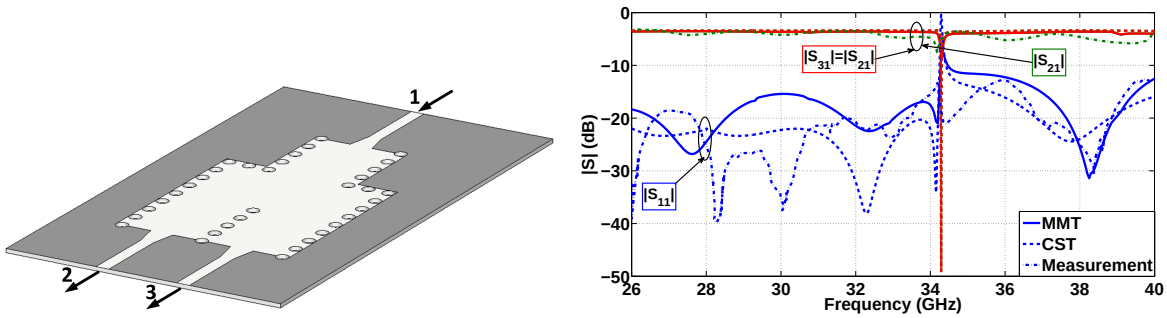
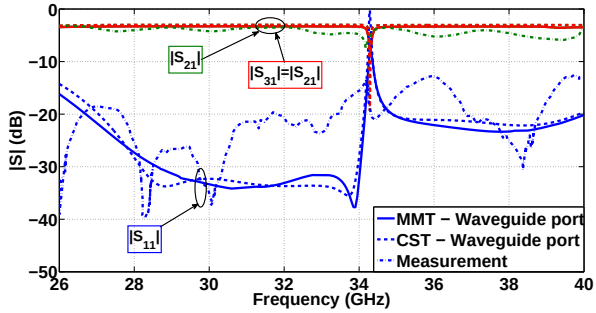


Figure 4.39: Performance of a $20dB$ SIW coupler with a short on the isolated port and comparison between MMT (square via holes) and CST (circular via holes).



(a) (b)



(c)

Figure 4.40: Layout and performance comparison between results obtained with MMT, CST and measurements according to [116] for a $3dB$ SIW bifurcation divider; (a) layout of the structure, (b) microstrip ports in MMT and CST, and (c) waveguide ports in MMT and CST.

plane SIW power divider with microstrip ports as presented in [116]. This divider was built on RT/duroid 5880 substrate with with $\epsilon_r = 2.2$, substrate height $h = 0.254mm$ and metallization thickness $th = 17.5\mu m$. The agreement between measurements and both MMT and CST is acceptable but not as good as compared to previous results.

This is due to the following reasons. First, reflection and transmission measure-

ments in [116] were carried out in a two-port set-up where the third microstrip port was covered with absorbing material. This can introduce some reflection which will propagate back to the input (port one) and the other output port (port 2). Secondly, the differences between MMT and CST are due to the staircase approximation of the microstrip tapers in the MMT algorithm Section 2.4.5. This is demonstrated in Figure 4.40(c) where the same divider is analyzed with waveguide ports. It is observed that the agreement between MMT and CST is significantly improved compared to Figure 4.40(b). The remaining small differences between MMT and CST in Figure 4.40(c) are due to the different modeling of the vias at the input and output ports. They cover the top metallization (Figure 4.40(a)) only partly and extend into the substrate. In MMT, they were modeled as half-square (rectangular) vias.

Chapter 5

Conclusion and Future Work

The advent of SIW technology in the early 2000 attracted a lot of research in the areas of analyzing and designing new compact size, low-loss and integrable microwave and millimeter-wave components based on this technology. However, further investigations are still required for SIW to be fully adopted by microwave engineers in industry. In this thesis, we present an efficient method for analyzing H-plane SIW structures. In addition, a new formula for calculation of the effective waveguide width of the SIW, a new wide-band microstrip-to-SIW transition, and some passive SIW components are presented.

5.1 Analysis of SIW

In most SIW structures, there is no structural variation in the direction of the E-field of the dominant mode (TE_{10}), and top and bottom metal sheets are intact. In this case, we are dealing with a 2D electromagnetic problem. This type of components, i.e., H-plane SIW structures, are analyzed in this thesis. As there is only the TE_{m0} set of modes in these structures (cf. Section 2.3.2), modal analysis techniques are proper choices for the analysis of H-plane SIW structures. A modal analysis approach, an MMT method, is presented in Chapter 2 for the analysis of H-plane SIW components with square vias. The presented method is capable of analyzing SIW circuitry with different via positioning and different excitation methods. As SIW components with circular vias are more common in industry, an equivalence between square via and circular via is adopted in Section 2.7. The MMT approach with the presented equivalence proved to be an effective and accurate method for the analysis of different

types of H-plane SIW circuitry with circular vias, e.g., filters, diplexers, couplers and dividers, and good agreement between MMT and simulation data, and in some cases measurement data, validates the analytical approach (cf. presented components in Chapter 4).

Having a reliable and fast analytical tool is crucial in the design of SIW devices. Considering the complexity of SIW structures and numerous amount of vias in them, which leads to a large number of optimization parameters, optimizing SIW components with commercially available field solvers is a tedious and cumbersome task. The presented MMT approach is 10 times faster than commercially available field solvers like CST Microwave Studio. Therefore, such a fast analytical approach permits the SIW components design in a timely fashion.

The presented MMT based method can be enhanced further to analyze 3D SIW structures. By taking into account other sets of TE and TM modes in E-plane aperture-coupled SIWs, a 3D SIW structure with any configuration can be analyzed.

5.2 Effective Waveguide Width of SIW

The effective waveguide width of the SIW is one of the fundamental design parameters. As the field patterns inside the SIW are similar to those of rectangular waveguides (cf. Figure 1.3), the design of any SIW structure starts with specifying the waveguide width for the desired frequency band and substrate material. A new relation between SIW width (a_{SIW}) and its equivalent waveguide width (W_{equi}) is presented in Section 3.1. An MMT approach is deployed to extract the formula (cf. Equation 3.6). Note that due to the normalization, the formula is independent of the relative permittivity of the substrate and frequency. The proposed formula allows the design engineer to directly obtain the optimum SIW width without solving complicated formulas presented in the literature. The proposed relation is based on the minimizing $|S_{11}|$ for the discontinuity between an all dielectric waveguide port with width W_{equi} and the SIW with width a_{SIW}.

Compared with previously proposed relations in the literature, the presented relation in this thesis proved to provide the best return loss, and thus the most accurate equivalence between a_{SIW} and its W_{equi} for different dielectrics, microwave frequency bands and all applicable ranges of d/p ratios.

Moreover, it is demonstrated that further optimization of the SIW width with different commercially available software does not improve the excellent performance

obtained with the new formula.

5.3 Transitions to SIW

In order to provide means for the excitation and measurement of SIW devices, and also integration of these components with other planar topologies, transitions between planar circuitry and SIW are required. More importantly, low-reflection transitions to microstrip are required to integrate and combine SIW circuits with active components such as amplifiers. In such applications, it is vital to provide low-reflection transitions so that the component design is independent of the influences of the transitions.

We present a new wide-band transition from microstrip to SIW in Section 3.2. It featured two vias, which have the same diameter as the SIW vias and are placed symmetrically at both sides of the microstrip taper. The presented transition shows return loss values better than $30dB$ over entire waveguide frequency bands, from X- to E-band. This is the lowest return loss achieved over wide frequency bands compared to previously proposed microstrip-to-SIW transitions. The performance of the transition is presented in the waveguide frequency bands ranging from $8.2GHz$ to $90GHz$. The formula introduced for the design of wide-band and low-reflection transitions (cf. Equation 3.9) is demonstrated to provide simplicity as well as robustness. The measured return loss for the back-to-back taper-via transition in Ku-band is better than $26.05dB$, which is the lowest measured return loss available over a full waveguide band.

Investigating such a wide-band transition with low return loss for interconnecting other planar topologies like CPW to SIW is a potential point of interest.

5.4 SIW Components Design

The design and analysis of some passive H-plane SIW components such as filters, diplexers, couplers, and power dividers are presented in Chapter 4. The SIW components with circular vias are analyzed and designed with the MMT approach presented in Chapter 2 along with the square-to-circular via equivalence (Equation 2.45). SIW structures are usually designed first in waveguide technology. The dimensions of the square via holes, as derived from Equation 2.45 for a given via diameter, can be incorporated from the onset in the all-dielectric waveguide design as, e.g., post thickness, aperture thickness, etc. Such an all-dielectric waveguide prototype is then translated

to an SIW structure with square via holes. Fine optimization with square vias using the MMT approach completes the design. Then square vias are replaced with the proper circular ones (Equation 2.45). Comparison of the MMT data with simulation and in some cases measurement data for the designed passive structures validates the MMT approach.

Beside the numerous research that has been conducted in order to design new microwave components based on SIW technology, this is still an ongoing trend. Possible extensions to this work are H-plane SIW cross junctions for multiplexer applications and, as mentioned before, E-plane aperture-coupled SIW circuits to vertically stack and connect a variety of planar SIW components. Also, investigating some guidelines for the synthesis of H-plane components directly in SIW technology, instead of designing them in waveguide circuitry first and then translating into SIW technology, is another potential point of interest.

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