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Electronic and Spintronic Transport in Germanium Nanostructures

by

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Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May 2014

Dedication

To my family.

Acknowledgements

I would like to express my sincere gratitude to my advisor, Prof. Emanuel Tutuc. His knowledge and guidance have been instrumental in carrying out the experiments and overcoming the difficulties along the road. His devotion and persistence in research exemplify the qualities of a true scientist, and encourage me to follow along. I would also like to thank my dissertation committee: Prof. Sanjay K. Banerjee, Prof. Jack C. Lee, Prof. Ananth Dodabalapur, Prof. Leonard F. Register, and Prof. Allan MacDonald, for their guidance throughout this project.

The path to this degree is paved with difficulties, problems, and failures. I am most grateful that my friends have always been there for me. I would like to thank my group members: Junghyo Nah, Babak Fallahazad, David Dillen, Kayoung Lee, Kyounghwan Kim, Stefano Larentis, Micah Points, Jiamin Xue, Seyoung Kim, Chris Corbet, and Kamran Varahramyan for their friendship and support. It is especially my privilege to have shared not only a cubical with Babak and Junghyo, but also numerous coffee hours over the ups and downs of life. I also thank the fellow researchers in Microelectronic Research Center who are keen to offer expertise and share friendship: Ping-Chun Li, Chen-Guan Lee, Yen-Ting Chen, Che-Yun Lin, Wei-Cheng Lai, Emmanuel Onyegam, Mustafa Jamil, Michael Ramon, Domingo Ferrer, Hema Movva, Davood Shahrjerdi, Fahmida Ferdousi, Jaehyun Ahn, and Yi Zhou. It is my pleasure to have met and worked with all these bright people.

I would also like to acknowledge the MRC technical and administrative staff. All our research would not have been possible without their hard work and constant, careful maintenance of the facilities.

Lastly, my deepest gratitude goes to my parents, brother, sister, Michelle and O'Neil. Their love and support propel me in every aspect of life. And most important of all, they believe in me even when I doubt myself.

Electronic and Spintronic Transport in Germanium Nanostructures

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The University of Texas at Austin, 2014

Supervisor: Emanuel Tutuc

The digital information processing system has benefited tremendously from the invention and development of complementary metal-oxide-semiconductor (CMOS) integrated circuits. The relentless scaling of the physical dimensions of transistors has been consistently delivering improved overall circuit density and performance every technology generation. However, the continuation of this trend is in question for silicon-based transistors when quantum mechanical tunneling becomes more relevant; further scaling in feature sizes can lead to increased leakage current and power dissipation. Numerous research efforts have been implemented to address these scaling challenges, either by aiming to increase the performance at the *transistor* level or to introduce new functionalities at the *circuit* level. In the first approach, novel materials and device structures are explored to improve the performance of CMOS transistors, including the use of high-mobility materials (e.g. III-V compounds and germanium) as the channel, and multi-gate structures. On the other hand, the overall circuit capability could be increased if other state variables are exploited in the electronic devices, such as the electron spin degree of freedom (e.g. spintronics).

Here we explore the potential of germanium nanowires in both CMOS and beyond-CMOS applications, studying the electronic and spintronic transport in this material system. Germanium is an attractive replacement to silicon as the channel

material in CMOS technology, thanks to its lighter effective electron and hole mass. The nanowire structures, directly synthesized using chemical vapor deposition, provide a natural platform for multi-gate structures in which the electrostatic control of the gate is enhanced. We present the realization and scaling properties of germanium-silicon-germanium core-shell nanowire *n*-type, Ω-gate field-effect transistors (FETs). By studying the channel length dependence of NW FET characteristics, we conclude that the intrinsic channel resistance is the main limiting factor of the drive current of Ge NW *n*-FETs.

Utilizing the electron spins in semiconductor devices can in principle enhance overall circuit performance and functionalities. Electrical injection of spin-polarized electrons into a semiconductor, large spin diffusion length, and an integration friendly platform are desirable ingredients for spin based-devices. Here we demonstrate lateral spin injection and detection in Ge NWs, by using ferromagnetic metal contacts and tunnel barriers for contact resistance engineering. We map out the contact resistance window for which spin transport is observed, manifestly showing the conductivity matching required for spin injection.

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Chapter 1: Introduction

1.1. Scaling and Its Challenges

Recent years have seen the semiconductor technology driven mostly by the advancement in the Si-based, metal-oxide-semiconductor field-effect-transistors (MOSFETs), the building block of modern integrated circuits. The transistor density and performance has largely followed the "Moore's Law" for the past 40 years, in which it is conjectured that the number of transistors per unit area will double approximately every two years (Fig. 1-1) [1]. This trend can also be observed in the evolution of static random memory (SRAM), as shown in Fig. 1-2 [2].

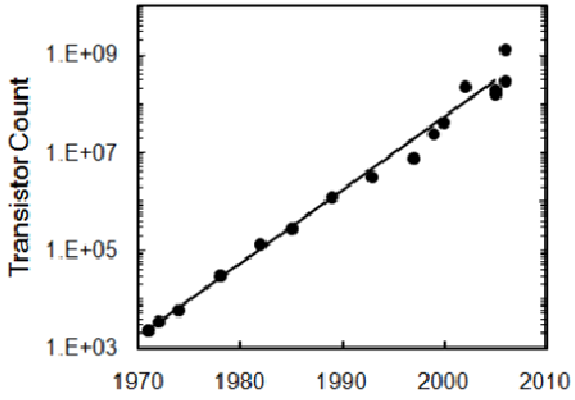


Figure 1-1. Number of transistors on Intel CPU's over the years. (Figure and caption adapted from Ref. [1])

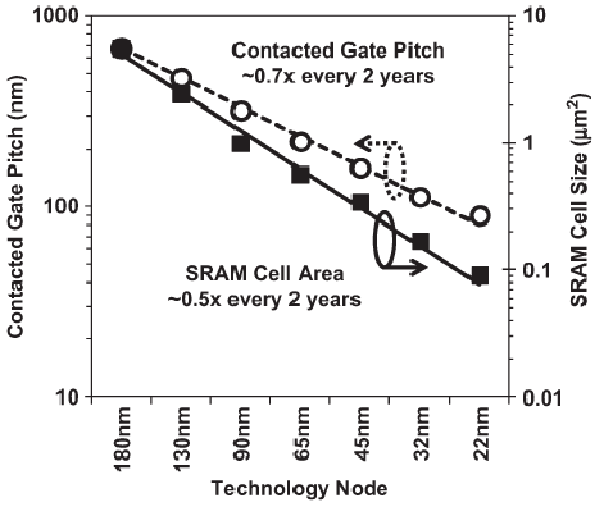


Figure 1-2. The key dimensional scaling is consistently achieved in every generation of SRAM. (Figure and caption adapted from Ref. [2])

At first, continuous performance gain, as well as improvements in power consumption and production cost, can be achieved by simply scaling down the physical dimensions of transistors, without modifying channel materials or structures. The proposed scaling guidelines aim to maintain a constant electric field in the channel by scaling various device parameters simultaneously with a factor κ, such as the channel length (L), drain voltage (V), and oxide thickness (t_{ox}) [3], as shown in Fig. 1-3. The results of this practice include an increase in operating speed and packing density, and a decrease in power consumption as the technology node progresses [4].

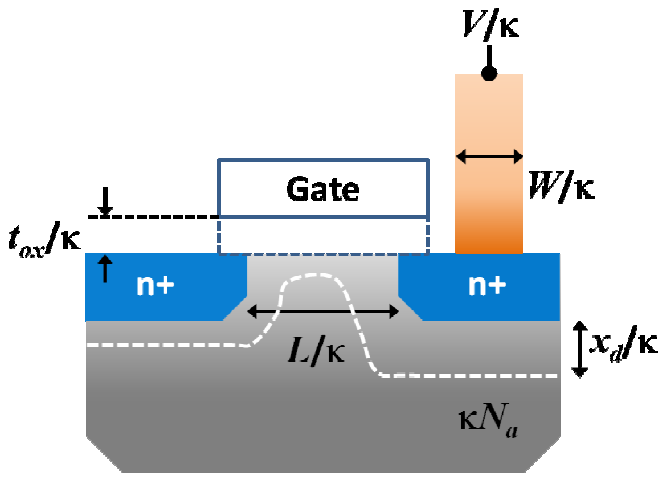


Figure 1-3. Illustration of a MOSFET with key parameters under constant-field scaling rules [3].

However, in the early 2000s, the thickness of the gate oxide (e.g. SiON) couldn't be further reduced without drawing too much gate leakage current; device performance can no longer be improved by merely decreasing its geometrical parameters [1]. Since then, various performance "boosters" have been introduced into the fabrication processes in order to further improve the performance of MOS devices, as an example shown in Fig. 1-4. Strained channel was first implemented in the 90 nm technology node [5], followed by the use of high-κ/metal-gate in the 45 nm node [6] and finally the tri-gate geometry in the 22 nm node [7].

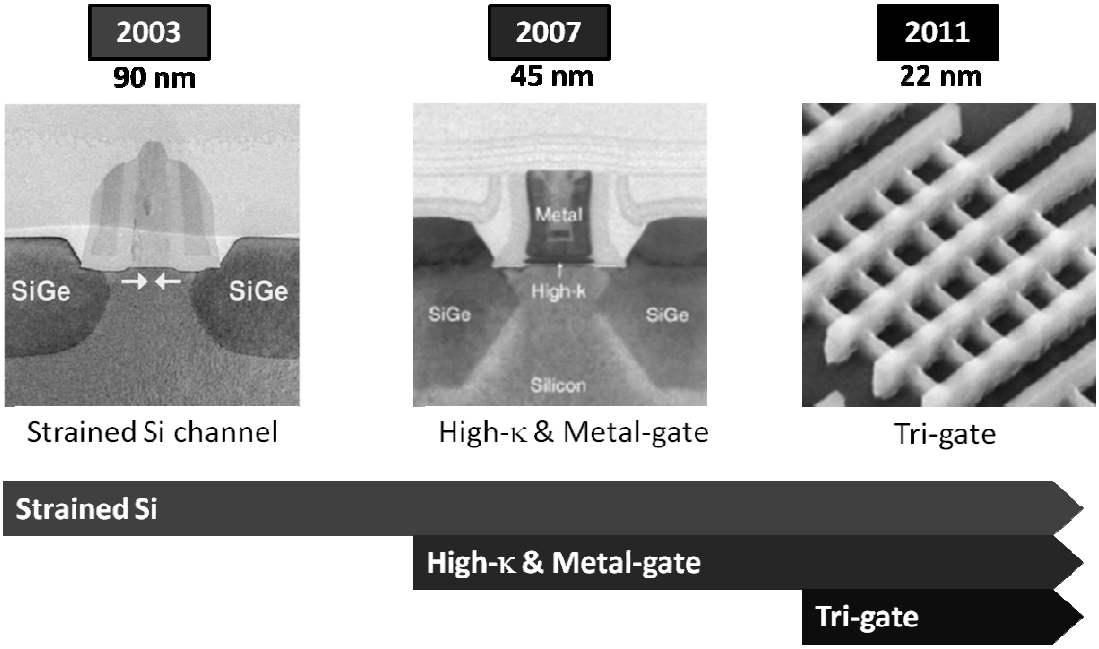


Figure 1-4. The evolution of transistors on Intel CPU's. New materials and device architectures are introduced along with the scaling of transistors. (Figure adapted Ref. [1], [8])

The performance enhancement due to each process innovation can be seen in Fig. 1-5, which shows the ON-current of a typical *p*-MOS in each generations and the corresponding contributions from each technology innovations [9]. However, the scaling trend is challenged by both physical and technological limitations. For example, in already aggressively scaled devices, further reduction in the gate pitch will result in a decrease in the stress level induced by the overlayer films, which translates into lower carrier mobility and drive current [9]. Traditional scaling also calls for a reduction in source/drain (S/D) footprint, which may limit the contact area for S/D metals, resulting in larger contact resistance and lower drive current. Among these "nonscaling" factors [4], the loss of control of gate over the channel is the most critical. As the channel length decreases, the depletion region from the drain extends into the channel, affecting the channel electrostatics. This is termed as the short-channel effect (SCE), and typical

expressions include threshold voltage shift with drain bias and higher OFF-state current, etc. [10]. As the technology node approaches 7 nm and beyond [11], and with the demand for high performance, low power devices surging, it is questionable whether the transistor performance can continue the scaling trend in Si-based technology. In the sections below, we discuss possible options that may keep improving the performance and functionalities of integrated circuits, including using germanium as the channel material, adopting multi-gate structure, and a paradigm shift into electronic devices that utilize the spin degree of freedom.

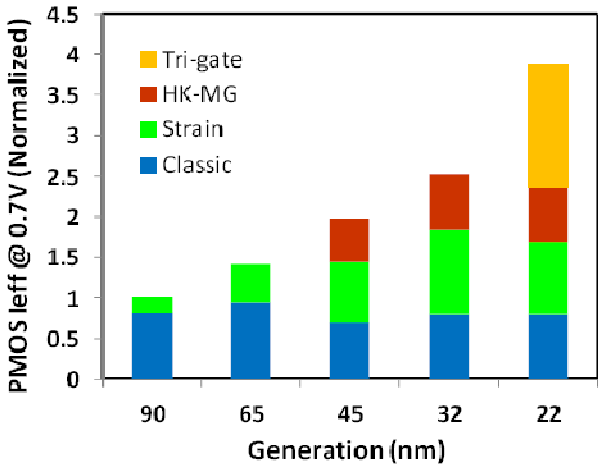


Figure 1-5. The drive current of a typical *p*-MOS in different technology nodes. The contribution due to various process innovations are labeled. (Figure adapted from Ref. [12])

1.2. GERMANIUM AS CHANNEL MATERIAL

In a MOSFET, the drain current (I_D) is proportional to the product of the inversion charge density (Q_{inv}) and carrier mobility (μ_{eff}), and is *inversely* proportional to the channel length (L) [10]. It is one reason why decreasing the channel length can increase I_D. As traditional scaling hit a bottleneck in increasing I_D (Fig. 1-5), replacing

the channel with high-mobility materials can further increase drain current and reduce gate delay [4]. Novel channel materials with intrinsically higher electron and hole mobilities, such as Ge, Si_xGe_{1-x}, III-V compounds, graphene and carbon nanotubes have all been considered possible candidates for future MOSFET building blocks. Figure 1-6 shows the comparison of carrier mobilities among some major semiconductor materials [13]. Germanium is of particular interest since its electron and hole mobilities are all higher than those of Si, and the difference between two carrier polarities is the smallest, which can in principle simplify the design and fabrication of CMOS circuits.

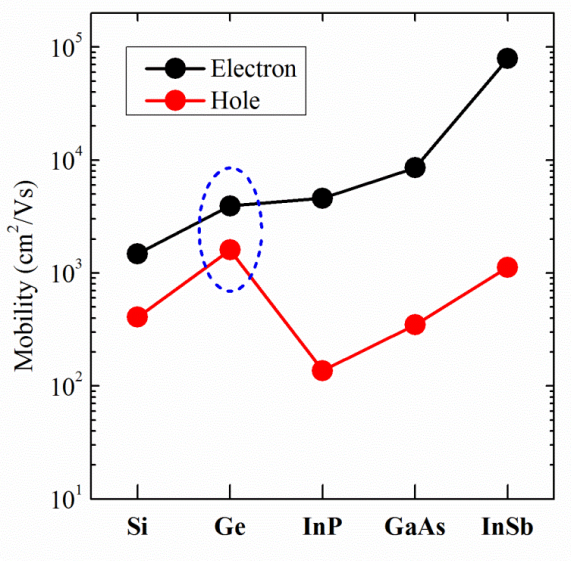


Figure 1-6. Bulk electron and hole mobility of major undoped semiconductors. Note that Ge has the highest hole mobility and the smallest disparity between the electron mobility. (Figure adapted from Ref. [13])

Another advantage of Ge to other candidates is that being a group IV semiconductor, it is compatible to current Si-technology. Moreover, the ability to grow Si_xGe_{1-x} alloy also enables the possibility of strain and bandgap engineering [13], [14].

1.3. MULTI-GATE STRUCTURES

Planar MOSFET scaling slows down partially due to its single-gate structure: the gate does not have full electrostatic control of the channel at short-channel lengths, in which the drain voltage affects the electric fields in the channel. The electrostatic coupling between the gate and channel can be improved by the use of multi-gate structures. Examples include double-gate (DG) FETs, FinFETs, tri-gate FETs, and gate-all-around (GAA) FETs, as shown in Fig. 1-7 [2].

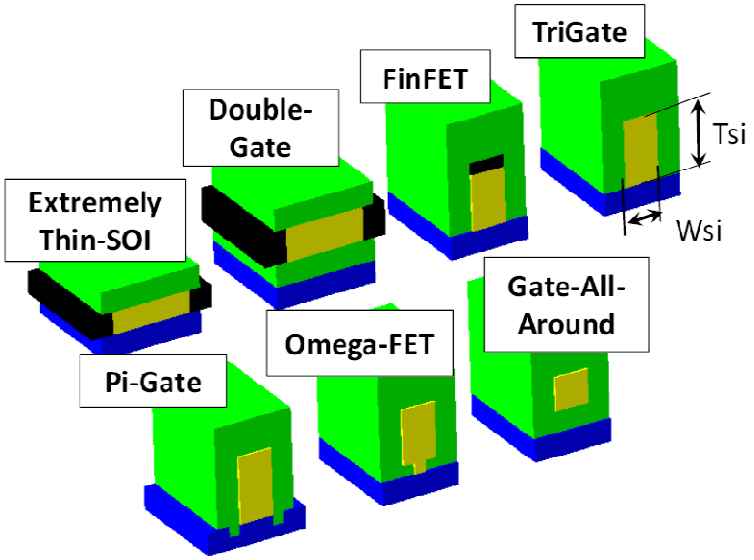


Figure 1-7. Multi-gate FET structures that can reduce short-channel effect. (Figure and caption adapted from Ref. [2])

Devices adopting multi-gate structures, when compared to their planar counterparts, show steeper sub-threshold slope, less OFF-state leakage, and higher drive current [1]. Among the structures shown in Fig. 1-7, the GAA structure provides the ultimate electrostatic control within the technology [2], [15]. Semiconductor nanowires (NWs) provide a natural platform for GAA structure, which can be formed either by metal-catalyzed chemical-vapor-deposition or by etching techniques. It is also possible to

grow radially [16], [17] and axially [18] heterogeneous structures in NWs, which can be used in strain and bandgap engineering.

1.4. SPIN AS COMPUTATIONAL VARIABLES

Instead of keeping focus on the transistor performance, one can introduce new functionalities into MOS-based technology to improve the overall circuit performance. For decades the logic operations in electronics are performed using the "charge" properties of electrons. However, the "spin" degree of freedom has largely been overlooked. By using spin as a computational variable in electronic devices (i.e. spintronics), it is possible to perform logic, communication and storage functions all within the semiconductor technology [19], [20]. Various advantages, such as greater computational capability, nonvolatile information storage, and reconfigurable output characteristics, etc. are expected in spintronics [19], [21], [22]. In this section below, we briefly introduce the area of spintronics and the principles of spin-based transistors.

The emergence of modern-day spintronics can be attributed to the discovery of giant magnetoresistance (GMR) effects, in which the resistance of a multilayer of magnetic and nonmagnetic metals depends strongly on the magnetization configurations [23]. Later the tunneling magnetoresistance (TMR) in magnetic tunnel junctions (MTJ) steadily increase with the advances in theoretical understanding and process technology, reaching more than 400% at room temperature [24]. These metal-based spintronic devices have found applications in hard disk write heads, magnetic random access memory (MRAM), etc. The interest in utilizing the spin degree of freedom in semiconductor devices started when the concept of the "spin-FET" was introduced [25]. The proposed device, similar to typical MOSFETs, uses semiconductor (preferably III-V compounds for their strong spin-orbit coupling) as the channel material. The source/drain

regions, instead of normal semiconductors, are composed of ferromagnetic materials with magnetization directions in parallel alignment, as shown in Fig. 1-8. The spin-FET exploits the Rashba spin-orbit coupling in the semiconductor channel to control the device resistance. The injected electrons have spin directions parallel to that of the source, and travel toward the drain ballistically in the $\boldsymbol{k}$-direction. By applying a gate voltage, the electrons see an effective magnetic field in the direction of $\boldsymbol{\Omega}$ due to the spin-orbit coupling in the channel, which causes precession of the electron spins during transit. The drain current is high (low) when arrived electrons have spin direction parallel (anti-parallel) to that of the drain.

Though the Datta-Das proposal ignited intense interest in semiconductor spintronics, it was later realized that the spin-FET has a fundamental issue in scalability. The conceptual device requires a channel long enough for the electron spins to make at least one 180° precession. Even in a material and structure with large spin-orbit coupling, the length scale is still expected to be on the order of 100 nm [26]. This limits the applications of spin-FETs in large-scale integrated circuits.

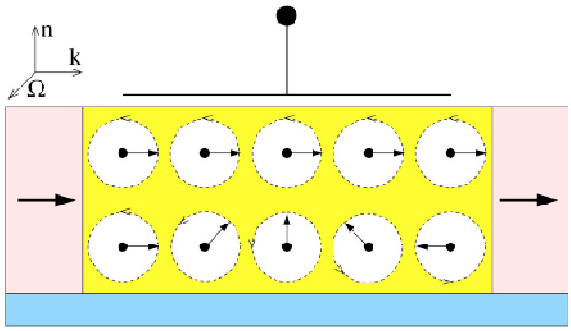


Figure 1-8. Schematic of the Datta-Das spin-FET. (Figure adapted from Ref. [19])

Other semiconductor devices utilizing spin as the information carrier are later proposed, such as spin-MOSFETs [22], [27], and spin logic gates [21]. The basic

principles of a spin-MOSFET are the same as those of a traditional MOSFET: the gate voltage controls the inversion charge density, and hence the channel conductivity. But similar to a Datta-Das spin-FET, the S/D are composed of ferromagnetic materials such that the injected carriers are spin-polarized. The key difference here is that the magnetization of the drain can be flipped, resulting in either parallel or anti-parallel magnetization configurations for the S/D, as shown in Fig. 1-89.

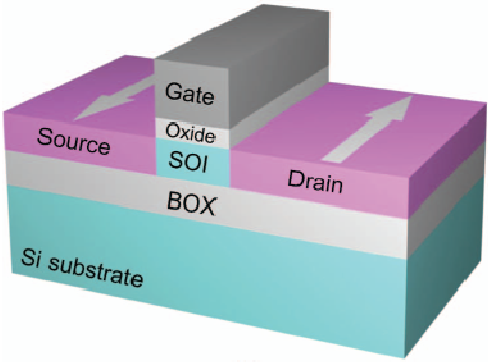


Figure 1-9. Schematic of a spin-MOSFET. The S/D are composed of ferromagnetic materials and the magnetization directions can be configured to parallel or anti-parallel alignments. (Figure adapted from Ref. [22])

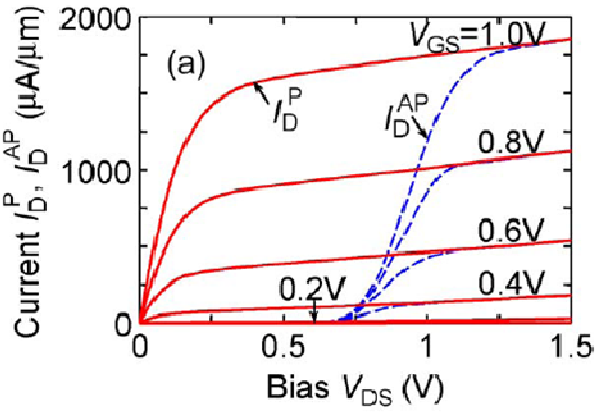


Figure 1-10. Calculated output characteristics of a spin-MOSFET, assuming 100% spin-polarization of the S/D. (Figure and caption adapted from Ref. [22])

The theoretical output characteristics of a spin-MOSFET is demonstrated in Fig. 1-10. The drain current (I_D) shows two group of traces based on the magnetization configurations: *P* for parallel and *AP* for anti-parallel. These results suggest that the spin-MOSFETs exhibit reconfigurable output characteristics, and can be used as the building blocks of logic applications. Moreover, unlike a spin-FET, it is preferable for the channel material to have *weak* spin-orbit coupling such that the injected carriers can retain the spin polarization while traveling toward the drain [22]. Conventional group IV semiconductors, e.g. Si and Ge, thanks to their inversion-symmetric crystal structure and natural abundance of isotopes with zero-nuclear spins, have weak spin-orbit coupling and long spin relaxation time. This suggests that part of the fabrication process of a spin-MOSFET can be readily integrated to current CMOS technology.

1.5. Role of Germanium Nanowires in Beyond CMOS Devices

In the previous sections, we listed potential routes to continuous performance scaling for integrated circuits: adopting multi-gate structures and novel channel materials for MOS-based devices, or a paradigm shift to spin-based devices. In the following chapters, we investigate the potential of germanium nanowires as the building block for these new devices.

Germanium has attracted interest as a replacing material for the Si-channel, thanks to its lighter effective electron/hole masses and its compatibility with Si technology. However, due to the larger dielectric constant and smaller band gap compared to those of Si, aggressively scaled planar Ge MOSFETs suffer from greater short-channel effects and larger OFF-state leakage current. The multi-gate structure can efficiently enhance the electrostatic control of gate over the channel, reducing the short-channel effects and increasing the scalability of Ge-based devices. Indeed, recent studies

have reported *p*- and *n*-type Ge FinFETs fabricated by top-down approaches [28]–[30], suggesting that Ge can serve as the material of choice for future logic devices. Germanium nanowires, on the other hand, are inherently compatible with the GAA structure, in which electrostatic coupling from the gate is maximized. In Chapter 2 we investigate the potential of this material system for complimentary MOS technology by demonstrating the *n*-channel operation in Ge-Si_xGe_{1-x} core-shell NW FETs.

We subsequently study the spin-polarized transport in Chapter 3, introducing possible spin relaxation mechanisms in semiconductors. Detailed spin relaxation processes in germanium, such as intervalley and intravalley spin scattering, will also be discussed. The standard model of spin injection from ferromagnetic metals into semiconductors will be presented.

In Chapter 4, we demonstrate lateral spin injection and detection in germanium nanowires, by using ferromagnetic metal contacts and tunnel barriers for contact resistance engineering. Using data measured from over hundred samples, we map out the contact resistance window for which lateral spin transport is observed, manifestly showing the conductivity matching required for spin injection. Our analysis, based on the spin diffusion theory, indicates that the spin diffusion length is larger than 100 μm in germanium nanowires at 4.2K. The summary will be presented in Chapter 5, and the focus of future work will be discussed.

Chapter 2: Germanium Nanowire *n*-type Field-Effect-Transistors

As the demand for high performance, low power semiconductor devices continue to grow, emerging materials, such as III-V compound semiconductors, and carbon nanotubes, have been pursued as potential candidates for future channel materials.

Germanium nanowire heterostructures enable the combination of band engineering [17] with the gate-all-around (GAA) structure, in which the electrostatic control of gate over the channel potential is enhanced [15]. High performance *p*-FETs on Ge-Si_xGe_{1-x} core-shell NWs have been demonstrated, showing high hole mobility thanks to the confinement provided by the valence band offset [16], [31]. In this chapter we focus on the *n*-channel operation in Ge-Si_xGe_{1-x} NW FETs, and study the limiting factors of the device performance.

The growth and characterization of the Ge-Si_xGe_{1-x} core-shell nanowires will be introduced first, followed by the NW *n*-type doping study using low energy phosphorous implantation. The fabrication process of Ω-gated, NW *n*-FETs will then be described. We compare the device characteristics fabricated using NWs with and without the shell, and demonstrate performance metrics comparable to state-of-the-art Ge *n*-FinFETs fabricated from top-down approach. Lastly, using the channel-length dependence of NW FET characteristics, we are able to isolate R_c out of the total device resistance, and conclude that the intrinsic channel resistance is the main limiting factor of the I_{ON} of Ge NW *n*-FETs, which can be explained by the presence of large interface trap density at the NW/dielectric interface.

2.1. DEVICE FABRICATION

2.1.1. Nanowire Growth

The NWs are grown on a Si (111) substrate, in a cold-wall, ultra-high vacuum chemical-vapor deposition (UHV-CVD) chamber, via gold-catalyzed vapor-liquid-solid (VLS) growth mechanism, as depicted in Fig. 2-1. Prior to loading, the Si wafer with a 7Å-thick, evaporated Au layer is treated with diluted hydrofluoric acid (HF) to remove the native oxide [Fig. 2-1(a) and (b)]. The wafer is then annealed at 475°C in H_2 for 20 min, such that Au coalesces into nanoparticles, which serve as the catalysts for NW growth, as shown in Fig. 2-1(c). The Ge NW core [Fig. 2-1(d)] is grown at a substrate temperature of 250°C and a chamber pressure of 2.5 Torr, with a 50 sccm (standard cubic centimeters per minute at STP) flow of GeH_4 (20.8% in He). An epitaxial Si_xGe_{1-x} shell is grown *in situ* after the Ge core by co-flowing SiH_4 (100%, 50 sccm) and GeH_4 (10 sccm) precursors at 400°C and 20 mTorr [Fig. 2-1(e)]. The resulting NWs have a length of 6.5 μm, and a total diameter (*d*) of 30-70 nm. An example scanning electron microscopy (SEM) image is shown in Fig. 2-1(f), in which we can see that the NWs grow epitaxially on the Si (111) substrate. Transmission electron microscopy (TEM) and energy dispersive X-ray spectroscopy data are used to assess the growth and content of the shell. Figure 2-2 is an example TEM image, showing the epitaxial shell growth on the core. We determine that the shell is 8 nm-thick, and has a silicon content of 35% [32]. A NW wafer that underwent only the Ge core growth process is also prepared as the control sample in this study.

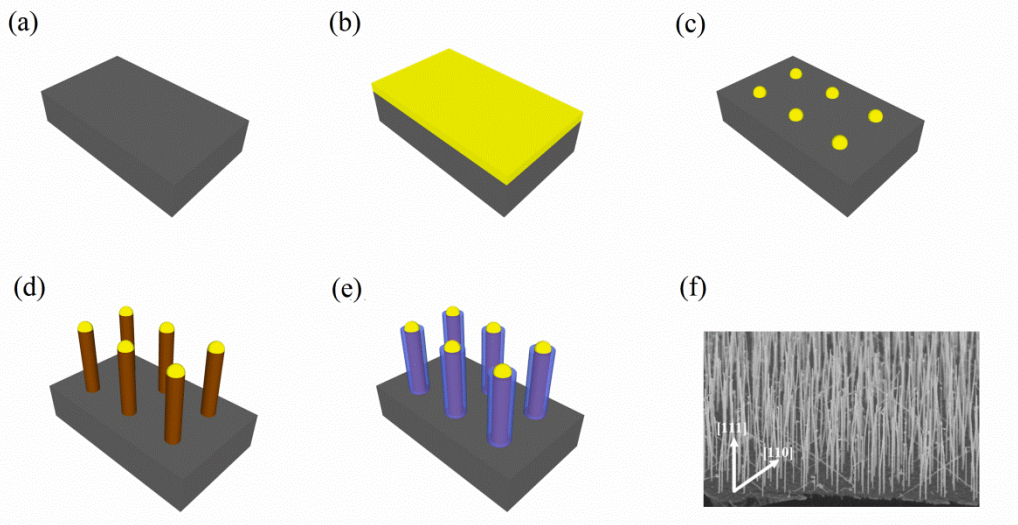


Figure 2-1. NW growth process flow (a) A Si (111) is used as the substrate. (b) 7Å-thick Au is deposited by e-beam evaporation. (c) The wafer is annealed in a cold-wall UHV CVD chamber at high temperature such that the Au film coalesces into nanoparticles, which serve as catalysts for the growth. (d) The Ge NW core is grown using GeH_4 as precursor, via VLS mechanism. (e) The Si_xGe_{1-x} Shell is grown by co-flowing SiH_4 and GeH_4 at the same time. (f) An example SEM image of the grown NWs.

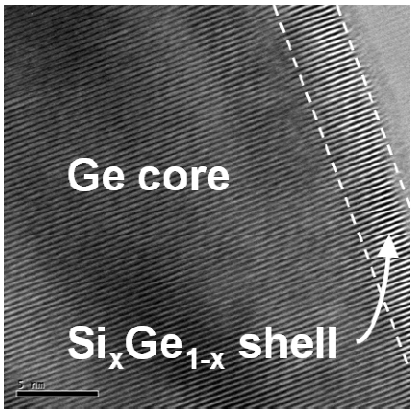


Figure 2-2. Core-shell NW TEM image. The boundary of the shell is indicated by the white dashed lines. (Batch number: NW056)

2.1.2 Phosphorus-implanted nanowires

In order to realize highly doped, *n*-type S/D semiconductor region in the

nominally undoped Ge-Si_xGe_{1-x} core-shell NWs, we employ low-energy ion implantation, using phosphorus as dopant. To characterize this processing step, the NWs are suspended in ethanol and transferred onto a 50 nm-thick SiO_2/p-Si substrate. The sample are then implanted with phosphorus at an ion energy of 6 keV and a normal incidence angle, with dose of 10^{15} cm^{-2}, followed by a 500°C, 5 min anneal in a N_2 ambient for dopant activation and NW recrystallization [33]. Multi-terminal, back-gated FETs with various channel lengths (L) are subsequently fabricated using e-beam lithography (EBL), Ni evaporation, and lift-off. The highly doped Si substrate serves as back-gate in this case. A scanning electron micrograph (SEM) of the finished devices is shown in the inset of Fig. 2-3(a).

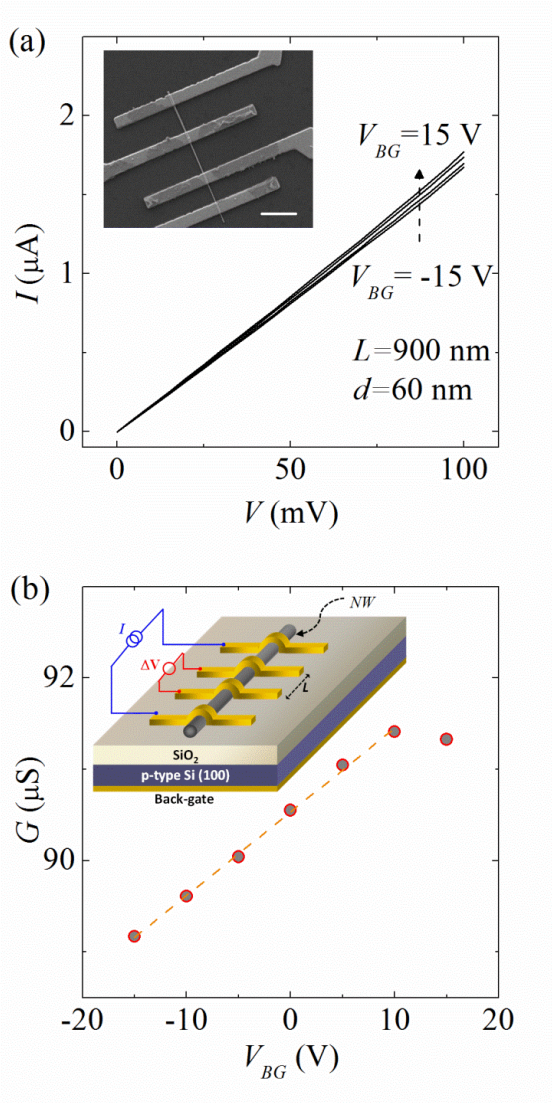


Figure 2-3. Electrical characteristics of P-implanted Ge-Si_xGe_{1-x} NWs. (a) Two-point *I vs. V* data for a P-implanted back-gated NW device. The device shows weak back-gate dependence, consistent with a high doping density. Inset: SEM image of a multi-terminal, back-gated device. The scale bar is 500 nm. (b) *G vs.* V_{BG} data obtained from four-point measurement on the same pair of contacts in (a). Inset: four-point measurement scheme.

To assess the NW resistivity and metal/NW contact resistance of the implanted region, we conduct two-point and four-point back-gated current (*I*) - voltage (*V*) measurements for the same pair of contacts. Figure 2-3(a) shows an example of the two-

point I vs. V data, at different back-gate bias (V_{BG}) from -15 V to 15 V. We note that I is linear with V, and only weakly dependent on V_{BG}, consistent with highly doped semiconductors. The intrinsic channel conductance (G) can be extracted from the voltage drop (ΔV) between two inner contacts while flowing current between two outer contacts, and using $G=I/\Delta V$ [Fig. 2-3(b) inset]. We extract an intrinsic nanowire resistivity of 8.6±3.3 mΩ·cm, and a metal (Ni)-nanowire contact resistance of 24±7 kΩ, corresponding to a specific contact resistance of $8.6\pm3.1\times10^{-6}$ Ω·cm^{-2} [34]. The P-implanted nanowire resistivity and metal/NW specific contact resistance could be further reduced by using flash rapid thermal process for dopant activation [35].

2.1.3. Fabrication of NW *n*-FETs

We choose a gate-last process for the NW *n*-FETs fabrication, as depicted in Fig. 2-4. Figure 2-4(a) is a cross-sectional SEM of the core-shell NW wafer, showing the epitaxial growth of NWs along (111) direction. After transferring the NWs onto a 50 nm-thick SiO_2/*p*-Si substrate, a polymethyl-methacrylate (PMMA) implantation mask is defined by EBL [Fig. 2-4(b)]. The PMMA mask width sets the NW *n*-FET channel length, L_{ch}. A phosphorous implantation using the same conditions described in the previous section defines the S/D [Fig. 2-4(b)]. After dopant activation [Fig. 2-4(c)] and a cyclic cleaning with diluted HF and deionized water, a thin layer of native oxide is grown by rapid-thermal oxidation (RTO) at 400°C for 90 sec, which has been shown to passivate the surface for planar Ge *n*-FETs [36]. A high-κ Al_2O_3 layer with effective oxide thickness of 3.7 nm is subsequently deposited by atomic layer deposition (ALD) at 250°C, followed by EBL, TaN sputtering and lift-off to finish to gate stack, as shown in Fig. 2-4(d). The gate length (L_g) and gate layout are carefully chosen to fully cover the undoped NW section previously protected by PMMA. Finally, S/D metal contacts are

formed by EBL, Ni deposition and lift-off [Fig. 2-4(e)]. Multiple devices with various gate lengths are fabricated in order to study the scaling properties of NW *n*-FETs. Figure 2-4(f) shows a SEM of a completed device. All NW *n*-FETs have the same S/D extension lengths (L_{ext}) [Fig. 2-4(e)], and Ni contact width in order to minimize the impact of contact resistance variation on the device characteristics. A separate set of devices, serving as reference, is also fabricated using the same process flow, but using Ge NWs without the Si_xGe_{1-x} shell as channel material.

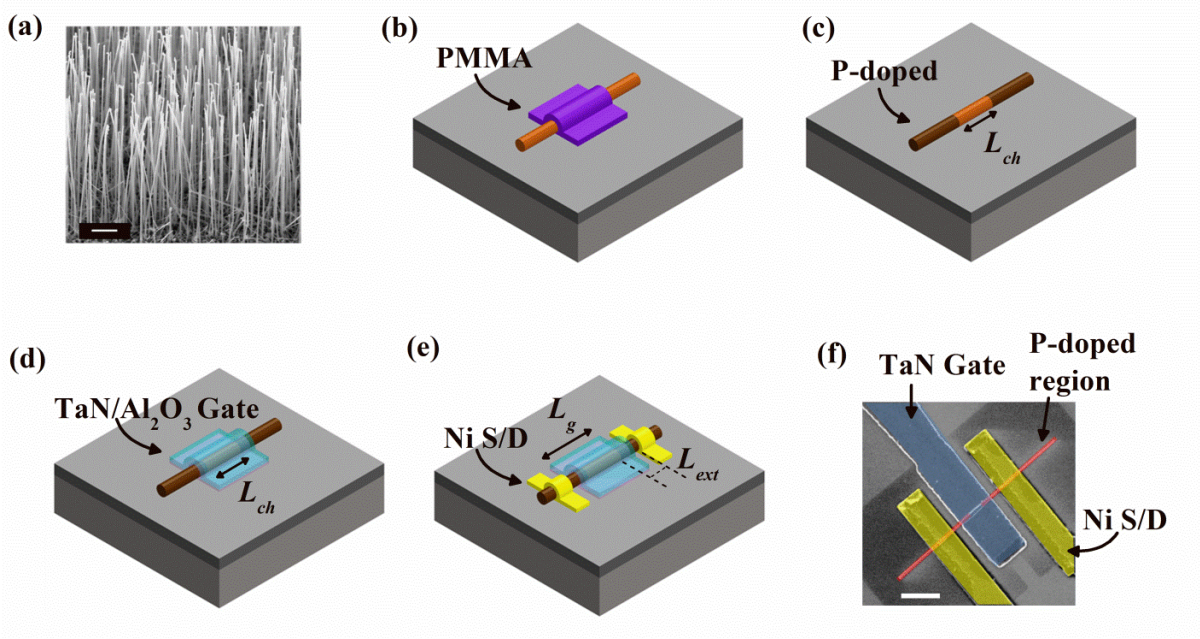


Figure 2-4. Process flow for NW *n*-FETs. (a) SEM of the Ge-Si_xGe_{1-x} core-shell NWs epitaxially grown on a Si (111) substrate (Batch number: NW048). The scale bar is 1 μm. (b) PMMA is used as the mask for P-implantation; the exposed NW sections represent the S/D regions. (c) PMMA removal and dopant activation anneal define the S/D. The channel (L_{ch}) is defined by the previously masked region. (d) Al_2O_3 and TaN are then deposited to form the gate stack. (e) The S/D contacts are formed by EBL, Ni deposition and lift-off. Each fabricated device has the same L_{ext} and contact width. (f) SEM of a completed device. The yellow (blue) areas represent the contact (gate) metal. The NW sections that receive P-implantation are highlighted in red. The scale bar is 500 nm.

2.2. DEVICE CHARACTERIZATION & SCALING PROPERTIES

2.2.1. Ge NW *n*-FETs

We first discuss the device performance of the *n*-FETs fabricated using Ge NWs as the channel material. Figure 2-5 shows an example of the electrical characteristics, including (a) the transfer characteristics: the drain current (I_D) versus gate voltage (V_G) at different drain biases (V_D), and (b) the output characteristics: I_D vs. V_D as a function of V_G. The drain current presented here is normalized to nanowire diameter. The device, with L_{ch}=320 nm and d=50 nm, shows an I_{ON} of 4 μA/μm and an ON/OFF ratio less than 10^3. A noteworthy observation is that in the output characteristics [Fig. 2-5(b)], I_D is not a linear function with V_D at low bias. This indicates a barrier for electron injection at S/D contacts. Indeed, the Fermi level at the metal/*n*-Ge interface is typically pinned at the top of Ge valence band [37], [38], resulting in a large Schottky barrier for electrons, hence inefficient electron injection. We also note that the transfer characteristics in Fig. 2-5(a) show a large hysteresis in V_G, which also suggests a large D_{it} of this device in spite of the RTO techniques being employed for Ge surface passivation [36].

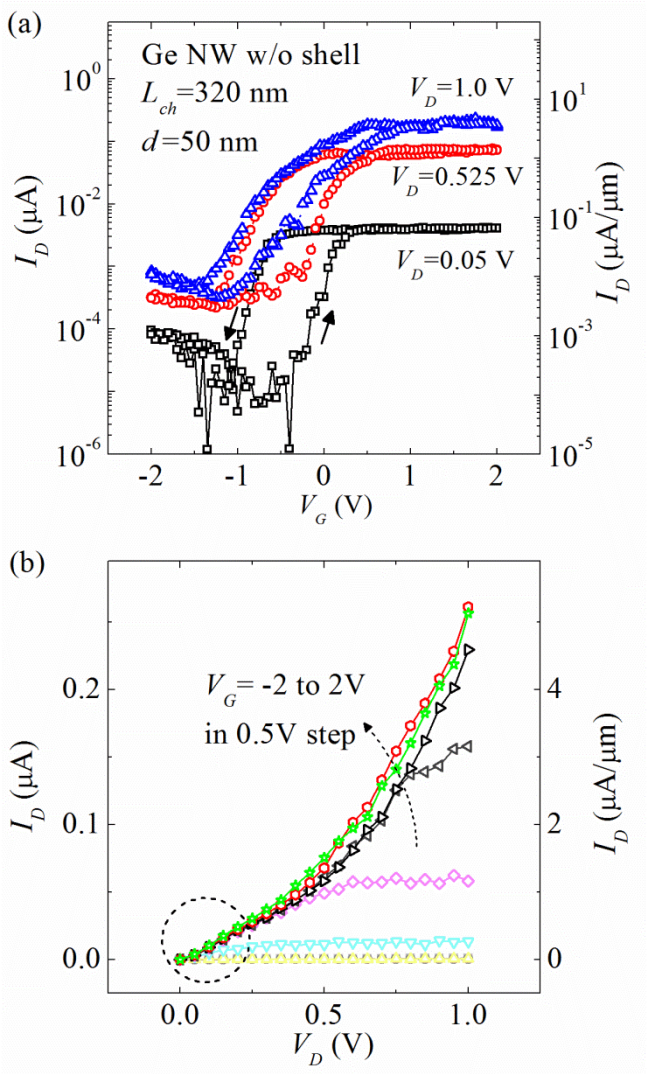


Figure 2-5. Electrical characteristics of Ge NW *n*-FETs. (a) Transfer characteristics of a NW *n*-FET fabricated on Ge NWs. The arrows indicate the V_G sweep direction, and a large hysteresis is observed. (b) Output characteristics of the same device. I_D is not linear with V_D at small biases, as indicated by the dashed circle. The right-hand axes show the current normalized by the NW diameter.

2.2.2. NW *n*-FETs with core-shell NW channel

Next we present the transfer and output characteristics of a Ge-Si_xGe_{1-x} core-shell NW *n*-FET in Fig. 2-6(a) and (b), respectively. With a similar device dimension (L_{ch}=380

nm and d=40 nm), this device exhibits an improved performance than the reference sample, namely an I_{ON} of 60 μA/μm and an ON/OFF ratio of 5×10^4. Both the top-gate and back-gate leakage currents are negligible, less than 10^{-4} μA/μm under all bias conditions. The OFF-state current increases by nearly two orders of magnitude as V_D is increased from 50 mV to 1 V, as shown in Fig. 2-6(a), which can be explained by the gate-induced drain leakage. These performance metrics are comparable to those of Ge *n*-FinFETs fabricated from epi-Ge grown directly on Silicon-on-Insulator [39], [40]. Unlike the reference device without a Si_xGe_{1-x} shell (Fig. 2-5), the transfer characteristics exhibit only a negligible gate hysteresis [Fig. 2-6(a)]. This can be attributed to an improved NW/Al_2O_3 interface thanks to the passivation provided by the Si_xGe_{1-x} shell. Moreover, the existence of a Si_xGe_{1-x} shell enables efficient electron injection at S/D, as evidenced by the low contact resistance presented in Fig. 2-3, as well as the linearity of I_D at low V_D in Fig. 2-6(b).

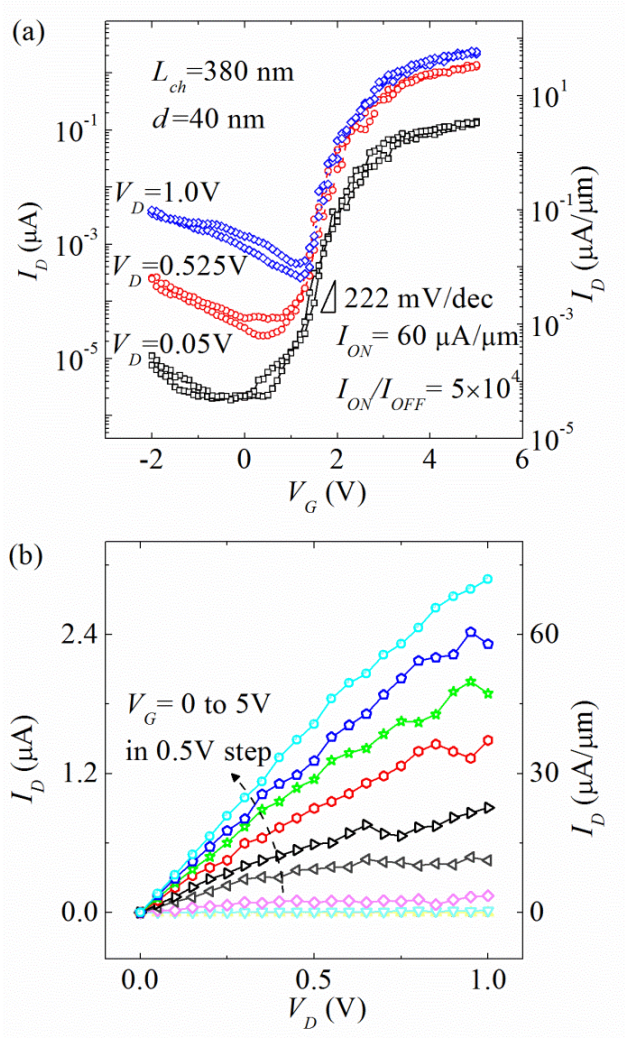


Figure 2-6. Electrical characteristics of a Ge- Si_xGe_{1-x} core-shell NW *n*-FET. (a) Transfer characteristics, showing a I_{ON} of 60 μA/μm, and a ON/OFF ratio of 5×10^4. (b) Output characteristics of the same device. The right-hand axes show the normalized current with respect to the NW diameter.

2.2.3. Scaling properties of core-shell NW *n*-FETs

In Fig. 2-7 we show the total NW *n*-FETs resistance ($R_{total}\equiv V_D/I_D$) vs. L_{ch} for the devices probed in the study. The data are taken at V_D=50 mV, and at fixed V_G-V_T values, where V_T is the threshold voltage. At each V_G-V_T value, R_{total} has a linear dependence on L_{ch}, and the linear fits share a common intercept, at R_c=0.21 MΩ and ΔL=240 nm. Here

R_c includes the metal/NW interface resistance and the NW resistance of the doped sections, and ΔL the channel length reduction due to dopant diffusion during the thermal activation. The effective channel length can be defined as $L_{eff} = L_{ch} - \Delta L$. We note that the ΔL value is larger than that of NW *p*-FETs using B-doped S/D [31], thanks to the faster diffusion of phosphorous than boron in both germanium and silicon [41].

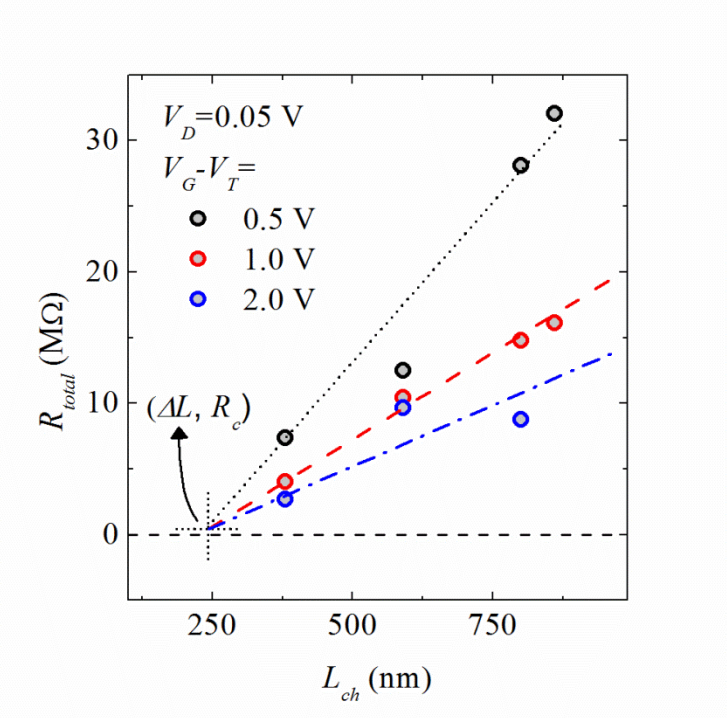


Figure 2-7. R_{total} *vs.* L_{ch} at different V_G-V_T values of the core-shell NW *n*-FETs at V_D=50 mV. A channel length reduction (ΔL) of 240 nm and contact resistance (R_c) of 0.21 MΩ can be determined from the intercept of the linear fits of each V_G-V_T group. The diameters of NWs examined here range from 35 to 60 nm.

In the diffusive transport regime, R_{total} can be expressed as $R_{total} = R_c + R_{ch}$. R_{ch} is proportional to $L_{eff}/[C_{ox}(V_G - V_T)]$, where C_{ox} is the dielectric capacitance per unit length. The C_{ox} values, calculated using self-consistent simulations (Sentaurus, ©Synopsis), range from 750 aF/μm to 1050 aF/μm, for *d* values between 40 nm and 60 nm. By plotting R_{total} versus L_{ch}, we are able to decouple R_c and R_{ch}, and investigate the

limiting factors of the ON-current of Ge-Si_xGe_{1-x} core-shell NW *n*-FETs. Figure 2-7 data reveals that at a value of 0.21 MΩ, R_c is at least one order smaller than R_{total} in all devices. This indicates that the device characteristics are not dominated by the contacts, but rather by R_{ch}.

2.2.4. Short-channel effects in core-shell NW *n*-FETs

Figure 2-8 data summarizes the channel length dependence of the OFF-state device characteristics, namely the *SS*, V_T, and drain-induced barrier lowering (DIBL). The DIBL value is defined as the change of V_T at V_D = 1 V with respect to that of V_D= 50 mV. Figure 2-8(a) shows the *SS,* extracted at V_D=50 mV for devices with L_{eff} from 70 nm to 620 nm. The *SS* ranges from 180 mV/dec. to 500 mV/dec. without a clear dependence on L_{eff}. On the other hand, both V_T and DIBL show a monotonic dependence on L_{eff}, particularly at channel lengths below 300 nm. The large *SS* values and their apparent insensitivity to the channel length can be explained by a large D_{it}, which obscures the short channel effect. Unlike its impact on *SS*, the D_{it} has only secondary effects on both V_T and DIBL via electrostatic coupling to the channel potential [42]–[45], which can be explained in the frame work of top-of-the barrier model [46], as discussed in the following section.

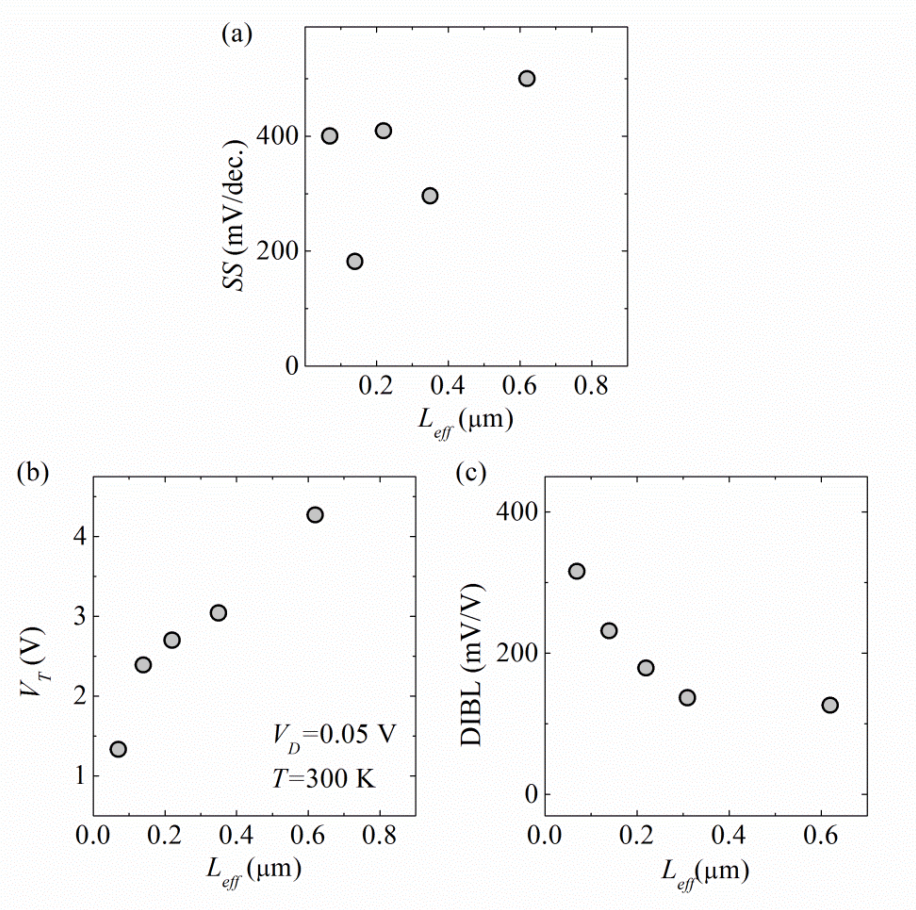


Figure 2-8. OFF-state device characteristics of Ge-Si_xGe_{1-x} core-shell NW *n*-FETs. (a) *SS vs.* L_{eff} data. The *SS* values are larger than the thermal limit and do not show a clear dependence on L_{eff}. (b) V_T *vs.* L_{eff} and (c) DIBL *vs.* L_{eff} data shows the onset of short-channel effect.

2.2.4.1. Top-of-the-barrier model

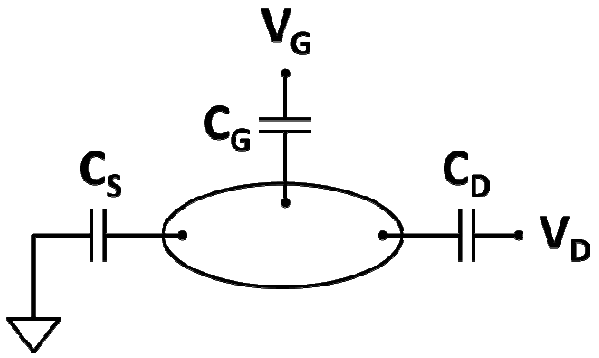


Figure 2-9. Circuit model for NW FETs.

The equivalent circuit model for a short-channel NW FET is shown in Fig. 2-9. Here C_G, C_D, and C_S represents the capacitance of gate, drain and source to the channel, respectively. V_G (V_D) is the bias to the gate (drain) terminal, and the source is grounded. To calculate the self-consistent potential, U, we first find out the potential due to the terminal biases, which is

$$U_L = -q(\alpha_G V_G + \alpha_D V_D).$$

Here $\alpha_{G,D} = C_{G,D}/(C_G + C_D + C_S) \equiv C_{G,D}/C_\Sigma$, q is the elemental charge and C_Σ is the parallel combination of the three capacitors. Next we consider the potential induced by the mobile charges in the channel, $U_P = q^2(N_1 + N_2)/C_\Sigma$, where $N_1 = -U\frac{1}{2}D'_{it}$ and $N_2 = -(qV_D - U)\frac{1}{2}D'_{it}$. N_1 and N_2 are the number of states of positive and negative k-values in momentum space filled by the source and drain due to D_{it}, respectively. D'_{it} is the total number of interface traps in the device, defined as $D_{it} \cdot \pi d L_{ch}/q$. Using $U = U_L + U_P$, we get

$$U = U_L + \frac{q^2}{C_\Sigma}\left(-UD'_{it} - \frac{qV_D D'_{it}}{2}\right)$$

$$U\left(1+\frac{q^2D'_{it}}{C_\Sigma}\right)=U_L-\frac{q^2}{2C_\Sigma}(qV_DD'_{it})$$

First we consider the case when transistor is in the subthreshold region, i.e., V_D is small. Therefore,

$$U\approx U_L/\left(1+\frac{q^2D'_{it}}{C_\Sigma}\right)$$

Considering $I_{OFF}\propto e^{-U/kT}$, where k is the Boltzmann constant, we can write I_{OFF} as

$$I_{OFF}\propto exp\left[\frac{q\alpha_GV_G}{kT}\Big/\left(1+\frac{q^2D'_{it}}{C_\Sigma}\right)\right]$$

$$=exp\left(\frac{q}{kT}\frac{C_G}{C_\Sigma}\frac{1}{1+C'_{it}/C_G}V_G\right)$$

where C'_{it} is defined as $q^2D'_{it}$. The *SS* is then

$$SS\propto\frac{dV_G}{d\ln I_{OFF}}=\frac{kT}{q}\frac{C_\Sigma}{C_G}(1+C'_{it}/C_G)$$

$$=\frac{kT}{q}\left(\frac{C_\Sigma}{C_G}+\frac{C'_{it}}{C_G}\right)$$

$$=\frac{kT}{q}\left(1+\frac{C_D+C_S}{C_G}+\frac{C'_{it}}{C_G}\right)$$

This result shows that C'_{it} has a first order effect on the *SS*, which can explain the rather large *SS* in our devices. Using the SS values of Fig. 2-8(a), self-consistently calculated $C_G(=C_{ox}\cdot L_{ch})$ and neglecting C_D and C_S, we estimate a D_{it} of 18±8×10^{12} V^{-1}·cm^{-2} in our devices, corresponding to a C'_{it}/C_G ratio between 2 and 7. We can see that a large D_{it} can lead to increased *SS*, and the variation in D_{it} among devices can mask the change of *SS* due to SCE.

Next we want to calculate the effect of V_D on the threshold voltage. The total number of charges in the channel, N, is $N_1 + N_2$, which reads

$$N = -UD'_{it} - \frac{qV_D}{2}D'_{it}$$

$$= -\frac{U_L - \frac{q^2}{2C_\Sigma}(qV_D D'_{it})}{1 + \frac{q^2 D'_{it}}{C_\Sigma}}D'_{it} - \frac{qV_D}{2}D'_{it}$$

$$= -\frac{U_L - \frac{qV_D C'_{it}}{2C_\Sigma}}{1 + \frac{C'_{it}}{C_\Sigma}}D'_{it} - \frac{qV_D}{2}D'_{it}$$

$$\approx -\frac{U_L}{1 + \frac{C'_{it}}{C_\Sigma}}D'_{it}\text{ , assuming small } V_D$$

Suppose the number of charges at threshold voltage is N^*, we can write the above expression as

$$\left(1 + \frac{C'_{it}}{C_\Sigma}\right)q^2 N^* = -U_L C'_{it}$$

$$-U_L = \left(\frac{1}{C'_{it}} + \frac{1}{C_\Sigma}\right)q^2 N^*$$

$$q\alpha_G V_G + q\alpha_D V_D = \left(\frac{1}{C'_{it}} + \frac{1}{C_\Sigma}\right)q^2 N^*$$

$$V_G = -\frac{\alpha_D}{\alpha_G}V_D + \left(\frac{C_\Sigma}{C'_{it}} + 1\right)\frac{qN^*}{C_G}$$

Here V_G represents the threshold voltage, and the first term on the right-hand side is the modification due to V_D, also known as DIBL. It can be seen from these equations that the DIBL is less sensitive to D_{it} compared to the *SS*, as shown in Fig. 2-8(b) and (c).

2.2.4.2. Effective mobility of Core-shell NW n-FETs

The detrimental effects of high D_{it} on I_{ON} of FETs are two-fold. First, it adds an

additional capacitance in series of C_G, rendering the gate control over the channel less effective, which results in reduced inversion charge density in the channel. Second, a larger D_{it} leads to increased Coulomb scattering for electrons in the inversion layer, which degrades the electron mobility and lowers I_{ON}. Indeed, the inversion charge mobility, calculated using $\mu_{eff} = L_{eff}/[R_{ch}C_G(V_G - V_T - V_D/2)]$, is approximately 10 $cm^2/(V{\cdot}s)$, as shown in Fig. 2-10. We note however, that since the effective gate capacitance is lower than C_G due to the large D_{it}, the mobility value should be regarded as a lower bound estimate.

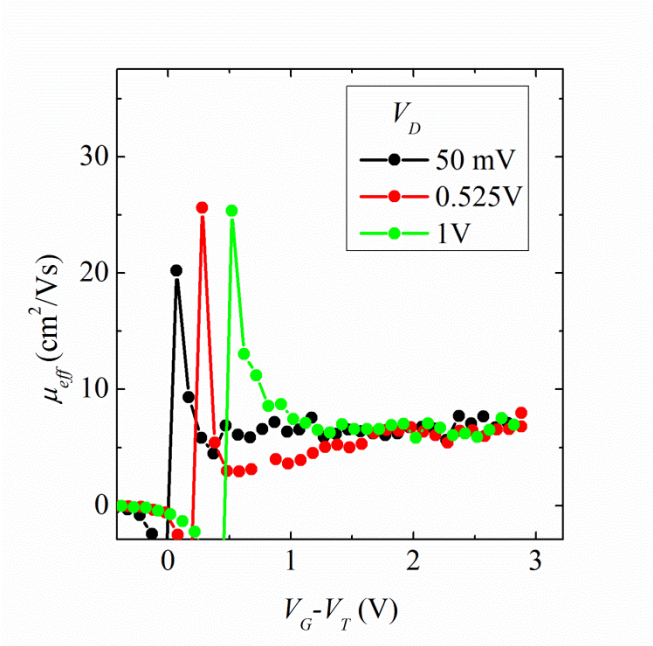


Figure 2-10. Effective mobility of the Ge-Si_xGe_{1-x} NW *n*-FET presented in Fig. 2-6.

2.2.5. Mobile charge distribution in core-shell NW *n*-FETs

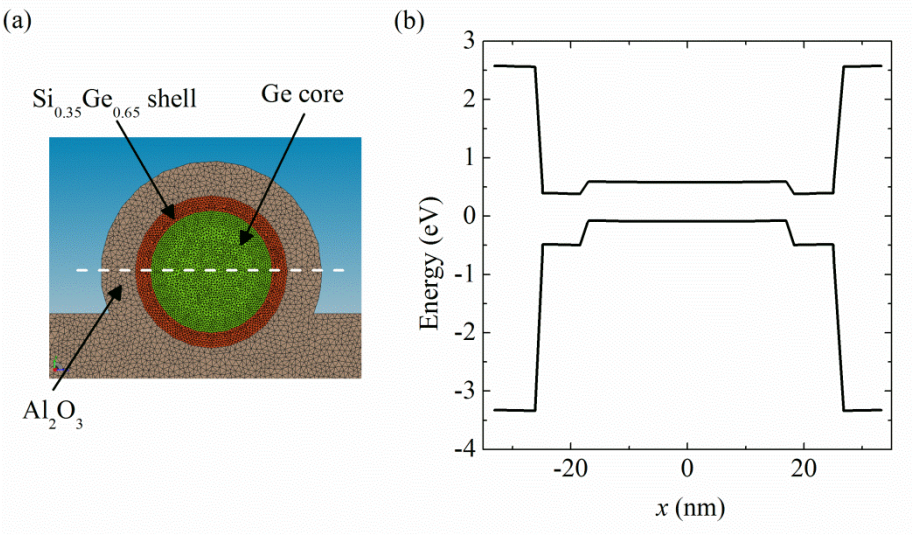


Figure 2-11. Simulation structure and band edges in core-shell NWs (a) Schematic of core-shell NWs. (b) Band edges of a Ge-$Si_{0.35}Ge_{0.65}$ core-shell NW considering the effect of elastic strain. The *x*-cut is taken at the center of the NW along the *x*-axis, as indicated by the dashed line in (a).

Another mechanism responsible for a lower I_{ON} is the distribution of carriers in the channel. Assuming a coherently strained core-shell NW [47], and the effect of the elastic strain on the energy bands [14], we calculate a Ge-Si_xGe_{1-x} conduction band offset of -0.19 eV. We then use self-consistent numerical simulations (Sentaurus, Synopsis) to calculate the carrier distribution in the NWs. Figure 2-11(a) shows the structure used in the simulations, and the energy band edges along the x-axis at the center of the NW is shown in Fig. 2-11(b). Figure 2-12(a) data plot the electron densities along the x-axis as a function of V_G, suggesting that most electrons are in the shell. Indeed, plotting the total electron density of the cross-section of the NW in both shell and core as a function of gate voltages [Fig. 2-12(b)], we can see that only the electron density in the shell responds to V_G. Consequently, the inversion charges reside near the dielectric/NW interface, and are subject to increased surface roughness and fixed interface charge

scattering.

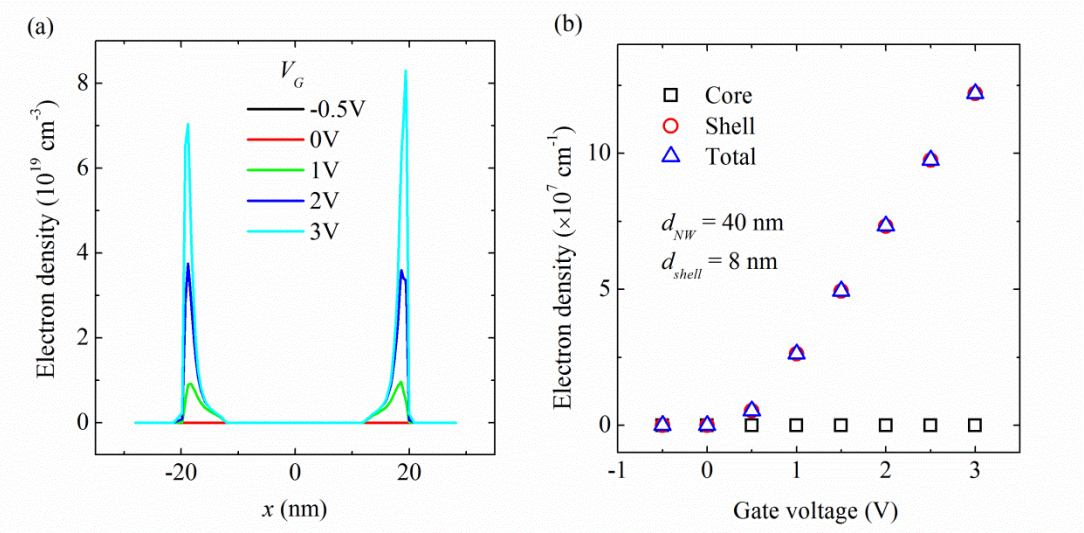


Figure 2-12. Inversion charge distribution in core-shell NWs. (a) Electron density plotted along the *x*-axis at the center of the NW as function of gate-voltage. (b) The electron density integrated over the cross-section of the NW. Majority of the inversion charges reside in the shell rather than core.

2.3. CONCLUSIONS

	Planar [48]	Ge/SOI FinFET [49]	Ge (triangular)/SOI FinFET [40]	**This work Nanowire** [50]
L/W/H	5μm/30μm/--	120nm/40nm/60nm	350nm/58nm/58nm	380nm/40nm/40nm
EOT (nm)	0.76	GeO_2/5.5 nm Al_2O_3	5.5nm	3.7nm
I_{ON} (μA/μm)	12	80	110	60
ON/OFF	10^3	$>10^5$	1.6×10^4	5×10^4
SS (mV/dec.)	80	110	94	222
DIBL (mV/V)	--	110	--	200

Table 2-1. Comparison of planar Ge *n*-FETs, FinFETs using top-down approaches and NW *n*-FETs.

We presented the realization of Ge-Si_xGe_{1-x} core-shell NW *n*-FETs using highly doped source and drain, and systematically studied their scaling properties. The devices exhibit comparable I_{ON} and ON/OFF ratio to state-of-the-art Ge *n*-FinFETs fabricated by top-down techniques, as shown in Table 2-1. The scaling study shows that the Ge-Si_xGe_{1-x} core-shell NW *n*-FETs channel, and not contact resistance controls the ON state current, a finding explained by a large density of interface traps at the dielectric/NW interface. Planar, long channel Ge *n*-MOSFETs with optimized gate stacks have shown D_{it} of the order of 10^{11} $V^{-1}\cdot cm^{-2}$, as measured by low-temperature conductance method [48], [51], [52]. While the I_{ON} values measured in our Ge/Si_xGe_{1-x} NW *n*-FETs are comparable to those of short channel Ge *n*-FinFETs fabricated using top-down methods [39], [40], our data strongly suggested that these values can be increased significantly using optimized gate stacks.

Chapter 3: Spin injection and relaxation in semiconductors

Using the spin degree of freedom in electronic devices can potentially introduce novel functionalities in solid-state systems. In metal-based spintronics, the discovery of giant magnetoresistance (GMR) has fueled intense research in the correlation of electron spins and electrical resistance [53]. GMR effect describes the resistance difference in a ferromagnetic (*F*) – nonmagnetic (*N*) multilayered metal structures when the magnetization of *F*'s are parallel or anti-parallel. It results from the fact that in magnetic materials, the electron scattering rates depends on the relative orientation of electron spins to local magnetization [54], [55].

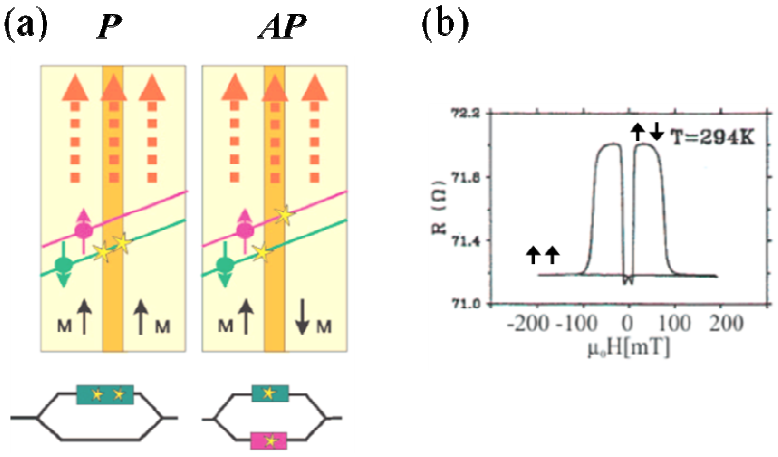


Figure 3-1. GMR effect. (a) A multilayer structure with a nonmagnetic film sandwiched by two ferromagnetic layers. In the case shown in the left, the two magnetic layers have same magnetization (***M***), and the electrons with spin parallel to the layers can pass through without being scattered. This creates a short circuit for the structure, as shown in the circuit model below. In the case with anti-parallel (AP) magnetizations (right panel), either electron spins are subject to scattering in one layer or the other, resulting in a circuit model with two parallel resistors. (b) Magnetoresistance of a Co/Au/Co structure. The arrows indicate the magnetization directions of the Co layers. (Figure and caption adapted from Ref. [55], [56])

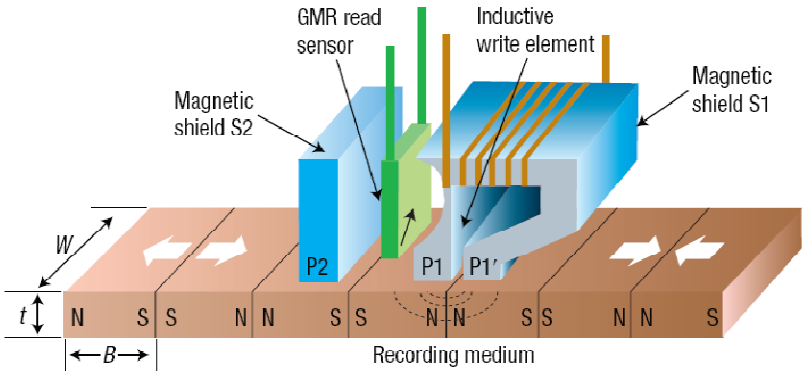


Figure 3-2. Schematic of the magnetoresistive HDD write/read head. The ring-type, inductive element is used for writing information onto the recording medium, while the magnetoresistive sensor is used for reading. W is the track width and t is the thickness of the recording medium. B is the length of magnetic domains. (Figure and caption adapted from Ref. [57]).

Figure 3-1(a) explains the origin of GMR effect in a typical F/N/F structure. In the left panel, the ferromagnetic layers have same magnetizations, therefore the electrons with parallel spin direction can pass through, creating a short-circuit channel for conduction current and a low resistance state. On the other hand, when one of the magnetic layer's magnetization is reversed, this short-circuit channel does not exist because either spin directions are subject to scattering in one of the magnetic layers. The structure now exhibits a high resistance state. The magnetoresistance data of a typical Co/Au/Co multi-layer structure is shown in Fig. 3-1(b). The discovery of GMR greatly improves the performance and capacity of commercial hard disks (HDD) as the sensors based on GMR effects replaced the previous anisotropic magnetoresistive (AMR) sensors [57], as shown in Fig. 3-2. AMR describes the dependence of the electrical resistance of a piece of ferromagnetic metal on the angle between the direction of magnetization and electrical current, and typically does not exceed a few percent [57]. GMR, on the other hand, can reach as large as 85% [23]. The introduction of GMR sensors to HDD

technology has since greatly improved the sensitivity of HDD heads and the overall area density [54], [57]. Even larger magnetoresistance ratio can be achieved in magnetic tunnel junctions (MTJs), in which the normal metallic film is replaced by non-conducting insulators [58]–[60]. Very large tunneling magnetoresistance (TMR) up to 600% has been reached in CoFeB/MgO/CoFeB structures [24]. TMR sensors have been implemented in commercial HDD heads, and demonstrated better signal-to-noise ratio than GMR sensors thanks to its higher magnetoresistance ratio [61].

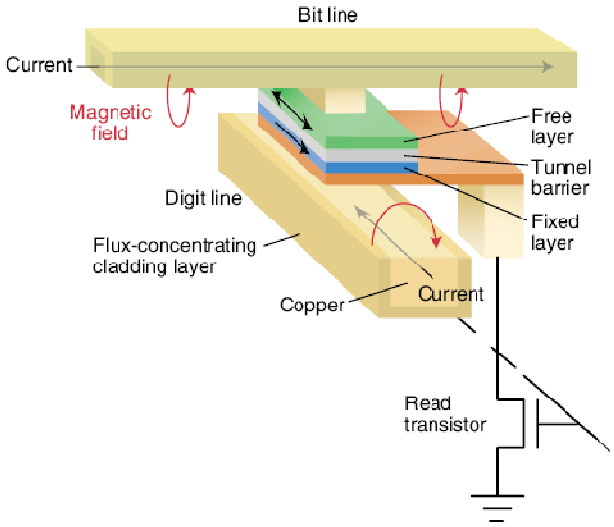


Figure 3-3. Schematic of a MRAM bit cell. The MTJ is in series with a transistor for bit read selection. Here the magnetization of the free layer can be programmed by flowing current through the Bit and Digit lines. (Figure and caption adapted from Ref. [62])

MTJs may also find applications in magnetic random access memories (MRAM), as shown in the schematic in Fig. 3-3 [62]. The information is encoded in the magnetization configurations of the MTJ, which can be programmed by rotating the magnetization of the free layer. The state is read out by turning on the read transistor and measuring the tunneling resistance [62]. In modern technologies, different kinds of memories are used depending on the applications: Flash for storage, static/dynamic

random access memory (SRAM/DRAM) for logic operations, etc. However, adopting various memory schemes in one single chip results in increased system complexity and fabrication cost [62]. MRAM has the advantage of fast write/read speed, low power, high endurance, and most important of all, non-volatility [57], [62], [63]. It can in principle become the "universal memory", replacing SRAM/DRAM for logic operations and Flash for data storage.

While metal-based spintronics have been largely successful, the usages are rather limited to data storage purposes. Semiconductor-based spintronics, on the other hand, can in principle provide logic, communication and storage functions in one material system, greatly enhancing the functionalities of semiconductor devices [20]. Compared to metals, the spin lifetime in semiconductors is usually much longer, on the order of ms to a few hundred ns, which is more preferable for spin manipulation. However, generating non-equilibrium electron spins in semiconductors is proven to be more difficult than in metals. While both optical spin orientation [64] and spin resonance [65], [66] have been employed to create spin-polarized electrons in semiconductors, generating spin imbalance by electrical means is a preferred method for application purposes. Electrical spin injection, in which the spin accumulation is created in nonmagnetic materials by injecting spin polarized current from ferromagnetic materials, has been extensively studied in ferromagnetic/normal (*F/N*) metal junctions [67], [68]. The Datta-Das proposal of a spin-FET in turn fuels the interest in spin injection in semiconductors [25]. Two types of ferromagnetic materials have been suggested as the spin source: magnetic semiconductors and ferromagnetic metals. While using magnetic semiconductors [69] and half-metallic ferromagnet [70] can achieve high spin polarization (80%) in the normal semiconductor, this technique has only limited applications if the Curie temperature of the magnetic semiconductor cannot exceed room temperature [71], [72].

Ferromagnetic metals, such as Co, Fe and Ni, on the other hand, have significant spin polarization at room temperature. However, the *conductivity mismatch* between metal and semiconductor greatly limits the efficiency of spin injection in *F/N* contacts [73], [74]. In this chapter, we will first discuss in detail the standard model of spin injection [75], and the conditions of efficient spin injection in semiconductors [74], followed by the calculation of magnetoresistance of *F/N/F* systems with different device geometries [74]. Finally, the spin relaxation mechanisms in semiconductors will be reviewed, particularly the main spin scattering processes in germanium.

3.1. Model of Spin Injection in Semiconductors

We consider first the simplest case: a single ferromagnetic/semiconductor junction, as shown in Fig. 3-4, which has a constant current j following from F to N. We want to calculate how much spin accumulation is created in the semiconductor region due to the presence of j. The discussions below follow the approach in Ref. [75].

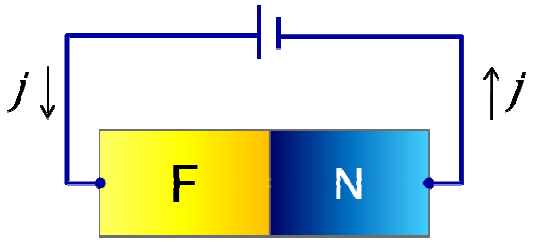


Figure 3-4. Schematic representation of a *F/N* junction.

We start by considering the difference of ferromagnetic metals and normal materials. As shown in Fig. 3-5, ferromagnetic materials have different density of states of spin up and spin down electrons, $g_{\uparrow}$ and $g_{\downarrow}$, respectively. This leads to imbalanced number of electron spins at the Fermi energy, which translates into ferromagnetism. Typical ferromagnets have a spin polarization of 10% to 50% [53]. For normal materials, the density of states for different electron spins are the same, as depicted in Fig. 3-5. In

the frame work of the two-current model, we can then consider spin-dependent conduction of electrons in either materials, defining spin-dependent current $(j_{\uparrow,\downarrow})$, chemical potential $(\mu_{\uparrow,\downarrow})$ and conductivity $(\sigma_{\uparrow,\downarrow})$. Note that for simplicity, we neglect the effects of spin mixing, which allows for current exchange in these two channels [53].

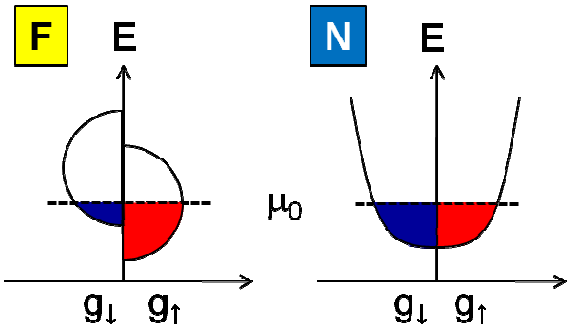


Figure 3-5. Schematic representation of the spin-dependent density of states for ferromagnetic and normal materials. Here μ_0 denotes the Fermi energy.

The current and chemical potential of each spin channel are linked via the spin-dependent conductivity by

$$j_{\uparrow,\downarrow} = \sigma_{\uparrow,\downarrow} \cdot \nabla \mu_{\uparrow,\downarrow}.$$

In the following discussions we will use subscripts of F and N to denote the corresponding values in ferromagnetic metals and normal materials, respectively. We can also define the spin polarization of a spin-dependent quantity X, as

$$P_X = \frac{X_\uparrow - X_\downarrow}{X_\uparrow + X_\downarrow},$$

in which X can be the conductivity or current, etc. The total charge current can be expressed by the sum of two spin currents

$$j = j_\uparrow + j_\downarrow,$$

while the spin current, j_s, can be expressed as the difference

$$j_s = j_\uparrow - j_\downarrow.$$

Similarly, we can define both charge (σ) and spin (σ_s) conductivities as

$$\sigma = \sigma_\uparrow + \sigma_\downarrow,$$

$$\sigma_s = \sigma_\uparrow - \sigma_\downarrow.$$

The charge and spin currents are therefore

$$j = \sigma\nabla\mu + \sigma_s\nabla\mu_s\,, \qquad (1)$$

$$j_s = \sigma_s\nabla\mu + \sigma\nabla\mu_s\,, \quad (2)$$

where

$$\mu = (\mu_\uparrow + \mu_\downarrow)/2$$

$$\mu_s = (\mu_\uparrow - \mu_\downarrow)/2$$

are the charge chemical and spin chemical potentials, respectively. In normal metals and semiconductors, $\sigma_s = 0$, and the charge and spin currents are independent. On the other hand, we can write the densities of spin-up ($n_\uparrow$) and spin-down ($n_\downarrow$) electrons as

$$n_\uparrow = n_{\uparrow 0}(\eta + e\mu_\uparrow + e\phi) \cong n_{\uparrow 0} + \frac{\partial n_{\uparrow 0}}{\partial \eta}(e\mu_\uparrow + e\phi),$$

$$n_\downarrow = n_{\downarrow 0}(\eta + e\mu_\downarrow + e\phi) \cong n_{\downarrow 0} + \frac{\partial n_{\downarrow 0}}{\partial \eta}(e\mu_\downarrow + e\phi),$$

where η is the equilibrium chemical potential, ϕ the electrostatic potential, $n_{\uparrow 0}$ and $n_{\downarrow 0}$ the spin-up and down electron densities at equilibrium chemical potential, respectively. It is also assumed here that $\mu + \phi$ is much smaller than η. Using local charge neutrality, i.e., $n_\uparrow + n_\downarrow = n_{\uparrow 0} + n_{\downarrow 0} = n_0$, we have

$$g(\mu + \phi) + g_s\mu_s = 0,$$

where

$$g = g_\uparrow + g_\downarrow$$

$$g_s = g_\uparrow - g_\downarrow.$$

We can define the spin polarization, s, as $n_\uparrow - n_\downarrow$, which becomes

$$s = n_\uparrow - n_\downarrow = (n_{\uparrow 0} - n_{\downarrow 0}) + e(g_\uparrow \mu_\downarrow - g_\downarrow \mu_\uparrow) + e g_s \phi$$

$$= s_0 + e(g\mu_s + g_s \mu) + e g_s \phi$$

$$= s_0 + 4e\mu_s \frac{g_\uparrow g_\downarrow}{g}$$

$$= s_0 + \delta s$$

where s_0 and δs are the equilibrium and accumulated spin density, respectively. For nonmagnetic materials, s_0 is zero and δs becomes $eg\mu_s$.

We are now ready to solve for μ_s, the spin accumulation chemical potential. The continuity condition for spin accumulation requires that

$$\nabla j_s = e\frac{\delta s}{\tau_s} = 4e^2 \mu_s \frac{g_\uparrow g_\downarrow}{g}\frac{1}{\tau_s}, \qquad (3)$$

where τ_s is the spin relaxation time.

From Eq. (1) and (2), the spin current can also be expressed as

$$j_s = \frac{\sigma_s}{\sigma}(j - \sigma_s \nabla \mu_s) + \sigma \nabla \mu_s$$

$$= \frac{\sigma_s}{\sigma} j + \left(\sigma - \frac{\sigma_s^2}{\sigma}\right)\nabla \mu_s$$

$$= P_\sigma j + 4\frac{\sigma_\uparrow \sigma_\downarrow}{\sigma}\nabla \mu_s$$

Taking the divergence of j_s, it reads

$$\nabla j_s = 4\frac{\sigma_\uparrow \sigma_\downarrow}{\sigma}\nabla^2 \mu_s\,, \quad (4)$$

where we used the continuity of electric current, i.e., $\nabla j = 0$.

Comparing the two expressions of ∇j_s [(3) and (4)], the spin accumulation chemical potential has the space distribution as

$$\nabla^2 \mu_s = \frac{\mu_s}{{l_s}^2},$$

where l_s is defined as the generalized spin diffusion length. The above equation can be used to describe the spin accumulation chemical potential as function of position in either ferromagnetic or normal materials.

3.1.1. Spin injection at *F/N* junction

Considering the case of *F/N* junction, such as the one in Fig. 3-1, we can to solve for the diffusion equation of μ_s in each material using proper boundary conditions. For simplicity, we consider only one dimensional case, and assume that *F* occupies the space between $x = -\infty$ to $x = 0$, and *N* extends from $x = 0$ to $x = \infty$.

The solution for μ_s in the ferromagnetic region, when considered with the boundary condition $\mu_{sF}(-\infty) = 0$, is

$$\mu_{sF}(x) = \mu_{sF}(0)e^{x/l_{sF}},$$

where the subscript *F* denotes the corresponding quantities in the ferromagnetic region. From Eq. (4), we can write P_{jF}, i.e. j_{sF}/j, as

$$\begin{aligned} P_{jF}(0) &= P_{\sigma F} + 4\frac{\sigma_{\uparrow F}\sigma_{\downarrow F}}{j\sigma_F}\nabla\mu_{sF}(0) \\ &= P_{\sigma F} + 4\frac{\sigma_{\uparrow F}\sigma_{\downarrow F}}{j\sigma_F l_{sF}}\mu_{sF}(0) \\ &= P_{\sigma F} + \frac{\mu_{sF}(0)}{jr_F} \end{aligned}$$

where r_F is defined as

$$r_F = \frac{\sigma_F}{4\sigma_{\uparrow F}\sigma_{\downarrow F}} l_{sF}.$$

r_F can be viewed as the *effective spin resistance* of the ferromagnet. Similarly, we can derive the spin accumulation chemical potential and current spin polarization in the *N* region,

$$\begin{aligned} \mu_{sN}(x) &= \mu_{sN}(0)e^{-x/l_{sN}} \\ P_{jN}(0) &= -\frac{\mu_{sN}(0)}{jr_N}. \end{aligned}$$

Here we used the boundary conditions of $\mu_{sN}(\infty) = 0$ and $P_{\sigma N} = 0$. The *effective spin resistance*, r_N, is now l_{sN}/σ_N, since the spin-up and down conductivities are the same in nonmagnetic materials.

Assuming that the spin current is conserved across the junction, i.e. $P_j = P_{jF}(0) = P_{jN}(0)$, we can solve for P_j, and it reads

$$P_j = \frac{r_F P_{\sigma F}}{r_F + r_N}.$$

This is the main result describing the spin injection efficiency of a *F/N* junction. In the case where *F* is metal and *N* is semiconductor, $\sigma_N \ll \sigma_N$, and $l_{sF} \ll l_{sN}$. The current spin polarization is then $P_j \sim (\sigma_N l_{sF})/(\sigma_F l_{sN})$, which is typically negligible. This is usually termed as the *"conductivity mismatch"* problem, since it stems from the unpaired conductivities between ferromagnetic metals and normal semiconductors.

3.1.1.1. Equivalent circuit model

The root of conductivity mismatch problem mentioned above can be more clearly appreciated if we consider the equivalent circuit model of the *F/N* junction, as shown in Fig. 3-6. The resistor network represents the effective resistances of both spin-up or spin-down channels in *F* and *N*.

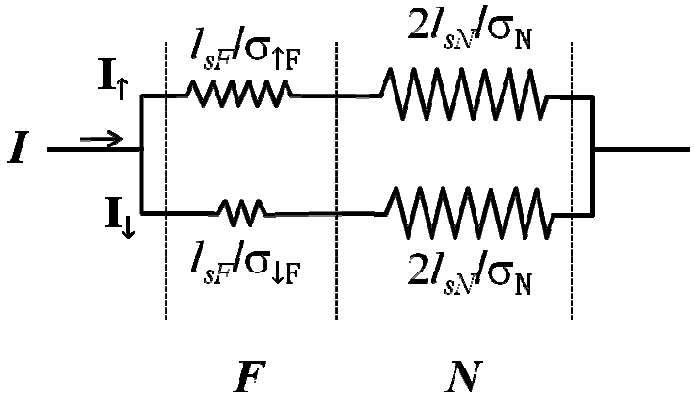


Figure 3-6. The equivalent circuit model for spin injection of *F/N* junction. Electric current flows through two channels: spin-up and spin-down. The resistors indicate the effective spin resistance of either channels in both *F* and *N*.

Standard circuit theory can be used to solve for $(I_\uparrow - I_\downarrow)/I$, the current spin polarization, and it agrees with the results derived from previous section [75]. In the framework of the circuit model, it can be noted that in the case where the effective resistance of the *N* section is much larger than its counterpart in the *F* region, the current will be distributed evenly between each spin channel, resulting in negligible spin polarization.

3.1.2. Spin injection at *F/N* junction with interface resistance

In order to achieve sizable current spin polarization at the *F/N* junction, the resistor network in Fig. 3-6 must become unbalanced. As shown in Fig. 3-7, a spin-dependent interface resistance with proper values can restore the spin injection efficiency.

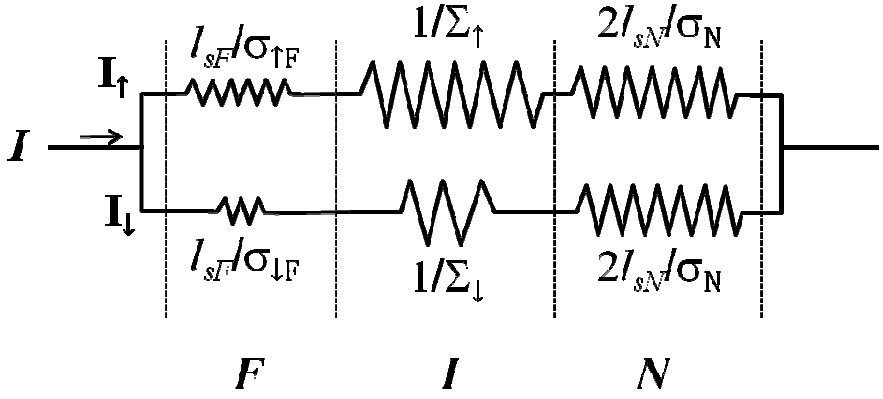


Figure 3-7. Equivalent circuit model for *F/N* junction, the interface is indicated by the *I* region. The spin-filtering nature of the contact is described by the spin-dependent conductance, $\Sigma_{\uparrow,\downarrow}$.

With the insertion of an interface layer, characterized by spin-dependent conductance $\Sigma_\uparrow$ and $\Sigma_\uparrow$, the current spin polarization becomes

$$P_j = \frac{r_F P_{\sigma F} + r_C P_\Sigma}{r_F + r_N + r_C} \qquad (5)$$

where $P_\Sigma = (\Sigma_\uparrow - \Sigma_\uparrow)/(\Sigma_\uparrow + \Sigma_\uparrow)$. The effective spin resistance of the interface, r_C, is defined as $(\Sigma_\uparrow + \Sigma_\uparrow)/(4\Sigma_\uparrow\Sigma_\uparrow)$. In the case when $r_C \gg r_F, r_N$, Eq. (5) reduces to P_Σ: the spin injection efficiency is largely determined by the interface properties.

3.1.2.1. MgO layer for spin-dependent tunneling conductance

The discussion above suggests that the insertion of spin-dependent interface resistance can overcome the conductivity mismatch problem in ferromagnetic metal/semiconductor junctions. The spin injection efficiency will depend strongly on the properties of the interface, such as the contact resistance value and spin-polarization, and have to be carefully chosen. A crystalline layer of magnesium oxide (MgO) contacted by Fe or Co is an attractive candidate, since it simultaneously provides tunable tunneling resistance and spin-filtering effect that are needed for spin injection efficiency restoration.

The research of coherent tunneling through crystalline MgO barrier has been fueled by the advances in MTJ devices. In crystalline FM(001)/MgO(001)/FM(001) structures, where FM is bcc ferromagnetic metals (e.g. Fe and Co), three kinds of evanescent states can exist in the bandgap of MgO (Δ_1, Δ_2, and Δ_5) when we consider the transport with the highest tunneling probability ($k_{||}$=0, electrons travelling perpendicular to the interface) [76], [77], as shown in Fig. 3-8. To conserve the symmetry of tunneling wave functions, the bcc FM Δ_1 Bloch states couple with MgO Δ_1 evanescent states, which is also the dominant tunneling modes [53], [76]. This can result in large spin-polarized current injected from bcc FM(001)/MgO(001) contacts.

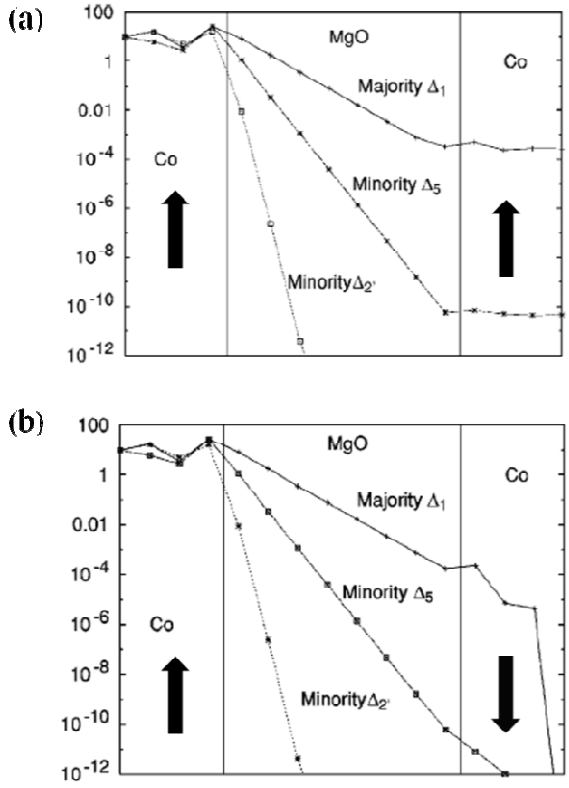


Figure 3-8. The tunneling density of states in bcc Co(100)/MgO(100)/Co(100) structures when the magnetizations of Co layers are (a) parallel and (b) anti-parallel, as indicated by the arrows. The slow-decaying tunneling channel (Δ_1) in MgO can be connected to the Bloch states of the majority spin direction subband in Co, but not to the minority one. Thus only in parallel magnetization states can the Δ_1 channel be connected by both electrodes; in the anti-parallel situation all states are completely reflected. (Figure and caption adapted from Ref. [54], [78])

3.2. MAGNETORESISTANCE AND GEOMETRY EFFECTS IN *F/N/F* STRUCTURES

Having determined the spin injection efficiency of a single *F/N* junction, we want to understand how it translates into the *magnetoresistance* of a *F/N/F* structure, as illustrated in Fig. 3-9.

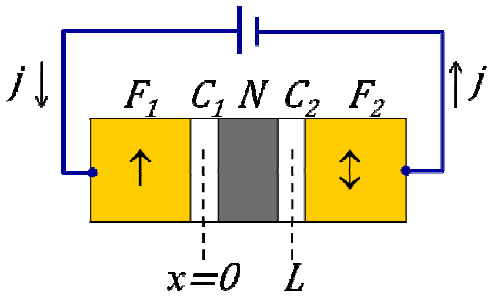


Figure 3-9. Schematic of a semiconductor region with thickness L sandwiched by two layers of ferromagnetic metals, F_1 and F_2. The magnetization of the magnets can be programmed into parallel or anti-parallel configurations by switching the magnetization of F_2. The *F/N* interface region is denoted by C_1, and C_2. Both *F* and *C* regions are assumed to be identical for simplicity.

Here a semiconductor (*N*) with a finite thickness d is sandwiched between two ferromagnetic metals with identical physical parameters. We also assume that the two *F/N* junctions are identical, with a contact resistance of r_C and a spin-polarization P_Σ. We are interested in knowing the difference of the total electrical resistance when the magnetization directions of two magnets are parallel (R_P) or anti-parallel(R_{AP}):

$$\Delta R = R_{AP} - R_P \,.$$

Using the same principles in solving for the spin injection efficiency for single *F/N* junction, we can write down the differential equations of spin accumulation to all the regions. The proper boundary conditions that ensure the continuity of spin current at both interfaces are

$$P_{jF1}(0) = P_{jC1} = P_{jN}(0)\,,$$
$$P_{jF2}(d) = P_{jC1} = P_{jN}(d)\,.$$

Assuming that the ferromagnets have a length much larger than their spin diffusion length, we can calculate the R_P of a *F/N/F* structure as,

$$R_P = 2\left(1 - {P_{\sigma F}}^2\right)r_F + r_N\frac{L}{l_{sN}} + 2\left(1 - {P_\Sigma}^2\right)r_C + 2\frac{(P_{\sigma F} - P_\Sigma)^2 r_F r_C + r_N\left({P_{\sigma F}}^2 r_F + {P_\Sigma}^2 r_C\right)\tanh\left(\frac{L}{2l_{sN}}\right)}{r_F + r_C + r_N\tanh\left(\frac{L}{2l_{sN}}\right)}$$

And the magneto-resistance is

$$\Delta R = \frac{2(P_{\sigma F}r_F + P_\Sigma r_C)^2}{(r_F + r_C)\cosh\left(\frac{L}{l_{sN}}\right) + \frac{r_N}{2}\left[1 + \left(\frac{r_C}{r_N}\right)^2\right]\sinh\left(\frac{L}{l_{sN}}\right)}$$

3.2.1. Magneto-resistance dependence on semiconductor length

Using the material parameters from cobalt [74] and germanium, we calculate the expected magneto-resistance of *F/N/F* structures as a function of semiconductor channel length and spin diffusion length. Figure 3-10 is the MR versus contact resistance with different channel lengths. The relevant parameters are $P_{\sigma F} = 0.46$, $r_F = 4.5 \times 10^{-11}$ Ω·cm^2 [74], and a semiconductor resistivity of 2 mΩ·cm, which is typical in highly doped Ge. And we have assumed a P_Σ of 0.5 and a l_{sN} of 5 μm. As expected, the maximum MR increases with decreasing semiconductor channel length. When the structure has a r_C smaller than 10^{-8} Ω·cm^2, the MR is very low. Indeed, under small r_C condition, and using the fact that $r_F \ll r_N$, the ΔR and R_P expressions above are reduced to

$$\Delta R = \frac{4{P_{\sigma F}}^2{r_F}^2}{r_N\sinh\left(\frac{L}{l_{sN}}\right)}$$

$$R_P = 2r_F + r_N\frac{L}{l_{sN}} = r_N\frac{L}{l_{sN}},$$

which leads to

$$\mathrm{MR} = {\Delta R}/{\mathrm{R_P}} = 4{P_{\sigma F}}^2\left(\frac{r_F}{r_N}\right)^2\frac{l_{sN}}{d\sinh\left(\frac{L}{l_{sN}}\right)} \approx 0$$

This result is a restatement of the conductivity mismatch problem in *F/N* junctions.

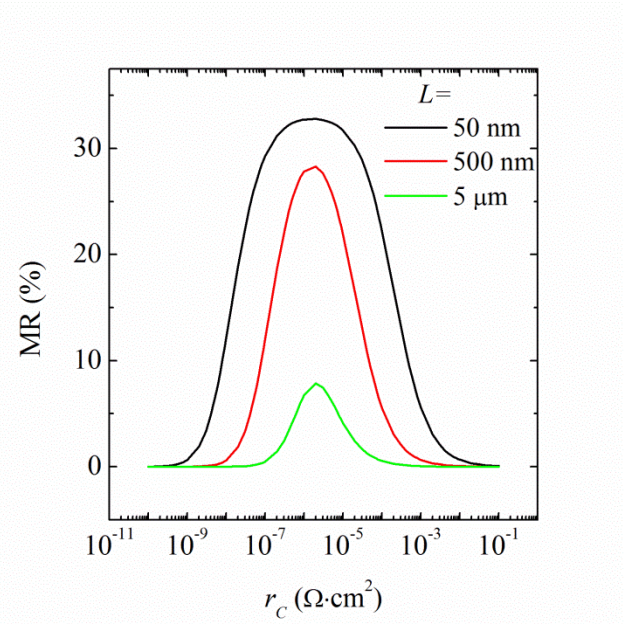


Figure 3-10. Expected magneto-resistance of a *F/N/F* structure as shown in Fig. 3-9. Cobalt and germanium parameters are used in the calculation.

As seen in Fig. 3-7, as the contact resistivity increases, the MR increases as well, until it decreases again when the contact resistivity becomes larger. This can be more clearly understood if we consider the case where $L \ll l_{sN}$, then ΔR can be expressed as

$$\Delta R = \frac{2 r_C {P_{\sigma F}}^2}{1 + r_C L/(2 r_N l_{sN})}.$$

The ΔR is maximized when $r_N l_{sN} \gg r_C L$, which, using the definition of r_N and l_{sN} as well as the Einstein relation ($\sigma_N = e^2 D_N g_N$), becomes

$$1 \gg \frac{r_C L}{r_N l_{sN}} = \frac{r_C L}{{l_{sN}}^2}\sigma_N = \frac{r_C L}{D_N \tau_{sN}} e^2 D_N g_N = e^2 L g_N \frac{1}{\tau_{sN}} \frac{1}{\Sigma_C}.$$

Here D_N is the diffusion constant, g_N the density of states, and τ_{sN} is spin relaxation time in the semiconductor, respectively. Σ_C is the conductance of the *F/N* contact, and can be expressed in terms of the tunneling probability of an electron through the interface, P_{tunnel}:

$$\Sigma_C = eLg_N P_{tunnel} = eLg_N \frac{1}{\tau_{dwell}}$$

Here τ_{dwell} is the dwell time, defined as the inverse of tunneling probability. The inequality relation then becomes

$$\frac{\tau_{sN}}{\tau_{dwell}} \gg 1$$

This expression infers that in order to achieve significant spin accumulation and MR values, the spin relaxation time of the semiconductor must be much larger than the average time electrons spent between two F/N junctions [74], [75].

3.3. Detection of Spin Accumulation in Non-local Geometry

In *F/N/F* structures, two electrodes are used for the magneto-resistance measurements, which is usually termed as *local* spin injection/detection. This scheme may not allow the decoupling of spurious effects that can prevent correct spin detection, such as Hall effect, magneto-Coulomb effect [79], and anisotropic magneto-resistance effects [80]. On the other hand, the extended geometry described in previous section enables the possibility of *direct* detection of spin accumulation. Figure 3-11 depicts the *non-local* spin injection/detection scheme, in which the spin injection and detection circuits are separated.

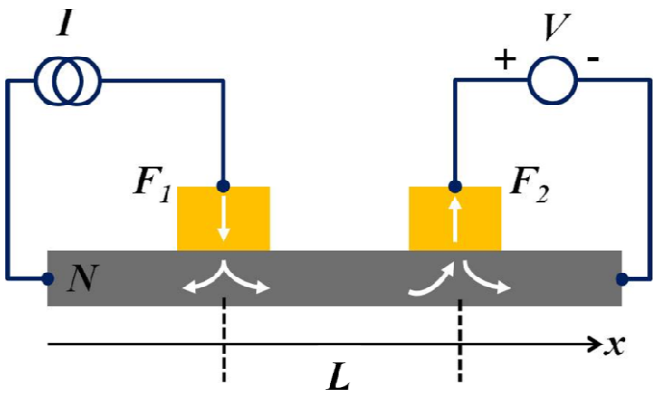


Figure 3-11. Schematic of non-local spin detection. The spin-polarized current is injected from the left-side *F* into the *N* region, and the spin current is detected from the right-hand side *F*.

In a non-local geometry, a spin-polarized charge current is sourced through a *F/N* junction, and drained away through a normal metal/N junction instead of another *F/N* junction, as shown in Fig. 3-11. The spin current, on the other hand, flows toward either directions, and the F_2/N junction is used to detect the emf it generates at the open circuit. Assuming that both ends of the *N* region extend over the spin diffusion length such that at the boundary $\mu_{sN}(\pm\infty) = 0$, and consider only the case in which the dimensions of *F/N* contacts and *N* thickness are much larger than the spin-diffusion length, we can calculate the voltage detected by the F_2/N junction. For *F/N* contacts with proper contact resistance values and significant spin injection efficiencies, the detected voltage (V_{NL}) for the F_2/N contact reads

$$V_{NL} = j\frac{r_N}{2}{P_\Sigma}^2 e^{-L/l_{sN}} .$$

Here j is the charge current density, and we assume same contact polarization (P_Σ) for both *F/N* contacts. This result indicates that the spin accumulation decays exponentially from the injected point, on the scale of l_{sN}, and is proportional to the injection current j. In the following chapter, we will present both local and non-local spin injection/detection

results in germanium nanowires. We will now discuss in more detail the mechanisms responsible for spin relaxation in semiconductors in the next section.

3.4. SPIN RELAXATION IN SEMICONDUCTORS

The spins in semiconductors interact with the environment and relax over time and distance. Historically the interest in spin relaxation in semiconductors was focused on the localized donor electrons. Electron spin resonance experiments were carried out to extract the spin relaxation rate of localized electrons in nondegenerate semiconductors at low temperatures [81], [82]. Typically the samples have low doping density (10^{13}-10^{15} cm^{-3} [81], [82]), and exhibit large resistivities (~10MΩ·cm) at low temperatures (<20 K) [81]. In this regime, the electron spin relaxes via electron-phonon Raman processes and hyperfine interaction [81], [82], and can have extremely long spin relaxation time: 10^3 s in Si [81] and 10^{-3} s in Ge [82]. However as the temperature and doping density changes, the dominant spin relaxation mechanisms might be different, resulting in very different spin lifetimes. For example, Fig. 3-12 shows the major spin relaxation processes for *n*-type silicon as a function of doping density and temperature. The spin relaxation time can vary as much as 12 orders of magnitude for Si in different relaxation regimes [83]. Earlier theoretical and experimental efforts study the relaxation physics of region 1, in which the electrons are localized. For spintronic applications that involve the transport of electrons, it is essential to understand the relaxation mechanisms of conduction electrons. In the sections below, we will discuss mainly the relaxation mechanisms relevant to conduction electrons in semiconductors.

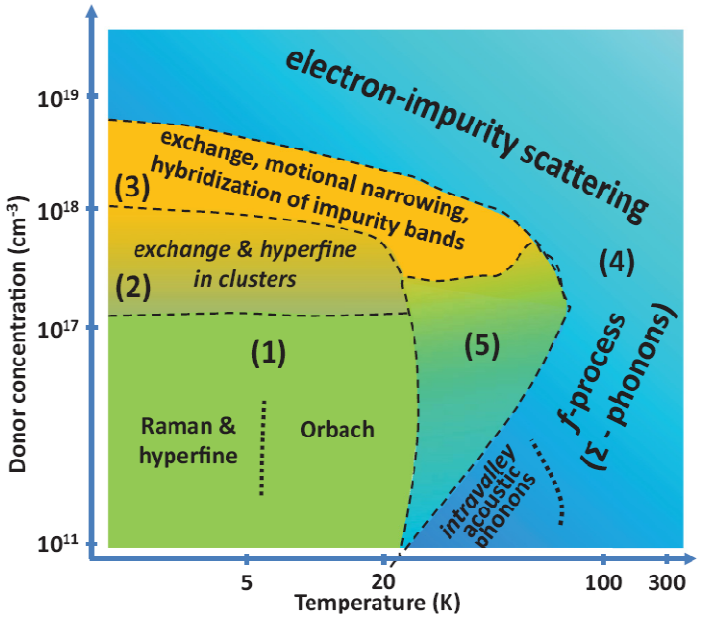


Figure 3-12. Diagram of dominant spin relaxation mechanisms in *n*-type silicon as a function of temperature and donor concentration. In region 1 electrons are localized on isolated impurity sites. In regions 4 (3) they populate the conduction (impurity) band. Region 2 is a precursor of the impurity band (donor clusters). Region 5 includes more than a single phase. (Figure and caption adapted from Ref. [83])

For conduction band electrons in group IV semiconductors, the most efficient spin interactions are spin-orbit coupling and spin-phonon interactions. Hyperfine interactions are negligible since group IV materials contain mostly zero-spin nuclear isotopes. Considering the relativistic effect of an electron moving in a potential, $V(r)$, there is an effective Hamiltonian acting on the angular momentum [19], [84]

$$H_{SO} = \frac{1}{4m_0^2c^2}\mathbf{p}\cdot[\boldsymbol{\sigma}\times\nabla V(\boldsymbol{r})]\,,$$

where m_0 is the free electron mass, c the velocity of light in vacuum, $\mathbf{p}$ the momentum of the electron, and $\boldsymbol{\sigma}$ the Pauli matrix. For semiconductors, $V(r)$ can be an applied field, the periodic potentials due to the ion core, crystal defects, and impurities. These effective fields result in spin-orbit interaction, and contribute to the most efficient spin relaxation

mechanisms in semiconductors. In the following sections, we will discuss in detail the most relevant mechanisms in group IV semiconductors: D'yakonov-Perel' [85] and Elliot-Yafet mechanisms [86], [87]. Next we will focus on the spin relaxation of conduction electrons in germanium, and present the intrinsic spin lifetime in Ge due to electron-phonon scattering.

3.4.1. D'yakonov-Perel' mechanism

In an semiconductor with space inversion asymmetry, the spin-up and spin-down electrons have different energies even they possess the same momentum (***k***) states, i.e., $\varepsilon_{k\uparrow} \neq \varepsilon_{k\downarrow}$. It is equivalent of an effective magnetic field that breaks the spin degeneracy of the *k* states,

$$H_{SO} = \frac{1}{2}\boldsymbol{\Omega}(\boldsymbol{k}) \cdot \boldsymbol{\sigma} .$$

Here $\boldsymbol{\Omega}(\boldsymbol{k})$ is the equivalent magnetic field, and an odd function of wave vector ***k*** [84]. This effective magnetic field causes the moving electron to precess at a Larmor frequency ω, which is proportional to the magnetic field, and hence ***k***. After encountering a scattering event, the electron can possess a different ***k***-state, and the precession frequency and direction changes. This causes the spin to precess randomly between adjacent scattering events, and result in spin relaxation, as illustrated in Fig. 3-13.

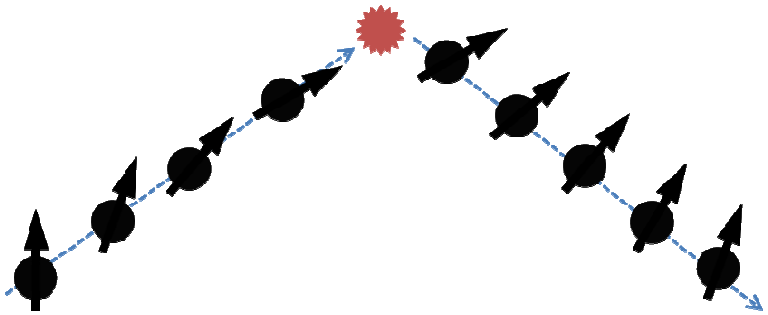


Figure 3-13. Illustration of D'yakonov-Perel' spin relaxation mechanism. The electron spin precesses at a frequency and direction depending on the momentum state. After encountering a scattering event, the momentum as well as the direction and frequency of precession changes randomly.

In strong scattering regime, i.e., the mean free path of electrons is short, and the spin relaxation time (τ_s) has the relationship with momentum scattering time (τ_p) [84],

$$\frac{1}{\tau_s} \propto \tau_p ,$$

indicating that the faster the momentum scattering, the slower the spin relaxation.

The relation between spin relaxation time and momentum scattering time can be explained by motional narrowing [53] in the weak magnetic field regime. Suppose the field has a constant magnitude but can randomly switch directions between up and down. This causes the electron spin to precess clockwise or anticlockwise randomly as well, and each step between the direction change takes time τ_p. After n steps, i.e., $t = n\tau_p$, the standard deviation of the phase will be $\omega\tau_p\sqrt{n}$. Defining the spin relaxation time is the time it takes for $\omega\tau_p\sqrt{n} = 1$, and using $\tau_s = n\tau_p$, we can obtain the $\tau_s = 1/(\omega^2\tau_p)$ [53].

D'yakonov-Perel' mechanism is the dominating spin relaxation mechanism in III-V semiconductors thanks to their noncentrosymmetric crystal structures. For group IV semiconductors, the D'yakonov-Perel' mechanism is usually negligible in bulk materials because there is no effective magnetic field due to spin-orbit coupling. However, for conduction electrons near an interface, the space inversion symmetry is lost, which can

result in another term of spin-orbit coupling [84]. Therefore the D'yakonov-Perel' mechanism may have to be considered for spins in a quantum dot, wire, or well structures.

3.4.2. Elliot-Yafet mechanism

In the presence of spin-orbit coupling induced by the lattice ions, the spin-up and down eigenstates are mixed. Assuming space inversion symmetry, the corresponding Bloch states can be expressed as [19], [84]

$$\Psi_{\boldsymbol{k}n\uparrow}(\boldsymbol{r}) = [a_{\boldsymbol{k}n}(\boldsymbol{r})|\uparrow\rangle + b_{\boldsymbol{k}n}(\boldsymbol{r})|\downarrow\rangle]e^{i\boldsymbol{k}\cdot\boldsymbol{r}}$$

$$\Psi_{\boldsymbol{k}n\downarrow}(\boldsymbol{r}) = [a^*_{-\boldsymbol{k}n}(\boldsymbol{r})|\downarrow\rangle - b^*_{-\boldsymbol{k}n}(\boldsymbol{r})|\uparrow\rangle]e^{i\boldsymbol{k}\cdot\boldsymbol{r}}$$

Here n is the band index and a and b are the complex lattice-periodic coefficients. It can be seen that the spin states are mixed, i.e., the spin-up(down) state contains a small component of the spin-down(up) state, respectively. Typically the mixing is small, with $|b| \ll 1$, and by itself does not lead to spin relaxation. However, in the presence of momentum scattering off crystal defects, impurities and phonons, spin-flip events can occur and eventually lead to spin relaxation, as shown in Fig. 3-14.

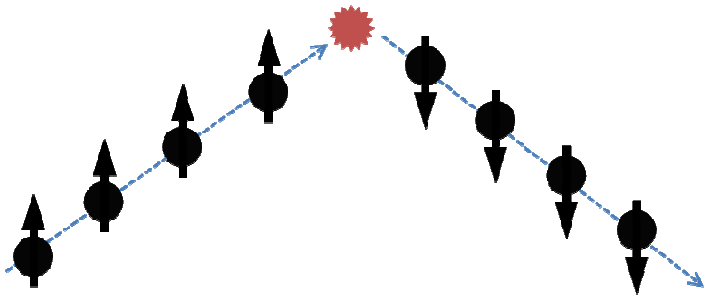


Figure 3-14. Illustration of Elliot-Yafet spin relaxation mechanism. The electron has a finite chance to undergo spin-flip process at each momentum scattering event.

The Elliot-Yafet mechanism, mediated by momentum scattering, has the relationship between spin relaxation time and momentum scattering time [84]

$$\frac{1}{\tau_s} \propto \frac{1}{\tau_p},$$

indicating that the spin relaxation rate is proportional to momentum scattering rate. Elliot-Yafet mechanism is the dominant spin relaxation process in elemental semiconductors with a center of inversion symmetry, such as silicon, germanium and carbon. In the subsections below, we discuss in more detail the spin-flip processes due to electron-phonon scattering in germanium.

3.4.3. Spin relaxation in *n*-type Germanium

There have seen increased research interest in germanium as a spintronic material, for its inversion symmetric crystal structure precludes D'yakonov-Perel' spin relaxation and their compatibility to current Si-based semiconductor industry. Moreover, compared to other group IV materials (Si and C), the lowest conduction band (*L* point) is at the edge of the Brillouin zone and is farther away from other bands, resulting in very slow intravelly spin relaxation process [88]. The dominating spin relaxation mechanism in nondegenerate Ge is therefore intervalley electron-phonon scattering.

Recently, Li *et al.* studied the intervalley spin scattering matrix elements in nondegenerate Ge [88]. Consider an electron in the conduction band with quantum numbers $\boldsymbol{k_1}$ and $\boldsymbol{s_1}$, where $\boldsymbol{k_1}$ and $\boldsymbol{s_1}$ represents the wave vector and spin state, respectively. In the case of scattering into state $|\boldsymbol{k_2}, \boldsymbol{s_2}\rangle$ with a phonon, the amplitude is

$$\begin{aligned}\langle \boldsymbol{k_2}, \boldsymbol{s_2}; n_{v,\boldsymbol{q}} \pm 1 | \mathcal{H}^{v}_{ep}(\boldsymbol{q}) | \boldsymbol{k_1}, \boldsymbol{s_1}; n_{v,\boldsymbol{q}} \rangle \\ = -\sqrt{\frac{\hbar^2}{2\varrho\Omega_{v,\boldsymbol{q}}V}} \sqrt{n_{v,\boldsymbol{q}} + \frac{1}{2} \pm \frac{1}{2}} \cdot \boldsymbol{M}_v(\boldsymbol{k_1}, \boldsymbol{s_1}; \boldsymbol{k_2}, \boldsymbol{s_2}) .\end{aligned}$$

Here $\mathcal{H}_{ep}^{v}$ denotes the Hamiltonian for electron-phonon scattering, $n_{v,\boldsymbol{q}}$ the phonon occupation number, v the phonon mode and $\boldsymbol{q} = \boldsymbol{k_2} - \boldsymbol{k_1}$ the phonon wave vector. $\Omega_{v,\boldsymbol{q}}$, ϱ, and V are the phonon energy, density of Ge, and volume, respectively. $\boldsymbol{M}_v(\boldsymbol{k_1}, \boldsymbol{s_1}; \boldsymbol{k_2}, \boldsymbol{s_2})$ is the matrix elements for intervalley electron-phonon scattering, which reads

$$\boldsymbol{M}_v(\boldsymbol{k_1}, \boldsymbol{s_1}; \boldsymbol{k_2}, \boldsymbol{s_2}) = \sum_{j,\alpha} \boldsymbol{\xi}_{\alpha,v}(\boldsymbol{q}) e^{i\boldsymbol{q}\boldsymbol{R}_{j\alpha}} \langle \boldsymbol{k_2}, \boldsymbol{s_2} | \nabla_{\mathrm{r}} \mathcal{V}_{at}(\boldsymbol{r} - \boldsymbol{R}_{j\alpha}) | \boldsymbol{k_1}, \boldsymbol{s_1} \rangle.$$

Here j sums over the N primitive cells and α sums over the atoms in a primitive cell. The atom position is represented by $\boldsymbol{R}_{j\alpha}$, and the mode-dependent displacement vector by $\boldsymbol{\xi}_{\boldsymbol{\alpha},\boldsymbol{v}}$. The potential, $\mathcal{V}_{at}$, includes the periodic potential formed by crystal atoms and the spin-orbit coupling, $\frac{\hbar}{4m_0^2c^2}[\nabla V_{at}(\boldsymbol{r}) \times \mathbf{p}] \cdot \boldsymbol{\sigma}$. For spin flipping events, $\boldsymbol{s_2} = -\boldsymbol{s_1}$, and the corresponding spin relaxation rate is

$$\frac{1}{\tau_{s,v}} = \frac{2\pi\hbar}{\varrho N_c} \int d^3\boldsymbol{k_1} \frac{\partial f(E_{\boldsymbol{k_1}})}{\partial E_{\boldsymbol{k_1}}} \int \frac{d^3\boldsymbol{k_2}}{(2\pi)^3} \frac{|\boldsymbol{M}_v(\boldsymbol{k_1}, \boldsymbol{s}; \boldsymbol{k_2}, -\boldsymbol{s})|^2}{\Omega_v(\boldsymbol{q})} \cdot \sum_{\pm} \left(n_{v,\boldsymbol{q}} + \frac{1}{2} \pm \frac{1}{2} \right) \delta(E_{\boldsymbol{k_2}} - E_{\boldsymbol{k_1}} \pm \Omega_{v,\boldsymbol{q}}).$$

Here N_c is the density of states and $f(E_{\boldsymbol{k}})$ the distribution of electronic states. Finding out the value of the matrix elements $\boldsymbol{M}_v(\boldsymbol{k_1}, \boldsymbol{s}; \boldsymbol{k_2}, -\boldsymbol{s})$ is the most crucial part to determine the spin relaxation rate. In Ge, the thermal electrons are located at the four valleys in which the center of each valley is at the L points, the edge of the Brillouin zone [Fig. 3-15(a)] [88]. Six intervalley scattering are possible, with one indicated by the $\mathbf{q}_{001}$ vector. These transitions are mediated by absorbing or emitting phonons near the X point, as shown in Fig. 3-15(b).

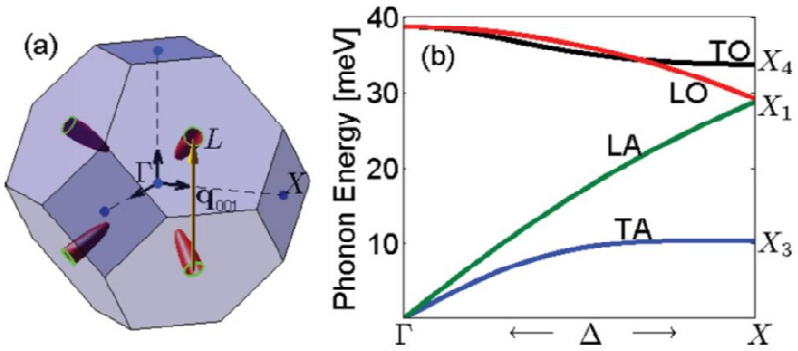
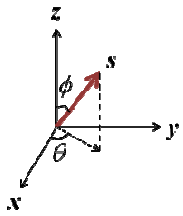


Figure 3-15. Electron-phonon scattering in germanium. (a) The four conduction band valleys, with the centers located at the *L* points in the Brillouin zone. One of the six possible intervalley transitions is indicated by the $\mathbf{q}_{001}$ vector. (b) Phonon dispersion in germanium along the dashed line in (a), i.e., the Γ–Δ–X direction. The symmetries and modes of the X phonon are noted in the figure. (Figure and text adapted from [88])

The matrix elements $\boldsymbol{M_v(k_1, s; k_2, -s)}$ of intervalley scattering can be computed using group theory and selection rules, and the square of the amplitude for all six possible spin-flipping transitions are shown in Table 3-1. Here the spin direction $\hat{\boldsymbol{s}}$ is described by (θ, ϕ), in which θ is the angle between $\hat{\boldsymbol{s}}$ and $+\hat{\boldsymbol{z}}$ and ϕ is the azimuthal angle in the xy-plane measured from $+\hat{\boldsymbol{x}}$.



$L \leftrightarrow L_t$	X_1	X_4
$L_{111} \leftrightarrow L_{11\bar{1}}$	$1+\cos^2\theta+\sin^2\theta\sin 2\phi$	$1-\cos^2\theta$
$L_{111} \leftrightarrow L_{1\bar{1}1}$	$1+\sin^2\theta\sin^2\phi+\sin 2\theta\cos\phi$	$1-\sin^2\theta\sin^2\phi$
$L_{111} \leftrightarrow L_{\bar{1}11}$	$1+\sin^2\theta\cos^2\phi+\sin 2\theta\sin\phi$	$1-\sin^2\theta\cos^2\phi$
$L_{\bar{1}11} \leftrightarrow L_{11\bar{1}}$	$1+\sin^2\theta\sin^2\phi-\sin 2\theta\cos\phi$	$1-\sin^2\theta\sin^2\phi$
$L_{\bar{1}11} \leftrightarrow L_{1\bar{1}1}$	$1+\cos^2\theta-\sin^2\theta\sin 2\phi$	$1-\cos^2\theta$
$L_{1\bar{1}1} \leftrightarrow L_{11\bar{1}}$	$1+\sin^2\theta\cos^2\phi-\sin 2\theta\sin\phi$	$1-\sin^2\theta\cos^2\phi$

Table 3-1. The matrix elements of intervalley spin-flip scattering for all six possible transitions. The X_1 and X_4 columns indicate either the X_1 or X_4 phonons are involved in the process, respectively. All values should be multiplied by the square of the corresponding deformation potentials, i.e., $D_{X_i}^2$, for i=1 or 4. The coordinates are shown in the figure to the left. (Table and text adapted from [88])

The spin relaxation rate due to intervalley scattering in unstrained, bulk germanium is then [88]

$$\frac{1}{\tau_s}=\frac{4}{3}\left(\frac{2m_d}{\pi}\right)^{\frac{3}{2}}\left[\frac{8D_{X_1}^2}{\hbar^2\varrho\sqrt{\Omega_1}}\frac{\vartheta\left(\frac{\Omega_1}{k_BT}\right)}{e^{\frac{\Omega_1}{k_BT}}-1}+\frac{4D_{X_4}^2}{\hbar^2\varrho\sqrt{\Omega_4}}\frac{\vartheta\left(\frac{\Omega_4}{k_BT}\right)}{e^{\frac{\Omega_4}{k_BT}}-1}\right],$$

where m_d is the effective electron mass (0.22m_e), and $\vartheta\left(\frac{\Omega_i}{k_BT}\right)$ is associated with the Bessel function of the second kind. The multiplying factors before $D_{X_i}^2$ (8 and 4 for i=1 and 4, respectively) are the summation of all terms in the X_i column in Table 3-1, and are independent of the spin orientation. With the knowledge of the deformation potentials (35 meV/Å and 46 meV/Å for X_1 and X_4 phonon modes, respectively), the intrinsic spin relaxation time can be readily calculated, as shown in the solid curve in Fig. 3-16 [88].

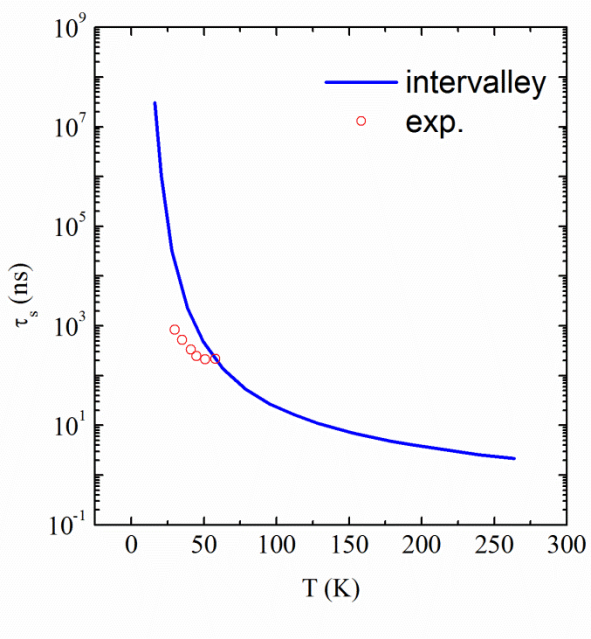


Figure 3-16. Spin relaxation time of conduction electrons in bulk, unstrained Ge. The theoretical values are calculated by considering intervalley scattering only [88], while the experimental values are obtained through spin transport measurements in long-distance germanium spin-valves [89]. (Figure and text adapted from Ref. [88], [89])

As temperature lowers, the population of phonons decreases, resulting in fewer spin-flipping events and longer spin relaxation time. Recently spin transport in vertical spin-valves utilizing hot electron spin injection in Ge is demonstrated [89], and the spin relaxation time for a temperature range between 30 K and 60 K are obtained, as shown in Fig. 3-16. The extracted spin relaxation time matches theoretical calculations well near 60 K, but deviates increasingly from the calculations as the temperature decreases. This suggests that while intervalley scattering is the dominating spin relaxation mechanism at high temperatures, other spin scattering processes become more important as intervalley scattering is suppressed at low temperatures. These mechanisms may include intravalley scattering, electron-impurity scattering, etc.

3.4.3.1. Spin relaxation due to intravalley scattering

Intravalley scattering describes the electron-phonon scattering events in which the initial and final states of the electrons are within the same valley. For Ge, due to the space-inversion and time-reversal symmetries of the electrons in the *L* valley, this effect is relatively weak compared to intervalley scattering [87], [88]. Recently Li *et al.* studied the intravalley spin scattering matrix elements by deriving a spin-dependent **k·p** Hamiltonian at the vicinity of the *L* point [88]. They found that the intravalley scattering is anisotropic, and much slower than intervalley scattering. Figure 3-17 is a reproduction of Fig. 3-16, with the addition of the intrinsic spin relaxation time due to *intravalley* scattering (red curve) [88]. The intravalley scattering is about two orders slower than that of intervalley scattering at high temperatures, and becomes more important when crystal temperature is lower than 20 K. Remarkably, if intervalley scattering can be quenched, the spin relaxation time is predicted to reach 1 μs at room temperature [88], as discussed in the next section.

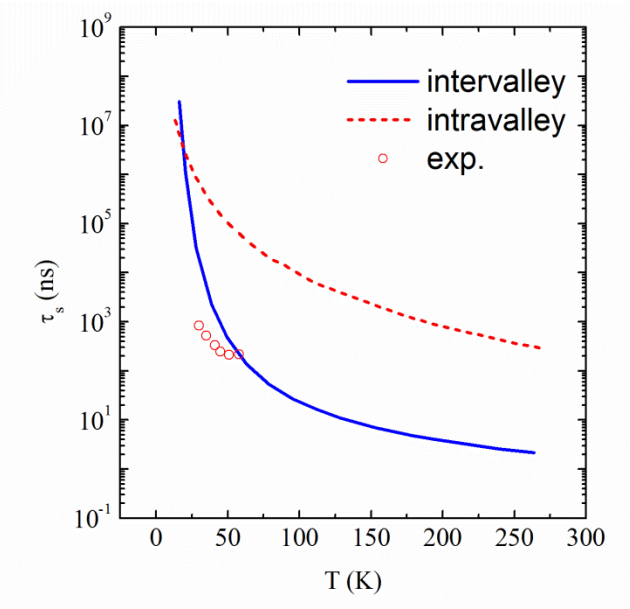


Figure 3-17. The intrinsic spin relaxation time of intervalley and intravalley scattering, and experimental results. The intravalley scattering is calculated for L_{111} valley, and assuming a spin orientation along the **z** axis. Figure and caption adapted from Ref. [88].

3.4.3.2. Effects of strain on spin scattering and anisotropy

In Table 3-1 it is clear that the spin-flipping scattering is dependent on the spin orientation $\hat{\boldsymbol{s}}$. In bulk Ge, the four L valleys are degenerate and all six transitions are equally possible, resulting in isotropic spin relaxation. However, if the degeneracy is lifted, for example by strain, geometry confinement, or in the presence of an electric field, the spin relaxation rate could become anisotropic.

For instance, in the case of [111] uniaxial *compressive* strain, the L valleys split into one low-energy valley and three high-energy valleys. At a strain level of 1%, the energy separation is 0.16 eV [90]. This energy difference can effectively suppress all intervalley scattering processes, leaving intravalley scattering the dominant spin relaxation mechanism [88], [90]. Since the intravalley scattering is two orders of magnitude slower than intervalley scattering, the spin relaxation can be significantly

prolonged at room temperature [88]. However, in the case of [111] uniaxial *tensile* strain, three valleys shift down and one valley shifts up in energy. Intervalley scattering is still present among the three low-energy valleys, but now the multiplying factors of $D_{X_i}^2$, instead of being 8 and 4, are $[16 - 4\sin^2\theta \sin 2\phi - 4\sin 2\theta\,(\sin\phi + \cos\phi)]/3$ and $8/3$, respectively [88]. The spin relaxation time is now dependent on the spin orientation $\hat{\boldsymbol{s}}$.

3.4.4. Possible spin relaxation mechanisms in highly-doped Ge nanowires

In the next chapter the experimental results of spin injection in lateral Ge nanowires (NWs) will be presented. It is of merit to discuss possible spin relaxation mechanisms in this material platform besides the aforementioned intervalley and intravalley scattering. Since the NWs investigated in this study are highly doped with phosphorous, electron-impurity scattering is expected to be present. At low temperatures, while intervalley scattering is quenched, scattering off impurities can become an important spin relaxation mechanism [83]. On the other hand, although D'yakonov-Perel' spin relaxation is typically ignored in group IV materials, it could be of impact in NWs since the inversion symmetry is broken at the NW interface [84].

3.5. SUMMARY

In this chapter the standard model of spin injection is presented. The conductivity mismatch between ferromagnetic metals and semiconductors is realized to be the fundamental problem impeding efficient spin injection in *F/N* structures. With the insertion of a spin-dependent contact resistance between the *F/N* interface, the spin injection efficiency hence the magnetoresistance of a *F/N/F* structure can be restored. The technique of nonlocal spin injection/detection is also described.

Elliot-Yafet mechanism is identified to be the dominating spin relaxation process in group IV semiconductors, thanks to the space inversion symmetry in the diamond crystal structure that suppresses the D'yakonov-Perel' mechanism. Spin relaxation in Ge mediated by intervalley electro-phonon scattering is discussed and compared with that of intravalley scattering. A recent experimental result is compared with theoretical calculations and is of excellent agreement at 60 K. It is predicted that if intervalley scattering can be quenched by lifting the degeneracy of the *L* valleys, the spin relaxation time in Ge can increase by two orders of magnitude.

Chapter 4: Spin injection in Germanium Nanowires

In this chapter we demonstrate the electrical spin injection in Ge NWs. First the growth and characterization of phosphorous-doped Ge NWs will be presented, followed by detailed fabrication processes of Ge NW spin-valves. We will also discuss the various design aspects of the spin-valve devices, namely the choice of tunnel barrier and the realization of different magnetization configurations in the spin-valves. Next we show the experimental results of both local and nonlocal spin-valve effect, which can be explained by spin accumulation in the Ge NWs. Using data measured from over hundred samples, we map out the contact resistance window for which lateral spin transport is observed, manifestly showing the conductivity matching required for spin injection. Our analysis, based on the spin diffusion theory, indicates that the spin diffusion length is larger than 100 μm in germanium nanowires at 4.2K. Finally we will discuss the impact of contact magnetization uniformity and tunnel barrier crystallinity in the strength of spin accumulation signal.

4.1. Growth of highly-doped n-type Ge NWs

The P-doped Ge NWs are grown via the VLS mechanism, in a cold-wall UHV-CVD chamber, as described in chapter 2. Here both GeH_4 (20% dilution in helium) and PH_3 (100ppm dilution) are used as precursors for the growth. Due to different precursor decomposition rates at the liquid catalyst and solid NW interface, Ge NWs grown in presence of PH_3 have an undoped core, surrounded by a P-doped shell [91], [92]. In order to understand the incorporation rate of P-atoms and the doping density, we carried out two growths, differing in growth pressures and gas flow rates. The growth parameters are summarized in Table 4-1.

		NW054_ Ge003	NW082_ Ge004
Gas flow rate (sccm)	**GeH_4**	50	100
	PH_3	10	10
Pressure (Torr)		2.5	5
Temperature (°C)		300	290
Duration (min)		90	90
Diameter (nm)		20 (tip) -75 (base)	30 (tip) -90 (base)
Length (μm)		5.2	11.4

Table 4-1. Summary of P-doped Ge NWs growth.

In both growths depicted in Table 4-1, the chamber is first held at 1 Torr for 15 min in order for the nucleation of NWs to occur. The pressure is subsequently increased to higher pressures during the main growth sequence. In both cases, the resulting NWs are epitaxial to the substrate, and have small tapering from tip to base.

4.1.1. Doping Density of P-doped Ge NWs

Next we study the electrical properties and doping density of the grown NWs. The NWs are first harvested onto a 25 nm-thick SiO_2 film, thermally grown on a heavily doped p-type Si substrate, which serves as the back-gate for all devices. The NWs are fabricated into multi-terminal NW field-effect transistors (FETs) with various channel lengths (L), using e-beam lithography, cobalt (Co) evaporation and liftoff [Fig. 4-1(a)]. Prior to Co deposition, the sample is treated with a short dilute HF dip to remove the

native oxide. A 10 nm-thick gold film is deposited on top of Co to prevent post-processing oxidation.

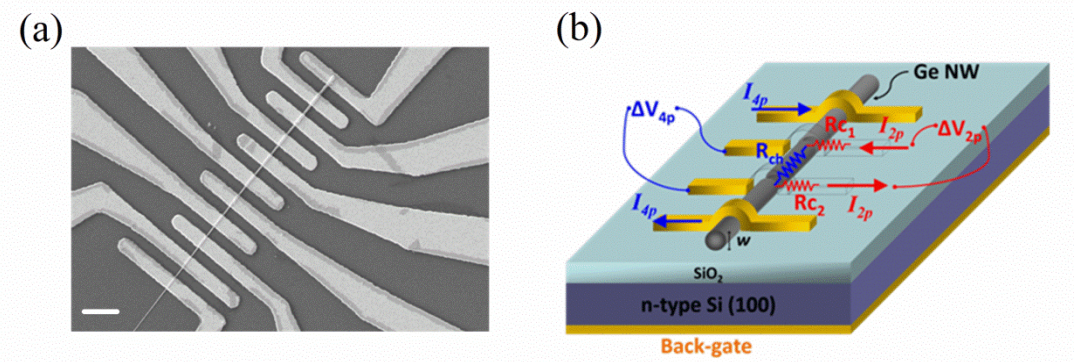


Figure 4-1. Test structure used to characterize the P-doped Ge NWs. (a) SEM of a back-gated, multi-terminal Ge NW FET. Scale bar is 1 μm. (b) Two-point (2p) and four-point (4p) measurement scheme. The intrinsic channel resistance (R_{ch}) is obtained through 4p-measurement, and the total resistance (R_c) is the difference between R_{4p} and R_{2p}.

We use both two-point (2p) and four-point (4p) measurements to determine the NW resistance and metal/NW contact resistance (R_c), as shown in Fig. 4-1(b). The intrinsic NW conductance (G) is defined as $G = 1/R_{4p} = I_{4p}/\Delta V_{4p}$. An example of two-point and four-point current (I) vs. voltage (V) data as a function of back-gated voltages (V_{BG}) is shown in Fig. 4-2(a). Both NW054-Ge003 and NW082-Ge004 shows intrinsic NW resistivities (ρ_s), defined as $R_{4p}\pi r^2/L$, as low as a few mΩ-cm. However the typical NW length of NW054-Ge003 is only 5μm, which is too short for multi-terminal device structure that will be implemented in the spin-valve devices. Therefore NW082-Ge004 will be the primary source of NWs used in the device fabrication and characterization presented in later sections.

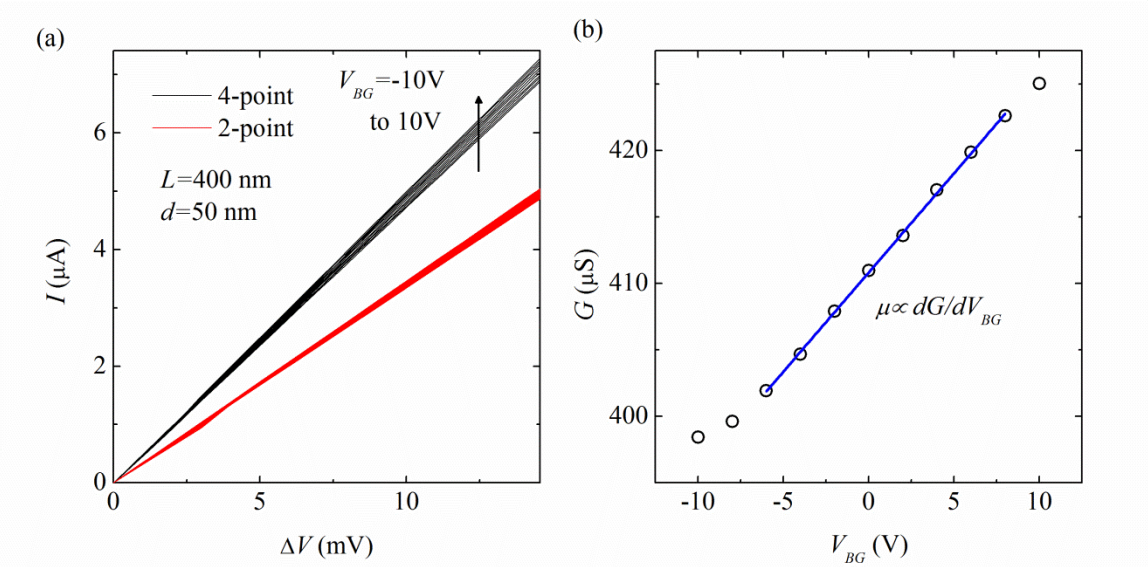


Figure 4-2. Electrical properties of phosphorous-doped Ge NWs. (a) Four-point and two-point *I-V* characteristics of a Ge NW FET, measured for V_{BG} = 10V to -10V in 2V step. (b) G vs. V_{BG} data, in which the field-effect mobility can be extracted from dG/dV_{BG}. (NW source: NW082_Ge004)

Figure 4-2(b) plots the conductance versus back-gate voltage. The electron mobility, μ, is proportional to the slope, dG/dV_{BG}, and can be extracted using $\mu = {C_{ox}}^{-1} \cdot d(G \cdot L)/dV_{BG}$. Here C_{ox} is the back-gate to NW capacitance per unit length calculated using self-consistent numerical simulations (Sentaurus), which ranges between 74 and 91 aF/μm for d values between 41 and 70 nm. The extracted mobility in our NWs is 70±20 $cm^2(V \cdot s)^{-1}$. The doping concentration (n) can be then be extracted from $(G \cdot L)|_{V_{bg}=0} = \pi e \mu n d^2/4$. Figure 4-3 shows the NW conductance-channel length product, measured at a temperature T = 4.2 K, plotted versus the NW diameter (d) square. The linear dependence of these two quantities indicates that the doping density is constant for the diameter range investigated. The doping concentration of the P-doped NWs is $5\pm2\times10^{19}$ cm^{-3}.

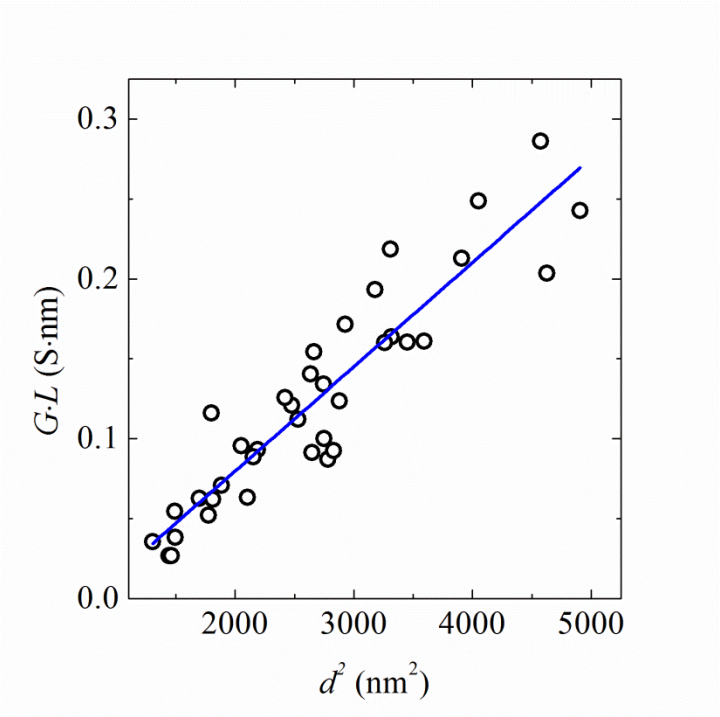


Figure 4-3. Conductance-channel length product of back-gated, P-doped Ge NW FETs. The linear dependence on the square of diameter suggests that the NW doping density is constant along the NW axial direction in the diameter range probed here.

4.1.2. Metal-NW contact resistivity

The R_c values for our Ge NWs with Co contacts, extracted from $(R_{2p} - R_{4p})/2$, are 300±100 Ω. We employ the transmission line model (TLM), which takes into account the geometry of NWs, to accurately obtain the specific contact resistance, ρ_c.

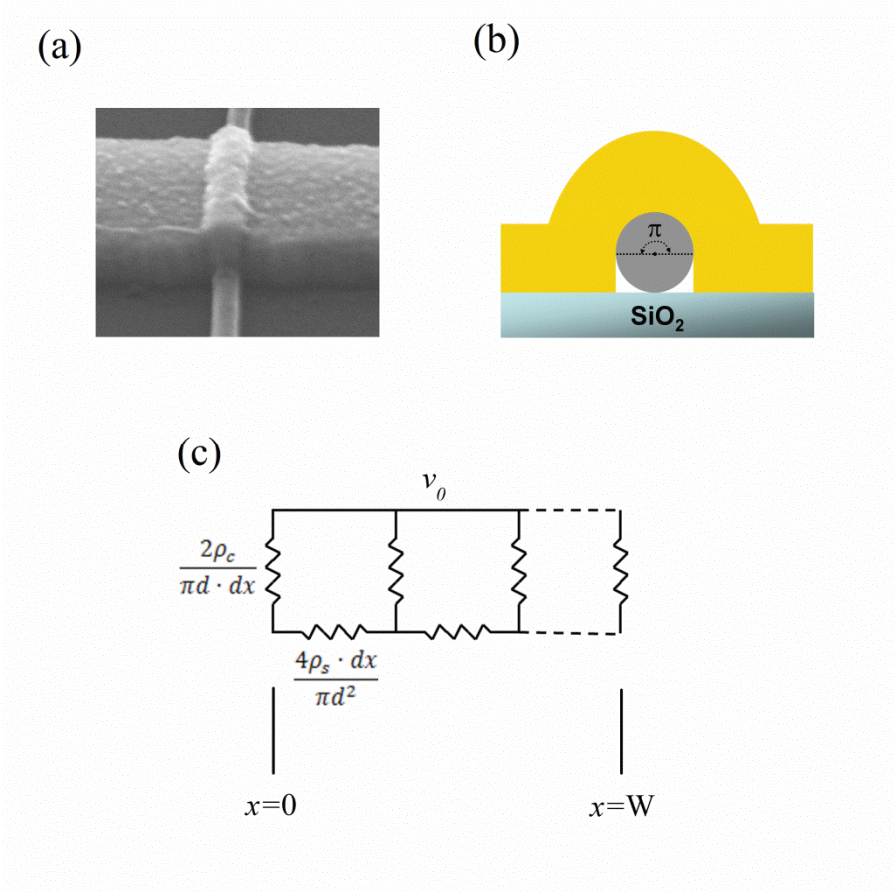


Figure 4-4. Transmission line model for specific contact resistance extraction. (a) SEM image showing a typical metal-to-NW contact. (b) Schematic of the coverage of evaporated metal on a NW. Here we assume that only the top half of the NW is in contact with the metal. (c) Transmission line model for a metal-NW contact with length W.

The SEM image in Fig. 4-4(a) represents a typical metal-NW contact with e-beam evaporated metal. It can be seen that not the entire circumference of NW is in direct contact with the metal. Here we assume that the metal only contacts the top section of the NW, as shown schematically in Fig. 4-4(b). We then use the transmission line model [Fig. 4-4(c)] to describe the current distribution of a metal-NW contact with length W. Here v_0 is the voltage applied to the contact, ρ_s the NW resistivity, and d the NW

diameter. The voltage and current at position x in the NW is $V(x)$ and $I(x)$, respectively, and the current flows from $x=0$ to $x=W$. The voltage drop at each infinitesimal dx is then

$$dV = -\frac{4\rho_s}{\pi d^2} dx \cdot I$$

And the current difference between $I(x)$ and $I(x+dx)$ is

$$dI = \frac{v_0 - V}{2\rho_c/(\pi d \cdot dx)} = \left(\pi d \frac{v_0 - V}{2\rho_c}\right) dx$$

Rewriting the above equations, we have

$$\frac{dV}{dx} = -\frac{4\rho_s}{\pi d^2} I$$

$$\frac{dI}{dx} = \frac{\pi d}{2\rho_c}(v_0 - V)$$

Combining these two, we then have

$$\frac{d^2 I}{dx^2} = \frac{\pi d}{2\rho_c}\left(-\frac{dV}{dx}\right) = \frac{2\rho_s}{\rho_c d} I$$

Solving for $I(x)$ and using the boundary conditions $I(0)=0$ and $I(W)=i_0$, we have

$$I(x) = i_0 \frac{\sinh(x/L_T)}{\sinh(W/L_T)}$$

where the transfer length L_T is defined as

$$L_T = \sqrt{\frac{d\rho_c}{2\rho_s}}$$

The voltage is then

$$V(x) = v_0 - \frac{2\rho_c i_0}{\pi d L_T} \frac{\cosh(x/L_T)}{\sinh(W/L_T)}$$

Using boundary condition $V(W)=0$, we can get

$$v_0 = \frac{2\rho_c i_0}{\pi d L_T} \coth(W/L_T)$$

$$R_c \equiv \frac{v_0}{i_0} = \frac{2\rho_c}{\pi d L_T} \coth(W/L_T) = \frac{4\rho_s L_T}{\pi d^2} \coth(W/L_T)$$

By experimentally measuring R_c, ρ_s, d, and W, the L_T, hence ρ_c, can be determined unambiguously. We calculate a specific contact resistance of $1.8\pm1.6\times10^{-8}$ $\Omega\cdot cm^2$ for Co contacts, which is the record low value for metal contacts on n-type Ge [93]–[95]. The contact resistance to n-type Ge is typically large, and has been usually attributed to the Fermi level being pinned near the valence band and inefficient n-type dopant activation in Ge, resulting in a large Schottky barrier height and contact resistance [38], [95], [96]. Our results suggest that using highly doped n-type Ge ($n=5\pm2\times10^{19}$ cm^{-3}), the Schottky barrier width becomes narrow and electron tunneling through the barrier is more efficient, reducing the metal-Ge contact resistance. The low contact resistances between Co and the Ge NWs allows for interface resistance engineering to overcome the conductivity mismatch problem stated previously in Chapter 3.

4.2. Fabrication of Ge NW spin-valves

Having grown highly-doped, phosphorous-doped Ge NWs and realized low Co/NW contact resistances, we discuss here the process flow and design rules for Ge NW spin-valve devices. Below in Fig. 4-5 is the schematic of the NW spin-valve device. The fabrication process is similar to those of previously described multi-terminal devices, except that here a thin layer of MgO is deposited between the NW and Co by e-beam evaporation. Besides, the electrodes are designed to have different widths such that the magnetization can be tuned individually. In the sections below we discuss in more detail the methods of MgO deposition and the layer quality, as well as the considerations for the contact width.

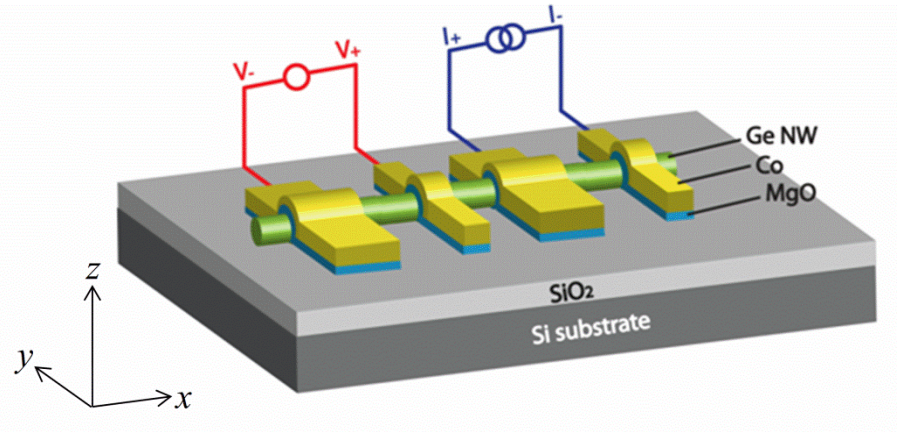


Figure 4-5. Schematic of NW spin-valve device, featuring MgO tunnel barrier and multi-terminal structure.

4.2.1. Tunnel barrier formation

As discussed in the chapter 3, in order to restore spin polarization in the semiconductor, an interfacial resistance with spin-polarization is needed at the metal/semiconductor interface. Magnesium oxide (MgO) has a large band gap (7.8 eV [97]), and exhibits spin-dependent tunneling when contacted with bcc FM, therefore can serve as an ideal tunnel barrier for metal/semiconductor interface.

Magnesium oxide can be grown by several techniques, including sputtering, atomic-layer-deposition, and e-beam evaporation. Epitaxial MgO has been achieved in *F*/MgO/*F* magnetic tunnel junctions (MTJs) by sputtering techniques [98], [99]. Multi-layer structures of FM's and MgO are usually deposited *in situ* using conventional radio-frequency (RF) sputtering techniques, and are subsequently fabricated into spin-valve devices. However, sputtering deposition might cause plasma-induced damage to the semiconductor [100], [101], and is therefore not suitable for tunnel barrier deposition on NWs. Atomic layer deposition (ALD) of MgO has also been proposed, using sequential exposures of bis(ethylcyclopentadienyl)magnesium [$Mg(CpEt)_2$] and H_2O [102]. It has the advantages of well-controlled growth rate and good conformality over structures with

high aspect ratio. However, the *F* layers must be deposited *ex situ*, which increases the possibility of interface contamination. Evaporation techniques, such as molecular beam epitaxy (MBE) or e-beam evaporation, on the other hand, are capable of depositing both *F* layers and MgO *in situ*, and are relatively damage-less processes. Indeed, magnetoresistance ratio of a MTJ as large as 410% at room temperature has been demonstrated using MgO grown by MBE as the tunnel barrier, featuring fully epitaxial MgO(001) on Co(001) [60]. In this study, we choose to deposit MgO by e-beam evaporation under high-vacuum, room-temperature conditions. Below we present the properties of the tunneling *F*/MgO/NW contacts, including surface roughness, tunnel-barrier uniformity and temperature dependence.

4.2.1.1. Surface roughness

The MgO is deposited on a Si (100) wafer, using stoichiometric, amorphous MgO source in a CHA 4-pocket e-beam evaporation tool (SEC 1000 RAP), at room temperature and with a base pressure of 5×10^{-6} Torr. The deposition rate is less than 0.1 Å/s. Prior to loading, the wafer is treated with HF to remove native oxide. The final thickness (100 Å) is confirmed using a spectroscopic ellipsometry. The sample is then scanned in an atomic force microscope (AFM), as shown in Fig. 4-6. The surface is relatively flat, with a roughness measure of 0.2 nm. This ensures that the current injection through the tunnel barrier is uniform and does not crowd into pin holes.

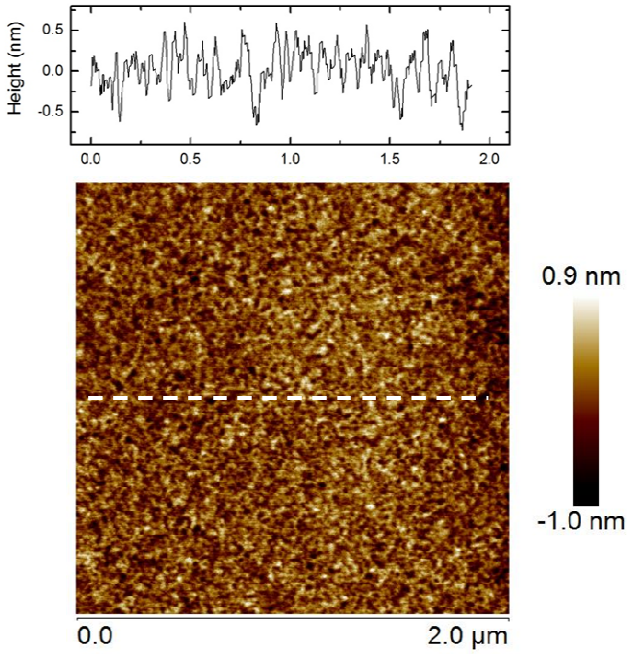


Figure 4-6. AFM image of evaporated MgO on Si (111) surface. The surface roughness is 0.2 nm. A surface profile (top) is taken along the dashed white line.

4.2.1.2. Tunnel barrier quality

To prove the current injection mechanism through the contacts, we fabricated a test structure to assess the tunnel barrier quality of MgO, as shown in Fig. 4-7. The first half of the device fabrication process is similar to that described in the previous section: NW dispersion, followed by EBL and Ni lift-off. Here Ni is directly deposited onto the NW, which serves as the ohmic contact. The device subsequently went through another EBL and Co lift-off process, but a thin layer of MgO (12 Å) is evaporated onto the NW before Co deposition. This contact will serve as the tunneling contact of the device. Temperature-dependent *I-V* measurements are performed between each adjacent Ni-Co/MgO contacts to characterize the tunnel barrier properties (Fig. 4-8). The *I-V* curves exhibit non-linear characteristics, in which the current increases exponentially with voltage. In addition, the *I-V* shows only weak temperature dependence. These signatures

suggest that in this device, tunneling through the MgO barrier is the main current injection mechanism.

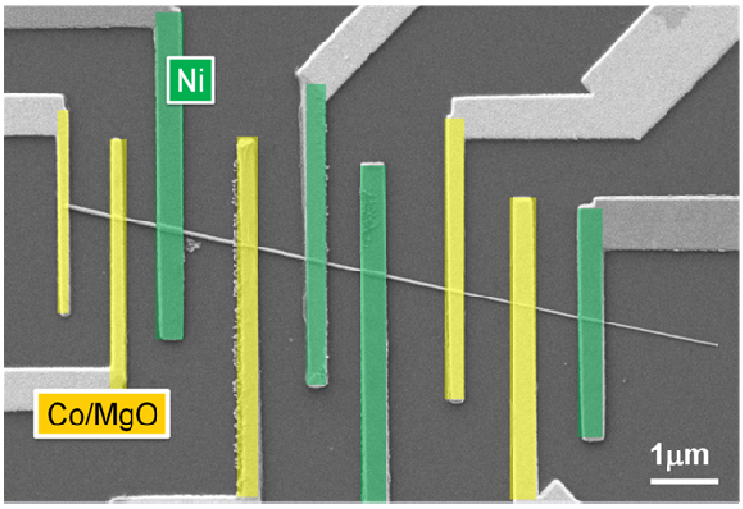


Figure 4-7. Test structure for Co/MgO/NW tunnel barrier assessment. Two kinds of contacts are formed on the NW: the tunneling (yellow) contact by Co/MgO and the ohmic (green) contact by Ni. (NW source: NW082_Ge004)

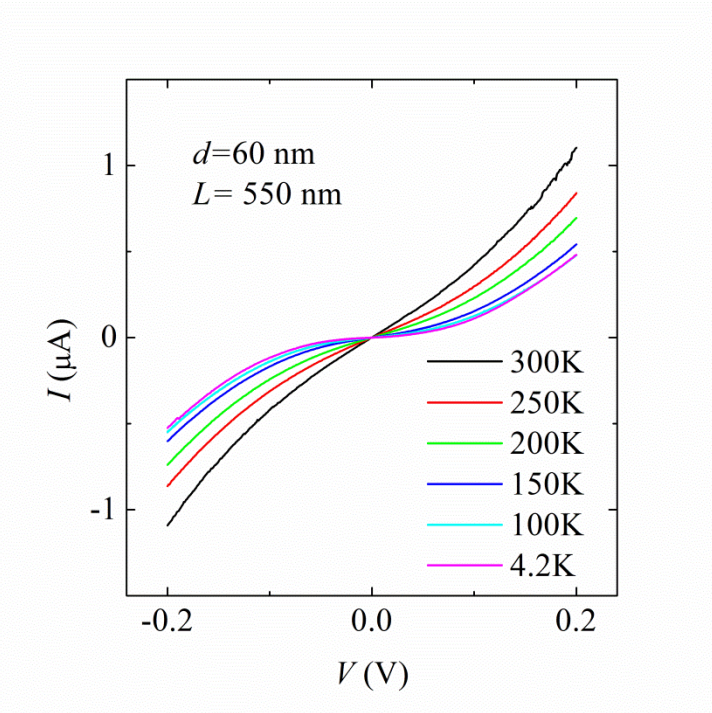


Figure 4-8. Electrical data of a NW device that consists of both ohmic and tunneling contacts as a function of temperature. The *I-V* curve is non-linear and is weakly dependent on temperature, consistent with tunneling mechanism.

To establish that single-step tunneling is the dominating carrier transport mechanism in Co/MgO/NW junctions, we apply the "Rowell criteria" to assess the quality of the contact [103], [104]. The Brinkman–Dynes–Rowell (BDR) model [103] states that the conductance of the tunnel contact should have a parabolic dependence on applied voltage. By differentiating the current with voltage, *dI/dV*, we can obtain the conductance at each voltage point in our NW tunnel contacts, as shown in Fig. 4-9.

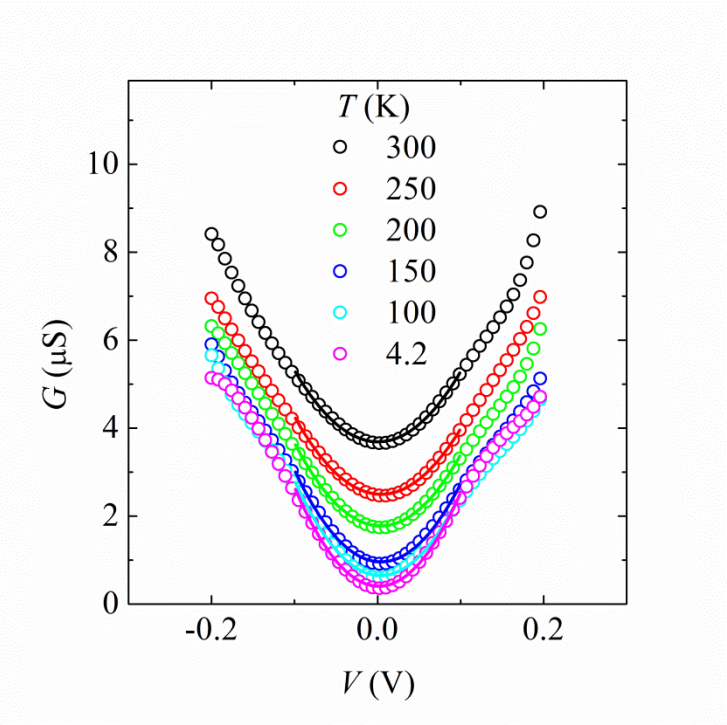


Figure 4-9. Temperature-dependent conductance of NW tunnel junctions. Solid-lines are fitting results to parabolic dependence on voltage.

However being able to fit the BDR model is only a necessary but not sufficient condition. It has been shown that tunnel barriers with pinholes can still exhibit parabolic *G vs. V* signature [105]. The temperature-dependence of zero-bias-resistance (ZBR), namely $G(0)^{-1}$, is another indicator of the tunnel barrier quality. In the NW tunnel contacts, the ZBR has only modest dependence on temperature [106], [107], as shown in Fig. 4-10, suggesting the integrity of MgO as a tunnel barrier on Ge NWs.

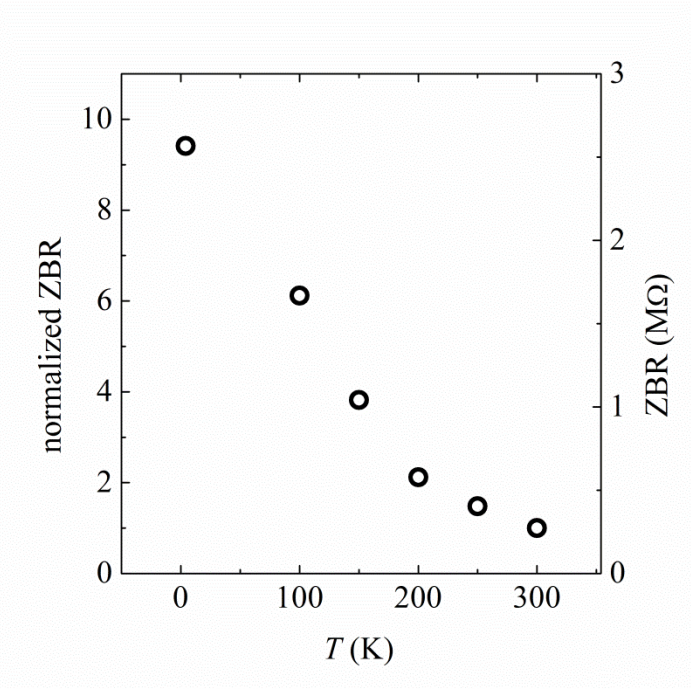


Figure 4-10. Zero-bias-resistance as a function of temperature. Left-hand axis values are normalized to 300 K data.

4.2.2. Magnetization of nanomagnets

In order to observe spin-valve effect in Ge NW devices, the experimental apparatus must be able to attain different magnetization configurations. To achieve this, we use rectangular-shaped magnets in which the length is much longer (μm's) than the width (<500 nm). The shape anisotropy ensures that the electrodes' magnetization direction is pinned to the long-axis. The magnetization direction can then be switched by sweeping an external magnetic field parallel to the easy axis. Utilizing non-identical electrode width in one device, we will then be able to flip the magnetization of individual electrode by sweeping a magnetic field along the easy-axis, and study the device characteristics at various magnetization configurations.

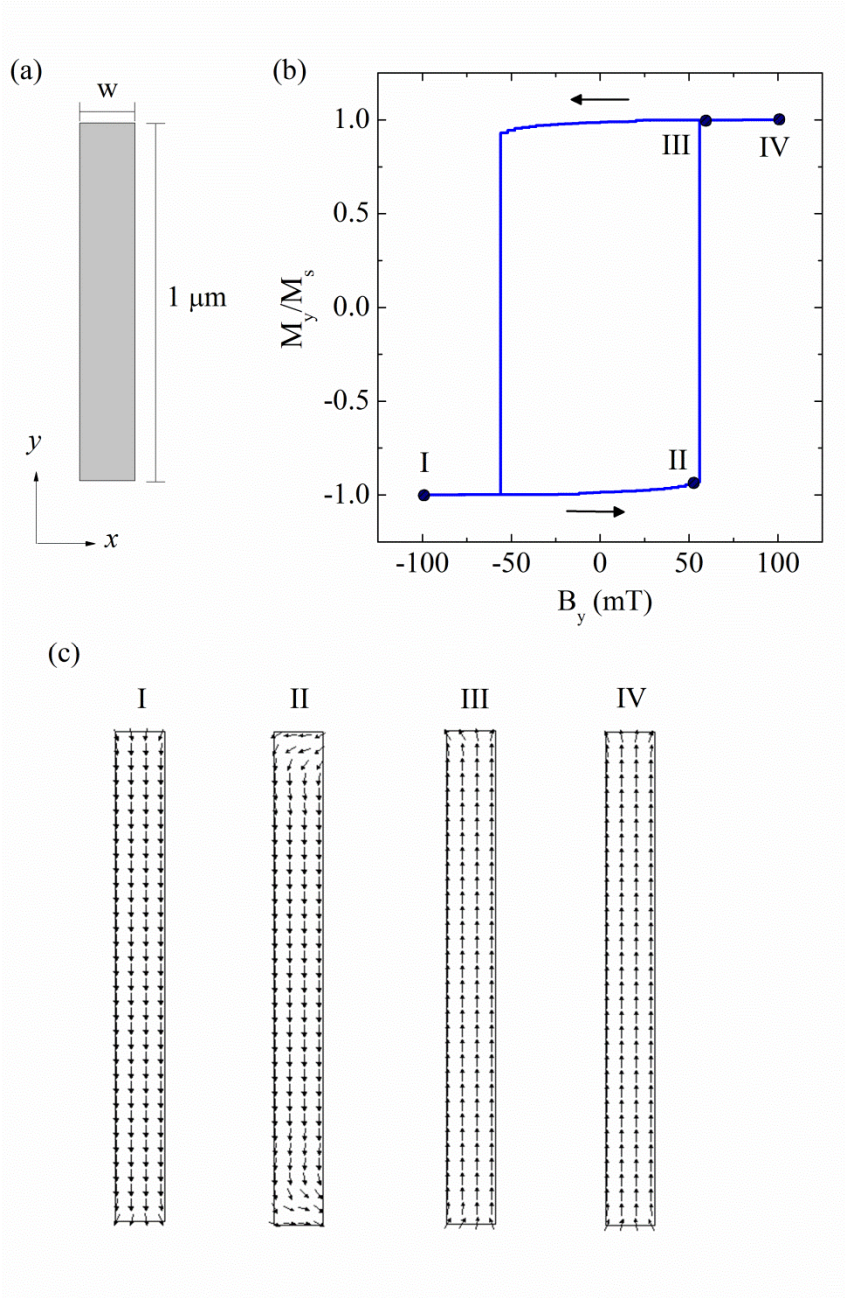


Figure 4-11. OOMMF simulations of Co nanomagnets. (a) Structure used in the simulation. The rectangle width varies from 100 nm to 500 nm. Cobalt material parameters are assumed. (b) Magnetization hysteresis as the magnetic field is sweeping up and down in the y-direction. (c) Microscopic view of the domain magnetizations at different stages of the simulation, as labeled in (b).

We employ micomagnetic simulations (Object Oriented Micromagnetic Framework, OOMMF) [108] to study the switching filed of nanomagnets as a function of width. The simulation structure is shown in Fig. 4-11(a), which is a rectangle with a length of 1 μm. The width ranges from 100 nm to 500 nm. The cobalt material parameters are used here. The simulation results of a Co strip with width of 100 nm is shown in Fig. 4-11(b), in which it plots the y-direction magnetization normalized to saturation magnetization as a function of the magnetic field in y-direction. The magnetization hysteresis can be clearly observed, and the coercive field can be readily recognized. Figure 4-11(c) plots the microscopic view of the domains at different stages of positive-field sweep, as indicated in Fig. 4-11(b).

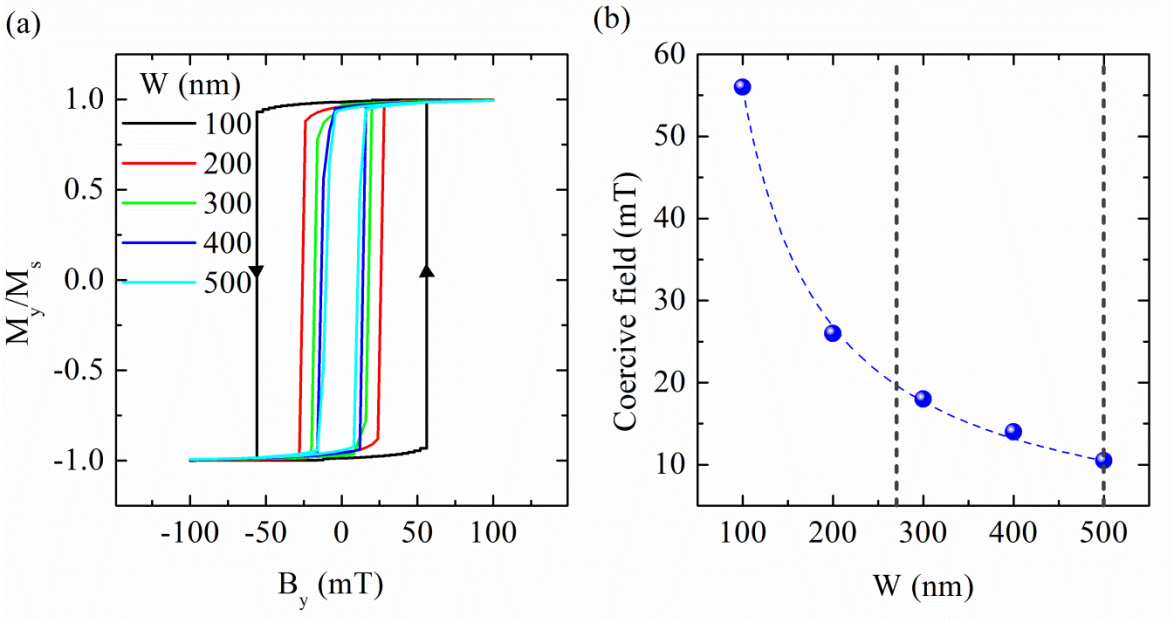


Figure 4-12. OOMMF simulation results of nanomagnets. (a) Hysteresis curves of Co stripes with different widths. (b) Coercive field *vs.* width. The wider the magnet, the smaller the coercive field is. The dashed lines represent the typical widths of contacts used in this study.

The data in Fig. 4-12 summarizes the simulations results. Figure 4-12(a) shows the hysteresis curves for different widths, in which the narrower strip has wider hysteresis window. Indeed, the plot of the coercive field against width in Fig. 4-12(b) clearly shows that the coercive field is inversely proportional to the width. Therefore we can probe the spin-valve effect in our devices if we employ varying contact width in one device.

4.3. SPIN INJECTION IN GE NWS

4.3.1. Two-point (local) spin-valve measurement

We use semiconductor analyzer to characterize the electrical properties of the spin-valve devices. Figure 4-13 is a typical two-point *I-V* data of a Ge NW device with 10 Å-thick MgO at 4.2K. We can see that the *I-V* curve is nonlinear and the resistance (>0.1 MΩ) is much larger than that of devices without MgO presented in section 4.1.

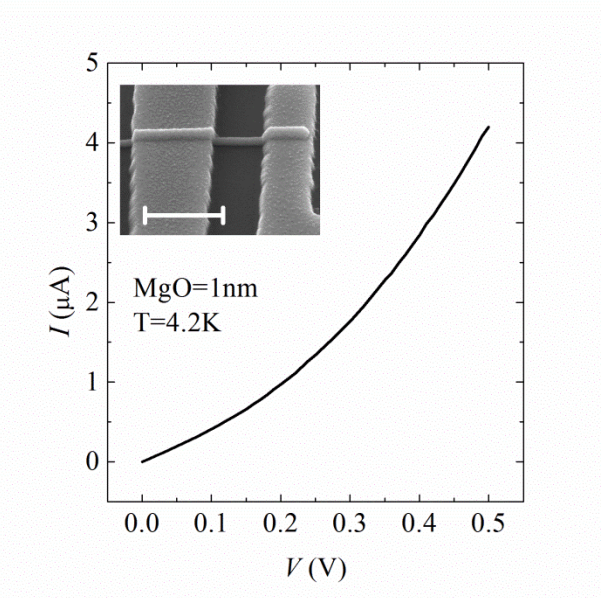


Figure 4-13. Current-voltage data of a Ge NW spin-valve device using 1nm-thick MgO as tunnel barrier at 4.2K. The device is dominated by the tunnel barrier, showing non-linear *I-V* and high resistance. The scale bar is 500 nm.

We use low frequency lock-in techniques to characterize the magnetoresistance (R) of the NW devices. The voltage drop between two adjacent contacts is monitored while a contact AC current (100 nA, 11 Hz) is maintained between the two contacts and an external magnetic field (B) in the direction parallel to the contacts is being slowly swept (1 mT/s). Figure 4-14 shows the R *vs.* B data of the device presented in the previous figure. The B-field is first ramped to 250 mT, and is slowly swept to -250 mT and back, as indicated in the figure. The data exhibits hysteresis as a function of B-sweep, and is symmetric about B=0, which can be explained by the spin-valve effect. For the positive sweep (red curve) of Fig. 4-14, at B = -250 mT, both electrode magnetizations are aligned with the B-field, as indicated by the arrows. As B is increased to +50 mT, the magnetization directions of the two electrodes become antiparallel as the wider electrode changes polarization, and the resistance increases by 60 kΩ. The resistance stays constant until B reaches +160 mT, at which the magnetization of the narrow electrode reverses. Sweeping the B-field further, the electrodes' magnetizations become parallel again and the resistance falls back to the initial value. The reverse sweep generates a symmetric trace and both positive and negative sweeps are repeatable.

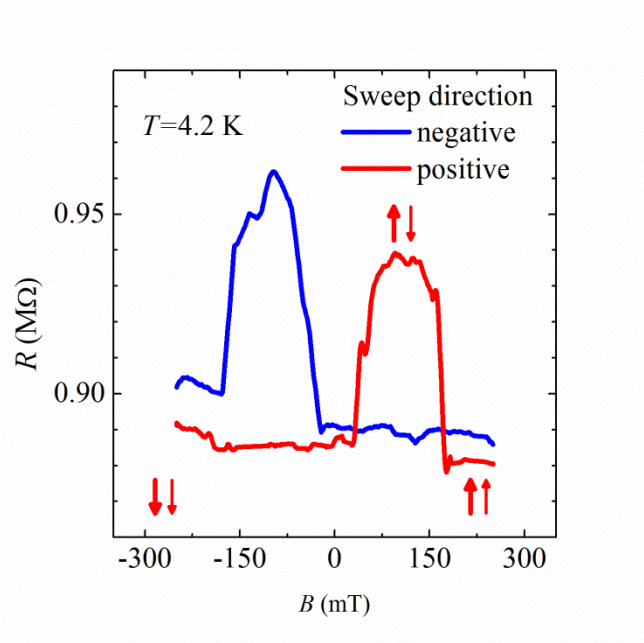


Figure 4-14. *R vs.* in-plane *B*-field measured in the two-point configuration. The red (blue) trace corresponds to the positive (negative) sweep direction. The solid arrows indicate the magnetization directions of the contacts.

4.3.2. Four-point (nonlocal) spin-valve measurement

In order to verify that the observed spin valve-like signal in the two-point configuration stems from spin injection, we performed MR measurements in the nonlocal configuration. Figure 4-15(a) inset shows a SEM of the device and the contact configuration used in the nonlocal MR measurement; the device contains a 15 Å-thick MgO tunnel barrier. The top panel of Fig. 4-15(a) shows the nonlocal voltage difference ($V_{NL} \equiv V_+ - V_-$) *vs.* B.

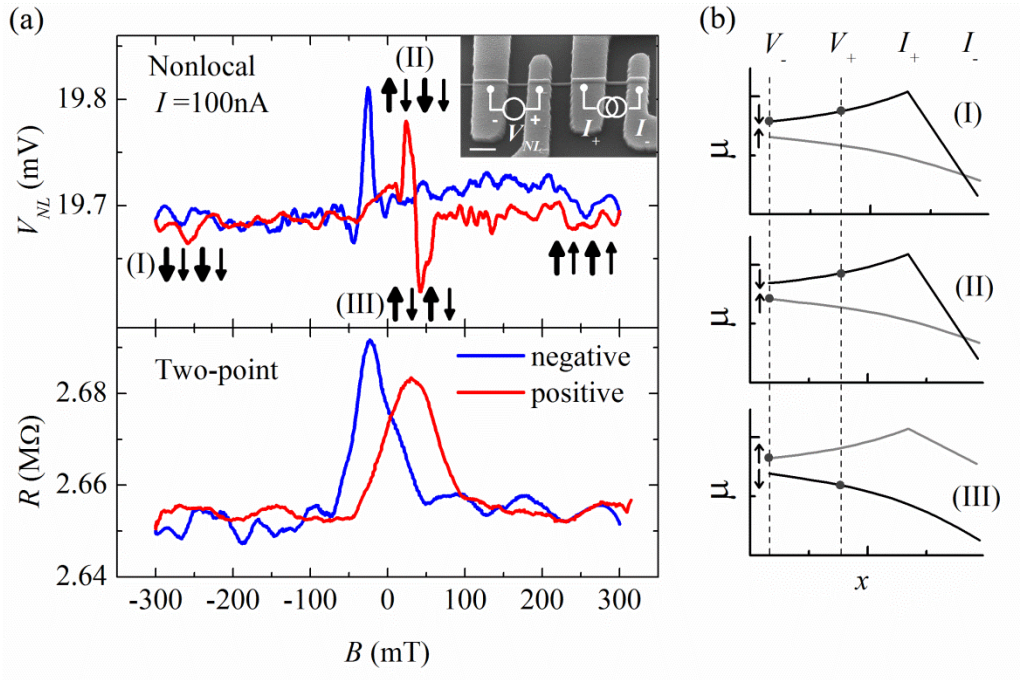


Figure 4-15. Nonlocal magnetoresistance measurement of a Ge NW spin-valve device. Spin signal in nonlocal and two-point configuration, and schematics of spatial-dependent $\mu_\uparrow$ and $\mu_\downarrow$ at different magnetization configurations. (a) Top panel: Nonlocal voltage (V_{NL}) as a function of the in-plane B-field for positive and negative sweep direction. At large negative B, all four electrodes' magnetization directions are parallel. As B is swept toward the positive direction, the signal jumps to a maximum when the magnetization direction of the V_- electrode switches and becomes antiparallel to other three contacts. The I_- contact switches magnetization as B is further increased, and the signal drops. At larger B all contacts magnetizations are parallel and the signal returns to background value. Inset: SEM of the Ge NW device, and the nonlocal measurement configuration. Bottom panel: Two-point MR data measured between the two contacts used as current leads in the nonlocal measurement. The resistance peaks when the two contacts have antiparallel magnetizations, and occurs at the same B-field where the transitions happen in the nonlocal traces. (b) Schematics of the $\mu_\uparrow$ and $\mu_\downarrow$ along the NW; the dots indicate the spin orientation probed by the voltage contacts.

The measured signal can be explained by examining the correspondence between the magnetizations of the contacts and the spin-up ($\mu_\uparrow$) and spin-down ($\mu_\downarrow$) chemical potentials, as shown in Fig. 4-15(b). At B = -300 mT, all four electrodes are magnetized toward the negative direction, as indicated by configuration (I). The spin-polarized electrons injected into the NW create spatial-dependent $\mu_\uparrow$ and $\mu_\downarrow$ along the NW axis, as shown in the top panel of Fig. 4-15(b). The constant background signal in Fig. 4-15(a) is typically observed in nonlocal measurements, independent of the spin valve effect. As B is ramped to +23 mT [configuration (II) of Fig. 4-15(a), and middle panel of Fig. 4-15(b)], V_- reverses and detects $\mu_\uparrow$ while V_+ still senses $\mu_\downarrow$. This translates into a 90 μV increase in V_{NL}. At B = 41 mT, the I_+ electrode switches and is now injecting spin-up electrons into the NW [configuration (III) in Fig. 4-15(a), and the bottom panel of Fig. 4-15(b)]. While V_+ and V_- are still sensitive to $\mu_\downarrow$ and $\mu_\uparrow$, respectively, the voltage difference is now of the same magnitude but opposite sign to that of the previous stage, which translates into the 70 μV drop below the background level in Fig. 4-15(a). At even larger B-field all the electrodes' magnetizations are aligned, and the signal now represents the spatial dependence of $\mu_\uparrow$. Reverse sweeps show similar behaviour. Also shown in the bottom panel of Fig. 4-15(a) is the two-point MR data measured between electrodes I_+ and I_-, which behaves similarly to that of Fig. 4-14: the resistance initially stays constant while the field is slowly being swept toward the opposite direction, jumps to a larger value when the wider electrode flips its magnetization, and drops to the initial value after both electrodes are again aligned with the field. The transitions in two-point and nonlocal data occur at the same B-field, which strongly suggests that the spin valve effect observed in two-point MR originates from spin injection and accumulation in Ge NWs.

4.3.2.1. Baseline value of nonlocal measurement

In typical nonlocal measurements, a non-zero baseline voltage is usually observed, as shown in the previous section. It may originate from the small leakage currents between large contact pads. However in our devices the leakage current is less than 1 pA and hence can be ruled out. Another possibility is the non-uniform electron injection at the contacts, which may be due to the uneven tunnel barrier thickness or the existence of pinholes. Though we established in previous section that the tunnel barrier dominates the contact, it is possible that the MgO is not deposited onto the NW conformally. We discuss here how a non-uniform tunnel barrier can relate to the baseline voltages of nonlocal measurements in lateral NW spin-valve devices.

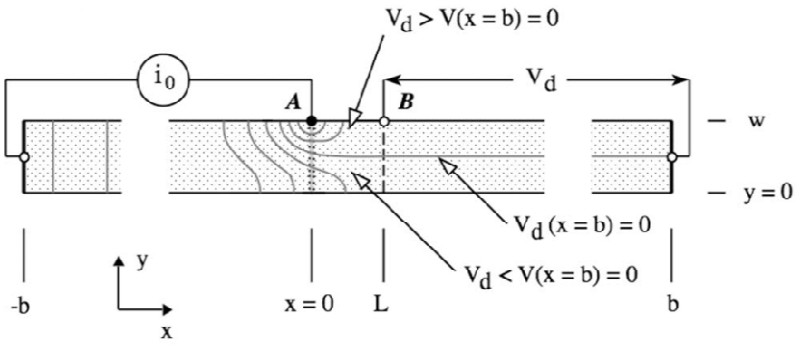


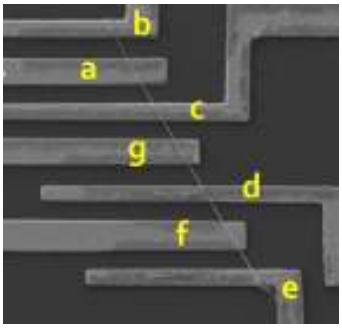
Figure 4-16. Top-view schematic of nonlocal measurement of NW spin-valve devices. A constant current i_0 is maintained between x=0 and x=-b, while the voltage difference is measured between x=L and x=b. Here we consider a specific case in which the current injection and detection happens at point A (x, y) = (0, w), and B (x, y) = (L, w), respectively. The equipotential lines are also shown in the grey area. (Figure and caption adapted from Ref. [109])

In Fig. 4-16, we sketch the nonlocal measurement schematic of a NW spin-valve device. The current is injected at x=0 and the voltage is detected at x=L. If the tunnel barrier is conformal, the current should be injected uniformly across the junction. Here we consider a case that the current injection happens at the point A, as shown in the figure. For the region $x \leq 0$, the equipotential lines are concentric semicircle near the

injection point, and becomes parallel to y-direction near x=-b. For positive x region, the current first spreads out to x>0 and then curls back toward negative x, resulting in the nonzero, varying voltage along $x=L$. If the voltage detection at $x=L$ is also non-uniform, the nonlocal voltage will have a baseline voltage, and is proportional to the injection current i_0. It should be noted that the baseline voltage depends strongly on the nature of non-uniformities of the contacts, and could be either positive or negative.

To further understand the baseline in nonlocal measurements, we fabricated a test sample which consists of multiple contacts with a MgO thickness of 0.8 nm, as shown in Fig. 4-17(a). Two electrodes are used as current leads, and the nonlocal voltage is measured between each pair of adjacent contacts on the NW. The data in Fig. 4-17(b) shows that as the injection current is increased from 10 nA to 100 nA, the measured voltage generally increases by 10-fold as well. Moreover, both positive and negative voltages appear, depending on which pairs are used as voltage detectors. These are consistent with non-uniform tunneling current at the contacts, which can be explained by uneven MgO thickness around the NW.

(a)



(b)

I+	*I*-	*V*+	*V*-	*I* (nA)	V_{NL} (μV)
f	e	d	g	10	-7.2
				100	-75
		g	c	10	-1.5
				100	-14
		c	a	10	3.4
				100	33

Figure 4-17. Nonlocal voltage baseline test results. (a) SEM of the device used for nonlocal baseline voltage measurement. (b) Two contacts ("f" and "e") are used as current injectors, and voltage is measured between each adjacent pair of contacts. As the injection increases, the V_{NL} also increases. Both positive and negative values have been observed, depending on which pair of contacts are used as detectors.

4.3.3. Spin diffusion length in Ge NWs

A key parameter to describe the spin transport is the electron's spin diffusion length (l_{sf}), which describes the length-scale that an electron can travel before losing its spin orientation. The reported l_{sf} values in other semiconductors are, 1.8 μm in GaAs [74], and 2 μm in graphene at low (< 10 K) temperatures [110]. For Si, coherent spin transport over 10 μm was demonstrated using hot electron injection at 85K [111], and recently a l_{sf} of 0.2 μm at room temperature has been reported [112]. The l_{sf} value in a semiconductor is related to the two-point MR ($\equiv \Delta R/R_P$) [74], as described in Chapter 3:

$$\Delta R = \frac{2(P_{\sigma F} r_F + P_{\Sigma} r_C)^2}{(r_F + r_C)\cosh\left(\frac{L}{l_{sN}}\right) + \frac{r_N}{2}\left[1 + \left(\frac{r_C}{r_N}\right)^2\right]\sinh\left(\frac{L}{l_{sN}}\right)}$$

$$R_P = 2\left(1 - {P_{\sigma F}}^2\right)r_F + r_N\frac{L}{l_{sN}} + 2\left(1 - {P_\Sigma}^2\right)r_C + 2\frac{(P_{\sigma F} - P_\Sigma)^2 r_F r_C + r_N\left({P_{\sigma F}}^2 r_F + {P_\Sigma}^2 r_C\right)\tanh\left(\frac{L}{2l_{sN}}\right)}{r_F + r_C + r_N\tanh\left(\frac{L}{2l_{sN}}\right)}$$

ΔR is the resistance difference between the antiparallel (R_{AP}) and parallel (R_P) configurations of the electrodes' magnetizations, $P_{\sigma F}$ and P_Σ are the bulk spin asymmetry coefficient in a Co electrode and spin-dependent tunnelling coefficient of the Co/MgO/NW contact, r_N and r_F are the product of l_{sf} and resistivity (ρ_s) of the Ge NWs and Co, respectively. The parameters in these equations are either known, such as $P_{\sigma F}$ and and r_F, or can measured in the experiments, such as the Ge NW resistivity, and r_C. However, the spin-dependent tunnelling coefficient remains unclear for the Co/MgO/Ge NW tunnel contact used here. Moreover, owing to the absence of a well defined crystal direction at the Co/MgO/NW contact, as well as the e-beam evaporated MgO, we expect the P_Σ values to be device dependent.

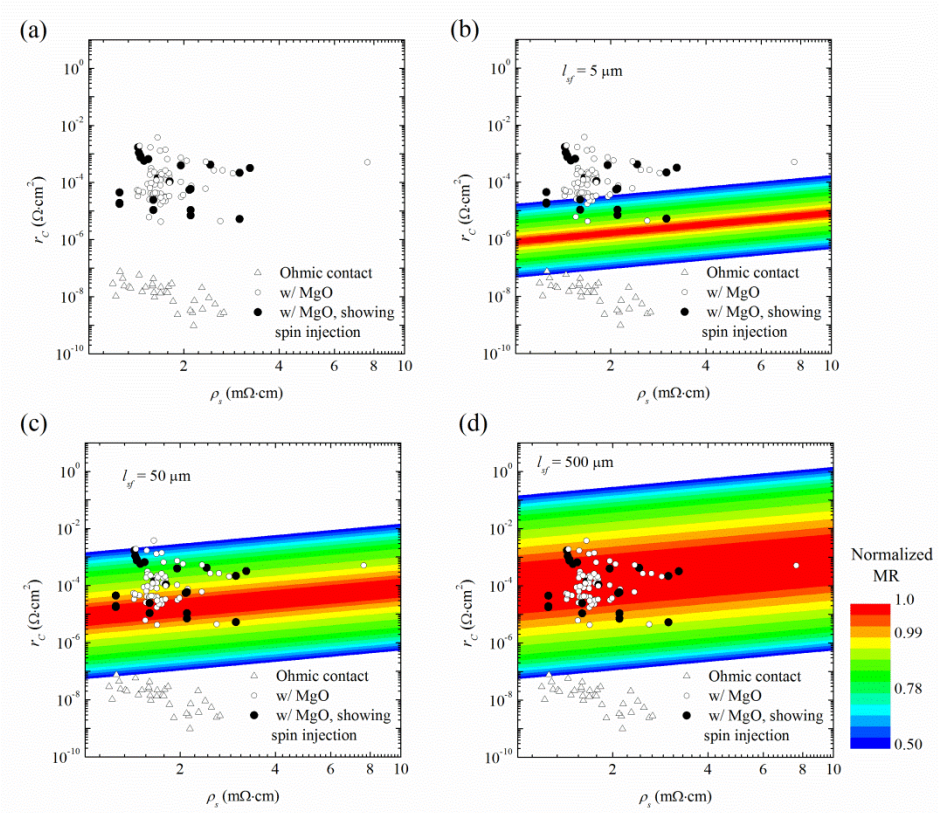


Figure 4-18. Specific contact resistance (r_C) *vs.* resistivity (ρ_s) data for Ge NWs with Co contacts. (a) The different symbols represent devices with (circles) or without (triangles) MgO tunnel barriers, and the closed symbols represent devices that exhibit spin valve effect. (b), (c), and (d) are the MR contour plots calculated using l_{sf} = 5, 50, and 500 µm, respectively. In (d) the maximum MR contour (red corridor) overlaps best with the devices showing spin injection; partial overlap is obtained as long as l_{sf} is assumed to be larger than 100 µm. We note that some devices in the red band did not exhibit spin valve effect, a finding we attribute to variability associated with e-beam evaporation of MgO, namely lack of crystallinity or a well defined crystal direction of the Co/MgO/Ge NW stack.

In order to estimate the l_{sf} in Ge NWs we examined more than hundred devices spanning over six orders of magnitude in r_C, and manifestly mapped out the optimum conditions for spin injection. Figure 4-18(a) shows r_C *vs.* ρ_s for all devices examined in this study; the closed (open) symbols represent devices in which spin valve effect is

present (absent). The data show that spin injection is only observed in devices with r_C between 10^{-4} and 10^{-3} $\Omega\cdot cm^2$, and are absent at higher or lower r_C. We then calculated the optimal range of r_C and ρ_s values for spin injection (red corridor in Fig. 4-18) using P_Σ and l_{sf} as fitting parameters; higher (lower) l_{sf} values move this corridor upward (downward), while P_Σ impacts mainly the MR value. The r_F used in the calculation is 4.5×10^{-11} $\Omega\cdot cm^2$ [74]. In order to overlap the calculated (r_C, ρ_s) corridor which allows for spin injection with the *measured* (r_C, ρ_s) window where spin valve effects are experimentally observed, the l_{sf} values in the Ge NWs examined here have to be at least 100 μm. As shown in Fig. 4-18(d), the best overlap between theory and experiment is obtained for l_{sf} = 500 μm. Though the l_{sf} cannot be determined more accurately using this technique, it is clear that the spin diffusion length in Ge NWs at 4.2 K is larger than 100 μm.

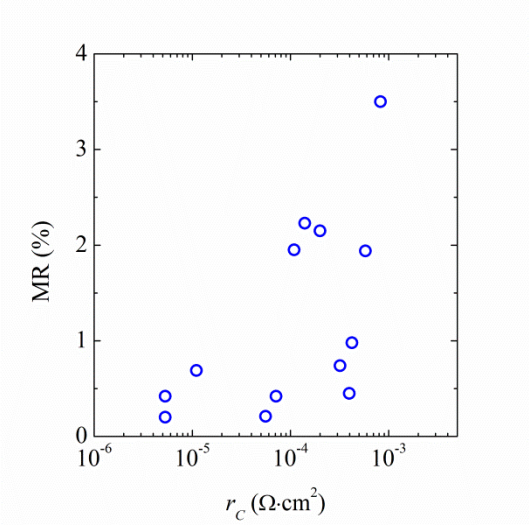


Figure 4-19. Magnetoresistance ratio versus contact resistivity. A measurable MR ratio can only be observed between a r_C of 10^{-5} to 10^{-3} $\Omega\cdot cm^2$; there are no observable spin-valve effect for devices with either larger or smaller contact resistivity values.

Indeed, if we plot the MR ratio as a function of r_C, as shown in Fig. 4-19, we find that the highest values of MR fall onto devices with r_C of 10^{-4}, consistent with the results from 4-18. We note that since the input impedance of the lock-in amplifier is 100 MΩ, electrical characterization for devices with contact resistivities larger than 10^{-3} Ω·cm^2 is not reliable. It can in principle to be resolved by using lock-in amplifiers with larger input impedance.

4.3.4. Temperature dependence of spin-valve effect

The temperature-dependence of spin-valve signal can provide insight into the spin relaxation mechanisms in Ge NWs. As discussed in chapter 3, the dominating spin relaxation mechanism is Elliot-Yafet spin relaxation, which is proportional to momentum scattering rate [86]. Therefore as temperature increases, the spin relaxation rate is expected to increase thanks to elevated phonon scattering. Figure 4-20 data shows the nonlocal spin-valve signal measured from 1.5 K to 20 K; the device has a 10Å-thick MgO tunnel barrier. The signal is the strongest at 1.5 K, and decreases as the temperature is increased to 20 K. Figure 4-21 plots the change in nonlocal voltage (ΔV_{NL}) versus T^{-1}. Recently it is shown that in bulk Ge [113], the spin relaxation time, τ_s, is proportional to $T^{-1.9}$. We surmise here that in Ge NWs, other extrinsic mechanisms which are less temperature-dependent might also be involved in spin relaxation scattering.

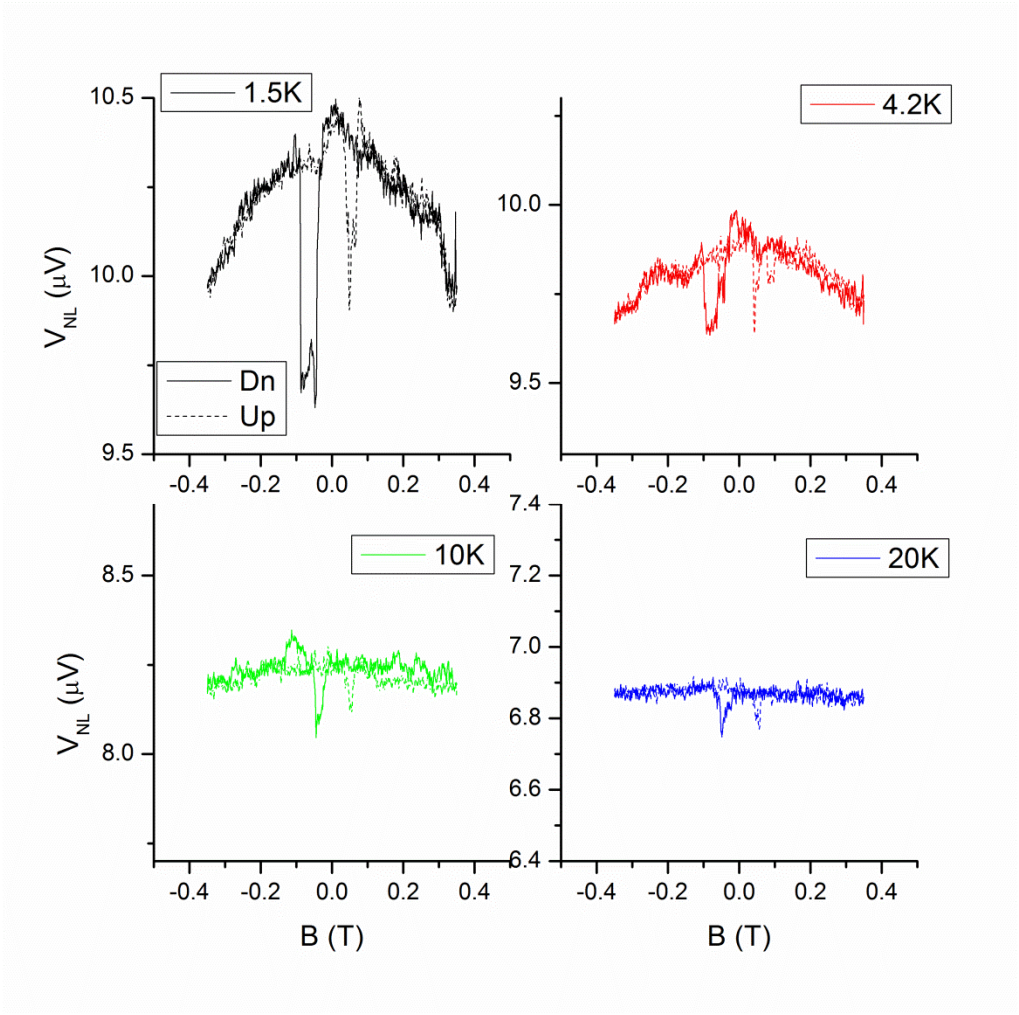


Figure 4-20. Temperature-dependence of nonlocal spin-valve signal. The signal, ΔV_{NL}, decreases as the temperature increases, which may be explained by Eliot-Yafet spin relaxation mechanism.

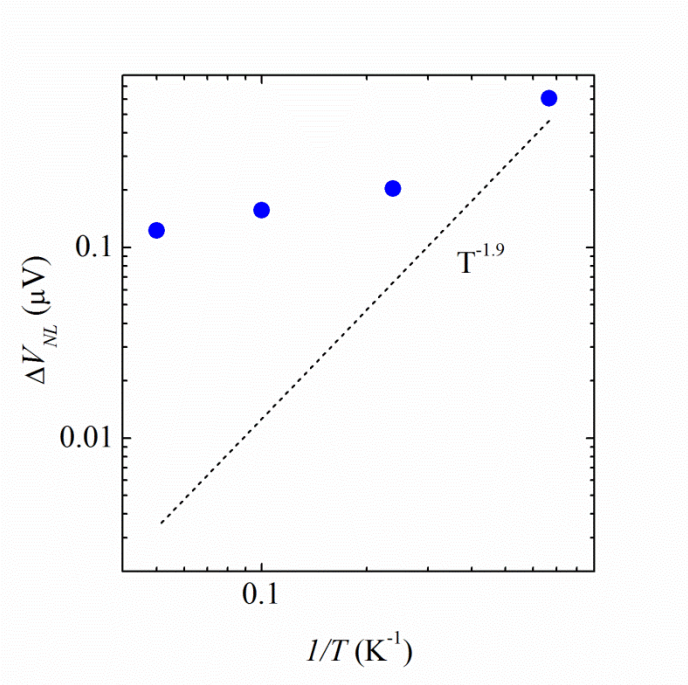


Figure 4-21. Nonlocal signal as a function of 1/T. The temperature dependence is weaker than that of momentum scattering in bulk Ge ($T^{1.9}$) [113].

4.4. MECHANISMS LEADING TO UNDERPERFORMED NW SPIN-VALVES

In this section we discuss possible reasons that may reduce the magnetoresistance in NW spin-valve devices. First we investigate the magnetization of electrodes in more detail, and find that non-uniform magnetization of the magnetic materials covering the NW may decrease the polarization of electric current. Next we focus on the crystallinity of the deposited MgO, and its effect on the spin-valve signal.

4.4.1. Non-uniform magnetization of ferromagnetic electrodes

In most studies of electrical spin injection using ferromagnetic electrodes, the contacts are assumed to have uniform magnetization direction. This is reasonable since most of the normal metal or semiconductor that serves as the channel are either planar structures or have a low aspect ratio [112], [114]. However, evaporated contacts on NWs

might have discontinuities due to shadowing effects, which in turn can lead to disconnected contacts and/or non-uniform magnetization direction.

We implement OOMMF simulation to illustrate the effect of non-conformal contacts on the magnetization process. Figure 4-22(a) depicts the 2D simulation structure, the NW is assumed to be into the plane. At an external *B*-field of 200 mT along the long axis of the contact, Fig. 4-22(b) shows the microscopic magnetizations in the ferromagnetic contact. Here we use Co's parameters in the simulation. It can be noted that while the domains away from the NW region is uniform and parallel to the applied field, the magnetization along the circumference of the NW is not uniform. As highlighted by the red circle, only the very top of the contact has same magnetization direction as the main body of the electrode. This will reduce the spin polarization of the injected current, and lead to smaller spin-valve effect.

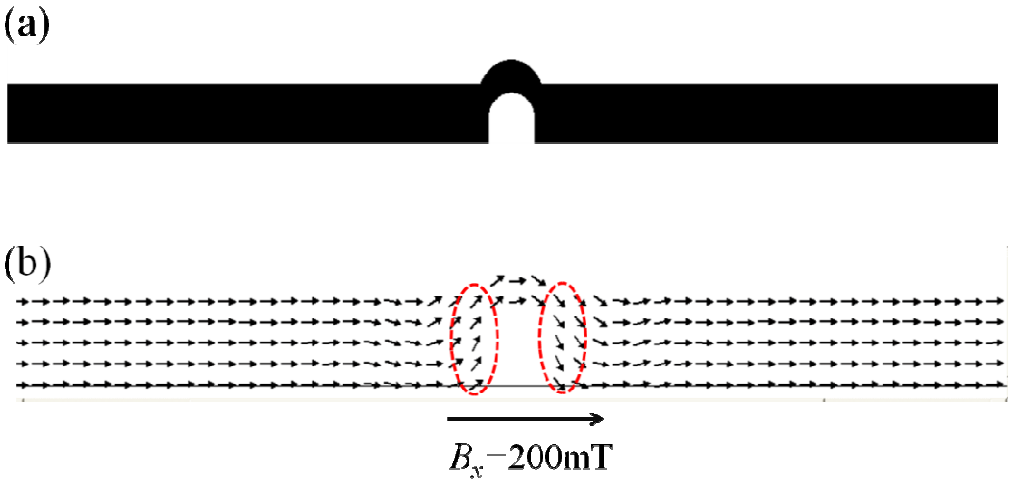


Figure 4-22. OOMMF simulation for the magnetization of ferromagnetic electrodes on the NW. (a) Simulation structure, showing only the Co contact; NW is pointing into the plane. (b) Microscopic magnetization distribution at a *B*-field of 200 mT.

Magnetic force microscopy (MFM) imaging is used to study the magnetization of non-planar nanomagnets [115]. The characterization is done in a commercial atomic force microscope (Digital Instruments Dimension 3000), using a rectangular Si cantilever coated with Co-Cr alloy (Bruker MESP). The MFM tip has a nominal coercive field of 400 Oe and a magnetic moment of 10^{-13} emu. The magnetic information of the sample is acquired using the "Lifting" mode: as illustrated in Fig. 4-23, first the topography of the sample is measured with typical tapping mode AFM [Fig. 4-23(a)], and the it is repeated on the same line with the tip lifted to a constant height (H) [Fig. 4-23(b)], in the range of 15 nm to 50 nm. This prevents the interference from the surface force, which is short-ranged. Prior to characterization, an external B-field of 500 mT parallel to the long axis of the contacts is applied to magnetize the electrodes.

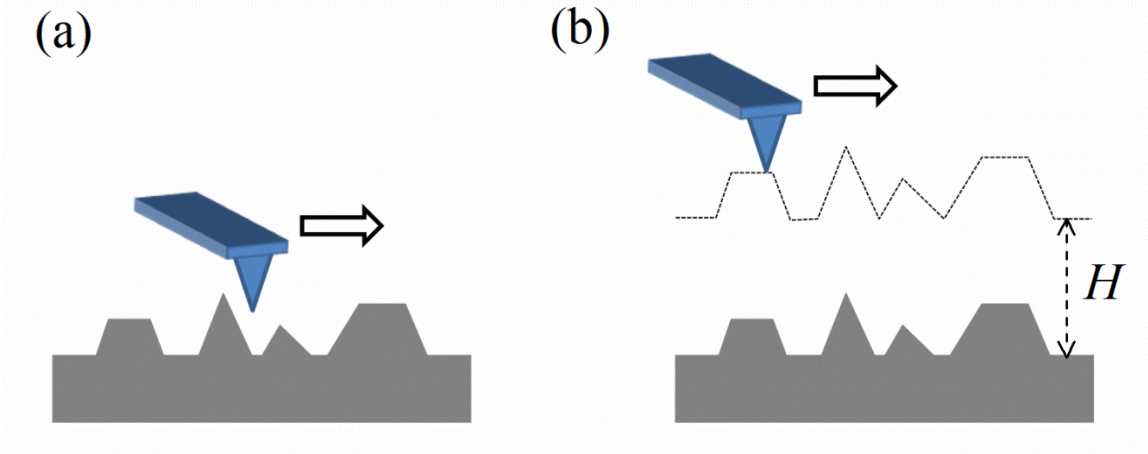


Figure 4-23. Illustration of magnetic force microscopy imaging. (a) The topography is first acquired using AFM tapping mode. (b) The magnetic information of the surface is measured by repeating the scan following the topography of the sample, with the tip lifted by a height H.

The MFM tip, on the other hand, has a magnetization direction *perpendicular* to the sample surface. Therefore the force will be strongest if the local magnetization of sample is out of plane. In Fig. 4-24 we show the MFM results of a typical, multi-terminal

NW spin-valve device. The topography is shown in Fig. 4-24(a) and the MFM in Fig. 4-24(b), taken at a lift height of 50 nm. The MFM data reveals the force exerted on the tip at any point of the map. Here in the color-coded image, red and purple denotes opposite directions of the force the tip measured. We can see that near the circumference of the NW where the cobalt makes contact, there are opposite directions of forces on either side of the NW, as noted by the dashed circle in Fig. 4-24(b). This is consistent with OOMMF simulation presented in Fig. 4-22, and may partially explain the small MR ratio of NW spin-valve devices.

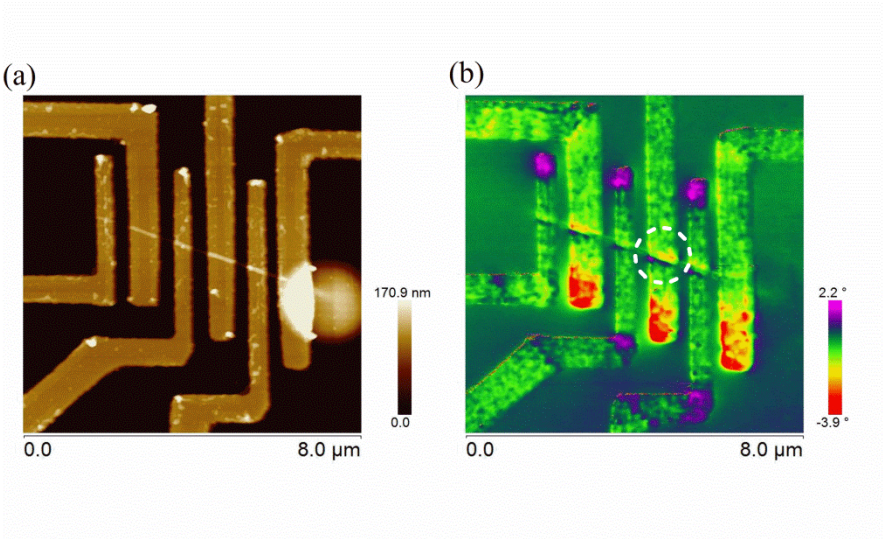


Figure 4-24. MFM data of a NW spin-valve device. (a) Topography of the NW device. (b) MFM of the same device. The measured magnetic force is strongest if the domain has magnetization direction *perpendicular* to the plane. It can be seen that the force has opposite polarity at either side of the NW.

4.4.2. MgO crystallinity

For spin-valve devices, crystalline MgO has proven crucial to achieving high MR ratio performance. For bcc $Co_{1-x}Fe_x$/MgO structures, the spin-filtering can reach up to 85% if the MgO is crystalline and in (001) direction. Indeed, MTJ's utilizing highly oriented MgO(100) as the tunnel barrier have shown superior MR ratio than that of

MTJ's with amorphous tunnel barrier, e.g. Al_2O_3 [59]. In our devices, the MgO is deposited by e-beam evaporation from amorphous target, at room temperature and without further heat treatment. It is expected that the MgO layer is polycrystalline. The lack of a well-defined crystal direction might lead to lower spin-filtering effect of the Co/MgO/Ge NW tunnel junction.

Recent years have seen raised interest in growth of crystalline MgO on Ge substrate [116], [117]. Han *et al* has shown that via MBE at 250°C, MgO grown on Ge(001) is (001) oriented and has a 45° in-plane rotation with respect to that of Ge [116]. Petti *et al* investigated in more detail the effect of substrate preparation, deposition temperature and post-growth annealing on the crystallinity of MgO [117]. They found that, by growing MgO via MBE at room temperature with post-growth annealing at 500°C, the grown MgO is epitaxial and has a well-defined [110] direction parallel to [100] direction of Ge substrate [117], as shown in Fig. 4-25. The Ge substrate also has the least amount of oxidation.

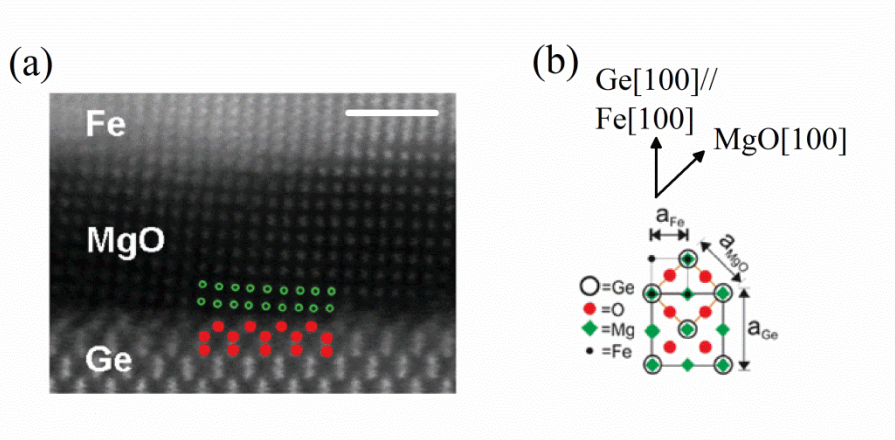


Figure 4-25. Epitaxial MgO grown on Ge. (a) High resolution STEM of Fe/MgO/Ge heterostructure, with surface parallel to Ge (-110) planes. The epitaxial relation of MgO and Ge is clearly seen. (b) Schematics of the lattices and crystal direction. (Figure and caption adapted from Ref. [117])

4.5. CONCLUSION

In this chapter, we demonstrated the growth and characterization P-doped, *n*-type Ge NWs. We achieved electrical spin injection and detection in *n*-type Ge NWs, and mapped out the contact resistance window which allows for spin injection, manifestly showing the conductivity matching required for spin injection. By exploring a wide parameter space in contact resistivity, we show that the spin diffusion length in Ge NWs might be larger than 100 μm. These findings highlight Ge NWs as a potential spintronic material. We also investigate possible parameters that may have hindered highly polarized spin current in Ge NWs, including the uniformity of electrode magnetization and MgO crystallinity. Processes that may improve the MgO crystallinity are suggested, which are based on dry etching of the tunneling contact stacks grown at high temperatures.

Chapter 5: Summary and Future Work

5.1. SUMMARY

The principle of scaling was addressed in Chapter 1, followed by a review on the challenges and issues of scaling in deeply scaled Si MOSFETs. It is established that conventional scaling cannot continue improving the transistor performance, largely due to the onsets of short-channel effects. Adopting novel channel materials and applying multi-gate structures are considered promising routes toward continued MOSFET scaling trends. Besides, using the spin degree of freedom in the electronic devices is expected to enhance the functionality and performance of the overall integrated circuits. In this work, germanium nanowires are investigated as potential platforms for future electronic and spintronic devices.

In Chapter 2, the growth and characterization of the Ge-Si_xGe_{1-x} core-shell nanowires are discussed, followed by the NW *n*-type doping study using low energy phosphorous implantation. The implantation conditions are carefully chosen such that not all part of the NWs are amorphourized after ion implant. The fabrication process of Ω-gated, NW *n*-FETs is described. We then compare the device characteristics fabricated using NWs with and without the Si_xGe_{1-x} shell, and demonstrate performance metrics comparable to state-of-the-art Ge *n*-FinFETs fabricated from top-down approach. Lastly, using the channel-length dependence of NW FET characteristics, we are able to isolate the contact resistance out of the total device resistance, and conclude that the intrinsic channel resistance is the main limiting factor of the ON-current of Ge NW *n*-FETs, which can be explained by the presence of large interface trap density at the NW/dielectric interface.

In the next part of this work we study the aspects of spintronic applications of Ge NWs. In Chapter 3 general theories of spin relaxation in semiconductors are briefly

reviewed, particularly Elliot-Yafet and D'yakonov-Perel' mechanisms. The relationship between the spin relaxation rate and momentum relaxation rates in these two processes are discussed. The dominant spin scattering mechanism in nondegenerate Ge is spin-flipping mediated by intervalley phonon scattering, and is reviewed in detail. It is noted that intervalley scattering is anisotropic in Ge, and can be slowed down by lifting the degeneracy of the four *L* valleys. Calculated intrinsic spin relaxation time is then compared with experimental results. Other relaxation mechanisms relevant to spin-polarized electrons in highly-doped Ge NWs are also discussed, which include electron-impurity scattering and structure-enhanced spin-orbit coupling.

In Chapter 4 we demonstrate spin-polarized transport in Ge NWs. The NWs are grown via Au-catalyzed, VLS mechanism, using phosphine and germane as precursors. The grown NWs are *n*-type, showing an average resistivity of 2×10^{-3} $\Omega\cdot$cm, corresponding to a doping level near high-10^{19} cm^{-3}. Thanks to such a high doping density, the contact resistivity between Co/Ge NW is remarkably low, reaching 10^{-8} $\Omega\cdot cm^2$. With such a low intrinsic contact resistivity, we are able to engineer the Co/MgO/Ge NW tunnel contact resistance by adjusting the MgO thickness, mapping out the optimal conditions for spin injection in Ge NWs. Both two-point (local) and four-point (nonlocal) spin-valve signals are demonstrated in lateral NW devices. Using data collected over hundred samples spanning over six orders of magnitude in contact resistance, it is suggested that the spin diffusion length may be longer than 100 μm in Ge NWs at low temperatures. Our results indicate that Ge nanostructures can be a desired platform for spin-based devices.

5.2. FUTURE WORK

5.2.1. High performance Ge NW *n*-FETs

5.2.1.1. NW/dielectric interface passivation

In Chapter 2 we demonstrated Ge/Si_xGe_{1-x} core/shell NW *n*-FETs with performance comparable to that of FinFETs fabricated from top-down approaches. However the ON-current is still smaller than its *p*-FET counterparts [118]. The underperformance of the NW *n*-FETs investigated in this study is attributed to the high interface trap density, possibly present in NW/dielectric interface. Indeed, the poor interface between Ge and dielectric is one of the most critical issues in Ge-based MOSFETs [2], [119]. Various interface passivation schemes, such as Si-cap [120], [121], GeON [122], and GeO_2 [36], [48], [51], have been demonstrated to reduce the interface trap density and increase the inversion charge mobility in either *p*- or *n*-FETs. Recently Ge planar *n*-FETs with high-*k*/GeO_x/Ge gate stack are fabricated with the interfacial GeO_x layer formed by plasma post-oxidation [48]. The devices show a low D_{it} in the 10^{11} $cm^{-2}\cdot eV^{-1}$ range, and a peak electron mobility close to 550 $cm^2/V\cdot s$ [48]. It is expected that if the NW/dielectric gate stack quality can be improved, the ON-current of Ge NW *n*-FETs can be further increased.

5.2.1.2. S/D extrinsic resistance

As the channel resistance continues to decrease with the scaling of channel length, the parasitic resistance, comprised of the metal/semiconductor contact resistance and S/D extension resistance, can become an important fraction in the total device resistance. Indeed, for deeply scaled devices the area of S/D contacts becomes smaller due to limited S/D footprints, and can result in larger contact resistance. It is therefore essential to minimize the extrinsic resistance in order to achieve high performance in aggressively

scaled devices. For example, in the tri-gate MOSFET structures introduced by Intel in its 22 nm node, it is instrumental to use *in situ* doped, raised S/D (RSD) to reduce the impact of external resistance to overall device performance, as shown in Fig. 5-1 [7].

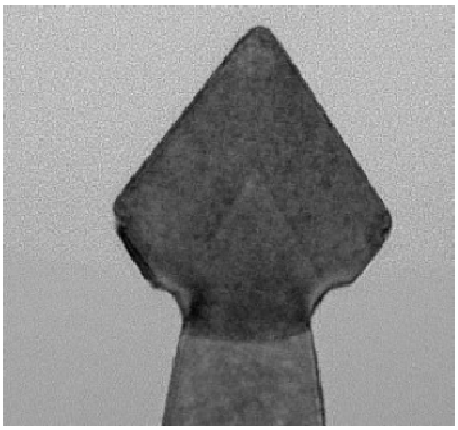


Figure 5-1. TEM image of the raised S/D technology used in Intel's 22 nm technology node. The RSD is deposited by SiGe epitaxy. (Figure adapted from Ref. [7])

On the other hand, due to the lower *n*-type dopant activation levels in Ge [123] and Fermi level pinning [37], [38], the specific contact resistance (ρ_c) can be as large as 10^{-4} $\Omega \cdot cm^{-2}$ [96]. Various solutions, including laser annealing [93], spin-on-dopants [124], and insertion of interfacial layer [94], [125], have been shown to lower the metal/Ge contact resistivity, effectively reducing the S/D contact resistance and improving FET performance. However in aggressively scaled devices, the doping profile achieved using thermally activated or diffused dopants is hard to control, and can result in less-sharp n+ regions. The raised S/D (RSD) technology, on the other hand, can effectively decrease the S/D contact resistance by enlarging the contact area, and provides the shallow and sharp junctions needed to minimize short-channel effects [126]–[128]. While the RSD process has been demonstrated on planar Ge *n*-MOSFETs [126], there are no reports of this technology implemented on deeply scaled, multi-gate Ge

FETs. We have developed a process to selectively deposit *n*-Ge on undoped Ge NWs, as shown in Fig. 5-2.

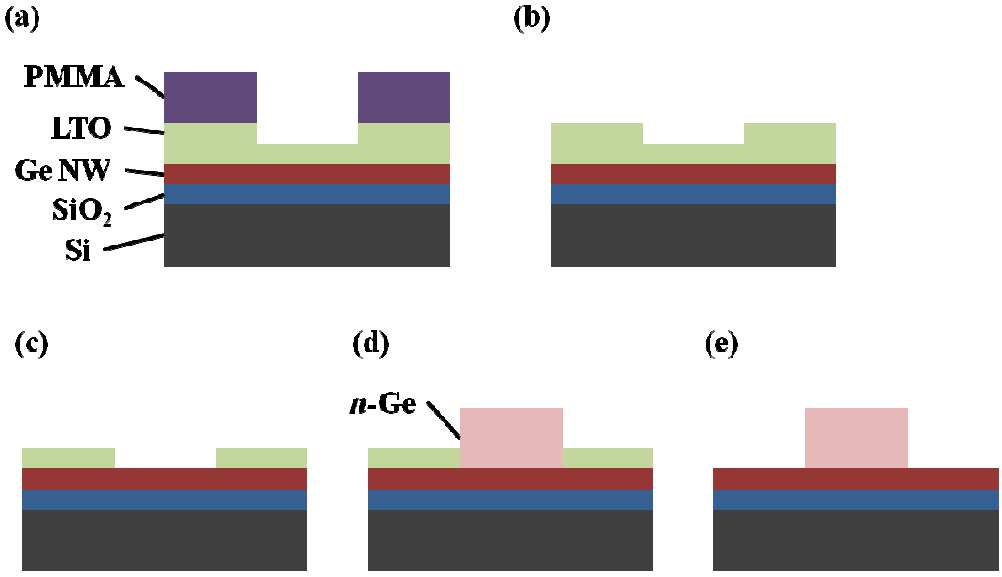


Figure 5-2. Proposed process flow for *n*-Ge RSD on Ge NWs. (a) LTO is first deposited on the NW and patterned using PMMA mask and RIE etch. (b) PMMA mask is removed before the pattern transfer is complete. (c) Residual LTO is removed in HF dip. (d) *n*-Ge is grown selectively on the NW. (e) LTO is removed and RSD completed.

The grown Ge NWs are first transferred onto a SiO_2/Si substrate, and a thin film of low-temperature oxide (LTO) is conformally deposited. The S/D region is patterned using EBL and etching techniques [Fig. 5-2(a)-(c)]. The sample is then transferred into a UHVCVD chamber, and a highly-doped *n*-Ge layer is grown selectively atop the opened NW region in presence of PH_3 and GeH_4, as shown in Fig. 5-2(d). The growth conditions are similar to those of NW082_Ge004, and the resulting layer is expected to have similar doping concentration, near 5×10^{19} cm^{-3}[129]. The remaining LTO is removed using HF etch and the MOSFET process can be continued hereafter [Fig. 5-2(e) and Fig. 5-3].

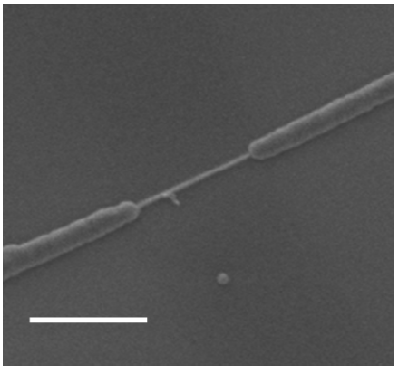


Figure 5-3. Selectively grown *n*-Ge on a Ge NW. Scale bar is 1 μm.

We demonstrate the prospects of the selectively grown *n*-Ge as RSD by fabricating the structures into planar Ge *n*-MOSFETs. The substrate is nominally undoped Ge (100), with resistivity larger than 30 Ω·cm. The wafer undergone same selective *n*-Ge growth using the processes described above. We use time-of-flight secondary ion mass spectrometry (ToF-SIMS) to characterize grown layer, as shown in Fig. 5-4. We note that the phosphorous signal is roughly constant until it reaches the *n*-Ge/Ge interface. It is also observed that there are strong hydrogen and carbon group signals at the interface, suggesting possible surface contamination. The structures are fabricated into ring-FETs with various channel width/length (W/L) combinations. The gate stack comprises of ALD Al_2O_3 (EOT = 3.7 nm) and sputter-deposited TaN. S/D contacts are formed by EBL and Ni lift-off.

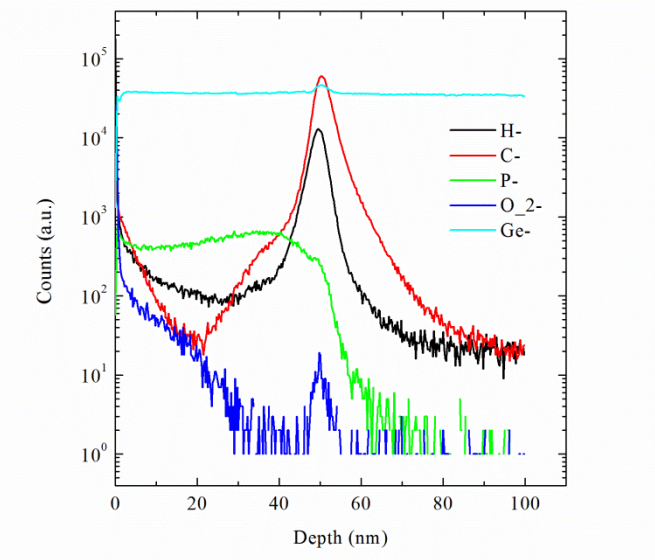


Figure 5-4. TOF-SIMS results of selectively grown *n*-Ge on undoped Ge substrate. The phosphorous signal shows a constant level until it reaches the *n*-Ge/Ge interface. The peaks of H- and C- indicate surface contamination at the interface.

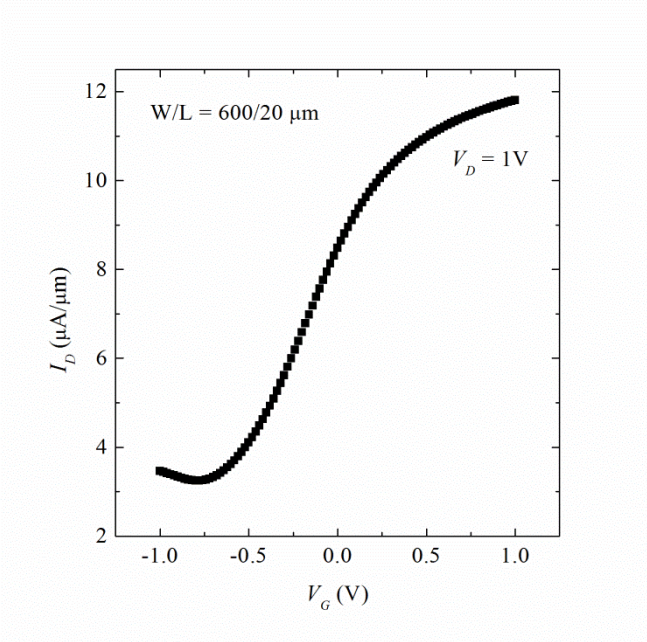


Figure 5-5. Transfer characteristics of a planar Ge *n*-FET with RSD. The ON-current is larger than 10 μA/μm with a channel length of 20 μm, comparable to state-of-the-art Ge planar *n*-FETs.

The devices exhibit high ON-current, larger than 10 μA/μm for a channel length of 20 μm. This is comparable with other Ge MOSFETs with S/D formed using spin-on-dopants [124] or RSD techniques [126]. Note that this set of devices have large OFF-current, possibly due to the use of an undoped substrate. Nevertheless, the results suggest that with highly-doped RSD and an optimized gate stack, Ge NW *n*-FETs are capable of delivering higher ON-current.

5.2.2. Spin injection in Ge NWs

5.2.2.1. Crystalline MgO tunnel barrier

In Chapter 4 we explored Ge NW devices with a wide spread of contact resistances, and determined the optimal conditions for lateral spin injection. However it is noted that some devices, albeit residing in the optimal conditions for spin injection, did not show a measurable spin-valve signal. It is partially attributed to the lack of uniform crystallinity of the MgO tunnel barrier, as discussed in Chapter 4.4.2. In order to achieve crystalline FM/MgO/Ge heterostructure, the whole stack must be deposited *in situ* and undergone high-temperature annealing processes. The lift-off process, from which we use to demonstrate spin-valve effect in Ge NWs, will not be suitable for this purpose, since typical EBL resist (e.g. PMMA) cannot tolerate temperature higher than 100°C without reflowing. Here we describe a new process flow that can withstand processes that have high thermal budget. The *F*/MgO layer will be deposited first on the NW, and subsequently patterned into contacts using inductively coupled plasma (ICP) etching.

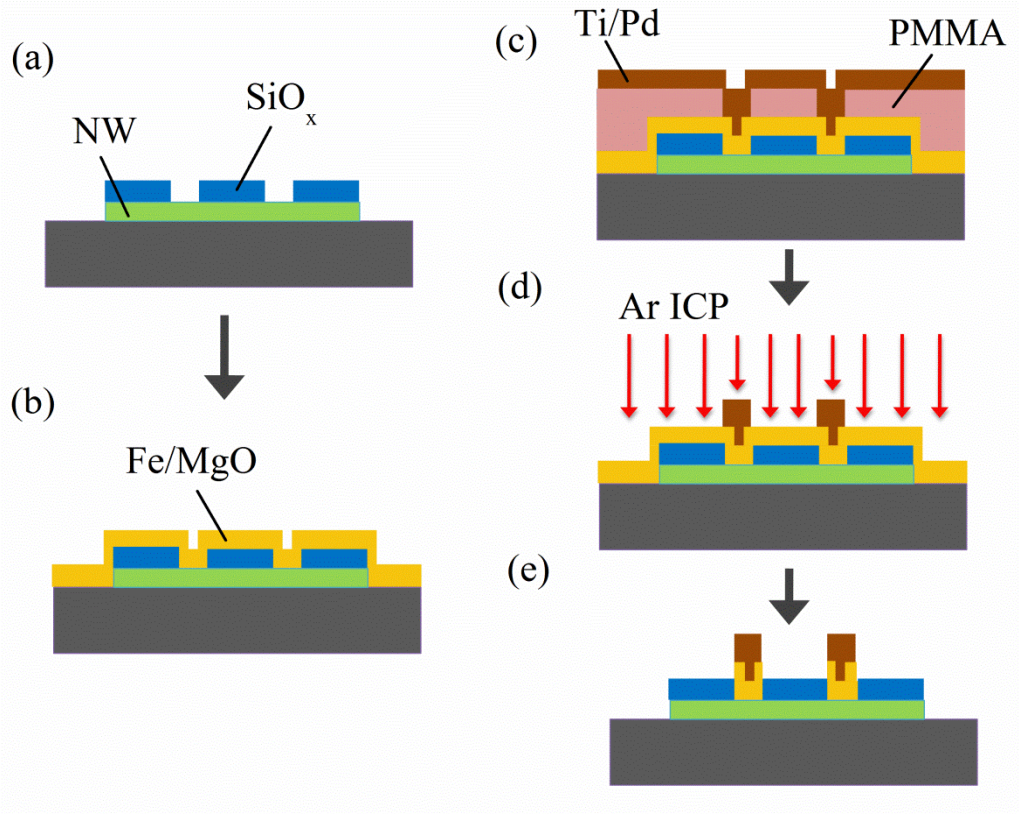


Figure 5-6. Process flow for NW spin-valve devices with MgO grown at high temperature. (a) A SiO_x layer is selectively deposited onto the NW, and serves as the protection layer in the etching process. (b) Fe/MgO is grown at room temperature and annealed at high temperature *in situ*. A capping gold layer is used to prevent oxidation. (c) The hard mask is formed using EBL, Ti/Pd deposition and lift-off. (d) Fe/MgO is etched using ICP in Ar ambient. (e) The finished structure.

The process is depicted in Fig. 5-6. First a SiO_x layer is patterned on a Ge NW using EBL, SiO_x evaporation and lift-off [Fig. 5-6(a)]. This SiO_x layer is crucial in providing protection to the NW in the flowing etching process, since Ge NWs are prone to plasma-induced damage. The Fe/MgO layer is then deposited and annealed at high temperature to improve the crystallinity of the tunneling stack [Fig. 5-6(b)]. Subsequently a Ti/Pd layer is patterned with lift-off process [Fig. 5-6(c)], and acts as the hard mask in the ICP etching step [Fig. 5-6(d)]. The finished structure is shown in Fig. 5-6(e).

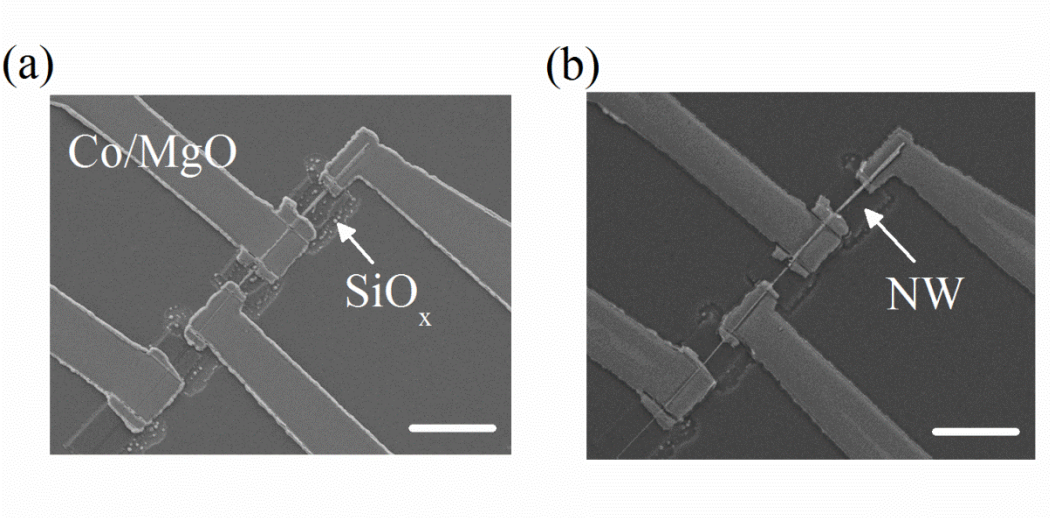


Figure 5-7. Ge NW device with etched contacts. (a) SEM of a NW device fabricated using the processes described in Fig. 5-6. (b) The SiO_x layer is removed by dilute HF, showing that the NW remains intact after plasma etching. Scale bar is 2 μm.

The SEM images in Fig. 5-7 show a NW device fabricated using the processes described above. The Co/MgO electrodes are etched using ICP etching, in an Ar ambient of 10 mTorr, ICP power of 500 W, and RF power of 50 W. After removing the SiO_x with dilute HF [Fig. 5-7(b)], we can see that the NW is intact after the etching process.

In light of the success on the deposition of epitaxial Fe/MgO tunnel barrier on Ge (001), we recently started collaboration with the authors in Ref. [117] to grow MgO on Ge NWs. The NWs are first transferred onto a SiO_2/Si substrate, and subsequently deposited with Fe/MgO by molecular beam epitaxy (MBE) using the optimized deposition/annealing recipe, as described in Ref. [117]: MgO (1.2 nm) is deposited at room temperature and annealed at 500°C for crystallization. The Fe (90 nm) is subsequently deposited at room temperature and annealed at 200°C. The samples are fabricated in spin-valve devices using the process depicted describe above.

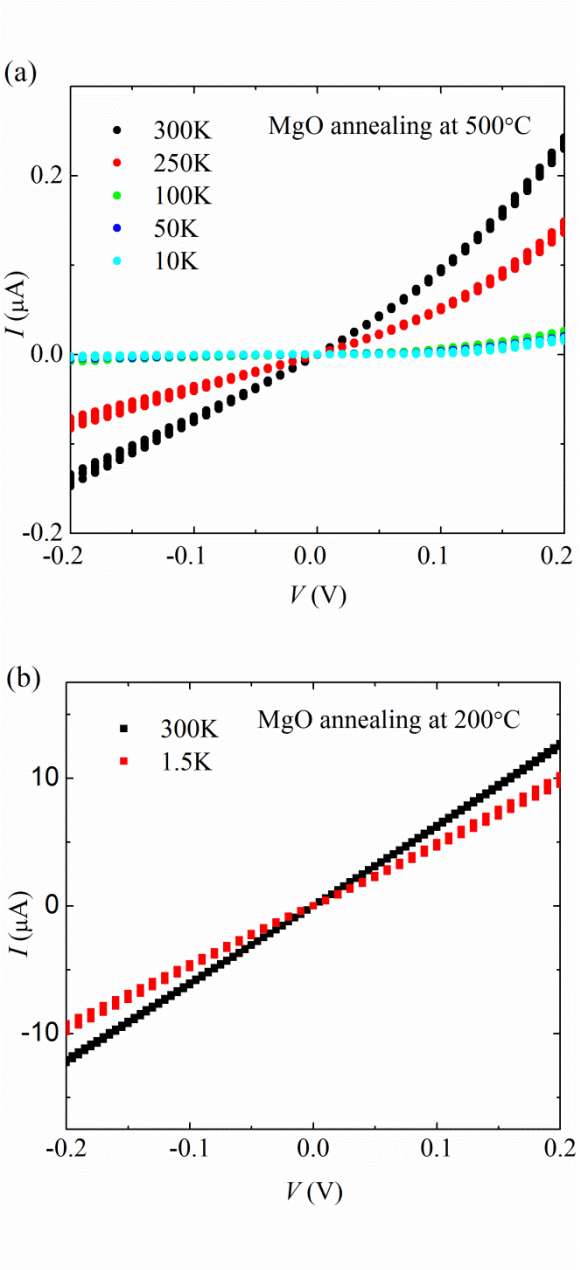


Figure 5-8. Electrical *I-V* data of Ge NW devices with Fe/MgO tunnel contacts. The MgO annealing temperature is 500°C in (a) and 200°C in (b). Both have same MgO thickness of 1.2 nm.

An example of a two-point measurement is shown in Fig. 5-8(a). It is noted that the current level is low when compared to typical devices with MgO that has not gone

through high temperature anneals [129]. The current level also shows a strong dependence on temperature; it decreases as temperature lowers. These indicate that the NWs are no longer highly doped, possibly due to oxidation during the annealing step. To confirm this hypothesis, another set of NW samples are deposited with MgO/Fe using the same process, except that this time the MgO is annealed at 200°C instead of 500°C. The electrical characterization results, shown in Fig. 5-8 (b), are similar to devices with low temperature MgO: current level is high and temperature dependence is weak, consistent with highly doped NWs.

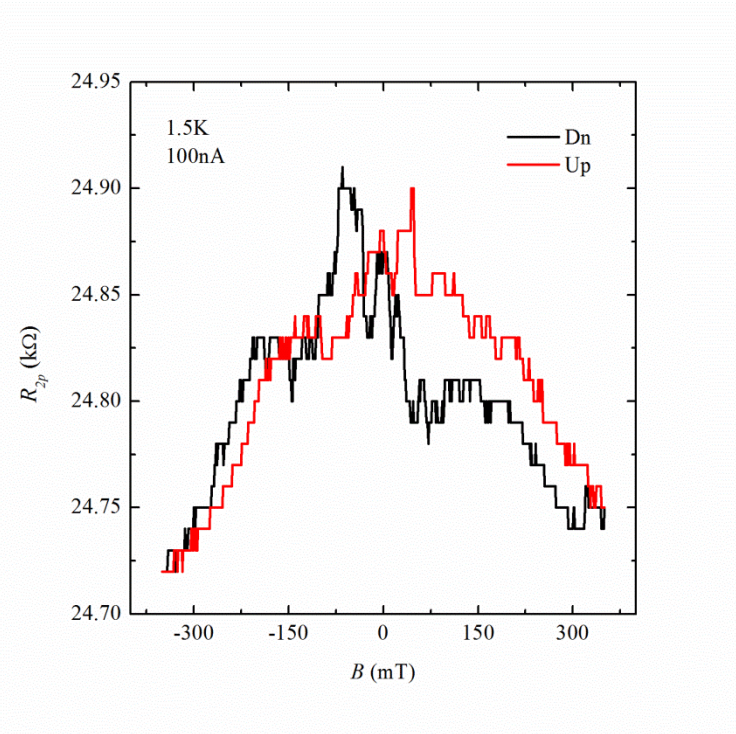


Figure 5-9. Two-point magnetoresistance data of a Ge NW spin-valve with MgO annealed at high temperatures.

Typical two-point magnetoresistance of this set of sample is shown in Fig. 5-9. The devices exhibit spin-valve effect, showing a low (high) resistance state when the

magnetization of contacts are parallel (antiparallel). The MgO thickness shall be optimized in order to further increase the signal level.

5.2.2.2. Spin relaxation mechanisms in Ge NWs

While the study of spin dynamics in bulk semiconductors can be dated decades ago, rigorous theoretical treatment on the spin relaxation mechanisms in the semiconductor nanostructures are to be augmented. The intrinsic spin relaxation time due to intervalley scattering in nondegenerate Ge is only recently calculated, as described in Chapter 3. However there are other mechanisms that need to be considered in NWs, such as the spin flipping due to electron-impurity scattering in highly doped semiconductors, and structure-induced D'yakonov-Perel' relaxation expected at the NW surface. Further understanding in the physics of semiconductor spin dynamics can help guide the design and realization of semiconductor spintronics.

References

[1] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 1.1.1–1.1.6.

[2] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[3] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.

[4] M. Ieong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, "Silicon Device Scaling to the Sub-10-nm Regime," *Science*, vol. 306, no. 5704, pp. 2057–2060, Dec. 2004.

[5] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," in *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, 2003, pp. 11.6.1–11.6.3.

[6] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mcintyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 247–250.

[7] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. Mcintyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in *2012 Symposium on VLSI Technology (VLSIT)*, 2012, pp. 131–132.

[8] "Intel 22nm 3-D Tri-Gate Transistor Technology," *Intel Newsroom*. [Online]. Available: http://newsroom.intel.com/docs/DOC-2032.

[9] K. J. Kuhn, “Moore’s crystal ball: Device physics and technology past the 15 nm generation,” *Microelectron. Eng.*, vol. 88, no. 7, pp. 1044–1049, Jul. 2011.
[10] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. John Wiely & Sons, 1983.
[11] “International Technology Roadmap for Semiconductors, 2012 Update.”
[12] K. J. Kuhn, U. Avci, A. Cappellani, M. D. Giles, M. Haverty, S. Kim, R. Kotlyar, S. Manipatruni, D. Nikonov, C. Pawashe, M. Radosavljevic, R. Rios, S. Shankar, R. Vedula, R. Chau, and I. Young, “The ultimate CMOS device and beyond,” in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 8.1.1–8.1.4.
[13] K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, “Past, Present and Future: SiGe and CMOS Transistor Scaling,” *ECS Trans.*, vol. 33, no. 6, pp. 3–17, Oct. 2010.
[14] Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors - Theory and Device Applications*. Springer, 2010.
[15] C. P. Auth and J. D. Plummer, “Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET’s,” *IEEE Electron Device Lett.*, vol. 18, no. 2, pp. 74–76, 1997.
[16] J. Nah, D. C. Dillen, K. M. Varahramyan, S. K. Banerjee, and E. Tutuc, “Role of Confinement on Carrier Transport in Ge–SixGe1–x Core–Shell Nanowires,” *Nano Lett.*, vol. 12, no. 1, pp. 108–112, Jan. 2012.
[17] W. Lu, J. Xiang, B. P. Timko, Y. Wu, and C. M. Lieber, “One-dimensional hole gas in germanium/silicon nanowire heterostructures,” *Proc. Natl. Acad. Sci. U. S. A.*, vol. 102, no. 29, pp. 10046–10051, Jul. 2005.
[18] M. T. Bjork, C. Thelander, A. E. Hansen, L. E. Jensen, M. W. Larsson, L. R. Wallenberg, and L. Samuelson, “Few-electron quantum dots in nanowires,” *Nano Lett.*, vol. 4, no. 9, pp. 1621–1625, Sep. 2004.
[19] I. Zutić, J. Fabian, and S. D. Sarma, “Spintronics: Fundamentals and applications,” *Rev. Mod. Phys.*, vol. 76, no. 2, p. 323, 2004.
[20] D. D. Awschalom and M. E. Flatté, “Challenges for semiconductor spintronics,” *Nat. Phys.*, vol. 3, no. 3, pp. 153–159, Mar. 2007.
[21] H. Dery, P. Dalal, Ł. Cywiński, and L. J. Sham, “Spin-based logic in semiconductors for reconfigurable large-scale circuits,” *Nature*, vol. 447, no. 7144, pp. 573–576, May 2007.
[22] S. Sugahara and J. Nitta, “Spin-Transistor Electronics: An Overview and Outlook,” *Proc. IEEE*, vol. 98, no. 12, pp. 2124–2154, 2010.
[23] M. N. Baibich, J. M. Broto, A. Fert, F. N. Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, “Giant Magnetoresistance of (001)Fe/(001)Cr Magnetic Superlattices,” *Phys. Rev. Lett.*, vol. 61, no. 21, pp. 2472–2475, Nov. 1988.
[24] S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. M. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, “Tunnel magnetoresistance of 604% at 300K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature,” *Appl. Phys. Lett.*, vol. 93, no. 8, p. 082508, Aug. 2008.

[25] S. Datta and B. Das, “Electronic analog of the electro-optic modulator,” *Appl. Phys. Lett.*, vol. 56, no. 7, pp. 665–667, Feb. 1990.
[26] R. Jansen, S. P. Dash, S. Sharma, and B. C. Min, “Silicon spintronics with ferromagnetic tunnel devices,” *Semicond. Sci. Technol.*, vol. 27, no. 8, p. 083001, Aug. 2012.
[27] S. Sugahara and M. Tanaka, “A spin metal–oxide–semiconductor field-effect transistor using half-metallic-ferromagnet contacts for the source and drain,” *Appl. Phys. Lett.*, vol. 84, no. 13, pp. 2307–2309, Mar. 2004.
[28] G. Vellianitis, G. Doornbos, B. Duriez, T. M. Shen, C. C. Wu, R. Oxland, K. Bhuwalka, M. Holland, T. L. Lee, and C. Wann, “Demonstration of scaled Ge p-channel FinFETs integrated on Si,” in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 23–5.
[29] W. Chern, P. Hashemi, J. T. Teherani, T. Yu, Y. Dong, G. Xia, D. A. Antoniadis, and J. L. Hoyt, “High mobility high-κ-all-around asymmetrically-strained Germanium nanowire trigate p-MOSFETs,” in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 16–5.
[30] C.-W. Chen, C.-T. Chung, G.-L. Luo, and C.-H. Chien, “Body-Tied Germanium FinFETs Directly on a Silicon Substrate,” *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1678–1680, Dec. 2012.
[31] J. Nah, E.-S. Liu, K. M. Varahramyan, D. Shahrjerdi, S. K. Banerjee, and E. Tutuc, “Scaling Properties of Ge-SiGe Core -Shell Nanowire Field-Effect Transistors,” *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 491–495, 2010.
[32] K. M. Varahramyan, D. Ferrer, E. Tutuc, and S. K. Banerjee, “Band engineered epitaxial Ge–SixGe1−x core-shell nanowire heterostructures,” *Appl. Phys. Lett.*, vol. 95, no. 3, pp. 033101–033101–3, Jul. 2009.
[33] J. Nah, E.-S. Liu, K. M. Varahramyan, and E. Tutuc, “Ge-SiGe Core-Shell Nanowire Tunneling Field-Effect Transistors,” *IEEE Trans. Electron Devices*, vol. 57, no. 8, pp. 1883–1888, 2010.
[34] S. E. Mohney, Y. Wang, M. A. Cabassi, K. K. Lew, S. Dey, J. M. Redwing, and T. S. Mayer, “Measuring the specific contact resistance of contacts to semiconductor nanowires,” *Solid-State Electron.*, vol. 49, no. 2, pp. 227–232, Feb. 2005.
[35] J. Nah, E.-S. Liu, K. M. Varahramyan, D. Dillen, S. McCoy, J. Chan, and E. Tutuc, “Enhanced-Performance Germanium Nanowire Tunneling Field-Effect Transistors Using Flash-Assisted Rapid Thermal Process,” *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1359–1361, 2010.
[36] M. Jamil, J. Oh, M. Ramon, S. Kaur, P. Majhi, E. Tutuc, and S. K. Banerjee, “High-Mobility TaN/ /Ge(111) n-MOSFETs With RTO-Grown Passivation Layer,” *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1208–1210, 2010.
[37] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, “Fermi-level pinning and charge neutrality level in germanium,” *Appl. Phys. Lett.*, vol. 89, no. 25, pp. 252110–252110–3, Dec. 2006.

[38] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Appl. Phys. Lett.*, vol. 91, no. 12, pp. 123123–123123–3, Sep. 2007.

[39] C.-T. Chung, C.-W. Chen, J.-C. Lin, C.-C. Wu, C.-H. Chien, G.-L. Luo, C.-C. Kei, and C.-N. Hsiao, "Epitaxial Germanium on SOI Substrate and Its Application of Fabricating High $rm I_rm ON/rm I_rm OFF$ Ratio Ge FinFETs," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1878–1883, 2013.

[40] S.-H. Hsu, H.-C. Chang, C.-L. Chu, Y.-T. Chen, W.-H. Tu, F. J. Hou, C. H. Lo, P.-J. Sung, B.-Y. Chen, and G.-W. Huang, "Triangular-channel Ge NFETs on Si with (111) sidewall-enhanced I on and nearly defect-free channels," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 23–6.

[41] H. Mehrer, *Diffusion in Solids - Fundamentals, Methods, Materials, Diffusion-Controlled Processes*, 1st ed. Springer, 2007.

[42] G. Hellings, G. Eneman, J. Mitard, K. Martens, W.-E. Wang, T. Hoffmann, M. Meuris, and K. De Meyer, "A Fast and Accurate Method to Study the Impact of Interface Traps on Germanium MOS Performance," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 938–944, Apr. 2011.

[43] Y.-S. Jean and P. D. Ching-Yuan Wu, "The threshold-voltage model of MOSFET devices with localized interface charge," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 441–447, 1997.

[44] E. G. Ioannidis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, and J. Jomaah, "Effect of Localized Interface Charge on the Threshold Voltage of Short-Channel Undoped Symmetrical Double-Gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 433–440, 2011.

[45] A. A. Mutlu and M. Rahman, "Two-dimensional analytical model for drain induced barrier lowering (DIBL) in short channel MOSFETs," in *Proceedings of the IEEE Southeastcon 2000*, 2000, pp. 340–344.

[46] A. Rahman, J. Guo, S. Datta, and M. S. Lundstorm, "Theory of ballistic nanotransistors," *IEEE Trans. Electron Devices*, vol. 50, no. 9, pp. 1853–1864, 2003.

[47] D. C. Dillen, K. M. Varahramyan, C. M. Corbet, and E. Tutuc, "Raman spectroscopy and strain mapping in individual Ge-Si_xGe_{1-x} core-shell nanowires," *Phys. Rev. B*, vol. 86, no. 4, p. 045311, Jul. 2012.

[48] R. Zhang, P.-C. Huang, J.-C. Lin, N. Taoka, M. Takenaka, and S. Takagi, "High-Mobility Ge p- and n-MOSFETs With 0.7-nm EOT Using Gate Stacks Fabricated by Plasma Postoxidation," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 927–934, 2013.

[49] C.-T. Chung, C.-W. Chen, J.-C. Lin, C.-C. Wu, C.-H. Chien, and G.-L. Luo, "First experimental Ge CMOS FinFETs directly on SOI substrate," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 16–4.

[50] E.-S. Liu, D. C. Dillen, J. Nah, B. Fallahazad, K. Kim, and E. Tutuc, "Realization and Scaling of Core-Shell Nanowire n-FETs," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4027–4033, 2013.

[51] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi, "Evidence of low interface trap density in GeO2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *Appl. Phys. Lett.*, vol. 93, no. 3, pp. 032104–032104–3, Jul. 2008.
[52] C. H. Lee, T. Nishimura, T. Tabata, S. K. Wang, K. Nagashio, K. Kita, and A. Toriumi, "Ge MOSFETs performance: Impact of Ge interface passivation," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 18.1.1–18.1.4.
[53] E. Tsymbal and I. Zutic, *Handbook of Spin Transport and Magnetism*. .
[54] A. Fert, "Nobel Lecture: Origin, development, and future of spintronics," *Rev. Mod. Phys.*, vol. 80, no. 4, pp. 1517–1530, 2008.
[55] P. A. Grünberg, "Nobel Lecture: From spin waves to giant magnetoresistance and beyond," *Rev. Mod. Phys.*, vol. 80, no. 4, pp. 1531–1540, Dec. 2008.
[56] J. Barnaś, A. Fuss, R. E. Camley, P. Grünberg, and W. Zinn, "Novel magnetoresistance effect in layered magnetic structures: Theory and experiment," *Phys. Rev. B*, vol. 42, no. 13, pp. 8110–8120, Nov. 1990.
[57] C. Chappert, A. Fert, and F. N. Van Dau, "The emergence of spin electronics in data storage," *Nat. Mater.*, vol. 6, no. 11, pp. 813–823, Nov. 2007.
[58] J. S. Moodera, L. R. Kinder, T. M. Wong, and R. Meservey, "Large Magnetoresistance at Room Temperature in Ferromagnetic Thin Film Tunnel Junctions," *Phys. Rev. Lett.*, vol. 74, no. 16, pp. 3273–3276, Apr. 1995.
[59] S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S.-H. Yang, "Giant tunnelling magnetoresistance at room temperature with MgO (100) tunnel barriers," *Nat. Mater.*, vol. 3, no. 12, pp. 862–867, Dec. 2004.
[60] S. Yuasa, A. Fukushima, H. Kubota, Y. Suzuki, and K. Ando, "Giant tunneling magnetoresistance up to 410% at room temperature in fully epitaxial Co/MgO/Co magnetic tunnel junctions with bcc Co(001) electrodes," *Appl. Phys. Lett.*, vol. 89, no. 4, p. 042505, Jul. 2006.
[61] S. Mao, Y. Chen, F. Liu, X. Chen, B. Xu, P. Lu, M. Patwari, H. Xi, C. Chang, B. Miller, D. Menard, B. Pant, J. Loven, K. Duxstad, S. Li, Z. Zhang, A. Johnston, R. Lamberton, M. Gubbins, T. McLaughlin, J. Gadbois, J. Ding, B. Cross, S. Xue, and P. Ryan, "Commercial TMR heads for hard disk drives: characterization and extendibility at 300 gbit/in2," *IEEE Trans. Magn.*, vol. 42, no. 2, pp. 97–102, Feb. 2006.
[62] J. Åkerman, "Toward a Universal Memory," *Science*, vol. 308, no. 5721, pp. 508–510, Apr. 2005.
[63] K. L. Wang, J. G. Alzate, and P. K. Amiri, "Low-power non-volatile spintronic memory: STT-RAM and beyond," *J. Phys. Appl. Phys.*, vol. 46, no. 7, p. 074003, Feb. 2013.
[64] S. A. Crooker, J. J. Baumberg, F. Flack, N. Samarth, and D. D. Awschalom, "Terahertz Spin Precession and Coherent Transfer of Angular Momenta in Magnetic Quantum Wells," *Phys. Rev. Lett.*, vol. 77, no. 13, pp. 2814–2817, Sep. 1996.

[65] G. Feher, "Electron Spin Resonance Experiments on Donors in Silicon. I. Electronic Structure of Donors by the Electron Nuclear Double Resonance Technique," *Phys. Rev.*, vol. 114, no. 5, pp. 1219–1244, Jun. 1959.
[66] D. K. Wilson and G. Feher, "Electron Spin Resonance Experiments on Donors in Silicon. III. Investigation of Excited States by the Application of Uniaxial Stress and Their Importance in Relaxation Processes," *Phys. Rev.*, vol. 124, no. 4, pp. 1068–1083, Nov. 1961.
[67] M. Johnson and R. H. Silsbee, "Spin-injection experiment," *Phys. Rev. B*, vol. 37, no. 10, pp. 5326–5335, Apr. 1988.
[68] M. Costache, M. Zaffalon, and B. van Wees, "Spin accumulation probed in multiterminal lateral all-metallic devices," *Phys. Rev. B*, vol. 74, no. 1, Jul. 2006.
[69] P. V. Dorpe, Z. Liu, W. V. Roy, V. F. Motsnyi, M. Sawicki, G. Borghs, and J. D. Boeck, "Very high spin polarization in GaAs by injection from a (Ga,Mn)As Zener diode," *Appl. Phys. Lett.*, vol. 84, no. 18, pp. 3495–3497, Apr. 2004.
[70] L. E. Hueso, J. M. Pruneda, V. Ferrari, G. Burnell, J. P. Valdés-Herrera, B. D. Simons, P. B. Littlewood, E. Artacho, A. Fert, and N. D. Mathur, "Transformation of spin information into large electrical signals using carbon nanotubes," *Nature*, vol. 445, no. 7126, pp. 410–413, Jan. 2007.
[71] R. Fiederling, M. Keim, G. Reuscher, W. Ossau, G. Schmidt, A. Waag, and L. W. Molenkamp, "Injection and detection of a spin-polarized current in a light-emitting diode," *Nature*, vol. 402, no. 6763, pp. 787–790, Dec. 1999.
[72] Y. Ohno, D. K. Young, B. Beschoten, F. Matsukura, H. Ohno, and D. D. Awschalom, "Electrical spin injection in a ferromagnetic semiconductor heterostructure," *Nature*, vol. 402, no. 6763, pp. 790–792, Dec. 1999.
[73] G. Schmidt, D. Ferrand, L. W. Molenkamp, A. T. Filip, and B. J. Van Wees, "Fundamental obstacle for electrical spin injection from a ferromagnetic metal into a diffusive semiconductor," *Phys. Rev. B*, vol. 62, no. 8, pp. R4790–R4793, 2000.
[74] A. Fert and H. Jaffrès, "Conditions for efficient spin injection from a ferromagnetic metal into a semiconductor," *Phys. Rev. B*, vol. 64, no. 18, Oct. 2001.
[75] J. Fabian and I. Zutic, "The standard model of spin injection," *ArXiv09032500 Cond-Mat*, Mar. 2009.
[76] W. H. Butler, X.-G. Zhang, T. C. Schulthess, and J. M. MacLaren, "Spin-dependent tunneling conductance of Fe|MgO|Fe sandwiches," *Phys. Rev. B*, vol. 63, no. 5, p. 054416, Jan. 2001.
[77] J. Faure-Vincent, C. Tiusan, E. Jouguelet, F. Canet, M. Sajieddine, C. Bellouard, E. Popova, M. Hehn, F. Montaigne, and A. Schuhl, "High tunnel magnetoresistance in epitaxial Fe/MgO/Fe tunnel junctions," *Appl. Phys. Lett.*, vol. 82, no. 25, pp. 4507–4509, Jun. 2003.
[78] X.-G. Zhang and W. H. Butler, "Large magnetoresistance in bcc Co/MgO/Co and FeCo/MgO/FeCo tunnel junctions," *Phys. Rev. B*, vol. 70, no. 17, p. 172407, Nov. 2004.

[79] F. A. Zwanenburg, D. W. van der Mast, H. B. Heersche, L. P. Kouwenhoven, and E. P. A. M. Bakkers, "Electric Field Control of Magnetoresistance in InP Nanowires with Ferromagnetic Contacts," *Nano Lett.*, vol. 9, no. 7, pp. 2704–2709, Jul. 2009.
[80] C. Gould, C. Rüster, T. Jungwirth, E. Girgis, G. M. Schott, R. Giraud, K. Brunner, G. Schmidt, and L. W. Molenkamp, "Tunneling Anisotropic Magnetoresistance: A Spin-Valve-Like Tunnel Magnetoresistance Using a Single Magnetic Layer," *Phys. Rev. Lett.*, vol. 93, no. 11, p. 117203, Sep. 2004.
[81] G. Feher and E. A. Gere, "Electron Spin Resonance Experiments on Donors in Silicon. II. Electron Spin Relaxation Effects," *Phys. Rev.*, vol. 114, no. 5, pp. 1245–1256, Jun. 1959.
[82] D. K. Wilson, "Electron Spin Resonance Experiments on Shallow Donors in Germanium," *Phys. Rev.*, vol. 134, no. 1A, pp. A265–A286, Apr. 1964.
[83] Y. Song and H. Dery, "Analysis of phonon-induced spin relaxation processes in silicon," *Phys. Rev. B*, vol. 86, no. 8, p. 085201, Aug. 2012.
[84] M. W. Wu, J. H. Jiang, and M. Q. Weng, "Spin dynamics in semiconductors," *Phys. Rep.*, vol. 493, no. 2–4, pp. 61–236, Aug. 2010.
[85] M. Dyakonov and V. Perel, "Spin Relaxation of Conduction Electrons in Noncentrosymmetric Semiconductors," *Sov Phys Solid State*, vol. 13, no. 12, pp. 3023–3026, 1972.
[86] R. J. Elliott, "Theory of the Effect of Spin-Orbit Coupling on Magnetic Resonance in Some Semiconductors," *Phys. Rev.*, vol. 96, no. 2, pp. 266–279, Oct. 1954.
[87] F. Seitz and D. Turnbull, *Solid state physics*. New York, Academic Press, 1955.
[88] P. Li, Y. Song, and H. Dery, "Intrinsic spin lifetime of conduction electrons in germanium," *Phys. Rev. B*, vol. 86, no. 8, p. 085202, Aug. 2012.
[89] P. Li, J. Li, L. Qing, H. Dery, and I. Appelbaum, "Anisotropy-Driven Spin Relaxation in Germanium," *Phys. Rev. Lett.*, vol. 111, no. 25, p. 257204, Dec. 2013.
[90] J.-M. Tang, B. T. Collins, and M. E. Flatté, "Electron spin-phonon interaction symmetries and tunable spin relaxation in silicon and germanium," *Phys. Rev. B*, vol. 85, no. 4, p. 045202, Jan. 2012.
[91] E. Tutuc, J. O. Chu, J. A. Ott, and S. Guha, "Doping of germanium nanowires grown in presence of PH3," *Appl. Phys. Lett.*, vol. 89, no. 26, p. 263101, Dec. 2006.
[92] D. E. Perea, E. R. Hemesath, E. J. Schwalbach, J. L. Lensch-Falk, P. W. Voorhees, and L. J. Lauhon, "Direct measurement of dopant distribution in an individual vapour–liquid–solid nanowire," *Nat. Nanotechnol.*, vol. 4, no. 5, pp. 315–319, May 2009.
[93] K. Martens, A. Firrincieli, R. Rooyackers, B. Vincent, R. Loo, S. Locorotondo, E. Rosseel, T. Vandeweyer, G. Hellings, B. De Jaeger, M. Meuris, P. Favia, H. Bender, B. Douhard, J. Delmotte, W. Vandervorst, E. Simoen, G. Jurczak, D. Wouters, and J. A. Kittl, "Record low contact resistivity to n-type Ge for CMOS

and memory applications," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 18.4.1–18.4.4.

[94] J.-Y. J. Lin, A. M. Roy, and K. C. Saraswat, "Reduction in Specific Contact Resistivity to Ge Using Interfacial Layer," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1541–1543, 2012.

[95] K. Gallacher, P. Velha, D. J. Paul, I. MacLaren, M. Myronov, and D. R. Leadley, "Ohmic contacts to n-type germanium with low specific contact resistivity," *Appl. Phys. Lett.*, vol. 100, no. 2, p. 022113, Jan. 2012.

[96] J. Oh, I. Ok, C.-Y. Kang, M. Jamil, S.-H. Lee, W.-Y. Loh, J. Huang, B. Sassman, L. Smith, S. Parthasarathy, B. E. Coss, W.-H. Choi, H.-D. Lee, M. Cho, S. K. Banerjee, P. Majhi, P. D. Kirsch, H.-H. Tseng, and R. Jammy, "Mechanisms for low on-state current of Ge (SiGe) nMOSFETs: A comparative study on gate stack, resistance, and orientation-dependent effective masses," in *2009 Symposium on VLSI Technology*, 2009, pp. 238–239.

[97] J. Robertson, "High dielectric constant oxides," *Eur. Phys. J. - Appl. Phys.*, vol. 28, no. 03, pp. 265–291, 2004.

[98] S. Ikeda, J. Hayakawa, Y. M. Lee, F. Matsukura, Y. Ohno, T. Hanyu, and H. Ohno, "Magnetic Tunnel Junctions for Spintronic Memories and Beyond," *IEEE Trans. Electron Devices*, vol. 54, no. 5, pp. 991–1002, 2007.

[99] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, and H. Ohno, "A perpendicular-anisotropy CoFeB–MgO magnetic tunnel junction," *Nat. Mater.*, vol. 9, no. 9, pp. 721–724, Sep. 2010.

[100] X. Cao, D. S. Macintyre, S. Thoms, X. Li, H. Zhou, C. D. W. Wilkinson, M. Holland, L. Donaldson, F. McEwan, H. McLellend, and I. Thayne, "Low damage sputter deposition of tungsten for decanano compound semiconductor transistors," *J. Vac. Sci. Technol. B*, vol. 23, no. 6, pp. 3138–3142, Dec. 2005.

[101] H. Takeuchi, M. She, K. Watanabe, and T.-J. King, "Damage-Less Sputter Depositions by Plasma Charge Trap for Metal Gate Technologies," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 3, pp. 350–354, 2005.

[102] B. B. Burton, D. N. Goldstein, and S. M. George, "Atomic Layer Deposition of MgO Using Bis(ethylcyclopentadienyl)magnesium and H2O," *J. Phys. Chem. C*, vol. 113, no. 5, pp. 1939–1946, Feb. 2009.

[103] W. F. Brinkman, R. C. Dynes, and J. M. Rowell, "Tunneling Conductance of Asymmetrical Barriers," *J. Appl. Phys.*, vol. 41, no. 5, pp. 1915–1921, 1970.

[104] B. Oliver, Q. He, X. Tang, and J. Nowak, "Tunneling criteria and breakdown for low resistive magnetic tunnel junctions," *J. Appl. Phys.*, vol. 94, no. 3, pp. 1783–1786, Jul. 2003.

[105] B. J. Jönsson-Åkerman, R. Escudero, C. Leighton, S. Kim, I. K. Schuller, and D. A. Rabson, "Reliability of normal-state current–voltage characteristics as an indicator of tunnel-junction barrier quality," *Appl. Phys. Lett.*, vol. 77, no. 12, pp. 1870–1872, Sep. 2000.

[106] C. H. Li, G. Kioseoglou, O. M. J. van ‘t Erve, P. E. Thompson, and B. T. Jonker, “Electrical spin injection into Si(001) through a SiO2 tunnel barrier,” *Appl. Phys. Lett.*, vol. 95, no. 17, p. 172102, Oct. 2009.
[107] C. H. Li, O. M. J. van ’t Erve, and B. T. Jonker, “Electrical injection and detection of spin accumulation in silicon at 500 K with magnetic metal/silicon dioxide contacts,” *Nat. Commun.*, vol. 2, p. 245, Mar. 2011.
[108] M. J. Donahue and D. G. Porter, “OOMMF User’s Guide, Version 1.0.” .
[109] M. Johnson and R. Silsbee, “Calculation of nonlocal baseline resistance in a quasi-one-dimensional wire,” *Phys. Rev. B*, vol. 76, no. 15, Oct. 2007.
[110] C. Józsa, M. Popinciuc, N. Tombros, H. T. Jonkman, and B. J. van Wees, “Electronic Spin Drift in Graphene Field-Effect Transistors,” *Phys. Rev. Lett.*, vol. 100, no. 23, p. 236603, Jun. 2008.
[111] I. Appelbaum, B. Huang, and D. J. Monsma, “Electronic measurement and control of spin transport in silicon,” *Nature*, vol. 447, no. 7142, pp. 295–298, May 2007.
[112] S. P. Dash, S. Sharma, R. S. Patel, M. P. de Jong, and R. Jansen, “Electrical creation of spin polarization in silicon at room temperature,” *Nature*, vol. 462, no. 7272, pp. 491–494, Nov. 2009.
[113] L.-T. Chang, W. Han, Y. Zhou, J. Tang, I. A. Fischer, M. Oehme, J. Schulze, R. K. Kawakami, and K. L. Wang, “Comparison of spin lifetimes in n-Ge characterized between three-terminal and four-terminal nonlocal Hanle measurements,” *Semicond. Sci. Technol.*, vol. 28, no. 1, p. 015018, Jan. 2013.
[114] P. J. Zomer, M. H. D. Guimarães, N. Tombros, and B. J. van Wees, “Long-distance spin transport in high-mobility graphene on hexagonal boron nitride,” *Phys. Rev. B*, vol. 86, no. 16, p. 161416, Oct. 2012.
[115] D. Rugar, H. J. Mamin, P. Guethner, S. E. Lambert, J. E. Stern, I. McFadyen, and T. Yogi, “Magnetic force microscopy: General principles and application to longitudinal recording media,” *J. Appl. Phys.*, vol. 68, no. 3, pp. 1169–1183, Aug. 1990.
[116] W. Han, Y. Zhou, Y. Wang, Y. Li, J. J. I. Wong, K. Pi, A. G. Swartz, K. M. McCreary, F. Xiu, K. L. Wang, J. Zou, and R. K. Kawakami, “Growth of single-crystalline, atomically smooth MgO films on Ge(0 0 1) by molecular beam epitaxy,” *J. Cryst. Growth*, vol. 312, no. 1, pp. 44–47, Dec. 2009.
[117] D. Petti, M. Cantoni, C. Rinaldi, S. Brivio, R. Bertacco, J. Gazquez, and M. Varela, “Sharp Fe/MgO/Ge(001) epitaxial heterostructures for tunneling junctions,” *J. Appl. Phys.*, vol. 109, no. 8, p. 084909, Apr. 2011.
[118] J. Nah, E.-S. Liu, D. Shahrjerdi, K. M. Varahramyan, S. K. Banerjee, and E. Tutuc, “Realization of dual-gated Ge–SixGe1−x core-shell nanowire field effect transistors with highly doped source and drain,” *Appl. Phys. Lett.*, vol. 94, no. 6, pp. 063117–063117–3, Feb. 2009.
[119] S. Takagi, R. Zhang, T. Hoshii, N. Taoka, and M. Takenaka, “MOS Interface Control Technologies for III-V/Ge Channel MOSFETs,” *ECS Trans.*, vol. 41, no. 3, pp. 3–20, Oct. 2011.

[120] O. Weber, Y. Bogumilowicz, T. Ernst, J.-M. Hartmann, F. Ducroquet, F. Andrieu, C. Dupré, L. Clavelier, C. Le Royer, N. Cherkashin, M. Hytch, D. Rouchon, H. Dansas, A.-M. Papon, V. Carron, C. Tabone, and S. Deleonibus, "Strained Si and Ge MOSFETs with high-k/metal gate stack for high mobility dual channel CMOS," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 137–140.

[121] R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, "High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (Vcc = 0.5 V) III-V CMOS architecture," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 6.7.1–6.7.4.

[122] D. Kuzum, A. J. Pethe, T. Krishnamohan, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Interface-Engineered Ge (100) and (111), N- and P-FETs with High Mobility," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 723–726.

[123] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P. A. Pianetta, H.-S. P. Wong, and K. C. Saraswat, "High-Mobility Ge N-MOSFETs and Mobility Degradation Mechanisms," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 59–66, 2011.

[124] M. Jamil, J. Mantey, E. U. Onyegam, G. D. Carpenter, E. Tutuc, and S. K. Banerjee, "High-Performance Ge nMOSFETs With n+-p Junctions Formed by "Spin-On Dopant"," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1203–1205, 2011.

[125] A. M. Roy, J.-Y. J. Lin, and K. C. Saraswat, "Specific Contact Resistivity of Tunnel Barrier Contacts Used for Fermi Level Depinning," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1077–1079, 2010.

[126] H.-Y. Yu, M. Kobayashi, J.-H. Park, Y. Nishi, and K. C. Saraswat, "Novel Germanium n-MOSFETs With Raised Source/Drain on Selectively Grown Ge on Si for Monolithic Integration," *IEEE Electron Device Lett.*, vol. 32, no. 4, pp. 446–448, Apr. 2011.

[127] M. Saitoh, Y. Nakabayashi, K. Uchida, and T. Numata, "Short-Channel Performance Improvement by Raised Source/Drain Extensions With Thin Spacers in Trigate Silicon Nanowire MOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 273–275, Mar. 2011.

[128] V. Ramanjaneyulu, S. Baishya, and R. H. Laskar, "Optimization consideration of undoped raised source/drain FinFET with effective SCE control," in *Mechanical and Electronics Engineering (ICMEE), 2010 2nd International Conference on*, 2010, vol. 1, pp. V1–150.

[129] E.-S. Liu, J. Nah, K. M. Varahramyan, and E. Tutuc, "Lateral Spin Injection in Germanium Nanowires," *Nano Lett.*, vol. 10, no. 9, pp. 3297–3301, Sep. 2010.