Copyright

by

Yujia Zhai

2014

The Dissertation Committee for Yujia Zhai Certifies that this is the approved version of the following dissertation:

Novel 3-D IC Technology

Committee:

Sanjay Banerjee, Supervisor

Grant C. Willson, Co-Supervisor

Frank Register

Rajesh Rao

Emanuel Tutuc

Novel 3-D IC Technology

by

Yujia Zhai, B.S.; M.S.E

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

MAY, 2014

Dedicated to

My family

Acknowledgements

I would like to thank all the people who have helped and inspired me during my Ph.D. I want to express my deepest gratitude to my advisor, Dr. Sanjay Banerjee, for his guidance, assistance, and support, during my research and study. Over the past years his mentorship has been far beyond science and discovery: he has taught me not only the professional knowledge but also integrity, persistence and excellence. I have been fortunate enough to have his supervision during my Ph.D. studies.

I also appreciate my co-advisor, Dr. Grant C. Willson, for his constant advice and encouragement during my graduate study. The valuable discussions always inspired me. Without his knowledge and assistance this study would not have been successful.

I would like to acknowledge my other committee members, Dr. Frank Register, Dr. Emanuel Tutuc and Dr. Rajesh Rao for serving as the dissertation committee members.

I also appreciate the support from Applied Novel Device, Inc, especially Leo Mathew. His suggestions and technical support made this Ph.D. work better.

Special thanks go to my research team members. I really appreciate the help and suggestions from the senior group members: Dr. Shan Tang, Dr. Mustafa Jamil, Dr. Fahmida Ferdousi and Dr. Michael Ramon. They trained me on device fabrication, and taught me the electrical characterization skills. I also appreciate all the valuable support from the current group members.

All colleagues at the Microelectronics Research Center made it a friendly place to work. In particular, I would like to thank Aiting Jiang, who gives me magnificent help on

my research. Without his assistance, the fabrication process could not be set up in such a short time.

I am also thankful to the entire MER staff, especially Jean Toll, Marylene Palard, Bill Ostler, Jesse James, Gabriel Glenn, Ricardo Garcia, Johnny Johnson, Joyce Kokes, and Gerlinde Sehne, for their continuous help and support.

Lastly and most importantly, I wish to express my love and gratitude to my beloved family for their understanding through the duration of my studies.

Novel 3-D IC Technology

Yujia Zhai, B.S.; M.S.E.
The University of Texas at Austin, 2014

Supervisor: Sanjay Banerjee
Co-supervisor: C.Grant Willson

For many decades silicon based CMOS technology has made continual increase in drive current to achieve higher speed and lower power by scaling the gate length and the gate insulator thickness. The scaling becomes increasingly challenging because the devices are approaching physical quantum limits. Three-dimensional electronic devices, such as double gate, tri-gate and nanowire field-effect-transistors (FETs) provide an alternative solution because the ultra-thin fin or nanowire provides better electrostatic control of the device channel. Also high-κ oxides lower the gate leakage current significantly, due to larger thickness for the same equivalent oxide thickness (EOT) compared with SiO_2 beyond the 22 nm node. Moreover, metal gate that avoids the poly-depletion effect in poly-Si gate has become mainstream semiconductor technology.

The enabler technologies for high-κ / metal gate 3D transistors include fabrication of high quality, vertical nanowire arrays, conformal metal and dielectric deposition and vertical patterning. One of the main focuses of this dissertation is developing a fabrication process flow to realize high performance MOSFETs with high-κ oxide and metal gate on vertical silicon nanowire arrays. A variety of approaches to fabricating highly ordered silicon nanowire arrays have been achieved. Deep silicon etching process

was developed and optimized for nanowire FETs. Process integration and patterning mythologies for high-κ / metal gate were investigated and accomplished. 3-D electronic devices including nanowire capacitors, nanowire FETs and double gate MOSFETs for power applications were fabricated and characterized.

The second part of this dissertation is about flexible electronics. Mechanically flexible integrated circuits (ICs) have gained increasing attention in recent years with emerging markets in portable electronics. Although a number of thin-film-transistor (TFT) IC solutions have been reported, challenges still remain for fabrication of inexpensive, high performance flexible devices. We report a simple and straightforward solution: mechanically exfoliating a thin Si film containing ICs. Transistors and circuits can be pre-fabricated on bulk silicon wafer with conventional CMOS process flow without additional temperature or process limitations. The short channel MOSFETs exhibit similar electrical performance before and after exfoliation. This exfoliation process also provides a fast and economical approach to produce thinned silicon wafers, which is a key enabler for three-dimensional (3D) silicon integration based on Through Silicon Vias (TSVs).

Table of Contents

List of Tables xi

List of Figures xii

Chapter 1 Introduction 1

1.1 Overview of 3D nanowire capacitor and nanowire MOSFETs 1

1.2 Nanowire array fabrication and patterning techniques 5

1.3 Overview of power MOSFET 6

1.4 Overview of 3D flexible electronics 8

Chapter 2 Silicon nanowire array and nanowire devices 10

2.1 Vapor-Liquid-Solid silicon nanowire growth and patterning 10

2.2 Patterned silicon nanowire array by deep silicon etching 12

2.3 Single crystal nanowire capacitor 14

Chapter 3 Gate-All-Around Nanowire FET 22

3.1 Integration challenges for GAA-nanowire FET 22

3.1.1 Etching optimization for high quality nanowires 22

3.1.2 Plasma Enhanced ALD as gate metal. 28

3.1.3 Gate isotropic etch and vertical patterning 32

3.2 Process development Gate-All-Around nanowire FETs 38

3.3 Device characterization and discussion 49

Chapter 4 Double gate power MOSFET Introduction 56

4.1 Process development of vertically diffused finFET 56

4.2 Device characterization and discussion 61

Chapter 5 Flexible thin-film transistors exfoliated from bulk wafer 70

5.1 Process review of flexible electronics 70

5.2 Process of wafer exfoliation 73

5.3 Performance of exfoliated thin-film transistors 79

Chapter 6 Future work 86
6.1 Future work for nanowire FET 86
6.2 Thinned wafer for 3D-IC 86

Appendix A: Process flow of vertical Si nanowire FET......................................88

Appendix B: Process flow of vertically diffused finFET 90

Bibliography 92

Vita…...104

List of Tables

Table 1. 1 Natural length in devices with different geometries[15, 17, 23] 4

Table 3. 1 Process conditions of polymer deposition and silicon etching for each DSE cycle. Tool: PlasmaTherm Silicon deep RIE. 24

Table 3. 2 Process conditions and film qualifications of TiN deposited in N_2 and NH_3 31

Table 3. 3 Materials and etching techniques for the nanowire FET gate metal integration. Successful integration is achieved by utilizing PEALD TiN (NH_3) as the gate metal, PECVD SiO_2 as the gate mask and 1:1:5 SC-1 as the gate metal etchant. 37

Table 3. 4 Parameters and constants for hole mobility extraction in silicon nanowire FETs. 54

Table 4. 1 Implantation and annealing conditions for vertically diffused finFET doping. 57

List of Figures

Figure 1. 1 Evaluation of device geometries as CMOS scale down [24] 4

Figure 1. 2 The cross-sectional view of a LDMOS [35] 6

Figure 1. 3 The cross-sectional view of a VDMOS [36] 7

Figure 1. 4 Schematic of vertical diffused finFET. 8

Figure 2. 1 Cross-sectional SEM image of single crystalline silicon nanowire. 11

Figure 2. 2 a) SFIL/R nano-imprint process flow for patterned nanowire growth. b) Patterned Au dots with SiO_2 barrier. c) Patterned nanowire growth. 12

Figure 2. 3 Silicon nanowire capacitor fabrication process flow 13

Figure 2. 4 (a-d) Si-nanowire array after DSE with 4, 8, 12, and 15 etch cycles, respectively, resulting in nanowire arrays with an increasing height. ... 14

Figure 2. 5 a) 70° tilted SEM image of Si-nanowires after ALD Al_2O_3 and sputtered TaN. b) and c) Cross-section TEM image of Si-nanowire head after ALD Al_2O_3 and sputtered TaN 15

Figure 2. 6 SEM images of Si-nanowire: a) top view; b) 45° tilted view 16

Figure 2. 7 C-V measurements of conventional planar capacitor and Si-nanowire capacitors with nanowire etch cycles of 4, 8, and 12, delivering nanowire arrays with heights between 130nm to 450nm. The Al_2O_3 dielectric thickness is 24 nm for a) and 8 nm for b). 18

Figure 2. 8 C-V measurement results compared with calculated values................. 19

Figure 2. 9 Dielectric leakage current for conventional planar capacitor and Si-nanowire capacitors with nanowire etch cycles of 4, 8, and 12. Al_2O_3 dielectric thickness is 24nm for a) and 8 nm for b). 20

Figure 2. 10 Time-Dependent Dielectric Breakdown measurement on Si-nanowire capacitors compared with conventional planar capacitors. 21

Figure 3. 1 High aspect ratio nanowires are achieved by deep silicon etch with metal salicide mask. The aspect ratio is more than 20 on nanowires. The defect in center post probably results from metal out-diffusion during salicide anneal. 23

Figure 3. 2 Cross-sectional SEM images of deep silicon etching. Samples were etched with different etch/deposition ratio and sidewall undercut angels were evaluated. Result shows that the combination of 1.0 sec deposition and 2.0 sec etching yield almost 90° vertical sidewall. 25

Figure 3. 3 Etched sidewall morphology optimization. The original recipe has 2.0 sec deposition time and 1.0 sec etch time in each cycle. Scallops are observed on the etched sidewall. The optimized recipe reduces the deposition time to 1.0 sec and the etch time to 0.5 sec, and scallops are minimized on the etched sidewall. Note that the etch/deposition ratio is kept as a constant (2) in the process optimization. 26

Figure 3. 4 Recipe optimization result for silicon nanowire etching. The left image a) shows the nanowires etched with the original recipe. Scallops are observed on the sidewall of nanowires as well as undercutting defect. Etching process undercuts the nanowire bottom as the cycle number

increases. The right image b) shows the nanowires etched with the optimized recipe. Sidewall smoothness is improved and undercutting is minimized. 27

Figure 3. 5 Illustrations of plasma enhanced ALD TiN process in N_2 (a) and NH_3 (b) respectively. Note that NH_3 should be turned off while pulsing TDMAT. 29

Figure 3. 6 C-V characteristics of fabricated MOS capacitors with plasma enhanced ALD TiN as the gate metal 32

Figure 3. 7 Illustration for resist spin-on and etch-back process to vertically pattern the gate metal. 33

Figure 3. 8 Resist spin-on and etch-back process to vertically pattern the gate metal. a) Al_2O_3 and TiN are deposited on nanowires. b) Resist is spun and etched back to define the gate length. c) Exposed TiN is wet etched by SC-1 solution and the resist is removed. 33

Figure 3. 9 Test structures to investigate TiN film conductivity degradation. 35

Figure 3. 10 Measured I-V on TiN gate metal with different test structures of TiN process integration. 36

Figure 3. 11 Schematic of a vertical nanowire field-effect-transistor. 39

Figure 3. 12 Simulated doping concentration for nanowire FETs. 40

Figure 3. 13 Etched silicon nanowire array patterned by e-beam lithography and masked by Ti/Ni salicide. Nanowires height is ~ 720 nm and diameter is ~ 90 nm. Aspect ratio is ~ 1:8. 42

Figure 3. 14 Process flow of nanowire FETs 44

Figure 3. 15 nanowire FET after resist thinning (left) and gate patterning (right). 45

Figure 3. 16 Silicon nanowire FETs with vertical wrapped gate pattern. 46

Figure 3. 17 Tilted SEM image of silicon nanowire FET after PECVD SiO_2 etch. Nanowire cores are exposed on top of the device for the drain metallization.. 47

Figure 3. 18 Top-view microscope image of final device layout. Drain is the top nickel films and gate is buried under SiO_2 inter-metal dielectric. A contact window is opened by photolithography. 48

Figure 3. 19 Cross-sectional SEM image of a nanowire FET. The cross-section that is created by focused ion beam (FIB) cuts through the nanowire core. 49

Figure 3. 20 Measured transfer characteristics of a silicon nanowire FET with 25 nanowires in parallel. 50

Figure 3. 21 Measured output characteristics of silicon nanowire FET with 25 nanowires in parallel. 51

Figure 3. 22 Trans-conductance of silicon nanowire FET measured at V_{DS} = -0.2 V. 52

Figure 3. 23 Low temperature transfer characteristics compared with room temperature. 55

Figure 4. 1 Illustration of process flow for vertically diffused finFET 58

Figure 4. 2 Etched fins after 30 cycles of deep silicon etch. Right image is a 45° tilted SEM image of a vertically diffused finFET with 4 fins. The length of the fin is 15 μm. Left upper is a close-up image of at the tip of an etched fin. The width of the fin is around 70 nm after the salicide annealing. Left Lower is the top view of the device layout.................. 59

Figure 4. 3 Completed vertically diffused finFET. 60

Figure 4. 4 TEM images of the fin cross-section and high magnification image of salicide on top of the fin. 61

Figure 4. 5 Transfer characteristics of fabricated vertically diffused finFETs with 1-fin (a), 2 fins (b), 3 fins (c) and 4 fins (d). 62

Figure 4. 6 ON-current versus fin number in one device. Linear dependence is observed. 63

Figure 4. 7 Output characteristics of vertically diffused finFETs with fin number from 1-4 in (a) to (d), respectively. 64

Figure 4. 8 Transfer characterization comparison of the swapped S/D configuration and the original S/D configuration. 65

Figure 4. 9 Low temperature transfer characteristic comparing with room temperature. V_{DS} = -0.2V 68

Figure 5. 1 Exfoliation process flow: (**A**) Transistors are pre-fabricated on conventional silicon wafer with standard CMOS process flow. (**B**) PECVD Si_3N_4 for passivation. (**C**) E-beam evaporation of thin metal seed layer. (**D**) Electro-chemical plating of Ni on seed layer. (**E**) Thermal expansion mismatch exfoliates the film from wafer. (**F**) Nickel foil is removed by SC-2 solution. 75

Figure 5. 2 (A) Surface roughness of exfoliated thin-film silicon (B) TEM image of microstructure of the exfoliated Si. 76

Figure 5. 3 The variation of stress coefficient f_{mn} for $0 < \bar{y} \leq 1$. The upper inset shows the residual strain ε_0 between Si and Ni layers and the co-

ordinate system used to compute the stress distribution. The lower inset schematically shows the stress distributions in Si and Ni layers after the exfoliation. 78

Figure 5. 4 Image of a bent, flexible integrated circuit with high performance CMOS devices. (A) is flexible IC with the size of 35 mm x 50 mm. (B) shows an 8-inch exfoliated wafer with metal foil. 79

Figure 5. 5 Comparison of transfer characteristics before exfoliation (On-wafer, black curve) and after exfoliation (exfoliated, red curve) with V_{DS} = 0.1 V and 1.0 V. The channel length is 150 nm and width is 10 μm with gate oxide of 20Å SiO_2 for both n-MOSFETs and p-MOSFETs. 81

Figure 5. 6 Comparison of output characteristics before exfoliation (On-wafer, black curve) and after exfoliation (exfoliated, red curve) with V_{GS} from 0.1 V to 1.0 V, in steps of 0.1 V. The channel length is 150nm and width is 10 μm with gate oxide of 20Å SiO_2 for both n-MOS and p-MOS. 82

Figure 5. 7 Gate dielectric leakage current as a function of gate bias. Black curve shows the leakage current before exfoliation (on-wafer), and red curve after exfoliation. 83

Figure 5. 8 Diode I-V characteristics with reverse breakdown voltage. Black curve shows the leakage current before exfoliation (on-wafer), and red curve after exfoliation. 84

Chapter 1 Introduction

1.1 OVERVIEW OF 3D NANOWIRE CAPACITOR AND NANOWIRE MOSFETS

Semiconductor nanowires have gained increasing interest in the last decade since this geometry provides a wide range of 3-dimensional electronic devices [1]. Because of its high aspect ratio, nanowire array or forest can dramatically enhance the effective surface area and is capable of achieving high density storage capacity in a limited silicon real estate, benefiting potential applications such as analog and mixed signal ICs. Analog and mixed signal ICs require on-chip passives with storage capacity in excess of 1 $\mu F/cm^2$, and leakage densities less than $\sim 1x10^{-6}/cm^2$ at a voltage of ~2V. This can be difficult to achieve with planar capacitors. With more aggressive effective oxide thickness (EOT) and a concomitant relaxation of leakage current requirement, these 3D capacitors may be useful for DRAMs also [2]. DRAM capacity or bit density has been increasing by a factor of 4 every three years, whereas, memory cell size has been reduced by almost 1/3 each generation for the sake of cost [3, 4]. Along with scaling down, the reduced voltage pushes the capacity requirements to ensure a constant cell signal [5]. One approach to coping with the dilemma of size vs. capacitance is to reduce insulator thickness and implement high-κ technology [6]. Another approach to obtaining high capacitance is to construct 3-dimensional structures such as stacked capacitors, trenches [7], pillars [8, 9], etc. For example, carbon nanotubes fabricated by bottom-up growth have been utilized to enhance the capacitance[10]. Compared to trench capacitors, the topography of nanowires is more compatible with FinFETs and vertical gate-all-around transistors, which are promising technology solutions for 22nm and beyond[11].

The ongoing scaling-down of electronic devices has become more challenging since dimensions are approaching the physical limits of semiconductors [12]. Short

channel effects, e.g. sub-threshold swing (SS) degradation and drain-induced barrier lowering (DIBL) are caused by the encroachment of electric field line from the drain into the channel region, thereby competing for the available depletion charge. DIBL effectively reduces the barrier between source and drain [13] and consequently reduces the threshold voltage (V_{th}). Fully depleted multiple-gate field-effect-transistors (MuGFETs) that have excellent control of short-channel effects and are compatible with standard CMOS fabrication process have been proposed and under intense research as promising candidates for the next generation of CMOS technology [14-16].

To gain insight into threshold voltage roll-off and sub-threshold characteristics in fully depleted devices, Yan *et. al.* solved Poisson's equation to examine the potential distribution in the channel region:

$$\frac{d^2\Phi}{dx^2}+\frac{d^2\Phi}{dy^2}=\frac{qN_A}{\varepsilon_{Si}}$$

where $0 \le x \le L_{eff}$ and $0 \le y \le t_{Si}$. L_{eff} is the effective channel length, and t_{Si} is silicon film thickness.

A natural length scale λ is introduced to describe the potential distribution:

$$\lambda=\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{Si}t_{ox}}$$

and

$$\phi(x)=\Phi_f(x)-\Phi_{gs}+\frac{qN_A}{\varepsilon_{Si}}\lambda^2$$

Then Poisson's equation can be simplified as :

$$\frac{d^2\phi}{dx^2}-\frac{d^2\phi}{d\lambda^2}=\frac{qN_A}{\epsilon_{Si}}$$

$\phi(x)$ differs from $\Phi_f(x)$ only by a position-independent term. The derivation result indicates that short channel effects can be minimized when effective channel length is much larger than the natural length scale λ [17].

Colinge *et. al.* deduced the natural length scales for single gate, double gate and surrounding gate devices by applying corresponding boundary conditions. The derivation results are presented in Table 1.1. It can be inferred that the scaling requirement is more relaxed for double gate MOSFETs, and further relaxation is obtained by using the gate-all-around structure [15, 18-20]. In this structure, the wrapped gate has better electrostatic control as compared to other gate designs. Fabricated on a cylindrical pillar of silicon, this device has the benefits of both reducing the short channel effects and improving the sub-threshold slope (SS), as well as potentially higher packing densities. Simulation shows that the DIBL and SS can be maintained if scaling laws are followed [21, 22].

Gate geometries	Natural length
Single-gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}}$
Double-gate	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$
Surrounding-gate	$\lambda \approx \sqrt{\frac{\varepsilon_{Si}}{4\varepsilon_{ox}} t_{Si} t_{ox}}$ (square-section) $\lambda = \sqrt{\frac{2\varepsilon_{Si} t_{Si}^2 \ln\left(1+\frac{2t_{ox}}{t_{Si}}\right)+\varepsilon_{ox} t_{Si}^2}{16\varepsilon_{ox}}}$ (circular cross-section)

Table 1. 1 Natural length in devices with different geometries[15, 17, 23]

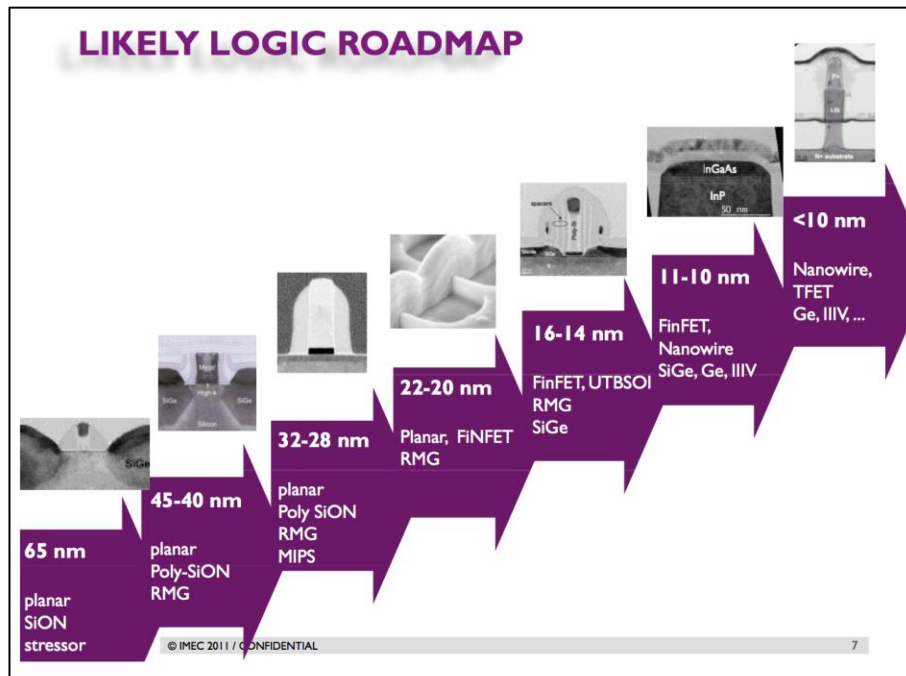
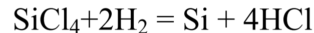


Figure 1. 1 Evaluation of device geometries as CMOS scale down [24].

1.2 NANOWIRE ARRAY FABRICATION AND PATTERNING TECHNIQUES

The approaches to fabricating semiconductor nanowires fall into two categories: bottom-up growth and top-down etching. An intensively studied bottom-up growth technique for silicon nanowire is Vapor-Liquid-Solid (VLS) growth mechanism [25]. According to this mechanism, a metal catalyst forms liquid alloy droplets at high temperature since substrate atoms dissolve into catalyst and melting point is reduced. Anisotropic crystal growth takes place at the liquid/solid interface. The growth is done in a chemical vapor deposition (CVD) chamber at temperatures ranging from 600 to 1000 ^{o}C. The precursors, $SiCl_4$ and H_2, flow into the chamber and react as:



$$SiCl_4+2H_2 = Si + 4HCl$$

The droplets are preferred sinks for the arriving silicon atoms, and continuing incorporation leads to a super-saturation. Consequently, the silicon atoms in the alloy droplets begin to precipitate onto the liquid/solid interface, and finally on the substrate. As a result, anisotropic silicon growth takes place at the interface, elevating the droplets to the top of the crystalline silicon nanowire. The preferred growth direction is <111>, and sometimes also <110> [26, 27]. Selective positioning of the nanowires requires isolating the catalyst in SiO_2 wells, in order to prevent the catalyst from migrating during annealing. [28]

Using selective etching to fabricate silicon nanowires is more straightforward and compatible with modern semiconductor technology. Lithography patterns the hard mask (e.g. silicon nitride) as dot shapes at the location of each nanowire. Subsequent anisotropic etching removes the most of the silicon, except in regions that are protected by dots, and leaves the high aspect ratio nanowires beneath the dots. Optional sacrificial silicon oxidation and HF etching can further thin down the nanowires and improve the surface of sidewalls. However, it is difficult to pattern nanowires with small diameter by

optical lithography, while electron beam writing has low throughput and is not a manufacturable option. We use a simple and manufacturable technique, Step and Flash Imprint Lithography (S-FIL) [29] to produce the core of our semiconductor nanowires.

1.3 Overview of power MOSFET

Various types of mobile telecommunication devices, for example cellphone, personal digital assistant and tablet computer, as well as electric automobile, power electronic devices are gaining in importance. Power MOSFET devices are quite interesting in terms of the fast switching speed and the capability of handling high voltage in such devices [30]. There are two major categories of power MOSFET: laterally diffused MOSFET (LDMOS) and vertically diffused MOSFET (VDMOS or VMOS). The LDMOS（shown in Figure 1.2) is analogous to conventional MOSFET in terms of horizontal current-flow configuration, except that an extended, lightly doped drain region is utilized. The long, lightly doped drain extension acts as a drift-region to support a large voltage drop, enabling power applications. [30-34]

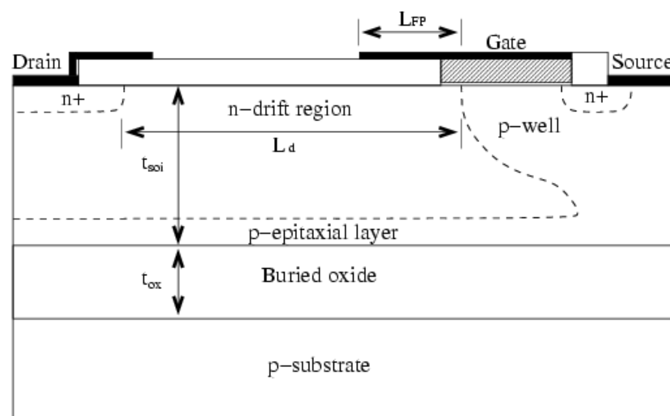


Figure 1. 2 The cross-sectional view of a LDMOS [35]

On the contrary, VDMOS, cross-sectional structure shown in figure 1.2, has a vertical current-flow pattern. Traditionally VDMOS utilizes two successive diffusion steps to define two closely spaced p-n junctions at different depths below the silicon surface. The channel length does not depend on the lithography step; rather it depends on the diffusion processes. Since the long drift-region is integrated vertically, VDMOS saves valuable silicon real estate [31, 33].

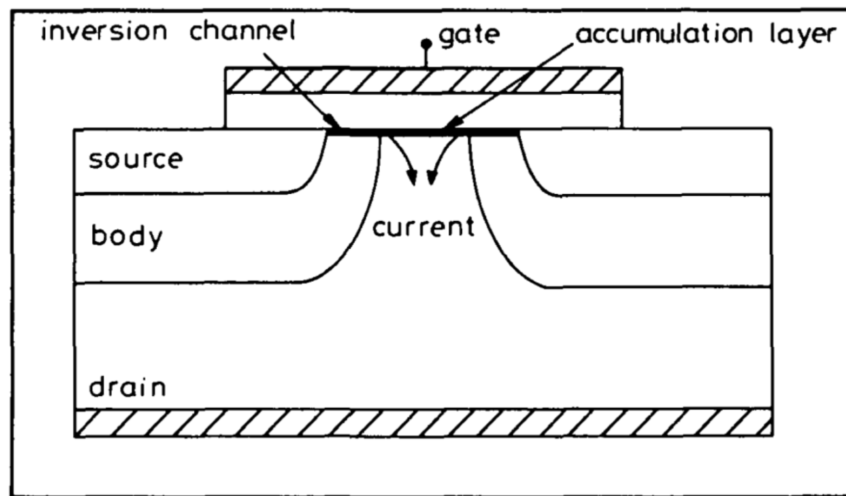


Figure 1. 3 The cross-sectional view of a VDMOS [36]

We developed, fabricated and characterized a vertically defused finFET for potential power applications. The design of the finFET structure is illustrated in figure 1.3. A narrow fin with a width of 50 nm and length of 15 μm was etched on substrate surface. One end of the fin was connected to a 50x50 μm^2 mesa for source contact. Gate dielectric and metal were deposited and fully cover the fin region. The desired doping profile along the fin was achieved by ion implantations and diffusions before the fin was etched. To further reduce source contact resistance, i.e. from the top of the fin to the mesa, salicide was formed, which also acted as a hard mask when etching the fin.

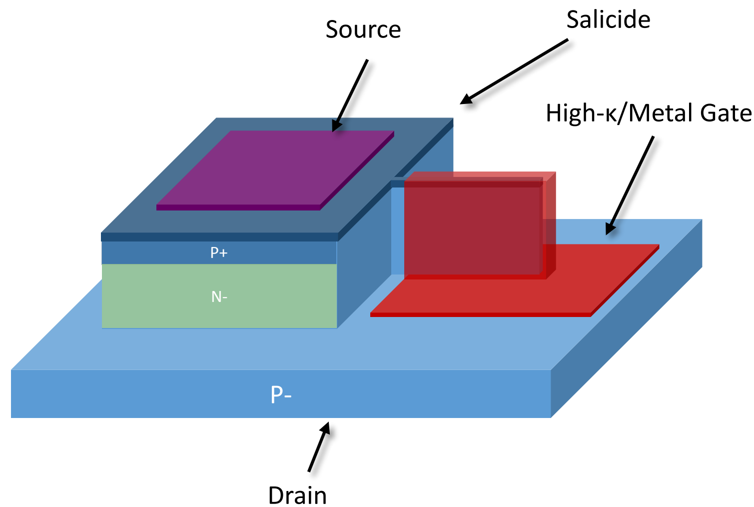


Figure 1. 4 Schematic of vertical diffused finFET.

1.4 Overview of 3D flexible electronics

Mechanically flexible integrated circuits (ICs) have gained increasing attention in recent years, with emerging markets in portable electronics, e.g. sensors, electronic textiles, and bio-medical technology [37-39]. Although a number of amorphous and single crystalline thin-film-transistor (TFT) solutions have been reported [40, 41], challenges still remain for fabrication of inexpensive, high performance flexible devices. In comparison with state-of-the-art Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology, hydrogen-passivated amorphous silicon (a-Si:H) TFT has much lower carrier mobilities[42], whereas the implementation of nanowire/nano-ribbon transistors requires a complex process flow. We propose a simple and straightforward solution: mechanically exfoliating a thin silicon film containing ICs that have been pre-fabricated on a bulk silicon wafer using conventional CMOS technology. Transistors and circuits can be pre-fabricated on silicon wafer with standard

CMOS process without additional temperature or process limitations. For example, some TFT processes require low temperature condition to prevent thermal degradation of plastic substrates. We realize high performance single crystalline TFTs by mechanical exfoliation. The short channel MOSFETs exhibit similar electrical performance before and after exfoliation. This exfoliation process also provides a fast and economical approach to producing thinned silicon wafers, which is a key enabler for three-dimensional (3D) silicon integration based on Through Silicon Vias (TSVs).

Chapter 2 Silicon nanowire array and nanowire devices

2.1 VAPOR-LIQUID-SOLID SILICON NANOWIRE GROWTH AND PATTERNING

The VLS growth mechanism has been introduced in Chapter one. Silicon wafer with <111> orientation was cleaned by piranha and HF to remove organic contamination and native oxide. 7Å Au was deposited by e-beam assisted-evaporation at a rate of 0.1 Å /sec. Right after a dilute HF dip, the wafer was transferred into Reduced Pressure Chemical Vapor Deposition (RPCVD) chamber for single crystalline silicon nanowire growth. The growth started with a 15 min. H_2 (15 sccm) anneal at a temperature of 650°C and pressure of 0.5 Torr. During the annealing, pre-deposited Au film began to form Si/Au alloy droplets on the wafer surface. Then SiH_4 was flown into the chamber (35 sccm) and silicon nanowires started to grow. Chamber pressure was maintained at 80 mTorr during the 30 min. growth. Cross-sectional SEM image after growth is shown in figure 2.1. <111> is the preferred growth direction, which is perpendicular to the plane. Some of the nanowires grew along the <110> direction. The typical nanowire has a length of 1-2 μm and diameter of 60-100 nm. These studies were done in collaboration with Prof. Tutuc.

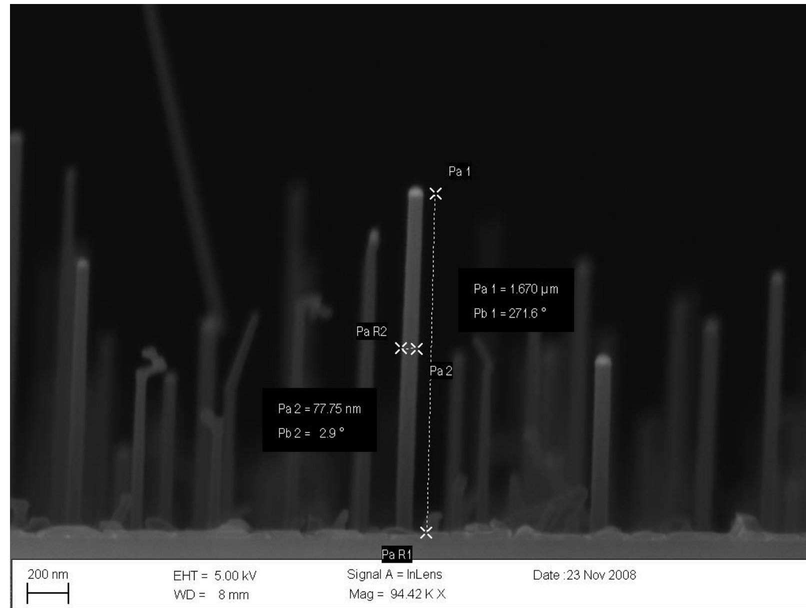


Figure 2. 1 Cross-sectional SEM image of single crystalline silicon nanowire.

Nanowires grow at the location where the catalyst droplets are formed, with a preferred orientation of <111> [25]. Diameter is determined by the size of the droplet [26] . Therefore it is possible to control the nanowire location if Au can be patterned. However, patterned Au dots have low fidelity with respect to their original shape under the high temperature annealing due to substantial agglomeration [28]. As a result, SiO_2 was used as a barrier or buffer to confine etch Au dots during the growth.

Patterning Au dots in nano scale was developed with Step and Flash Imprint Lithography (SFIL), illustrated in figure 2.2 a) [43]. In this process, 100 nm SiO_2 was grown on <111> silicon wafer by 7 min. wet oxidation at 1050°C. After spin coating adhesion layer on the wafer, SFIL was done by the IMPRIO 100 system (Molecular Imprints Inc): Imprint resist was ink-jet-ed onto the wafer and then a quartz template with patterned holes was pressed on. UV light exposure cured the resist and then the template

was released, leaving the resist as a form of nano-pillar array. After imprint, Silspin (Molecular Imprints Inc) was spun on the resist, followed by 3 steps of well-controlled etchings: Silspin etching (by CHF_3+O_2), monomat (O_2) etching and SiO_2 (by CHF_3+O_2) etching, transferring the pillar array into an array of holes in the SiO_2. After a buffered HF dip, 20nm Au was evaporated onto the wafer surface. Piranha solution lifted off the monomat layer, leaving Au dots isolated by SiO_2 barrier, as shown in figure 2.2 b). Finally silicon nanowire growth was carried out using RPCVD and the growth result is shown in figure 2.2 c).

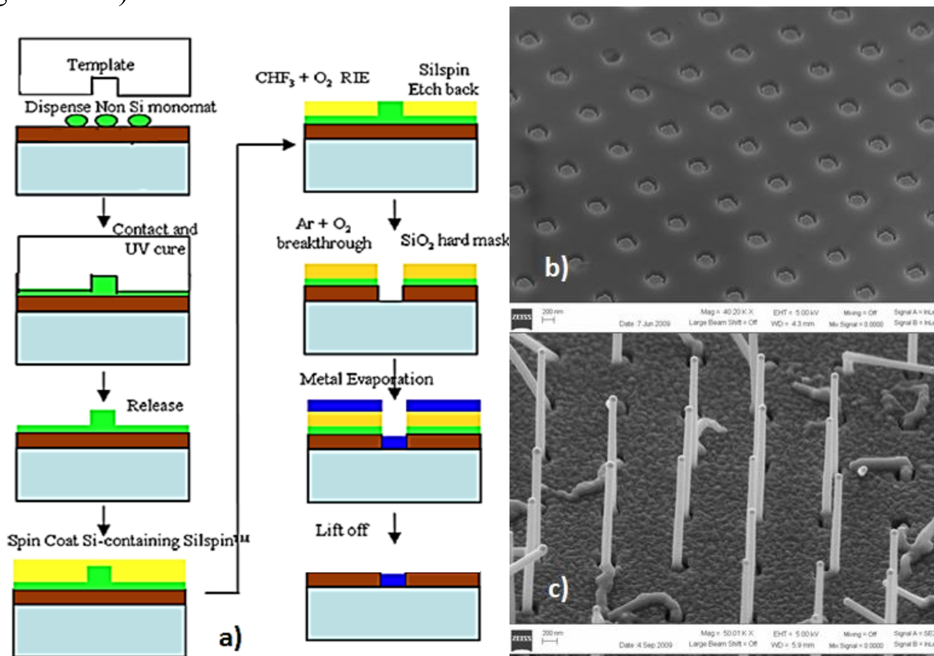


Figure 2. 2 a) SFIL/R nano-imprint process flow for patterned nanowire growth. b) Patterned Au dots with SiO_2 barrier. c) Patterned nanowire growth.

2.2 PATTERNED SILICON NANOWIRE ARRAY BY DEEP SILICON ETCHING

An alternative approach to fabricating nanowire arrays is by patterning dot-shaped mask and then etching silicon. The process flow is shown in figure 2.3. A 100 nm layer

of silicon nitride (Si_3N_4) was deposited on the substrate by low pressure chemical vapor deposition (LPCVD), serving as a hard-mask for Si etching. Following imprint process utilized a quartz template with an array of holes, and it produced the resist pattern as pillar-array. Each pillar has a diameter of 130 nm and height of ~200 nm, with a residual underlying layer of around 100 nm. We patterned 1 cm^2 dies for each imprint in a few seconds, unlike time consuming e-beam lithography. Up to 40 imprint patterns or dies were patterned on a 100 mm wafer. An O_2 plasma anisotropic etching breaks through the imprint resist residual layer and then a mixture of CHF_3 and O_2 plasma was used to etch the Si_3N_4 film, transferring the nano-pillar pattern onto Si_3N_4 dot array on the silicon substrate, with a height of 100 nm and pitch of 280 nm. The dot-shaped Si_3N_4 mask was used to etch dense ordered Si nanowires by deep silicon etching (DSE). The diameter of the nanowire was determined by the dot size, while the height was controlled by silicon etching Bosch process cycles that alternately etch with SF_6 gas and cause polymer build-up with C_4F_8 gas.

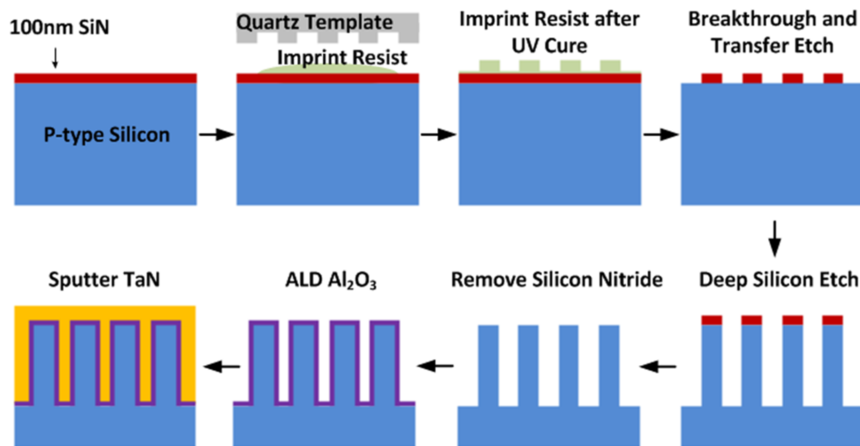


Figure 2. 3 Silicon nanowire capacitor fabrication process flow

2.3 SINGLE CRYSTAL NANOWIRE CAPACITOR

The geometry of nanowire array can be utilized as 3-dimensional nano-capacitors, as introduced in chapter 1. In this work, four splits of different deep Si etch (DSE) varying from 4 to 15 cycles spanning from 8-sec to 30-sec results in nanowire heights of 130 nm to 600 nm (Figure 2.4). Residual polymer and Si_3N_4 mask were cleaned by dry etch and piranha. After cleaning, a high-κ gate dielectric Al_2O_3 was deposited on the Si nanowire surface by Atomic Layer Deposition (ALD). TaN was sputtered as the top metal, and contact pads were defined by photolithography. In Figure 2.5 cross-sectional SEM (a) and TEM micrographs (b and c) of the final structures are shown.

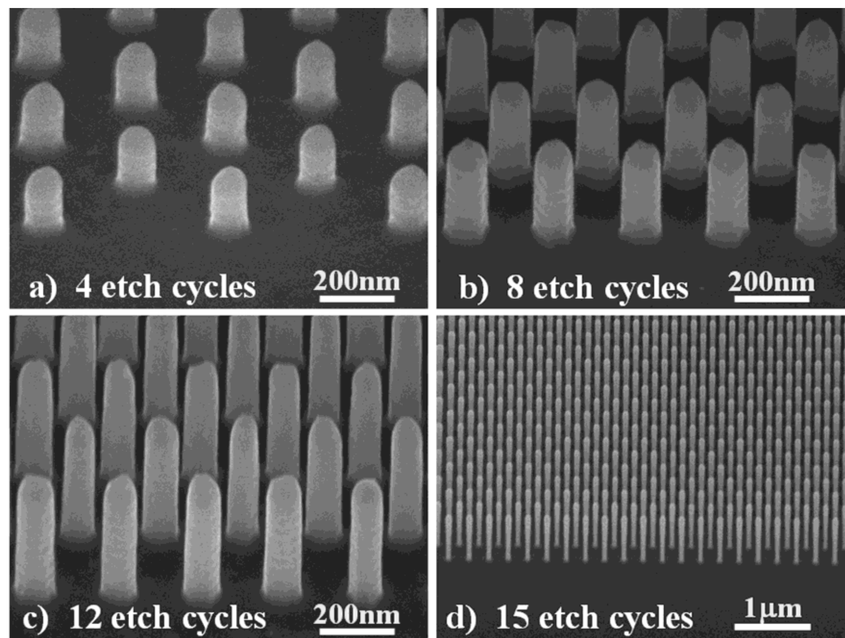


Figure 2. 4 (a-d) Si-nanowire array after DSE with 4, 8, 12, and 15 etch cycles, respectively, resulting in nanowire arrays with an increasing height.

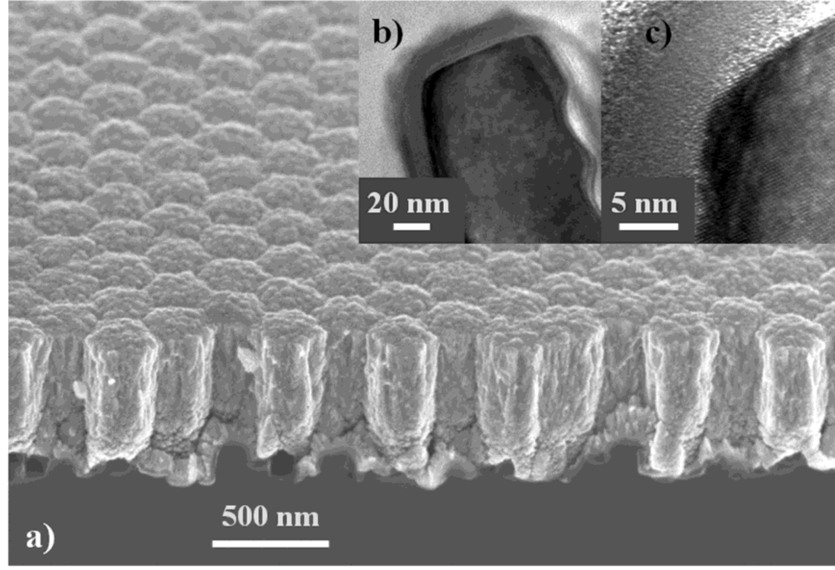


Figure 2. 5 a) 70° tilted SEM image of Si-nanowires after ALD Al_2O_3 and sputtered TaN. b) and c) Cross-section TEM image of Si-nanowire head after ALD Al_2O_3 and sputtered TaN

We calculated the Metal-Oxide-Semiconductor (MOS) capacitance of fabricated vertical nanowire capacitors based on the geometry of the 3-D structure. The layout of our Si-nanowire is an array of hexagons, with one nanowire in the center (Figure 2.6a). The edge of the unit is 162 nm since the pitch between each nanowire is 280 nm. Thus, each unit has an area of 6.82 x 10^{-10} cm^2. The capacitor of each unit (C_{unit}) consists of 3 components [44]: planar capacitor on the substrate (C_{plane}), sidewall capacitor along the vertical nanowire ($C_{cylinder}$) and top capacitor on the head of each nanowire ($C_{hemisphere}$). Since, the 3 capacitors are in parallel:

$$C_{unit} = C_{plane} + C_{cylinder} + C_{hemisphere}$$

where C_{plane} is the planar capacitor of the hexagonal unit excluding the area of Si-nanowire:

$$C_{plane} = (A_{unit} - A_{SiNW})\frac{\varepsilon_s \varepsilon_0}{d}$$

with d the dielectric thickness. In this work, we used 2 different dielectric thicknesses: 8 nm and 24 nm.

The cylindrical nanowire side wall capacitor $C_{cylinder}$ is[45]:

$$C_{cylinder} = \frac{2\pi\varepsilon_0\varepsilon_s h}{\ln(b/a)}$$

where h is the height of the cylinder, a the radius of the Si-nanowire and b the radius to the TaN gate. Therefore we have:

$$b = a + d$$

The SEM tilted view in figure 2.6b shows that the top of the nanowire could be considered as a hemispherical capacitor, $C_{hemisphere}$, due to Si_3N_4 over etching process.

$$C_{hemisphere} = \frac{2\pi\varepsilon_s\varepsilon_0}{\frac{1}{a} - \frac{1}{b}}$$

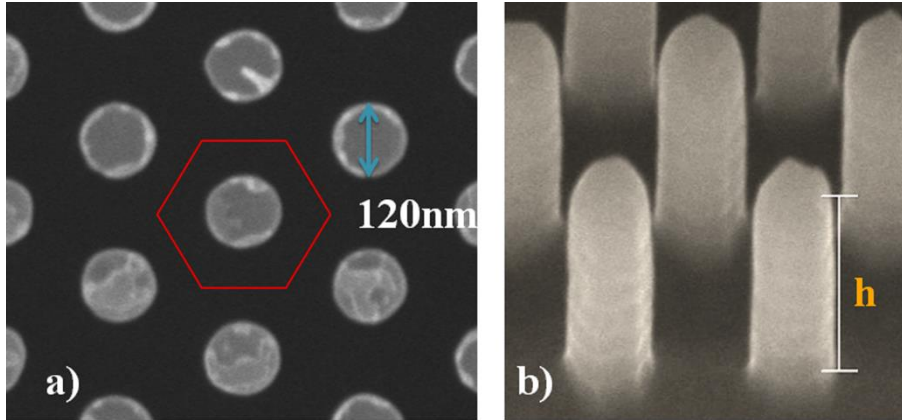


Figure 2. 6 SEM images of Si-nanowire: a) top view; b) 45° tilted view

The fabricated Si-nanowire MIS capacitors were measured by an Agilent B1500 system. Along with nanowire devices with different heights, or etching cycles during DSE, conventional planar capacitors with identical dielectric thickness were fabricated as

control samples. All capacitance measurements are normalized to microfarad per surface area in ($\mu F/cm^2$). As the substrate is lightly P-type doped, MOS capacitor accumulation condition is attained when sufficient negative bias voltage is applied.

C-V measurements of 24 nm Al_2O_3 dielectric thickness are shown in Figure 2.7a. The MOS capacitance measured on 160 nm-nanowire-height capacitors shows accumulation capacitance of 0.55 $\mu F/cm^2$. MOS capacitor with double nanowire height (320 nm) leads to higher capacitance at 0.88 $\mu F/cm^2$. Larger capacitance can be achieved by increasing etching cycles i.e. nanowire heights. The 450 nm-nanowire-height capacitor exhibits a capacitance of 1.08 $\mu F/cm^2$, which is four times the planar control sample capacitance of 0.25 $\mu F/cm^2$.

Similar devices with 8 nm Al_2O_3 as dielectric are also fabricated and the results are presented in Figure 2.7b. The 12-etching-cycle sample (450 nm Si-nanowire heights capacitors) achieves a capacity of 2.6 $\mu F/cm^2$, which is more than three times the capacity of control planar capacitors.

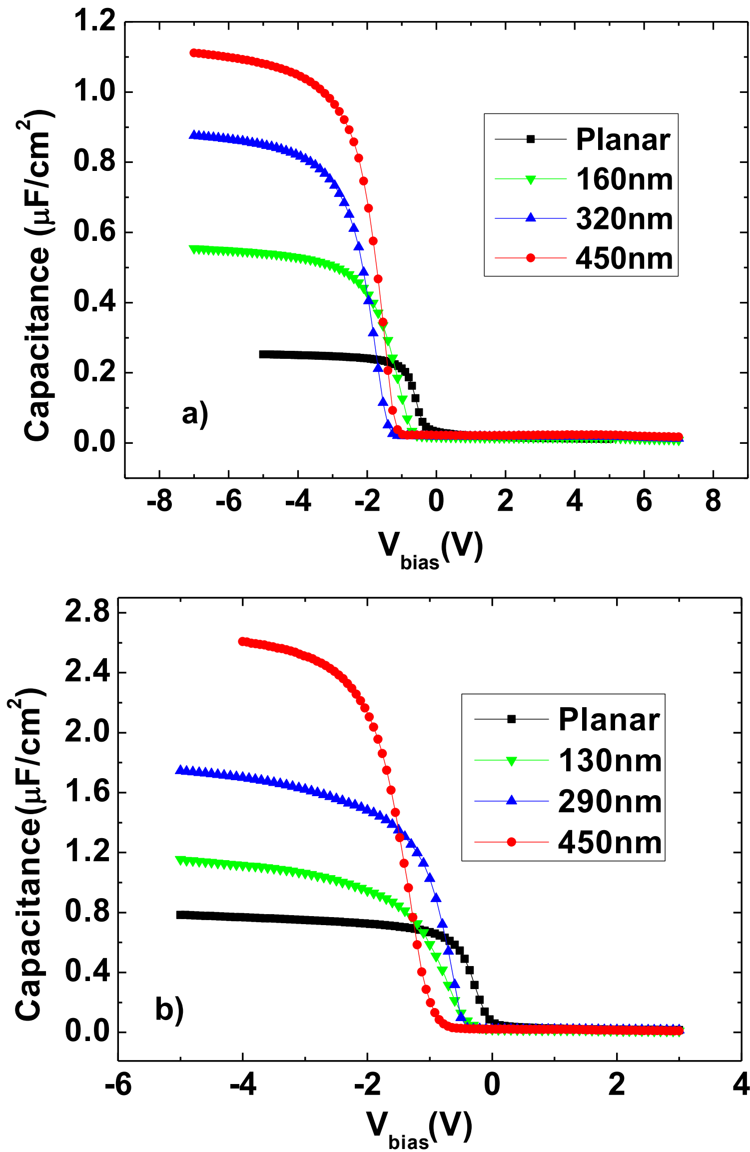


Figure 2. 7 C-V measurements of conventional planar capacitor and Si-nanowire capacitors with nanowire etch cycles of 4, 8, and 12, delivering nanowire arrays with heights between 130nm to 450nm. The Al_2O_3 dielectric thickness is 24 nm for a) and 8 nm for b).

Accumulation capacitance measurements from all Si-nanowire capacitors and our theoretical calculations are summarized in Figure 2.8. As the height of silicon nanowire increases, accumulation capacitance rises linearly. Also thinner dielectric layer leads to a

higher capacitance, as expected. The simple model fits well for the 24 nm Al_2O_3 thickness capacitors but overestimates the experimental capacitance for the 8 nm Al_2O_3 thickness. In the case of capacitors fabricated with a thinner Al_2O_3 layer, the native oxide becomes a non-negligible contributor for EOT: 1nm native oxide corresponds to ~2 nm Al_2O_3 and therefore the device behavior is similar to 10 nm Al_2O_3 dielectric.

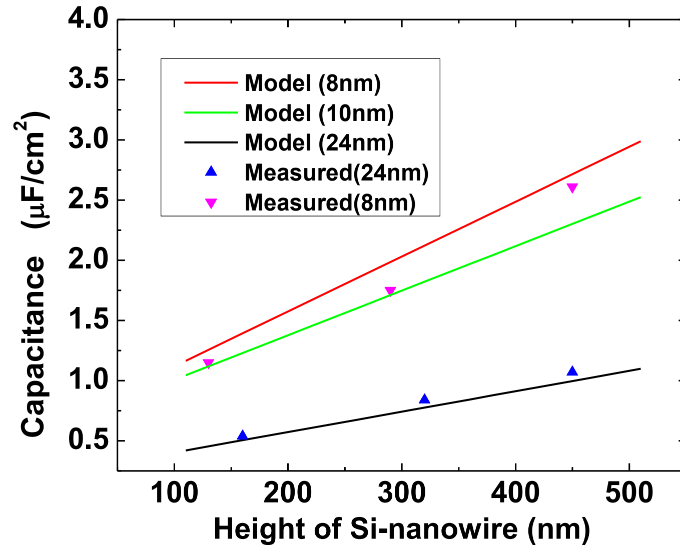


Figure 2. 8 C-V measurement results compared with calculated values

The dielectric leakage current is also measured (Figure 2.9) for our nanowire capacitors. The planar capacitors, with the both dielectric thicknesses, have the lowest leakage current (3.7×10^{-9} A/cm^2 for 24 nm and 9.64×10^{-6}A/cm^2 for 8nm at 5V bias). Capacitors fabricated with taller nanowires have larger leakage density due to the greater 3-D aspect ratio, possibly leading to field enhancement and dielectric thinning near the edges. We observe more than one order of magnitude higher leakage density for 450nm Si-nanowire capacitors compared with planar capacitor, for 24 nm Al_2O_3 dielectric

thickness. Capacitors with reduced dielectric thickness have higher leakage density. The highest leakage current is obtained with the combination of thinner dielectric thickness and highest nanowire height (36 mA/cm^2 at 5V bias).

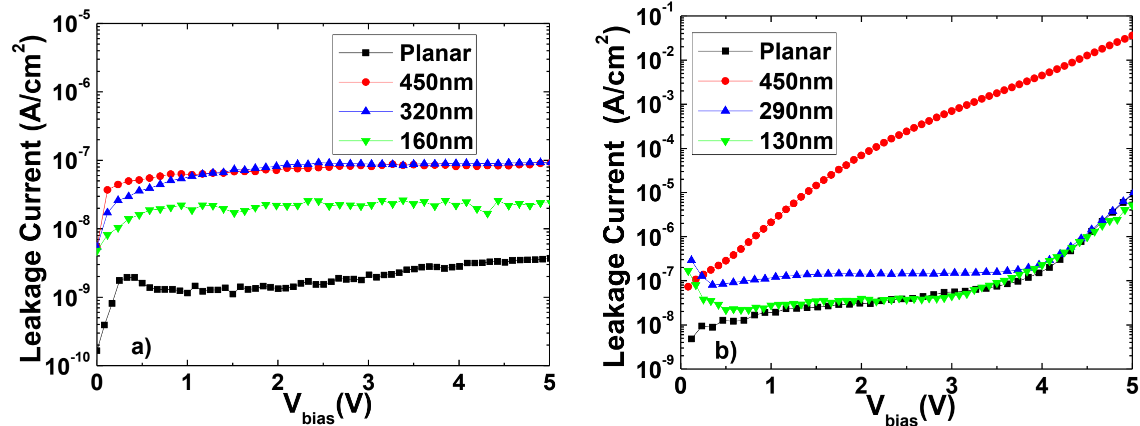


Figure 2. 9 Dielectric leakage current for conventional planar capacitor and Si-nanowire capacitors with nanowire etch cycles of 4, 8, and 12. Al_2O_3 dielectric thickness is 24nm for a) and 8 nm for b).

Time-dependent dielectric breakdown is also measured on Si-nanowire capacitor and compared with planar structure (Figure 2.10). The capacitor is fabricated with 450nm nanowire heights and a dielectric thickness of 24 nm Al_2O_3. Compared with planar structure, nanowire capacitors are slightly easier to break-down due to non-planar 3-D geometry which can enhance electric fields.

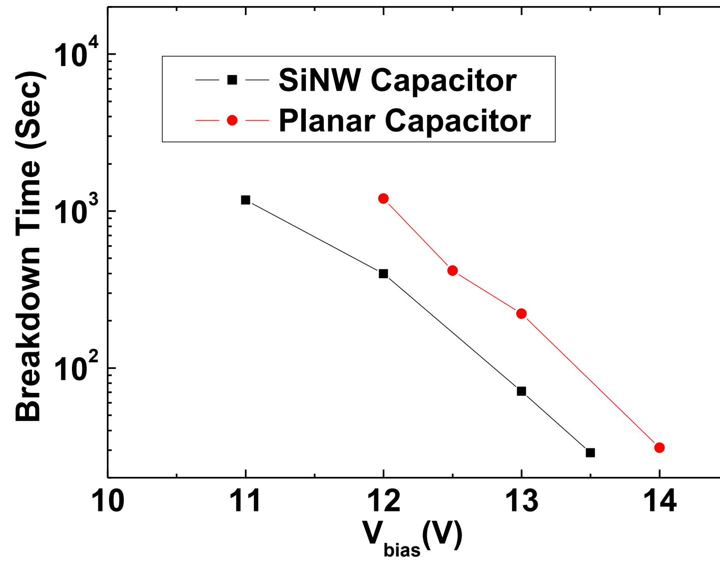


Figure 2. 10 Time-Dependent Dielectric Breakdown measurement on Si-nanowire capacitors compared with conventional planar capacitors.

Chapter 3 Gate-All-Around Nanowire FET

3.1 Integration challenges for GAA-nanowire FET

In chapter 2 we described a successful technique to fabricate nanowire arrays, which enables the process integration of vertical silicon nanowire field-effect-transistors. However, successful fabrication of nanowire FET requires extra steps. In this section we discuss several major challenges in the development of nanowire FET process integration:

1) Etching optimization for high quality nanowires.
2) Plasma enhanced ALD titanium nitride (TiN) as gate metal.
3) Gate isotropic etch and vertical patterning.

3.1.1 Etching optimization for high quality nanowires

There are several crucial elements to achieve vertical nanowire structure of high aspect ratio by the top-down etching approach: a nano-scale dot-shaped hard mask, high etching selectivity and very anisotropic etching technique.

It has been demonstrated in chapter 2 that silicon nitride films patterned by nano-imprint lithography can be utilized as a hard mask to etch silicon nanowires. Experimental results show that 100 nm silicon nitride film is able to sustain 1 μm-deep silicon etching, i.e. the selectivity is around 1:10.

An alternative candidate for the hard mask is silicon/metal salicide[46]. In particular metal salicide is very hard to etch, so higher etch selectivity can be reached. Figure 3.1 shows a tilted SEM image of a very high aspect ratio nanowire achieved by the salicide dot mask and DSE. Also, for fabricating nanowire transistors, metal salicide is capable of reducing contact resistance to the nanowire body from top, and therefore potentially improves device performance. Electron beam lithography is compatible with

this salicide-mask-nanowire-etching process: Instead of exposing a large area on positive e-beam resist that consumes a lot of time, we exposed 100 nm-diameter area to form holes. Afterwards metal was evaporated and lifted off to achieve pillar shaped dots. Salicide was formed with 10 sec 600˚C rapid thermal anneal in N_2 atmosphere. In Figure 3.1, the etched nanowires have a diameter of 70 nm and the height is more than 1.4 µm.

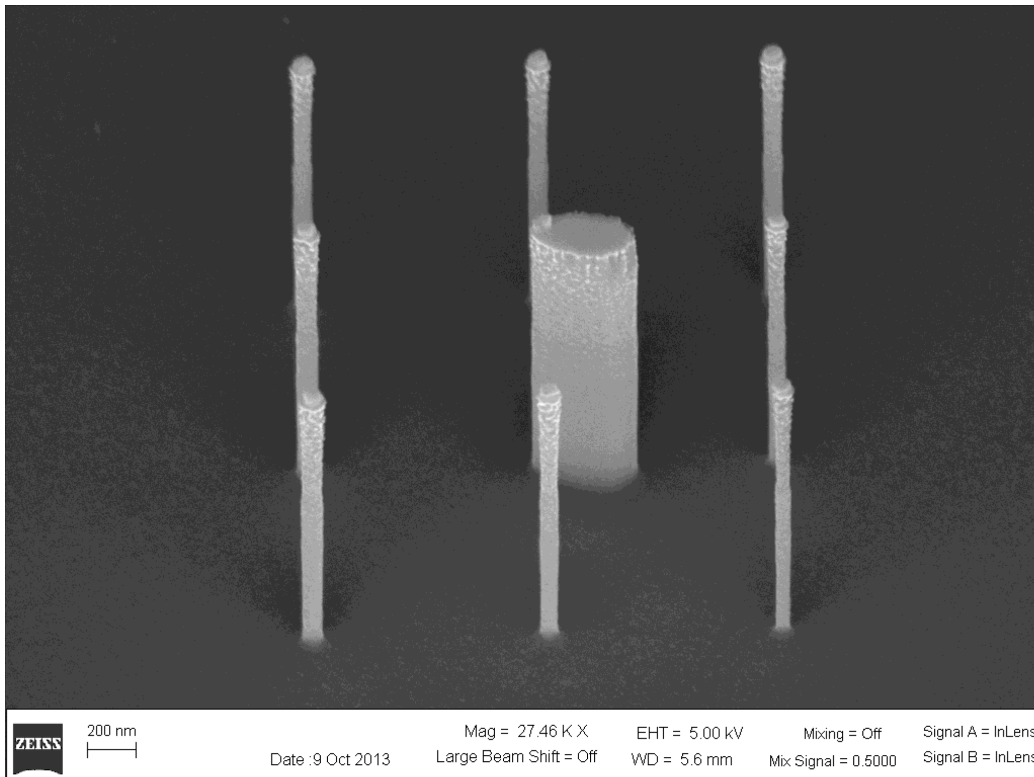


Figure 3. 1 High aspect ratio nanowires are achieved by deep silicon etch with metal salicide mask. The aspect ratio is more than 20 on nanowires. The defect in center post probably results from metal out-diffusion during salicide anneal.

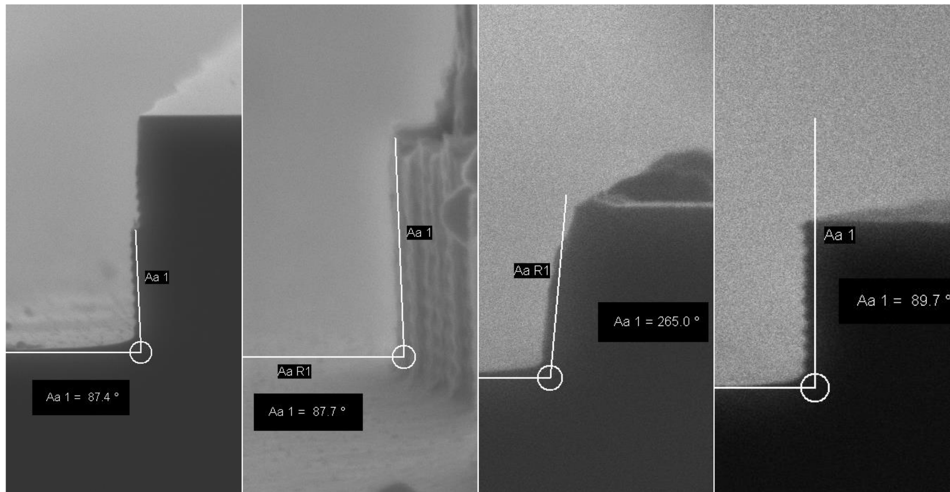
Although anisotropic silicon etching approaches by wet chemical etchants have been reported, e.g. KOH and TDMAH, it is more straightforward and controllable to etch silicon by reactive ions. HBr and Cl_2 plasma is able to anisotropically etch silicon with a smooth sidewall, though a well-tuned recipe is necessary[47]. In the previous chapter, we

have demonstrated another etching process (Bosch etch) that alternatively deposits polymer and etches silicon to fabricate nanowires. In our etching process, PlasmaTherm Silicon Deep RIE was utilized and C_4F_8 plasma deposits polymer while SF_6 etches silicon. Table 3.1 includes the detailed parameters for each process cycle that we employed in the fabrication of nanowires.

	Deposition Cycle	**Etch Cycle**
Time	0.8 sec	2.0 sec
Pressure	20 mTorr	20 mTorr
Gas Flow ($Ar/SF_6/C_4F_8$)	10/50/125 sccm	10/50/40 sccm
ICP Power	1600 Watt	1500Watt
RF Bias	10 Volt	450 Volt

Table 3. 1 Process conditions of polymer deposition and silicon etching for each DSE cycle. Tool: PlasmaTherm Silicon deep RIE.

The profile of nanowire sidewall can be optimized by adjusting the ratio of etching time to deposition time in every cycle. Excessive etch/deposition ratio will undercut the etched sidewall, leading to a nail-shaped nanowire and mechanical frangibility. To investigate the influence of etch/deposition ratio on the etched sidewall, a series of experiments with a range of etch/deposition ratio were carried out, and etch results were characterized by cross-sectional SEM images, as shown in Figure 3.2. A good vertically etched sidewall is achieved when etch/deposition ratio = 0.5.

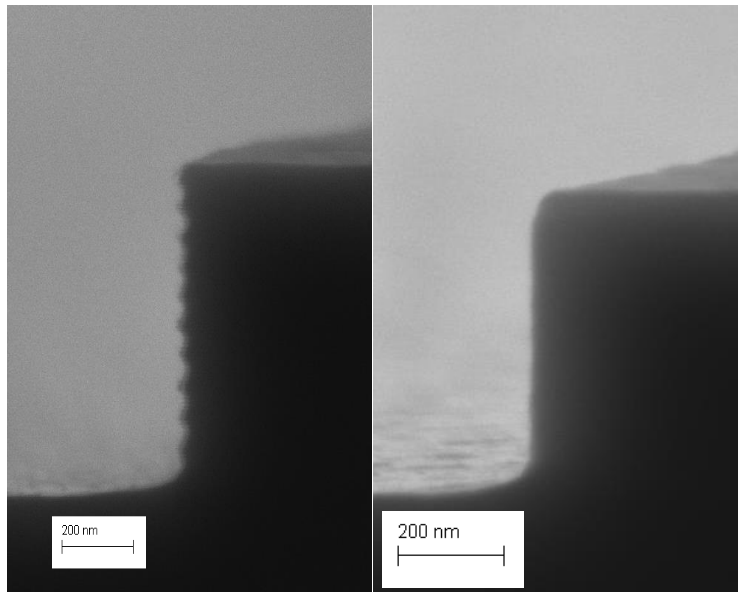


Dep time	0.8sec	0.8sec	0.8sec	1.0sec
Etch time	2.0sec	1.5sec	1.0sec	2.0sec
Dep/Etch ratio	0.4	0.53	0.8s	0.5
Undercut angel	-2.6^o	-2.3^o	+10°	-0.3^o

Figure 3. 2 Cross-sectional SEM images of deep silicon etching. Samples were etched with different etch/deposition ratio and sidewall undercut angels were evaluated. Result shows that the combination of 1.0 sec deposition and 2.0 sec etching yield almost 90° vertical sidewall.

In Figure 3.2 it also can be observed that the scallops are formed on the etched sidewall, which is a signature of Bosch etching process. Each concave feature corresponds to one etch/deposition cycle. The scallops can be minimized by scaling down etching time in every cycle while keeping etch/deposition ratio as a constant. Cross-sectional SEM images of etched samples with different etching time in one cycle are shown in Figure 3.3 and the optimized sidewall was obtained when the etching time was 1.0 sec and the deposition time was 0.5 sec for each cycle. From the image, scallops were observed from the sidewall in the original recipe (left), whereas a much smoother sidewall was achieved in the optimized recipe (right). It was also noted that the etch rate

was reduced in term of the same etch time. In Figure 3.3, both samples were etched by 20 sec in total. The original recipe achieved a etch depth of ~840nm, compared to ~660nm achieved by the optimized recipe.



Parameter	Baseline	Optimized
Etch time/cycle	2.0 sec	1.0 sec
Dep time/cycle	1.0 sec	0.5 sec
Cycle #	10 cycles	20 cycles
Etch Depth*	839.5nm	660.2nm

Figure 3. 3 Etched sidewall morphology optimization. The original recipe has 2.0 sec deposition time and 1.0 sec etch time in each cycle. Scallops are observed on the etched sidewall. The optimized recipe reduces the deposition time to 1.0 sec and the etch time to 0.5 sec, and scallops are minimized on the etched sidewall. Note that the etch/deposition ratio is kept as a constant (2) in the process optimization.

In this section we developed a new approach to fabricating high aspect ratio nanowires by e-beam lithography, metal salicide and deep silicon etching. The etched

sidewall morphology highly depends on the etching conditions such as deposition/etch time, ICP power, RF bias etc,. By adjusting the etching time and deposition time in every cycle, we achieved nanowires with a smoother sidewall and undercutting defect was minimized. Figure 3.4 compares the nanowire sidewall morphologies before and after the recipe optimization. The optimized recipe greatly improves the undercutting defect and the sidewall smoothness.

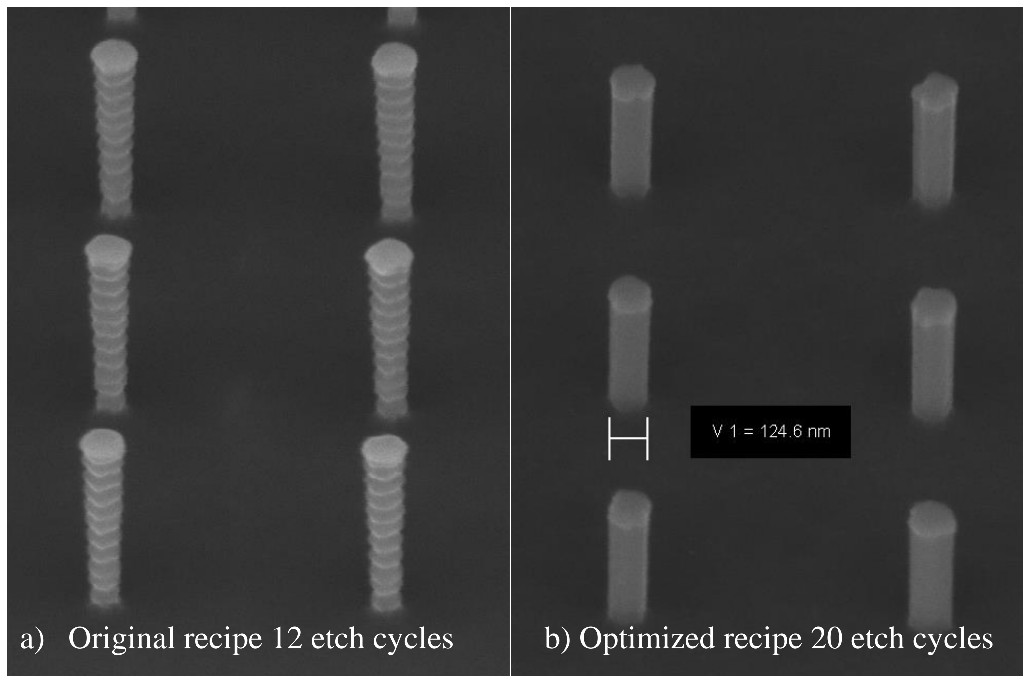


Figure 3. 4 Recipe optimization result for silicon nanowire etching. The left image a) shows the nanowires etched with the original recipe. Scallops are observed on the sidewall of nanowires as well as undercutting defect. Etching process undercuts the nanowire bottom as the cycle number increases. The right image b) shows the nanowires etched with the optimized recipe. Sidewall smoothness is improved and undercutting is minimized.

3.1.2 Plasma Enhanced ALD as gate metal.

Gate deposition and patterning are exceedingly challenging in process integration of nanowire FETs. First, a very conformal deposition of the gate metal is necessary in order to wrap around the nanowire core and realize the gate-all-around structure. Second, the vertical gate pattern on the nanowire sidewall cannot be defined by traditional lithography approaches. The gate metal and dielectric on the upper portion of the nanowire need to be removed to expose the silicon nanowire core to the drain metal. Moreover, the gate metal should be well isolated from the drain metal on top to avoid leakage between the two metal layers.

Plasma enhanced atomic layer deposition (PEALD) provides a very conformal deposition technique and is suitable for the nanowire FET process integration. ALD TiN technologies have been well studied and reported[48-50]. Several different deposition recipes were developed with Fiji plasma enhanced ALD system using TDMAT as the precursor. Figure 3.5 illustrates two typical PEALD processes in N_2 atmosphere and in NH_3.

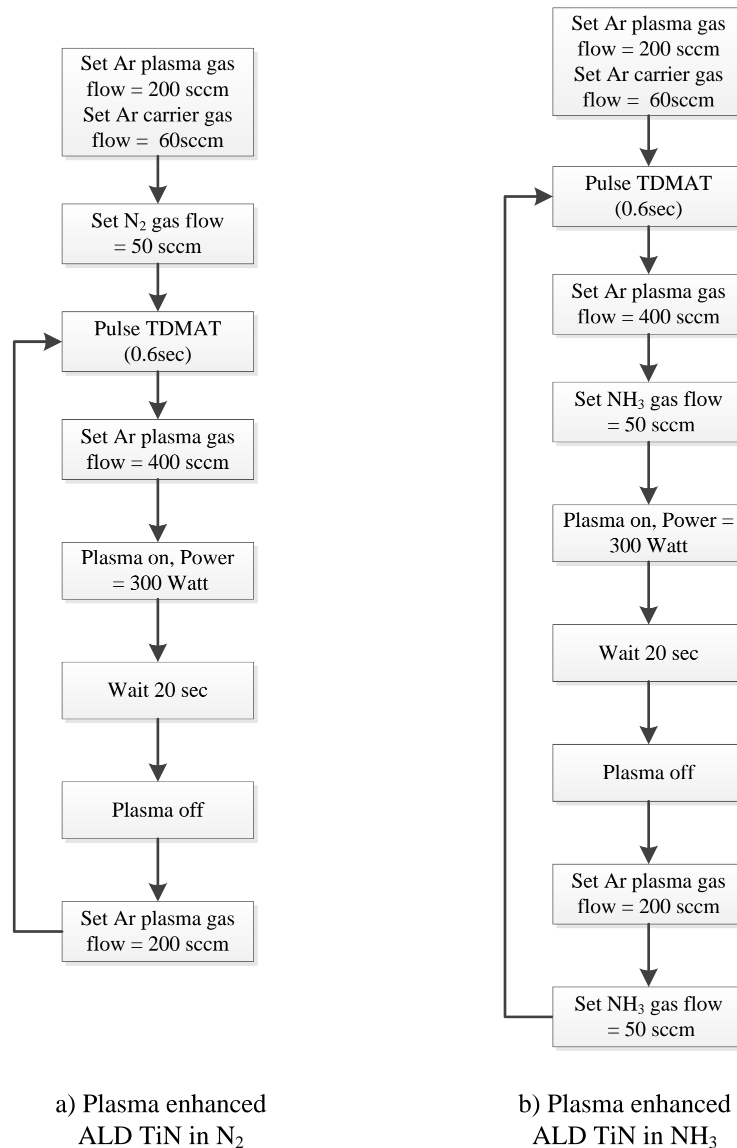


Figure 3. 5 Illustrations of plasma enhanced ALD TiN process in N_2 (a) and NH_3 (b) respectively. Note that NH_3 should be turned off while pulsing TDMAT.

Since NH_3 is reactive to TDMAT, NH_3 valve must be turned off when pulsing TDMAT. The deposition rates of PEALD TiN are 0.73 Å and 1.82 Å per cycle in N_2 and NH_3 atmosphere, respectively. Sheet resistances were measured on PEALD TiN films on

silicon substrate with 100 Å Al_2O_3 dielectric. Resistivity can be calculated with the measured sheet resistance and the film thickness by:

$$\rho = R_s \times t$$

where t is the film thickness.

Measured sheet resistances of TiN films deposited in N_2 and NH_3 are 136.2 Ω/□ and 1132.6 Ω/□ respectively, and therefore the calculated resistivities are 367 μΩ cm and 2830 μΩ·cm.

Deposited TiN films can be etched by reactive ion etching (dry etch) or wet chemical etching. In the test vehicle 270 Å TiN was etched by CF_4 plasma within 2 min with 200 watt power. To form the vertical pattern along the sidewall of nanowire, isotropic etching is preferred. TiN wet chemical etching with SC-1 solution (NH_4OH:H_2O_2:H_2O=1:1:5) had been reported[51] and etching tests were carried out on TiN samples prepared in N_2 and in HN_3 respectively. Test results show that SC-1 solution etches the TiN film prepared in NH_3 with a rate of c.a. 2.2 nm/min, and that prepared in N_2 at a very slow rate.

The properties of the films deposited by two different approaches are compared in Table 3.2.

Process Conditions	Recipe 1	Recipe 2
Deposition atmosphere	N_2	NH_3
Plasma Power	300 Watt	300Watt
Cycles	350 cycles	150 cycles
Film thickness	~270 Å	~270 Å
Deposition	0.77 Å/cycle	1.8 Å/cycle
Sheet Resistance	136 Ω/□	1133 Ω/□
Resistivity	367 μΩ cm	3059 μΩ cm
Etch Rate	Very Slow	2.2nm/min

Table 3. 2 Process conditions and film qualifications of TiN deposited in N_2 and NH_3 .

Metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated with both types of TiN and test results show good C-V characteristics. The results confirm that the fabricated TiN films perform well as a gate metal material (Figure 3.6). The measured samples were fabricated on a lightly doped p-type substrate with 100 Å ALD Al_2O_3 as the dielectric. Under a negative bias, the accumulation capacitance is ~ 0.6 $\mu F/cm^2$, which agrees with the theoretical parallel-plate capacitor model.

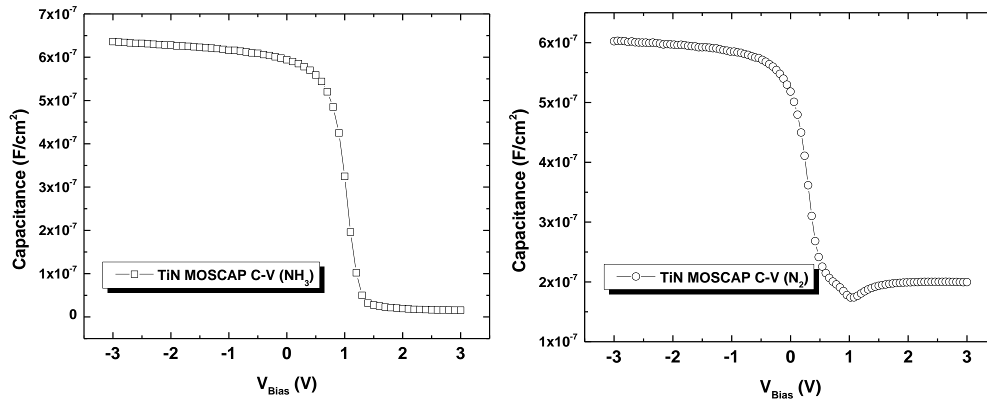


Figure 3. 6 C-V characteristics of fabricated MOS capacitors with plasma enhanced ALD TiN as the gate metal

3.1.3 Gate isotropic etch and vertical patterning

After conformal atomic layer depositions, silicon nanowires were fully covered by gate dielectric and gate metal. On the nanowire sidewall, the gate metal needs to be patterned to achieve the designed gate length, and also to expose the nanowire core to the drain metal. Since traditional lithography approaches could not define the vertical pattern, an alternative resist spin-on and etch back process was developed. As illustrated in Figure 3.7, after the gate metal and dielectric were deposited onto nanowires, resist was spun on the sample and fully covered the nanowires and planarized the surface. Following O_2 plasma etching slowly thinned the resist at a controllable rate, until the desired gate length was achieved. Then the uncovered metal was removed by anisotropic etching. Figure 3.8 shows tilted SEM images of a nanowire sample with this spin-on and etch-back process to form the gate pattern.

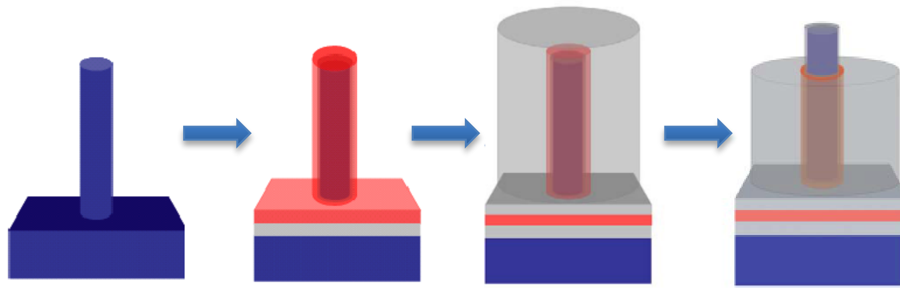


Figure 3. 7 Illustration for resist spin-on and etch-back process to vertically pattern the gate metal.

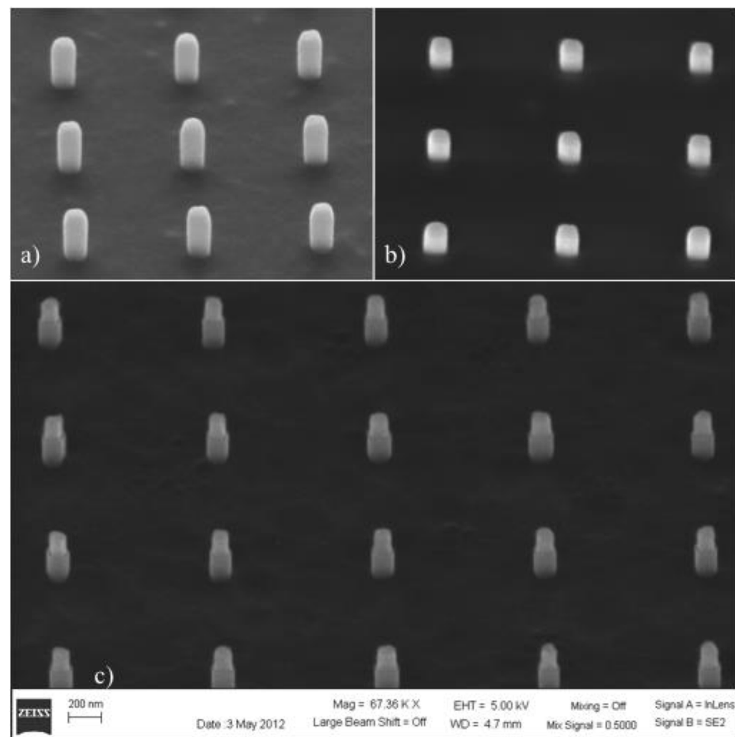


Figure 3. 8 Resist spin-on and etch-back process to vertically pattern the gate metal. a) Al_2O_3 and TiN are deposited on nanowires. b) Resist is spun and etched back to define the gate length. c) Exposed TiN is wet etched by SC-1 solution and the resist is removed.

For the process integration of nanowire FETs, TiN was patterned as the gate metal pad and PECVD SiO_2 was used as an inter-metal dielectric to electrically isolate the drain metal from the gate metal. After the drain metallization, PECVD SiO_2 was locally etched away by hydrofluoric acid (HF) to access the buried gate metal, i.e. the TiN film. However, it had been found that the conductivity of the TiN film was severely degraded after a series of processes of photolithography, PECVD SiO_2 and HF etching. The TiN film after these processes exhibited an extraordinarily high resistivity and hindered the gate control. A set of experiments were designed to diagnose the failure and find a feasible approach to avoid the degradation: Three dummy structures were fabricated to test the TiN conductivity after the process integration:

a) A PEALD TiN film was patterned by photolithography, followed by PECVD SiO_2 deposition. A contact window was opened by the second lithography and HF wet etching so that the buried TiN film was accessed. As shown in Figure 3.9a.

b) PECVD SiO_2 was deposited on TiN immediately after PEALD. Photolithography patterned the SiO_2, followed by HF etching to access the TiN film. As shown in Figure 3.9b.

c) A PEALD TiN film was patterned by photolithography, covered by 200 Å ALD Al_2O_3 capping layer. Then PECVD SiO_2 was deposited on the Al_2O_3. The 2nd photolithography opened a contact window and HF etched SiO_2 and Al_2O_3 through the window to access the TiN film. As shown in Figure 3.9c.

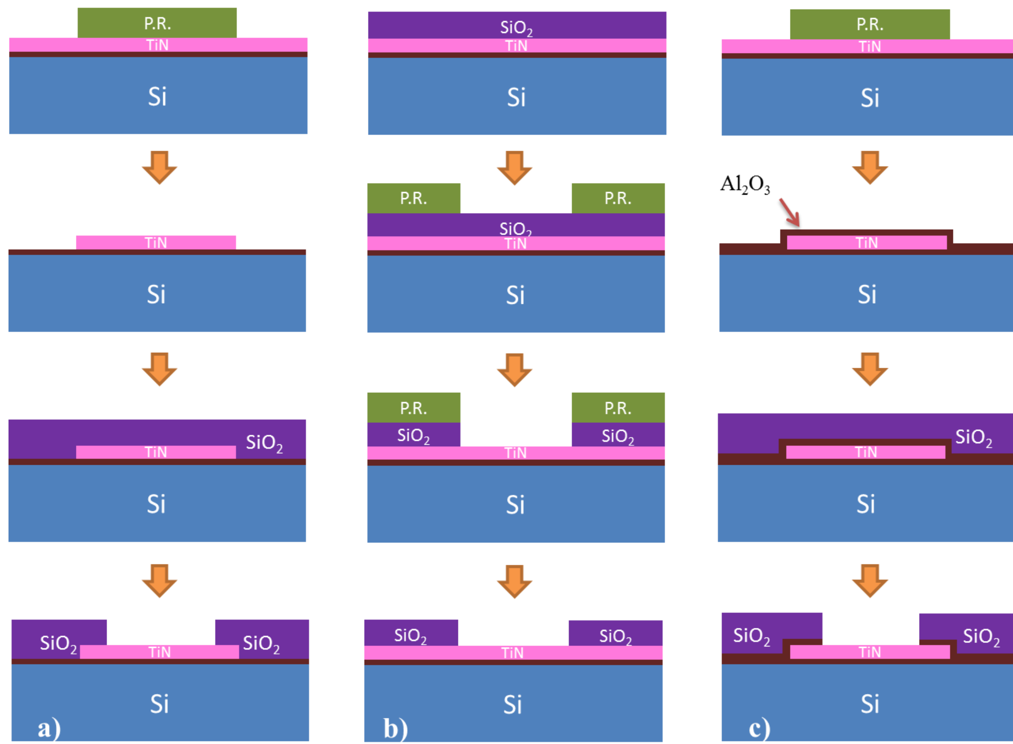


Figure 3. 9 Test structures to investigate TiN film conductivity degradation.

To evaluate the conductivity degradation, two probes were placed on the same TiN contact pad (size: 100 μm x 100 μm) and the conducting current was measured under a voltage bias. For comparison, the I-V characteristic of a bare TiN film was also measured. It was found that the TiN film in test structure b) and c) behaved as a conductive metal, whereas in structure a) the TiN became highly resistive as an insulator. Although the degradation mechanism was unknown, the results indicated that the TiN conductivity degradation can be avoided by capping SiO_2 on TiN before photolithography, or by capping Al_2O_3 on post-lithography TiN before PECVD SiO_2. The measured data is plotted in Figure 3.10.

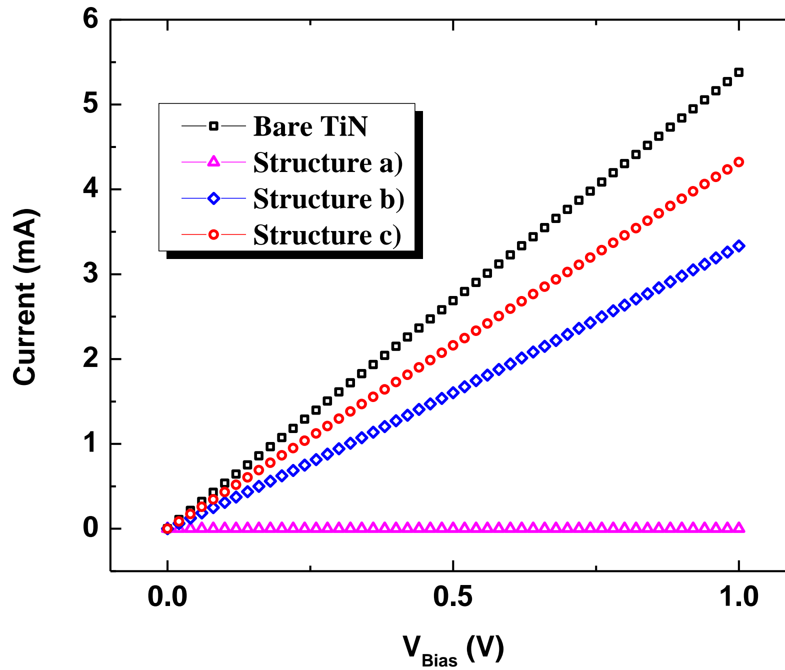


Figure 3. 10 Measured I-V on TiN gate metal with different test structures of TiN process integration.

Besides PEALD TiN, other metal candidates and potential etching techniques are also investigated for the nanowire FET process integration. For instance, sputtered TaN was deposited and tested for as the gate metal candidate. However it was very difficult to vertically pattern TaN: the poor sidewall deposition quality makes wet etch uncontrollable, wet etching. CF_4 dry etch also introduces contamination and lead to large C-V hysteresis. Table 3.3 summaries the materials and techniques for the gate metal integrations. Functional nanowire FET devices are achieved by utilizing PEALD TiN (NH_3) as the gate metal, PECVD SiO_2 as the etch mask and 1:1:5 SC-1 as the metal etchant.

Gate Metal	Etch Mask	Etchant	Patterning result	Post Process resistivity	Other Comments
Sputtered TaN	Resist	EDTA+H_2O_2	**Over etch**	-	-
	Resist	CF_4 dry etch	Good	Very low	Large C-V hysteresis
ALD TiN (N_2)	Resist	1:1:5 SC-1	**Very slow etch rate**	**Very High**	No significant TiN etching
	Resist	CF_4 dry etch	**Recipe not stable**	**Very High**	-
	PECVD SiO_2	Piranha Dip	**Over etch**	Very low	Etching is un-controllable and sidewall pattern is lost
	PECVD SiO_2	1:2:5 SC-1 @60˚C	**Over etch**	Very low	
ALD TiN (NH_3)	Resist	1:1:5 SC-1	Good	**Very High**	-
	PECVD SiO_2	1:1:5 SC-1	Good	Low	**Functional device achieved**

Table 3. 3 Materials and etching techniques for the nanowire FET gate metal integration. Successful integration is achieved by utilizing PEALD TiN (NH_3) as the gate metal, PECVD SiO_2 as the gate mask and 1:1:5 SC-1 as the gate metal etchant.

In summary, we discussed several major challenges for the nanowire FET process integration and explored mythologies to address the technical barriers. Firstly we proposed a new approach to patterning the nanowires with EBL and metal salicide. Then DSE process was optimized to achieve vertical nanowires with a smooth sidewall. We also developed conformal metal deposition methods with plasma enhanced ALD. The

film quality and etching approaches were also investigated. In order to integrate TiN film as a gate metal without compromising the conductivity, several test structures were compared and solutions were proposed.

3.2 PROCESS DEVELOPMENT GATE-ALL-AROUND NANOWIRE FETS

Based on the highly ordered silicon nanowire array, gate-all-around nanowire pMOSFETs were fabricated. The design of the device structure is illustrated in Figure 3.11. Similar to nanowire capacitors, the silicon nanowires that were fabricated by DSE were vertical to the substrate wafer. Multiple nanowires can be integrated in one device in parallel to contribute a larger drive current. The boron doped substrate served as the source terminal for the p-type MOSFET, and the Si nanowires were lightly doped by phosphorus as the channel. On the top of nanowires, the drain was heavily doped by boron and metal salicide was formed to reduce the contact resistance. Along the nanowire sidewall, the high-κ dielectric and gate metal were wrapped around the silicon nanowire core to achieve the gate-all-around structure. Atomic layer depositions can yield very conformal films and thus is the preferred process for dielectric and metal depositions[52]. The drain metal on top was isolated from the buried gate metal layer by an inter-metal dielectric, for example PECVD SiO_2.

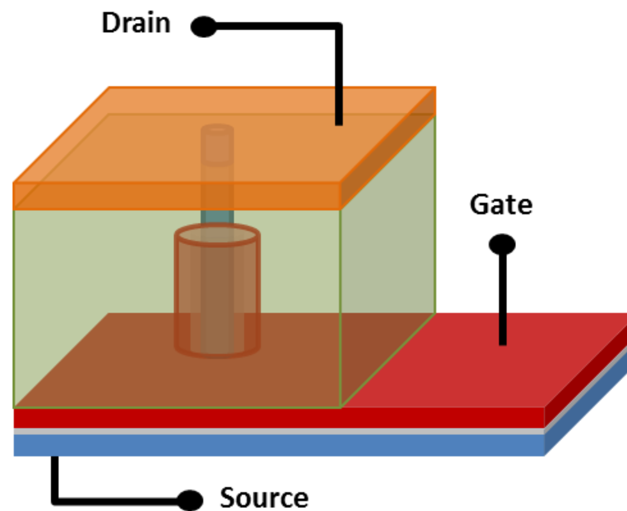
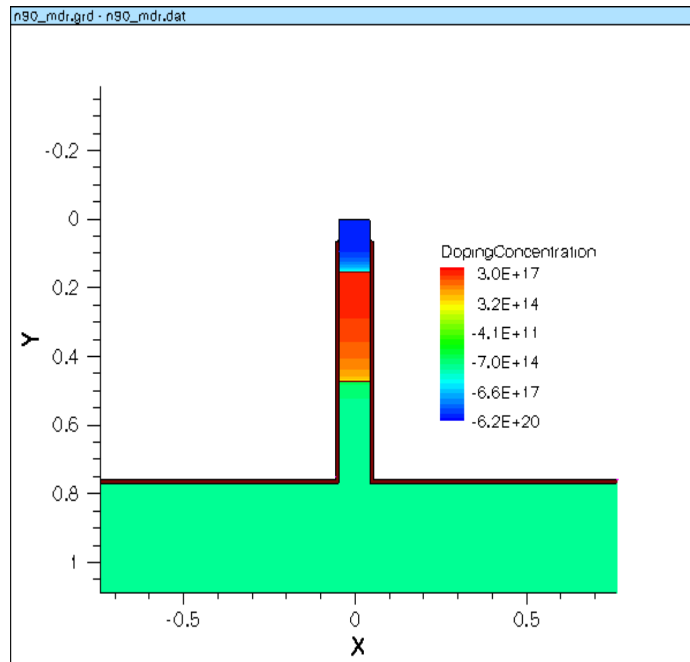


Figure 3. 11 Schematic of a vertical nanowire field-effect-transistor.

In order to achieve the desired the p-n-p doping profile for p-MOS, we used epitaxy silicon wafer and pre-doped the wafer before the nanowire was etched. The wafer had a highly doped p-type substrate and an epitaxy p- layer of 7-11 μm in thickness, which served as the common source for the nanowire FETs. Phosphorus was implanted using 100 keV energy and $1x10^{13}/cm^2$ dose to dope the n-type channel region. After 1 hour 1000˚C activation annealing, the junction depth was diffused to 470 nm below the wafer surface. Drain is doped by boron implantation with a dosage of $5x10^{15}/cm^2$ at 20 keV, followed by a 10 sec thermal activation at 1000˚C. Figure 3.12 shows the simulated doping concentration profile for nanowire FETs. Simulation result indicates that the drain doping has a peak concentration of 10^{21} $/cm^3$ and a junction depth of 150nm, while the peak concentration in n-type channel is 10^{17} $/cm^3$ and channel length is ~ 320nm.



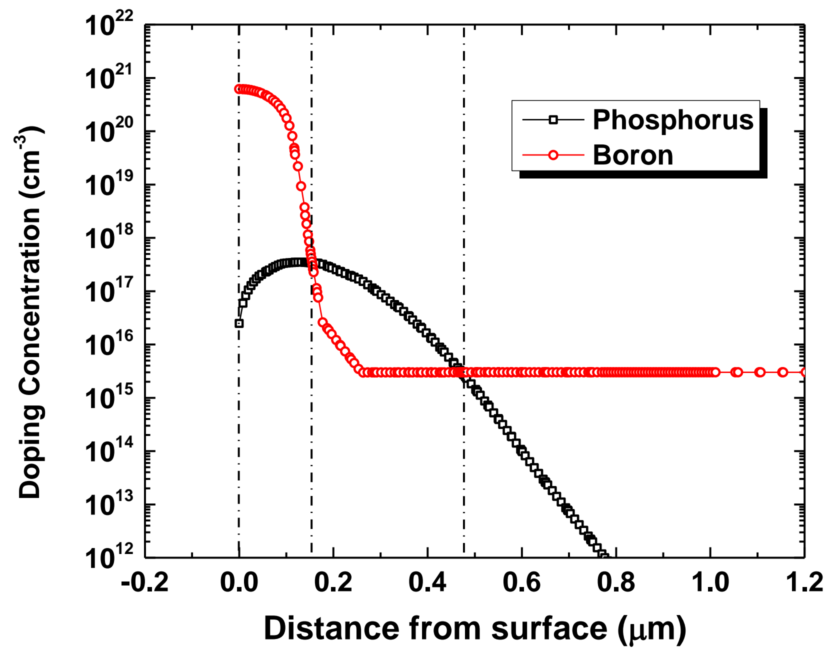


Figure 3. 12 Simulated doping concentration for nanowire FETs.

The sample was patterned by JEOL electron beam lithography after doping. First 100 nm-diameter hole-array was patterned on the ZEP resis. Next, 200Å titanium followed by 200Å nickel was deposited on the sample with e-beam assisted evaporation and consequent lift-off process left metal dots array on silicon surface. Metal/silicon salicide was formed after 600˚C 10 sec rapid thermal anneal in N_2, which not only acted as a hard mask for DSE but also reduced the drain contact resistance. We patterned a variety size of arrays: 1×1, 2×2, 3×3, 4×4 and 5×5. The following 30 cycles of DSE realized the nanowire array with a height of ~720nm. 45˚ tilted SEM images are shown in Figure 3.13. The salicide on top of each nanowire is observed.

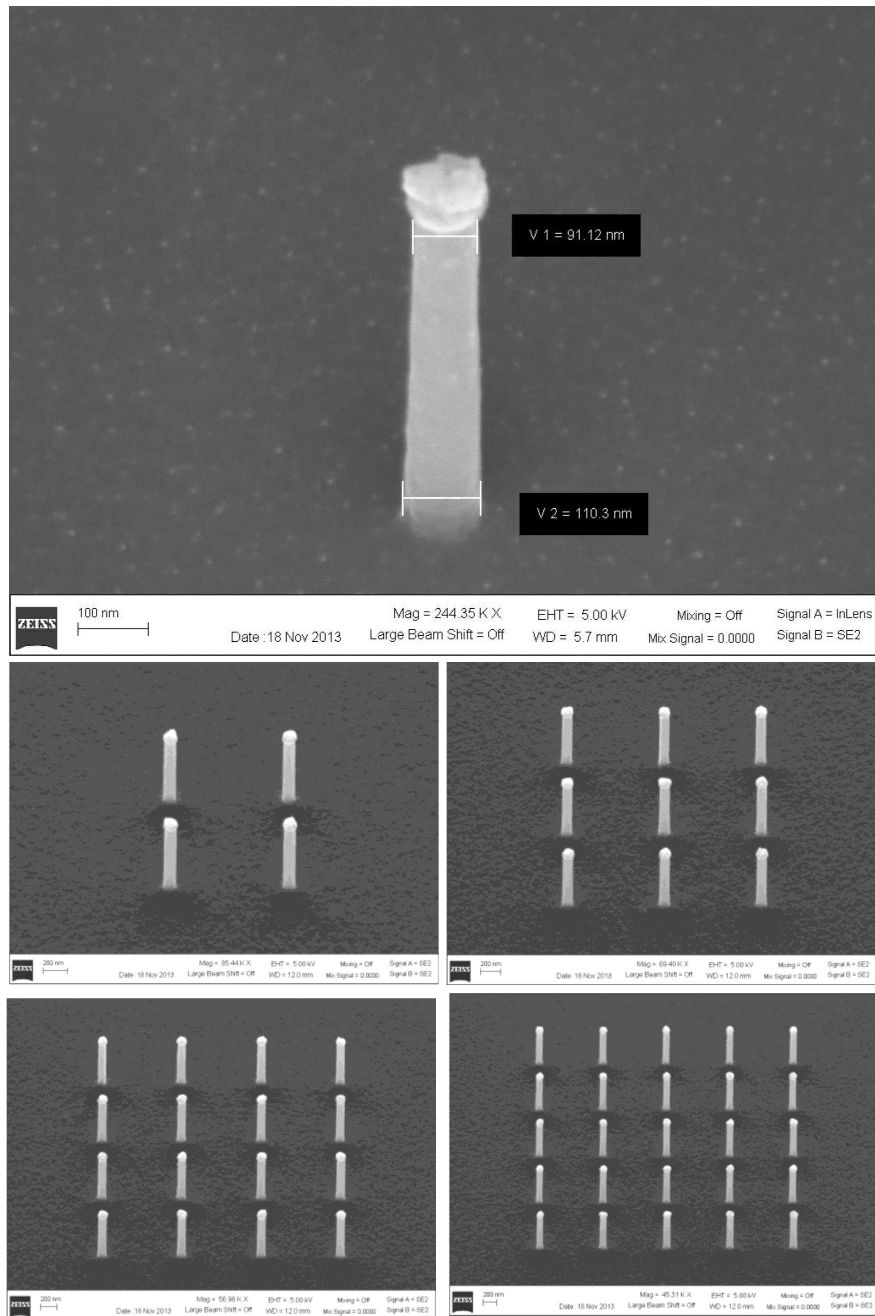


Figure 3. 13 Etched silicon nanowire array patterned by e-beam lithography and masked by Ti/Ni salicide. Nanowires height is ~ 720 nm and diameter is ~ 90 nm. Aspect ratio is ~ 1:8.

The fabrication process flow of silicon nanowire FETs is illustrated in Figure 3.14. First 200 Å Al_2O_3 was deposited by ALD on the nanowire as gate dielectric at 250˚C, followed by the PEALD 500Å TiN for gate metal in NH_3 atmosphere. Then a 500Å SiO_2 capping layer was deposited by PECVD to protect the gate metal (Figure 3.14 a-b)

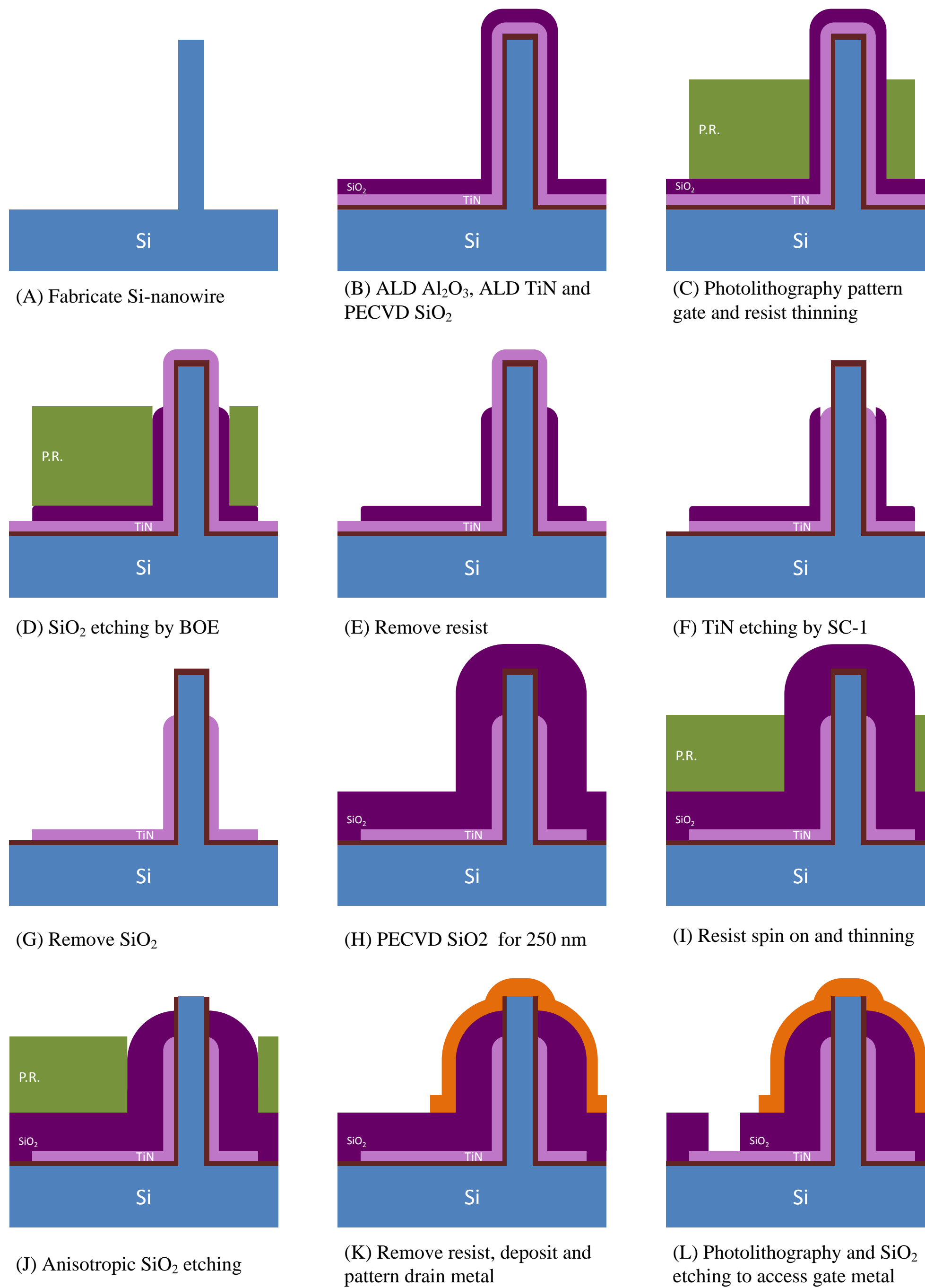


Figure 3. 14 Process flow of nanowire FETs

After the 3-step depositions, photolithography defined 200×500 μm^2 gate metal pads. After development and hard bake, the photoresist had a height of 0.9 μm so that the 720 nm-tall nanowires were completely buried by the resist. To vertically pattern the gate metal, a controllable O_2 plasma etch-back process was performed to thin the resist. After 2 min etch-back, residual resist only covered the bottom portion of nanowires, as shown in Figure 3.14c. The exposed SiO_2 capping layer was removed by 15sec BOE dip (Figure 3.14d) and afterwards SC-1 (NH_4OH:H_2O_2:H_2O = 1:1:5 at room temperature) solution etched upper portion of TiN to form the wrapped-gate pattern (Figure 3.14f). Figure 3.15a shows a device with 9 nanowires after the resist thinning and figure 3.15b exhibits the gate pattern after TiN was etched (resist was removed). The gate covers the lower portion of the nanowires and channel length is ~320nm. Gate overlap can be controlled by O_2 plasma thinning process. Figure 3.16 shows devices with different number of nanowires when the gate-all-around pattern was accomplished.

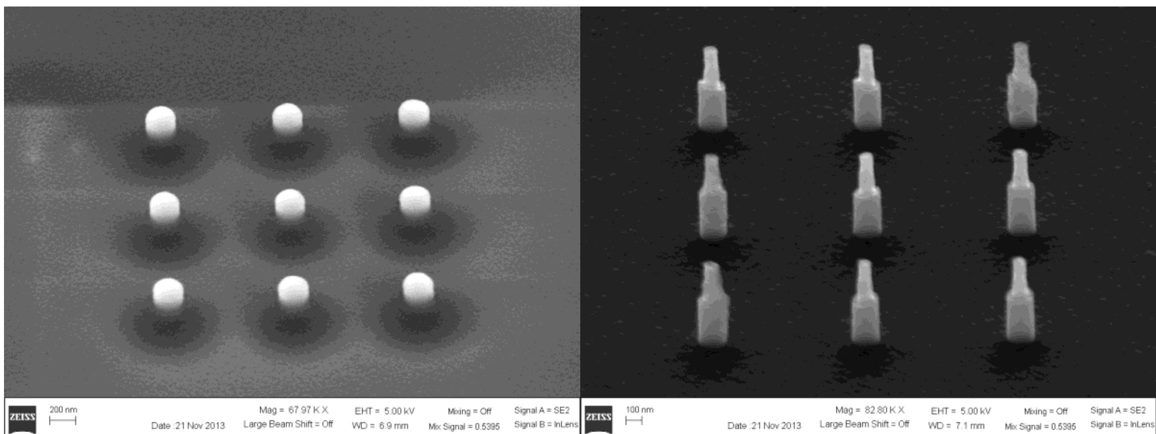


Figure 3. 15 nanowire FET after resist thinning (left) and gate patterning (right).

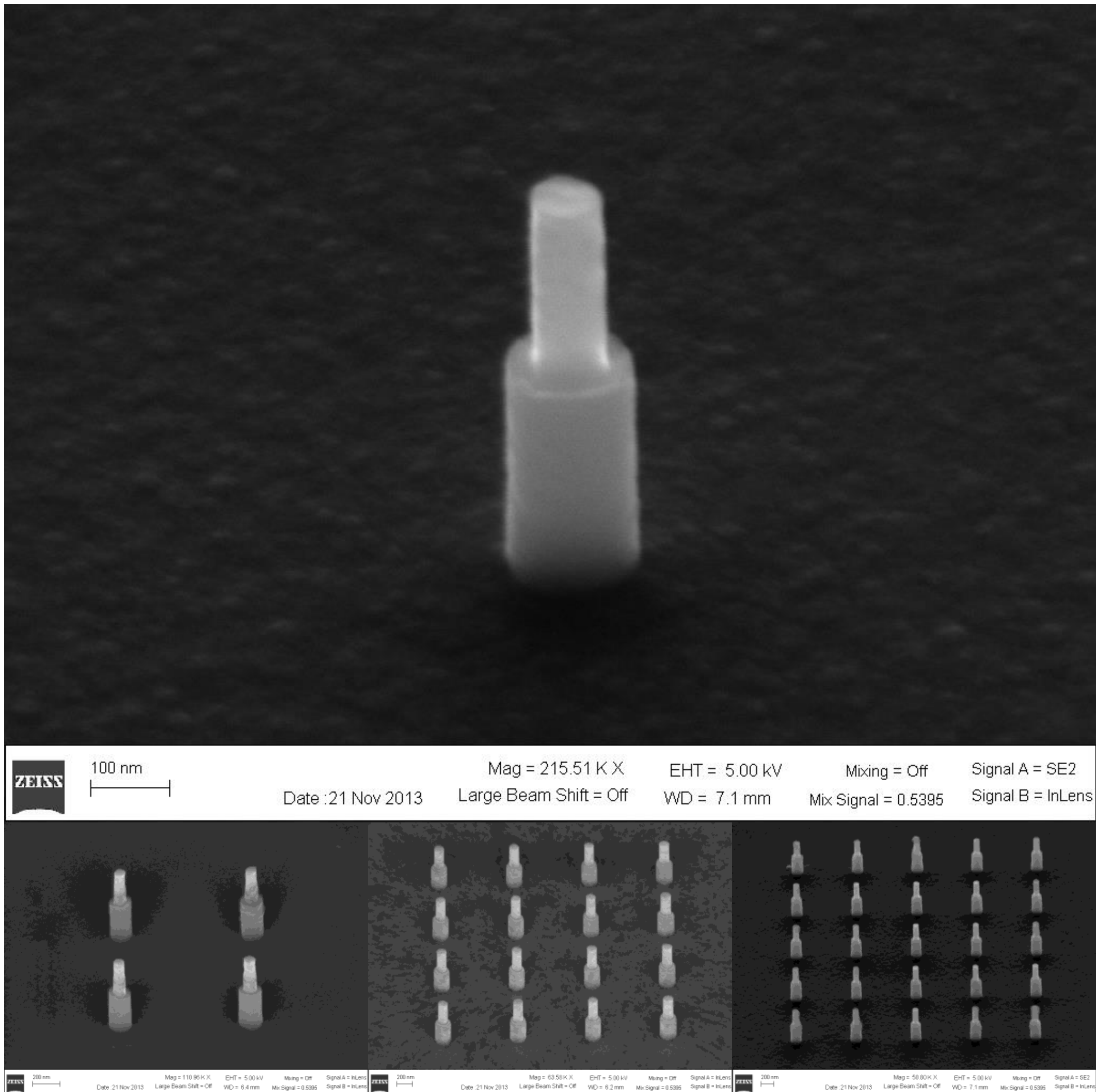


Figure 3. 16 Silicon nanowire FETs with vertical wrapped gate pattern.

To isolate the gate metal layer from the drain metal layer, a 250 nm PECVD SiO_2 film was deposited as inter-metal dielectric (Figure 3.14h). Similar to the gate vertical patterning, resist was spun-on and thinned with 130 sec O_2 plasma etch-back (Figure 3.14i). PECVD SiO_2 cap was removed by a controllable anisotropic plasma etch with a

mix gas of CHF_3 and O_2 (Figure 3.14j) to uncover the nanowires for the drain metallization. As shown in Figure 3.17, a 5 min etching consumed approximately 350 nm SiO_2 and exposed c.a. 100 nm Si nanowire core. Al_2O_3 gate dielectric on top of the nanowire was also broken through during the excessive plasma etching. From the image it can be observed that nanowire cores are uncovered from the PECVD SiO_2 and exposed to the drain metallization.

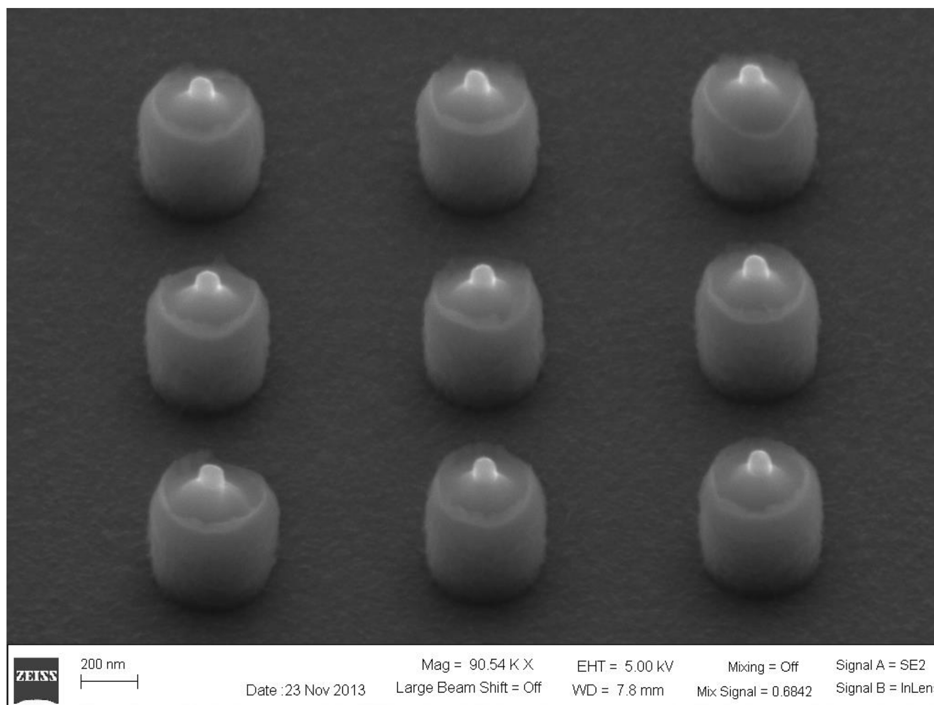


Figure 3. 17 Tilted SEM image of silicon nanowire FET after PECVD SiO_2 etch. Nanowire cores are exposed on top of the device for the drain metallization.

The drain contact pad was patterned by the 2nd photolithography and lifted-off. 150nm nickel film was deposited by e-beam assisted evaporation so that the metallization was formed with the salicide on nanowires (Figure 3.14k). To access the buried TiN gate

metal, contact windows through PECVD SiO_2 were opened by the 3rd photolithography and 2 min BOE dip (Figure 3.14l). Top-view microscope image is shown in Figure 3.18 for device layout illustration.

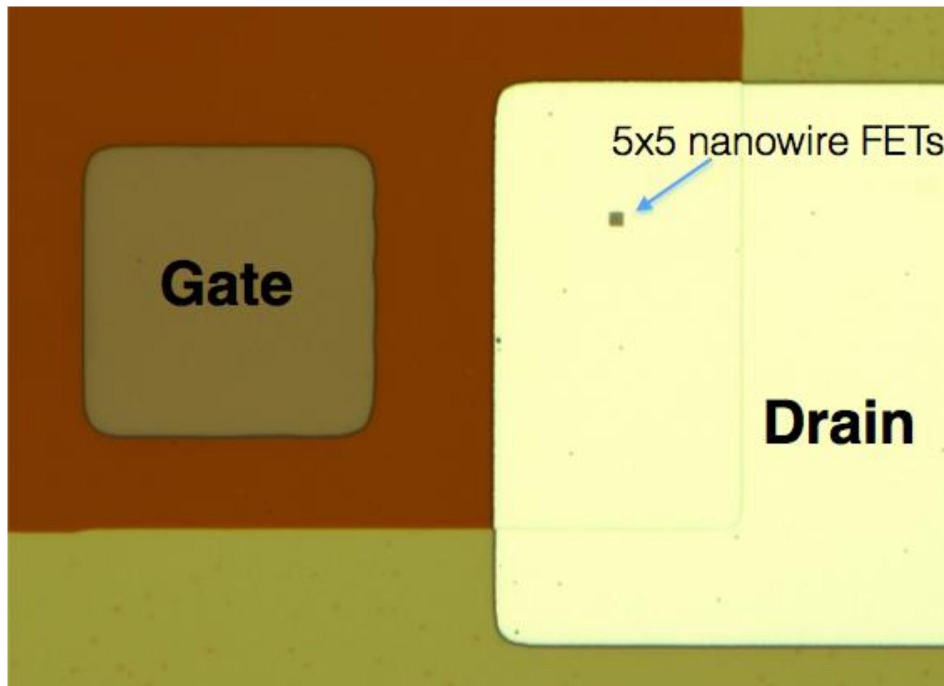


Figure 3. 18 Top-view microscope image of final device layout. Drain is the top nickel films and gate is buried under SiO_2 inter-metal dielectric. A contact window is opened by photolithography.

To gain the inside view of the fabricated nanowire FET, focused ion beam (FIB) was utilized to create a cross-section through a particular nanowire, along with the MOSFET structures. In Figure 3.19 a SEM image of the created cross-section is presented.

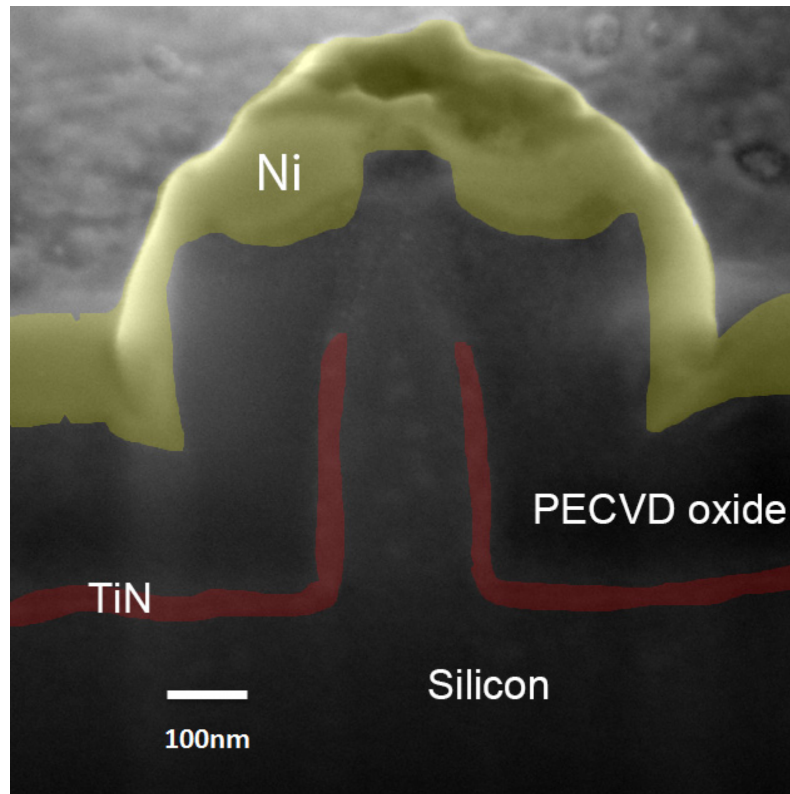


Figure 3. 19 Cross-sectional SEM image of a nanowire FET. The cross-section that is created by focused ion beam (FIB) cuts through the nanowire core.

3.3 DEVICE CHARACTERIZATION AND DISCUSSION

The fabricated vertical nanowire FETs were characterized at room temperature using the substrate as the source. The transfer characteristic (I_d-V_g) indicates that the Si nanowire FET behaves as a typical p-MOS field-effect-transistor and the result is plotted in Figure 3.19. This characterized device has 25 nanowires in parallel, with a channel length of approximately 320nm. Each nanowire has a diameter of 90 nm and a gate dielectric of 200 Å Al_2O_3, i.e. ~10 nm effective oxide thickness (EOT). The gate voltage is swept from 1 V to -2 V with a step of -0.02 V, while V_{DS} is kept at -0.2 V and -1.0 V. The I_d-V_g curve shows a good DC characteristic with the I_{on}/I_{off} ratio >10^5. The on-state

current is 11.8 μA, achieved at V_{DS} = -1 V and V_{GS} = -2 V, compared to an off-state current that is below 10^{-10} A when V_{DS} = -1 V and V_{GS} = 1 V. Considering that this device has 25 nanowires in parallel, each nanowire contributes a current of ~ 0.47 μA. The measured curve also shows a very small threshold voltage (V_{th}) roll-off with V_{DS}: the drain induced barrier lowering (DIBL) measured at I_{DS} = 100 nA is 25 mV/V. The sub-threshold swing (SS) of the champion device is 87mV/dec and 96mV/dec extracted at V_{DS} = -0.2 V and -1 V, respectively.

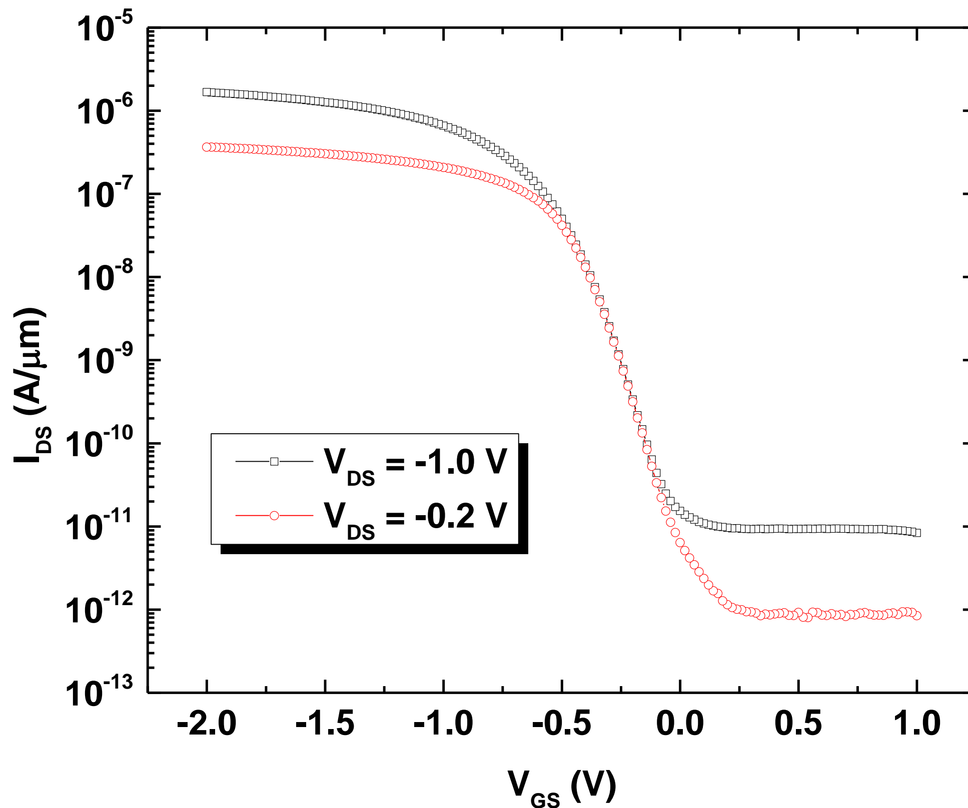


Figure 3. 20 Measured transfer characteristics of a silicon nanowire FET with 25 nanowires in parallel.

The measured output characteristic (I_d-V_d) is plotted in Figure 3.21. V_{DS} is swept from 0 to -2 V, and V_{GS} ramps from 1 V to -1.5 V with a step of -0.5 V. The device behaves as an excellent long channel-like pMOS. For a certain V_{GS}, the output current enters the saturation region with the increase of V_{DS}.

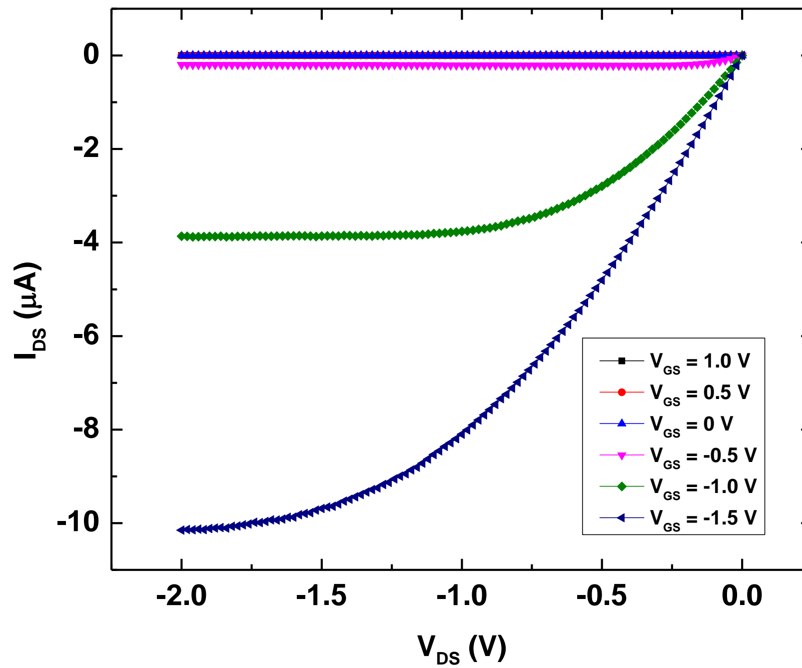


Figure 3. 21 Measured output characteristics of silicon nanowire FET with 25 nanowires in parallel.

The trans-conductance (g_m) of the tested device is also extracted and plotted in Figure 3.21 at V_{DS} = -0.2 V. The maximum g_m is achieved at V_{GS} = -0.56 V.

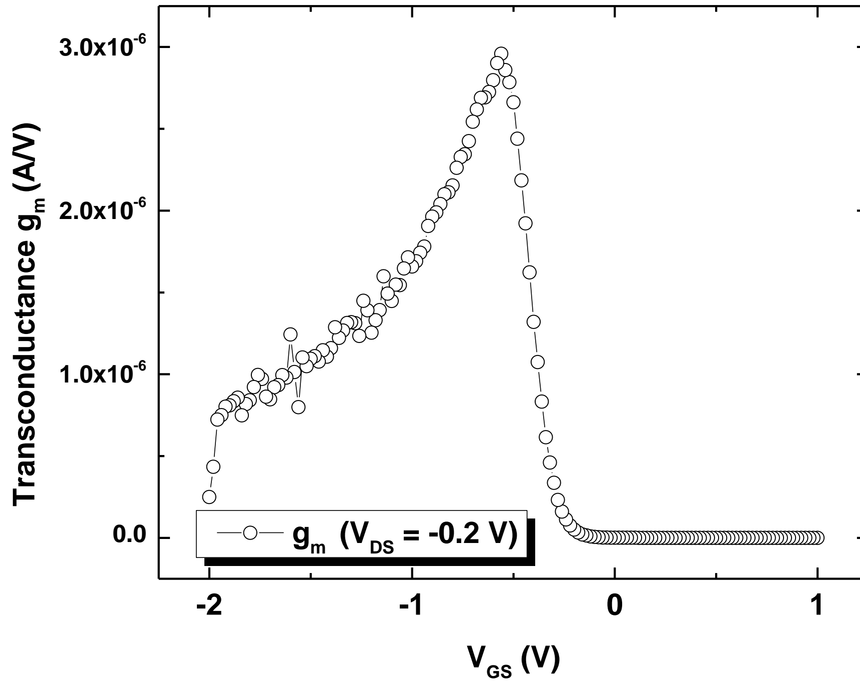


Figure 3. 22 Trans-conductance of silicon nanowire FET measured at V_{DS} = -0.2 V.

The drive current of a MOSFET can be expressed by

$$I_{DS} = \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \ (V_{DS} < V_{GS} - V_{th})$$

$$I_{DS,sat} = \frac{W}{L}\mu C_{ox}\left[\frac{(V_{GS} - V_{th})^2}{2}\right] \ (V_{DS} \geq V_{GS} - V_{th})$$

The trans-conductance g_m quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}}$$

In a small V_{DS} (linear region), g_m can be expressed by

$$g_m = \frac{\partial I_d}{\partial V_{GS}}|_{V_{DS}} = \frac{W}{L}\mu C_{ox} V_{DS}$$

Therefore the carrier mobility μ can be extracted by:

$$\mu = \frac{g_m L}{W C_{ox} V_{DS}}$$

where L is the channel length and W is the channel width. C_{ox} is the gate oxide capacitance.

In the tested device, the channel length is 320 nm. As for the channel width, each nanowire has a diameter of ~ 90nm and thus the effective width per nanowire is the circumference: ~ 283 nm. Considering that there are 25 nanowires in parallel in this device, the total effective channel width is 7.065 μm.

The oxide capacitance can be calculated by $C_{ox} = \frac{\varepsilon_s \varepsilon_0}{d}$ for planar MOSFETs, where d is the dielectric thickness, ε_s is the relative permittivity of the dielectric and ε_0 is the vacuum permittivity. Table 3.4 summarizes the parameters that we used to extract the hole mobility. Therefore the extracted hole mobility is 2.16 cm^2/V sec.

For the gate-all-around structure, it is more accurate to use the cylinder capacitor model to calculate the total capacitor per nanowire:

$$C_{cylinder} = \frac{2\pi\varepsilon_0\varepsilon_s h}{\ln(b/a)}$$

where h is the height of the cylinder, a the radius of the Si-nanowire and b the radius to the TiN gate. Therefore we have $b = a + d$.

The re-calculated hole mobility is 0.97 cm^2/V sec by the cylinder capacitor model. The relatively low mobility can probably be attributed to the non-ideal external contact resistance, i.e. from the low doping concentration in the source.

Parameters	Value
ε_s	7
ε_0	8.85×10^{-12} m/F
a	90 nm
b	110 nm
d	20 nm
h or (L)	320 nm
$W = 2\pi r$	283 nm

Table 3. 4 Parameters and constants for hole mobility extraction in silicon nanowire FETs.

The fabricated devices were also characterized at 77K for the low temperature performance. The sample was cooled down by liquid nitrogen (LN_2) and the transfer characteristic was measured. Figure 3.22 shows the comparison of the low temperature and room temperature transfer characteristics with V_{DS} = -0.2 V. Compared to the room temperature performance, steeper sub-threshold slope is observed at 77K, with a

reduction in the drive current and an increase in $|V_{th}|$. The extracted sub-threshold swing at 77K is 65 mV/dec, compared to 87 mV/dec that is extracted at room temperature.

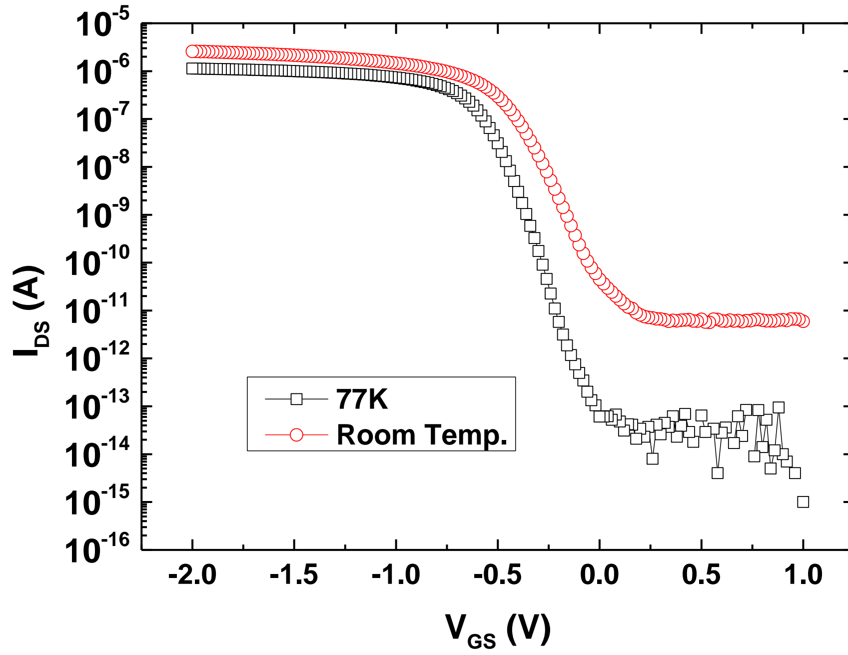


Figure 3. 23 Low temperature transfer characteristics compared with room temperature.

Chapter 4 Double gate power MOSFET Introduction

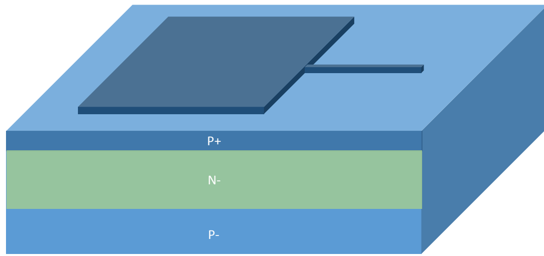
4.1 Process development of vertically diffused finFET

Vertically diffused finFETs inherit the processes developed for nanowire FETs in the previous chapters. Comparable to the nanowire FETs, p-type vertically diffused finFET was fabricated with a p-n-p doping profile. A similar epitaxial silicon wafer was utilized and doping was pre-diffused before the fin was etched. The lightly doped epitaxy p- layer was 7-11 μm in thickness and serves as the drift-region, therefore the substrate was used as the drain for potential power applications. Phosphorus was implanted at 100 keV, followed by 1-hour diffusion at 1000˚C to dope the n-type channel region. The junction depth is 470nm below the wafer surface. The second boron implantation with an energy of 20 keV and a dosage of $5x10^{15}/cm^2$ followed by 10sec rapid thermal anneal at 1000˚C doped the drain region. Simulation result indicates that the source doping has a peak concentration of 10^{21} $/cm^3$ and a junction depth of 140nm, while the peak concentration in n-type channel is 10^{17} $/cm^3$ and the channel length is around 320 nm. Implantation and annealing conditions are summarized in Table 4.1.

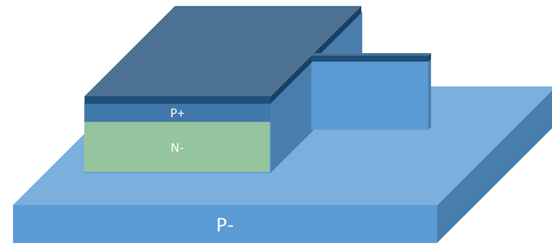
	Phosphorus Implant (Channel)	Boron Implant (Source)
Energy	100 keV	20 keV
Dose	10^{13} cm^{-2}	5×10^{15} cm^{-2}
Tilt	0°	7°
Anneal Temp.	1000^oC	1000^oC
Anneal Time	1 hr	10 sec

Table 4. 1 Implantation and annealing conditions for vertically diffused finFET doping.

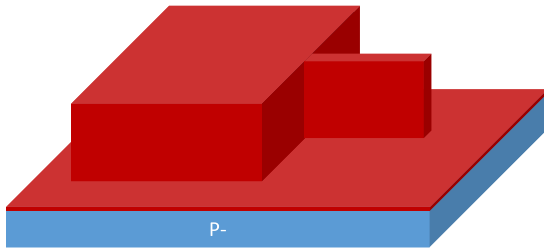
The process flow is illustrated in Figure 4.1. After the 2-step ion implantations and annealing, the fins and mesas were patterned by JOEL e-beam lithography. The electron beam exposed an area of 50 nm × 15 μm for the fin pattern, adjoining to a 50 × 50 μm^2 square for the source contact mesa. After the resist was developed, 200Å Ti followed by 200Å Ni was deposited on the sample with the e-beam-assisted evaporation. Unwanted metal was lifted off by an overnight soaking in remover PG. After an oxygen plasma descum, the sample was annealed in N_2 atmosphere for 10 sec at 600˚C to form the salicide. The subsequent 30 cycles DSE consumed 720 nm silicon and thus formed the fin structure as well as the mesa. We fabricated a variety of devices with 1, 2, 3 and 4 fins. Figure 4.2 shows a tilted SEM image of the etched fin structure.



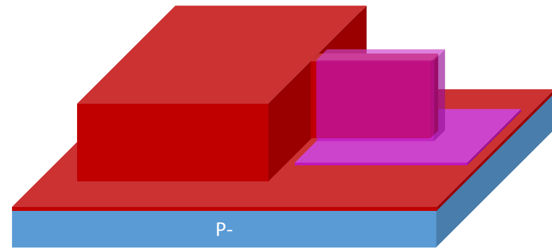
A) Pattern fin and mesa by e-beam lithography, metal evaporation and lift-off. Anneal to form salicide



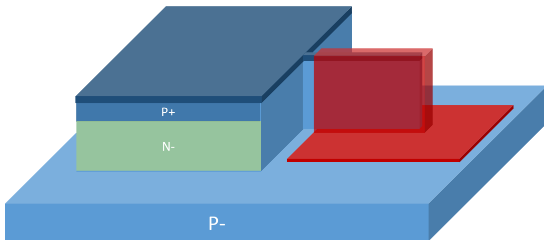
B) Deep silicon etch to form the fin and mesa



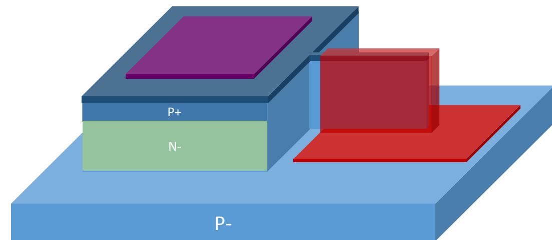
C) ALD 200 Å Al_2O_3 gate dielectric and plasma enhanced ALD 250 Å gate metal



D) PECVD SiO2 capping layer and photo-lithography to define gate contact pad



E) TiN wet etch and SiO2 wet etch



F) Photo-lithography to open source contact via and Al_2O_3 wet etch. Source metal evaporation and lift-off

Figure 4. 1 Illustration of process flow for vertically diffused finFET

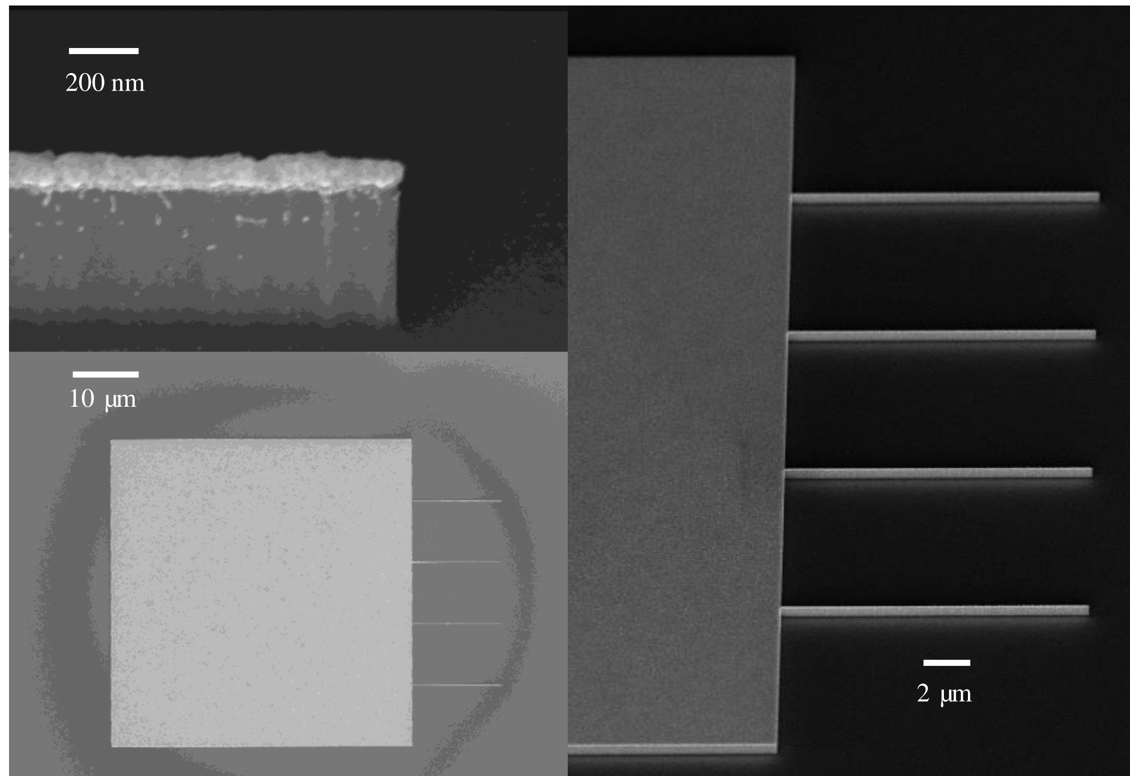


Figure 4. 2 Etched fins after 30 cycles of deep silicon etch. Right image is a 45° tilted SEM image of a vertically diffused finFET with 4 fins. The length of the fin is 15 μm. Left upper is a close-up image of at the tip of an etched fin. The width of the fin is around 70 nm after the salicide annealing. Left Lower is the top view of the device layout.

Afterwards, the sample was cleaned with piranha and diluted HF. A sequence of ALD 200Å Al_2O_3, PEALD 250 Å TiN and PECVD 500Å SiO_2 was deposited, which covered the entire sample. Photolithography defined 100 x 100 μm^2 gate contact pads that overlapped the fins but excluded the mesa. Unmasked SiO_2 was removed by 15 sec BOE dip, followed by an isotropic TiN wet etch to pattern the gate metal. Excessive SiO_2 was removed by another 15 sec BOE dip.

The 2nd photolithography opened a window on the top of the mesa. Al_2O_3 was etched by 3 min BOE dip and thus the buried salicide layer was exposed. A 150 nm nickel film was deposited by e-beam assisted evaporation and then lifted off as a source contact pad. Tilted SEM images of the completed devices with different fin numbers are shown in Figure 4.3. A cross-sectional TEM image of one fin is shown in Figure 4.4, as well as a high magnification TEM image of salicide.

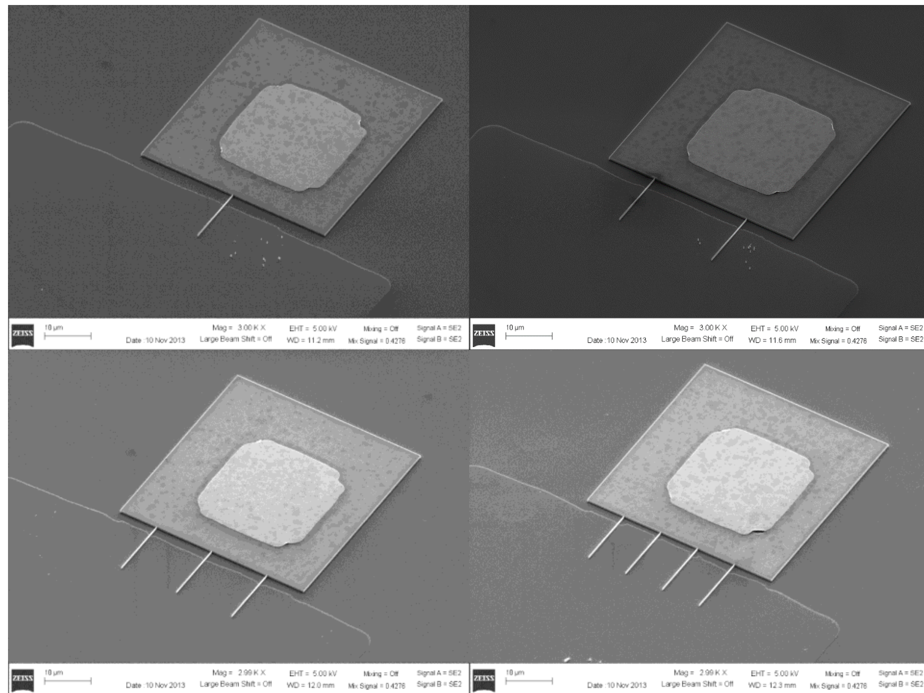


Figure 4. 3 Completed vertically diffused finFET.

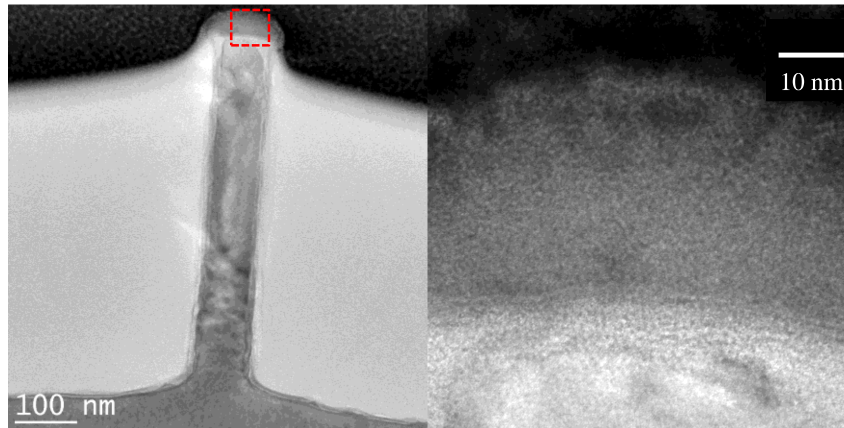


Figure 4. 4 TEM images of the fin cross-section and high magnification image of salicide on top of the fin.

4.2 DEVICE CHARACTERIZATION AND DISCUSSION

Fabricated vertically diffused finFETs were characterized at room temperature and the performances were compared among the devices with different fin numbers. We first utilized the configuration that is suitable for power application, i.e. the top electrode was connected as the source while the bottom substrate as the drain. Transfer characteristics (I_d-V_g) were measured and plotted in Figure 4.5. Test results indicate that the devices behave as typical p-MOS transistors with an I_{on}/I_{off} ratio more than one magnitude. The drive currents are measured at a small V_{DS} = -0.2 V and a large V_{DS} = -1.0V, while V_{GS} is swept from 1.0 V to -2.0 V. The on-state currents achieved at V_{GS} = -2.0V and V_{DS} = -1.0V are 8.98×10^{-5} A, 1.44×10^{-4} A, 2.05×10^{-4} A and 2.59×10^{-4} A for devices with 1, 2, 3 and 4 fins, respectively. The relatively high off-state current can probably be attributed to the large junction leakage on the mesa and further discussion is included in the following section.

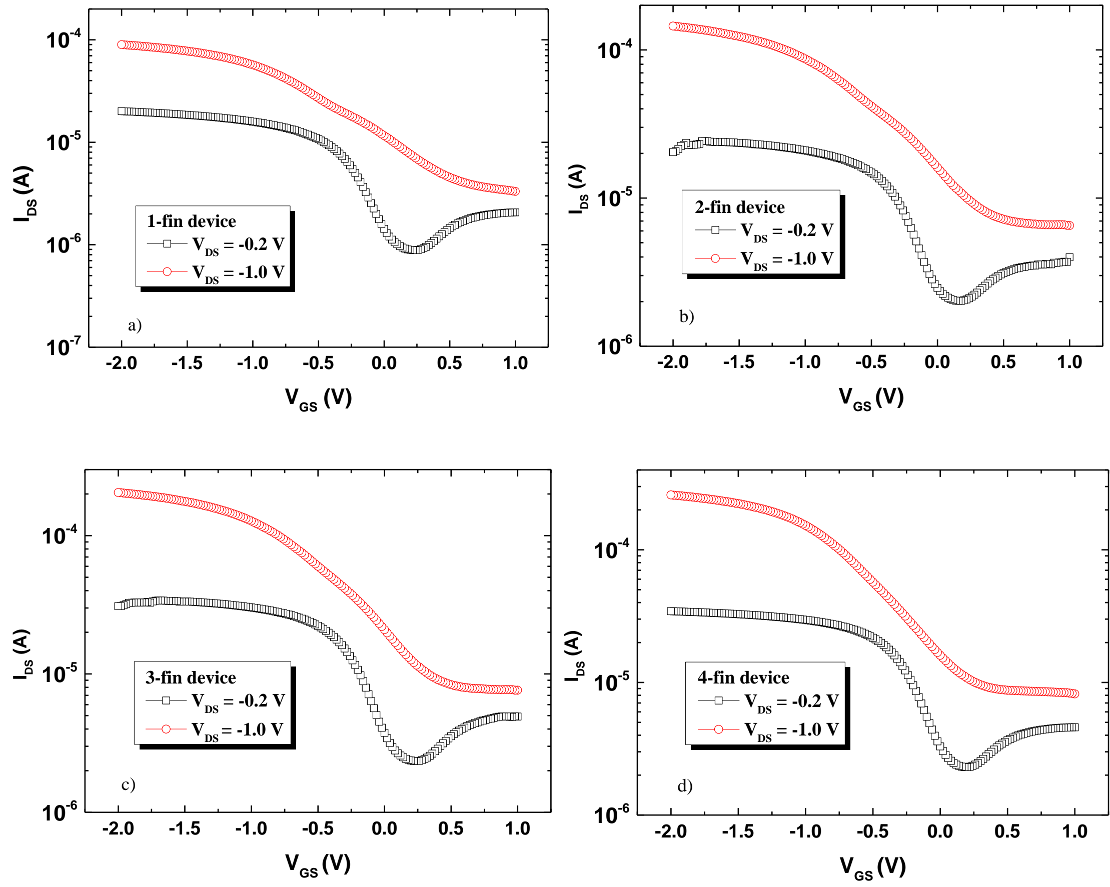


Figure 4. 5 Transfer characteristics of fabricated vertically diffused finFETs with 1-fin (a), 2 fins (b), 3 fins (c) and 4 fins (d).

Though performances are slight different between deivces, larger drive current is achieved as the fin number increses, as expected. We plot the ON-current versus the fin number for these four devices in Figure 4.6. Linear dependence of the drive current on the fin number is observed. The output characteristics are also measured and plotted in Figure 4.7.

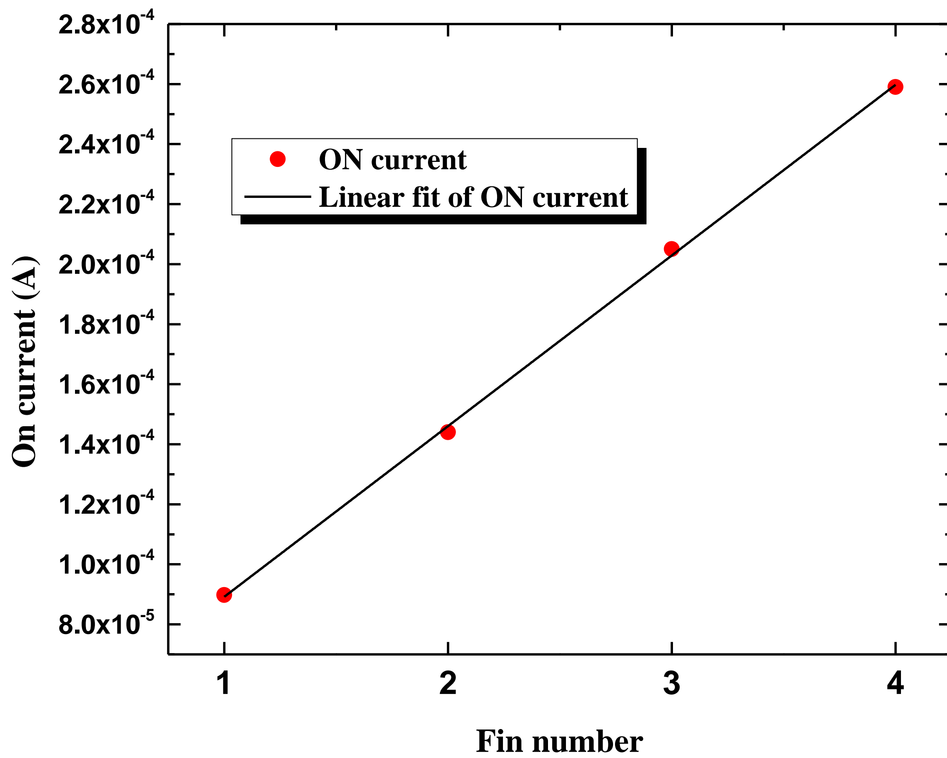


Figure 4. 6 ON-current versus fin number in one device. Linear dependence is observed.

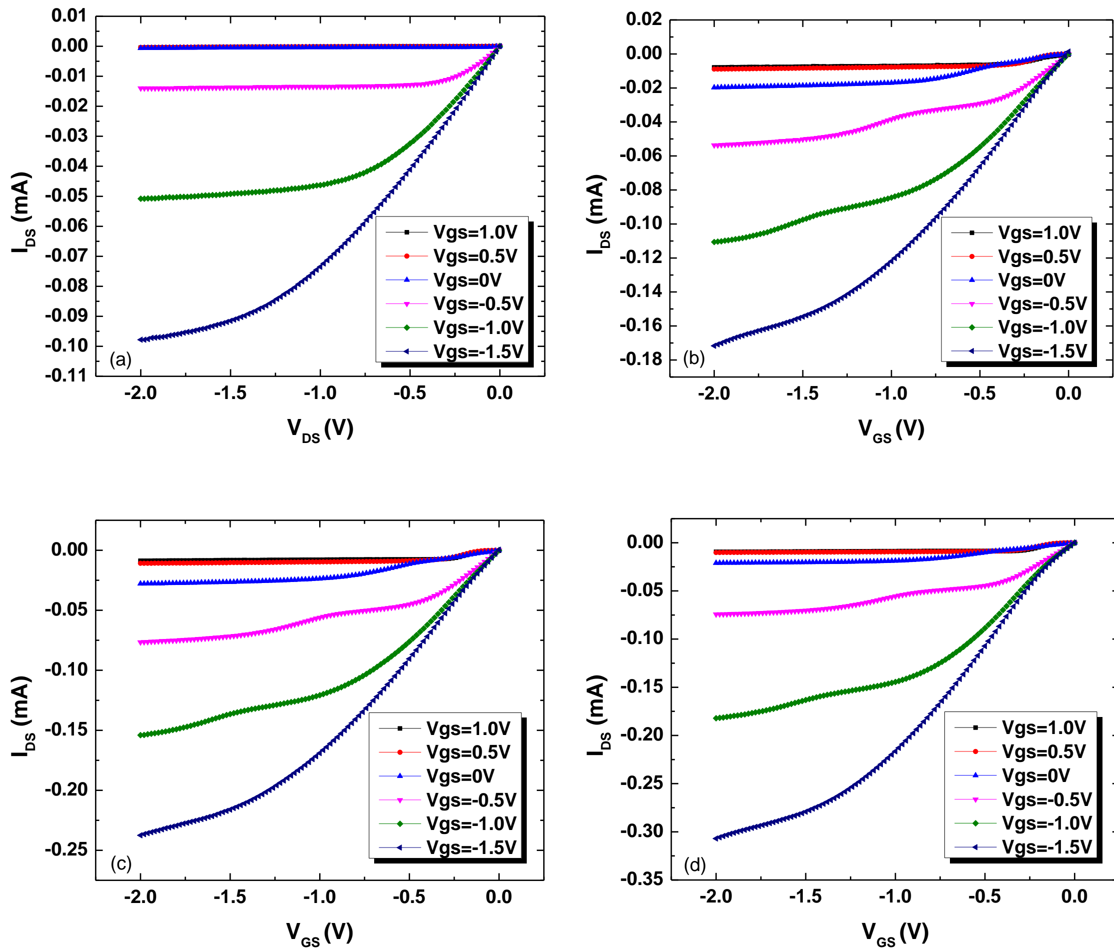


Figure 4. 7 Output characteristics of vertically diffused finFETs with fin number from 1-4 in (a) to (d), respectively.

Interestingly the off-state current is significantly reduced when the source/drain configuration is swapped. In Figure 4.7 we plot the transfer characteristic of a 4-fin device with lowest off-state current in swapped source/drain configuration, and compared it with the original measurement on the same device. The comparison indicates that the on-state current is not affected by the change of the configuration, whereas the off-state current is reduced by 2 orders of magnitude.

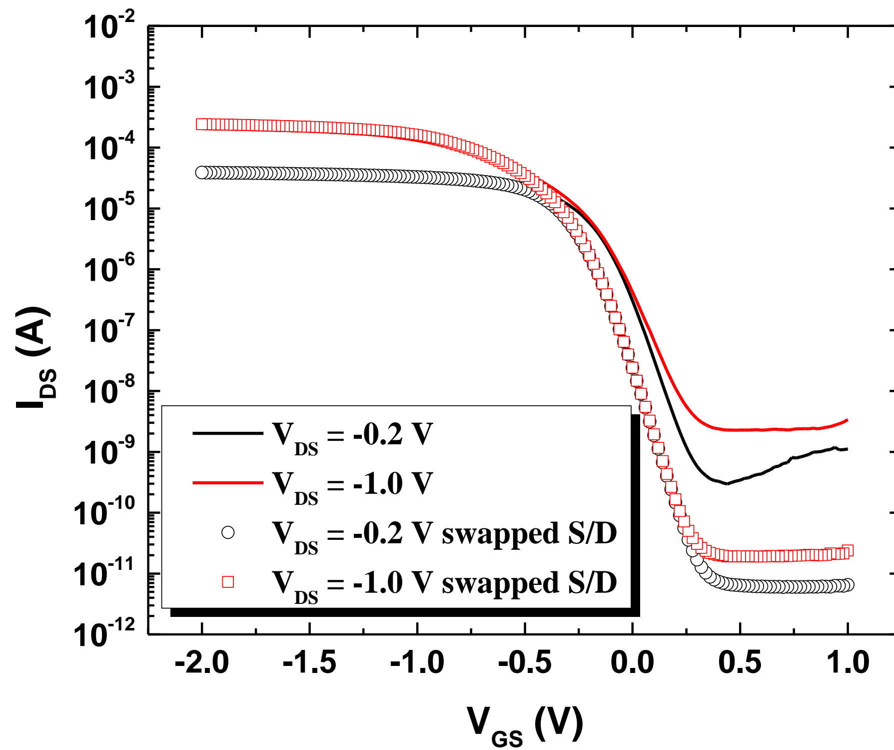


Figure 4. 8 Transfer characterization comparison of the swapped S/D configuration and the original S/D configuration.

For p-type MOSFETs, the source and drain are doped by acceptors while the channel is doped by donors. In off-state, i.e. $V_{GS} >0$ and $V_{DS} <0$, the p-n junction of

source to channel (source junction) is forward biased while the channel-drain junction (drain junction) is reverse biased. In this device, a large area mesa (50×50 μm^2) is connected to the device in parallel, sharing the same doping profile with the fins. Therefore there are two p-n junctions under the mesa: the top junction and bottom junction, corresponding to the source junction and the drain junction in the fin. It is also noted that these junctions are out of the gate control; consequently the off-state current is largely determined by the reverse leakage current of the two junctions.

When the device is characterized with the original configuration, where top electrode is grounded and negative voltage is applied to the substrate, the off-state current is determined by the reverse leakage of the bottom junction in the mesa, whereas, when source/drain is swapped, i.e. the bottom electrode is grounded and negative voltage is applied on the top, the off-state leakage current is determined by the top junction reverse leakage current.

For a p-n junction, the I-V characteristics can be express by:

$$I = I_s(e^{V_D/(nV_T)} - 1)$$

where V_D is the voltage across the junction. V_T is the thermal voltage defined as :

$$V_T = k_B T/q$$

Under a negative bias, i.e. $V_D < 0$, the reverse junction leakage is the saturation current:

$$I \approx I_s$$

The saturation current can be expressed theoretically by:

$$I_s = eA\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right)$$

where e is the electron charge, A is the cross-sectional area, $D_{p,n}$ are the diffusion coefficients of holes and electrons, respectively, $N_{A,D}$ is the donor and acceptor concentrations in the p-type side and n-type side, respectively, n_i is the intrinsic carrier concentration, and $\tau_{p,n}$ is the carrier lifetimes of holes and electrons, respectively.

Therefore, approximately the saturation current is largely determined by the lightly doped side in an asymmetric doped junction, assuming the $\sqrt{\frac{D_p}{\tau_p}}$ and $\sqrt{\frac{D_n}{\tau_n}}$ are of the same magnitude.

Referring to the doping concentration profile of the device structure and the analysis above, it can be concluded that the off-state current is $\propto 1/N_{A,source}$, where $N_{A,source}$ is the doping concentration in the lightly doped side of the bottom junction, if the original source/drain configuration is applied, whereas the off-state current of the swapped source/drain configuration is $\propto 1/N_{D,channel}$, where $N_{D,channel}$ is doping concentration in the lightly doped side of the top junction. Since the channel doping is ~ $10^{17}/cm^3$, which is two orders of magnitude larger than the source doping ($10^{15}/cm^3$), the off-state current is reduced by two orders of magnitudes by swapping the source and drain.

The fabricated devices were also characterized at 77K for the low temperature performance. The sample was cooled down by liquid nitrogen (LN_2) and the transfer

characteristic was measured. Figure 4.8 shows the comparison of the low temperature and room temperature transfer characteristics with V_{DS} = -0.2 V. Comparing with the room temperature performance, steeper sub-threshold slope is observed at 77K, with a reduction in the drive current and an increase in $|V_{th}|$.

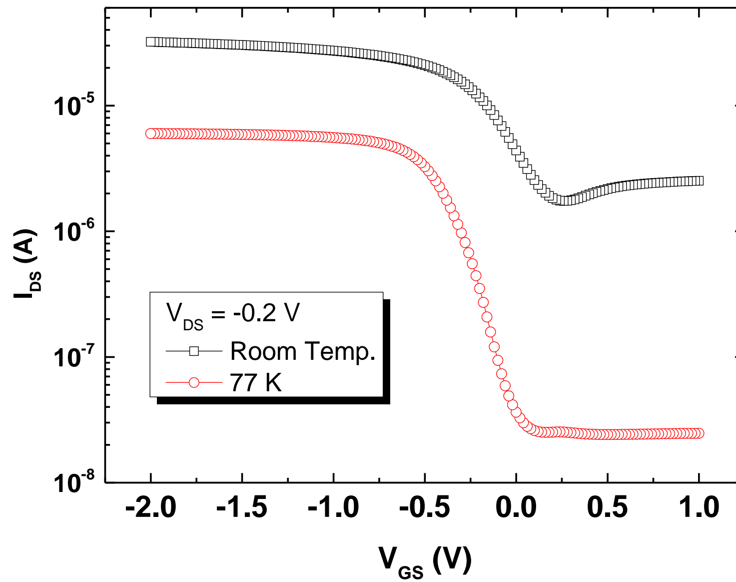


Figure 4. 9 Low temperature transfer characteristic comparing with room temperature. V_{DS} = -0.2V

Breakdown voltage test is also performed for vertically diffused finFET. Figure 4.10, which shows I_{DS} versus V_{DS} plots with V_{GS} = 0 V was used to characterize BV_{DSS}. No significant breakdown is observed below 20 V.

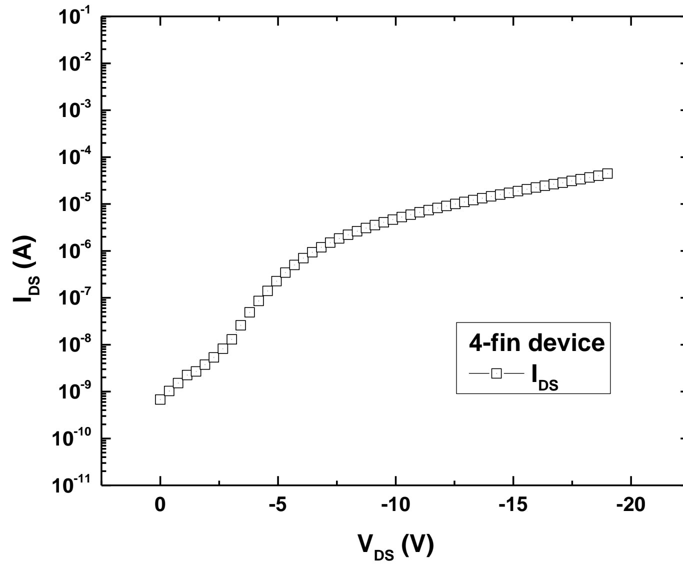


Figure 4.10 Breakdown test on vertically diffused fin FET

Chapter 5 Flexible thin-film transistors exfoliated from bulk wafer

5.1 PROCESS REVIEW OF FLEXIBLE ELECTRONICS

Mechanically flexible integrated circuits and electronic systems have received a lot of attention. Unlike traditional electronic devices which are typically fabricated on bulk, rigid Si wafers with a thickness of ~ 700 microns, flexible integrated circuits, using thin-film-transistors (TFTs), are usually mounted on a bendable substrate such as plastic or polyimide. Such mechanical flexibility enables new classes of applications beyond traditional electronics products, for example, flexible displays, electronic textiles and "epidermal" electronics.[37-39]

Mechanically flexible organic film transistors, for instance, based on pentacene have been demonstrated[53, 54]. However, the low carrier mobility, and thus low drive current and high operating voltage, still remains as a major challenge for this kind of organic material [55]. To achieve higher mobility and performance, inorganic semiconductors are attractive candidates for flexible electronics.

One of the most successful inorganic TFTs is based on hydrogenated amorphous silicon (a-Si:H) [41]. This technique involves low temperature RF plasma enhanced chemical vapor deposition (PECVD), to deposit thin film amorphous silicon on plastics or glass substrates. The quality of the a-Si:H can be engineered by deposition parameters such as temperature and hydrogen concentration [40]. To directly deposit a-Si on plastic substrates, the process temperature must be below the thermal degradation temperature of the plastic, which limits the quality of the a-Si:H film, and results in low carrier mobility. For instance, a 75C RF-PECVD a-Si:H film with a thickness of 50nm shows a very low carrier mobility of 0.4 cm^2/Vs [42], while 150C PECVD with higher RF power produces nanocrystalline-Si and increases the mobility to still a modest value

of 12 cm^2/Vs [56]. To achieve better performance, higher temperature and hydrogen concentration are required, which are often precluded on plastic substrates.

Carrier mobility can be drastically improved by substituting single crystalline silicon for a-Si [57]. To maintain the mechanical flexibility, single crystal nanowire devices on flexible substrates have been demonstrated. Single crystalline nanowires can be prepared by the well-known vapor-liquid-solid (VLS) approach [25]. In this bottom-up technique, a metal catalyst is deposited on a "donor" substrate which can withstand high temperatures, and high quality single crystalline nanowires are grown at temperatures of several hundred degrees Centigrade using a gas precursor [58]. The nanowires are transferred from the donor substrate to a flexible "receiver" substrate, for example glass or plastic, which might not be able to withstand high temperatures. It usually requires additional tricks to achieve aligned monolayer nanowires in the desired location and orientation on the receiver. The Javey group has developed innovative contact printing techniques that exploits sliding frictional forces between the donor and the receiver wafer whose surface is pre-treated with specially terminated chemical bonds, for instance, $–NH_2$, to maximize adhesion. Consequently, the transferred nanowires are mostly aligned in the direction of sliding. Schottky diodes on bendable plastic substrates made with nanowires have been demonstrated. Doping the transferred nanowires is difficult since the high temperature activation of the dopants is not compatible with the plastic substrate [59].

Instead of bottom-up VLS growth, top-down approach to fabricating nano-ribbons or thin-film single crystalline silicon from conventional wafers has also been reported. This technique involves fabrication of arrays of devices, lifting off thin-film silicon and transfer printing. First, photolithography defines the active region of device or ICs arrays. Conventional CMOS fabrication process flow is carried out, including high temperature

source/drain (S/D) dopant activation, thermal gate oxide growth and metallization anneals. The wafer is then covered by passivation layer such as PECVD Si_3N_4 or SiO_2, and subsequent reactive ion etching (RIE) opens trenches through the passivation and down to the sacrificial layer outside the active region. The sacrificial layer can be either (111) silicon that can be anisotropically etched by KOH or TMAH, or buried oxide (BOx) in a silicon-on-insulator (SOI) substrate that can be selectively etched by hydrofluoric acid[60, 61]. For example, the Rogers group uses (111) silicon and defines strip patterns with sidewall terminated on (110) planes. After a shallow RIE, top surface and parts of the sidewalls of the trenches are coated with thin SiO_2 and Au. A subsequent anisotropic KOH wet etch that is highly selective to (110) over (111), undercuts the masked strips and generates nano-ribbons. The ribbons are then contact printed by Polydimethylsiloxane (PDMS) onto a polyethylene terephthalate (PET) substrate. Back-gate MOSFETs were fabricated, using indium tin oxide (ITO) on the backside of PET as the common gate and PET as dielectric. The devices exhibited a mobility of $360cm^2/Vs$ and I_{ON}/I_{OFF} ratio of 10^3 [62, 63].

Transfer printing that enables parallel assembly of massive numbers of thin-film devices from the donor wafer onto the receiver substrate is becoming a mature technique. Semprius Inc. has demonstrated an approach that utilizes SOI wafer to fabricate thin film transistors and transfer print, with yields in excess of 99.5% and alignment accuracies better than 5 μm. Device arrays are pre-fabricated with conventional CMOS process on SOI wafer. After a passivation layer encapsulates the devices, deep trenches in the periphery of the active region are etched down to the buried oxide. Hydrofluoric acid etches the sacrificial oxide and frees the thin film silicon from the substrate. An elasto-metric transfer stamp is designed to have well-defined posts corresponding to the device pattern. Transfer process is carried on a specific transfer printer which is able to precisely

align the transfer-stamp to the source wafer. In a test vehicle, Semprius Inc. successfully transfer printed 1024 ICs within 4μm misalignment[64].

5.2 Process of wafer exfoliation

Here, we discuss a new, simpler approach to fabricate high performance flexible electronic devices and circuits based on a wafer-scale thin crystalline Si film exfoliation scheme similar to spallation [65, 66]. Devices and circuits are fabricated using a conventional CMOS process flow on a bulk Si wafer. Devices are not restricted to nano-ribbons or nanowires as in other approaches, and, because devices are made on a bulk silicon wafer, the process temperature is not limited by the plastic substrate as mentioned before. In this work, p-MOSFET and n-MOSFETs s with a variety of channel lengths from 150 nm to 1 μm, as well as capacitor and diode test structures were fabricated on conventional 8-inch wafers using a standard 0.13μm CMOS process flow with poly-Si gate and 20Å SiO_2 gate dielectric. After final metallization and passivation, the contact pads were opened up for probing.

Subsequently, a mechanical exfoliation process was carried out to peel off the top 25-30 μm of silicon, from the bulk wafer. The CMOS devices are contained in the top ~1 μm of the exfoliated Si film. This process, previously developed for solar cells where Si substrate cost is paramount [67], has been adapted to CMOS applications to produce flexible ultra-thin Si ICs. As depicted in figure 5.1, the process begins with the deposition of a 70 nm PECVD silicon nitride film over the whole wafer as an isolation layer, followed by e-beam assisted evaporation of nickel as metal seed layer. Subsequently a nickel film is electroplated over the wafer with typical thickness ranges from 10-100 μm, and the wafer is subjected to a low temperature annealing (<300°C)

treatment which results in a negative residual strain in the nickel film, as shown in Figure 5.1 (D). The stress fields in the metal film and underlying wafer resulting from the negative residual strain provide the driving force for the exfoliation. An electromechanical wedge is then used to create and propagate a sub-surface crack across the wafer, which results in exfoliation of the top 20-30 μm of the silicon wafer, along with all pre-fabricated electronic devices and circuits. While this process is used in solar cells for reducing cost of Si by enabling substrate reuse, in CMOS applications this process enables flexible form factor of high performance devices, which was not easily possible with the previously developed approaches described in previous sections.

The thickness of the exfoliated Si can be controlled between 10 and 80μm by modulating the residual stresses in the metal and Si substrate system, which are determined by the annealing temperature, metal profile and the electroplating process that introduces stresses in the metal during plating. Annealing temperature is below 300°C, making the process compatible with standard back end of line (BEOL) process. The electroplated nickel can be deposited with a thickness from 10 to 100 μm to produce 10 to 80 μm exfoliated silicon film. While it is ideal for photo-voltaics (PV) applications, for flexible CMOS applications, further thinning of the Si to sub-micron thicknesses may be desired for improved mechanical flexibility, and should be achievable with a chemical mechanical polish (CMP) after the exfoliation process, if needed.

Figure 5.2 shows the physical characteristics of the as-exfoliated foil. The microscope image of the surface of the Si shows ridges of approximately 0.2 μm in height and, as expected for a fracture surface, these ridges run perpendicular to the crack propagation direction. In order to further investigate if the mechanical exfoliation process introduces cracks or defects in the Si foil, TEM imaging was used to study the microstructure of the exfoliated Si. The TEM micrograph in Fig 5.2 (B) shows that the

perfect crystallinity of the Si wafer is preserved after exfoliation, as indicated by the lattice fringes in the image. No defects or microcracks were observed.

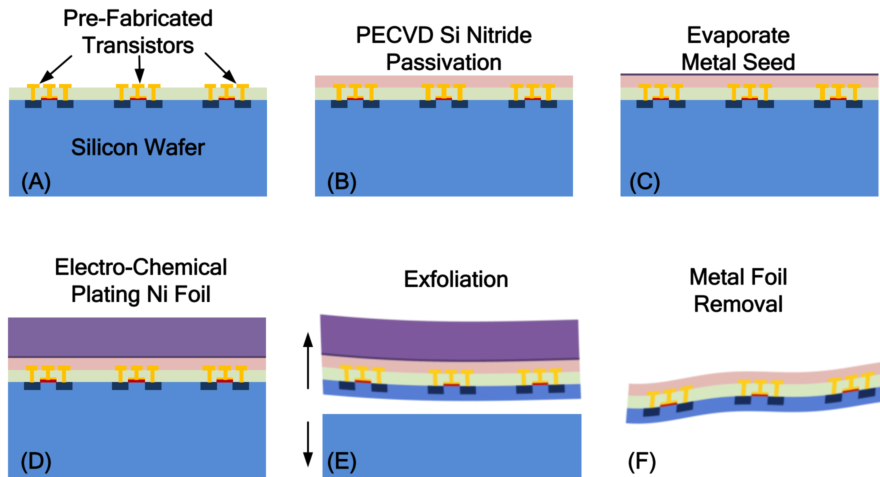


Figure 5. 1 Exfoliation process flow: (**A**) Transistors are pre-fabricated on conventional silicon wafer with standard CMOS process flow. (**B**) PECVD Si_3N_4 for passivation. (**C**) E-beam evaporation of thin metal seed layer. (**D**) Electro-chemical plating of Ni on seed layer. (**E**) Thermal expansion mismatch exfoliates the film from wafer. (**F**) Nickel foil is removed by SC-2 solution.

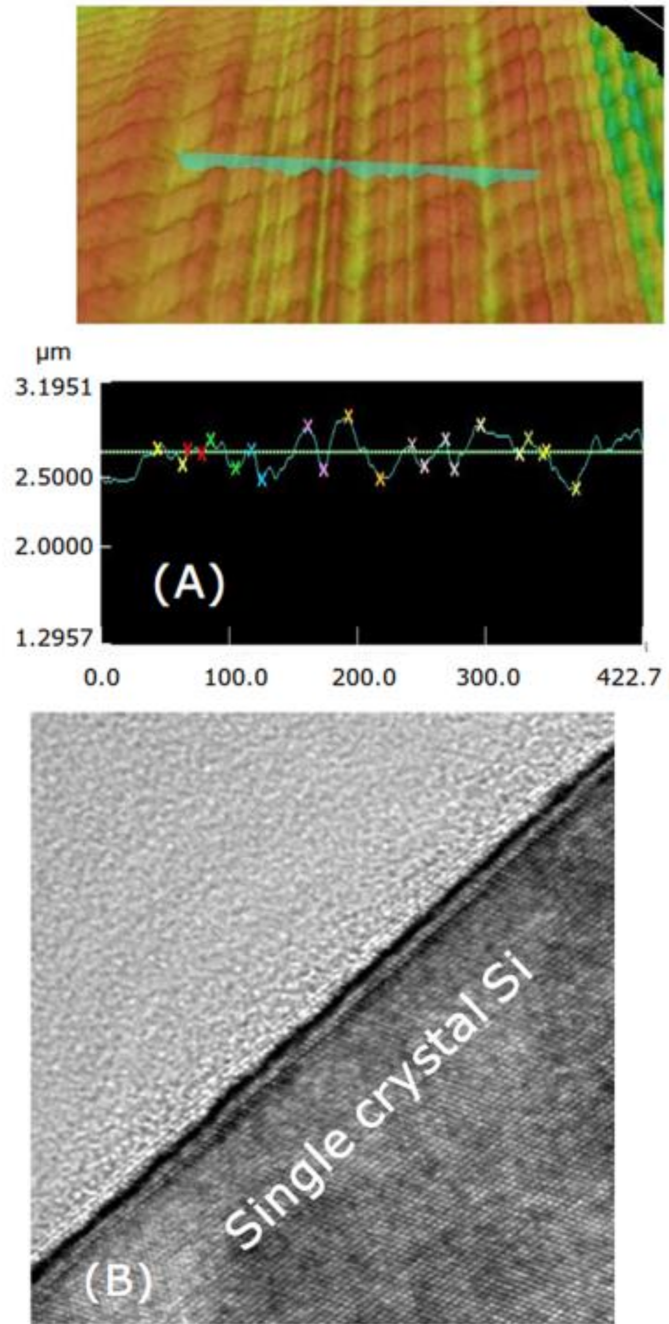


Figure 5. 2 (A) Surface roughness of exfoliated thin-film silicon (B) TEM image of microstructure of the exfoliated Si.

After exfoliation, a negative residual strain ε_0 remains in the nickel film. Accordingly, there exists a compressive stress component in the silicon layer and tensile stress component in the metal layer. The residual strain ε_0 which determines the mechanical strength and reliability of such a composite foil has been analyzed previously[68]. Assuming that the thicknesses of the silicon layer and the metal are h_1 and h_2, respectively, Young's modulus E_1 and Poisson's ratio v_1 for silicon, and E_2 and v_2 for nickel, respectively, based on the assumption of plain strain condition, the stress distribution in silicon layer is given as

$$\sigma_1(\bar{y}) = -\frac{E_1\varepsilon_0}{1-v_1^2}\frac{4mn+3mn^2+m^2n^4-6mn(1+n)\bar{y}}{1+4mn+6mn^2+4mn^3+m^2n^4} = -\frac{E_1\varepsilon_0}{1-v_1^2}f_{mn} \quad \text{for } 0<\bar{y}\le 1, \quad (1)$$

where, $m = E_2(1-v_1^2)/(E_1(1-v_2^2))$, $n = h_2/h_1$ and $\bar{y} = y/h_1$. Eq. (1) shows that the stress in the silicon layer is determined by the coefficient, *n*, for a certain value of ε_0. Figure 3 shows the variation of the coefficient f_{mn} with $\bar{y}$ as $m = 1.24$ and $n = 2$ for a typical exfoliated Si substrate. It can be seen that f_{mn} is positive for $0 < \bar{y} \le 1$ and, accordingly, the stress in the entire silicon layer is negative or compressive. It is known that silicon is a brittle material and is prone to breakage under tensile stress. This compressive stress from ε_0 can offset tensile stresses resulting from occasional external forces during handling of the silicon foils and tensile thermal stresses due to the mismatch of coefficients of thermal expansion of silicon and nickel at high temperature. Therefore, the existence of ε_0 makes the exfoliated substrate extra rugged and improves the yield of exfoliated substrate during handling and further processing.

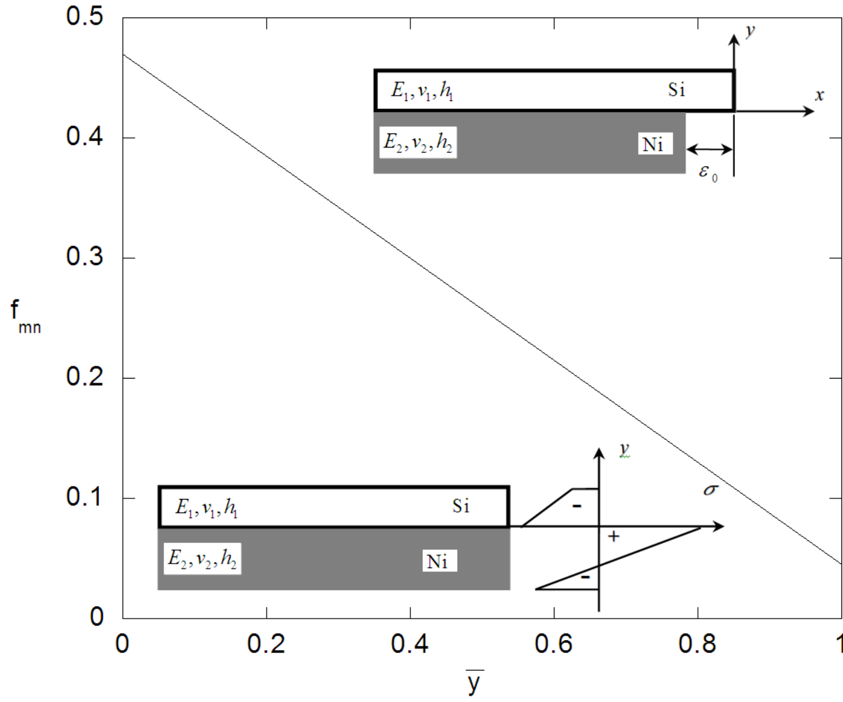


Figure 5. 3 The variation of stress coefficient f_{mn} for $0 < \bar{y} \leq 1$. The upper inset shows the residual strain ε_0 between Si and Ni layers and the co-ordinate system used to compute the stress distribution. The lower inset schematically shows the stress distributions in Si and Ni layers after the exfoliation.

After the exfoliation, the thin, bendable, single crystalline silicon foil with the metal backing is bonded onto a plastic substrate, which is attached to glass for easier handling and testing. The metal foil is slowly etched away in a mixture of 3:3:10 HCl:H_2O_2:H_2O (RCA SC-2 solution) in room temperature until the silicon nitride passivation is reached (~20min). Figure 5.3 shows the flexible silicon films with devices when detached from the glass substrate, with a size ca. 30mm x 50mm. The inset shows an 8 inch (200 mm) exfoliated wafer with metal foil. Our exfoliation process can exfoliate wafers at least up to 8 inch diameter.

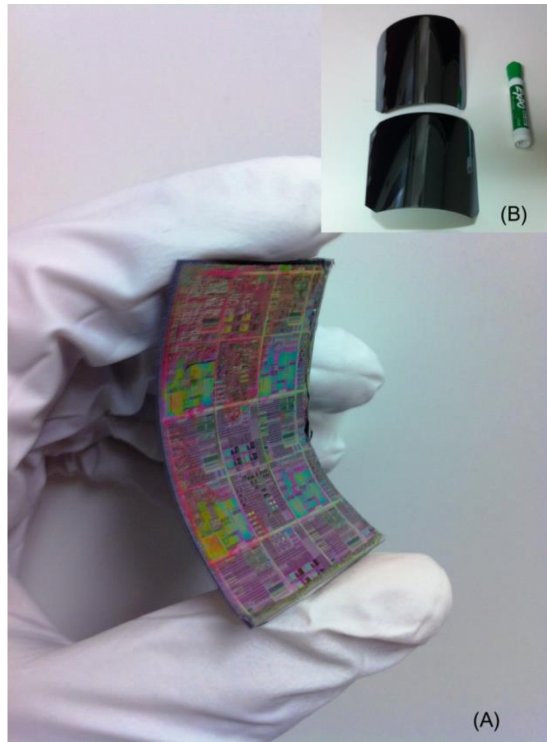


Figure 5. 4 Image of a bent, flexible integrated circuit with high performance CMOS devices. (A) is flexible IC with the size of 35 mm x 50 mm. (B) shows an 8-inch exfoliated wafer with metal foil.

5.3 PERFORMANCE OF EXFOLIATED THIN-FILM TRANSISTORS

Fabricated thin-film n-MOS and p-MOS FETs with different gate lengths were tested in terms of I_D-V_G transfer and I_D-V_D output electrical characteristics before and after exfoliation. Besides MOSFETs, gate dielectric breakdown and diode reverse leakage and breakdown characteristics were also compared before and after exfoliation.

Figure 5.4 presents a comparison of transfer characteristics of n-MOS and p-MOS devices with channel length of 150 nm, channel width of 10 μm, and 20Å SiO_2 gate oxide. Black curves show the transfer characteristics of the MOSFETs on bulk Si wafers, before exfoliation. The red curves show the measured I_D -V_G after exfoliation, showing

no significant degradation of transistor characteristics. The ON current of 150 nm n-MOSFETs after exfoliation is 0.413mA/micron at V_{GS} = 1.0 V and V_{DS} = 1.0 V, comparable with the value of 0.422mA/micron before exfoliation. The I_{ON}/I_{OFF} ratio is ~10^6, and the sub-threshold slope (SS) is 72mV/decade. Five different n-MOSFETs with the same parameters were measured and the ON currents ranged from 4mA to 4.13mA, so the difference with original device was within 5.3%. On p-MOSFETs, the ON current is 0.155mA/micron before exfoliation and 0.151mA/micron after exfoliation, respectively, with I_{ON}/I_{OFF} ratio = 10^6 and SS = 81mV/decade. Measured results on different devices with same parameters shows that the difference of pMOSFET ON current before and after exfoliation is less than 3%. The carrier mobilities were extracted from transfer curve of the MOSFETs with 1 μm channel length and 10 μm width. After exfoliation the electron mobility in n-MOSFETs is 252 cm^2/Vs, comparable with the value of 261 cm^2/Vs before exfoliation. Similar comparison of hole mobility in p-MOSFETs yielded values of 51 cm^2/Vs vs. 53 cm^2/Vs, before and after exfoliation, respectively. It was difficult to measure exactly the same device before and after exfoliation, because the probes scratched the metal pads during the first measurement (before exfoliation), and the scratched metal pads are more easily damaged during the exfoliation process.

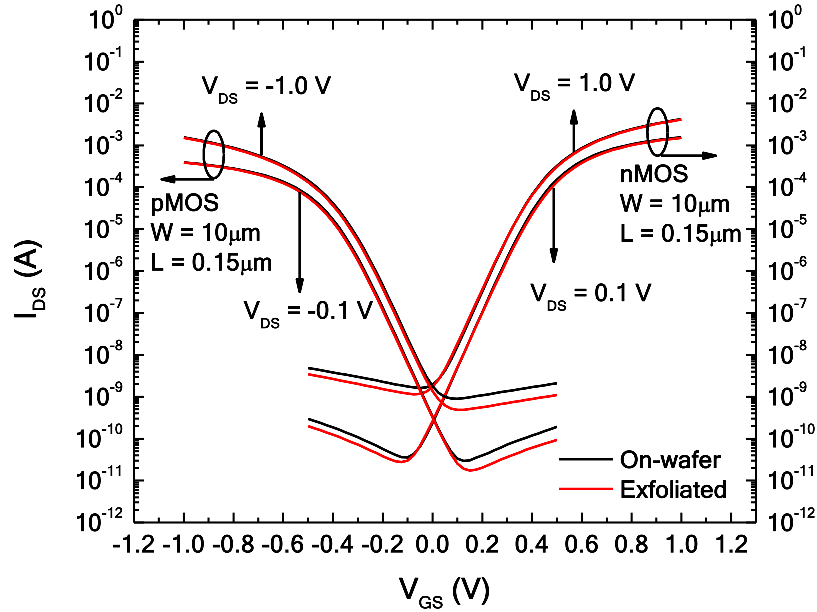


Figure 5. 5 Comparison of transfer characteristics before exfoliation (On-wafer, black curve) and after exfoliation (exfoliated, red curve) with V_{DS} = 0.1 V and 1.0 V. The channel length is 150 nm and width is 10 μm with gate oxide of 20Å SiO_2 for both n-MOSFETs and p-MOSFETs.

Figure 5.5 exhibits the output characteristics of both n-MOSFETs and p-MOSFETs before and after exfoliation. V_{DS} was varied from 0 V to 1.0 V, and V_{GS} from 0 to 1.0 V in steps of 0.1 V. Red and black curves denote the results before and after exfoliation, respectively. The curves match quite well, except that the result after exfoliation has slightly lower saturation current for each V_{GS}, probably because the residual silicon nitride passivation gives additional source/drain contact resistance.

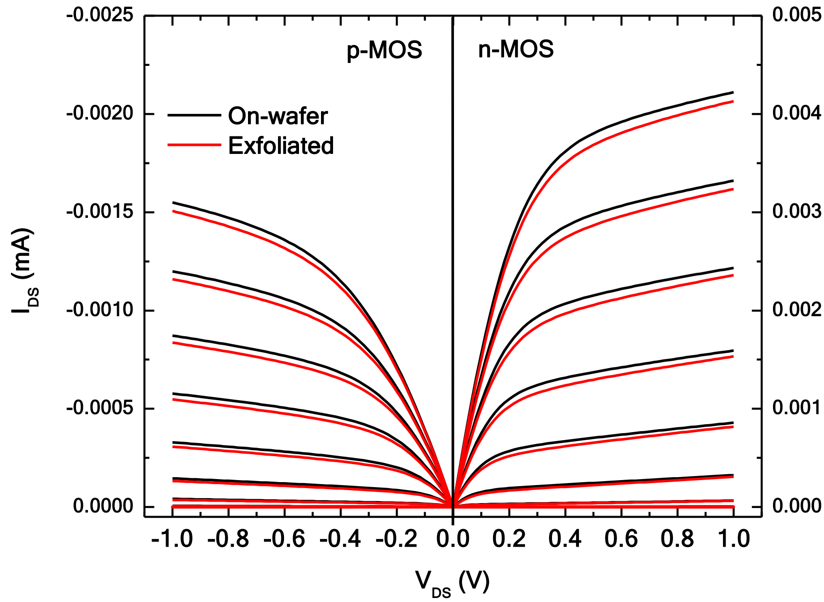


Figure 5. 6 Comparison of output characteristics before exfoliation (On-wafer, black curve) and after exfoliation (exfoliated, red curve) with V_{GS} from 0.1 V to 1.0 V, in steps of 0.1 V. The channel length is 150nm and width is 10 µm with gate oxide of 20Å SiO_2 for both n-MOS and p-MOS.

To study the effect on the gate dielectric during exfoliation process, we characterized the gate leakage currents and breakdown voltages before and after the exfoliation. In each case, we tested three devices and the results of six curves in two sets are plotted in figure 5.6. Black curves represent the gate leakage current versus gate bias voltage of un-exfoliated devices. Before exfoliation, we find that the leakage current through the gate dielectric begins to significantly increase when gate bias is larger than 2.5 V. Considering that the gate dielectric is 20Å SiO_2, the result shows an equivalent breakdown electric field of 12.5 MV/cm, which is consistent with the breakdown field of the material. In the post-exfoliation set, gate dielectric becomes leaky at 2.2 V in the

worst case, which is slightly lower than before exfoliation. Breakdown field is 11 MV/cm, still in a reasonable range for SiO_2.

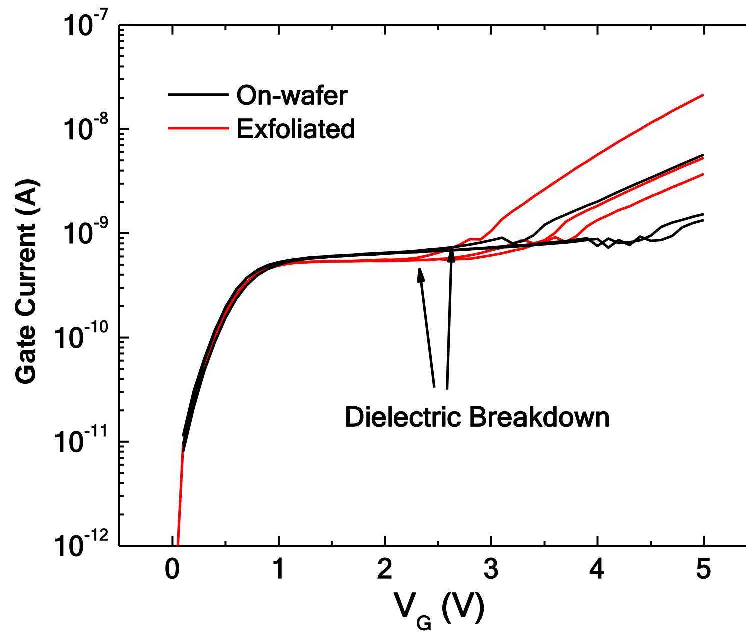


Figure 5. 7 Gate dielectric leakage current as a function of gate bias. Black curve shows the leakage current before exfoliation (on-wafer), and red curve after exfoliation.

We also investigated the diode characteristics on flexible c-Si substrate. Two sets of I-V curves were measured before (black) and after (red) exfoliation, respectively, with three different diodes in each set (Figure 5.7). In forward bias, current increases exponentially from 0.7V. Reverse leakage current is low until a reverse bias of 8V. Before exfoliation, the three diodes break down in the range of 7.8V-8.2V, while after exfoliated diodes break down at around 8V. This comparison indicates that the exfoliation process does not degrade the diode breakdown voltage significantly.

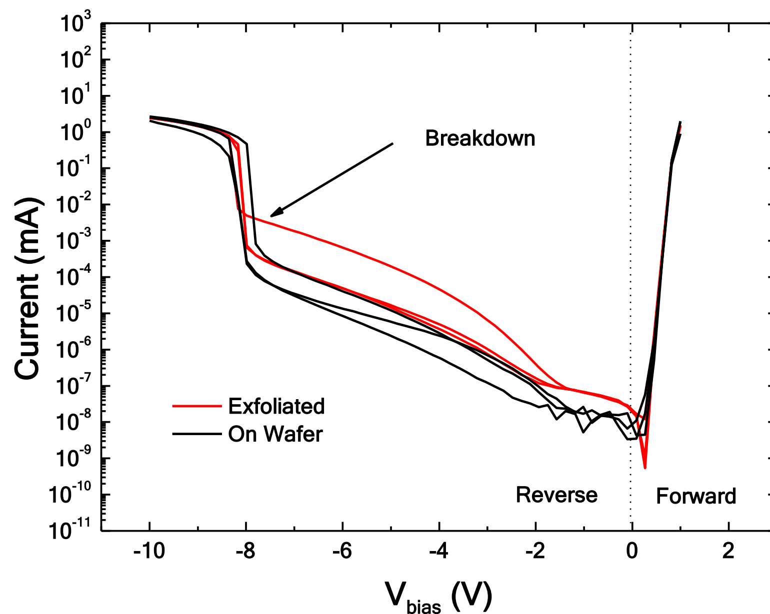


Figure 5. 8 Diode I-V characteristics with reverse breakdown voltage. Black curve shows the leakage current before exfoliation (on-wafer), and red curve after exfoliation.

In summary, we demonstrated a new approach to produce high performance flexible thin-film-transistors by exfoliating the top surface of wafers with pre-fabricated devices or circuits. This approach uses high quality single crystal silicon and avoids process temperature limitations. Different from the contact printing technique that transfers nanowires or ribbons, devices or circuit system are pre-fabricated on conventional wafers with industry standard semiconductor process flow. The exfoliation process is very simple and straight forward. Comparing the electronic device performance before and after exfoliation we find that the exfoliated TFTs have almost the same high performance as on the bulk wafer in terms of high drive current, I_{ON}/I_{OFF} ratio, steep sub-threshold slope and high channel mobility. The devices are completely

compatible with state-of-the-art industry level semiconductor technology and are ready for system integration. This technology has huge potential not only for flexible electronics, but also provides a fast and economical solution of thinning silicon for 3D-IC integration.

Chapter 6 Future work

6.1 Future work for nanowire FET

Due to the high aspect ratio of the vertical nanowire structure, gate dielectric is vulnerable to break down, especially at the foot of nanowire, where the profile is changing from horizontal to vertical. High temperature sacrificial oxidation can be adopted to smooth the curvature. The oxidation rate at the bottom of the pillar is low due to increased stress at high curvature [69-71]. As a result, smoothly controlled Si profile is formed after oxidation. The grown oxide can be stripped in dilute hydrofluoric acid.

6.2 Thinned wafer for 3D-IC

Besides the application in flexible electronics, this thin film exfoliation technology also provides a fast, simple and economical method for thinning Si, which is one of the most important enablers for next generation of three-dimensional (3D) integration. 3D silicon integration, using Through Silicon Vias (TSVs) that vertically stacks multiple integrated circuits (IC) on the floor plan is able to achieve much higher integration density[72]. Also, the interconnect length between different components will be significantly shortened by this 3D integration, and consequently the signal delays will be reduced. Moreover, this technology allows heterogeneous integration of various components onto a system-on package platform to achieve a complete functional unit in a tiny space.[73, 74]

For the last ten years, researchers have recognized that silicon thinning technology is one of the three important enablers for 3D silicon integration, along with fine-pitch interconnection by TSV and wafer-to-wafer bonding. Vertical Si-on-Si stacking requires very thin and uniform silicon wafers, usually below 50um and down to the active layer. Several thinning approaches have been reported, e.g. fast mechanical

grinding, slow but gentle chemical-mechanical polishing and wet chemical etching[75-78]. However, compared with silicon exfoliation which peels off only a small surface portion of the wafer and leaves the rest of the bulk silicon wafer reusable, these approaches waste most of the volume of silicon to get a thinned wafer. Although our approach leads to a somewhat high rms roughness of ~1-5 microns, it should be possible to use CMP to smoothen the surface to enable 3D integration.

Exfoliation pre-fabricated ID from conventional wafer provides an economical and fast option to fabricate thinned silicon wafer. As described in the previous chapter, traditional thinning technology including the fast mechanical grinding and dry/wet etching, has a required uniformity of < 1-2 μm. The thickness uniformity from the exfoliated wafer films remains unknown. Further polishing processes are probably necessary for exfoliated wafer to cater to 3D-IC's requirements. The roughness on the backside of exfoliated wafer is also an interesting topic for evaluation and improvement.

Appendix A: Process flow of vertical Si nanowire FET

Process	Tool	Recipe	Material / Chemical	Parameter
Ion Implantation			Phosphorus	100keV, DOSE = 1E13, tilt = 0°
Piranha + HF clean	Hood C16			
Anneal	MRL Anneal Furnace			1hr, 1000^oC
Ion Implantation			Boron	20keV, DOSE = 5E15, tilt = 7°
Piranha clean + HF	Hood C16			
Anneal	AET	1000^oC, 10sec		1000C, 10sec
Piranha clean + HF	C16			
E-beam lithography	Hood L10		ZEP 520A:ZEP A=2:3	500rpm 100ramp 5sec; 2000rpm 1000ramp 35sec
	Hotplate			180^oC 2min
	EBL			dose=126 $\mu c/cm^2$
	Develop		ZED N50	Develop 2min
Ti/Ni evaporation	CHA#1			Ti/Ni = 200Å/200Å
Lift off	Hood E5/hotplate		Remover PG	90^oC Overnight soak
Acetone rinse	Hood E5			Sonicate 2min
O_2 descum	March Asher			3min
Acetone rinse	Hood E5			Sonicate 2min
Salicide Anneal	AET	600^oC N_2 10sec		600^oC N_2 10sec
Deep Silicon Etch	DSE	coulee_shallow_etch		30 cycles
Piranha + HF clean	G12/14			
ALD Gate Dielectric	Fiji ALD	Yujia/thermal Al_2O_3		200 cycles
ALD Gate Metal	Fiji ALD	Yujia/TiN_NH3		150 cycles
PECVD SiO_2	PlasmaTherm#2	YJSIO02		1min
Pattern gate pad	Hood J23	4000RPM 30sec	HDMS	4000RPM 30sec
	Hotplate			95-115^oC 1min
	Hood J23	4000RPM 30sec	AZ5209	4000RPM 30sec
	Hotplate			90-95^oC 1min
	Photolitho	4.5 sec		Mask = Gate metal pad
	Develop		MIF726	1min
	Oven			120^oC 5min
Resist etch-back	PlasmaTherm#2	YJ_O2_2	O_2 plasma	2 min
SiO_2 etch	Hood G12		BOE	15 sec dip
Acetone rinse	Hood E5			Sonicate 2 min
TiN wet etch	Hood G12		SC-1	12 min

<table>
<tr><td>SIO₂ etch</td><td>Hood G12</td><td></td><td>BOE</td><td>15sec dip</td></tr>
<tr><td>PECVD SiO₂</td><td>PlasmaTherm#2</td><td>YJSIO02</td><td></td><td>5min</td></tr>
<tr><td>Resist spin-on</td><td>Hood J23</td><td>4000RPM 30sec</td><td>AZ5209</td><td>4000RPM 30sec</td></tr>
<tr><td>Resist hard bake</td><td>Oven</td><td></td><td></td><td>120°C 5min</td></tr>
<tr><td>Resist etch-back</td><td>PlasmaTherm#2</td><td>YJ_O2_2</td><td>O₂ plasma</td><td>130 sec</td></tr>
<tr><td>SiO₂ etch</td><td>PlasmaTherm#2</td><td>YJ_NIT1</td><td>CHF₃+O₂</td><td>5 min</td></tr>
<tr><td>Acetone rinse</td><td>Hood E5</td><td></td><td></td><td>Sonicate 2 min</td></tr>
<tr><td rowspan="9">Pattern drain pad</td><td>Hood J23</td><td>4000RPM 30sec</td><td>HDMS</td><td>4000RPM 30sec</td></tr>
<tr><td>Hotplate</td><td></td><td></td><td>95-115°C 1min</td></tr>
<tr><td>Hood J23</td><td>4000RPM 30sec</td><td>AZ5214</td><td>4000RPM 30sec</td></tr>
<tr><td>Hotplate</td><td></td><td></td><td>90-95°C 1min</td></tr>
<tr><td>Photolitho</td><td>3 sec</td><td></td><td>Mask=Drain metal pad</td></tr>
<tr><td>Hotplate</td><td>115°C 1min</td><td></td><td>1min</td></tr>
<tr><td>Flood expose</td><td></td><td></td><td>1min</td></tr>
<tr><td>Develop</td><td></td><td>MIF726</td><td>1min</td></tr>
<tr><td>Oven</td><td>120°C 5min</td><td></td><td></td></tr>
<tr><td>Ni evaporation</td><td>CHA#1</td><td></td><td></td><td>1500Å</td></tr>
<tr><td>Lift off</td><td>Hood E5</td><td></td><td>Acetone</td><td>Sonicate 2 min</td></tr>
<tr><td rowspan="9">Pattern gate contact window</td><td>Hood J23</td><td>4000RPM 30sec</td><td>HDMS</td><td>4000RPM 30sec</td></tr>
<tr><td>Hotplate</td><td></td><td></td><td>95-115°C 1min</td></tr>
<tr><td>Hood J23</td><td>4000RPM 30sec</td><td>AZ5209</td><td>4000RPM 30sec</td></tr>
<tr><td>Hotplate</td><td></td><td></td><td>90-95C 1min</td></tr>
<tr><td>Photolitho</td><td>3 sec</td><td></td><td>Mask = Gate via</td></tr>
<tr><td>Hotplate</td><td></td><td></td><td>115°C 1min</td></tr>
<tr><td>Flood expose</td><td></td><td></td><td>1min</td></tr>
<tr><td>Develop</td><td></td><td>MIF726</td><td>1min</td></tr>
<tr><td>Oven</td><td>120°C 5min</td><td></td><td></td></tr>
<tr><td>SiO₂ etch</td><td>Hood G12</td><td></td><td>BOE</td><td>3min</td></tr>
<tr><td>Acetone rinse</td><td>Hood E5</td><td></td><td></td><td>Sonicate 2 min</td></tr>
</table>

Appendix B: Process flow of vertically diffused finFET

Process	Tool	Recipe	Material / Chemical	Parameter
Ion Implantation			Phosphorus	100keV, DOSE = 1E13, tilt = 0°
Piranha + HF clean	Hood C16			
Anneal	MRL Anneal Furnace			1hr, 1000^oC
Ion Implantation			Boron	20keV, DOSE = 5E15, tilt = $^o0$
Piranha clean + HF	C16			
Anneal	AET	1000^oC, 10sec		1000C, 10sec, N_2
Piranha clean + HF	C16			
E-beam lithography	Hood L10		ZEP 520A:ZEP A=2:3	500rpm 100ramp 5sec; 2000rpm 1000ramp 35sec
	Hotplate			180^oC 2min
	EBL			dose=126 $\mu c/cm^2$
	Develop		ZED N50	Develop 2min
Ti/Ni evaporation	CHA#1			Ti/Ni = 200Å/200Å
Lift off	Hood E5/hotplate		Remover PG	90^oC
Acetone rinse	Hood E5			Sonicate 2min
O2 descum	March Asher			3min
Acetone rinse	Hood E5			Sonicate 2min
Salicide Anneal	AET	600C N2 10sec		600^oC N_2 10sec
Deep Silicon Etch	DSE	coulee_shallow_etch		30 cycles
Piranha + HF clean	G12/14			
ALD Gate Dielectric	Fiji ALD	Yujia/thermal Al2O3		200 cycles
ALD Gate Metal	Fiji ALD	Yujia/TiN_N2ONLY		200 cycles
PECVD SiO_2	PlasmaTherm#2	YJSIO02		1min
Pattern Gate Pad	Hood J23	4000RPM 30sec	HDMS	4000RPM 30sec
	Hotplate			95-115^oC 1min
	Hood J23	4000RPM 30sec	AZ5209	4000RPM 30sec
	Hotplate			90-95^oC 1min
	Photolitho	4.5 sec		Mask = Gate via
	Develop		MIF726	1min
	Oven	120^oC 5min		
SiO_2 etch	Hood G12		BOE	15sec dip
TiN wet etch	Hood G12		Piranha	10-15sec dip
SiO_2 etch	Hood G12		BOE	15sec dip
Pattern Source Pad	Hood J23	4000RPM 30sec	HDMS	4000RPM 30sec
	Hotplate			95-115^oC 1min

	Hood J23	4000RPM 30sec	AZ5209	4000RPM 30sec
	Hotplate			90-95°C 1min
	Photolitho	3 sec		Mask = MODFET Level 0
	Hotplate			115°C 1min
	Flood expose			1min
	Develop		MIF726	1min
	Oven	120°C 5min		
Al_2O_3 etch	Hood G12/14		BOE	2min
Ni evaporation	CHA#1			1000Å
Lift off	Hood E5		Acetone	

Bibliography

[1] A. I. Hochbaum, R. Fan, R. He, and P. Yang, "Controlled Growth of Si Nanowire Arrays for Device Integration," *Nano Letters,* vol. 5, pp. 457-460, 2005/03/01 2005.

[2] www.itrs.net. (2009). *International Technology Roadmap for Semiconductors*. Available: www.itrs.net

[3] H. Sunami, "Development of three-dimensional MOS structures from trench-capacitor DRAM cell to pillar-type transistor," *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on,* pp. 853-856, 20-23 Oct. 2008 2008.

[4] H. Sunami, "The Role of the Trench Capacitor in DRAM Innovation," *Solid-State Circuits Newsletter, IEEE,* vol. 13, pp. 42-44, 2008.

[5] W. Mueller, G. Aichmayr, W. Bergner, E. Erben, T. Hecht, C. Kapteyn, A. Kersch, S. Kudelka, F. Lau, J. Luetzen, A. Orth, J. Nuetzel, T. Schloesser, A. Scholz, U. Schroeder, A. Sieck, A. Spitzer, M. Strasser, P. F. Wang, S. Wege, and R. Weis, "Challenges for the DRAM cell scaling to 40nm," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International,* pp. 4 pp.-339, 5-5 Dec. 2005 2005.

[6] K. Koyama, T. Sakuma, S. Yamamichi, H. Watanabe, H. Aoki, S. Ohya, Y. Miyasaka, and T. Kikkawa, "A stacked capacitor with $(Ba_xSr_{1-x})TiO_3$ for 256M DRAM," *Electron Devices Meeting, 1991. IEDM '91. Technical Digest., International,* pp. 823-826, 8-11 Dec 1991 1991.

[7] M. Gutsche, H. Seidl, J. Luetzen, A. Birner, T. Hecht, S. Jakschik, M. Kerber, M. Leonhardt, P. Moll, T. Pompl, H. Reisinger, S. Rongen, A. Saenger, U. Schroeder, B. Sell, A. Wahl, and D. Schumann, "Capacitance enhancement techniques for sub-100 nm trench DRAMs," *Electron Devices Meeting, 2001. IEDM Technical Digest. International,* pp. 18.6.1-18.6.4, 2001 2001.

[8] S. Nakamura, M. Kosugi, A. Sato, A. Hatada, H. Minakata, M. Kobayashi, T. Kurahashi, R. Suzuki, and N. Sasaki, "A simple 4 G-bit DRAM technology utilizing high-aspect-ratio pillars for cell-capacitors and peripheral-vias simultaneously fabricated," *Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International,* pp. 29-32, 7-10 Dec 1997 1997.

[9] P. Mensch, K. E. Moselund, S. Karg, E. Lortscher, M. T. Bjork, H. Schmid, and H. Riel, "C-V measurements of single vertical nanowire capacitors," *Device Research Conference (DRC), 2011 69th Annual,* pp. 119-120, 20-22 June 2011 2011.

[10] J. E. Jang, S. N. Cha, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Nanoscale capacitors based on metal-insulator-carbon nanotube-metal structures," *Applied Physics Letters,* vol. 87, p. 263103, 2005.

[11] K. J. Kuhn, M. Y. Liu, and H. Kennel, "Technology options for 22nm and beyond," *Junction Technology (IWJT), 2010 International Workshop on,* pp. 1-6, 10-11 May 2010 2010.

[12] C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, W. Riess, B. J. Ohlsson, U. Gösele, and L. Samuelson, "Nanowire-based one-dimensional electronics," *Materials Today,* vol. 9, pp. 28-35, 2006.

[13] O. Sang-Hyun, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *Electron Device Letters, IEEE,* vol. 21, pp. 445-447, 2000.

[14] C.-W. Lee, S.-R.-N. Yun, C.-G. Yu, J.-T. Park, and J.-P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid-State Electronics,* vol. 51, pp. 505-510, 2007.

[15] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics,* vol. 48, pp. 897-905, 2004.

[16] H. Iwai, "Technology roadmap for 22nm and beyond," in *Electron Devices and Semiconductor Technology, 2009. IEDST '09. 2nd International Workshop on*, 2009, pp. 1-4.

[17] Y. Ran-Hong, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," *Electron Devices, IEEE Transactions on,* vol. 39, pp. 1704-1710, 1992.

[18] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "Impact of surrounding gate transistor (SGT) for ultra-high-density LSI's," *Electron Devices, IEEE Transactions on,* vol. 38, pp. 573-578, 1991.

[19] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, and F. Masuoka, "Multi-pillar surrounding gate transistor (M-SGT) for compact and

high-speed circuits," *Electron Devices, IEEE Transactions on,* vol. 38, pp. 579-583, 1991.

[20] S. Watanabe, K. Tsuchida, D. Takashima, Y. Oowaki, A. Nitayama, K. Hieda, H. Takato, K. Sunouchi, F. Horiguchi, K. Ohuchi, F. Masuoka, and H. Hara, "A novel circuit technology with surrounding gate transistors (SGT's) for ultra high density DRAM's," *Solid-State Circuits, IEEE Journal of,* vol. 30, pp. 960-971, 1995.

[21] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 40, pp. 2326-2329, 1993.

[22] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *Electron Device Letters, IEEE,* vol. 18, pp. 74-76, 1997.

[23] C. P. Auth and J. D. Plummer, "A simple model for threshold voltage of surrounding-gate MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 2381-2383, 1998.

[24] S. Biesemans, "FinFET for sub-22nm technology nodes."

[25] R. S. Wagner and W. C. Ellis, "VAPOR-LIQUID-SOLID MECHANISM OF SINGLE CRYSTAL GROWTH," *Applied Physics Letters,* vol. 4, pp. 89-90, 1964.

[26] P. Yang, Y. Wu, and R. Fan, "Inorganic Semiconductor Nanowires," *International Journal of Nanoscience,* vol. 1, p. 1, 2002.

[27] H. J. Fan, P. Werner, and M. Zacharias, "Semiconductor Nanowires: From Self-Organization to Patterned Growth," *Small,* vol. 2, pp. 700-717, 2006.

[28] B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, "Growth of vertically aligned Si wire arrays over large areas (>1 cm2) with Au and Cu catalysts," *Applied Physics Letters,* vol. 91, p. 103110, 2007.

[29] B. J. Smith, N. A. Stacey, J. P. Donnelly, D. M. Onsongo, T. C. Bailey, C. J. Mackay, D. J. Resnick, W. J. Dauksher, D. P. Mancini, K. J. Nordquist, S. V. Sreenivasan, S. K. Banerjee, J. G. Ekerdt, and G. C. Willson, "Employing Step-and-Flash imprint lithography for gate-level patterning of a MOSFET device," vol. 5037, pp. 1029-1034, 2003.

[30] A. Galluzzo, M. Melito, S. Musumeci, M. Saggio, and A. Raciti, "A new high voltage power MOSFET for power conversion applications," in *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE*, 2000, pp. 2966-2973 vol.5.

[31] I. Yoshida, "2-GHz Si power MOSFET technology," in *Electron Devices Meeting, 1997. IEDM '97. Technical Digest., International*, 1997, pp. 51-54.

[32] W. Qi, L. Minhua, J. Sharp, and A. Challa, "The Effects of Double-Epilayer Structure on Threshold Voltage of Ultralow Voltage Trench Power MOSFET Devices," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 833-839, 2007.

[33] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*: Wiley. com, 2006.

[34] S. Shan, J. S. Yuan, and Z. J. Shen, "Performance of Trench Power MOSFET With Strained Si/SiGe Multilayer Channel," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 1517-1522, 2011.

[35] J. M. Park, *Novel power devices for smart power applications*, 2004.

[36] J. T. Davies, P. Walker, and K. I. Nuttall, "Optimisation of VDMOS power transistors for minimum on-state resistance," *Solid-State and Electron Devices, IEE Proceedings I,* vol. 134, pp. 87-91, 1987.

[37] Z. Lisong, J. Soyoun, E. Brandon, and T. N. Jackson, "Flexible substrate micro-crystalline silicon and gated amorphous silicon strain sensors," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 380-385, 2006.

[38] Y. Sun and J. A. Rogers, "Inorganic Semiconductors for Flexible Electronics," *Advanced Materials,* vol. 19, pp. 1897-1916, 2007.

[39] A. J. Baca, J.-H. Ahn, Y. Sun, M. A. Meitl, E. Menard, H.-S. Kim, W. M. Choi, D.-H. Kim, Y. Huang, and J. A. Rogers, "Semiconductor Wires and Ribbons for High- Performance Flexible Electronics," *Angewandte Chemie International Edition,* vol. 47, pp. 5524-5542, 2008.

[40] A. R. Middya, S. Hazra, S. Ray, C. Longeaud, and J. P. Kleider, "New regime of RF PECVD for the growth of a-Si:H and its alloys with improved electronic properties," in *Photovoltaic Specialists Conference, 1997., Conference Record of the Twenty-Sixth IEEE*, 1997, pp. 655-658.

[41] J. M. Xu, "Plastic electronics and future trends in microelectronics," *Synthetic Metals,* vol. 115, pp. 1-3, 2000.

[42] A. Sazonov and C. McArthur, "Sub-100°C a-Si:H thin-film transistors on plastic substrates with silicon nitride gate dielectrics," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 22, pp. 2052-2055, 2004.

[43] D. D. Cheam, P. S. K. Karre, M. Palard, and P. L. Bergstrom, "Step and flash imprint lithography for quantum dots based room temperature single electron transistor fabrication," *Microelectronic Engineering,* vol. 86, pp. 646-649, 2009.

[44] S.-w. Chang, J. Oh, S. T. Boles, and C. V. Thompson, "Fabrication of silicon nanopillar-based nanocapacitor arrays," *Applied Physics Letters,* vol. 96, pp. 153108-153108-3, 2010.

[45] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Applied Physics Letters,* vol. 73, pp. 2447-2449, 1998.

[46] L. R. Mathew, Rajesh, "AND015 - Method of manufacturing a semiconductor device and a structure therof, pending patent."

[47] H. Yung-Jr, L. San-Liang, B. J. Thibeault, and L. A. Coldren, "Fabrication of Highly Ordered Silicon Nanowire Arrays With Controllable Sidewall Profiles for Achieving Low-Surface Reflection," *Selected Topics in Quantum Electronics, IEEE Journal of,* vol. 17, pp. 869-877, 2011.

[48] J. Y. Kim, S. Seo, D. Y. Kim, H. Jeon, and Y. Kim, "Remote plasma enhanced atomic layer deposition of TiN thin films using metalorganic precursor," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 22, pp. 8-12, 2004.

[49] Z. Wenjie, C. Jian, W. Dejun, W. Qian, and W. Shuidi, "Properties of TiN films deposited by atomic layer deposition for through silicon via applications," in *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on*, 2010, pp. 7-11.

[50] K.-E. Elers, J. Winkler, K. Weeks, and S. Marcus, "TiCl4 as a Precursor in the TiN Deposition by ALD and PEALD," *Journal of the Electrochemical society,* vol. 152, pp. G589-G593, 2005.

[51] Y. X. Liu, T. Kamei, K. Endo, S. O'Uchi, J. Tsukada, H. Yamauchi, T. Hayashida, Y. Ishikawa, T. Matsukawa, K. Sakamoto, A. Ogura, and M. Masahara, "Nanoscale TiN wet etching and its application for FinFET fabrication," in *Semiconductor Device Research Symposium, 2009. ISDRS '09. International*, 2009, pp. 1-2.

[52] M. Ritala and M. Leskela, "Atomic layer deposition," vol. 1, ed: Academic Press: San Diego, CA, 2001, p. 103.

[53] R. F. Service, "New Age Semiconductors Pick Up the Pace," *Science,* vol. 287, pp. 415-417, January 21 2000.

[54] A. Dodabalapur, "Organic and polymer transistors for electronics," *Materials Today,* vol. 9, pp. 24-30, 2006.

[55] T. Jung, A. Dodabalapur, R. Wenz, and S. Mohapatra, "Moisture induced surface polarization in a poly(4-vinyl phenol) dielectric in an organic thin-film transistor," *Applied Physics Letters,* vol. 87, pp. 182109-182109-3, 2005.

[56] I.-C. Cheng and S. Wagner, "Hole and electron field-effect mobilities in nanocrystalline silicon deposited at 150 ^{o}C," *Applied Physics Letters,* vol. 80, pp. 440-442, 2002.

[57] M. C. McAlpine, R. S. Friedman, and C. M. Lieber, "High-Performance Nanowire Electronics and Photonics and Nanoscale Patterning on Flexible Plastic Substrates," *Proceedings of the IEEE,* vol. 93, pp. 1357-1363, 2005.

[58] J. Hu, T. W. Odom, and C. M. Lieber, "Chemistry and Physics in One Dimension: Synthesis and Properties of Nanowires and Nanotubes," *Accounts of Chemical Research,* vol. 32, pp. 435-445, 1999/05/01 1999.

[59] Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, and A. Javey, "Wafer-Scale Assembly of Highly Ordered Semiconductor Nanowire Arrays by Contact Printing," *Nano Letters,* vol. 8, pp. 20-25, 2008/01/01 2008.

[60] H.-J. Chung, T.-i. Kim, H.-S. Kim, S. A. Wells, S. Jo, N. Ahmed, Y. H. Jung, S. M. Won, C. A. Bower, and J. A. Rogers, "Fabrication of Releasable Single-Crystal Silicon–Metal Oxide Field-Effect Devices and Their Deterministic Assembly on Foreign Substrates," *Advanced Functional Materials,* vol. 21, pp. 3029-3036, 2011.

[61] J. W. Hamer, R. S. Cok, G. J. Parrett, D. Winters, B. Primerano, C. A. Bower, E. Menard, and S. Bonafede, "63.2: AMOLED Displays Using Transfer-Printed Integrated Circuits," *SID Symposium Digest of Technical Papers,* vol. 40, pp. 947-950, 2009.

[62] S. Mack, M. A. Meitl, A. J. Baca, Z.-T. Zhu, and J. A. Rogers, "Mechanically flexible thin-film transistors that use ultrathin ribbons of silicon derived from bulk wafers," *Applied Physics Letters,* vol. 88, p. 213101, 2006.

[63] D.-H. Kim, J.-H. Ahn, W. M. Choi, H.-S. Kim, T.-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, "Stretchable and Foldable Silicon Integrated Circuits," *Science,* vol. 320, pp. 507-511, April 25, 2008 2008.

[64] C. A. Bower, E. Menard, S. Bonafede, and S. Burroughs, "Transfer-printed microscale integrated circuits," in *Electronic Components and Technology Conference,(59th ECTC)*, 2009, pp. 618-623.

[65] L. Mathew and D. Jawarani, "Method of forming an electronic device using a separation-enhancing species," US Patent 7749884, 2010.

[66] J. W. Hutchinson and Z. Suo, "Mixed Mode Cracking in Layered Materials," *Advances in Applied Mechanics,* vol. Volume 29, pp. 63-191, 1991.

[67] L. M. R.A. Rao, S. Saha, S. Smith, D. Sarkar, R. Garcia, R. Stout, A. Gurmu, D. Ahn, D. Xu, D. Jawarani, E. Onyegam, M. Hilali, S. Banerjee, J. Fossum, "A Novel Low Cost 25 µm Thin Exfoliated Monocrystalline Si Solar Cell Technology," in *26th European Photovoltaic Solar Energy Conference and Exhibition*, 2011, pp. 2439 - 2442.

[68] X. Dewei, P. S. Ho, R. A. Rao, L. Mathew, S. Smith, S. Saha, D. Sarkar, C. Vass, and D. Jawarani, "Mechanical strength and reliability of a novel thin monocrystalline silicon solar cell," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*, 2012, pp. 4A.3.1-4A.3.7.

[69] D. B. Kao, J. P. McVittie, W. D. Nix, and K. C. Saraswat, "Two-dimensional thermal oxidation of silicon. II. Modeling stress effects in wet oxides," *Electron Devices, IEEE Transactions on,* vol. 35, pp. 25-37, 1988.

[70] K. Dah-Bin, J. P. McVittie, W. D. Nix, and K. C. Saraswat, "Two-dimensional thermal oxidation of silicon—I. Experiments," *Electron Devices, IEEE Transactions on,* vol. 34, pp. 1008-1017, 1987.

[71] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET," *Electron Device Letters, IEEE,* vol. 29, pp. 791-794, 2008.

[72] P. Falkenstern, X. Yuan, C. Yao-Wen, and W. Yu, "Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis," in *Design Automation Conference (ASP-DAC), 2010 15th Asia and South Pacific*, 2010, pp. 169-174.

[73] T. Wang, K. Jeppson, L. Ye, and J. Liu, "Carbon-Nanotube Through-Silicon Via Interconnects for Three-Dimensional Integration," *Small,* vol. 7, pp. 2313-2317, 2011.

[74] K. W. Guarini, A. W. Topol, M. Ieong, R. Yu, L. Shi, M. R. Newport, D. J. Frank, D. V. Singh, G. M. Cohen, S. V. Nitta, D. C. Boyd, P. A. O'Neil, S. L. Tempest, H. B. Pogge, S. Purushothaman, and W. E. Haensch, "Electrical integrity of state-of-the-art 0.13 /spl mu/m SOI CMOS devices and circuits transferred for three-dimensional (3D) integrated circuit (IC) fabrication," in *Electron Devices Meeting, 2002. IEDM '02. International*, 2002, pp. 943-945.

[75] L. Wu, J. Chan, and C. S. Hsiao, "Cost-performance wafer thinning technology," in *Electronic Components and Technology Conference, 2003. Proceedings. 53rd*, 2003, pp. 1463-1467.

[76] K. Woonseong, L. Jaesik, V. Lee, J. Seetoh, Y. Yenchen, K. YeeMong, N. Ranganathan, T. Keng Hwa, and G. Shan, "Novel thinning/backside passivation for substrate coupling depression of 3D IC," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1395-1399.

[77] S. J. Koester, A. M. Young, R. R. Yu, S. Purushothaman, K. N. Chen, D. C. La Tulipe, N. Rana, L. Shi, M. R. Wordeman, and E. J. Sprogis, "Wafer-level 3D integration technology," *IBM Journal of Research and Development,* vol. 52, pp. 583-597, 2008.

[78] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel, R. J. Polastre, K. Sakuma, R. Sirdeshmukh, E. J. Sprogis, S. M. Sri-Jayantha, A. M. Stephens, A. W. Topol, C. K. Tsang, B. C. Webb, and S. L. Wright, "Three-dimensional silicon integration," *IBM Journal of Research and Development,* vol. 52, pp. 553-569, 2008.

Vita

Yujia Zhai, son of Gangyi Zhai and Yuzhi Li, was born in Xi'an, China. He graduated from No.1 Railway Middle School in Xi'an, China in 2003 and attended Peking University in Beijing, China from 2003 to 2007. He received his Bachelor of Science degree in Microelectronics in July 2007. In the fall of 2007, Yujia began graduate studies in the Department of Electrical and Computer Engineering at The University of Texas at Austin under the supervision of Professors Sanjay Banerjee and Grant Willson.

E-mail address: yujia.zhai@me.com

This dissertation was typed by Yujia Zhai