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Graphene Field Effect Transistors for High Performance Flexible Nanoelectronics

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Graphene Field Effect Transistors for High Performance Flexible Nanoelectronics

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Dedication

This dissertation is dedicated to my parents for providing endless love and support, and to my wife and daughter.

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Graphene Field Effect Transistors for High Performance Flexible Nanoelectronics

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The University of Texas at Austin, 2014

Supervisor: Deji Akinwande

Abstract: Despite the widespread interest in graphene electronics over the last decade, high-performance graphene field-effect transistors (GFETs) on flexible substrates have been rarely achieved, even though this atomic sheet is widely understood to have greater prospects for flexible electronic systems. In this work, we investigate the realization of high-performance graphene field effect transistors implemented on flexible plastic substrates. The optimum device structure for high-mobility and high-bendability is suggested with experimental comparison among diverse structures including top-gate GFETs (TG-GFETs), single/multi-finger embedded-gate GFETs with high-k dielectrics (EG-highk/GFETs), and embedded-gate GFETs with hexagonal boron nitride (h-BN) dielectrics. Flexible graphene transistors with high-k dielectric afforded intrinsic gain, maximum carrier mobility of 8,000 $cm^2/V \cdot s$, and importantly 32 GHz cut-off frequency. Mechanical studies reveal robust transistor performance under repeated bending down to 0.7 mm bending radius whose tensile strain corresponds to 8.6%. Passivation techniques, with robust mechanical and chemical protection in order to operate under harsh environments, for embedded-gate structures are also covered. The integration of

functional coatings such as highly hydrophobic fluoropolymers combined with the self-passivation properties of the polyimide substrate provides water-resistant protection without compromising flexibility, which is an important advancement for the realization of future robust flexible systems based on graphene.

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Chapter 1: Introduction

Graphene Field-Effect Transistor

The outstanding charge transport in graphene field effect transistors offers attractive prospects for high-speed analog and radio-frequency (RF) electronics. These outstanding features including high mobilities at room temperature,[1,2] sub-THz cutoff frequencies at moderate channel lengths,[3] and ambipolar electron-hole symmetry, afford linear and non-linear analog signal processing with the simplicity of a single transistor.[4,5] In addition, graphene is substrate agnostic and mechanically flexible. Hence, it is an ideal material for flexible electronics on polymeric substrates.

Although intrinsic carrier mobility of graphene approaching 100,000cm^2/V-s has been reported at room temperature on suspended devices,[6] the carrier mobility of graphene degrades on oxide supported graphene field-effect transistors (GFETs) with values around 10,000cm^2/V-s frequently measured on clean exfoliated graphene on SiO_2 in agreement with theoretical upper limits.[7–9] However, it is unclear how fast charge carriers can travel in monolayer graphene on polymeric substrates, which is an important substrate for flexible electronics. It has been suggested that remote phonon scattering from the broad continuum of modes from the polymer substrate should impact the carrier mobilities at a scale comparable to SiO_2.[10] As graphene holds great potential for fast flexible electronics, it is crucial to experimentally access its fast carrier transport on polymer supports.

Flexible Electronics

The field of flexible electronics has been active for more than a couple of decades, driven by the desire for the realization of low-cost, large-area electronics. The development of flexible electronics operating at radio-frequencies (RF) requires materials that combine excellent electronic performances and the ability to withstand high levels of strain. Circuit components required to implement flexible devices include (1) a supporting flexible film as a substrate, (2) electrically conducting films as electrodes, (3) dielectric films to be used as gate dielectrics and device isolation/passivation layers, and (4) active channel materials. The technical bottleneck in this field of research has been the preparation of high performance active channels due to the process compatibility to flexible substrates. Due to limited carrier mobilities of less than 100cm^2/V-s for diverse semiconducting materials reported as flexible channels, the resulting electronic device performance has been relatively poor.[11–13] The desire to improve the performance of these devices has led to the introduction of other materials which include carbon nanotubes,[14,15] silicon thin-films and nanowires,[16–18] and compound semiconductors.[19] III-V compound semiconductors and graphene show the highest mobility up to 10,000 cm^2/V-s on plastics while others show still relatively low values. However, enhancements in electronic performance have been achieved at the expense of device flexibility. In addition to the high carrier mobility and GHz cutoff-frequency, graphene is able to survive the mechanical tensile strain above 20%,[20] and offers a technical method for wafer-scalability.[21–23]

Thesis Outline

This thesis is organized as follows. In chapter 2, the preparation of electronic-grade flexible substrate will be reviewed. We will take a look at candidates for flexible substrates, their material properties, and requirements to be used as supporting films for electronic applications. In chapter 3, transistor device topologies we have investigated are explained and compared with each other. Several approaches in order to optimize the performance of the fabricated devices are covered in chapter 4. The origin of the contact resistance at the graphene-metal interface will be revisited to suggest the modified contact designs for better (lower) contact resistance values. A modified layout/process for low gate resistances and passivation techniques are also covered. In chapter 5, key device data on DC/RF electrical measurements and measurements under harsh environments (mechanical deformation and exposure to common liquids) will be presented. In chapter 6, a summary of this work is presented.

Chapter 2: Preparation of Electronic-Grade Flexible Substrates

Requirements for Flexible Substrates

Substrates to be used as a flexible supporting layer replacing the conventional rigid substrates should meet several requirements. Those requirements are listed as follows.

1. Surface quality/roughness

   Highly uneven surface topography limiting the fine resolution of lithographic steps has to be avoided. Nanometer-scale short/long range roughness values are desirable to prepare sub-micron channel length devices. Roughness over long distance (or more generally thickness variation) larger than the unit device structure is still acceptable. Chemical-Mechanical-Planarization (CMP) or other surface treatment processes are usually required for commercial flexible substrates to achieve acceptable roughness values.

2. Thermal properties

   The maximum processing temperature for the flexible substrates should not exceed their glass transition temperatures (Tg). During the exposure to high temperature processes even with highest temperature less than Tg, the mismatch in thermal expansion coefficients of integrated films and its resulting built-in stress of the sample have to be minimized. Metallic foils and glass substrates are superior in this aspect than polymer substrates.

3. Mechanical properties

   Materials with high elastic modulus are less flexible and easier to handle during the fabrication. Highly elastic polymers and elastomers may require

hard carrier wafers, where flexible substrates are attached, during the device fabrication.

4. Chemical properties/compatibilities

   Substrates should not react with chemicals (acids and solvents) used during device fabrication. Different coating layers may be required to protect the underlying base substrates.

5. Electrical conductivity

   Metallic foils are electrically conductive and require additional electrical isolation. Glass substrates and most polymers are good insulators.

6. (Optional) Optical clarity

   Not always required, but becoming an important metric for transparent electronics or optoelectronic applications.

Commercially Available Flexible Substrates

1. Glass substrate

Even though glass plates are considered to be hard and rigid, they become flexible when their film thickness are thinned down to less than 100 μm.[24,25] Glass substrates have high optical transparency and thermal stabilities (low thermal expansion coefficient and high glass transition temperature) suggesting good opportunities for wide-range of electronic applications including flat-panel displays. Mechanical and chemical properties are also attractive. However, they are brittle and cannot tolerate high level of strain, which can be introduced while handling them for fabrication.

2. Metallic foil

Stainless steel is one of the popular metallic foils currently being considered as a flexible substrate. They also become flexible similar to glass substrates when their film thicknesses are thinned down to 100 μm-scale, though their surface qualities are lower than that of glass substrates.[26,27] Metal foils are not transparent and electrically conductive, however can be still attractive for such applications where reflective surfaces are required. Surface planarization layers are also applied to offer electrical isolation and/or further improve the surface quality.[28,29] Inorganic materials such as plasma-enhanced chemical vapor deposited (PECVD) silicon nitride and oxide are also used to give the electrical isolation.

3. Polymer substrate

Polymers offer great opportunities to be used as flexible substrates. Diverse candidates are commercially available and a part of them are listed in Table 2.1. These are highly flexible and inexpensive. However, thermal properties are a major concern while utilizing these materials for electronics. Low thermal conductivities along with low glass transition temperatures of polymers limit several processing,[11,30] and operating conditions.[31,32]

Dimensional stabilities are also not as great as other candidate substrates listed above. Though high flexibility and low elastic modulus are among desirable features here, when these candidates are exposed to thermal processes repeatedly during device fabrication, the resulting built-in thermal stresses induce non-negligible film curvatures due to mismatch in their thermal expansion coefficients.

Material properties of commonly used flexible substrates are listed in Table 2.1.[33–37]

Table 2.1 *Material properties of commercial flexible substrates*

Property	Unit	Flexible substrates				
		Glass	Stainless steel	Polymer		
				PEN	PET	PI
Transparency		Good	N/A	Good	Good	Poor (Orange)
Max. process temperature	°C	600	900	155	120	300
CTE	ppm/°C	3~4	18	20	20~80	15~35
Elastic modulus	GPa	70	200	5	2~4	2~3
Electrical conductivity		Low	High	Low	Low	Low
Thermal conductivity	W/m°C	1	16	0.15	0.15~0.4	0.1~0.35

Surface Preparation of Polymer Substrates for Device Fabrication

Flexible industrial polyimide sheet (50-100μm thick) was chosen as the substrate because of its high glass transition temperature (>300ºC), Young's modulus (~3.5GPa), and high solvent resistance making it compatible with conventional device fabrication. The polyimide sheets used in this study are commercially available from American Durafilm Inc. (#300 FPC) and Dupont Inc. (Kapton film). Industrial polyimide (PI) has an uneven topography with surface roughness that can exceed 100nm.[38] To make the uneven surface of the industrial PI films smooth, liquid polyimide (PI 2574 from HD Microsystems) was spin-coated onto the polyimide sheet. The coated substrate was soft-baked at 200ºC for 30 min and subsequently cured at 300ºC for 1 hour under a nitrogen atmosphere to obtain a smooth surface (RMS ~1-2nm),[38] necessary for preserving the quality of electronic materials and for achieving the best results in lithographic resolution and registration. This coated polyimide sheet was then carefully mounted onto a supporting Si carrier wafer to ensure the flatness for the following fabrication process. Prior to use, the polyimide sheet was rinsed again in Acetone and 2-propanol (IPA) for 5 min each. The surface roughness of the polyimide surface before and after coating was measured using a VeecoVR D-5000 atomic force microscope (AFM) in tapping mode. Figure 2.1 shows the AFM images of polyimide surfaces scanned over the as-received commercial PI film and the PI film after the surface treatment.

To further improve the surface roughness, additional step of depositing high-k atomic layer deposition (ALD) dielectrics is done to improve the surface. This ALD dielectric layer can work as i) the high quality gate dielectric for embedded-gate device structures, and ii) the heat spread layer, which is an important component for the thermal management on flexible substrates, which will be discussed in a later chapter.

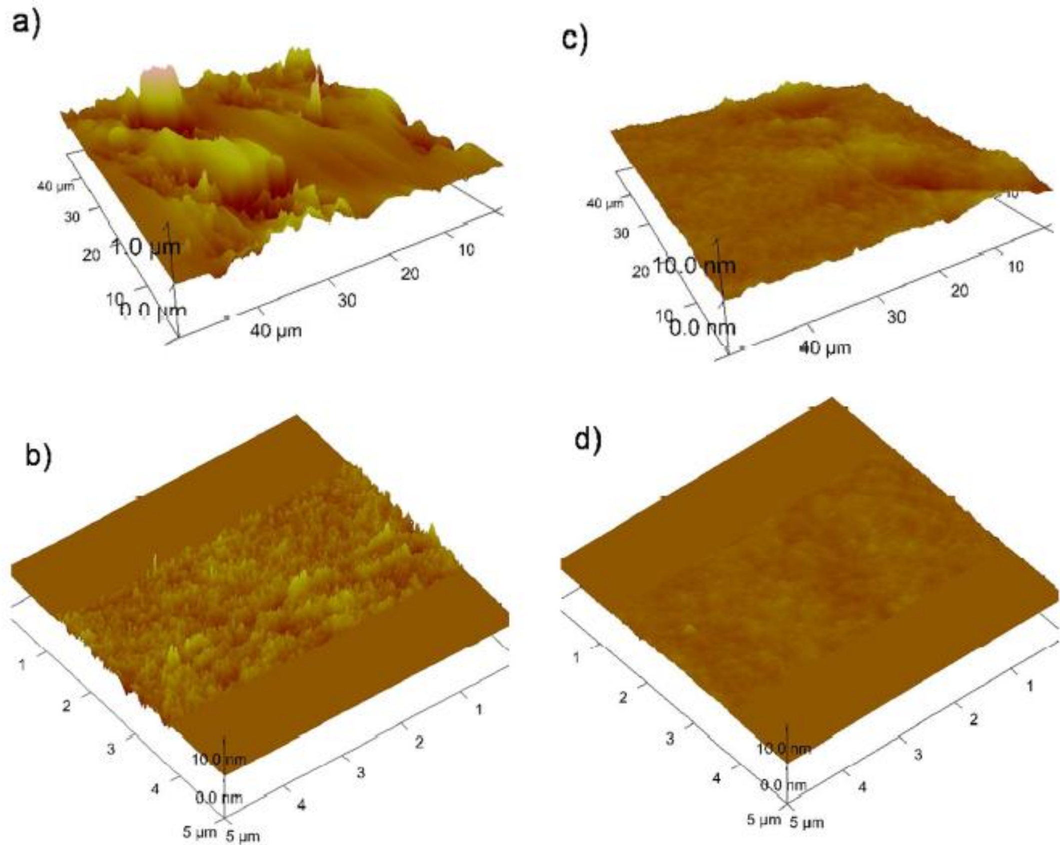

Figure 2.1. AFM images of polyimide surfaces. (a) 50x50 μm^2, (b) 5x2.5 μm^2 scan on polyimide sheet as received and (c) 50x50 μm^2, (d) 5x2.5 μm^2 scan after surface treatment.

Despite the attractive features of graphene, diverse charge scattering mechanisms prevent access to the intrinsic electrical performance. These challenges include ionized impurity scattering which degrades the mean-free-path,[39,40] substrate and interface charge traps resulting in charge puddles, and random shifting of the charge-neutrality point.[8,41] Each of the mechanical and chemical non-idealities can result in deviation of the band structure and transport characteristics, emphasizing the need for a high purity, ultra-

smooth dielectric that is compatible with graphene devices. Hexagonal boron nitride (h-BN) is an insulating isomorph of graphene with boron and nitrogen arranged in a hexagonal lattice, with a small lattice mismatch of ~1.8% compared to graphene.[42] Several features of h-BN make it an excellent candidate dielectric for GFETs on flexible substrates. The ultra-flat surface of h-BN significantly reduces the electron–hole charge fluctuations, compared to polymeric interfaces or SiO_2. This enables the observation of near-ideal graphene properties without the use of complex suspended structures.[42] Owing to its strong in-plane covalent bonds and relatively weak inter-plane bonds due van der Waals interactions, h-BN is cleaved and exfoliated in the same way as graphene.[42,43] Recently a series of reports have suggested that graphene/h-BN heterostructures enhance field-effect performance.[42–44]

Here, we report the method of utilizing an h-BN film as a gate dielectric for flexible FETs. The preparation of the substrate is as follows. h-BN (from Momentive Performance Materials) was exfoliated on silicon wafers with 285-nm thick thermal oxide, which offers good optical contrast between thin h-BN films and substrates for easy identification. The sample was first annealed under nitrogen at 300°C for 1 hour to achieve a smooth h-BN surface and remove residual adhesive on its surface to define a better interface between gate electrodes and h-BN films. Gate electrodes can be also patterned over annealed h-BN films on SiO_2/Si substrates by electron-beam lithography (EBL), e-beam evaporation, and liftoff to prepare the embedded-gate structures. Liquid-type PI (PI-2574 from HD Microsystems) was spin-coated on the patterned sample and cured under nitrogen to capture the device structures within PI. Thermal oxide was then etched by buffered-oxide-etchant (BOE) and the PI films with embedded gates and dielectrics were released (capture-release process). The released sample was then

annealed again under nitrogen to provide a clean high-quality interface between graphene and dielectrics (two-step annealing process). Figure 2.2 shows the comparison between different substrate preparation techniques.

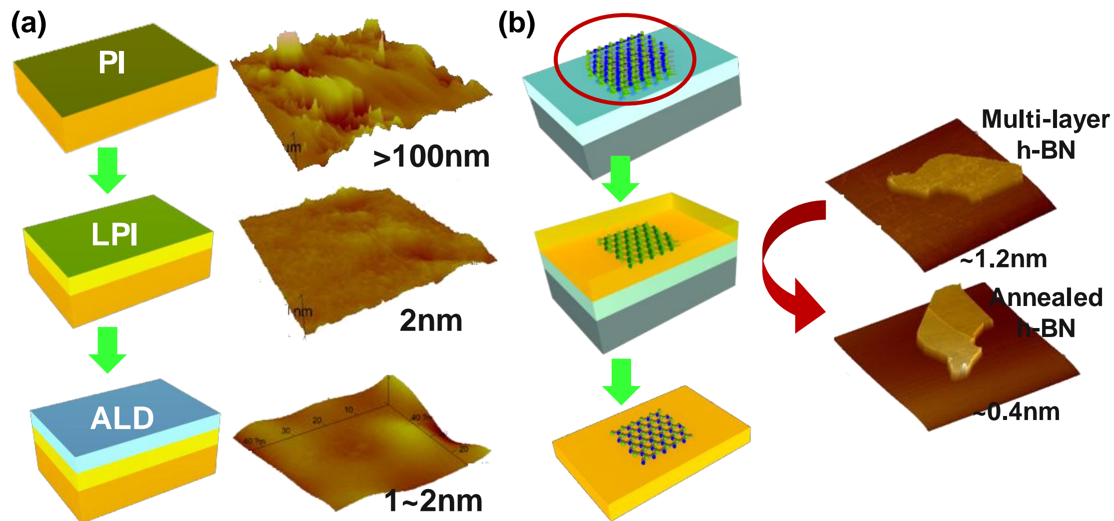

Figure 2.2. 3-D illustrations of different flexible substrates preparation techniques. (a) The surface treatments on flexible PI films. An as-received PI film, a cured liquid PI coated on a PI film, and an ALD deposited on a cured film are shown with their AFM images and roughness values. (b) Preparation of an embedded h-BN film captured in a free-standing PI substrate. The simplified process flow is given with the AFM images scanned over an as-exfoliated h-BN film (roughness ~1.2nm) and an annealed h-BN film (roughness ~0.4nm).

Chapter 3: Transistor Device Topology

Top-Gate Graphene Field-Effect Transistors

The graphene monolayer employed in this study was prepared via low-pressure chemical vapor deposition (CVD) on copper foil as reported previously.[45] A typical Raman spectrum of graphene synthesized with the CVD procedure on copper foil is shown in Figure 3.1a. The full width at half maximum of the 2D peak is approximately 35cm^{-1}, the 2D/G ratio is ~3, and the D-peak is negligible, indicating high-quality monolayer graphene. The typical solution-based poly(methyl methacrylate) (PMMA) assisted graphene transfer from the copper foil,[46] was employed to integrate the graphene onto the PI sheet. The AFM image in Figure 3.1b shows the substrate surface after graphene transfer on polyimide sheet with roughness of about 2nm in small areas but with wrinkles as high as 8nm due to the transfer process. These wrinkles from the polymer residue are detrimental to transport and mobility.[47]

An array of graphene transistors were fabricated directly on to the polyimide sheet using standard microelectronic processes and electron-beam lithography with a charge compensation layer essential for patterning insulating substrates. The simplified fabrication process is illustrated in Figure 3.2a. In brief, the first e-beam lithography patterns the active area while isolating graphene channels from each other. Oxygen plasma is used to etch the superfluous graphene. After defining source and drain electrodes by lithography and evaporation, high-k gate dielectric is deposited by ALD. The gate dielectric is composed of evaporated 1nm titanium that oxidizes readily in air at 200ºC and serves as the seed layer for uniform ALD of 30nm Al_2O_3,[7] with estimated capacitance of ~200nF/cm^2 (k~6.8). The gate electrode is subsequently patterned. The gate and source/drain metals are Ni (50nm) and Ni/Au (10nm/40nm) respectively. An

optical image of a completed device with ground-signal-ground (GSG) input (GFET gate) and output (GFET drain) pads necessary for RF measurements is shown in Figure 3.2b. Figure 3.2c is a photograph of the flexible polyimide substrate with an array of integrated GFETs.

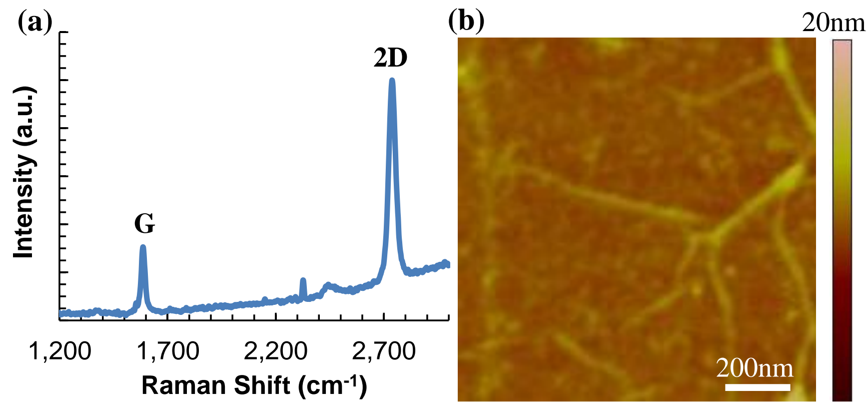

Figure 3.1. Monolayer graphene on copper foil (a) Raman spectrum of the synthesized monolayer graphene on copper foil indicating the 2D and G peaks. (b) AFM image of graphene transferred to flexible polyimide sheet with a surface roughness ~2nm and wrinkles as high as 8nm.

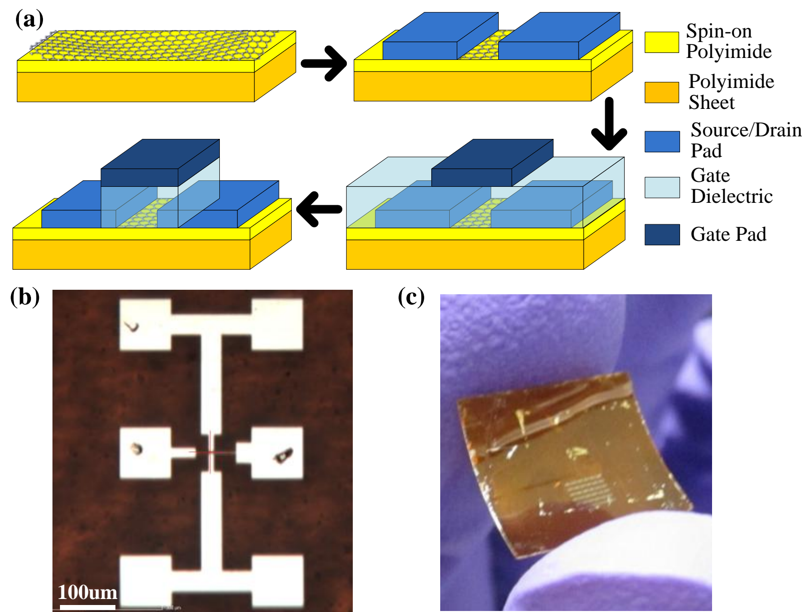

Figure 3.2. Top-gate graphene transistor on polyimide sheet (a) Simplified cross-sectional fabrication process for graphene transistor on polyimide sheet featuring transferred CVD graphene, high-k $Al_2 0_3$ dielectric, and metal electrodes. (b) Optical image of a completed GFET with two gate fingers in a GSG configuration to facilitate high-frequency measurements. The device length and total width are 0.25µm and 10µm respectively. (c) Photograph of the flexible substrate with an array of integrated GFETs.

Embedded-Gate Graphene Field-Effect Transistors

Two types of embedded-gate graphene field-effect transistors (EGFETs) have been realized in this work. The first one is a detachable EGFET. The fabrication process for the detachable EGFET is illustrated in Figure 3.3a.[48] Liquid polyimide (PI-2574 from HD Microsystems) was spin-coated on a 50-nm thick plasma-enhanced chemical vapor deposited Si_3N_4 sacrificial layer on silicon. The 15μm-thick spin-coated polyimide (PI) affords a smooth surface with root-mean-square (RMS) roughness of <1nm. The PI coated film is soft-baked at 200ºC for 30 min and subsequently cured at 300ºC for 1 hr under a nitrogen atmosphere. An array of gate electrodes were patterned on a PI-coated silicon substrate by electron-beam lithography, evaporation, and liftoff. A high-k dielectric of 20-nm thick Al_2O_3 is deposited by ALD. A CVD grown graphene film from a $Cu/SiO_2/Si$ growth substrate was then transferred via a conventional wet-transfer process using ammonia persulfate to etch the copper.[46] Oxygen plasma reactive-ion-etching (RIE) was used to pattern the active channel region while removing the superfluous graphene and ensuring channel isolation. Source and drain electrodes were defined to complete the device fabrication. The gate and source/drain metals are Ni/Au (10nm/40nm) and Ni (50nm) respectively. Lastly, buffered oxide etchant (BOE 6:1) was used to strip the Si_3N_4 sacrificial layer and release the flexible polyimide film from the underlying silicon substrate.

The second type of EGFET is using a cured PI film as the supporting flexible substrate. The 3D image of the fabricated 10-finger multi-finger EGFET unit-cell is illustrated in Figure 3.4a. In brief, an array of gate electrodes were patterned directly on PI by electron-beam lithography (EBL), evaporation, and lift-off. A high-k dielectric of 15-nm thick Al_2O_3 was deposited by ALD with estimated gate-oxide capacitance of

405nF/cm^2. Another EBL followed by wet-etching of Al_2O_3 by a 1:3 diluted solution of H_3PO_4:DI water isolated each device while leaving local dielectric islands for the channel. High quality CVD monolayer graphene film was then transferred via the conventional poly(methyl methacrylate) (PMMA) wet-transfer process using ammonia persulfate to etch the supporting copper foil.[45,46] The active channel area of graphene was then patterned, and source and drain electrodes were defined to complete the device structure. The top of the sample was then covered with a 30-nm thick plasma-enhanced chemical vapor deposited (PECVD) Si_3N_4 layer to protect the multi-finger EGFETs from the outside environment. The channel length and width for each finger were fixed at 0.5μm and 20μm, respectively. Devices with both 10-finger and 18-finger configurations were prepared resulting in effective channel widths of 200μm and 360μm, respectively, on the same PI substrate. The optical image given in Figure 3.4b shows the freestanding PI with an array of flexible MEGFETs bent with fingers. The inset shows a 3×3 array of the unit cells. Figure 3.4c is a high-resolution image of the active channel area obtained with an atomic force microscope (AFM) revealing a 10-finger electrode configuration.

Modified Embedded-Gate Graphene Field-Effect Transistors

The fabrication process for the modified EGFET is as follows. h-BN (from Momentive Performance Materials) was exfoliated on silicon wafers with 285-nm thick thermal oxide; the thickness of the h-BN flake was confirmed with AFM to be 19nm. The sample was first annealed under nitrogen at 300°C for 1 hour to achieve a smooth h-BN surface and remove residual adhesive on its surface to define a better interface between gate electrodes and h-BN films. The simplified process flow is given in Figure 3.5a. In brief, gate electrodes were patterned over annealed h-BN films on SiO_2/Si substrates by

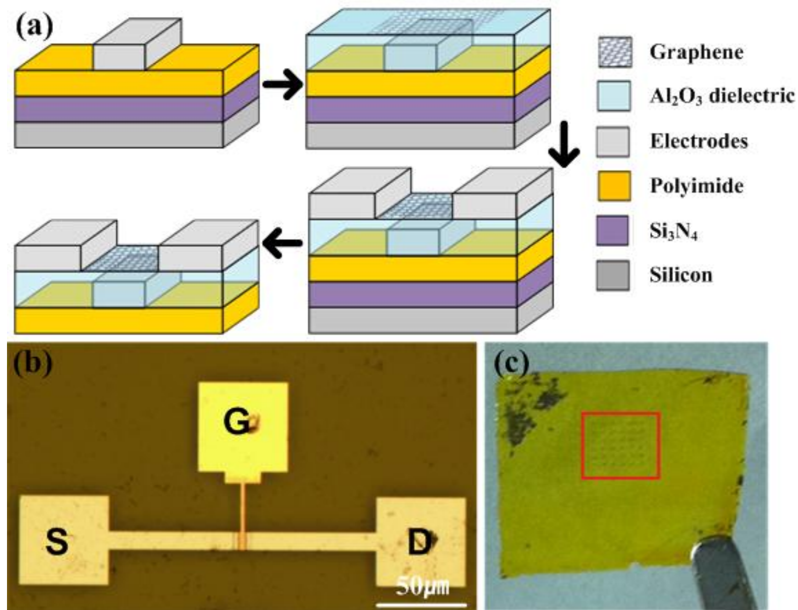

Figure 3.3. Embedded-gate graphene FET (a) Illustration of the EGFET fabrication process on spin-coated PI on a Si_3N_4/Si substrate. (b) Optical image of a completed EGFET. The device length and width are 4 and 8 μm respectively. (c) Photograph of the flexible substrate with an array of EGFETs. The highlighted square shows the array of devices.

EBL, evaporation, and liftoff. Liquid-type PI (PI-2574 from HD Microsystems) was spin-coated on the patterned sample and cured under nitrogen to capture the device structures within PI. Thermal oxide was then etched by buffered-oxide-etchant (BOE) and the PI films with embedded gates and dielectrics were released (capture-release process). The released sample was then annealed again under nitrogen to provide a clean high-quality interface between graphene and dielectrics (two-step annealing process). Monolayer graphene film grown by chemical vapor deposition (CVD) process was transferred via the poly(methyl methacrylate) (PMMA) assisted wet-transfer process using ammonia

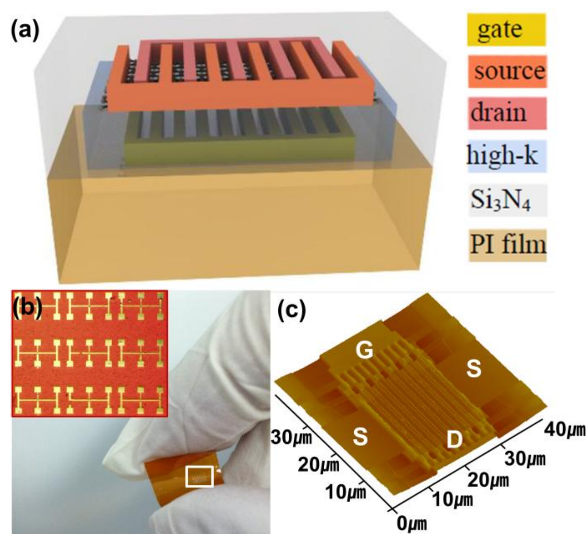

Figure 3.4. Multi-finger EGFET fabricated on plastic substrates. (a) 3-D image of the complete device of a 10-finger unit cell. (b) Optical image of the sample. The device area is highlighted by a white rectangle. Inset shows an array of the unit cells with gate (G), source (S), and drain (D) pads. (c) AFM image of the active channel area revealing a device with 10-fingers.

persulfate as a copper etchant.[46] Redundant area of graphene film was removed by oxygen plasma etching. Finally, source and drain electrodes were defined to complete the device structure (Figure 3.5b).

A high-resolution image over the active channel area and an optical image of the free-standing PI substrate with the device are shown in Figure 3.5c and 3.5d, respectively. Figure 3.5e shows an AFM topographical scan of the h-BN film after anneal and Figure 3.5f compares the surface roughness of several gate dielectrics for GFETs on plastics. Previous works in our lab were focused on improving the surface quality of plastics by applying additional liquid-type layer and/or depositing high-k dielectrics over flexible films. The surface roughness has been remarkably improved down to 1~2nm

using these methods,[48] however, its roughness is still higher than monolayer graphene, which can introduce mechanical strain and result in band structure deviation and transport degradation.[49,50]

Comparison of Device Structures

Three device structures, namely, top-gate GFET (TG-GFET), embedded-gate GFET with high-k dielectric (EG-highk/GFET), and embedded-gate GFET with h-BN dielectric (EG-hBN/GFET), which is the modified version of the previous EGFET to integrate h-BN into PI films, were fabricated on PI and evaluated in this work. Due to uneven surface topography of polymeric films, additional treatments are necessary to achieve the best lithographic resolution and registration.[38] In brief, PI films were spin-coated with liquid polyimide (PI2574 from HD Microsystems) and cured. TG-GFETs were prepared directly on these substrates, while others require more processing steps before graphene-transfer; ALD Al_2O_3 or exfoliated h-BN films were prepared as gate dielectrics. Optimized annealing was performed at 300ºC to improve the surface smoothness of h-BN films under nitrogen ambient. Figure 3.5f compares the roughness of the surfaces evaluated in this work. While the surface of as-exfoliated h-BN film is comparable to that of high-k on PIs, it is further improved by annealing as shown in the figure. After annealing, h-BN flakes on PI show the root mean square (RMS) roughness ~0.4nm, comparable to the inter-layer spacing and indicative of an almost perfect residue-free interface.

Table 3.1 compares the merits of the three device structures, investigated in this work. TG-GFET has an issue with the need for insulating seed layer prior to deposit

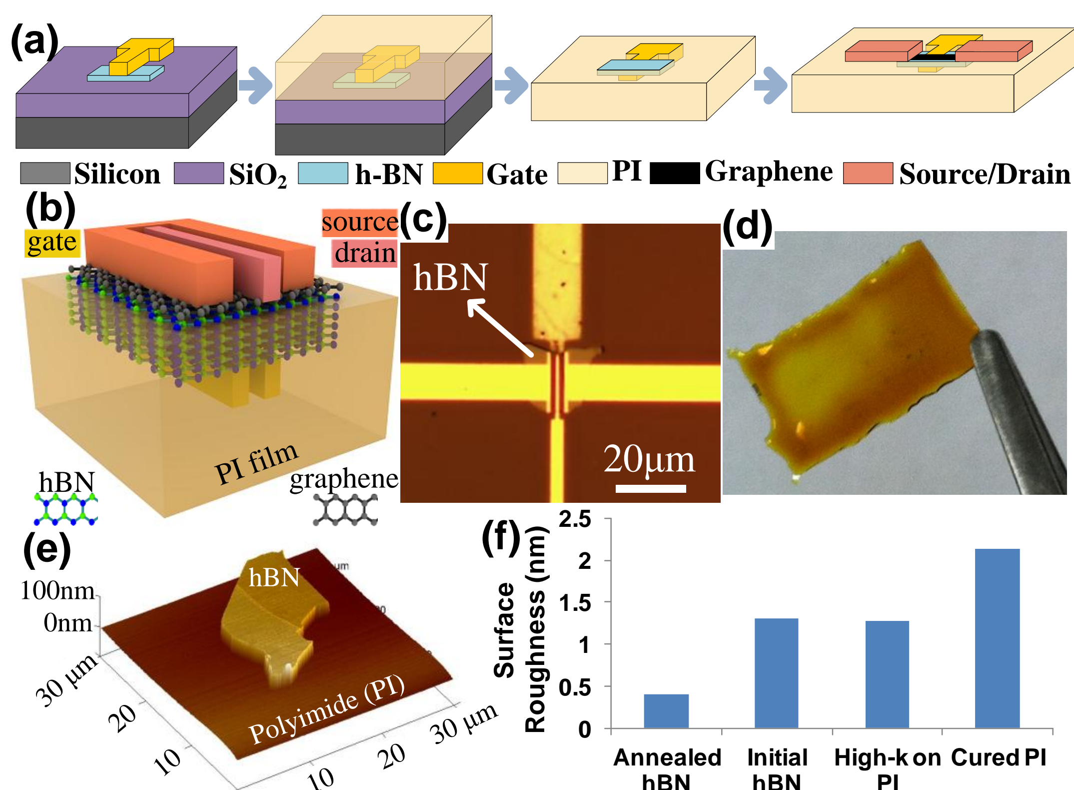

Figure 3.5. Illustration and images of fabricated EG-hBN GFET. (a) Simplified process flow. (b) Illustration of a fabricated device. (c) Optical image of the channel area with a dual-finger embedded-gate GFET. (d) GFETs on a PI film. (e) Surface of the smooth h-BN on flexible PI as measured by AFM. (f) Comparison of different surface roughnesses for graphene integration on flexible PI. The annealed h-BN surface features smoothness comparable to interlayer spacing in graphene.

ultra-thin high-quality dielectric over channel, which makes it difficult to scale down the oxide thickness. For embedded gate devices, oxide scaling is not a critical issue. While h-BN offers the best interface for GFET, substantial research has to be done to synthesize large-area uniform (monolayer to few layer) h-BN films. This leads to the conclusion that

while embedded-gates with h-BN dielectric is ideal, EG-highk/GFET is the best practical device structure for now because further synthesis progress is needed for the integration of h-BN/graphene layers.

Table 3.1 *Comparison of 3 flexible GFET device structures*

Device process \ Device structure	TG-GFET	EG-hBN/ GFET	EG-highk/ GFET	Comments
Finger scalability in a single layer	No	Yes	Yes	Realizing large # of fingers is straight - forward without the need for 2nd interconnect level.
Gate dielectric seed layer	Needed	None	None	Seed layer is needed for even coating of high-k on graphene. Not needed for embedded-gate.
Gate dielectric scalability	No	Yes	Yes	For top-gate devices, seed layer prevents ultra-thin dielectrics (<5nm).
Automated gate dielectric process	Yes	No	Yes	Currently, growth and transfer of uniform large-area sheets of h-BN is not available.
Expected GFET performance	Good	Excellent	Very good	h-BN gate dielectric is expected to yield the best GFET performance

Chapter 4: Design Considerations for Optimization

The two most important metrics to quantify the high frequency response of the RF device are the transit frequency, f_T, and the maximum oscillation frequency, f_{MAX}. These are highly dependent on intrinsic and extrinsic device parameters. In order to achieve the highest RF performance, we need to take a look at which parameters affect the metrics. The following equations ((1) - (3)) are for (1) the intrinsic transit frequency, (2) the extrinsic transit frequency, and (3) the maximum oscillation frequency.[51]

$$f_{T,int} = \frac{g_m}{2\pi C_{gs}} \qquad (1)$$

$$f_{T,ext} = \frac{g_m}{2\pi\left(C_{gs}+C_{p,gs}+C_{p,gd}\right)\left(\left(R_{p,s}+R_{p,d}\right)g_d+1\right)+C_{p,gd}g_m\left(R_{p,s}+R_{p,d}\right)} \qquad (2)$$

$$f_{MAX} = \frac{f_T}{\sqrt{2g_d\left(R_{p,s}+R_{gate}\right)+2\pi f_T C_{p,gd}R_{gate}}} \qquad (3)$$

where g_m is the transconductance, g_d is the drain-conductance, C_{gs} is the gate capacitance, $C_{p,gd}$ and $C_{p,gs}$ are the parasitic gate-to-drain and gate-to-source capacitances, $R_{p,s}$ and $R_{p,d}$ are the parasitic resistances at the source and drain electrodes, and R_{gate} is the gate resistance.

The reduction in the channel length is the most straightforward way to improve the intrinsic f_T since the intrinsic f_T scales proportional to $\frac{1}{L}$.[52] The extrinsic f_T can be dominated by the device parasitics. Currently, the source/drain electrodes for our devices show much higher resistances than the values frequently obtained from other reports on GFETs; the contact resistances from our devices range from 1k $\Omega\cdot\mu m$ to 5k $\Omega\cdot\mu m$, while other reports show mostly less than 1k $\Omega\cdot\mu m$ or even less than 100 $\Omega\cdot\mu m$. This requires more investigations on the interface between graphene and metal electrodes and proper designs to reduce the contact resistance.

The power gain, f_{MAX}, is also the important metric for RF devices. The improvements on f_{MAX} can be achieved by (1) reduction in parasitics by better layouts or fabrication, and (2) reduction in the gate resistance.

Contact Resistance

The contact resistance of graphene transistors consists of the following components: the metal electrode interconnection, the un-gated graphene resistance, and the resistance at the metal-graphene interface. By utilizing the highly conductive metals like gold as the electrodes, the first term can be improved, while the second term can be neglected with the proposed gate-overlap device structure. This makes the last term, the resistance at the metal-graphene interface, becomes the most critical component determining the overall contact resistance of the fabricated device. The low quality interface, leading to the high contact resistance, is the fundamental limiting factor on the electrical performance of graphene devices. It can degrade the transconductance and the cutoff frequency of GFETs by more than an order of magnitude.[53]

Previously, the fundamental charge transport physics on the graphene metal contacts and interface quality were investigated to provide better understanding on the graphene-metal contact resistance. [47,54–57]

The chemical residues can be introduced onto graphene films during the transfer of graphene films from Cu foils to desired substrates for fabrication. PMMA used during this transfer process can reside on the graphene surface and it is difficult to be completely removed from the surface by acetone during the cleaning process. The detrimental effects from these residues on graphene devices result in poor electrical performances with low field-effect mobilities. High vacuum annealing (1×10^{-9} mbar) at 300°C for 3 hours has

been suggested to remove them.[47] However, annealing samples at 300°C for extended time is not feasible for flexible substrates which are not thermally stable. Another approach suggested using an Al sacrificial layer prior to lithographic steps defining contact patterns.[54] In this case, the effect from the chemical residue can be minimized since the chemical is not touching the graphene surface at any time during the entire lithographic procedures, which results in up to 10X improvement in a contact resistance.

The selection of contact metals also plays a role determining the electrical performances of graphene FETs. A theoretical study using density functional theory suggested that the doping of graphene can be induced by adsorption on metal films and the cross-over of doping from p-type to n-type can be also expected by utilizing different metals (more importantly utilizing their work-functions).[55] Another experimental study also showed the p-n junction formation at the interface of graphene/metal can be induced by utilizing different metals; high work-function metals afford a more transparent interface (p-type to p-type) for hole transport in contrast to electron transport that involves a p-n junction interface with an additional contribution to the contact resistance.[58] This effect can lead to the asymmetry in the contact resistance between electron and hole transports.[48,59]

Recently, another publication suggested an interesting idea to further reduce those values. In order to improve the carrier injection at the metal-graphene interface, the contact regions of graphene devices are patterned into multiple cuts.[60] By simply modifying the design under the contact areas, two carrier injecting mechanisms, "edge-contacted" injection and "top-contacted" injection, contribute to lower the contact resistance values by 22~32% compared to those values without patterns.[60]

In our work, the contact resistances coming from source and drain metal electrodes interfacing with the graphene channel offers a great portion of the total resistance, limiting its extrinsic electrical performance. In order to access the complete usefulness of the fascinating properties of graphene, we introduced the patterned contacts to improve the carrier injection at the interface between metal contacts and the graphene channel.

The total contact resistance is the parallel combination of the interface resistance at the metal-graphene interface by the top-contacted injection, R_{Top}, and the resistance coming from the edge-injection effects, R_{Edge}.

$$R_{Total} = R_{Top} \,//\, R_{Edge} \quad \text{.......... (4)}$$

The equation given above can be also expressed in terms of the conductance for analysis.

$$G_{Total} = G_{Top_Total} + G_{Edge_Total} \quad \text{.......... (5)}$$

$$G_{Total} = \sigma_{Top/width} \cdot W_{Channel} + \sigma_{Edge/width} \cdot W_{Edge} \quad \text{.......... (6)}$$

where G_{Total} is the total conductance through the contacts, G_{Top_Total} is the contribution through the metal-graphene interface, and G_{Edge_Total} is for the contribution from the edge charge injection. Again, the equation can be further expanded considering the channel width, $W_{Channel}$, and the electrode width for the edge injection, W_{Edge}, and the per-width partial conductances from the top-contacted injection and the edge-contacted injection effects.

In the experiment, we fabricated devices with different contact patterns as given in Figure 4.1. Figure 4.1a is the conventional contact layout without edge-injection patterns. The device has a multi-finger (6 fingers) configuration with narrow metal

electrodes for minimum edge-injection effect. Figure 4.1b is the proposed contact layout with line-type edge-injection patterns and Figure 4.1c is another proposed contact layout with array-type edge-injection patterns.

The contributions from the top-injection at the metal-graphene interface and the edge-injection can be extracted from electrical measurements. Firstly, the devices are measured to extract the contact resistance values for each patterned structure. Then, a simple matrix calculation can be used to extract the individual contributions as follows. R_{Total} is extracted directly from the electrical measurements, while other parameters of $W_{Channel}$ and W_{Edge} are from the physical layouts.

$$G_{Total} = \frac{1}{R_{Total}} \qquad (7)$$

$$\begin{pmatrix} W_{Channel_1} & W_{Edge_1} \\ W_{Channel_2} & W_{Edge_2} \end{pmatrix} \cdot \begin{pmatrix} \sigma_{Top/width} \\ \sigma_{Edge/width} \end{pmatrix} = \begin{pmatrix} G_{Total_1} \\ G_{Total_2} \end{pmatrix} \qquad (8)$$

$$\begin{pmatrix} \sigma_{Top/width} \\ \sigma_{Edge/width} \end{pmatrix} = \begin{pmatrix} W_{Channel_1} & W_{Edge_1} \\ W_{Channel_2} & W_{Edge_2} \end{pmatrix}^{-1} \cdot \begin{pmatrix} G_{Total_1} \\ G_{Total_2} \end{pmatrix} \qquad (9)$$

From the electrical measurements, the total contact resistances are extracted as follows.

$$R_{Total,Type-I} = 93.03\ \Omega$$

$$R_{Total,Type-II} = 53.67\ \Omega$$

$$R_{Total,Type-III} = 40.28\ \Omega$$

After calculating the partial contributions, the resistances from each component are also extracted.

$$R_{Top} = \frac{1}{\sigma_{Top/width} \cdot W_{Channel}} = 108\ \Omega$$

$$R_{Edge,Type-II} = \frac{1}{\sigma_{Edge,Type-II/width} \cdot W_{Edge}} = 114\ \Omega$$

$$R_{Edge,Type-III} = \frac{1}{\sigma_{Edge,Type-III/width} \cdot W_{Edge}} = 63.9\ \Omega$$

The patterned contacts, Type-II and Type-III, offered lower contact resistances compared to the conventional one, Type-I. The data confirm the array-type (Type-III) patterned contacts offer the effective reduction in the total contact resistance while providing an additional 25% reduction in the contact resistance compared to the line-type (Type-II) patterned contacts.

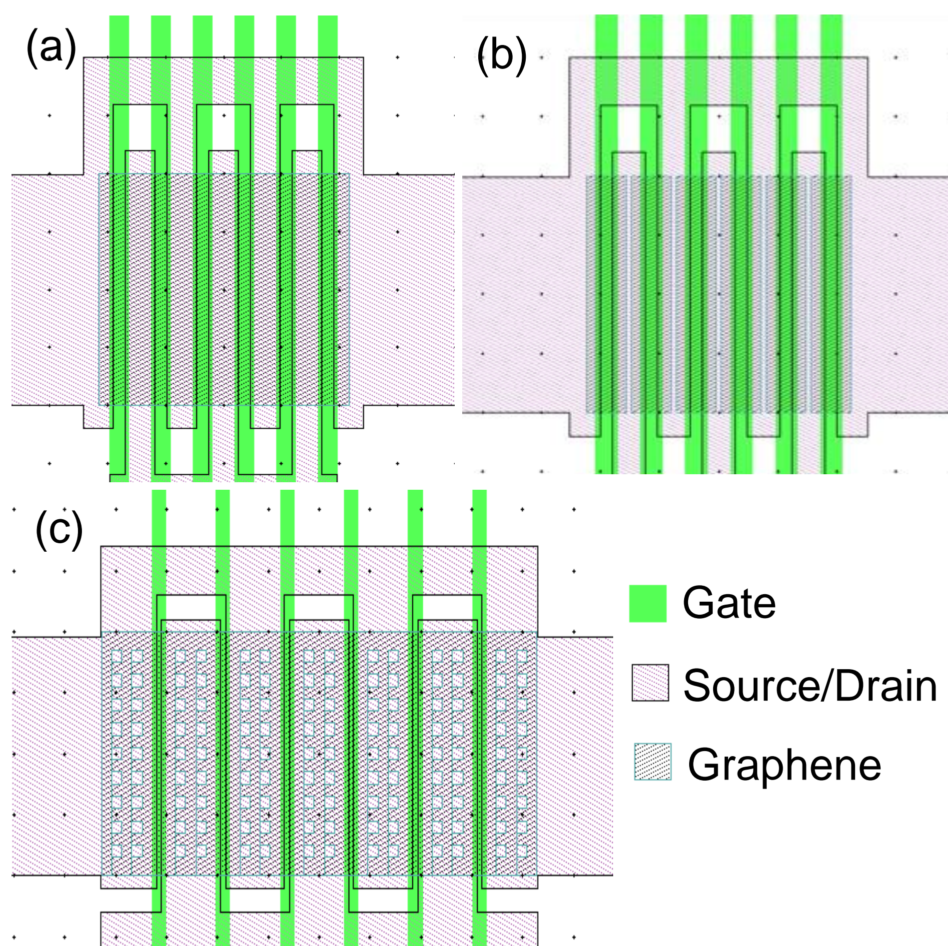

Figure 4.1. Contact electrodes patterns. (a) Type-I. Conventional contacts without edge-injection patterns. (b) Type-II. Contacts with line-type edge-injection patterns. (c) Type-III. Contacts with array-type edge-injection patterns.

Embedded-Gate Electrodes

Since the power gain, f_{MAX}, strongly depends on the gate resistance, we investigated different options for preparing the embedded-gate electrodes. While selecting the materials, several things to be considered in this process are i) surface oxidation of the metal, which leads to higher resistance over time, ii) high electrical conductivity for lower resistance, iii) structure of the embedded-gates in order to minimize the device parasitics, and iv) surface roughness over the metal film. The last requirement is crucial since the graphene devices are currently prepared on top of the gate metals covered with dielectric films to have an embedded-gate structure to access high electrical performance as mentioned in the previous chapter.

In this work, we compared Ti/Pd (2nm/80nm), Ti/Ag/Pd (2nm/70nm/10nm), Ti/Pd/Au (2nm/10nm/70nm) for preparing gate electrodes. The first one stands for the reference device that we routinely utilize to implement graphene field-effect transistors. Palladium offers reasonably low resistance while providing smooth surface where short-channel devices are easily implemented. Silver and Gold are considered in order to further reduce the gate resistances. Since the surface oxidation of Silver is detrimental while that has negligible effects on Gold, we covered the Silver electrodes with an additional Palladium of 10nm to prevent this surface oxidation.

The electrical conductivities of the three candidates are compared via the TLM (transmission line method) measurements to extract their sheet resistance values. The surface roughness values are also compared using an atomic force microscopy scanning over 15μm x 15μm area for each candidate. Figure 4.2 shows the comparison of these candidates.

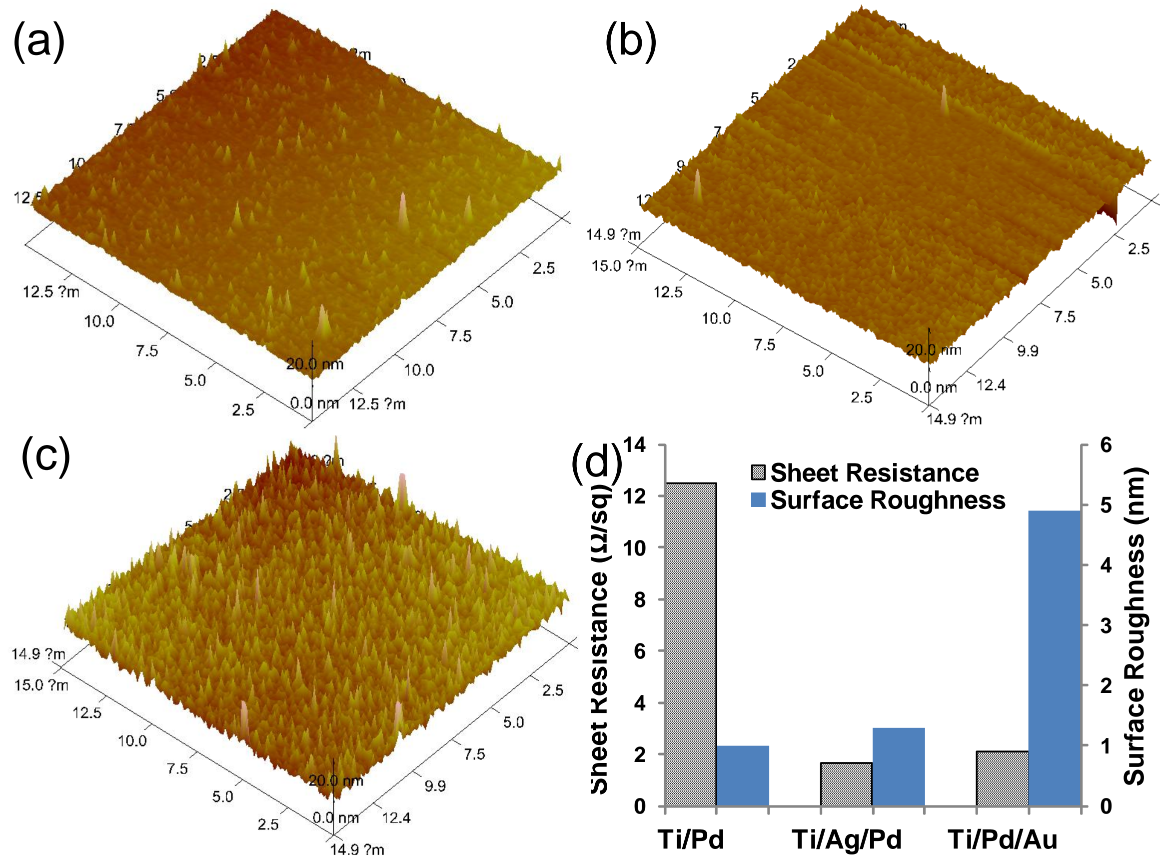

Figure 4.2. Comparison of gate electrodes. (a) AFM image of Ti/Pd (2nm/80nm). (b) AFM image of Ti/Ag/Pd (2nm/70nm/10nm). (c) AFM image of Ti/Pd/Au (2nm/10nm/70nm). All images are scanned over 15㎛ x 15㎛. (d) Comparison of sheet resistances and surface roughness values for three candidates.

As shown in Figure 4.2d, Ti/Ag/Pd offers the highest electrical conductivity along with a reasonable surface roughness making it as the most fascinating choice among the compared candidates. Ti/Pd offers the best (lowest) surface roughness while providing relatively higher sheet resistance, which may severely limit the power gain performance of the fabricated device. The last option of Ti/Pd/Au also offers a reasonable sheet

resistance, however the un-even surface limits its usefulness as the embedded gate electrodes.

Another way to further improve the electrical conductivity of the gate electrodes is increasing the thickness of the metal stacks. The direct deposition of high metal stacks leads to proportionally lower resistance at the cost of higher parasitic capacitances as shown in Figure 4.3a. The better way to deal with this issue would be introducing the trench structure where the gates electrodes are fully embedded (Figure 4.3b). The extension length of source and drain electrodes over the gate electrodes is 200nm for the prepared device leading to the parasitic overlap capacitance, $C_{OV,TOP}$. With 50nm-thick gate electrodes, the parasitic component of the side-wall overlap capacitance, $C_{OV,SIDE}$, increases the overall parasitic capacitance by additional 25%. Increase in the thickness of this metal stack would also increase this parasitic part leading to the limited extrinsic high frequency performance. In order to avoid this trade-off, we suggest the trench-type gate electrodes as shown in Figure 4.3b to remove the side-wall overlap capacitance while lowering the gate-overlap capacitance and also effectively increasing the cutoff frequency performance of the device. Figure 4.3c shows the simple self-aligned patterning technique to define the dielectric trench and deposit the embedded gates in one lithography step. The electron-beam lithography is used to define the trench patterns and the fluorine-based dry etch etches the nitride trenches where the metal electrodes are refilled via the electron-beam evaporation and the subsequent liftoff process.

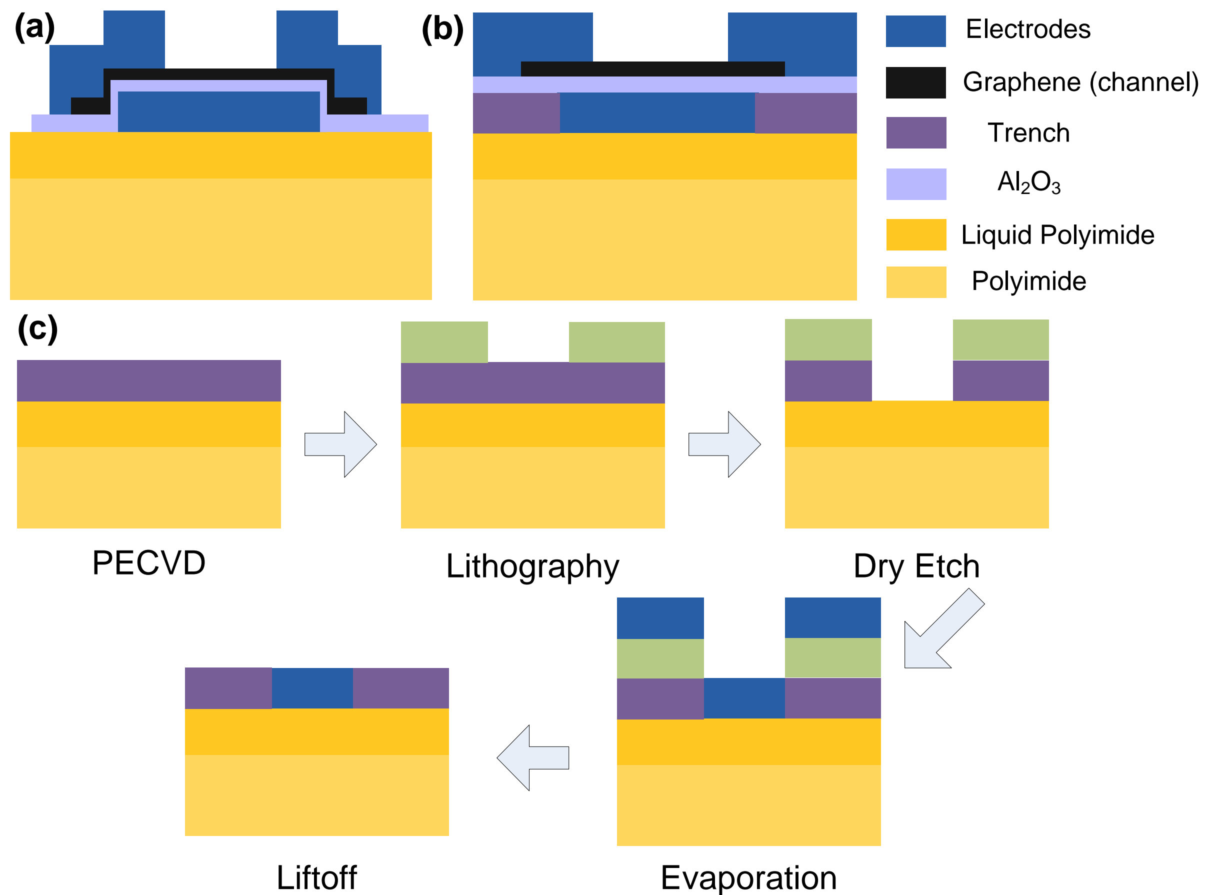

Figure 4.3. The embedded gate structures. (a) Direct deposition of gate electrodes on the substrate. (b) Gate electrodes embedded in dielectric trench structures. (c) Simplified process steps to prepare the self-aligned gate-electrodes embedded in the dielectric trench.

The successful patterning of trenches strongly depends on the high-aspect ratio reactive-ion-etching and the high-selectivity between the e-beam resist (PMMA) and the dielectric material used for the trench structures. Here, we used the plasma-enhanced chemical vapor deposited silicon nitride for the dielectric material. This process enables

the deposition of thick dielectric films and its low-temperature process (250°C) is compatible with the flexible substrates.

For the reactive ion etching of nitrides, CF_4 is commonly used, however it also shows a very high etch rate for PMMA. Introducing Ar can significantly improve the etching selectivity while lowering the etch rate for PMMA. We used the 790 Plasma Therm RIE Etcher during this process. The process condition is as follows. 50 sccm of CF_4, 20 sccm of Ar, RF power of 100W, and the pressure of 80mTorr. Figure 4.4 shows the results. Figure 4.4a is the AFM image of the patterned trenches showing the area for the 6-finger gate electrodes and the pad. Figure 4.4b is another AFM image of the same area after refilling metals using the electron-beam evaporation of Ti/Ag/Pd. The height of the metal stack and the depth of the trench are determined to be the same (80nm) to provide the flat surface where the devices are to be implemented. The etch rate for the nitride and PMMA are 114nm/min and 88nm/min, respectively, offering the good etch selectivity of over 1.29:1. The thickness of the resist layer is 250nm.

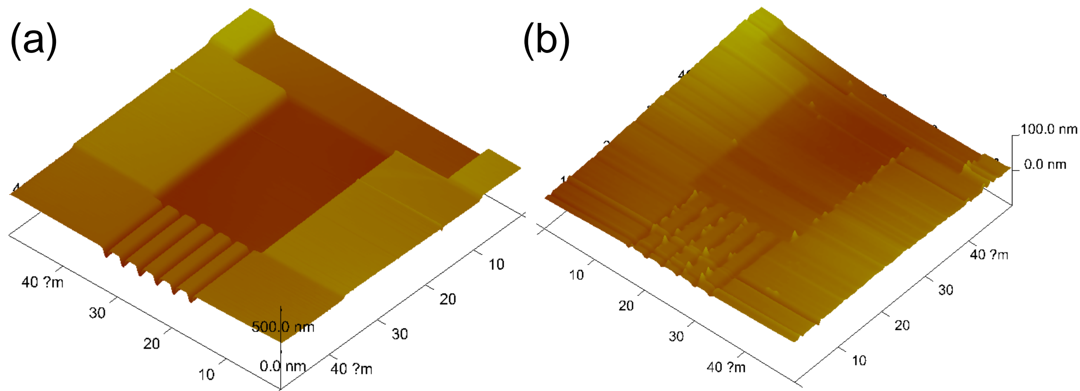

Figure 4.4. The trench refilling process. (a) AFM image of the patterned trenches showing the area for the 6-finger gate electrodes and the pad. (b) AFM image of the same area after refilling metals using the electron-beam evaporation of Ti/Ag/Pd.

Passivation Techniques for Embedded-Gate Structures

While the embedded-gate GFETs outperform the conventional top-gate GFETs as described in Table 3.1, the still remaining issue is the passivation of exposed graphene channel. The proper passivation is required for 1) improved hysteresis, 2) preventing degradation during device operation, 3) mechanical robustness, and 4) protection over direct liquid exposures. Several approaches have been reported for GFETs on conventional rigid substrates: bilayer (organic/inorganic) passivation,[61] PECVD silicon nitride directly on graphene,[59,62] and hydrophobic organic polymer spincoated on graphene.[63]

Here, we have investigated different options: ALD high-k dielectrics, PECVD Si_3N_4, bilayer films of PECVD Si_3N_4 covered with CYTOP fluoropolymer.

ALD Dielectrics

The first one we investigated is using ALD dielectrics. ALD films offer high quality dielectric films good for both gate oxides and device passivation layers. Several high-k dielectric materials are available including Al_2O_3, HfO_2, and ZrO_2. However, this process requires the deposition of an insulating seed layer prior to deposit dielectrics over graphene due to the chemical inertness of graphene surface and not reliable.[64] While preparing this film as the gate dielectric, we can still avoid this issue by adopting the embedded-gate FET structure.[59,65]

PECVD Dielectrics

PECVD is another option and oxides and nitrides are routinely deposited on substrates as interlayer dielectrics, passivation layers, or gate dielectrics. PECVD oxide is excluded among the feasible candidates for the device passivation since it requires the deposition involving oxygen radicals, which effectively etch the graphene channel leaving pin-holes after the deposition.[62] The conventional PECVD recipe for Si_3N_4 is also evaluated. However, still the graphene channel has been degraded during plasma process significantly degrading the field-effect mobility of the device after passivation. The modified recipe using low power N_2-rich PECVD[62,65] could prevent this degradation in its electrical properties and also offers good mechanical robustness.[59] When the nitride-passivated sample is exposed to liquids, the nitride passivation layer fails to protect the underlying FET device and the device experienced significant reduction in quality over time, which will be covered shortly in the later chapter.

Integration of Organic Polymers on Graphene

Several publications suggest the usefulness of organic polymers introduced on graphene surfaces as promising options to enhance or modify the electrical properties of graphene devices prepared on rigid substrates.[66–68]

Self-assembled monolayers (SAMs) are molecular thin films formed via chemical or physical interactions of molecules with a substrate without the utilization of high-temperature or vacuum processes.[69] B. Lee et al reported that they could successfully grow uniform and stable fluoroalkyl silane self-assembled monolayer (FTS SAM) on the graphene surface, which leads to a high level of hole doping effect with a density of up to 1.5×10^{13} cm^{-2}.[66] Even though the field-effect mobility from the graphene device

degraded significantly, this approach highlights the potential of SAM layers for graphene electronics with the capability of modifying the electronic properties of devices.

Another report focused on the effect of the hydrophobicity of supporting layers; a thin, hydrophobic self-assembled layer of hexamethyl disilazane (HMDS) was introduced on the supporting substrate prior to the fabrication of graphene devices.[67] From the results, the hysteresis coming from the adsorption of dipolar substances on graphene surface could be minimized or improved via the HMDS treatment on substrates. This suggests that SAMs are also useful to access the superior electronic properties of graphene with low intrinsic doping level, which is largely dependent on processing conditions and ambient conditions, in a reproducible manner.

More recently, T. -J. Ha reported spin-on-fluoropolymers offer a simple and fascinating method to achieve a restorative effect on electrical properties of graphene field-effect transistors.[68] The strong polar nature of the C-F chemical bond in the spin-on fluoropolymer deposited on graphene devices results in the favorable improvements in all aspects of electrical properties of graphene devices including high field-effect mobility, low Dirac voltage close to zero, and very low residual carrier density.

While aforementioned approaches may offer promising options to change or enhance the electrical properties of graphene, low boiling points and melting points of most organic polymers prevent the direct introduction of these materials on graphene FETs prepared on plastic substrates where the temperature on the active channel area can become significantly higher than those values. Here, as an alternative way, we utilize a bi-layer structure of PECVD Si_3N_4 and hydrophobic fluoropolymer. This preserves the electrical performance of the graphene devices along with the additional benefit of

protection over liquids and its results on the electrical performance will be covered in the later chapter.

Thermal Management

Due to poor thermal stability of most flexible substrates, the thermal management for these films has crucial effects on realizing reliable high performance flexible devices. Especially, the 2-D material operating under high current density like graphene, this becomes more significant issue. Figure 4.5 exemplifies this issue on flexible GFETs.

The physical deformation of the device (shown in Figure 4.5b) results from the fact that the GFET is implemented on the thermally unstable material with low thermal conductivity (polyimide). Due to both low glass transition temperature of plastic substrates and elevated channel temperature at high bias, flexible films tend to melt or deform under these conditions. The current saturation, which is essential to obtain high f_{MAX}, can be achieved under high lateral field and, partly for this reason, current-saturating GFETs on plastics are not easily realized while similar devices are reported frequently on rigid substrates. This needs some ways to prevent direct heat transfer from the channel to the substrate. Diverse solutions on this matter are currently under active investigation: direct heat spreading via electrodes, and integration of high thermally conductive dielectrics as heat spreading layers and dielectric heat insulators to protect the substrates.

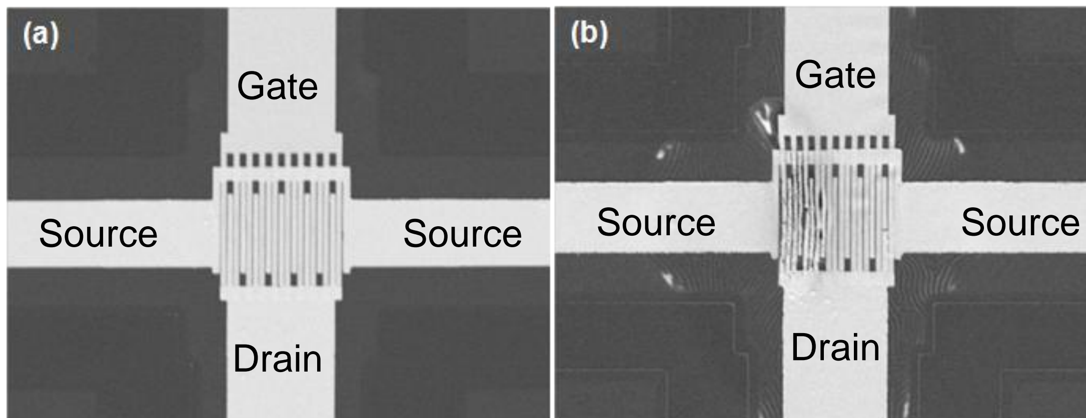

Figure 4.5. Thermal effects on GFETs under high lateral electric fields. (a) SEM image of the GFET before applying high electric fields. The device has a multi-finger electrodes configuration and the graphene channel is located at the center of the image. (b) SEM image of the same device (damaged) after applying high electric fields.

Chapter 5: Experimental Results : Electrical / Mechanical Performances

DC Characteristics of Graphene Field-Effect Transistors

Electrostatic measurements for hBN-EGFET are presented in Figure 5.1. The device parameters were extracted and showed good agreements with a widely used diffusive transport model.[64] The extracted mobilities were 2,324cm^2/ V · s and 2,307cm^2/V·s for holes and electrons, respectively. While the quality of CVD graphene on evaporated Cu film is very good, however, the graphene domains are smaller than those achieved on Cu foil. Hence for our devices, transport is likely occurring over several grain boundaries which limits the carrier mobility. Low impurity concentration ($<5x10^{11}/cm^2$) owing to high quality dielectric interface, allows symmetric charge transport and high mobility. High work-function metal electrodes (50-nm Au) form excessive junction resistance for electron transport and reduce the drive current.[56] Relatively high extracted contact resistance of 800 Ω·μm indicates that the current density can be further enhanced by improving the metal-channel interface. Current saturation, which also offers record-high current density from flexible GFETs, was observed for the first time on flexible plastics as shown in Figure 5.1b and 5.1c with strong agreement with a validated GFET circuit model;[70] data reported on previous works on flexible substrates so far only provide the linear I-V relation without any current saturation.[71,72] We note that our device model includes both velocity saturation (~2 x 10^7cm/s) and electron-hole charge crossover phenomena, which account for the current saturation in graphene.[73] The current saturation observed in our device is due to velocity saturation as determined from device modeling. h-BN offers high quality interface with low impurity density and high thermal conductivity; beneficial properties that enables

access to the intrinsic graphene device behavior under high fields. This, in addition to low contact resistance from clean metal deposition is crucial for observing velocity and current saturation.[73]

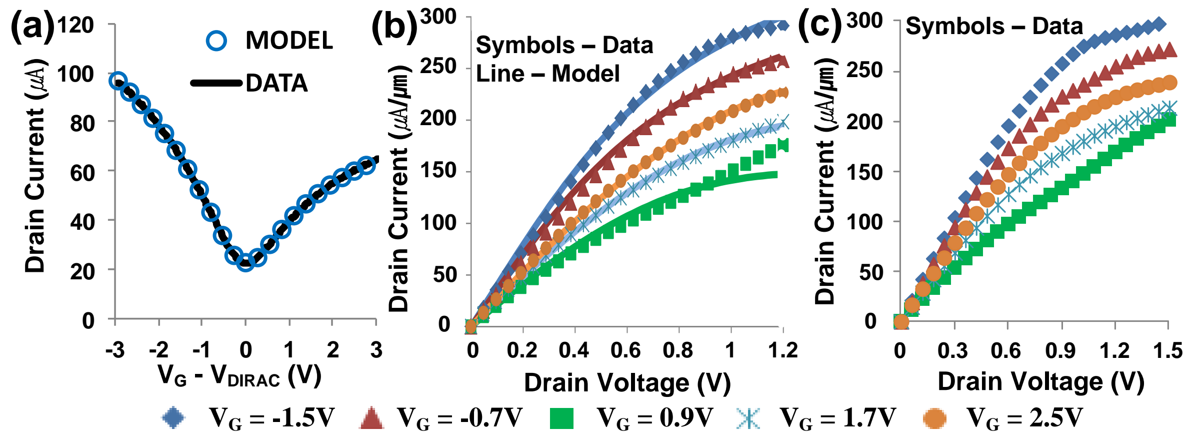

Figure 5.1. DC measurement of hBN-EGFET. (a) I_D-V_G profile measured at V_D of 10mV. (b) I_D-V_D profile showing the current saturation. (c) I_D-V_D profile at V_D up to high-field of 1.5V.

Figure 5.2 shows the electrical properties of the multi-finger EGFETs evaluated under ambient conditions; the device is utilizing a modified CVD-process grown graphene films to achieve the highest electrical performance, which offers exfoliated quality large-area graphene films.[74] The gate modulation over the total resistance including contributions from the graphene channel and the metal contacts from the lithography-free device and the EBL patterned device are shown in Figure 5.2a and 5.2b, respectively. The lithography-free devices have the same process flow (same metal electrodes and dielectrics) as the EBL patterned device with the exception of a global bottom-gate instead of patterned finger-type electrodes used in the other devices in order

to identify the highest performance achievable with pristine, un-damaged (during the lithographic process introducing several chemicals and mechanical handling) graphene films. Data have good agreement with a low-field diffusive transport model for graphene transistors.[64] The peak carrier mobilities of 8,000 $cm^2/V{\cdot}s$ from the lithography-free device and 3,900 $cm^2/V{\cdot}s$ from the EBL device are measured and confirmed with the device model. The asymmetry in the carrier transport comes from the use of high work-function metal as electrodes, which favors hole transport while introducing additional junction resistances for electron transport.[59] The degradation in the carrier mobility from the latter device is coming from the undesirable resist residue left on the graphene channel,[47] which requires further studies on an efficient resist removal and surface cleaning process compatible with flexible substrates.

The hBN-EGFET, which offered the high symmetry in both electron and hole transports along with low impurity density, was also evaluated as a frequency doubler. The graphene frequency doubler has been previously reported to offer intrinsically high spectral purity (>90%) without filtering.[70,75] The input and output terminals were terminated with a 50Ω cable/load typical of RF circuits and the GFET was biased at the Dirac point. Figure 5.3a shows the graphene frequency doubler circuit. Figure 5.3b shows the output power at the doubled frequency as a function of the input power at the fundamental frequency. The solid line in Figure 5.3b is a visual guide with a slope of 20dB/decade that indicates the expected behavior of an ideal square law doubler. The inset is a photograph of the signal analyzer display. The conversion gain (CG) is -29.5dB with an output power of -22.2dBm, which was afforded by the low impurity interface between graphene/h-BN and the low inter-plane thermal conductivity of h-BN, which protected the underlying PI from thermally induced deformation and damage at high

fields. At higher input power, the even/odd symmetry from the transistor output characteristics introduces some non-linearity which degrades the doubler conversion loss and spectral purity.[76]

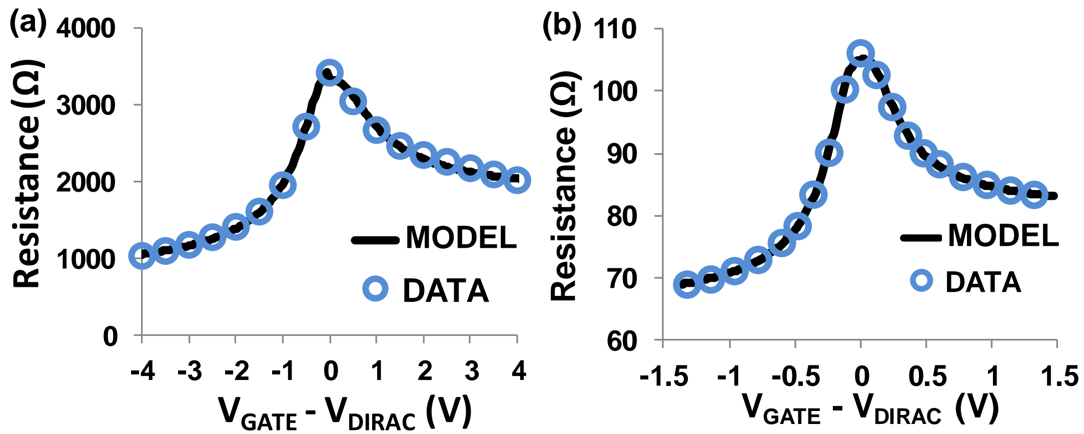

Figure 5.2. Electrical measurements. (a) Gate modulation from the lithography-free GFET with the carrier mobility of 6,600 $cm^2/V{\cdot}s$ for hole transport and 8,000 $cm^2/V{\cdot}s$ for electron transport. (b) Gate modulation of the EBL GFET showing the carrier mobility of 2,800 $cm^2/V{\cdot}s$ for hole transport and 3,900 $cm^2/V{\cdot}s$ for electron transport, respectively. The device has a channel length of 0.5㎛, and effective width of 100㎛.

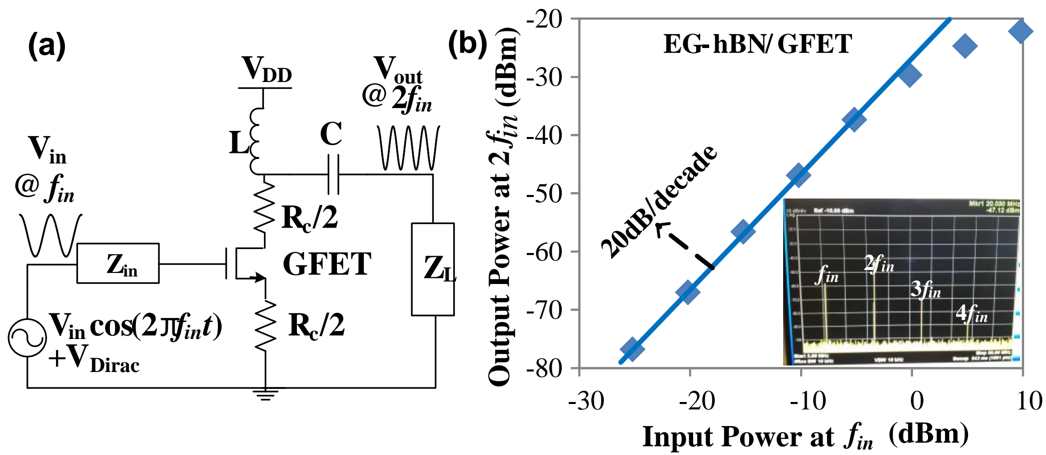

Figure 5.3. Experimental GFET frequency doubler circuit on flexible PI. (a) Schematic for doubler evaluation. (b) GFET output-input doubler characteristics (f_{IN}=10MHz, V_D=0.5V).

Figure 5.4 is the simulated performance assessment of a GFET frequency doubler with ultra-scaled gate dielectric consisting of a monolayer of h-BN. Figure 5.4a shows the impact of charge impurity density on the I_D-V_G curvature and gate modulation, parameters that are critical for doubler operation. Figure 5.4b is the dependence of the maximum CG on device parameters. In order to reach the theoretical limit of GFET doublers, several requirements have to be satisfied including high gate capacitance, low charge impurity density, and low contact resistance.[31] A theoretical CG of ~-4.5dB is predicted in 50Ω systems indicating that optimized GFETs with scaled h-BN dielectrics can outperform ideal varistor diode doublers. The inset shows the dependence of the maximum CG on contact resistance. There is negligible impact for Rc<100Ω-μm.

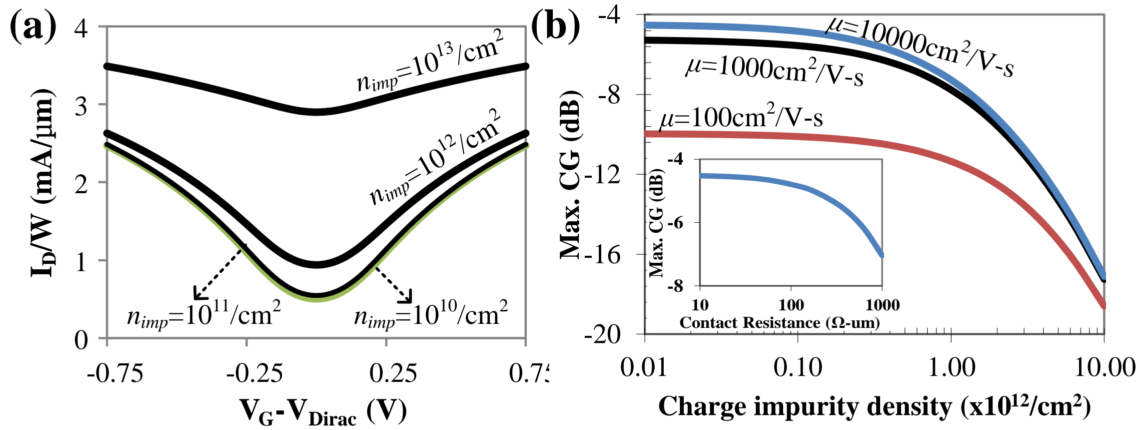

Figure 5.4. Simulated ultimate performance prediction of GFET frequency doubler with ultra-scaled gate dielectric. (monolayer h-BN, L=0.2μm and W=100μm. μ=10,000cm²/V-s) (a) Detrimental impact of charge impurity density on gate modulation. (b) The dependence of the max CG on device parameters. The inset is the dependence on contact resistance.

High Frequency Response (f_T and f_{MAX})

A central motivation for exploring graphene is its high-speed charge transport which can enable RF and high-frequency electronic applications on flexible substrates. In this light, we experimentally evaluated its scattering parameters (S-parameters) to determine the current gain (h_{21}) and cut-off or transit frequency (f_T) which is a key metric of device speed.[77–79] The as-measured S-parameters typically include delay contributions from parasitic capacitance and interconnect resistance that prevents direct evaluation of the intrinsic speed of charge carriers.[79] The parasitic components arise from the metal electrodes used in the RF device structure. To overcome this limitation, we employ a two-step de-embedding method that involves measurement of so-called *open* and *short* test structures identical to the device structure and fabricated on the same substrate but

without the graphene active layer in order to subtract out the parasitic capacitance and resistance respectively.[78,79] The intrinsic current gain is shown in Figure 5.5a revealing an f_T ~ 25 GHz. We note that the graphene contact resistance which represents a heterogeneous interface resistance is not removed by the de-embedding method. Hence, the extracted 25 GHz f_T reflects a conservative estimate of intrinsic speed especially in light of the relatively high contact resistance (3kΩ-μm) in the present device.

The extracted flexible GFET f_T is about 50% lower than the highest reported GFETs of similar channel length on conventional hard substrates,[78] albeit the drain voltage of our flexible GFET is less than half of that on the hard substrate. The low thermal conductivity and glass transition temperature of plastic sheets are a barrier that restricts the fields and current densities necessary to probe the ultimate cut-off frequency on flexible substrates.[31,32] Basic exploration of heat management materials (such as hexagonal boron nitride and other suitable thin films) is a matter of critical importance for advanced flexible electronics and warrants awareness and further studies. An f_{MAX} ~ 2.1 GHz was extracted from Mason's unilateral gain as given in Figure 5.6. The relatively low f_{MAX} is due to the well-recognized impact of un-optimized gate metal resistance and gate-drain coupling capacitance.[79,80] Applied research utilizing self-aligned T-gate structures on flexible substrates is needed in order to achieve substantial improvement in f_{MAX}.[61,81]

The intrinsic cut-off frequency can also be estimated from the well-established analytical expression for field-effect transistors.

$$f_T = \frac{g_m}{2\pi C_{gc}} \qquad (10)$$

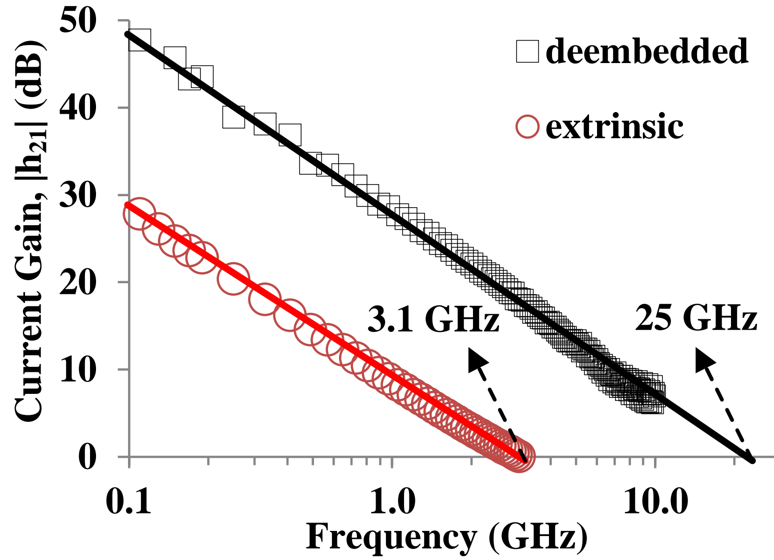

Figure 5.5. The extrinsic and intrinsic cut-off frequency measured from the device. The de-embedded current gain reveals an intrinsic f_T of 25 GHz for flexible GFET.

where g_m is the intrinsic transconductance and C_{gc} is the gate to channel capacitance. Normally, C_{gc} is taken to be the gate oxide capacitance (the parallel plate capacitance between the gate metal and the channel layer). However, owing to the relatively thin (10 nm) high-k dielectric used in our device, the contribution from the quantum capacitance (C_q) cannot be neglected. C_q can be considered approximately 2,000 nF/cm^2 for the typical range of carrier densities (1-10 x10^{12} cm^{-2}). This value was also previously used by Petrone et al.[32] The effective C_{gc} is the series combination of the oxide capacitance and the quantum capacitance. Capacitance-voltage measurements of test structures with identical high-k deposition condition and thickness yielded a gate oxide capacitance of ~600 nF/cm^2, which resulted in an effective C_{gc}~124.5 fF for the device.

Owing to source and drain metal contact resistance, the intrinsic device g_m is different from the measured extrinsic transconductance symbolized by G_m (dI_d/dV_g). In brief, G_m includes the detrimental effects of metal resistance, while g_m is solely due to the graphene transistor. From classical circuit theory, the transistor with source resistance (R_S) and a possible drain resistance (R_D) is considered a source-degenerated common-source transistor.[82] The intrinsic g_m can be extracted from the extrinsic G_m *via* the relation for source-degenerated transistor

$$g_m = \frac{G_m}{1 - G_m\left[R_S + (R_S + R_D)/(G_m / G_{ds})\right]} \quad (11)$$

where G_{ds} is the extrinsic device conductance (dI_d/dV_d). Measurements of a test structure with the same source and drain metal patterns of the device yielded an estimate of 68 Ω and 22.67 Ω for R_S and R_D respectively. The experimental device was biased around the peak (hole) transconductance (~100 μS at V_D=0.01 V). Since the device is operating in the linear region, it is expected that the G_m scales linearly with V_D, resulting in G_m~5 mS at the drain bias of 0.5 V used for the f_T measurement. From above relation, the intrinsic g_m is extracted to be 24.2 mS. This results in an estimated f_T ~ 30.9GHz in close agreement with the experimental deembedded data shown in Figure 5.5. The extrinsic f_T can also be estimated analytically by including the parasitic overlap capacitances. The sum of the overlap of the source and drain fingers with the gate finger is about 400 nm, which results in an estimated extrinsic f_T ~ 3GHz which is in good agreement with the experimental data reported in Figure 5.5. We note that the ratio between intrinsic and extrinsic cut-off frequency in this work (~ a factor of 8) is significantly less than the ratio between intrinsic and extrinsic frequencies reported in other works,[77,83] which could be as large as a factor of 128.[77]

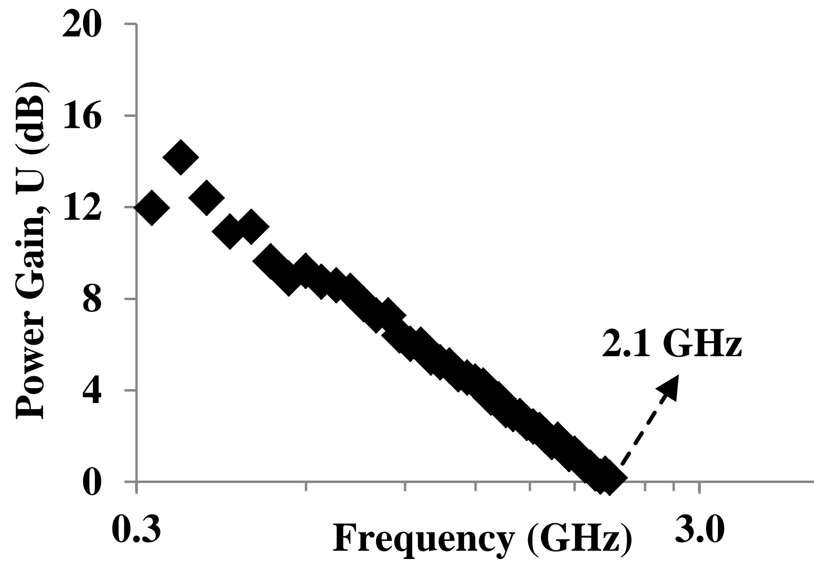

Figure 5.6. The power-gain frequency measured from the device.

As mentioned in the previous chapter, the reduction in the channel length is the most straightforward way to improve the intrinsic f_T performance without significant changes in device structures or deposited materials. Here, we scaled the channel length of the GFETs down to 0.25㎛. Without any change in device structures, the intrinsic f_T has been improved by 40% from 25 GHz to 32 GHz as shown in Figure 5.7. The former device has the channel length of 0.5㎛ and the later device has the channel length of 0.25 ㎛. Devices for both measurements are biased at the same high lateral electric field of 1V/㎛. Initially, the 2X improvement in the intrinsic transit frequency was expected due to the reduction in its channel length from 0.5㎛ to 0.25㎛. However, due to the lower quality graphene film of the later device with low field-effect mobility results in relatively moderate improvement in the intrinsic transit frequency by 40%. Despite of this moderate improvement, further investigations to improve the quality of CVD-grown graphene films and more aggressive reduction in its channel length will invariably

provide even higher performances suitable for future high-performance electronic applications. Also from the analysis on the extrinsic and intrinsic high-frequency performances, currently the overlap parasitic capacitance from the device structure limits the extrinsic device speed and highlights the need for a suitable self-aligned FET structure compatible with bendable flexible substrates.

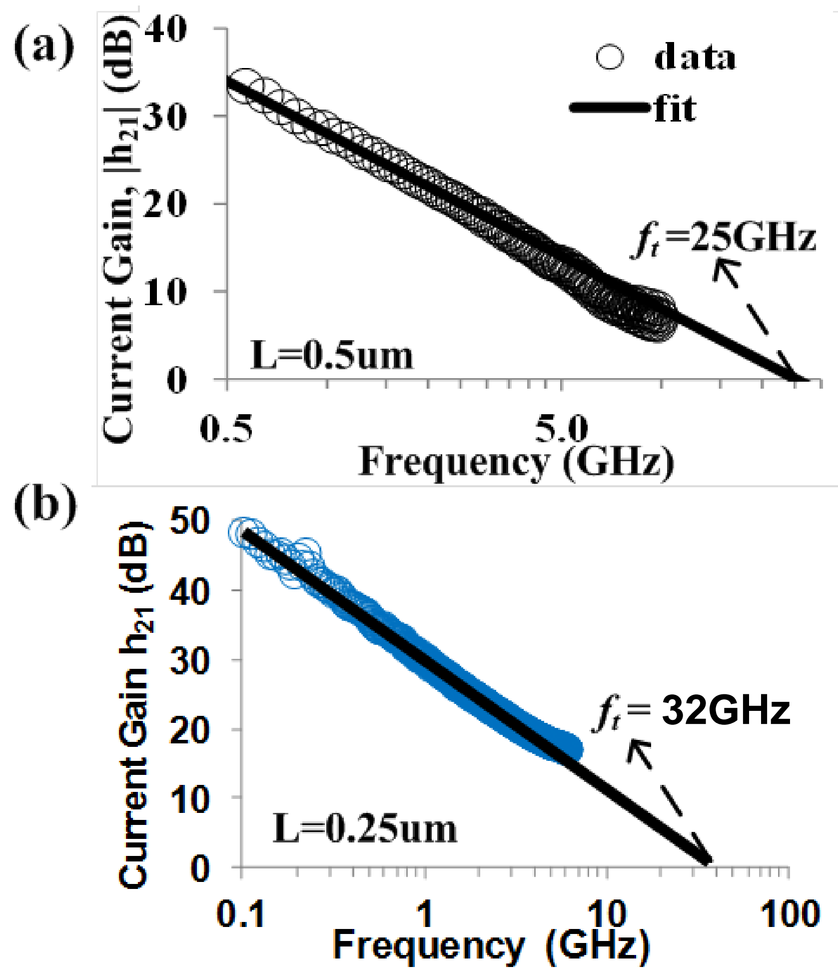

Figure 5.7. Channel-length scaling of GFETs. (a) Intrinsic cut-off frequency measured from the 0.5㎛ channel-length device. V_{DS} = 0.6V. (b) Intrinsic cut-off frequency measured from the 0.25㎛ channel-length device. V_{DS} = 0.3V.

Mechanical Bendability

The components integrated in the fabricated devices have two broad categories: flexible components and rigid components. While graphene film (with ε_{CR}~25%),[84] and PI substrates (with ε_{CR}~10%), are considered as flexible components, high-k dielectrics (prepared by ALD) and metal electrodes are regarded as rigid components in this work. While the maximum achievable mechanical flexibility (ε_{CR}~10%) is limited by the critical strain of PI substrates, the issue is how we can improve the flexibilities of rigid components.

In order to understand the failure mechanisms of rigid components during mechanical bending, test structures with metal interconnects and metal-oxide-metal (MIM) capacitors were prepared and experimentally evaluated as given in Figure 5.8. Figure 5.8a shows the change in normalized conductance from metal interconnects corresponding to the bending radius down to 0.7 mm; G stands for the conductance at the specific bending radius while Go represents the original value under the flat condition. Figure 5.8b presents the similar test results for capacitors; $10\times10\mu m^2$, $50\times50\mu m^2$, $100\times100\mu m^2$, and $200\times200\mu m^2$ unit devices were patterned on PI substrates; 30-nm thick ALD Al_2O_3 was deposited as dielectrics. The metal interconnects show lower conductances (40% reduction) at smaller bending radius owing to mechanical deformation and elongation making locally thinner lines with higher resistance. While supported on polymeric substrates, metal electrodes are uniformly stretched so as to approach their maximum allowable strain without degradation of over 4%,[85] which corresponds to the bending radius of ~1.5 mm. Beyond this point, metal films show increasing resistance while still maintaining functionality, indicating good adhesion at the PI interface without de-bonding of metal films from the substrate.[86] In Figure 5.8b, MIM

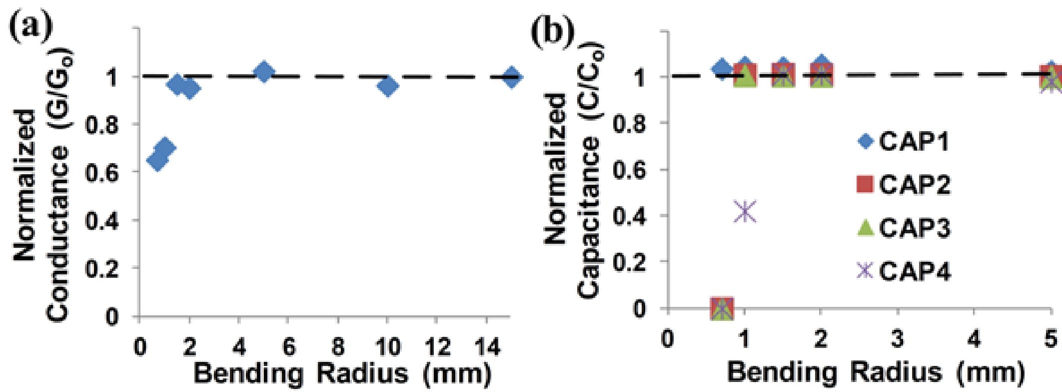

Figure 5.8. Mechanical bending experiments for metal interconnects and MIM capacitors on PI films. (a) The change in conductance of metal lines. (b) The change in normalized capacitances of MIM capacitors. CAP1, CAP2, CAP3, and CAP4 are 10x10µm^2, 50x50µm^2, 100x100µm^2, and 200x200µm^2, respectively. The dashed line is a visual guide indicating invariant properties over a wide bending radius.

capacitors are evaluated. Here, C and Co are the capacitance at the specific bending radius and the original capacitance under the flat condition, respectively. The largest unit cell (CAP4 with 200µm×200µm dimension) shows dramatic reduction in its value at the radius of 1 mm and total failure at smaller radius. CAP2 (50µm×50µm) and CAP3 (100µm×100µm) cells failed at the minimum bending radius of 0.7 mm. The smallest unit cell (CAP1) didn't lose functionality even at the smallest bending radius. These results supports the idea that by predefining local dielectric islands where the active channel is located, the bendability of the flexible devices can be further improved and maximized with perhaps a small degradation of the electrical properties owing to increased electrode resistances.

The mechanical flexibility of the GFET was also evaluated with custom designed bending test fixtures. In order to achieve high flexibility, the rigid components (electrodes

and gate dielectrics) integrated in the device are patterned. While un-patterned devices only survive the maximum bending radius of 2 mm, which corresponds to ~ 3% tensile strain mostly due to the dielectric breakdown,[59] the patterned devices can survive bending down to a radius of 0.7 mm, which corresponds to ~ 8.6% strain. The tensile strain (ε) is computed according to the relation $\varepsilon = t_s/(2R_B)$ where t_s and R_B are the substrate thickness and bending radius respectively.[32,86] During the measurements, the normalized resistance extracted from the device model has been monitored as shown in Figure 5.9a; no noticeable degradation was observed. Figure 5.9b shows the robust electrical performance of the device; the mobility remains over 80% compared to the value at the flat condition at the minimum bending radius of 0.7 mm. Repeated measurements under the minimum bending radius shown in Figure 5.9c and 5.9d confirm the reliability of the graphene device structure. At lower bending radius, we observe mechanical breakdown of the gate dielectric leading to high gate leakage and poor gate modulation, however, the metal electrode is structurally intact and remains conductive.[59]

The graphene transistors were also evaluated in a variety of harsh conditions as given in Figure 5.10, that can be hazardous for conventional monolithic electronics. The sample was exposed to mechanical stresses such as a walking test at ~4ft/sec, and automobile driving test at ~5miles/hr. The human and automobile weigh approximately 1,15lbs and 3,300lbs, respectively. As seen in Figure 5.10, the GFETs retain their electrical functionality under these harsh conditions. In the graphene device selected for monitoring, the degradation in current was less than 4%. The mobility dropped by as much as ~40% after immersion in warm coffee, but recovered to 90% of the initial mobility after the walking test, indicating that the impact of the warm fluid is at least partially reversible likely owing to thermal relaxation and fluid desorption.

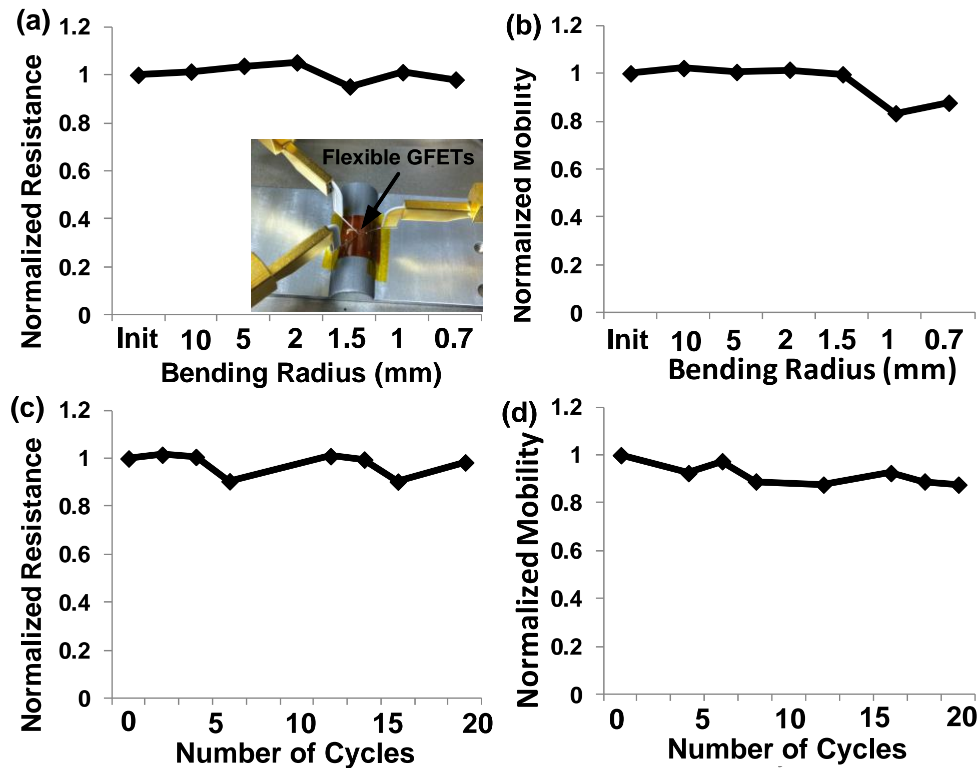

Figure 5.9. Mechanical bending measurements. The change in (a) normalized resistance and (b) normalized mobility under different bending radii down to 0.7 mm. The inset in (a) shows the flexible GFETs attached to the bending fixture. Repeated measurements of (c) normalized resistance and (d) normalized mobility at the minimum bending radius of 0.7 mm.

These electrical results suggest that nitride passivated GFETs on PI provide a route for realizing high-performance rugged nanoelectronic systems. More systematic precision uniaxial compressive loading and impact testing are required for further electro-mechanical understanding.

Figure 5.10e shows the frequency doubler performance of the device evaluated after completing dynamic loading tests. The frequency doubler evaluated in this work showed high-spectral purity (>90%) while affording a peak conversion loss of ~39.7dB,

which is within 5dB of our earlier report achieved with graphene transistors on a smooth single-crystal quartz substrate.[70] These results motivate further developments of graphene-based analog and RF circuits on flexible sheets.

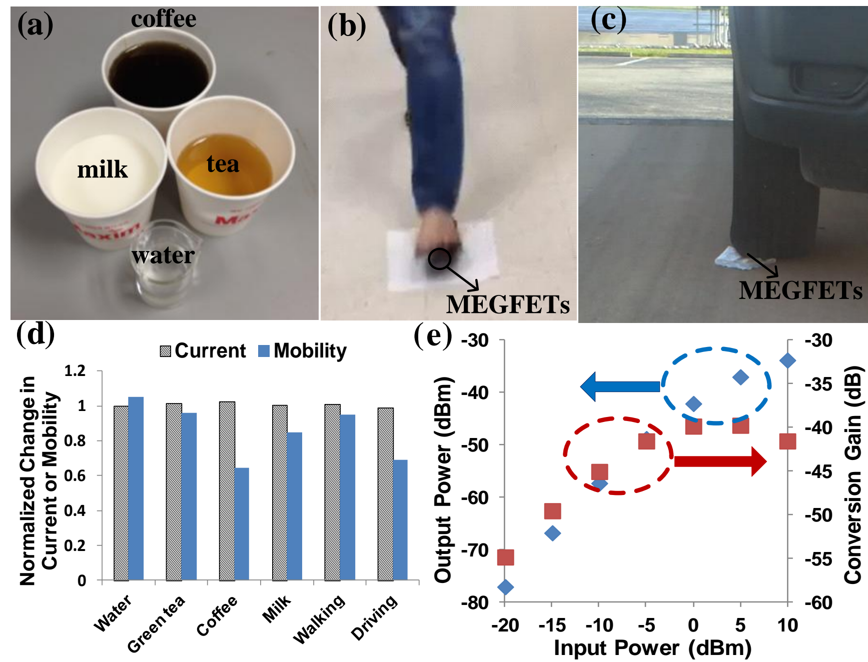

Figure 5.10. Experiments involving harsh conditions. (a) Still image of the devices been walked over to emulate a slow-moving load. (b) Still image of 2002 Honda CRV sport-utility vehicle going over the devices. (c) Doubler characteristics. The output power at the doubled frequency (2f) and the conversion gain as a function of the input power at the fundamental frequency (1f=2MHz) are given. The gate is biased at the Dirac point and V_D = 300mV.

Liquid Exposure

The effective encapsulation and protection of the flexible GFET by an hybrid bilayer (inorganic/organic) coating to liquid exposure (DI water) has been evaluated by the static contact angle measurements. The FTA200 contact angle goniometer is used to measure the contact angles for different passivation materials investigated including bare PI films, cured PI films, PECVD Si_3N_4, and CYTOP® coating on the flexible devices. The fabricated sample was self-passivated at the back-side by the bare PI substrate, while the top-side of the device was implemented on the smooth, cured PI surface and passivated by Si_3N_4/CYTOP bilayer.

Figure 5.11 shows the optical images captured by the optical microscope attached to the goniometer. During the measurement, DI water of 20µL is dropped on each surface. Bare PI films offer high hydrophobicity with high contact angle of 82.5°, which affords good protection to DI exposure. However, the bare PI film is not recommended for integrated graphene devices due to the surface roughness and requires the coating/curing process to smoothen the surface.[38,59] After curing the spin-coated smoothing layer, the hydrophobicity of the PI surface is slightly reduced down to 79.2°. Si_3N_4 doesn't improve the hydrophobicity, though, it provides outstanding mechanical robustness even to extreme static loading conditions.[59] Of the different coating films investigated in this work, we identified highly hydrophobic CYTOP® which offers a high contact angle exceeding 110° as the most suitable water protection layer.

Figure 5.12 present the electrical measurements under DI water exposure; Figure 5.12a and 5.12b are the data from Si_3N_4 passivated devices and Figure 5.12c and Figure 5.12d are the data from the bilayer (Si_3N_4/ CYTOP) passivated devices. The devices were dipped into DI water for 10 s, dried with N_2 flow, and repeatedly measured. To evaluate

the short-term protection against DI water immersion, the measurements were repeated up to 150 s while monitoring the changes in the normalized resistance and the carrier mobility. As for the long-term DI water exposure, the same measurements were performed after immersion for 2 days. The dotted lines in Figure 5.12 represent the virtual boundary between short-term measurements and long-term measurements. The normalized resistance does not show any noticeable degradation for both cases, while the carrier mobility degraded significantly for nitride passivated devices down to 30% of the initial value. This reduction in the mobility is due to nonideal water protection from the nitride passivation layer. A low contact angle (less hydrophobic surface) of the layer allows water molecules to wet the surface and eventually introduces carrier traps in the dielectric interfaces, hence, weakening the gate modulation. The bilayer coated device shows no degradation of its resistance and slight degradation of its mobility, while providing 80% of the initial electrical performance. The improved water-resistant protection is attributed to the strong hydrophobic surface of CYTOP. This result suggests that functional coatings can be employed to protect flexible GFETs from water or liquid exposure, which is anticipated as a future requirement for robust flexible smart systems.

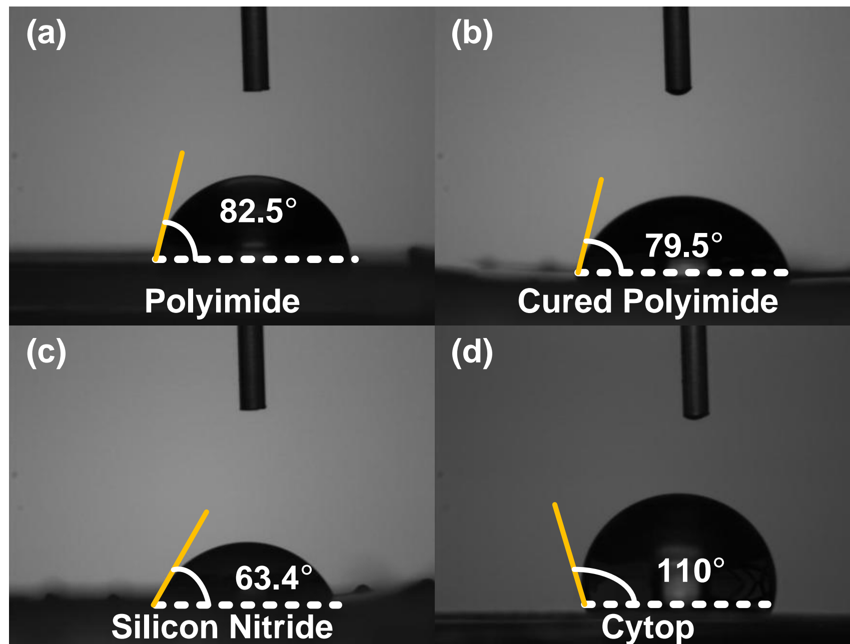

Figure 5.11. Contact angle measurements. 20µL DI water dropped on prepared samples including (a) as-received commercial polyimide film, (b) cured polyimide film, (c) PECVD Si_3N_4, and (d) Cytop coated on Si_3N_4/PI.

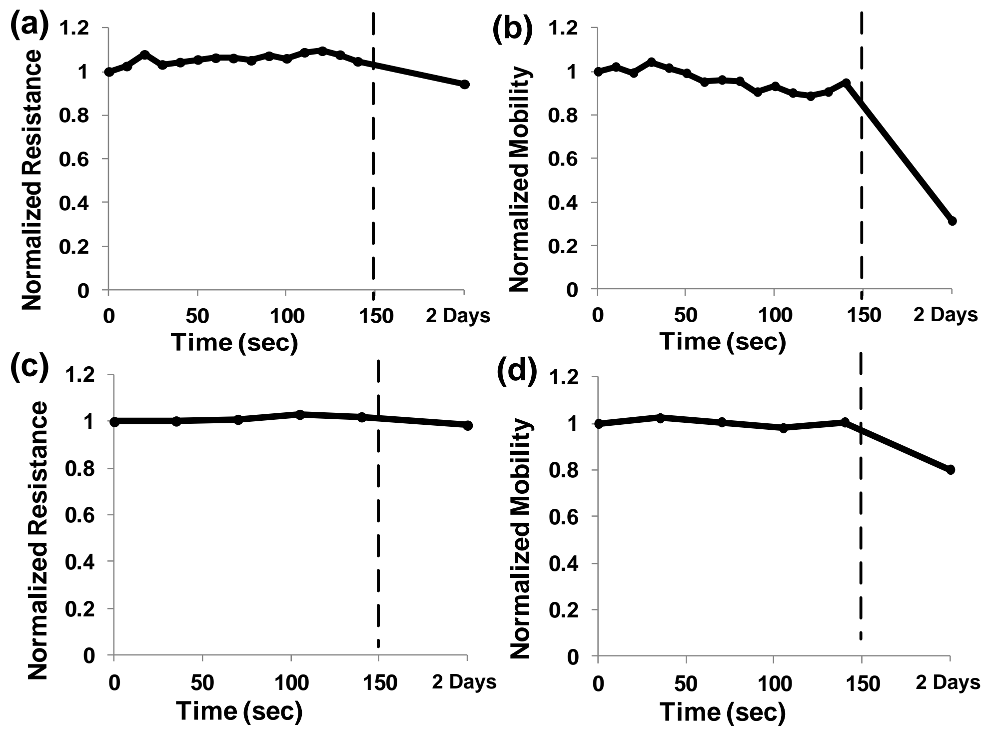

Figure 5.12. Immersion test results for the normalized resistance and mobility. Data shown on the left side of the dashed line are for short-term exposure to DI water, and data on the right side of the line are for long-term exposure to DI water. (a), (b) Normalized resistance and mobility measured from Si_3N_4 passivated devices. (c), (d) Normalized resistance and mobility measured from Cytop/Si_3N_4 passivated devices.

Chapter 6: Summary and Future Works

Summary

In this work we have realized the high performance graphene field-effect transistors on flexible plastic sheets. With the smoothened surface by applying and curing liquid PI, the surface roughness of the polymeric substrates could be significantly reduced so that the fabrication of novel devices are realized on those surfaces. The advanced technique using h-BN as the gate dielectric in PI films offers high electrical performance along with the first observation of the current saturation on plastic substrates. The embedded-gate device structure outperforms the conventional top-gate FET structure for several advantages: no need for the insulating seed layer prior to the gate dielectric deposition, dielectric scalability, and simpler fabrication process, which minimizes the chemical contamination to the graphene film during the device fabrication, which results in lower impurity density and higher electrical performance. The transistors are also robust against a variety of harsh conditions that are hazardous for conventional electronics, including immersion in liquids, and mechanical deformations; the devices remain fully functional with no significant degradation in their gate modulation. This study motivates further research on flexible graphene field-effect transistors and also accelerate the realization of high-performance flexible nanoelectronics.

Future Works

Future flexible smart systems will be integrated and realized on environmentally friendly flexible or plastic substrates. A major contemporary technical concern is the choice of the channel material suitable for high-performance field-effect transistors (FETs) with high flexibility. Graphene has shown its ability suitable for analog and radio-

frequency electronic devices while providing great mechanical flexibility and superior electronic properties as proven in this work. However, its lack of an electronic bandgap becomes a serious issue while implementing low-power electronics or simply digital logic applications.

Semiconducting transition metal dichalcogenides (TMDs) have been suggested as alternative options to provide low power capabilities. Among commercially available TMD materials, molybdenum disulfide (MoS_2) is investigated to implement low-power field-effect transistors for flexible electronics.[87] The design layouts and process techniques compatible with polymeric substrates studied and developed in this work are also applicable when implementing electronic devices out of those materials. Following the similar process flows, proto-type devices are fabricated and evaluated. Preliminary data measured from those devices offered good electrical properties including high current on-off ratio, sub-threshold slope, field-effect mobility, and current saturation. The current technical challenges include large-area uniform growth TMD materials via chemical-vapor deposition and implementation of CMOS out of these materials. Further studies on synthesizing continuous MoS_2 films are crucial for the successful outcome of this research.

Appendix

A.1. Preparation of Double-Side Coated Polyimide Substrates

Step	Details
1	Clean polyimide substrates - Acetone rinse for 10min - IPA rinse for 2min - Blow dry with N_2 gun
2	Attach polyimide substrates to silicon carrier wafers for handling
3	Spin-coat liquid polyimide (PI-2574) on polyimide substrates - Spin rate : 2000 rpm - Ramp rate : 2000 rpm/sec - Time : 30 sec
4	Curing of polyimide substrates Equipment : NEYTECH furnace - Vent / load spin-coated samples / pump down - Turn on N_2 flow (remain on during the entire procedure) - Ramp up to 200°C at rate of 4C°/min - Hold for 30 min for soft-bake - Ramp up to 300°C at rate of 2.5C°/min - Hold for 60 min for cure - Cool down to 80°C at rate of -4C°/min - Turn off N_2 flow - Unload cured samples - Detach cured samples from silicon carrier wafers

5*	Double-side coating - Repeat step-2 ~ 4 for the other side of polyimide substrates
6	Surface cleaning before lithography Equipment : Plasmatherm 790 - Oxygen plasma reactive ion etch for 10 sec (see Appendix A.3 for the details)

* This side becomes the top side of the substrate where devices will be patterned.

* The double-side curing process helps to cancel the built-in strain coming from the mismatch in the mechanical properties between the commercial polyimide film and the cured liquid layers while making the substrate more planar.

A.2. Wet Transfer Process of Graphene Films

Step	Details
1	Chemical Vapor Deposition of Graphene using Cu foils
2	Attach Graphene/Cu foil samples on silicon carrier wafers
3	Spin-coat PMMA A4 on Graphene/Cu foil samples - Step-1. Spin-rate : 500 rpm, Ramp-rate : 1000 rpm/sec, Time : 5 sec - Step-2. Spin-rate : 4000 rpm, Ramp-rate : 2000 rpm/sec, Time : 40 sec - Step-3. Spin-rate : 0 rpm, Ramp-rate : 2000 rpm/sec, Time : 1 sec
4	Detach the spin-coated samples from silicon carrier wafers
5	Leave the samples in a desiccator overnight to remove residual solvents
6	Back-side graphene etching - Load the spin-coated samples upside-down in an RIE system - Oxygen plasma RIE for 1min to remove back-side graphene films (see Appendix A.3 for the details)
7	Cu wet-etch - Prepare clean, triple-rinsed beakers - Pour ammonia persulfate (APS-100) in each beaker - Float the sample in the beaker to etch supporting Cu - Wait for 2 hours to complete etching Cu foils
8	Rinse samples with deionized (DI) water - Prepare three triple-rinsed beakers - Transfer one sample to the first beaker and wait for 30 min. - Transfer the sample to the second beaker and wait for 5 min. - Transfer the sample to the last beaker and wait for 5 min.

9	Transfer the sample to the target substrate
10	Dehydrate the samples overnight to remove residual moisture
11	Softbake samples at 180°C for 2~3min
12	Rinse samples with Acetone - Prepare a triple-rinsed beaker - Leave samples in the beaker for one day (Three cycles 6~8 hours each)
13	Visual inspection of transferred samples using an optical microscope
14*	Raman spectroscopy to confirm the quality of films

* Raman spectroscopy is not available when polyimide films are used as target substrates. Users should prepare a reference sample (oxidized silicon wafer with 285-nm thick thermal oxide) for this process.

A.3. Oxygen Plasma Reactive Ion Etch of Graphene Films

Step	Details
1	Equipment : Plasmatherm 790 Place samples on a silicon carrier wafer Load samples with a carrier wafer at the center of the chamber
2	Pump (pressure : 100 mTorr, hold time : 10 sec)
3	Evacuation (pressure : 10 mTorr, hold time : 1 min)
4	Purge (pressure : 200 mTorr, hold time : 30 sec)
5	Evacuation (pressure : 10 mTorr, hold time : 30 sec)
6	Process step 1 O_2 flow rate : 10 sccm, pressure : 200 mTorr no RF power applied, hold time : 1 min (fixed)
7*	Process step 2 O_2 flow rate : 10 sccm, pressure : 200 mTorr RF power : 50 W, hold time : 40 sec
8	Evacuation (pressure : 10 mTorr, hold time : 30 sec)
9	Purge (pressure : 200 mTorr, hold time : 30 sec)
10	Evacuation (pressure : 10 mTorr, hold time : 30 sec)

* Etch for 40 sec for patterning graphene channel area with PMMA as a mask.

A.4. Capture-Release Process for Exfoliated Hexagonal Boron Nitride Embedded in Polyimide

Step	Details
1	Prepare oxidized silicon wafer with 285nm-thick thermal oxide
2	Rinse silicon substrates with Acetone and IPA for 2min each
3	Spin-coat AZ-5209 (positive photo-resist) on silicon substrates - Spin-rate : 3000 rpm, Ramp-rate : 2000 rpm/sec, Time : 30 sec - Soft-bake at 95°C for 1min
4	Optical lithography to define alignment marks on substrates Equipment : EVG-Aligner - Hard-contact, Exposure time : 2.5 sec - Develop samples using MIF-726 for 1min
5	Ti/Au (2nm/50nm) deposition using e-beam evaporation
6	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water for 1min each
7*	Surface cleaning of silicon wafers - Oxygen plasma RIE for 1 min
8	Exfoliate hexagonal boron nitride films - Exfoliate PolarTherm (PT-110) from Momentive Performance Materials Onto the prepared silicon substrates
9	Visual inspection of exfoliated samples using an optical microscope
10	Atomic force microscope to confirm the thickness of exfoliated films Equipment : VeecoVR D-5000 (in tapping mode)

11	Annealing of h-BN films Equipment : NEYTECH furnace - Temperature : 300°C under N_2 ambient - Time : 1 hour
12	Digitize locations for h-BN films - Capture optical images of h-BN films - Use a graphic digitizer to extract locations for each h-BN film - Design layouts using polygons (See Figure A.3)
13	Spin-coat PMMA A4 on silicon substrates (see A.2 step-3) - Soft-bake at 180°C for 2min for a thickness of 180 nm
14	E-beam lithography of embedded gates Equipment : Carl Zeiss SEM/EBL - Expose the desired patterns with a 20 kV electron beam at 240 $\mu C/cm^2$ - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
15	Ti/Au (2nm/50nm) deposition using e-beam evaporation for gates
16	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water for 1min each
17	Apply liquid polyimide - Follow A.1 step-2 to step-3
18**	Wet-etch thermal oxide (sacrificial layer) - Leave prepared substrates in BOE (1:6) for 4~6 hours - Pick up detached polyimide films - Rinse polyimide films with DI water

	- Dehydrate polyimide films overnight
19	Post annealing of the polyimide substrates with embedded patterns Equipment : NEYTECH furnace - Temperature : 300°C under N_2 ambient - Time : 1 hour
20	Wet-transfer of graphene films (see A.2 for details)
21	Spin-coat PMMA A4 and ESpacer on polyimide substrates - Spin-coat PMMA A4 and soft-bake (see A.4 step-13) - Spin-coat ESpacer Spin-rate : 3000 rpm, Ramp-rate : 2000 rpm/sec, Time : 60 sec
22***	E-beam lithography of graphene channels Equipment : Carl Zeiss SEM/EBL - Expose the desired patterns with a 20 kV electron beam at 240 $\mu C/cm^2$ - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
23	Oxygen plasma etch of graphene channels (see A.3 for details)
24	Spin-coat PMMA A4 and ESpacer on polyimide substrates (see A.4 step-21)
25	E-beam lithography of source/drain electrodes Equipment : Carl Zeiss SEM/EBL - Expose the desired patterns with a 20 kV electron beam at 240 $\mu C/cm^2$ - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
26	Ti/Au (2nm/50nm) deposition using e-beam evaporation for source/drain
27	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water

* This improves the adhesion between h-BN films and substrates resulting in higher yield during the subsequent exfoliation process.

** Cured liquid polyimide films will be detached and this will work as a new substrate for device fabrication with fully embedded h-BN films.

*** Layouts have to be horizontally inverted since for the sample is released from silicon substrates. (See Figure A.5)

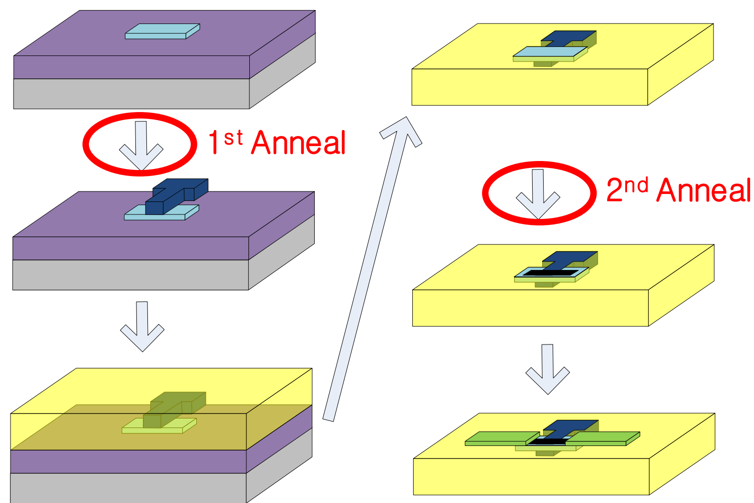

Figure A.1. Process steps for embedded-gate GFETs with h-BN films

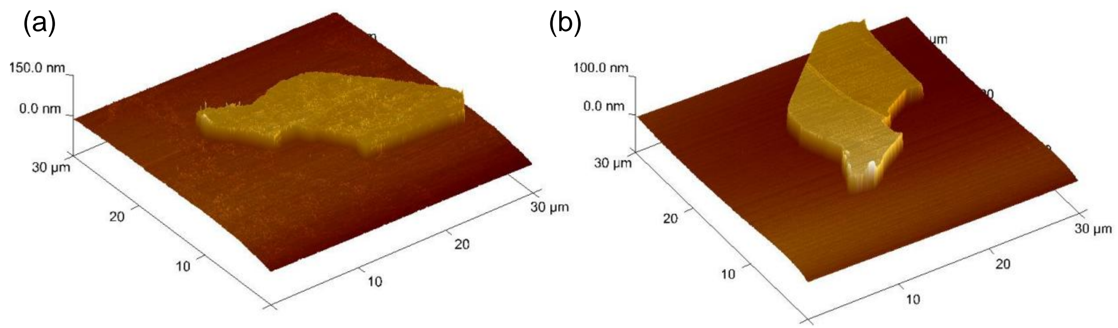

Figure A.2. Exfoliated h-BN films. (a) AFM image captured as exfoliated, (b) AFM image captured after annealing under nitrogen ambient

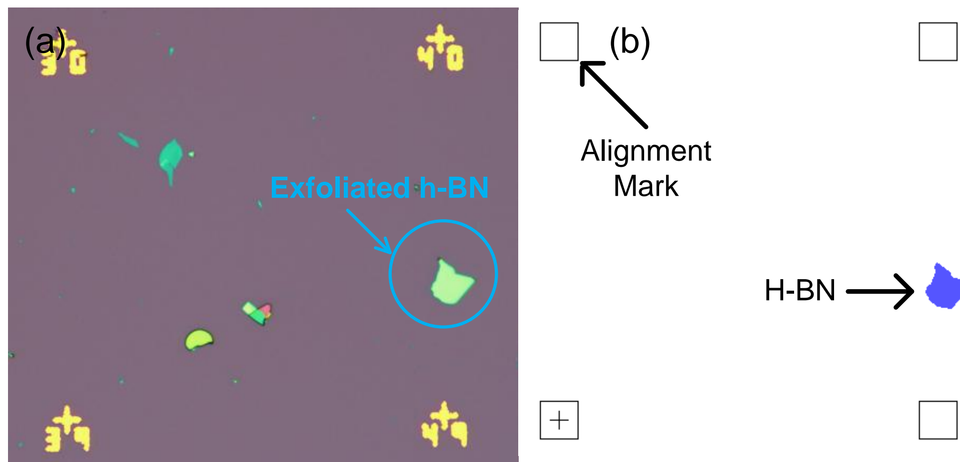

Figure A.3. Digitizing locations for h-BN films. (a) Optical image of an exfoliated h-BN film, (b) Designed layout. h-BN is drawn as a polygon.

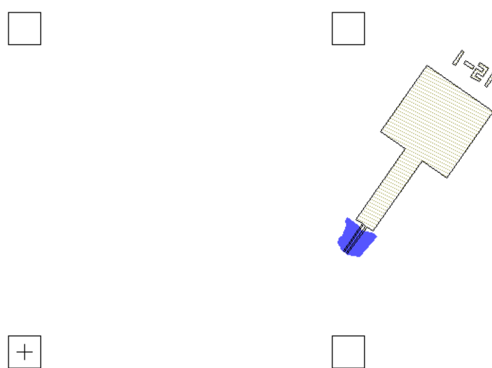

Figure A.4. Define embedded gate patterns on exfoliated h-BN films.

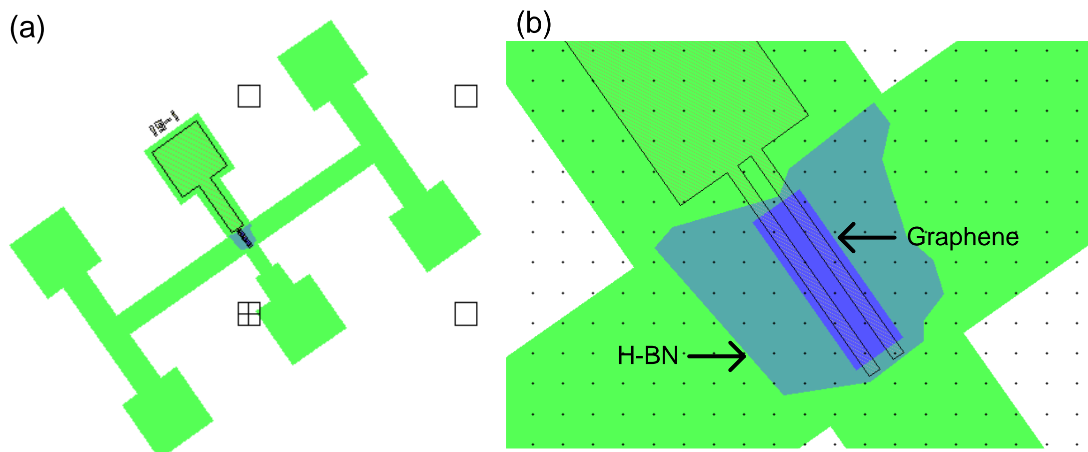

Figure A.5. Define graphene active layers (a) Designed layout, (b) Zoom-in picture of the channel area highlighting graphene channel and an h-BN dielectric film

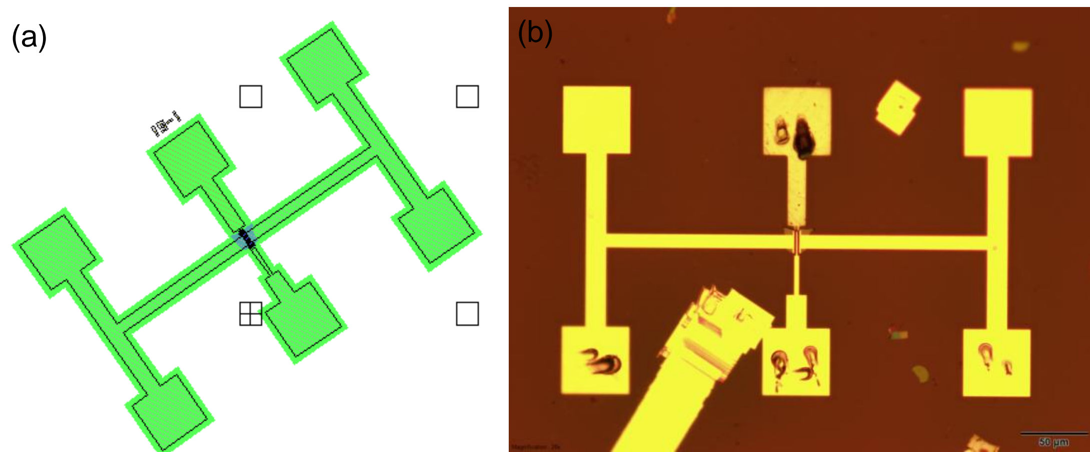

Figure A.6. Complete device structure with h-BN dielectric films. (a) Designed layout for the entire device structure including source/drain electrodes, (b) Optical image captured after the liftoff of source/drain (Ti/Au) electrodes

A.5. Low Power Plasma Enhanced Chemical Vapor Deposition of Si_3N_4

Step	Details
1	Equipment : Plasmatherm 790 Deposition temperature : 250 °C Place samples on a silicon carrier wafer Load samples with a carrier wafer at the center of the chamber
2	Pump (pressure : 20 mTorr, hold time : 10 sec)
3	Purge (pressure : 300 mTorr, hold time : 30 sec)
4	Evacuation (pressure : 20 mTorr, hold time : 2 min)
5	Purge (pressure : 300 mTorr, hold time : 30 sec)
6	Evacuation (pressure : 20 mTorr, hold time : 2 min)
7	Process step 1 NH_3 flow rate : 10 sccm, SiH_4 flow rate : 50 sccm, H_2 flow rate : 5 sccm, pressure : 500 mTorr, no RF power applied, hold time : 45 sec (fixed)
8*	Process step 2 NH_3 flow rate : 10 sccm, SiH_4 flow rate : 50 sccm, H_2 flow rate : 5 sccm, pressure : 500 mTorr, RF power : 10 W, hold time : variable
9	Evacuation (pressure : 10 mTorr, hold time : 30 sec)
10	Purge (pressure : 200 mTorr, hold time : 30 sec)
11	Evacuation (pressure : 10 mTorr, hold time : 30 sec)

* Si_3N_4 deposition rate is 53 A/min.

A.6. Selective Dry Etch of Plasma Enhanced Chemical Vapor Deposited Si_3N_4

Step	Details
1	Equipment : Plasmatherm 790 Place samples on a silicon carrier wafer Load samples with a carrier wafer at the center of the chamber
2	Pump (pressure : 100 mTorr, hold time : 10 sec)
3	Evacuation (pressure : 40 mTorr, hold time : 1 min)
4	Purge (pressure : 200 mTorr, hold time : 30 sec)
5	Evacuation (pressure : 40 mTorr, hold time : 30 sec)
6	Process step 1 Ar flow rate : 20 sccm, CF_4 flow rate : 50 sccm, pressure : 80 mTorr, no RF power applied, hold time : 1 min (fixed)
7*	Process step 2 Ar flow rate : 20 sccm, CF_4 flow rate : 50 sccm, pressure : 80 mTorr, RF 100 W, hold time : variable
8	Evacuation (pressure : 40 mTorr, hold time : 1 min)
9	Purge (pressure : 200 mTorr, hold time : 30 sec)
10	Evacuation (pressure : 40 mTorr, hold time : 1 min)

* The etch rate for Si_3N_4 is 114 nm/min.

* 950 PMMA A4 is used as a mask. The etch rate for PMMA is 88 nm/min.

(selectivity of PMMA:Si_3N_4 = 1:1.29)

A.7. Multi-Finger Embedded-Gate Graphene Field Effect Transistor (MEGFET)

Step	Details
1	Prepare double-side coated polyimide substrates (see A.1 for details)
2	Spin-coat PMMA A4 and ESpacer on polyimide substrates (see A.4 step-21)
3	E-beam lithography of alignment marks Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 μC/cm^2 - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
4	Ti/Au(2nm/50nm) deposition using e-beam evaporation for alignment marks
5	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water for 1min each
6	Spin-coat PMMA A4 and ESpacer on polyimide substrates (see A.4 step-21)
7	E-beam lithography of gate patterns Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 μC/cm^2 - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
8	Ti/Pd (2nm/40nm) deposition using e-beam evaporation for gate patterns
9	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water for 1min each
10	Atomic layer deposition of Al_2O_3

	- Deposition rate : 0.92 A/cycle at 250 °C - Cycles : 100 cycles
11	Spin-coat PMMA A4 and ESpacer on polyimide substrates (see A.4 step-21)
12	E-beam lithography of gate-dielectric patterns Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 μC/cm^2 - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
13	Wet-etch ALD Al_2O_3 - Use a 1:3 mixed solution of H3PO4 : DI water - Etch rate : 0.3 nm/min - Etch patterned samples for > 35min - Rinse samples with Acetone for 10min - Rinse samples with IPA for 2min - Rinse samples with DI water for 2min
14	Wet-transfer of graphene films onto prepared substrates (see A.2 for details)
15	Spin-coat PMMA A4 and ESpacer on polyimide substrates (see A.4 step-21)
16	E-beam lithography of graphene channels Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 μC/cm^2 - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
17	Oxygen plasma etch of graphene channels (see A.3 for details)
18	Spin-coat PMMA A4 and ESpacer on polyimide substrates

	(see A.4 step-21)
19	E-beam lithography of source/drain electrodes Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 $\mu C/cm^2$ - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
20	Ti/Au (2nm/50nm) deposition using e-beam evaporation for source/drain
21	Liftoff of deposited metal films - Leave samples in Acetone for 1 hour and then rinse with IPA and DI water for 1min each
22	Deposit a passivation layer of 30nm-thick PECVD Si_3N_4 - Deposition rate : 5.3 nm/min - Deposition time : 6 min (see A.5 for details)
23	E-beam lithography of a Si_3N_4 passivation layer Equipment : JEOL-6000 FSE - Expose the desired patterns with a 50 kV electron beam at 500 $\mu C/cm^2$ - Develop the pattern for 1min in 1:3 mixture of MIBK and isopropanol
24	Dry-etch PECVD Si_3N_4 passivation layer - Etch rate : 114 nm/min - Etch time : 20 sec (see A.6 for details) - Rinse samples with Acetone for 10 min - Rinse samples with IPA for 2 min

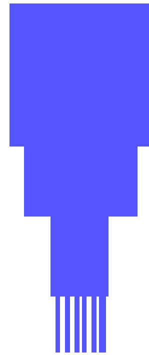

Figure A.7. Mask1 for Multi-finger Embedded-gate Graphene Field-Effect Transistors to define gate fingers.

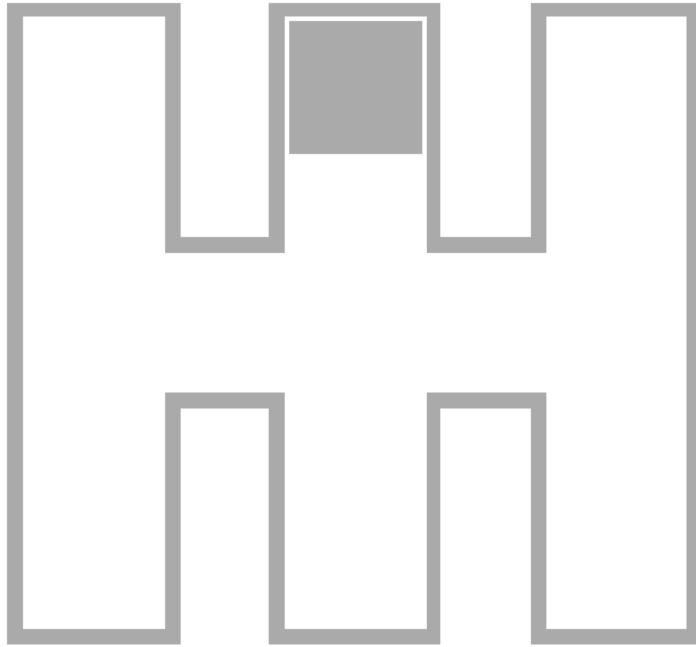

Figure A.8. Mask2 for Multi-finger Embedded-gate Graphene Field-Effect Transistors to define ALD gate oxides.

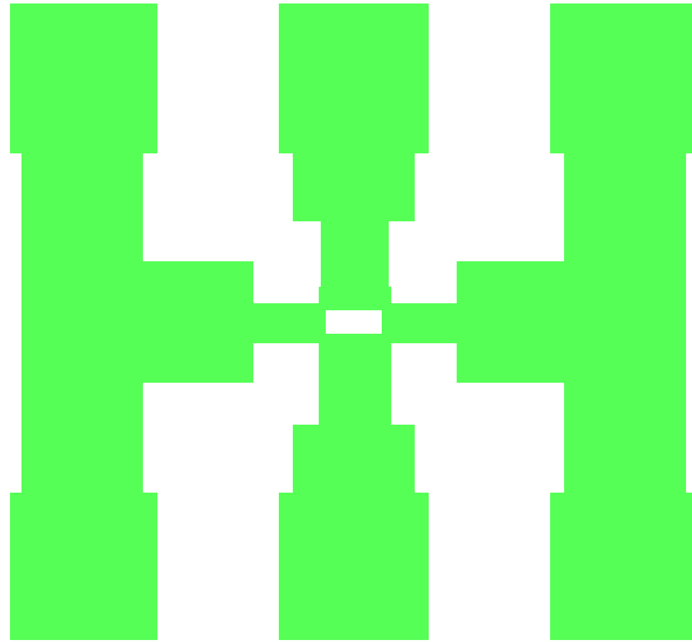

Figure A.9. Mask3 for Multi-finger Embedded-gate Graphene Field-Effect Transistors to define graphene active areas.

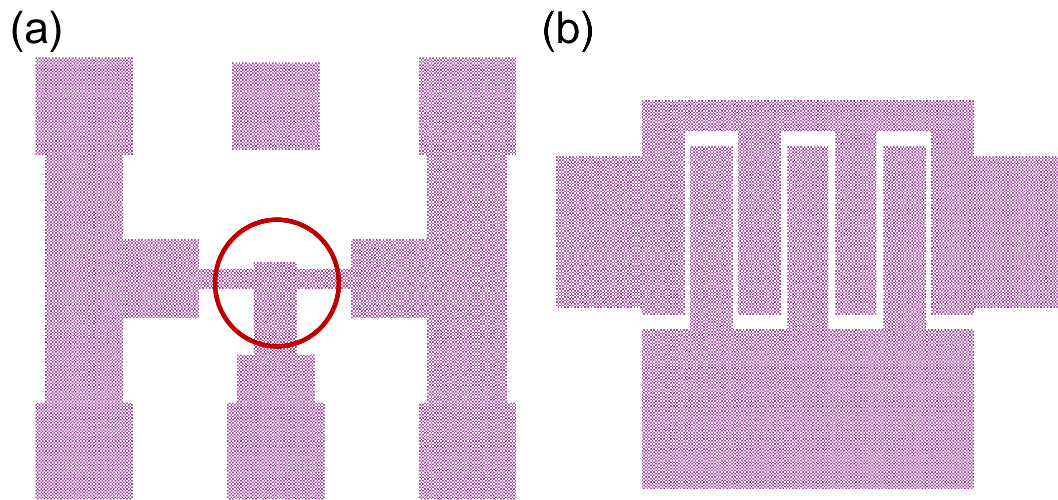

Figure A.10. (a) Mask4 for Multi-finger Embedded-gate Graphene Field-Effect Transistors to define source and drain electrodes. (b) Zoom-in picture over the channel area highlighted in red in (a).

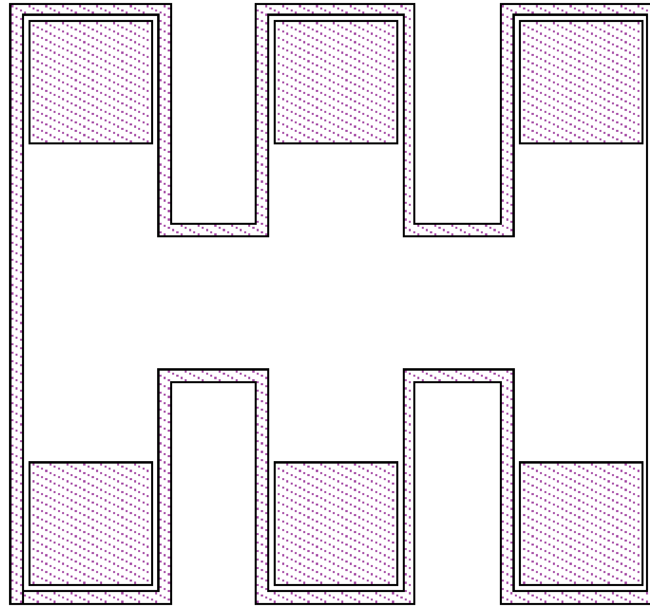

Figure A.11. Mask5 for Multi-finger Embedded-gate Graphene Field-Effect Transistors to define the silicon nitride passivation layer.

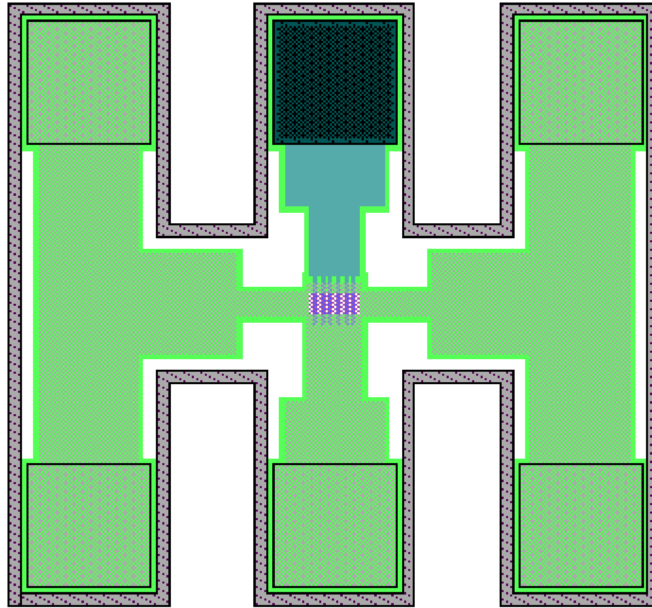

Figure A.12. Combined Layouts for Multi-finger Embedded-gate Graphene Field-Effect Transistors.

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