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Cost Effective High Efficiency Solar Cells

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Cost Effective High Efficiency Solar Cells

by

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Dedication

To my mother

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Cost Effective High Efficiency Solar Cells

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To make solar energy mainstream, lower-cost and more efficient power generation is key. A lot of effort in the silicon photovoltaic industry has gone into using fewer raw materials (i.e., silicon) and using more inexpensive processing techniques and materials to reduce cost.

Utilizing thinner substrates not only reduces cost, but improves cell efficiency provided both front and back surfaces are well-passivated. In the current work, a kerf-less process is developed in which ultra-thin (~25 μm), flexible mono-crystalline silicon substrates can be obtained through an exfoliation technique from a thicker parent wafer. These substrates, when exfoliated, have thick metal backing which provides mechanical support to the thin silicon and enables ease of processing of the substrates for device fabrication. Optical, electrical, and reliability characterization studies for completed cells show this technology's compatibility with a heterojunction solar cell process flow.

Building on the promising results achieved on exfoliated substrates, further optimization work was carried out. Namely, an improved cleaning process was developed to remove front surface contamination on textured surfaces of exfoliated, flexible mono-crystalline silicon. This process is very effective at cleaning metallic and organic residues, without introducing additional contamination or degrading the supporting back

metal used for ultra-thin substrate handling. Spectroscopic studies were performed to qualitatively and quantitatively understand the efficacy of different cleaning procedures in order to develop the new cleaning process. Results of the spectroscopic studies were further supported by comparing the electrical performance of cells fabricated with different cleans.

To replace silver as contact metal with a cheaper substitute like nickel or copper, patterning and etching processes are generally used. A low-cost alternative is proposed, where a reusable shadow mask with a metal grid pattern is kept in contact with the surface of the substrate in a plasma-enhanced chemical vapor deposition chamber during silicon nitride deposition. This leaves a patterned silicon surface for selective metal growth by direct electro-deposition. The viability of this process flow is demonstrated by fabricating diffused junction n^+pp^+ monofacial and bifacial cells and electrically characterizing them. Investigation of the factors limiting the efficiency of the cells was carried out by lifetime measurement experiments.

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Chapter 1: Introduction

1.1 CHALLENGES IN MODERN SOLAR INDUSTRY

The most common energy resource in the world for generating electricity is based on fossil fuel, which comes from coal, natural gas and oil. It is a forgone conclusion that such resources are limited [1] and eventually we would have to completely depend on alternative resources. One such potential resource is renewable energy such as solar, wind, geothermal, hydropower, etc. There is an even more urgent need right now to move towards renewable energy. This is to counteract climate change due to greenhouse gas effect. Use of renewable energy reduces carbon emission caused by use of fossil fuels [2]. Among renewables photovoltaics (PV) or solar energy as a viable alternative source of energy have been touted since the 1970s [3].

Solar power offers a number of benefits compared to fossil fuel or other renewable resources:

1) Solar energy is available almost everywhere in the world.
2) There is no fuel cost associated with PV. Operation and Maintenance (O & M) cost is relatively low.
3) PV energy generation varies over the year. However, the peak energy demand in the summer coincides with the peak electricity generation.
4) What makes PV truly stand out from other renewable energy options is perhaps that it is the only renewable source of power generation that could be installed with a relative ease on a roof of a house, residential or otherwise. The

electricity generated is of more value at the point of use than it is generated at a remote place from which it is supplied.

Solar energy needs to be low-cost to be competitive to conventional fossil fuel based large scale electricity generators. The metric $\$/W_p$ is usually used to compare the capital costs of various forms of electricity generation. It is calculated by using the total capital cost required to generate 1 Watt of peak power (W_p) on an average. In that respect coal is still much more cheap than solar [4]. $\$/W_p$ need to be brought down significantly for solar to be more mainstream rather than niche. There are two obvious ways to bring down $\$/W_p$: increase efficiency and reduce cost. Fabricating high efficiency solar cells, reducing cost by using less or cheaper raw material and reducing process complexity have been focus of research for the past four decades. Because of that solar cell technology has evolved over the years. It can be classified into three generations, depending on the basic material used and commercial maturity.

- **1st Generation:** Based on mostly crystalline silicon (c-Si), including single, multi-crystalline and poly-crystalline. This currently is the most mature technology and fully commercialized. This generation of cells are of high efficiency. However, it is also somewhat expensive, mostly because of the material and processing cost.
- **2nd Generation:** Based on thin films such as amorphous silicon (a-Si), Cadmium Telluride (CdTe), Copper Indium Selenide (CIS) and Copper Indium Gallium Diselenide (CIGS). This is a still evolving technology but

already commercialized. These are significantly cheaper to produce but have much lower module efficiencies.

- **3rd Generation:** Based on concentrator PV (CPV), organic PV (OPV), dye sensitized PV (DSSC) which are either still in the demonstration phase or do not have wide enough market bases. Additionally some advanced concepts such as tandem cells, quantum dots, perovskite solar cells are still in the research phase. These are traditionally not large area cells, and so far have found applications in only niche areas. Some of these advanced concept cells lead to very high efficiency cells, but the manufacturing costs are significantly higher than the 1st generation cells. Other types of cells are very cheap to manufacture but have shown even lower efficiencies than 2nd generation solar cells.

Table 1.1 shows range of efficiency on large area (meter square) module conversion efficiencies of different generation of technologies. This data is from a survey taken in 2012 [5] based on entire spectrum of modules available in the market and does not reflect the best in class module efficiency numbers.

Generation	Technology	Efficiency Range (%)
I	Single crystalline Si	15-19
	Multi-crystalline Si	13-15
	Poly-crystalline Si	5-8
II	CIGS	7-11
	CdTe	8-11
III	CPV	25-30
	OPV	1
	DSCC	1-5

Table 1.1: Efficiency range for solar cells from different generations and different technologies [5].

Back in 2007 it was predicted that the 3rd generation solar cells were going to be extremely efficient but as cheap to produce as thin film devices in the 2nd Generation technologies [6]. Figure 1.1 shows the projections for efficiency versus cost for three generations of solar cells. The inset figure shows real cost in 2012 for 1st and 2nd Generation cells. The first two generations of PV are still so cost competitive that they match the best projections for 3rd Generation technologies [7]. Moreover, c-Si based technology still accounts for more than 80% of the current market share [8].

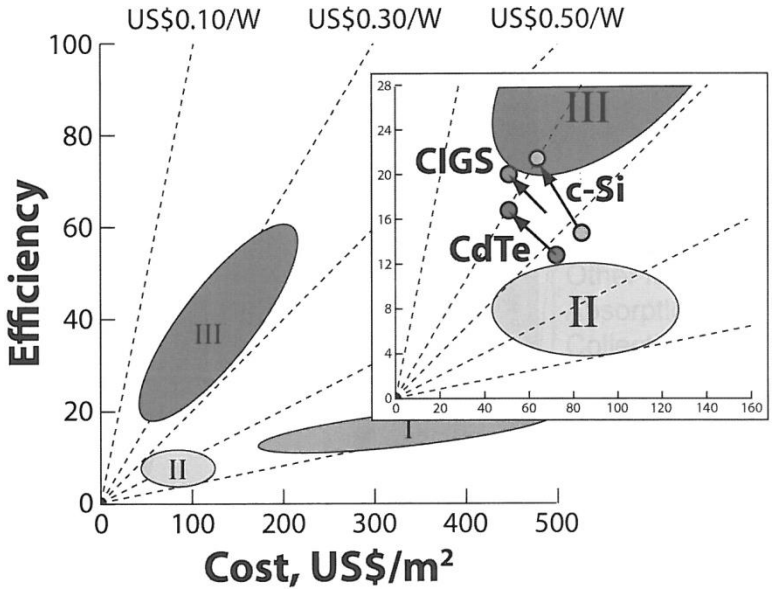


Figure 1.1: Efficiency versus cost for the three generations of solar cells predicted back in 2007. The inset shows how the c-Si, CIGS, CdTe technologies are still cost competitive with 3rd Generation solar cells in 2012 [6], [7].

The importance of efficiency cannot be overstated with regards to reducing the $\$/W_p$ metric. That is the main reason why 1st Generation solar cells are still beating solar cells belonging to more advanced technologies. To emphasize this point Figure 1.2 shows the value chain starting at poly Si to going all the way to the system completion. The approximate costs for each of the steps in the link are shown in the figure. All of the steps leading up to making a complete solar cell are only about 40% of the total system cost. For 2nd Generation of solar cells that cost is relatively low. However, in order for 2nd Generation cells to make a real difference in $\$/W_p$ front, it has to be 40% or more efficient. In reality, thin film cells are much lower efficiency as shown in Table I. For this

reason 1st generation solar cells, especially single crystalline Si solar cells are still very much important in the area of research in the industry.

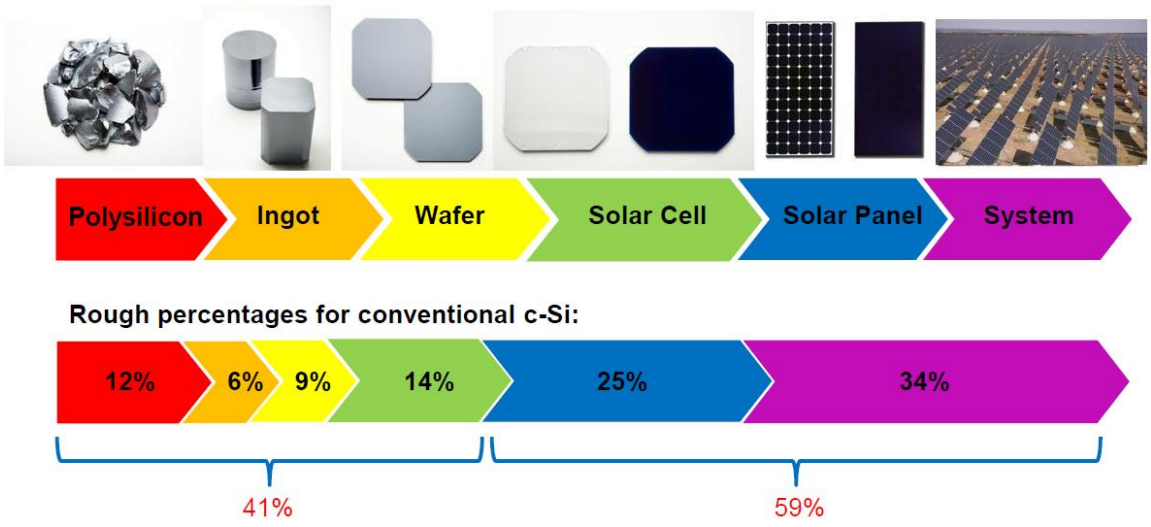


Figure 1.2: Conventional wafered Si value chain with percentage of total cost shown associated with each step [9].

1.2 THIN CRYSTALLINE SILICON SOLAR CELLS

The silicon (Si) photovoltaic industry has been pushing towards thinner substrates as the raw Si wafer cost accounts for over 40% of the final module cost. In addition, reducing the Si wafer thickness below 100μm can potentially improve cell efficiencies. This is largely due to the enhancement in the open circuit voltage (V_{OC}) of the cell in the

Auger recombination limited regime [10], [11]. Furthermore, reducing the Si wafer thickness minimizes bulk recombination in the cell. As a result, high cell efficiencies can be attained using wafers with low-to-moderate (~100μs or less) minority carrier lifetimes, provided the surfaces are well passivated and effective light trapping is implemented. Figure 1.3 shows the theoretical efficiency limit of an n-type silicon solar cell with ideal light trapping and different surface passivation with surface recombination velocities (cm/s) marked along calculated lines [12]. The gain in efficiency for thinner cells is only seen for surface recombination velocity <100 cm/s. According to the simulated graph, there exists a so called "Golden Decade" between 10 μm and 100 μm where with the most optimum surface passivation and light trapping one can reach close to the theoretical limit to the efficiency for a Si solar cell.

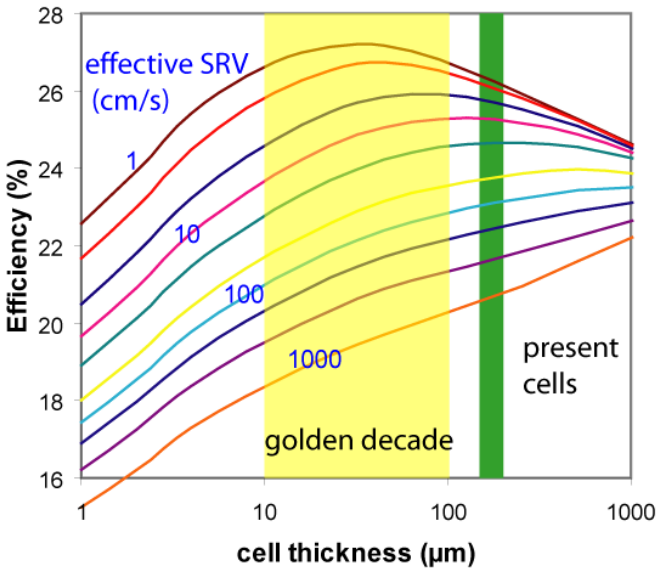


Figure 1.3: Efficiency versus cell thickness curves with different surface passivation, assuming perfect light trapping [12].

Therefore, thin crystalline silicon solar cells are of much interest due to their potentially high efficiency and low material cost. However, Si substrates with sub-100 μm thickness can easily break or mechanically crack with wafer handling, resulting in low yield in a solar cell manufacturing line. The solar industry does not currently have an economically viable solution to implement standard processes such as wet chemical cleaning, texturing, depositions and mechanical handling in general on such thin wafers. We have developed a kerf-less process in which ultra-thin (~25μm) and flexible mono-crystalline Si substrates can be obtained through an exfoliation technique from a thicker parent wafer [13]. These substrates, when exfoliated, have thick metal backing and are designated as Semiconductor On Metal (SOM®). The metal backing provides mechanical support to the thin Si and enables ease of processing of the SOM® substrates for semiconductor device fabrications. In Chapters 2, 3 and 4 exfoliation process, initial process development and further process optimization are respectively discussed.

1.3 REDUCING FABRICATION COMPLEXITY: ALTERNATIVE TO SCREEN PRINTING

One other way to reduce $\$/W_p$ is to use cheaper alternative materials. In order to do that processing complexity needs to be kept at the same level or if possible made even simpler. The number of lithography/alignment steps to define metal contact areas is one of the main causes for driving the cost up in any semiconductor manufacturing process. Specifically, in the c-Si solar cell industry where manufacturing cost containment is one of the key issues and typical metal electrode feature size is of the order of ~100μm or a

little less, lithography/alignment related steps are generally avoided. That is why commercially available low-cost bulk crystalline silicon solar cells, having efficiencies in 10%-15% range, have simple p-n diffused junctions with screen-printed front side contact on plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) and aluminum (Al) back surface field (BSF) on the rear side. Screen printing technique does not involve lithography but requires a certain level of alignment, a two-step process for applying metal on both surfaces of substrate, and co-firing at high temperature.

Though it is the most standard technique currently used, screen printing presents some challenges as the industry is moving towards thinner substrates. Preventing wafer breakage is an issue for thinner and more fragile Si as screen printing requires hard contact [14]. The rising cost of silver is another problem that calls for an electrically equivalent alternative, which is also cheaper. These pressing issues have led to a push towards an alternative approach [15]. In this approach, front surface SiN_x has been patterned and etched to expose doped Si underneath for the purpose of depositing/growing a different metal stack for ohmic contact. This metal stack is typically Nickel (Ni) or Copper (Cu) with Ni diffusion barrier. However, this approach adds process complexity in terms of either introducing photolithography or adding some other process related cost in the process flow. International Technology Roadmap for Photovoltaic (ITRPV) predicts that introduction of alternative metal stack to replace silver is not expected before year 2018 as shown in Figure 1.4 [16].

In chapter 5 we proposed a method which gets rid of both of those limitations by use of a lithography/alignment-less method for patterning contact holes, and a low

temperature metallization scheme used for both the front and rear surfaces to grow metal simultaneously.

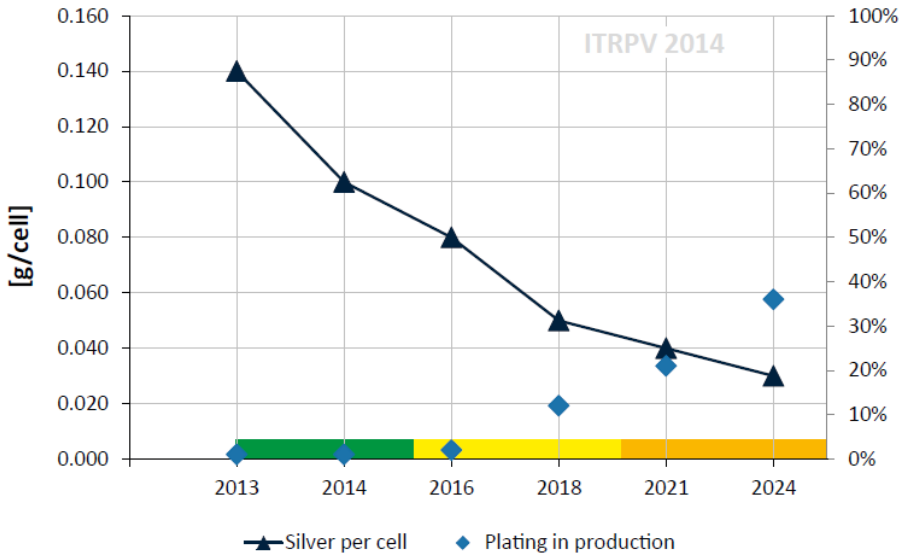


Figure 1.4: ITRPV prediction of trend in proportion of silver and introduction of new metal stack in cells in the next few years. Color coding of at the bottom of the graph depicts reduction in the share of silver in the future technology [17].

1.4 CHAPTER ORGANIZATION

This chapter provided an overview of the current photovoltaic technology landscape, as well as a discussion of some of the key challenges in cost reduction that are currently being researched. Moreover, the main two approaches i.e. thin crystalline Si solar cells and introducing new methods to form alternative metal stack to replace silver

as metal contact to reduce the $/$W_p$ metric, are discussed briefly. The remainder of this dissertation is divided into two parts, and is aimed at addressing some of the most pressing challenges to the implementation of both thin crystalline Si solar cells and alternative metal stack.

Chapters 2 to 4 include the first part of this work. In Chapter 2, the some of the prior work on thin crystalline Si substrates for solar cells and the challenges associated with them are discussed. Subsequently a novel exfoliation method to obtain ultra-thin (~25 μm) mono-crystalline and flexible substrate with metal backing for solar cell fabrication purpose is introduced in detail. Through quantitative and experimental analysis the stress and residual strain is measured on the exfoliated substrates. Based on that the temperature limit for cell processing and module integration was determined. A modification in the exfoliation process is introduced to improve back surface reflection.

In Chapter 3 initial development work is introduced on mono-crystalline silicon single heterojunction solar cells on flexible, ultra-thin (~25 μm) substrates. Optical and electrical measurements were carried out to demonstrate structural integrity process uniformity on these flexible substrates. Preliminary reliability test results are shown including thermal shock and highly accelerated stress test (HAST) are also shown to demonstrate compatibility of exfoliation technology for use in photovoltaic modules.

In Chapter 4 an improved cleaning process is developed to remove front surface contamination for single heterojunction solar cells on textured surfaces on ~25 μm thick exfoliated substrates. The process is very effective in cleaning metallic and organic residues, without introducing additional contamination or degrading the supporting back

metal used for ultrathin substrate handling. Quantitative analysis of the Auger electron spectra is shown to reduce potassium contamination significantly (~0.89% atomic). An open-circuit voltage enhancement of 22 mV and an absolute 1.5% increase in conversion efficiency are observed with the new cleaning procedure for the exfoliated thin solar cells.

Chapter 5 is the second part of the rest of the dissertation. A low-cost alternative silver screen printing process has been proposed in this chapter for patterning and metallization. In this approach a reusable shadow mask is used to form metal grid pattern during PECVD SiN_x deposition. The metal is then selectively grown on heavily doped Si surface using electrochemical deposition. The viability of this process flow is demonstrated by fabricating diffused junction n^+pp^+ monofacial and bifacial cells and electrically characterizing them.

Chapter 6 provides a summary of this work and discusses suggestions for future directions of this research.

Chapter 2: A Kerf-less Exfoliation Technique to Obtain Ultra-thin Monocrystalline Silicon Substrates for Solar Cell Applications [1]

2.1 THIN CRYSTALLINE SILICON SOLAR CELL TECHNOLOGIES

Thin crystalline silicon solar cells are of much interest due to their potentially high efficiency and low material cost. In addition, thin crystalline silicon solar cells are more apt to be used in bifacial cell architectures since the backside efficiency increases with decreasing cell thickness [18], [19]. There are ongoing efforts to produce ultra-thin wafers in a cost effective and manufacturable way and they can be broadly categorized into three different approaches. They are as follows.

- **Wafering Process:** Substrates are either obtained very thin using sawing technique or chemically thinned down thicker wafers. Either way, there is significant kerf-loss involved in this approach.
- **Lift-off or Layer Transfer Process:** This approach could be divided into two subdivisions. In the lift-off method a stressor layer is bonded with a thick parent wafer and made to go through thermal cycling. The coefficient of thermal expansion (CTE) mismatch causes strain in the bi-layer to cause lift-off of a thin substrate with the aid of the stressor layer. Layer transfer

[1] Certain parts of this chapter are reproduced from the following two conference articles. All the authors contributed to either experimental or technical or both the aspects.
1) D. Jawarani, D. Xu, S. Smith, R. A. Rao, L. Mathew, **S. Saha**, S. Banerjee, and P. S. Ho, "Integration and Reliability of Ultra Thin Silicon Solar Cells and Modules Fabricated using SOM Technology," in *38th Photovoltaic Specialist Conference*, pp. 1–4, Austin, 2012.
2) D. Xu, P. S. Ho, R. a. Rao, L. Mathew, S. Smith, **S. Saha**, D. Sarkar, C. Vass, and D. Jawarani, "Mechanical strength and reliability of a novel thin monocrystalline silicon solar cell," in *IEEE International Reliability Physics Symposium (IRPS)*, pp. 4A.3.1–4A.3.7, Anaheim, 2012.

technology employs different method but it has the similar appearances as lift-off approach. In the layer transfer method absorber layers are grown on a reusable substrate using chemical vapor deposition (CVD) and cells are completed. Afterward using laser scribing or chemical etching the cells lifted off from the dummy substrate.

- **Wafer Equivalent Process:** In this approach the cell is fabricated by growing the thin layers of BSF, absorber, and emitter on an inexpensive highly doped Si wafer using CVD or hot wire CVD (HWCVD) technique.

A summary of thin silicon technology is shown in Table 2.1. The first two approaches do not address the issue of handling. Once the thin wafers are obtained they could give rise to yield or breakage related issues while processing. Additionally, the layer transfer method is also cost prohibitive due to the use of CVD technique requiring ultra-high vacuum (UHV). The third approach is simply cost prohibitive because it requires UHV techniques such as CVD and HWCVD. They also require a handling wafer to grow the thin films on.

Method	Institute/organization	Substrate thickness (μm)	Details
Wafering process (with kerf-loss)	UNSW [20]	47	Wafer chemical thinning
	Applied Materials [21]	~100	Sawing
Lift-off/layer transfer technology (kerf-less)	IMEC [22],	~20	Resin, Solvent, paste (deposit, bond) + Anneal + Cleave
	SiGen [23]	20-50	Implant+Bond+Anneal+ Cleave
	ISFH [24], IPE [25] (Germany)	~45	Porous Silicon + Epitaxial(Growth)+ Bond + Cleave
Wafer equivalent approach	Fraunhofer ISE [26], IMEC [27]	20-50	CVD growth
	NREL [28]	2	HWCVD growth

Table 2.1: The three main approaches in thin silicon technology for solar cells. The color coding is shown to indicate the inadequacy in each approach.

The benefits of thin crystalline Si solar cells are exciting with respect to the significant material cost reduction and potentially higher converting efficiency. However, there are significant challenges to commercialize this type of solar cells due to the difficult mechanical handling and reliability issues. While thick Si substrates do not require a mechanical support, it becomes necessary to add a supporting substrate for thin crystalline films to improve the handling and yield during wafer transfer, cell process and module integration. For example, assuming a vacuum chuck is used during wafer transfer, the resulting maximum mechanical stress in the silicon wafer can be expressed as $\sigma \propto \frac{p}{h^2}$ where p is the pressure difference between the atmosphere and the vacuum and h represents the wafer thickness. When h is reduced to a fraction of the standard cell thickness (180~200 μm), the corresponding stress may increase by more than one order of magnitude, making it necessary to use a supporting substrate. Since silicon solar cells are fabricated at an elevated temperature, the resulting thermal stress due to the difference in the CTE between silicon and the supporting substrate material determines the allowable temperature limit for cell processing and module integration. A prediction from ITRPV of trend in mass-produced thin as-cut wafers is shown in Figure 2.1. It also shows the cell thickness limits of current module technologies. Due to the price of Si feedstock saturating, pressure to use thinner substrates will likely be back again by 2017-2018 [29]. However, the red marking at the bottom of the graph covering the years beyond 2019 for sub-100 μm Si thickness means that the industry still doesn't have solution for handling, thermal budget, warping yield loss related issues.

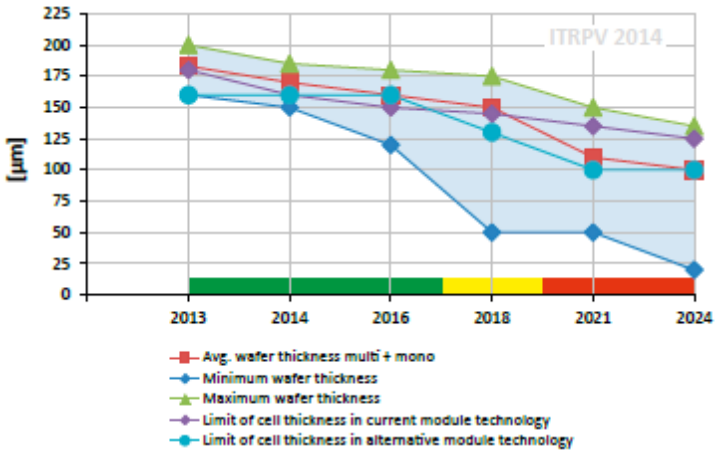


Figure 2.1: ITRPV prediction of trend in minimum as-cut thickness in mass production of solar cells and minimum cell thickness in module manufacturing [17].

Since thin Si needs a handling substrate or layer, the maximum temperature that the silicon-substrate bilayer structure can sustain has to be carefully evaluated prior to fabrication. It is worth noting that the resulting bow and fracture issues from the thermal residual stress due to the CTE mismatch between front silicon solar cells and rear aluminum paste layer is already a problem for solar cells at current thickness of ~200 µm [30], [31]. Furthermore, the state-of-the-art silicon solar cells are textured on the front surface with pyramid structures to improve light-trapping in the devices [32], [33]. These pyramids can behave as initial crack sources under thermal stresses to break the thin crystalline silicon film at high temperature. Such fracture-related reliability issues are more sensitive during the fabrication of thin crystalline silicon solar cells.

2.2 A KERF-LESS EXFOLIATION TECHNIQUE TO OBTAIN ULTRA-THIN SILICON: SOM® TECHNOLOGY

In our approach a patented technology called SOM® (Semiconductor on Metal) is developed at Microelectronic Research Center with an objective to manufacture ultra-thin monocrystalline silicon solar cells [13]. The resulting SOM® substrate is composed of ~25 μm thin monocrystalline silicon and a supporting metal foil which also behaves as the rear contact layer in cell architectures. These substrates could further be processed due to their mechanical robustness without handling issues. They are flexible and sturdier than regular Si substrates of < 200 μm thickness.

This approach involves forming a thick but flexible metal foil over a silicon substrate using an electrochemical deposition process. This is done by first depositing a thin seed layer of metal stack on a contamination free clean thick wafer surface. This deposition is done using electron beam evaporation. Other techniques such as, sputtering could also be used to form the seed layer. The wafer could have a thickness 200 μm and above. Since the seed layer is used to facilitate electroplating of Nickel (Ni), the top layer of the metal stack is kept as Ni. The adhesion to Si surface for Ni is fairly poor. To promote better adhesion a layer of Titanium (Ti) is deposited first. Ti is not only the adhesion layer but also could potentially be the diffusion barrier for Ni during the subsequent processing. The thickness for Ti and Ni in the metal stack is 20 nm each.

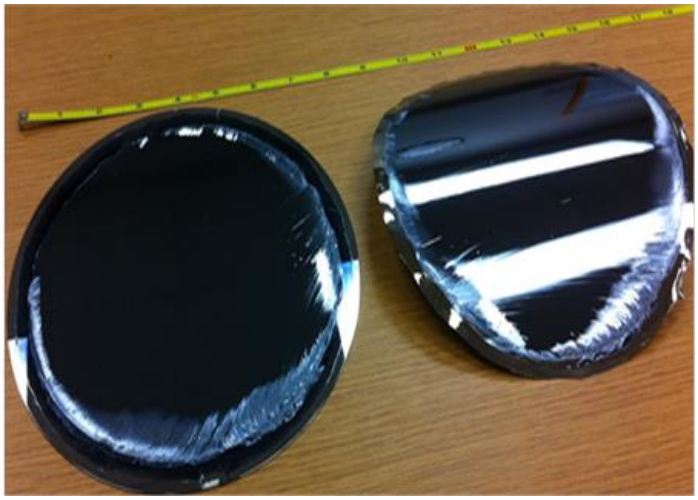
After seed layer deposition the wafer is used as a cathode in an electroplating system. The contact to the seed layer is usually made with the help of silver paste which cures at room temperature. The lead for the cathode is connected to the silver contact.

Electroplating is done in a bath using a Nickel Sulfamate based chemistry called Technisol® Ni 2420 C. Since the same plating bath is used during the entire time of electro-deposition, initially a very thin (~1-2 μm) layer of Ni is plated at a low current. Typically a "strike" or a high current, low ion concentration deposition would be performed in order to get high quality film with good adherence to the substrate. The low current thin layer deposition was done instead in this case, with the same effect. This serves as a foundation for subsequent plating processes. The process is slow, so a more efficient plating process can be used once the desired thickness is obtained. The current afterwards is ramped up slowly to avoid Joule heating and burning the metal. Once the current reaches the target value, electroplating is carried out until a thickness of ~50-55 μm is obtained. The target value of current is dependent on the area of the cathode.

After the electroplating is completed, we have a thick Si wafer bonded to a thick electroplated Ni foil. Subsequently an annealing process is performed at a temperature range between 230° C to 270° C, and the silicon substrate is in compression at the end of the annealing process due to the compressive plastic residual strain developed in the metal foil during annealing. This compressive strain is the key reason for exfoliation. This is further aided and controlled by a motor controlled mechanical wedge which applies mechanical force at a predetermined location on the wafer, leading to fracture along a sub-surface plane of the substrate. The thickness of the exfoliated Si has been statistically observed to vary within ±10% of the target thickness (~25 μm) in a large area (> 4 inch square) substrate. Figure 2.2 summarizes the process flow used for exfoliation method. Figure 2.3 (a) shows an 8 inch exfoliated substrate from a parent 8 inch round

wafer. The exfoliated round substrate can be laser cut into a pseudo-square shape (Figure 2.3 (b)). A typical commodity solar cell has similar pseudo-square shape. Exfoliated substrates have an inherent curvature as evident by the Figure 2.3.

Figure 2.2: Schematic of the exfoliation process flow.



(a)

(**Figure 2.3** continued next page)

(b)

Figure 2.3: (a) 8 inch exfoliated parent wafer and exfoliated flexible substrate. (b) 6 inch pseudo-square exfoliated substrate, laser cut from the 8 inch exfoliated substrate.

2.3 EXPERIMENTAL RESULTS ON STRESS IN THE BILAYER SUBSTRATE BEFORE EXFOLIATION

In order to better understand the change in stress that aides exfoliation processes, some quantitative and experimental analysis was carried out. Fig. 2.4 shows a schematic of the change in thermal stress during the electroplating and subsequent thermal cycling process. In order to measure the thermal stress bending beam technique was used [34]. The bending beam system employs an optical method to monitor the curvature of the bilayer material with respect to temperature. A schematic setup of the bending beam system is shown in Figure 2.5. The whole system consists of a laser-positioning module, a thermal cycling vacuum chamber, and a controlling computer. Stress is calculated by

measuring the bending in the sample using the laser system during thermal cycling. Figure 2.6 shows the variation of stress in the metal layer with temperature during an annealing cycle from a bending beam test and the onset of the compressive plastic deformation. This plastic deformation gives rise to the residual strain in the bilayer material. This residual stress is what aides in exfoliation process.

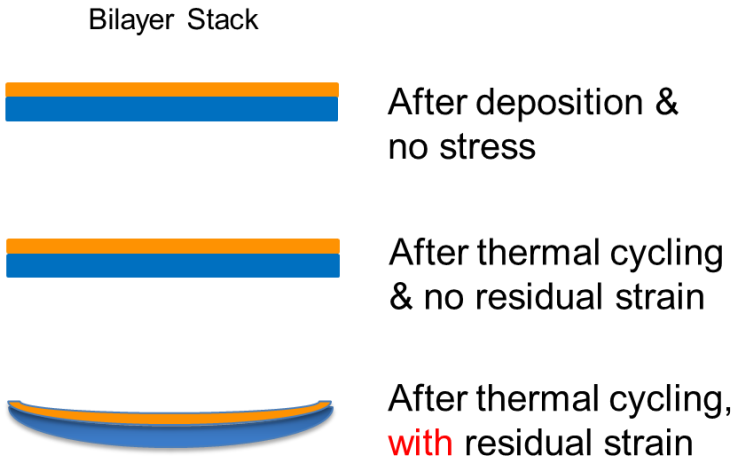


Figure 2.4: Changes in stress in the bilayer substrate before exfoliation.

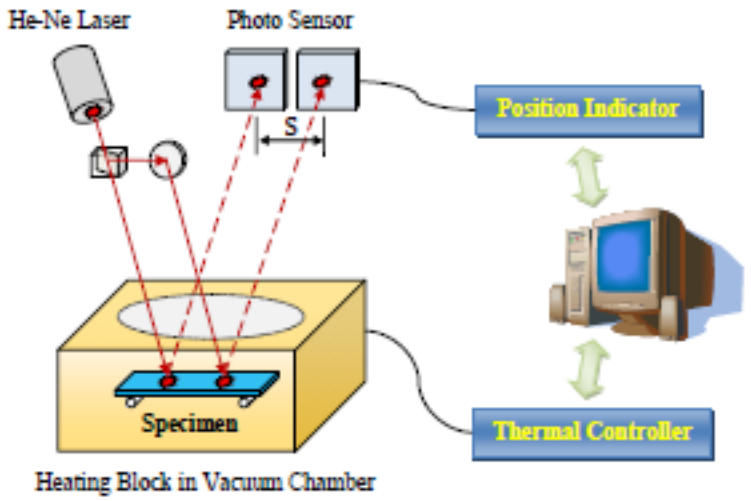


Figure 2.5: Schematic of the bending beam setup [35].

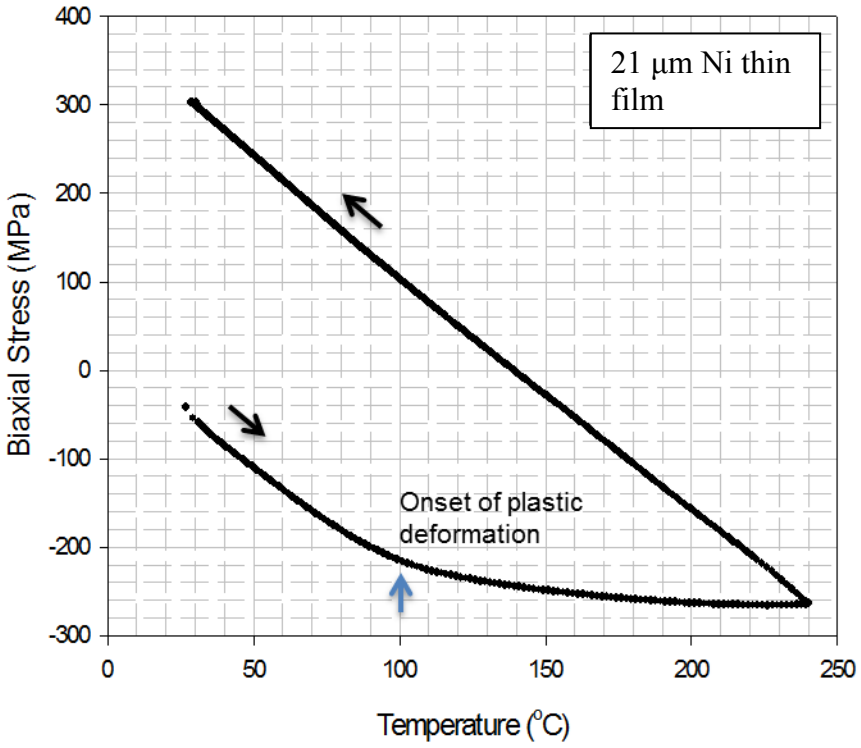
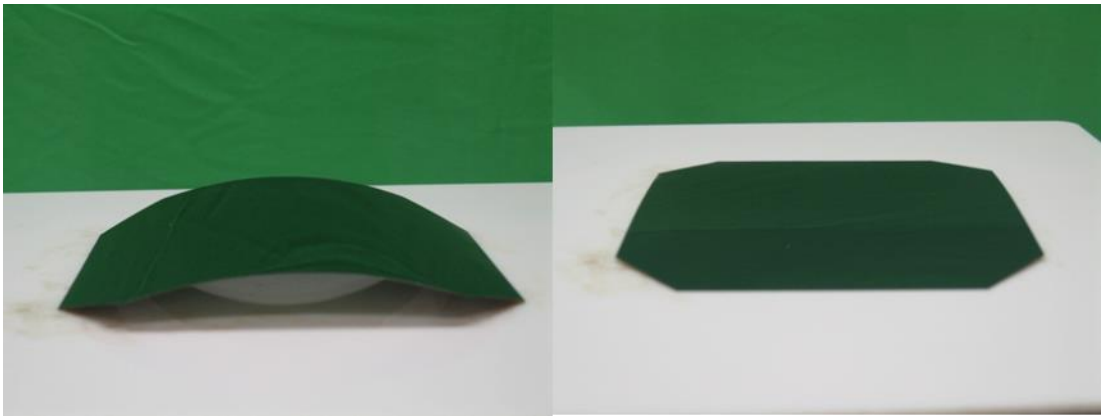


Figure 2.6: The variation of thermal stress in metal layer with annealing temperature as measured by bending beam technique [36].

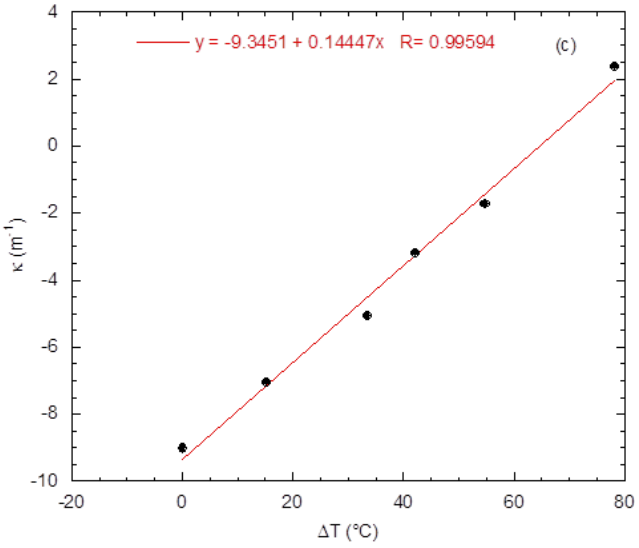
2.4 EXPERIMENTAL RESULTS ON RESIDUAL STRESS IN THE BILAYER SUBSTRATE BEFORE EXFOLIATION

The inherent curvature of the SOM® substrates is investigated. Figure 2.6 (a) show pictures of the exfoliated bilayer substrate at room temperature 22°C on a hot plate and Figure 2.6 (b) shows the corresponding picture when the foil becomes flat at ~85 °C. Figure 2.6 (c) shows the variation of measured curvature with the temperature differential ΔT and corresponding linear curve-fit. From the curve-fit, the temperature differential at zero curvature is $\Delta T_0 = 64.7^{\circ}\ C$ (the intercept of the ΔT -axis) and residual strain $\varepsilon_0 = 6.98\times10^{-4}$. The corresponding slope of 0.144 m^{-1} from curve-fitting is close to the theoretical prediction [37].



(a) (b)

(**Figure 2.7** continued next page)



(c)

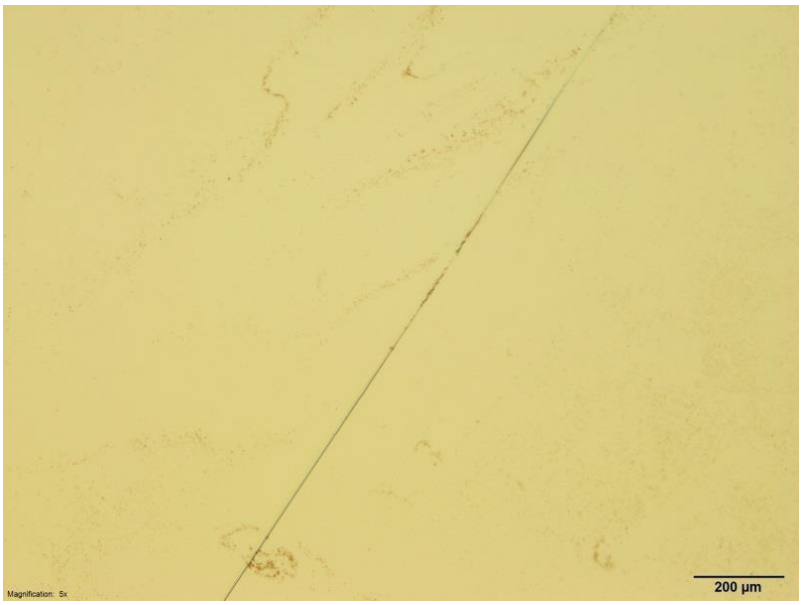
Figure 2.7: Pictures of the composite foil on a hot plate at room temperature 22° C (a) and ~85° C (b), (c) The variation of measured curvature with the temperature differential ΔT and corresponding linear curve-fit. Each data is the average of three measurements [37].

2.5 CRITICAL PROCESSING TEMPERATURE LIMIT

For the thin crystalline silicon backed by a metal layer, due to the CTE mismatch between silicon and metal, tensile stresses at high temperatures can develop. Under these stresses, cracks can propagate and run through the entire silicon layer, especially when the silicon surface is textured. Furthermore, de-bonding at the interface between the silicon layer and metal substrate can also occur at high temperatures. The high temperature limit that the SOM® bi-material composite foil can endure without reliability

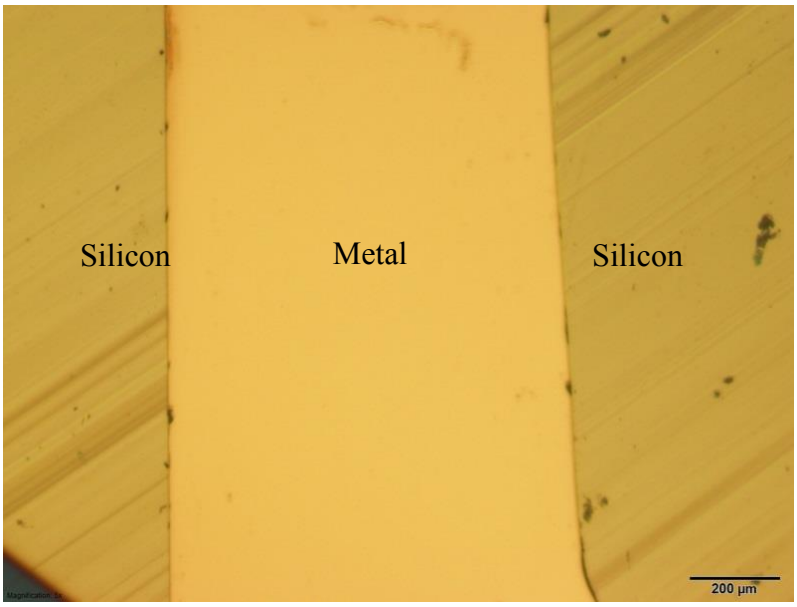
issues, such as breakage in silicon film or de-bonding at the interface, has to be determined in order to choose appropriate cell processing strategy and recipes.

Figure 2.8 (a) shows a crack resulting from a temperature field which runs through a SOM® silicon film. This is a view from the interface side of the silicon film (the metal substrate was etched away) due to the low reflectivity of the textured surface. The other failure mode is the interfacial de-bonding between the silicon film and the supporting substrate. Figure 2.8 (b) shows an example from interfacial de-bonding; a strip of silicon initiated from the edge of the SOM® foil and de-bonded from the metal substrate.



(a)

(**Figure 2.8** continued next page)



(b)

Figure 2.8: Optical images showing the failure modes of the SOM® silicon film resulting from temperature field: (a) a crack run through the silicon film and (b) a narrow strip of silicon film de-bonded from the metal substrate [37].

A detailed analytical study was done in [37] to find the processing temperature limit to avoid crack propagation and breakage in silicon film to be ΔT_K = 310º C. The temperature limit to prevent interfacial de-bonding was calculated to be ΔT_G = 240º C. The maximum allowable process temperature differential $\Delta T_{\max}$ is the lesser of ΔT_K and ΔT_G , i.e., $\Delta T_{\max} = \min(\Delta T_K, \Delta T_G) = 240$ °C or the highest process temperature $T_{\max}$ = 262°C.

2.6 MODIFICATION OF THE SEED METAL LAYER STACK TO ENHANCE BACK SURFACE REFLECTION

A metal stack of Ti and Ni was used at the initial phase of the exfoliation technology development. This seed layer also acts in the capacity of a back surface reflector (BSR) to reflect the long wavelength light to facilitate more effective absorption. To fabricate a solar cell using this method, typically a dielectric such as SiN_x is used to passivate the most of the back surface. A combination of dielectric and the metal stack is typically employed as BSR. However, Ti is generally a poor reflector as compared to Aluminum (Al) and Silver (Ag) used in the PV industry. That is why a 20 nm of Al is introduced before depositing Ti/Ni stack. It was found that this change in metal stack does not hinder exfoliation process in any way.

With additional metal enhanced BSR, further improvement in light trapping can be expected. Therefore the new metal stack is compared with the old metal stack and dielectric/metal stack in Figure 2.9. All three of the foils do not have any front or rear surface texture, or front ARC. The rise in reflectance in the long wavelength region (950-1100nm) in the graph is due to the fact that longer wavelength light gets reflected from the rear surface and is coupled out of Si substrate through the front surface. The reflectance curve for the exfoliated substrate with the new metal stack is found to be more closely following that of the dielectric/old metal stack. Higher reflectance in the 950-1120nm region in the Figure 2.9 is an indication of better back surface reflectance. Therefore, we can conclude that the new metal stack by itself is a better BSR than the old metal stack.

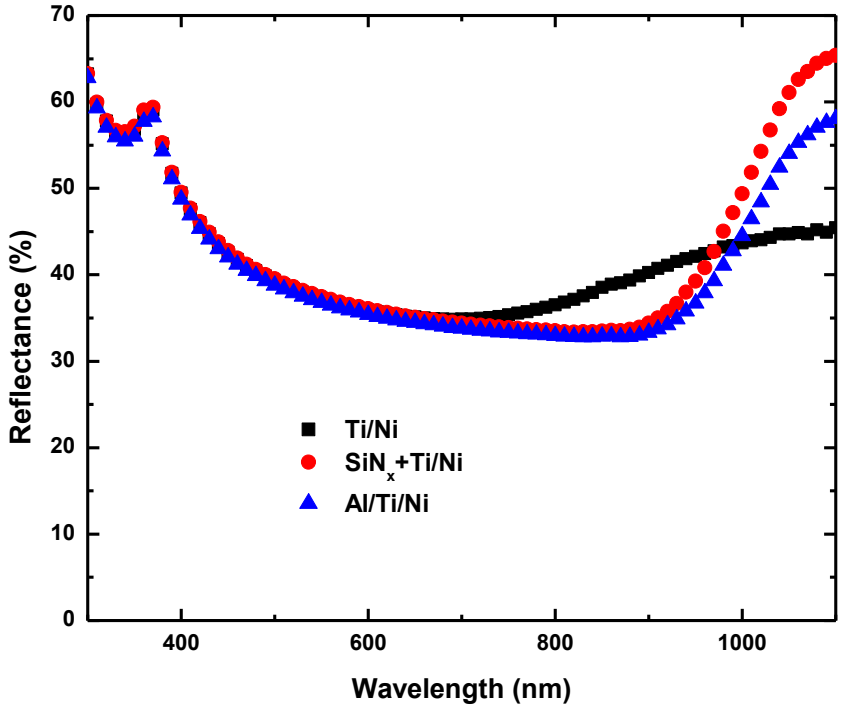


Figure 2.9: Reflectance comparison of different metal stacks as BSR for exfoliated substrates.

2.7 SUMMARY

A novel exfoliation technology capable of producing large area ~25µm thin flexible mono c-Si is introduced. These substrates have thick electroplated metal backing which provides support, mechanical strength and electrical contact so that they could potentially be used to fabricate high efficiency c-Si solar cells without the yield losses and handling issues that are major problems for traditional thin Si wafers. Experiments were carried out to quantify compressive stress and residual strain before and after exfoliation respectively. The failure modes for these substrates were observed. The

temperature limit for cell processing and module integration was also determined. A modification of the seed metal stack was done successfully to increase the back surface reflectance the substrates without modifying the thermal cycling process drastically.

Chapter 3: Single Heterojunction Solar Cells on Exfoliated Substrates [2]

3.1 CHOICE OF SOLAR CELL STRUCTURE

In Chapter 2, it has been established that exfoliated substrates with metal backing need to have a low thermal budget process to complete solar cells on them. That is why amorphous crystalline heterojunction (a-Si:H/c-Si) stack is chosen as preferred device architecture. Heterojunction solar cells have the following features.

- It is a low temperature approach. The a-Si:H could be deposited using plasma enhanced chemical vapor deposition (PECVD) method at a temperature <200 ºC. All the processes involved in the heterojunction solar cells are completed at low thermal budget and process time. Figure 3.1 shows a comparison of thermal budget and process time between regular diffused junction cells and heterojunction cells.
- Doped a-Si:H deposited through PECVD creates the pn junction. There is a significant difference of bandgap (E_g) between *c*-Si (Eg = 1.12 eV) and *a*-Si:H (Eg=1.6…1.9 eV). The beneficial aspect of the pn junction created by this method is that one type of carriers can be selectively collected at the contact while the other type of carriers could be blocked by a potential barrier. This is shown in the Figure 3.2, between p^+ emitter and n-type absorber and n^+ back surface field (BSF). The bandgap of doped a-Si:H depends very much on the deposition

[2] Certain parts of this chapter are reproduced from the following journal article. All the authors contributed to either experimental or technical or both the aspects.
S. Saha, M. M. Hilali, E. U. Onyegam, D. Sarkar, D. Jawarani, R. A. Rao, L. Mathew, R. S. Smith, D. Xu, U. K. Das, B. Sopori, S. K. Banerjee *Single heterojunction solar cells on exfoliated flexible ~25 μm thick mono-crystalline silicon substrates*, Appl. Phy. Lett., Vol. 102, pp. 163904-163908 April, 2013.

condition. Therefore one can engineer the a-Si:H thin films in such a way that large barrier at the band edge hinders minority carrier to recombine at the contact. Consequently, dark saturation ($I_{dark\ saturation}$) current goes down and open circuit voltage (V_{OC}) goes up.

- Additionally a very thin intrinsic amorphous Si (i-a-Si:H) is deposited between the doped and c-Si interface. This layer passivates the surface very well by reducing surface dangling bonds. Consequently surface recombination can be minimized drastically. Despite providing chemical passivation this layer is thin enough to facilitate tunneling of the carriers through this layer. This way any metallic contact is not directly touching the absorber surface and the passivation is maintained uniformly everywhere. In a diffused junction solar cell metal contacting the absorber directly provide recombination centers for minority carriers. Because of all of these reasons a purely heterojunction solar cell with thin i-a-Si:H passivation layer can reach a $V_{OC} > 700$ mV with an optimized process.
- Doped a-Si:H film is highly resistive. Therefore a direct metal contact to a-Si:H will not facilitate effective way of current collection due to a huge amount of lateral resistance in thin film. A transparent conducting oxide (TCO) is deposited on top of doped a-Si:H thin film. Traditionally this is a mixture of Indium Oxide (In_2O_3) and Tin Oxide (SnO_2). The metal contact is formed on top of this layer. Because of the conductive nature of this film lateral resistance is greatly reduced.

This is also a transparent layer which acts as a front surface Anti-Reflective Coating (ARC) to facilitate effective light absorption.

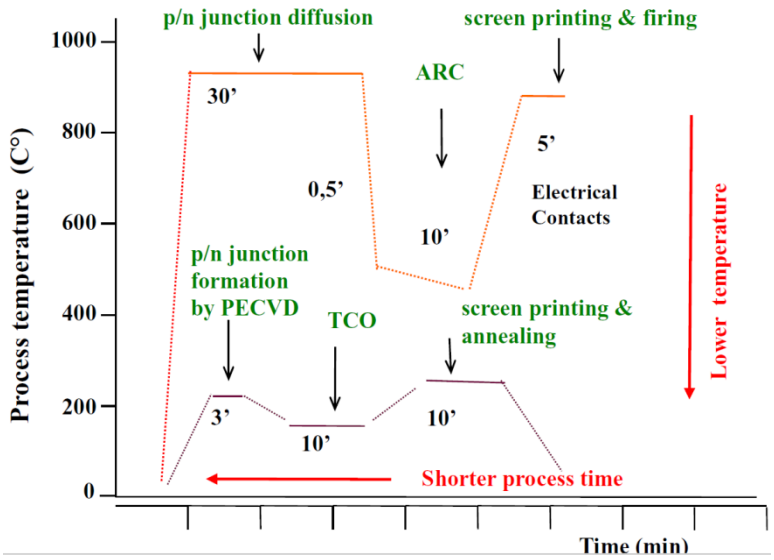


Figure 3.1: Estimated thermal budget and process time for the diffused junction c-Si technology (top curve) and heterojunction technology (bottom curve) [38].

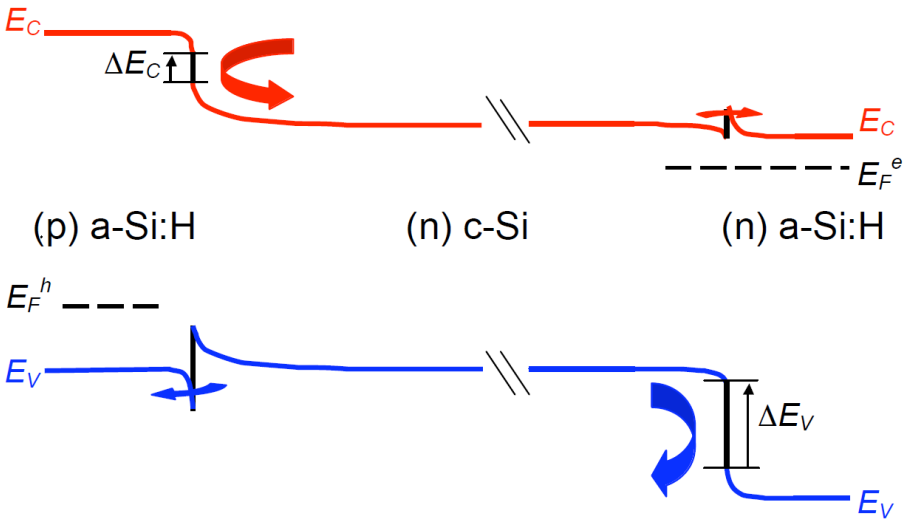


Figure 3.2: Illustrated band diagram of a (p) a-Si:H / (n) c-Si / (n) a-Si:H heterojunction solar cell under illumination [39].

3.2 SINGLE HETEROJUNCTION SOLAR CELL PROCESS FLOW

The exfoliated substrates are obtained from a thicker "parent substrate". Therefore part of the processing required to complete a solar cell could be carried out while it is still at a thick wafer stage. This is a beneficial feature of the exfoliation technique. One surface of the wafer can be doped, passivated and metallized to complete processing on one side of the final cell on exfoliated substrate. A schematic of the process flow and the final cell structure is shown in figure 3.3.

A thick (> 200 μm) n-type (~2 Ω.cm resistivity) mono-crystalline wafer is textured using a mix of 2% KOH and 8% iso-propyl alcohol (IPA) at 80° C temperature to obtain a random pyramidal texture, right before creating n^+ diffused junction to form BSF, as shown in Figure 3.3(a)**.** The n^+ diffusion doping is carried out at a $POCl_3$ furnace to create the back surface field (BSF). This BSF could have been created alternatively by

using plasma assisted chemical vapor deposition of n^+ a-Si:H. However, at the start of the process flow development, the effect of thermal cycling during exfoliation process on diffusion of contact metal to a-Si:H thin film could not be gauged. That is why for BSF, diffusion doping is chosen in the beginning. The sheet resistance is measured to be ~90 Ω/□.

The top surface of the doped substrate is coated with plasma-enhanced chemical vapor deposited (PECVD) silicon nitride (SiN_x) for passivation. The nitride is patterned with the help of photolithography. A positive photo-mask with 25% opening for metal contact was used. Positive photoresist (AZ5209) is spun coat at 500 rpm for 60 seconds to have conformal coating on a textured surface. Consequently the exposure time was increased to bleach the entire thickness of photoresist. After using developer (AZ726 MIF) to wash away the cross-linked photoresist, a wet etching is performed to open local contact windows (Figure 3.3(b)). This was done in 6:1 volume ratio of 40% NH_4F in water to 49% HF in water bath or better known as Buffered Oxide Etch (BOE) bath for 35 minutes. Figure 3.4 shows the point contact pattern during photolithography and etch. The windows are 100 μm by 100 μm and separated from one center of the square to another center of square by 200 μm.

A metal seed layer stack consisting Ti (20 nm) / Ni (20 nm) or Al (20 nm) / Ti (20 nm) / Ni (20 nm) is then deposited on the patterned surface using e-beam evaporation and subsequently electroplated with ~50-55 μm thick nickel metal layer (figure 3.3 (c)). In this way partial fabrication of the cell is completed while it is still in thick wafer form. The Si wafer bonded with thick metal layer is subjected to thermal cycling process (<

300°C) lasting approximately 10 minutes to generate stress in the metal/semiconductor stack due to the coefficient of thermal expansion (CTE) mismatch between the back metal and the Si. This bi-material under stress is put through exfoliation process, aided and controlled by a mechanical wedge at a predetermined location on the wafer, leading to fracture along a sub-surface plane of Si (Figure 3.3 (d)) to obtain the exfoliated substrate. The residual parent wafer can be reused for exfoliation again. The exfoliated substrate is laser cut in to square or pseudo-square shape to carry out further processing. The exposed Si surface of the exfoliated substrate is then cleaned and textured (Figure 3.3 (e)) using the same KOH based chemistry as mentioned in the first step of the process flow. Since the substrates are inherently curved, in order to have uniform etching in the chemical bath a chemically resistant Teflon holder with a top and bottom plate is used. A picture of the holder with a substrate is shown in Figure 3.5.

After texturing, the substrate is treated with piranha solution (1:1 ratio of H_2O_2, H_2SO_4) for 2 minutes to decontaminate. Hydrofluoric acid (HF) with 5% concentration is used to dewet the surface before plasma assisted chemical vapor deposition of intrinsic (i-layer) and p^+ doped hydrogenated amorphous Si (a-Si:H) is carried out to passivate and create the front surface emitter respectively. Indium Tin Oxide (ITO) is sputter deposited as a transparent conducting oxide (TCO). In order lower the thermal budget the film was initially deposited at room temperature. Though the integrated transmission was close to 90%, the sheet resistance was ~90 Ω/□, for a film thickness of 100 nm. The sheet resistance was further lowered to ~70 Ω/□ when the temperature of the platen in contact with the substrate is gradually raised 200° C during deposition. The integrated

transmission was further improved too. A comparison in sheet resistance and transmission is shown between room temperature and 200° C process in Figure 3.6. In the final step, a low-temperature silver (Ag) paste (PV-412 from DuPont) is screen-printed to form the front contact. The solar cell is subsequently heated at 140°C for 30 minutes to cure the Ag paste. A picture of the completed device is shown Figure 3.7. The separate dies are created by depositing ITO through a shadow mask on a-Si:H thin film. This way numerous isolated devices could be measured on a single substrate.

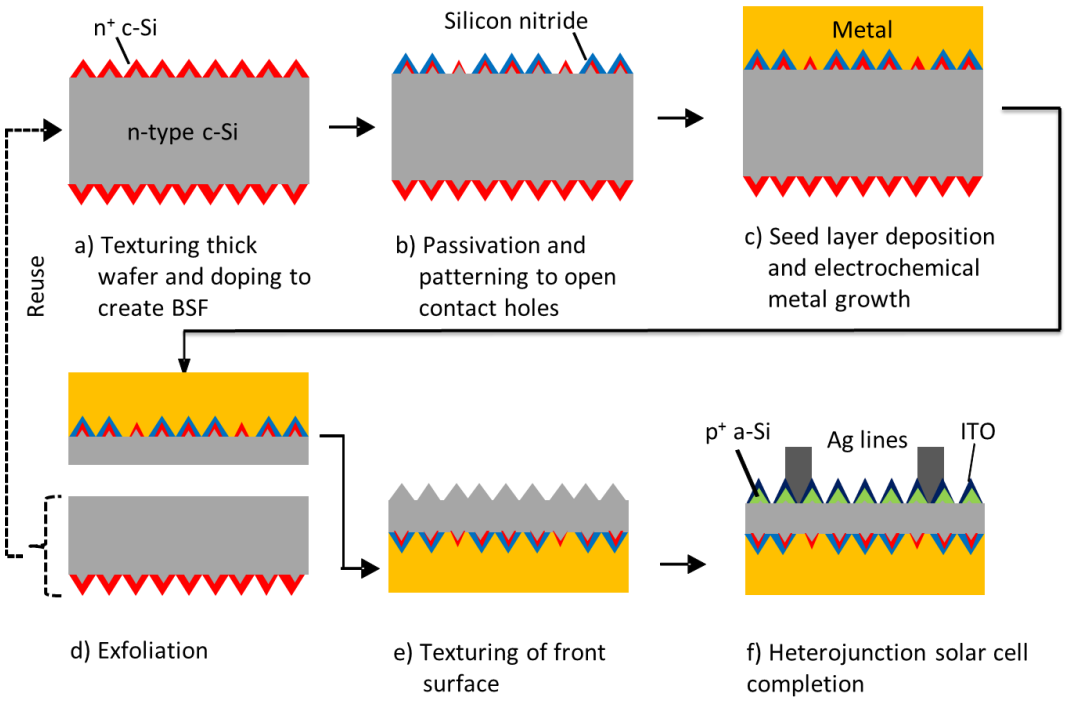
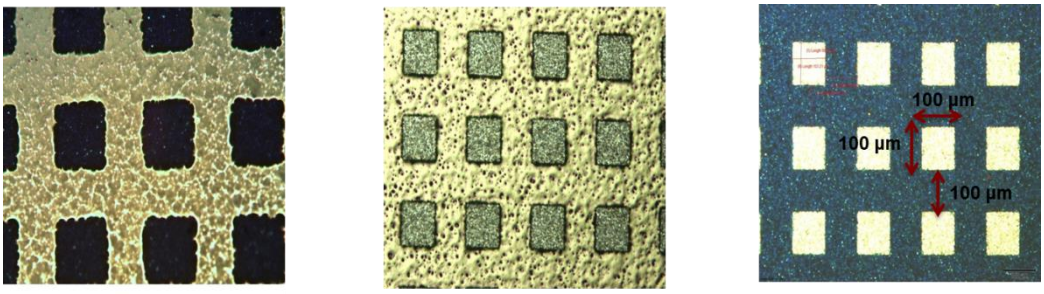


Figure 3.3: Process flow for SHJ solar cells on ~25µm-thick Si SOM® substrates.



(a) (b) (c)

Figure 3.4: Rear contact pattern with 25% metal coverage (a) after exposure and development, (b) after BOE etch for 35 minutes with photoresist still on, (c) after stripping off photoresist.

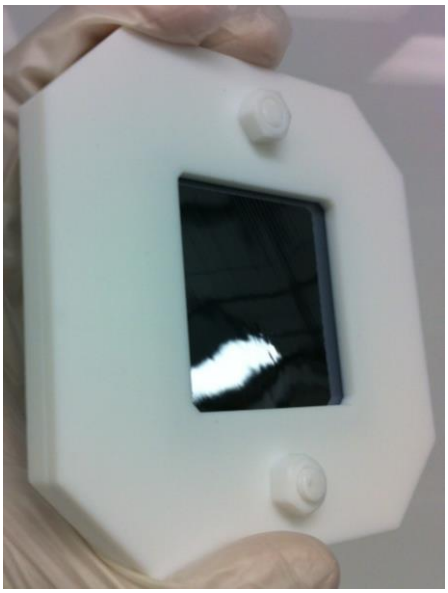
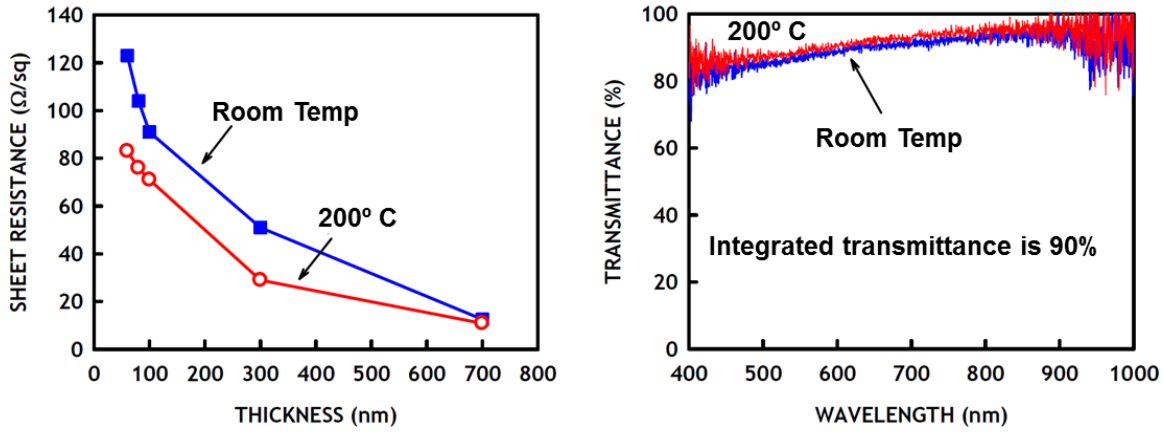


Figure 3.5: Custom made exfoliated substrate holder used for uniform KOH texturing.



(a) (b)

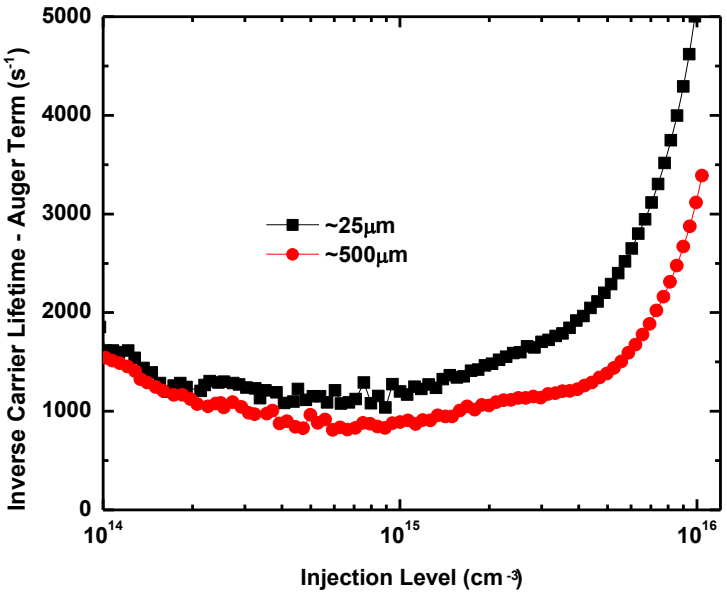
Figure 3.6: (a) Sheet resistance variation with thickness of ITO sputtered at room temperature and at 200° C, (b) measured transmission of ITO sputtered on glass slide at room temperature and at 200° C.

Figure 3.7: A completed single heterojunction (SHJ) solar cell on 2 inch square substrate. The individual blue squares are isolated devices.

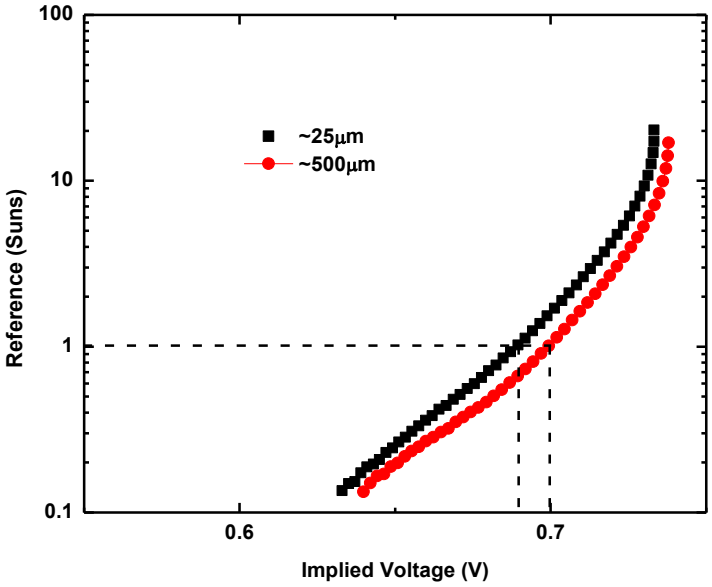
3.3 CRYSTALLINE INTEGRITY OF EXFOLIATED SUBSTRATES: BULK LIFETIME MEASUREMENT

Since exfoliation uses mechanical cleaving, it may introduce surface defects and more importantly compromise crystalline integrity. Thus bulk lifetime of exfoliated substrate could be compared with a thick wafer to verify the quality of the bulk. Free-standing ~25 μm Si is obtained by etching the backing metal (Ni) SOM® using SC-2 solution (3:1:1 ratio of H_2O:H_2O_2:HCl). Lifetime is measured using contactless quasi steady state photoconductivity current (QSSPC) method using WCT-120 lifetime tester [40]. The effective lifetime of free-standing ultra-thin substrate is compared with the effective lifetime of its parent wafer before exfoliation. The passivation of both surfaces of the wafer in either case is achieved with the help of quinhydrone/methanol (QHY/ME) solution using 0.01mol/dm^3 concentration. Previous work has shown this concentration of QHY/ME to passivate high resistivity FZ wafers with a surface recombination velocity of 7cm/s [41]. Figure 2(a) shows comparison of Auger corrected inverse lifetime data as a function of the injection level measured on an exfoliated ~25μm wafer and its ~500μm parent wafer before exfoliation. The measurement is carried out under high-injection condition ($1\times10^{15}cm^{-3}$). The graph of the inverse lifetime is compared with the best possible linear fit. The fit intercept value is used to calculate the bulk lifetime. In both cases the effective lifetime is similar at a low injection level ($1\times10^{14}cm^{-3}$) as evident from figure 2(a). At higher injection level (close to $1\times10^{16}cm^{-3}$) the inverse lifetime curves depart from each other due to greater influence of the surface passivation. In case of exfoliated Si, surface lifetime (τ_s) decreases with decreasing thickness of the bulk (W) as

shown by the equation $\tau_s = \frac{W}{2S} + \frac{1}{D}(\frac{W}{\pi})^2$, where S is the surface recombination velocity assuming both surfaces are identically passivated, and D is the minority carrier diffusivity. Consequently, effective lifetime (τ_{eff}) is lower because $\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}$, where τ_b is bulk lifetime. Bulk lifetime calculated from linear fit intercept at y-axis is found to be ~1700μs in both cases. Therefore, it is reasonable to infer that there is no significant change in crystalline integrity of the thin Si due to exfoliation. Figure 2(b) shows comparison between the implied V_{OC} of the same parent wafer and exfoliated wafer. It was found in previous work that there is a good agreement between implicit and actual V_{OC} for crystalline Si solar cells. The V_{OC} curve is generated by the tester from the measured τ_{eff} and diffusion length (L_{eff}) [42]. This also takes into account the optical constant based on the thickness of the substrate and coating (or lack of coating) on the surface. Under 1 sun illumination the implied V_{OC} of the exfoliated substrate is 689mV whereas that of the parent wafer before exfoliation is 699mV. This further reinforces absence of negative impact of exfoliation process on intrinsic material property of mono-crystalline Si.



(a)

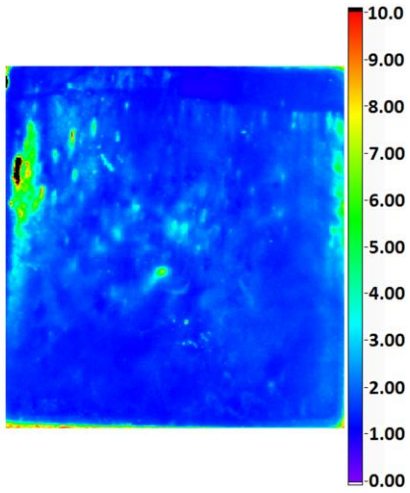


(b)

Figure 3.8: (a) Auger-corrected inverse lifetime as a function of injection level and (b) implied V_{OC} versus light-bias curves for the parent wafer (before exfoliation) and exfoliated free-standing thin Si.

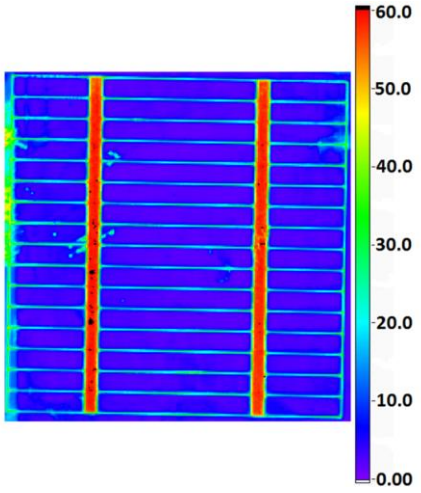
3.4 UNIFORMITY OF THIN FILM AND TEXTURE AND ON EXFOLIATED SUBSTRATE

Completed large area (18.6cm^2) solar cells with front surface texture were measured at an optical wavelength of 633nm using a PV reflectometer to obtain the reflectance spectrum mapping of entire active area. Figure 3 shows scan profile obtained from reflectance spectroscopy on flexible cells (a) without and (b) with screen printed contacts. Most of the surface area is shown in blue color at ~4% reflectivity. Some edge areas which were masked during the texturing process show higher reflectivity (~8-25%) shown in yellow and green color in figure 3(a) and (b) respectively. As expected, the screen-printed silver grid shows the highest reflectivity (~60%) as shown by the red color in figure 3(b). This profile implies that it is possible to obtain uniform random pyramid texturing and anti-reflective coating for light trapping purpose on such flexible substrates over a large area.



(a)

(**Figure 3.9** continued next page)



(b)

Figure 3.9: Reflectance profile map obtained on 18.6cm^2 area solar cells (a) without and (b) with screen printed metal contacts.

3.5 ELECTRICAL CHRACTERISTICS OF SINGLE HETEROJUNCTION SOLAR CELLS ON EXFOLIATED SUBSTRATES

J-V characteristics of several completed SHJ cells were measured using a 1.1cm^2 aperture area. The best results so far, are summarized in table I and the characteristics curves are shown in figure 4. Internal quantum efficiency (IQE) spectra (figure 5(b)) for the individual cells (tabulated in table I) were obtained from corresponding external quantum efficiency (EQE) and reflectance (R) spectra in figure 5(a). The IQE is calculated using IQE=EQE/(1-R) to allow for a more accurate representation of the spectral collection efficiency. The cells are differentiated based on front surface morphology and absence or presence of i-layer. We observed the highest V_{OC} (603mV)

on a cell with no front surface texture and no i-layer. With i-layer inclusion V_{OC} is reduced by 23mV, but we see a boost in short circuit current density (J_{SC}) and fill factor (FF), thereby increasing the overall efficiency by 1.2% absolute. The reduction in V_{OC} could be due to unintentional surface contamination introduced during chemical cleaning process before a-Si deposition. This issue could be resolved by improved surface cleaning which is discussed in the next chapter in detail. The cells with front-surface texture without the i-layer have low V_{OC} and FF. The textured surface has higher effective surface area and hence surface recombination velocity (SRV) is even higher due to surface contamination. This again indicates that the cleaning process and a-Si:H deposition needs to be more optimized for the textured surface. However, we do see a significant boost in J_{SC} for the textured solar cells. Even without an i-layer passivation the highest J_{SC} is 34.4mA/cm^2. This suggests that our cell is benefiting from significant internal photon reflection or light trapping. The IQE (figure 5(b)) for all the cells in the mid-wavelength region (600-800nm) is high (>97%) and indicates absence of any major bulk defects post exfoliation. The rapid decline of IQE at wavelengths >850nm is likely due to the sub-optimal quality of the rear-surface passivation. The back surface recombination can be reduced by reducing the back metal contact surface area and passivating most of the back surface with better quality SiN_x or thermal oxide. Alternatively, a dual heterojunction (DHJ) solar cell design with a-Si:H (i/n$^+$) layer on the back of the solar cell can be employed for enhanced back surface passivation.

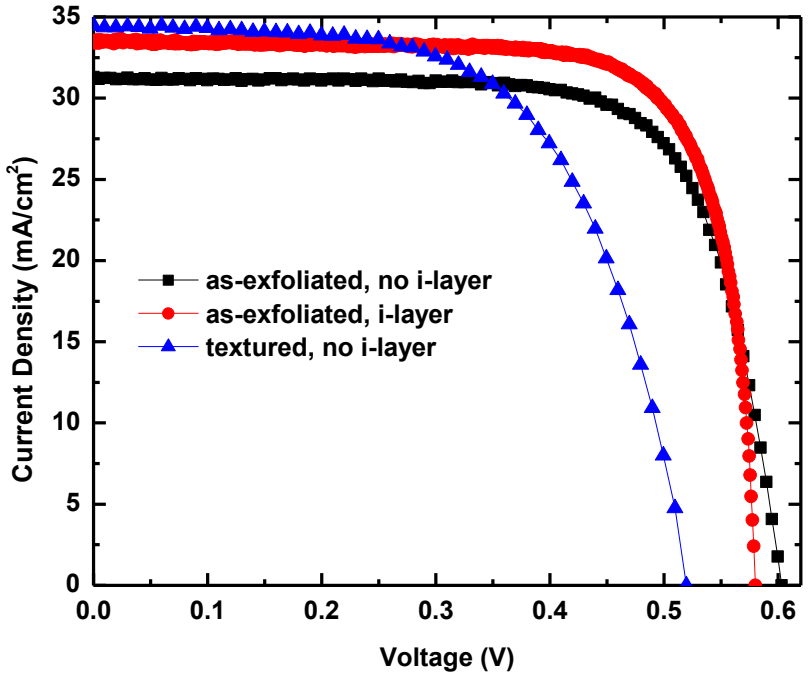
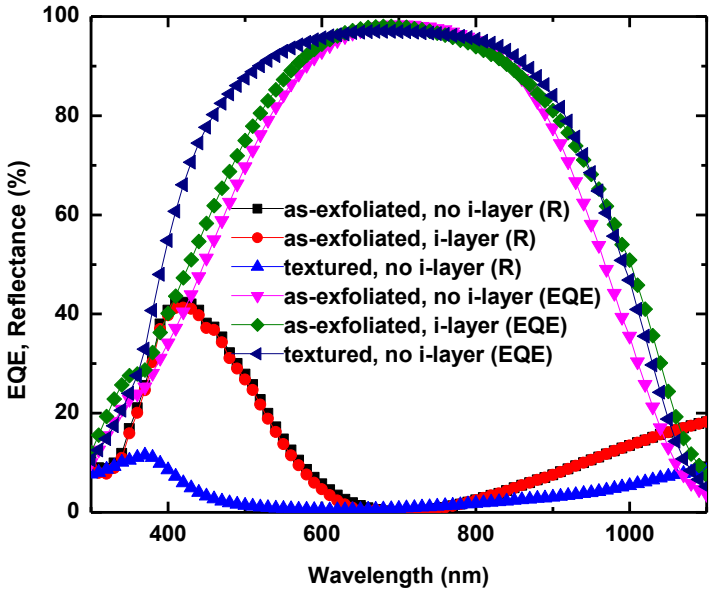


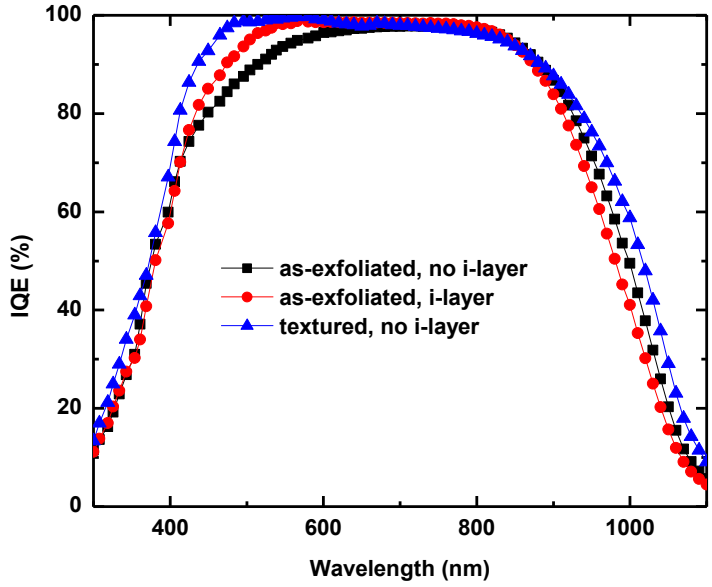
Figure 3.10: J-V characteristics at AM1.5 illumination for three devices, differentiated based on front surface morphology and exclusion/inclusion of i-layer.

Cell	**V_{OC} (mV)**	**J_{SC} (mA/cm^2)**	**FF (%)**	**Efficiency (%)**
As-exfoliated, no i-layer	603	31.3	72.7	13.7
As-exfoliated, i-layer	580	33.6	76.7	14.9
Textured, no i-layer	523	34.4	61	11

Table 3.1: J-V data summary at AM1.5 illumination for three devices, differentiated based on front surface morphology and exclusion/inclusion of i-layer.



(a)

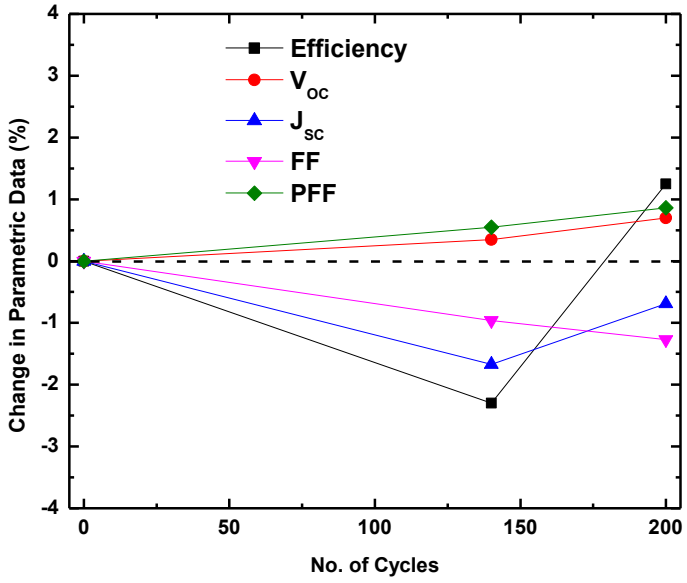


(b)

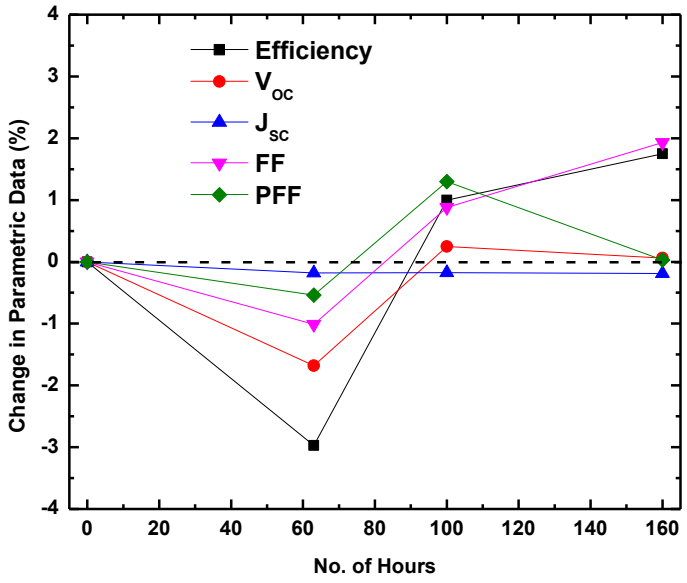
Figure 3.11: (a) EQE and reflectance spectra measured on as-exfoliated and textured solar cells in the 300-1100nm range, (b) IQE spectra extracted from corresponding EQE and reflectance curves.

3.6 MODULE RELIABILITY: THERMAL SHOCK TEST AND HIGHLY ACCELERATED STRESS TEST (HAST)

Though heterojunction solar cells comprises of both a-Si and c-Si, they do not show strong light induced degradation [43] (like thin film a-Si cells), or exhibit strong temperature dependence on performance [44]. However, due to the inherent residual stress left in the bi-material substrates, module reliability is a major concern to address. Thermal shock test and highly accelerated stress test (HAST) [45] are standardized tests that are usually carried out on PV modules for reliability. Modules were made by laminating tabbed solar cells using then un-optimized cell fabrication process on SOM® substrates. In order to validate that the SOM® bi-material composite substrate can endure in the modules without reliability issues, such as breakage in Si film or de-bonding at the Si/metal interface, modules were subjected to thermal shock (-40°C to 85°C) and HAST (120°C & 100% relative humidity (RH)) tests. Figures 3.12 (a) and (b) show preliminary thermal shock and HAST test results respectively from one such module. As illustrated in the figures, after 200 thermal shock cycles and 160 HAST hours, the module parameters (efficiency, V_{OC}, J_{SC}, FF, and pseudo FF (PFF)) are still within standard PV module reliability testing performance specifications (<5%); thus, demonstrating the robustness of the heterojunction SOM® solar cell technology.



(a)



(b)

Figure 3.12: (a) Thermal shock test data, and (b) highly accelerated stress test (HAST) data for a PV module made with SOM® solar cells.

3.7 SUMMARY

In conclusion, we have shown integration of the SHJ architecture in solar cells made on flexible Si (~25μm) substrates (SOM®) obtained through an exfoliation process. This was carried out using standard toolsets without any special handling or breakage problems. We have presented optical and electrical characteristics of large area cells to show the viability of this technology. Among several single heterojunction ~25μm thick solar cells fabricated with un-optimized processes, the highest V_{OC} of 603mV, $J_{SC}$of 34.4mA/cm^2, and conversion efficiency of 14.9% were achieved separately on three different cells. Initial reliability test results on modules showed compatibility of this technology with SHJ cell process flow.

Chapter 4: Improved Surface Preparation for Single Heterojunction Solar Cells on Exfoliated Substrates [3]

4.1 CHALLENGES IN SURFACE PREPARATION OF EXFOLIATED SUSBSTRATES

In the previous chapter we have demonstrated single heterojunction (SHJ) solar cells fabricated on exfoliated substrates exhibiting efficiencies 14.9% on as-exfoliated substrates. However, on textured surfaces efficiency was limited to 11%. We postulated that one of the issues that could be limiting the performance of the cells is unintentional front surface contamination introduced during wet chemical processes before hydrogenated amorphous Si (a-Si:H) deposition of the front surface emitter, which can limit the open-circuit voltage (V_{OC}) of these solar cells. This could happen due to the presence of potassium ions introduced from potassium hydroxide (KOH) during texturing. For decontamination we could not use SC-2 solution (5:1:1 ratio of H_2O, H_2O_2, HCl at 80ºC) as it reacts rather aggressively with the electroplated Ni back metal. Instead, we used a piranha solution (1:1 ratio of H_2O_2, H_2SO_4) for both decontamination from potassium ions and removal of organic contaminants, which did not seem to show corrosion degradation in the backside Ni. The pH level of HCl is slightly lower compared to H_2SO_4, and SC-2 solution has a stronger effervescent action than piranha solution. This may explain why the Ni is much more affected by the SC-2 clean compared to the

[3] Certain parts of this chapter are reproduced from the following journal article. All the authors contributed to either experimental or technical or both the aspects.
S. Saha, M. M. Hilali, E. U. Onyegam, S. Sonde, R. A. Rao, L. Mathew, A. Upadhyaya, S. K. Banerjee, *Improved Cleaning Process for Textured ~25µm Flexible Mono-crystalline Silicon Heterojunction Solar Cells with Metal Backing*, J. Solid State Sc. And Tech, Vol. 3 (7) Q1-Q4, 2014.

piranha clean. Nevertheless, piranha-treatment alone is probably inadequate for metal residues or potassium related contaminant removal after texturing.

In this chapter, we attempted to address the front surface contamination issue by developing an improved cleaning procedure for textured silicon surfaces for mono-crystalline exfoliated Si substrate. We assumed the cleaning process employed for the rear surface is sufficient as it was done using traditional RCA cleaning [46] on a textured thick parent wafer. With the help of X-ray Photoelectron Spectroscopy (XPS) we have identified the chemical bonding nature of key contaminants at the surface i.e. carbon and potassium. We have also employed Auger electron spectroscopy (AES) to quantify the atomic concentration of the impurities before and after implementation of various wet chemical cleans. We have fabricated and characterized SHJ solar cells on both exfoliated and bulk (~180 μm) substrates to study the effect of contamination on device performance and how an improved surface clean procedure can affect the solar cell efficiency.

4.2 COMPARISON OF CLEANING PROCEDURE BY MONITORING SURFACE CONTAMINATION USING SPECTROSCOPIC METHOD

For spectroscopic analysis, we cut exfoliated substrates into 10×10 mm^2 pieces. These small area substrates were degreased by using acetone and isopropyl alcohol (IPA) sonication. They were then textured on the front (exfoliated) side using a KOH (2%), IPA (8%) and water mixture at 80ºC followed by a 5 minute deionized (DI) water rinse. Four separate samples (numbered 1 to 4) were fabricated based on the surface treatment they went through, right after texturing. Sample 1 is used as a control sample with no

additional cleaning processes done to decontaminate the surface. Sample 2 was cleaned with piranha solution (1:1 ratio of H_2O_2, H_2SO_4) for 2 minutes. This is the old cleaning procedure employed in our previous work [47]. Sample 3 was treated with a 1:40 water based solution of SC-15 [48] (Surface Chemistry Discoveries, Inc.) at 40ºC for 5 minutes. SC-15 is used as an alternative to RCA clean. It is well documented in the literature [49], [50] that SC-1 step (5:1:1 ratio of H_2O, H_2O_2, NH_4OH at 80ºC) in RCA cleans causes micro-roughening and even pitting of silicon substrates, thereby introducing trap states (D_{it}) at the heterointerface [51]. We ensure extremely low anisotropic silicon etch rate to reduce roughening the surface by using high dilution (1:40) of SC-15 formulation. This is verified by scanning electron microscopy (SEM) done before and after SC-15 treatment. The surface morphology doesn't change as the solution was not concentrated enough and the temperature wasn't high enough to round off the sharp edges of the random pyramids that has been typically shown in previous literature [52], [53] due to different isotropic etches for heterojunction cell processing. The diluted solution has a composition of 0.05 to 10% by weight water soluble alkanolamine, 0.01 to 2.5% by weight of quaternary ammonium hydroxide, 0.01 to 2% by weight chelating agent, and the pH of this composition is about 10 to 13. The solvating action of quaternary ammonium hydroxide helps in removing the organic compounds, and additionally raises the pH level to help the organic amine remove metal contaminants, which acts as a ligand and forms complexes with the metal cations [54], [55]. The chelating agent was used to increase the capacity of the cleaning bath to retain metals in solution by acting as a multi-dentate ligand forming a stable multi-dentate complex with the metal cations, which enhances the dissolution of

metallic residues on the silicon surface [56], [57]. The temperature of 40ºC aids in the contaminant removal, but is still not high enough to result in anisotropic etching of the silicon. Finally, sample 4 was treated with SC-15, followed by DI water rinse and then 2 minute piranha cleaning process. This was done to see if additional piranha clean at the end results in further removal of organic impurities from the surface. Complete details of the cleaning steps employed on samples 1 to 4 are shown in Table 4.1.

Step	Sample 1	Sample 2	Sample 3	Sample 4
1	Acetone+IPA sonication	Acetone+IPA sonication	Acetone+IPA sonication	Acetone+IPA sonication
2	Texturing (2% KOH+ 8% IPA)	Texturing (2% KOH+ 8% IPA)	Texturing (2% KOH+ 8% IPA)	Texturing (2% KOH+ 8% IPA)
3	5 min DI water rinse	5 min DI water rinse	5 min DI water rinse	5 min DI water rinse
4	5% HF dewet	5% HF dewet	5% HF dewet	5% HF dewet
5	-	5 min DI water rinse	5 min DI water rinse	5 min DI water rinse
6	-	Piranha (2min)	SC-15 (@40ºC, 2min)	SC-15 (@40ºC, 2min)
7	-	5 min DI water rinse	5 min DI water rinse	5 min DI water rinse
8	-	5% HF dewet	5% HF dewet	5% HF dewet
9	-	-	-	5 min DI water rinse
10	-	-	-	Piranha (2min)
11	-	-	-	5 min DI water rinse
12	-	-	-	5% HF dewet

Table 4.1: Cleaning/etching processes used in preparing samples 1 to 4 for XPS and AES analysis.

XPS measurements were carried out on these four samples using monochromatic Al Kα X-ray source of 1486.7eV excitation energy with an analyzer work function of 4.5eV. For this analysis we concentrated our focus on monitoring photoelectron peaks for organic (carbon) (C) and potassium (K). This was done based on the identification of probable organic/metallic contamination in the XPS survey spectra. High-resolution multi-region spectra of the main signals, i.e. C 1*s*, O 1*s* and K 2*p* with Gaussian-Lorentzian curve (continuous line) fitting of the recorded photoelectron spectra (points) was used in order to characterize and understand the chemical bonding nature of the contaminants based on the observed chemical shifts.

The C 1*s* (284.6 eV) and K 2*p* (292.9 eV) photoelectron peaks are very close to each other and the former is a more intense peak than the latter one, thereby making the K 2*p* peak less apparent in a survey spectra scan in Figure 4.1. In Figure 4.2 (a) the main peak of the C 1*s* signal at 284.6 eV is due to hydrocarbons. The other fitted peaks show binding energy signals due to different C-O functional groups [58]. The source for these C peaks in sample 1 could be due to trace amounts of IPA residue from the KOH solution, as well as dissociation of organic additives (brightener) and carbonate (used to maintain pH balance of the electroplating bath) from the electroplated back metal. Some of these C-O peaks become relatively less intense or nonexistent compared to C-C peak in subsequent samples (2-4) with improved sample cleans. This effect is most prominent in sample 4. This suggests that the organic contamination is most effectively removed when the cleaning procedure in sample 4 is employed. This could be validated further by comparing the O 1*s* peak for the most contaminated sample (i.e. sample 1) with that of

sample 4. When the O 1*s* peak is de-convoluted to find out the different contributions (Figure 4.2 (b)), it shows peaks due to native oxide (SiO_x) at 532.2 eV and C-O bonding at 532.8 eV. In case of sample 4, the relative intensity of the peak suggesting C-O bonding is significantly less than that in sample 1. For sample 4 the peak due to SiO_x is more dominant, suggesting a surface less organically contaminated. For K $2p_{3/2}$ (292.9 eV), K $2p_{1/2}$ (295.7 eV) peaks, only sample 1 shows any detectable intensity (Figure 4.2 (c)), even in high spatial resolution XPS (0.2 mm diameter lens aperture). This is probably due to limitation in lateral detection area posed due to high spatial resolution lens aperture compounded by non-uniform distribution of K contaminants. With 0.2 mm lens aperture the photoelectron counts for K is lost in the background noise for samples 2, 3 and 4.

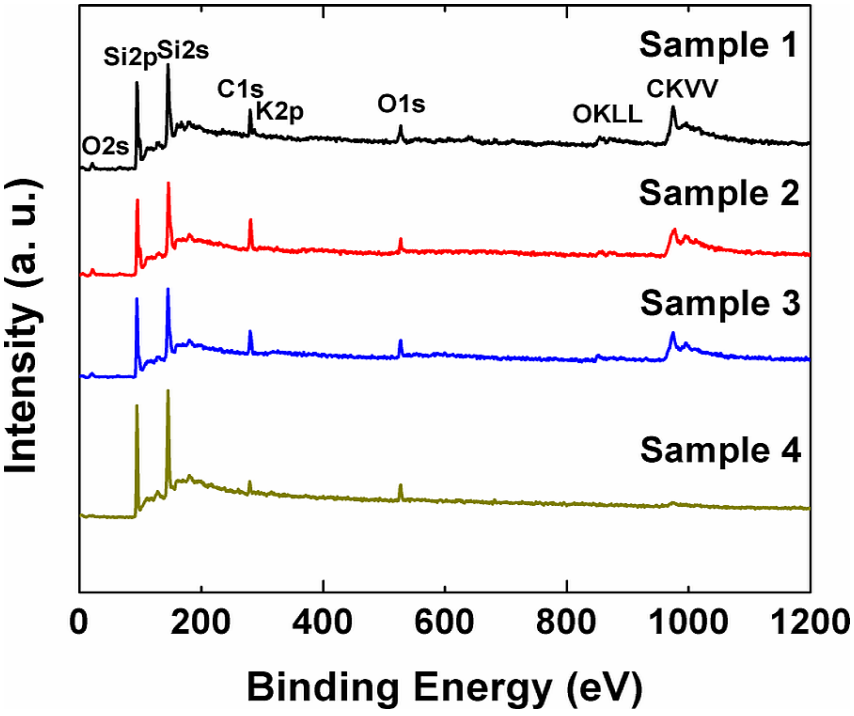
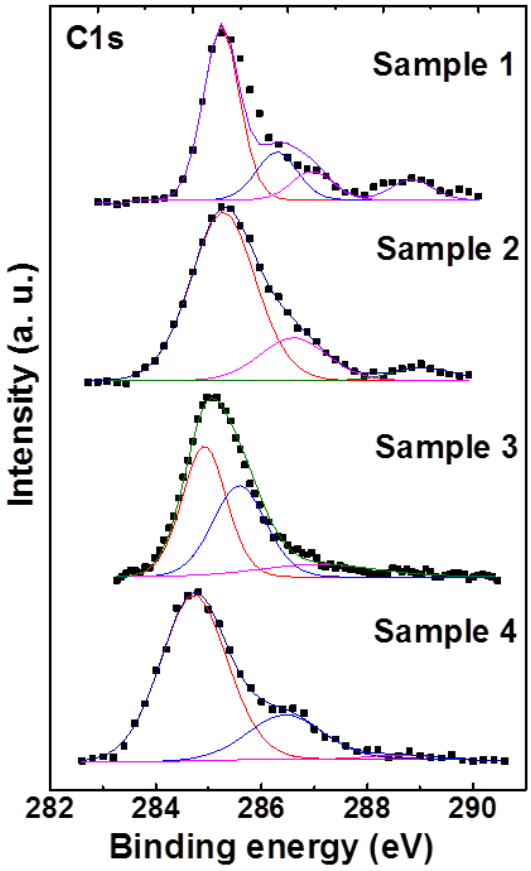
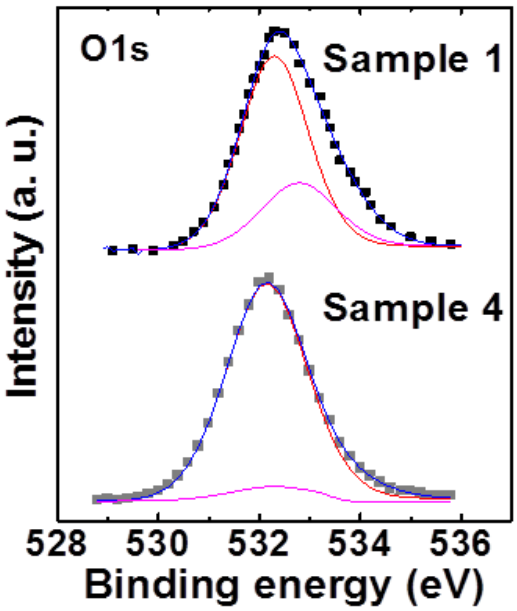


Figure 4.1: XPS survey spectra of the different sample surfaces.

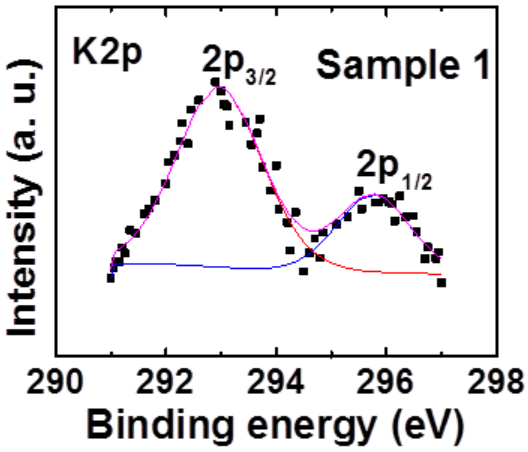


(a)

(**Figure 4.2** continued next page)



(b)



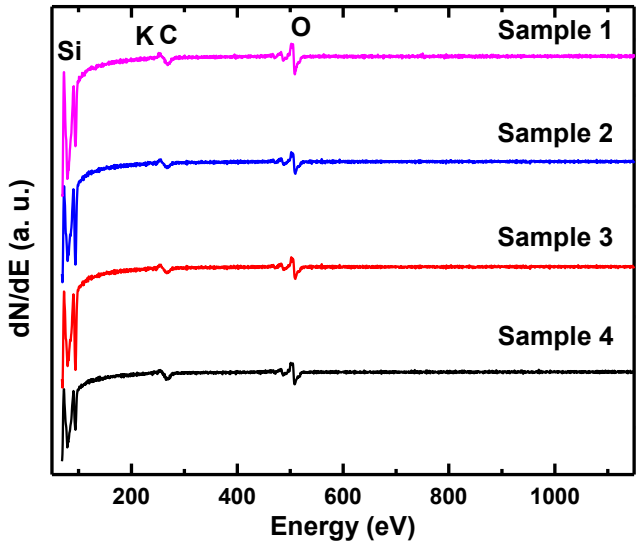
(c)

Figure 4.2: XPS multi-region high-resolution spectra of different sample surfaces, showing photoelectron peaks with Gaussian-Lorentzian fitting. The intensity is shown with arbitrary units (a. u.).

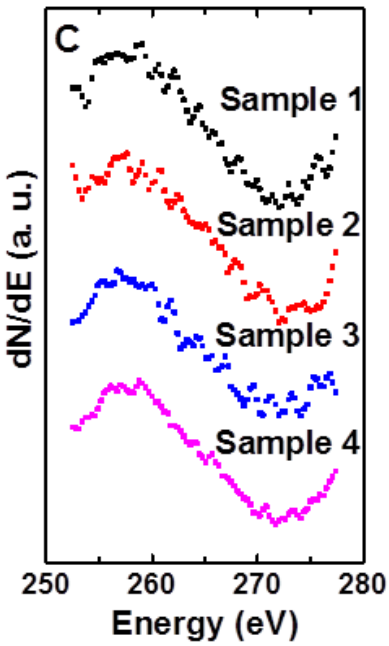
Samples 1 to 4 were also characterized using AES *in situ*. AES provides higher lateral resolution measurement when the surface distribution of the elements is less than a micrometer scale [59]. To detect trace amount of contaminants on a surface this might be useful. The AES peaks are superimposed on an imported background of different types of secondary electrons. Hence, the AES spectra are represented in the differentiated form. After differentiation the data is further smoothened using a five point Savitzky-Golay filter.

Figure 4.3 (a) shows the AES survey spectra of the substrate surfaces for the four samples. Figure 4.3 (b) and (c) show high resolution spectra for C (272 eV) and K (252 eV) respectively. The concentration of each element is calculated by $C_X = \frac{\frac{I_X}{S_X d_X}}{\sum \frac{I_j}{S_j d_j}}$; where I_X is the peak-to-peak amplitude of the element X from the test spectra, S_X and d_X are the relative sensitivity and the scale factor of the element X, respectively; Σ denotes the sum for all the peaks [60]. Table 4.2 gives the atomic concentrations for C and K. The percentage data shown in Table II suggest that although the old clean (sample 2) reduces the C and K contamination by 0.52% and 0.23% absolute, respectively; SC-15 is much more effective in reducing the K contaminant (by 0.86% absolute), and organic contaminants are reduced by 0.73% absolute as observed for sample 3. Some heavy organic contaminants may be hard to oxidize and remove through piranha clean alone. However, a piranha clean following SC-15 is even more effective in reducing the organic contaminants further down by 0.48% from sample 3. Therefore, the cleaning process

used in sample 4 is more optimal in reducing both C (by 1.21% absolute) and K (by 0.89% absolute) contamination.

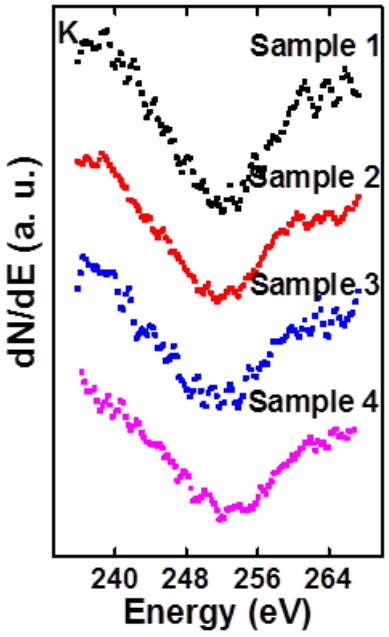


(a)



(b)

(**Figure 4.3** continued next page)



(c)

Figure 4.3: (a) AES survey spectra of the different sample surfaces, (b) AES multi-region high-resolution spectra of different sample surfaces with differentiated peaks for C (272 eV) and (c) differentiated peaks for K (252 eV). The intensity is shown with arbitrary units (a. u.).

Sample	Sample 1	Sample 2	Sample 3	Sample 4
C	2.84%	2.32%	2.11%	1.63%
K	1.11%	0.88%	0.25%	0.22%

Table 4.2: Atomic percentages calculated for C and K from the surfaces of samples 1 to 4.

4.3 COMPARISON OF CLEANING PROCEDURE BY ELECTRICAL MEASUREMENTS

Single heterojunction cells with diffused back junction were fabricated to evaluate the efficacy of the developed new clean (sample 4) as compared to the old clean (sample 2) on exfoliated substrates with front-surface texture. The thickness of the Indium Tin Oxide (ITO) is reduced from 100 nm (used in previous chapter) to 75 nm to increase short wavelength response. Current-voltage (J-V) measurements were carried out to obtain the short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and maximum power point (MPP) for cells that employed the old cleaning process, and the new cleaning process, under AM 1.5 sun illumination. The measurement was done using a 1.1 cm^2 cell aperture area. Internal quantum efficiency (IQE) measurements for the individual cells were calculated from corresponding external quantum efficiency (EQE) and reflectance (R) measurement data (IQE=EQE/(1-R)) to obtain a more accurate representation of the spectral collection efficiency. We have also fabricated ~180 μm thick wafer-based solar cells using identical process flow (save for the exfoliation step) and device architecture to that of the ultrathin solar cells. These cells are fabricated in order to compare their performance to that of the exfoliated solar cells. For this experiment we have compared samples which have gone through old (sample 2) and new (sample 4) cleaning procedure.

The current-voltage results for the exfoliated cells are summarized in Table 4.3 and the J-V curves are shown in Figure 4.4. We observed that with the newer and more optimized cleaning process the V_{OC} increases by 22 mV, and the current increases by 0.7

mA/cm^2. The fill factor is further increased by 3.5% absolute. As a result the overall efficiency increases by 1.5% absolute (or 12.7% relative). This again indicates that the new cleaning process is more effective in removing elements that can result in mid-gap traps like potassium in Si. The solar cell with the new cleaning process shows an average of 4.5% improvement in short-wavelength response (300-500 nm) (Figure 4.5), as compared to the cell using the old cleaning procedure. This suggests reduced surface recombination at the a-Si:H/c-Si interface due to reduction in surface states. The slight improvement in the mid-to-near infrared wavelength response suggests that bulk lifetime may have effectively been slightly improved as well for such ultrathin Si solar cell with the new clean compared to that using the old clean. However, in order to achieve a V_{OC} greater than 600 mV we still need to optimize the thin film deposition on textured surfaces and use intrinsic a-Si layer (i-layer) to passivate the dangling bonds at the c-Si surface.

Cell	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
old clean	525	35.2	64	11.8
new clean	547	35.9	67.5	13.3

Table 4.3: J-V data summary at AM1.5 illumination for solar cells on exfoliated substrates, based on cleaning process employed.

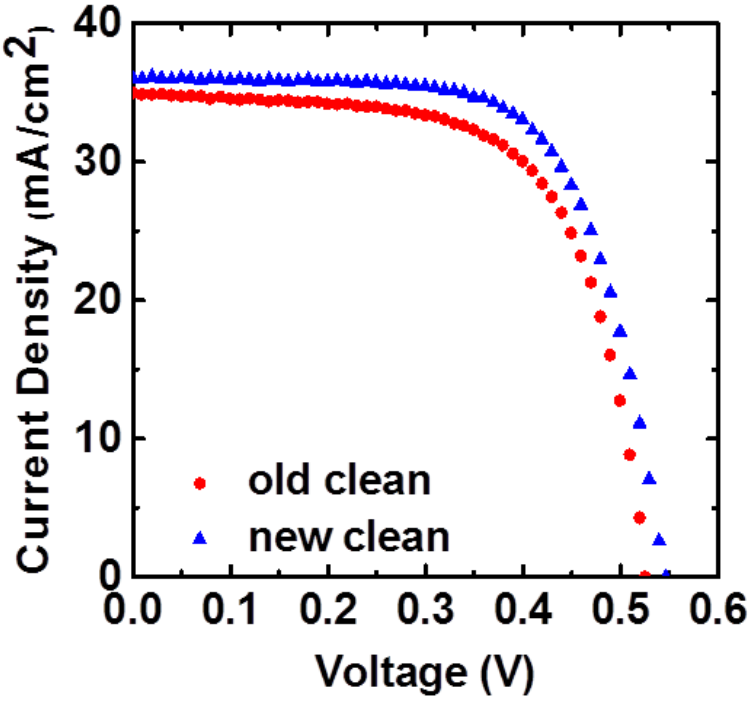


Figure 4.4: J-V characteristics at AM1.5 illumination for solar cells on exfoliated ~25 μm thick substrates, differentiated based on cleaning process employed.

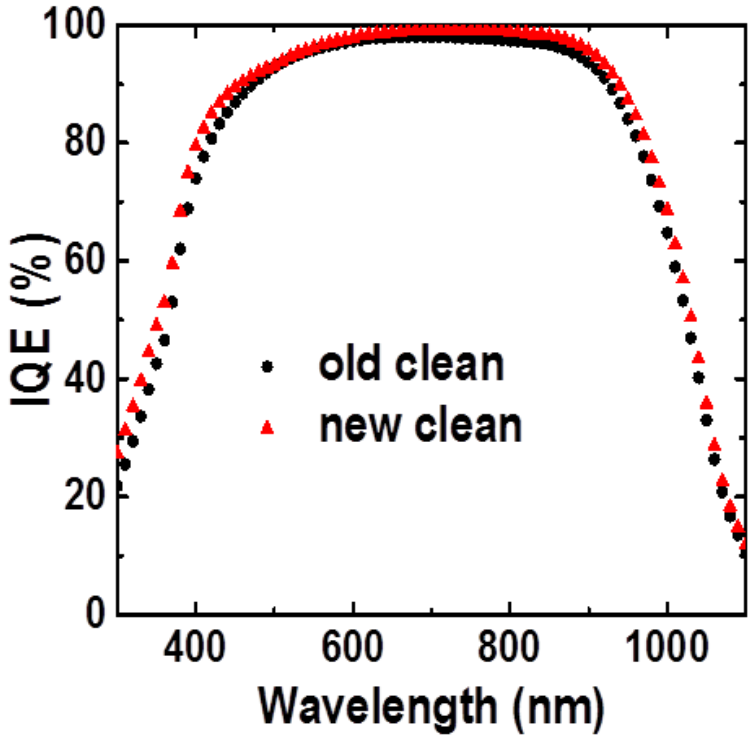


Figure 4.5: IQE response measured on textured solar cells on exfoliated ~25 μm thick substrates in the 300-1100 nm range, differentiated based on cleaning process employed.

The current-voltage results for the bulk cells are summarized in Table 4.4 and the J-V curve is shown in Figure 4.6. The corresponding IQE curves are shown in Figure 4.7. The V_{OC} of the cell which has gone through new cleaning method is 9 mV higher and the overall efficiency is improved only by 0.45% absolute (or 3% relative). The 576 mV is comparable with the expected V_{OC} that is possible to achieve with no i-layer surface passivation [61]. The improvement in short-wavelength response, as shown in Figure 4.7, is quite small. The reason that the improvement due to the new cleaning method is not as

much as that observed on cells made on exfoliated substrates is because surface recombination is a more dominant factor affecting V_{OC} in case of the much thinner ~25 μm thick substrates compared with the ~180 μm thick substrate. Consequently, such thin substrates have a very stringent requirement for surface passivation to achieve high V_{OC}. Due to a more relaxed surface passivation requirement; cells made on a thicker bulk substrate tend to show higher V_{OC} for similar surface passivation.

Cell	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
old clean	567	36.2	71.4	14.65
new clean	576	36.7	71.4	15.1

Table 4.4: J-V data summary at AM1.5 illumination for solar cells on bulk substrates (~180μm), based on cleaning process employed.

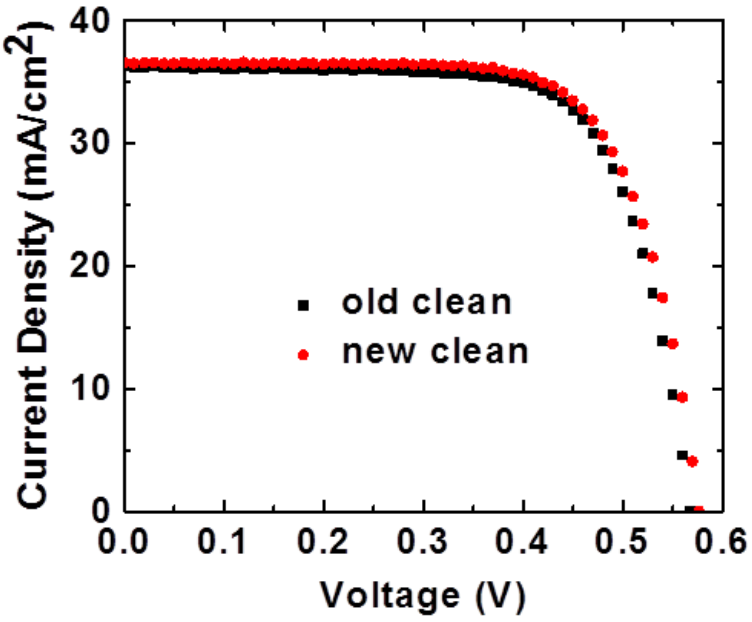


Figure 4.6: J-V characteristics at AM1.5 illumination for solar cells on exfoliated ~180 μm thick substrates, differentiated based on cleaning process employed (cell structure is identical to exfoliated cells in Figure 4.4.

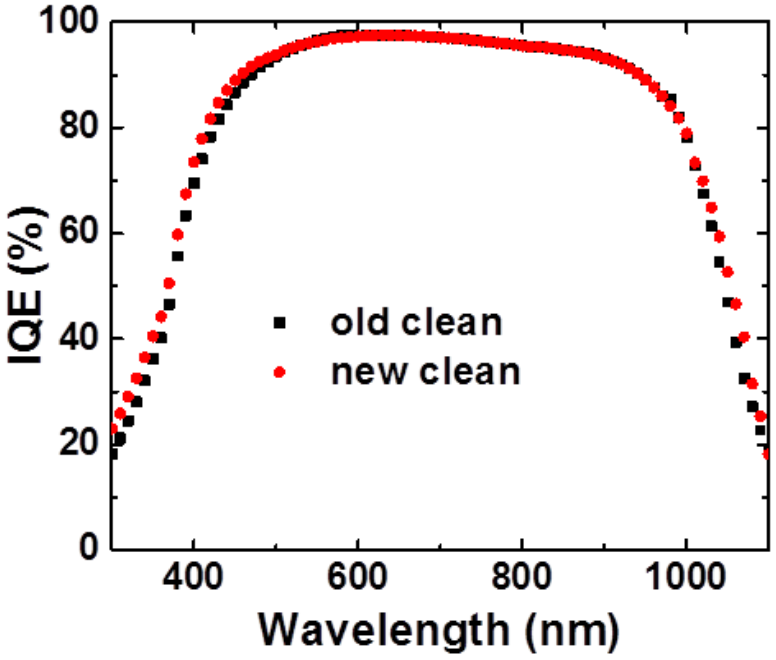


Figure 4.7: IQE response measured on textured solar cells ~180 μm thick substrates in the 300-1100 nm range, differentiated based on cleaning process employed (cell structure is identical to exfoliated cells in Figure 4.5.

The J-V and IQE characteristics shown for both exfoliated and bulk cells above are taken from a batch of four cells in each case. The average increment in efficiency is 1.35% and 0.36% for ~25 μm and ~180 μm cells respectively; the standard deviation of increment in efficiency is 0.12% and 0.09% respectively. Therefore the increase in device performance is due to new and improved cleaning procedure and not a statistical anomaly. The average and standard deviation statistics are shown for both exfoliated and bulk cells in Figure 4.8.

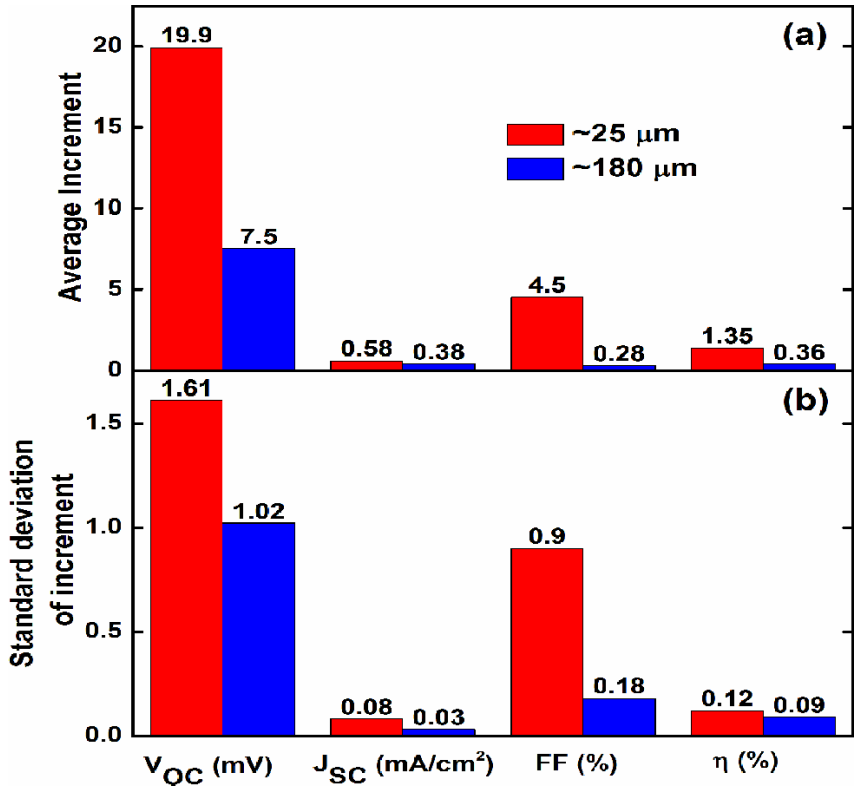


Figure 4.8: (a) Comparison of average increment in V_{OC}, J_{SC}, FF and efficiency (η) between exfoliated (~25 μm) and bulk (~180 μm) cells, (b) Comparison of standard deviation of increment in V_{OC}, J_{SC}, FF and efficiency (η) between exfoliated (~25 μm) and bulk (~180 μm) cells.

4.4 J-V CHARACTERISTICS OF SHJ CELL WITH INTRINSIC LAYER PASSIVATION

The solar cells discussed in this chapter has so far been devices without intrinsic a-Si:H passivation. The aim of including an intrinsic a-Si:H layer between doped a-Si:H and c-Si is to passivate the dangling bonds on the c-Si surface which results defect-state density in the a-Si:H/c-Si interface getting significantly reduced. The inclusion of the

intrinsic layer results in an enhancement of the V_{OC} and FF, and with an optimal thickness one can achieve a very high efficiency [62]. Passivation on textured surface using intrinsic a-Si:H is a more difficult proposition compared to passivation of planar surface. This is not only because of the roughness of the surface but also there is effectively more surface area to passivate. Therefore development of such thin film requires separate effort. Intrinsic a-Si:H deposition process development on textured surface is still in progress; currently these solar cells suffer from so-called "s-shape" J-V curve under light bias. The best case electrical performance with intrinsic a-Si:H passivation is shown in Figure 4.9. The summary of the curve is shown in Table 4.5. The curve shows "s-shape". Both the JSC and FF are reduced to give a final efficiency of 11%. However, the open circuit increased by 20 mV which can be attributed to a better passivation.

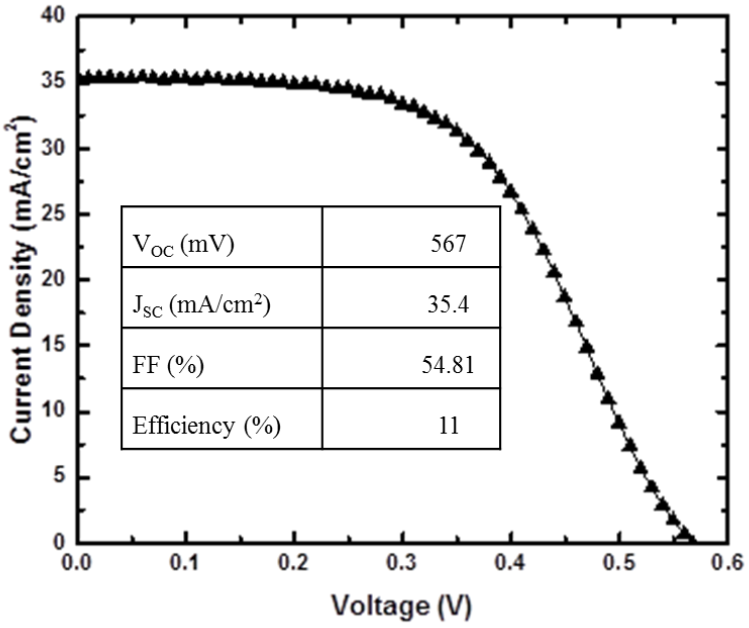


Figure 4.9: J-V data for SHJ solar with intrinsic a-Si:H passivation on textured surface.

The "s-shape" could be caused by unoptimized or too thick of a layer of intrinsic a-Si:H. This not only results in a lower J_{SC} due to the parasitic absorption losses in the a-Si:H layers but also decreases FF because of the high resistivity of the intrinsic a-Si:H, which acts as a transport barrier [63]. The low open circuit voltage could be explained by partial epi-Si growth on a-Si:H/c-Si interface. This usually happens at the sharp edges of the pyramids. When a-Si:H layer is deposited, discontinuous silicon surfaces like the sharp edges of the pyramids are like point defects and can act as growing sites. The growth is partially epitaxial and defective and hence creates more recombination sites, which can reduce the efficiency of solar cell by reducing V_{OC} [64]. In addition, the plasma assisted CVD deposition method can make plasma damage during the deposition. This plasma damage can also make epitaxial growth sites [65]. One possible solution is

using a mixture of nitric acid and hydrofluoric to iso-tropically etch the Si to round off the sharp edges [52]. Such etching process is needed to be modified for exfoliated substrates due to its metal backing.

4.5 SUMMARY

In this chapter, a cleaning process is developed to effectively remove surface contamination on textured, exfoliated ~25 μm thick substrates without degrading the back metal or introducing additional metallic or organic contamination. XPS measurements were carried out. Carbon and potassium were detected to be the main contaminants and their chemical bonding nature was evaluated. AES measurement was used to monitor the concentration changes on the surface following the different cleaning processes. Completed single heterojunction solar cells on ultrathin substrates with the new and improved cleaning process show a significant improvement in V_{OC} by 22 mV and an efficiency increase of 1.5% absolute. Using the newly developed clean, intrinsic a-Si:H passivation is included on textured surface. J-V curve shows an "s-shape" with 11% efficiency.

Chapter 5: A non-photolithographic, self-aligned method for patterning and metallization for diffused junction monofacial and bifacial cells [4]

5.1 SCREEN PRINTING TECHNIQUE AND ITS ALTERNATIVE TO METALLIZATION IN SOLAR CELLS

The most common and inexpensive method of metallization in solar cells is screen printing technique. The basic workings of screen printing are as follows.

- Instead of using pure metal, a silver based paste comprising 70-85% by weight silver powder, glass frits, and organic components is used. The glass frits helps melting the dielectric layer during firing and promotes adhesion to Si. The organic component acts as a solvent to use the mix of metal powder and glass frits as paint.
- A screen made of stretched fabric consisting mesh with stencil design held in a frame is used for pattern transfer. The screen is flooded with the paste.
- The Si substrate is aligned with design of the screen.
- A squeegee with a fixed, flexible resilient blade is used to press the screen physically in contact with the wafer to transfer the paste through stencil opening on to the surface to create the pattern.

[4] Certain parts of this chapter are reproduced from the following two conference articles. All the authors contributed to either experimental or technical or both the aspects.
1) **S. Saha**, R. A. Rao, L. Mathew, M. Ainom, S. K. Banerjee, *A Novel Non-Photolithographic Patterning Method for Fabricating Solar Cells*, Proceedings of 38th IEEE PVSC, pp. 2250-2253, Austin, 2012.
2) **S. Saha**, R. A. Rao, L. Mathew, M. Ainom, S. K. Banerjee, *A Novel Low-Cost Method for Fabricating Bifacial Solar Cells*, Proceedings of 39th IEEE PVSC, pp. 2268-2271, Tampa, 2013.

- After deposition the substrate is made to go through a drying process to dissolve organic solvent and then a rapid thermal annealing process or "firing" to diffuse the metal through dielectric and create contact.

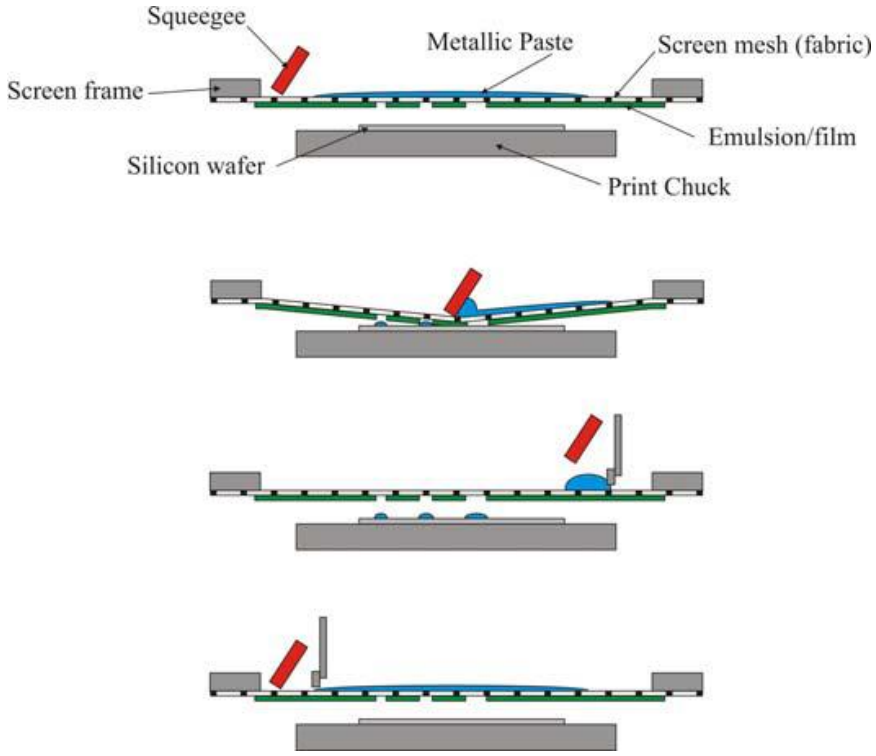


Figure 5.1: Schematic drawing of the screen printing process [66].

It is evident why screen printing is a preferred way to form contact as no photolithography or fine alignments are necessary. The screens could be reused to carry out printing on multiple wafers. However the problems associated with screen printing as discussed in Chapter 1 is making Industry move toward cheaper alternatives such as Ni or Cu with thin Ni diffusion barrier. The Ni is grown with the help of electroless plating or ink-jet printing of metal paste, whereas Cu is plated using electroplating. In order to achieve this, the ARC layer needs to be patterned and etched, which are extra steps in the

process flow that are undesirable. We propose a low-cost method for patterning and metallization for solar cell fabrication purposes. We keep a shadow mask with a metal grid pattern in contact with the surface of the substrate in the PECVD chamber for SiN_x deposition. This leaves us with a patterned surface to selectively grow metal at low temperature on exposed doped Si surface using electrochemical deposition. We have used Ni, which has low barrier height, which eventually leads to a low contact resistivity ~10.5μΩ.cm [67]. The concept of electrochemical metal growth to form electrodes for solar cells has been demonstrated in the literature before. For example, the extra steps for pattern and etch could be laser ablation of SiN_x [68], [69], inkjet printing of photoresist and etch [70], laser chemical processing [71], or simply photolithography and etch [72].

Some of these alternative methods that are gaining traction are discussed briefly.

- **Laser ablation of ARC for plated contact:** A dry laser is used to ablate SiN_x layer to expose the doped Si underneath. A subsequent damage etch and second diffusion with PSG etch is required afterwards. SiN_x is then used as hard mask to selectively grow Ni metal using electro-deposition. The contact could further be improved by electroplating Cu on Ni [73], [74], [75]. A schematic of the methodology is shown in Figure 5.2.

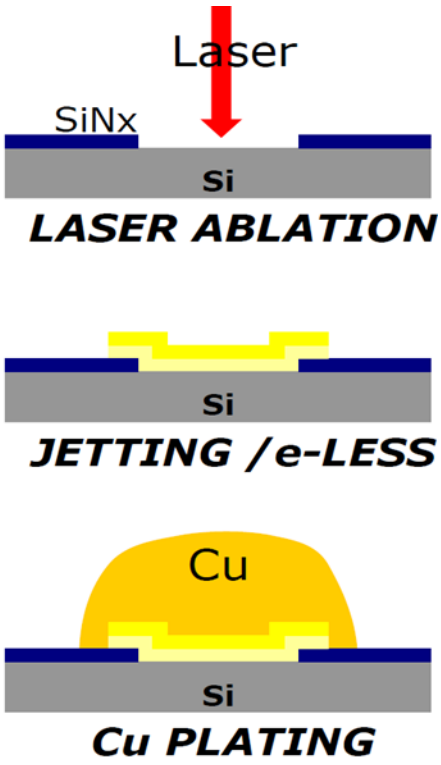


Figure 5.2: Laser ablation used to etch ARC to expose doped Si to selectively electroplate metal [76].

- **Laser Chemical Processing (LCP):** In this method two different pulse lasers are used. The first one used to ablate the ARC to expose the lightly doped emitter. A second one, which is a chemical liquid jet-guided laser, performs local diffusions at high speed and accuracy to facilitate electro-deposition. Phosphoric acid (H_3PO_4) is used as a liquid carrier which is the source for the dopants [71]. The entire process is done without the need of masking or any high-temperature step of the entire wafer. A cartoon of the process is shown in Figure 5.3. The advantage of this method over the last one is that the opening of the ARC and the

doping of the groove is done in one step without needing to use any wet chemical etch to remove damage after the laser process and also remove post diffusion PSG. Thus metal seed layer deposition and contact thickening via electroplating can follow right after LCP. In this way, two wet etching steps (damage etch and PSG etch) and one high temperature step (second diffusion) are saved.

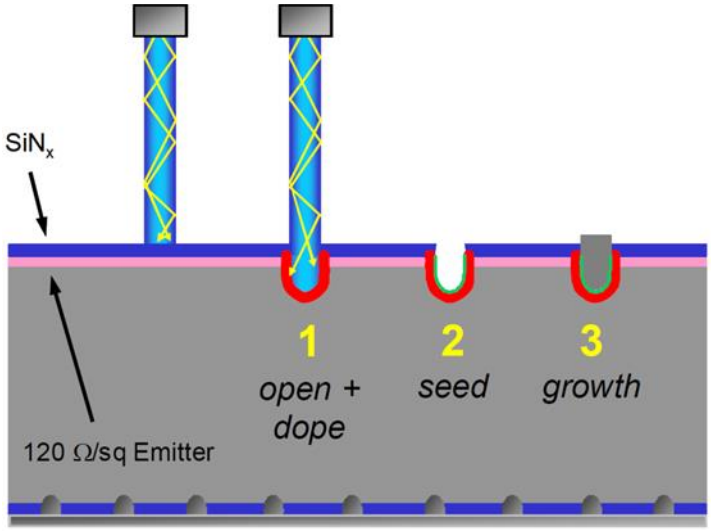


Figure 5.3: LCP assisted ablation and local diffusion doping followed by seed layer deposition and metal contact thickening via electroplating [71].

- **Screen printing of photoresist and etch:** In this method photoresist is screen printed on top ARC layer. The photoresist is used as a hard mask to etch away the exposed ARC layer with proprietary etching solution [70]. The seed layer is grown using electroless process. The contact is further thickened by electroplating. The process flow is shown in Figure 5.4.

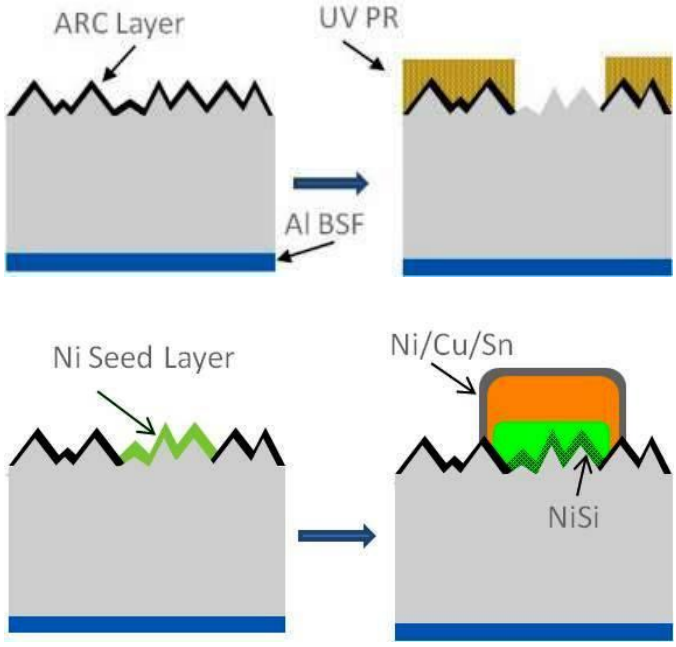


Figure 5.4: Screen printing of etch resist to define the contact pattern and etching away exposed ARC layer. Followed by seed layer growth and contact thickening using electro-depostion [70].

All of the processes described above require at least a couple of extra steps to pattern/etch the surface to use the Anti-Reflective Coating (ARC) as a hard mask to selectively grow the metal. In our approach, we get rid of that extra step of pattern formation, and metallize the front surface at a low temperature, thereby reducing cost of manufacturing. This process flow could particularly be useful for fabricating solar cells with diffused junction n^+pp^+ structures requiring metallization for global/selective emitters or locally doped silicon regions. Moreover, this approach could come in handy in fabricating bifacial cells where metallization of both sides could be done simultaneously. Bifacial solar cells, unlike monofacial ones, can collect sunlight from both sides and convert it into electrical power. The sunlight incident on the front side and

the reflected sunlight from ground (diffuse sunlight) or intentionally designed glass panels collected at the rear side are the sources of photo-generated currents in bifacial solar cells. Bifacial cells, therefore, effectively can have similar structures to conventional solar cells, with some minor modifications at the rear side of the cell, and still can potentially produce up to 50% additional power output [77]. Since they generate more power, they have a higher power-to-material-weight ratio than other commercial cells making them more cost effective. Besides using bifacial cells instead of monofacial ones for conventional uses, a broad spectrum of applications is possible; applications in places such as for shop windows, private homes, offices and industrial buildings [78]. In this chapter we demonstrate viability of our process flow in both monofacial and bifacial cells.

5.2 A NON-PHOTOLITHOGRAPHIC APPROACH TO CREATE PATTERN AND USE ARC LAYER AS HARD MASK TO SELECTIVELY GROW METAL USING ELECTRO-DEPOSITION

A schematic of the process flow for diffused junction monofacial and bifacial cells are shown in Figure 5.5 and 5.6 respectively. A 200μm thick p-type mono-crystalline Si wafer is cleaned and textured using a KOH-based chemistry. For monofacial cells N-type dopants on the front surface and for bifacial cells both n-type on the front surface and p-type dopants on the back surface of the textured wafer are ion implanted and annealed in a rapid thermal furnace at 1100°C to activate the dopants and create junction. SiN_x is selectively deposited on the front surface using a shadow mask

with metal grid pattern in a PECVD chamber. The nitride not only passivates the surface, but also acts as an ARC. After this step only the doped Si surface for metal contact is exposed. Same process is repeated on the back surface by flipping over the substrate in case of bifacial cells. However, for monofacial cells instead of carrying out another round of deposition in the PECVD chamber, on the rear surface BSF is formed by applying Al5130V aluminum conductor paste (from Ferro Corporation) on the backs surface and firing at 850°C in a rapid thermal process (RTP) chamber. After this, in case of both monofacial and bifacial cells, the samples are then cleaned to remove organic and metal contaminants and treated with hydrofluoric acid (HF) to deglaze the exposed Si surface. After that, they are introduced in an ammonia based electroless Ni plating solution (heated to 90-95ºC) from Transene, called ENPAT, for a short period of time. This was done to form a thin seed layer of Ni on top of the exposed Si. Nickel grown in this manner is self-limiting after some time. Therefore, in order to increase the thickness of the metal further, Ni is electroplated using Technic chemistry. A typical grid patterned surface before and after metallization is shown in Figure 5.7.

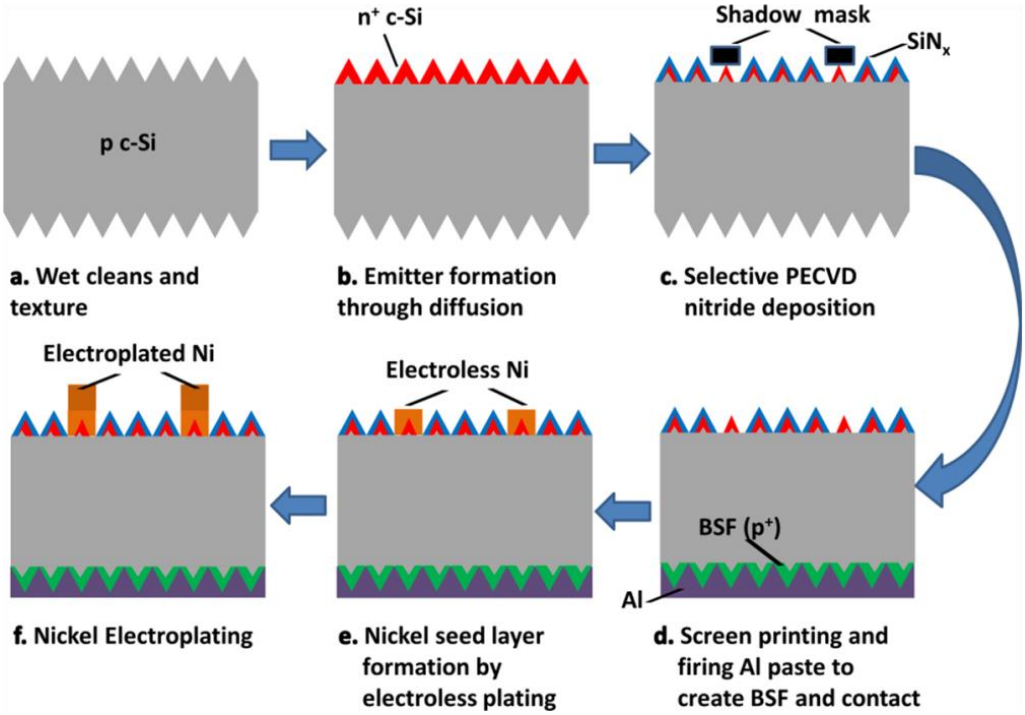


Figure 5.5: Process flow for fabricating monofacial solar cell using non-photolithographic patterning of silicon nitride and self-aligned metallization, aided by electroplating**.**

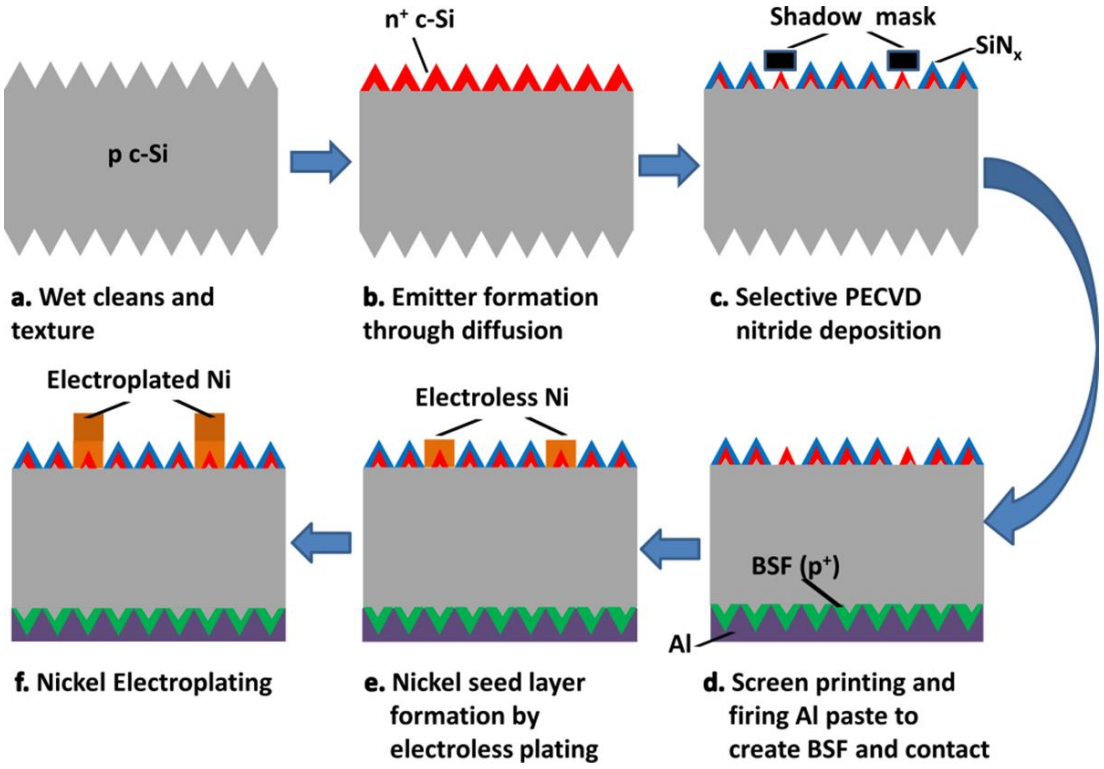
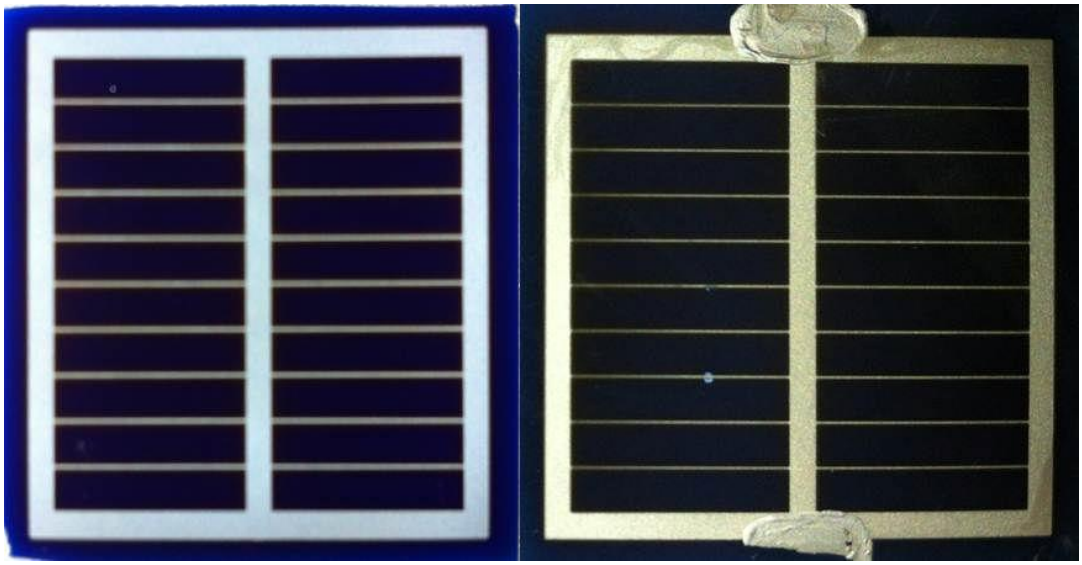


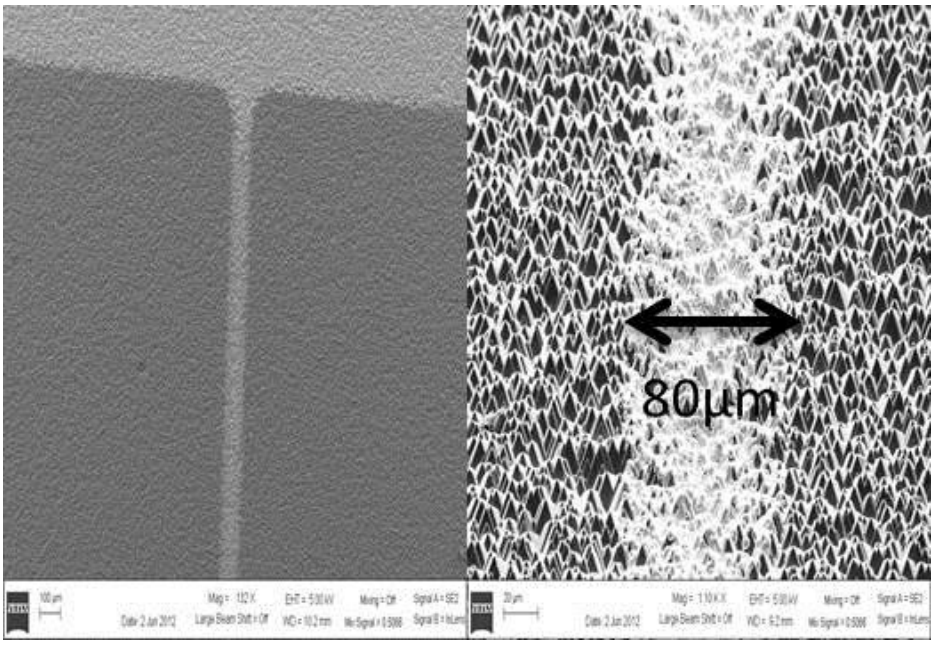
Figure 5.6: Process flow for fabricating bifacial solar cell using non-photolithographic patterning of silicon nitride and simultaneous metallization, aided by electroplating**.**



(a) (b)

Figure 5.7: (a) Pattern achieved on SiN_x using shadow mask in PECVD chamber, (b) completed solar cell with electroplated Ni metal for front contact.

The minimum finger width of the electroplated front surface metal electrode is 80 μm in this case, as shown in the SEM image in Figure 5.8. A smaller size-width can potentially be obtained with shadow mask with finer feature size. The same shadow mask is used create pattern on both surfaces for bifacial cells. However, a more optimized cell would probably require different metal coverage on front and rear surfaces.

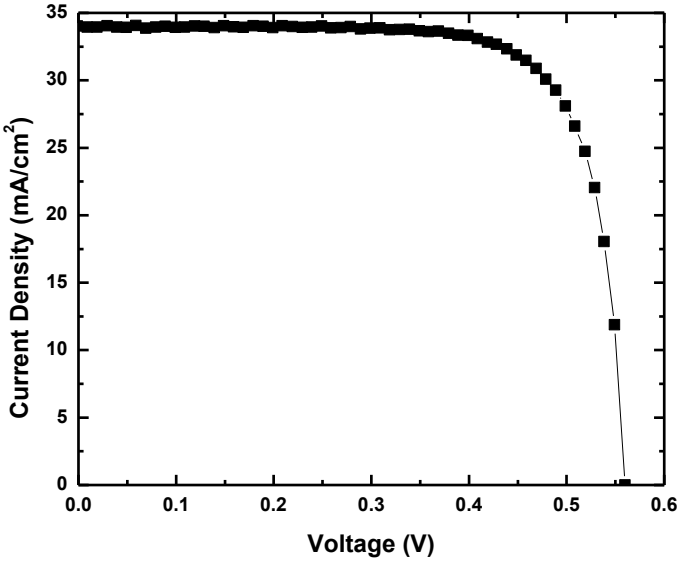


(a) (b)

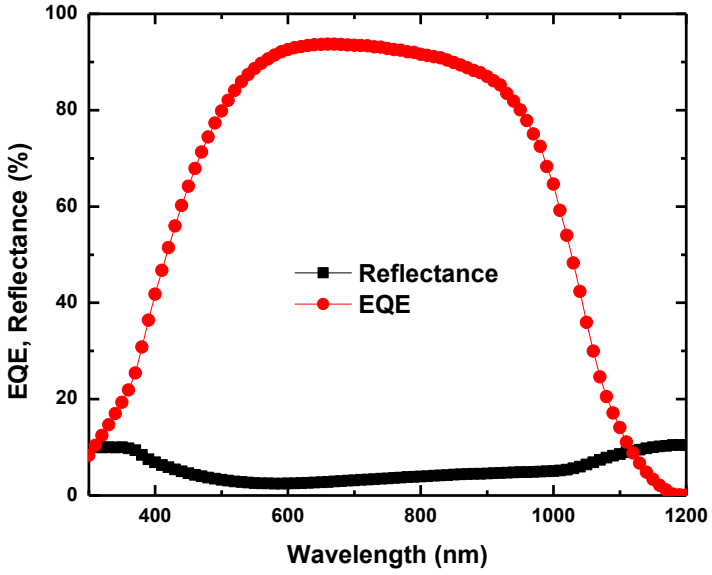
Figure 5.8: (a) SEM image (at 132x) of pattern formed on the front surface of the solar cell after SiN_x is deposited selectively in the PECVD chamber, (b) SEM image (at 1.10Kx) of a metallized finger after electroplating; finger width is 80 µm.

5.3 ELECTRICAL DATA FOR BOTH MONOFACIAL AND BIFACIAL CELLS

The measured J-V data and EQE and reflectance data capture cell performance of a monofacial cell is shown in Figure 5.9. The low V_{OC} number could be attributed to sub-optimum SiN_x passivation of the front surface, due to a limitation in our PECVD process. A QSSPC study in determining the quality of SiN_x deposited in the PECVD chamber reveals surface recombination velocity (SRV) on a high lifetime float zone wafer to be >1500cm/s, whereas, PECVD-deposited nitride should provide a passivation with SRV <100cm/sec.



(a)



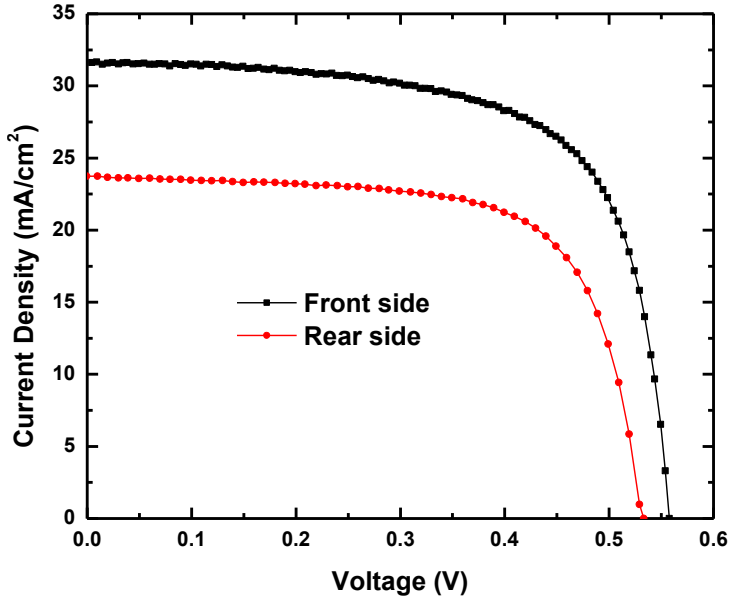
(b)

Figure 5.9: (a) I-V curve for solar cell with area 7.25cm2. V_{OC}=560mV, J_{SC}=34mA/cm2, Fill Factor (FF)=76%, Efficiency=14.5%, (b) percentage EQE, Reflectance vs. wavelength plot.

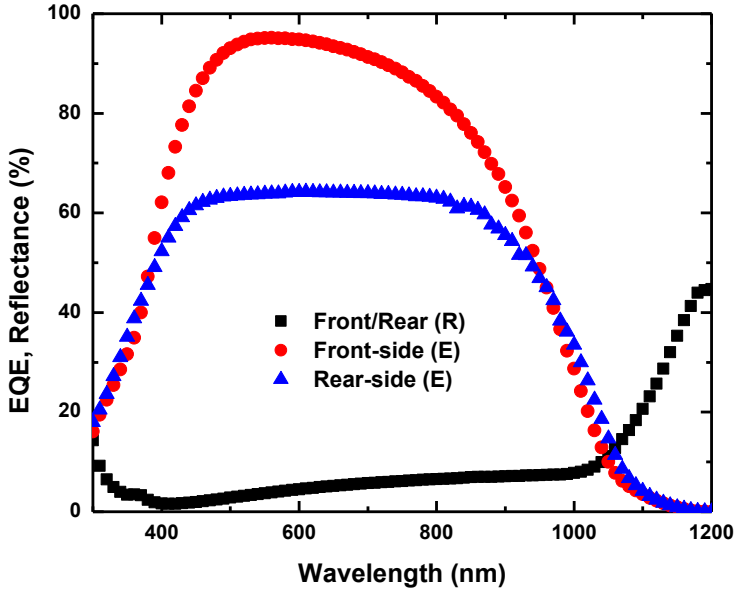
Figure 5.9 shows J-V characteristics and EQE data collected from both sides of a bifacial cell under illumination. Table 5.1 shows the collection efficiencies from both surfaces under AM1.5G 1 sun illumination. It can be observed that recombination at rear side high-low junction is higher than at front surface pn junction. This is because bulk recombination is a limiting factor here. The UV and blue response can be enhanced by improving the quality of SiN_x film to provide better surface passivation, and by reducing the surface doping density to reduce Auger recombination. Some of the light is not effectively collected in long wavelength regime due to lack of a metal back surface reflector (BSR) completely covering the surface.

Cell	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
Front Surface	558	31.6	68	12
Rear Surface	533	23.7	69	8.66

Table 5.1: J-V data summary at AM1.5 illumination for front and rear surface of the bifacial cell.



(a)



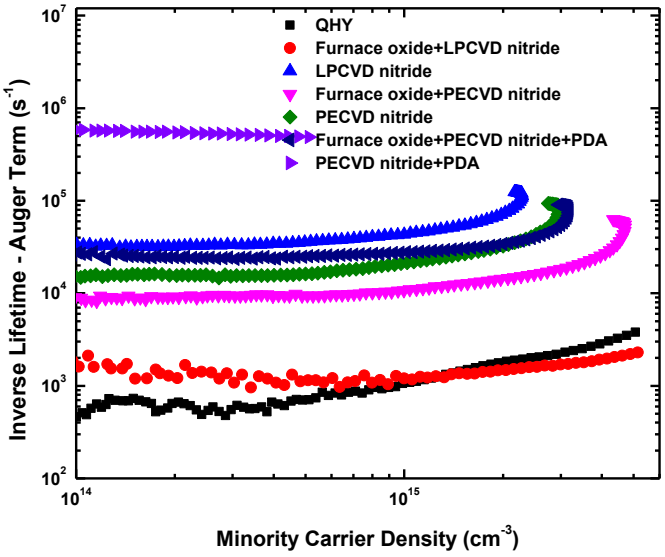
(b)

Figure 5.10: (a) J-V characteristics from both surfaces under AM1.5G illumination (b) EQE and reflectance of both surfaces of the bifacial cell.

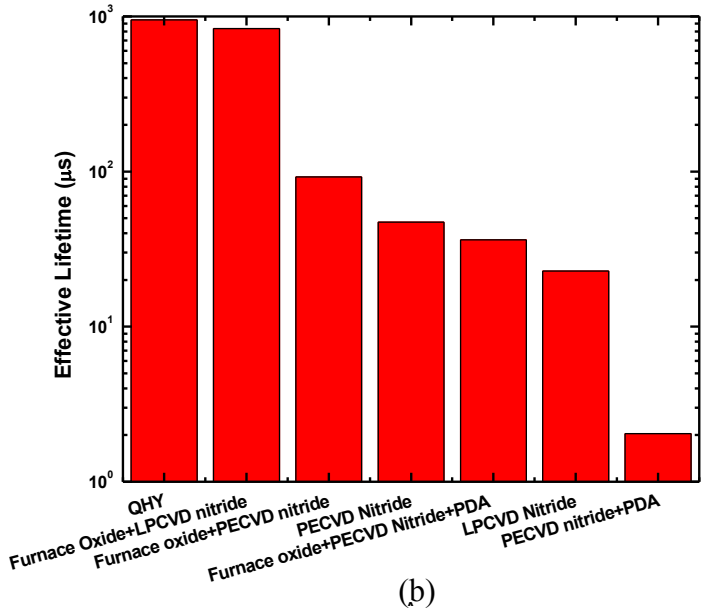
5.4 INVESTIGATION OF FACTORS DETERMINING THE PERFORMANCE OF THE CELLS

In order to determine the main factor(s) in low device performance in the cells described above we have measured Suns_V_{OC} after completion of each process step and found slight V_{OC} degradation after SiN_x passivation. An even bigger drop in V_{OC} is observed after electroless plating, which could be attributed to pinholes in PECVD SiN_x causing parasitic plating on nitride. In order to confirm that passivation quality in combination with electroless plating is the root cause of low device performance we carried out an experiment. In this experiment, we tried different kinds of passivation schemes on low resistivity p-type float-zone wafers to assess quality of passivation by measuring effective lifetime using contactless QSSPC method. Results shown in Figure 5.11 (a) and (b) shows, not surprisingly, furnace oxide (dry thermal oxide) with LPCVD nitride ARC is the best possible passivation option after quinhydrone/methanol (QHY/ME). In some of the cases shown in the figure, PECVD/LPCVD SiN_x is annealed at 850ºC in a furnace (PDA). This was done to make the SiN_x denser by reducing pinholes and making it less susceptible to parasitic plating. However, as evident by the Fig. 13(a) and (b) the anneal causes the effective lifetime to go down significantly. Some of the passivated samples showing higher effective lifetime (i.e. better quality passivation) is then put into electroless plating solution at 90º-95ºC for 2 minutes. Effective lifetime of these selected samples were measured again (Figure 5.11 (c)) to see degradation in lifetime only in samples where the SiN_x is not dense enough, confirming that parasitic plating on SiN_x film is indeed a problem, and the solution is a denser film

which also passivates well. For our current process flow LPCVD nitride is not a viable option. However, a better quality SiN_x deposited at an industry standard PECVD chamber might solve this problem.

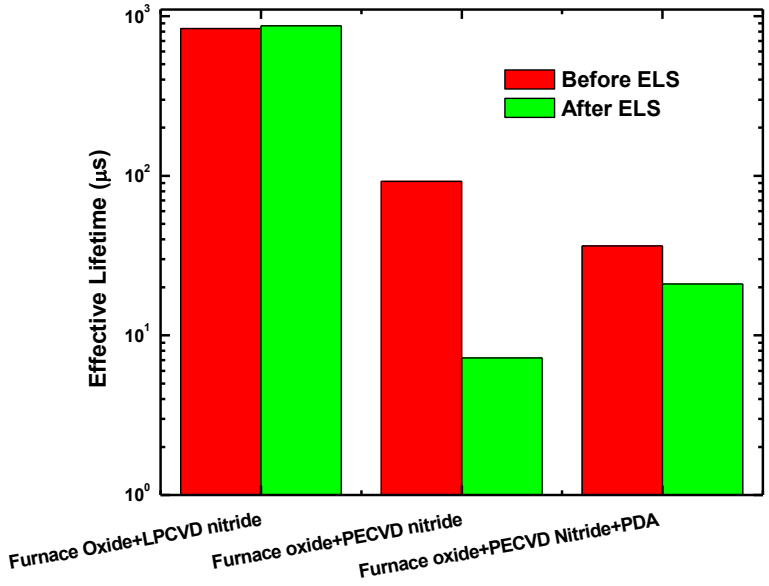


(a)



(b)

(**Figure 5.11** continued next page)



(c)

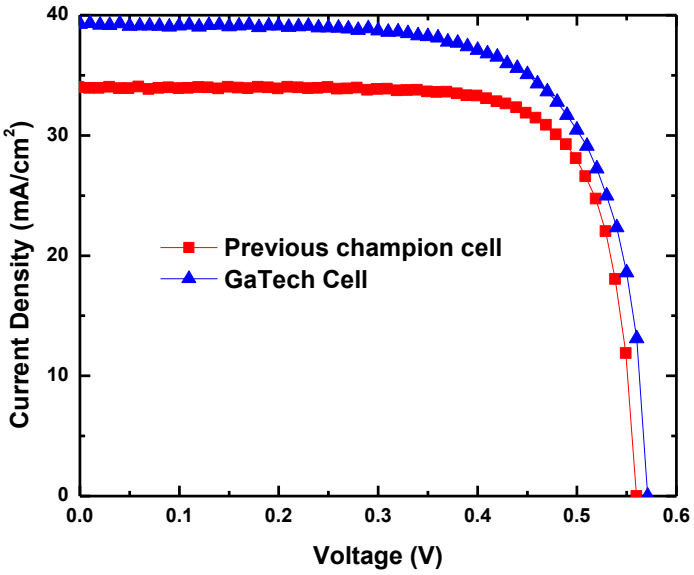
Figure 5.11: (a) Auger corrected inverse lifetime vs. minority carrier density, (b) effective lifetime, (c) post electroless plating effective lifetime for different passivation schemes.

In order to further verify that an improved quality of SiN_x will indeed enhance the device performance, the previous champion diffused junction monofacial cell was compared with a solar cell with improved nitride film quality. The improved thin film is obtained by SiN_x deposited in a PECVD chamber dedicated for high efficiency solar fabrication at Georgia Institute of Technology. The large area substrates have full face SiN_x on one side and screen printed Al on the other side for BSF and electrical contact. The SiN_x is then patterned on multiple ~8 cm^2 die area using photolithography and etched using BOE while the Al at the back is masked by photoresist. The individual patterned

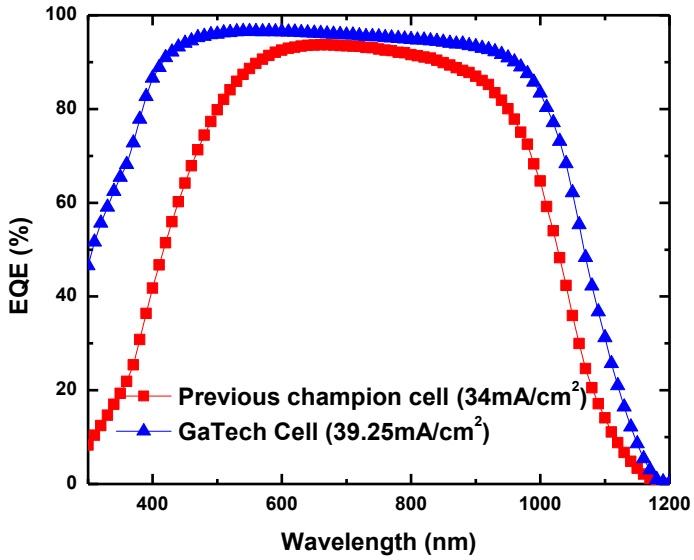
areas were then cleaved and metallized as before. The results are shown in Table 5.3 and Figure 5.12. With gradual improvement in film quality an improvement in overall device performance have been observed. However, the V_{OC} improvement is not as drastic (12 mV) as before, probably because of introduction of micro-cracks while cleaving the substrates to separate the devices. This is mostly because a ~180 μm thick, large area Si substrate with very thick layer of Al paste screen printed at the back does not cleave very clean. However, at a smaller level we have a clearly improved device as evident by the EQE curve 5.12 (b). The short wavelength response drastically improved due to improved little or no parasitic plating and improved surface passivation. This effect is observable because of the localized nature of the EQE measurement.

Cell#	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)
Previous champion cell (litholess)	560	34	76	14.5
GaTech Cell (litho)	572	39.25	71	15.8

Table 5.2: J-V data summary at AM1.5 illumination for three devices, differentiated based on different passivation schemes. [Note: "litholess" implies use of shadow mask method. "litho" means use of traditional photolithography.]



(a)



(b)

Figure 5.12: (a) J-V characteristics , (b) measured EQE of cells completed with different passivation schemes.

5.5 SUMMARY

In this chapter, a novel method to fabricate semiconductor devices using a shadow mask that allows selective deposition of PECVD layer while forming a metal grid pattern exposing doped silicon regions is proposed and demonstrated. The exposed regions then act as seed layers for selective metallization by a process such as electro-deposition. Diffused junction monofacial and bifacial solar cells were fabricated on c-Si substrates using this method. Ni was electrochemically grown to form front surface electrode. The feature size of metal electrodes formed in this way is 80 μm and could potentially be narrowed down to smaller size-width. The cells fabricated utilizing this method, were suboptimal in performance. Part of the low performance of the cell is attributed to poor quality of the passivation layer and the post deposition annealing to reduce pinholes in deposited SiN_x layer to prevent parasitic plating. With improved surface passivation improvement in device performance was observed.

Chapter 6: Conclusion

6.1 SUMMARY

Despite the rapid growth in manufacturing volume and significant drop in module selling price, the relatively high cost associated with solar power generation is one of the main obstacles to widespread global use of solar electricity. Reduction of manufacturing costs by using more inexpensive processing techniques and materials is expected to be the key for making solar industry mainstream. Though there are several emerging technologies involving different materials to address these issues, crystalline silicon (Si) still retains 80% of the total market share of solar cell industry. Thus, cost reduction in crystalline Si solar cells remains an important area of interest. This work has tried to address the cost reduction issue by proposing and demonstrating two different approaches.

In the first approach, a novel exfoliation method is introduced as a kerf-less way of obtaining ultra-thin (~25 μm) monocrystalline and flexible substrates. These substrates are obtained by bonding a thick electroplated Ni layer with a thick (>200 μm) substrate and making it go through a thermal cycling process to generate compressive stress. Then with the help of a mechanical wedge a crack is initiated and propagated along a subsurface plane utilizing the residual strain in the bi-material to obtain large area thin substrates. The exfoliated substrate has metal backing which not only provides mechanical support but also act as a back surface reflector (BSR) and an electrical contact. Not only this type of substrates addresses the issues like yield and breakage that

are associated with such thin substrates but also one surface of the substrate can be completely processed while it is still in a thick wafer form. The Ni metal is not required to be etched off to complete the cell and integrate it in a module. The residual parent wafer can be recycled multiple times to obtain more and more exfoliated substrates. This is the reason the material cost can be drastically reduced and bring the overall cost of fabricating cells down.

There are few challenges that arise because of the substrates having Ni metal backing and an inherent curvature due to residual strain, such as process uniformity, surface preparation, implementation of light trapping, optimizing thin film deposition conditions, front side metallization, module reliability, etc. In Chapters 3 and 4 some of these issues have been addressed. Process optimization has been done to increase the V_{OC}, J_{SC}, and FF with an ultimate goal of fabricating high efficiency cells in a manufacturable way.

In the second approach, an alternative to silver as metal contact for solar cell fabrication has been explored. A cheaper alternative silver screen printing is electro-deposition of Ni metal on doped Si surface. However, this approach requires an additional step of patterning and etching to open the ARC layer. This means a disruptive yet cheap alternative process to photolithography has to be introduced in a turnkey line. However, in our approach an inexpensive reusable shadow mask can be used during PECVD SiN_x deposition. This enables selective deposition of the ARC layer with exposed doped Si in a metal grid pattern. Consequently, the ARC layer can be used as a hard mask to selectively and in a self-aligned way to grow a thin layer of Ni on doped Si

surface using electroless plating. This thin metal layer could be used as a seed layer to further thicken up the contact using electroplating. This method could be useful for diffused junction n^+pp^+ structured solar cells; especially bifacial cells, where each surface needs to be processed individually thereby adding cost to the process flow. Adopting this method can simultaneously metallize both sides of the cell. Using this novel approach monofacial and bifacial cells have been fabricated and characterized. The main factors limiting the device performance are determined.

6.2 SUGGESTIONS FOR FUTURE WORK

All the work reported in Chapters 3, 4, and 5 can be further optimized to reach the goal of efficiency 20% or greater. The work on heterojunction cells on exfoliated substrates can be improved by optimizing the intrinsic a-Si:H on textured surface. Since the substrates are ultra-thin, surface passivation requirement is very stringent. Therefore, for a single heterojunction cell it is difficult to obtain high V_{OC}, since part of the c-Si substrate at the back is directly in contact with metal. The metal/c-Si contact area act as recombination centers. A better approach to achieve high efficiency performance is fabricate dual heterojunction or so called "HIT" structure on these substrates. In this way both surfaces will be covered with intrinsic a-Si:H layer. Some initial work on implementing HIT structure on exfoliated substrates have been already reported [79]. However, those cells do not have front surface texture and the cells with intrinsic a-Si:H passivation have "s-shape" problem in their J-V characteristics.

Interdigitated Back Contact (IBC) Cells have a two dimensional structure where the emitter and BSF regions are formed at the back. Therefore the metal contacts are all

in the back side of the cell. The front side has no metal. The structure is shown in Figure 6.1. IBC cells have the advantage of zero shading loss and heterojunction (HJ) solar cells have the capability to achieve high quality surface passivation at low thermal budget. Combining these two approaches can potentially make a solar cell achieve efficiencies >25% [80]. Since back contact solar cells benefit from high bulk lifetime [81], it is imperative to fabricate these kinds of cells on high quality substrates. That is why very thin substrates, where bulk recombination is negligible are desirable so that high efficiency could be achieved even with a very low quality and low cost substrate. Therefore to combine advantages from all of these approaches and fabricate HJ-IBC devices on ~25 μm thick monocrystalline substrates could potentially give high conversion efficiency at a low cost.

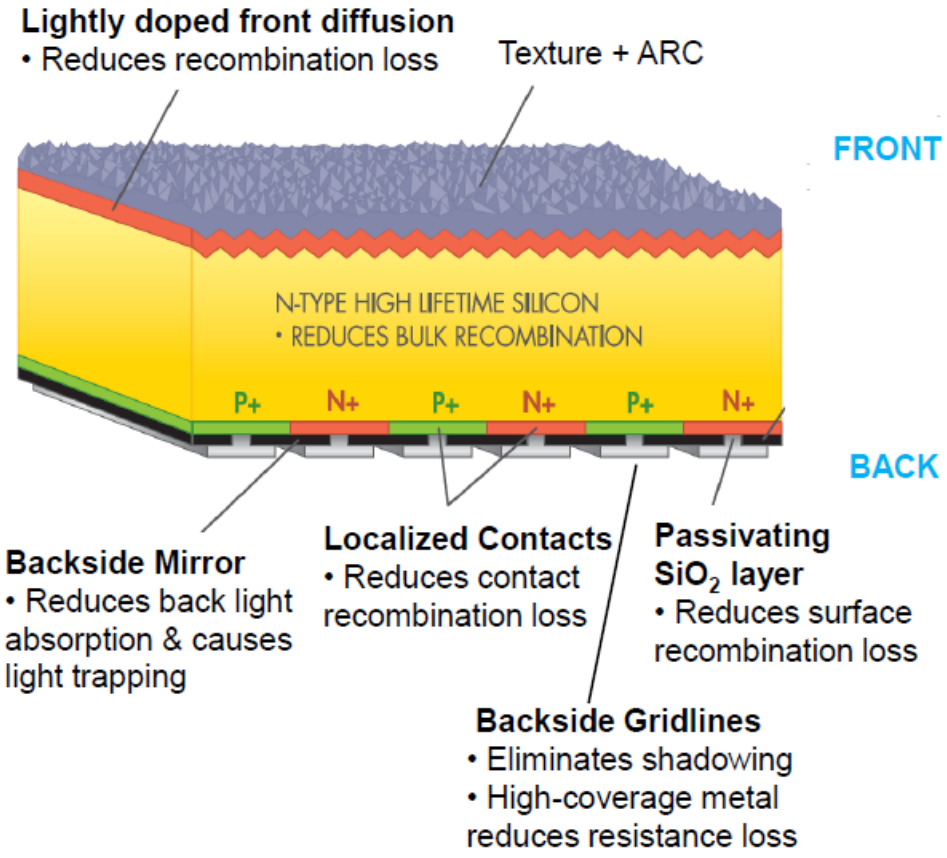
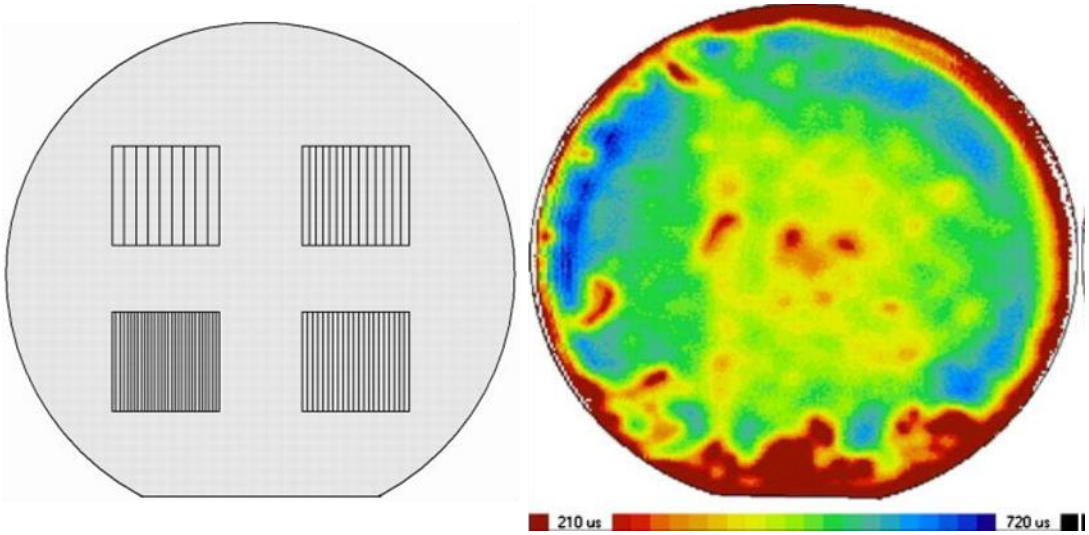


Figure 6.1: Schematic of a IBC solar cell [9].

The non-photolithographic, self-aligned method described can further be optimized by using high quality PECVD SiN_x which provides excellent passivation as well as serves as an efficient hard mask to prevent parasitic plating. Another concern in this approach is degradation of surface passivation due to introduction of a shadow mask in PECVD chamber. The shadow mask approach has advantage over other approaches in that it does not cause any surface damage by destructive process as compared to other processes. Thus taking out damage removal etch step from the process flow. However, whether the presence of shadow mask causes any lifetime degradation around the pattern area is another question. Knorz *et al*. [73] carried out a lifetime map study using

microwave photoconductive decay (MW-PCD) method in order to find out if the most optimized lase ablation process to open up ARC layer causes lifetime degradation in the overall surface area or not (as shown in Figure 6.2). A similar study could be carried out for a patterned Si substrate using the shadow mask approach to answer the concern about overall surface passivation quality post PECVD SiN_x deposition and pattern formation.



(a) (b)

Figure 6.2: (a) Laser ablated test pattern used for MW-PCD lifetime scan mapping, (b) MW-PCD scan map for a planar, SiN_x coated Si surface patterned with the most optimized laser ablation method [73].

BIBLIOGRAPHY

[1] "The End Of Fossil Fuels." [Online]. Available: https://www.ecotricity.co.uk/our-green-energy/energy-independence/the-end-of-fossil-fuels. [Accessed: 20-Jul-2014].

[2] National Research Council, "Advancing the Science of Climate Change," Washington D.C., 2010.

[3] J. Carter, "The President's Proposed Energy Policy," in *Vital Speeches of the Day, Vol. XXXXIII*, Washington D.C., 1977, pp. 418–420.

[4] U. S. E. I. Administration, "Annual Energy Outlook," Washington, DC, 2014.

[5] "Renewable Energy Cost Analysis - Solar Photovoltaics," 2012.

[6] E. Cartlidge, "Bright outlook for solar cells," *Physics World*, pp. 21–24, Jul-2007.

[7] A. Rockett, "Photovoltaics 101/201 Introduction to Photovoltaics." IEEE, Austin, TX, p. 28, 2012.

[8] F. Colville, "Can PV technology change before 2015?," *PV Tech*, 2014. [Online]. Available: http://www.pv-tech.org/guest_blog/can_pv_technology_change_before_2015. [Accessed: 20-Jul-2014].

[9] R. Swanson, "The Silicon Photovoltaic Roadmap," 2011. [Online]. Available: http://energyseminar.stanford.edu/sites/all/files/eventpdf/11-11-14 Swanson.pdf. [Accessed: 20-Jul-2014].

[10] M. a. Green, a. W. Blakers, E. M. Keller, and S. R. Wenham, "High-efficiency silicon solar cells," *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 679–683, May 1984.

[11] T. O. M. Tiedje, E. L. I. Yablonovitch, G. D. Cody, and B. G. Brooks, "Limiting Efficiency of Silicon," *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 711–716, 1984.

[12] S. Bowden, "From the Valley of Death to the Golden Decade: Crystalline Silicon Solar Cells from 10 to 100 microns," in *19th Workshop on Crystalline Silicon Solar Cells and Modules*, 2009, pp. 192–195.

[13] L. Mathew and D. Jawarani, “Method of forming an electronic device using a separation-enhancing species,” 7,749,8842010.

[14] J. L. Hernández, M. Alemán, C. Allebé, T. Bearda, J. John, I. Kuzma, H. Philipsen, N. Posthuma, S. Rodet, and J. Poortmans, “The Way Towards Front Side Metallization By Copper-plating : What We Can Learn From Microelectronics,” in *2nd Workshop on Metallization for Crystalline Silicon Solar Cells*, 2010, p. 4.

[15] D. Kray, N. Bay, G. Cimiotti, N. Fritz, M. Glatthaar, S. Kleinschmidt, A. Lösel, O. Lühn, J. Schramm-Moura, A. Rodofili, A. Träger, H. Kühnlein, and H. Nussbaumer, “Reducing Ag cost and increasing efficiency. Multicrystalline silicon solar cells with direct plated contacts exceeeding 17% efficiency,” in *26th European Photovoltaic Solar Energy Conference*, 2011, pp. 1199 – 1202.

[16] “International Technology Roadmap for Photovoltaic (ITRPV) 2013 Results,” Berlin, Germany, 2014.

[17] “International Technology Roadmap for Photovoltaic (ITRPV) 2013 Results,” Berlin, Germany, 2014.

[18] K. Adolf, M¨. Konstantin, T. Holdermann, R. E. Schlosser, and S. Sterk, “Thin monocrystalline silicon solar cells,” *IEEE Trans. Electron Devices*, vol. 46, no. 10, pp. 2055 – 2061, 1999.

[19] A. C. Pan, C. del Cafiizo, and A. Luque, “Effect of thickness on bifacial silicon solar cells,” in *Spanish Conference on Electron Devices*, 2007, pp. 234–237.

[20] A. Wang, J. Zhao, S. R. Wenham, and M. A. Green, “21.5% Efficient thin silicon solar cell,” *Prog. Photovoltaics Res. Appl.*, vol. 4, pp. 55–58, 1996.

[21] A. Goodrich, P. Hacke, Q. Wang, B. Sopori, R. Margolis, T. L. James, and M. Woodhouse, “A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs,” *Sol. Energy Mater. Sol. Cells*, vol. 114, pp. 110–135, Jul. 2013.

[22] F. Dross, J. Robbelein, B. Vandevelde, E. Van Kerschaver, I. Gordon, G. Beaucarne, and J. Poortmans, “Stress-induced large-area lift-off of crystalline Si films,” *Appl. Phys. A*, vol. 89, no. 1, pp. 149–152, Jul. 2007.

[23] E. Wesoff, “SiGen Targets Thin Silicon Wafers With Ion Implant Technology for Solar PV,” *GreenTech Solar*, 2012. [Online]. Available:

http://www.greentechmedia.com/articles/read/SiGen-Targets-Thin-Silicon-Wafers-with-Ion-Implant-Technology-for-Solar-PV. [Accessed: 20-Jul-2014].

[24] J. H. Petermann, D. Zielke, J. Schmidt, F. Haase, E. G. Rojas, and R. Brendel, "19 % efficient and 43 µm - thick crystalline Si solar cell from layer transfer using porous silicon," *Prog. Photovoltaics Res. Appl.*, vol. 20, pp. 1–5, 2012.

[25] R. . Bergmann, C. Berge, T. . Rinke, J. Schmidt, and J. . Werner, "Advances in monocrystalline Si thin film solar cells by layer transfer," *Sol. Energy Mater. Sol. Cells*, vol. 74, no. 1–4, pp. 213–218, Oct. 2002.

[26] P. Rosenits, F. Kopp, and S. Reber, "Epitaxially grown crystalline silicon thin-film solar cells reaching 16.5% efficiency with basic cell process," *Thin Solid Films*, vol. 519, no. 10, pp. 3288–3290, Mar. 2011.

[27] K. Van Nieuwenhuysen, M. R. Payo, I. Kuzma-Filipek, J. Van Hoeymissen, G. Beaucarne, and J. Poortmans, "Epitaxially grown emitters for thin film silicon solar cells result in 16% efficiency," *Thin Solid Films*, vol. 518, no. 6, pp. S80–S82, Jan. 2010.

[28] K. Alberi, I. T. Martin, M. Shub, C. W. Teplin, M. J. Romero, R. C. Reedy, E. Iwaniczko, A. Duda, P. Stradins, H. M. Branz, and D. L. Young, "Material quality requirements for efficient epitaxial film silicon solar cells," *Appl. Phys. Lett.*, vol. 96, no. 7, p. 073502, 2010.

[29] V. Shah, J. Booream-Phelps, and S. Min, "2014 Outlook: Let the Second Gold Rush Begin," 2014.

[30] T. van Amstel and I. J. Bennett, "Towards a better understanding of the thermo-mechanical behavior of h-pattern cells during metallization," in *34th Photovoltaic Specialist Conference*, 2008, pp. 1–5.

[31] S. Hegedus and A. Luque, "Achievements and Challenges of Solar Electricity from Photovoltaics," in *Handbook of Photovoltaic Science and Engineering*, 2nd ed., A. Luque and S. Hegedus, Eds. Chichester, West Sussex, U.K: Wiley, 2011, pp. 1–38.

[32] Z. Xi, D. Yang, W. Dan, C. Jun, X. Li, and D. Que, "Investigation of texturization for monocrystalline silicon solar cells with different kinds of alkaline," *Renew. Energy*, vol. 29, no. 13, pp. 2101–2107, Oct. 2004.

[33] E. Vazsonyi, K. De Clercq, R. Einhaus, E. Van Kerschaver, K. Said, J. Poortmans, J. Szlufcik, and J. Nijs, "Improved anisotropic etching process for industrial

texturing of silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 57, no. 2, pp. 179–188, Feb. 1999.

[34] J.-H. Zhao, T. Ryan, P. S. Ho, A. J. McKerrow, and W.-Y. Shih, "On-wafer characterization of thermomechanical properties of dielectric thin films by a bending beam technique," *J. Appl. Phys.*, vol. 88, no. 5, p. 3029, 2000.

[35] K. H. Lu, S.-K. Ryu, Q. Zhao, K. Hummler, J. Im, R. Huang, and P. S. Ho, "Temperature-dependent thermal stress determination for through-silicon-vias (TSVs) by combining bending beam technique with finite element analysis," in *61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 1475–1480.

[36] D. Jawarani, D. Xu, S. Smith, R. A. Rao, L. Mathew, S. Saha, S. Banerjee, and P. S. Ho, "Integration and Reliability of Ultra Thin Silicon Solar Cells and Modules Fabricated using SOM Technology," in *38th Photovoltaic Specialist Conference*, 2012, pp. 1–4.

[37] D. Xu, P. S. Ho, R. a. Rao, L. Mathew, S. Smith, S. Saha, D. Sarkar, C. Vass, and D. Jawarani, "Mechanical strength and reliability of a novel thin monocrystalline silicon solar cell," in *IEEE International Reliability Physics Symposium (IRPS)*, 2012, pp. 4A.3.1–4A.3.7.

[38] W. G. J. H. M. van Sark, L. Korte, and F. Roca, "Introduction – Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells," in *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, 1st ed., W. G. J. H. M. van Sark, L. Korte, and F. Roca, Eds. Berlin: Springer, 2012, p. 3.

[39] J.-P. Kleider, "Band Lineup Theories and the Determination of Band Offsets from Electrical Measurements," in *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, 1st ed., W. G. J. H. M. van Sark, L. Korte, and F. Roca, Eds. Berlin, Germany: Springer, 2012, p. 407.

[40] R. a. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Appl. Phys. Lett.*, vol. 69, no. 17, p. 2510, 1996.

[41] B. Chhabra, S. Bowden, R. L. Opila, and C. B. Honsberg, "High effective minority carrier lifetime on silicon substrates using quinhydrone-methanol passivation," *Appl. Phys. Lett.*, vol. 96, no. 6, p. 063502, 2010.

[42] R. A. S. Andreas Cuevas, “Prediction of the Open-circuit Voltage of Solar Cells from the,” *Prog. Photovoltaics Res. Appl.*, vol. 5, no. November 1996, pp. 79–90, 1997.

[43] T. Sawada, N. Terada, S. Tsuge, T. Baba, T. Takahama, K. Wakisaka, S. Tsuda, S. Nakano, and N. Materials, “High-efficiency a-Si/c-Si Heterojunction Solar Cell,” in *24th IEEE Photovoltaic Specialists Conference*, 1994, pp. 1219–1226.

[44] E. Maruyama, A. Terakawa, M. Taguchi, and Y. Yoshimine, “Sanyo ’ s Challenges to the Development of High-efficiency HIT Solar Cells and the Expansion of HIT Business,” in *4th World Conference on Photovoltaic Energy Conversion*, 2006, pp. 1455–1460.

[45] F. N. Sinnadurai, B. Post, and M. Heath, “The accelerated ageing of plastic encapsulated semiconductor devices in environments containing a high vapour pressure of water,” *Microelectron. Reliab.*, vol. 13, pp. 23–27, 1974.

[46] W. Kern, “The Evolution of Silicon Wafer Cleaning Technology,” *J. Electrochem. Soc.*, vol. 137, no. 6, pp. 1887–1892, 1990.

[47] S. Saha, M. M. Hilali, E. U. Onyegam, D. Sarkar, D. Jawarani, R. A. Rao, L. Mathew, R. S. Smith, D. Xu, U. K. Das, B. Sopori, and S. K. Banerjee, “Single heterojunction solar cells on exfoliated flexible ~25 μm thick mono-crystalline silicon substrates,” *Appl. Phys. Lett.*, vol. 102, no. 16, p. 163904, 2013.

[48] S. Naghshineh, E. Oldak, and G. Schwartzkopf, “Conditioning compositions for solar cells,” US20120187336 A12012.

[49] H. F. Schmidt, M. Meuris, P. W. Mertens, A. L. P. Rotondaro, M. M. Heyns, T. Q. Hurd, and Z. Hatcher, “H2O2 Decomposition and Its Impact on Silicon Surface Roughening and Gate Oxide Integrity,” *Jpn. J. Appl. Phys.*, vol. 34, pp. 727–731, 1995.

[50] S. Verhaverbeke, M. Meuris, P. W. Mertens, M. M. Heyns, A. Philipossian, D. Graf, and A. Schnegg, “The effect of metallic impurities on the dielectric breakdown of oxides and some new ways of avoiding them,” in *Electron Devices Meeting*, 1991, pp. 71–74.

[51] H. Angermann and J. Rappich, “Wet-Chemical Conditioning of Silicon Substrates for a-Si:H/c-Si Heterojunctions,” in *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, 1st ed., W. G. J. H. M. van Sark, L. Korte, and F. Roca, Eds. Berlin: Springer, 2012, pp. 45–94.

[52] M. Edwards, S. Bowden, U. Das, and M. Burrows, “Effect of texturing and surface preparation on lifetime and cell performance in heterojunction silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 11, pp. 1373–1377, Nov. 2008.

[53] L. Fesquet, S. Olibet, J. Damon-Lacoste, S. De Wolf, A. Hessler-Wyser, C. Monachorr, and C. Ballif, “Modification of textured silicon wafer surface morphology for fabrication of heterojunction solar cell with open circuit voltage over 700 mV,” in *34th IEEE Photovoltaic Specialists Conference (PVSC)*, 2009, no. 100, pp. 000754–000758.

[54] K. A. Reinhardt and W. Kern, Eds., *Handbook of Silicon Wafer Cleaning Technology*, 2nd ed. Norwich: William Andrew Inc., 2008, pp. 25, 28–29.

[55] B. Kanegsberg and E. Kanegsberg, Eds., *Handbook for Critical Cleaning: Cleaning Agent and Systems*, 2nd ed. Boca Raton: CRC Press, 2011, pp. 73–74.

[56] C. Beaudry, H. Morinaga, and S. Verhaverbeke, “A study of metallic contamination removal and addition using modified SC-1 solutions,” in *Ceaning Technology in Semiconductor Device Manufacturing VII*, 2002, pp. 118 – 125.

[57] G. W. Gale, D. L. Rath, E. I. Cooper, S. Estes, H. F. Okorn-Schmidt, J. Brigante, R. Jagannathan, G. Settembre, and E. Adams, “Enhancement of Semiconductor Wafer Cleaning by Chelating Agent Addition,” *J. Electrochem. Soc.*, vol. 148, no. 9, p. G513, 2001.

[58] E. Desimoni, G. I. Casella, A. M. Salvi, T. R. I. Cataldi, and A. Morone, “XPS investigation of ultra-high-vacuum storage effects on carbon fibre surfaces,” *Carbon N. Y.*, vol. 30, no. 4, pp. 527–531, Jan. 1992.

[59] M. Prutton and M. M. El Gomati, Eds., *Scanning Auger Electron Microscopy*, 1st ed. Chichester, UK: John Wiley & Sons, Ltd, 2006, pp. 3–12.

[60] L. E. Davis, N. C. MacDonald, P. W. Palmberg, and G. E. Riach, *Handbook of Auger electron spectroscopy : a reference book of standard data for identification and interpretation of Auger electron spectroscopy data*, 2nd ed. Eden Prairie: Physical Electronics Industries, 1976, p. 5.

[61] M. Taguchi, A. Terakawa, E. Maruyama, and M. Tanaka, “Obtaining a higherVoc in HIT cells,” *Prog. Photovoltaics Res. Appl.*, vol. 13, no. 6, pp. 481–488, Sep. 2005.

[62] M.Tanaka, M.Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, and Y. Kuwano, “Development of new a-Si/c-Si heterojunction solar

cells: ACJHIT (artificially constructed junction-heterojunction with Intrinsic thin-layer)," *Jpn. J. Appl. Phys.*, vol. 31, no. 11, p. 3518, 1992.

[63] U. Das, S. Hegedus, L. Zhang, J. Appel, J. Rand, and R. Birkmire, "Investigation of hetero-interface and junction properties in silicon heterojunction solar cells," in *35th Photovoltaic Specialists Conference*, 2010, pp. 001358–001362.

[64] H. Fujiwara and M. Kondo, "Impact of epitaxial growth at the heterointerface of a-Si:H/c-Si solar cells," *Appl. Phys. Lett.*, vol. 90, no. 1, p. 013503, 2007.

[65] M. G. Kang, S. Tark, J. C. Lee, C.-S. Son, and D. Kim, "Changes in efficiency of a solar cell according to various surface-etching shapes of silicon substrate," *J. Cryst. Growth*, vol. 326, no. 1, pp. 14–18, Jul. 2011.

[66] L. J. Caballero, "Contact Definition in Industrial Silicon Solar Cells," in *Solar Energy*, no. February, R. D. Rugescu, Ed. Rijeka, Croatia: InTech Europe, 2010, p. 376.

[67] J. Bartsch, A. Mondon, C. Schetter, M. Horteis, and S. W. Glunz, "Copper as conducting layer in advanced front side metallization processes for crystalline silicon solar cells, exceeding 20% on printed seed layers," in *35th Photovoltaic Specialists Conference*, 2010, pp. 001299–001303.

[68] C. E. Dube and R. C. Gonsiorawski, "Improved contact metallization for high efficiency EFG polycrystalline silicon solar cells," in *21st Photovoltaic Specialist Conference*, 1990, vol. 01821, pp. 624–628.

[69] A. Knorz, M. Aleman, A. Grohe, R. Preu, and S. W. Glunz, "Laser ablation of antireflection coatings for plated contacts yielding solar cell efficiencies above 20%," in *24th European Photovoltaic Solar Energy Conference*, 2009, pp. 1002–1005.

[70] A. Nguyen, M. V. Rane-Fondacaro, H. Efstathiadis, and P. Haldar, "Formation of low ohmic contact nickel silicide layer on textured silicon wafers using electroless nickel plating," in *25th European Photovoltaic Solar Energy Conference*, 2010, pp. 2672–2675.

[71] D. Kray, M. Alemán, A. Fell, S. Hopman, K. Mayer, M. Mesec, R. Müller, G. P. Willeke, S. W. Glunz, B. Bitnar, D. Neuhaus, R. Lüdemann, T. Schlenker, and D. Manz, "Laser-doped Silicon Solar Cells by Laser Chemical Processing (LCP) exceeding 20 % Efficiency," in *34th Photovoltaic Specialist Conference*, 2008, pp. 20–22.

[72] M. Aleman, N. Bay, M. Fabritius, and S. W. Glunz, “Characterization of electroless nickel plating on silicon solar cells for the front side metallization,” in *22nd European Photovoltaic Solar Energy Conference*, 2007, pp. 1590–1592.

[73] A. Knorz, M. Peters, A. Grohe, C. Harmel, and R. Preu, “Selective Laser Ablation of SiN x Layers on Textured Surfaces for Low Temperature Front Side Metallizations,” *Prog. Photovoltaics Res. Appl.*, vol. 17, no. October 2008, pp. 127–136, 2009.

[74] A. Mondon, J. Bartsch, B. J. Godejohann, M. Horteis, and S. W. Glunz, “Advanced front side metallization for crystalline silicon solar cells based on a nickel-silicon contact,” in *2nd workshop on Metallisation for crystalline silicon solar cells*, 2010, pp. 1–23.

[75] A. A. Brand, F. Meyer, J. F. Nekarda, and R. Preu, “Reduction of picosecond laser ablation threshold and damage via nanosecond pre-pulse for removal of dielectric layers on silicon solar cells,” *Appl. Phys. A*, no. July, 2014, pp. 1–5, 2014.

[76] J. L. Hernández, M. Alemán, C. Allebé, T. Bearda, J. John, I. Kuzma, H. Philipsen, N. Posthuma, S. Rodet, and J. Poortmans, “The Way Towards Front Side Metallization By Copper-plating : What We Can Learn From Microelectronics,” in *2nd Workshop on Metallization for Crystalline Silicon Solar Cells*, 2010, p. 5.

[77] A. Hübner, A. G. Aberle, and R. Hezel, “Novel cost-effective bifacial silicon solar cells with 19.4% front and 18.1% rear efficiency,” *Appl. Phys. Lett.*, vol. 70, no. 8, p. 1008, 1997.

[78] R. Hezel, “Novel applications of bifacial solar cells,” *Prog. Photovoltaics Res. Appl.*, vol. 11, no. 8, pp. 549–556, Dec. 2003.

[79] E. U. Onyegam, D. Sarkar, M. M. Hilali, S. Saha, L. Mathew, R. a. Rao, R. S. Smith, D. Xu, D. Jawarani, R. Garcia, M. Ainom, and S. K. Banerjee, “Realization of dual-heterojunction solar cells on ultra-thin ∼25 μm, flexible silicon substrates,” *Appl. Phys. Lett.*, vol. 104, no. 15, p. 153902, Apr. 2014.

[80] M. Lu, S. Bowden, U. Das, and R. Birkmire, “Interdigitated back contact silicon heterojunction solar cell and the effect of front surface passivation,” *Appl. Phys. Lett.*, vol. 91, no. 6, p. 063507, 2007.

[81] T. Saga, “Advances in crystalline silicon solar cell technology for industrial mass production,” *NPG Asia Mater.*, vol. 2, no. 3, pp. 96–102, Jul. 2010.

Vita

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