ENABLING LOW COST TEST AND TUNING OF DIFFICULT-TO-MEASURE DEVICE SPECIFICATIONS: APPLICATION TO DC-DC CONVERTERS AND HIGH SPEED DEVICES

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ENABLING LOW COST TEST AND TUNING OF DIFFICULT-TO-MEASURE DEVICE SPECIFICATIONS: APPLICATION TO DC-DC CONVERTERS AND HIGH SPEED DEVICES

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To my loving family and friends...

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
BER	Bit Error Rate
CUT	Circuit Under Test
DAC	Digital to Analog Converter
DUT	Device Under Test
FFT	Fast Fourier Transform
GA	Genetic Algorithm
IFFT	Inverse Fast Fourier Transform
OFDM	Orthogonal Frequency Division Multiplexing
RF	Radio Frequency
RMS	Root Mean Square
SoC	System On a Chip
UWB	Ultra Wide Band
VCO	Voltage Controlled Oscillator
LPF	Low-pass Filter
BPF	Band-pass Filter

SUMMARY

Along with low-cost compact integrated circuit trends, the scale of analog and mixed-signal devices has been reduced to the nanometer level. As technology feature sizes shrink further in the nanometer regime, circuit specifications and performances are becoming increasingly vulnerable to manufacturing process variations, leading to unstable yield during mass production. To maintain high production yield, post-manufacture testing and tuning of manufactured devices is essential and imperative. However, with the increased levels of integration, power consumption, and circuit operating frequency, many important circuit specifications are difficult to measure during post-manufacture test and require either expensive automatic test equipment (ATE) or specially designed test hardware resulting in increased test cost. To reduce the overall manufacturing cost [1] and improve production yield, low-cost test and tuning methods for difficult-to-measure specifications are urgently needed. This need is addressed in this research from the following perspectives:

"Safe" test and self-tuning for power converters: In conventional specification-based testing, sequential testing of each specification is performed and pass/fail decisions are made on the basis of datasheet specifications. Such specification based testing of devices in production requires the use of relays on the tester load board for reconfiguration of test circuitry between tests for different device specifications. In general, the test time for each specification is dominated by the time taken to reconfigure the tester load board relays. One possible way to alleviate the extra test time incurred by relay reconfiguration is to use alternative signature-based test methods [2-5] where a single measurement is used to predict multiple DUT specifications. However, this

method cannot be applied directly to power converter testing since IC socket parasitics [6], causes large voltage spikes during high current testing resulting in circuit damage. In this thesis, a "safe" alternate test structure is developed where the power converter (boost/buck converter) is placed in a different mode of operation during alternative test (light switching load) as opposed to standard test (heavy switching load) to prevent damage to the DUT during manufacturing test. Based on the alternative test structure, self-tuning methods for both boost and buck converters are also developed in this thesis. In addition, to make these test structures suitable for on-chip built-in self-test (BIST) application, a special sensing circuit has been designed and implemented. Stability analysis filters and appropriate models are also implemented to predict the DUT's electrical stability condition during test and to further predict the values of tuning knobs needed for the tuning process.

High bandwidth RF signal generation: Prior research has focused on creating high frequency RF signals using up-conversion mixers [7-10]. However, mixer nonlinearity results in signal distortion that is difficult to eliminate with such methods. To resolve this problem, a framework for low-cost high-fidelity wideband RF signal generation is developed in this thesis. Depending on the band-limited target waveform, the input data for two interleaved DACs (digital-to-analog converters) system is optimized by a matrix-model-based algorithm in such a way that it minimizes the distortion between one of its image replicas in the frequency domain and the target RF waveform within a specified signal bandwidth. The approach is used to demonstrate how interferers with specified frequency characteristics can be synthesized at low cost for interference testing of RF communications systems. The frameworks presented in this thesis have a significant

impact in enabling low-cost test and tuning of difficult-to-measure device specifications for power converter and high-speed devices. The thesis outline is presented in Figure 1 below:

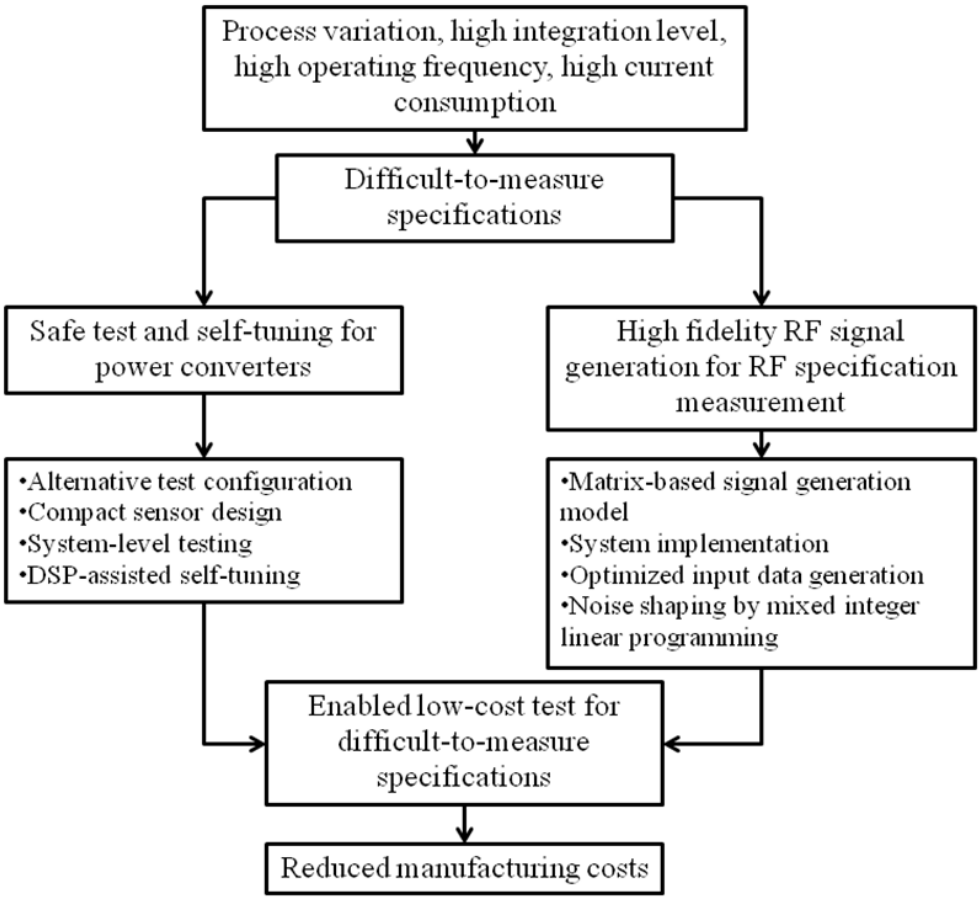


Figure 1: Dissertation outline and scope.

CHAPTER 1: INTRODUCTION

With the rapid advancement of integrated circuit (IC) technology, electronic devices have evolved dramatically during the past few decades in terms of processing speed, power consumption, and size. This evolution has mainly been catalyzed by the increase in transistor density, which in turn has been driven by increased technology scaling down to 14nm transistor feature sizes. Indeed, through the past 30 years, the semiconductor manufacturing resolution has increased from 10 um to 14 nm in accordance with Moore's law [11, 12], which indicates that the size of transistors has been scaled down by a factor of hundreds. Such incredibly small transistor size leads to a large integration scale with billions of transistors on a single die. At the same time, thanks to the reduction in transistor size, circuit operation speed—which is inversely proportional to the size of a transistor has increased from 108 KHz (Intel 4004) to several GHz.

The manufacture and test of highly integrated ICs with high operation speeds are not without technical challenges. As manufacturing resolution continues to scale down, fabricated ICs become more vulnerable to process variations. In addition, the number of input/output pins available on a small-sized IC is limited. This, together with high circuit operation speed, makes testing such ICs more difficult. As shown in Figure 2, a typical IC development flow consists of three stages: the design stage, the characterization stage, and a high-volume production stage. The design stage starts with design definition and implementation where the product specifications and design methodology are defined. Once the schematic design meets all the desired specifications in simulation, in the characterization stage, an actual prototype is built and tested on the bench to ensure that all measured specifications meet the product specifications as

defined in the design stage. Should there be any discrepancy between simulated results and bench measurements, the design process is iterated to ensure that all specifications of the final design are met.

Manufacture takes place after the prototype in the characterization stage meets all performance expectations as defined in the design stage. Manufactured chips need to be tested to ensure that their specifications in operation are within acceptable limits. Wafer-sort test and final test are conducted using automatic test equipment (ATE) before and after packaging, respectively. The total manufacturing cost for each IC consists of production cost from manufacturing/packaging and test cost from wafer-sort test/final test.

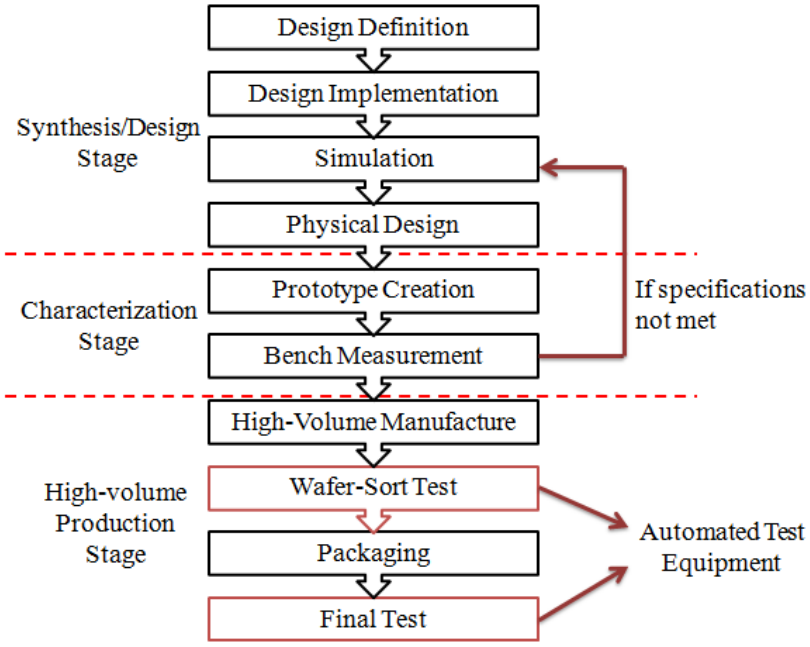


Figure 2: Standard IC development flow.

Even though high levels of system integration has brought down the production cost of a single transistor, as shown in Figure 3, the test cost per transistor is rising over the last two decades. In fact, as discussed above, the increase in operation speed and the

decrease in chip size bring more challenges to IC test in the production stage. Rising peak power consumption of power ICs further pushes up the test cost . Unsurprisingly, the test cost of integrated circuits, especially mixed-signal and RF Systems on Chips (SoCs) , is the fastest growing portion of total manufacturing cost (production cost + test cost) [1] and can amount to as much as 45% of the total manufacturing cost [14].

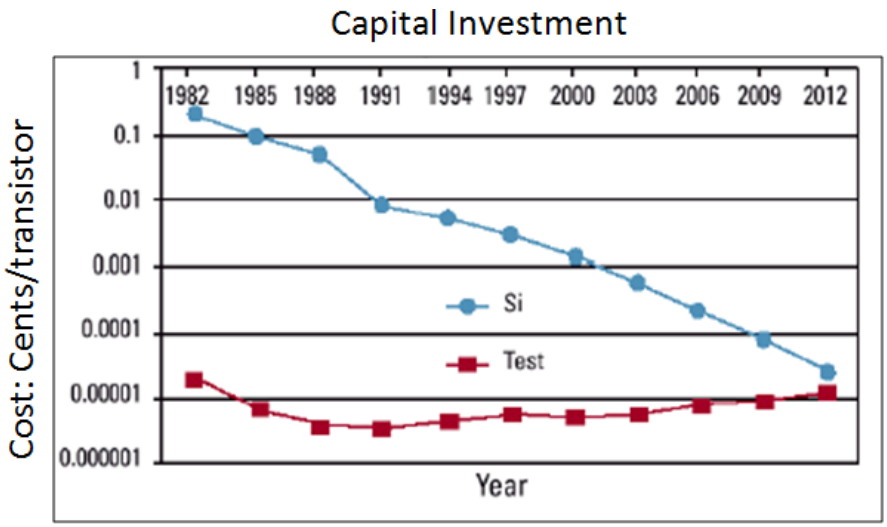


Figure 3: Rising test cost.

To reduce the test cost and thereby the total manufacturing cost, a number of techniques (defect-oriented testing[15], quiescent current testing[16], structural testing[17]) that involve concepts such as test ordering, compaction, test generation, and designs for test have been explored in the past. However, with increased circuit complexity, many specifications are difficult to measure and require complex test instrumentation that increases test cost drastically. The section below provides a brief overview of typical causes of specification measuring difficulties, summarizes and reviews some existing low-cost methods for alleviating the cost of such specification measurement.

1.1 Increased Overall Test Time

Due to the competitive nature of the semiconductor industry, more functions, such as power conversion/management, signal upconversion/downconversion, and micro-controllers, have been integrated into a die geometry to improve cost efficiency, performance, and functionality. To guarantee that all fabricated chips meet their manufacturing specifications, a sophisticated test process has to be conducted during post-manufacturing test where each of device under test (DUT)'s specification is measured and compared to the target value sequentially. Since some specifications require distinctive test setups, ATE load board has equipped with relays to properly re-configure test circuitries. However, the slow switching time of relay has dramatically increased the overall test time of each DUT. Even built-in self-test (BIST) structures have been introduced to replace ATE test partially, some specifications that requires special test conditions are still measured on ATE load board and cost significantly amount of test time. To reduce the test time and therefore increase test efficiency, test data compression techniques have been proposed where multiple DUT specifications are measured through a single DUT response and the test time cost for switching relays are avoided. This single DUT response is referred to as the "signature" of the DUT and the test method is called "signature test".

The RF/mixed-signal signature test basically performs an analog data compression which has evolved gradually from digital test compressing approaches such as transition counting[20], checksums[21-23], and syndrome testing[24] for digital circuit testing. It uses DUT's transient response under a stimulation to predict specifications and detect catastrophic failures through a pre-built statistical model. Since signature test depends on transient responses, it does not require DUT to settle down after stimulation. Therefore, apart from the load board reconfiguring time it saves, the signature test also saves circuit settling time when compared with conventional tests such as DC (static state)[25, 26] and

AC (steady state) [27] tests. The reduction of this part of test time is more pronounced when the time constant of DUT is large.

The basic flow of the signature test is presented in Figure 4(b). The conventional test as shown in Figure 4(a), requires individual test setups, involving an overhead for setting up the test equipment and test circuit configuration for the measurement of each specification. In contrast, for the signature test, multiple specifications of the DUT are computed using a single response. In addition, the signature test does not require as complex testing instrument as does the conventional test. For these reasons, the signature test has been defined as a low-cost alternative to specification testing [2].

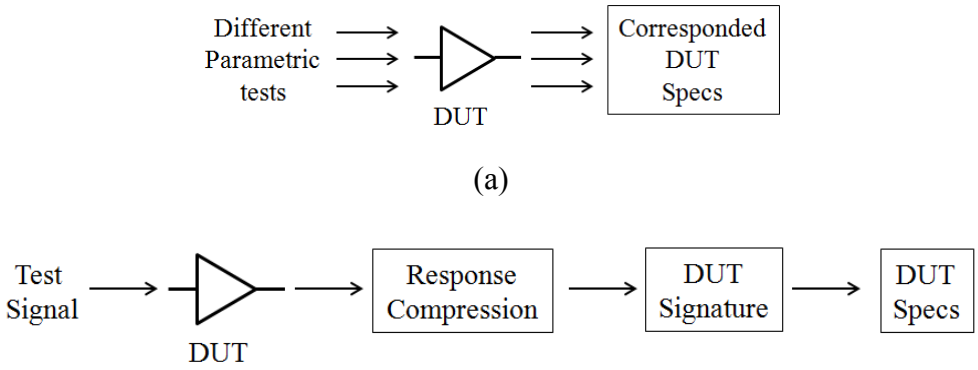


Figure 4: Basic test configuration for the (a) conventional test and (b) signature test.

Signature test is based on the assumption that any process parameter variations in the parameter space $\boldsymbol{P}$ affect both the specification space $\boldsymbol{S}$ and the response measurement space $\boldsymbol{M}$ of the circuit. Therefore, $\boldsymbol{P}$ can be mapped to $\boldsymbol{S}$ and $\boldsymbol{M}$ separately through nonlinear mappings: f_{ps}: $\boldsymbol{P}\rightarrow\boldsymbol{S}$ and f_{pm}: $\boldsymbol{P}\rightarrow\boldsymbol{M}$[2-5]. Based on the indirect relation between space $\boldsymbol{S}$ and space $\boldsymbol{M}$, a study shows that a nonlinear statistical multivariate regression analysis is able to extract a mapping function f_{ms}: $\boldsymbol{M}\rightarrow\boldsymbol{S}$ that generates predictions of specifications of DUT based on a given set of measurements[3].

The general flow for the signature test is shown in Figure 5. Note that the DUT in signature test may be connected in a different configuration to enhance the sensitivity of critical components. The test begins with injecting a pre-optimized test stimulus into the properly configured DUT. Then the key information carried by DUT's output waveform is extracted by some built-in circuitry, digitized by an analog-to-digital converter (ADC), and analyzed by a digital signal processing (DSP) unit. The specifications of the DUT are then predicted by the DSP unit based on the captured results.

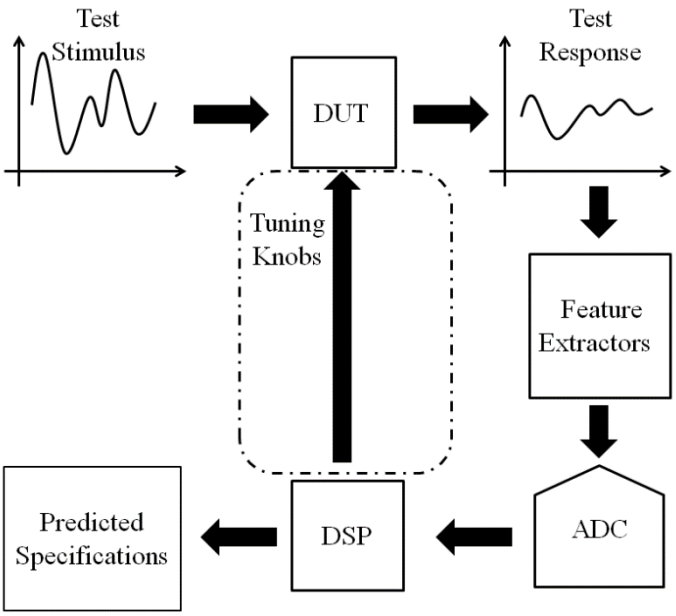


Figure 5: Overview of the alternative test procedure.

In a tunable circuit, the path in the rectangular dash is built for tuning purposes[33], where all tuning settings are also predicted by a DSP unit. The built-in circuitry that extracts key information from the test response is called a sensor. The purpose of such sensing circuitry is to convert important high-frequency information to a lower-frequency range (within the Nyquist region of ADC). By applying sensors in this conversion, the problems of high-frequency external test access and signal integrity issues are avoided. In addition, since the sensor performs analog processing on high-frequency signals, the

same test approach is applicable to both high- and low-operating frequencies[34]. Because of the same process variation in built-in sensors, a sensor calibration test is generally recommended prior to the signature test.

In this thesis, signature test based alternate test structures have been introduce to measure difficult-to-measure specifications while achieving significant time reductions in overall test time.

1.2 Test Risk: Power Converter Test

The design of power converters with small form factor, fast response, and high power efficiency[35] is gaining increasing attention because of the proliferation of integrated electronic systems with diverse power supply requirements. A large number of portable devices use DC-DC buck converters [36] to step down the DC voltage from a battery and use boost converters [37] to step up a DC voltage (from the fuel cell battery of electrical cars or alternative power supplies) with high efficiencies. It is necessary to stabilize the power supply to such devices in the face of battery output voltage variations as well as changes in supply load conditions [38]. Such stabilizations are referred to as line and load regulation capability of the power converter employed, and they are enhanced by the use of specific design techniques within the power converter circuitry. However, traditional measurement of the line and load regulation capability of a DC-DC converter requires excitation of the power supply line of the converter as well as switching of the load seen by the converter [39] in a closed-loop test configuration with a sufficient load current to keep it operating with acceptable switching frequency[40]. Therefore, during the manufacturing test, it is difficult to measure load regulation because of the fact that switching leads to sharp voltage transients at the input node of the buck converter and the

output node of the boost converter. These voltage transients are caused by parasitic inductances associated with the test socket leads and can damage the drive transistors of the power converter. Depending on the type of power converter, the locations of these voltage transients vary. A detailed explanation of the causes and locations of these voltage transients on buck-boost converter is discussed in Chapter 2.2 Test Risk Analysis for Power Converters. As a consequence, even though customers require close guarantees of line and load regulation capability from power converter manufacturers, these specifications are not evaluated during the manufacturing test of majority of DC-DC converters manufactured. Rather, these are guaranteed by design or measured across only a few manufactured parts that are not shipped to the customer.

Alternative approaches for testing the specifications of DC-DC power converters that eliminate the possibility of damage to the DUT (which happens when conventional line and load regulation tests are performed) are presented for buck and boost converter, respectively, in this work. For all test approaches, specially designed output filters are used as sensors to filter out important information, and analog-to-digital converters (ADCs) are used to capture the responses of the DUTs under a carefully optimized test stimulus/perturbation in light-load switching conditions. The resulting data is then used to predict line/load regulation and other specification values under heavy-load switching conditions as required by standard test procedures.

1.3 High-Fidelity Wideband Signal Generation

The cost and complexity of testing equipment continue to increase as more complex high-speed and high-precision consumer products are manufactured for the marketplace. For advanced high-speed communication, timing, interference, and signal noise are

critical parameters that limit system-level performance. Because of its efficient usage of available frequency band and robustness against multipath fading, orthogonal frequency division multiplexing (OFDM) is gaining increasing attention in the field of LAN/MAN communication systems[41, 42]. After 7,500 MHz of bandwidth (3.1 GHz to 10.6 GHz) has been opened up for Ultra-wideband (UWB) devices by the Federal Communications Commission (FCC), many research has been focusing on the UWB OFDM with the expectation that UWB devices would provide low-cost solutions to the increasing demand for high data rates[43]. With the wide bandwidth, the channel conditions can no longer be assumed as an evenly distributed white noise across all subcarriers during these tests [44]. To test the performance of adaptive RF systems that continuously adapt to the channel conditions[45-51], it is extremely important to create channel conditions that mimic the real application environment to achieve a more realistic testing condition for adaptive RF systems. With such demands, a high-fidelity RF generating method is critical.

To accurately measure system-level jitter tolerance, a high-speed wideband signal generation with precise jitter injection capability is necessary[52]. In prior research, diverse mechanisms for jitter injection have been studied. These include modulating either the output buffer voltage or reference clock[53, 54] using an arbitrary waveform generator (AWG) with pre-stored jitter and a timing set from ATEs[55]. However, these methods have several limitations. These jitter modulation techniques are effective for periodic and random jitter injection, but synchronization between the injected jitter and the applied test signal is difficult because jitter generation is generally decoupled from test pattern application. In addition, conventional AWG-based jitter injection is able to

generate different kinds of jitter characteristics, but its speed is limited by the sampling rate of the digital circuit and is not scalable to very high-speed wideband signals. The timing set function of ATE facilitates on-the-fly jitter characteristic modulation but lacks flexibility since timing set resources within the ATE are limited[56].

Since AWG-based jitter injection is more flexible across different injected jitter types, significant research has been performed in the past on increasing the effective Nyquist rate of the generated test signal without using very high speed digital-to-analog converters (DACs). Theoretically, N-parallel DACs can increase the effective Nyquist rate up to N times the sampling frequency of each individual DAC[57]. But since precise interleaving increases built cost and complexity, a large scale of interleaved DACs is impractical. As a consequence, a low-cost wideband high-fidelity RF signal generation method is urgently needed for testing RF devices.

In this work, a higher-than-Nyquist-rate RF signal synthesis method is introduced to provide a low-cost high-fidelity RF signal generation method for high-speed testing. It calculates the optimized input for a DAC system to minimize the differences between the first image of its output and the target signal within a predefined bandwidth. This first image is then passed through a band-pass filter and used as the primary output of the system. This signal generation method finds its applications in wideband high-speed jitter/signal generation and has been used to generate high-fidelity wideband channel interference for low-cost adaptive system testing.

CHAPTER 2: POWER CONVERTER BACKGROUND

2.1 Power Converter Overview

Switched-mode power converters have drawn wide attention in applications where high efficiency is one of the primary concerns because of their high power efficiency in DC voltage conversion compared with linear regulators. In this thesis, we will focus on the study of voltage-controlled step-down switched-mode power converters that are also called buck converters and voltage-controlled step-up switched-mode power converters that are also called boost converters.

2.1.1 Buck Converter

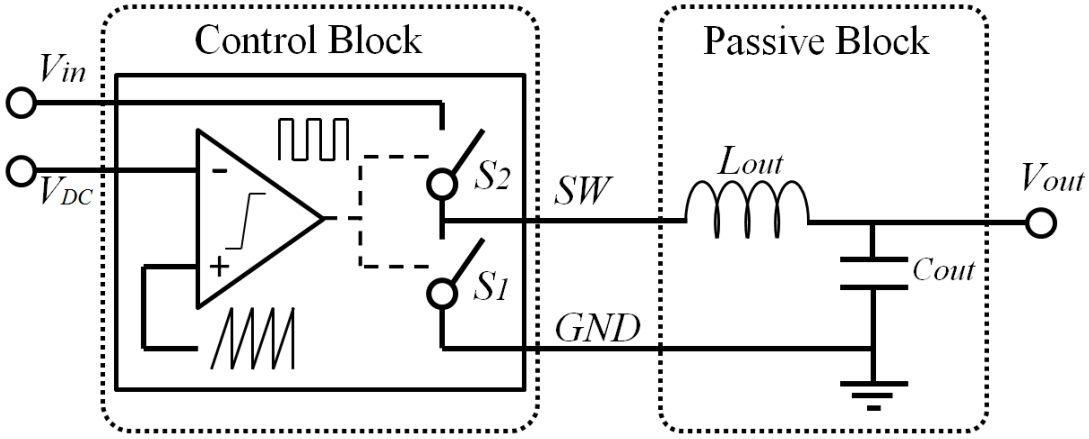


Figure 6: Block diagram of buck converter without feedback control.

There are two main modules in an open-loop buck converter as shown in Figure 6: control block and passive block. The control block generates a pulse train whose width is directly proportional to the output voltage generated by the converter. When the output voltage falls below the stipulated output voltage value, the pulse width is increased and vice versa (negative feedback, shown in Figure 7). The pulse train is generated by comparing a periodic ramp signal with a reference voltage (V_{DC}) derived by scaling and filtering the output voltage of the converter. When the reference voltage is low, the

comparator in Figure 6 produces a pulse train with higher width and vice versa. The circuitry that produces the modulated pulse widths in response to the value of the output voltage of the converter is called the pulse-width modulator (PWM) of the converter. The output of the PWM controls the ON and OFF states of the power MOSFET switches shown in Figure 6. When S_2 is turned on by a "low" value of the pulse train, the current through the inductor increases linearly, charging the capacitor. Subsequently, when the output of the comparator becomes "high," S_2 is turned off, and S_1 is turned on. The current through the inductor continues to flow in the same direction as before, releasing the energy stored in the inductor as the current decreases linearly with time, and the process is repeated.

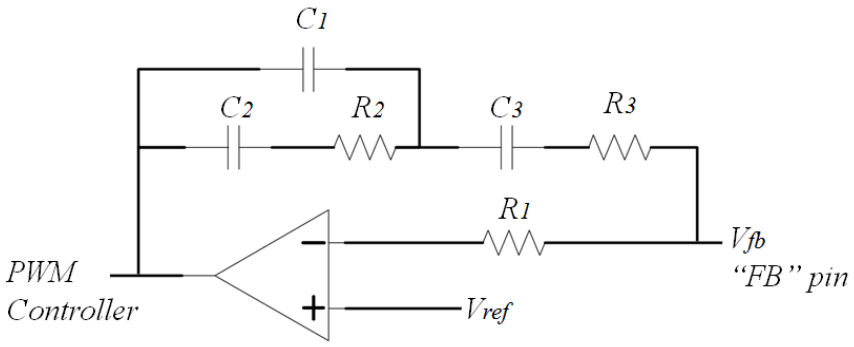


Figure 7: An error amplifier configuration with type III compensation network.

There are two operation modes of a buck converter. It operates in continuous mode if the inductor's current never falls to zero during operation; otherwise, it operates in discontinuous mode. For this thesis, only the general continuous mode is considered since it is the most commonly used mode for switch regulators. Equation 1 shows the transfer function of the open-loop buck converter system in Figure 6:

$$H_{open} = \frac{(R_{ESR}Cs+1)}{V_{osc}(LCs^2+(R_{ESR}+R_{DCR})Cs+1)} \qquad \text{Equation 1}$$

Since all physical components are constructed with materials of finite electrical resistance, R_{ESR} and RDCR in Equation 1 denote the equivalent series resistances of the capacitor C and inductor L, respectively[58].

To make the converter capable of adjusting to the perturbations of the external load and the line input voltage, a closed-loop control unit with a compensation network is needed. From Equation 1, we can observe that for a very low RESR and RDCR, the phase slope will be very sharp at the corresponding double pole, and the gain will have a high peak. Therefore, the phase needs to be boosted to allow enough phase margin for stability[58] . A type III compensator is usually used and is shown in Figure 7. Its transfer function is given in Equation 2.

$$H_{comp} = -\frac{(C_2R_2s+1)(sC_3(R_1+R_3)+1)}{R_1s(C_1+C_2)(\frac{C_1C_2R_2}{C_1+C_2}s+1)(C_3R_3s+1)} \qquad \text{Equation 2}$$

As Equation 2 shows, the two zeros from the type III network give a phase boost of 180^o that is needed to counteract the effects of the double pole caused by the output filter as discussed above. With this kind of compensation, the loop transfer function of buck converter with feedback control is given by

$$H_{loop} = H_{comp}H_{open} \qquad \text{Equation 3}$$

Because of the stability compensation requirement[58], the converter often has its first zero at f_{Z1} and has its second zero and first two poles near f_{ZP} to reach unconditional stability. The values of these frequencies are shown in Equation 4.

$$f_{Z1} = \frac{1}{2\pi R_2 C_2},\ f_{ZP} = \frac{1}{2\pi\sqrt{LC}} \qquad \text{Equation 4}$$

The closed-loop connection of buck converters is presented in Figure 8. In a steady state, the error amplifier in the compensation network compares the output voltage of the converter with the internal reference voltage V_{ref} and generates a DC voltage accordingly. By modulating this voltage using the PWM, the ON and OFF states of the power MOSFETs are controlled.

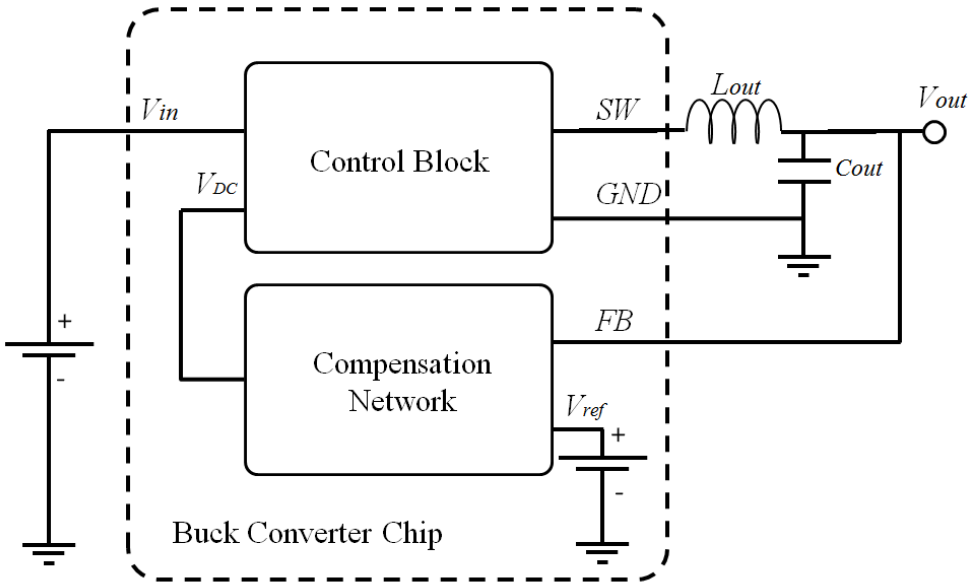


Figure 8: Block diagram of buck converter with closed-loop feedback control.

2.1.2 Boost Converter

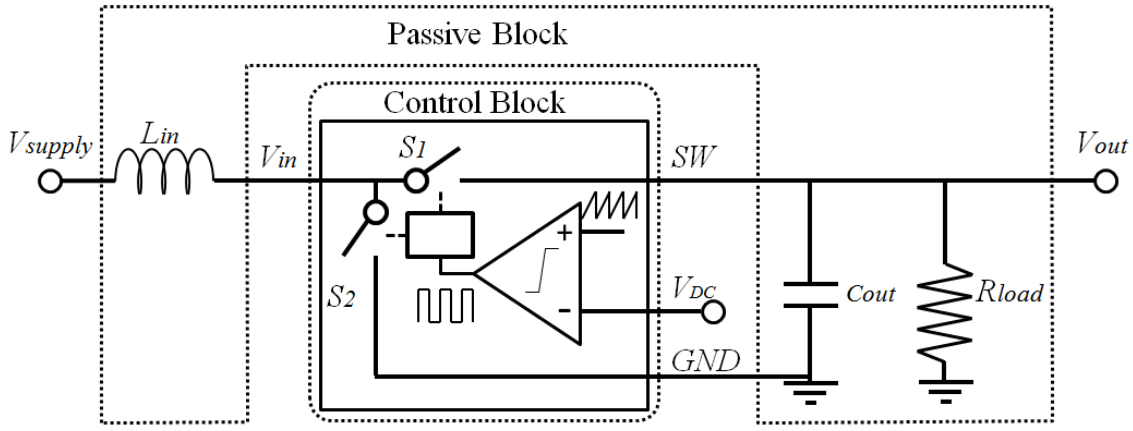


Figure 9: Block diagram of boost converter without feedback control.

An open-loop boost converter also consists of two blocks as shown in Figure 9: control block and passive block. The control block generates a current pulse train whose *amplitude* is directly proportional to the output voltage generated by the converter. When the output voltage falls below the stipulated output voltage value, the pulse width is increased and vice versa (negative feedback, shown in Figure 10). The pulse train is generated by comparing a periodic ramp signal with a reference voltage (V_{DC}) derived by scaling and filtering the output voltage of the converter. When the reference voltage is low, the comparator in Figure 9 produces a pulse train with higher width and vice versa. The output of the PWM controls the ON and OFF states of switches S_1 and S_2 in Figure 9. When S_2 is turned on by a "low" value of the pulse train, the current through the inductor increases linearly, and the energy is stored in the inductor. Subsequently, when the output of the comparator becomes "high," S_2 is turned off, and S_1 is turned on. The current through the inductor continues to flow in the same direction as before, releasing the energy stored in the inductor as the current decreases linearly with time charging the output capacitor, and the process is repeated.

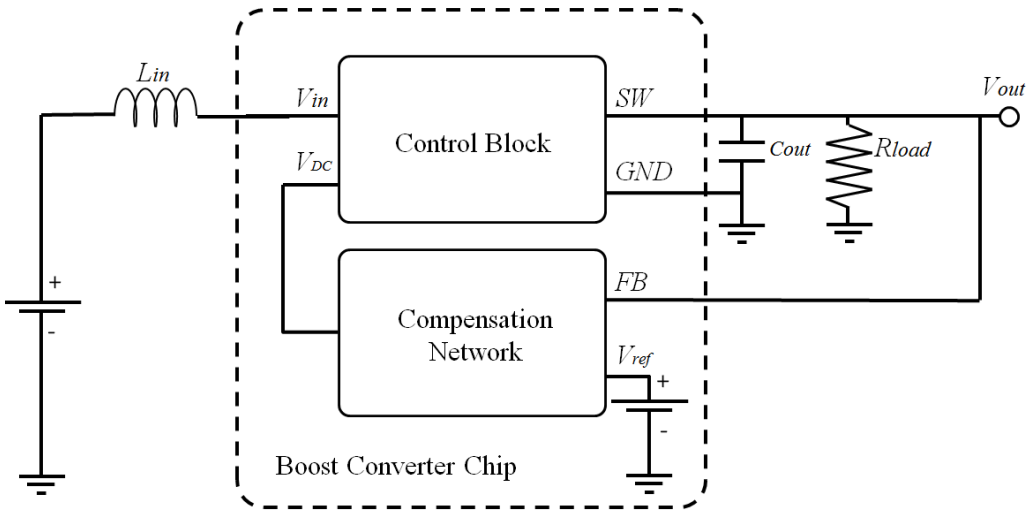


Figure 10: Block diagram of boost converter with closed-loop feedback control.

Assuming that the type III compensation network shown in Figure 7 is used, the loop transfer function is given by Equation 5[59].

$$H_{comp} = -\frac{(C_2R_2s+1)(sC_3(R_1+R_3)+1)}{R_1s(C_1+C_2)(\frac{C_1C_2R_2}{C_1+C_2}s+1)(C_3R_3s+1)} \times \frac{(R_{load}+R_{ESR})(sC_oR_{ESR}+1)(D'^2\,R_{load}{}^2-(sL_o+R_{DCR})(R_{load}+R_{ESR}))R_{load}V_{in}}{(D'R_{load}(D'R_{load}+R_{ESR})+R_{DCR}(R_{load}+R_{ESR}))P(s)} \quad \text{Equation 5}$$

where

$$P(s) = L_oC_o(R_{load}+R_{ESR})^2s^2 + (L_o(R_{load}+R_{ESR})+R_{DCR}C_o(R_{load}+R_{ESR})^2+D'R_{load}R_{ESR}C_o(R_{load}+R_{ESR})) + R_{DCR}(R_{load}+R_{ESR})+D'R_{load}(D'R_{load}+R_{ESR}) \quad \text{Equation 6}$$

In both equations, R_{ESR} and R_{DCR} are serial resistances associated with capacitor C_o and inductor L_o, respectively. Since the boost converter has an inherent right half-plane (RHP) zero at $f_{Z1} \approx R_{load}V_{in}{}^2/(2\pi LV_o{}^2)$, its stability also depends on the load resistance R_{load}.

2.2 Test Risk Analysis for Power Converters

In production test and post-manufacture tuning, the converter DUTs are interfaced with the ATE load board through a socket, which brings extra parasitic inductances[2] . The power and ground traces between the power supply and ground pins of the DUT and the corresponding terminals of the load board present significant parasitic inductances shown in Figure 11 and referred as L_{p1}, L_{p2}, L_{p3}, and L_{p4}. The pins of the "converter chip" in Figure 8 (buck converter) and Figure 10 (boost converter) are referred as pin *SW* in Figure 11, and the feedback voltage is connected to pin *FB* (the inverting input of the error amplifier presented in Figure 7). In general applications, the effects caused by the relevant inductances are minimized by placing large capacitors close to the pin V_{in} and the pin *GND* of the converter. However, this is not feasible during production test since capacitors can only be placed on the side of the V_{in} and *GND* leads between the test socket and the load board (on the side of the load board only). Therefore, because of the absence of decoupling capacitors connected directly to pins V_{in} and *GND* of the DUT to alleviate the effects of the lead inductances L_{p1} and L_{p2} in Figure 11, the current discontinuity caused by switching and the converter high load current caused voltage oscillations and severe voltage spikes at pin V_{in} (for buck converter) and pin *GND*(for both buck and boost converters) of the DUT, resulting in destructive high-voltage values across the DUT and switching MOSFETs.

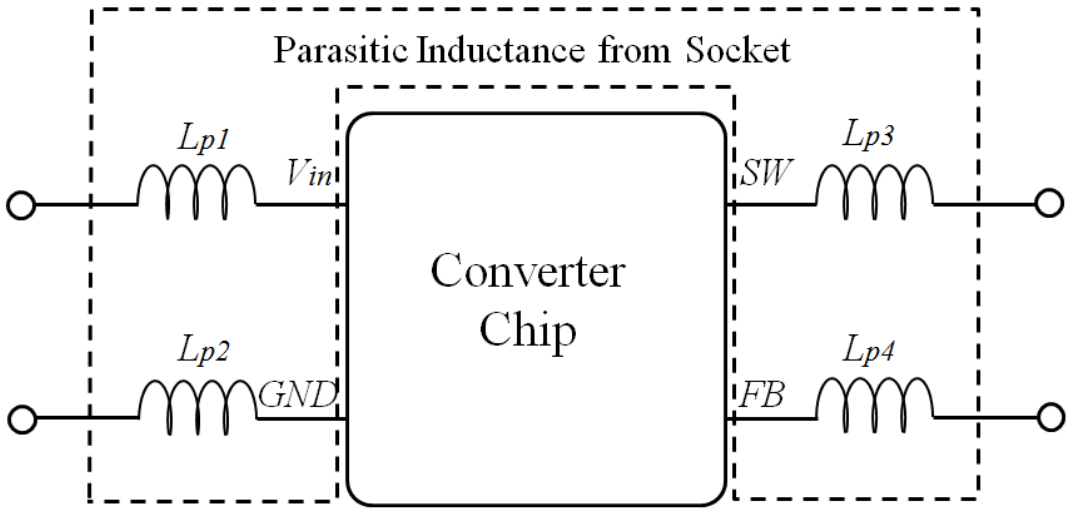


Figure 11: Block diagram of power converter in socket.

Since the same current discontinuities are observed in both types of power converters, buck converter is used as an example for the following voltage spike analysis:

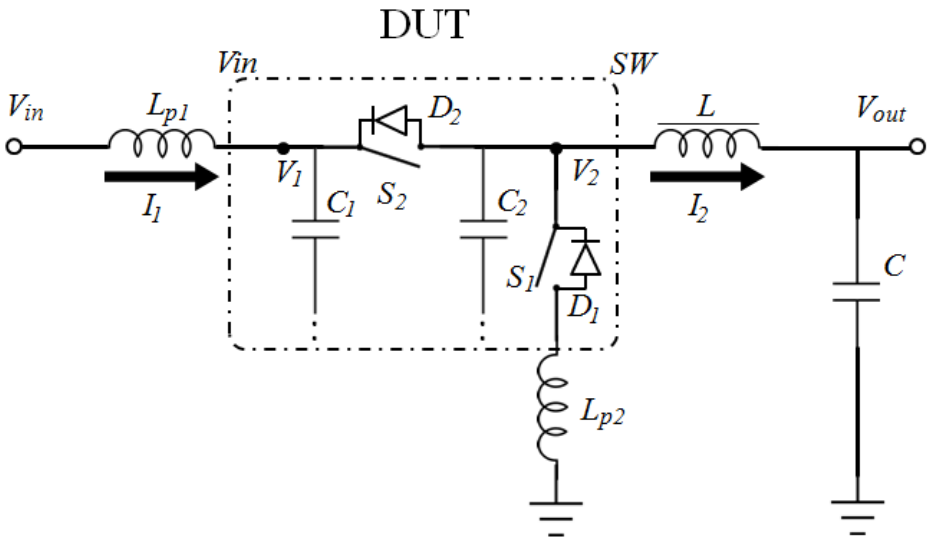


Figure 12: Equivalent circuit of power switch stage for spike analysis.

For analyzing the causes and properties of these voltage spikes, the output switch stage is presented in Figure 12. Since the built-in body-drain diode and the power transistor act independently during operation, simplified models of the switch transistors are used for

simpler analysis. In Figure 12, C_1 represents the input pin capacitance at pin V_{in}, and C_2 represents the pin capacitance at pin *SW*. Switches S_2 and S_1 represent the top and bottom transistors, respectively. Because of the similarity and symmetry between pin V_{in} and pin *GND*, only voltage spikes at pin V_{in} and pin *SW* are analyzed.

As mentioned in the previous section, in steady state, the output current I_2 is continuous with a negligible ripple. In order to simplify the analysis, I_2 is considered as a DC current. The switching process is divided into three stages based on the states of switches S_2 and S_1. In stage 1, the circuit is stable with S_2 in ON state and S_1 in OFF state. As a result, $I_1 = I_2$ and $V_{in} \approx V_1$ (since $L_1 << L$). In stage 2, S_2 is turned off, and in order to avoid the formation of a path for current to "shoot through" from V_{in} to ground, S_1 remains off. The current in L_{p1} flows continuously since the inductor resists changes in current. This current charges C_1 and results in an increase of V_1. When the energy stored in L_{p1} is completely dissipated, C_1 starts to release energy, resulting in a decline in V_1 and an increase in I_1 in the opposite direction. The frequency f_{v1} and peak voltage V_{Pv1} of this oscillation are given in Equation 7 and Equation 8 below:

$$f_{v1} = \frac{1}{2\pi\sqrt{L_{p1}C_1}} \qquad \text{Equation 7}$$

$$V_{Pv1} = \sqrt{2(\frac{1}{2}C_1V_{1\_int}^2 + \frac{1}{2}L_{p1}I_{1\_int}^2)/C_1} \qquad \text{Equation 8}$$

where V_{1_int} and I_{1_int} are V_1 and I_1 at the end of stage 1, respectively. Since both switches are off, the large inductor L sinks current from capacitor C_2, resulting in a decrease in V_2. This decrease is calculated through Equation 9.

$$\Delta V_{stage\_2} = \frac{I_2}{C_2}\Delta t \qquad \text{Equation 9}$$

When V_2 drops below D_1's built-in potential or switch S_1 is turned on, stage 3 is enabled. In stage 3, the bottom switch is in the ON state (either through D_1 or S_1). Since inductor L_2 resists changes in current, the current in L_2 increases gradually, while the output current I_2 constantly drains charge out of C_2, resulting in a further decline of potential at pin *SW*. The *LC* circuit formed by L_2 and C_2 results in oscillations, and this voltage variation is calculated and presented in Equation 10, where t represents the relative time after stage 3 commences and $V_{3\_int} = V_{in} - \Delta V_{stage\_2}$.

$$V_2 = 2C_2RV_{3\_\text{int}} - \frac{\beta(\cosh(\omega t) - \dfrac{\sinh(\omega t)(\dfrac{R}{2L_{p2}} - \dfrac{\alpha}{\beta})}{\omega})}{C_2L_{p2}e^{\frac{Rt}{2L_{p2}}}} \qquad \text{Equation 10}$$

In Equation 10, R represents the resistance between the capacitor C_2 and the ground. The parameters ω, α, and β are represented below:

$$\omega = \frac{\sqrt{\dfrac{C_2R^2}{4} - L_{p2}}}{\sqrt{C_2}L_{p2}} \qquad \text{Equation 11}$$

$$\alpha = I_2L + 2C_2RV_{3\_\text{int}} \qquad \text{Equation 12}$$

$$\beta = 2V_{3\_\text{int}}C_2{}^2R^2 + I_2L_{p2}C_2R - L_{p2}V_{3\_\text{int}}C_2 \qquad \text{Equation 13}$$

The whole process repeats when switch S_1 is turned off and switch S_2 is turned on again. Based on this analytical discussion, it is seen that the amplitude of voltage peaks is directly proportional to I_2, L_{p1}, and L_{p2} and inversely proportional to C_1 and C_2.

A SPICE model is built to demonstrate the spikes discussed above. In this demonstration, $C_1=C_2=10pF$, $L_{p1}=L_{p2}=20nF$, $R=10\ Ohm$, $V_{in}=5V$, and $I_2=1A$. And the length of stage 2 is set to $10nS$. The simulated results are presented in Figure 13. In Figure 13, all symbols are consistent with those in Figure 12. I_{S1} and I_{D1} denote currents flowing through the bottom transistor S_1 and its body-drain diode D_1, respectively.

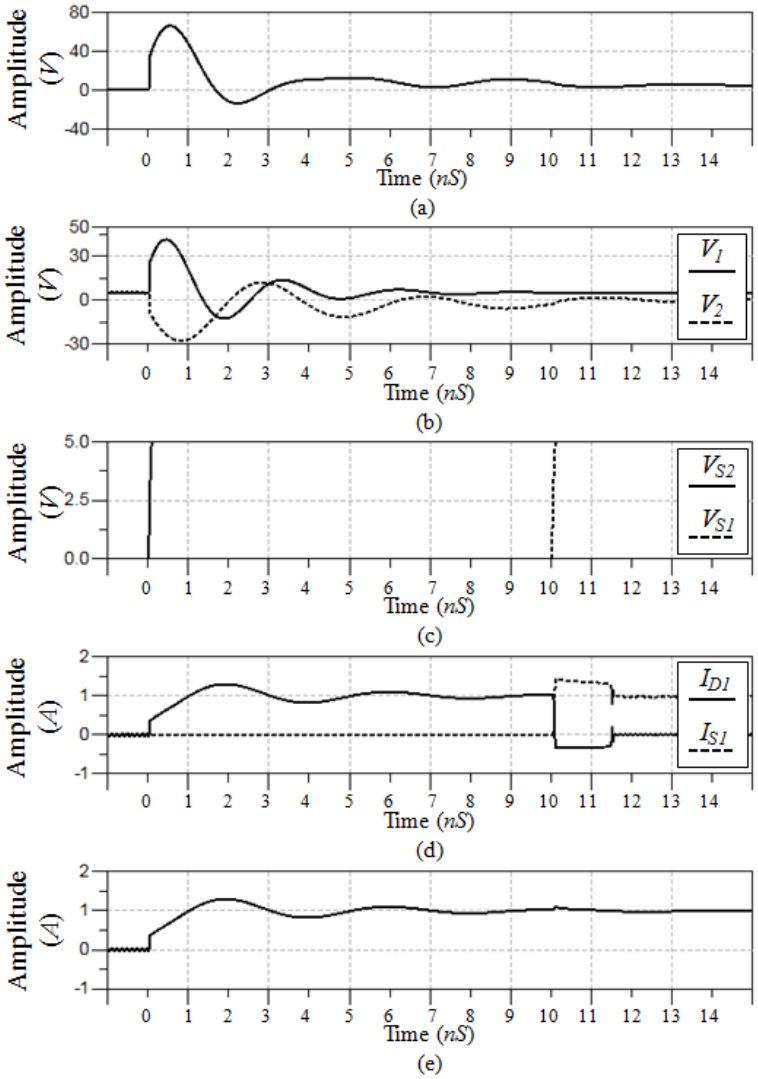


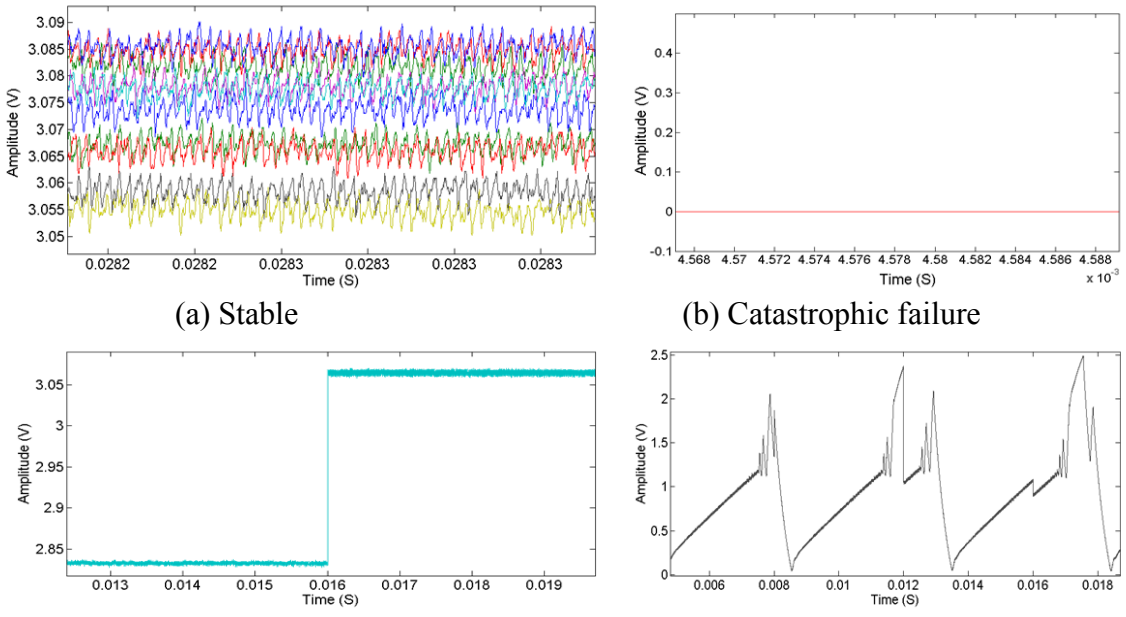
Figure 13: Simulated results for (a) voltage across top transistor, (b) voltages at V1 and V2, (c) control voltage of top and bottom transistors, (d) currents through bottom transistor and its built-in diode, and (e) total current through bottom transistor.

In the simulated results, before *0nS*, the circuit operates in steady state and $V_1=V_2$. The top transistor is turned off at *0nS*, which results in a voltage spike $V_{Pv1}=42V$ in V_1 at pin V_{in} of DUT. V_2 follows Equation 10 and reaches a negative voltage spike $\Delta V_{stage\_3}=-28V$. Although the worst-case scenario gives the maximum voltage across the top transistor as $V_{Pv1}- \Delta V_{stage\_3}=70V$, the simulated value is $66V$ due to the difference in oscillating frequency between V_1 and V_2. These voltage spikes at V_1 and V_2 far exceed the tolerable voltage region of DUT and can result in a fatal DUT damage. Thus, it is proved analytically and confirmed numerically that using conventional closed-loop test in production test for buck converters is not feasible.

CHAPTER 3: ALTERNATIVE SAFE TEST

In this chapter, novel alternative built-in test structures, which are specially tailored for power converters, are presented. During the alternative test, a sequence of carefully crafted perturbations is injected through specially designed circuitry into the feedback loop of the converter. The response of the converter to the applied perturbations is captured and passed through a defect filter[60, 61] and a stability filter to determine the type of possible failure. After the DUT's response passed the filters, it is then used to predict specifications, such as load/line regulation, DC voltage, ripple voltage, and transient voltage peak, through a preconstructed statistical mapping model for pass/fail/marginal classification.

3.1 Overview



(a) Stable (b) Catastrophic failure

(c) Regulation failure (d) Stable failure

Figure 14: Measured response for buck converter in conventional load/line regulation test.

To design an alternative system that classifies DUTs and performs predictions of difficult-to-measure test specifications such as load/line regulation, a case study is performed, and 20 test responses of untrimmed buck converter IC under conventional load/line regulation measured with test bench are shown in Figure 14 above. Since no socket was used, the risk of voltage spike was avoided. The failures shown in Figure 14 are classified into two groups: catastrophic failure, as indicated in Figure 14(b), which cannot be fixed through tuning, and minor failures, which include regulation failure and stability failure as shown in Figure 14(c) and (d). The DUT is discarded when it is diagnosed as a catastrophic failure and passed to further measuring and tuning when it has minor failures.

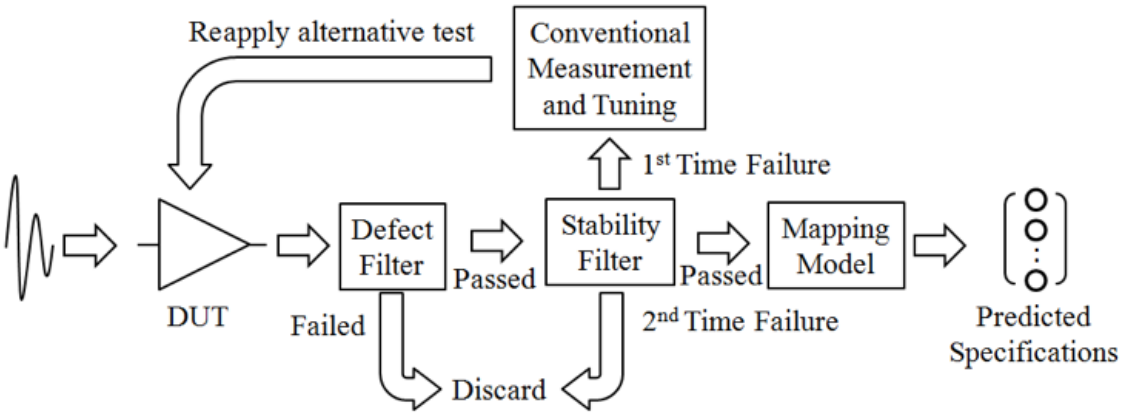


Figure 15: Complete alternative test flow with defect filter.

The block diagram of the proposed alternative test is shown in Figure 15. It consists of two more blocks when compared with a typical alternative (signature) test flow discussed previously in Figure 4: a defect filter and a stability filter. The defect filter is designed to remove outliers (catastrophic failure, Figure 14[b]) since they are inconsistent with the statistical nature of the training set and will affect the fit results[61]. Once the DUT is diagnosed as an outlier, it is discarded as faulty. After the defect filter, the captured

perturbed response is passed to the stability filter to classify DUT's stability. Once the DUT is diagnosed as unstable (minor failure, Figure 14[c] and [d]), it is subjected to a conventional correlation-based tuning, and it is retested after. If the tuning does not fix the stability problem, this DUT will be discarded.

3.2 Test Generation

As mentioned previously, the parameters that define the perturbation/stimulus need to be optimized in such a way that the correlation between perturbed output response and targeted specifications is maximized. Assuming that all the parameters that are required to be optimized are quantified and included in the vector set P_{opt}, a genetic algorithm (GA)[62] based optimization algorithm is proposed in Figure 16 to optimize the perturbation/stimulus.

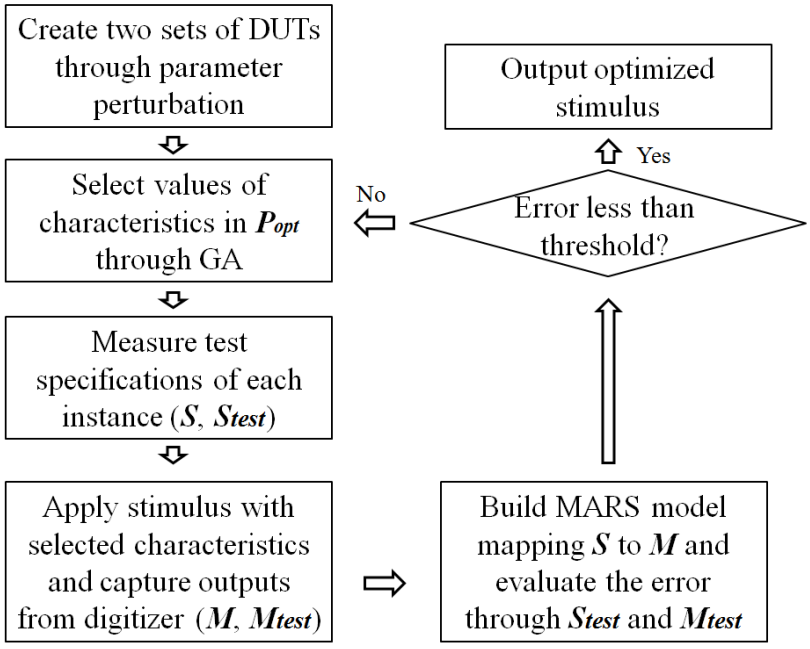


Figure 16: GA based optimization flow chart

As shown in the Figure, two sets of DUTs are created by sampling the process space for a specified process statics. The values of perturbation/stimulus' parameters (details are perturbation depended and are discussed in later section) in P_{opt} are then selected by

the GA within their given boundaries. The captured stimulated/perturbed response (M, M_{test}) and the test specification (S, S_{test}) of each instance of the two sets are both measured. The perturbed/stimulated responses (M) and test specifications (S) of first set of instance are used to construct a nonlinear regression model that relates the captured data to the target test specification values. The second set of DUT instances (each instance corresponds to a DUT with unique specification values generated via statistical sampling of the performance space of the converter) is used to evaluate the regression model to determine the accuracy with which specifications are predicted by the model. If the prediction error (defined by the cost function) from the model is larger than a desired threshold, the digital sequence is dropped, and the GA picks a new set of values in P_{opt}, and the entire procedure is repeated. Figure 17 shows the optimization process with the MSE between the predicted specifications and measured specifications as the cost function. The algorithm converges in six generations and reaches the optimized stimulus.

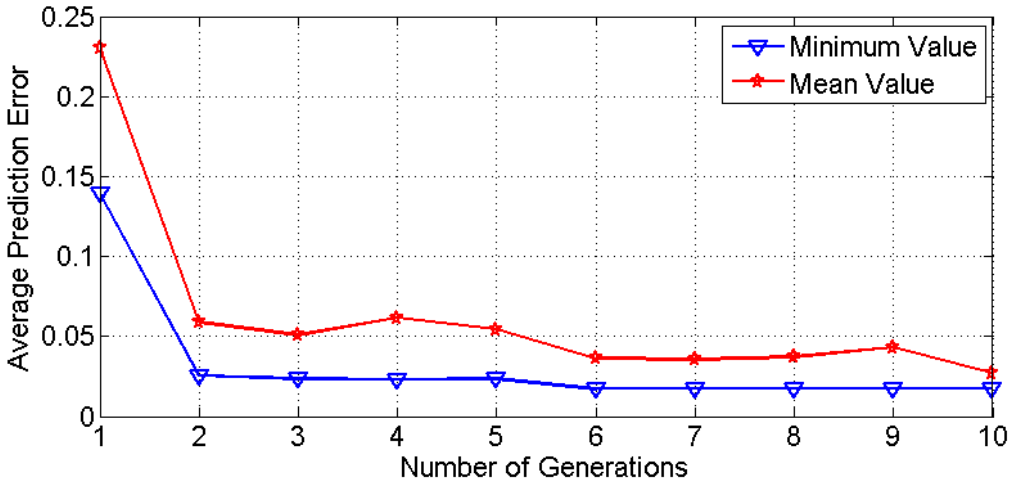


Figure 17: Optimization of stimulus by GA

3.3 Defect Filter

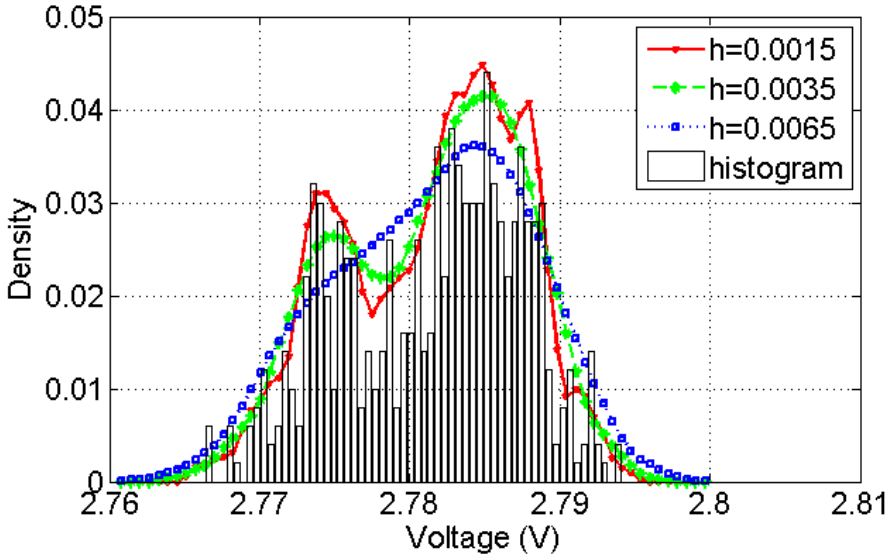


Figure 18: Estimated density function with different bandwidth.

The proposed defect filter uses the joint probability density function estimated by kernel density estimator as a statistical reference. It calculates the estimated data distribution at each observation (each captured data point) and declares DUT as an outlier if all values of its captured output responses (observations) have zero probabilities in their estimated distribution functions.

Practically, the density estimator for each data point is defined by

$$\hat{f}_h(x) = \sum_{i=1}^{n} n^{-1} h_i^{-d} K(h_i^{-1}(x - x_i)) \qquad \text{Equation 14}$$

where *K(.)* is the quartic kernel function,

$$K(u)=\begin{cases}\frac{15}{16}(1-u^2)^2 & |u|\le 1\\ 0 & otherwise\end{cases}$$ Equation 15

x_i, $i=1,...,n$, is a d-dimensional vector that contains d alternate measurements (observations) of i^{th} device. h_i is the local bandwidths for i^{th} device, and its value is selected based on[61, 63]. The density estimator estimates the density distribution of each observation across n devices and classifies a device as outlier when all of that device's observations lying outside their corresponded estimated density functions ($\hat{f}_h(x)=0$).

This density estimation process can be interpreted as a sum of the quartic kernel functions whose center point is sweeping across the range of observation data. Bandwidth parameter h_i controls the coverage of each kernel functions, and its value affects the smoothness of the estimated density function. Figure 18 demonstrates the effect of h_i over the estimated density function of the first sampling point crossing 500 devices.

3.4 Stability Filter

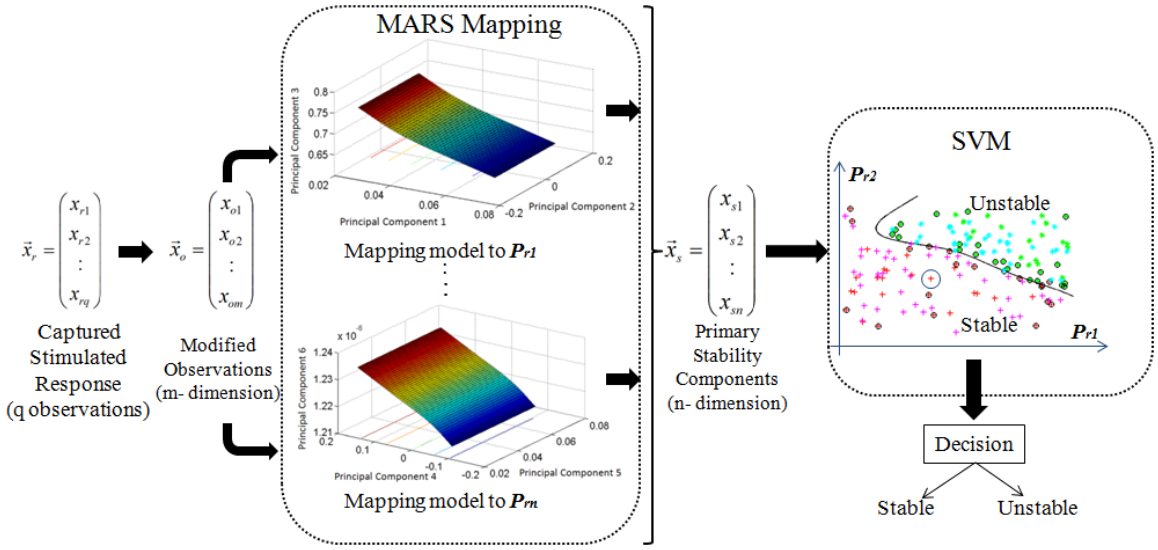


Figure 19: Decision process of stability filter.

The stability of a power converter is defined as the amplitude of its output ripple voltage. Once its output ripple voltage is beyond the guard band, the converter is considered as unstable. It can either fail the regulation (Figure 14[c]) or oscillate unstably (Figure 14[d]). Figure 19 shows the working flow of the proposed stability filter. The captured response $\vec{x}_r$ (sampled by ADC) is piecewise averaged based on LFSR's (linear feedback shift register)[64] frequency to remove high-frequency noise. The averaged output is calculated using Equation 16:

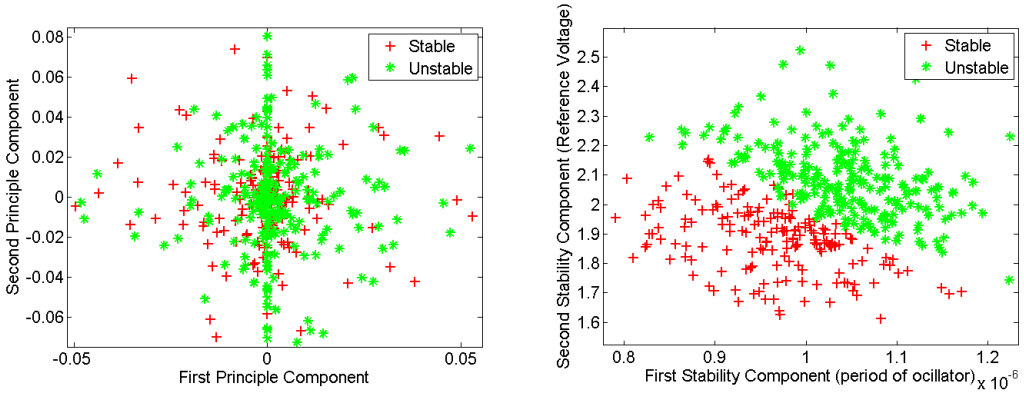
$$x_o(j) = \sum_{i=1}^{N} x_r(i + N \cdot j) / N, N = \left\lfloor \frac{f_{sw}}{f_S} \right\rfloor \qquad \text{Equation 16}$$

where f_{sw} is the switching frequency of boost converter, and f_S is the sampling frequency of data acquisition ADC. The vector $\vec{x}_o$ is then mapped to "primary stability components (PSC)" ($\vec{x}_s$) through pre-calculated MARS models. These "primary stability components" are some circuit parameters to which the stability is most sensitive. Though the actual components that $\vec{x}_o$ should be mapped to depend on converter design, the general sensitive parameters include reference voltage, gain of error amplifier, oscillator frequency, and estimated position of poles and zeros of the system. A support vector machine (SVM) is then used to decide the converter's stability based on $\vec{x}_s$.

The construction of stability filter involves two major steps: first, MARS mapping models need to be constructed to map modified observations ($\vec{x}_o$) to PSCs ($\vec{x}_s$) that have higher correlations to the converter's stability. Then a SVM needs to be built to classify the converter's stability.

As mentioned previously[30], the alternative measurement space is correlated to circuit parameters space, and hence, a standard MARS model training process is able to map captured response to the selected circuit parameters. The detail of the training process has already been covered in Section 3.2.

In our case, two parameters P_{r1} and P_{r2} (oscillator's period and reference voltage) have been selected as PSCs, and two MARS models are constructed accordingly. Figure 20 below shows how these mappings can result in a clear boundary between stable (red circles) and unstable devices (green stars) when compared to principle component analysis.



(a) (b)

Figure 20: Components (a) before MARS mapping and (b) after MARS mapping.

The second step is to construct a SVM for stability classification purpose. A SVM is a supervised learning model that constructs a hyperplane or a group of hyperplanes in high dimensional space for data separation. The task of this SVM and its training stage can be formulated as below:

Given a set of training examples,

$$(\vec{x}_{s1}, y_1),...,(\vec{x}_{sm}, y_m), \vec{x}_{si} \in \Re^N, y_i \in \{stable, unstable\}$$ Equation 17

where N is the number of PSCs obtained in previous step for each test case, and m is the total number of training examples. And define a set of decision functions.

$$\{f_i(\vec{x}_s) : i \in \Re, \vec{x}_s \in \Re^N\}, f_i : \Re^N \to \{-1(stable), 1(unstable)\}$$ Equation 18

SVM can select a decision function $f_k(\vec{x}_s)$ such that the possible value of the risk (Equation 18) is minimized:

$$R(k) = \int \left| f_k(\vec{x}_s) - y \right| dP(\vec{x}_s, y)$$ Equation 19

where *P(.)* is an unknown probability distribution. Since the proposed stability filter is based on a nonlinear SVM that uses Gaussian radial basis function as its nonlinear kernel function[65], the decision function takes the form of

$$f(\vec{x}_s) = \text{sgn}(\sum_{i=1}^{l} y_i \alpha_i K(\vec{x}_s, \vec{x}_{si}) + b)$$ Equation 20

where *K(.)* is the Gaussian radial basis function, and it is in the form of

$$K(x, x_i) = \exp(-\left\| x - x_i \right\|^2 / c)$$ Equation 21

All the parameters are obtained by maximizing the following equation:

$$W(\alpha) = \sum_{i=1}^{l} \alpha_i - \frac{1}{2} \sum_{i,j=1}^{l} y_i y_j \alpha_i \alpha_j K(\vec{x}_{si}, \vec{x}_{sj})$$ Equation 22

under the constraint

$$0 \le \alpha_i \le \gamma, i = 1,...,l, and \sum_{i=1}^{l} a_i y_i = 0$$ Equation 23

where l is the total number of training devices, γ is a positive constant [66] , and

$$y_i = \begin{cases} -1, & when\ device\ i\ is\ stable \\ 1, & when\ device\ i\ is\ unstable \end{cases}$$ Equation 24

This quadratic programming optimization problem can be solved by conjugate gradient method or some other quadratic programming solvers. In addition, the details about SVM supervised learning process is concluded in [65]. Since not all PSCs can result in a clear boundary, SVM based on all possible combinations of PSCs are built, and the one with the best performance is selected. This performance evaluation process is described below.

Denoting stable case as "true" and unstable one as "false," three figures of merit based on the numbers of true positive (TP), true negative (TN), false positive (FP), and false negative (FN) are used to evaluate the performance of SVM models. These figures of merit are fault coverage (FC), pass coverage (PC), and accuracy (AC). They are calculated by [67]

$$FC = \frac{TN}{TN + FP} \cdot 100\%$$ Equation 25

$$PC = \frac{TP}{TP + FN} \cdot 100\%$$ Equation 26

$$AC = \frac{TP + TN}{TN + FP + TN + FP} \cdot 100\%$$ Equation 27

And the evaluate function to SVM's performance is

$$f_{eva}(P_{r1}, P_{r2}, P_{r3}) = W \cdot FC + PC$$ Equation 28

where W is a weighting factor with a value larger than 1 to avoid FP at all cost.

3.5 Test Structure

3.5.1 Open-Loop Test Structure for Buck Converter

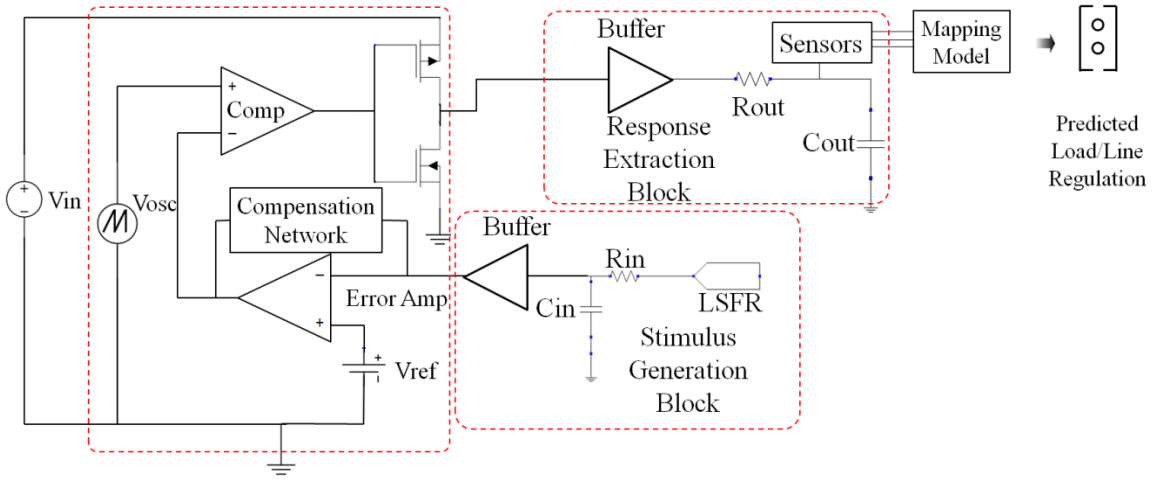


Figure 21: Block diagram of buck converter in BIT setup with feature extracting sensors.

The proposed alternative test setup uses an open-loop test configuration to increase the sensitivity of the DUT response to parametric variations as shown in Figure 21. Buffers are used to isolate the test instrumentation resources from the converter. This also limits the output transistor's load current to resolve the voltage spike problem.

Two low-pass filters consisting of R_{out}, C_{out}, R_{in}, and C_{in} are designed based on Equations 3 and 4 to match the band-limiting behavior of the closed-loop converter to eliminate undesired noise from high-frequency components that do not exist in closed-loop test.

$$\frac{1}{2\pi R_{in}C_{in}} = f_{ZP} \qquad \text{Equation 29}$$

$$\frac{1}{2\pi C_{in}R_{in}} < \frac{1}{2\pi C_{out}R_{out}} << f_{osc} \qquad \text{Equation 30}$$

In the above equations, f_{ZP} is the 3 dB cutoff frequency mentioned in Section 2, and f_{osc} is the frequency of periodic ramp signal V_{osc} fed to the input of the comparator of Figure 6.

The test stimulus is an n-bit pattern with V_{b1} and V_{b0} denoting logic high and logic low, respectively. In order to ensure that the stimulus covers the linear region of operation of the error amplifier of the converter, the following equations have to be satisfied:

$$\frac{R_{Nerror}}{R_{Nerror}+R_{in}}\frac{(V_{b1}-V_{b0})}{2}=V_{ref} \qquad \text{Equation 31}$$

$$V_{b1} \le V_{Psat},\ V_{b0} \ge V_{Nsat} \qquad \text{Equation 32}$$

where R_{Nerror} is the standard input impedance of the error amplifier, and V_{Nsat} and V_{Psat} are the negative and positive saturation voltages of the error amplifier.

3.5.2 Closed-Loop Test Structure

3.5.2.1 Buck Converter

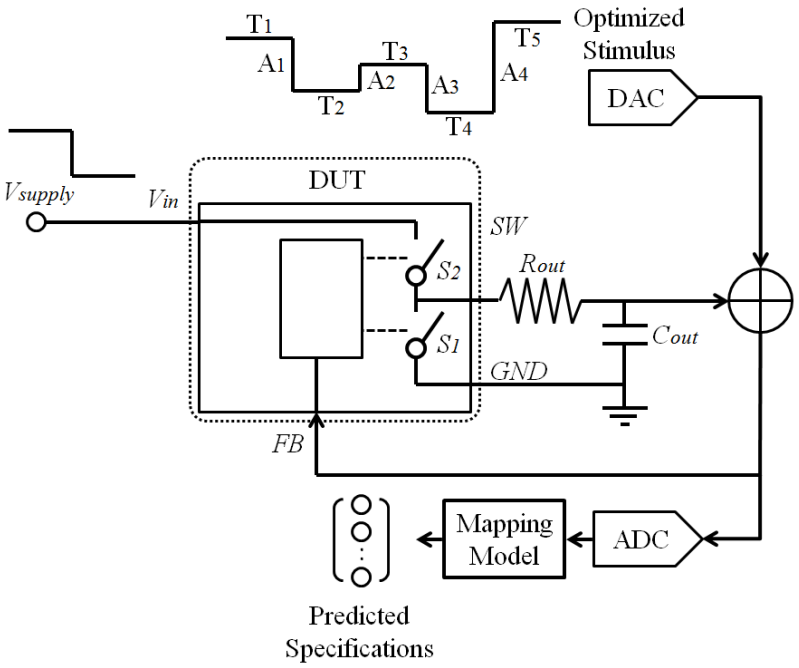


Figure 22: Block diagram of buck converter in proposed test setups.

The proposed alternative test setup uses a modified *RC* low-pass filter as shown in Figure 22. The 3 dB cutoff frequency of the *RC* low-pass filter is designed to be the same

as that of the *LC* low-pass filter of the nominal buck converter. Therefore, values of R_{out} and C_{out} satisfy the relation shown in Equation 33 below:

$$R_{out}C_{out} = \sqrt{LC} \qquad \text{Equation 33}$$

where *L* and *C* are values of inductor and capacitor in Figure 8, respectively. Test stimulus is a sequence of *K* voltage steps with controllable parameter sets T=[T_1 T_2 ... T_k] and A=[A_1 A_2 ... A_k] as shown in Figure 22. T_i and A_i denote the duration and amplitude of i^{th} step separately. Those parameters are generated by the test optimization algorithm described in Section 3.2 with the constraints listed below in Equation 34 and Equation 35:

$$T_s \leq T_i \leq 5T_s \qquad \text{Equation 34}$$

$$\frac{\Delta V}{2} - V_{out} \leq A_i \leq V_{in} - \frac{\Delta V}{2} \qquad \text{Equation 35}$$

where T_s is the settling time of the test circuit in Figure 22. The sampling frequency (f_s) of ADC is designed to be at least twice of the maximum oscillation frequency (f_{sw}) of the converter to avoid aliasing.

3.5.2.2 Boost Converter

The alternative test architecture for boost converter is more complicated since DUT operates in a different way as it is designed to be. As shown in Figure 23 below, input resistor R_{in} is used to limit input current and, hence, reduce the risk of voltage spikes at *GND* pin. The output resistor R_{out} is to provide a discharging path to avoid saturation on output voltage.

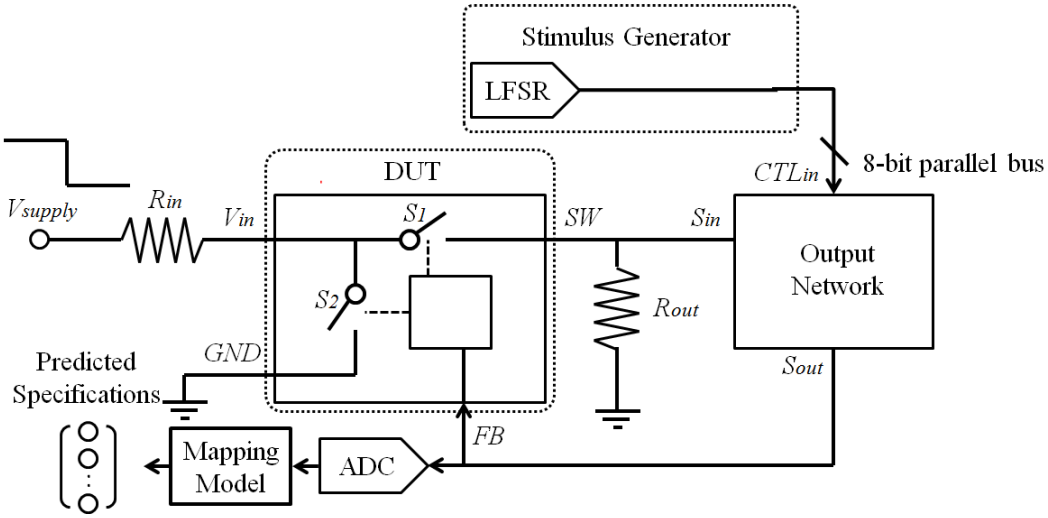


Figure 23: Block diagram of boost converter in proposed BIT configuration.

In conventional operation, the duty cycle of S_2 in Figure 23 is proportional to the averaged DC voltage at *SW* pin, and this relationship mode is expressed as [68]

$$\overline{V}_{SW} = \frac{V_{in}}{1 - D_{S2}} \qquad \text{Equation 36}$$

where D_{S2} denotes the duty cycle of switch S_2. However, in the proposed architecture, the duty cycle of S_2 is inversely proportional to the averaged DC voltage at *SW* pin, and it is calculated as

$$\overline{V}_{SW} = \frac{R_{out} V_{in}}{(R_{in} + R_{out})} D_{S1} \approx \frac{R_{out} V_{in}}{(R_{in} + R_{out})} (1 - D_{S2}) \qquad \text{Equation 37}$$

where D_{S1} is the duty cycle of switch S_1 and can be approximated as (1- D_{S2}). Therefore, the output network in Figure 23 should be designed in such a way that its output DC voltage level is inversely proportional to the averaged DC voltage of the pulse train at *SW* pin. The boost converter will only start regulating when this prerequisite is met. Because of this, the *RC* low-pass filter used in buck converter testing is not

applicable in boost converter case since its output DC voltage is proportional to its input ones.

In the proposed alternative test, the test stimulus is stored in a linear feedback shift register (LFSR) and injected as an 8-bit parallel digital sequence into the "Output Network" block to perturb the effective time constant and DC gain of this block. This perturbation then affects the loop gain and leads to a variation in feedback voltage, which is captured by an ADC and used to accurately predict specifications, such as load/line regulations, ripple voltage, and voltage transient peaks.

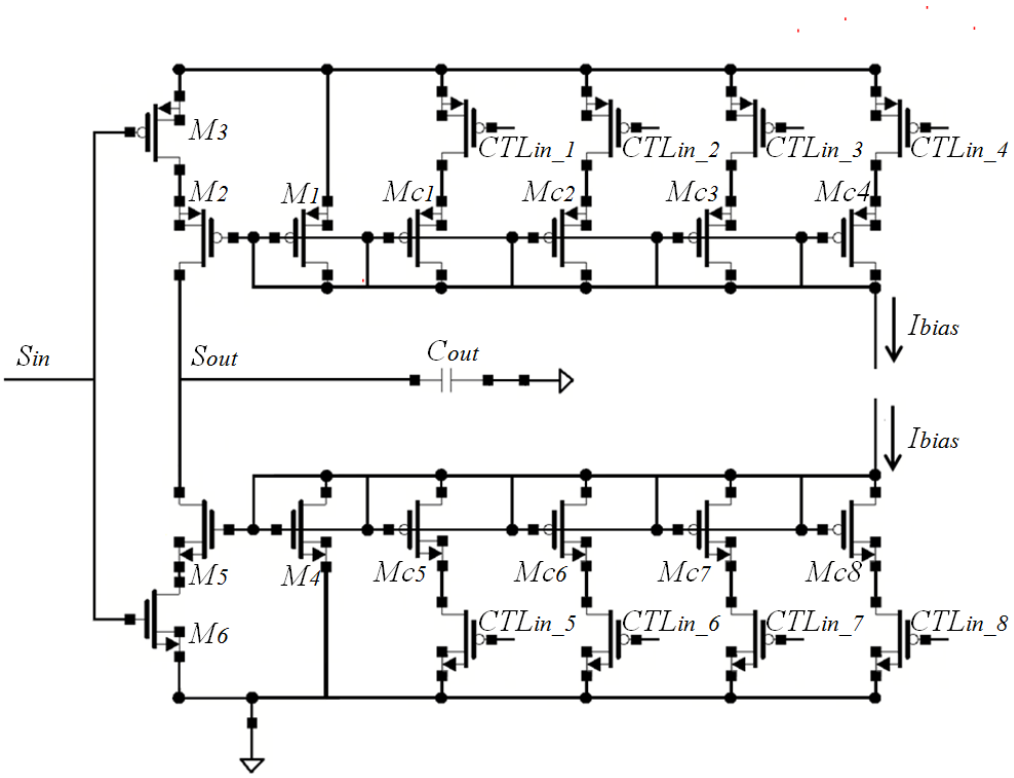


Figure 24: Proposed Output Network.

The transistor-level implementation of the proposed output network based on passive filter and a charge pump is proposed in Figure 24. Equation 38 should be satisfied to maximize the correlation between the alternative test setups and the conventional test setups.

$$\left(\frac{1+\lambda V_{DS}}{\lambda I_{inject}}\right)C_{out} = C_o R_{load} \qquad \text{Equation 38}$$

where C_o and R_{load} represent the capacitor and resistor's values used in normal application in Figure 10, I_{inject} denotes the bias current flows in/out the drains of transistor M_4/M_1, λ denotes the channel-length modulation parameter, and V_{DS} represents drain-to-source voltage of M_1/M_4.

The digital control signals from CTL_{in} pin are connected to gates of MOSFET M_{c1}–M_{c8} accordingly as shown in Figure 24. Depending on the state of each parallel branch, the injected current I_{inject} to C_{out} is given by Equation 39 below:

$$I_{inject} = \left(\frac{(W/L)_{M2}}{(W/L)_{M1} + \sum_{n=1}^{4} \alpha_{CTLin\_n}(W/L)_{Mcn}} - \frac{(W/L)_{M5}}{(W/L)_{M4} + \sum_{n=5}^{8} \alpha_{CTLin\_n}(W/L)_{Mcn}}\right) I_{bia.} \qquad \text{Equation 39}$$

where $(W/L)_{Mn}$ denotes the width-to-length ratio of transistor M_n. $\alpha_{CTLin\_n} = 1$ when control signal at CTL_{in_n} is "high" and $\alpha_{CTLin\_n} = 0$ when control signal at CTL_{in_n} is "low."

Both LFSR's output bit pattern and transistors M_{c1}–M_{c8}'s sizes are generated by the test generation flow described in Section 3.2 with the following constraints:

$$\frac{(W/L)_{M2}}{(W/L)_{M1}+\sum_{n=1}^{4}(W/L)_{Mcn}} I_{bias} < I_{inject} < \frac{(W/L)_{M2}}{(W/L)_{M1}} I_{bias} \quad \text{Equation 40}$$

$$f_{LFSR} < \frac{1}{5}\left(\frac{\lambda I_{bias}}{2\pi C_{out}(1+\lambda V_{DS})} \frac{(W/L)_{M2}}{(W/L)_{M1}+\sum_{n=1}^{4}(W/L)_{Mcn}} \right) \quad \text{Equation 41}$$

$$\frac{(W/L)_{M2}}{(W/L)_{M1}+\sum_{n=1}^{4}(W/L)_{Mcn}} = \frac{(W/L)_{M5}}{(W/L)_{M4}+\sum_{n=5}^{8}(W/L)_{Mcn}} \quad \text{Equation 42}$$

where f_{LFSR} is the bit rate of LFSR in Figure 23, and the constraints on transistor sizing based on fabrication technology should also be applied.

3.6 Simulation Results

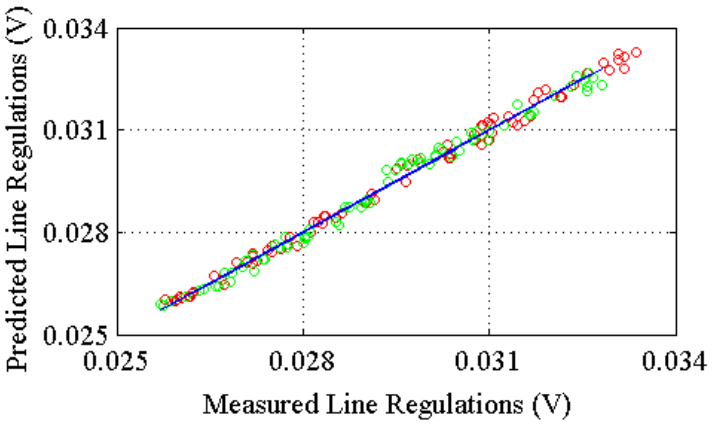
In this section, the proposed test methods for both buck and boost converters are demonstrated by simulations. To generate groups of buck/boost converter instances, a standard buck/boost converter is designed. Then by incorporating process variation effects through Monte Carlo simulation across all circuitries of this standard design, hundreds of instances with distinct specifications are created by sampling based on a standard design. These instances are further divided evenly into two sets for "training" (supervised learning) and "evaluation." The effects of the stability filter are also demonstrated in the boost converter section.

3.6.1 Open-Loop Test for Buck Converter

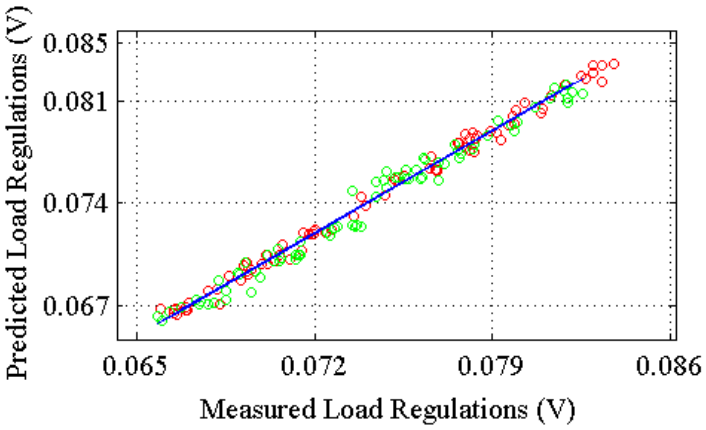
The proposed testing methodology is verified by simulation on a standard buck converter model (in Figure 6) with type III compensation network. The values of the passive components in type III compensation network (referring to Figure 7) are given as

C_1 = 7.64pF, C_2 = 12nF, C_3 = 4.7nF, R_1 = 7.5K, R_2 = 5.1K, R_3 = 2K. Sawtooth waveform (V_{osc}) in Figure 6 has an amplitude of 0.7 V and a frequency of 100 KHz.

There are 300 instances that are created by Monte Carlo sampling, incorporating process variation effects on this standard buck converter model. The variation effects are realized through randomly perturbing circuit parameters of standard buck converter within $\pm 20\%$ of its original value. These circuit parameters include resistance, capacitance inside the compensation network, reference voltage (V_{ref}), amplitude and frequency of sawtooth waveform (V_{osc} and f_{osc}), and some other critical parameters. These 300 instances are further divided evenly into two sets for "training" and "evaluating."



(a)



(b)

Figure 25: Simulated prediction of (a) line regulation and (b) load regulation.

Plots of line and load regulations for 300 training and evaluating circuits obtained using the conventional testing method and those predicted using proposed testing approach are displayed in Figure 25.The x-axis of the plots represents the line and load regulation value measured through conventional method, while the y-axis represents the line and load regulation predicted through the proposed methodology. The red dots are those training instances, and the green ones are those evaluating instances. The ideal 45^{o} blue line indicates the perfect correlation between the predicted and conventionally measured specifications. As Figure 7 shows, the prediction dots are accurately aligning

with reference blue line over a large range. And the maximum prediction error for load regulation is 1.52% and 2.26% for line regulation.

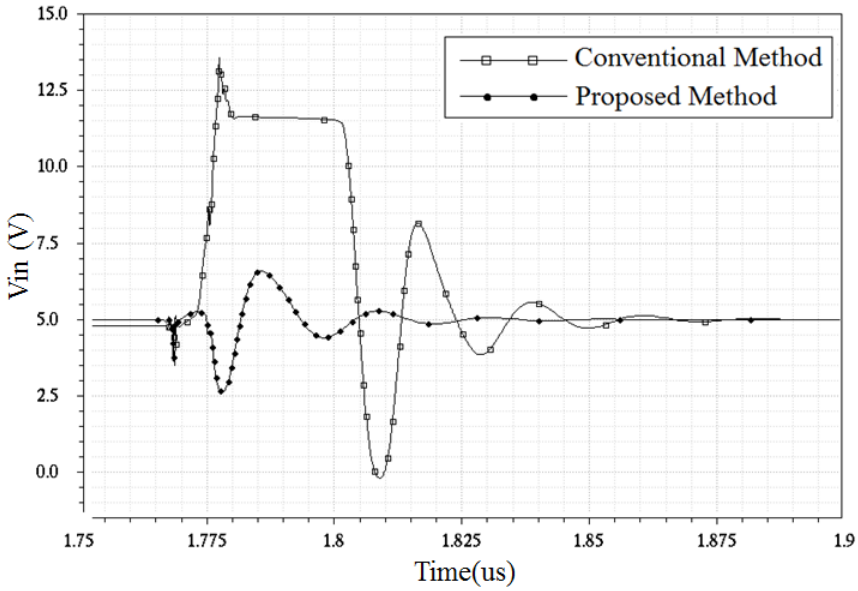
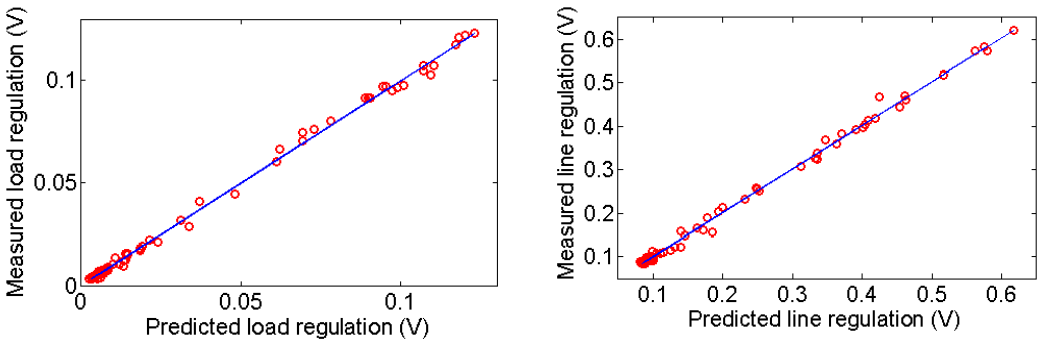


Figure 26: Compare of voltage at V_{in} during switching.

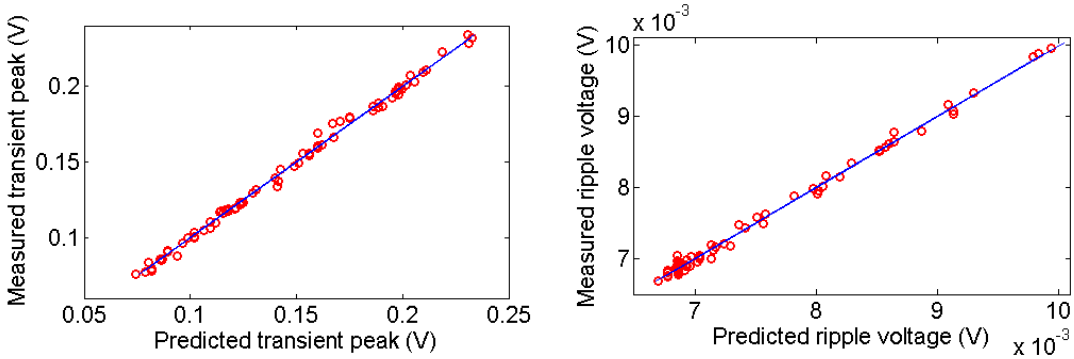
A transistor-level simulation is also done to prove the safety of the proposed method. The voltage at V_{in} in Figure 11 with both the conventional test method and the proposed method is compared in Figure 26. It can be seen from the plot that the large voltage spike has been greatly reduced.

3.6.2 Closed-Loop Test for Power Converter

3.6.2.1 Buck Converter



(a) (b)



(c) (d)

Figure 27: Buck converter simulated prediction of (a) load regulation, (b) line regulation, (c) transient peak, and (d) ripple voltage.

A buck converter is designed as the standard instance that takes input voltage in the range from 2.7 V to 5.5 V and able to source up to 5 A output current. Based on this standard buck converter design, 300 distinct instances are generated and used evenly for model training and evaluating purpose.

Figure 27 presents the scattering plots of line and load regulations, ripple voltage, and transient voltage peaks for 150 evaluating circuits. The y-axis of the plots represents the specification value measured through conventional method, while the x-axis represents the specification predicted through the proposed approach. Each circle in the figure stands for instances with specific predicted and measured specification. And the mean square error of line regulation is 8.38e-05, of load regulation is 3.96e-6, of transient voltage peak is 6.99e-6, and of the ripple voltage is 3.59e-9. This shows that the specifications are accurately predicted based on the proposed method and therefore proves the feasibility of the proposed method.

3.6.2.2 Boost Converter

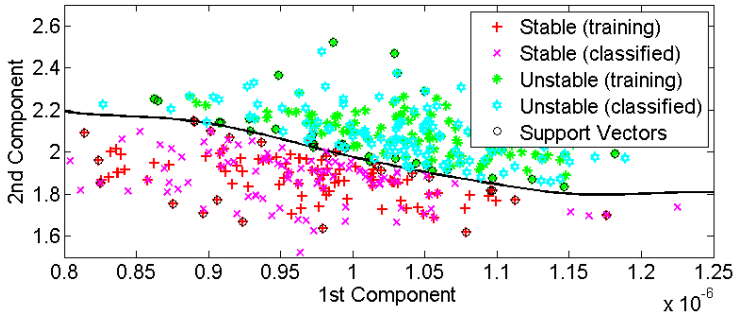


Figure 28: Plot of primary components of measurement pattern.

A standard boost converter is designed for instance generation. In order to prove more unstable instances to evaluate the performance of the proposed stability filter, each circuit parameter has been perturbed through Monte Carlo simulation with 10 times its original variance. Figure 28 above shows how classification has been done through proposed stability filter. Each point in the figure denotes a distinct device. The SVM model draws a boundary between stable and unstable region based on historical data. Once a device falls into "stable region," it is classified as stable and vice versa.

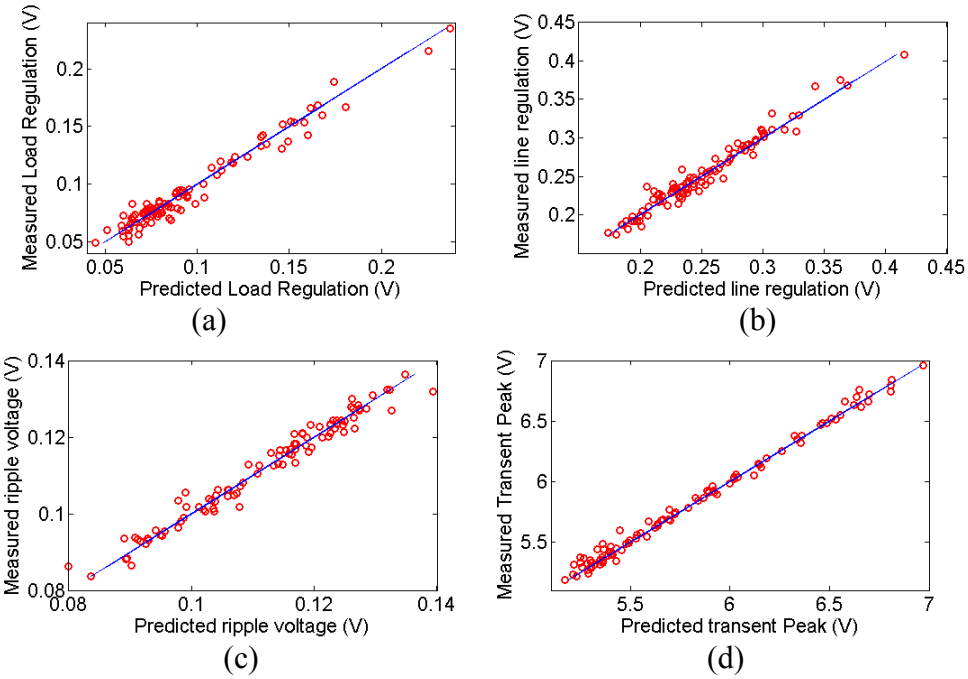


Figure 29: Boost converter simulated prediction of (a) load regulation, (b) line regulation, (c) transient peak, and (d) ripple voltage.

Based on the simulation, this proposed SVM-based stability filter has achieved a fault coverage of 98.6%, a pass coverage of 96.4%, and an accuracy of 97.6%.

The plots of predicted specifications for stable DUTs using the proposed testing approach are presented in Figure 29. The mean square errors for load regulation is 6.53e-5, for line regulation 4.34e-5, for transient peak 6.4e-4, and for ripple voltage 9.23e-6. Note that the predictions for boost converters are slightly worse than that of buck converter since the proposed output network in Figure 24 is also suffering from process variations.

3.7 Experimental Results

In this section, the proposed alternative methods for both buck and boost converters were validated through hardware experiments with real buck/boost converter test cases. The characteristics of proposed output network used in boost converter application were built through discrete transistor pairs, and its characteristics have also been studied.

3.7.1 Open-Loop Test for Buck Converter

A buck converter with proposed test circuit is implemented on a PCB for proof of concept. TL5001 is used as the buck controller, and a compensation network is designed based on that. Three single-pole five-throw switches are added to introduce perturbations on circuit parameters.

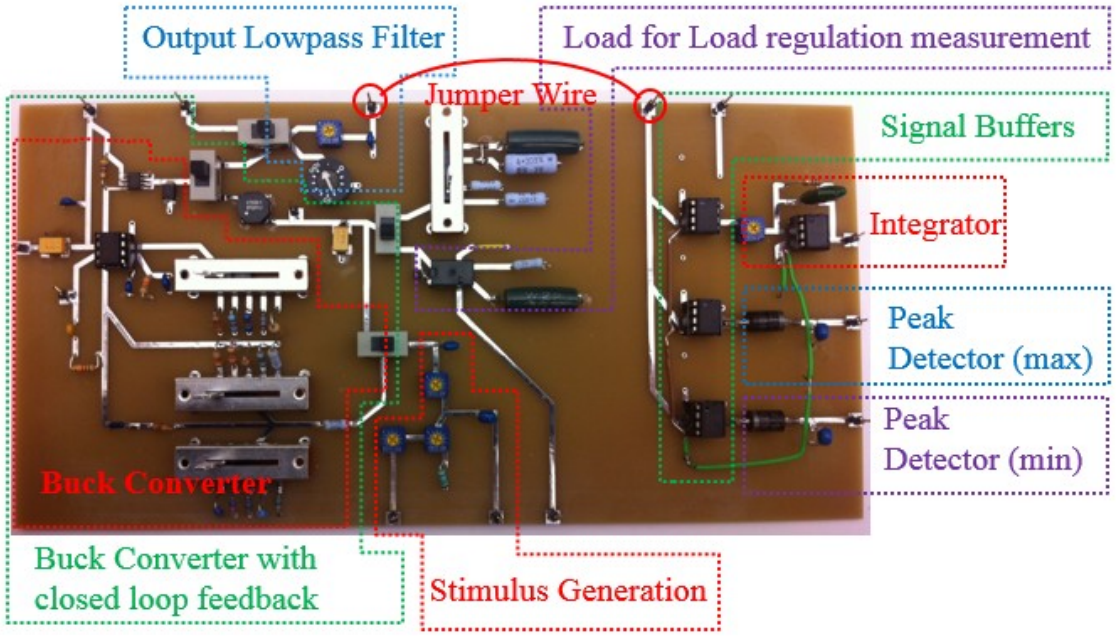
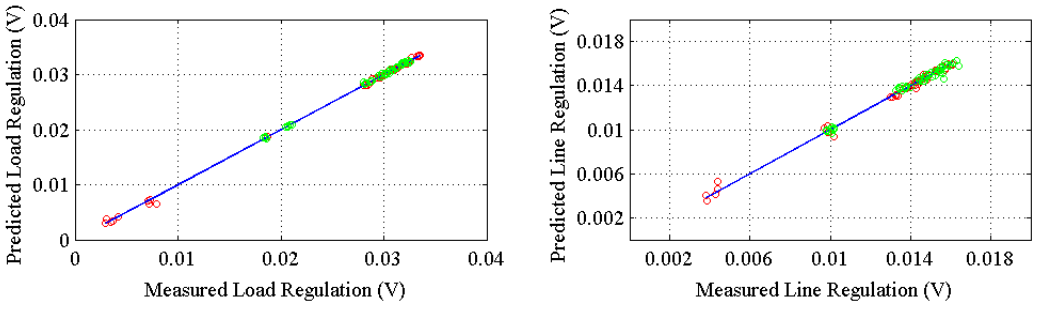


Figure 30: Circuit layout.

The circuit is fabricated, and each part is marked in Figure 30. The sensors are built separately and connected through jumper wire. Each switch has five different positions with different circuit parameters connected. In total, it generates 5^3=125 instances.

Among the 125 instances, 75 are used to train the regression model, and 50 are used to evaluate the prediction.



(a) (b)

Figure 31: Measured results (a) predicted vs actual load regulation and (b) predicted vs actual line regulation.

The results are plotted in Figure 31. This discrete distribution of load and line regulations is caused by discretely changed circuit parameters manipulated through

switches. And the relative errors between predicted specifications (S'_{test}) and conventionally measured ones (S_{test}) are less than 2%. This gives a solid proof of the accuracy of the proposed method.

3.7.2 Closed-Loop Test for Power Converter

3.7.2.1 Buck Converter

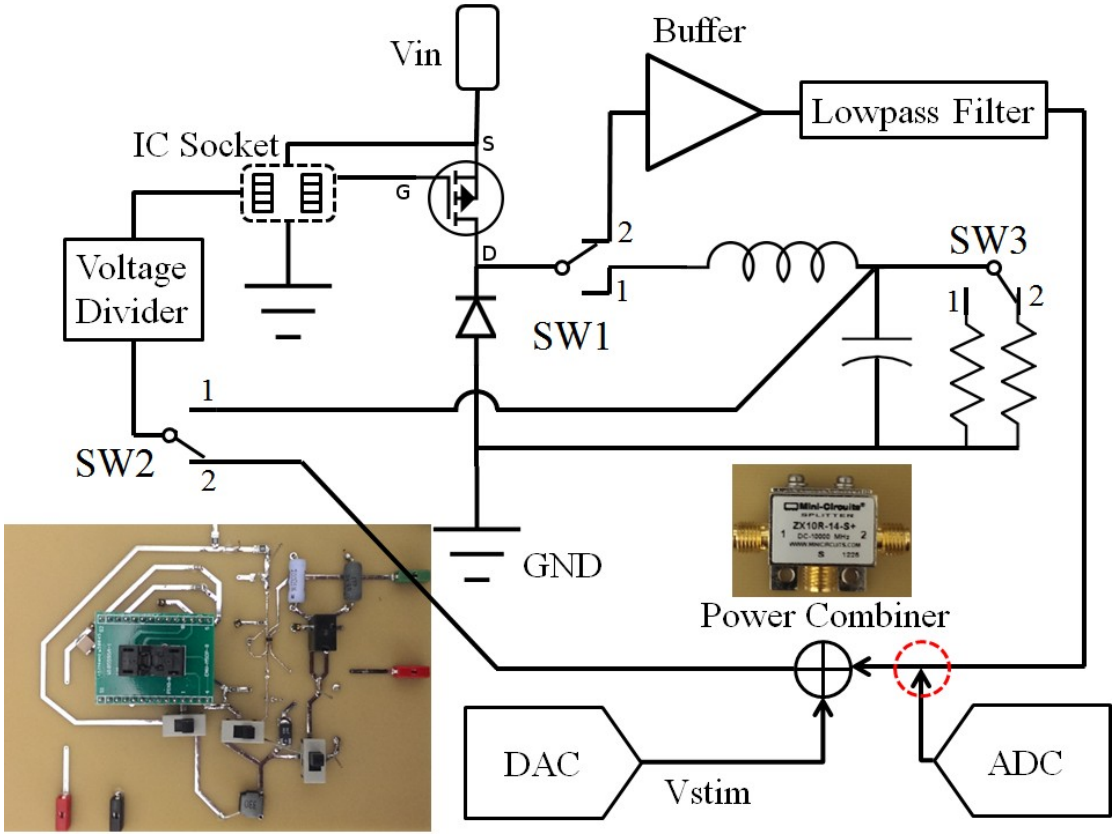
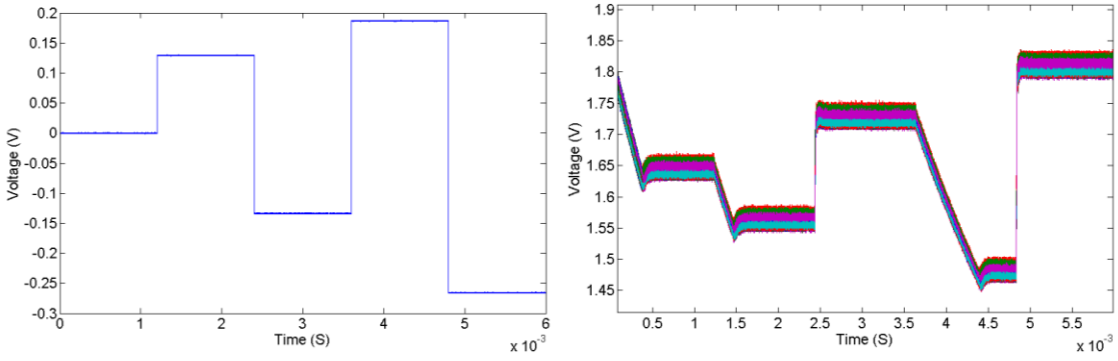


Figure 32: Hardware layout and test configuration for hysteretic buck converter.

As a proof of concept for alternative test of buck converter, a buck controller with external PMOS switch was implemented in both conventional and proposed test configurations on a PCB. The controller with external PMOS allows a close capacitor to be placed across the power switch in order to get rid of voltage spike for conventional measurement.

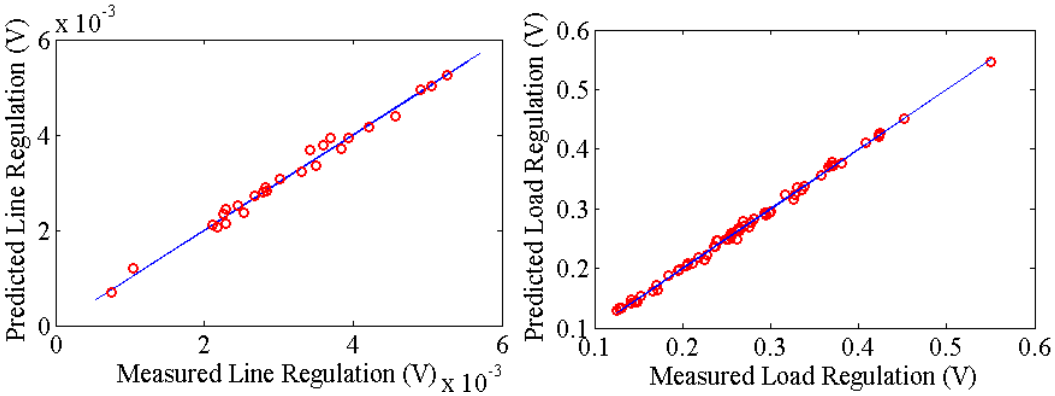
As shown in Figure 32, two switches (*SW1* and *SW2*) were designed to switch between the conventional test and the proposed alternative one. When they were all in position 1, the circuit operated in the conventional test configuration. The load regulation was measured by changing the load through *SW3*, and line regulation was measured through stepping supply voltage between two predefined values. When those switches (*SW1* and *SW2*) are in position 2, the circuit was configured for the proposed alternative test. The stimulus has been added through a power combiner.

The circuit was fabricated and presented with its block diagram in Figure 16. Measurements have been made across 100 test cases. In order to reduce the effects of noise in data acquisition, each measurement was repeated 20 times, and the average value was used. Among these 100 sets of data, 70 are used to train the regression model, and 30 are used to evaluate the prediction. The injected stimulus and captured output responses are presented in Figure 33 below:



(a) Stimulated waveform (b) Output responses

Figure 33: Experiment responses.



(a) (b)

Figure 34: Measured specifications vs. predictions of (a) load regulation and (b) line regulation.

Since the load current has been significantly reduced by the proposed method, the sharp transient in load current was avoided. The predicted load/line regulations are shown in Figure 34. The relative mean square errors between predicted specifications (S'_{test}) and conventionally measured ones (S_{test}) were 3.16% for line regulation and 1.93% for load regulation, with maximum relative errors less than 5%. This gives a solid proof of the accuracy of the proposed method.

The predictions of specifications (excluding ripple voltage, peak voltage, and load/line regulation) that were measured by ATE in the conventional test were also done as a proof of concept of test time reduction. There specifications include pin capacitance, transistor on resistance, etc. To demonstrate the possible correlations between the stimulated response and those ATE measurements, 200 test cases were randomly sampled from 5,000 untuned PWM voltage-controlled buck converters. The specifications of the 200 test cases were measured by ATE and used as training/evaluation targets in this experiment. The test setup for the proposed measurement was the same as the one shown in Figure 32 with PXI 5105 as the ADC, and the layout of the load board was fabricated and presented in Figure 35 below:

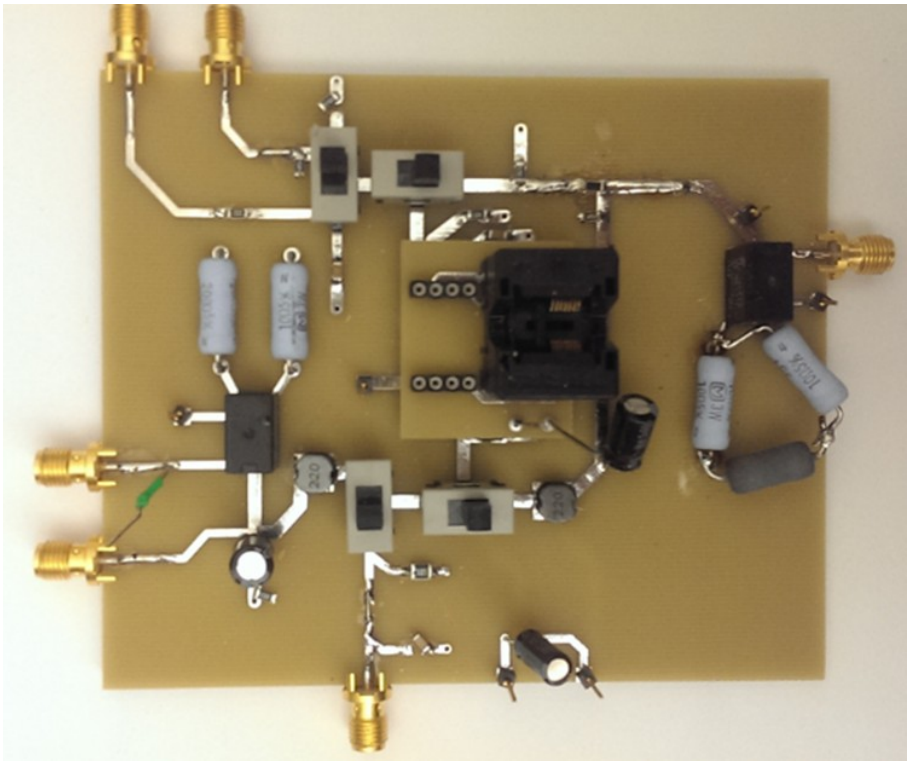
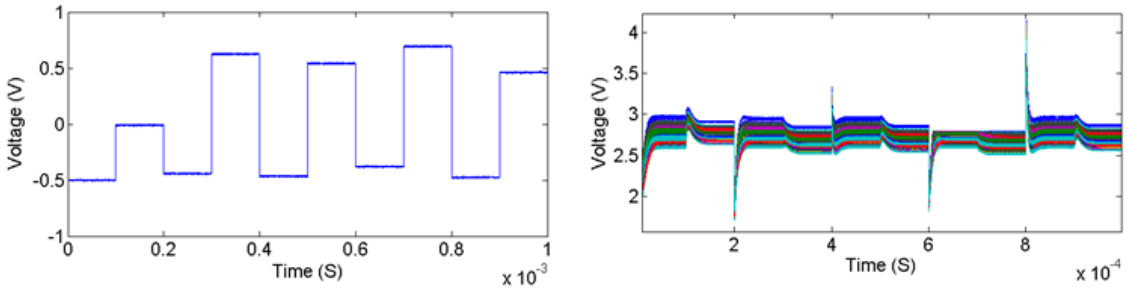


Figure 35: Hardware layout for PWM buck converter testing.



(a) Injected stimulation (b) Stimulated responses

Figure 36: Measured response.

As shown in Figure 36(a), a pre-optimized stimulus was injected into the system, and the output responses in Figure 36(b) were observed and captured. Based on this hardware results, the proposed method was also able to predict feedback voltage under different load conditions, internal reference voltage, and on resistance of up transistor. Predictions of part of those specifications are shown in Figure 37.

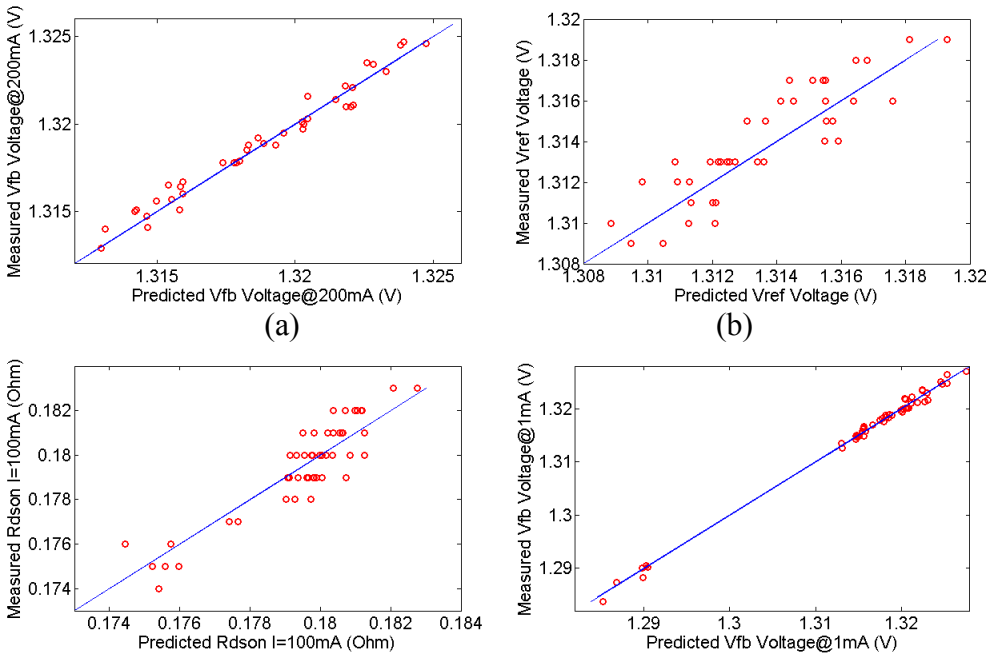


Figure 37: Measured specifications vs predictions.

Note that the inaccuracies of predicting V_{ref} (internal reference voltage) and R_{dson} (on resistance of power transistor) were partially coming from the inaccurately measured training set as the quantization errors of these specifications can be clearly observed in Figure 37(b) and (c).

3.7.2.2 Boost Converter

As proof of concept, a hardware prototype of the proposed alternative test approach for boost converter was fabricated using commercially available components. Instead of building the output network proposed in Figure 24, a simplified test structure was used as a proof of concept. Figure 38 shows the test setup for proof of concept.

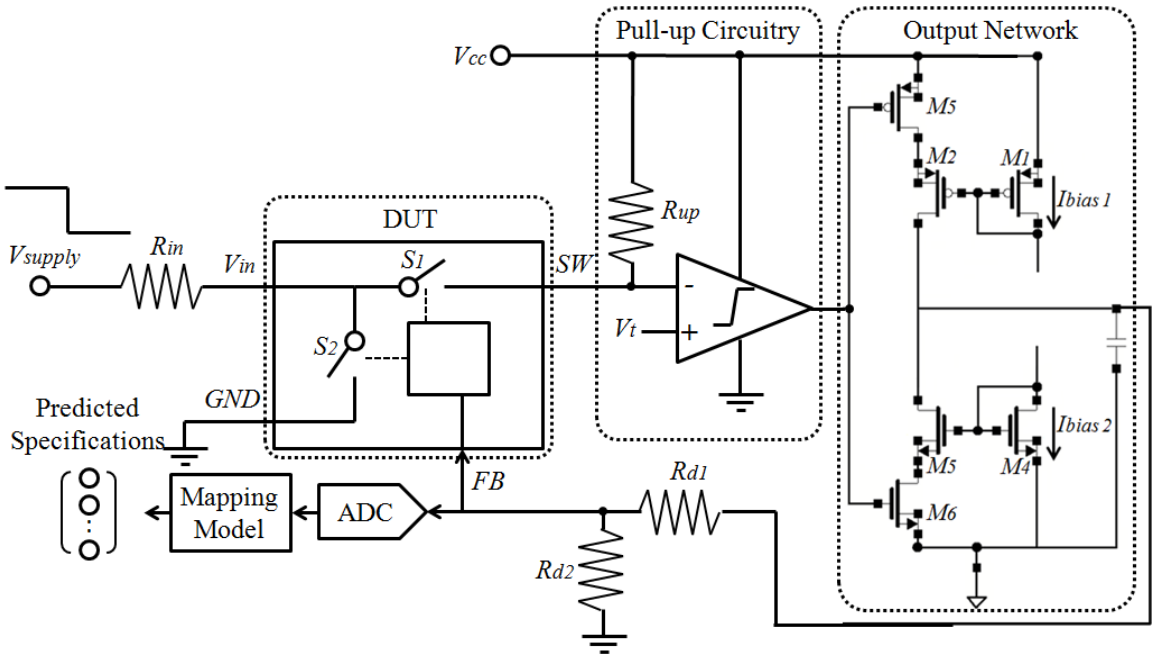
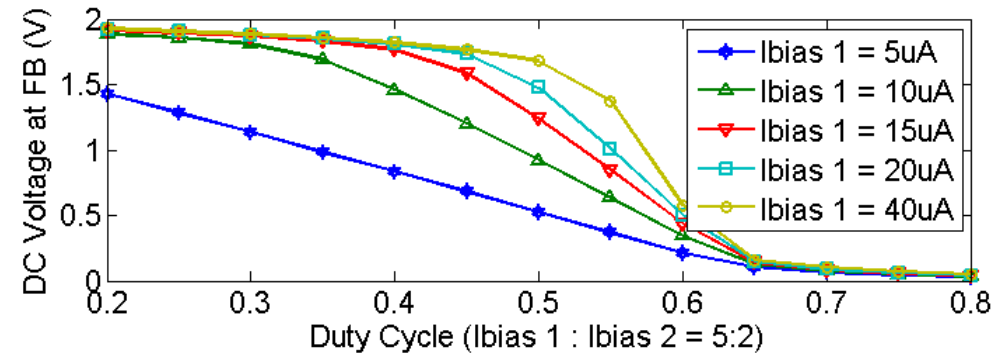
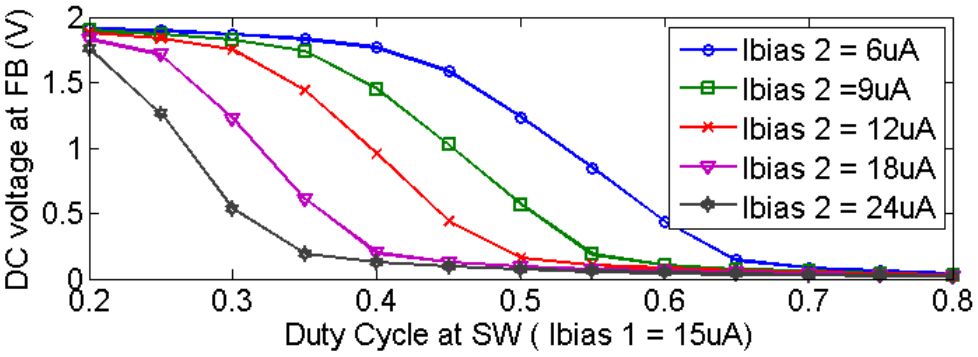


Figure 38: Test setups for proof of concept.

The pull-up resistor and comparator were used in this experiment to maintain a certain DC (above 1.8 V) voltage at *SW* pin so that the duty cycle of the test case was not locked at a single value. The details of this feature of test case were described in its datasheet (TLV61220). Two current sources (Keithley 2400) were connected to the output circuit to provide I_{bais_1} and I_{bias_2}. By changing those two bias currents, the transfer function of the output circuit varies. The relations between the duty cycles of input pulse train (1 MHz, 0 V for "low," 2 V for "high") and output DC voltage under different bias currents were studied and presented in Figure 39 below:



(a) Fixed ratio between I_{bias} 1 and I_{bias} 2



(b) Fixed I_{bias} 1 at 15uA

Figure 39: Relation between stabilized DC voltage and bias current.

As discussed in the previous section, the duty cycle of input pulse train of output network and its output DC voltage was inversely proportional. This was observed in Figure 39. Since the relation between the duty cycle and output network's DC output voltage depends on both biasing current ratio and amount, the bias currents should be optimized in such a way that their perturbations have the maximal correlations with targeted specifications. This was done through a simulation-based test generation process discussed in Section 3.2.

In this experiment, PXI 5105 was used as ADC. The biasing voltages in pull-up circuitry were calculated using the equations below:

$$\frac{V_{CC} - V_{\sup ply}}{R_{in} + R_{up}} R_{in} + V_{\sup ply} = V_{LOW} \quad \text{Equation 43}$$

$$V_{CC} = V_{HIGH} \quad \text{Equation 44}$$

$$V_t = \frac{V_{HIGH} + V_{LOW}}{2} \quad \text{Equation 45}$$

where "on" resistances of two switches were negligible. There were 104 boost converter samples that were used as test cases, where 75% were used to build the statistical mapping model and 25% were used to evaluate the performance of the model. The layout of the load boards for both the conventional test circuit and the proposed alternative test circuit is shown in Figure 40. Note that the pull-up circuitry was added externally and not included in the layout figure.

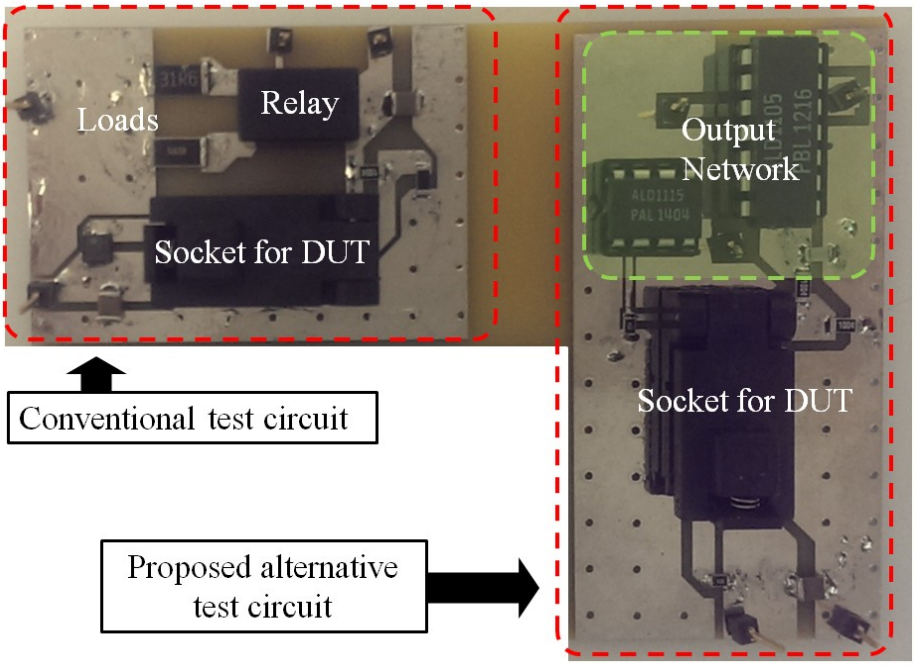


Figure 40: Circuit layout for boost converter safe test.

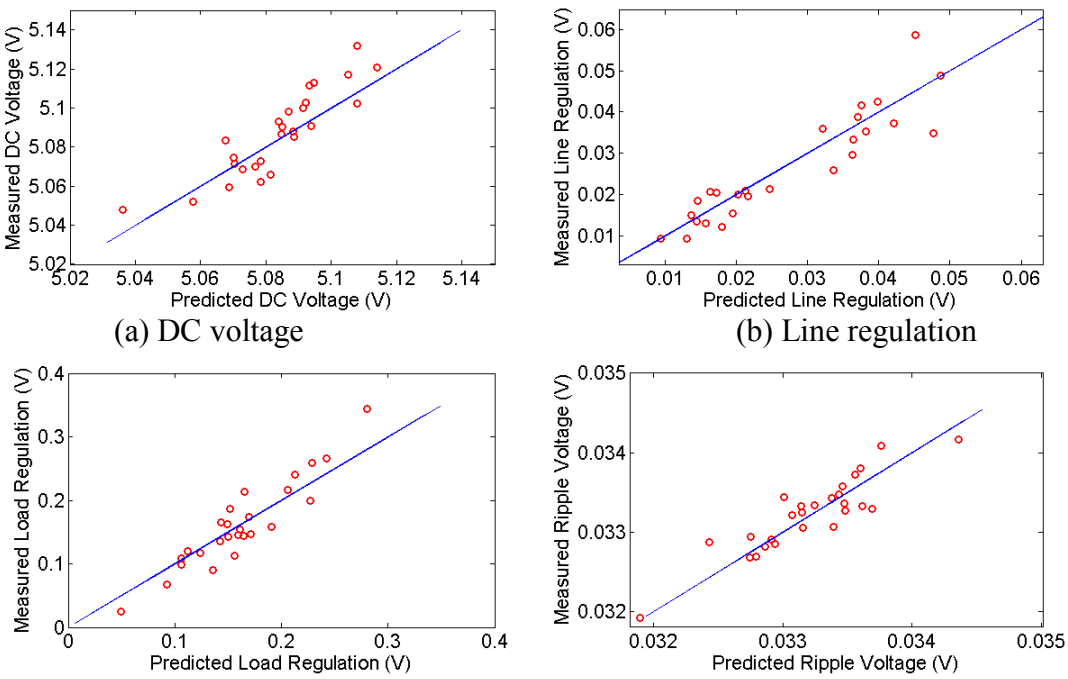


Figure 41: Measurement results for predicted specifications.

To reduce the effects of noise in data acquisition, each measurement was repeated 20 times, and the average value was used. The experimental results are shown in Figure 41. Four specifications were predicted from the stimulated response: DC voltage, load/line regulation, and ripple voltage. Clear correlations were observed in Figure 41, and the inaccuracies were caused mainly by two aspects: one was the loss of amplitude information due to the pull-up circuitry, and the other was the low-frequency noise during data acquisition. However, as a proof of concept, this experiment clearly shows the correlation between the perturbed output voltage and the specifications.

CHAPTER 4: SELF-TUNING FOR POWER CONVERTERS

4.1 Self-Tuning Flow

Though self-tuning of switch-mode power converters have been well discussed from control prospective[69-71] , there are not many self-tuning methods that solve the voltage spike issues for production test and tuning. With the proposed alternative safe test structure, a self-tuning framework is introduced in this chapter to enable safe self-tuning of switch regulators during manufacturing test. As shown in Figure 42 below, after configuring the buck converter into an alternative test mode, the first step is to apply an optimized alternative test stimulus to the buck converter, capture its response, and use that to predict the DUT specifications of interest [29, 30, 34, 72-75] using a regression-based mapping model. As opposed to explicit stimulus, in our approach, the stimulus consists of optimized perturbations of the feedback loop of the buck converter design. The response of the converter to the perturbations is captured using an ADC and used to activate the tuning process. The perturbations are designed in such a way as to maximize the correlation between the buck converter specifications (e.g., load/line regulation) and its response to the applied perturbations. This correlation is used later to build a specification-prediction regression model using hardware "training" experiments [29, 30, 34, 72-75]. A "defect filter" [61] is used next to determine if the DUT is an "outlier device" (i.e., suffers from a catastrophic fault). If so, the device cannot be tuned. If not, then the specification-prediction regression model discussed earlier is used to predict the buck converter specifications from the observed DUT response. Concurrently, using a different tuning-prediction regression model, constructed using a different set of

hardware training experiments, the optimal tuning knob values for the buck converter are predicted directly from the observed test response in one step.

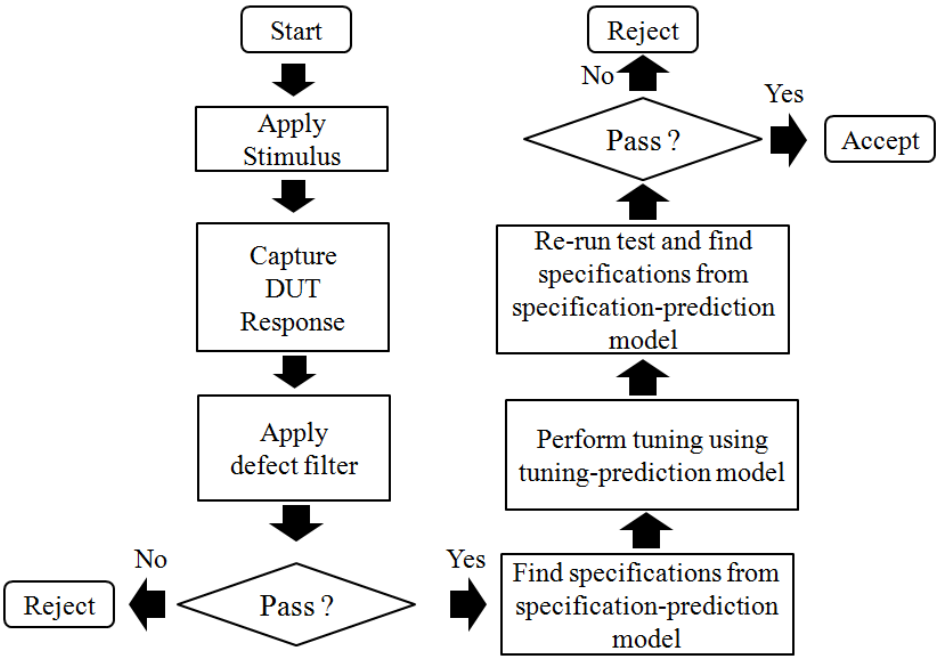


Figure 42: Power converter self-tuning flow.

4.2 Self-tuning Architecture

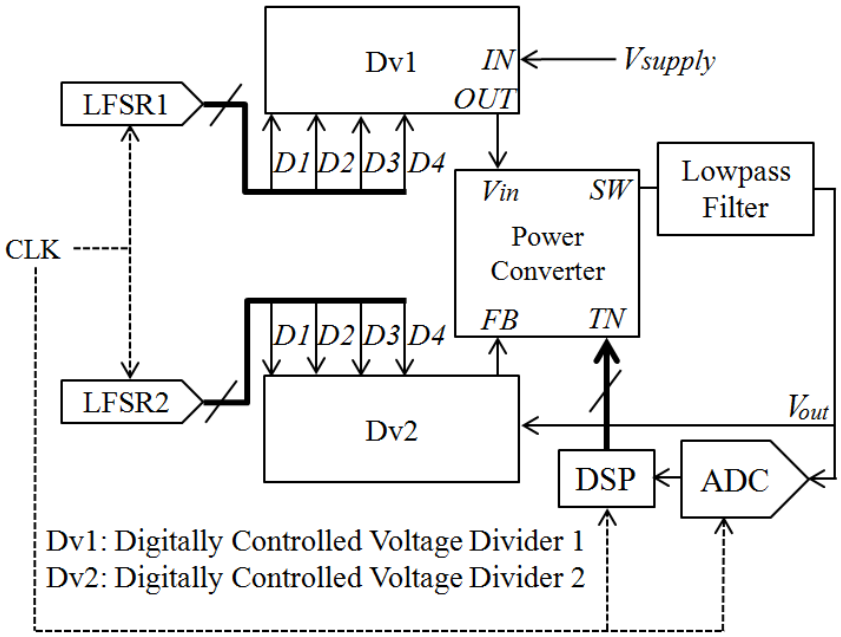


Figure 43: Block diagram of the self-tuning architecture.

Since the entire self-tuning process is based on predicted values of the DUT specifications and tuning knobs, the accuracy of the regression models concerned that map the converter response to either specifications or tuning knob values is extremely critical. To maximize this accuracy, the correlation between the DUT response and its specifications as well as the optimal tuning knob values for a comprehensive set of devices across the manufacturing process space must be maximized. To achieve this, the perturbations of the feedback loop of the converter are selected in such a way that the bandwidth of the converter after each perturbation is within the bandwidth of the original design specifications of the converter.

In addition to the careful selection of loop perturbations, this alternative test methodology introduces two major modifications to reduce voltage spikes caused by parasitic inductances. First, because of the proportional relationship between the load current and voltage spikes at pin V_{in} (according to Equation 8), a high impedance output low-pass filter is used to suppress load current.

Based on sensitivity analysis of the power converter, two nodes are selected for perturbing the feedback loop of the converter. The optimized perturbations are stored as digital patterns and are generated by two LFSRs. By injecting perturbations through voltage dividers that are controlled by these two LFSRs, voltage variations at both pin V_{in} and pin V_{FB} are induced artificially during testing and tuning. The converter response to the applied perturbations is acquired by an ADC and passed to a DSP chip for analysis. The DSP uses the specification-prediction and tuning-prediction regression models discussed earlier to determine the specifications of the device and to determine the optimal values of the converter tuning knobs from the acquired DUT response. In the

following, we will discuss the optimization and injection mechanisms for the loop perturbations. Figure 43 shows the support architecture for the alternative test/tuning methodology. The low-pass filter is designed in such a way that during the steady state, the duty cycle of pulse train at pin *SW* is the same as that during conventional test. This is essential to maximize the correlation between the alternative method and the conventional ones. The details of this low-pass filter are discussed separately for buck/boost converter cases below:

4.2.1 Low-Pass Filter Design for Buck Converter

Compared with the *LC* low-pass filter used in the conventional test condition, the objective of the low-pass filter design for buck converter is about designing a circuit that takes a pulse train as input and generates a DC voltage *proportional* to the duty cycle of that pulse train. Figure 44 shows the structure of this alternative test methodology. In previous work [74], a *RC* network that shares the same 3 dB cutoff frequency as that of the *LC* low-pass filter in normal application was used as the output low-pass filter in Figure 43, but the resulted large capacitor/resistor values are not suitable for on-chip application. This new output low-pass filter structure takes the advantage of a charge pump structure and increases its effective time constant. The values of I_{bias1}, I_{bias2}, and C_{out} should satisfy the relation shown in Equation 46 and Equation 47 to maximize the correlation between the alternative test architecture and the conventional one.

$$\left(\frac{1+\lambda V_{DS}}{\lambda I_{bias1}}\right)C_{out}=\tau \qquad \text{Equation 46}$$

$$\frac{I_{bias1}}{I_{bias2}}=\frac{(1-D)}{D} \qquad \text{Equation 47}$$

where τ represents the time constant of the output low-pass filter during normal application, λ denotes the channel-length modulation parameter, and V_{DS} represents drain-to-source voltage of M_1/M_2. D is the duty cycle of the output pulse train at pin *SW* of buck converter in conventional test. By reducing the bias current, the size of required output capacitor C_{out} is reduced to several *pF*.

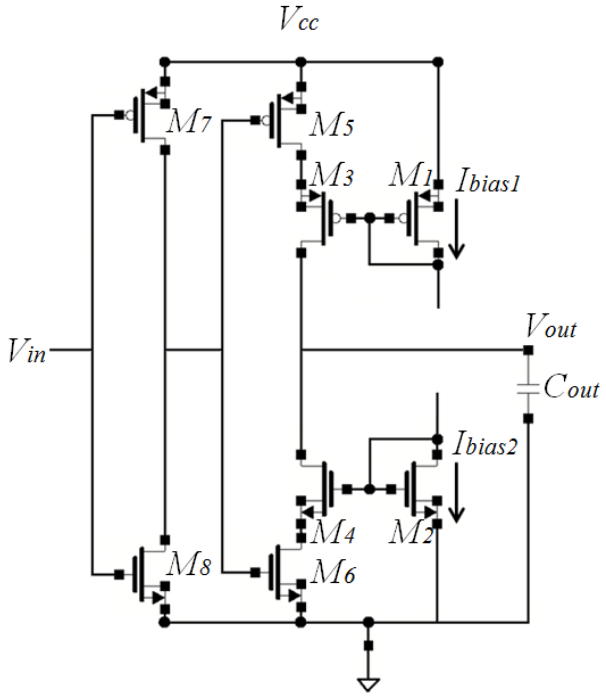


Figure 44: Schematic of output low-pass filter for buck converter.

4.2.2 Low-Pass Filter Design for Boost Converter

In conventional operation, the duty cycle of S_2 in Figure 9 is proportional to the averaged output DC voltage at *SW* pin, and this relationship mode can be expressed as [68]

$$V_{SW} = \frac{V_{in}}{1 - D_{S2}} \qquad \text{Equation 48}$$

where D_{S2} denotes the duty cycle of switch S_2. However, in the proposed architecture, since the input inductor has been replaced by the resistive voltage divider, the averaged output DC voltage at *SW* pin is inversely proportional to the duty cycle of S_2, and it is calculated as

$$V_{SW} = \frac{R_{out} V_{in}}{(R_{in} + R_{out})} D_{S1} \approx \frac{R_{out} V_{in}}{(R_{in} + R_{out})} (1 - D_{S2}) \qquad \text{Equation 49}$$

where D_{S1} is the duty cycle of switch S_1 and can be approximated as (1- D_{S2}). Therefore, the low-pass filter for boost converter in Figure 43 should be designed in such a way that its output DC voltage level is inversely proportional to the duty cycle of pulse train at *SW* pin. The boost converter will only start regulating when this prerequisite is met.

The transistor-level implementation of the low-pass filter for boost converter is proposed in Figure 45. A discharging resistor R_{in} is added to pull voltage at *SW* pin to ground when S_1 in Figure 9 opens and therefore generates a pulse train at pin *SW*. The relations mentioned previously in Equation 46 and Equation 47 should also be satisfied with L as the input inductor L_{in} and C as the output capacitor in Figure 9.

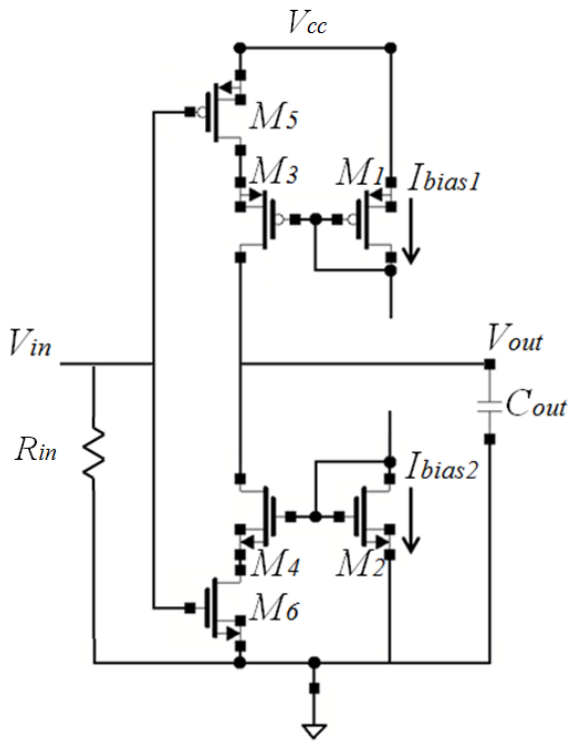


Figure 45: Schematic of output low-pass filter for boost converter.

4.3 Loop Perturbations

The test parameters to be optimized are the resistor values of both voltage dividers of Figure 43, the bit patterns of both 16-bit shift registers, and the period of the clock signal. The following constraints should be satisfied in order to prevent the perturbations from causing device instability and voltage spikes.

$$V_{supply} / R_{Min\_D\_IN} < I_{max} \qquad \text{Equation 50}$$

$$f_{CLK} < f_{3dB} \qquad \text{Equation 51}$$

where $R_{Min\_D\_IN}$ denotes the minimal input resistance of the voltage divider and is discussed in the next section, I_{max} denotes the maximum allowable input current of the buck converter that avoids destructive voltage spikes, f_{CLK} denotes the clock frequency of the self-tuning network in Figure 43, and f_{3dB} denotes the -3 dB cutoff frequency of the

low-pass filter. Note that the logic levels of the LFSRs are always consistent with that of buck converter's internal logic. The optimization of the LFSR structure is performed via genetic optimization similar to that discussed in [29, 30, 34, 72-75] and produces an LFSR that generates perturbations in such a way that the response of the converter to the applied perturbations is maximally correlated with the specifications of the converter under multiparameter statistically representative process variations.

4.4 Injection of Loop Perturbation Stimulus

In the proposed approach, a digitally controlled voltage divider is used to introduce perturbations to the control loop of the power converter by varying its loop gain.

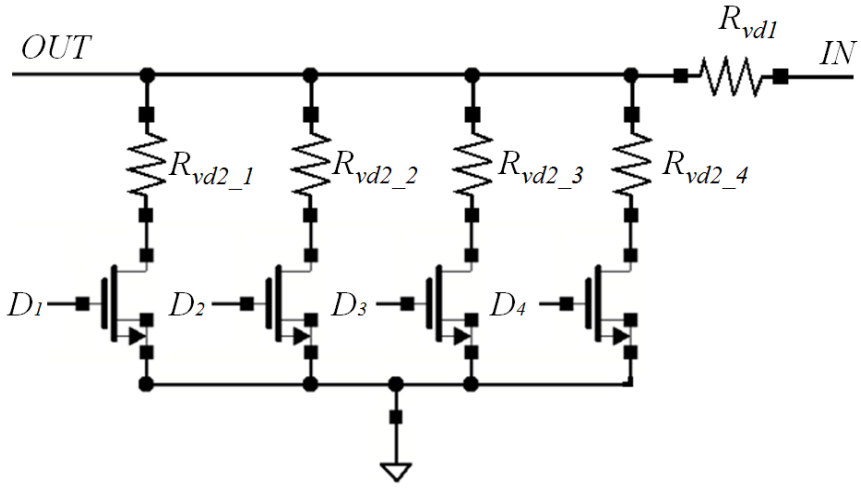


Figure 46: Schematic of digitally controlled voltage divider.

The digitally controlled voltage divider, as shown in Figure 46, has a parallel resistor network that has a transistor connected to each branch. All transistors are properly sized in such a way that a digital "high" in a particular transistor gate allows conduction in that particular branch. The four parallel digital control signals (D_1, D_2, D_3, D_4) are obtained from the output of an LFSR as indicated in Figure 43. Therefore, the minimal input

resistance at node *IN* of this voltage divider is given as R_{vd1}+ R_{vd2_1}|| R_{vd2_2}|| R_{vd2_3}|| R_{vd2_4}. Both voltage dividers of Figure 43 have the same topology as shown in Figure 46.

4.5 Generation of Regression-Based Mapping Models

In the alternative test paradigm [29, 30, 34, 72-75], the test stimulus (loop perturbations in our approach) is designed in such a way that any process variations in the parameter space *P* that affect the specifications of the DUT in the specification space *S* also affect the captured response of the DUT in the response measurement space *M* of the circuit (i.e., that the specifications of the DUT and the alternative test measurements are statistically correlated under prescribed process variations in the space *P*). Under these conditions, there exist multiparameter nonlinear mappings: $f_{ps}: P \to S$ (from the process space to the specification space) and $f_{pm}: P \to M$ [29, 30, 34, 72-75] (from the process space to the alternative measurement space). Consequently, a nonlinear statistical multivariate regression analysis is able to extract a mapping function $f_{ms}: M \to S$ that generates predictions of specifications of the DUT based on a given set of alternative test response measurements. To build the specification-prediction regression mapping function [76], a set of devices is randomly picked across wafers and represents a sample of devices corresponding to the expected (diverse) process variations. This set is henceforth referred to as the "training" set of devices. The DUT specifications are measured for each of the devices (converters) in the training set. Also, the alternative test stimulus is applied to every device in the set. A multivariate nonlinear regression model [76] is built based on the above data that maps the observed DUT response to the measured DUT specifications. This regression model is used to predict the specifications (such as load/line regulation, transient peak voltage, DC voltage, and ripple voltage) of an

arbitrary DUT from its response to the applied alternative test. In practice, a defect filter is used to determine if the response characteristics of the DUT match those of the devices in the training set. If not, the device is subjected to standard testing procedures as well as the developed alternative test measurements. This data is then used to "update" the specification-prediction regression model. If the DUT "passes" the defect filter, then the existing regression model can be used to predict the specifications of the DUT from its observed alternative test response.

To build the tuning-prediction regression model, each of the devices in the training set that does not meet the DUT specification requirements is tuned using a gradient search algorithm (converges in 4–6 iterations). A regression model is then built from the generated data that maps the observed DUT responses to the applied alternative test to the corresponding optimized tuning knob values. The cost function for this optimization is implemented as a weighted sum of the performance metrics of the converter (including performance guard bands) as shown in Equation 52.

$$f(T) = \sum_{i=1}^{5} w_i g(S_i - S_{norm\_i} - Gb_i) + w_6 \frac{|S_6 - S_{norm\_6}|}{Gb_6} \qquad \text{Equation 52}$$

$$g(x) = \begin{cases} 0 & (x \le 0) \\ x & (x > 0) \end{cases} \qquad \text{Equation 53}$$

In Equation 52, S_i $(i \in \{1,2,3,4,5\})$ denotes the load/line regulation values, transient peak voltages during load/line change, and ripple voltage of the respective devices; S_6 denotes the output DC voltage level; Gb_i denotes the guard band value of the i^{th} specification; S_{norm_i} denotes the nominal specification value; W_i denotes the weight assignment for the i^{th} performance metric; and T denotes a vector that contains the values of all the tuning knobs.

The above gradient descent search results in a set of tuning knob values for each tuned device that forces the specifications of such devices (from the training set of devices) that initially do not meet device performance requirements to conform to design requirements at the end of the tuning process. Since the response of each device in the training set to the applied alternative test is known prior to tuning, the tuning-prediction regression model can be built that maps this response to the final values of the tuning knobs of the tuned switching converters.

4.6 Tuning Knob Design and Calibration

Based on a sensitivity analysis, two parts of the power converter are critical to all the targeted specifications: the reference voltage (V_{ref}) and the characteristics of the error amplifier (gain and stability). The reference voltage is normally generated by an internal DAC that already provides tunability and it is used as the first tuning knob (T_0). A tunable operational amplifier (op-amp) is used as the error amplifier to provide control of the gain and stability of the control loop of the buck/boost converter.

The schematic of the tunable operational amplifier is shown in Figure 47. The three transistors (M_5, M_8, M_{10}) provide gain and stability tenability of the op-amp. By controlling bias voltages at the gates of transistors M_5 and M_{10}, the gains of the first and second stages of the op-amp are controlled. Therefore, the gate bias voltages of the transistors M_5 and M_{10} are used as the second and third tuning knobs (T_1 and T_2, respectively) for gain adjustment. The stability of op-amp is controlled by adjusting the gate voltage of M_8, which works in the triode region as a nulling resistor in such a way that its resistance matches the actual transresistance of M_9 under process variations. This matching compensates the op-amp's phase margin, which is affected when the

transresistance of M_9 changes from its nominal value due to process variations. The details of this tunable amplifier are covered in [77] .

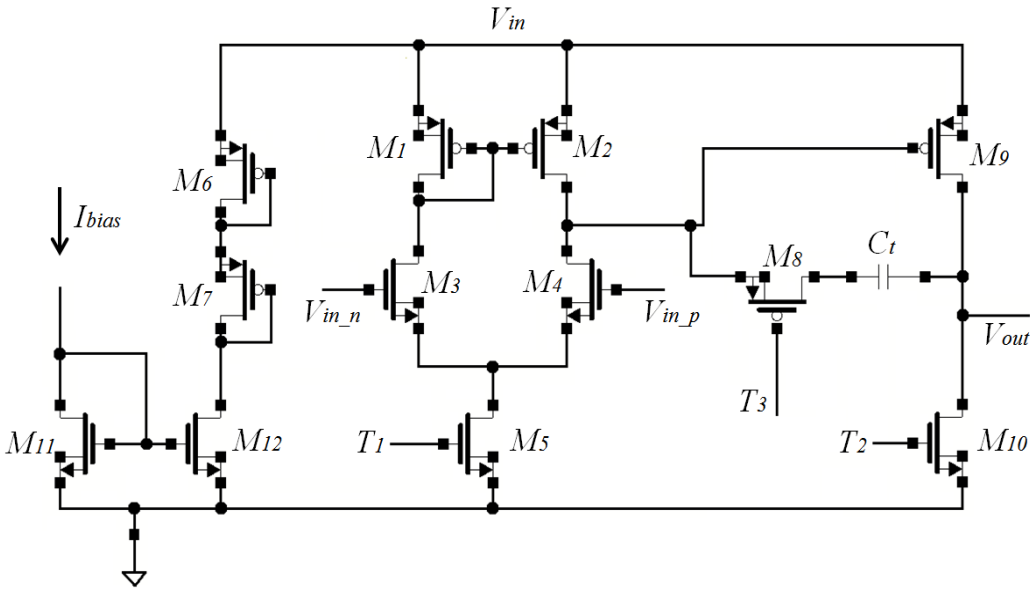


Figure 47: Schematic diagram of tunable op-amp.

As a result, four tuning knobs (T_0, T_1, T_2, T_3) are selected accordingly for tuning V_{ref}, the gain of the amplifier, and the stability of the amplifier.

4.7 Defect Filter

The proposed defect filter uses the joint probability density function estimated by kernel density estimator as a statistical reference. It calculates the estimated data distribution at each observation (each captured data point) and declares DUT as an outlier if all values of its captured output responses have zero probabilities in their estimated distribution functions.

Practically, the density estimator for each data point is defined by

$$\hat{f}_h(x) = \sum_{i=1}^{n} n^{-1} h_i^{-d} K(h_i^{-1}(x - x_i)) \qquad \text{Equation 54}$$

where $K(.)$ is the quartic kernel function,

$$K(u) = \begin{cases} \frac{15}{16}(1-u^2)^2 & |u| \le 1 \\ 0 \quad otherwise \end{cases}$$ Equation 55

x_i, $i=1,...,n$ are d-dimensional alternate measurements (samples) at a specific sampling point of i^{th} device, and h_i are local bandwidths, and their values are selected based on [61, 63] . The density estimator calculates the density distribution of each observation across n devices and classifies a device as outlier when all of that device's observations are lying outside their corresponding estimated density functions ($\hat{f}_h(x) = 0$).

4.8 Simulation Results

In this section, the proposed methodology is demonstrated by the creation of 400 models (instances) of buck converter devices and 400 models of boost converter devices corresponding to different corners of the manufacturing process space. Monte Carlo sampling of the process space is performed to generate the instances above from specified process statistics. Each of the device instances generated were verified for stability, and less than 2% of the devices deemed to be unstable and were eliminated from the sample set.

4.8.1 Selection of ADC

Six specification-prediction regression models were built to map the alternative test response of the DUT (buck/boost converter) to the output DC value, load regulation, line regulation, peak voltage during load transient, peak voltage during line transient, and steady-state ripple voltage of the converter. The stimulated response of each instance was sampled by an ADC and passed to a DSP chip for prediction of the DUT specifications from the regression model. The relation between the ADC's bit resolution and the accuracy of specification prediction (for buck converter) was studied and is plotted in

Figure 48. It should be mentioned that all root-mean-square errors of the predicted specifications in Figure 48 are normalized by their minimal values. Based on the data, a 5-bit ADC was selected as representing an acceptable trade-off between hardware complexity and specification-prediction accuracy.

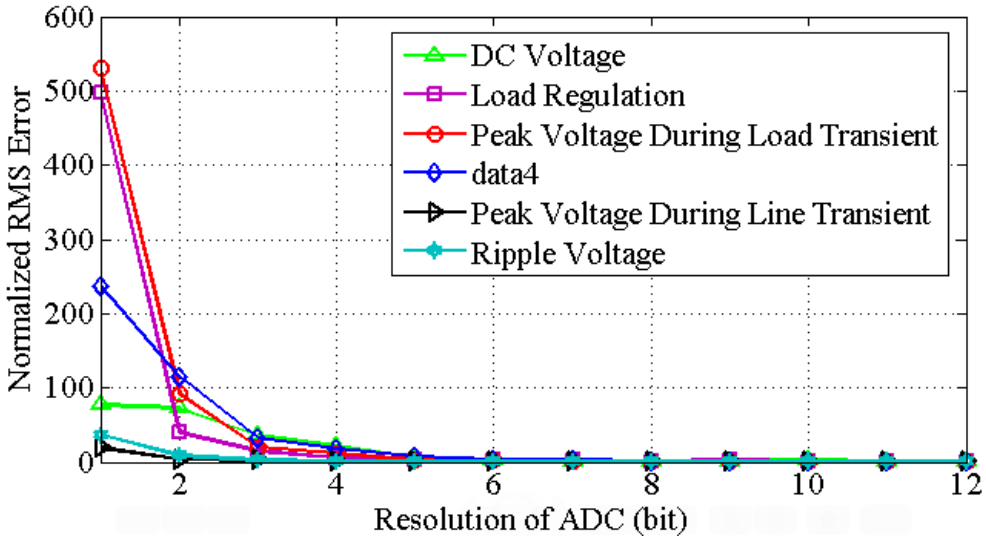
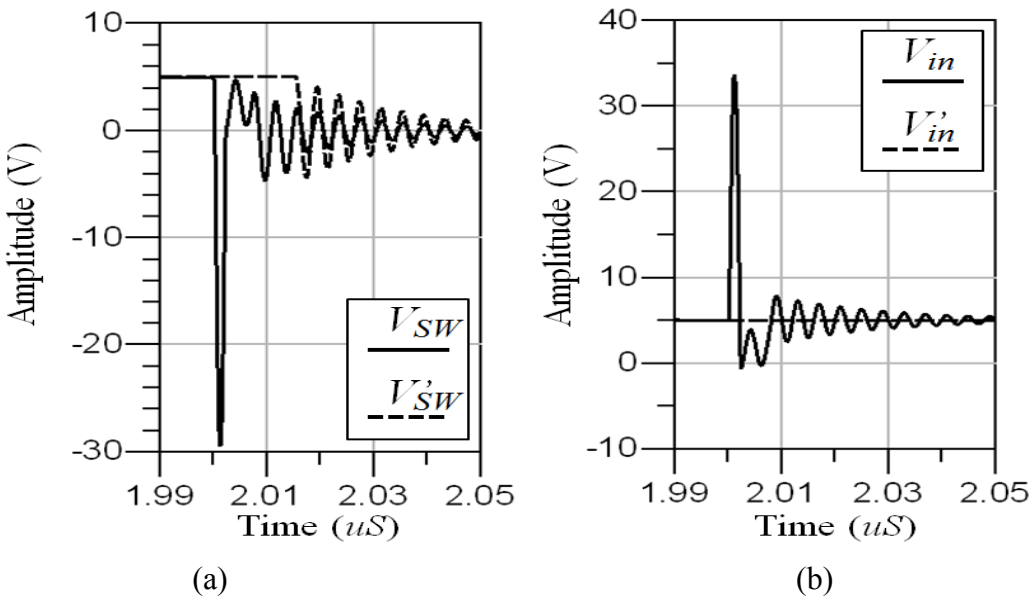


Figure 48: Relation between resolution of ADC and accuracy of prediction.

4.8.2 Prediction of Test Specifications

To prove the ability of the proposed method to reduce voltage spikes, the amplitudes of voltage spikes occurring at pin V_{in} and pin SW during the proposed alternative test and conventional test are compared in Figure 49. V_{in} and V_{SW} denote the voltage at pin V_{in} and pin SW during the conventional test, and V_{in} and V_{SW} denote these voltages during the proposed alternative test.



(a) (b)

Figure 49: Comparison of voltage spikes between the conventional method and the proposed method at (a) SW pin and (b) V_{in} pin.

As shown in Figure 48, the top transistor is turned off at 2 uS, and the bottom transistor is turned on at 2.02 uS after a 20nS delay. This delay is intentionally added to avoid "shoot through." After the top transistor is turned off, since the load current (I_1 in Figure 12) corresponding to the proposed method is very small, the voltage spike it causes is unobservable in Figure 48(b). Since the external inductor is removed, the output current declines to zero instantaneously after the top transistor is turned on. This prevents further voltage drop at pin *SW*. However, after the bottom transistor is turned on, the voltage oscillation between C_2 and Lp_2 (in Figure 12) is inevitable, and the voltage spikes caused are significantly reduced from -29 V to -4.6 V.

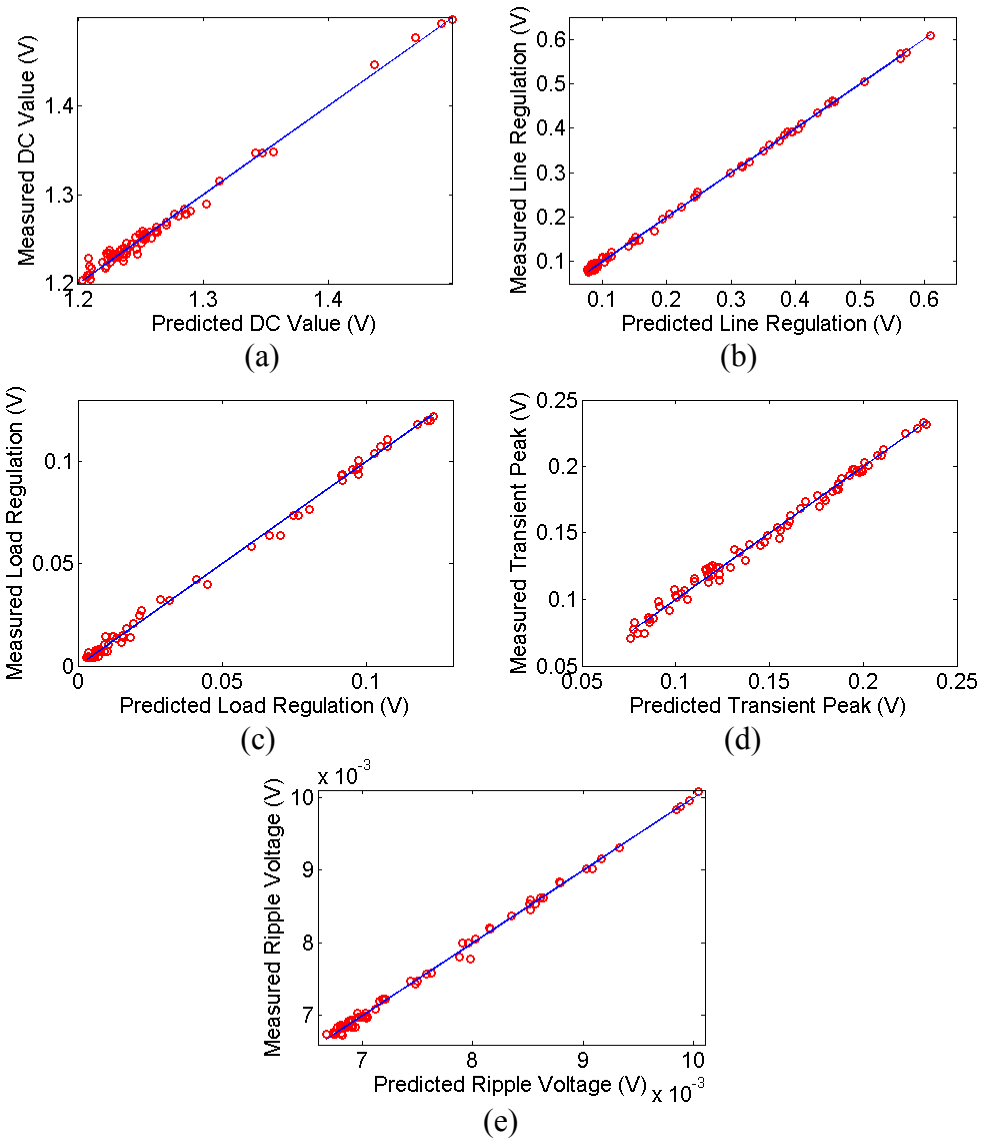


Figure 50: Simulated predictions of targeted specifications of buck converter.

Figure 50 shows the performance of the proposed alternative test methodology using a 5-bit ADC on buck converter, and Figure 51 shows that on boost converter. The predicted specifications are presented along the x-axis, and the corresponding actual values of the specifications are calculated and presented along the y-axis of each graph. Most specifications are accurately predicted with average relative error less than 5%.

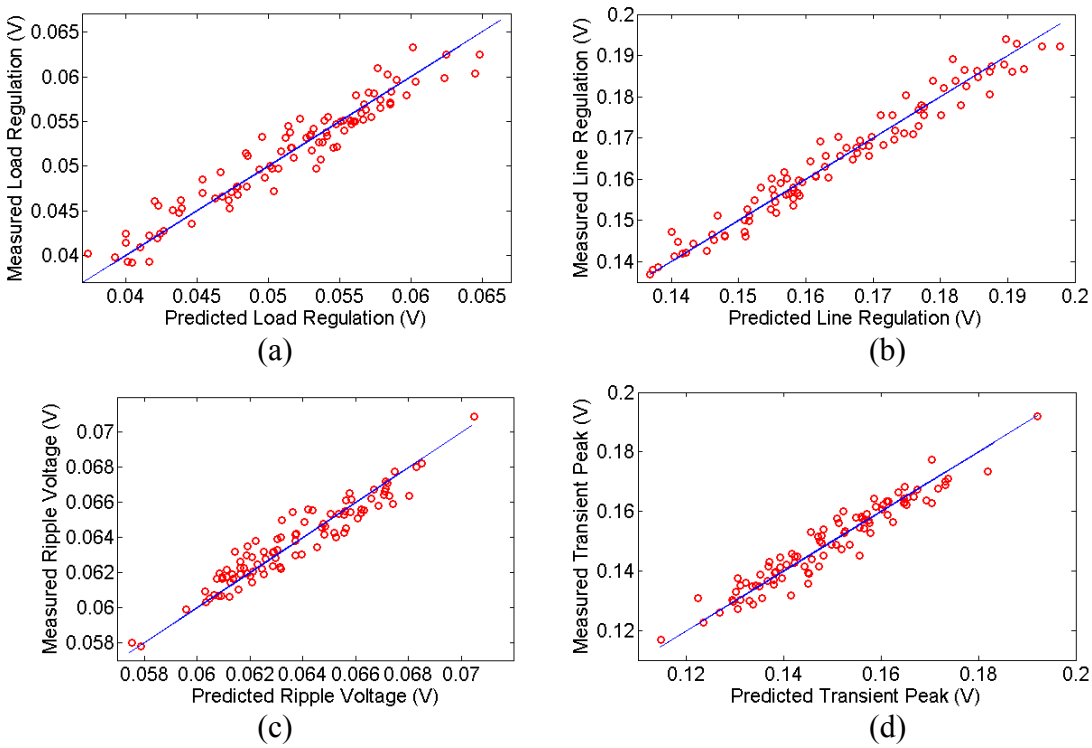


Figure 51: Simulated predictions of targeted specifications of boost converter.

4.8.3 Calibration Based on Tuning Knobs

Since the cost function (Equation 52) takes multiple specifications into consideration, the tuning knobs' values are computed rapidly through the tuning-prediction regression model used to tune all the six specifications of the converter simultaneously. The specification distributions of the DC value, load regulation, line regulation, peak voltage, and ripple voltage for buck converter are given in Figure 52, and the summary of yield improvement is given in Table 1 and Table 2. Please note that the voltages of tuning knobs are set at zero when no tunings are required.

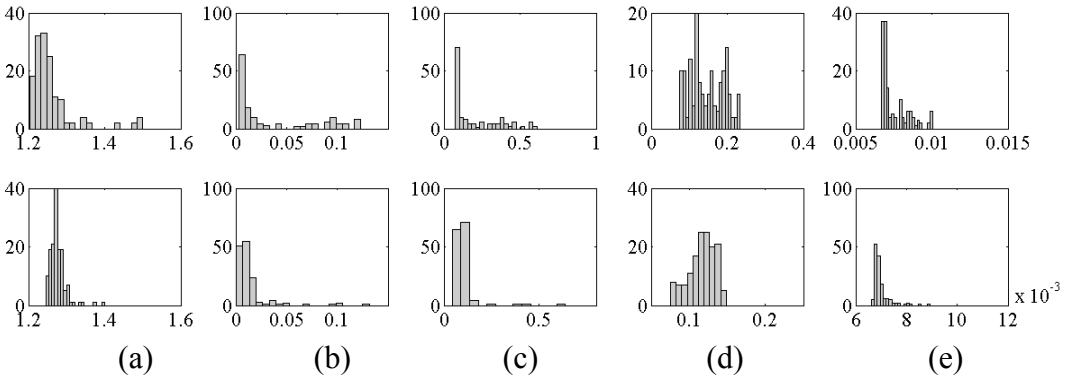


Figure 52: (a) DC value, (b) Load regulation, (c) Line regulation, (d) Peak voltage during transient, and (e) ripple voltage, with (bottom) and without (top) self-tuning.

Table 1: Summary of calibration results on yield (DC characteristics).

	Specifications		
	DC Value	Load Regulation	Line Regulation
Before Tuning	56.85%	67.12%	61.64%
After Tuning	95.9%	92.47%	97.26%

Table 2: Summary of calibration results on yield (transient characteristics).

	Specifications	
	Peak Voltage	Ripple Voltage
Before Tuning	51.37%	75.34%
After Tuning	96.58%	97.26%

The same tuning procedure has been done on boost converter as well. The specification distributions are given in Figure 53, and the yield improvement is summarized in Table 3.

Table 3: Summary of calibration results on yield.

	Specifications			
	DC	Load Reg	Line Reg	Ripple Voltage
Before Tuning	70.85%	93.97%	64.82%	52.76%
After Tuning	98.49%	98.49%	91.96%	99.5%

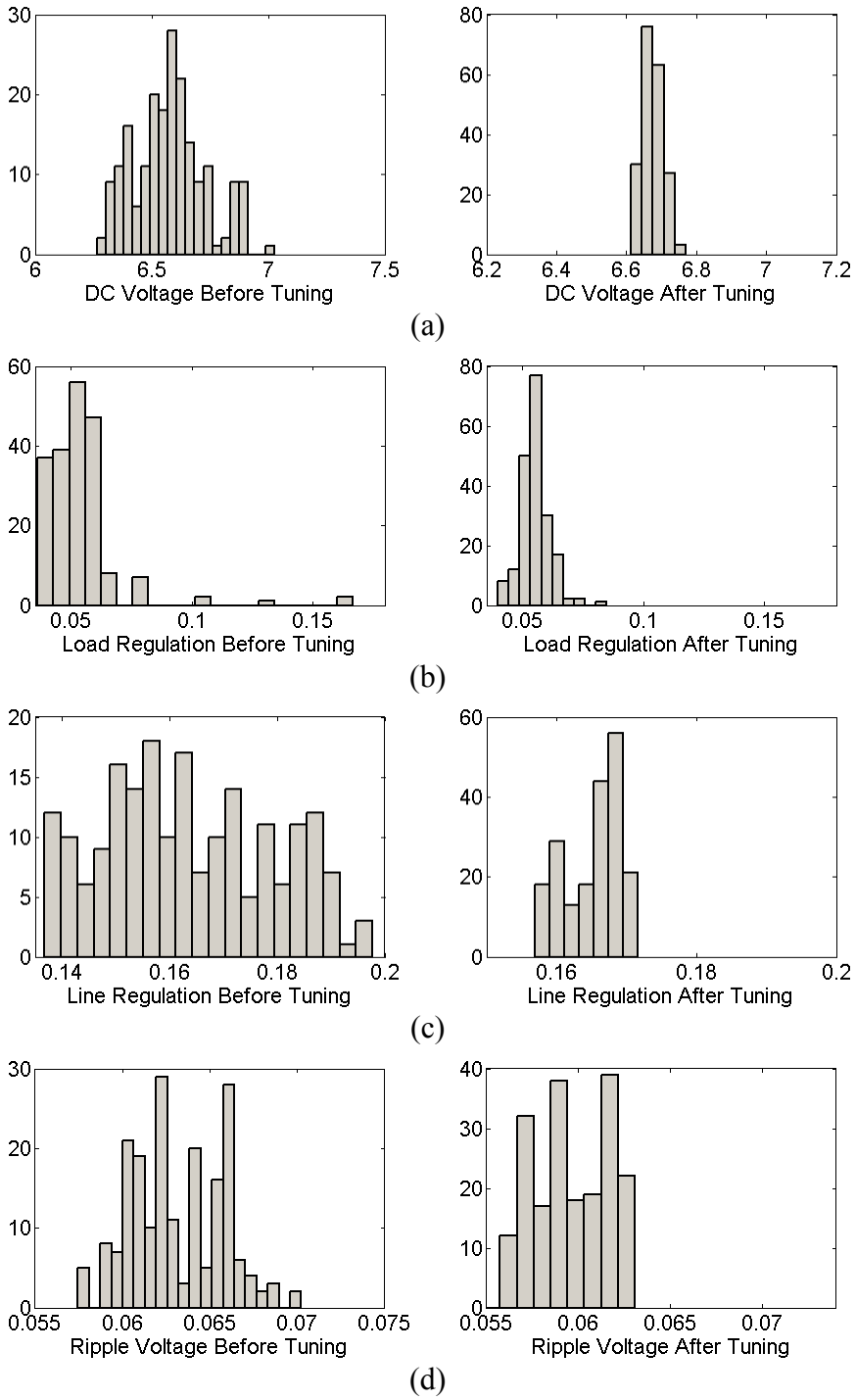


Figure 53: (a) DC value, (b) Load regulation, (c) Line regulation, and (d) Ripple voltage, with (right) and without (left) self-tuning.

4.9 Experimental Results

Figure 54 shows the separated layout of the output low-pass filter structure presented in Figure 45. Its characteristics were verified through the test setup shown in Figure 55. A pulse train with predefined duty cycle was generated and fed to V_{in} of the proposed low-pass filter. The corresponding DC output at V_{out} was then captured by a digital voltage meter. The impact on the relationship between the output voltage and the duty cycle of the input pulse train was plotted in Figure 56 as well.

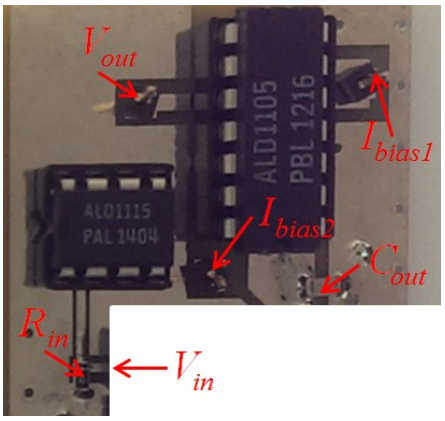


Figure 54: Layout of proposed low-pass filter.

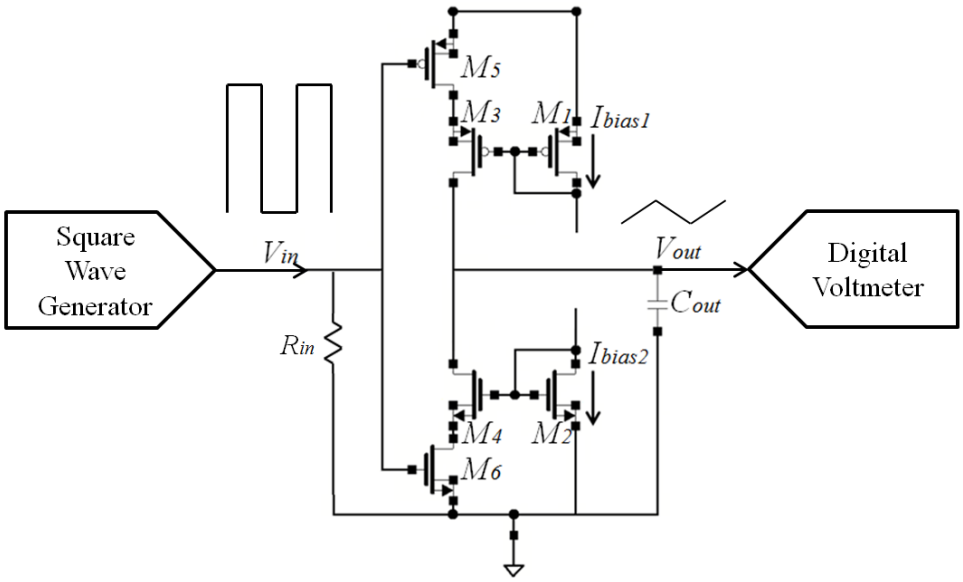


Figure 55: Low-pass filter test setup.

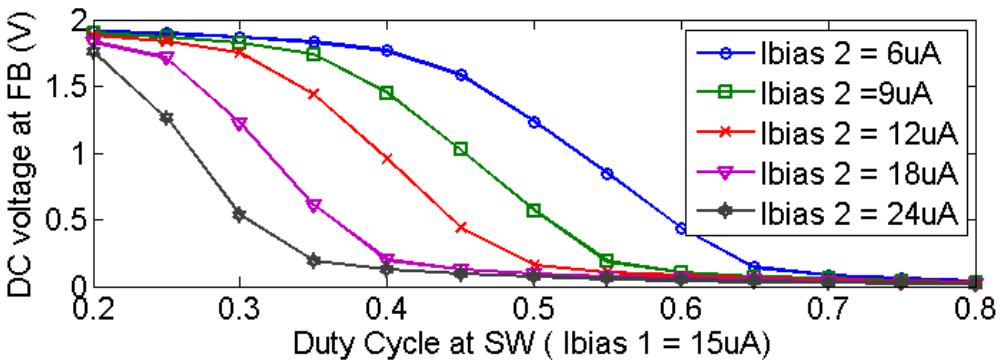


Figure 56: Relation between stabilized DC voltage and the duty cycle of input pulse train under different biasing currents.

Figure 56 demonstrated the impact of the biasing current on the mapping between the duty cycle of input pulse train and the output DC voltage. Therefore, both biasing currents need to be pre-optimized in order to maximize the correlation between the alternative test and the conventional one and hence increase the prediction and tuning accuracy.

As proof of concept, hardware prototypes of the proposed self-tuning architecture for buck converter were fabricated using commercially available components. Figure 57 shows the layout of the tunable converter prototype. The buck converter was implemented based on three primary building blocks. The control block contains a signal buffer, a PWM modulator, and a comparator. The low-pass filter block containing a half H-bridge driver, *LC* low-pass filter, and *RC* low-pass filter was used in this demonstration instead of the proposed output low-pass filter in Figure 44 as a hardware simplification. Relays were used to switch between the conventional test mode and the proposed alternative test mode. The last block is the compensation network built with a variable gain amplifier. Two tuning knobs were designed to adjust the gain of the

amplifier and the level of the buck converter's internal reference voltage (V_{ref}), respectively.

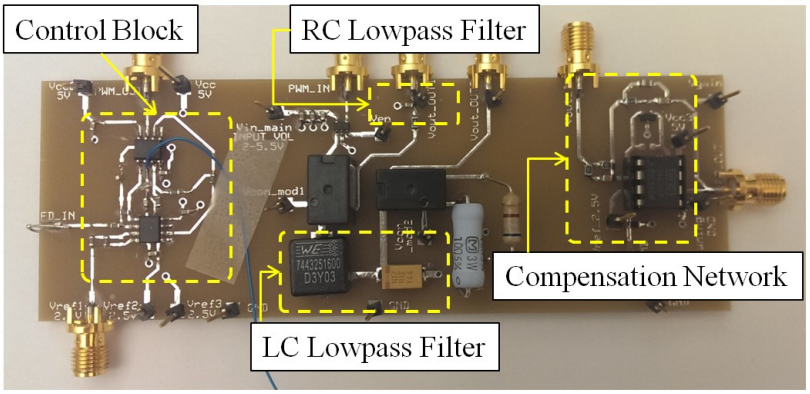


Figure 57: Layout of buck converter with tuning knobs.

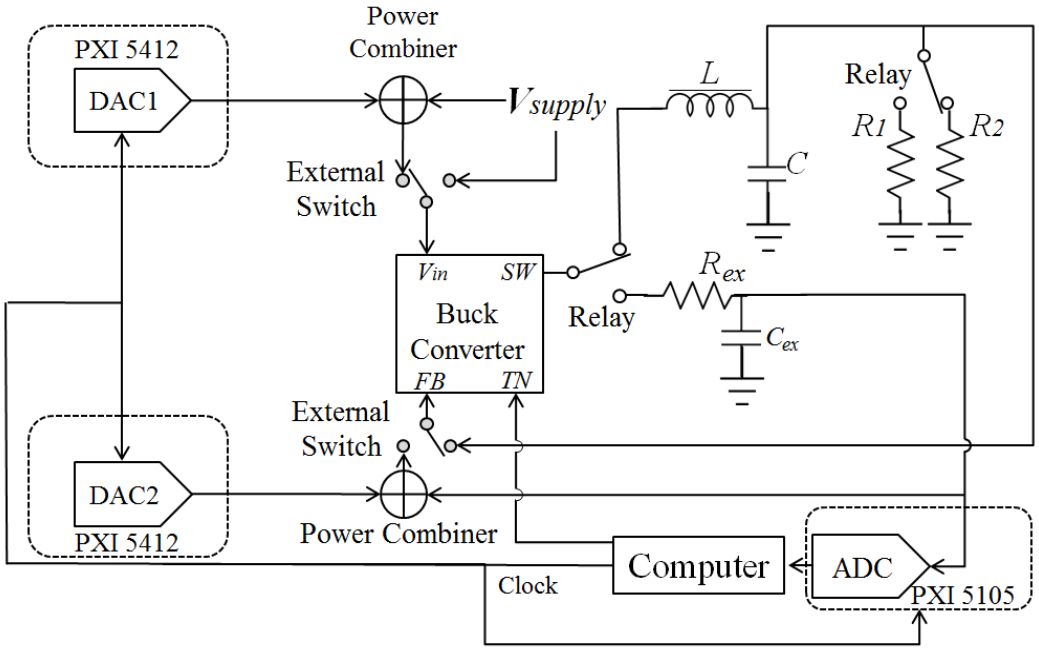
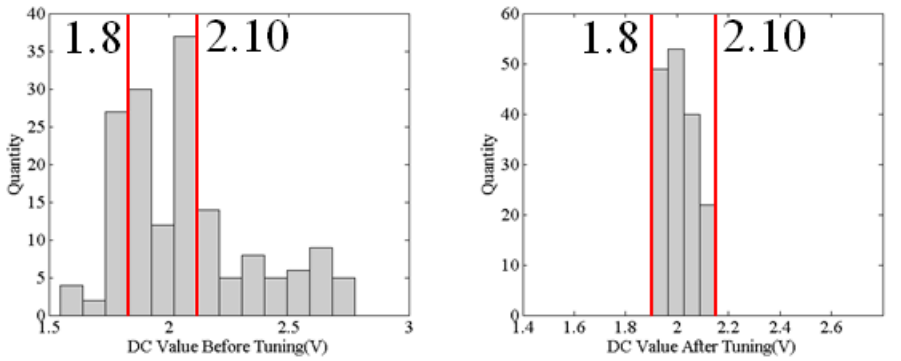


Figure 58: Measurement setup.

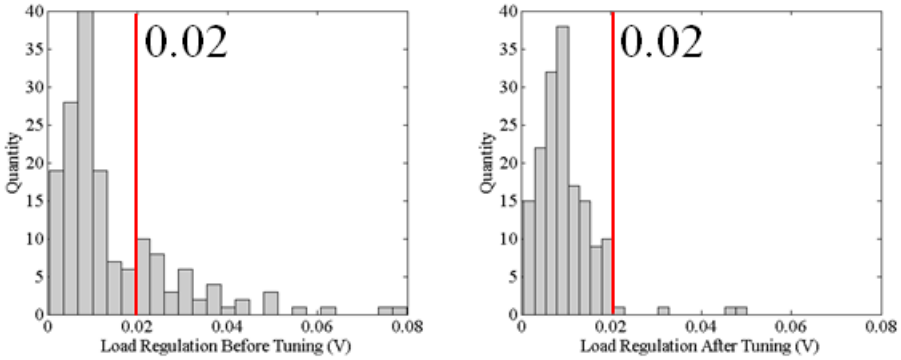
As proof of concept, the tunable buck converter was connected in a slightly different test environment as compared to the configuration in Figure 43. The low-pass filter in Figure 44 has not been used in this experiment because the exact model of this buck converter is not available, and therefore, the optimization on biasing currents was not

feasible. The overall test setup is depicted in Figure 58. Compared to the self-tuning configuration shown in Figure 43, the loop perturbations were emulated via DACs (PXI 5412) and wideband power combiners. The DSP was emulated via an external computer, and PXI 5105 was used as a built-in ADC. In addition, onboard relays and external switches were used to switch between the proposed self-tuning method and the conventional tuning approach based on explicit specification measurement-based tuning.

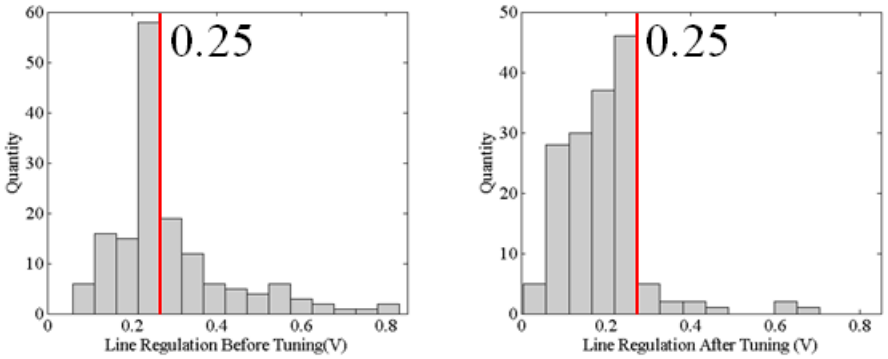
To emulate different DUT performances, the reference voltages of all blocks and some critical resistances were perturbed randomly within ±*20%* of their standard values. This ±*20%* variation was chosen to demonstrate that this method can tune DUT specifications even under large parameter perturbations. With such perturbation of converter parameters, 300 instances with different performance levels were created. Half of them have been used as the "training" set, and the remaining 150 instances were used to validate the proposed tuning approach.



(a) DC Value



(b) Load Regulation



(c) Line Regulation

Figure 59: Specifications before and after self-tuning.

In this hardware prototype, only DC value, load regulation, and line regulation were assigned as tuning targets. Based on the predicted tuning knobs' settings, each instance was properly calibrated, and the specifications after tuning were measured using the standard test setup.

Figure 59 shows the distribution of each specification. In this figure, the red lines depict the guard bands for each specification. The distributions on the left are pre-calibration. The distributions on the right are post-calibration.

A summary of the yield improvement is shown in Table 4 below. Based on these results, the yield of the buck converter has been improved from 34.38% to 89.38% through the use of the proposed self-tuning methodology.

Table 4: Summary of calibration results on yield.

	DC Value	**Load Reg**	**Line Reg**	**Yield**
Before Tuning	46.88%	73.12%	61.88%	34.38%
After Tuning	100%	97.5%	91.87%	89.38%

CHAPTER 5: HIGH-FIDELITY SIGNAL GENERATION

Because of its efficient usage of available frequencies and robustness against multipath fading, orthogonal frequency division multiplexing (OFDM) is used extensively in the field of LAN/MAN communication systems [41, 42]. After 7,500 MHz of bandwidth (3.1 GHz to 10.6 GHz) was opened up for UWB devices by the FCC, much research has focused on reliable UWB communication with the expectation that UWB devices will provide low-cost solutions that can satisfy the increasing demand for high data rates [43]. With wide communication bandwidths available, it is necessary to test modern OFDM communication systems for performance in the presence of interferers with different spectral characteristics [45-48] . This drives the need for generating high-frequency signals with specified spectral content to function as "channel interferers" during communication systems performance testing and requires the use of expensive test instrumentation.

To create channel interferers with specified spectral characteristics (shapes), the conventional approach is to upconvert a baseband signal with the desired spectral characteristics to the frequency range of interest using an upconversion mixer. However, this can cause signal (interferer) distortion due to mixer nonlinearity and is particularly troublesome when the interferer bandwidth is large. To solve this problem, a higher-than-Nyquist-rate RF signal synthesis [78] is implemented. This method takes advantage of a specific type of digital-to-analog converter (DAC) reconstruction filter and generates an optimized input for two interleaved DACs in such a way that higher-order image replicas in the frequency domain conform to the desired spectrum. This image replica is filtered

and used as the primary output of the system, achieving higher-than-Nyquist-rate signal generation.

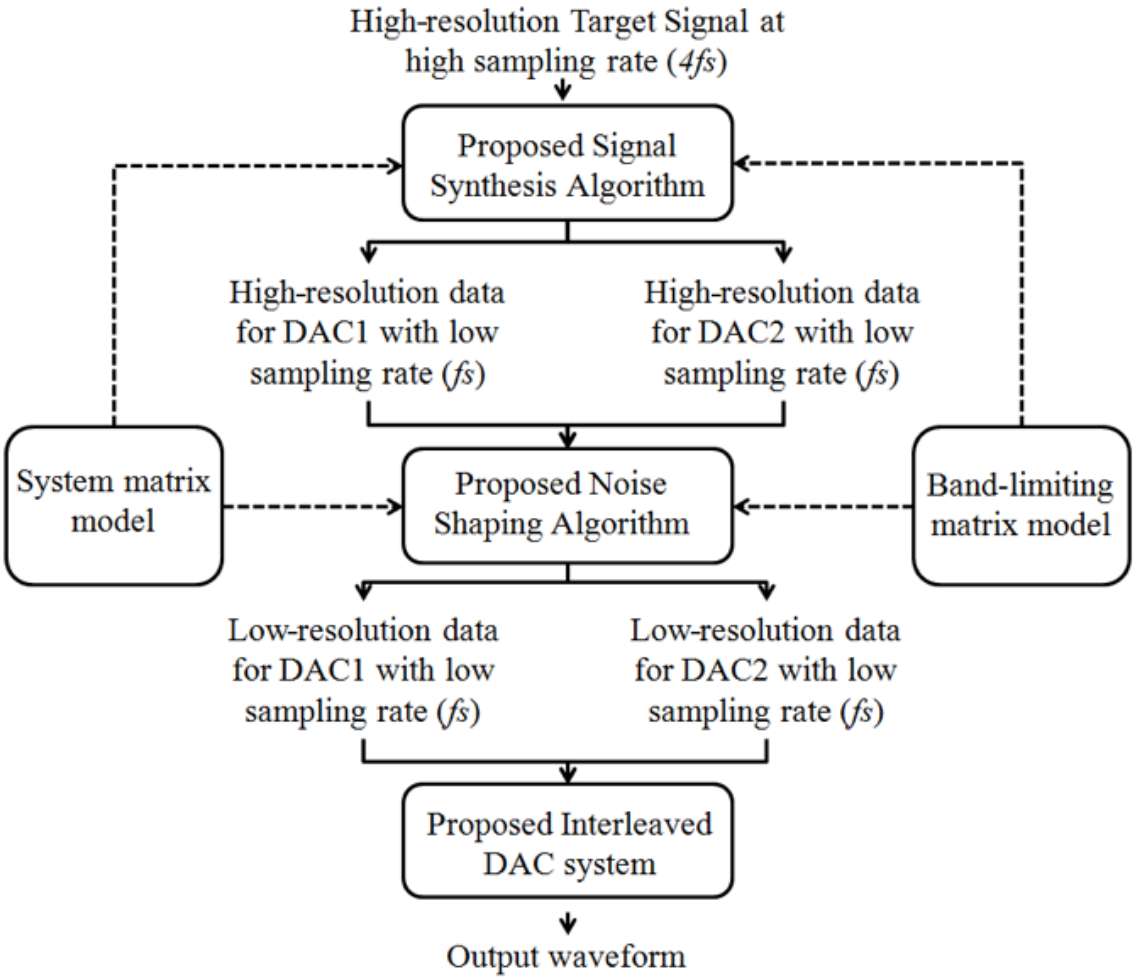


Figure 60: Flow of proposed RF waveform synthesis method.

As shown in Figure 60, this method consists of two distinct algorithms (a signal synthesis algorithm and a noise-shaping algorithm), two matrix models (system matrix model and band-limiting matrix model), and an architecture of an interleaved DAC system with sampling rate at f_s. A signal that consists of high-resolution (32-bit) digital samples with a sampling rate of *4fs* is first defined as the target signal. The proposed signal synthesis algorithm then calculates two sets of high-resolution (32-bit) data for the matrix models in such a way that its output image tone perfectly reconstructs the target

signal within a given bandwidth (defined by band-limiting matrix model). These two sets of 32-bit data are converted into lower resolution (8-bit) by the noise-shaping algorithm with the help of proposed matrix models and optimization algorithm in such a way that the in-band quantization noise is minimized. These optimized two sets of data are then fed to two interleaved 8-bit DACs with proposed architecture to generate the target RF waveform as its image tone.

The key problem is to determine what data to feed into the two interleaved DACs at f_s (called the baseband frequency) so as to produce the desired test signal at the higher frequency obtained by band-pass filtering the first or the second image replica of the data fed to the DACs at the baseband frequency. Further, we desire to introduce noise into the baseband data so that the desired jitter statistics are obtained at the higher frequency corresponding to the synthesized waveform (image replica).

To achieve this, a combined matrix system with two models is introduced. The first matrix model is called "system matrix model." It imitates the data transformation that occurs between the data fed into the two interleaved DACs and the resulting combined waveform. This system matrix model combines two concepts: (a) sampling frequency translation from the baseband data sampled at f_s to the output waveform sampled at $4f_s$, and (b) a model for combining the responses of each of the two interleaved DACs. The other matrix model is referred to as "band-limiting matrix model." It is used to isolate the image replica from the system response. This process is referred to as "in-band noise shaping" in the rest of this discussion. Through the use of a "pseudo inverse" on the whole combined matrix system, the best linear approximation to the target waveform within a limited bandwidth is determined. Note that the image replica carries the same

jitter characteristics of the baseband signal, allowing a high-speed signal (the image replica of the baseband/fundamental signal) with precise jitter characteristics to be obtained. Finally, an external band-pass filter is used to remove out-of-band noise. Note that to enhance the image tones, DAC with a special type of reconstruction filter is required. The details are provided in Section 5.1.

5.1 Fundamentals: Reconstruction Filters

When a discrete-time signal is fed to the data input of a data converter, the discrete-time signal is converted to a continuous-time signal by being convolved with an output reconstruction filter. The impulse response of the reconstruction filter of a zero-order-hold (ZOH) DAC is given by

$$h_{ZOH}(t) = \frac{1}{T_s} rect(\frac{t - T_s/2}{T_s}), \qquad \text{Equation 56}$$

where T_s denotes the sampling time interval and *rect(.)* is the rectangular function [79]. The continuous-time signal reconstructed by using this filter is

$$x_{ZOH}(t) = \sum_{k=0}^{n-1} x[k] \cdot rect(\frac{t - T_s/2 - kT_s}{T_s}), \qquad \text{Equation 57}$$

where *x[16]* denotes the discrete-time samples of the signal being generated and *n* is the number of samples. As the ZOH data conversion is observed in the frequency domain (Equation 58), the reconstructed continuous-time signal contains multiple spectral components even beyond the Nyquist frequency, which are known as spectral image replicas.

$$X_{ZOH}(j\omega) = \frac{1}{T_s}\sum_{n=-\infty}^{+\infty} X_B(j(\omega - \frac{2\pi n}{T_s})) \cdot \frac{2\sin(\omega T_s/2)}{\omega} e^{-j\omega T_s}, \qquad \text{Equation 58}$$

Equation 58 indicates that spectral components appear over multiple frequency locations (image replicas) with a *sinc* frequency response. The frequency domain of a sine wave reconstructed by zero-order-hold reconstruction filter is shown in Figure 61. Note that the image tones in the second and third Nyquist zones suffer from severe attenuations when the zero-order-hold reconstruction filter is used.

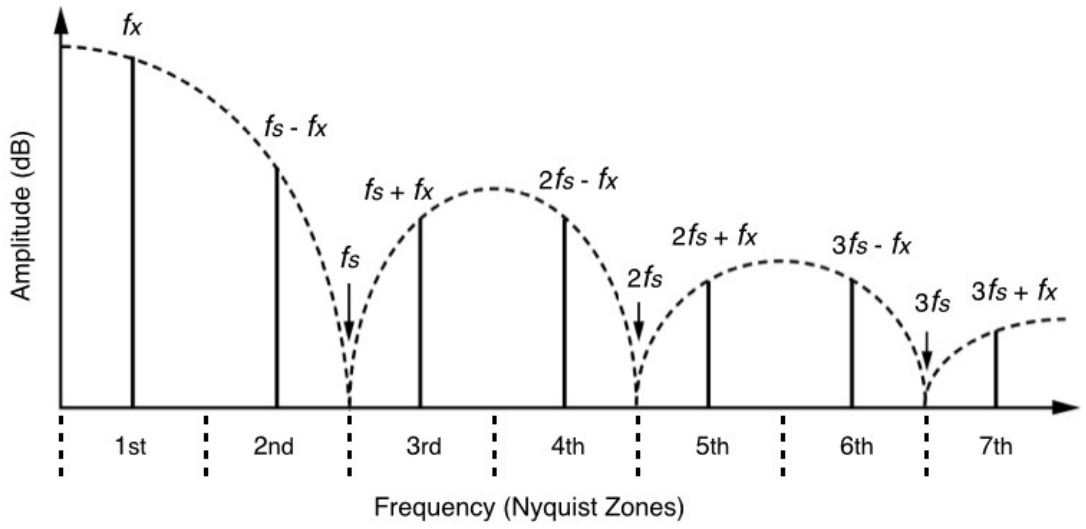


Figure 61: ZOH-mode reconstructed spectra at multiple Nyquist zones; f_x is the synthesized frequency at the first Nyquist zone, and f_s is the sampling frequency.

There exist other types of reconstruction filters that are integrated with commercially available DACs. The frequency domain representations of these reconstruction filters are presented below[57] Return-to-zero (RZ) filter:

$$H(j\omega) = \frac{\sin(\omega T_s/4)}{\omega} e^{-j\omega T_s/4} \qquad \text{Equation 59}$$

Mix filter:

$$H(j\omega) = \frac{\sin(\omega T_s/4)}{\omega} e^{-j\omega T_s/4} + \frac{\sin(\omega T_s/4)}{\omega} e^{-j\omega 3T_s/4} \qquad \text{Equation 60}$$

The spectrum responses corresponding to each of the three different filters can therefore be calculated and are shown in Figure 62.

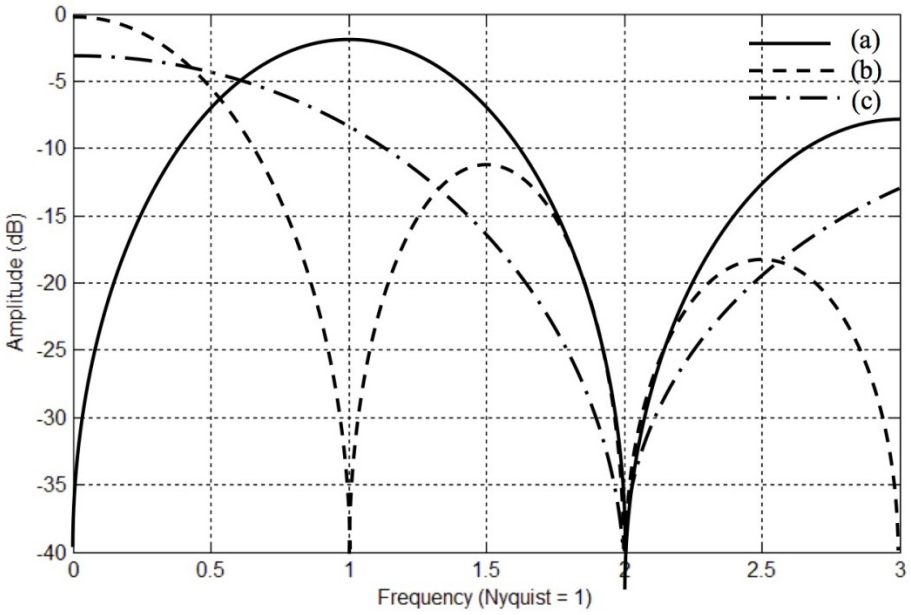
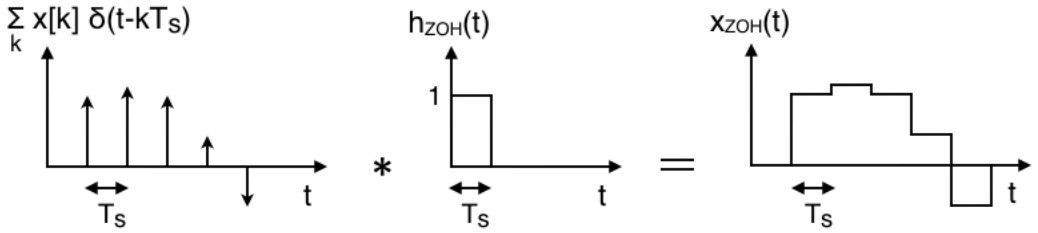
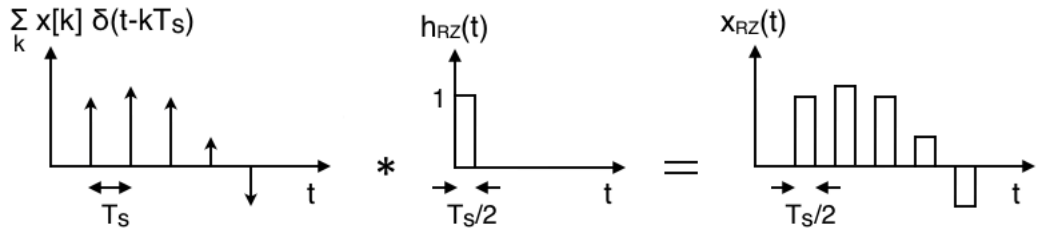


Figure 62: Spectral response of various reconstruction filter of data converter: (a) ZOH filter, (b) RZ filter, and (c) mix filter.

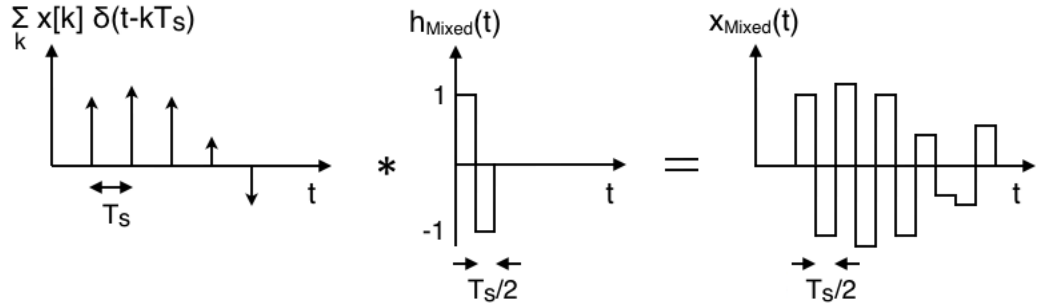
Since the mix filter offers least attenuation on the image replicas in the second and third Nyquist zones, it is selected as the reconstruction filter of DACs used in the proposed method, and a time domain demonstration of signal generation through DAC with different reconstruction filters are also presented in Figure 63 for future reference in Section 5.2.



(a) Zero-order-hold (ZOH) reconstruction filter.



(b) Return-to-zero (RZ) reconstruction filter.



(c) Mix reconstruction filter.

Figure 63: Convolution of a discrete-time signal with various reconstruction filters.

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5.2 Proposed Signal Synthesis

Figure 64 shows an overview of the proposed faster-than-Nyquist signal synthesis technique using dual data converters with mix reconstruction filter. This selection reduces attenuations on the second and third image tones caused by other reconstruction filters. A high-precision discrete reference signal is digitally computed and generated using a direct digital synthesis (DDS) algorithm that uses 32-bit resolution, which is much higher than the bit resolution of the DAC hardware being used. This discrete reference signal consists of digital samples at a sampling rate of $4f_s$, where f_s is the DAC sampling speed. The reference signal is then fed to the proposed waveform synthesis algorithms (signal synthesis and noise shaping) to determine the individual, optimal input sequences of the multiple time-interleaved DACs (two DACs used in this research). The given input sequences are converted to analog signals by the DACs in time-interleaved modes (90-

degree phase offset) with a mix reconstruction filter, and the generated analog signals are combined (added) using a RF power combiner. The transient waveforms at the power combiner inputs and output are illustrated in Figure 65 as well. The combined signal is then fed through a band-pass filter if necessary to select a particular band under interest (higher-than-the-Nyquist frequency).

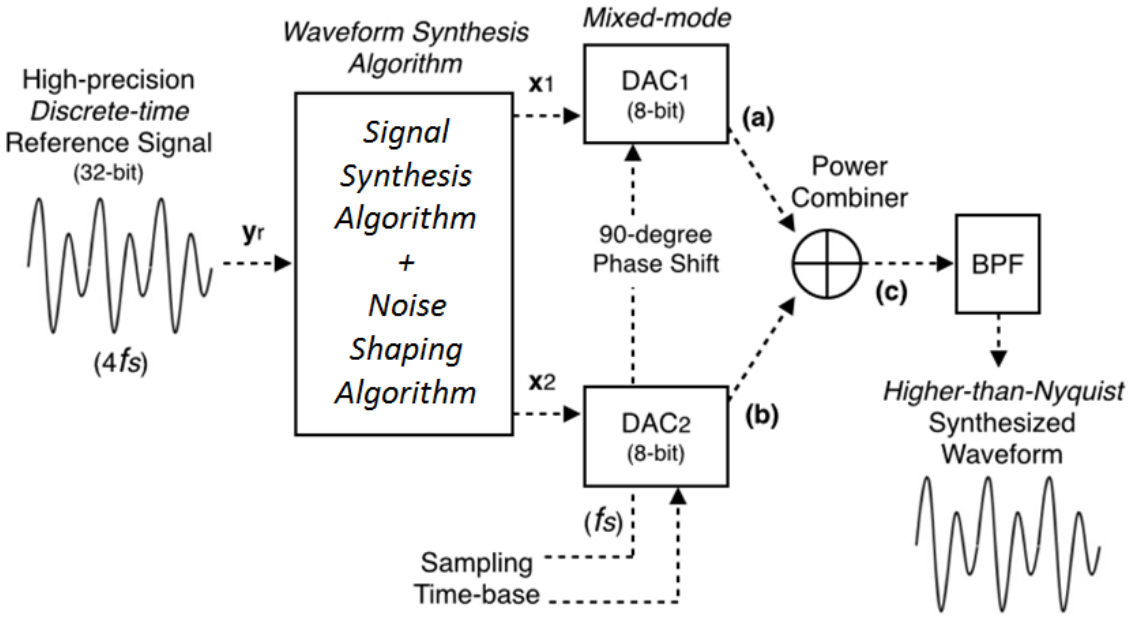


Figure 64: Block diagram of the proposed faster-than-Nyquist waveform synthesis architecture using dual mixed-mode direct digital-to-RF data converters.

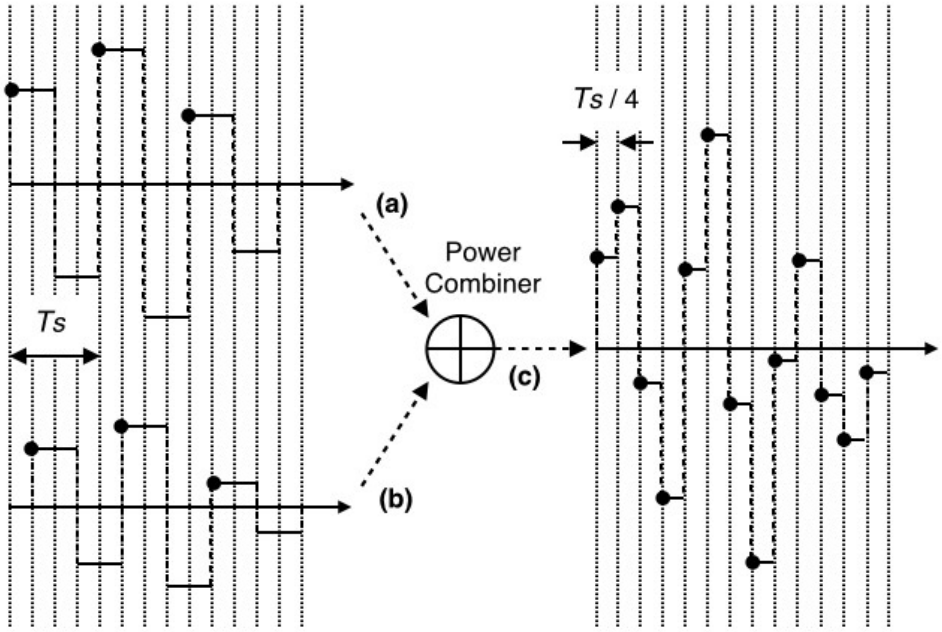


Figure 65: Illustration of time-interleaved sampling and waveforms at (a), (b), and (c) shown in Figure 64.

As shown earlier in Figure 61, since the whole waveform synthesis algorithm is based on the combined system matrix (system matrix model and band-limiting matrix model), the constructions of these models are discussed in detail in Section 5.2.1, while the algorithms are covered in Section 5.2.2.

5.2.1 Matrix Models

As mentioned in the previous section, the matrix models consist of two parts. The first part is the system matrix model, which models the signal generation process that occurs between the data fed into the two interleaved DACs and the resulting combined waveform. The other part is the band-limiting matrix model, which defines the bandwidth that proposed algorithms are focusing on.

5.2.1.1 System Matrix Model

The system matrix model is a matrix that maps the digital input data sampled at f_s to the output waveform sampled at $4f_s$. Since the mix reconstruction filter is used for the dual

time-interleaved data converters, the input data sequences for the 14-bit DAC1 and DAC2 are respectively given by $\boldsymbol{x}^{T}_{1(14\text{-}bit)}=[x_1[1]\ x_1[2]\ x_1[3]\ \ldots\ x_1[n]]$ and $\boldsymbol{x}^{T}_{2(14\text{-}bit)}=[x_2[1]\ x_2[2]\ x_2[3]\ \ldots\ x_2[n]]$. The mix reconstruction filter matrix of DAC1 is given by Equation 61. Notice that 1 and -1 in the reconstruction filter matrix respectively represent the normal and inverse sampling in the mix filter (refer to Figure 63[c]). The mix reconstruction filter matrix of DAC2, which sampling phase is 90-degree offset from the samples of DAC1, is given by Equation 62. Note that the sampling space of each row of the matrix is $4f_s$ and that of each column is f_s.

$$H_{1(4n\times n)} = \begin{bmatrix} 1 & 0 & \dots & 0 \\ 1 & 0 & \dots & 0 \\ -1 & 0 & \dots & 0 \\ -1 & 0 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & -1 & \dots & 0 \\ 0 & -1 & \dots & 0 \\ \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & -1 \\ 0 & 0 & \dots & -1 \end{bmatrix}$$

Equation 61

$$H_{2(4n\times n)} = \begin{bmatrix} 0 & 0 & \dots & -1 \\ 1 & 0 & \dots & 0 \\ 1 & 0 & \dots & 0 \\ -1 & 0 & \dots & 0 \\ -1 & 0 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & -1 & \dots & 0 \\ 0 & -1 & \dots & 0 \\ \vdots & \vdots & \dots & \vdots \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & -1 \end{bmatrix}$$

Equation 62

Using these two reconstruction filters, we construct the system matrix model (Equation 63) to compute the output waveform $y_{0(32\text{-bit})}$ based on input data sets $x_{1(32\text{-bit})}$ and $x_{2(32\text{-bit})}$ with the reconstruction filters. In this linear system, x_1 and x_2 are input data sets to this system, and 32-bit resolution is used for these vectors so as not to lose numerical accuracy. However, the bit resolution of the vectors is supposed to be reduced later to fit the number of bits of the data converter input, which is 14-bit in this particular example.

$$y_{0(4n\times 1,32-bit)} = H_{1(4n\times n)} \cdot x_{1(n\times 1,32-bit)} + H_{2(4n\times n)} \cdot x_{2(n\times 1,32-bit)} \quad \text{Equation 63}$$

Equation 63 can be expressed with its simplified form as shown below:

$$y_{0(4n\times 1,32-bit)} = [H_1 \quad H_2]_{(4n\times 2n)} \cdot \begin{bmatrix} x_{1(n\times 1,32-bit)} \\ x_{2(n\times 1,32-bit)} \end{bmatrix}_{(2n\times 1)} = H_{c(4n\times 2n)} \cdot x_{c(2n\times 1,32-bit)}, \quad \text{Equation 64}$$

where H_c is the combined matrix of H_1 and H_2, and $\boldsymbol{x_c}$ is the combined matrix of $\boldsymbol{x_1}$ and $\boldsymbol{x_2}$. Notice that H_c is not square, and its rank is not equal to $2n$. For this reason, the inverse of the matrix does not exist, and the correct input value x_c cannot be directly calculated by replacing y_0 with target waveform and then performing a matrix inversion on H_c[80, 81]

5.2.1.2 Band-Limiting Matrix Model

The band-limiting matrix model is a matrix that removes unwanted frequency components in a digital sample set at $4f_s$. Because of the existence of unwanted image tones that are inherently present in the synthesized waveform, it is not feasible for the

synthesized waveform to have frequency spectra that are well-fitted to the reference waveform in wideband without confining the basic sampling and signal reconstruction theory. For this reason, we apply a filtering matrix to the existing system matrix model to define the frequency range under interest (or in-band frequency range). This limitation is very critical for proposed algorithms to operate efficiently.

Assuming that the waveform that needs unwanted frequency components removed is $y^T_{in(32\text{-}bit)} = [y_{in}[1]\ y_{in}[2]\ y_{in}[3]\ \ldots\ y_{in}[4n]]$ (n is an integer and power of 2). This band-limiting matrix model consists of three parts and is presented in Equation 65

$$H_{filter(4n\times 4n)} = W^{-1}{}_{(4n\times 4n)} F_{(4n\times 4n)} W_{(4n\times 4n)} \qquad \text{Equation 65}$$

where W is the discrete Fourier transform (DFT) matrix, which converts the discrete-time domain signal $y^T_{in(32\text{-}bit)}$ in the time domain to the frequency domain, and W^{-1} is the inverse DFT matrix, which translates a frequency-domain signal back to the time domain. F is a diagonal matrix that defines the frequency bands of interest to attenuate any unwanted signals that are present outside the band. If the band of interest is defined as [f_1, f_2] where f_2 is larger than f_1, F is given as

$$F_{i,j} = \begin{cases} 1 & if \quad \dfrac{f_1}{f_s} n < i < \dfrac{f_2}{f_s} \quad and \quad i = j \\ 0 & otherwise \end{cases} \qquad \text{Equation 66}$$

Therefore, by performing Equation (12) below

$$y_{out(4n\times 1)} = H_{filter} y_{in(4n\times 1)} \qquad \text{Equation 67}$$

the discrete-time domain waveform y^T_{in} is converted into the discrete frequency domain, and the signal power outside the predefined frequency bands (or in-bands) is attenuated by matrix F, then the signal is converted back to the time domain as y^T_{out}.

5.2.2 Waveform Synthesis Algorithm

The waveform synthesis algorithm generates optimized input data for two interleaved DACs in such a way that the mean-square error (MSE) between the reference signal and the generated signal is minimized within a given bandwidth. A high-precision discrete-time reference signal is digitally computed and generated using direct digital synthesis (DDS) algorithms that use a bit resolution that is finer than the hardware-defined data converter bit resolution. This discrete reference signal consists of digital samples with a sampling rate of *4fs*, where *fs* is the sampling speed of each DAC used in the proposed hardware architecture. The discrete-time reference signal with a bit resolution of 32 used in this thesis, $y^{T}_{r(32\text{-}bit)} = [yr[1]\ yr[2]\ yr[3]\ \ldots\ yr[4n]]$ (n is an integer and power of 2), can be a multitone signal with a proper amplitude/phase modulation or random jitter injected if needed. The generalized expression for this signal is shown in Equation 68 below:

$$y_r[k]_{(32-bit)} = \sum_{m=1}^{\alpha} A_m\left(\frac{k}{4f_s}\right)\cdot \sin\left(2\pi f_m \frac{k}{4f_s} + \varphi_m\left(\frac{k}{4f_s}\right)\right), k = 1,2,\ldots,4n \qquad \text{Equation 68}$$

where f_m denotes the frequency of the reference signal, α is the number of spectral components, and $Am(.)$ and $\varphi m(.)$, respectively, represent the amplitude and phase modulation functions. Phase noise injection is achieved through predefining $\varphi m(.)$ and using it in the reference signal. Periodic or random phase noise components are defined as

$$\varphi_{\mathrm{m}}(t) = \sum_{k} A_{p,k} \sin(2\pi f_{p,k} t) + n_p(t) \qquad \text{Equation 69}$$

where $A_{p,k}$ and $f_{p,k}$ denote the amplitude and the frequency of the k^{th} periodic phase noise term, respectively, and n_p indicates a random phase noise component. These phase noise

terms defined in the reference signal are reconstructed in the synthesized waveform and consequently in the analog signal output of the two DACs.

In this study, we use a 32-bit DDS algorithm (without using signal dithering) to derive a high-precision discrete-time reference signal. With this well-defined reference signal y_r, two algorithms are presented to generate the optimized input data of two interleaved DACs.

5.2.3 Signal Synthesis Algorithm

The signal synthesis algorithm calculates the high-resolution (32-bit) data ($\boldsymbol{x}_c$) for the matrix models in such a way that one of its output image tones perfectly reconstructs the target signal within a given bandwidth (defined by band-limiting matrix model). This can be illustrated as a minimization of Equation 70.

$$\left\| y_{t(4n\times 1)} - H_{total(4n\times 2n)} x_{c(2n\times 1)} \right\| \qquad \text{Equation 70}$$

$$H_{total(4n\times 2n)} = H_{filter(4n\times 4n)} H_{c(4n\times 2n)} \qquad \text{Equation 71}$$

$$y_{t(4n\times 1)} = H_{filter(4n\times 4n)} y_{r(4n\times 1)} \qquad \text{Equation 72}$$

As mentioned before, since H_{total} is not invertible, we solve this linear problem by using the pseudo-inverse of H_{total} [82]. The singular value decomposition is used since it is a computationally simple, accurate way to compute the pseudo-inverse of a matrix. If the singular value decomposition of H_{total} is

$$H_{total(4n\times 2n)} = U\Sigma V^* \qquad \text{Equation 73}$$

where U is a $4n\times 4n$ real (or complex) unitary matrix, $\sum$ is a $4n\times 2n$ rectangular diagonal matrix with nonnegative real numbers on the diagonal, and V^* (the conjugate transpose of V) is a $2n\times 2n$ real (or complex) unitary matrix, the pseudo-inverse of H_{total} is derived as

$$H^{+}_{total(4n\times 2n)} = V\Sigma^{+}U^{*} \quad \text{Equation 74}$$

where $\sum^{+}$ (the pseudo-inverse of $\sum$) is obtained by taking the reciprocal of each nonzero element on the diagonal, leaving the zeros in place, and transposing the resulting matrix. The pseudo-inverse estimation (shown in Equation 73 and Equation 74) can be computed once for all waveform generation unless the configuration of the reconstruction filters is changed. For this reason, the pseudo-inverse can be precomputed offline.

The estimated pseudo-inverse of H_{total} derives the solution of the linear system as below:

$$\hat{x}_{c(2n\times 1,32-bit)} = H^{+}_{total(2n\times 4n)} \cdot y_{t(4n\times 1,32-bit)} \quad \text{Equation 75}$$

where the solution minimizes the quantity of Equation 70.

5.2.4 Noise-Shaping Algorithm

With signal synthesis algorithm presented, a simple optimization process is used to shape quantization noise away from interested band. Any mixed integer optimization program could be used in this process to minimize[83]

$$\left\| \xi \cdot H_{total(4n\times 2n)} \cdot \vec{Z}_{(2n\times 1)} - H_{total(4n\times 2n)} \cdot (\vec{x}_c - \vec{x}_{quan}) \right\| \quad \text{Equation 76}$$

where ξ is the minimal quantization level, $\vec{x}_{\mathrm{c}}$ is the set of high-resolution values (32-bit) of input data obtained by Equation 75, and $\vec{x}_{\mathrm{quan}}$ is the set of rounded-down values of x after quantizing $\vec{x}_{\mathrm{c}}$. The optimization algorithm picks each entry value of binary vector $\vec{Z}$ between *0* and *1* to decide rounding down/up of each data in $\vec{x}_c$ and hence minimize Equation 76.

Assuming that 8-bit DACs are used, after obtaining the optimized value $\vec{Z}_{opt}$, the optimized input vector is calculated as below:

$$\begin{bmatrix} \vec{x}_{1(n\times 1,8-bit)} \\ \vec{x}_{2(n\times 1,8-bit)} \end{bmatrix}_{(2n\times 1)} = \vec{x}_{opt(2n\times 1)} = \xi \cdot \vec{Z}_{opt(2n\times 1)} + \vec{x}_{quan(2n\times 1)} \qquad \text{Equation 77}$$

The input data sequences for the 8-bit DAC1 and DAC2 are obtained and respectively given by $\vec{x}^{T}_{1(8\text{-}bit)}$=[$\vec{x}_1[1]$ $\vec{x}_1[2]$ $\vec{x}_1[3]$ ... $\vec{x}_1[n]$] and $\vec{x}^{T}_{2(8\text{-}bit)}$=[$\vec{x}_2[1]$ $\vec{x}_2[2]$ $\vec{x}_2[3]$ ... $\vec{x}_2[n]$].

5.2.5 Long Signal Generation with Single DAC System

In the following work, a modified higher-than-Nyquist-rate direct RF signal synthesis method is introduced to generate high-fidelity signals with specified spectral characteristics. Such signals can function as interferers during the testing of OFDM-based communication systems. The method optimizes the input to a DAC with a specified output reconstruction filter to minimize the difference between the first image of the output and the target signal across a predefined signal bandwidth. The first image (*beyond the Nyquist frequency of the DAC*) is then passed through a band-pass filter and used as the primary output of the system. This allows the modified method to shape higher-than-Nyquist-rate signal, which cannot be achieved by the direct digital synthesis (DDS) method. Compared to the original method of [78], the modified technique introduces a scalable and efficient way to calculate the optimized input data string for a desired image with specified bandwidth. The method also differs from the previously introduced one [78] in that it simplifies signal generation by using only one DAC instead of an interleaved system of DACs.

There are two limitations of the direct RF signal synthesis method discussed previously. The first involves the underlying computing complexity. Since a pseudo-

inversion needs to be performed on a matrix whose size is proportional to the number of sample points of the reference waveform, a reference waveform with a large number of sample points, which is essential for channel interference generation, leads to extensive computation. Second, the interleaved system is very sensitive to the frequency response of the power combiner used to combine the outputs of the interleaved DACs and requires careful calibration.

This long signal generation method reduces the required computational cost by allowing input vector generation via analysis of matrices of smaller size than that of the original method and simplifies the system to the use of a single DAC. The method is shown in Figure 66 below. Assuming that the discrete reference waveform y has M sample points obtained at a sampling frequency of $4f_{clk}$, it is divided into M/N subgroups where N is the length of the matrix model used in the waveform synthesis algorithm that is similar to Equation 64 with $H_c = H_1$. The optimized $N/4$-dimensional vectors are then obtained through this process and regrouped to form the input data sequence x for the DAC. The targeted band-limited signal (interferer) is then selected by a band-pass filter and used as the primary output of the system. To perform such input data generation, two matrix models, which mimic the waveform generation process and the output signal band-limiting process respectively, are required.

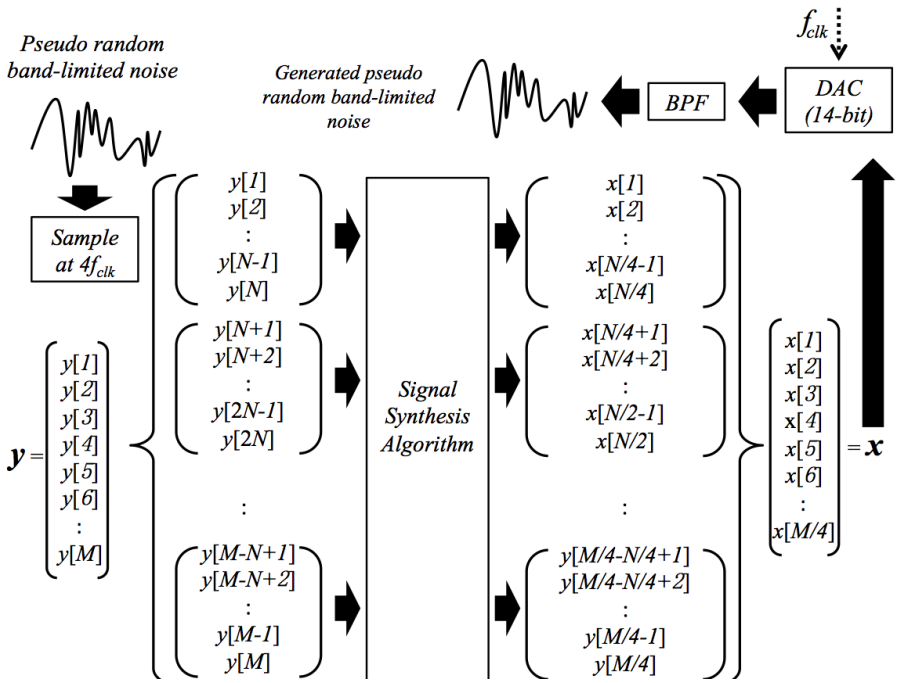
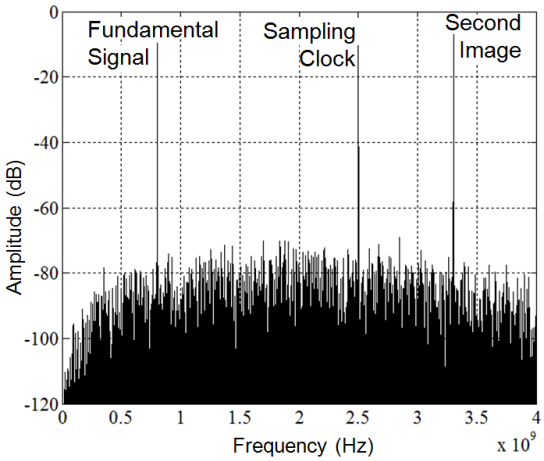


Figure 66: Block diagram of proposed band-limited channel interference generation with a single DAC.

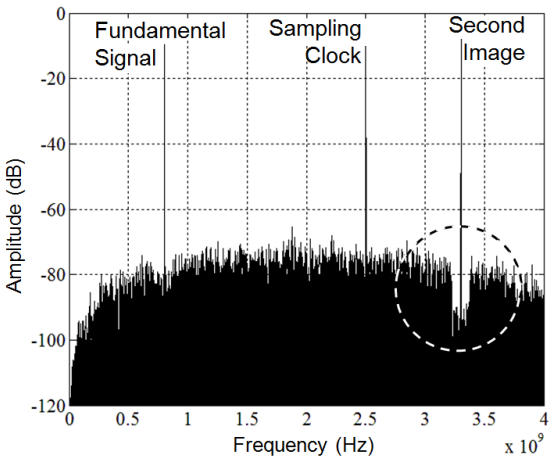
5.3 Numerical Simulation

The proposed waveform synthesis technique is validated in numerical simulation for band-limited noise injection and possible application in direct RF waveform synthesis for software-defined radio (SDR). We implement the simulation of two mixed-mode DACs with a sampling rate of 2.5 GSPS and a bit resolution of 8. The high-precision reference waveform consists of 4,096 data sample points with a sampling rate of 10 GSPS.

5.3.1 Noise Injection



(a) 3.3 GHz spectrum (or second image) synthesis without in-band noise shaping.



(b) 3.3 GHz spectrum (or second image) synthesis with in-band noise shaping of 150 MHz bandwidth.

Figure 67: Simulation on a single-tone signal synthesis with 8-bit time-interleaved data converters (with mix reconstruction filter) whose sampling rate is 2.5 GSPS.

Figure 67(a) shows the power spectrum of the higher-than-Nyquist frequency synthesis (3.3 GHz sine wave), where a high-precision reference signal is generated by using a 32-bit DDS algorithm and fed as input to the signal synthesis algorithm, but noise-shaping algorithm. In comparison, Figure 67(b) shows the power spectrum of a waveform with the same frequency synthesized with noise-shaping algorithm performed at a bandwidth of 150 MHz. The noise floor or spurious distortion level of the in-band spectrum in Figure 67(b) is lower than that of Figure 67(a) by 14.1 dB, which results in enhanced spurious-free dynamic range (SFDR). The out-band noise level is, however, increased in Figure 67(b) because of noise shaping. The relation between the filter bandwidth and in-band SFDR is shown in Figure 68 (for 3.3 GHz waveform synthesis). If the filter bandwidth increases to 0.7 GHz, SFDR approaches that of the spectrum obtained without using in-band noise shaping (68 dB).

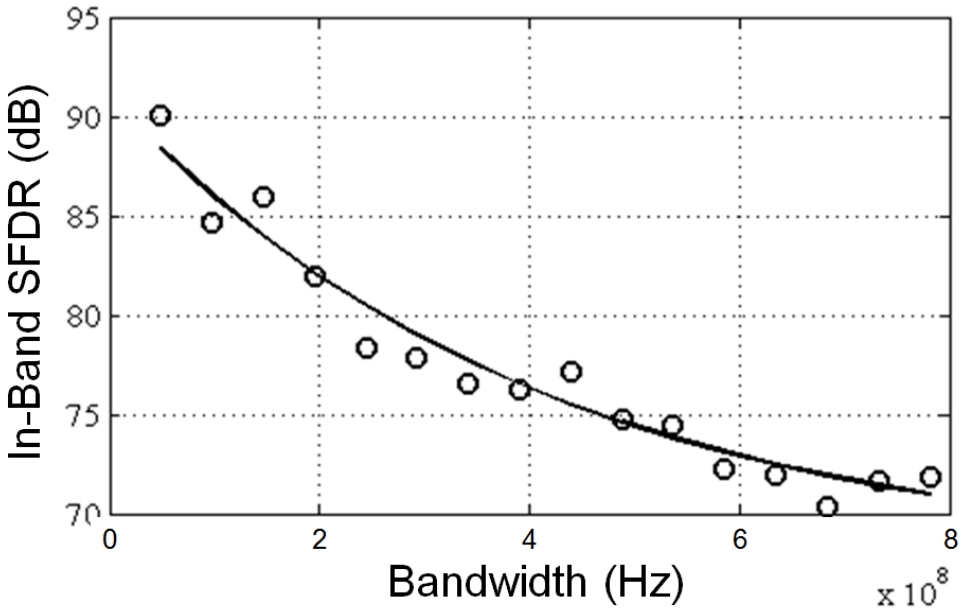
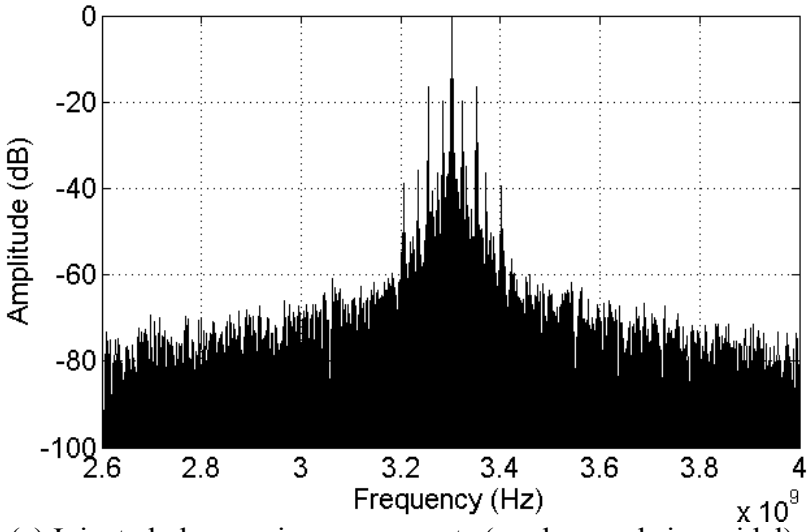


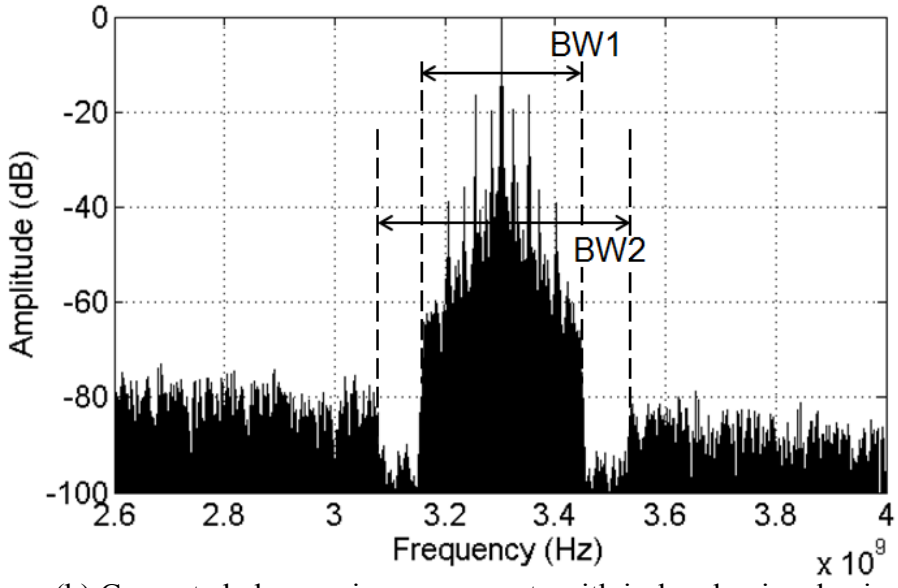
Figure 68: Relation between in-band SFDR and noise-shaping-filter bandwidth (for 3.3 GHz waveform synthesis).

Phase noise injection (based on Equation 68) is validated in simulation. Periodic phase noise terms ($f_{p\_1} = 20\ MHz$ and $f_{p\_2} = 50\ MHz$) and random phase noise components are digitally injected to the discrete-time reference signal with a carrier frequency of 3.3 GHz. In Figure 69(b), the spectrum synthesized with two different band-limiting matrix models of different filter bandwidths (BW1=0.3 GHz for signal synthesis algorithm; BW2=0.5 GHz for noise-shaping algorithm) is shown, and the reference signal with injected phase noise is shown on Figure 69(a). With the help of the noise-shaping algorithm and band-limiting matrix model described in Section 5.2.1.2 and Section 5.2.4, the power spectra of the reference waveform and the generated waveform are very similar within the frequency band of interest. In addition, a clear reduction on in-band noise is also observed due to in-band noise shaping. However, the spectra outside the frequency band of interest are different. This is because the proposed waveform synthesis

algorithm aims at minimizing in-band synthesis errors only within the frequency band of interest.



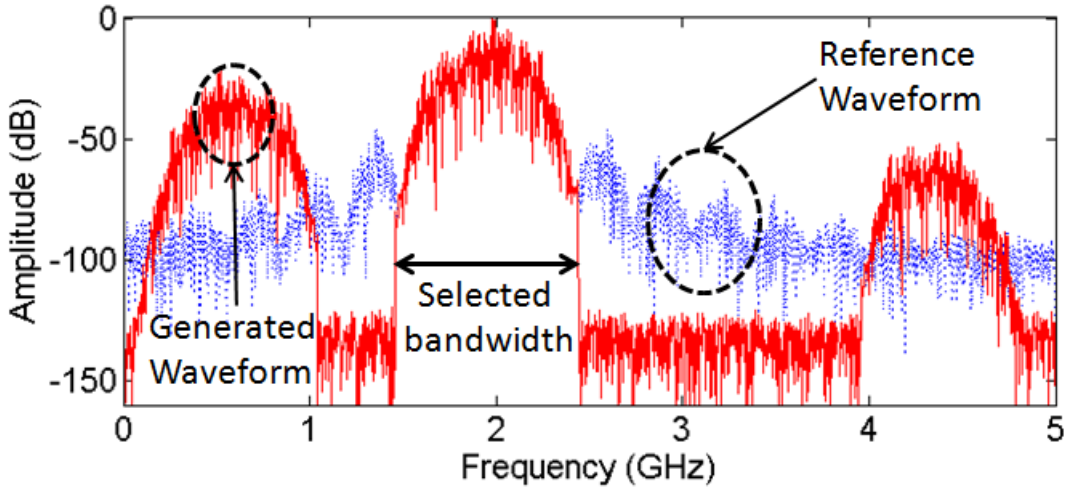
(a) Injected phase noise components (random and sinusoidal).



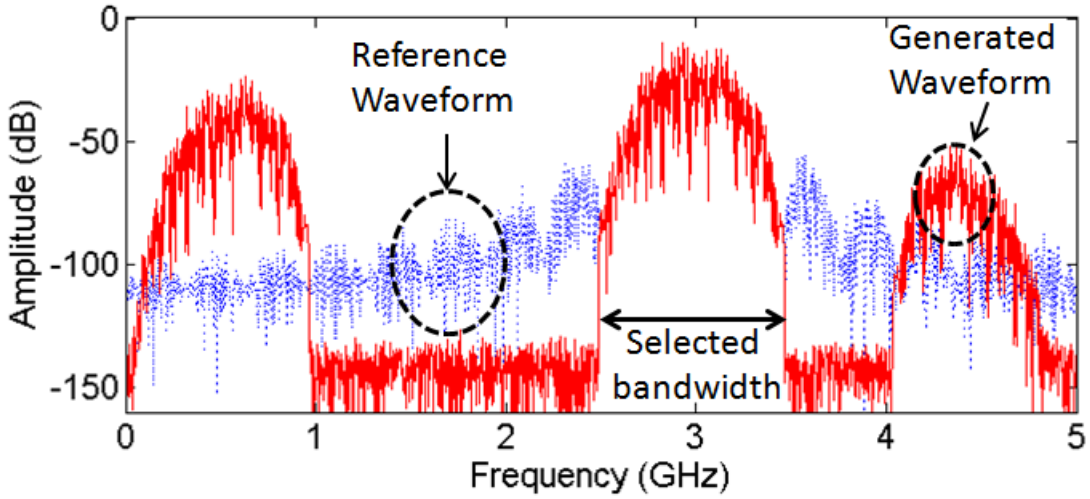
(b) Generated phase noise components with in-band noise shaping.

Figure 69: Simulation on phase noise generation: (a) injected phase noise components (random and sinusoidal) and (b) generated phase noise components with in-band noise shaping.

5.3.2 Direct RF Waveform Synthesis



(a) MSK modulation with a carrier frequency of 2 GHz.



(b) MSK modulation with a carrier frequency of 3 GHz.

Figure 70: Simulation on minimum shift keying (MSK) waveform generation with 625 Mbps data speed.

Since the proposed method offers minimal distortion on a band-limited RF signal, it has the potential of being used in software-defined radio. In a typical SDR, two reconfigurable parts are essential: a tunable phase-locked loop (PLL) and reconfigurable filters for channel selection and isolation [84] . By calculating the output modulated and upconverted RF waveform of a sequence of bit pattern, using it as the discrete-time

reference signal (y_t), and solving Equation 75, the corresponded input data to the interleaved DAC system is obtained, and the spectrum of the output waveform of the interleaved DAC system is identical to that of the reference signal within the selected bandwidth. As opposed to the conventional phase-locked loop (PLL) based software-defined radio architecture, the proposed method only requires a fixed-frequency system clock, and it is able to change the carrier frequency instantaneously. And since the reference waveform is digitally generated, a synthesized waveform inherently has a very wide carrier frequency range.

This ability is demonstrated through simulation by generating an upconverted signal with minimum shift keying (MSK) modulation. The carrier frequencies of generated signals are 2 GHz in Figure 70(a) and 3 GHz in Figure 70(b). As it is observed in the figure, the spectrum of the waveform generated through the proposed method follows that of the reference waveform tightly within the selected bandwidth. The sharp edges between the selected in-band and out-band noise also reduce the power of sidebands and hence reduce out-of-band interference between signal carriers in adjacent frequency channels. Note that a reconfigurable band-pass filter is still needed to isolate the frequency band of interest.

Since the distortion on the synthesized RF waveform is related with the width of the selected bandwidth, the simulated bit error rate performance of a fixed selected bandwidth (800 MHz) under a different bit rate is presented in Figure 71. A simulation has been done to compare the transmited time domain waveform of the MSK modulated signal and the received one after downconvertion. In the simulation, the MSK signal is upconverted by a 2 GHz carrier wave and sampled at 10 GSPS to create the discrete

reference signal. The proposed algorithm is then used to calculate the corresponding input data to the interleaved DACs system based on this reference signal. The waveform that is generated by the system is passed to a band-pass filter and then subjects to a conventional downconversion with a mixer. Figure 72(a) shows the target MSK modulated waveform, and the downconverted MSK modulated signal from the direct generated RF signal is shown in Figure 72(b). The details of the waveforms at each stage of the synthesis are presented in the experimental section.

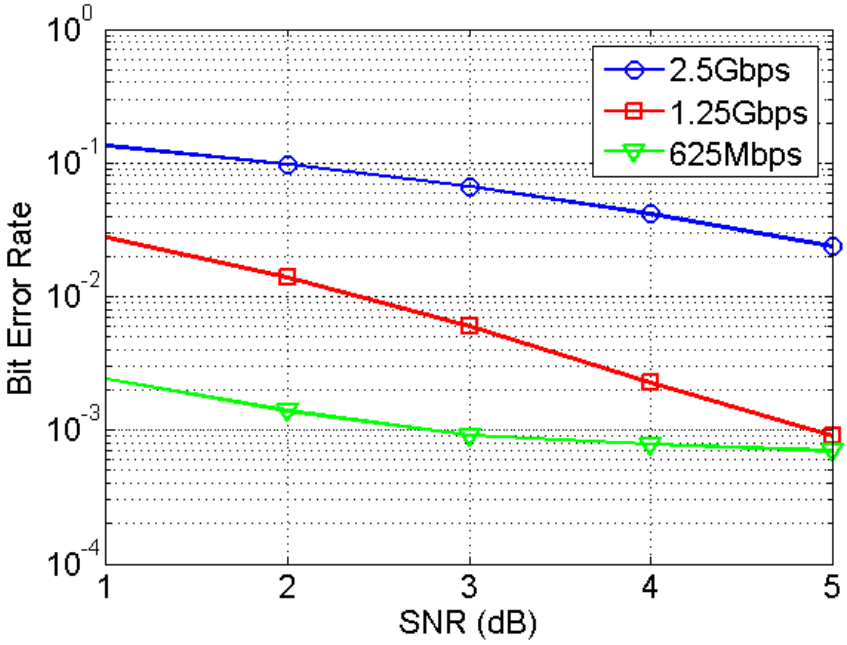
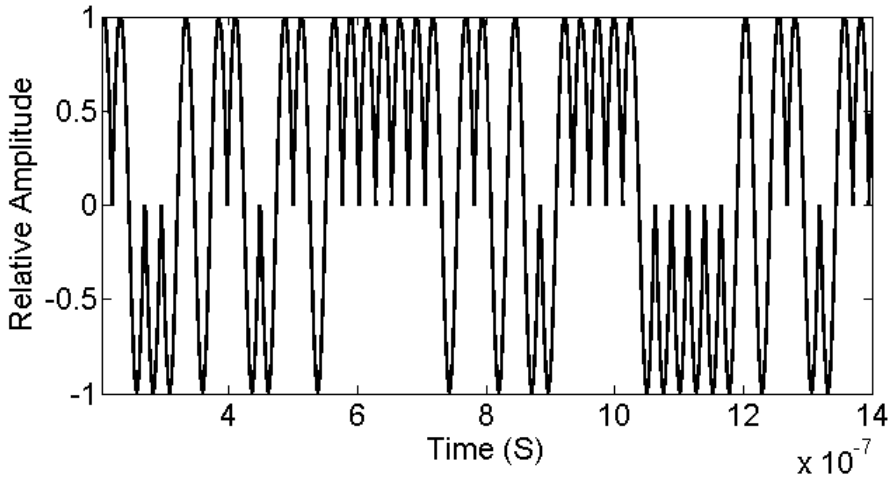
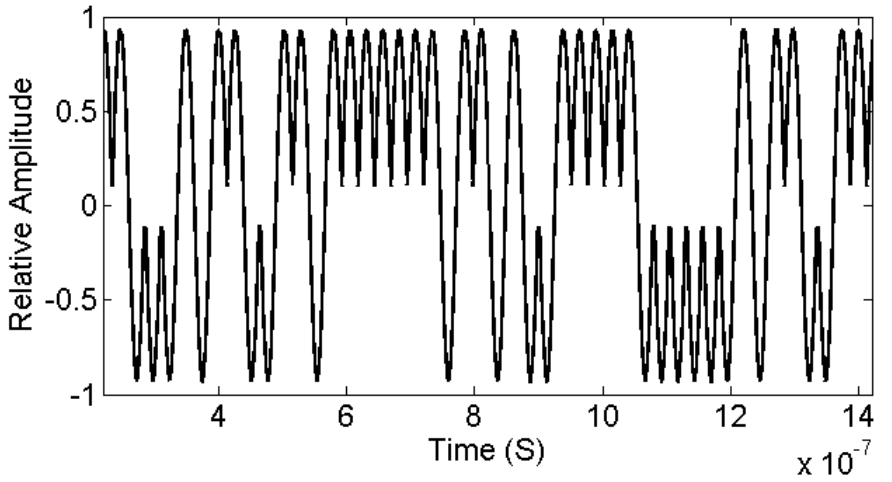


Figure 71: Bit error rate with different bit rate.



(a) Target MSK modulated waveform.

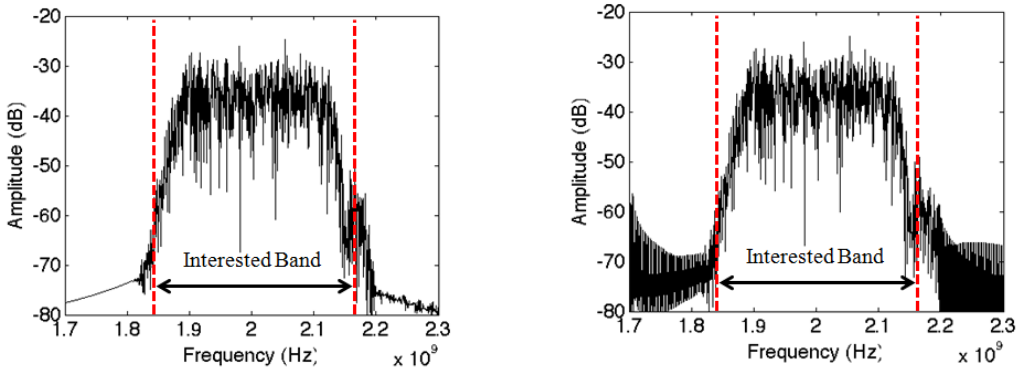


(b) Received MSK modulated waveform.

Figure 72: Comparison between transmitted MSK waveform and received one with 2 GHz carrier wave and proposed direct synthesizing transmitter front-end.

5.3.3 Wideband Spectrum Shaping

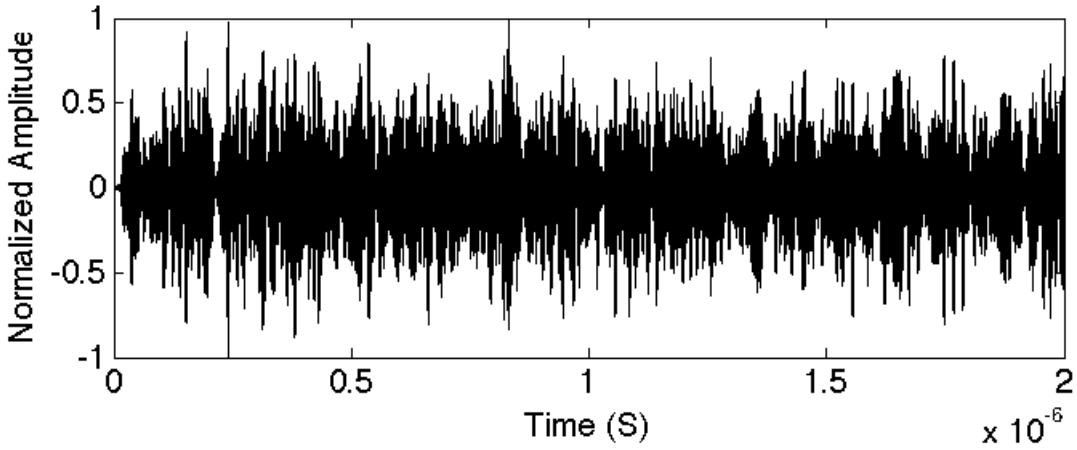
The wideband spectrum shaping technique mentioned in Section 5.2.5 is also validated in numerical simulation for a band-limited channel interference generation. In this section, the waveform synthesis process is first demonstrated with a sine wave generation. Then a wideband spectrum shaping is presented. All the simulations are done under the assumption that a 14-bit DAC with a mix reconstruction filter (as shown in Figure 63[c]) is clocked at 2.5 GHz.



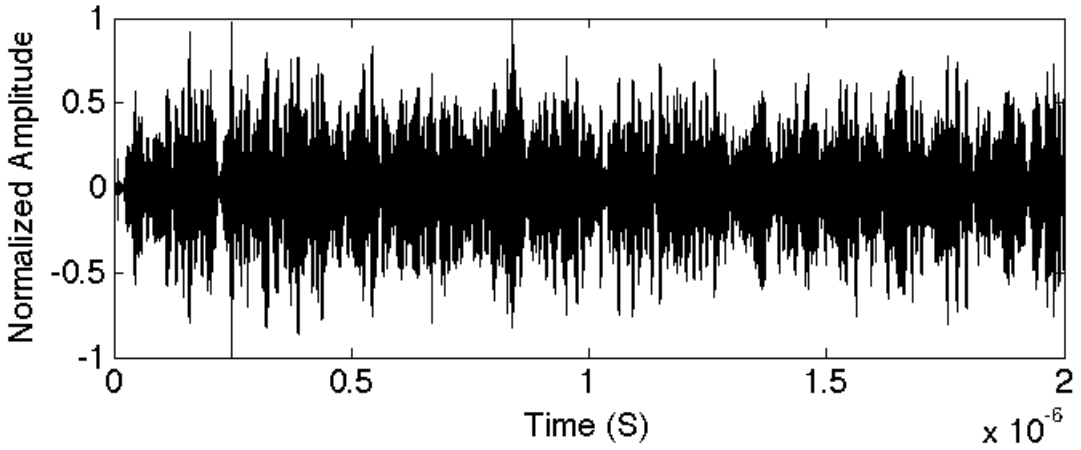
(a) (b)

Figure 73: Simulation on 200 MHz wideband interference (a) target spectrum and (b) generated spectrum.

To demonstrate the proposed method's ability to generate complex channel interferers, a reference waveform (interference with specific characteristics) with 20,480 sample points is used. The size of the matrix model of the system is 4096 x 1024. To fit the long reference waveform, it is further divided into five subgroups with 4,096 sample points each as explained previously.



(a) Time domain waveform of targeted noise.



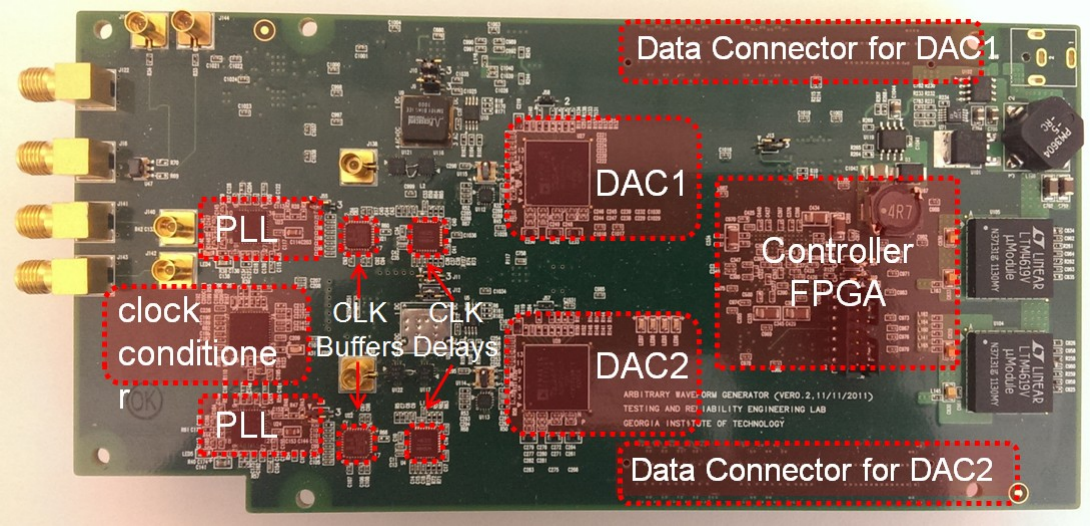
(b) Time domain waveform of generated noise

Figure 74: Time domain comparison between generated waveform and targeted one.

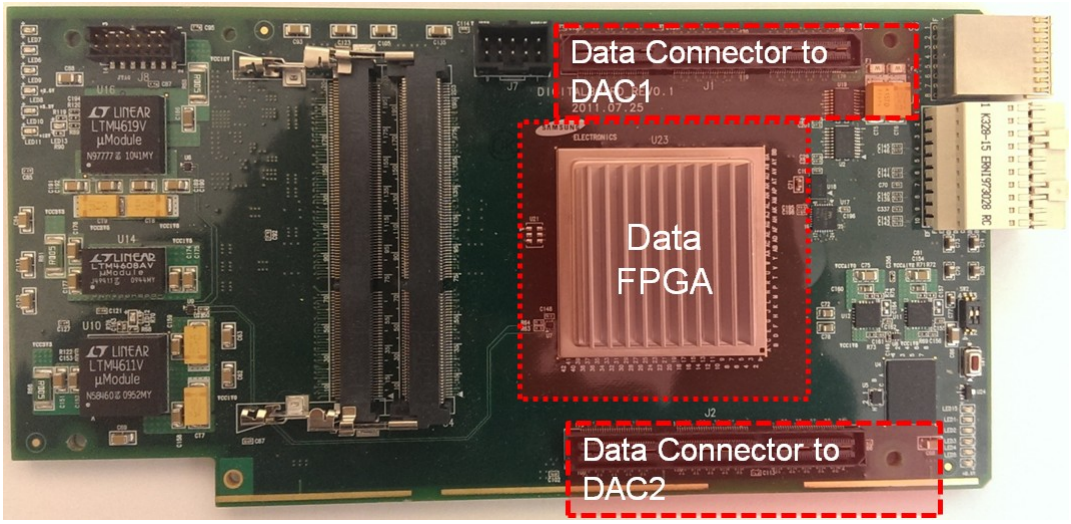
Figure 73 compares the frequency domain representation of the generated band-limited channel interferer (right) with the target interferer (left). The attenuation and distortion within the predefined bandwidth (1.9 GHz to 2.1 GHz) has been minimized by the proposed method. Also, the time domain comparison is presented in Figure 74. Note that this high-frequency interferer is generated by a single DAC clocked at 2.5 GHz, and the first image replica is used as the primary output signal.

5.4 Hardware Validation

5.4.1 Method Demonstration



(a) Picture of the arbitrary waveform generator (AWG) board.



(b) Picture of the digital board for digital sample data generation.

Figure 75: Picture of a hardware prototype used for experiments.

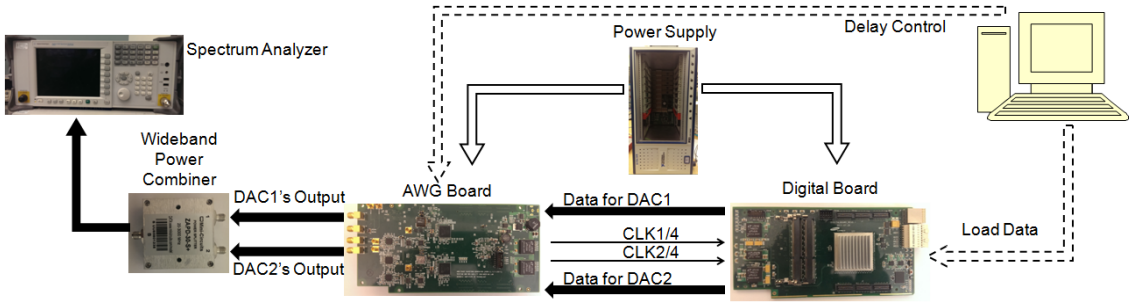
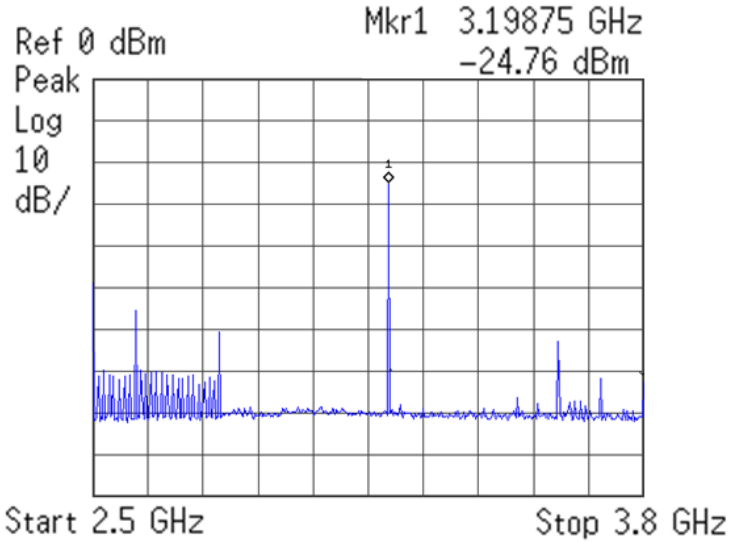


Figure 76: Hardware experiment setup.

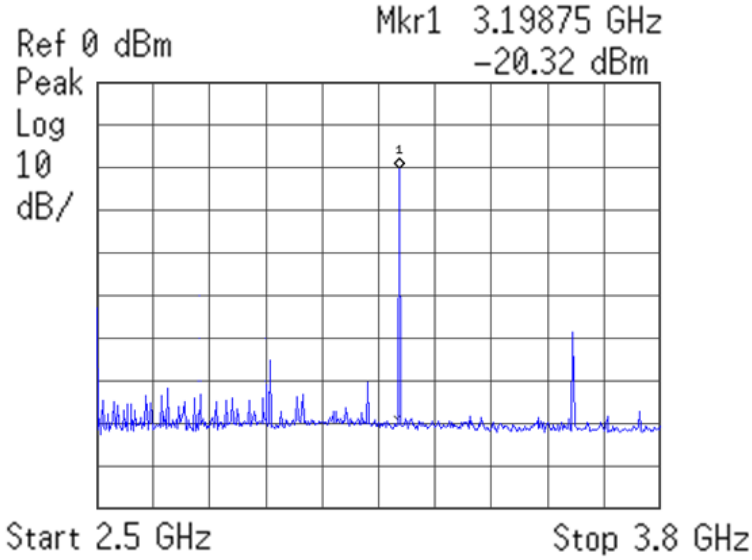
A hardware prototype consisting of two separate boards (AWG board and digital board) is designed to validate the proposed algorithm. AWG Board shown in Figure 75(a) contains two identical DACs (Analog Devices AD9739A) with a maximum sampling rate of 2.5 Gbps. A clock conditioner with a crystal oscillator generates a 100 MHz reference clock for two separate phase-locked loops (PLLs) and associated voltage-controlled oscillators (VCOs) that generate sampling time bases (2.5 GHz is used in this application). The two sampling time bases are independently time-delayed by delay components to realize time-interleaved sampling, whose sampling time points are spaced by the amount of Ts=4, before being fed to the clock inputs of the two DACs. An onboard control FPGA (Xilinx Spartan 6) provides a control interface to these components described above. Digital board shown in Figure 75(b) contains an FPGA (Xilinx Vertex 6) that is synchronized with AWG board in operation frequency and provides digital sample data to DACs on AWG board through high-speed data connectors. Pre-calculated and optimized sample data obtained from the proposed algorithm are stored in memory blocks implemented in the FPGA. In addition, digital logics such as serializers and data buffers are implemented for synchronized data delivery. Figure 76 shows an experiment setup where time-interleaved 2.5 GHz sampling time bases and 8-bit resolution are used for the DACs. An external power combiner is used to combine the signal outputs of the

two DACs. The generated signal is fed to a spectrum analyzer for signal analysis of the effect of noise shaping or phase noise injection.

The single-tone 3.2 GHz waveforms generated with and without using noise shaping are respectively shown in Figure 77(a) and Figure 77(b). In Figure 77(a), the in-band (2.8 GHz to 3.6 GHz) noise level is low because of the noise-shaping effect, while the out-of-band noise is increased.



(a) A single-tone generation with noise shaping.



(b) A single-tone generation without noise shaping.

Figure 77: Spectrum measurement with and without noise shaping.

Figure 77 shows a synthesized waveform with 250 MHz filter bandwidth and 20 MHz deterministic phase noise injection (-67d Bc/Hz). In the figure, the second image tone is used as the primary output, while the power of the first image tone is suppressed by the amount of 40 dB using the proposed technique, even though it is not completely removed because of the potential gain/phase mismatch between the two DAC outputs. The effect of noise shaping is observed near both the fundamental and image tones.

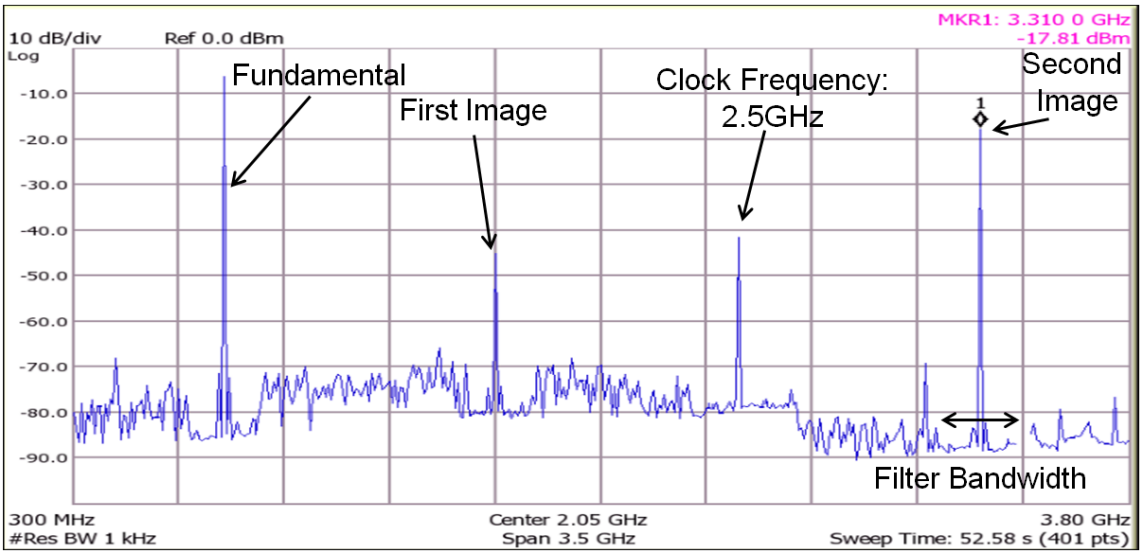


Figure 78: Wideband spectrum measurement of a 3.3 GHz sine wave (or the second image tone) with 20 MHz deterministic phase noise.

Figure 78 provides a close look at the primary output (or the second image tone) with various types of phase noise injection. Figure 79 shows 40 MHz deterministic phase noise injection with a relative power of -52 dBc/Hz. Figure 80(a) shows random phase noise injection where the filter bandwidth of the least-square data optimization (BW1) is narrower than the filter bandwidth of noise shaping (BW2). This results in the random phase noise power that is confined in BW1, while the noise-shaping algorithm shapes quantization noise outside BW2, which reduces the noise floor by more than 10 dB. In Figure 80(b), both deterministic phase noise (20 MHz and 40 MHz) and random phase noise (10 dB/Hz less than that of Figure 80[a]) are shown.

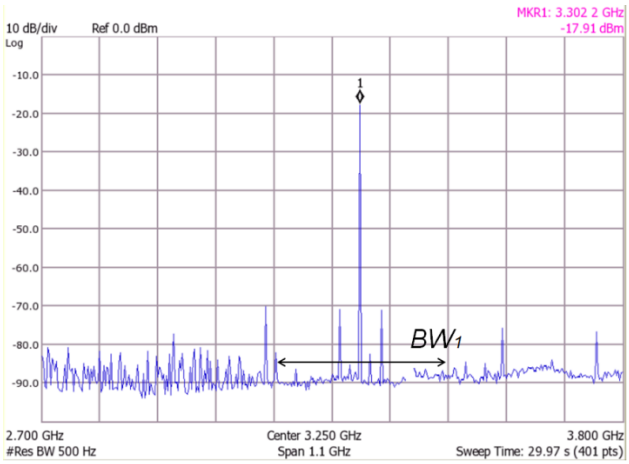
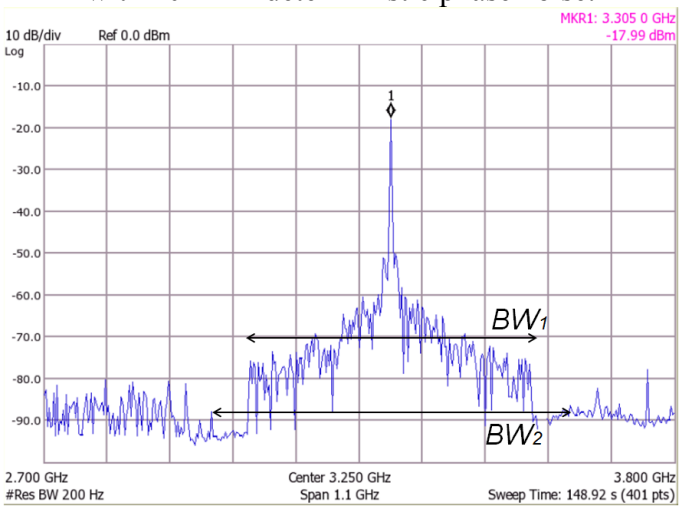
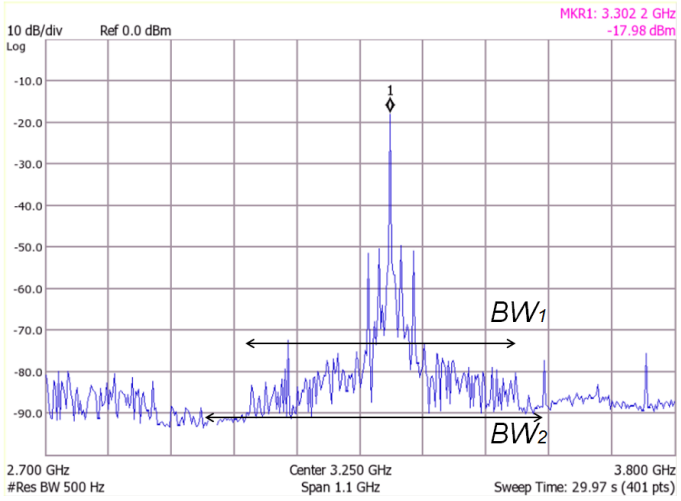


Figure 79: Spectrum measurement of a 3.3 GHz (or the second image tone) sine wave with 40 MHz deterministic phase noise.



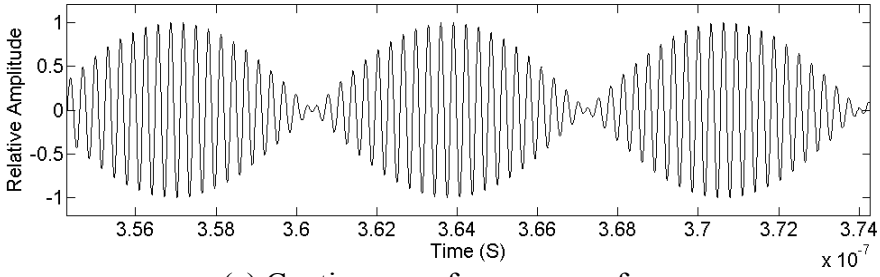
(a) Random phase noise.



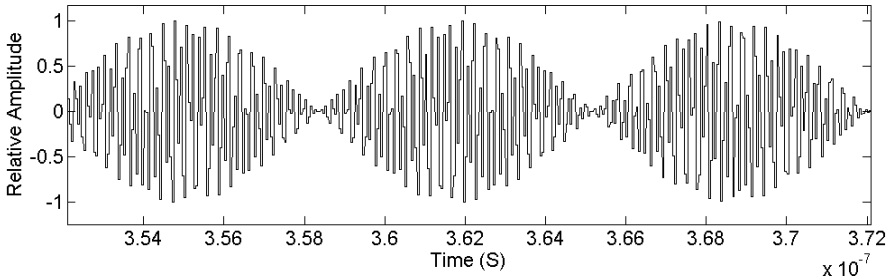
(b) 20 MHz/40 MHz deterministic phase noise and random phase noise.

Figure 80: Spectrum measurement of a 3.3 GHz (or the second image tone) sine wave with various types of phase noise.

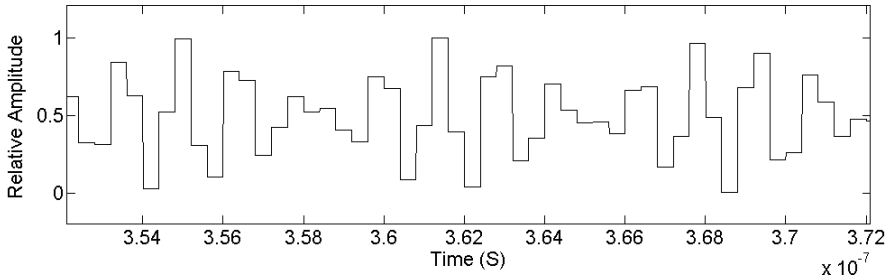
The time domain waveform of each step for a multitone RF signal generation (3.125 GHz and 3.271 GHz) with a single DAC system (let $H_1 = H_c$ in Equation 64) that is clocked by 2.5 GHz is also demonstrated to enhance the understanding of the whole process. As shown in Figure 81, the continuous reference signal is shown in Figure 81(a), and the discrete one sampled at 10 GHz is presented in Figure 81(b). By using the discrete data as input to a modified DAC system, the actual input data (shown in Figure 81[c]) to the system is calculated. The synthesized waveform with mix reconstruction filter used is presented in Figure 81(d), and the waveform after band-pass filtering is shown in Figure 81(e). An experiment result is also presented in Figure 81(d) for comparison. As seen from Figure 81, the time domain waveform of the experimental result has more attenuations than the simulated output. Such attenuation is caused by the non-ideal band-pass filter used in the experiment. The screenshot of the waveform is also shown in Figure 82.



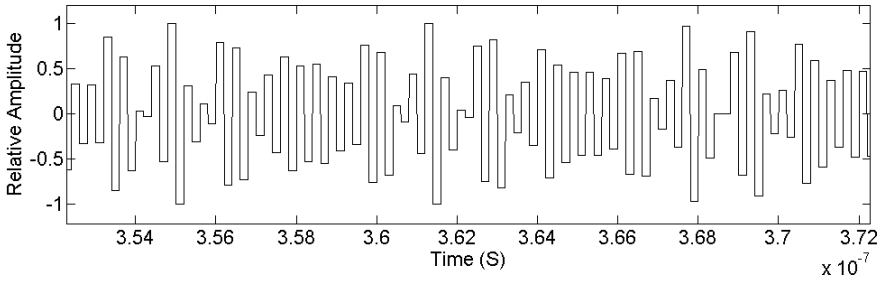
(a) Continuous reference waveform



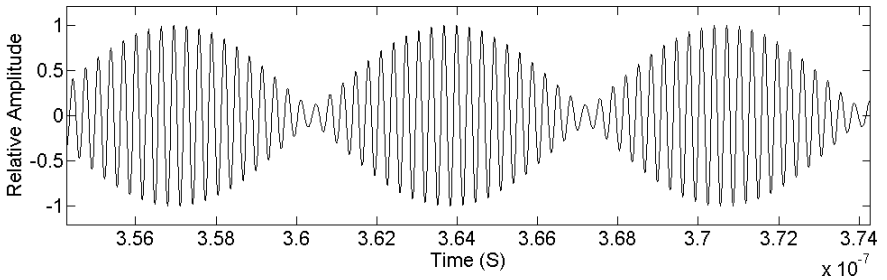
(b) Discrete reference waveform (sampled at 10GHz)



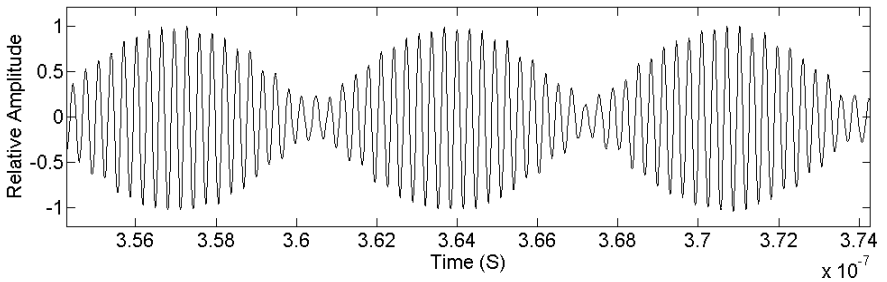
(c) Calculated input for DAC



(d) Output of DAC using mixed filter



(e) Output of DAC after filtering



(f) Experimental result

Figure 81: Waveforms of entire RF signal generation process.

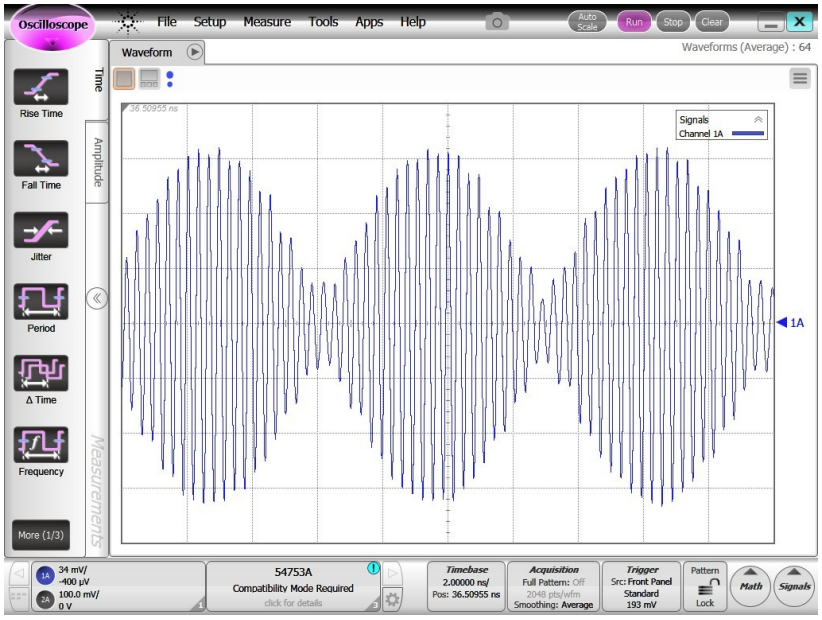
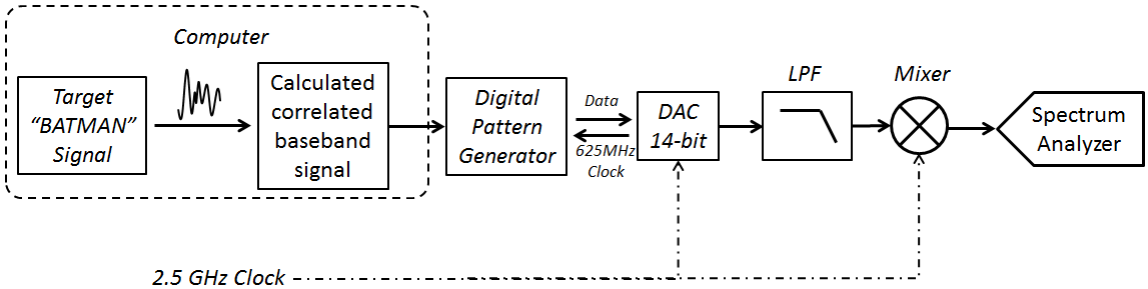


Figure 82: Screenshot of the experimental result (generated by a single DAC at 2.5 GHz clock frequency).

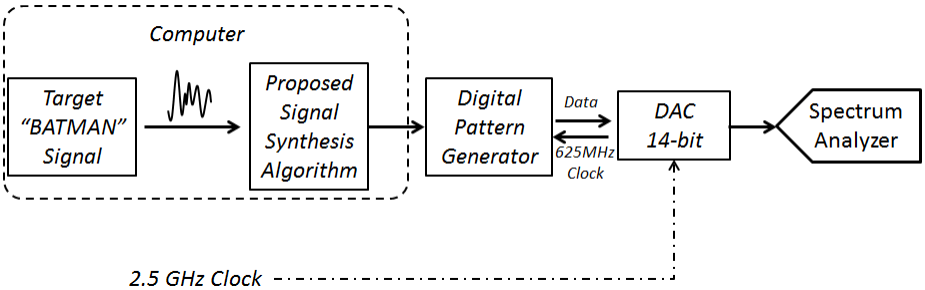
5.4.2 Comparison with Existing Techniques

Since using a mixer to upconvert a baseband signal to radio frequency is commonly used for high-speed signal generation, this experiment was set up to demonstrate that the RF waveform generated using the proposed method suffers significantly less distortion as compared to one generated using an upconversion mixer [85]. The test setups for both methods are presented in Figure 83.

To demonstrate the benefits of the proposed approach on a wideband RF waveform, a signal with sharp band-limited spectrum is used as the reference waveform. As shown in Figure 84, the signal has a bandwidth of 200 MHz and is centered at 2 GHz. Because of the shape of the spectrum, this target waveform is referred to as the “BATMAN” signal for future reference [86].



(a) Conventional method



(b) Proposed method

Figure 83: Experimental setups for (a) Conventional method (b) Proposed method.

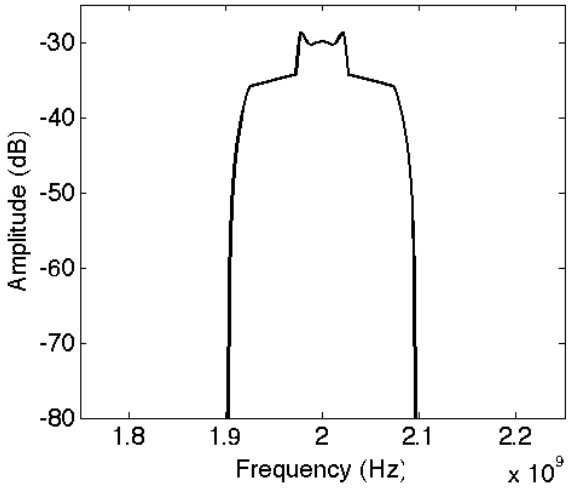
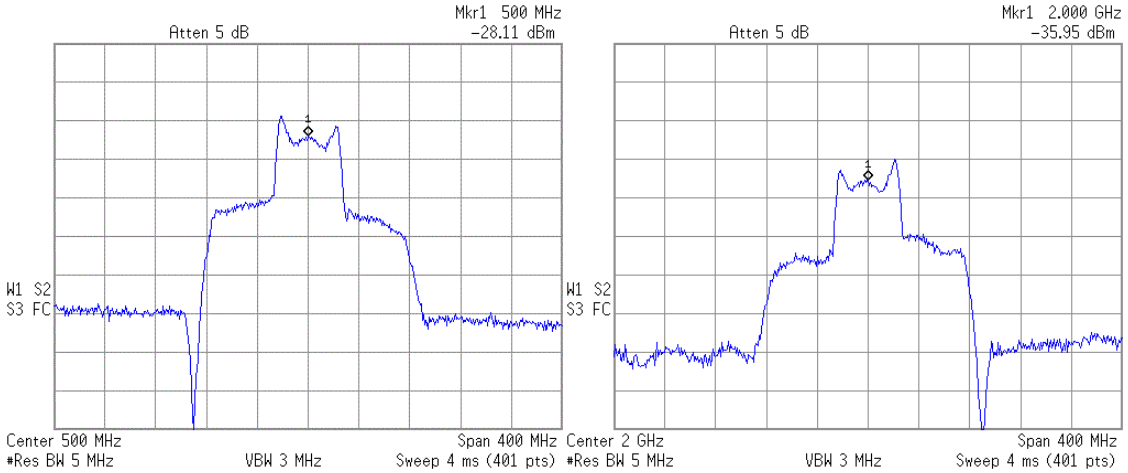


Figure 84: Spectrum of target signal.

In Figure 85(a), the baseband of the target "BATMAN" signal was calculated and used as the digital input to the DAC (AD9739a, operated with ZOH reconstruction filter). This baseband signal was mixed with a 2.5 GHz carrier wave, and the spectrum of the upconverted waveform is shown in Figure 85(b), while the spectrum of the baseband signal is shown in Figure 85(a).

In the modified method, the target waveform is converted into digital samples at a sampling rate of 10 GHz. These samples are then used as the reference waveform y_c in Equation 68. Note that during the experiment for the proposed method, the DAC was operated with a mix reconstruction filter. The spectrum of the generated waveform is shown in Figure 86.

By comparing the upconverted signal in Figure 85(b) and the directly synthesized one in Figure 86, distortions were clearly observed in the upconverted signal using a mixer. This experiment demonstrates that the proposed signal generation approach produces signals with less distortion than existing schemes that use mixer-based signal upconversion.



(a) Spectrum of baseband signal (b) Upconverted signal after mixer

Figure 85: "BATMAN" signal generation with conventional upconverting method.

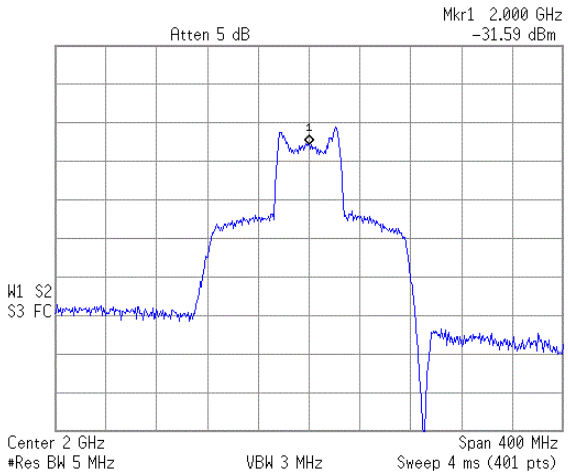


Figure 86: Spectrum of signal generated through proposed approach.

5.4.3 Channel Interference Generation in Adoptive System Testing

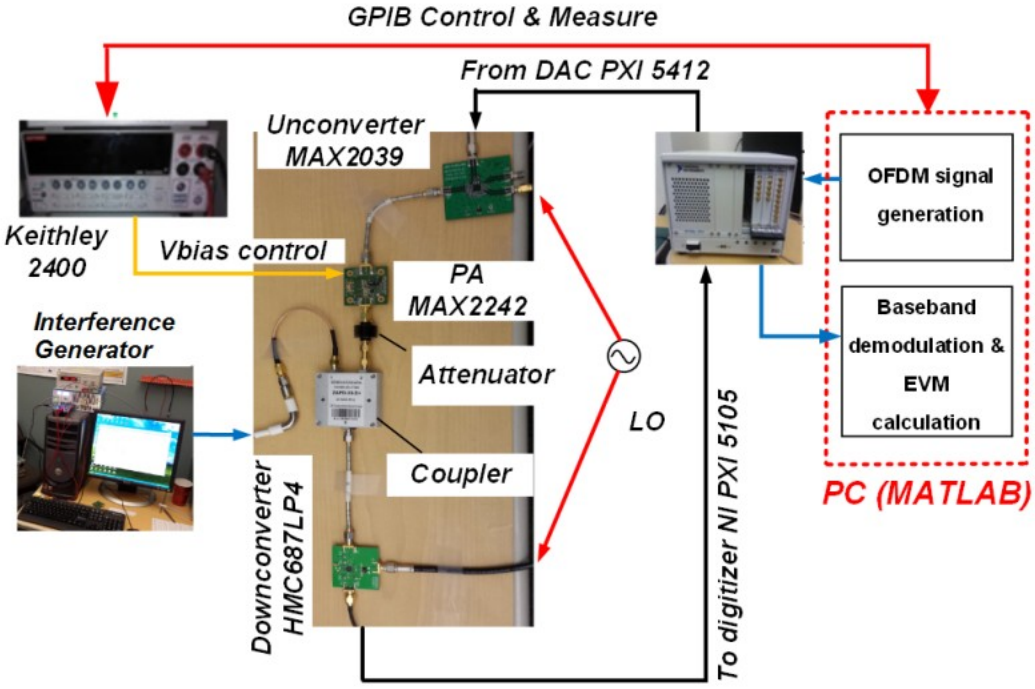


Figure 87: Transmitter adaptation hardware setup.

To demonstrate the proposed channel interference generation technique, we observe its effect on the performance of a SISO front-end as shown in Figure 87. The OFDM baseband signal generated by the PC and PXI 5412 DAC is upconverted to a center frequency of 2 GHz by MAX2039 upconversion mixer passed the channel with interferer

added, downconverted by HMC687LP4 downconversion mixer, and captured by PXI5105 digitizer. The interferer generation is performed as per the block diagram shown in Figure 88. By using different simulated channel interferers as target waveforms, different channel conditions were emulated.

The band-limited channel interference is synthesized through the algorithm suggested in Section 5.2.5 with a single DAC matrix model. By setting discretely sampled digital data of the desired type of channel interference as the target waveform, the algorithm is capable of digitally controlling the characteristic of the synthesized waveform even in the high-order Nyquist zones. Figure 89 shows the spectrum of the band-limited channel interference thus generated.

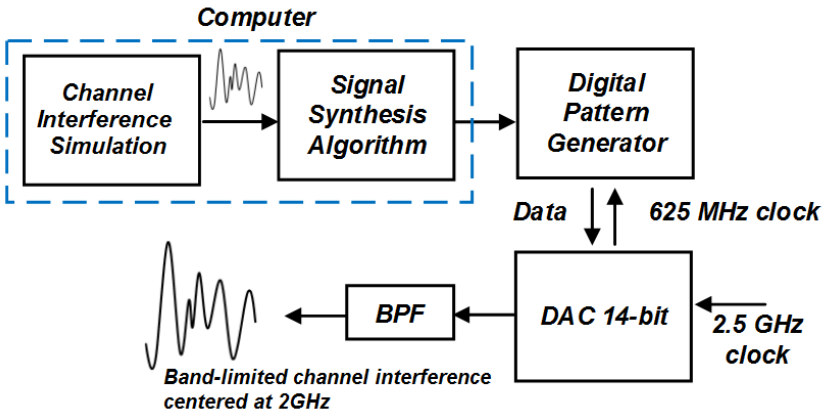


Figure 88: Band-limited channel interference generation setup.

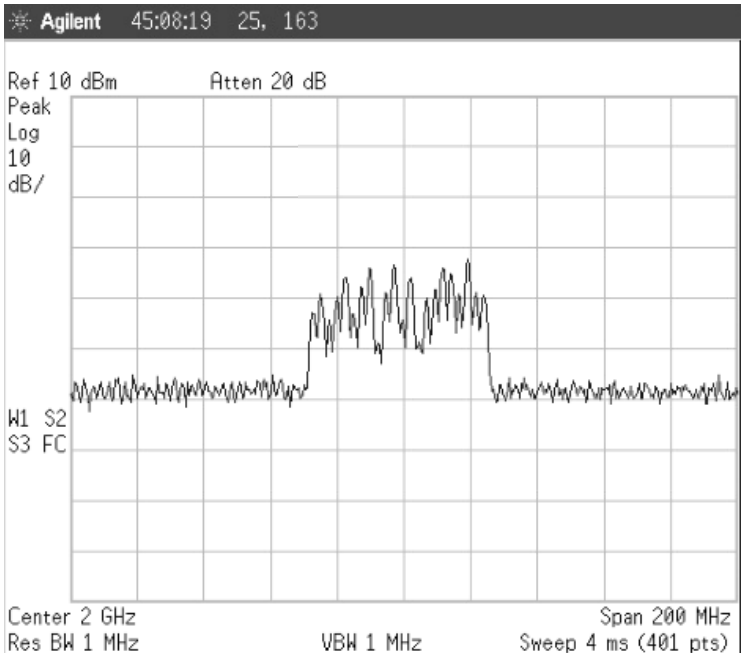


Figure 89: Band-limited channel interference spectrum.

Figure 89 shows the spectrum of the generated band-limited interferer. The interferer generation setup injects variable amounts of interference into the system to create different channel conditions, depending on the channel condition (or interference level encountered) the performance of the system changes. This is observed as an increase in EVM (and correspondingly BER) for the system. The degradation in EVM with injected interference strength is shown in Figure 90 for the nominal transmitter as well as the degraded transmitter (consumes less power but worse performance). As clearly shown, the performance varies with the degraded emulated channel (more interference), allowing the interference generation algorithm to be suitable for the testing of the performance of such systems.

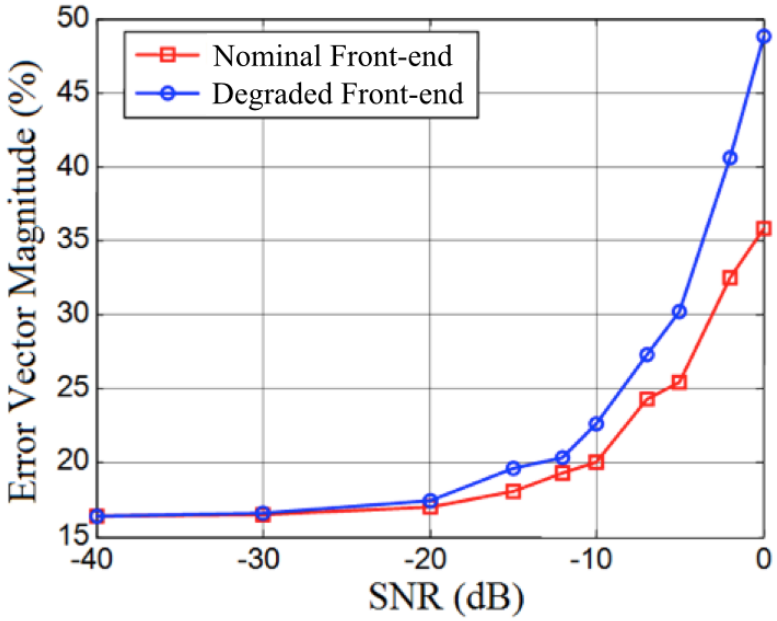


Figure 90: Variation of EVM with increasing amount of interference added to the channel.

CHAPTER 6: CONCLUSION

The introduced safe alternative tests for power converters have not only resolved the safety issues during manufacturing test but also been extended to enable post-manufacturing self-tuning of power converters and hence improved manufacturing yield. The architectures and test-generating methodology that is used to achieve accurate predictions of power converters specifications, such as load/line regulation, DC voltage, transient peak voltage, and ripple voltage, have been explained and demonstrated using both simulations and hardware measurements. To increase the accuracy of test specification value prediction, transistor-level alternative output networks have been implemented for various types of power converters. These specially tailored output networks maximize the correlation between the stimulated response of the DUT in the alternative test configuration and the target specifications through mimicking the functionality of the conventional external test circuitry of the DUT but with significantly lower current consumption. With the reduction of current consumption, the voltage spike on the power supply pins of the DUT is reduced dramatically, and safe testing is achieved. Self-tuning architectures for power converters, which improve manufacturing yield and ensure safety during production testing, are then introduced and demonstrated based on the accurate prediction of target specifications. These self-tuning structures allow safe test of power converters with large improvements in manufacturing yield. In addition, a high-fidelity RF signal generation methodology is presented that permits band-limited high-fidelity signal generation to enable testing of advanced adaptive RF systems. This method has been demonstrated using hardware measurements and extended to generate band-limited pseudo noise for adaptive RF front-end testing.

In Chapter 2, the risk of catastrophic voltage spikes during conventional power converter testing is explained both intuitively and analytically. During closed-loop measurement, with full load current, the parasitic inductances of the IC socket lead to

severe voltage spikes at either the input or ground pin of the power converter. Such voltage spikes can result in catastrophic damage of not only the ESD diodes of the package but also the internal control circuitry and the power MOSFETs. Because of this, even though customers have specific requirements on load/line regulation of power converters, these are not tested in production but rather "guaranteed by design."

In Chapter 3, an alternative test architecture for safe power converter testing is presented [73,74,87]. The risk of voltage spikes has been resolved through the use of an alternative test architecture where external circuitry is used to mimic conventional external testing circuitry characteristics while minimizing the converter load current. By injecting an optimized electrical perturbation into the test circuitry the DUT is electrically stimulated, and its output response is captured by an ADC. Targeted specifications, such as ripple voltage, DC voltage, transient peak voltage, and load/line regulations, are then predicted through a statistical regression-based mapping model that maps the captured perturbed response of the DUT to its test specification values. This statistical mapping model is generated through a set of training experiments in which both the alternative test response of the device being tested and the conventional specifications are obtained for a set of DUTs selected across a range of process corners. A GA-based test generation process is presented where the test stimulus (device perturbation) is optimized to maximize the correlation between the alternative test response and the specifications of the DUT that are predicted from the test response . A support vector machine (SVM) based stability filter and defect filter have also been introduced to identify outlier devices that must be subjected to standard specification testing methods. Experimental results that validate the accuracy of prediction of key target specifications and other ATE measured specifications (such as R_{dson} and feedback voltage under different current condition) are shown.

In Chapter 4, a self-tuning architecture based on the alternative safe test of power converters is introduced and implemented. The alternative test circuitry has been

modified to fit on-chip for BIST application. This work is the first to apply alternative tuning concepts to power converter architectures. The mechanisms for stimulating the device and observing the DUT response are different from prior sensor-based alternative test methods for RF and mixed-signal devices. Instead of using specific test input signals, a reconfigurable transistor network is placed in the feedback loop of the converter that allows the effects of pulses generated by the switching action of the converter on the feedback DC voltage to be controlled in a flexible way. This transistor network is reconfigured dynamically, under digital control during test application, to stimulate the device. The manner in which reconfiguration is performed is optimized using a genetic algorithm to maximize test and tuning accuracy. This has the additional benefit that the complete test infrastructure can be placed on-chip instead of the use of off-chip capacitors and resistors. Experimental results are presented and prove the utility of this approach.

In Chapter 5, a high-fidelity higher-than-Nyquist-rate RF signal synthesis method is presented. The method relies on the use of pseudo-inverse over a matrix model that mimics the behavior of DACs. This allows the optimized digital input data sequence for DACs to be calculated and optimized in such a way that the difference between the image replica of the generated waveform and the targeted RF waveform is minimized within a limited band allowing the image replica to be used as the primary output. The method can be applied to both interleaved and single DAC system. The ability to generate high-fidelity RF stimulus signal aids in the synthesis of channel interferers for testing of advanced RF systems.

To conclude, this research has enabled low-cost test and tuning of difficult-to-measure device specifications of DC-DC converters and high-speed devices. The key contributions are the following:

- Designed safe alternative test structure for buck/boost converters.
- Enabled load/line regulation based self-tuning of buck/boost converters.

- Designed beyond-Nyquist-rate matrix-based high-fidelity signal generation.
- Enabled high-fidelity channel interference generation for adaptive RF system test.

In the future, the developed diagnosis technique for power converters can be extended to enable specification prediction and self-tuning for multiphase buck converters used in SoCs. The high-fidelity RF signal generation method can be used for testing of High-speed systems.

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