COMPLIANT COPPER MICROWIRE ARRAYS FOR RELIABLE INTERCONNECTIONS BETWEEN LARGE LOW-CTE PACKAGES AND PRINTED WIRING BOARD

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COMPLIANT COPPER MICROWIRE ARRAYS FOR RELIABLE INTERCONNECTIONS BETWEEN LARGE LOW-CTE PACKAGES AND PRINTED WIRING BOARD

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Dedicated to my parents

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LIST OF SYMBOLS AND ABBREVIATIONS

BGA	Ball grid array
CMOS	Complementary metal-oxide semiconductor
CTE	Coefficient of thermal expansion
DRAM	Dynamic random access memory
ENEPIG	Electroless nickel electroless palladium immersion gold
ENIG	Electroless nickel immersion gold
FEM	Finite element method
FPGA	Field-programmable gate array
HASL	Hot air solder leveling
IMC	Intermetallic compound
LTCC	Low temperature co-fired ceramic
MCM	Multi-chip module
MWA	Microwire array
OSP	Organic solderability preservative
PGA	Pin grid array

PWB	Printed wiring board
RDL	Redistribution layer
SCP	Single chip package
SEM	Scan electron microscope
SIP	Stacked ICs and packages
SMT	Surface mount technology
SRAM	Static random access memory
TAB	Tape automated bonding
TSV	Through-silicon via
WLCSP	Wafer level chip scale packaging
WLP	Wafer-level packaging

SUMMARY

The trend to high I/O density, performance and miniaturization at low cost is driving the industry towards shrinking interposer design rules, requiring a new set of packaging technologies. Low-CTE packages from silicon, glass and low-CTE organic substrates enable high interconnection density, high reliability and integration of system components. However, the large CTE mismatch between the package and the board presents reliability challenges for the board-level interconnections. Novel stress-relief structures that can meet reliability requirements along with electrical performance while meeting the cost constraints are needed to address these challenges. This thesis focuses on a comprehensive methodology starting with modeling, design, fabrication and characterization to validate such stress-relief structures. This study specifically explores SMT-compatible stress-relief microwire arrays in thin polymer carriers as a unique and low-cost solution for reliable board-level interconnections between large low-CTE packages and printed wiring boards.

The microwire arrays are pre-fabricated in ultra-thin carriers using low-cost manufacturing processes such as laser vias and copper electroplating, which are then assembled in between the interposer and printed wiring board (PWB) as stress-relief interlayers. The microwire array results in dramatic reduction in solder stresses and strains, even with larger interposer sizes (20 mm × 20 mm), at finer pitch (400 microns), without the need for underfill. The parallel wire arrays result in low resistance and inductance, and therefore do not degrade the electrical performance. The scalability of the structures and the unique processes, from micro to nanowires, provides extendibility to finer pitch and larger package sizes.

Finite element method (FEM) was used to study the reliability of the interconnections to provide guidelines for the test vehicle design. The models were built

in 2.5D geometries to study the reliability of 400 µm-pitch interconnections with a 100 µm thick, 20 mm × 20 mm silicon package that was SMT-assembled onto an organic printed wiring board. The performance of the microwire array interconnection is compared to that of ball grid array (BGA) interconnections, in warpage, equivalent plastic strain and projected fatigue life.

A unique set of materials and processes was used to demonstrate the low-cost fabrication of microwire arrays. Copper microwires with 12 µm diameter and 50 µm height were fabricated on both sides of a 50 µm thick, thermoplastic polymer carrier using dryfilm based photolithography and bottom-up electrolytic plating. The copper microwire interconnections were assembled between silicon interposer and FR-4 PWB through SMT-compatible process. Thermal mechanical reliability of the interconnections was characterized by thermal cycling test from -40°C to 125°C. The initial fatigue failure in the interconnections was identified at 700 cycles in the solder on the silicon package side, which is consistent with the modeling results. This study therefore demonstrated a highly-reliable and SMT-compatible solution for board-level interconnections between large low-CTE packages and printed wiring board.

CHAPTER 1

INTRODUCTION

1.1 Evolution of Electronic packaging

Moore's Law [1], which holds that the number of transistors on an IC doubles every 18 months, has driven the transistor scaling which enabled cost reduction and performance-enhancement at device level. However, this CMOS-based era is beginning to pose major barriers beyond 22 nm due to design complexity, minimal performance gain and escalating wafer costs. A new era focusing on packaging and architecture innovations, going beyond the shrinkage of single devices and single- or multichip wirebond and flipchip packages, is emerging to address these barriers. The future of electronic system performance, miniaturization and integration are driven by these packaging innovations.

Figure 1.1 demonstrates the evolution of electronic packaging. Conventionally single chip packages (SCPs) are used to support each single device to ensure its electrical, mechanical and thermal performance, testability, and enable the device to be attached to the system board. One popular single chip package structure is the leaded package, where the interconnections are achieved by the metal leads located on the peripheral area of the package. The main challenge of leaded package is the low pin count, which limits its application to low-end microprocessors and memories including DRAMs and SRAMs. Area array packaging significantly improved the I/O count by using the whole area of the package for interconnections. Area array packages, such as pin grid arrays (PGAs) and ball grid arrays (BGAs) have been extensively used in microprocessors.

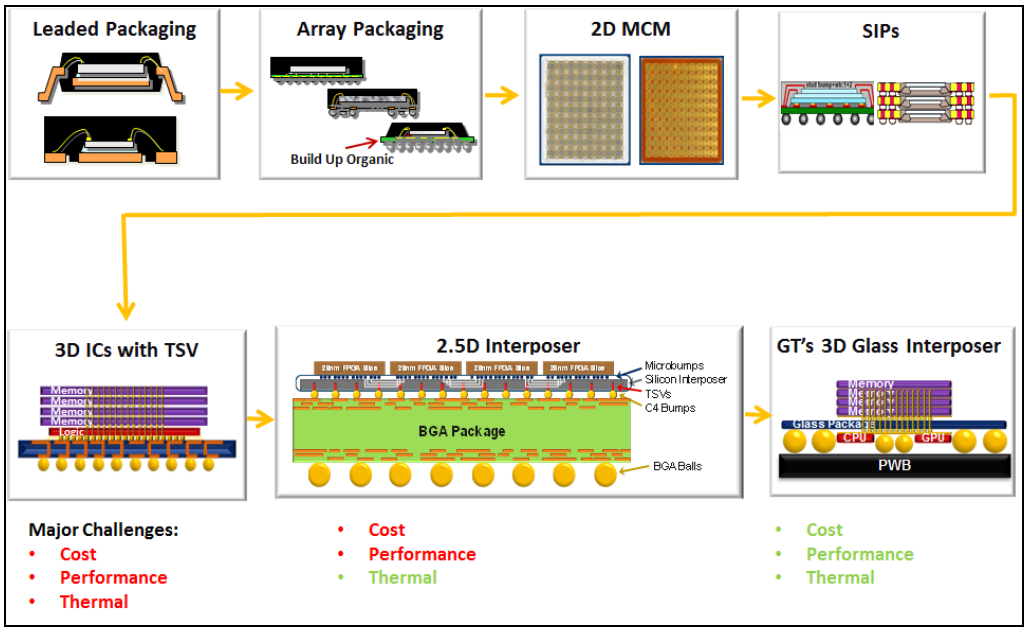


Figure 1.1 Evolution of electronic packaging.

Multi-chip packages, where multiple chips or a sub-system is packaged within one package unit, have become a major thrust because of the high performance and density compared to SCPs. Multi-chip packages allow the chips to be spaced more closely with less overall volume and weight than individually packaged parts [2]. Traditionally, multiple chips are assembled on a package in a 2D format for high-performance applications, pioneered by the ceramic MCM (multi-chip module) architecture of IBM [3]. Organic packaging, also pioneered by IBM, emerged as the next major packaging technology for these digital and also RF applications and is currently used as the primary workhorse in the industry. Such 2D systems have been limiting the system size and performance because of large interconnection lengths and package size.

To reduce the system footprint and interconnection length, stacked ICs and packages (SIPs) are emerging, where two or more layers of chips are integrated vertically. Besides the benefits of footprint and bandwidth, the SIP also enables partitioning of a large chip into multiple smaller dies which improves the yield and reduces the cost. There are two categories of SIPs: (1) stacking by wire bonds, tape

automated bonding (TAB), or flip-chip technologies, and (2) stacking by through-silicon vias (TSVs). Figure 1.2 shows an example of SIP with wire bonds. The wire bonds interconnection technology has high yield, mature infrastructure and low cost, but limits the interconnection density, since the wires are only located along the edges. Similar challenges apply to SIPs with TAB and flip-chip technologies. TSVs are being developed to enable vertical interconnection through the chips to further reduce the interconnection length and signal latency, to achieve ultra-high interconnection density and bandwidth, as illustrated in Figure 1.3. However, the 3D chip-stacking faces critical challenges including the fabrication of TSVs, process integration, management of stress and strain induced by the vias in silicon, and heat generation from the large chip stacks.

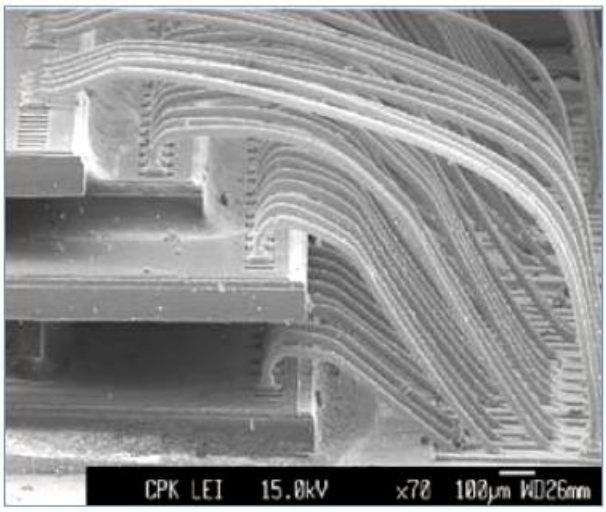


Figure 1.2 3D chip stacking with wire bonds (Courtesy of Palomar Technologies).

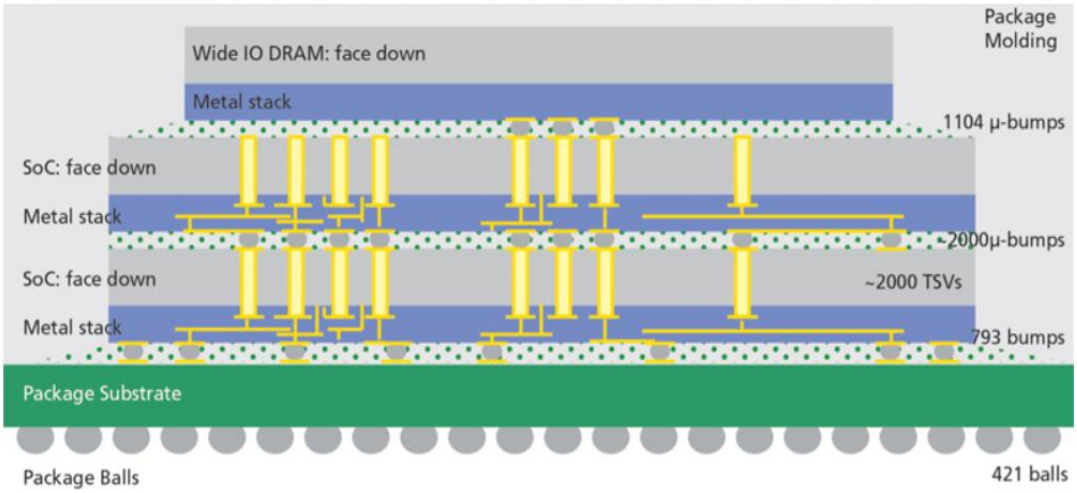


Figure 1.3 3D ICs using TSVs (Courtesy of ST- Ericsson).

To address the limits of 3D ICs, and achieve even higher performance, smaller form-factor, lower cost and higher functionality, novel concepts such as 2.5D and 3D packages are being explored.

In a 2.5D package, the ICs are integrated side-by-side through the RDLs (redistribution layers), which are several layers of copper traces and microvias. The dies are then connected to the BGAs on the board level by through-package-vias, as shown in Figure 1.4a. Copper traces with ultra-fine line and space, and microvias with ultra-fine pitch can be achieved on the packages, which allows for short interconnections between the ICs and thus high bandwidth. By having the ICs side-by-side, 2.5D packages resolves the thermal issues posed by 3D ICs, but faces challenges including larger footprint of the system and therefore performance and cost concerns.

In a 3D package, the ICs are assembled on both sides of the interposers, as shown in Figure 1.4b. The 3D packaging scheme allows for vertical interconnection between the logical and memory chips by through-package-vias at extremely fine pitch (as low as 20-40 µm), and promises even higher interconnection density and bandwidth, higher performance and lower cost compared to the 2.5D scheme.

A closer look of the interconnection structures in 3D packages is shown in Figure 1.5. There are typically two levels of interconnections in the package, which connect the copper wiring on the chip with submicron dimensions, to the wiring on the board that is much larger, typically five hundred microns to several millimeters. The first level of interconnection is between the chip and the package. This interconnection is accomplished by a variety of methods, such as wire bonding and flip chip assembly. The wiring on top side of the package is then redistributed and connected to the bottom side using through-vias. The second level of interconnection is between the package substrate to organic printed wiring board. This connection is usually achieved with metallurgical bonding using solder alloys.

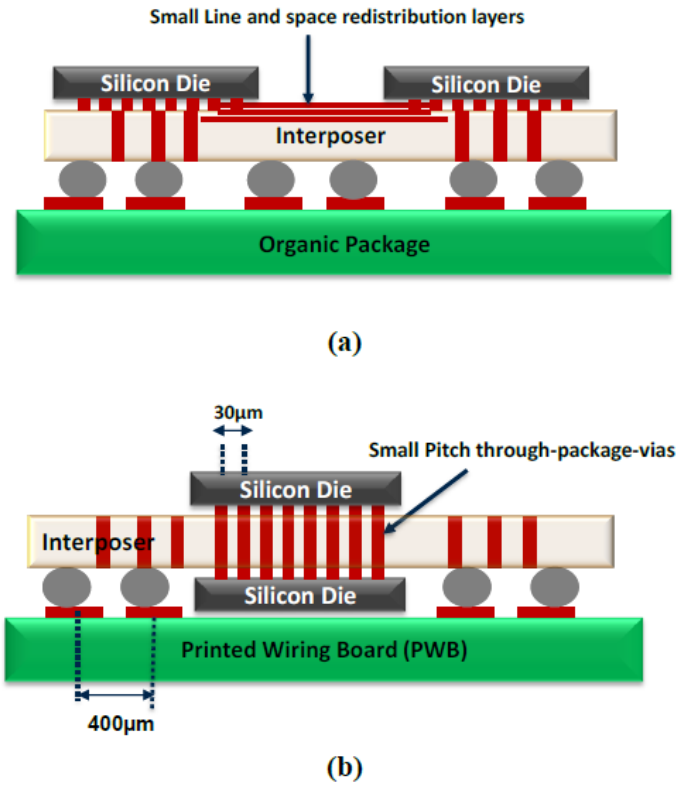


Figure 1.4 Schematic of: (a) 2.5D packages, (b) 3D packages (Courtesy of Vijay Sukumaran of Georgia Tech PRC).

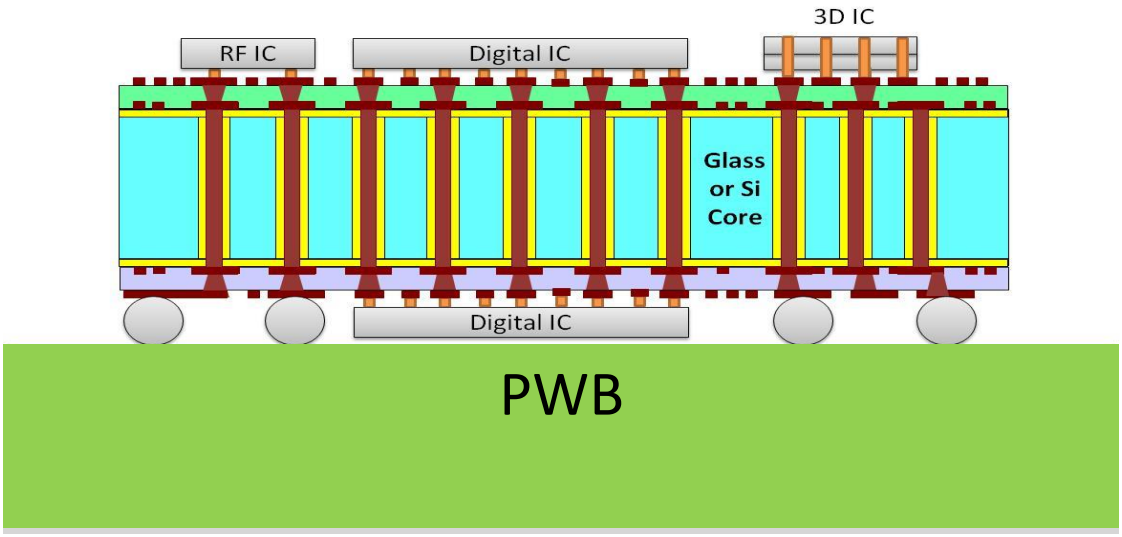


Figure 1.5 Structure of large 3D package for direct attach to PWB.

1.2 System drivers for large low-CTE packages

Both 2.5D and 3D packages aim at reducing interconnection length to lower power consumption and latency, as well as increase the number of interconnections to satisfy the demand for higher bandwidth [4]. Lower interconnection length and higher interconnection density can benefit mobile devices, such as smart phones, by enabling more sophisticated functions without increasing product size and power consumption; as well as high-performance computers, by providing 3D memory stacks close-by the processor cores. The increasing demand for heterogeneous integration, high bandwidth and computing power, therefore requires further shrinkage of the interconnection pitch at the package level (Figure 1.6), and new package materials and technologies with unprecedented wiring capability.

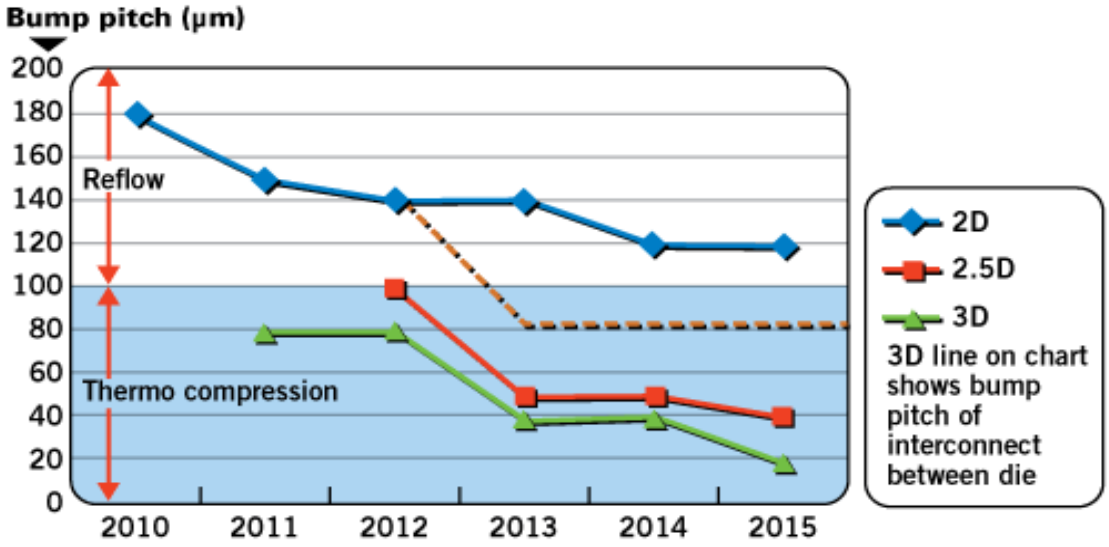


Figure 1.6 Growing I/O density and shrinking package interconnect pitch requesting low CTE packages (Courtesy of David McCann of Global Foundries).

1.2.1 Drivers for large package size: 1) integration and 2) cost

The need for high performance is also driving increase in package size. Such large package sizes are primarily needed for two reasons.

Integration: The packages for advanced smart systems are multifunctional subsystems which integrate RF chipset, passives, and mobile processors. With the growing complexity and increasing functionality, more chips and devices will be integrated on a package, thus driving the need for large mobile packages.

Cost: The requirements for high-speed computing and networking have boosted the number of transistors needed for the system. However integrating all the functions on a large chip is both extremely expensive and technically challenging. Integration at the package level by having multiple smaller dies allows for much lower cost and provides design convenience. The hybrid integration of memory-intensive and multi-core logic processors or multi-logic devices such as ASICs or FPGAs in 3D and 2.5D architectures within the packages, therefore drives the increase of package sizes. Xilinx has demonstrated a 2.5D silicon package which integrated four FPGA modules, each of 7

mm x 12 mm, and the packages size was 25 mm x 31 mm [5]. The recently released game console Sony PS4 utilizes a GPU on interposer with a 512-wide data bus and on-interposer memory, as shown in Figure 1.7.

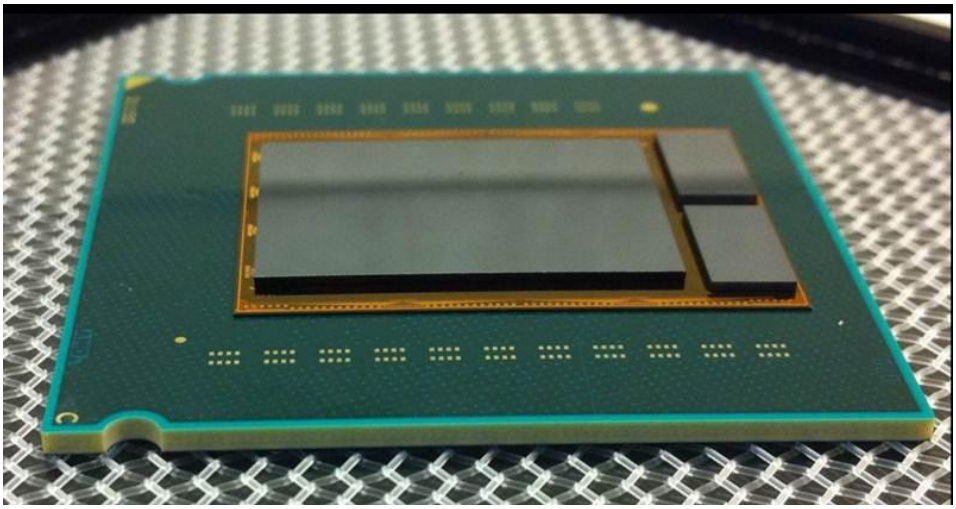


Figure 1.7 Demonstrator of GPU on interposer with on-interposer memories (Courtesy of Global Foundries).

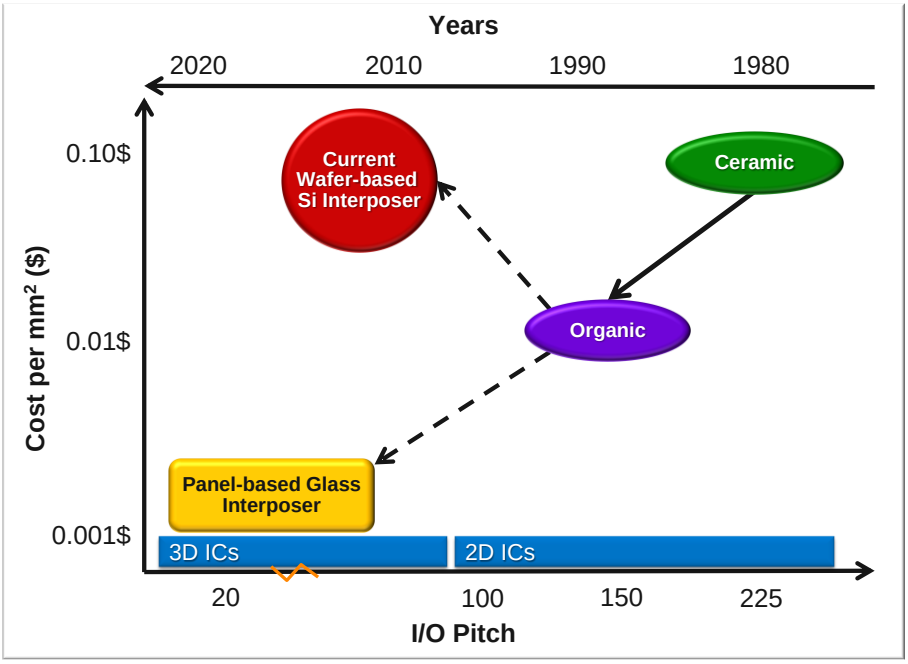


Figure 1.8 Evolution of panel-based low CTE glass interposers for next-generation packages. (Figure Courtesy: Prof. Rao Tummala, GT-PRC).

1.2.2 Drivers for low CTE: (1) first-level interconnection density and (2) reliability of ICs with ultra-low K dielectrics

First-level interconnection density: The demand for high interconnection density on the package requires small interconnection pitch and low stand-off height, which increases the strain in the first-level interconnections. To ensure good interconnection reliability at high density, low pitch and small geometrical dimension, package materials with low CTE which matches the CTE of the die is preferred.

Reliability of ICs with ultra-low K dielectrics: Organic packages have mismatched coefficient of thermal expansion (CTE) with the ICs, which induces high stress in the ultra-low-K on-chip dielectrics, and the warpage of the substrates. The elevated stress, adding on to the poor adhesion and low fracture strength of low-K materials, further causes delamination and fracture of the back end of the line (BEOL) stack [6]. The reliability demand therefore favors packages with lower CTEs.

The need for reduced packaging costs and I/O pitch has, however, led to the replacement of low-CTE ceramic packages with organic packages as illustrated in Figure 1.8, contrary to the need described above. Organic materials are most commonly used for today's packages, as shown in Figure 1.9 (a). They are easily processable and cost efficient. However, organic substrate systems are known to have poor dimensional stability, which limits their miniaturization, as well as through-vias pitch and reliability for high density interconnections. Traditional organic packages also have a high CTE of 15-18 ppm/C. To enable higher interconnection density on the package, new package materials with low CTE and outstanding dimensional stability are required.

A new generation of silicon, glass and low-CTE organic packages are being developed to address these fundamental challenges associated with traditional organic substrates [7] as shown in the left side of Figure 1.. Compared to traditional organic substrates, the novel substrates have excellent dimensional and thermal stabilities,

thereby, enabling ultra-high I/O densities. While their low coefficient of thermal expansion (CTE ~ 3ppm/°C), approaching that of the die helps to reduce the stresses in the chip-package interconnections and in the fragile low-K dielectrics, their CTE being so low compared to printed wiring boards (PWB, CTE~17 ppm/°C) on which they are assembled to form the final system, causes fatigue-related reliability failures for board-level interconnections.

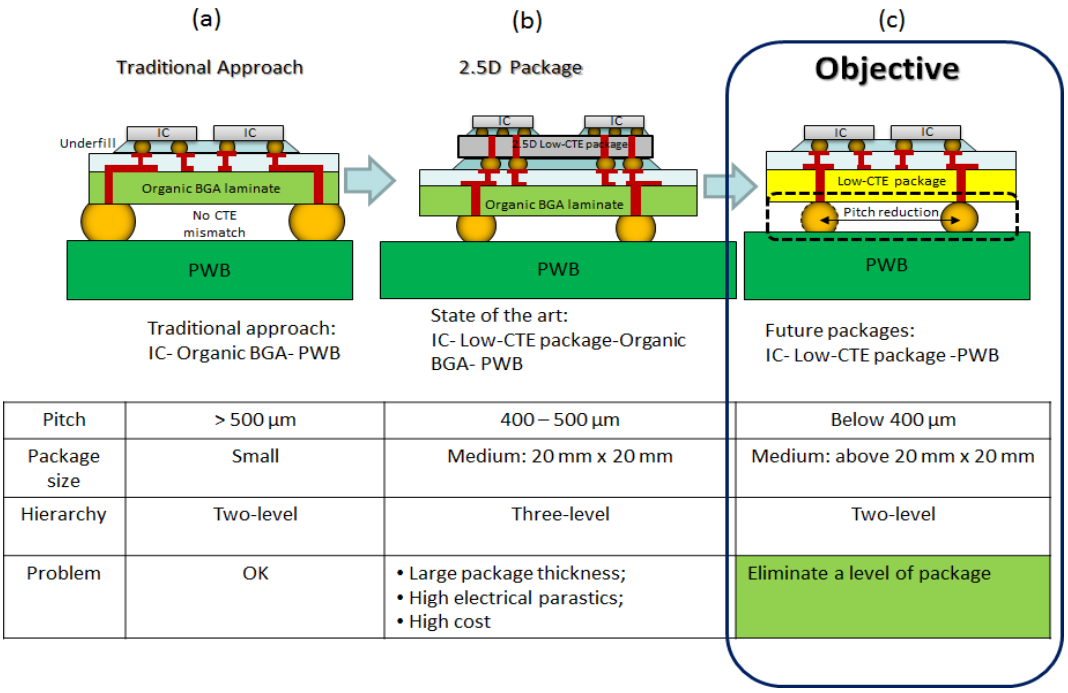
Three types of such low-CTE packages are prevalent in R&D today. Silicon interposers provide high-density through-silicon vias (TSVs) and RDL using back-end-of-the-line (BEOL) processes to interconnect the ICs. Silicon has outstanding dimensional stability, surface smoothness and mature processing techniques to achieve high I/O density. However, the semi-conducting nature of silicon requires insulting liners in the TSVs for electrical isolation, which adds on processing complexity and limits the electrical performance. In addition, there are cost challenges with silicon packages, due to a) the wafer size is limited (200-300mm), which limits the number of large packages that can be yield per wafer, b) The BEOL processes, such as PVD, CVD and RIE, are costly.

Major progress has also been made in the leading-edge organic substrates with low CTE, high modulus and high Tg, which have achieved 12-15 μm line and space, and 120 μm I/O pitch. However, fundamental challenges exist for further miniaturization, including (1) the visco-plastic properties of organic materials limiting the dimensional stability and layer-to-layer registration, and (2) warpage of the package due to thermal processing in critical zones, such as dielectric lamination and curing, and assembly.

As an alternative, Georgia Tech PRC is pioneering glass-based 2.5D and 3D packages for unparalleled miniaturization, performance and cost, beyond today's integration approaches. The glass package consists a) of an ultra-thin substrate, b) made of glass with the ultra-low electrical loss, c) with ultra-short through-package via for double-sided assembly of active and passive components separated by only about 50

microns in interconnect length, d) embedded and surface-assembled ultrathin actives and passives, e) using ultra short, low-temperature and fine-pith Cu-Cu interconnections with high current handling, f) integrated thermal and shielding structures. The 3D glass substrate uses finer-pitch RDL wiring layers and TPVs, compared to the existing ceramic and organic substrates. It reduces the X-Y footprint of the module at least by half, by virtue of double-side mounting, enabled by low-cost and small-pitch through-vias, and by embedding of active and passive devices in high precision cavities, allowing for 3D stacking of multiple ICs and passives. The passives footprint is also reduced by direct deposition of thin-film passives or separately fabricating testable and yieldable ultra-thin glass substrates referred to as 3D IPDs, which are then diced and assembled onto the mother glass substrate. The reduction in thickness of the module, in addition to ultra-thin glass and ultra-thin RDL layers is due to ultra-short device-to-substrate interconnections that are about 10μm tall, compared to the flip-chip solder interconnections that are 100μm. Thermal management of ICs is addressed by incorporating thermal vias in the glass, or direct integration of heat-spreaders on the back of the die.

The current approach to achieve reliable interconnections for these low-CTE packages is to insert an intermediate organic ball-grid-array (BGA) laminate, as shown in Figure 1.9 (b). The additional organic package decouples the stress in the interconnections, at the same time however, increases the thickness of the system, enlarges the electrical parasitics and decreases the performance. The ultimate goal is to eliminate the organic BGA layer, and achieve direct and surface mount technology (SMT) compatible interconnections from the low CTE packages to the PWB, as shown in Figure 1.9 (c).



Pitch	> 500 µm	400 – 500 µm	Below 400 µm
Package size	Small	Medium: 20 mm x 20 mm	Medium: above 20 mm x 20 mm
Hierarchy	Two-level	Three-level	Two-level
Problem	OK	• Large package thickness; • High electrical parastics; • High cost	Eliminate a level of package

Figure 1.9 Industry needs and challenges in board-level interconnections. (a) Traditional approach with organic package. (b) 2.5D low-CTE package with organic intermediate layer. (c) Direct interconnection from low-CTE package to printed wiring board.

Direct assembly of low CTE packages on PWB has so far been accomplished with pin grid array (PGA) packages for high-performance computing applications (Figure 1.10 a). While PGA packages are not assembled by standard SMT processes at small pitch, they have the same fundamental problem, the mismatch-driven reliability. This problem is solved by using high aspect ratio pins to lower the interconnection strain and improve its reliability. Wafer level packaging of ICs for direct assembly on PWB without the need of an intermediate package forms another class of low CTE packages, as shown in Figure 1.10 b. WLPs are made of small silicon ICs and yet assembled on PWBs with acceptable reliability, because they are smaller in sizes, typically less than 7mm, and therefore smaller strains in the interconnections. The redistribution layers, in addition, serve as stress-buffer layers and help improve the reliability of interconnections.

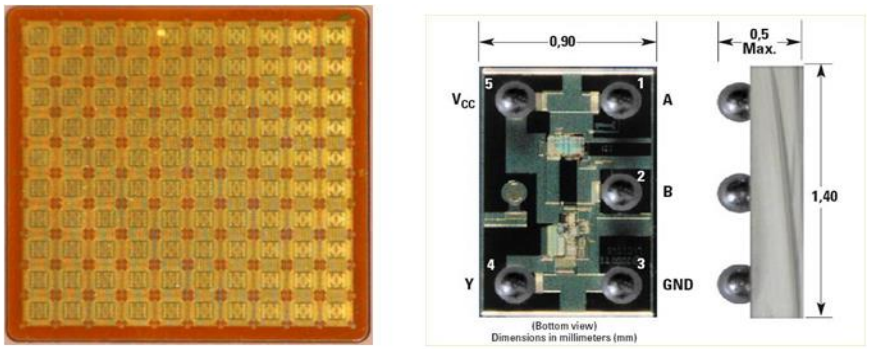


Figure 1.10 : Examples of low-CTE packages: (a) Pin Grid Array (PGA) package (Courtesy of IBM), (b) Wafer-level package (Courtesy of TI).

1.3 Engineering and Scientific challenges in board-level interconnections with large low-CTE packages

Solders are widely used as the interconnections between ICs and packages, as well as between packages and boards. Eutectic tin lead (SnPb) alloy has been the material of choice for SLI because it exhibits good mechanical properties and low-temperature processability. However, there has been a decline in the use of lead because of its toxicity, leading to the investigation of alternative Pb-free materials. Sn-based near eutectic or eutectic alloy systems such as SnAg, SnCu, SnSb, SnZn, SnIn, SnBi and SnAgCu are the primary candidates to replace traditional lead-bearing solders. Among these alloys, SnIn and SnBi have low melting points, but possess inferior mechanical properties. Wojciechowki et al. reported that SnZn does not provide good wettability, and has poor corrosion resistance compared to SnPb [8]. In addition, SnSb is not a good candidate due to the low ductility. Among the remaining candidates - SnCu, SnAg and SnAgCu - SnCu is the most inexpensive alloy available, but has highest melting point and poorest mechanical properties, as reported by Richards et al [9]. SnAg and SnAgCu

have good mechanical properties and solderability, and are the most popular lead-free solder systems.

Lead-free alloy systems, which are invariably Sn-rich, are found to be less ductile and more prone to failures. When used for assembly of low-CTE packages on PWB, the reliability of lead-free solder interconnections becomes even more of a concern due to more aggressive thermo-mechanical loading. Therefore, traditional Pb-free alloys have fundamental limitations in addressing the thermo-mechanical reliability issue under high CTE mismatch.

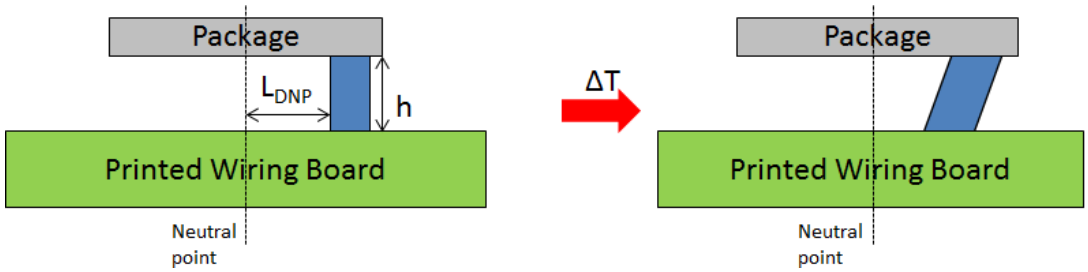


Figure 1.11 Cyclic strain in solder joints induced by component CTE mismatch.

As shown in Figure 1.11, the difference in coefficient of thermal expansion (CTE) between the package (silicon or glass) and the organic printed wiring board induces cyclic thermomechanical loading in the solder joints when the device is in operation. When the system is powered on, the device heats up causing expansion, and when it is powered off, the device cools down causing contraction. The displacement of a solder joint due to temperature change (ΔX) is given by:

$$\Delta X = L_{DNP}(\alpha_{PWB} - \alpha_{pac})\Delta T \tag{1.1}$$

L_{DNP} is the distance to neutral point (DNP), which is the distance from the joint to the center of the package substrate. ΔT is the temperature change during each loading cycle; α_{pac} and α_{PWB} are the CTEs of package and PWB, respectively. Due to the geometrical symmetry, the position of substrate center is not affected by thermal

expansion. Therefore, this geometric center is also referred to as the neutral point. Assuming the height of joint to be h, the shear strain range for the temperature change is:

$$\Delta\gamma = \frac{L_{DNP}(\alpha_{PWB} - \alpha_{pac})\Delta T}{h} \tag{1.2}$$

From Equations (1.1) and (1.2), it can be seen that the cyclic strain induced on the solder joints is determined by the distance to neutral point, the difference in CTE, temperature range and the geometry of the joints.

Emerging packages aggravate the strain in solder joints in three ways. The trend towards low-CTE packages made of silicon, glass and low-CTE organic materials causes large CTE mismatch between the package and the board. The large package size of as much as 50mm in the emerging 2.5D and 3D multi-chip architectures for high-bandwidth applications in high-performance computing, networking and consumer products further increases the strains as seen in Equation (1.2). The third reason from high strains comes from the shrinking board level interconnection pitch, which is projected to reach below 300 μm, requires lower stand-off height and interconnections and adds other reliability challenge. These three factors - the CTE mismatch at package-to-board level, large interposer size, and shrinking interposer-board interconnection pitch - create large thermo-mechanical strain in the board-level interconnections.

Current packages utilize solder ball arrays to provide electrical connections between the package and PWB, and also provide mechanical support. Eutectic SnAg and SnAgCu are the most common solders in use today. The plastic strain range in each thermal cycle is related the fatigue life of the solders by Coffin-Manson relationship:

$$N_f = 0.5\left(\frac{2\varepsilon_f}{\Delta\gamma_P}\right)^{\frac{1}{c}} \tag{1.3}$$

where N_f is the number of cycles to failure, $\Delta\gamma_P$ is the cyclic plastic strain range, ε_f and c are material-related constants [10]. Therefore, the fatigue performance deteriorates

with larger plastic strain. For a given package, the solder at the corner has the maximum DNP, and is most likely to fail. Figure 1.12 shows the fatigue life of SnAgCu solder as a function of plastic strain in each thermal cycle. For traditional organic BGAs, the plastic strain per cycle in the solder is about 0.85%, which corresponds to 1000 cycles of fatigue life. However, with the application of large low-CTE packages and small interconnection pitches, the strain is anticipated to reach 1.5%. With close to 2X increase in the plastic strain, the projected fatigue life is below 500 cycles, far below the reliability requirement of the electronic systems.

This board-level interconnection reliability has been identified as a grand challenge by the semiconductor and electronics industry because it creates several bottlenecks for advances in ultra- high I/O 2.5D and 3D packages and systems.

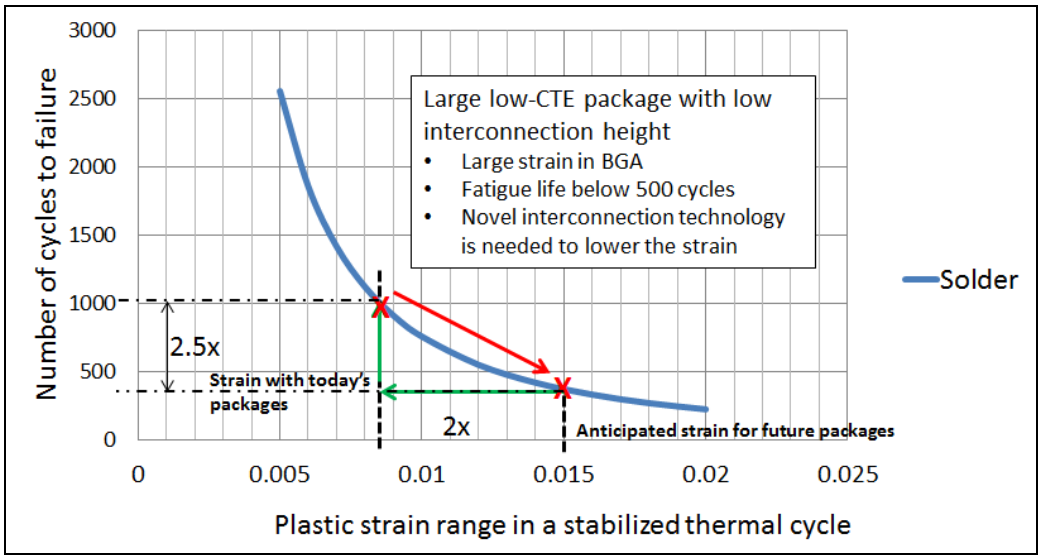


Figure 1.12 Fatigue life of SnAgCu solder versus the plastic strain range in each thermal cycle.

1.4 Objectives and approach

The engineering objective of this research is to explore and demonstrate highly-reliable, SMT-compatible interconnections between large low CTE packages and organic

boards. The specific objectives are benchmarked with prior art in terms of package size, pitch and height, as shown in Table 1-1.

Achieving the above engineering objectives requires addressing fundamental scientific challenges arising from the large strains in the solder-based interconnections as a result of large CTE mismatch, large interposer size and small pitch. A systematic and fundamental approach was undertaken, involving modeling, design, fabrication, and validation by model-to-hardware correlation.

Table 1-1. Specific objectives of the study.

Performance Metrics	**Prior Art**	**Objectives**
Package size for SMT	7mm × 7mm (WLP)	20 mm × 20mm and above
Scalability to small pitch	500-800 μm	400 μm and below
Interconnection height	250 μm	150 μm and below
Manufacturability	PGA for large package size	SMT-compatible

A novel interconnection technology using compliant copper microwire arrays (MWA) is proposed to address the reliability issue of lead-free solder joints, as shown in Figure 1.13. The MWA comprises of high aspect ratio copper pillars with inherent compliance that can accommodate the differential expansion between the package and the board, and therefore reduce the plastic-strain induced damage, both in the copper and solder joints during thermal cycling.

The proposed research, for the first time, explores micro-scale copper wires with high aspect ratio to address the reliability challenge of the board-level interconnections. The interconnection technology is SMT-compatible, scalable to small interconnection pitch, and can accommodate large low-CTE packages. It can be fabricated separately, which introduces minimum interruptions to the fabrication of package and the board.

Finite element modeling with ANSYS will be used to optimize the geometrical and material parameters of the copper microwire arrays to achieve lowest plastic strains in the copper wires and solder. Parametric study will be carried out to understand the effect of each geometrical and material parameter on the reliability performance of the interconnection. Coffin-Manson relationship will then be used to calculate the projected fatigue life of the interconnection.

Based on the modeling result, a packaging-compatible and cost-efficient fabrication process will be designed. The silicon package, microwire array interconnection, and printed wiring board will then be fabricated to demonstrate the feasibility of the proposed technology. An SMT-compatible assembly approach will be presented for wider industry adoption. The reliability of the interconnection will be tested by accelerated thermal cycling, to prove the effectiveness of the MWA interconnection, and validate the models.

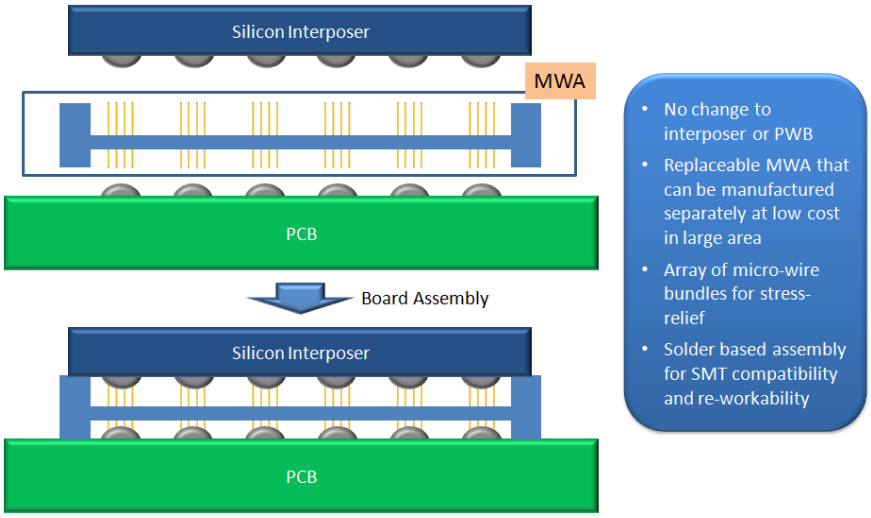


Figure 1.13 Schematic of copper microwire array interconnections.

CHAPTER 2

LITERATURE REVIEW

This chapter begins with an overview of state-of-the-art board-level interconnections, and then reviews two major innovations in interconnection materials and structures that are being pursued in order to address the reliability challenges with emerging large low-CTE packages on high-CTE boards. The first approach focuses on the ball grid array (BGA) interconnections, and is aimed at enhancing solder materials and solder-pad interfaces to increase their strength and fatigue resistance. The second approach deals with novel interconnection structures that provide stress-relief and, therefore, lower the effective strain-induced damage to improve their reliability. Copper is emerging as a strategic interconnection materials for providing stress-relief in board-level interconnections. The last section, therefore, reviews the recent findings in electrochemical processing - microstructure - mechanical property relations in fine-grained copper.

2.1 Current technologies in manufacturing for board-level interconnections

Three major categories of interconnection technologies are used for board-level assembly. The first one is a pin grid array (PGA) package, which utilizes high aspect ratio metal pins for reliable board level assembly, and has been widely used in manufacturing by IBM [11], to connect very large glass-ceramic LTCC ceramic modules of same CTE as silicon to the system board. As shown in Figure 2.1, the high aspect ratio pins accommodate the large CTE mismatch between the large low-CTE packages and the

boards. However, the interconnection pitch of PGAs has not scaled much below 1mm, which limits their application in today's high-end electronic systems.

The second type is BGA interconnections, which uses an array of solder balls to connect the package onto the board, as shown in Figure 2.2. BGAs have been vastly successful, due to their scalability to low interconnections pitches, compatibility with surface mount technologies, outstanding electrical performance and low cost. However, as discussed in Chapter 1, the low fatigue resistance of solder alloys has become the bottleneck for the application of advanced low CTE packages. Major innovations in solder materials have been made to improve the interconnection reliability, and will be discussed in more detail in Section 1.2 of this chapter.

BGAs are formed on the backside of the package substrate with the chips mounted on the topside with flipchip or wirebonding. However, board-level interconnections are also formed directly at wafer level to achieve small system size and low cost. The dies are attached directly onto the board with flipchip technology. The wafer-level packaging process is demonstrated in Figure 2.3. Due to the CTE mismatch between the die and the board, only small die sizes (up to 5mm) have been demonstrated. R&D efforts targeting on improving the reliability of WLP are discussed in Section 1.3 of this chapter.

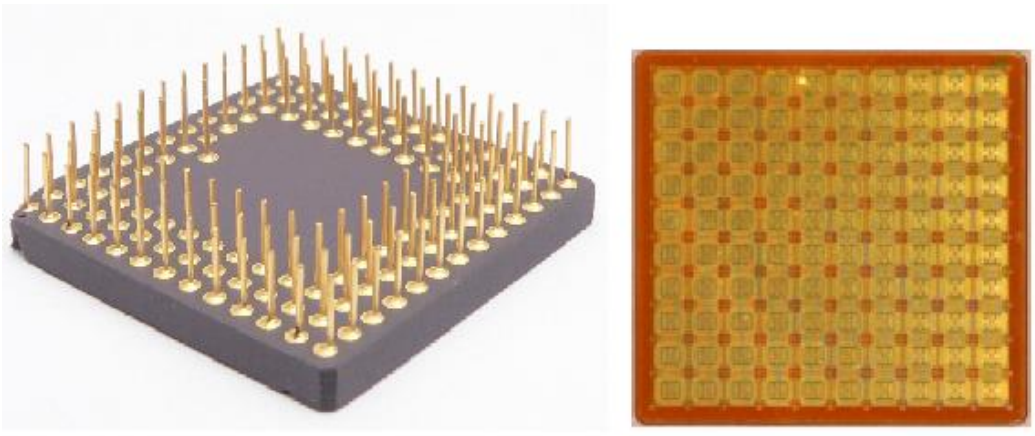


Figure 2.1 Pin grid array in high-performance computing applications for large low-CTE package to board interconnections [11].

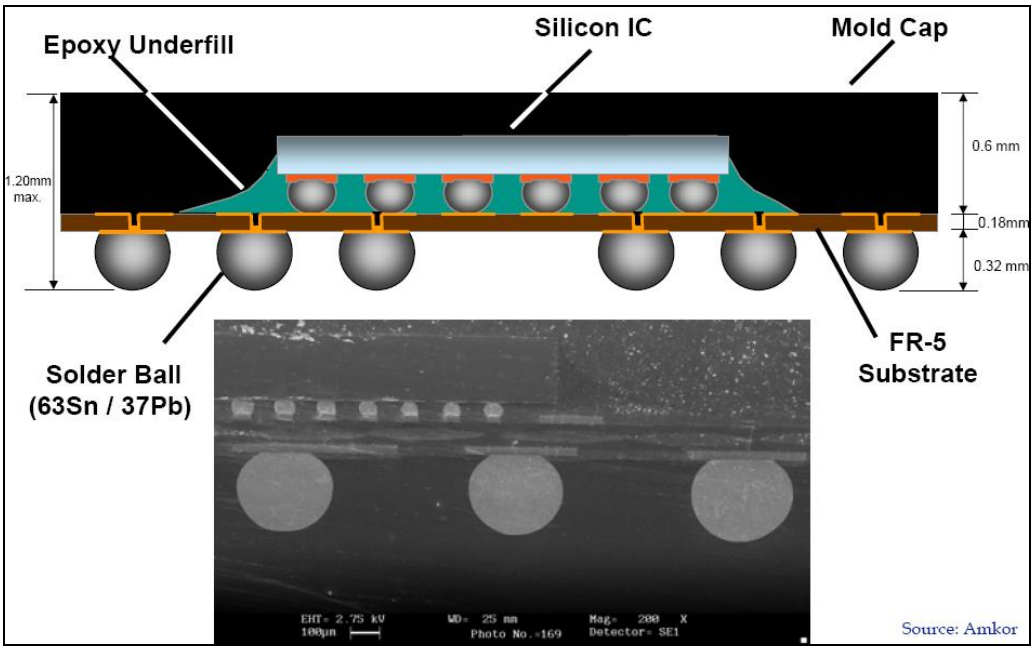


Figure 2.2 Board level interconnections with ball grid array (Courtesy of Amkor).

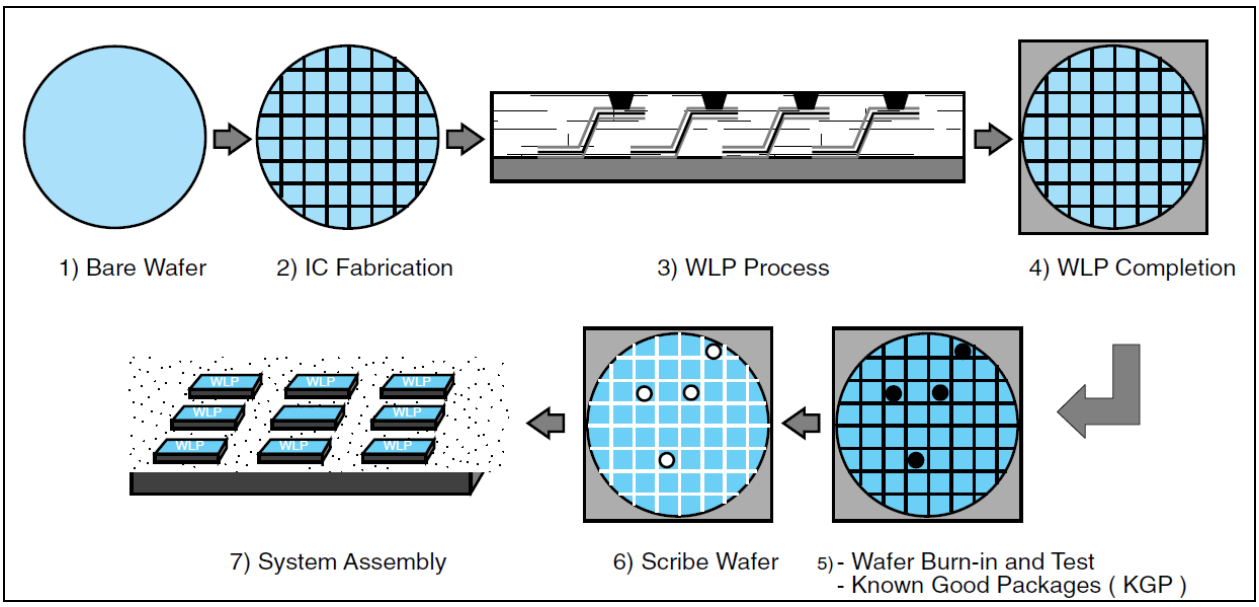


Figure 2.3 Wafer-level packaging process (Courtesy of IFC, Georgia Tech).

2.2 Recent advances with solder interconnections

Solders are the dominant materials used for board-level interconnections. These interconnections consist of solders that comprise the bulk of the interconnections, and solder-pad interfaces that are predominantly intermetallics. Both have distinct microstructures and mechanical properties, which play critical roles in the reliability of

solder interconnections as illustrated in Figure 2.4. This section comprehensively reviews the formation of the metallurgical joints, the relationship between the solder microstructure and fatigue properties, the key advances in solders with composition and microstructural control to improve their mechanical properties, and pad surface finish with advanced diffusion barriers to form controlled intermetallics.

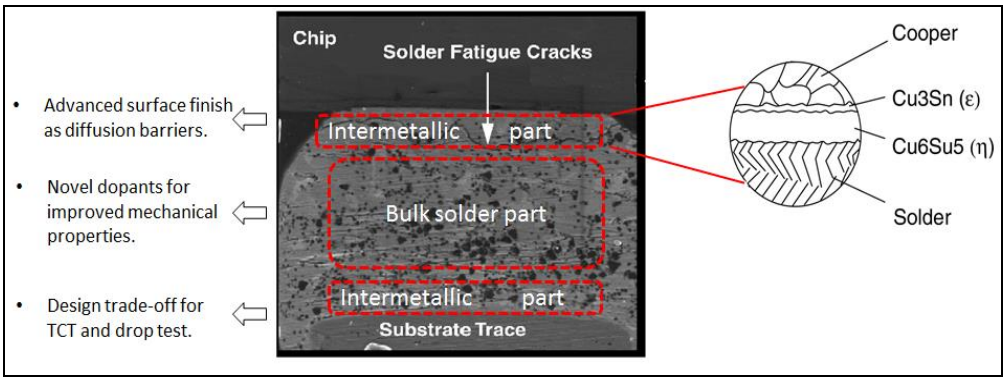


Figure 2.4 Material innovations in solder and base metals.

2.2.1 Metallurgical joint formation with solder alloys

Metallurgical joints are formed between solder alloy and the metallic surfaces on the package and the board. The copper pad on both the package and the board typically has a thin nickel and gold layer on top of it as surface finish, to provide a suitable surface for soldering. Initially, the solder balls are placed on the copper pad of the package, and then heated above solder liquidus to form a metallurgical bond via a process called reflow. During reflow process, the solder alloy undergoes melting, and the molten solder wets the copper pad. While wetting, the melt dissolves the protective gold layer and also a portion of the underlying nickel up to the solubility limits, thereby forming intermetallic compounds (IMCs) of Ni-Sn and Au-Sn. Nickel provides a flat and uniform surface and also acts as a diffusion barrier between solder and copper, to prevent excess growth and Cu-Sn intermetallic compounds (IMCs) [12]. Gold is used to protect the surface from oxidation, and also enhance the wettability. The package is then assembled onto the PWB

via a similar reflow process during which the bonding between solder and PWB pad is formed.

Wetting is crucial for joint formation. It involves melting, followed by spreading of the melt across the surface to be joined. During spreading, the solder will dissolve base metals from the wetted surfaces and form intermetallic compounds to achieve a proper metallurgical bond. Wetting characteristics are largely dependent on surface energy of the interfaces. The critical surfaces can be defined as: 1- soldering atmosphere; 2- the molten solder; and 3- the substrate. At equilibrium, the contact angle θ, as shown in Figure 2.5, can be described by the following equation:

$$\gamma_{13} = \gamma_{12} \cos\theta + \gamma_{23} \tag{2.1}$$

where γ_{ij} represents the surface energy of annotated interfaces. A lower contact angle is favored for sufficient wetting and joint formation. Pb-free solders normally have deteriorated wetting behavior compared to traditional SnPb solders. Bukat et al. [13] compared the wetting behavior of various SnAgCu alloys and SnAg near-eutectics, presented in Table 2-1.

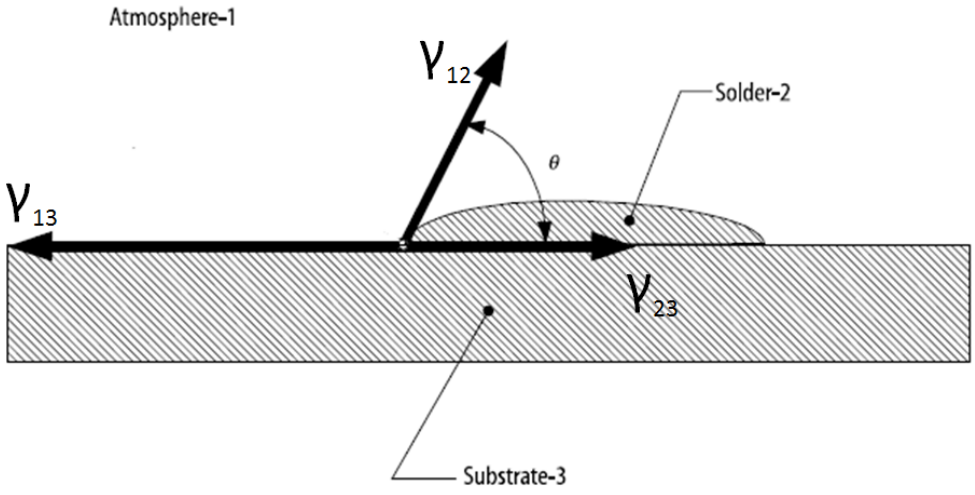


Figure 2.5 Equilibrium of surface tension at contact angle θ.

Table 2-1 Wetting data for SnAgCu alloys at 250°C on Cu substrates.

Alloy	Melting point (°C)	Surface tension (mN/m)	Wetting force (mN/m)	Wetting time (s)	Wetting angle (θ°)
96.5 Sn3.5Ag	221	445	50	1.5	70
96.5Sn3.0Ag0.5Cu	217-219	450	110	1.3	55
95.7Sn3.6Ag0.7Cu	217-218	463	110	1.2	55
95.5Sn4.0Ag0.5Cu	217-219	460	120	1.2	55

2.2.2 Evolution of solder microstructure and thermo-mechanical fatigue failures

Most of the Pb-free alloys studied are Sn-rich, and alloyed with elements such as Ag, Cu, Zn, Bi, In and Sb. Due to the high Sn content and generally low solid solubilities of most elements in solid Sn, the dominant phase in most Sn-base solder joints is body centered tetragonal Sn, or β-Sn [14]. The Sn phase may be present in several morphologies simultaneously, ranging from β-Sn dendrites to eutectic microstructures.

Yu et al. [15] showed that the microstructures of Sn–2.5Ag–0.7Cu, Sn–3.5Ag–0.7Cu alloys have coarse β-Sn grains. As seen in Figure 2.6 (a) and (b), the light regions are the β-Sn grains with an average size of 20–30μm in Sn–2.5Ag–0.7Cu while they are slightly smaller (15–25μm) in Sn–3.5Ag–0.7Cu alloy. The dark eutectic regions consist of Ag_3Sn, Cu_6Sn_5 and Sn matrix with the width of about 10μm in both the alloys. As shown in Figure 2.7 (a), the size of Ag_3Sn and $Cu6Sn_5$ intermetallic particles in Sn-2.5%Ag-0.7%Cu are about 1μm. With the increase in Ag content, the intermetallics become coarser, about 2–4μm in Sn-3.5%Ag-0.7%Cu as shown in Figure 2.7 (b).

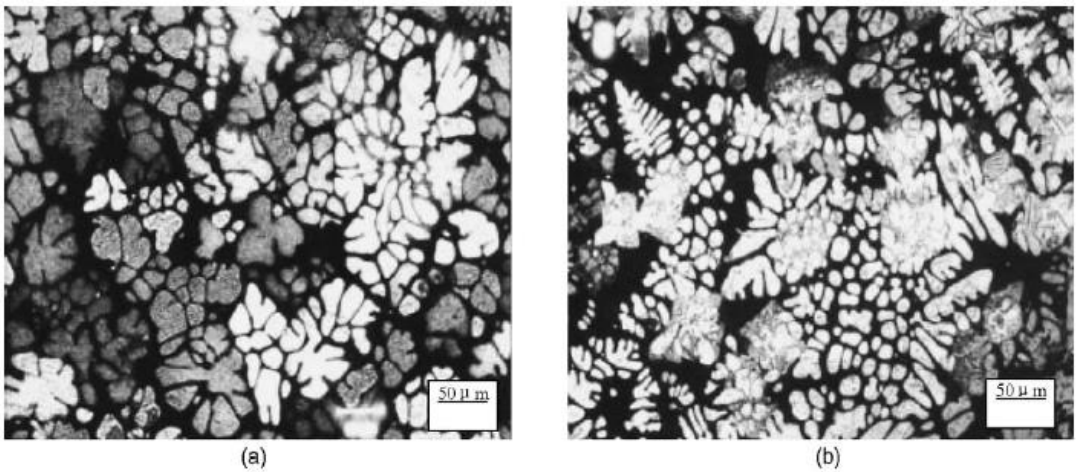


Figure 2.6 Optical microscopic images of (a) Sn-2.5%Ag-0.7%Cu, and (b) Sn-3.5%Ag-0.7%Cu (Courtesy of D.Q. Yu).

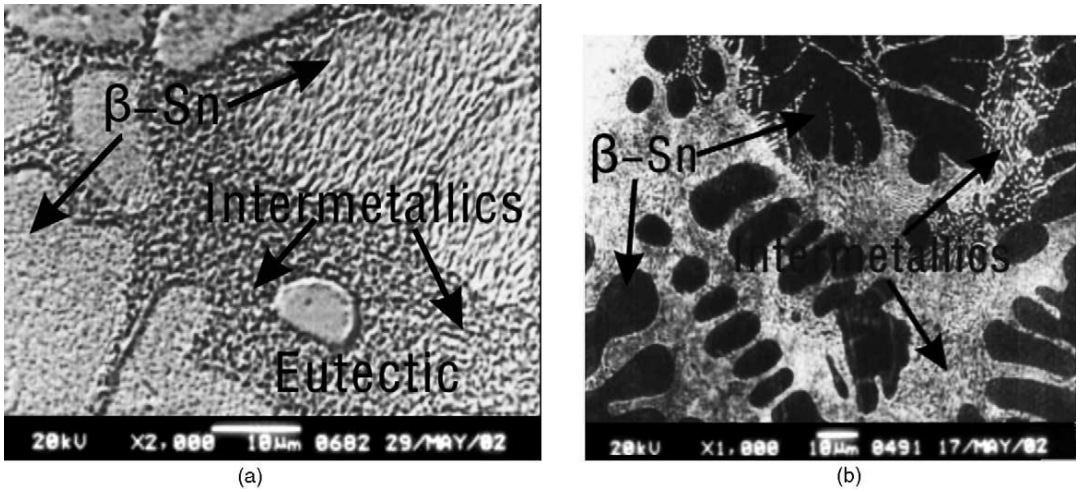


Figure 2.7 SEM images for (a) Sn-2.5%Ag-0.7%Cu, and (b) Sn-3.5%Ag-0.7%Cu (Courtesy of D.Q. Yu).

The as-reflowed microstructure of Pb-free solder alloy is not stable under normal operational conditions. Significant coarsening takes place over time after assembly. Within the solder joints, the interface spacing between the constituents of microstructure increases and the intermetallic particles, or secondary phases within the Sn matrix increase in size. The major driving forces for the evolution of microstructures are high operating temperature and cyclic shear stress.

The first driving force for microstructure coarsening is the high homologous temperature. The homologous temperature T_h, is defined as the ratio of the operating temperature, T, to the melting temperature, T_m,

$$T_h = \frac{T}{T_m} \tag{2.2}$$

Solder alloys are chosen to have low melting temperatures such that the joining process is compatible with other materials and processes used for semiconductor fabrication. Therefore, they are usually subjected to high homologous temperatures, exceeding 0.3-0.5 in operation. High temperature promotes diffusion; therefore diffusion-driven processes such as grain boundary diffusion and interface-boundary diffusion become more active. These processes drive thermal coarsening of solders, resulting in the growth of secondary-phase particles in the primary matrix, and morphological changes across the bulk microstructure.

The second driving force for coarsening is the mechanical loading. Cyclic mechanical loading induces strain energy, which, in turn, promotes boundary migration. The movement of boundaries increases the overall size of the grain, which is favored by strain energy reduction. Dutta et al. [16] investigated the combined effects of temperature-and strain-induced coarsening in 93.6Sn4.7Ag1.7Cu. In this study, an increase in intermetallic particle size and spacing was observed after the solder joints were cycled from -25°C to 125°C. As can be seen from Figure 2.8 (a)-(c), the average particle size of Ag_3Sn intermetallics increased from about 0.3μm to about 2μm after 1200 cycles, and the spherical particles grew into platelets.

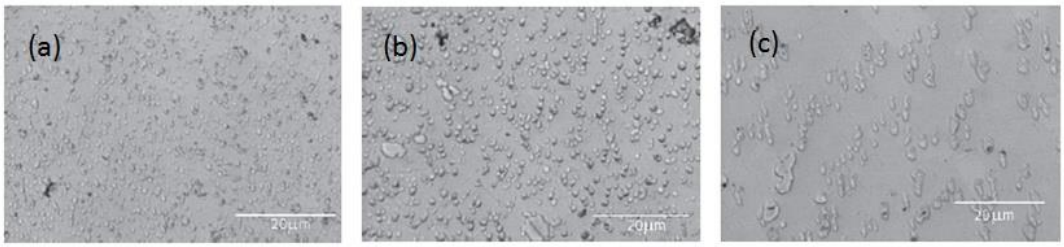


Figure 2.8 Microstructure of Ag_3Sn particles in SnAgCu (a) as-reflowed condition, (b) after 200 thermal cycles, and (c) after 1200 thermal cycles [16].

The change in microstructure has a significant influence on the mechanical properties of the joints. The yield strength becomes lower as coarsening takes place, as predicted by Hall-Petch equation:

$$\sigma_y = \sigma_0 + kD^{-1/2} \tag{2.3}$$

where σ_y is the yield strength, k is a constant and D is the mean grain diameter. As the applied stress goes beyond the yield stress, dislocation motion is onset, and plastic deformation occurs. More importantly, the grain size also affects the fatigue behavior of solder alloys under cyclic loading. Hall et al. showed that fine-grained solder joints exhibit fatigue lives larger than coarse-grained solder joints in accelerated tests [17]. Small grains tend to distribute the load evenly over the specimen and enhance both the strength and ductility. Fine intermetallic precipitates hinder dislocation motion, which strengthens the material as well as improves creep resistance.

2.2.3 Advances in solders with microstructure and composition control

Recently, development of new solder materials has been reported by alloying of grain-refining elements into Sn-Ag and Sn-Cu-Ag systems to achieve better mechanical properties. Wu et al. reported that the doping of rare earth elements refined the size of grains and intermetallic particles, and improved the tensile strength and creep resistance of lead-free solders [18]. Aggarwal et al. showed improved solder properties shear strength of solders by adding organic derived nano reinforcements with appropriate

functional groups, which promoted bonding with the metallic matrix and helped pin the grain boundaries and constrain the grain boundary sliding [19].

The fatigue resistance of bulk solders is mathematically described using Coffin-Manson relationship as discussed in Chapter 1. Improved fatigue resistance is needed to meet the reliability targets with the high plastic strains seen with large low CTE packages. Lead-free solders have better fatigue resistance compared to lead-tin solders at lower strain ranges, and higher strength. Lead-free solders are also known to have a higher creep resistance compared to PbSn solders. The higher strength and creep resistance, however, comes at the expense of ductility. At higher strains, SAC cannot readily accommodate deformations and become more susceptible to crack propagation than ductile PbSn.

Strengthening and toughening agents are investigated to further increase the fatigue, creep and fracture resistance of Pb-free solders. Precipitation of particles along interfaces can significantly reduce grain boundary sliding. Ag_3Sn platelets in tin are known to increase creep resistance by the same mechanism. However, as discussed previously, Ag_3Sn platelets coarsen significantly during thermal cycles. The large Ag_3Sn platelets, when formed nearby the solder-substrate interface, facilitate the propagation of fatigue cracks and deteriorate the reliability of solder interconnections. Liu et al. studied the effect of manganese doping in SAC solder [20]. They reported manganese-containing particles near the IMC layer, which enhanced the bonding strength between the IMC and the substrate, and therefore helped improve the fracture resistance along the interface, as shown in Figure 2.9. Pandher et al. demonstrated the benefits of bismuth doping in SAC solders [21]. As shown in Figure 2.10, Bi doping refines the grain structures in SAC alloys and is expected to improve the thermomechanical reliability of the SAC solder.

Reliable interconnections demand both thermal cycling test (TCT) and drop-test performance. However, TCT and drop-test have conflicting requirements for solders.

Terashima et al. showed that the SnAgCu solders with higher silver content (3%-4%) had better TCT performance [22]. They had finer Sn grains, due to the dispersion of Ag_3Sn intermetallic particles, which hinders the microstructure coarsening and improves the strength of the solder. On the other hand, Lee et al. reported better drop-test performance with low silver content [23]. The solders with lower silver content (1%) had less Ag_3Sn particles and thus softer bulk solder, which absorbs shock better and conveys less shock-induced strain at the interfacial stress concentration locations. Therefore it is challenging to select a solder which fulfills both the requirement for TCT and for drop-test.

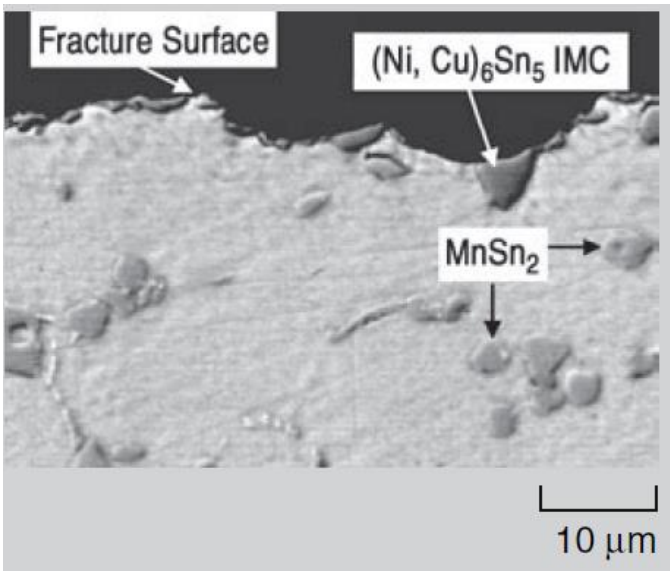


Figure 2.9 Cross section of a SAC105+0.25 Mn solder joint [20].

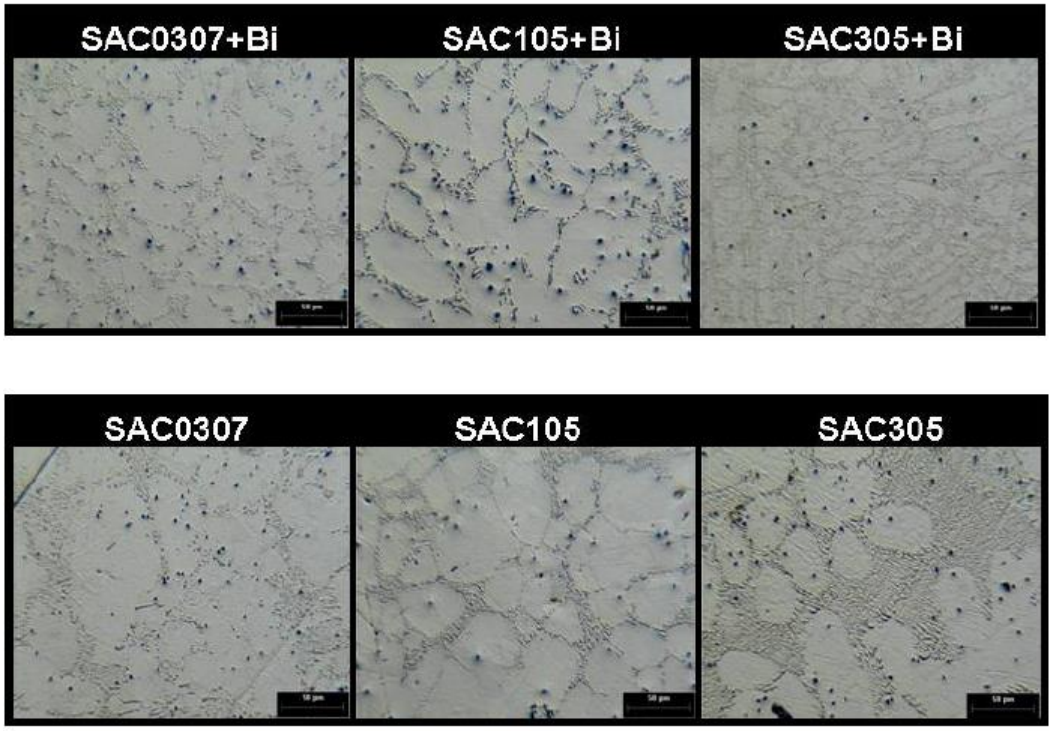


Figure 2.10 Effect of Bi addition on the microsturcture of SAC alloys [21].

2.2.4 Advances in pad surface finish

Surface finish plays a crucial role in improving solderability and reliability of the joints. Some of the traditional coatings used on copper pads include hot air solder leveling (HASL) and organic solderability preservative (OSP). HASL has low cost, but has poor thickness control, and involves lead which is not preferred because of environmental considerations. OSP has been demonstrated as an alternative with good reliability. However, it does not withstand multiple reflows. Plated metal coatings have become more popular because of their good reliability, and compatibility with the requirement for small lines and spaces.

Two of the most popular surface finish technologies with plated metal used for packaging are ENIG (Electroless Nickel Immersion Gold) and ENEPIG (Electroless Nickel Electroless Palladium Immersion Gold).

In the ENIG system, the gold layer is very thin (below 0.2μm), and dissolves readily in solder during the assembly process. Therefore the nickel dominates the interface reactions. As shown in Figure 2.4, a layer of IMC is formed during reflow. The IMC layer primarily consists of Cu-Sn intermetallic species (Cu_6Sn_5 and Cu_3Sn), and it also contains Ni-Sn and Au-Sn due to the surface finish applied on top of the copper pad. The IMC layer serves as the bonding interface material, however, thick IMC layers have been found to be deleterious to the reliability of the interconnections. The thickness of the IMC layers depends on the reflow time and temperature [24], and longer reflow time and higher reflow temperature leads to thicker IMC layers. Tu et al. showed that the lifetime of solder joints degrades rapidly with the increase of IMC thickness, and the fatigue failure occurs mainly at the IMC/solder interfaces [25]. As shown in Figure 2.11, the crack initiated at the solder-IMC interface and propagated through the solder joints [26]. Despite the widespread implementation of ENIG, there are evidences that the ENIG finish may cause catastrophic, brittle, interfacial joint fractures [27][28]. The fracture mode is characterized as brittle nickel-gold interfacial fracture. One of the causes for the brittle interface is the high phosphorous (P) content (10-15%) of the electroless Ni, which leads to interfacial P segregation and promotes a brittle fracture [29].

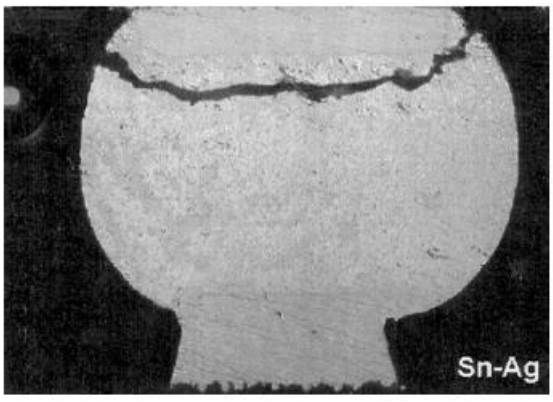


Figure 2.11 Crack at IMC/solder interface with ENIG surface finish.

The ENEPIG system, on the other hand, adds a palladium (Pd) layer in between the Ni and the Au. The Pd layer controls the diffusion of Ni into the solder, and restricts the growth of IMC thickness. Ha et al. reported that the IMC layer formed on ENEPIG pads grows slower than that formed on ENIG pads in thermal aging, and the joints with ENEPIG surface finish had better reliability in both thermal cycling and drop test, as shown in Figure 2.12 [30].

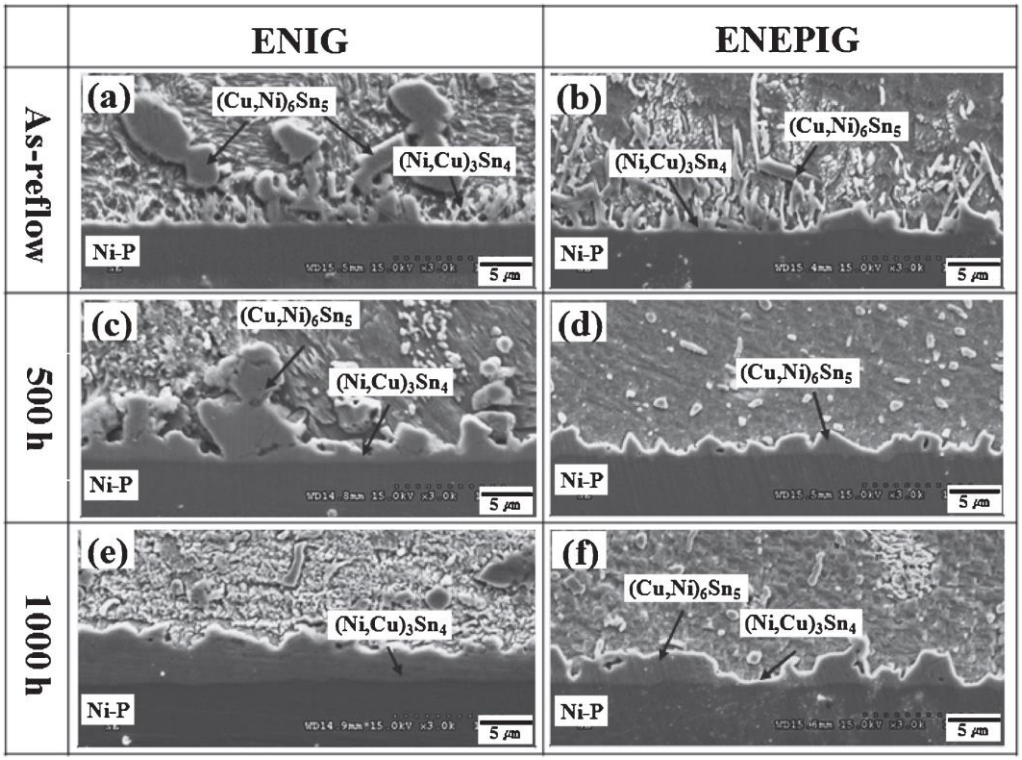


Figure 2.12 Cross section of solder joints after reflow and thermal aging: ENIG (a), (c), (e) and ENEPIG (b), (d), (f) [30].

2.3 Compliant interconnections with improved fatigue resistance

In spite of the various innovations in the solder materials, only incremental improvements in solder joint fatigue resistance have been achieved. An alternative strategy that further alleviates the stresses and strains in the solders is hence widely investigated by industry and academia. These approaches have been primarily developed for large ceramic BGAs or wafer-level packages. The stress-relief (or strain-relief) is

achieved by providing compliant or mechanically flexible structures that are easily deformable, and therefore induce minimal plastic strains in the solder or copper interconnections. These are broadly classified as metal-based compliant structures or polymer-based compliant structures, or a combination of both.

2.3.1 Compliant metal structures for reliable interconnections

2.3.1.1 Copper posts with plated solder cap

Copper post with solder cap is one of the popular metal-based interconnection techniques which utilize both the fatigue resistance of copper, and the assembly convenience of solders. The copper posts can be achieved by electroplating through photoresist patterns, and are compatible with fine-pitch features, therefore they are widely adopted for first-level interconnections and wafer-level interconnections.

T. Wang et al. reported first-level interconnections from a 10 mm × 10 mm IC to organic substrate with copper base and plated solder bump [31]. The interconnections are at 200μm pitch with an overall height of about 105 μm, as shown in Figure 2.13. The assembly was underfilled for improved reliability. The interconnections survived 1000 cycles in accelerated thermal cycling test from -40°C to 125°C.

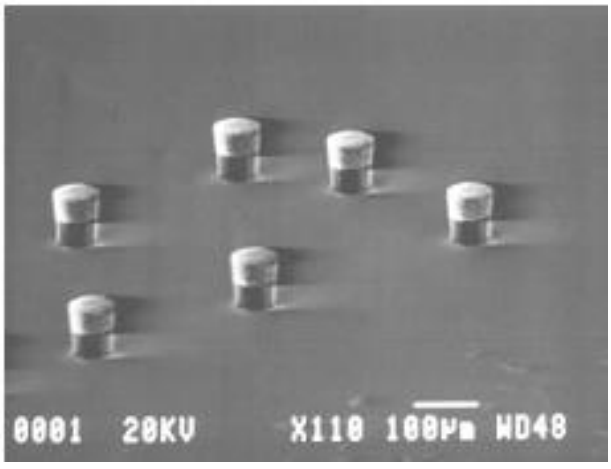


Figure 2.13 Copper base with solder bump for first level interconnection [31].

V. S. Rao et al. explored the copper-solder interconnection for even smaller pitch [32]. In their study, a 10 mm × 10 mm silicon chip was connected to organic substrate with copper pillars with aspect ratio of 3, without using underfills. The pillar height was 68 µm and the pitch was 100 µm. Initial failure was identified between 500-600 cycles in accelerated test.

Similar concept was also adopted by Fujitsu in wafer level chip scale packaging (WLCSP) [33]. The copper posts were embedded in an encapsulation, with solder cap plated on top, as shown in Figure 2.14. The interconnections are at the pitch of 700 µm, and are shown to survive 500 cycles before the first fatigue failure.

From the above three examples, it can be observed that the copper pillar or copper bump based interconnections are still relatively stiff, and are subject to early failures without underfill.

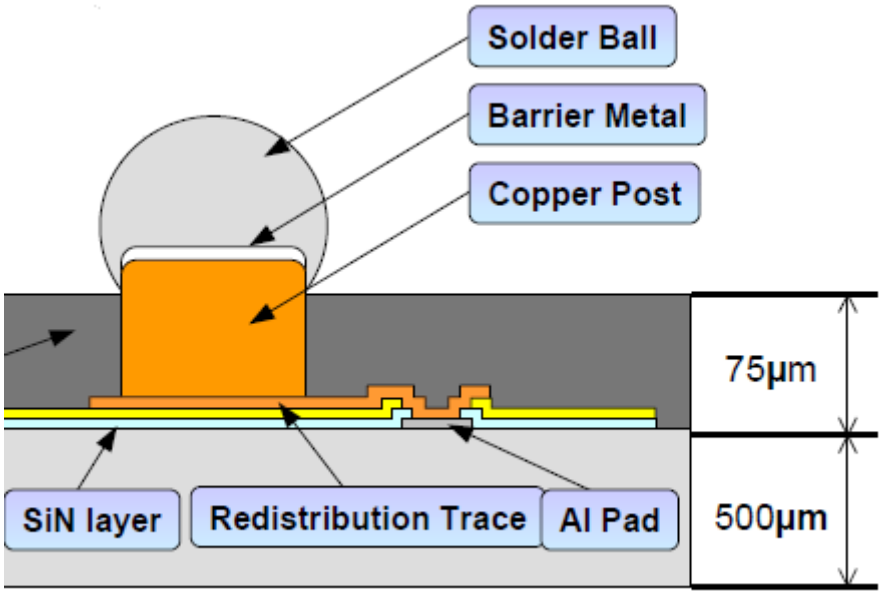


Figure 2.14 Super CSP by Fujitsu [33].

2.3.1.2 Compliant metal springs or leads

To achieve higher compliance and reliability, metal springs or leads with various geometries have been explored. George Lo et al. reported ‘G-Helix’ structure for silicon die to organic substrate interconnections [34]. As shown in Figure 2.15, a copper arch structure was used to provide helical compliance.

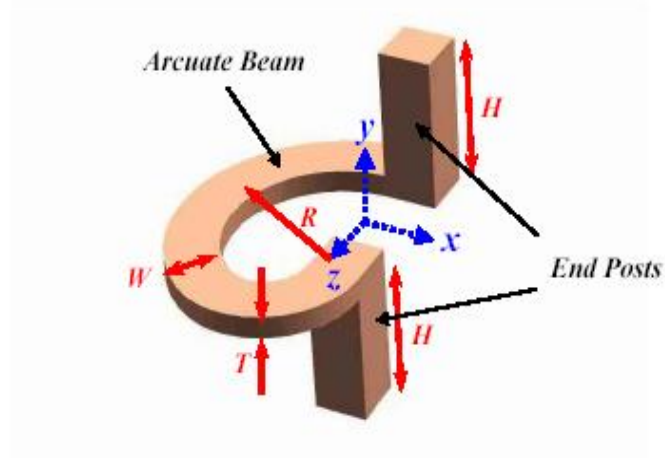


Figure 2.15 G-Helix Interconnections [34].

Tessera demonstrated IC-to-package interconnections with compliant copper lead, as shown in Figure 2.16 [35]. The compliant copper leads were embedded in a compliant polymer layer, which connected with the solder ball for assembly. Such packages passed more than 1500 cycles during accelerated thermal cycle tests at 600 μm pitch. The initial failures were identified in the copper lead, rather than in the solder. The microspring concept has also been adopted by FormFactor, as shown in Figure 2.17 [36]. The gold springs were achieved by wirebonding technique, and provided both in-plane and out-of-plane compliance. The metal springs can also be achieved by releasing sputtered thin metal films with the aid of their intrinsic stress gradient, as demonstrated in Figure 2.18. The microsprings can be assembled using the self-alignment between the pits on the die and the spacer balls on the substrate, the connections are therefore in contact mode,

without metallurgical bonding. The wavy metal lead structures, however, share common challenges with electrical performance, due to their large parasitics.

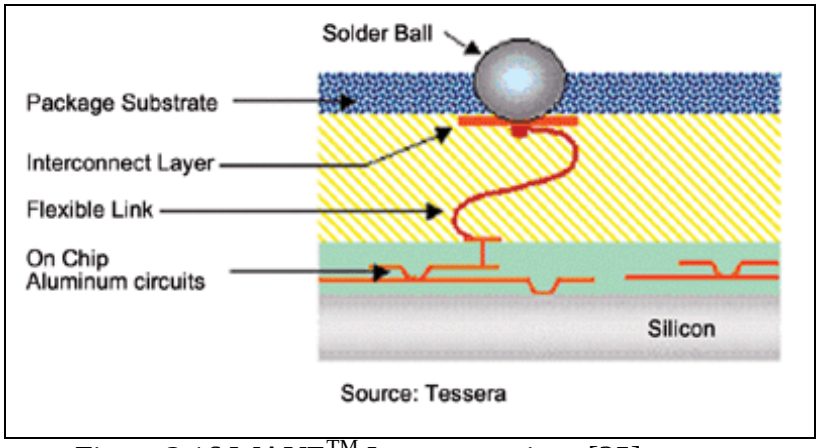


Figure 2.16 WAVE^{TM} Interconnections [35].

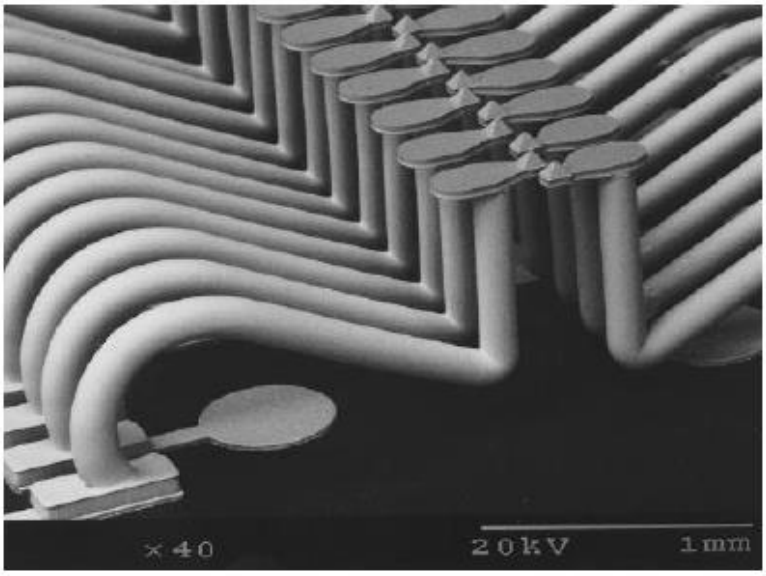


Figure 2.17 Microspring on silicon technology (MOST^{TM}) by FormFactor [36].

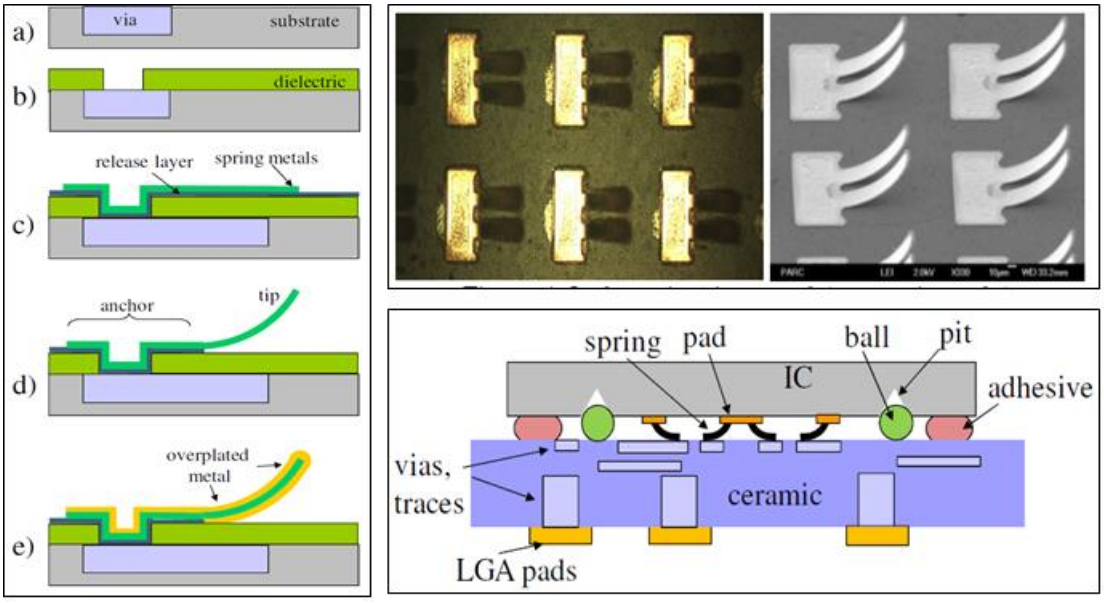


Figure 2.18 Au-MoCr-Au microspring fabrication and assembly [37].

2.3.2 Low-modulus stress buffers for stress-relief

The second category of compliant interconnection technologies mainly uses low-modulus stress buffers, such as air gaps and polymer dielectrics. The deformation of the stress buffers accommodates the CTE mismatch and reduces the stress and strain in the interconnections.

Bakir et al. demonstrated chip-to-substrate interconnection at 100 µm pitch with embedded airgaps, as shown in Figure 2.19 [38]. The metal leads were deposited on a sacrificial polymer layer, which was thermally decomposed into air gaps. Similar under-bump stress buffer can also be achieved by polymer materials. Dudek et al. demonstrated silicone bumps with patterned metal wirings for wafer-level packaging [39]. The polymer redistribution layer, when designed with the right thermo-mechanical properties, can also benefit the reliability of the interconnections. John et al. studied wafer level packages with solder bumps for a small die (4.5 mm), where the reliability of the bumps was enhanced with polymer redistribution layers. The packages demonstrated good thermal-mechanical reliability, as shown in Figure 2.20 [40].

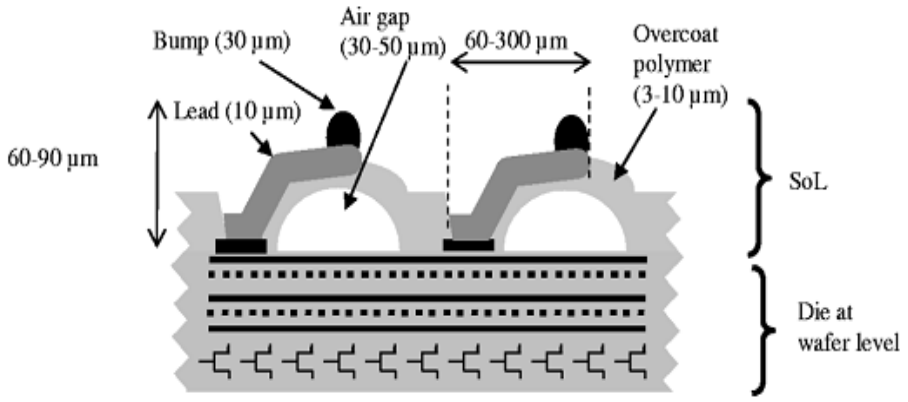


Figure 2.19 Sea of leads interconnections [38].

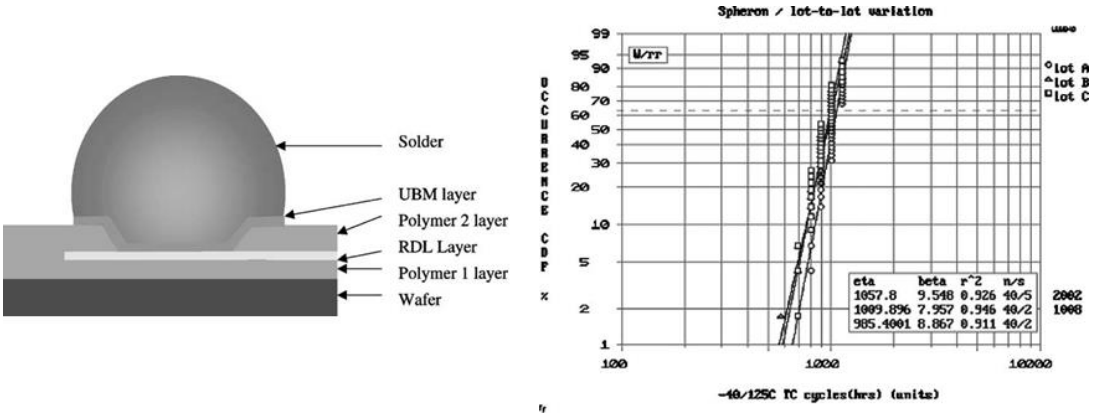


Figure 2.20 Bump-on-polymer structure [40].

Polymer stress buffers have also been explored for board-level interconnections. GT-PRC has demonstrated highly reliable SMT interconnections from glass and silicon packages to organic PWB with polymer dielectric layers [41]. High CTE glass (8.5 ppm/°C), low CTE glass (3.8 ppm/°C) and silicon packages with 7.2 mm body size were directly assembled on FR-4 PWB with lead-free solder balls of 250 µm diameter. Polymer layers of 25 µm were laminated on the packages to relieve the stress and strain in the solder interconnections, as shown in Figure 2.21. For the high CTE and low CTE glass packages, fatigue life was found to be 1800 cycles and 1300 cycles, respectively, while for the silicon package, the initial failure was identified at 300 cycles, due to the combination of lower CTE and higher modulus compared to the glass counterparts. SMT

interconnections for large low-CTE packages haven't been achieved with adequate reliability.

Stress relief using polymer collars has also been explored, where the polymer material in liquid form was spin-coated onto the roots of the solder balls, as shown in Figure 2.22 [42]. The polymer was then cured to form a 'collar' at the solder-pad interface. Such polymer collar layers resist crack initiation and improve reliability of the interconnections.

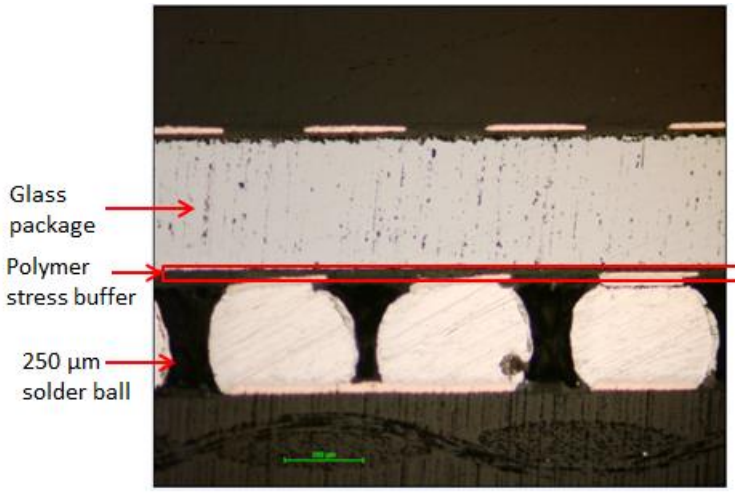


Figure 2.21 Glass package to organic PWB interconnections with polymer stress buffer [41].

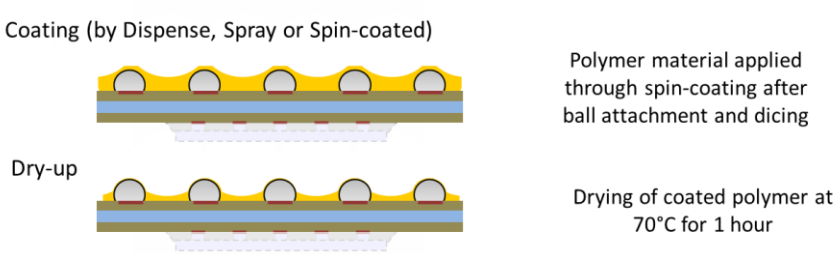


Figure 2.22 Stress relief by polymer collars [42].

2.3.3 Plastic core with metal shells for reliable interconnections

Hybrid interconnection structures which combine the low modulus polymer materials and metals have also been studied. Nobuyuki et al. demonstrated organic packages- to- ceramic board interconnections with plastic core with solder shell

structures [43]. The interconnections survived 600 cycles in accelerated test and the initial failure was identified at the metal layer near the center of the ball, as shown in Figure 2.23. Similar concept was employed by GT-PRC where polymer posts with metal shell were proposed as complaint interconnections, as shown in Figure 2.24 [44].

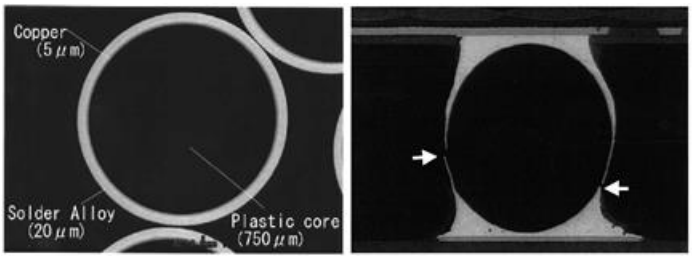


Figure 2.23 Plastic core with solder shell interconnection [43].

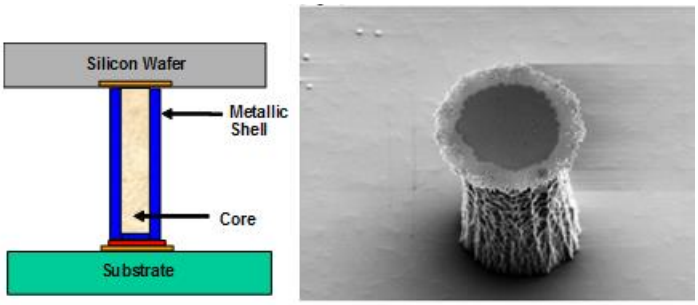


Figure 2.24 Polymer core with metal shell interconnection [44].

2.4 Electro-deposited copper wires for highly-reliable interconnections

The emergence of Cu-low K technologies and copper pillars or bumps for reliable chip-level interconnections made copper the most strategic interconnection material. Copper has excellent current-handling capability, much higher melting temperature compared to solders and good mechanical properties such as ductility and fatigue resistance. Electrodeposition is one of the most widely used methods to obtain copper films, lines and vias in microelectronic industry. Because of the widely-available infrastructure for electrodeposited copper at chip, package and board-levels, copper structures are also pursued for board-level interconnections. Both the elastic properties and the plastic behavior, which predominantly controls the strain to failure and fatigue

characteristics, are strongly dependent on the microstructural characteristics such as grain morphology and size. These characteristics can be controlled with plating conditions. Therefore, a brief review of structure-property relations in copper is provided in the subsequent sections.

2.4.1 Microstructure of electro-deposited copper

The microstructures of electroplated copper can be modulated by changing the current density, plating modes (DC plating or pulse plating), additives in the electrolyte, etc. With proper selection of the plating condition, copper deposits with grain size in nanometer range can be achieved. Seah et al. reported copper-filled vias with 100nm grain size obtained by DC plating at the current density of 0.05 A/cm2 [45]. At the same current density, Ibañez et al. reported copper film with lower grain size of 70 nm [46], and the microstructure of the plated copper is also significantly affected by the current supply cycles. The morphology of copper deposited by DC current, rectangular pulse current, square pulse current and triangular waveform was studied. With DC current, the deposit had fine-grained and compact surface, while with the pulse current, the deposit had a rougher surface with cracks or crevices, as shown in Figure 2.25.

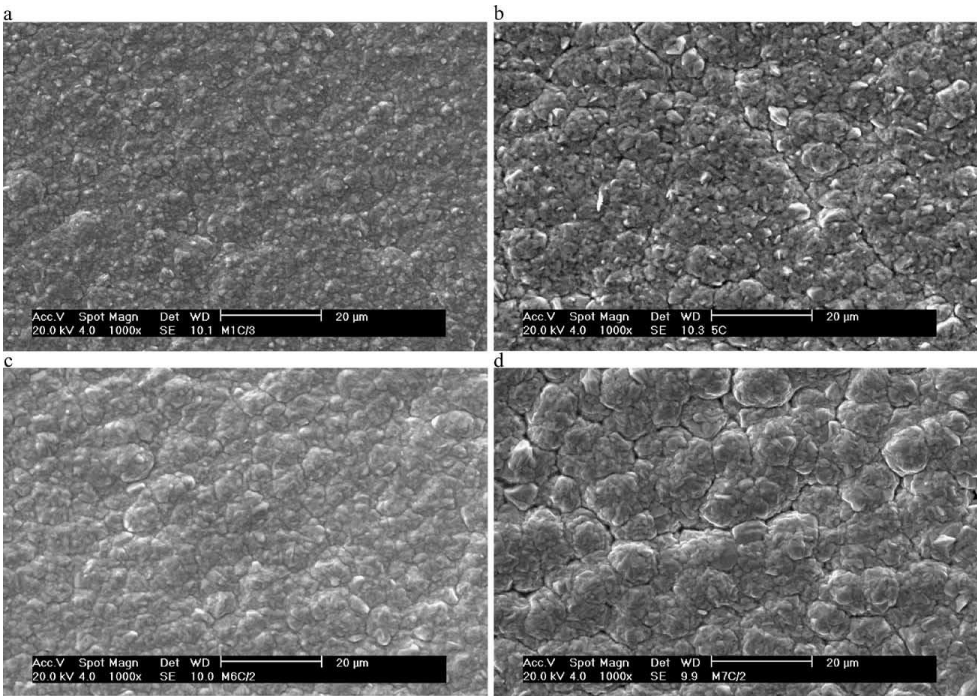


Figure 2.25 SEM micrographs of the copper electrodeposits (a) direct current, (b) rectangular pulse current, (c) square pulse current and (d) triangular waveform [46].

2.4.2 Mechanical properties of submicrocrystalline and nanocrystalline copper

The ultrafine grained materials (submicroncrystalline and nanocrystalline) have been a subject of growing interest because of their promising mechanical properties such as high yield strength and ductility. In many metals and alloys with average grain size of over 100 nm, the strengthening mechanism of grain refinement has been well understood by the Hall-Petch effect [47][48]. The dislocation pile-up at grain boundaries resist plastic flow and improve the yield strength. With further grain refinement, however, the yield stress peaks in many cases, and further decrease in grain size causes weakening of the material, as shown in Figure 2.26 [49].

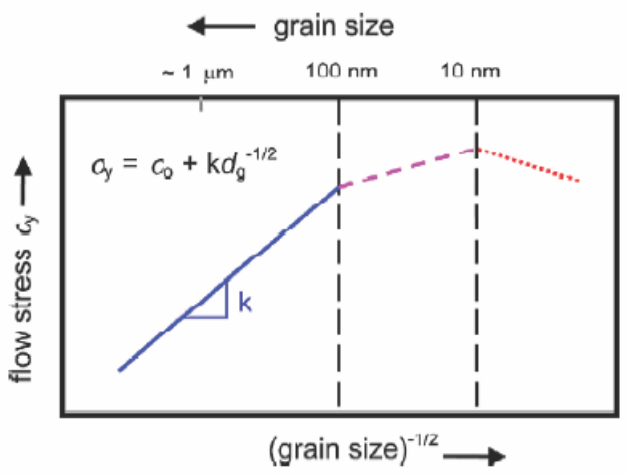


Figure 2.26 Effect of grain size on yield stress [49].

Nieh et al. [50] reasoned the inverse Hall-Petch effect by a critical grain size, which is the equilibrium distance between two edge dislocations given by the following equation:

$$l_c = \frac{3Gb}{\pi(1-\upsilon)H} \tag{2.4}$$

Where H is the hardness, G is the shear modulus and b is the burgers vector of the material. If the grain size is smaller than this distance, the dislocation cannot pile up and Hall-Petch effect breaks down. Furthermore as the grain size reduces, the volume fraction of the grain boundaries increases, and the material properties becomes more representative of the grain boundary activity, which results in the strength being inversely proportional to the grain size [51].

Several extensive studies of microscale and nanoscale copper have been recently reported. Koh et al. studied the mechanical properties of nanocrystalline copper with molecular simulation, and reported that the modulus of nanocrystalline copper decreases as the grain size reduces in the nanometer regime, due to an increase of the volume fraction of grain boundaries [52]. Witney et al [53] conducted tensile-tensile fatigue testing with a maximum stress amplitude of 80% yield stress on bulk nancrystalline

copper samples prepared by inert gas condensation, and reported stress-assisted grain growth. Bansal et al. [54] reported similar observation with ECAE nanocrystalline copper, where the average grain size increased from 45 nm to 56 nm for 1% total strain range, and the nanocrystalline copper failed before the microcrystalline counterparts. Mughrabi et al. [55] observed that a much improved high-cycle fatigue life for ultrafine grained copper produced by severe plastic deformation but the low-cycle fatigue life was shown to be worse than that of coarse-grained copper.

The mechanical properties of micro-scale specimen can be very different from those of the bulk materials. For copper wires with the diameter of a few microns, motion of dislocations is affected by the surface and edge effects from the microdimensions [56]. The direct investigations of mechanical properties of copper microwires are very limited, due to the difficulties of handling and measurement. Khatibi et al. [57] studied the high cycle fatigue property of copper wires with bamboo microstructure, prepared by drawing. The copper wires have diameter in between 10-125 μm, and the wires with 10 μm diameter showed improved yield strength and fatigue life. The fatigue behavior of free standing electro-deposited copper microwires, especially in the low-cycle regime, has not been reported.

CHAPTER 3

MECHANICAL DESIGN FOR RELIABILITY

Micro-scale copper wires with high aspect ratio, acting as compliant interconnections, are explored to address the interconnection reliability challenges between large low CTE packages and printed wiring boards, as outlined in Chapter 1 and shown in Figure 3.1. The primary focus of this chapter is to: 1) Model the impact of material and geometry parameters on the interconnection reliability, and 2) Arrive at design guidelines to define the microwire array geometry. Finite element models (FEM) are used to model and design the geometrical and material parameters of the microwire interconnections, to achieve low plastic strain in both the copper wires and the solder joints, and therefore high fatigue resistance.

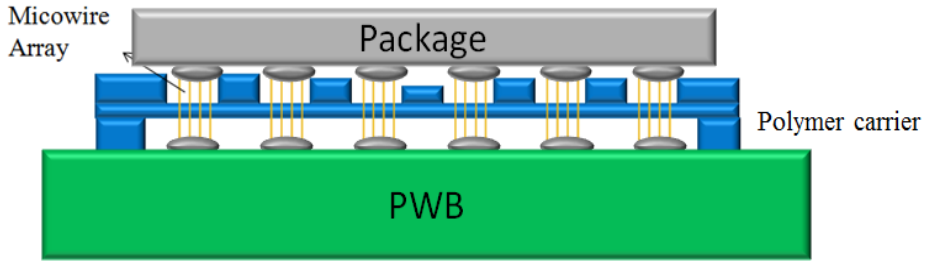


Figure 3.1 Copper microwire array compliant interconnections.

3.1 Finite element modeling

The assembly of 20 mm × 20 mm silicon package directly attached to FR-4 printed wiring board by microwire array (MWA) compliant interconnections at 400 μm pitch was modeled with ANSYS in this study. The FEM based on 2.5D geometry construction is used to model the three-dimensional structure of the assembly. Using to the half-symmetric nature of the geometry, a 400 μm × 10 mm strip located in the geometrical center was modeled, as shown in Figure 3.2. The strip contains 25 units, each with a dimension of 400 μm × 400 μm, with the detailed structure of each unit for the initial set

up, as shown in Figure 3.3. The thickness of the silicon package is 100 µm, and that of the PWB is 800 µm. The copper microwires are held together by a polymer layer, and are connected to the pads on the silicon side and on the PWB side with solders. The initial set up has one wire for each interconnection. The effect of wire geometry and number of wires per interconnection is discussed in Section 3.3.

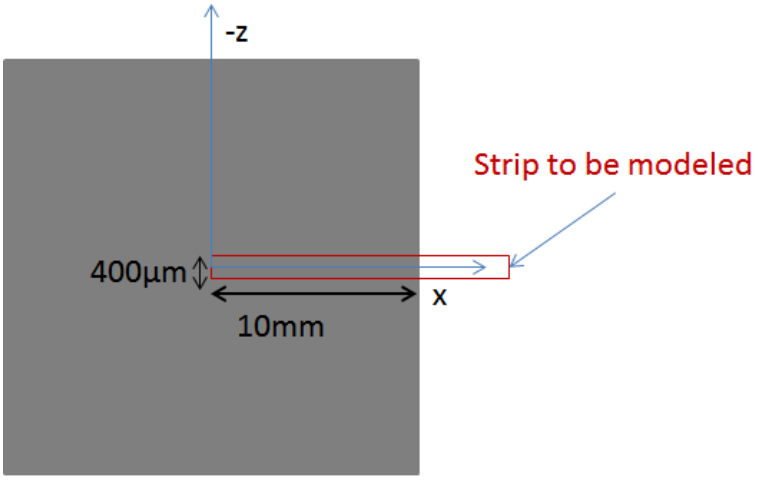


Figure 3.2 Top view of the half-strip used in 2.5D modeling.

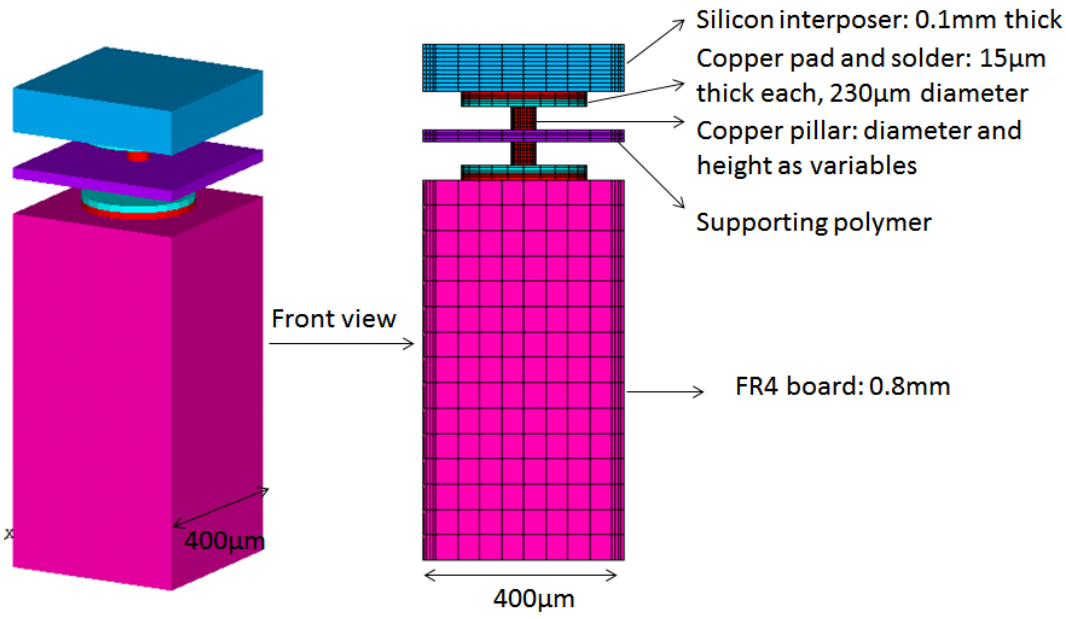


Figure 3.3 Detailed structure of each interconnection unit for initial set up.

3.2 Material properties for finite element modeling

Solder: Solder is a visco-plastic material at room temperature, therefore it undergoes both plastic deformation and creep under load beyond its yield strength. Anand's visco-plastic constitutive model was used for this study to capture the rate-dependent deformation of the solder. The primary equations in Anand's model are shown below, and the nine Anand constants used for SAC305 solder material are shown in Table 3-1 [58].

$$\dot{\varepsilon_P} = Ae^{-\left(\frac{Q}{RT}\right)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \tag{3.1}$$

$$\dot{s} = \left[h_o\left(1-\frac{s}{s^*}\right)^a sign\left(1-\frac{s}{s^*}\right)\right]\dot{\varepsilon_P}; a > 1 \tag{3.2}$$

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon_P}}{A}e^{\left(\frac{Q}{RT}\right)}\right]^n \tag{3.3}$$

Copper: Bilinear, isotropic hardening model was used for copper, which describes the elastic behavior up to the yield point, and the plastic behavior beyond this yield, as shown in the stress-strain curve (Figure 3.4). The elastic modulus used in the model is 121 GPa; the yield stress 172.4 MPa; and the tangent modulus 1034 MPa. The temperature dependence below the reflow temperature is negligible for copper.

FR4: Temperature-dependent elastic orthotropic properties were used for the FR4 printed wiring board. At room temperature, the elastic moduli are 22.4 GPa in the in-plane directions, and 1.6 GPa in the out-of-plane direction. The CTEs are 16 ppm/°C in the in-plane directions, and 25 ppm/°C in the out-of-plane direction.

Silicon: Silicon is modeled as linear elastic isotropic material with a modulus of 130 GPa and CTE of 2.7 ppm/°C.

Table 3-1 Anand constants for SAC 305.

Constant Number	Anand Constant	Units	SAC305 Multiple Creep Tests
1	s_0	MPa	23
2	Q/R	1/K	10150
3	A	sec^{-1}	5200
4	ξ	Dimensionless	6.0
5	m	Dimensionless	0.18
6	h_o	MPa	34000
7	$\hat{s}$	MPa	30.0
8	n	Dimensionless	0.008
9	a	Dimensionless	1.62

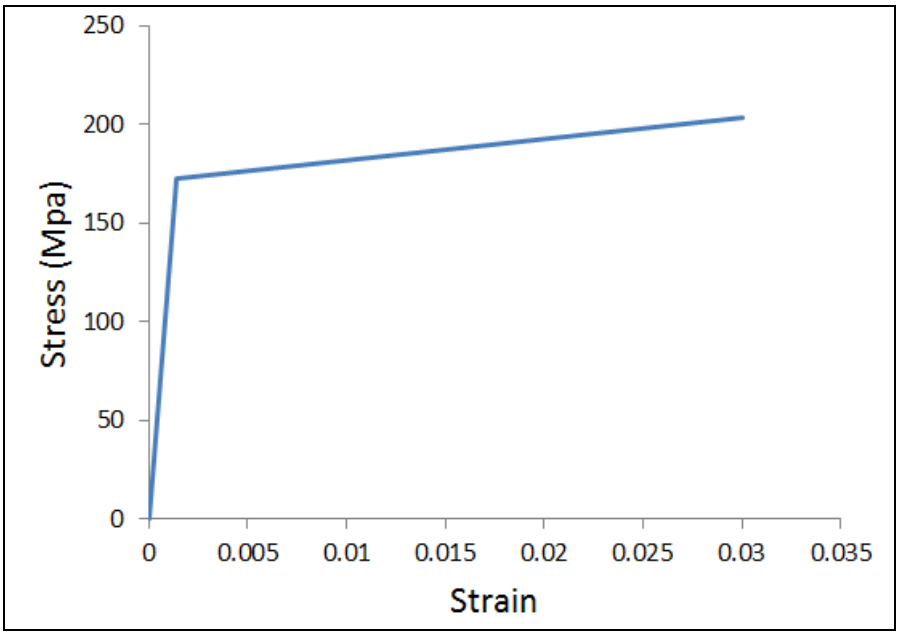


Figure 3.4 Stress-strain curve of copper.

3.3 Geometry optimization with one unit

To reduce the complexity and computing time, a single unit within the whole package cross-section, referred to as the strip, was first studied to evaluate the effect of interconnection geometry on reliability. The optimized copper wire geometry for one unit is anticipated to provide the optimized solution for the whole strip.

3.3.1 "Double pads" structure for assembly convenience and higher bonding strength

In the initial design, the copper microwires are directly assembled onto the silicon pacakge pads and PWB pads using solder. This may cause assembly concerns due to solder wicking onto copper wires. Furthermore, the bonding strength between copper wires and solder may not be sufficient due to small contact area. "Double pad" structure was proposed to address these concerns, as shown in Figure 3.5. Prior to assembly, an additional copper pad is formed on both sides of the wires, and the assembly is then achieved by the solder joint between two copper pads. The "double pads" structure increases the contact area which helps to improve the bonding strength, and also prevents solder wicking onto the copper wires. The additional pads can be formed by "mushroom plating" during wire fabrication, without adding lithography steps.

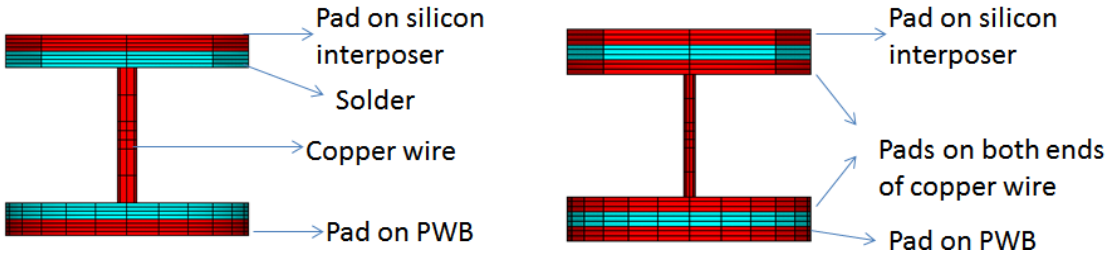


Figure 3.5 "Double pads" structure.

3.3.2 The effect of copper wire diameter on the strain in interconnections

The unit with "double pad" structure was submitted to a temperature drop from reflow temperature (250 °C) to room temperature (25 °C), and the equivalent plastic strain in both solder and copper wires were calculated to assess the reliability performance. The diameter of the wires was varied to study the influence on the strain in interconnects. The diameters considered were 100 µm, 50 µm, 20 µm and 10 µm, while the height of the wires was kept constant at 125 µm. As the wire diameter decreases from 100 µm to 10 µm, the maximum nodal plastic strain in solder reduces from 19.9% to 0.94%, while that in copper wire increases from 0.2% to 3.47%, as shown in Figure 3.6. The maximum nodal strain site moves from solder to copper wires, which indicates that more CTE mismatch is accommodated by the plastic deformation of copper wires, and less by the solder.

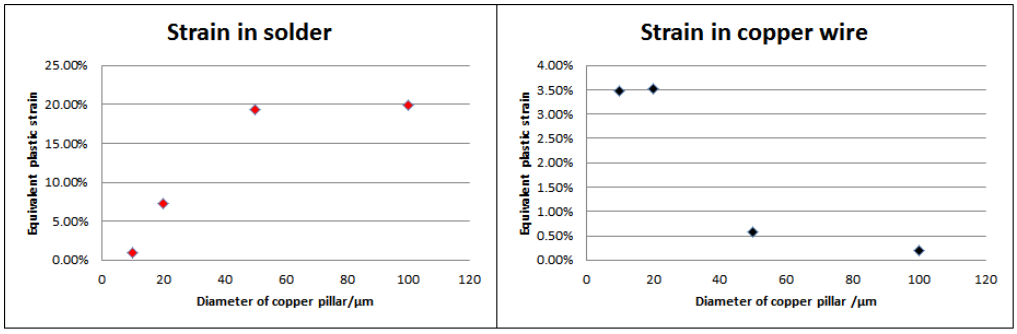


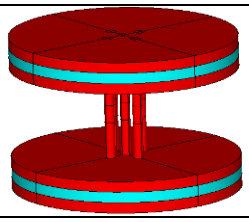
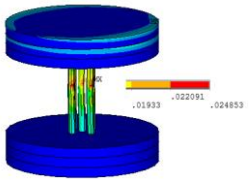
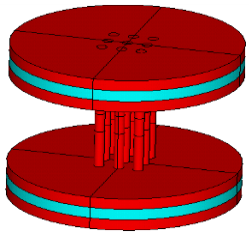
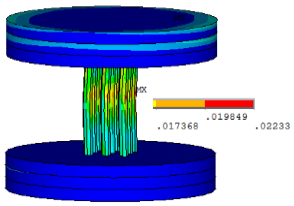
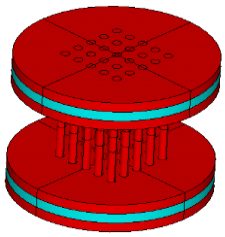
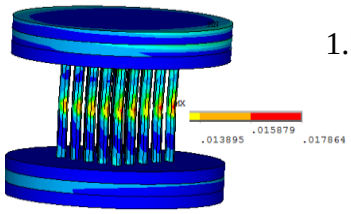
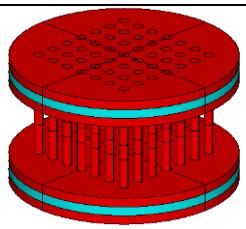
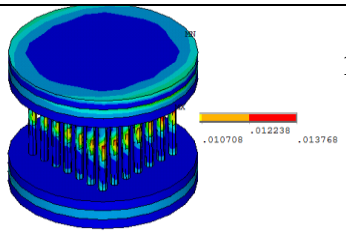
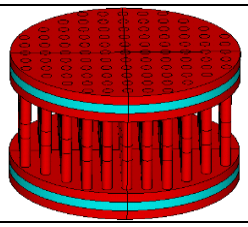
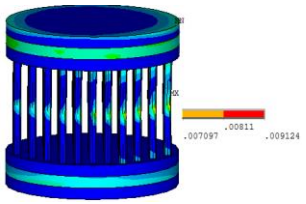
Figure 3.6 Equivalent plastic strain in solder and copper microwire as a function of wire diameter.

3.3.3 The effect of number of wires per interconnect

Having multiple wires per interconnect offers redundancy in the structure which ensures both electrical conductivity and mechanical integrity. The strain in copper wires was calculated as a function of wire numbers per interconnect, as shown in Table 3-2. The wire diameter was chosen as 10 µm, and wire pitch as 20 µm in all these models. The maximum nodal strain reduces as the number of wires increases, since the deformation can be shared by multiple wires. As extracted in Figure 3.7, the maximum

equivalent plastic strain reduces from 2.5% to 0.9%. At the same time, the strain in the solder increases from 0.97% to 1.12%, which is marginal compared to the 2.7x reduction of the strain in the copper wires.

Table 3-2 Strain contour in copper wires with multiple wires per interconnect.

Number of wires per interconnect	Geometry	Maximum nodal equivalent plastic strain in wires
5		 2.48%
9		 2.23%
25		 1.79%
49		 1.38%
Fully populated (97)		 0.91%

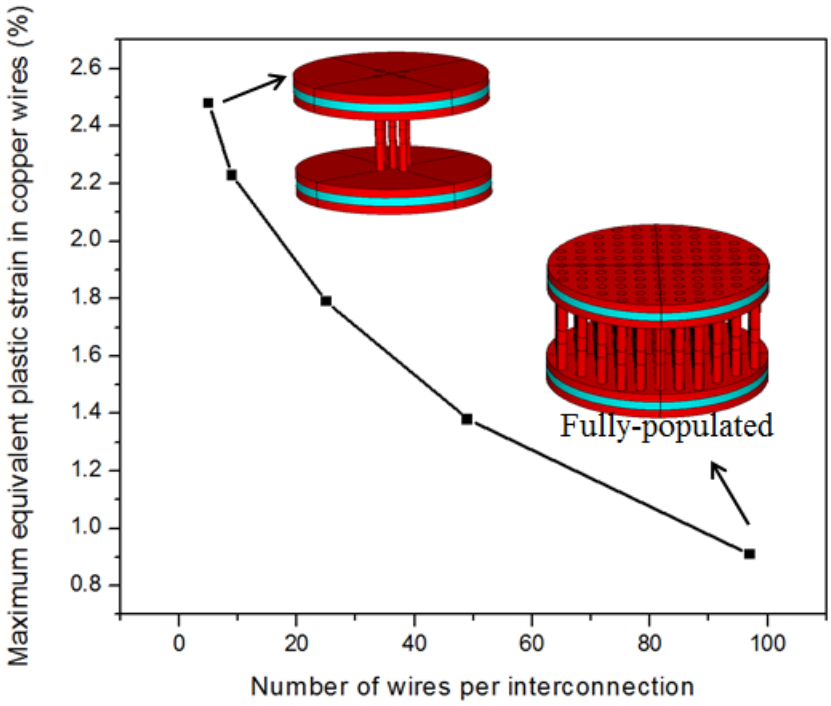


Figure 3.7 Effect of number of copper wires on plastic strain.

3.4 Modeling with whole strip and estimation of fatigue life

The complete package array cross-section, referred here as strip, was modeled based on the geometry study of the single unit. The polymer layer was initially designed as a carrier to hold the wires, which can also be used to transfer the wires during fabrication and for assembly. In this section, the effect of the polymer carrier material properties on the interconnection reliability was studied with the whole strip model, including the CTE and Young's modulus. In these studies, the geometry of the copper wires was kept constant: the wires are fully populated on each pad, with 10 µm diameter at 20 µm pitch, and 50 µm height on both side of the polymer carrier.

The units further away from the geometrical center are more critical for the study, since they have larger distance from neutral point and higher strain in the interconnections compared to the inner units, and therefore are expected to have earlier failures. The edge units were modeled with full detail as shown in Figure 3.8 (a).

Simplified structure was used for inner units to reduce the calculation complexity. As shown in Figure 3.8 (b), a cylinder with the same diameter as the copper wire bundle was used for the inner units. The cylinder was chosen such that the simplified unit has the same response (deformation in the vertical direction) when the same uniaxial force is applied. The cylinder material with 40 GPa modulus was used, such that the deformation values of the two structures are very close to each other, 0.031 mm and 0.032 mm, respectively, under the same load of 2.7N in y axis (Figure 3.9).

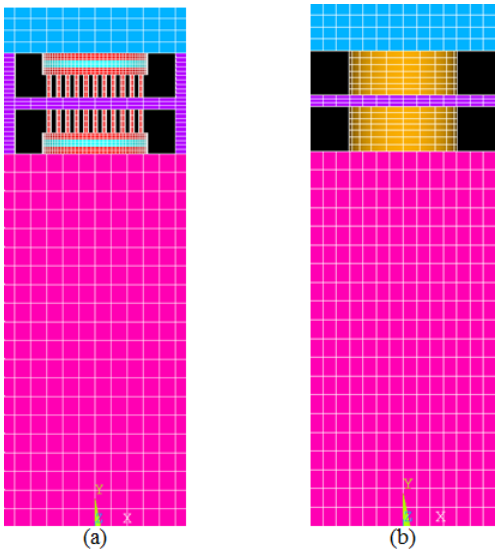


Figure 3.8 (a) Detailed structure for edge units, (b) Simplified structure for inner units.

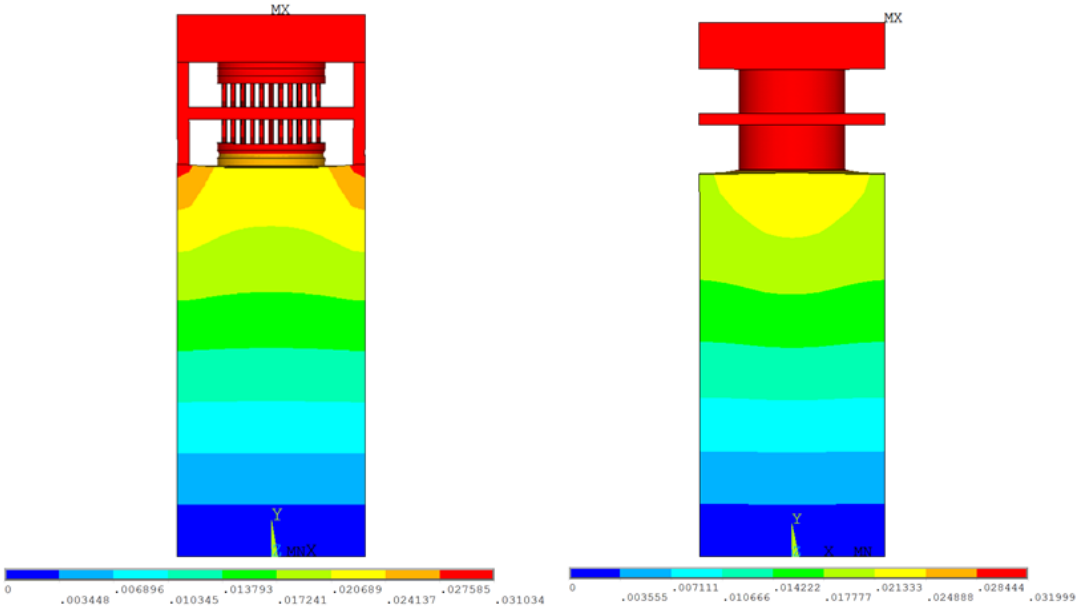


Figure 3.9 Deformation in vertical direction under uniaxial load for microwire unit and simplified unit.

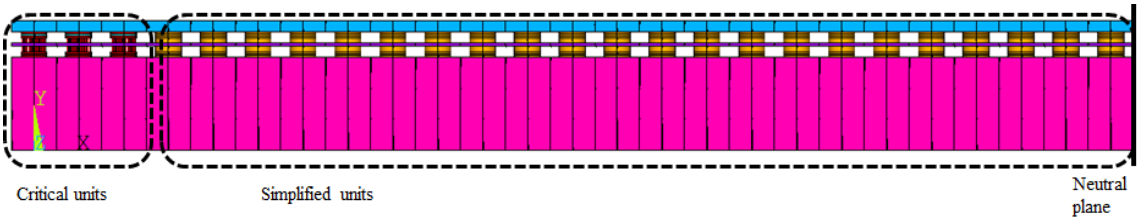


Figure 3.10 Complete strip with simplified structure for inner units and detailed structure for critical units.

The complete strip is shown in Figure 3.10. Three units on the edge were modeled in detail, and the inner units were simplified. The right most face of the strip was defined as the neutral plane, and symmetrical boundary conditions were applied, with one node pinned to avoid hard body movement. The model was subjected to a temperature drop from reflow temperature to room temperature, followed by thermal cycles, each from -40°C to 125°C, as per JEDEC standard (JESD22-A104D, type G).

The effect of the modulus and CTE of the organic carrier were studied using the whole strip model. The modulus values studied were 3500 MPa, 2000 MPa and 1000 MPa, and the CTE was varied from 60 ppm/°C to 20 ppm/°C at each modulus value. The corresponding maximum nodal equivalent plastic strain values in copper wires are shown

in Figure 3.11. At a given modulus, the strain in copper decreases with lower carrier CTE. With higher carrier modulus, the strain reduces at an even faster rate. Therefore, carriers with high modulus and low CTE correspond to lower strain in copper wires.

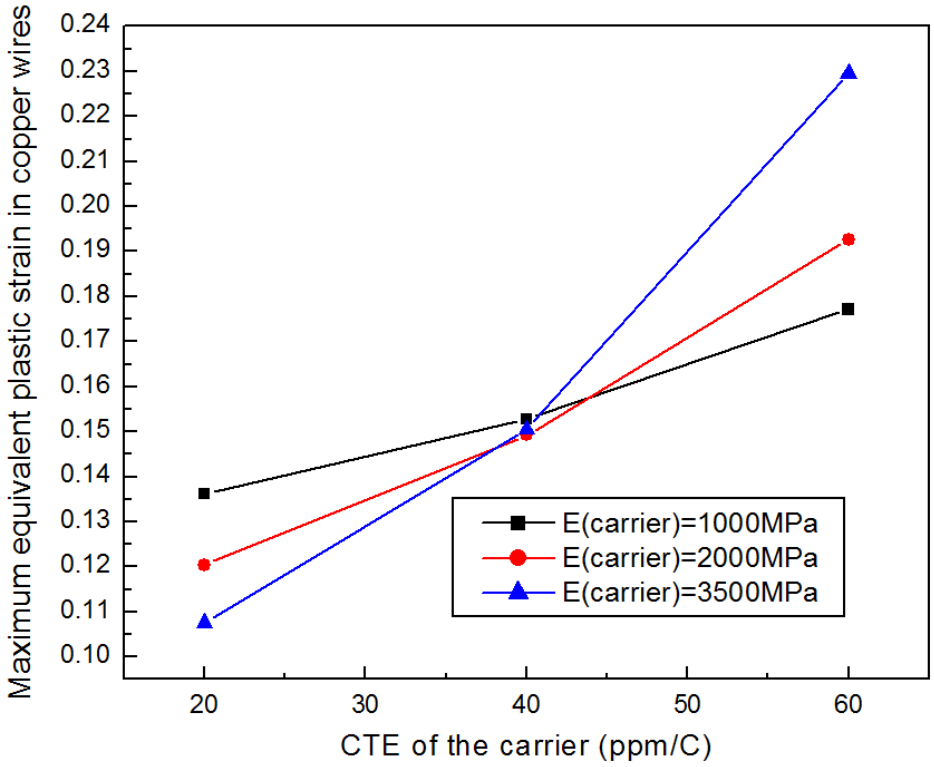


Figure 3.11 The effect of modulus and CTE of the carrier.

The corresponding strain in solder as a function of carrier properties was calculated, as shown in Figure 3.12. The strain in solder is not as sensitive to the carrier CTE change as the strain in copper wires. There is a mild increase in solder stain as the carrier CTE decreases and the modulus increases. The black dashed line shows the extrapolated strain in copper if the polymer frame has higher modulus (higher than 3500 MPa). As indicated the Figure 3.12, the earliest failure site will move from copper wires to solder joint if a very stiff carrier with low CTE is applied. The optimized carrier properties are identified when the balance between the corresponding fatigue life of copper wires and that of solder is achieved.

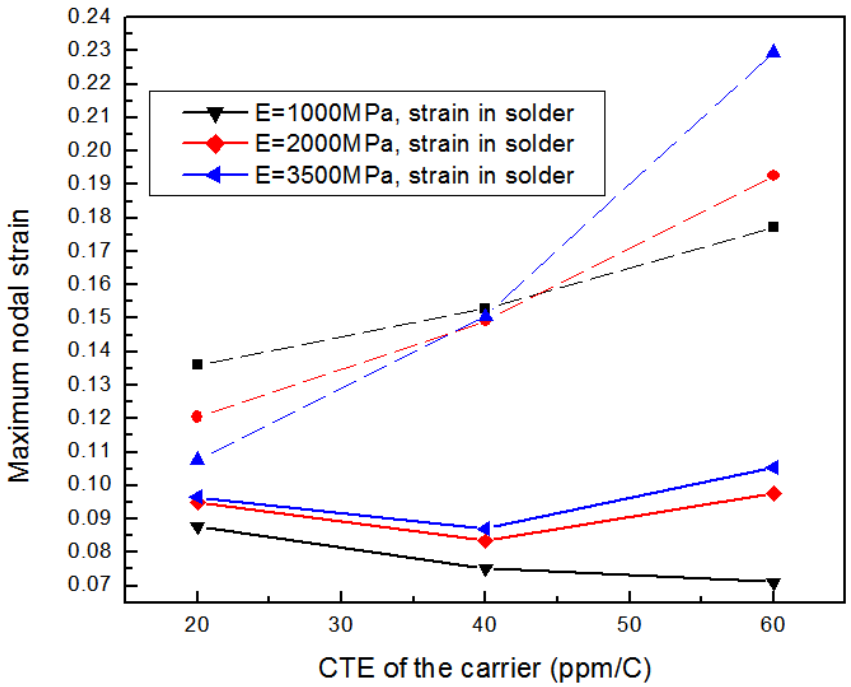


Figure 3.12 Corresponding strain in solder as a function of carrier property.

The fatigue life of copper wires and that of solder was found to be very close when the carrier modulus is 7500 MPa and CTE is 20 ppm/°C. The maximum elemental equivalent plastic strain range per cycle in copper wires is 0.4146%, and that in solder is 0.785%. The elemental strain is the volume average of the strain in the elements in the vicinity of the nodes where the maximum nodal strain occurs. The fatigue life was calculated using Coffin-Manson relationship, as shown in Equations (4) and (5). The corresponding fatigue life of copper is calculated to be 1447 cycles, and that of solder as 1158 cycles. The performance is compared with a structure where no carrier frame is used in the middle, as shown in Table 3-3. Without the carrier, high plastic strain was found in copper wires, especially on the top tips and bottom tips where the wires connect to the pads. The strain was more uniformly distributed and the maximum value was significantly reduced with the proper selection of the carrier frame. This phenomenon is illustrated by Figure 3.13. When no carrier was applied, the copper wires are simply tilted as the assembly gets cooled from stress-free temperature to room temperature, due to

large shrinkage ratio of the PWB side compared to the interposer side. A carrier in the middle would act as an anchor, which pulls the wire towards the center due to the higher CTE of the carrier material, and thus introduce additional deformation site in the middle and helps uniformly distribute the strain along the wires.

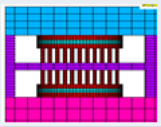
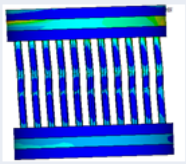
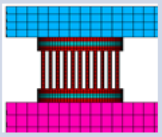
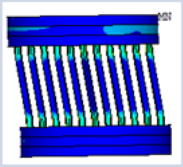
Coffin-Manson model for copper:

$$N^{-0.6} \times 0.2249^{0.75} = \Delta\varepsilon_p \tag{3.4}$$

Coffin-Manson model for solder:

$$\mathrm{N} = 0.5 \times \left(\frac{0.65}{\Delta\varepsilon_p}\right)^{\frac{-1}{0.57}} \tag{3.5}$$

Table 3-3 Equivalent plastic strain range per cycle and corresponding fatigue life of interconnection.

	Strain contour at the end of five thermal cycles	Equivalent plastic strain per cycle	
		Averaged over 1 element **(for conservative estimation)**	Averaged over adjacent elements
Modeled structure: frame in the middle 		Copper: 0.4146% • 1447 cycles Solder: 0.785% • 1158 cycles	Copper: 0.1836% • 5625 cycles Solder: 0.5077% • 2488cycles
V.S. no frame used 		Copper: 1.11% • 280 cycles Solder:0.43% • 3275 cycles	Copper:0.37% • 1749 cycles Solder:0.4215% • 3449 cycles

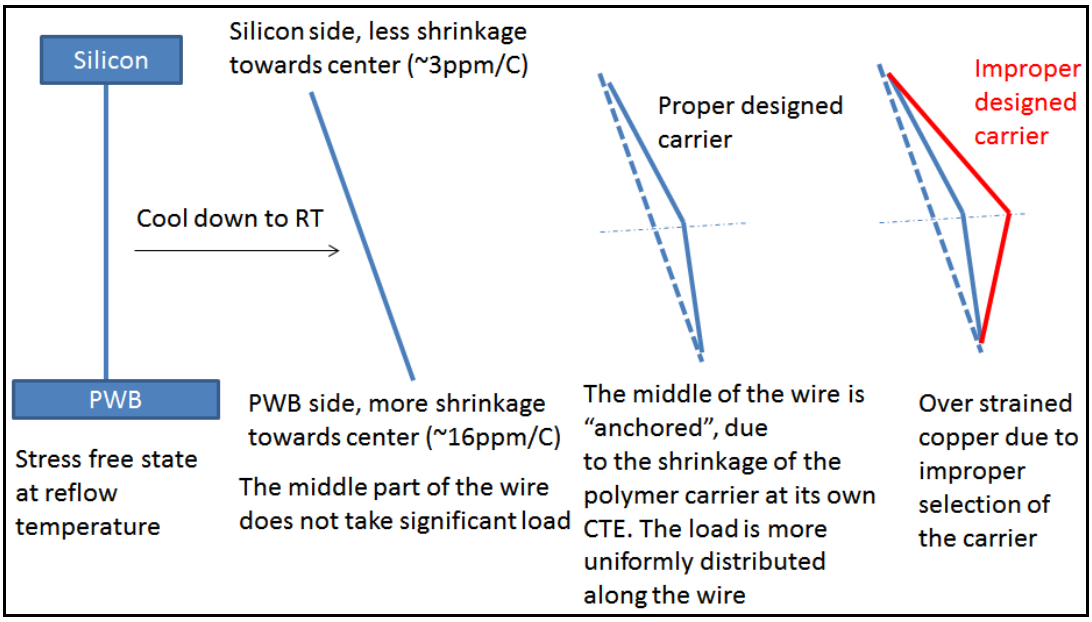


Figure 3.13 Anchor effect of polymer carrier.

3.5 Fatigue life comparison against standard BGA SMT interconnections

The reliability performance of the microwire array interconnection was compared with BGA interconnection with finite element modeling. A 2.5D model of a silicon package directly connected to FR-4 printed wiring board through standard solder balls was built to estimate the fatigue life of BGA interconnections. Same material properties for silicon, solder, copper and FR-4 were used for the BGA model as for the MWA model, and the as shown in Figure 3.14. The calculated fatigue life of SAC305 solder joint is 459 cycles, as shown in Table 3-4. Therefore the traditional BGA solder interconnection does not provide sufficient reliability performance for direct attachment of large low-CTE packages onto organic PWBs. In contrast, the MWA interconnections are projected with over 1000 cycles fatigue life and thus promise outstanding reliability of large silicon packages, as large as 20 mm × 20mm.

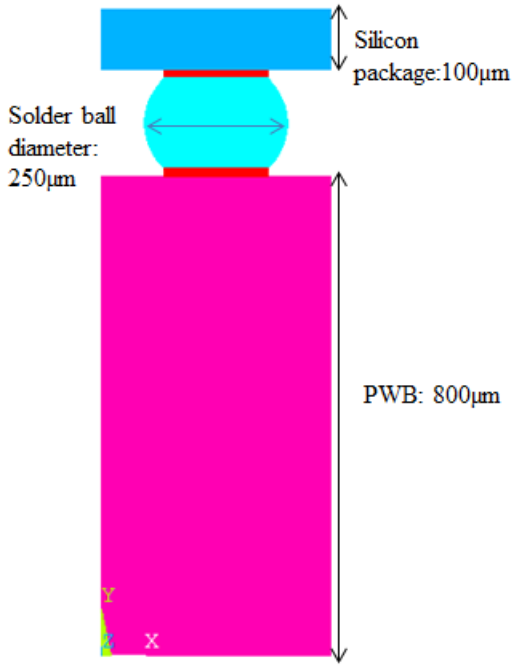


Figure 3.14 BGA interconnection unit.

Table 3-4 Fatigue life calculation for MWA and BGA interconnections.

Structure	**Equivalent plastic strain range per cycle**	**Projected fatigue life**
Copper microwire array	Solder- 0.785%	Solder- 1158
	Copper- 0.414%	Copper- 1450
BGA	1.33%	459

3.6 Summary of the mechanical design

The geometry and material parameters were decided based on the modeling results. Fully populated copper microwires with 10 μm diameter at 20 μm pitch held by a polymer carrier were used as the compliant interconnections, and the polymer material parameters, including modulus and CTE, were optimized for lowest plastic strain and highest fatigue life. The reliability performance of the MWA interconnections was

compared with conventional BGA interconnections, and projected more than 2X improvement in fatigue life in accelerated test.

CHAPTER 4

MATERIALS AND PROCESSES FOR FABRICATION OF THE TEST VEHICLES

This chapter focuses on materials and fabrication processes to achieve the interconnection structure following the finite element modeling.

4.1 Summary of design inputs from finite element modeling

Based on the studies from Chapter 3, the design of microwire array interconnections is shown in Figure 4.1. The wires are positioned on both sides of the carrier that are 10 µm in diameter and 50 µm in height. These wires are fully populated on the pads at 20 µm pitch. "Double pad" design is used for the interconnections, where the wires are connected by a first copper pad (as shown in Figure 4.1) and then connected to the pad on the package and board side by solder joints. The optimal polymer carrier, as per modeling inputs, has a modulus of 7.5 GPa, CTE of 20 ppm/°C, and thickness of 25 µm.

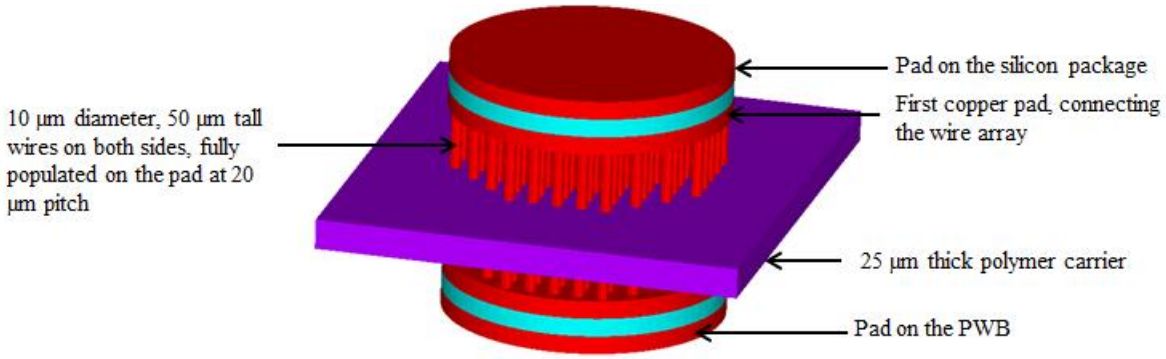


Figure 4.1 Design of MWA Interconnection Insert.

4.2 Polymer Carrier

Two polymer candidates were identified from the modeling results. The first one is a 25µm-thick Pyralux AC film from Dupont, with 7.58 GPa modulus and 19 ppm/ °C CTE. The second one is a 50µm-thick Syron 7000 film from Rogers, with 8.6 GPa modulus

and 18-23 ppm/°C CTE. A comparison of the fatigue life of copper wires with solder joints with different carrier materials is shown in Table 4-1. The Syron 7000 showed much better performance with more balanced strain distribution between the copper wires and solder joints, benefited from its higher film thickness, and therefore increased stand-off height of the interconnections. Thicker polymer carriers also improve handling, and control of wrinkles and warpage during fabrication. Syron 7000 material is a thermoplastic polymer, with 18 µm copper foil cladding on both sides. It is also thermally and chemically stable, lead-free compatible and halogen-free. With both reliability and processing benefits, Syron 7000 was chosen as the carrier material for this study.

Table 4-1 Fatigue life of the interconnection with different carrier materials.

Carrier Material	Projected solder fatigue life	Projected copper fatigue life
Pyralux AC	931 (0.89%)	1634 (0.38%)
Syron 7000	1762 (0.618%)	1831 (0.36%)

4.3 Process development for copper wire fabrication

One of the major challenges in fabrication of the MWA interconnections is to achieve high aspect ratio copper wires with low cost. This section discusses the process development for wire fabrication, including the lithography optimization and electrolytic deposition.

4.3.1 Lithography optimization for high aspect ratio features

The goal for lithography experiments is to open 10µm-diameter vias in 50µm-thick photoresists. Certain liquid photoresist materials have high aspect ratio capability, but are not compatible with panel processing, and are usually costly. The resist candidates were, therefore, narrowed down to dry-film photoresists, for easier adoption by the packaging industry.

Sample-A, the Hitachi (SA) 25 µm film, was identified as a good candidate for this application. It was indeed qualified for high-density 5µm wiring traces. Two layers of SA films are required on both sides of the carrier to form 50µm-thick resists. For process development, an existing mask with 15 µm diameter features (full array) was used.

The lithography experiments were conducted on silicon substrates. Two layers of SA films were laminated using a roll laminator at a temperature of 115°C. The optimum exposure dose was found to be 120 mJ/cm^2. A minimum of 1hr post-exposure dwell time at room temperature is required for sufficient crosslinking before development. The spray development system in PRC cleanroom was used for photoresist patterning. The development solution is 3 wt. % Na_2CO_3, and the development temperature and speed are 30 °C and 7 inches/minute, respectively. Figure 4.2 shows the openings in 2 layers of SA films. The opening diameter is around 14.65 µm, slightly smaller than the mask size of 15 µm. Resist residue was found at the bottom of the vias, with a thickness of about 400 nm. Plasma treatment (CF_4 and O_2) for 10 mins was used to remove the resist residue, as shown in Figure 4.3.

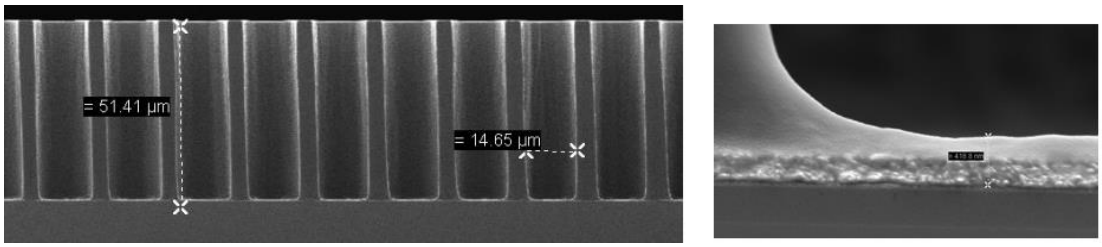


Figure 4.2 Cross section of 15µm openings in 50µm thick resist.

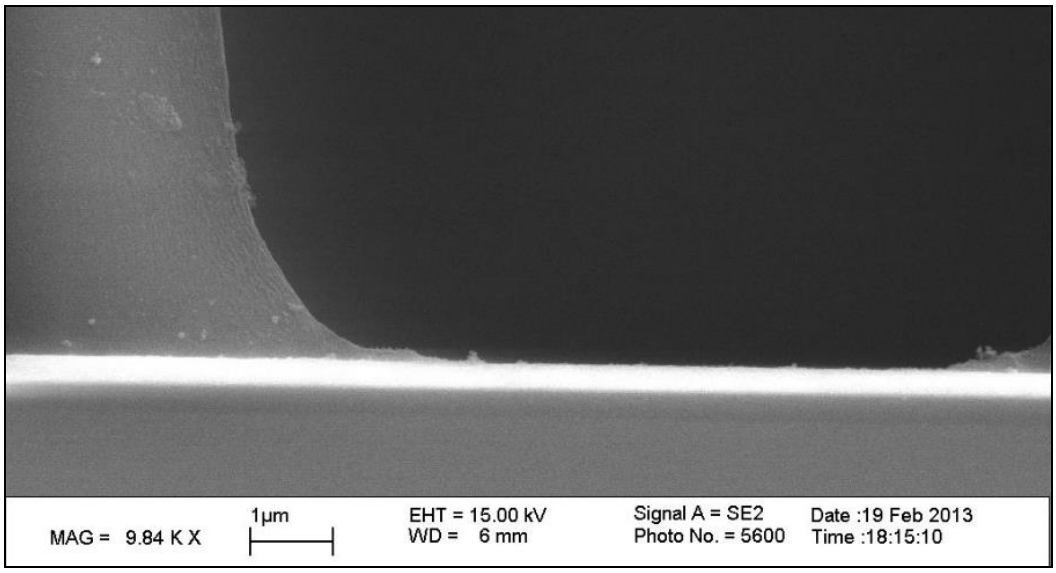


Figure 4.3 Photoresist residue removal by plasma.

4.3.2 Electrolytic plating experiments for copper wire fabrication

Plating experiments were conducted on FR-4 substrates with 50 µm thick patterned photoresists on both sides. A DC current of 5A was applied to a 6’’x 6’’ sample. Plating was performed for ~4 hrs to fill the 50 µm tall vias and to form a mushroom pad on top. The average thickness of the mushroom is about 12 µm. Figure 4.4 shows the cross-section of wires plated on both sides of the substrate, and Figure 4.5 shows the detailed structure of the wires from measurements. From the mask with 15 µm diameter features, the actual wire diameter after seed layer removal is about 10-14 µm. Based on 5 measurements, the average value is about 13.6 µm on bottom, and 11.86 µm on top.

The final goal is to achieve wires with 10 µm diameter. However, there are risks associated with 10 µm opening, including fully open the vias in photoresist, resist removal and wire plating for the structure with higher aspect ratios. Therefore, 15 µm features were used for mask design based on the process development results, and the fabricated wires can be further thinned down with acid etch. As shown in Figure 4.6, the wire diameter reduced to 10.5-11.6 µm after 3 minutes microetch, and further reduced to 7.1-8 µm after 6 minutes microetch.

Based on fabrication considerations, certain parameters are altered from the modeling results:

1. Syron 7000 polymer was chosen as the carrier, which has 50 μm thickness other than 25 μm used in the modeling;
2. The modulus and CTE of the carrier differ from the optimal values suggested by modeling by 15% and 10%, respectively.
3. The copper wire mask design has 15 μm opening size instead of 10 μm.

The above compromises are made based on considerations from both processability and materials availability. The effect of the above changes on the fatigue life of the interconnections will be discussed in Chapter 5.

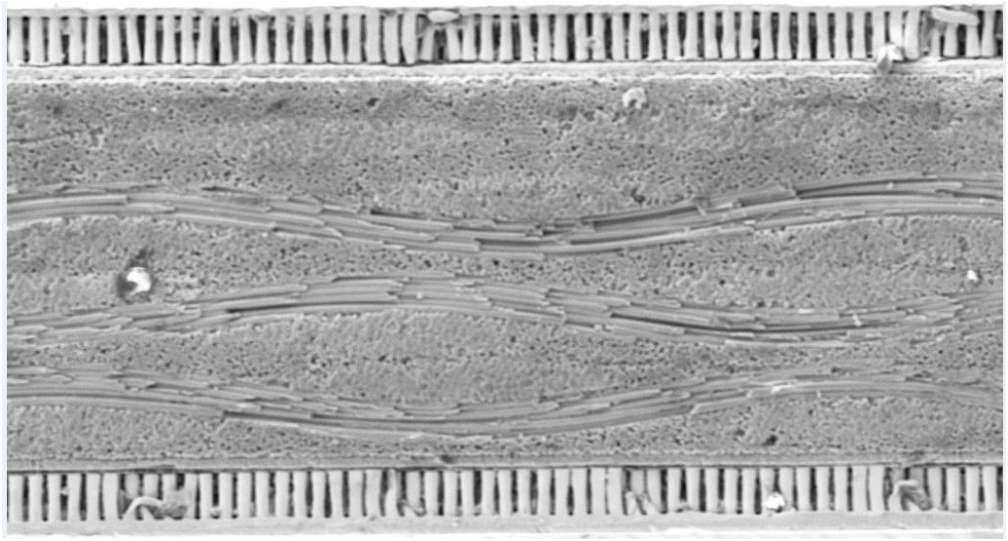


Figure 4.4 Plated copper wires on both sides of a FR-4 substrate.

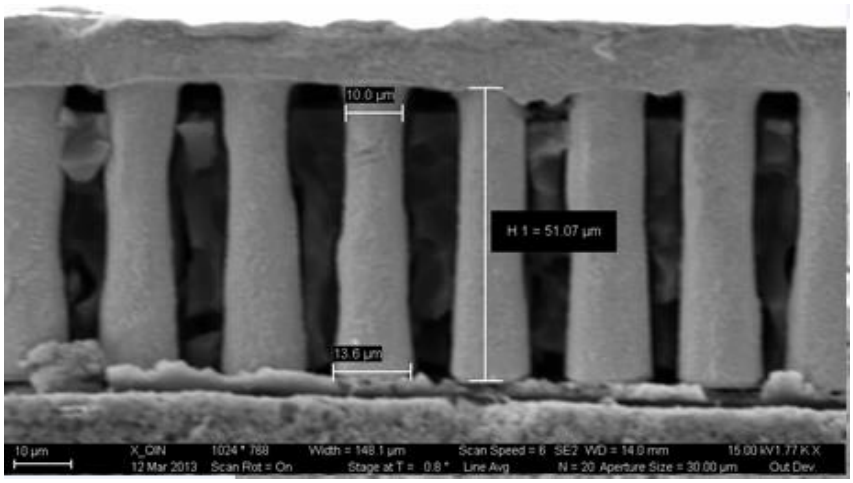
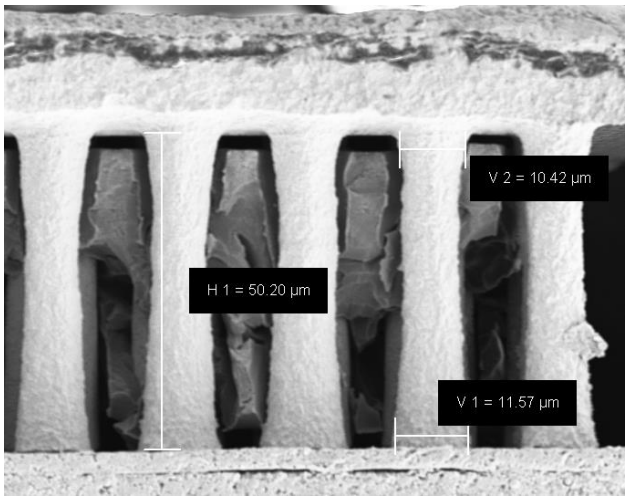
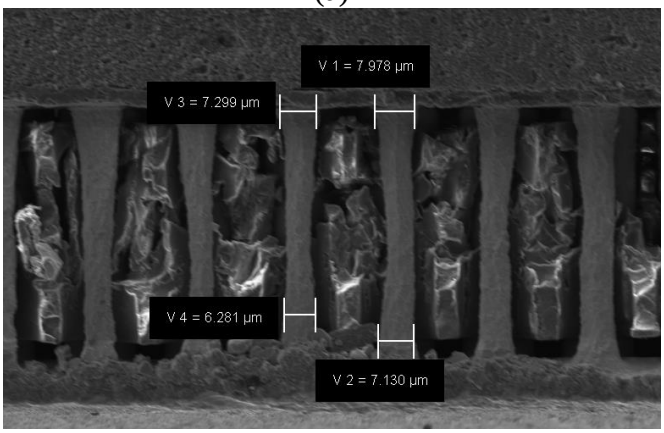


Figure 4.5 Copper wires fabricated from mask with 15 µm features.



(a)



(b)

Figure 4.6 Wire dimension after microetching for (a) 3 minutes, (b) 6 minutes.

4.4 Fabrication process design

The fabrication process was designed based on the input from both modeling and process development, as shown in Figure 4.7. The process includes two major parts: the fabrication of the polymer carrier (a-c), and the fabrication of the wires on both sides of the carrier (d-h).

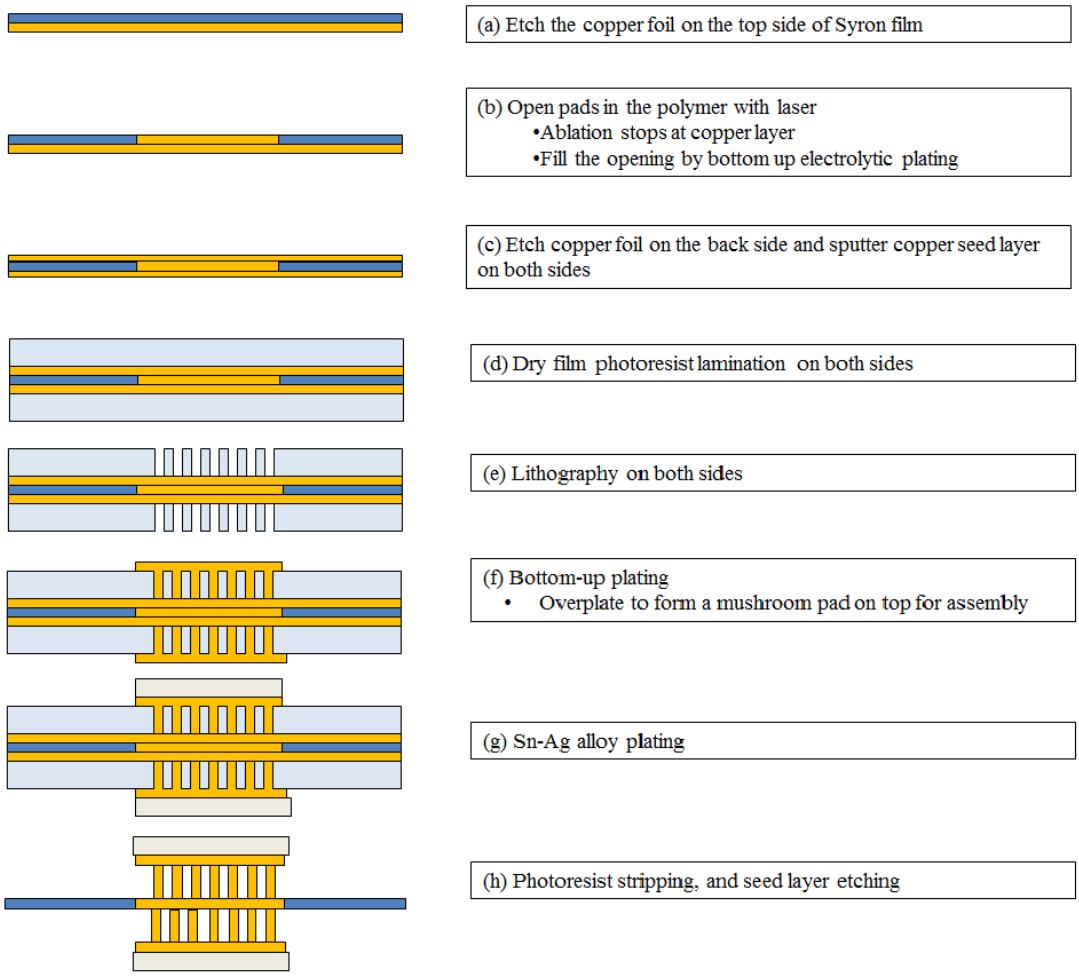


Figure 4.7 Fabrication procedure for microwire array interconnections.

4.5 Fabrication of the Syron carrier

The Syron material has 18 μm copper foil cladding on both sides. As shown in Figure 4.7(a), the copper foil on the top side was first removed with an acid etcher. The polymer was then sent for laser drilling (Micron Laser Technologies) to open the vias. Figure 4.8 shows the design of the polymer carrier for via drilling. The pad size is

designed for 225 µm. The via entrance is ~249 µm, and exit is ~217 µm, as shown in Figure 4.9. The vias were metallized by bottom-up electrolytic plating for electrical connections between the wires on the top and bottom side of the polymer, and the copper foil on the back side was used as the seed layer. The height variation of the plated post was severe across the 6''x6'' panel, due to the non-uniform plating rate. The height variation and rough surface of the plated post could cause poor adhesion of wires onto the post. The backside copper clad was then etched, with the front side covered by dryfilm photoresist as protection. The fabricated Syron sample is shown in Figure 4.10. Copper with titanium adhesion layer was sputtered on both sides of the Syron film as seed layer for wires fabrication.

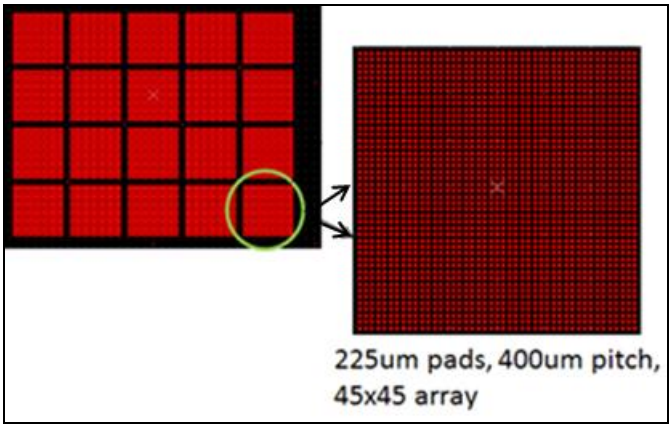
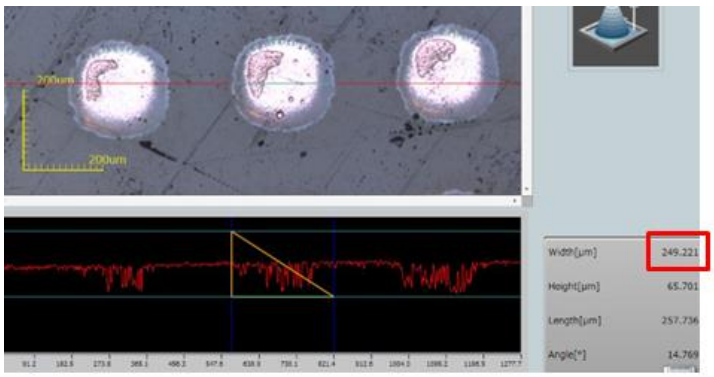
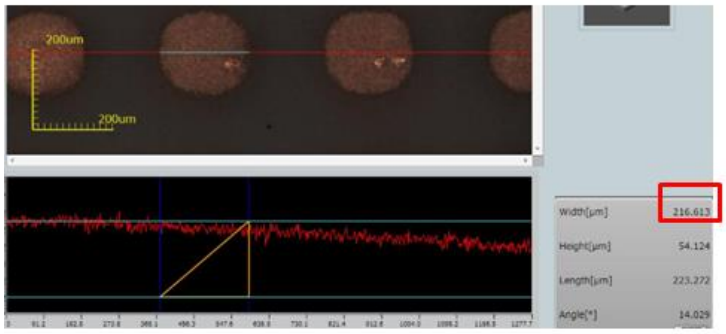


Figure 4.8 Layout design for laser via drilling in the polymer carrier.



Via entrance



Via exit

Figure 4.9 Via dimension measurement.

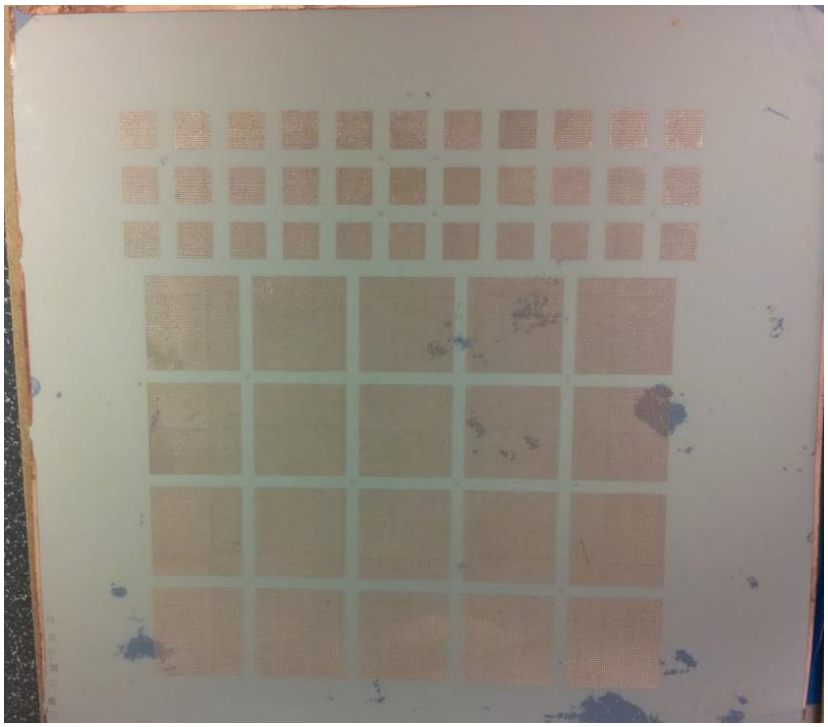


Figure 4.10 Syron carrier with plated copper posts.

4.6 Fabrication of the copper wire arrays on the carrier

As shown in Figure 4.7 (d)-(h), the wire fabrication includes lithography, wire formation by bottom-up electrolytic plating, solder plating, resist stripping and seed layer etching. The design of copper microwires is optimized for the properties of Syron carrier, as shown in Figure 4.11. The wire diameter is 15 micron, and the pitch is 20 micron. The wire diameter is chosen based on fabrication concerns, as discussed in Section 4.3. The wires can be further thinned down to 10 microns by extended microetching during seed-layer removal. Sample-A 25 μm film from Hitachi (SA) was used for lithography. Two layers of SA film were laminated on both sides of the carrier to achieve 50 μm wire height. Exposure was conducted with Karl Suss TSA-MA6 lithography tool, with the expose energy of 120 mJ/cm^2. Development was performed with an aqueous sodium carbonate (3 wt.%) solution developer in an automated tool (CHEMCUT Corp.), with the speed set for 7 inch/minute and temperature at 86° F. Oxygen plasma was used for cleaning up the resist residue after development. Copper microwire arrays were fabricated with bottom-up electrolytic plating, and an overplated mushroom top was formed on the top of the wires for assembly. Figure 4.12 shows the top view and the side view of the wires plated on the posts with overplated mushroom pads.

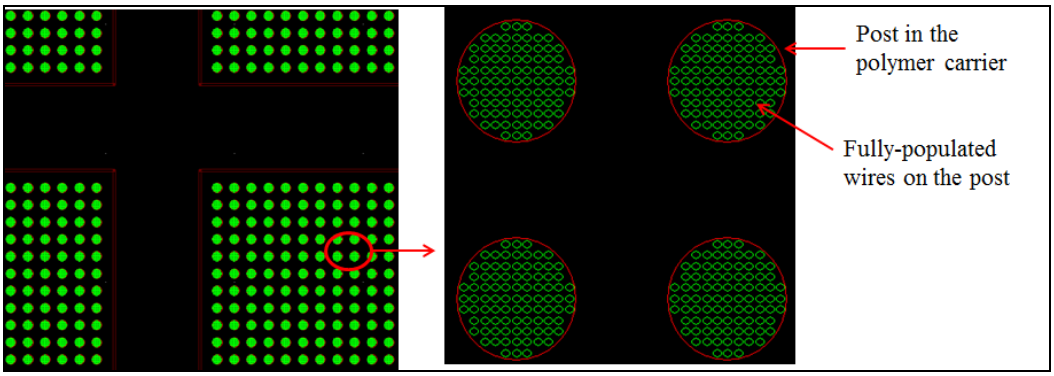


Figure 4.11 Design of copper wires on the posts.

Figure 4.12 Copper wires plated on the posts with overplated mushroom pads.

SAC 305 solder was used as the solder material for the modeling. However, SAC 305 plating is not a standard established process yet. Therefore, eutectic SnAg alloy (Sn-3.5Ag) was used as an alternative, which can be co-plated on the top of the mushroom pads for assembly. Atotech's solderfill AG800 bath was used for plating, with a current density of 1.5 mA/cm^2. The calculated plating rate was 0.75 µm/minute. In order to achieve reliable bonding and accommodate the non-planarity of the carrier, a solder thickness of 20 µm is targeted. .

One potential challenge is to remove the photoresist residue in between the wires. Photoresist breaks into small pieces in the stripper, which remained in the structure due to the small spacing in between the wires, and the mushroom pad covering the top, as shown in Figure 4.13. A different stripper which can dissolve the photoresist can be explored to better remove the residue.

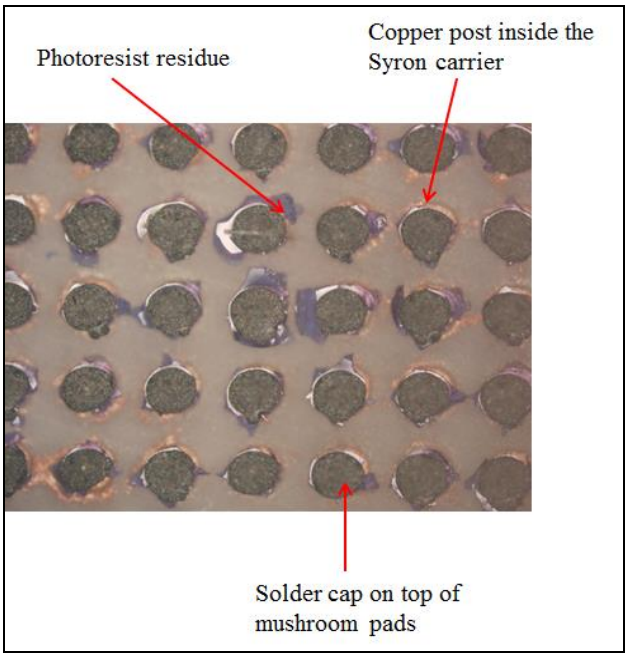


Figure 4.13 Top view of the polymer carrier after solder plating.

As discussed in Section 4.3, controlling the plating rate of the copper posts within the Syron carrier across the 6''×6'' carrier is very challenging. Therefore, the plated posts had a rough surface. The rough and non-uniform copper surfaces weakened the adhesion of the wires onto the posts, and caused detachment of the wires from the posts during resist stripping, as shown in Figure 4.14. In this figure, the wires were slightly misaligned from the posts, and left footprints on the polymer surface in the vicinity of the posts.

Figure 4.14 Surface of plated copper posts in the Syron carrier.

Two approaches were explored to improve the adhesion strength of the wires onto the posts. The first approach is to smoothen the post surfaces by a microetch process. As shown in Figure 4.15, the surface texture was improved by microetch, however, the acid etch is isotropic in nature, and could not planarize the surface completely. The second approach is a mechanical cut to remove the extra copper plated above the polymer surface. The mechanical surface planarization was performed by Disco with the DAS8930 Automatic Surface Planer. The mechanical planarization is illustrated in Figure 4.16, where the excess copper was removed by a diamond bit. The height of the posts after planarization was controlled within 3-3.3 μm above the polymer surface, and the roughness of the post surfaces was significantly improved, as shown in Figure 4.17.

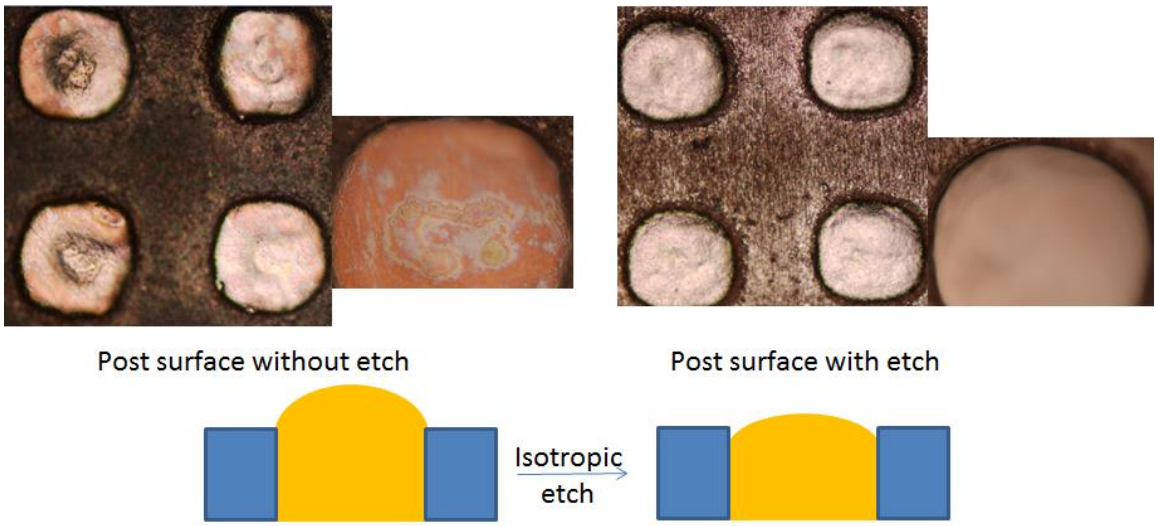


Figure 4.15 Surfaces of the posts before and after isotropic microetch.

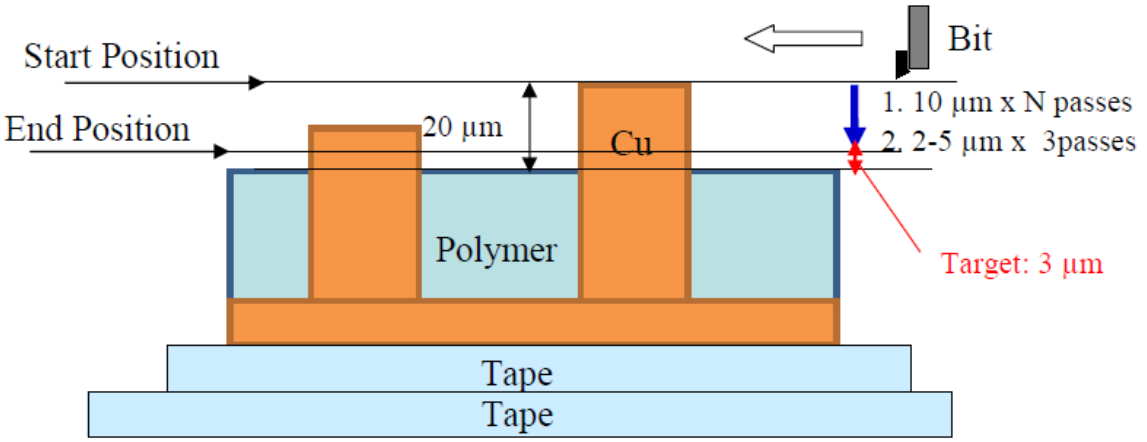


Figure 4.16 Process illustration for mechanical planarization.

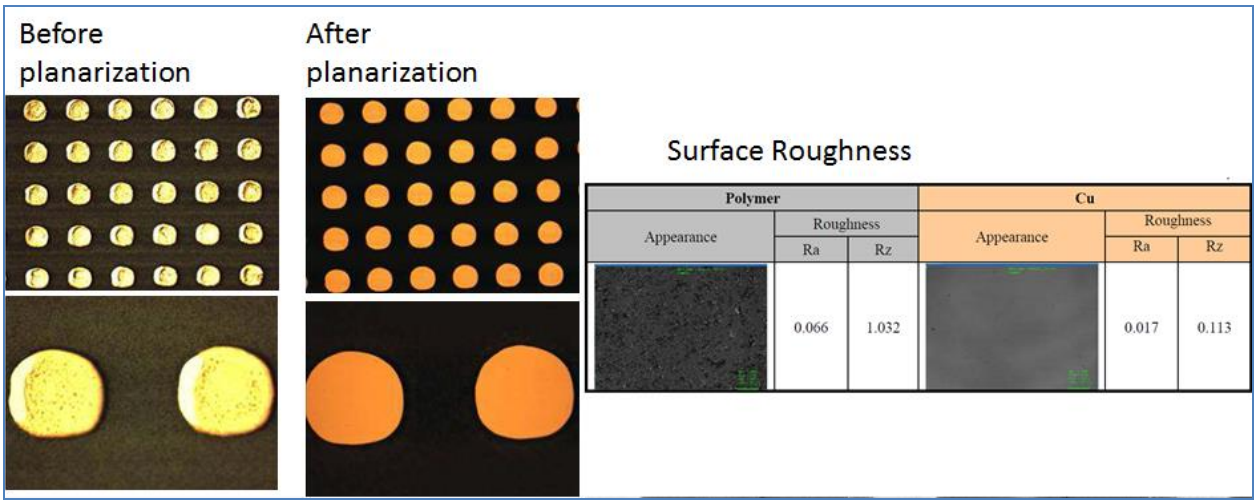


Figure 4.17 Surface roughness before and after planarization.

The mechanical planarization promises better results compared to the isotropic acid etching, although it increases process complexity and the turnaround time. The microetch process could be fulfilled in-house and was applied to the initial set of samples. Figure 4.18 shows the cross-section of the MWA interconnections where the posts were treated with acid etching. The interconnections comprise of polymer carrier with embedded copper posts, copper wires on both sides, overplated mushroom pads, and co-plated solder cap. As can be observed from the cross section, the posts still protruded from the polymer surfaces on the top side. The dryfilm photoresist conformed to the protrusion during roll lamination, and yielded lower resist thickness on top of the posts. Therefore, the filling of the wire openings with bottom-up electrolytic plating was faster on the top

side compared to the bottom side, which then generated thicker mushroom plating over the top.

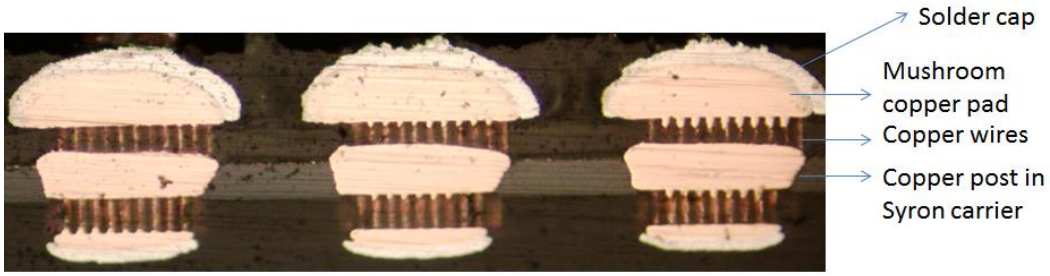


Figure 4.18 Cross section of MWA interconnections.

4.7 Fabrication of the silicon package and the printed wiring board

Solder-mask-defined (SMD) design was used for the silicon package, as shown in Figure 4.19. The diameter of the copper pads is 344 μm, and that of the nitride passivation is 225 μm, which is about 10% smaller than the bump diameter for optimal joint shape and reliability as per BGA design standard. The silicon package was fabricated from 6'' silicon wafers with 600 μm thickness. Semi-additive method was used for wafer processing, which includes seed-layer deposition, lithography, electrolytic plating, passivation deposition, passivation etch and surface finish.

Titanium was first deposited to improve the adhesion of the copper seed layer, and 0.5μm-thick copper was then sputtered on top of the titanium. Hitachi 5315 (15 μm thick) photoresist was used to pattern the copper pads and traces with an exposure dose of 90mJ/cm^2. The same development solution (3 wt.% sodium carbonate) and tool (from CHEMCUT Corp.) as that for SA films was used, with a conveyor speed of 50 inch/minute. Copper with 12 μm thickness was plated through the photoresist openings to form the traces. Plasma enhanced chemical vapor deposition was used to deposit nitride layer as the passivation, and the passivation was then patterned with SF_6 and O_2 plasma. ENIG was used as the surface finish, where 5 μm nickel was plated as the barrier layer,

with 50 nm immersion gold on top to prevent oxidation and also enhance solder wetting. The top view of the silicon package after surface finish is shown in Figure 4.20.

The printed wiring board has matched daisy-chain design with 90° rotational symmetry with the silicon package, as shown in Figure 4.21. The copper traces were patterned by an etch-back method, while solder mask was used for the passivation, and OSP was applied as surface finish. An NSMD design was used for the board, where the pad diameter is 231 μm, and the passivation opening is 344 μm. As per the industry design rules for package-board applications, NSMD is commonly used for board design, while SMD is used for the package design.

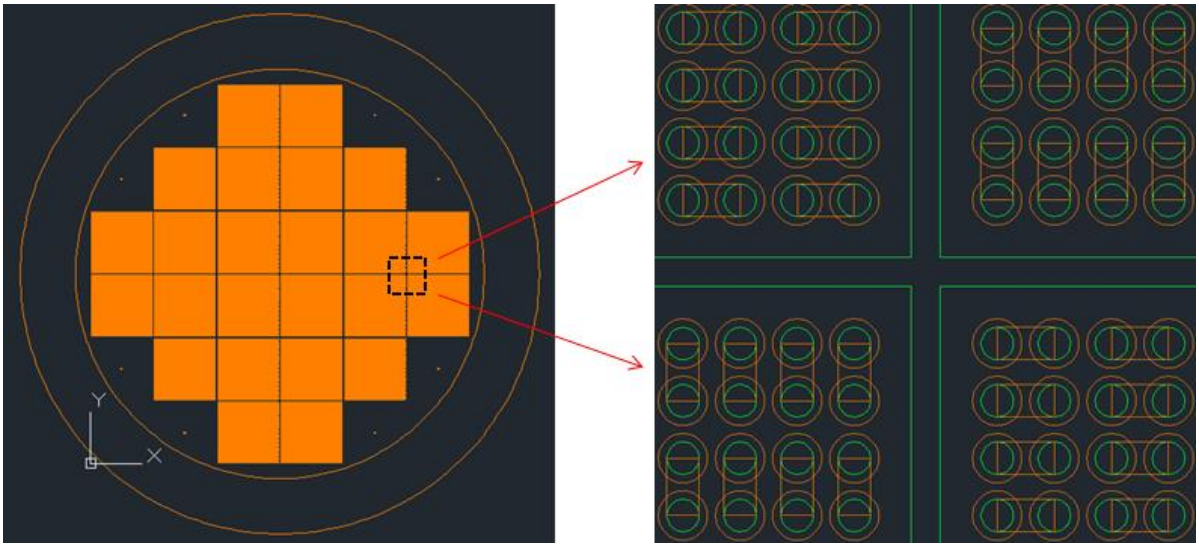


Figure 4.19 Design of the silicon package.

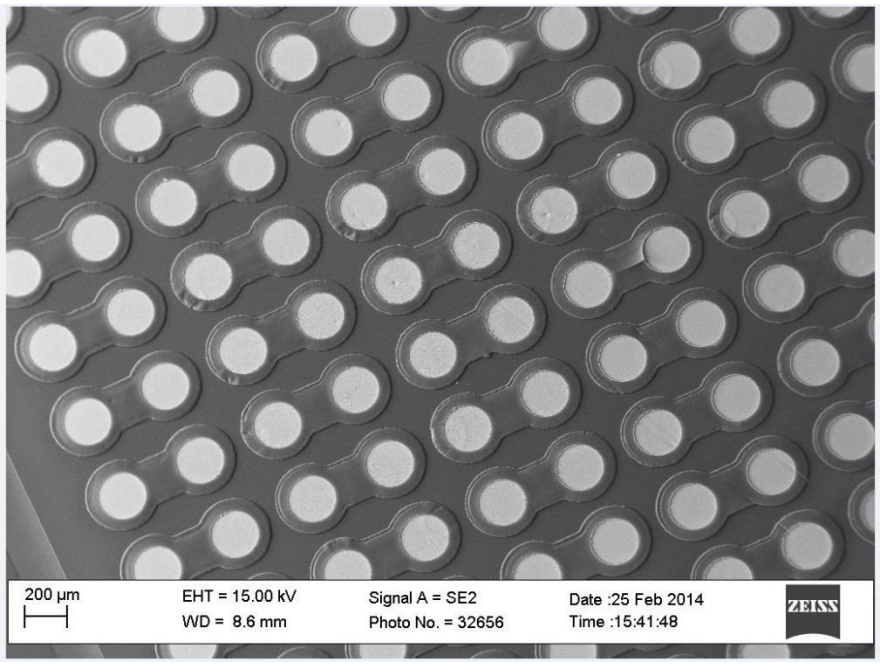


Figure 4.20 Silicon package with ENIG surface finish.

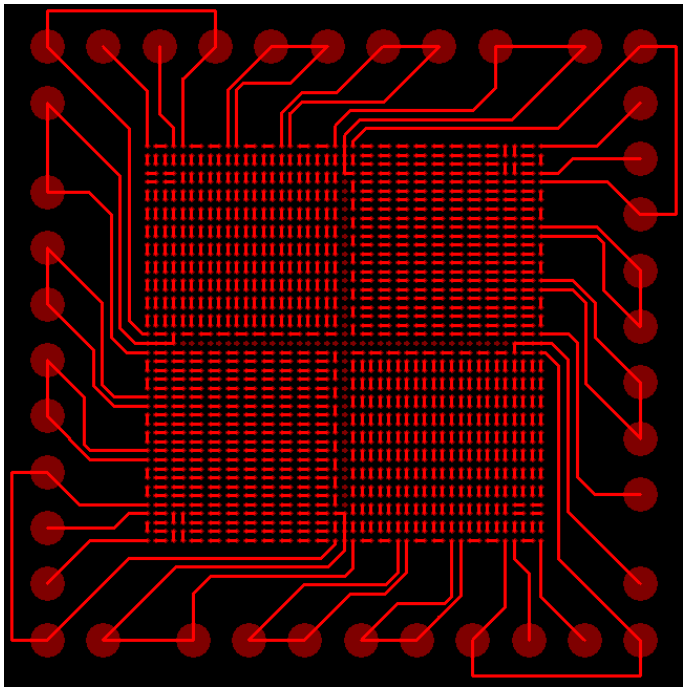


Figure 4.21 Design of the printed wiring board.

4.8 Summary of the test vehicle fabrication

Based on the design inputs from finite element modeling, a packaging-compatible fabrication process based on dry-film photoresist was designed. Syron 7000

thermoplastic polymer was chosen as the carrier material. Copper microwires of 50 μm height and average diameter of 12 μm were fabricated on both sides of the carrier. Silicon packages and FR-4 printed wiring boards with daisy chain designs were fabricated for assembly and reliability test.

CHAPTER 5

ASSEMBLY AND RELIABILITY ASSESSMENT

This chapter describes the assembly process and reliability characterization of the MWA interconnections. The critical geometry and material parameters of the fabricated samples which are different from the original design will be discussed in detail, to study their effect on the reliability performance of the interconnections.

5.1 Assembly of the silicon package on PWB with MWA

The assembly was carried out with a semi-automated flip-chip bonder (Finetech Matrix Fineplacer), with a placement accuracy of ±3μm. A two-step process was developed to assemble the silicon package to the printed wiring board with MWA interconnections, as shown in Figure 5.1. The first step is to place the MWA onto the board (Figure 5.1a), using a vacuum-locked 20 mm × 20 mm gimbal tool. The Syron carriers with copper wires and solder bumps plated on both sides were not ideally flat. Tacky flux (ALPHA NCX-FD) was applied to the board to hold down the carrier. ALPHA NCX-FD flux is a non-clean flux that does not leave residues, and is compatible with lead-free applications which require higher reflow temperatures. The amount of flux has to be carefully controlled to avoid heavy degassing, which may cause voids in the solder joints. External force was also applied to offset the non-coplanarity of the carrier. The applied force was limited to below 5N to avoid damage in the solders. However, it only partially solved the problem. Some of the severely warped samples had corners lifted from the board after placement. An example of the Syron carrier placed on the PWB is shown in Figure 5.2.

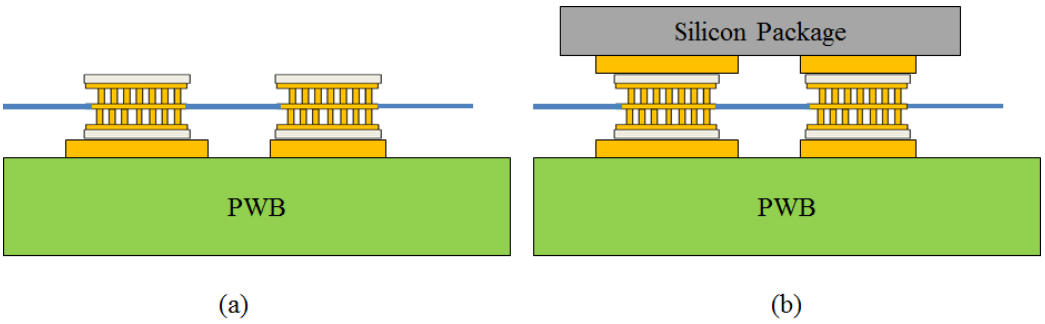


Figure 5.1 Two-Step assembly process: (a) placement of the MWA interconnections onto the PWB, (b) placement of the silicon package, and reflow.

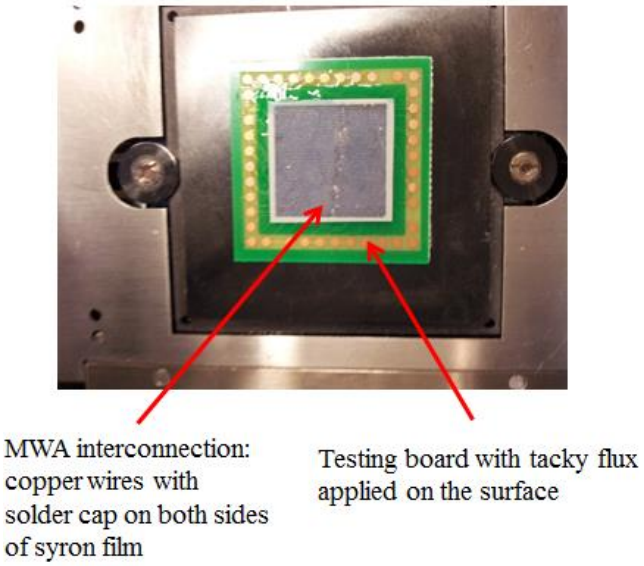


Figure 5.2 Syron carriers with MWA interconnections placed on PWB.

The silicon package was then picked up with a 10 mm × 10 mm flat tool head, aligned onto the MWA interconnections, and pressed on top with a 5N placement force. The joints on both sides were simultaneously formed during reflow of the solder. External force was applied during the reflow process, to offset the warpage and non-coplanarity of the sample, as shown in Figure 5.3. The olive –colored line shows the designed temperature profile, applied on both the heating plate and tool head. Although the tool head is smaller than the silicon package, the temperature gradient across the package is insignificant due to the thickness of the package and the high thermal

conductivity of silicon. According to the datasheet, the activation temperature for the flux is 110°C, maintained for at least 30s. As the melting point of the eutectic 96.5Sn3.5Ag alloy is 221°C, the peak temperature was thus set to 260°C, following standard lead-free reflow metrics. The temperature was first raised to 110°C with the dwell time of 30s to activate the flux, and then raised to the peak temperature. The assembly was finally cooled down to room temperature. The ramp rate for all stages was 2°C/s, which is the maximum capability of the equipment. The blue line and green line show the temperature measurement of the plate of the flip-chip bonder (close to the board temperature) and that of the tool head (close to the silicon package), respectively. In this specific example, an external force of 5N was applied during the placement of the silicon package, and the force was reduced to 2N during the reflow.

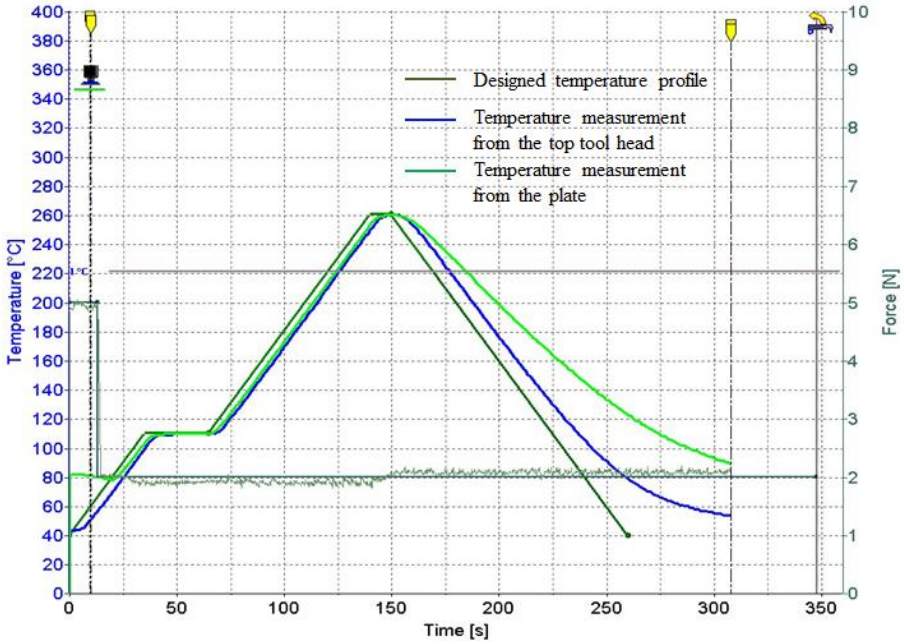


Figure 5.3 Temperature and force profile for reflow.

5.2 Challenges with assembly and processing defects observed after assembly

Major challenges come from the warpage of the Syron carrier, and the non-coplanarity of the plated solder bumps. The warpage of the Syron carrier is caused by: (1) the low thickness and modulus of the polymer material, which makes the stand-alone film

prone to deformations during the fabrication process; (2) the asymmetry in the structure on both sides of the polymer film, which is induced by the missing bumps and unbalanced copper and solder plating. These two aspects are interrelated, since the intrinsic deformation in the thin Syron film led to non-ideal contact between the photoresist and the mask during lithography in some locations, and therefore incomplete resist development, non-plating or weak adhesion of copper wires, and missing interconnections in the affected areas.

The non-coplanarity is primarily caused by the non-uniform current distribution in both the copper and solder plating processes. The difference in copper plating rates generated mushroom pads of different diameters and thicknesses, which subsequently affected the plating rate of solder on these copper pads. The plating non-uniformity of the solder itself further exaggerated this concern. Plated solders with thickness of as large as 84 μm has been observed, as shown in Figure 5.4. The large height variation prohibited proper landing of all solder caps and degraded the assembly yield of the daisy chains. As shown in Figure 5.5, the difference in solder sizes within one sample is still quite severe. When the external force applied during assembly is too large, the interconnections with larger solder volume tended to spread sideways, sometimes to the point of bridging. However, if the applied load is too small, the smaller solders could not land. Forces of 2-5N were found to be the optimal range which ensured both sufficient landing and minimum solder spreading.

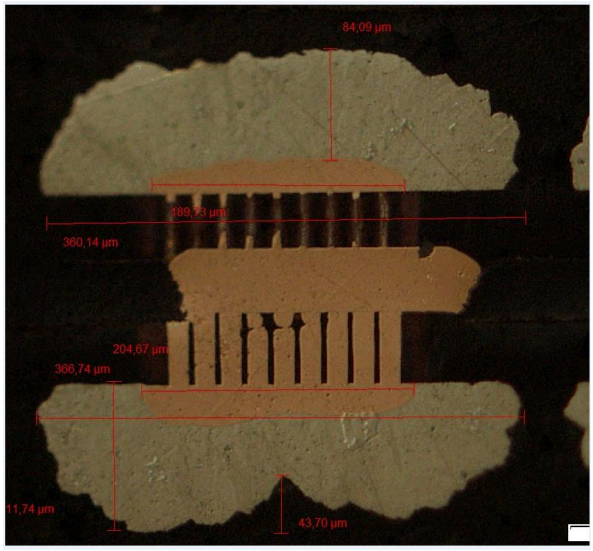


Figure 5.4 Non-uniform and erratically plated solder.

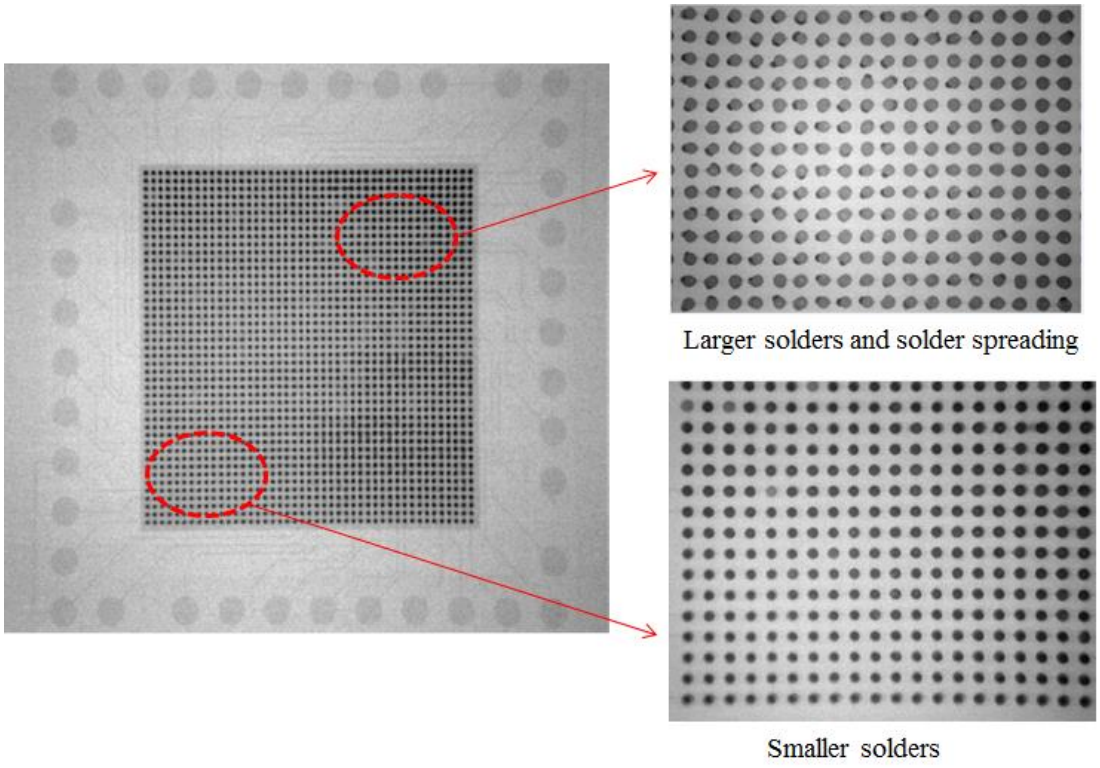


Figure 5.5 X-ray image of the solder bumps after assembly.

Due to the challenges discussed above, four major types of defects were observed after assembly, as shown in Figure 5.6. The first one is misalignment, which is caused directly by the warpage of the carrier. The overall surface could only be partially in focus during alignment and bonding, which affected the alignment precision between the solder

and the pads on the silicon, and caused solder spreading sideways in some of the interconnections.

In locations where there were missing bumps, the carrier flexed and warped locally, especially at higher temperatures. This local deformation created larger gap in one side and narrower gap in the opposite side. In the location where the gap is larger than adjacent areas, the carrier created tensile forces in the interconnections, and pulled the wires out from the copper posts in severe cases (Figure 5.6 b). While in locations where the gap is narrower, or where the solder joints were larger, bridging was observed in between adjacent interconnections (Figure 5.6 c).

The voiding defects (Figure 5.6 d) were related to both the contaminants on the copper pads prior to solder plating, and the erratic solder shape, such as the crevice on the bottom solder shown in Figure 5.4. The degassing of flux and the OSP surface finish also contributed to the voids. Up to 25% of void volume is accepted by industry. Samples with large voids are subjected to early failures.

In samples with comparatively better coplanarity and solder quality, successful assembly was achieved by the two-step process. The cross-section images of the silicon package-MWA-PWB assembly with both planarized and non-planarized samples are shown in Figure 5.7. With the mechanical planarization, the height of the posts was controlled at the polymer surface, and therefore the wires on both sides had identical height. In the samples without planarization, the height of the wires on the plated-up or protruding side was shorter than the other side.

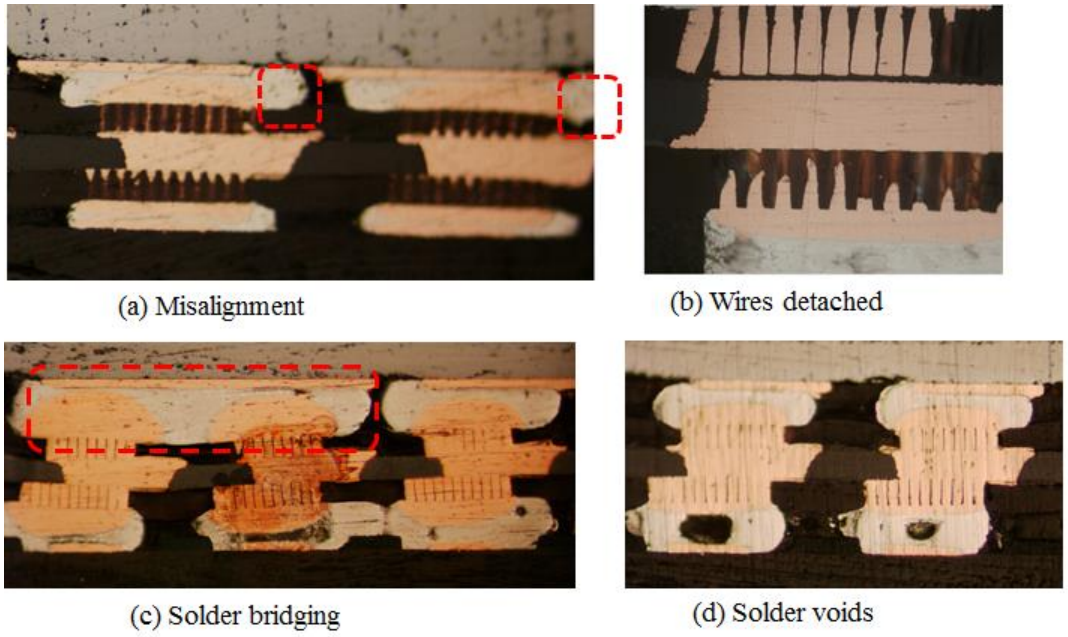


Figure 5.6 Processing defects observed after assembly.

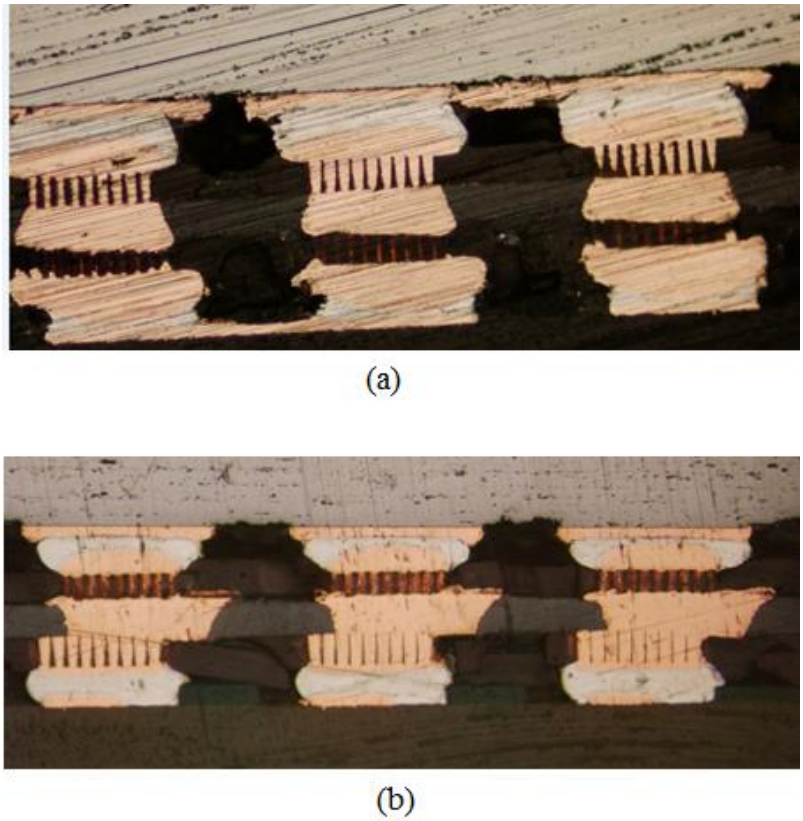


Figure 5.7 Cross section of silicon package-MWA-PWB assembly (a) Sample without mechanical planarization, (b) Sample with mechanical planarization.

5.3 Reliability assessment

Thermal cycling tests were used to assess the reliability performance of the MWA interconnections. The temperature range was from -40°C to 125°C, with 15min dwell time at each temperature extreme, at a rate of 1 cycle/h, as per JEDEC standard (JESD22-A104D, type G). The temperature profile is shown in Figure 5.8. The resistance of each daisy chain was measured every 50 cycles.

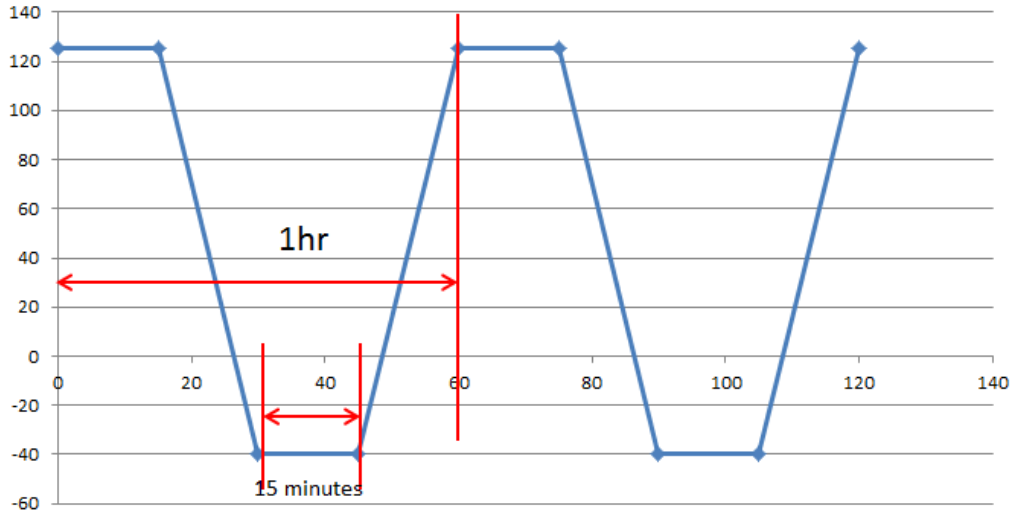


Figure 5.8 Temperature profile of thermal cycling test.

5.3.1 Reliability performance analysis

The resistance measurement of sample#1 is shown in Figure 5.9. The initial failure was detected in DC #7 at 700 cycles. DC #13 and 14 survived 800 cycles before a dramatic increase in resistance. Figure 5.10 shows the location of the failed daisy chains in sample #1. The chain that failed the earliest, DC #7, is one of the corner daisy chains, while DC #13 and #14 are longer chains that are located more towards the inner area, which is expected since the interconnections at the corners experienced higher strains. The sample was cross sectioned for detailed analysis.

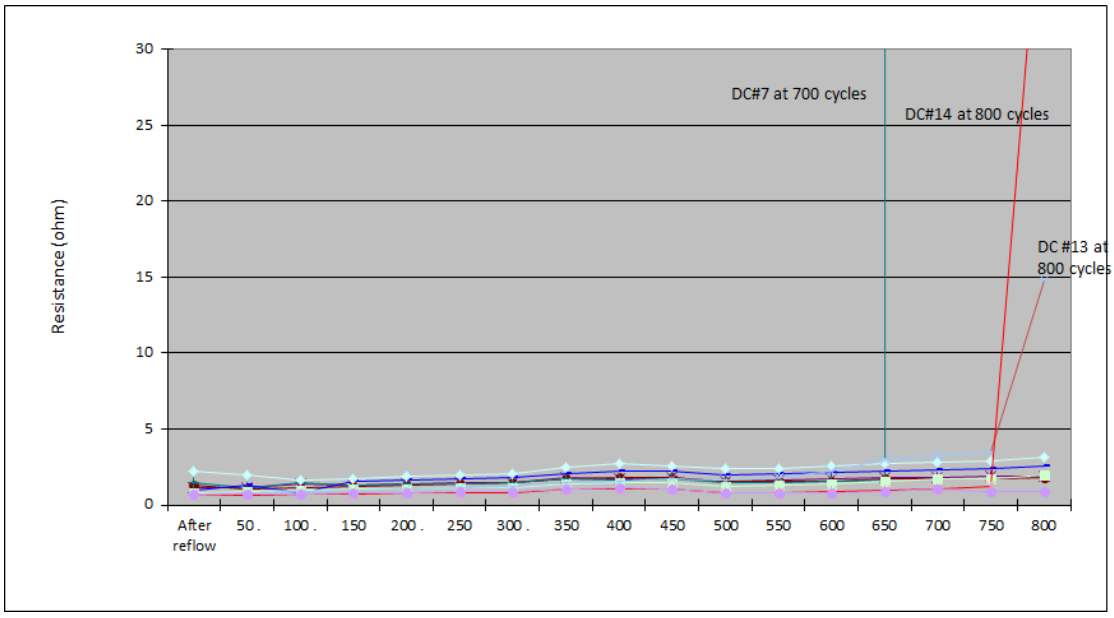


Figure 5.9 Resistance measurement of sample #1.

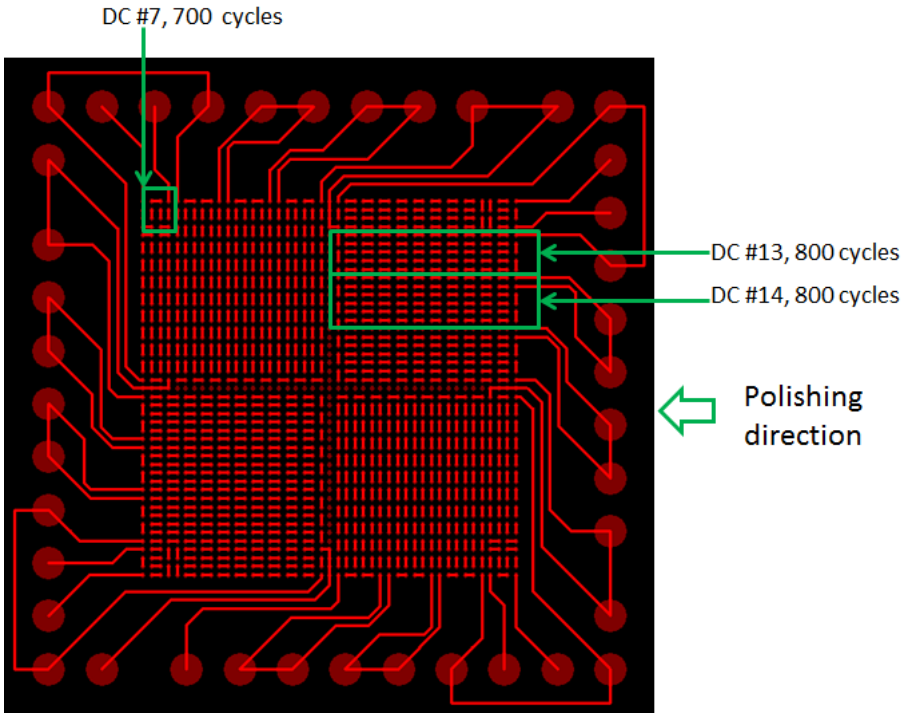


Figure 5.10 Location of failed daisy chains in sample #1.

The sample was underfilled before epoxy-molding for cross-sectioning to prevent smearing of copper wires and solder joints during polishing. The polished direction is shown in Figure 5.10 since most failures were identified along this edge. Figure 5.11

shows the interconnections located in daisy chain #13. The solder on the interposer side showed fatigue cracks, which propagated along the diagonal direction. Two reasons may have contributed to the way the crack propagates. The first one is the warpage of the carrier itself, which pulled the solder joints in the vertical direction. The second reason is the imperfect alignment between the solder and the capture pads on the silicon package (shown in Figure 5.11), which caused necking in the joints and accelerated crack initiation. In the interconnections towards the middle (Figure 5.12), the crack has not propagated through the solder joints, since the thermo-mechanical loading on these interconnections is smaller compared to the corner ones.

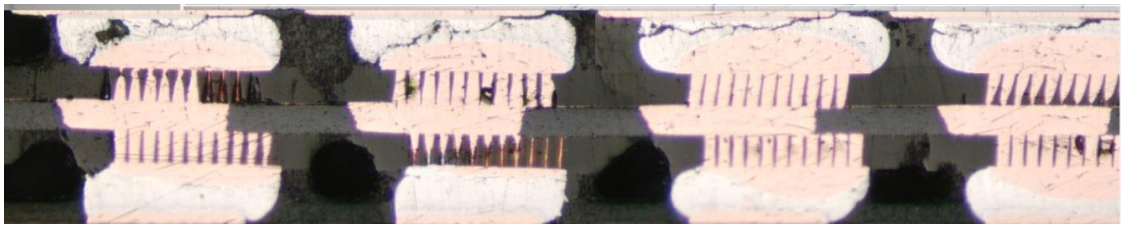


Figure 5.11 Interconnections located in daisy chain #13.

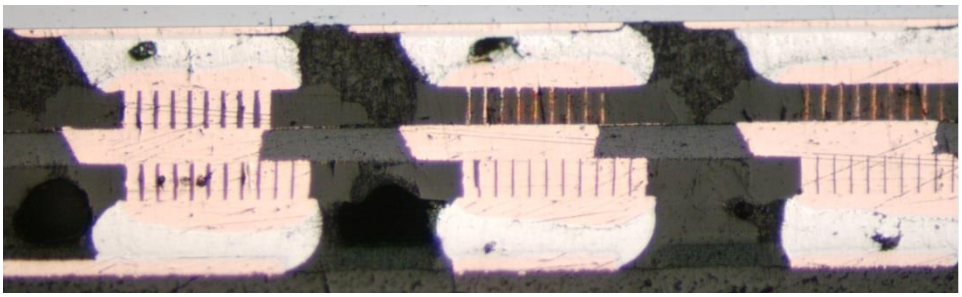


Figure 5.12 Interconnections towards the middle.

5.3.2 Early failures induced by processing defects

Figure 5.13 shows the resistance reading of sample #2. A dramatic increase in the daisy chain that connected the edge bumps was detected after 400 thermal cycles, much earlier than the failure detected in sample #1. The sample was cross-sectioned for failure analysis. As shown in Figure 5.14, the cracks were located in the solder joints on the silicon interposer side. The solder volume on this side was found to be significantly less

than that on the board side. The insufficient solder volume could be caused by non-uniform solder plating, as discussed in Section 5.2. To determine the origin of the crack, the sample was etched in a 3% HCl in ethanol solution to remove the solder on the sample surface and expose the intermetallics. The crack seems to propagate along the IMC phase, as shown in Figure 5.15. EDS analysis shows a copper atomic ratio of about 38%, and tin of 58%, which represents a combination of Cu_6Sn_5 intermetallic compound and Sn. Therefore, the crack was located at the interface of IMC layer and the solder, rather than inside the solder bulk. The IMC phases have very different mechanical properties compared to the solder bulk phase, which makes the IMC/solder interface intrinsically highly-stressed and prone to crack, as described in Chapter 2. The low solder volume resulted in higher volume ratio of the IMC phases, and less deformation was accommodated by the bulk solder, with more stress translated to the IMC/solder interface. Moreover, the finite element modeling suggested high strain concentration on the silicon package side, compared to the board side. The low solder volume, high stress at IMC/solder interface, and high strain on the package side, resulted in early failure of the interconnection.

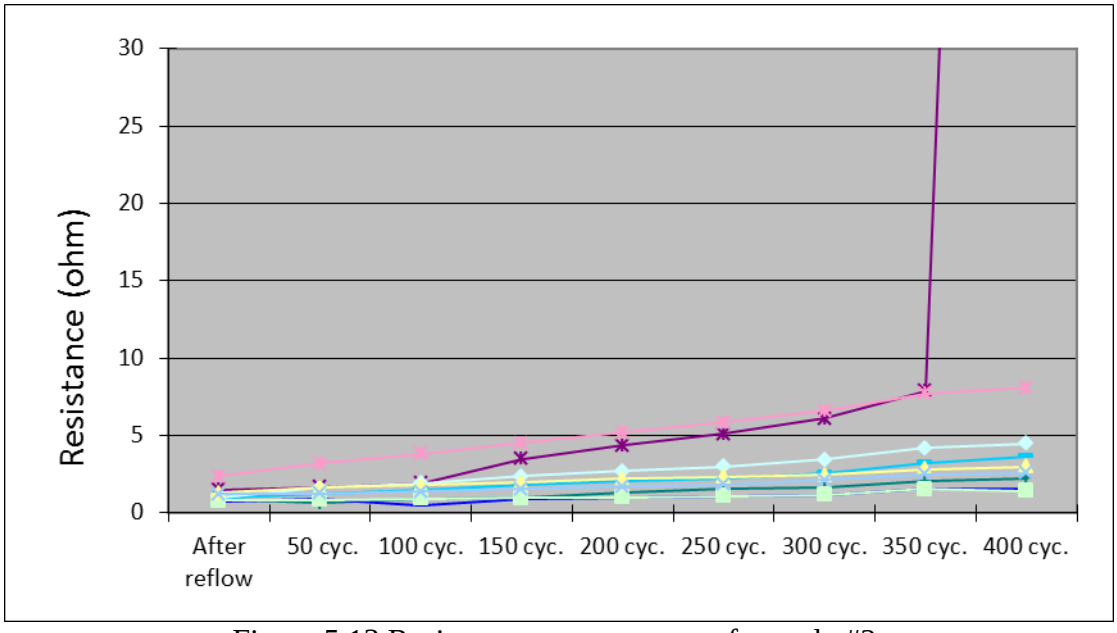


Figure 5.13 Resistance measurement of sample #2.

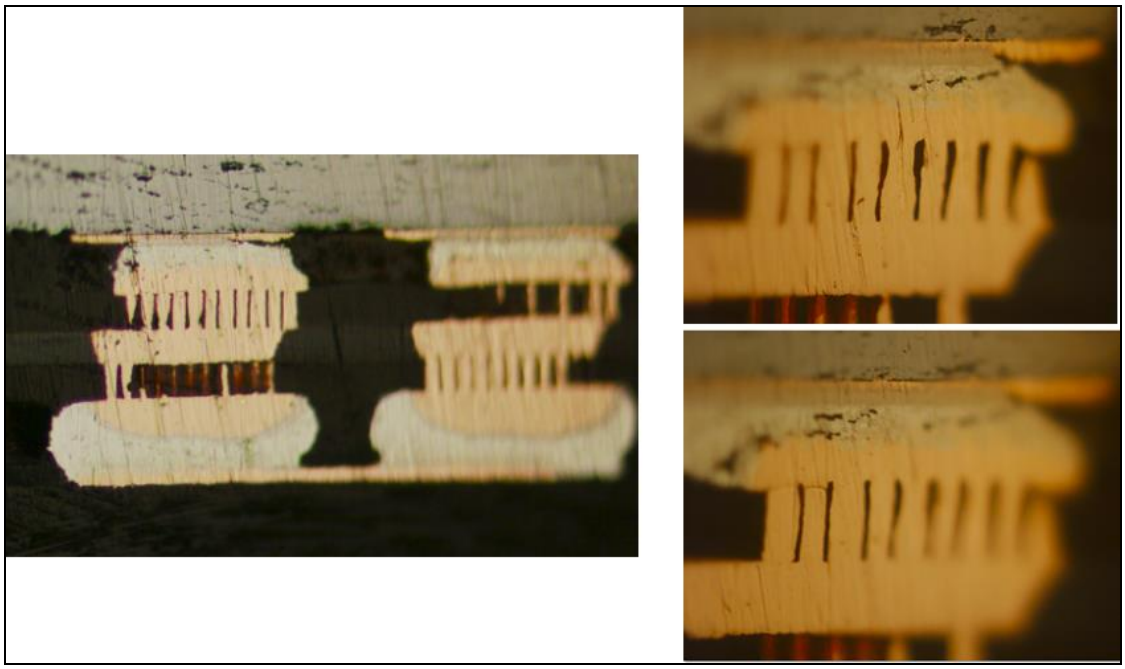
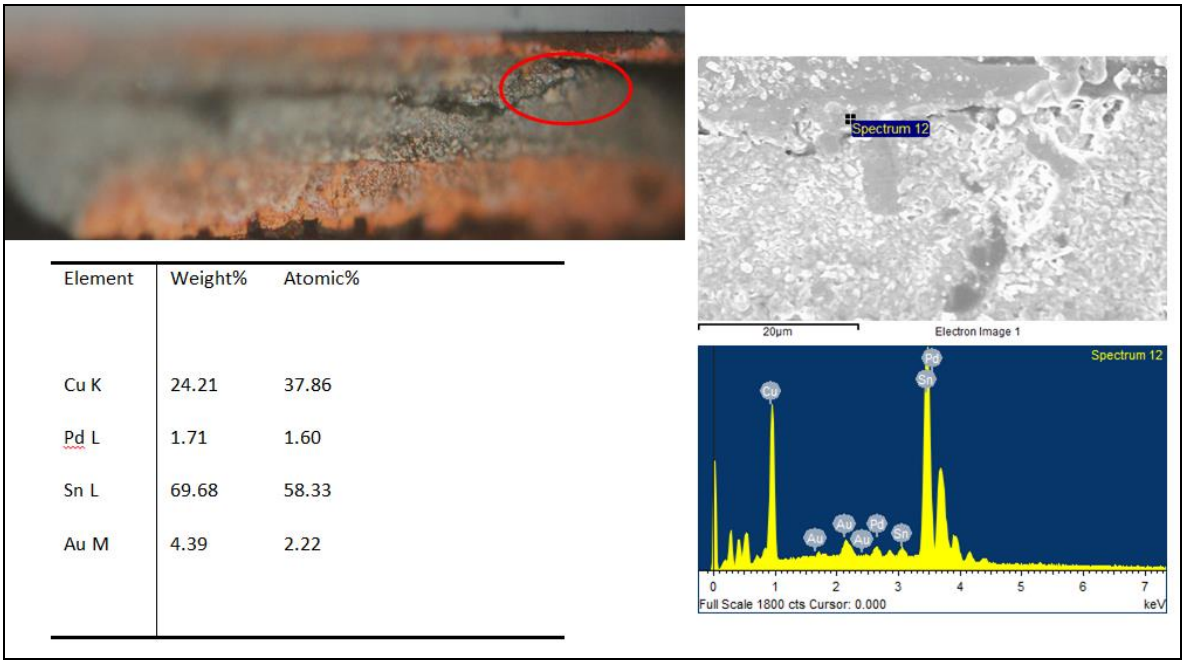


Figure 5.14 Cross section of sample #2 at 400 cycles.



Element	Weight%	Atomic%
Cu K	24.21	37.86
Pd L	1.71	1.60
Sn L	69.68	58.33
Au M	4.39	2.22

Figure 5.15 SEM and EDS analysis on etched sample.

5.4 Analysis and discussion

From the results, it can be observed that the warpage of the polymer carrier and non-coplanarity of the solder joints not only created assembly challenges, but also caused

defects that led to early failure of the interconnections. In spite of these defect-induced failures, in the regions with comparatively less warpage and better coplanarity, the interconnections were able to survive 700 cycles prior to the initial failure. As discussed in Chapter 4, some design trade- offs were made in processing and in materials, such as using thick silicon packages (600 µm other than 100 µm) and larger wire diameters (15 µm other than 10 µm). This section reviews in detail the critical material and geometry parameters in the fabricated samples, and how they affected the reliability of the interconnections.

5.4.1 Analysis of critical material parameters

Characterization of mechanical properties of the plated copper wires: The mechanical properties of the electroplated copper vary significantly due to different plating conditions, which result in different microstructures. The mechanical properties of the copper wires are critical since they determine the fatigue behavior of the wires under thermo-mechanical loading. Three types of samples were studied: the copper wire interconnections after assembly, the copper wire interconnections before assembly, and the copper wires annealed at 150°C for 1000 hours after plating. The samples were characterized by a nano-indentor (Fisherscope H100C) at Atotech, Germany. The indentation depth was ~ 0.15 µm, and the maximum load was 10 mN, as per ISO 14577. The samples are labeled as following for easier reference:

S1: Assembled

S2: Non-assembled, non-annealed

S3:Non-assembled, annealed at 150°C for 1000 hours.

The samples were molded and cross-sectioned prior to nano-indentation. The indentation locations in sample S1 is shown in Figure 5.16. The test was conducted in three locations: 1) top: the over-plated mushroom, 2) middle: the wires, 3) bottom: the

post in the Syron carrier. The test results are shown in Table 5-1. The copper modulus in the wire part was significantly lower compared to that in the top and bottom posts. However, it has to be noted that the testing results are affected by the material surrounding the indent location. The wire part has the smallest dimensions, and the wires deformed as three-point-bending when the indentation force was applied. Therefore, the measurements were more affected by the epoxy molding compound around it, thereby showing the lowest modulus. Similarly, the bottom part, which is surrounded by the polymer carrier, showed lower modulus than the top part which has solder and silicon in its proximity. The bottom and top part comprises of copper pads that are much larger in dimension, and less affected by the surrounding materials. The plated wires and the over-plated post show the same microstructure in the SEM (Figure 5.17), and are expected to have the same mechanical properties. Therefore, the measurement from the top part is assumed to represent the modulus of the whole structure. In the as-plated samples, this corresponds to about 113GPa modulus, and the hardness is about 127 HV. Similar analysis was performed for sample S2, and S3.

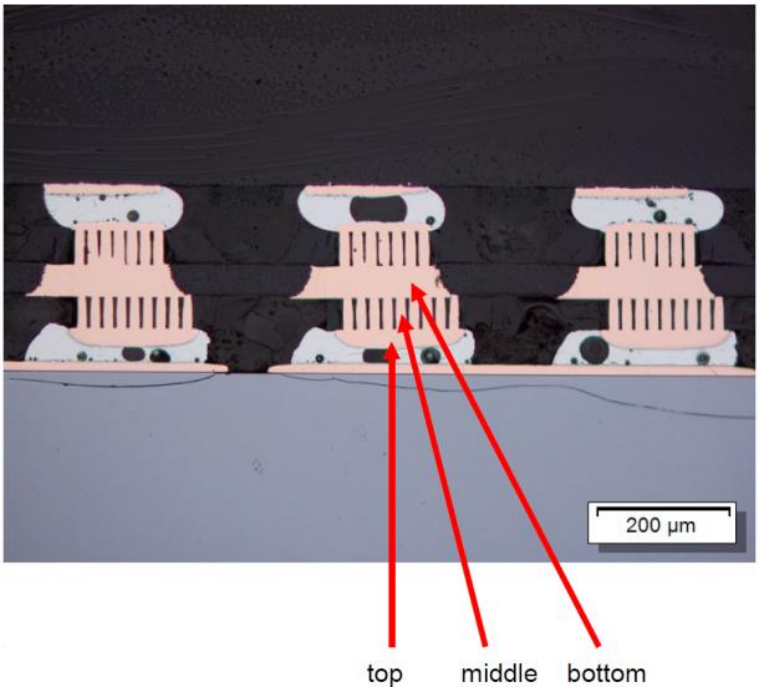


Figure 5.16 Indentation locations in the as-assembled sample.

Table 5-1 Indentation test results from the as-assembled sample.

Location	Modulus [GPa]	Hardness [HV]
Top	113	127
Middle	52	118
Bottom	106	125

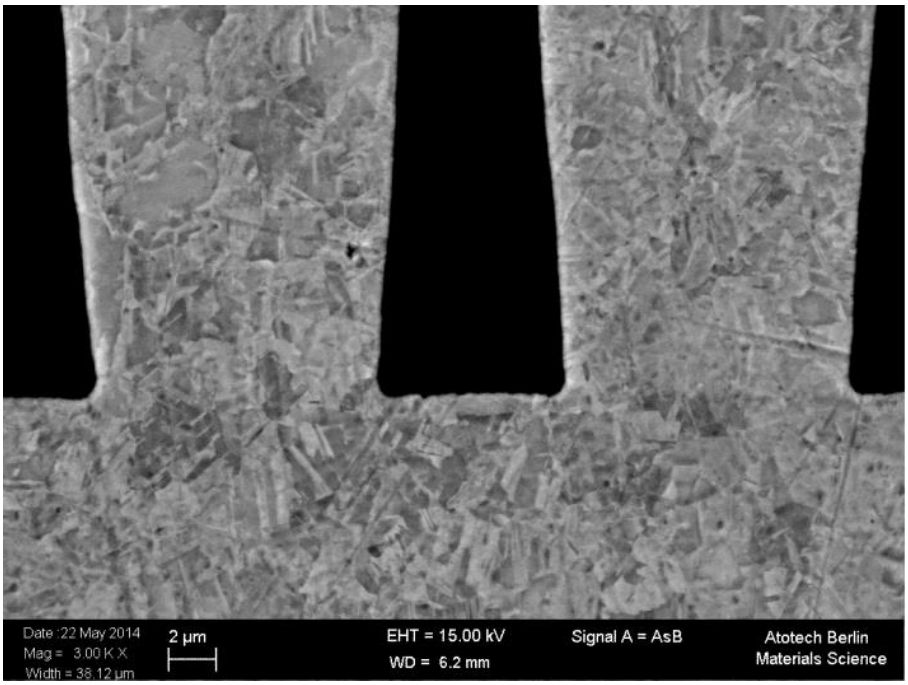


Figure 5.17 Copper microstructure in the as-assembled sample.

Different indentation hardness values were observed in Sample 1-3, as shown in Figure 5.18. The non-assembled, non-annealed sample (S2) had the highest hardness of 167 HV. After annealing at 150°C for 1000 hours, the hardness reduced to 140 HV (S3). The assembled sample had the lowest hardness 127 HV (S1). The reduction of hardness and increase in ductility is due to the recovery and recrystallization phenomenon during annealing. During the assembly process, the interconnections were heated up to the reflow temperature (260°C), which is much higher than the annealing temperature of 150°C. Though the reflow time is much shorter than the annealing time, the assembled samples showed the lowest hardness. The microstructures of plated copper in the three samples are shown in Figure 5.19. Sample S2 (non-assembled, non-annealed) has more elongated grains and smaller grain sizes, while the annealed and assembled samples have polygonal grains and larger grain sizes.

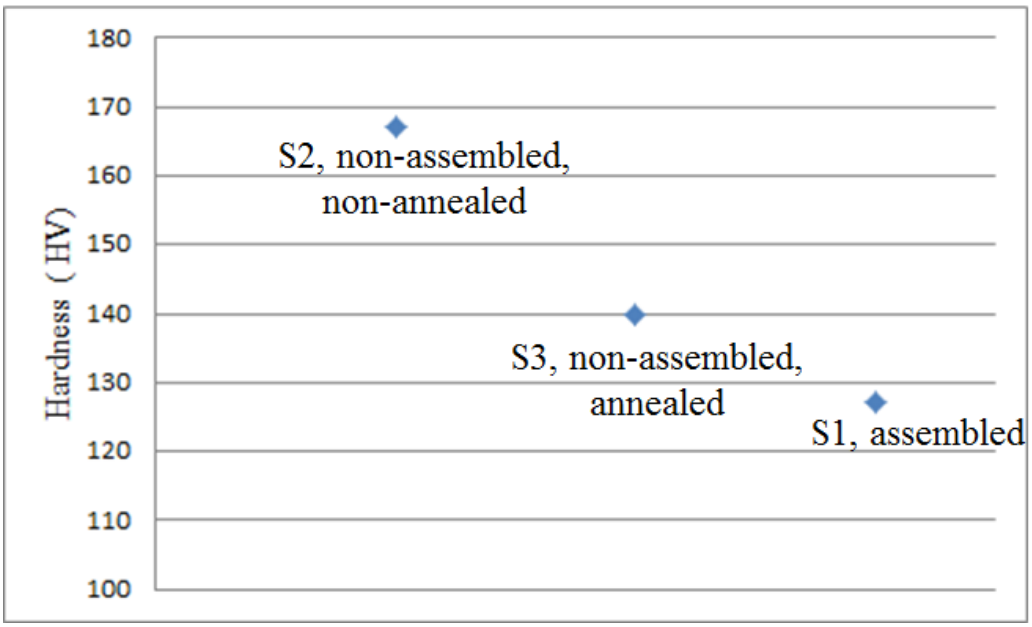
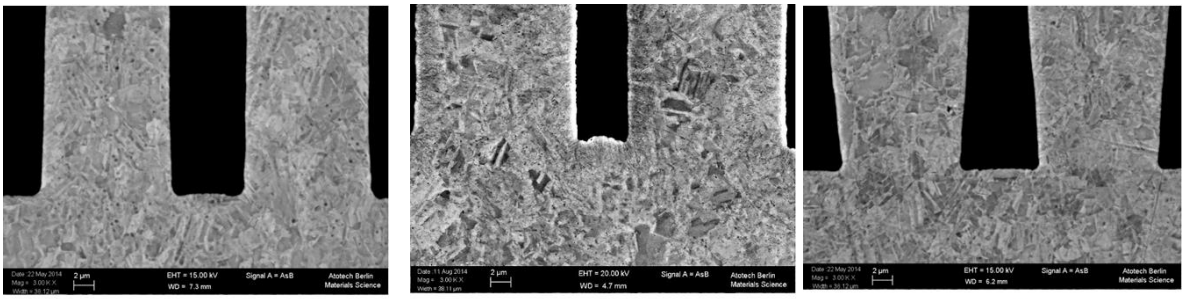


Figure 5.18 Hardness of plated copper in sample 1-3.



S2, non-assembled, non-annealed

S3, non-assembled, annealed at 150°C for 1000 hr

S1, assembled

Figure 5.19 Microstructure of plated copper in sample 1-3.

The grain size of the assembled sample varied from ~2-5 μm. Therefore, Hall-Petch relation is applicable to estimate the mechanical properties of the microwires used in the reliability test (Chapter 2). Gertsman et al. studied the effect of grain sizes on the yield stress of copper for a wide grain size range [59]. When $d^{-1/3}$ is within 0-3 $\mu m^{-1/3}$, where d is the average grain size, the yield stress is proportional to $d^{-1/3}$, as show in Figure 5.20. In the tested samples, the average grain size d is ~3.5 μm, $d^{-1/3}$ is ~ 0.66 $\mu m^{-1/3}$, which corresponds to the yield stress of 185 MPa. The copper properties used in the modeling, 121 GPa modulus and 172 MPa yield stress, therefore, represent the behavior of the copper wires in the actual assembled samples within 10% discrepancy.

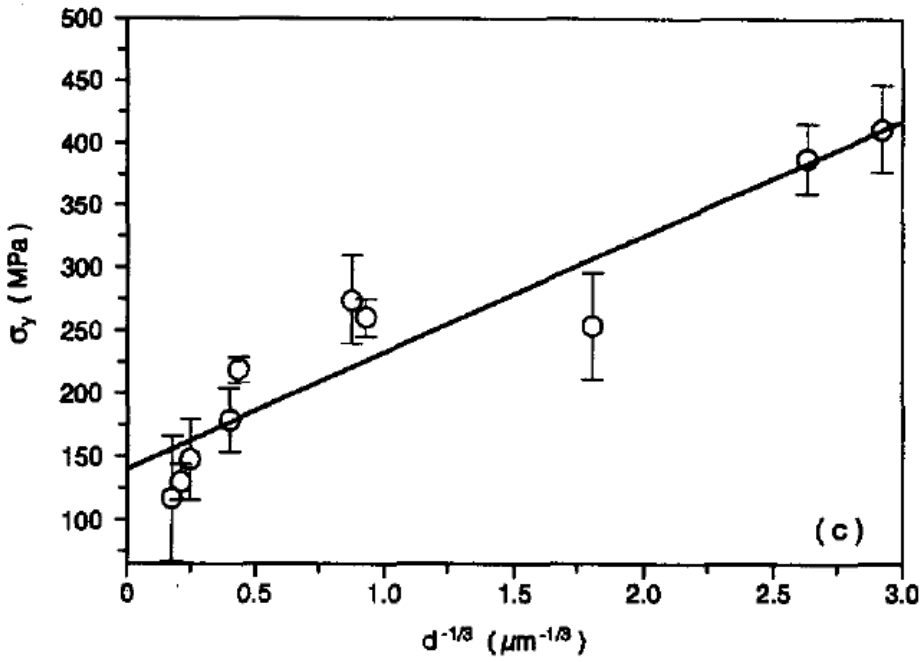


Figure 5.20 Effect of grain size on yield stress of copper [59].

Change in solder material: The solder material used in the original models was SAC305, as it is one of the most popular lead-free solders. However, SnAg eutectic solder (96.5Sn3.5Ag) was used for the actual fabrication because of its processability with electroplating. The two solder materials, however, have different visco-plastic characteristics and fatigue performance. Wang et al. reported the Anand model for 96.5Sn3.5Ag, as shown in Table 5-2 [60].

The low-cycle fatigue performance of 96.5Sn3.5Ag was studied by Kanchanomai et al. in detail [61], and the ductility-modified Coffin-Manson relationship was used for fatigue life prediction of the solder, as shown in the following equation. In Equation (5.1), D is the fracture ductility, which equals to 1.6 for 96.5Sn3.5Ag solder. α and θ are material constants, which are 1.07 and 13, respectively.

$$\left(\frac{\Delta\varepsilon_P}{2D}\right) N_f^{\alpha} = \theta \tag{5.1}$$

Table 5-2 Anand model for SnAg eutectic solder [60].

Constant Number	Anand Constant	Units	96.5Sn3.5Ag
1	s_0	MPa	39.09
2	Q/R	1/K	8900
3	A	sec^{-1}	22300
4	ξ	Dimensionless	6.0
5	m	Dimensionless	0.182
6	h_o	MPa	3321.15
7	$\hat{s}$	MPa	73.18

5.4.2 Analysis of critical geometry parameters

Change in silicon thickness: In the mechanical design (Chapter 3), the thickness of the silicon package used in the models is 100 µm, representing the typical package thickness for 2.5D and 3D architectures. In the fabricated samples, however, the packages are not thinned down, and have a thickness of 600 µm. A comparative model with thicker package was built to study how the package thickness affects the reliability of interconnections.

The geometry of each unit that contains one interconnection is shown in Figure 5.21. Same element sizes, material properties, boundary conditions and loadings as in the original models discussed in Chapter 3 were used in this model. The maximum elemental equivalent plastic strains in both copper and solder, and the corresponding fatigue life calculations are shown in Table 5-3. As the package becomes thicker, it's more rigid and less prone to deformation, which results in smaller warpage of the package. The rigidity of the package significantly increased the strain in both the solder joints and copper wires, and led to the reduction of fatigue life from 1158 cycles to 707 cycles.

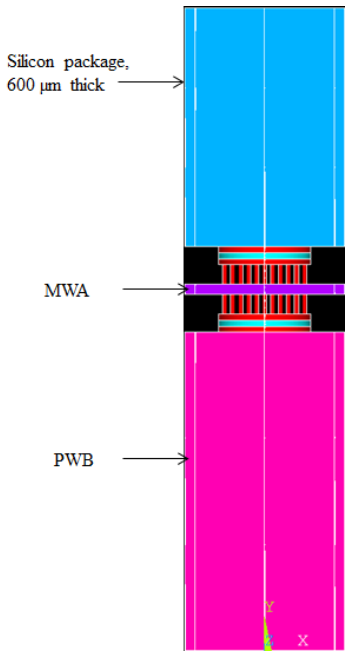


Figure 5.21 Model with 600 µm silicon.

Table 5-3 Effect of package thickness on interconnection reliability.

Thickness of the silicon package	Maximum elemental equivalent plastic strain in solder and the corresponding fatigue life	Maximum elemental equivalent plastic strain in copper and the corresponding fatigue life	Warpage of the package
100 µm	0.785%, 1158 cycles	0.4146%, 1447 cycles	96.97 µm
600 µm	1.04%, 707 cycles	0.46%, 1210 cycles	169.08 µm

Change in wire diameter: Copper wires with 10 µm diameter were used in the original models. However, the mask used in the fabrication had 15 µm wire openings for processability. From the discussion in Chapter 4, with the mask having 15 µm diameter features, the fabricated wires have a diameter of 10-14 µm after seed layer removal, which is ~ 12 µm on average. The wider wires reduced the compliance of the wire arrays, and increased the strain in the solder joints.

Change in carrier thickness: The Syron carrier used in the samples is 50 µm thick, while the original model used 25 µm for the polymer thickness. Thicker polymer carriers are easier to handle and less prone to wrinkles and deformations during processing. At

the same time, the thicker film increases the overall stand-off height of the interconnections.

5.4.3 Effect of the change of material and geometry parameters on interconnection reliability

To understand the effect of the above material and geometry parameters, that are different from original design on the interconnection reliability, a refined model was built. The refined model incorporated the changes in solder material, silicon thickness, copper wire diameter and carrier thickness to better describe the behavior of the MWA interconnections, as shown in Figure 5.22. The same boundary conditions, loading, and element sizes as the original model were applied in the refined model. The maximum elemental plastic strain range per cycle was calculated for estimating the fatigue life. The calculated strain and fatigue life for both solder joints and copper is shown in Table 5-4. Due to the combination of thicker silicon packages and larger wire diameters, the strains in the interconnections are larger compared to that showed in Chapter 3. With the refined model, the estimated fatigue life is 801 cycles, defined by the failure in the solders. As discussed in Section 5.3, the fatigue failure was detected in one of the corner daisy chains at 700 cycles. The calibrated fatigue life calculation is therefore consistent with the experiment data, with less than 15% discrepancy.

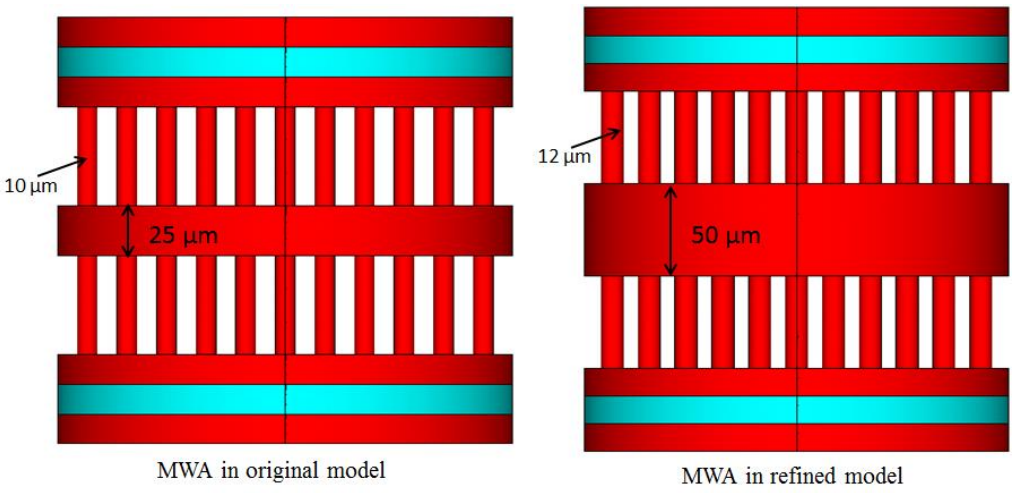


Figure 5.22 MWA geometries in the original and refined models.

Table 5-4 MWA fatigue life calculation with the refined model.

Structure		Equivalent plastic strain range per cycle	Projected fatigue life
Refined model	Solder (SnAg)	0.03249873	801 (from Eqn. 1)
	Copper	0.00498	1066
Original model	Solder (SnAgCu)	0.00785	1158
	Copper	0.00414	1450

5.5 Summary

The assembly and reliability characterization of the MWA interconnections are discussed in this chapter. Despite the challenges resulted from the warpage of the polymer carrier and non-coplanarity of the solder joints, the sample was able to survive 700 cycles prior to initial failure. The critical material and geometry parameters that are different from the original design were reviewed in detailed, and a refined model incorporating these parameters was built to better describe the behavior of the fabricated MWA interconnections. The calibrated fatigue life was 801cycles, which is consistent

with the experiment data with less than 15% discrepancy. The major factor that led to the decrease in fatigue life compared to the original design is the thick silicon, which added to the stiffness of the package and increased the strain in the interconnections. With thinner packages, such as the ones used in today's 2.5D and 3D architectures, the MWA interconnections are expected to survive more than 1000 cycles in accelerated test for 20 mm × 20 mm package size. The MWA interconnections, therefore, provide a SMT-compatible solution for reliable interconnections between the large low-CTE packages and the organic printed wiring board.

CHAPTER 6

SUMMARY AND OUTLOOK

6.1 Research summary

Large low-CTE packages, including silicon, glass and low-CTE organic packages, are needed to enable high interconnection density to achieve high bandwidth in high performance computing applications. These low-CTE packages are also needed for reliability of the ultra-low K on-chip dielectrics. However, all these strategic, large low-CTE packages offer huge CTE mismatch between them and the organic printed wiring board, posing a grand challenge for the reliability of board-level interconnections.

This study investigates an innovative approach to address the reliability challenge using copper microwire array approach. The MWAs benefit from the high aspect ratio of copper wires, leading to low plastic strain and outstanding fatigue performance of the interconnections.

The first part of the study focuses on the design of the interconnections. Finite element method was used to optimize the geometry and material parameters. With copper wires of 10 μm diameter and 50 μm height on both sides of an appropriate polymer film, the model predicted over 1000 cycles of fatigue life for a 20 mm × 20 mm silicon interposer.

The second part of the study explores the processing aspects of the MWA interconnections. A packaging-compatible fabrication procedure was designed. Copper microwires of 12 μm diameter and 50 μm height were developed with low-cost dryfilm photoresists. SnAg solder were plated on both sides of the wires for ease of assembly. Trade-offs of geometry and material parameters of the interconnections were made for processibility. A two-step assembly process was developed to assemble the MWA interconnections between silicon packages and the PWB. Accelerated thermal cycling

tests were used to assess the reliability performance of these interconnections. The initial fatigue failure was identified at 700 cycles, featuring the cracks in the solders on the silicon package side.

A refined model with updated geometry and material parameters was developed to better describe the performance of the fabricated samples. Due to the thick silicon package and wider copper wires, the calculated fatigue life declined to 801 cycles, which correlated well with the experimental data, with less than 15% discrepancy. The finite element models are therefore validated. Based on the validated model, the interconnections will survive more than 1000 cycles if thinner silicon packages are used.

6.2 Future work

The following directions are suggested for future research in this area:

- Assess the reliability of the MWA interconnections with thin silicon and glass packages: The thickness of packages used in today's 2.5D and 3D architectures is usually 100 μm or below, to enable through-package-vias with small diameters. Based on the modeling, thinner packages are less rigid and induce less deformation in the interconnections, which help to improve the reliability performance.
- Explore options to fabricate microwires with higher aspect ratio for larger packages and other more demanding applications: Copper microwires of 12 μm diameter have been achieved in the current study. The wires of 10 μm diameter or below can help to further improve the compliance of the interconnections, and thus reduce the strain in the solder joints.
- Study the single-sided microwire array interconnections (Figure 6.1), as a low-cost interconnection solution for packages with medium sizes or intermediate CTEs: The MWAs can be directly plated on the back-side of the

packages, and assembled on the board with thin solder caps. The single-sided structure eliminates the polymer carrier, therefore avoids the assembly challenges induced by the polymer warpage. Due to the smaller stand-off height and aspect ratio of the copper wires, the reliability performance is expected to be lower than that from the double-sided structure. However, they offer adequate compliance along with improved manufacturability.

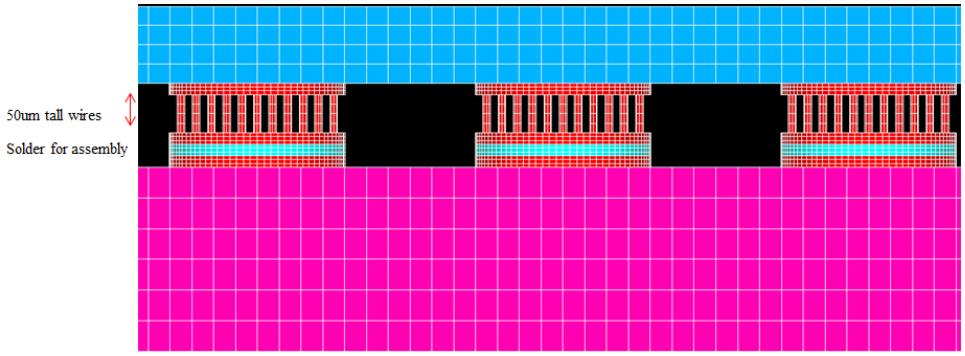


Figure 6.1 Single-sided MWA interconnections.

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