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Olli-Erkki Kursu

MICROMOTION COMPENSATION AND A NEURAL RECORDING AND STIMULATION SYSTEM FOR ELECTROPHYSIOLOGICAL MEASUREMENTS

UNIVERSITY OF OULU GRADUATE SCHOOL;
UNIVERSITY OF OULU,
FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING,
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INFOTECH OULU

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Academic dissertation to be presented with the assent of the Doctoral Training Committee of Technology and Natural Sciences of the University of Oulu for public defence in the OP auditorium (L10), Linnanmaa, on 11 December 2015, at 12 noon

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Abstract

The goal of this thesis was to investigate and build new circuit solutions for electrophysiological measurements that would be used in biophysical research of nervous system and brain activity. The first aim was to build a micromotion compensation system that could compensate for the relative movement of measurement microelectrodes and neurons that can cause signal attenuation or even loss. The purpose of this work was to stabilize the microelectrode with respect to the preparation in order to achieve more stable measurements with small test animals, such as insects, rodents or reptiles. The movement is measured with a touch probe sensor and a feedback loop containing a piezoelectric actuator that adjusts the position of the electrode. A prototype micromotion compensation system was built and its performance was measured in a realistic measurement condition. The compensation system was used to reduce the motion of the probe to below 1 μm, resulting in up to 98% compensation below 10 Hz. The design of the micromotion compensation system took advantage of a preceding study on a piezoelectric bimorph actuator/ sensor structure. This study is also presented in the thesis.

Another aim of the research was to design and build an integrated multichannel neural signal recording system with stimulation capabilities. The circuit was designed to amplify, digitize and stream out data from extracellular neuronal signal measurements. The main target of the measurement system are action potential signals, which are a type of "digital communication" between nerve cells that evolution has produced. The waveform of these action potential signals is the focus of interest. To accomplish this measurement, the developed circuit contains preamplification, multiplexing, post-amplification, A/D conversion and control logic for the A/D converter and data transmission. The circuit is also externally programmable, and it contains DACs for tuning high-pass filter corner frequency, amplifier bias current and stimulation current.

The implemented electronics have low noise, low power and small circuit area. The gain of the circuit is adjustable from 100 to 5000 and the high-pass filter corner frequency from 0.5 Hz to 900 Hz. The sample rate is 20.833 kSps and the data rate is 3.5 Mbps. The measured noise level of the circuit is 7.5 μV (rms) (300 Hz - 10 kHz) and the whole chip consumes less than 2 mW of power. A 16-channel prototype chip with 0.35 μm CMOS technology was manufactured and its performance was measured. Backend electronics containing a microcontroller supporting high-speed USB data transfer was also programmed for the system. The device was tested in real measurements of neuronal signals in a cockroach (*Periplaneta americana*) preparation, and reliable streaming of the recorded data to the PC verified its proper function.

Keywords: action potential measurement, electrophysiology, micromotion compensation, neural signal measurement, neural signal measurement system, neural stimulation

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Tiivistelmä

Tämän väitöskirjatyön tavoitteena oli kehittää mittaus- ja säätöjärjestelmiä aivotutkimuksen ja biofysiikan sovelluksiin. Ensimmäisenä tutkimuskokonaisuutena oli mittaus- ja säätöjärjestelmän kehittäminen, minkä tavoitteena oli mahdollistaa aivojen sähköisen signaloinnin mittaaminen mahdollisimman luonnollisessa tilassa olevilla koe-eläimillä (esim. hyönteiset, matelijat tai pienet nisäkkäät). Tätä varten kehitettiin aktiivinen liikekompensointimekanismi, jossa kosketusanturilla mitattiin aivokudoksen mikrometriluokan mekaanista liikettä ja kompensoitiin sähköistä mittausta suorittavan anturin ja aivon välinen suhteellinen liike liikuttamalla takaisinkytkentälenkissä olevaa pietsosähköistä aktuaattoria. Kompensointimekanismin toiminta testattiin realistisissa mittausolosuhteissa. Liikekompensoinnilla saatiin vähennettyä mittausanturin liikettä suhteessa kudokseen alle mikrometriin, maksimikompensoinnin ollessa noin 98 % alle 10 Hz:n taajuudella. Väitöskirjaan liitettiin pietsosähköisiin komponentteihin liittyen taustatiedoksi artikkeli aiemmin suunnitellusta pietsosähköisestä bimorph aktuaattori/sensori -komponentista.

Toisen tutkimuskokonaisuuden muodosti suurten hermosolupopulaatioiden toiminnan mittaamiseen sekä stimulointiin kehitetty monikanavainen järjestelmä. Tärkeimpänä mittauskohteena työssä ovat ekstrasellulaariset aktiopotentiaalisignaalit, jotka ovat eräänlainen evoluution tuottama “digitaalinen” hermosolujen välinen kommunikaatiomenetelmä. Kiinnostuksen kohteena ovat näiden aktiopotentiaalisignaalien aaltomuodot. Mittauksia varten työssä kehitettiin hermosolujen solun ulkopuoliseen nesteeseen asetettaviin elektrodeihin kytkettävä elektroniikka, jolla pystytään sekä stimuloimaan että mittaamaan jokaista elektrodia.

Suunniteltu vahvistinelektroniikka on matalakohinainen, matalatehoinen ja pienikokoinen. Mittausjärjestelmään on suunniteltu myös multipleksointi, A/D-muunninelektroniikka sekä ohjauslogiikka, joka sisältää muunnostulosten puskuroinnin integroidun piirin rekisteripankkeihin, SPI-liitynnän high-speed USB protokollaa tukevalle mikrokontrollerille sekä konfiguraatiorekistereitä, joihin SPI-väylän kautta kirjoittamalla voidaan säätää piirin vahvistusta, operaatiovahvistimien biasvirtoja, kaistanleveyttä sekä stimulaatiovirtojen voimakkuuksia. Piirin vahvistus on säädettävissä 100:n ja 5000:n välillä ja ylipäästösuodatuksen kulmataajuus välillä 0,5 Hz - 900 Hz. Piirin näytteistystaajuus on 20,833 kSps ja tiedonsiirtonopeus 3,5 Mbps. Piirin kohinatasoksi mitattiin 7,5 µV (rms) (300 Hz - 10 kHz) ja koko piirin tehonkulutukseksi alle 2 mW. Integroidusta piiristä valmistettiin 16-kanavainen prototyyppi 0,35 µm:n CMOS-teknologialla. Kehitetyn laitteen toiminta varmistettiin mittaamalla hermosignaaleja torakkapreparaatista (*Periplaneta americana*). Mittausdata siirrettiin onnistuneesti ja luotettavasti PC:lle.

Asiasanat: aktiopotentiaalien mittaus, hermosignaalien mittaus, hermosignaalien mittausjärjestelmä, hermosignaalien stimulointi, liikekompensointi, sähköfysiologia

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This thesis is based on research carried out primarily in 2010 - 2015 in the Electronics laboratory of the University of Oulu. Work on the micromotion compensation system began in autumn 2009. Most importantly I would like to express my gratitude to the principal supervisor of the thesis, professor Timo Rahkonen, who hired me to the Electronics laboratory in 2005 as a diploma thesis worker. Timo's guidance and advice have been invaluable to me. I would like to also thank the second supervisor of the thesis Ph.D. Mikko Vähäsöyrinki for guidance and for hiring me to develop a micromotion compensation system in 2009 with M.Sc.(tech) Tuomas Tuukkanen, who I also wish to thank. I would like to thank Ph.D. Marko Pudas who hired me to the Microelectronics laboratory during 2006 - 2009 where I worked on various projects and gained experience on electronics design. Towards the end of that time I was also introduced to some of the work done in the Biophysics laboratory and decided to apply for a graduate school position with a research plan related to the field of biophysics.

I would also like to thank the current and former colleagues working at the Electronics laboratory for providing a pleasant working atmosphere. Special thanks also to Prof. Matti Weckström for helping with the action potential measurements and chief technician Matti Polojärvi for chip bonding and help with acquiring all the parts I needed for building my various prototype boards.

I wish to thank professor Juha Voipio and associate professor Pietro Andreani for reviewing my thesis. Their input was much appreciated, and based on their comments I made significant improvements to the thesis. I wish to express my gratitude to those foundations and partners that supported me financially during my time as a Ph.D. student. Warm thanks to Tauno Tönning Foundation, Emil Aaltonen Foundation, Tekniikan edistämissäätiö (TES), Infotech Oulu Graduate School and University of Oulu Graduate School.

Finally, I would like to thank my family, my parents Sirkka and Antti and my sister Marja and her husband Antti for patience and support.

Oulu, September 2015 Olli Kursu

List of abbreviations and symbols

A/D	*analog-to-digital*
AC	*alternating current, varying signal*
ADC	*analog-to-digital converter*
ADP	*adenosine diphosphate*
AP	*action potential*
APC	*adaptive power control*
ASIC	*application specific integrated circuit*
ATP	*adenosine triphosphate*
BiCMOS	*bipolar-CMOS, a semiconductor technology containing both bipolar and CMOS transistors*
BW	*bandwidth*
CAD	*computer-aided design*
CDC	*communication device class, a generic way to enable communications with the USB bus*
CLK	*clock signal*
CMOS	*complementary metal-oxide semiconductor, a semiconductor technology containing both NMOS and PMOS transistors*
CS	*chip select, SPI bus signal*
DAC	*digital-to-analog converter*
DC	*direct current, constant signal*
DNL	*differential nonlinearity*
DNR	*dynamic range*
DUT	*device under test*
ECG	*electrocardiography*
EEG	*electroencephalography*
EMG	*electromyography*
ENOB	*effective number of bits*
EOG	*electrooculography*
FM	*frequency modulation*
FPGA	*field programmable gate array*
FSK	*frequency shift keying*

GUI	*graphical user interface*
I/O	*input/output*
IC	*integrated circuit*
INL	*integral nonlinearity*
kbps	*kilobits per second*
LED	*light emitting diode*
LFP	*local field potential*
LSB	*least significant bit*
Mbps	*megabits per second*
MCU	*microcontroller (unit)*
MEMS	*microelectromechanical system*
MISO	*master in, slave out, SPI bus signal*
MOSI	*master out, slave in, SPI bus signal*
MSB	*most significant bit*
NEF	*noise efficiency factor*
NMOS	*n-channel metal-oxide semiconductor*
OA	*operational amplifier*
OTA	*operational transconductance amplifier*
PA	*power amplifier*
PI	*proportional integral*
PID	*proportional integral derivative*
PM	*phase margin*
PMOS	*p-channel metal-oxide semiconductor*
PSRR	*power supply rejection ratio*
PZT	*lead zirconate titanate*
rms	*root mean square*
S&H	*sample and hold*
SAR	*successive approximation register*
SCK	*SPI bus clock signal*
SDRAM	*synchronous dynamic random access memory*
SNR	*signal-to-noise ratio*
SPI	*serial peripheral interface*
USB	*universal serial bus*
UWB	*ultra wide band*
WBAN	*wireless body area network*

WLAN	*wireless local area network*
A	*gain*
A_0	*DC gain*
$BaTiO_3$	*barium titanate*
Ca^{2+}	*calcium ion*
C_{attn}	*attenuation capacitance*
C_{dl}	*electrical double layer capacitance*
$C_{electrode}$	*microelectrode capacitance*
Cl^-	*chloride ion*
C_L	*load capacitance*
C_{ox}	*gate oxide capacitance per unit area*
$\mathbf{D}$	*electric charge density displacement matrix*
$\mathbf{d}$	*piezoelectric coupling coefficient matrix*
$\mathbf{E}$	*electric field strength matrix*
F	*Faraday constant*
f	*frequency*
gm	*transconductance*
I_{tot}	*total supply current*
K^+	*potassium ion*
k	*Boltzmann constant*
K_N	*NMOS transistor 1/f noise coefficient*
K_P	*PMOS transistor 1/f noise coefficient*
L	*transistor channel length*
Na^+	*sodium ion*
p_1	*first pole*
p_2	*second pole*
P_k	*ion concentration*
R	*gas constant*
R_I	*output impedance of the first amplifier stage*
R_{II}	*output impedance of the second amplifier stage*
$\mathbf{S}$	*strain matrix*
$\mathbf{s}$	*elastic compliance matrix*
T	*temperature*
$\mathbf{T}$	*stress matrix*

V_{dd}	*positive supply voltage*
V_{in}	*input voltage*
V_{LSB}	*voltage change corresponding to a change of 1 LSB*
V_{mid}	*mid-supply voltage*
V_{namp}	*noise voltage (rms) due to neural signal measurement electronics, referred to the input*
V_{nbrain}	*noise voltage (rms) due to background neural activity*
$V_{nelectrode}$	*electrode noise voltage (rms)*
V_{nopamp}	*operational amplifier noise voltage (rms), referred to the input*
V_{nq}	*quantization noise voltage (rms), referred to the input*
V_{nqrms}	*quantization noise voltage (rms)*
V_{nsign}	*signal noise voltage (rms)*
V_{ntot}	*total noise voltage (rms), referred to the input*
V_{out}	*output voltage*
V_{ss}	*negative supply voltage*
V_T	*p-n junction thermal voltage*
W	*transistor channel width*
$Z_{electrode}$	*microelectrode impedance*
Δf	*bandwidth*
$\Delta\sigma$	*surface charge density difference*
$\Delta\Phi$	*surface potential difference*
$\boldsymbol{\varepsilon}$	*electric permittivity matrix*

List of original publications

This thesis is based on the following articles, which are referred to in the text by their Roman numerals (I–V):

I Kursu O, Kruusing A, Pudas M & Rahkonen T (2009) Piezoelectric bimorph charge mode force sensor. Sensors and Actuators A: Physical 153(1): 42–49.

II Kursu O & Rahkonen T (2011) Charge scaling 10-bit successive approximation A/D converter with reduced input capacitance. Proceedings of the 29th IEEE Norchip conference, Lund Sweden.

III Kursu O, Tuukkanen T, Rahkonen T & Vähäsöyrinki M (2012) 3D active stabilization system with sub-micrometer resolution. PLoS ONE 7(8): e42733.

IV Kursu O & Rahkonen T (2014) Integrated circuit for neural recording and stimulation. Proceedings of the 32nd IEEE Norchip conference, Tampere, Finland.

V Kursu O, Vähäsöyrinki M & Rahkonen T (2015) Integrated 16-channel neural recording and stimulation circuit. Journal on Analog Integrated Circuits and Signal Processing 84(3): 363–372.

All papers were written by the author, except Paper III which was written in collaboration with M.Sc.(Tech) T. Tuukkanen, Ph.D. M. Vähäsöyrinki and Prof. T. Rahkonen. On Paper III M. Vähäsöyrinki also acted as the corresponding author.

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1 Introduction

This work consists of two main areas. First, active piezoelectric micromotion compensation of neural signal measurement electrodes was investigated. Second, an integrated neural signal measurement and stimulation system is presented. Prior to the work on these two areas, a piezoelectric bimorph actuator for force sensing was developed. This previous work is also included in the thesis to serve as background information related to piezoelectric components and their electrical properties.

To illustrate the context of this work, some background information on neural signaling is first presented in Chapter 2. The measurement environment is described and some design requirements for the neural signal recording microelectrode and recording electronics are presented. Ways of canceling the DC offset present in neural signal measurements are also discussed. In Chapter 3 piezoelectric components and an analysis of the actuating piezoelectric bimorph sensor published in Paper I is presented. The piezoelectric component was analyzed both analytically and with finite element simulations. The analytic calculations were based on the earlier work by the co-author Ph.D. Arvi Kruusing. The finite element simulations and the analytic solution were made by the author.

In Chapter 4, three-dimensional micromotion compensation is explored. The micromotion compensation system is intended to be used with in vivo measurements for small animals, such as insects or rodents. Even if the preparation is fixed, e.g. muscle motions or respiration may move the tissue and change the relative position between the neurons and the probe. A micromotion sensor and movement compensation electronics published in Paper III are presented. The sensor was designed by the co-author M.Sc.(Tech) Tuomas Tuukkanen and simulated using a finite element analysis tool by Mr. Tuukkanen and the author. The sensor was implemented by the Center of Microscopy and Nanotechnology of the University of Oulu. The compensation and measurement electronics were designed by the author. The measurements were made in collaboration with Mr. Tuukkanen. Also some unpublished results that were not included in Paper III are presented in Chapter 4.

Chapter 5 presents a neural recording and stimulation circuit that was published in Paper V. The circuit was designed by the author and its performance was verified by

measurements using a test setup developed by the author. New measurement results with biological signals are also presented.

Finally, in Chapter 6 future developments and issues faced in the current work are discussed. Wireless transmission options are discussed along with digital post-processing of measurement results.

The main contributions of the work are the following: Paper I shows an analytical expression for a piezoelectric bimorph used as an actuating force sensor. It also shows that a high impedance measurement does not leak the accumulating charge which affects the mechanical movement.

Paper II presents an effective successive approximation register (SAR) A/D converter architecture that was simulated yet not eventually implemented. It was shown that small timing errors easily drive the DAC summing node of the A/D converter outside the power rails, which causes charge leakage.

Paper III presents an implemented micromotion compensation system for stabilizing neural recording electrodes with respect to the preparation. The performance is mostly dictated by the mechanical implementation while the electrical control loop is rather straightforward. The possibility of cross axis oscillations was studied.

Papers IV and V describe an integrated circuit with 16 channels that can be used either to record neural data or to excite neurons with bipolar current pulses. The circuit was designed and its performance was measured by the author. The chip was designed using a 0.35 μm CMOS process and it was fabricated by ams AG. The measured performance of the circuit is comparable to that of the state-of-the-art implementations. Main design efforts concentrated on minimizing power consumption and guaranteeing uninterrupted data flow.

2 Neural signals and the measurement environment

2.1 Chemical origins of neural signaling

All living cells have an energy transfer mechanism in them that makes cell metabolism possible. The final step of energy transfer to energy-consuming molecules within cells is based on the molecule Adenosine Triphosphate (ATP) which is often called the energy currency of the cell. Its function is analogous to that of a battery as it can store energy and release it when needed. This energy release happens when the molecule is decomposed into Adenosine Diphosphate (ADP) inside the cell when a phosphor molecule separates from it. This process is called dephosphorylation. Dephosphorylation occurs via hydrolysis, i.e. when chemical bonds are broken down by the addition of water. This chemical reaction is catalyzed by an enzyme class called ATPase. ATP is formed in the body in several ways when nutrients are consumed. The primary way is oxidative phosphorylation during cellular respiration. Cellular respiration is a complex set of chemical reactions where glucose is oxidized and ATP is synthesized.

Two of the ATPase enzymes, the Na^+/K^+ ATPase and Ca^{2+} ATPase pumps are mainly responsible for maintaining electrochemical gradients of these ions across the cell membrane at rest. The cell membrane contains proteins (such as ATPase enzymes) that pump ions through the membrane and proteins that change the permeability of the membrane to specific ions. The former are known as active transporters and the latter as ion channels. The cell membrane potential with respect to the outside of the cell is mainly defined by the difference of the Na^+, K^+, Cl^- and Ca^{2+} (which are the most important ones) ion concentrations inside and outside the cell and by the cell membrane permeability to each of these ions. While the ATPase enzymes slowly pump ions against their concentration gradients, ion channels can release larger in- and outfluxes of ions in shorter periods of time. In a typical living cell at rest this potential is about -40 mV to -90 mV with respect to the outside of the cell, depending on the type of the cell. One exception are red blood cells, which have a resting potential of about -10 mV [1].

The cell membrane potential V_m can be calculated by the Goldman-Hodgkin-Katz equation (Goldman 1943 [2], Hodgkin-Katz 1949 [3]).

$$V_m = \frac{RT}{F} \ln \frac{P_k[K]_2 + P_k[Na]_2 + P_k[Cl]_1}{P_k[K]_1 + P_k[Na]_1 + P_k[Cl]_2}, \quad (1)$$

where R is the gas constant, T the absolute temperature, F the Faraday constant and P the membrane permeability coefficient to each ion. The elements in square brackets indicate ion concentrations (mM) both inside (1) and outside (2) of the cell. If we convert the equation to a base 10 logarithm, the part before the logarithm simplifies to 61.5 at human body temperature (310 K). Since the valence of K^+ and Na^+ is one and Cl^- is minus one, the Cl^- subscripts have interchanged. If the membrane is permeable to only one ion species, Eq. 1 reduces to the Nernst equation developed by Walther Nernst in 1889, and the membrane potential will equal the equilibrium potential of the permeant ion [1].

If the nerve cell is stimulated by a signal that elevates the membrane potential above a certain threshold level, an action potential (AP) is generated. The action potential either occurs fully or not at all. The ATP molecule plays a crucial role in maintaining long-term restoration of ion concentrations via ATPase. The ATPase pumps are fueled by the energy released from the hydrolysis of the ATP. While the immediate energy for the action potential generation is taken from the ionic gradient, thus not requiring energy from the ATP, it has been calculated that in the long term it takes roughly a billion ATP molecules to propagate an AP pulse through a human neuron [4]. A typical duration for the spike is 1 ms and the amplitude of the spike is independent of the amount of the current injected. If the duration of the stimulus is increased, multiple consecutive action potentials are generated. If the threshold is not surpassed, only smaller passive responses are generated (graded potentials), reflecting the voltage change proportionally to the injected current. When the membrane potential drops with respect to the resting potential, the membrane is called “hyperpolarized” and when it rises, it is called “depolarized”.

Cells can be divided into two categories, excitable and non-excitable cells. All cells have a resting (or membrane) potential, but excitable cells, such as nerve or muscle cells, respond to electrical stimuli either by creating graded potentials (such as receptor cell potentials or synaptic cell potentials) which transfer signals between short distances or regenerative action potentials which transfer signals over long distances. Nerve cells or neurons are the principal cells of the nervous system along with the supporting glia cells. These cells are assembled into complex neural circuits. The nervous system can be divided into three different systems: sensory, motor and associational systems. Neurons

are not particularly good electrical conductors, but have evolved mechanisms to improve signal transmission. Action potentials are the main electrical signal transmission method in the nervous system, but other kinds of electrical potentials are also generated in the nervous system by the activation of synaptic contacts. Nerve cells consist of three basic elements, the axon, the cell body and dendrites. Axon is the signal output pathway of a neuron. While neurons only have a single axon, it branches out and forms several thousands of synapses. Synapses, the contacts between neurons that permit signals to travel from neuron to neuron, are mostly made on dendrites and less frequently on cell bodies. Furthermore, also axo-axonic synaptic contacts exist. A functioning nerve cell can have between 1 to 100,000 synaptic inputs.

The cell resting potential is maintained at negative levels because the cell membrane is more permeable to K^+ than Na^+ ions. Ion pumps pump Na^+ and in neurons often also Cl^- out of the cell and replenish the cell's K^+ content. An action potential is generated when, as a response to depolarization, the membrane permeability suddenly changes and becomes more permeable to Na^+ than K^+. As a result, a positive feedback loop is generated, as Na^+ ions pour into the cell down their electrochemical gradient, depolarizing the membrane further and opening new voltage gated Na^+ channels. This sudden change is transient and is quickly followed by increased permeability to K^+ and decreased permeability to Na^+. At peak voltage, Na^+ permeability decreases because of the inactivation of Na^+ channels.

As the membrane becomes more permeable to K^+, K^+ ions flow out of the cell, causing the membrane potential to hyperpolarize. The cell potential even undershoots briefly when the K^+ permeability increases above the resting level, resulting in a negative feedback loop. This hyperpolarization voltage turns off the K^+ channels and the cell returns to its resting potential. The behavior during the action potential cycle is caused by opening and closing of ion channels. These ion channels are proteins that change their shape depending on the membrane potential. Therefore, the membrane potential itself affects the membrane permeability to specific ions.

In some neurons Ca^{2+} channels give rise to action potential signals in the same way as Na^+ channels do. By affecting intracellular concentrations, Ca^{2+} channels regulate a huge number of biochemical processes within cells. Most importantly, the channels regulate the release of neurotransmitters at synapses. Cl^- channels are present in every type of neuron and they control excitability, contribute to membrane resting potential and help regulate cell volume.

In addition to generating intracellular signals, membrane currents underlying postsynaptic responses and action potentials also generate signals in the extracellular space. These signals are much smaller in amplitude than their intracellular counterparts. Typically, synaptic excitation is caused by a current loop that flows into dendrites via postsynaptic channels and spreads towards the soma of the neuron and returns along the extracellular space. Extracellular currents generated by many adjacent cells merge and form a volume current that generates in the resistive extracellular fluid a signal that is known as local field potential (LFP). The polarity of LFP indicates whether it is measured at a site dominated by transmembrane current sinks or sources. Similarly, current loops responsible for the generation and spreading of action potentials evoke extracellular potential signals that are called, for example, unit spikes when generated by a single neuron, or population spikes when generated by a synchronously spiking group of neurons [1, 5].

2.2 Extracellular action potential measurements

Action potentials have been measured intracellularly using glass capillary microelectrodes and less invasively using extracellular metal or glass microelectrodes. While intracellular methods measure action potentials that are in the range of hundred millivolts with little attenuation, extracellular methods measure these signals outside of the cell where the signal level is only hundreds of microvolts or less. Extracellular electrodes record from the extracellular fluid that surrounds nerve cells. The ion currents of the action potential generate signals in the extracellular fluid which couple capacitively to the measurement electrode and are called extracellular action potential signals.

Neural signals are generated by nerve cells which are located in the central nervous system (brain and the spinal cord) or the peripheral nervous system, which connects organs to the central nervous system. Signaling between these cells is of interest to researchers who want to understand how the brain and the nervous system operate. Optimally, extracellular measurements should be made simultaneously from several points and in a wake, freely behaving animal. Furthermore, the damage to the cells should be minimal and an implanted recording chip should function for long periods of time. Such neural implants require either a wireless link or a wired transcutaneous interface.

Integrated extracellular neural signal recording solutions were pioneered by Kensall D. Wise, who in 1970 wrote an article on manufacturing a neural signal measurement

probe using integrated circuit manufacturing techniques [6]. A year later he and his research team attached discrete component amplifiers to the probe, and in 1974 an integrated liquid-oxide FET amplifier was attached to another probe [7, 8]. In 1985 Khalil Najafi and Wise proposed an integrated circuit compatible multichannel recording array [9]. This discrete component design used several operational amplifiers (op-amps) and a multiplexer that could be used to multiplex up to 40 channels. A multichannel recording probe was also introduced. A year later they published a paper of an integrated version of the circuit, which contained an integrated amplifier and a multiplexer (which they called "an active probe"). Analog demultiplexing was accomplished with external electronics [10]. This paper probably presents the first complex custom ASIC for neural signal recording. In 1992 Jin Ji and Wise integrated a 32:8 front-end selector followed by 8 amplifiers and an 8:1 multiplexer [11]. High-pass filtering was done with an integrated diode-capacitor filter, where the filter was formed by the diode resistance and the capacitor. It did not offer great accuracy in setting the corner frequency and had a limited dynamic range.

Another significant contributor to the field is Reid R. Harrison, who in 2002 designed a neural signal amplifier based on the current mirror operational transconductance amplifier (OTA) [12]. In 2003 the same amplifier was published in a journal paper [13]. Harrison and his team have also made integrated action potential spike detector circuits and wireless data transmission circuits [14, 15].

In our work we focus on the measurement of extracellular action potential signals (AP) and local field potentials (LFP). Their relation to different neural signal types with respect to signal level and frequency band are shown in Fig. 1 (solid line) [16].

2.3 Neural recording site

The extracellular measurement site consists of a connection between the extracellular fluid that surrounds the cell membrane and the metallic measurement microelectrode. This constitutes a metal-solution interface in which the solution contains some salts and is therefore conductive. Usually precious metals, such as platinum or tungsten, are used as the microelectrode, since they do not oxidize easily. At the metal-solution interface an electrical double layer is generated that can be modeled as a capacitor. This is also the simplest way to model the microelectrode impedance. A double layer is formed when charge accumulation and separation occur at the microelectrode-solution interface. Depending on the polarization of the microelectrode, either negative anions or positive

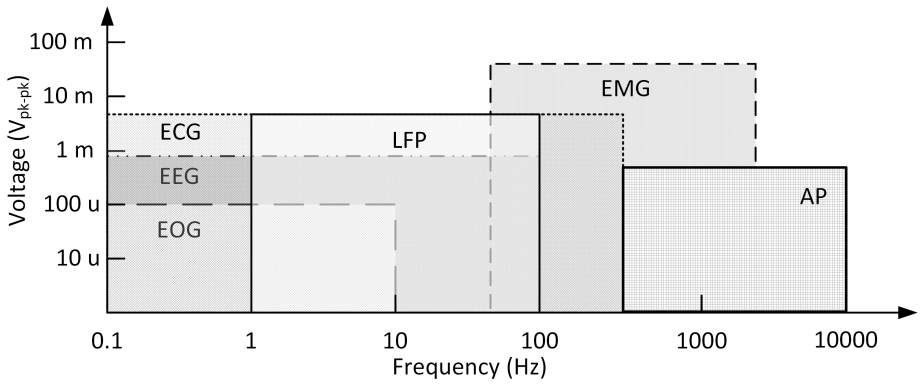

Fig. 1. Voltage and frequency ranges of some common physiological signals, where EOG, EEG, ECG, EMG, LFP and AP refer to the electrooculography, electroencephalography, electrocardiography, electromyography, local field potential and extracellular action potential, respectively. Adapted from [16].

cations accumulate in the solution (the opposite side of the double layer). The electrical double layer capacitance is defined by a differential capacitance according to

$$C_{dl} = \frac{\Delta\sigma}{\Delta\Phi}, \tag{2}$$

where $\Delta\sigma$ is the surface charge density difference and $\Delta\Phi$ is the surface potential difference [17].

To suppress low-frequency fluctuations and DC offsets generated by electrode polarization, the amplifier connected to the capacitive microelectrode-cell interface is usually AC-coupled. The amplifier implementation shown in Fig. 2B uses a capacitively coupled op-amp where the gain is defined by the ratio of the input capacitance to the feedback capacitance. This means that if the capacitance of the microelectrode-cell interface is low compared to the input capacitor, the op-amp gain is reduced since the input capacitor is in series with the microelectrode impedance. The microelectrode impedance $Z_{electrode}$ is usually measured at 1 kHz and can be calculated by

$$Z_{electrode} = \frac{1}{2\pi C_{electrode} f}, \tag{3}$$

where the $C_{electrode}$ is the microelectrode capacitance and f is the measurement frequency. Typical values for extracellular microelectrode impedances are 100 kΩ - 3

MΩ, corresponding to a capacitance of 1.6 nF - 50 pF at 1 kHz, but impedances even as high as tens of MΩ (10 MΩ is 16 pF at 1 kHz) have been measured.

In integrated circuits large capacitors take a lot of die area. If the circuit needs to be implantable and many channels are needed, capacitances should be limited to around tens of picofarads. Typical input capacitor sizes are 10 pF (Olsson 2005 [18]) and 20 pF (Harrison 2003 [13]). Both circuits have feedback capacitances that give a gain of 100 (0.1 pF and 0.2 pF). With such capacitances the 3 MΩ microelectrode would cause a gain attenuation of 16% and 27% at 1 kHz, respectively. Making the op-amp input capacitor smaller would thus reduce the problem, but this would also reduce the gain, since capacitors below 100 fF are not easily implemented due to parasitic capacitances which are on the same range.

Precise calculation of the noise generated by the microelectrode-cell interface is difficult, since electrochemical processes and fluid motion in the microelectrode-solution interface are involved. The size of the microelectrode has the largest influence on its noise, since larger microelectrodes have smaller resistances and the resistive elements in the microelectrode are responsible for noise generation [19]. The noise generated by an electrode $V_{nelectrode}$ can be expressed by

$$V_{nelectrode} = 2\sqrt{kT\Delta f Re(Z)}, \tag{4}$$

where k is the Boltzmann constant, T the temperature, Δf the bandwidth over which the noise is measured, and $Re(Z)$ is the real part of the electrode impedance. Typical noise levels at the recording site of around 10 µV rms (around 60 µV peak-to-peak) have been measured. From the previous we can deduce that smaller microelectrodes have smaller capacitances and larger resistances (the surface area of the electrical double layer is smaller) and therefore attenuate the signal more and generate more noise [20]. A probe with an area of 1000 µm^2 generates approximately 5 µV rms noise at a frequency range of 100 Hz - 10 kHz [19]. In addition to the noise produced by the electrode ($V_{nelectrode}$), background neural activity (V_{nbrain}) and the neural signal measurement electronics (V_{namp}) contribute to the noise, making the total noise level [21]

$$V_{ntot} = \sqrt{V_{nelectrode}^2 + V_{namp}^2 + V_{nbrain}^2}. \tag{5}$$

2.4 DC offset removal techniques

AC coupling or high-pass filtering is essential in extracellular action potential spike measurements. High-pass filtering will, however lead to long recovery time if large inputs, such as stimulation signals are present. There are four simple ways to implement a high-pass op-amp filter. These have been collected by Thomas Jochum in his neural signal amplifier literature review [19].

Simple realizations are putting an RC filter in front of the op-amp like in Fig. 2A or integrating the filter inside the op-amp. The former has been implemented by Perelman and Ginosar [22] and the latter approach has been taken by Demosthenous and Triantis who put a 100 Hz - 10 kHz RC band-pass filter inside the op-amp [23].

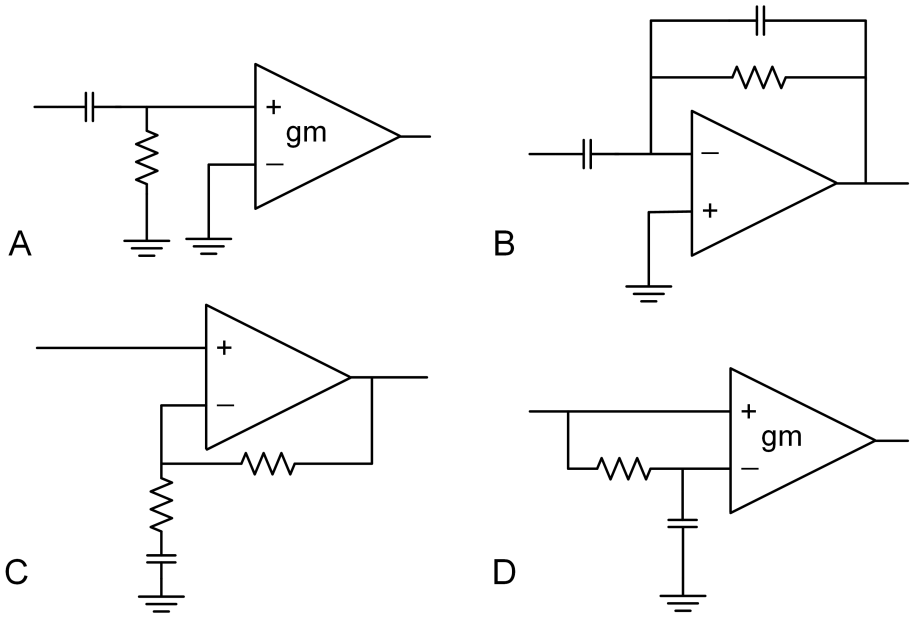

Fig. 2. Different high-pass filter realizations. For details, see text. The gm denotes an operational transconductance amplifier (OTA). Adapted from [19].

The most commonly used way to implement a high-pass op-amp filter is to use a pseudoresistor element in parallel with a capacitor in the feedback path, as shown in Fig. 2B. This topology was first implemented in a neural signal amplifier by Harrison in 2002 [12]. The low cut-off frequency can be controlled by controlling the value

of the pseudoresistor element, which is made of a MOS transistor biased in the deep subthreshold region. The value of the NMOS-NMOS pseudoresistor implemented by Harrison also depends on the magnitude of the input and output signals. A similar design (some using PMOS pseudoresistors) has been used, for example, by Horiuchi (2004) [24], Olsson (2005) [18], Wattanapanich (2007) [25], Chae (2008) [26], Aziz (2009) [27], Zou (2009) [16], Mollazadeh (2009) [28], and several others. An NMOS-PMOS pseudoresistor element has been proposed by Yin and Ghovanloo (2007) [29]. This circuit can behave more linearly when input or output voltages change, but it requires a separate biasing circuit.

The third way is to put a low-pass filter in the feedback path like in Fig. 2C where it is subtracted from the input signal, resulting in a high-pass filter. This kind of design has been used by Ji and Wise (1992) [11] and Obeid (2003) [30]. This topology has the highest input impedance and can thus handle very high impedance microelectrodes. Such a subtraction scheme is conceptually similar to autozeroing and correlated double sampling techniques [19]. The drawback of this topology is that it has a DC gain of unity and thus does not suppress low-frequency fluctuations or power line interference.

The fourth way to implement high-pass filtering is to subtract a low-pass filter from the original input signal like in Fig. 2D. This topology has been rarely used. One example is Pathasarathy (2006) [31]. In this setup, the linearity of the pseudoresistor is improved because the voltage over it is smaller than in the feedback configuration. Tuning the pseudoresistor with a current signal is more difficult since the pseudoresistor bias needs to be close to the input voltage. This would require drawing current from the input node that would need to be compensated for. The high-pass filter corner frequency tuning could also be accomplished by switching a capacitor bank in place of the input capacitance, but that would considerably increase the circuit area.

Chopper stabilization is an old technique for canceling offset voltages and reducing 1/f noise of op-amps and can be implemented in the previously described topologies. The input signal is modulated to a higher frequency, amplified like an AC signal where 1/f noise and offset have no effect, and then demodulated back to the original frequency. If the input signal frequency is limited to half of the chopper frequency, there is no aliasing, and 1/f noise and offset from the amplifier between the modulators is suppressed. The switching operation in choppers can introduce more noise from switching transients. Choppers are quite rarely implemented in recent neural signal recording designs, but have been used, for example, by Hu (2002) [32], Lee (2006) [33], Denison (2007) [34]

and Avestruz (2008) [35]. Chopper stabilization can be a very attractive solution for low-frequency neural signal recording, such as EEG and EOG measurements.

In our design we chose the option shown in Fig. 2B. The pseudoresistor element was implemented using two PMOS transistors. Current biasing with a local diode-connected PMOS transistor was used to improve matching between the channels.

3 Micropositioning using piezoelectric actuators

3.1 Piezoelectric materials and their properties

Piezoelectricity was discovered in 1880 by Jacques and Pierre Curie. They discovered that applying pressure to certain crystalline materials such as quartz produced a charge. The phenomenon was named "piezoelectricity" by W. Hankel in 1881. A year later the Curies demonstrated that the opposite was also true: charging a piezoelectric material caused it to deform. This effect was called the "inverse piezoelectric effect" or "electrostriction". Some tiny amount of electrostriction is present in all non-conducting materials, but the effect is especially pronounced in piezoelectrics. Purely piezoelectric materials such as quartz are monocrystalline and produce a small piezoelectric effect.

Piezoelectricity was not utilized in an industrial sense until piezoelectric ceramics were discovered. These materials behave similarly to natural piezoelectric materials but are not intrinsically piezoelectric. They are multicrystalline and ferroelectric materials with random crystallite orientation that are processed to become piezoelectric. This process includes steps such as heating and exposing the material to a high electric field (poling). When the electric field is applied, electric dipoles in the piezoelectric material polarize in the chosen direction of the electric field. When the electric field is removed, the material is permanently polarized and piezoelectric. If piezoelectric materials are heated above a certain temperature (Curie point), they lose their piezoelectric effect.

Nowadays piezoelectric components made out of piezoelectric ceramics, such as lead-zirconate-titanate compounds (PZT) and barium-titanate ($BaTiO_3$), are used as both actuators and sensors. Out of these two, PZT compounds are the most commonly used materials. The piezoelectric effect is used in force measurement, which is used in car airbag safety systems and microphones, for example. The inverse piezoelectric effect or electrostriction is arguably even more useful. There are various applications that require precise positioning and utilize the inverse piezoelectric effect to accomplish this. Other applications include vibration compensation (damping) and piezoelectric motors. Piezoelectric devices are used in fields such as optics, astronomy, physiology, materials science, fluid control and precision machining. The most common application that utilizes electrostriction is the crystal oscillator that is used as a time keeper in billions of

clocks. The National Institute of Standards and Technology (NIST) in the United States has estimated that more than two billion quartz oscillators are manufactured annually [36].

3.2 Piezoelectric components

Piezoelectric actuators require voltage driving, typically with high voltage if the maximum movement range is required. Piezo actuators offer very precise actuation capabilities, but suffer from nonlinearity and hysteresis. In closed-loop configurations these problems are mitigated and piezoelectric actuators are capable of sub-nanometer resolution. The maximum electric field a piezoelectric ceramic can withstand is in the order of 1 kV/mm. To improve the actuation distance, thin slices of piezoelectric material are often glued together to form a piezoelectric stack actuator. This kind of actuators can typically compress and elongate to distances of tens to hundreds of micrometers and block forces up to several kilonewtons, depending on the size and material of the actuator.

A typical piezoelectric stack actuator is actuated with a peak-to-peak voltage of tens to hundreds of volts. Below their resonance frequency, the electrical behavior of piezoelectric stack actuators can be modeled as capacitors. More complex models exist that also model the resonance frequency, but for our purposes modeling the piezo with a capacitor is sufficient. Piezoelectric stack actuators have high impedance and are not susceptible to the coupling of electrical or magnetic fields. Piezoelectric actuators can be driven in three ways. If a rigid displacement is required, either servo drive or pulse width modulation drive is employed. These are the so-called DC drive methods. The third way is related to ultrasonic motors where the piezo is driven with an AC voltage at the piezo resonance frequency [37].

The mechanical behavior of piezoelectric components can be analyzed either analytically or numerically. Typically analytic solutions for piezoelectric components of complex shapes are difficult to solve. Piezoelectric components are typically simulated with simulation tools that use the finite element method. In finite element analysis, the simulated structure is divided into a two- or three-dimensional (or 2.5-dimensional where one of the dimensions is assumed to be invariant) mesh. The response of the whole structure is assumed to approximate that of the glued-together “finite elements”. Using this approach, a complex problem can be divided into smaller parts. Finite element

analysis involves solving partial differential equations and satisfying the associated boundary value conditions.

Since piezoelectric materials are anisotropic, their electromechanical properties are mathematically described as matrices, which are simplified from 3rd rank tensors. They can be described in several forms which are interchangeable. In the commonly used Strain-Charge form, the strain **S** (a dimensionless quantity of form dx/x, where x is length) and the electric charge density displacement **D** ($[C/m^2]$) are

$$\mathbf{S} = \mathbf{s}^E \cdot \mathbf{T} + \mathbf{d} \cdot \mathbf{E} \tag{6}$$

$$\mathbf{D} = \mathbf{d} \cdot \mathbf{T} + \boldsymbol{\varepsilon}^T \cdot \mathbf{E}, \tag{7}$$

where **s** is a 6x6 elastic compliance matrix which describes the strain **S** produced per unit of stress applied, **T** is a 6x1 stress matrix, **d** is a 3x6 piezoelectric coupling coefficient matrix that describes how much charge (polarization) is produced by the applied stress, **E** is the 3x1 electric field strength matrix, and $\boldsymbol{\varepsilon}$ is a 3x3 matrix describing the electric permittivity. The matrix elements have two-part subscripts (such as 11,31,15) that indicate the direction of the applied force (or electric field) and the direction polarization. The number of non-zero elements in the matrix depends on the symmetry of the piezoelectric crystal structure [38].

The coefficients also change depending on whether the element is under constant stress (mechanically free), constant strain (mechanically clamped), constant electric field (short circuit), or constant electrical displacement (open circuit). The superscripts in the coefficients define in which condition the coefficient was measured. Superscript E denotes constant (zero) electric field and superscript T constant (zero) stress field. The other forms of piezoelectric equations (Stress-Charge, Strain-Voltage, Stress-Voltage) can be calculated using matrix transformations. As with our finite element simulations with the bimorph, it is often the case that material parameters are given by manufacturers in a different form than what is required by the simulation tools.

3.3 Piezoelectric bimorph

In Paper I, a piezoelectric actuator that was also acting as a force sensor was investigated. The sensor/actuator structure was based on a piezoelectric bimorph. A piezoelectric bimorph has two piezo layers glued on a thin elastic middle electrode (shim), as shown in Fig. 3A. The shim is optional, but it improves the mechanical durability of the

bimorph. The shim is electrically connected to both piezo sheets. The poling direction of the bimorph (a general convention for all piezoelectric components) is axis 3. Due to symmetry constrictions in poled ceramics, the directions perpendicular to the poling direction are regarded as direction 1. Therefore, for example, the piezoelectric coupling coefficients in poled ceramics are d_{33}, $d_{31} = d_{31}$ and $d_{15} = d_{24}$ [39].

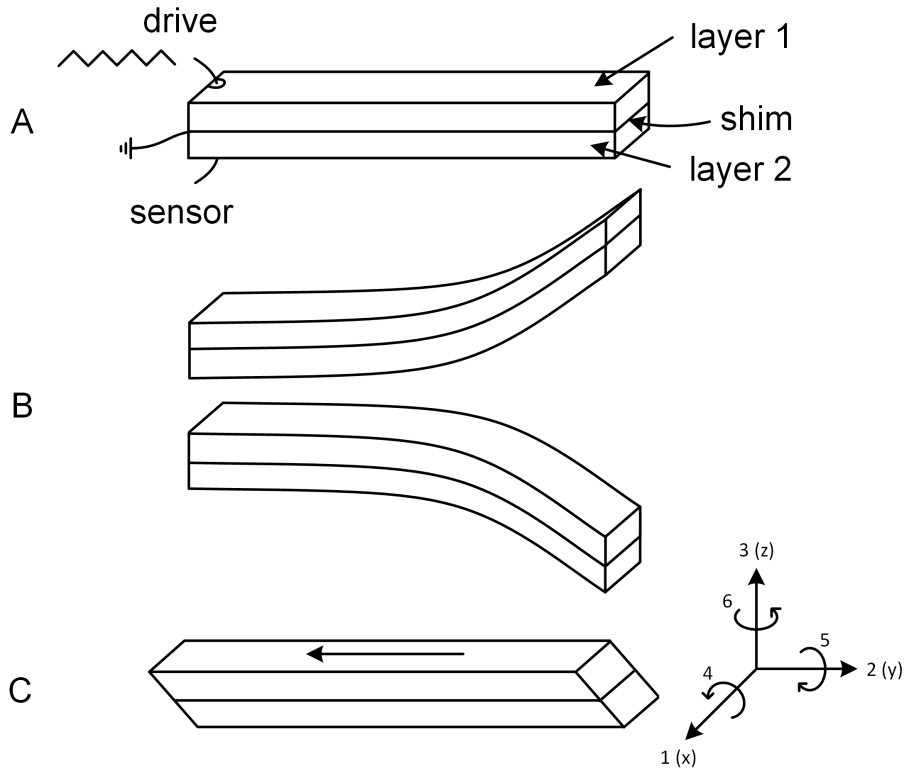

Fig. 3. Piezoelectric bimorph in an actuator/sensor configuration a) connections, b) deformation when the left head is fixed and c) direction of shear stress and notation of axes for piezoelectric components.

Both piezo layers and the shim have electrical connections. The piezos are aligned so that when an electrical field is applied to both sides and the shim is grounded, on side contracts and the other one expands. This setup requires that both piezo sheets have a parallel poling direction. In this configuration it is used as an actuator. Typically the other head of the actuator is clamped, resulting in a deformation shown in Fig. 3B. If

only one of the sides is actuated, the other one can be used as a sensor. In our case the bimorph is driven with an AC voltage, but its frequency is so low that the system is essentially a DC drive.

Due to its relatively large size compared to micronewton range strain gauges, for example, its force sensitivity was in the range of millinewtons. An analytical model of the actuator-sensor was presented. It was based on the earlier work by the co-author Arvi Kruusing. A circuit was constructed that actuated the bimorph and measured the produced charge as the other side of the bimorph was loaded. A finite element model with approximately 10,000 tetrahedral elements of the sensor was simulated with Comsol Multiphysics and it was found that the analytical, simulated and measured results for the bimorph agreed quite well. Addition of the shim to the finite element model further improved the agreement of the simulations with the measurements. One end of the bimorph was clamped both in the simulations and the measurements. In the simulations the electrical potential of the sensing part of the bimorph was volume integrated to reveal the sensor voltage.

The piezo is driven with a 5 V drive and the response is measured while the edge of the bimorph actuates freely and in a situation where the edge is loaded with a mass. The response was measured both with an oscilloscope and a charge amplifier and the displacement was measured with an optical displacement sensor. In our experiments with the piezoelectric bimorph, we found that measuring the bimorph with a dissipative charge amplifier produced a response that more closely followed the actuation of the bimorph. Continuously discharging the piezo seemed to be essential for making successful measurements, because residual charge in the capacitive piezo causes additional deformation.

The bimorph sensor/actuator was not used in the following implementations, but it gave experience in measuring small forces and understanding of mechanical time constants. It also served as a useful introduction to the simulation of mechanical components using finite element analysis. An interesting finding was the effect of the input impedance of the sensor amplifier: a high input impedance amplifier does not remove the charge generated on the sensing side of the bimorph caused by the strain of the actuating side of the bimorph. This stored charge affects the movement of the bimorph, especially if it is in continuous actuation.

4 Micromotion compensation in 3 dimensions

4.1 Need for micromotion compensation

A common problem with physiological measurements is the motion of the measurement microelectrode in relation to the neurons that are being measured. This can cause quick signal attenuation or even loss. Ideally electrophysiological measurements would be made from living, freely behaving animals. Often this is not possible due to recording electrode motion with respect to the measured neurons, and some restraint has to be used. Even with a fixed animal head, muscle motion and cardiac and respiratory pulses may cause movement near the recording site. Removing these movement sources requires surgical procedures unless they can be compensated for. In the case of small animal brains it is possible to use piezoelectric stack actuators that typically have movement ranges of tens of micrometers.

This kind of approach has been attempted by measuring respiratory pressure or direct measurement of brain micromotion with an interferometer to control the position of a piezo manipulator [40]. These methods were unable to compensate for larger movements in wake animals and can therefore only be used on anesthetized animals. Direct measurement of brain micromotion has also been previously attempted with a microminiature differential variable reluctance transducer [41]. Piezoelectric actuators have also been used to maintain the position of extracellular recording electrodes [42]. Another possibility is to attach a head-anchored recording electrode with a motor-controlled positioner. This kind of system works well for short durations with freely behaving larger animals such as rats but requires a long preparation time [43].

Three-dimensional force sensors have been built for robot-assisted manipulation. Using MEMS components, flexure beams and strain gauges, a sub-millinewton force resolution has been reached [44]. With MEMS components 3D forces down to the nanonewton range have been measured [45]. However, for custom applications, MEMS components typically require complex and costly design and manufacturing steps.

Previously a low-cost optical sensor with nanonewton range force sensitivity for measuring three-dimensional brain micromotion was developed in the Biophysics laboratory of the University of Oulu [46]. With this sensor, blowfly brain micromotion was measured to be below 5 µm and its frequency mostly below 10 Hz. This sensor had, however, a very low resonance frequency mainly due to its length, which is why

it was not suitable for compensation. In our system the idea was expanded further to include micromotion measurement and compensation in all three dimensions. In Paper III we improved the sensor further and presented the manufactured sensor in detail and showed that it functions in realistic neural signal measurement conditions. The system is intended to be used with small animal models, where brain micromotion is mostly below 5 μm in magnitude with dynamics below 10 Hz. As a performance target, the residual tissue micromotion after compensation should be at the level of 1 μm to enable stable neurophysiological experiments.

There are several challenges related to this area of research. One challenge is making the probe and actuator construction in such a way that there are no mechanical resonances at the frequency range of the control loop. Another challenge is the positioning of the micromotion measurement probe in relation to the electrode that is used to measure neural activity and the actuator that is used to compensate for the motion. Ideally all components would be in the same axis, but in practice this is difficult to achieve. In the worst case, cross axis coupling can reduce the compensation performance or even cause instability.

A glass tube was chosen as the probe material. Quartz glass tubes are readily available and easy to make, and it was thought that at least in principle the tube would also be able to house the neural measurement electrode. Another benefit of quartz glass is its high Young's modulus in relation to its low density, which means that the tube itself will not resonate at a low frequency. A concentric arc type sensor was simulated and machined from brass. This requires some complicated manufacturing steps, but is not nearly as complex or intricate as a 3D MEMS sensor. This sensor is described in greater detail in section 4.2.1.

4.2 System structure

A block diagram of the micromotion compensation system is shown in Fig. 4. The details of the electronics and a low-frequency model of the system are presented in Paper III. The optical sensor is used to detect movement originating from the test subject or user interference and the PI control loop adjusts the position of the optical sensor by driving the 3D piezo actuator, attempting to zero the movement. A custom piezo actuator with a movement range of 28 μm was built for the system, although commercial 3D options would have been available.

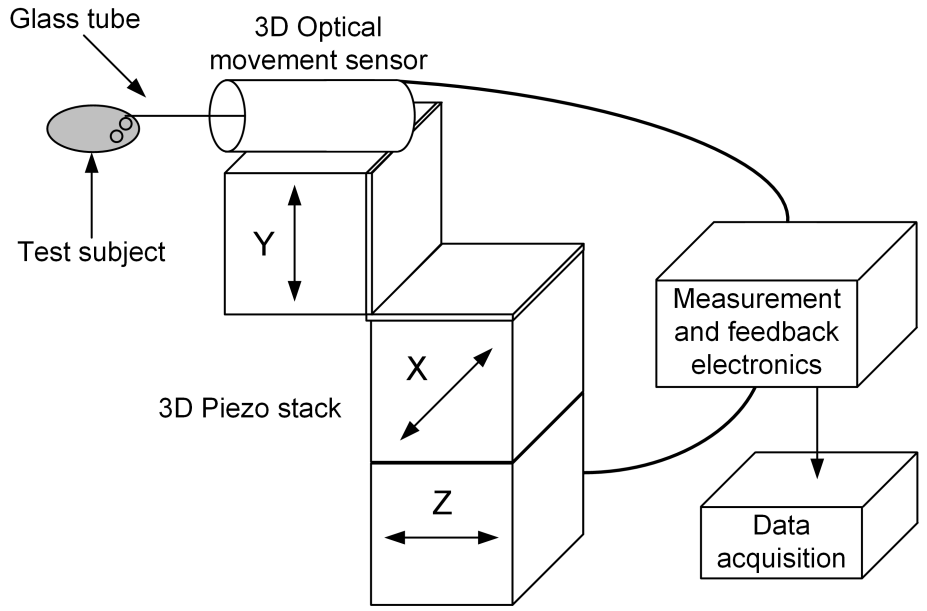

Fig. 4. Structure of the 3D micromotion compensation system.

4.2.1 Movement sensor

Since the movement sensor itself is very light-weight, it is designed to have a resonance frequency of hundreds of Hertz. However, when the sensor is loaded, the resonance frequency can drop sharply. A certain length is also required from the sensor to improve force sensitivity, which is a contradictory requirement in terms of resonance frequency, since a longer beam also has a lower resonance frequency.

The movement sensor is a touch-probe sensor, which detects movement at the tip of a glass tube in three dimensions with very little resistive force. The movement sensor was built around Omron EE-SX1107 photo interrupters. The photointerrupter consists of a light-emitting diode and a photodetector, which are situated on the opposite sides of a fork-like structure. The photointerrupter has a 150 µm wide and 600 µm high slit in front of the detector, enabling precise detection of an object's position. Movement of a light-blocking element between the fork prongs is detected at the current output of the sensor. A capillary quartz glass tube functions as the light-blocking element. The glass tube was sputtered with platinum to make it opaque. The inner diameter of the tube is 100 µm and outer 170 µm. The glass tube is wide enough to block light in x- and

y-directions by itself. A small piece of the same tube was glued to the end of the main tube in a 90° angle to function as a light-blocker in z-direction.

The tube is suspended by a round concentric arc patterned flexible film. It was made of thin brass foil and moves rather freely in three dimensions. The pattern was premachined with Siemens Microbeam laser and then etched with nitric acid. Direct laser machining easily bends thin structures due to heating but prepatterning and etching help to keep the structures straight. The groove pattern was made to a brass foil which had an original thickness of 50 µm. After the etching process the thickness was reduced to 20 µm while pattern dimensions were etched to the desired values. The glass tubing was glued to the hole in the middle of the film and the film itself was clamped between the sensor housing and the rim. The flexible film acts as a spring element and the glass tubing as a rigid probe. The film allows the glass tube to move linearly along the probe z-axis, thus enabling a seesaw-like movement perpendicular to it.

The sensor housing and the rim were machined from brass. Fig. 5 shows a CAD model of the sensor.

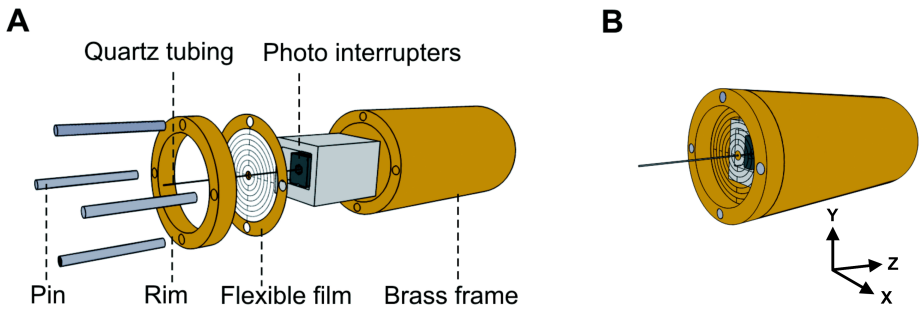

Fig. 5. 3D optical movement sensor construction: a) an exploded view of the 3D movement sensor, b) the complete 3D movement sensor.

Finite element analysis with COMSOL Multiphysics was used to determine the final shape and to verify the operational precondition of the sensor. Good flexibility, good machinability, high force sensitivity and high resonance frequency were used as design criteria. The concentric arc design constructed from brass alloy fulfilled these requirements adequately. Steel film would have provided a higher resonance frequency, but it was found to bend too easily during laser pattering. The sensor housing and the photo interrupters were excluded from the simulations for the sake of clarity and to reduce the mesh size. The finite element model consisted of 32,990 tetrahedral elements.

Forces were added to the tip of the quartz tubing, and corresponding displacements were simulated in Paper III.

Unfortunately we did not have a sensitive enough reference sensor to measure the force sensitivity of our sensor, but the finite element simulations suggest that the force sensitivity is in the range of tens of nN/μm in x- and y-direction and in the range of hundreds of nN/μm in z-direction.

4.2.2 Control electronics

The feedback electronics were built using discrete components, mostly operational amplifiers. A schematic of one axis of the movement compensation electronics is shown in Fig. 6. An op-amp LED driver was used to eliminate LED current variation due to temperature change. A non-inverting sensor amplifier measures the photointerrupter response, amplifies the signal to 5 V supply range and provides it to the analog PI (proportional-integral) control. PI control was chosen over PID (proportional-integral-derivative) to simplify the tuning procedure and to reduce amplification at higher frequencies where it is possible that the mechanical resonances of the components could be amplified. An adjustable resistor in the integrating op-amp circuit acts as the control for the integrator in the PI loop.

Depending on the position of the photon-interrupting flag, light current can either increase or decrease when the sensor head is moved, which could cause a 180-degree phase shift. This issue was tackled by implementing an inverting buffer before the integrator. The power amplifier's adjustable gain provides the proportional tuning in the PI loop and drives the piezo, which is essentially a capacitive load.

4.3 Results

In addition to the results presented in Paper III, compensation performance of the 3D system was tested in realistic measurement conditions by measuring movement from the edge of a blowfly (Calliphora vicina) medulla (Fig. 7). The tip of the glass tube was inserted into the blowfly brain and brain movement was recorded without compensation. Next, the compensation was turned on and after tuning the PI control loop, attenuation of 47%, 73% and 88% at 6 Hz was attained for X, Y and Z axes, respectively.

It should be noted that the amplitude of the movement was quite small, which limited the attenuation percentage. The residual movement itself was close to the noise level.

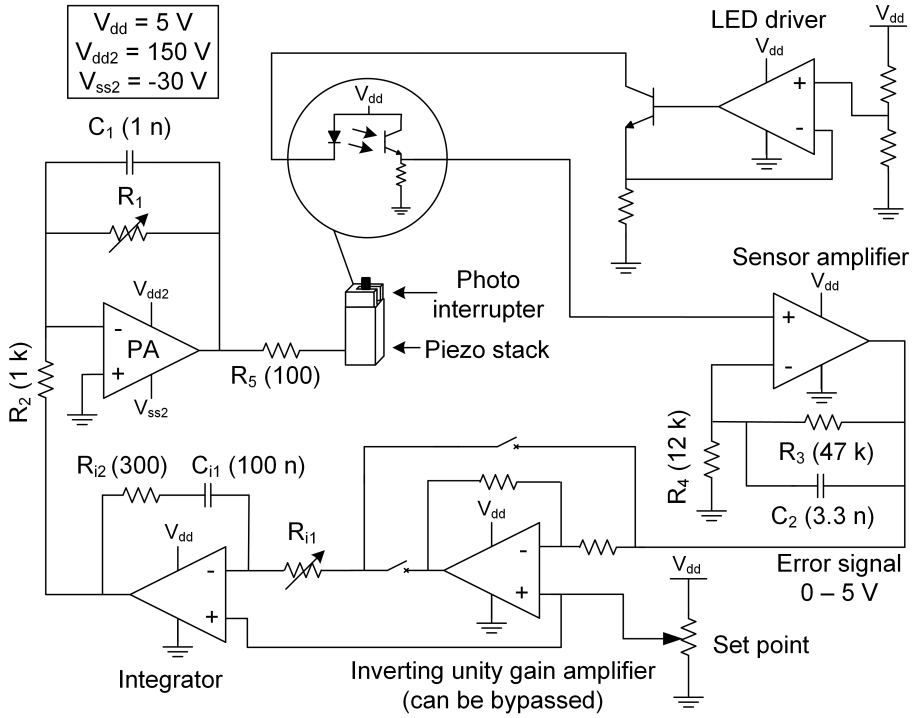

Fig. 6. Simplified circuit diagram of the measurement and control electronics block used in the micromotion compensation system. Presented in Paper III. Used under the Creative Commons Attribution (CC BY 4.0) license.

With a larger and slower movement the attenuation was measured to be 70%, 85% and 98%. Due to the large amplitude, the loop was no longer able to compensate for the whole movement, which is clearly seen on the right side of the first curve in Fig. 8A. Still, the system worked well and the compensation returned after the overshoot.

The results show that with our design up to 98% of the movement can be compensated for. The compensation performance was largely limited by the sensor mechanics and the signal-to-noise ratio at sensor output. Due to the low resonance frequency of the sensor, the control loop bandwidth had to be reduced, which limited the compensation performance.

Ideally all the components would move in the same reference coordinates, but in practice this is not possible. Some cross axis coupling is always present. The cross axis-coupling was measured on two prototype designs and found to be typically

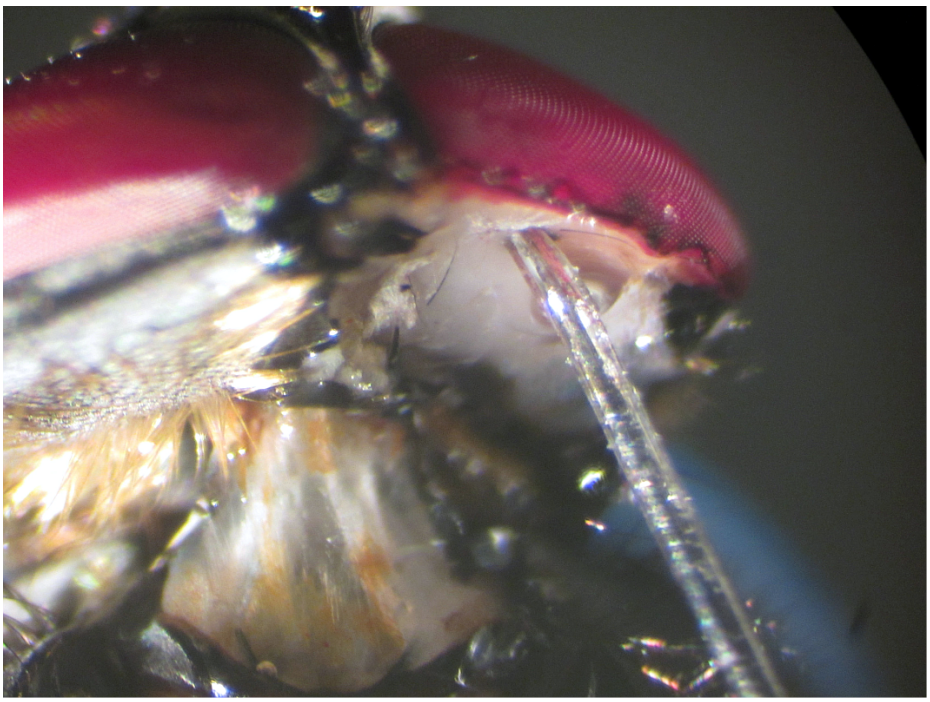

Fig. 7. A photograph through microscope of the glass tube edge inserted into the medulla of a blowfly.

below 10% and maximally roughly 30%. Cross axis coupling depends heavily on the proper alignment of the sensing element placed between the photo interrupters and the alignment between the photo interrupters themselves. Since the coupling is weak, it does not affect the stability of the control loop. It can, nevertheless, slow down the response of the loop to external perturbation.

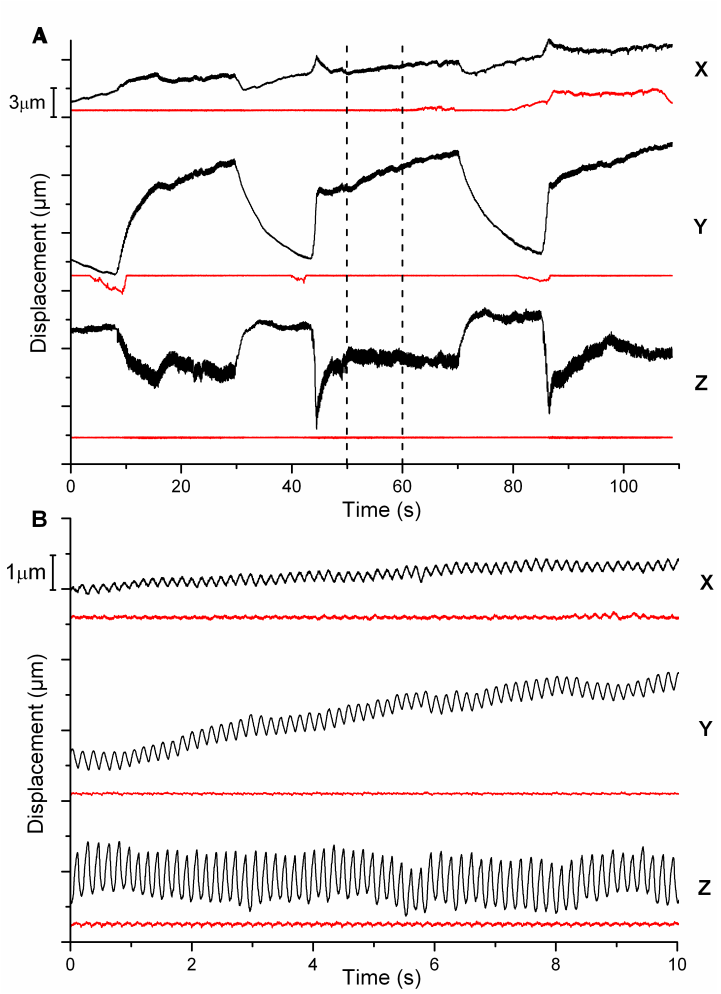

Fig. 8. 3D compensation of medulla movement of Calliphora vicina, recorded before (black) and after (red) applying compensation for each axis: a) recorded 110 s sample, b) magnified 10 s sample (from the dashed section of Fig. A).

5 Neural recording and stimulation system

5.1 System structure

The neural recording and stimulation system is a mixed-signal integrated circuit that contains high-pass filtering preamplifiers for biopotential acquisition, a multiplexer, two post-amplifiers, a successive approximation register (SAR) A/D converter, stimulation circuitry, and control and data read-out logic. A block diagram of the designed circuit is shown in Fig. 9.

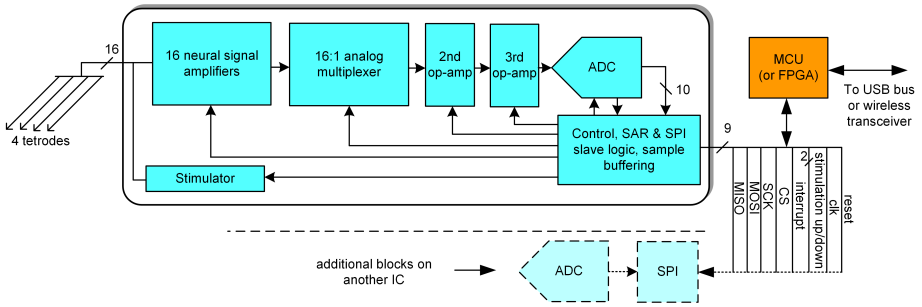

Fig. 9. Block diagram of the entire neural recording and stimulation system. Presented in Paper IV. Reprinted with permission from IEEE.

The SAR A/D converter was selected for the application, because of their very low power consumption and moderately good speed and lack of latency. Various SAR A/D converter structures were evaluated. First, a minimum component topology was simulated where the DAC is also used to sample the input signal. A split-capacitor DAC structure was chosen to reduce the area of the converter. Some problems using this kind of solution were identified in Paper II. The first complication is the short sampling time, which is only a single clock cycle, which with a converter using a 4 MHz clock is 250 ns. This can be doubled if two whole cycles are used, but the conversion time is increased. Such a short sampling time poses a somewhat demanding requirement for the settling time of the op-amp that is driving the sampling capacitance. This was the main reason why a topology with a separate sample and hold circuit was later implemented.

Another problem in the structure was that the voltage over the capacitor banks could momentarily go beyond the supply voltage because of the different timing of switching

transistors and so trigger the source-bulk diode of the CMOS switch that resets the LSB capacitor bank. This could cause significant current spikes, i.e. charge leakage from the sampling capacitor, thus resulting in errors. This problem was especially prominent in a design where the input signal is sampled with the charge scaling DAC. A similar problem was not found in a structure where the input signal is sampled with a separate circuit, as the DAC only follows the voltage that is set by the SAR logic.

5.2 Preamplifier

5.2.1 Choice of input stage

The choice of input stage depends somewhat on the chosen technology, but generally it can be said that a PMOS differential pair has lower transconductance than an NMOS pair, but also has lower 1/f noise, which is an advantage in low-frequency neural signal recording. On the other hand, white noise on the PMOS input pair is slightly higher. This tradeoff depends somewhat on the technology and chosen frequency range, but mostly favors the PMOS input stage when action potential signals are measured, and so most authors have chosen to go with a PMOS input stage. A bipolar input stage provides even better noise performance, but BiCMOS implementations are quite rare since they are more expensive and also suffer from lower input impedance. One BiCMOS neural signal amplifier has been implemented by Rieger (2003) [47] and another by Demosthenous and Triantis (2005) [23].

5.2.2 Preamplifier topology

One simple op-amp topology is the current mirror operational transconductance amplifier (current mirror OTA) introduced to neural signal recording applications by Harrison [13]. The main advantages of the OTA is its low number of components, which translates to low noise and low power consumption and thus high noise efficiency factor (NEF). The OTA can be seen as having two stages, a differential input stage and a cascode output stage, but it is usually understood as a single stage op-amp, since it has only one amplifier stage. The output transistors simply translate the current generated by the transconductance of the input stage into a voltage. The output voltage of the OTA is the output current multiplied by the total output impedance. Using cascodes or a high impedance load the gain can be very high. The main drawbacks are lack of controllability

of the dominant pole, low gain without cascoding and high output resistance. The dominant pole of the OTA is introduced by the load capacitor and thus the high cut-off frequency depends on the amplifier load. In addition to basic current mirror OTAs, folded cascode OTA (Heer 2006 [48], Wattanapanitch 2007 [25]), telescopic OTA (Aziz 2009 [27]) and differential output OTA (Heer 2006 [48], Chae 2008 [26]) have also been used in neural signal recording.

Two-stage Miller compensated op-amps typically contain more poles than the previously mentioned ones. The dominant pole is now formed by the compensation capacitor whose value is more predictable than that of the load capacitor. Gains are comparable to cascode OTAs, but now cascoding is not needed and output swings can be higher. The first amplifier stage is used to provide high gain and the second amplifier stage provides a high output swing. A third source follower stage is often added to provide a low output impedance. A two-stage PMOS input stage op-amp with an output buffer and a single-ended output has been used by Dabrowski (2004) [49], Mohseni (2004) [50], Olsson (2005) [18] and Sodagar (2009) [51], while an NMOS input stage has been used by Obeid (2003) [30]. Differential output versions with PMOS input stage are quite rare, but they have been made by Nielsen [52] (2003) and Mollazadeh (2009) [28]. In our application a high output swing is not needed for the first amplifier stage, since the signal level at this point is small. Also, the op-amp will drive a multiplexer, which is a small capacitive load, and thus the output impedance of the preamplifier can be high.

Since the preamplifier works with a static gain of approximately 40 dB, unity gain stability is not required. Stability is often improved by increasing the gm of the second amplifying stage of the two-stage op-amp and using a nulling resistor to cancel the second pole. The increase in gm is accomplished by making the amplifying transistor W/L ratio large and by mirroring a larger current for the second stage. In our case the current of the second stage was kept at the same level as at the input stage. This both saves power and allows us to drive the input stage with higher current. Leaving out the nulling resistor improves PSRR slightly on higher frequencies, since it is often made out of a PMOS transistor operating on the triode region, and power supply perturbations can couple via its substrate to the output. The chosen topology for the preamplifier is shown in Fig. 10.

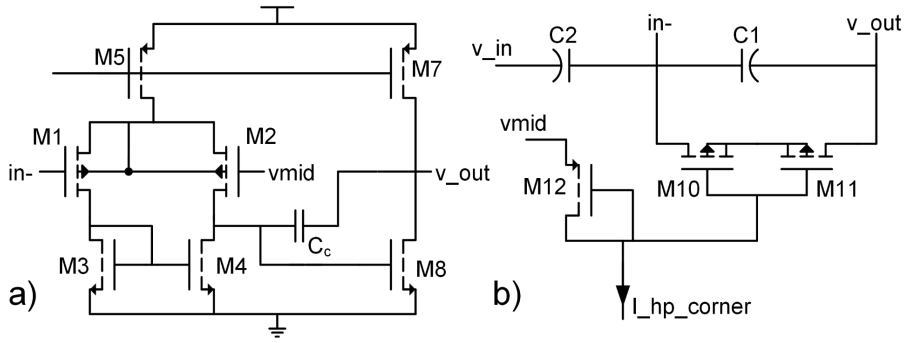

Fig. 10. Schematic of a) the preamplifier and b) its feedback components, first published in Paper IV. Reprinted with permission from IEEE.

5.2.3 Noise performance

The most significant contributor to the op-amp noise is the input stage. In both OTAs and two-stage op-amps, differential input stages are used with current mirror loads. For such a circuit, provided that the transconductance of the input pair is much larger than the current mirror and in the two-stage op-amp case, the input referred noise V_n^2 is given by

$$V_n^2 = 16kT\left(\frac{1}{3gm_{1,2}} + \frac{gm_{3,4}}{3gm_{1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{3,4}C_{ox}f}\frac{gm_{3,4}^2}{gm_{1,2}^2}, \qquad (8)$$

where $gm_{1,2}$ is the transconductance of the input differential pair and $gm_{3,4}$ is the transconductance of the load transistors and K_N and K_P are the 1/f noise coefficients of NMOS and PMOS transistor, respectively, W and L are the width and length of the MOS transistor, C_{ox} is the oxide capacitance and f is the frequency [53]. In a two-stage op-amp the noise from the second stage is negligible, since it is divided by the gain of the first stage when referred to the input. From Eq. 8 we can see that the op-amp noise can be minimized when $gm_{1,2} >> gm_{3,4}$.

In order to reduce the noise coming from the input stage mirror NMOS pair M3 and M4, their W/L ratios were made small. Due to offset minimization, which requires that the W/L ratio of the output stage transistor M8 to the input stage load transistor M4 is twice the ratio of current mirror op-amps M7 to M5, the transconductance of the output stage is also small. This reduces the overall gain and the size of the required compensation capacitor, which sets the bandwidth of the preamplifier.

In Fig. 11, a noise performance comparison between several different amplifier designs is made, including the publication year. The graph made by Mollazadeh et al. has been used as a source and edited to include some newer designs [28]. Since integrated neural signal and stimulation systems often have widely varying features and complexity, different channel counts, and many of them specialize in measuring specific neural signal types, it is useful for comparison to use a single metric such as NEF that is calculated for the preamplifier only. In the aforementioned graph, the bias current consumption and the bandwidth of the preamplifier are also compared.

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{V_T \cdot 4\pi kT \cdot BW}}, \tag{9}$$

where $V_{ni,rms}$ is the input referred rms noise voltage, I_{tot} is the preamplifier supply current, V_T is the p-n junction thermal voltage and BW is the preamplifier bandwidth [54].

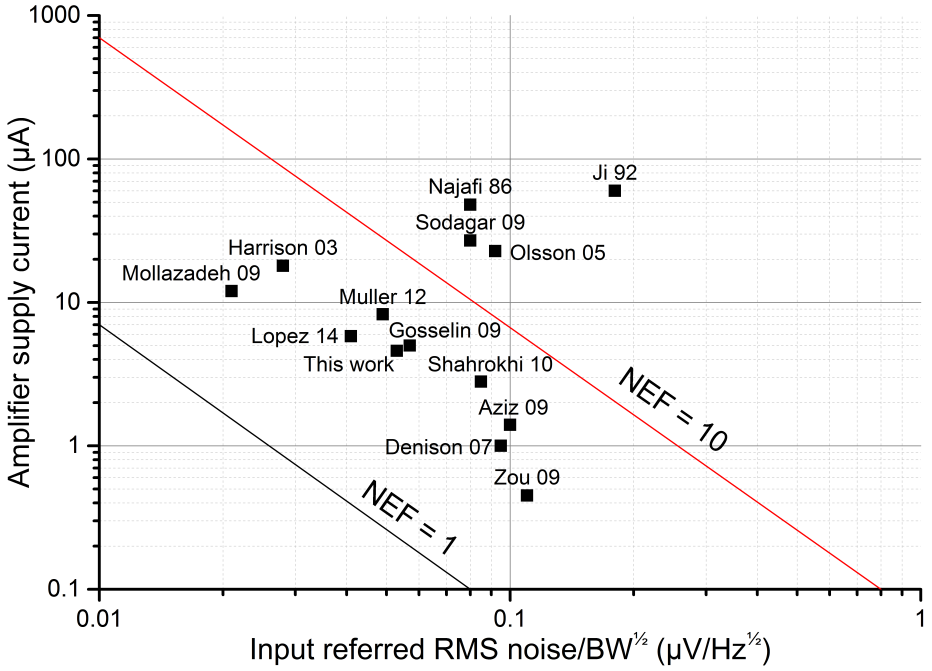

Fig. 11. Comparison between the noise performances of different designs, adapted from [28]. Additional references include Muller (2012) [55] and Lopez (2014) [56].

Rieger (2007) [57] made the observation that single channel systems are typically less noisy than multichannel systems.

5.3 Multiplexing

The multiplexer consists of 16 CMOS transmission gates, which are controlled by a 4-bit digital selection logic made out of 4-input NAND gates and inverters. The transmission gate transistor sizes were kept small to minimize capacitive loading to the preamplifier. As nearly simultaneous sampling of all channels is required (some time delay exists between channels, but it is small compared to the overall time of the neural AP pulse), multiplexer channel selection time is tied to the sampling time. A new channel must always be selected before a sample of the channel voltage is taken. A sampling rate of 20.833 kHz was selected, which is close to the required sampling rate of 20 kHz. This way, the total sampling time of 16 channels is an even 48 µs, giving a sampling time of 3 µs per channel. If the channel count is increased, the sampling time must be reduced or a dedicated A/D converter for each channel bank must be implemented. It would have been possible to also implement a channel selection register to sample one channel with a high sample rate, but this was not done for the sake of reducing circuit complexity. The multiplexer thus runs continuously.

5.4 Post-amplifier topology

The designed circuit contains two post-amplifiers. They provide adjustable gain for the system and the latter amplifier drives the sample and hold capacitors. The first post-amplifier has an adjustable gain of 1X - 10X and the second one has 1X - 5X. Both post-amplifiers are Miller compensated two-stage operational amplifiers. Since unity gain operation was required for these amplifiers, lead compensation was implemented to improve stability. The third op-amp has to settle with close to 10-bit accuracy so that it is not limiting the performance of the system. Due to the sample and hold circuit design choice presented in Section 5.5.1, the settling time requirement is the full conversion period of the A/D converter, which is 12 clock cycles. The A/D converter was designed to work with a 4 MHz clock, which results in a conversion time of 3 µs.

Since the noise of the system is dominated by the preamplifier, the main design parameters for the post-amplifiers are their power consumption and settling time. A two-stage op-amp can be approximated by a two-pole model

$$A(s) = \frac{A_0}{(1+\frac{s}{p1})(1+\frac{s}{p2})}. \tag{10}$$

Here, A_0 is the DC gain and the dominating pole $p1$ is described by

$$p1 = -\frac{1}{gm_2 R_I R_{II} C_C}, \tag{11}$$

where gm_2 is the transconductance of the second stage, R_I is the output impedance of the input stage and R_{II} is the output impedance of the second stage and C_c is the compensation capacitor. The second pole $p2$ is described by

$$p2 = -\frac{gm_2}{C_L}, \tag{12}$$

where C_L is the load capacitance. If the bias current is reduced, the gm_2 is reduced, but the output resistances are increased, reducing the p1 frequency. Operating in strong inversion, gm_2 grows proportional to the square root of the bias current. R_I and R_{II} decrease proportionally to the bias current. When bias current is increased, the dominating pole rises approximately proportional to the bias current to the power of 3/2 and the second pole rises proportional to the square root of the current.

The phase margins of the post-amplifiers change when the amplifier gain is changed. To ensure that the amplifier has a good settling performance with high gain and good stability with low gain, 5-bit bias current tuning was implemented for both amplifiers. This way the bandwidth of the amplifier can be reduced with low gains, improving stability, and increased with high gain, improving settling, keeping the phase margin large with all gain configurations. The simulation was done with extracted layout, which models parasitic capacitances and resistances. The test bench is shown in Fig 12.

The feedback path is broken and a large inductor and a large capacitor were used to make DC feedback in an open-loop configuration. The 2nd mirror op-amp simply loads the phase margin measurement node (PM) by simulating the input impedance of the node in a closed-loop configuration. The gain and bias current of the mirror op-amp track that of the tested op-amp. Fig. 13 shows a contour plot of the simulated phase margin of the first post-amplifier. The line crossing the plot indicates the selected bias points with corresponding gain configurations.

The smallest phase margin is a bit surprisingly found to be with a closed-loop gain of 2. This is most probably caused by the time constant caused by the feedback resistance. In this gain configuration, the resistance seen at the input of the post-amplifier is at its

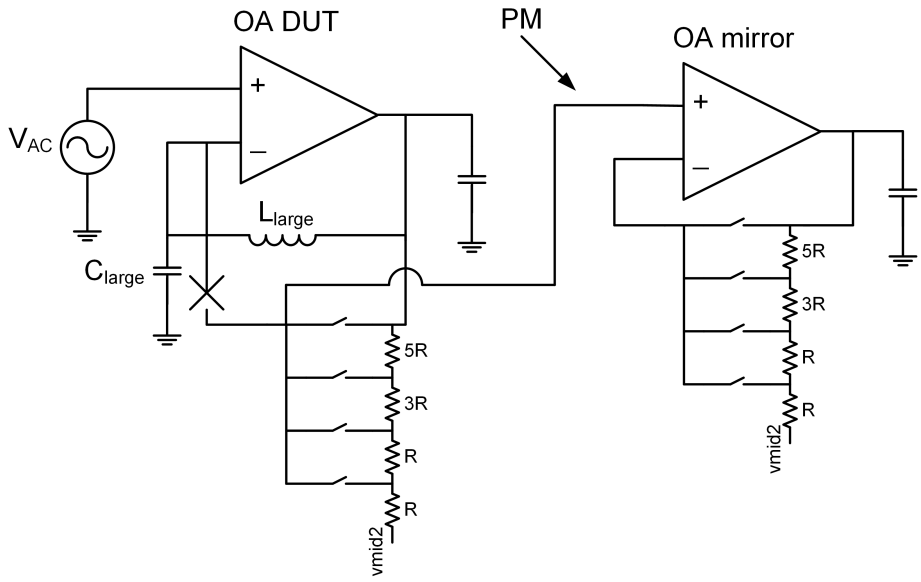

Fig. 12. Op-amp open-loop phase margin simulation test bench with feedback components.

highest. This causes an RC time constant with the input capacitance and a corresponding phase shift. The resistors at the feedback network were constructed out of high resistive polysilicon and they are relatively large: the size of R is approximately 13.3 kΩ. Using large resistors minimizes current consumption and improves matching. The behavior with the second post-amplifier was found to be similar. Testing with a resistor network made out of smaller resistors restored the "normal" behavior: phase margin with the gain configuration of 2 rose above the unity gain phase margin.

5.5 A/D conversion

According to Olsson and Wise [58] there is some disagreement on the requirements for neural signal A/D conversion. This is reflected by the resolution choices made by different authors. A popular architecture has been the SAR A/D converter, used for example by Olsson (5-bit) [58], Shahrokhi (8-bit, 6.2-bit ENOB) [59], Chae (9-bit, although says 6 bits is optimal) [60], Perelman (10-bit, although says 7 bits is enough) [61] and Harrison (10-bit) [14] and Zou (12 bits) [16].

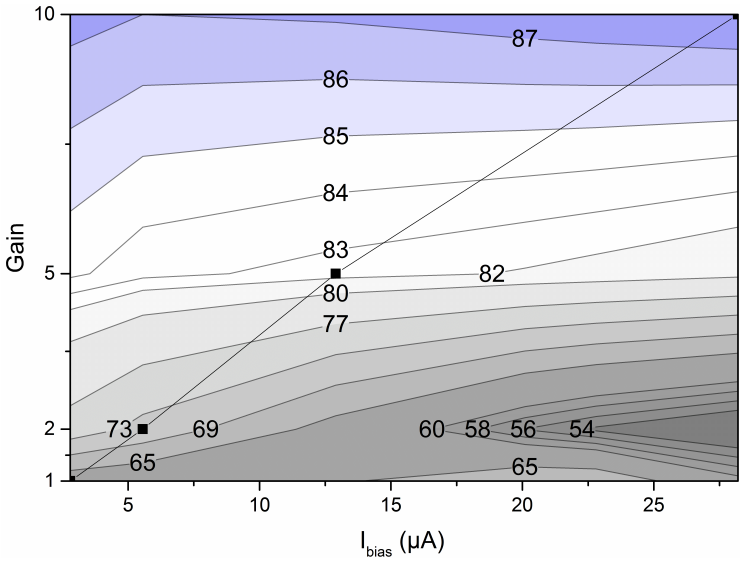

Fig. 13. Simulated post-amplifier phase margin with varying bias current and closed-loop gain.

Another possible solution is the delta-sigma converter which has been implemented by Mollazadeh (gm-C incremental delta-sigma converter) [28] and Roham (Continuous time delta-sigma modulator) [62]. The delta-sigma converter's advantages are its high resolution and inherent low-frequency quantization noise suppression. The disadvantages are low speed and complexity, especially regarding simulation. Some have chosen to use an external data acquisition system. These include, for example, Dabrowski [49], Gosselin [63] and Rizk (12 bits) [64].

One way to calculate the required dynamic range was proposed by Chae [65]. Since neural signals have very small amplitudes ranging from tens to hundreds of microvolts, and the noise level due to the sensor element and measurement environment is also high, the achievable dynamic range is:

$$DNR = 20\,log\frac{V_{signal}}{V_{noise}}. \tag{13}$$

In a best-case scenario of 500 μV neural spike and 10 μV rms noise level, a DNR of around 34 dB can therefore be achieved. DNR and effective number of bits (ENOB) in an ideal A/D converter are related by

$$ENOB = \frac{DNR}{6.02\,dB}. \tag{14}$$

Thus the required ENOB for a neural signal A/D converter is around 6 bits. This calculation, however, divides peak voltages with rms voltages. The rms value of a spike train type signal depends heavily on its duty cycle and therefore also the SNR depends on it. In addition, the A/D converter quantization noise has an effect on the required number of bits. The amount of gain also has an effect and it sets the limit for the required minimum number of bits. In addition, a one- or two-bit margin is added in order to compensate for non-idealities. The most demanding requirement for the A/D converter resolution is set with minimum gain. Since noise adds up quadratically, the overall noise due to the signal noise, op-amp noise and quantization noise is

$$V_{ntot} = \sqrt{V_{nsign}^2 + V_{nopamp}^2 + V_{nq}^2}. \tag{15}$$

Both signal noise and input referred op-amp noise are amplified similarly, but quantization noise depends on the A/D converter resolution. If the signal noise is around 10 µV rms and the input referred op-amp noise is around 5 µV rms, the total noise referred to the input of the first op-amp is approximately 11.2 µV rms. Before A/D conversion it is therefore 1.12 mV rms with the minimum gain of 100. With a 1 mV signal noise at the op-amp output, a 6-bit converter would have a quantization noise that would surpass the signal noise. If we set a requirement that quantization noise can add no more than 10% to the total noise, the required ENOB can be calculated from

$$V_{LSB} = \frac{V_{dd}}{2^N} \tag{16}$$

which gives an rms quantization noise of

$$V_{nqrms} = \frac{V_{LSB}}{\sqrt{12}}. \tag{17}$$

Based on these equations, in order to reach less than 10% additional noise due to quantization with a signal gain of 1000 and a supply voltage of 3.3 V, an 8-bit converter would be required. Olsson and Wise proposed a 5-bit A/D converter based on their measured integrated noise from the 300 Hz - 10 kHz band where the recording site noise was 9.6 µV, noise from the microelectrode circuitry was 8.9 µV and gain before the A/D converter was 1000. With their 5-bit quantization, the integrated noise is increased from 13.1 µV to 15.8 µV [58].

On the other hand, if we want to be able to detect very small spikes from the vicinity of the noise and use a gain that is adjustable from 100 to 10,000, the reference voltage of a 5-bit converter must be set very low, or a higher resolution A/D converter would be required. If the input referred noise is around 11.2 µV rms, we would like to be able to detect spikes that barely rise above this level. The typical neural spike detection and sorting threshold is about 60 µV [66]. With a gain of 1000, an A/D converter with an ENOB of 11-12 could resolve a spike that is just above the noise rms voltage. Such a small amplitude reading is probably not reliable, but a spike occurrence can probably be detected. On the other hand, with a low resolution converter the same requirement can be achieved by scaling the reference.

To reach the same input referred resolution as a 12-bit converter with a 3.3 V reference, a 5-bit converter's reference voltage would have to be 3.3 V divided by 128 and that of a 6-bit converter by 64. These converters could not measure large output voltages and their reference voltages would be much more sensitive to noise. A 5-bit converter with a 0.5 V reference that could still barely measure close to 500 µV neural spikes with a gain of 1000 could be used to measure multiples of the noise rms voltage.

For our design we chose a 10-bit SAR converter with a separate sample and hold stage. The topology, presented in Paper IV, is shown in Fig. 14. The chosen topology does not require an external reference voltage. The converter works with a 3 V supply voltage.

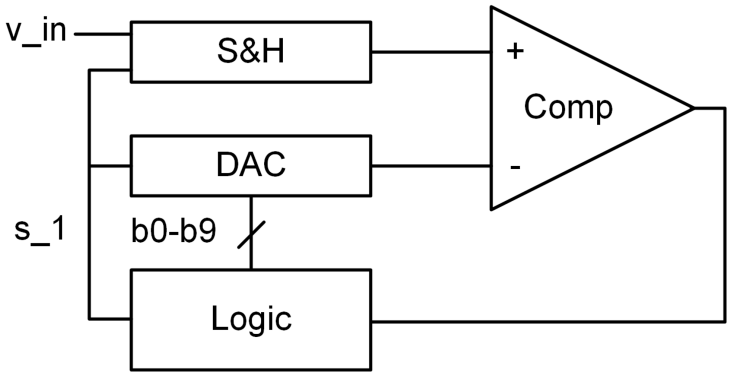

Fig. 14. Block diagram of the designed A/D converter. Presented in Paper V. Reprinted with kind permission from Springer Science and Business Media.

5.5.1 Sample and hold

The sample and hold circuit, shown in Fig. 15, is a double sample and hold structure. The circuit contains two 1.6 pF sampling capacitors that are switched alternately. While one capacitor is sampling the output of the post-amplifier, the other one is connected to the comparator input. This helps to alleviate the settling time requirement for the post-amplifier driving the sampling capacitor. Instead of one or two clock cycles, the op-amp can settle for the full multiplexer switching period. A non-overlapping clock circuit generates the sampling timing.

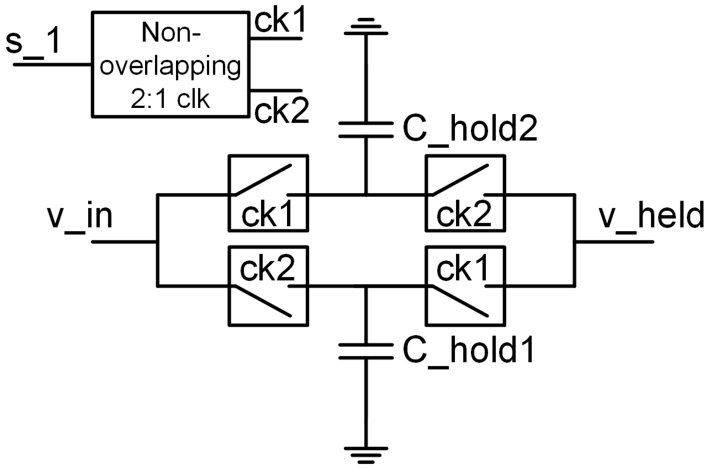

Fig. 15. Dual sample and hold circuit. First presented in Paper IV. Reprinted with permission from IEEE.

5.5.2 Comparator

The comparator is a two-stage rail-to-rail input latched comparator. The design is based on previously designed topologies implemented by Chin (2010) and Lan (2011) [67], [68]. The comparator contains an adaptive power control (APC) circuit that shuts off the input stage after the latch has settled. The APC circuit is timed so that the input stage is turned on before the latch is turned to the evaluate state. With this structure the comparator consumes dynamic power only.

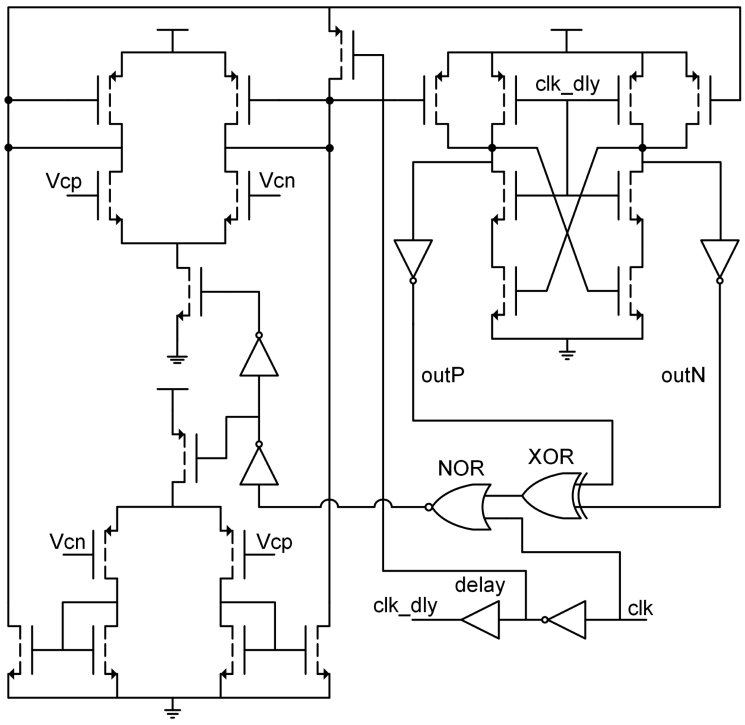

Fig. 16. Two-stage latched comparator with adaptive power control. First presented in Paper IV. Reprinted with permission from IEEE.

5.5.3 DAC

A split-capacitor structure, shown in Fig. 17, was selected for the DAC to reduce the required chip area. The implemented topology has been previously described by Agnes (2010) [69]. Compared to a traditional split capacitor DAC, this design has a unit sized attenuation capacitor instead of a fractional one and both MSB and LSB banks have an equal number of unit capacitors. In a traditional fractional design, the attenuation capacitance is calculated by

$$C_{attn} = \frac{\text{sum of LSB capacitors}}{\text{sum of MSB capacitors}}, \tag{18}$$

where the sum of MSB capacitors is equal to the sum of LSB capacitors minus one unit capacitor [70]. In a traditional 10-bit design the attenuation capacitor size would have been 32/31 unit capacitors.

The implemented topology causes only a small gain error and improves the symmetry of the layout. The capacitors are driven with an inverter bank of 10 inverters, which are placed close to the edge of the capacitor bank in order to isolate the DAC from the digital switching noise of the logic block.

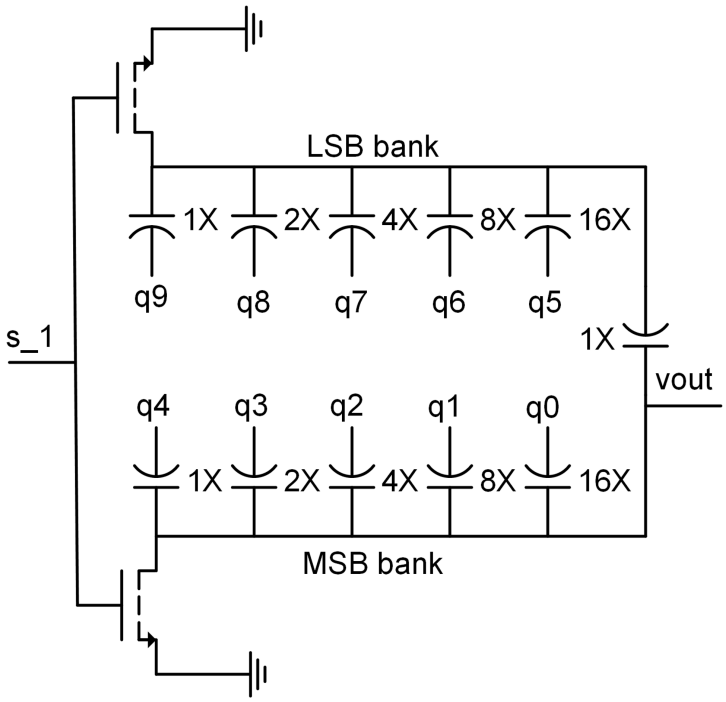

Fig. 17. Split-capacitor DAC used in the SAR converter. First presented in Paper IV. Reprinted with permission from IEEE.

5.6 Stimulation

The circuit includes a 16-channel stimulation circuit, shown in Fig. 18. In order to save chip area and power, the same stimulation current is used for each channel. The stimulation current configuration register includes 7-bit current setting values for both cathodic and anodic current. The stimulation circuit on the chip is a simple current output DAC programmable current mirror. The DAC has 5-bit binary weighted switches and 10X and 100X current switches. The stimulation current can be adjusted via the SPI

bus from ±50 nA to ±160 µA. On the prototype the stimulation current DAC also has an optional external biasing input, which makes the generation of smaller or larger stimulation currents possible.

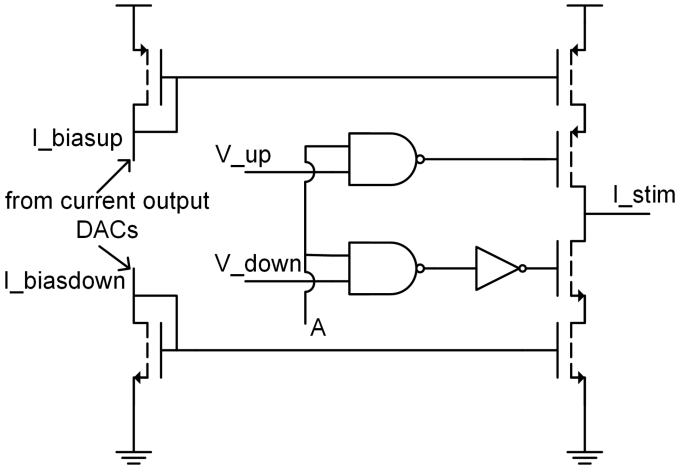

Fig. 18. Biphasic stimulation circuit. Presented in Paper V. Reprinted with kind permission from Springer Science and Business Media.

Each channel has a stimulation enable switch between the I/O pad and the preamplifier so that specific channels can be configured for either measurement or stimulation. With signal A, stimulation excitation to channels that are not configured for stimulation is suppressed. As this was the first prototype of the chip, no special care other than layout matching was taken in order to achieve precise current values. The stimulation times are externally programmable and should be set so that the charge moves in equal amounts into and out of the electrode. Charge balance can be adjusted by tuning the stimulation times. If the charge balance requirement is not satisfied, the voltage on the electrode can rise or drop beyond the supply voltage of the IC, and current injection ceases. Small differences in the amount of transferred charge was not believed to saturate the channel, since the electrode-solution capacitor continuously leaks current.

Since it is possible that a net charge injection can cause chemical reactions in the neural interface that can lead to cellular damage and deterioration of the electrode, another popular possibility for rejecting DC current is the use of a large blocking capacitor in series with the neural probe to reduce the DC current to negligible values (less than 1 nA). Periodically discharging the blocking capacitor may be necessary.

Some methods for balancing the charge movement with and without a blocking capacitor have been presented in the literature [71], [72], [73].

5.7 Control logic and data transmission

In Table 1 the required data transmission rates for different information types are compared. It can be seen that for only 16 channels the required data rate for waveform information transfer is over 3 Mbps. Additional requirements, such as timing information or data transmission overhead required by the communication protocol, have not been taken into account.

Table 1. Required transmission speeds for different data types, adapted from [74].

Signal Type	Spike + LFP Wform	Spike Wform	LFP Wform	Spike Time	LFP Energy
ADC Resol.	10-bit	10-bit	8-bit	1-bit	6-bit
Sample Rate	20 kS/s	20 kS/s	500 S/s	1000 S/s	20 S/s
No. of Ch.	16	16	16	16	16
Data rate	3.2 Mbps	3.2 Mbps	64 kbps	16 kbps	1.92 kbps

Data transmission was implemented on the chip with microcontroller (MCU) backend electronics in mind. Generally they are easier to implement and more cost-effective than FPGA implementations. For a higher number of channels (>64) an FPGA and a separate buffer memory are likely necessary. With the current MCU, which is a 32-bit Atmel UC3A3256, it is possible to address up to 15 devices with 4 chip select lines and an external decoder. The tests were made with an evaluation board (EVK1104) which had only two external SPI connections.

Verilog hardware description language was used to implement digital blocks such as an SPI slave interface on the IC. SAR logic for the A/D converter was also embedded in the logic block. Sampling and a counter for multiplexer timing were a part of the SAR logic block. Nine configuration registers with varying lengths from 5 to 8 bits for programming gain, bias current, high-pass frequency corner and stimulation current values were also implemented. The IC also contained two 20x8-bit conversion result buffer register banks. The converted 10-bit results were organized and stored into these registers so that the first 8 MSBs were stored in the first four registers and the 2 LSBs of each conversion result were combined into one register. The position of the first channel

could be identified based on an incrementing stamp byte that was transferred before the first 8-bit register. In total there were 42 8-bit registers out of which 21 were transmitted in one burst, resulting in a total data rate of 21 x 8 x (1/48 µs) = 3.5 Mbps.

Once one of the buffers is full, an interrupt signal is toggled for the backend read-out electronics. The backend electronics detects the signal value change and identifies the full half of the buffer register bank based on the signal state. Once the signal state has been detected, write and read commands are sent to the IC. The SPI logic on the IC operates at SPI mode 0, which means that data is read on the rising edge of the clock and then written on the falling edge. Since the data in and data out lines are separate, the SPI logic is capable of full-duplex communication. The SPI module also contains modules for read and write command detection. The read register address is either incremented automatically, or a specific register can be addressed by adding an address value to the read command byte. If the 2nd 21x8 buffer register needs to be read, an address value (21) that points to the first byte of that register bank must be written.

The MCU was programmed using Atmel Studio 6.2. The MCU acts as an SPI master and data transmission between the SPI bus and the USB CDC (communication device class) device happens in one interrupt routine. The interrupt routine is activated every time the interrupt signal is toggled. First, the data in the USB buffer that buffers chip configuration data from the PC is read to the MCU. After this, the full register on the IC is identified based on the interrupt signal state. Then, a write command is sent via the SPI bus to the IC and the received chip configuration data from the USB buffer is written to the IC followed by a read command. The write command byte is followed by a separate address byte, whereas the read command byte also contains a 7-bit address value. The read address is incremented automatically on the IC. The MCU sends a new read command every time the interrupt signal is toggled. The data read via the SPI bus is immediately transmitted to the USB bus and to the PC. It was found that using additional buffering, such as storing the data in an external SDRAM, was not needed, and the data is streamed reliably to the PC using only the internal buffers.

On the PC side, a C# program was written to capture the data from the USB bus. The MCU acts as a USB CDC device and appears as a virtual COM port on the PC. This makes it simple to interface to the port on the application side. The program contains a simple GUI and communication with the serial port. The program writes the received data in binary format to the disk. The program also contains configuration settings for the IC so that the chip can easily be reprogrammed. The files are then read into Matlab for post-processing, which includes organizing, filtering and plotting the data.

5.8 Results

Simulations of the developed IC were presented in Paper IV. Bench-top measurement results of the IC were presented in Paper V. Additional findings are presented in this chapter. A microphotograph, also presented in Paper V of the designed integrated circuit, can be seen in Fig. 19. The core of the circuit is surrounded by a 44 I/O pad ring. The digital I/O and digital supply pins are located on the right side of the chip. There is a cut on the top and bottom part of the ring that separates the digital I/O from the analog I/O. On the core, the 16 preamplifiers are located in a U-shaped pattern (turned 90° clockwise) on the left side of the circuit. The multiplexer, post-amplifiers, bias and high-pass filter corner frequency tuning DACs and the stimulation circuit are located in the middle of the chip. The A/D converter is bottom right and the logic block is top right.

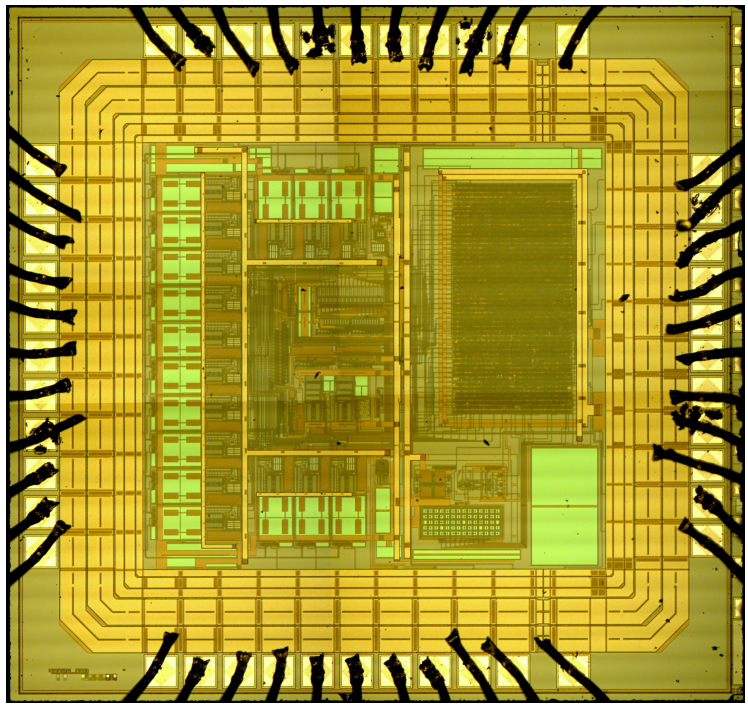

Fig. 19. Photo of the designed integrated circuit presented in Paper V. Reprinted with kind permission from Springer Science and Business Media.

Action potential signals were measured with extracellular tungsten electrodes having an impedance of 400 kΩ - 500 kΩ at 1 kHz. The thickness of the electrodes was 1 mm and they were insulated with epoxylite and had an etched contact surface of approximately 1 µm in diameter. Connected to the 10 pF input capacitor of the preamplifier, the probe impedance causes less than 3% signal attenuation. The measurements were made using one standard preparation in electrophysiology teaching laboratories, the isolated cockroach (Periplaneta americana) leg. The leg, the electrodes and the test board were placed inside a Faraday cage and the test board was powered by a lithium-ion battery. The backend electronics were placed outside the cage and powered by the USB bus from a battery powered laptop. The recording electrodes were inserted into the shank and thigh of the leg and the reference electrode into the leg haemolymph from the severed side. Unused channels were tied together with the reference. A gain setting of 1000 was used and the high-pass filter corner frequency was set around 300 Hz. A photo of the measurement setup is shown in Fig. 20.

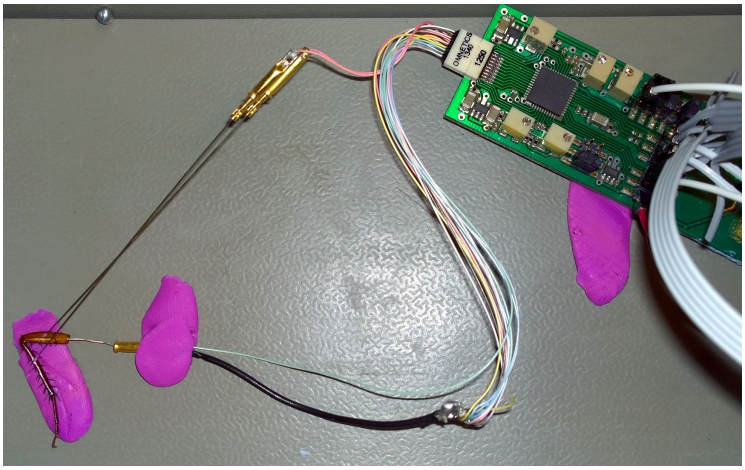

Fig. 20. Cockroach neural signal measurement setup.

The electrodes are likely to record both spontaneous activity in the mechanosensory axons and also activity triggered by mechanical stimulation, like vibrations of the recording base or air turbulence displacing the mechanosensory sensilla (e.g. by blowing) [75], [76]. Fig. 21 shows the action potential spikes measured without external excitation. Different amplitude levels correspond to signals from different nerve cells, the strongest one being closest to the probe. Fig. 22 shows the response

to mechanosensory stimulation: a series of high-density pulses is triggered by the airflow moving the sensing hairs of the leg. The voltage readings are at the output of the amplifier chain.

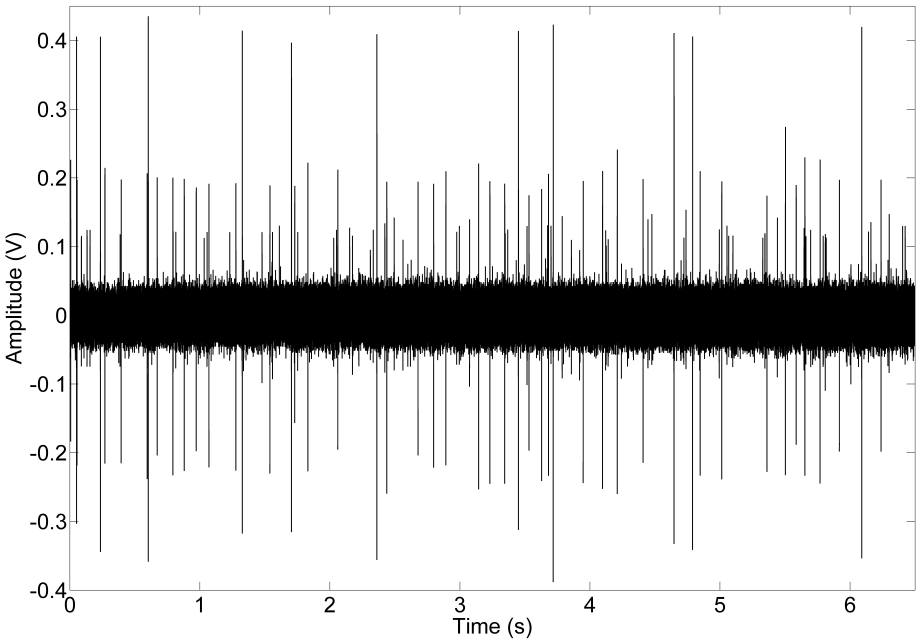

Fig. 21. Measured neural signal data without excitation. Different amplitudes correspond to nerve signals coming from neurons at different distances of the probe. Measured with a gain of 1000.

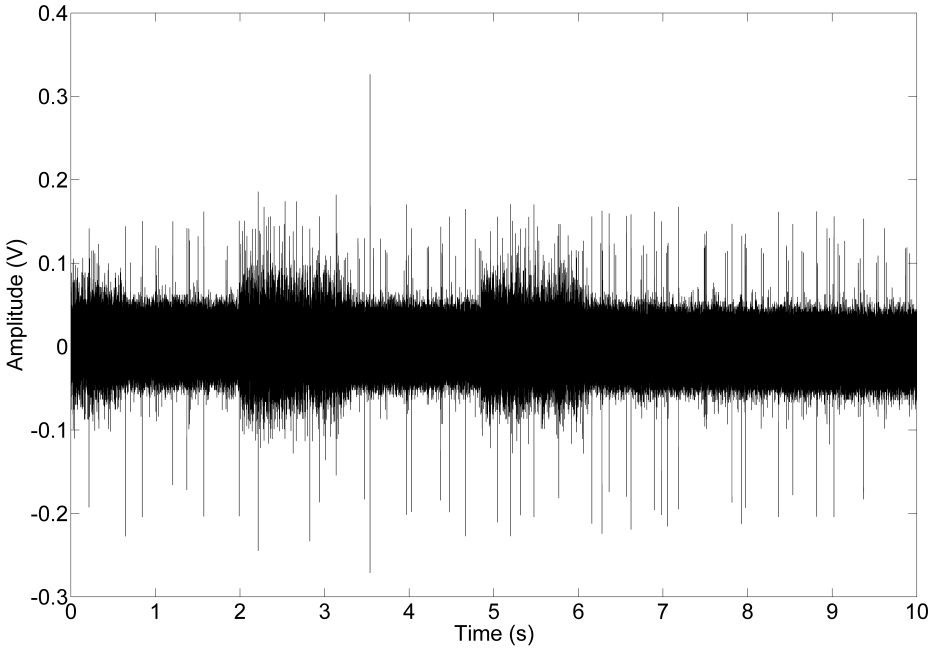

Fig. 22. Measured neural signals with excitation to mechanosensory sensilla. Measured with a gain of 1000.

6 Discussion and future work

6.1 Future work related to the micromotion compensation system

The present implementation of the motion compensation electronics is built using discrete electronics. An integrated implementation could include several improvements, such as a current-limited piezo driver to increase reliability. This device could be integrated using a high-voltage process. Digital tuning of the control loop and the set point could also be implemented. At the moment the control axes are calibrated manually. As the compensation bandwidth is narrow, a full digital control is also possible. This would allow easy rotation of the coordinates, if needed (this would require one matrix product, i.e. nine multiplications). Digital control also gives more degrees of freedom for damping the mechanical resonance of the probe.

In the author's opinion, the most difficult aspect of this design is developing a micromotion sensor that could also house a measurement electrode. While our developed sensor is an important proof-of-concept and a step to that direction, building a mechanically robust sensor with high force sensitivity and high mechanical resonance frequency is a difficult task. This development area would require additional resources and mechanical design expertise.

6.2 Future work related to the neural recording and stimulation IC

The designed prototype published in Paper V contained 22,682 transistors according to Cadence's layout verification software Assura on a chip area of 3.722 mm^2. The design was fully functional, but had some issues. The gain of the PMOS input side of the rail-to-rail latched comparator was slightly lower than required, causing a large INL error in the upper conversion region (2 V - 3 V). This issue did not show in transient DNL and INL simulations but resulted in a large INL in the measurements. Two missing codes were also detected from the A/D converter output, probably caused by the same issue. This issue can be fixed in the next development version of the chip. The current chip worked well with only $\sim$0.1 LSB DNL error, provided that the post-amplifier DC bias was tuned so that the converter only had to work on the linear region.

The harmonic distortion performance of the pseudoresistor element has some room for improvement. Currently, the 2nd harmonic was measured to be 36 dBc with a 500 µV

rms input signal using a high-pass filter corner frequency value of approximately 200 Hz. The distortion dropped significantly, close to 60 dBc, when the high-pass filter corner frequency was moved below 10 Hz. This seems to implicate the pseudoresistor as the main culprit: the distortion increases as more current flows through the pseudoresistor.

Future developments could include increasing the number of channels on the IC and canceling channel-specific offsets by periodically changing the reference voltage of the post-amplifier. This could be implemented with a DAC and a set of configuration registers that could be programmed via the SPI bus. One register for each channel would be required since the offset value would have to change periodically. If the design were to be implemented using a process with smaller line width such as 0.18 µm, power savings could be achieved especially on the digital side due to reduced gate capacitances and parasitic capacitances. Having a smaller supply voltage (1.8 V is the maximum for 0.18 µm) would also mean power savings and make having some form of offset minimization practically mandatory, if a large gain (5000 or more) would still be a requirement. Using 5 V gates for the stimulation circuit and the I/O ring would mean that larger stimulation currents would still be possible. If smaller noise is set as another goal, the new chip should have a smaller preamplifier bandwidth to minimize noise folding. If the channel count is increased, running the mid-supply line through all amplifier stages could present a new problem. The length of the metal strip would mean that the impedance seen by each amplifier could vary significantly from one chip edge to another and also increase the possibility of interference coupling.

Future developments could also include an integrated data compression algorithm. Analog on-chip delta compression of neural data has been previously implemented by Aziz (2009) [27]. Data reduction methods such as delta compression are suitable for neural recording circuits due to the pulse-like nature of neural signaling. In principle delta compression followed by run-length encoding algorithm is useful with slowly moving signals. However, neural data is noisy, which limits the usefulness of the delta compression algorithm. Reducing the number of bits to decrease the delta would alleviate this problem but increase quantization noise. If the fluctuation between pulses is of no interest, it is wasteful to transmit uncompressed data between the pulses.

Implementing data compression schemes would require different kind of data buffering compared to our design. Using data compression methods it could be possible to reduce power consumption and keep high channel count implementations within the capacity of the SPI bus. Currently it seems that the data transfer from the SPI bus to the USB bus would be the bottleneck with higher channel count systems. Without data

compression some sample buffering to an external SDRAM would be necessary. The high-speed USB bus itself should be able to handle more than ten times the current effective data rate.

6.3 Wireless transmission

Implementing a wireless transmission system is usually the last step in building complete neural signal data acquisition systems. There are two general architectures for placing the electronics for neural signal recording. The first one is to implant all of the electronics inside the test animal. This sets very strict requirements for wireless data transmission, since it is usually the worst offender regarding power consumption. If data needs to be transmitted from several recording sites and with a high bit rate, it is very difficult to keep power consumption down. In implanted systems, where the circuit itself is located in biological tissue, heat generation due to power consumption will also become a problem. Some data reduction techniques have to be implemented, such as sending only the time and amplitude information of the neural spike. This will limit the data transmission requirement, as shown in Table 1. To further reduce power consumption, the transmission distance will have to be very short. For example, inductive links that transmit data just outside the skin have been used by Harrison (2007) [14].

Harrison presented a 100-channel wireless system where digital spike location data was sent at 330 kbps with an 433 MHz FSK transmitter over an inductive link. Fully integrated neural signal wireless FM transmission has also been implemented by Mohseni in 2005 [77] where 3 electrodes transmitted analog waveform at 94-98 MHz to a distance of 50 cm with an SNR of around 9 dB. Both of these designs dissipated only milliwatts of power. Roham [62] used a similar transmitter in 2009 and achieved a 381 μW transmitter power consumption for a distance of 25 cm. Sodagar presented in 2009 [51] a 64-channel inductive link where an external transmitter transmits data to a computer. The implanted transmitter is powered by the wireless link itself and consumes around 13 mW. Spike detectors are again used, but in this paper they can detect both positive, negative and biphasic spikes. The data rate is 2 Mbps. The system contains an 8-bit converter, or optionally the analog spike detector output can be sent directly. If an implantable chip that is inductively powered via a wireless link is designed, it will be hard to transmit full action potential waveforms with several measurement electrodes due to the high data rate requirement.

Commercial implementations of wireless links that transmit with high data rate require and dissipate a lot of power. Due to their high power consumption, very few neural recording systems with a WLAN interface have been implemented. A 6 mW consuming fully integrated Ultra Wide Band (UWB) transmitter was designed by Chae (2009) [60]. This complex design includes integrated 40 dB gain amplifiers, 9-bit A/D conversion, spike detectors and maximum 90 Mbps wireless data transmission from 128 channels all built in 0.35 µm CMOS. As demonstrated by Chae, UWB transceivers are one promising transmission type for fully implantable solutions. Such transceivers can reach data rates of 480 Mbps and consume mere milliwatts of power. One such design uses integrated components, a class E and a class A two-stage amplifier which consumes less than a milliwatt and can transmit over 50 Mbps, designed in 0.18 µm CMOS [78]. While UWB transceivers are an attractive option, they are susceptible to signal blocking from WLAN and other wireless networks due to the wide band receiver requirement and therefore require filtering for such signals.

Besides short range UWB transmission, high-speed or medium-speed data transmission methods that could be implemented in a small neural recording IC are lacking. IEEE standards such as the Wireless Body Area Network (WBAN) standard limit the data rate to 10 Mbps and thus leave high data rate neural recording outside of the scope of the standard [79]. Commercially, the situation is even worse. Due to their short range of ten meters and 2-4 meters with the highest data rates, UWB transceivers were superseded by the more power hungry 802.11n/ac/ad WLAN transceivers.

The second way is to implant only the amplifier and move the wireless transmission unit outside of the animal. This is usually the safest and simplest way, although a wired link will increase the chance of infection and is therefore undesirable in human applications. If large batteries are used, higher data rates are possible through a WLAN circuit, and more complex signal processing can be used (for example microcontrollers or FPGAs) on the waveform information. This kind of systems can consume several hundred milliwatts of power. This kind of design has been implemented by Obeid (2004) where a wearable embedded 486 computer had a WLAN card [80]. Rizk (2009) implemented one system where it is claimed that the whole FPGA is implantable and can be powered through an inductive link, but in case that is not enough, another FPGA is also put outside of the body [64]. This system had a commercial 1 Mbps transmitter. The power consumption and size of systems which contain FPGAs or MCUs that are not part of the backend electronics are most likely too large for implanted applications.

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