# MODELING, DESIGN AND DEMONSTRATION OF THROUGH-PACKAGE-VIAS IN PANEL-BASED POLYCRYSTALLINE SILICON INTERPOSERS FOR HIGH PERFORMANCE, HIGH RELIABILITY AND LOW COST

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# MODELING, DESIGN AND DEMONSTRATION OF THROUGH-PACKAGE-VIAS IN PANEL-BASED POLYCRYSTALLINE SILICON INTERPOSERS FOR HIGH PERFORMANCE, HIGH RELIABILITY AND LOW COST

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*To my grandma, my parents, and my wife*

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# SUMMARY

Interconnections between integrated circuits (ICs) and print circuit boards (PCBs) are primarily achieved currently with organic packages at low I/O pitch. Organic packages, however, have limitations in increasing these I/Os due to their poor thermal and dimension stabilities for them to be fabricated as fine pitch interposers. To address these challenges, silicon interposers have been developed and manufactured. Current silicon interposers, based on through-silicon-via (TSV) techniques, however, suffer from high production cost because of expensive CMOS (Complementary metal-oxide semiconductor) processes and small wafer sizes. They also suffer from electrical loss issues in spite of thin $SiO_2$ layers. In addition, the thin $SiO_2$ layers can also lead to reliability problems. To address these issues, this research, for the first time, presents an entirely different approach by proposing and demonstrating polycrystalline silicon in large panel form, which is widely used in solar industry, as an interposer material at much lower cost.

The objective of this research is to study, explore and demonstrate thin panel-based, low-resistivity polycrystalline silicon as a suitable interposer material to achieve high electrical performance at lower cost with reliable through-package-vias (TPVs) for interposer applications. A thick, low loss polymer, with double-side processing, has been developed to address the electrical challenges presented by the much lower resistivity of polycrystalline silicon panel. The TPV structure in polycrystalline silicon, combined with polymer coating with low Young's modulus, is also proposed to achieve reliability under

thermal cycling. Such polymer layers can also help to improve the handling and processing of thin panels.

Both electrical and mechanical models have been developed for the polymer-lined TPV in polycrystalline silicon panels. Parametric studies have also been carried out. The fabrication of TPV in polycrystalline silicon has been developed without any carriers for handling and processing the thin panels. The fracture strength, which is critical in handling and processing large thin panels, has been fundamentally quantified by using both four-point bending tools and Weibull plots. Surface liners are used to improve the handling of silicon panels and the results are quantitatively studied. Several TPV formation methods and mechanisms are explored, including UV laser, excimer laser and picosecond laser ablation. The technical approach for the liner formation involved polymer-filling of TPV, followed by laser ablation to form an "inner" via, leading to in-via polymer liners with controlled thickness. The mechanisms of both silane treatment to improve polymer-silicon adhesion and polymer filling are discussed. The TPV metallization consists of a low cost, double-side all-wet electroless copper seed layer, followed by Cu electroplating. By integrating all these processes, polycrystalline silicon interposer test vehicles have been demonstrated with up to four metal RDLs (redistribution layers) and characterized for their insertion loss. The model-to-hardware correlation has also been carried out. Reliability test vehicles are fabricated for thermal cycling tests and SEM (scanning electron microscope) cross-section imaging.

The key contributions and novelty of this study are as follows:

- First demonstration of TPV in polycrystalline silicon to achieve
    - High performance

        - High reliability
        - Panel-based approach for potential low cost
- Simpler TPV vs. traditional TSV
        - Large size polycrystalline silicon panel vs. small size single-crystalline silicon wafer
        - Laser-based TPV vs. DRIE (deep reactive-ion etching)-based TSV
        - Simpler process with reduced number of steps vs. complex processes for TSV
- In addition, demonstration of double-side processed dry film polymer in TPV with
        - Low dielectric loss to improve TPV performance
        - Low modulus to act as stress buffer in TPV
        - Improvement on handling of thin polycrystalline silicon panels

# CHAPTER 1

# INTRODUCTION

The rapid development of microelectronic systems, such as smartphones and tablets, has fueled the growing interest of improving the advanced packaging technologies, including: a) higher performance, b) smaller form factor, c) multi-functionality, d) better reliability and e) lower cost. Such a need continues to drive rapid transistor scaling with system-on-chip (SOC) [1]. However the implementation of SOC has several critical issues including design complexity, fabrication challenges and high cost. More importantly, transistor scaling following Moore's law is being predicted to reach performance and cost barriers beyond 16 nm technology node [2]. Therefore, in order to continue miniaturizing the size of electronic systems, the industry focus has begun to shift to three-dimensional (3D) integration techniques, such as 3D IC (integrated circuits) stacking enabled by through-silicon-vias (TSVs). Georgia Tech Packaging Research Center (GT-PRC), on the other hand, proposes 3D interposer with through-package-vias (TPVs) to package entire system with the concept of system-on-package (SOP) technology. Such concept tends to eliminate the gap between ICs, packages and print-circuit-boards (PCBs), aiming to revolutionize the system functionality with smallest system size and lowest cost, yet achieving high performance and good reliability [3]. The schematic cross-section drawing of SOP has been shown in Figure 1.

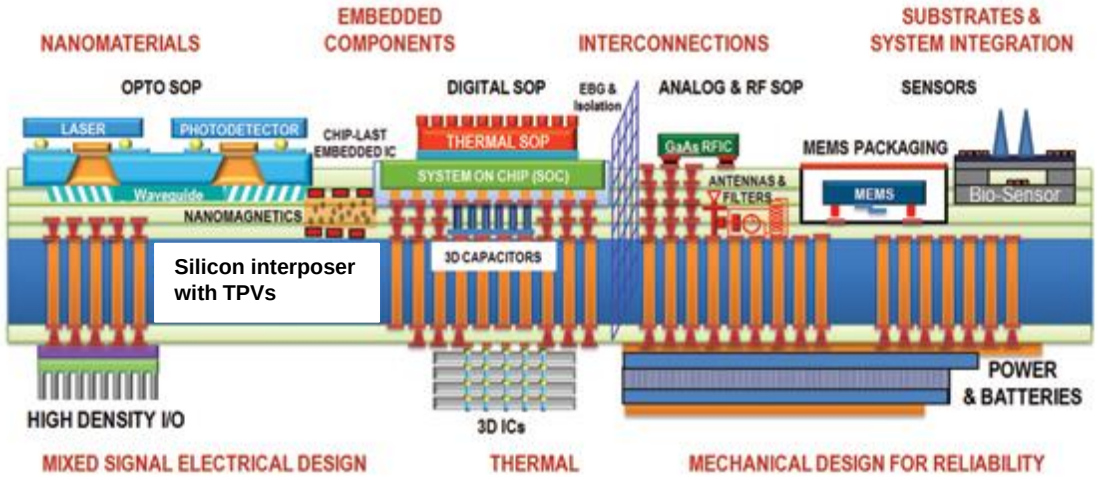



**Figure 1. SOP concept for 3D system integration (Prof. Tummala)**

As presented in Figure 1, TPVs in the interposer serve as the high-density interconnections between different components and are important for enabling the SOP concept for next generation 3D system integration. Hence this study is focused on modeling, design and demonstration of TPVs in the interposer, targeting at high performance and reliability with low cost.

### 1.1 Evolution of Interposer Technology

Interposers by definition connect ICs with fine pitch I/Os (Inputs/Outputs) on the top side and to BGA (ball grid array) packages on the bottom side with larger-pitch with flip-chip assembly. Currently, the package approach for interconnections is mainly based on organic packages at low pitch and not as interposers [4, 5]. But interposers are necessary for pitches below 40 microns. Organic substrates are limited in achieving this pitch, due to poor dimensional and thermal stabilities and high CTE (Coefficient of Thermal Expansion) [6]. Therefore silicon interposers with TSVs processed on passive silicon wafers are being pursued [7, 8]. The fabrication of such traditional silicon

interposers with TSVs usually involves the well-known Bosch process to form blind vias in single-crystalline silicon wafers. Inside these TSVs, thin layers of $SiO_2$ are widely used as the liners to insulate the lossy silicon. There is also the need for diffusion control between copper inside TSV and silicon, which is typically accomplished by using barriers such as Ti, TiN and TaN. The Cu seed is then formed using sputtering process and the via is then filled with Cu by electrolytic plating. A CMP (chemical mechanical polishing) process is necessary to expose the Cu vias. Figure 2 is a typical traditional silicon interposer with TSVs from Xilinx [9].

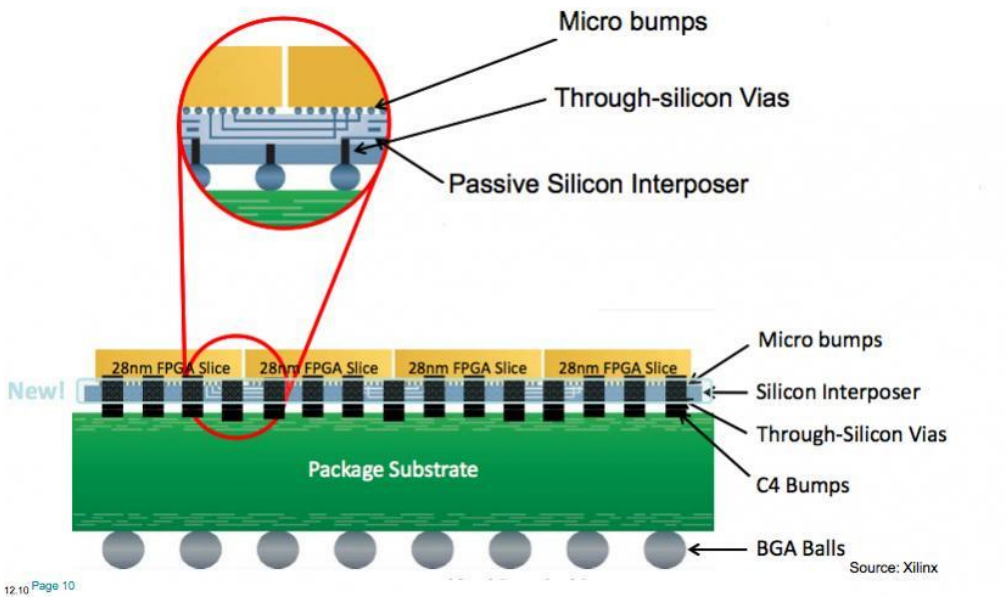



**Figure 2. Schematic drawing of traditional silicon interposer (Xilinx)**

Although silicon interposers have been developed to address the limitations of organic interposers, they have their own challenges [10, 11]. Since the number of interposers coming from 200 or 300 mm silicon wafers is low, particularly if the interposers are large, 50-60 mm in size, serious cost concerns remain as the biggest barriers for adoption of silicon interposers. The high cost is also attributed to the

expensive process to form TSVs as well as the process for single-side redistribution layers (RDLs). Additional challenge with silicon interposers is to do with electrical loss of silicon in spite of $SiO_2$ dielectric layer. This is always recognized as the second major concern with traditional silicon interposers. The thin insulation layer can also result in reliability problems, leading to cracking, current leakage and finally signal loss.

### 1.2 Rational of Polycrystalline Silicon Interposers with TPVs

This study tends to address the shortcomings of traditional silicon interposers by presenting an entirely different approach. The strategy of interposer technology of Georgia Tech Packaging Research Center is a panel-based polycrystalline silicon aimed at lowering the total cost of fabricating the interposer that includes raw polycrystalline silicon cost as well as all other materials and processes required to form the interposer wiring with high performance and reliability.

The top view of the 200 μm polycrystalline silicon panel used in this study is shown in Figure 3. Polycrystalline silicon panels have been widely used in photovoltaic industry as the substrate material for solar cell applications. The manufacturing process for polycrystalline silicon panels is summarized in Figure 4 [12, 13]. In this particular study, solar-grade polycrystalline silicon panels are used. The fabrication process of polycrystalline silicon panel starts with sand or quartz. Metallurgical-grade (MG) silicon is obtained from the reduction of silicon oxide in the presence of carbon, followed by chemical refinement through various gasses to achieve solar grade polycrystalline silicon. Such silicon is then transformed into ingots by directional solidification. Finally the large ingots are cut to blocks and wire-cut to form polycrystalline silicon panels. The specific process has led to lower purity and resistivity of solar grade polycrystalline silicon in

contrast to electrical grade single-crystalline silicon. But the manufacturing costs are also reduced significantly.

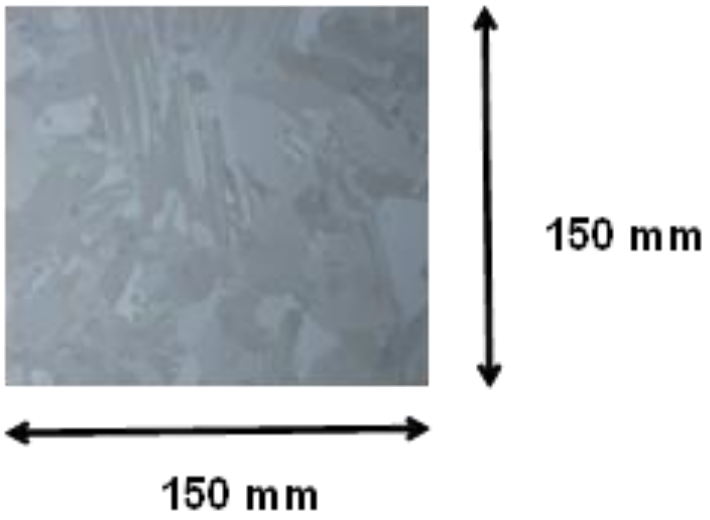



**Figure 3. Top view of the polycrystalline panel used in this study**

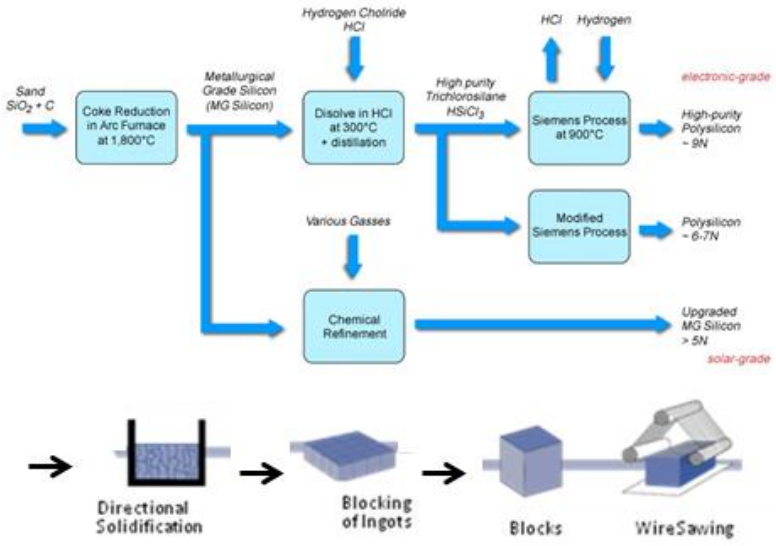



**Figure 4. Manufacturing process for polycrystalline silicon panels [12, 13]**

Polycrystalline silicon panel to form the interposer substrates has a few advantages, namely: simpler and cheaper to fabricate than single-crystalline wafer and

can be scaled to large sizes, up to 700 mm, as shown in Figure 5. More importantly, the larger size substrate means, it yields more numbers of interposers. Figure 6 presents a comparison of 700 mm by 700 mm square panel versus 300 mm round wafer, in yielding numbers of 25 mm by 25 mm interposers. As the calculation shows, the large-size panels (729) produce about 8X more interposers than from 300 mm wafer (89), promising to lower the cost of single unit interposers.

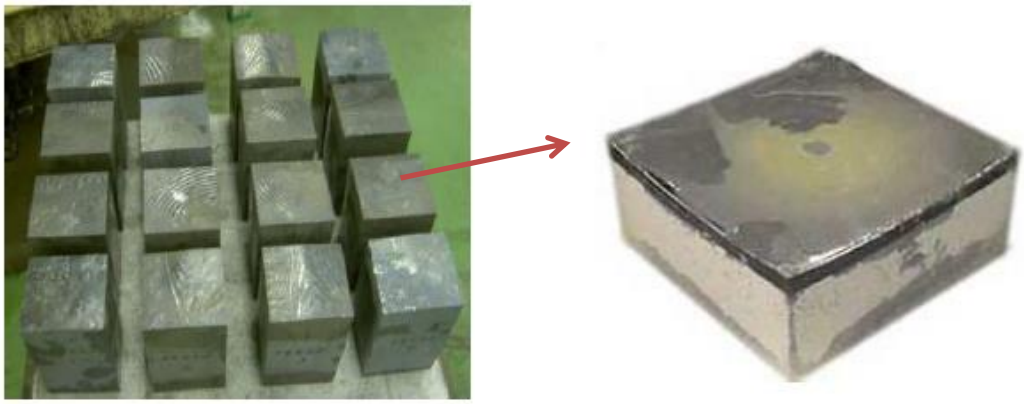


**Figure 5. 700 mm x 700 mm polycrystalline silicon blocks [13]**

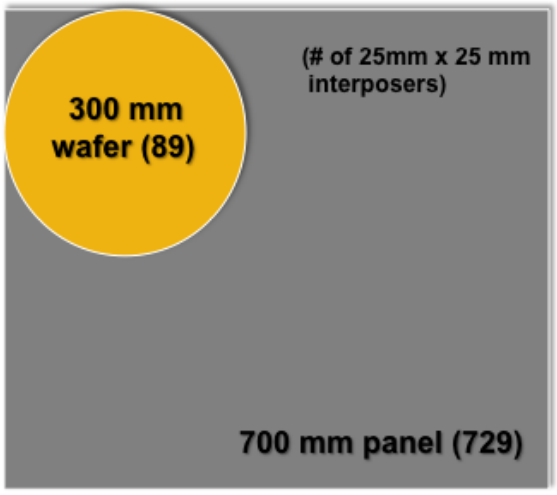



**Figure 6. Comparison of large square panel versus round wafer (GT-PRC)**

Furthermore, the double-side process for fabricating the TPVs simplifies and replaces the costly steps used in TSV techniques. Figure 7 breaks down the cost for TSV fabrication process. It can be seen that for particularly high cost processes such as etching and liner formation, TPV presents a significantly simpler process with reduced steps, leading to lower production cost. Steps such as wafer thinning and bonding/de-bonding are also completely eliminated.

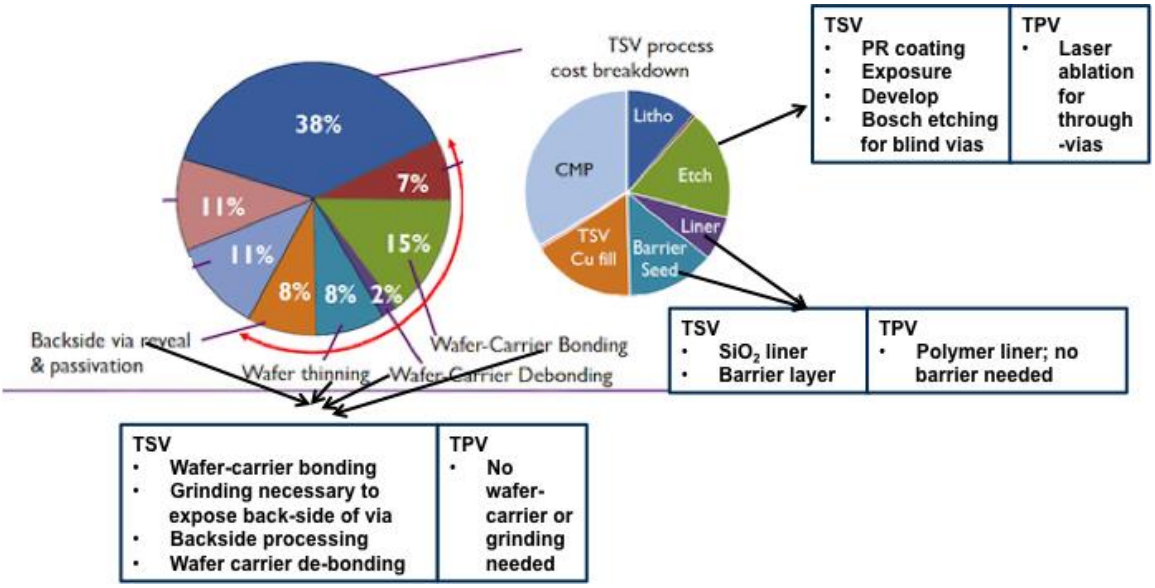
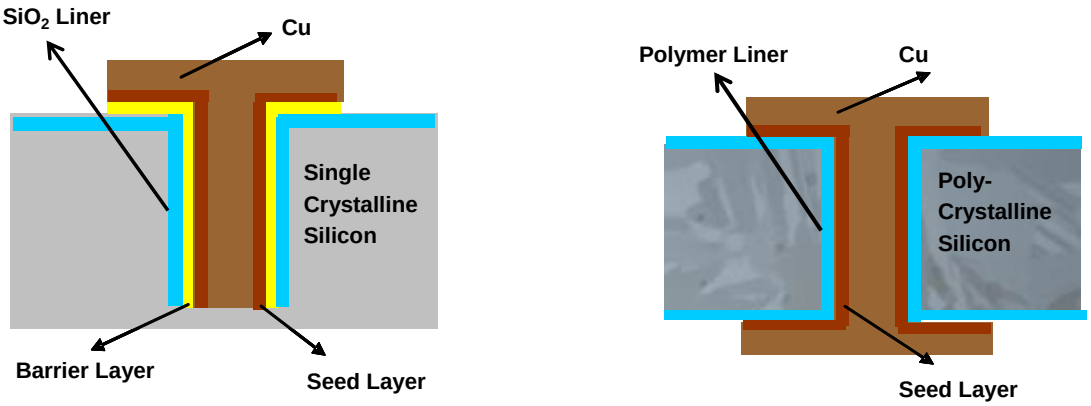



**Figure 7. Cost breakdown of TSV process (modified from IMEC [14])**

Besides lower cost than traditional silicon interposers, the polycrystalline silicon interposer also targets at higher performance and reliability. Figure 8 illustrates a cross-section schematic, comparing TSV in traditional single-crystalline silicon interposers with TPV in proposed polycrystalline silicon interposers. Table 1 summarizes and compares substrate size and key process steps in two technologies. In the TPV process, thick polymer liner is proposed to replace the combination of thin $SiO_2$ and diffusion barrier layer for TSV. Such a low loss polymer material improves the electrical

performance of TPVs in comparison with the low resistivity of the polycrystalline silicon substrate. Furthermore, the polymer material presents good mechanical properties such as low modulus, which help to achieve good reliability of TPV under thermal attack.




(a) (b)

**Figure 8. Schematic cross-section comparison between (a) TSV in traditional Si interposer and (b) TPV in proposed polycrystalline Si interposer**

**Table 1. Through-via processes in single-crystalline silicon interposer vs. proposed polycrystalline silicon interposer**

| | Traditional Si Interposer | Polycrystalline Si Interposer |
|---|---|---|
| Material Form | Single-crystalline silicon wafer | Polycrystalline silicon panel |
| Manufacturing Size | 200~300 mm | Up to 700 mm |
| Hole Formation | Bosch process (Need polishing to expose via on the back side) | Laser ablation |
| Liner Formation | $SiO_2$ by CVD (chemical vapor deposition) + Barrier by PVD (physical vapor deposition) | Double-side polymer filling and laser via |
| Seed Layer | Sputtering | Electroless plating |
| RDL Process | Single-side process | Double-side dry film lithography and plating |

In general, the proposed polycrystalline silicon interposer has the potential to achieve the same performance as the traditional silicon interposer at significantly lower cost, for the following reasons:

1) A panel-based approach that is as much as 8X larger substrate size using polycrystalline silicon
2) Polycrystalline silicon is a lower cost material than single-crystalline silicon
3) Lower cost TPV processes not requiring Bosch process for TSV and $SiO_2$ liner
4) Thick polymer liner within TPV, for higher performance and higher reliability
5) Double-side, low cost process for fabrication of RDLs

A cross-section schematic of the polycrystalline silicon interposer with TPVs and assembly of multiple ICs is presented in Figure 9. The double-side approach used in integrating the components on both sides results in a reduced interposer size, leading to miniaturized packages at even lower cost. This study presents a first, pioneering research to explore polycrystalline silicon in large panel form as a low cost and high performance interposer. It presents a combination of materials and processes to form TPVs and RDLs.

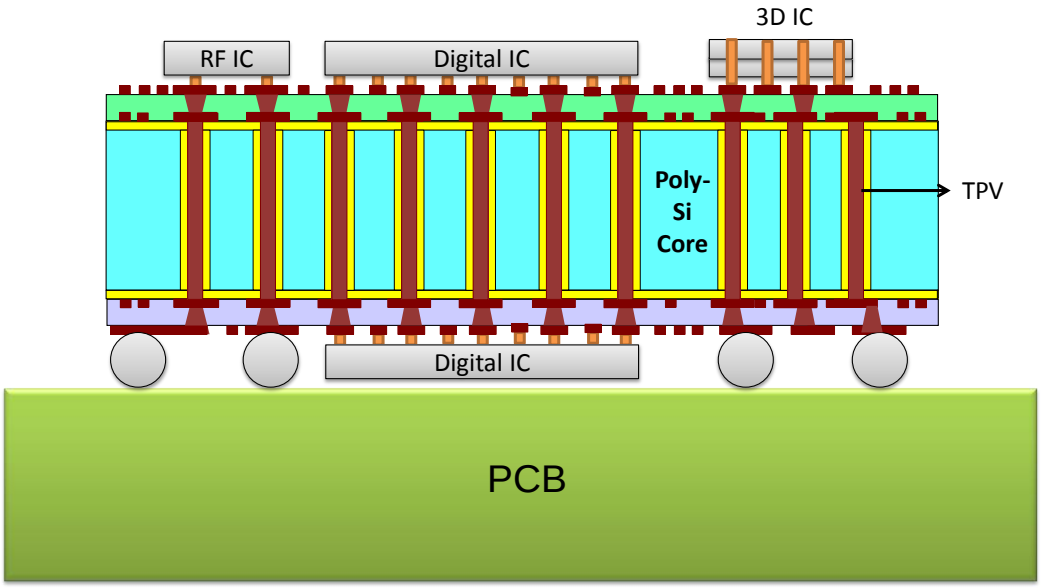



**Figure 9. Cross-section schematic of polycrystalline silicon interposer with TPVs, RDL wiring and assembly with different ICs on both sides**

### 1.3 Research Objectives, Challenges and Tasks

The objective of the proposed research is to explore and demonstrate thin polycrystalline silicon as a suitable interposer material to achieve high performance and high reliability but at lower cost. The critical parameters, which this study is targeting, are listed in Table 2. The high electrical performance and reliability are proposed to be achieved by development of the thick polymer liner with low electrical loss and low modulus.

**Table 2. Comparison between TSV and TPV**

| Parameters | TSV in traditional silicon interposer | TPV in polycrystalline silicon interposer |
|---|---|---|
| 1. Electrical Performance | Low performance due to thin $SiO_2$ insulator | High performance with thick insulating polymer |
| 2. Reliability | Failure due to thin $SiO_2$ cracking or breakdown | High reliability due to low modulus polymer liner |
| 3. Cost | High cost due to<br>• Small wafer size, up to 300 mm<br>• High process complexity | Lower cost due to<br>• Low cost of polycrystalline silicon<br>• Large panel size, up to 700 mm<br>• Simpler double-side process with reduced steps |

To achieve the above goals, three main research challenges are identified:

a) High electrical performance: Due to its lower purity level, polycrystalline silicon material presents a much lower resistivity (0.5 Ω-cm) than the traditional wafer. Hence addressing this higher loss and yet achieve higher performance is a major challenge.

b) TPV reliability: achieving reliability in spite of the CTE mismatch between Cu and polycrystalline silicon.

c) Handling and processing: Polycrystalline silicon is a brittle material and it has never been studied as the interposer substrate. So the handling of the thin substrate and its processability to form interposers are very critical.

To address these challenges, three research tasks are proposed and carried out. The details are organized into following chapters. Chapter 2 summarizes the prior art of

research in fabricating traditional TSVs and in polycrystalline silicon. Chapter 3 describes the electrical and mechanical modeling and design of TPVs in polycrystalline silicon. Chapter 4 addresses the challenges in handling and fabrication of TPVs in polycrystalline silicon, including via formation, liner fabrication, and metallization. Both the electrical and reliability characterization of TPVs in fabricated-polycrystalline silicon interposers are summarized in Chapter 5. The final chapter, Chapter 6, summarizes the key contributions and future extensions.

# CHAPTER 2

# LITURATURE SURVEY

The previous chapter discussed the motivation for TPVs in polycrystalline silicon research, and defined the research objectives, fundamental challenges and research tasks. This chapter summarizes the prior art literature on traditional silicon interposers with TSVs and polycrystalline silicon materials.

## 2.1 Prior Art on Silicon Interposers with TSVs

The first research on silicon interposers dated back to the 1980s by IBM and Bell Labs [15, 16]. The early silicon interposers were fabricated on small wafers with copper-polymer re-distribution layers, but without TSVs, and had to be interconnected to the system using wire bonds. The development of TSV processes in the 1990s and 2000s led to thin silicon interposers with TSV interconnections to packages or printed wiring boards (PWB) [17, 18]. Most of the recent research has focused on TSVs in single-crystalline silicon for high-density 2.5D interposers. This section provides a brief overview of TSV and TSV-based interposer research pursued in both industry and academia.

### 2.1.1 Electrical Modeling and Performance of TSVs

The high electrical loss of silicon and the performance limits of TSVs were identified as a key motivation for this research. This section reviews selected published literature in the electromagnetic simulation and characterization of TSVs.

Bandyopadhyay [19, 20] presented an accurate equivalent circuit model for TSVs by considering the semiconducting effect of silicon substrates. The need for low capacitance signal vias to reduce the propagation delay was highlighted. A parametric study was performed on TSV capacitance, leading to a recommendation of small via diameters and thick liners for improving signal TSV performance. Other options proposed to reduce the TSV capacitance and improve TSV performance in single crystalline-silicon include the use of low-k dielectrics, high-resistivity silicon substrates, and TSVs filled with low work function metals.

The insertion loss of TSVs was studied by Xu [21, 22], where the effect of different TSV configurations on TSV performance was analyzed using 3D electromagnetic solvers. It was shown that TSVs of smaller height and radius reduced the insertion loss. Swaminathan [23] also reported simulation results for TSVs with 15 μm radius, 100 μm height and with 0.1 μm thickness of $SiO_2$. However, it was observed that the obtained insertion loss (Figure 10) was higher than expected for TSVs with such short lengths.

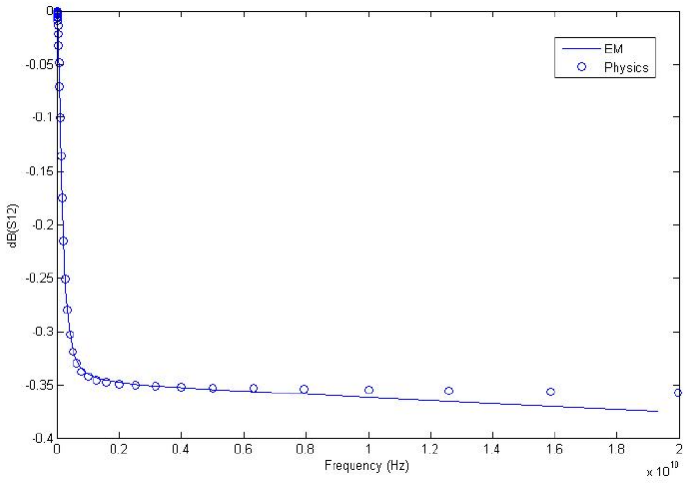



**Figure 10. Typical insertion loss simulation for TSVs [23]**

As mentioned in Chapter 1, the electrical performance of the silicon via is limited by the lossy silicon substrate. Thick oxide layers and high resistivity silicon substrate reduce the insertion loss, but are viewed as high cost solutions. Therefore, the electrical performance issues remain a fundamental challenge for traditional silicon interposers with TSVs.

### 2.1.2 Mechanical Modeling and Reliability of TSVs

The second fundamental challenge for silicon interposers with TSVs is their thermo-mechanical reliability, driven by the difference in CTE (Coefficient of Thermal Expansion) between Cu of 17 ppm/$^{o}$C and silicon of 3 ppm/$^{o}$C. There have been a number of published studies on the mechanical modeling and reliability analysis of TSVs in single-crystalline silicon, but no publications on polycrystalline silicon TPV reliability.

Liu [24-28] have reported extensively on the finite element modeling (FEM) simulations of the stress distribution in copper filled TSVs. These models showed that the stresses in the Cu/$SiO_2$ interface and in the $SiO_2$ layer lead to potential failure mechanisms in TSVs, such as liner delamination and cracking. Arrays of TSVs with 40 μm diameter and 260 μm height were fabricated and characterized to verify the modeling results. X-ray diffraction (XRD) was used to measure the average stress distribution in the TSVs and to determine the stress-free temperature in the Cu. These parameters were used as inputs in the finite-element models for better accuracy. The TSV samples that were reliability tested by thermal shock from -55℃ to 125℃ for 4000 cycles showed both delamination of the Cu/$SiO_2$ interface and cracks in the $SiO_2$ liner (Figure 11). Liu also reported in a later publication [29] that a low modulus SU-8 polymer helped to improve the TSV reliability due to a “cushion effect” (Figure 12).

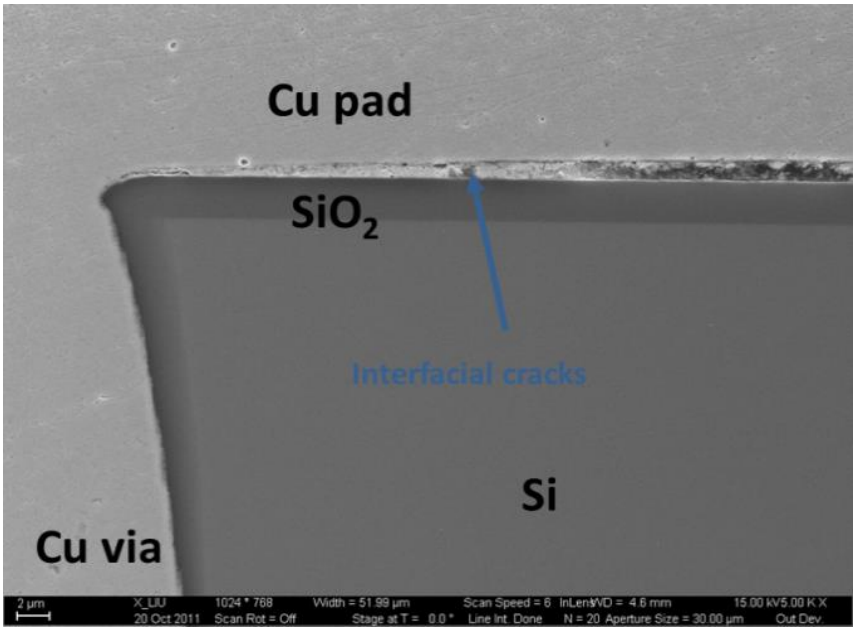



**Figure 11. Interfacial crack around $SiO_2$ [25]**

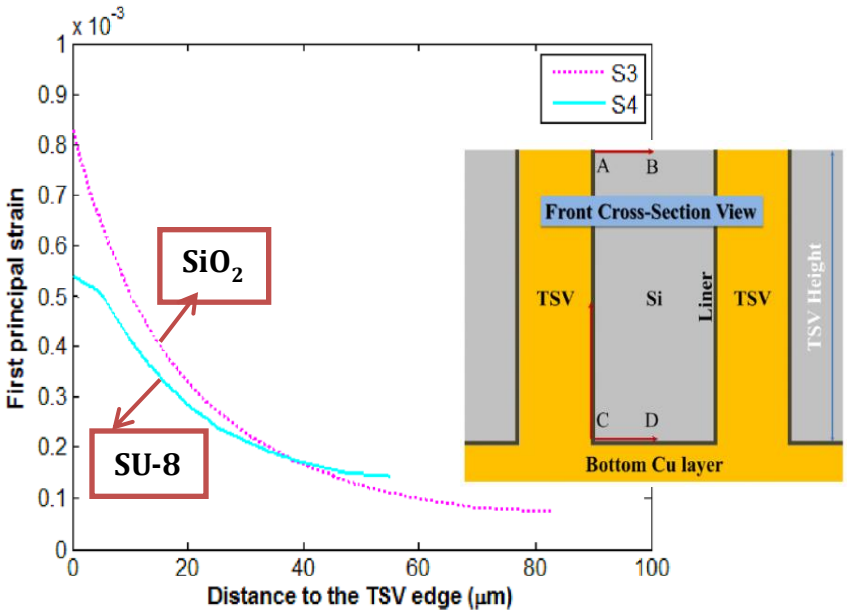



**Figure 12. Cushion effect due to polymer material [29]**

Cassidy [30] studied TSV reliability with blind vias of 250 μm depth and 100 μm diameter. The oxide liner thickness was 400 nm, and the conformally plated metal had a nominal thickness of 200 nm. Key parameters impacting the reliability, such as residual stress, leakage and dielectric breakdown, were discussed. It was reported that the residual stresses localize around the TSV sidewalls, leading to a high potential for failures. In addition, the thin oxide liner was susceptible to other problems such as leakage and dielectric breakdown. It was pointed out that the TSV sidewall defect density may be critical to the reliability of the TSVs.

From these published studies, it can be summarized that TSV failures in single-crystalline silicon are more likely to occur in or around the thin oxide liner, which remains as the primary concern for the reliability of TSV-based interposers.

### 2.1.3 TSV Fabrication in Single-crystalline Silicon Interposers

Traditional silicon interposers are based on single-crystalline silicon wafers and TSV interconnections (Figure 13 [31]). This section discusses the typical steps in TSV fabrication, including via formation, insulation liner fabrication and metallization, and summarizes the published work on silicon interposer integration.

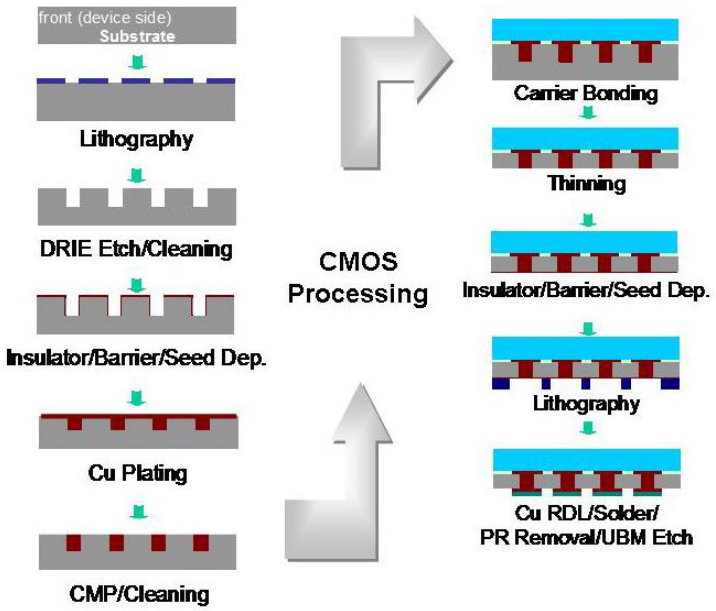



**Figure 13. Typical TSV fabrication process [31]**

The ability to form through vias is the first and most essential step to convert the raw silicon material into a functional silicon interposer. The most common method for via hole formation is deep reactive-ion etching (DRIE), also called the Bosch process. However, this process suffers from scalloped profiles in the via sidewall, especially for high aspect ratio (HAR) TSVs. Therefore, a large body of research has focused on improving via profiles and increasing the aspect ratio of the vias. Knizikevicius [32] and Abhulimen [33] have reported that the etch anisotropy was improved by configuring the process parameters such as temperature and pressure. Blauw [34] developed an advanced time-multiplexed plasma etch process by adding a third step called de-passivation. Abdolvand [35] reported a similarly-etched via profiles using mixed Ar and $O_2$ plasma in the de-passivation step, and structures with aspect ratios as high as 40:1 were successfully demonstrated. However, the challenges in forming high aspect ratio TSVs at low cost remain, and through vias in silicon substrates beyond a certain thickness are not practical.

Because silicon is a semiconductor substrate, a dielectric insulation layer is necessary to electrically isolate the silicon via wall from the signals traveling in the filled Cu. $SiO_2$ is the most widely used insulator for TSVs, and it is typically deposited by using plasma-enhanced chemical vapor deposition (PECVD) at 500-800 ℃. In addition, a barrier layer is needed between the $SiO_2$ and plated copper to prevent the Cu from diffusing into $SiO_2$. A number of studies have been conducted in the area of formation and characterization of diffusion barrier layers. Takeyama [36] compared Ti with TiN as barrier layers by using XRD and Auger electron spectroscopy, with the conclusion that TiN was better due to its stability after annealing at 850 ℃. Lee [37] deposited TaN as the barrier layer by using an ionized metal plasma process, and found that it had a better barrier effect than traditional CVD (chemical vapor deposition) deposited TaN, since the plasma made the TaN structure more close-packed and consequently more resistant to Cu diffusion into $SiO_2$. However, the results showed that diffusion induced failures happened at 900 ℃, when a new compound $Cu_5Ta_{11}O_{30}$ was formed. Len [38] used Ti/TiN and Ta/TaN multi-layer structures as the barrier, and XRD, Atomic Force Microscopy (AFM) and Current-Voltage measurements were used to test the film stability. The results showed that the multi-layer structures had better performance than the single-barrier layers because of the additional diffusion blocking effect.

As discussed in sections 2.1.1 and 2.1.2, the thin $SiO_2$ liner layers are the major cause of the electrical and reliability problems. Therefore, studies have been carried out to replace the $SiO_2$ with polymer liners for their improved insulating properties. IMEC [39, 40] used spin-on polymer dielectrics to replace the traditional CVD oxide liner for TSVs with different heights. For TSVs with 50 μm height, the polymer liner was coated

in two Bosch-etched small trenches. The silicon core between the two trenches was then opened and etched in order to expose the polymer liner. For the TSVs with 100 μm height, a more traditional spin-on method was used for a conformal coating around the via sidewall. Improved electrical and reliability performance was observed with the polymer liner in these studies.

Metallization in TSV holes is necessary for electrical interconnections, and copper is the most widely used metal due to its high electrical conductivity. The metallization process usually consists of two major steps: Cu seed formation to create a conductive layer for current, and Cu electrolytic plating to the final thickness desired. Most of the recent studies have focused on the filling of copper in high aspect ratio vias by advanced electrolytic plating processes. Dixit [41] demonstrated completely void-free electroplating in 500 μm deep silicon, by continuously varying the current during the plating process to minimize void formation. TSV interconnections with aspect ratios as high as 15:1 were reported. Wolf [42] explored different seed layers to study their effects on high aspect ratio Cu filling in TSVs, and recommended a combination of CVD and sputtering processes as an improved approach to Cu seed layer formation.

By integrating the aforementioned processes, silicon interposers with TSVs and re-distribution layers have been fabricated and studied. Sunohara [43-45] built a TSV-based silicon interposer module with 200-300 μm thick single crystalline-silicon substrates by CMP (Chemical Mechanical Polishing) with fine line multilayer wiring. Good electrical performance of TSVs was reported with the use of high resistivity silicon substrates. Improved reliability of chip-to-interposer interconnections was reported, compared to organic interposers, due to better CTE matching of silicon chips to silicon

interposers. Rao [46] demonstrated silicon interposers with similar thicknesses and process flows, but used support wafer bonding and de-bonding processes to thin down the silicon substrate. Such interposers were fabricated for large dies and the TSV interconnections were reliability tested without any failures. Other published research has focused on thinner silicon interposers. Chaware [47] and Zoschke [48] reported the demonstration of 100 µm thick silicon interposers with TSV holes of 10 to 20 µm diameters. In order to achieve such thicknesses, carrier wafer bonding and de-bonding, and CMP processes were necessary to achieve good interposer yield.

In summary, published research on TSVs in traditional wafer silicon interposers highlighted the process complexity and cost challenges. Since interposers and packages require re-distribution wiring layers on both sides of the silicon core, the high cost and complexity of single-crystalline silicon wafer interposers form the basis for motivation of this research on panel-based, double-side polycrystalline silicon interposers with through-package-vias (TPVs).

## 2.2 Prior Art on Polycrystalline Silicon

Polycrystalline silicon panels have been widely used in the photovoltaic industry as the substrate for solar cell production. This section reviews the prior art in fabrication, laser drilling and characterization of polycrystalline silicon panels, that form the basis of this novel research on low cost and high performance silicon interposers.

The fabrication process and purity control of polycrystalline silicon are two main factors that control the performance and cost of polycrystalline silicon [49-52]. The solar-grade polycrystalline silicon is fabricated from metallurgical grade silicon, obtained by silicon oxide reduction with carbon. There are two ways to produce polycrystalline

silicon; a chemical route, using the gas-based Siemens process, and a metallurgical route by purifying directly from metallurgical grade silicon. Generally, the latter experiences much lower energy consumption and thus lower cost. Direct solidification is one of the metallurgical methods to produce polycrystalline silicon, which segregates the impurities in the melt, and polycrystalline silicon panels made by this method were used in this study.

Laser drilling in polycrystalline silicon has been used for wrap-through silicon solar cells. The drilled 50 μm diameter through-vias were used to contact the front and back sides of the panel. A variety of laser technologies have been implemented and high throughputs have been reported by controlling the laser parameters [53-56].

Since polycrystalline silicon is a brittle material, the processing and handling of polycrystalline silicon panels are recognized as an engineering challenge, especially for panels with thickness of 200-300 μm. Therefore, fundamental understanding of the fracture strength of polycrystalline silicon panels is very important. Four-point bending methods and the statistical method of Weibull plots were used to characterize the fracture strength of polycrystalline silicon panels [57-60]. These studies showed that the fracture strength was directly related to the defect density in the polycrystalline silicon panels.

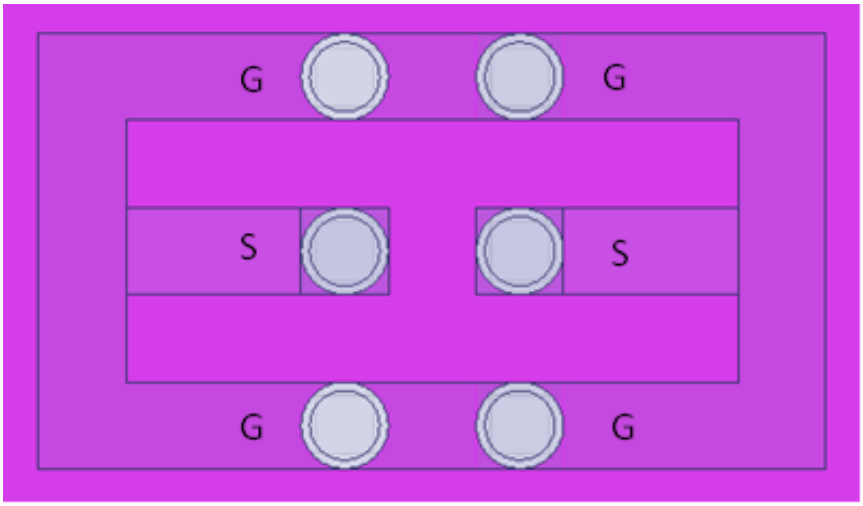
# CHAPTER 3

# MODELING AND DESIGN OF TPVS

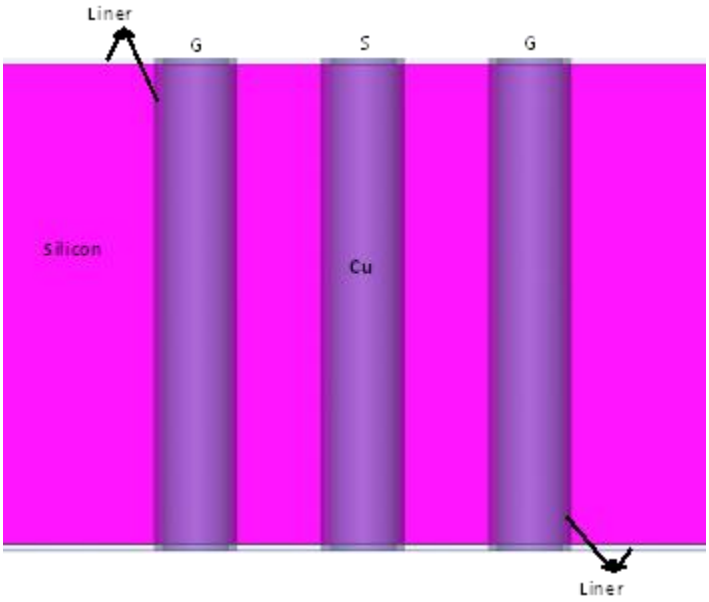
This chapter discusses electrical and mechanical modeling of TPVs in polycrystalline silicon interposers. Simulation results of TPVs are compared to TSVs in traditional single-crystalline silicon interposers. Parametric studies are also carried out. These investigations aim to provide solutions to address the electrical (lossy silicon substrate) and mechanical (CTE mismatch) challenges defined in Chapter 1. The analysis also targets to present design guidelines for TPV fabrication and test vehicle demonstration, which will be discussed in the following two chapters.

## 3.1 Electrical Modeling and Design of TPVs

One of the fundamental challenges with polycrystalline silicon is its low resistivity (high conductivity), lower than single-crystalline silicon, due to low purity level resulting from the fabrication processes. This issue is proposed to be addressed by thick and low loss insulating polymer liner on the walls of TPV. To evaluate the effect of the thick polymer liner, in this section, the electrical performance of TPVs in polycrystalline silicon was simulated and compared to TSVs in single-crystalline silicon. The 3D electromagnetic software HFSS was used to simulate the through-via structure, as shown in Figure 14. The structure consists of two signal vias (marked as “S”) and four ground vias (marked as “G”). Both insertion loss and crosstalk of the silicon via were generated from the model.




(a)




(b)

**Figure 14. (a) Top view and (b) cross-section view of the GSG model**

It has been previously reported [61] that the through-via capacitance and substrate conductance are two of the most critical factors impacting the electrical performance. Generally, lower via capacitance and lower substrate conductance are favorable for smaller insertion loss and crosstalk. The via capacitance is generally dominated by insulator capacitance and can be written as:

$$C_{insulator} = \varepsilon_{liner} \times \frac{2\pi h_{TV}}{\ln(\frac{r_{TV} + t_{liner}}{r_{TV}})} \quad (1)$$

where $C_{insulator}$ is the capacitance of the insulation liner, $\varepsilon_{liner}$ is the dielectric constant of the insulation liner, $h_{TV}$ is the height of the via, $r_{TV}$ is the radius of the via, and $t_{liner}$ is the thickness of the insulation liner. It can be seen from the equation that the electrical properties and thickness of the liner impact the via capacitance and thus the electrical performance. On the other hand, the conductance of the silicon substrate is governed by following equation:

$$G_{Si\_sub} = \frac{\pi \times \sigma_{Si} \times h_{TV}}{\cosh^{-1}(\frac{p_{TV}}{d_{TV}})} \quad (2)$$

where $G_{Si\_sub}$ is the conductance of the silicon substrate, $\sigma_{Si}$ is the conductivity of the silicon, $h_{TV}$ is the height of the via, $p_{TV}$ is the pitch of the via and $d_{TV}$ is the diameter of the via. The physical origin of substrate conductance is the conductivity of silicon material, which can greatly affect the electrical performance.

Therefore, in this section, through-vias with silicon substrates of different conductivity (resistivity) and with different types of liners are simulated. Parametric study has also been carried out for the thickness of in-via liner.

### 3.1.1 Electrical Performance Comparison between TPV and TSV

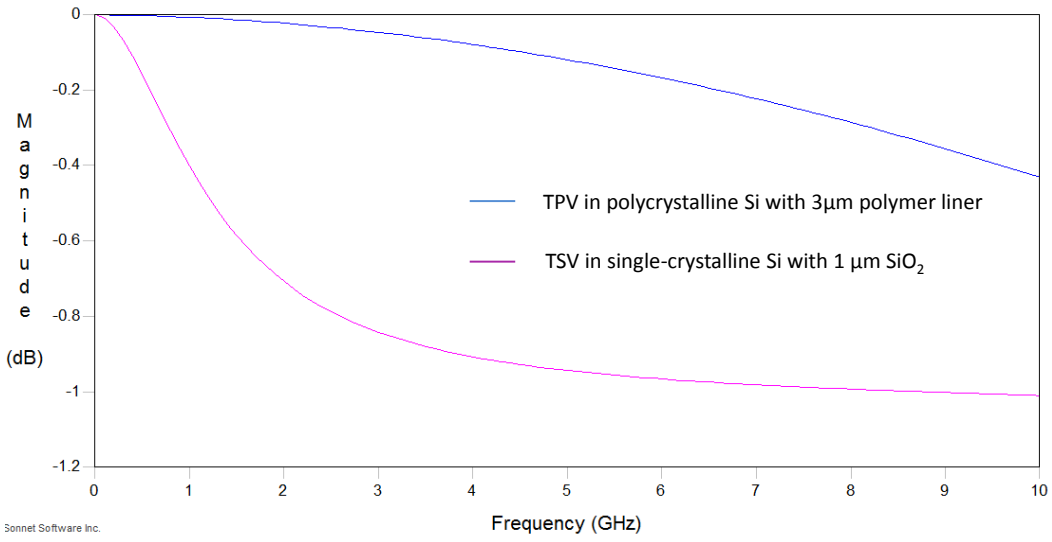
A typical 10 Ω-cm silicon material with $SiO_2$ liner was used as an example for TSV in single-crystalline silicon interposer while a much lower, 0.5 Ω-cm silicon, with thick and low electrical loss polymer liner (tanδ=0.002) was used for TPV in polycrystalline silicon interposer. The key parameters used in the simulation are listed in Table 3.

**Table 3. Key parameters for electrical modeling**

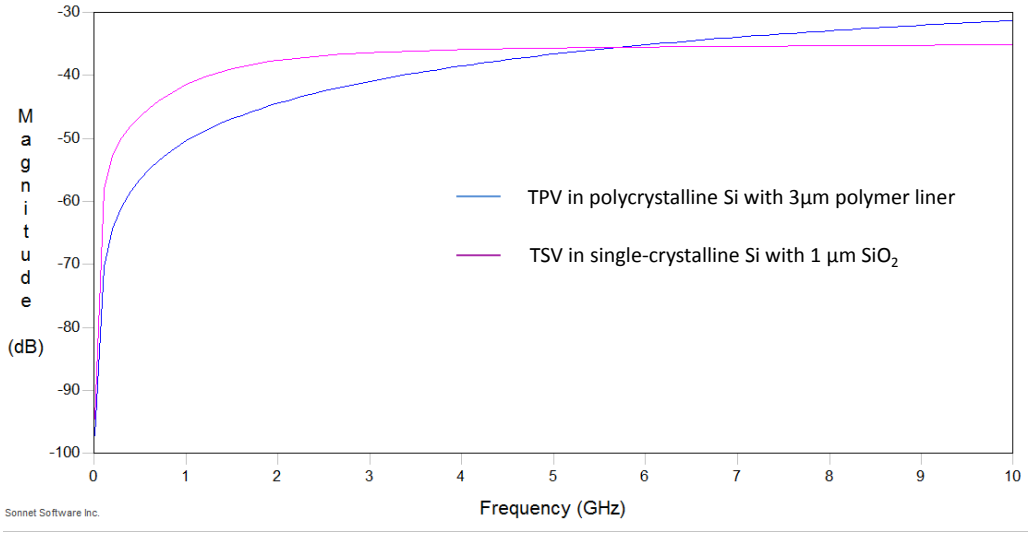
| Parameters | TSV in traditional silicon interposer | TPV in polycrystalline silicon interposer |
|---|---|---|
| Substrate thickness(μm) | 200 μm | 200 μm |
| Via diameter size(μm) | 30 μm | 30 μm |
| In-via liner thickness(μm) | 1 μm $SiO_2$ | 3 μm polymer |
| Surface liner thickness(μm) | 1 μm $SiO_2$ | 3 μm polymer |
| Substrate Resistivity | 10 Ω-cm | 0.5 Ω-cm |
| Liner dielectric constant | 4 | 3.1 |

Figure 15 compares the insertion loss and FEXT (far end crosstalk) between TPV and TSV. It can be observed that TPV in polycrystalline silicon interposer shows lower insertion loss up to 10 GHz and crosstalk up to 6 GHz. The superior electrical performance of TPV is attributed to the thick insulating polymer liner. This helps reduce the electrical loss and coupling in the silicon substrate.

However, it can also be observed that, as the frequency increases, the crosstalk tends to increase a lot for TPV and is worse than TSV at higher frequency, as shown in Figure 15(b). This is because the coupling of TPV increases with frequency, primarily decided by substrate conductance at high frequency. Hence, the lower crosstalk of TPV, due to thick polymer, starts to be offset because of high conductivity of the polycrystalline silicon substrate. TPVs designed with even thicker polymer liners help to maintain a better crosstalk for TPV over TSV at higher frequency, as shown in Figure 16 with 5 µm liner.




(a)




(b)

**Figure 15. (a) Insertion loss and (b) FEXT plots for TPV in polycrystalline silicon interposer (3 µm liner) and TSV in single-crystalline silicon interposer**

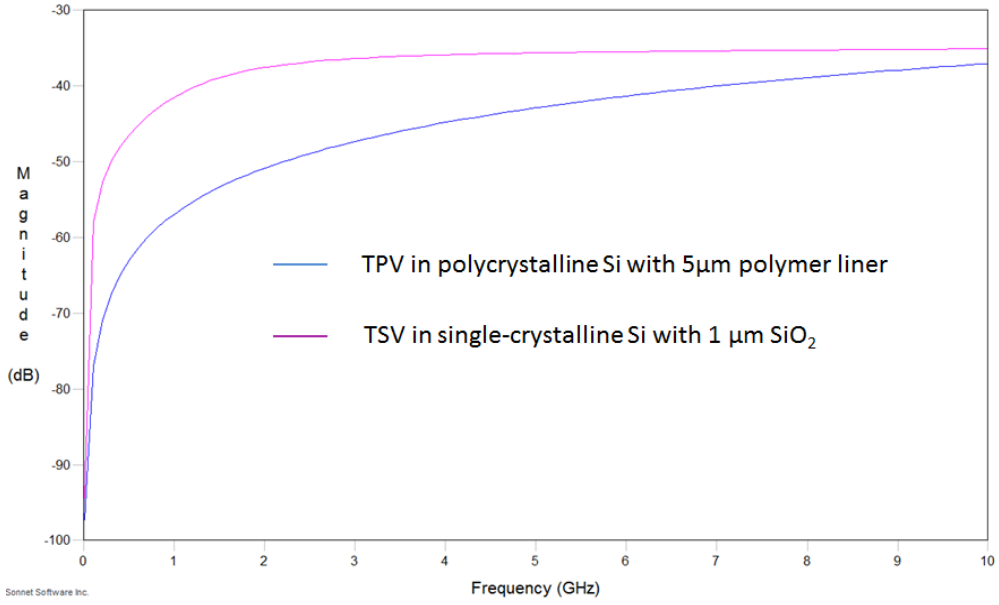
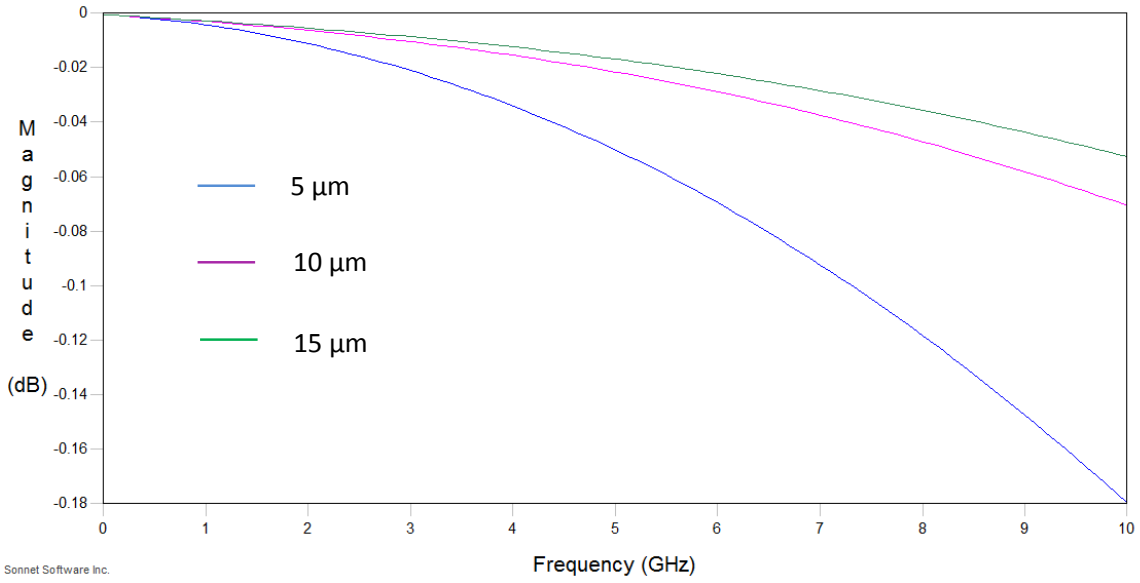


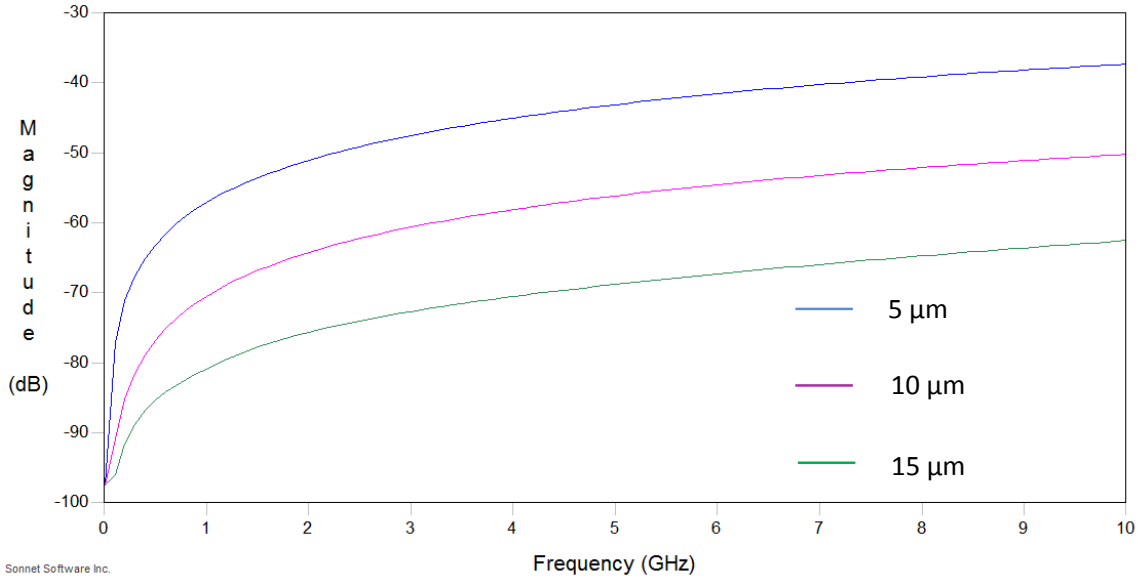

**Figure 16. FEXT plots for TPV in polycrystalline silicon interposer (5 µm liner) and TSV in single-crystalline silicon interposer**

### 3.1.2 Effect of Sidewall Liner Thickness

The parametric study of in-via liner thickness is necessary since it can provide important design guidelines for TPV. The effect of the sidewall liner thickness (5 µm, 10 µm and 15 µm) on the insertion loss and crosstalk in TPVs is studied in Figure 17. The TPV diameter and pitch were 30 µm (diameter of the Cu filled region) and 120 µm respectively. The silicon substrate resistivity and thickness were 0.5 Ω-cm and 200 µm respectively. It is seen from Figure 17 that the insertion loss and crosstalk can be reduced by using a thicker in-via liner. This is because, as the thickness increases, the capacitance of TSV decreases, resulting in lower insertion loss and crosstalk.




(a)




(b)

**Figure 17. (a) Insertion loss and (b) FEXT plots for TPV with different in-via liner thickness**

### 3.1.3 Design Guidelines for Electrical Consideration

It has been shown by electrical simulations that the thick polymer liner is effective in addressing the fundamental challenge of low resistivity for the polycrystalline silicon material. As the results show, a polymer liner as thin as 3 µm is able to maintain better insertion loss up to 10 GHz and crosstalk up to 6 GHz for TPV than TSV with 1 µm $SiO_2$. However as the frequency increases such positive effect on crosstalk is compromised by the low resistivity of the silicon substrate. Therefore, to address this problem, a liner thicker than 5 µm is recommended.

## 3.2 Mechanical Modeling and Design of TPVs

Another fundamental challenge with TPV in polycrystalline silicon is the difference in CTE between silicon and Cu. Such CTE mismatch, in combination with

temperature change, will lead to stress localization and finally reliability problems. The polymer liner, introduced to provide insulation for electrical purpose, can also improve TPV reliability due to its low modulus. The thick polymer liner tends to play the role as "cushion" during thermal attack to buffer the stresses in the TPV system. In this part, Finite Element (FE) modeling was performed using Ansys to simulate proposed TPV structure with polymer liner in comparison to TSV with thin $SiO_2$ liner. Both interfacial shear stresses and first principal stresses in silicon due to thermal loading were generated and analyzed. As is the case with electrical modeling, parametric studies were also performed with in-via liner thickness.

### 3.2.1 Stress Comparison between TPV and TSV

A two-dimensional axisymmetric model was built in Ansys to simulate the stress in TPV and TSV. The schematic cross-section (1/4 via) is presented in Figure 18 with geometry values. The Cu via size was 30 μm with a height of 200 μm. The diameter of the pad was 50 μm and the thickness was 10 μm. The liner thickness varied for different cases.

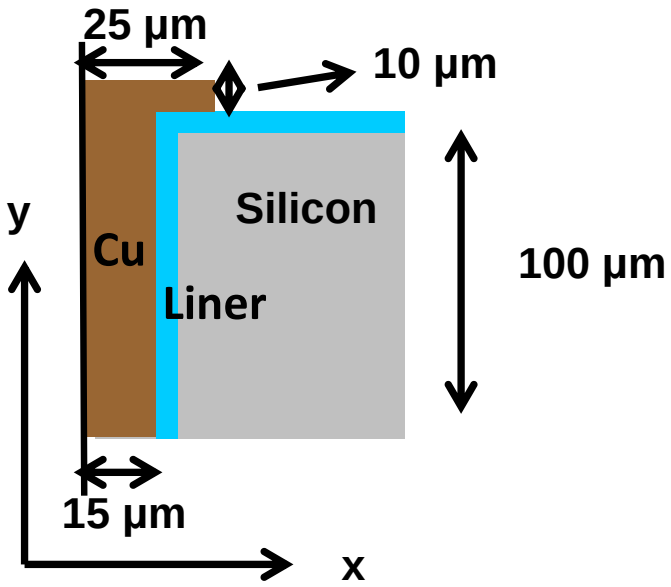



**Figure 18. Schematic cross-section drawing of TPV for mechanical modeling**

Figure 19 compares the schematic cross-section and meshed models for TPV and TSV. In this study, TPV was simulated with 3 µm thick polymer liner on top and bottom surfaces and 3 µm thick via sidewall liner compared with 1 µm thick $SiO_2$ liner on top and bottom surfaces of silicon and 1 µm thick via sidewall liner for TSV. The effect of the very thin diffusion barrier was neglected in TSV modeling.

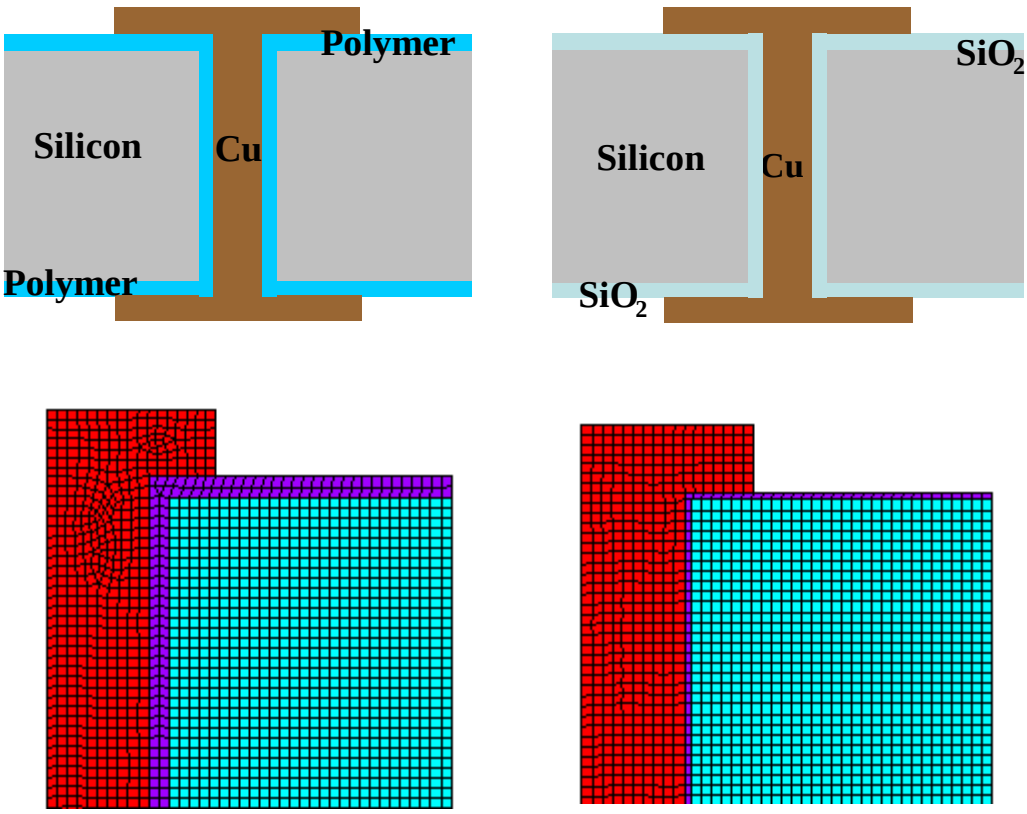



**Figure 19. Schematic cross-section drawings and meshed models for (a) TPV and (b) TSV**

The material properties used in the simulations are given in Table 4 and Table 5. The polymer presents much lower modulus than $SiO_2$. The non-linear model of Cu was used based on our previous studies. A standard thermal load cycle of -55℃ to 125℃ (Figure 20) was used in the analysis with dwelling time of 15 minutes at both extreme temperatures.

**Table 4 Material properties used in mechanical modeling**

| | Young's Modulus (GPa) | Poisson's Ratio | CTE (ppm/℃) | Stress free Temperature (℃) |
|---|---|---|---|---|
| Single-crystalline Silicon[62] | 169 | 0.28 | 2.6 | 25 |
| Poly-Silicon[62] | 161 | 0.26 | 2.4 | 25 |
| $SiO_2$[24] | 71.4 | 0.16 | 0.5 | 250 |
| Polymer[63] | 6.9 | 0.3 | 31 | 180 |
| Copper[24] | Table 5[24] | 0.3 | 17.3 | 25 |

**Table 5 Cu properties used in mechanical modeling**

| *Temperature (℃)* | *27* | *38* | *95* | *149* | *204* | *260* |
|---|---|---|---|---|---|---|
| Young's Modulus (GPa) | 121.00 | 120.48 | 117.88 | 115.24 | 112.64 | 110.00 |
| *Temperature (℃)* | *27* | | | | | |
| Plastic Curve -stress (MPa) vs. strain | 121@ 0.001ε<br>186@ 0.004 ε<br>217@ 0.01 ε<br>234@ 0.02 ε<br>248@ 0.04 ε | | | | | |

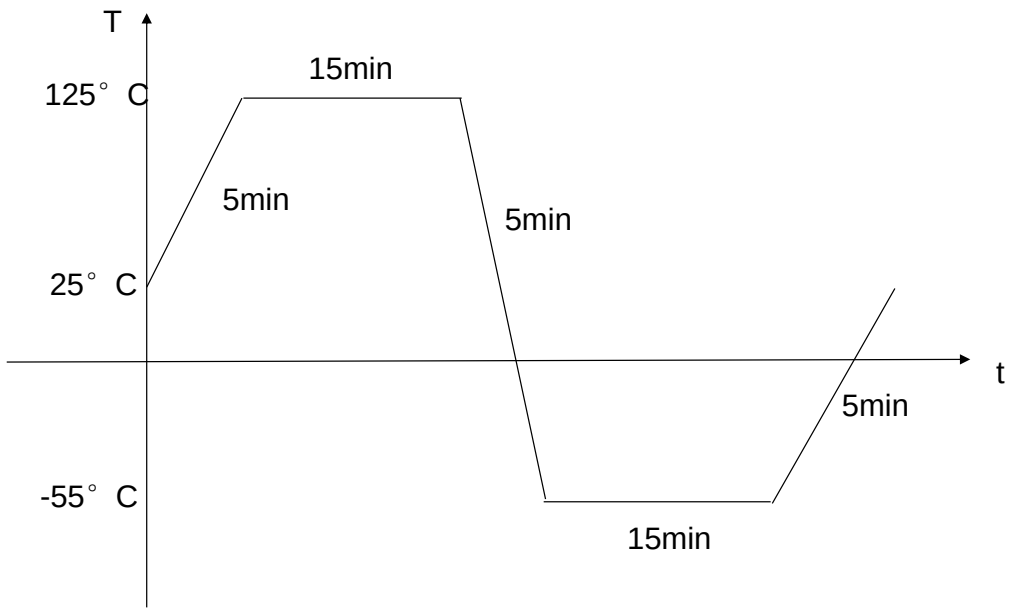
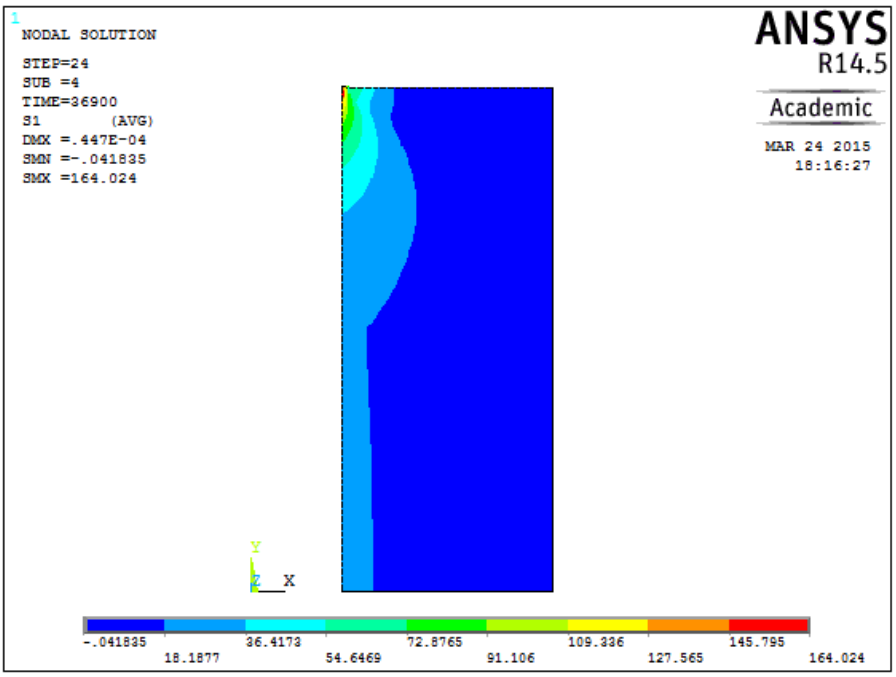
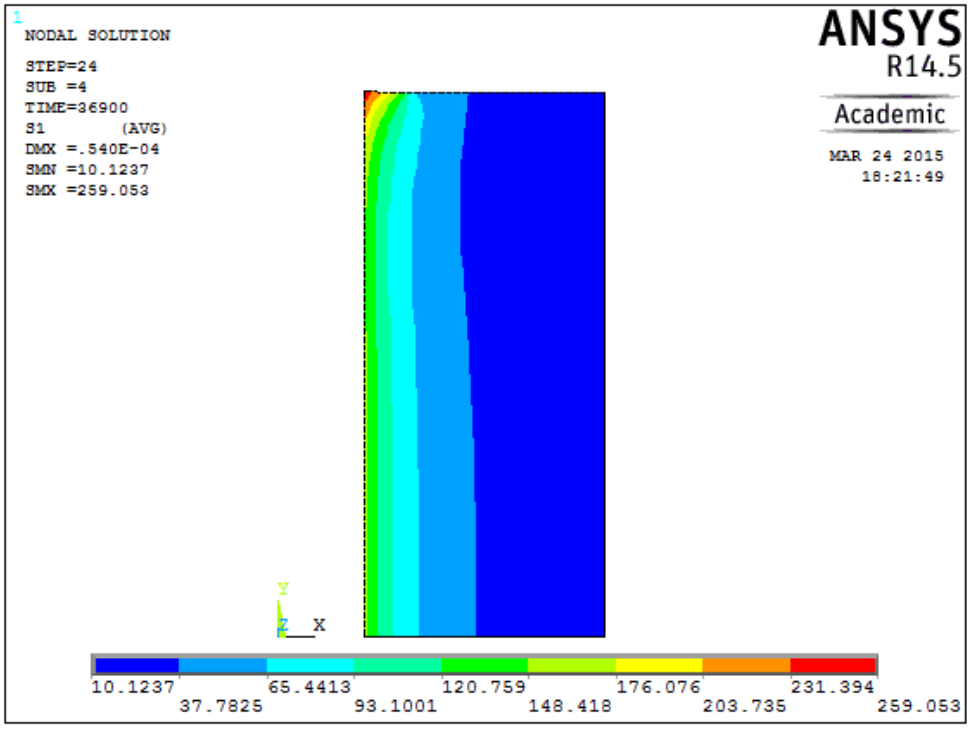



**Figure 20. Thermal loading curve for mechanical modeling**

Figure 21 compares the first principal stress in TPV and TSV at 125℃. It can be observed that the first principal stress in silicon is significantly reduced in TPV (164 MPa) compared to TSV (259 MPa). This is due to the low modulus and "cushion" effect of the polymer material. The much smaller stress in TPV can mitigate the possibility of failures.




(a)

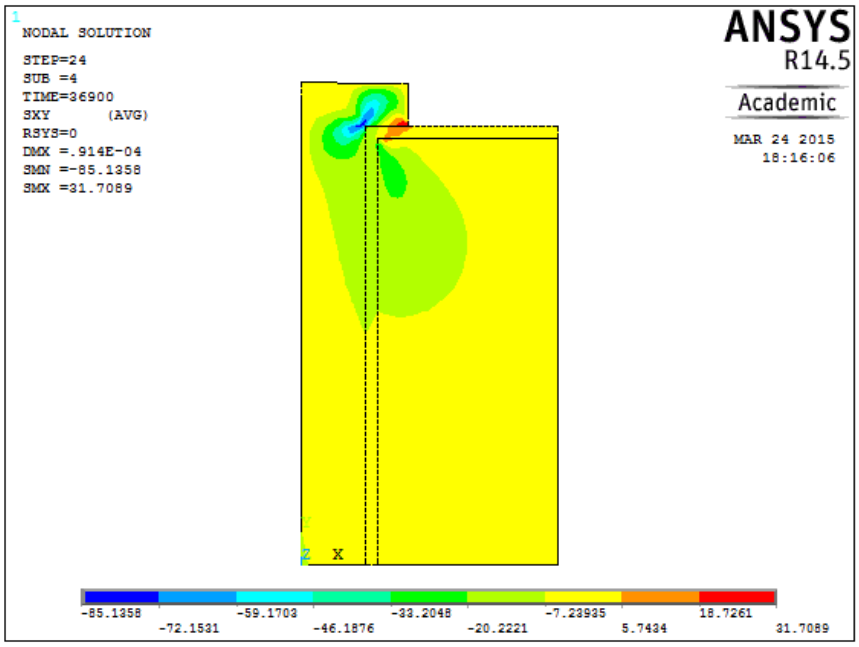



(b)

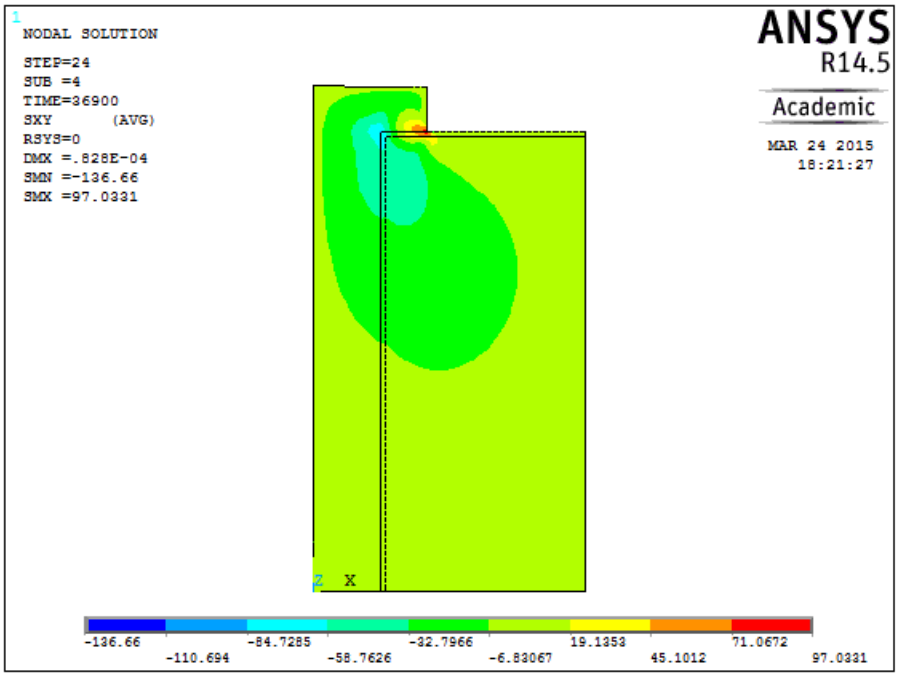
**Figure 21. First principal stress in silicon for (a) TPV and (b) TSV at 125℃**

Similarly, Figure 22 illustrates the shear stress in TPV and TSV at 125℃. It can be concluded that shear stress localization occurs at the interfaces of different materials, such as Cu/liner and silicon/liner joints. As expected, TSV shows larger (137 MPa) shear stress than TPV (85 MPa). The relatively higher interfacial shear stress localization in TSV structures can be attributed to the higher CTE mismatch of $SiO_2$ with Cu vias. This makes it more susceptible to interfacial failures compared to TPV structures.

Based on the discussions above, thick polymer liners in TPV act as buffer layers and can reduce the risk of failures. On the other hand, TSV shows higher stress in spite of the thinner layer of $SiO_2$. Furthermore, due to higher stiffness of $SiO_2$, the TSV structures are more prone to cohesive cracks in liners compared to TPV structures. It is also expected that TSV structures would experience additional stresses during the back-grinding processes required for fabricating these structures.




(a)

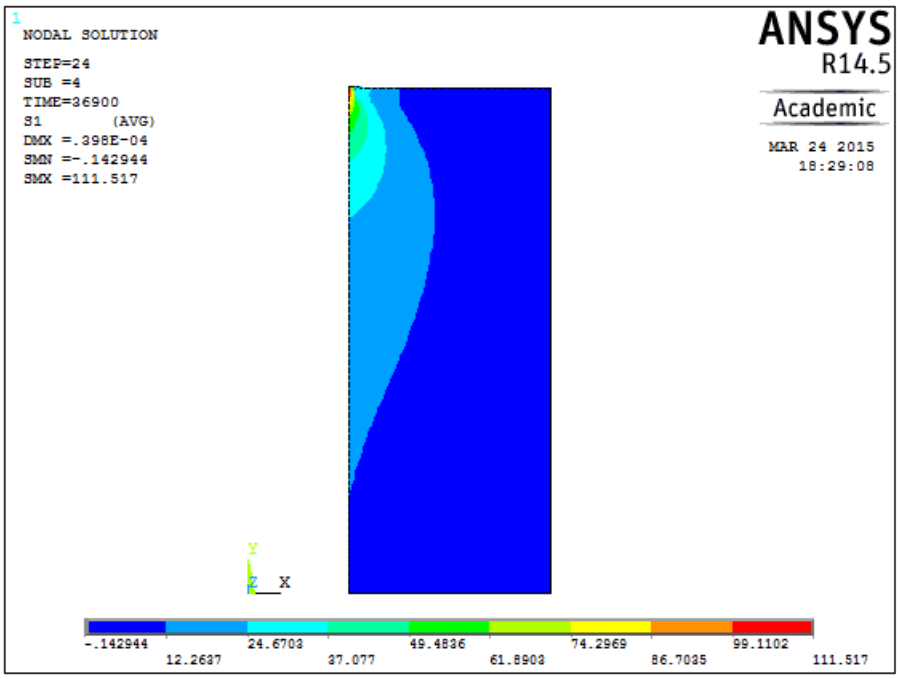



(b)

**Figure 22. Shear stress in (a) TPV and (b) TSV at 125℃**

### 3.2.2 Effect of Sidewall Liner Thickness

It has been shown that thicker sidewall liners help to improve the electrical performance of TPVs. This section investigates the effect of the in-via liner thickness on the first principal stress and shear stress in TPVs. Three different cases, with 5 μm, 10 μm and 15 μm in-via liners were studied and compared. The substrate thickness was 200 μm and the diameter of the via (Cu filled) was 30 μm. The surface liner was 15 μm thick. As the contour plots presented in Figure 23, when the liner becomes thicker (5 μm, 10 μm and 15 μm) the first principal stress at 125℃ gradually decreases (111 MPa, 52 MPa and 21 MPa). Hence, at elevated temperature, larger polymer liner thicknesses absorb the stresses more effectively and lead to less first principal stresses in silicon and thus less risk of cohesive cracking in the substrate. It can also be summarized from Figure 24 that the shear stresses for TPV are 82 MPa, 80 MPa and 79 MPa for TPVs with 5 μm, 10 μm and 15 μm liners, respectively. As expected, the shear stresses localize at material interfaces and larger liner thicknesses help also to reduce the shear stresses, thus leading to a smaller possibility of interfacial failures.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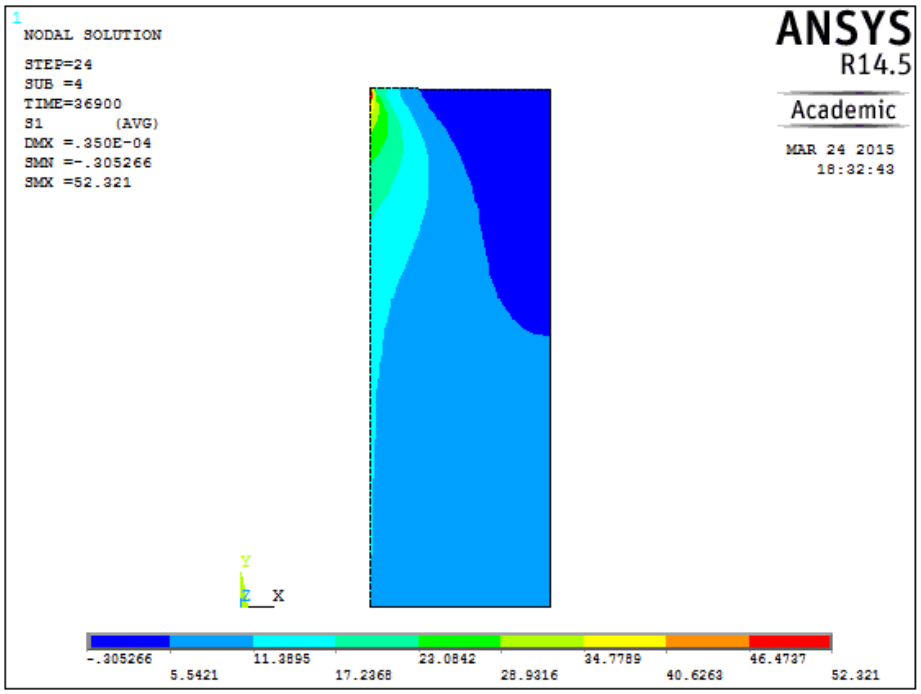
(a)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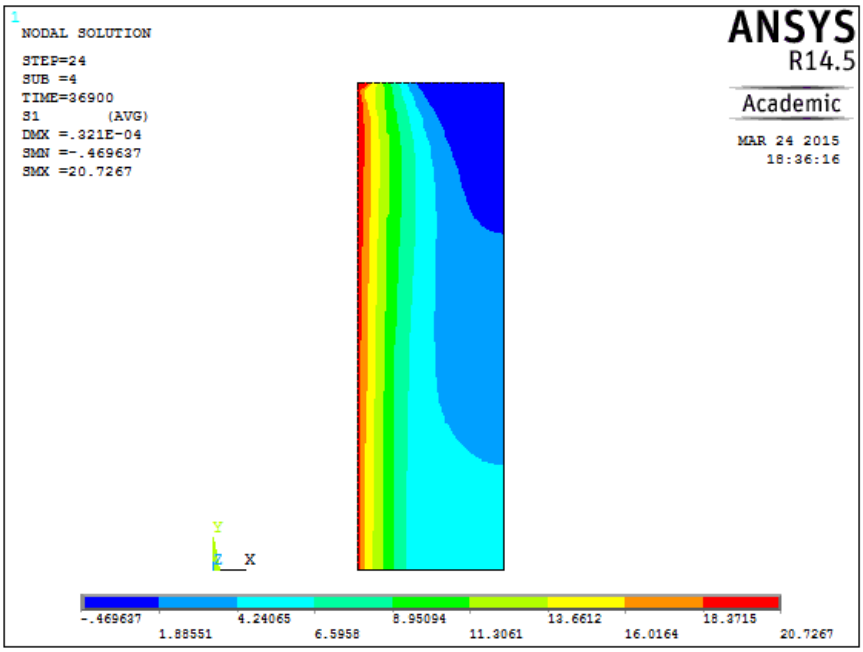
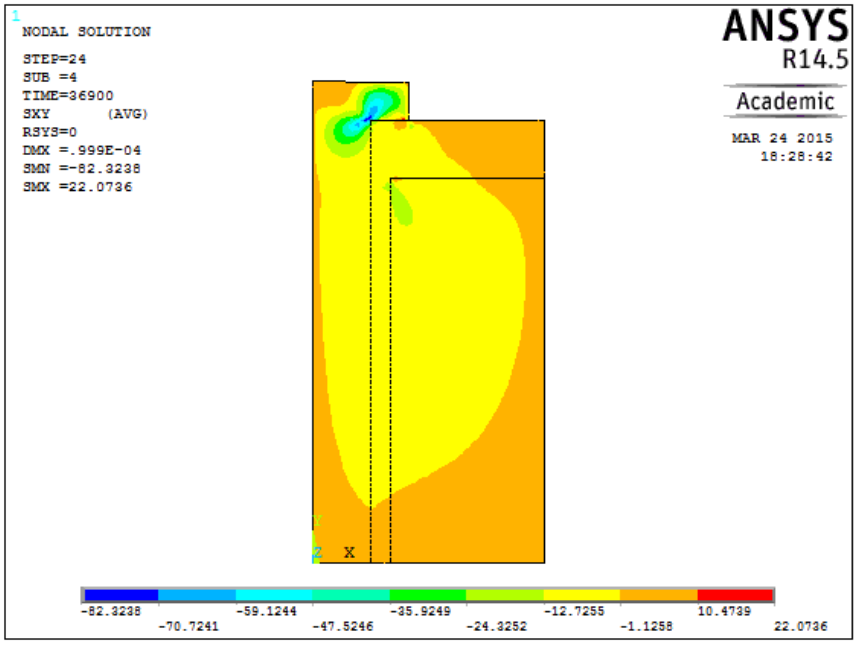
(b)

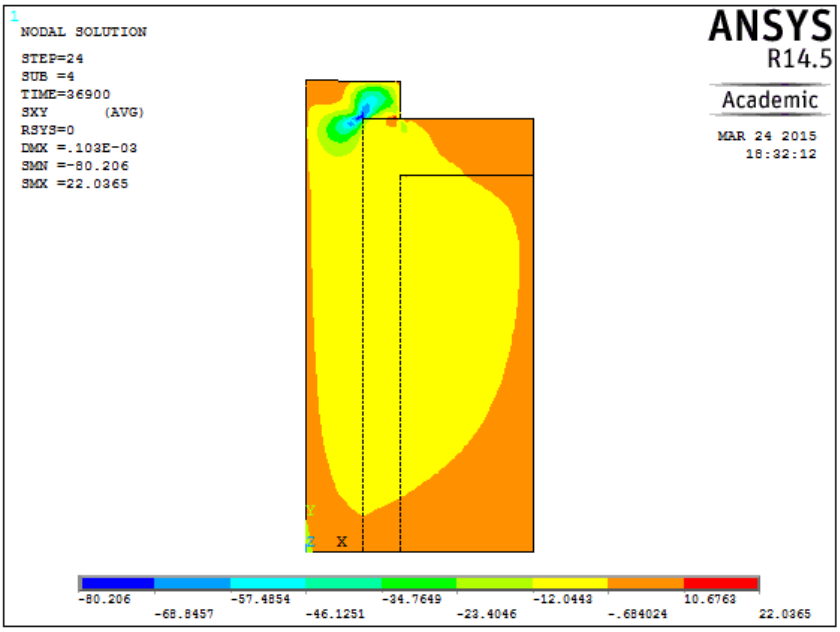



(c)

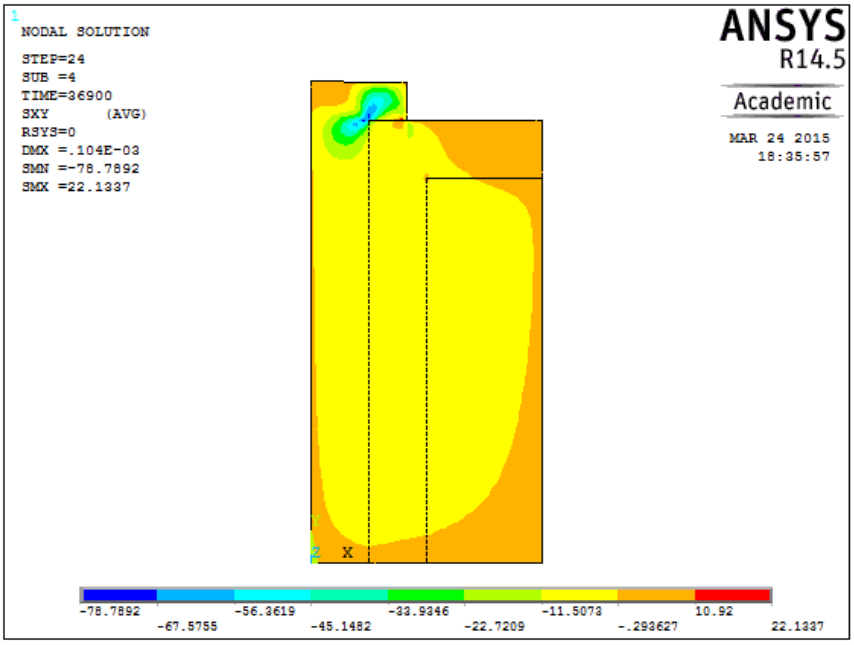
**Figure 23. First principal stress in Si for TPV with sidewall liner thickness of (a) 5 μm, (b) 10 μm and (c) 15 μm at 125℃**




(a)




(b)




(c)

**Figure 24. Shear stress in TPV with sidewall liner thickness of (a) 5 μm, (b) 10 μm and (c) 15 μm at 125℃**

### 3.2.3 Design Guidelines for Mechanical Consideration

The first principal stress in Si and shear stress in TPVs at 125℃ for different liner types and thicknesses are summarized in Table 6. It can be observed that the introduction of thick polymer liners can greatly lower the stress by acting as "cushion" layer due to the low modulus. This enables improved mechanical stability of TPVs than TSVs. These investigations also suggest that thicker sidewall liners can help to mitigate the possibility of failures. Generally, TPVs with a sidewall liner more than 10 μm should be able to experience good reliability under thermal attack.

**Table 6 Summary of stresses for different liner types and sidewall liner thicknesses**

| Sidewall Liner | First principal stress in Si (MPa, 125℃) | Shear stress (MPa, 125℃) |
|---|---|---|
| 1 μm $SiO_2$<br>(1 μm $SiO_2$ surface liner) | 259 | 137 |
| 3 μm polymer<br>(3 μm polymer surface liner) | 164 | 85 |
| 5 μm polymer<br>(15 μm polymer surface liner) | 111 | 82 |
| 10 μm polymer<br>(15 μm polymer surface liner) | 52 | 80 |
| 15 μm polymer<br>(15 μm polymer surface liner) | 21 | 79 |

### 3.3 Summary and Overall Design Guidelines for TPV

**a. Electrical Modeling**

- A 3D EM HFSS model has been used to simulate the insertion loss and crosstalk of TPVs.
- TPVs present better insertion loss than TSVs with thin $SiO_2$ due to the low loss and high thickness of polymer liners. At high frequency, the crosstalk of TPVs is primarily determined by the conductivity of silicon substrate. Thicker polymer liners (5 μm and above) are required to maintain low crosstalk with TPVs at higher frequency.
- Parametric studies indicate that thicker sidewall liners result in better electrical performance.

**b. Mechanical Modeling**

- A 2D axisymmetric model was established in Ansys to simulate the first principal stresses in silicon and shear stresses in TPV under thermal cycling.
- TPVs with thick polymer liners present both smaller principal stresses and shear stresses than TSVs at 125℃ due to the low modulus of polymer. This helps to mitigate the risks of substrate cohesive crack as well as interfacial failures.
- Parametric studies suggest that sidewall liners act as stress buffers and thicker liners result in better mechanical performance.

**c. Design Guidelines**

- For electrical considerations, sidewall liners with 5-15 μm thickness are required to maintain low insertion loss and crosstalk at high frequency.
- For mechanical considerations, in-via liners of 10-15 μm help to significantly lower the stresses in TPV.
- In summary, sidewall liners with 10-15 μm are necessary to achieve both better electrical performance and mechanical reliability. Thicker in-via (15 μm) liners are more favorable.

- Design guideline provided are considered and reflected in the TPV fabrication and test vehicle demonstrations as discussed in Chapter 4 and 5, respectively.

# CHAPTER 4

# FORMATION, LINER FABRICATION AND METALLIZATION OF TPVS IN POLYCRYSTALLINE SILICON

This chapter discusses the fundamental research on TPV formation, thick polymer liner fabrication and copper metallization in 200 μm thin polycrystalline silicon panels. The biggest fundamental challenge for polycrystalline silicon panels is the brittleness of the material, and the engineering challenges include the handling of thin silicon panels, TPV hole formation without defects, thick insulating liner formation consistent with the design guidelines presented in Chapter 3. The first part of this chapter discusses the fundamental studies on the fracture strength of the polycrystalline panels. Based on this quantitative analysis, solutions are proposed to improve the handling of thin silicon panels while resisting bending forces during the fabrication processes. The second part of this chapter presents laser-silicon interaction mechanisms, materials and processes to form TPVs in polycrystalline panels, various processes to form thick polymer insulation liners on the surfaces and via walls, and finally copper plating of TPVs, considering the design guidelines summarized in Chapter 3.

The process flow used to achieve metalized, polymer-lined TPVs in polycrystalline silicon interposers is shown in Figure 25. There are three major steps: (1) TPV hole formation, (2) TPV liner formation, and (3) TPV metallization. This unique approach involving double-side processes, wherein TPV holes are formed through the entire thickness of the silicon substrate, and both surfaces of the silicon panel are processed simultaneously, leading to a significant reduction in the number of unit

processes as well as the process complexity of published [31] TSV processes in single-crystalline silicon wafers. The unit processes that contribute to this potential cost reduction include:

a) Laser ablation for via formation in lieu of DRIE and Bosch etching,

b) Thick polymer liner fabrication, eliminating the need for vacuum deposited oxide liners and barrier metal layers,

c) Electroless plated copper seed layers as opposed to PVD (physical vapor deposition) or CVD deposition, and

d) Cu electrolytic through-via filling without any CMP process.

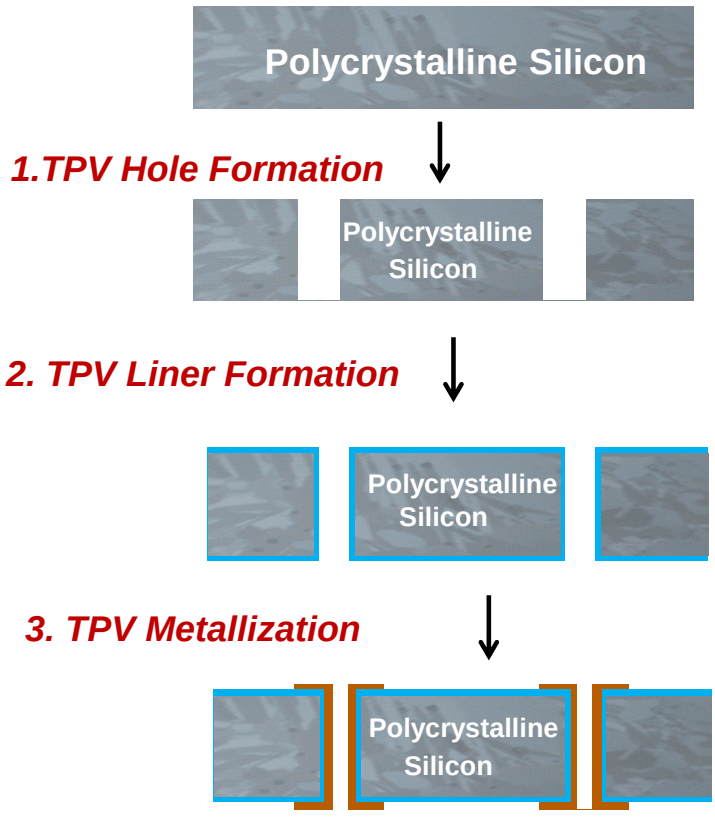



**Figure 25. TPV fabrication process flow**

### 4.1 Fracture Strength of Thin Polycrystalline Silicon Panels

Polycrystalline silicon is a brittle material, and therefore, one of the fundamental challenges is the high fracture rate caused by handling during the TPV and liner formation and metallization process steps. These challenges get exacerbated when moving to thinner panels and larger panel sizes, which are essential to meet the research targets.

The fracture of thin silicon panels at any given process step is not only a function of the residual stress generated in the previous process steps, but also the stress applied due to panel handling, transport and processing at that step. Assuming the rule of linear elastic superposition stands, the stress that leads to substrate breakage can be written as [58]:

$$\sigma_{total} = \sigma_{applied} + \sigma_{residual} \quad (3)$$

where $\sigma_{total}$ is the total stress on the panel, $\sigma_{applied}$ is the external force applied and $\sigma_{residual}$ is the residual stress in the panel.

The residual stress can be evaluated by digital transmission photoelasticity method [64, 65] and is usually much smaller compared to the external stress induced during process handling. So, in this study, the focus was on the panel strength to withstand the external stresses from handling. Hence, the fracture strength of the 200 μm thick polycrystalline silicon panel was studied by four-point bend testing as shown in Figure 26. The applied stress was extracted from the force data recorded by the reader (the green tool on the left bottom of Figure 26).

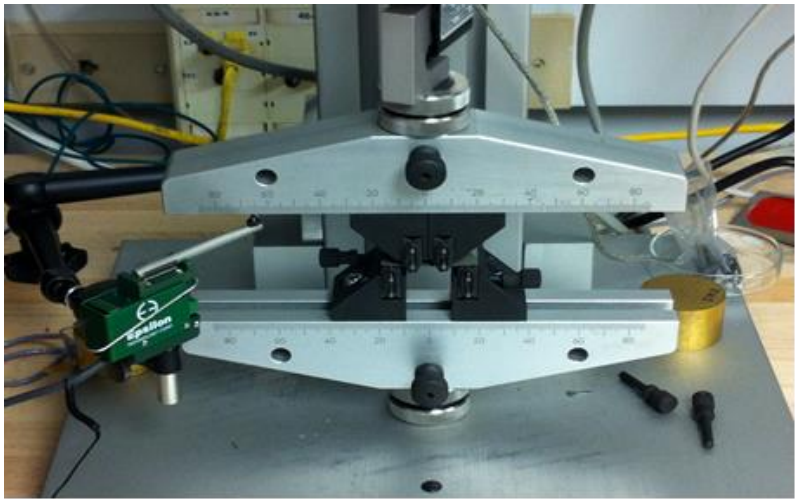


**Figure 26. Four-point bend testing tool to evaluate fracture strength**

The fracture strength of a brittle material is controlled by the existence of critical defects, which act as the origins of the final failure. Unlike single-crystalline silicon, defects are distributed randomly in the polycrystalline silicon panels, due to different crystal orientations and grain boundaries. Different grain orientations can be clearly observed in the top view detail of an as wire-cut polycrystalline silicon panel made by directional solidification shown in Figure 27. An additional challenge for upgraded metallurgical grade poly-silicon panels is the wide distribution of grain sizes across the panel. For example, the part shown in Figure 28 (a) with larger grain sizes is expected to have different fracture strength from the one shown in Figure 28 (b) with multiple small grains. Therefore it is inaccurate to evaluate the fracture of the sample by carrying out the experiment on an entire large panel.

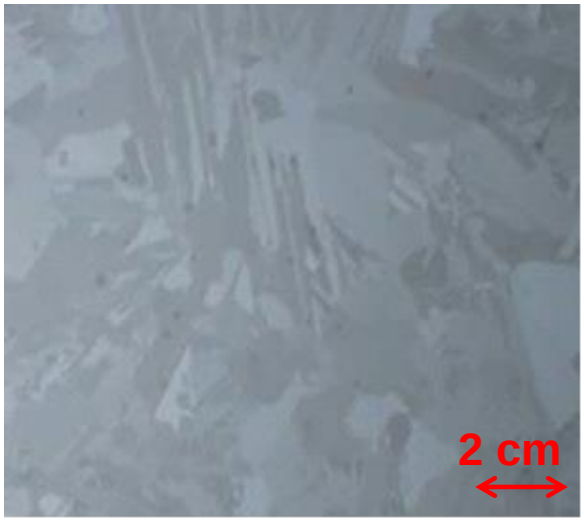



**Figure 27. Top view of an as-cut polycrystalline silicon panel**


**(a)**


**(b)**

**Figure 28. Top view of polycrystalline silicon panel with (a) large grain and (b) multiple small grains**

In order to accurately assess the fracture strength of polycrystalline silicon with a broad range of grain sizes, the test was designed and carried out as follows:

1) 150 mm by 150 mm full size panels were diced into 24 rectangular pieces, each having a length of 37.5 mm and a width of 25 mm, as illustrated in Figure 29.

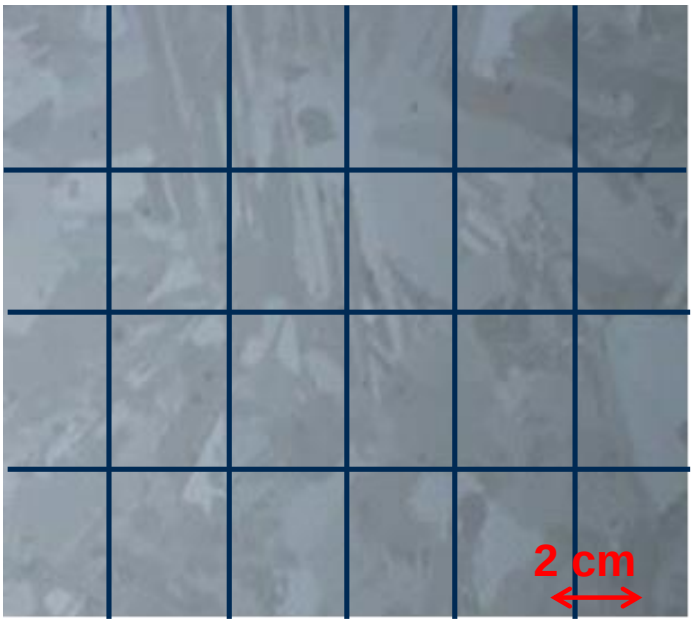



**Figure 29. Schematic drawing of the sample diced into small pieces**

2) Four-point bend tests were carried out on each small specimen, consisting of different textures and grain sizes. Force data was collected for each test and the strength values were calculated. The testing fixture with the sample mounted is shown in Figure 30. The stress was calculated from the following equation [65]:

$$\sigma = \frac{3P(L - L_i)}{2bd^2} \tag{4}$$

where $\sigma$ = the stress due to applied load, $P$ = applied load, $L$ =outer span, $L_i$ =inner span, $b$ = sample width and $d$ =sample thickness.

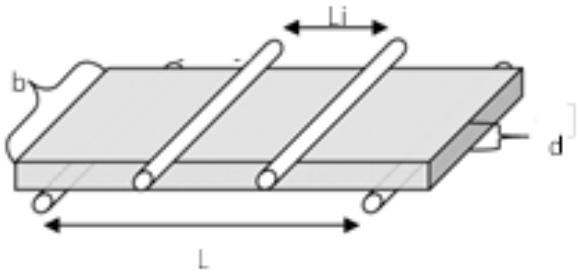



**Figure 30. Schematic drawing of Fixture setup for four-point bending test (modified from [59])**

It has to be noted that, due to the fixture setup, the supporting and loading rollers rotated outward and inward respectively during the test. This creates friction, which in turn leads to tensile stresses near the center of the specimen. According to previously reported results [59], the ratio of this friction-induced stress to the bending stress can be written as:

$$\frac{\sigma_f}{\sigma_b} = \frac{4df}{3L} \tag{5}$$

Where $\sigma_f$ = friction-induced stress, $\sigma_b$ = bending stress, $d$ = specimen thickness, $f$ = friction coefficient between roller and specimen and $L$ = outer span.

Given the sample thickness of 200 μm and an outer span of 30 mm, as well as a very small $\frac{d}{L}$ value that equals to 0.0067, the resulting stress ratio can be treated as very low and the friction stress does not significantly affect the results.

3) Analysis of the data: Consistent with the hypothesis about the randomness of the defects, strength data with a large amount of scatter was acquired due to the different

defect locations, grain sizes and orientations. Therefore, statistical treatment of the strength data was necessary, and Weibull plots were used. Weibull theory of brittle fracture is based on the fact that failure of the whole body depends on a combination of survival probabilities of the individual volume elements. For the given test, the Weibull equation can be written as [65]:

$$P_f = 1 - \exp[-\left(\frac{\sigma}{\sigma_\theta}\right)^m] \tag{6}$$

where $P_f$ =probability of failure due to applied stress $\sigma$, $\sigma_\theta$ = characteristic strength when 62.5% of the sample fails and $m$ =Weibull modulus.

In general, the Weibull plots can be obtained by assigning $P_f$ to each strength point. The two important factors, $\sigma_\theta$ (usually used as a reference for the fracture strength of the sample) and $m$ (Weibull modulus describing the variation of the data) are achieved by plotting $\ln(1/\ln(1-P_f))$ versus $\ln(\sigma)$ followed by a linear regression analysis.

The Weibull plots of the strength data from the aforementioned tests are presented in Figure 31. By linear regression, a characteristic fracture strength of the silicon panel of around 143 MPa was extracted. This value is similar as the ones shown in previous publications [57-59, 65].

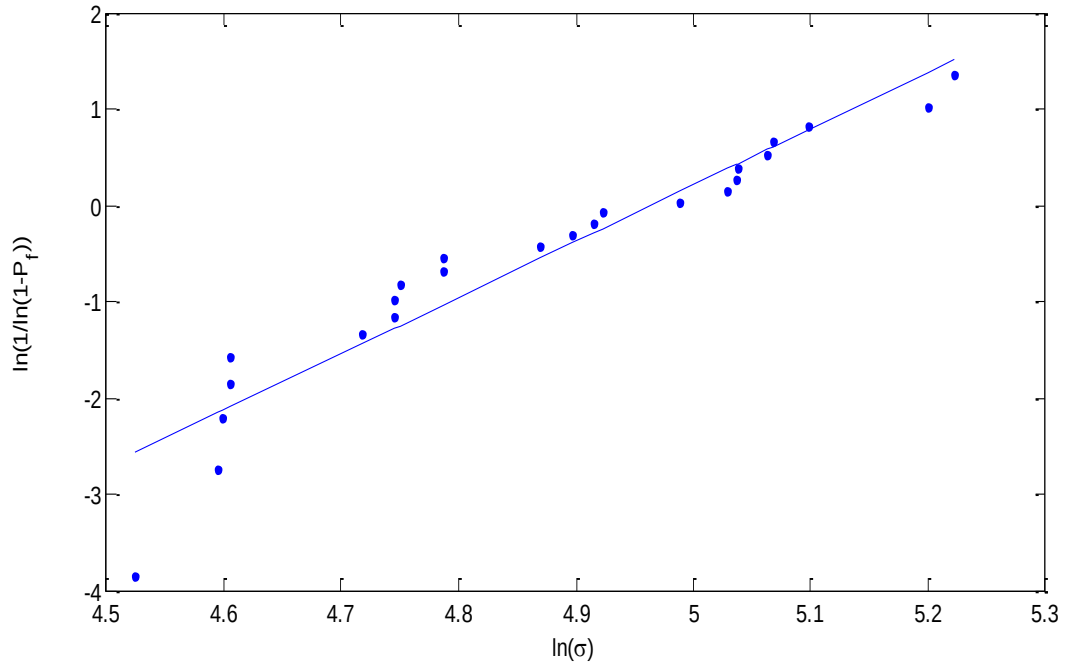



**Figure 31. Weibull plot for fracture strength of polycrystalline silicon panel**

In order to overcome the challenges of panel breakage, surface polymer liners on both sides of the panel were introduced. The surface liner not only improves the strength and enables handling of the thin silicon panels, but also functions as an electrical insulator to isolate signals from leaking into the lossy silicon. The surface liner was deposited by vacuum lamination of thin dry film polymer dielectrics in the second step of the TPV fabrication process, as shown in Figure 25. Figure 32 shows a top view of the polymer-laminated polycrystalline silicon panel.

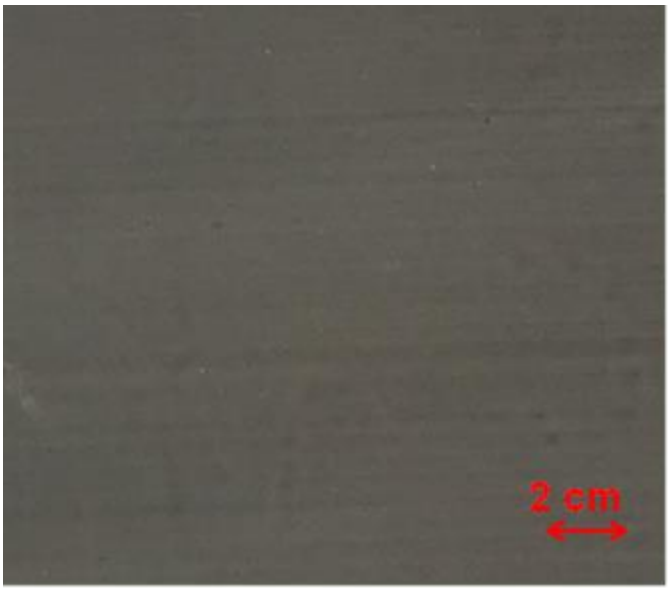



**Figure 32. Top view of polymer-laminated polycrystalline silicon panel**

To quantify the fracture strength of the stack consisting of the silicon panel with liner, two polymer-laminated samples were prepared, with polymer thicknesses of 22.5 μm and 40 μm, respectively. Each test sample was diced into 24 pieces, tested by four-point bending, and the data collected was analyzed by Weibull plots, and compared with the bare silicon panels. The Weibull plots for three types of test samples (silicon panel without polymer, silicon panel with 22.5 μm polymer laminated on both sides, as well as silicon panel with 40 μm polymer laminated on both sides) are compared in Figure 33 and critical factors obtained from linear regression are summarized in Table 7. It can be concluded from Figure 33 and Table 7 that polymer liner significantly improved the fracture strength and thus the handling of the thin polycrystalline panels. The thicker polymer led to even higher fracture strength. The comparison between Weibull modulus from different sets of data suggests that the variations were small enough and were similar in each data set, confirming the validity of the tests. These results proved the

hypothesis that surface liners on both sides of the panel help improve the handling of the substrate and thus mitigate the panel breakage problem.

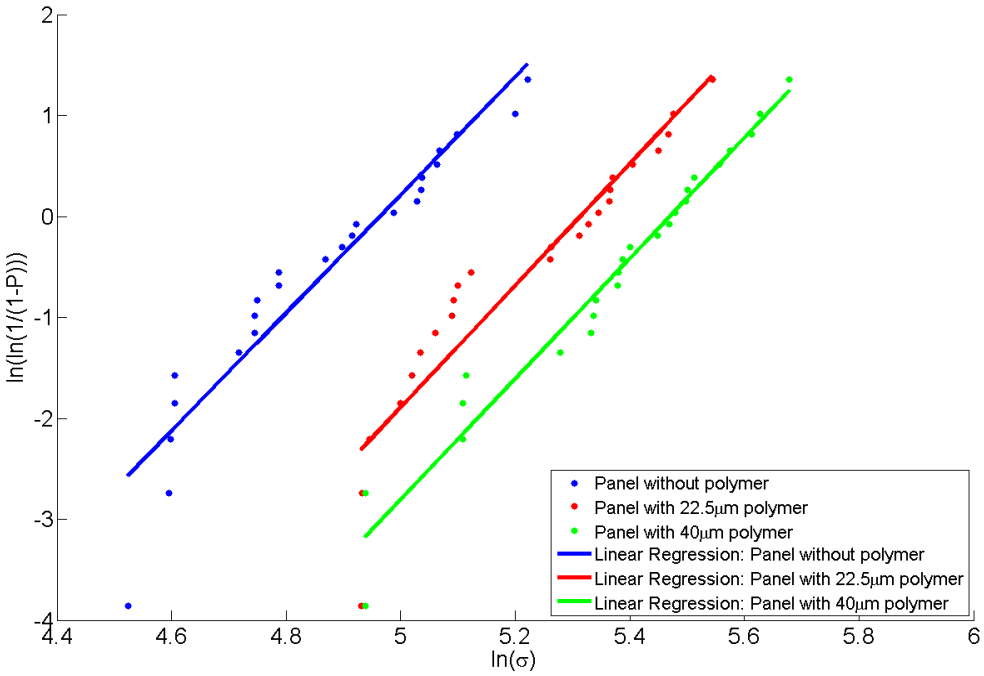



**Figure 33. Weibull plots of fracture strength for silicon panels with and without polymer liners**

**Table 7. Parameter values for fracture strength after linear regression**

| Samples | Average (MPa) | $\sigma_\theta$ (MPa) | $m$ |
|---|---|---|---|
| Panel without polymer | 132 | 143 | 5.85 |
| Panel with 22.5 μm polymer | 188 | 202 | 5.78 |
| Panel with 40 μm polymer | 220 | 237 | 6.25 |

## 4.2 TPV Formation

Via formation, as the first step to achieve high-density 3D interconnections, is one of the critical processes to enable the fabrication of silicon interposers. Unlike DRIE or Bosch process used to form TSVs in single-crystalline silicon, laser ablation is introduced to form TPVs in polycrystalline silicon panels. In this section, the process flows and throughput of DRIE TSVs and laser-ablated TPVs are compared. This section also discusses the theory of laser ablation in silicon and the exploration of different laser methods to form TPVs in polycrystalline silicon panels.

### 4.2.1 DRIE-based TSV vs. Laser-drilled TPV

DRIE or Bosch process is one of the key processes to etch deep and vertical TSVs in single-crystalline silicon wafers. The Bosch process (shown in Figure 34) essentially decouples the two necessary ingredients for anisotropic etching: 1) dissolution of silicon at the bottom, and 2) passivation of the side walls and protecting them against etching. These two steps of etching silicon and protecting the walls with polymer alternate every few seconds. As shown in Figure 34, the etching process uses $SF_6$ plasma chemistry and silicon etching occurs by a reaction with F atoms:

$$Si + 4F \longrightarrow SiF_4 \tag{7}$$

Next, fluorocarbon deposition is used for passivation with gases like $C_4F_8$, $C_3F_6$ or $CHF_3$. This step forms a thin polymer coating on both the bottom of the trench and sidewalls. Since the etching speed of the polymer at the bottom is much faster than the one on the sidewall, in the next step, $SF_6$ etches the polymer in the bottom of the trench and once that is removed, the silicon below the polymer, thus maintaining anisotropy and

enabling vertical profiles. It has been previously reported [66] that the etch rate of up to 10 μm/min is possible by process optimization. However, the frequent switching of gases and etching parameters makes the system quite complicated and expensive.

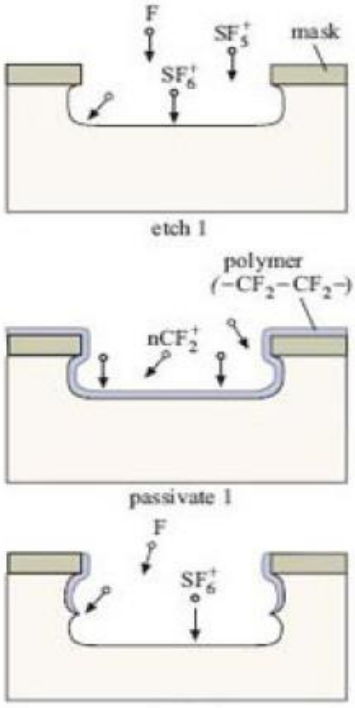



**Figure 34. Schematic drawing of Bosch process [67]**

On the other hand, laser ablation has also been implemented in via drilling for crystalline-silicon. Unlike DRIE, laser ablation enables the removal of materials from a substrate by direct absorption of laser energy, as illustrated in Figure 35. It is a process combining absorption, heating, melting, ablation and finally material removal. Table 8 summarizes the differences between DRIE and Laser on processability. The Bosch process, as discussed previously, requires a mask as well as the complicated lithography process to pattern the substrate for via locations. Laser ablation uses a precise-positioning system to easily locate the via through the coordinates. Such a technology can greatly reduce processing steps for lower production cost. Furthermore, laser ablation can easily

scale to large size substrate panels, which is extremely important for this research targeting 700 mm x 700 mm polycrystalline silicon panels.

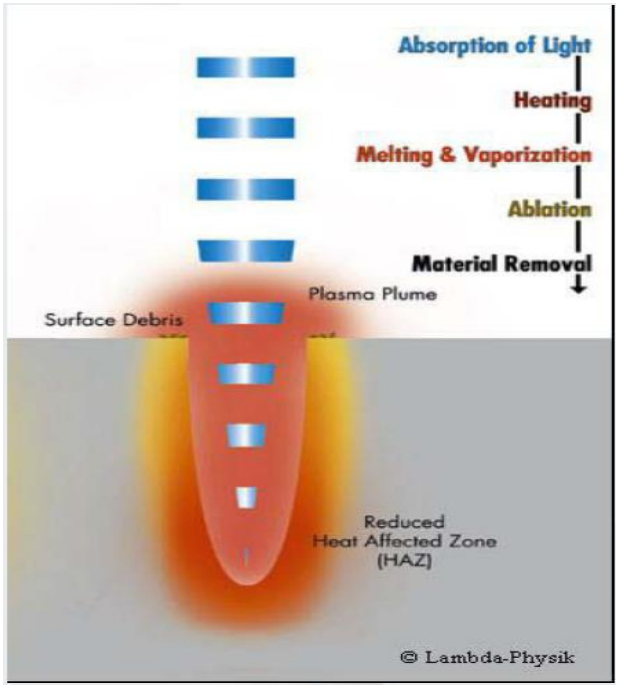



**Figure 35. Schematic drawing of laser ablation [68]**

**Table 8 Process comparison of DRIE and Laser**

| | **Deep reactive-ion etching (DRIE)** | **Laser** |
|---|---|---|
| Process | Bosch process | Laser ablation |
| Photoresist and lithography Required | Yes | No |
| Scalable to large size panels | Challenge | Yes |

In terms of the throughput, two case studies were carried out to evaluate processing time for Bosch process on 300 mm round wafer and laser ablation on 700 mm x 700 mm square panel and the results are listed in Table 9. In this study, the etching time for one substrate was calculated with the assumption of 200 μm substrate thickness, 50 μm via diameter and via density of 2000 per 25 mm x 25 mm interposer sample for both cases. For the Bosch process, the processing time is reasonably independent of the via size and the via density and only relates to the thickness of the substrate. The equation for calculating the throughput of the Bosch process can be simply written as:

$$t = \frac{h}{v} \tag{8}$$

where $t$ =processing time, $h$ =sample thickness and $v$ =processing speed (μm/min). With the reported [66] rate of 10 μm/min, the time for etching the 200 μm wafer is 1200 seconds. It has to be noted that this calculated value excludes any time used for preparation steps before etching, such as lithography and vacuum draw down time.

The case of laser ablation is more complicated. Besides the processing speed, both via density and number of interposers per substrate need to be taken into account during calculation. Therefore, the equation used to calculate the throughput is:

$$t = \frac{cn}{v} \tag{9}$$

where $t$ =processing time, $c$ =via density, $n$ =number of interposers per panel and $v$ = processing speed (vias/second). By plugging in the via density of 2000 per 25 mm by 25 mm interposer, a total number of 729 interposers in one panel (obtained from Chapter 1) and a reported drilling speed of 10,000 vias per second in previous study with a highly

customized laser system [54], the time to produce a 700 mm panel is around 146 seconds, much faster than the case of Bosch process.

**Table 9 Throughput comparison between DRIE and Laser**

| | **Deep reactive-ion etching (DRIE)** | **Laser** |
|---|---|---|
| Via density | 2000/interposer (25 mm by 25 mm) | 2000/interposer (25 mm by 25 mm) |
| Substrate | 300 mm wafer | 700 mm panel |
| # of interposers (25 mm by 25 mm) | 89 | 729 |
| Substrate thickness | 200 μm | 200 μm |
| Via size | 50 μm | 50 μm |
| Etch/drilling rate | Up to 10 μm/min[66] | Up to 10000 vias/sec[54] |
| Processing time | 1200s | ~146s |

In summary, considering the simpler process steps, higher throughput as well as the ability to scale to larger substrate, laser ablation was selected to form TPVs in this particular study.

### 4.2.2 Theory of Laser Ablation in Silicon

Laser ablation was chosen for TPV formation in polycrystalline silicon panels based on the published data on throughput. This section discusses the theory of laser ablation in silicon, based on which different laser types were explored for TPV formation at small via diameter and pitch.

The first step in laser processing is the absorption of incident irradiation by the material. Such a step can be described by the Beer-Lambert's law [69], which relates the attenuation of light with the properties of the material in which light is travelling:

$$\frac{I}{I_0} = e^{-\alpha l} \tag{10}$$

where $I$ is the intensity of transmitted radiation, $I_0$ is the intensity of the incident radiation, $l$ is the penetration size and $\alpha$ is the absorption coefficient. In this equation, the absorption coefficient is the most critical factor, which determines how far the light of a particular wavelength can penetrate into a material before it is absorbed. A material with lower absorption coefficient means poor absorption and if the material is thin enough, it appears transparent to that wavelength. The absorption coefficient depends on both the material and the laser wavelength. In Figure 36, the absorption coefficient of silicon is plotted against the wavelength [70]. It can be seen that silicon shows good absorption with light of wavelength smaller than 1000 nm, and very high absorption when the wavelength is between 200 and 400 nm.

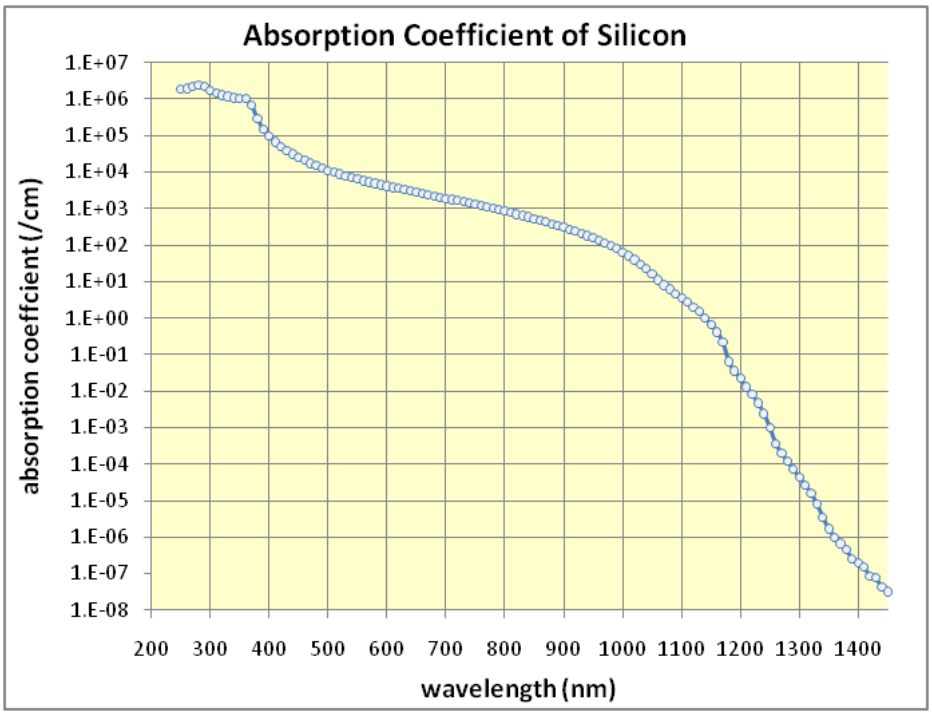



**Figure 36. Absorption coefficient of silicon for light with different wavelength [70]**

The reason that silicon presents higher absorption with light having smaller wavelength relates also to the energy of the photon. Generally, the energy of photon corresponding to a specific wavelength can be written as:

$$E = \frac{hc}{\lambda} \tag{11}$$

where $E$ is the energy, $h$ is the plank constant $c$ is the speed of light and $\lambda$ is the wave length of the light. It is clear that the energy is in inverse proportion to the wavelength of the light. For semiconducting materials like silicon, photons which have energy levels below the band gap do not have sufficient energy to excite an electron into the conduction band from the valence band and the light will not be absorbed. This is the reason for the lack of absorption in silicon for laser wavelengths over 1000 nm.

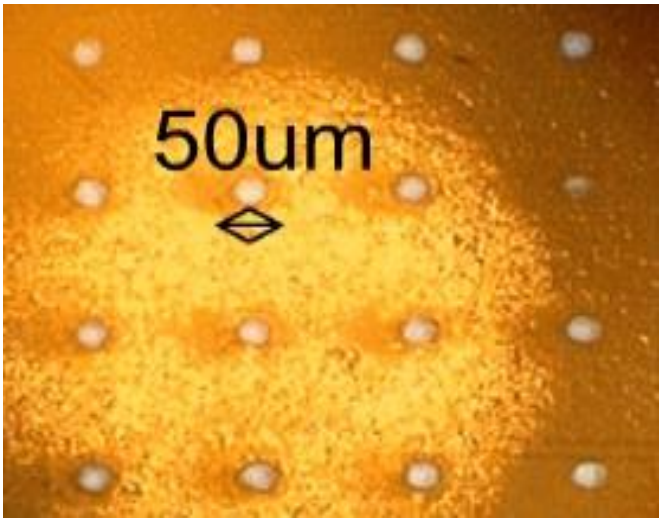
Therefore, smaller wavelengths with higher energy are preferred for laser ablation of silicon due to its high absorption.

The laser ablation mechanism for silicon can be simply described as follows: when light is absorbed in silicon, the photon with sufficient energy leads to the stimulation of electron over the bandgap. The energy generated then can contribute significantly to the heating and finally removal of the material.

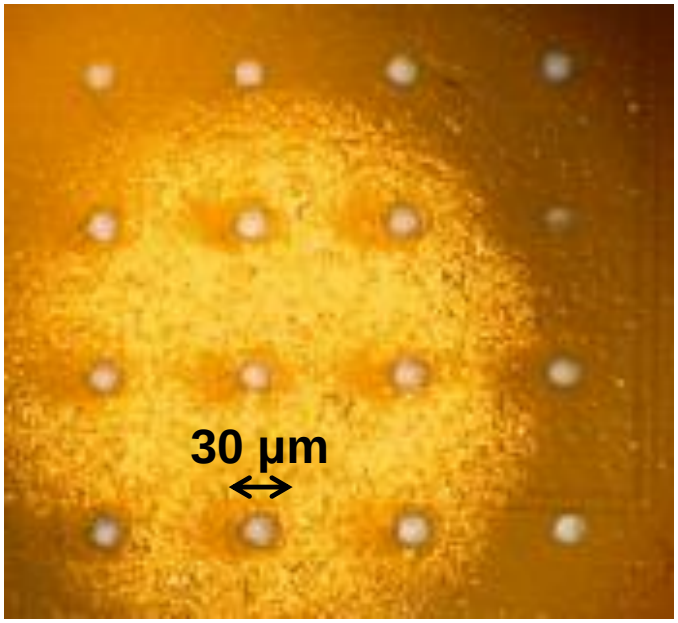
Based on the theoretical understanding, three types of lasers were selected for TPV formation, including picosecond lasers (355 nm), excimer lasers (248 nm) and solid-state UV lasers (355 nm). The exploration of TPV formation in thin polycrystalline silicon panels by three different laser technologies is discussed in the following sections.

### 4.2.3 Picosecond Laser

Picosecond laser is a relatively new type of laser and is defined by pulse durations of a few picoseconds to some tens of picoseconds. Such a laser was chosen for the experiments because of its ability to mitigate heating effects with short pulse lengths and long relaxation times in between pulses. The operating parameters of the picosecond laser used in this study were: wavelength - 355 nm; pulse energy - 16 μJ; repetition rate - 500 KHz. Vias with 50 μm diameter were successfully formed in 200 μm thick polycrystalline panels and the top and bottom views are shown in Figure 37.




(a)




(b)

**Figure 37. (a) Entrance and (b) exit view of the via drilled by picosecond laser**

Although picosecond lasers achieved good quality vias, their biggest disadvantage is the low throughput. This is due to the trepanning drilling method the picosecond laser used in this study. In a trepanning method (Figure 38), the position of the beam will move and remove cylindrical core from the material. Such a method can improve the hole

quality but can be very slow especially for relatively larger vias. In the test carried out above, the via throughput was limited to 2~3 vias per second. Due to this drawback, picosecond laser ablation was not pursed further for TPV formation.

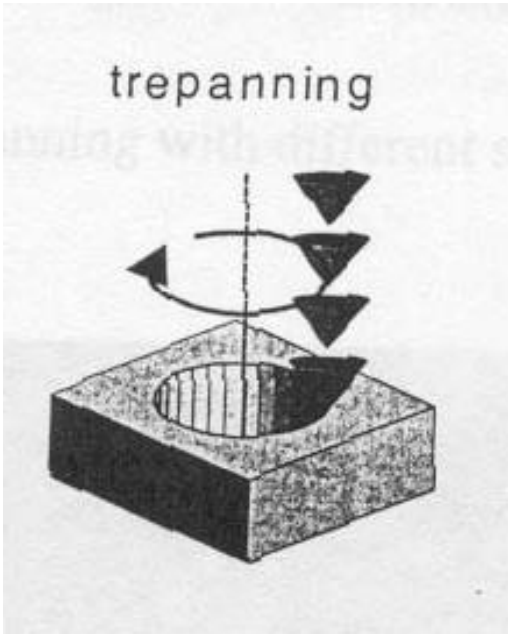



**Figure 38. Trepanning method for via drilling [71]**

### 4.2.4 Excimer Laser

As shown in Figure 36, silicon has very high absorption for light with wavelengths between 200 nm and 400 nm. As a result, excimer lasers, which fall in this range, were selected for exploration. Excimer lasers usually generate laser energy by applying a high voltage across a gas cavity consisting of a mixture of noble gases and halogens. In this experiment, a KrF-based excimer laser with 248 nm characteristic wavelength was used. During the operation of the excimer laser, the energy absorbed causes the krypton gas to react with the fluorine gas, producing the complex KrF at its

excited state. In the second step, the complex dissociates into unbounded atoms, resulting in laser energy at 248 nm wavelength. The complete step can be presented in the following equation form:

$$2K_r + F_2 \longrightarrow 2K_rF \tag{12}$$

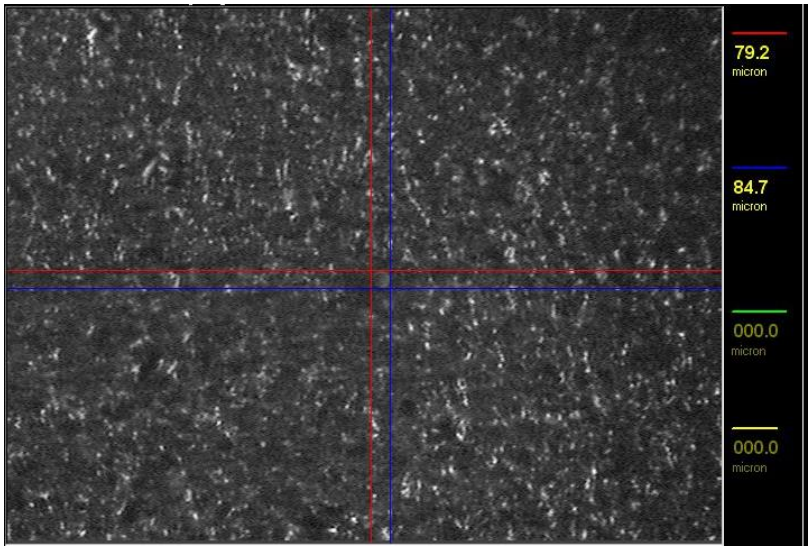
And then

$$2K_rF \longrightarrow 2K_r + F_2 \tag{13}$$

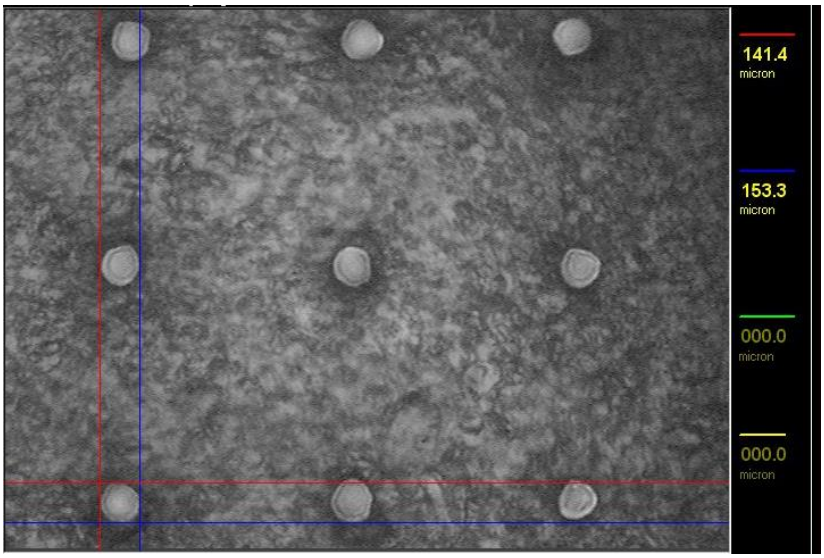
Typical excimer lasers have output powers of between a few watts and hundreds of watts, making them the most powerful laser sources in the ultraviolet region. Furthermore, the smaller wavelength of the excimer laser helps to achieve smaller via diameter due to minimum thermal effects and damage around the vias. Smaller beam spot sizes are required to form smaller diameter TPVs and the spot size formula can be written as:

$$d = \frac{4M\lambda f}{\pi D} \tag{14}$$

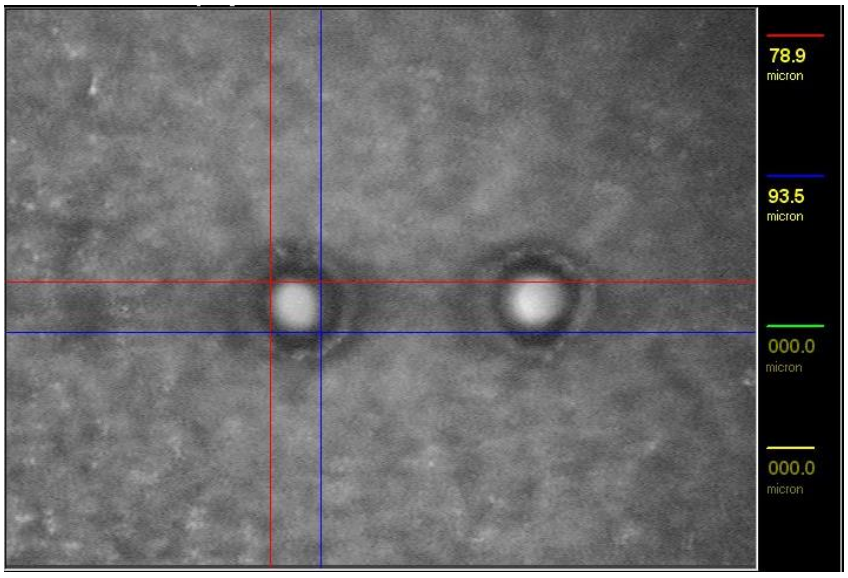
where $d$ is the spot size, $\lambda$ is the wavelength, $f$ is the lens focal length, $D$ is input beam diameter at the lens and $M$ is the beam mode parameter. It is clear that shorter wavelengths of the excimer laser can lead to smaller spot sizes, and thus smaller via sizes. Figure 39 shows a few SEM images of the TPVs formed by 248 nm excimer laser ablation in polycrystalline silicon. Vias with diameters ranging from 6 to 15 μm were successfully fabricated by excimer laser.


79.2
micron
84.7
micron
000.0
micron
000.0
micron

(a)


141.4
micron
153.3
micron
000.0
micron
000.0
micron

(b)




(c)

**Figure 39. Top view of vias drilled by excimer laser with diameter of (a) 6 µm, (b) 12 µm and (c) 15 µm**

Although excimer laser ablation resulted in small via diameters, it usually suffers from high production cost due to the high operating cost of the complex gas based laser source, and the damage to the projection optics at ultra-short wavelengths. Since cost reduction is one of the main goals for the implementation of polycrystalline silicon interposers, excimer lasers were excluded from further studies to form liners and metallize the TPVs.

### 4.2.5 UV Laser

Due to the disadvantages of both picosecond lasers and excimer lasers, solid state UV lasers were explored for the best combination of via size reduction, cost and throughput. Unlike picosecond and excimer lasers, which are mainly used in research, UV lasers have been widely adopted in the industry for manufacturing and thus the operating cost is relatively low. UV lasers in this study operated at 355 nm wavelength

and used percussion drilling, as shown in Figure 40. Such a method delivers continuous laser pulses to the same spot and has been regarded as the best compromise between via quality and throughput. Both small and large vias were formed by UV lasers, operating at 355 nm, and some examples are shown in Figure 41 with different entrance diameters. The SEM image of cross-sections of the drilled vias is also shown in Figure 42.

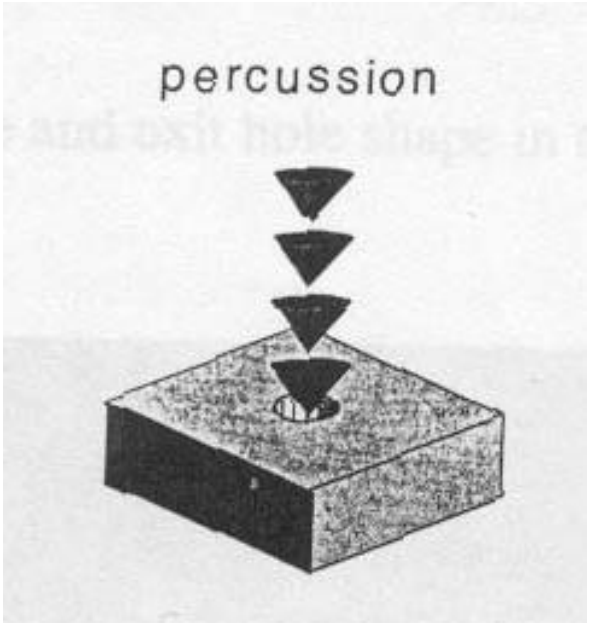
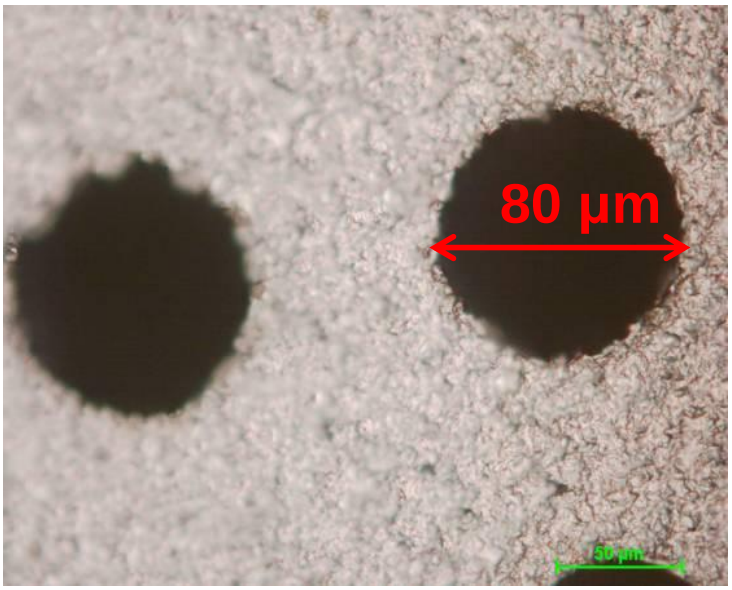
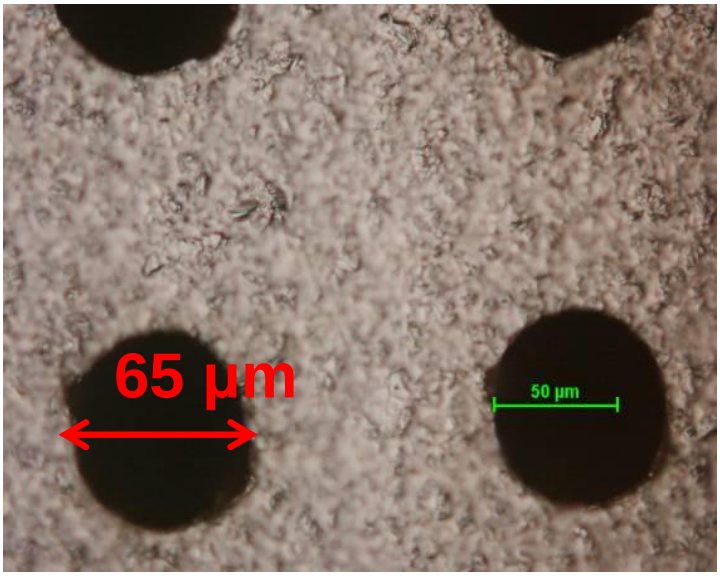


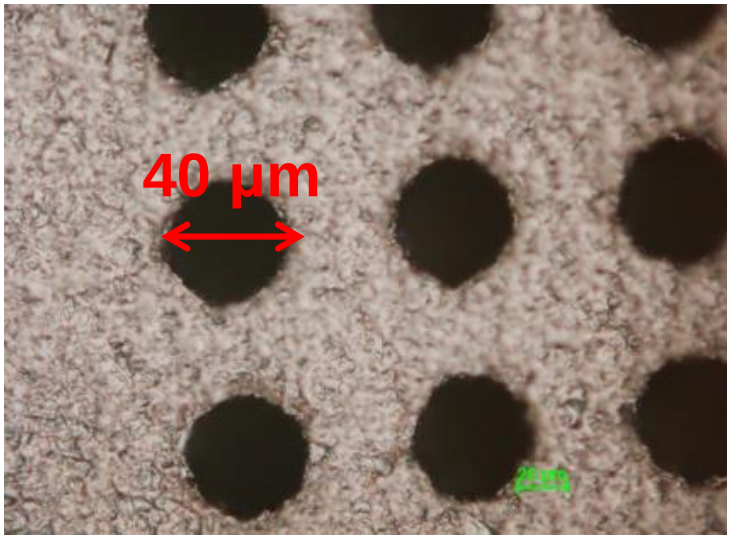

**Figure 40. Percussion method for via drilling [71]**



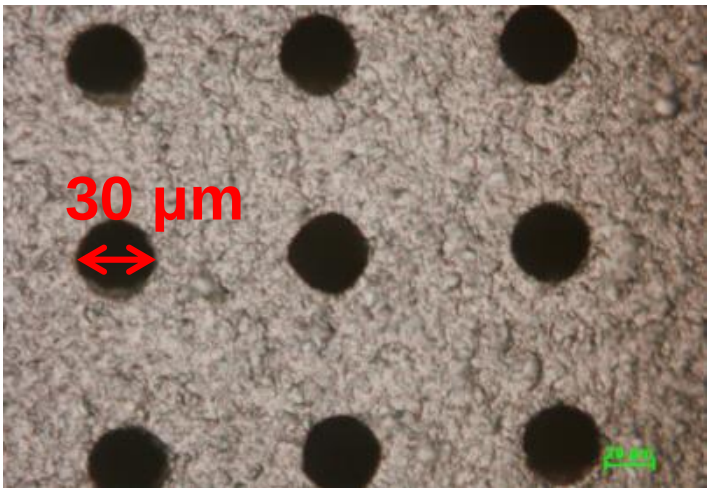

(a)



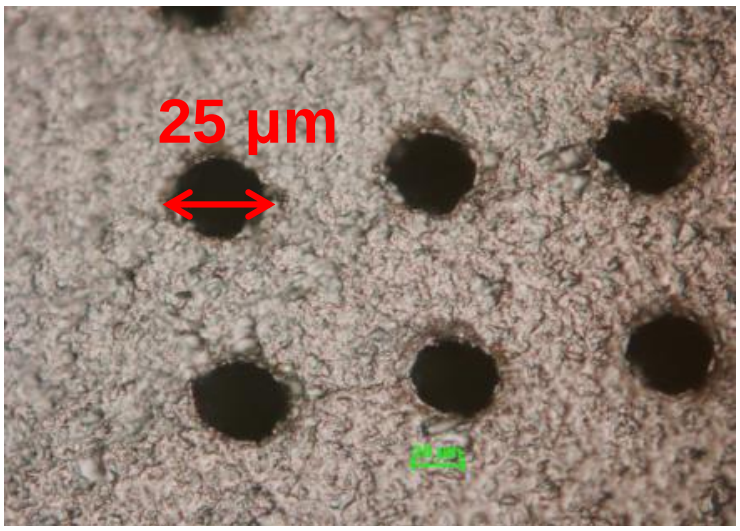

(b)



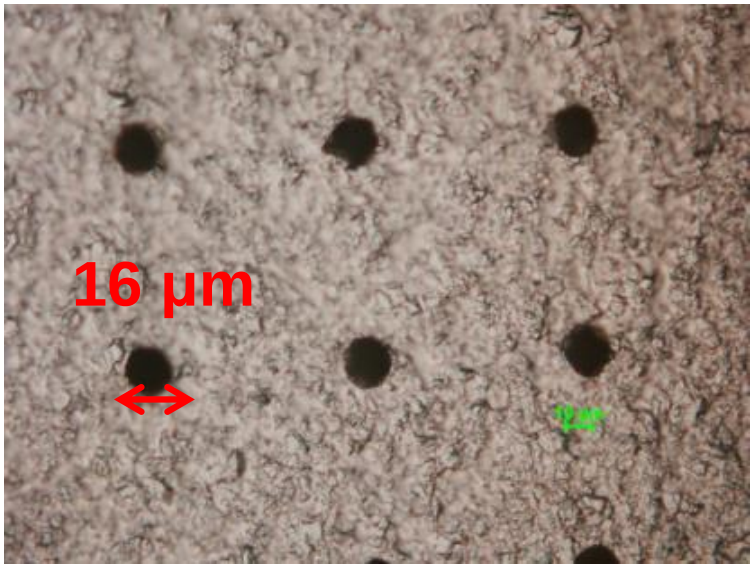

(c)




(d)




(e)




(f)

**Figure 41. Optical images of vias drilled by UV laser with (a) 80 µm entrance and (b) 65 µm exit; and (c) 40 µm entrance and (d) 30 µm exit ; and (e) 25 µm entrance and (f) 16 µm exit**

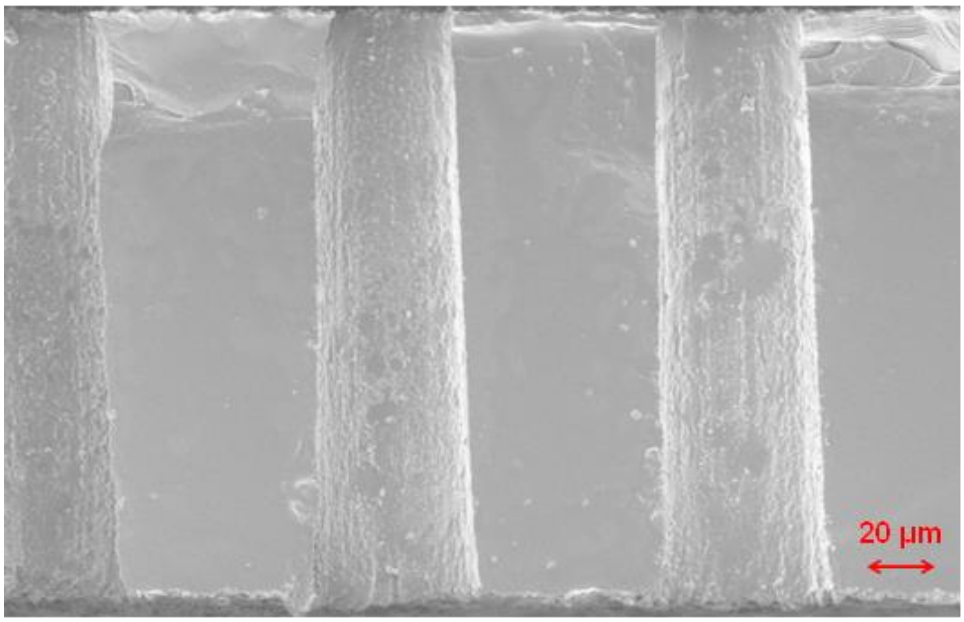



**Figure 42. SEM cross-section image of TPV drilled by UV laser**

Due to the nature of the percussion process, some amount of via tapering can occur and this can be seen from both Figures 41 and 42. Tapering by definition refers to the reduction of via diameter with depth and a schematic view is shown in Figure 43.

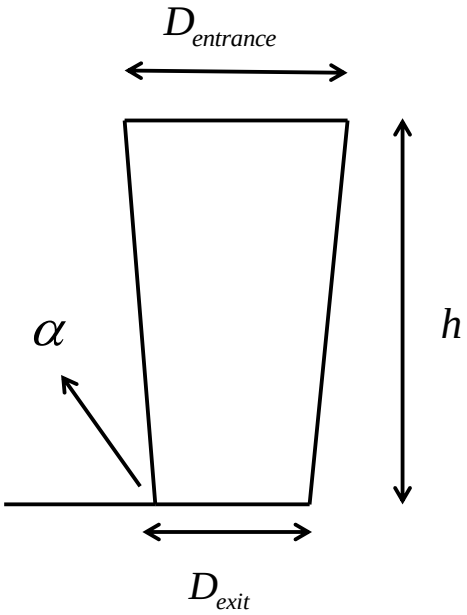



**Figure 43. Schematic cross-section drawing of via tapering**

Based on Figure 43, the via tapering can be calculated by the following equation:

$$\alpha = \arctan\left(\frac{2h}{D_{entrance} - D_{exit}}\right) \tag{15}$$

where $\alpha$ is the tapering angle, $D_{entrance}$ is the diameter of the via entrance, $D_{exit}$ is the diameter of the via exit and $h$ is the thickness of the substrate. Considering the case with via entrance of 80 μm and via exit of 65 μm (Figure 41 (a), (b)), a tapering angle of around $88°$ can be calculated. A small amount of via taper can be acceptable to meet the electrical performance requirements [21], and it can be beneficial for ease of metallization.

Based on the exploration of multiple laser options, UV laser ablation was down selected for further studies since it provided the best trade-off between hole quality, throughput and cost. Therefore UV lasers, operating at 355 nm, were used to form the TPVs in polycrystalline silicon panels for electrical characterization and reliability tests, which will be discussed in the next chapter.

### 4.3 TPV Liner Fabrication

In polycrystalline silicon interposers, liners are required on the top and bottom surfaces of the silicon as well as the TPV sidewalls for electrical isolation, as discussed in Chapter 3. The improved reliability of TPVs due to the stress buffering effect of the low modulus polymer liners was also shown by finite element modeling. As a result, thick polymer liners are required as a replacement for the thin oxide liners and diffusion barriers used for TSVs. This section describes the exploration of three different methods for TPV liner fabrication, namely, spray coating, electrophoretic deposition (ED) and a

double laser process. The mechanisms for each method are explained, and the results are analyzed based on theory.

### 4.3.1 Spray Coating

Spray coating was initially developed to address the uniformity challenges of spin coating processes. Figure 44 shows the schematic drawing of a spray coating system. Such a process uses an ultrasonic spray nozzle, which generates a distribution of droplets of micrometer size, minimizing centrifugal forces and improving uniformity.

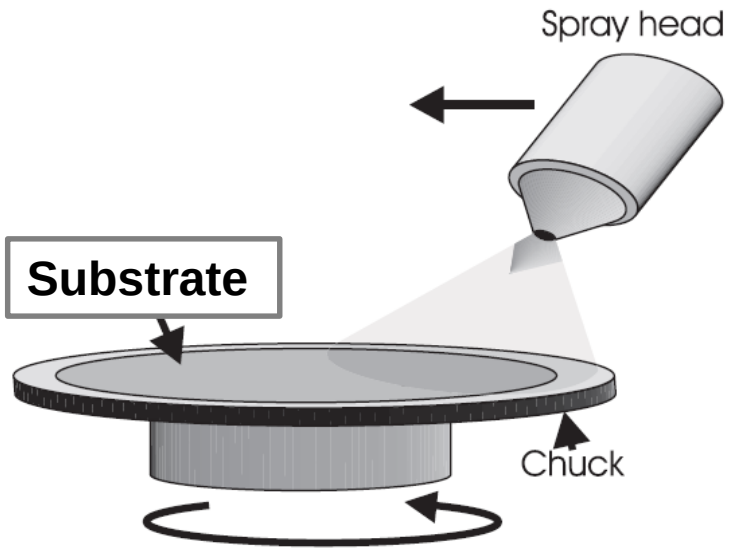



**Figure 44. Schematic drawing of spray coating system (modified from [72])**

Spray coating was applied to TPVs with 200 μm height and 60 μm entrance diameter for conformal liner deposition and the cross-section of the polymer-lined TPV is shown in Figure 45. The coating process was done using an EVG 150 spray coating tool and benzocyclobutene (BCB) polymer from Dow Chemical. Spray coating was applied to both upper and lower sides of the polycrystalline silicon panel, followed by a 250℃ hard

cure to achieve polymerization. It can be seen that both the top and bottom surfaces were successfully coated with 10 μm polymer liner thickness, while the TPV sidewall liner was around 5 μm thickness. However, thinner coverage around the via hole corners was observed, and this presents the biggest challenge for this process, and such thin corner liners can lead to potential electrical and reliability problems.

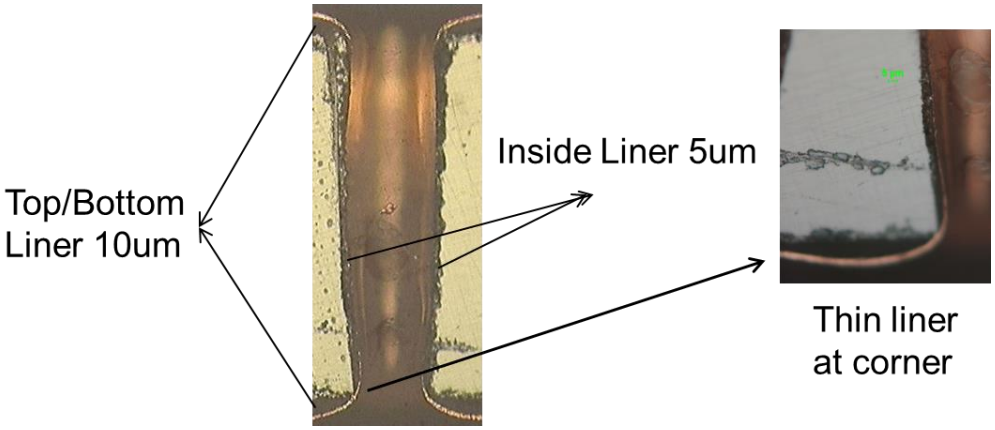



**Figure 45. Cross-section image of TPV with polymer liner by spray coating**

The poor coverage on the via corners can be explained based on the physical behavior of liquids. This is illustrated in Figure 46, and is due to the gravitational and surface tension forces that act to pull back the BCB polymer from sharp topographic edges. On one hand, gravity reduces the film thickness on the edge, since the polymer tends to flow down the slope. At the same time, surface tension of the resist pulls the resist back from the corner and leads to bead formation. This poor coverage is a fundamental challenge and therefore, spray coating was not further explored in this study.

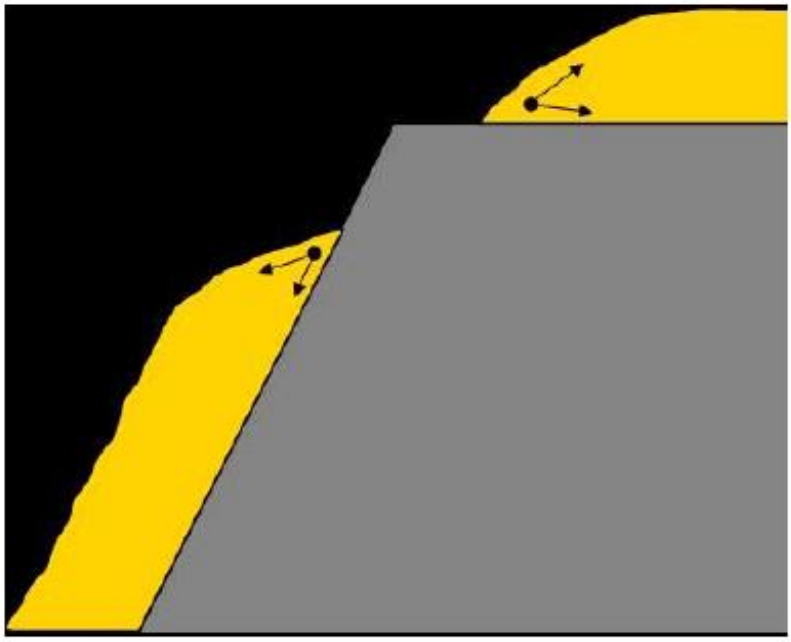


**Figure 46. Physical behavior of liquid around edge [73]**

### 4.3.2 Electrophoretic Deposition

Electrophoretic deposition (ED) is an electrolytic plating process in which ionically charged materials are deposited from aqueous solutions onto a conductive substrate by application of a voltage driven external bias. In this study, the ED materials deposited were polymer aggregates with positively charged surfaces. The mechanism of the ED process is explained in Figure 47. First, $OH^-$ ions are generated from $H_2O$ due to free electrons. Then at the cathode (substrate), the positively charged polymer (red dot in Figure 47) reacts with $OH^-$ ions to form a thin polymer liner (blue dot in Figure 47). With polymeric materials, the deposited film insulates the conductive substrate and hence the process becomes self-limiting at a certain layer thickness, beyond which further deposition cannot take place. Because the substrate is used as an electrode, a conductive

layer such as a thin metal seed layer is usually required. However, since the polycrystalline silicon panels used in this study had low resistivity (0.5 Ω-cm), the conductivity of the substrate was sufficient to initiate electrophoretic deposition without a seed layer. This represents one of the breakthroughs in this research and the ability to directly deposit electrophoretic materials on conducting silicon substrates has many potential applications.

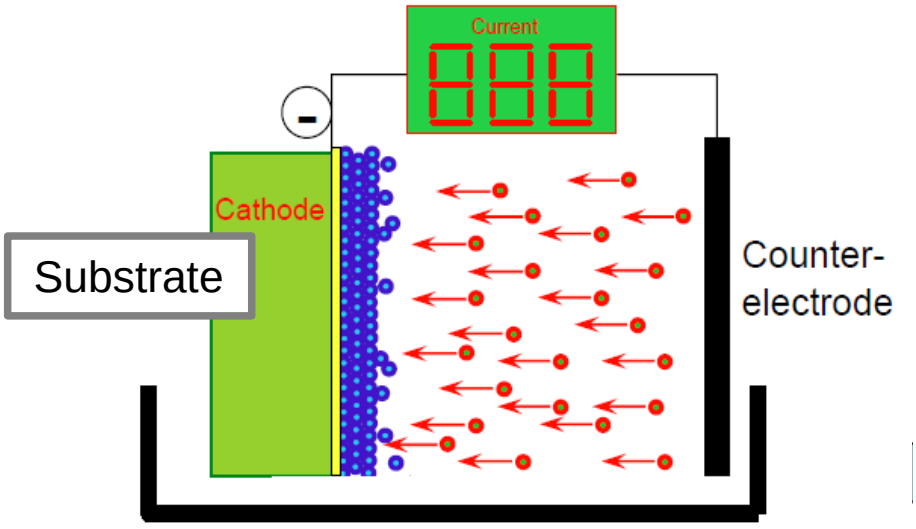



**Figure 47. Schematic drawing of ED system (modified from [74])**

The ED process experiments were carried out on 200 μm thick silicon panels with 100 μm diameter TPVs. One side coating was applied at room temperature, followed by a soft cure at 75°C for 5 minutes, UV exposure at 250 mJ/cm$^2$, and thermal cure to densify the coating at 160℃. The samples were then sputtered with Ti-Cu seed layers and the TPVs were filled by electrolytic copper plating. The cross-section of TPVs with filled Cu and ED polymer liner is shown in Figure 48. Both surfaces were coated with 10 μm thick liners. The via sidewall liner thickness varied, with thin coverage (~1 μm) around the via

entrance and exit corners. Such a thin liner does not meet the design guidelines proposed in Chapter 3. This non-uniformity may be due to different local conductivity, which controls the thickness of ED polymer, resulting from various surface topologies. Besides this issue, the ED process also requires a dedicated high voltage power source (>1kV) and also suffers from plating bath stability challenges. Due to the challenges in liner thickness control, this method was not pursued further in this research.

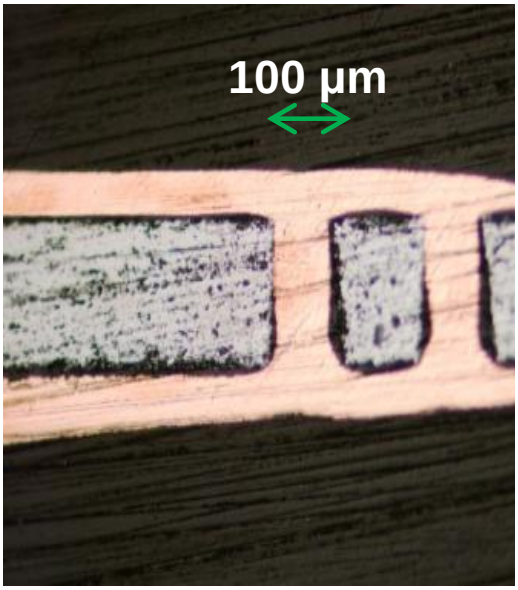



**Figure 48. Cross-section view of metalized TPV with ED polymer**

### 4.3.3 Double Laser Method

The double laser method was developed to address the shortcomings of both the spray coating and ED processes. As the name represents, such a method involves two laser steps to enable polymer-lined TPV fabrication in polycrystalline silicon panels. As shown in Figure 49, the first laser step is actually used for via formation, after which the

TPVs are filled with polymer and surface liners are also formed. Then a second laser process is carried out to ablate the polymer inside the TPV using a smaller beam diameter than that used for the TPV in silicon, leading to thick polymer liners on the via side walls. The double laser method has several advantages over spray coating and ED processes, including: 1) good corner and edge coverage, 2) control of thicknesses of via sidewall liners, and 3) double-side processing with dry film polymers for large panel scalability and cost reduction.

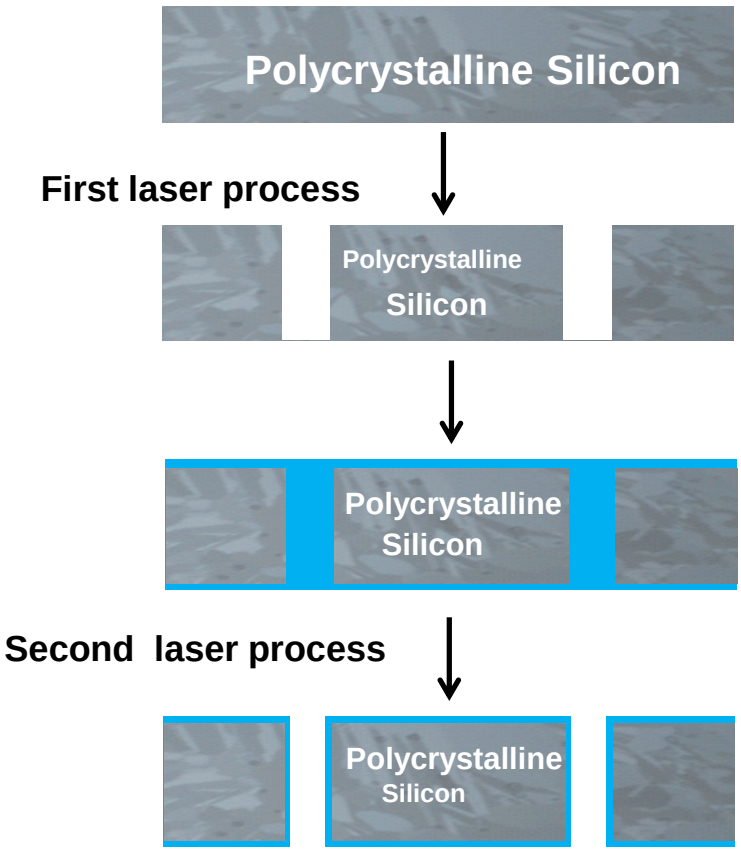



**Figure 49. Double laser method for liner formation**

4.3.3.1 Liner Material Selection

In order to meet the requirements of the liner as a replacement for $SiO_2$ liners and the diffusion barrier layers, the polymer material has the following property requirements, based on the discussion from Chapter 3 as well as the nature of the double laser process: 1) comparable or lower electrical loss than $SiO_2$ to achieve high performance, 2) high insulation reliability to prevent Cu diffusion, 3) low modulus to improve reliability, 4) high flow for ease of via filling, and 5) high absorption of laser irradiation for efficient ablation. For this study, a number of polymer chemistries were considered, and finally a cyclo-olefin resin system, named Zeon Insulation Film (ZIF), from Zeon Corporation, Japan was selected due to its unique properties, which are summarized in Table 10.

**Table 10. Unique properties of ZIF material**

| **Properties** | **Value** |
|---|---|
| Dielectric Constant | 3.1 |
| Loss Tangent | 0.002 |
| Water Absorption | 0.1% |
| Young's Modulus | 6.9 GPa |
| Laser Processable | Yes |
| Flow-ability | Yes |

In addition to its excellent dielectric properties (loss tangent of 0.002), ZIF material has low water absorption of 0.1%, which helps in achieving high insulation reliability. Such a property was evaluated by the experiment shown in Figure 50 [75]. The stacks of Cu-ZIF-Cu were fabricated with ZIF liners of different thicknesses. The samples were preconditioned at 125℃ for 6 hours, followed by a 60℃/60%RH environment for 4 hours and lastly subjected to 5x reflow cycles at 260℃. Then the resistance between the two Cu layers was monitored under 130℃ /85%RH with 3.3 V external voltage. The high and stable resistance for over 400 hours confirmed the excellent insulation and Cu diffusion barrier properties of the polymer. The ZIF polymer also exhibits low elastic modulus that is required to buffer the stress between the copper and silicon, and improve the thermo-mechanical reliability of the TPVs. The ZIF polymer is available as a thin dry film that can be laminated on both sides of the silicon substrate and has high flow at moderate temperatures for good via filling. It is also compatible with commonly used UV and $CO_2$ laser ablation systems, which is essential for double laser method.

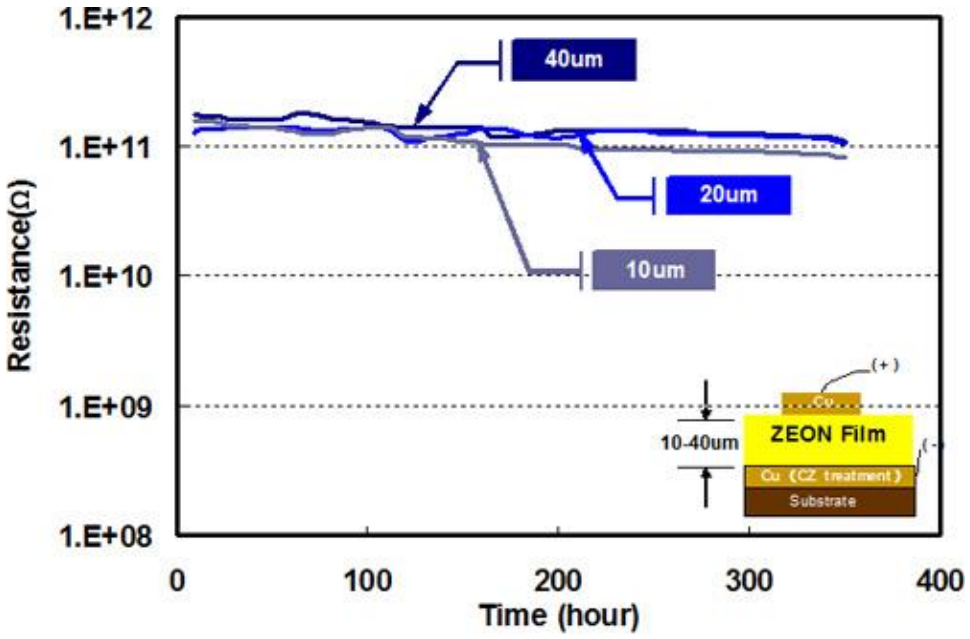



**Figure 50. High insulation reliability of ZIF polymer [75]**

4.3.3.2 Polymer Filling in TPVs and Surface Liner Formation

Following the first laser process to form TPVs in the silicon panels, ZIF polymer dry films were laminated on both sides to fill the TPVs and form the surface liners in a single step. A key challenge with the use of dry film polymers is their inferior adhesion to silicon compared to liquid polymers. This adhesion challenge was addressed by a two-step process, starting with a plasma cleaning step to remove impurities from the silicon surface, followed by surface treatment with silane solutions (3-aminopropyltrimethoxy silane). This silane treatment results in the formation of covalent bonds at the interfaces between silicon and the applied polymer films to improve adhesion. The mechanism of such adhesion improvement has been reported [76] and is illustrated in Figure 51. The process is briefly described as follows: OH groups first form on the silicon surface after plasma treatment due to oxidization. Then the silane reacts with the OH groups and robust chemical bonds are formed between the silane molecules and the surface of silicon

after a drying process. When ZIF is laminated, the polymer displaces the “H” atom sites and forms “ZIF-N-Si” bonds. Hence silane tends to bridge between silicon and ZIF to improve the interfacial adhesion. SEM images (Figure 52) obtained on silicon surfaces before and after silane treatment confirmed the salinization process.

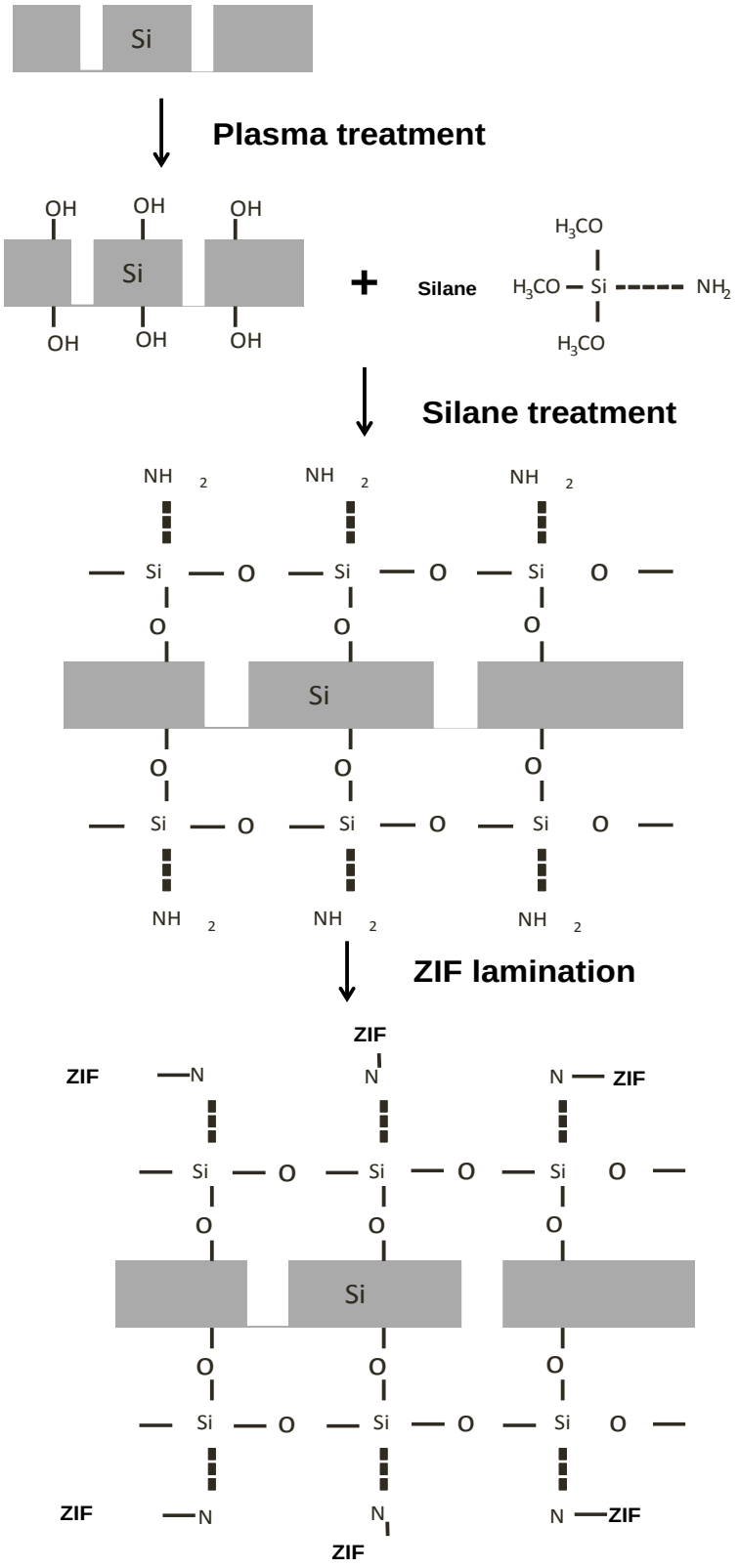
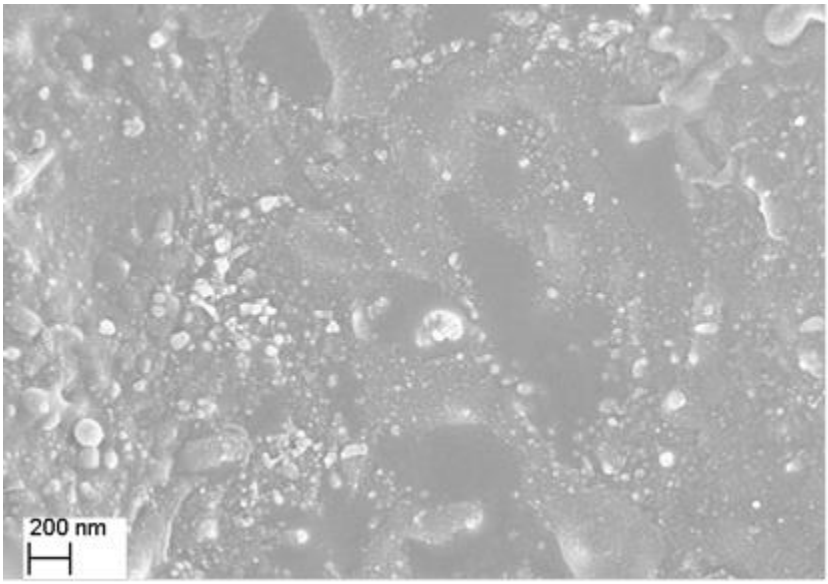
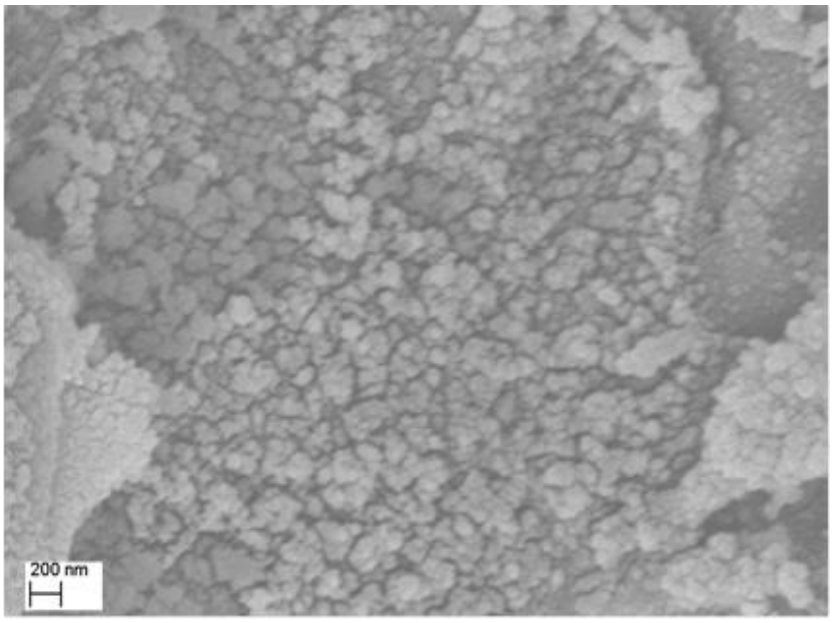



**Figure 51. Mechanism of silane treatment for adhesion improvement process**



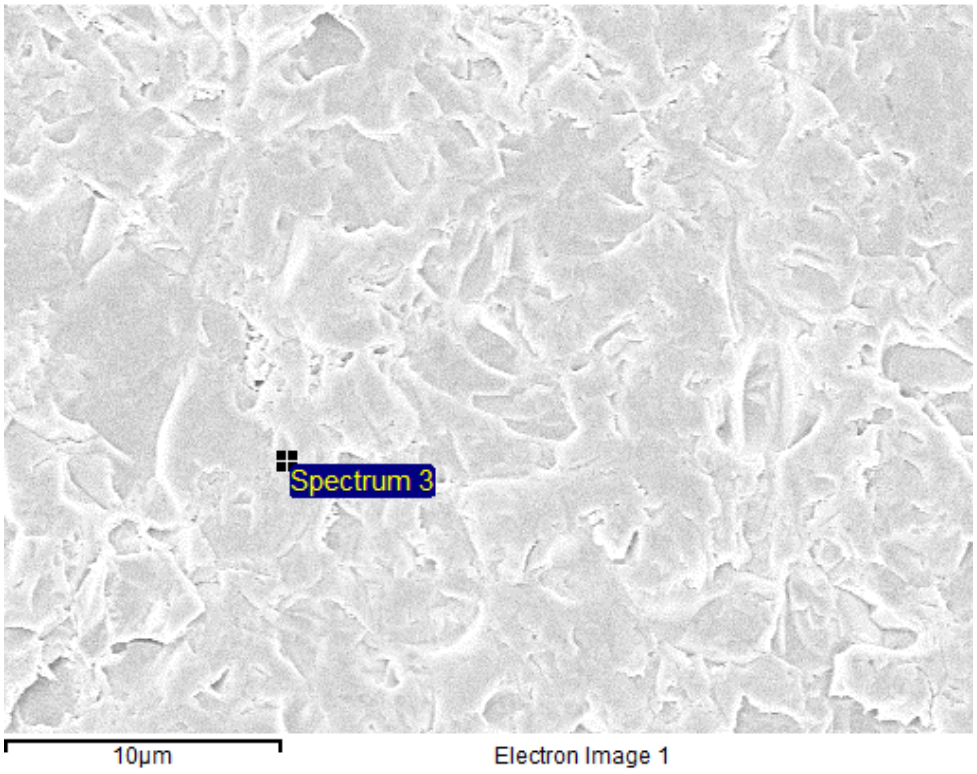

(a)



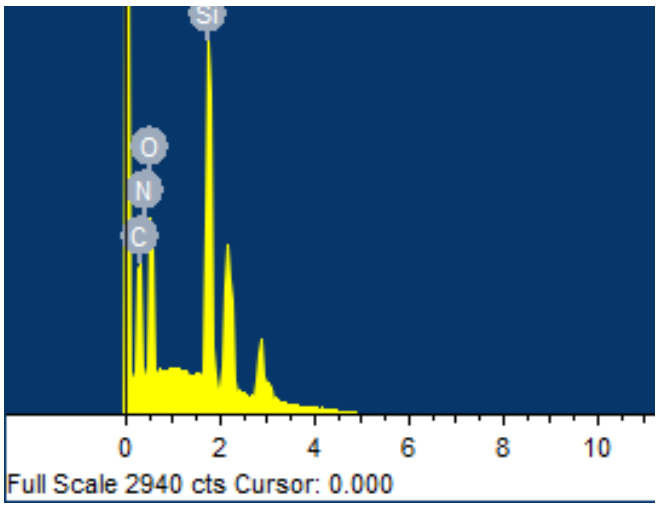

(b)

**Figure 52. SEM images for silicon surfaces (a) before and (b) after silane treatment**

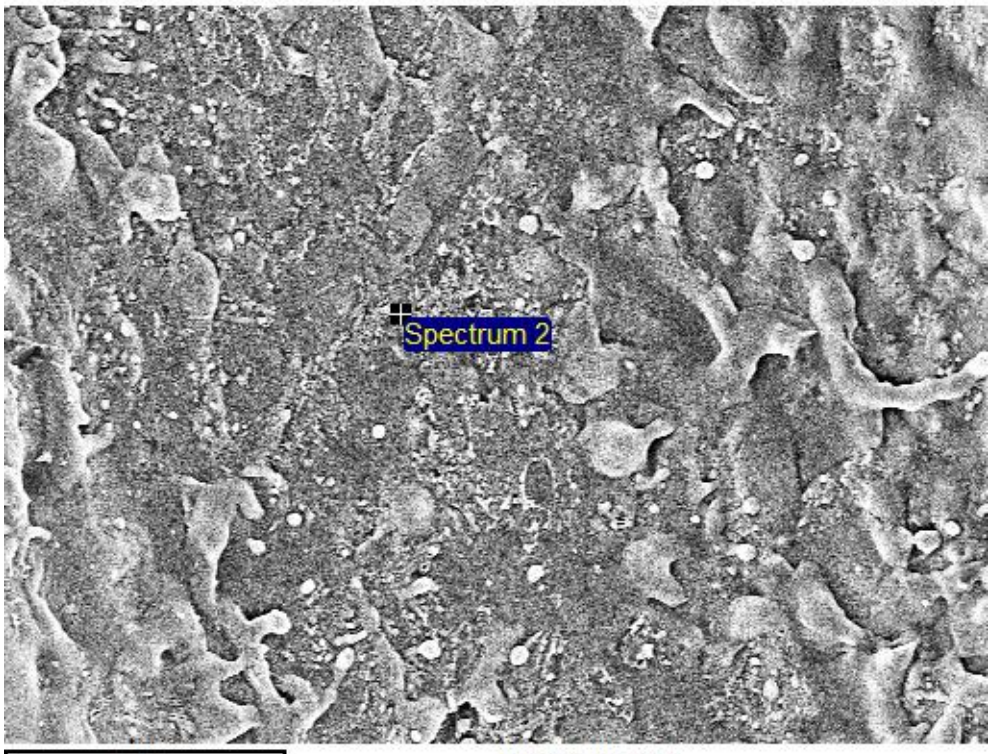
In order to show that this mechanism also improves the via sidewall adhesion, the TPV sidewall was first characterized using SEM and EDS (Energy Dispersive X-ray Spectroscopy) before and after plasma treatment, respectively. The EDS results (Figure 53) confirmed the increase of oxygen atoms originating from the oxidation process during plasma treatment. Then, SEM analysis was carried out on the TPV sidewalls before and after silane treatment. It can be observed from the SEM images in Figure 54, that after silane treatment the coating covered the surface of the via sidewall, and later formed covalent bonds with the deposited ZIF polymer.



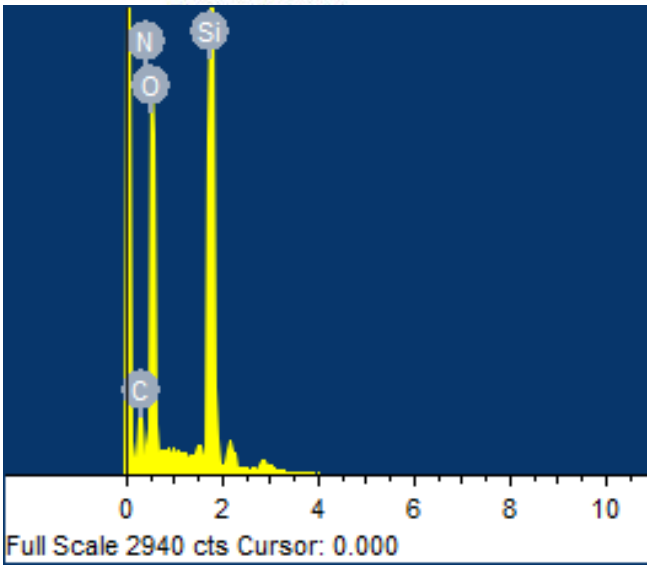

| Element | Atomic% |
|---|---|
| C K | 12.86 |
| N K | 3.83 |
| O K | 24.76 |
| Si K | 58.55 |
| Totals | 100 |




(a)

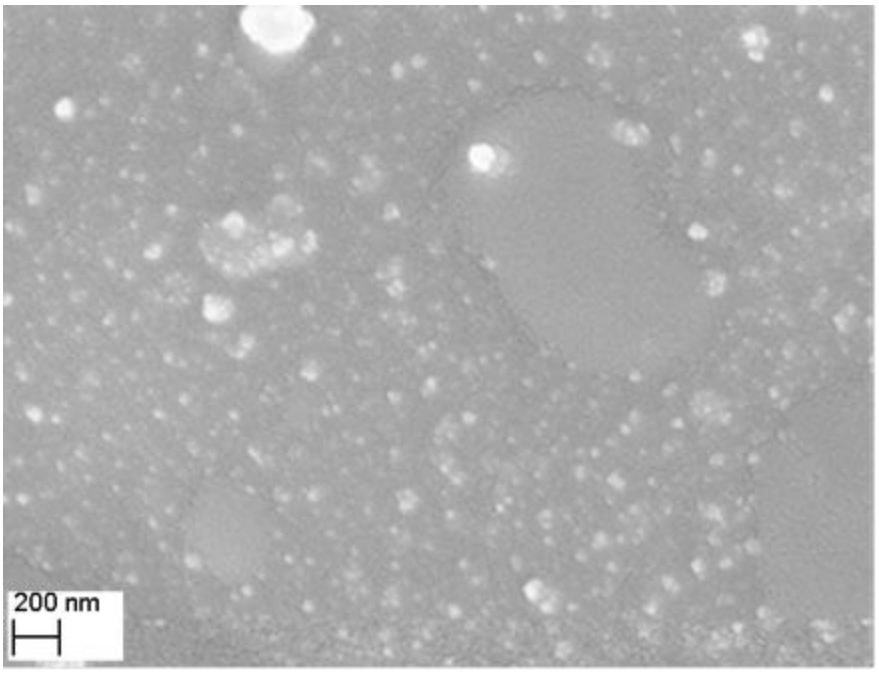



| Element | Atomic% |
|---|---|
| C K | 9.72 |
| N K | 2.15 |
| O K | 32.70 |
| Si K | 55.44 |
| Totals | 100 |

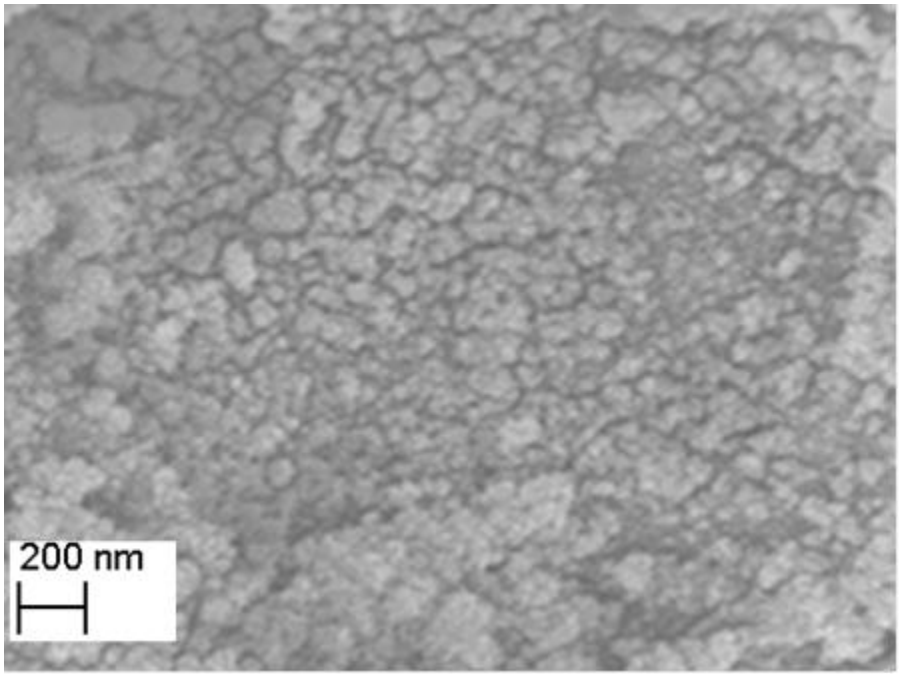



(b)

**Figure 53. EDS results of TPV sidewall (a) before plasma treatment and (b) after plasma treatment**




(a)




(b)

**Figure 54. SEM images of TPV sidewall (a) before silane treatment and (b) after silane treatment**

After silane treatment, the polymer was laminated for TPV filling. The flow-ability of polymer is directly related to the intrinsic viscosity of the polymer, which, based on Mark–Houwink equation [77], can be written as:

$$[\eta] = KM^{a} \tag{16}$$

where $[\eta]$ is intrinsic viscosity of the polymer, $K$ and $a$ are Mark–Houwink parameters, and $M$ is molecular weight. Under heat treatment, the viscosity decreases and the polymer starts to flow and finally fill the via. This is regarded as the mechanism of polymer filling. Since ZIF has a low molecular weight, it has smaller intrinsic viscosity and hence higher flow for filling during lamination.

Two methods, with roll lamination and vacuum lamination, were evaluated for polymer filling. Figure 55 shows a comparison between the single-side and double-side lamination processes. The single-side roll lamination process was first studied. In this process polymer was laminated by a small amount of pressure applied from a hot roll to the top and bottom surfaces, sequentially one side at a time. However voids were observed inside the vias after filling. This was attributed to the air trapped inside the via during the lamination step, and these voids create potential problems in subsequent laser ablation and via reliability. An improved filling method using a vacuum lamination tool was then carried out, in which both sides of the silicon substrate were laminated at the same time at 95℃. The stack-up used in the lamination chamber is shown in Figure 56. Thick Cu foils were used for protection and to avoid polymer contact with the lamination platens, which could have resulted in contamination and defects in the liner. This vacuum-assisted process removed the air inside the via, leading to a faster and void-free filling process for the TPVs. In addition, such a double-side process can help to mitigate

any potential warpage of the thin silicon panel generated by the heating and cooling cycles in the lamination process.

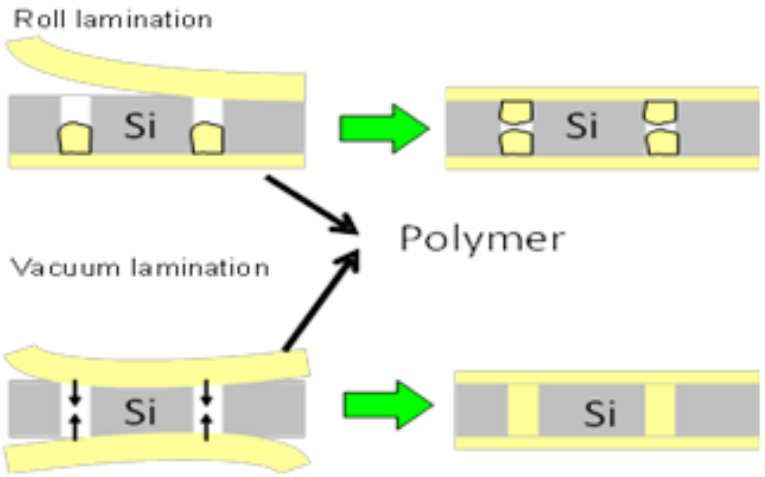



**Figure 55. Single-side roll lamination vs. double-side vacuum lamination**

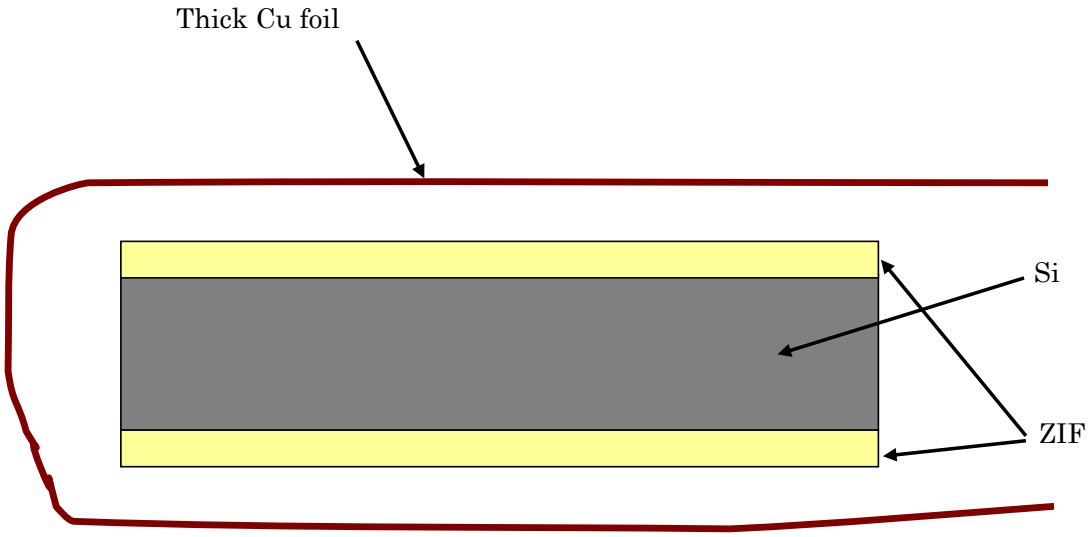



**Figure 56. Schematic drawing of setup for vacuum lamination**

After double-side lamination, a short hot press cycle was performed at 120℃ with 1 ton force for better planarity by eliminating any dimples resulting from the filling process. The schematic setup used for the hot press process is shown in Figure 57 and the stack was carefully designed to prevent any cracking of the brittle silicon during the process.

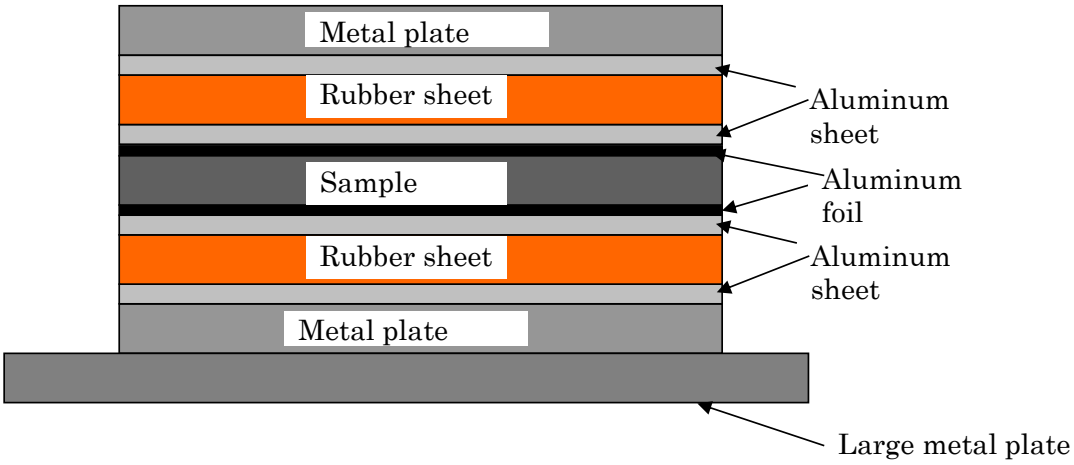



**Figure 57. Schematic drawing of stack-up for hot-press**

A thermal cure was required to complete the polymerization reactions at 180℃ for 30 minutes. The temperature profile for the ZIF curing is shown in Figure 58. The mechanism can be explained as follows: Upon exposure to heat, the interaction of reactive oligomer groups occurs. This results in the decrease of viscosity, cross-linking of polymer chains and thus toughening of the polymer.

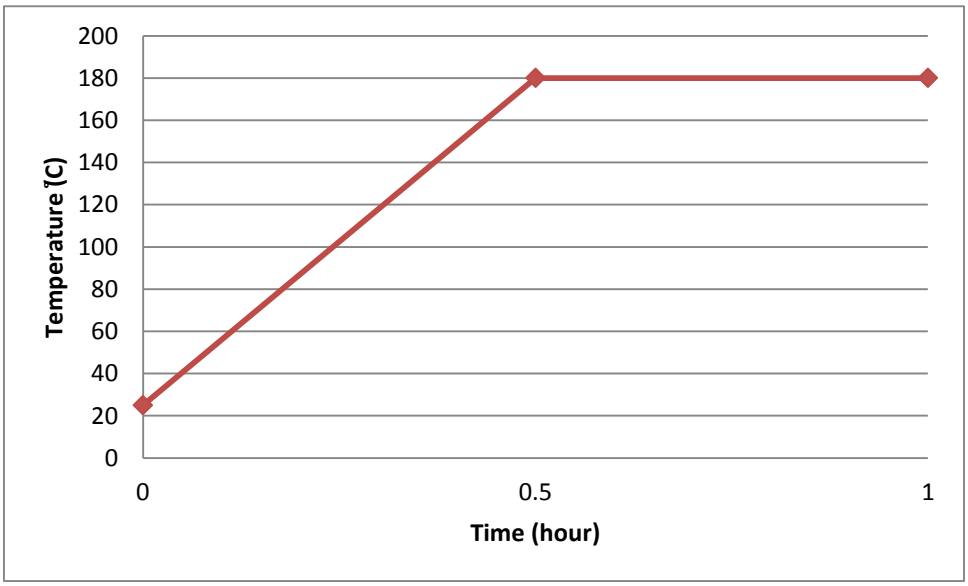



**Figure 58. Thermal profile for ZIF polymer curing**

Adhesion between polymer and silicon was measured qualitatively after curing by IPC standard tape test [78] for peel strength and the samples showed good adhesion.

4.3.3.3 Laser Ablation in Polymer

The last step in the thick liner formation by double laser method involved the laser ablation of a smaller diameter through hole in the polymer filling the TPVs. In this step, the absorption of the UV laser photons resulted in direct bond breaking, enabling laser ablation of the polymer with minimum heat affected zones (HAZ). This is especially important for silicon TPVs since the bulk silicon material has a very high thermal conductivity. Precise alignment of the laser beam to the TPV locations was necessary to ensure that the ablation process happened in the center of the vias in silicon and to maintain sufficient polymer liner thickness on the side walls. Furthermore, by customizing the beam size of the laser system, it was possible to control the thickness of the polymer liner on the via sidewalls.

## 4.4 TPV Metallization

Metallization of the TPVs with copper was required to complete electrical interconnections from top side to bottom side for connecting components to each other and to the system board. The metallization process consisted of two steps: 1) double-side electroless plating for Cu seed in TPVs that is scalable to high throughput on large panels, as opposed to vacuum-based sputtering used for TSVs, and 2) electrolytic Cu plating. This section summarizes the key steps and mechanisms for both processes.

### 4.4.1 Cu Electroless Plating

Electroless plating forms a thin layer of seed (usually 100 nm-1 μm) on the non-conductive polymer liner to provide electrical conductivity and allow the TPVs to be electrolytically plated to final thickness thereafter. Unlike electroplating, electroless plating uses chemical reactions to deposit metal on the surface without any external electrical source. Prior to the electroless plating, a desmear process was necessary to treat the polymer surface. Such a step roughens the smooth surfaces of the polymer to improve adhesion between Cu and the polymer liner. Cu electroless plating was done by reducing complexed copper with formaldehyde in an alkaline solution. The reaction was catalyzed by palladium, which was deposited on the surface in a previous activation step. The Cu electroless plating process is governed by the reaction formula:

$$CuSO_4 + 2HCHO + 4NaOH \xrightarrow{Pd} Cu + 2HCO_2Na + H_2 + 2H_2O + Na_2SO_4 \qquad (17)$$

For the ZIF polymer, the desmear process was divided into a few steps, as illustrated in Figure 59, including Sweller (swelling of polymer), Permanganate ($KMnO_4$ to etch polymer surface to increase roughness) and Reducer (remove residue of permanganate).

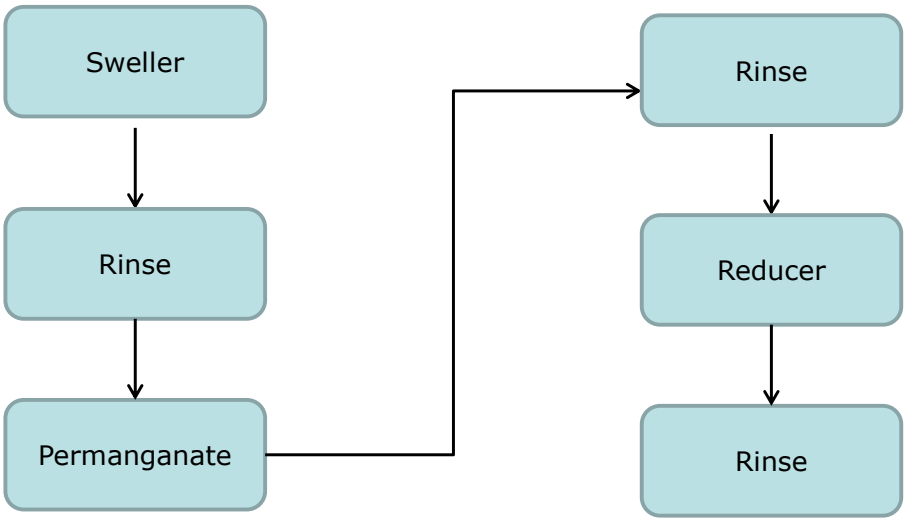



**Figure 59. Detailed steps for Desmear process**

The thin Cu seed layer was deposited by electroless plating, and the process steps are summarized in Figure 60. Conditioning and pre-dip steps cleaned the polymer surface by removing any residues and prepared the surfaces for the catalyst deposition. Then the palladium catalyst was formed on the surface and sidewall liners during the activation process and acted as activation sites for the subsequent electroless Cu plating by reducing Cu ions. The last step, acid dip, was to clean the copper surfaces prior to electrolytic plating.

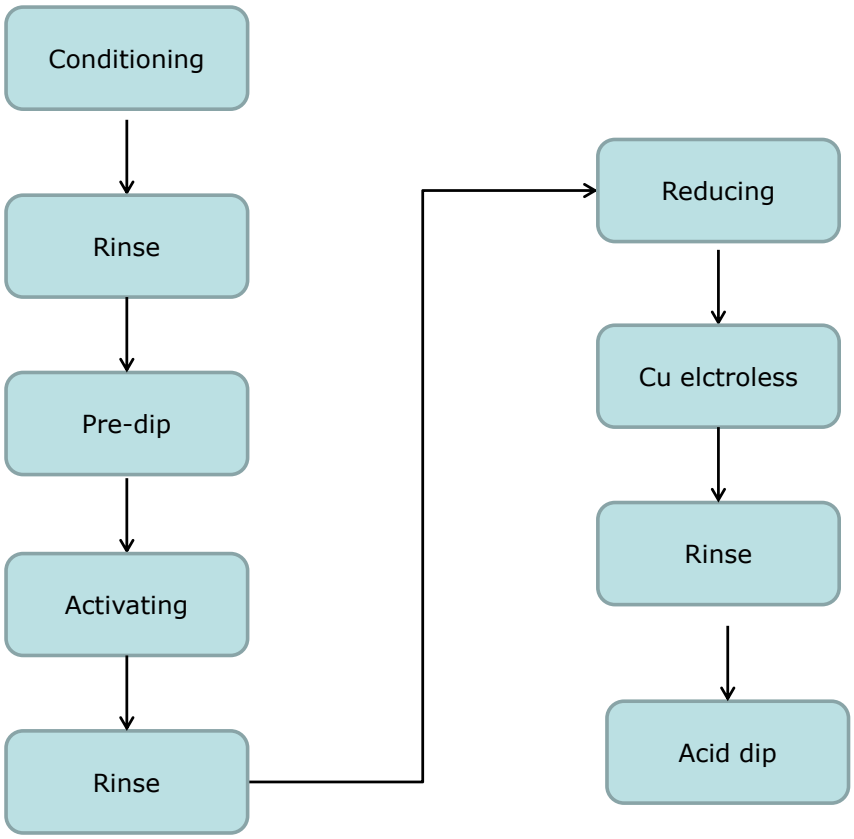



**Figure 60. Detailed steps for electroless Cu plating**

Peel strengths of greater than 0.7 kN/m have been demonstrated in prior work on copper metallization of ZIF polymer [75]. The mechanism of adhesion for such a process is illustrated in Figure 61 [79]. During the electroless plating process, micro-phase interaction occurs between the plated Cu and epoxy resin sites in the polymer. Such reactions form Cu and resin mixture layers, which greatly improves the adhesion between the electroless Cu seed and the ZIF polymer liner.

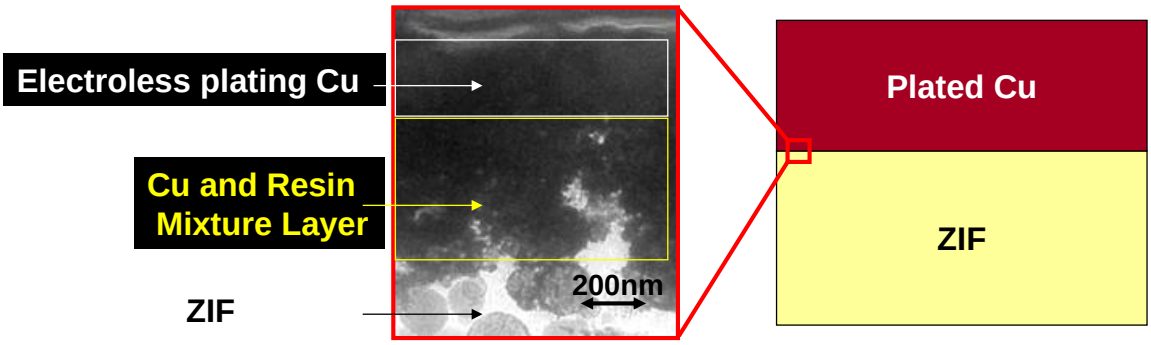



**Figure 61. Cross-section of interface between electroless plated Cu and ZIF [79]**

### 4.4.2 Cu Electrolytic Plating

Cu electrolytic plating is the most widely used technique for through via filling. Electrolytic plating uses current for metal cations to dissolve and form a metal layer on the conducting surface. A typical setup for Cu electrolytic plating is shown in Figure 62. The plating tank includes $CuSO_4$, $H_2SO_4$ and organic additives, such as brightener and leveler. As the direct current is applied, the cathode (silicon panel) is rich in negative charge, and positively charged Cu cations tend to migrate towards the cathode, and are reduced to Cu to fill the TPVs. The reaction at the cathode can be written as:

$$Cu^{2+} + 2e^{-} \longrightarrow Cu \qquad (18)$$

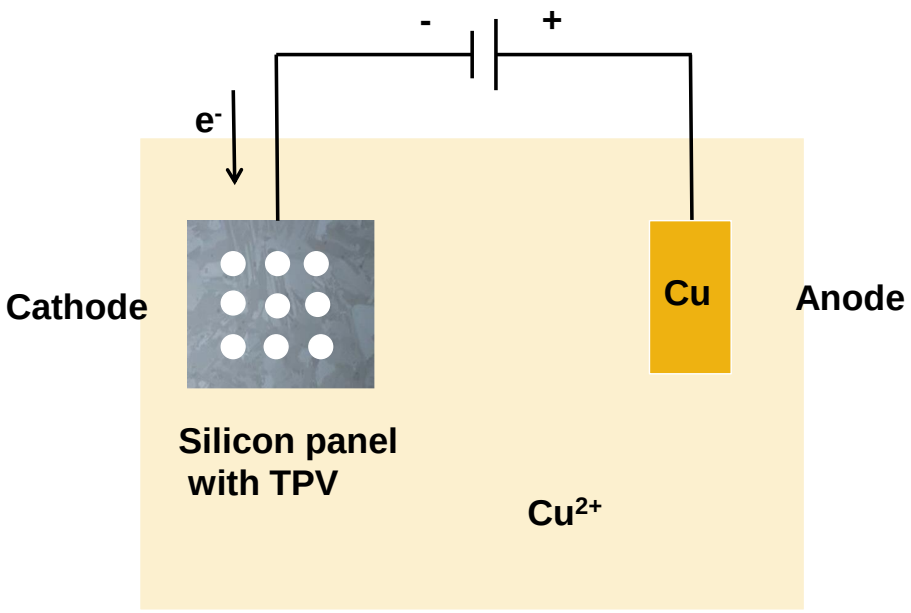



**Figure 62. Schematic drawing of Cu electrolytic plating system**

The thickness of Cu plated is governed by the equation:

$$h = i * A * t \tag{19}$$

where $h$ is the plated thickness, $i$ is the current density, $A$ is the plating surface area and $t$ is the plating time. The current density is usually presented with the unit ASD or Amperes per Square Decimeter. Current densities of 1~3 ASD are used to ensure high quality plating. In our study, a current density of 2 ASD was applied for smooth Cu plated surfaces. During the plating process, the sample surface was checked at 30-minute intervals using a stylus profilometer to verify the plated Cu thickness and avoid over-plating. The cross-section of the conformally plated TPVs is shown in Figure 63. Good silicon-to-liner and liner-to-Cu adhesion was confirmed, without any interfacial failures.

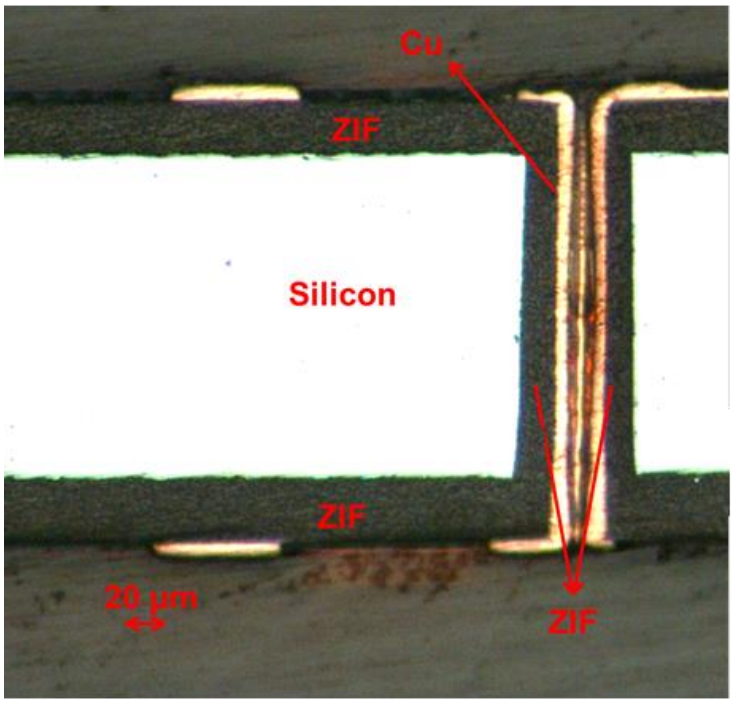



**Figure 63. Optical cross-section image of metalized TPV with ZIF liner**

## 4.5 Summary

**a. Fracture strength of polycrystalline silicon panel**

- Fracture strength of polycrystalline silicon panel has been fundamentally studied with four-point bending tool and Weibull plot.
- Surface polymer liners on both sides were introduced to improve the handling of thin silicon panels. Quantitative study showed higher characteristic fracture strength for the panel with surface liners than raw silicon panel. Thicker liner helps further strengthen the panel.

**b. TPV formation**

- Laser ablation is used for TPV formation due to its higher throughput and simpler steps than Bosch process.

- Crystalline-silicon presents high absorption of light with 200 nm to 400 nm wavelength. Hence, three types of lasers, involving 355 nm picosecond lasers, 248 nm excimer lasers and 355 nm UV lasers, were explored.
- UV laser was selected with comprehensive consideration of via quality, throughput and cost. Via tapering effect due to percussion drilling method was also analyzed.

**c. TPV liner fabrication**

- Three processes, spray coating, ED and double laser method, were studied for liner formation. Spray coating and ED, however, suffer from poor edge coverage and non-uniformity respectively. To address the issues of spray coating and ED, double laser method has been developed, including two laser steps to achieve polymer-lined TPV from as-cut silicon panel. The technical approach for the liner formation involves polymer filling in TPVs followed by laser ablation to form an "inner" via,
- ZIF polymer was used as the liner material due to its low electrical loss, high insulation reliability, low modulus for stress buffer, high flow for ease of via filling, and high absorption of laser irradiation for efficient ablation. Such material was selected based on the design guidelines discussed in Chapter 3 and the nature of double laser method.
- Silane treatment was used to improve the adhesion between silicon and polymer during TPV filling and the mechanism has been studied with

SEM and EDS for both the silicon surface and TPV sidewall. The mechanism of laser ablation in polymer has also been analyzed.

- Key process steps for double laser method were introduced, including vacuum lamination to form surface liners and TPV filling, hot process for better planarization, and curing for complete polymerization. Qualitative tape test confirmed good adhesion between polymer and silicon.

**c. TPV metallization**

- Low cost Cu electroless plating was used for seed layer formation to replace sputtering. Process details for desmear to roughen the liner surface and electroless plating to deposit thin Cu layer were discussed. The mechanism of adhesion between Cu and ZIF was also summarized.
- Cu electrolyte plating was used for TPV filling. The cross-section image of metalized TPV showed good adhesion at Si-Liner interface and Liner-Cu interface.

# CHAPTER 5

# ELECTRICAL AND RELIABILITY CHARACTERIZATION OF TPVS IN POLYCRYSTALLINE SILICON INTERPOSERS

In the previous two chapters, the modeling, design and demonstration of TPVs in polycrystalline silicon panels were investigated. Considering the design guidelines from Chapter 3 as well as the mechanism and analysis of TPV and liner formation in Chapter 4, this chapter discusses the integration of TPV and re-distribution layers (RDL) to form polycrystalline silicon interposers, ready for assembly to ICs and boards. The design and fabrication of both electrical and reliability test vehicles are discussed. High frequency electrical characterization results are presented and correlated with the electromagnetic simulation results. The reliability test vehicles were subjected to thermal cycling tests, and the resistance of the daisy chain structures was monitored. Reliability samples were analyzed by micro-sectioning and imaging by SEM.

## 5.1 Electrical Test Vehicles with TPVs*

This section discusses the design, fabrication and characterization of electrical test vehicles. Two types of test vehicles, one with two metal RDLs and the other with four metal RDLs, were designed and fabricated. The insertion loss of test structures, including co-planar waveguide (CPW) transmission lines and CPW-TPV transitions, were measured at high frequencies.

*In collaboration with Gokul Kumar and Tapobrata Bandyopadhyay from GT-PRC

### 5.1.1 Electrical Test Vehicles with TPVs and Two Metal RDLs

#### 5.1.1.1 Design of Test Vehicles

The snapshot of the mask design is shown in Figure 64. Both long CPW lines (Figure 65(a)) with different lengths as well as CPW-TPV transitions (Figure 65(b)) were designed based on EM modeling and simulations. The critical design parameters used are listed in Table 11. The test vehicle was built on a 200 μm thick polycrystalline silicon panels with resistivity of 0.5 Ω-cm. The TPV diameter was 80 μm and the Cu-filled inner via diameter was 50 μm, resulting in a liner thickness of 15 μm on the TPV sidewalls. The thickness of the surface liners was 40 μm. CPW lines with lengths of 6.2 mm and 11.2 mm were designed with line widths of 160 μm and signal-to-ground gaps of 36.5μm. CPW-TPV structures, on the other hand, consisted of 0.5 mm, 1 mm and 1.5 mm long line segments and varying numbers of TPV transitions.

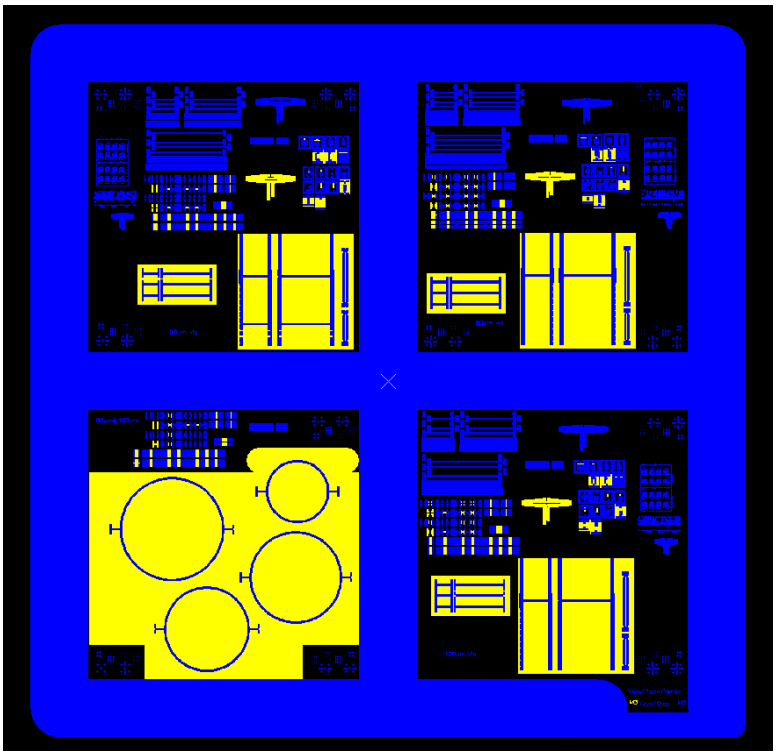
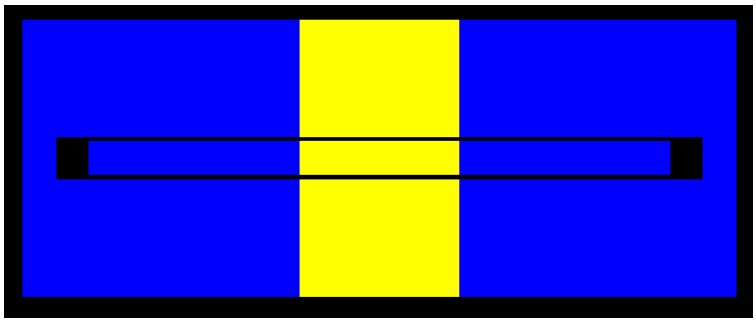


**Figure 64. Snapshot of the mask for electrical test vehicle with two metal RDLs**

(a)



(b)

**Figure 65. Snapshot of designed (a) CPW lines and (b) CPW-TPV structure with two transitions**

**Table 11. Parameters for electrical test vehicle with TPV and two metal RDLs**

| Parameters | Value |
|---|---|
| Substrate thickness | 200 μm |
| Substrate resistivity | 0.5 Ω-cm |
| TPV diameter | 80 μm |
| Cu-filled via diameter | 50 μm |
| Liner material | ZIF |
| Sidewall liner thickness | 15 μm |
| Surface liner thickness | 40 μm |
| CPW line length | 6.2 mm, 11.2 mm |
| CPW line width/gap | 160 μm/36.5 μm |
| CPW-TPV line length | 0.5 mm, 1 mm, 1.5 mm |
| CPW-TPV transition | 2, 4, 6 |

5.1.1.2 Fabrication of Test Vehicles

The process flow for fabricating the electrical test vehicle is shown in Figure 66. The process combined the key TPV formation and metallization steps discussed in Chapter 4 with double-side RDL fabrication.

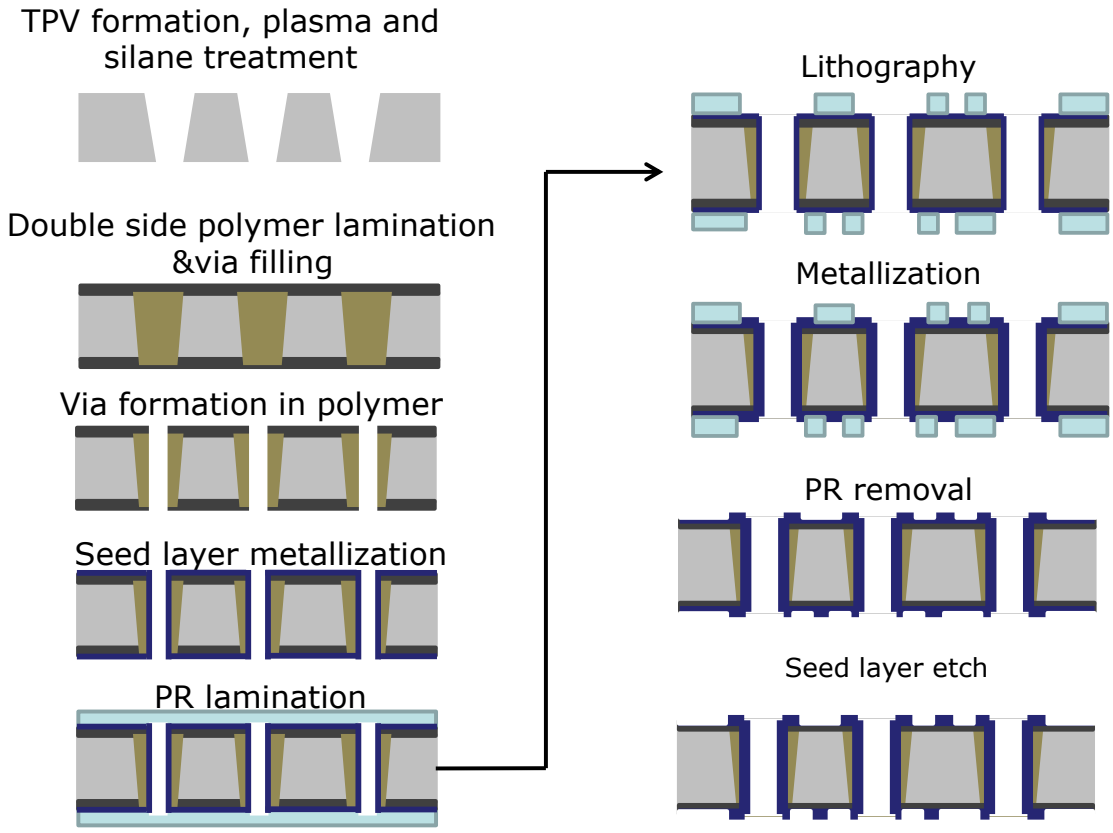



**Figure 66. Process flow for electrical test vehicle with TPVs and two metal RDLs**

The process started with the cleaning of 150 mm as-cut polycrystalline silicon panels with acetone, methanol, isopropanol and DI (deionized) water. Then TPVs were drilled by 355 nm UV laser ablation with via entrance diameters of 80 μm. The RF (radio frequency) plasma treatment was then carried out on the substrate. This step aimed to remove impurities and provide OH groups for the subsequent silane treatment as discussed in the previous chapter. ZIF polymer dry films were laminated on both sides to insulate the surface and fill the via. This step was achieved using a vacuum laminator at 95℃. A planarization step was added using a hot press, followed by thermal curing of the polymer. Then a second UV laser ablation process step was applied to remove the

polymer from the center of the vias to form TPV sidewall liners. The TPV metallization and RDL fabrication required an electroless copper plated seed layer, prior to which a chemical desmear process was done to roughen the polymer liner surface and improve Cu-to-polymer adhesion.

The panel was then patterned by a double-sided lithography process. This process consisted of several steps, starting with dry-film photoresist lamination using a hot roll laminator, followed by UV exposure and photoresist development by dilute sodium carbonate solution in a spray tool. Copper electrolytic plating using a semi-additive process (SAP) method was carried out, and the current density as well as the plating time was adjusted to control the final Cu thickness. The photoresist was then stripped by potassium hydroxide and the Cu seed layer was etched by dilute $CuCl_2$ solution based on the following reaction:

$$CuCl_2 + Cu \longrightarrow 2CuCl \tag{20}$$

The top view of one completed 150 mm by 150 mm size polycrystalline silicon interposer test vehicle with TPVs and two metal RDLs is shown in Figure 67.

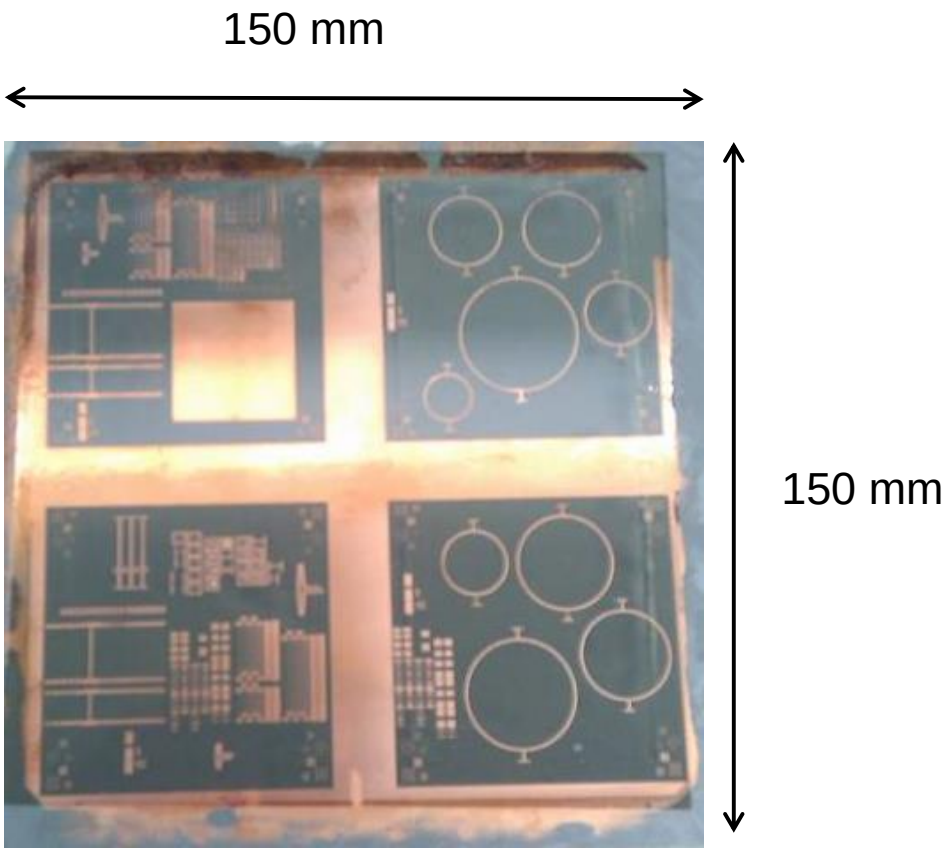



**Figure 67. Top view of the electrical test vehicle with TPVs and two metal RDLs**

5.1.1.3 Characterization of Test Vehicles

High frequency characterization of the test vehicles was performed up to 10 GHz using ground-signal-ground (GSG) probes and a Vector Network Analyzer (VNA), after short-open-load-through (SOLT) calibration, as shown in Figure 68.

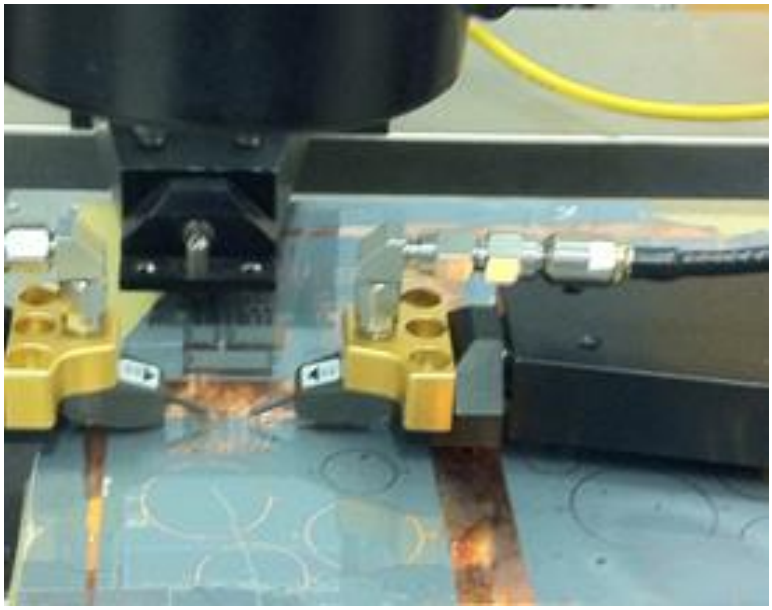


**Figure 68. High frequency measurement for polycrystalline silicon interposer**

Figure 69 shows the insertion loss measurements for both 6.2 mm and 11.2 mm CPW traces without vias. It can be observed that the 6.2 mm and 11.2 mm transmission lines had less than 1.5 dB and less than 2.5 dB insertion loss respectively at 10 GHz. The unit loss can be simply calculated as:

$$IL_{unit} = \frac{IL_{trace}}{l} \tag{21}$$

where $IL_{unit}$ is the unit insertion loss, $IL_{trace}$ is the insertion loss of the trace and $l$ is the length of the line. This translates to a loss of 0.22-0.24 dB/mm at 10 GHz. The insertion loss in the transmission lines on polycrystalline silicon interposer were much lower than published values of loss for TSV interposers with thin oxide liners [80], in spite of the much lower resistivity of the upgraded metallurgical grade silicon, primarily due to the thick polymer insulating liners on the surface of the silicon panel.

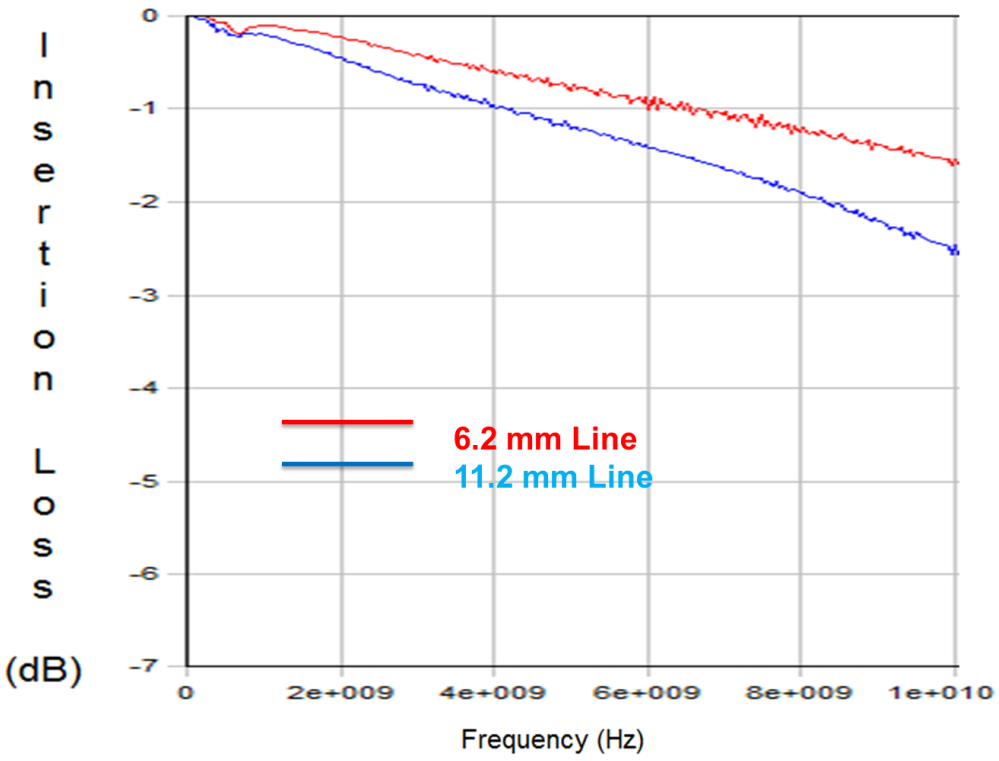



**Figure 69. Insertion loss measurements for CPW lines with different lengths**

The insertion loss of the CPW-TPV structures with two transitions in the two-metal layer test vehicles is plotted in Figure 70 with signal lines of different lengths. The impact of the transmission line length on the insertion loss was studied. The results showed that the insertion loss increased with larger signal length, but the total impact of the length increase on the insertion loss at lower frequencies was negligible. Thus, local routing can be performed in the interposer between signal TPVs without significant impact on the signal integrity.

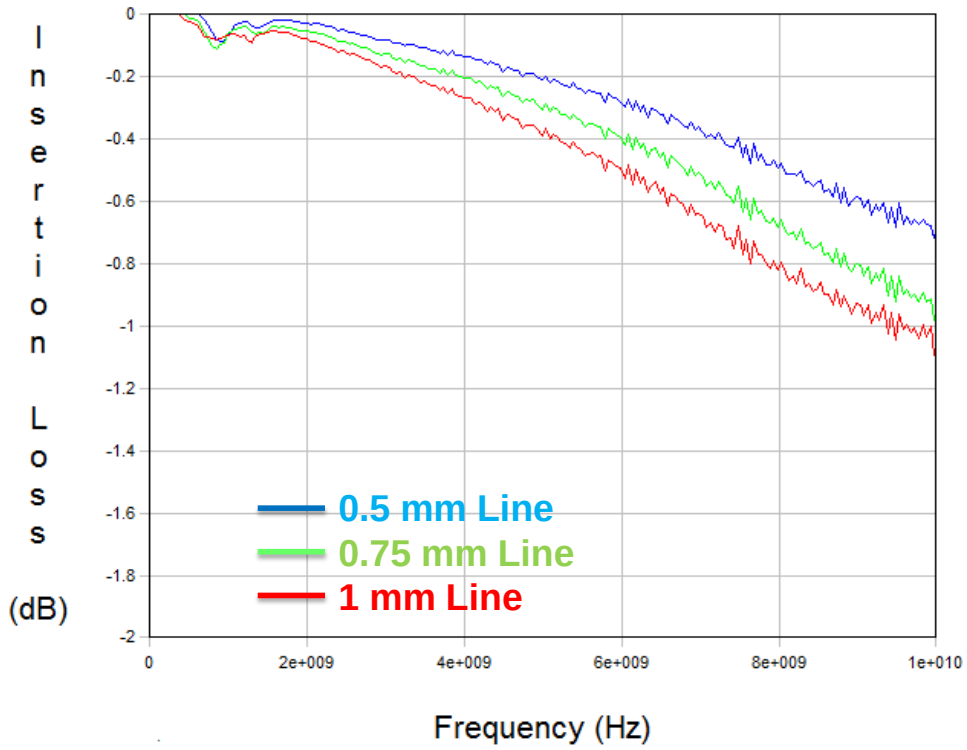



**Figure 70. Insertion loss measurements for CPW-TPV transitions with different trace length**

The insertion loss of a single TPV at 10 GHz was extracted based on Figure 69, Figure 70, and with the equation:

$$IL_{TPV} = \frac{IL_{transition} - IL_{unit} \times l}{n} \tag{22}$$

where, $IL_{TPV}$ is the insertion loss of single TPV, $IL_{transition}$ is the total loss for CPW-TPV transition, $IL_{unit}$ is the unit insertion loss, $l$ is the total length for CPW traces in the transition, and $n$ is number of TPVs in the transition. In the case of 0.5 mm long CPW lines, the total length of CPW traces was 1.5 mm in the CPW-TPV structures in Figure 71. With the loss per unit length of 0.23 dB/mm (average value of the unit loss for two lines in Figure 69) and the total loss of 0.7 dB (read from Figure 70), the insertion loss of

a single TPV was calculated to be approximately 0.1775 dB. This value is much smaller than the reported [43-45] value of 1-2 dB per TSV (200-350 μm height, 60 μm Cu-filled via diameter) with 15 Ω-cm single-crystalline silicon and 1.5 μm thick $SiO_2$. This is due to the low loss and thick insulation sidewall liner, which greatly reduces the TPV capacitance and thus improve the electrical performance.

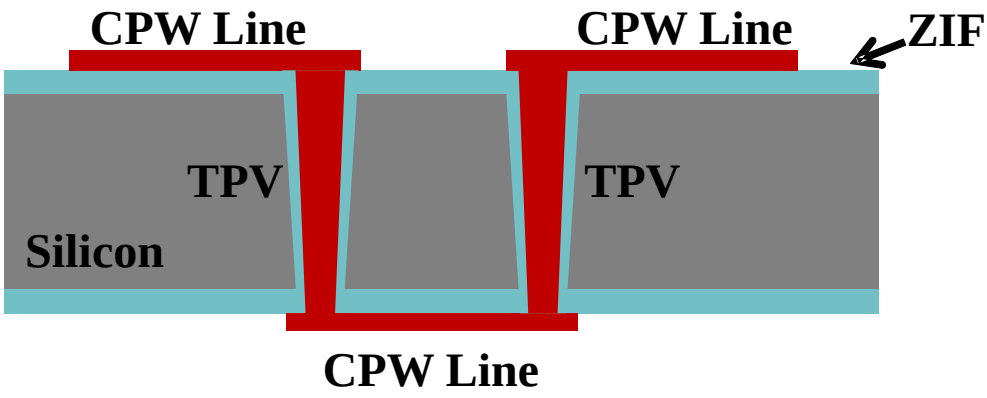



**Figure 71. Schematic cross-section drawing of CPW-TPV transition (2 transitions)**

The insertion loss of CPW-TPV structures with different numbers of via transitions is shown in Figure 72, where the CPW trace length was fixed at 1 mm. As expected, the insertion loss tended to increase with the number of transitions, due to the additional loss from the CPW traces and TPVs.

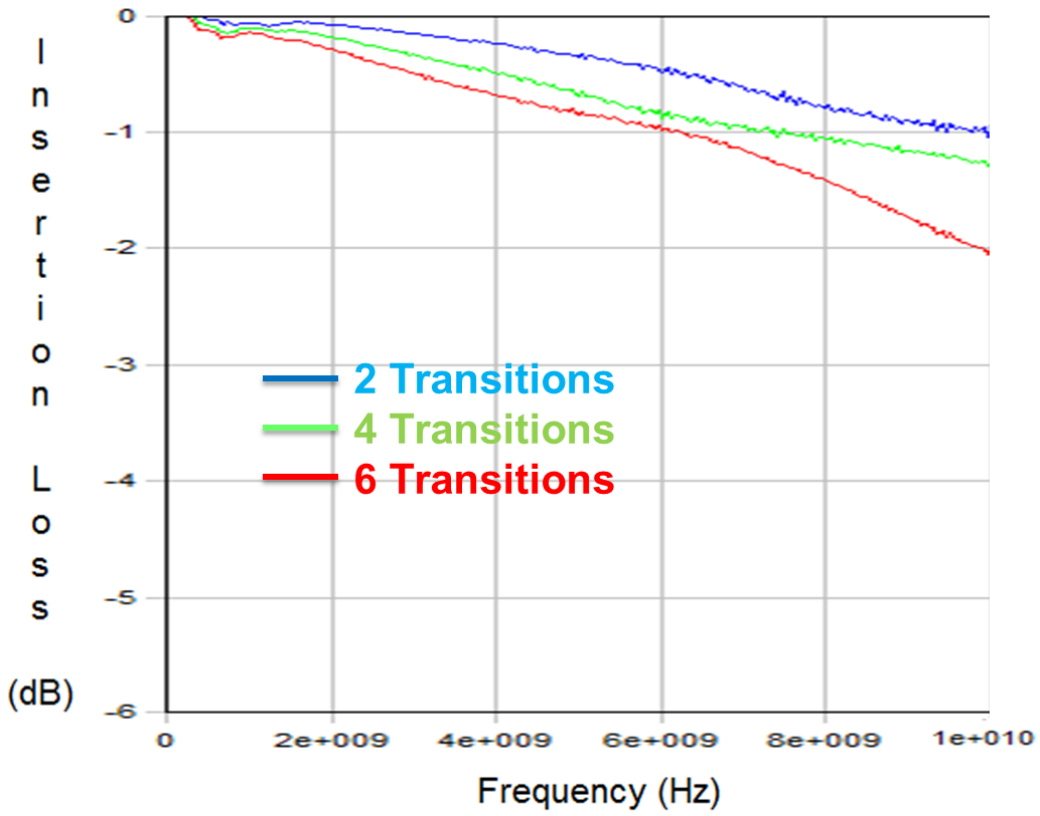



**Figure 72. Insertion loss measurements for CPW-TPV structures with different numbers of transitions**

### 5.1.2 Electrical Test Vehicles with Four Metal RDLs

5.1.2.1 Design and Fabrication of Test Vehicles

To demonstrate polycrystalline silicon interposers with multi-layer interconnections, test vehicles with four metal RDLs were designed and fabricated. Compared to the test vehicles discussed in 5.1.1 with two metal RDLs (M1 and M2), the new test vehicles added two more layers (M3 and M4), which are connected to the internal metal layers (M3 to M1 and M4 to M2) by micro-vias in polymer dielectric films. A snapshot of the completed mask layout is shown in Figure 73. This new design shared the same guidelines listed in Table 11, and ZIF dry film polymers (17.5 μm thick)

were used as the build-up layers. Both 2ML (metal layer) test structures, similar to those shown in Figure 65, and 4ML structures were included in this design.

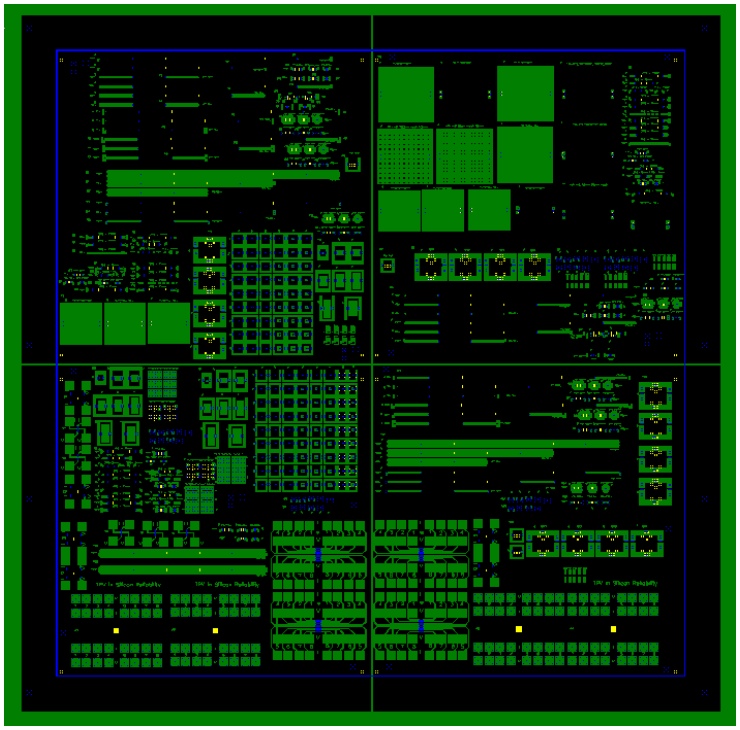


**Figure 73. Snapshot of mask design for electrical test vehicle with four metal RDLs**

The fabrication process for the test vehicles with four metal RDLs consisted of two major process segments. The first segment was TPV formation, liner formation and TPV and two metal layer metallization by SAP (Semi-additive plating) method, identical to the process flow shown in Figure 66. After the 2ML process was completed, the insertion loss of CPW traces and CPW-TPV transitions was measured and the results will be analyzed in 5.1.2.2. The second segment consisted of the process to form the two additional metal layers and is illustrated in Figure 74.

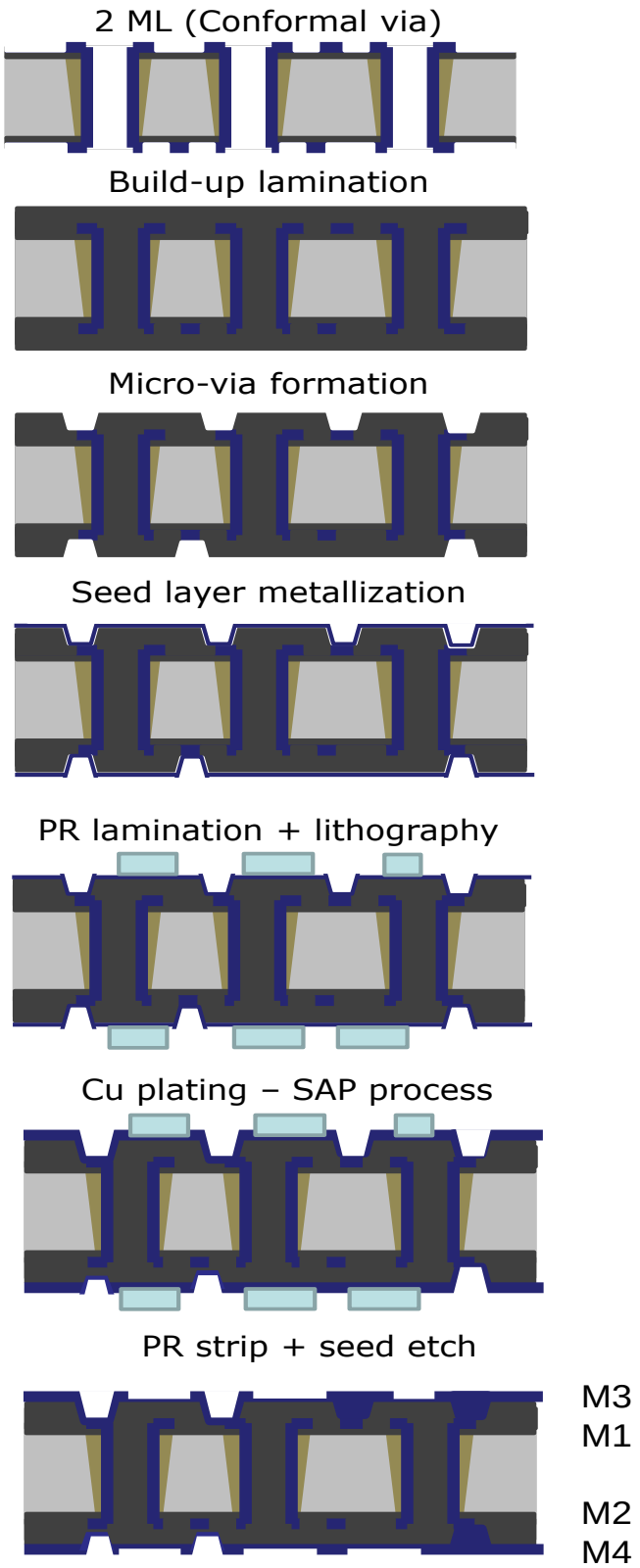



**Figure 74. Process flow for test vehicles with 4-metal RDLs (segment 2)**

At first, two build-up polymer dielectric layers (ZIF) were formed on the 2ML structures by double-side vacuum lamination processes. Then, 355 nm UV laser ablation was used to form blind micro-vias in the cured polymer dielectrics for vertical interconnections. The micro-vias and build-up layers were coated with a 1 μm thick electroless plated Cu seed layer, followed by semi-additive electrolytic copper plating using double-side dry film photoresist lamination and UV lithography processes. The final steps included photoresist removal by KOH solution and Cu seed layer etching by $CuCl_2$ solution. Figure 75 shows the top view of the completed 150 mm by 150 mm size polycrystalline silicon panel with TPVs and four metal RDLs. The micro-section photograph of the four-metal layer interposer is shown in Figure 76.

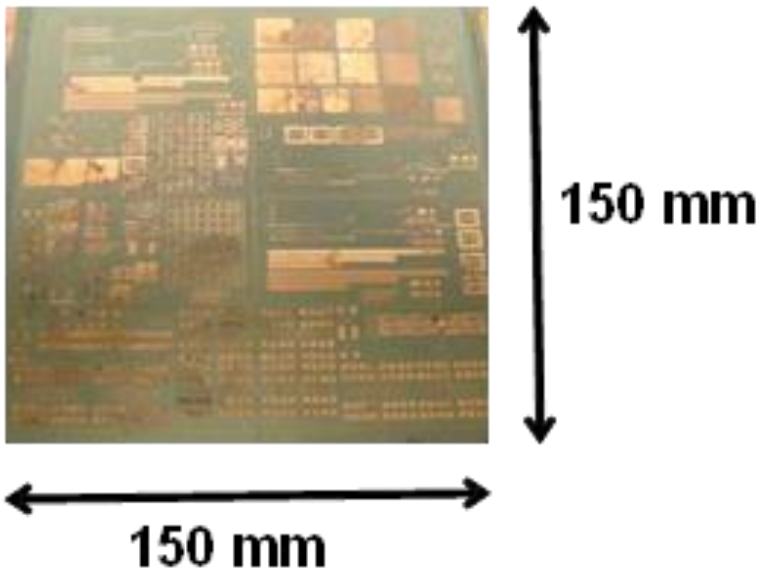



**Figure 75. Top view for polycrystalline silicon interposer with TPVs and four metal RDLs**

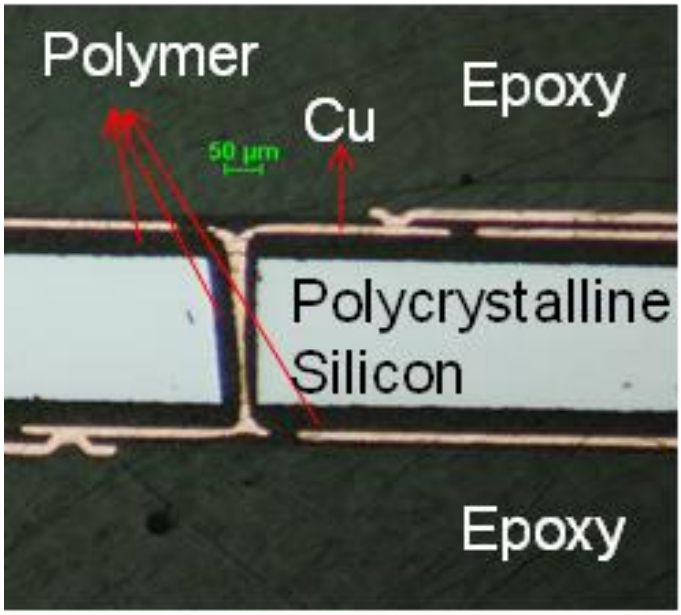



**Figure 76. Optical image of cross-section for polycrystalline silicon interposer with TPVs and four metal RDLs**

5.1.2.2 Characterization of Test Vehicles

As mentioned in 5.1.2.1, after the 2ML structures were fabricated, high frequency measurements up to 10 GHz were performed and the results are presented in Figure 77 and Figure 78. It can be concluded that both CPW lines and CPW-TPV transitions presented low insertion loss, consistent with the measurements from the two metal layer test vehicles. Good model to hardware correlation was also observed.

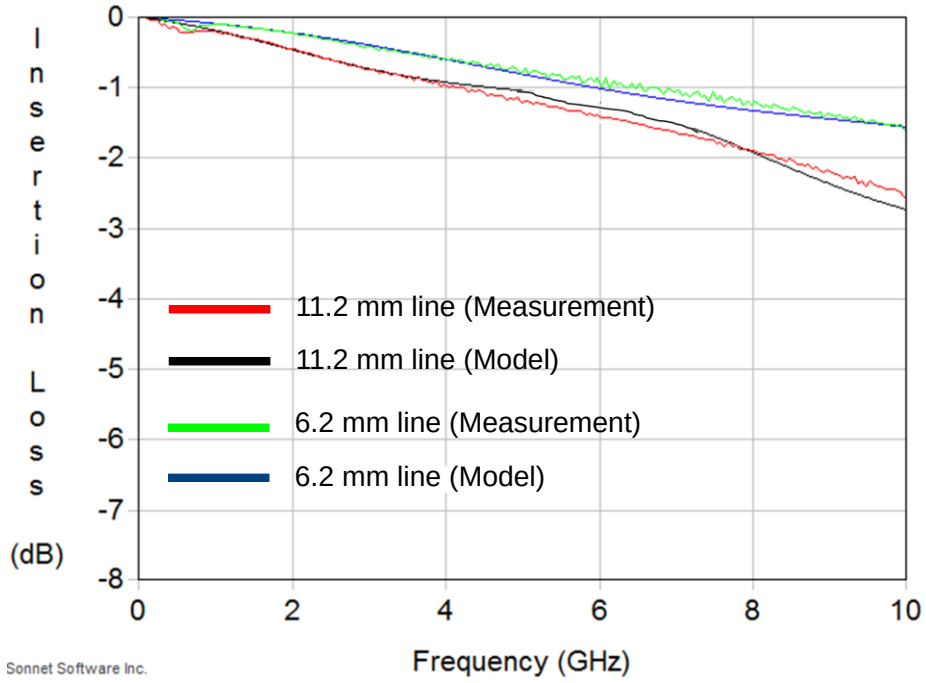



**Figure 77. Simulation and test results of Insertion loss for CPW lines**

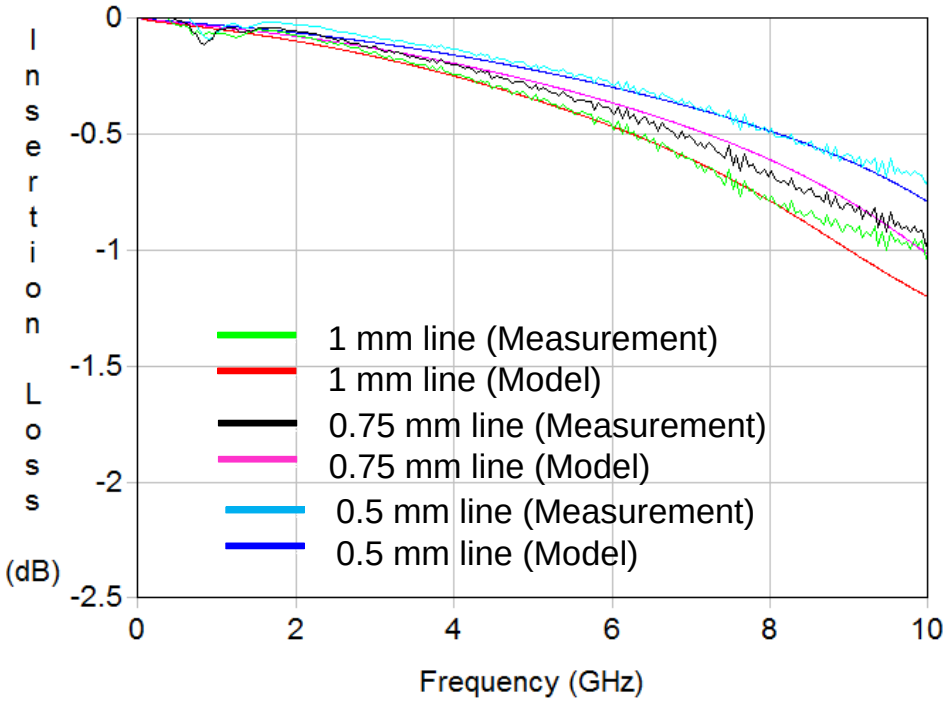



**Figure 78. Simulation and test results of Insertion loss for CPW-TPV transitions**

After fabrication of silicon interposers with four metal RDLs, the electrical performance of CPW lines and via transitions in structures with up to four metal layers was also characterized and insertion loss results up to 10 GHz are plotted in Figure 79. The length of the CPW line was fixed at 1 mm. As shown in Figure 79, the one-metal layer structures consisted of only the transmission lines on the top metal layer, while the two-metal layer structures included blind vias to transfer the signals to the second metal layer. Both the three-metal layer and four-metal layer structures included TPVs to connect the lines to the metal layers on the bottom side of the silicon. These measurements showed that the insertion loss increased with frequency, and with the number of metal layers. This is due to the added loss coming from the vertical micro-via transitions. The overall loss was low and remained below 0.9 dB at 2.4 GHz for the four-metal layer structures. This result indicates that multiple signal layer escape routing is possible due to the excellent isolation of the thick polymers to achieve low loss and high performance panel-based polycrystalline silicon interposers.

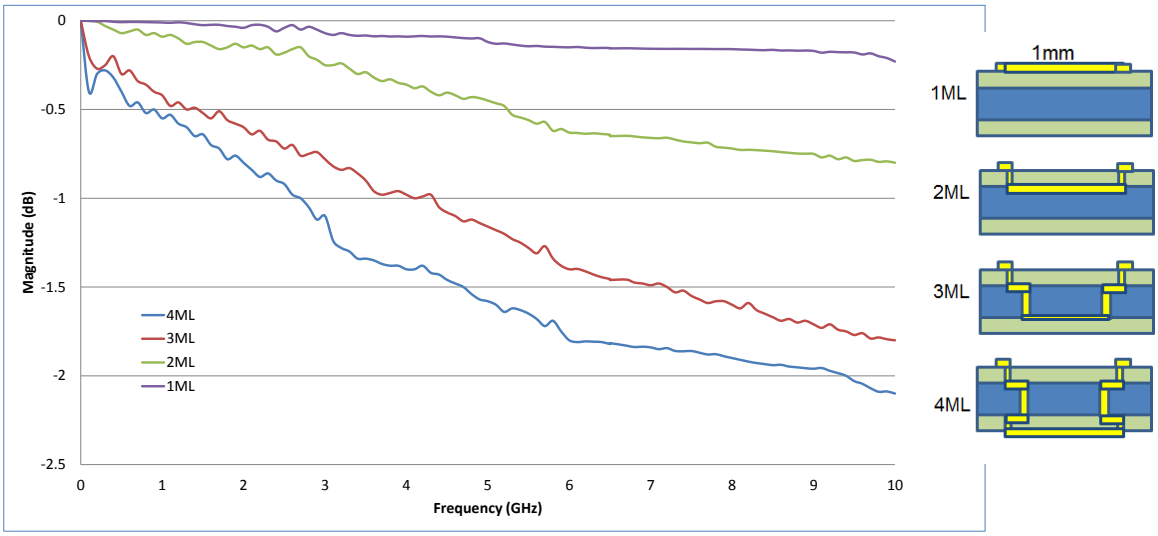



**Figure 79. Measurements of insertion loss in CPW lines, TPVs and blind via transitions in structures with different numbers of metal layers**

## 5.2 Reliability Test Vehicles with TPVs

Reliability test vehicles were designed and fabricated to evaluate the thermo-mechanical stability of TPVs in polycrystalline silicon interposers. These test vehicles consisted of two metal layers and TPV transitions with daisy chain structures. In addition, four-point probe pads (Kelvin structures) were included in the design and resistance monitoring was carried out for daisy chains during the thermal cycling tests. Scanning Electron Microscopy imaging was conducted to analyze the samples.

### 5.2.1 Design and Fabrication of Test Vehicles

The four-point probe method, or Kelvin method [81], as depicted schematically in Figure 80, involved the use of both an ammeter and a voltmeter. Because of the voltmeter's high resistance, the inner loop ideally does not draw any current, leading to a voltage reading that is nearly the same as if it were connected directly across the subject

resistance. Hence this method is able to exclude any errors from probe contact resistances and wire resistances. And the resistance of the device under test (DUT) can be simply written as:

$$R_{chain} = \frac{Voltmeter\ Indication}{Ammeter\ Indication} \tag{23}$$

where $R_{chain}$ is the resistance of the daisy chain.

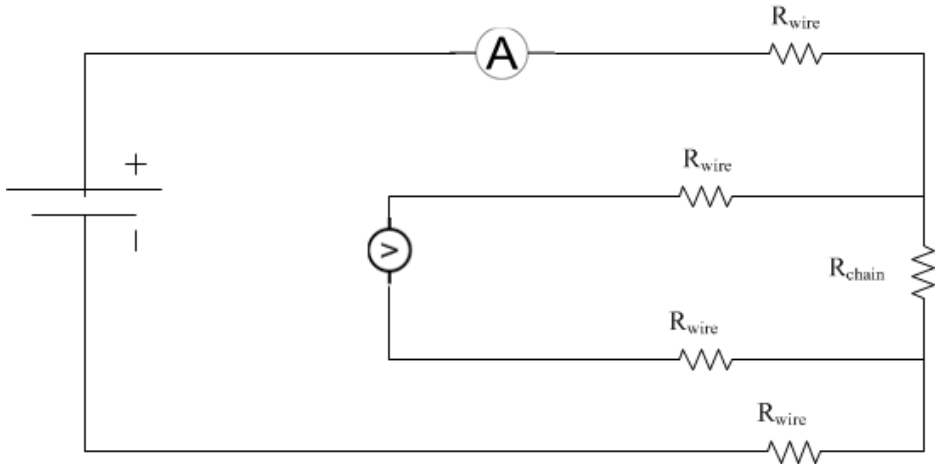



**Figure 80. Schematic circuit drawing for four-point probe method**

A snapshot of the designed test structures in final panelized form is shown in Figure 81, and the design parameters are listed in Table 12. The fabrication process was identical to that described in the previous section on electrical test vehicles with TPVs and two metal layers, as shown in Figure 66. The top view of the fabricated test structures is shown in Figure 82.

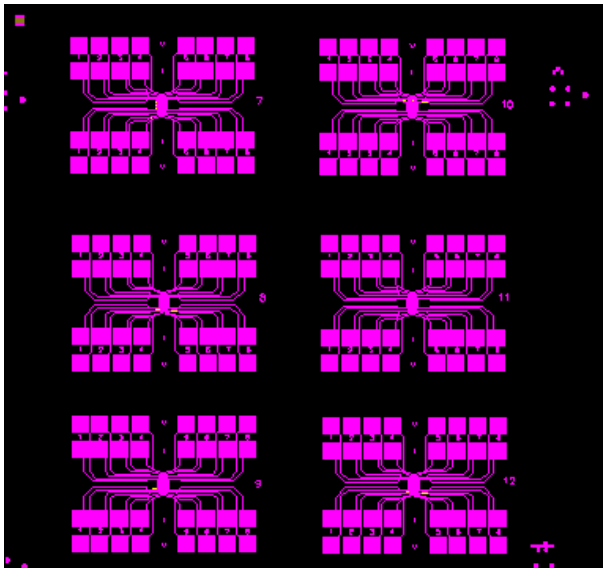


**Figure 81. Snapshot of the designed test structures**

**Table 12. Parameters for reliability test vehicle**

| Parameters | Value |
|---|---|
| Substrate thickness | 200 µm |
| TPV diameter | 80 µm |
| Cu-filled via diameter | 50 µm |
| Via pitch | 150 µm |
| Liner material | ZIF |
| Sidewall liner thickness | 15 µm |

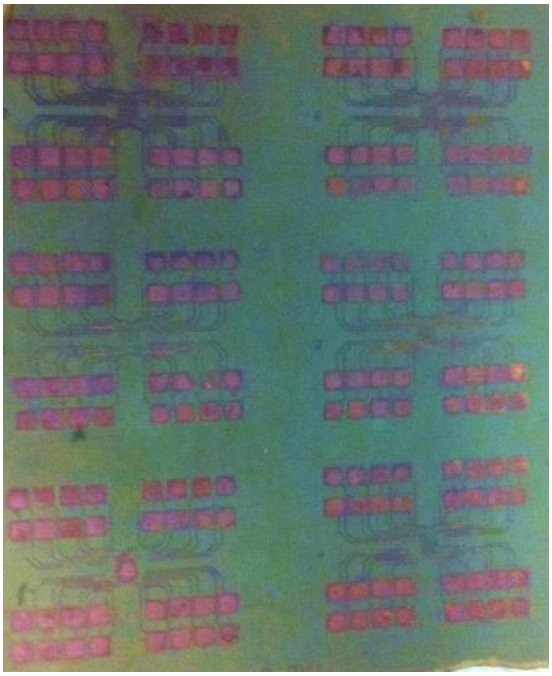


**Figure 82. Top view of fabricated test structures**

### 5.2.2 Thermal Cycling Tests and Resistance Measurement

The test vehicles were first subjected to a 24-hour bake at 125 ℃, followed by accelerated moisture sensitivity level 3 (MSL-3) preconditioning (60 ℃, 60% RH for 40 hours), and three times reflow at a peak temperature of 260 ℃, to simulate the lead-free board assembly processes. The test vehicles were then subjected to thermal cycles between -55 ℃ and 125 ℃ with a dwell-time of 15 minutes at each temperature extreme as described in JEDEC JESD22-A104 condition B test standard. The samples were taken out at 100, 200, 500 cycles, and every 500 cycles thereafter, and the daisy chain resistances were measured to detect TPV failures, as shown in Figure 83. No significant resistance changes were observed during the test. All the TPV daisy chains survived 4000

thermal shock cycles with a stable resistance value of 0.17 ohms, confirming the thermo-mechanical reliability of TPVs and RDLs in polycrystalline silicon interposers.

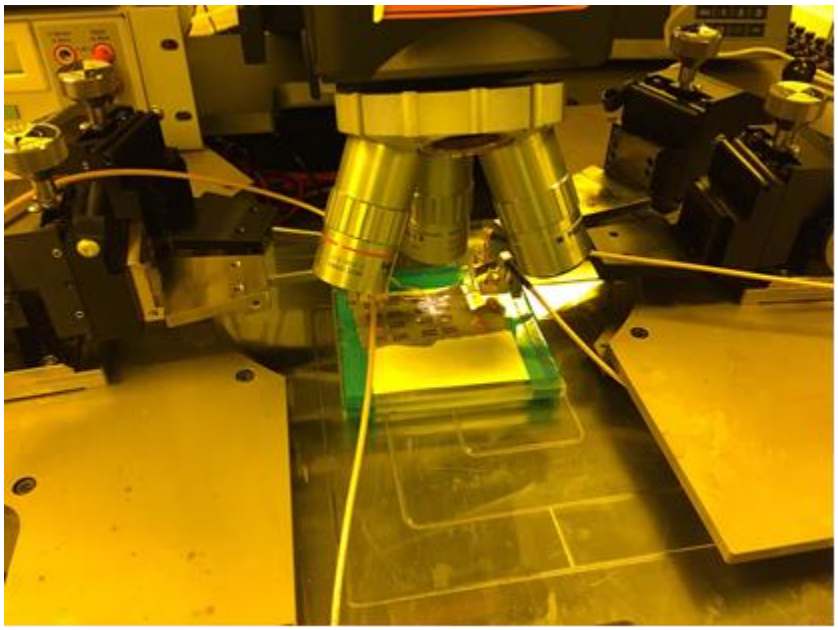


**Figure 83.Resistance measurement of reliability sample**

### 5.2.3 SEM imaging

To evaluate the samples after thermal cycling tests, SEM imaging was carried out after micro-sectioning and fine polishing. To protect the sample and to avoid any artificial cracking during sample handling and cross-sectioning, TPV samples were first molded with epoxy resins. Then, the molded samples were fine polished to expose the TPVs. No Cu cracking was found, which may explain why there were no obvious resistance changes. In addition, no silicon cracking was observed which can be attributed to the "cushion" effect of polymer to mitigate the first principal stresses in silicon, as discussed in Chapter 3. Magnified images at TPV corners were also observed to analyze the interfaces between different materials, where shear stresses localization occur as

predicted by the finite element modeling based simulations. The Cu/liner and liner/Si interfaces are shown in Figure 84 and Figure 85 respectively. Good adhesion for Cu-ZIF and Si-ZIF interfaces was confirmed.

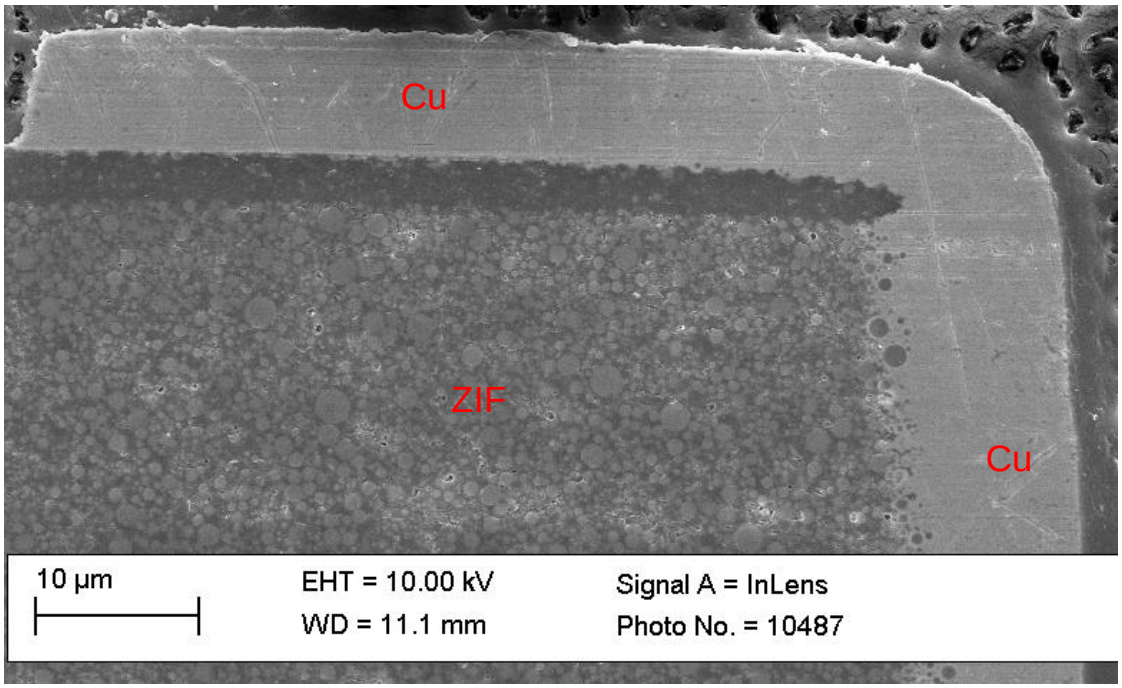



**Figure 84. SEM image of Cu/ZIF interface**

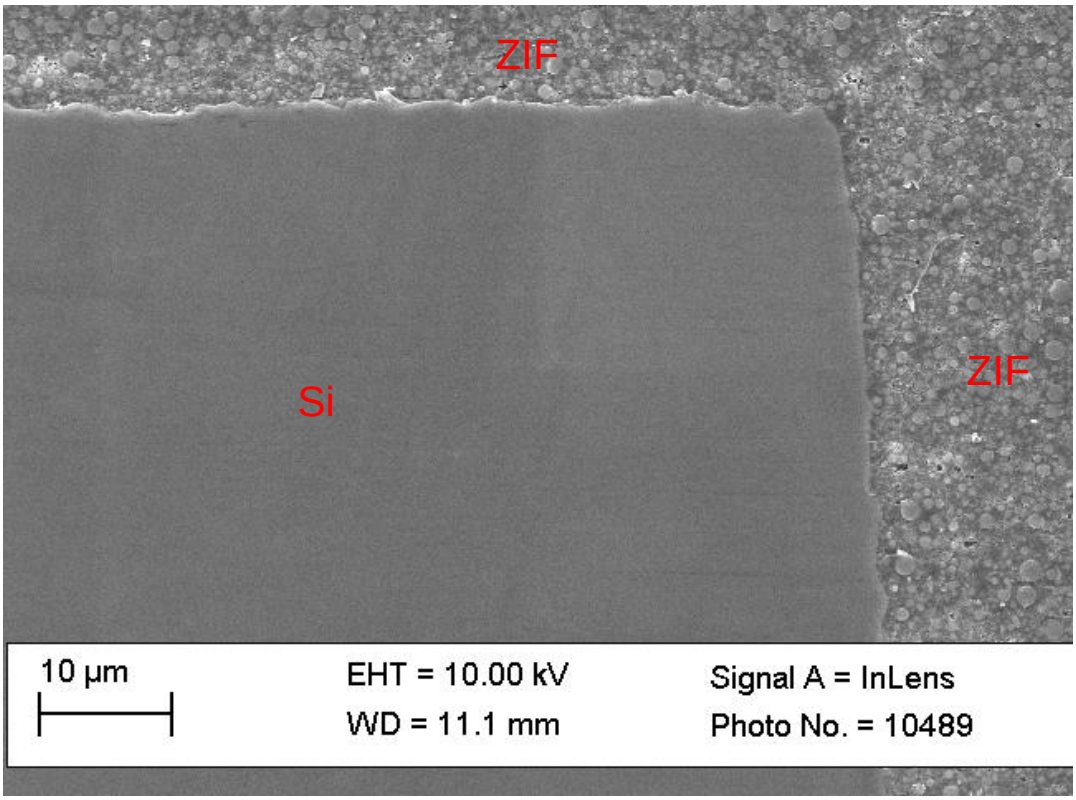



**Figure 85. SEM image of Si/ZIF interface**

## 5.3 Summary

### a. Electrical Test Vehicles with TPVs

- Based on the design guidelines provided in Chapter 3 and results from Chapter 4, electrical test vehicles with TPVs were demonstrated with multi-layer RDLs.
- High frequency measurements for 2ML structures indicated that both CPW lines and CPW-TPV transitions had very low insertion loss due to the isolation from the thick polymer liners. Good model to hardware correlation was also observed.

- Electrical performance of CPW lines and via transitions in structures with up to four metal layers was also characterized and the overall insertion loss was low due to the thick insulation liners.

**b. Reliability Test Vehicles with TPVs**

- Reliability test vehicles with daisy chain structures and four-point probe Kelvin structures were designed and fabricated. Such test vehicles shared the same design guidelines and fabrication processes as the electrical test vehicles with two metal layers.
- Thermal cycling tests were carried out on the fabricated samples and resistance was monitored during the test. No significant changes were observed, confirming good thermo-mechanical reliability of TPVs and RDLs in polycrystalline silicon interposers.

- SEM imaging was conducted on sample cross-sections after test. No Cu cracking was found, which explains the high number of cycles without any changes in resistance. No silicon cracking was observed either, due to the thick polymer liners, which lower the first principal stresses in the silicon substrate caused by CTE mismatch between copper and silicon. The interfaces of Cu/liner and Si/liner at the TPV corners were also analyzed and good adhesion was confirmed.

# CHAPTER 6

# RESEARCH SUMMARY AND CONCLUSIONS

Silicon interposers with TSVs have been developed in single-crystalline silicon wafer to address the high I/O density requirements between high performance logic, memory, graphic and other devices. However, single-crystalline silicon interposers suffer a few problems such as cost, electrical performance and reliability. To overcome these shortcomings of traditional silicon interposers, an entirely different approach using polycrystalline silicon interposers with polymer liners are proposed by GT-PRC, aiming to achieve lower cost silicon interposers with high performance and reliability.

The objective of this research is to explore and demonstrate thin polycrystalline silicon as a suitable interposer material to achieve high performance and high reliability TPVs in polycrystalline silicon materials with lower cost. Three fundamental challenges were defined, including: 1) low resistivity of the polycrystalline silicon material, resulting in high electrical loss; 2) potential reliability problems resulting from CTE mismatch between silicon and Cu, and 3) handling and processing of thin silicon panels. Accordingly, three research tasks were carried out to address the aforementioned challenges, involving: 1) electrical and mechanical modeling of TPV to provide design guidelines; 2) TPV formation, liner fabrication and TPV metallization with the handling of thin silicon panels and 3) electrical and reliability characterization of TPVs in polycrystalline silicon interposers.

This chapter presents the summary of this study with key contributions and potential future extensions. A list of the published papers, patent applications and awards is also provided.

## 6.1 Research Summary

### 6.1.1 Modeling and Design of TPVs

- **Electrical Modeling and Design of TPVs**
    - A 3D EM HFSS model was developed to simulate insertion loss and crosstalk of TPVs and compared with TSVs. TSVs were simulated with a typical 10 Ω-cm silicon material and 1 μm $SiO_2$ liner while TPVs were simulated with a much lower, 0.5 Ω-cm silicon, and 3 μm thick low electrical loss polymer liner ($\tan\delta$=0.002). TPVs showed lower insertion loss for up to 10 GHz and lower crosstalk for up to 6 GHz than TSVs. This is due to the thick insulating polymer on sidewalls, which decreases the capacitance of TPVs. The relativity larger crosstalk of TPVs at higher frequency resulted from the low resistance of the silicon substrates. This issue can be addressed with even thicker polymer liners.
    - Parametric studies suggested that thicker sidewall liners improved the electrical performance due to the decrease of TPV capacitance. Sidewall liners with 5-15 μm thickness are recommended to obtain low insertion loss and crosstalk at high frequency, with thicker liners preferred for even better electrical performance.
- **Mechanical Modeling and Design of TPVs**

- A 2D axisymmetric model was used in Ansys to simulate first principal stresses in Si and shear stresses in TPVs with 3 μm thick, low modulus polymer liners. The results were compared to TSVs with 1 μm $SiO_2$ insulation liners. TPVs presented much lower stress, showing that polymer liners act as stress buffer layers. This means a much lower risk of failures for TPVs.
- Thicker sidewall liners greatly reduce the stresses since thick liners tend to absorb stresses more effectively. In-via liners of 10-15 μm are necessary to significantly improve the reliability under thermal attack.

### 6.1.2 Formation, Liner Fabrication and Metallization of TPVs in Polycrystalline Silicon

- **Fracture Strength of Polycrystalline Silicon Substrates**
  - Four-point bending tool and Weibull plot were used for the fundamental study on fracture strength of the thin silicon panels. Weibull plot was used to obtain the characteristic strength value because the strength of the brittle polycrystalline silicon materials relates to the defects, which distribute randomly.
  - Surface polymer liners were introduced to improve the handling of the silicon panels. Fabrication of such surface liners can be integrated into the process flow for TPV. The experiment results showed that the existence of the surface liners significantly strengthened the samples, leading to a larger characteristic fracture strength and improved handling. Thicker liners can in further increase the impact.

- **TPV Formation**
    - Laser ablation was used for TPV formation, due to its reduced steps and higher throughput compared to DRIE for TSV etching. The absorption coefficient of silicon material enables high ablation efficiency of light with 200-400 nm wavelengths. Such light presents enough energy to excite the electrons, generate heat and finally lead to the removal of the material.
    - As a result, three types of lasers, a 355 nm picosecond laser, a 248 nm excimer laser and a 355 nm UV laser, were investigated. However, picosecond laser and excimer laser had disadvantages of low throughput and high production cost respectively. Hence, UV laser was selected since it is the best trade-off among via quality, throughput and cost.
- **TPV Liner Fabrication**
    - Spray coating and electrophoretic deposition were explored for TPV liner formation but suffered from poor edge coverage and non-uniformity respectively.
    - So the double laser method was developed, including a two-step laser process to enable TPV liners from raw silicon panels. The technical approach for liner formation involved a polymer filling in TPVs followed by laser ablation in polymer liners. ZIF dry film polymer was chosen as liner material due to its excellent properties as well as its easy processing with double laser method.

- Silane treatment was implemented before polymer filling to improve polymer adhesion to silicon by forming the covalent bonds. Fundamental studies on such mechanism were carried out and SEM imaging with EDS results confirmed the silanization process at both silicon surfaces and TPV sidewalls after treatment.
- The low intrinsic viscosity of ZIF at moderate temperature ensured void-free filling of polymer inside the via. The final step of laser ablation applied UV laser at 355 nm to directly break the bond in polymer liners and form the inner via, resulting in polymer liners around sidewall.

- **TPV Metallization**
  - A low cost, double-side electroless Cu plating process was applied to replace sputtered Cu seed. Desmear process was necessary to roughen the liner surface to improve adhesion. Thin Cu layer was formed on polymer surface with the reduction of Cu ions by Pd catalyst. Peeling tests suggested good adhesion between Cu and polymer liner, which is due to the formation of Cu/Resin mixture layer.
  - Semi-additive plating was carried out for TPV metallization. Optical cross-section imaging confirmed no cracking or interfacial failures.

### 6.1.3 Electrical and Reliability Characterization of TPVs in Polycrystalline Silicon Interposers

- **Electrical Characterization of TPVs in Polycrystalline Silicon Interposers**

- First, silicon interposers with TPVs and two metal RDLs were designed based on design guidelines in Chapter 3 and demonstrated with a low cost, double-side process based on the studies and analysis in Chapter 4. High frequency characterization results showed that both CPW lines and CPW-TPV transitions presented low insertion loss.
- Next, test vehicles with TPVs and four metal RDLs were designed and fabricated in two process segments, including 1) fabrication of test vehicle with two metal layers and 2) another two build-up layers and UV laser drilled micro-vias. After first segment, CPW lines and CPW-TPV transitions of the 2ML test vehicle were measured, showing low insertion loss. A good model-to-hardware correlation was also observed. After segment 2, the structures with up to four metal RDLs were characterized and overall low insertion loss was obtained, enabling multiple signal layer escape routing. Such good electrical performance is due to the thick insulating polymer liners.

- **Reliability Characterization of TPVs in Polycrystalline Silicon Interposers**
  - Reliability test vehicles of silicon interposers were also designed with daisy chain structures and four-point probe pads. Such test vehicles shared the same design guidelines and fabrication processes as the electrical test vehicles with two metal RDLs.

- Thermal cycling test between -55℃ and 125℃ was applied and resistance of the daisy chain was monitored throughout the test. TPVs survived 4000 cycles without significant resistance changes.
- SEM imaging was carried out to observe the cross-section of the sample after thermal cycling. No Cu or silicon cracking was found. Zoom-in images around corner also suggested good adhesion at Cu/liner and Si/liner interfaces.

### 6.2 Key Contributions

- First study of large size polycrystalline silicon panels to design, fabricate and characterize to achieve low cost silicon interposers with high performance and reliability
- First fundamental investigation of TPVs in polycrystalline silicon interposers with the introduction of thick polymer liners for insulation and stress buffering
  - Electrical simulations of TPVs showed superior electrical performance in comparison to TSVs.
  - Mechanical modeling of TPVs to investigate the effect of the low modulus polymer liners to act as stress buffer layers. TPVs presented lower first principal and shear stresses, resulting in lower possibility of failures.
  - Electrical and mechanical simulations as well as parametric studies provided design guidelines for polycrystalline silicon interposers with high performance and reliable TPVs.

- Fundamental analysis on the improved handling of thin polycrystalline silicon panels due to surface liners with four-point bending tool and Weibull plot.
- Demonstration and study of mechanism of laser ablation of TPV formation in polycrystalline silicon interposers.
- Introduction and mechanism of double laser method to form TPV liners. Fundamental mechanism study in adhesion of polymer to silicon surface was also carried out.

- First demonstration and characterization of polycrystalline silicon interposers with TPVs and RDLs
  - Low cost, novel and double-side processes to demonstrate fabrication of polycrystalline silicon interposers with TPVs and RDLs. Such process is proposed to replace the expensive CMOS (Complementary metal-oxide semiconductor) processes for single-crystalline silicon interposer with TSVs.
  - Electrical and reliability characterization of test vehicles showed high electrical performance and reliability of polycrystalline silicon interposers with TPVs and RDLs.
    - The characterization of electrical test vehicles with TPVs and multi-metal RDLs showed low insertion loss and good model-to-measurement correlation. This is attributed to the low loss and thick insulating polymer.

- TPVs in reliability test vehicles survived 4000 thermal cycles. SEM imaging confirmed no Cu or silicon cracking. Observations at the corners also suggested good adhesion at Cu/liner and liner/Si interfaces.

## 6.3 Future Extensions

The objective of this study is for modeling, design and demonstration of TPVs in polycrystalline silicon interposers to achieve low cost, high performance and reliability. Beyond the focus of this dissertation, there are still a few topics that can be investigated for improved polycrystalline silicon interposers in the future. For example, demonstration of smaller TPVs with finer pitch in polycrystalline silicon. This will help to improve I/O density for the package. It has been demonstrated that laser ablation can help achieve small TPVs in polycrystalline silicon panels. Liner fabrication processes, such as optimized ED and double laser method or other potential methods, can be developed to form liners in smaller TPVs. A second research topic could be on assembly of the polycrystalline silicon interposers. This includes the studies of both first level and second level interconnections. Materials, processes and assembly conditions can be investigated thoroughly. The mechanical stability of the interconnections should also be studied with focus on the warpage, especially for large size substrates.

## 6.4 Publications, Patents and Awards

### 6.4.1 Peer-reviewed Journals

1. **Qiao Chen**; Lu, H., Sundaram, V.; Tummala, R.R., " Modeling, Fabrication and Reliability of Through Vias in Polycrystalline Silicon Panels," Components,

Packaging and Manufacturing Technology, IEEE Transactions on, 2015 (Submitted)

2. **Qiao Chen**; Suzuki, Y.; Kumar, G.; Sundaram, V.; Tummala, R.R., "Modeling, Fabrication, and Characterization of Low-Cost and High-Performance Polycrystalline Panel-Based Silicon Interposer With Through Vias and Redistribution Layers," Components, Packaging and Manufacturing Technology, IEEE Transactions on, vol.4, no.12, pp.2035-2041, Dec. 2014
3. **Qiao Chen**; Xi Liu; Sundaram, V.; Sitaraman, S.K.; Tummala, R.R., "Double-Side Process and Reliability of Through-Silicon Vias for Passive Interposer Applications," Device and Materials Reliability, IEEE Transactions on, vol.14, no.4, pp.1041-1048, Dec. 2014
4. Xi Liu, **Qiao Chen**, Venkatesh Sundaram, Rao R. Tummala, Suresh K. Sitaraman, Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test, Microelectronics Reliability, Volume 53, Issue 1, January 2013, Pages 70-78
5. Xi Liu; **Qiao Chen**; Sundaram, V.; Simmons-Matthews, M.; Wachtler, K.P.; Tummala, R.R.; Sitaraman, S.K., "Reliability Assessment of Through-Silicon Vias in Multi-Die Stack Packages," Device and Materials Reliability, IEEE Transactions on, vol.12, no.2, pp.263-271, June 2012

### 6.4.2 Conference Proceedings

1. Demir, K.; Ramachandran, K.; Sato, Y.; **Qiao Chen**; Sukumaran, V.; Pucha, R.; Sundaram, V.; Tummala, R., "Thermomechanical and electrochemical reliability of fine-pitch through-package-copper vias (TPV) in thin glass interposers and

packages," Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, pp.353-359, 28-31 May 2013

2. Sundaram, V.; **Qiao Chen**; Tao Wang; Hao Lu; Suzuki, Y.; Smet, V.; Kobayashi, M.; Pulugurtha, R.; Tummala, R., "Low cost, high performance, and high reliability 2.5D silicon interposer," Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd, pp.342-347, 28-31 May 2013
3. Tummala, R.; Sundaram, V.; **Qiao Chen**; Lu, H.; Kumar, G., Low-cost and High Performance Silicon Interposers and Packages (LSIP)–A New Georgia Tech PRC Industry Consortium, Pan Pacific Symposium Conference Proceedings, 2013
4. Sundaram, V.; **Qiao Chen**.; Suzuki, Y.; Kumar, G.; Fuhan Liu; Tummala, R., "Low-cost and low-loss 3D silicon interposer for high bandwidth logic-to-memory interconnections without TSV in the logic IC," Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd, pp.292-297, May 29 2012-June 1 2012
5. Xi Liu; **Qiao Chen**; Sundaram, V.; Simmons-Matthews, M.; Wachtler, K.P.; Tummala, R.R.; Sitaraman, S.K., "Thermo-mechanical behavior of through silicon vias in a 3D integrated package with inter-chip microbumps," Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st, pp.1190-1195, May 31 2011-June 3 2011
6. **Qiao Chen**; Bandyopadhyay, T.; Suzuki, Y.; Fuhan Liu; Sundaram, V.; Pucha, R.; Swaminathan, M.; Tummala, R., "Design and demonstration of low cost, panel-based polycrystalline silicon interposer with through-package-vias (TPVs),"

Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st, pp.855-860, May 31 2011-June 3 2011

7. Sukumaran, V.; Bandyopadhyay, T.; **Qiao Chen**; Kumbhat, N.; Fuhan Liu; Pucha, R.; Sato, Y.; Watanabe, M.; Kitaoka, Kenji; Ono, M.; Suzuki, Y.; Karoui, C.; Nopper, C.; Swaminathan, M.; Sundaram, V.; Tummala, R., "Design, fabrication and characterization of low-cost glass interposers with fine-pitch through-package-vias," Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st, pp.583-588, May 31 2011-June 3 2011
8. Sukumaran, V.; **Qiao Chen**; Fuhan Liu; Kumbhat, N.; Bandyopadhyay, T.; Chan, H.; Min, S.; Nopper, C.; Sundaram, V.; Tummala, R., "Through-package-via formation and metallization of glass interposers," Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th, pp.557-563, 1-4 June 2010
9. Liu, Xi; **Qiao Chen**; Sundaram, Venkatesh; Muthukumar, Sriram; Tummala, Rao R; Sitaraman, Suresh K; Reliable design of electroplated copper through silicon vias, ASME 2010 International Mechanical Engineering Congress and Exposition, pp. 497-506, 2010
10. Tummala, R.R.; Sundaram, V.; Chatterjee, R.; Raj, P.M.; Kumbhat, N.; Sukumaran, V.; Sridharan, V.; Choudury, A.; **Qiao Chen**; Bandyopadhyay, T., "Trend from ICs to 3D ICs to 3D systems," Custom Integrated Circuits Conference, 2009. CICC '09. IEEE, pp.439-444, 13-16 Sept. 2009
11. Xi Liu; **Qiao Chen**; Dixit, Pradeep; Chatterjee, R.; Tummala, R.R.; Sitaraman, S.K., "Failure mechanisms and optimum design for electroplated copper Through-

Silicon Vias (TSV)," Electronic Components and Technology Conference, 2009. ECTC 2009. 59th, pp.624-629, 26-29 May 2009

### 6.4.3 Patents

1. Venkatesh V Sundaram, Fuhan Liu, Rao R Tummala, **Qiao Chen**, Through package via structures in panel-based silicon substrates and methods of making the same, 2012 (pending)
2. Venkatesh Sundaram, Fuhan Liu, Rao R Tummala, Vijay Sukumaran, Vivek Sridharan, **Qiao Chen**, Through-package-via (TPV) structures on inorganic interposer and methods for fabricating same, 2011 (allowed)

### 6.4.4 Awards

1. Co-author, Intel Best Student Paper, 60$^{th}$ Electronic Components and Technology Conference, 2010
2. Travel Award, 61$^{st}$ Electronic Components and Technology Conference, 2011

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[1] Tummala, R. R., Fundamentals of Microsystems Packaging, McGraw-Hill, 2001

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