# INTERPOSER PLATFORMS FEATURING POLYMER-ENHANCED THROUGH SILICON VIAS FOR MICROELECTRONIC SYSTEMS

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# INTERPOSER PLATFORMS FEATURING POLYMER-ENHANCED THROUGH SILICON VIAS FOR MICROELECTRONIC SYSTEMS

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*Dedicated to my parents Ajaybhai and Pallaviben,*

*wife Neha, brother Chirag, and sister Krishna*

*for their endless support.*

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# SUMMARY

Novel polymer-enhanced photodefined through-silicon via (TSV) and passive technologies have been demonstrated for silicon interposers to obtain compact heterogeneous computing and mixed-signal systems. These technologies include: (1) Polymer-clad TSVs with thick ($\sim$20 $\mu$m) liners to help reduce TSV losses and stress, and obtain optical TSVs in parallel for interposer-to-interposer long-distance communication; (2) Polymer-embedded vias with copper vias embedded in polymer wells to significantly reduce the TSV losses; (3) Coaxial vias in polymer wells to reduce the TSV losses with controlled impedance; (4) Antennas over polymer wells to attain a high radiation efficiency; and (5) High-Q inductors over polymer wells.

Cleanroom fabrication and characterization of the technologies have been demonstrated. For the fabricated polymer-clad TSVs, resistance and synchrotron x-ray diffraction (XRD) measurements have been demonstrated. High-frequency measurements up to 170 GHz and time-domain measurements up to 10 Gbps have been demonstrated for the fabricated polymer-embedded vias. For the fabricated coaxial vias and inductors, high-frequency measurements up to 50 GHz have been demonstrated. Lastly, for the fabricated antennas, measurements in the W-band have been demonstrated.

# CHAPTER I

# INTRODUCTION

The information revolution, fueled by the development of computing and communication technologies, has significantly improved our lives and promises to provide a world of highly interconnected devices. By 2020, more than 30 billion devices are estimated to be connected to the internet and the amount of digital data in this interconnected world is estimated to be greater than 40 zettabytes ($10^{21}$ bytes) [1]. This enormous rise of interconnected devices and digital data demands high-performance systems with faster connectivity and data storage. To cope with these demands, significant technology innovations are highly desired.

This research focuses on the development of photodefined polymer-enhanced interconnection and passive technologies to enable compact heterogeneous computing and mixed-signal systems. The motivation for the development of these components is described next.

## *1.1 Motivation*

Since the invention of the transistor in 1947, the information revolution has been consistently driven by semiconductor technology innovations. The integrated circuit (IC), invented in 1958, has been the key technology fueling the revolution owing to its constant improvements in productivity and performance [2]. Following Gordon Moore's projection in 1965 [3], the number of transistors in a given area has continually increased with device scaling, as shown in Figure 1 [4]. This increase in the number of transistors has been a key factor in reducing gate cost and leading to affordable ICs with more functionality and thereby significantly improved productivity. Moreover, the performance of microprocessor ICs has increased by more than

3000X while the gate speeds have increased by more than 100X since the mid-1980s when complementary metal-oxide semiconductor (CMOS) microprocessors were introduced [4]. To sustain the continued improvement in microprocessor performance while limiting power dissipation, multicore microprocessors have been implemented since the early 2000s instead of aggressive clock frequency scaling [5–7]. However, the migration to multicore microprocessors has created an incredible demand for low-energy and high-bandwidth off-chip communication [8].

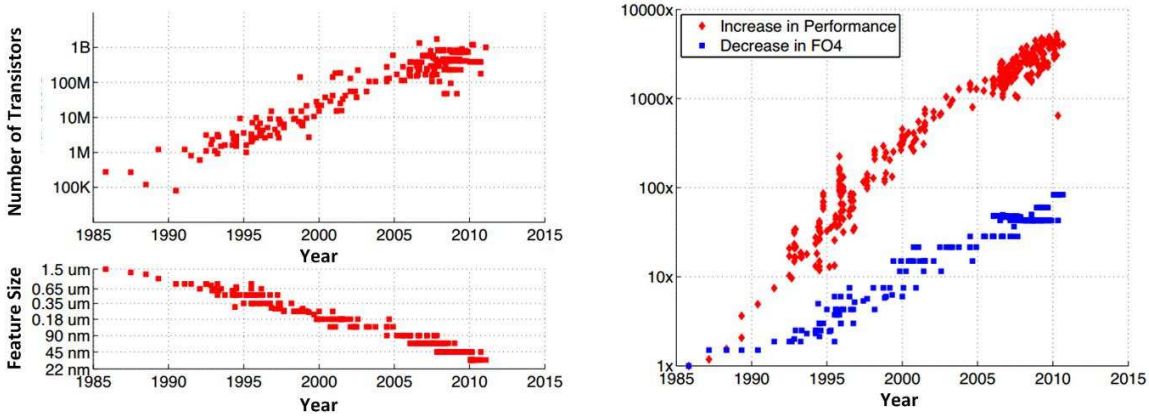



Figure 1: Consistent increase in transistor count, consistent transistor scaling, and improvements in microprocessor performance (normalized to that of a 386) and gate speeds (approximation of the FO4) since the introduction of CMOS microprocessors [4].

### 1.1.1 Demand for High Off-chip Bandwidth

K. Bowman et al. [9] have demonstrated that increasing the communication bandwidth greatly improves throughput for a system with a many-core CPU and memory (Figure 2) using the following equation:

$$TP(N) = \frac{N}{\frac{CPI_{com}}{F_{clk}} + \frac{CPI_{mem,lat}(F_{clk})}{F_{clk}} + \frac{CPI_{mem,bw}(F_{clk})}{F_{clk}}}, \quad (1)$$

where $N$ represents the number of cores, $F_{clk}$ the clock frequency, $CPI_{com}$ the computation component of cycles per instruction (CPI), $CPI_{mem,lat}$ the memory latency component of CPI, and $CPI_{mem,bw}$ the bandwidth component of CPI.

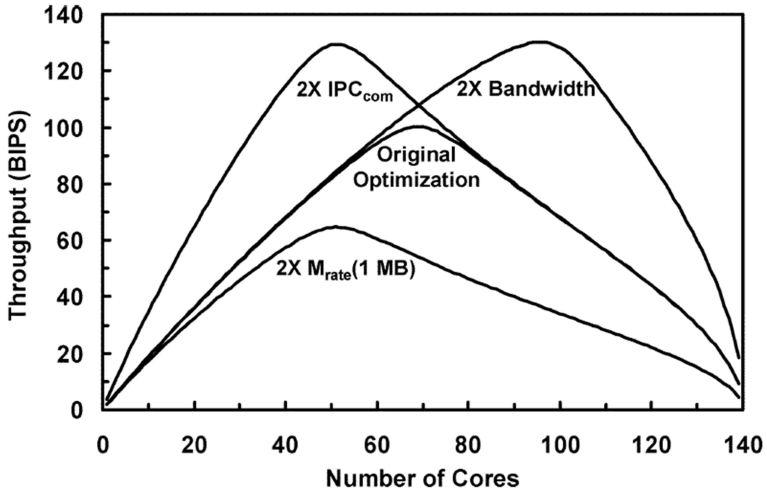



Figure 2: Plot showing performance improvement in a many-core chip with high memory bandwidth [9].

Equation 1 shows that to improve the system throughput, the memory bandwidth must be improved in addition to reducing memory latency (which includes interconnect and memory access delays). As the memory bandwidth increases, the cache size constraints are lowered thus allowing for more cores in the same area resulting in higher performance.

Moreover, Figure 3 qualitatively shows the increasing off-chip bandwidth demands, due first of all to the integration of the memory controller hub in the CPU, and then to the transition to multi-core microprocessors, requiring innovative interconnection and packaging solutions.

### 1.1.2 Demand for Heterogeneous Integration Platforms

In addition to the digital circuits, analog and radio-frequency (RF) functionalities are highly desired for high-performance and high-speed computing and communication systems. This need for the integration of different functionalities has led to the development of heterogeneous platforms such as system-on-chip (SoC) architectures [10]. However, there are challenges with the heterogeneous integration platforms as described next.

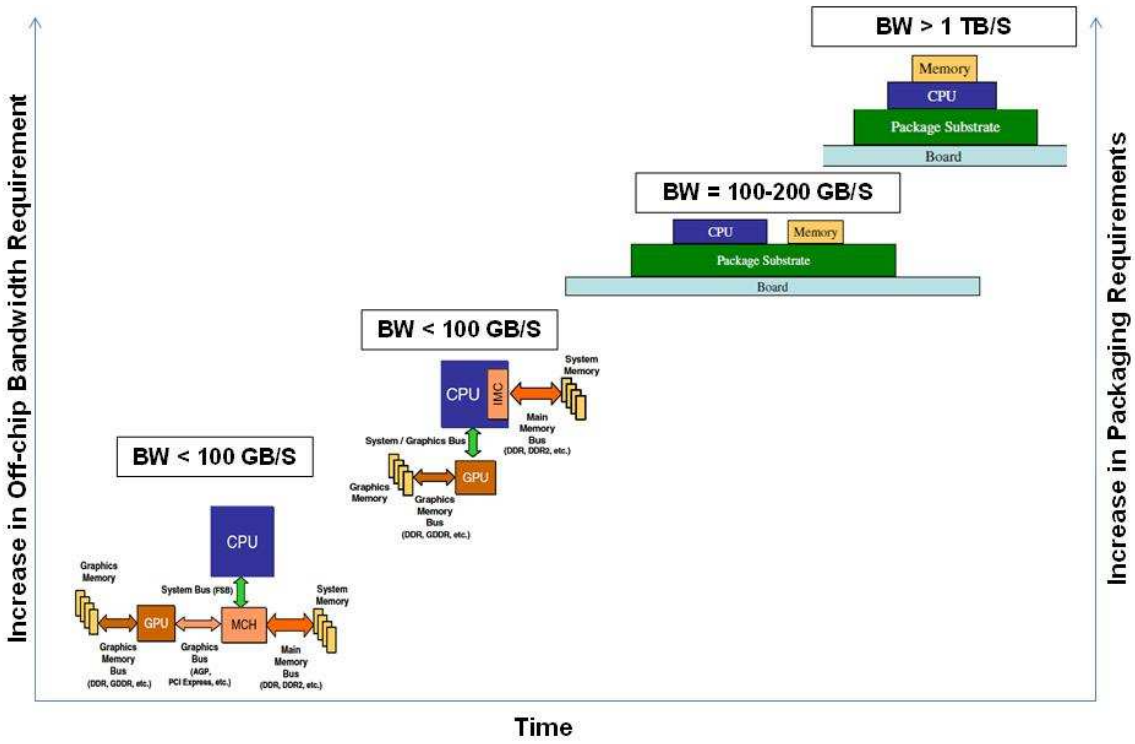



Figure 3: Increase in off-chip bandwidth and demand for innovative interconnection and packaging technologies. Images in the plot are from L. Polka et al. [8].

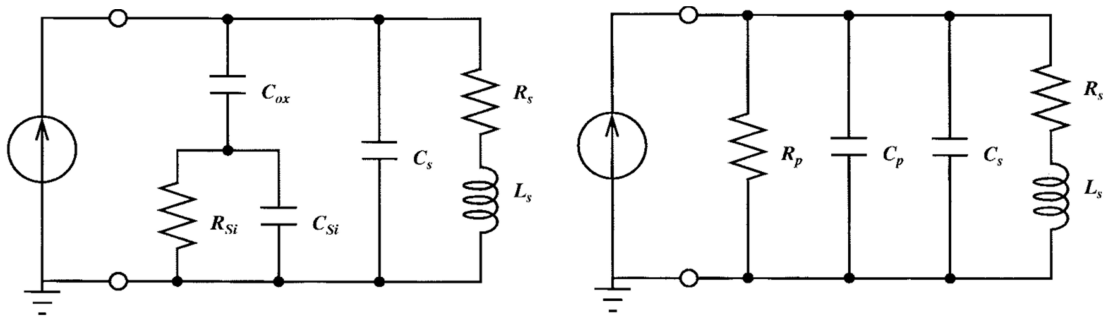
#### *1.1.2.1 Analog and Radio-frequency IC Integration*

Unlike digital circuits, the performance and precision of analog systems have not been significantly improving due to scaling. Instead, scaled MOS transistors worsen matching and noise, while a reduction of the supply voltage affects signal energy and signal-to-noise ratios [11]. Moreover, with respect to RF systems, power amplifiers (a critical building block in wireless systems) are traditionally implemented using III-V heterojunction bipolar transistor (HBT) based solutions for performance and cost effectiveness [12]. Hence, significantly different requirements must be met by a platform such as SoC for the integration of heterogeneous technologies.

#### *1.1.2.2 Integration of Passives*

Additionally, for RF and analog/mixed-signal (AMS) systems, the implementation of high-performance on-chip passive components such as inductors is highly desired,

although very challenging [10]. This need for the integration of passives has been a key barrier to the scaling of RFICs, including power amplifiers, voltage controlled oscillators and filters [13]. For example, on-chip inductors in CMOS processes yield poorer Q-factors (<30) compared to off-chip inductors due to high-frequency losses in silicon and ohmic losses in metal layers [14]. To explain this more clearly, a 2D planar inductor (a spiral inductor, for example) model with one-port excitation over silicon and an oxide layer between the inductor and the silicon is shown in Figure 4(a) [15].




(a) (b)

Figure 4: Inductor physical models: (a) Lumped model and (b) Equivalent circuit model using the lumped model [15].

In the series path of the inductor, $L_s$ represents the spiral inductance, $R_s$ the metal series resistance, and $C_s$ the capacitance due to the overlaps between the spiral and the center-tap underpass. The parasitics in the shunt path include $C_{ox}$ representing the oxide capacitance between the spiral and the substrate, $C_{Si}$ the silicon substrate capacitance, and $R_{Si}$ the silicon substrate resistance. Converting the shunt path into $R_p$ and $C_p$ in parallel, an equivalent circuit model is obtained, as shown in Figure 4(b). From the equivalent circuit model, the Q-factor for the inductor is obtained as follows [15]:

$$Q = \frac{\omega L_s}{R_s} * \frac{R_p}{R_p + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right] R_s} * \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p)\right], \quad (2)$$

where Equation 2 could be rewritten as

$$Q = \frac{\omega L_s}{R_s} * \text{substrate loss factor} * \text{self-resonance factor.} \tag{3}$$

In the Equations 2 and 3, $\omega L_s/R_s$ represents the magnetic energy stored and the ohmic loss in the series resistance. The other two components of the Q-factor are represented by the substrate loss factor and the self-resonance factor. At low frequencies, the Q-factor depends on $\omega L_s/R_s$ and at higher frequencies it primarily depends on the substrate loss factor. The equation for the substrate loss factor shows that with a very high $R_p$ the loss factor approaches unity resulting in a significant reduction in the impact of the substrate loss on the Q-factor. Consequently, the Q-factor can be improved by reducing the parallel conductance. Typically, this is accomplished with techniques such as high-resistivity silicon or removing silicon from the back side of a chip [16, 17], but these options could be expensive at chip level.

Moreover, according to the International Technology Roadmap for Semiconductors (ITRS), Q-factors greater than 50 will be needed beyond 2020 [10]. This requirement suggests a need for high-performance off-chip inductors that can be integrated close to ICs with minimal impact from the interconnect parasitics.

#### *1.1.2.3 Integration of Antennas and Millimeter-wave Applications*

Similar to inductors, the performance of on-chip antennas suffers from losses in silicon yielding low gains (<-2 dBi) [18]. This low-gain performance results because on-chip antennas find a low-resistivity path through the silicon substrate and the high dielectric constant of the silicon substrate causes most of the antenna power to be confined in the substrate [18]. Moreover, antennas built on CMOS or SiGe have very narrow impedance and gain bandwidths [19].

The poor on-chip antenna performance has consequently created a demand for the integration of off-chip antennas close to ICs for a wide range of applications,

specifically for those in the millimeter-wave (mm-wave) frequency bands (30 GHz - 300 GHz) with smaller antenna sizes. For example, the frequency band around 60 GHz has been explored for high-speed multimedia transfer and short-range communications [20]; the band around 28 GHz has been explored for the future 5G communications [21]; the band around 77 GHz has been explored for radars in automobiles [22]; and the D-band has been explored for medical imaging and pico-cell cellular links [23]. For these applications the integration of heterogeneous ICs, inductors and antennas on a platform with short distance communication between them is highly desired.

### 1.1.3 Interposers for Heterogeneous Integration

To cope with these demands, 2.5-dimensional (2.5D) interconnection of microelectronic circuits is currently being extensively explored [24–31]. Compared to multichip modules with chips over ceramic or organic substrates, 2.5D integration is enabled by interposers with fine-pitch wiring and vertical through-substrate vias supporting multiple chips. Silicon, glass and organic substrates have chiefly been explored in the literature for interposers with a second level package in between them and motherboard [31–33]. However, silicon interposers (as shown in Figure 5) have clear advantages over glass and organic interposers: (1) a denser metallization can be obtained over silicon interposers with relative ease using conventional back-end-of-line (BEOL) processing techniques; (2) silicon has better thermal conductivity; and (3) the fabrication of through-silicon vias (TSVs) and fine-pitch microbumps is becoming well established. These advantages enable high bandwidth-density communication between the chips mounted over silicon interposers (using a comparatively simpler fabrication) [29]. Additionally, silicon interposers provide opportunities for the integration of antennas and inductors close to ICs, yielding compact RF and AMS systems. The TSVs, with copper conductors insulated from the silicon commonly using a thin ($<1$ $\mu$m) silicon dioxide liner, are the key enablers for system integration

using silicon interposers.

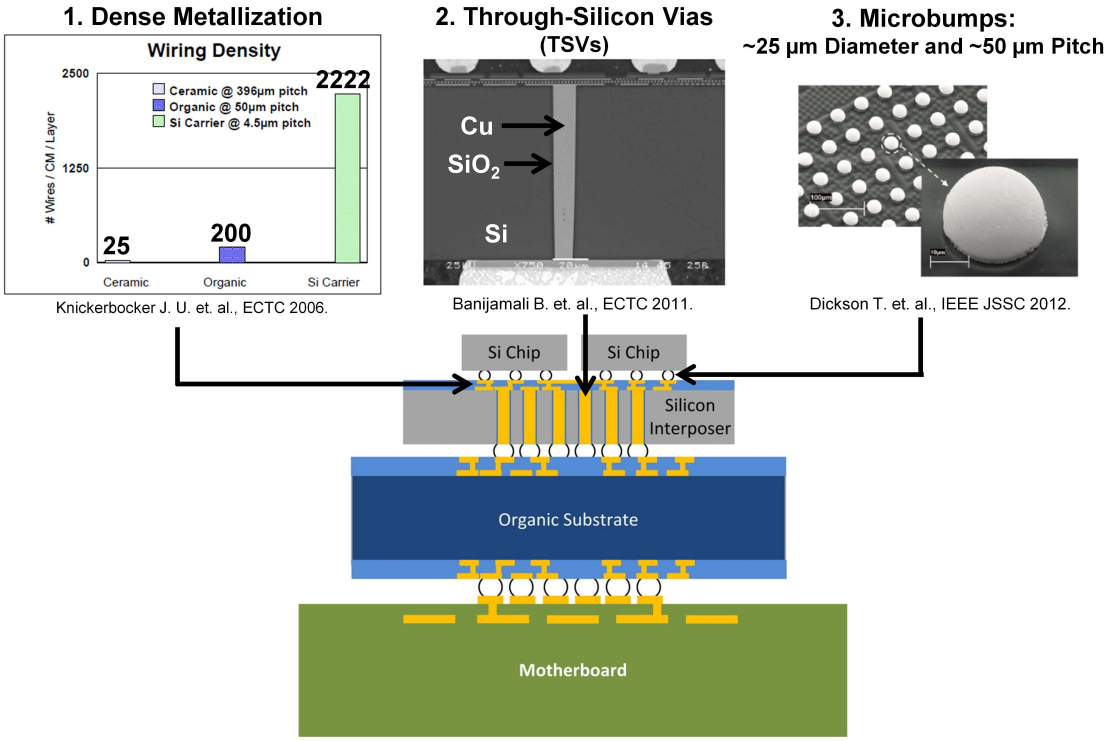



Figure 5: Schematic of a 2.5D system using silicon interposer technology with key components shown [24, 25, 29].

Figure 6 highlights select systems demonstrated in the literature using silicon interposers, with

- IBM's demonstration of a 21.2 mm x 21.2 mm silicon interposer consisting of 4-level fine-pitch metallization and supporting chips with 50 $\mu$m pitch C4 microbumps to enable an 8x10 Gb/s synchronous communication between the chips [29];

- Xilinx/TSMC's demonstration of a 25 mm x 31 mm silicon interposer (65 nm metallization) consisting of 10 $\mu$m diameter and 100 $\mu$m tall TSVs on a 150 $\mu$m pitch and mounted over a second-level organic package to enable a complete 2.5D system such as an interposer supporting two 28 nm FPGA dice and two 65 nm mixed-signal dice [25, 26];

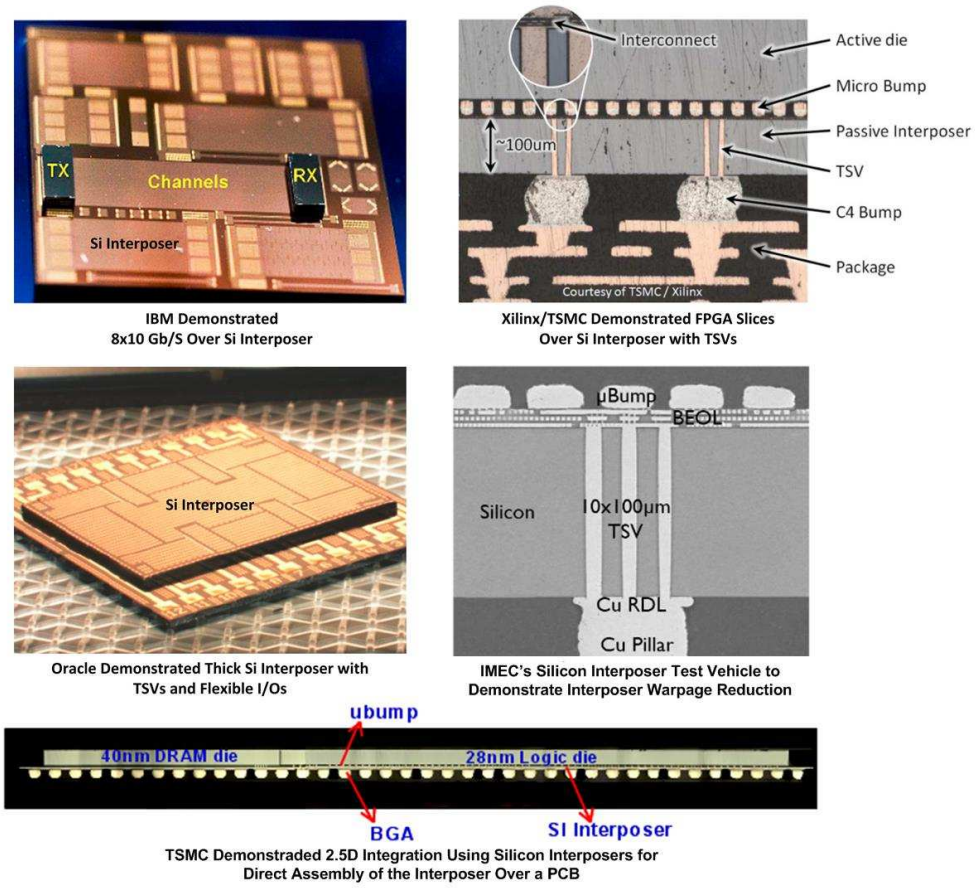



Figure 6: 2.5D system demonstrations in the literature [26–30].

- Oracle's demonstration of a 13.1 mm x 16.1 mm silicon interposer consisting of 50 $\mu$m diameter and 400 $\mu$m tall TSVs and MoCr flexible I/Os for opto-electronic Macrochip application [30];

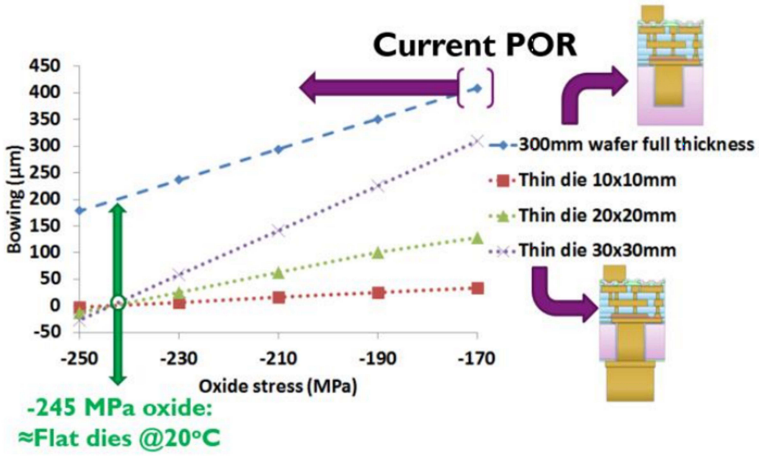
- IMEC's demonstration of a 30 mm x 30 mm silicon interposer consisting of 10 $\mu$m diameter and 100 $\mu$m tall TSVs to understand and minimize warpage [28]; and

- TSMC's demonstration of a 26 mm x 24 mm silicon interposer to enable a 2.5D chip-on-wafer (CoW) technology with direct assembly of the interposer (supporting two 40 nm DRAM dice and one 28 nm logic die) over a printed circuit board (PCB) without a second-level package [27].

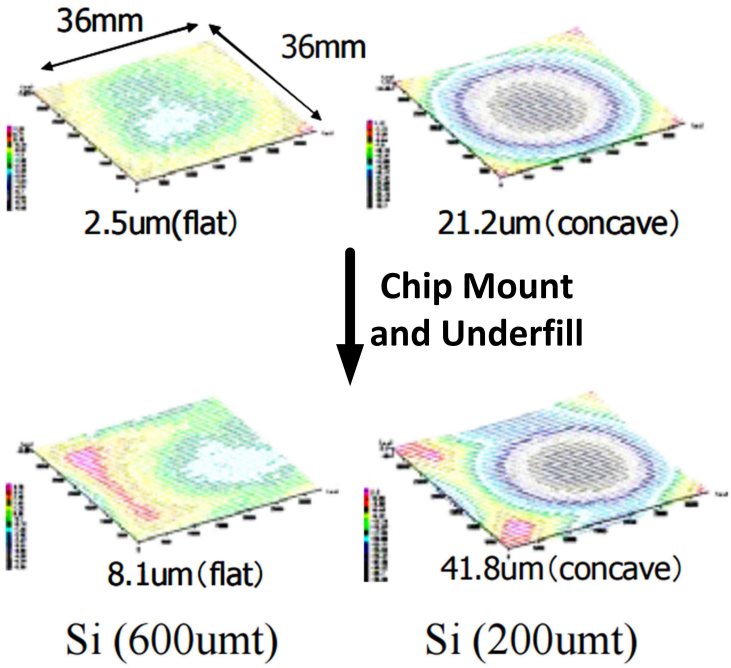
Despite these advances with silicon interposers, there are electrical and thermo-mechanical challenges with TSVs in the interposers and electrical challenges (similar to the ones for silicon ICs) with passives over the interposers. Additionally, there is a demand for optical paths for large-scale multi-interposer systems. The challenges and the needs are described as follows:

- **Large-area thick interposers increase TSV loss:** Large-area (limited by the reticle size) silicon interposers are desired for the integration of heterogeneous ICs with antennas and inductors close to the ICs [20, 34]. Greater silicon thickness (greater than 300-400 $\mu$m) is desired for the large-area interposers to minimize warpage and bow, and improve mechanical stability as described in the following two examples: (1) Figure 7(a) demonstrates the analysis results for bow after the TSV, BEOL and bump fabrication showing a higher bow for large-area interposer dice [28]; and (2) Figure 7(b) demonstrates the warpage measurements of a 36 mm x 36 mm interposer showing reduced warpage for a thicker interposer [35]. However, increasing the interposer thickness results in longer TSVs with increased losses [36], as shown in Figure 8. These factors drive the need for low-loss TSV technologies for large-area thick interposers to compensate for the increased length.

- **Silicon affects the antenna and inductor performance:** The availability of a large area with silicon interposers could be leveraged to form antenna arrays for compact RF systems [20]. Moreover, it could be leveraged to form high-Q (>50) inductors close to ICs with minimized interconnect parasitics and thereby improve the performance of circuits such as digital controlled oscillators, low-noise amplifiers and power amplifiers [37]. However, the presence of a silicon interposer underneath antennas and inductors results in lower radiation efficiency and Q-factor, respectively, similar to the silicon ICs as described in




(a)




(b)

Figure 7: (a) Bow simulation for thinned interposer dice and wafer after TSV, BEOL and bump fabrication, [28] and (b) warpage measurement of silicon interposers from the BGA pad side after chip mount and underfill [35].

Section 1.1.2. This performance degradation due to silicon demands for innovative antenna and inductor integration technologies with silicon interposers.

- **Issues with high-resistivity silicon and glass:** High-resistivity silicon and glass interposers have been explored in the literature to address the challenges

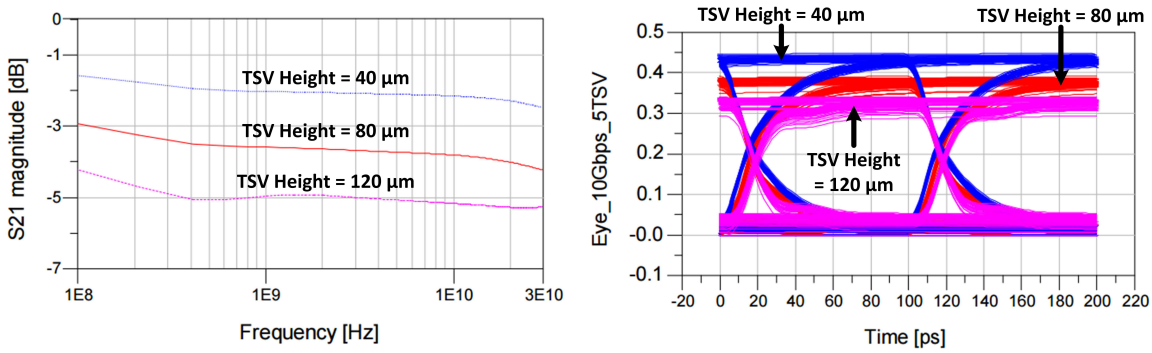



Figure 8: Impact of TSV length on insertion loss and eye diagram [36].

with silicon [20,34]. However, high-resistivity silicon is relatively expensive and the fabrication of vias in glass is challenging. As a result, innovative interposer technologies are desired.

- **CTE mismatch causes TSV stress:** The coefficient of thermal expansion (CTE) mismatch between the copper and silicon results in high TSV stresses, leading to thermomechanical reliability issues such as cohesive cracks in silicon and interfacial delaminations [38]. Consequently, TSV stress reduction techniques are needed.

- **Demand for the integration of optical paths:** For longer interconnect distances that traverse the motherboard (between chips on different silicon interposers, for example), optical interconnects may provide a path for higher bandwidth and lower energy communication relative to conventional electrical interconnects [39]. As such, there is a need to integrate optical links with conventional electrical interconnects, including at the silicon interposer level [40].

## 1.2 Research Objective and Contribution

The objective of this research is to fabricate and characterize novel electrical TSVs that exhibit low electrical loss for silicon interposer applications and utilize the technology developed for fabricating the novel TSVs to attain high-Q inductors and high radiation efficiency antennas. To achieve the research objective, the contribution of this research includes the fabrication and characterization of photodefined polymer-enhanced TSVs, and polymer-enhanced inductors and antennas obtained using the TSV photodefinition technique (Figure 9). The developed photodefined polymer-enhanced technologies are described as follows:

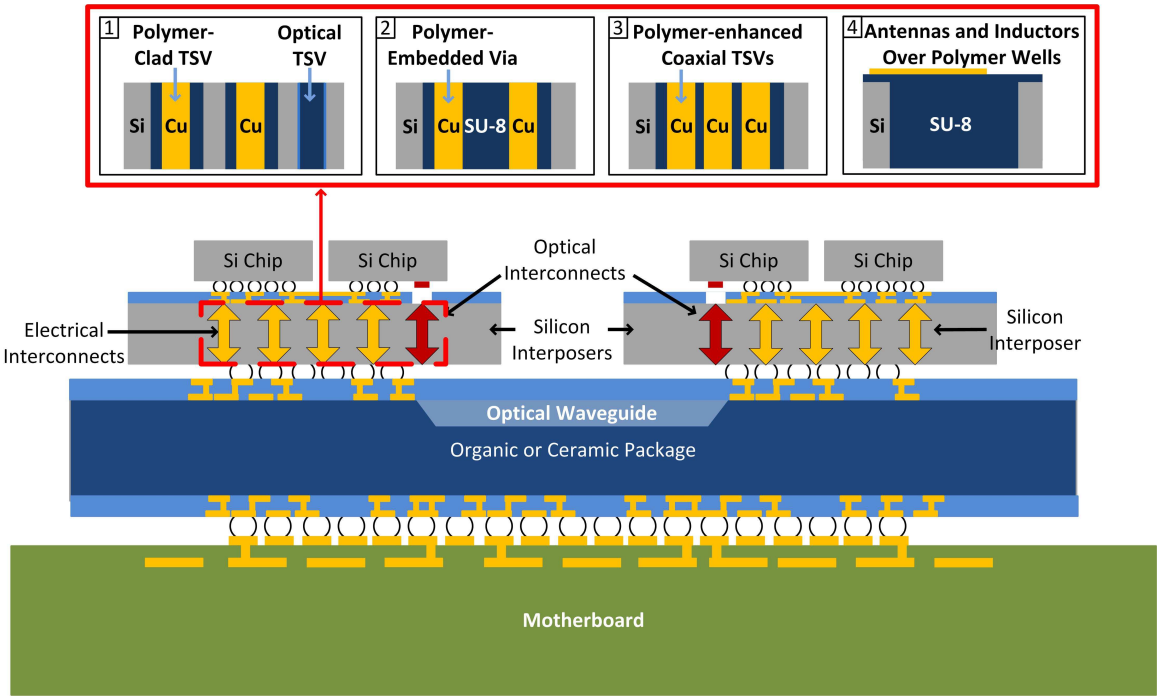



Figure 9: Envisioned silicon interposer based system featuring photodefined (a) polymer-clad TSVs and optical TSVs that can be fabricated simultaneously, (b) polymer-embedded vias, (c) polymer-enhanced coaxial vias, and (d) polymer-enhanced inductors and antennas.

**1. Photodefined polymer-clad TSVs:** The proposed TSVs consist of a thicker polymer liner compared to the state-of-the-art TSVs with a thin (<1 $\mu$m) silicon dioxide liner. Due to the thicker polymer liner, a reduction in TSV thermomechanical

stress, TSV dielectric capacitance and high-frequency loss is expected. An additional feature of the proposed TSVs is that they enable simultaneous fabrication of polymer-filled optical TSVs with no additional lithography steps. The optical TSVs help achieve a high-bandwidth interposer-to-interposer communication. Resistance measurements are performed for the fabricated polymer-clad TSVs and optical loss measurements are performed for the fabricated optical TSVs. To characterize strains in the fabricated polymer-clad TSVs and compare them to the TSVs with silicon dioxide liner, synchrotron x-ray diffraction (XRD) measurements are demonstrated.

**2. Photodefined polymer-embedded vias:** To attain even further reduction in TSV high-frequency loss compared to the polymer-clad TSVs, this research demonstrates the fabrication and characterization of polymer-embedded vias with copper vias embedded within polymer-filled wells in a 10 Ω-cm resistivity silicon. Since a polymer separates the copper vias, a reduction in TSV loss is expected for the fabricated polymer-embedded vias. High-frequency measurements from 100 MHz to 50 GHz and from 110 GHz to 170 GHz, and time-domain measurements up to 10 Gbps are demonstrated for the fabricated polymer-embedded vias.

**3. Photodefined polymer-enhanced coaxial vias:** To attain greater control over TSV impedance, reduce loss, and lower coupling, coaxial configuration of the polymer-embedded vias is demonstrated. High-frequency measurements up to 50 GHz are demonstrated for the fabricated coaxial vias.

**4. Photodefined polymer-enhanced antennas and inductors:** To attain higher radiation efficiency and Q-factors, polymer-enhanced antennas and inductors are demonstrated, respectively, over polymer wells. The antennas integrated over polymer wells can be utilized in the future to form antenna arrays on silicon interposers yielding compact RF systems [20]. Moreover, the proposed high-Q inductors could be utilized in the future to improve the figure of merit of digital controlled oscillators, to improve the noise figure of low-noise amplifiers, and increase the power

efficiency of power amplifiers [37].

**Rationale underlying photodefinition:** The fabrication of the proposed TSVs in this research differs from the fabrication of the TSVs with silicon dioxide liner principally due to the fact that the fabrication of the proposed TSVs leverages the advantage of high aspect-ratio dielectric photodefinition [41], as described in Figure 10. In the fabrication of the TSVs with silicon dioxide liner, the diameter and aspect-ratio scaling depend on the availability of plasma etching tools and processes. Whereas, for the proposed TSVs obtained using dielectric photodefinition, etching requirements are relaxed since a larger area (via or trench) can easily be etched in silicon followed by polymer filling, photodefinition and electroplating. There is fairly minimal analysis and technological development reported in the literature for photodefined TSVs; S. W. Ho et al. [42] have shown the fabrication of coaxial TSVs using photodefinition to obtain impedance matching.

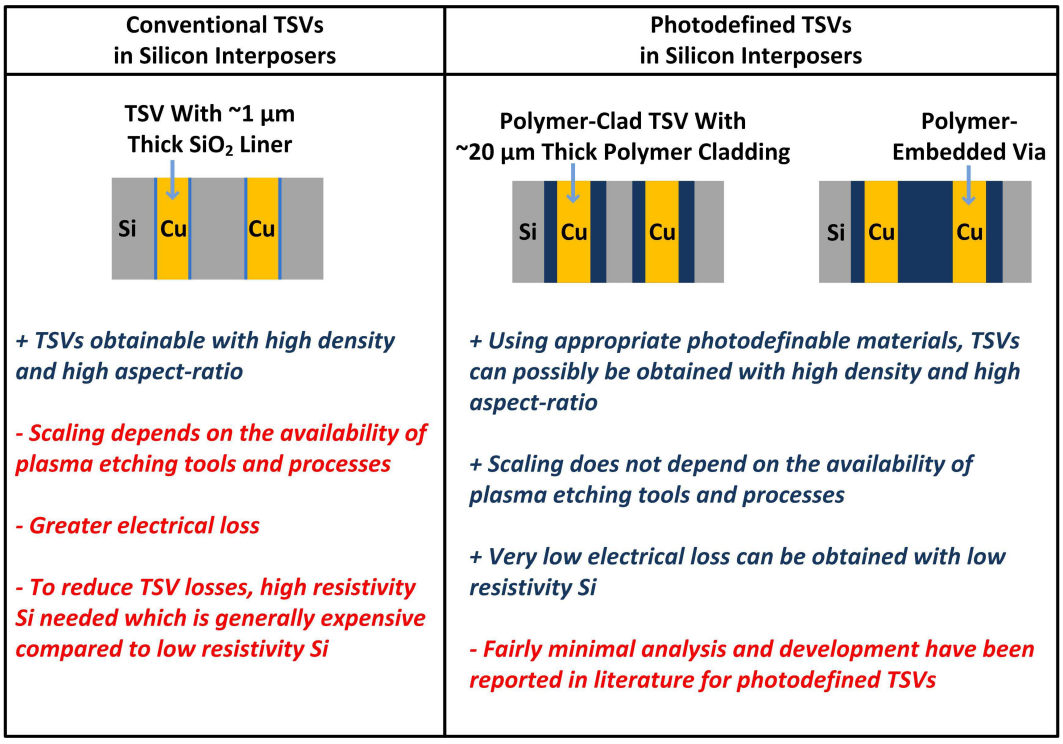



Figure 10: Comparison between conventional and photodefined TSVs for silicon interposers.

Hence, the rationale underlying this research is to both investigate and advance the fabrication process of photodefined TSVs that provide lower loss compared to the TSVs with silicon dioxide liner. Moreover, inductors and antennas are demonstrated in this research leveraging the expertise developed for the photodefined TSVs.

## *1.3 Organization*

The dissertation is organized as follows:

- Chapter 2: The fabrication and characterization of polymer-clad TSVs with a thick polymer liner is demonstrated. Moreover, the fabrication and characterization of optical TSVs that can be obtained in parallel with the polymer-clad TSVs is also demonstrated.

- Chapter 3: The fabrication of polymer-embedded vias is demonstrated along with the challenges addressed during their fabrication.

- Chapter 4: RF and time-domain characterizations of polymer-embedded vias are demonstrated.

- Chapter 5: The fabrication and characterization of polymer-enhanced coaxial vias, antennas and inductors are demonstrated.

- Chapter 6: A summary is given and potential future work on the demonstrated technologies is described.

# CHAPTER II

# POLYMER-CLAD AND OPTICAL TSVS: FABRICATION AND CHARACTERIZATION

This chapter describes the fabrication of TSVs with thick polymer liners and optical TSVs, strain and DC characterizations of the TSVs with thick polymer liners, and optical loss characterization of the optical TSVs.

## *2.1 Literature Survey and Analysis*

### 2.1.1 Electrical TSV Fabrication Processes

As shown in Figure 11, the fabrication process commonly used for TSVs begins with the etching of blind vias in a silicon wafer using the anisotropic BOSCH process etching followed by the formation of a dielectric liner [43, 44]. Once the dielectric liner is formed, barrier and seed layers are deposited followed by superfill copper electroplating. The additional copper obtained over the electroplated vias is removed using chemical-mechanical polishing (CMP). The additional silicon at the base of the fabricated copper-filled vias is then removed by either CMP or silicon etching to obtain TSVs.

However, voids may be obtained in the TSVs that are fabricated using the commonly implemented process. Moreover, this process requires back side silicon removal. In order to address these issues, an alternative fabrication process has been described in the literature [45] using bottom-up copper electroplating of TSVs with a group of microvias (called mesh) in the oxide layer at the base of the etched vias. The latter process is utilized in this research to develop novel TSV technologies.

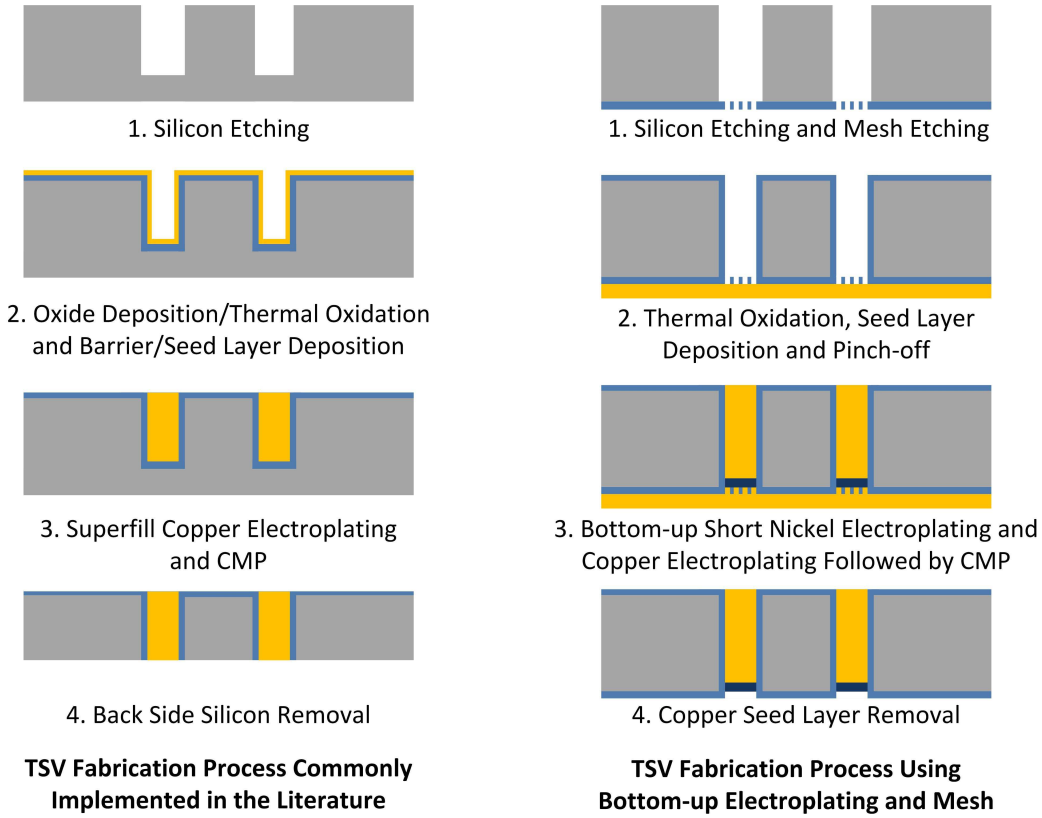



Figure 11: TSV fabrication processes.

### 2.1.2 Polymer Liner for TSVs

#### *2.1.2.1 Survey of Liner Materials and Polymer Liner Fabrication Processes*

Various types of TSV liners have been described in the literature, including silicon dioxide, air and polymer. A silicon dioxide liner can either be obtained using thermal oxidation or oxide deposition. However, it is difficult to achieve conformal thick (>1 $\mu$m) silicon dioxide liners.

Compared to the silicon dioxide liner, air liners with a lower relative dielectric constant have been described in the literature to achieve reduced TSV dielectric capacitance and loss. Thick (~30 $\mu$m) air liners can be fabricated by etching silicon around the fabricated TSVs [35]. Whereas, thin (~3 $\mu$m) air liners can be fabricated by depositing silicon dioxide over etched circular trenches in silicon until the tops of the trenches get pinched-off or alternatively by using a sacrificial material filled

in the etched circular trenches [46] followed by TSV fabrication at the center of the trenches [47].

In addition to silicon dioxide and air liners, thick polymer liners have also been described in the literature. The main advantage of using polymer liners compared to air liners is that the fabrication of horizontal interconnects is easier over thick (∼20 $\mu$m) polymer liners than thick air liners.

The fabrication of polymer liners has been described in the literature using polymer vapor deposition [48], polymer filling in circular trenches within silicon [49], laser ablation of polymer-filled vias [50], and photodefinition of polymer-filled vias with a temporary release film to fabricate coaxial TSVs [42]. The photodefinition process (using SU-8 [41]) combined with the TSV fabrication process with mesh (Figure 11) is explored in this research. To better differentiate the polymer cladding fabrication processes, a comparison is shown in Table 1.

#### *2.1.2.2 Survey of TSV Stress Reduction Using Polymer Liners*

The thick liners fabricated using polymers with low Young's modulus can reduce TSV thermomechanical stress by acting as a cushion layer between the copper and the silicon. Various modeling results have been shown for TSVs with thick polymer liners demonstrating a reduction in TSV stresses. Using a 5 $\mu$m thick BCB stress buffer layer for 30 $\mu$m diameter vias, S. K. Ryu et al. [51] have shown a significant reduction in radial and shear stress along Cu/BCB and BCB/Si interfaces compared to Cu/Si interface. Using Parylene as a liner, Z. Chen et al. [52] have shown that normal stresses in copper, dielectric and silicon are lower for the TSVs with a Parylene liner compared to the TSVs with silicon dioxide liner; when the Parylene thickness is increased from 1 $\mu$m to 15 $\mu$m, the normal stresses in copper, dielectric and silicon are reduced by half.

Table 1: Comparison of TSV polymer cladding fabrication processes.

| | Fabrication Method | Principle | Benefit | Limitation |
|---|---|---|---|---|
| **1** | **Vapor deposition** [48] | Deposition of parylene | Deposition at room temperature | Limited cladding thickness |
| **2** | **Circular trench polymer filling** [49] | Polymer filling in etched circular trench followed by removal of silicon from center | Flexibility in polymer material selection | High aspect-ratio polymer filling may be difficult |
| **3** | **Laser ablation** [50] | Serial ablation of polymer filled in vias | Panel-scale fabrication possible | Serial process and precision of ablation |
| **4** | **Photodefinition with a release film (for coax TSVs)** [42] | Photodefinition of polymer-filled vias with a temporary release film at the base | Knowledge of high aspect-ratio photodefinition easily available in the literature | Temporary release film needed to support polymer and limited selection of high aspect-ratio photodefinable materials |
| **5** | **Photodefinition with mesh (The concept presented in this research)** | Photodefinition of polymer-filled vias with a mesh layer at the base | Knowledge of high aspect-ratio photodefinition easily available in the literature, and mesh helps for void-free polymer filling and bottom-up electroplating | Limited selection of high aspect-ratio photodefinable materials |

#### 2.1.2.3 *Survey and Analysis of TSV Dielectric Capacitance Reduction Using Polymer Liners*

Thick polymer liners help attain lower TSV dielectric capacitance and high-frequency loss compared to the thin (<1 $\mu$m) silicon dioxide liners. The reduction in TSV dielectric capacitance is primarily due to the greater thickness of the polymer dielectric liners with lower relative dielectric constants compared to silicon dioxide [53], which in turn helps reduce TSV loss [54]. To better understand the dielectric capacitance reduction using polymer liners (considering SU-8 and Parylene-C as the polymer liner materials in this research), a comparison is shown in Figure 12 using Equation 4 [55], as follows:

$$C_{liner} = \frac{2\pi\epsilon_{liner}}{\ln\left(\frac{radius_{coppervia} + thickness_{liner}}{radius_{coppervia}}\right)}. \tag{4}$$

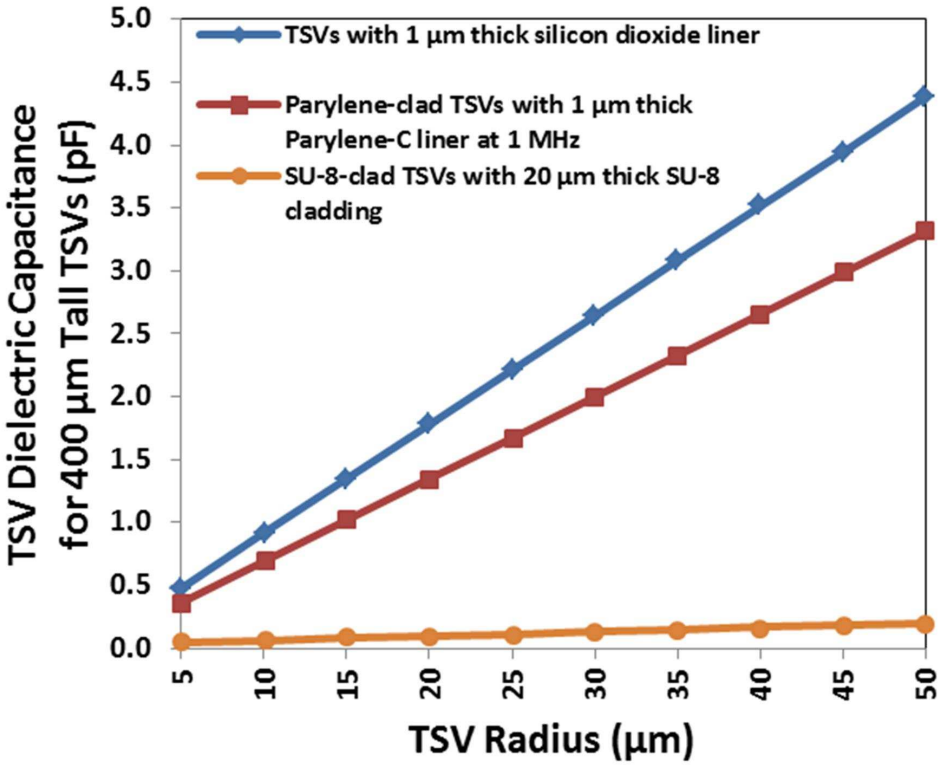



Figure 12: Comparison of TSV dielectric capacitance.

The relative dielectric constants of silicon dioxide, Parylene-C and SU-8 are 3.9, 2.95 (at 1 MHz) and 3, respectively [56–59]. In the literature, the dielectric constant of SU-8 has been reported between 3 and 4 [58, 59]. To calculate the best case capacitance reduction, a dielectric constant of 3 was selected for SU-8. While a thin Parylene liner reduces TSV dielectric capacitance as shown in Figure 12, the use of a thick SU-8 liner results in a significant reduction in the TSV dielectric capacitance. A 400 $\mu$m tall and 80 $\mu$m diameter copper via has a dielectric capacitance of 0.165 pF and 3.515 pF when the liner is 20 $\mu$m thick SU-8 and 1 $\mu$m thick silicon dioxide, respectively.

### 2.1.3 Optical TSVs

In addition to electrical interconnections, a key motivation for the integration of optical paths is that the electrical interconnections have become a bottleneck for low-power off-chip communications over longer distances owing to their high parasitics (such as resistance and capacitance). Whereas, optical interconnections do not suffer from resistive and capacitive losses and can consequently yield high-speed off-chip signaling with enhanced integrity. For long-distance intra-rack and rack-to-rack compute nodes in high-performance computing systems, 850 nm vertical-cavity surface-emitting laser (VCSEL) based parallel optical modules are commonly implemented [40]. The VCSEL-based links have been demonstrated in the literature with a data rate up to 56.1 Gbps, and high energy efficiency of 1.37 pJ/bit at 15 Gb/s and 3.6 pJ/bit at 25 Gb/s; an individual VCSEL device energy consumption being as low as 100 fJ/bit [60].

Optical TSVs in silicon interposers integrated with VCSEL-based parallel transceivers can help provide high-bandwidth and low-energy data transmission for long-distance interposer-to-interposer communications. In order to fabricate the optical TSVs, either vias could be etched in silicon and kept empty (as etched holes) or the etched vias

could be filled with a material capable of providing low-loss optical transmission, as described follows: (1) F. E. Doany et al. [61] have demonstrated an optical transciever module using 150 $\mu$m diameter etched holes for optical connectivity through a 150 $\mu$m thick silicon interposer; and (2) Polymer filled optical vias have been demonstrated by K. Oda et al. and Y. Takagi et al. [62, 63]. The latter approach is explored in this research using SU-8 [41] to fabricate optical TSVs simultaneously with the TSVs consisting of thick photodefined polymer liners. SU-8 is utilized in this research since it has been shown as a promising material in the literature for optical waveguides [64].

In addition to the VCSEL-based communication, silicon photonics based communication has been widely explored in the literature due to (1) high scalability of the silicon photonic interconnections; (2) possibility of lower cost due to compatibility with CMOS fabrication processes; and (3) demonstrations of ultra-compact ring devices with wavelength division multiplexing (WDM) [60]. Exploration of optical TSVs with silicon photonics in the future could enable highly scalable high-performance computing systems.

## *2.2 Fabrication of TSVs with Vapor Deposited Parylene Liner*

First, the technology development of Parylene-clad TSVs with vapor deposited Parylene-C liners is demonstrated using the mesh process [45] with bottom-up copper electroplating. The fabrication process for the Parylene-clad TSVs begins with the deposition of silicon dioxide on the back side of a silicon wafer, as shown in Figure 13.

Next, using the BOSCH process [65], vias are etched in the silicon; a negative photoresist (Futurrex) mask is used during the BOSCH process. Once the vias are etched, a pattern of microvias (called mesh [45]) is formed in the silicon dioxide suspended membrane at the base of the vias. After mesh fabrication, Parylene-C is deposited over the etched vias using vapor deposition at room temperature to obtain a 2.25 $\mu$m thick conformal coating. Parylene blocking in meshes is etched using oxygen plasma,

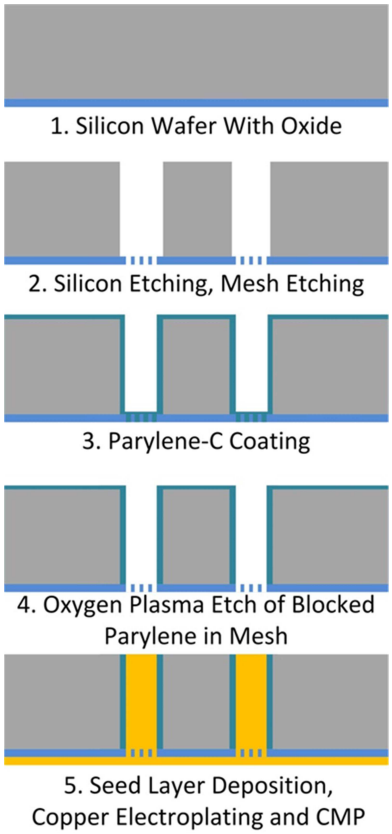
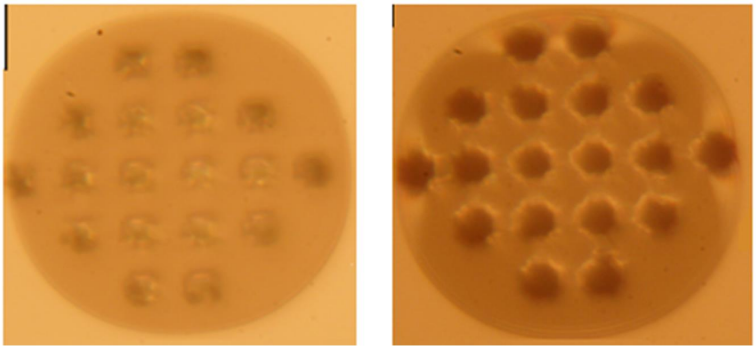
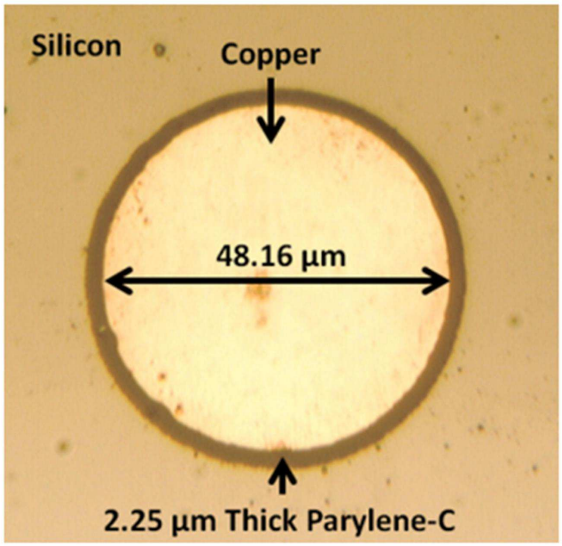



Figure 13: Fabrication process of parylene-clad TSVs.

as shown in Figure 14(a). Once the Parylene blocking is removed, a titanium-copper seed layer is deposited on the mesh side. The titanium layer is used to obtain adhesion between the copper and the silicon dioxide. After seed layer deposition, the mesh is pinched-off using copper electroplating followed by bottom-up copper electroplating of the Parylene-clad vias using Microfab DVF 200 MU solution from Enthone. Additional copper at the end of the bottom-up electroplating is removed using CMP with the iCue 5001 slurry from Cabot Microelectronics Corporation. Using this fabrication process, 390 $\mu$m tall and $\sim$48 $\mu$m diameter copper TSVs surrounded by a $\sim$2.25 $\mu$m thick Parylene-C cladding were fabricated, as shown in Figure 14(b).



(a)




(b)

Figure 14: Parylene-clad TSV processing results (a) after mesh fabrication and Parylene-C deposition (left) and after oxygen plasma etch of Parylene blocking (right), and (b) after CMP showing the top view of the fabricated 390 $\mu$m tall Parylene-clad TSVs with $\sim$48 $\mu$m diameter copper vias surrounded by a $\sim$2.25 $\mu$m thick cladding.

## *2.3 Fabrication of TSVs with Thick Photodefined Polymer Liner*

To fabricate thick (~20 $\mu$m) polymer liners, SU-8 is used because it can provide high aspect-ratio photodefined structures with relative ease compared to other photodefinable materials [41]. Thick SU-8 cladding can provide a reduction in TSV losses as well as a reduction in TSV stresses since the Young's modulus of SU-8 (4.02 GPa) is lower relative to that of copper and silicon [41]. The 20 $\mu$m liner thickness is selected since the maximum Von-Mises stresses in silicon at the liner-silicon interface show a minimal change with the SU-8 liner thickness beyond 15 $\mu$m for the 80 $\mu$m diameter copper vias explored in this research (as observed from preliminary ANSYS simulations at 200 °C).

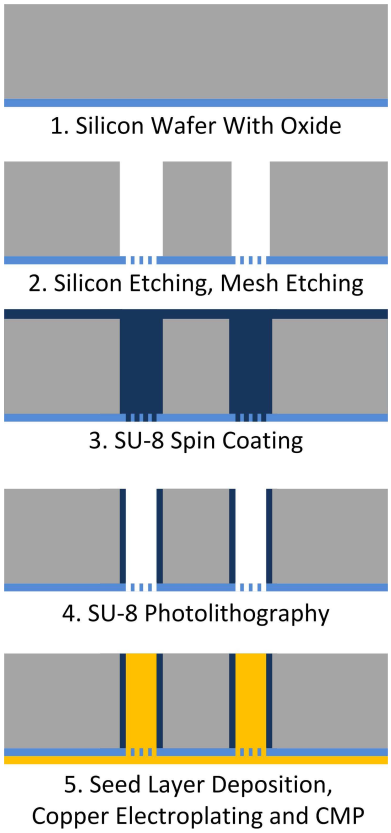



Figure 15: Fabrication process for photodefined polymer-clad TSVs.

As shown in Figure 15, the fabrication process for polymer-clad TSVs begins

with the deposition of silicon dioxide on the back side of a silicon wafer similar to the Parylene-clad TSVs, followed by via etching and mesh fabrication. Next, SU-8 is spin coated to fill the vias. Following a soft bake, the SU-8-filled vias are optically defined using UV exposure (i-line with 365 nm wavelength) followed by a post exposure bake and SU-8 development to yield SU-8-clad vias, as shown in Figure 16. The optical definition is performed with exposure from the mesh end of the vias since it is smoother compared to the non-mesh end of the vias. Once the SU-8 cladding is fabricated, a titanium-copper seed layer is deposited on the mesh side similar to the Parylene-clad TSVs, followed by mesh pinch-off, bottom-up copper electroplating and CMP.

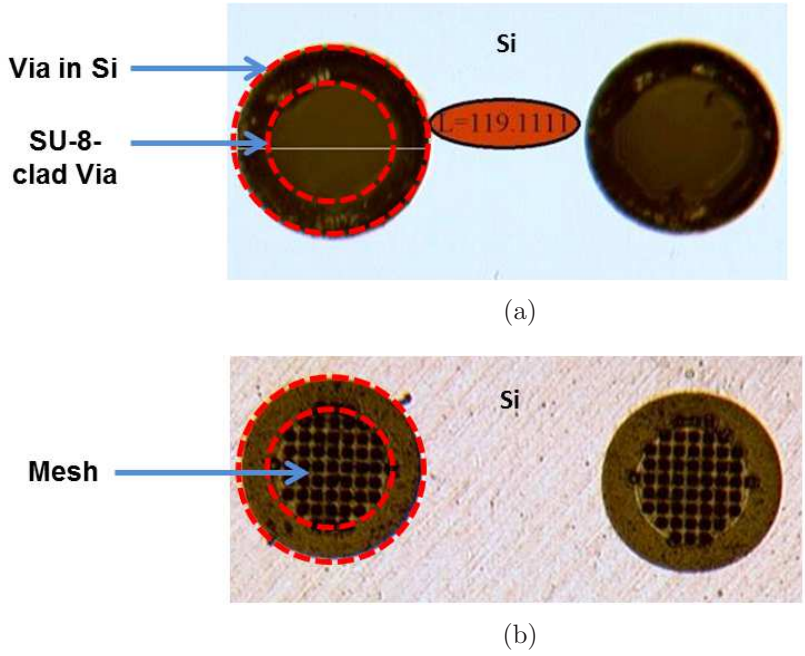
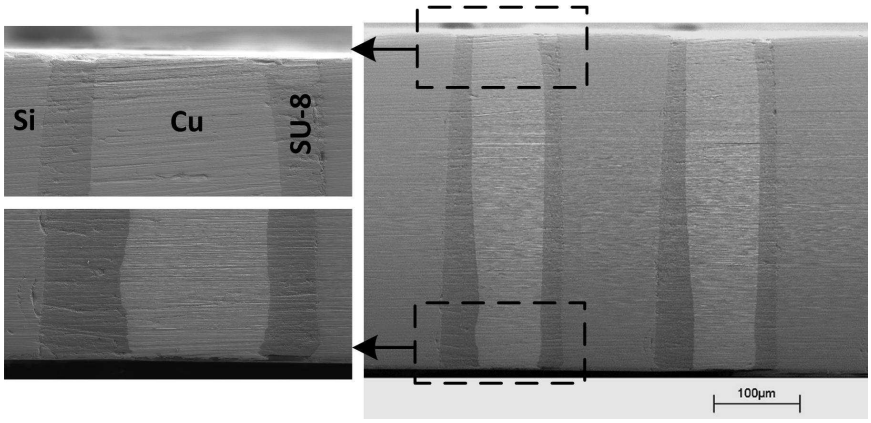
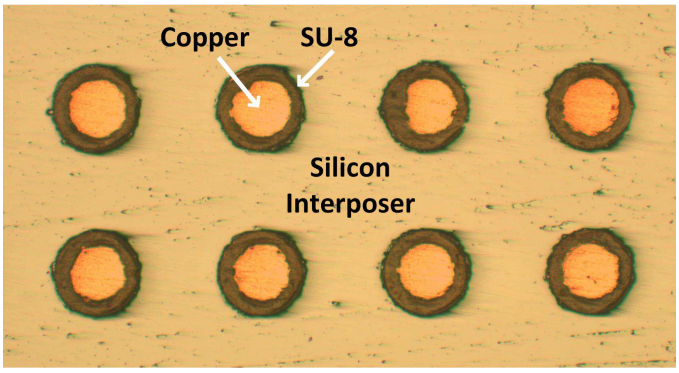



Figure 16: Fabricated 390 $\mu$m tall SU-8-clad vias with ~80 $\mu$m diameter openings and ~20 $\mu$m thick cladding on a 250 $\mu$m pitch: (a) Top view and (b) Base view.

As shown in Figure 17(a) and Figure 17(b), 390 $\mu$m tall copper TSVs with ~80 $\mu$m diameter and surrounded by a ~20 $\mu$m thick SU-8 cladding were fabricated on a 250 $\mu$m pitch. Void-free copper electroplating was obtained, as shown in the x-ray image (Figure 17(c)) of the fabricated polymer-clad TSVs.




(a)

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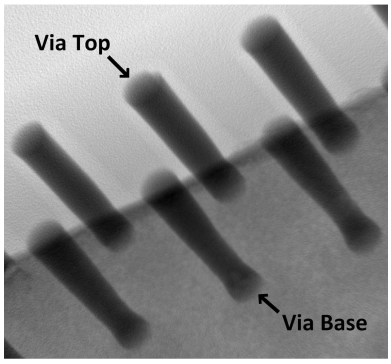
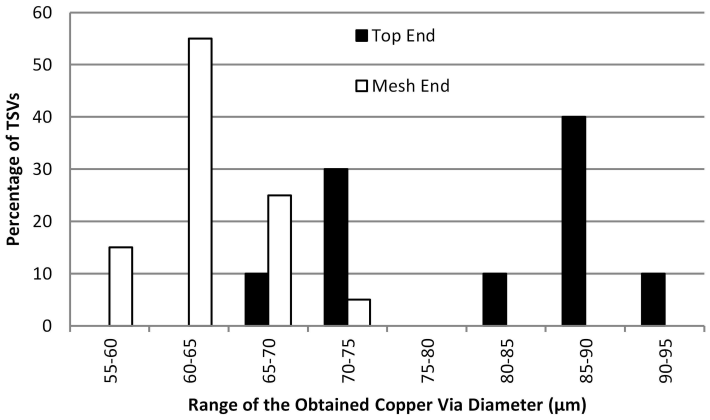



(c)




(d)

Figure 17: Fabricated 390 $\mu$m tall SU-8-clad TSVs with ~80 $\mu$m diameter copper vias surrounded by a ~20 $\mu$m thick cladding on a 250 $\mu$m pitch: (a) Cross section view; (b) Top view; (c) X-ray image showing void-free copper electroplating; and (d) Distribution of the obtained copper via diameters of 20 measured polymer-clad TSVs.

Figure 17(d) illustrates the distribution of the fabricated copper via diameters using the described photodefinition process. The average measured copper via diameter at the top (non-mesh) end is 81 $\mu$m with a standard deviation of 8.3 $\mu$m, and the average measured copper via diameter at the mesh end is 63.5 $\mu$m with a standard deviation of 3.4 $\mu$m. Further process optimization would address this issue.

## *2.4 Optical TSVs*

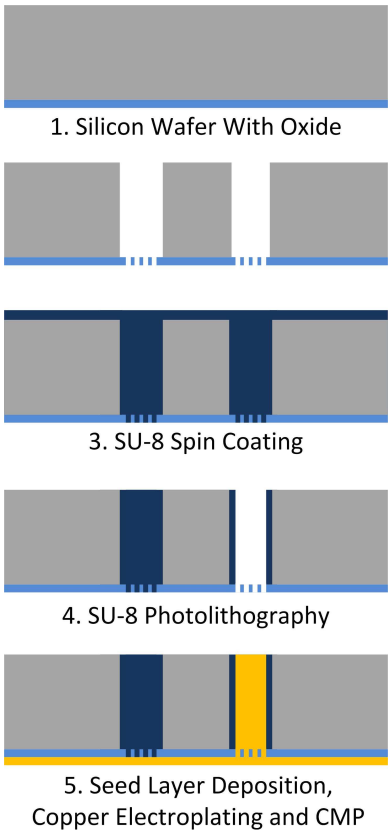



Figure 18: Fabrication process for simultaneous fabrication of photodefined optical and polymer-clad TSVs.

As shown in Figure 18, optical TSVs can be fabricated simultaneously with polymer-clad TSVs using the same photodefinable polymer (SU-8). Since SU-8 has good optical transmission characteristics in the window of 850 nm wavelength, and optical interconnects have been demonstrated using SU-8 [64], it has been selected as the core of the optical TSVs; silicon dioxide is used as the cladding to obtain total

internal reflection.

With respect to the fabrication of optical TSVs, the etched vias in silicon are filled with SU-8, followed by SU-8 soft bake similar to the fabrication of polymer-clad TSVs. However, during the UV exposure step for the polymer-clad TSVs, the polymer-filled vias intended for optical TSVs are simply flood exposed. Since SU-8 is negative tone, the polymer remains in the flood-exposed vias at the end of the SU-8 development, yielding the optical TSVs. As shown in Figure 19, 390 $\mu$m tall optical TSVs were fabricated with a 118 $\mu$m diameter SU-8 core surrounded by a 2 $\mu$m thick silicon dioxide cladding.

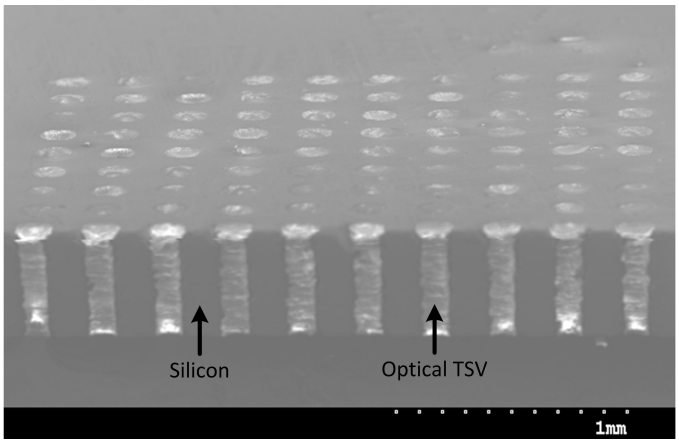



Figure 19: Fabricated 390 $\mu$m tall optical TSVs with a 118 $\mu$m diameter SU-8 core surrounded by a 2 $\mu$m thick silicon dioxide cladding on a 250 $\mu$m pitch.

## *2.5 Mesh-less High Aspect Ratio Via Filling Process for Polymer-clad TSVs*

The fabrication of polymer-clad TSVs with a thick photodefined SU-8 liner was shown earlier in the chapter (Figure 17). After spin coating of SU-8, the mesh at the base of the vias assists fill the vias without voids or air gaps. To prevent any possible leakage from the mesh end of the TSVs during the SU-8 soft bake, a commercial Blue Spinner Strip from the Semiconductor Equipment Corporation was pasted over a hot plate (leaving the non-sticky side on top) before placing the TSV wafer over the hot

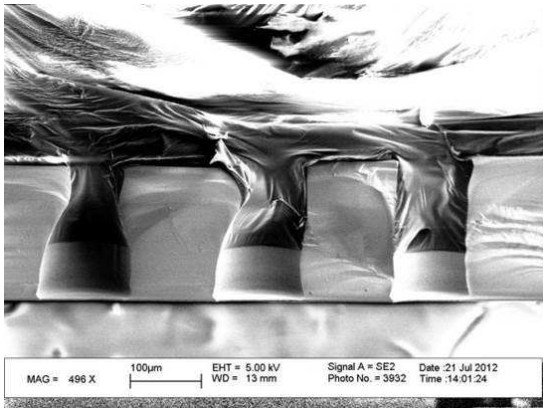
plate. To prevent damage to the silicon dioxide mesh layer at the end of the soft bake during wafer release, the TSV wafer was heated for a short time and it was released safely. The wafers used for the fabrication were 100 mm in diameter.

However, the implementation of this photodefined polymer-clad TSV technique with mesh may be difficult for larger diameter wafers in real-life manufacturing. This difficulty may result because the safe release of a large wafer from the Blue Spinner Strip may be difficult after the soft bake. Moreover, the warpage of a larger wafer may also cause leakage of SU-8 in certain areas making the following steps challenging. To address these challenges, exploration of a mesh-less polymer-clad TSV fabrication process with void-free filling of SU-8 in etched vias (closed at the base) is necessary.

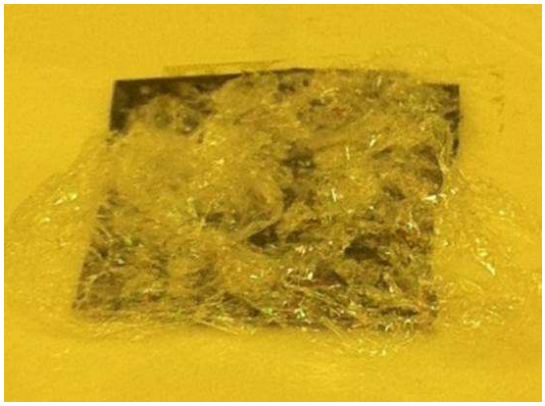
Void-free polymer filling has been described in the literature for vias in silicon with a closing at the base using a longer waiting time after polymer covering on the vias, and with a vacuum-assisted process [66, 67]. Implementing the longer waiting time technique may not yield a void-free filling when using SU-8 with greater viscosities (needed for polymer-cladding with lower shrinkages) and the vacuum-assisted technique may damages SU-8, as described next in the chapter. Thus, robust SU-8 filling methods are needed for high aspect-ratio vias with their bases covered.

To obtain SU-8-filled vias, silicon dioxide is deposited at the base of a silicon wafer followed by the etching of vias using the BOSCH process. The following experiments are then performed to attain high aspect-ratio SU-8 via filling:

- First, SU-8 is dispensed over a sample with 120 $\mu$m diameter and 200 $\mu$m tall vias on a 250 $\mu$m pitch. The sample is then placed on a flat surface at room temperature for six hours. Next, the sample is soft baked and a cross-section image is obtained, as shown in Figure 20(a). The vias cannot be filled by capillary action and gravitational force alone. The via cross section is obtained using only a diamond scriber cleaving to show the via status without accumulated dirt at the base of the vias.




(a)



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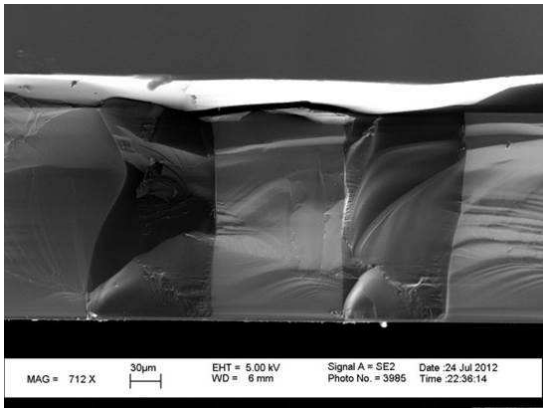


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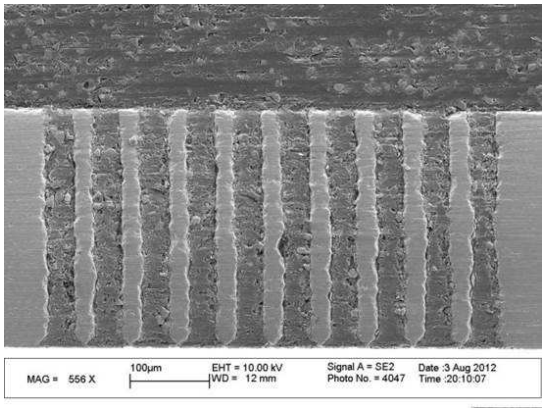



(d)

Figure 20: SU-8 filling experiments for vias in silicon with a silicon dioxide layer at the base: (a) 120 $\mu$m diameter and 200 $\mu$m tall vias on a 250 $\mu$m pitch in silicon after SU-8 dispensing, a 6 hour wait and soft bake; (b) A silicon sample with 120 $\mu$m diameter and 200 $\mu$m tall vias on a 250 $\mu$m pitch after SU-8 dispensing and vacuum processing; (c) 120 $\mu$m diameter and 200 $\mu$m tall vias on a 250 $\mu$m pitch in silicon after SU-8 dispensing, heat treatment in a vacuum oven, vacuum processing in the oven, cooling and soft bake; and (d) 30 $\mu$m diameter and 300 $\mu$m tall vias on a 60 $\mu$m pitch in silicon after SU-8 dispensing, heat treatment in a vacuum oven, vacuum processing in the oven, cooling and soft bake.

- For the next sample, SU-8 is dispensed over the 120 $\mu$m diameter vias and the sample is placed inside a vacuum oven at room temperature. Next, the vacuum oven pressure is reduced slowly. With this experiment, SU-8 suffers damage possibly due to bubble explosions during the vacuum treatment, as shown in Figure 20(b).

- Learning from the previous two experiments, SU-8 is dispensed over the 120 $\mu$m diameter vias but the sample is first placed inside the vacuum oven at room pressure and temperature. The oven is then heated to 110 °C followed by a pressure reduction. The sample is heated in the oven for 10 minutes followed by a ramped cooling. SU-8 soft baking is then performed and a cross-section image is obtained, as shown in Figure 20(c), demonstrating a void-free filling. Moreover, SU-8 filling is also obtained for 30 $\mu$m diameter and 300 $\mu$m tall vias on a 60 $\mu$m pitch, as shown in Figure 20(d), where the image is obtained after cross section polishing.

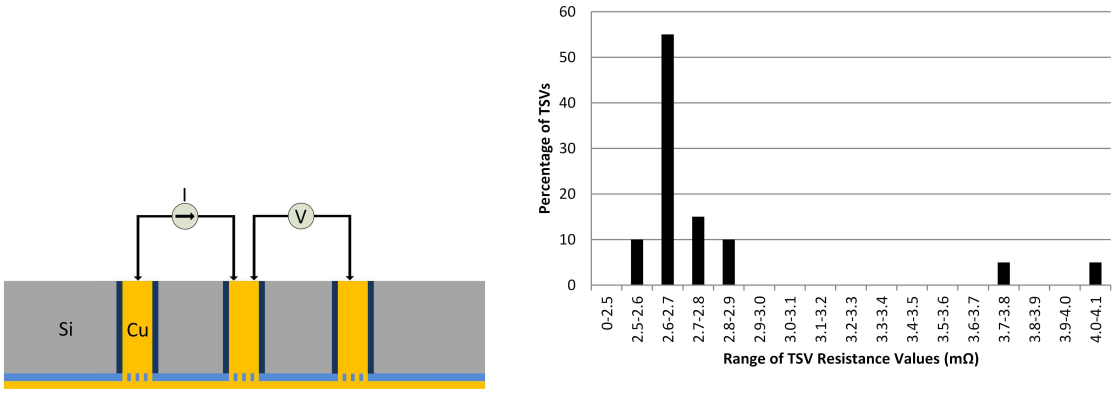
The high aspect-ratio SU-8-filled vias can assist leakage-free fabrication of polymer-clad TSVs in large-diameter wafers. Moreover, they can help reduce TSV coupling [68] and loss, and also be used as high-density optical TSVs (with a silicon dioxide liner cladding).

## *2.6 Resistance and Optical Loss Measurements*

Four-point resistance measurements were performed for the fabricated SU-8-clad TSVs, as shown in Figure 21. The average measured resistance of 20 different SU-8-clad TSVs with ~80 $\mu$m diameter copper vias is 2.81 m$\Omega$. Figure 21(b) illustrates the distribution of the measured polymer-clad TSV resistances.

For the optical loss measurements of the fabricated optical TSVs, an experimental setup was established, as shown in Figure 22(a). Input to an optical TSV was provided from an 830 nm wavelength laser source using a single mode optical fiber. The output power from the optical TSV was measured using a photodetector held on the other end of the optical TSV.

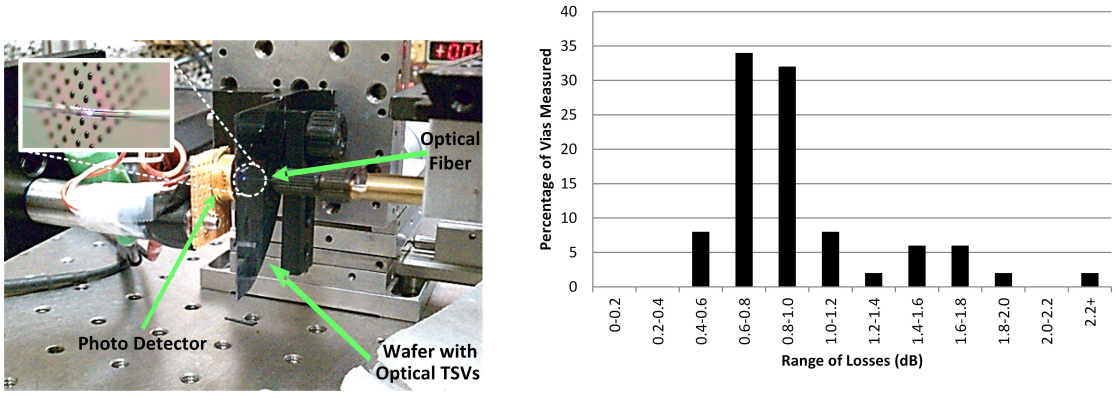
For a large number of the fabricated 390 $\mu$m tall and 118 $\mu$m diameter SU-8 core optical TSVs (2 $\mu$m thick silicon dioxide cladding), the average measured optical loss is 0.59 dB with a standard deviation of 0.15 dB. Figure 22(b) illustrates the




(a) (b)

Figure 21: Four-point resistance measurements of the fabricated polymer-clad TSVs: (a) Four-point resistance measurement setup and (b) Distribution of the measured resistance values.

distribution of the measured optical losses of the fabricated optical TSVs. Moreover, the average measured optical loss was found to be the same when the measurements were performed by reversing the wafer demonstrating symmetric losses as expected. Previous work on optical vias have measured higher insertion loss for similar sized vias [62, 63].




(a) (b)

Figure 22: Optical loss measurements for the fabricated optical TSVs: (a) Setup to measure optical loss of the fabricated optical TSVs with an inset image showing optical fiber in contact with an optical TSV and (b) Distribution of the measured optical losses.

## *2.7 TSV Strain Measurements Using Synchrotron XRD*

State-of-the-art TSVs with thin (<1 $\mu$m) silicon dioxide liner have thermomechanical reliability issues since copper expands almost seven times more than silicon when a thermal load is applied. The TSV stresses can be reduced using a thick polymer liner. However, characterization of the TSV stress with comparison between different types of TSVs is challenging. Prior efforts in TSV stress/strain measurements for understanding TSV reliability include micro-Raman spectroscopy, bending beam technique, indentation, and XRD, as shown in Table 2.

Table 2: Comparison of TSV stress measurement techniques in the literature.

| | **Techniques** | **Principle** | **Benefit** | **Limitation** |
|---|---|---|---|---|
| **1** | **Micro-Raman spectroscopy [69, 70]** | Frequency shift measurement of an impinging laser | Localized near surface Si stress measurement | Stress in copper cannot be measured |
| **2** | **Bending beam technique [71]** | Curvature measurement | Stress measurement in Si and Cu | Averaged stresses obtained |
| **3** | **Indentation [72]** | Residual-stress-induced normal load measurement | Stress measurement in Si and Cu | Requires a known stress-free state |
| **4** | **Synchrotron XRD [73]** | Raster scanning under a micro focused x-ray beam | Stress measurement in Si and Cu with minimum destruction | Challenging data interpretation |

Micro-Raman spectroscopy works on the principle of measuring the frequency shift of an impinging laser to quantify localized near surface silicon stress [69, 70].

However, stresses in copper cannot be measured using micro-Raman spectroscopy. The bending beam technique works on the principle of measuring the curvature of the sample to quantify the stress in silicon and copper [71]. However, the measured stresses obtained from using the bending beam technique are averaged across the sample. Indentation techniques work on the principle of analyzing the residual-stress-induced normal load to measure localized stress in silicon and copper [72]. However, it is difficult to measure residual stress in the absence of a known stress-free state using the indentation techniques. Synchrotron XRD can measure all the stress components in a copper via and the surrounding silicon with minimal destruction to the sample.

XRD is a commonly used technique to study structural properties of materials [74]. With the development of high-brilliance synchrotron sources, advanced x-ray focusing optics and diffraction-pattern analysis codes, diffraction patterns can be obtained by using sample scans under a submicrometer polychromatic (white x-ray beam) or monochromatic beam. This can provide crystal orientations and strain distribution maps (both deviatoric and hydrostatic) in localized areas with the ability to distinguish the maps for specific materials. Consequently, for structures like TSVs, synchrotron XRD can help obtain separate strain distributions for silicon and copper. Due to this capability, minimum destruction is needed to the TSV samples for the synchrotron measurements. However, data interpretation is challenging for thick structures. Raster scanning the sample under a micro focused x-ray beam provides a 2D strain distribution map of the sample, whereas the strain distributions in TSVs are 3D in nature. How the strain distribution along the x-ray penetration depth direction is averaged and projected is a complicated matter because it involves the depth-dependent attenuation of x-ray energy and the influence of different materials along the path. The understanding of the strain averaging and projection may not be an issue for thin structures [75, 76], however, it is essential for the interpretation of measurement results of thick samples such as silicon wafers with embedded copper

TSVs, and it is explored in this research.

Using synchrotron XRD, deviatoric strains are obtained for TSVs and analyzed for silicon in this research since the aim is to compare the strains for the TSVs with silicon dioxide liner and polymer-clad TSVs. The obtained synchrotron XRD strain measurements are 2D, whereas the TSV strains are 3D. A beam intensity based data averaging method, relating the synchrotron XRD measurements and finite-element modeling (FEM), is demonstrated in order to interpret the measured TSV strains. To compare the strains in the TSVs with silicon dioxide liner and polymer-clad TSVs, an indirect method of FEM calibration using synchrotron measurements is demonstrated. The synchrotron XRD tests were carried out on beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL).

**Sample preparation and measurement setup:** For preliminary TSV measurements using synchrotron XRD, 50 $\mu$m diameter and 300 $\mu$m tall TSVs were fabricated with 1 $\mu$m thick silicon dioxide liner on a 150 $\mu$m pitch, as shown in Figure 23. The TSV fabrication technique with mesh and bottom up electroplating, as described earlier (Figure 11), was used to fabricate the TSVs with silicon dioxide liner. For the comparative characterization of polymer-clad TSVs and the TSVs with silicon dioxide liner, the fabricated polymer-clad TSV sample described earlier in the chapter (Figure 17) was utilized along with a TSV sample with the same copper via dimensions and 1 $\mu$m thick silicon dioxide liner. Moreover, to mimic the TSV behavior in electronic packages, a 50 $\mu$m thick copper layer was kept at the bottom of the TSVs to introduce a bending effect during temperature excursions. Additionally, since x-rays attenuate as they travel from materials, the TSV samples were cross-section polished until the silicon thickness approximately equal to half the separation between two TSVs was remaining. The TSV samples were then mounted on a heater setup as shown in Figure 24 followed by their positioning on a high precision beamline stage.

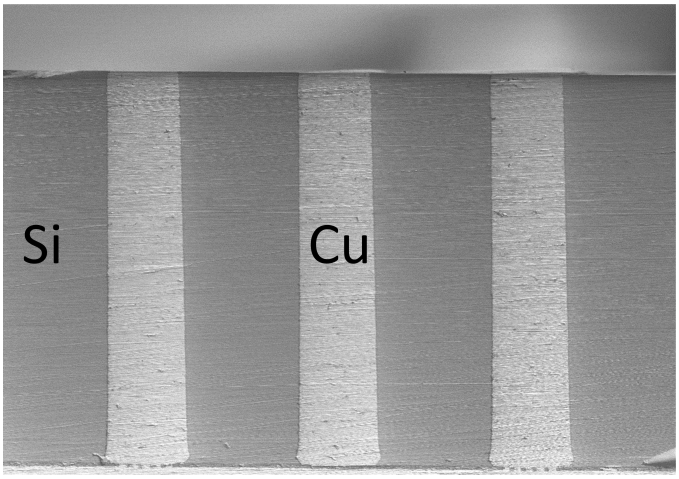
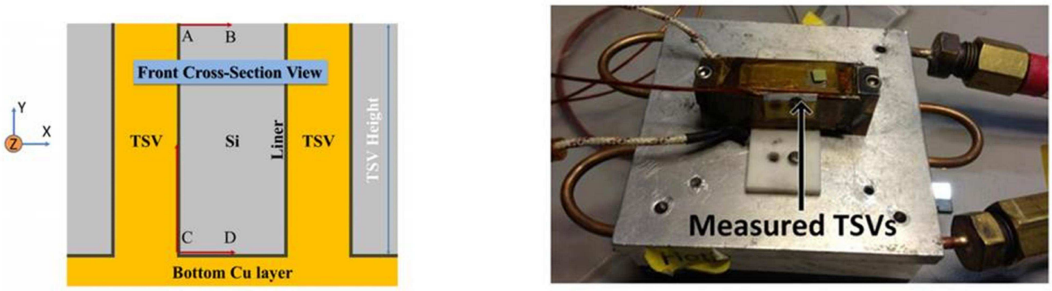


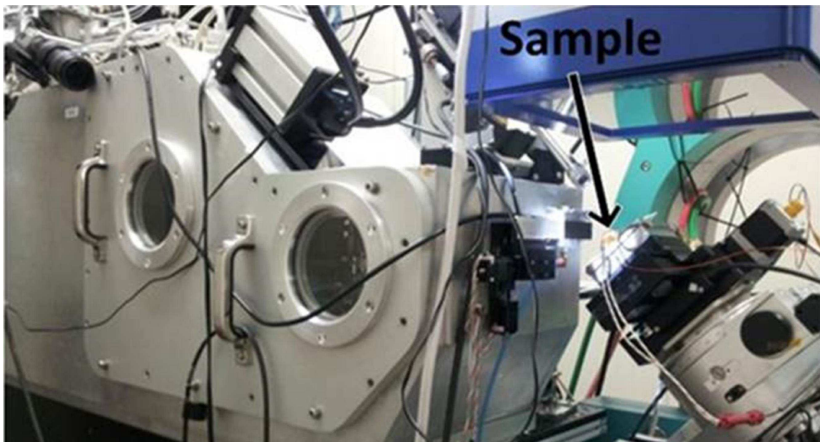

Figure 23: Fabricated 50 $\mu$m diameter and 300 $\mu$m tall TSVs with 1 $\mu$m thick silicon dioxide liner and on a 150 $\mu$m pitch.

**Measurement details:** Sample scans were conducted at 150 °C using a focused polychromatic x-ray (white) beam to measure the deviatoric strain distribution, followed by hydrostatic strain measurements of the TSV samples at multiple selected locations using monochromatic beam scans. However, since only limited information is obtained from the monochromatic scans of the selected locations, only the deviatoric strain distributions were analyzed for the entire TSV scanning plane. The x-ray beam was focused to a 1 $\mu$m size using a pair of elliptically bent Kirkpatrick-Baez mirrors (Figure 24). Laue pattern data analysis was carried out using the x-ray microdiffraction analysis software (X-MAS) to calculate all the strain components [74].

**Interpretation of measurements using FEM:** Since the obtained 2D strain maps using synchrotron XRD actually represent 3D strain distributions in the silicon surrounding the TSVs, an averaging method based on energy dependent beam absorption is proposed, as shown in Figure 25. In this method, the fluxes corresponding to the beam intensities in the silicon are calculated and then normalized to form the white beam intensity weight function. Simultaneously, finite element TSV array models are built with the same geometry and materials [41, 77] as the tested TSV samples.




(a) (b)

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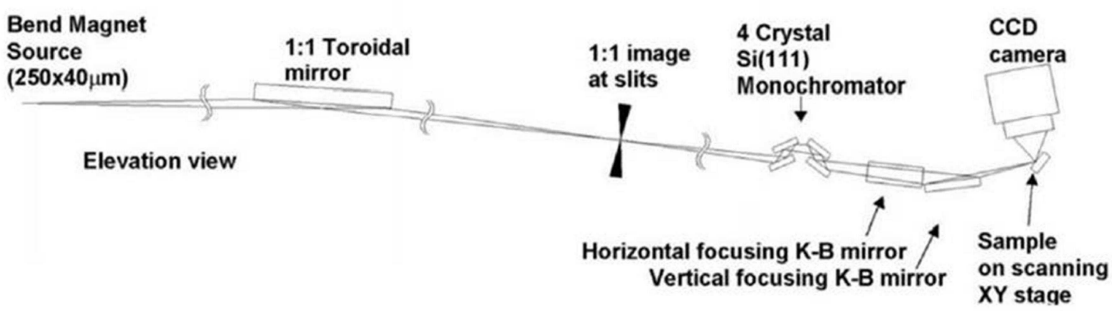



(d)

Figure 24: Synchrotron XRD setup for TSV strain measurements: (a) Schematic of the TSV area measured; (b) Setup of a TSV sample attached to a heater; (c) Beamline setup with the TSV sample; and (d) Schematic layout of the beamline [74].

To capture the process-induced stresses of the TSV samples, the thermal profiles of the fabrication processes are sequentially applied to the models. To mimic the sequential fabrication process, all the materials are activated sequentially at their process stress-free temperature through the ANSYS element birth-and-death approach.

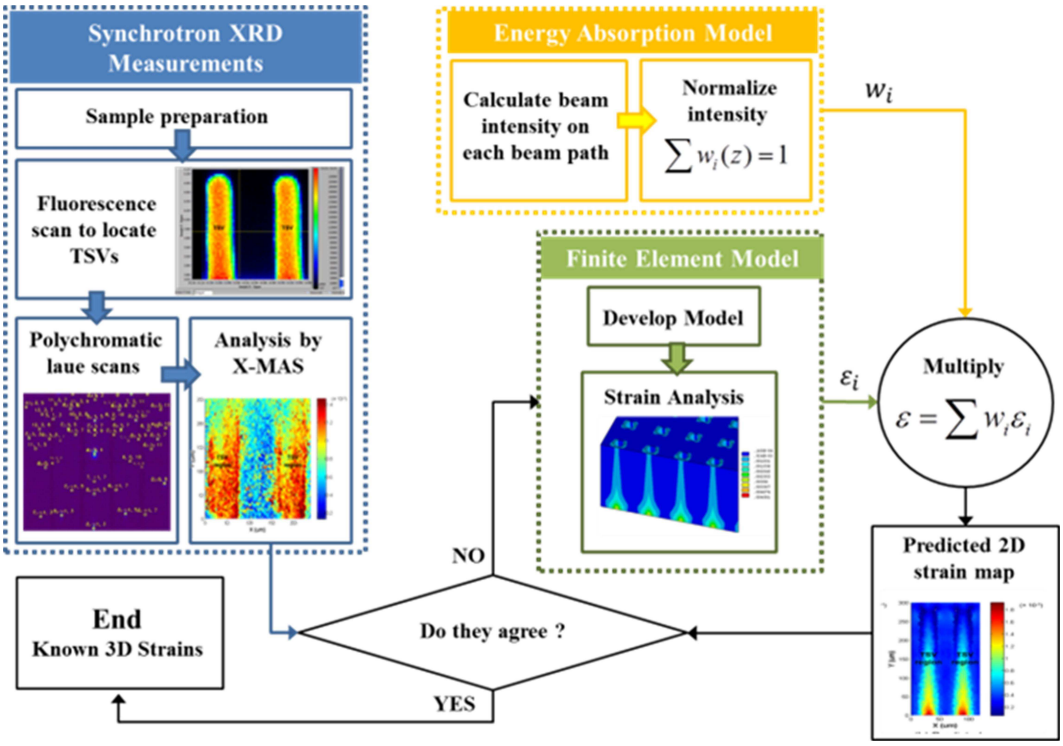



Figure 25: Beam intensity based data averaging method.

Thereafter, the deviatoric strains at 150 °C along the beam penetration direction are extracted and multiplied by the beam intensity based weight function to obtain a strain value at any given point on the scanning plane. This process is repeated until all the points on the scanning plane are covered to form a 2D strain map. The results from the measurements and the model are shown in Figure 26 for the fabricated 50 $\mu$m diameter and 300 $\mu$m tall TSVs with 1 $\mu$m thick silicon dioxide liner and on a 150 $\mu$m pitch. The comparison shows that the trends of the model results generally agree well with the strain measurement data, although with some discrepancies for various reasons. First, it was observed that while repeating the measurements on the same sample, a few of the measured values differed from the modeled values because of the stress history during the high-temperature measurements. However, the strain distribution trends remained unchanged. Second, the finite element model considers an ideal thermal loading case without accounting for the fabrication induced defects and copper grain coarsening during the fabrication.

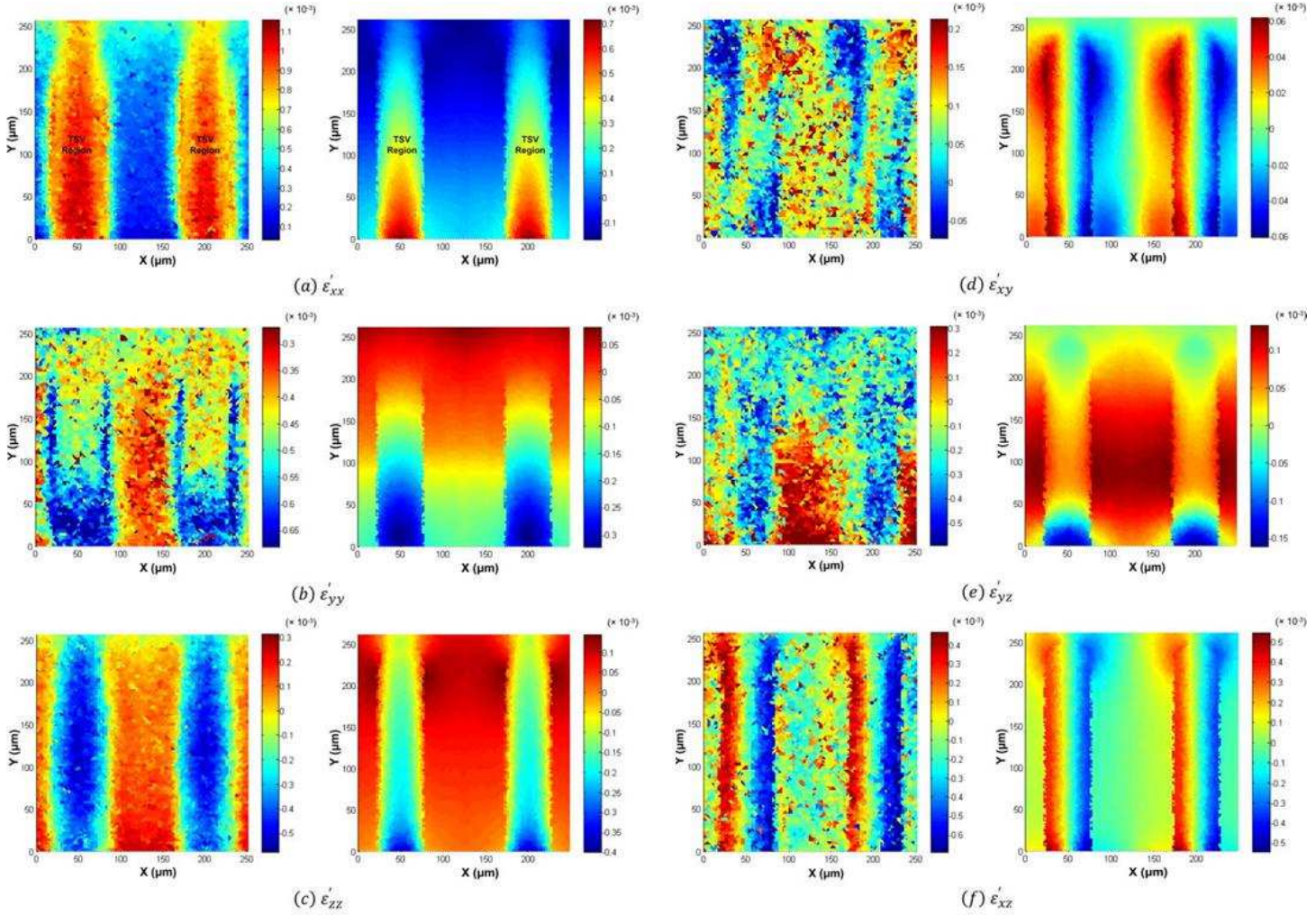
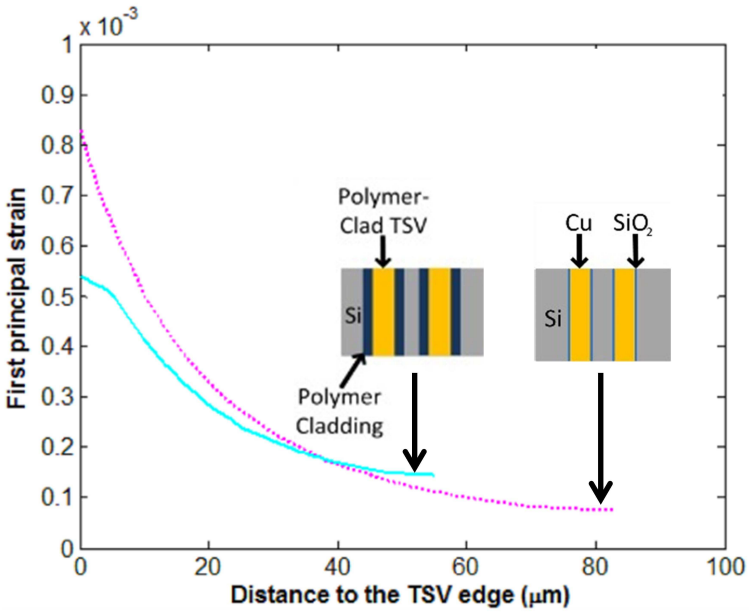



Figure 26: Measured deviatoric strain distribution maps of silicon (left) vs. model predicted strain maps (right) at 150 °C for the fabricated 50 $\mu$m diameter and 300 $\mu$m tall TSVs with 1 $\mu$m thick silicon dioxide liner and on a 150 $\mu$m pitch.

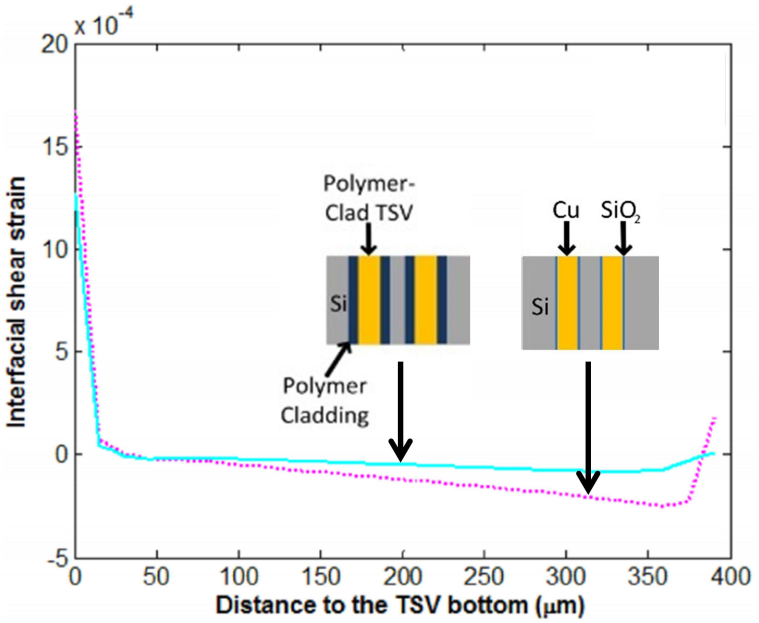
**Comparison of strain in TSV samples:** In the prepared TSV samples, a certain thickness of silicon was kept unpolished in front of the first row of TSVs to preserve the mechanical boundary condition. The front silicon thicknesses affect the measured 2D strain maps in several ways. First, the dimension dependent mechanical boundary conditions of the TSVs near the scanning plane change with varying front silicon thicknesses. Second, the different front silicon thicknesses affect the x-ray penetration depth and consequently affect the captured strain information along the penetration depth.

To address this issue, an indirect approach is applied by using the measured 2D strain distribution maps to calibrate a 3D finite element analysis (FEA) model. The calculated strain from the 3D FEA model is used to compare different TSV structures. To calibrate the 3D FEA models, the aforementioned beam intensity based data averaging method is applied to project the 3D strain distribution from the 3D FEA models onto 2D strain distribution maps. This allows a direct comparison between polymer-clad TSVs and the TSVs with silicon dioxide liner (Figure 27) where both consist of copper vias with the same dimensions.

Since the dominating TSV thermomechanical failure modes are comprised of silicon cracking and copper/liner separation, the first principal strain in the silicon and the copper/liner interfacial shear strain are compared. As shown in Figure 27(a), the thick SU-8 liner serves as a cushion layer and reduces the thermomechanical force applied to the surrounding silicon as the copper via expands at a high temperature. Moreover, the SU-8 liner mitigates the interfacial shear strain, and thus reduces the possibilities of interfacial separation, as shown in Figure 27(b). The higher interfacial shear strain near the bottom of the TSV is due to the presence of the copper layer.




(a)




(b)

Figure 27: At 150 °C, predicted (a) first principal strain of silicon at the top of TSVs along the path stretching radially away from the liner-silicon interface and (b) interfacial shear strain along copper/liner interface.

## 2.8 *Endpoint Detection for TSV Etching: Controlling TSV Critical Dimension*

For polymer-clad and optical TSVs, the silicon etching is performed using the BOSCH process, which consists of alternating etch and passivation cycles [65]. $SF_6$ is used as the reactive etch gas and $C_4F_8$ is used for fluorocarbon sidewall passivation. For given TSV dimensions, the number of etch cycles needs to be accurately determined during silicon via etching to avoid under-etching or over-etching at the base of the vias. In the case of over-etching, positive ions accumulate over the $SiO_2$ etch stop layer at the base of the vias causing repulsion to the incoming positive ion flux. The repelled incoming positive ion flux can attack the silicon sidewall at the base of the vias resulting in notching (as shown in Figure 28) [78]. The instant during an etching process when a material (silicon) is completely etched without under- or over-etching is called the etch endpoint, and the process of identifying the endpoint and terminating the etching is called endpoint detection (EPD). Correct detection of the etch endpoint in TSVs improves the control of the critical dimension.

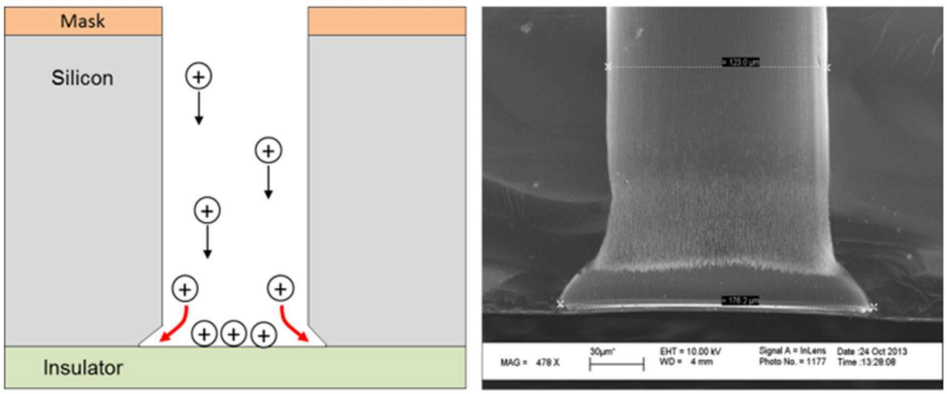



Figure 28: Notching mechanism in TSV fabrication using BOSCH process (Left) and cross-section of a 120 $\mu$m diameter via showing notching at the base (Right).

EPD has been shown in the literature for the etching of polymer films using a Langmuir probe [79], blanket polysilicon using laser interferometry [80], and chrome dry etching using RF sensors [81]. However, it is difficult to predict the endpoint

during TSV fabrication for two key reasons: (1) the BOSCH process used for silicon etching involves time division multiplexing (TDM) of etch and passivation cycles, requiring the incorporation of multiplexing in an EPD methodology; and (2) the aggregated TSV area typically consumes less than 1% of the die area, requiring an EPD methodology capable of detecting a very low quantity of etch byproducts.

The EPD for etching a silicon-on-insulator (SOI) wafer has been demonstrated by R. Westerman et al. by implementing an envelope follower algorithm using optical emission spectroscopy (OES) [82]. The EPD method using OES focuses on identifying the wavelength corresponding to a chemical species that shows a pronounced transition at the endpoint. However, the signals for demonstrating the envelope follower algorithm using OES utilized both the passivation and the etch steps. As a result, the envelope follower algorithm was influenced by the passivation step, where the $SiF_x$ (etch byproduct) intensity includes carbon noise from $C_4F_8$. Additionally, with respect to EPD for TSV etching using OES, low open areas and high TSV aspect ratios can result in extremely low signal-to-noise ratios (SNR) and a weak intensity of the selected wavelength to be detected.

To perform EPD during the etching of TSVs with low open areas and high aspect-ratios, a hybrid partial least squares-support vector machine (PLS-SVM) model is experimentally validated using OES that focuses solely on the silicon etch step during the BOSCH process. The steps for the EPD are shown in Figure 29 and are described in detail in [83].

TSV etching is performed in an STS inductively coupled plasma-reactive ion etch (ICP-RIE) system using the BOSCH process with an OES system installed on top of the process chamber, as shown in Figure 30.

The OES system used in this experiment is a Korea Spectral Products SM440 optical sensor. The optical fiber is fixed on to the topside quartz window view port of the chamber during the etching process to collect plasma glow discharge directly

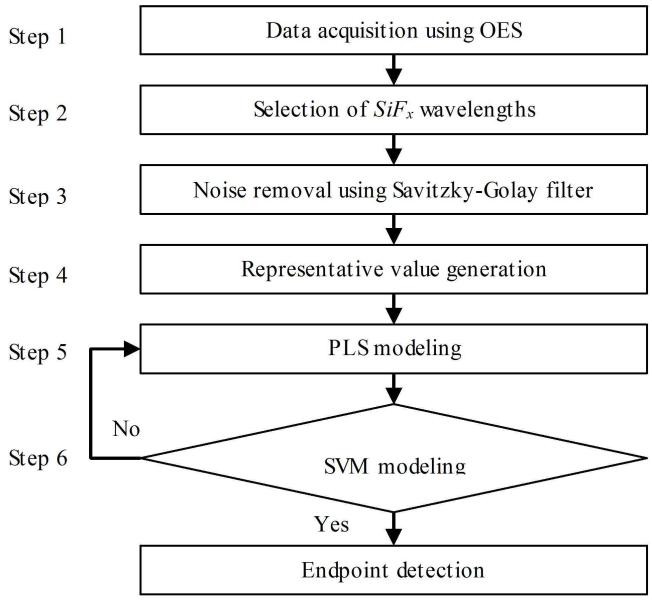



Figure 29: Flowchart of the proposed PLS-SVM model.

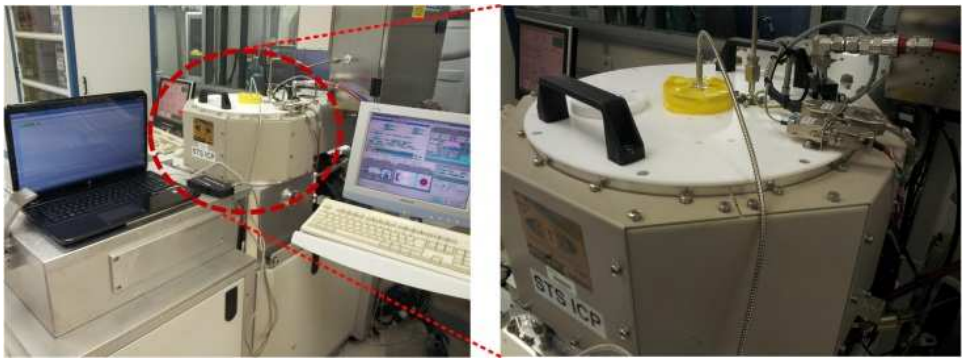
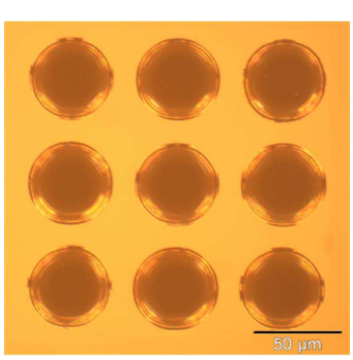


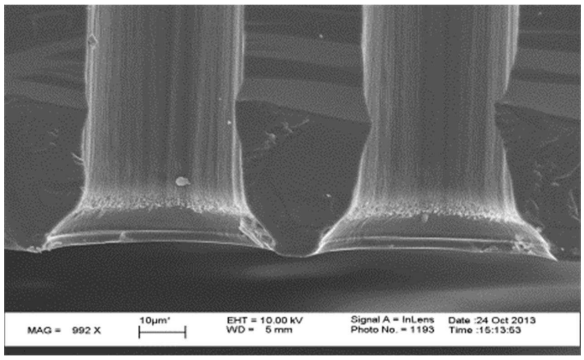

Figure 30: OES setup with sensor mounted on top of ICP etching tool process chamber (closer image shown on the right).

through a 300 $\mu$m diameter fiber with the detection range of 200 nm to 1050 nm. To fabricate the TSV sample wafer, a silicon dioxide layer is first deposited on the back side of an approximately 300 $\mu$m thick and 100 mm diameter silicon wafer, followed by etching from the top side of the wafer using a photoresist mask. To avoid wafer-to-wafer thickness variation in the samples for model establishment and verification, the TSV etching was performed on one half of the wafer initially, while keeping the rest of the wafer covered. Once the etching of the first half was completed, the second half was etched, guided by the EPD prediction to verify the accuracy of the suggested

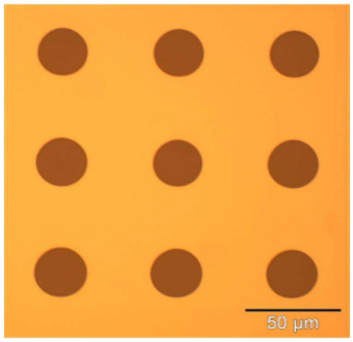
hybrid PLS-SVM model.



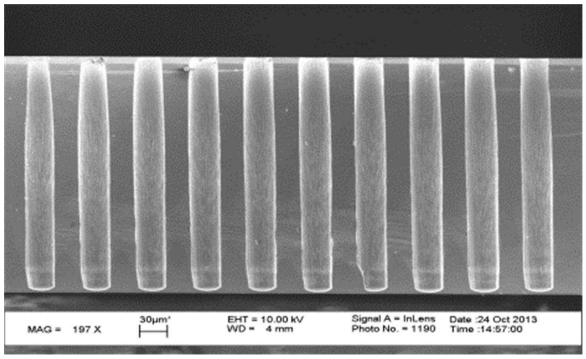

(a)




(b)




(c)




(d)

RESULTS OF THE TSVS BACK-TO-BACK ETCHING WITH 120, 80, AND 25 µm

| TSV Diam. (µm) | Wafer Half | Process Cycle | Average Diameter for 100 vias (µm) | | Variations between The Maximum and The Minimum Diameters (µm) | |
|---|---|---|---|---|---|---|
| | | | Top | Bottom | Top | Bottom |
| 120 | 1st | 350 | 128.9 | 175.7 | 6.90 | 8.96 |
| | 2nd | 222 | 123.7 | 121.1 | 3.75 | 4.37 |
| 80 | 1st | 420 | 84.72 | 122.85 | 5.96 | 12.21 |
| | 2nd | 390 | 83.11 | 79.54 | 3.98 | 6.54 |
| 25 | 1st | 650 | 29.61 | 48.39 | 1.84 | 5.43 |
| | 2nd | 624 | 28.87 | 28.20 | 1.5 | 3.81 |

(e)

Figure 31: Etching results for 300 $\mu$m tall vias with $\sim$25 $\mu$m diameter for EPD: (a) Optical image from base of the vias for the first half of a wafer; (b) SEM image of via cross section for the first half of the wafer; (c) Optical image from base of the vias for the second half of the wafer; (d) SEM image of via cross section for the second half of the wafer; and (e) Summary of the TSV etching results for the two wafer halves.

The hybrid model has been successfully validated for the EPD of TSVs with low open areas in their diameters of 120 $\mu$m, 80 $\mu$m and 25 $\mu$m. To verify these results, SEM analysis was conducted, and the results for the 25 $\mu$m diameter TSVs are presented in Figure 31. Moreover, the results of all the TSV samples are also tabulated in Figure 31. These results confirm the accuracy of EDP.

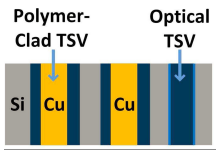
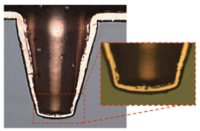
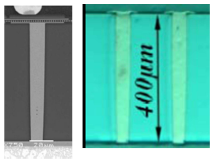
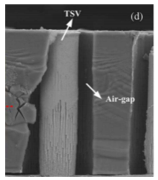
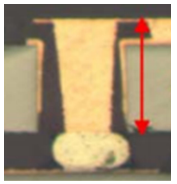
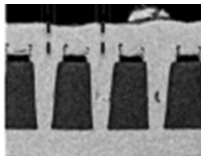
## *2.9 Technology Comparison and Chapter Conclusion*

Table 3 compares the photodefined polymer-clad TSVs with other competing TSV technologies from the literature [25, 30, 42, 46, 48, 84, 85]. The polymer-clad TSVs have dimensions similar to the TSVs with silicon dioxide liner for 400 $\mu$m thick silicon interposers. Moreover, the polymer-clad TSVs provide low stresses, dielectric capacitance and losses with a relative ease of fabrication. Additionally, the special features of the polymer-clad TSVs include their photodefinition assisted fabrication and parallel fabrication of optical TSVs.

In conclusion, this chapter has demonstrated the fabrication of TSVs with $\sim$20 $\mu$m thick photodefined SU-8 liners using a mesh-based TSV fabrication process. Moreover, the fabrication of polymer liners with vapor deposited Parylene-C was also demonstrated. Additionally, the fabrication of optical vias, which can be fabricated in parallel to the SU-8-clad TSVs, was demonstrated and the fabrication of high aspect-ratio SU-8 filled vias was shown to fabricate the SU-8-clad TSVs without a mesh at the base.

Resistance and synchrotron XRD strain measurements were demonstrated for the fabricated SU-8-clad TSVs. Moreover, optical loss measurements were shown for the fabricated optical TSVs. Lastly, endpoint detection using OES for TSV etching was demonstrated to experimentally validate a hybrid PLS-SVM model for controlling the TSV critical dimensions.

Table 3: Comparison of polymer-clad TSVs to other TSV technologies from the literature.

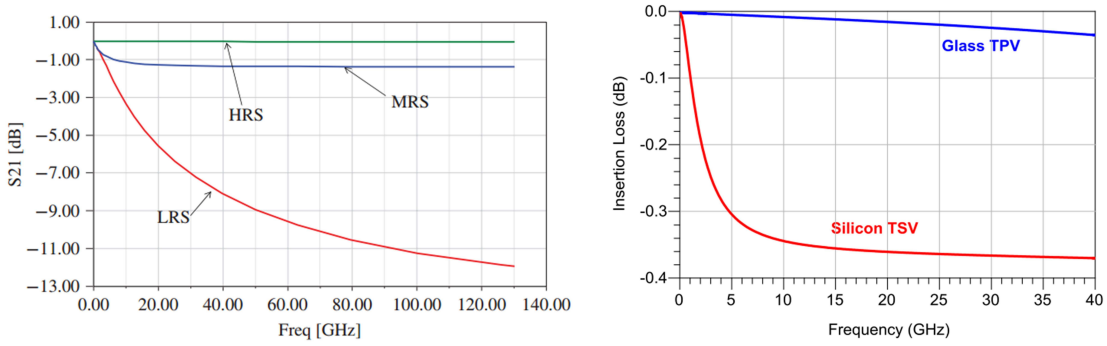
| No. | Parameters | Polymer-clad TSVs | Parylene liner TSVs [48] | $SiO_2$ liner TSVs [25]/ [30] | Air liner TSVs [46] | Laser ablated coax [84] | Photodefined coax [42] | Glass Vias [85] |
|---|---|---|---|---|---|---|---|---|
| 1 | Images |  |  |  |  |  |  |  |
| 2 | Copper via diameter | 80 $\mu$m | 50 $\mu$m | 10/50 $\mu$m | 20 $\mu$m | 70 $\mu$m | 100 $\mu$m | 15 $\mu$m at top |
| 3 | TSV height | 390 $\mu$m | 100 $\mu$m | 100/400 $\mu$m | 65 $\mu$m | 150 $\mu$m | 300 $\mu$m | 30 $\mu$m |
| 4 | TSV pitch | 250 $\mu$m | Not available | 150/180 $\mu$m | 50 $\mu$m | Surrounded by non-coax | 500 $\mu$m | 27 $\mu$m |
| 5 | Liner thickness | 20 $\mu$m | 2.3 $\mu$m | Not available | 2.5 $\mu$m | 20-120 $\mu$m | $\sim$100 $\mu$m | Not applicable |
| 6 | TSV stresses | Low | Moderate | High | Low | Low | Low | High in copper |
| 7 | TSV oxide capacitance | Low | Moderate | High | Very low | Not applicable | Not applicable | Not applicable |
| 8 | Loss at high frequency | Low | Moderate | High | Low | Very low | Very low | Very low |
| 9 | Ease of fabrication | High | High | Very high | Low | Moderate | Moderate | Moderate |
| 10 | Special features | Photodefinition and optical TSVs | Ease of electroplating | Simpler fabrication | Metallization over air liners | Coax and non-coax in parallel | Photodefinition | Panel-scale fabrication |

# CHAPTER III

# POLYMER-EMBEDDED VIAS: TECHNOLOGY DEVELOPMENT AND DC CHARACTERIZATION

This chapter describes the fabrication of low-loss polymer-embedded vias with the techniques used to reduce cracks in SU-8 and determine an optimum exposure dose. Moreover, the scalability of the technology is demonstrated. Additionally, to test their electrical functionality, DC measurements are demonstrated.

## *3.1 Technology Description*




(a) (b)

Figure 32: Losses of copper vias (a) in high-resistivity silicon with 75 $\mu$m diameter and 300 $\mu$m tall copper vias with a 0.6 $\mu$m thick silicon dioxide liner [86], and (b) in glass substrate with 15 $\mu$m diameter and 30 $\mu$m tall copper vias and in 10 S/m conductivity silicon with 15 $\mu$m diameter and 50 $\mu$m tall copper vias with a 0.5 $\mu$m thick silicon dioxide liner [85].

High-resistivity silicon interposers can help achieve a reduction in TSV losses, as shown in Figure 32(a). However, high-resistivity silicon is expensive [86, 87]. Moreover, glass has been demonstrated as being a promising interposer technology to support and interconnect multiple chips [85]. Since glass is a dielectric, through-glass vias (TGVs) exhibit lower electrical losses compared to the TSVs with silicon dioxide

liner, as shown in Figure 32(b). However, the fabrication of TGVs is challenging, involving serial ablations to form vias in the glass. Moreover, glass has poor thermal conductivity compared to silicon. In order to address these challenges, a silicon interposer technology with copper vias embedded within polymer wells in low-resistivity silicon is explored in this research.

The proposed technology is called polymer-embedded vias. This technology helps attain a low-loss electrical performance compared to the TSVs with silicon dioxide liner (similar to glass interposers) using the commonly implemented 10 Ω-cm resistivity silicon, making it an intermediate solution between glass and high-resistivity silicon interposers, as shown in Figure 33. Moreover, since polymer is present between copper vias, this technology provides a reduction in TSV-to-TSV capacitance.

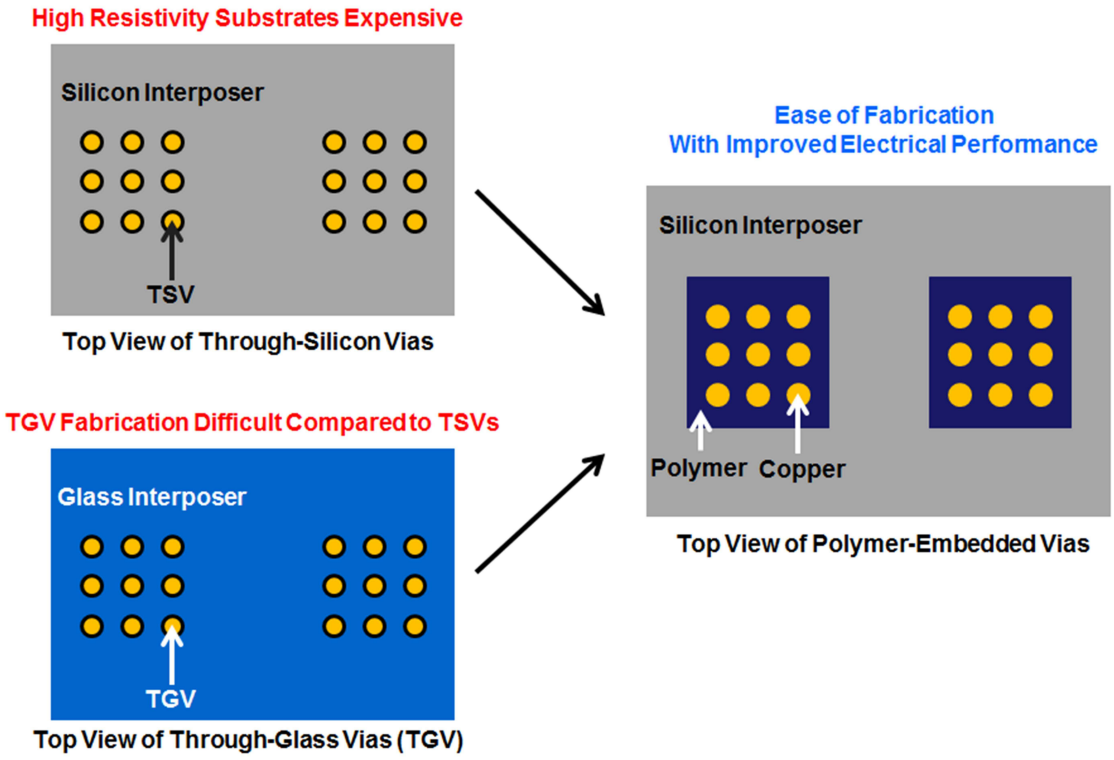



Figure 33: Comparison between through-silicon vias, through-glass vias and polymer-embedded vias.

Similar demonstrations in the literature to obtain copper vias within dielectric

regions in silicon include: (1) metal coated silicon pillars in polymer wells [88] and (2) glass reflow over etched areas in silicon followed by silicon pillar etching [89]. This research focuses on utilizing SU-8 photodefinition to fabricate low-loss TSVs, similar to the polymer-clad TSVs described in the previous chapter. To better understand polymer-embedded vias with respect to the literature, a comparison is shown in Table 4.

Table 4: Comparison of via fabrication processes in dielectric wells.

| | **Fabrication Method** | **Principle** | **Benefit** | **Limitation** |
|---|---|---|---|---|
| **1** | **Metal coated silicon pillars in polymer wells [88]** | Metal deposition over silicon pillars within wells in silicon followed by polymer filling | Wide selection of polymer is available | Back side silicon polishing needed and possibly poor low frequency performance |
| **2** | **Copper vias in glass wells [89]** | Glass reflow over etched areas in silicon followed by silicon pillar etching | CTE of glass close to silicon and seedless electroplating | Glass reflow required to be performed at 1000 °C for 5 hours |
| **3** | **Polymer-embedded vias (This research)** | Photodefinition of polymer-filled wells in silicon | Photodefinable and enhanced electrical performance at high as well as low frequencies | Limited selection of high aspect-ratio photodefinable materials |

## 3.2 Via-to-via Capacitance Analysis

To quantify the reduction in TSV-to-TSV capacitance that can be obtained by using polymer-embedded vias, via-to-via capacitance is plotted in Figure 34 utilizing TSV models in the literature for passive (floating) silicon interposers (without TSV depletion capacitance) [43, 55, 90, 91] and using Synopsys Raphael's RC2 (2D) interconnect solver.

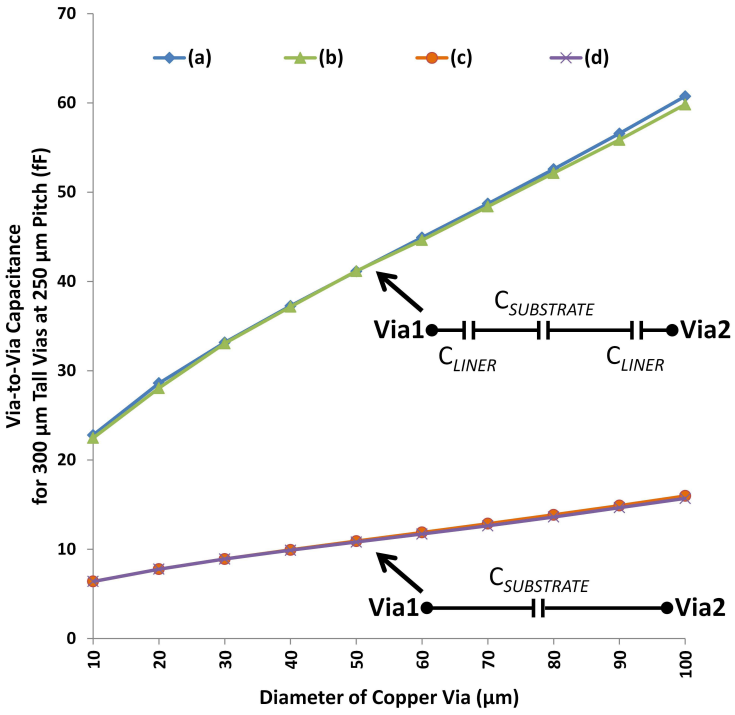



Figure 34: Via-to-via capacitance for passive silicon interposers: (a) Using the model for TSVs with a 1 m thick silicon dioxide liner; (b) Using Raphael simulations for TSVs with a 1 $\mu$m thick silicon dioxide liner; (c) Using the model for polymer-embedded vias; and (d) Using Raphael simulations for polymer-embedded vias.

$$C_{liner} = \frac{2\pi\epsilon_{liner}}{\ln\left(\frac{radius_{coppervia} + thickness_{liner}}{radius_{coppervia}}\right)}. \tag{5}$$

$$C_{substrate} = \frac{\pi\epsilon_{substrate}}{\cosh^{-1}\left(\frac{pitch}{2 * radius_{TSV}}\right)}. \tag{6}$$

Since the silicon is floating, for the TSVs with a silicon dioxide liner the capacitance between two copper vias can be represented by three capacitances in series: dielectric liner capacitance, substrate (silicon) capacitance and again dielectric liner capacitance [43]. However, for polymer-embedded vias, the capacitance between two copper vias is represented by only substrate (SU-8) capacitance since only dielectric is present between the copper vias. To obtain the plots in Figure 34, the equations for TSV dielectric capacitance and substrate capacitance (Equation 5 and Equation 6) are selected from the literature [55,90,91]. The relative dielectric constants of silicon, silicon dioxide and SU-8 are 11.68, 3.9 and 3, respectively [56–59]. In the literature, the dielectric constant of SU-8 has been reported between 3 and 4 [58, 59]. To calculate the best case capacitance reduction, a dielectric constant of 3 was selected for SU-8. Using the analytical models, via-to-via capacitance of copper vias 100 $\mu$m in diameter, 300 $\mu$m tall and at 250 $\mu$m pitch is 60.75 fF and 16 fF when the liner is 1 $\mu$m thick silicon dioxide and when the copper vias are embedded in a polymer well, respectively (Figure 34).

## *3.3 Fabrication of Polymer-embedded Vias*

The fabrication processes explored for polymer-embedded vias are described next. Bottom-up copper electroplating helps to fabricate high aspect-ratio void-free vias [92]. To perform bottom-up copper electroplating, two processes were investigated for the fabrication of polymer-embedded vias, as shown in Figure 35. The first process entails a copper support layer and the second a mesh seed layer [45].

Similar to the polymer-clad and optical TSVs, polymer-embedded vias are also fabricated using SU-8. As shown in Figure 35, the fabrication of polymer-embedded vias begins with the deposition of silicon dioxide, titanium (for adhesion between silicon dioxide and copper) and copper on one side of a silicon wafer.

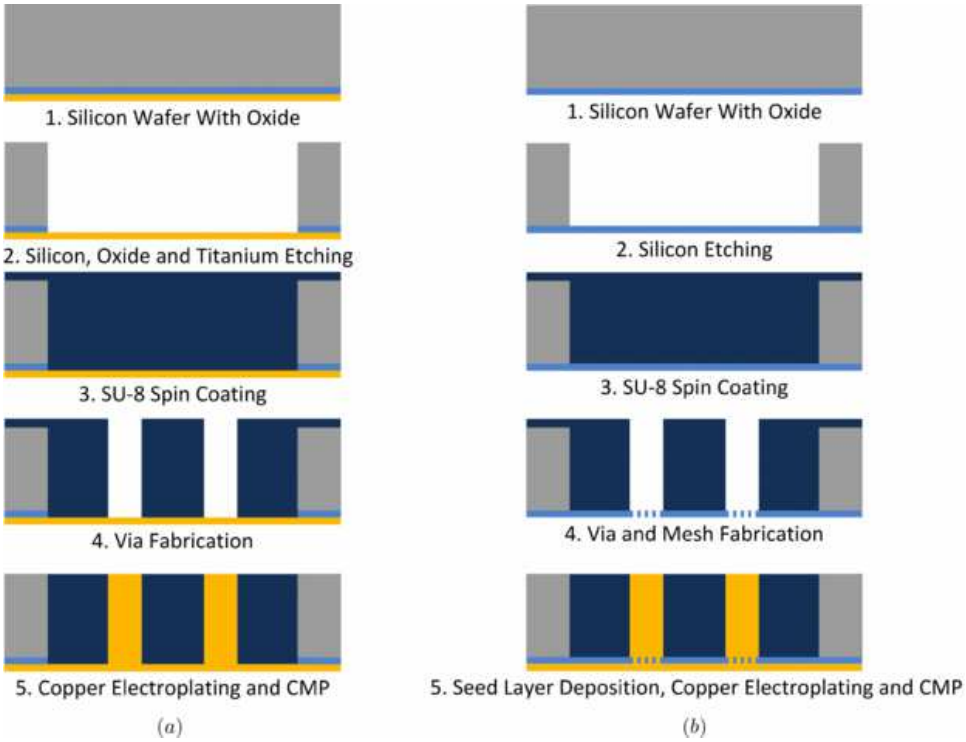



Figure 35: Fabrication processes for polymer-embedded vias: (a) Process with copper support layer and (b) Process with mesh seed layer.

With respect to the fabrication process using a copper support layer, silicon dioxide, titanium and copper are deposited on the back side of a silicon wafer where titanium acts as an adhesion layer between the silicon dioxide and the copper. Next, using anisotropic dry etching with a photoresist mask, wells are etched in silicon followed by etching of silicon dioxide and titanium using buffered oxide etch (BOE). Once the titanium is etched, SU-8 is spin coated in two steps. The first coating step is performed at a low rpm value since higher values would lead to non-uniform SU-8 filling of the wells. However, spin coating at low rpm yields a thick SU-8 layer with a non-planar surface across a wafer. The spin-coated SU-8 is soft baked with temperature ramping during heating and cooling, and the thick layer of uncrosslinked SU-8 over silicon is removed by polishing. The polishing setup to remove the uncrosslinked SU-8 is shown in Figure 36. Following this, the second coating step is performed where a thin layer of SU-8 is spin coated. Consequently, the planarity of the SU-8

surface is improved. Once the SU-8 is uniformly coated, soft bake is performed with temperature ramps followed by exposure. After exposure, the post exposure bake is performed with slow temperature ramps followed by the SU-8 development and an isopropanol clean to obtain vias in the polymer filled wells in silicon, as shown in Figure 37. The developed vias are then kept in 5 % sulfuric acid solution followed by bottom-up copper electroplating and CMP to remove the additional copper and SU-8. The copper layer at the bottom of vias can be removed using CMP or wet etching [45].

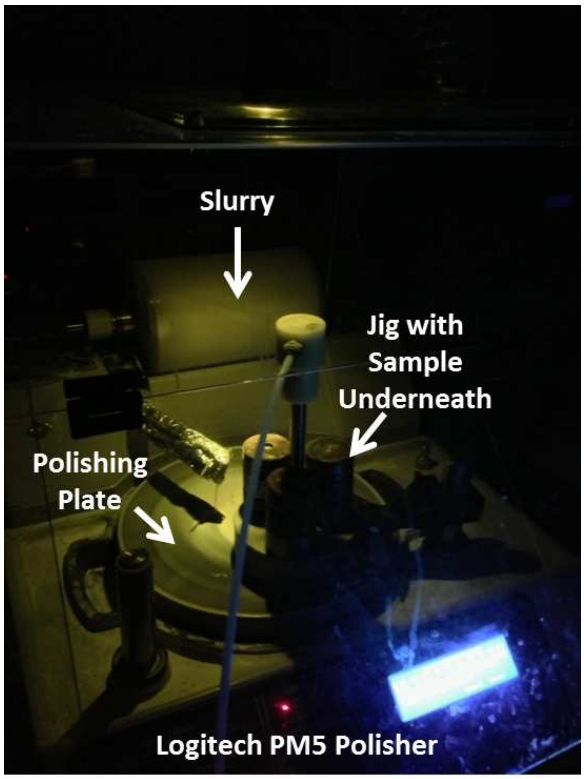



Figure 36: An image of the setup used to polish uncrosslinked SU-8 in an ultra-low light environment.

A fabrication process with a mesh seed layer (similar to the polymer-clad TSVs in the previous chapter) was also explored. With respect to this process (Figure 35), silicon dioxide is first deposited on the back side of a silicon wafer. Next, using anisotropic dry etching, wells are etched in silicon followed by SU-8 processing as

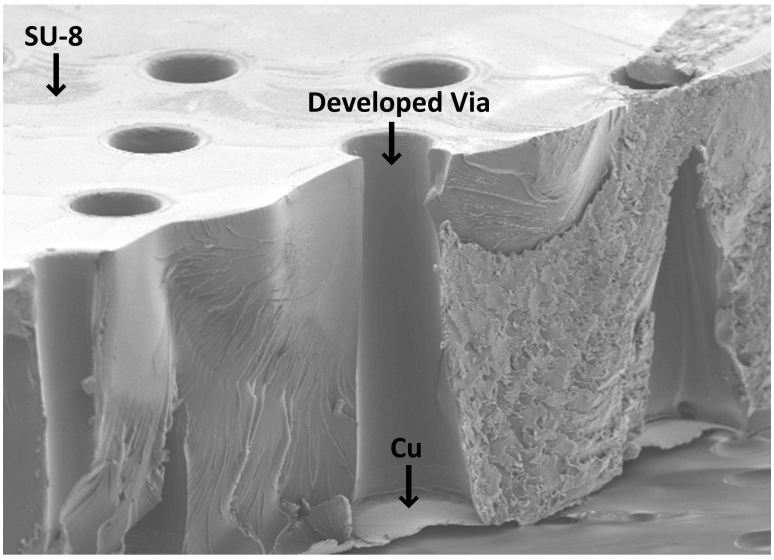



Figure 37: Cross section of a polymer-embedded via after SU-8 development.

described earlier to obtain vias in the SU-8 filled wells in silicon. A mesh is then fabricated in the suspended silicon dioxide membrane underneath the developed vias. Once this mesh is fabricated, a titanium-copper seed layer is deposited over the silicon dioxide mesh where the titanium acts as an adhesion layer between the silicon dioxide and the copper. After seed layer deposition, the mesh is pinched off using copper electroplating followed by bottom-up copper electroplating and CMP to remove the additional copper and SU-8. The titanium-copper seed layer can be removed using CMP or wet etching.

## *3.4 Crack Reduction and Optimum Exposure Dose Determination*

Based on the two different processes analyzed (with a copper support layer and with a mesh seed layer) for the fabrication of polymer-embedded vias, the process with a copper support layer was implemented to reduce masking steps. There were two major challenges to the fabrication of polymer-embedded vias: crack formation in SU-8 after SU-8 development and optimum exposure dose determination.

Cracks occur in thick SU-8 layers primarily after the post exposure bake and

development due to the impact of large process-induced internal stresses. As shown in Figure 38, several processing methods have been shown in the literature to reduce cracks in SU-8 including: (1) a reduction of SU-8 soft-bake temperature to 50 °C [93]; and (2) a slow ramp rate at the end of post exposure bake [94]. Moreover, the use of a higher exposure dose has been discussed in the open literature to reduce cracks in SU-8.

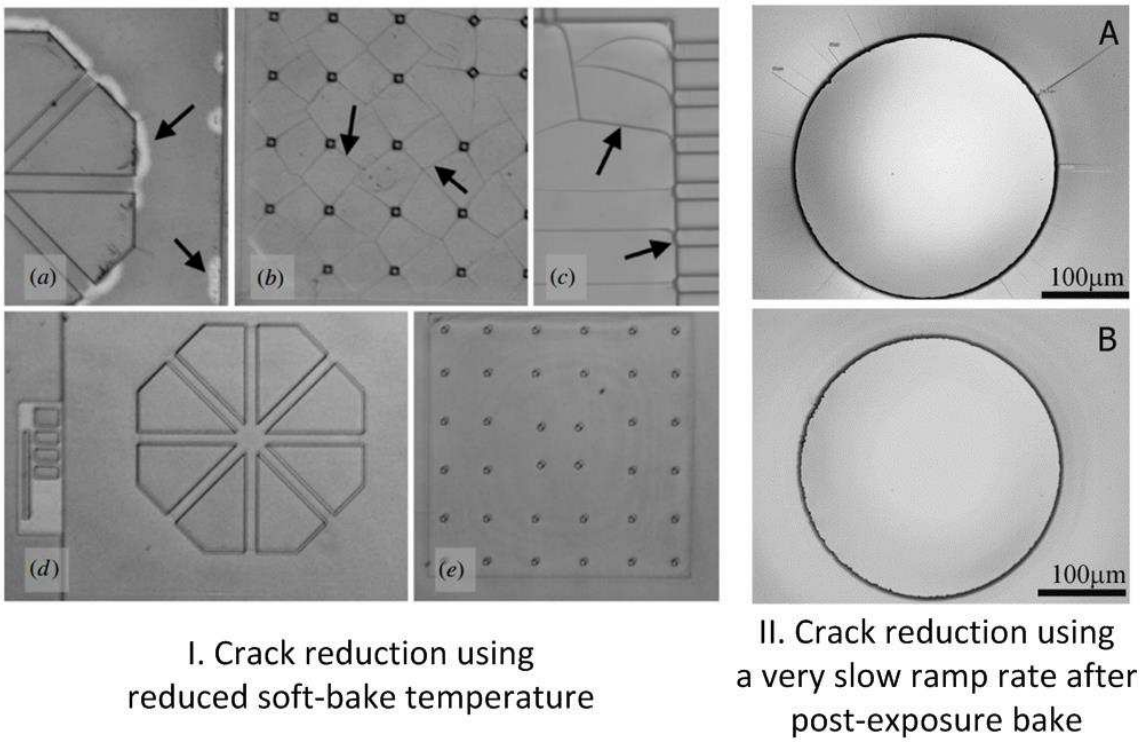


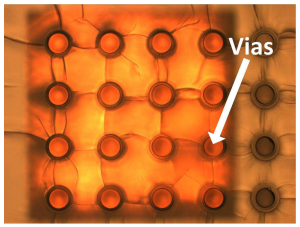
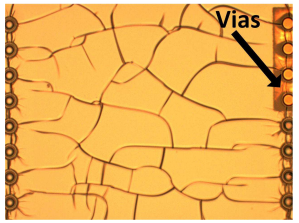
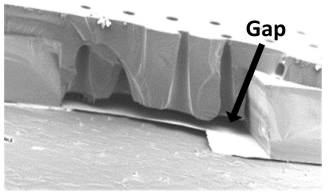
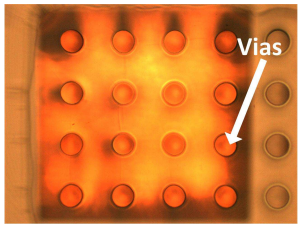
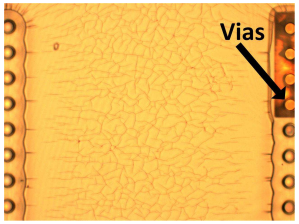
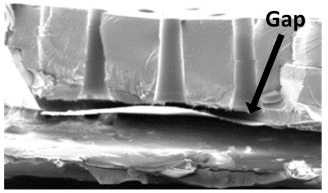
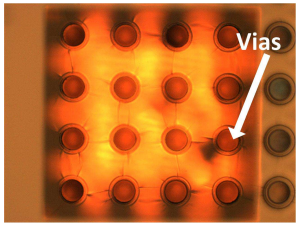
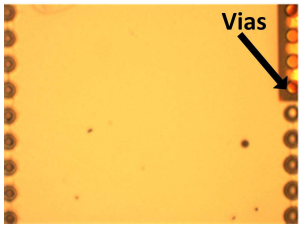
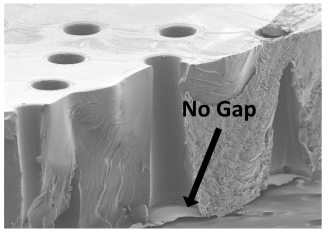

Figure 38: Crack reduction techniques demonstrated in the literature [93, 94]

The technique of reducing the SU-8 soft-bake temperature is not a feasible solution for polymer-embedded vias with a thick SU-8 since it would require a very long time. With respect to the second technique, cracks have been observed in the SU-8-filled wells with copper vias even after the implementation of slow temperature ramps. Lastly, with respect to increasing the exposure dose to reduce cracks in SU-8, an optimum dose determination is needed since (1) a higher dose (which reduces cracks) would make the formation of smaller via dimensions (<100 $\mu$m diameter) in SU-8 difficult, while (2) a lower dose would result in underexposed SU-8 with faster

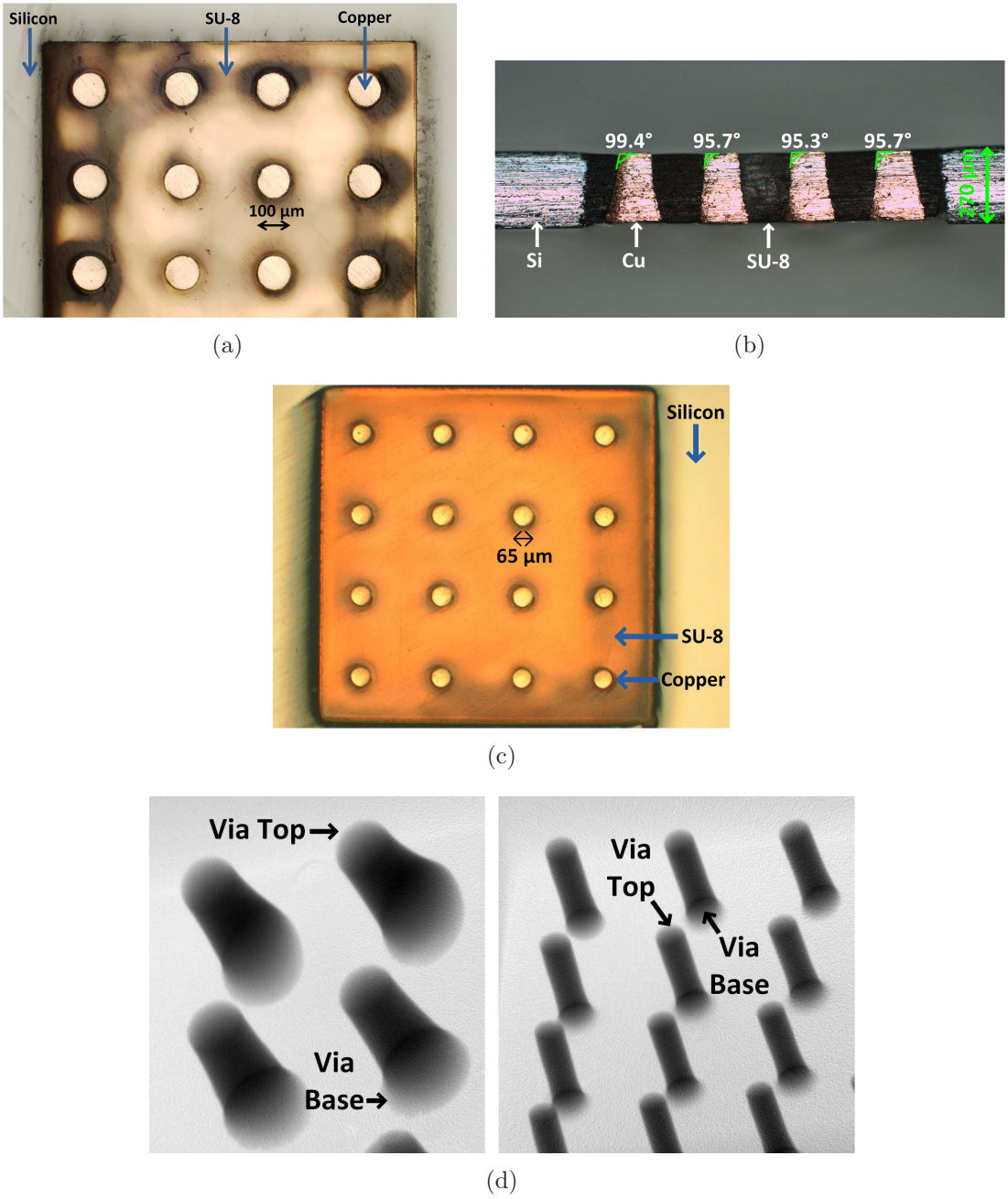
development at the base, as explained in the next section. Moreover, the SU-8 in the wells also experiences polishing when in the uncrosslinked phase which makes the SU-8 conditions significantly different compared to that in the literature. To address these challenges, a set of experiments were performed, as shown in Table 5.

In this research, the impact of the exposure dose and development method is explored to reduce crack formation in SU-8 as well as to determine the optimum dose for exposure. Different dosage values were selected for experimentation. With respect to the first experiment, corresponding to a fixed exposure dose, SU-8 filled wells were exposed for 208 seconds in a Karl Suss MA-6 Mask Aligner and development was performed using a spinner in a beaker. In this experiment, deep cracks were obtained in SU-8 as well as vias were underexposed leaving a gap between the SU-8 and the copper at the end of development. With respect to the second experiment, SU-8 filled wells were again exposed for 208 seconds using the same mask aligner described for the first experiment but development was performed with ultrasonic agitation. Here small but numerous cracks were obtained in SU-8 and again vias were underexposed leaving a gap between the SU-8 and the copper. With respect to the third experiment, SU-8 filled wells were exposed for 416 seconds (doubling the exposure dose compared to the first two experiments) and development was performed with ultrasonic agitation. With this experiment, only a few near-surface cracks were observed in SU-8 (these cracks are removed during CMP) and the vias were completely exposed.

Table 5: Set of experiments for crack reduction and optimum dose determination.

| No. | Exposure Time (Seconds) | Development Method | Top View of Vias | Top View of Area Between Vias | Cross-Section of Vias |
|---|---|---|---|---|---|
| 1 | 208 | Using spinner in developer |   |   |   |
| 2 | 208 | Using ultrasonic agitation |   |   |   |
| 3 | 416 | Using ultrasonic agitation |   |   |   |

## 3.5 Fabrication Results




(a) (b)

(c)

(d)

Figure 39: Fabricated 270 $\mu$m tall polymer-embedded vias on a 250 $\mu$m pitch: (a) Top view of 100 $\mu$m diameter TSVs; (b) Cross-section view of the 100 $\mu$m diameter TSVs; (c) Top view of 65 $\mu$m diameter TSVs; and (d) X-ray image showing void-free copper electroplating of the 100 $\mu$m diameter TSVs (left) and the 65 $\mu$m diameter TSVs (right).

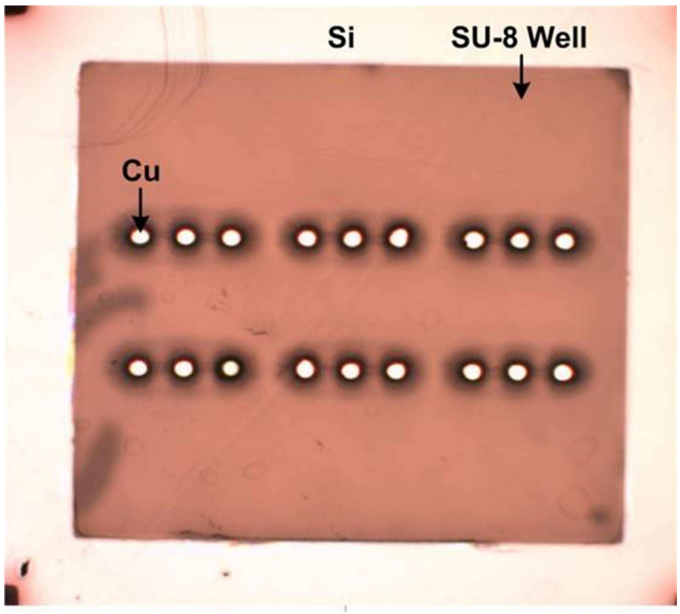
Figure 39(a) is a top view image of the fabricated 270 $\mu$m tall and 100 $\mu$m diameter polymer-embedded vias on a 250 $\mu$m pitch. Figure 39(b) is a cross-section image illustrating the polymer-embedded vias; the approximate taper for each via is also shown for completeness. Moreover, scaling of the polymer-embedded vias is demonstrated by fabricating 65 $\mu$m diameter and 270 $\mu$m tall polymer-embedded vias on a 250 $\mu$m pitch, as shown in Figure 39(c). As with polymer-clad TSVs, void-free copper electroplating was achieved for the fabricated polymer-embedded vias, as shown in the x-ray image (Figure 39(d)).

Further scaling of polymer-embedded vias is demonstrated by fabricating 65 $\mu$m diameter and 370 $\mu$m tall polymer-embedded vias on a 150 $\mu$m pitch, as shown in Figure 40.

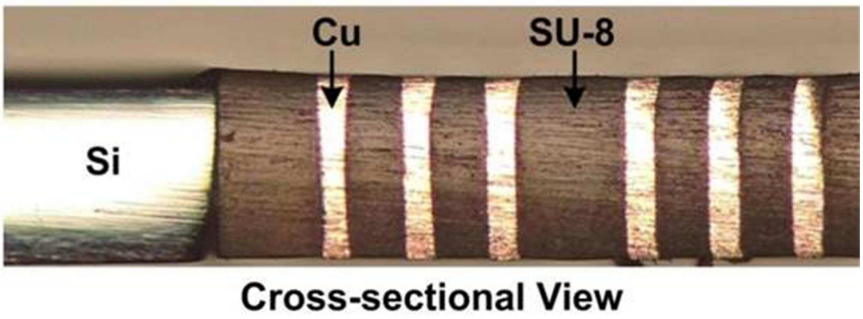
Polymer-embedded vias were thus fabricated with several dimensions to demonstrate technology scaling, as summarized in Table 6.

Table 6: Fabricated polymer-embedded via dimensions.

| Parameter | **TSV Set 1** | **TSV Set 2** | **TSV Set 3** |
|---|---|---|---|
| **Diameter** | 100 $\mu$m | 65 $\mu$m | 65 $\mu$m |
| **Height** | 270 $\mu$m | 270 $\mu$m | 370 $\mu$m (37 % increase) |
| **Pitch** | 250 $\mu$m | 250 $\mu$m | 150 $\mu$m (40 % reduction) |
| **Aspect ratio** | 2.70 | 4.15 | 5.69 |
| **Polymer well** | 1 mm x 1 mm | 1 mm x 1 mm | 1.8 mm x 1.8 mm (80 % increase in width) |
| **Sample size** | Quarter wafer | Quarter wafer | Full 4-inch diameter wafer |




(a)

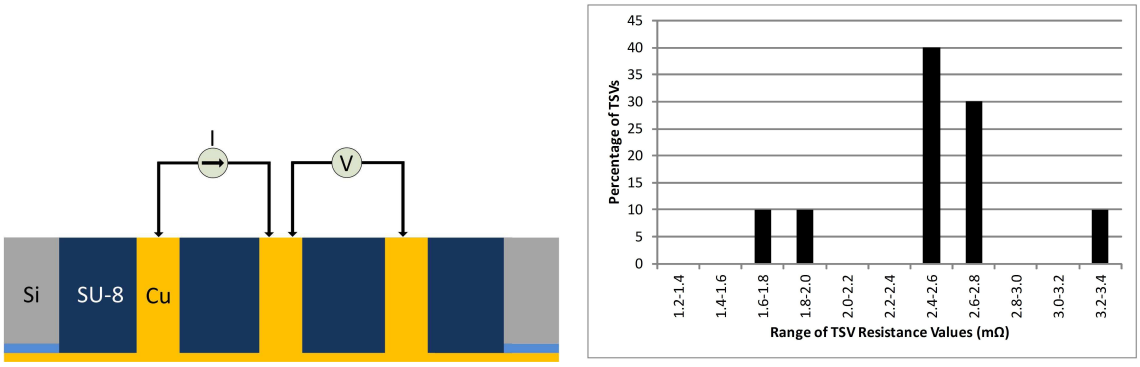



(b)

Figure 40: Fabricated 370 $\mu$m tall polymer-embedded vias on a 150 $\mu$m pitch: (a) Top view and (b) Cross-section view.

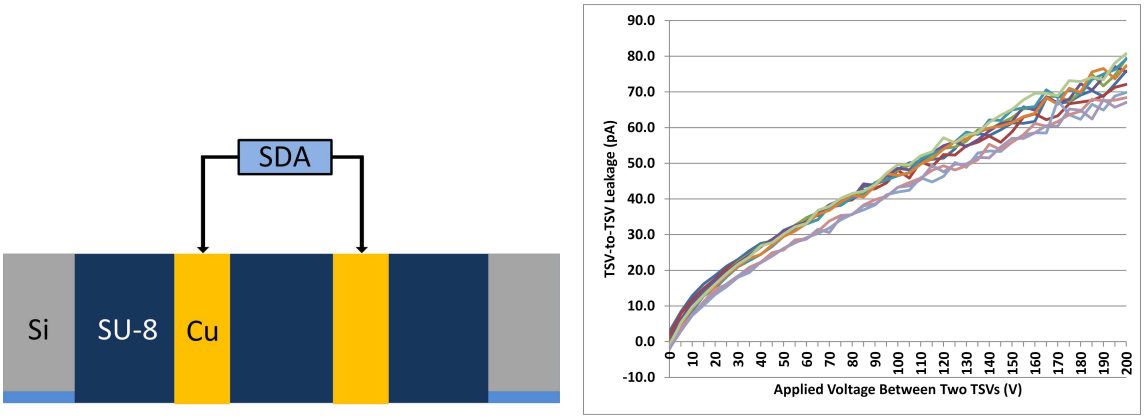
## *3.6 DC Measurements of Polymer-embedded Vias*

The resistance of the fabricated 100 $\mu$m diameter and 270 $\mu$m tall polymer-embedded vias was measured using the 4-point method, as shown in Figure 41(a). The average measured value of 20 different polymer-embedded vias is 2.54 m$\Omega$. Distribution of the measured via resistance values is given in Figure 41(b). Moreover,




(a) (b)

Figure 41: Resistance measurements of polymer-embedded vias with 100 $\mu$m diameter and 270 $\mu$m height: (a) Schematic of 4-point resistance measurement setup and (b) Distribution of 4-point resistance measurements for 20 polymer-embedded vias.




(a) (b)

Figure 42: Via-to-via leakage measurement of polymer-embedded vias with 100 $\mu$m diameter and 270 $\mu$m height: (a) Schematic of leakage measurement setup and (b) Leakage measurements of 10 pairs of polymer-embedded vias.

via-to-via leakage measurements were performed for 10 pairs of the fabricated 100 $\mu$m diameter and 270 $\mu$m tall polymer-embedded vias using a semiconductor device analyzer (SDA), as shown in Figure 42(a). The copper layer at the base of the vias was removed using wet etching, which was carefully monitored to prevent copper etching in the vias. The measured maximum via-to-via leakage current is 80.8 pA for an applied voltage of 200 V, as shown in Figure 42(b). The measured via-to-via leakage current is lower than the TSV leakage currents measured in the literature [95, 96].

## *3.7 Chapter Conclusion*

In conclusion, this chapter has demonstrated the fabrication of polymer-embedded vias in which copper vias are embedded within polymer-wells in a 10 Ω-cm resistivity silicon. Moreover, dimension scaling was shown to increase the TSV density and indicate the possibility of fabricating polymer-embedded vias with dimensions similar to the TSVs with silicon dioxide liner found in the literature [25]. For the fabricated polymer-embedded vias, resistance and leakage measurements were demonstrated showing their electrical functionality and high via-to-via isolation, respectively.

# CHAPTER IV

# POLYMER-EMBEDDED VIAS: RF AND TIME-DOMAIN CHARACTERIZATIONS

For the fabricated polymer-embedded vias demonstrated in the previous chapter, this chapter focuses on the RF and time-domain analysis and characterization.

## *4.1 Analysis*

### 4.1.1 TSV Frequency-domain Analysis

To compare the high-frequency parasitics of polymer-embedded vias and the TSVs with silicon dioxide liner, electrical analysis is performed for signal-ground TSV pairs. TSV high-frequency electrical modeling has been widely explored in the literature [86, 97–101]. As shown in Figure 43, the TSVs are modeled using resistors and inductors with conductance and capacitances between the signal and ground TSVs. For the TSVs with silicon dioxide liner, the path between the signal and ground TSVs consists of per-unit-length substrate capacitance $C_{u_{sub}}$, substrate conductance $G_{u_{sub}}$ and dielectric capacitances $C_{u_{liner}}$. For polymer-embedded vias, the path between the signal and ground TSVs consists of only per-unit-length substrate capacitance $C_{u_{sub}}$ and substrate conductance $G_{u_{sub}}$ since a dielectric liner is not present.

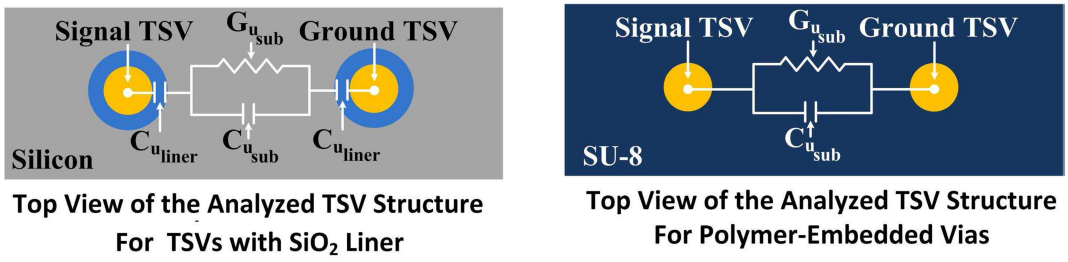



Figure 43: Top view of *RLCG* schematic for signal-ground TSV pairs.

*RLGC* **models:** The formulas for per-unit-length resistance, inductance, conductance and capacitance (*RLGC*) are implemented as demonstrated by X. Zheng et al. and I. Ndip et al. [86, 99], and are shown as follows:

**A. Resistance per unit length ($R_u$):** In the equation for resistance per unit length, $\rho$ is the resistivity of copper, $r$ is the copper via radius, $p$ is the TSV pitch, $f$ is the frequency, $\mu$ is the permeability and $\delta$ is the skin depth. The per-unit-length resistance is given by

$$R_u = \sqrt{R_{dc_{TSV}}^2 + R_{ac_{TSV}}^2}, \tag{7}$$

where $R_{dc_{TSV}} = \dfrac{\rho}{\pi r^2}$; $R_{ac_{TSV}} = (2\pi f\delta)\left(\dfrac{\mu}{\pi}\right)\left(\dfrac{p}{2r\sqrt{p^2-4r^2}}\right)$; and $\delta = \sqrt{\dfrac{\rho}{\pi\mu f}}$.

**B. Inductance per unit length ($L_u$):** The per-unit-length inductance is given by

$$L_u = \left[\frac{\mu}{\pi}\cosh^{-1}\left(\frac{p}{2r}\right)\right] + \left(\frac{R_u}{2\pi f}\right). \tag{8}$$

**C. Capacitance ($C_u$) and conductance ($G_u$) per unit length:** In the equations for capacitance and conductance per unit length, $\epsilon$ is the permittivity, $t_{liner}$ is the thickness of dielectric liner, and $\sigma_{sub}$ is the substrate conductivity. Since the silicon interposer is floating, the depletion capacitance is neglected [43].

First, the per-unit-length liner capacitance is evaluated as

$$C_{u_{liner}} = \frac{2\pi\epsilon_{liner}}{\ln\left(\dfrac{r+t_{liner}}{r}\right)}. \tag{9}$$

Next, to evaluate the per-unit-length substrate capacitance and conductance between the signal and ground TSVs, $C'_{u_{sub}}$ is evaluated first accounting for the combined contribution of the capacitance and conductance components as

$$C'_{u_{sub}} = \frac{\pi\epsilon_{sub}\left(1 - j\left(tan_{\delta_d} + tan\delta_c\right)\right)}{\ln\left(\dfrac{p}{2(r+t_{liner})} + \sqrt{\left(\dfrac{p}{2(r+t_{liner})}\right)^2 - 1}\right)}, \tag{10}$$

where $tan\delta_d$ represents the polarization losses of silicon and can be considered zero for the TSVs with silicon dioxide liner. Moreover, $tan\delta_c$ represents losses as a result of the conductivity of silicon and can be considered zero for polymer-embedded vias. Additionally, for polymer-embedded vias, the $r + t_{liner}$ component is given by only the radius ($r$) of the copper vias.

For the TSVs with silicon dioxide liner,

$$tan\delta_c = \frac{1}{\omega \epsilon_{sub} \rho_{Si}}. \tag{11}$$

Next, the combined capacitance and conductance component for the TSVs with silicon dioxide liner is given by

$$C_{u_T} = \frac{1}{\frac{1}{C_{u_{liner}}} + \frac{1}{C'_{u_{sub}}} + \frac{1}{C_{u_{liner}}}}, \tag{12}$$

and the combined capacitance and conductance component for polymer-embedded vias is given by

$$C_{u_T} = C'_{u_{sub}}. \tag{13}$$

From the calculated $C_{u_T}$, the TSV capacitance and conductance are extracted as follows:

$$C_u = Re\left(C_{u_T}\right); \text{ and} \tag{14}$$

$$G_u = -\omega Im\left(C_{u_T}\right). \tag{15}$$

**Validation using EM full-wave simulations:** Once the per-unit-length $RLGC$ are calculated, full-wave electromagnetic simulations are performed using ANSYS High-Frequency Structure Simulator (HFSS) to validate the analytically calculated circuit parameters. The simulation structures are shown in Figure 44.

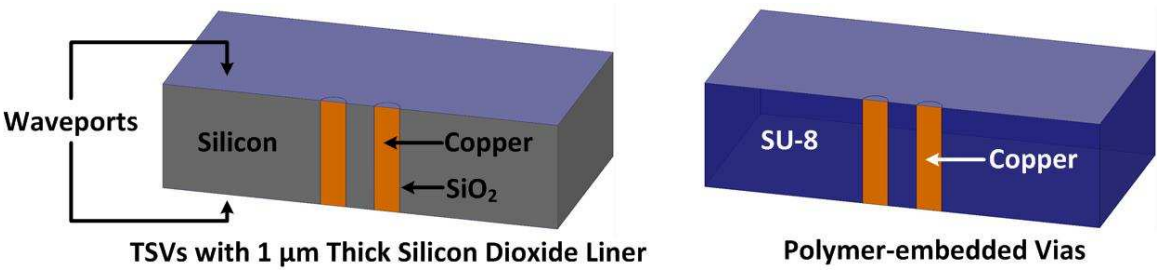



Figure 44: HFSS simulation structures.

From the port-only solutions (yielding 2D extractions), characteristic impedances ($Z_0$) and propagation constants ($\gamma$) of the TSV structures are extracted, as described by I. Ndip et al. [86], and the per-unit-length $RLGC$ are obtained as follows:

$$R_{u_{extracted}} = Re\left(\gamma Z_0\right); \tag{16}$$

$$L_{u_{extracted}} = \frac{Im\left(\gamma Z_0\right)}{\omega}; \tag{17}$$

$$G_{u_{extracted}} = Re\left(\frac{\gamma}{Z_0}\right); \text{ and} \tag{18}$$

$$C_{u_{extracted}} = \frac{Im\left(\frac{\gamma}{Z_0}\right)}{\omega}. \tag{19}$$

Using the circuit models and extraction, the evaluated per-unit-length $RLGC$ values for the TSVs with silicon dioxide liner and polymer-embedded vias are shown in Figure 45; copper vias are 300 $\mu$m tall and 70 $\mu$m in diameter on a 150 $\mu$m pitch. The thickness of the silicon dioxide liner is 1 $\mu$m. The relative dielectric constants of silicon, silicon dioxide and SU-8 are 11.68, 3.9 and 3, respectively; silicon resistivity is 10 Ω-cm and SU-8 loss tangent is 0.04 [56–59].

As shown in Figure 45, the per-unit-length resistance and inductance for the TSVs with silicon dioxide liner and polymer-embedded vias match well. Polymer-embedded vias attain 96.2% and 72.8% reduction in TSV conductance and capacitance at 50

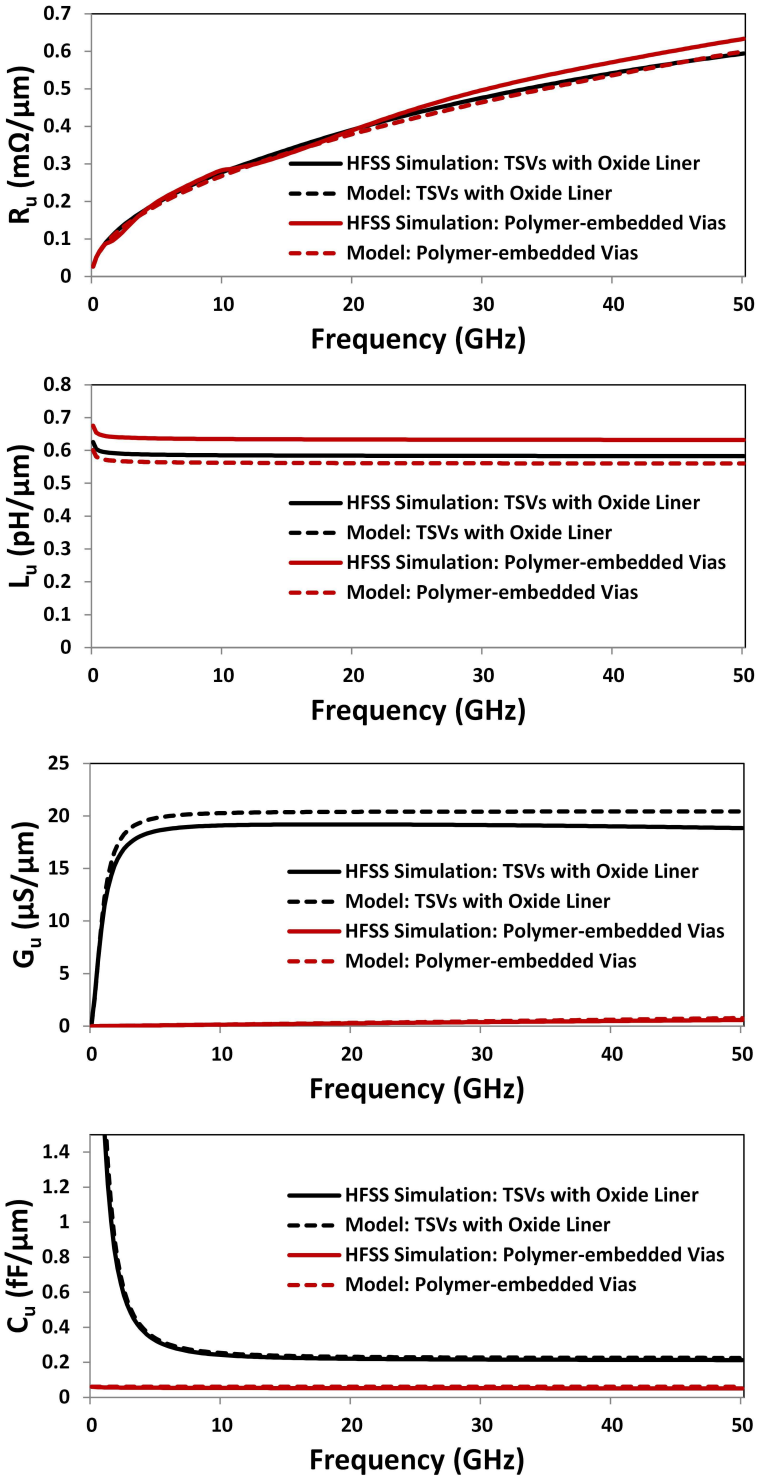



Figure 45: Evaluated per-unit-length TSV *RLGC* values using circuit models and HFSS simulations.

GHz, respectively, compared to the TSVs with silicon dioxide liner. The reduction in the capacitance and conductance of polymer-embedded vias helps attain a low-loss electrical performance and hence will be focused upon later in the chapter in the section on TSV de-embedding.

### 4.1.2 TSV Time-domain Analysis

In addition to the frequency-domain analysis, time-domain analysis is performed using eye diagrams to compare the time-domain behavior of polymer-embedded vias and the TSVs with silicon dioxide liner. Eye diagrams help assess intersymbol interference, jitter and skew, and thereby understand the performance of transmission links. Eye-diagram construction has been explored in the literature using $S$-parameters [36, 102–104] and is implemented in this research. The $S$-parameters of polymer-embedded vias and the TSVs with silicon dioxide liner (signal-ground TSV) obtained from HFSS simulations are imported in Keysight's Advanced Design System (ADS) using an S2P component for a transient analysis, as shown in Figure 46. The setup in Figure 46 corresponds to a time-domain measurement scenario where a pattern generator with 50 Ω impedance delivers electrical signals to one end of a TSV link and the other end of the TSV link is connected to an oscilloscope with 50 Ω impedance. A time-domain pseudo-random bit sequence voltage source (VtPRBS) with an internal 50 Ω impedance in series is used as input to the S2P component. Accounting for the internal 50 Ω impedance in series (corresponding to a pattern generator output) and the 50 Ω termination impedance (corresponding to an oscilloscope input), the VtPRBS generates a 1 Vpeak-to-peak pseudo-random bit sequence (PRBS) of $2^{11} - 1$ with a rise-and-fall time of 30 ps [105].

Using the setup shown in Figure 46, a transient analysis is performed yielding eye diagrams for the TSVs with silicon dioxide liner and polymer-embedded vias with 300 $\mu$m tall and 70 $\mu$m diameter copper vias on a 150 $\mu$m pitch; the liner thickness

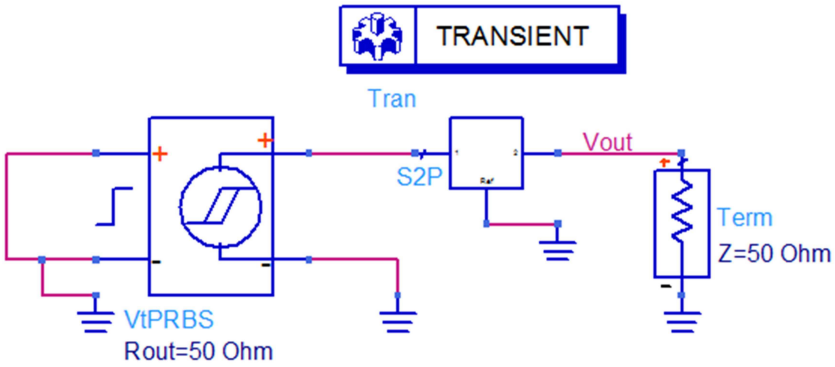



Figure 46: ADS schematic setup for eye diagrams of TSVs.

is 1 $\mu$m. As shown in Figure 47, polymer-embedded vias help improve eye opening and timing jitter at 5 Gbps and 10 Gbps.

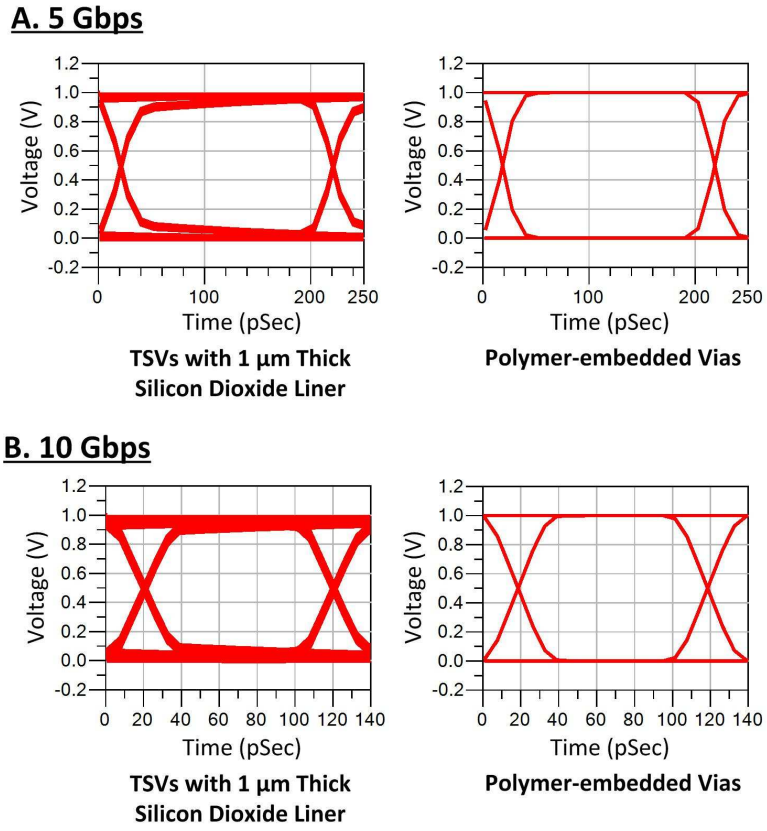



Figure 47: Eye diagrams of TSVs with silicon dioxide liner and polymer-embedded vias.

## 4.2 TSV RF De-embedding and Parasitics Extraction

### 4.2.1 TSV RF Characterization in the Literature and RF Measurement Setup in this Research

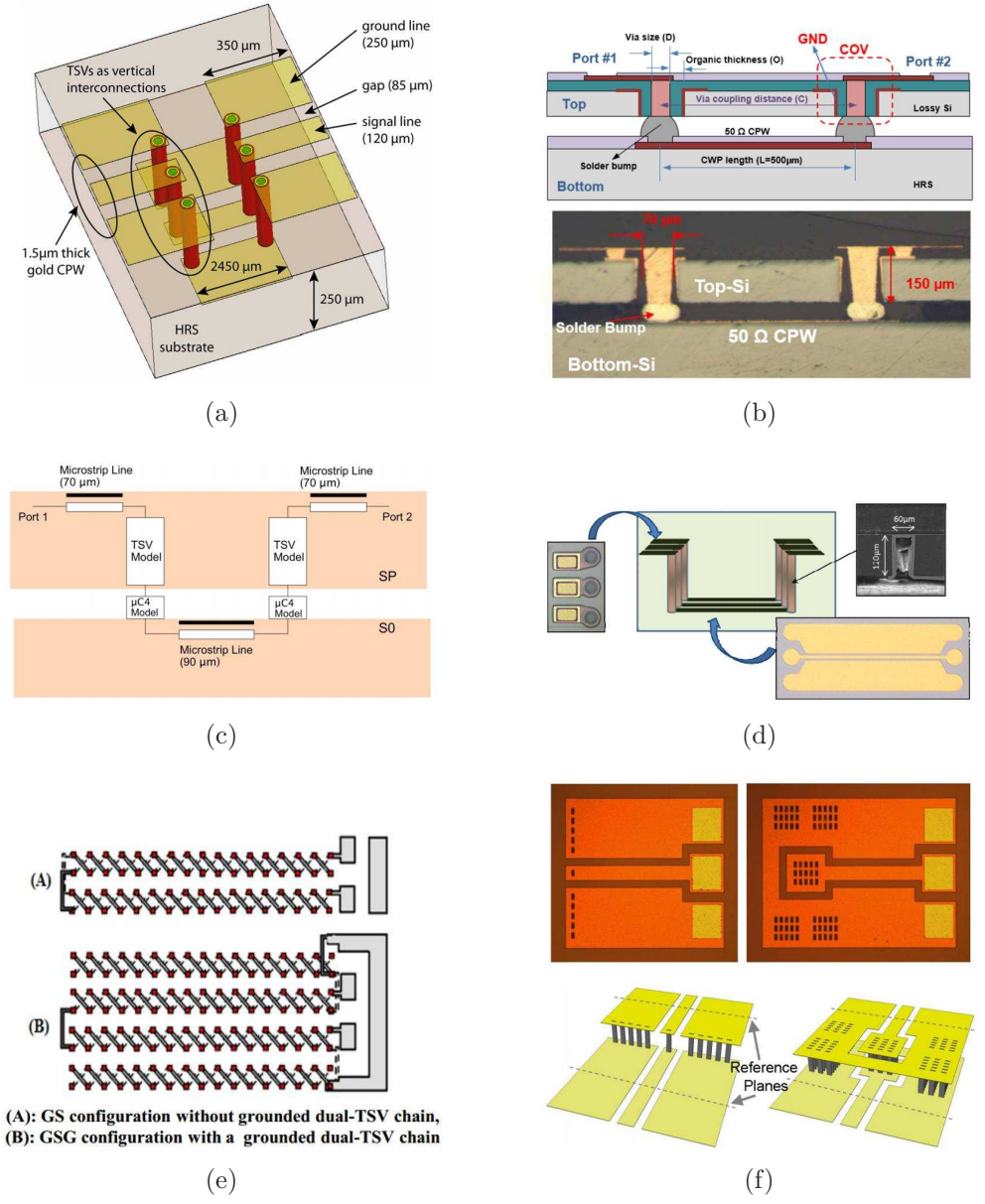



Figure 48: TSV RF measurement structures in the literature for: (a) TSVs with gold coated nickel wires assembled magnetically [106]; (b) coaxial structures with laser ablated polymer-filled vias [84]; (c) TSV loss characterization in CMOS SOI technology [104]; (d) characterization of TSVs in high-resistivity silicon for RF interposer applications [107]; (e) characterization of tungsten-filled dual-TSV chains [102]; and (f) implementation of TRL de-embedding using TSV bundles [108].

For RF measurements of TSVs, various structures have been explored in the literature including links with two or more TSVs. Two-port TSV measurement structures have mainly been demonstrated in the literature including chains with TSVs and traces [84, 102, 104, 106–108], as shown in Figure 48.

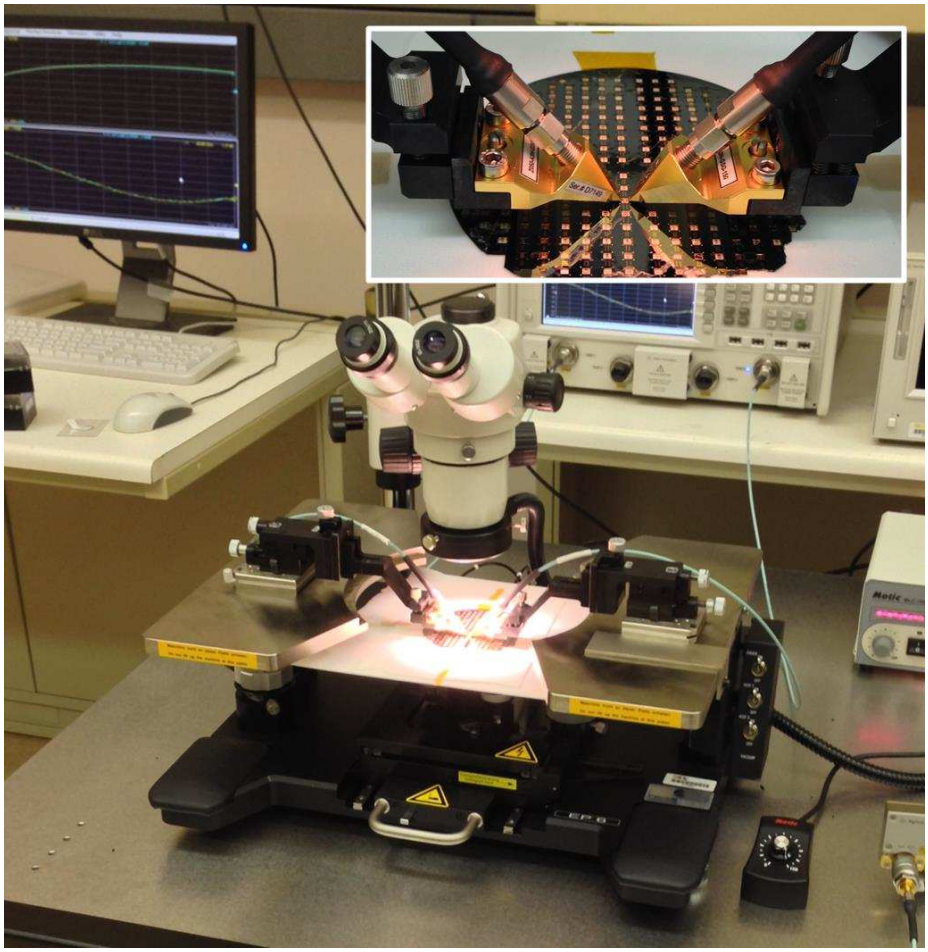


Figure 49: TSV RF measurement setup.

TSV RF measurements have been demonstrated in this research using two-port measurement structures. These measurements were performed up to 30-50 GHz for the fabricated TSVs and were compared to HFSS simulations. A dedicated RF probe station with a Keysight N5245A PNA-X network analyzer and Cascade MicroTech 150 $\mu$m pitch |Z| probes was used for the TSV measurements, as shown in Figure 49. Prior to the measurements of the TSVs, calibration was performed using the LRRM

protocol.

### 4.2.2 Fabrication and RF Measurements of TSVs with Silicon Dioxide Liner

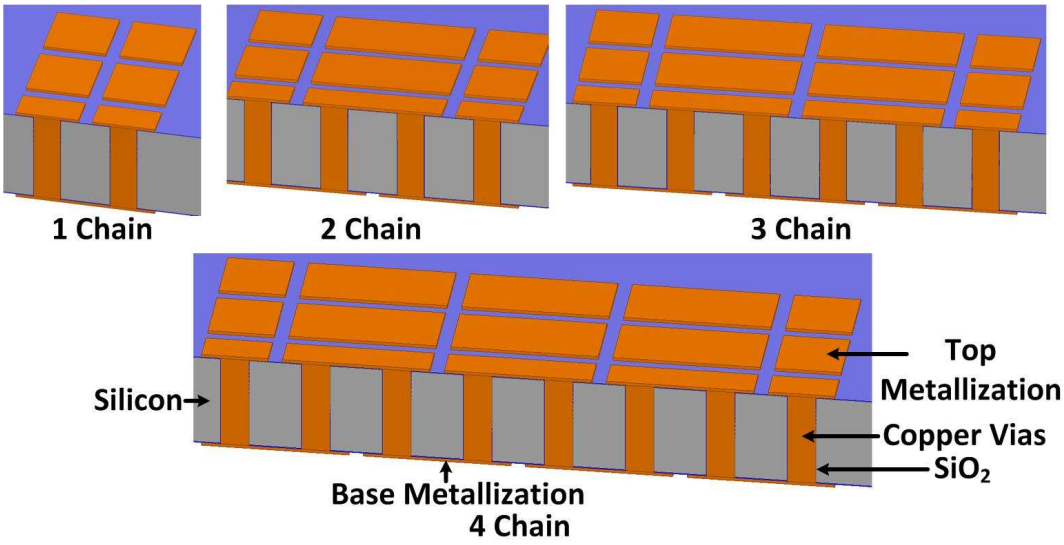



Figure 50: Structures simulated in HFSS for chains of TSVs with silicon dioxide liner.

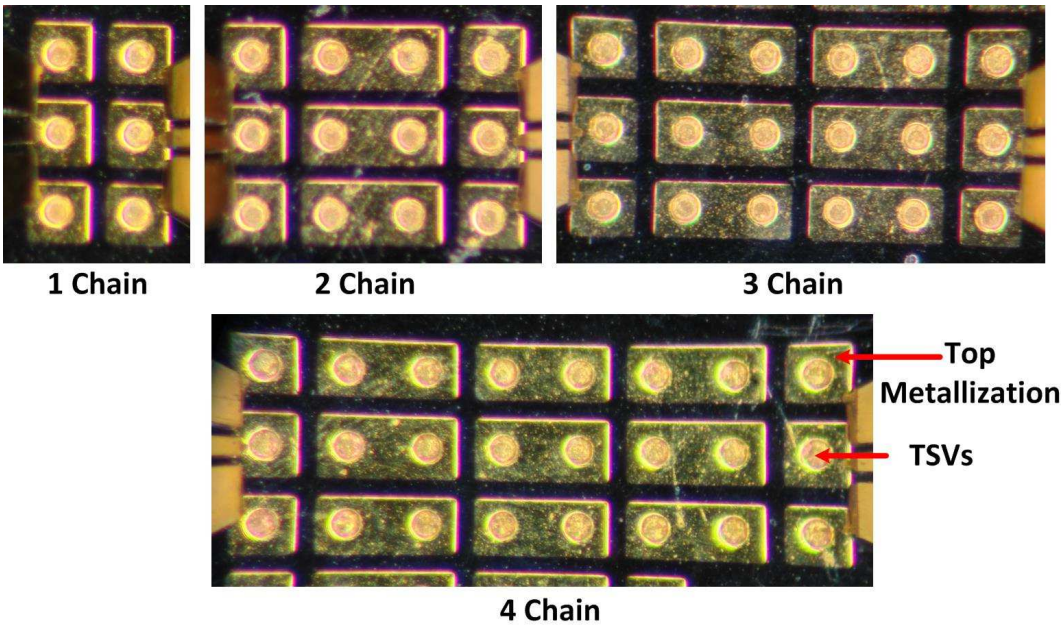



Figure 51: Fabricated chains of TSVs with silicon dioxide liner.

To validate the RF measurement setup and HFSS simulation structures for TSV measurements up to 50 GHz, TSVs with silicon dioxide liner were fabricated using

a process with mesh layer at the base (Figure 11). After the TSV fabrication, the top and base metallizations were fabricated using a metal lift-off process yielding RF measurement structures with different numbers of TSV-trace-TSV chain structures. Figure 50 shows the simulated TSV structures and Figure 51 the fabricated TSV structures with one to four TSV-trace-TSV chains. The TSVs consist of 88 $\mu$m diameter and 300 $\mu$m tall copper vias on a 250 $\mu$m pitch with 1 $\mu$m thick silicon dioxide liner, and 200 $\mu$m wide metal pads/traces. Figure 52 demonstrates that the TSV measurements match well with the HFSS simulations.

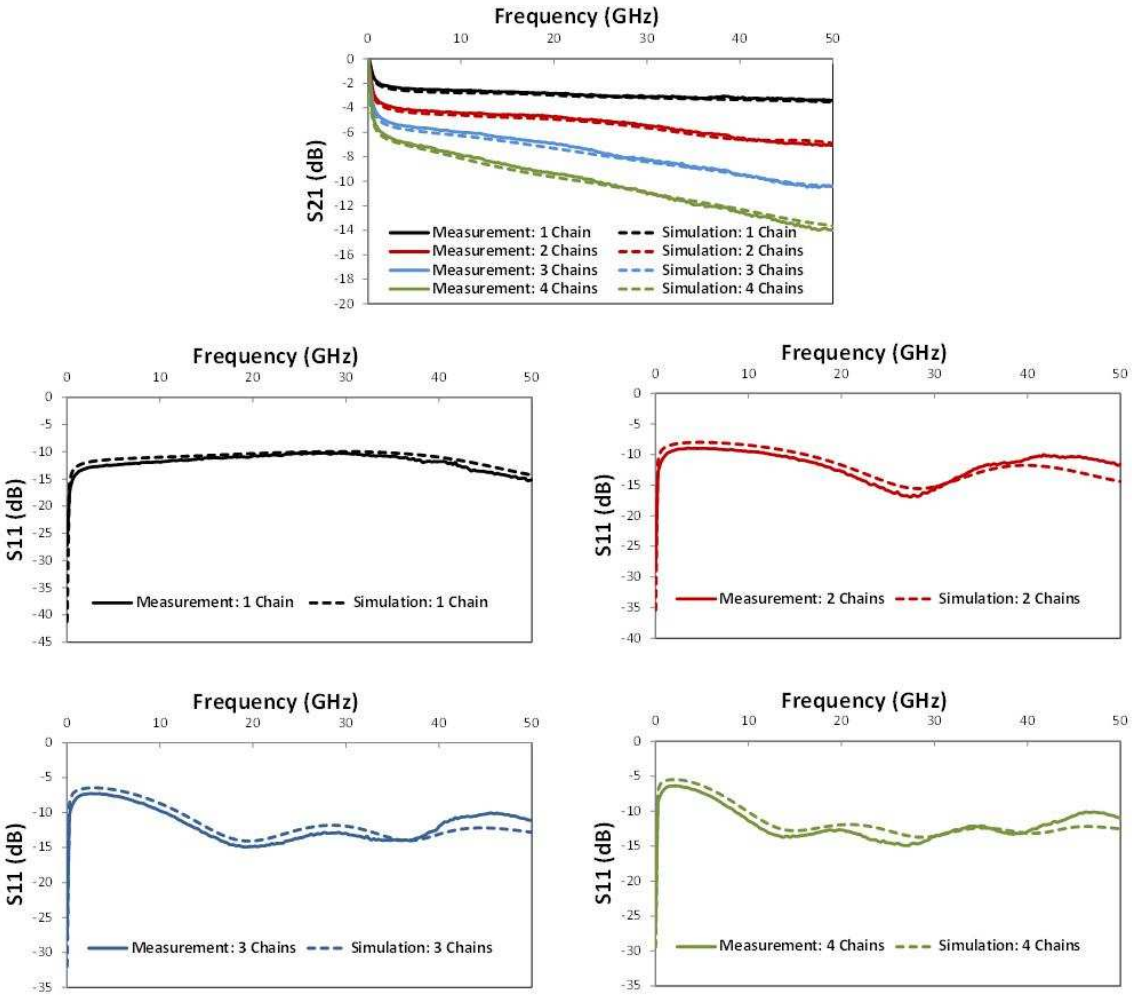



Figure 52: RF measurements and simulations of TSVs with silicon dioxide liner.

### 4.2.3 De-embedding and $CG$ Extraction of Polymer-embedded Vias

Extracting the losses of a TSV is important in order to understand the TSV parasitics and their impact on an electrical link performance. To extract the losses of TSVs, various techniques have been explored in the literature including Thru-Reflect-Line (TRL), single-port, L-2L and open short, as explained in Table 7.

Table 7: Comparison of TSV de-embedding techniques in the literature.

| | **Techniques** | **Principle** | **Benefit** | **Limitation** |
|---|---|---|---|---|
| **1** | **TRL [108]** | Second and third tier TRL implementation | Accurate de-embedding demonstrated up to 60 GHz | Difficulty in obtaining reference impedances for 3D transitions |
| **2** | **Single-port [109]** | Open and short structures for $RLGC$ extraction | Simpler fabrication for $RLGC$ extraction | Difficult to obtain accurate opens and shorts at higher frequencies |
| **3** | **L-2L [110]** | TSV-trace-TSV links with different trace lengths | Simpler TSV loss extraction structures | Demonstrated in the literature up to 50 GHz; application at higher frequencies unknown |
| **4** | **Open-short [111]** | Open-short structures with $ABCD$ matrices extract TSV loss | Simpler TSV loss extraction structures | Difficult to obtain accurate opens and shorts at higher frequencies |

To extract the losses of polymer-embedded vias, two de-embedding methodologies are explored in this research, L-2L and open-short, due to their ease of implementation and validity up to higher frequencies [110,111]. Figure 53 shows the schematics of the fabricated and simulated structures for TSV de-embedding. Figure 54 shows the fabricated polymer-embedded vias with traces (using the fabrication process shown in Figure 35 followed by the fabrication of the top and base metallizations). The fabricated polymer-embedded vias consist of 60 $\mu$m diameter and 285 $\mu$m tall copper vias with traces on a 150 $\mu$m pitch within 1800 $\mu$m x 1800 $\mu$m wells. Standalone polymer-embedded via structures are simulated for the sole purpose of benchmarking their results to those obtained from de-embedding. Similarly, standalone TSV structures with silicon dioxide liner are also simulated (with 1 $\mu$m thick silicon dioxide liner and similar sized via dimensions in 10 $\Omega$-cm resistivity silicon) for comparison with the de-embedded losses, and the extracted capacitance and conductance of polymer-embedded vias.

***For L-2L de-embedding*** [110], TSV-trace-TSV structures with 400 $\mu$m and 800 $\mu$m long traces between the TSVs (with pads) were fabricated, simulated and measured. The measured and simulated $S$-parameters of polymer-embedded vias are converted to $ABCD$-parameters in MATLAB and the TSV losses are extracted as follows:

First,

$$ChainL = TSV * Trace * TSV; \text{ and} \tag{20}$$

$$Chain2L = TSV * Trace * Trace * TSV; \tag{21}$$

where $ChainL$, $Chain2L$, $TSV$ and $Trace$ represent matrices of $ABCD$-parameters. Moreover, $ChainL$ represents the TSV-trace-TSV structure with 400 $\mu$m long traces between the TSVs, $Chain2L$ the TSV-trace-TSV structure with 800 $\mu$m long traces between the TSVs, $TSV$ the GSG TSVs and $Trace$ the 400 $\mu$m long GSG traces

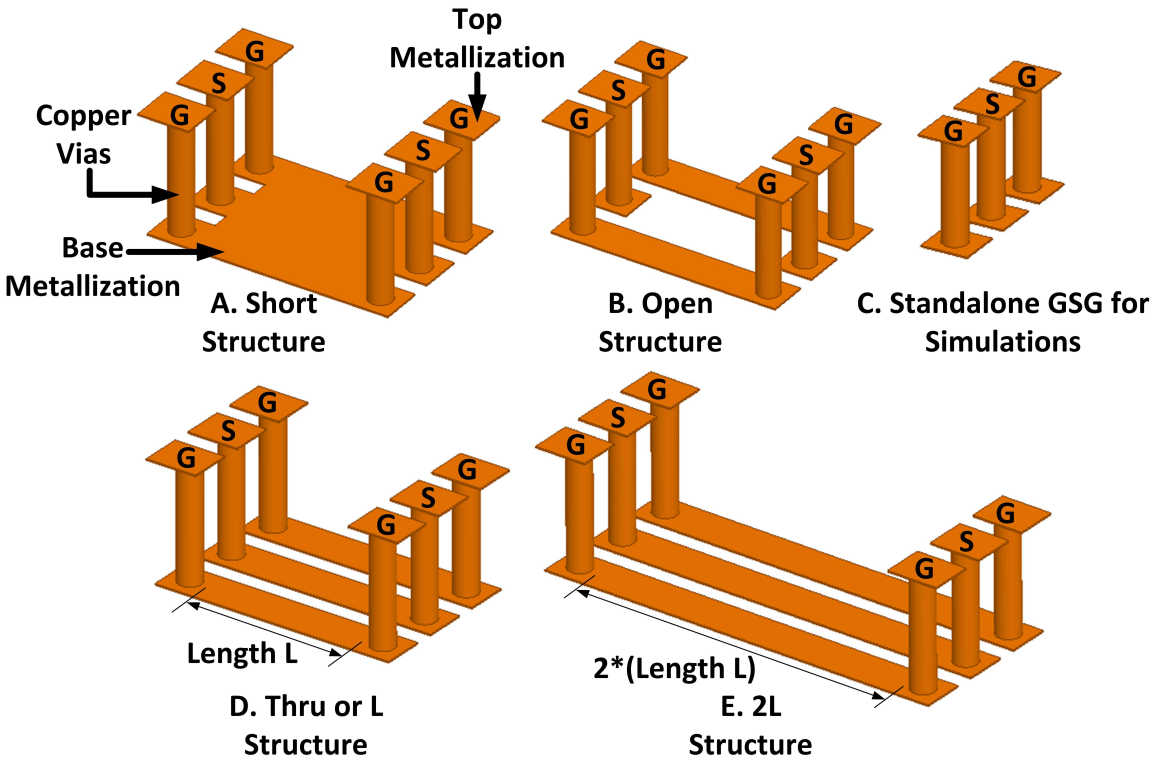



Figure 53: Schematic of measured and simulated TSV structures for de-embedding.

between the TSVs.

From Equation 20 and Equation 21,

$$TSV_{L-2L} = \sqrt{ChainL^{-1} * Chain2L * ChainL^{-1}}^{-1}. \tag{22}$$

***For open-short de-embedding*** [111], the TSV-trace-TSV structure with 400 $\mu$m long traces (thru or L structure), and open and short structures with the same distance between the TSVs were fabricated, simulated and measured.

The open-short technique provides the loss of the traces at the base of the thru structure, which is followed by the extraction of the loss of GSG TSVs using $ABCD$ matrices. First, the $S$-parameters of the open, short and thru structures are converted to $Y$-parameters to evaluate the following matrices:

$$Matrix1_Y = Thru_Y - Open_Y; \text{ and} \tag{23}$$

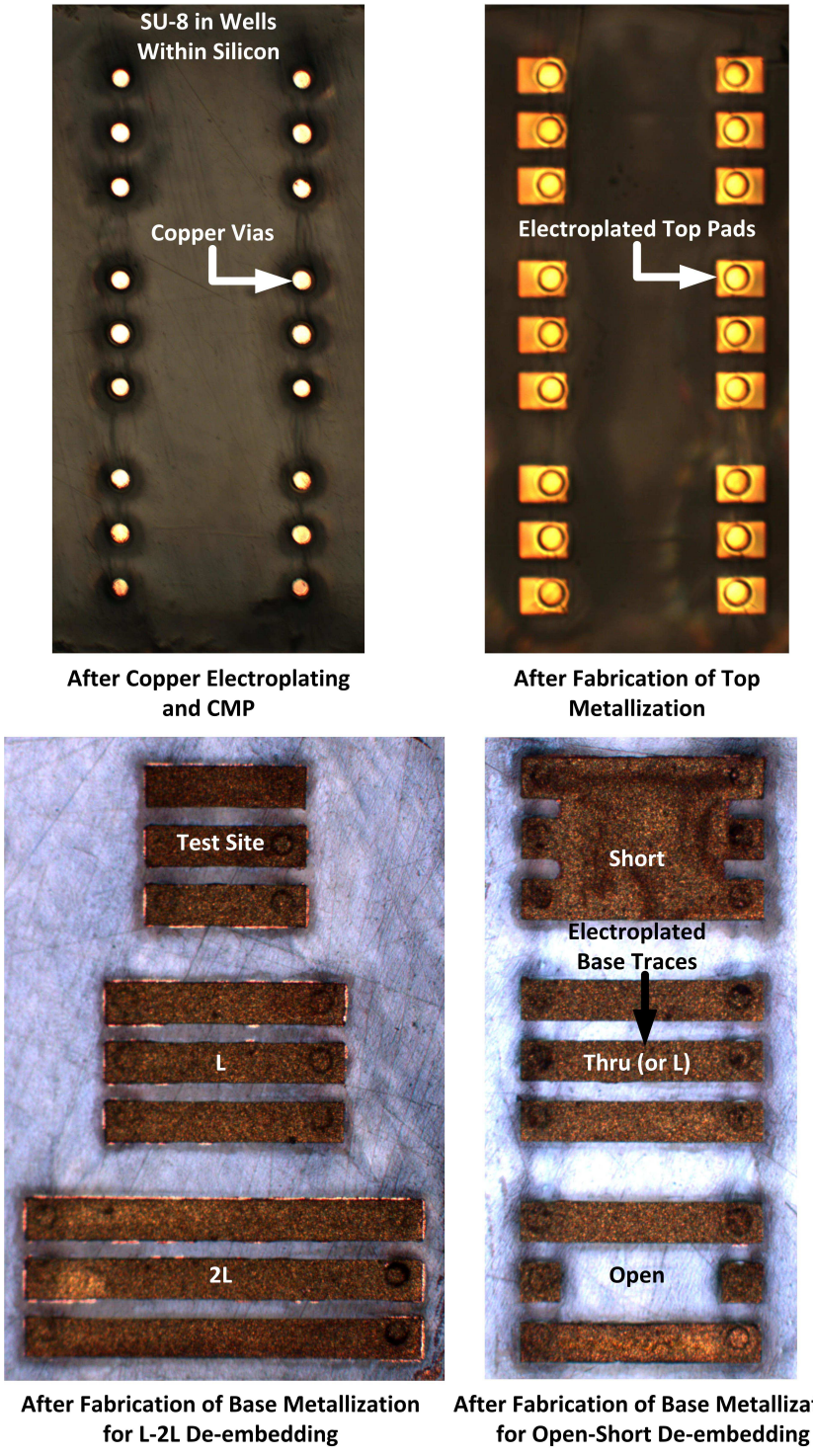



Figure 54: Fabricated polymer-embedded via de-embedding measurement structures.

$$Matrix2_Y = Short_Y - Open_Y. \tag{24}$$

Next, the evaluated $Y$-parameter matrices are converted to $Z$-parameter matrices and the $Z$-parameters of the traces at the base of the thru structure are obtained as follows:

$$Trace_Z = Matrix1_Z - Matrix2_Z. \tag{25}$$

Once the $Z$-parameters of the trace are obtained, they are converted to $ABCD$-parameters to extract the TSV loss from the thru structure as follows:

$$Thru = TSV * Trace * TSV; \tag{26}$$

$$Thru * Trace = TSV * Trace * TSV * Trace; \text{ and therefore} \tag{27}$$

$$TSV_{Open-Short} = \sqrt{Thru * Trace} * Trace^{-1}. \tag{28}$$

As shown in Figure 55, the via losses attained from both de-embedding techniques are in good agreement up to 30 GHz with minor differences between the de-embedded and the standalone loss due to fabrication variations. The de-embedding results from the measurements yield 0.22 dB insertion loss per polymer-embedded via at 30 GHz. Compared to the simulated insertion loss of a standalone TSV with silicon dioxide liner, an 87% reduction in insertion loss can be obtained using the polymer-embedded vias at 30 GHz.

Moreover, since the key contribution to the low-loss behavior of polymer-embedded vias results from the reduced capacitance and conductance compared to the TSVs with silicon dioxide liner (Figure 45), capacitance and conductance of the de-embedded GSG polymer-embedded vias are extracted using $Y$-parameters (obtained from the measured and simulated $S$-parameters) from the following equations [99, 101]:

$$C = \frac{Im\left(Y_{11} + Y_{22} + Y_{12} + Y_{21}\right)}{\omega}; \text{ and} \tag{29}$$

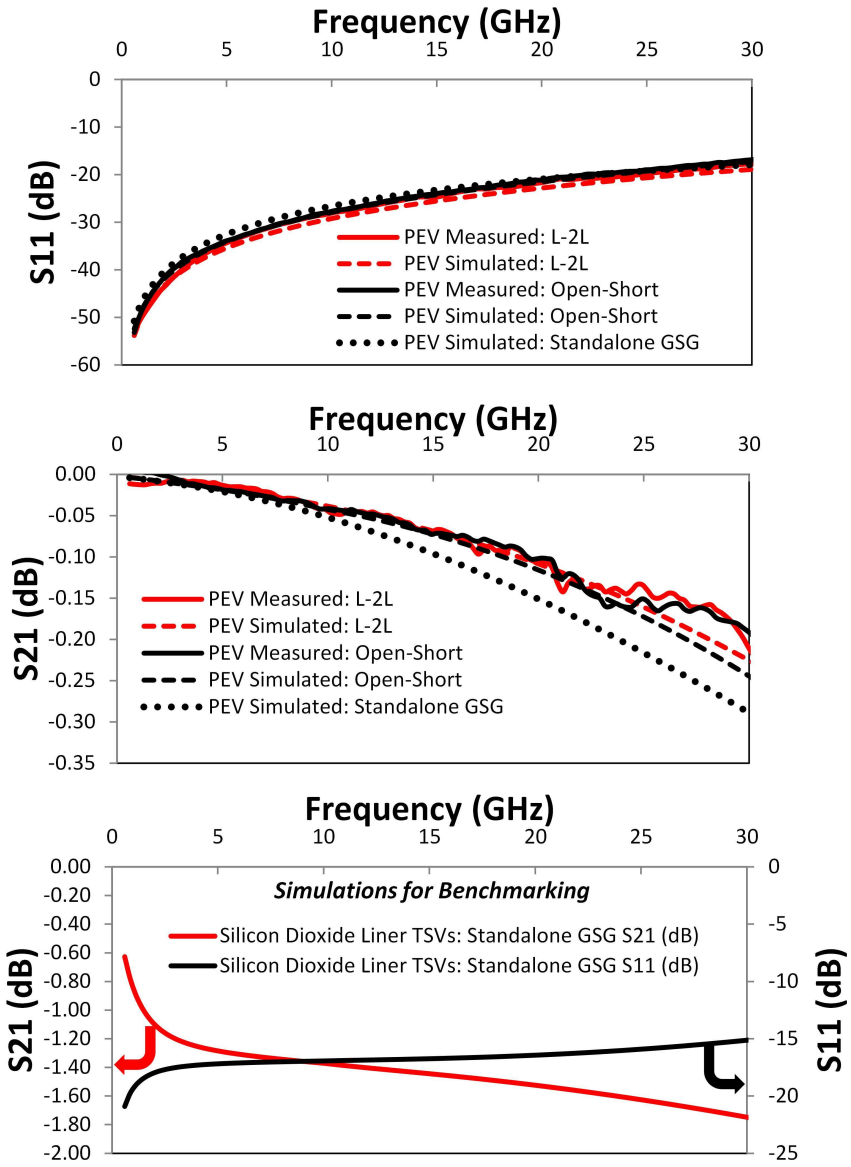



Figure 55: De-embedded polymer-embedded via (PEV) loss using measurements and simulations; TSVs with silicon dioxide liner included for benchmarking.

$$G = Re\left(Y_{11} + Y_{22} + Y_{12} + Y_{21}\right). \tag{30}$$

The $C$ and $G$ extractions demonstrate a significant reduction in the extracted capacitance and conductance for polymer-embedded vias, as shown in Figure 56.

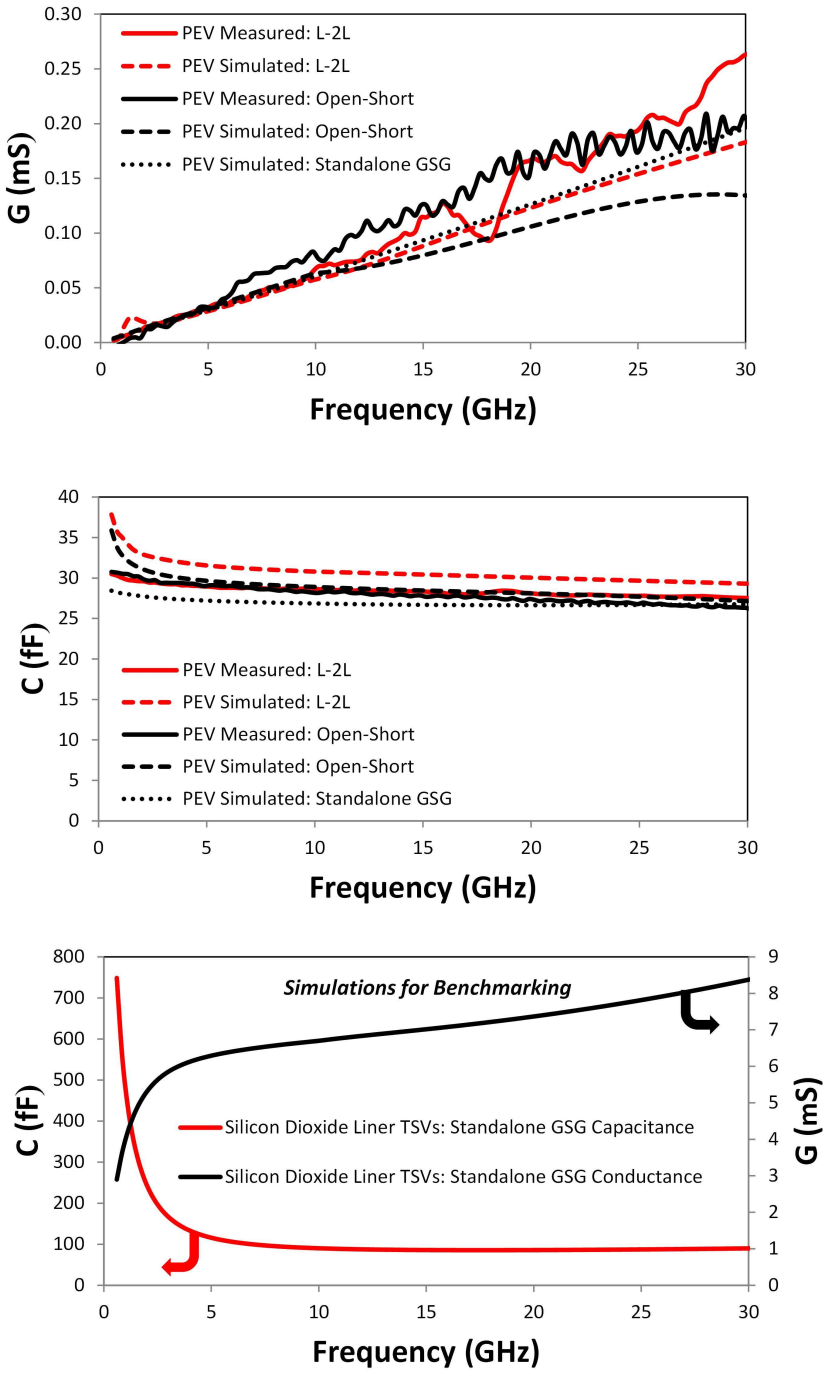
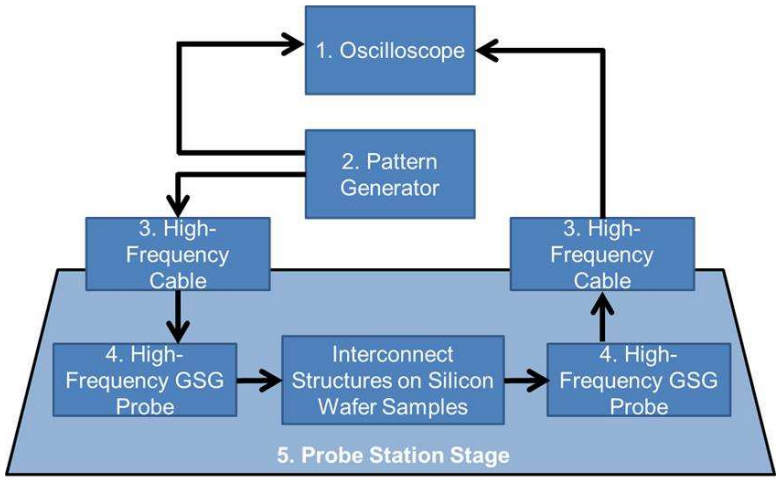


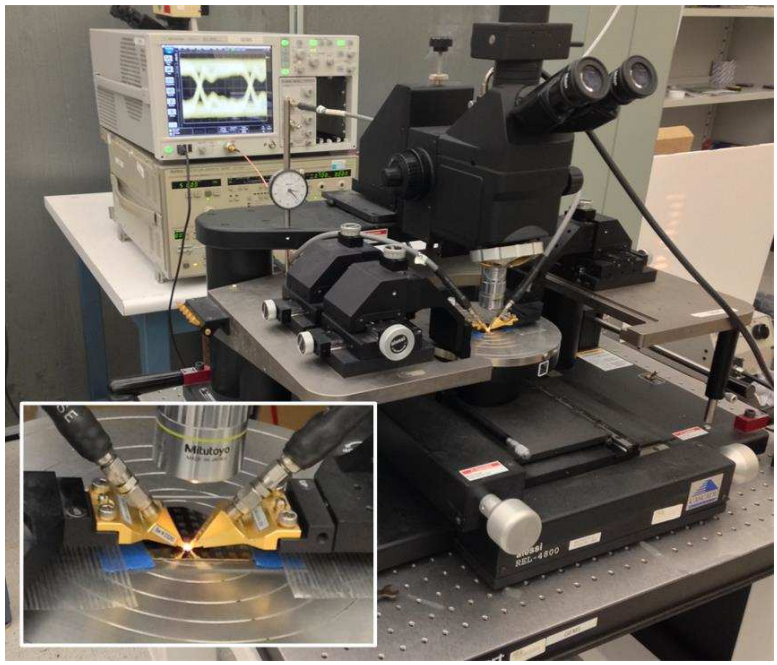

Figure 56: Extracted conductance and capacitance of the de-embedded polymer-embedded vias (PEVs) using measurements and simulations; TSVs with silicon dioxide liner included for benchmarking.

## *4.3 TSV Time-domain Characterization*

### 4.3.1 TSV Time-domain Measurement Setup and Loopback Measurements




(a)




(b)

Figure 57: TSV time-domain measurement setup: (a) Schematic and (b) The measurement setup.

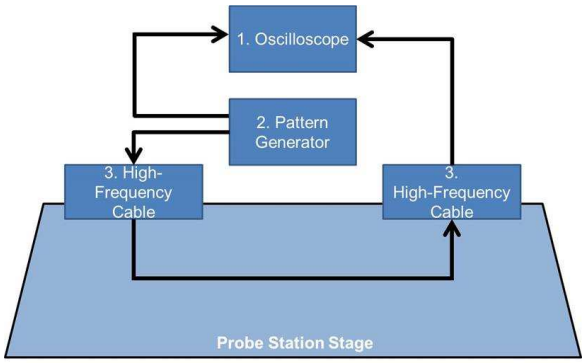
As with the TSV RF measurements, two-port measurement structures have been explored in the literature for time-domain measurements of TSVs using a pattern

generator and an oscilloscope [112]. For TSV time-domain measurements, a setup including an Anritsu MP1761C pulse pattern generator and an Agilent DCA-X 86100D oscilloscope was used with Cascade MicroTech 150 $\mu$m and 200 $\mu$m pitch |Z| probes, as shown in Figure 57. The measurements were performed with a 0.7 V (limited by the oscilloscope measurement capability) PRBS of $2^{11} - 1$.

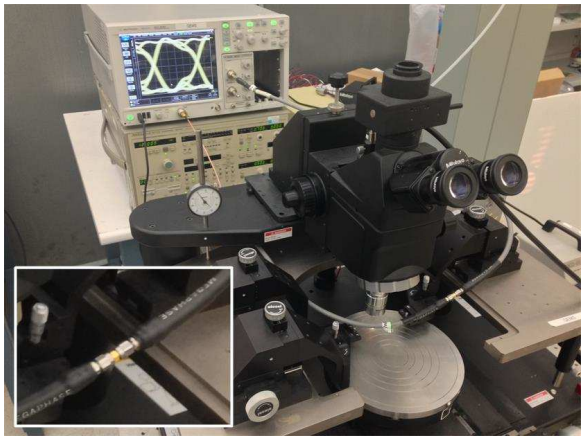
Once the setup is assembled (Figure 57), a loop-back measurement is performed with the output of the pulse pattern generator given directly to the oscilloscope in order to understand the time-domain performance of the setup without TSVs and two probes, as shown in Figure 58. The time-domain measurements at 5 Gbps and 10 Gbps show the presence of ringing due to the fast rise-and-fall time of the pulse pattern generator.

### 4.3.2 Time-domain Measurements of the TSVs with Silicon Dioxide Liner

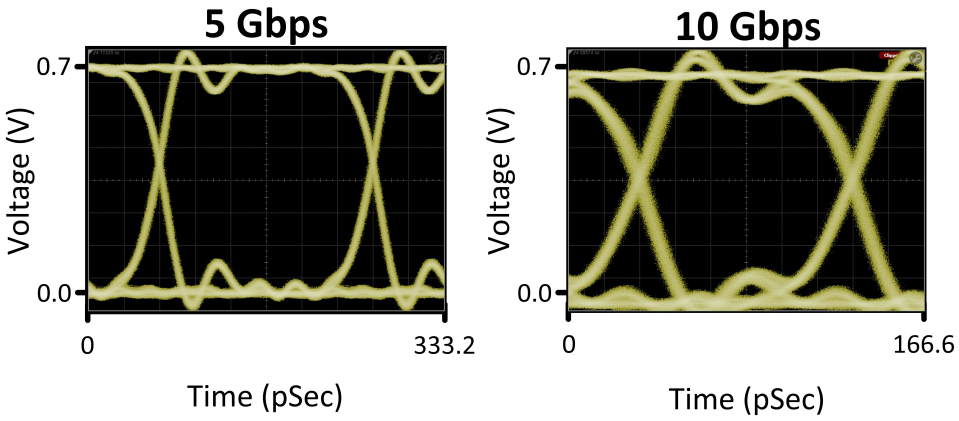
Once the loopback measurements are performed, time-domain measurements are first performed for the fabricated chains of TSVs with silicon dioxide liner (Figure 51). This results in eye diagrams for TSV chains, as shown in Figures 59 and 60. The TSV chains emulate the performance of a packaging architecture with stacked silicon interposers [113], demonstrating performance degradation with the increase in the number of TSVs in a link. To validate the time-domain measurements, $S$-parameter measurements of the TSV chains (Figure 52) were imported in ADS using the setup shown in Figure 46 for extracting eye diagrams with 0.7 Vpeak-to-peak swing (similar to the time-domain analysis section with 1 Vpeak-to-peak swing). The extracted eye diagrams in ADS have trends and eye openings similar to the time-domain measurements. The measurements show additional loss from cables and probes compared to the extraction yielding smaller eye openings.




(a)



(b)




(c)

Figure 58: Time-domain loopback characterization (a) schematic, (b) measurement setup, and (c) measurements.

### 4.3.3 Polymer-embedded Via Time-domain Measurements

To characterize the time-domain behavior of the fabricated polymer-embedded vias (the L or Thru structure in Figure 54), similar eye-diagram measurements are

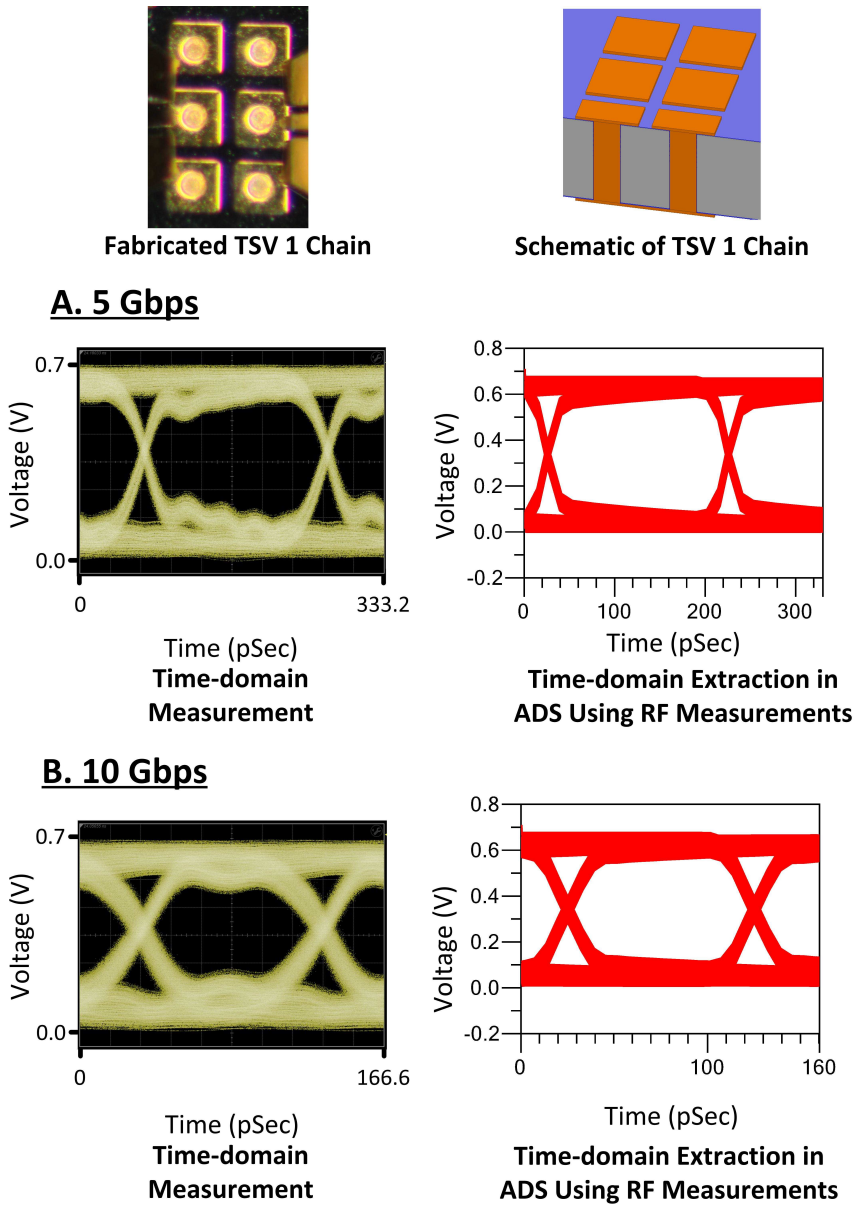



Figure 59: Time-domain measurements and extractions in ADS using RF measurements for TSV 1 chain.

performed to the TSVs with silicon dioxide liner, as shown in Figure 61. Moreover, using the eye-diagram extraction methodology in Keysight's ADS (Figure 46), eye diagrams are generated from the RF measurements of the fabricated polymer-embedded vias and from the HFSS simulations of the TSVs with 1 $\mu$m thick silicon dioxide liner and the same copper via dimensions. The time-domain characterization demonstrates an improvement in eye opening and timing jitter using polymer-embedded

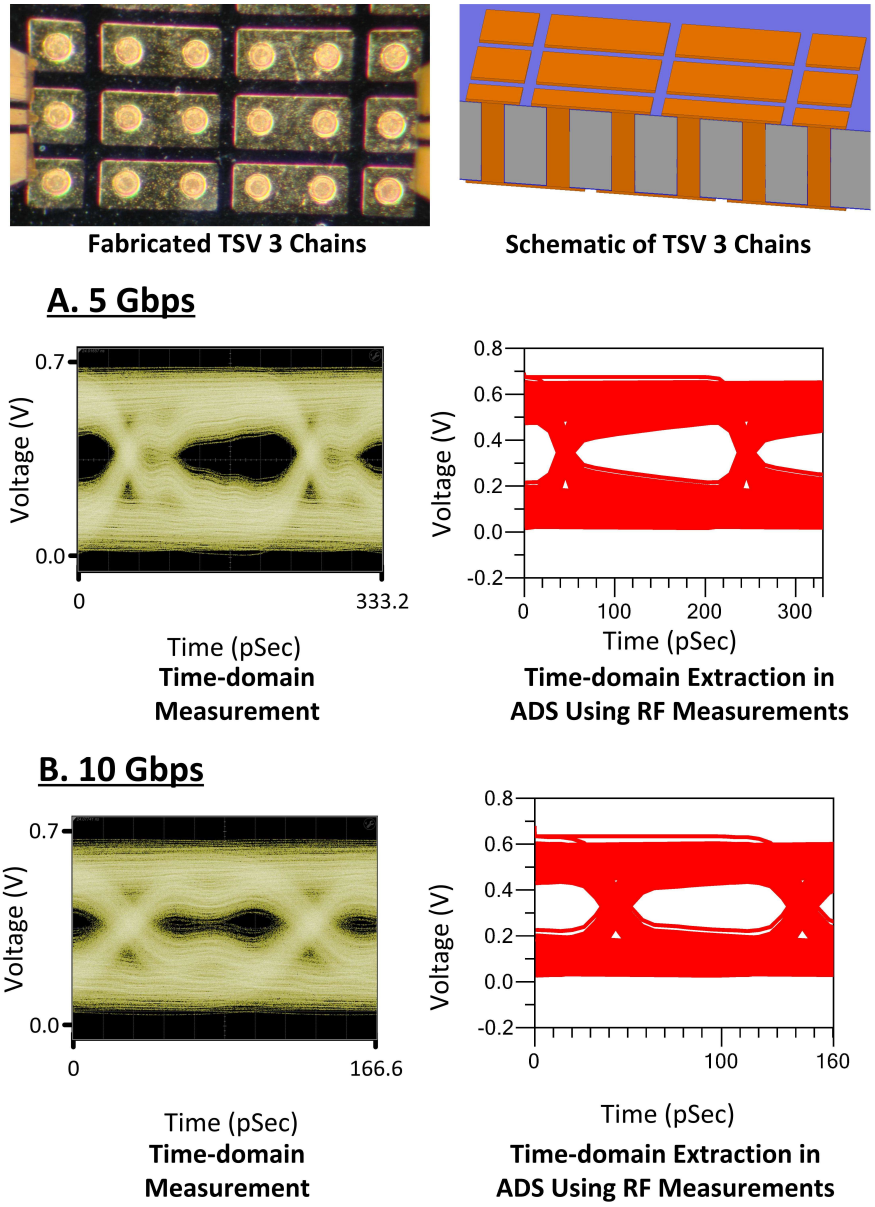



Figure 60: Time-domain measurements and extractions in ADS using RF measurements for TSV 3 chains.

vias compared to the TSVs with silicon dioxide liner.

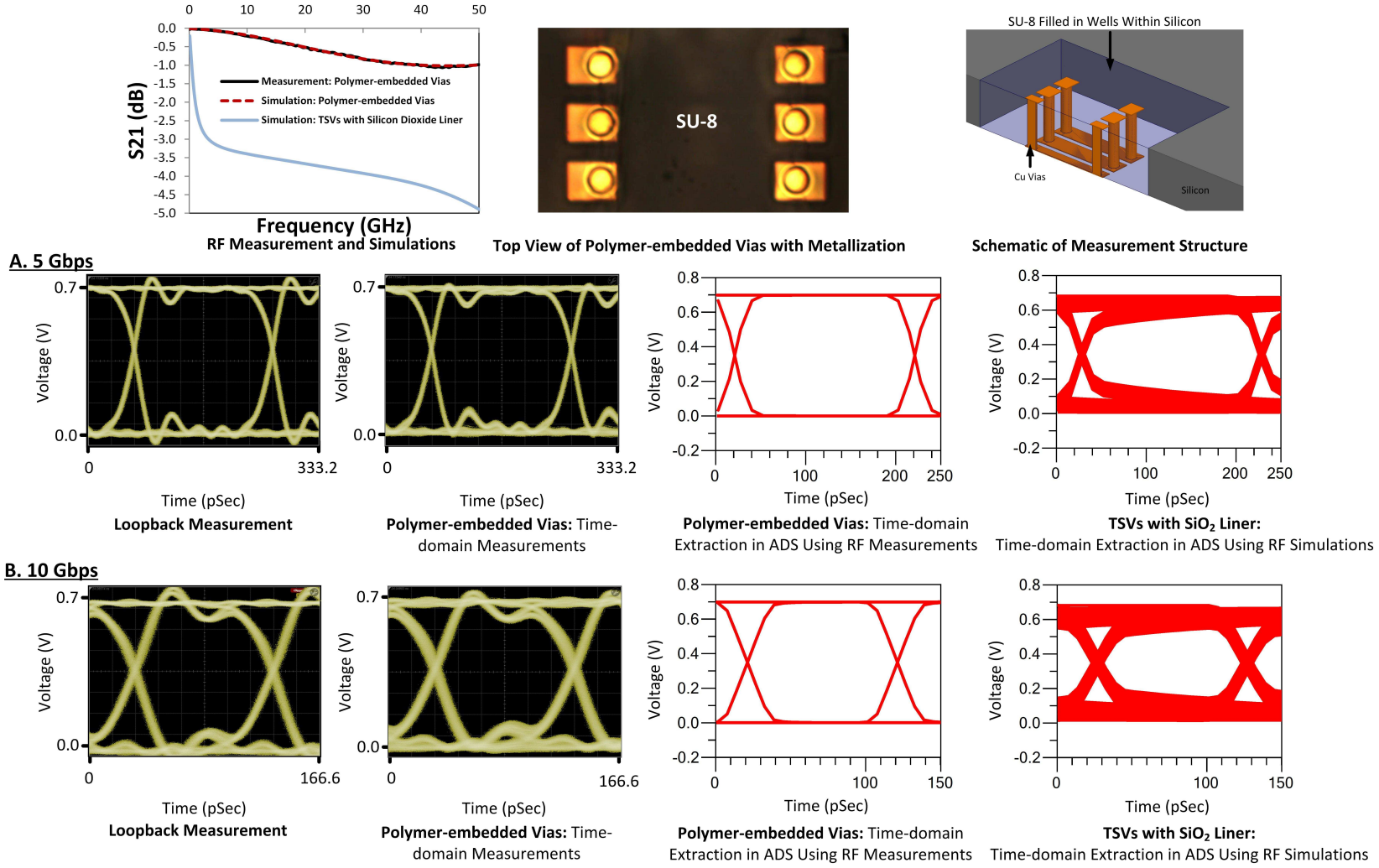



Figure 61: Measured eye diagrams of polymer-embedded vias (Figure 54) with constructed eye diagrams in ADS using the RF measurements of polymer-embedded via chains. Loopback measurement and extracted eye diagrams from the RF simulations of the TSVs with silicon dioxide liner are also shown for benchmarking.

## *4.4 TSV D-band Characterization*

In addition to the polymer-embedded via de-embedding up to 30 GHz and time-domain measurements, D-band measurements are demonstrated in order to understand their electrical performance for a large number of emerging applications in the D-band.

### 4.4.1 D-band Measurement Setup

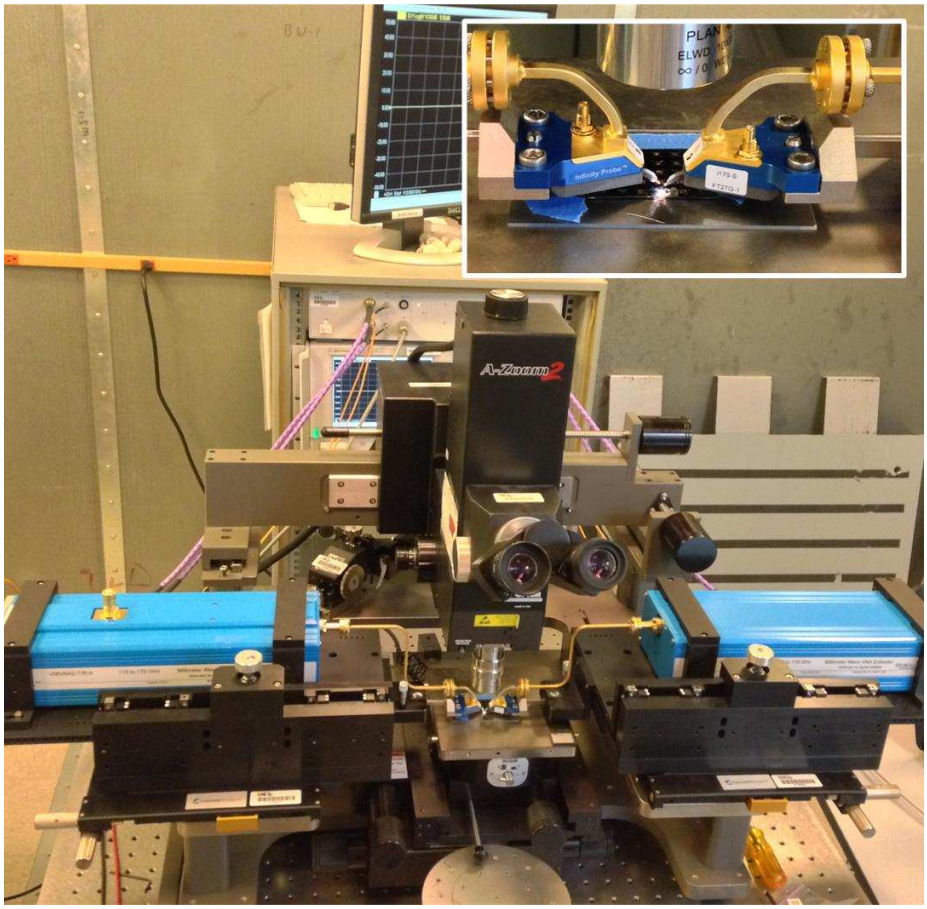


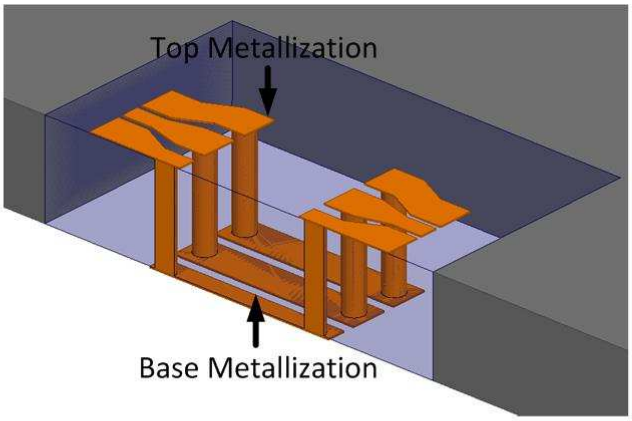
Figure 62: D-band measurement setup for polymer-embedded vias.

Applications such as wireless short-range communication, high-speed multimedia transfer, medical imaging, and high-speed pico-cell cellular links have been explored in the D-band (110-170 GHz) [23]. For the D-band measurements of polymer-embedded vias, a setup including a Keysight E8361C vector network analyzer extended with

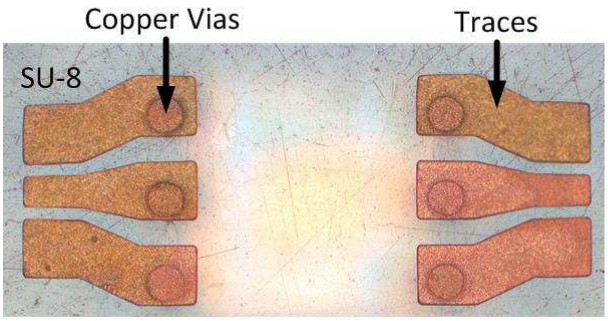
an N5260A mm-wave controller and V06VNA2 mm-wave test heads was used with Cascade MicroTech Infinity 75 $\mu$m pitch D-band probes, as shown in Figure 62. Prior to the TSV measurements, calibration of the probes was performed using the LRRM protocol. The measured results are compared to ANSYS HFSS simulations, and benchmarked to simulations of the TSVs with 1 $\mu$m thick silicon dioxide liner (10 $\Omega$-cm silicon resistivity) and the same dimensions.

### 4.4.2 Fabrication and D-band Measurements of Polymer-embedded Vias

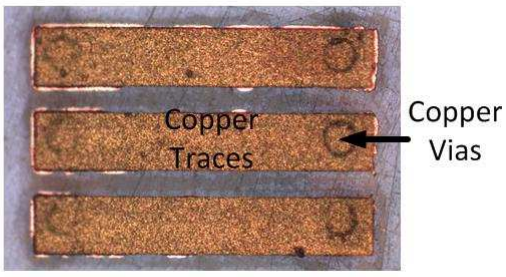
For D-band characterization of polymer-embedded vias, longer traces with fan-in are fabricated to measure using the Cascade MicroTech Infinity 75 $\mu$m pitch D-band probes, as shown in Figure 63.




**Schematic of Structure for D-band Measurements**




**Top View of Fabricated TSV Link**




**Base View of the TSV Link**

Figure 63: Fabricated polymer-embedded vias for measurements in the D band including traces with fan-in at top.

The D-band measurements of a polymer-embedded via link are demonstrated in Figure 64, showing 1.5 dB insertion loss at 170 GHz. Compared to the simulated insertion loss of a link consisting of the TSVs with silicon dioxide liner, a significant reduction in the insertion loss can be obtained using the polymer-embedded vias.

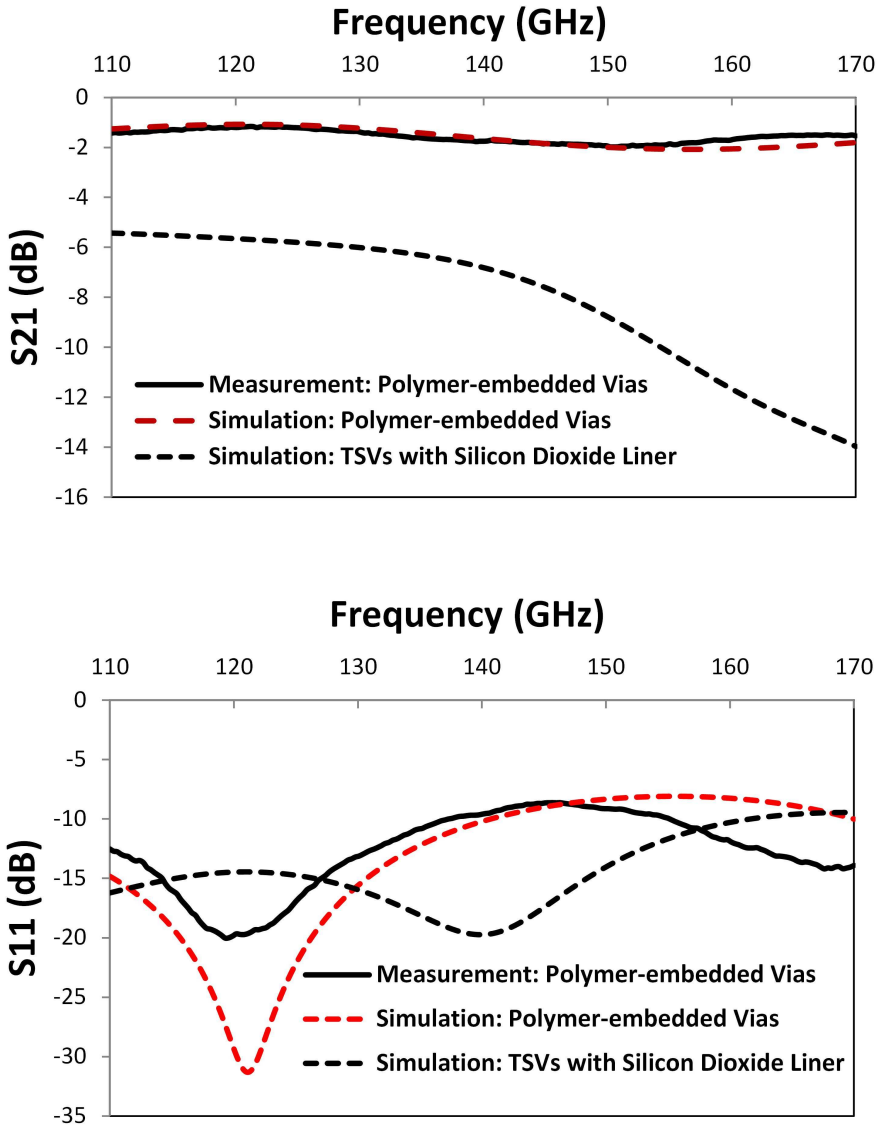


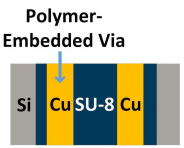
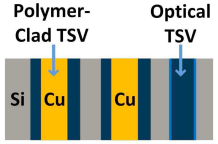
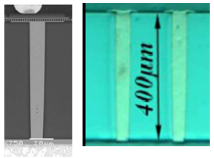
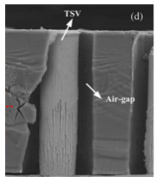
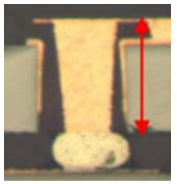
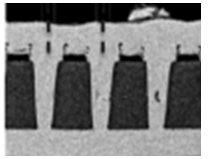

Figure 64: D-band measurements and simulations of a polymer-embedded via link; TSVs with silicon dioxide liner included for benchmarking.

## *4.5 Technology Comparison and Chapter Conclusion*

Table 8 compares the demonstrated photodefined polymer-embedded vias with other competing TSV technologies from the literature [25, 30, 42, 46, 84, 85]. The polymer-embedded vias have dimensions similar to the TSVs with silicon dioxide liner for 400 $\mu$m thick silicon interposers found in the literature. Moreover, the polymer-embedded vias attain significant reductions in TSV loss compared to the TSVs with silicon dioxide liner with a relative ease of fabrication due to the photodefinition based silicon interposer technology.

In conclusion, this chapter has demonstrated RF and time-domain analysis and measurements of polymer-embedded vias and the TSVs with silicon dioxide liner for benchmarking. L-2L and open-short techniques were implemented to perform RF de-embedding of the fabricated polymer-embedded vias. Moreover, the extracted parasitics of the de-embedded polymer-embedded vias demonstrate a reduction in the capacitance and conductance of the polymer-embedded vias compared to the TSVs with silicon dioxide liner. Additionally, time-domain measurements were demonstrated up to 10 Gbps showing an improved eye opening and timing jitter using polymer-embedded vias. Moreover, D-band measurements were demonstrated for polymer-embedded via links showing a lower loss compared to the TSVs with silicon dioxide liner.

Table 8: Comparison of polymer-embedded vias with other TSV technologies from the literature.

| No. | Parameters | Polymer-embedded vias | Polymer-clad TSVs | $SiO_2$ liner TSVs [25]/ [30] | Air liner TSVs [46] | Laser ablated coax [84] | Photodefined coax [42] | Glass Vias [85] |
|---|---|---|---|---|---|---|---|---|
| 1 | Images |  |  |  |  |  |  |  |
| 2 | Copper via diameter | 100/65 $\mu$m | 80 $\mu$m | 10/50 $\mu$m | 20 $\mu$m | 70 $\mu$m | 100 $\mu$m | 15 $\mu$m at top |
| 3 | TSV height | 270/370 $\mu$m | 390 $\mu$m | 100/400 $\mu$m | 65 $\mu$m | 150 $\mu$m | 300 $\mu$m | 30 $\mu$m |
| 4 | TSV pitch | 250/150 $\mu$m | 250 $\mu$m | 150/180 $\mu$m | 50 $\mu$m | Surrounded by non-coax | 500 $\mu$m | 27 $\mu$m |
| 5 | Loss at high frequency | Very low | Low | High | Low | Very low | Very low | Very low |
| 6 | Ease of fabrication | High | High | Very high | Low | Moderate | Moderate | Moderate |
| 7 | Special features | Photodefinition | Photodefinition and optical TSVs | Simpler fabrication | Metallization over air liners | Coax and non-coax in parallel | Photodefinition | Panel-scale fabrication |

# CHAPTER V

# COMPONENTS FOR MIXED-SIGNAL SILICON INTERPOSER PLATFORM: APPLICATIONS OF THE PHOTODEFINED POLYMER-ENHANCED SILICON INTERPOSER TECHNOLOGY

## *5.1 Mixed-signal Silicon Interposer Platform*

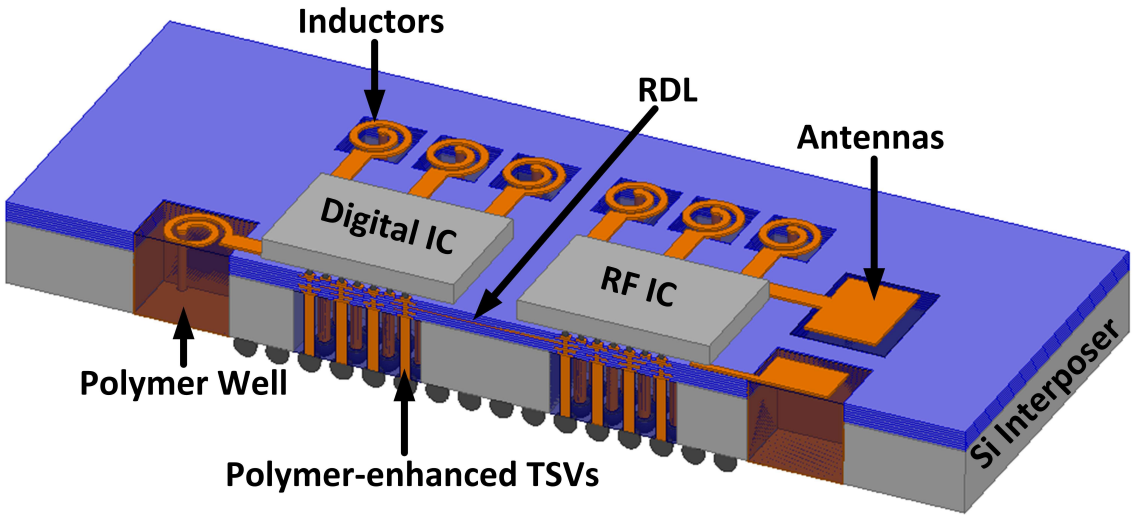



Figure 65: Envisioned mixed-signal silicon interposer platform featuring polymer-enhanced TSVs, antennas and inductors.

As described in the introduction, silicon interposers with dense fine-pitch metallization and through-silicon vias (TSVs) have been widely explored for high bandwidth-density communication and provide a platform for heterogeneous IC and passive integration [20, 24–31, 34]. However, the TSVs in silicon interposers have high losses and frequency-dependent impedance variations, and the presence of silicon underneath antennas and inductors results in a lower radiation efficiency and Q-factor, respectively.

In this chapter, the photodefined polymer-enhanced silicon interposer technology leading to the development of polymer-embedded vias in the prior chapters, is explored in order to demonstrate: (1) coaxial copper vias within photodefined polymer wells in a silicon interposer showing a wideband impedance matching and low loss; (2) W-band antennas over metal-coated polymer wells showing a 10-dB return loss bandwidth of 13.35 GHz around 100 GHz; and (3) inductors over metal-coated shallow polymer wells showing a peak Q-factor greater than 50. A mixed-signal silicon interposer platform featuring the proposed polymer-enhanced technologies is shown in Figure 65 and the proposed technology demonstrations are described as follows.

## *5.2 Polymer-enhanced Coaxial TSVs*

### 5.2.1 Fabrication of Coaxial TSVs

A coaxial interconnect configuration of polymer-embedded vias is demonstrated using the fabrication process shown in Figure 66. The proposed process is similar to that for the GSG configuration in the prior chapters (Figure 35). The fabrication of coaxial vias begins with the etching of wells in a silicon wafer containing a copper seed layer at the base followed by SU-8 coating, photodefinition, via electroplating and CMP to remove the additional copper at the top of the vias. Next, top metallization is fabricated yielding coaxial vias electrically shorted at the base. After the measurement of the short structure, the copper layer at the base is removed using CMP yielding coaxial vias that are electrically open at the base.

### 5.2.2 One-port Measurements and Impedance Extraction

To perform one-port measurements of coaxial vias and extract their impedances, Figure 67 illustrates the fabricated 285 $\mu$m tall polymer-enhanced coaxial vias within an 1800 $\mu$m x 1800 $\mu$m well in silicon prior to top layer metallization. The copper via diameter is 65 $\mu$m and the signal-to-ground via pitches are 150 $\mu$m and 125 $\mu$m. The coaxial vias with 125 $\mu$m pitch also show that polymer-enhanced vias (the

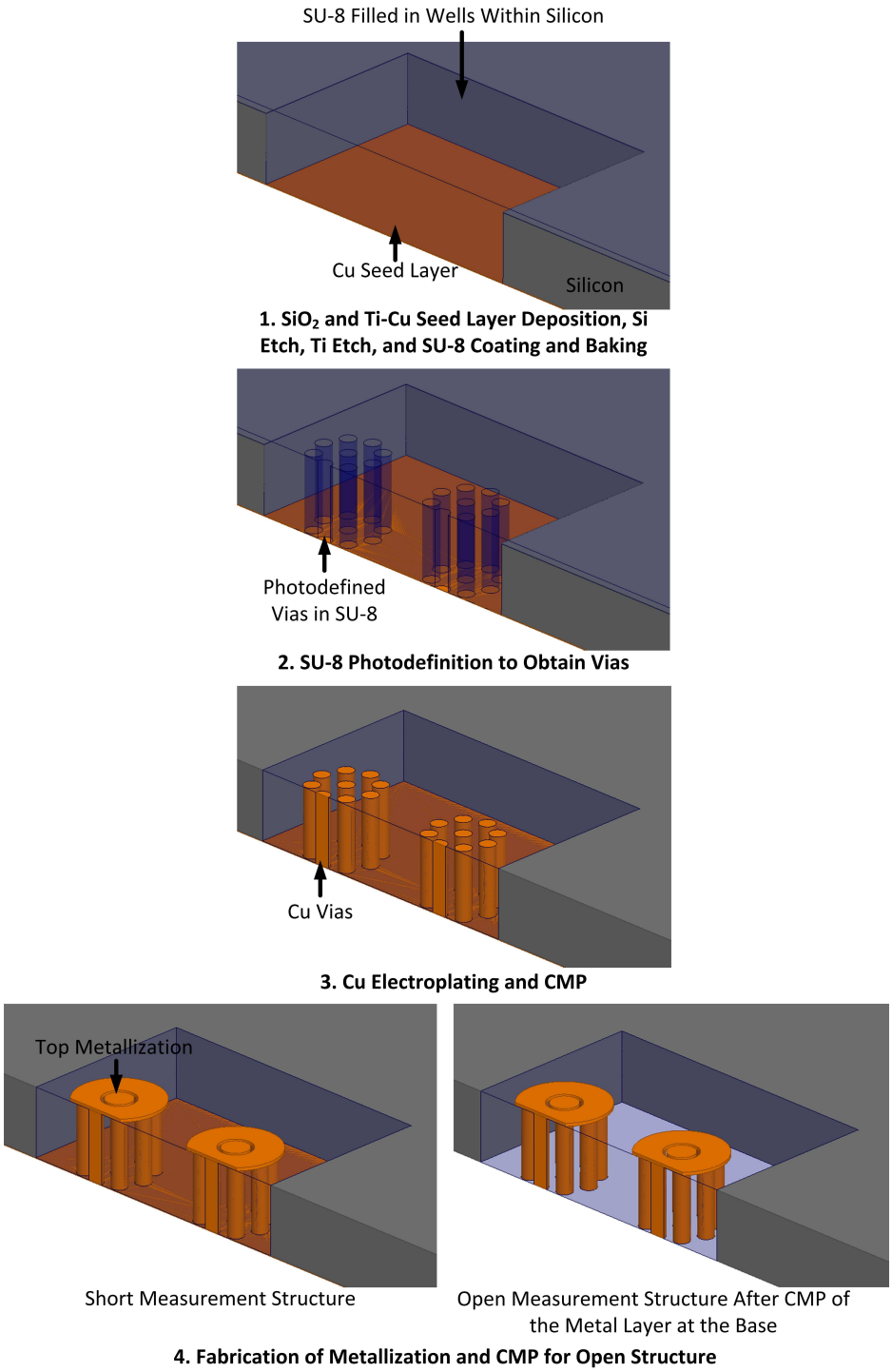



Figure 66: Fabrication process of coaxial vias.

ground vias) with a distance of 30 $\mu$m (i.e. 95 $\mu$m pitch) between the vias have been demonstrated.

High-frequency measurements were performed from 1 GHz to 50 GHz for the

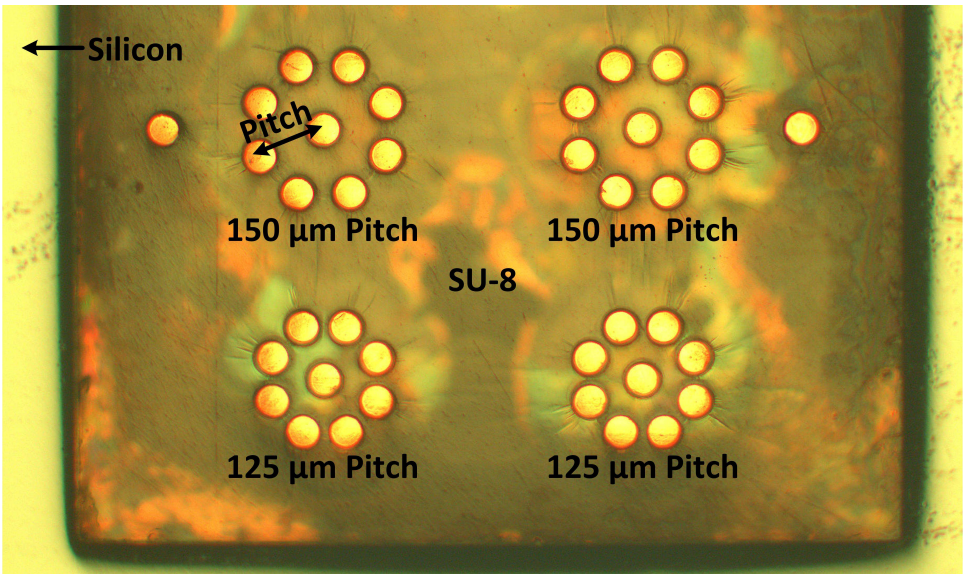



Figure 67: Fabricated coaxial vias for 1-port measurements.

fabricated coaxial vias, as shown in Figure 68. Using the measured $S$-parameters, $Z$-parameters and $Y$-parameters are obtained with 50 Ω as the reference impedance. Using the $Z$-parameters of the short structure, $R$ and $L$ are extracted, and using the $Y$-parameters of the open structure, $C$ and $G$ are extracted, as shown in the following equation [99]:

$$R = Re\left(Z_{11}\right); \tag{31}$$

$$L = \frac{Im\left(Z_{11}\right)}{\omega}; \tag{32}$$

$$G = Re\left(Y_{11}\right); \text{ and} \tag{33}$$

$$C = \frac{Im\left(Y_{11}\right)}{\omega}. \tag{34}$$

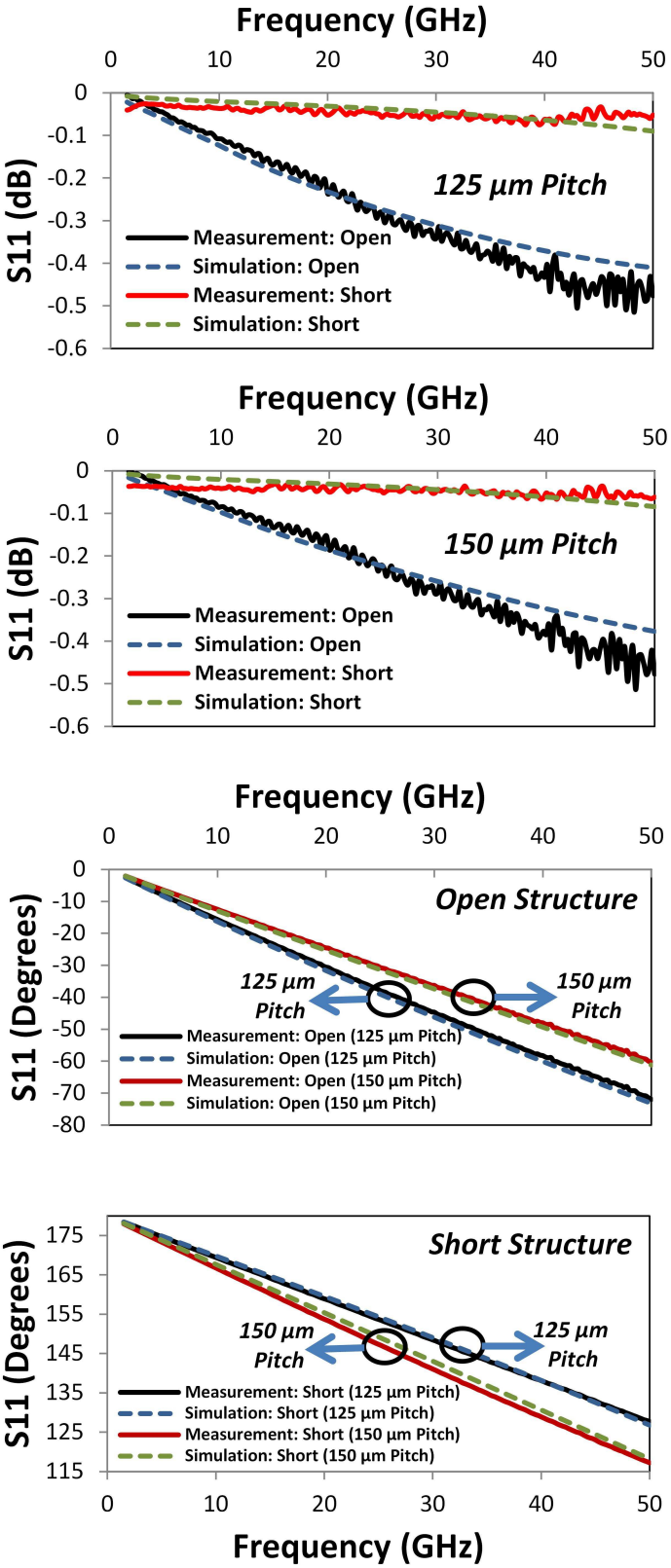



Figure 68: Single-port RF measurements of coaxial TSVs.

Using the extracted $RLGC$, impedance is evaluated as follows:

$$Z = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}}. \tag{35}$$

The extracted impedances from the one-port coaxial via measurements are shown in Figure 69, demonstrating a wideband impedance matching to approximately 50 Ω using the 150 $\mu$m pitch vias and approximately 40 Ω using the 125 $\mu$m pitch vias. Moreover, a two-port simulation of the coaxial TSVs in HFSS (yielding 0.1 dB insertion loss per coaxial via at 50 GHz) demonstrates a 55% reduction in insertion loss at 50 GHz compared to a GSG via configuration with the same copper via dimensions and signal-to-ground via pitch.

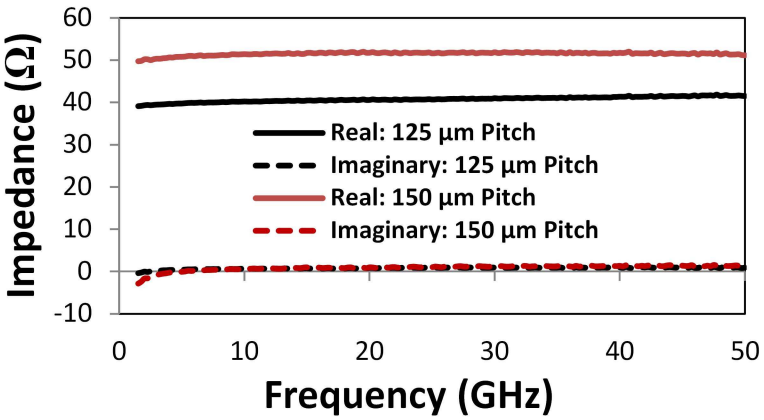



Figure 69: Extracted impedance from the coaxial TSV measurements.

### 5.2.3 Coupling Measurements

In addition to the one-port measurements, coupling measurements are also demonstrated. For the coupling measurements, coaxial and non-coaxial configurations are fabricated. As shown in Figure 70, 285 $\mu$m tall and 65 $\mu$m diameter polymer-enhanced coaxial TSVs are fabricated within 1800 $\mu$m x 1800 $\mu$m wells in silicon; the signal-to-ground via pitches are 150 $\mu$m and 175 $\mu$m. To fabricate the horizontal metallization over the coaxial via structures for coupling measurements, following the fabrication

of coaxial copper vias (Figure 66, step 3), the seed layer at the base is removed using CMP. Next, a metallization layer is formed over the fabricated vias to electrically short the ground vias and perform signal-to-signal copper via coupling measurements.

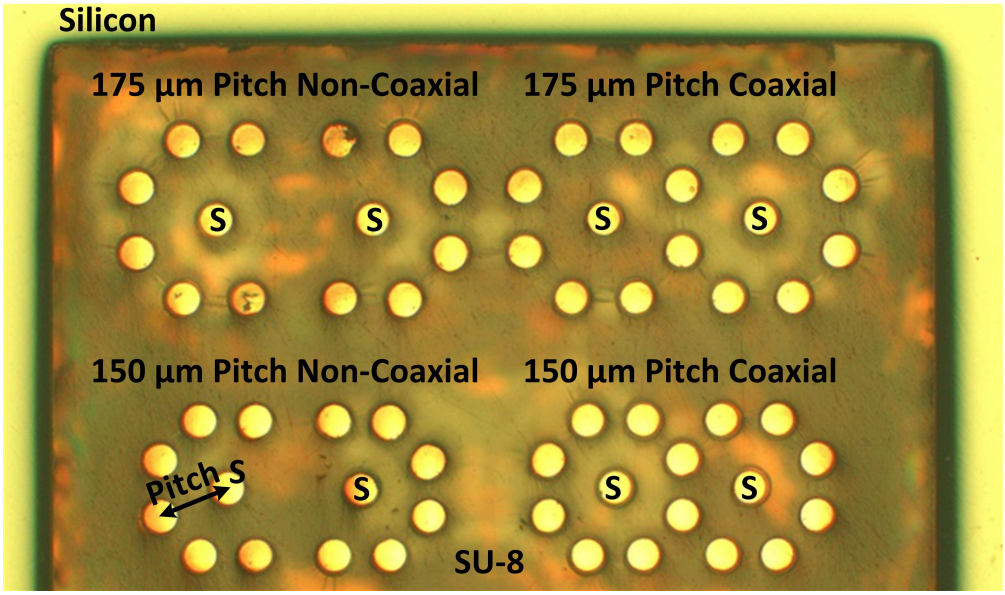



Figure 70: Fabricated polymer-enhanced coaxial vias and non-coaxial vias (for benchmarking).

In the measured frequency band of 10 MHz to 50 GHz, the coaxial configuration attains an average of 14.5 dB and 13.1 dB reduction in the signal-to-signal via coupling compared to the corresponding non-coaxial structures at 150 $\mu$m and 175 $\mu$m signal-to-ground via pitches, respectively, as shown in Figure 71.

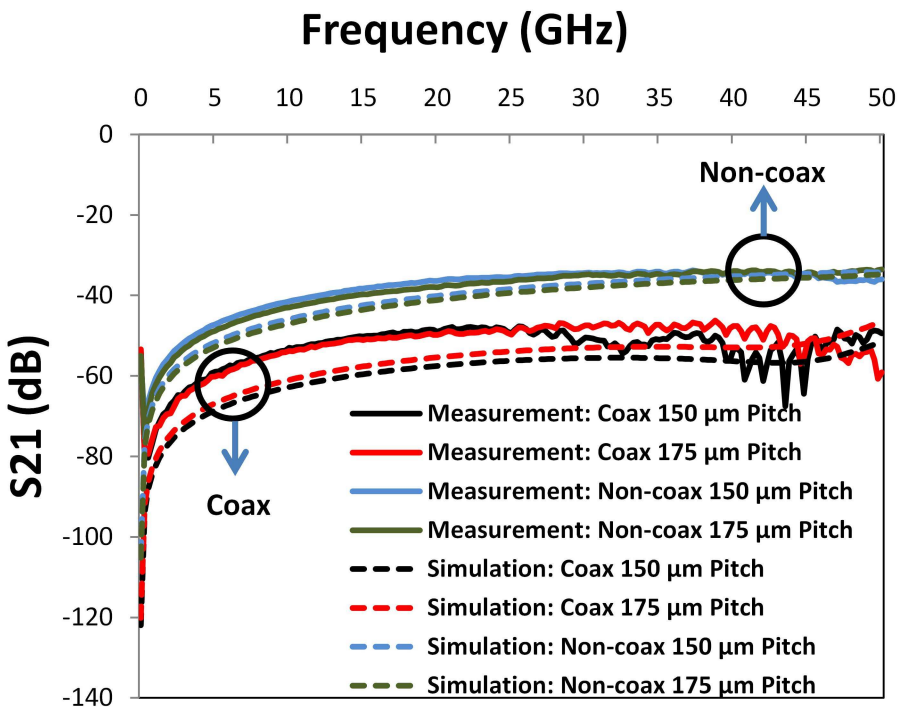


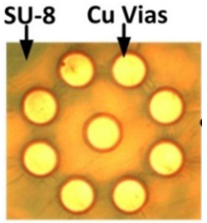
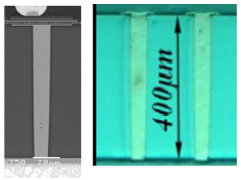
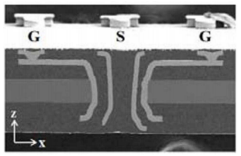
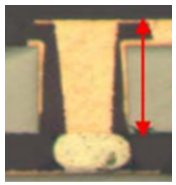

Figure 71: Coupling measurements of the fabricated polymer-enhanced coaxial and non-coaxial TSVs.

### 5.2.4 Coaxial TSVs: Technology Comparison

The photodefined polymer-enhanced coaxial vias are compared to the coaxial TSVs and the TSVs with silicon dioxide liner from the literature, as shown in Table 9. The literature includes laser-ablated ABF based coaxial TSVs with annular and cylindrical signal conductors, and photodefined coaxial TSVs fabricated using a temporary release layer [42, 84, 112].

Compared to the TSVs with silicon dioxide liner, an ultra-low loss electrical performance is shown using the polymer-enhanced coaxial vias. Moreover, scaled coaxial via dimensions using a simpler photodefinition-based fabrication process have been demonstrated in this research compared to the literature.

Table 9: Comparison of the demonstrated coaxial vias to other coaxial TSV technologies from the literature.

| No. | Parameters | **Photodefined coax vias** | $SiO_2$ **liner TSVs** [25]/ [30] | **Laser ablated annular coax** [112] | **Laser ablated coax** [84] | **Photodefined coax** [42] |
|---|---|---|---|---|---|---|
| **1** | **Images** |  |  |  |  |  |
| **2** | **Copper via diameter** | 65 $\mu$m | 10/50 $\mu$m | 42 $\mu$m | 70 $\mu$m | 100 $\mu$m |
| **3** | **TSV height** | 285 $\mu$m | 100/400 $\mu$m | 205 $\mu$m | 150 $\mu$m | 300 $\mu$m |
| **4** | **TSV pitch** | 150/125/95 $\mu$m | 150/180 $\mu$m | 450 $\mu$m | Surrounded by non-coax | 500 $\mu$m |
| **5** | **Insertion loss at high frequency** | 0.1 dB at 50 GHz (for one coaxial TSV) | ~1.2 dB at 29 GHz (for a chain with 2 TSVs) | ~5.5 dB at 20 GHz (for a chain with 4 TSVs) | 0.044 dB at 10 GHz (for one coaxial TSV) | ~0.25 dB at 10 GHz (for a TSV-trace link) |
| **6** | **Ease of fabrication** | High | Very high | Moderate | Moderate | Moderate |
| **7** | **Special features** | Photodefinition | Simpler fabrication | Laminated ABF with laser ablation | Coax and non-coax in parallel | Photodefinition |

## 5.3 Polymer-enhanced W-band Antennas

### 5.3.1 Antenna Fabrication

Using the photodefined polymer-enhancement technology, W-band antennas are explored in this research to enable their fabrication in parallel to the demonstrated polymer-enhanced TSVs.

#### *5.3.1.1 Selection of Antenna Type*

Various microfabricated antenna types such as patch, folded dipole, slot, and Yagi-Uda have been explored in the literature [19, 20, 114, 115]. Patch antennas have been selected in this research owing to their ease of fabrication and good radiation control [116].

#### *5.3.1.2 Selection of Antenna Shape*

The rectangular patch has been selected instead of circular, elliptical, triangular or annular shapes in order to achieve higher gain and bandwidth [116].

#### *5.3.1.3 Fabrication Process*

As shown in Figure 72, the fabrication of the antennas begins with the etching of wells in a silicon wafer with a silicon dioxide etch stop layer at the base followed by silicon nitride and copper deposition over the etched wells. Next, SU-8 filling and photodefinition, copper electroplating, and CMP are performed. Following CMP, antennas are fabricated over the polymer-filled wells using a lift-off process of titanium, copper and gold.

#### *5.3.1.4 Fabrication Result*

Figure 73 shows the fabricated 1100 $\mu$m x 650 $\mu$m and 2 $\mu$m thick patch antennas over 1530 $\mu$m x 1030 $\mu$m and 280 $\mu$m deep wells.

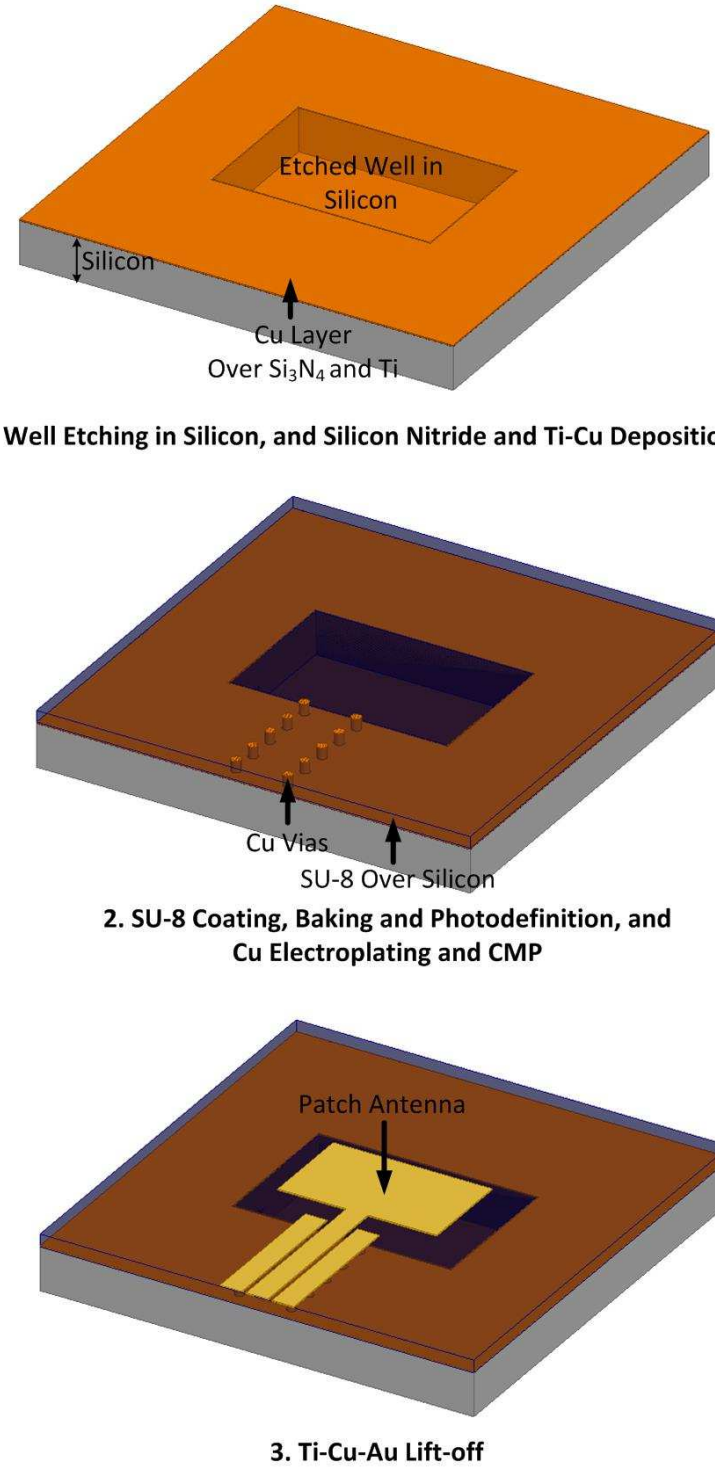



Figure 72: Fabrication process of polymer-enhanced antennas.

### 5.3.2 Antenna Measurement

High-frequency measurements were performed for the fabricated antennas from 60 GHz to 110 GHz demonstrating a 13.35 GHz 10-dB return loss bandwidth at the

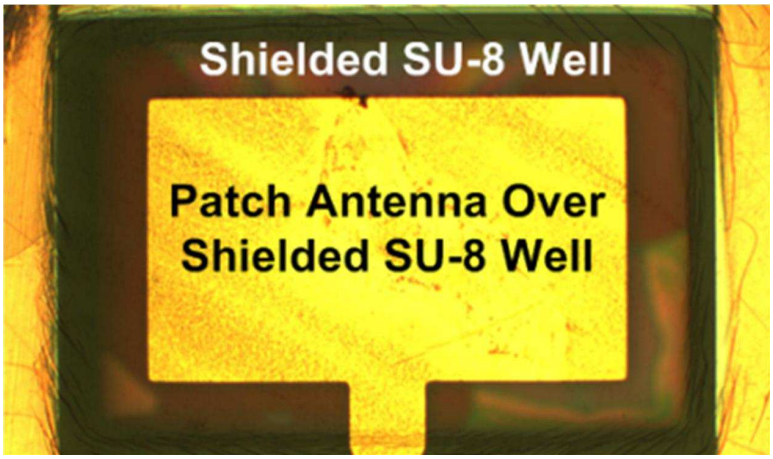
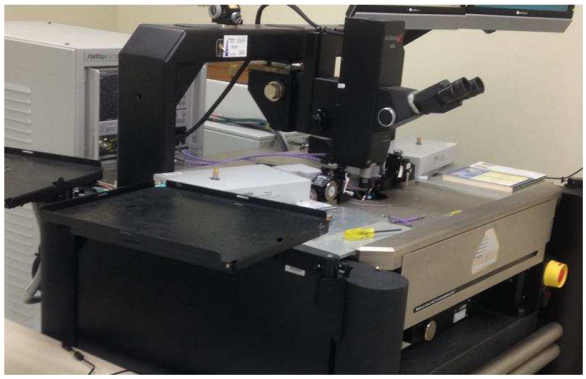



Figure 73: Fabricated patch antenna over a metal-coated polymer well.

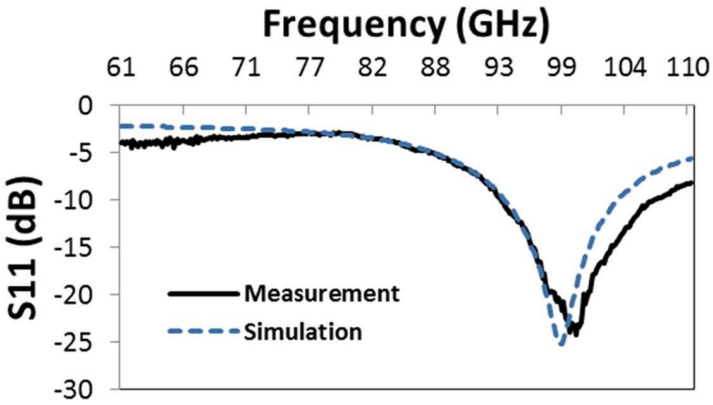
center frequency of 100 GHz, as shown in Figure 74. Moreover, HFSS simulation of the fabricated antenna show a gain of 4.4 dBi and 70% radiation efficiency at 100 GHz. A radiation pattern simulation is shown in Figure 74(c) demonstrating a high-gain primary lobe. A further improvement in the gain, radiation efficiency and radiation pattern could be obtained by improving the antenna and feed designs, and using a polymer material with a lower loss tangent (BCB, for example).

### 5.3.3 Antennas: Technology Comparison

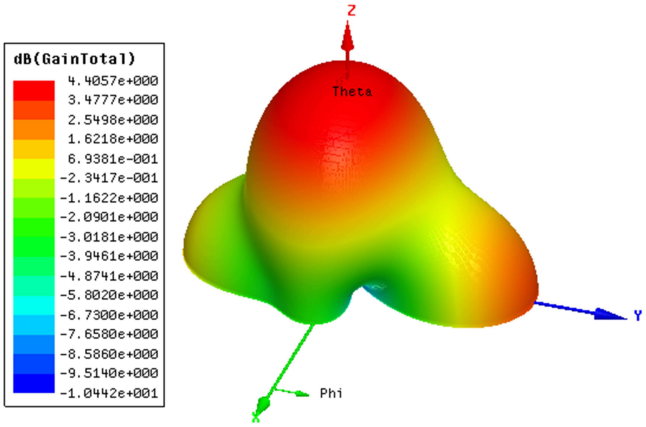
The demonstrated polymer-enhanced antenna on interposer is compared to select similar off-chip antennas from the literature, as shown in Table 10. The literature includes antennas over (1) high-resistivity silicon with cavity backing, (2) molding material, (3) suspended SU-8 substrate, and (4) polymer-filled wells [19, 20, 117, 118]. The gain of the demonstrated antenna is close to the gains of the similar off-chip antennas in the literature. Moreover, the demonstrated antenna is easy to fabricate.



(a)



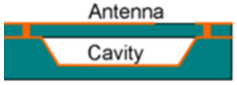
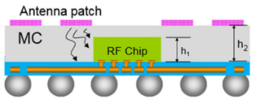
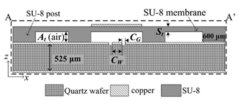
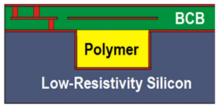

(b)




(c)

Figure 74: Antenna measurement and simulations: (a) Setup; (b) One-port measurement and simulation; and (c) Radiation pattern simulation at 100 GHz.

Table 10: Comparison of the demonstrated antenna to other off-chip antennas from the literature.

| No. | Parameters | **Photodefined polymer well** | **High-resistivity silicon** [20] | **Molding material** [117] | **Suspended SU-8** [118] | **Polymer well** [19] |
|---|---|---|---|---|---|---|
| **1** | **Images** |  |  |  |  |  |
| **2** | **Antenna type** | CBCPW-fed patch | Microstrip-fed folded dipole | Aperture-coupled patch | Conductor-backed slot fed patch | CPW-fed cavity-backed slot |
| **3** | **Antenna size** | 1100 $\mu$m by 650 $\mu$m over 280 $\mu$m deep wells | Over 120 $\mu$m thick high-resistivity silicon and 275 $\mu$m deep cavity | 890 $\mu$m by 1020 $\mu$m over 300 $\mu$m molding material | 1250 $\mu$m by 1500 $\mu$m over 100 $\mu$m thick SU-8 with 200 $\mu$m air underneath | 1300 $\mu$m by 300 $\mu$m over 150 $\mu$m deep wells |
| **4** | **Substrate underneath** | SU-8 | High-resistivity silicon and air cavity | Molding material with $\epsilon_r$ of 4 | Suspended SU-8 | Polymer with $\epsilon_r$ of 2.65 in well and BCB |
| **5** | **Gain** | 4.4 dBi at 100 GHz | 4-7.9 dBi in the 57-66 GHz band | 5.1 dBi in the 57-66 GHz band | 5.5-7 dBi in the 57-66 GHz band | 6.26 dBi at 135 GHz |
| **6** | **10 dB bandwidth** | 13.35 GHz around 100 GHz | 15 GHz around 60 GHz | 10 GHz around 60 GHz | 10 GHz around 60 GHz | 25 GHz in the 117-142 GHz band |
| **7** | **Ease of fabrication** | High | Moderate | High | Moderate | Moderate |

## 5.4 Polymer-enhanced Inductors

### 5.4.1 Fabrication of Inductors

Using the photodefined interposer technology, high Q-factor inductors are demonstrated over polymer wells in thick silicon interposers. The proposed inductors can be fabricated in parallel to the polymer-enhanced TSVs, easing the fabrication of the envisioned silicon interposer system shown in Figure 65.

#### *5.4.1.1 Depth of Well*

The inductors are fabricated over shallow wells (100 $\mu$m deep) in a silicon wafer to ease fabrication and since a significant improvement is not observed in the Q-factor beyond 100 $\mu$m well depth.

#### *5.4.1.2 Selection of Inductor Shape*

Spiral inductors have been implemented with the photodefined copper vias in the polymer wells to show the benefits of the photodefined polymer-enhanced silicon interposer technology using a simpler inductor geometry.

#### *5.4.1.3 Inductors Without Wells*

Alongside the inductors over wells, inductors are demonstrated over a thick polymer layer in order to (1) understand the impact from the wells in silicon, (2) calibrate/validate HFSS simulations for the inductors, and (3) demonstrate another high-Q inductor technology with a simpler fabrication process in parallel to the polymer-enhanced TSVs. Similar inductors over a thick SU-8 layer have been shown by A. Ghannam et al. [119].

#### *5.4.1.4 Fabrication Process*

As shown in Figure 75, the fabrication of inductors begins with the etching of wells in a silicon wafer followed by silicon nitride and titanium-copper deposition. Next,

SU-8 filling, photodefinition, copper electroplating and CMP are performed followed by the fabrication of the electroplated inductors.

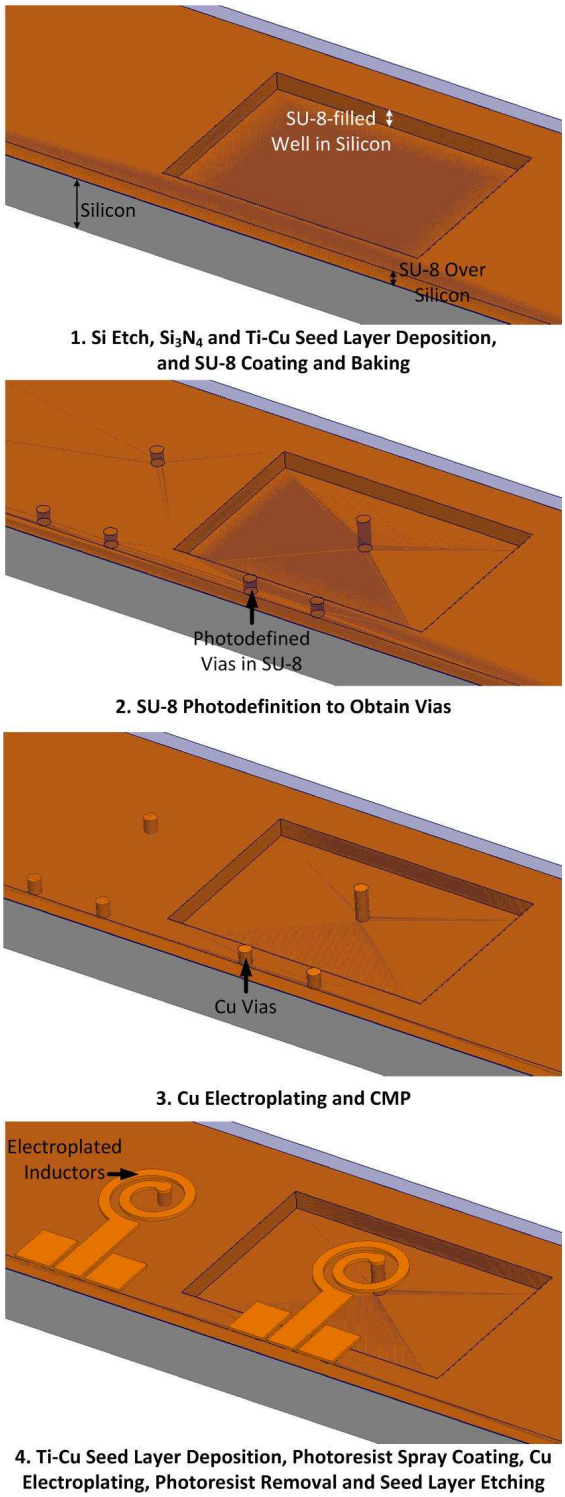



Figure 75: Fabrication process of polymer-enhanced inductors.

#### 5.4.1.5 *Advantage of the Proposed Inductor Technology*

An advantage of the proposed inductors is that they could be implemented as post-processing technologies for silicon interposers (with metallization and TSVs) from different vendors. When used as a post-processing technology, the inductors also provide ease of fabrication compared to inductors found in the literature over non-photodefinable dielectrics [120, 121] since a mechanical polishing after filling the wells is not required in order to implement the inductors.

#### 5.4.1.6 *Fabrication Results*

Figure 76 illustrates the fabricated 8-12 $\mu$m thick inductors with 55-65 $\mu$m trace width and 100 $\mu$m trace pitch. The inductors over an SU-8 layer (80 $\mu$m thick) are shown with 1.5, 2.5 and 3.5 turns and the inductors over wells (1530 $\mu$m x 1030 $\mu$m and 100 $\mu$m deep with additional 80 $\mu$m SU-8 on top) are shown with 1.5 turn. The 80 $\mu$m thickness results from the spin speed required during SU-8 coating to fill the 100 $\mu$m deep wells without voids.

### 5.4.2 One-port Measurements and $Q$ and $L$ Extraction

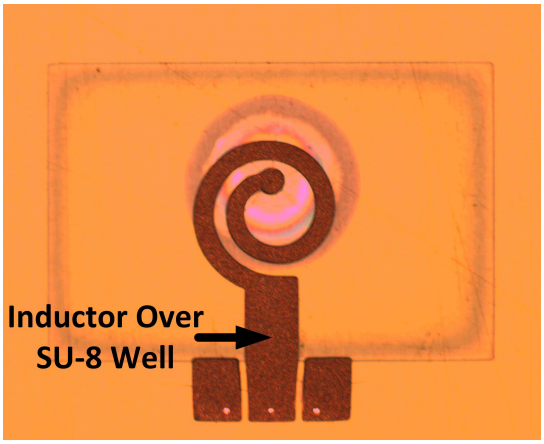
High-frequency measurements were performed for the fabricated inductors up to 50 GHz. Inductance and Q-factors are extracted using the following formulas [122]:

$$L = \frac{Im\left(\frac{1}{Y_{11}}\right)}{\omega}; \text{ and} \tag{36}$$

$$Q = \frac{Im\left(\frac{1}{Y_{11}}\right)}{Re\left(\frac{1}{Y_{11}}\right)}. \tag{37}$$

As shown in Figure 77, the fabricated inductors over a thick polymer layer demonstrate a peak Q-factor of 37.5 at 7.5 GHz ($f_{Q_{peak}}$) and a 0.78 nH inductance at $f_{Q_{peak}}$


(a)

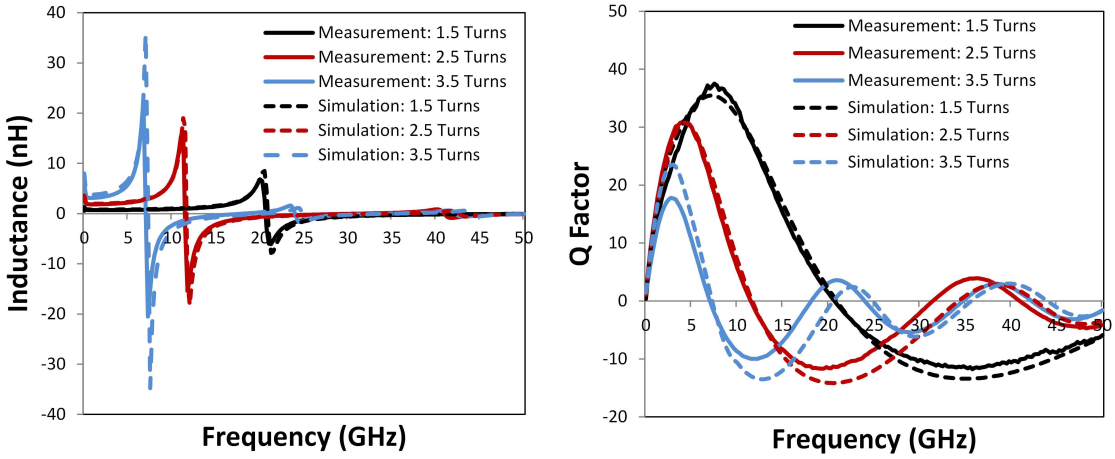



(b)

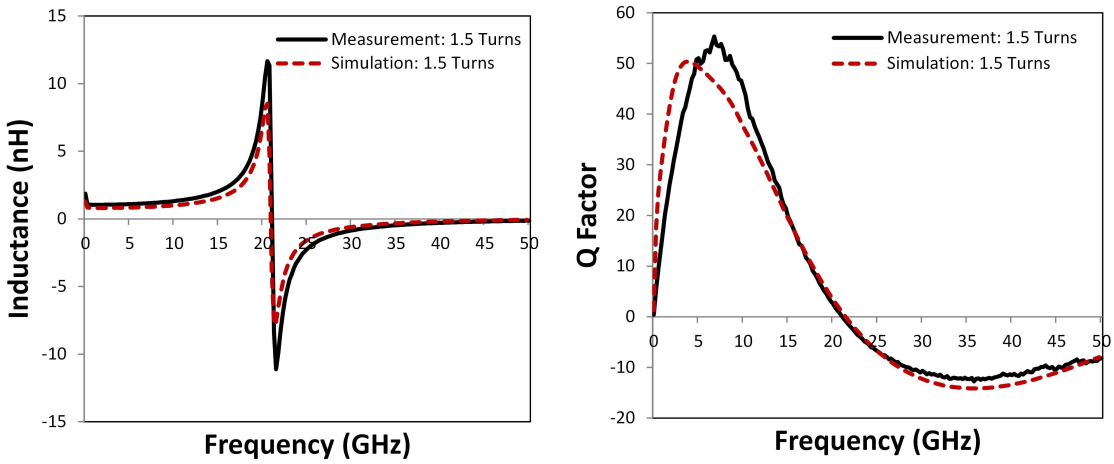
Figure 76: Fabricated inductors over: (a) thick SU-8 layer and (b) polymer well.

with a self-resonance frequency (SRF) at 20 GHz for the 1.5 turn inductor. Moreover, the fabricated inductor over polymer well with 1.5 turns demonstrates a peak Q-factor of 55 at 6.75 GHz and a 1.14 nH inductance at $f_{Q_{peak}}$ with an SRF at 21 GHz.

To enhance the performance of these inductors, increasing the metal thickness or using high-conductivity metal (such as silver) could improve the Q-factor at lower frequencies. Moreover, using a lower loss polymer material (such as BCB) could improve the Q-factor at higher frequencies [14]. Additionally, reducing the length of the feed line could also improve the Q-factor [121].




(a)




(b)

Figure 77: Measurements of inductors over: (a) thick SU-8 layer and (b) polymer well.

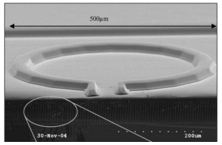
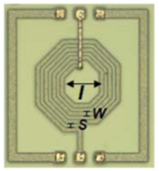
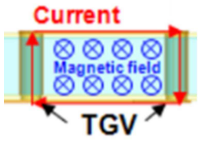
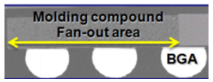
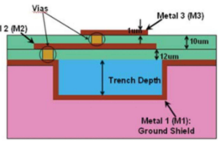
### 5.4.3 Inductors: Technology Comparison

The demonstrated polymer-enhanced inductors on interposer are compared to similar selected off-chip inductors from the literature, as shown in Table 11. The literature includes inductors that are (1) over dielectric coated trenched silicon, (2) over glass interposers, (3) using vias in the glass interposers, (4) under a molding compound, and (5) over polymer wells [14,34,37,120]. The inductors in this research and the inductor over dielectric coated trenched silicon [14] are implemented using one-port measurement structures and the remaining inductors shown from the literature are two-port measurement structures. Moreover, the inductors in this research are easy to fabricate.

## *5.5 Chapter Conclusion*

In conclusion, this chapter has demonstrated applications of the photodefined polymer-enhanced silicon interposer technology (demonstrated in the prior chapters), including high-performance polymer-enhanced coaxial TSVs, antennas and inductors. The coaxial TSVs were demonstrated with an impedance-controlled design, and they shows a significant reduction in TSV coupling and loss. Moreover, a polymer-enhanced W-band antenna with high gain and radiation efficiency was demonstrated. Additionally, using the photodefined silicon interposer technology, high-Q (>50) inductors were demonstrated.

Table 11: Comparison of the demonstrated inductor to other off-chip inductors from the literature.

| No. | Parameters | Photodefined polymer well | Trenched silicon [14] | Glass [34] | Via-based inductor in glass [34] | Molding material [37] | Polymer well [120] |
|---|---|---|---|---|---|---|---|
| 1 | Images |  |  |  |  |  |  |
| 2 | **Inductor type** | 1.5 turn spiral | 1 turn spiral | 2.5 and 3.5 turn hexagonal | 4 turn embedded helical | In the post-passivation interconnects | 1.5 turn spiral |
| 3 | **Inductor dimensions** | 8-12 $\mu$m thick traces with 55-65 $\mu$m width | 20 $\mu$m thick traces with 50 $\mu$m width | 8 $\mu$m thick traces with 20 $\mu$m width | 8 $\mu$m thick traces with vias at 80 $\mu$m pitch | Not available | 30 $\mu$m wide traces |
| 4 | **Substrate underneath** | SU-8 | Dielectric covered trenches in silicon | Glass | Glass | Under molding material | DuPont PerMX polymer |
| 5 | **Measurement method** | 1-port | 1-port | 2-port | 2-port | Not available | 2-port |
| 6 | $Q_{peak}$ | 55 at 6.75 GHz | >50 from 5-10 GHz | 37 near 3 GHz | 69 | 42 near 5 GHz | 37.8 at 8.6 GHz |
| 7 | **Inductance at** $f_{Q_{peak}}$ | 1.14 nH | 0.8 nH | 2.3 nH | 2.3 nH | 3.3 nH | 1.61 nH |
| 8 | **Ease of fabrication** | High | High | High | Moderate | High | Moderate |

# CHAPTER VI

# SUMMARY AND FUTURE WORK

Key research contributions are first summarized followed by potential future activities.

## *6.1 Summary*

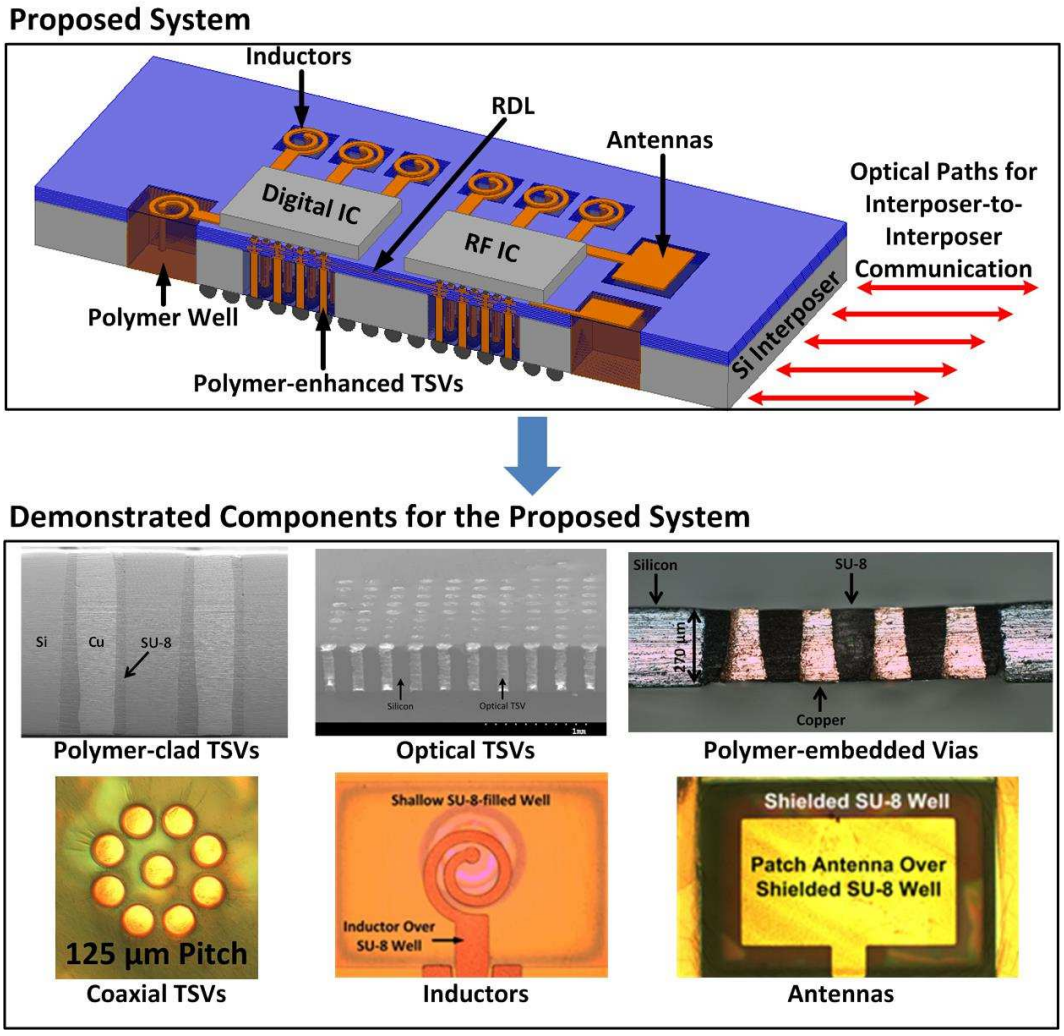



Figure 78: Proposed RF/mixed-signal large-scale interposer-based system with the key components demonstrated in this research for the system.

Figure 78 shows the key components demonstrated in this research for a polymer-enhanced photodefined silicon interposer. These components are described as follows:

### 6.1.1 Polymer-enhanced TSVs

To attain enhanced electrical performance, novel photodefined polymer-enhanced TSVs are fabricated and characterized, including (a) polymer-clad TSVs with copper vias surrounded by a thick polymer liner (for TSV stress reduction in addition to capacitance and loss reduction) and optical TSVs in parallel for interposer-to-interposer long-distance communication; (b) low-loss polymer-embedded vias with copper vias embedded within polymer wells in silicon; and (c) a coaxial configuration of the polymer-embedded vias with a wideband controlled impedance and reduced coupling.

DC resistance measurements are demonstrated for the polymer-clad TSVs and polymer embedded vias. For the polymer-clad TSVs, synchrotron XRD measurements are demonstrated showing a 30 % reduction in the first principal strain compared to the TSVs with silicon dioxide liner. Moreover, for the polymer-embedded vias, RF measurements, de-embedding and $GC$ extraction are demonstrated up to 30 GHz along with TSV-link measurements in the D-band, showing a significant electrical performance enhancement using the polymer-embedded vias. Additionally, eye diagrams with improved eye opening and timing jitters for the polymer-embedded vias are demonstrated up to 10 Gbps. Lastly, for the coaxial vias, single-port measurements are demonstrated to extract their impedance and coupling measurements are demonstrated to show a reduction in coupling using the coaxial configuration.

### 6.1.2 Polymer-enhanced Inductors and Antennas

To build compact mixed-signal systems, high-performance inductors and antennas are demonstrated using the photodefined polymer-enhanced silicon interposer technology. Polymer-enhanced W-band patch antennas are demonstrated showing a

13.35 GHz 10-dB return loss bandwidth at the center frequency of 100 GHz. Moreover, polymer-enhanced inductors are demonstrated with a peak Q-factor of 55 at 6.75 GHz and a 1.14 nH inductance at $f_{Q_{peak}}$ with a self-resonance frequency at 21 GHz.

## *6.2 Future Work*

The development of the photodefined polymer-enhanced silicon interposer technology with high-performance components such as polymer-clad TSVs, optical TSVs, polymer-embedded vias, coax vias, inductors and antennas opens doors to many research and development opportunities. These include further development of these components to improve their electrical performance and thermomechanical reliability, and further exploration for system-level development with heterogeneous ICs. This future work is summarized in Figure 79 and described as follows:

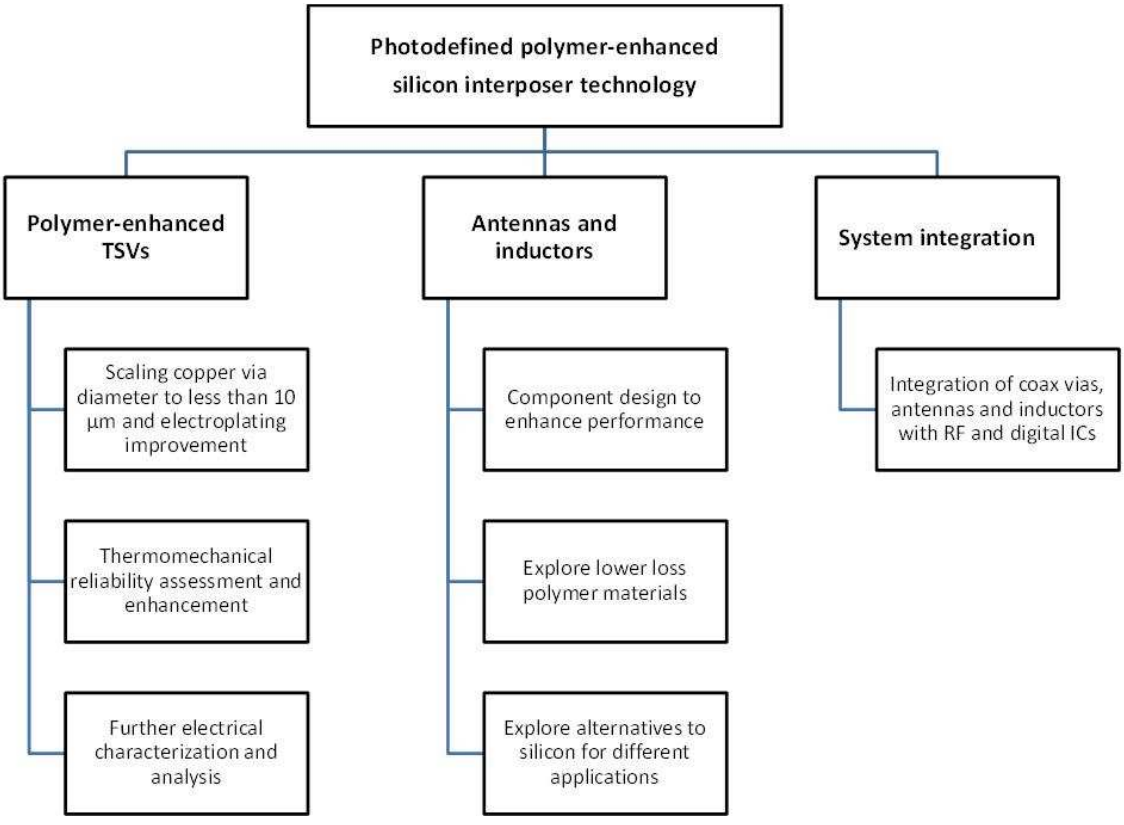



Figure 79: Summary of the proposed future work.

### 6.2.1 Scaling Polymer-enhanced Via Diameter and Electroplating Improvements

Industrial demonstrations for silicon interposers include 10 $\mu$m diameter and 100 $\mu$m tall TSVs [25]. In this research, polymer-enhanced TSVs are shown for thick (approximately 270 $\mu$m and greater) silicon interposers with larger via diameters. The scalability of the TSVs is demonstrated by reducing their diameter and pitch from 100 $\mu$m and 250 $\mu$m to 65 $\mu$m and 95 $\mu$m pitch, respectively. Further diameter scaling could help to increase TSV density. Moreover, the polymer-enhanced coaxial via configuration provides low-loss TSVs with reduced coupling when the TSV densities increase.

To attain further scaling, h-line (405 nm) exposure could be used. The h-line exposure has been shown in the literature to attain very high aspect-ratio SU-8 pillars since the absorbance of the h-line in SU-8 is low compared to the i-line (365 nm) [41]. Moreover, the use of a material with a refractive index similar to SU-8 (for example, glycerol) between a mask and a substrate with SU-8 during exposure could improve photolithography by significantly reducing the impact of SU-8 surface non-uniformity [41].

Additionally, the implementation of the mesh-less process (Section 2.5) could help extend the fabrication of polymer-clad TSVs to large-scale wafers. Moreover, the implementation of superfill copper electroplating instead of the mesh-based bottom-up electroplating could also be used to explore various adhesion layers between the copper and SU-8, thereby making the polymer-enhanced TSV process more robust.

### 6.2.2 Further Electrical Characterization and Analysis of TSVs

The *RLGC* extraction of the polymer-embedded vias in the D-band would help better understand their loss mechanism and to improve future designs. Moreover, measurements of polymer-embedded vias for higher data rates would increase understanding of their operation with high-speed transceivers.

### 6.2.3 Polymer-enhanced Antennas and Inductors

For the polymer-enhanced antennas and inductors, further electrical design is needed to improve their performance. Moreover, low-loss polymer materials such as BCB could be explored to improve their performance. In addition to silicon platform, the photodefined polymer-enhanced technology could be explored for low-cost substrates for applications such as low-cost sensor networks. Lastly, radiation pattern measurements for the polymer-enhanced antennas would assist better understand their performance.

### 6.2.4 Exploration of Suspended SU-8 Substrates

Using the knowledge from the polymer-embedded via technology, suspended-SU-8 wells could be attained with the help of deep-UV exposure.

Transmission lines fabricated over silicon have high conductivity-dependent losses. Polymer wells help attain horizontal metallization with lower loss compared to the transmission lines (like coplanar waveguides) built over a thin dielectric above silicon. Moreover, the polymer wells help attain high-performance inductors and antennas as described in the previous chapter. However, the losses of transmission lines and the performance of passives over polymer wells depend on the dielectric losses of the polymer material. To address these challenges, suspended dielectric/polymer wells are investigated. In the literature, the fabrication of suspended dielectric layers in silicon substrates is shown using the etching of silicon after deposition of a dielectric layer [123]. Moreover, suspended SU-8 layers have been shown in the literature using either reduced exposure dose for thick layers or using deep-UV exposure [118, 124]. The deep-UV exposure with a wavelength of less than 250 nm has very high surface absorbance with SU-8, leaving a desired thickness of SU-8 unexposed and yielding suspended SU-8 layers.

This research shows suspended polymer wells with controlled thicknesses of the

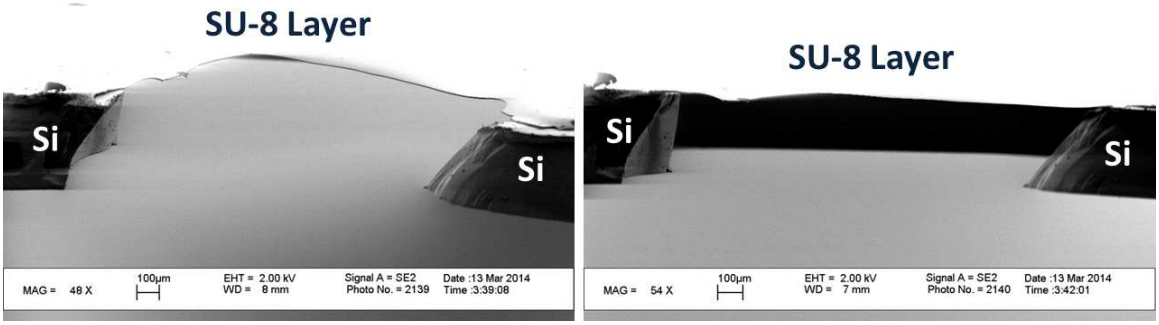



Figure 80: Fabricated suspended SU-8 wells.

SU-8 layers using the dose control for deep UV exposure, as shown in Figure 80. Suspended SU-8 wells with thickness controlled from 3 $\mu$m to 15 $\mu$m have been attained by increasing the exposure dose. Due to the presence of wavelength components below 248 nm for the mask aligner used, a significantly higher dosage was needed for a desired thicknesses compared to those in the literature [124]. This could be addressed by using high-pass filters with cut-off below approximately close to 250 nm.

### 6.2.5 Thermomechanical Reliability Assessment and Enhancement

Reliability is a key requirement for the demonstrated technologies to enable their implementation in the real-life products. To assess the reliability of these technologies, thermal cycle testing using JEDEC standards is necessary [125]. Moreover, an exploration of photodefinable polymer materials in order to improve thermomechanical reliability is also desired. A few potential photodefinable materials for the proposed technologies include BCB, TMMR S2000, and photodefinable polyimide [126–128].

### 6.2.6 System Integration

Finally, integration of the demonstrated photodefined polymer-enhanced silicon interposer technology featuring novel TSVs and passives with RF and digital ICs could help in the development of systems for various applications using mm-wave

frequencies.

## *6.3 Research Conclusion*

Thus, novel photodefined polymer-enhanced interconnect and passive technologies were demonstrated in this research. Their electrical design, cleanroom fabrication, and RF, time-domain and thermomechanical measurements were demonstrated. In the future, the demonstrated technologies when implemented at system level could help enable a large number of mixed-signal applications.

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# VITA

Paragkumar Thadesar was born in 1987 in Gujarat, India. He received the Bachelors of Engineering (B.E.) degree in Electronics and Communication (E.C.) engineering from V.V.P. Engineering College, Rajkot in 2009 with gold medal in the final year and university 1st rank in the 3rd, 7th and 8th semesters for the E.C. branch. For his final year project in B.E., he received 1st position in a software project competition at Prevoyance 2009 in Nirma University, India. He continued his interest in electronics by pursuing a Masters of Science degree from 2009-2011 at the Georgia Institute of Technology with focus on analog and digital circuit design.

In the May of 2010, he joined Dr. Muhannad Bakir's research group to pursue a Ph.D. degree in microelectronics with focus on experimental research for advanced interconnect technologies. Since then he has worked in his Ph.D. over novel technology development and characterization for stacked-silicon systems.

For his research, he has received the Best Student Paper awards at the IEEE Global Interposer Technology Workshop 2011 and 2012, 2nd Best Oral Presentation award at the Georgia Tech Graduate Technical Symposium 2013, 3rd Place Microelectronics Foundation Prize at the IMAPS Device Packaging 2013, Best in Session award at SRC TECHCON 2013, and Outstanding Interactive Presentation Paper award at the IEEE ECTC conference 2013. Moreover, he was awarded the IBM Ph.D. fellowship for the 2014-2015 academic year, greatly assisting his journey towards completing his Ph.D.