MANAGING SIGNAL AND POWER INTEGRITY USING POWER TRANSMISSION LINES AND ALTERNATE SIGNALING SCHEMES

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Satyanarayana Telikepalli

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MANAGING SIGNAL AND POWER INTEGRITY USING POWER TRANSMISSION LINES AND ALTERNATIVE SIGNALING SCHEMES

Approved by:

Dr. Madhavan Swaminathan, Advisor
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. Arijit Raychowdhury
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. David Keezer
School of Electrical & Computer Engineering
Georgia Institute of Technology

Dr. Suresh Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical & Computer Engineering
Georgia Institute of Technology

Date Approved: December 05, 2014

Dedicated to my parents and grandparents

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LIST OF SYMBOLS AND ABBREVIATIONS

IC	Integrated Circuit
SSN	Simultaneous Switching Noise
PDN	Power Delivery Network
I/O	Input/Output
PTL	Power Transmission Line
CC-PTL	Constant-Current Power Transmission Line
PB-PTL	Pseudo-Balanced Power Transmission Line
CC-PTL	Constant Voltage Power Transmission Line
RPD	Return Path Discontinuity
PCB	Printed Circuit Board
PRBS	Pseudo-Random Binary Sequence
VRM	Voltage Regulator Module
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
ATE	Automatic Test Equipment
TSV	Through Silicon Via
BGA	Ball Gate Array

CHAPTER 1: INTRODUCTION

1.1 Background and Motivation

As transistor technologies continue to improve, researchers and integrated circuit (IC) manufacturers are able to push the operating frequencies of ICs higher than ever before. These advancements allow for very high bandwidth and correspondingly high data rates. From Figure 1, data rates in commercially available products have approached nearly 32 GB/s (uni-directional) in 2014 [1-4].

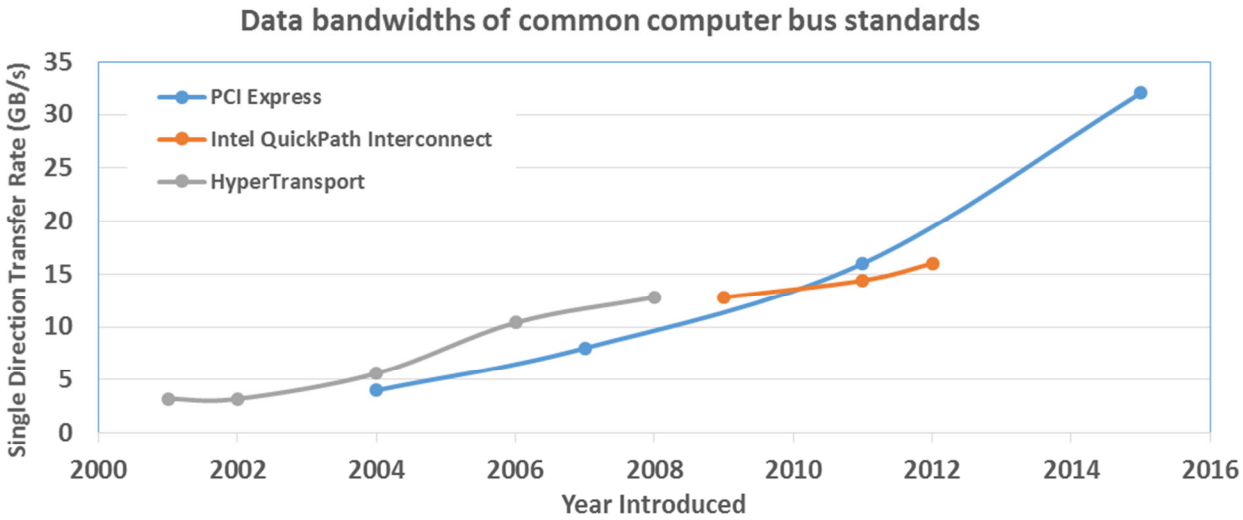


Figure 1 Increasing data rates in various commercially available I/O bus standards [1-4]

However, this trend means signal and power integrity engineers are faced with significant challenges in the form of limited channel bandwidth, inter-symbol interference, crosstalk, impedance mismatches, and simultaneous switching noise (SSN), among other issues. While these are all significant obstacles that have garnered much research interest, this dissertation will primarily focus on SSN. Switching noise can be attributed to two key sources. The IC's bond wires, lead frame, on-die power/ground grid, as well as the board-level power delivery network

contribute to the parasitic inductance and resistance [5]. Fast current transients flowing across these parasitic inductances induce voltage fluctuations on the PDN. SSN is also due to the physical discontinuities that are encountered by forward and backward flowing currents on the signal and reference planes, such as via transitions, plane apertures, split planes, etc. [5]. Supply noise, if not properly managed, can severely affect the voltage and timing margins in high speed digital systems.

In order to mitigate the effects of switching noise, the standard practice is to design the power distribution network (PDN) to have the lowest impedance possible. However, this can be difficult to achieve as power and ground planes exhibit cavity resonances at certain frequencies. At resonance frequencies, the plane cavities have local maximum impedances. The impedance spikes can be removed by placing decoupling capacitors between the power and ground rails with the corresponding resonance frequency. This method, however, presents several disadvantages. First, the capacitor itself adds to the loop-inductance to the overall system due to its lead inductance and the cross-sectional loop area formed between the capacitor body and the circuit. In addition, adding decoupling capacitors does not always help the design meet the desired target impedance target in ICs with high inductances, as shown in [6, 7]. Furthermore, decoupling capacitors take up valuable real estate on ICs, which can be used for other purposes [8].

In conventional power distribution network designs used today, solid power and ground planes are used for power delivery. However, the power planes cause return path discontinuities (RPDs), which induce power supply noise and coupling between the signal distribution network and power delivery network [5]. Previous work has shown that simultaneous switching noise can be greatly reduced by utilizing current steering and power transmission lines (PTLs) to connect the voltage supply directly to the digital circuitry [9-11]. The PTL-based PDN allows both power and signal transmission lines to be referenced to the same ground plane. As a result, a continuous current loop is established, which therefore removes return path discontinuity (RPD) effects [11, 12].

1.2 Power Delivery Network & Simultaneous Switching Noise

The power distribution network (PDN) is used to provide clean, stable power for the various ICs in the system. In most systems, the PDN ideally serves to provide a constant voltage source while allowing the current to vary as required by the load circuitry. In many high speed digital systems, power and ground planes are used as a low-impedance supply path. Unfortunately, the design of a PDN is difficult due to the presence of parasitic inductances from the printed circuit board, package inductance, bond wires, and solder bumps, as shown in Figure 2.

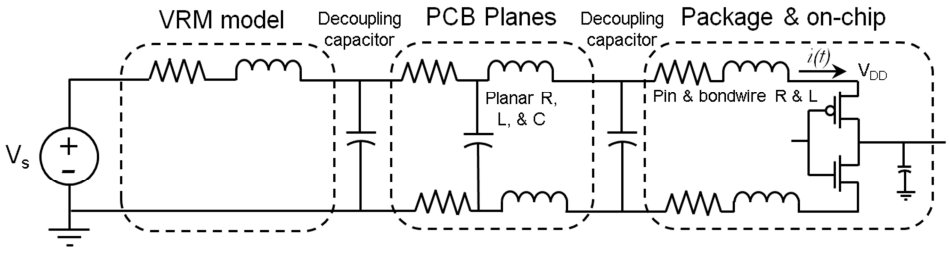


Figure 2 Simplified circuit schematic of a standard power distribution network

The various parasitic inductances in the PDN all contribute to the occurrence of noise on the supply rail of the digital ICs. The time-variant voltage drop across the PDN can be described by Equation (1).

$$V_{SSN}(t) = N \cdot L_{PDN} \frac{di(t)}{dt} \quad (1)$$

In Equation (1), L_{PDN} is the total equivalent inductance of the PDN (which is frequency dependent), *i(t)* is the current transient attributed to the switching activity of the digital device, and N is the number of devices that are switching simultaneously.

In addition to the interconnect inductance, parasitic inductance can also be generated by return path discontinuities. Whenever a current flows on the PDN, an equal current must be flowing in the opposite direction on the signal's reference plane so as to create a closed current loop. However, when the forward and return current encounter a layer transition or plane discontinuity, this presents some undesirable effects, as summarized in Figure 3.

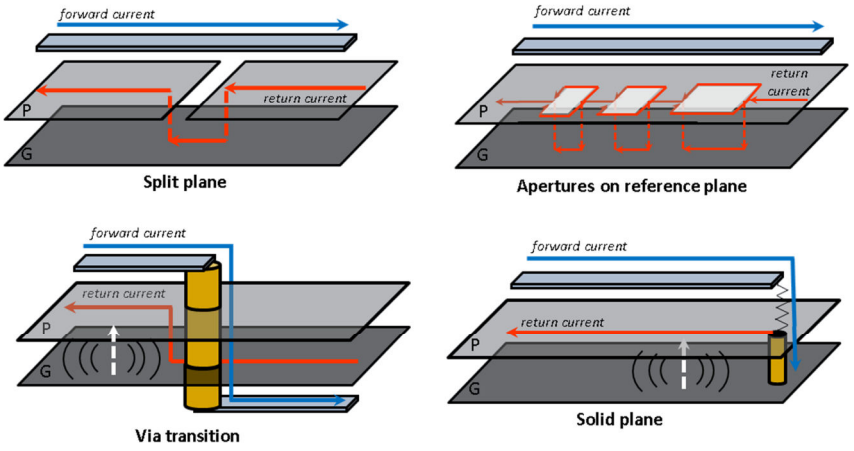


Figure 3 Several examples showing the effect of return path discontinuities [12]

When a signal current encounters a split plane, aperture on the reference plane, via transition, or insufficient grounding, there is a mismatch between the forward and return currents. It is known that inductance generated by a current loop is proportional to the area encircled by the current loop, as shown by Equation (2).

$$L_{ij} = \frac{\psi_{ij}}{I_j} = \frac{\iint B_{ij} \cdot ds_{ij}}{I_j} \qquad (2)$$

As can be seen from Figure 3, these return path discontinuities tend to increase the area of the loop formed by the forward and return currents, which in turn cause the self-inductance to increase as well. When the return current transitions between planes that are at different DC potentials, the circuit compensates by injecting a displacement current that flows vertically in the plane cavity [12]. If sufficient grounding vias are not present, this displacement current can couple energy into adjacent planes and nearby vias, thereby generating crosstalk and producing unwanted higher-order waveguide modes [13].

If the device under test is a simple single inverter circuit, with the input being the square wave shown in Figure 4a, then the voltage "seen" by the inverter at its drain would be as shown in Figure 4b.

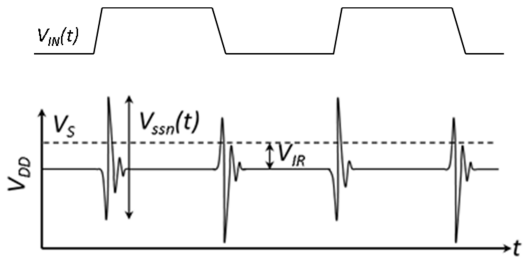


Figure 4 (top) Input voltage (bottom) V_{DD} node voltage with ohmic drop and switching noise

During the rising and falling edges, a current transient therefore causes large voltage fluctuation in the supply rail.

1.3 Current Methods for Power Distribution

1.3.1 Target Impedance

The conventional method for mitigating the issues discussed in the previous section is to place decoupling capacitors between the voltage and ground planes. Decoupling capacitors reduce the high-frequency impedance between the voltage and ground planes such that any large current transients do not translate to large voltage fluctuations on the PDN. In addition, decoupling capacitors serve to store and provide additional electrical charge to the load circuitry when the power supply is unable to react fast enough. It has been shown in [14] that carefully selecting the location of the capacitor placement can directly affect noise performance. The capacitor location determines how fast the electric charge can be delivered to the IC when the supply voltage drops below the nominal value. Ideally, one should place sufficiently large decoupling capacitors at RPD locations for optimal performance.

The concept of target impedance is a frequency domain design methodology that is commonly used in the design of a PDN. The target impedance, described by Equation (3), defines the maximum PDN impedance based on the maximum allowed supply noise.

$$Z_{\mathrm{Target}} = \frac{V_{\mathrm{DD}} \cdot \%\mathrm{ripple}_{\mathrm{max}}}{I_{\mathrm{DD}}} \tag{3}$$

In Equation (3), $\%ripple_{max}$ is the maximum percentage of voltage ripple that is allowed on the VDD rail. The variable ΔI_{DD} is the maximum current transient that is expected to be drawn by the supply.

1.3.2 Decoupling Capacitors

Once the maximum tolerable supply ripple voltage and target impedance is chosen, decoupling capacitors can be placed strategically on the PCB or on-chip to lower the PDN impedance to meet the target impedance. Many optimization algorithms and design techniques have been presented to determine the optimal value and placement location of decoupling capacitors, such as that shown in [15]. However, decoupling capacitors exhibit non-ideal behavior, as shown in the circuit model of a non-ideal capacitor in Figure 5.

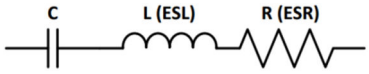


Figure 5 Circuit model of a decoupling capacitor with non-ideal components

Capacitors have an equivalent series inductance (ESL) and equivalent series resistance (ESR). From this model, the impedance of a non-ideal decoupling capacitor can be described by Equation (4).

$$Z_{Decap} = \frac{1}{j\omega C} + j\omega L_{ESL} + R_{ESR} \tag{4}$$

The consequence of Equation (4) is that decoupling capacitors are only effective in reducing the PDN impedance for frequencies below the capacitor's resonance frequency, which is the frequency at which the capacitor exhibits the lowest impedance. At higher frequencies, the decoupling capacitor can actually exacerbate the problem by increasing the PDN impedance. For example, Figure 6 shows the insertion loss of a 1000pF ceramic capacitor. Above approximately 200MHz, the capacitor's insertion loss, and therefore impedance, begins to increase and behaves

like an inductor. Above the capacitor's resonance frequency, its ESL dominates the impedance profile.

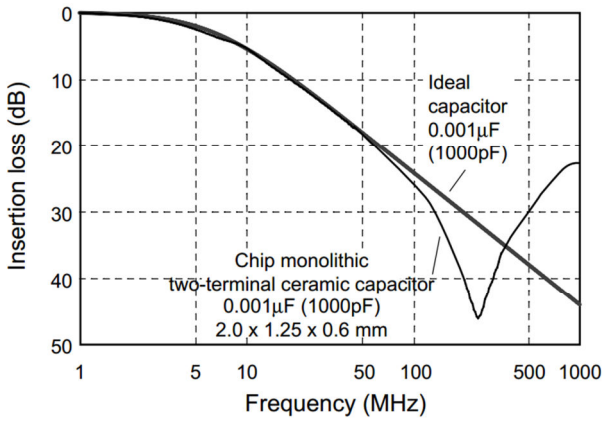


Figure 6 Insertion loss of ideal vs. non-ideal 1000pF capacitor [16]

An example of using decoupling capacitors to achieve the target impedance is shown below in Figure 7.

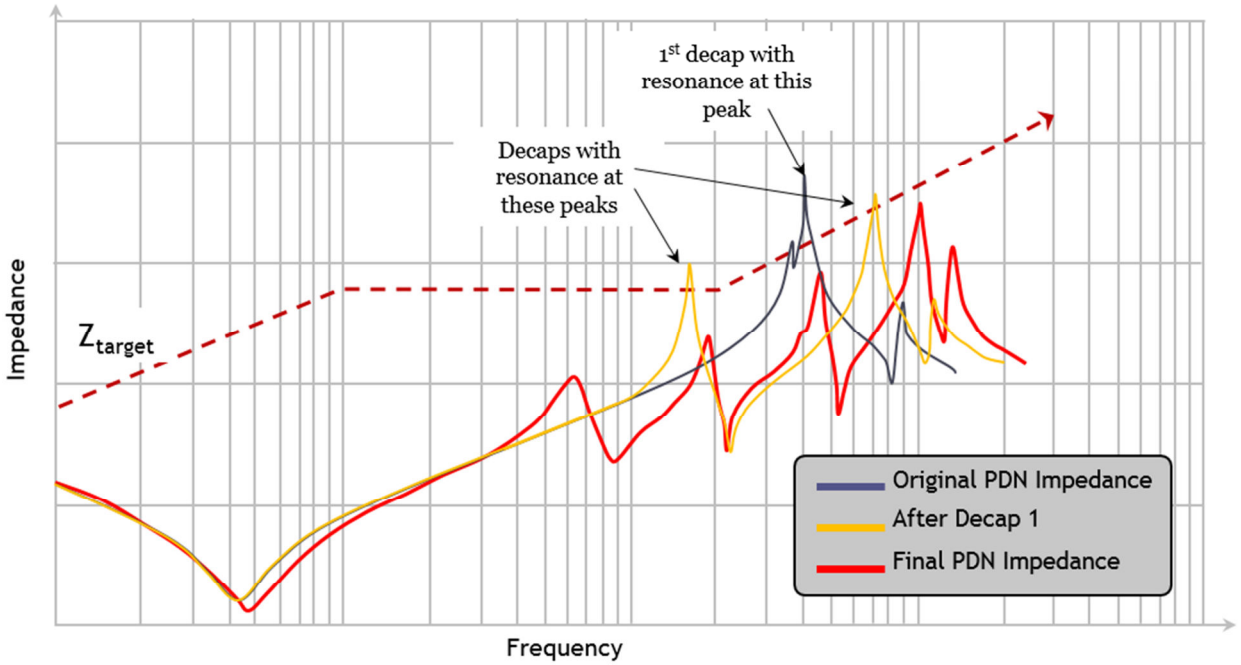


Figure 7 Example of decoupling capacitor placement

The impedance profile of a power/ground plane pair is shown in Figure 7. Since there is an impedance peak that exceeds the target frequency, it is necessary to place a decoupling capacitor with a resonance frequency corresponding to the impedance peak. However, after placing the decoupling capacitor, this causes two other impedance peaks that exceed the target frequency. Decoupling capacitors with resonance frequencies corresponding to these peaks must be placed as well. Consequently, the final PDN impedance after all decoupling capacitors is shown as the red curve and meets the target impedance specification for all frequencies of interest.

1.4 Alternative Methods for Power Distribution

1.4.1 Power Transmission Line

New I/O signaling schemes have been proposed to specifically address the SSN problem. These solutions are based on the power transmission line (PTL) concept [9], in which a transmission line is used in place of a power plane to transfer power from the voltage regulator module (VRM) to an IC on the PCB. The PTL-based PDN allows both power and signal transmission lines to be referenced to the same ground plane so that a continuous current loop is established, thereby lessening the effects of RPDs [11]. This configuration is shown in Figure 8.

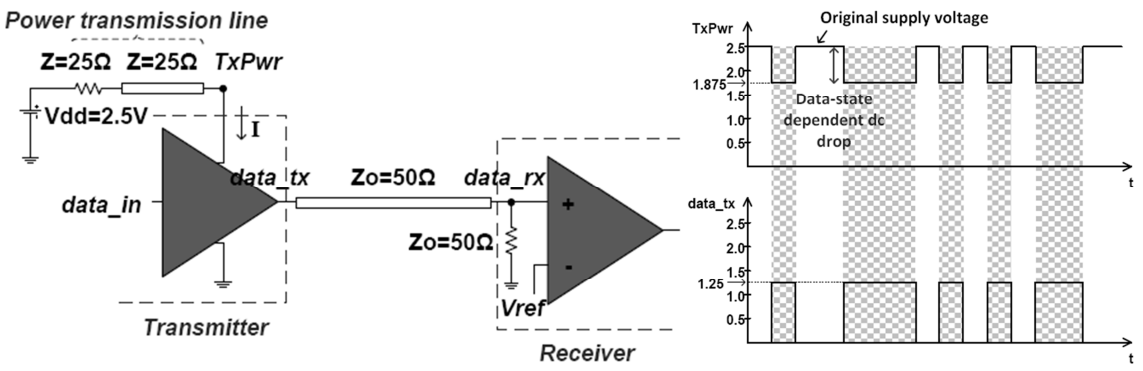


Figure 8 Single-ended signaling using a PTL (a) schematic (b) waveform showing data-dependent voltage drop on driver's supply pin[11]

In Figure 8, R_S is the PTL terminating resistor. The resistor RS, placed at the far-end of the PTL, serves to prevent any reflections that can propagate across the line and back into the driver's power pin. In addition, if a high quality PCB substrate with controlled trace impedances and low tolerance passive components are used, the matched termination can also remove the transmission line resonances at higher frequencies, as shown in Figure 9.

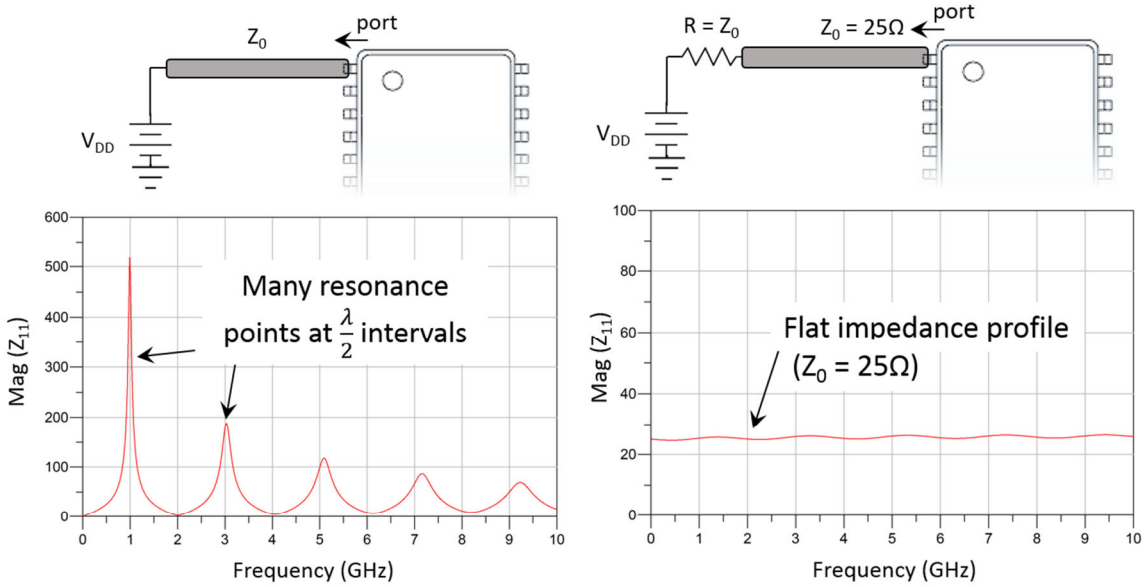


Figure 9 Comparision of PTL's self impedance, Z11, (left) without termination, (right) with termination

The left figure in Figure 9 shows the Z_{11} (self-impedance) for an unterminated transmission line. The line exhibits resonances at $\lambda/2$ intervals. By terminating the line with a resistance equal to the characteristic impedance of the transmission line (right figure in Figure 9), the resonances are eliminated, resulting in a flat impedance profile.

While using PTLs helps solve the RPD issue, it presents additional difficulties. One such issue that arises with the PTL-based signaling scheme is the dynamic DC drop due to the terminating resistance [11]. The state of the output data dictates the amount of current the I/O driver draws from the PDN. In the case of a voltage-mode driver, the high state of the output data induces current to flow from the PDN through the signal transmission line, while the low state of the output data causes very little current flow. Thus, the DC drop that occurs on the PDN is data-dependent [11]. This effect is shown in Figure 8 and Figure 10, with the PTL supporting multiple drivers.

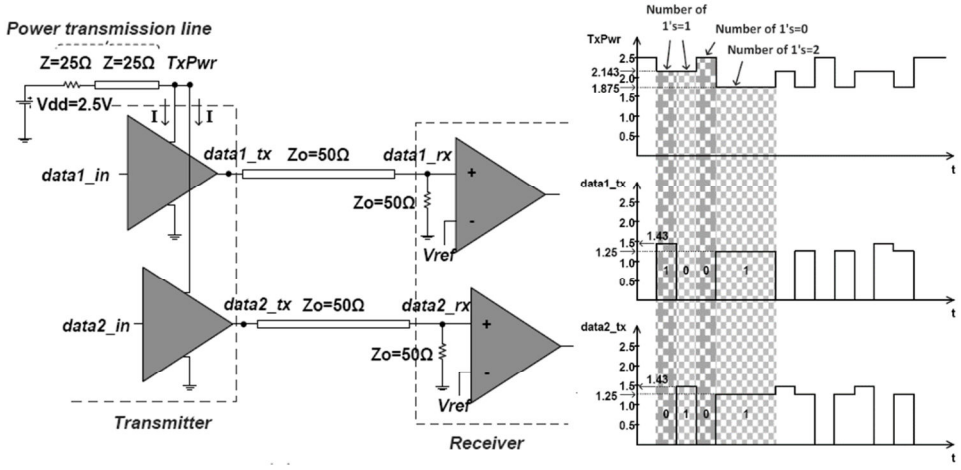


Figure 10 PTL powering two drivers (a) schematic (b) waveform showing data-dependent voltage drop on driver's supply pin [11]

In order to prevent this data dependent DC drop issue, the PTL scheme must be modified. The following sections discuss several variations of the power transmission line scheme that resolve the data-dependent DC drop issue, each with its own advantages and disadvantages.

1.4.2 Constant Current Power Transmission Line (CC-PTL)

The constant-current power transmission line (CC-PTL) scheme is shown in Figure 11. The CC-PTL scheme resolves the dynamic DC-drop issue described in the previous section. The varying DC drop on the driver's supply node shown in Figure 8 and Figure 10 is due to current flowing through the PTL only during the high states of the output data. To maintain a constant DC voltage level, a current path is required during the low state of the data as well. In the CC-PTL scheme, an additional current path from power to ground is included using a data pattern detector and "dummy path" [10]. This scheme is illustrated in Figure 11. The data pattern detector detects the state of the input data and then determines whether to connect or disconnect the dummy path to the PTL. The dummy path is resistive, and its impedance is matched with that of the signal path so as to induce the same amount of current during both the low and high states.

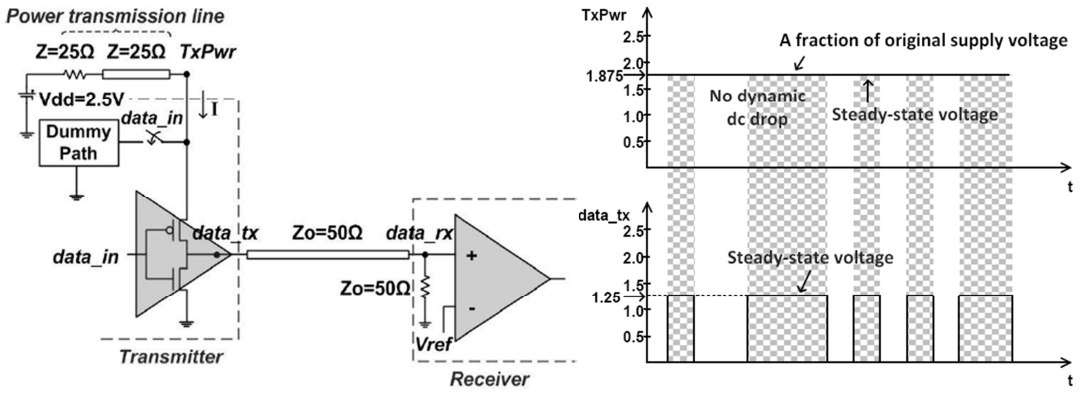


Figure 11 Single-ended signaling using CC-PTL (a) schematic with dummy path (b) waveform with constant supply voltage [11]

Because this scheme consumes constant current, and is independent of the data pattern, multiple drivers can be connected to the same PTL, unlike the original PTL scheme. This design's disadvantage, however, is that to operate a single driver, the current consumed is double that of a

single driver in a conventional PDN design. However, the power consumption would be similar to that of differential signaling.

1.4.3 Pseudo-Balanced Power Transmission Line (PB-PTL)

In order to address the issue of increased power consumption of the CC-PTL, the pseudo-balanced power transmission line (PB-PTL) scheme was presented in [17]. For this scheme, the data is encoded prior to transmission. Each transmitted sequence, or symbol, has extra bits in order to keep the number of high states that are transmitted constant. The criterion for encoding is described by Equations (5) and (6), where N is the length of the original data sequence and M is the length of the encoded data word [18].

$$\frac{M!}{\left(\frac{M}{2}\right)!} + \frac{M!}{\left(\frac{M}{2}-1\right)!} \geq 2^N, \textit{ if M is even} \tag{5}$$

$$\frac{M!}{\left(\frac{M-1}{2}\right)!} + \frac{M!}{\left(\frac{M-1}{2}-1\right)!} \geq 2^N, \textit{ if M is odd} \tag{6}$$

For example, when the original data word consists of 4 bits (N=4), then by using the pseudo-balanced coding scheme, Equation (6) is satisfied with M=5. Thus, the encoded string becomes 5-bits long. The counts of 1s and 0s are either (2,3) or (3,2). By adding an extra balancing bit that is set to 1 when the count becomes (2,3), then the count will always be (3,3). Consequently, by keeping the number of high states transmitted during each cycle constant, the $di(t)/dt$ experienced in the PDN is minimized, and results in significantly reduced SSN [18].

1.5 Dissertation

In this dissertation, a new signaling scheme known as Constant Voltage Power Transmission Line (CV-PTL) is presented to supply power to a digital I/O circuit. This signaling scheme provides power through a transmission line in place of a power plane while dynamically changing the impedance of the power delivery network to keep a constant voltage at the power pin of the IC. Consequently, this reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. Through theory, simulation, and measurements, we show that this new method can be used to reduce jitter and eye height with the proposed PDN methodology. In addition, the signaling scheme was extended to vertically-stacked 3D integrated circuits (3D ICs) [19]. It is known that power supply noise worsens as one goes higher up in the stack of dies due to increased interconnect inductance. However, by utilizing the CV-PTL concept in the PDN design of a 3-layer 3DIC system, the circuit showed considerable improvement in power supply noise and peak-to-peak jitter as compared to the conventional design approach.

In addition to signal and power integrity of these signaling schemes, the noise coupling between digital and RF components is also investigated. A simple design for mitigating the coupling of power supply noise in mixed-signal electronics is presented. Currently used methods, such as electromagnetic bandgap structures have been shown to exhibit excellent noise isolation characteristics [20, 21], and are a popular area of research in this area. However, these structures can pose difficulties for signal integrity. The proposed method extends the previous power transmission line work to address both the power supply noise generation and isolation. Test vehicles using these proposed methods, as well as using an EBG structure were fabricated and tested with regards to power supply noise, jitter, and noise isolation. The proposed methods show significant improvements in almost all performance metrics as compared to EBG.

Finally, this dissertation discusses the effect of implementing a power transmission line in a power distribution network composed of a switching regulator and a voltage regulator module. The DC conductor losses of the PTL can not only affect power efficiency of the entire system, but can also affect the proper operation of the linear regulator module when supporting large currents. Consequently, recommendations are made on the design of the PTL to ensure proper operation and efficiency.

1.5.1 Contributions

The major contributions of the dissertation are the following:

1. A new power delivery method called Constant Voltage Power Transmission Line (CV-PTL) is introduced and investigated that can significantly reduce the occurrence of return path discontinues. It is shown in simulations and lab measurements that this signaling scheme performs much better in terms of power supply noise and jitter than that of conventional power and ground planes.
2. The CV-PTL concept was extended to 3D ICs in simulations. It has been demonstrated through simulation that power supply noise worsens as one goes higher up in the stack of dies. However, by utilizing the CV-PTL concept in the PDN design of a 3-layer 3DIC system, the circuit showed considerable improvement in power supply noise and p-p jitter as compared to the conventional design approach.
3. A custom IC was designed with an LDO powering 6 parallel-connected I/O buffers using a 0.18μm CMOS process based on the CV-PTL concept. This solution would allow the circuit to operate at much higher data rates than the CV-PTL test vehicle using off-the-shelf parts.
4. A simple method for power delivery design for mitigating the coupling of power supply noise in mixed-signal electronics. The method, which uses a bandstop filter embedded in

the power transmission line can isolate the amount of coupled noise between the digital and RF supply voltage pins. Test vehicles using these proposed methods were fabricated and tested and showed considerable improvement with regards to power supply noise, jitter, and noise isolation compared to an electromagnetic bandgap (EBG) structure.

5. An analysis of the power efficiency of a standard power distribution network with a switching and linear regulator connected by a PTL is presented. Simulations are performed on the DC loss across the PTL and its effect on the total system efficiency.

1.5.2 Organization of the Thesis

This dissertation consists of eight chapters. Chapter 2 introduces a new power delivery network technique known as constant-voltage power transmission line (CV-PTL). Details on the fabricated test vehicle are shown along with the corresponding lab measurements. In Chapter 3, the CV-PTL concept is extended to 3D integrated circuits. Simulations were performed and the results are shown and compared to a corresponding conventional power delivery network design. In Chapter 4, the design of an integrated low dropout voltage regulator is discussed. The design equations, circuit schematics, simulation results, and IC layouts are presented. In Chapter 5, a new noise isolation technique that is based on the power transmission line is presented. Circuit simulations and test vehicle designs are shown. Power supply noise, eye diagrams, jitter, and noise isolation lab measurements are shown between the two PTL-based methods and an electromagnetic band gap structure. In Chapter 6, the power efficiency is discussed in a power delivery network consisting of a switching regulator and linear regulator connected through a PTL. Finally, a summary and conclusion of the research work are shown in Chapter 7.

CHAPTER 2: CONSTANT VOLTAGE-POWER TRANSMISSION LINE

2.1 Introduction

Table 1 summarizes the various PTL-based signaling schemes and each method's advantages and disadvantages. The original power transmission concept presented a new PDN design paradigm that is in stark contrast to the conventional low-impedance plane approach. The CC-PTL and PB-PTL improved on the design and both were shown to exhibit characteristics that are beneficial for both power and signal integrity. However, each has its drawbacks in the form of power consumption and extra hardware.

Table 1 Advancements in PTL research

Gen 0: Power Transmission Line	Gen 1: Constant Current PTL (CC-PTL)	Gen 2: Pseudo-Balanced PTL (PB-PTL)	Gen 3: Constant Voltage PTL (CV-PTL)	Gen 4: Integrated Voltage Regulator with PTL
▪ Significant reduction in RPDs and SSN	▪ Significant reduction in RPDs and SSN ▪ Constant V_{DD}	▪ Significant reduction in RPDs and SSN ▪ Constant VDD ▪ Less power consumption than CC-PTL	▪ Significant reduction in RPDs and SSN ▪ Constant V_{DD} ▪ Even lower power consumption	▪ Utilize on-die low-dropout voltage regulator
▪ Data dependent voltage fluctuation on V_{DD}	▪ Power consumption per bit is doubled	▪ Requires extra encoding hardware		

This chapter will introduce the next evolution of the PTL concept called Constant Voltage Power Transmission Line (CV-PTL), which addresses the shortcomings of the previously discussed methods.

2.2 Constant Voltage-Power Transmission Line (CV-PTL) Concept

The constant voltage power transmission line scheme, or CV-PTL, was developed to resolve the DC drop issue as well as lower the power consumption requirements of the CC-PTL and PB-PTL schemes [19, 22]. The configuration for this scheme is shown in Figure 12. For the CV-PTL scheme, depending on the input data, a data pattern detector is used to select a resistor path in the PDN to keep the impedance looking into the input of the PTL, denoted as $Z_{PTL,in}$, constant.

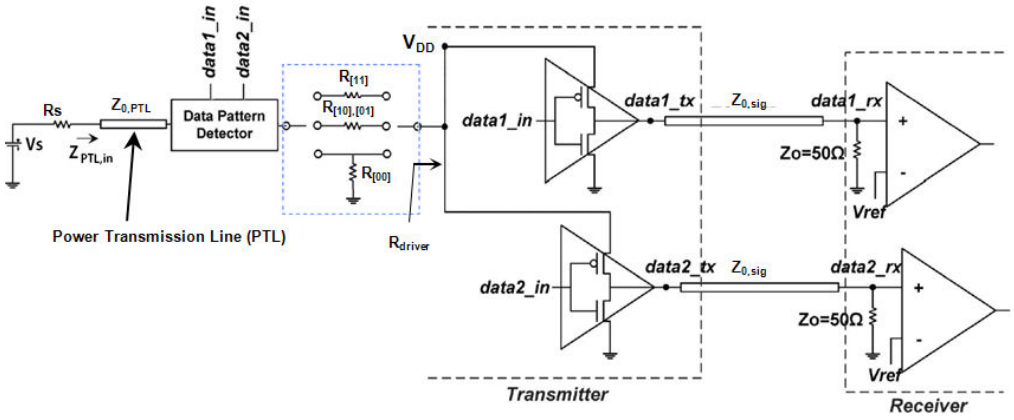


Figure 12 Constant Voltage Power Transmission Line

The resistor values (shown as $R_{[00]}$, $R_{[01],[10]}$, and $R_{[11]}$ in Figure 12) are carefully chosen to keep the power supply voltage seen by the drivers, V_{DD}, at a constant level regardless of driver states. For N drivers, there are a total of 2^N possible data combinations. However, the current that is drawn by the PDN is dictated by the number of drivers that are in a "high" state at any given time. Consequently, for *N* drivers, *N+1* different values of source current can be drawn, so *N+1* different resistor values are required in the PDN.

In order to maintain $Z_{PTL,in}$ constant, the resistor network must be carefully designed. One important parameter is $R_{driver}[k]$, which is the resistance looking into the power supply node of the drivers, and is calculated using Equation (7).

$$R_{driver}[K] = \frac{R_{on} + R_L}{k} \tag{7}$$

The variable k denotes the number of "on" drivers at any given time (and thus, $k = 1,2,\ldots N$). Consequently, one can determine the value of each resistor value for each driver state, as shown below. Consequently, one can easily determine the resistor value for each driver state by treating it as a simple resistor divider network.

$$V_{DD} = V'_{DD} \frac{R_{driver}[k]}{R_{driver}[k] + R_S + R[k]} \tag{8}$$

From the above equation, the resistor values R[k], when solved for, result in the following:

$$R[k] = \frac{1}{V_{DD}} \left(V_S \cdot R_{driver}[k] - V_{DD}(R_{driver}[k] + R_S) \right) \tag{9}$$

(for k = 1,…,N)

When all the drivers are "low", i.e., the output is all zeroes, then we assume that $R_{driver[k]} \approx \infty$. The resistor divider network becomes:

$$V_{DD} = V_S \frac{R[k]}{R[k] + R_S} \tag{10}$$

And the corresponding R[k] value can be determined.

$$R[0] = \frac{1}{V_{DD} - V_S} (-V_{DD} \cdot R_S) \tag{11}$$

The independent variable *k*, is the number of active drivers at a given time, and not the actual bit pattern itself, so the data pattern detector would select the same resistor value when the data pattern is "0101" and "1010". The number of active drivers dictates the amount of current flow, not the actual bit pattern. The quantity R_S is the PTL terminating resistor. The quantity R_{ON} is the on-resistance of the data drivers, V_S is the voltage provided by the power supply, V_{DD} is the desired supply voltage of the drivers, and R_L' is the load resistance as seen by the driver's output pin.

2.3 Test Vehicle

Test vehicles were designed and fabricated to evaluate the effectiveness of the CV-PTL signaling scheme and the design of which will be discussed in this section. The CV-PTL scheme test vehicle will be compared to the conventional power and ground plane PDN method. Both test vehicles were designed to transmit a 4-bit data sequence.

A commercially available 20-pin octal buffer/line driver (MC74ACT540 from On Semiconductor) was used as the device-under test for both test vehicles. The test vehicle utilizing the conventional PDN, designated TV1, has power and ground planes measuring 240mm by 52mm. The other test vehicle, TV2, is implemented with a 25Ω power transmission line and a 25Ω resistor termination.

Table 2 CV-PTL Test Vehicles

Designation	Method
TV1	Conventional power and ground planes
TV2	CV-PTL

A circuit schematic illustrating the CV-PTL test vehicle implementation is shown in Figure 13.

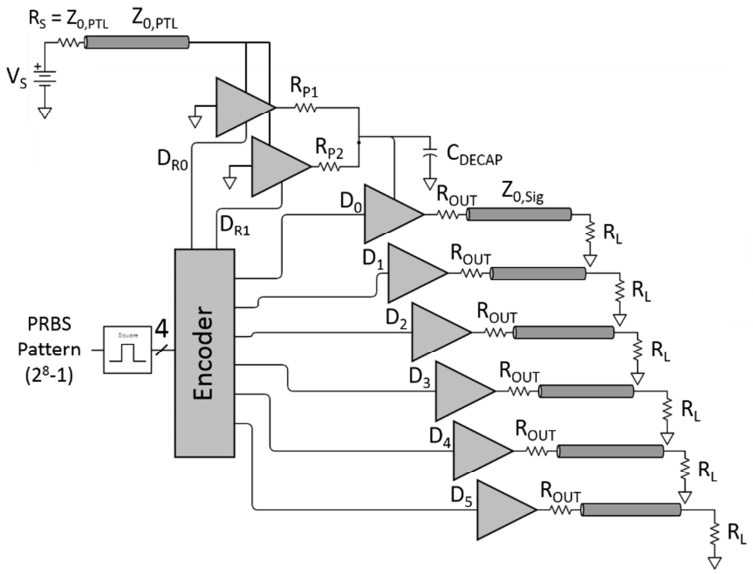


Figure 13 Constant Voltage Power Transmission Line topology as implemented on test vehicle

At the output pin of each driver, a 450Ω series resistor is placed to limit the amount of current that the driver has to supply, as well as the amount of current that can flow into the oscilloscope. Each output connects to an SMA connector using a 205mm long 50Ω microstrip trace, which is terminated with a 50Ω load. In addition, a 0.1μF decoupling capacitor is connected between the power and ground pins of the driver to supply the high frequency charge for both boards. It is important to note that an additional benefit of using the PTL configuration is that a power plane is not used so fewer layers are required.

2.3.1 Bus-inversion encoding

Equations (7)-(11) were used to determine the resistor path values. In order to implement the circuit to transmit 4 data channels, one would require 5 unique resistor values that would have to be toggled on and off according to the data sequence. To simplify implementation, it was chosen to encode the input data by using a bus-inversion encoding scheme. This encoding

scheme, described in [23, 24], requires an extra bit to be transmitted in addition to the 4-bit data sequence. This encoding scheme is described in Figure 14.

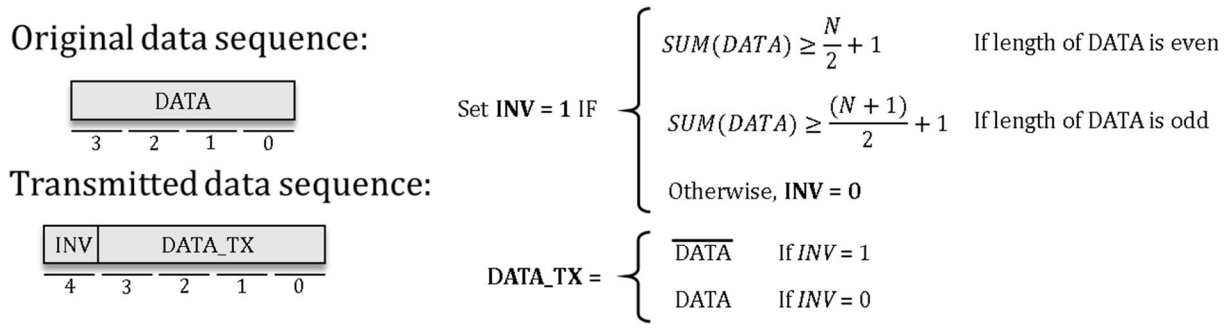
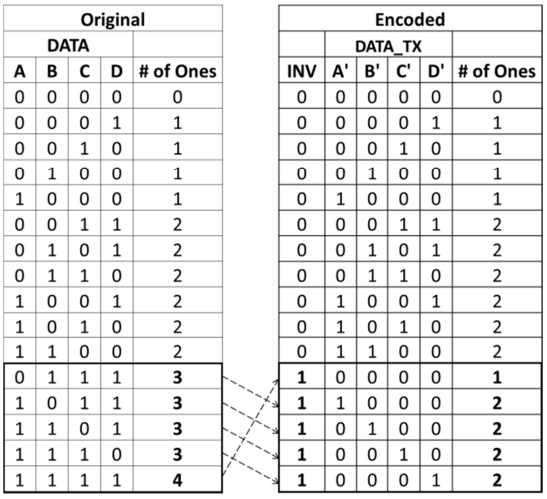


Figure 14 Bus-inversion encoding scheme

This encoding scheme requires an extra "inversion" bit, or INV, to be transmitted along with the data sequence. INV is set to '0' by default. When the number of '1's in the 4-bit data exceeds 3, INV is set to '1' and the data sequence is inverted. For example, when the data sequence to be transmitted is '1011', the actual transmitted sequence is "10100", where the first bit is the inversion bit (INV = 1) and the remaining four bits are the compliment of the original data sequence. With this encoding scheme, instead of requiring 5 resistors in the PDN, we only require 3 because the encoding scheme will only transmit 0, 1, or 2 high states at any given time. Figure 15 shows the truth table for a 4-bit data sequence and the resulting transmitted data sequence after applying bus-inversion encoding.



Original				
DATA				
A	B	C	D	# of Ones
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	0	1	1	2
0	1	0	1	2
0	1	1	0	2
1	0	0	1	2
1	0	1	0	2
1	1	0	0	2
0	1	1	1	**3**
1	0	1	1	**3**
1	1	0	1	**3**
1	1	1	0	**3**
1	1	1	1	**4**

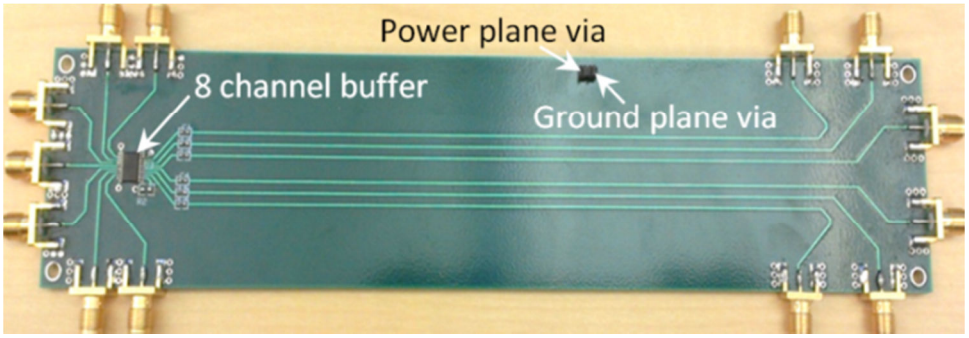
Encoded					
	DATA_TX				
INV	A'	B'	C'	D'	# of Ones
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	1	0	0	1
0	1	0	0	0	1
0	0	0	1	1	2
0	0	1	0	1	2
0	0	1	1	0	2
0	1	0	0	1	2
0	1	0	1	0	2
0	1	1	0	0	2
1	0	0	0	0	**1**
1	1	0	0	0	**2**
1	0	1	0	0	**2**
1	0	0	1	0	**2**
1	0	0	0	1	**2**

Figure 15 Truth table for 4-bit data and transmitted data sequence with bus-inversion encoding

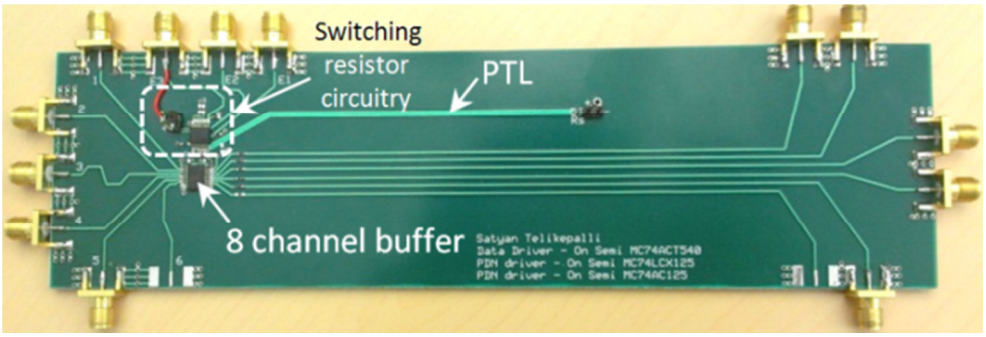
The physical design of the encoder and optimization of the encoding algorithm are beyond the scope of this thesis. However, it should be noted that bus inversion encoding, as well as its variants, are already used in commercially available products. In DDR4 SDRAM memory controllers, a feature called Data Bus Inversion (DBI) is used to improve data signal integrity and reduce power consumption. This scheme limits the number of 1s and 0s that are transmitted during each clock cycle in order to reduce the number of simultaneous switching outputs, lower crosstalk between adjacent data lines, and also decrease DC power consumption [25, 26].

Due to the difficulty in implementing a discrete resistor that is switched by a solid-state switch, it is necessary to implement this switching network using an alternate means. By placing extra drivers in the power supply path, one can dynamically affect the impedance that is seen by the PDN. Therefore, enabling these extra drivers effectively serves to add a series resistance onto the power supply path. It should be noted that these drivers in the test vehicle are inverting tri-state buffers. Therefore, the output enable pin is used to toggle the driver. Additional resistors, R_{p1} and R_{p2}, are placed at the output of the PDN drivers so that the resistances can be adjusted to the desired value. To account for the all 0s case, in which a shunt resistor must be selected (R[00] in Figure 12), an extra data driver (F2) is added.

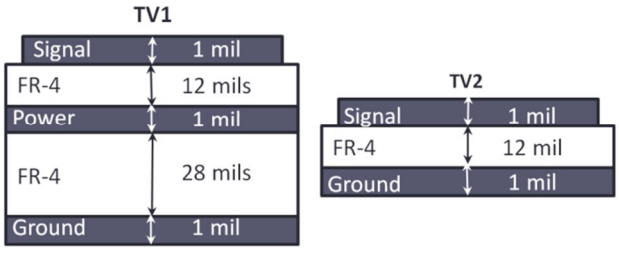
Photos of the test vehicles are shown in Figure 16 along with the corresponding stack-up of the PCB board. The board size for both test vehicles is 23.5cm by 5.21cm. Both test vehicles utilize the same data buffers with the same load impedances. The only difference in the two circuits is the method of power delivery. Detailed layouts and schematics of both test vehicles are shown in the appendix.



(a)



(b)



(c)

Figure 16 (a) TV1 with conventional power and ground planes, (b) TV2 with CV-PTL (c) layer stack up

It should be noted that from Figure 16, the board stack-ups for each test vehicle is quite different. Both test vehicles are fabricated on standard 4-layer FR4 PCB. For TV1, the bottom layer is not shown as it is not used in the design and no traces on routed on it. For TV2, the bottom two layers are not used. Because the PTL is used as the power delivery network, there is no dedicated power layer in TV2. For TV1, the stack-up is such that the power layer is below the top signal layer. If the power and ground planes are switched, this may mitigate some coupling between the signal and power planes, but it would not prevent the occurrence of return path discontinuities entirely. Since RPDs are created when the forward and return currents change reference planes, this would happen in either case, albeit in different locations on the package.

The relevant parameters for the test vehicle are shown in Figure 16 and Table 3, respectively.

Table 3 Test Vehicle Parameters

Description	Value
PTL characteristic impedance, Z_0	25 Ω
PTL termination resistor, R_S	25 Ω
Buffer output resistor, R_{OUT}	450 Ω
Signal line characteristic impedance, $Z_{0,SIG}$	50 Ω
Load resistance, R_L	50 Ω
On-resistance of data buffers, $R_{ON,DATA}$	11 Ω
On-resistance of PDN buffers, $R_{ON,PDN}$	13 Ω
Desired power supply voltage of data buffers, V_{DD}	4.5 V
Source voltage, V_S	5.3 V

The drivers used in both test vehicles require a supply voltage of 4.5V at the V_{DD} node. In order to maintain 4.5V at the V_{DD} node with a 5.3V source (V_S), and by using Equations 9-11, the resistor path values were determined to be 64Ω and 12Ω.

2.4 Measurement Setup

Both test vehicles were tested with an HP 83000 Automated Test Equipment (ATE) with a pseudo-random binary sequence (2^8-1 PRBS) at data rates of 100Mbps, 200Mbps, and 300Mbps. The measurement setup is shown in Figure 17.

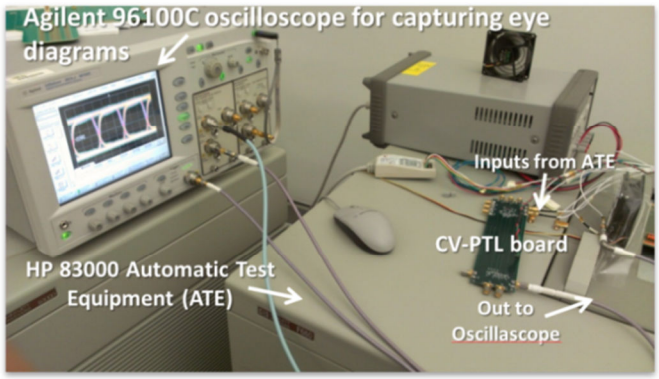


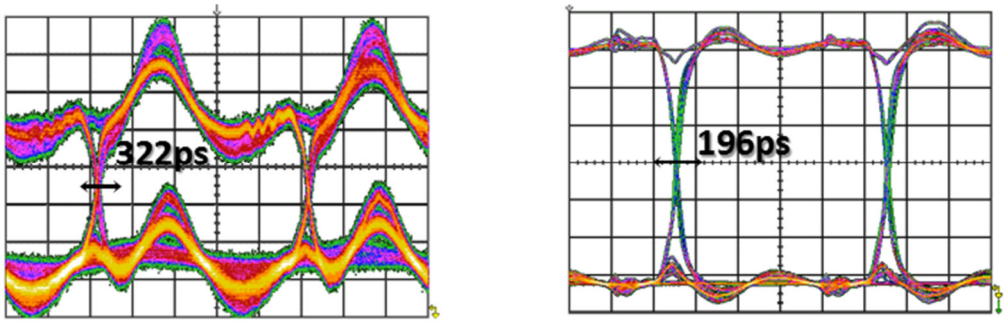
Figure 17 Laboratory setup for measurements

The ATE was programmed to provide both the test vehicles with the appropriate PRBS input pattern. For the TV2, the input was encoded using the bus inversion scheme, as described earlier in this section.

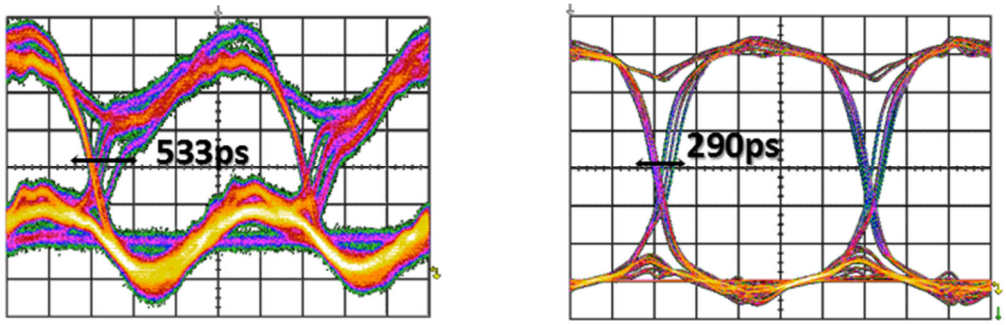
2.5 Measurement Results

The measured eye diagrams, as well as the time-domain waveforms of the output signal and power supply noise are shown below.

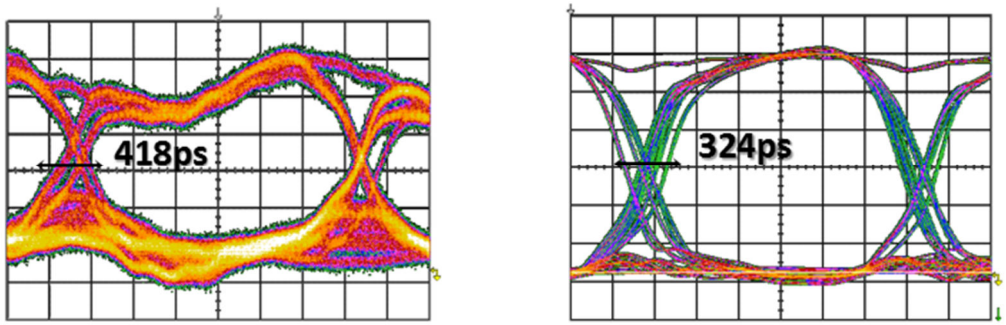
TV1 (Conventional) **TV2 (CV-PTL)**



(a) eye diagrams at f = 100Mbps



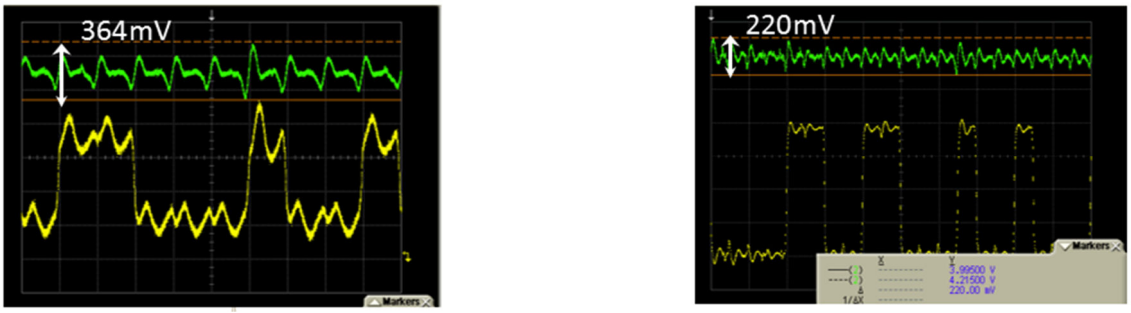
(b) eye diagrams at f = 200Mbps



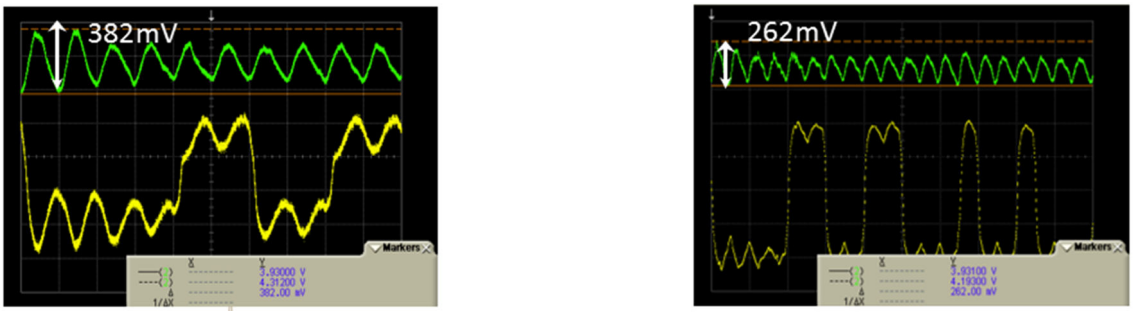
(c) eye diagrams at f = 300Mbps

Figure 18 Eye diagrams for both test vehicles

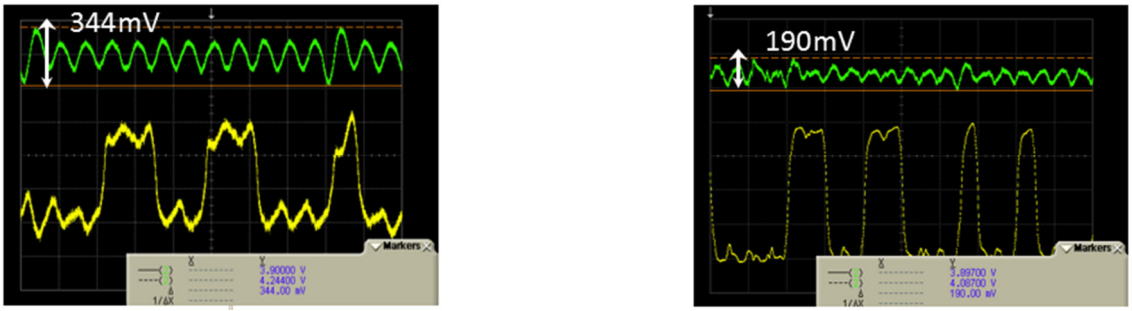
TV1 (Conventional) **TV2 (CV-PTL)**



(a) f = 100Mbps



(b) f = 200Mbps



(c) f = 300Mbps

Figure 19 Supply noise (top) and driver output voltage (bottom) for both test vehicles

In Figure 18 and Figure 19, the signal traces was referenced to the V_{DD} plane for the conventional design and hence the SI is worse than expected. It is also expected that the power supply noise would be the worst at 300Mbps. However, the noise is largest at 200Mbps. The test vehicles have dimensions of 23.5x5.21cm, so therefore, the power and ground planes will exhibit cavity resonances at certain frequencies due to the plane dimensions. It can be calculated that the $TM_{1,0}$ mode occurs at approximately 315MHz. In addition, the frequency spectrum of the PRBS

pattern exhibits a nulls at integer multiples of the data rate frequency, and local maximums in between. Consequently, at a data rate of 200Mbps, a local maximum exists at 300MHz. This harmonic of the PRBS signal, coupled with the $TM_{1,0}$ mode causes an increase in the supply noise at the 200Mbps measurement.

One can see that the use of the power transmission line with constant voltage significantly improves the shape of the waveform, as it reduces return path discontinuities and results in less power and ground bounce, as seen in the waveforms in Figure 19. Note that the "%Δ" values given in Table 2 compare the PTL results with the corresponding plane-based case. At the maximum operating data rate of the device, 300Mbps, the peak-to-peak jitter is reduced by 22.5% when using a constant voltage power transmission line as opposed to using conventional power and ground planes. This is due to the fact that the PTL reduces return path discontinuities by providing a smaller current loop on which the return current can travel.

Table 4 CV-PTL Measurement Summary

	Plane-based Test Vehicle		**PTL-based Test Vehicle**			
Data rate	**p-p jitter (ps)**	**ΔV_{DD} (mV)**	**p-p jitter (ps)**	**Jitter %Δ**	**ΔV_{DD} (mV)**	**ΔV_{DD} (mV) %Δ**
100Mbps	322	364	196	-39%	220	-39.5%
200Mbps	533	382	290	-46%	262	-31.4%
300Mbps	418	344	324	-22.5%	190	-44.7%

2.6 Power Calculations

Previous work showed the merits of using the (CC-PTL) and (PB-PTL) schemes [11, 17]. Both of these schemes show improvement in terms of signal integrity over the conventional power/ground plane PDNs, however, both suffer in terms of excess power consumption, as shown in Table 5 below.

Table 5 Truth table for uncoded binary pattern

Uncoded Binary Pattern				
A	B	C	D	SUM
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**2**
0	1	0	0	**1**
0	1	0	1	**2**
0	1	1	0	**2**
0	1	1	1	**3**
1	0	0	0	**1**
1	0	0	1	**2**
1	0	1	0	**2**
1	0	1	1	**3**
1	1	0	0	**2**
1	1	0	1	**3**
1	1	1	0	**3**
1	1	1	1	**4**
Average				**2**

The columns labeled “SUM” shows the total number of “high” states, or active drivers, that are transmitted during the respective clock cycle. For single-ended buffers with resistive load terminations, these states will consume more power than “low” output states. For a 4-bit uncoded binary pattern, there will be, on average, 2 high states transmitted for a perfectly random data pattern. For PB-PTL, there will always be 3 high states transmitted on each clock cycle [22]. No encoding scheme is used for CC-PTL, so its truth table will look like that of Table 5. However, since either the signal path or the dummy path will always be active during each clock cycle, there will always be 4 high states transmitted. However, by utilizing a CV-PTL PDN scheme, there can be either 1 or 2 “high” states at any given time, as shown in Table 8. Consequently, using this scheme for a PRBS input, on average, only 1.625 drivers will be active. Since less high states are encountered as compared to the other schemes, this would lead to considerable power savings in terms of static power consumption. However, this is only true if

the source voltage for all the schemes are the same, which is not the case when comparing CV-PTL, CC-PTL, and PB-PTL.

Table 6 Truth tables for PB-PTL and CV-PTL signaling schemes

PB-PTL						
A	B	C	D	E	F	SUM
0	1	0	0	1	1	3
1	0	0	0	1	1	3
0	0	1	1	0	1	3
0	1	0	1	0	1	3
1	0	0	1	0	1	3
0	1	1	0	0	1	3
1	0	1	0	0	1	3
1	1	0	0	0	1	3
0	0	1	1	1	0	3
0	1	0	1	1	0	3
1	0	0	1	1	0	3
0	1	1	0	1	0	3
1	0	1	0	1	0	3
1	1	0	0	1	0	3
0	1	1	1	0	0	3
1	0	1	1	0	0	3
Average						3

CV-PTL						
A	B	C	D	E	F	SUM
0	0	0	0	0	1	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	2
0	1	0	0	0	0	1
0	1	0	1	0	0	2
0	1	1	0	0	0	2
1	0	0	0	1	0	2
1	0	0	0	0	0	1
1	0	0	1	0	0	2
1	0	1	0	0	0	2
0	1	0	0	1	0	2
1	1	0	0	0	0	2
0	0	1	0	1	0	2
0	0	0	1	1	0	2
0	0	0	0	1	0	1
Average						1.625

The above analysis is purely statistical and does not take into account the physical quantities used in the real circuit. Consequently, the actual power consumed by the signaling topology was calculated and compared with an equivalent standard plane-based test vehicle as well as a test vehicle using Constant-Current Power Transmission Line (CC-PTL) topology. These calculations assume that, in all cases, the same data drivers are used as those discussed in the previous section and all parameters are the same as those shown in Table 1. The PDN drivers function to modulate the impedance of the PDN, which is required to counteract the data-dependent DC drop incurred by the presence of the terminating resistor R_S, as discussed in Section 1.4.1. The CC-PTL and PB-PTL methods address this issue through alternate means and therefore, there is no need for the PDN drivers for these methods. The PTL for the CV-PTL and CC-PTL case has a characteristic impedance of 25Ω and is terminated with a 25Ω resistor. Finally, in order to get the desired 4.5V at the power pins of the drivers, and to compensate for the voltage drop across the PTL termination and the PDN drivers and resistors in the CV-PTL

case, the power supply voltages used for the CV-PTL case is 5.4V, 4.75V for CC-PTL, and 4.5V for the standard plane-based case.

With the desired 4.5V at the power pins of the drivers and the 500 Ω load, each driver consumes approximately 8.8mA when "high". This is calculated from Equation (12).

$$I_{DD} = \frac{V_{DD}}{R_{ON,DATA} + R_{OUT} + R_L} = \frac{4.5V}{11\Omega + 450\Omega + 50\Omega} = 8.8mA \tag{12}$$

Since, on average, there will be 1.625 drivers activated for a PRBS input, the CV-PTL topology will consume 14.33mA. Therefore, with a 5.4V supply voltage, the CV-PTL circuit will dissipate on average 74.5mW of power. The corresponding figures for all the discussed signaling strategies are shown in Table 3.

Table 7 Power consumption calculations

	CV-PTL	**CC-PTL**	**PG**
Current for 1 driver (mA)	8.82	8.82	8.82
Average "high" drivers	1.625	4.0	2.0
Average Current (mA)	14.33	35.28	17.64
Voltage Source (V)	5.4	4.75	4.5
Average Total Power (mW)	**74.53**	**167.58**	**79.38**

From Table 7, the CV-PTL strategy consumes approximately 55% less power than the CC-PTL case and less than the standard power/ground plane case, while also providing significantly better signal integrity, as shown in Table 4.

2.7 Summary

This paper presents a new power delivery network called constant-voltage power transmission line (CV-PTL). This signaling scheme provides power through a transmission line in place of a power plane while dynamically changing the resistance of the power delivery network to keep a constant voltage at the power pin of the IC. Consequently, this reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. Two test boards were fabricated, one with conventional power and ground planes, and the other with the PTL-based power delivery network. The test boards were measured with a PRBS input signal and encoded using a bus inversion encoding scheme. The signal quality of the output waveform was measured and analyzed in the form of transition jitter as well as power supply fluctuation. Measurements of jitter show that by using the CV-PTL configuration, the total peak-to-peak jitter can be reduced by up to 46% and the supply voltage variation can be reduced by up to 44.7% as compared to using a power plane, while also exhibiting significant power savings.

CHAPTER 3: CV-PTL APPLIED TO 3D INTEGRATED CIRCUITS & POWER ANALYSIS

3.1 Introduction

The previous chapters presented techniques that can be used to reduce the amount of power supply noise in high speed digital I/O circuits. Board-level test vehicles were designed and tested to verify the efficacy of the concept. However, as the demand for smaller, faster, and more power efficient systems grows, there is a shift toward emerging technologies, such as system-on-chip (SoC) or system-on-package (SoP). These technologies allow digital, analog, RF, and passive components to be fabricated onto the same die or package. In addition, stacking multiple dies or multiple-stacked ICs onto a single package has been shown as being a viable approach [27]. 3D-based IC technology provides many advantages in terms of integration, system speed, and lowering power consumption. In a 3D IC system, multiple chips are stacked together by through silicon vias, or TSVs, and micro bumps. TSV technology greatly reduces the interconnection lengths between vertically stacked ICs, thereby reducing interconnect parasitics, and increasing channel bandwidth. The stack is then soldered onto a Printed Circuit Board (PCB) using a silicon interposer or package. The addition of structures such as TSVs and solder bumps further contribute to the existing parasitic inductance of the overall structure. As demonstrated in [6], the inductance increases from a lower die to the next higher die along the stack. To overcome this problem, the Constant Voltage Power Transmission Line (CV-PTL) signaling scheme is used to supply power to a 3D stack. Through simulation it is shown that high speed signaling between the dies in the stack is possible with minimum jitter and maximum eye height with this PDN. In addition, this scheme achieves significantly reduced power consumption when

compared to the PDN schemes used in [8, 11], which are based on constant current- and pseudo-balanced PTL signaling.

3.2 3D System Simulation Model

In the following sections we apply the conventional PDN and CV-PTL design approaches to 3D ICs on silicon interposers mounted on a printed circuit board (PCB). The 3D system considered here consists of a first-level package, an interposer, and three IC dies stacked on each other as shown in Figure 8. Each die size is 1mm x 1mm. Each IC contains a TSV layer, PDN and digital logic. For the remainder of the document, the phrase "conventional PDN" will refer to the use of a power and ground plane on the PCB as opposed to a PTL.

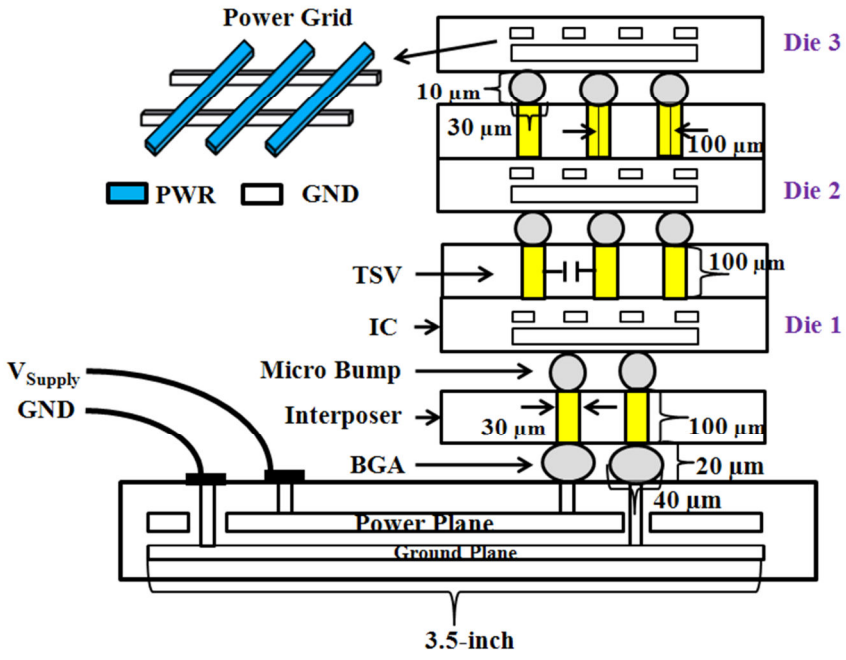
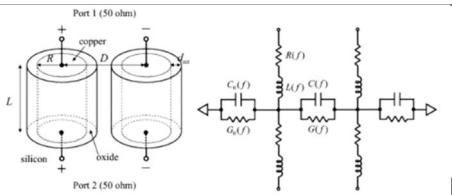


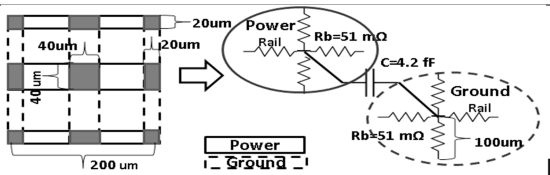
Figure 20 Cross-sectional view of a conventional power-plane 3D system [8, 19]

The TSV layer is modeled based on [28]. It consists of three TSV types; namely power, signal and ground TSVs. The interposer model was constructed using CST [29], a 3D electromagnetic simulation solver. It contains a power and ground TSV pair. All TSVs are surrounded by a 0.1µm thick oxide layer. The micro bumps and ball gate array (BGA) balls between layers are modeled as a resistor in series with an inductor. Resistance and inductance of BGA balls are 2.4mΩ and 6.44pH, respectively, while those of micro bumps are 2.8mΩ and 0.8pH, respectively. The PDN contains power and ground grid corresponding to the top metal layers in the IC. In each grid, the rails are laid out orthogonally in two separate layers separated by 40um with rail width of 40um. Each grid is divided into unit cells with individual cell size 200µm x 200µm.

Each cell is modeled as two separate resistor networks with resistance in each branch (R_b) calculated to be ~51 mΩ. The coupling capacitance between power and ground rails within a cell is approximated to be 4.2fF. The package for the power plane-based design is a two layer board with a power and ground plane [3]. The plane model was created using Sonnet EM simulation software [16]. The source is modeled as an ideal voltage source in the simulations. A summary of how each component is modeled is described in Table 8.

TABLE 8 SUMMARY OF COMPONENT MODELING

Component	**Model**
Silicon Interposer	CST (S-Params)
Through Silicon Vias with 0.1µm SiO_2	 [28]
Micro bumps	Lumped: 2.8mΩ + 0.8pH
BGA balls	Lumped: 2.4mΩ + 6.44pH

Power and ground grid	 [8]
PCB Model (3.5”)	Sonnet EM (S-Params)
Voltage Source	Ideal

The impedance profile of the power rail was simulated for the 3D system utilizing the power and ground plane, and shown in Figure 21 [8]. In addition, the impedance profile for just the interposer and the stack-up (not including the PCB package) is shown in Figure 22.

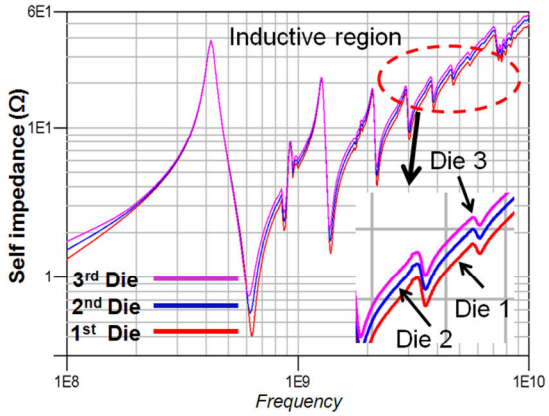


Figure 21 Impedance profile at each die, including package [8]

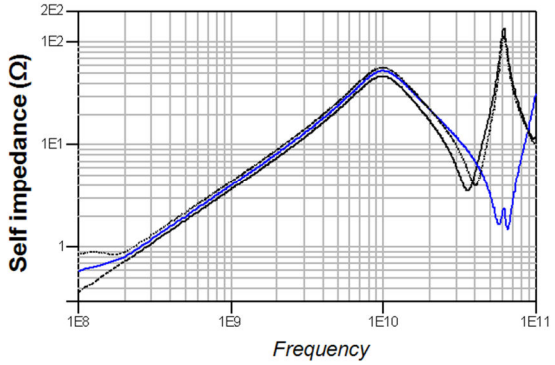
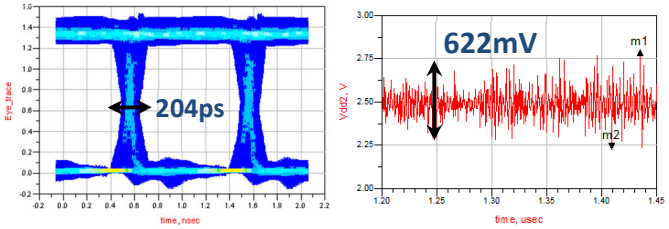
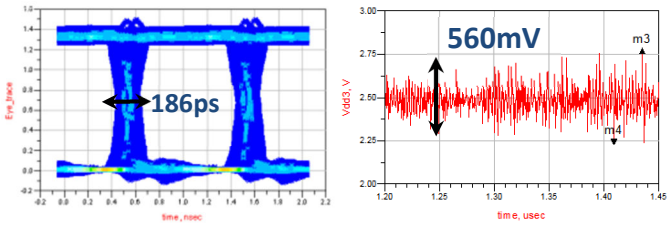


Figure 22 Impedance profile of interposer and stack-up only

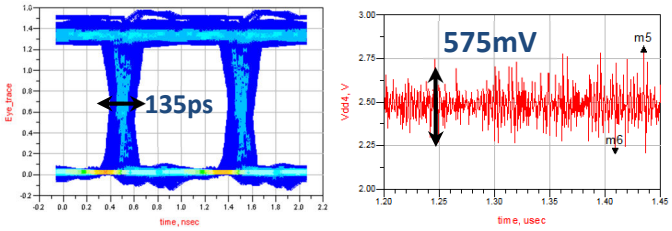
In order to obtain the impedance profile, the ports are placed in the middle of the power grid (see Figure 20) at each stack. The impedance profile in Figure 21 shows many fluctuations versus frequency. These are due to the cavity mode resonances of the power and ground plane cavity. When the switching frequency, or a higher-order harmonic, of the data driver corresponds to a cavity resonance frequency, this can cause large voltage fluctuations on the supply node due to higher PDN impedance at that particular frequency. In addition, the impedance profile of the power rail for each of the three IC dies increases as one moves up the stack. More importantly, the impedance in the inductive region increases as the position of die in the stack increases. This trend is also corroborated by [6]. As a result of this increased inductance, the power supply noise will increase as the position of the die in the stack increases. This phenomenon is reinforced by the study detailed in [7]. However, one can see that in Figure 22, when the PCB package is not included, the impedance profile is smooth up to about 10GHz. This means that the resonance peaks are primarily attributed to the package, and by modifying the package-level PDN, one can mitigate the effect of the switching noise. The figures below show the resulting eye diagrams of the output of each driver at each layer. A 4-bit pseudo-random binary stream (2^8-1 PRBS) pattern was used as the input at 1Gbps. Each eye diagram was measured at the output of each signal buffer and the supply noise was measured at the supply pin of each buffer. In addition, each buffer is terminated to 50Ω and is fed by an input signal on the same layer. One can see that the eye quality deteriorates as one goes up the stack due to an increase in the power supply noise.



(a) Top layer, jitter = 204ps, ΔV_{DD} = 622mV



(b) Middle layer, jitter = 186ps, ΔV_{DD} = 560mV



(c) Bottom layer, jitter = 135ps, ΔV_{DD} = 575mV

Figure 23 Simulated eye diagrams at the output of drivers on each layer with 1Gbps PRBS input with a conventional planar PDN

The transition jitter determined from the eye diagrams shown above is 204ps, 186ps, and 135ps, for stack 3 (top), stack 2, and stack 1 (bottom), respectively. Correspondingly, the peak-to-peak voltage variation on the V_{DD} node of the drivers is 622mV, 560mV, and 575mV, for stack 3, stack 2, and stack 1, respectively.

3.3 CV-PTL Results for 3D Stack

The simulation results for the conventional plane-based PDN shown above serve as a baseline for comparing the signal and power integrity in a 3D system. The CV-PTL PDN scheme was also integrated into the same 3-layer 3D stack-up shown in the previous section to demonstrate the methodology's effectiveness when used in a 3D system. The CV-PTL circuitry was simulated with 4-data bits. However, by utilizing the bus-inversion encoding scheme described in Section 2.3, the input data is encoded into 6-bits. The encoding scheme is used to reduce the amount of variation in the driving current through the PDN by encoding the original

data bits into data words with minimal change in the number of 1s and 0s that are transmitted. The important parameters used in the simulation are shown in Table 9.

Table 9 CV-PTL 3DIC simulation parameters	
PTL characteristic impedance, Z_0	25Ω
PTL termination resistor, R_S	25Ω
Signal transmission line $Z_{0,sig}$	50Ω
Load resistance, R_L	50Ω
On-resistance of data buffers	39Ω
Desired power supply voltage of data buffers, V_{DD}	2.5V
Source voltage, V_{DD}'	4.0V

The resulting resistor values, according to Equations (7)-(11), are R[1] = 28Ω and R[2] = 2Ω. The simulation models for the data drivers, TSVs, silicon interposer, micro bumps, BGA balls, and IC PDN are the same as used in Section 3.2. The one difference is that on the PCB layer, instead of utilizing a power and ground plane, three power transmission lines (PTLs) are placed going from the supply voltage to the BGA balls located below the bottom layer. Each PTL will supply power to each layer. In addition, each die includes the extra CV-PTL circuitry, such as the additional buffers that are necessary for implementing the dynamic resistor paths, as discussed in Section 2.3. This implementation is shown in Figure 24. It is important to note that while the impedance profile for the conventional 3D stack design, like that shown in Figure 21, can be used to analyze the various resonances points in the voltage planes, it has no purpose in this design. In this PTL based design, since there are no planes on the PCB, the impedance profile does not show any relevant information, and consequently is not shown here.

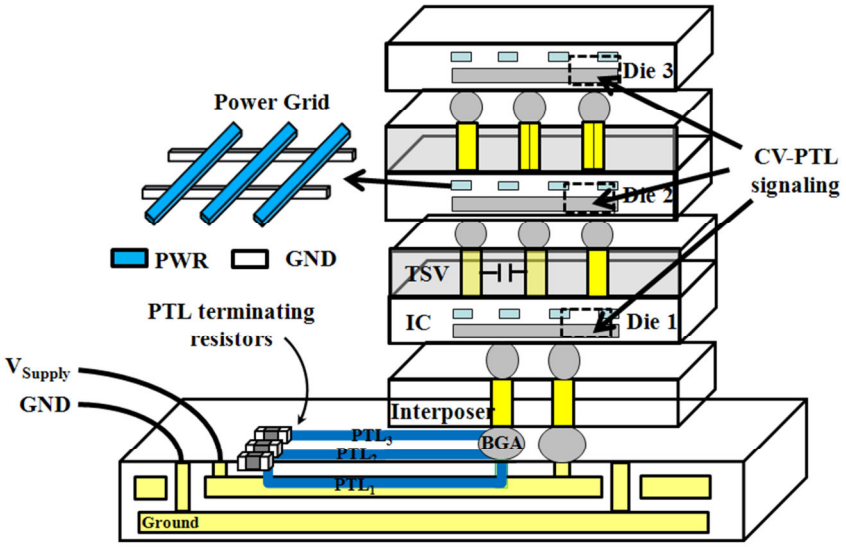
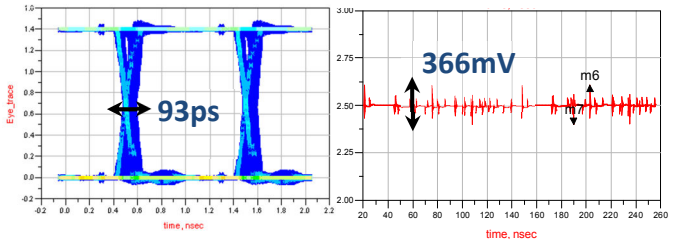
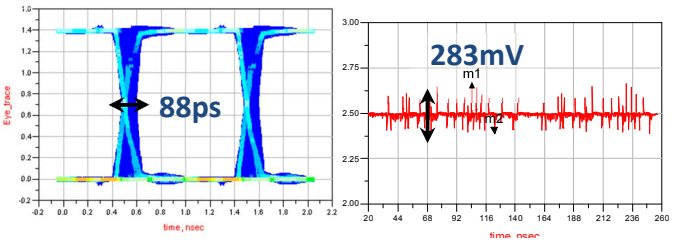


Figure 24 Cross-sectional view of the 3D system using CV-PTL

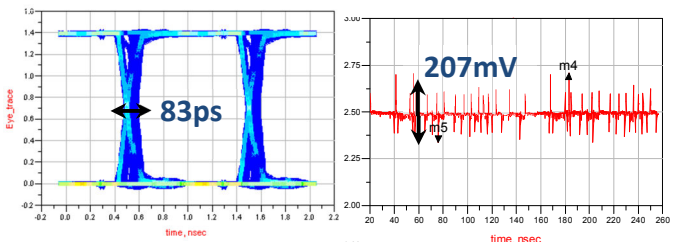
The figures below show the resulting eye diagrams of the output of each driver at each layer when using the CV-PTL PDN scheme.



(a) Top layer, jitter = 93ps, ΔV_{DD} = 366mV



(b) Middle layer, jitter = 88ps, ΔV_{DD} =283mV



(c) Bottom layer, jitter = 83ps, ΔV_{DD} = 207mV

Figure 25 Simulated eye diagrams at the output of drivers (left column) and power supply voltage variation (right column) on each layer utilizing CV-PTL

The eye diagrams and the power supply noise are considerably improved when using the CV-PTL methodology. The transition jitter determined from the eye diagrams and the corresponding peak-to-peak power supply noise is 93ps and 366mV, 88ps and 283mV, and 83ps and 207 mV, for stack 3 (top), stack 2, and stack 1 (bottom), respectively. The reduction in the transition jitter and p-p supply noise compared to the PDN scheme in Figure 8 is approximately 38.5% and 64%, 52.7% and 49.5%, and 54.4% and 41.2%, in the bottom, middle, and top stack, respectively, which is substantial. The power transmission line serves to reduce the effect of return path discontinuities. As described previously, the switching resistor network functions to modulate the impedance of the PDN, which is required to counteract the data-dependent DC drop incurred by the terminating resistor R_S. Consequently, for a PDN design using power and ground planes, there is no source terminating resistor, so the switching resistor paths would not be effective in improving supply noise. In addition, there were no decoupling capacitors used in the simulations as the primary purpose of this work was to compare the effectiveness of both PDN methods in reducing simultaneous switching noise under the same conditions. Since the CV-PTL design exhibits considerably less switching noise, it can be concluded that smaller value decoupling capacitors can be used to meet the same noise margin goals as compared to that of the conventional PDN design.

3.4 Power Consumption Comparison

It is shown in [8] the feasibility of extending the power transmission line concept to 3D systems. More specifically, the work showed the results of using CC-PTL PB-PTL schemes in a 3D integrated circuit. While both of these schemes show an improvement in terms of signal integrity over using power and ground plane PDNs, they both suffer in terms of excess power consumption. In Section 2.6, the DC power consumption of the CV-PTL scheme was presented. However, that analysis was purely statistical and did not take into account the losses associated with the resistor network or the differing source voltages. Consequently, a more thorough power consumption analysis is needed. The following discusses the issue of power consumption with the physical quantities used in the real circuit. Consequently, the actual power consumed by both circuits, one utilizing a power and ground plane and the other with the CV-PTL scheme, was simulated and compared with a 1Gbps 256-bit long PRBS input pattern. The instantaneous power is calculated by multiplying the voltage source (V_S = 2.5V for the power and ground plane circuit, and V_S = 4.0V for the CV-PTL circuit) by the instantaneous current sourced by the entire circuit at the supply. The power consumed by the 3D stack for each of the CV-PTL and conventional PDN is shown in Figure 26 and Figure 27, respectively.

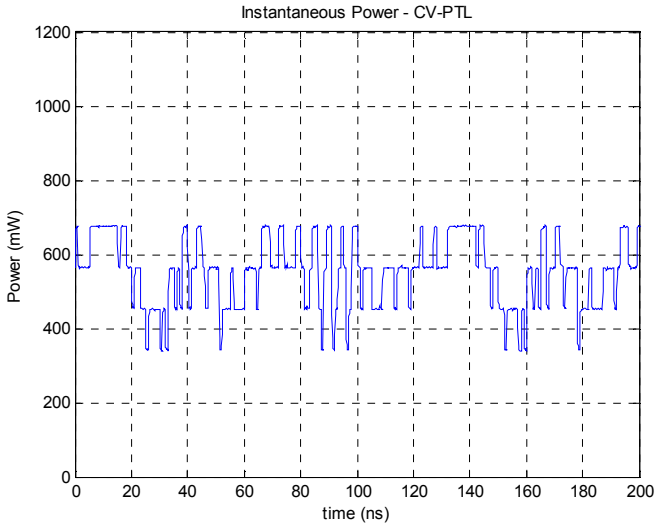


Figure 26 Instantaneous power consumed by the CV-PTL 3D stack (in mW) with 256-bit long PRBS signal at 1Gbps

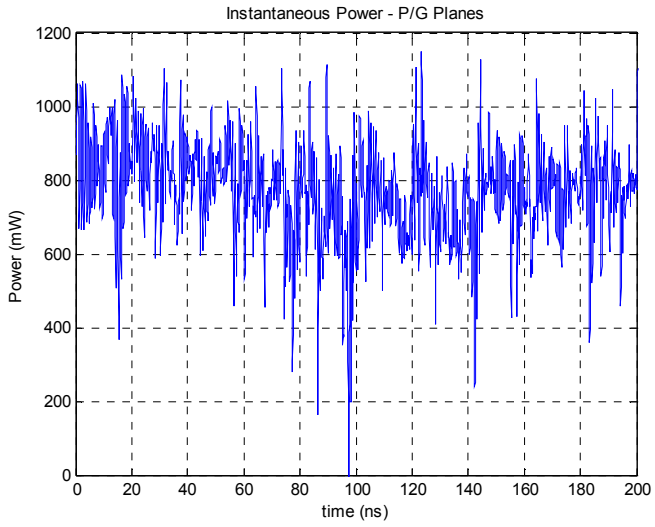


Figure 27 Instantaneous power consumed by the conventional PDN circuit

The total energy consumed by the circuit with the same input pattern at 1Gbps, as well as the energy/bit values are summarized below. In the simulations, 256 bits were transmitted to all 12 data buffers (4 buffers on each of the 3 dies). The total energy dissipated by the each circuit is obtained by integrating the instantaneous power over the entire time period. Consequently, the energy/bit is calculated by dividing the total energy by 3072 (256 bits · 4 bits/die · 3 die). These

figures take into account the losses associated with the resistor network as well as the increased supply voltage.

Table 10 Energy savings comparison

Scheme	Total Energy	Energy/bit	%Δ of CV-PTL
CV-PTL	0.099µJ	32.2pJ	N/A
PB-PTL [17]	0.124µJ	40.4pJ	**+25.5%**
CC-PTL [11]	0.165µJ	53.7pJ	**+67.0%**
P/G Planes	0.110µJ	35.8pJ	**+11.5%**

In the above simulation and analysis, the CV-PTL scheme used a supply voltage of 4.0V, while the PB-PTL and P/G Plane circuits used the nominal 2.5V supplies. This is because, from Figure 12 and Figure 24, the PTLs are terminated with resistors. The PTL terminating resistor serves to prevent any reflections that may occur on the line that can propagate across the line and back into the driver's power pin. However, the voltage drop across the terminating resistor means the supply voltage must be raised in order to meet the V_{DD} requirements of the I/O buffers.

From Table 10, one can see that the CV-PTL scheme consumes significantly less power than the conventional scheme. Although the CV-PTL scheme has a higher supply voltage, the energy to transmit each bit is still less than the other signaling schemes, even the conventional scheme utilizing power and ground planes. For a 256-bit PRBS input pattern, the CV-PTL circuit dissipates 11.5% less power than the conventional scheme. In addition, the power consumption calculations were extended to include the PB-PTL scheme as well. With the same PRBS input pattern, and a 4b/6b encoding, the PB-PTL encoding would consume about 0.124µJ, which translates to approximately 40.4pJ/bit. This is a 25.5% increase from what is expected from the CV-PTL implementation.

3.5 Summary

In this chapter, we propose to replace the power planes that are commonly used in conventional PCB designs with power transmission line (PTL) to deliver power directly to an IC. This enables the elimination of return path discontinuities which would otherwise degrade signal quality. The CV-PTL signaling scheme was previously shown to improve signal integrity on a board level design by reducing the effect of return path discontinuities and in turn, mitigating the effects of power and ground bounce [22]. Here, we have shown that this novel signaling scheme can also be extended to 3D integrated circuits with the same benefits in signal and power integrity. It has been demonstrated through simulation that power supply noise worsens as one goes higher up in the stack of dies. However, by utilizing the CV-PTL concept in the PDN design of a 3-layer 3DIC system, the circuit showed considerable improvement in power supply noise and p-p jitter as compared to the conventional design approach. In the CV-PTL circuit, the transition jitter showed improvement of over 50% when comparing the transition jitter in each layer. In addition, the supply noise is reduced by 40-60% in each layer.

In addition, the power consumption of the proposed PDN design was analyzed. The analysis shows that the CV-PTL scheme consumes less power than the typical method of using power planes for a random bit sequence. The results and analysis presented here confirm the validity and possibility of utilizing the CV-PTL design in power delivery networks for integrated 3D systems.

CHAPTER 4: INTEGRATED VOLTAGE REGULATOR MODULE

4.1 Introduction

The results presented in Sections 2.2 validate the CV-PTL concept on the board-level. However, the selected components and implementation method limits the maximum switching frequency of the data driver to 300Mbps. In order to make this scheme more competitive with state of the art signaling schemes, it is desirable to operate at much faster data rates. The switching resistor paths function to keep the voltage at the data driver's supply pin constant while allowing the current to change as needed. This behavior is similar to a digitally controlled linear voltage regulator. Consequently, the possibility of incorporating the CV-PTL scheme into an integrated solution is investigated in this chapter. Furthermore, the objective of this work is to investigate signal integrity issues when an integrated voltage regulator module is used in conjunction with a power transmission line. A custom chip was designed and will be fabricated with a 0.18μm CMOS process to verify this scheme on an IC scale. The IC consists of an integrated low-dropout linear regulator (LDO) powering 6 parallel-connected output buffers.

In modern high speed digital systems, multiple voltage regulators are distributed throughout the board to deliver accurate and clean power to various components. It is desirable to place the regulators as close to the load circuits as possible to minimize supply impedance and regulation delay. However, due to board size constraints, this is usually not possible, and a more feasible solution is to use a point-to-point regulator distribution system using multiple regulators throughout the system. In addition, advancements in integration technologies have allowed regulators to be integrated on the die or package with the load circuits. It is has been shown in recent literature that significant performance improvement can be achieved by utilizing per-core

voltage regulators with dynamic voltage and frequency scaling (DVFS) algorithms [30] and fully integrated on-chip switching regulators [31].

4.2 Design Process

4.2.1 Process & Circuit Specifications

The circuits are to be implemented on a 0.18µm CMOS process with the specs shown in Table 11.

Table 11 Process specification

Process node	**0.18µm CMOS**
Layers	1 polysilicon layer 6 metal layers
Devices voltages	1.8V (thin oxide)/3.3V (thick oxide)/5V
Minimum gate length	0.18µm for 1.8V devices 0.30/0.35µm for 3.3V devices (thick oxide)
Substrate	P-substrate with N-wells
Max Design Area	3.8mm x 3.8mm

The IC design was done as part of a multi-project wafer service (MPW) in collaboration with KAIST and is being fabricated using a 0.18µm CMOS process from MagnaChip Semiconductor and SK Hynix. In Figure 28, the schematic of the CV-PTL circuit implemented in Section 2.3 is shown along with the linear voltage regulator. The voltage regulator consists of several components, including a pass transistor, an error amplifier, a voltage divider sampling network, and six output buffers.

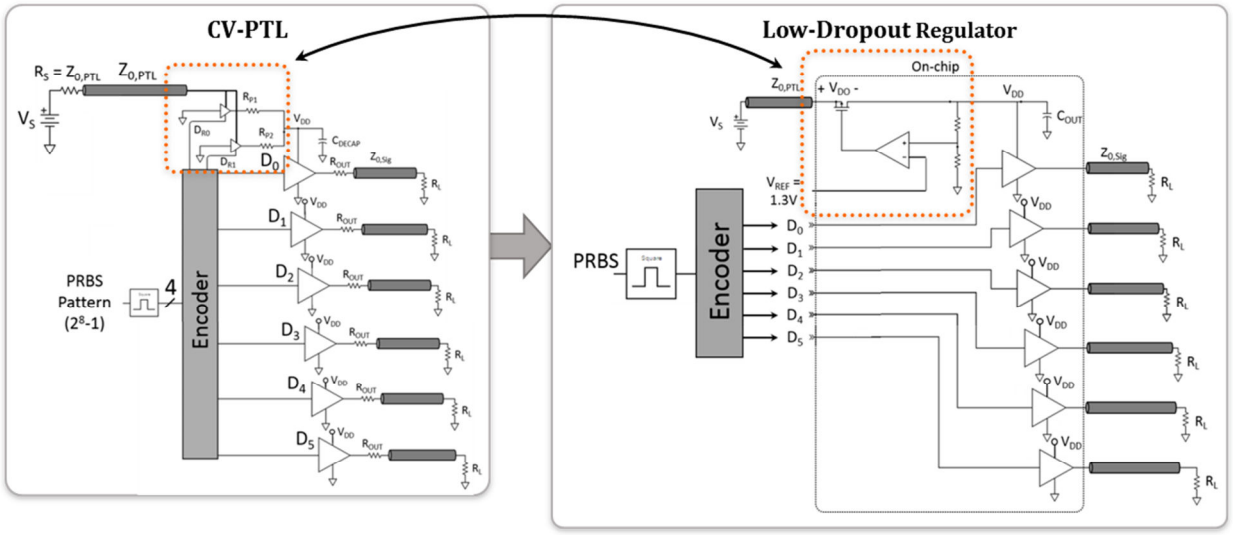


Figure 28 Schematic of CV-PTL implementation and voltage regulator circuit

As presented in Chapter 2, the CV-PTL circuit was implemented by using a set of buffers and output resistors to modulate the PDN impedance. The circuit was implemented with off-the-shelf components on a PCB. In Figure 28, the switching resistor circuit is replaced with a low dropout voltage regulator. The integrated circuit solution will present several benefits over the CV-PTL test vehicle. Firstly, the linear regulator will be able to operate at much higher frequencies. In addition, the control signals for toggling the PDN buffers in the CV-PTL test vehicle were provided with a separate FPGA or an automatic testing equipment (ATE). For the integrated circuit, the feedback loop will be self-regulating. Also, a 1.3V reference voltage required for the error amplifier will be provided externally. The design of the integrated low dropout voltage regulator and the buffers will be presented in this chapter.

A simplified circuit schematic of the voltage regulator is shown in Figure 29.

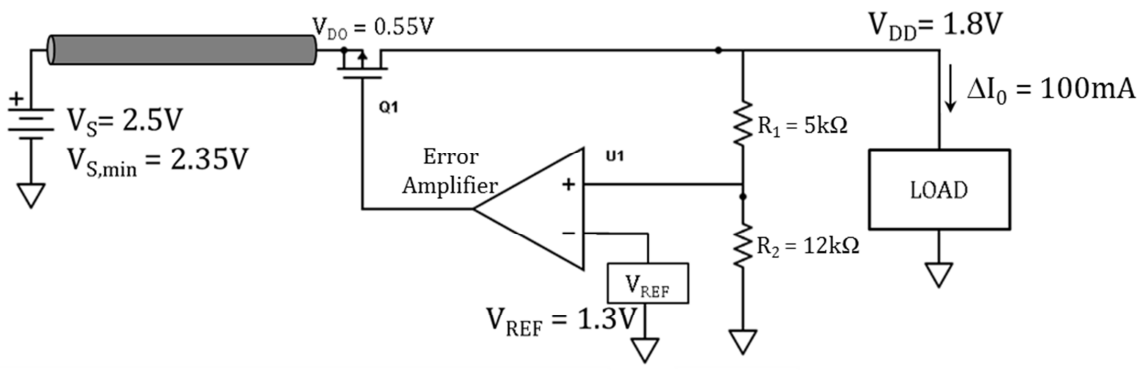


Figure 29 Voltage regulator circuit schematic

The nominal input voltage (V_S) to the regulator is 2.5V and the regulated output voltage (V_{DD}) is 1.8V. The maximum output current swing supported by the regulator is 20-100mA. The minimum operating input voltage is 2.35V, so the minimum drop-out voltage is approximately 0.55V. Therefore, if V_S drops below 2.35V, the pass transistor will not operate in the saturation region and V_{DD} will not be regulated at 1.8V.

The following sections describe the design for each component. The input voltage to the LDO is 2.5V. To ensure reliable operation, the thick-oxide 3.3V devices were used. Consequently, the minimum gate width is 0.35µm for NMOS and 0.30µm for PMOS devices.

4.2.2 Pass Transistor

The pass transistor must support the total load current and must be properly sized such that it has a low dropout voltage, and therefore good power efficiency. There are several methods for designing the pass transistor, such as using a Darlington pair, or an NMOS/PMOS transistor. Table 12 describes the differences in these pass element types.

Table 12 Pass transistor types (reproduced from [32])

Parameter	Darlington	NMOS	PMOS
$\mathbf{I_{O,max}}$	High	Medium	Medium
$\mathbf{I_Q}$	Medium	Low	Low
$\mathbf{V_{dropout}}$	$V_{Sat} + 2 \cdot V_{BE}$	$V_{Sat} + V_{GS}$	$V_{SD(Sat)}$
Speed (transient response time)	Fast	Medium	Medium

A Darlington pair configuration can support the highest output current due to its inherently high current gain and can also achieve the fastest response time. However, bipolar devices suffer from low power efficiency. MOS transistors offer the best power efficiency due to lower saturation voltages. A PMOS device is chosen for the pass transistor because the dropout voltage is $V_{DO} = V_{SD(sat)}$, as opposed to $V_{DO} = V_{SD(sat)} + V_{GS}$ for an NMOS. In order to keep the saturation voltage, and therefore the on-resistance and dropout voltage low, the pass transistor is generally made to be relatively large. In this design, the dimensions of the transistor are W_{gate} = 1mm and $L_{gate} = L_{min,p}$ = 300nm.

The gate of this pass transistor is driven by the error amplifier, and therefore its gate capacitance must be determined as it will serve as the load for the error amplifier. From [33], the total gate capacitance for a MOS transistor in saturation can be approximated by Equation (13).

$$C_G \cong G_{GS} + C_{GD} = \frac{2}{3} WLC_{OX} = 3.54pF \tag{13}$$

4.2.3 Error Amplifier

The error amplifier used for the regulator is a two-stage CMOS op-amp with miller compensation, as shown in Figure 30.

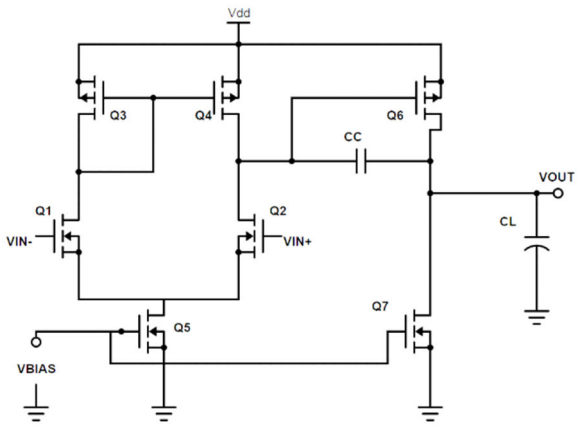


Figure 30 Two-stage CMOS op-amp

A single stage CMOS op-amp has only one dominant pole so stability is generally not an issue. However, a two-stage design has two dominant poles, therefore the location of the poles and the unity gain frequency must be carefully considered to prevent the amplifier from becoming unstable when it is operated in a feedback loop. The unity gain frequency is the frequency at which the magnitude of the open-loop gain is equal to 1, or 0dB. The stability condition is met when the unity gain frequency is lower than the frequency at which the open-loop phase response changes by 180° from its DC value.

$$|A_{OL}(j\omega_0)| < 1$$

Where ω_0 is defined as (14)

$$\angle A_{OL}(j\omega_0) = 0°$$

Therefore, a frequency compensation technique must be employed to ensure the stability condition is met. In this work, a frequency compensation called “pole splitting” is used. In this technique, the lower pole is moved to lower frequencies while the higher pole is moved to a higher frequency. Consequently, this increases the stability and step response of the amplifier, but at the expense of a lower bandwidth. An undesirable side-effect of this technique is the right-half plane (RHP) zero that is created. However, the effect of the RHP zero can be mitigated by

moving it to a very high frequency. This effect of this technique on the amplifier's open loop frequency response is shown in detail in Figure 31.

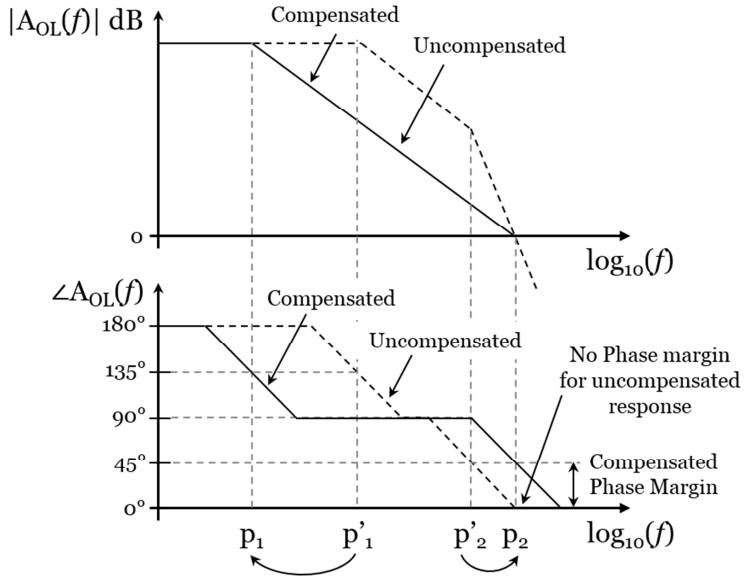


Figure 31 Effect of miller compensation

The initial design specifications of the error amplifier are shown in Table 13.

Table 13 Initial Error Amplifier Specifications

Specification	Value
L_{NMOS}, NMOS gate length	0.35µm
L_{PMOS}, PMOS gate length	0.30µm
V_{DD}, Supply voltage	2.5V
A_V, Open Loop DC gain	46dB
C_L, Load capacitance	3.54pF
ICM+, Maximum input common mode	1.9V
ICM-, Minimum input common mode	1.2V
SR, Slew Rate	2 V/µs
GBP, Gain bandwidth product	50 MHz
PM, Phase Margin	60°

The small-signal model of a 2-stage CMOS op-amp is shown in Figure 56. The important equations pertaining to the design of the error amplifier are shown in Table 14, but for a complete derivation of all these equations, the reader can refer to [33] and [34].

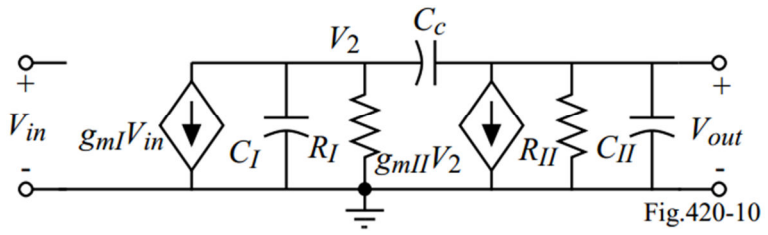


Figure 32 Small-signal approximation of 2-stage CMOS amplifier for frequency-response analysis [33]

Table 14 Design equations for a two-stage CMOS amplifier

Description	Equation	
DC gain	$A_{DC} = g_{m1}R_1 \cdot g_{m2}R_2$	(15)
Output resistance of first stage	$R_1 = r_{o2} \parallel r_{o4}$	(16)
Output stage of second stage	$R_2 = r_{o6} \parallel r_{o7}$	(17)
First stage transconductance	$G_{m1} = g_{m1} = g_{m2}$	(18)
First stage transconductance	$G_{m2} = g_{m6}$	(19)
First pole frequency (rad/s)	$p_1 = \frac{1}{G_{m2}R_2R_1C_C}$	(20)
Second pole frequency (rad/s)	$p_2 = \frac{G_{m2}}{C_2}$	(21)
Zero frequency (rad/s)	$z = \frac{G_{m2}}{C_C}$	(22)
Gain bandwidth product	$GBW = \frac{G_{m1}}{C_C}$	(23)
Slew rate	$SR = \frac{I_O}{C_C}$	(24)
Phase of transfer function	$\angle\frac{V_o}{V_{id}} = -\tan^{-1}\left(\frac{\omega}{z}\right) - \tan^{-1}\left(\frac{\omega}{p_1}\right) - \tan^{-1}\left(\frac{\omega}{p_2}\right)$	(25)
Phase evaluated at GBW	$-180° + 60° = -\tan^{-1}\left(\frac{1}{10}\right) - \tan^{-1}\left(\frac{G_{m1}G_{m2}R_1R_2}{1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right)$	(26)

frequency for phase margin of 60°.		

A common rule of thumb used in the design of a miller compensated amplifier is to place the zero at a much higher frequency than the unity gain frequency. So consequently, it is chosen to keep $z = 10 \cdot GBW$. The result of this assumption is given by Equation (27).

$$z = 10 \cdot GBW \rightarrow C_C = 0.22 \cdot C_L \tag{27}$$

In addition, simplifying Equation (26), results in Equation (28).

$$p_1 = 2.2 \cdot GBW \tag{28}$$

From Equation (29), the minimum value of the compensation capacitance can be determined.

$$C_C = 0.122 \cdot C_L = 0.122 \cdot 3.54pF = 0.42pF \tag{29}$$

The minimum value of the capacitance is C_C = 0.42pF, so the compensation capacitor was chosen to be twice this value, C_C = 0.84pF, in case the load capacitance is larger than expected. The slew rate of the error amplifier is dictated primarily by the bias current provided by transistor Q_5 in Figure 30. The initial specification calls for the slew rate to be 2 V/μs.

$$SR = \frac{I_O}{C_C} = 2\frac{V}{\mu s} = \frac{I_O}{0.84pF} \Rightarrow I_O = 17.3\mu A \tag{30}$$

As with the compensation capacitor, the bias current is increased by 50% to allow for a margin in the slew rate, and therefore the bias current is 25.9μA. The size of the differential amplifier

transistors can be determined by first calculating g_{m1} (since $g_{m1} = g_{m2}$), which is accomplished with Equation (23).

$$GBW = \frac{G_{m1}}{C_C} \Rightarrow G_{m1} = 0.27 \Rightarrow 0.30mS \tag{31}$$

$$\frac{W}{L}_1 = \frac{W}{L}_2 = \frac{2 \cdot I_D}{\mu_n C_{ox} \cdot (V_{GS} - Vth)^2} = \frac{(g_{m1})^2}{2 \cdot I_O \cdot \mu_n C_{ox} \cdot (V_{GS} - V_{th})} = 22.5 \tag{32}$$

Transistors Q3 and Q4 in Figure 30 form an active load for the differential pair. The size of these transistors is related to the maximum input voltage, the maximum input common mode specification. The ICM+ is the maximum input voltage to ensure that Q3 and Q4 remain in saturation.

$$\frac{W}{L}_3 = \frac{W}{L}_4 = \frac{2 \cdot \left(\frac{I_O}{2}\right)}{\mu_n C_{ox} \cdot \left(V_{DD} - ICM_+ - V_{th.max} - V_{th,min}\right)^2} = 1.2 \tag{33}$$

Similarly, the size of transistor Q5 is related to the minimum input voltage, ICM- specification, which is the minimum input voltage to ensure that Q5 remains in saturation. More specifically, Equation (34) must be satisfied.

$$(ICM_-) > V_{GS1} + V_{DSsat_5} \tag{34}$$

Since the bias current flowing through Q1 is $I_0/2$, or 13µA, the gate-source voltage of Q1 can be determined and substituted into Equation (34) to get the saturation voltage of Q5.

$$V_{GS_1} = \sqrt{\frac{2 \cdot I_1}{\mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_1}} + V_{th1\max} = 1.02V \tag{35}$$

$$CMR- > V_{GS1} + V_{DSsat_5} \rightarrow V_{DSsat_5} \approx (CMR-) - V_{GS1} = 174mV \tag{36}$$

$$\frac{W}{L}_5 = \frac{2 \cdot I_0}{\mu_n C_{ox} \cdot \left(V_{DSsat_5}\right)^2} = 8.5 \tag{37}$$

In Equation (29), the relationship between the location of the zero and the gain bandwidth product was shown. Expanding that equation gives the result shown in Equation (38).

$$z = 10 \cdot GBW \rightarrow G_{m2} = 10 \cdot G_{m1} \tag{38}$$

Therefore, $G_{m2} = g_{m6} = 3.1$mS. As before, the size of Q6 can be determined from g_{m6}.

$$\frac{W}{L}_6 = \frac{g_{m6}}{gm_4} \frac{(g_{m1})^2}{2 \cdot I_O \cdot \mu_n C_{ox} \cdot (V_{GS} - V_{th})} = 22.5 \tag{39}$$

In Figure 30, transistors Q3, Q4, and Q6 are current mirror transistors. Q3 and Q4 form a matched current mirror pair and the gate of Q6 is connected to its gate. Consequently, an approximate relationship between the V_{DS} voltages of these transistors can be expressed by Equation (40).

$$V_{SD_3} \approx V_{SD_4} \approx V_{SD_6} \tag{40}$$
$$V_{SG_3} \approx V_{SG_4} \approx V_{SG_6}$$

The approximate expressions from Equation (40) can be exploited to give an expression that can be used to determine dimensions of Q6.

$$\frac{\left(W/L\right)_6}{\left(W/L\right)_4} = \frac{g_{m6}}{g_{m4}} \tag{41}$$

$$g_{m4} = \sqrt{2 \cdot \mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_4 \left(\frac{I_O}{2}\right)} = 0.037mS \tag{42}$$

$$\left(W/L\right)_6 = \frac{g_{m6} \cdot \left(W/L\right)_4}{g_{m4}} = 100 \tag{43}$$

Finally, the size of transistor Q7 can be determined by comparing the current flowing through Q6 and Q4.

$$\frac{\left(W/L\right)_6}{\left(W/L\right)_4} = \frac{I_6}{I_4} \Rightarrow I_6 = \frac{I_4 \cdot \left(W/L\right)_6}{\left(W/L\right)_4} = 1.1mA \tag{44}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_6}{I_5} \cdot \left(\frac{W}{L}\right)_5 = 360 \tag{45}$$

The final circuit schematic of the error amplifier is shown in Figure 33, and its frequency response is shown Figure 34.

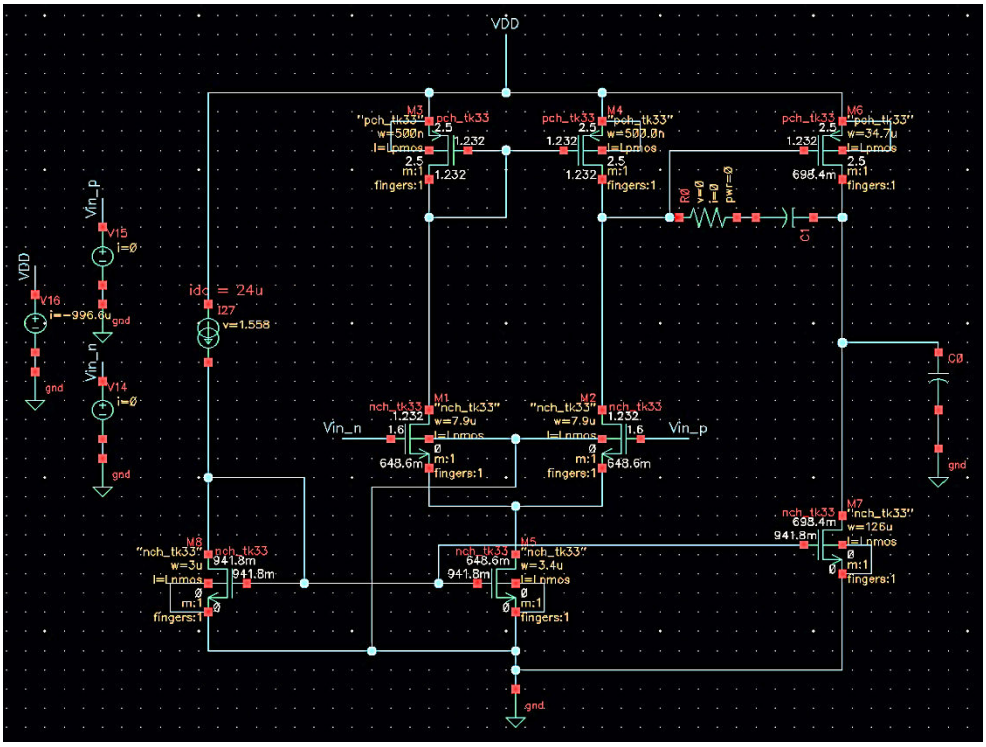


Figure 33 Error amplifier schematic in Cadence

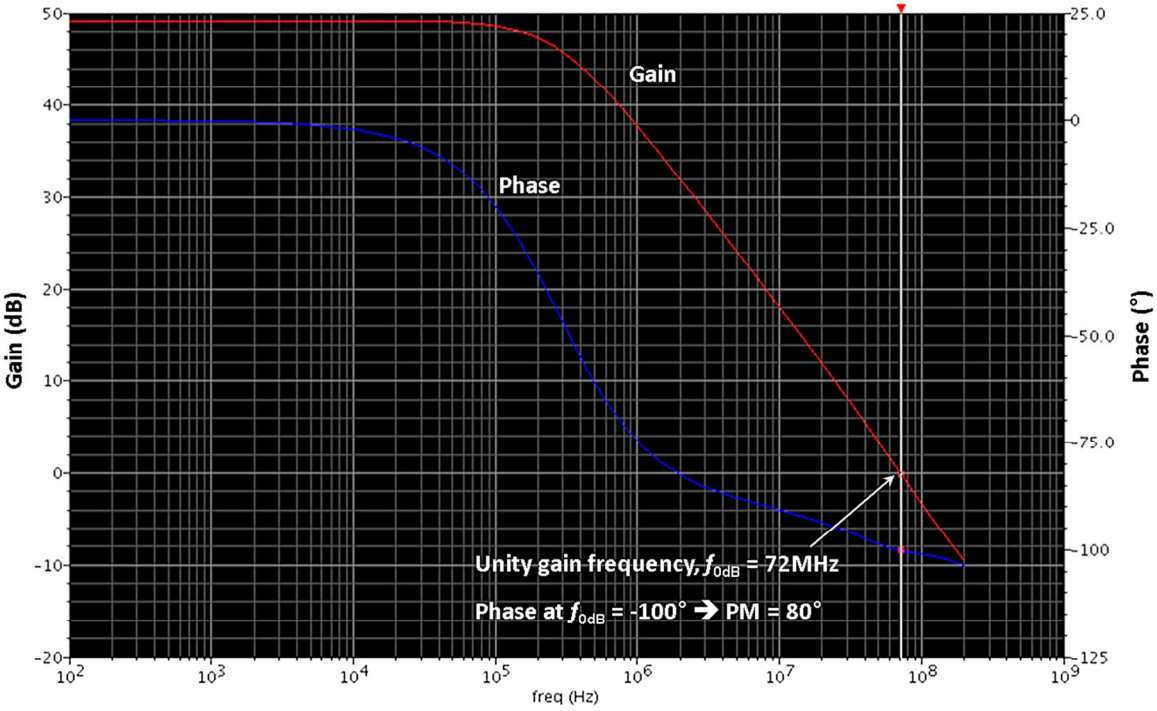


Figure 34 Frequency response of error amplifier

At DC, the gain of the error amplifier is approximately 50dB and the unity gain frequency is 72MHz, at which it as 80° of phase margin.

4.2.4 Biasing Network with Start-Up Circuit

A reference circuit is required to bias the error amplifier. To this end, a self-biasing threshold-reference circuit is used. The circuit schematic is shown in Figure 35. This circuit is commonly used to generate a stable reference current that is dependent on the MOSFET's threshold voltage. An advantage of this type of circuit is that the threshold voltage is relatively insensitive to variations in the supply voltage. From [33], it is shown that the fractional change in the bias current from a fractional change in the supply voltage for this type of current reference circuit is approximately 0.045 (assuming V_{TH} = 1V, $V_{GS} - V_{TH}$ = 0.1V, and current mirror is ideal).

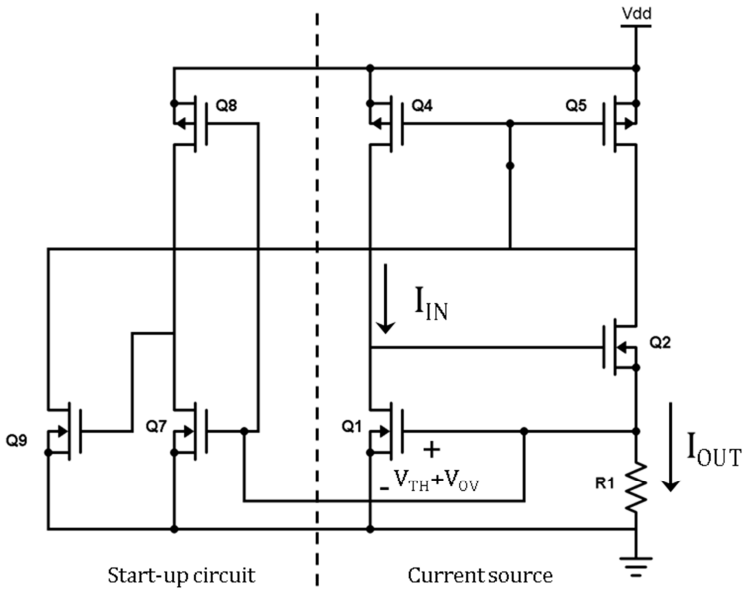


Figure 35 Self-biasing V_{th} reference circuit with start-up circuit

This reference circuit serves two functions. Firstly, the circuit generates a reference current through the resistor R_1. From [33], it is shown that the output current can be expressed by Equation (39).

$$I_{OUT} = \frac{V_{GS1}}{R_1} = \frac{V_{th} + V_{ov1}}{R_1} = \frac{V_t + \sqrt{\frac{2I_{IN}}{k_n \left(\frac{W}{L}\right)_1}}}{R_1} \tag{46}$$

As long as the overdrive voltage of Q1 is kept small, Equation (46) shows that the output reference current is dependent primarily on the threshold voltage of Q1 and the accuracy of resistor R_1. The start-up circuit utilizes self-biasing, in which the input and output currents are made to be dependent on each other [33]. This greatly reduces the power-supply sensitivity of the circuit and prevents the circuit from "getting stuck" in a zero-current state, as illustrated in Figure 36.

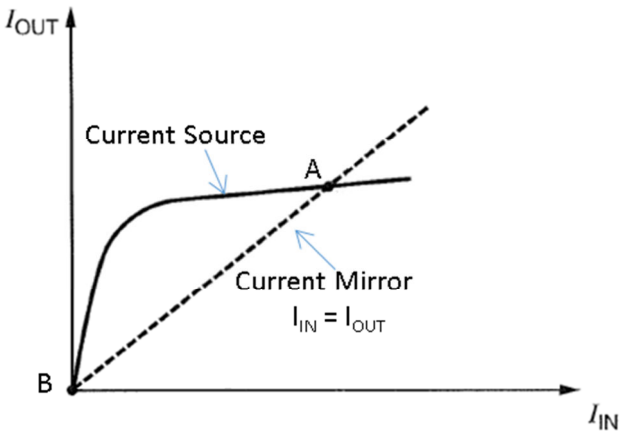


Figure 36 Operating point of self-biased reference circuit (reproduced from [33])

The biasing circuit consists of two sub-circuits, the current mirror formed by Q4 and Q5, and the current source formed by Q1, Q2, and R_1. If the current mirror transistors are well matched and operating in saturation mode, the input and output currents are essentially equal (I_4

= I_5 = I_{IN} = I_{OUT}). The current source, however, will generate a stable output current for a range of input currents as long as all the transistors remain in saturation. Consequently, from Figure 36, the circuit must obey both conditions, and therefore the circuit will operate at either point A or point B. However, it is possible that the circuit can operate in a "zero-current" state, point B. Therefore, the self-biasing start-up circuit is utilized to prevent this from happening.

The start-up circuit is composed of transistors Q7, Q8, and Q9. It is shown in Figure 35 that Q7 and Q8 form a CMOS inverter, the input and output of which are connected to the gates of Q1 and Q9, respectively. If the current source reaches the "zero current state", then Q1 will no longer operate in the saturation mode. Consequently, this causes the gate-source voltage of Q1 to drop and therefore, the input to the CMOS inverter will be low. The output of the inverter will become high and turn on Q9. The drain of Q9 is connected to the gates of current mirror transistors Q4 and Q5. The increased voltage across Q9 lowers the gate voltage of Q4 and Q5 causing them to return to saturation mode and generate the output current [33]. It is important to make sure that the start-up circuit does not interfere with operation of the current source circuit. Consequently, it is necessary to ensure that Q9 is completely turned off when the current source is operating correctly. Therefore, during steady state, the output of the CMOS buffer must be low enough to completely turn off Q9, which can be accomplished by making the aspect ratio of Q_7 to be much larger than Q_8 [33].

Figure 37 shows the completed current reference circuit with the corresponding start-up circuit. The resistor chosen to be 26.6kΩ, which generates a 33.9μA reference current.

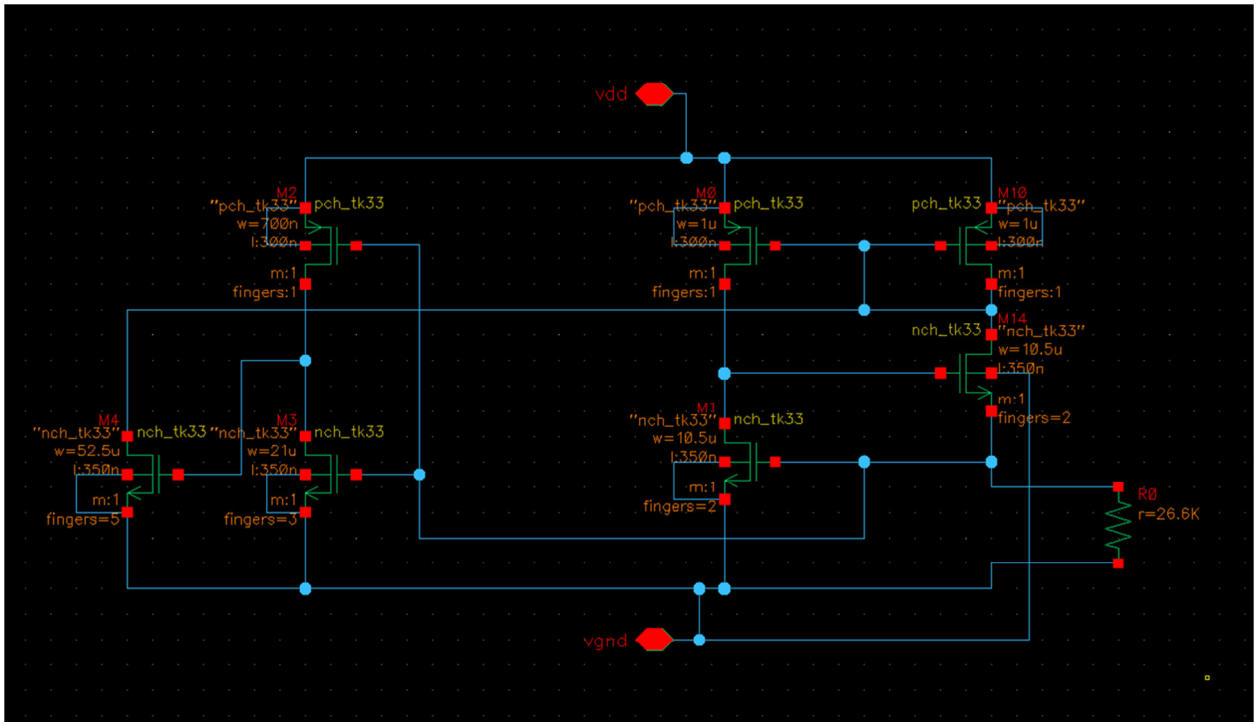


Figure 37 Current reference with start-up circuit

4.2.5 Sampling Network

Resistors R_1 and R_2 form a voltage divider that provides the error amplifier with the sampled output voltage. The resistor values are selected such that, at steady state, the input to the positive terminal of the error amplifier matches the reference voltage. The reference voltage is chosen to be 1.3V, which is the input common mode voltage that results in the most gain. Consequently, for V_O = 1.8V, R_1 = 5kΩ and R_2 = 12kΩ. The quiescent DC current flowing through this sampling network is approximately 106μA. For simplicity, the reference voltage for the error amplifier is provided externally from an off-chip voltage source.

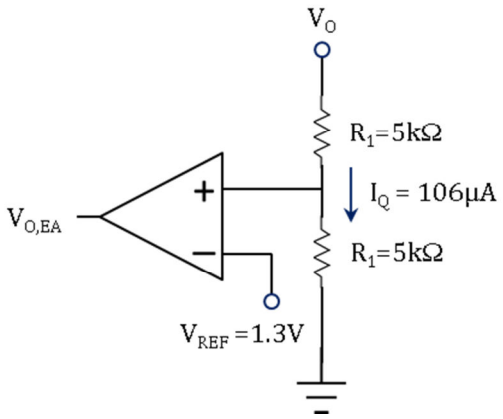


Figure 38 Voltage divider used for output sampling

4.2.6 Output Buffers

The schematic of the output buffer is shown in Figure 39. Each buffer consists of a chain of six inverters. The output of the buffer is terminated by a 50Ω load resistor through a 50Ω transmission line on the PCB. The dimensions of the NMOS and PMOS transistors for each stage are given in Table 15.

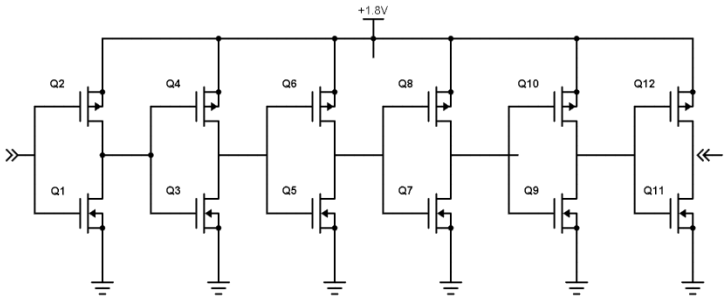


Figure 39 Buffer schematic

Table 15 Transistor widths for each inverter stage

Stage	NMOS width	PMOS width
1	4.2 μm	8.4 μm
2	8.4 μm	16.8 μm

3	16.8 µm	33.6 µm
4	33.6 µm	67.2 µm
5	67.2 µm	134.4 µm
6	134.4 µm	268.8 µm

Six inverter stages were selected so that the buffer could source the desired amount of current from the voltage regulator. In the high state, each buffer sources approximately 18mA of supply current. Six buffers are connected to the output of the voltage regulator. Consequently, a current swing of 108mA can be achieved by toggling all the buffers at once. The time domain simulation of the output voltage of a single buffer and supply current sourced by all six buffers is shown in Figure 40 when powered by an ideal 1.8V supply.

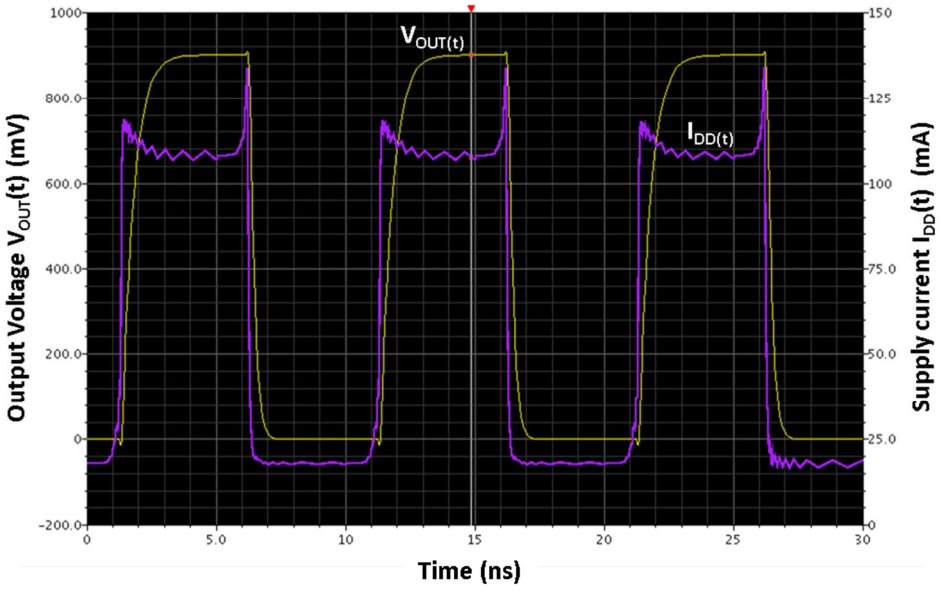


Figure 40 Output voltage of a single buffer and total supply current sourced by all six buffers

4.2.7 System Simulation

Figure 41 shows the load regulation performance of the LDO, which characterizes the LDO's ability to maintain the desired output voltage under varying load conditions.

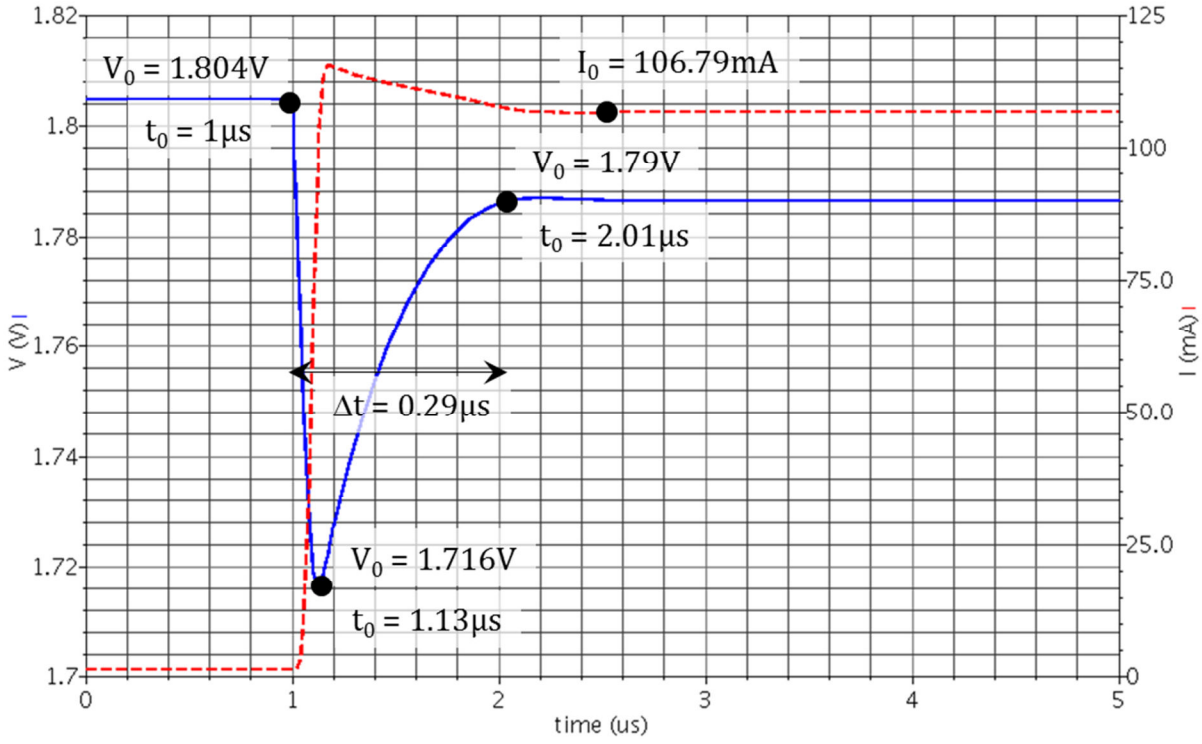


Figure 41 Output load voltage regulation of LDO corresponding to a 107mA load current step

A 107mA load step current is applied and the output voltage droop is shown. The output voltage drops by 17.5mA, which is approximately 0.97% of the nominal regulated voltage and corresponds to a load regulation $\left({}^{\Delta V_O}/_{\Delta I_O}\right)$ of 0.167. The response time of the regulator is approximately 2µs.

The entire system, consisting of the LDO and the buffers, was simulated. In the first simulation, the input voltage to the LDO is provided by a 5 inch long (127mm) microstrip

transmission line. The width of the line is 60 mils (1.52mm) and the substrate is FR4 with ε_r = 4.6 tan σ = 0.025 and substrate height of 10 mils (0.254mm). A 100nF capacitor is placed at the output of the LDO. The eye diagram at the output of the buffers is shown in Figure 42. The input signal is a pseudo-random binary sequence (PRBS) with a length of 1024 bits at 500Mbps.

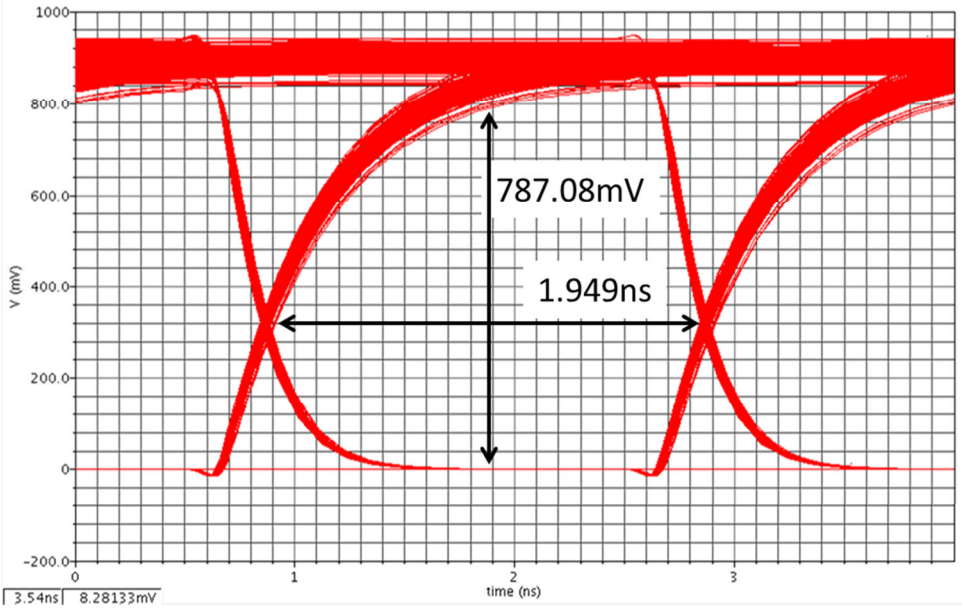


Figure 42 Eye diagram with 500Mbps PRBS-10 input with LDO powered by PTL

The power supply noise, measured at the output of the LDO, is shown in Figure 43. The maximum peak-to-peak voltage swing is approximately 87.7mV, which is approximately 5% of the nominal power supply voltage of 1.8V.

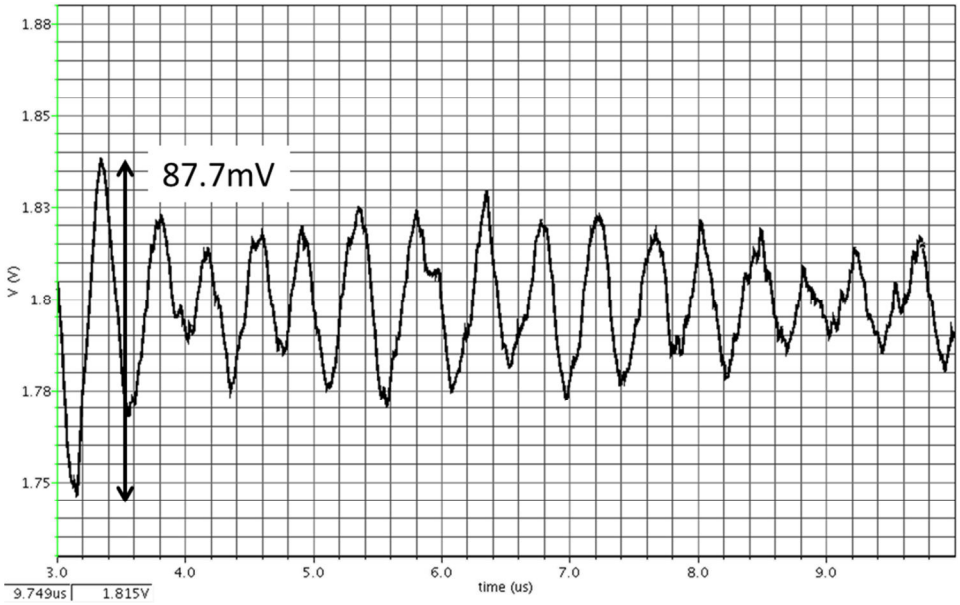


Figure 43 Power supply noise with 500Mbps PRBS-10 input to all six buffers

In the previous simulation, the PTL had a characteristic impedance of 25Ω. When the PTL is terminated, the result of the simulations is shown in Figure 44.

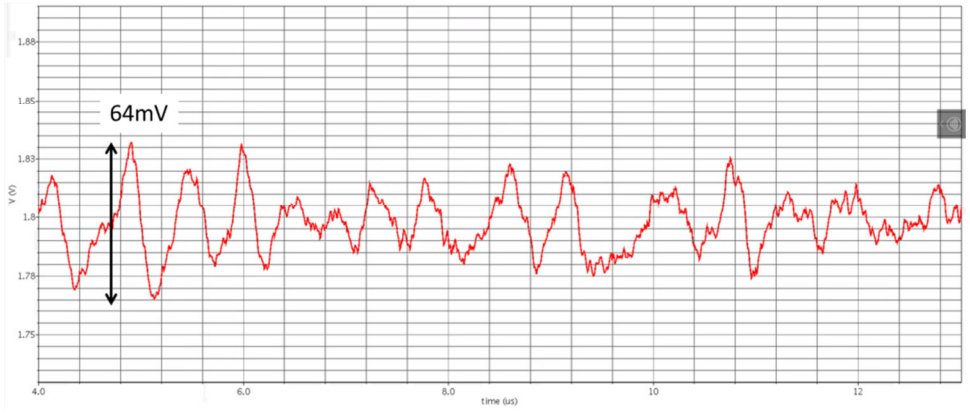


Figure 44 Power supply noise with terminated PTL

One can see that the presence of the termination reduces the amount of power supply noise seen by the buffers. By terminating the PTL, the amount of voltage fluctuation on the PTL is reduced, as shown in previous sections. In addition, the LDO serves to isolate the system power supply, V_S, and the V_{DD} node. Consequently, the relatively high line regulation, which his defined as the

amount of output load variation due to a an input voltage variation, helps to prevent reflections on the PTL from affecting the power supply voltage.

The regulator circuit was also simulated with the input voltage provided by a power and ground plane. The 3 inch by 3 inch plane model consists of a power plane and a ground plane separated by 10 mils. The substrate properties are the same as that of the transmission line model mentioned above. Again, a 100nF output capacitor is placed at the output of the LDO. The eye diagram is shown below with the same PRBS-10 input pattern in Figure 45 along with the power supply noise at the output of the LDO in Figure 46.

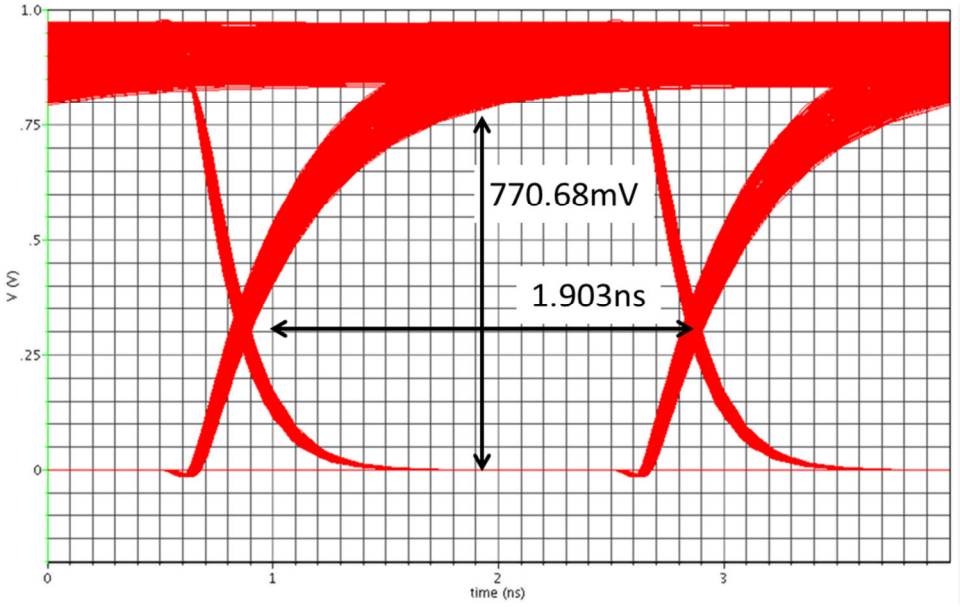


Figure 45 Eye diagram with 500Mbps PRBS-10 input with LDO powered by power plane

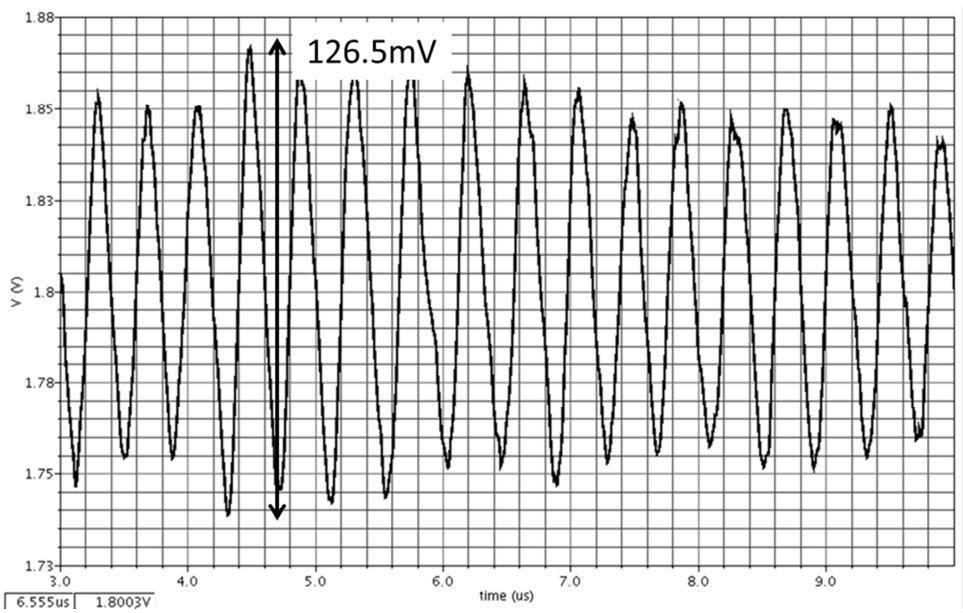


Figure 46 Power supply noise with 500Mbps PRBS-10 input to all six buffers

From the above figures, it can be seen that when the LDO is connected to the power supply voltage through the power transmission line, the circuit shows better performance. The eye height and eye width are increased slightly, but the power supply noise is increased from 87mV to 126.5mV, an increase of 45%.

Figure 47 shows the input/output voltage characteristic of the LDO. The output of the LDO is regulated at 1.8V when the input voltage (V_S) is more than 2.5V. However, operating the input greater than 2.5V means that the lower LDO efficiency.

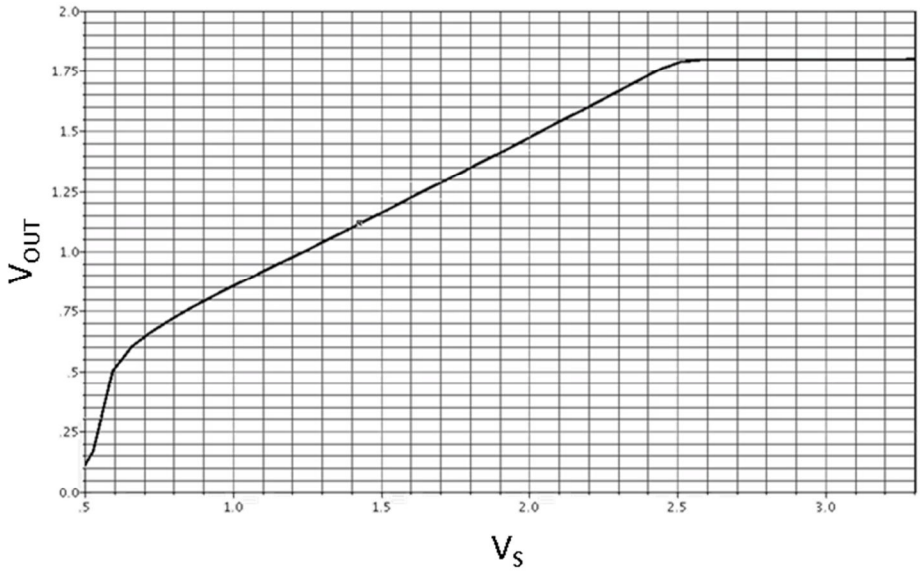


Figure 47 Input/Output voltage characteristic of LDO

4.3 IC Layouts

The layouts of the components used in the LDO circuit are shown in the following sections. As previously mentioned, the transistors used in this design are the 3.3V thick-oxide devices. In addition, all layouts have passed design rule (DRC), and layout versus schematic (LVS) checks.

Pass Transistor

The layout of the pass transistor is shown in Figure 48. The pass transistor was created with 20 interdigitated transistors each with a gate width of 50µm (W_n). This creates a transistor with a total effective gate width of 1mm. The total length (L_{total}) is 18.6µm.

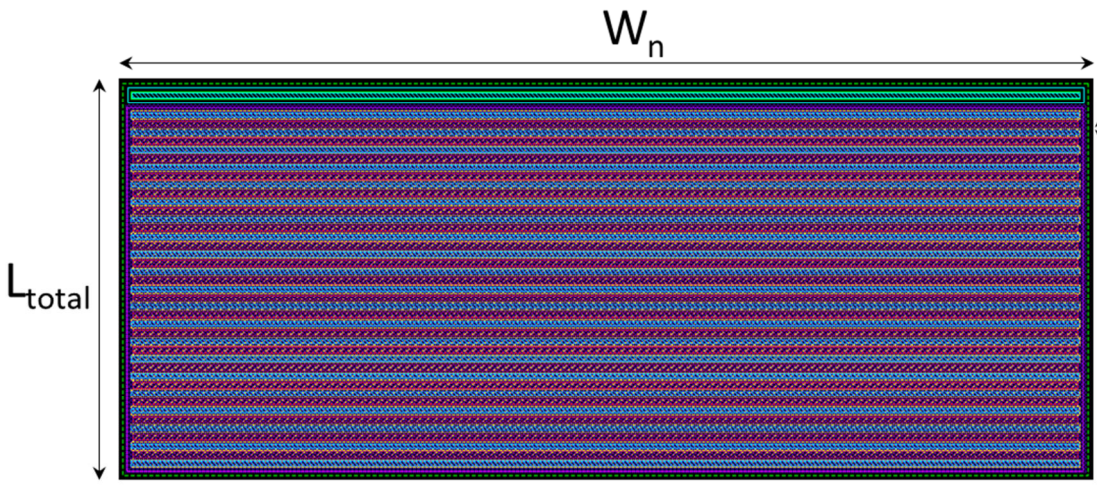


Figure 48 Layout for the 1mm wide PMOS pass transistor

Error Amplifier

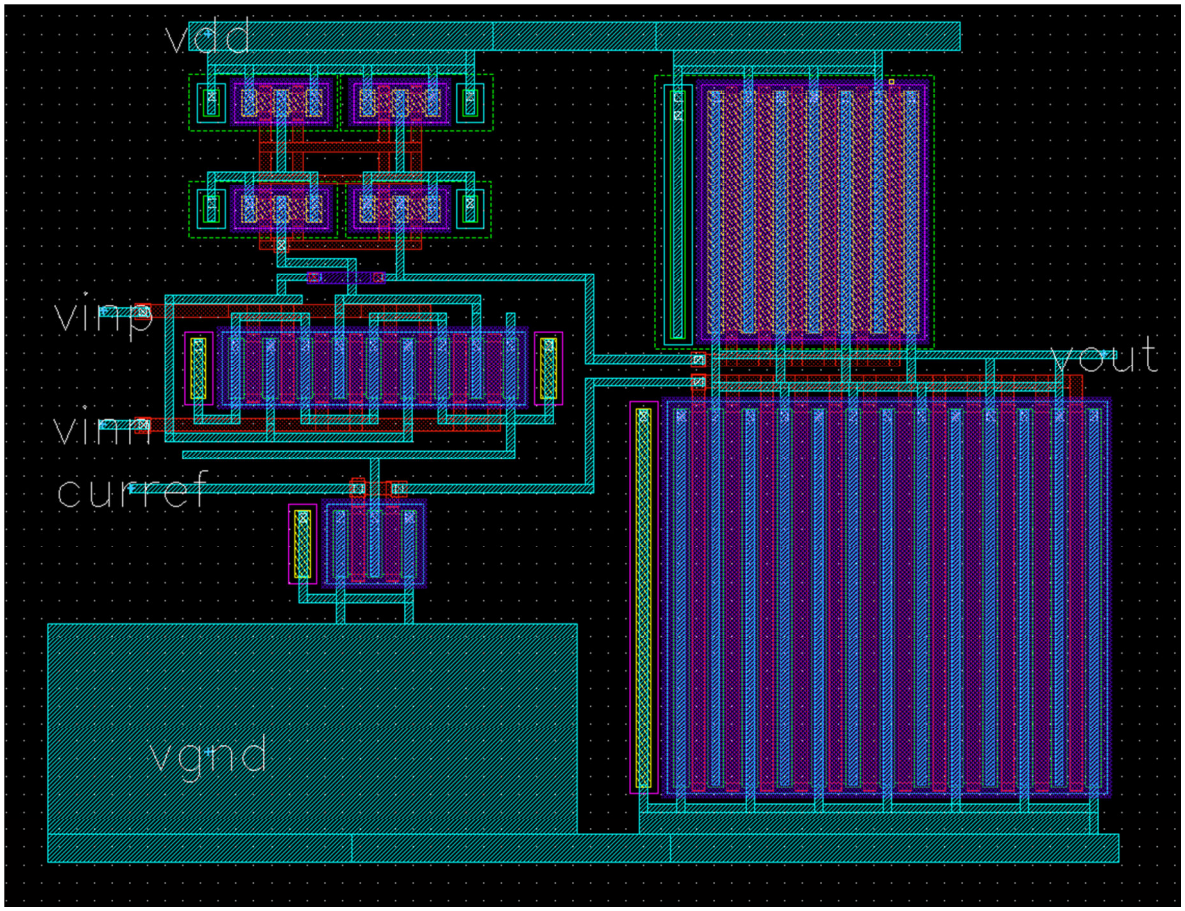


Figure 49 Layout of error amplifier (without current reference circuit)

The differential amplifier layout was accomplished by splitting each transistor into four transistors each and interleaving them. This advantageous in that the layout is less susceptible to process variation and the two differential transistors will have the same effective drain and source area, which leads to better matching.

Current Reference

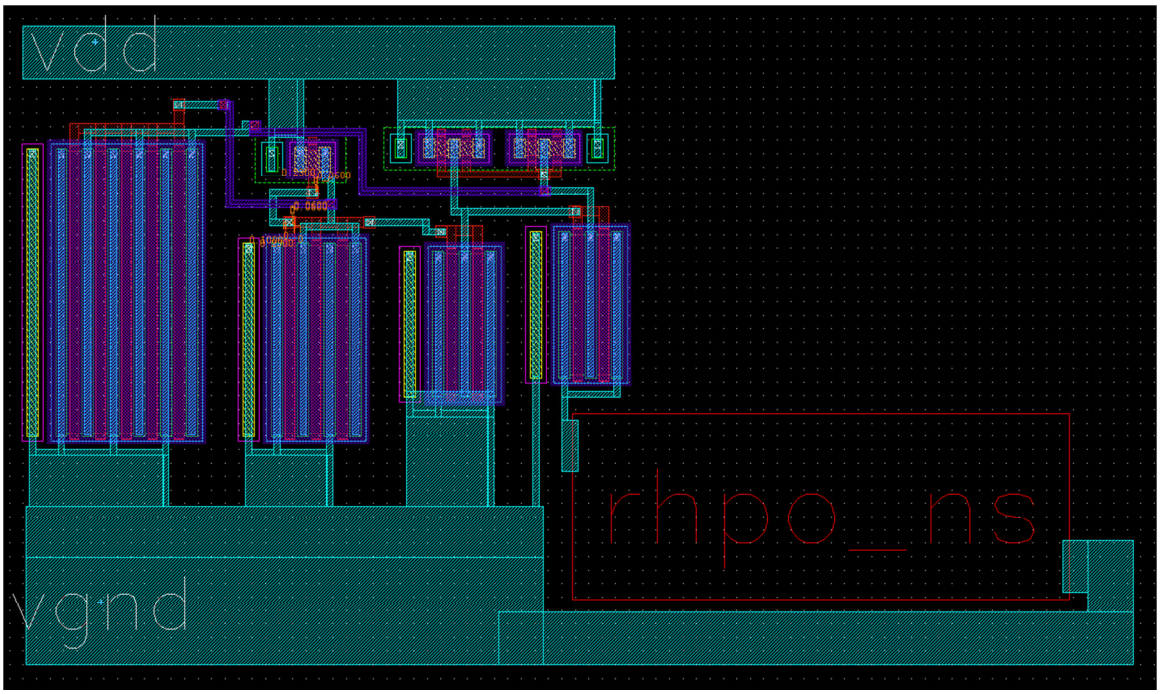


Figure 50 Layout of current reference circuit

Output Buffers

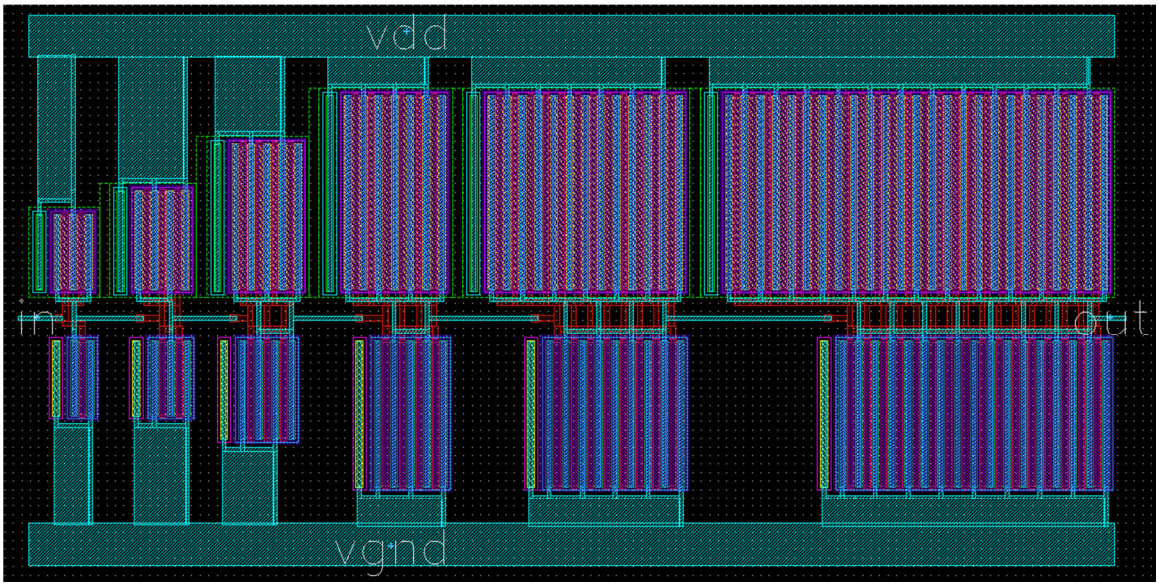


Figure 51 Layout of bufffer circuit

Combined Layout

The layout of the combined circuit is shown in Figure 52. Here, only one buffer is shown, but all six buffers are implemented on the die.

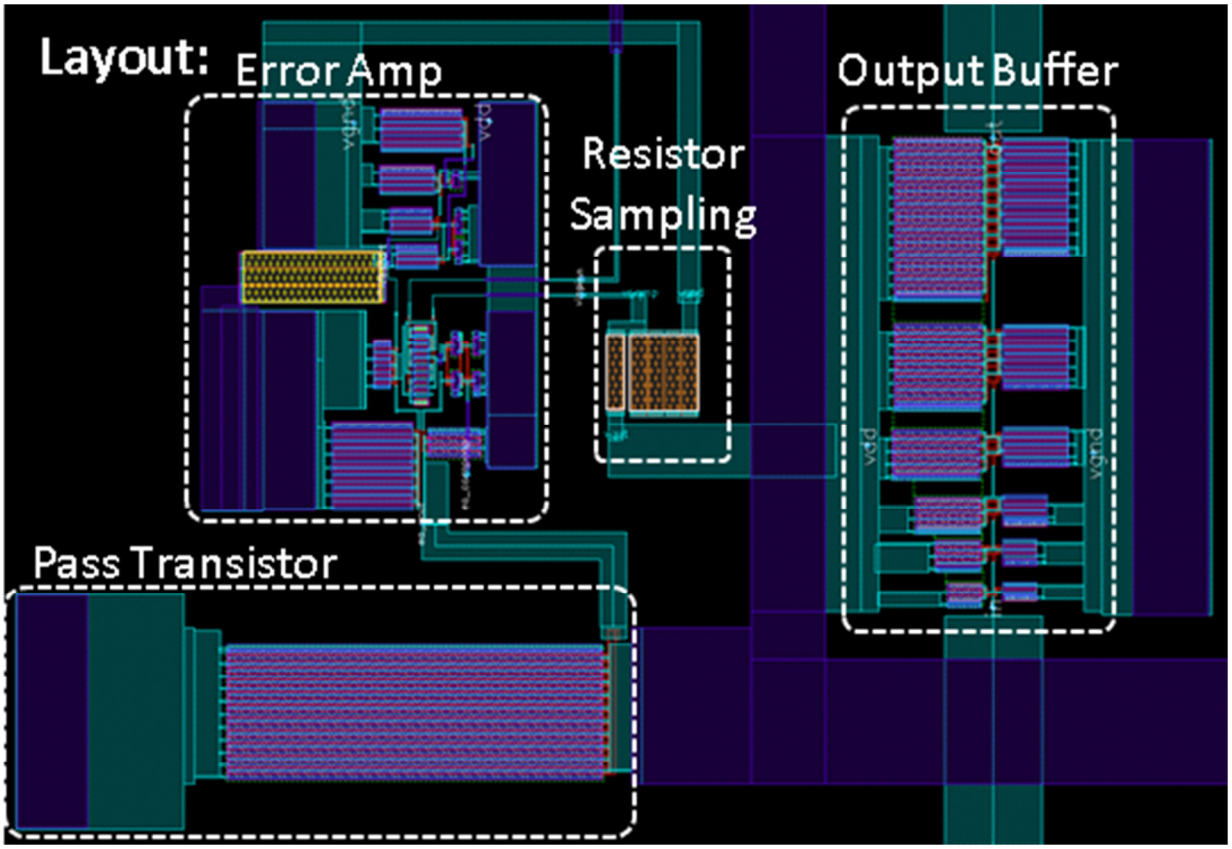


Figure 52 Layout of complete circuit

4.4 Summary

It was shown in the previous sections the advantages of the CV-PTL concept. However, the board-level implementation is somewhat restricted to lower data rates. The PDN drivers, which control the switching network, must be able to switch as fast, or even faster, than the data drivers for proper operation. Also, the switching resistor network can be difficult to scale to a larger number of I/Os. Consequently, in this chapter, an integrated circuit solution is presented that functions similar to the CV-PTL concept. In this implementation, a power supply connects to the input of the low dropout regulator via a power transmission line implemented on the PCB. The LDO powers a set of digital buffers, both of which are implemented on chip. The chip was designed and will be fabricated with a 0.18µm CMOS process to verify this scheme on an IC

scale. The design was simulated and compared with the LDO being powered via a power and ground plane and the PTL-based PDN showed improved eye height, eye width, and lower power supply noise. The IC design was submitted for fabrication in August 2014, and is expected to be returned for measurement in March 2015. Due to time these constraints, lab measurements have not yet been conducted on the fabricated chip.

CHAPTER 5: MIXED SIGNAL NOISE ISOLATION

5.1 Introduction

The previous chapters discussed a PDN design based on the notion of powering a digital circuit through a power transmission line instead of power and ground planes. It was shown through theory and lab measurements that this method can reduce power supply noise and consequently improve the output signal quality. This chapter will build upon those results and will address another important issue in mixed signal circuits, namely, noise coupling between digital and RF components. Currently used methods, such as electromagnetic bandgap structures show excellent noise isolation characteristics at wide bandwidths, and are a popular area of research. However, these structures can pose difficulties for signal integrity by increasing the noise at the power supply pin. In this chapter, a simple method for power delivery design for mitigating the coupling of power supply noise in mixed-signal electronics is presented. The method, which uses a bandstop filter embedded in the power transmission line can isolate the amount of coupled noise between the digital and RF supply voltage pins. In addition, it is shown that utilizing a terminated power transmission line can also improve noise isolation. Test vehicles using the proposed methods are fabricated and tested and compared with regards to power supply noise, jitter, and noise isolation compared to an electromagnetic bandgap (EBG) structure.

5.2 Noise Isolation Methods

Power distribution is a difficult challenge for engineers working in mixed signal systems, such as smartphones and other low power applications. The trend toward lower supply voltages, higher clock frequencies, tighter power constraints, and limited board/die area leaves designers

with ever-decreasing margins for maintaining power integrity. Furthermore, in emerging technologies, such as system-on-chip (SoC) or system-on-package (SoP), disparate circuit blocks are integrated together onto the same die or package, thus further complicating the issue. In these complex mixed signal systems, the isolation of supply noise between sensitive circuit blocks is crucial.

The nature of digital circuitry cause digital supplies to be inherently noisy. The switching noise generated by large current transients of digital devices, if injected into the supply rail of sensitive RF components, can lead to significant reduction in performance. Several methods can be used to mitigate the noise coupling, as shown in Figure 53.

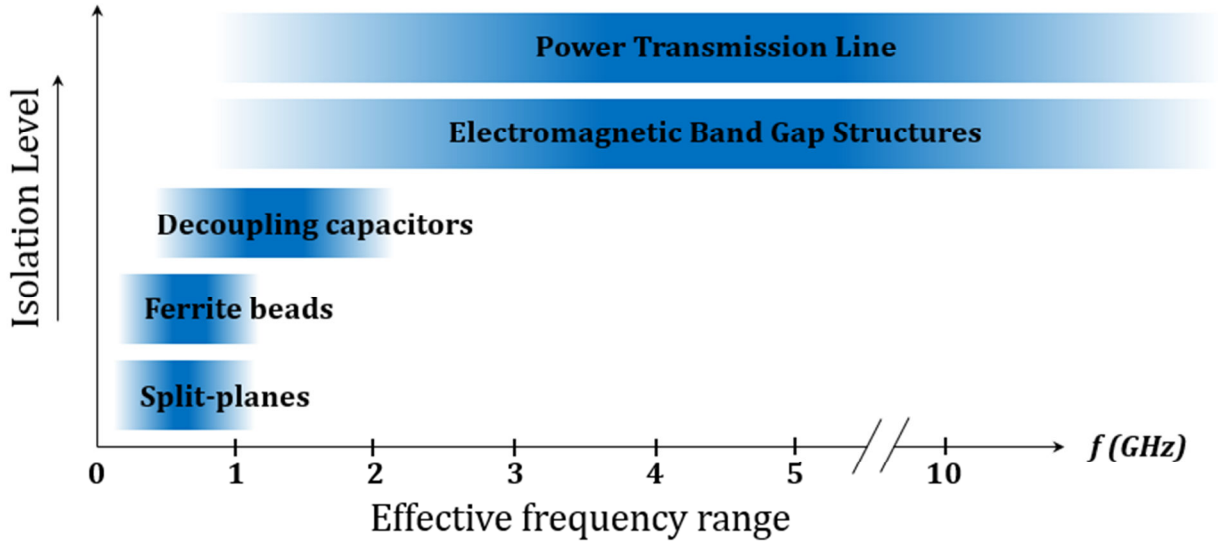
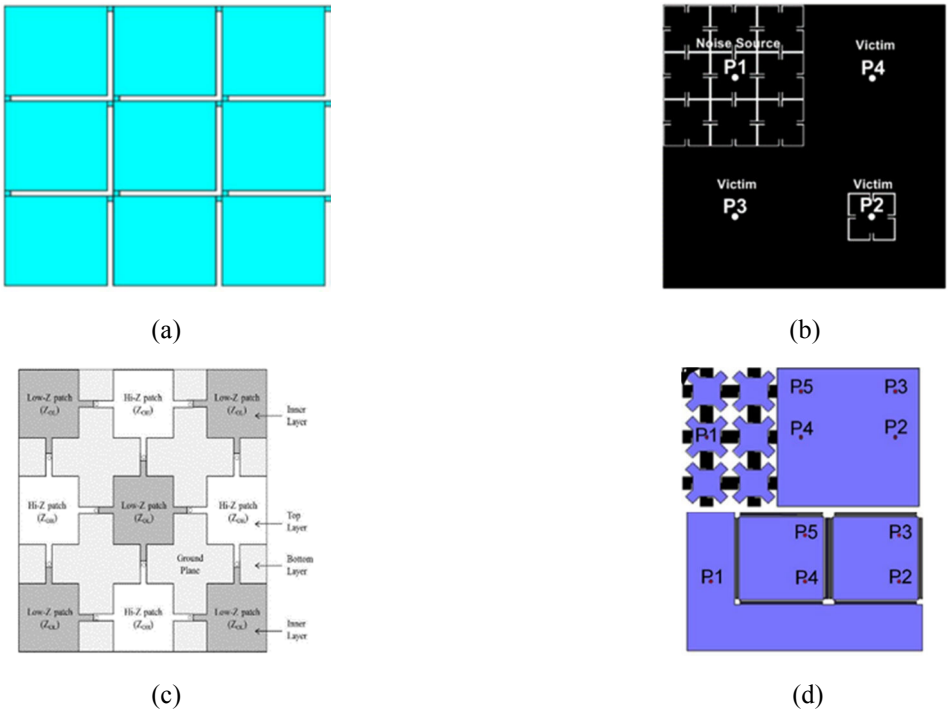


Figure 53 Effective frequency range of several noise isolation techniques

The most common methods are to use ferrite bead EMI filters, split planes, or electromagnetic bandgap structures. However, ferrite bead inductors have maximum isolation frequencies of only several hundred megahertz [16]. Also, the inherent resistance of ferrite beads produces additional ohmic loss. Split planes can also be used to create separate digital and analog voltage/ground planes. However, great care must be taken to choose the location of the split plane since this can lead to return current discontinuities [5]. As discussed previously,

decoupling capacitors can be used to suppress power supply noise, but are only effective up to ~1-2GHz due to parasitic inductance from the package.

Electromagnetic bandgap (EBG) structures, sometimes referred to as high-impedance surfaces, are a popular topic of research in this area. EBGs are composed of an array of periodic metal patterns, the geometry of which can be altered and optimized to exhibit a desired frequency response to act as a distributed filter. With careful design, EBGs can demonstrate very good noise isolation characteristics. In addition, one of the strengths of EBGs is its flexibility in design. Many different geometries and configurations have been presented in recent research literature.



(a) (b)

(c) (d)

Figure 54 Examples of EBG geometries; (a) Uniplanar EBG [21], (b) partial EBG placement [35] (c) multi-player stepped impedance EBG [36], (d) separate EBGs on power and ground layers [37]

The most common configuration is uniplanar EBGs, which have been shown to achieve greater than 50dB of isolation, as shown in [21] and [38, 39]. In [35], a design is presented that has partial placement of EBG cells placed near only noise sources and noise sensitive components. In [36], a wide bandwidth multi-layer alternating impedance EBG design is shown that achieves 40dB of isolation up to 20GHz. In [37], two EBG structures are placed on both the power and ground planes, and both work in tandem to suppress noise coupling. In [40], it is shown that an alternating impedance electromagnetic bandgap (AI-EBG) structure-based power delivery network can be used to effectively suppress unwanted noise coupling in a mixed-signal system. These are just a few examples that demonstrate the versatility and design flexibility of EBGs.

However, because these structures are generally composed of meandering lines, vias, and irregular shapes, EBGs are generally not well suited for supporting good signal quality. The work in [41] and [42] shows that referencing a signal trace to an EBG can lead to reduced signal quality, for both single and differential-ended signaling. Even if the signal lines are referenced to a solid ground plane, the presence of the EBG can significantly increase the noise at the source due to increased PDN impedance.

The focus of the work shown here is to demonstrate a technique based on transmission line theory that is simple to implement, has better noise characteristics than EBG, can reduce layer count, and is especially suitable for low power applications where space is a constraint. This method, based on the power transmission line (PTL), addresses both power supply noise generation and isolation, unlike EBG structures, which are designed specifically for noise isolation purposes only. It was shown in the previous chapters that a PTL-based PDN strategy can result in lower power supply noise generated at the digital supply pins [11, 17, 19]. In [43] and [44], it has been shown that a filter embedded in the PTL can help reduce the noise coupling between the digital and RF blocks.

It is shown in the subsequent sections that lower power supply noise, better signal quality, as well as good noise isolation can all be achieved by using a PTL based PDN. In

addition, it is shown that a variation of the PDN without the filter can also be used effectively. This paper will compare, through conceptual and experimental results, the effectiveness of using this PTL based PDN strategy.

5.3 Noise Isolation using SSN filter

Before discussing the proposed noise isolation strategy, consider the scenario presented in Figure 55. A set of digital I/O buffers and an RF low noise amplifier are connected to a common power delivery network. When the buffers are switching, the frequency spectrum of the generated power supply noise will contain many harmonics that are dependent on the input data pattern. In this work, the input is a clock signal, so the harmonics occur at integer multiples of the fundamental clock frequency (ideally consisting of only odd integer harmonics). If the noise harmonics fall within the operating bandwidth of the low noise amplifier (LNA) and no precautions are in place for noise isolation, then the coupled noise will appear at the RF output.

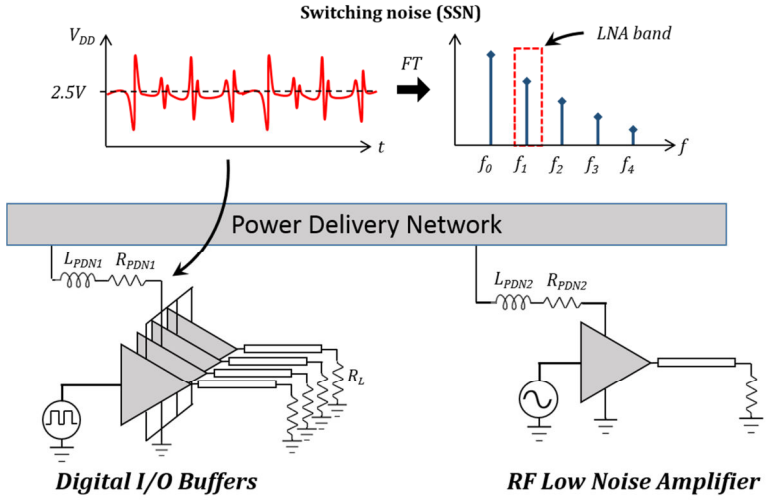


Figure 55 Power supply noise coupling

A proposed technique is shown in Figure 56. A common supply voltage powers both digital and RF circuitry via a PTL.

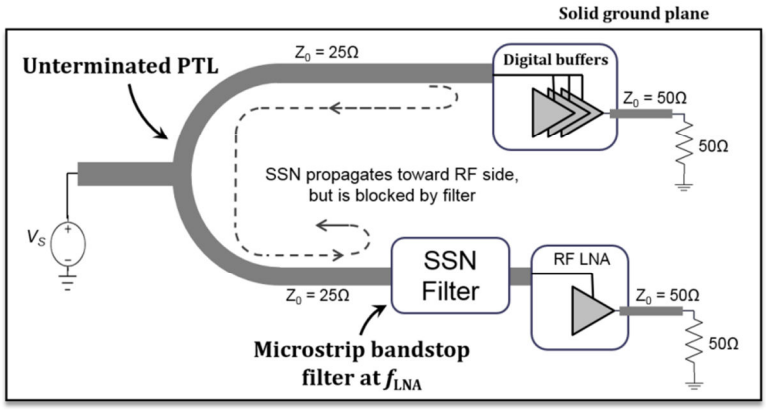


Figure 56 Mixed signal noise isolation concept showing the use of the SSN filter.

In Figure 56, a bandstop filter is placed in the supply path of the LNA. The stop band of this filter covers the operating bandwidth of the LNA and serves to attenuate the digital switching noise from propagating between the two circuits. It should be noted that for this method, the PTL is not source terminated and there is a solid ground plane below the signal layer.

5.4 SSN Filter Simulation

Simulations were performed to demonstrate the viability of this concept in Agilent Advanced Design Systems (ADS) [45]. The LNA used in the simulation is a simple common-gate configuration operating at a center frequency of 2.4GHz with V_{DD} = 2.5V [46]. At 2.4GHz, the gain of the amplifier is approximately 11.95dB.

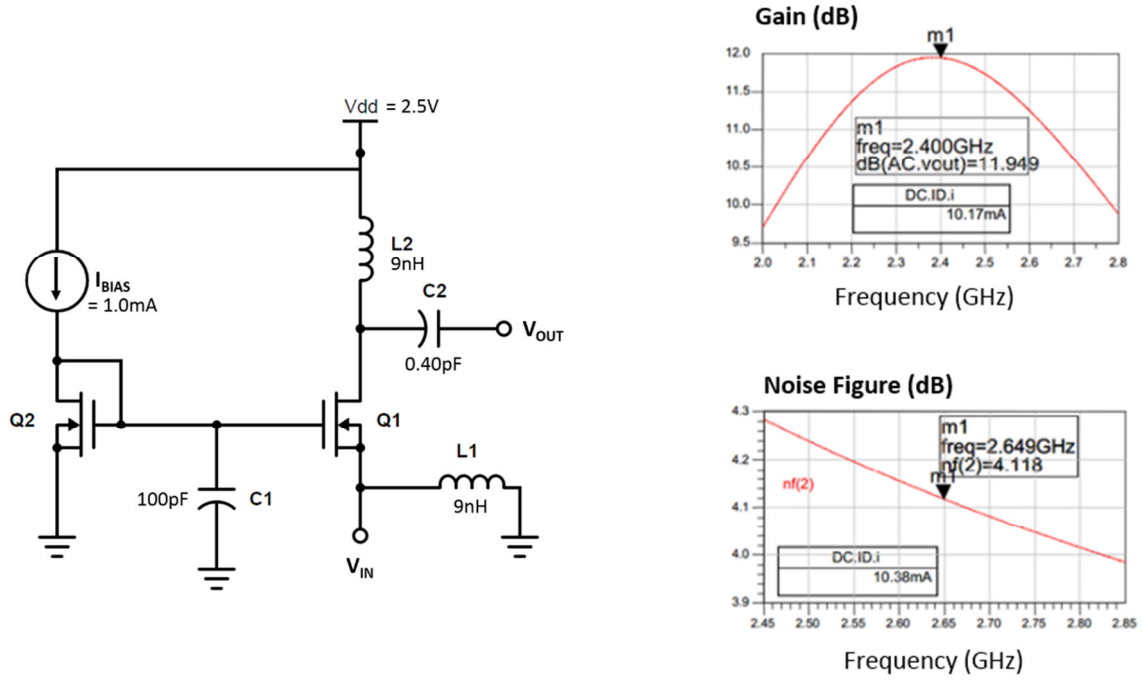


Figure 57 RF LNA used in simulations

A 10Ω power transmission line serves as the PDN and four 2.5V CMOS buffers are operating with a 1.2Gbps PRBS-8 input, in the configuration shown in Figure 58. Figure 59 shows the power spectrum of the noise generated at the V_{DD} node of the buffers.

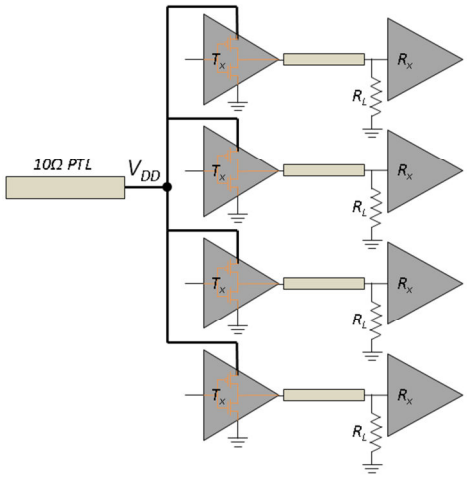


Figure 58 Configuration of bufffers and PTL in simulation

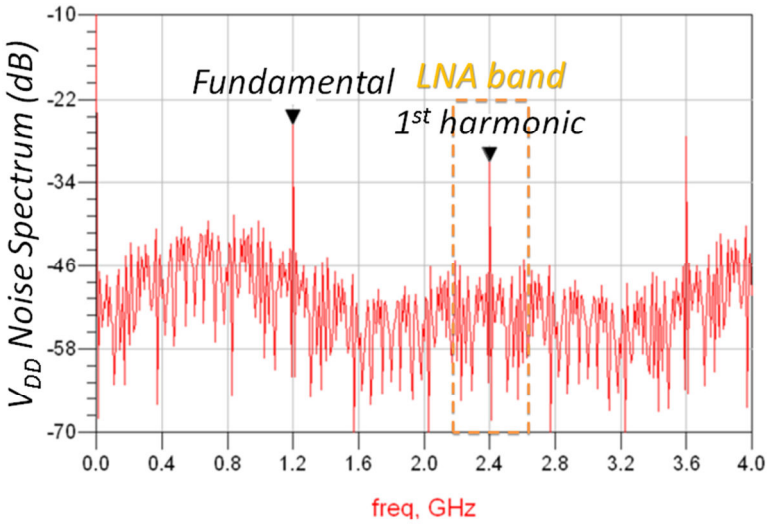


Figure 59 Spectrum of power supply noise

Most of the switching noise generated by the digital buffers will be concentrated at the switching frequency, 1.2GHz. However, there will also be noise generated at the 1st harmonic, 2.4GHz. This corresponds to the operating frequency of the LNA, so any coupling between the two devices will cause noise to show up at the output of the LNA. In the subsequent simulations, the SSN filter is a 3rd order transmission line stub filter that is optimized to give a stop-band response at 2.4GHz [47] with very high insertion loss. This will prevent the noise at 1st harmonic of the SSN from coupling into the RF output. The circuit is simulated under various conditions, which are summarized below.

Case 1: Digital buffers are OFF, RF LNA is ON

This is the control case, in which no input signal is applied to the digital buffers and there is a -50dBm signal at the input to the LNA. As expected, there is a -41dBm signal at 2.4GHz due to the gain of the LNA.

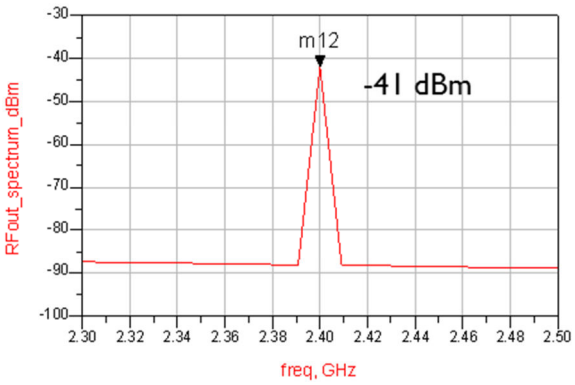


Figure 60 Frequency spectrum of LNA output

Case 2: Digital buffers are ON, RF LNA is OFF; no SSN filter

Figure 61 and Figure 62 show the noise voltage at the supply node of the buffers and the LNA, respectively. In this case, even without an input signal to the LNA, there is an output signal at the desired frequency band, as shown in Figure 63. This is due to the switching noise from the digital circuits that is coupling into the supply node of the LNA.

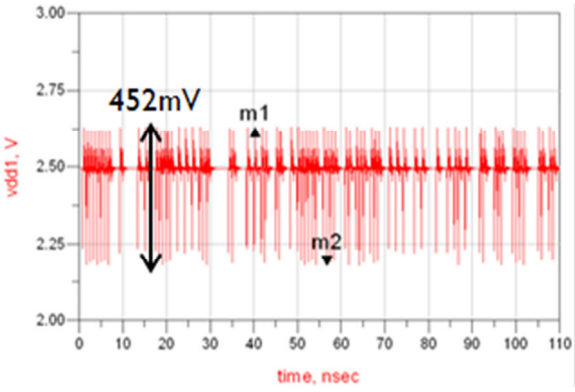


Figure 61 Digital supply noise

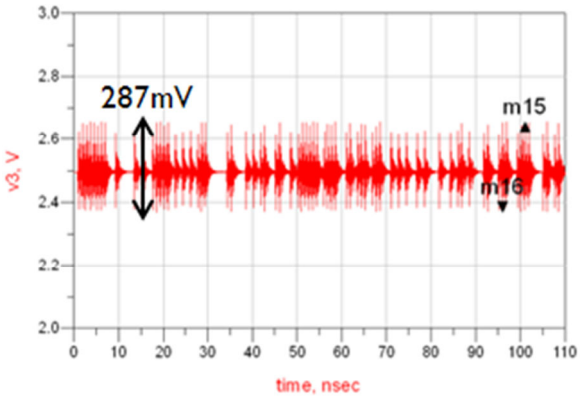


Figure 62 RF supply noise

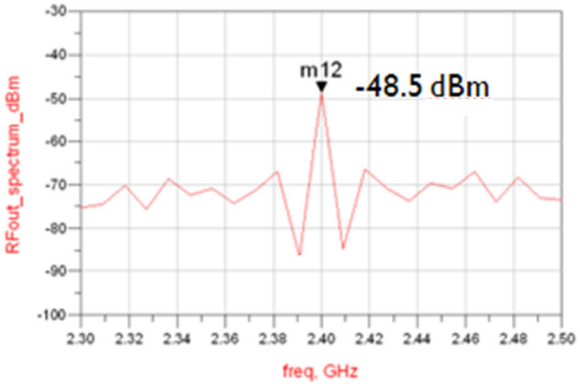


Figure 63 LNA output spectrum at 2.4 GHz

Case 3: Digital buffers are ON, RF LNA is OFF with SSN filter

In this case, a 3rd order Chebyshev transmission line notch filter [47] is placed in the supply path of the LNA. The filter has a very high insertion loss at 2.4GHz, as shown by its frequency response in Figure 64.

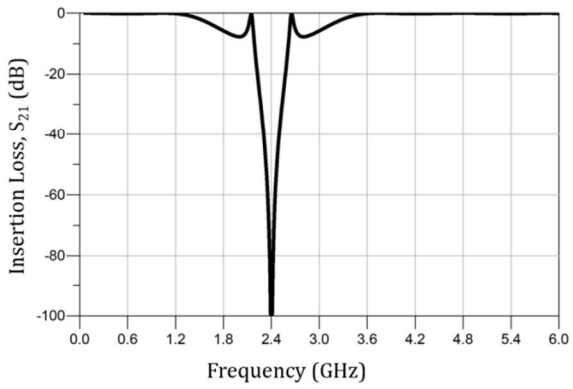


Figure 64 Frequency response of 2.4GHz bandstop filter

Consequently any supply noise generated by the digital circuitry at the bandstop frequency is highly attenuated and does not propagate to the output of the LNA, as shown in Figure 67. Notice that the peak-to-peak supply noise that is generated by the digital circuits is approximately the same with and without the presence of the notch filter (Figure 65 and Figure 61, respectively). Consequently, the filter helps provide isolation between the two circuits, but does not contribute additional noise. In addition, although the supply noise from other frequencies may couple into the LNA, these signals can generally be filtered out further down the receiver chain in a real system.

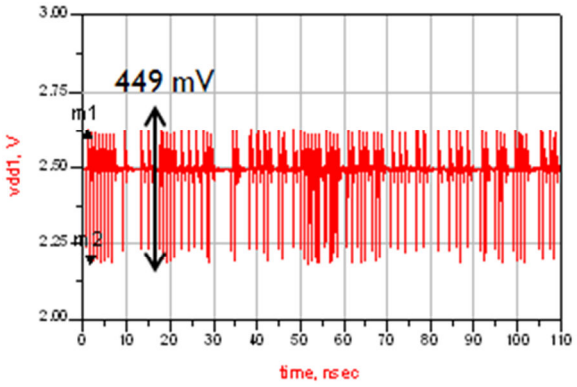


Figure 65 Digital supply noise

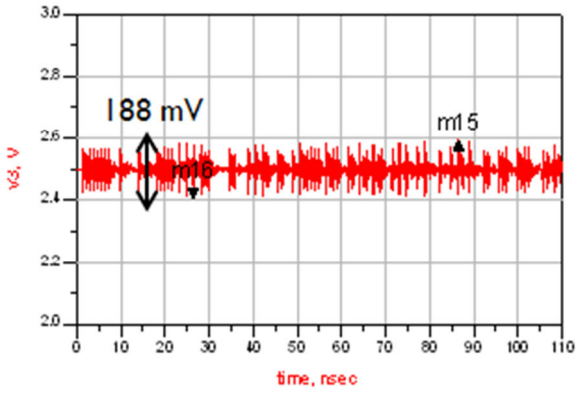


Figure 66 RF supply noise

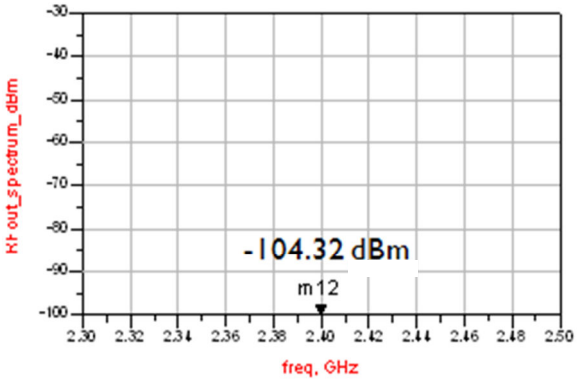


Figure 67 LNA output spectrum

Case 4: Digital buffers are ON, RF LNA is ON; no SSN filter

In this case, both the digital and RF sections are operating simultaneously. Consequently, there is significant noise at the supply node of the LNA and the in-band noise is being coupled into the output of the LNA, as shown by the larger than expected output in Figure 70.

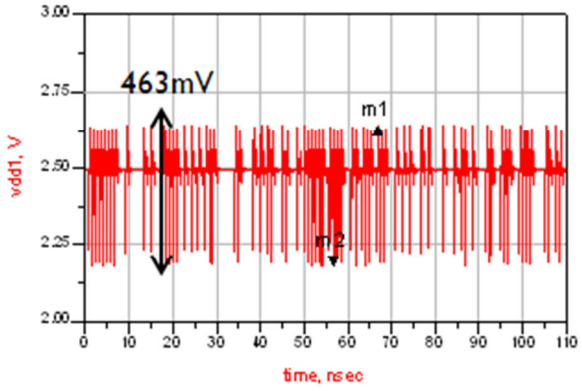


Figure 68 Digital supply noise

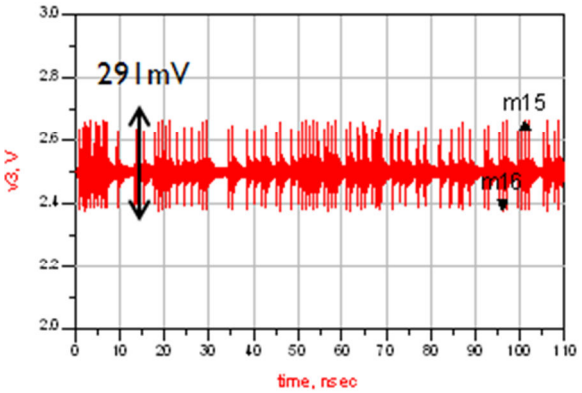


Figure 69 RF supply noise

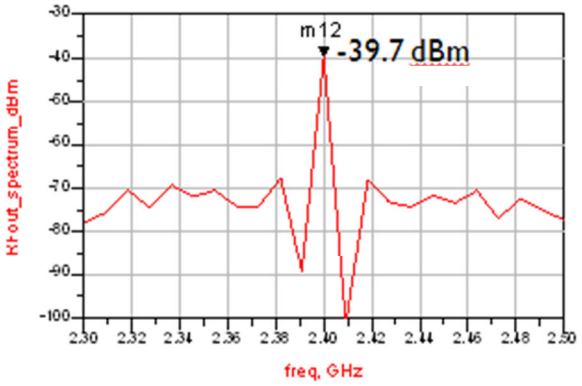


Figure 70 LNA output spectrum

Case 5: Digital buffers are ON, RF LNA is ON; with SSN filter

When Case 4 is repeated with the presence of the SSN filter, the noise at the output of the LNA is significantly reduced and the output spectrum of the LNA is nearly identical to that of Case 1, which is desired.

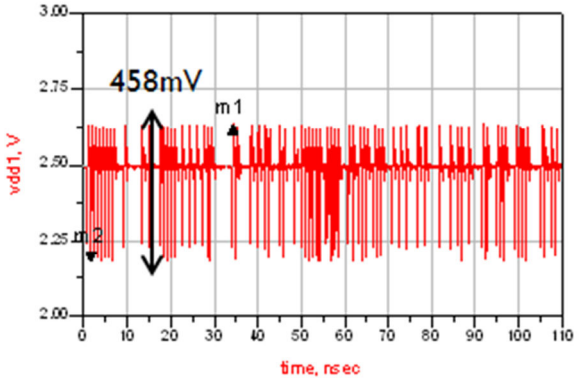


Figure 71 Digital supply noise

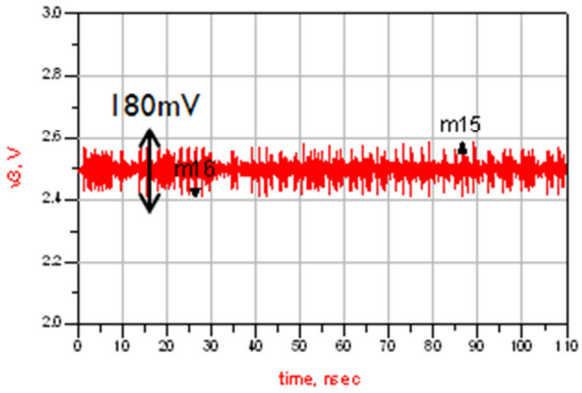


Figure 72 RF supply noise

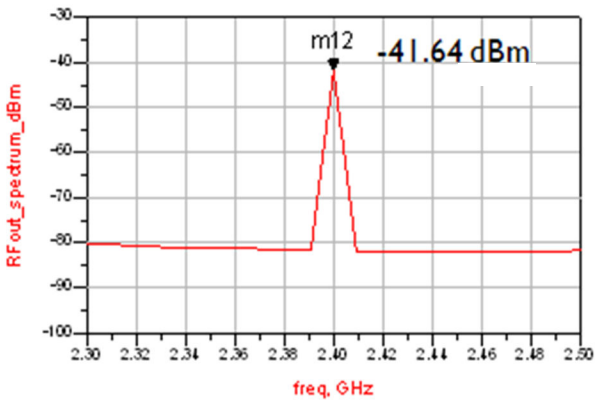


Figure 73 LNA output spectrum

These simulation results show the effectiveness of this strategy. By carefully designing the power delivery network and the SSN filter, it is possible to isolate the power supply noise between digital and RF circuit blocks in mixed signal systems. In order to further demonstrate this concept, several test vehicles were designed and measured.

5.5 Noise Isolation using PTL termination

In the second method, shown in Figure 74, the PTL connected to the digital buffers is source terminated. In addition to the reasons previously mentioned, the termination also has the added benefit of preventing noise from propagating into the supply rail of the LNA by absorbing digital supply noise. Therefore, this can be used as an effective method for noise isolation. Furthermore, the inclusion of the termination eliminates the need for the redundant bandstop filter.

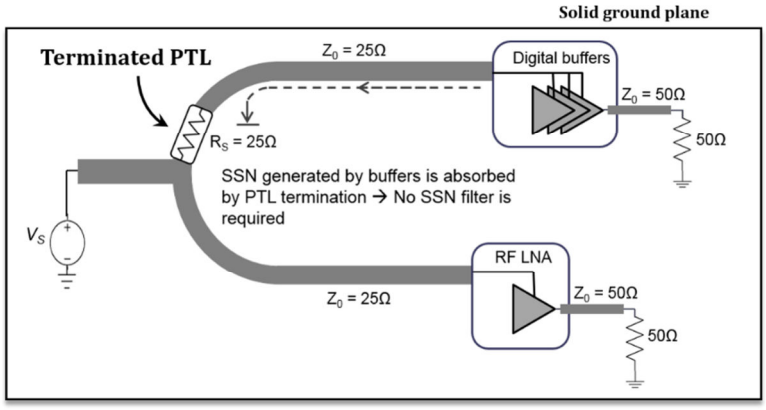


Figure 74 Mixed signal noise isolation concept using PTL termination without the filter.

5.6 Test Vehicles & Performance Metrics

In this paper, three test boards were designed, fabricated, and tested to demonstrate the effectiveness of each technique, and are listed in Table 16.

Table 16 Test Vehicles

Designation	Method
TV1	Electromagnetic bandgap structure
TV2	PTL with noise isolation filter
TV3	Terminated PTL without filter

All the test vehicles use the same commercially available 20-pin octal buffer/line driver with four 3.3V differential PECL drivers. The characteristic impedance of the PTL is chosen to be Z_0 = 25Ω for all cases. The RF circuit consists of an LNA with 11dB gain and an operating frequency f_0 = 1.8GHz, along with its corresponding biasing circuitry. The design of each is described in detail in the next section.

The purpose of this comparison is to investigate the effects of each method on power delivery, and, consequently, their impact on noise coupling and signal quality. Therefore, several

performance metrics are chosen to measure the efficacy of each technique. In terms of power integrity, the peak-to-peak noise voltage on the driver's supply pin on each test vehicle is measured for a range of data rates. This metric shows the relationship between the location of the PDN resonances and the input data rate. In addition, this serves as a baseline measurement for the amount of supply noise that is actually generated by each power distribution technique.

The signal integrity performance is characterized by capturing the eye diagrams of the transmitted digital signal. This metric provides a qualitative comparison of the signal quality that can be expected using the various schemes. In addition, it is known that power supply noise is a primary cause of data dependent jitter. The jitter and supply noise measurements can be correlated to gain a better understanding of the signal and power integrity performance of the various PDN schemes.

Lastly, the signal at the output of the LNA is measured to evaluate noise coupling. When the digital data drivers are switching, noise attributed to the higher order harmonics of the digital signal will appear at the output of the LNA. Viewing the LNA output in the frequency domain shows these undesirable signals. This metric establishes the effectiveness of the EBG and PTL solutions as viable methods for noise isolation.

5.6.1 Test Vehicle TV1 (EBG) Design

The EBG structure used in this work is based on the design described in [48]. However, it is important to note that the conclusions drawn here are independent of the specific EBG design used. A single unit cell consists of a square patch with meandering lines. To obtain the desired frequency response, which in this case is a bandstop at the operating frequency of the LNA, 1.8GHz, the dimensions of the patch and length of the meandering lines were adjusted. The completed EBG structure with port locations, as it is implemented in TV1, is shown in Figure 75

and Figure 76. The signal layer and the EBG are separated by a solid ground plane, in order to maintain a solid reference plane for the signals.

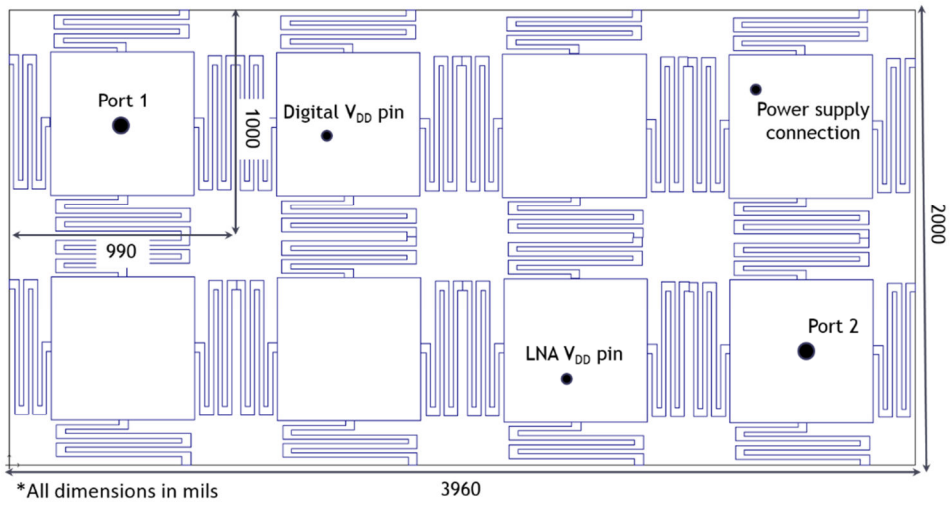


Figure 75 Electromagnetic band gap structure

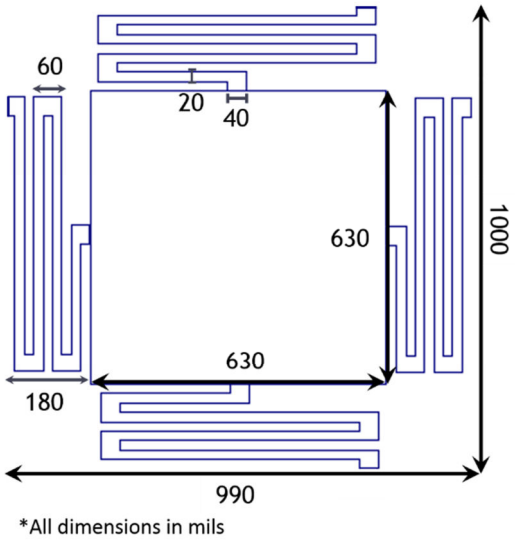


Figure 76 EBG unit cell

The measured insertion loss is shown in Figure 77. The EBG exhibits two bandstops, one from 0.5-1.2GHz and another from 1.4 to 2.0GHz, the latter of which is the focus of this work.

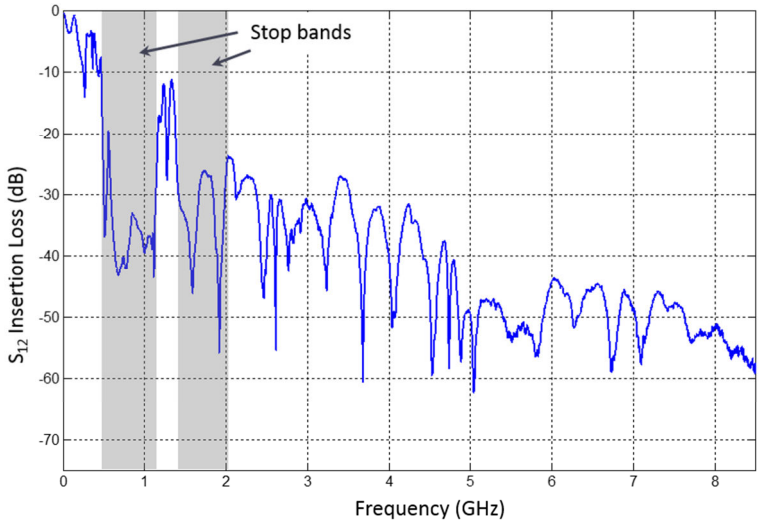


Figure 77 Electromagnetic band gap measured frequency response

The EBG's self-impedance, or Z_{11} parameter, is shown in Figure 78. As expected, the EBG self-impedance exhibits many resonance peaks outside the bandgap. This is a tradeoff between its high level of isolation and discontinuities encountered from the shape of the metal patterns. For EBG structures, the isolation levels can be increased, but at the cost of a corresponding increase in its self-impedance. In this design, the EBG structure has been optimized to obtain at least 30dB isolation in the stop band while concurrently keeping the self-impedance levels reasonably low to minimize noise at the source.

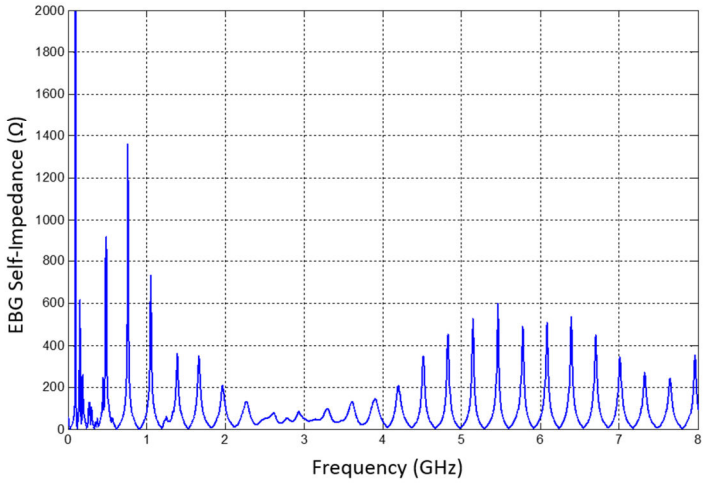


Figure 78 Measured self-impedance (Z11) of EBG structure

The test vehicle measures 5.08cm by 10.05cm. The cross-section of the test vehicle is shown in Figure 79. The fabricated test vehicle is shown in Figure 80.

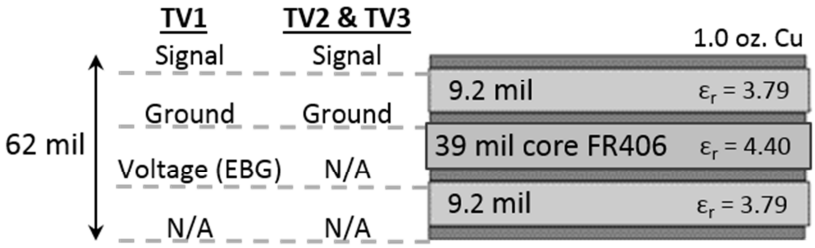


Figure 79 Test vehicle cross-section

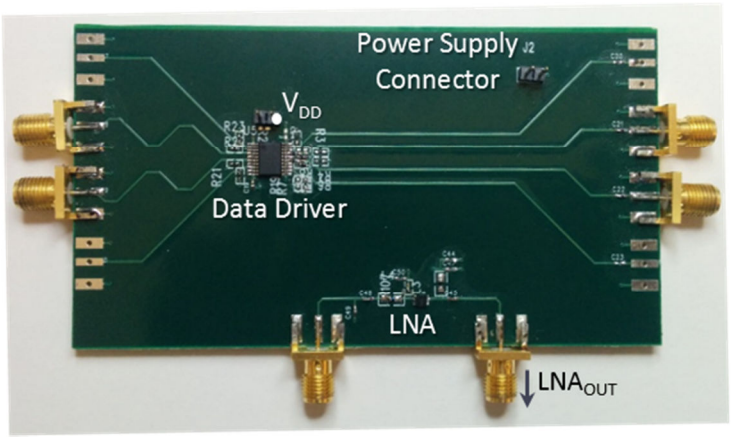


Figure 80 Layout of TV1

5.6.2 PTL-Based Test Vehicles

The fabricated test vehicle TV2 is shown in Figure 81 and is identical in size as TV1. The PTL is routed on the same layer as the signal traces, with the cross section shown in Figure 79. Since the PTL replaces the voltage layer, the voltage layer in Figure 79 was not used in TV2 and TV3. The PTL, which behaves as a transmission line and is referenced to the solid ground layer located beneath it, is used to power both the LNA and digital buffers. Furthermore, the bandstop filter is embedded in the PTL.

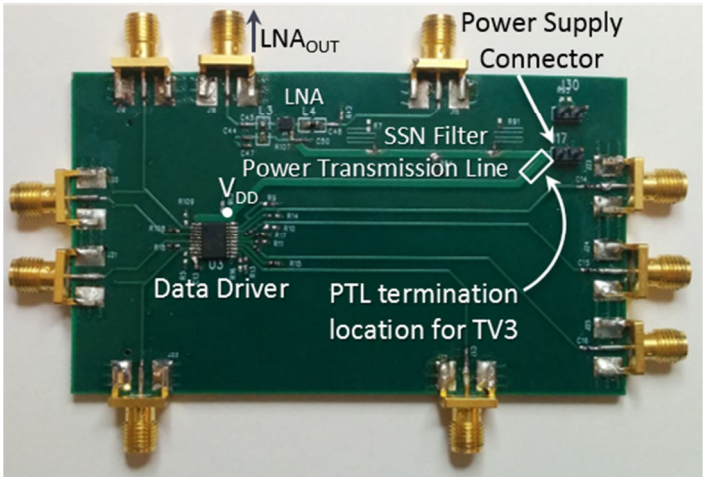


Figure 81 Layout of TV2

The bandstop filter used is a third-order Chebyshev filter created using the transmission line stub method [47]. In terms of implementation, the advantage of this method is that the filter is easy to design, requires minimum layout space, and does not require an extra layer or components. It is important to note that the EBG structure similarly functions as a distributed bandstop filter. In TV2, the transmission line stubs effectively replace EBG structure and use much less space, as shown in Figure 81 and Figure 82. The measured response of the Chebyshev filter is shown in Figure 83 and exhibits a bandwidth of 184MHz centered at 1.82GHz. The isolation level provided by the filter is 32.8dB.

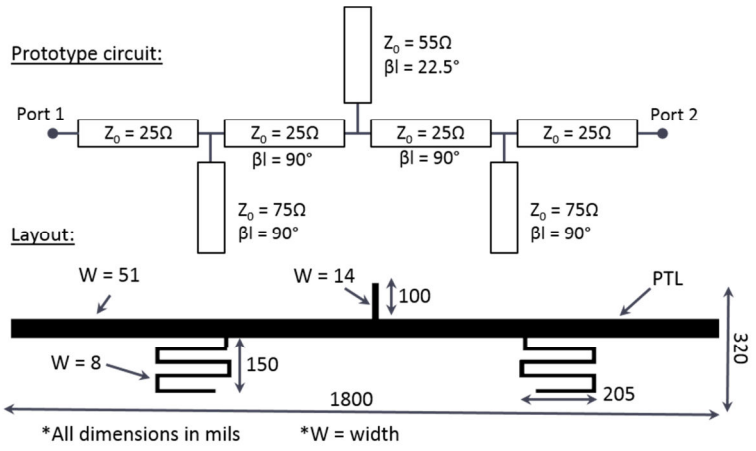


Figure 82 Layout of microstrip bandstop filter and PTL for TV2

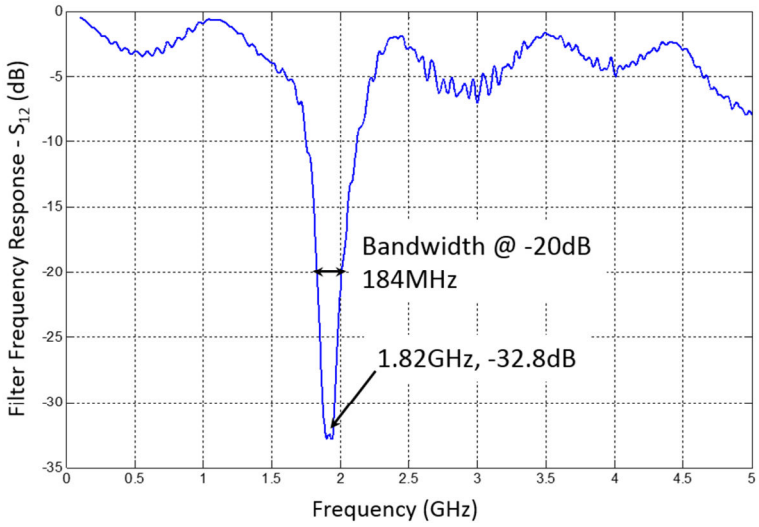
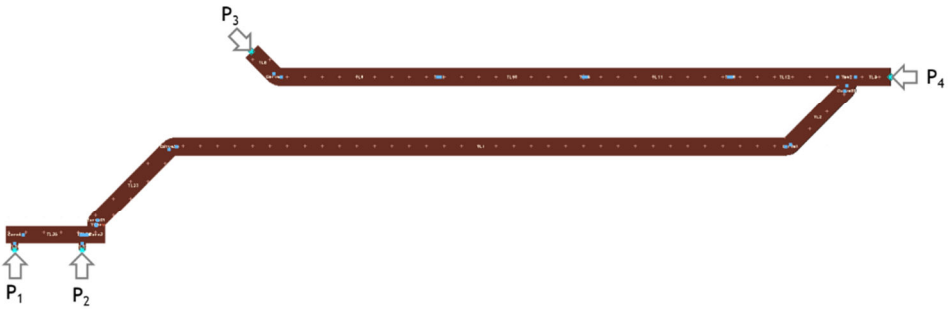


Figure 83 Bandstop filter frequency response

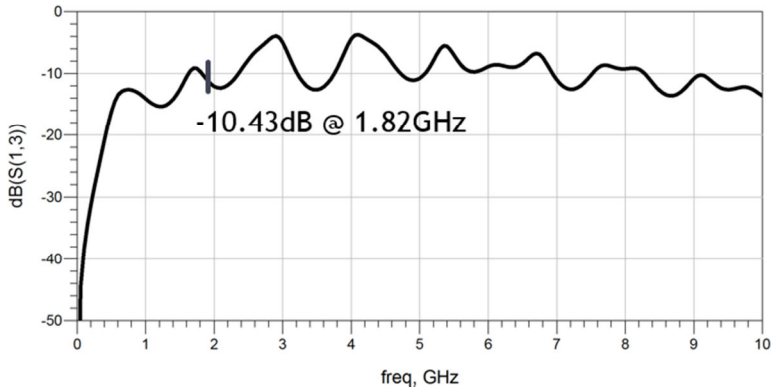
The layout for TV3 is not shown in this paper since it is similar to Figure 81, with a few modifications. TV3 has a 25Ω 0402 package surface mount resistor placed at the location shown in Figure 81 which acts as the source termination for the PTL. Therefore, TV3 does not use the SSN filter, so the stubs of the filter in Figure 82 are removed such that a single 25Ω PTL trace connects the power supply to the LNA.

5.7 Test Vehicle Noise Isolation Simulation Results

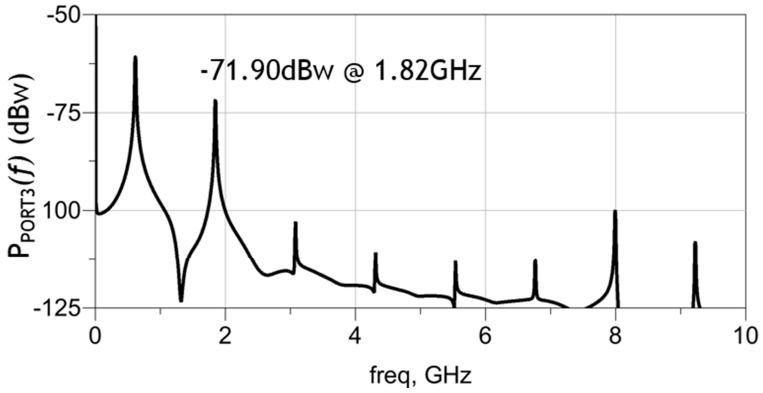
The subsequent sections provide detail on the experiments conducted to verify the effectiveness of the proposed noise isolation scheme. The PTL-based PDNs were simulated using Advanced Design System [49] and are compared in this section. Below, three cases are presented. In all of the structures port 4 is the location of the voltage supply. Ports 1 and 2 both connect to the V_{DD} pin of the digital buffers and port 3 connects to the bias voltage of the LNA. In the first case, the PDN consists of two unterminated power transmission lines powering the buffers and the LNA. In the second case, the PTL structure has the embedded bandstop filter, which is the same as TV2. In the third case, the PTL structure is terminated, as in TV3. These structures were extracted directly from the board layouts. For each case, the insertion loss between port 1 and port 3 (V_{DD} to LNA) was simulated. For this simulation, port 4 is shorted to ground, since the power supply can be approximated as an AC ground. In addition, a 100mV square wave with a frequency of 615MHz was injected into ports 1 and 2. All other ports are terminated with 50Ω. The spectrum of the voltage at port 3 is shown for the three structures in Figure 84 - Figure 86.



(a) Layout

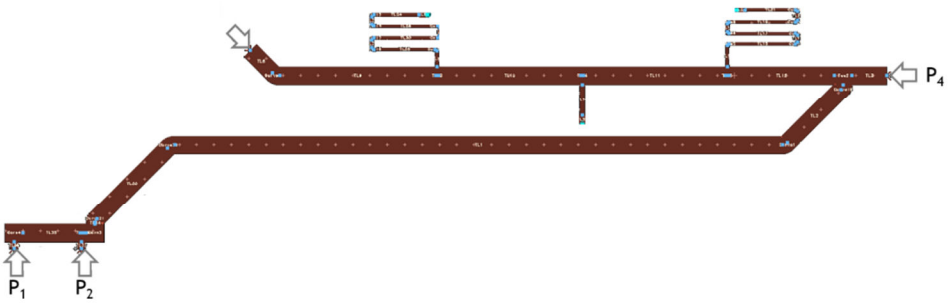


(b) S_{13} (dB)

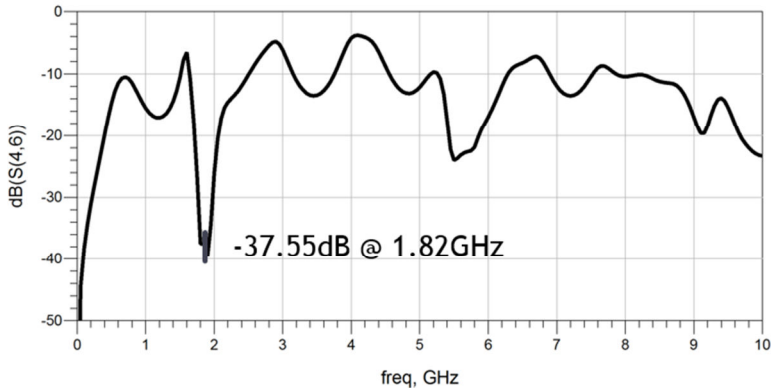


(c) $V_{PORT3}(f)$ (dB)

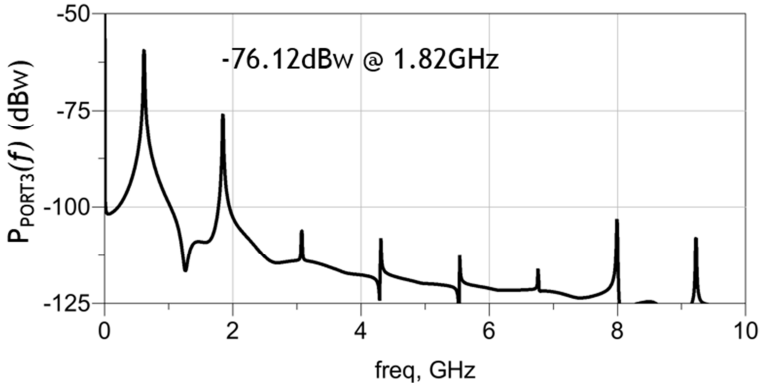
Figure 84 Simulations for Power Transmission Line (no filter or termination)



(a) Layout

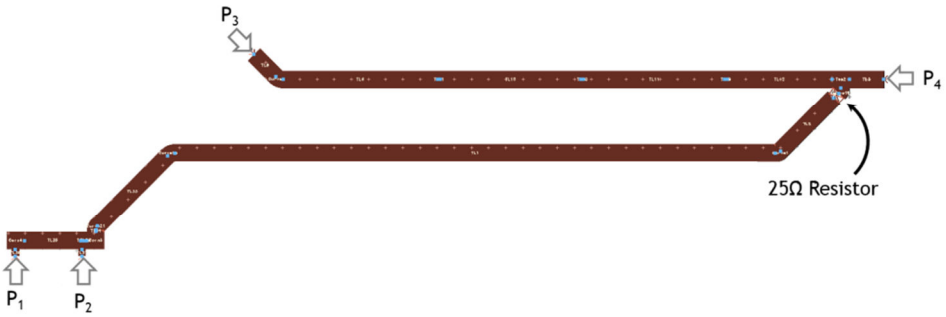


(b) S_{13} (dB)

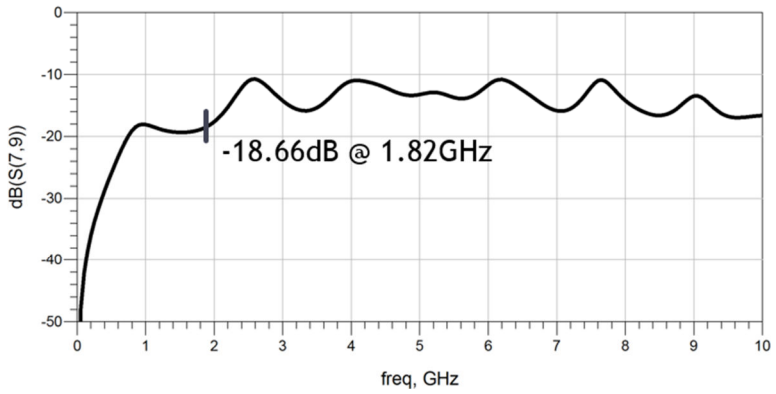


(c) $V_{PORT3}(f)$ (dB)

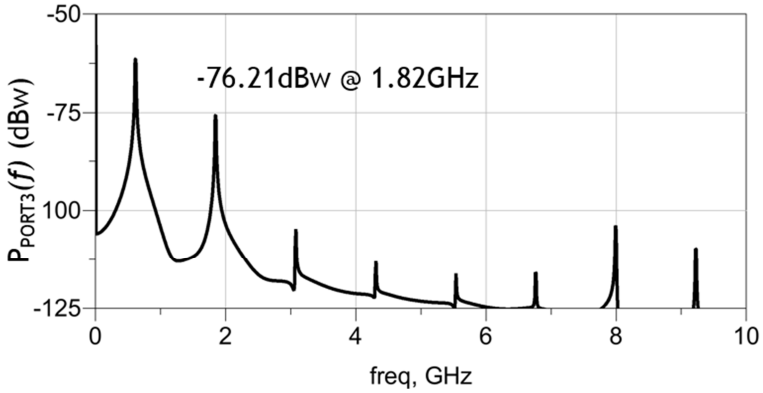
Figure 85 Simulations for Power Transmission Line with SSN filter (TV2)



(a) Layout



(b) S_{13} (dB)



(c) $V_{PORT3}(f)$ (dB)

Figure 86 Simulations for Power Transmission Line with 25Ω Termination (TV3)

Table 17 summarizes the results from these simulations. The addition of the SSN filter lowers the insertion loss by 27dB at 1.82GHz as compared to the standard PTL case. Similarly, the termination lowers the insertion loss by 8.2dB at 1.82GHz. This, in turn, translates to lower coupled supply noise seen at port 3.

Table 17 Summary of PTL noise isolation simulation results

Structure	Insertion Loss S_{13} at 1.82GHz	$P_{PORT3}(f)$ at 1.82GHz
PTL (no filter or termination)	-10.43dB	-71.90dBw
PTL with SSN filter (TV2)	-37.55dB	-76.12dBw
PTL with 25Ω Termination (TV3)	-18.66dB	-76.21dBw

It is important to note that in these simulations, the digital supply noise injected into ports 1 and 2 is the same for all three cases. Consequently, this is purely a measure of the noise isolation characteristics of each structure. It will be shown in the next section that in a realistic case, the amount of noise generated at port 1 and 2 by the digital buffers will not be the same.

5.8 Measurement Results

5.8.1 Power Integrity Comparison

The first measure of comparison is the magnitude of power supply noise generated by the digital drivers. The peak-to-peak power supply noise was measured as the input clock frequency is swept from 50MHz to 2GHz in 50 MHz increments, and is shown in Figure 87. The test point location for measuring the supply noise was at the driver's V_{DD} pin (the test point locations are labeled in Figure 80 and Figure 81). In Figure 87, the x-axis is the frequency of the input clock signal and the y-axis is the corresponding peak-to-peak power supply noise. It is important to note that every point on the curve in Figure 87 represents the noise measured at a specific input frequency and should not be confused with a simple Fourier transform of the supply noise. A Fourier transform of the supply noise would only show the frequency distribution for a given input signal. However, the representation shown in Figure 87 is much more useful, since it can

be used to correlate power supply noise as a function of PDN impedance for the range of input data rates.

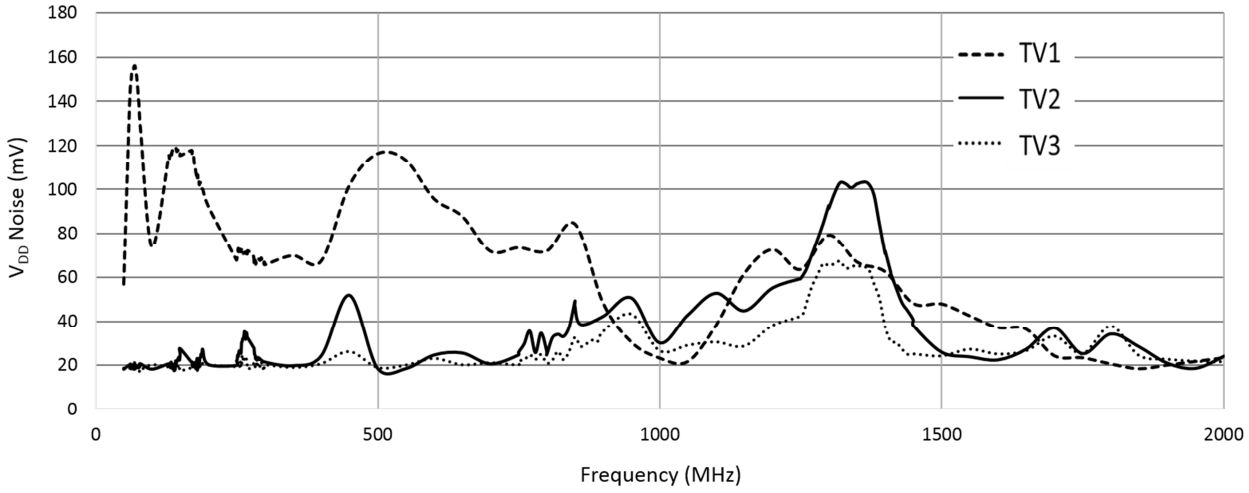


Figure 87 Measured power supply noise for all test vehicles versus clock frequency

From Figure 87, TV1 generates more noise than both TV2 and TV3 up to ~ 950MHz. This can be attributed to the large impedance spikes seen in Figure 78 below 1GHz. At 1GHz, the power supply noise reduces significantly due to the lower impedance at this frequency point (Figure 78). Around 1.3GHz, there are peaks for TV2 and TV3 with a similar increase in noise for TV1. Above 1.5GHz, the noise reduces in all three designs. The peaks in noise for TV2 and TV3 can be explained by transmission line effects.

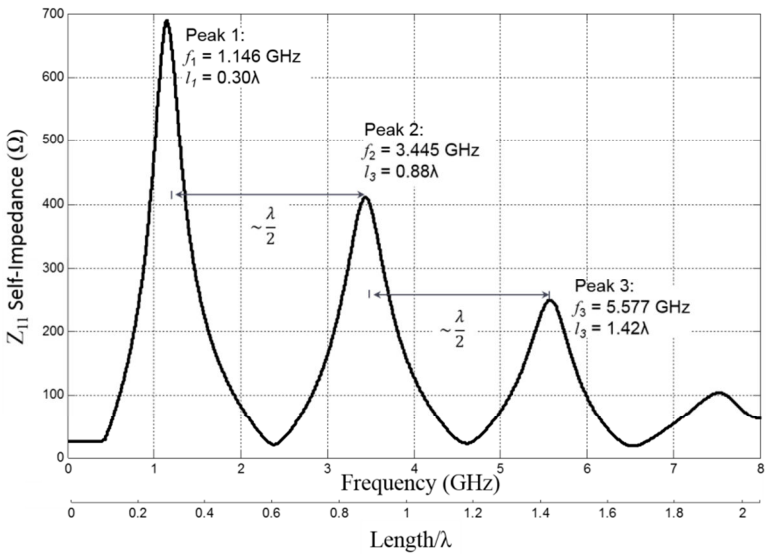


Figure 88 Simulated Z11 of power transmission line

The self-impedance of the PTL trace is shown in Figure 88 with the x-axes in terms of frequency and wavelength. The self-impedance is measured at the point where the PTL connects to the V_{DD} pin of the driver and the other end is connected to a voltage source (an AC short to ground). Therefore, the impedance profile shown is for a short circuited PTL for TV2. Like the EBG, the PTL also exhibits peaks in its impedance profile. When the PTL is source terminated, as it is in TV3, the resonances still exist due to board parasitics, and non-ideal resistive termination, albeit to a much lesser extent than TV2. This explains the reduced supply noise measured for TV3 as compared to TV2 in Figure 87. The location of the resonance points can be predicted from transmission line theory. As shown in Figure 88 impedance peaks occur at λ/2 resonance points.

By carefully analyzing the location of these resonances, along with the current flow in the circuit, the increased noise at specific frequencies for TV2 and TV3 can be explained. The noise voltage spectrum is proportional to the product of the PTL's self-impedance and the frequency spectrum of the current flowing through the PTL.

$$V_{DD}(f) = Z_{11}(f)I(f) = Z_{11}(f)S_{clk}(f) \tag{47}$$

TV1, TV2, and TV3 all utilize differential signaling, so the total current flowing through the PDN is nearly constant and independent of the data states, as discussed in [11].

Therefore, the supply noise is dictated primarily by the data edge transitions. For simplicity, it is assumed that the current has the same form as a clock signal, so $I(f) \approx S_{clk}(f)$. Consequently, the current spectrum is composed of impulse functions at odd integer multiples of the fundamental clock frequency. When one or more of the impulses overlap with the impedance peaks, a large amount of supply noise is generated.

Figure 89 shows the product of the clock spectrum and the PTL self-impedance for clock signals at 1.1GHz, 1.25GHz, and 1.400 GHz. At 1250 MHz, the peaks in the clock spectrum overlap with the peaks in the impedance curves and result in a larger noise voltage than at the other frequencies.

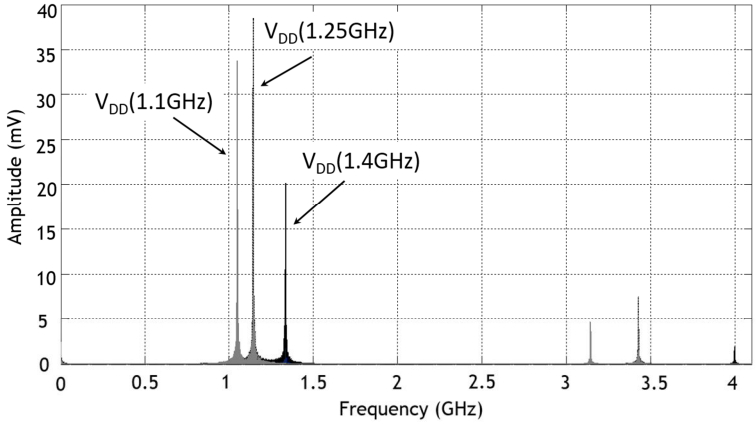


Figure 89 Calculated V_{DD} spectrum for three input frequencies

The balanced currents serve to reduce the current transients flowing across the PDN, and therefore mitigate the effect of the impedance peaks on supply noise for each test vehicle. However, comparing Figure 78 and Figure 88, there are less impedance peaks for the PTL for the considered frequency range and the peaks are significantly lower in amplitude. Consequently, the reduced impedance peaks translates to fewer decoupling capacitors for the PTL-based designs

compared to the EBG-based designs. In addition, a high frequency resistor with smaller tolerances and parasitics can completely eliminate resonances, thereby further reducing the need for decoupling capacitors in PTL-based designs.

5.8.2 Signal Integrity Comparison

The second measure of comparison was on signal quality by capturing the eye diagrams and the resulting jitter. The eye diagrams were measured using an Infiniium DCA-X 86100D oscilloscope. Power supply noise is a major contributor to signal integrity performance, especially jitter. Therefore, the total jitter was extracted from the eye diagrams to characterize the performance of each PDN scheme at various frequencies. The input signal was a 2^8-1 pseudo-random binary sequence (PRBS) at 500, 1000, 1300, 1650, and 2000 Mbps. Figure 90 shows the eye diagrams for the three test vehicles. The jitter values, determined using the Dual-Dirac jitter model at BER = 10^{-12} [50], are shown in Figure 91.

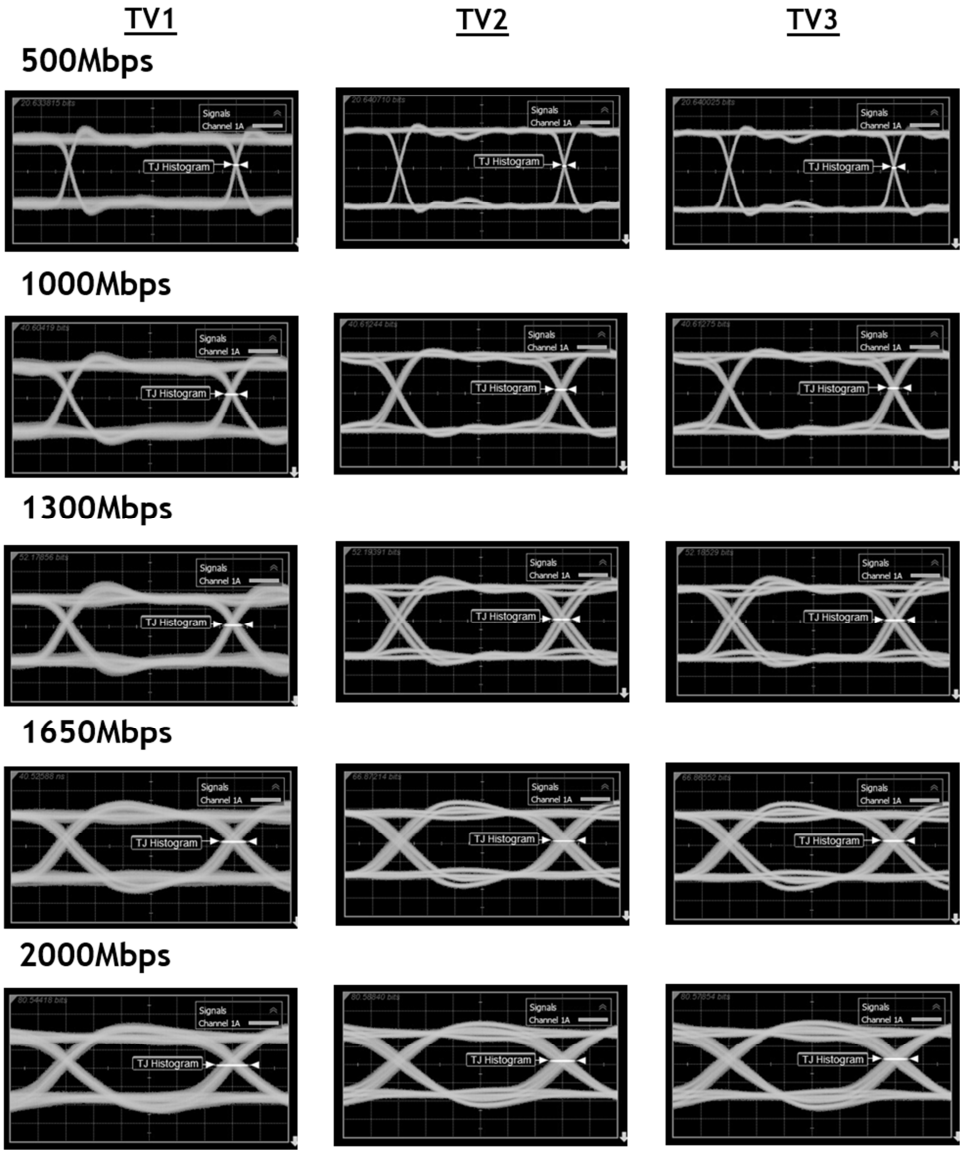


Figure 90 Eye diagrams for TV1, TV2, and TV3

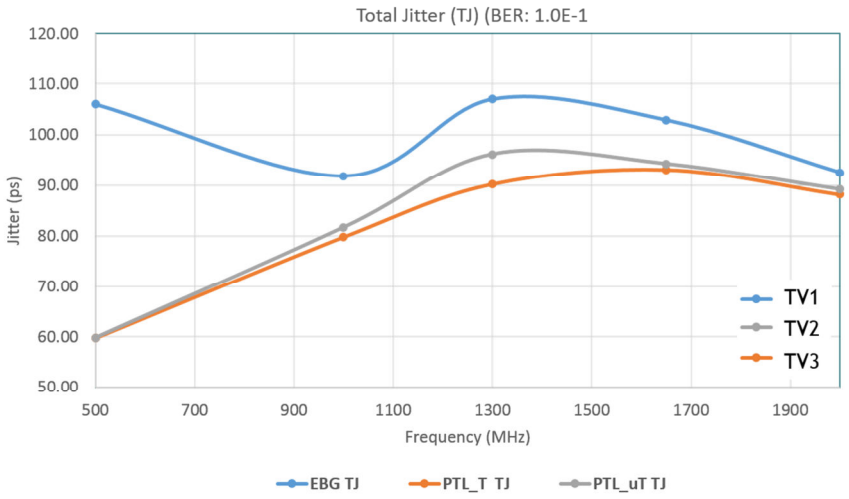


Figure 91 Total jitter (TJ) measured for all test vehicles

From Figure 91, TV1 exhibits consistently more jitter at all frequencies than either TV2 or TV3. At 500Mbps, both TV2 and TV3 show 60ps of total jitter. This is approximately 22.6% less than TV1, which shows 77.5ps. In general, it is expected that the jitter worsens at higher data rates, which is consistent with these findings. However, at 1300 Mbps, all three test vehicles exhibit the most jitter. This can be explained by Figure 87, where the power supply noise profile of each test vehicle shows a local maximum at approximately 1300MHz. In addition, TV3 has the lowest supply noise at 1300MHz, which is also consistent with the jitter results.

5.8.3 Noise Isolation Comparison

The third measure for comparison is the isolation level achievable at the output of the LNA in the presence of the switching data drivers. The source of this coupling is through the power distribution network. The test setup for the noise isolation measurements is shown in Figure 92.

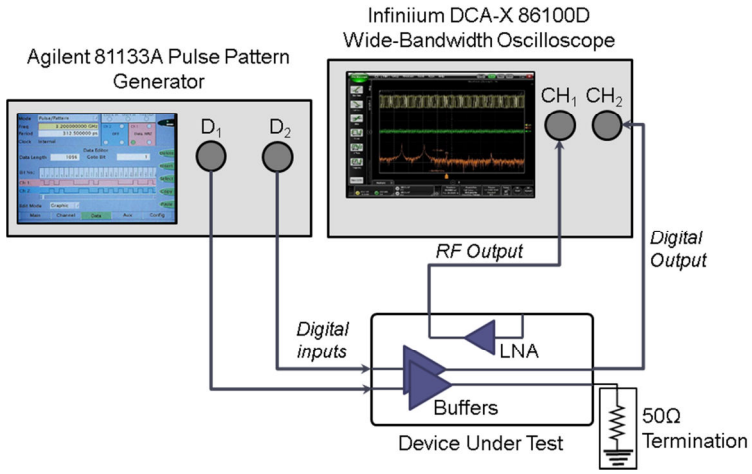


Figure 92 Measurement setup for noise isolation measurements

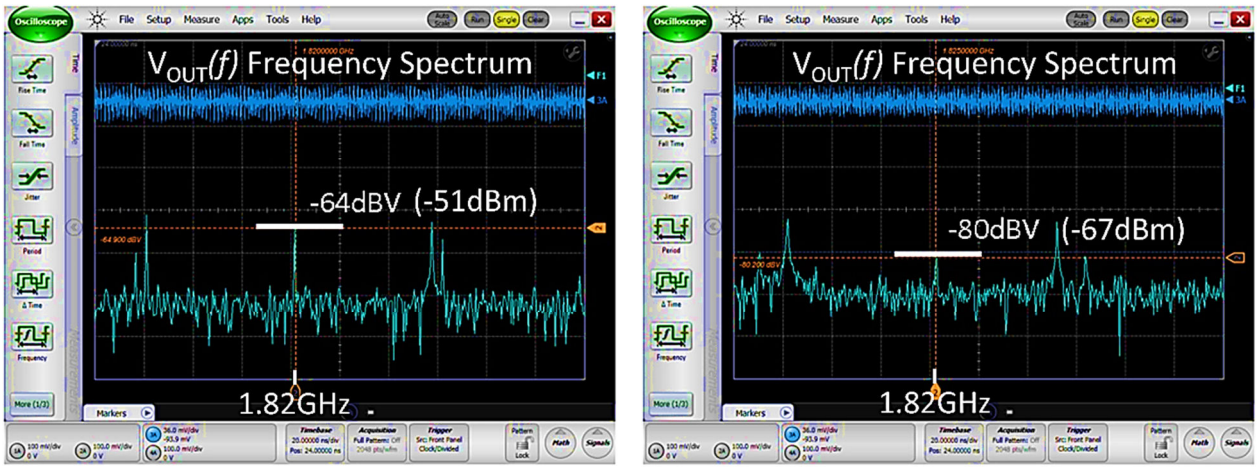
An Agilent 81133A pattern generator was used to provide the inputs for the digital buffers and an Infiniium 86100D oscilloscope was used to measure the coupled noise at the output of the LNA when the buffers are active.

5.8.3.1 Noise isolation of PTL vs. PTL with embedded SSN filter

Before presenting the noise isolation measurement results for the three test vehicles presented in this chapter, it will be informative to study the effect of just the embedded bandstop on noise coupling. Simulations showed that embedding the bandstop filter in the PTL significantly reduced the noise coupling in Section 5.4. However, in this section, the effectiveness of the filter will be characterized through lab measurements. The PTL-based test vehicle with the bandstop filter is shown in Figure 81. To get a true measure of the noise isolation benefits introduced by the filter, it must be removed. Consequently, the test vehicle presented in Figure 81 was modified by removing the filter's meandering stubs, resulting in a straight 25Ω transmission line connecting the supply voltage to the LNA circuitry. Without the stubs, the standard transmission line does not exhibit a bandstop response and does not isolate

noise between the digital and RF sections of the board. Other than this change, the rest of the test vehicle is identical to Figure 81.

For both test vehicle variants, the input data for the digital buffers was provided by a separate FPGA board which was programmed to provide four parallel pseudo-random bit (PRBS-8) patterns at 606MHz. At this data rate, the switching behavior of the drivers generates a harmonic at 1.82GHz, which is within the bandstop of the SSN filter. Figure 93 shows the measured frequency spectrum of the output of the LNA. Without the SSN filter, the peak in the spectrum at 1.82GHz has a magnitude of approximately -64dBV. The input impedance to the oscilloscope is 50Ω so the measured power level is -51.4dBm. With the presence of the filter, the peak is at -80dBV, or -67dBm. Consequently, the filter is effective in reducing the amount of switching noise that is coupled to the output of the LNA by 16dB [51].

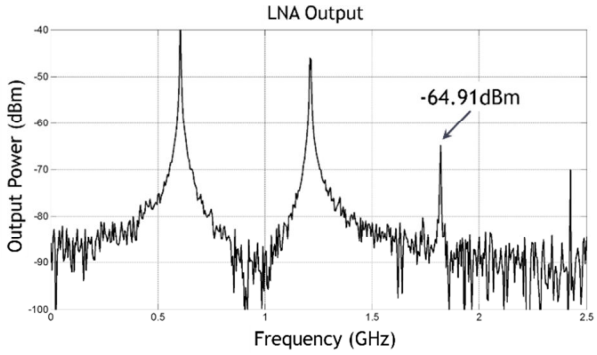


(a) (b)

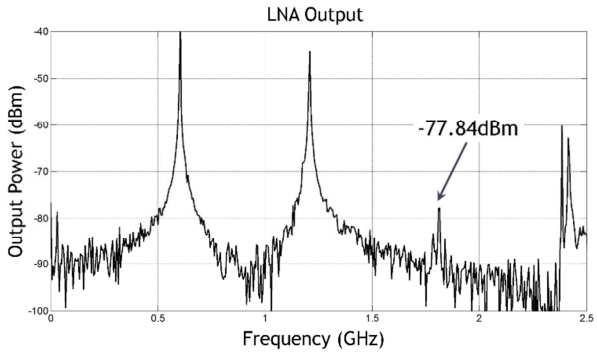
Figure 93 LNA output without filter (b) LNA output with SSN filter

5.8.3.2 Noise Isolation Comparison

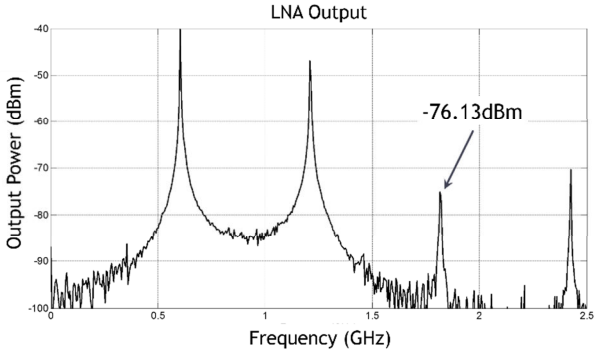
The input to the digital buffers is a 606MHz clock signal. Therefore, the supply noise from the digital buffers has a harmonic at 1.82GHz, which falls within the operating frequency of the LNA. Figure 94 shows the output of the LNA for TV1, TV2, and TV3 test vehicles, respectively.



(a)



(b)



(c)

Figure 94 Output of LNA for (a) EBG (TV1), (b) PTL + Filter (TV2), (c) PTL + termination (TV3)

For TV1, the LNA output is -64.91dBm at 1.82GHz. For TV2, the output signal is at -77.84dBm while for TV3, it is at -76.13dBm. A zoomed view of the measured waveforms is shown in Figure 95, which clearly shows the noise isolation performance of each test vehicle in the frequency range of interest. The presence of the embedded bandstop filter in TV2 reduces the noise coupling into the LNA by 13dB as compared to TV1. The improvement is due to two factors, namely, (i) the SSN filter is effective in attenuating switching noise components that fall within the operating bandwidth of the LNA, and (ii) the use of a power transmission line generates less noise at the V_{DD} node as compared to the EBG for an input signal at 606MHz, as shown in Figure 87.

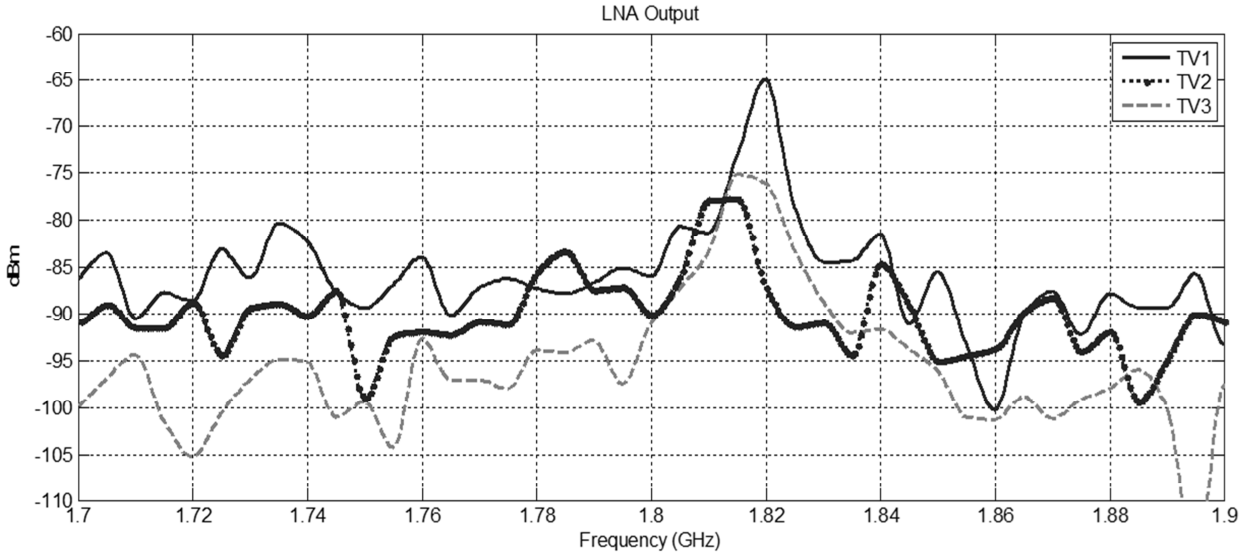


Figure 95 Frequency domain output of LNA for each test vehicle

In addition, TV3 shows 11.2dB reduction in the peak noise at 1.82GHz as compared to TV1. The source termination absorbs voltage fluctuations generated at the supply pin of the digital buffers, effectively attenuating noise from propagating to the LNA. This serves the same function as the SSN filter, except the resistive source termination is not frequency selective and therefore provides broadband performance. In all of these examples, the noise at out-of-band

frequencies still exists. However, the SSN harmonics are far away from the operating frequency of the LNA and therefore can be filtered at the output of the LNA**.**

5.9 Comparison

In this section, we provide a qualitative and quantitative comparison of the three approaches based on design experience and measurement results. The measurement results are compared for the three test vehicles using the metrics described earlier at several frequencies. A comprehensive comparison of the three test vehicles from the measurements is shown in Table 18.

Table 18 Measurement Comparision of TV1, TV2, and TV3

	Power Supply Noise (V_{pk-pk} in mV)			**Total Jitter (in ps)**			**Noise Isolation**
	500 MHz	1000 MHz	1500 MHz	500 MHz	1300 MHz	2000 MHz	$V_{LNA,OUT}$ @ 1.82GHz
TV1	77.5	23.33	47.95	77.5	107.0	106.7	-64.91dBm
TV2	19.05 (-75.4%)	30.23 (+29.5%)	25.9 (-45.9%)	59.8 (-22.6%)	96.2 (-10.2%)	89.2 (-15.8%)	-77.84dBm (-12.93dB)
TV3	19.05 (-75.4%)	26.72 (+14.5%)	24.3 (-45.9%)	59.7 (-22.6%)	90.3 (-15.9%)	88.2 (-16.8%)	-76.13dBm (-11.22dB)

In Table 18, three frequencies, namely 500 MHz, 1000 MHz, and 1500 MHz, were chosen for the power supply noise and jitter comparison. Except at 1000MHz, the PTL-based designs show substantial improvement in power supply noise. Around 1000 MHz, the PTL-based designs show an increase in power supply noise due to the half-lambda resonance, which can be suppressed using decoupling capacitors.

With jitter measurements, the PTL-based designs always performed better than the EBG design. For isolation measurements, the PTL design showed substantial improvement as well. EBGs, while capable of achieving high levels of isolation, have several disadvantages. A major concern for highly integrated systems is board space. EBGs, depending on the stop band specifications, require large board area and must be placed on a separate layer. This further adds to routing difficulties and increases cost. In addition, and perhaps more importantly, EBGs exhibit cavity resonances along both x and y dimensions. In comparison, transmission line structures exhibit resonances along only the length dimension and are, therefore, easier to control.

In contrast to EBG structures, power transmission lines are easier to design and their response is easier to predict. In addition, filters and termination resistors can be designed into the PTL, thereby reducing board space. Table 19 provides a qualitative comparison of the three design approaches.

Table 19 Qualitative comparison

	Advantages	Disadvantages
EBG (TV1)	▪ Good noise isolation	▪ Complex design ▪ Requires large area ▪ Requires separate layer for EBG ▪ Larger power supply noise ▪ Resonances along two dimensions ▪ More decoupling capacitors required
PTL w/ Filter (TV2)	▪ Simple design ▪ Better noise isolation ▪ Lower supply noise ▪ Predictable resonances ▪ Filter requires less area than EBG ▪ Fewer decoupling capacitors required ▪ PTL & signal traces always referenced to solid ground layer	▪ Requires filter ▪ λ/2 resonance frequencies along one dimension
PTL w/ Resistor (TV3)	▪ Simple design ▪ No filter ▪ Best noise isolation ▪ Fewest decoupling capacitors required ▪ Reduced λ/2 resonances based on resistor tolerance and parasitics	▪ DC drop across termination resistor

5.10 Summary

It is well known that digital circuitry, especially high-speed I/Os and logic, produce large amounts of power supply noise. In highly integrated systems, it is important to consider noise coupling between noisy digital circuitry and sensitive RF components. In this work, three techniques are proposed to address this problem and compared with regards to noise isolation and signal/power integrity. The first method used an electromagnetic bandgap structure that functions as both a power delivery network and a distributed filter for noise isolation. The other two methods use a combination of a power transmission line and embedded bandstop filter or source terminated resistor as the mode of power delivery. The findings are corroborated with extensive laboratory measurements, including power supply noise across a range of frequencies, eye diagram, jitter, and noise isolation. The EBG is an interesting solution due to its flexibility. However it has fundamental limitations that include large board area, unpredictable self-impedance, and long design time. The proposed methods, however, utilize simple transmission line structures. These structures are well defined and easy to design and predict. The PTL methods showed significantly better signal and power integrity performance compared to the EBG solution. Consequently, the PTL methods could be a promising solution for isolation in mixed-signal electronics due to its simplicity in design and implementation especially for low power electronics.

CHAPTER 6: POWER DISTRIBUTION EFFICIENCY WITH POWER TRANSMISSION LINES

6.1 Introduction

In the previous sections, it has been shown that power transmission lines can be an effective alternative to standard voltage and ground plane power distribution. In this section, the effect of the power transmission line on the efficiency of a power delivery system is discussed. Figure 96 shows a standard power distribution network using a switching voltage regulator and a linear low dropout voltage regulator.

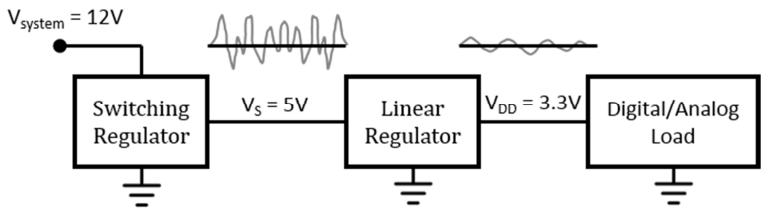


Figure 96 Power distribution with a switching and linear regulator

Switching and linear regulators are used in power distribution networks to provide a constant and stable voltage supply that is relatively independent to changes in the input voltage, operating conditions, and environmental factors. However, each has its own advantages and disadvantages, as described in Table 20.

Table 20 Comparison of switching and linear regulators [52]

	Linear Regulators	Switched Regulators
Output voltage range	$V_{OUT} < V_{IN}$	$V_{OUT} < V_{IN}$ (Buck), or $V_{OUT} > V_{IN}$ (Boost)
Efficiency	Limited by V_{OUT}/V_{IN}	High (commonly > 80%)
Transient response	Fast	Slow, limited by switching frequency
Output power	Low/Moderate	High
Output noise	Low	High
Integration	Can easily be integrated with other digital/analog components	Inductor requires large die space, usually placed off-chip

Switching regulators generally offer greater flexibility since these circuits can be designed to output a voltage that can be either higher or lower than the input voltage. Linear regulators, which generate an output voltage by modulating the resistance of a pass element, are limited to $V_{OUT} < V_{IN}$. In addition, since switching regulators operate by repeatedly charging and discharging a storage element, very little power is lost. It is common for switching regulators to achieve efficiencies upwards of 85-95% at maximum load current, as shown by the efficiency-current profile of a LTC3601 step-down regulator in Figure 97 [53].

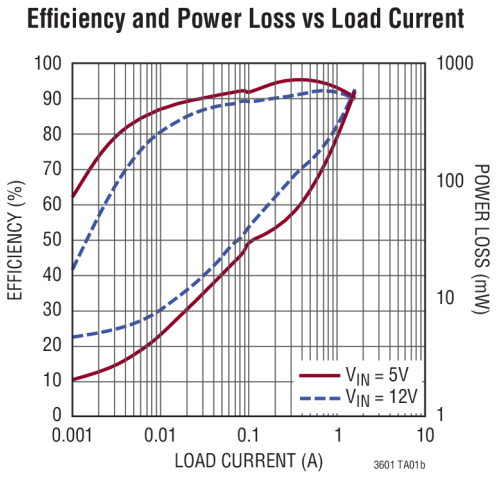


Figure 97 Efficiency and power loss vs. load current of LTC3601 from Linear Technology [53]

Linear regulators, however, shunt excess current to ground, and therefore are inherently less efficient than their switching counterparts. The efficiency of linear regulators can be improved by designing the quiescent current to be as low as possible and by keeping the difference in the input and output voltage to be low. The power efficiency of a linear voltage regulator is given by Equation (48) [52].

$$\eta_{LDO} \approx \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} = \frac{I_O \cdot V_O}{(I_O + I_Q) \cdot V_{IN}} < \frac{V_O}{V_{IN}} \tag{48}$$

The switching behavior of switching regulators leads to a large ripple in the output voltage. Therefore, an LDO can be placed at the output of the switching regulator to maintain a constant voltage without the undesirable ripple noise. Consequently, both the high efficiency of a switching regulator and the good noise performance of a linear regulator can be maintained when used in a configuration as shown in Figure 96.

The inductors used in switching regulators are generally too large to easily be integrated on the die along with the power FETs and control circuitry. The inductor can be made smaller by increasing the switching frequency, but that will reduce system efficiency, as discussed in [54]. Therefore, the size constraints require that a switching regulator is commonly placed far away from the load circuits. In Figure 98, the switching and linear regulators are connected together using a power transmission line. Unlike conventional power and ground planes, the power transmission line will exhibit inherently larger ohmic loss. Therefore, when the power distribution system is operating at maximum load conditions, it is important to account for the losses on the PTL when computing overall system efficiency, which will be presented in this chapter.

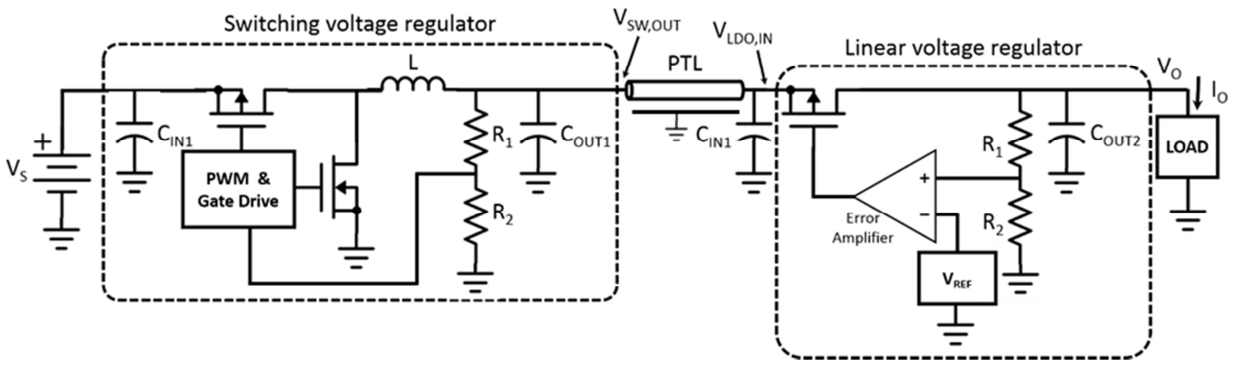


Figure 98 Power distribution network with a switching and linear regulator connected using a PTL

6.2 Design Parameters

In the subsequent analysis, several assumptions have been made, and are summarized below.

1) The PTL is implemented as a microstrip transmission line and the metal layer used is copper ($\sigma = 5.97 \cdot 10^{-7}$ S/m).
2) The switching frequency of the buck regulator is very low compared to digital signals (from hundreds of kHz up to 10MHz). Consequently, the spectral content of its output voltage will consist of only low frequency components. Therefore, high-frequency losses, such as dielectric loss and skin effect, are neglected for this analysis.

The conductor loss of the PTL can be determined by the cross-section of the PTL, shown in Figure 99.

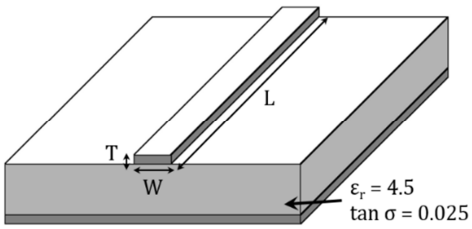


Figure 99 Microstrip cross-section

From [55], the DC loss per-unit-length of a microstrip line can be calculated from Equation (49).

$$R'_{DC} = \frac{1}{\sigma TW} = \frac{\rho}{TW} \tag{49}$$

In Equation (49), σ and ρ are the conductivity and resistivity of the conductor, respectively, and T and W are the dimensions of the line as shown in Figure 99. The DC conductor loss is calculated for varying PTL lengths and widths. The length of the PTL is varied from 1,000mils (2.54cm) to 12,000mils (30.48cm) in 100mil (0.25cm) increments. Concurrently, the width is varied from 25mils (0.06cm) to 1,000mils (2.54cm) in 25mil increments. For reference, the 25Ω PTL in the CV-PTL test vehicle in Section 2.3 has dimensions W = 50mils and L = 3500mils. The total calculated DC resistance is shown in Figure 100.

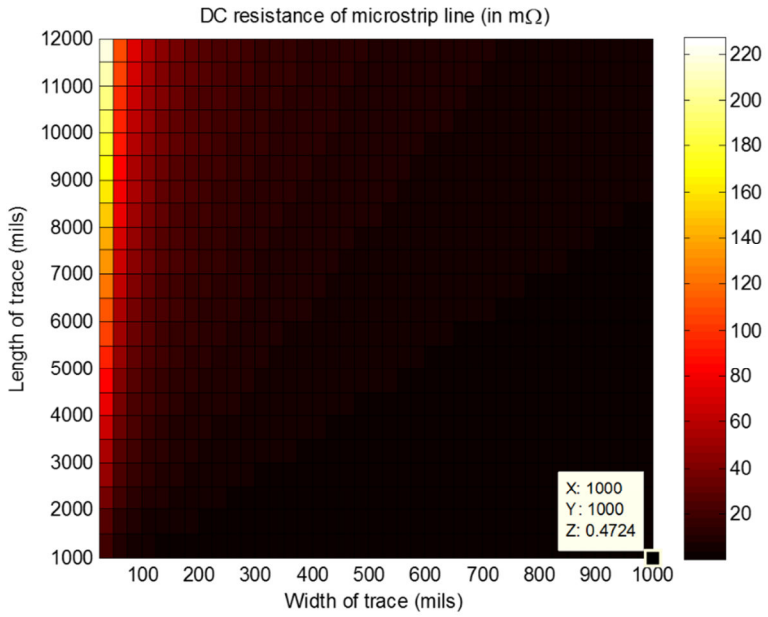


Figure 100 Total DC resistance (mΩ) for PTL with varying width and length

The maximum resistance, for a line that is 12,000mils long and 25mils wide, is 226mΩ. The voltage regulators have the parameters shown in Table 21.

Table 21 Power distribution network parameters

Parameter	Value
System voltage, V_S	5V
Output voltage of switching supply, $V_{SW,OUT}$	3.3V
Output voltage, V_{OUT}	2.5V
Max output current, I_{OUT}	1A
LDO dropout voltage, V_{DO}	300mV
LDO quiescent current, I_Q	0.5mA

The system voltage, which is the input to the switching regulator, is 5V. This voltage is then stepped-down to 3.3V ($V_{SW,OUT}$) and fed through the PTL to the LDO. The LDO regulates the load at 2.5V for a maximum current of 1.0A. In the absence of the PTL, the nominal efficiencies of the switching regulator and the LDO are 95.10% and 75.72%, respectively. The efficiency of

the switching regulator was simulated using LTSpice with a LTC3601 synchronous buck regulator model from Linear Technology and agrees with the data from Figure 97. When the PTL is included, the DC voltage at the input of the LDO will be given by Equation (50).

$$V_{LDO,IN} = V_{SW,OUT} - (I_O + I_Q) \cdot R_{DC} \tag{50}$$

The input voltage for the LDO for varying PTL lengths and widths is shown in Figure 101.

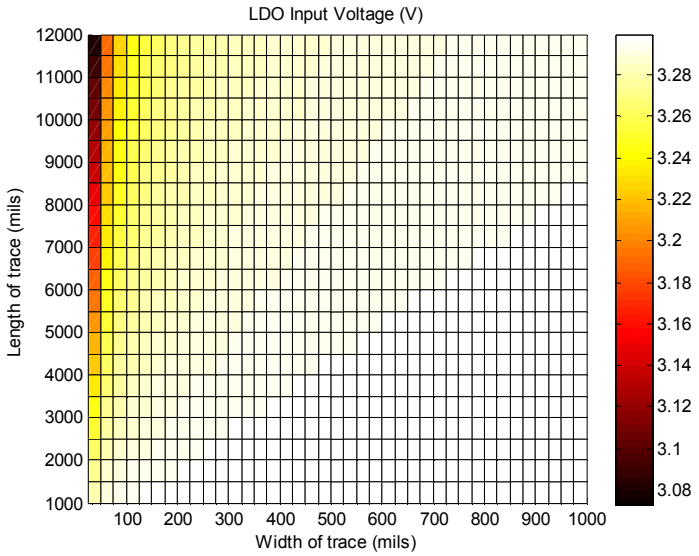
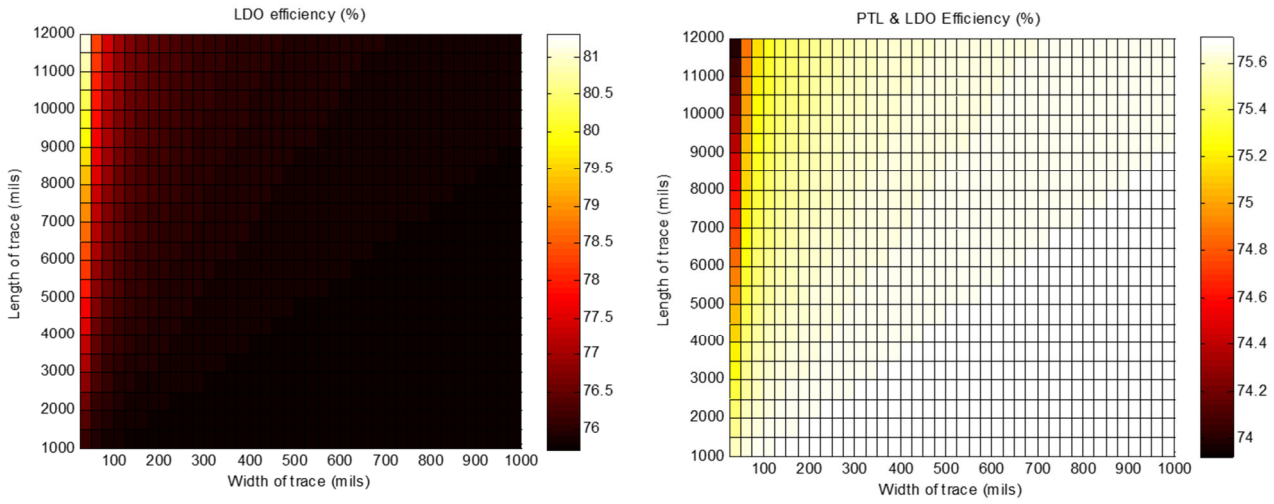


Figure 101 LDO input voltage ($V_{SW,OUT}$ = 3.3V, V_O = 2.5V, $I_{O,Max}$ = 1A)



(a) (b)

Figure 102 (a) Power efficiency of the LDO, (b) Power efficiency of the LDO including PTL loss

In Figure 102, the power efficiency of the LDO is shown in Figure 102(a) and the efficiency of the PTL and LDO combination is shown in Figure 102(b). The equation to calculate the efficiency of the LDO is given by Equation (51), where $V_{LDO,IN}$ can be found from Equation (50).

$$\eta_{LDO} \approx \frac{P_{IN} - P_{LOSS}}{P_{IN}} = \frac{I_O \cdot V_O}{(I_O + I_Q) \cdot V_{LDO,IN}} \tag{51}$$

The efficiency of the PTL and LDO is calculated from Equations (52)-(55). $P_{LOSS,DO}$ is the power loss associated with the LDO's dropout voltage. $P_{LOSS,Q}$ is the loss from the quiescent current and $P_{LOSS,PTL}$ is the power loss from the PTL.

$$\eta_{LDO+PTL} \approx \frac{P_{IN} - P_{LOSS}}{P_{IN}} = \frac{V_{SW,OUT} \cdot I_O - (P_{LOSS,DO} + P_{LOSS,Q} + P_{LOSS,PTL})}{V_{SW,OUT} \cdot I_O} \tag{52}$$

$$P_{LOSS,DO} = (V_{LDO,IN} - V_O) \cdot I_O \tag{53}$$

$$P_{LOSS,Q} = V_{LDO,IN} \cdot I_Q \tag{54}$$

$$P_{LOSS,PTL} = I_O^2 \cdot R'_{DC} \tag{55}$$

These calculations do not include the effect of the switching regulator since the PTL does not affect the operation of the switching regulator and therefore, its efficiency will stay constant. Also, in a real system, the power efficiency is dependent on the switching activity of the load circuits (peak power, idle, sleep mode, etc.), but the efficiencies shown here apply for maximum current consumption.

The DC resistance of the PTL causes a voltage drop across the line, therefore the input voltage to the LDO will be lower than the output of the switching regulator. Consequently, the difference between the $V_{LDO,IN}$ and V_{OUT} is reduced. From (51), this actually results in an increase in the LDO efficiency. However, as shown by Figure 102(b), this does not change the combined efficiency much because the power loss from the PTL is offset by the increase in efficiency of the LDO.

The LDO used in this analysis has a dropout voltage of 300mV. Therefore, the component will output a stable voltage as long as the input is above 2.80V, as shown in Figure 103.

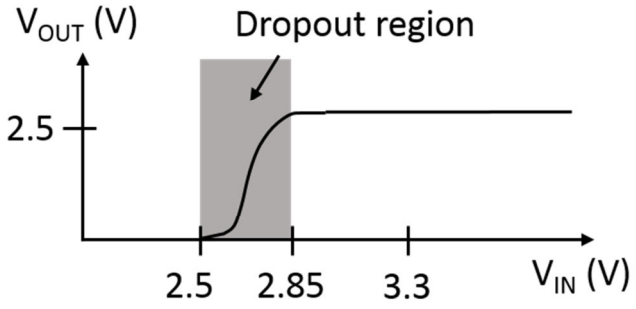


Figure 103 Dropout voltage of LDO

However, if the switching regulator is designed to output a voltage of 2.85V, which is at the edge of operation for the LDO, the effect of the voltage drop across the PTL will be more pronounced. For this situation, the nominal efficiency for the LDO is 87.7% from Equation (48). Figure 104 shows the input voltage for the LDO when the output of the switching regulator is 2.85V.

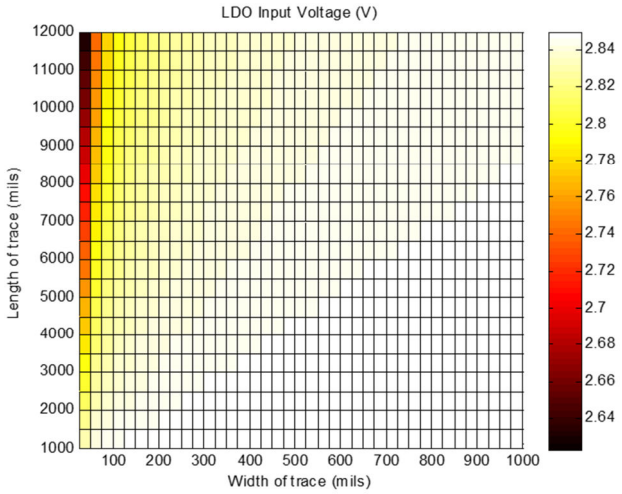


Figure 104 LDO input voltage ($V_{SW,OUT}$ = 2.85V, V_O = 2.5V, I_O = 1A)

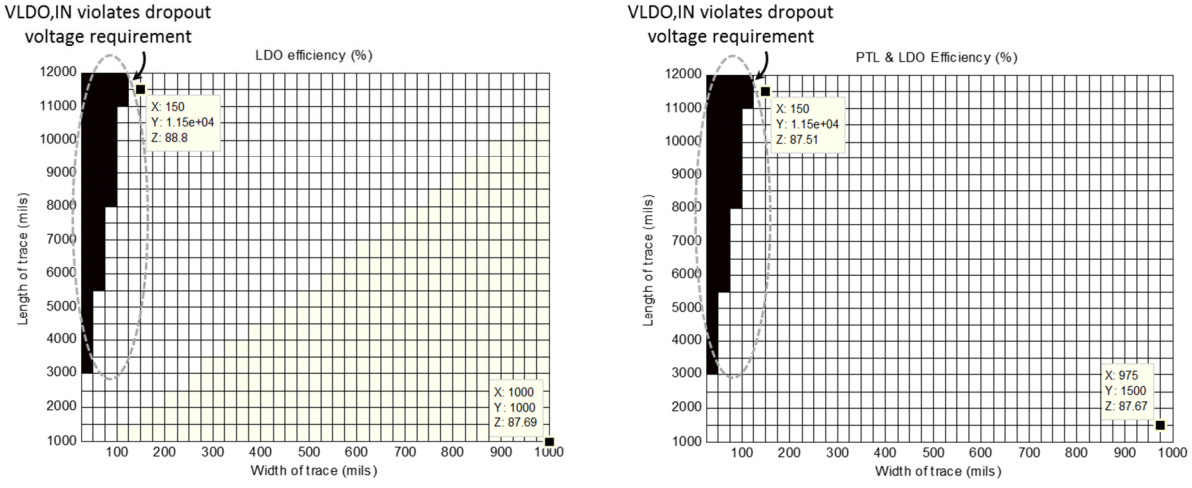


Figure 105 (left) Power efficiency of the LDO (right) Power efficiency LDO with PTL loss ($V_{SW,OUT}$ = 2.85V, V_O = 2.5V, I_O = 1A)

Figure 105 shows the efficiency for the LDO and the combined PTL & LDO combination as before. For most cases, the efficiency is nearly unchanged from its nominal value. However, there are states, which are circled in Figure 105, in which the input to the LDO drop below 2.8V. For these states, the pass transistor will no longer have sufficient voltage across it to operate in saturation mode. The transistor will enter triode mode, and therefore will have much larger drain-source resistance. Consequently, the LDO will no longer be able to support a regulated output voltage, causing the entire system to fail.

In fact, at higher currents this can have a substantial impact on the overall performance of the system. For instance, if the output current is designed to be 2A, then the voltage drop across the PTL due to its ohmic loss will violate the LDO's dropout voltage condition for all the PTL lengths and widths.

Therefore, the design curves shown in Figure 106 can be used to determine the appropriate dimensions of the transmission line used to connect the switching and linear regulator. In Figure 106, the ratio of the length to width of the PTL is plotted against the load current for various output voltages of the switching regulator. It was shown in this chapter that the dimensions of the PTL dictate its resistance and therefore its power loss. Depending on the output voltage of the switching regulator ($V_{SW,OUT}$), the DC voltage drop across the PTL may be sufficient to violate the dropout voltage requirement LDO.

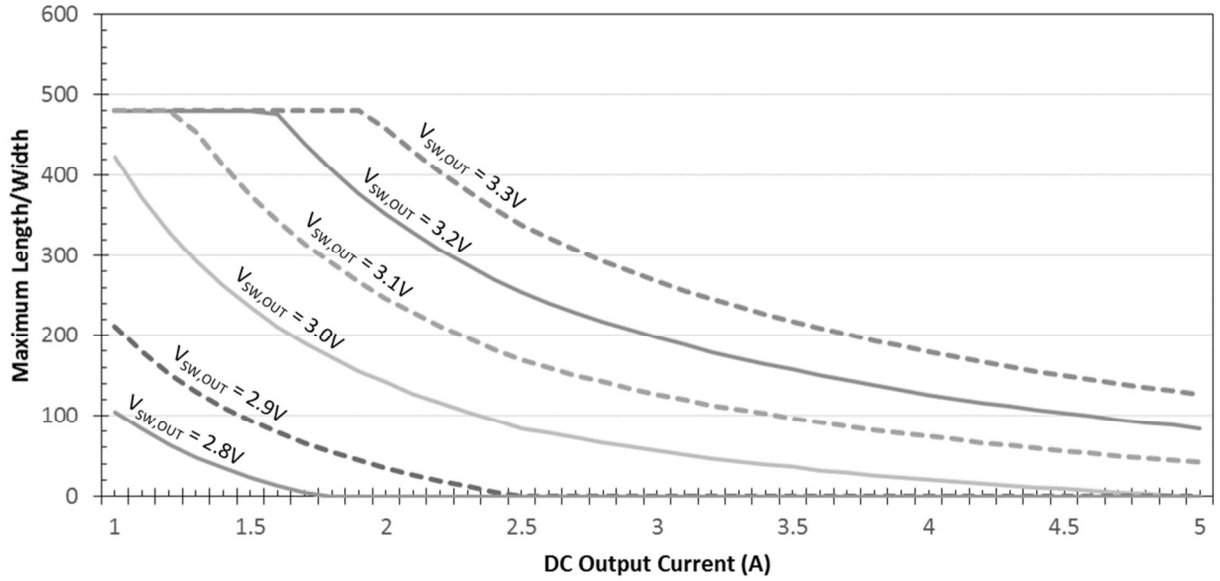


Figure 106 Design curves for maximum PTL (W/L) to support a specified DC output current

For a certain $V_{SW,OUT}$ value, the PTL can be properly sized according to these design curves such that the LDO will be able to output a proper regulated output voltage at peak DC current. The relevant system parameters are those given in Table 21. The input system voltage is 5V, the quiescent current of the LDO is 0.5mA, and the desired load voltage is 2.5V.

If the PTL is to be terminated, as shown in Figure 107, then the voltage drop across the termination resistor significantly affects the design.

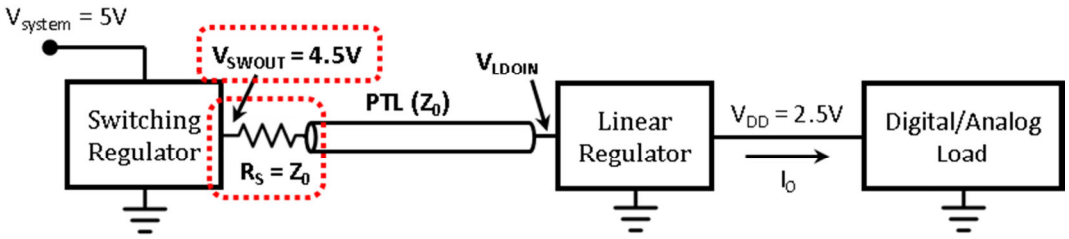


Figure 107 Power distribution network with a linear regulator powerd by a terminated PTL

It is shown in the previous sections that terminating the PTL reduces the voltage reflections on the line and suppresses cavity mode resonances. However, the voltage drop across

the terminating resistor places an addition constraint on the dimensions of the PTL. In Figure 108, the above simulation was repeated with a terminated PTL. In this case, the characteristic impedance of the PTL calculated for each of the PTL's length and width [47], and the power loss of the corresponding termination resistor is included into the power budget. For simplicity, the output of the switching regulator is fixed at 4.5V.

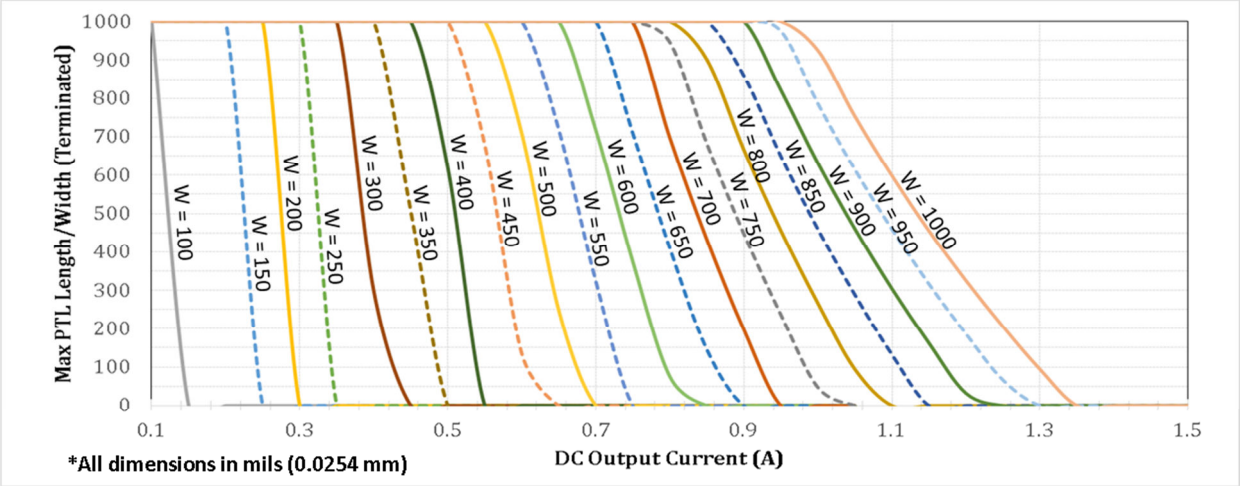


Figure 108 Design curves for maximum PTL (W/L) to support a specified DC output current when using a terminated PTL

One can see that this configuration has a limitation in the amount of DC current that is supported by the system. In order to support above 1A, the PTL must be designed to be very wide, to ensure a small Z_0, or very short. This is an inherent trade-off of this PTL implementation.

6.3 Summary

In this chapter, the feasibility of using a power transmission line to connect a switching regulator and a linear regulator is investigated with regard to power efficiency. Although a complete design methodology has not been developed, simple power efficiency calculations

show that the resistive loss of the PTL can be a major factor in the operation of the circuit. In order to maintain the highest possible efficiency, the input and output voltages of the low dropout regulator should be kept close. However, in a complex power distribution network, it may not always be possible to keep the power management circuitry and the load close to each other. Consequently, if the power trace connecting to the regulators or the load is long, then great care must be taken to ensure that the DC drop across that trace does not violate the dropout voltage of the LDO. When operating at high output currents, the input to the LDO can drop below the minimum input as dictated by the dropout voltage. In this case, the LDO will not be able to generate a stable output voltage. A series of design curves are presented that can serve as an initial guideline for determining the maximum dimensions of the PTL to ensure proper operation.

CHAPTER 7: SUMMARY & FUTURE WORK

7.1 Conclusion

The rapid advancement of transistor technologies and system integration has pushed data rates in digital systems to multi-GB/s speeds and beyond. This trend poses significant challenges for signal and power integrity engineers, especially in the design of power delivery networks. Currently used PDNs suffer from channel bandwidth limitations, inter-symbol interference, crosstalk, impedance mismatches, and simultaneous switching noise (SSN). The IC's bond wires, lead frame, on-die power/ground grid, as well as the board-level power delivery network contribute to the parasitic inductance and resistance. In addition, power supply noise is also generated by the physical discontinuities that are encountered by forward and backward flowing currents on the signal and reference planes, such as via transitions, plane apertures, split planes, etc. For these reasons, supply noise, if not properly managed, can severely affect the voltage and timing margins in high speed digital systems. To mitigate the effects supply noise, the standard practice is to design the power distribution network (PDN) to have a very low self-impedance. However, this can be difficult to achieve due to cavity mode resonances and the aforementioned parasitic inductances.

In this dissertation, a new signaling scheme called Constant Voltage Power Transmission Line (CV-PTL) is presented. This PDN scheme provides power through a transmission line in place of a power plane while dynamically changing the impedance of the power delivery network to maintain a constant supply voltage at the power pin of the IC. This reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. The signaling scheme was extended to vertically-stacked 3D integrated circuits

(3D ICs). A integrated circuit was designed on a 0.18μm CMOS process that will allow for better performance than the board-level test vehicle.

In addition, the noise coupling between digital and RF components was investigated. A simple design for mitigating the coupling of power supply noise in mixed-signal electronics was presented. The proposed method uses a simple embedded bandstop filter that is easy to implement and takes less board space than an electromagnetic bandgap structure. The proposed methods show significant improvements in almost all performance metrics, such as power supply noise, jitter, and noise isolation, when compared to EBG.

Finally, this dissertation discusses the effect of implementing a power transmission line in a power distribution network composed of a switching regulator and a voltage regulator module. The effect of the DC conductor loss from the PTL is investigated in terms of power efficiency power efficiency. Consequently, recommendations are made on the design of the PTL to ensure proper operation and efficiency.

7.2 Contributions

1. **Constant Voltage Power Transmission Line -** A new power delivery network called constant-voltage power transmission line (CV-PTL) was presented. This signaling scheme provides power through a transmission line in place of a power plane while dynamically changing the resistance of the power delivery network to maintain a constant voltage at the power pin of the IC. Consequently, this reduces the effects of return path discontinuities and can improve the quality of output signal by reducing power and ground bounce. Two test boards were built, one with conventional power and ground planes, and the other with the PTL-based power delivery network. The test boards were measured with a PRBS input signal that was encoded using a bus inversion encoding scheme. The signal quality of the output waveform was measured and analyzed in the form of transition jitter as well as power supply fluctuation.

Measurements of transition jitter show that by using the CV-PTL configuration, the transition jitter can be reduced by up to 46% and the supply voltage variation can be reduced by up to 44.7% as compared to using a power plane, while also exhibiting significant power savings [19].

2. **CV-PTL in 3D ICs –** The CV-PTL signaling scheme was extended to 3D IC application with similar benefits in signal and power integrity. It was demonstrated through simulation that power supply noise worsens as one goes higher up in the stack of dies. However, by utilizing the CV-PTL concept in the PDN design of a 3-layer 3DIC system, the circuit showed considerable improvement in power supply noise and p-p jitter as compared to the conventional design approach. In the CV-PTL circuit, the transition jitter showed improvement of over 50% when comparing the transition jitter in each layer. In addition, the supply noise is reduced by 40-60% in each layer. In addition, the power consumption of the proposed PDN design was analyzed. The analysis showed that the CV-PTL scheme consumes less power than the typical method of using power planes for a random bit sequence. The results and analysis presented here confirm the validity and possibility of utilizing the CV-PTL design in power delivery networks for integrated 3D systems.

3. **Integrated LDO –** The switching resistor paths in the CV-PTL scheme function to modulate the impedance of the power delivery network to keep the voltage at the data driver's supply pin constant while allowing the current to change as needed. This behavior is similar to that of a linear voltage regulator. Consequently, the incorporation of a low dropout voltage regulator (LDO) in place of the resistor paths was investigated. A custom IC was designed with an LDO powering 6 parallel-connected I/O buffers using a 0.18μm CMOS process. This solution would allow the circuit to operate at much higher data rates than the CV-PTL test vehicle using off-the-shelf parts. Simulations were performed at 500MHz. At the time of this dissertation submission, the IC is still in fabrication, and will be returned in March 2015. Due to this, lab measurements could not be performed.

4. **Switching Noise Isolation Technique for Mixed Signal Systems –** This work presents a simple power delivery design for mitigating the coupling of power supply noise in mixed-signal electronics. A set of parallel digital buffers and a low noise amplifier (LNA) were powered by a power transmission line instead of a voltage plane. An embedded bandstop filter in the power transmission line significantly reduced the amount of coupled noise between the digital and RF supply voltage pins. In addition, source terminating the power transmission line provided good noise isolation with even lower supply noise. This comes at the cost of increased power consumption, as the supply voltage must be increased to compensate for the voltage drop across the termination. The proposed methods are easy to design, implement, and use much less space than an equivalent EBG structure. Test vehicles using these proposed methods, as well as using an EBG structure were fabricated and tested by measuring power supply noise, jitter, and noise isolation. The proposed methods showed up to 13dB decrease in coupled power as compared to the EBG. In addition, the measured supply noise decreased by 75% and the total jitter in the transmitted eye diagram improved by 23% using the proposed method.

5. **LDO Efficiency –** It was discussed in the previous sections that the merits of using the power transmission line scheme to reduce power supply noise in high speed digital systems. In many power distribution networks, a combination of switching and linear voltage regulators are used. The power efficiency of these systems is of primary importance, and therefore the effect of using a power transmission line in this system to connect the switching and linear regulator was investigated. The DC conductor losses of the PTL can not only affect power efficiency of the entire system, but can also affect the operation of the linear regulator module when supporting large currents. Consequently, a set of design curves are presented that can serve as an initial guideline for determining the maximum dimensions of the PTL to ensure proper operation and to maintain high power efficiency.

7.3 Contributions

7.3.1 Journals

[1] **Telikepalli, S**.; Zhang, D.C.; Swaminathan, M.; Keezer, D., "Constant Voltage-Based Power Delivery Scheme for 3-D ICs and Interposers," *Components, Packaging and Manufacturing Technology, IEEE Transactions on* , vol.3, no.11, pp.1907,1916, Nov 2013

[2] **Telikepalli, S**.; Swaminathan, M.; Keezer, D., "A Simple Technique for Power Distribution with Better Characteristics than Electromagnetic Bandgap Structures," Submitted to *IEEE Transactions on Components, Packaging and Manufacturing Technology.*

7.3.2 Conferences

[1] **Telikepalli, S**.; Swaminathan, M.; Keezer, D., "An Alternate Power Distribution Scheme with Superior Noise Suppression Characteristics than EBG," Electrical Performance of Electronic Packaging and Systems (EPEPS), 2014 IEEE 23rd Conference on ,Oct. 2014

[2] **Telikepalli, S**.; Swaminathan, M.; Keezer, D., "Minimizing Coupling of Power Supply Noise Between Digital and RF Circuit Blocks in Mixed Signal Systems," 2014 IEEE 64th Electronic Components and Technology Conference (ECTC), 27-30 May 2014

[3] **Telikepalli, S**.; Swaminathan, M.; Keezer, D., "Minimizing simultaneous switching noise at reduced power with constant-voltage power transmission lines for high-speed signaling," Quality Electronic Design (ISQED), 2013 14th International Symposium on , pp.714,718, 4-6 March 2013

[4] **Telikepalli, S**.; Sang Kyu Kim; Sung Joo Park; Swaminathan, M.; Youkeun Han, "Managing signal and power integrity using power transmission lines and alternative signaling schemes," 2013 IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS), pp.1,4, Feb. 27 2013-March 1 2013

[5] **Telikepalli, S**.; Swaminathan, M.; Keezer, D., "Minimizing simultaneous switching noise at reduced power with power transmission lines for high-speed signaling," 2012 IEEE 21st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), pp.29,32, 21-24 Oct. 2012

[6] Sang Kyu Kim, **Satyanarayana Telikepalli**, Sung Joo Park, Madhavan Swaminathan, David Keezer, Youkeun Han, "Implementation of Power Transmission Lines to Field Programmable Gate Array ICs for Managing Signal and Power Integrity ,"2013 IEEE International Symposium on Electromagnetic Compatibility (EMC), 5-9 Aug. 2013

[7] Zhang, David C.; Swaminathan, Madhavan; Keezer, David; **Telikepalli, Satyanarayana**, "Characterization of alternate power distribution methods for 3D integration," Electronic Components and Technology Conference (ECTC), 2014 IEEE 64th , vol., no., pp.2260,2265, 27-30 May 2014

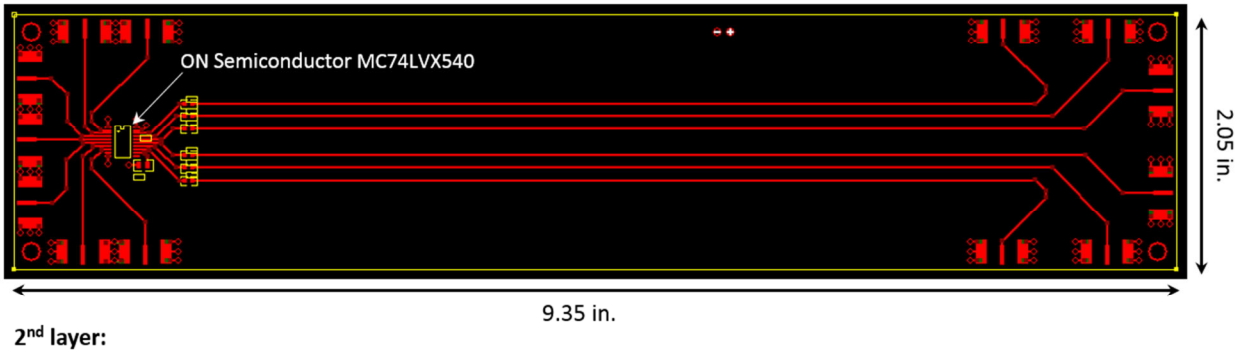
APPENDIX

Test Vehicle Schematics & Layouts

1. Power & Ground Plane Test Vehicle

    a. Layout

Top layer:



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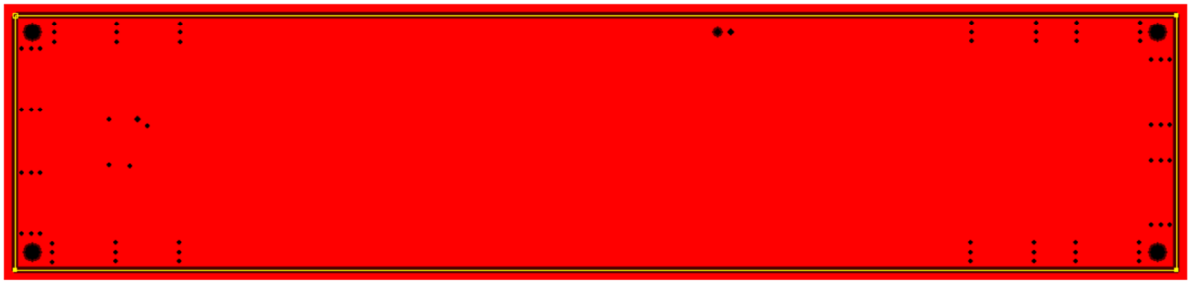

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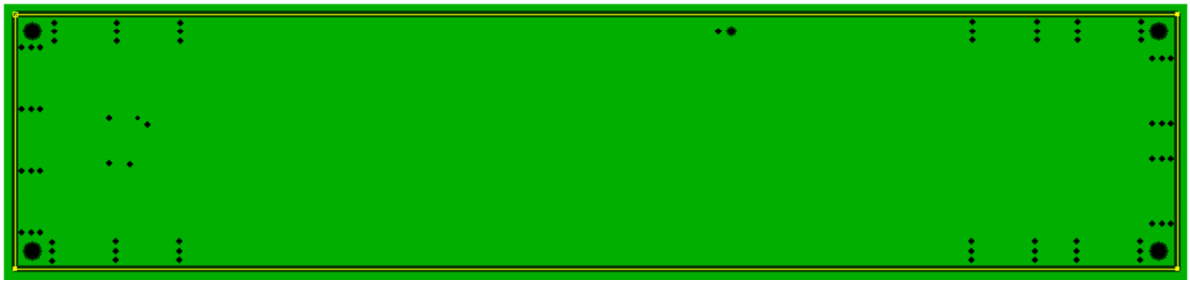
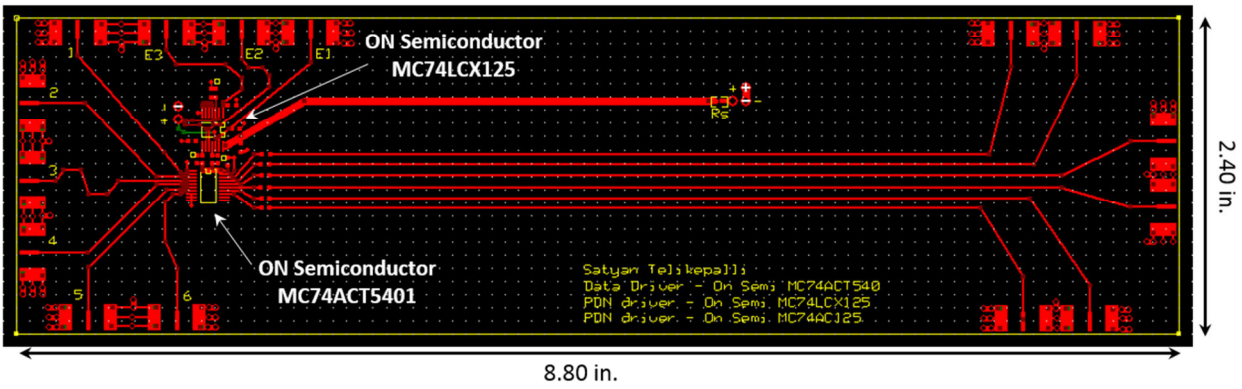


Test vehicle designed by Suzanne Huh

2. CV-PTL Test Vehicle

a. Layout

Top layer:



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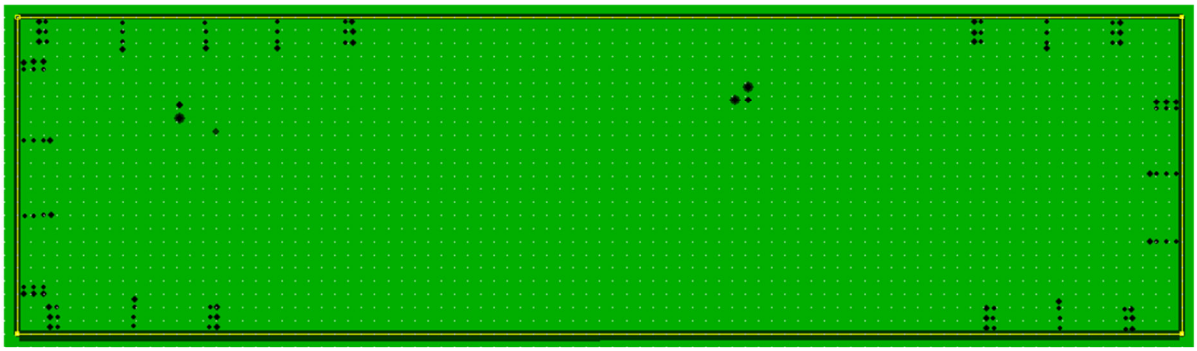

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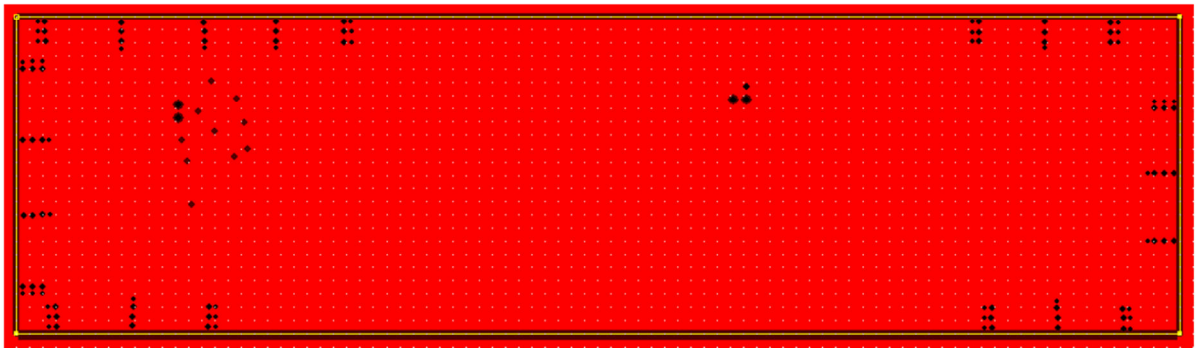
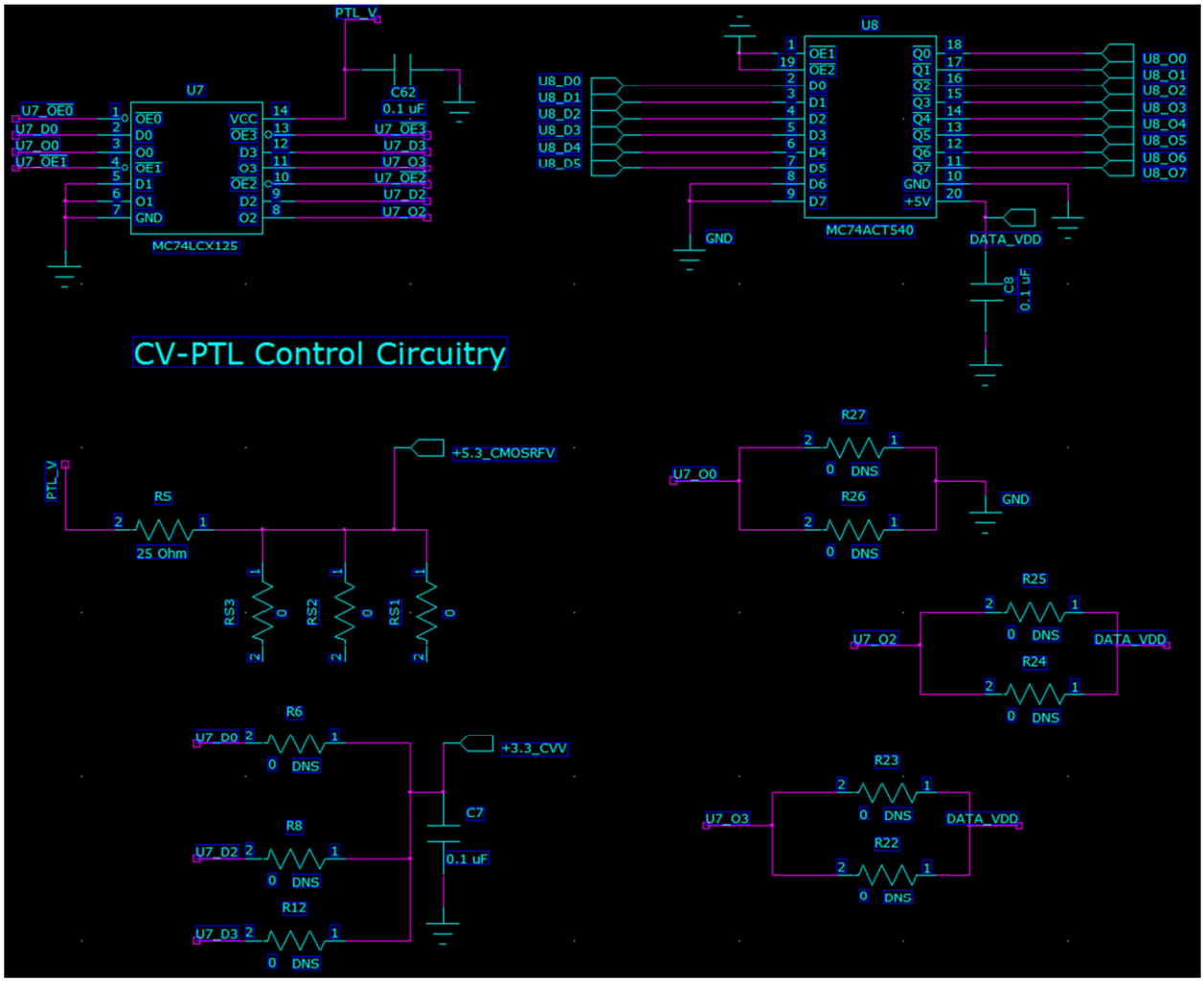
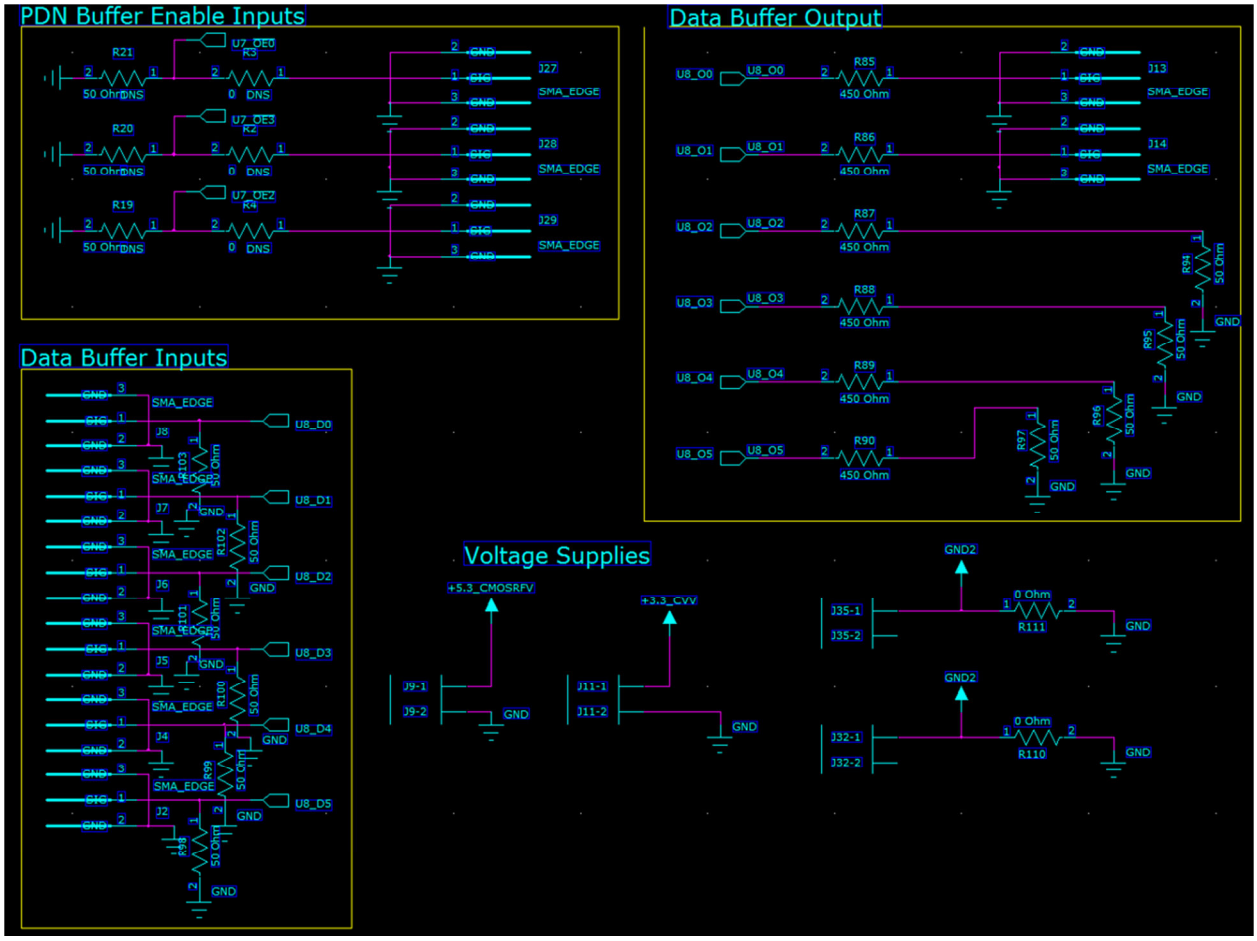


b. Schematic

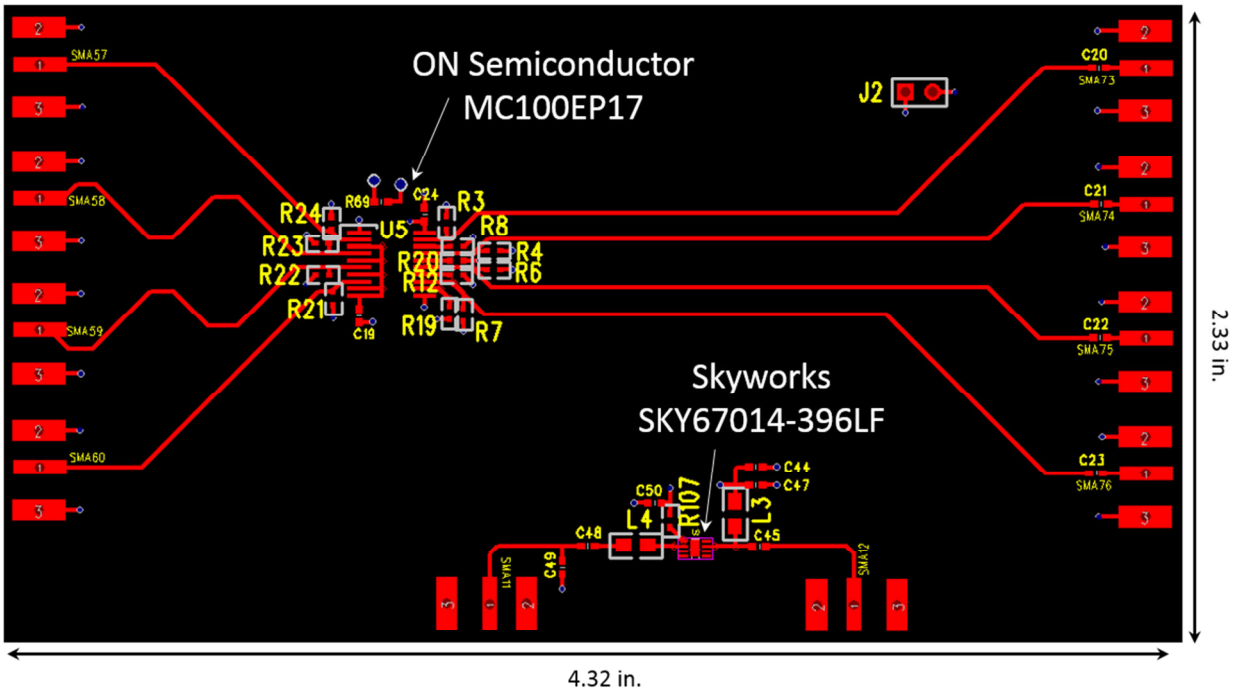

CV-PTL Control Circuitry
PTL_V
U7
U7_OE0
U7_D0
U7_O0
U7_OE1
OE0
D0
O0
OE1
D1
O1
GND
VCC
OE3
D3
O3
OE2
D2
O2
C62
0.1 uF
U7_OE3
U7_D3
U7_O3
U7_OE2
U7_D2
U7_O2
MC74LCX125
U8
U8_D0
U8_D1
U8_D2
U8_D3
U8_D4
U8_D5
OE1
OE2
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
GND
+5V
U8_O0
U8_O1
U8_O2
U8_O3
U8_O4
U8_O5
U8_O6
U8_O7
MC74ACT540
DATA_VDD
C8
0.1 uF
RS
25 Ohm
+5.3_CMOSRFV
RS3
RS2
RS1
R27
R26
U7_O0
DNS
GND
R25
R24
U7_O2
DATA_VDD
R6
R8
R12
U7_D0
U7_D2
U7_D3
+3.3_CVV
C7
0.1 uF
R23
R22
U7_O3


PDN Buffer Enable Inputs
Data Buffer Output
Data Buffer Inputs
Voltage Supplies
U7_OE0
U7_OE3
U7_OE2
R21
R20
R19
R3
R2
R4
50 Ohm DNS
0 DNS
J27
J28
J29
SMA_EDGE
GND
GND2
U8_O0
U8_O1
U8_O2
U8_O3
U8_O4
U8_O5
R85
R86
R87
R88
R89
R90
450 Ohm
J13
J14
R94
R95
R96
R97
50 Ohm
U8_D0
U8_D1
U8_D2
U8_D3
U8_D4
U8_D5
J8
J7
J6
J5
J4
J2
R103
R102
R101
R100
R99
R98
+5.3_CMOSRFV
+3.3_CVV
J9-1
J9-2
J11-1
J11-2
J35-1
J35-2
J32-1
J32-2
0 Ohm
R111
R110

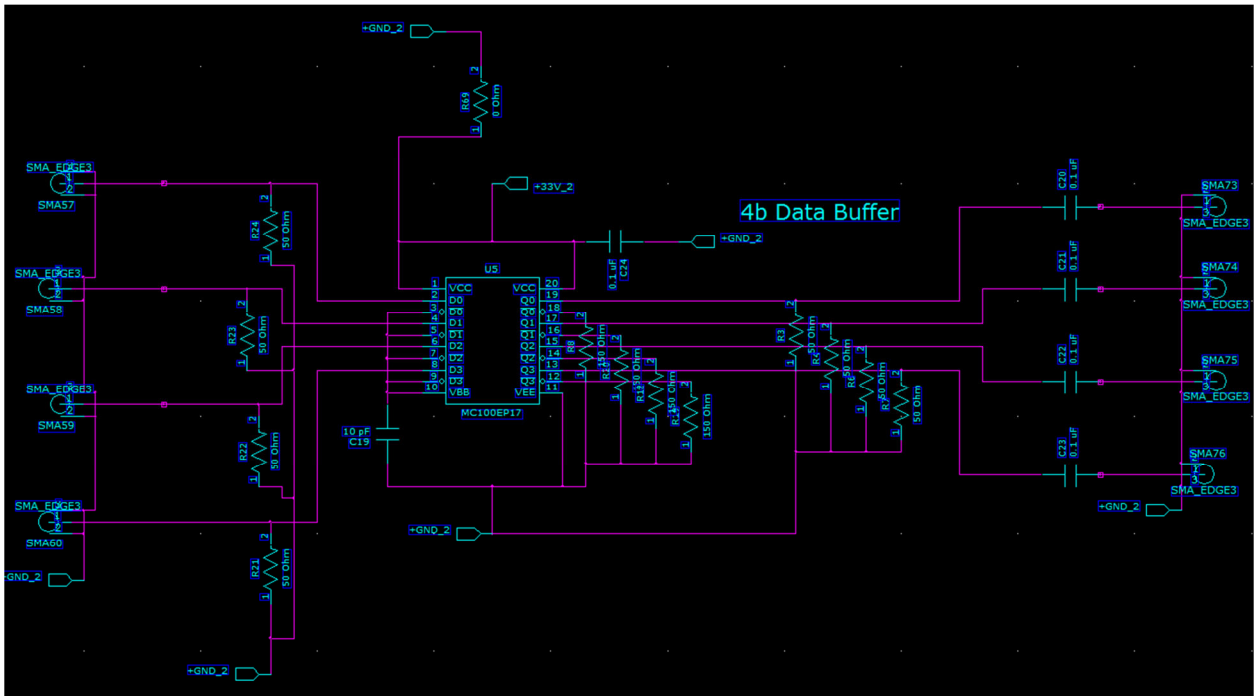
3. Noise Isolation Test Vehicles

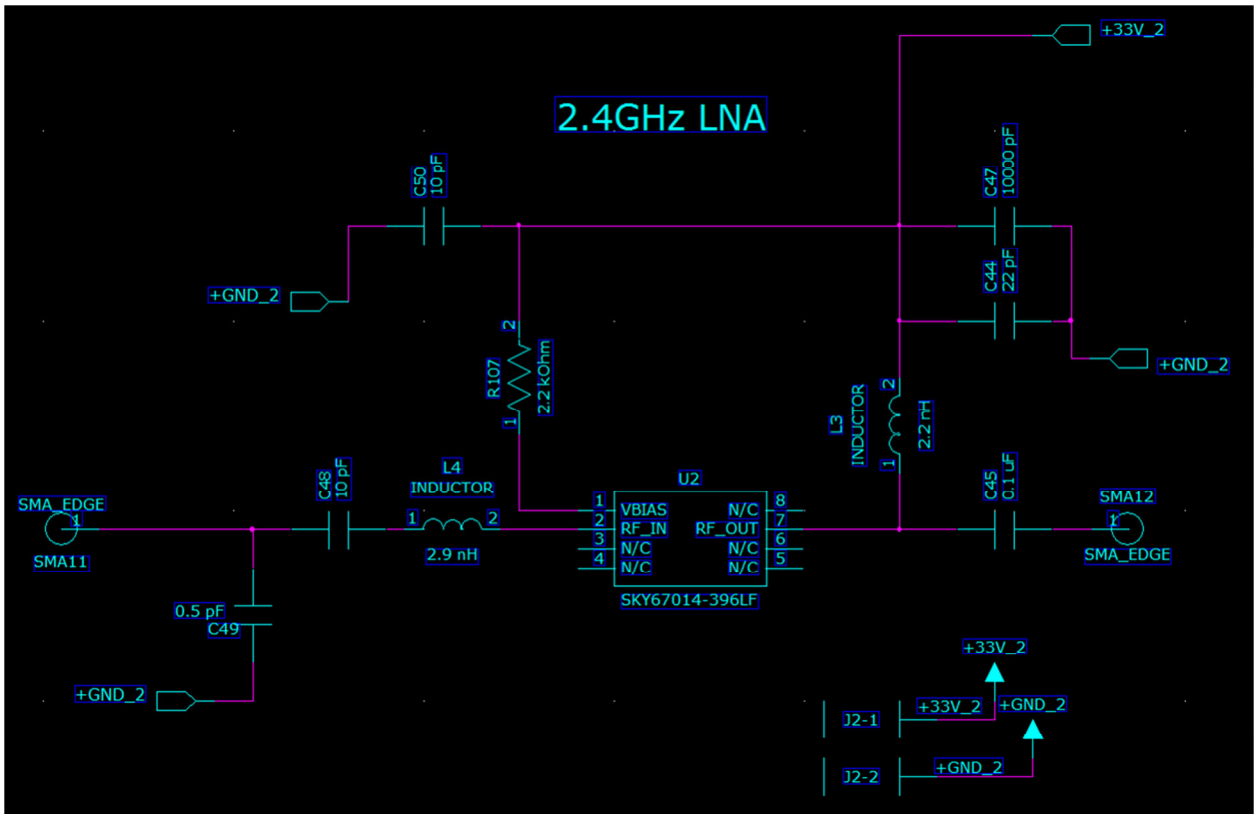
a. EBG Test Vehicle (TV1)

i. Layout



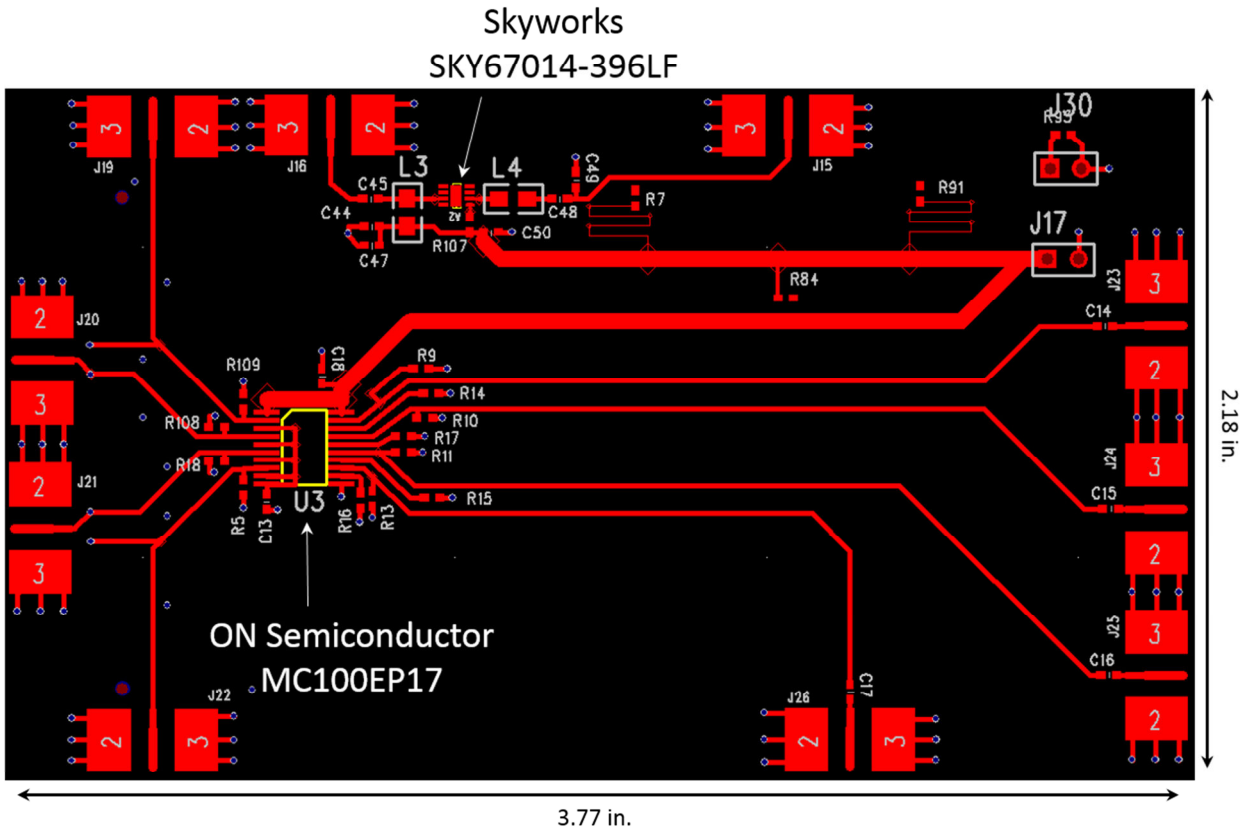
ii. Schematic



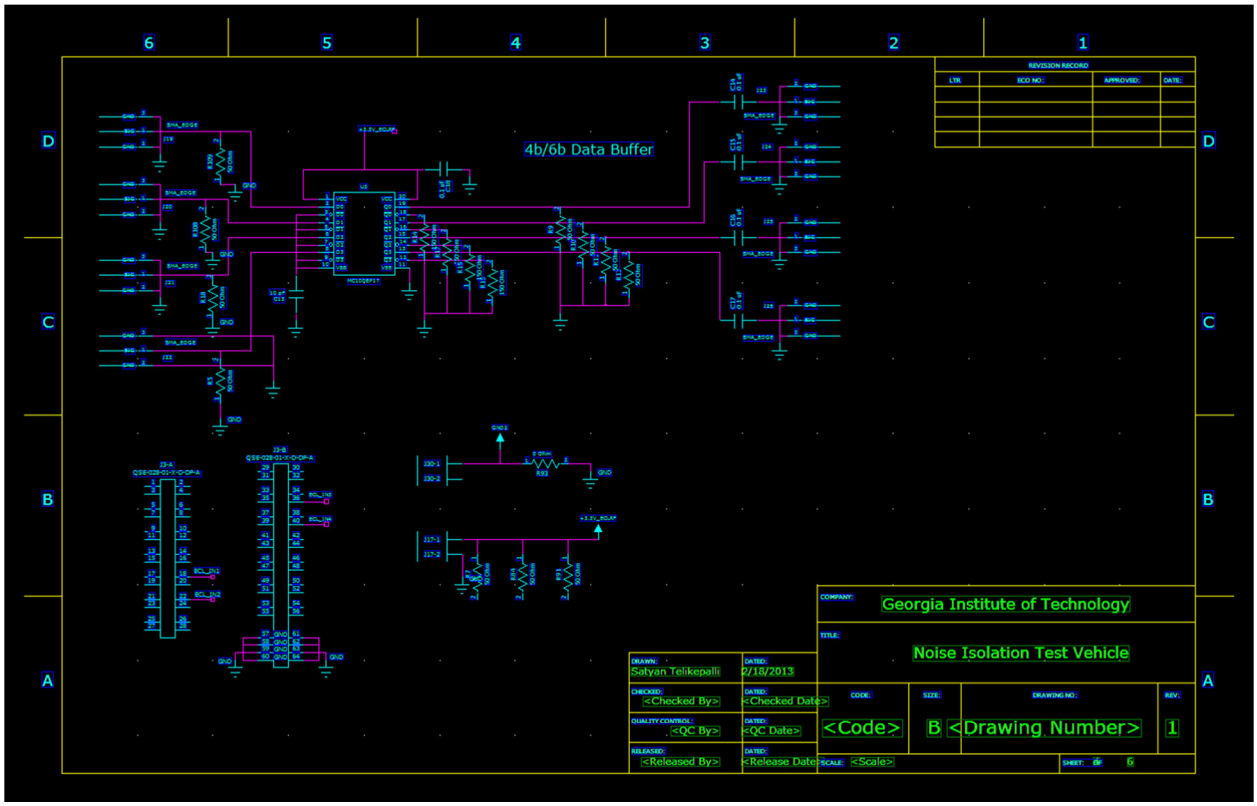


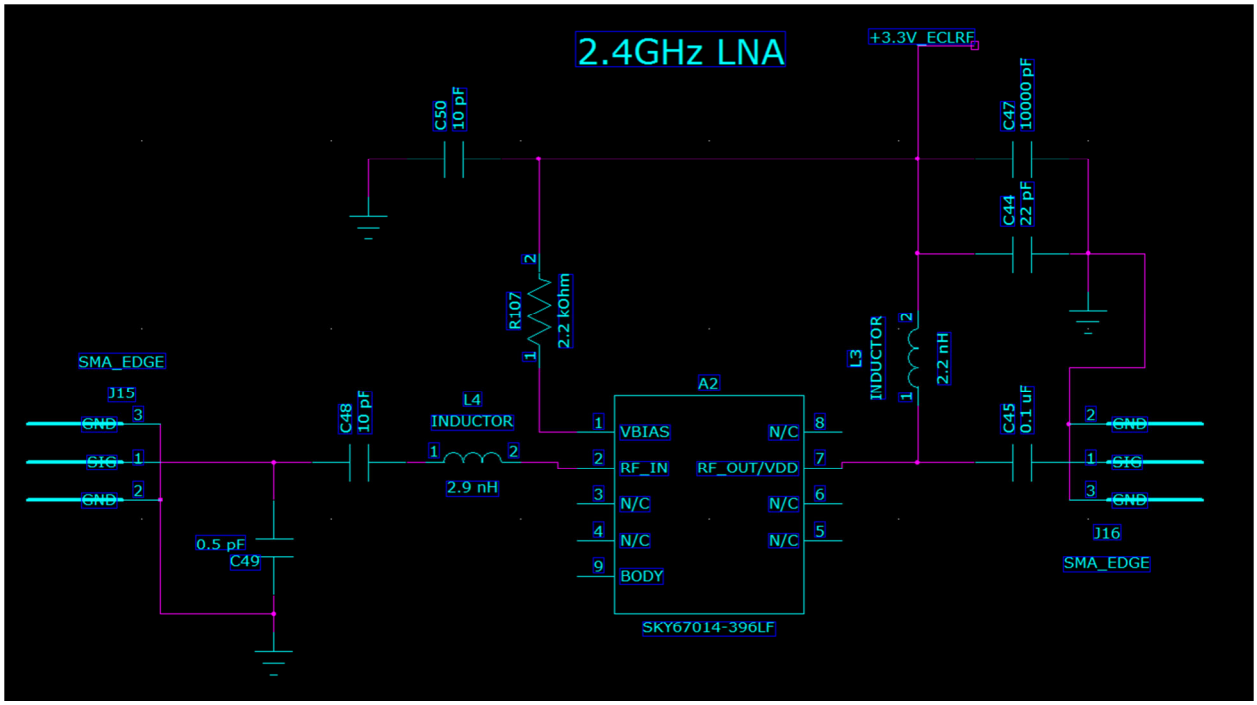
b. PTL w/ SSN Filter (TV2 in)

i. Layout



ii. Schematic





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