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Departament d'Enginyeria Electrònica

Voltage-Source Inverters with Legs Connected in Parallel

Thesis submitted in partial fulfillment of the requirement for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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Originality Statement

'I hereby declare that this submission is my own work and to the best of my knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at UPC or any other educational institution, except where due acknowledgment is made in the thesis. Any contribution made to the research by others, with whom I have worked at UPC or elsewhere, is explicitly acknowledged in the thesis. I also declare that the intellectual content of this thesis is the product of my own work, except to the extent that assistance from others in the project's design and conception or in style, presentation and linguistic expression is acknowledged.'

Signed:

Date: 30th January 2015

Dedicated to Reme, Esther and Vicente.

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Abstract

The number of applications that require the use of power converters has been continually increasing in the last years on account of environmental and economical concerns. The power to be processed by these converters has been growing too. These applications include uninterruptible power supplies, motor drives, and distributed generation, such as solar photo-voltaic panels and wind turbines. The rated power of such converters can be raised by increasing the output currents. This can be achieved by connecting converters, converter legs or power devices in parallel.

The connection of legs in parallel in a voltage-source inverter is made by means of inductors, which can be either magnetically coupled or uncoupled. One of the issues that needs to be addressed is achieving an even contribution to the output current from all the legs. Current imbalances are due to circulating currents among the legs which must be avoided or controlled since they produce additional losses and stress to the power devices of the converter. An efficient technique to attain such a balance is presented in this thesis. The balancing technique achieves the objective regardless of the type of inductors used.

In spite of the aforementioned issues, the potential benefits of paralleling converter legs make their use a worthwhile option. Some of the additional benefits of paralleling are the improvement in the total harmonic distortion of the output current and voltage and the reduction of the output filters. Besides, inverters with legs connected in parallel are modular and because of that, their production and maintenance become less expensive. Moreover, they qualify for the implementation of fault-tolerant techniques thus offering the possibility of achieving systems with improved overall reliability.

Interleaving of the carriers can be used to modulate the reference signals for each leg, which leads to a reduction in the output current ripple without resorting to increasing the switching frequency. A whole set of shifted carriers is required if interleaved pulse-width modulators are used. Implementing this by means of a digital signal processor (DSP) means that the higher the number of carriers, the higher the number of DSP timing resources required. Provided that the latter are usually limited, this could be a drawback when increasing the number of interleaved carriers. In this thesis the implementation of a pulse-width modulation (PWM) scheme where all modulators use the same carrier offering the same results as if a set of n interleaved carriers were used is presented.

Since the proposed algorithm takes maximum benefit from the PWM units available in a DSP, a higher number of legs connected in parallel can be controlled without adding any external processing hardware.

In multiphase voltage-source inverters with n interleaved parallel-connected legs, the best single-phase output voltage is achieved when the carriers are evenly phase shifted. However, switching among nonadjacent levels can be observed at regular intervals in the line-to-line voltages, causing bad harmonic performance. This thesis includes a novel implementation of PWM that improves the quality of the line-to-line output voltages in interleaved multiphase voltage-source inverters. With the proposed method, switching in the line-to-line voltages happens exclusively between adjacent levels. The modulator utilizes two sets of n evenly phase-shifted carriers that are dynamically allocated. Because of its generality, the proposed implementation is valid for any number of phases and any number of legs in parallel.

All the modulation and control algorithms proposed in this thesis have been firstly simulated on Matlab/Simulink models, and then experimentally corroborated on a low-power laboratory prototype.

Contents

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List of Acronyms

Acronym	*Definition*
ac	Alternating current
ADC	Analog to digital converter
APOD-PWM	Alternative phase opposition disposition pulse-width modulation
CB-PWM	Carrier-based pulse-width modulation
dc	Direct current
DEE	Departament d'Enginyeria Electrònica
DSP	Digital signal processor
DVR	Dynamic voltage restorer
EM	Event manager
EMI	Electro-magnetic interference
FPGA	Field programmable gate array
I/O	Input/Output
LS-PWM	Level-shifted pulse-width modulation
MOSFET	Metal-oxide semiconductor field-effect transistor
MAF	Moving-average filter
MMC	Modular multilevel converter
NP	Neutral point
NPC	Neutral point clamped
PC	Personal computer
PD-PWM	Phase-disposition pulse-width modulation
PI	Proportional integral
POD-PWM	Phase-opposition disposition pulse-width modulation
PS-PWM	Phase-shifted pulse-width modulation
PWM	Pulse-width modulation

S&H	Sample and hold
SHE-PWM	Selective harmonic elimination pulse-width modulation
SPWM	Sinusoidal pulse-width modulation
STATCOM	Static compensator
SVM	Space-vector modulation
SV-PWM	Space-vector pulse-width modulation
THD	Total harmonic distortion
TIEG	Terrassa Industrial Electronics Group
ULA	Upper and lower arms
UPC	Universitat Politècnica de Catalunya
VOC	Voltage oriented control
VSC	Voltage-source converter
VSI	Voltage-source inverter
WTHD	Weighted total harmonic distortion

List of Symbols

Symbol	Definition
$\vec{a}$	$j\frac{2\pi}{3}$
C	Capacitor
dv/dt	Derivative of voltage with respect to time
d_k	Duty cycle of a voltage vector in SV-PWM
e_d	d-component of the grid voltages in a synchronous reference frame
e_q	q-component of the grid voltages in a synchronous reference frame
e_x	Grid voltage, x being the phase identification
f_c	Carrier frequency
f_r	Reference signal frequency
f_s	Apparent switching frequency
f_{sw}	Switching frequency
i_d	d-component of the grid current in a synchronous reference frame
i_d^*	i_d reference
i_q	q-component of the grid current in a synchronous reference frame
i_q^*	i_q reference
i_x	Phase current, x being the phase identification
I_M	Amplitude of the current
$I_{\text{P-P}}$	Peak-to-peak value of the current
L	Inductor
L_g	Grid inductor
L_{eq}	Equivalent inductor
L_L	Load inductor
m_a	Amplitude modulation index
m_f	Frequency modulation index

M	Mutually coupling inductance
n	Number of legs connected in parallel
(n)	Neutral point of the grid
N_x	Number of turns in winding x
R	Resistor
R_p	Parasitic resistor
R_L	Load resistor
$\Re$	Magnetic reluctance
s_{xy}	Switch control function of a VSI, x being the phase identification and y, the leg identification
sel_y	Selection signal of a two-channel multiplexer y being the identification of the multiplexer
t	Time
t_k	Dwelling time per switching period of a voltage vector
T	Fundamental time period
T_s	Apparent switching period
T_{sw}	Switching period
$v_{carr\,x}$	Carrier voltage, x being the carrier identification
v_{x0}	Phase voltage with respect to the neutral point, x being the phase identification
v_{xy}	Voltage of the y-leg in x-phase with respect to the neutral point
$v_{x\mathrm{COM}}$	Thevenin equivalent phase voltage of n paralleled legs x being the phase identification
v_0	Zero sequence voltage
$\vec{v}$	Voltage vector
V_{C1}, V_{C2}	Voltage across the dc-bus capacitors
V_{dc}	Voltage of the dc-bus
V_{dc}^*	Reference voltage of the dc-bus
$\hat{V}_{SV-PWM}$	Maximum achievable voltage with SV-PWM
$\hat{V}_{SPWM}$	Maximum achievable voltage with SPWM
$\hat{V}_{\mathrm{REF}}$	Maximum amplitude of the reference voltage
x	Phase identification, where $x = \{a, b, c\}$
z_{refxy}	Voltage reference zone code for x-phase and y-leg

$\Delta v_{x\,y}$	Incremental control voltage for x-phase and y-leg
$\bar{x}$	Locally averaged value of magnitude x
Φ	Magnetic flux
θ	Grid voltage angle
ω	Angular frequency

Chapter 1

Introduction

This chapter presents the context of this research work and the motivation to approach it. It includes a review of the research previously carried out on modulation techniques and carriers' disposition. The chapter also states the main objectives of this thesis, including the publications derived from it. To conclude, the thesis outline and the main contributions are presented.

1.1 Research Environment

The present thesis has been developed in the Departament d'Enginyeria Electrònica (DEE) of the Universitat Politecnica de Catalunya (UPC) within the Terrassa Industrial Electronics Group (TIEG). The main interests of the research group are:

- Electro-magnetic compatibility: Electro-magnetic interference (EMI) modeling, diagnostic and mitigation techniques for industrial environments, in vehicles, ships and aircrafts.
- Renewable energy: Modeling and design of power converters for wind and photovoltaic (PV) systems.
- Power quality in electric systems: Measuring and correction of power supply disturbances in the generation and distribution system.
- Control techniques for electric drives: Advanced techniques for matrix converters and multilevel converters.
- Modeling and mitigation techniques for EMI in the range of radio frequency and microwaves.

This work is part of the activities in the RURALGRID and CONNECT-DC (ENE2012-36871-C02-01) projects.

The RURALGRID project, *Feasibility study in order to introduce renewable energies by means of microgrids in the Pyrenees Area* was developed under the Comunidad de Trabajo de los Pirineos (CTP) frame, involving research groups from Aragón (Universidad San Jorge and INYCOM), Euskadi (Universidad del País Vasco/Euskal Herriko Unibertsitatea, Tecnalia Research & Innovation, and Jema Energy), Catalunya (UPC), Aquitaine (École Supérieure des Technologies Industrielles Avancées, IMS Bordeaux, and LOREKI), and Midi-Pyrénées (École Nationale d'Ingénieurs de Tarbes). In the case of Catalunya, the project was supported by the Secretaria d'Universitats i Recerca of the Departament d'Economia i Coneixement of the Generalitat de Catalunya. The RURALGRID project was devoted to study the feasibility of implementing micro-grids in the Pyrenees area. New technologies were also analyzed to improve the energy efficiency of micro-grids and distributed generation systems. One of the goals of this project was to improve the control and parallelization of power electronic converters comprising a micro-grid, and to optimize the quality of voltages and currents.

The CONNECT-DC project, *Topologies and control of power electronic converters for offshore high voltage dc energy transmission*, funded by the Ministerio de Economía y Competitividad (MINECO) of Spain is a collaboration between two research groups: one of Tecnalia Research and Innovation and the other from the UPC. The CONNECT-DC project is devoted to analyze a medium voltage dc transmission architecture for offshore applications. The main feature of this architecture lies in the fact that the ac to dc current transformation is not located in an offshore platform but it is distributed in each of the wind turbines. This way, it is possible to eliminate or, at least, significantly reduce, the size of the offshore platform thus reducing the costs of the transmission system. Other targets of this project are the development of control algorithms for wind turbine generators in order to optimize the energy conversion efficiency, the characterization of the wind resources, and the development of control strategies for the medium voltage dc/ac onshore grid-connected power converters, including, but not limited to, the modular multilevel converter (MMC). Another of the objectives of this project is to investigate the possibility of connecting converter structures in parallel in order to deal with higher current levels of the generation systems. The use of interleaved modulation strategies is implemented in order to obtain high quality voltage and current waveforms. This objective is fulfilled with the results obtained in the present thesis.

1.2 Research Motivation

Significant electrical grid changes are being produced nowadays. Distributed generation systems are becoming more and more common; thus, huge central stations are starting to share electricity production with such distributed systems. Many of those generation devices require to process voltages and currents through power electronic converters for a proper grid connection. Some examples include renewable energy systems; e. g. solar PV, wind turbines, and marine energy [1–4]. Other promising generation sources are fuel cells. Some other systems that require grid-connected converters are energy storage applications and power quality devices, such as active filters, static compensators (STATCOMs), or dynamic voltage restorers (DVRs).

As the power to be processed increases, it also does the rated power of the power electronics converters required. When it comes to increasing the rated power of a voltage-source converter (VSC) either voltages, currents, or both can be raised. Increasing the voltages handled by the converter is usually done by resorting to multilevel converters [5–8]. The main reason for this is because they can deal with higher voltages that are shared among a higher number of semiconductor switches.

On the other hand, paralleling switching devices, legs, or even converters are different ways to increase the output current values [9–17]. An advantage that deserves to be mentioned concerning this second approach is the fact that converters may be kept in the low-voltage range and, therefore, under the low-voltage regulations, which are less demanding than medium-voltage regulations. Furthermore, combining both alternatives, i.e. extending the topology of legs connected in parallel to multilevel converters would help achieve systems capable of handling really large amounts of power [18].

The modulation of a voltage-source inverter (VSI) with legs connected in parallel requires the use of a specific modulator for each leg. Therefore, as many modulators as parallel-connected legs are needed. Given the fact that the number of timing resources or pulse-width modulation (PWM) modules available in a standard digital signal processor (DSP) is limited, and that it is quite common for each PWM module to use just one carrier signal, the possibility of using several interleaved carriers is seriously hindered. The implementation of modulation schemes able to modulate the corresponding reference signals for n parallel-connected legs by making the most of the limited timing resources of a DSP is something that deserves to be researched on.

Converters with legs connected in parallel can produce more than two voltage levels at the outputs. The type of modulation has a crucial influence on the quality of the output voltage and its waveform. Standard modulation strategies based on phase-shifted PWM (PS-PWM) cannot render optimal line-to-line voltages. The disposition of the

carriers should then be modified in order to improve the quality of the line-to-line output voltages.

This thesis is an attempt to contribute to all these topics.

1.3 Review of Previous Research

1.3.1 Modulation of VSIs with Legs Connected in Parallel

In order to connect several phase-legs of a VSC in parallel, inductors are the passive components to be used [19–24]. They not only qualify for averaging the voltage from several legs to form the output voltage, but also for limiting circulating currents among the phase legs. Because of the averaging, the Thevenin equivalent output voltage of the phase would have more than two levels. The maximum number of voltage levels is $n + 1$, n being the number of legs connected in parallel [17, 25].

Making sure that the output current is evenly shared among the legs connected in parallel is an important issue [26]. It would be optimal if current sharing among the legs were balanced; however, there is no guaranty for this to happen unless a proper control is used. A great variety of techniques can be applied to reach a balanced distribution of current among the legs. Most of them are based on proportional-integral (PI) controllers and they usually include two control loops: one to control the output voltage and another one to regulate the current sharing [11–13, 27–31]. Optimal regulators are used in [32–34] in order to create robust feedback control systems or robust droop controllers [35, 36], whereas a sliding control is proposed in [37], in spite of the serious drawback of leading to a variable switching frequency, albeit limited. By and large, all the considered methods provide good balancing performance on the whole. However, all of them need some parameter tuning and the balancing dynamics may not be optimal. Quick response of the balancing control is crucial to avoid long transitory over-currents on specific legs which might be destructive. The method presented in [38] aims to balance active currents by changing the carrier frequency at any switching cycle. Yet again, a specific parameter has to be properly adjusted to achieve optimal performance. In [25] a current-balancing strategy capable of achieving current balance very quickly is presented. The exact modification of the modulation signals is calculated and applied. The method is performed without distorting either the output voltages or the currents.

Since systems using paralleled legs are modular, their production and maintenance become efficient hence less expensive. Moreover, fault-tolerant techniques can be implemented in these modular systems offering high overall reliability [39–41].

A study on several PWM algorithms for three-phase interleaved converters is performed in [42], proving sinusoidal PWM (SPWM) to be more advantageous than space vector PWM (SV-PWM) in interleaved applications. Using a carrier-based PWM (CB-PWM) scheme in multilevel converters requires the use of several level-shifted carriers, even when no interleaving is implemented.

The analysis of PWM schemes has been a wide research area for decades. This analysis is usually carried out by digital simulation of the switched output waveform and subsequent fast Fourier transformation FFT or assessment of a specific performance index, except for a limited number of specific modulation strategies whose analytical solution can be found [43]. In [44] and [45], different multi-carrier PWM strategies for multilevel inverters are studied and compared. After comparing the analytical solutions for PS-PWM of cascaded inverters, the phase-opposition disposition PWM (POD-PWM), and the alternative phase-opposition disposition PWM (APOD-PWM) strategies, the authors conclude that the quality of the output voltages of PS-PWM and APOD-PWM techniques can be made to be the same when the carrier frequencies are adjusted to achieve the same number of total switch transitions over a fundamental cycle. They also demonstrate that phase-disposition PWM (PD-PWM) achieves a superior line-to-line performance. From this understanding, they develop an equivalent PD-PWM with phase-shifted carriers within each bridge of the cascaded inverter. Such a strategy for a hybrid multilevel inverter is implemented in a way that only one carrier (or its phase-opposite one) is used. The concept presented there requires the use of discontinuous modulation. For a cascaded multilevel inverter operating under discontinuous modulation, the reference waveform is split into sections and each cascaded inverter synthesizes a different section of the main reference waveform. Therefore, it is a level shifting strategy which, instead of using multiple level-shifted carriers, uses a modified reference signal that is held to a constant value when the actual reference signal moves beyond the boundaries of its region. Even although the implementation of a level-shifted multi-carrier PWM scheme for a multilevel cascade inverter with just one carrier leads to a slightly more complex modulation process, the discontinuous nature of the PWM pattern makes the process straightforward for a digital modulator. The idea of using a single carrier and several level-shifted modulating signals used to implement a non-interleaved PWM scheme for cascaded multilevel VSCs has been developed in [46] and [47].

Another way of achieving multilevel output voltage waveforms in a two-level VSI is the use of interleaved parallel-connected legs. However, in such a type of inverters, PD-PWM cannot be applied in a straightforward way, as it would cause huge circulating currents; therefore, PS-PWM should be used instead. While the reduction of a whole

set of level-shifted carriers to only one carrier can be easily implemented, the reduction of a set of phase-shifted carriers to only one carrier is not that simple. A novel implementation that accomplishes the goal is presented in Chapter 4.

Some space-vector modulation (SVM) approaches for converters with multiple legs in parallel are presented in [48] and [49]. In both of them the current sharing control and the converter output control are decoupled by the SVM. A study of the modulation is performed in [48]; however, in order to simplify its practical implementation, the current sharing control is carried out with a hysteresis controller. In [49], a dual-modulator compensation technique for eliminating the zero-sequence circulating current caused by power sharing control systems is proposed.

When connecting VSIs in parallel to create a local net, it is quite common that each inverter uses its own reference signal and its local controller. Owing to the fact that phase, frequency and amplitude have to be the same in order to minimize circulating currents, some kind of synchronization has to be included either providing communication lines among them [41, 50] or a self-synchronizing mechanism [26, 51].

The limitations in order to achieve a proportional load sharing in a conventional droop control scheme are revealed in [35, 52], and modified robust droop controllers are presented, notwithstanding the trade-off between voltage drop and sharing accuracy when the load voltage is not accurately measured. The multilayer control based upon a modified droop control presented in [53] allows for the parallel operation of inverters without intercommunications.

A method that avoids the use of intermodule inductors in three-phase parallel-connected inverters is presented in [54]. The proposed method compares the actual and the desired current value for each converter. The error signal is utilized by a PI compensator to provide the modulation index to a space-vector modulator. The control method divides the switching cycle evenly between the equally rated converters. Accordingly, the intermodule inductors become redundant.

An analytical model for a parallel-connected inverter system is developed in [38]. The internal Thevenin impedance of inverters is identified as the sensitive element affecting current distribution. An active control strategy to tune the effective Thevenin impedance by using a resistor emulation approach is developed. The proposed method relies on tuning the carrier frequency at any single switching cycle. Yet again, a parameter has to be adjusted properly to guarantee the stability of the system.

A very challenging modulation strategy applied to a 22MW/27-MVA machine test bench is presented in [55]. The 27-MVA rating for a variable frequency driver is

achieved by paralleling two three-level neutral-point-clamped (NPC) integrated-gate-commutated-thyristor. A specific modulator based on PD-PWM is designed to meet, among others, the following requirements: control of the circulating currents between the paralleled legs, thermal stress balancing of the paralleled converters, and balancing of the neutral-point (NP) voltage. The circulating current, the thermal balancing and the NP balancing can be regulated simultaneously. As each inverter can generate three different output voltage levels, the overall output of the paralleled system shows up to five different levels. Some of these levels can be achieved by two different ways (the so-called redundant states) that differ in the individual output level of each NPC inverter. The selection of one or another of the redundant states to generate a specific voltage output level deeply influences the circulating current and the thermal and NP voltage balance. The control algorithm has then to predict and prioritize which of the three regulating magnitudes needs a faster control action.

The modulation technique known as selective harmonic elimination PWM (SHE-PWM) aims to obtain an output voltage waveform from the inverter where some harmonics, usually the ones harder to filter, are canceled. The angles at which switching should happen are calculated off-line, correlating the selected harmonics to be eliminated [56–58]. The implementation of interleaved SHE-PWM in converters with legs in parallel creates additional difficulties in keeping circulating currents under control, as it reduces both the number and continuity of the possible solutions. A compromise is required between the number of output voltage levels and the maximum number of harmonics that can be minimized [59].

The connection of legs in parallel to increase the current ratings and, hence, the overall power handling capability is also applied to MMCs in [60]. Consequently, each phase of the MMC is integrated by several legs or sets of upper and lower arms (ULAs). This paper proposes a current-control strategy for each ULA in order to ensure a balanced current-sharing among them. In addition, each ULA has its own circulating-current control which follows a reference obtained from the instantaneous magnitudes of the output current and the modulation signal.

1.3.2 Disposition of the Carriers

Modulation strategies can be classified in several ways [61–64]. Their effect on the harmonic spectrum has been largely investigated, specially the multilevel H-bridge cascaded topologies [63, 65–67]. An overview of the different modulation alternatives is presented in Chapter 2. Various multi-carrier PWM techniques suitable for high power converter structures and capable of generating multilevel output voltage waveforms are discussed

in [9]. The performance of the various techniques with respect to the total harmonic distortion (THD) of the output voltage in the linear and over-modulation regions is reported.

The mathematical analysis of PS-PWM modulation for MMC is performed in [68] in order to identify the PWM harmonic characteristics of the output voltage and the circulating current. Moreover, the influence of the carrier-displacement angle between the ULAs on these harmonics is also studied. Using this analysis, the optimum displacement angles are specified for the output voltage harmonics minimization and the circulating-current harmonics cancellation, respectively. The harmonic features of the line-to-line voltage and the dc-link current are also investigated in [68].

In CB-PWM, interleaving is implemented by using the same number of carriers as the number of legs connected in parallel [25, 69]. In order to achieve optimal output voltage and current spectra, the carriers should be evenly time-shifted within a switching period [63, 70]. This technique is known as PS-PWM. It is well-known that in terms of THD of the line-to-line voltages, level-shifted carrier modulators behave much better than phase-shifted carrier modulators [44, 71]. However, level-shifted PWM (LS-PWM) techniques cannot be applied directly to converters with legs connected in parallel. The reason why is because as each carrier is usually associated to one leg, only the leg linked to the carrier that is in the same zone as the reference signal would be switching. The remaining legs would be clamped to either the positive or the negative dc-link voltage, depending on the relative position of their reference signal. This process would produce extremely large circulating currents at the fundamental frequency since the impedance of the limiting inductors is very low at that frequency [20, 21]. Furthermore, dc voltage components would also appear across the inductors, producing extremely large dc circulating currents, only limited by the voltage drops in the semiconductors and parasitic resistors. Therefore, further research can be performed on the disposition of the carriers in converters with legs connected in parallel.

1.4 Thesis Objectives

The main objectives of the thesis are to develop:

- A current-balancing method for interleaved VSIs with legs connected in parallel. The balancing method will be applicable regardless of whether the legs are linked by means of magnetically coupled or uncoupled inductors. It will not require any parameter tuning.

- A modulation scheme for VSIs with legs connected in parallel that can produce interleaved modulation for n legs by using only one carrier instead of the n carriers utilized in a standard implementation. Such an implementation of the modulator will aim to fully exploit the timing resources of the DSP and to maximize the number of legs that can be paralleled for a specific number of DSP timers.
- An optimal disposition of the carriers in a PS-PWM scheme that can improve the quality of the output voltage in order to achieve THD values close to the ones achievable with a LS-PWM scheme.

1.5 List of Publications

The following papers are a result of the research developed in this thesis and have been published in different conferences and journals.

1.5.1 Journal Papers

The following journal papers have been published or are already accepted for publication:

[1] J. Pou, J. Zaragoza, G. J. Capellá, I. Gabiola, S. Ceballos, and E. Robles, "Current balancing strategy for interleaved voltage source inverters," *EPE Journal*, vol. 21, no. 1, pp. 29–34, Jun. 2011.

[2] G.J. Capellá, I. Gabiola, J. Pou, S. Ceballos, J. Zaragoza, and V.G. Agelidis, "Minimum signal modulation scheme based on a single carrier for interleaved operation of parallel phase legs in voltage source converters," *IET Power Electron.*, vol. 7, no. 5, pp. 1305-1312, May 2014.

[3] G.J. Capellá, J. Pou, S. Ceballos, G. Konstantinou, J. Zaragoza, and V.G. Agelidis, "Enhanced phase-shifted PWM carrier disposition for interleaved voltage-source inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1121–1125, Mar. 2015.

[4] G.J. Capellá, J. Pou, S. Ceballos, G. Konstantinou, J. Zaragoza, and V.G. Agelidis, "Current balancing technique for interleaved voltage source inverters with magnetically-coupled legs connected in parallel," *IEEE Trans. Ind. Electron.*, early access, DOI: 10.1109/TIE.2014.2345345.

1.5.2 Conference Papers

The following papers have been presented in international conferences:

[5] J. Pou, J. Zaragoza, G. J. Capellá, I. Gabiola, S. Ceballos, and E. Robles, "Current balancing strategy in parallel-connected legs of power inverters," in *Proc. EPE Conf. Appl.*, Barcelona, Spain, Sep. 8–10 2009, pp. 1–9.

[6] G.J. Capellá, J. Pou, J. Zaragoza, S. Ceballos, I. Gabiola, and E. Robles, "Parallel-connected legs in a grid-tied inverter system for distributed generation", in *Proc. Int. Conf. Renewable Energies Power Quality (ICREPQ)*, Las Palmas de Gran Canaria, Spain. Apr. 13–15, 2011. Online: http://www.icrepq.com/icrepq'11/630-capella.pdf

[7] J. Pou, S. Ceballos, G. Konstantinou, G. J. Capellá, V. G. Agelidis, "Control strategy to balance operation of parallel connected legs of modular multilevel converters," in *Proc. IEEE Int. Symp. Ind. Electron. (ISIE)*, Taipei, Taiwan, May 28–31, 2013, pp. 1–7.

[8] G. Konstantinou, J. Pou, G. J. Capellá, S. Ceballos, and V. G. Agelidis, "Reducing circulating currents in interleaved converter legs under selective harmonic elimination pulse-width modulation," to appear in Proc. *IEEE Int. Conf. Ind. Tech. (ICIT)*, Seville, Spain, Mar. 17–19, 2015.

1.5.3 Papers under Revision

The following paper has been submitted to a journal and it is currently under consideration for publication:

[9] A.M.Y.M. Ghias, J. Pou, G. J. Capellá, V. G. Agelidis, R. Aguilera, and T. Meynard, "Single-carrier phase-disposition PWM implementation for multilevel flying capacitor converters," submitted to *IEEE Trans. Power Electron.*

The selected journal and conference papers are associated with the chapters of the thesis as shown in Table 1.1.

1.6 Thesis Outline and Main Contributions

- Chapter 2 presents the topologies of two-level and multilevel VSIs made up with legs connected in parallel that are commonly used at the moment. It also reviews

Chapter	**Publication**
Chapter 3 Current-Balancing Techniques	[1],[4],[5],[7],[8]
Chapter 4 Single Carrier Modulator for Interleaved Operation of Parallel Phase-legs in Voltage-Source Converters	[2],[9]
Chapter 5 Disposition of the Carriers	[3]
Chapter 6 Application to Grid-Connected Voltage-Source Inverters	[6]

TABLE 1.1: Relationship between chapters and publications.

the different modulation techniques. It finally provides the characteristics of the prototypes used in this thesis.

- In Chapter 3, a current-balancing method for VSIs with legs connected in parallel is presented. The method does not use any PI controller nor requires any parameter tuning. It can be applied to legs connected in parallel by means of either coupled or uncoupled inductors.

- In Chapter 4, the implementation of a modulation scheme which is able to produce carrier-based interleaved modulation for n parallel-connected legs in a VSI that uses of just one carrier signal is presented.

- In Chapter 5, on the basis of a PS-PWM scheme, an improved disposition of the carriers is presented. Such modified modulation scheme is able to achieve line-to-line output voltages in VSIs with legs connected in parallel similar to the ones that can be obtained with a LS-PWM scheme. The new disposition of the carriers achieves an improvement in the THD with respect to the standard phase-shifted disposition of the carriers.

- Chapter 6 deals with the application of the current-balancing method described in Chapter 3 to a grid-connected VSI made up with legs connected in parallel.

- Finally, Chapter 7 summarizes the thesis major contributions and includes some discussion on possible future research.

Chapter 2

Voltage-Source Inverters And Modulation Techniques

This chapter recalls the concepts of two-level and multilevel inverters and presents an overview of the modulation techniques. It focuses on multicarrier PWM techniques that can be applied to VSI with legs connected in parallel. The configuration of the parallel connection by means of coupled or uncoupled inductors is presented too. The chapter also includes a reference to the software tools and the VSI prototypes used to obtain the simulation and experimental results.

2.1 Introduction

VSIs are usually the power circuits used to convert electric power from dc sources into standard sinusoidal currents suitable for the grid (see Fig. 2.1). Such inverters are commonly designed for single- or three-phase systems. Inverters can be primarily classified into two categories: two-level and multilevel topologies [72,73]. Two-level converters can only generate two voltage levels at their outputs, whereas multilevel converters are able to generate three or more voltage levels. Multilevel converters are made of several power semiconductor switches or submodules connected in series so that the overall system can deal with higher voltage and power than two-level inverters. Multilevel topologies have several advantages over the conventional two-level topology such as: improved efficiency, lower voltages and currents applied to the power devices, lower distortion in the output voltages and currents, lower d_v/d_t and less audible-noise generated as a result of smaller voltage steps, and smaller switching frequency per device. On the other hand, multilevel topologies present some drawbacks as the fact that they require a great number of

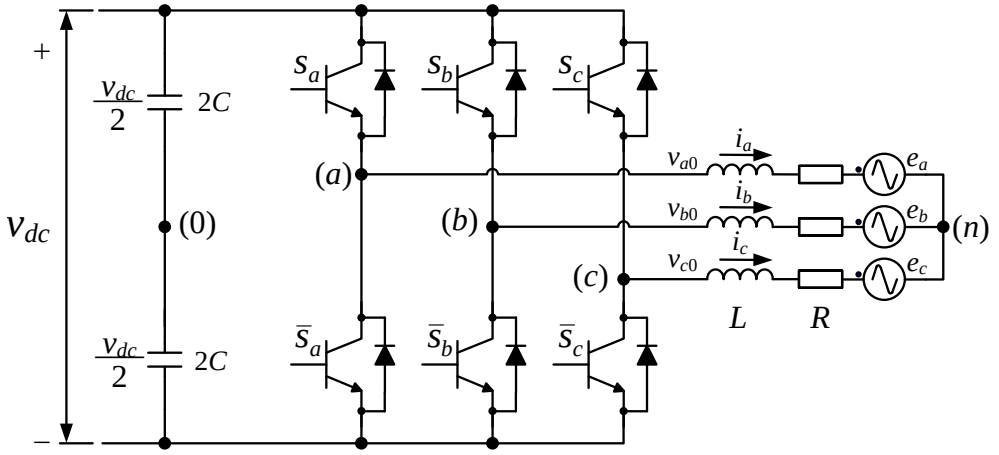


FIGURE 2.1: Grid-connected three-phase inverter.

power switches and the need for the implementation of some capacitor-voltage balancing technique. Moreover, the overall system is expensive and complex.

In order to raise the electric power handled by a VSI either voltages, currents, or both can be increased. Multilevel converters are extensively used in high power systems because they can deal with higher voltages due to the fact that the voltage to be switched is shared among several semiconductors [5,6,74,75]. They also yield better output voltage spectra than two-level converters [63]. On the other hand, currents, rather than voltages, can be increased in order to achieve higher power in some fields: wind generation would be a good example. Consequently, such a type of converters can be kept in the low-voltage range and, therefore, under the low-voltage regulations, which are less demanding than mid-voltage regulations. Furthermore, the cost of low-voltage maneuver devices is usually much more economical. However, dealing with high currents requires the use of proper connectors, bus bars, etc. This increase in the output current can be attained either with VSIs made up with legs connected in parallel –see Fig.2.2(a)– if all the legs are connected to a common dc-bus, or by means of the parallel connection of inverters –see Fig. 2.2(b)– when each one has its own isolated dc-bus [76,77]. In addition, inverters with legs connected in parallel are modular and because of that, their production and maintenance become less expensive. Moreover, they qualify for the implementation of fault-tolerant techniques thus offering improved overall reliability [39, 40].

Paralleling power semiconductors is another way to increase the output currents of such power systems [16]. Nevertheless, mismatches among the power devices may lead to additional conduction and commutation losses. Metal-oxide semiconductor field-effect transistors (MOSFETs) are one of the exceptions to this rule, due to the fact that they have positive temperature coefficient, which helps achieving current balance among the parallel-connected devices.

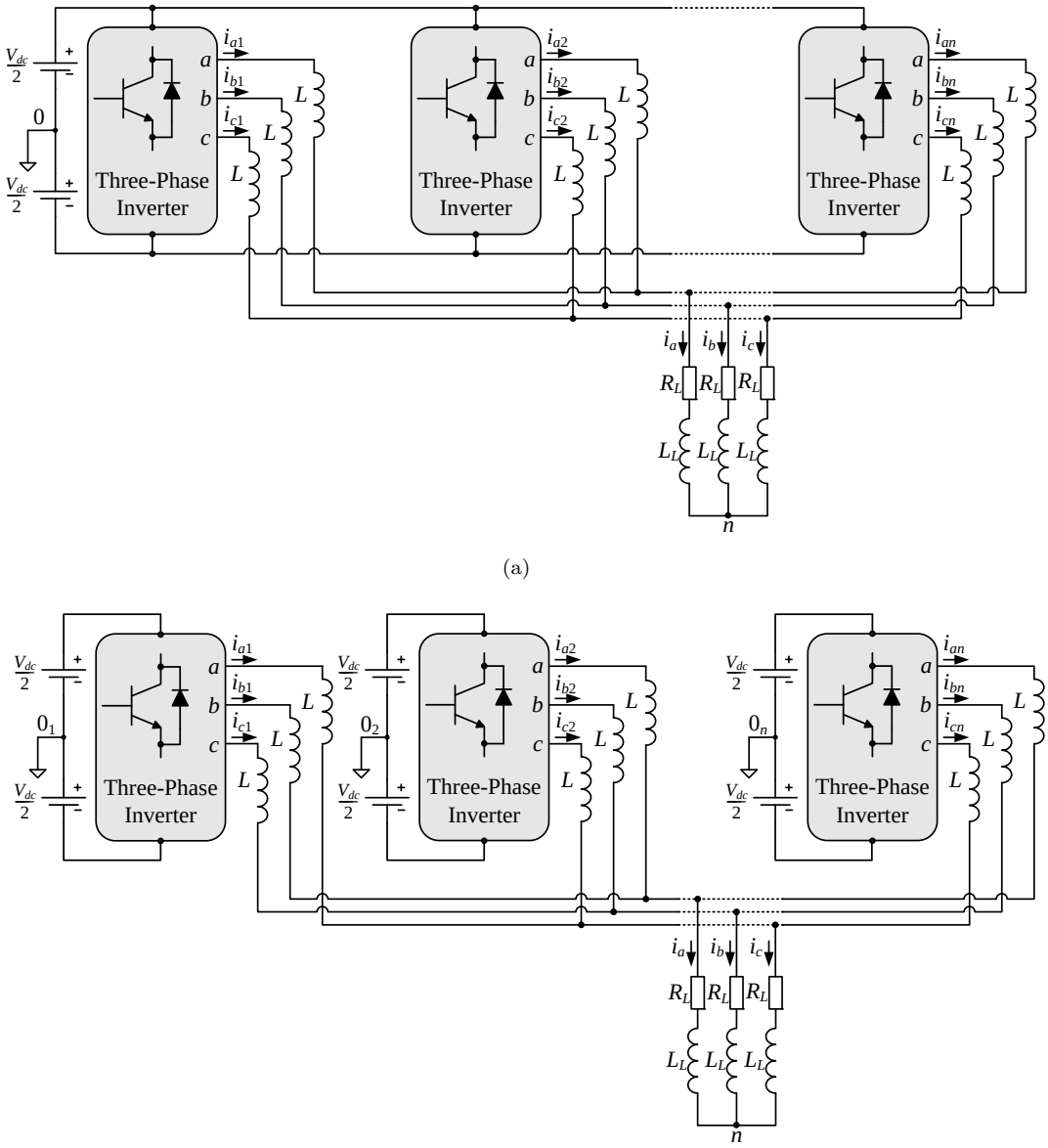


FIGURE 2.2: (a) VSI with legs connected in parallel (i.e. with a common dc-bus). (b) VSIs conected in parallel (i.e. with isolated dc-buses).

Rather than by paralleling devices [78, 79], higher current values can be achieved either by paralleling whole converters or just by paralleling the legs of several converters [34, 48, 80]. The operation of autonomous converters in parallel or the operation of a converter with legs in parallel brings some issues that have to be addressed. For instance, the controllers have to guarantee that each converter unit or converter-leg processes a fair share of the total power. In addition, circulating current among the converters must be avoided or controlled. Despite those issues, the potential benefits of paralleling converters makes their use worthwhile. Among the benefits of paralleling the reduction of output filtering requirements, the output harmonic content, easy modularity and expandability could be cited. Furthermore, in high power grid-connected converter

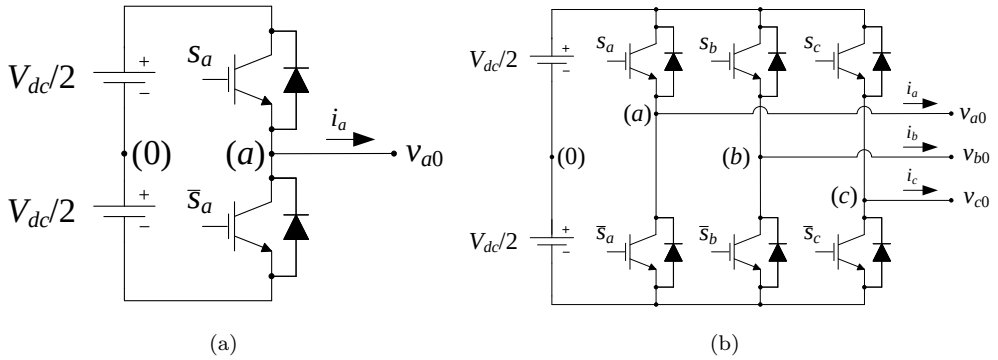


FIGURE 2.3: (a) Half-bridge inverter. (b) Three-phase inverter.

applications, where standard regulations may limit the current harmonic injection into the grid, the reduction of the output filter also relieves the reactive energy processed that usually limits the converter power transfer capability.

In this thesis, the conventional two-level inverter made up with legs connected in parallel has been selected. Nevertheless, the main contributions of this thesis can also be applied to multilevel converter topologies with legs connected in parallel or can be easily adapted to them.

2.2 Two-Level and Multilevel Inverters

The two-level inverter is based on the half-bridge topology, as shown in Fig. 2.3(a). It delivers output voltage waveforms with only two levels ($+V_{dc}/2$ or $-V_{dc}/2$). The three-phase configuration is shown in Fig. 2.3(b). The switches on each leg always operate in a complementary mode, i.e., there is only one switch in the on-state at any time, while the other one is in the off-state. In the case of a three-phase inverter this can be expressed as follows:

$$s_x + \bar{s}_x = 1 \quad \text{for} \quad x = \{a, b, c\}, \tag{2.1}$$

where s_x is the control function of the upper switch and can only take two values: 1, when the switch is on and 0 when it is off.

Fig. 2.4 shows an example of multilevel converter. The topology shown in this figure is a three-level converter known as NPC converter. Table 2.1 summarizes the switching states and the corresponding output voltage for phase a, assuming that the dc-link voltage is evenly shared between the capacitors ($v_{C1} = v_{C2} = V_{dc}/2$).

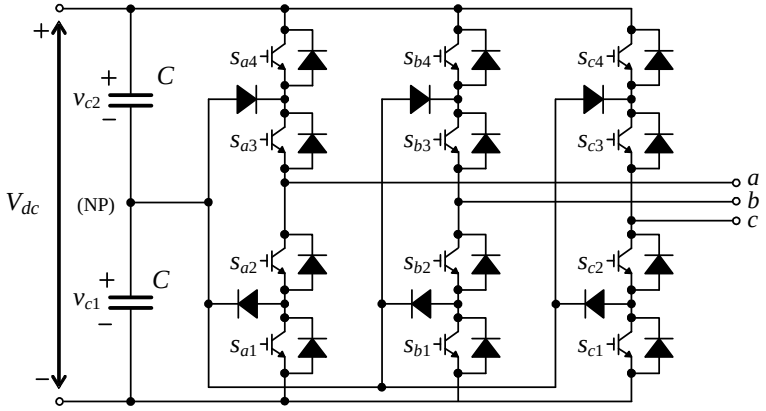


FIGURE 2.4: Three-level NPC converter.

TABLE 2.1: Switching States of an NPC Converter

S_{a4}	S_{a3}	S_{a2}	S_{a1}	Output Voltage
On	On	Off	Off	$V_{a0} = V_{dc}/2$
Off	On	On	Off	$V_{a0} = 0$
Off	Off	On	On	$V_{a0} = -V_{dc}/2$

2.3 Modulation Techniques

The on-off state of the switches in the converter is defined by a modulator stage, which acts according to the control variables. Fig. 2.5 illustrates one of the possible ways to classify modulation techniques that can produce multilevel output voltages. Fundamental switching frequency techniques are beyond the scope of this thesis. High-frequency switching techniques can be roughly divided into space-vector pulse-width modulation (SV-PWM) and carrier-based pulse-width modulation (CB-PWM).

2.3.1 Carrier-Based PWM

CB-PWM is achieved by comparing a modulating signal to a triangular or saw-tooth shaped carrier signal, which usually has a significantly higher frequency. If the reference signals are sinusoidal, the CB-PWM is referred to as sinusoidal PWM (SPWM). In such a modulation technique the width of the pulses generated at the outputs of the inverter change according to the sinusoidal reference signal. Fig. 2.6 shows the concept of a SPWM depicting the carrier signal, the modulating signal and the output voltage from a half-bridge inverter.

Some degrees of freedom are introduced in the aforementioned technique [66]. The amplitude modulation index (m_a), which is the ratio of the amplitude of the sinusoidal reference to the amplitude of the triangular signal, and the frequency modulation index

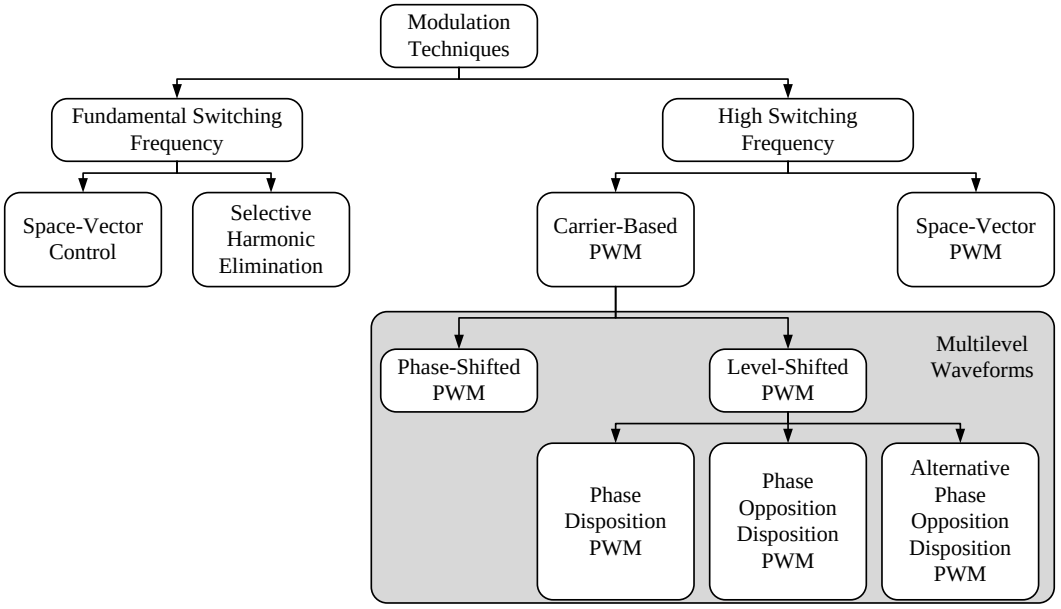


FIGURE 2.5: Classification of modulation techniques.

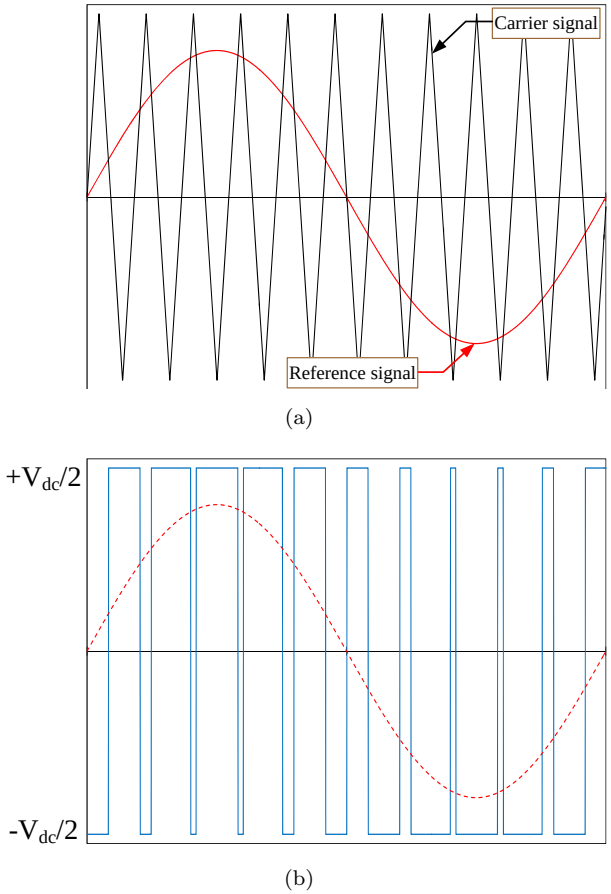


FIGURE 2.6: Half-bridge signals using SPWM. (a) Carrier and reference signals. (b) Output voltage and fundamental component.

($m_f = f_c/f_r$), where f_c is the carrier frequency and f_r is the frequency of the sinusoidal reference signal.

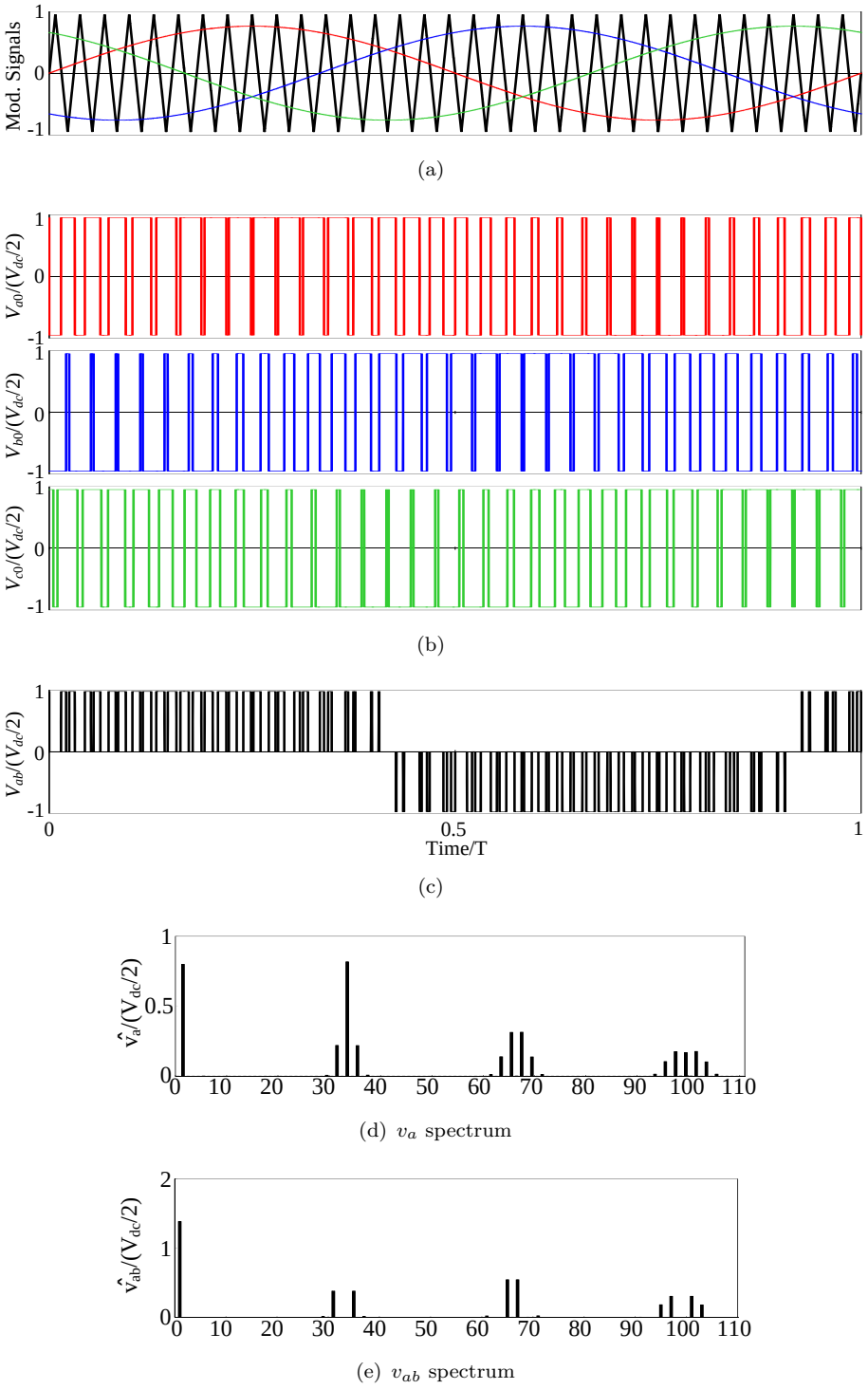


FIGURE 2.7: SPWM performance. (a) Modulation and carrier signals. (b) Normalized phase voltages (v_{a0}, v_{b0}, and v_{c0}). (c) Normalized line-to-line voltage (v_{ab}). (d) Single-phase voltage (v_{a0}) spectrum. (e) Line-to line (v_{ab}) spectrum.

In a CB-PWM implementation, the switching frequency of the power devices is essentially dependent on the carrier frequency. If the carrier frequency increases, the switching frequency of the power devices increases too, and thus the switching power losses. On the other hand, the larger the carrier frequency, the better the quality of

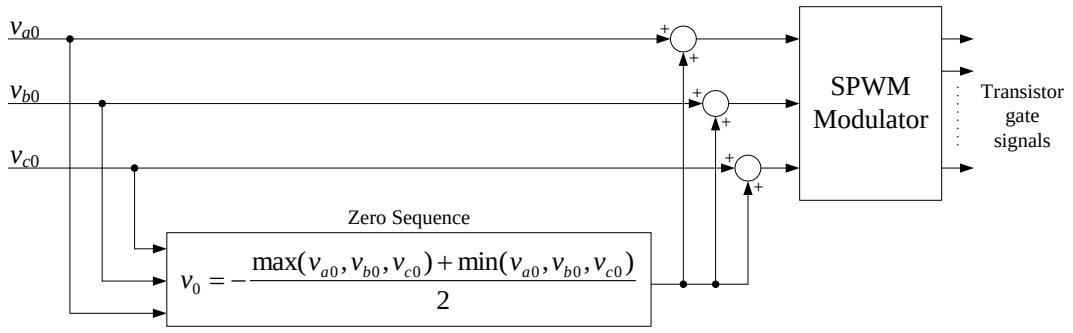


FIGURE 2.8: Modified SPWM scheme with zero-sequence voltage injection.

the output voltages. As a consequence, there is a trade-off between output quality and power losses when choosing the carrier frequency. In an n-phase inverter, n evenly phase-shifted reference signals are compared to the carrier signal to obtain the control signals for the switches. Fig. 2.7 shows this concept for a three-phase inverter, and illustrates the performance of the SPWM technique. In Figs. 2.7(a) to 2.7(c), the time has been normalized on the fundamental output period $T_r = 1/f_r$, f_r being the fundamental frequency, whereas in Figs. 2.7 (d) and 2.7(e) the frequency has been normalized, based on the fundamental output frequency.

For the three-phase inverter case, a couple of things deserve to be highlighted. The first one is the fact that there are no harmonics multiple of three (triplets) in the line-to-line voltages: the triplets contained in the phase voltages disappear in the line-to-line voltages. This is because these harmonics are zero-sequences (they are common to the three phases). Besides, a specific zero-sequence reference could be added on purpose to the modulation signals to achieve larger amplitudes of the output voltage fundamentals under linear operation mode, and to lower the actual switching frequency in the power devices [8, 9, 11].

In order to avoid over-modulation, the amplitude of the reference signals should never exceed the amplitude of the carrier signal. Over-modulation is a nonlinear operational mode of the inverter where the amplitudes of the fundamental output voltages are no longer proportional to the modulation index. It also produces low-frequency harmonic distortion.

Fig. 2.8 illustrates an example of a zero sequence injection and its performance is illustrated in Fig.2.9. Such a zero sequence is defined by

$$v_0 = -\frac{\max(v_{a0}, v_{b0}, v_{c0}) + \min(v_{a0}, v_{b0}, v_{c0})}{2}, \tag{2.2}$$

where $\max(v_{a0}, v_{b0}, v_{c0})$ and $\min(v_{a0}, v_{b0}, v_{c0})$ are the maximum and minimum values, respectively, of the three reference signals for v_{a0}, v_{b0}, and v_{c0}.

TABLE 2.2: Status of the inverter switches and output voltages

Vector	s_a	s_b	s_c	v_{a0}	v_{b0}	v_{c0}	v_{ab}	v_{bc}	v_{ca}
V_0	0	0	0	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	0	0	0
V_1	1	0	0	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	V_{dc}	0	$-V_{dc}$
V_2	1	1	0	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	0	V_{dc}	$-V_{dc}$
V_3	0	1	0	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}$	V_{dc}	0
V_4	0	1	1	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}$	0	V_{dc}
V_5	0	0	1	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	0	$-V_{dc}$	V_{dc}
V_6	1	0	1	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	V_{dc}	$-V_{dc}$	0
V_7	1	1	1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	0	0	0

As this zero-sequence is added to the reference signals for the three phases, it does not show when looking into the line-to-line output voltages as they cancel themselves out. The benefit of injecting this zero-sequence component is that it reduces the peak values of the reference signals while keeping the same fundamental components. As a result, linear operation mode of the inverter can be extended beyond $m_a = 1$, up to 1.15 without causing over-modulation.

2.3.2 Space-Vector PWM

The SV-PWM technique is based on a vector representation of the output voltages of the inverter on the $\alpha - \beta$ plane. A cube can be drawn in a three-dimension representation by joining the tips of the vectors obtained from conventional topologies of inverters [81].

The same vectors can be seen from another orthogonal and stationary base called $\alpha\beta\gamma$(or $\alpha\beta 0$), in which the γ component (or zero sequence) does not have a significant role in the modulation. This is generally true if the load is not connected to the dc-link side of the inverter. Due to this fact, the only variables of interest are the ones that are on the $\alpha\beta$ plane. SV-PWM processes the modulation of the three phases as a whole and thus exploits the interaction between the three phases. A proper zero-sequence component is intrinsically generated and, therefore, maximum extension of the linear operation mode is achieved. The space vector representation is obtained by applying the Clarke's transformation to the output voltages of the inverter:

$$\vec{v}_k = \frac{2}{3}(v_{a0} + \vec{a}v_{b0} + \vec{a}^2 v_{c0}) \tag{2.3}$$

where $\vec{a} = j\frac{2\pi}{3}$. The magnitude of the active vectors is $\frac{2}{3}V_{dc}$.

Fig. 2.10(a) illustrates the scheme of a three-phase two-level inverter. Eight vectors, which produce the voltage vectors shown in Fig. 2.10(b), are defined according to the possible states of the switches. Table 2.2 summarizes the eight possible states of the inverter.

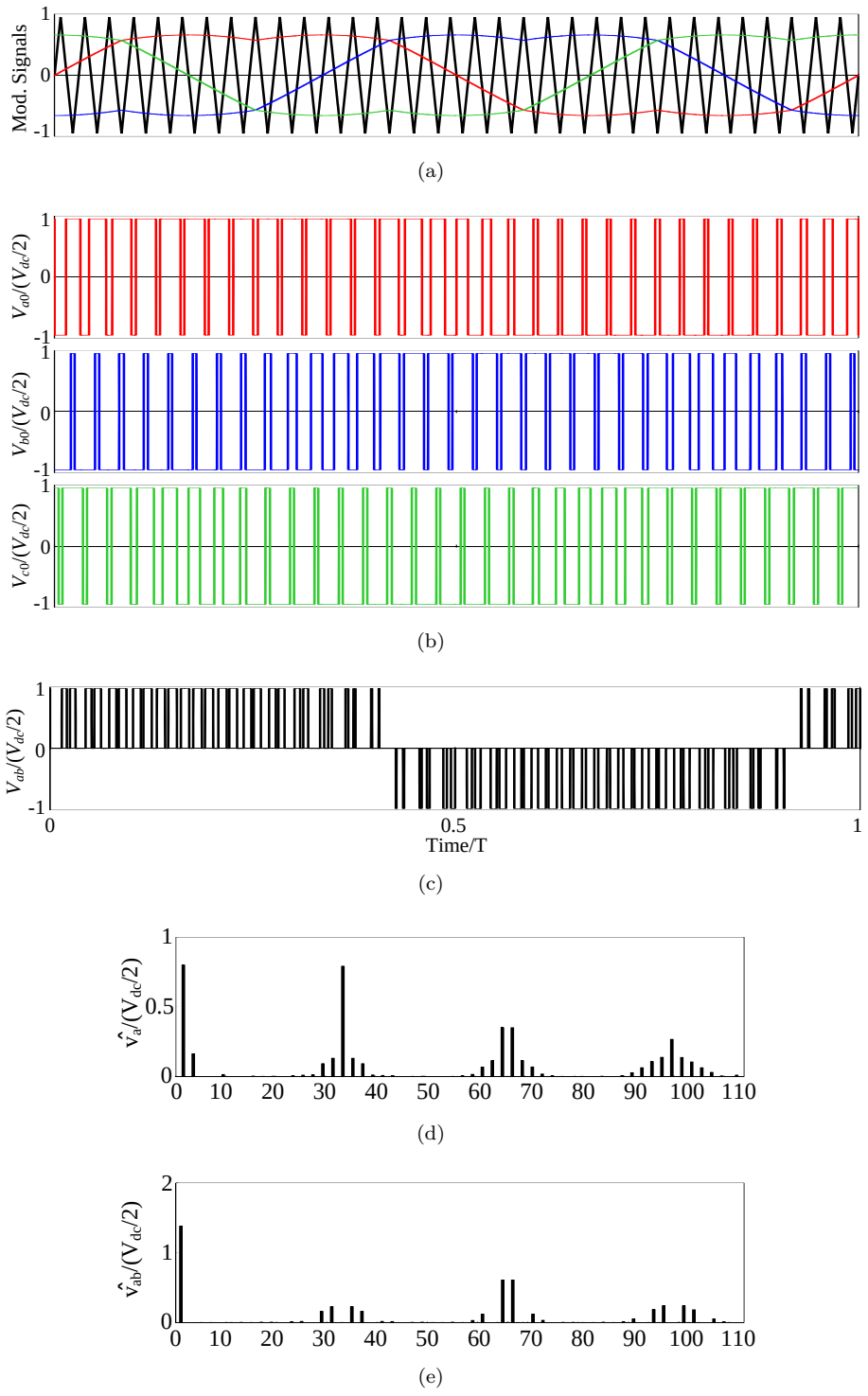


FIGURE 2.9: Modified SPWM performance. (a) Modulation and carrier signals. (b) Normalized phase voltages (v_{a0}, v_{b0}, and v_{c0}). (c) Normalized line-to-line voltage (v_{ab}). (d) Single-phase voltage (v_{a0}) spectrum. (e) Line-to line (v_{ab}) spectrum.

In Fig. 2.11 the state of the switches is illustrated by 1 or 0, which denote the on-off state of the upper transistor in each phase-leg. The corresponding voltage levels are $V_{dc}/2$ or $-V_{dc}/2$ with respect to the NP. Six of the space vectors (V_1 to V_6) have the

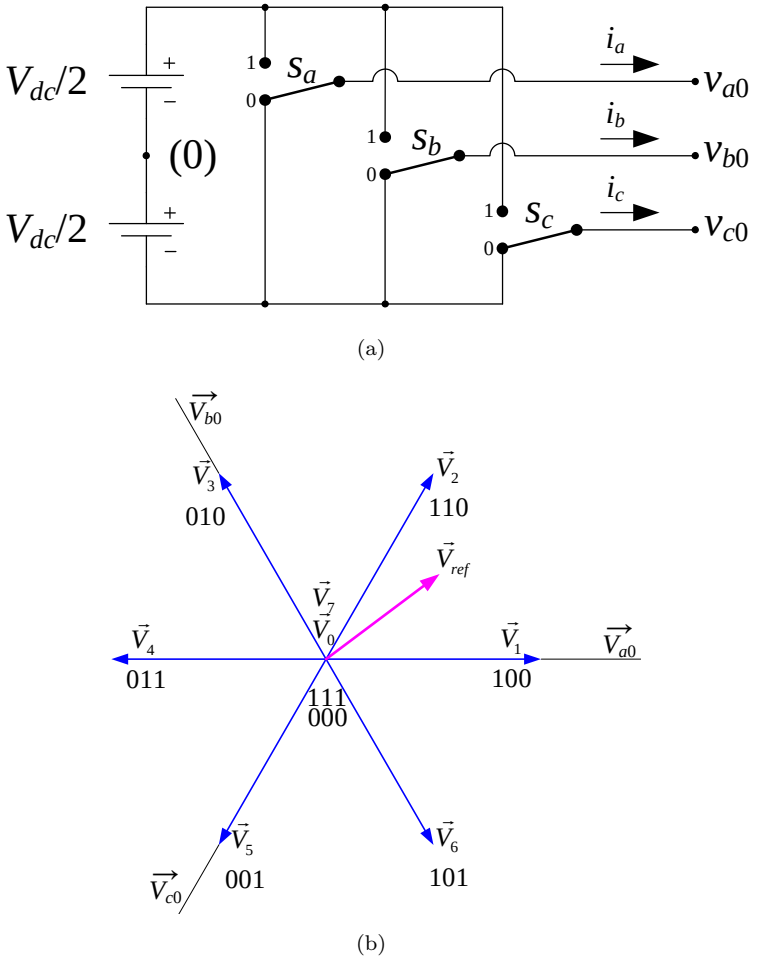


FIGURE 2.10: SV-PWM. (a) Two-level three-phase VSI scheme. (b) Voltage vectors and their corresponding switching states.

same length and are phase-shifted by sixty degrees; they are called active vectors. The other two vectors (V_0 and V_7) are in the origin because of their null lengths.

The aim of the SV-PWM is to generate a reference vector in the same plane for each modulation cycle. Since the reference vector will usually not coincide with any of the available vectors in the diagram, it will have to be generated on average using more than one vector per modulation cycle by PWM-averaged approximation. Selecting proper vectors and applying them in a suitable order helps reduce the actual switching frequency of the semiconductor devices.

In the steady-state condition, the reference vector has constant length and rotates at a constant speed as depicted in Fig. 2.11(a). Consequently, the generated output voltage fundamentals will be balanced; with a constant amplitude and angular frequency (ω). The reference vector will be sampled (discrete positions) and should be synthesized for each position making use of the available vectors in the diagram.

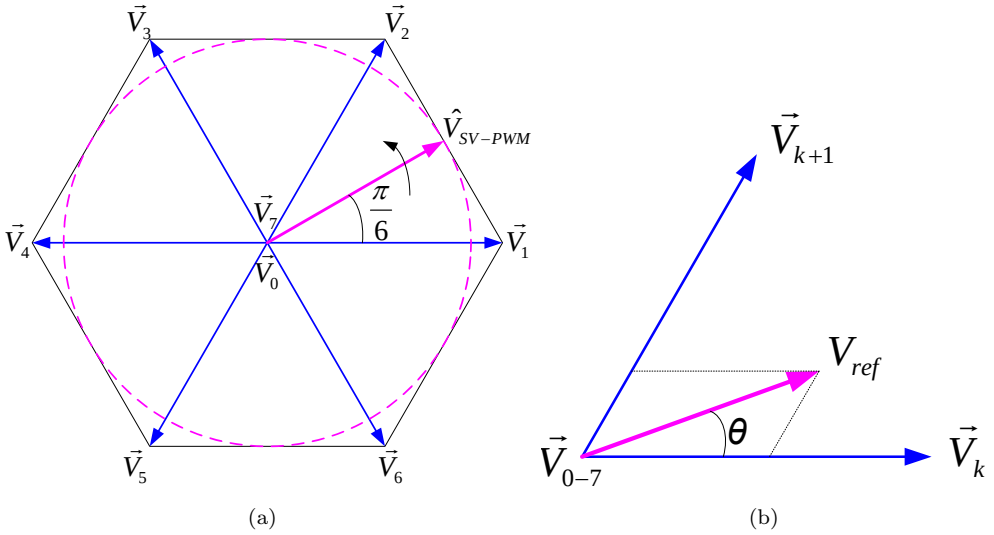


FIGURE 2.11: Sampled generation of the output voltage. (a) Rotating reference vector. (b) Vector components.

The vectors selected are usually the two adjacent active vectors and one null vector. Consider a reference vector located in one of the six sectors as depicted in Fig. 2.11(b). Either of the null vectors ($\vec{V}_0$ and $\vec{V}_7$), or both, can be used as the third space vector. The reference vector can be derived as follows:

$$\vec{V}_{\text{ref}} = \frac{t_k}{T_s}\vec{V}_1 + \frac{t_{k+1}}{T_s}\vec{V}_2 + \frac{t_{0-7}}{T_s}\vec{V}_{0-7} \tag{2.4}$$

or

$$\vec{V}_{\text{ref}} = d_k\vec{V}_k + d_{k+1}\vec{V}_{k+1} + d_{0-7}\vec{V}_{0-7}, \tag{2.5}$$

where d_k, d_{k+1}, and d_{0-7} are the duty cycles of the corresponding space vectors. The duty cycles d_k and d_{k+1} can be computed as:

$$\begin{bmatrix} d_k \\ d_{k+1} \end{bmatrix} = \frac{\sqrt{3}}{V_{dc}} \begin{bmatrix} sin\frac{k\pi}{3} & -cos\frac{k\pi}{3} \\ sin\frac{(k-1)\pi}{3} & -cos\frac{(k-1)\pi}{3} \end{bmatrix} \tag{2.6}$$

The sum of the duty cycles is always the unity:

$$d_k + d_{k+1} + d_{0-7} = 1. \tag{2.7}$$

Therefore, the third duty cycle can be obtained by subtraction as follows:

$$d_{0-7} = 1 - d_k - d_{k+1}. \tag{2.8}$$

The maximum amplitude of the reference space vector as shown in Fig. 2.11(a) is calculated as:

$$\hat{V}_{\text{REF}} = \frac{2}{3} V_{dc} cos(\frac{\pi}{6}) = \frac{V_{dc}}{\sqrt{3}}. \tag{2.9}$$

and the ratio between the maximum fundamental output voltage amplitudes of SV-PWM with regard to SPWM with no zero-sequence injection is:

$$\frac{\hat{V}_{\text{SV-PWM}}}{\hat{V}_{\text{SPWM}}} = \frac{\frac{V_{dc}}{\sqrt{3}}}{\frac{V_{dc}}{2}} = \frac{2}{\sqrt{3}} = 1.15. \tag{2.10}$$

2.4 Multicarrier PWM Techniques

Multicarrier PWM techniques are commonly used when dealing with multilevel converters, but also with converters made up with legs connected in parallel. Such PWM techniques are based on a single reference signal which is compared with a series of triangular-shaped carrier waveforms. That is the reason why they are referred to as multicarrier PWM techniques. Several dispositions of the carriers are possible and, depending on the type of disposition, multicarrier PWM can be categorized into PS-PWM and LS-PWM.

2.4.1 PS-PWM: the Interleaving Technique

In order to apply a PS-PWM technique to a VSI made up with n legs connected in parallel, n carrier signals are required, i.e. in a PS-PWM case, as many carriers as legs connected in parallel are used. All the carriers have the same amplitude and frequency, their normalized domain ranges from -1 to +1, and they are phase-shifted among themselves with an angle of $360°/n$. Fig. 2.12(a) shows the disposition of three carriers and the reference signal in such a case. Fig. 2.12(b) shows the general n-case carriers' disposition ($v_{carr\,1}$, $v_{carr\,2}$, ... $v_{carr\,n}$) although only the first three carriers have been depicted.

The interleaving technique is applied to the VSIs with legs connected in parallel in order to procure an apparent switching frequency n times higher than the individual switching frequency of each leg ($f_s = nf_{sw} = n/T_{sw}$) [25]. Each carrier is associated with a specific leg and the result of the comparison between the reference signal and the carrier determines the state of the switches in that leg.

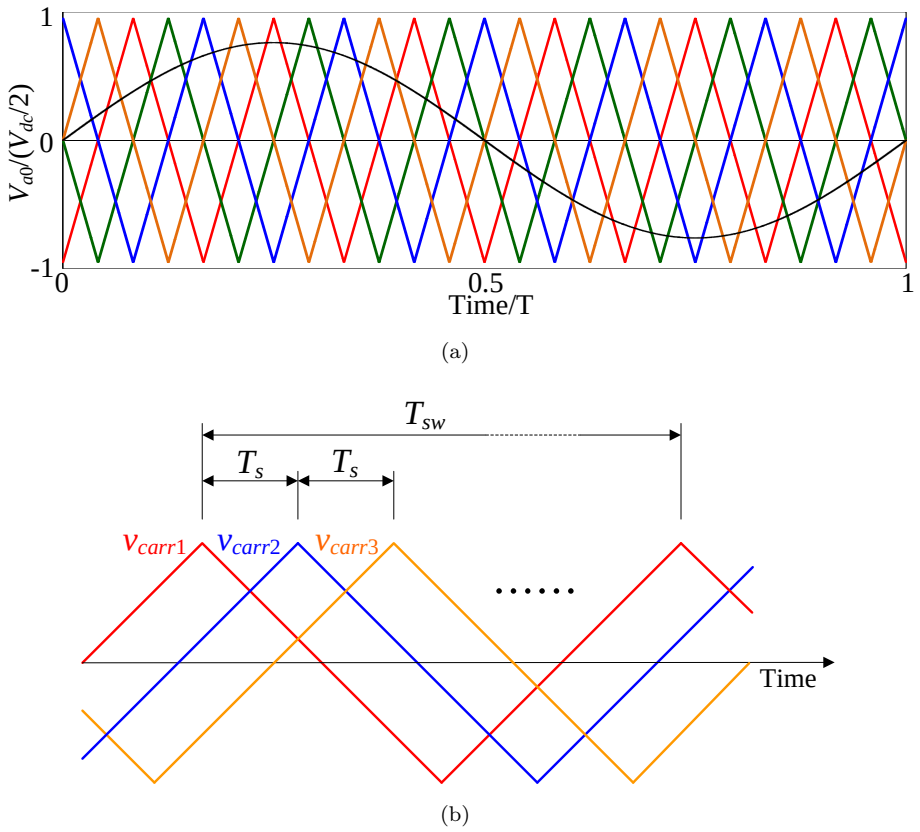


FIGURE 2.12: Phase-shift disposition of the carriers for interleaving operation mode. (a) Reference and carrier signals in a four-carrier case. (b) Generic-case shifting.

2.4.2 Level-Shifted PWM

In multilevel LS-PWM, the carriers have the same amplitude $(2/n)$ and frequency, and they are arranged in level-shifted bands to fully occupy the range between -1 and +1. Three main alternatives for LS-PWM have been developed in the technical literature [45, 61, 65]:

- PD-PWM
- POD-PWM
- APOD-PWM

In PD-PWM all the carriers signals are in phase, as shown in Fig. 2.13(a). In POD-PWM, all the carriers above zero are in phase, all the ones below zero are in phase too, but there is a 180° phase-shift between both groups of carriers as can be seen in Fig. 2.13(b). In APOD-PWM the carriers in adjacent bands are phase shifted by 180° as illustrated in Fig. 2.13(c). For all three mentioned dispositions the significant line-to-line voltage harmonics are presented as sidebands around the carrier frequency.

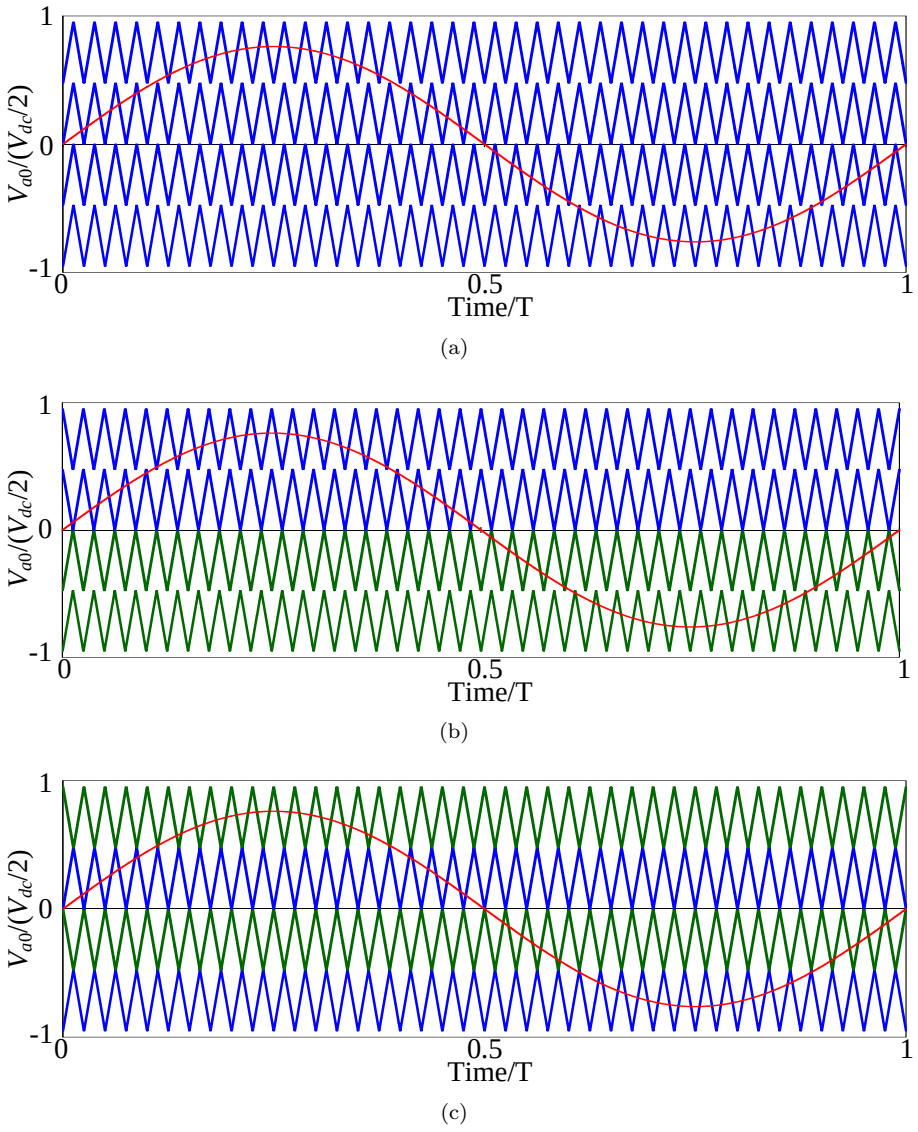


FIGURE 2.13: Reference signal and multicarrier dispositions for LS-PWM. (a) PD. (b) POD. (c) APOD.

Fig. 2.14 shows an example of PD-PWM applied to a five-level converter, which requires the use of four carriers. It is well known that among the level-shifted techniques, the output voltages generated by PD-PWM have better spectra [17, 45, 55].

In the examples shown in Fig. 2.13 the implementation of LS-PWM requires the use of four carriers of the same amplitude, frequency and phase, which are arranged into contiguous bands that fully occupy the linear modulation range. In each case, a sinusoidal reference signal (v_{ref}) is compared with the four triangular carriers to define the voltage level that has to be generated at the output. The PD-PWM, POD-PWM and APOD-PWM control methods have the property of producing signals with a switching frequency that is significantly lower than the carrier frequency [66].

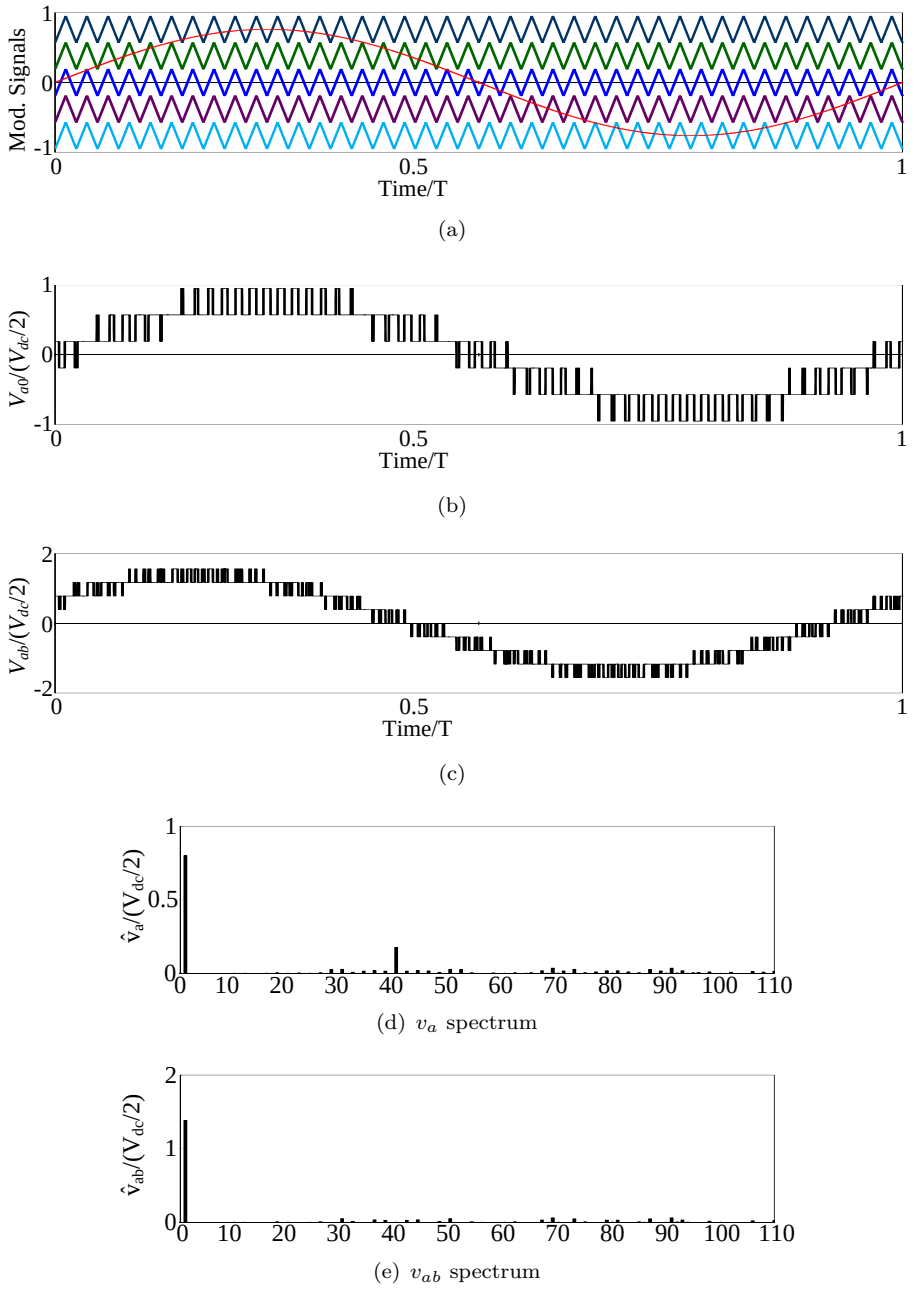


FIGURE 2.14: Five-level VSI performance. (a) Level-shifted disposition of the carriers. (b) Single-phase voltage (v_{a0}). (c) Line-to-line voltage (v_{ab}). (d) Single-phase- and (e) Line-to-line output-voltage spectrum.

2.5 Phase Configuration of Legs Connected in Parallel

Parallel-connected legs of a VSI cannot be directly connected in order to avoid short-circuits [25]. An appropriate filter is required in order to obtain a single averaged output voltage from several input legs, and keep the overall amount of harmonics under acceptable limits. Since inductors can limit the circulating currents without producing

significant power losses, they are the optimal passive components to achieve the following benefits: (*i*) limiting circulating currents among the legs and (*ii*) averaging voltages of several legs for each output phase. Because of the averaging, the equivalent output voltage of the phase would show more than two levels [17]. In a symmetrical configuration the number of voltage levels will be $n+1$, n being the number of legs connected in parallel.

In grid-connected systems, where some L or L-C-L filters are required, the equivalent inductance of the legs connected in parallel from the output side may work as a filter itself or, at least, can help reduce the size of any additional filtering inductor required. However, stability degradation due to resonances resulted from interaction among filter, grid impedance and current controllers is an issue to be carefully addressed, specially when considering the grid impedance uncertainty at the point of common connection [82, 83]. The aforementioned filters have a double function: on the one hand, they get rid of high frequency harmonics produced by the PWM switching in the converter, so that almost pure sinusoidal currents are delivered to the grid. On the other hand, they place some impedance between two voltage sources, i.e. the output of the converter and the mains. Without such a filter, a direct connection of the converter to the grid would cause short-circuit [84].

The connection of the different legs can be implemented with either single inductors or with magnetically coupled inductors. Using single inductors facilitates modularity and scalability as the contribution to the output current from one leg is not affected by the others. This peculiarity eases the management in case of a leg faulty operation and also allows for the implementation of fault tolerant systems. On the other hand, the use of coupled inductors despite not having the aforementioned advantages, can bring significant size reduction in the amount of magnetic material required and, as a consequence, a reduction in magnetic losses. The use of one or another type of inductors boils down to a trade-off between modularity and lower size and lesser losses.

2.5.1 Uncoupled Inductors

Fig. 2.15 shows an example of parallel-connected legs that utilizes single inductors. The n legs shown in this circuit diagram correspond to one single phase of the converter (phase a, for instance).

The fact of using uncoupled inductors makes the converter configuration modular and easily expandable to a different number of legs connected in parallel. The higher the inductance value of the inductor in this configuration, the more efficient the filtering is. However, low frequency components of the output current also flow through the

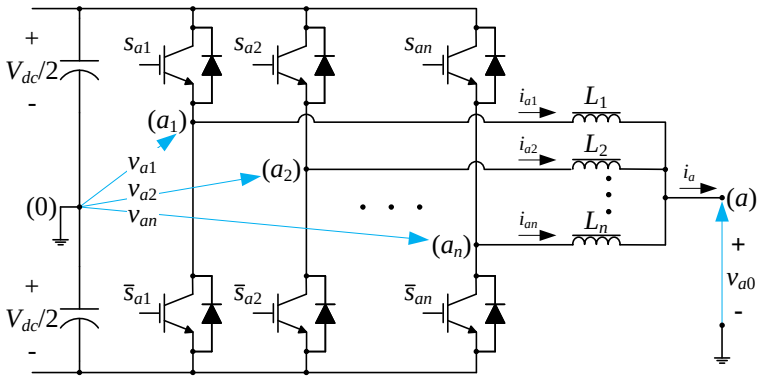


FIGURE 2.15: Phase configuration of a VSI with n legs connected in parallel by means of uncoupled inductors.

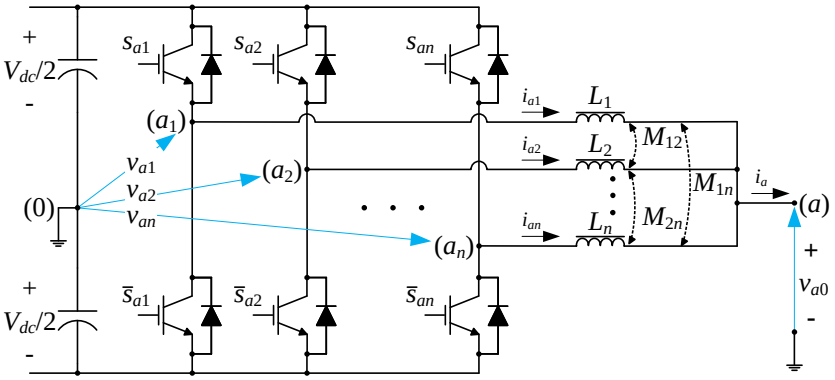


FIGURE 2.16: Phase configuration of a VSI with n legs connected in parallel by means of coupled inductors.

inductors. These low frequency components greatly influence the energy stored by the inductors, as the low frequency current components make up a large amount of the overall current. As the size of the inductors depends on the maximum amount of stored energy, low volume inductors will lead to low inductances. These two items lead to an opposite conclusion. The first one involves using a high permeability material whereas the second involves a low permeability material that gives a smaller inductance providing a size reduction but also a worse filtering efficiency. It can be noticed that a classical inductance is a technological trade-off between these two limits.

2.5.2 Coupled Inductors

Fig. 2.16 shows an example of parallel-connected legs where multiple magnetic coupling among the inductors is assumed, although the analysis could be extrapolated to different types of coupling, like the ones presented in [85]. Again, the n legs shown in these scheme correspond to one single phase of the converter (phase a, for instance).

Multi-cell transformers are magnetic devices that offer two possible magnetic paths: one with low permeability for the low-frequency components and another one with a high permeability for the switching harmonics. This is achieved by magnetic coupling so that, at least one piece of the magnetic path of all the leg inductors is shared among them [20, 21]. The use of multi-cell transformers [20] allows for extending the output ripple cancellation to the switches and the inductors. In comparison to the uncoupled multi-leg converter, smaller inductors can be used at the same switching frequency without inducing more ripple current, if magnetic coupling is used.

In [20] a comparison between the output-current ripple in interleaved paralleled converters using single inductors and coupled inductors (multi-cell transformers) is performed. When uncoupled inductors are used to connect several interleaved legs, ripple cancellation affects the converter output. In this structure, the inductor-current ripple in each channel is still large and the current ripple frequency is unchanged. If the L value is lowered in order to improve transient response, the inductor-current ripple increases and so do inductor winding losses and semiconductor switching losses. The current balancing method for both configurations is described in Section 3.2 of Chapter 3.

2.6 VSI Prototypes and Tools Used

The experimental results presented in this thesis have been obtained by means of two prototypes which are available at the UPC in the research laboratory #1 of TIEG in the Campus of Terrassa. Each prototype is a small-power two-level three-phase inverter (around 3 KW), with an up-to-800-V dc-bus, with 680-μF capacitors. Their power modules are Mitsubishi PM15CZF120. Every inverter is mounted along with its signal conditioning circuitry that facilitates the measurement of the output current and voltage of each leg. They also include a circuit, based on a programmable logic device, which is configured to protect the converter. The circuit also prevents from applying any either hazardous or damaging combination to the switches. A picture of such a prototype can be seen in Fig. 2.17. A 24-V power supply is used to feed the circuit that includes the power drivers, the measurement circuitry and the over-current protections. A symmetrical $\pm$30-V power supply is normally used as the primary power source for the converters.

All the models for the different configurations of the experimental plant, the control algorithms and the modulation strategies have been firstly simulated on a personal computer (PC) in a Matlab/Simulink [86] environment. The blocks used in the simulation process have then been adapted to interact with the prototypes. A dSPACE DS1103-PPC [87] board and its associated software package (ControlDesk) [88] are installed in

FIGURE 2.17: VSI prototype used for the experimental results.

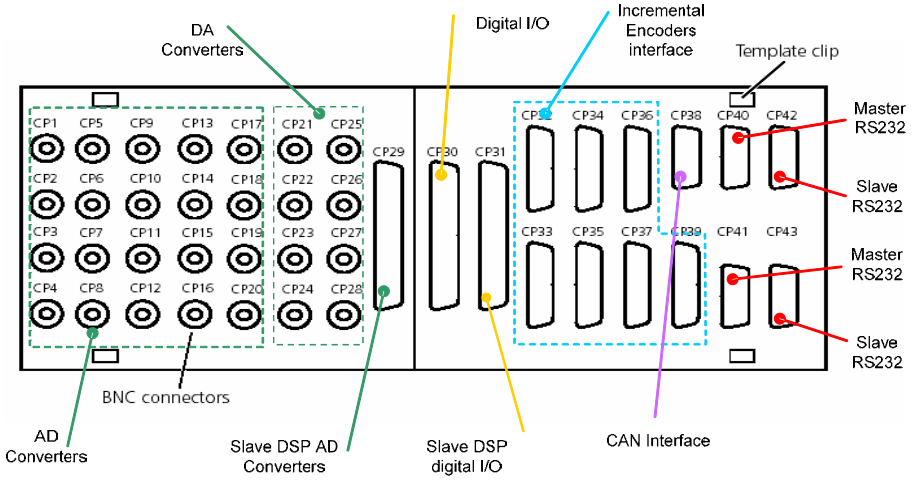


FIGURE 2.18: CP1003 connexion layout.

a PC that runs the Matlab modulation and control programs. Both converter prototypes can be connected to the dSPACE DS1103-PPC-based platform, which acts as a link between the Matlab/Simulink models and the external circuitry and facilitates the acquisition of experimental results

The dSPACE has a master-and-slave multiprocessor architecture. The master processor is a Motorola's Power-PC604 type, whereas the slave is a DSP TMS320-F240 manufactured by Texas Instruments. It includes digital input/output (I/O) ports and analog-to-digital-conversion (ADC) connectors to plug in the signals coming from the measuring transducers. Fig. 2.18 shows the appearance of the CP1103 module.

Chapter 3

Current-Balancing Techniques

This chapter presents a novel current-balancing method to ensure a fair sharing of the output currents of a VSI among the legs it is made up with. The method applies to VSIs with legs connected in parallel by means of either magnetically coupled or uncoupled inductors.

3.1 Introduction

Parallel-connected legs of a VSI require the use of inductors to obtain a single output voltage from several input legs [19–21, 85, 89, 90]. The use of uncoupled inductors does not bring any size reduction in the amount of magnetic material needed but facilitates modularity and management in case of faulty legs [21]. The use of coupled inductors provides a high impedance path for limiting the common-mode circulating currents while providing a low impedance path for the output currents [89]. Through the use of coupled inductors, a converter is capable of responding faster to a load transient depending on the coupling coefficient and control mechanism [19]. A theoretical study dealing with different options to connect multiple legs in parallel by means of transformers is developed in [85].

It would be optimal if current sharing among the legs were balanced; however, there is no guaranty for this to happen unless a proper control is used. The balancing method proposed in this chapter can achieve current balance very quickly since the exact required modification of the modulation signals is calculated and applied. The method is performed without distorting the output voltages or currents and thus it does not affect any external control loop.

3.2 Current-Balancing Method

3.2.1 Parallel Connection with Uncoupled Inductors

In this study, no magnetic coupling among the inductors is assumed, although the analysis could be extrapolated to magnetically-coupled inductors such as the configurations presented in [11]-[13]. However, in those coupling solutions, the equivalent inductance of the output phase is very small, which might be a drawback for grid-connected applications, for instance. On the other hand, if there is not magnetic coupling between the inductors, the equivalent output inductance is L/n, where n is the number of parallel-connected legs. Consequently, the same inductances used for the parallel connection among the legs contribute to the output inductance of the phase needed in grid-connected applications.

The following expression describes the relationship between voltages and currents in each leg of both versions of the system, i.e. the one made with uncoupled inductors (Fig. 2.15) and the one made with coupled inductors (Fig. 2.16).

$$L\frac{di_{aj}}{dt} = v_{aj} - v_{a0} \quad \text{for} \quad j = \{1, 2, ..., n\} \tag{3.1}$$

Adding up all the terms included in (3.1):

$$\sum_{j=1}^{n} L\frac{di_{aj}}{dt} = \sum_{j=1}^{n} \left(v_{aj} - v_{a0}\right), \tag{3.2}$$

which taking into account that

$$i_a = \sum_{j=1}^{n} i_{aj}, \tag{3.3}$$

can be written as:

$$L\frac{di_a}{dt} = \left(\sum_{j=1}^{n} v_{aj}\right) - nv_{a0} \tag{3.4}$$

or:

$$L_{eq}\frac{di_a}{dt} = v_{a\mathrm{COM}} - v_{a0}; \tag{3.5}$$

where

$$L_{eq} = \frac{L}{n} \qquad \text{and} \qquad v_{a\mathrm{COM}} = \frac{1}{n}\sum_{j=1}^{n} v_{aj}. \tag{3.6}$$

The common voltage $v_{a\mathrm{COM}}$ would be the output voltage from an equivalent single leg.

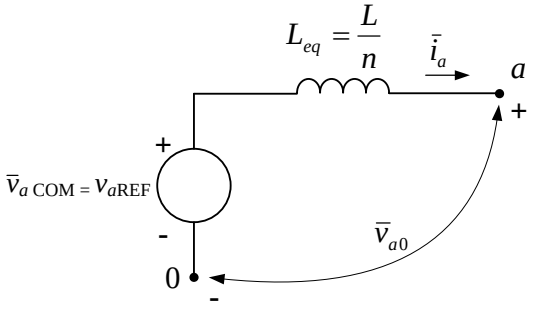


FIGURE 3.1: Averaged equivalent leg.

The locally-averaged operator is defined as follows:

$$\bar{x}(t) = \frac{1}{T_w} \int_{t-T_w}^{t} x(\tau) d\tau. \tag{3.7}$$

If the window-width (T_w) used in this operator is defined to be the same as the converter switching period, switching frequency ripples in the voltages and currents will be completely filtered and canceled; as a consequence, those variables will become continuous. Applying the locally-averaged operator to (3.5), and considering that the averaged variable $\bar{v}_{a\mathrm{COM}}$ is the same as the global reference voltage of the phase ($\bar{v}_{a\mathrm{COM}} = v_{a\mathrm{REF}}$), (3.5) becomes

$$v_{a\mathrm{REF}} - \bar{v}_{a0} = L_{eq} \frac{d\bar{i}_a}{dt} \tag{3.8}$$

where

$$v_{a\mathrm{REF}} = \bar{v}_{a\mathrm{COM}} = \frac{1}{n} \sum_{j=1}^{n} \bar{v}_{aj}, \tag{3.9}$$

which corresponds to the averaged equivalent leg of the whole phase that can be seen in Fig. 3.1.

If there were no current-balancing control in the system, the global reference of the phase would be the voltage reference provided to each leg, i.e. $\bar{v}_{aj} = v_{a\mathrm{REF}}$ for $j = \{1, 2, ..., n\}$. However, in order to provide a control law for each leg current, each individual voltage is modified as follows:

$$\bar{v}_{aj} = v_{a\mathrm{REF}} + \Delta\bar{v}_{aj} \quad \text{for} \quad j = \{1, 2, ..., n\}, \tag{3.10}$$

where $\Delta\bar{v}_{aj}$ are the control signals.

Adding the control variables $\Delta\bar{v}_{aj}$ into the expression of $\bar{v}_{a\mathrm{COM}}$ in (3.8), the following relationship is obtained:

$$\begin{aligned}\bar{v}_{a\mathrm{COM}} &= \frac{1}{n}\sum_{j=1}^{n}\left(v_{a\mathrm{REF}} + \Delta\bar{v}_{aj}\right) \\ &= v_{a\mathrm{REF}} + \frac{1}{n}\sum_{j=1}^{n}\Delta\bar{v}_{aj}.\end{aligned} \tag{3.11}$$

Taking into account that the control variables should not affect the output voltage generated by the leg ($\bar{v}_{a\mathrm{COM}} = v_{a\mathrm{REF}}$), from (3.8) and (3.11) it can be inferred that the control voltages have to meet the following condition:

$$\sum_{j=1}^{n}\Delta\bar{v}_{aj} = 0. \tag{3.12}$$

Since $\bar{v}_{a\mathrm{COM}}$ becomes unaltered if restriction (3.12) is applied, from (3.8) and its equivalent circuit in Fig. 3.10, one can conclude that $\bar{i}_a$ and $\bar{v}_{a0}$ will not be affected by the control variables either.

Applying the locally-averaged operator given in (3.7) to (3.1):

$$L\frac{d\bar{i}_{aj}}{dt} = \bar{v}_{aj} - \bar{v}_{a0} \quad \text{for} \quad j = \{1, 2, \ldots, n\} \tag{3.13}$$

and adding the effect of the control variables, the following relationship is obtained:

$$L\frac{d\left(\bar{i}_{aj} + \Delta\bar{i}_{aj}\right)}{dt} = \bar{v}_{aj} + \Delta\bar{v}_{aj} - \bar{v}_{a0} - \Delta\bar{v}_{a0} \tag{3.14}$$

in which

$$\Delta\bar{i}_{aj} = \bar{i}_{aj} - \frac{\bar{i}_a}{n}, \qquad \text{for} \qquad j = \{1, 2, \ldots, n\}. \tag{3.15}$$

Comparing (3.13) and (3.14), and considering that $\Delta\bar{v}_{a0} = 0$ as a consequence of the control restriction given in (3.12):

$$L\frac{d\Delta\bar{i}_{aj}}{dt} = \Delta\bar{v}_{aj}. \tag{3.16}$$

Assuming a current imbalance $\Delta\bar{i}_{aj}(k)$ at the instant kT_s, the voltage necessary for achieving the reference current $(\bar{i}_a/n)$ can be calculated by imposing the condition $\Delta\bar{i}_{aj}(k+1) = 0$ to the discrete representation of (3.16), as follows:

$$L\frac{\Delta\bar{i}_{aj}(k+1) - \Delta\bar{i}_{aj}(k)}{T_s} = \Delta v_{aj}(k) \tag{3.17}$$

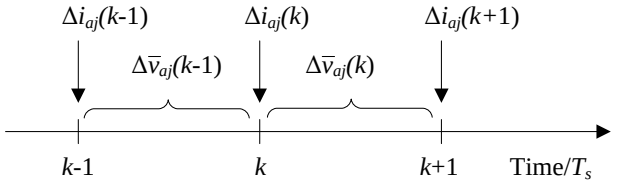


FIGURE 3.2: Time sequence of the sampling process for current-balancing.

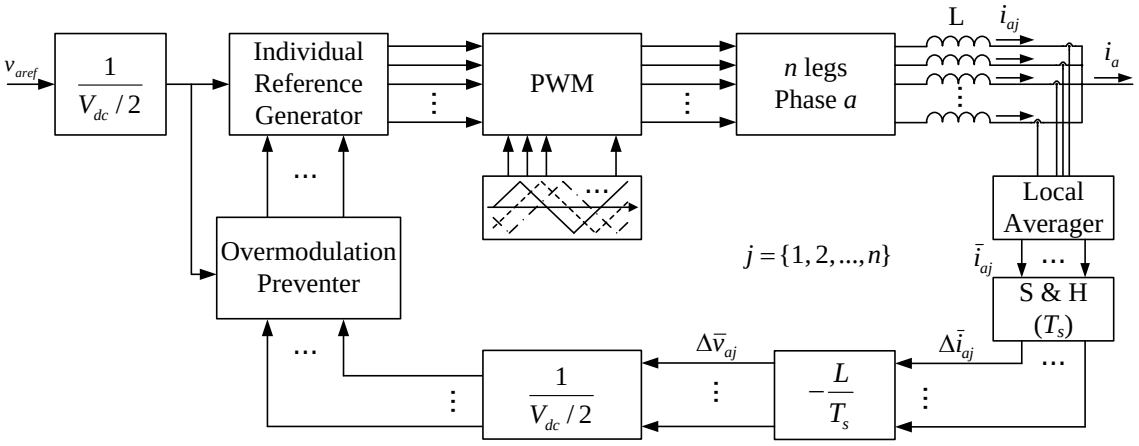


FIGURE 3.3: Current-balancing control diagram.

and as the desired value is $\Delta\bar{i}_{aj}(k+1) = 0$, the required $\Delta\bar{v}_{aj}$ value is

$$\Delta\bar{v}_{aj}(k) = -\frac{L}{T_s}\Delta\bar{i}_{aj}. \tag{3.18}$$

A timing diagram for this on-line process can be seen in Fig. 3.2.

Fig. 3.3 shows the control scheme of the current-balancing strategy for phase a. It can be seen that n current sensors are used to provide the information needed. The current of each leg (i_{aj}) is sensed and then, locally averaged ($\bar{i}_{aj}$). The local averager block in Fig. 3.3 is based on a moving average filter (MAF) with a window width equal to the carrier period, i.e. the switching period (T_{sw}). As a consequence, the current ripple of the circulating currents is completely removed. Afterwards, those averaged currents are synchronously sampled at the apparent switching period T_s (see Fig. 2.12(b)). The value of the variable $\Delta\bar{v}_{aj}$ is calculated according to (3.17) and applied to the particular modulation signal of each leg. If it were not possible to achieve the current balance in a single sampling period because of the large value required for $\Delta\bar{v}_{aj}$, this control voltage should be limited to avoid overmodulation (block "Overmodulation Preventer" in Fig. 3.3). This block trims down the biggest of the $\Delta\bar{v}_{aj}$ computed values to its maximum value without causing over-modulation and downscales the rest of the $\Delta\bar{v}_{aj}$ values accordingly. Even if this restriction had to be applied, condition (3.12) would still have to be satisfied in order to avoid distortion in the global output voltage phase.

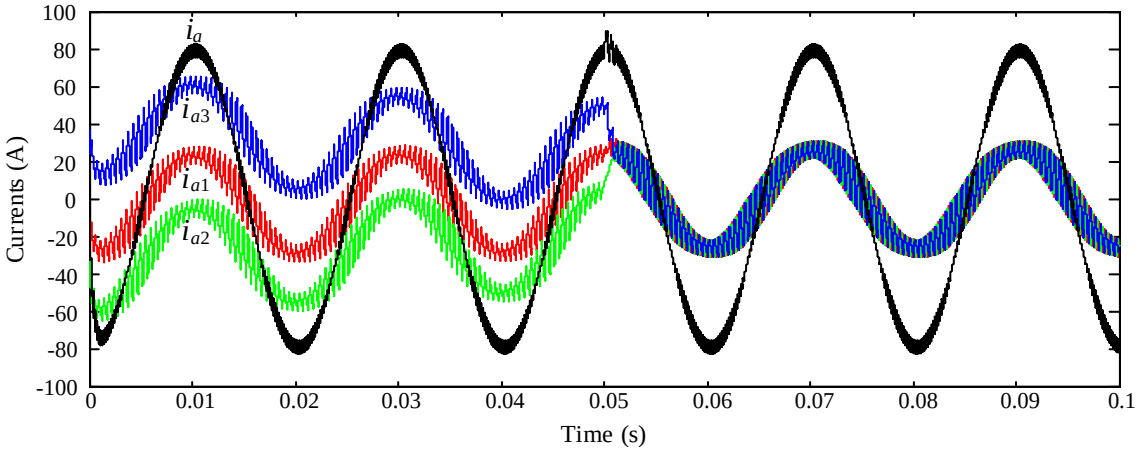


FIGURE 3.4: Simulation results for an initial current imbalance. The balancing control is activated at t=50 ms.

3.2.2 Simulation and Experimental Results

The proposed balancing strategy has been simulated by Matlab-Simulink. A single-phase converter with three parallel-connected legs has been considered. The load is resistive and it is connected between the output ("a") and the dc neutral point ("0"). The main data for the simulation are: V_{dc}= 1 kV, m_a= 0.8, fundamental frequency f= 50 Hz, carrier frequency f_{sw}= 2 kHz, sampling frequency f_s= 6 kHz, L= 5 mH with an internal resistance of R_p= 50 mΩ, and R_L= 5 Ω.

Fig. 3.4 shows the leg currents when the system starts with the balancing control disconnected. An initial current imbalance has been provoked at the beginning of the process. It can be noticed that the currents tend to be naturally balanced; however, the balancing dynamics is very slow. Since the three currents are significantly different for some time, the consequences might be critical for the legs that carry more current. The balancing control is activated at the instant t= 50 ms. One can observe that the three currents are quickly balanced and the legs carry similar current values henceforth. Thus, similar power losses are to be expected in all the transistors of the converter.

Permanent current imbalances are produced due to different voltage drops on the power devices of the legs. Even small differences among the transistor voltage drops can produce large currents imbalances, since they depend mostly on the internal resistor values of the inductances, which are usually very small. In Fig. 3.5, an additional voltage drop on the lower transistor of the leg a_1 is assumed. The system starts with a permanent current imbalance due to this voltage drop. The balancing control is activated a t=80 ms, again quickly compensating for such imbalance. It should be remarked that these kinds of permanent imbalances are much more dangerous for the legs than those

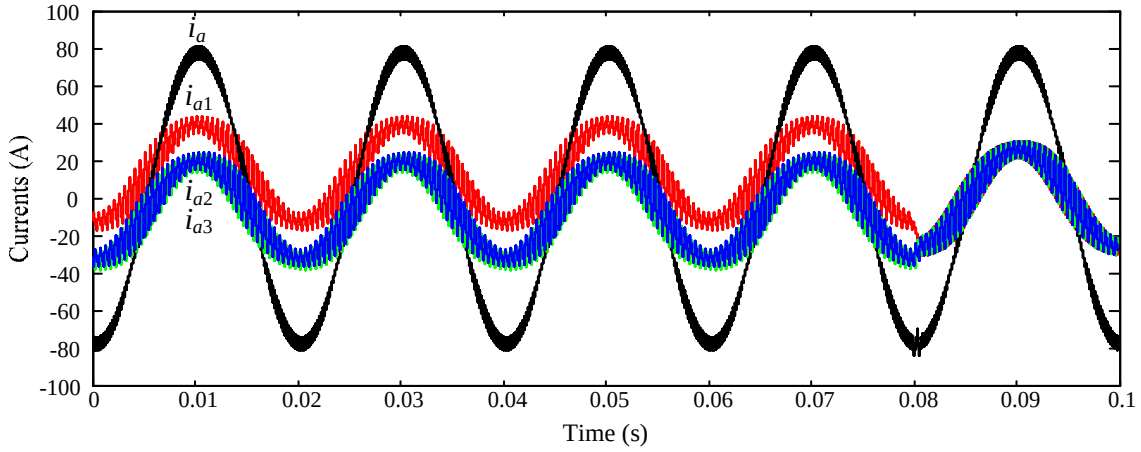


FIGURE 3.5: Simulation results assuming different voltage drops on the power devices. The balancing control is activated at t=80 ms.

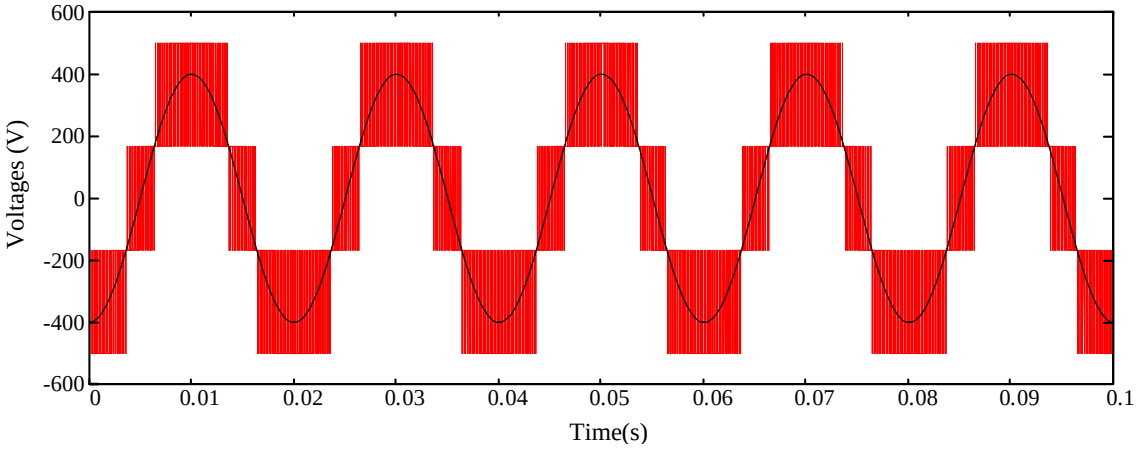
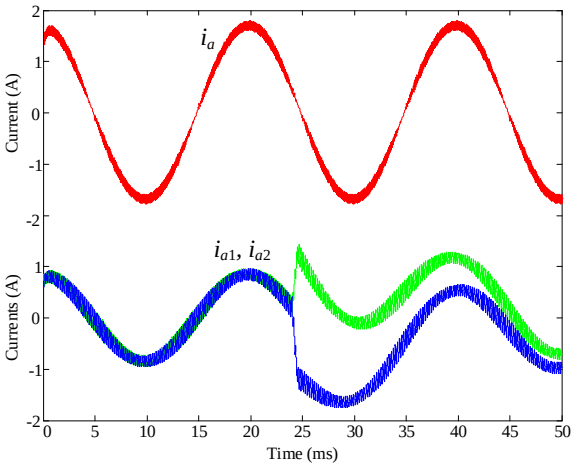


FIGURE 3.6: Simulation results of the phase-a equivalent voltage ($v_{a\mathrm{COM}}$) and its reference ($v_{a\mathrm{REF}}$).

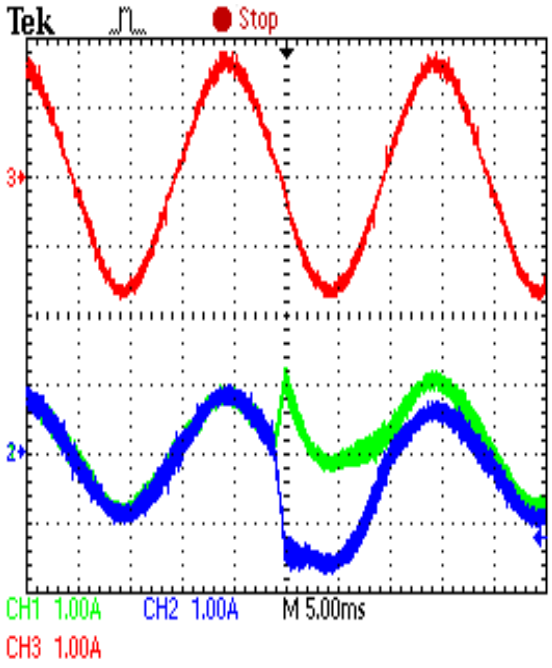
produced by transitory processes. Nevertheless, when the controller is activated the currents become balanced very quickly, no matter what the reason for the imbalance is.

Fig. 3.6 shows the equivalent voltage of phase a, i. e. $v_{a\mathrm{COM}} = (v_{a1} + v_{a2} + v_{a3})/3$. It can be seen that the equivalent voltage takes four levels as it does in a multilevel converter. This figure also shows the voltage reference signal for that phase.

A single-phase laboratory prototype has been used to verify the proposed current-balancing strategy. The converter has two parallel-connected legs and operates over a resistive load. The main parameters are: V_{dc}= 50 V, m_a= 0.7, f= 50 Hz, f_{sw}= 5 kHz, f_s= 10 kHz, L= 6 mH with an internal resistance of R_p= 0.54 Ω, and R_L= 10 Ω. All the figures presented henceforth include simulation and experimental results. In Fig. 3.7, a current imbalance is produced. This imbalance is achieved by applying an instantaneous uncontrolled Δv_a to the modulation signals of the legs. The current compensator is not activated in this experiment. Although the two leg currents are naturally balanced, they



(a)

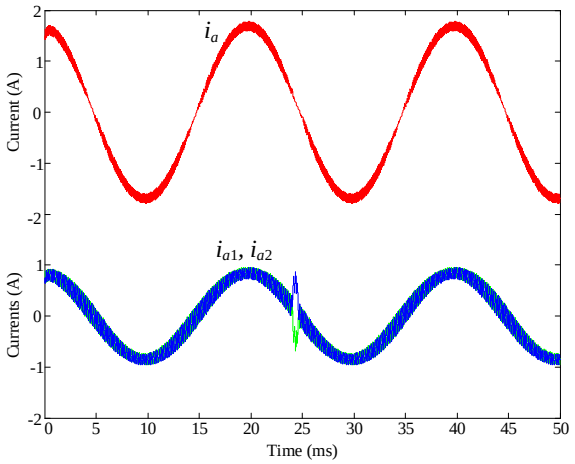


(b)

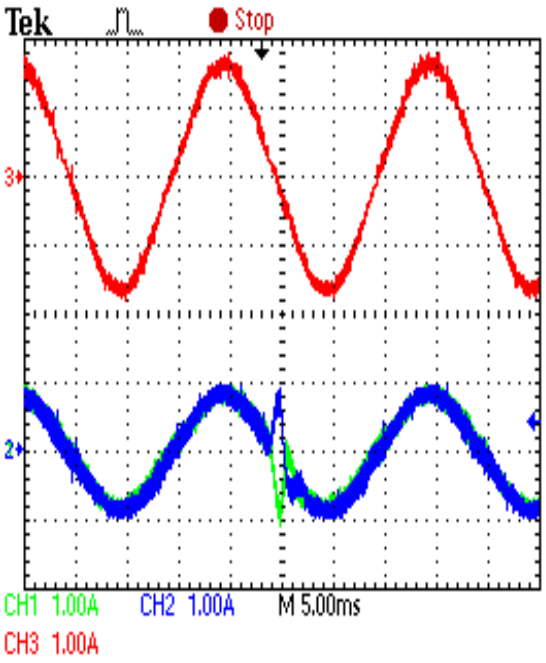
FIGURE 3.7: Two parallel legs operating without the balance compensator. (a) Simulation results. (b) Experimental results.

remain unbalanced for some time related to the time constant τ. The time constant value is much larger in real high power systems because resistors associated to huge power inductors are very small. Hence, transitory imbalances would produce significant stress to the power semiconductors of the legs.

A similar process is presented in Fig. 3.8 with the compensator activated. One can observe how the proposed compensator can balance currents very quickly. It can be noticed that the output current has practically no distortion due to compensation. This is because the controller only produces differential voltage for current compensation, but it does not change the global output voltage generated by the phase.



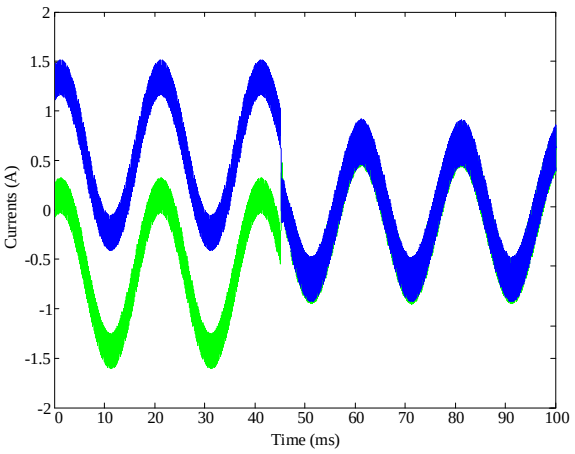
(a)



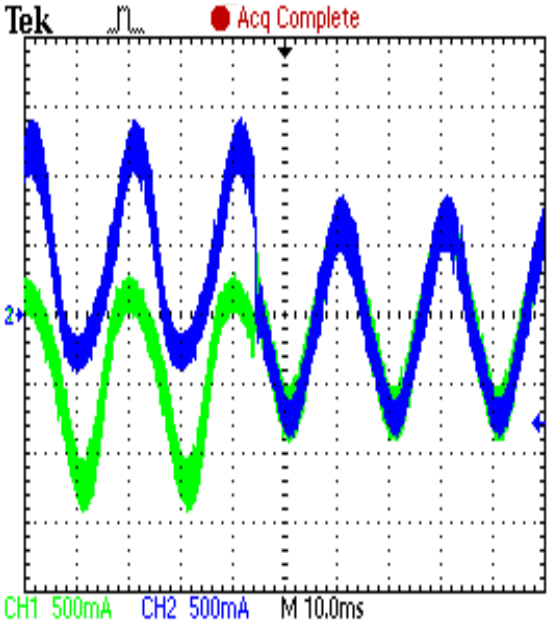
(b)

FIGURE 3.8: Two parallel legs operating with the balance compensator activated. (a) Simulation results. (b) Experimental results.

In order to emulate the case of different voltage drops in the transistors of the legs, a low dc-voltage battery has been added to the output of one leg. This would create a permanent current imbalance. Fig. 3.9 shows some current waveforms from the system starting with such current imbalance. When the control is activated, the currents are balanced almost instantaneously.



(a)



(b)

FIGURE 3.9: Current imbalance produced by a small dc voltage difference between the legs and activation of the compensator. (a) Simulation results. (b) Experimental results.

3.2.3 Parallel Connection with Coupled Inductors

Fig. 2.16 shows an example of parallel-connected legs where multiple magnetic coupling among the inductors is assumed, although the analysis could be extrapolated to different types of coupling, like the ones presented in [85]. The n legs shown in these schemes correspond to one single phase of the converter (phase a, for instance).

A similar analysis to that performed in Section 3.2.2 is done in this section. In this case, the coupling parameters between inductors are taken into account. As a

consequence, matrix formulation is more convenient. The relationship between voltages and currents in each leg of the system depicted in Fig. 2.16 is

$$\mathbf{V}_a = \mathbf{L}\frac{d}{dt}\mathbf{I}_a + \mathbf{V}_{a0}, \tag{3.19}$$

where

$$\mathbf{V}_a = \begin{bmatrix} v_{a1} \\ v_{a2} \\ \vdots \\ v_{an} \end{bmatrix}, \qquad \mathbf{I}_a = \begin{bmatrix} i_{a1} \\ i_{a2} \\ \vdots \\ i_{an} \end{bmatrix}, \qquad \mathbf{V}_{a0} = \begin{bmatrix} v_{a0} \\ v_{a0} \\ \vdots \\ v_{a0} \end{bmatrix}, \tag{3.20}$$

and

$$\mathbf{L} = \begin{bmatrix} L_1 & -M_{12} & -M_{13} & \dots & -M_{1n} \\ -M_{12} & L_2 & -M_{23} & \dots & -M_{2n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -M_{1n} & -M_{2n} & -M_{3n} & \dots & L_n \end{bmatrix}. \tag{3.21}$$

Considering a symmetrical magnetic structure for the whole set of inductors, (3.19) could be stated as

$$\begin{bmatrix} v_{a1} \\ v_{a2} \\ \vdots \\ v_{an} \end{bmatrix} = \begin{bmatrix} L & -M & \dots & -M \\ -M & L & \dots & -M \\ \vdots & \vdots & \ddots & \vdots \\ -M & -M & \dots & L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{a1} \\ i_{a2} \\ \vdots \\ i_{an} \end{bmatrix} + \begin{bmatrix} v_{a0} \\ v_{a0} \\ \vdots \\ v_{a0} \end{bmatrix}. \tag{3.22}$$

Adding all the single equations in (3.22) leads to

$$\sum_{j=1}^{n} v_{aj} = [L - (n-1)M] \sum_{j=1}^{n} \frac{di_{aj}}{dt} + n v_{a0}. \tag{3.23}$$

Provided that the output current is made up of the phase-leg currents

$$i_a = \sum_{j=1}^{n} i_{aj}, \tag{3.24}$$

and $v_{a\mathrm{COM}}$ being the equivalent average output voltage of the n phase-legs, i.e. the voltage that would be generated from an equivalent single leg

$$v_{a\mathrm{COM}} = \frac{1}{n} \sum_{j=1}^{n} v_{aj}, \tag{3.25}$$

(3.23) can be written as

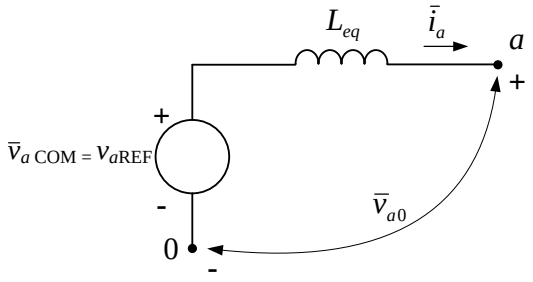


FIGURE 3.10: Averaged equivalent leg.

$$v_{a\mathrm{COM}} - v_{a0} = \left(\frac{L}{n} - \frac{n-1}{n}M\right)\frac{di_a}{dt}. \tag{3.26}$$

Calling L_{eq} the equivalent output inductance of that fictitious leg

$$L_{eq} = \frac{L}{n} - \frac{n-1}{n}M, \tag{3.27}$$

(3.26) becomes

$$v_{a\mathrm{COM}} - v_{a0} = L_{eq}\frac{di_a}{dt}. \tag{3.28}$$

If the window-width (T_w) used in the locally-averaged operator (3.7) is defined to be the same as the converter switching period, switching frequency ripples in the voltages and currents will be completely filtered and canceled; as a consequence, those variables will become continuous. Applying the locally-averaged operator to (3.28), and considering that the averaged variable $\bar{v}_{a\mathrm{COM}}$ becomes the global reference voltage of the phase ($\bar{v}_{a\mathrm{COM}} = v_{a\mathrm{REF}}$), (3.28) becomes

$$v_{a\mathrm{REF}} - \bar{v}_{a0} = L_{eq}\frac{d\bar{i}_a}{dt} \tag{3.29}$$

that corresponds to the averaged equivalent leg of the whole phase that can be seen in Fig. 3.10.

If there were no current-balancing control in the system, the voltage reference provided to each leg and the global reference of the phase would be the same, i.e. $\bar{v}_{aj} = v_{a\mathrm{REF}}$ for $j = \{1, 2, ..., n\}$ or

$$\bar{\mathbf{V}}_a = \begin{bmatrix} \bar{v}_{a1} \\ \bar{v}_{a2} \\ \vdots \\ \bar{v}_{an} \end{bmatrix} = \begin{bmatrix} v_{a\mathrm{REF}} \\ v_{a\mathrm{REF}} \\ \vdots \\ v_{a\mathrm{REF}} \end{bmatrix}. \tag{3.30}$$

In order to provide a control law for each leg current, each individual voltage is modified as follows:

$$\bar{v}_{aj} = v_{a\mathrm{REF}} + \Delta\bar{v}_{aj} \quad \text{for} \quad j = \{1, 2, ..., n\}, \tag{3.31}$$

where $\Delta\bar{v}_{aj}$ are the control signals.

Applying the locally-averaged operator to (3.19) allows it to be written as

$$\bar{\mathbf{V}}_a = \mathbf{L}\frac{d}{dt}\bar{\mathbf{I}}_a + \bar{\mathbf{V}}_{a0}. \tag{3.32}$$

When including the effect of the control variables ($\Delta\bar{v}_{aj}$) into (3.32), this becomes

$$\bar{\mathbf{V}}_a + \Delta\bar{\mathbf{V}}_a = \mathbf{L}\frac{d}{dt}(\bar{\mathbf{I}}_a + \Delta\bar{\mathbf{I}}_a) + \bar{\mathbf{V}}_{a0} + \Delta\bar{\mathbf{V}}_{a0}. \tag{3.33}$$

The Δ terms that derive from such control variables can be isolated by subtracting (3.32) from (3.33), that leads to

$$\Delta\bar{\mathbf{V}}_a = \mathbf{L}\frac{d}{dt}\Delta\bar{\mathbf{I}}_a + \Delta\bar{\mathbf{V}}_{a0}, \tag{3.34}$$

where

$$\Delta\bar{\mathbf{V}}_a = \begin{bmatrix} \Delta\bar{v}_{a1} \\ \Delta\bar{v}_{a2} \\ \vdots \\ \Delta\bar{v}_{an} \end{bmatrix}, \tag{3.35}$$

$$\Delta\bar{\mathbf{I}}_a = \begin{bmatrix} \bar{i}_{a1} - \bar{i}_a/n \\ \bar{i}_{a2} - \bar{i}_a/n \\ \vdots \\ \bar{i}_{an} - \bar{i}_a/n \end{bmatrix}, \tag{3.36}$$

and

$$\Delta\bar{\mathbf{V}}_{a0} = \begin{bmatrix} \Delta\bar{v}_{a0} \\ \Delta\bar{v}_{a0} \\ \vdots \\ \Delta\bar{v}_{a0} \end{bmatrix}. \tag{3.37}$$

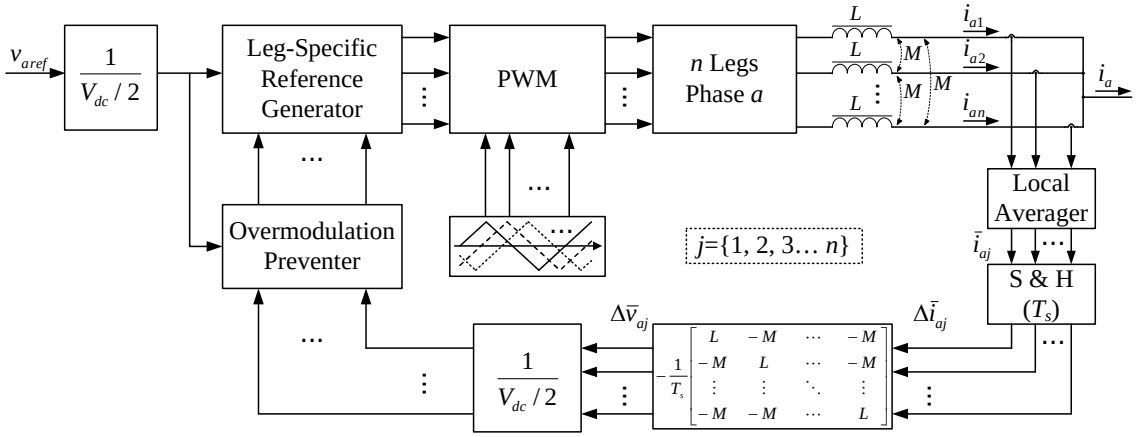


FIGURE 3.11: Current-balancing control diagram.

Considering the control variables introduced in (3.31), (3.25) can be stated as

$$\begin{aligned} \bar{v}_{a\mathrm{COM}} &= \frac{1}{n}\sum_{j=1}^{n}(v_{a\mathrm{REF}} + \Delta\bar{v}_{aj}) \\ &= v_{a\mathrm{REF}} + \frac{1}{n}\sum_{j=1}^{n}\Delta\bar{v}_{aj}. \end{aligned} \tag{3.38}$$

Bearing in mind that the control variables should not affect the output voltage generated by the leg ($\bar{v}_{a\mathrm{COM}} = v_{a\mathrm{REF}}$), one can conclude that the control voltages have to meet the following condition:

$$\sum_{j=1}^{n}\Delta\bar{v}_{aj} = 0. \tag{3.39}$$

Since $\bar{v}_{a\mathrm{COM}}$ becomes unaltered if restriction (3.39) is applied, from (3.29) and its equivalent circuit in Fig. 3.10, it can be inferred that $\bar{i}_a$ and $\bar{v}_{a0}$ will not be affected by the control variables either. As a consequence, $\Delta\bar{\mathbf{V}}_{a0} = 0$ and therefore (3.34) becomes

$$\Delta\bar{\mathbf{V}}_a = \mathbf{L}\frac{d}{dt}\Delta\bar{\mathbf{I}}_a. \tag{3.40}$$

When the phase current is equally shared among the phase legs, i.e. $\bar{i}_{aj} = \bar{i}_a/n$ for $j = \{1, 2, \ldots, n\}$, then $\Delta\bar{\mathbf{I}}_a = 0$. If there were a current imbalance ($\Delta\bar{\mathbf{I}}_a \neq 0$) at the instant kT_s, the discrete representation of (3.40)

$$\boldsymbol{\Delta}\bar{\mathbf{V}}_a(k) = \frac{1}{T_s}\mathbf{L}[\Delta\bar{\mathbf{I}}_a(k+1) - \Delta\bar{\mathbf{I}}_a(k)] \tag{3.41}$$

could be used to compute the control voltages necessary to achieve a fairly shared current in the next sampling period by imposing the condition $\Delta\bar{\mathbf{I}}_a(k+1) = 0$, that would render

$$\boldsymbol{\Delta}\bar{\mathbf{V}}_a(k) = -\frac{1}{T_s}\mathbf{L}\Delta\bar{\mathbf{I}}_a(k). \tag{3.42}$$

Fig. 3.11 shows the control diagram of the current-balancing technique for phase *a*. The local averager block in Fig. 3.11 is based on a moving average filter (MAF) with a window width equal to the carrier period, i.e. the switching period (T_{sw}). As a consequence, the current ripple of the circulating currents is completely removed. On the other hand, the sampling period of the converter controller, which includes the current-balancing control, is at the apparent switching period, i.e. T_s, as shown in Fig. 3.2. This period is smaller than T_{sw} ($T_s = T_{sw}/n$) and therefore, the dynamic of the converter becomes faster. Ideally, all the reference signals should be updated at any sampling period (T_s). However, in some practical implementations, updating the reference signal may not be feasible until the corresponding carrier signal of the specific leg completes a PWM cycle. In those cases, only one reference signal is updated at a time, just before its carrier signal cycle starts.

It can be seen in Fig. 3.11 that n current sensors are used to provide the information needed. The current of each leg (i_{aj}) is sensed and then, locally averaged ($\bar{i}_{aj}$) with a window width of T_{sw}. Afterwards, those averaged currents are synchronously sampled every apparent switching period T_s (see Fig. 2.12(b)). The values of the Δv_{aj} variables are calculated according to (3.42) and, after checking that they will not cause over-modulation, applied to the specific modulation signal for each leg. In case that the Δv_{aj} values required to achieve the current balance were such that some of the them might cause over-modulation in their legs, i.e. $|v_{a\mathrm{REF}} + \Delta\bar{v}_{aj}| > 1$, the biggest one would have to be trimmed down to its maximum possible value and the rest of them rescaled accordingly in order to make sure that condition (3.39) is always met. That is to avoid distortion in the overall output voltage phase, even if some of the Δv_{aj} values had to be limited because of the aforementioned restriction. This task is performed by the "Overmodulation Preventer" block that can be seen in Fig. 3.11.

3.2.4 Implementation of Multi-Coupled Inductors

The implementation of a multi-coupled set of inductors by means of a common magnetic core with several windings implies some assembly difficulties if a total symmetry is to be achieved. In other words, it would be difficult to attain that all the M_{ij} terms (for

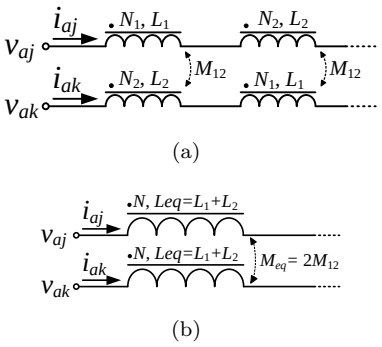


FIGURE 3.12: Transformers between two generic legs in a combinatorial cascade connection. (a) Original configuration. (b) Equivalent configuration.

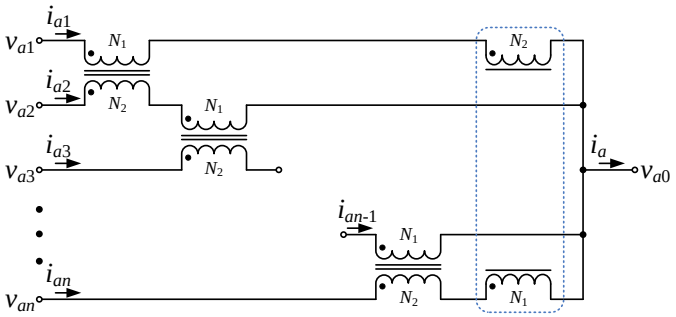


FIGURE 3.13: Cyclic cascade connection.

$i, j = \{1, 2, ..., n\}$ and $i \neq j$) included in (3.21) be of the same value. An equivalent multi-coupling effect can be achieved by using only one-to-one coupled inductors (transformers) as described below.

Assuming that all the magnetic cores of the transformers have the same reluctance ($\Re$) and calling i_p and i_s the currents in their primary and secondary windings respectively, the magnetic flux in each core is

$$\Phi = \frac{N_1 i_p - N_2 i_s}{\Re} \tag{3.43}$$

where N_1 and N_2 are the number of turns of each winding. The inductance parameters in each transformer are

$$L_1 = N_1 \frac{d\Phi}{di_p} = \frac{N_1^2}{\Re}, \tag{3.44}$$

$$L_2 = -N_2 \frac{d\Phi}{di_s} = \frac{N_2^2}{\Re}, \tag{3.45}$$

$$M = N_1 \frac{d\Phi}{di_s} = -N_2 \frac{d\Phi}{di_p} = \frac{N_1 N_2}{\Re}. \tag{3.46}$$

In a cyclic cascade connection [85], two transformers are used in every leg, as shown in Fig. 3.13. Every transformer links the current in one leg to the current in the next

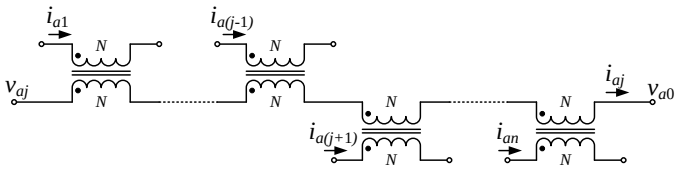


FIGURE 3.14: Generic leg in a combinatorial cascade connection.

one, except for the last one that is linked to the first one. In this configuration, (3.21) becomes

$$\mathbf{L} = \begin{bmatrix} L_1 + L_2 & -M_{12} & 0 & \dots & -M_{12} \\ -M_{12} & L_1 + L_2 & -M_{12} & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -M_{12} & 0 & \dots & -M_{12} & L_1 + L_2 \end{bmatrix}. \tag{3.47}$$

Comparing (3.47) to (3.21) and (3.22), it can be observed that:

$$L = L_1 + L_2 = \frac{N_1^2 + N_2^2}{\Re}, \tag{3.48}$$

and the term M is either zero or

$$M = M_{12} = \frac{N_1 N_2}{\Re}. \tag{3.49}$$

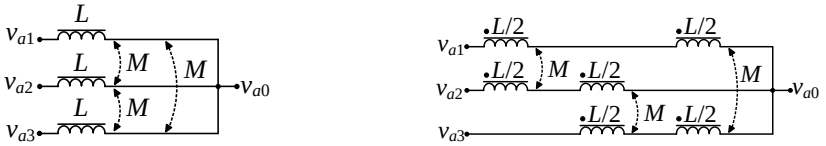
The M/L ratio can be adjusted by means of the number of turns in each winding (N_1 and N_2) according to the expression

$$\frac{M}{L} = \frac{N_1 N_2}{N_1^2 + N_2^2} = \frac{1}{\frac{N_1}{N_2} + \frac{N_2}{N_1}}, \tag{3.50}$$

and its maximum value is

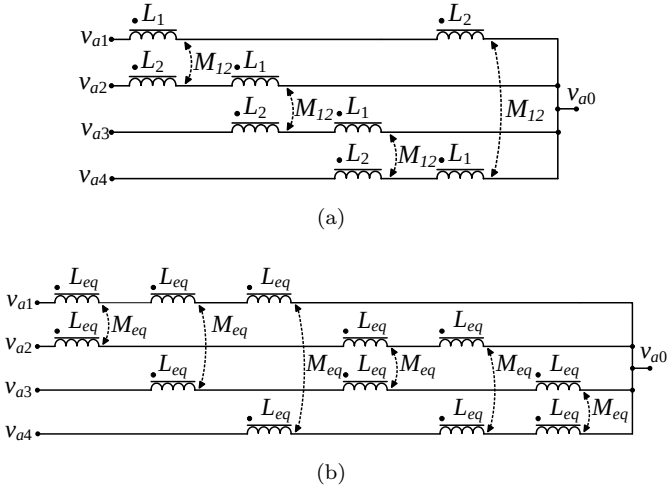
$$\frac{M}{L} = \frac{1}{2}. \tag{3.51}$$

In the cycling cascade connection, some mutually coupling coefficients of the matrix are zero. The combinatorial cascade connection [85] can achieve that all the mutually coupling coefficients be equal and different from zero. In such a connection, the current in each leg should be magnetically coupled to the current in each of the other $n-1$ legs. In order to ensure a complete magnetic symmetry that would require the use of $2(n-1)$ transformers; $n-1$ to be connected through their primary winding to the other legs, and $n-1$ to be connected through their secondary winding. Fig. 3.12(a) shows the transformers between two legs in the combinational cascade connection, where N_1 and N_2 are the turns in the primary and secondary windings of the $2(n-1)$ transformers, L_1 and L_2 their respective inductances, and M_{12} the mutually coupling coefficient. This theoretical set of $2(n-1)$transformers, is equivalent to a set of $(n-1)$ transformers with



(a) (b)

FIGURE 3.15: (a) Three multi-coupled inductors. (b) Cyclic/combinatorial cascade connection.



(a)

(b)

FIGURE 3.16: Coupling four voltage sources with transformers. (a) Cyclic cascade coupling. (b) Combinatorial cascade coupling.

a number of turns N in each of their windings and their magnetic parameters would be $L_{eq} = L_1 + L_2$ and $M_{eq} = 2M_{12}$. An equivalent transformer between two generic legs is shown in Fig. 3.12(b). Fig. 8 presents the magnetic links among the inductors connected in series in a generic leg and the coupled ones connected in the rest of the legs.

In such a combinatorial cascade configuration (3.21) becomes

$$\mathbf{L} = \begin{bmatrix} (n-1)L_{eq} & -M_{eq} & \dots & -M_{eq} \\ -M_{eq} & (n-1)L_{eq} & \dots & -M_{eq} \\ \vdots & \vdots & \ddots & \vdots \\ -M_{eq} & -M_{eq} & \dots & (n-1)L_{eq} \end{bmatrix}. \tag{3.52}$$

Comparing (3.52) to (3.21) and (3.22), it can be observed that $L = (n-1)L_{eq}$ and $M = M_{eq}$. Therefore, the ratio between these parameters is:

$$\frac{M}{L} = \frac{M_{eq}}{(n-1)L_{eq}} = \frac{2}{(n-1)\left(\frac{N_1}{N_2} + \frac{N_2}{N_1}\right)}. \tag{3.53}$$

TABLE 3.1: Specifications of the Laboratory Prototype

Symbol	Parameter	Value
V_{dc}	dc-bus voltage	60 V
f	Reference signal frequency	50 Hz
m_a	Modulation index	0.8
n	Number of legs	2/3
f_{sw}	Carrier/switching frequency	2 kHz
f_s	Apparent switching frequency	4/6 kHz
R_L	Load resistance	3.3 Ω
L	Self inductance	8.8 mH
M	Coupling inductance	2.8 mH

The disposition of the transformers in a four-leg cyclic cascade coupling is shown in Fig. 3.16(a), whereas the combinatorial one is shown in Fig. 3.16(b). For the three-coupled-leg case (Fig. 3.15), if $N_1 = N_2$ both the cyclic cascade and the combinatorial cascade structures are equivalent.

3.2.5 Simulation and Experimental Results

The proposed balancing technique has firstly been simulated on a Matlab-Simulink model. Then, it has been implemented on a dSPACE DS1103 PPC Controller board and verified on a single-phase laboratory prototype whose schemes are depicted in Fig. 3.17. The single-phase converter has two/three legs connected in parallel and drives a resistive load connected between the output ("a") and the dc neutral point ("0"). The main parameters are shown in Table 4.2.

In order to achieve a multi-coupling effect among the inductors (Fig. 3.15(a)) by using only one-to-one coupled inductors, the cyclic cascade connection shown in Fig. 3.15(b) has been used.

An occasional instantaneous disturbance Δv_{a0} is applied to the modulation of the reference signals in the captures in Fig. 3.18 to Fig. 3.21. It can be observed that when the balance controller is activated such distorting source is not significantly affecting the output currents. Comparing the current waveforms without balancing control (Figs. 3.18 and 3.20) to the ones with balancing control (Figs. 3.19 and 3.21) it is noteworthy that the currents are fairly shared when the controller is on.

Permanent current imbalances can happen on account of different voltage drops across the power devices when they are in the on state. Such drifts might produce different dc offsets among the output voltages of the legs. As a result, provided that inductors cannot stop dc circulating currents, the resistances among the legs are the ultimate elements capable of limiting this type of circulating currents. Since the internal

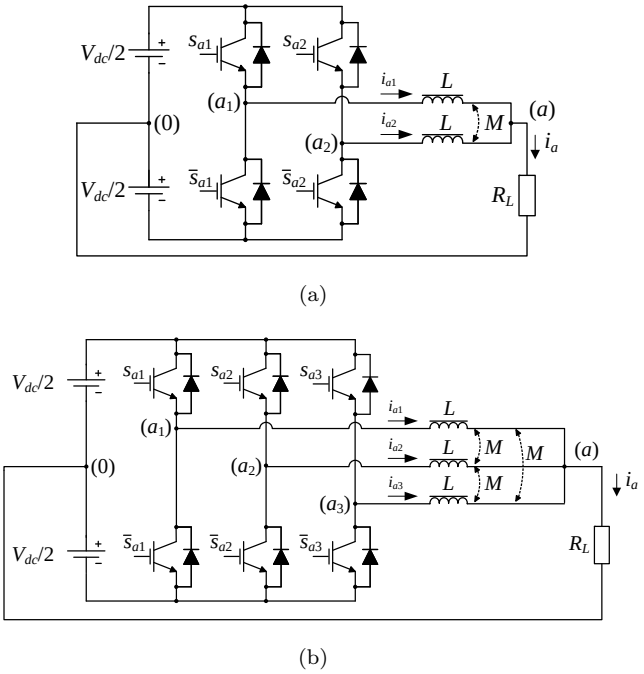


FIGURE 3.17: Laboratory prototype schemes with (a) two and (b) three legs in parallel.

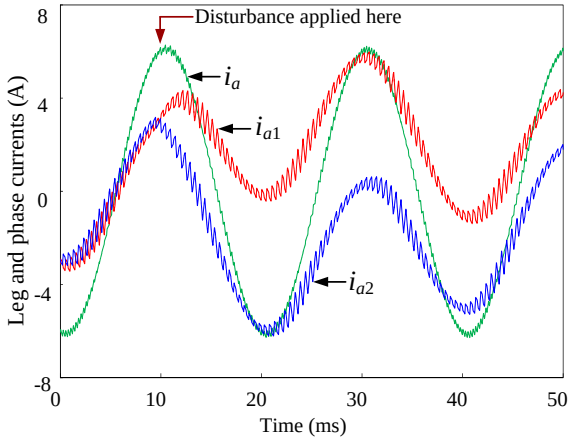
resistor values of the inductances are very small, even small differences among the voltage drops across the transistors can cause large current imbalances. It should be remarked that these kinds of permanent imbalances are much more dangerous for the legs than those produced by transitory processes.

Fig. 3.22(a) shows a VSI with two legs connected in parallel where the lower switch $\bar{s}_{a1}$ has an additional voltage drop (ΔV_{dc}) compared to the other switches. This will produce a dc voltage component in the leg-to-leg voltage. The equivalent circuit for the dc components is shown in Fig. 3.22(b). In the steady state, the dc circulating current would be:

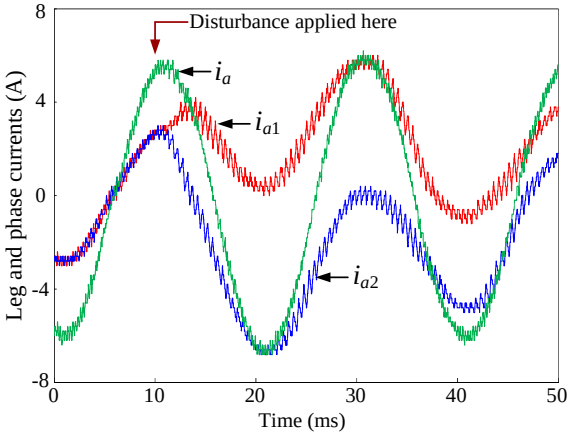
$$I_{dc} = \frac{\Delta V_{dc}}{2R}. \tag{3.54}$$

In order to emulate the case of different voltage drops in the transistors of the legs, a 1-V battery has been connected in series with the lower transistor of one leg. This creates a permanent current imbalance. Fig. 3.23 shows current waveforms from the system starting with such current imbalance. When the control is activated, the currents are balanced almost instantaneously as the proposed controller can compensate for the different dc output voltages produced in the legs. In real high power systems, where resistors associated to huge power inductors are very small, the dc component of the circulating current can be significant.

For instance, if $\Delta V_{dc} = 0.1V$ and $R = 10$ mΩ, according to (3.54), the dc component of the circulating current would be 5 A. In other words, the output current in Leg 1



(a)

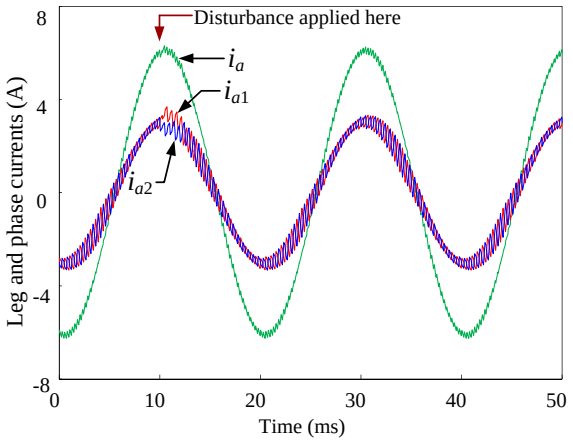


(b)

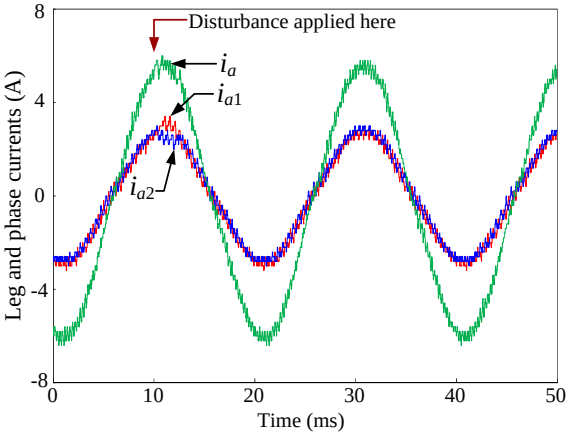
FIGURE 3.18: Disturbance effect on the currents of two legs connected in parallel without balancing control: (a) Simulation results. (b) Experimental results.

(s_{a1}, $\bar{s}_{a1}$) would be level shifted by 5A and the output current in Leg 2 (s_{a2}, $\bar{s}_{a2}$) by -5A (ΔI_a= 5A), which is a significant value.

One can observe how the output current has practically no distortion due to compensation. This is because the controller only produces differential voltage for current compensation, but it does not change the global output voltage generated by the phase.

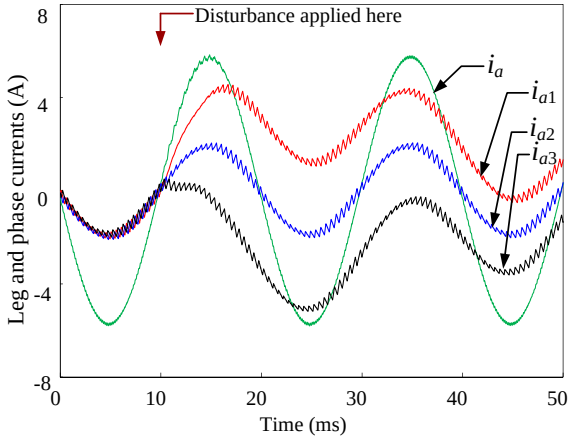


(a)

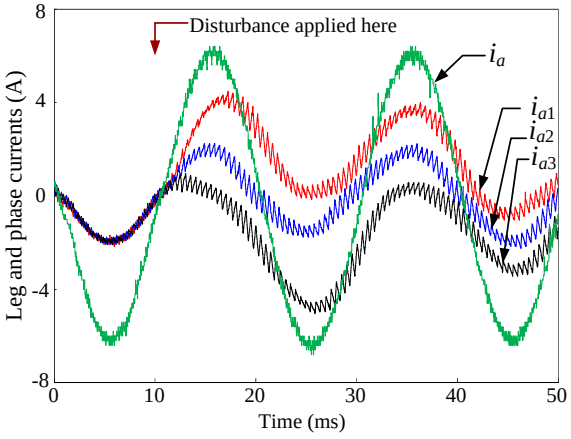


(b)

FIGURE 3.19: Disturbance effect on the currents of two legs connected in parallel with balancing control: (a) Simulation results. (b) Experimental results.

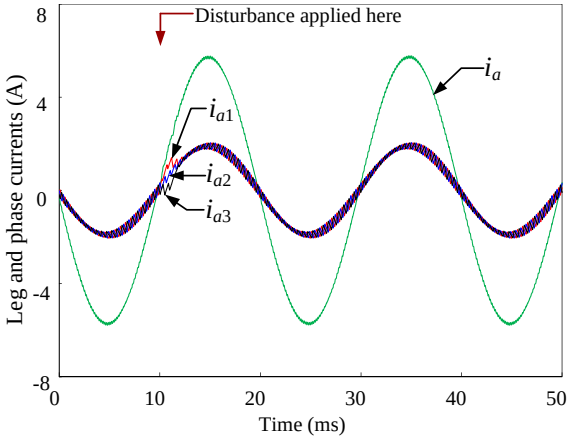


(a)

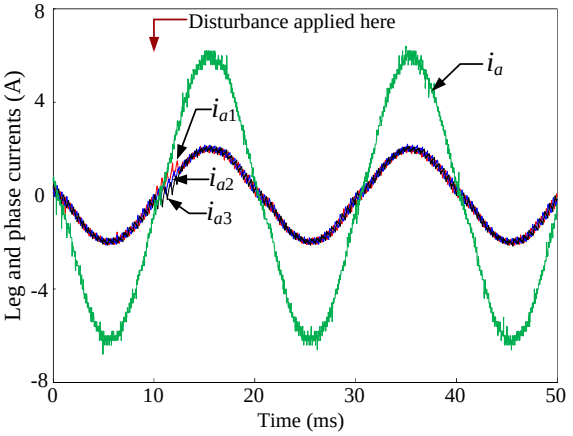


(b)

FIGURE 3.20: Disturbance effect on the currents of three legs connected in parallel without balancing control: (a) Simulation results. (b) Experimental results.

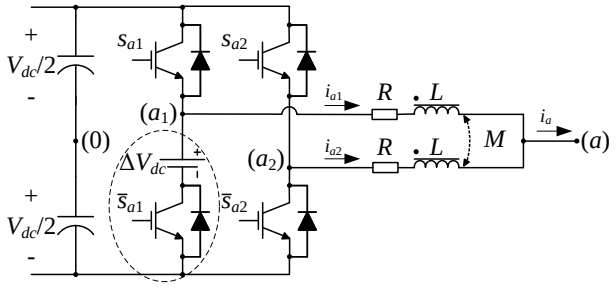


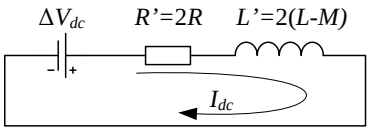
(a)



(b)

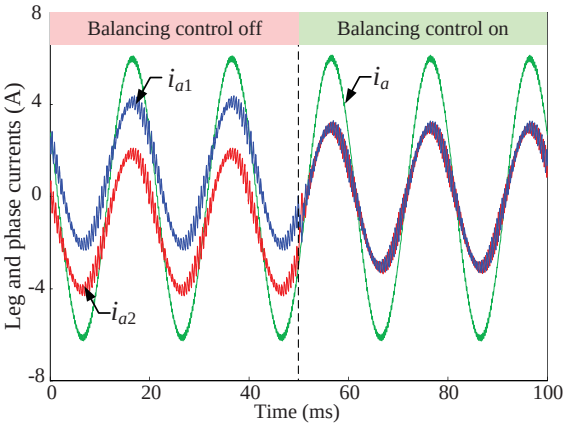
FIGURE 3.21: Disturbance effect on the currents of three legs connected in parallel with balancing control: (a) Simulation results. (b) Experimental results.



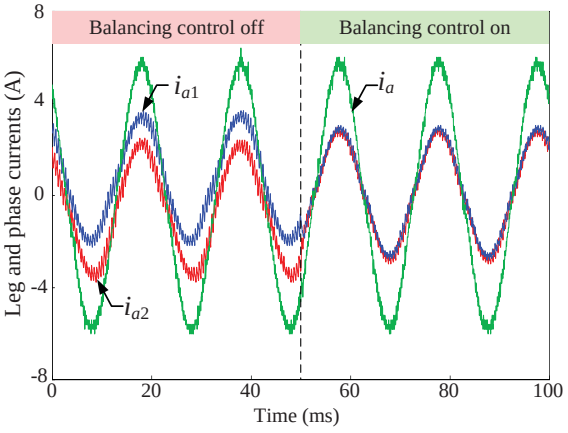


(b)

FIGURE 3.22: Example of two legs connected in parallel where one switch $\bar{s}_{a1}$ has a larger voltage drop. (a) Circuit diagram. (b) Equivalent leg-to-leg circuit for the dc components.



(a)



(b)

FIGURE 3.23: Current imbalance caused by a small dc voltage difference for the 2-leg case. (a) Simulation results. (b) Experimental results.

3.3 Conclusion

Achieving evenly shared currents among the parallel-connected legs of a power inverter is a remarkable challenge. The control technique presented in this chapter is capable of achieving a fair current distribution with very fast dynamics. It is based on calculating the exact control actuation needed for current balance; therefore, no PI controller is required. Because of its generic formulation, the proposed balancing technique can be applied to converters with any number of legs connected in parallel. The balancing method has been applied first to the case of uncoupled inductors and then to the general case of coupled inductors. As it has been shown, magnetic coupling can be achieved by the use of several one-to-one magnetic couplings or transformers.

Experimental results are provided to validate the behavior of the proposed compensator. The results show that currents are quickly balanced no matter what the reason for the imbalance is. Permanent current imbalances are the most dangerous and can be provoked by slight differences in the voltage drops across the power semiconductors.

Chapter 4

Single Carrier Modulator for Interleaved Operation of Parallel Phase-Legs in Voltage-Source Converters

The implementation of an interleaved PS-PWM scheme for VSIs with legs connected in parallel usually requires the use of a set of n evenly phase-shifted carriers. This can be rather demanding in terms of timing resources when implemented on a DSP. This chapter presents a modulation scheme that achieves the same results by using just one carrier.

4.1 Introduction

A new implementation of a carrier-based modulation strategy capable of producing interleaving by using only one carrier signal is presented next. One intrinsic advantage of the proposed technique is that it ensures the perfect synchronization required among the equivalent carriers that are being substituted. The methodology is general and, therefore, can be applied to converters with any numbers of legs connected in parallel. This inherent modularity is another advantage worth being emphasized. Although the proposed modulation approach does not alleviate the processing overhead for the controller because its interrupt rate is n times higher, what it really allows is the capability of implementing it with only one carrier. Furthermore, the dynamics of the system could benefit from this higher, synchronous sampling rate if taken into account when designing whatever control scheme may be used.

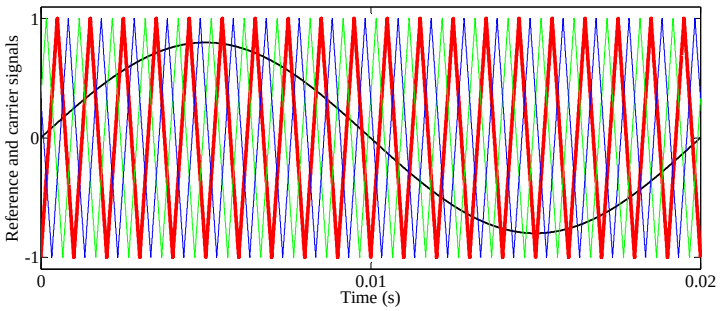
FIGURE 4.1: Phase a modulators having their own independent reference signal and their specific carrier.

4.2 Interleaved Parallel-Connected Legs

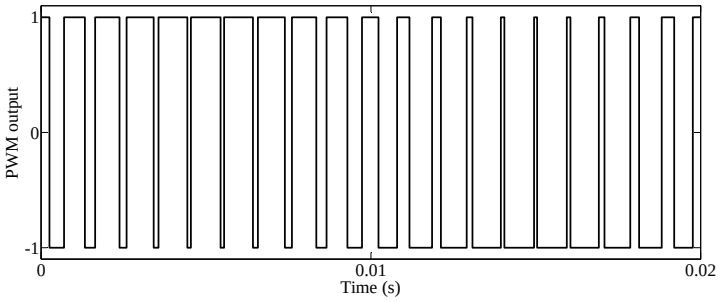
Figs. 2.15 and 2.16 show some examples of one of the phases of a converter (phase a, for instance) with n parallel-connected legs. Although the n legs shown in this scheme correspond to one single phase, connecting legs in parallel can actually apply to converters with any number of phases.

Carrier-based PWM is a simple and effective way to set up the state of the switches in a VSC. The current balancing control presented in [25] relies on the fact that each phase-leg may have its own reference signal individually adjusted so that the leg currents can be kept balanced. A modulator is used for every leg and, therefore, as many modulators as parallel-connected legs will be required as shown in Fig.4.1. Each PWM module uses its own reference signal $v_{ref\,ax}$, x defining each leg ($x = 1, 2, \ldots n$), and its own carrier v_{carrx} to set the control variables s_{ax} and $\bar{s}_{ax}$ for both switches in the leg. When using the interleaving technique in a carrier-based modulation strategy, in spite of the fact that every single leg is switching at a frequency f_{sw}, an n-times higher apparent switching frequency is achieved by using an n number of shifted carriers ($f_s = nf_{sw} = n/T_{sw}$). Fig. 2.12(b) shows the general n-carrier case disposition although only the first three carriers have been depicted. The disposition of the carriers in a three leg case and one reference signal are shown in Fig. 4.2(a); The correspondig carrier has been highlighted and the generated PWM output is depicted in Fig. 4.2(b).

Putting together the fact that each modulator uses its particular carrier and its specific reference and that, when using the interleaving technique, the carriers are phase shifted, may lead to a set of carriers and references' disposition as the one depicted in Fig. 4.3. Even if the modulating signals were the same for each leg, a modulator using a different carrier for each one of them would still be required because of the interleaving of the carriers (Fig. 4.4). The number of PWM modules available in a standard DSP is limited and it is quite common for each PWM module to use just one carrier signal, limiting therefore the possibility of using interleaved carriers.



(a)



(b)

FIGURE 4.2: Standard interleaved PWM signals. (a) Reference signal and three carriers. (b) PWM output of the leg corresponding to the highlighted (red) carrier.

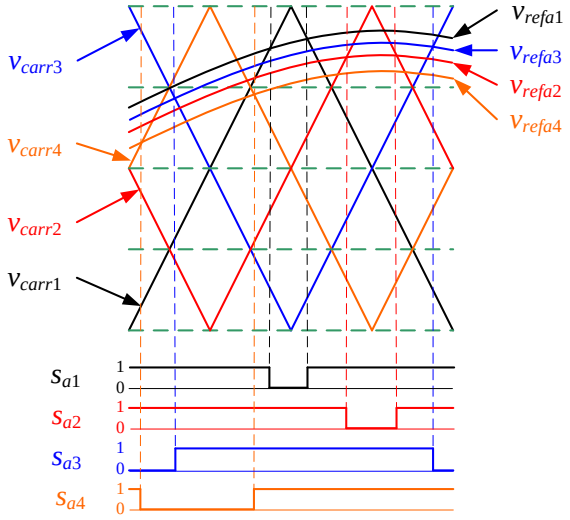


FIGURE 4.3: Carriers, references, and PWM outputs in a four parallel-leg case ($n = 4$).

4.3 The Proposed Modulation Technique

A method to achieve the same PWM signals yielded by n modulators with n shifted carriers but with just one carrier signal is presented in this section. The proposed technique uses n modulators as well, but the requirement of a set of n evenly phase-shifted carrier signals at an f_{sw} frequency is replaced by the need for only one carrier

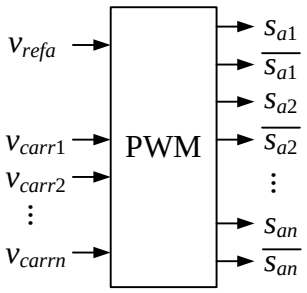


FIGURE 4.4: Modulator using only one reference (v_{refa}) but still n carriers ($x = 1, 2, ...n$).

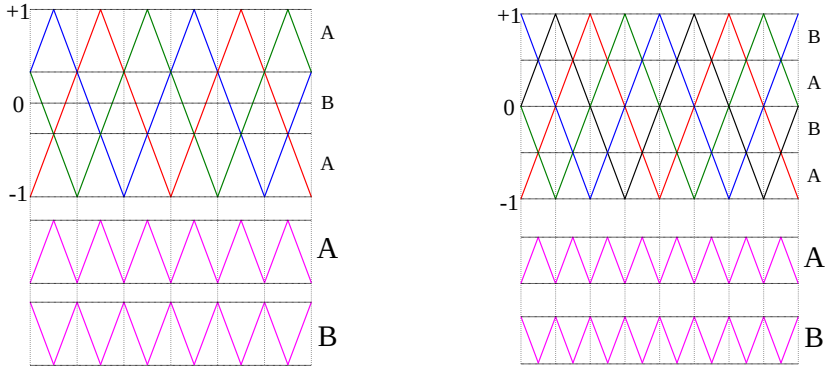
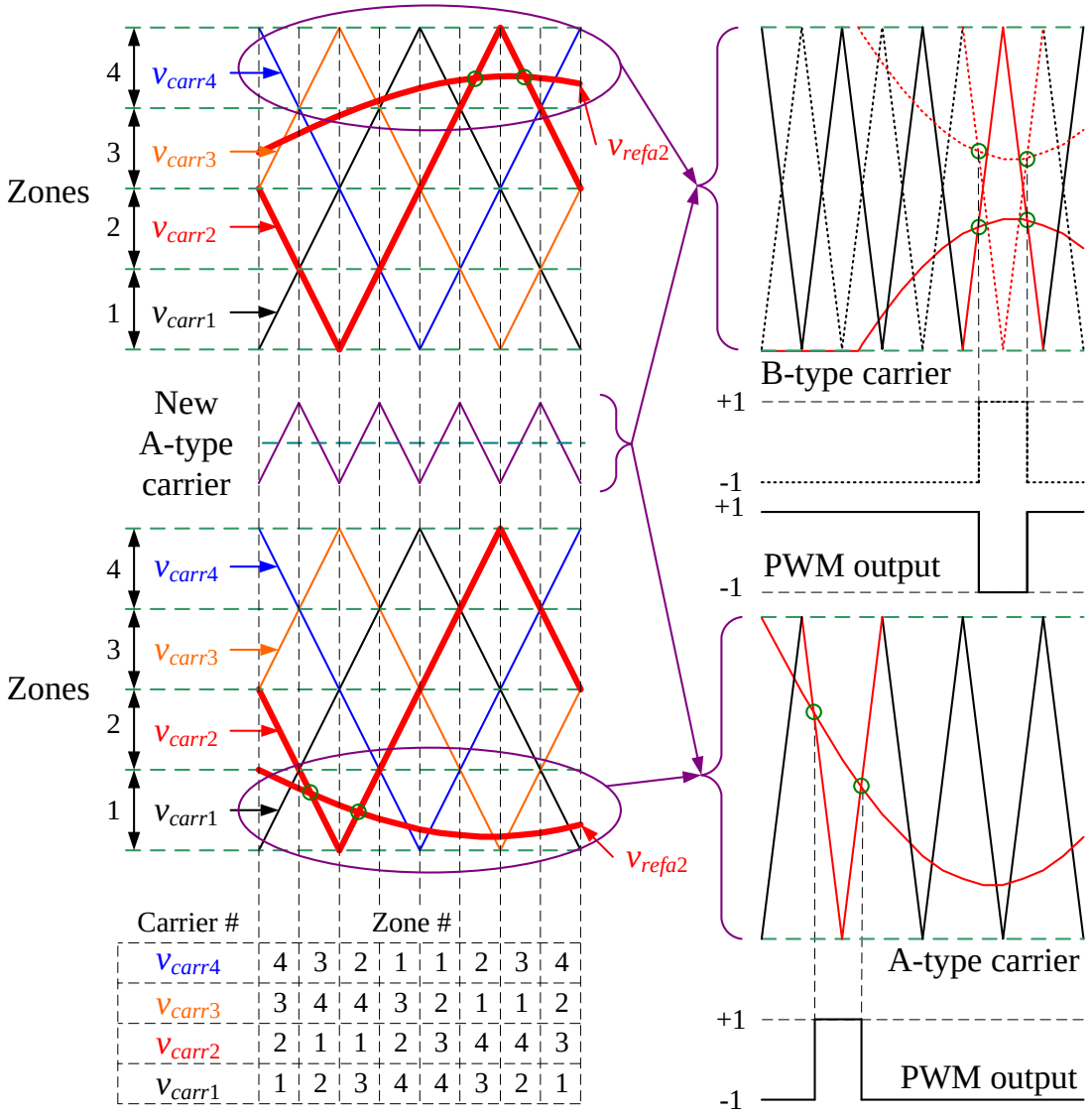


FIGURE 4.5: A-type and B-type "minicarriers". (a) Three carrier case. (b) Four carrier case.

signal at an n-times higher frequency (nf_s). The modulation technique is described in the following paragraphs.

In Fig. 4.5(a) a set of three interleaved carriers is depicted whereas in Fig. 4.5(b) the set shown is made up of four interleaved ones. The domain of the carriers, which ranges from -1 to +1, is divided into n zones. In each zone, a small piecewise carrier signal made up of fragments of the initial set of carriers can be defined. These small new carriers have an n-times higher frequency (nf_s) and an n-times smaller peak-to-peak value ($2/n$). Two types of carriers can be distinguished depending on their phase: A-type carriers and B-type ones. Let us define the A-type as the ones that are formed in the lowest zone, and the B-type as the ones in the next upper zone. Their phases are opposite and, all along the range, they are allocated every other zone (see Fig. 4.5).

In Fig. 4.6, a set of four interleaved carriers can be seen. Only one of the four reference signals has been drawn for the sake of clarity. The relative position between the reference signal and its carrier will set up the state of the switches in the corresponding leg. In other words, the crossings between the reference signal and the highlighted carrier have to be detected. The whole set of former carriers can be replaced by just a new single carrier and a code sequencer. This new carrier could be either an A-type or a B-type



Carrier #	Zone #							
v_{carr4}	4	3	2	1	1	2	3	4
v_{carr3}	3	4	4	3	2	1	1	2
v_{carr2}	2	1	1	2	3	4	4	3
v_{carr1}	1	2	3	4	4	3	2	1

FIGURE 4.6: Extracting information from a four phase-shifted interleaved carrier case for the proposed single-carrier implementation. Rescaling of the reference signal and PWM output with a B-type carrier (upper right) and with an A-type carrier (bottom right), and code sequence (bottom left).

carrier. In Fig. 4.6, an A-type carrier signal has been chosen. Although this small new carrier has an n-times smaller peak-to-peak value $(2/n)$, the actual carrier that is being used ranges from -1 to +1 as well. When replacing the set of carriers by this new single one, some scale readjustments need to be performed on the reference signal in order to make sure that the crossings happen at the very same instants as they would have happened with the initial set. A continuous assessment of the instantaneous location of the reference signal has to be performed in order to know what adjustments are needed. Provided that the carrier that is actually used can swing from -1 to +1, the reference signal will have to be level shifted and rescaled.

The shifting value $v_{offsetx}$ that has to be added depends on the zone where the

instantaneous reference value is located. $z_{ref\,ax}$ being the zone number, and n the former number of carriers, i.e. the number of paralleled legs, its value is defined in the following expression

$$v_{offset\,ax} = \frac{2}{n}\left(\frac{n+1}{2} - z_{ref\,ax}\right). \tag{4.1}$$

Adding this offset value to the reference signal makes sure that the new one is in the range [-1/n, +1/n]. Then, when rescaled by an n factor, this modified reference signal becomes again normalized to the [-1, +1] range. The following equation defines the arithmetical expression of this new reference signal $v'_{ref\,ax}$

$$v'_{ref\,ax} = (v_{ref\,ax} + v_{offset\,ax})\, n\, (-1)^{(z_{ref\,ax}+1)}. \tag{4.2}$$

In order to modulate this new shifted and rescaled signal, two carriers would be required depending on the zone where the former reference signal was set in: an A-type (in Zones 1 and 3) or a B-type carrier (in Zones 2 and 4). Provided that both carriers are phase-opposite, the same modulation results can be achieved using only one carrier —let us say an A-type carrier— and inverting both the reference signal and the modulation results in zones where a B-type carrier would be required (i.e. even zones) as depicted in Fig. 4.6. The same could also have been attained by using a B-type carrier and inverting when the reference signal is in an odd zone.

One of the original reference signals used in a three parallel-leg VSC is depicted in Fig. 4.7(a). Provided that three interleaved carriers are used, the domain of these carriers is broken down into three zones. Assuming that modulation is performed by means of an A-type carrier signal, the initial reference signal is only shifted and rescaled when in the top zone ($z_{ref\,ax} = 3$) or in the bottom zone ($z_{ref\,ax} = 1$), whereas when in the central zone ($z_{ref\,ax} = 2$) it is rescaled and inverted; the shifting value is null in that case. The new A-type carrier and the modified waveform of the reference are shown in Fig. 4.7(b). Just for the purpose of illustration, the frequency of the carrier has been chosen deliberately low. When comparing the initial reference signal to one of the carriers in the original scheme, two crossings per switching period (T_{sw}) happened. Now, as the modified reference signal is compared to an n-times higher frequency carrier, $2{\cdot}n$ crossings happen every T_{sw} period, but still only two of them are valid. In order to disregard all the invalid crossings some digital processing is performed. Valid crossings are the ones that happen when both, original carrier and reference signal are in the same zone. On the one hand, when the original reference signal is set in a zone higher than its carrier, no crossings must lead to actual switching and the PWM output has to be clamped up. On the other hand, if the original reference is set in a zone lower than its carrier, the PWM output must be clamped down and any crossings detected

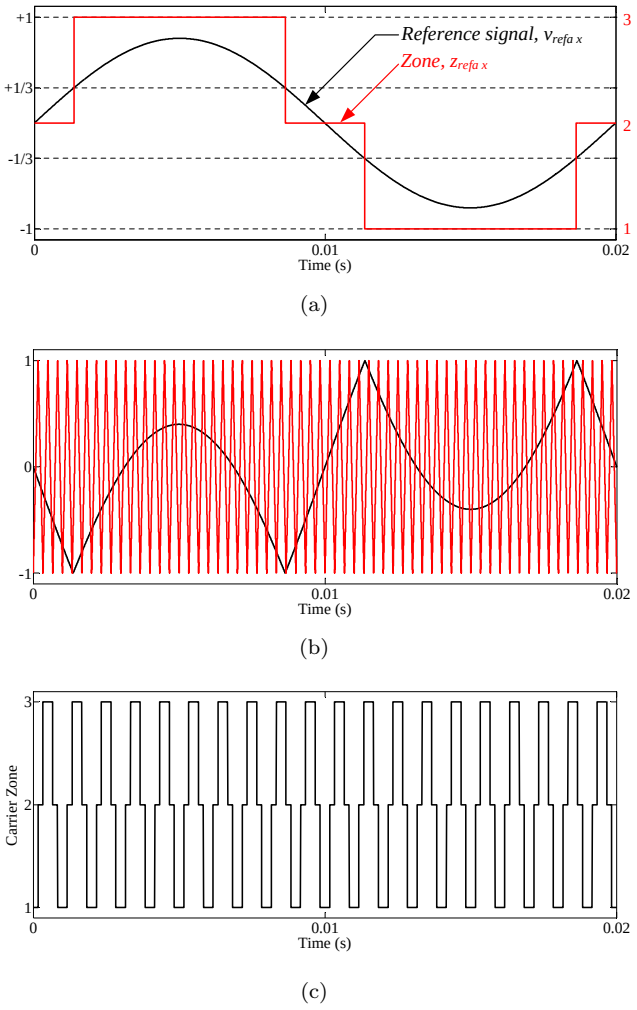


FIGURE 4.7: Carrier and reference related signals from the proposed interleaved single-carrier modulator. (a) Reference signal and zone code. (b) Shifted-and-rescaled reference signal and new carrier. (c) Carrier-zone sequence.

should be ruled out. Information about which zone the original carriers would be located in is provided by a code sequencer (Fig. 4.6), whereas the so called Zone-Pinpointing block provides data about where the reference signal is set in. Fig. 4.7(c) shows what the output of the carrier zone sequencer looks like, and Fig. 4.8(a) shows a clamping signal whose value is -1, 0 or +1, depending on the relative position between the original reference signal and the original carrier. Fig. 4.8(b) depicts the results of comparing the modified reference signal to the new carrier. It should be noted that a huge number of false crossings are detected. Finally, Fig. 4.8(c) shows the actual PWM output once the former has been digitally processed by means of the clamping mask shown in Fig. 4.8(a). As it can be seen, the PWM output in Fig. 4.8(c) matches perfectly the one depicted in Fig. 4.2(b), when the original set of three phase-shifted carriers was used.

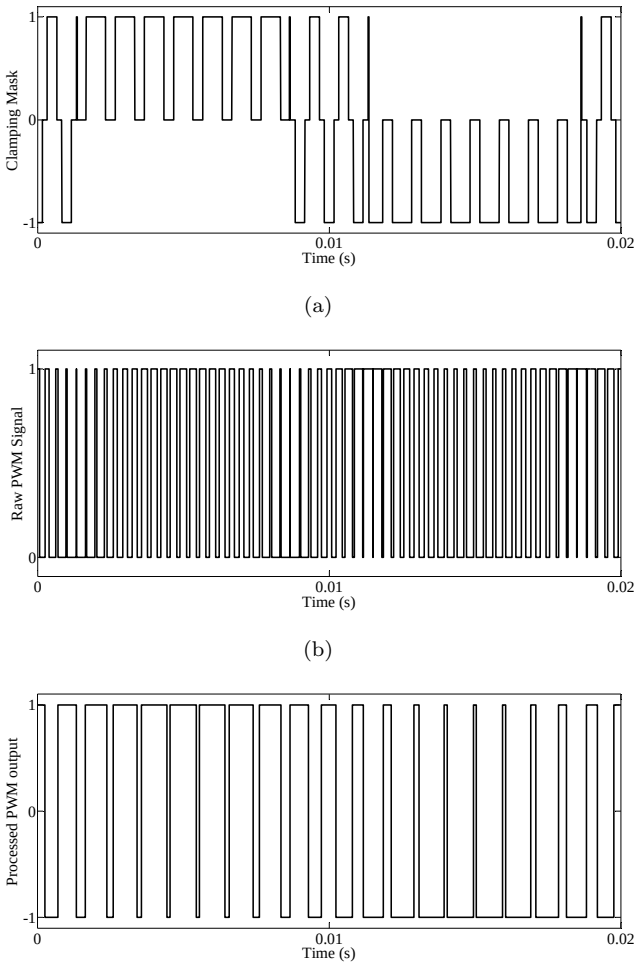


FIGURE 4.8: (a) Clamping mask. (b) Raw PWM signal. (c) Processed PWM output signal.

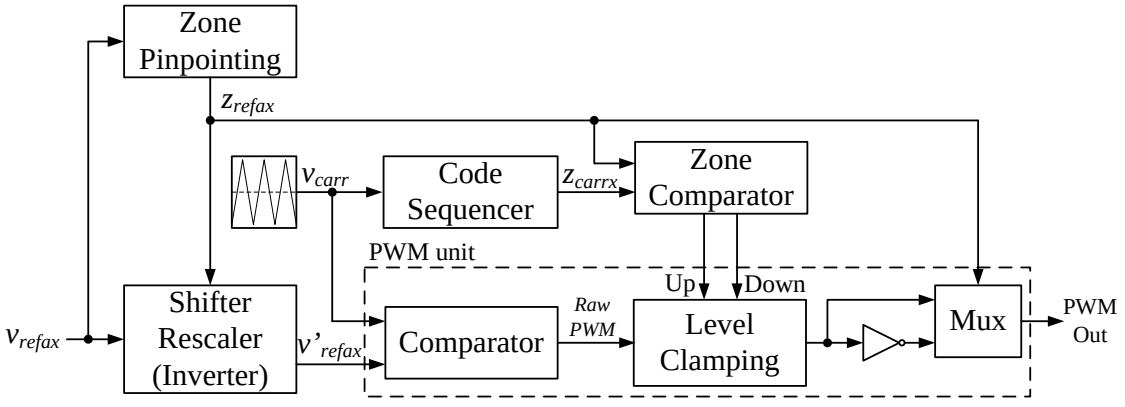


FIGURE 4.9: Proposed one leg single-carrier modulator.

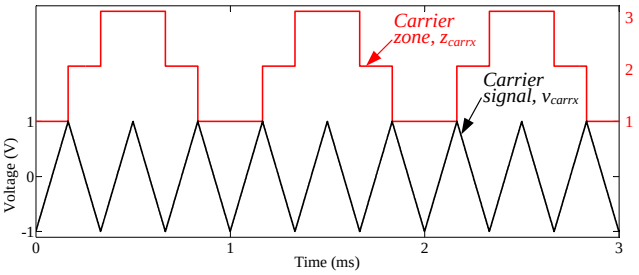


FIGURE 4.10: New carrier and carrier code sequence.

4.4 Implementing the Modulator

The overall working of the proposed strategy is illustrated in Fig. 4.9 and can be described as follows. A new normalized carrier v_{carr}, whose frequency is n times higher than the original one, is used. The carrier domain is broken down into n equally sized zones of $2/n$ peak-to-peak value that are numbered upwards. The task of identifying which zone the reference signal $v_{ref\,ax}$ is in is continuously carried out by the Zone-Pinpointing block that generates the $z_{ref\,ax}$ signal. With these data and the instantaneous value of the reference signal, a new level-shifted, rescaled and occasionally inverted reference signal $v'_{ref\,ax}$ is generated. Assuming that the modulation is performed by means of an A-type carrier, the new reference $v'_{ref\,ax}$ is inverted when the input reference is set in an even zone, i.e. the ones that would need a B-type carrier to perform the equivalent modulation. However, the new reference $v'_{ref\,ax}$ is not inverted when the input $v_{ref\,ax}$ is set in an odd zone, i.e.: the ones that use an A-type carrier. Depending on whether the modified reference $v'_{ref\,ax}$ has been inverted or not, the result of the modulation has to be inverted, accordingly. That is the reason why there is a link between the Zone-Pinpointing block and the output multiplexer that is responsible for performing such inversion. Because of the rescaling, the new reference $v'_{ref\,ax}$ is allowed to swing in a [-1, +1] range (linear modulation) so that it can be compared to the normalized triangular carrier signal. This comparison is performed by the PWM block that detects all the crossings between carrier v_{carr} and reference signal $v'_{ref\,ax}$.

However, some of these crossings have to be disregarded. This disregarding task is implemented by means of the Level Clamping block. In order to know which zone the original carrier that is being replaced would be set in, a code number $z_{carr\,ax}$ is continuously provided by the Code Sequencer block. This block is synchronized with the new carrier, as shown in Fig. 4.9 and Fig. 4.10. Depending on the result of the comparison between the zone code of the reference signal $z_{ref\,ax}$ and the original carrier $z_{carr\,ax}$, the output of the PWM block is clamped either up (+1), down (-1), or passed without any change (0) to the modulator output.

Table 4.1: TMS320F2812 PWM resources

Event Manager	16 bit Timer	Number of Compare Units	PWM Outputs
EMA	1	3	6
EMA	1 or 2	2	2
EMB	3	3	6
EMB	3 or 4	2	2

In order to assess the features of the proposed PWM implementation, let us consider Texas Instruments' TMS320F2812 [91], one of the most widely used DSPs in the power control field; its PWM generating resources are shown in Table 4.1. There are two event managers (EM) which include three full-compare units each [92]. These compare units use one of the timers (Timer 1 or Timer 3, for EMA or EMB, respectively) as the time base to generate six PWM outputs that include programmable dead-band circuits. The state of each of the six outputs can be configured independently. Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) by the three full-compare units and two independent PWMs by the remaining compare units.

If a standard interleaved PWM strategy were to be implemented using this DSP, the maximum number of legs that could be connected in parallel would be four. In other words, the number of carriers would be limited by the number of available timers. With the implementation presented in this paper, the limitation in the number of legs would not come from the number of timers but from the number of compare units. Each EM provides three pairs of PWM outputs (derived from Timer 1 or Timer 3) plus two extra PWM outputs (derived from Timers 1 and 2 or Timers 3 and 4, respectively) that can be used to form an extra pair. Provided that all four timers can be arranged to work synchronously thus behaving as a single timer –i.e. a single carrier– all in all, eight pairs can be generated thus allowing the control of up to eight legs in parallel. Alternatively, if the two extra PWM outputs in each EM were not used to form a pair but used as independent outputs, up to ten legs in parallel could be controlled if some external hardware to create the complementary outputs and their dead-time were added.

When implementing a carrier signal in a DSP, one can achieve a specific frequency by tuning either the modulus of the timer or the timer clock frequency. The modulus of the timer will determine the resolution. If the new carrier has an n-times higher frequency, in order not to worsen the resolution, the timer clock frequency should be n-times higher too. If that were not possible, a compromise between frequency and modulus would be required. Considering Texas Instruments' TMS320F2812 as a representative example, using only 12 bits of their timers (maximum modulus of 4096) and a maximum timer

TABLE 4.2: Specifications of the Laboratory Prototype

Symbol	Parameter	Value
V_{dc}	dc-bus voltage	48 V
f	Reference signal frequency	50 Hz
m_a	Modulation index	0.7
n	Number of legs	3
f_{sw}	Carrier/switching frequency	2 kHz
f_s	New carrier frequency	6 kHz
R_L	Load resistance	10 Ω
L	Inductor	6 mH

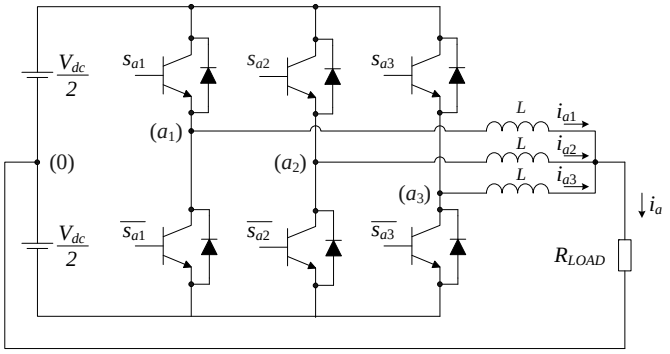


FIGURE 4.11: Circuit of the experimental prototype (n=3).

clock frequency of 150 MHz, each slope of the carrier ($T_s/2$) can last up to 27.3 μs that corresponds to a frequency of 18.31 kHz, which will be the apparent switching frequency seen from the output of the interleaved converter. This would be enough to handle 8 legs in parallel, each of them switching at a frequency slightly above 2 kHz. If a higher frequency were required, the modulus of the timer could be changed. This would decrease the resolution of the carriers.

4.5 Experimental Results

In order to check the validity of the proposed modulator, an experimental Matlab-Simulink-based modulator has been implemented on a dSPACE DS1103 PPC Controller board. It has been used to drive the single phase VSC made up of three legs in parallel with a resistive load depicted in Fig. 4.11 and whose values are listed in Table 4.2. A picture of the experimental plant is shown in Fig. 4.12.

The inductors used in this experiment were not designed for optimum results of the specific converter application but were rather selected because of their availability in the lab. Therefore, they are rated for currents much higher than the values used in the tests. If one wishes to design the inductors, the value of L should be calculated in such a way so

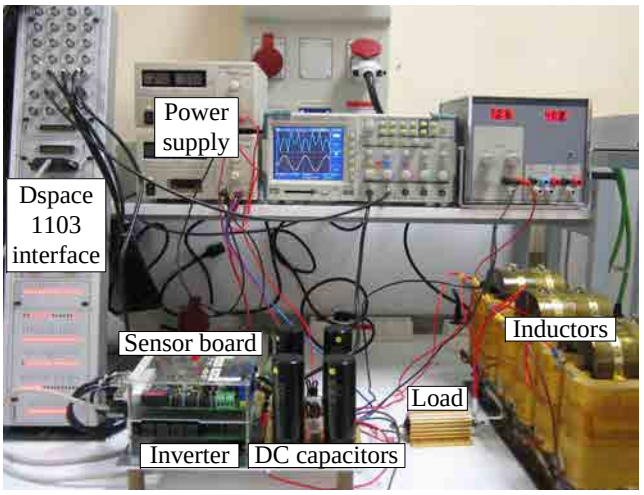


FIGURE 4.12: Laboratory prototype with 3 legs in parallel.

as to ensure that the current ripple in each inductor does not exceed a maximum value related to the rms rated output current of the converter (I_M). The maximum current ripple is produced when operating at a duty cycle of 50%. Therefore, an estimation of the peak-to-peak current ripple (I_{p-p}) is:

$$I_{p-p} = \frac{T_{sw} V_{dc}}{4L}, \tag{4.3}$$

T_{sw} being the switching period and V_{dc} the value of the dc-bus voltage.

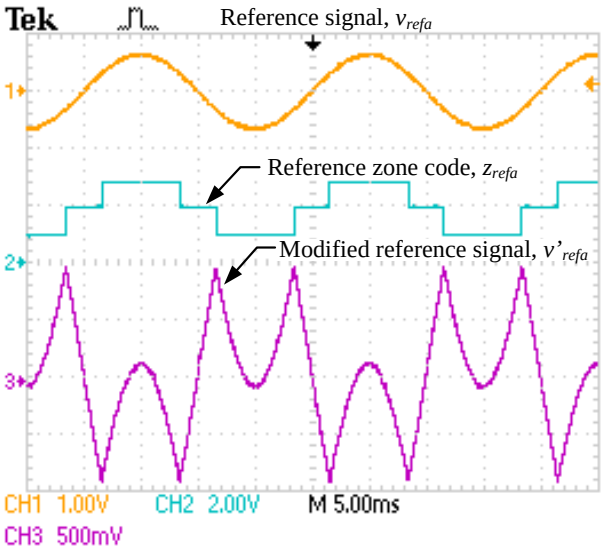
Imposing the peak-to-peak current ripple in each of the n legs not to be higher than a specific percentage of the amplitude of the rated current, for instance 50%::

$$I_{p-p} \leq 0.5\sqrt{2}\frac{I_M}{n}, \tag{4.4}$$

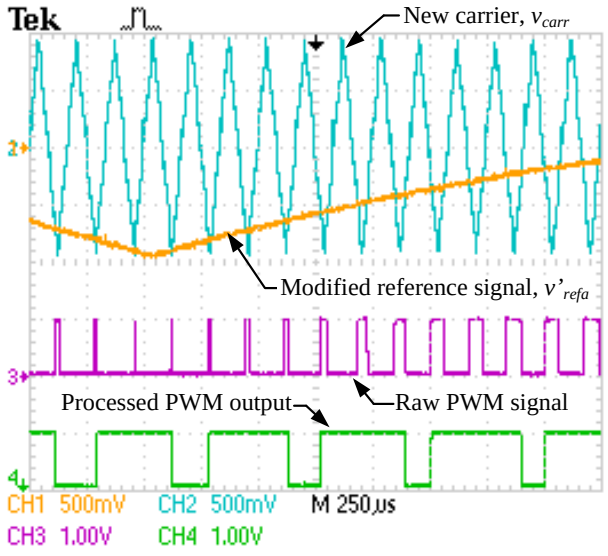
the value of the inductor should be:

$$L \geq \frac{T_{sw} V_{dc} n}{2\sqrt{2} I_M}. \tag{4.5}$$

A normalized reference signal for one leg can be seen in Fig. 4.13(a). The code zone supplied by the Zone-Pinpointing block and the resulting modified reference signal are also displayed in Fig. 4.13(a). The inversion of the modified reference signal when in Zone 2 can be seen. In Fig. 4.13(b), a partial view of the modified reference signal and the carrier is displayed. The reference signal is moving from Zone 2 to Zone 3. The raw, unprocessed modulated signal is displayed too. The resulting PWM signal is shown in the lower part of Fig. 4.13(b). The undesired crossings have been disregarded and the



(a)

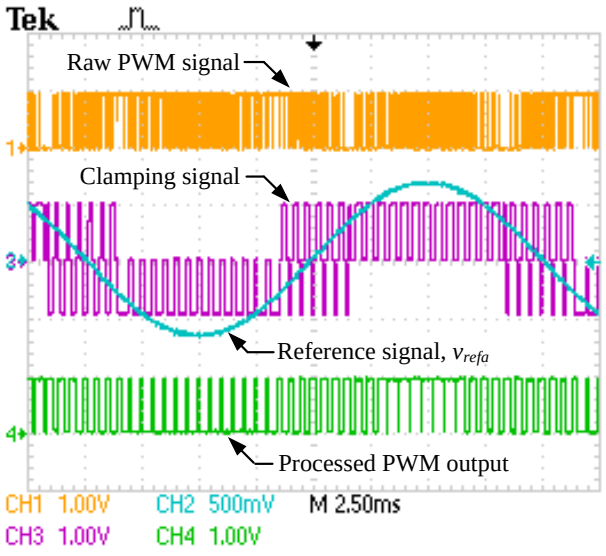


(b)

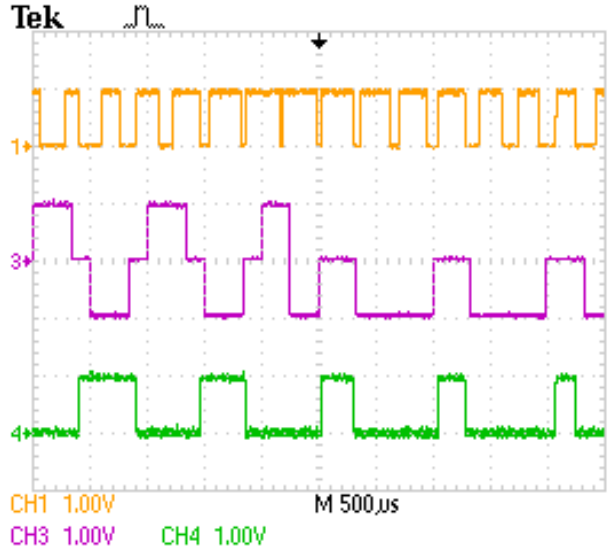
FIGURE 4.13: Experimental results: main modulator signals. (a) Modified reference signal. (b) Raw and processed PWM signals.

output signal has been inverted where, as in Zone 2, a B-type carrier would have been required.

The effect of the digital processing task carried out by the Clamping Block can be clearly observed in Fig. 4.14(a). The reference signal and the consequent clamping signal are displayed in the center of Fig. 4.14(a). When the reference signal is set in Zone 1, the only clamping action required, if any, is downwards. Similarly, clamping upwards is the only option when the reference is in Zone 3. While when in Zone 2, depending on the relative position between carrier and reference, the clamping action could be either upwards, downwards or none. The upper signal displayed in Fig. 4.14(a) corresponds to



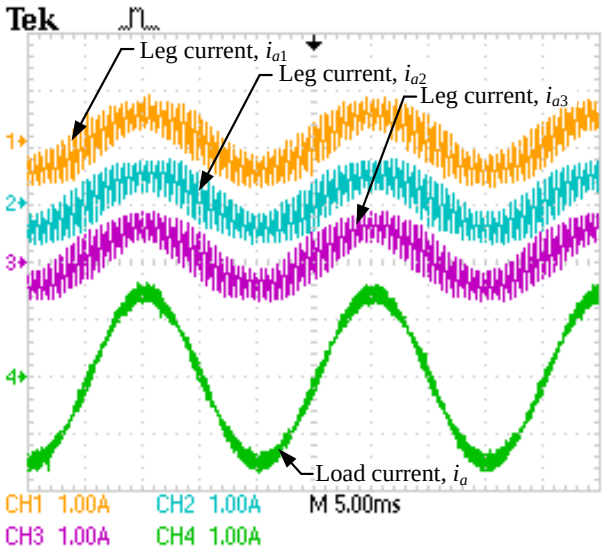
(a)



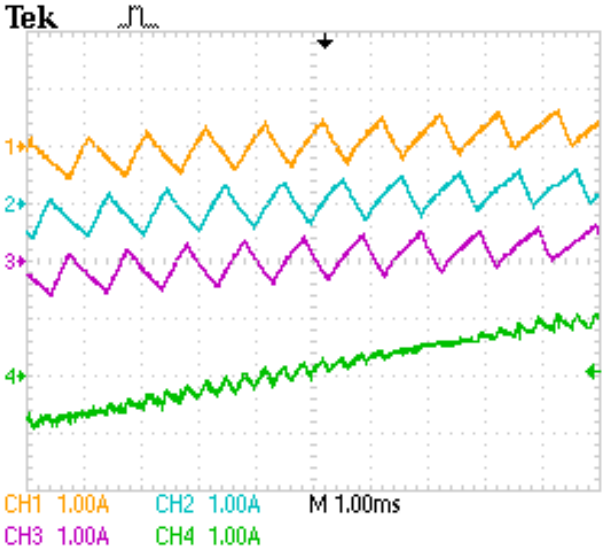
(b)

FIGURE 4.14: Experimental results: main modulator signals. (a) PWM signals: raw, clamping signal, and output. (b) Zoom of the PWM signals.

the direct output of the PWM block (raw PWM), whereas the one displayed in the lower part corresponds to the final PWM output of the modulator (processed PWM output). Fig. 4.14(b) shows an expanded version of Fig. 4.14(a) where the reference signal has been removed for purposes of clarity. The zooming corresponds to the moment when the reference signal crosses from Zone 2 to Zone 1. The clamping signal is swinging up and down in the left part of Fig. 4.14(b) –that corresponds to Zone 2– whereas it can only be clamped down when in the right part —that corresponds to Zone 1—. When comparing the raw PWM signal to the digitally processed PWM output, the inversion of the latter when the reference is in Zone 2 can also be noticed.



(a)



(b)

FIGURE 4.15: (a) Interleaved leg currents and load current. (b) Zoom of leg and load currents.

Fig. 4.15(a) and Fig. 4.15(b) illustrate the waveforms of the currents in each of the parallel legs and the overall load current. The noticeable reduction in the load current ripple that can be observed is due to the interleaving effect when modulating the reference signal in each leg.

The results of a step change in the modulation index (m_a), i.e. the amplitude of the reference signal v_{refax}, from 0.3 to 0.6 have been captured in Fig. 4.16. On the left part of Fig. 4.16, while $m_a = 0.3$, the reference signal is confined to the central zone (Zone 2) and rescaling but no inverting is required to generate the new reference. By contrast, on the right part of the figure, when the modulation index changes to 0.6, the reference

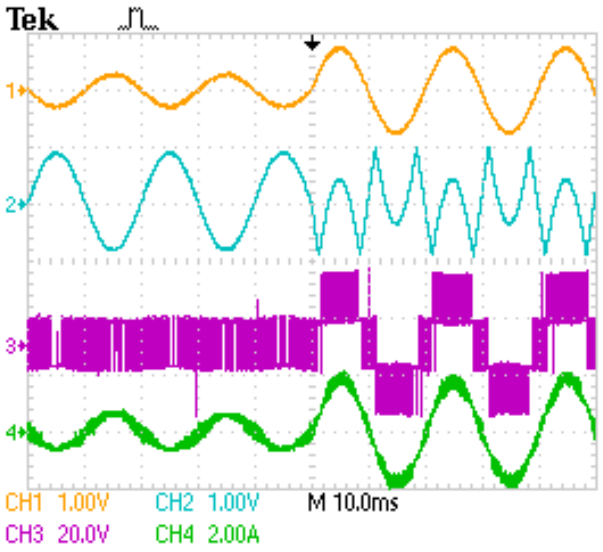


FIGURE 4.16: Reference signal v_{refa} (channel 1), modified reference signal v'_{refa} (channel 2), equivalent output voltage v_{aeq} (channel 3), and load current i_a (channel 4).

signal swings across the three zones and the effect of shifting and rescaling on the new reference is clearly noticeable.

Since there are three legs connected in parallel, v_{ax} being the output voltage of the x leg (Fig. 4.11), the equivalent (Thevenin) output voltage of the phase becomes

$$v_{aeq} = \frac{1}{3}\sum_{x=1}^{3} v_{ax}, \tag{4.6}$$

owing to the averaging effect of the parallel connection. The waveform of this v_{aeq} is also displayed in channel 3 of Fig. 4.16 and, because of the fact that there are three legs connected in parallel, four voltage levels can be seen $(n+1)$. The seamless change in the output current is also displayed in channel 4 of Fig. 4.16.

4.6 Conclusion

This chapter presented a new implementation of interleaved PWM for VSC with legs connected in parallel which is able to produce interleaving using just a single carrier. Therefore, there is no need to generate n phase-shifted carriers as it is usually required to achieve such an effect. The modulation signals are properly shifted and rescaled to achieve the same effects as in the case of an n-carrier modulation. The proposed technique is presented in a general way so that it could be applied to a converter with any number of parallel legs per phase (i.e. n legs). It is, therefore, appropriate for modular parallel converters. The modulation algorithm can be implemented in a DSP

or field programmable gate array (FPGA). Since a single carrier signal is used, the problems associated with carrier synchronization to achieve proper phase shifting are avoided. Furthermore, when the proposed algorithm is implemented in a DSP, a higher number of legs connected in parallel can be controlled using the PWM units available within the DSP. For instance, using the Texas Instruments TMS320F2812, up to four legs in parallel can be controlled with the standard phase-shifted PWM implementation. In contrast, using the proposed algorithm, the maximum number of legs that can be controlled is eight. Moreover, this limit can be increased to ten just by adding some basic additional hardware, consisting of digital inverters and dead-time generators, to process four PWM output signals.

Chapter 5

Disposition of the Carriers

This chapter deals with the influence of the disposition of the carriers in a PS-PWM scheme on the quality of the output voltages. A new PS-PWM implementation for interleaved multi-phase VSIs where switching in the line-to-line voltages happens exclusively between adjacent levels is presented. The proposed method improves improves the quality of the line-to-line output voltages when compared to the conventional PS-PWM implementation.

5.1 Introduction

Different methods to set the instantaneous output voltage level in VSIs with legs connected in parallel can be used, including SV-PWM or CB-PWM. The effect on their harmonic spectra has been largely investigated [45, 63, 65, 67]. In CB-PWM, the use of as many carriers as legs are connected in parallel is the standard procedure if interleaving is to be implemented. In an interleaved PS-PWM scheme, all the carriers have the same frequency and amplitude (usually ranging from -1 to +1 per unit) and are evenly phase-shifted within a switching period. Each carrier is associated with a specific leg. In LS-PWM schemes, n triangular carriers with the same frequency and $2/n$ peak-to-peak value are arranged in contiguous zones to fully occupy the range from -1 to +1. Depending on the relative phase relationship among the carriers, different PWM strategies are commonly referenced. The most popular one is PD-PWM [45].

In multilevel inverters, a PD-PWM scheme provides line-to-line voltages where switching happens only between adjacent levels. However, LS-PWM techniques, such as PD-PWM, cannot be applied without modification in converters with legs connected in parallel. If each carrier were associated with one leg, only the leg associated with the carrier

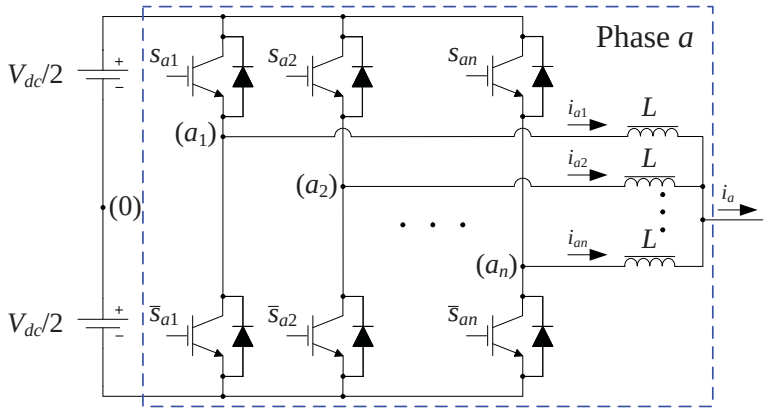


FIGURE 5.1: One phase of a VSI incorporating n legs connected in parallel.

in the zone where the reference signal was, would be switching. The remaining $n-1$ legs would be clamped to either the positive or the negative dc-link voltage, depending on the relative position of their reference signal. This process would create dc-voltage components across the inductors and produce extremely large circulating currents.

For a VSI with n legs in parallel, the proposed modulator utilizes two sets of n evenly phase-shifted carriers that are dynamically allocated. Because of its generality, the proposed implementation can be applied to VSIs with any number of phases and any number of legs connected in parallel.

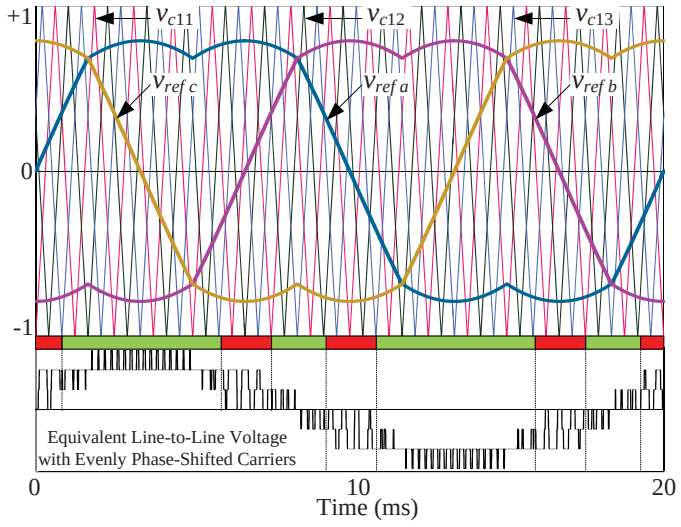
5.2 Interleaved PS-PWM

The interleaving technique is applied to VSIs with legs in parallel to achieve an apparent switching frequency n times higher than the individual switching frequency of each leg [25]. When operating with a CB-PWM this is achieved by using n evenly phase-shifted carriers. Since there are n legs connected in parallel per phase, the Thevenin-equivalent output voltage of the y-phase becomes

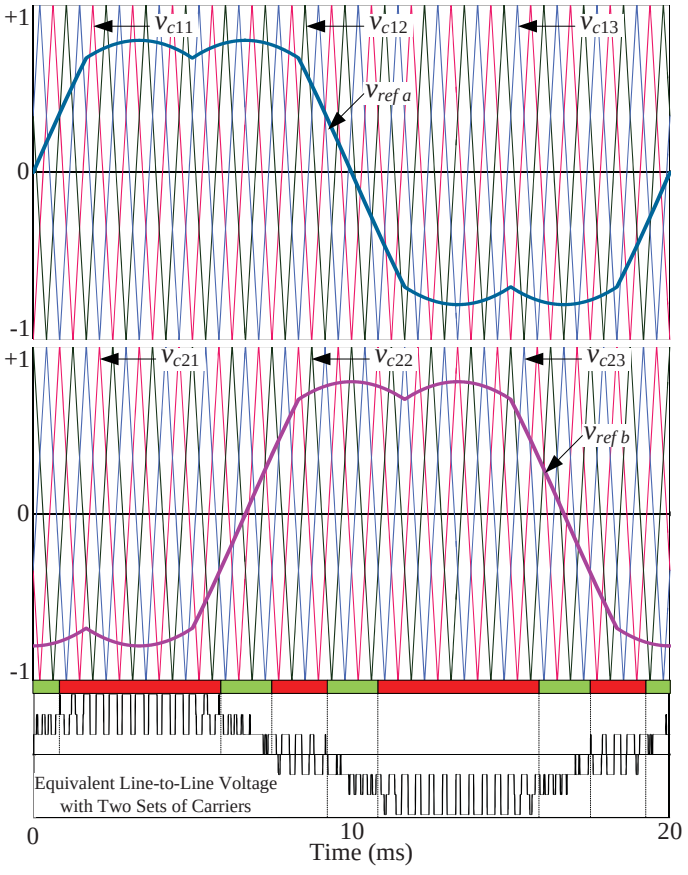
$$v_y = \frac{1}{n}\sum_{x=1}^{n} v_{yx}, \tag{5.1}$$

due to the averaging effect of the parallel connection. The equivalent line-to-line voltage is the difference between the equivalent output voltage of two phases.

Fig. 5.2(a) illustrates the case of a three-phase VSI with three legs in parallel per phase. The phase angles for the three carriers used (v_{c11}, v_{c12}, and v_{c13}) are 0°, 120°, and 240°, respectively. The reference signals (v_{refa}, v_{refb}, and v_{refc}) are compared to their respective carrier signal to set the on-off state of the switches. In order to further



(a)



(b)

FIGURE 5.2: Voltage references, set of carriers, and Thevenin-equivalent line-to-line output voltage (v_{ab}) for a three-phase VSI with three legs connected in parallel for m_a= 0.8 and f_c= 800Hz. (a) One set of carriers. (b) Two sets of carriers.

extend the range of the linear modulation index (m_a) up to 1.15, the offset voltage

$$v_{offset} = -\frac{max(v_{refa}, v_{refb}, v_{refc}) + min(v_{refa}, v_{refb}, v_{refc})}{2} \tag{5.2}$$

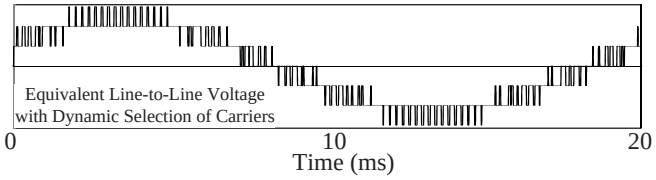


FIGURE 5.3: Line-to-line voltage waveform for a three-phase VSI with three legs in parallel per phase achieved when using a dynamic assignment of carriers.

is added as a zero sequence component to the three-phase references. The same equivalent output voltages as if centered SV-PWM was used are obtained [8].

Although the use of a set of evenly shifted carriers yields the best attainable single-phase output voltage in terms of THD, that is not the case for line-to-line output voltages [63]. From the equivalent line-to-line voltage in Fig. 5.2(a), it can be observed that during certain intervals there is switching among three adjacent levels, thus worsening the overall THD and with negative implications in terms of electromagnetic interference on account of bigger voltage steps. The use of a different, but also evenly phase-shifted, set of carriers does not fix that. But if two different sets of carriers are used to modulate two different phases, the periods of time where three-level switching in the line-to-line voltages is observed, vary. Fig. 5.2(b) depicts the results obtained for the aforementioned VSI if v_{refa} is modulated by means of the first set of carriers, i.e. v_{c11}, v_{c12}, and v_{c13}, and v_{refb} is modulated by means of a second set of carriers, i.e. v_{c21}, v_{c22}, and v_{c23}, whose respective angle phases are 60°, 180°, and 300°.

Upon scrutinizing the examples shown in Fig. 5.2, one can conclude that those intervals of two-level and three-level switching, when using one or another set of carriers, are fully complementary. As a consequence, line-to-line output voltages with switching only happening between adjacent levels are achievable with a dynamic selection of the appropriate set of carriers, as can be seen in Fig. 5.3. The proposed implementation is described in Section 5.3.

5.3 Enhanced Modulator

The new modulator requires the use of two sets of carriers. For the general case of n legs connected in parallel per phase, carrier Set 1 is made up of n phase-shifted carriers (v_{c11}, v_{c12}, ..., and v_{c1n}) with a relative phase shift of $360°/n$. A second set of carriers (v_{c21}, v_{c22}, ..., and v_{c2n}) —Set 2— is also evenly phase shifted, but the whole set is phase-shifted by $360°/(2n)$ with regards to Set 1. Table 5.1 shows the relative phase-shifting among the carriers. The phase shift depends on the number of carriers, i.e. the number of legs in parallel.

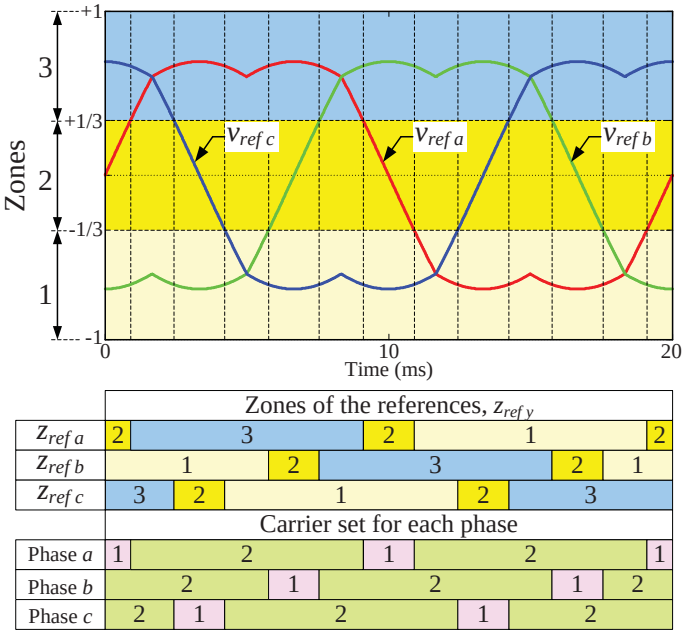


FIGURE 5.4: Single-phase voltage reference zones and carrier set allocation for a three-phase three-paralleled-leg VSI.

The carrier set selection is dynamically assessed depending on the instantaneous value of the modulating reference signals ($v_{ref\,a}$, $v_{ref\,b}$, ..., and $v_{ref\,m}$). For that purpose, and considering linear modulation, the carrier/reference signal domain (which ranges from -1 to +1) is broken down into n equally sized zones of $2/n$ peak-to-peak value that are numbered upwards as it is shown in Fig. 5.4. In order to quantize them, the following expression is used:

$$z_{ref\,y} = 1 + \left\lfloor \frac{1 + v_{ref\,y}}{\frac{2}{n}} \right\rfloor \quad \text{for} \quad y = \{a, b, ..., m\}, \tag{5.3}$$

where $z_{ref\,y}$ variables can take values from 1 to n.

Fig. 5.5 shows a block diagram of the proposed modulator for m phases and n legs per phase. The modulators for each phase use either Set 1 or Set 2 depending on the position of their reference signals. The Even/Odd Zone Detectors pinpoint the zones where the reference signals are, and generate the $z_{ref\,a}$, $z_{ref\,b}$, ..., and $z_{ref\,m}$ signals. The Even/Odd Zone Detectors also assess the parity of the $z_{ref\,y}$ signals and generate the sel_y selection signals according to:

$$sel_y = mod[z_{ref\,y}, 2] \quad \text{for} \quad y = \{a, b, ..., m\}. \tag{5.4}$$

Depending whether a phase reference signal lies within an even or an odd zone, its modulation is carried out by means of one or another set of carriers, respectively. For the example considered in Fig. 5.4, Set 1 is assigned to even zones and Set 2 to odd zones.

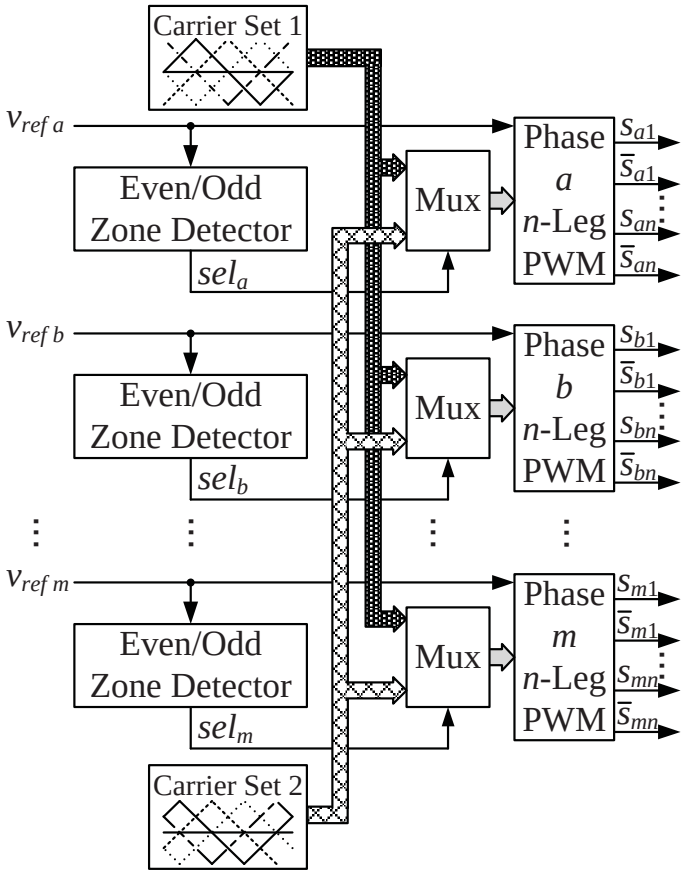


FIGURE 5.5: Generalized m-phase n-leg modulator diagram.

TABLE 5.1: Phase Shift of the Two Sets of Carriers

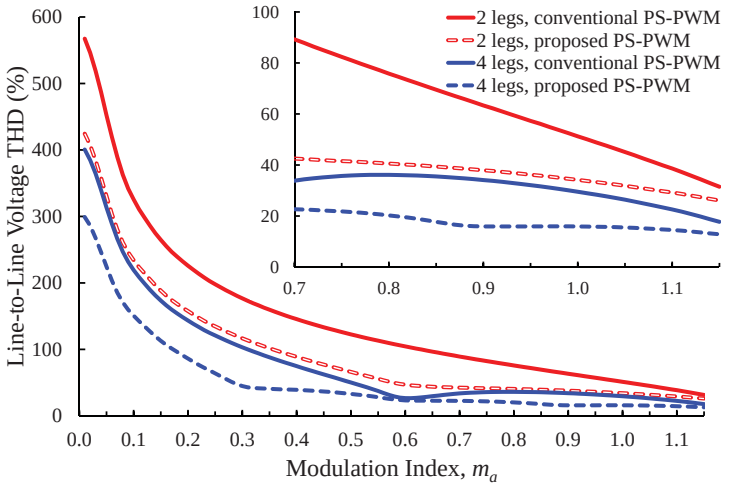
Number of carriers	Carriers' Phase Shift (°)	
	Set 1	Set 2
2	0, 180	90, 270
3	0, 120, 240	60, 180, 300
4	0, 90, 180, 270	45, 135, 225, 315
n	$360\left(0, \frac{1}{n}, \ldots, \frac{n-1}{n}\right)$	$360\left(\frac{1}{2n}, \frac{3}{2n}, \ldots, \frac{2n-1}{2n}\right)$

Those sel_y signals control the multiplexers that route one or another set of carriers to the PWM blocks that, ultimately, set the on-off state of the VSI switches.

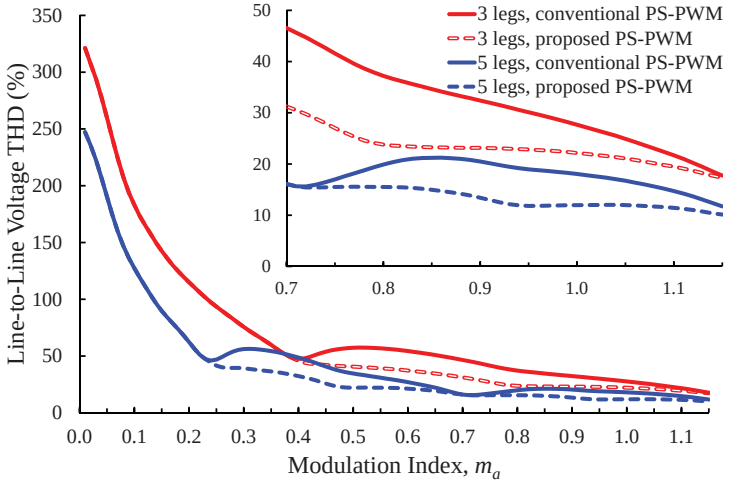
5.4 Simulation and Experimental Results

5.4.1 Simulation Results

The proposed modulator has been simulated on three- and four-phase Matlab-Simulink models with up to five legs in parallel per phase. Fig. 5.3 depicts the line-to-line voltage waveform for a three-phase three-leg VSI. THD and WTHD values for a three-phase



(a)



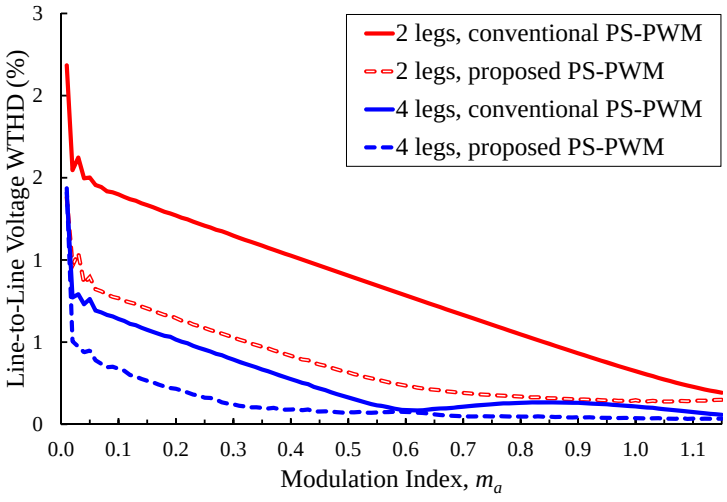
(b)

FIGURE 5.6: Line-to-line THD vs. modulation index. (a) 2 and 4 legs in parallel. (b) 3 and 5 legs in parallel.

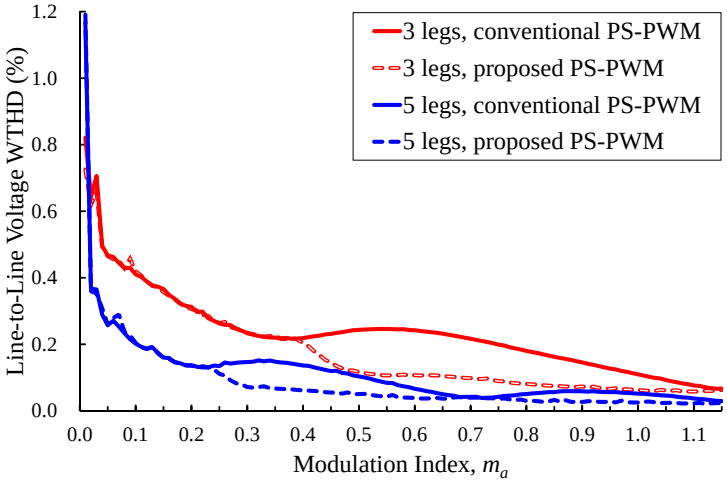
inverter, with a switching frequency of 3 kHz, and considering the first 2000 harmonics have been computed and plotted in Figs. 5.6 and 5.7, respectively. It can be seen that for an odd number of legs, i.e. an odd number of zones, the improvement in the THD is only achieved if the reference signal exceeds the central zone, e.g. $m_a > 1/n$.

5.4.2 Experimental Results

A three-phase modulator has been implemented on a dSPACE DS1103 PPC Controller board and tested on a laboratory prototype. There are two three-phase VSIs in the lab, which leaves up to six legs available for different connections. Two different configurations have been studied: (i) a full three-phase VSI with two legs in parallel per phase, and (ii) the implementation of phases a and b of a VSI with three legs per phase.



(a)



(b)

FIGURE 5.7: Line-to-line WTHD vs. modulation index. (a) 2 and 4 legs in parallel. (b) 3 and 5 legs in parallel.

Nevertheless, those two phases are modulated as if a full three-phase system had been implemented. The parameters that are common for both configurations are: dc-bus voltage V_{dc}= 48V, carrier frequency f_c= 2kHz, inductors L= 6mH, and Wye-connected load resistors R= 10Ω. In order to be able to visualize the Thevenin output voltage, two (or three, depending on the configuration) 10-kΩ Wye-connected resistors have been connected to the mid point of each leg.

Fig. 5.8 corresponds to the case of two-legs per phase with m_a= 0.8. It shows the phase voltage (v_{a0}), the line-to-line voltage (v_{ab}), the phase current (i_a), and the leg currents (i_{a1} and i_{a2}) for that phase. At the beginning of the figure the modulation is carried out with only one set of carriers, i.e. using conventional PS-PWM. From t= 50 ms on, the proposed PS-PWM method is used. Although the waveform of the phase voltage is not visually affected, the improvement in the line-to-line voltage is significant.

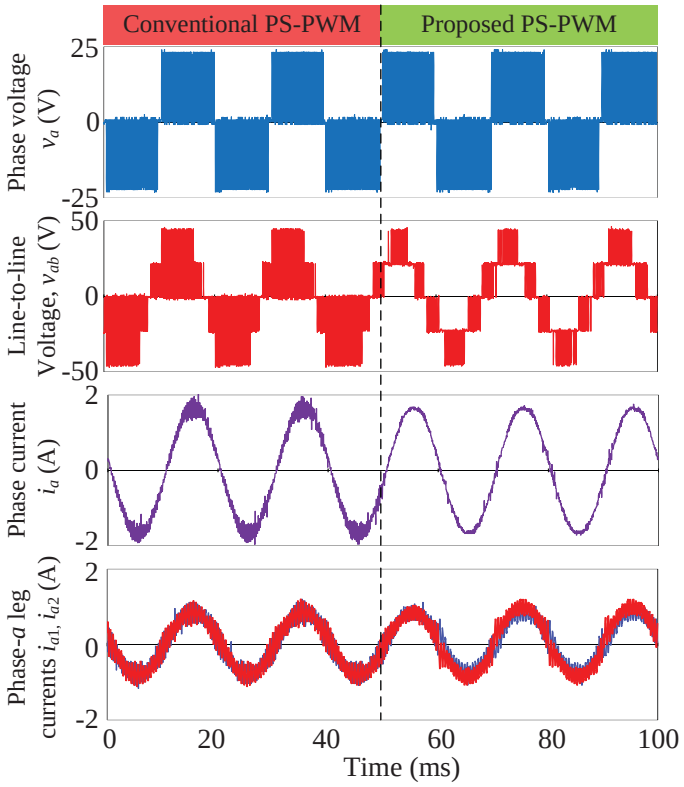


FIGURE 5.8: Experimental results with two legs connected in parallel. Transient from conventional PS-PWM to proposed PS-PWM with a modulation index m_a= 0.8. From top to bottom: phase voltage, line-to-line voltage, phase current, and leg currents.

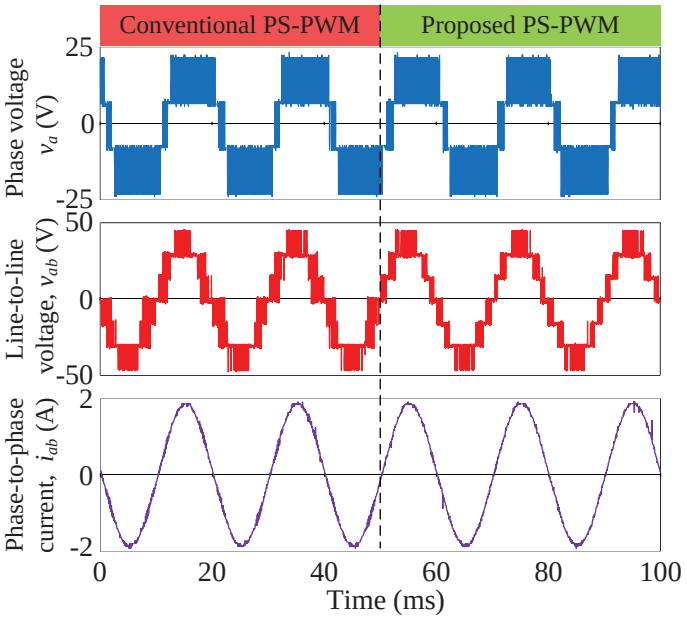


FIGURE 5.9: Experimental results with three legs connected in parallel. Transient from conventional PS-PWM to proposed PS-PWM with a modulation index m_a= 1.0. From top to bottom: phase voltage, line-to-line voltage, and phase-to-phase current.

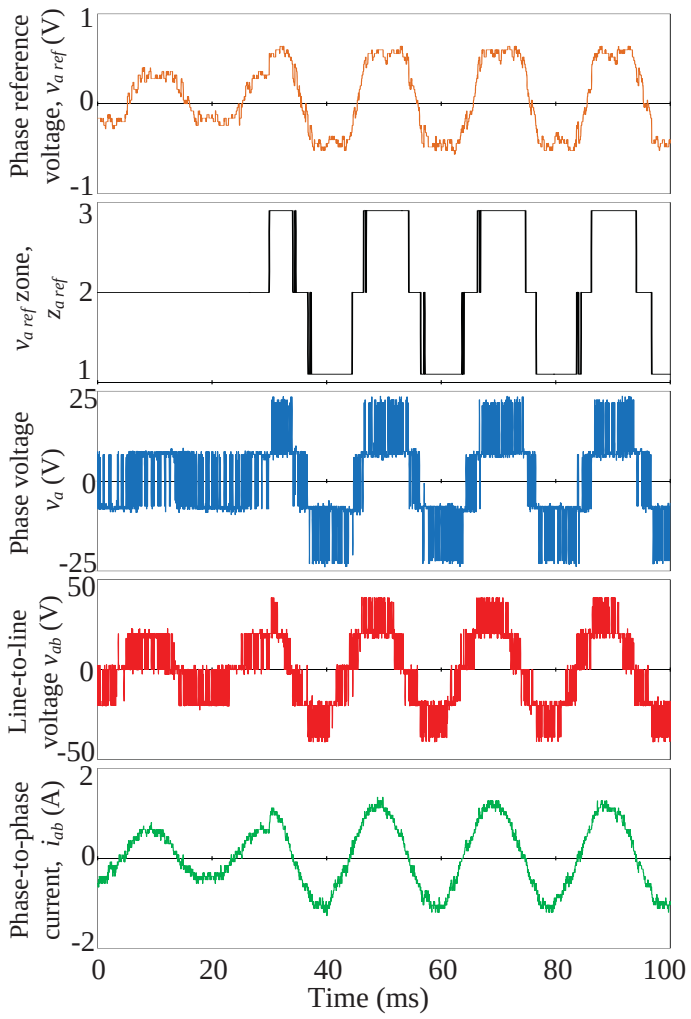


FIGURE 5.10: Experimental results with three legs connected in parallel showing a step in the modulation index m_a from 0.3 to 0.6. The reference signal includes random noise to represent a control action. From top to bottom: phase-a reference voltage, reference zone, phase voltage, line-to-line voltage, and phase-to-phase current.

There is also a perceptible reduction in the current ripple. It can be seen that the change from the conventional to the proposed PS-PWM causes a slight imbalance in the leg currents that is not significant.

The experimental results obtained with three legs per phase, can be seen in Figs. 5.9 and 5.10. As phase c is not implemented in this configuration, the resistor load between phases a and b is $R = 20\Omega$. Fig. 5.9 shows the phase voltage (v_{a0}), the line-to-line voltage (v_{ab}) and the phase-to-phase current (i_{ab}) for m_a= 1.0. The current ripple reduction and the improvement in the quality of the line-to-line voltage can be noticed here too, although to a lesser extent than in the previous case, with two legs connected in parallel. In order to emulate the behavior of the modulator in a close-loop control system, a randomly shaped signal has been added to the reference signals. Fig. 5.10 displays such a reference signal for phase-a (v_{refa}), the internal signal generated by the

even/odd zone detector (z_{refa}), the equivalent phase voltage (v_{a0}), the equivalent line-to-line voltage (v_{ab}), and the phase-to-phase output current (i_{ab}). When at first m_a is 0.3, the reference signal is confined to Zone 2 and only one set of carriers is used. At t= 30 ms, there is a step change to m_a= 0.6 and, as all the zones are used, the dynamic selection of the carriers begins. Although the shape of the reference signal causes some additional zone transitions that imply changes in the set of carriers to be used, neither the equivalent phase voltage nor the output current is apparently affected.

5.5 Conclusion

This chapter has presented a new interleaved PWM implementation for VSIs with legs connected in parallel. With the proposed implementation, the quality of the line-to-line output voltages is improved owing to the fact that switching occurs exclusively between adjacent levels. The modulator makes use of two sets of n evenly phase-shifted carriers that are dynamically allocated. The implementation is presented in a general way so that it can be applied to multi-phase converters with any number of phases and any number of legs in parallel per phase. It is, therefore, appropriate for modular parallel converters. Because of the improvement in terms of line-to-line voltages, better THD values are achieved, which can lead to a reduction in the output filtering requirements.

Chapter 6

Application to Grid-Connected Voltage-Source Inverters

The current-balancing strategy presented in Chapter 3 is used in this chapter in the implementation of a grid-connected system in which the VSI is made up with legs connected in parallel. The aim of such an implementation is to build a modular system where a fair contribution to the output current from the parallel-connected legs is garanteed. Unlike in the previous chapters, where the converter with legs in parallel was tested operating with a passive load, in this chapter the converter is connected to the electricity grid. A voltage-oriented control (VOC), which is capable to regulate the dc-link voltage as well as the amount of reactive current injected into the grid, is used. Such a modular converter can be applied to grid-connected systems including, but not limited to, distributed generation.

6.1 Introduction

Distributed generation systems are becoming increasingly common these days. For a proper grid connection, the energy delivered by such devices, like solar PV panels or wind turbines, needs to be processed through power electronic converters. In order to increase the rated power of power electronic converters, either the voltages or the currents can be increased (or both of them).

The strategy presented in this thesis is to increase the output rated current of a VSI by means of adding legs connected in parallel. In VSIs, if the dc-link is fed by a current source, the converter itself takes care of the dc-link voltage regulation. Therefore,

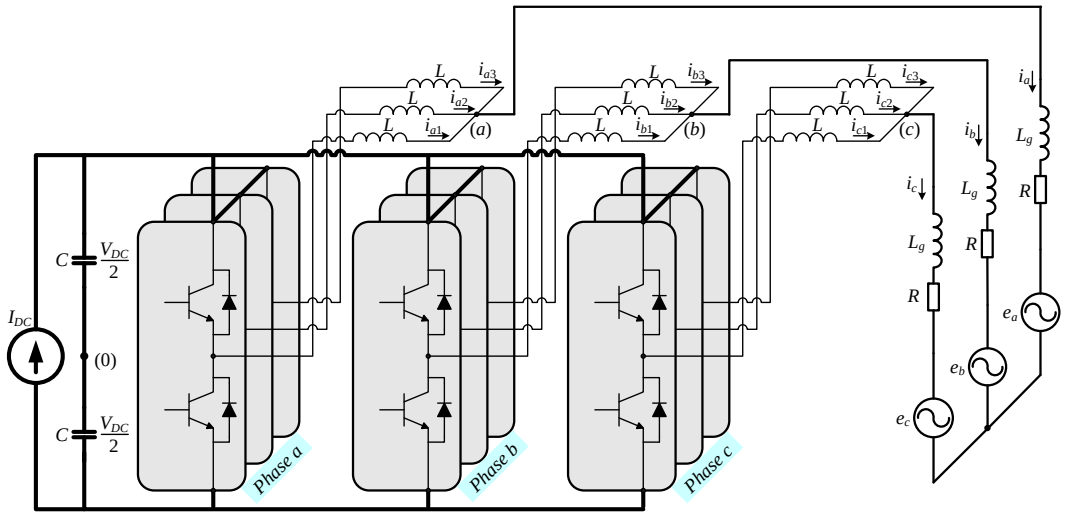


FIGURE 6.1: Grid-connected structure.

a proper control loop is needed. In the implementation described in this chapter, a VOC [93, 94] is used.

This chapter is organized as follows. Firstly, a three-phase grid-connected converter with three legs in parallel per phase is introduced. In the following sections, the current balancing technique used in this application for the particular case of three legs connected in parallel is presented and the control loop is described. Finally, some simulation and experimental results are presented. In the experimental results, the three-phase converter is tested with two legs connected in parallel.

6.2 The Grid-Connected System

The core of the plant used to implement and test the current-balancing control strategy is a three-phase grid-connected inverter whose phases are made up with three legs connected in parallel. The simulations have been run on a three-leg per phase VSI, whereas the experimental results have been obtained on a VSI with two legs per phase, on account of the number of operating VSIs available and due to the limitations in the computing speed of the dSPACE platform and its ControlDesk available in the TIEG's laboratory. Fig. 6.1 illustrates the version that includes three legs per phase. The primary source of energy is represented by a current source. This current could come from different kinds of sources, such as PV panels, wind turbines, or storage energy systems. The dc-link voltage is regulated by the VOC.

In this study, no magnetic coupling among the inductors is assumed; therefore, the equivalent output inductance is $L/3$. Consequently, the same inductances used for the

parallel connection among the legs contribute to the output inductance of the phase needed in grid-connected applications. Additional inductances may be required. L_g inductances stand for both, the intrinsic grid impedances and those additional inductances. The total inductance can be represented by L_t, where $L_t = L_g + L_{eq}$ with $L_{eq} = L/3$.

6.3 Current Balancing Method

The current-balancing strategy that was introduced in Chapter 3 for the connection of legs in parallel and was tested operating with a passive load is applied to the grid-connected three-phase system studied in this chapter. A summary of the main concepts and equations used for the particular case of $n = 3$ are given next.

The relationship between voltages and currents in each leg of the system in Fig. 6.1 is

$$L\frac{di_{xy}}{dt} = v_{xy} - v_{x0} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2, 3\} \tag{6.1}$$

Adding up the terms for each phase (x), and taking into account that $i_x = i_{x1} + i_{x2} + i_{x3}$, (6.1) becomes:

$$L\frac{di_x}{dt} = v_{x1} + v_{x2} + v_{x3} - 3v_{x0}. \tag{6.2}$$

If we think of $v_{x\mathrm{COM}}$ as the voltage that would be generated from an equivalent single leg, then (6.2) can be written as

$$L_{eq}\frac{di_x}{dt} = v_{x\mathrm{COM}} - v_{x0}; \tag{6.3}$$

$$\text{where} \quad L_{eq} = \frac{L}{3} \quad \text{and} \quad v_{x\mathrm{COM}} = \frac{v_{x1} + v_{x2} + v_{x3}}{3}. \tag{6.4}$$

If the locally-averaging operator is applied to the equations, the switching frequency ripples in the variables are removed and they become continuous.

Considering that the locally-averaged variable $\bar{v}_{x\mathrm{COM}}$ becomes the global reference voltage of the phase, i.e. $\bar{v}_{x\mathrm{COM}} = v_{x\mathrm{REF}}$, (6.3) can be written as follows:

$$L_{eq}\frac{d\bar{i}_x}{dt} = \bar{v}_{x\mathrm{COM}} - \bar{v}_{x0}. \tag{6.5}$$

From (6.5), the averaged equivalent leg of the whole phase can be deduced, as it is shown in Fig. 6.2.

If there were no current balancing control in the system, every leg of a same phase would receive the very same voltage reference, $\bar{v}_{\mathrm{REF}}$. However, in order to provide a

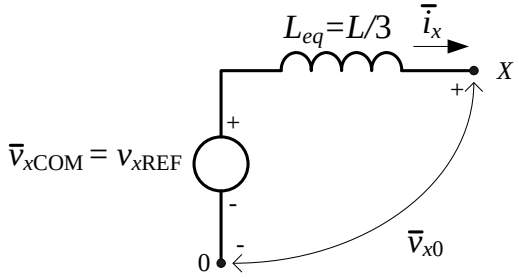


FIGURE 6.2: Averaged equivalent leg.

control law for every leg current, each individual voltage is modified as follows:

$$\bar{v}_{xy} = v_{x\mathrm{REF}} + \Delta\bar{v}_{xy} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2, 3\}. \tag{6.6}$$

Taking into account that the control variables should not affect the output voltage generated by the leg ($\bar{v}_{x\mathrm{COM}} = v_{x\mathrm{REF}}$), the control voltages have to meet the following condition:

$$\Delta\bar{v}_{x0} = \Delta\bar{v}_{x1} + \Delta\bar{v}_{x2} + \Delta\bar{v}_{x3} = 0. \tag{6.7}$$

Since $v_{x\mathrm{COM}}$ becomes unaltered if restriction (6.7) is applied, $\bar{i}_x$ and $\Delta\bar{v}_{x0}$ will also be unaffected by the control variables.

Applying the locally-averaging operator to (6.1):

$$L\frac{d\bar{i}_{xy}}{dt} = \bar{v}_{xy} - \bar{v}_{x0} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2, 3\} \tag{6.8}$$

and adding the effect of the control variables, the following relationship is obtained:

$$L\frac{d(\bar{i}_{xy} + \Delta\bar{i}_{xy})}{dt} = \bar{v}_{xy} + \Delta\bar{v}_{xy} - \bar{v}_{x0} - \Delta\bar{v}_{x0}, \tag{6.9}$$

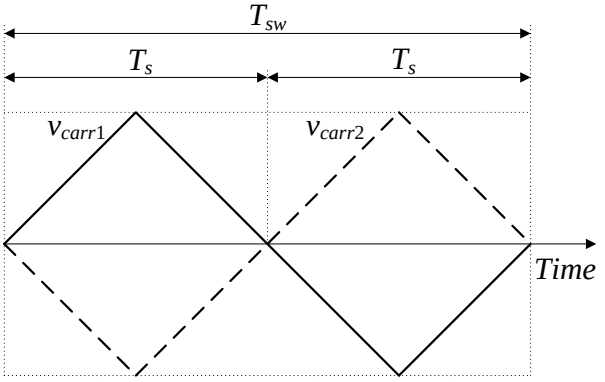
in which

$$\Delta\bar{i}_{xy} = \bar{i}_{xy} - \frac{\bar{i}_x}{3} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2, 3\}. \tag{6.10}$$

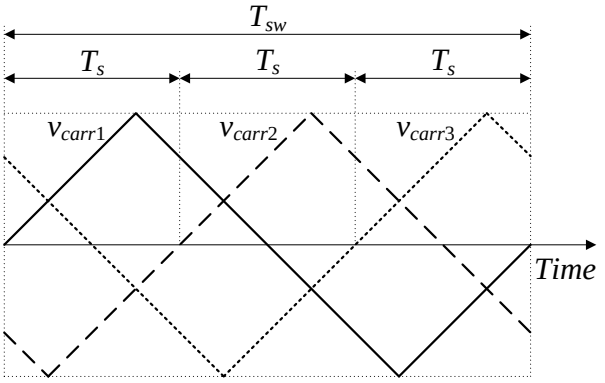
Comparing (6.8) and (6.9), and bearing in mind that $\Delta\bar{v}_x = 0$ as a consequence of the control restriction given in (6.7), the following relationship is obtained:

$$L\frac{d(\Delta\bar{i}_{xy})}{dt} = \Delta\bar{v}_{xy} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2, 3\}. \tag{6.11}$$

Assuming that there is a current imbalance $\Delta\bar{i}_{xy}(k)$ at the instant kT_s, the necessary voltage to achieve the reference current $\bar{i}_x/3$ can be calculated by imposing the condition



(a)



(b)

FIGURE 6.3: (a) Two and (b) three phase-shifted interleaved carriers.

$\Delta\bar{i}_{xy}(k+1) = 0$ to the discrete representation of (6.11), as follows:

$$L\frac{\Delta\bar{i}_{xy}(k+1) - \Delta\bar{i}_{xy}(k)}{T_s} = \Delta\bar{v}_{xy}(k) \quad \text{with} \quad \Delta\bar{i}_{xy}(k+1) = 0. \tag{6.12}$$

The timing diagram for this on-line process was presented in Fig. 3.2.

Sometimes, achieving current balance in a single sampling period may not be possible because of the large $\Delta\bar{v}_{xy}$ values required. If so, the control voltages should be limited to their maximum value in order to avoid overmodulation. Condition (6.7) has always to be satisfied, even when this restriction applies, to avoid distortion in the global output phase voltage.

The interleaving technique is applied to the system shown in Fig. 6.1. In order to achieve an apparent switching frequency three times higher than the individual switching frequency of each leg, three evenly phase shifted, interleaved carriers are used. As for the experimental results, where only two parallel legs have been implemented, two interleaved carriers have been used. Fig. 6.3 shows the the disposition of evenly phase-shifted carriers for both two and three parallel-connected legs.

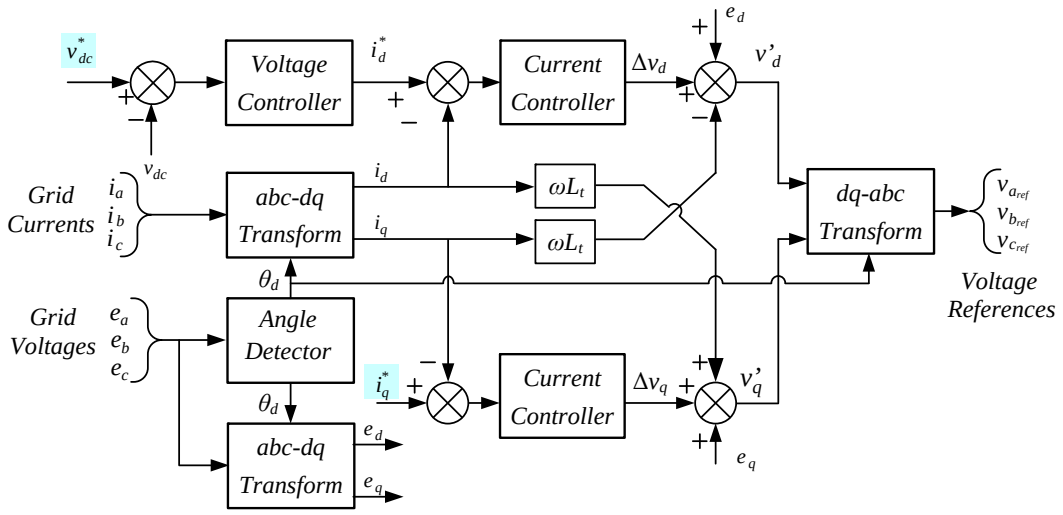


FIGURE 6.4: VOC diagram.

The output current ($\bar{i}_x$) and the individual current of each leg ($\bar{i}_{xy}$) are sensed at the maximum (or minimum) peak of the corresponding carrier ($v_{\text{carr}\,y}$). The value of the variable is calculated at any sampling period and applied to the particular modulation signal of each leg. Subsequently, the balancing dynamic is as fast as the apparent switching frequency ($f_s = 1/T_s$).

6.4 Control Strategy.

The control strategy used in this grid-connected system is a VOC. A short description of this type of control is presented next.

From the $d-q$ model of a grid-connected system [93, 94], the voltage references for the converter can be given by

$$v_{d\,ref} = e_d - \omega L_t i_q + \Delta v_d \tag{6.13}$$

and

$$v_{q\,ref} = e_q + \omega L_t i_d + \Delta v_q, \tag{6.14}$$

where,

$$\Delta v_d = L_t \frac{di_d}{dt} + R_t i_d \qquad \text{and} \qquad \Delta v_q = L_t \frac{di_q}{dt} + R_t i_q. \tag{6.15}$$

From (6.13) and (6.14), the control diagram shown in Fig. 6.4 can be deduced. In this scheme, the positive-sequence angle of the grid voltages (θ_d) is firstly detected. For the detection of this angle, the phase-locked loop (PLL) described in [95] is used. Then, θ_d is used for the $d-q$ transformations of the grid currents and voltages. As a consequence of such synchronization, the grid component e_q becomes zero when operating under

balanced and undistorted grid voltages. Besides, the d and q current components will define the active and reactive powers, respectively [94].

This control diagram has three loops: an external loop to control the dc-link voltage (v_{dc}) and two internal ones to regulate the d and q current components. The controller provides the voltages Δv_d and Δv_q that, applied to the equivalent grid impedances (L_t), will impose the desired grid currents. In order to obtain the voltage references for the converter, $v_{d\,ref}$ and $v_{q\,ref}$, two additional kinds of terms need to be added. One kind of them is added to cancel the crossing influence between the two current components. The other ones are the transformed grid voltages, e_d and e_q, although the latter will usually be zero.

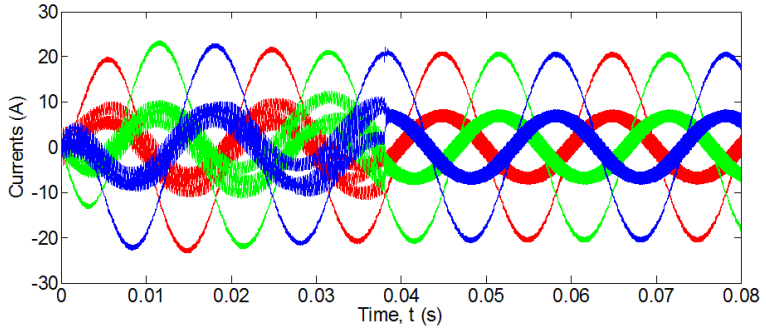
In order to achieve unity power factor, the reactive current reference (i_q^*) is normally zero for many applications. However, some regulations require imposing a value different from zero during particular circumstances such as grid voltage sags. Under such conditions, specific regulations define the amount of reactive power that should be injected into the electrical grid.

6.5 Simulation Results

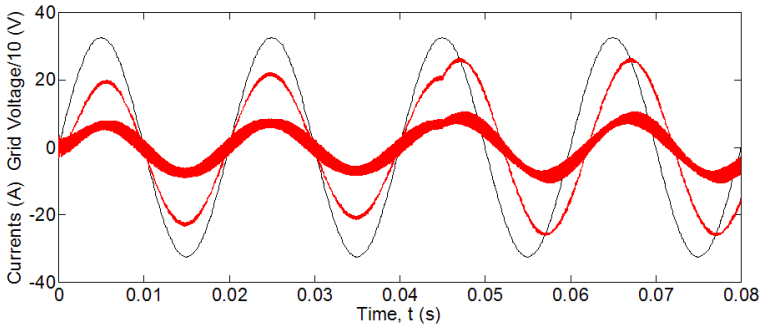
A model of the three-phase grid-connected VSI that includes three legs connected in parallel per phase (Fig. 6.1) and the proposed controllers has been developed in Matlab-Simulink. The main parameters of the model are the following: grid voltages 380 V - 50 Hz; grid inductors L_g= 1 mH; leg inductors L= 10 mH with an internal resistance of R= 0.05 Ω; dc-link capacitor C= 2 200 μF; dc-link reference voltage V_{dc}^*= 1 000 V; dc-link input current I_{dc}= 10 A; carrier frequency f_{sw}= 5 kHz; and reference reactive current i_q^*= 0.

Fig. 6.5(a) shows the system starting with the balancing control disconnected. It can be seen that the currents are not equal and therefore some legs carry more current than the others. The balancing control is activated at the instant t= 38 ms. It can be observed that the three currents are quickly balanced and the legs carry similar current values henceforth. Thus, similar power losses are to be expected in all the transistors of the converter. Additionally, the ripple in any of the output phase currents is much smaller than the ripple in their contributing leg currents, due to the benefits of the interleaving effect.

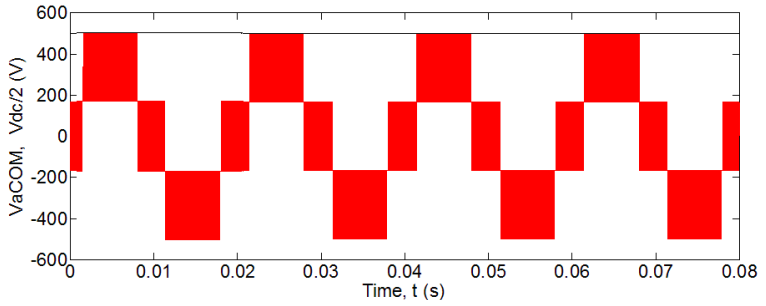
In order to test the reactive-current control, Fig. 6.5(b) shows the phase-a leg and grid currents, and the grid voltage of that phase. At the beginning of the process the reactive current reference is zero but it is changed at the instant of t= 45 ms, in which it



(a)



(b)



(c)

FIGURE 6.5: Simulation results of the grid-connected system. (a) Leg and phase currents with balancing control activation. (b) Leg and phase currents and grid voltage with reactive current reference change. (c) Dc-link voltage and equivalent phase voltage ($v_{a\,\mathrm{COM}}$).

becomes i_q^*= -20 A. It can be noticed that the relative phase of the grid current changes and it is no longer in phase with the corresponding grid voltage.

Fig. 6.5(c) shows the equivalent voltage of phase a, i. e. $v_{a\,\mathrm{COM}} = (v_{a1} + v_{a2} + v_{a3})/3$. It can be seen that the equivalent voltage takes four levels as it does in a multilevel converter. This figure also shows the dc-link voltage ($v_{dc}/2$) which is regulated to its reference value.

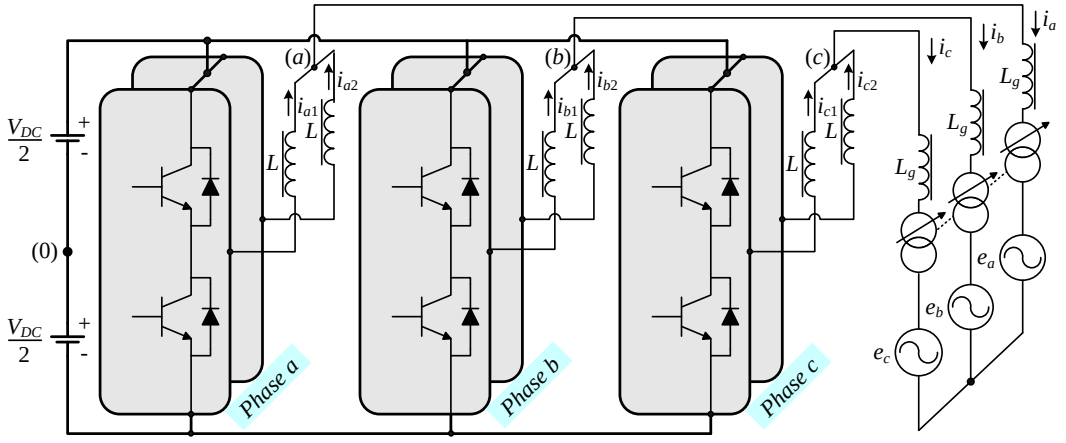


FIGURE 6.6: Circuit diagram of the experimental setup consisting of a three-phase grid-connected inverter with two legs in parallel per phase.

TABLE 6.1: Specifications of the Grid-Connected Laboratory Prototype

Symbol	Parameter	Value
V_{dc}	dc-bus voltage	80 V
f	Grid frequency	50 Hz
v_g	Grid voltage	220 V
t_a	Transformation ratio	12/220
n	Number of legs per phase	2
f_{sw}	Carrier/switching frequency	2.77 kHz
L	Leg inductor	6 mH
L_g	Grid inductor	1.5 mH

6.6 Experimental Results

As a first stage of the experimental checking on this study, a three-phase laboratory prototype has been built. Due to the limitations in the features of the ControlDesk linked to the dSPACE board mentioned before, the implementation of a three-phase VSI with three legs in parallel per phase has not been possible. Besides, in order to allow the ControlDesk to handle all the interface signals in real time, the time computing step has had to be increased up to 18 μs, which sets the minimum achievable dead time for the transistors and that is far too large. The implemented VSI has two legs connected in parallel per phase and it is fed by a voltage source. Therefore, the part of the control loop that regulates the input voltage has not been implemented either. The connection to the grid has been made by means of an adjustable autotransformer that was set to a 12/220 transformation ratio. Fig. 6.6 shows the scheme of the system that has been set up and Table 6.1 summarizes the main parameters.

The fact that only two legs per phase are used, affects the current-balancing method described in Section 6.2 in the following way: The relationship between voltages and

currents in each leg of the system in Fig. 6.6 is

$$L\frac{di_{xy}}{dt} = v_{xy} - v_{x0} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2\} \tag{6.16}$$

Adding up the terms for each phase (x), and taking into account that $i_x = i_{x1} + i_{x2}$, (6.16) becomes:

$$L\frac{di_x}{dt} = v_{x1} + v_{x2} - 2v_{x0}. \tag{6.17}$$

The expression of the voltage that would be generated from an equivalent single leg $v_{x\text{COM}}$, was defined in (6.3). The values of L_{eq} and $v_{x\text{COM}}$ that appear in (6.5) and in Fig. 6.2 are now

$$L_{eq} = \frac{L}{2} \quad \text{and} \quad v_{x\text{COM}} = \frac{v_{x1} + v_{x2}}{2}. \tag{6.18}$$

In order to provide a control law for every leg current, each individual voltage is modified as follows:

$$\bar{v}_{xy} = v_{x\text{REF}} + \Delta\bar{v}_{xy} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2\}. \tag{6.19}$$

Taking into account that the control variables should not affect the output voltage generated by the leg ($\bar{v}_{x\text{COM}} = v_{x\text{REF}}$), the control voltages have to meet the following condition:

$$\Delta\bar{v}_{x0} = \Delta\bar{v}_{x1} + \Delta\bar{v}_{x2} = 0. \tag{6.20}$$

Since $v_{x\text{COM}}$ becomes unaltered if restriction (6.20) is applied, $\bar{i}_x$ and $\Delta\bar{v}_{x0}$ will not be affected by the control variables either.

The application of the locally-averaging operator to (6.16) leads to:

$$L\frac{d\bar{i}_{xy}}{dt} = \bar{v}_{xy} - \bar{v}_{x0} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2\} \tag{6.21}$$

and considering the effect of the control variables into (6.21) the following expression

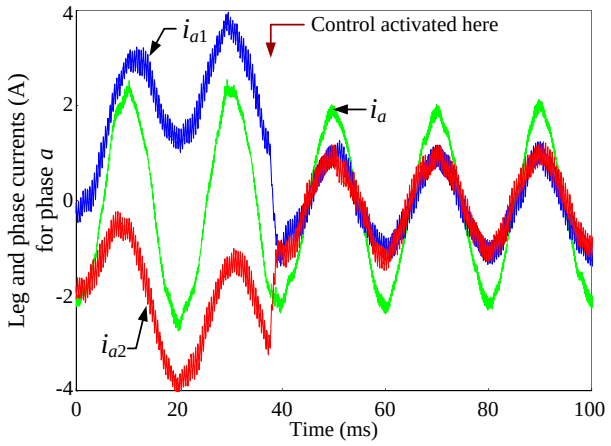
$$L\frac{d(\bar{i}_{xy} + \Delta\bar{i}_{xy})}{dt} = \bar{v}_{xy} + \Delta\bar{v}_{xy} - \bar{v}_{x0} - \Delta\bar{v}_{x0}, \tag{6.22}$$

is again obtained, but in which now

$$\Delta\bar{i}_{xy} = \bar{i}_{xy} - \frac{\bar{i}_x}{2} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2\}. \tag{6.23}$$

Comparing (6.21) and (6.22), and bearing in mind that $\Delta\bar{v}_{x0} = 0$ as a consequence of the control restriction given in (6.20), the following relationship is obtained:

$$L\frac{d(\Delta\bar{i}_{xy})}{dt} = \Delta\bar{v}_{xy} \quad \text{for} \quad x = \{a, b, c\} \quad \text{and} \quad y = \{1, 2\}. \tag{6.24}$$



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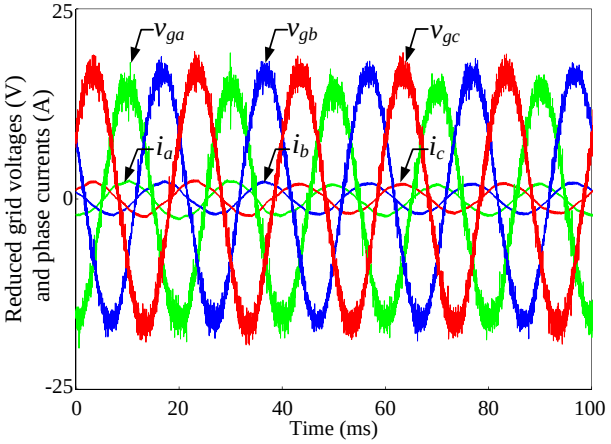

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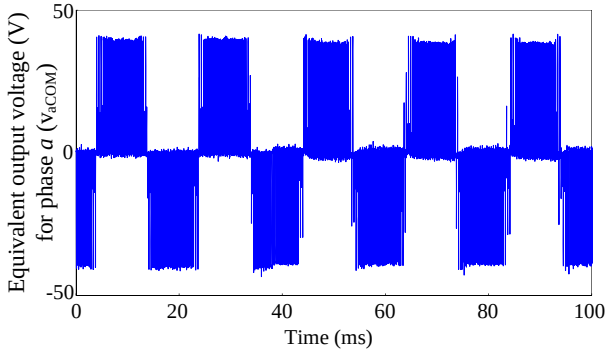

(c)

FIGURE 6.7: Transient current imbalance and activation of the compensator. (a) Leg and phase currents for Phase-a. (b) Phase currents and reduced grid voltages. (c) Phase-a output voltage.

Assuming that there is a current imbalance $\Delta\bar{i}_{xy}(k)$ at the instant kT_s, the necessary voltage to achieve the reference current $\bar{i}_x/2$ can be calculated by imposing the condition $\Delta\bar{i}_{xy}(k+1) = 0$ to the discrete representation of (6.11), as described in (6.12) and illustrated in Fig. 3.2.

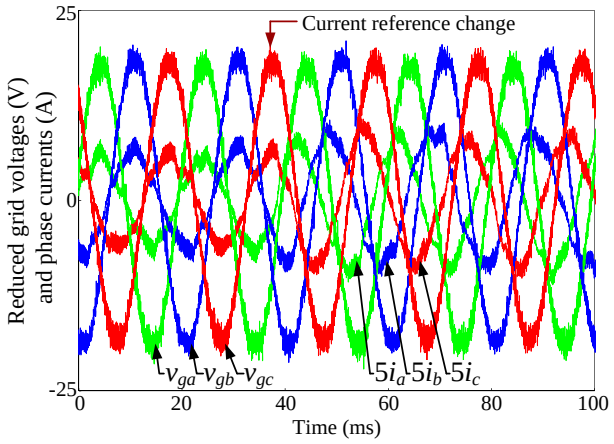

FIGURE 6.8: Effect of a sudden change of the i_q^* value on the phase of the output currents.

In order to test the velocity of the balancing control, a current imbalance has been provoked by applying an uncontrolled ΔV to the voltage references of the legs of phase a with the balancing control disconnected. The current references were set at $i_d^* = 2.5$ A and $i_q^* = 0$ A. Fig. 6.7(a) shows the leg currents and the output current for phase-a. The balancing control is activated at the instant t= 38 ms. It can be noticed that the two leg currents are balanced almost forthwith and the legs carry similar current values since then on. Additionally, the ripple in any of the output phase currents is much smaller than the ripple in their contributing leg currents, due to the benefits of the interleaving effect. Fig. 6.7(b) shows the phase currents and the reduced grid voltages. No additional distortion can be appreciated in phase-a current due to the leg-current imbalance. In Fig. 6.7(c) the output voltage for phase-a is shown. It illustrates how even though a two-level VSI is used, due to the averaging effect of the parallel-connection of the legs, the output voltage for a single phase has three levels.

As for the testing of the reactive-current control, a step change in the i_q^* reference value has been applied as can be seen in Fig. 6.8. Fig. 6.8 shows the phase currents and the reduced grid voltages. At the beginning of the image the reactive current reference is i_q^*= 0 A but at the instant of t= 37 ms is changed to i_q^*= 1.5 A, while the active current reference i_d^* is kept unchanged at 1.5 A. It can be noticed that the relative phase and the amplitude of the grid currents change and they are not in phase with their corresponding grid voltage anymore.

The control of the energy flow from or to the grid has been tested too. Fig. 6.9 displays the phase currents and the reduced grid voltages and illustrates the change in the phase of the output currents when a step change in the sign of the active reference current i_d^* is applied. At the beginning of the image the active current reference value is

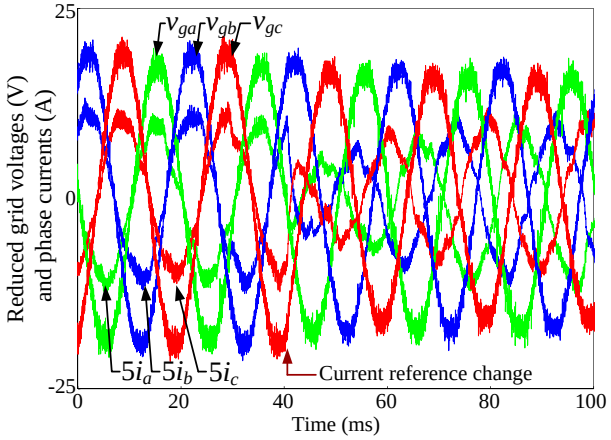

FIGURE 6.9: Effect on the phase of the output currents of a change in the sign of the active current reference (i_d^*).

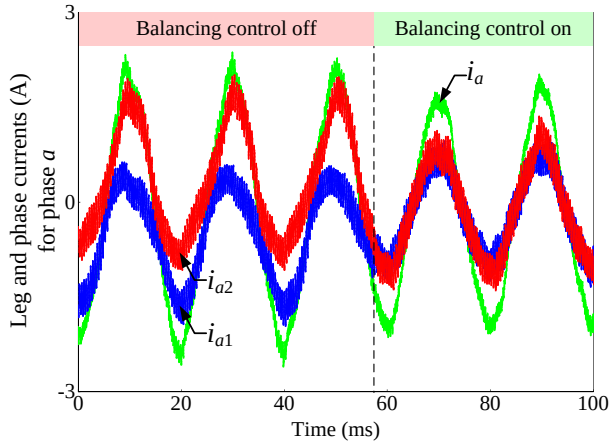

FIGURE 6.10: Continuous current imbalance produced by a small dc voltage difference between the legs and activation of the compensator.

set to $i_d^* = 2.5$ A and changed to $i_d^* = -2.5$ A at the instant of $t = 40$ ms. The reactive current reference is held to $i_q^* = 0$ A throughout the whole process.

In order to emulate the case of a difference in the voltage drops on the transistors of two paralleled legs, a low dc-voltage has been added in series with the transistor of one leg by means of a battery. This process crates a permanent current imbalance as can be seen in the left part of Fig. 6.10. Since $t = 56$ ms on, when the current balancing control is activated, the currents are balanced almost instantaneously, thus compensating the potentially damaging permanent imbalance.

6.7 Conclusion

The current balancing strategy introduced in Chapter 3 is tested in a grid-connected VSI. Each phase of the inverter is made up with two or three legs connected in parallel

through uncoupled inductors. The current balancing strategy implemented can achieve evenly shared currents among the legs with very fast dynamics. A VOC loop is able to regulate the dc-link voltage and to control the phase of the current delivered to the grid, thus controlling the amount of reactive current or the sign of the energy flow.

This system has special interest for applications such as distributed generation, energy storage, and power quality devices. The particularity of having more than one leg per phase allows for not only increasing the rated power of the converter, but also for improving fault tolerance capability. In the case of failure of one switch, the corresponding leg could be isolated and the system would be able to keep on running, with a reduction of the maximum output current and power, though.

Chapter 7

Conclusion and Future Research

This chapter summarizes the main conclusions of this thesis and introduces some future research topics that can be derived from it.

7.1 Conclusion

Achieving a fair contribution to the output current of the parallel-connected legs of a power inverter is a remarkable challenge. The current balancing technique presented in Chapter 3 is capable of achieving even current distribution with very fast dynamics. It is based on calculating the exact control actuation needed for current balance; therefore, no PI controller is required. The proposed balancing technique has been formulated in such a way that can be applied to converters with any number of legs connected in parallel. The inductors utilized for the implementation of the parallel-connection of the legs can be either magnetically coupled or uncoupled. The use of coupled inductors allows for a size reduction in the amount of magnetic material needed. Depending on the degree of coupling and the control mechanism a converter is capable of responding faster to load transient. However, as the contributions to the output current from magnetically-coupled legs are highly cross-influenced, there is no flexibility in terms of modularity and management in case of faulty legs. Modularity and fault-tolerant operation are easier to deal with if uncoupled inductors are used. The balancing method can be applied regardless of whether the inductors are magnetically coupled or not. The results show that currents are quickly balanced no matter what the reason for the imbalance is. Permanent current imbalances are the most dangerous and can be provoked by slight differences in the voltage drops across the power semiconductors.

In Chapter 4 a new implementation of interleaved PWM for VSC with legs connected in parallel which is able to produce interleaving using just a single carrier is presented.

Therefore, there is no need to generate n phase-shifted carriers as it is usually required to achieve such an effect. The modulation signals are properly shifted and rescaled to achieve the same effects as in the case of an n-carrier modulation. The proposed technique is presented in a general way so that it could be applied to a converter with any number of parallel legs per phase (i.e. n legs). It is, therefore, appropriate for modular parallel converters. The modulation algorithm can be implemented in a DSP or a FPGA. Since a single carrier signal is used, the problems associated with carrier synchronization to achieve proper phase shifting are avoided. Furthermore, when the proposed algorithm is implemented in a DSP, a higher number of legs connected in parallel can be controlled using the PWM units available within the DSP.

It is well known that modulation techniques like PD-PWM generate better line-to-line output voltages than PS-PWM in VSI. However, LS-PWM techniques, such as PD-PWM, cannot be applied without modification in converters with legs connected in parallel, as this would create dc-voltage components across the inductors and produce extremely large circulating currents. In Chapter 5 a new interleaved PWM implementation for VSIs with legs connected in parallel has been presented. With the proposed implementation, the quality of the line-to-line output voltages is improved owing to the fact that switching occurs exclusively between adjacent levels. The proposed modulator makes use of two sets of n evenly phase-shifted carriers that are dynamically allocated. The implementation is presented in a general way so that it can be applied to multi-phase converters with any number of phases and any number of legs in parallel per phase. It is, therefore, appropriate for modular parallel converters. Because of the improvement in terms of line-to-line voltages, better THD values are achieved, which can lead to a reduction in the output filtering requirements.

In Chapter 6 the current balancing strategy described in Chapter 3 is applied to a grid-connected three-phase inverter which is made up of three legs connected in parallel per phase. The current balancing strategy implemented there can achieve evenly shared currents among the legs with very fast dynamics. A VOC loop is able to regulate the dc-link voltage and to control the reactive current delivered to the grid. This system has special interest for applications such as distributed generation or energy storage, among others. The fact that the VSI has more than one leg per phase allows not only for increasing the rated power of the converter by increasing the output current capability, but also for implementing fault-tolerant operation capability. In the case of failure of one switch, i.e. one leg, the corresponding leg could be isolated and the system would be able to keep on working, in spite of a reduction in the maximum output current and power.

7.2 Future Work

From the work developed in this thesis, new research areas can be foreseen. Some studies have already been initiated while others, suggested in this section, are just basic ideas that need to be confirmed.

- **VSIs in parallel with common or isolated dc-buses**

  The main concern in case of parallel operation of VSIs is the load current distribution between the parallel-connected units. The deviation from the desired current level is usually referred to as circulating current. Depending on the parallel configuration, there are certain differences in the circulating current characteristics [76]. For example, if the units are connected directly in parallel from both the input and output sides, thus sharing the their dc-bus, additional current paths may be formed between the units, and because of this, the sum of three-phase currents of a single unit may not be equal to zero [96]. The validity of the current balancing method presented in Chapter 3 has only been verified on VSI with a common dc-bus. Future work concerning that should extend it to the case of parallel-connected VSI with isolated dc-buses.

- **Current balancing technique for multilevel VSIs with legs in parallel**

  The current balancing method presented in Chapter 3 has only been posited for two-level VSIs. However, the generic way it has been stated makes it very likely to be extended and generalized to the parallel connection of multilevel converters. To that extent, a first step has been taken in [60] where the aforementioned balancing technique is the core of a new strategy to achieve balanced operation of modular multilevel converters with legs connected in parallel.

- **Other balancing techniques for multi-leg VSIs**

  A modulation technique that combines SHE-PWM with the selection of redundant states in order to curtail the circulating currents in two paralled-connected NPC inverters has been developed. The extension of such a technique to a larger number of paralleled inverters, regardless whether they are two-level or multilevel inverters, is something that is worth studying.

- **Universal modulator**

  In Chapter 4, a technique to implement PS-PWM based on the use of just one carrier was presented. This single carrier was linked to a code sequencer and to a so-called pinpointing block whose main role was to determine the instantaneous position of the modulating signal at any time. Combining such information with

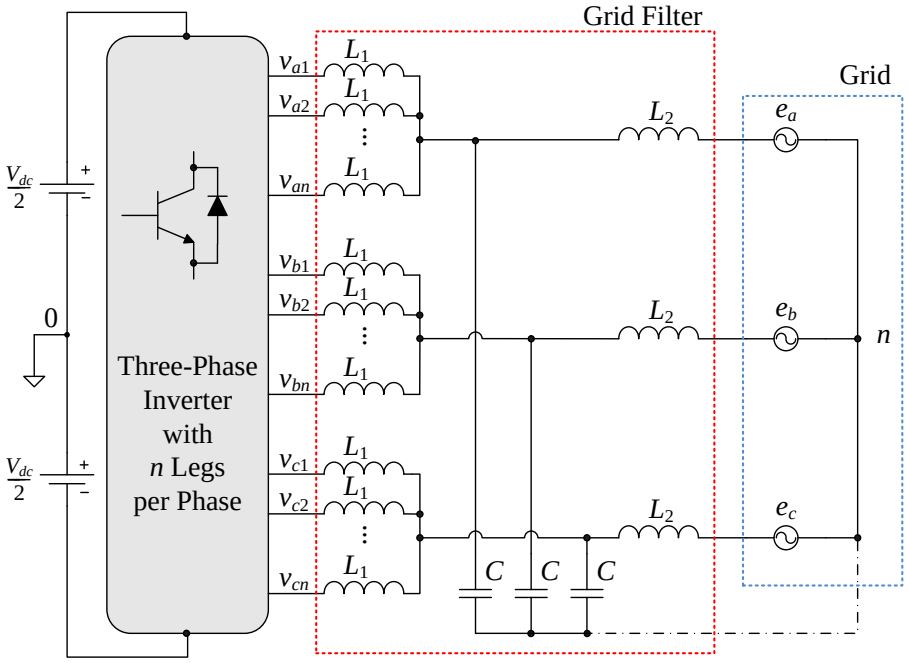

FIGURE 7.1: L-C-L filter in a grid-connected three-phase VSI with paralleled legs.

an alternative code sequence should be able to allow for the implementation of a different modulation strategy, e.g. any LS-PWM, such as PD-PWM, POD-PWM or APOD-PWM. The goal for this future research would be to implement LS-PWM using one single carrier instead of a set of level-shifted ones. The ultimate goal would be the implementation of a universal modulator that based on just one carrier which, upon user choice, could produce either PS-PWM or any of the LS-PWM. As the latter are multilevel modulation techniques, such a universal modulator would work for either two-level and multilevel converters.

- **Magnetic material**

  A new modeling approach for analyzing coupled inductors is proposed in [19] and a novel canonical symmetrical circuit model is developed. The proposed model is easy to use and allows for comparing paralleled power converters utilizing coupled or uncoupled inductors with ease. The symmetrical model reveals how model parameters affect the steady state and transient performance of power converters. It is found that coupled inductors are able to respond faster to a load transient if phase overlapping is allowed, but also that the output voltage ripple in a coupled inductor converter is always greater than that in an uncoupled inductor converter if the comparison is carried out with the very same L value. This conclusion apparently contradicts what is said in [20, 21]. Some research needs to be done on that issue.

- **Single inductor vs. L-C-L output filtering**

The two most popular topologies of high frequency filters to attenuate the PWM harmonics in grid-connected inverters are the L and L-C-L filters [84]. Fig. 7.1 illustrates an L-C-L filter in a grid connected VSI made up with legs connected in parallel. As L filters are first other filters, the switching frequency of the converter should be high enough so that a noticeable attenuation of the harmonics caused by the inverter switching could be achieved with reasonably sized inductors. As L-C-L filters are third order filters, a higher attenuation at the switching frequency can be achieved with the same inductor value. This extra attenuation depends on the relationship between the resonance frequency of the filter and the frequency of the switching harmonics. As they include a capacitor, such type of filters come in handy when reactive power needs to be injected into the grid. Their main drawbacks are a more limited variety of options for the choice of the components and some more difficult- to-handle control algorithms.

According to [83] a good performance in terms of current harmonic distortion can be achieved using strongly inductive filters so that resonances could be avoided. The main disadvantage of strongly inductive filters is the high consumption of reactive energy when used in high current applications. This disadvantage can be overcome by the use of a converter with multiple legs or by converters in parallel and an appropriate modulation strategy [48].

The effect on the filtering requirements in case of VSis with legs connected in parallel can be further investigated.

- **Carriers' disposition**

  A new disposition of the carriers for a two-level multi-phase VSI PS-PWM was presented in Chapter 5. Such disposition helps improve the quality of the line-to-line output voltage in VSIs made up with parallel-connected legs. The method is based on a dynamic selection of the set of carriers used for carrying out the modulation. Applying the same strategy to implement the modulation for multilevel converters would open another research line. Such a strategy fits in particularly well for floating capacitor converters and there is already some ongoing research about it. Besides, a straightforward change of the set of carriers implies an increase, albeit limited, in the actual number of switchings in the VSI power switches. Some modification in the way the transitions between the sets of carriers are performed in order to avoid such increase should be researched.

- **Fault tolerance techniques for VSI with legs in parallel**

  One of the advantages inherent to paralleling legs, apart from flexibility and modularity, is the fact that converters may become fault-tolerant systems. To allow for operation under faulty conditions, some additional hardware able to modify

the topology should be included. Software would have to be modified too; primarily, the modulation strategy. The fact that a VSI with legs in parallel has more switching semiconductors than a conventional VSI, implies that it is more likely for a fault to happen. Nevertheless, having a bigger amount of output voltage levels also opens a fan of possibilities to keep the inverter on duty, under restricted operation though.

Faulty switches in VSI with parallel-connected legs will be considered. This will include the detection of the fault for a start and then, once spotted the faulty switch and identified the kind of fault (short-circuit or open-circuit), the modulation stage should be reconfigured. Resumption of converter operation once it has been reconfigured should then be achievable.

Bibliography

[1] M. Hua, H. Hu, Y. Xing, and Z. He, "Distributed control for AC motor drive inverters in parallel operation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5361–5370, Dec. 2011.

[2] R. Li and D. Xu, "Parallel operation of full power converters in permanent-magnet direct-drive wind power generation system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1619–1629, Apr. 2013.

[3] X. Zhuang, L. Rui, Z. Hui, X. Dianguo, and C. H. Zhang, "Control of parallel multiple converters for direct-drive permanent-magnet wind power generation systems," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1259–1270, Mar. 2012.

[4] M. Borrega, L. Marroyo, R. Gonzalez, J. Balda, and J. L. Agorreta, "Modeling and control of a master-slave PV inverter with n-paralleled inverters and three-phase three-limb inductors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2842–2855, Jun. 2013.

[5] J. Rodriguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, and M. Perez, "Multilevel converters: an enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[6] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[7] K. K. Gupta and S. Jain, "Topology for multilevel inverters to attain maximum number of levels from given DC sources," *IET Power Electron.*, vol. 5, no. 4, pp. 435–446, Apr. 2012.

[8] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard, and D. Boroyevich, "A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 642–651, Feb. 2012.

[9] V. G. Agelidis and H. C. Goh, "Low-distortion variable-level PWM technique," *IEE Proc. Electr. Power Appl.*, vol. 145, no. 2, pp. 73–78, Mar. 1998.

[10] Z. Qiu and G. Chen, "Study and design of grid connected inverter for 2 MW wind turbine," in *Conf. Rec. IEEE IAS Annu. Meeting*, New Orleans, LA, 23-27 Sep. 2007, pp. 165–170.

[11] I. W. Jaskulski, H. Pinheiro, and L. Mariotto, "Multi-leg voltage source converter for grid connected wind turbines," in *Proc. ICCEP*, Capri, Italy, May 21–23 2007, pp. 229–235.

[12] C. Wen, J. Li, X. Zhu, and H. Xu, "Research on circulation of parallel three-phase converters in MW wind power system," in *Proc. Workshop PEITS*, Guangzhou, China, Aug. 2–3 2008, pp. 349–354.

[13] L. Jian-lin, H. Shu-ju, L. Mei, Z. Ying, K. De-guo, and X. Hong-hua, "Research on the application of parallel back-to-back PWM converter on direct-drive wind power system," in *Proc. IEEE Int. Conf. Elect. Utility DRPT*, Nanjuing, China, Apr. 6–9 2008, pp. 2504–2508.

[14] W. Hu, Y. Wang, W. Yao, J. Wu, H. Zhang, and Z. Wang, "An efficient experimental method for high power direct drive wind energy conversion systems," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Rhodes, Greece, Jun. 15–19 2008, pp. 3955–3959.

[15] H. Cai, R. Zhao, and H. Yang, "Study on ideal operation status of parallel inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2964–2969, Nov. 2008.

[16] V. Agarwal and D. Krishna, "Statistical approach to robust design of control schemes for series or parallel connected power devices," *EPE J.*, vol. 19, no. 3, pp. 15–21, Sep. 2009.

[17] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "PD modulation scheme for three-phase parallel multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 690–700, Feb. 2012.

[18] R. Stala, "A natural DC-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008–5018, Nov. 2013.

[19] G. Zhu, B. McDonald, and K. Wang, "Modeling and analysis of coupled inductors in power converters," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1355–1363, May 2011.

[20] E. Laboure, A. Cuniere, T. A. Meynard, F. Forest, and E. Sarraute, "A theoretical approach to intercell transformers, application to interleaved converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 464–474, Jan. 2008.

[21] F. Forest, E. Laboure, T. A. Meynard, and V. Smet, "Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 812–821, Mar. 2009.

[22] J. Salmon, A. M. Knight, and J. Ewanchuk, "Single-phase multilevel PWM inverter topologies using coupled inductors," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1259–1266, May 2009.

[23] B. Cougo, T. Meynard, and G. Gateau, "Parallel three-phase inverters: optimal PWM method for flux reduction in intercell transformers," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2184–2191, Aug. 2011.

[24] Z. Di, W. Fei, R. Burgos, and D. Boroyevich, "Total flux minimization control for integrated inter-phase inductors in paralleled, interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1679–1688, Apr. 2012.

[25] J. Pou, J. Zaragoza, G. J. Capella, I. Gabiola, S. Ceballos, and E. Robles, "Current balancing strategy for interleaved voltage source inverters," *EPE J.*, vol. 21, no. 1, pp. 29–34, Jun. 2011.

[26] T. Lazzarin, G. Bauer, and I. Barbi, "A control strategy for parallel operation of single-phase voltage source inverters: analysis, design and experimental results," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2194–2204, Jun. 2013.

[27] M. Xie, Y. Li, K. Cai, P. Wang, and X. Sheng, "A novel controller for parallel operation of inverters based on decomposing of output current," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 3, Hong Kong, Oct. 2–6 2005, pp. 1671–1676.

[28] C. Zhang, F. Zu, Q. Zhao, W. Wu, and G. Chen, "An interactive following current-sharing control strategy for paralleled inverters in full digital," in *Proc. IEEE Int. Conf. Electr. Machines Syst. (ICEMS)*, vol. 2, Nanjing, Oct. 2–6 2005, pp. 1080–1083.

[29] H. M. Hsieh, T. F. Wu, Y. E. Wu, H. S. Nien, and Y. K. Chen, "A compensation strategy for parallel inverters to achieve precise weighting current distribution," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 2, Hong Kong, Oct. 2–6 2005, pp. 954–960.

[30] M. Yu, Y. Kang, Y. Zhang, M. Yin, S. Duan, H. Shan, and G. Chen, "A novel decoupled current-sharing scheme based on circulating-impedance in parallel multi-inverter system," in *Proc. IEEE IECON*, Taipei, Taiwan, Nov. 5–8 2007, pp. 1668–1672.

[31] J. C. Le Claire and G. Lembrouck, "A simple feedback for parallel operation of current controlled inverters involved in UPS," in *Proc. EPE Conf. Appl.*, Aalborg, Denmark, Sep. 2–5 2007, pp. 1–10.

[32] S. Fukuda and K. Matsushita, "A control method for parallel-connected multiple inverter systems," in *Proc. IET Int. Conf. Power Electron. Variable-Speed Drives*, London, UK, Sep. 21–23 1998, pp. 175–180.

[33] Y. K. Chen, T. F. Wu, Y. E. Wu, and C. P. Ku, "A current-sharing control strategy for paralleled multi-inverter systems using microprocessor-based robust control," in *Proc. IEEE TENCON Int. Conf. Electr. Electron. Technol.*, vol. 2, Singapore, Aug. 19 –22 2001, pp. 647–653.

[34] N. Talebi, M. A. Sadrnia, and S. M. R. Rafiei, "Current and voltage control of paralleled multi-module inverter systems," in *Proc. MED Control Autom.*, Thessaloniki, Greece, Jun. 24–26 2009, pp. 1498–1503.

[35] Q. C. Zhong, "Robust droop controller for accurate proportional load sharing among inverters operated in parallel," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1281–1290, Apr. 2013.

[36] S. Shah and P. S. Sensarma, "Three degree of freedom robust voltage controller for instantaneous current sharing among voltage source inverters in parallel," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3003–3014, Dic. 2010.

[37] R. Ramos, D. Biel, E. Fossas, and F. Guinjoan, "Sliding-mode control design applied to parallel-connected modular inverters through FPGA-based implementation," *IET Control Theory Appl.*, vol. 3, no. 12, pp. 1611–1624, Dec. 2009.

[38] B. Shi and G. Venkataramanan, "Parallel operation of voltage source inverters with minimal intermodule reactors," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 1, Seattle, USA, Oct. 3–7 2004, pp. 156–162.

[39] X. Yu and A. M. Khambadkone, "Reliability analysis and cost optimization of parallel-inverter system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3881–3889, Oct. 2012.

[40] Y. J. Ko, K. B. Lee, D. C. Lee, and J. M. Kim, "Fault diagnosis of three-parallel voltage-source converter for a high-power wind turbine," *IET Power Electron.*, vol. 5, no. 7, pp. 1058–1067, Aug. 2012.

[41] Y. Zhang and H. Ma, "Theoretical and experimental investigation of networked control for parallel operation of inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1961–1970, Apr. 2012.

[42] D. O. Neacsu, E. Wagner, and B. S. Borowy, "A simulation benchmark for selection of the PWM algorithms for three-phase interleaved converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1628–1636, Apr. 2008.

[43] D. G. Holmes, "A general analytical method for determining the theoretical harmonic components of carrier based pwm strategies," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 2, St. Louis, MO, USA, Oct. 12–15 1998, pp. 1207–1214.

[44] B. P. McGrath and D. G. Holmes, "A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, vol. 2, Galway, Ireland, Jun. 18–23 2000, pp. 674–679.

[45] ——, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[46] N. A. Azli, L. Y. Teng, and P. Y. Lim, "Implementation of a single-carrier multilevel PWM technique using field programmable gate array (FPGA)," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst. (PEDS)*, Bangkok, Thailand, Nov. 27–30 2007, pp. 836–841.

[47] S. Zainal, J. Aziz, and S. S. Ahmed, "Single carrier PWM scheme for cascaded multilevel voltage source inverter," in *Proc. IEEE Int. Conf. PEDS*, vol. 1, Singapore, Nov. 17–20 2003, pp. 406–410.

[48] I. W. Jaskulski, I. J. Gabe, J. P. da Costa, M. Stefanello, and H. Pinheiro, "Space vector modulation extended to voltage source converters with multiple legs in parallel," in *Proc. EPE Conf. Appl.*, Aalborg, Denmark, Sep. 2–5 2007, pp. 1–10.

[49] T.-P. Chen, "Dual-modulator compensation technique for parallel inverters using space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3004–3012, Aug. 2009.

[50] Y. Zhang and H. Ma, "Analysis of networked control schemes and data-processing method for parallel inverters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1834–1844, Apr. 2014.

[51] K. Zhi-zhong, Z. Chun-jiang, Z. Bo, and W. Xiao-huan, "Analysis of the conflict between close-loop control and the current-sharing of ac parallel inverters and parallel control strategy," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC)*, Wuhan, China, May 17–20 2009, pp. 368–372.

[52] W. Yao, M. Chen, J. Matas, J. M. Guerrero, and Z.-M. Qian, "Design and analysis of the droop control method for parallel inverters considering the impact of the complex impedance on the power sharing," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 576–588, Feb. 2011.

[53] M. Hua, H. Hu, Y. Xing, and J. M. Guerrero, "Multilayer control for inverters in parallel operation without intercommunications," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3651–3663, Aug. 2012.

[54] B. M. H. Jassim, B. Zahawi, and D. Atkinson, "Simple control method for parallel connected three-phase PWM converters," in *Proc. IET Int. Conf. PEMD*, Bristol, U.K., Mar. 27-29 2012, pp. 1–5.

[55] J. Shen, S. Schröder, B. Qu, Y. Zhang, K. Chen, F. Zhang, Y. Li, Y. Liu, P. Dai, and R. Zhang, "A high-performance 2x27 MVA machine test bench based on multilevel IGCT converters," in *Proc. IEEE Energy Conversion Congress Exposition (ECCE)*, vol. pp, Pittsburg, PA, USA, Sep. 14–18 2014, pp. 3224–3233.

[56] Y. Sahali and M. K. Fellah, "Selective harmonic eliminated pulse-width modulation technique (she pwm) applied to three-level inverter/converter," in *IEEE Int. Symp. Ind. Electron. (ISIE)*, vol. 2, Jun. 9–11 2003, pp. 1112–1117.

[57] S. R. Pulikanti and V. G. Agelidis, "Five-level active NPC converter topology: SHE-PWM control and operation principles," in *Proc. Australasian Univ. Power Eng. Conf. (AUPEC)*, 9–12 Dec. 2007, pp. 1–5.

[58] G. Konstantinou, V. G. Agelidis, and J. Pou, "Theoretical considerations for single-phase interleaved converters operated with SHE-PWM," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5124–5128, Oct. 2014.

[59] M. Narimani and G. Moschopoulos, "Improved method for paralleling reduced switch VSI modules: harmonic content and circulating current," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3308–3317, Jul. 2014.

[60] J. Pou, S. Ceballos, G. Konstantinou, G. J. Capella, and V. G. Agelidis, "Control strategy to balance operation of parallel connected legs of modular multilevel converters," in *Proc. IEEE Int. Symp. Ind. Electron. (ISIE)*, Taipei, Taiwan, May 28–31 2013, pp. 1–7.

[61] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[62] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Trans. Ind. Electron.*, vol. 39, no. 5, pp. 410–420, Oct. 1992.

[63] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based PWM for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 574–582, Mar./Apr. 2001.

[64] W. Tengfei and Z. Yongqiang, "Analysis and comparison of multicarrier PWM schemes applied in H-bridge cascaded multi-level inverters," in *IEEE Conf. Ind. Electron. Appl. (ICIEA)*, Jun. 15–17 2010, pp. 1379–1383.

[65] R. Naderi and A. Rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1257–1269, May 2008.

[66] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal pwm techniques," in *Proc. IEEE Conf. Ind. Electron. Appl. (ICIEA)*, Xian, China, May 25-27 2009, pp. 3399–3404.

[67] D. J. Kostic, Z. Z. Avramovic, and N. T. Ciric, "A new approach to theoretical analysis of harmonic content of PWM waveforms of single- and multiple-frequency modulators," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4557–4567, Oct. 2013.

[68] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015.

[69] S. K. T. Miller, T. Beechner, and S. Jian, "A comprehensive study of harmonic cancellation effects in interleaved three-phase vscs," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Orlando, FL, USA, Jun. 17–21 2007, pp. 29–35.

[70] B. P. McGrath, D. G. Holmes, M. Manjrekar, and T. A. Lipo, "An improved modulation strategy for a hybrid multilevel inverter," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 4, Rome, Italy, Oct. 8–12 2000, pp. 2086–2093.

[71] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, vol. 1, Fukuoka, Japan, May 17–22 1998, pp. 172–178.

[72] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Industry Appl.*, vol. 41, no. 3, pp. 855–865, May/Jun. 2005.

[73] J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[74] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Magazine*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[75] D. Floricau, E. Floricau, and G. Gateau, "New multilevel converters with coupled inductors: properties and control," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5344–5351, Dec. 2011.

[76] T. Itkonen, J. Luukko, and R. Pollanen, "Analysis of current characteristics of parallel three-phase voltage source inverters," in *Proc. EPE Conf. Appl.*, Barcelona, Spain, Sep. 8–10 2009, pp. 1–10.

[77] J. S. Siva Prasad and G. Narayanan, "Minimization of grid current distortion in parallel-connected converters through carrier interleaving," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 76–91, Jan. 2014.

[78] J. J. Nelson, G. Venkataramanan, and B. C. Beihoff, "Investigation of parallel operation of IGBTs," in *Conf. Rec. IEEE IAS Annu. Meeting*, vol. 4, Pittsburgh, PA, USA, Oct. 13–18 2002, pp. 2585–2591.

[79] S. Musumeci, R. Pagano, A. Raciti, F. Frisina, and M. Melito, "Parallel strings of igbts in short circuit transients: analysis of the parameter influence and experimental behavior," in *Proc. IEEE Ind. Electron. Society Conf. (IECON)*, vol. 1, Nov. 5–8 2002, pp. 555–560.

[80] Q. Zhao, Z. Chen, and W. Wu, "Improved control for parallel inverter with current-sharing control scheme," in *Proc. IEEE Int. Power Electron. Motion Control Conf. (IPEMC)*, vol. 3, Shanghai, China, Aug. 14–16 2006, pp. 1–5.

[81] P. Rodriguez, J. Pou, R. Pindado, J. Montanya, R. Burgos, and D. Boroyevich, "An alternative approach on three-dimensional space-vector modulation of three-phase inverters," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Recife, Brazil, Jun. 15–18 2005, pp. 822–828.

[82] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Industry Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.

[83] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263–272, Jan. 2006.

[84] E. J. Bueno, "Optimización del comportamiento de un convertidor de tres niveles NPC conectado a la red eléctrica," Ph.D. Thesis, Universidad de Alcalá, Dep. Electrónica, Alcalá de Henares, 2005.

[85] I. G. Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, vol. 2, St. Louis, MO, USA, Jun. 22–27 1997, pp. 1164–1170.

[86] "Matlab/Simulink Software package. version 7.5.0.342 (r2007b)." [Online]. Available: http://www.mathworks.com

[87] "DS1103 PPC Controller Board." [Online]. Available: http://www.dspace.com/en/ltd/home/products/hw/singbord/ppcconbo.cfm

[88] "ControlDesk software package." [Online]. Available: http://www.dspace.com/en/inc/home/support/suptrain/controldesk.cfm

[89] J. Ewanchuk and J. Salmon, "Three-limb coupled inductor operation for paralleled multi-level three-phase voltage sourced inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979–1988, May 2013.

[90] B. Ge, X. Lu, X. Yu, M. Zhang, and F. Z. Peng, "Multiphase-leg coupling current balancer for parallel operation of multiple MW power modules," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1147–1157, Mar. 2014.

[91] "TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812 digital signal processors data manual," 2001 rev. 2012. [Online]. Available: http://www.ti.com/lit/ds/symlink/tms320f2812.pdf.

[92] "TMS320x281x DSP event manager (EV) reference guide," Nov. 2004 rev. Jun 2007. [Online]. Available: http://www.ti.com/lit/ug/spru065e/spru065e.pdf

[93] M. Molinas, B. Naess, W. Gullvik, and T. Undeland, "Cage induction generators for wind turbines with power electronics converters in the light of the new grid codes," in *Proc. EPE Conf. Appl.*, Dresden, Germany, Sep. 11–14 2005, pp. 1–10.

[94] J. Pou, E. Robles, S. Ceballos, J. Zaragoza, A. Arias, and P. Ibanez, "Control of back-to-back-connected neutral-point-clamped converters in wind mill applications," in *Proc. EPE Conf. Appl.*, Aalborg, Denmark, Sep. 2–5 2007, pp. 1–10.

[95] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Industry Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.

[96] P. Ching-Tsai and L. Yi-Hung, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825–838, Apr. 2007.