DEVELOPMENT OF LOW-COST AND HIGH-EFFICIENCY COMMERCIAL SIZE N-TYPE SILICON SOLAR CELLS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2015

DEVELOPMENT OF LOW-COST AND HIGH-EFFICIENCY COMMERCIAL SIZE N-TYPE SILICON SOLAR CELLS

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This thesis work is dedicated to my parents Jae Man Ryu and Sun Ja Yeon, my brother Joong Sun Ryu, my wife Aekyung Jung, and my daughter Claire Dain Ryu. This work would have been incomplete without their encouragement, support, and love.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Dr. Ajeet Rohatgi for supervising my Ph.D. study and giving me the opportunity to conduct this study in the School of Electrical and Computer Engineering at Georgia Institute of Technology. I really appreciate his valuable advising and mentoring on my research. He has also spent much time in helping me to improve writing and presentation skills and to grow as a scientist.

I also would like to thank to Dr. Thomas K. Gaylord, Dr. Miroslav M. Begovic, Dr. Gee-Kung Chang, and Dr. Shreyes Melkote for serving as my thesis reading committee and giving advice on my thesis.

I acknowledge the gratitude to former and current colleagues at University Center of Excellence for Photovoltaics Research and Education (UCEP). Special thanks to Dr. Young-Woo Ok and Ajay Upadhyaya for their guidance, support, and valuable discussions. I am also grateful to James Keane, and Francesco Zimbardi for their extensive and professional assistance with equipment maintenance, to Carla East for providing an excellent administrative support and motherly affection, to Vijay Upadhyaya, Brian Rounsaville, and Elizabeth Lori Chang for their active support and cooperation and discussions in research. Thanks to Dr. Abasifreke Ebong, Dr. Ian Cooper, Dr. Rishi Ramanathan, Dr. Moon-Hee Kang, Dr. John Renshaw, Dr. Jiun-Hong Lai, Chia-Wei (Ricky) Chen, Eunhwan Cho, and Keeya Madani for their true relationship and generous support. Special thanks to Keith Tate, Dr. Manav Sheoran, and Dr. Arnab Das for their training and valuable discussions during early year of my Ph.D.

I would also like to thank to Suniva members (Dr. Atul Gupta, Dr. Adam Payne, Dr. Vijay Yelunder, Vinodh Chandrasekaran, Preston Davis, Liladhar Dahal) for their generous support and cooperation in my research.

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LIST OF SYMBOLS AND ABBREVIATIONS

AES	Auger electron spectroscopy
Al_2O_3	Aluminum oxide
APCVD	Atmospheric pressure chemical vapor deposition
ARC	Anti-reflection coating
B	Boron
BBr_3	Boron tribromide
BOS	Balance of system
BRL	Boron-rich layer
BSF	Back surface field
BSG	Borosilicate glass
BSRV	Back surface recombination velocity
CET	Chemical etching treatment
Cz	Czochralski
D_{it}	Interface state density
EQE	External quantum efficiency
FF	Fill factor
FSRV	Front surface recombination velocity
H_3BO_3	Boric acid
HIT	Heterojunction with Intrinsic Thin layer
HREM	High resolution electron microscopy
IBC	Interdigitated back contact

IQE	Internal quantum efficiency
I-V	Current-voltage
J_{0b}	Base saturation current density
$J_{0b\text{-}metal}$	J_{0b} in the metalized emitter surface
$J_{0b\text{-}pass}$	J_{0b} in the passivated emitter area
J_{0e}	Emitter saturation current density
$J_{0e\text{-}metal}$	J_{0e} in the metalized emitter surface
$J_{0e\text{-}pass}$	J_{0e} in the passivated emitter area
J_{sc}	Short-circuit current density
LCOE	Levelized cost of electricity
LID	Light induced degradation
n^+	Heavily phosphorus doped
n_i	Intrinsic carrier concentration
NAO	Nitric acid grown oxide
P	Phosphorus
p^+	Heavily boron doped
PC1D	Name of one-dimensional device simulation program
PECVD	Plasma enhanced chemical vapor deposition
PERL	Passivated emitter and rear locally-diffused
PERT	Passivated emitter, rear totally-diffused
PV	Photovoltaics
PVD	Physical vapor deposition
QSSPC	Quasi-steady state photoconductance

R_s	Series resistance
R_{sh}	Shunt resistance
S	Surface recombination velocity
Si	Silicon
SIMS	Secondary ion mass spectroscopy
SiN_x	Silicon nitride
SiO_2	Silicon oxide
SRH	Shockley-Read-Hall
STEM	Scanning transmission electron microscopy
TEM	Transmission electron microscopy
UV	Utraviolet
Δn	Injection level
η	Energy conversion efficiency
τ_{bulk}	Bulk lifetime
τ_{eff}	Effective minority carrier lifetime

SUMMARY

Photovoltaics (PV) is one of the most promising candidate for sustainable energy source because sunlight is free, essentially unlimited, and not localized in any part of the world. In addition, PV is environmentally friendly and a non-polluting energy source. Even though levelized cost of electricity (LCOE) from PV has come down by a factor of five since 1998, PV accounts for only less than 0.2% of total energy consumed in United States due to a higher LCOE (~$0.15/kWh) compared to fossil fuel (≤$0.1/kWh). Therefore, it is necessary to further reduce the cost of modules as well as balance of system (BOS) to attain grid parity for mass adoption of PV.

The PV module price can be reduced by reducing module material and manufacturing cost and by increasing solar cell efficiency. Solar cell efficiency is the most effective way to reduce the PV system cost because higher efficiency not only reduces the amount of material and the number of cells or modules required to produce a given power but also it reduces the BOS cost by shrinking the footprint of the PV system. Since n-type Si has the potential for higher stabilized efficiency, the overall objective of this thesis is to produce ~ 21% n-type manufacturable PERT (**p**assivated **e**mitter, **r**ear **t**otally-diffused) Si solar cells at low-cost. However, there are several challenges that need to be overcome in order to accomplish this goal. The challenges provided the motivation to explore various B diffusion technologies in this thesis and develop process and dielectric stack combination to passivate its surface to minimize boron emitter recombination. In addition, a detailed study of the BRL layer is conducted to understand its role and mitigate or eliminate its negative impact on surface passivation and bulk lifetime. Finally, optimization of cell design and technology development is carried out using production tools to achieve

commercial ready cell efficiencies approaching 21% on large area (239 cm^2) commercial grade n-type Cz Si wafers.

Chapter 2 deals with the fundamental physics and the optical/electrical loss mechanisms of the solar cells. In chapter 3, the various technologies used for cell processing were reviewed. Also, various n-type Si solar cell concepts in the literature were reviewed. This research focused on development of low-cost and high-efficiency n-type PERT cells using commercially viable technologies.

In chapter 4, at the start of this research, J_{0e} of the inkjet-printed B emitter was studied by a combination of simulation and measurement. The boron-doped emitters with sheet resistance in the range of 60-120Ω/sq were formed by inkjet printing of liquid boron source followed by annealing in the temperature range of 900℃ to 950℃. All the doping profiles showed very high near surface doping concentration of $\geq 1x10^{21}$ cm^{-3} due to the formation of undesirable BRL. SiN_x passivated inkjet-printed B emitters with the BRL gave very high J_{0e} values (> 400fA/cm^2). However, when the BRL was completely removed by a thermal oxidation process followed by HF dip, J_{0e} value decreased by a factor of two to ~ 198fA/cm^2 but was still short of the J_{0e} target of ≤80fA/cm^2. It was found that SiO_2/SiN_x stack passivation after the BRL removal reduced the J_{0e} value to ~100fA/cm^2 which is close to the target value of 80fA/cm^2 for 21% efficient n-type PERT cells.

In chapter 5, process-induced bulk lifetime in n-type Si wafers was studied, because the bulk lifetime in finished device is very important for solar cell efficiency. Model calculations were performed to establish base resistivity and bulk lifetime requirements to achieve 21% cells. A 5Ω•cm n-type Cz Si material was selected in this thesis and the model calculations showed that at least 1ms bulk lifetime should be maintained in the finished

device for achieving ≥21% PERT cells. Process-induced lifetime study using $p^+/n/n^+$ structures on this material showed high bulk lifetime (>1ms) after the B and P co-diffusion in the temperature range of 900 ℃ to 950 ℃ due to phosphorus diffusion-induced effective gettering of impurities. However, a 850 ℃ thermal oxidation after the co-diffusion, used for BRL removal, degraded the bulk lifetime significantly to lower than 500μs. This negates the benefit of good surface passivation or low J_{0e} due to BRL removal. Therefore, an alternative method to the thermal oxidation is developed in the next chapter to remove the BRL which not only gives lower J_{0e}, but also preserves bulk lifetime.

In chapter 6, a chemical etching process was developed to remove the harmful BRL as an alternative to the thermal oxidation which leads to unwanted bulk lifetime degradation. In addition, this chapter showed a positive synergistic effect of passivating the BRL-free boron emitter surface with nitric acid-grown oxide (NAO) capped with PECVD SiN_x. The combination of chemical etching and NAO/SiN_x passivation resulted in low $J_{0e\text{-}pass}$ of 100fA/cm^2 without the degradation in bulk lifetime. This resulted in a large area (239 cm^2) n-type Cz Si solar cell with 19.0% conversion efficiency, compared to the 17.4% cells at the start of this research with the BRL and SiN_x passivation. Remainder of the thesis will focus on fundamental research and technology innovation to achieve the efficiency target of 21%.

In chapter 7, By developing technologies and optimizing solar cell fabrication process involving dual annealing for B and P dopants, rear surface planarization, and chemical etching for BRL removal, greater than 20% efficient n-type PERT cells with screen-printed contacts were achieved on commercial grade 239 cm^2 n-type Cz Si wafers. This represents over 1% (absolute) efficiency enhancement over the single anneal process

developed in chapter 6 which resulted in 19% efficiency. In addition, for B emitter formation, spin coating, screen printing, ion-implantation, and APCVD technologies were utilized and compared in this chapter. The etching process for the BRL removal was optimized for each technology. It was found that the maximum cell efficiency is achieved when only the BRL is etched away. Under etching the BRL results in inferior surface passivation, V_{oc} and J_{sc} while over etching degrades cell efficiency due to increase in R_s and n-factor. Due to different BRL thickness, the optimized etching times for spin coating, screen printing, implantation, and APCVD were 30s, 240s, 120s, and 180s, respectively. The corresponding best efficiencies were 20.0%, 20.2%, 20.2%, and 20.2%. This chapter also shows nearly the same efficiency potential of the four B diffusion technologies for high efficiency commercial-ready n-type PERT solar cells up to the efficiency of 20%. However, more research needs to be done to drive this efficiency toward 21%. Ion-implanted cell technology is selected in the next chapter to achieve 21% efficiency through device modeling and further technology enhancements.

Chapter 8 focused on advanced metallization on the front and back through technology development and design optimization for higher efficiency cells. Advanced metallization involved three enhancements : i) optimization of front grid design with five busbars to increase FF, ii) laser opening and PVD Al to reduce rear contact recombination, and iii) introduction of floating busbars. The front grid pattern was optimized using an analytical model, which revealed 5 busbars with 100 gridlines can provide 0.33% increase in absolute efficiency. Fabrication of 5 busbar cells raised the efficiency from 20.1% to 20.4%. Second technology enhancement involved replacing the 120μm wide 500μm apart screen printed metal dots on the rear surface with laser opening of a 40μm dot pattern with

300μm spacing followed by PVD Al metallization. This reduced the back metal/Si contact area from 4.5% to 1.4%, resulting in higher V_{oc} and another 0.36% increase in efficiency. Best cell efficiency with this technology enhancement was 20.86%. Finally, floating busbars were applied on the front to reduce the front metal/Si contact area from 7.5% to 4.5%. This did give another 4mV increase in V_{oc} but the cell efficiency did not increase because of the slightly lower FF due to the inferior busbar/gird contact resistance. Improved floating busbar paste can overcome this and provide ~21% cells.

In chapter 9, by developing and integrating several efficiency enhancement features, 20.84% efficient nPERT cell was achieved on commercial grade 239 cm^2 n-type Cz Si wafers. The technology developments involved chemical etching of BRL to improve emitter surface passivation and bulk lifetime, separate annealing of B emitter and P BSF to optimize diffused regions for lower J_0, rear side planarization for lower surface recombination and higher back reflectance, optimized grid pattern with 5 busbars for lower series resistance and higher fill factor, laser opening and PVD Al for rear contact metallization to reduce metal coverage and improve J_{0b} and V_{oc}. Floating busbar technology showed ~4mV increase in V_{oc}, but efficiency enhancement was not seen due to high bus and grid contact resistance. All these technology enhancements provided a 3.44% absolute increase in efficiency over the 17.4% efficient nPERT cell at the start of this research, resulting in 20.84% efficiency.

Lastly, chapter 10 suggests research directions to improve cell efficiency further and attain ≥21% efficient n-type PERT solar cells which involve two additional technology developments including the use of selective emitters and negatively charged aluminum

oxide (Al_2O_3) film for boron emitter surface passivation. These innovative technologies will raise cell efficiency further from 20.8 to 21.1%.

Chapter 1 : INTRODUCTION

1.1 Statement of the Problem

Historically, the fossil fuels such as gas, coal, oil have been the dominant resource for world energy supply. The consumption of the fossil fuels has been increasing steadily to satisfy growing world energy demand as shown in Figure 1.1. During the last 25 years, gas consumption has increased by over 80%, coal consumption by over 70%, and oil consumption by over 30%. However, this balance could change in the coming decades because fossil fuels are not only limited in supply but also cause detrimental impact on the environment through the emission of global warming gases (Figure 1.1).

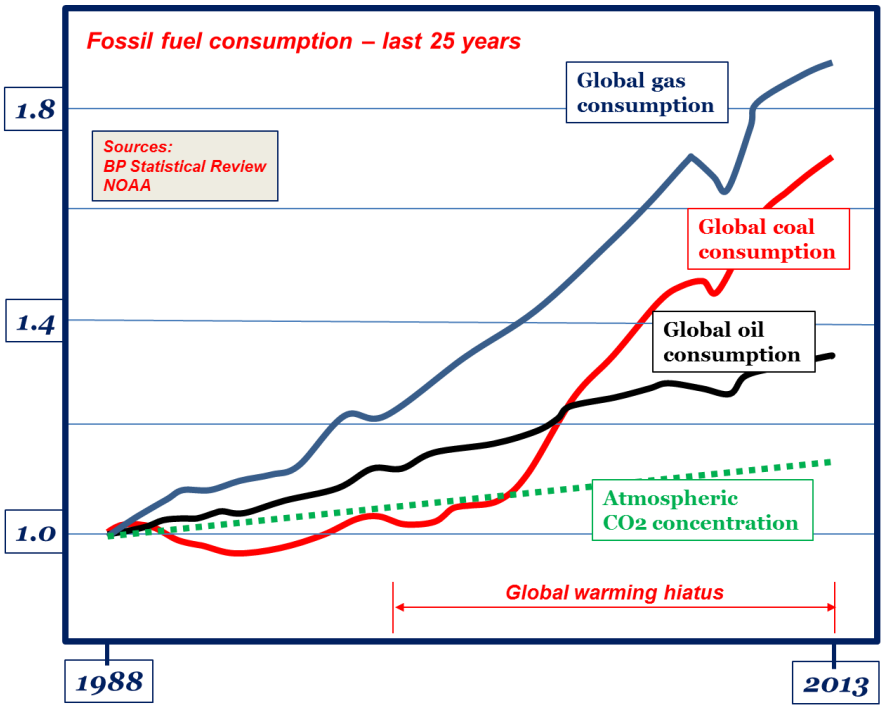


Figure 1.1 Fossil fuel consumption and carbon dioxide (CO_2) concentration in the air.

Nuclear energy has also attracted considerable interest as a substitute for the fossil fuels due to lower cost and clean production of electricity. However, nuclear energy raises

concerns about safety and radioactive waste disposal. In addition, it takes long time to build a nuclear plant, so it cannot fulfill the rapidly rising demand for energy. Therefore, a clean energy source needs to be developed to reduce the dependence on fossil fuels and nuclear energy.

Photovoltaics (PV) is one of the most promising candidate for sustainable energy source because sunlight is free, essentially unlimited, and not localized in any part of the world. In addition, PV is environmentally friendly and a non-polluting energy source. Even though levelized cost of electricity (LCOE) from PV has come down by a factor of five since 1998, PV accounts for only less than 0.2% of total energy consumed in United States as shown in Figure 1.2 [1] due to a higher LCOE (~$0.15/kWh) compared to fossil fuel (≤$0.1/kWh). Therefore, it is necessary to further reduce the cost of modules as well as balance of system (BOS) to attain grid parity for mass adoption of PV.

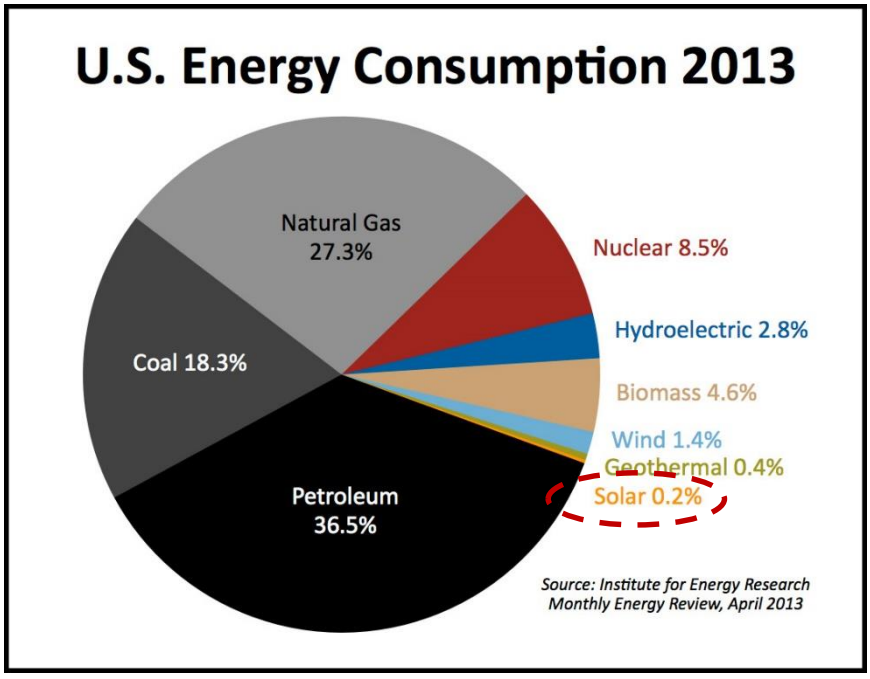


Figure 1.2 United States energy consumption in 2013

The PV module price can be reduced by reducing module material and manufacturing cost and by increasing solar cell efficiency. Solar cell efficiency is the most effective way to reduce the PV system cost because higher efficiency not only reduces the amount of material and the number of cells or modules required to produce a given power but also it reduces the BOS cost by shrinking the footprint of the PV system. LCOE contours in Figure 1.3, calculated by using the reasonable technical and financial inputs, reveal that the grid parity at ~ $0.1/kWh, which is average retail price of electricity in U.S., can be reached by increasing current Si PV module efficiencies from 15.0-16.5% to ≥19.0% while simultaneously reducing the current module cost from ~$0.80/W to < $0.50/W. Since cell-to-module conversion results in an efficiency loss of about 10-15% relative (2.0-2.5% absolute) [2], the corresponding cell efficiency needs to be ≥21%. This requirement established the overall goal for this thesis. It is important to note that Figure 1.3 assumed a total BOS cost of $2/W, which is close to the current situation in the U.S. for residential commercial PV system. However, if the BOS drops to $0.75/W, which is the DOE target, then ≥21% cells at ≤$0.50/W can reach the global grid parity at ¢10/kWh.

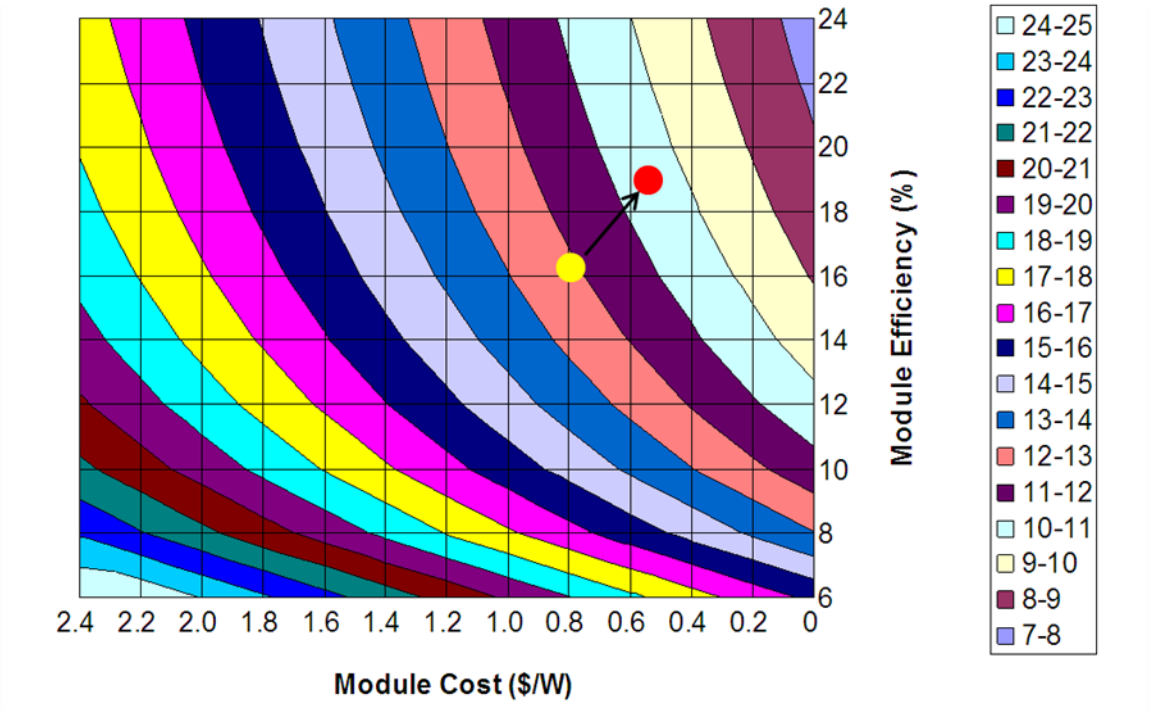


Figure 1.3 LCOE contour plot for Atlanta area as a function of module cost and module efficiency with a BOS cost of $2/W. Assumption for the chart :25 year lifetime: 20% derated: 7.69% WACC, No ITC, 50% debt fraction, 7% loan rate, and 5 year loan term.

1.2 Motivation

Silicon (Si) solar cells have been the workhorse of PV industry since their inception in 1956 at Bell laboratory. Si accounts for almost 90% of the PV modules shipped today. About 84% of PV module production is currently based on p-type crystalline silicon, while the n-type crystalline Si has a market share of only 4% as shown in Figure 1.4 [3].

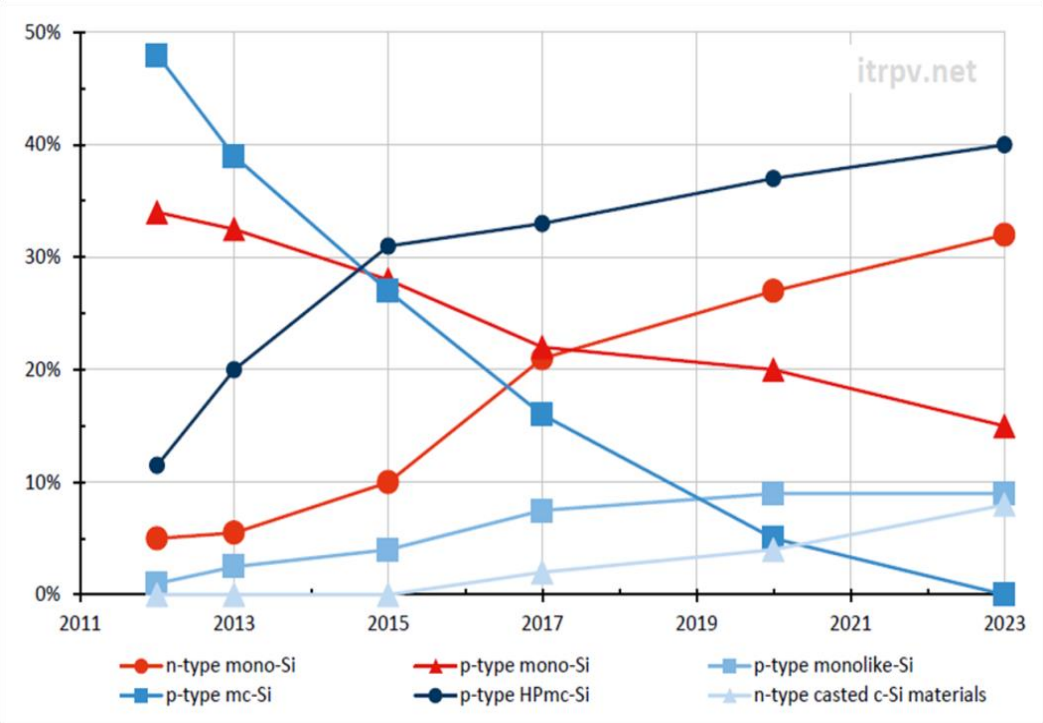


Figure 1.4 Predicted increase in the market share of n-type mono-Si solar cells.

This is because, until 1980s, PV was mostly used for space applications where p-type Si is more durable because it is more tolerant to high energy particle radiation in space. However, since then, many researchers have studied n-type Si for PV and confirmed its superior electrical properties compared to the p-type Si. The first positive attribute of n-type Si is that it is less sensitive to the harmful metallic impurities, such as interstitial Fe (Fe_i), which are usually present in the feedstock Si or introduced during cell manufacturing. These impurities can degrade bulk lifetime and cell performance by forming Shockley-Read-Hall (SRH) recombination centers. Note that the minority carriers in n-type Si are holes instead of electrons. Figure 1.5 shows that harmful impurities have higher capture cross section for electron than hole ($\sigma_n/\sigma_p > 1$). Therefore, they hurt the bulk lifetime in p-type Si more than n-type Si [4].

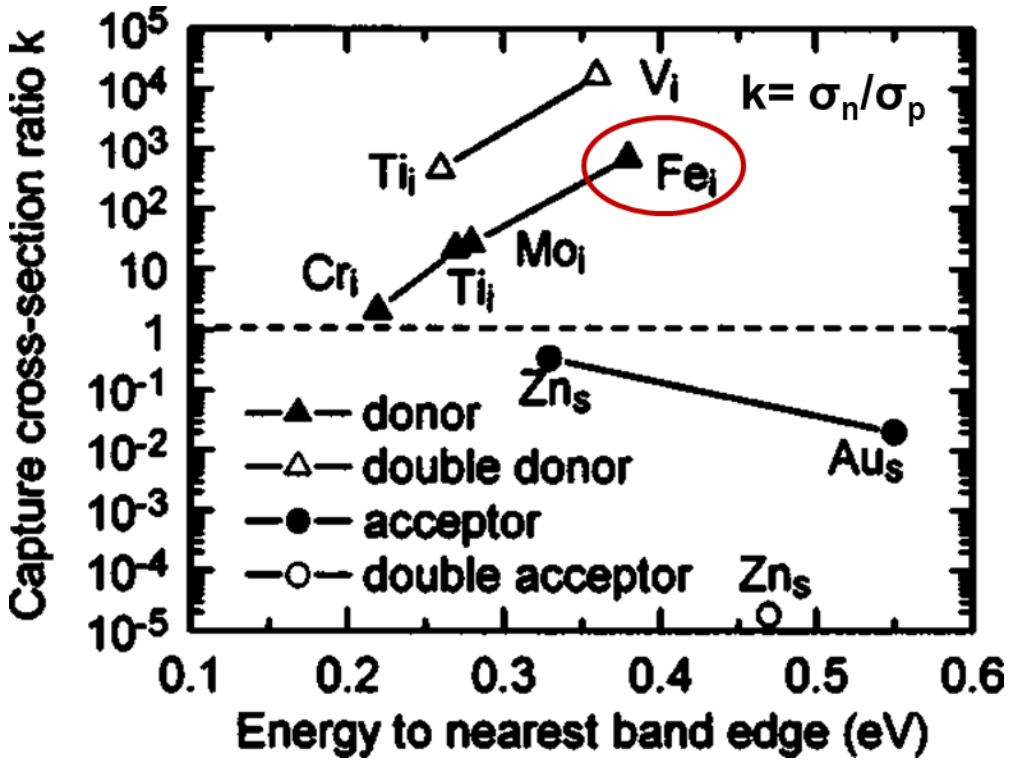


Figure 1.5 Capture cross-section of metal impurities.

Therefore, n-type Si generally has higher bulk lifetime than p-type Si for the same impurity concentration which provides opportunity for achieving higher cell efficiency. Secondly, due to absence of boron, n-type Si does not suffer from light induced degradation (LID) which can cause reduction in 0.5~1% absolute cell efficiency [5-7]. The LID is ascribed to boron-oxygen (B-O) defects which are formed by prolonged light exposure (≥24 hours) of boron-doped p-type Si.

As a consequence of above attributes and the need for higher efficiency cells for low-cost PV, n-type Si has recently attracted considerable attention for high efficiency solar cells, including the development of industrial tools and technologies for commercializing n-type Si cells. Therefore, it is not surprising that the international PV

roadmap in Figure 1.4 predicts that the n-type monocrystalline Si market share may reach 30% by 2015 and over 60% by 2020, compared to 6% in 2012 [8]. This potential of n-type Si for high efficiency without LID provided the motivation in this thesis to develop low-cost high-efficiency commercial ready n-type Si solar cells with efficiency $\geq$ 21% in an attempt to approach grid parity.

1.3 Thesis Objectives

Low-cost high efficiency is the key to reducing cost of PV system. Since n-type Si has the potential for higher stabilized efficiency, the overall objective of this thesis is to produce ~ 21% n-type manufacturable PERT (**p**assivated **e**mitter, **r**ear **t**otally-diffused) Si solar cells at low-cost. However, there are several challenges that need to be overcome in order to accomplish this goal. Most essential process for n-type solar cells is the formation of single-side boron emitter with low-cost, high throughput, and high quality. In addition, it is challenging to attain high quality boron (B) emitter surface passivation and maintain high bulk lifetime due to the formation of boron-rich layer (BRL) on top of the boron emitter after the boron diffusion. The BRL interferes with surface passivation and can cause lifetime degradation because of inactive boron, segregated metal impurities, and structural defects in the BRL. Furthermore, widely used PECVD SiN_x layer for anti-reflection coating and passivation of phosphorus doped n^+ emitter in p-base devices does not work well for boron emitters.

The above challenges provided the motivation to explore various B diffusion technologies in this thesis and develop process and dielectric stack combination to passivate its surface to minimize boron emitter recombination. In addition, a detailed study

of the BRL layer is conducted to understand its role and mitigate or eliminate its negative impact on surface passivation and bulk lifetime. Finally, optimization of cell design and technology development is carried out using production tools to achieve commercial ready cell efficiencies approaching 21% on large area (239 cm^2) commercial grade n-type Cz Si wafers.

The overall goal of fabricating commercial ready low-cost high-efficiency (~21%) n-type PERT Si solar cells, shown in Figure 1.6, will be achieved through following 6 tasks in this thesis.

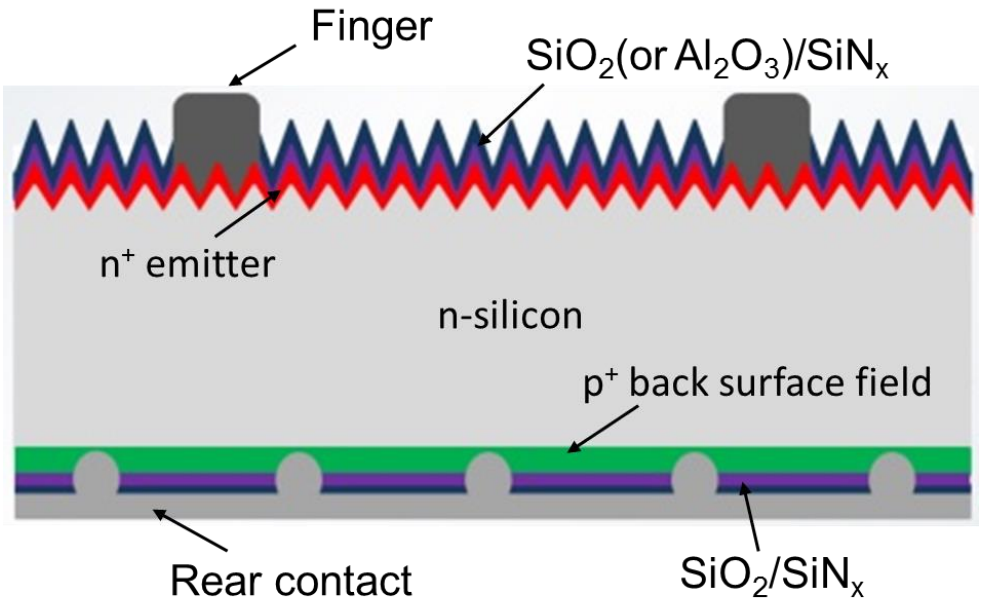


Figure 1.6 Structure of a screen-printed PERT n-type Si solar cell.

Task 1: Investigation and Development of a Novel Boron-doped Emitter Formed by Inkjet Printing and its Surface Passivation Properties.

The formation of high quality boron emitter is required for achieving high efficiency n-type solar cells. In this section, a novel inkjet printing technology is used at

the beginning to form B emitter because of its potential for low cost and suitability in photovoltaic manufacturing. Technology development involves formation of inkjet boron emitters using appropriate B doping pastes and optimized annealing condition. Doping profiles and reverse saturation current density (J_{0e}) are determined for various inkjet-printed B emitters to select the optimized B emitter for high efficiency n-type cells. In addition, various emitter surface passivating dielectrics are evaluated to minimize J_{0e}, while maintaining appropriate sheet resistance and antireflection coating. Finally, formation of BRL in the inkjet B emitters and its impact on surface passivation are studied.

Task 2: Investigation and Understanding of Process-induced Bulk Lifetime in N-type Silicon Wafers.

Since bulk lifetime (τ_{bulk}) in n-type Si is key to achieving high efficiency n-type Si solar cells, process-induced bulk lifetime of n-type Si wafer is investigated prior to cell fabrication. This study includes development of boron diffusion, phosphorus diffusion, and thermal oxidation processes to attain bulk lifetime in excess of 1 ms, required for high efficiency n-type cells. In addition, process conditions are tailored to maintain manufacturability of PERT devices.

Task 3: Development of a Rapid Chemical Etching Process for BRL Removal and Subsequent Surface Passivation for High Bulk Lifetime, Low J_{0e}, and High Efficiency.

Most of the processes currently used in industry for the B emitter formation result in an unintentional supersaturated boron-rich layer (BRL) on top of the B emitter. It has been conjectured that the BRL acts as high recombination site due to inactive boron,

segregated metal impurities, and structural defects. It can also interfere with the emitter surface passivation. For this reason, either BRL formation needs to be prevented or the BRL needs to be removed during cell processing to achieve high efficiency. Therefore, in this task, first a fundamental understanding of the formation and impact of BRL is established. Then methods for BRL removal are explored, without hurting the emitter, to attain low J_{0e} and high τ_{bulk}. These techniques are integrated in the cell process sequence to fabricate manufacturable high efficient n-type PERT solar cells. Finally, the effectiveness of the BRL removal process is validated by transmission electron microscopy (TEM) and auger electron spectroscopy (AES), and J_{0e} measurement.

Task 4: Technology Development and Fabrication of High Efficiency N-type Commercial Size Silicon Solar Cells with Four Promising B Emitter Technologies.

Four commercially viable B diffusion techniques are investigated in this task as an alternative to the conventionally-used BBr_3 tube diffusion and the novel inkjet printed B emitter. The proposed techniques will involve spin coating, screen printing, ion-implantation, and atmospheric pressure chemical vapor deposition (APCVD) of B source. First, the impact of each boron technology on cell efficiency is explored by fabricating n-type PERT solar cells using the same process sequence. Then, the process sequence is optimized for each B diffusion technology to attain highest efficiency n-type PERT cell.

Task 5: Technology Development and Optimization of Metallization for Achieving ~21% Efficient N-type PERT Cell.

Fill factor (FF) is one of key parameters to achieve high cell efficiency. The FF is affected by total series resistance (R_s) of the cell which consists of several components. These components are first analyzed for ion-implanted n-type PERT solar cell for the reference. The various components of R_s are calculated for different spacing and number of fingers and busbars using the analytical modeling. Using these predetermined R_s values from the modeling, optimized front grid design for producing a maximum cell efficiency is selected. In addition, sputtering of aluminum by physical vapor deposition (PVD) in combination with laser opening of dielectric stack is used on the rear side for metal contacts to reduce the contact area. This concept replaces the existing rear contacts formed by screen-printed and fire-through silver (Ag) dots followed by screen-printing low temperature cured Ag paste. Compared to the screen-printed rear contacts, the PVD Al metallization provides less metal contact fraction on the rear side and narrower point contact pitch. This lowers metal-induced recombination as well as lateral resistance from the rear side. These optimizations and improvements in metallization are implemented in full cell and benefits on J_{0e} and FF are quantified. Finally, the floating busbar is applied for a further improvement. The floating busbars make no direct contact with Si emitter and reside just on top of the anti-reflection coating. Therefore, this reduces the recombination further and hence give an added boost in V_{oc}.

Task 6: Quantitative Understanding of Impact of Each Technology Enhancement on Cell Parameters and Efficiency through Detailed Modeling and Characterization.

In this task, all the above fundamental understanding, cell design, and technology developments are integrated into a process sequence to achieve ~21% efficient large area

PERT solar cells on commercial size 239 cm^2 n-type Cz Si wafers. Screen-printed contacts to the boron emitter. Detailed device modeling and cell characterization are used to explain each of the five technology enhancements that led to the increase in PERT cell efficiency from ~17.4% to ~21% in this research. Device modeling is performed using PC1D model and cells are characterized by light and dark *I-V*, IQE, reflectance, J_{0e}, and bulk lifetime measurements.

Chapter 2 : BASIC OPERATION AND FUNDAMENTAL PHYSICS OF SOLAR CFELLS

2.1 Basic Operation and Equivalent Circuit of a Solar Cell

A solar cell is a power generating device which directly converts sunlight into electricity using the photovoltaic effect. The process of converting sunlight into electrical energy consists of the following three essential steps:

(1) Absorption of incident photons generates a large number of electron-hole pairs.

(2) Separation of electron-hole pairs by electric field inside the p-n junction.

(3) Transport of separated charge carriers to an external circuit or load.

The electrons then dissipate its energy in the external circuit or load and return to the solar cell.

Figure 2.1 illustrates a structure of a simple n-type Si solar cell and its basic operation. The n-type Si solar cell involves the formation of a boron-doped (p^+) emitter on the front side (p-n junction), diffusion of phosphorus-doped (n^+) back surface field (BSF) on the rear side, deposition of a silicon nitride (SiN_x) film on front and back for passivation and anti-reflection coating (ARC) on the emitter and passivation of the BSF surface, and screen-printed metallization for contacts. The boron emitter forms a p-n junction creating internal electric field in the depletion region. The light-generated electrons and holes are separated and swept across the junction by the internal electric field. The back surface filed (BSF) consists of a heavily phosphorus-doped (n^+) region on the rear surface of the n-type solar cell. The high-low region (n+/n) generates an electric field at the interface that serves as a barrier for minority carrier flow to the rear contact [9]. The BSF reduces back surface recombination by reflecting the holes back into the base. The SiN_x is frequently used for

Si surface passivation as well as ARC in PV industry. The SiN_x lowers surface recombination by reducing the number of dangling bonds at the Si surface and by providing field induced passivation via its built-in positive charge. In addition, it reduces the reflection from the front cell surface which raises the absorption of the incident light into the cell. Lastly, the front and back contacts on most commercial solar cells are formed by screen-printing technology because of its simplicity, high throughput, and low manufacturing cost. The cell efficiency can be improved significantly by avoiding the recombination of the generated carriers at the front and back surfaces, in the heavily doped emitter and BSF regions, and in the bulk. The importance of surface, emitter and bulk recombination will be quantified by device modeling to provide guidelines for technology development and optimized cell design.

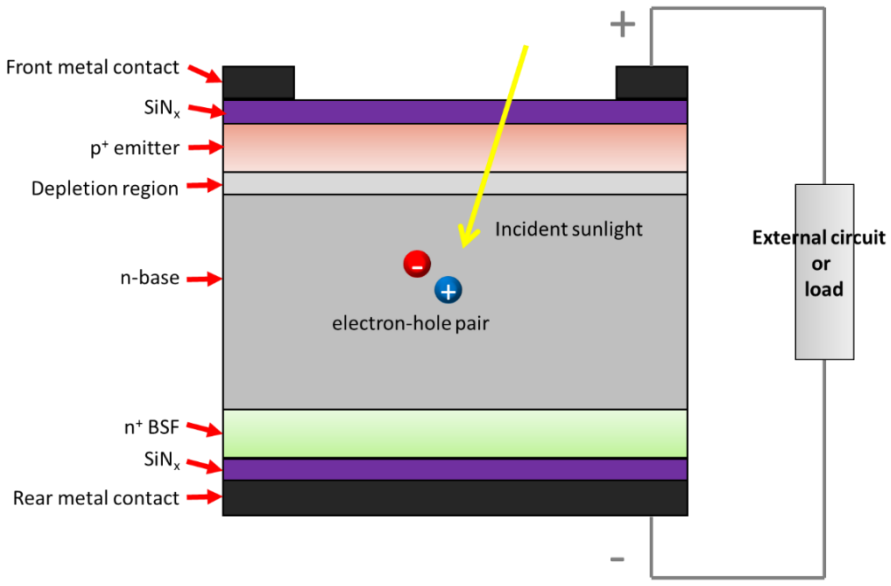


Figure 2.1 A structure of a simple n-type Si solar cell and its basic operation.

The basic structure of a Si solar cell can be modeled by a circuit with a current source (I_{light}) connected in parallel with two diodes (I_{01} & I_{02}), series resistance (R_s), and shunt resistance (R_{sh}) as illustrated in Figure 2.2. These diodes are characterized by their reverse saturation current I_{01} and I_{02}. I_{01} represents the recombination in the base and emitter of the solar cell, and I_{02} represents the recombination in the space charge region of the solar cell. The series resistance is composed of bulk, sheet, contact, grid, and busbar resistances. The shunt resistance is the leakage path of the current through a solar cells via parasitic shunting.

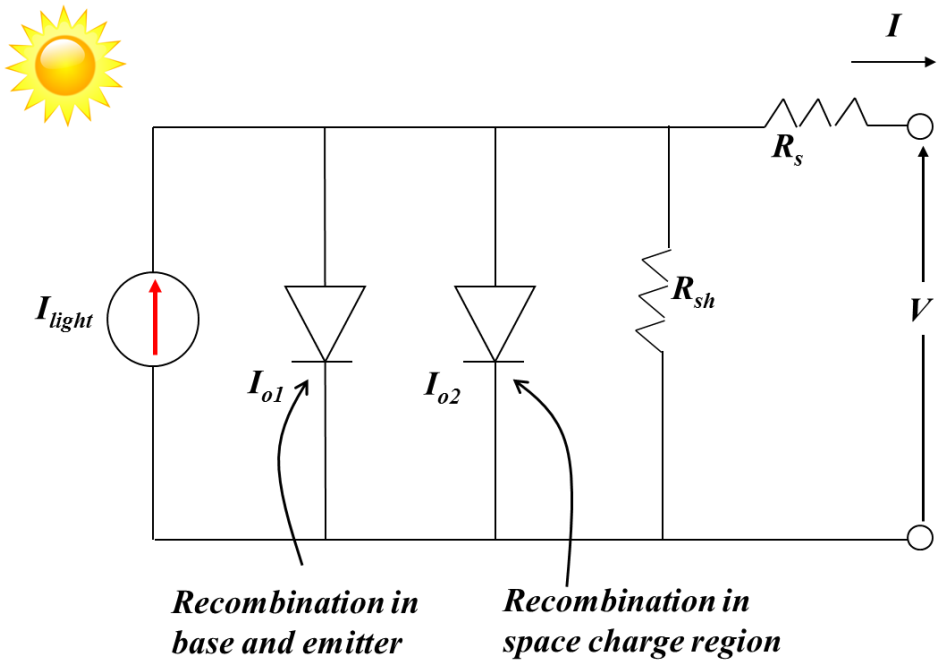


Figure 2.2 Equivalent circuit of a p-n junction solar cell.

2.2 Solar Cell Parameters

As explained in Chapter 2.1, a solar cell is a device which converts the incident sunlight into electrical energy. The conversion efficiency is the most important parameter

to characterize the performance of a solar cell. The cell efficiency is defined as the ratio of electrical power output (P_{out}) to the incident photon power (P_{in}) as shown in Figure 2.3 [10].

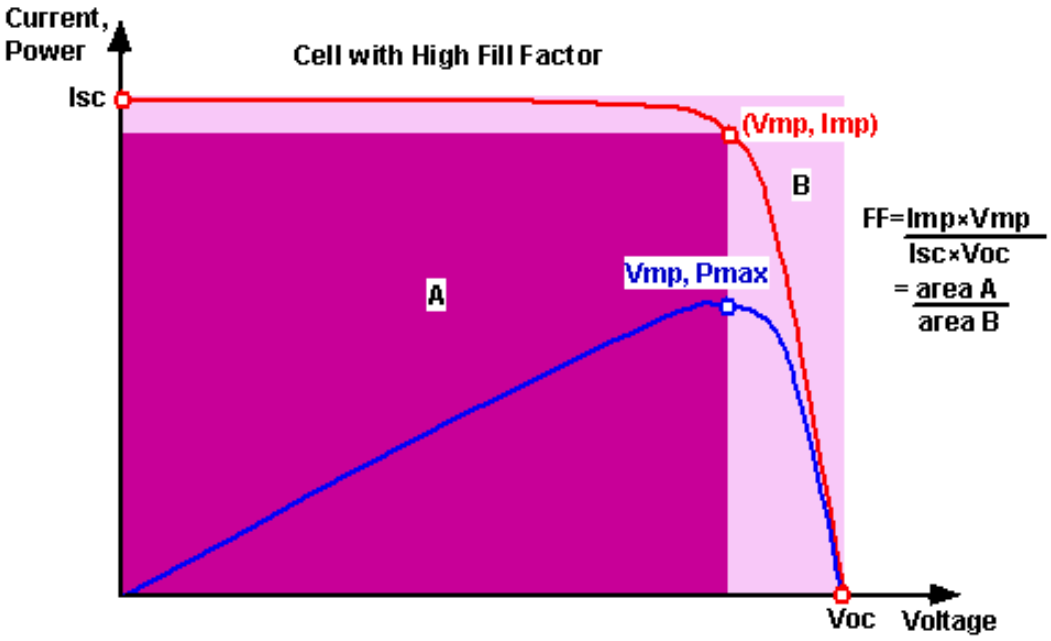


Figure 2.3 I-V characteristics of a solar cell.

The conversion efficiency (η) is expressed as [11]

$$E_{ff}(\eta) = \frac{P_{out}}{P_{in}} = \frac{V_{mp} \cdot I_{mp}}{P_{in}} = \frac{V_{oc} \cdot I_{sc} \cdot FF}{P_{in}} \tag{2.1}$$

where V_{mp} and I_{mp} are the voltage and current at maximum power point (P_{max}) and P_{in} is 100mW/cm^2 for standard test conditions (STC).

Fill factor (*FF*) is a measure of "squareness" of the I-V curve as illustrated in Figure 2.3. It is defined as the ratio of the maximum power output of a solar cell (area A) to the product of V_{oc} and I_{sc} (area B). The FF is expressed as

$$FF = \frac{V_{mp} \cdot I_{mp}}{V_{oc} \cdot I_{sc}} = \frac{area\_A}{area\_B} \tag{2.2}$$

FF can be also expressed by an empirical equation below:

$$FF = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \tag{2.3}$$

where the v_{oc} is the "normalized V_{oc}" is defined as a following equation

$$v_{oc} = \frac{q}{nkT} V_{oc} \tag{2.4}$$

where q is the electronic charge, n is the ideality factor, k is Boltzmann constant, and T is temperature.

Open circuit voltage *(V_{oc})* is the maximum voltage that the solar cell can generate. V_{oc} is expressed as

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{sc}}{I_o} + 1\right) \tag{2.5}$$

The I_o is a reverse saturation current of a finite dimension p-n junction diode and is expressed by following equations [11, 12]

$$I_o = I_{oe} + I_{ob} = A\left(\frac{qD_e n_i^2}{L_e N_A} \cdot F_P + \frac{qD_h n_i^2}{L_h N_D} \cdot F_N\right) = A\left(\frac{qn_i^2}{N_A} \cdot S_{eje} + \frac{qn_i^2}{N_D} \cdot S_{ejb}\right) \tag{2.6}$$

$$F_P = \frac{S_e \cosh(W_P / L_e) + D_e / L_e \sinh(W_P / L_e)}{D_e / L_e \cosh(W_P / L_e) + S_e \sinh(W_P / L_e)} \tag{2.7}$$

$$F_N = \frac{S_h \cosh(W_N / L_h) + D_h / L_h \sinh(W_N / L_h)}{D_h / L_h \cosh(W_N / L_h) + S_h \sinh(W_N / L_h)} \tag{2.8}$$

where S_h and S_e are hole and electron surface recombination velocities, respectively; W_P and W_N are the thickness of the emitter and the base, respectively. F_N and F_P are called

geometry factors. It is interesting note that if front and back surfaces have high recombination velocity (S_h and $S_e \approx \infty$), F_N and F_P can be expressed as :

$$F_N = \coth\left(\frac{W_N}{L_h}\right),\ F_P = \coth\left(\frac{W_P}{L_e}\right) \tag{2.8}$$

On the other hand, if front and back surfaces have very low recombination velocity (S_h and $S_e \approx 0$), F_N and F_P can be reduced to :

$$F_N = \tanh\left(\frac{W_N}{L_h}\right),\ F_P = \tanh\left(\frac{W_P}{L_e}\right) \tag{2.9}$$

The emitter saturation current (I_{0e}) is the recombination current at the junction edge on the emitter side and accounts for the recombination at the front surface and in the bulk of the emitter. The base saturation current (I_{0b}) is the recombination current at the depletion edge on the base side which accounts for bulk and rear surface recombination.

As defined in Equation (2.5), the V_{oc} depends on the short circuit current (I_{sc}) and reverse saturation current (I_0=I_{0e}+I_{0b}) of the solar cell. Thus, V_{oc} is a measure of the amount of recombination in a solar cell. I_{sc} typically has a small variation, the I_o may vary by orders of magnitude.

Shor circuit current (I_{sc}) is expressed as

$$I_{sc} = \int_{E_g}^{\infty} q \cdot N_{ph}(\lambda) \cdot EQE(\lambda) d\lambda \tag{2.6}$$

Where E_g (1.1eV) is the bandgap of silicon, N_{ph} is the number of incident photons, λ is the wavelength, and EQE is the external quantum efficiency. The EQE is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given wavelength incident on the solar cell. EQE can be written as following equation

$$EQE(\lambda) = [1 - R(\lambda)] \cdot IQE(\lambda) \tag{2.7}$$

where reflectance (R) is the percentage of the light reflected from the solar cell and IQE is the internal quantum efficiency. The IQE is the ratio of the number of carriers collected by the solar cell to the number of photons of a given wavelength entering the solar cell.

2.3 Losses in Si Solar Cells

The theoretical efficiency for Si solar cells under one sun operation is about 29.3% [13]. However, the maximum cell efficiencies fabricated by Sunpower, Panasonic, and UNSW are currently 25.0~25.5% [14-16]. The difference between the theoretical and the measured efficiency is due to optical and electrical losses as shown in Figure 2.4 [17]. The optical loss is due to the loss of photons which could not generate electron-hole pairs. This loss is due to the front surface reflection, shading, and incomplete absorption. The electrical loss is due to the generated e-h pairs that do not contribute to the cell output power. This loss is attributed to resistances and recombination.

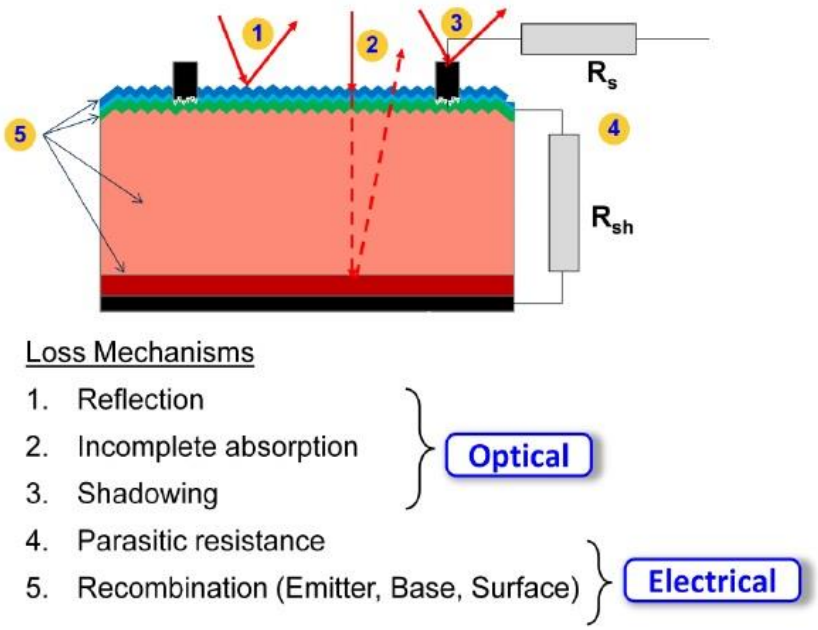


Figure 2.4 Losses in a Si solar cell.

2.3.1 Reflection Loss

The reflection loss is attributed to incident photons that are reflected from the solar cell surfaces. The reflection can be minimized by **anti-reflection coating** (ARC) and **surface texturing**.

(1) Anti-reflection coating (ARC) : ARC is formed by a thin dielectric material on the Si surface to reduce the reflection of incident light via destructive interference of the waves reflected from the top and bottom surfaces of the dielectric (Figure 2.5). Proper selection of thickness d_1 and refractive index n_1 of the ARC can reduce reflection significantly.

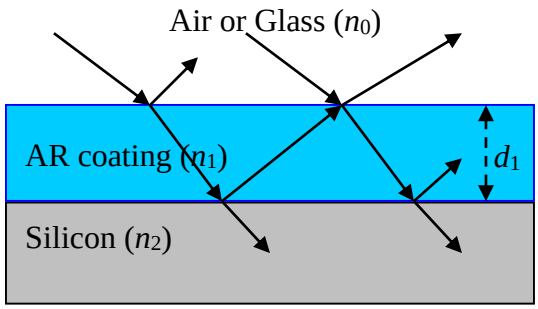


Figure 2.5 Anti-reflection coating to reduce the surface reflection.

For a single layer ARC, the reflectance (R) can be expressed by Fresnel's equation [11, 18].

$$R = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos\theta},\ \theta = \frac{2\pi n_1 d_1}{\lambda},\ r_1 = \frac{n_0 - n_1}{n_0 + n_1},\qquad r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{2.8}$$

where n is the refractive index of a layer. The reflectance has minimum R_{min} when $n_1 d_1 = \lambda/4$ [18] (quarter-wavelength AR coating) and is obtained by :

$$R_{min} = \frac{(n_0 n_2 - n_1^{\,2})^2}{(n_0 n_2 + n_1^{\,2})^2} \tag{2.15}$$

If $n_1 = \sqrt{n_0 n_2}$, R_{min} becomes zero at the desired wavelength $\lambda = 4n_1 d_1$ which can be selected by tailoring the ARC thickness d_1. Since solar spectrum has maximum photon energy at a wavelength (λ) of 630 nm [19], ARC is typically designed to minimize the reflection at 630 nm.

(2) Surface texturing : surface texturing is another effective technique for minimizing reflection. Any roughening of the surface reduces the reflection by increasing the number of bounces as illustrated in Figure 2.6 [20]. Surface texturing can be accomplished by etching along the surfaces of the Si crystal planes <100>. With the surface texturing, the weighted average reflection of the Si surface can be reduced from ~30% to about 11%. The ARC deposition on the textured Si surfaces can reduce this further to within 3%.

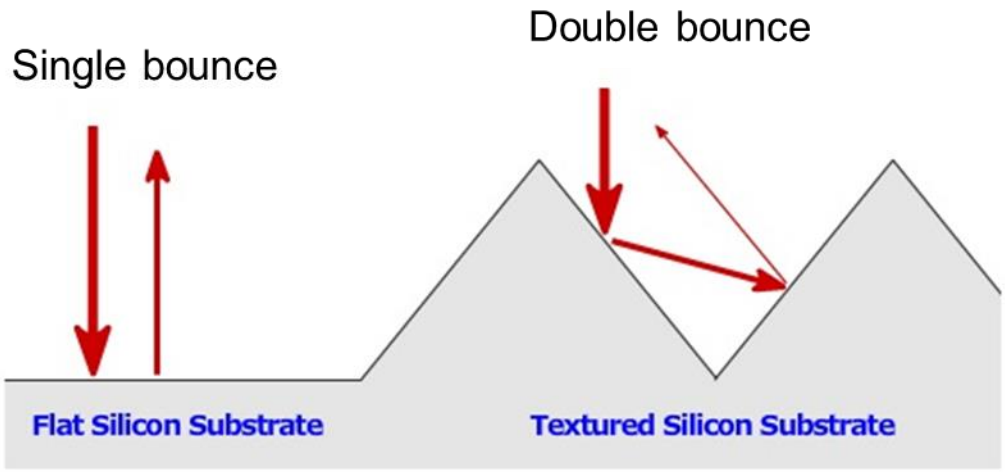


Figure 2.6 Incident light on flat Si surface and textured Si surface.

2.3.2 Shading Loss

A finished solar cell needs to be contacted at the front and back side in order to extract power from the solar cell. However, the front metal contact inhibits the light to enter into the solar cell which reduces I_{light}. This is referred to as the shading loss. Thus, the front contact including fingers and gridlines should cover as small at the front as possible. However, this results in increased resistive losses because carriers have to travel longer distance to be collected by the metal contact. Therefore, grid design has to be optimized in order to balance the shading and resistive losses.

2.3.3 Incomplete Absorption

The loss due to incomplete absorption refers to the loss of photons with energy $E>E_g$ which do not get absorbed in the solar cell due to smaller cell thickness or insufficient optical path length through the cell. This can be minimized by appropriate light trapping that enhances the absorption of long wavelength photons by reflecting them back into the cell from the surfaces.

Light trapping : the light trapping is achieved by changing the angle of incident light so that the rays can travel at certain angle, rather than perpendicular to the surface. This results in increased optical path length as shown in Figure 2.7 [21]. Therefore, the front surface should be textured in order for the rays to meet the surface at an angle. According to Snell's law :

$$n_1 Sin\theta_1 = n_2 Sin\theta_2 \tag{2.16}$$

the total internal reflection can occur at the rear surface if the incident angle is greater than the critical angle. Consequently, the path length can be increased by a combination of front

textured surface and rear reflector design. However, the textured surface leads to increased surface recombination in the cell because of increased interface trap density. Thus, to mitigate the surface recombination, the light trapping should be achieved with a planar rear surface, while keeping the front surface textured, to form a dielectric mirror that reflects light back nto the silicon.

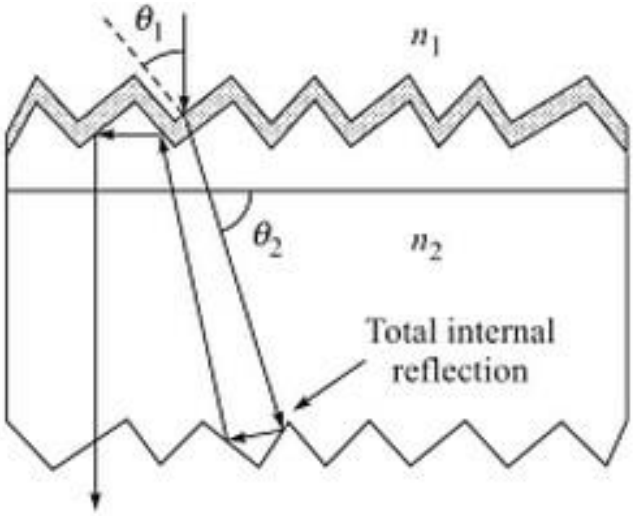


Figure 2.7 Light trapping in solar cell to increase the optical path length.

2.3.4 Resistive Losses

The resistive losses are the result of series (R_s) and shunt resistances (R_{sh}) of a solar cell. These two resistances affect the final FF of solar cell. The following equations show the effect of series and shunt resistances on FF.

$$FF = FF_S[1-\frac{(v_{oc}+0.7)}{v_{oc}}.\frac{FF_S}{r_{SH}}] \tag{2.17}$$

$$FF_S = FF_o(1-r_S) \tag{2.18}$$

$$r_S = \frac{R_{sh}}{R_{CH}},\ R_{CH} = \frac{V_{OC}}{I_{SC}},\ r_{SH} = \frac{R_{sh}}{R_{CH}} \tag{2.19}$$

where FF_o is the ideal FF without R_s and R_{sh} terms as defined in Equation (2.3). Consequently, R_s of a solar cell should be as low as possible and R_{sh} should be as large as possible in order to obtain high FF and efficiency.

The R_{sh} is generally due to process-induced defects that result in partial shunting of the p-n junction and lowering of shunt resistance. This low shunt resistance reduces the amount of photocurrent flowing through the p-n junction and reduces the voltage of the solar cell. Note that R_{sh} is not a design parameter, but the R_s is a design parameter that can be controlled.

The series resistance R_s of a solar cell consists of several components as illustrated in Figure 2.8 [21]. These include resistance of base (R_b), resistance of the emitter (R_e), resistance of the metal-Si interface (contact resistance R_c), and resistance R_{bf} associated with busbars and fingers.

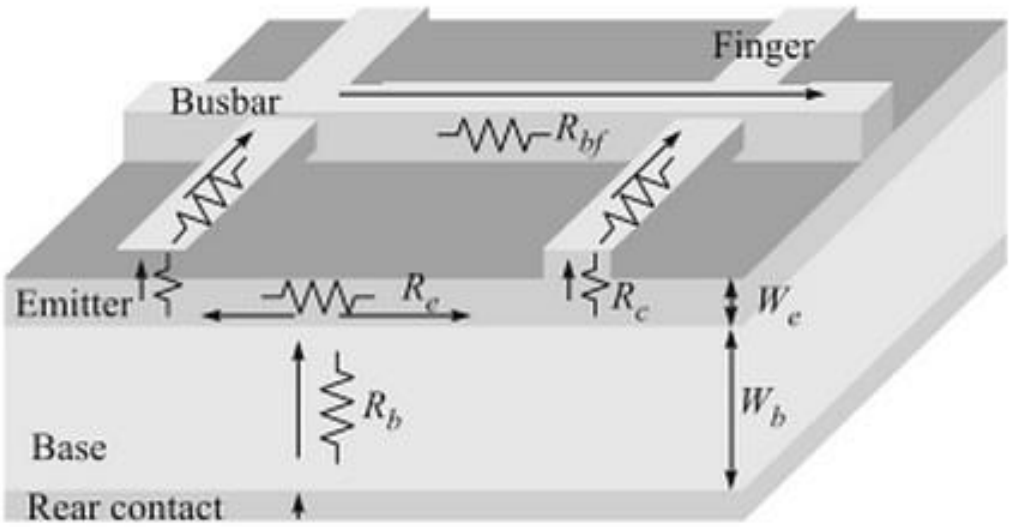


Figure 2.8 Series resistance components in a Si solar cell.

$$R_S = R_b + R_e + R_c + R_{bf} \tag{2.20}$$

Thus, the proper grid and emitter design is very important for lowering R_s and increasing FF and cell efficiency.

2.3.5 Recombination Loss

When illuminated, the generation of electron-hole pair occurs throughout a Si solar cell. The excess carriers return back to reach a thermal equilibrium by recombination of excess electrons and holes. There are four types of recombination processes in a Si solar cell.

1. Radiative recombination
2. Auger recombination
3. Shockley-Read-Hall (SRH) recombination
4. Surface recombination

(1) Radiative (Band-to-Band) recombination : In radiative recombination, an excited electron from the conduction band falls directly back into the valence band. The excited electron releases the energy in the form of a photon (Figure 2.9). The rate of this recombination depends on the number of carriers in the conduction and the number of empty states in the valence band. This recombination process is dominant in direct bandgap semiconductors, but it is not important in indirect bandgap material like Si.

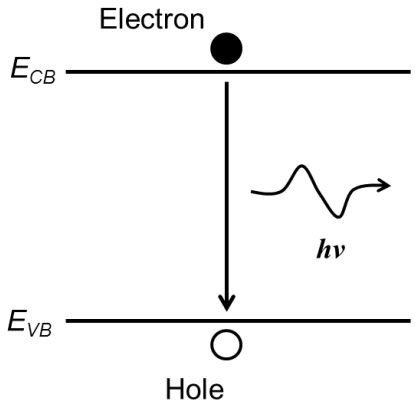


Figure 2.9 Energy band diagram of radiative recombination

(2) Auger recombination : This occurs at high carrier concentrations (> 10^{17} cm^{-3}). As shown in Figure 2.10, when an electron and a hole recombine and give that energy to another electron in the conduction band instead of giving the energy as heat or a photon. The electron that receives the energy goes to a higher energy level and then thermalizes back to the conduction band via scattering.

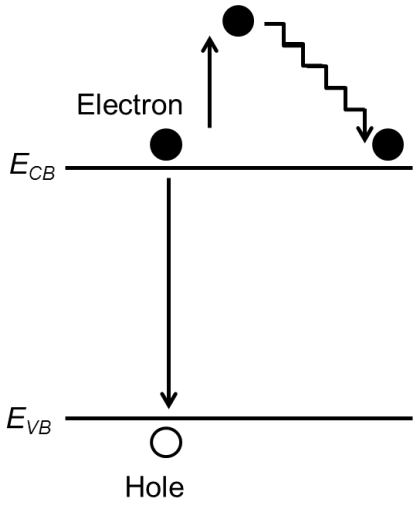


Figure 2.10 Energy band diagram of auger recombination.

(3) **Shockley-Read-Hall (SRH) recombination** : The SRH recombination occurs in material with defects which give rise to energy levels within the band gap. The SRH recombination involves two step processe as illustrated in Figure 2.11. First, an electron (or hole) is trapped by an energy state in the energy level introduced by the defects. If a hole moves up to the same energy state before the electron is re-emitted into the conduction band, it then recombines. The recombination via mid-gap energy levels is very effective in reducing bulk lifetime.

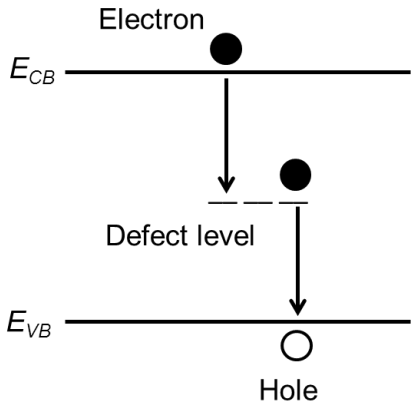


Figure 2.11 Energy band diagram of SRH recombination.

(4) Surface passivation : Si surface presents sudden discontinuity of the crystal arrangement with a large number of dangling bonds which gives rise to deep levels or defect states within the forbidden gap (Figure 2.12) [12, 22]. These bonds act as a recombination site. Thus, both front and rear Si surfaces should be passivated to avoid recombination. In practice, surface recombination can be reduced by two passivation schemes : chemical passivation and field effect passivation.

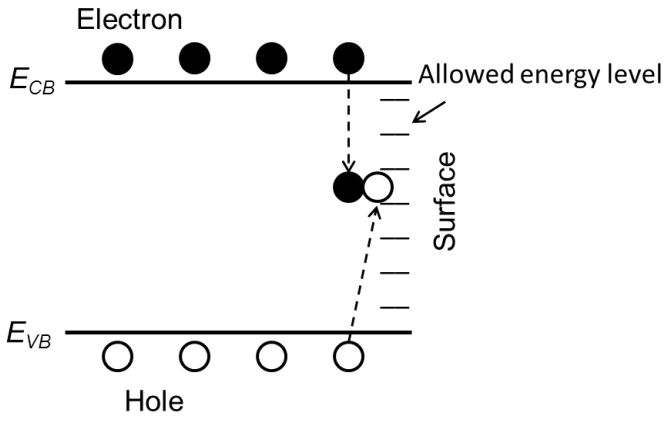


Figure 2.12 Schematic of recombination at Si surface.

The chemical passivation involves deactivating the dangling bonds on the Si surfaces by depositing thin dielectric film that reduces the density of surface states (D_{it}) as shown in Figure 2.13. Thermally-grown silicon dioxide (SiO_2), SiN_x, and aluminum oxide ($Al2O_3$) can be used for this purpose. Right combination of these dielectrics can provide excellent surface passivation for high efficiency.

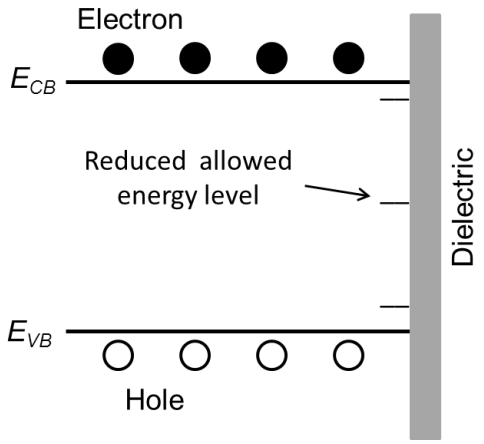


Figure 2.13 Schematic of chemical passivated Si surface.

The field-effect passivation is based on the reduction of either electron or hole concentration at the Si surface by using a built-in electric field. The electric field can induce accumulation or inversion layer by attracting or repelling carriers from the Si surface. This charge accumulation or inversion at the surface lowers recombination because recombination rate is the maximum when the electron and hole concentrations at the Si surface are equal. Accumulation is typically preferred because inversion layer can be shunted by the contact giving rise to parasitic shunt [23]. Negatively charged dielectric (e.g. Al_2O_3) on p-type surface or positively charged dielectric (SiO_2) on n-type surface are desirable because they create accumulation below the silicon surface (Figure 2.14).

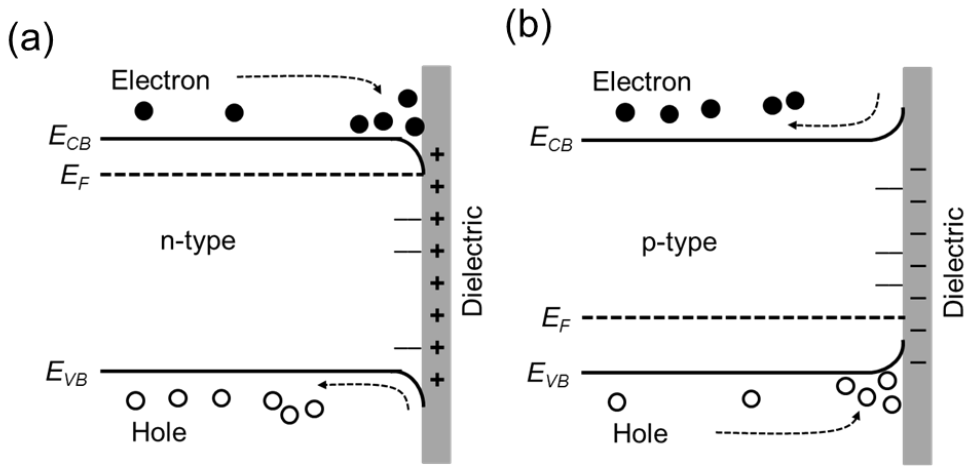


Figure 2.14 Schematic of band diagrams for (a) a positively charged dielectric on n-type Si and (b) a negatively charged dielectric on p-type Si.

Chapter 3 : LITERATURE REVIEW OF N-TYPE SOLAR CELLS

3.1 History of N-type Silicon Solar Cells

The first practical photovoltaic cell was ironically made on phosphorus-doped n-type Si in 1953 at Bell Laboratories by Darly Chapin, Calvin Souther Fuller, and Gerald Pearson, even though most current commercial PV modules today consist of p-type Si solar cells. The first Bell Lab cell efficiency was only 4.5% and increased to 6% in 1954. As shown in Figure 3.1, n-type cell efficiency increased sharply and reached 14.5% by 1961 [24]. With the advent of space program, transition started from n-type to p-type Si cells after 1960 because p-type cells were found to be more radiation tolerant, in spite of lower starting efficiency.

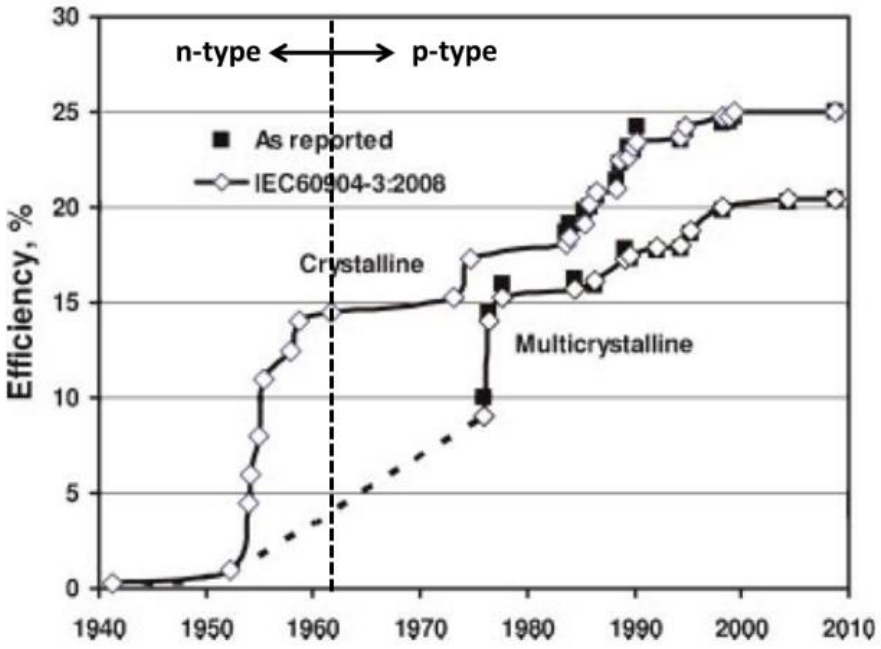


Figure 3.1 Evolution of crystalline and multicrystalline silicon solar cell efficiency.

In early 1970s, efficiencies of p-type Si cells surpassed n-type Si solar cell efficiency of 14.5%. Since then, p-type Si solar cell efficiencies have been constantly improving through technology innovations and cell design optimization. However, as mentioned in Chapter 1.2, p-type Cz Si solar cells suffer from light induced degradation (LID) due to the formation of B-O complex under illumination. These defects form recombination centers to lower bulk lifetime and efficiency. The efficiency loss due to LID could be 0.4-0.6% absolute in basic 18-19% cells today and can even increase significantly in advanced p-type cells with efficiencies exceeding 20% [7]. Because of no LID and superior electrical properties of n-type Si, PV industry is currently trying to shift back to n-type solar cells.

3.2 Investigation of Promising Technologies for Boron Emitter Formation

Low-cost high quality boron (B) emitter formation is critical to the fabrication and commercialization of high efficiency n-type Si solar cells. Various B emitter formation technologies are being explored but to date there is no single winner. Therefore, this thesis will investigate and evaluate the performance and formation of boron emitters using several promising industrially viable technologies (Chapter 7). In the following sections, methodology and understanding of the various promising B emitter technologies are described.

3.2.1 Boron Tribromide (BBr_3) Diffusion

One of the most popular and oldest technology for boron emitter formation involves boron diffusion in a tube furnace using liquid BBr_3 source. This process is generally divided in two steps : pre-deposition and drive-in. During the deposition, a gas mixture

consisting of oxygen (O_2), nitrogen (N_2), and BBr_3 vapors is flown in a heated tube furnace. This forms a B_2O_3-SiO_2 layer, called borosilicate glass (BSG), on the Si surface through the reaction of the gas mixture [25]. During the drive-in step, the elemental boron diffuses into the silicon wafer, resulting in the formation of homogeneous p^+ emitter with high boron surface concentration.

However, during the BBr_3 process, the high concentration of boron at the surface transforms the surface layer into a Si-B compound, SiB_6, which will be called a boron-rich layer (BRL) in this thesis. It has been conjectured that the BRL has negative effect on solar cell performance [26-28]. In addition, the BBr_3 source is a chemical hazard and involves additional process steps such as masking and etching to achieve single side B diffusion that is required for n-type Si cells. For these reasons, PV industry is somewhat reluctant to adopt the BBr_3 diffusion and is trying to explore an alternative. Therefore, this thesis will investigate B emitters formed by inkjet printing, spin coating, screen printing, ion-implantation, and APCVD which has the potential for single side diffusion and cost reduction.

3.2.2 Boron Diffusion by Spin Coating of Boric Acid Source

Boric acid (H_3BO_3) has been used as a spin-on source for boron diffusion which is applied on one side of the Si wafer by spin coating as illustrated in Figure 3.2. The Si wafer is then annealed in a furnace at a high temperature to diffuse boron from the boric acid source into Si wafer [29].

One advantage of this technique is that, unlike BBr_3 diffusion, it offers single side diffusion without masking steps. Moreover, the chemicals used in spin-on are safer than

the BBR_3 liquid source. Lastly, the applicability of this source and technique to p-type solar cells was confirmed by fabricating high efficiency p-base cells with p^+ BSF [29, 30]. However, this concept needs more technical development to solve wrap-around when the source is spread on one side. This could cause shunting problem and lead to loss in cell efficiency. This process may also lead to the formation of BRL on the surface, which will be studied in this thesis along with the impact of BRL on surface passivation, bulk lifetime, and n-type cell efficiency.

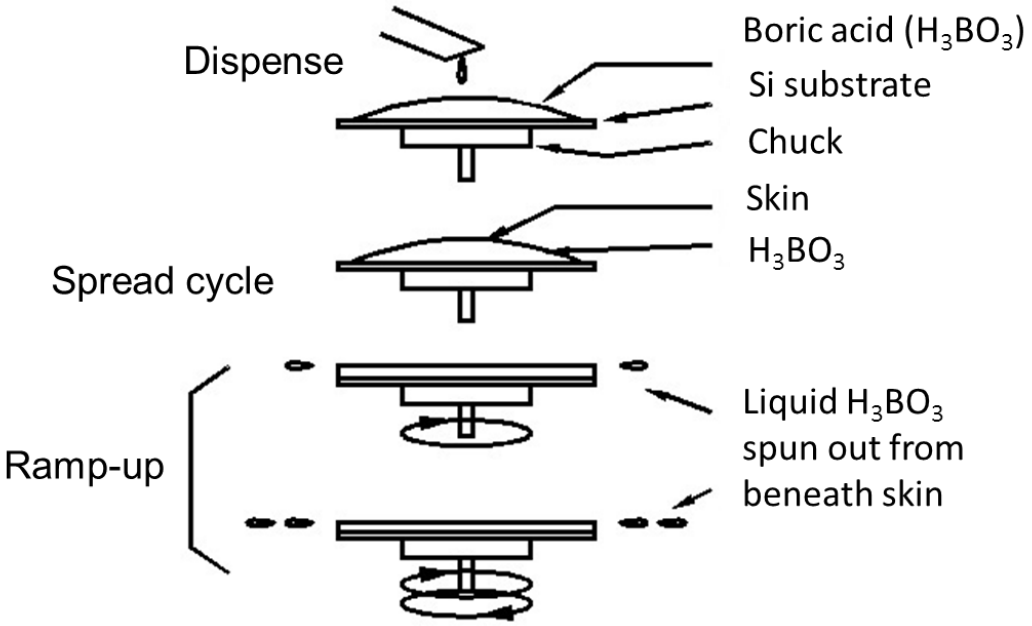


Figure 3.2 Schematic of spin coating process for boron diffusion.

3.2.3 Ion implantation

Ion-implantation for the formation of B emitters involves energetic charged B dopants which are accelerated and directly introduced into a substrate as shown in Figure

3.3 [31]. The substrate with B dopants then receives an anneal process at a high temperature. This process has been used extensively in semiconductor device fabrication and materials science research. In the late 1970s and early 1980s, ion implantation was used for the first time as a method for producing the p-n junction in photovoltaic devices by implanting dopant (boron or phosphorus) into silicon wafer followed by annealing process to remove implant damage and activate the implanted dopant [32]. Recently, commercial ready high efficiency Si solar cells have been fabricated using the ion implantation technology [20, 33].

Ion implantation offers following advantages in PV manufacturing : (1) Simplification of advanced cell formation by reducing complexity, number of processing steps, and cost, (2) sing-side diffusion and in-situ emitter oxide passivation without any masking step with high throughput of ≥1000 wafers per hour [34], and (3) patterned implantation to form selective emitters. In this thesis, the Solion ion implanter (Figure 3.3(b)) will be used for boron and phosphorus diffusion, which has been developed first for PV fabrication in collaboration with Suniva and Varian Semiconductor Equipment Associates (currently APPLIED MATERIALS) [35]. The implanter consists of five main components including the ion source, the mass analyzer, the accelerator, the beam shaping, and the end station for placing the silicon wafers for implantation.

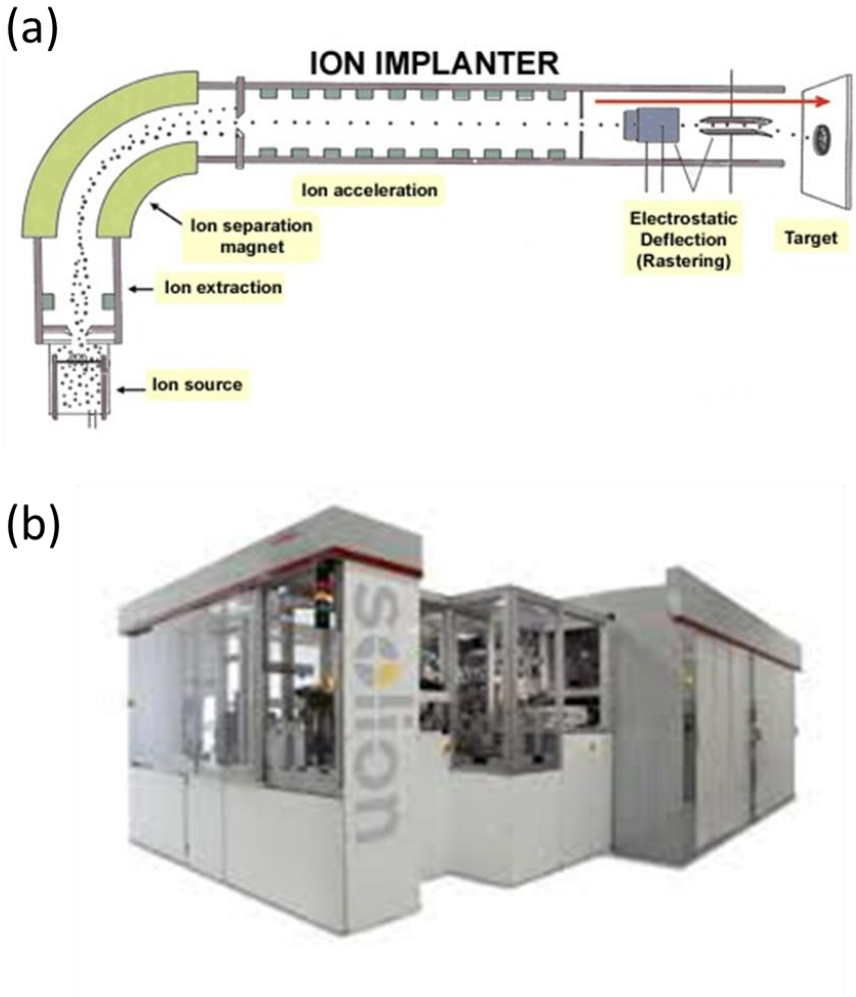


Figure 3.3 (a) Schematic diagram of ion implant system and (b) Varian Solion implanter.

3.2.4 Boron Emitter Formation by Inkjet and Screen Printing

Another promising low-cost high-throughput technology for boron diffusion involves the use of B containing source and printing tools like inkjet or screen printer. Like spin coating, in this thesis a commercial liquid boron source or paste (Honeywell Co. Ltd.) is deposited on Si wafer surface by using an inkjet printer (Fujifilm Dimatix DMP 2381) and screen printer (ASYS Group) as illustrated in Figure 3.4. After printing the source, a high temperature annealing is performed to drive-in B into Si. These printing techniques offer the potential for single-side diffusion without masking and patterning steps. However,

this technique may also be vulnerable to the formation of BRL layer, wrap-around issue, and challenges in maintaining bulk lifetime. Furthermore, the inkjet printing may have same throughput issues for mass production

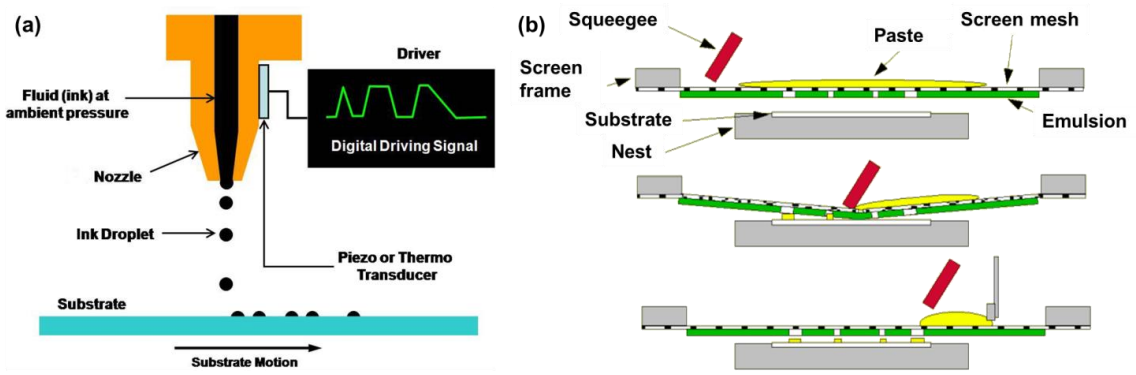


Figure 3.4 Schematic diagram of boron source deposition by (a) Inkjet printer and (b) Screen printer.

3.2.5. Atmospheric Pressure Chemical Vapor Deposition (APCVD)

APCVD is also a promising technology for B emitter formation because of the simplicity of tool and process in addition to a high deposition rate and low deposition temperature (~ 400℃). APCVD system configuration is also simple because it does not require a vacuum system. APCVD offers single side diffusion with high throughput and good uniformity. Like ion implantation, APCVD technique is mature in semiconductor industry and can be easily implemented in PV manufacturing. Figure 3.5 shows a schematic diagram of a APCVD system for film deposition [36]. For B emitter formation, a borosilicate glass (BSG) layer is deposited on the single side and then capped by amorphous silicon oxide (SiO_x) layer also grown by APCVD. This is followed by high temperature annealing or drive-in. The capped SiO_x layer serves as a dopant barrier to prevent out-diffusion.

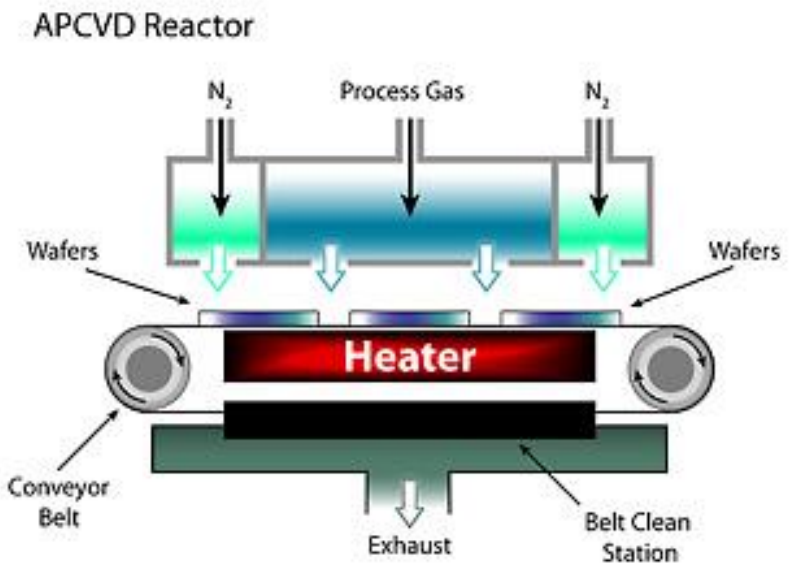


Figure 3.5 Schematic diagram of APCVD system for B-doped film deposition.

3.3 Understanding of Boron Rich Layer (BRL)

As shown in the previous section, the B emitter can be formed by various technologies. However, during the B emitter formation, an unintended boron-rich layer (BRL) is formed on the emitter surface which could have detrimental impact on surface passivation and bulk lifetime. Thus, the in-depth understanding of the BRL and its impact on achieving high efficiency n-type Si solar cells.

The BRL is a thin silicon boride layer in the form of SiB_6 compound, with very high B concentration, which can be formed between the boron silicate glass (BSG) and the heavily boron-doped emitter surface. Even though the BRL is linked to better sheet resistance uniformity, the BRL can be an undesirable product because of bulk lifetime degradation [28, 37]. In addition, the BRL is expected to interfere with surface passivation of boron emitter because of the presence of inactive boron, segregated metal impurities,

and structural defects in the BRL [27, 38]. For these reasons, the BRL has to be removed in order to achieve high efficiency n-type solar cells.

Thus, an important part of this thesis is to conduct a fundamental and applied research to understand the formation, role, and impact of BRL on emitter quality and cell efficiency. This will be done by investigating morphology, thickness, and composition of BRL in addition to quantifying the impact of BRL on all key cell parameters including τ_{bulk}, J_{0e}, V_{oc}, J_{sc}, and η. Research will be also conducted to develop an effective method for removing the BRL and so that high efficiency n-type cells can be manufactured.

3.4 Review of Dielectric Layers for Passivating Boron Emitter Surfaces

In addition to the formation of cost effective B emitter and the BRL issues, passivation of the boron emitter surfaces even without the BRL also been a challenging area for realizing the full efficiency potential of high efficiency n-type solar cells. The most commonly used dielectric layer in PV industry for passivating the n-type Si surfaces or emitter is PECVD silicon nitride (SiN_x), which also serves as anti-reflection coating. However, a single layer PECVD SiN_x film by itself is not suitable for boron emitter (p^+) surface passivation partly because it contains positive charge. This is reflected in the observed high emitter reverse saturation current density (J_{0e}) of ~ 100fA/cm^2 on planar and ~ 400fA/cm^2 on textured surfaces on 60~75Ω/sq boron emitters [39, 40]. Such high J_{0e} prevents achieving high V_{oc} and efficiency as explained in Chapter 2.2. Therefore, various dielectric layers are being explored today for improved boron emitter surface passivation. It has been shown that introducing a thin silicon oxide (SiO_2) layer between the boron emitter and SiN_x film can reduce J_{0e} value to ~ 25fA/cm^2 on a 75 Ω/sq emitter because

oxide has much lower positive density (Q_f) of $>10^{11}cm^{-2}$ and interface trap density (D_{it}) ~ $3x10^{10}eV^{-1}cm^{-2}$ [40]. A J_{0e} value of ~23fA/cm^2 has been also reported for boron emitter capped with a chemically-grown ultrathin oxide (SiO_x)/SiN_x stack layer [41]. Benick *et al.* reported excellent J_{0e} value of 10fA/cm^2 for 140 Ω/sq boron emitter capped with aluminum oxide (Al_2O_3)/SiN_x stack layer [42] because the Al_2O_3 has a high negative charge density (Q_f) of ~$10^{13}cm^{-2}$ as well as a low D_{it} of ~ $10^{11}eV^{-1}cm^{-2}$. This provides an effective filed effect passivation on highly doped p-type surfaces as explained in Figure 2.14 in chapter 2 [43, 44]. Therefore, in order to achieve ≥21% cells, this thesis will also explore and evaluate various dielectric layers to minimize J_{0e} for BRL free B doped emitters developed in this research.

3.5 A Review of Various Promising N-type Silicon Solar Cell Structures

Even though majority of the cells are made on p-type Si today, n-type Si solar cells offer potential for higher efficiencies because of superior electrical properties such as higher tolerance to metal impurities, higher lifetime of minority carriers, and no LID (Chapter 1.2). In addition to the excellent properties of n-type Si material, solar cell efficiencies are also dictated by cell design and process technologies. Therefore, this section will review various n-type solar cell structures and technologies used in the literature that have resulted in very high efficiency cells. The cell design and technologies to achieve low-cost high-efficiency n-type PERT cells in this research will be also established in this section.

3.5.1 N-type Si Solar Cell with Screen-printed Aluminum-alloyed Rear Emitter

This cell structure and process is simple, cost effective, and very similar to the fabrication of current p-type cells in production. It involves phosphorus diffusion on the front to create an n^+ front surface field and a screen printing of Al on the back to form an alloyed aluminum doped Si emitter at the rear. This results in n^+-n-p^+ back junction device structure shown in Figure 3.6. This structure is also referred to as PhosTop Si solar cell which has given ~ 18.9% efficiency [45, 46]. The advantage of this cell structure is low capital expenditures and rapid transfer to current industrial production lines, since most of the process steps including Al doped rear emitter and p-diffused front surface field are already being used for p-type cell production. However, this cell has an efficiency limit of ≤20% due to the absence of dielectric passivation and fully metalized Al emitter on the back. This represents a big cap between the efficiency potential of this cell structure and the target efficiency of 21% in this thesis. Therefore, this structure and concept will not be utilized in this research.

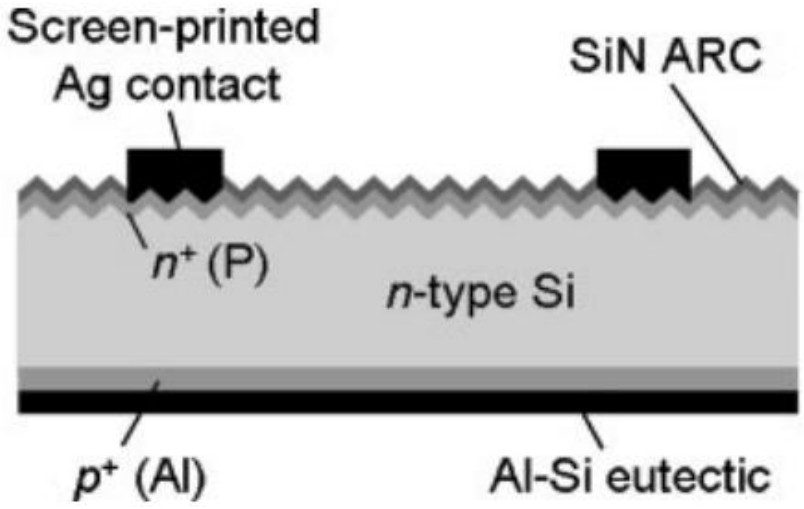


Figure 3.6 Schematic of n^+np^+ solar cell with screen-printed aluminum-alloyed rear junction.

3.5.2 N-type Front Junction Si Solar Cells with Al_2O_3 Passivated B Emitter

Unlike the PhosTop cell, this n-type cell structure has a p^+ emitter on the front and n^+ BSF layer on the rear. This cell structure (Figure 3.7(a)) is called PERT (**p**assivated **e**mitter and **r**ear **t**otally-diffused) and is shown in Fig. 3.7 (a) and is also the major focus of this research. This structure provides an enhanced optical confinement as well as an improved rear side passivation because of the point contacts to rear n^+ BSF layer which reduces metal recombination and a high quality rear dielectric layer capped with metal. In this structure, a trade-off is necessary for achieving high V_{oc} because a lightly-doped BSF layer is good for lowering J_{0b} and passivation, but a heavily-doped BSF layer is good for reducing metal recombination and achieving good ohmic contact [47]. Therefore, an optimized BSF is needed to balance rear surface passivation and contact.

Next, a PERL (**p**assivated **e**mitter and **r**ear **l**ocally-diffused) cell structure is shown in Figure 3.7(b), which overcomes this limitation of the PERT cell by introducing locally-diffused BSF. This not only helps in forming good ohmic contact, but also lowers J_{0b} because most of the back region is undoped and passivated with a high quality dielectric. Recently, 20.5% large area (239 cm^2) commercial-ready screen-printed PERT cell and 23.2% laboratory scale (22 cm^2) PERL cell with photolithography contacts have been reported [48, 49]. Al_2O_3 film was used in both cell structures for excellent surface passivation of B emitter to provide the field-effect passivation. For these reasons, the PERL cell structure gives higher efficiencies, but the processing cost is also higher than the PERT structure because of complex pattering or photolithography steps.

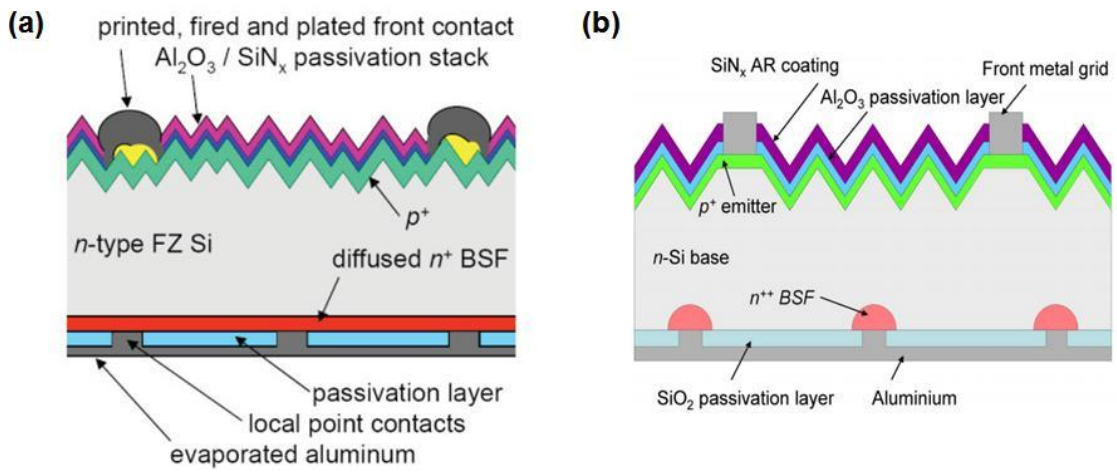


Figure 3.7 Schematic diagram of n-type (a) PERT and (b) PERL Si solar cell.

3.5.3 Interdigitated back Contact Silicon Solar Cell

Figure 3.8 shows a schematic diagram of the interdigitated back contact (IBC) cell. This cell structure is being mass produced by a company called SunPower [50]. The IBC structure demonstrates the very high efficiency potential of n-type solar cells with interdigitated boron-diffused rear emitter and phosphorus-diffused BSF. Since all the metal contacts in an IBC solar cells are on the rear (so called rear contact cell), the front side has no shading losses and excellent FSRV. Furthermore, it minimizes series resistance because metal coverage can be large on the rear side without any shading loss, resulting in a high fill factor. Recently, IBC cell efficiency as high as 25 % has been reported by SunPower [15, 51]. This is the most efficient silicon solar cell in production. However, fabrication process used for the IBC cells is very complex and expensive due to patterning which requires additional processing steps and multiple high temperature diffusion and oxidation. That is why in this thesis we opted for PERT cell with simplified process sequence. By

raising the cell efficiency of PERT cell to ≥ 21% it is possible to achieve much lower module and installed system cost ($/W) than IBC.

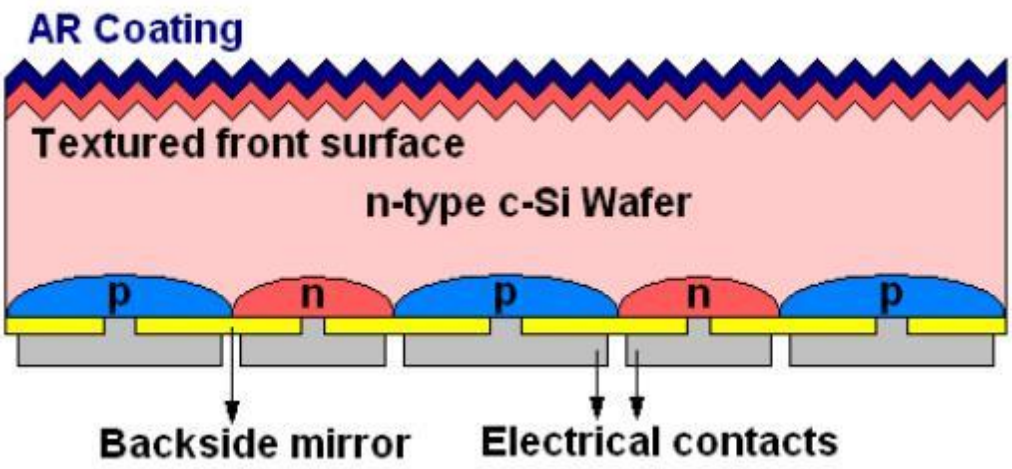


Figure 3.8 Schematic diagram of interdigitated back contact n-type solar cell.

3.5.4 Rationale of Selecting PERT Cell Structure in This Thesis

High cell efficiency alone is not sufficient for lower levelized cost of electricity if it comes at very high processing cost. Likewise lower cell cost is not enough unless the module efficiency is reasonable. This is because lower efficiency modules have much higher balance of system (BOS) cost which negates the benefit of lower module cost. Therefore, one needs to find the right intersection of cost and efficiency of silicon solar cells to achieve grid parity.

Among the cell designs mentioned above, PERL and IBC structures can already produce high efficiency (>21%), but their manufacturing cost is too high because of expensive and complex cell processing compared to PERT cell. On the other hand, the screen-printed Al-alloyed rear emitter (PhosTop) n-type solar cells can be manufactured at a very low cost relative to PERT, but their cell efficiency is too low to attain grid parity.

Therefore, overall objective of this thesis is to develop lower cost higher-efficiency large area n-type PERT solar cells with a target efficiency of ~21%.

Chapter 4 : INVESTIGATION AND DEVELOPMENT OF A NOVEL BORON-DOPED EMITTER FORMED BY INKJET PRINTING AND ITS SURFACE PASSIVATION PROPERTIES

The quantitative understanding of the reverse saturation current density J_{0e} of the B emitter is essential for designing and achieving high efficiency n-type Si solar cells. This is because the short wavelength response and open circuit voltage (V_{oc}) of a cell is affected by emitter recombination, which is characterized by J_{0e}. Once the J_{0e} value is known, the V_{oc} and the maximum attainable efficiency of n-type Si solar cells can be predicted.

The formation of a novel heavily-doped B emitter by inkjet printing technology was accomplished. In this chapter, J_{0e} of the inkjet-printed B emitter is studied by a combination of simulation and measurement. The B emitter and its passivation properties are optimized to reduce J_{0e} and achieve higher cell efficiency.

4.1 Modeling of N-type PERET Solar Cell to Establish Material and Device Parameters for Attaining ≥21% Efficiency.

Open-circuit voltage V_{oc} is expressed by the following equation :

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{4.1}$$

$$J_0 = J_{0e} + J_{0b} \tag{4.2}$$

where J_{0e} is emitter saturation current density and J_{0b} is the base saturation current density. It is clear that J_{0e} affects V_{oc} and cell efficiency. In order to assess the quantitative impact of J_{0e} on cell efficiency, device modeling was performed for a n-type PERT cell (Figure 3.7(a)) using the well-known PC1D device simulation program [52]. Table 4.1 summarizes

the practically achievable input parameters used for the PC1D model. Front surface recombination velocity (FSRV) was then varied from 1000 to 200000cm/s which varied the J_{0e} value in the range of 50-500fA/cm^2, while other parameters were fixed in Table 4.1. Note that the J_{0e} was calculated or extracted using PC1D for any given front surface recombination velocity (FSRV). Since J_{0e} includes the effect of emitter bulk and surface recombination, surface passivation alters the J_{0e} values. Note that the J_{0b} value was fixed at 150fA/cm^2 for these model calculations.

Table 4.1 Input parameters of n-type PERT cells for PC1D modeling.

Cell parameters		Unit
Resistivity	5	Ω.cm
Thickness	200	μm
Front reflectance	7	%
Bulk lifetime	1000	μs
Sheet resistance	65	Ω/sq
FSRV (J_{0e})	Varied	cm/s (fA/cm^2)
BSRV(n_n$^+$)	5	cm/s
Total R_s	0.45	Ω-cm^2

Figure 4.1 shows the PC1D calculated n-type solar cell efficiency as a function of J_{0e} or FSRV for the above input parameters. These calculations reveal that the J_{0e} should be less than 80fA/cm^2 to achieve ~21% efficient n-type solar cells. The corresponding FSRV is 3000cm/s. These calculations provide a quantitative guidelines for attaining material and device parameters, including bulk lifetime, FSRV, BSRV, and J_{0e} etc. for achieving the target of ~21% efficiency in this thesis. The formation of inkjet printed B emitter will be shown in the next chapter 5 in more detail.

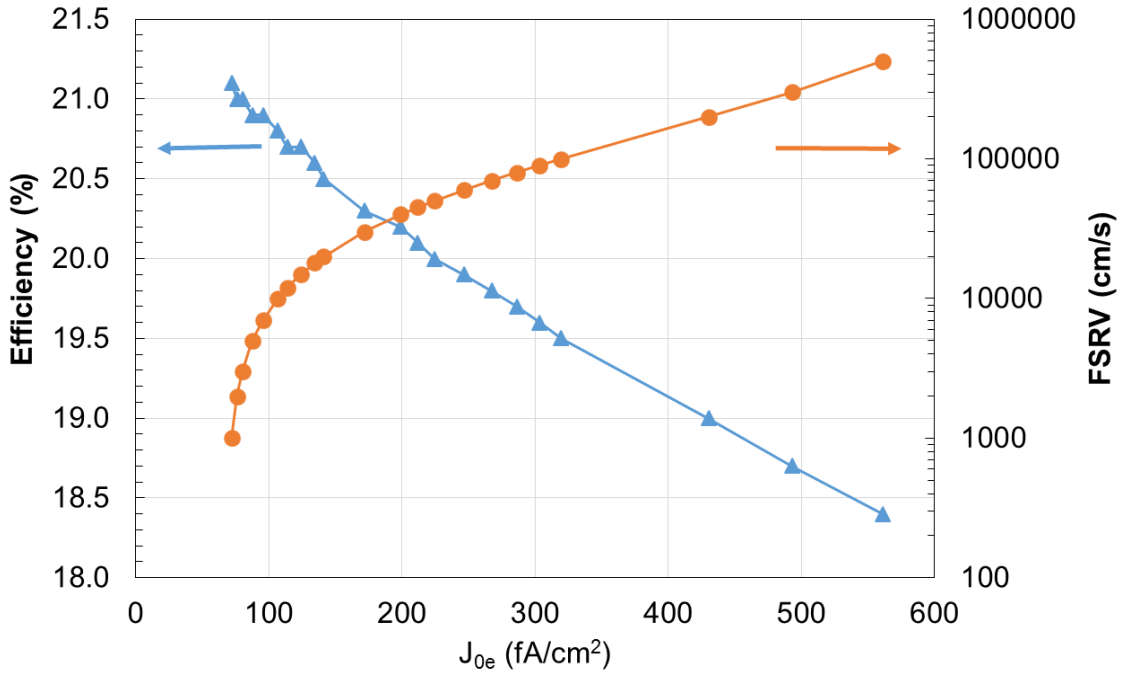


Figure 4.1 PC1D modeling of n-type solar cell efficiency as a function of J_{0e} and FSRV.

4.2 Formation and Analysis of Doping Profiles of Inkjet Printed Boron Emitters

Heavily boron-doped emitters were formed by using a novel inkjet printing technology in this thesis. As described in section 3.2.4, the inkjet printing technique provides single side homogeneous or selective B emitter without any masking or etching steps. This can lead to reduction in manufacturing cost of solar cell. The B emitter formation via inkjet printing involved applying a liquid boron source over the Si surface by the inkjet printer followed by an annealing process. The annealing process was optimized to achieve sheet resistances in the range of 45-120Ω/sq which is important for making good ohmic contacts to B emitter by screen printable metal paste. Besides sheet resistance, doping profile, the surface dopant concentration, and junction depth are also critical for high efficiency because they influence the contact quality, surface passivation,

and emitter recombination to impact FF, J_{0e}, V_{oc}, and cell efficiency. Note that for a good screen printed contact and high FF, the surface dopant concentration must be higher than $10^{19}cm^{-3}$ and the emitter thickness must be >0.3μm [53]. However, higher surface concentration increases the emitter recombination, therefore, the emitter profile needs to be optimized.

Different emitter profiles formed by the inkjet printing technique in this research were determined by secondary ion mass spectroscopy (SIMS) measurements. It was found that 900-950°C for 1 hour anneal in N_2 ambient resulted in the desired emitter sheet resistances in the range of 45-120Ω/sq for the B paste used in this study. Sheet resistances of 115Ω/sq, 70Ω/sq, and 45Ω/sq were obtained at annealing temperatures of 900, 925, and 950°C, respectively. The corresponding doping profiles for these three emitters are shown in Figure 4.2. All three emitters formed by the inkjet printing technique showed a very high surface concentration exceeding ~$1x10^{21}cm^{-3}$ with junction depth in the range of 0.3μm to 0.6μm. These doping profiles meet the requirement for good ohmic contact, however, the sharp rise in B concentration near the surface can have detrimental effect on surface passivation and J_{0e} due to Auger recombination and bandgap narrowing (BGN). This is because $J_0=qn_i^2*D/(N_A*L_{eff})$ and n_i increases and L_{eff} decreases with the increased heavy doping. This spiked heavily doped region, designated by the dotted line in Figure 4.2, will be defined as boron-rich layer (BRL) in this thesis and will be investigated in detail and eventually eliminated to achieve high efficiency cells with inkjet-printed B emitters.

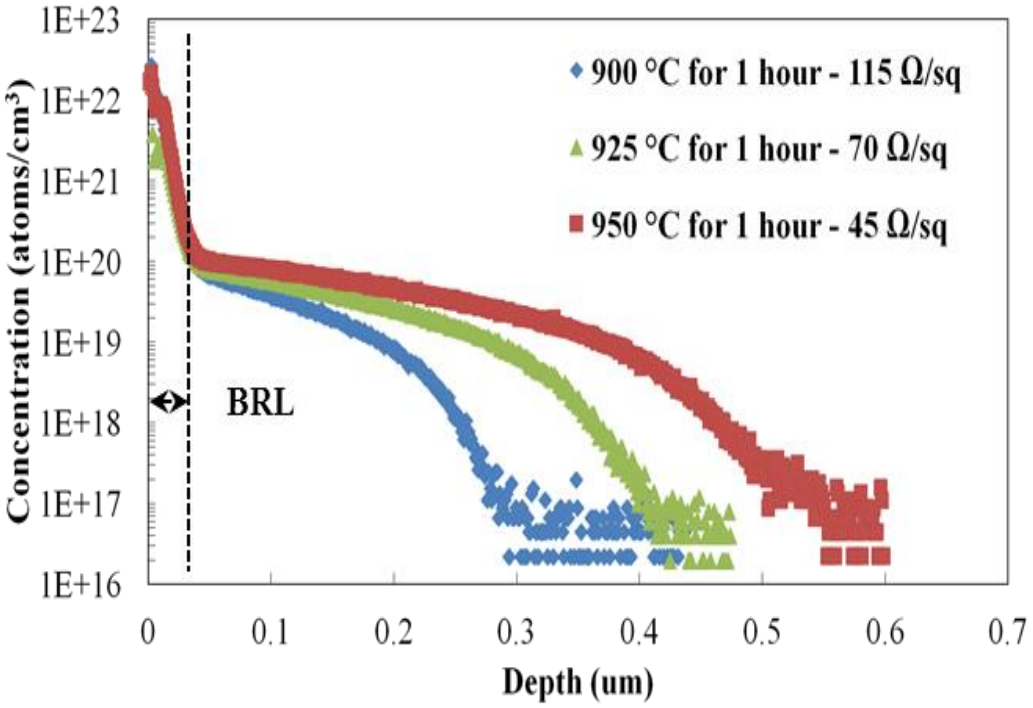


Figure 4.2 Sheet resistance and SIMS data for boron concentration profiles annealed at different temperature.

4.3 J_{0e} Study of Boron-doped Inkjet Emitters Passivated by SiN_x Antireflection Coating

Device modeling in Figure 4.1 showed that efficiency of an n-type Si solar cell depends on J_{0e} or the quality of passivated B emitter. Therefore, saturation current density J_{0e} of the p^+ emitters was examined quantitatively by a QSSPC technique by making symmetrically doped and passivated structures as shown in Figure 4.3. About 750Å thick PECVD SiN_x (refractive index, n=2.1) layer is routinely used on top of Si solar cell emitters as antireflection coating, which also serves as dielectric passivation layer. The thickness of SiN_x layer was selected (equation 2.15) to minimize reflectance at a wave length of 630nm where the solar spectrum has maximum power density.

Figure 4.3 Schematic diagram of J_{0e} sample structure.

The test samples for the J_{0e} measurement were prepared by forming identical p^+ emitters on both sides of a high resistivity n-type Si wafer (Figure 4.3). Based on the literature search at the start of this research, initial emitter sheet resistance target was selected to be 60~70Ω/sq [54, 55]. It was found that annealing time and temperature of 900℃ for 80min, 925℃ for 50min, and 950℃ for 25min gave nearly identical sheet resistance of ~ 65Ω/sq. The p^+ surfaces were then passivated by PECVD SiN_x without doing anything to the BRL. The recombination rate of the symmetric test samples can be expressed as [56]

$$U_{effetive} = U_{bulk} + 2U_{emitter} \tag{4.3}$$

$$\frac{\Delta n}{\tau_{eff}} = \frac{\Delta n}{\tau_{bulk}} + \frac{2J_{0e}np}{qWn_i{}^2} \tag{4.4}$$

which reduces to

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2J_{0e}(\Delta n+N_{dop})}{qWn_i{}^2} \tag{4.5}$$

where τ_{eff} is the effective lifetime, τ_{bulk} is the bulk lifetime, Δn is the excess minority carrier density, N_{dop} is the base doping concentration, and W is the sample thickness. The J_{0e}

measurement technique, developed by Kane and Swanson [57], acquires the injection level dependent recombination lifetime data from symmetric p^+np^+ structures made on lightly doped Si base in high injection. The J_{0e} is then determined from the slope of $1/\tau_{eff}$ vs Δn.

J_{0e} of the symmetric samples annealed at different temperatures for B diffusion (Figure 4.4) indicates that as the annealing temperature for the 65Ω/sq inkjet B emitters increases from 900℃ to 950℃, the J_{0e} value decreases from 625fA/cm^2 to 433fA/cm^2. However, the lowest J_{0e} value of 433fA/cm^2 is still too high for achieving ≥21% efficiency. Solar cell modeling in Figure 4.1 revealed that J_{0e} needs to be less than 80fA/cm^2 for ≥21% cell.

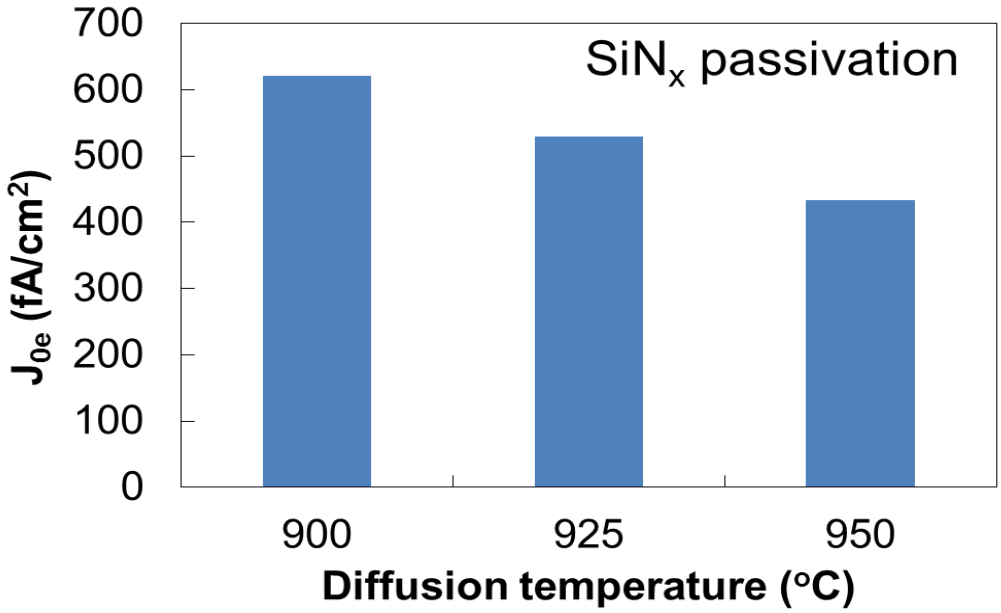


Figure 4.4 J_{0e} values of SiN_x capped inkjet B emitter annealed at different temperatures.

4.4 The Impact of BRL on J_{0e}.

Such high J_{0e} is attributed to the presence of BRL at the interface between the B emitter and SiN_x layer. As mentioned in section 3.3, the BRL can increase J_{0e} due to inferior

surface passivation. Therefore, the BRL should be removed before the dielectric surface passivation. To remove the BRL, a thermal oxidation was performed at 850℃ for 30min followed by HF dip. The idea was to consume the BRL by oxidation, which was confirmed by TEM measurements shown in Figure 4.5. TEM images clearly show that the BRL is composed of periodic agglomeration of dark regions near the surface which are clearly removed after the oxidation followed by HF dip.

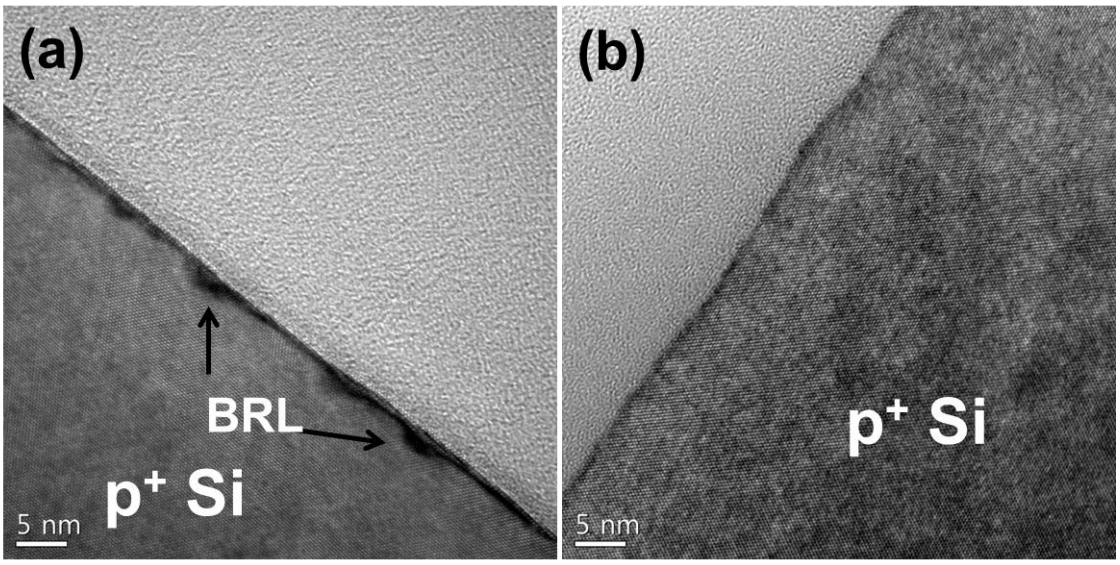


Figure 4.5 TEM images of cross-section of inkjet-printed boron emitter (a) Before oxidation and (b) After oxidation.

J_{0e} was re-measured after the BRL removal followed by SiN_x deposition. The result is shown in Figure 4.6. The J_{0e} of the SiN_x passivated 950℃ annealed boron emitter decreased sharply from 433fA/cm^2 to 198fA/cm^2 after the BRL removal. This proves that the BRL formed on the inkjet B emitters significantly degrades the J_{0e} but the BRL removal by post oxidation restores surface passivation, resulting in a factor of two reduction in J_{0e}.

However, even the 65Ω/sq BRL-free inkjet B emitter with SiN_x passivation was not able to achieve the target J_{0e} of ≤80fA/cm^2. This is attributed to the surface defects that have a relatively high capture cross section for minority electrons as reported in [58]. These defects are not passivated by PECVD SiN_x layer directly deposited on the B emitter. Therefore, instead of the SiN_x layer, we first applied a thermally-grown thin SiO_2 layer on B emitter after the BRL removal followed by SiN_x deposition. Figure 4.6 shows that the J_{0e} of the SiO_2/SiN_x capped B emitter, without the BRL, decreased further from 198fA/cm^2 to ~100fA/cm^2, which is approaching the target J_{0e} value of ~80fA/cm^2 for the 21% efficiency.

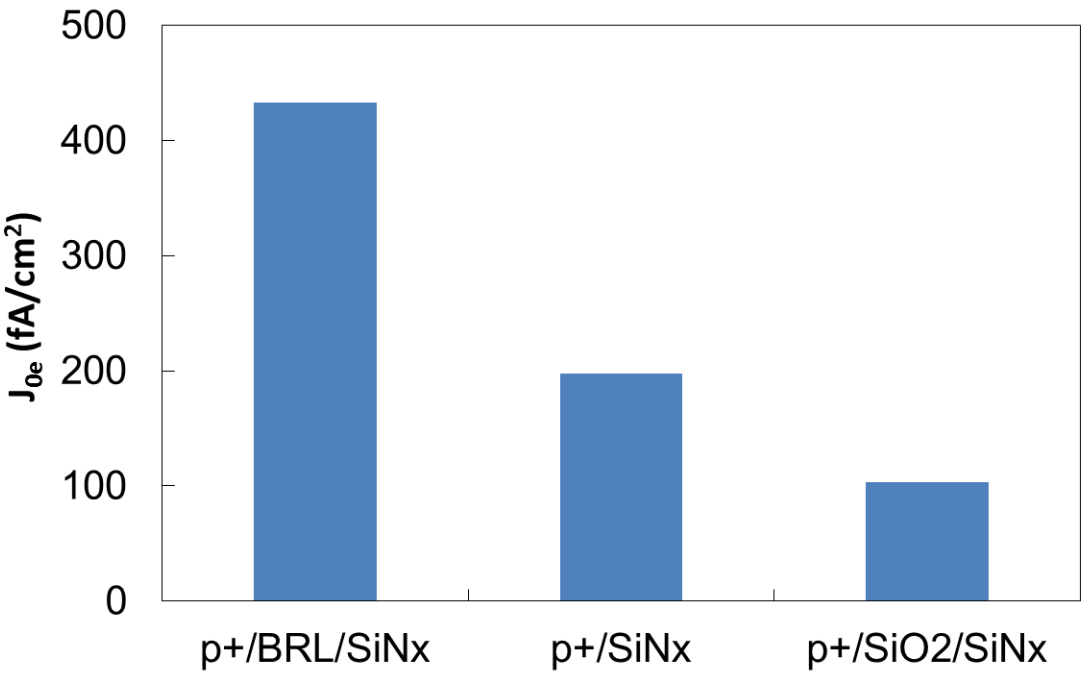


Figure 4.6 J_{0e} values of B emitter (p^+) capped with BRL/SiN_x, SiN_x only, and SiO_2/SiN_x layer.

4.5 Summary

Novel boron-doped emitters with sheet resistance in the range of 60-120Ω/sq were formed by inkjet printing of liquid boron source followed by annealing in the temperature range of 900℃ to 950℃. All the doping profiles showed very high near surface doping concentration of $\geq 1x10^{21}$ cm^{-3} due to the formation of undesirable BRL. SiN_x passivated inkjet-printed B emitters with the BRL gave very high J_{0e} values (> 400fA/cm^2). However, when the BRL was completely removed by a thermal oxidation process followed by HF dip, J_{0e} value decreased by a factor of two to ~ 198fA/cm^2 but was still short of the J_{0e} target of ≤80fA/cm^2. It was found that SiO_2/SiN_x stack passivation after the BRL removal reduced the J_{0e} value to ~100fA/cm^2 which is close to the target value of 80fA/cm^2 for 21% efficient n-type PERT cells.

Chapter 5 : INVESTIGATION AND UNDERSTANDING OF PROCESS-INDUCED BULK LIFETIME IN N-TYPE SILICON WAFERS

In chapter 4, J_{0e} of the inkjet-printed B emitter was investigated through various surface passivation schemes in order to minimize the J_{0e} for high V_{oc} and efficiency. This chapter focusses on process-induced bulk lifetime in n-type Si wafers because the bulk lifetime in the finished cell is extremely important for achieving 21% efficiency on n-type devices. Therefore, like the J_0 study in the previous chapter, the device simulations were performed using PC1D to quantitatively assess the impact of bulk lifetime on n-type solar cell efficiency and establish the target bulk lifetime value for achieving ~21% efficient cell. It is important to recognize that cell processing at high temperature can change bulk lifetime due to impurities and defects. Next, process-induced bulk lifetime in n-type Si is measured and a processes sequence is developed for cell fabrication in order to maximize bulk lifetime while maintaining low J_{0e}.

5.1 Solar Cell Modeling to Establish Bulk Lifetime and Resistivity Requirements for Achieving 21% Efficiency

Short circuit current density J_{sc} of solar cells can be expressed by :

$$J_{sc} = \int_{E_g}^{\infty} q \cdot N_{ph}(\lambda) \cdot EQE(\lambda) d\lambda \tag{5.1}$$

$$EQE(\lambda) \approx f(S_{01}, S_{02,} \tau) \tag{5.2}$$

As shown in the simplified Equation (5.2), external quantum efficiency (EQE) is dictated by front and back surface recombination velocities (S_{01} and S_{02} in Figure 5.1) and bulk lifetime (τ). Open circuit voltage is expressed as :

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{J_{sc}}{J_{0e}+J_{0b}}\right) \tag{5.3}$$

where J_{0b} is the base saturation current density. The J_{0b} is dictated by several terms as shown in the following Equation (5.4) [59]:

$$J_{0b} \approx (W, S_{02}, \tau) = \frac{q{n_i}^2}{N_D} \cdot \frac{D}{L} \cdot \frac{\frac{SL}{D}+\tanh\left(\frac{W}{L}\right)}{1+\frac{SL}{D}\tanh\left(\frac{W}{L}\right)} \tag{5.4}$$

where *W* is the thickness of a solar cell, N_D is the donor density in the bulk, *D* is the diffusion coefficient of the minority carriers in the bulk, and *L* is the diffusion length in the bulk (expressed as $\sqrt{D\tau}$). Since bulk lifetime τ affects both J_{sc} and V_{oc}, it is of important factor, along with J_{0e}, in dictating solar cell efficiency.

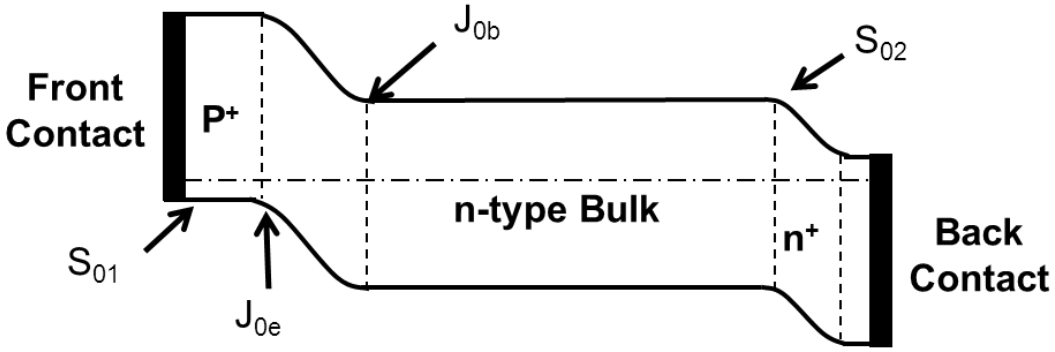


Figure 5.1 Energy band diagram of a n-type solar cell.

Therefore, in this section, solar cell simulations were performed by PC1D in order to establish the targets for bulk lifetime and resistivity for 21% efficient n-type Si solar

cells. The input parameters for these simulations are summarized in Table 5.1. Resistivity of n-type Si wafer was varied in the range of 1 to 20 ohm.cm and the bulk lifetime of the given resistivity varied in the range of 1 to 2000 μs. All other parameters except for resistivity and lifetime were fixed and were the same as for the J_{0e} simulation in the previous chapter. Also, note that the J_{0e} was fixed at 80fA/cm^2 (3000cm/s FSRV) for these simulations.

Table 5.1 Input parameters of n-type Si solar cells for PC1D simulation.

Cell parameters		Unit
Resistivity	1~20	Ω•cm
Thickness	200	μm
Front reflectance	7	%
Bulk lifetime	1~2000	μs
Sheet resistance	65	Ω/sq
FSRV (J_{0e})	3000 (80)	cm/s (fA/cm^2)
BSRV(n_n$^+$)	5	cm/s
Total R_s	0.45	Ω-cm^2

The result of the simulations are shown in Figure 5.2 where efficiency is plotted as a function of bulk lifetime in the range of 1~2000μs and resistivity in the range of 1 to 20Ω•cm. It is clear that both resistivity and lifetime are important for efficiency and 21% efficiency can be achieved by a several combinations of lifetime and resistivity for cell

parameters shown in Figure 5.2. Calculations also reveal that low resistivity and high lifetime combination gives the highest efficiency. However, in reality, lifetime tends to decrease with increased doping (decreased base resistivity). This decrease in lifetime is attributed to an increased dopant defect interaction or the presence of shallow traps [60]. Therefore, in this thesis, 5Ω•cm n-type Si wafers were selected which can comfortably give lifetime in excess of 1ms and help in achieving cell efficiency of 21% when combined with J_{0e} of 80fA/cm^2.

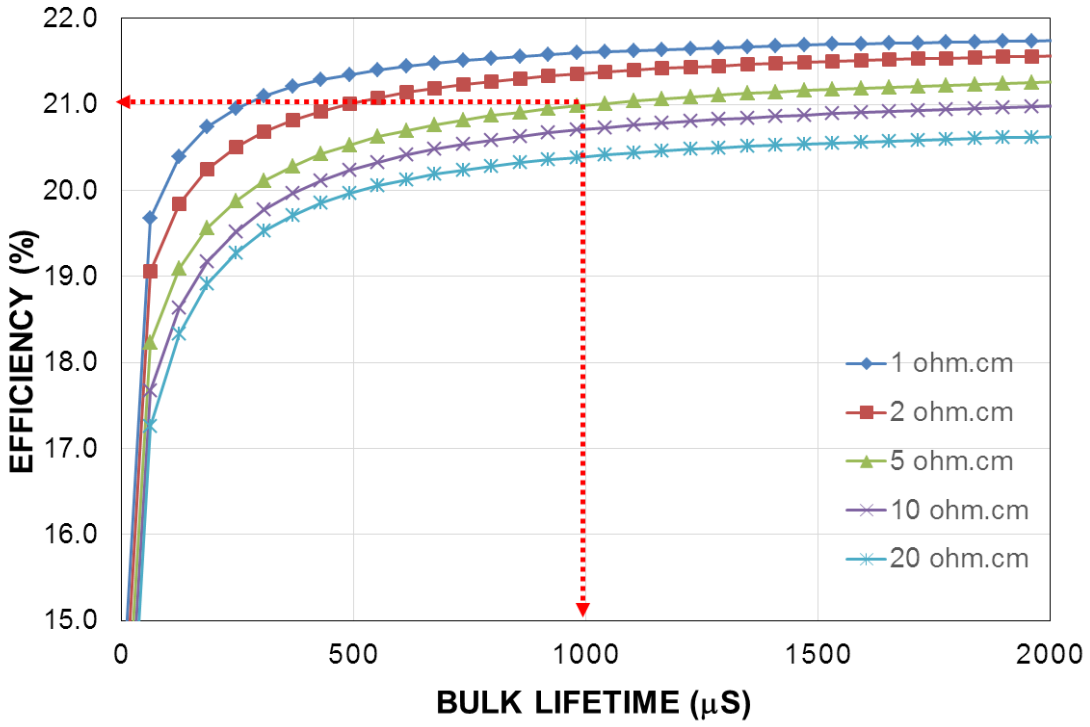


Figure 5.2 PC1D modeling of n-type solar cell efficiency as a function of bulk lifetime and resistivity.

5.2 Effect of Inkjet Boron Diffusion Process on Bulk Lifetime of N-type Si Wafer

Device modeling in Figure 5.2 showed that bulk lifetime over 1ms is needed in the finished device based on 5Ω•cm n-type Cz Si wafer for the efficiency target of 21%. This

is not trivial because it has been reported that high temperature B diffusion can sometimes lead to lifetime degradation [28] in spite of high lifetime in the starting Si wafer. This is especially important for liquid B source used for inkjet printing. Therefore, detailed investigation was performed to study inkjet B emitter process induced lifetime degradation in 5Ω•cm n-type Si wafers. Since both B emitter and P BSF are the essential components in n-type PERT solar cells, phosphorus (P) doped back surface field (BSF) process induced lifetime was also examined to determine the bulk lifetime in the finished n-type PERT solar cells. This was done by first preparing p^+/n test structures by inkjet printing the B source on the front and then using those samples for ion-implantation of P on the rear side as shown in Figure 5.3. The samples were then annealed at 900 ℃ for 80m, 925 ℃ for 50m, and 950 ℃ for 25m to form the B emitter and P-BSF simultaneously. After the annealing step, heavily-doped regions in the above three samples were removed by using a Si etching solution followed by immersing them in the iodine/methanol (I/M) solution passivation which is known to passivate the bare Si surface effectively [61].

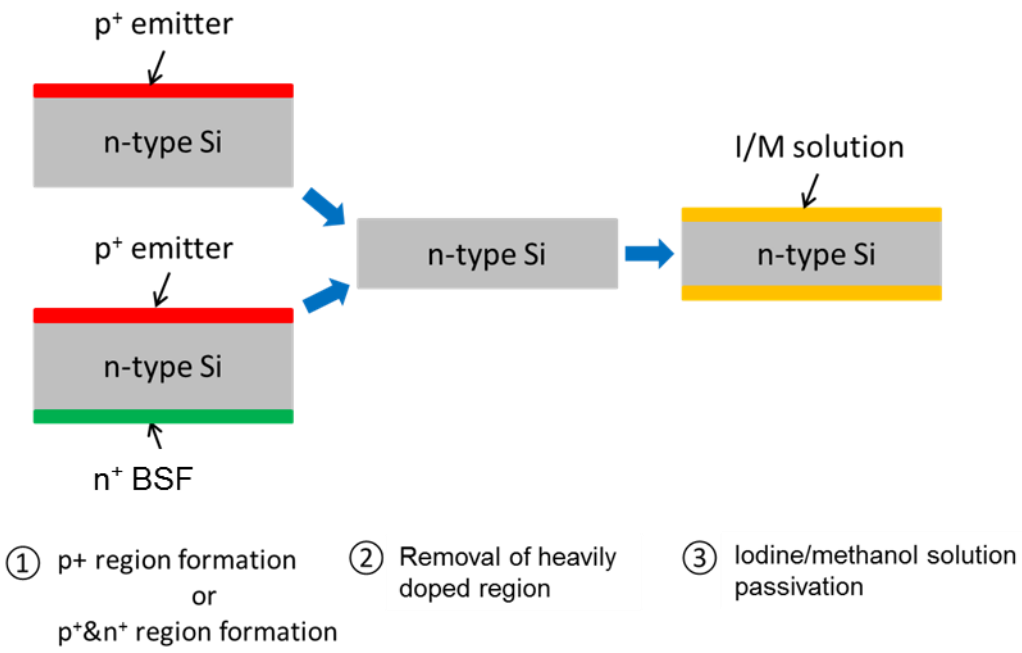


Figure 5.3 Process sequence of sample preparation for process-induced bulk lifetime measurements.

Then the effective lifetime (τ_{eff}) was obtained from the QSSPC measurement at an injection level of ~1x10^{15}cm^{-3}, which is expressed as,

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{W} \tag{5.5}$$

where *S* and *W* represent surface recombination velocity and wafer thickness, respectively. In this study, bulk lifetime (τ_{bulk}) was determined by assuming S=0 (consequently, $\tau_{bulk} \approx \tau_{eff}$) because I/M solution is known to provide excellent surface passivation for Si bare surface with S < 5cm/s [62].

The results of the measured bulk lifetime are summarized in Figure 5.4. Interestingly, lifetime degradation was observed in B diffused samples with p^+/n structure processed at 925 ℃ and 950 ℃ as shown in Figure 5.4(a). This is attributed to poor inkjet printed B diffusion gettering in this temperature range which is unable to extract process induced impurities and defects in Si [63]. On the other hand, all the $p^+/n/n^+$ samples in

Figure 5.4(b) showed over 1ms bulk lifetimes which is good enough for 21% efficiency. Unlike the B diffusion, P diffusion is known to enhance bulk lifetime due to effective gettering of impurities [64]. Therefore, P gettering during the co-annealing of B and P doped surfaces can help the lifetime preservation. This is also a significant finding because co-annealing reduces the number of processing steps and improves the manufacturability of the cells. This finding will be implemented in the fabrication of high efficiency n-type PERT solar cells.

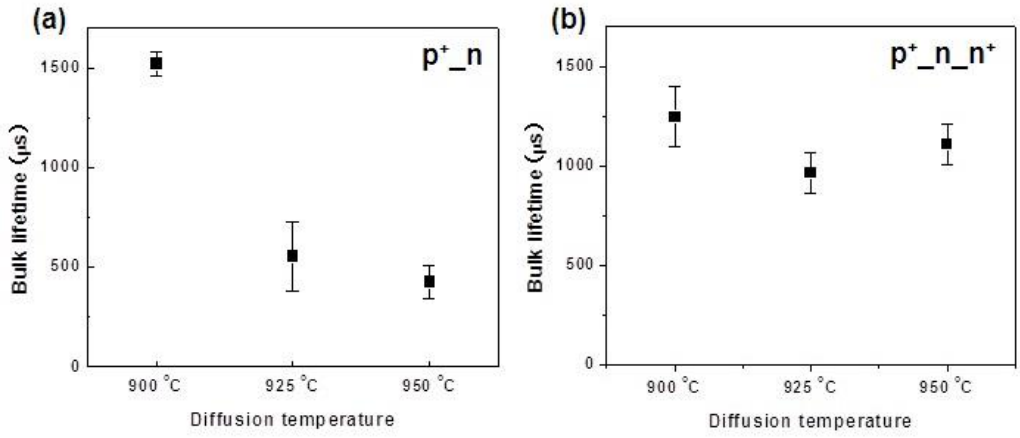


Figure 5.4 Bulk lifetime in (a) *p+/n* and (b) $p^+/n/n^+$ structures formed by annealing in the temperature range of 900 °C to 950 °C.

5.3 Effect of BRL Removal by Oxidation on Bulk Lifetime

In the above study, high bulk lifetime (≥1ms) was achieved after B and P co-diffusion in the temperature of 900℃ to 950℃ but the BRL was not removed for achieving low J_{0e}. It was demonstrated in section 4.4 that a thermal oxidation after the B diffusion was needed to remove the BRL in order to reduce J_{0e}. Therefore, the bulk lifetime was also studied after the BRL removal by oxidation in an attempt to achieve good lifetime as well

as low J_{0e} simultaneously. Figure 5.5 shows the process matrix and sample preparation sequence for oxidation induced lifetime measurement. A $p^+/n/n^+$ structure was first prepared using B and P co-diffusion at 900, 925, and 950°C. After that, a thermal oxidation was performed at 850°C for 30 minutes to consume the BRL. Then both p+ and n+ regions were removed by Si etching solution followed by I/M passivation to measure bulk lifetime by QSSPC technique.

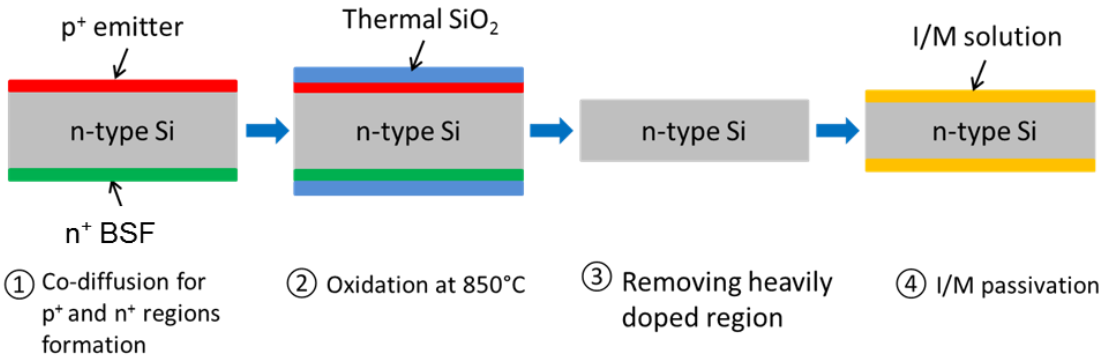


Figure 5.5 Process sequence studying for post-diffusion oxidation induced lifetime.

Figure 5.6 shows the results of this study. Surprisingly, a significant bulk lifetime degradation was observed in all cases due to the oxidation after co-diffusion (Figure 5.4(b)). This suggests that oxidizing the BRL gives rise to a source of contamination. This can happen if impurities trapped in the BRL are injected into Si during the oxidation process which consumes the BRL [63, 65]. This leads to a tradeoff between J_{0e} and bulk lifetime because BRL removal is necessary for lower J_{0e} but it also degrades bulk lifetime if the BRL removal is done by oxidation. Therefore, an alternative method to the thermal oxidation needs to be developed to achieve low J_{0e} and high bulk lifetime simultaneously. This will be developed in the next chapter.

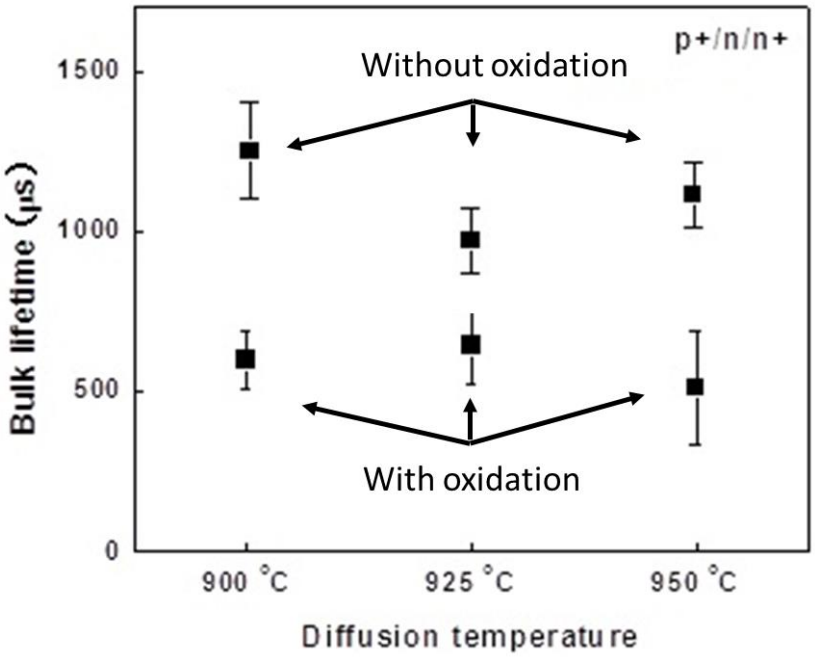


Figure 5.6 Bulk lifetime of $p^+/n/n^+$ structures before and after a thermal oxidation step after co-diffusion.

5.4 Summary

Process-induced bulk lifetime in n-type Si wafers was studied in this chapter, because the bulk lifetime in finished device is very important for solar cell efficiency. Model calculations were performed to establish base resistivity and bulk lifetime requirements to achieve 21% cells. A 5Ω•cm n-type Cz Si material was selected in this thesis and the model calculations showed that at least 1ms bulk lifetime should be maintained in the finished device for achieving ≥21% PERT cells. Process-induced lifetime study using $p^+/n/n^+$ structures on this material showed high bulk lifetime (>1ms) after the B and P co-diffusion in the temperature range of 900 °C to 950 °C due to phosphorus

diffusion-induced effective gettering of impurities. However, a 850°C thermal oxidation after the co-diffusion, used for BRL removal, degraded the bulk lifetime significantly to lower than 500μs. This negates the benefit of good surface passivation or low J_{0e} due to BRL removal. Therefore, an alternative method to the thermal oxidation is developed in the next chapter to remove the BRL which not only gives lower J_{0e}, but also preserves bulk lifetime.

Chapter 6 : DEVELOPMENT OF A RAPID CHEMICAL ETCHING PROCESS FOR BRL REMOVAL AND SUBSEQUENT SURFACE PASSIVATION FOR HIGH BULK LIFETIME, LOW J_{0e}, AND HIGH EFFICIENCY

As shown in previous chapters, the boron-rich layer (BRL) needs to be removed after the boron diffusion to attain high efficiency. It was shown in chapter 4 that a high temperature thermal oxidation after the B diffusion was successful in removing or consuming the BRL, but it led to bulk lifetime degradation. This resulted in reduction in cell efficiency in spite of better surface passivation. For this reason, an alternate method for BRL removal is developed in this chapter to achieve excellent surface passivation and high bulk lifetime simultaneously.

In this chapter, a low temperature chemical etching treatment (CET) was investigated to remove the BRL to avoid degradation in bulk lifetime. Furthermore, this chapter shows a positive synergistic effect of passivating the chemically-etched p^+ emitter surface with nitric acid-grown oxide (NAO) capped with plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) which reduced J_{0e} further from 430fA/cm^2 to100fA/cm^2. This led to a 1.6% increase in absolute cell efficiency including 22mV increase in V_{oc} and 1.9mA/cm^2 increase in J_{sc}. This resulted in screen-printed large area (239cm^2) n-type Si solar cells with efficiency of 19.0% compared to 17.4% with the BRL layer and SiN_x layer for surface passivation.

6.1 Impact of BRL Removal by Chemical Etching and Subsequent Passivation on J_{0e}, Bulk Lifetime, and Cell Efficiency

In this section, several alternative to thermal oxidation are investigated to remove the BRL followed by B emitter passivation to achieve high efficiency cells. Large area (239 cm^2) n-type Si solar cells with different surface passivation schemes were fabricated to evaluate the impact of various emitter surface passivation schemes. For J_{0e} measurements, 6 inch pseudo-square high lifetime n-type Cz Si wafers with a resistivity of 5 Ω•cm were used. After the RCA cleaning, a boron dopant source was printed on both surfaces using a Fuji Dimatix DMP 2831 inkjet printer. After that a drive-in was performed at 950 °C for 1 hour in a nitrogen (N_2) ambient followed by a short 5 % hydrofluoric acid (HF) dip for boron glass removal. This resulted in a boron emitter sheet resistance of 45 Ω/sq with the BRL intact. Then the wafers were divided into four groups : I, II, III, and IV, as shown in Figure 6.1(a). Groups I and II with the BRL were passivated by SiN_x and NAO/SiN_x stack, respectively, on both sides. Groups III and IV received a chemical etching treatment (CET) using a mixture of nitric acid (HNO_3), glacial acetic acid (CH_3COOH), and HF for a short period (<1min) to remove the BRL. After the CET, the sheet resistance of boron emitter increased from 45Ω/sq to 60Ω/sq. Wafers in group III and IV were subjected to symmetric double side passivation using SiN_x and NAO/SiN_x films. Finally, all the samples, without any metallization, were subjected to a thermal cycle with a peak temperature of 750 °C in a belt furnace to simulate the firing of screen-printed contacts. The quasi-steady state photoconductivity (QSSPC) technique was used on these symmetric structures for the J_{0e} measurements.

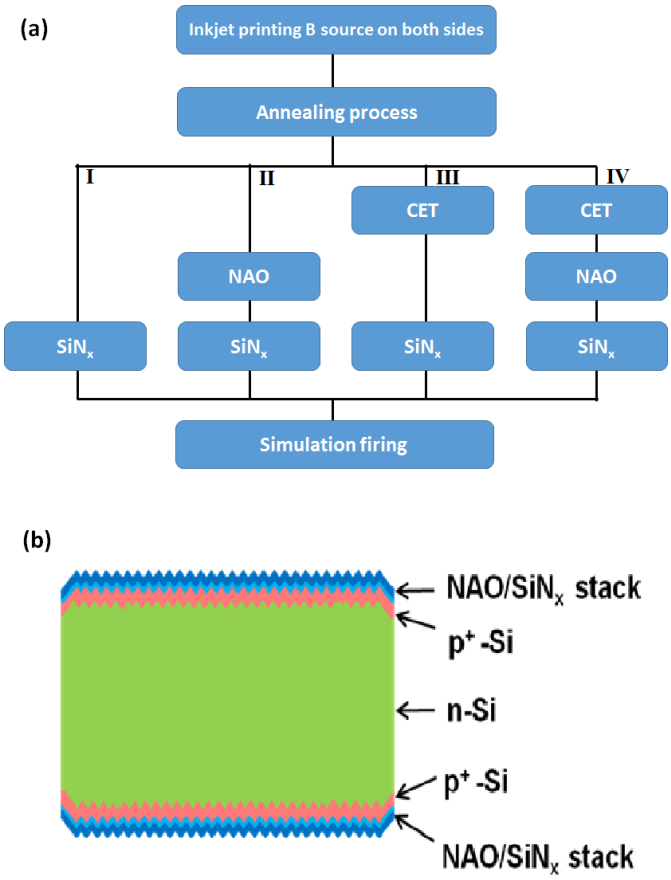


Figure 6.1 (a) Schematic diagram (a) experimental plan and (b) structure of J_{0e} sample.

Besides the symmetric test structure, large area (239cm^2) n-type Si solar cells (Figure 6.2(b)) were also fabricated on 6 inch pseudo-square 5Ω•cm Cz n-type Si wafers. Cell process sequence involved standard saw damage etching and chemical texturing, phosphorus implantation on the rear surface for the n^+ back surface field (BSF). A boron dopant source was deposited on the front surface using the inkjet printer. The samples were subjected to a 950^{o}C drive-in for 1 hour in a tube furnace in a N_2 ambient. Then the samples were divided into four groups for different surface passivation as shown in Figure 6.2(a). After the surface passivation, a grid pattern on the front and point contact pattern

on the rear were screen-printed by using silver/aluminum (Ag/Al) and Ag paste, respectively. A rapid co-firing process at a peak temperature of 750^{o}C was used to form the front and back screen printed contacts. Finally, a Ag paste was screen-printed on the rear to connect the point contacts and provide efficient back surface reflector.

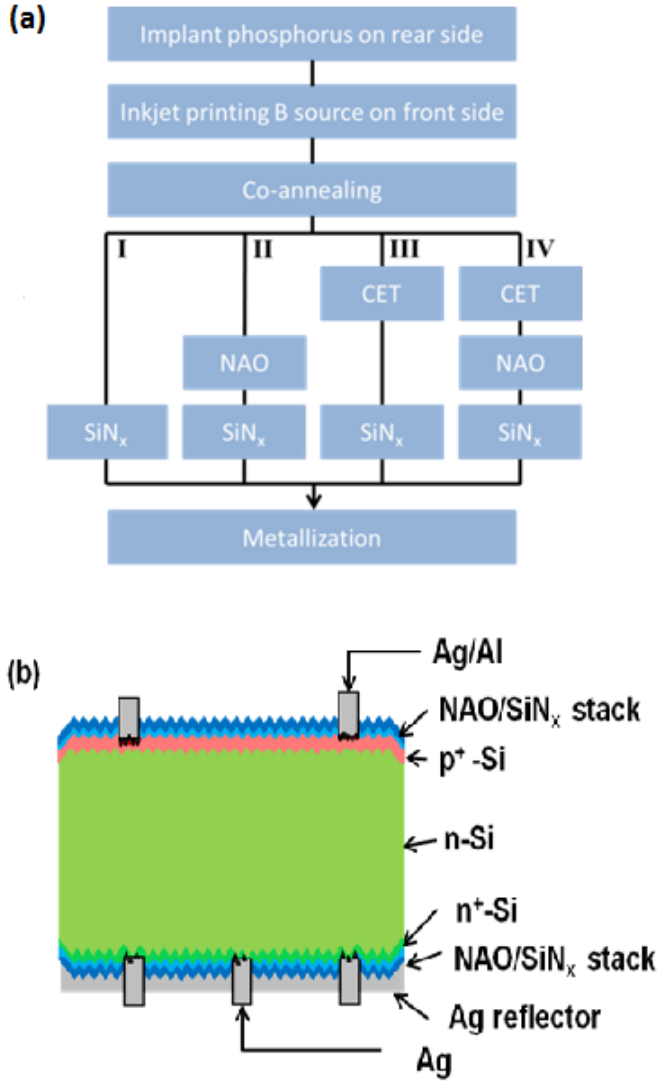


Figure 6.2 Schematic diagram of (a) experimental plan and (b) structure of n-type solar cell.

Table 6.1 shows the measured J_{0e} values (without metallization) and *I-V* parameters of the cells in groups I, II, III, and IV. A J_{0e} of 430fA/cm^2 and efficiency of only 17.4% was obtained for group I which had the BRL underneath the SiN_x passivation. The group II with NAO/SiN_x stack passivation on top of the BRL showed an improved J_{0e} of 230fA/cm^2 and cell efficiency of 18.0%. To investigate and quantify the effect of BRL removal by chemical etching prior to the passivation, J_{0e} and cells in the groups III and IV were also analyzed. The group III samples with SiN_x passivation showed a higher J_{0e} of 480fA/cm^2 compared to group I, in spite of BRL removal. This is probably because the chemical etching of BRL in group III may have induced some surface damage to increase interface recombination [66] which could not be passivated by SiN_x alone. This is consistent with the poor efficiency of 17.1% for group III. This indicates that the BRL removal by CET is not sufficient to lower the J_{0e} value unless a proper surface passivation is applied. The group IV samples with NAO/SiN_x passivation after the BRL removal showed a very significant improvement in surface passivation with a J_{0e} value of 100fA/cm^2 in conjunction with cell efficiency of 19.0%, open-circuit voltage (V_{oc}) of 644 mV, and short-circuit current (J_{sc}) of 38.6mA/cm^2. This is because the NAO is able to mitigate the impact of CET induced surface damage and provide a superior passivation compared to the direct SiN_x layer on the boron doped emitter surface.

Table 6.1 J_{0e} values and cell efficiencies with different passivation scheme.

Group	Passivation Scheme	J_{0e} (fA/cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
I	SiN_x	430	622	36.7	0.76	17.4
II	NAO/SiN_x	230	626	37.3	0.77	18.0
III	$CET + SiN_x$	480	620	36.5	0.76	17.1
IV	$CET + NAO/SiN_x$	100	644	38.6	0.76	19.0
Target	-	≤80	>644	>38.6	>0.77	~21

Note that 19% efficiency is well below the efficiency target of 21% so these cells require further improvement in V_{oc}, J_{sc}, and FF which will be discussed and accomplished in the next chapters.

6.2 Internal Quantum Efficiency (IQE) Analysis to Validate the J_{0e} and Cell Efficiency for Various Passivation Schemes

Internal quantum efficiency (IQE) of the finished solar cells was measured to understand and explain the significant improvement observed in J_{0e}, V_{oc}, J_{sc}, and efficiency of group IV cells with chemically etched BRL followed by NAO/SiN_x stack passivation. Figure 6.3 shows the IQE of cells with four different B emitter passivation schemes : I. $BRL+SiN_x$, II.$BRL+NAO+SiN_x$, III. chemically etched $BRL+SiN_x$, and IV. chemically etched $BRL+NAO+SIN_x$. Note that an appreciable difference in IQE is observed in the short wavelength range (350 to 650 nm) but almost no change in the long wavelength IQE. This confirms that the observed improvement in V_{oc}, J_{sc}, and efficiency of group IV cells is associated with the emitter passivation and not with the bulk lifetime or BSF. In addition,

the IQE trend in the short wavelength is entirely consistent with the trend in J_{0e}, as shown in Table I. Unlike the BRL removal by thermal oxidation which degraded bulk lifetime, the strategy to remove BRL by chemical etching followed by NAO/SiN_x passivation was able to preserve bulk lifetime (~1ms) in addition to providing excellent B emitter passivation.

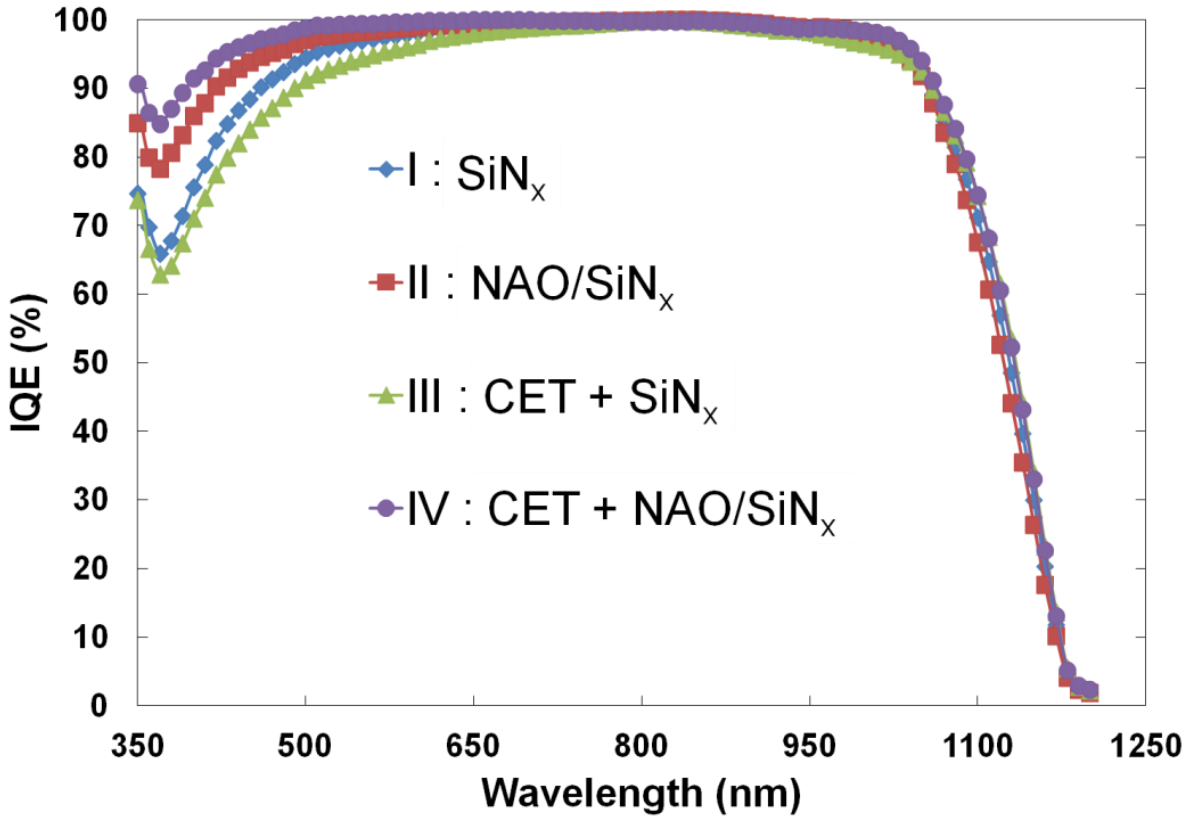


Figure 6.3 IQE data of the n-type Si solar cell by using different passivation process of group I – IV.

6.3 Detailed Understanding of the BRL and the Si Interface by Transmission Electron Microscopy (TEM)

Previous section showed that the BRL formed during the inkjet B emitter formation played an important role in controlling the bulk lifetime and emitter surface passivation. Therefore, an attempt is made in this section to gain an in-depth understanding of the formation and composition of the BRL by TEM and auger electron spectroscopy (AES) measurements. Figure 6.4 shows scanning transmission electron microscopy (STEM) and high resolution electron microscope (HREM) images of the SiN_x-NAO-p^+-Si interface of samples in groups II and IV, which represent NAO/SiN_x passivated samples with and without the BRL, respectively. A very thin dark layer with periodic agglomeration, indicated by black arrow in Figure 6.4(a), was observed at the Si/SiN_x interface in the case of NAO/SiN_x passivated sample with the BRL. However, NAO/SiN_x passivated p^+ emitter without the BRL in Figure 6.4(b) showed a very clean interface with no dark region or agglomeration. These agglomerations are attributed to impurities and structural defects in the crystal lattice that can give rise to recombination centers [67]. HREM images of the same spot are shown in Figure 6.4(c) and Figure 6.4(d) to magnify the image of the interface even further. HREM images revealed that the group II sample with the BRL showed a 10 nm thick dark layer in conjunction with the agglomerated regions of 20~25 nm in size [Figure 6.4(c)]. The group IV sample with the BRL removed, Figure 6.4(d), showed only few dark spots and virtually no agglomeration. Thus, the chemical etching process used in this study was able to remove the BRL composed of thin dark layer and the agglomerations at the interface. After the BRL removal, a very uniform light-colored

NAO layer with a thickness of about 1 nm is also observed in Figure 6.4(c) and (d) supporting that NAO is not directly passivating the Si interface.

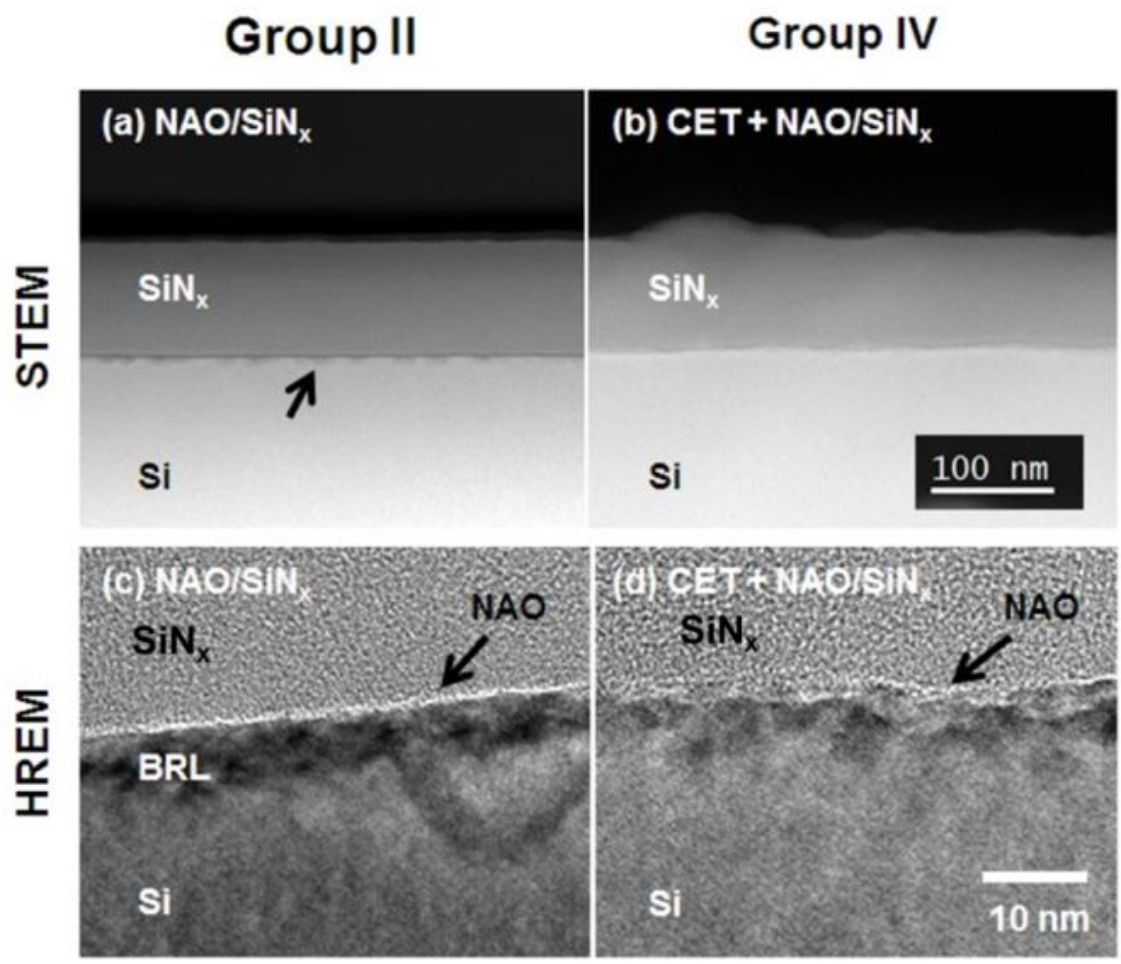


Figure 6.4 STEM and HREM images obtained from the symmetric NAO/SiNx passivated boron emitter (SiNx-NAO-p+-n-p+-NAO-SiNx) structure : (a) STEM of NAO/SINx passivated p+ emitter with BRL, (b) STEM of NAO/SiNx passivated p+ emitter with BRL removed, (c) HREM of NAO/SiNx passivated p+ emitter with BRL, and (d) HREM of NAO/SiNx passivated p+ emitter with BRL removed.

6.4 Investigation of the BRL at the Si Interface by Auger Electron Spectroscopy (AES)

AES depth profiling of key elements was performed near the interface of the group II and IV samples to reveal the change in chemical composition of the Si interface before and after the BRL removal by CET. Group II sample, with the BRL present, showed two different Auger peaks corresponding to boron and oxygen elements at the Si interface as shown in Figure 6.5(a). The boron concentration of the interface was found to be above $1x10^{20}$ cm^{-3} because boron detection limit of our AES is about $1x10^{20}$ cm^{-3}. Therefore, the combination of TEM and AES analysis of group II sample indicates that the light thin layer and the dark thin layer with periodic agglomeration underneath [Figure 6.4(c)] correspond to the chemical-oxide (NAO) and BRL, respectively. Also, notice that the boron peak at the interface of the group IV sample disappeared after the BRL etch [Figure 6.5(b)], demonstrating that CET used in this study was effective in removing the BRL.

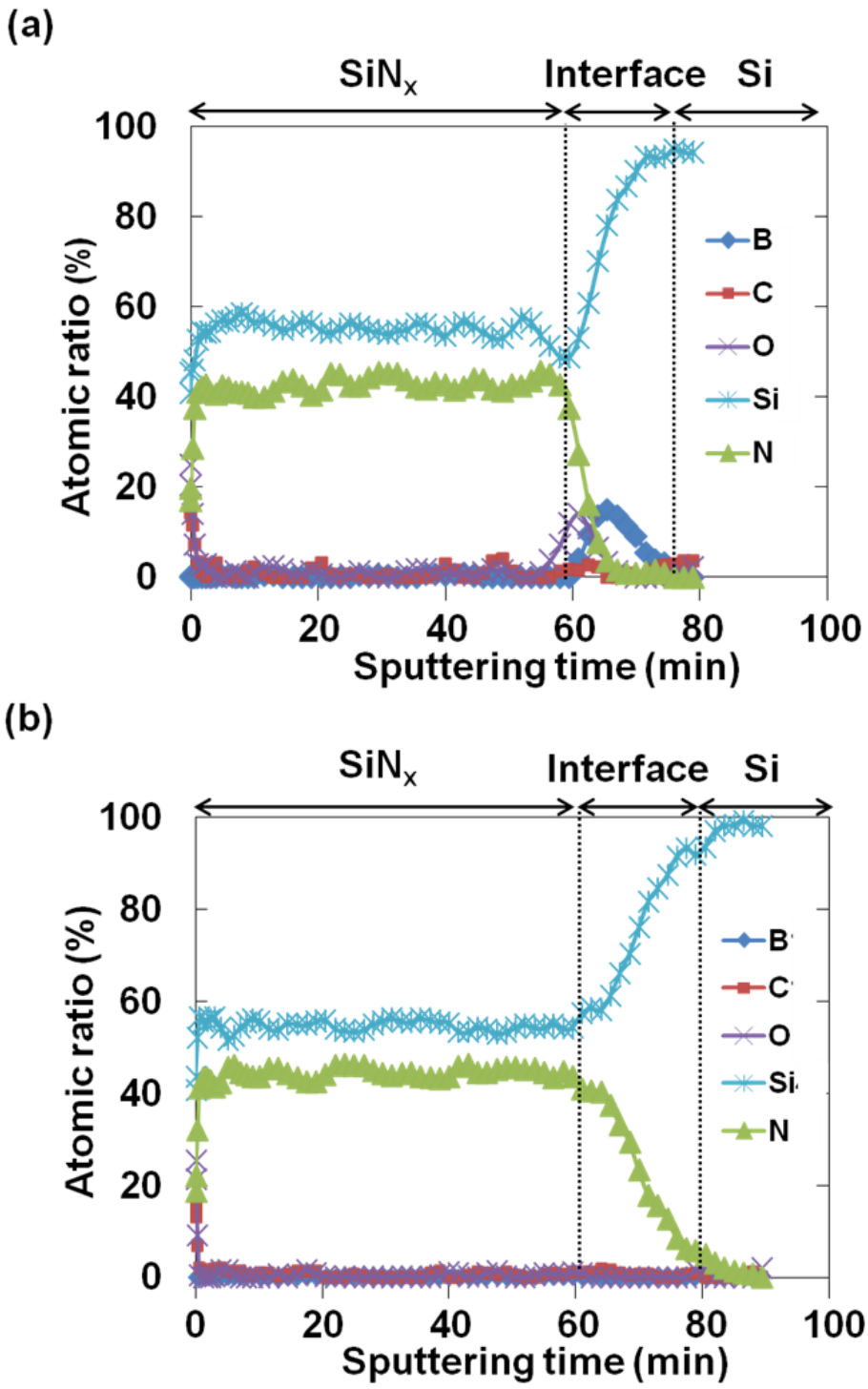


Figure 6.5 AES depth profiling analysis measured from the symmetric structure sample in (a) group II and (b) group IV.

6.5 Analysis of the 19.0% N-type PERT Solar Cell

To obtain deeper insight into the front and rear surface passivation of the 19.0% n-type cell, emitter reverse saturation current density (J_{0e}), base reverse saturation current density (J_{0b}), and surface recombination velocities (SRV) were quantitatively analyzed by a combination of device characterization and PC1D modeling. Note that J_{0e} was subdivided into $J_{0e\text{-}pass}$ and $J_{0e\text{-}metal}$ which are associated with passivated emitter surface and metallized emitter surface region, respectively. The $J_{0e\text{-}pass}$ of 100fA/cm^2 was obtained directly from the QSSPC measurement on symmetric structure. J_{0b} was calculated from the following equation :

$$J_{0b} = \frac{qn^2{}_iD_P}{N_DL}\left[\frac{BSRV\cdot\cosh\left(\frac{W}{L}\right)+\frac{D}{L}\cdot\sinh\left(\frac{W}{L}\right)}{\frac{D}{L}\cdot\cosh\left(\frac{W}{L}\right)+BSRV\cdot\sinh\left(\frac{W}{L}\right)}\right] \quad (6.1)$$

where the electronic charge q=1.6 x 10^{-19}, the hole diffusion coefficient D_P=11.78cm^2/s, the wafer thickness W=190μm, the background doping concentration N_D=9.2 x 10^{14}cm^{-3}, and the intrinsic carrier concentration n_i=8.6x10^{9}cm^{-3} [29]. The front surface recombination velocity of 20,000cm/s and the back surface recombination velocity (BSRV) of 15cm/s were extracted by numerical modeling in PC1D which involves matching the measured short- and long- wavelength IQEs shown in Figure 6.3. This gave a J_{0b} of 400fA/cm^2. Finally, a V_{oc} of 642mV was calculated from the extracted J_{0e} and J_{0b} using the following equation :

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{J_{SC}}{J_{0e}+J_{ob}}+1\right) \quad (6.2)$$

The calculated value of 642mV agreed very well with the measured cell V_{oc} of 644 mV, supporting the analysis of the cell.

The low J_{0e} and high IQE response of group IV cells in the 350-650nm wavelength range demonstrate that the chemically grown oxide/PECVD SiN_x stack can provide excellent passivation of B emitter formed by the inkjet printing followed by chemical etching of the BRL. However, literature on a thermally grown SiO_2/SiN_x stack on boron emitter suggests some instability resulting in significant loss in V_{oc} up to 100 mV after 2 years [68]. Therefore, we re-measured the *I-V* characteristics of the 19.0% n-type cell after 11 months, but saw no appreciable loss in V_{oc} and J_{sc} (0.1 mA/cm^2 loss). This is also consistent with the results reported by Das and supports the passivation stability of the oxide/nitride stack for p^+ emitters [69]. Next few chapters will focus on raising the efficiency to 21% through fundamental understanding and process optimization.

6.6 Summary

In chapter 6, a chemical etching process was developed to remove the harmful BRL as an alternative to the thermal oxidation which leads to unwanted bulk lifetime degradation. In addition, this chapter showed a positive synergistic effect of passivating the BRL-free boron emitter surface with nitric acid-grown oxide (NAO) capped with PECVD SiN_x. The combination of chemical etching and NAO/SiN_x passivation resulted in low $J_{0e\text{-}pass}$ of $100fA/cm^2$ without the degradation in bulk lifetime. This resulted in a large area (239 cm^2) n-type Cz Si solar cell with 19.0% conversion efficiency, compared to the 17.4% cells at the start of this research with the BRL and SiN_x passivation. Remainder of the thesis will focus on fundamental research and technology innovation to achieve the efficiency target of 21%.

Chapter 7 : TECHNOLOGY DEVELOPMENT AND FABRICATION OF HIGH EFFICIENCY N-TYPE COMMERCIAL SIZE SILICON SOLAR CELLS WITH FOUR PROMISING B EMITTER TECHNOLOGIES

Research on n-type solar cells with inkjet printed B emitter was very helpful in developing a basic process sequence and fundamental understanding of BRL which can have significant impact on bulk lifetime and J_{0e}. In the previous chapter, 19% efficiency was achieved which is still well below the target efficiency of 21%. Therefore, research was conducted in this chapter to understand the loss mechanisms and develop technologies to enhance V_{oc}, J_{sc}, and FF.

Since the inkjet printing of B is not yet commercially available partly due to high cost of the liquid source and low throughput, we decided to explore four additional promising and commercially viable B emitter technologies to drive cell efficiency to 21%. These technologies include (a) spin coating, (b) screen printing, (c) ion-implantation, and (d) APCVD. All these boron emitter formation technologies are currently being investigated for commercialization of n-type Si solar cells. Thus, the objective of this chapter is to develop new technology and cell designs and re-optimize the process sequence for each technology to reduce or eliminate loss mechanisms identified in the previous chapters in order to improve cell efficiency further.

7.1 Four Promising Technologies for Boron Emitter Formation

In this chapter, we chose four promising B technologies including spin coating, screen printing, ion-implantation, and APCVD to form single side B emitters. All these technologies are currently being explored but there is no clear or apparent winner yet. Table 7.1 summarizes the n-type PERT solar cells reported in the literature at the start of this research using these emitter technologies. Notice that besides emitter technology, different material, design, and process conditions (size, Si material, cell structure, surface passivation, etc.) were used by various investigators which makes it hard to determine which emitter technology is superior and more manufacturable. For example, Das *et al.* and Barth *et al.* reported on 4cm^2 20.3% [69] and a 241cm^2 19.3% [70] n-type front junction Cz Si solar cells, respectively, using spin-on boron dopant source. Ryu *et al.* showed a 239cm^2 19.6% n-type Cz Si solar cell using screen printed B emitter [71]. Yuguo *et al.* [72] and Boscke *et al*. [48] recently reported on 239cm^2 20.2% and 20.5% efficient ion-implanted n-type Cz Si solar cells, respectively. Benick *et al.* [73] also reported a 4cm^2 22.7% fully implanted PERT n-type solar cell. Finally, Rothhardt *et al.* [74] showed a 15.6x15.6cm^2 19.6% bifacial n-type Cz Si solar cell with B emitter formed by APCVD technique. However, these differences in cell conditions make it difficult to evaluate and compare different boron emitter technologies. Furthermore, no systematic study has been conducted on commercial ready > 20% efficient n-type solar cells with only difference in the B emitter formation. This chapter proposes to do so for the first time using spin coating, screen printing, ion-implantation, and APCVD B emitters while keeping the Si substrate size and all other cell processing steps identical.

Table 7.1 Efficiencies of n-type solar cells formed by different B technologies.

Boron technology	Author	Description	η
Spin coating	Das *et al.*	4cm^2, 3Ω•cm, FZ, screen printing, SiO_2/SiN_x passivation [69]	20.3%
	Barth *et al.*	241cm^2, 3Ω•cm, Cz, screen printing, bifacial, AlO_x/SiN_x passivation [70]	19.3%
Screen printing	Ryu *et al.*	239cm^2, 5Ω•cm, Cz, screen printing, SiO_x/SiN_x passivation [71]	19.6%
Ion implantation	Tao *et al.*	239cm^2, 1~6Ω•cm, Cz, screen printing, SiO_2/SiN_x passivation [72]	20.2%
	Boscke *et al.*	15.6x15.6cm^2, 1~6Ω•cm, Cz, screen printing, bifacial, Al_2O_3/SiN_x passivation [48]	20.5%
	Benick *et al.*	4cm^2, Cz, Al2O3/SINx/MgF2 passivation, photolithography, Ti/Pd/Ag for front contact [73]	22.7%
APCVD	Rothhardt *et al.*	156x156mm, 3~6 Ω.cm, Cz, screen printing, bifacial, Al_2O_3/SiN_x passivation [74]	19.6%

7.2 Advanced Process Development for N-type PERT Solar Cell for Higher Efficiency

In this chapter, an advanced manufacturing process was developed and used to improve cell efficiency further. In the previous chapter, co-annealing of B and P diffused regions limited the optimization of the two regions because B emitter requires higher temperature (≥1000°C) for full activation of B and lower J_0 while P, which is a fast diffuser, showed the annealing at lower temperature (≤900°C) to maintain high surface concentration for good ohmic contact. Co-annealing was done at 950℃ resulting in sub-optimum boron emitter and P back surface field. In this chapter, we decided to use separate anneals for B and P at 1000℃ and 840℃, respectively. This also allowed us to grow a thermal oxide, instead of NAO during the second P anneal. Thermal oxide should provide better passivation for B emitter. The process flow is illustrated in Figure 7.1. As shown,

the process (named “Dual anneal”) consists of more steps than the simple processing (“Co-anneal”) used in chapter 6. Both processes start with the texturing of wafers followed by a RCA clean. However, in “Dual anneal” process, boron emitter was first formed by using various B technologies such as spin coating, screen printing, ion-implantation, and APCVD followed by B annealing process at ~1000℃. After the B emitter formation, chemical etching treatment was performed to remove BRL. It was found that each B technology introduces a different thickness of BRL so chemical etching time was adjusted accordingly. This process will be shown later in this chapter. Next, rear planarization process was performed using following steps: 1) SiN_x deposition on front side, 2) potassium hydroxide (KOH) etching, and 3) SiN_x removal. Then, the P dopant was implanted on the planar rear side and activated by a second P annealing step at ~840℃. During the P annealing, thermal oxide layer (SiO_2) was grown in-situ on both Si surfaces for surface passivation. After the P annealing and in-situ oxidation, PECVD SiN_x layer was deposited on the SiO_2 to serve as the AR coating. The front grid and rear point contacts were screen-printed using silver-aluminum (Ag/Al) and Ag pastes, respectively, followed by a rapid co-firing step at ~700℃. A silver reflector was then printed on top of the rear screen printed point contacts followed by a short low temperature drying step. The final structure of n-type solar cell fabricated using the above process sequence (“Dual anneal”) is shown in Figure 7.2. This structure is referred to front junction PERT solar cell composed of B emitter on the textured front, P-BSF on the planar back, oxide/nitride stack on front and back for surface passivation, and screen printed Ag/Al grid on the front and screen printed Ag local contacts to the P-BSF on the rear.

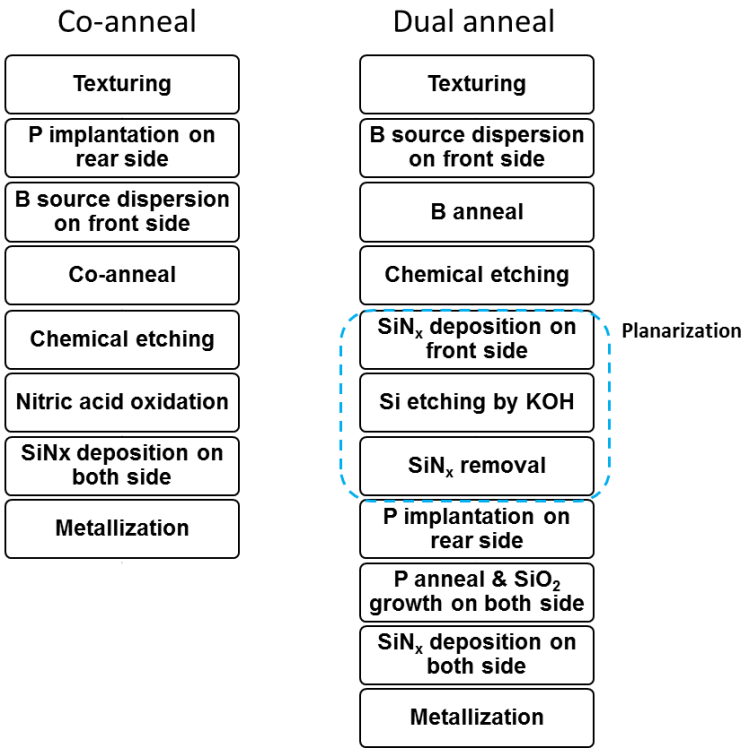


Figure 7.1 N-type PERT solar cell process flows.

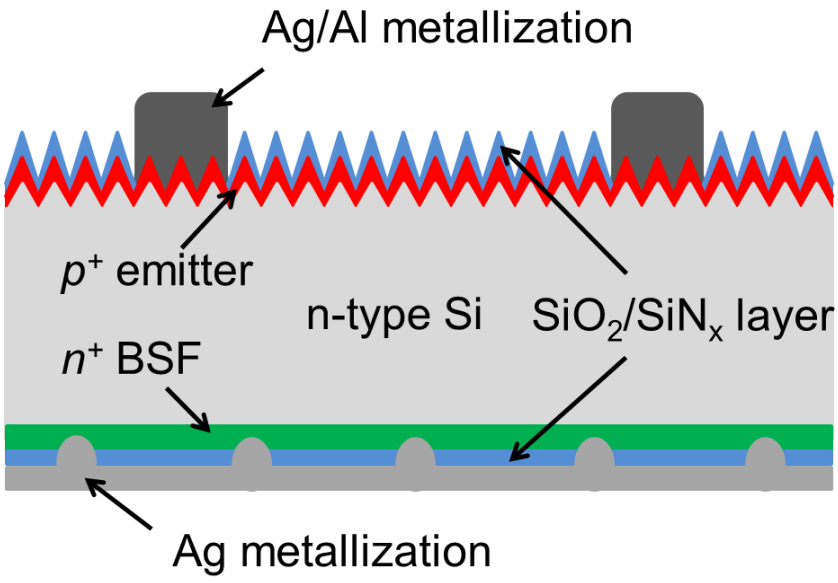


Figure 7.2 Schematics of n-type PERT solar cell structure.

7.3 Advantages of the Above Advanced Manufacturing Process for N-type PERT Cell

This section explains in more detail why the advanced manufacturing process (Dual anneal) was implemented for fabricating n-type PERT solar cells, instead of the "co-anneal" process used in chapter 6 which gave 19.0% efficiency. The major limiting factor in 19% cell was a low FF of 76%. This is attributed to too low rear surface doping concentration ($\sim 5x10^{19}cm^{-3}$) due to 950℃ co-anneal as shown in Figure 7.3(a). Screen-printed contacts generally require P surface doping concentration $\geq 1x10^{20}$ cm^{-3} for a good ohmic contact [53]. Such low surface concentration resulted in greater than $1\Omega \bullet cm^2$ series resistance (R_s) in the 19% cell bringing the FF down to 0.76%. In addition, P-doped surface was also subjected to BRL chemical etching process which also partly etched the rear P-doped Si surface to lower the P concentration even further. To prevent P BSF from the chemical etching and maintain high surface concentration, separate anneals were performed for each dopant activation. After the B emitter formation, the chemical etching was carried out for BRL removal and then the P BSF was formed at 840℃. This process sequence provides more control and sufficient surface phosphorus doping concentration ($\sim 1.5x10^{20}cm^{-3}$), as shown in Figure 7.2(b), to achieve a good screen-printed contact. In addition, a rear side planarization process was added prior to P implantation which consists of 3 steps : 1) SiN_x deposition on front side, 2) KOH etching for rear planarization, and 3) SiN_x removal. This is because the planar rear surface is known to give boost to V_{oc} and FF, compared to textured surface [72] due to low surface recombination velocity and reduced parasitic shunt effect from P BSF [17].

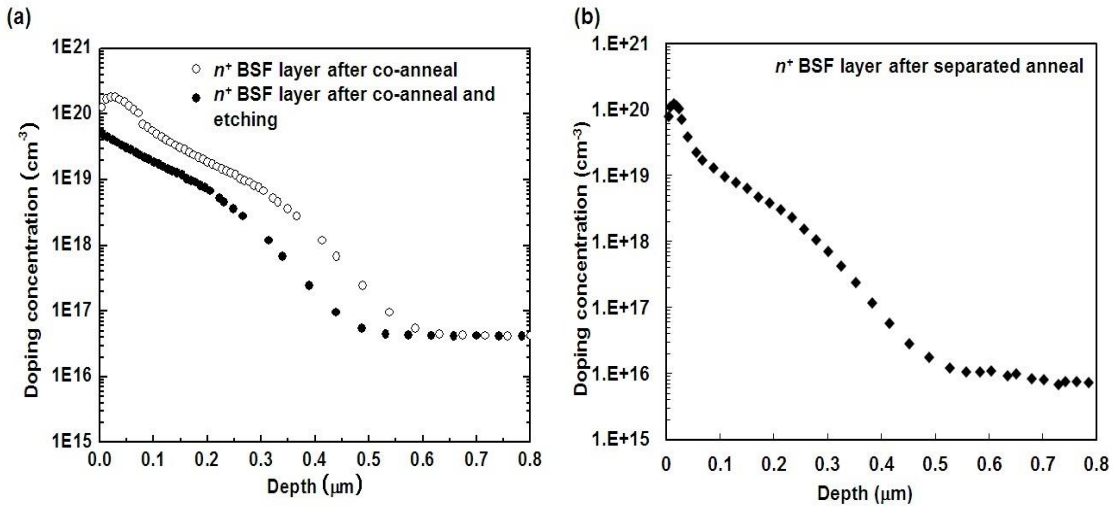


Figure 7.3 Phosphorus doping concentration after (a) co-anneal and (b) dual anneal process.

The advanced manufacturing process was implemented in this chapter in an attempt to improve cell efficiency further by solving the P BSF issues and a better B emitter with lower J_{0e}. As a result, a significant improvement in cell efficiency (mainly in FF) was achieved with efficiency exceeding 20%.

7.4 ≥20% N-type PERT Solar Cells with Different B Emitter Technologies

After developing the advanced process sequence described above, n-type PERT solar cells were fabricated. Four different technologies including spin coating, screen printing, ion-implantation, and APCVD were used for B emitter formation. After the B emitter formation, BRL on top of the B emitters was removed by the chemical etching. The BRL etching time was tailored for each diffusion technology due to the different BRL thickness for different B emitter technologies.

Table 7.2 shows the *I-V* results of n-type PERT solar cells with B emitters formed by spin coating, screen printing, ion-implantation, and APCVD technique. To highlight the

impact of BRL on each technology, cells were fabricated with and without BRL removal in Table 7.2. Note that the best cell efficiencies were in the range of only 19.7% to 19.9% for all four B emitter technologies without the BRL removal. However, compared to the 19% cell achieved in chapter 6, efficiency enhancement in this section is attributed to the increased FF from 76% to over ~ 79% due to the optimized BSF and improved screen printed contacts. As explained in chapter 7.3, the improvement in FF was accomplished by a planar rear surface with higher P surface doping concentration.

The second group of cells in Table 7.2, which involved BRL removal by chemical etching step, gave slightly higher efficiences in the range of 20.0% to 20.2% for all four B technologies. It is noteworthy that no appreciable difference was observed in the cell efficiency of all four technologies. With the exception of ion-implantation at the time (2013), these were score of the highest reported efficiencies for large area n-type PERT Cz Si solar cells with front B emitters fomed by spin coating, screen printing, and APCVD. These results indicate the potential of all four boron technolgoies for commercial use in terms of efficiency. However, cost, throughput, and yield needs to be evaluated to pick the winner.

Table 7.2 *I-V* of n-type PERT solar cells with B emitter formed by different technologies.

		Emitter formation	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Without BRL removal prior to 2nd anneal	Best	Spin coating	645	38.93	79.0	19.8
	Average		645	38.72	78.7	19.7
	Best	Screen printing	644	38.39	79.5	19.7
	Average		643	38.05	79.5	19.5
	Best	Implantation	641	38.93	79.6	19.9
	Average		640	38.71	79.6	19.7
	Best	APCVD	642	38.82	79.3	19.8
	Average		640	38.68	79.3	19.6
With BRL removal prior to 2nd anneal	Best	Spin coating	648	38.90	79.1	20.0
	Average		648	38.77	79.0	19.9
	Best	Screen printing	650	38.77	80.1	20.2
	Average		649	38.50	79.8	20.0
	Best	Implantation	650	39.23	79.2	20.2
	Average		649	39.11	79.1	20.1
	Best	APCVD	652	39.10	79.3	20.2
	Average		649	39.07	79.1	20.0

7.5 The Optimization of Chemical Etching Process for BRL Removal for Each B Diffusion Technology

Table 7.2 showed that the cell efficiency improved by 0.2 % to 0.5% after the BRL removal by the chemical etching which was optimized for each B diffusion technology. To do this, n-type solar cells with four different technologies were fabricated and subjected to different chemical etching time for BRL removal. Out of the four B technologies, the screen printing of B paste was chosen for in-depth analysis. Table 7.3 summarizes the *I-V* results of this technology for different chemical etching time in the range of 0 to 8 min. The V_{oc}, J_{sc}, FF, and efficiency are plotted in Figure 7.4 as a function of BRL etching time to gain a better understanding of the trend.

Table 7.3 Summary of *I-V* results of screen-printed B n-type solar cells with different chemical etching time.

Etching time	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]	n-factor	R_{SERIES} [Ω-cm^2]	R_{SHUNT} [Ω-cm^2]
0 min	644	38.18	79.5	19.5	1.06	0.46	4127
2 min	646	38.34	79.5	19.6	1.06	0.49	5755
4 min	649	38.53	79.8	20.0	1.06	0.51	8014
6 min	646	38.66	78.9	19.7	1.13	0.53	6518
8 min	641	38.86	77.7	19.4	1.14	0.69	7103

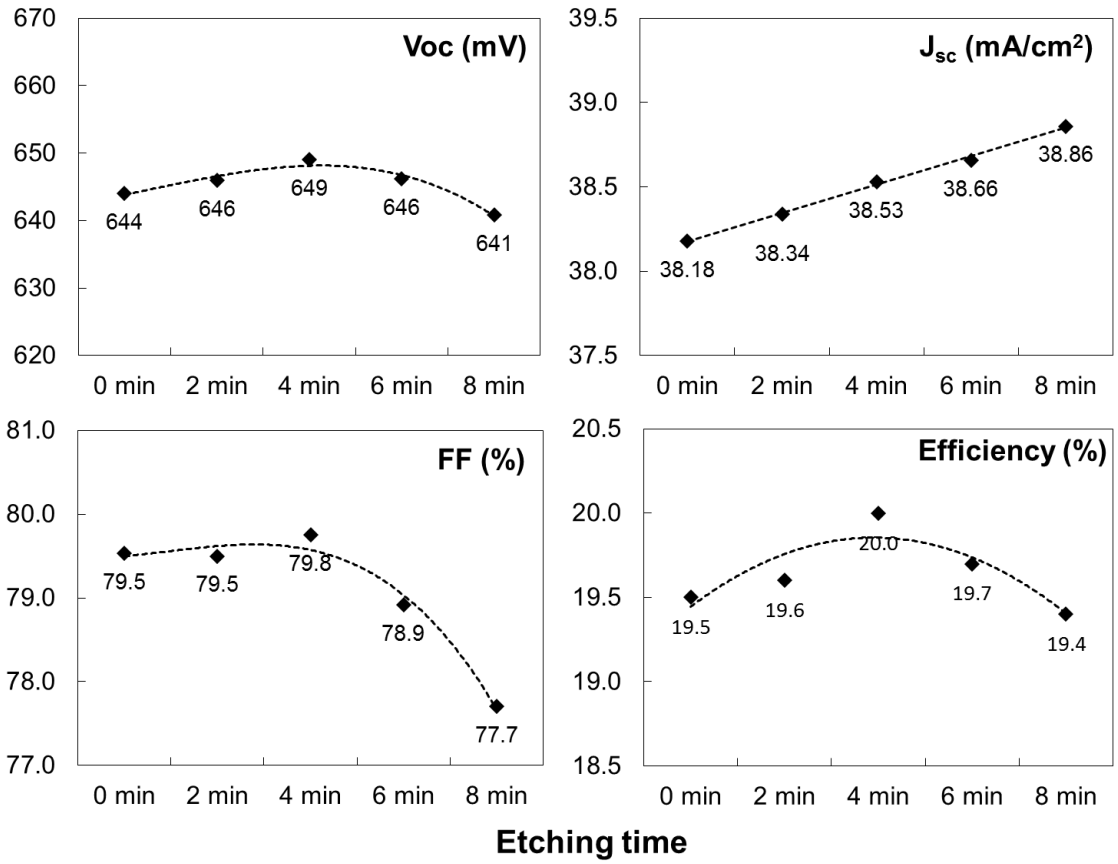


Figure 7.4 *I-V* results of n-type cells with screen-printed B emitter as a function of etching time.

Note that as the etching time increases, J_{sc} increases linearly while V_{oc} increases slightly until an etching time of ~4min and then the performance starts to decrease. The FF remains similarly until 4min, but after that it sharply decreases. The performance decrease after 4 minutes is more noticeable in FF than V_{oc}. Figure 7.5 shows that cell efficiency increase is dictated by J_{sc} until 4 minutes and after that FF decreases sharply.

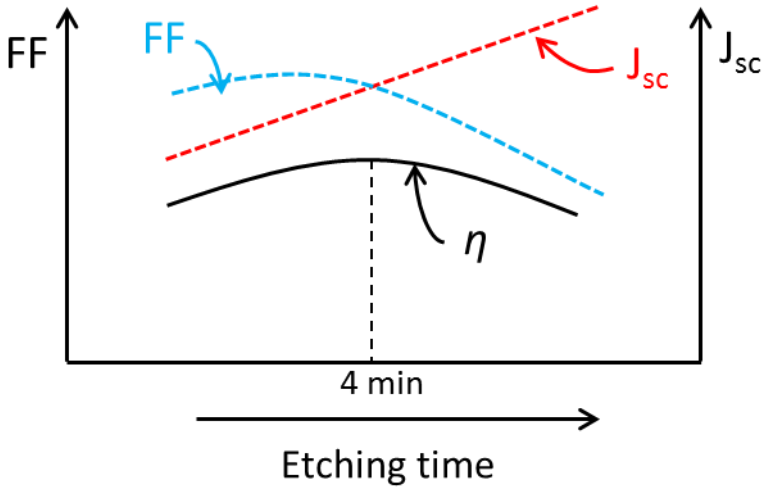


Figure 7.5 Diagram of changes in cell performance with the increased etching time.

7.6 The Impact of Chemical Etching of BRL on the IQE of N-type PERT Solar Cell

Internal quantum efficiency (IQE) measurements in Figure 7.6 confirm that the increased J_{sc} with the increased etching time is due to higher short and long wavelength response of the cells. The increased IQE response in the short wavelength is attributed to reduced front surface recombination velocity (FSRV) while the increase long wavelength response is attributed to better bulk lifetime. The reduced FSRV is attributed to the gradual removal of BRL which interferes with surface passivation. The increased bulk lifetime is attributed to reduced injection of impurities into Si during the second anneal and oxidation

as the BRL is gradually removed. Recall that in chapter 5, it was shown that the BRL acts as a source of impurities. Thus, as the etching time increases, bulk lifetime at the end of cell processing increases and hence the IQE response in the long wavelength (Figure 7.6).

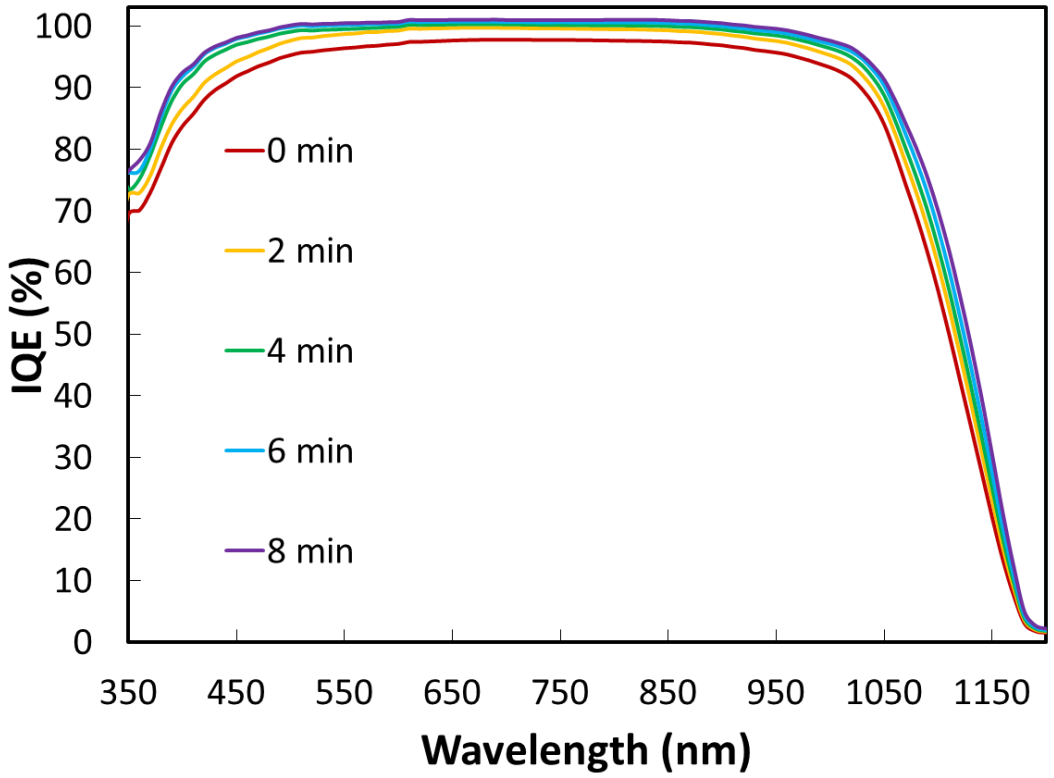


Figure 7.6 IQE response of n-type solar cell with the increased etching time.

After 4min of etching the performance drops because of FF degradation. This can be explained by the fact that 4 min of etching was sufficient to remove the BRL completely but beyond that it starts to etch the B emitter. This increases the sheet resistance and reduces the surface concentration, resulting in poor contact, high series resistance (R_s), lower FF, and lower η. TEM images in chapter 4 showed that the BRL exists in the form of agglomerations with different size. A model is proposed in Figure 7.7 which indicates that

initial rise in efficiency results from the gradual removal of BRL which reduces the injection of impurity as well as surface recombination. After 4 min, it starts to etch the Si emitter which lowers the surface concentration. This is supported by Figure 7.8 which shows TEM images of screen-printed B emitter with different etching time from 0 to 4min. As shown in Figure 7.8(a), the BRL exists in the form of agglomerations of different size. After 2 min etching, the smaller agglomeration regions were removed. Finally, the remaining agglomerations were completely removed after 4min etching.

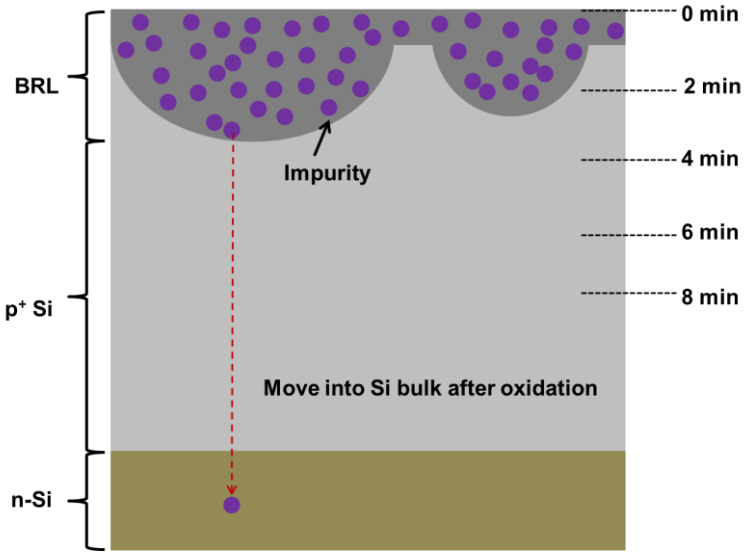


Figure 7.7 The chemical etching of BRL and B emitter formed by the screen printing technique.

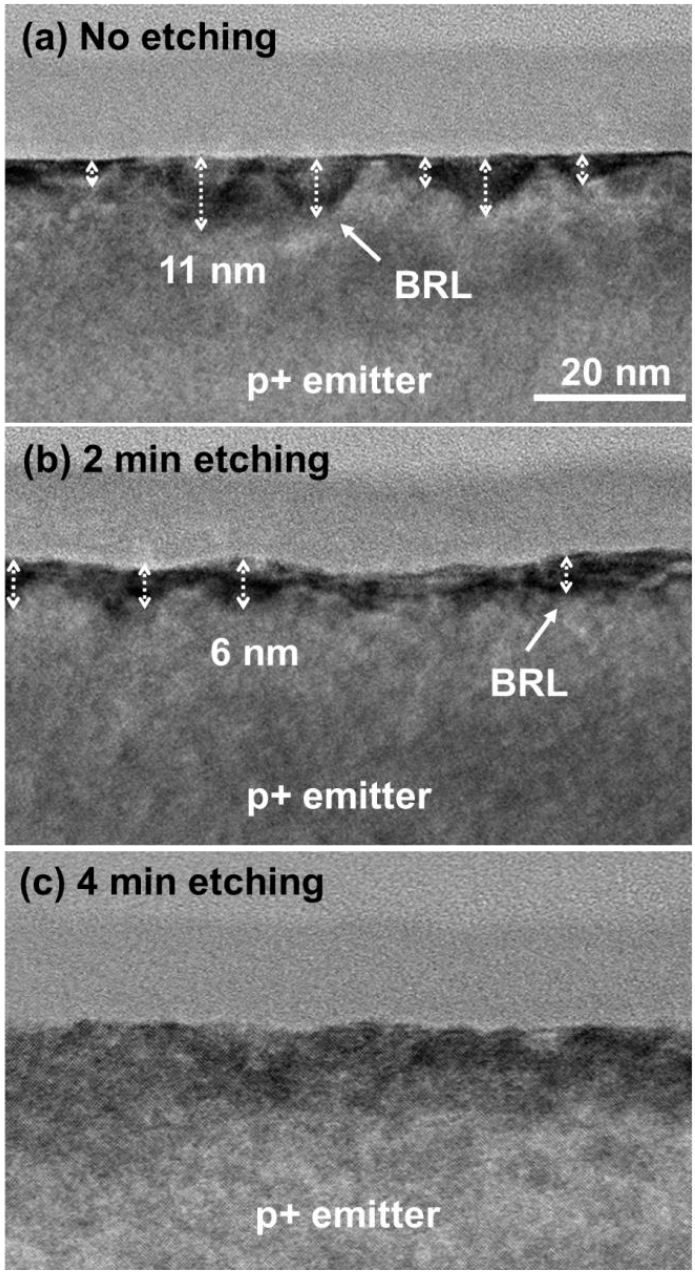


Figure 7.8 TEM images of cross section of boron diffused Si with different etching times for (a) 0 min, (b) 2min, and (c) 4min.

7.7 The Impact of Over Etching of BRL on N-type Solar Cell Parameters

Figure 7.9 shows the measured boron emitter sheet resistance and R_s of the n-type PERT solar cells as a function of etching time. The boron emitter sheet resistance increases

only slightly up to 4 minute etching time. However, after that, the sheet resistance increases sharply. Measured R_s follows the slope or trend in sheet resistance. This abrupt change in the slope after 4 minutes indicates that it starts to etch off the B emitter underneath the BRL. This increases both the sheet resistance and R_s. Table 7.3 shows that over-etching BRL after 4 min also showed an increase in the ideality n-factor from 1.06 to 1.14. This may be the result of thinning the emitter, which may lead to junction leakage due to metal spiking when firing the screen printed contacts. Higher n-factor also lowers the FF. It is important to note that optimum etching time may be process and technology dependent, so BRL etching time needs to be optimized for each case.

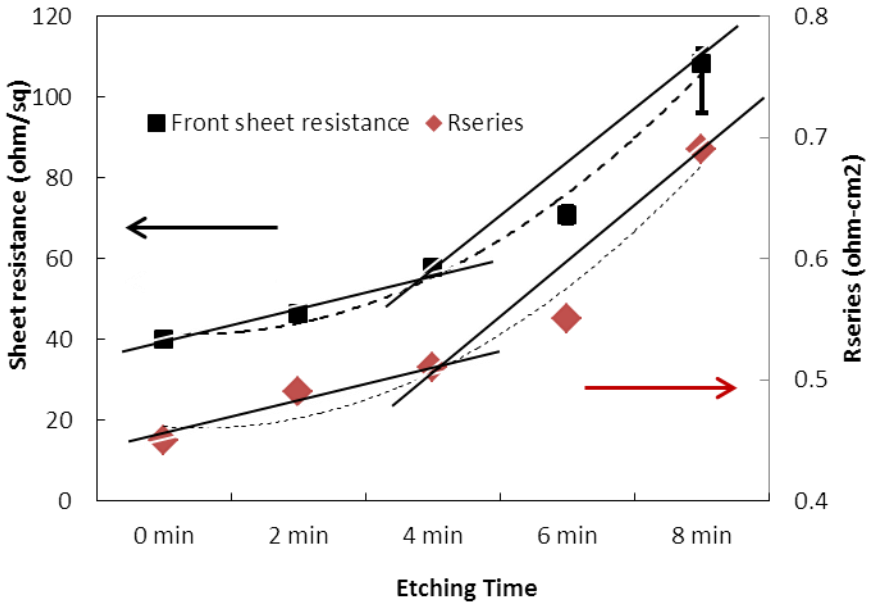


Figure 7.9 B emitter sheet resistance and R_s of n-type solar cells as a function of etching time.

7.8 Quantitative Impact of Increased R_s and n-factor on FF due to BRL over Etching.

The impact of the series resistance and n-factor on the FF can be calculated by the following equations [75].

$$\mathrm{FF} = FF_o(1 - r_s) \tag{7.1}$$

where r_s is the normalized resistance (R_s/R_{CH}) and the R_{CH} is the characteristic resistance given by V_{oc}/I_{sc}. FF_o is the ideal (maximum) fill factor and defined by :

$$FF_o = \frac{v_{oc} - \ln(v_{oc} + 0.72)}{v_{oc} + 1} \tag{7.2}$$

$$v_{oc} = \frac{V_{oc}}{(\frac{nkT}{q})} \tag{7.3}$$

where v_{oc} is a normalized voltage. Thus, higher the n-factor or R_s, smaller the fill factor. The effect of R_s and n-factor due to BRL over etching was calculated from the measured R_s and n values in Table 7.3. The calculated and measured FF are shown in Figure 7.10. The same trend is observed, but with a slight offset. Next, chemical etching optimization was performed for other three B technologies in the subsequent section.

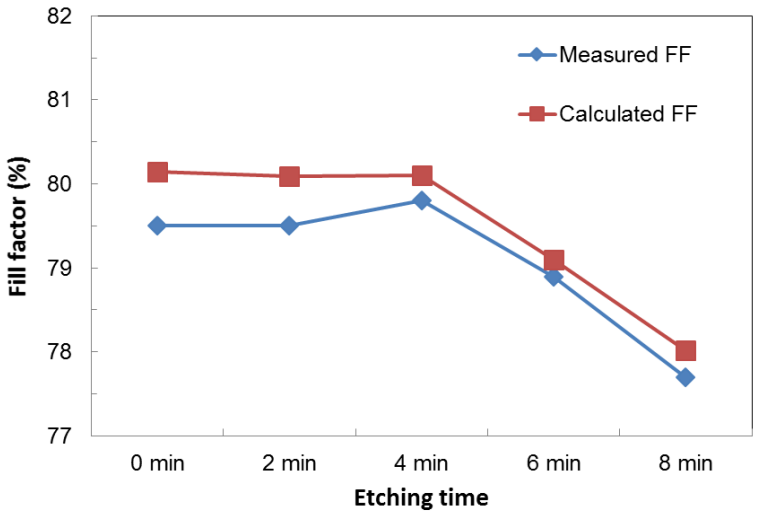


Figure 7.10 Comparison between the measured and calculated fill factor.

7.9 Optimization of Chemical Etching Time for Each Boron Technology

In order to find the optimized etching time for each B technology, n-type PERT solar cells with different B emitters were fabricated as a function of BRL etching time. Figure 7.11 shows the efficiency trend for each B technology. As expected, the cell efficiency increases initially for all cases and then decreases after the optimum BRL etching time. The optimized etching times for spin coating, screen printing, ion-implantation, and APCVD were found to be 30s, 240s, 120s, and 180s, respectively. This is attributed to different BRL thickness. The corresponding average efficiencies were 19.9%, 20.0%, 20.1%, and 20.0%. The best cell efficiencies for each technology was 20.0%, 20.2%, 20.2%, and 20.2%, respectively. Figure 7.11 also suggests that the spin coating technology forms the thinnest BRL while screen printing technology has the thickest BRL.

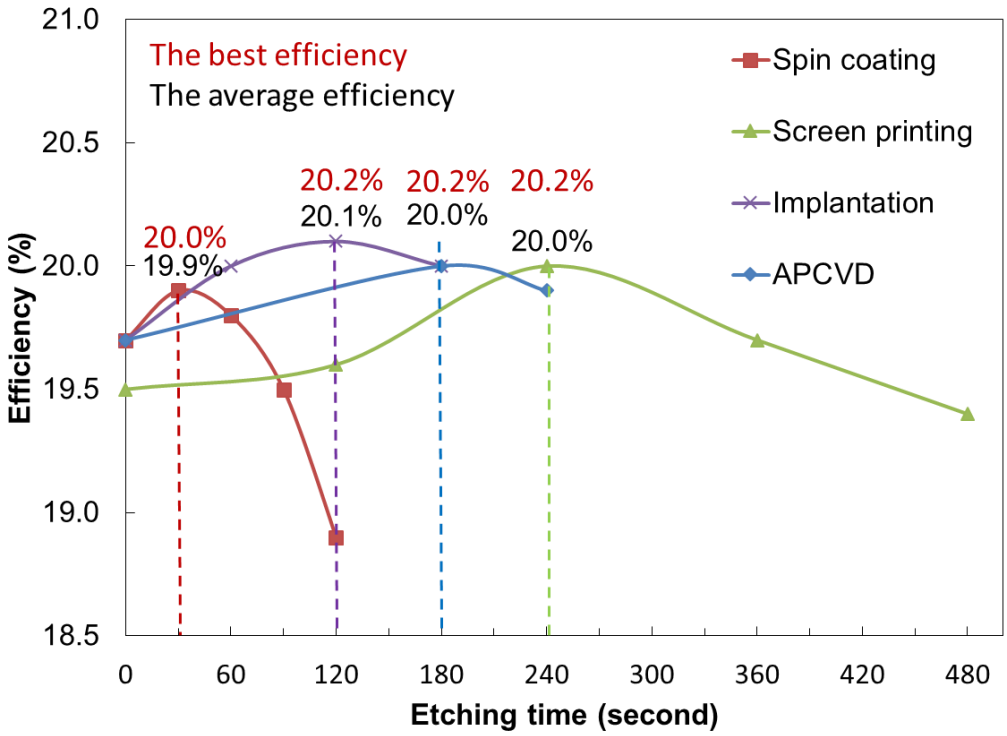


Figure 7.11 Efficiency trends of four different B technologies as a function of etching time.

7.10 Investigation of J_{0e} and Bulk Lifetime of the N-type PERT Solar Cells with Different B Emitter Technologies

In this section, $J_{0e\text{-}pass}$ of the passivated regions (between the metal gridlines) and bulk lifetime of the above n-type cells were measured. Figure 7.12(a) shows the $J_{0e\text{-}pass}$ for each B emitter technology. The symmetrical structures ($SiN_x/SiO_2/p^+/n/p^+/SiO_2/SiN_x$) were used for the measurement for $J_{0e\text{-}pass}$. About ~ 85fA/cm^2 of $J_{0e\text{-}pass}$ was achieved for the three B emitters formed by spin coating, ion implantation, and APCVD, which is close to our target J_{0e} for 21% efficiency as shown in the model calculations in chapter 4. The screen printed emitter had a higher J_{0e} (~ 109fA/cm^2) value due to higher doping concentration. Figure 7.12(b) shows bulk lifetime of n-type solar cell with each B emitter. For the bulk lifetime measurement, the test samples with the cell structure ($SiN_x/SiO_2/p^+/n/n^+/SiO_2/SiN_x$)

were prepared and then subjected to simulated contact firing without metallization. After the firing, the passivation stack and heavily-doped regions were etched away and the etched Si surface was passivated by I/M solution prior to lifetime measurement by QSSPC technique. Over 1ms bulk lifetime was achieved in all four emitter technologies, which also meets the target bulk lifetime (>1ms) for 21% efficiency shown in chapter 5. Even though the J_{0e} and bulk lifetime meet the condition for 21%, the cell efficiency achieved in this chapter is below the target efficiency of 21%. Table 7.4 showed a comparison of all the key parameters of the 20.1% fabricated cell and the 21% modeled cell. It is clear that in spite of achieving the J_{0e} and bulk lifetime required for 21% cell, 20.1% cell has higher metal recombination and lower FF. Therefore, next chapter will focus on the development and optimization of metallization for contact formation in order to bridge the gap between the 20.1% and 21% efficiency.

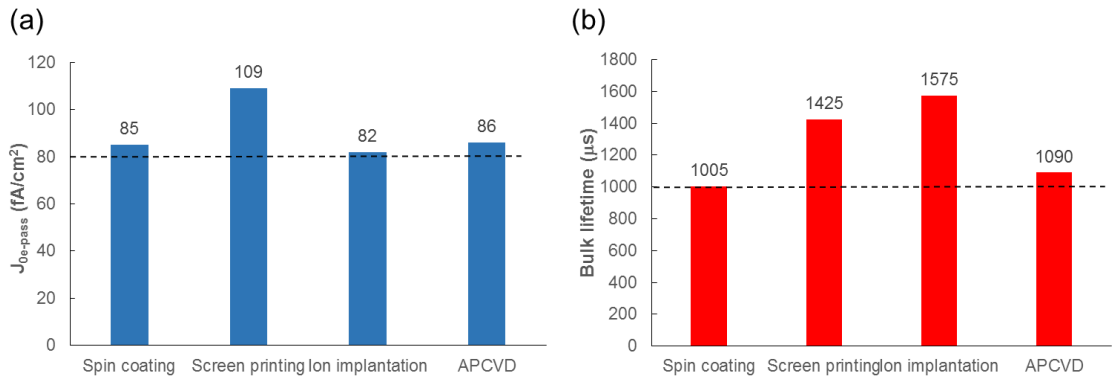


Figure 7.12 (a) $J_{0e\text{-}pass}$ of each B emitter passivated by SiO_2/SiN_x stack and (b) bulk lifetime of n-type Si wafer with 1st anneal for each B diffusion, 2nd anneal, and SiN_x passivation, and simulation firing.

Table 7.4 Comparison of key parameters of the implanted 20.1% cell and the 21% simulated cell.

Cell parameters	Simulated 21% cell	Implanted 20.1% cell	Unit
Resistivity	5	5	Ω.cm
Thickness	200	175	mm
Front reflectance	7	7.5	%
Bulk lifetime	1000	1500	μs
J_{0e}	80	~80	fA/cm^2
BSRV(n_n^+)	5	**12**	cm/s
Total R_s	0.45	**0.65**	Ω-cm^2
Efficiency	21.0	20.1	%

7.11 Summary

By developing technologies and optimizing solar cell fabrication process involving dual annealing for B and P dopants, rear surface planarization, and chemical etching for BRL removal, greater than 20% efficient n-type PERT cells with screen-printed contacts were achieved on commercial grade 239 cm^2 n-type Cz Si wafers. This represents over 1% (absolute) efficiency enhancement over the single anneal process developed in chapter 6 which resulted in 19% efficiency. In addition, for B emitter formation, spin coating, screen printing, ion-implantation, and APCVD technologies were utilized and compared in this chapter. The etching process for the BRL removal was optimized for each technology. It was found that the maximum cell efficiency is achieved when only the BRL is etched away. Under etching the BRL results in inferior surface passivation, V_{oc} and J_{sc} while over etching degrades cell efficiency due to increase in R_s and n-factor. Due to different BRL thickness, the optimized etching times for spin coating, screen printing, implantation, and APCVD were 30s, 240s, 120s, and 180s, respectively. The corresponding best efficiencies were 20.0%, 20.2%, 20.2%, and 20.2%. This chapter also shows nearly the same efficiency

potential of the four B diffusion technologies for high efficiency commercial-ready n-type PERT solar cells up to the efficiency of 20%. However, more research needs to be done to drive this efficiency toward 21%. Ion-implanted cell technology is selected in the next chapter to achieve 21% efficiency through device modeling and further technology enhancements.

Chapter 8 : TECHNOLOGY DEVELOPMENT AND OPTIMIZATION OF METALLIZATION FOR ACHIEVING ~21% EFFICIENT N-TYPE PERT CELL

In chapter6, we attained 19% efficient n-type cell by using a co-anneal process for B and P diffusion. In chapter 7, we raised this efficiency to 20.2% by implementing dual anneal process, rear planarization, and thermal oxidation for surface passivation. In this chapter, attempts are made to drive the cell efficiency to 21%. Measured cell parameters and model calculations in chapter 7 revealed that this can be achieved by reducing contact shading and metal recombination, and increasing the FF. Therefore, this chapter will focus on the development and optimization of metallization for contact formation that can accomplish this task. In this chapter, ion-implantation technology for B emitter formation will be selected for the development of metallization and ~21% efficient cell.

This chapter involves three additional technology developments : (1) modeling and optimizing the front grid design to reduce series resistance, (2) sputtering of aluminum by physical vapor deposition (PVD) in combination with laser opening of dielectric stack on the rear side for reduced metal contact area, and (3) implementation of the floating busbar on the front to reduce the metal contact recombination.

8.1 Analytical Model for Optimizing the Front Gird Design to Reduce R_s and Increase Fill Factor

In this section, an analytical model for optimizing the front grid pattern was developed. This requires experimentally measured parameters of the reference cell. The

20.1% efficient ion-implanted n-type PERT cell will be used as the reference and then the grid pattern will be modified to lower R_s. The model uses the measured cell parameters and appropriate equations to first calculate all the components (busbar resistance, gridline resistance, front and back contact resistance, sheet resistance, substrate resistance) of the series resistance (R_s), Figure 8.1, as a function of desired grid design (number and width of fingers and busbars). In addition, the model uses the R_s value to calculate cell output parameters such as FF, J_{sc}, and V_{oc}, and cell efficiency by accounting for the change in resistive and shading loss as a function of grid design.

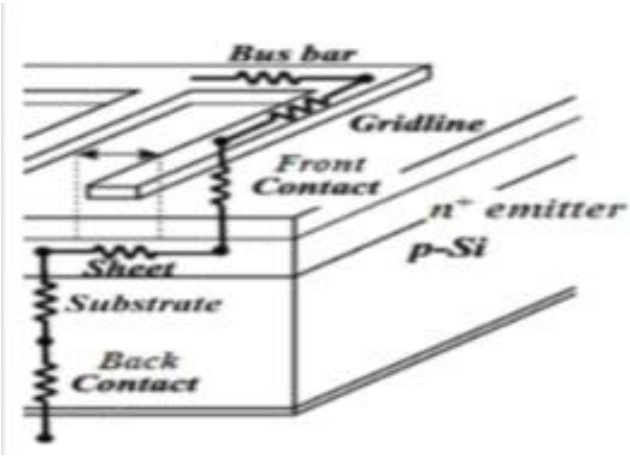


Figure 8.1 Components of series resistance of solar cell.

8.1.1 Series Resistance (R_s) Optimization

The model uses the methodology developed by Meier [76, 77] as used to calculate all the components on R_s from the experimentally determined parameters of the reference cell. Figure 8.2 shows the diagram of a rectangular cell with three busbar. This has an elementary subcell "a" units long and "2nb" units wide, with "n" grid lines having spacing

of “2b”. For a full cell “s” units long, the length of the subcell (a) is $s/(sn_{bb})$, where n_{bb} is the number of busbars.

For the 20.1% reference 6 inch cell design with 100 gridlines and 3 busbars, the unit cell has the length of 2.6 cm (a), width of 1cm (2nb), and finger spacing of 0.15 cm (2b). Current pick-up probes in a cell tester are assumed to have a spacing equal to the subcell width (2nb). The expressions used to calculate six components of R_s are summarized in Table 8.1 [78].

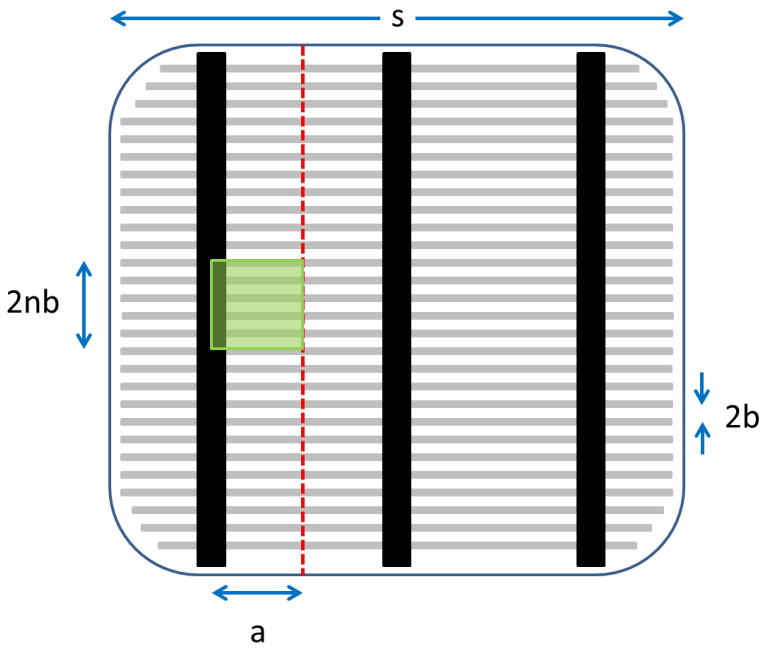


Figure 8.2 Diagram of an industrial solar cell with three busbar. Green square represents the unit cell for the analysis.

Table 8.1 Expression of six series resistance components for a ion-implanted n-type PERT cell.

Component	Expression
Front busbar	$R_s(busbar)=(1/3)a(n+1)(n+2)b^2(2R_{bus}/s)$
Gridlines	$R_s(gridline)=(1/3)(abn_{gl})BBR$
Emitter Sheet	$R_s(sheet)=(1/3)b^2R_{sheet}$
Substrate	$R_s(substrate)=\rho_w t_w$
Front contact resistance	$R_s(front\ contact)=\rho_{fc}/f_{fm}$
Back contact resistance	$R_s(back\ contact)=\rho_{bc}/f_{bm}$
Total series resistance	$R_s(total)=[V_{oc}/J_{sc}][(PFF-FF)/PFF]$

In this study, ion-implanted n-type PERT cell was analyzed, which has ~ 65μm wide Ag/Al fingers in combination with ~90Ω/sq homogeneous emitter. The measured input parameters from the cell are summarized in Table 8.2.

Table 8.2 Experimentally measured parameters of the 20.1% ion-implanted n-type PERT cell.

Parameter	Description	Value
n_{bb}	Number of busbars	3
a	Length of gridline per unit cell	2.6cm
2b	Grid line spacing	0.15cm
n	Gridlines per nit cell	6
n_{gl}	Total gridlines	100
l	Total length of gridline	15.6cm
w	Grid line width	70μm
2w'	Width of front busbar on cell	1.5mm
R_{sheet}	Emitter sheet resistance	100Ω/sq
ρ	Wafer resistivity	5Ω•cm
t_w	Wafer thickness	170μm
BBR	Busbar to busbar resistance	0.088Ω
R_{bus}	Busbar resistance	0.16Ω
J_{sc}	Measured short-circuit current density	39.1mA/cm^2
V_{oc}	Measured open-circuit voltage	649mV
FF	Measured fill factor	79.1 %
R_s	Measured series resistance	0.75Ω-cm^2
R_{sh}	Measured shunt resistance	7000Ω-cm^2
n	Ideality factor	1.03
Efficiency	Measured cell efficiency	20.1%
Pseudo FF	Pseudo fill factor measured by Suns-V_{oc}	80.3%
$J_{0e\text{-}pass}$	J_{0e} associated with passivated emitter surface	75fA/cm^2
$J_{0e\text{-}metal}$	J_{0e} associated with metalized emitter surface	1200fA/cm^2
$J_{0b\text{-}pass}$	J_{0b} associated with passivated emitter surface	70fA/cm^2
$J_{0b\text{-}metal}$	J_{0b} associated with metalized emitter surface	1300fA/cm^2
$J_{0b\text{-}bulk}$	J_{0b} from bulk	50fA/cm^2
f_{fm}	Fraction of front metal coverage	7.5%
f_{bm}	Fraction of back metal coverage	4.5%

The pseudo fill factor without the series resistance was obtained by using a Suns-V_{oc} measurement [79]. The buasbar resistance, gridline resistance, emitter sheet resistance, and substrate resistance were measured by four-point probe. The front contact resistance was determined by TLM measurement [80]. For this measurement, 1cm wide strip was laser

cut from the cell. Once these R_s components are determined, the back contact resistance can then be extracted by subtracting the sum of these components from the total series resistance. After obtaining the above parameters, various components of R_s for different number of fingers and busbars were calculated using this analytical model. The calculated results are summarized in Table 8.3. The number of busbars varied from 3 to 5 to reduce the grid resistance or grid length between the buses. Note that the busbar width was adjusted to keep the same total shading of busbars (number of busbar x width of busbar x length of busbar). The number of fingers varied in the range of 70 to 140 while keeping the finger width at 65μm. Note that the total front metal coverage (busbars + fingers) is affected by the number of fingers but not by the number of busbars.

Table 8.3 Calculated R_s and its R_s components for different number of busbars and fingers.

Grid design				Resistance (Ω-cm^2)					
Number of busbar	Width of busbar	Finger spacing (mm)	Number of finger	Busbar	Fingers	Contact	Emitter	Substrate	Total R_s
3	1.5 mm	2.20	70	0.008	0.858	0.063	0.403	0.102	1.43
		1.93	80	0.006	0.753	0.055	0.310	0.102	1.23
		1.71	90	0.005	0.667	0.049	0.244	0.102	1.07
		1.54	100	0.004	0.601	0.044	0.198	0.102	0.95
		1.40	110	0.003	0.546	0.040	0.163	0.102	0.85
		1.28	120	0.003	0.499	0.037	0.137	0.102	0.78
		1.19	130	0.002	0.462	0.034	0.117	0.102	0.72
		1.10	140	0.002	0.429	0.031	0.101	0.102	0.67
4	1.125 mm	2.20	70	0.006	0.644	0.063	0.403	0.102	1.22
		1.93	80	0.004	0.565	0.055	0.310	0.102	1.04
		1.71	90	0.004	0.500	0.049	0.244	0.102	0.90
		1.54	100	0.003	0.450	0.044	0.198	0.102	0.80
		1.40	110	0.002	0.410	0.040	0.163	0.102	0.72
		1.28	120	0.002	0.374	0.037	0.137	0.102	0.65
		1.19	130	0.002	0.347	0.034	0.117	0.102	0.60
		1.10	140	0.001	0.322	0.031	0.101	0.102	0.56
5	0.9 mm	2.20	70	0.005	0.515	0.063	0.403	0.102	1.09
		1.93	80	0.004	0.452	0.055	0.310	0.102	0.92
		1.71	90	0.003	0.400	0.049	0.244	0.102	0.80
		1.54	100	0.002	0.360	0.044	0.198	0.102	0.71
		1.40	110	0.002	0.328	0.040	0.163	0.102	0.63
		1.28	120	0.002	0.300	0.037	0.137	0.102	0.58
		1.19	130	0.001	0.277	0.034	0.117	0.102	0.53
		1.10	140	0.001	0.257	0.031	0.101	0.102	0.49

8.1.2 Calculation of the Impact of Number of Busbars and Fingers on J_{sc}, V_{oc}, FF, and Efficiency.

After determining all the R_s components for different number of busbars and fingers, their impact on J_{sc}, V_{oc}, FF, and η was assessed. As the number of fingers decreases, J_{sc} increases because of reduced shading, but the FF decreases by virtue of the increased series

resistance. In addition, V_{oc} increases with the decreased number of fingers due to the reduced recombination or the metal/silicon contact area. Thus, the optimization of the grid design involves the tradeoff between shading and series resistance.

In this study, we assumed that J_{sc} increases linearly with the reduced metal coverage and can be expressed as :

$$J_{sc} = J_{sc0} + J_{sc0}(f_{fmo} - f_{fm}) \tag{8.1}$$

where J_{sc0} is the short-circuit current density of the reference cell, f_{fm0} is the fraction of front metal coverage of the reference cell, and f_{fm} is front metal coverage to be adjusted.

The total reverse saturation current density J_0 is extracted from :

$$J_0 = (f_{fm})J_{0e-metal} + (1 - f_{fm})J_{0e-pass} + (f_{bm})J_{0b-metal} + (1 - f_{bm})J_{0b-pass} \tag{8.2}$$

where f_{fm} and f_{bm} are the fraction of front metal coverage and back metal coverage, respectively, and $J_{0e\text{-}metal}$ and $J_{0b\text{-}metal}$ represent the J_0 component associated with the front metalized surface and back metalized surface, respectively. In this study, $J_{0e\text{-}metal}$ and $J_{0b\text{-}metal}$ were found to be ~1200fA/cm^2 and 1300fA/cm^2, respectively, by using the technique described in reference [81]. $J_{0e\text{-}pass}$ and $J_{0b\text{-}pass}$ are the J_0 components associated with the unmetallized but passivated front and back passivated surface. These were attained by well documented QSSPC technique on symmetric structures with passivated B or P emitters on both sides without any metallization. This gave $J_{0e\text{-}pass}$ of 75fA/cm^2 for our B emitter and $J_{0b\text{-}pass}$ of P BSF of 70fA/cm^2 for our 20.1% reference cell. With the calculated J_{sc} and J_0 values, V_{oc} is obtained by the following equation :

$$V_{oc} = \frac{kT}{q}\ln\left(\frac{J_{sc}}{J_0} + 1\right) \tag{8.3}$$

Finally, the model calculates FF and cell efficiency using the following equations :

$$FF = FF_s[1 - \frac{(v_{oc}+0.7)FF_s}{v_{oc}r_{sh}}] \tag{8.4}$$

$$FF_s = FF_0(1 - r_s) \tag{8.5}$$

$$r_s = \frac{R_s}{R_{CH}}, R_{CH} = \frac{V_{oc}}{J_{sc}}, \text{ and } r_{sh} = \frac{R_{sh}}{R_{CH}} \tag{8.6}$$

$$FF_0 = \frac{v_{oc}-ln(v_{oc}+0.72)}{v_{oc}+1}, \text{ where } v_{oc} = \frac{qV_{oc}}{nkT} \tag{8.7}$$

$$\text{Efficiency } \eta = \frac{V_{oc}J_{sc}FF}{P_{in}} \tag{8.8}$$

The cell efficiency for various front grid designs were obtained from the above analytical model using the measured input parameters of the reference 20.1% cell. The calculated cell efficiency for different grid designs (number of gridlines and busbars) are summarized in Table 8.4 and illustrated in Figure 8.3. Notice that model predicts the optimum number of gridlines for a given number of busbars. Also, note that the 20.1% efficiency of the reference cell with 65μm wide 100 gridlines and 3 busbars is in very good agreement with the calculated efficiency which supports the accuracy of this model. Model calculations show that the cell efficiency can be increased from 20.1% to 20.4% simply by increasing the number of busbars from 3 to 5, while keeping the total area of busbars same (0.9mm wide 5 busbars as opposed to 1.5mm wide 3 busbars in the reference cell). A higher number of busbars reduces the series resistance of the front grid finger because the finger length between the two busbars is decreased. This increases the maximum attainable efficiency. Therefore, next step involved applying this five busbar grid design with 65μm side 100 gridlines to cell fabrication.

Table 8.4 Calculated J_0, J_{sc}, V_{oc}, FF, and efficiency for different number of busbar and finger based on the 20.1% reference cell.

# of busbar	# of finger	Front metal coverage	J_o (fA/cm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	η (%)
3	70	6.0%	330	39.68	655	0.761	19.78
	80	6.5%	335	39.50	655	0.771	19.95
	90	6.9%	341	39.32	654	0.779	20.06
	100	7.4%	346	39.15	654	0.785	20.10
	110	7.8%	351	38.97	653	0.790	20.12
	120	8.3%	357	38.79	653	0.794	20.11
	130	8.7%	362	38.62	652	0.797	20.08
	140	9.2%	367	38.45	652	0.800	20.04
4	70	6.0%	330	39.68	655	0.772	20.06
	80	6.5%	335	39.50	655	0.781	20.20
	90	6.9%	341	39.32	654	0.788	20.27
	100	7.4%	346	39.15	654	0.793	20.30
	110	7.8%	351	38.97	653	0.797	20.29
	120	8.3%	357	38.79	653	0.800	20.27
	130	8.7%	362	38.62	652	0.803	20.23
	140	9.2%	367	38.45	652	0.805	20.17
5	70	6.0%	330	39.68	655	0.778	20.23
	80	6.5%	335	39.50	655	0.786	20.35
	90	6.9%	341	39.32	654	0.793	20.40
	100	7.4%	346	39.15	654	0.797	20.41
	110	7.8%	351	38.97	653	0.801	20.40
	120	8.3%	357	38.79	653	0.804	20.36
	130	8.7%	362	38.62	652	0.806	20.31
	140	9.2%	367	38.45	652	0.808	20.25

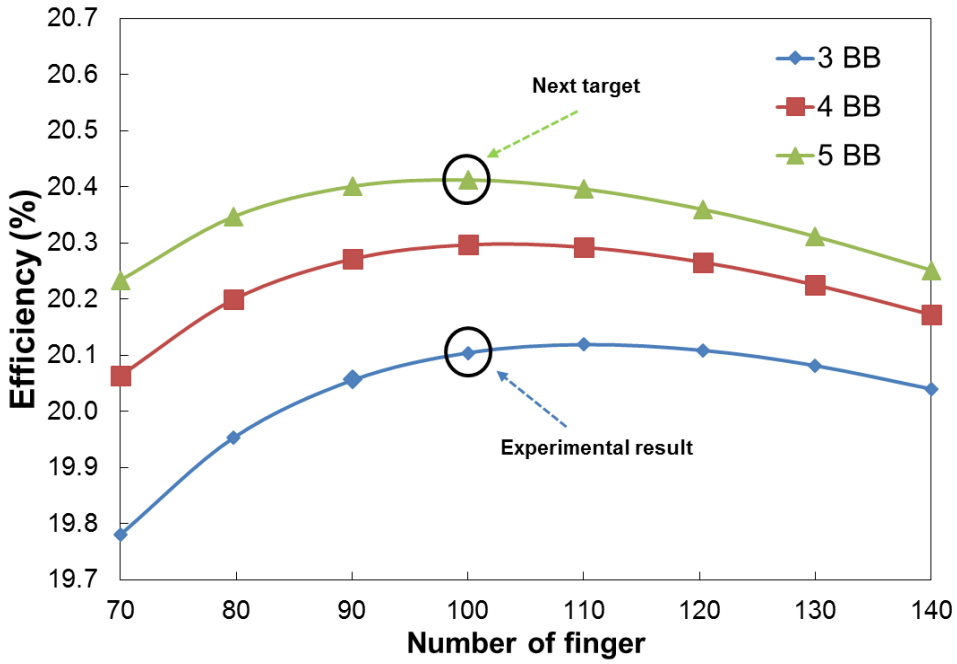


Figure 8.3 Calculated cell efficiencies with different number of busbars and fingers.

8.1.3 Application of the Optimized Front Grid Design with Five Busbars to Achieve 20.4% N-type PERT Cell.

In this section, 5 busbar grid design with 100 gridlines was used to fabricate n-type PERT solar cell to validate the model which predicts ~0.3% higher efficiency. The 3- and 5-busbar solar cells were fabricated with the dual anneal process sequence shown in Figure 7.1. Except for the front grid pattern design, all other process steps were exactly identical. Actual pictures of the cells fabricated with 3 and 5 busbars are shown in Figure 8.4 and the corresponding *I-V* results are summarized in Table 8.5.

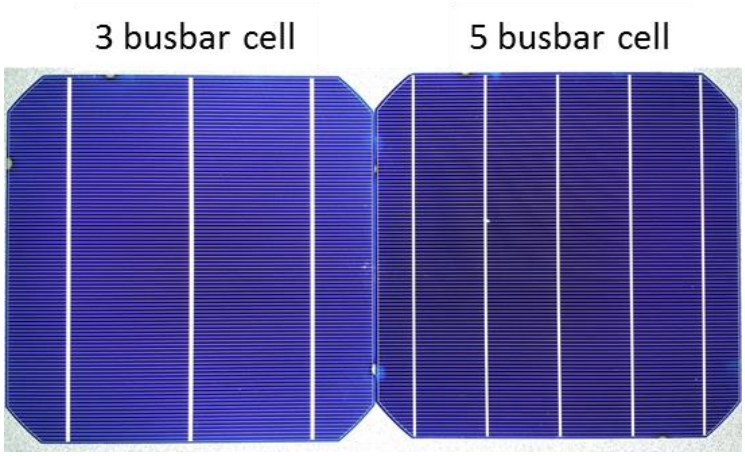


Figure 8.4 The front grid patterns with (left) 1.5mm wide 3 busbars and (right) 0.9mm wide 5 busbars.

Table 8.5 *I-V* results of n-type PERT solar cells with 3 busbars and 5 busbars.

Device ID	# of busbar	V_{oc} (V)	J_{sc} (fA/cm^2)	FF (%)	η (%)	n-factor	R_s (Ω-cm^2)	R_{sh} (Ω-cm^2)
3BB-1	3 busbar	0.652	38.83	79.36	20.1	1.03	0.72	7920
3BB-2		0.651	38.83	79.22	20.03	1.02	0.74	12000
3BB-3		0.651	38.9	79.38	20.11	1.04	0.67	12900
3BB-4		0.649	38.81	79.21	19.95	1.07	0.61	15800
3BB-5		0.650	38.76	79.2	19.94	1.07	0.65	4220
3BB-6		0.652	39.15	79.37	20.25	1.03	0.7	4500
AVG		**0.651**	**38.88**	**79.29**	**20.06**	**1.04**	**0.68**	**9557**
5BB-1	5 busbar	0.654	38.78	80.48	20.41	1.01	0.55	3590
5BB-2		0.652	38.88	80.39	20.38	1.02	0.55	13200
5BB-3		0.652	38.79	80.37	20.33	1.02	0.53	3450
5BB-4		0.652	38.89	80.57	20.43	1.03	0.51	7800
5BB-5		0.651	38.66	80.46	20.25	1.04	0.47	24900
5BB-6		0.652	38.87	80.69	20.45	1.03	0.46	11100
5BB-7		0.652	38.96	80.77	20.47	1.02	0.47	7010
5BB-8		0.653	38.79	80.54	20.40	1.04	0.49	1560
AVG		**0.652**	**38.82**	**80.53**	**20.39**	**1.03**	**0.50**	**9076**

The experimental results in Table 8.5 are entirely consistent with the model which predicted higher FF and ~0.33% increase in absolute cell efficiency for the 5 busbars. The 3 and 5 busbar cells resulted in an average efficiency of 20.06% and 20.39%, respectively.

8.2 Formation of Rear Point Contacts Formed by Laser Opening and Physical Vapor Deposition of Al to Reduce Contact Recombination.

This section focuses on the next technology enhancement associated with reducing the rear contact recombination. Reference cell used 120μm wide 500μm apart screen-printed fire-through Ag metal contacts on rear side with metal coverage of 4.5%. Here, we propose to open smaller contact windows by laser first followed by the sputtering of aluminum (Al) by physical vapor deposition (PVD) for the formation of rear point contacts. This should reduce the metal recombination on the back because metal coverage can reduce from ~4.5% to 1.4% by 40μm wide laser openings with 300μm spacing. Therefore, in this section, n-type PERT solar cells with the same process sequence except the back contacts will be fabricated by laser opening and PVD Al metallization to enhance cell efficiency.

8.2.1 Fabrication of N-type PERT Cell with Rear Contacts Formed by Laser Opening and PVD Al

Figure 8.5 shows the comparison of process flow for the rear contact formation by screen-printing of Ag and PVD of Al. PVD Al metallization process first received the Ag/Al grid formation on the front by screen printing followed by firing. Then the rear SiO_2/SiN_x passivation stack was opened to form of dot pattern using a UV laser with an appropriate pulse energy. The diameter of the laser opening was 40μm along with 300μm

spacing compared to 120μm size screen printed dots with 500μm spacing in the 20.4% cell. Then, approximately ~1μm thick Al film was sputtered by the PVD on the entire rear side. This reduced the back metal/Si contact coverage to 1.4% compared to 4.5%. Finally, the PVD cells received a short annealing at a temperature of ~ 400 ℃ in a belt furnace to form a good ohmic contact on the rear side.

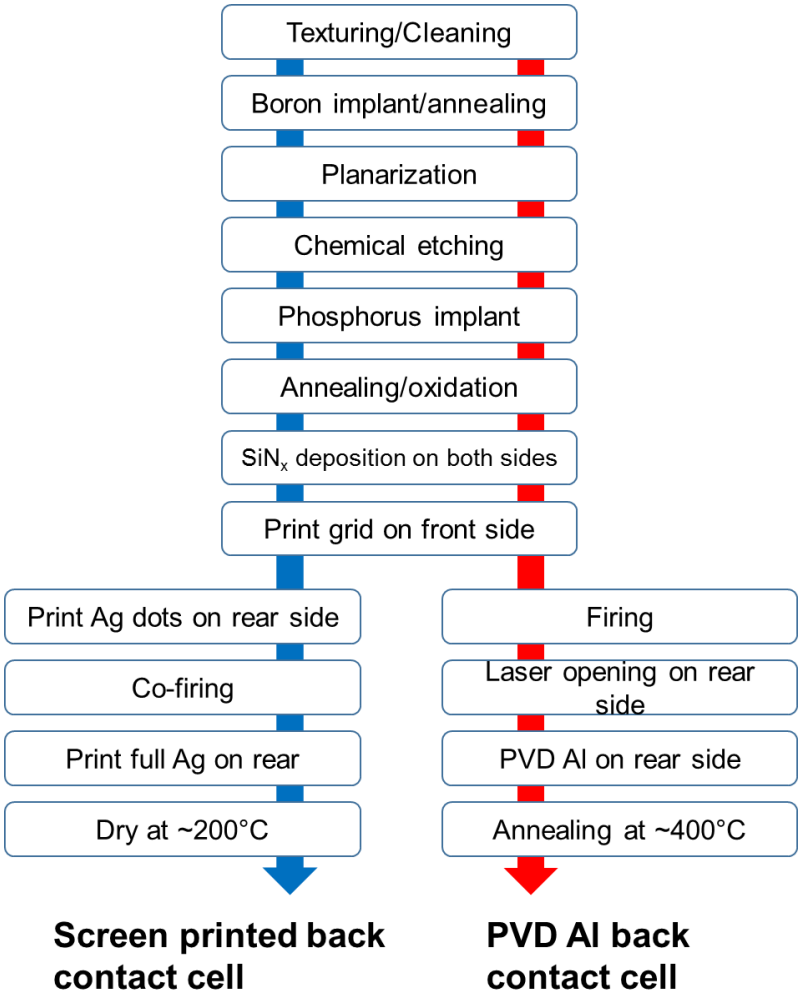


Figure 8.5 Comparison of process flow for the rear contacts formed by screen-printing and physical vapor deposition (PVD) Al.

The n-type PERT cells with PVD Al rear point contacts were fabricated and tested at AM1.5G, 100mW/cm^2. Table 8.6 shows that compared to n-type PERT cells with screen printed local contacts (Table 8.5), an improvement of 0.36% in absolute efficiency was achieved from the cells with PVD Al rear contacts. The data supports that the reduced metal-induced recombination on the rear side resulted in an increase in V_{oc}. Since the reduced recombination on the rear side reduces back surface recombination velocity and it should also give a slightly higher long wavelength IQE response [82]. Furthermore, PVD Al contact showed slightly higher FF, which is attributed to the combination of a reduced n-factor and improved V_{oc}, as shown by equation 8.7. These improvements resulted in average cell efficiency of 20.75% with a V_{oc} of 658mV, J_{sc} of 38.97mA/cm^2, and FF of 80.91%. The best cell efficiency was 20.84% with a V_{oc} of 659mV, J_{sc} of 39.05mA/cm^2, and FF of 80.99%. This is one of the highest efficiency reported to date for n-type PERT cell with screen printed front contact on 239cm^2 commercial grade Cz silicon. The other commercial n-type cells reported and produced by various manufacturers and research groups are summarized in Table 8.7.

Table 8.6 Summary of *I-V* results for n-type PERT cell with laser opening and PVD Al on the rear metal contacts.

Device ID	V_{oc} (V)	J_{sc} (fA/cm^2)	FF (%)	η (%)	n-factor	R_s (Ω-cm^2)	R_{sh} (Ω-cm^2)
PVD Al-1	0.659	38.84	81.00	20.73	1.02	0.47	5500
PVD Al-2	0.659	38.94	80.96	20.78	1.01	0.50	4580
PVD Al-3	0.659	39.05	80.99	20.84	0.99	0.51	4260
PVD Al-4	0.657	38.78	80.93	20.62	1.00	0.49	13400
PVD Al-5	0.658	39.05	80.83	20.77	1.01	0.50	10700
PVD Al-6	0.659	39.08	80.76	20.80	1.01	0.52	4190
PVD Al-7	0.656	39.04	80.89	20.72	1.00	0.51	4710
AVG	**0.658**	**38.97**	**80.91**	**20.75**	**1.01**	**0.50**	**6763**

Table 8.7 List of commercial grade large area n-type silicon solar cells fabricated using various processing techniques.

Institute	Area (cm^2)	η (%)	Description	Ref.
Panasonic	144	25.6	SHJ-IBC cell, rear junction, back contact	[15]
SunPower	155	25.0	IBC cell	[16]
Silevo	15.6x15.6	23.1	PERT bi-facial, tunnel oxide junction, electroplated Cu	[83]
Trina Solar	15.6x15.6	22.9	IBC cell, BBr_3 & $POCl_3$ diffusion, screen-printing	[84]
Bosch	15.6x15.6	22.1	Ion-implanted IBC cell	[85]
Motech	15.6x15.6	20.6	PERT bi-facial, cost-effective IPA_free texturization	[86]
IMEC	15.6x15.6	20.5	Ni/Cu plated nPERT	[87]
MegaCell	15.6x15.6	20.4	BiSoN, PERT bi-facial technology from ISC Konstanz	[88]
PVG Solution	15.6x15.6	20.1	PERT bi-facial, p^+ emitter & n^+ BSF	[89]

Table 8.7 continued

Neo Solar Power	15.6x15.6	20.0	PERT bi-facial, p^+ emitter & n^+ BSF	[90]
Yingli	239	19.8	Panda, PERT bifacial, co-diffused p+ emitter and n+ BSF	[91]
Mission Solar	15.6x15.6	19.7	PERT bi-facial, n-Pasha technology from ECN	[92]
LG electronics	15.65x15.65	*20.5~ 21.4	Implanted PERT, 18.6% module efficiency	[93]

*Expected cell efficiency based on the module efficiency

8.3 Application of Floating Busbar to Improve V_{oc}

Since reducing the back metal/Si contact area from 4.5% to 1.4% resulted in reduced metal recombination and higher V_{oc}, in this section, floating busbars were applied on the front to reduce metal recombination or J_0 associated with the metal busbars when they are fired through the SiN_x. In the 20.84% cell in the previous section, Ag/Al grid pattern with 5 busbars and 100 fingers was screen printed and fired through the SiO_2/SiN_x stack to establish ohmic contacts to the silicon emitter. The front metal contact fraction is ~ 7.5% which introduces significant surface recombination. In the floating busbar approach, busbars make no direct contact to the silicon emitter but reside on top of the anti-reflective coating. Only the gridlines are fired through but the floating busbars are connected to the grid lines only at the intersection of busbar and gridline. Figure 8.6 illustrates the concept of floating busbars compared to regular screen-printed and fire-through busbars. This reduces the metal/Si contact fraction from 7.5% to 4.5% because the busbar coverage alone contributes to about 3%. This should reduce contact recombination and increase V_{oc}.

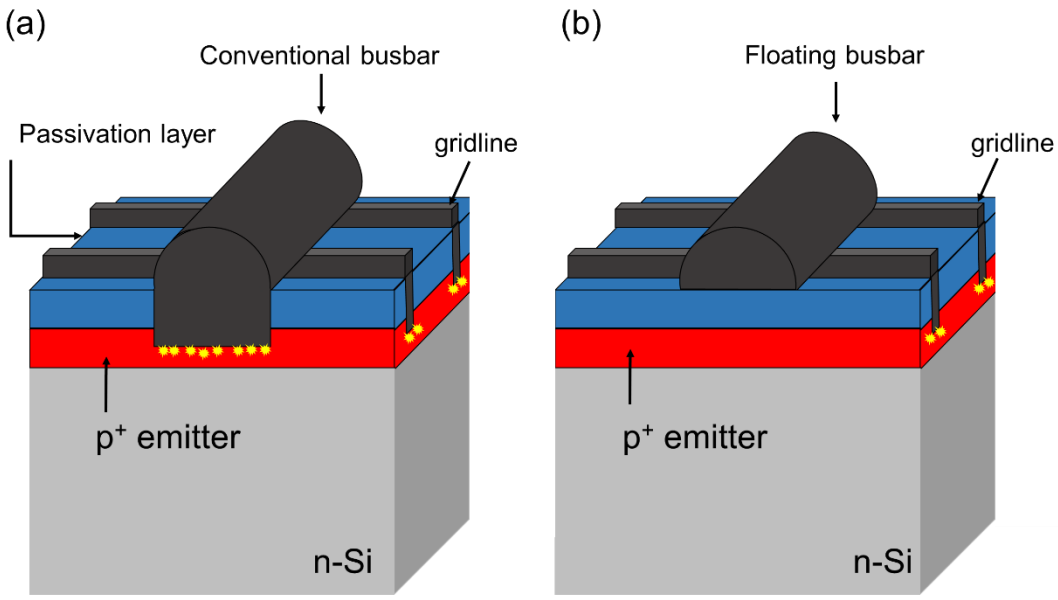


Figure 8.6 Schematic structure of (a)Fire-through busbars and (b)Floating busbars.

The expected increase in V_{oc} by applying the floating busbars can be calculated by the following equations :

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_o} + 1\right) \tag{8.9}$$

$$J_0 = (f_{fm})J_{0e-metal} + (1 - f_{fm})J_{0e-pass} + (f_{bm})J_{0b-metal} + (1 - f_{bm})J_{0b-pass} \tag{8.10}$$

Figure 8.7 shows a plot of V_{oc} vs J_0, assuming a J_{sc} of 39mA/cm^2. Since the 20.8% cell fabricated in the previous section had a V_{oc} 658mV, it corresponds to a J_0 of 295fA/cm^2 according to Figure 8.7. If the floating busbars are applied to the cell, the front metal contact fraction (f_{fm}) is reduced by 3% (7.5% → 4%). Since $J_{0e\text{-}pass}$ and $J_{0e\text{-}metal}$ are ~75fA/cm^2 and ~1200fA/cm^2, respectively, total J_0 should reduce by ~40fA/cm^2 to 255fA/cm^2 resulting in a V_{oc} of 662mV according to Figure 8.7.

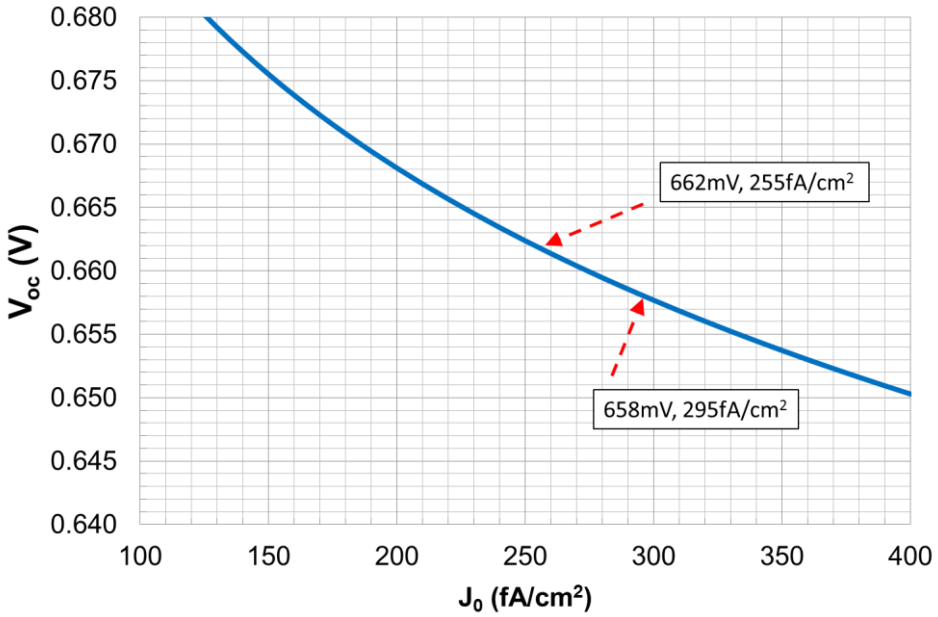


Figure 8.7 Calculation of V_{oc} as a function of total J_0.

Therefore, nPERT cells with floating busbars were fabricated with the process sequence shown in Figure 8.8. Unlike the nPERT process sequence shown in Figure 8.5, first 100 Ag/Al fingers were screen printed and fired through on the front. Then the 5 floating busbars were screen printed using a special paste from Dupont which requires curing at only 400℃ but no firing. Therefore, busbars do not fire through the SiO_2/SiN_x stack and remain floating on SiN_x on top of the emitter. Finally, rear contact metallization was done with the laser opening and PVD Al.

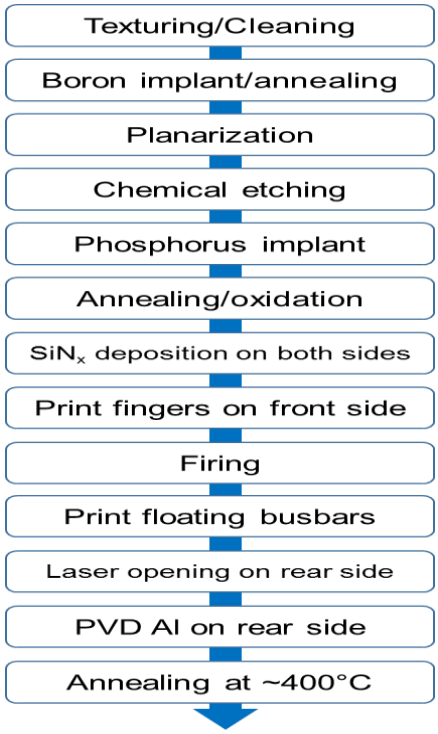


Figure 8.8 Process flow of nPERT cell with floating busbars.

Table 8.8 shows the *I-V* results of the nPERT cells with the 5 floating busbars. Average efficiency of these cells was 20.72% with a V_{oc} of 662mA, J_{sc} of 38.95mA/cm^2, and FF of 80.42%. In comparison to the 20.8% cells achieved in Table 8.6, J_{sc} remained unchanged but V_{oc} improved by 4mV, which is entirely consistent with the calculated V_{oc}. However, FF decreased slightly from ~80.9% to ~80.4% possibly due to the poor contact between busbars and grid lines when they intersect. That is why cell efficiency did not improve further in spite of the increased V_{oc}. Companies such as Heraeus and Dupont are currently developing pastes for the floating busbars to avoid this problem of FF which should raise the cell efficiency to ≥21%.

Table 8.8 Summary of *I-V* results for nPERT with floating busbars.

Device ID	V_{oc} (V)	J_{sc} (fA/cm^2)	FF (%)	η (%)	n-factor	R_s (Ω-cm^2)	R_{sh} (Ω-cm^2)
Floating BB-1	0.662	38.93	80.32	20.70	1.03	0.58	7640
Floating BB-2	0.663	38.96	80.62	20.81	1.02	0.54	9210
Floating BB-3	0.660	38.91	80.33	20.65	1.04	0.54	4710
Floating BB-4	0.661	38.99	80.42	20.73	1.04	0.54	2600
AVG	**0.662**	**38.95**	**80.42**	**20.72**	**1.03**	**0.55**	**6040**

8.4 Summary

This chapter focused on advanced metallization on the front and back through technology development and design optimization for higher efficiency cells. Advanced metallization involved three enhancements : i) optimization of front grid design with five busbars to increase FF, ii) laser opening and PVD Al to reduce rear contact recombination, and iii) introduction of floating busbars. The front grid pattern was optimized using an analytical model, which revealed 5 busbars with 100 gridlines can provide 0.33% increase in absolute efficiency. Fabrication of 5 busbar cells raised the efficiency from 20.1% to 20.4%. Second technology enhancement involved replacing the 120μm wide 500μm apart screen printed metal dots on the rear surface with laser opening of a 40μm dot pattern with 300μm spacing followed by PVD Al metallization. This reduced the back metal/Si contact area from 4.5% to 1.4%, resulting in higher V_{oc} and another 0.36% increase in efficiency.

Best cell efficiency with this technology enhancement was 20.86%. Finally, floating busbars were applied on the front to reduce the front metal/Si contact area from 7.5% to 4.5%. This did give another 4mV increase in V_{oc} but the cell efficiency did not increase because of the slightly lower FF due to the inferior busbar/gird contact resistance. Improved floating busbar paste can overcome this and provide ~21% cells.

Chapter 9 : QUANTITATIVE UNDERSTANDING AND IMPACT OF EACH TECHNOLOGY ENHANCEMENT ON CELL PARAMETERS AND EFFICIENCY THROUGH DETAILED MODELING AND CHARACTERIZATION

In the previous five chapters, all the above fundamental understanding, cell design, and technology developments were integrated into a process sequence to achieve ~21% efficient large area n-type PERT solar cell on commercial size 239 cm^2 Cz wafers. Detailed device modeling and cell characterization are used to quantitatively explain the impact of each technology enhancement on material and cell parameters for all the six generation nPERT cells (17.4%-21%) developed in this thesis. Device modeling is performed using PC1D model and cells are characterized and analyzed by light and dark *I-V*, IQE, reflectance, J_{0e}, and bulk lifetime measurements.

9.1 Summary of Technology Enhancements that Raised the N-PERT Cell Efficiency from 17.4% to ~21%.

In the previous chapters, we developed and demonstrated five technology enhancements for raising the nPERT cells efficiency. First, fundamental understanding of the formation role and impact of BRL was established. It was shown that BRL is extremely detrimental to the bulk lifetime and emitter surface passivation. This limited the 1^{st} generation baseline cell efficiency to 17.4%. 1^{st} generation cells involves co-annealing of inkjet B emitter and implanted P_BSF, no BRL removal, double side texturing, three busbars, screen printed local contacts on the back (Figure 9.1).

In the 2nd generation cells, an effective chemical etching process was developed to remove the BRL followed by a chemical grown oxide on the B emitter for passivation. BRL removal improved surface passivation and also resulted in high bulk lifetime. This resulted in 1.6% improvement in absolute efficiency raising the cell efficiency from 17.4% to 19.0%. Next, only the front surface was textured while rear surface was planarized to improve BSRV, BSR, and back contacts. In addition, dual anneals were used to optimize B emitter and P BSF profiles individually consistent with the model. This reduced the J_{0e} and J_{0b} and resulted in 3rd generation cells with average efficiency of 20.06% with best efficiency of 20.25%. For the 4th generation cells, front grid design was optimized by changing the number of busbars from 3 to 5 which reduced the grid resistance and gave higher FF. As predicted by the analytical modeling, a further improvement of 0.33% in efficiency was achieved in the 4th generation nPERT cells, resulting in 20.39% average efficiency with the best efficiency of 20.47%. Device modeling of these cells pointed out high metal recombination on the front and back which increases J_0 and reduces V_{oc}. Therefore, in the 5th generation cells, we reduced the metal/Si contact area on the back. This was accomplished by laser opening and PVD Al deposition instead of the screen printing of 120μm Ag dots and firing them through the dielectric. By opening 40μm vias through the dielectric followed by PVD Al deposition, back metal/Si contact area was reduced from 4.5% to 1.4% which reduced J_{0b} and increased V_{oc}, resulting in 0.36% boost in efficiency. Average cell efficiency was 20.75% with the best efficiency of 20.84% for the 5th generation. Finally, floating busbar technology was used on the front to reduce the metal/Si contact area by 3% to achieve higher V_{oc}. The 6th generation cells with floating busbars did show 4mV higher V_{oc} but the slight decrease in FF due to higher contact

resistance between the bus and gridlines negated the benefit of the increased V_{oc}. However, this study showed the potential of the floating busbar technique. Further development of floating busbar paste can overcome this shortcoming and raise the efficiency to ≥21%. Figure 9.2 summarizes the quantitative impact of each technology enhancements on device parameters and best cell efficiency.

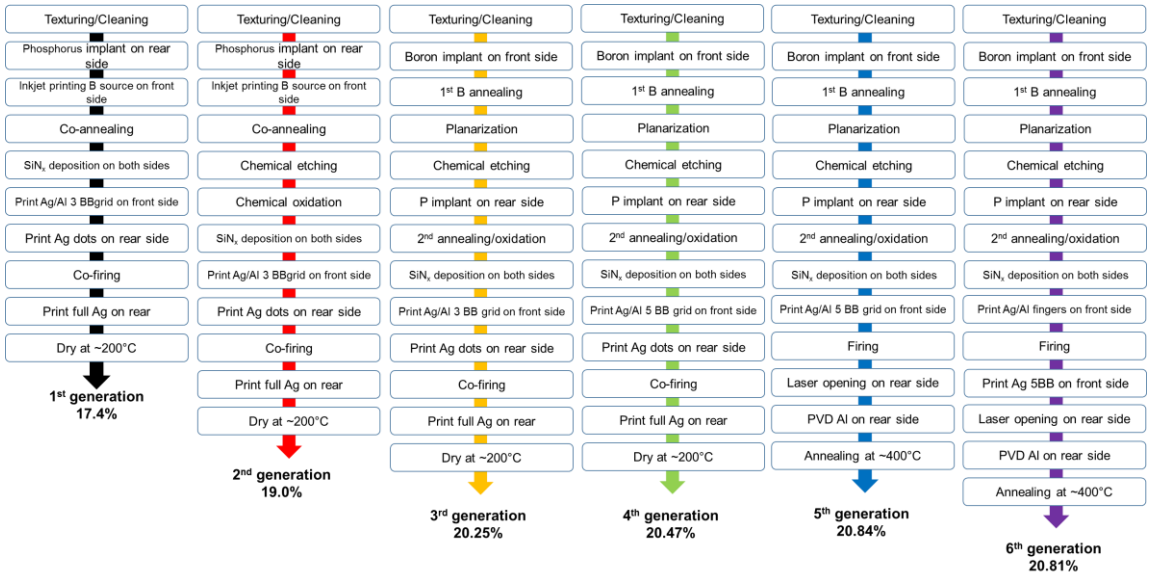
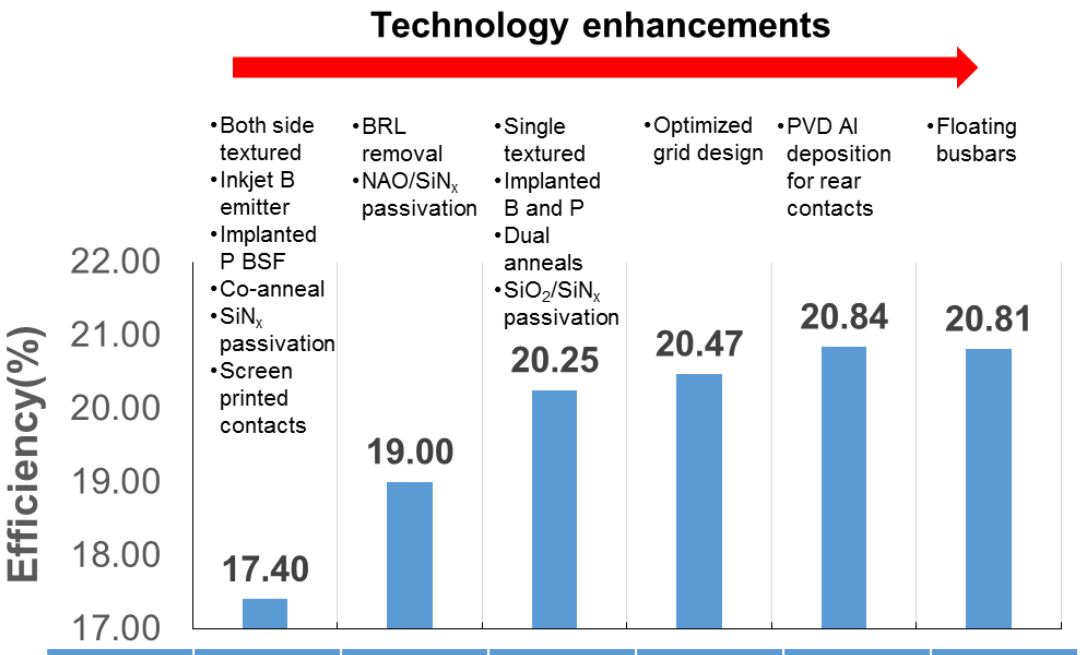


Figure 9.1 Process flow for nPERT cells of 1st to 6th generation.



	1st Generation	2nd Generation	3rd Generation	4th Generation	5th Generation	6th Generation
V_{oc} (mV)	622	644	652	652	659	663
J_{sc} (fA/cm^2)	36.70	38.60	39.15	38.86	39.05	38.96
FF (%)	0.76	0.77	0.794	0.808	0.810	0.806
η (%)	17.4	19.0	20.25	20.47	20.84	20.81

Figure 9.2 Efficiency roadmap toward ~21% on commercial grade 239 cm^2 Cz Si wafers.

9.2 Characterization Modeling and Analysis of 17.4% to 21% N-PERT Cells Fabricated in This Thesis

In this section, all the six versions of the nPERT cells developed in this thesis are extensively characterized and modeled using PC1D device modeling program to gain deeper insight into the efficiency enhancements. The objective of this section is to show quantitatively the impact of each technology enhancement on material, device, and cell parameters, in addition to the cell efficiency. Table 9.1 summarizes measured or extracted input parameters for PC1D modeling that matched the measured and modeled *I-V* as well as IQE of the best cell in each category ranging from the 1st 17.4% cell to the 20.81% 6th

generation cell. The extracted parameters for the cells are also listed in the table. Table 9.1 shows that the BRL removal by chemical etching in conjunction with NAO/SiN_x stack for surface passivation lowered the FSRV dramatically from 60000cm/s to 20000cm/s in the 2nd generation cell. The NAO/SiN_x stack for Si surface passivation also lowered the BSRV from 25cm/s to 15cm/s. Reduction in FSRV and BSRV lowered the $J_{0e\text{-}pass}$ and $J_{0b\text{-}pass}$, which increased the V_{oc} from 622mV to 644mV and J_{sc} from 36.7mA/cm^2 to 38.7mA/cm^2, resulting in a significant efficiency jump from 17.7% to 19.1%.

In the 3rd generation cell, back surface was planarized and dual anneal was implemented to independently tailor the B and P profiles. This allowed us to lower the B emitter surface concentration from $8x10^{19}cm^{-3}$ to $4x10^{19}cm^{-3}$ while maintaining high P concentration on the rear surface for good ohmic contact. Reducing the emitter surface concentration reduced the bulk Auger recombination as well as the FSRV from 20000cm/s to 6000cm/s. In addition, higher P concentration on the rear surface lowered the back contact resistance, lowered the R_s from 0.98 to 0.65Ω-cm^2, and increased the FF from 77.0% to 79.4%. Rear planarization in this device also reduced the BSRV from 15 to 12 which lowered the $J_{0b\text{-}pass}$ to increase V_{oc}. Reduction in FSRV and BSRV raised the IQE of the cell contributing to 0.6mA/cm^2 increase in J_{sc}. All these improvements gave an efficiency enhancement of 1.25% resulting in 20.25% efficient n-PERT cell.

4th generation cell involved front grid optimization which was achieved by replacing 3 busbars by 5 busbars while maintaining the same metal coverage and gridlines. This reduced the length of grid between the bus and lowered series resistance from 0.65Ω -cm^2 to 0.55Ω -cm^2, resulting in an increase in FF from 79.4% to 80.8%. Notice that V_{oc}

and J_{sc} were not affected and remained 652mV and ~39.0mA/cm^2. This FF enhancement due to 5 busbars increased the 4th generation n-PERT cell efficiency up to 20.47%.

5th generation technology enhancement addressed the back metal recombination and back contact. In 3rd generation cells, back dot contacts were 120x120μm with 500μm spacing. In this generation, back contacts were 40μm in size and 300μm apart. This reduced the metal/Si contact coverage from 4.5% to 1.4% which lowered the BSRV from 12 to 8cm/s. Reduction in BSRV lowered the J_{0b} [equal to $J_{0b\text{-}pass}$*(1-back metal coverage)+$J_{0b\text{-}metal}$* back metal coverage+$J_{0b\text{-}bulk}$] from 135 to 97fA/cm^2 and increased V_{oc} from 652mV to 658mV. Reduction in series resistance due to reduced back contact spacing also raised the FF from 80.8 to 81.0%. J_{sc} remained essentially unchanged but the efficiency went up by 0.33% to 20.84%. Seeing the success of reduced metal recombination on the back, we reduced the metal/Si contact area on the front by introducing the floating busbars which do not contact the emitter directly but reside over the AR coating. Since busbar shading area is ~3%, this concept reduces front metal/Si contact area by 3% which reduced the FSRV from 6000cm/s to 3500cm/s, resulting in a decrease in J_{0e} from 159 to 129fA/cm^2 and to ~4mV increase in V_{oc}. However, efficiency enhancement was not seen because of slightly higher contact resistance between busbar and gridlines.

Table 9.1 PC1D modeling of the nPERT cells from baseline to 5th generation.

Input parameters	1st Gen.	2nd Gen.	3rd Gen.	4th Gen.	5th Gen.	6th Gen.
Water thickness (μm)	195	195	170	170	170	170
Base resistivity (Ω-cm)	5	5	5	5	5	5
R_{series} (Ω -cm^2)	0.98	0.98	0.65	0.5	0.4	0.45
Texturing	Both sides	Both sides	Front side	Front side	Front side	Front side
Texture angle (degree)	54.74	54.74	54.74	54.74	54.74	54.74
Texure depth (μm)	3.5	3.5	3.5	3.5	3.5	3.5
Emitter surface concentration (cm^{-3})	3x10^{20}	8x10^{19}	4x10^{19}	4x10^{19}	4x10^{19}	4x10^{19}
Junction depth (μm)	0.71	0.67	0.6	0.6	0.6	0.6
τ_{bulk} (ms)	~1	~1	~1	~1	~1	~1
FSRV (cm/s)	60000	20000	6000	6000	6000	3500
BSRV (cm/s)	25	15	12	12	8	8
Front metal coverage (%)	7.5	7.5	7.5	7.5	7.5	4.5
Back metal coverage (%)	4.5	4.5	4.5	4.5	1.4	1.4
$J_{0e\text{-}pass}$ (fA/cm^2)	433	100	75	75	75	75
$J_{0e\text{-}metal}$ (fA/cm^2)	750	850	1200	1200	1200	1200
$J_{0b\text{-}pass}$ (fA/cm^2)	123	85	70	70	70	70
$J_{0b\text{-}metal}$ (fA/cm^2)	1300	1300	1300	1300	1300	1300
$J_{0b\text{-}bulk}$ (fA/cm^2)	150	150	50	50	50	50
Modeled V_{oc} (mV)	623	643	652	652	658	662
Modeled J_{sc} (mA/cm^2)	36.7	38.7	39.2	39.2	39.2	39.2
Modeled FF (%)	76.2	76.8	79	79.8	80.6	80.3
Modeled η (%)	17.5	19.1	20.2	20.4	20.8	20.8
Measured V_{oc} (mV)	622	644	652	652	659	663
Measured J_{sc} (mA/cm^2)	36.7	38.6	39.2	39.0	39.1	39.0
Measured FF (%)	76.0	77.0	79.4	80.8	81.0	80.6
Measured η (%)	17.40	19.00	20.25	20.47	20.84	20.81

9.3 Summary

By developing and integrating several efficiency enhancement features, 20.84% efficient nPERT cell was achieved on commercial grade 239 cm^2 n-type Cz Si wafers. The technology developments involved chemical etching of BRL to improve emitter surface

passivation and bulk lifetime, dual annealing of B emitter and P BSF to optimize diffused regions for lower J_0, rear side planarization for lower surface recombination and higher back reflectance, optimized grid pattern with 5 busbars for lower series resistance and higher fill factor, and laser opening and PVD Al for rear contact metallization to reduce metal coverage and improve J_{0b} and V_{oc}. Floating busbar technology showed ~4mV increase in V_{oc}, but efficiency enhancement was not seen due to high bus and grid contact resistance.

All these technology enhancements resulted in a 3.44% absolute increase in efficiency over the 17.4% efficient nPERT cell at the start of this research. Figure 9.3 shows pictorially the contribution of each technology enhancement leading to 20.84% efficiency in this thesis. Detailed PC1D modeling and analysis for each generation nPERT cell was performed to extract quantitatively the improvement in key cell parameters due to each technology enhancement. Excellent agreement was achieved in measured and modeled *I-V* parameters. Thus, this thesis demonstrates the potential of the n-type solar cells developed for commercialization of large area silicon solar cells for attaining global grid parity.

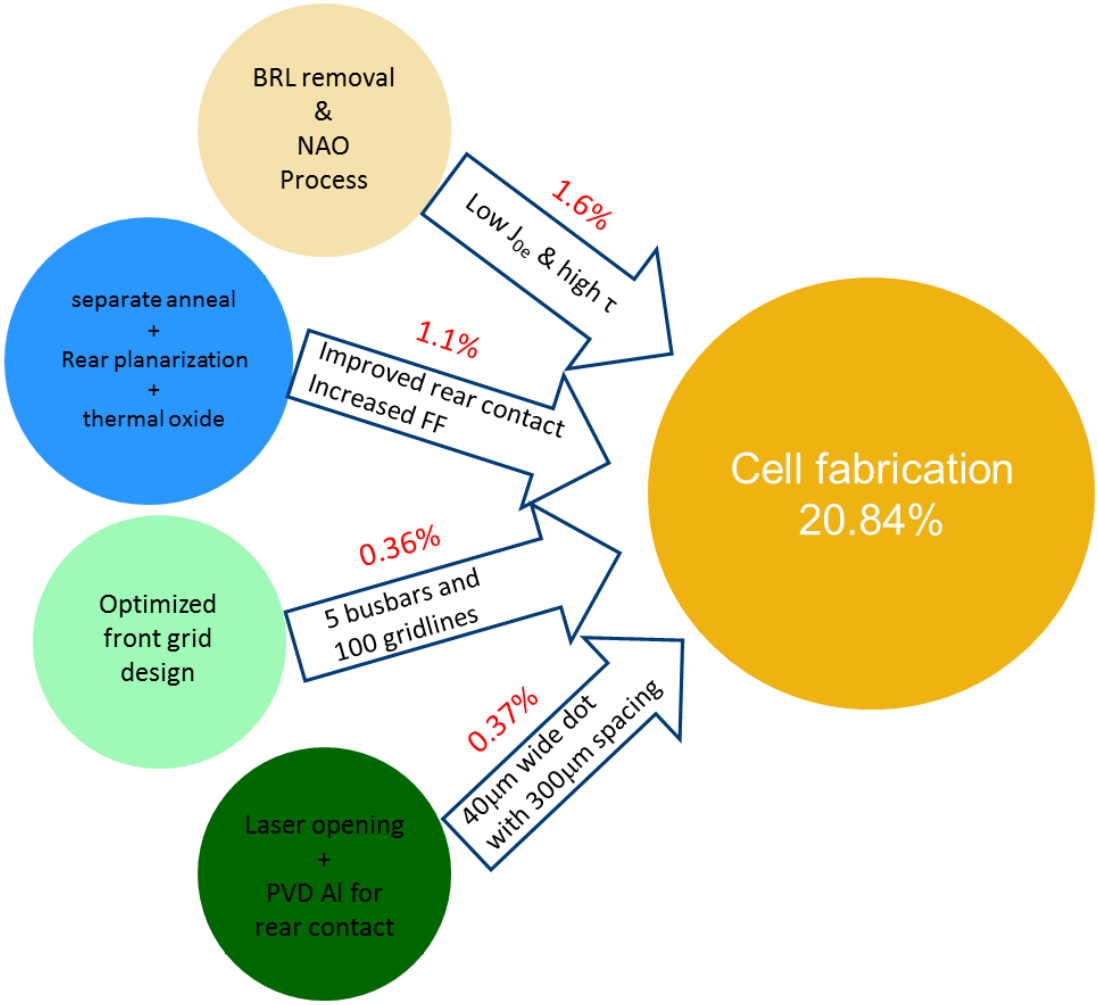


Figure 9.3 The contribution of each technology enhancement leading to 20.84% efficiency in this thesis.

Chapter 10 : FUTURE WORK

This thesis developed a manufacturable process sequence to fabricate low-cost high-efficiency n-type PERT cells on commercial grade large area (239cm^2) n-type Cz Si wafers using commercially feasible technologies and equipment. This innovative process involves implanted boron emitter and phosphorus back surface field, dual annealing at high temperatures, chemical etching treatment for BRL removal, SiO_2/SiN_x stack for surface passivation, optimized front grid design with screen-printed 5 busbars and 100 gridlines, laser opening and PVD Al for rear contact, and floating busbars which resulted in 20.84% efficiency. However, it is still slightly lower than the target of 21% efficiency of this thesis. Therefore, this chapter suggests research directions to improve cell efficiency further and attain ≥21% efficient n-type solar cells which involve two additional technology developments including the use of (1) selective emitters and (2) negatively charged aluminum oxide (Al_2O_3) film for boron emitter surface passivation. These innovative technologies will raise cell efficiency further from 20.8 to 21.1%.

10.1 Implementation of Selective Emitters

Selective emitters consist of two different regions, as shown in Figure 10.1, including heavy doping underneath the contacts and light doping in the photoactive area. The heavily doped emitter (p^{++}) ensures a good metal/Si contact and provides some shielding of the minority carriers from the contact. The lightly doped emitter (p^{+}) reduces emitter recombination losses and increases blue response. Thus, these selective emitters will improve cell efficiency further.

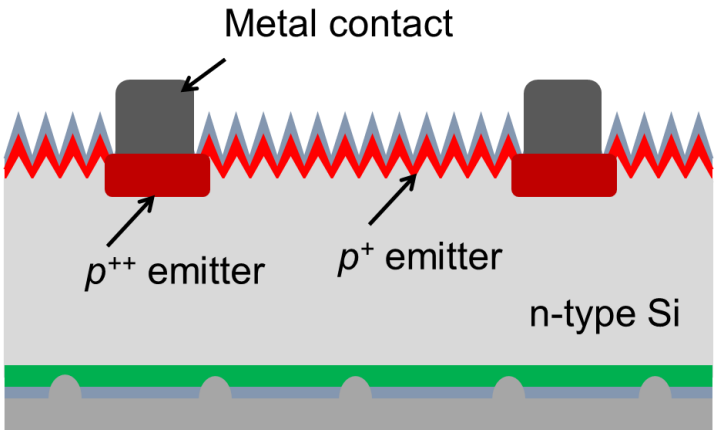


Figure 10.1 Structure of a n-type PERT cell with selective emitters.

The selective emitters can be formed by two in-situ patterned implants. First, a lower boron dose is implanted on the entire 6" n-type Cz Si wafer for a low doping emitter (field regions). A proximity grid patterned mask is then inserted between the wafer and the ion beam followed by a second implant with a higher boron dose for a heavy doping emitter (contact regions) to which the front screen printed contacts are aligned. Then the wafers are annealed at a high temperature ≥1000°C to activate the implanted B dopants and remove the implant damage. The grid pattern is easily visible after an oxidation because of difference in the oxide thickness on the contact regions and field regions, producing color contrast. Figure 10.2 shows an optical microscope image of an ion-implanted selective emitter cell [94].

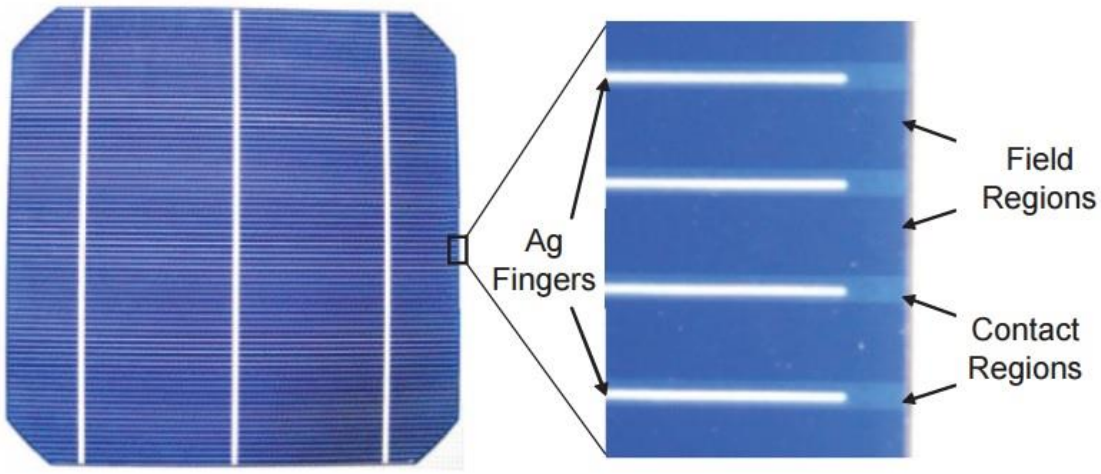


Figure 10.2 Optical micrograph of an ion-implanted selective emitter solar cell.

The boron emitter sheet resistance of the 5th generation 20.84% cell was 90Ω/sq. If more lightly doped selective emitters with ≥150Ω/sq for the field regions and more heavily doped selective emitters with ≤50Ω/sq for the contact regions are applied to the 20.84% cell, FSRV and J_{0e} will be reduced further while maintaining a good ohmic contact, which could lead ≥21% efficient n-type PERT cells. According to the PC1D modeling (Figure 10.3), the current FSRV of ~6000cm/s of the 20.84% n-type PERT cell needs to be reduced to ≤2800cm/s for achieving ≥21% efficiency, while keeping other device parameters unchanged. In order to achieve the target FSRV by using the selective emitter approach, implantation conditions for the field and contact region have to be optimized, which involve the dose amount of implanted dopant and annealing process.

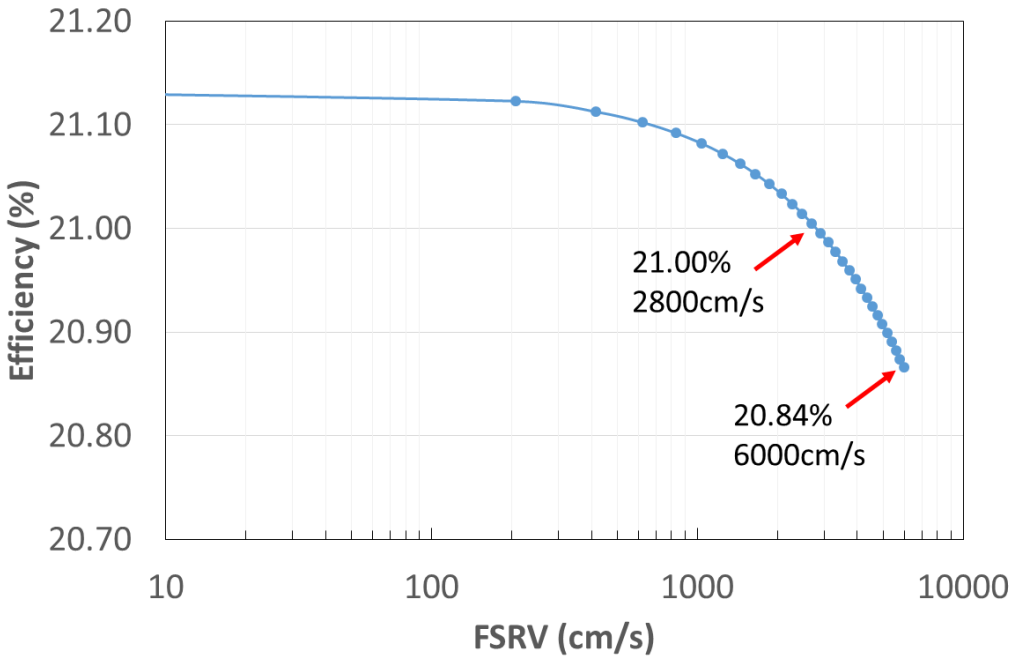


Figure 10.3 Modeling of n-type PERT cell efficiency as a function of BSRV.

10.2 Boron Emitter Surface Passivation by a Negatively Charged Aluminum Oxide Film

Aluminum oxide (Al_2O_3) film with SiN_x capping layer has been proved as an excellent surface passivation layer for p^+ Si region. This is because the Al_2O_3 provides a good chemical passivation due to a low interface trap density (D_{it}) of ~10^{11}eVcm^{-2} as well as a field-effect passivation due to high negative fixed charge (Q_f) of up to10^{13}cm^{-2} which accumulates majority carriers (holes) but repels the photo-generated minority carriers (electrons) from the Si surface. This charge accumulation reduces surface recombination losses. Note that recombination rate is the maximum when the electron and hole concentrations at the Si surface are equal. Thus, this section suggests the implementing Al_2O_3 film for boron emitter surface passivation instead of thermally-grown SiO_2, which will give a further boost in cell efficiency.

Figure 10.4 shows the 6th generation cell processing flow plus Al_2O_3/SiN_x stack for B emitter surface passivation. The Al_2O_3 deposition step is between oxidation and screen printing fingers. After oxidation, SiN_x is deposited on the rear side first, not on both sides. Then the SiO_2 film on the front side is removed by HF dip. About 10nm thick Al_2O_3 film is deposited on the front side by a plasma enhanced atomic layer deposition (PE-ALD). Finally, the Al_2O_3 film is capped by PECVD SiN_x layer.

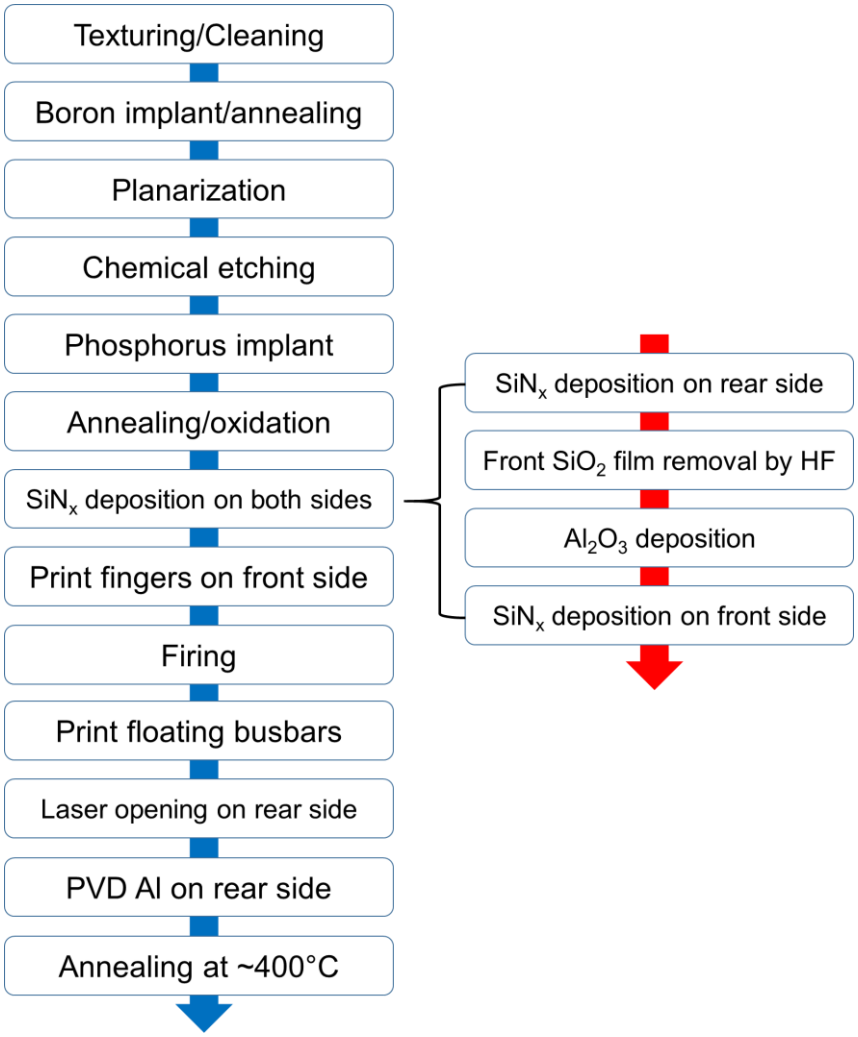


Figure 10.4 Processing flow of 6th generation cell with $Al_2O_3/SiNx$ stack for B emitter surface passivation.

Figure 10.5 shows the PC1D simulated cell efficiency as a function of negatively charged charge density. The input parameters of the 20.84% cell was used for the PC1D simulation. Since the Al_2O_3 has a high negative fixed charge density (Q_f) of up to ~$1x10^{13}cm^{-2}$ [95], cell efficiency can be improved by ~0.25% absolute, resulting in ~21.1% efficiency. Thus, the Al_2O_3 deposition on the selective boron emitters could provide a positive synergistic effect on cell efficiency, resulting in much higher than 21.1% efficiency.

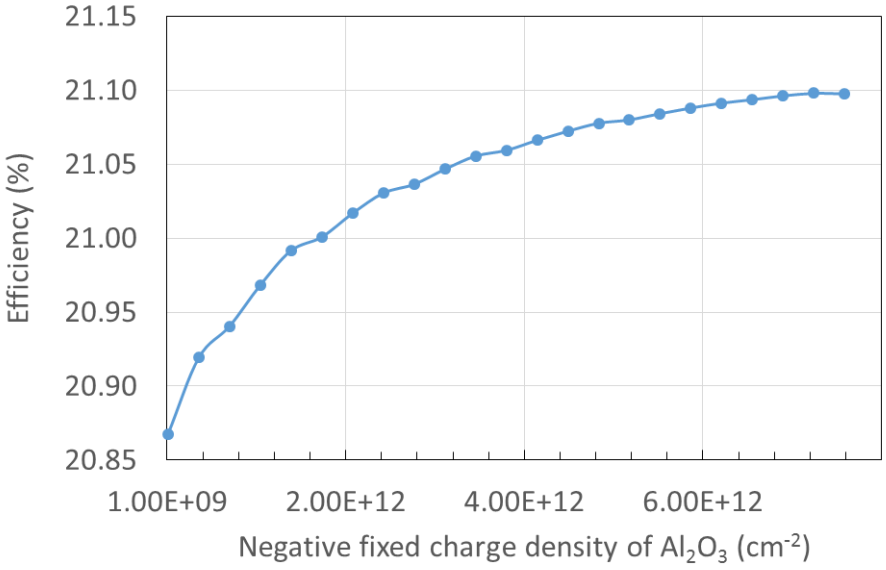


Figure 10.5 Cell efficiency as a function of negative fixed charge density of Al_2O_3.

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PUBLICATIONS FROM THIS WORK

Journal Publications :

[1] **Kyungsun Ryu**, A. Upadhyaya, V. Upadhyaya, A. Rohatgi, and Y.-W. Ok, "High efficiency large area n-type front junction silicon solar cells with boron emitter formed by screen printing technology," *Progress in Photovoltaics: Research and Applications*, vol. 23, pp. 119-123, 2015.

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