QUALITY ASSESSMENTS OF SOLDER BUMP INTERCONNECTIONS IN BALL GRID ARRAY PACKAGES USING LASER ULTRASONICS AND LASER INTERFEROMETER

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QUALITY ASSESSMENTS OF SOLDER BUMP INTERCONNECTIONS IN BALL GRID ARRAY PACKAGES USING LASER ULTRASONICS AND LASER INTERFEROMETER

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

The transition from traditional through-hole assembly to surface mount assembly is a significant step in the evolution of electronic packaging. Surface mount devices (SMDs), such as flip chip packages, chip scale packages (CSPs) and ball grid array (BGA) packages are gaining popularity in the microelectronics industry because they provide high density inputs/outputs, better electrical and thermal performance. However, the solder joint interconnections in SMDs are sandwiched between the silicon die and the substrate, and between the substrate and the printed wiring board (PWB). The qualities of these solder joints are difficult to evaluate because they are hidden from view. The solder joint is one of the most vulnerable parts in an electronic product, as it is to be subjected to various assembly process defects during manufacturing as well as reliability related failures during service. Therefore, inspection of solder joints has become a crucial process in the electronics manufacturing industry in order to reduce manufacturing costs, improve yield, and ensure product quality and reliability. Current non-destructive techniques for inspecting solder joint defects such as electrical testing, X-ray inspection and acoustic microscopy techniques have limitations on the types of solder joint defects that they can detect. A new solder joint inspection technique is urgently needed to fill the gap left by the current inspection techniques.

The laser ultrasonic inspection (LUI) technique has the potential to overcome the limitations of current non-destructive techniques. It is a non-contact, non-destructive, low

cost, high resolution inspection method which allows for rapid inspection of chips both in the assembly line and off-line. It uses a pulsed Nd:YAG laser to induce ultrasound in the chip packages in the thermoelastic regime, and it uses a laser interferometer to measure the transient out-of-plane displacement responses on the package surface. The quality of the solder joints can be evaluated by analyzing the out-of-plane displacement responses. Previous work in this area has shown the potential of using this laser ultrasonics and laser interferometer based inspection system to assess the qualities of solder joints in chip packages. However, there are still some research issues to address before the system will be ready for deployment in the assembly line and research laboratories. This dissertation addresses some of these existing issues. The research work consists of the following: 1) A control interface was developed to integrate all the different modules in the current system to achieve full automation and improve system user-friendliness. 2) A new signal-processing method was developed to analyze the transient out-of-plane displacement signals without the requirement of a known-good reference chip. 3) The application scope of the inspection system was expanded to inspect the second level solder joint interconnects in the BGA packages. Two types of process-induced defects including poor-wetting and solder ball voids were investigated. Meanwhile, solder ball fatigue caused by cyclic mechanical bending and thermal cycling was also studied using this system. 4) A finite element analysis was performed to study the thermo-mechanical reliability of solder balls in PBGA package under cyclic thermal loads.

The successful completion of the research objectives has led to a laser ultrasound solder joint inspection system prototype with more user-friendliness, higher throughputs, better repeatability and more flexibility. The application scope of this system is significantly expanded by the successful inspection of various process-induced and service-induced solder ball defects on BGA packages. All these accomplishments have built strong credential in the path of commercializing the system.

Chapter 1 INTRODUCTION

The technological revolution never stops in the microelectronics industry. Moore's Law, the doubling of transistor density every eighteen months, has led to increasing transistor counts, shrinking die size, and increasing performance. Meanwhile, the launch of the revolutionary iPhone and iPad dramatically changed the world by bringing us to a mobile world. While consumer demands are driving current trends in the microelectronics industry to make electronic products that are fast, compact, high-density, reliable and low-cost, these trends also place an ever-increasing challenge on technologies that are cable to make electronic products with good quality and reliability. Electronic products have to go through a series of complicated manufacturing processes before they become available for the end-users. What's more, when in use, they may experience extensive power and thermal cycling, vibration and other mechanical loading, and exposure to hostile environments. The solder joint interconnection, one of the most vulnerable parts in an electronic product, is likely to be subjected to various process defects during manufacturing as well as reliability related failures during service. Therefore, inspection of solder joints has become a crucial process in the electronics manufacturing industry in order to reduce manufacturing costs, improve yield, and ensure product quality and reliability.

Some non-destructive techniques have been developed and are commercially available for inspecting solder balls. Most of them fall into one of these four categories: 1) visual inspection 2) electrical testing, 3) X-ray inspection, and 4) acoustic inspection. While many of these techniques and systems are suitable for specific inspection tasks, they do not necessarily encompass all the capabilities required for evaluating the quality of the overall assembly. Therefore, new inspection techniques are urgently needed to fill the gap between available inspection capabilities and industry requirements for nondestructive, noncontact, low-cost, and fast inspection systems.

1.1 Visual Inspection

Dedicated visual inspection systems have been used in manufacturing environments for a long time. Both 2-dimensional (2D) and 3-dimensional (3D) visual inspection systems are available. A basic 2D inspection system includes an illumination source to light up the object, a camera to record the reflected light from the object, and an image processor that produces a recognizable image. Subsequently, the image can either be compared with a previously recorded good image to find the difference, or it can be interpreted using image processing and pattern recognition techniques. Capson and Eng [1] developed a tiered illumination source which uses two circular color lamps and one camera to highlight the joint's structure as shown in Figure 1-1. They have reported that

this system is able to detect and classify solder joint defects including no solder, insufficient or excess solder, poor wetting of components leads or solder pad, and faults due to improper insertion of component leads.

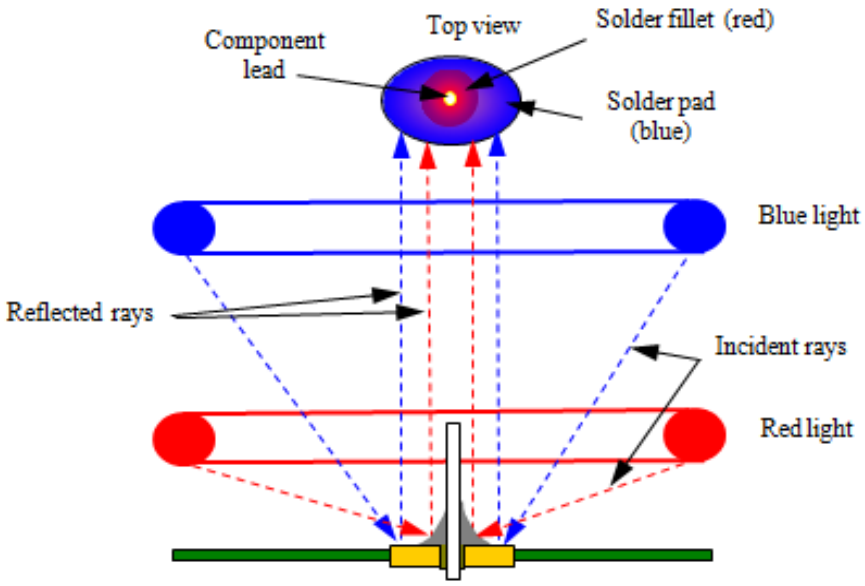


Figure 1-1: Schematic of tiered-color illumination solder joint inspection system with two light sources

A 3-D machine vision system using a laser triangulation technique [2, 3] has also been used in solder joint inspection. As shown in Figure 1-2, laser triangulation shines a laser beam onto the sample's surface, and the reflected beam is collected by photodetectors [4]. The reflected beam will move relative to the sample's height as the beam scans across the sample's surface. Using geometric triangulation, the system can calculate the contour of the solder joint from the displacement of the reflected beam and then evaluate the quality of the solder joint.

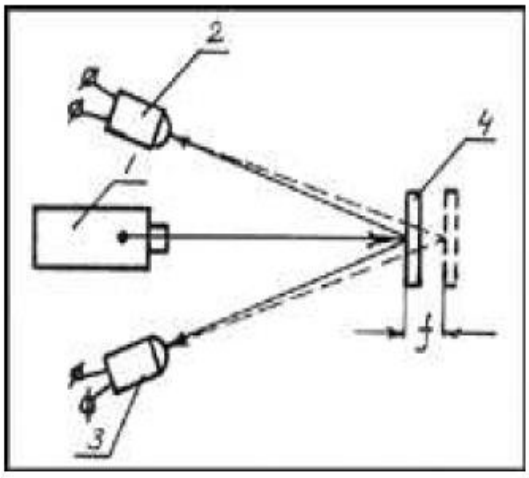


Figure 1-2: Schematic of a laser triangulation measuring system, f = displacement, 1 = laser light source, 2 and 3 = light sensors, 4 = surface

However, all of the aforementioned visual inspection techniques can only be used for inspecting traditional visible solder joints. As hidden solder balls deny the access of light beams, they become almost unfeasible. As shown in Figure 1-3, an industrial endoscope has been tried for inspecting solder joints in area array packages but this can only provide information for the peripheral columns. In summary, visual inspection techniques have limited application for inspecting solder balls.

Figure 1-3: Solder balls inspection using an endoscope (Courtesy of Caltex Scientific)

1.2 Electrical Testing

Electrical testing is the most widely-used non-destructive technique to examine solder joints. Electrical testing is the identification and segregation of electrical failures from a population of devices. An electrical failure is any unit that does not meet the electrical specifications defined for the device. In simplified terms, electrical testing consists of providing a series of electrical excitation to the device under test (DUT) and measuring its response. For every set of electrical stimuli, the measured response is compared to the expected response, which is usually defined in terms of a lower and an upper limit. Any DUT that exhibits a response outside of the expected range of response is considered a failure.

Electrical testing consists of two primary methods: functional testing and in-circuit testing. Functional testing is characterized by exercising the circuit to drive all possible

functions performed under all possible environmental conditions, which can then verify that the circuit performs the intended functions [5]. However, this test is often uable to locate failure sites. In-circuit testing, also known as the “bed of nails” test, analyzes the circuit from a structural perspective. It is more efficient than functional testing because the circuit can be portioned into simpler sub-circuits that are checked independently from the other sub-circuits [5]. Figure 1-4 illustrates an in-circuit testing station. It consists of a fixture whose top and bottom plates are outfitted with test probes. The plates close down on the unit under test, contacting each test point and measuring the resistance between points. The drawbacks of the electrical testing are that the testing pads take up a lot of board space and that it doesn’t reflect failure modes such as non-wetting or bridging. Electrical testing is also incapable of detecting intermittent defects.

Figure 1-4: In-circuit testing station (Courtesy of National Instrument)

1.3 X-Ray Inspection

The X-ray technique has been used for variety of applications including medical imaging and microelectronic package inspection as it offers the advantage of being non-destructive and non-invasive. X-ray emission is caused by the sudden deceleration of the electrons as they collide with the target. X-rays have a wavelength in the range of 0.01 to 10 nanometers. This short wavelength allows them to penetrate most materials. The resolution of the X-Ray technique is about 1~2 microns, depending on the X-ray wavelength. A typical system usually has an X-ray source, an X-ray collector to receive the penetrated radiation, and a camera to convert the photons on the collector to a digital form and imaging interpretation software. The images for different materials will be displayed in different pixels because of different X-ray absorption. Generally speaking, solder attenuates the intensity of the X-ray beam to a much greater degree than any other material present in the assembly, such as copper and substrates [6]. There are three methods of X-ray inspection: radiography, tomography [7] and laminography.

Most commercially available 2-D X-ray inspection systems use radiography (shown in Figure 1-5), since it can see through the whole solder joint. This technique has been used for years in both medicine and technology for looking through opaque materials to find the underlying material's structure. The smaller the grain size of the X-ray converting screen, the better the resolution, but the shorter its life [8]. X-ray radiography

has been used to detect the presence and location of the defects in the packages, including shorted or missing solder joints, voids in solder joints or underfill, misalignment, missing copper traces resulting in electronic opens, and broken gold wires that result in electronic opens. Figure 1-6 shows a 2D X-ray image of a BGA package with shorted solder joints and misalignment. X-ray radiography has difficulty inspecting solder joints in the presence of interference. The interference may come from the multiple-layer components, overshadowed balls or the presence of via and trace on substrates. Figure 1-7 shows a 2D X-ray image of solder balls with an overshadowing capacitor [9]. Obviously, the overshadowing capacitor introduces some difficulties when interpreting the X-ray image. As more complex packages, such as 3-D packages, emerge in the market, this problem will limit the application scope of 2-D X-ray tools. Another disadvantage of 2-D X-ray tools is that it is difficult to detect cracks with them. The cracks can be identified only when the joints are properly positioned relative to the radiation to promote sufficient contrast.

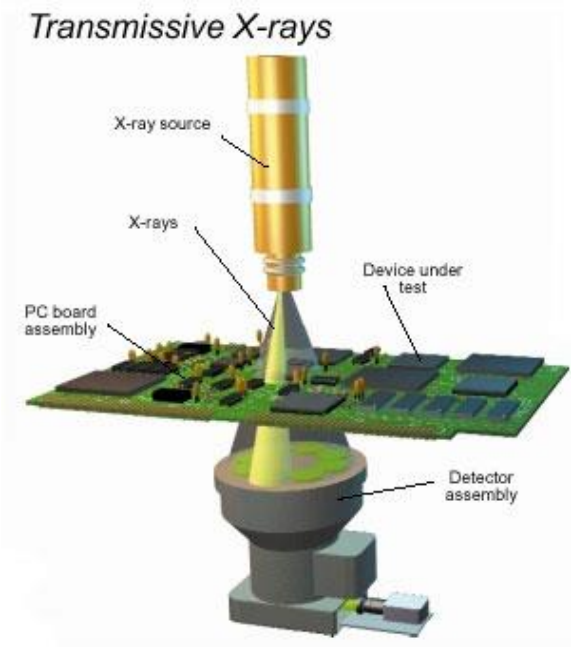


Figure 1-5: X-ray radiography (Source: Machinedesign®)

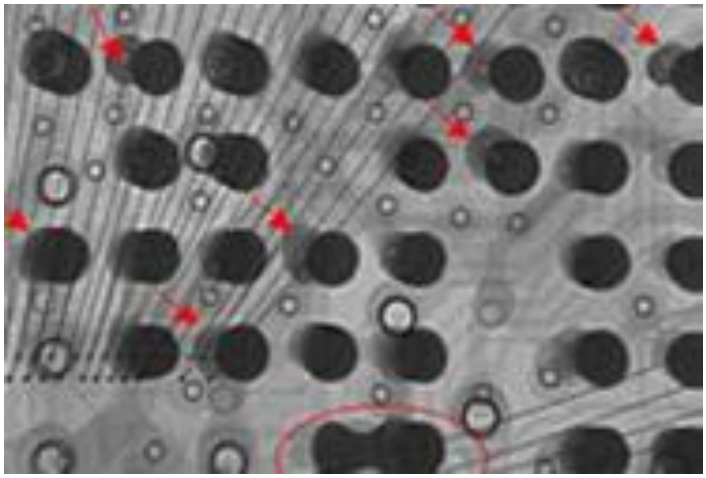


Figure 1-6: 2D X-ray image showing shorted and misaligned solder balls

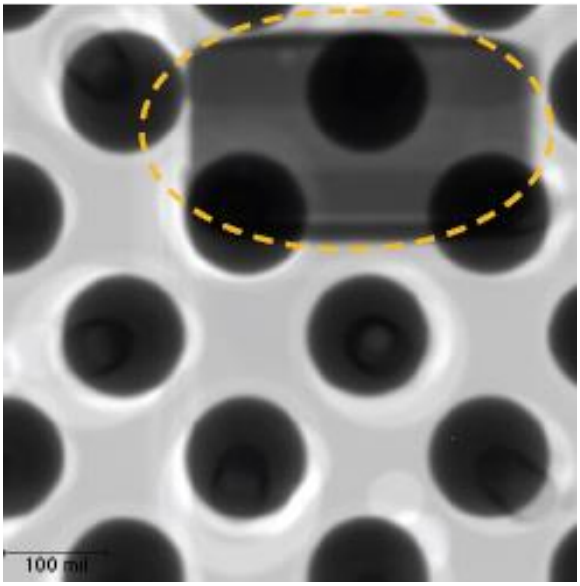


Figure 1-7: 2D X-ray image showing overshadowing capacitor

Both X-ray laminography and X-ray tomography are viewed as 3D X-ray techniques. In X-ray laminography, the X-ray beam is focused on one plane at a time and slices the specimen horizontally, as shown in Figure 1-8. The X-ray source and the detector are moved synchronously in opposite directions. Due to that correlated motion, the vertical location of the focus plane can also move within the sample, so it is able to create a 3D image. X-ray laminography is a natural extension of radiography that can give the depth as well as the X-Y position of defects. However, its spatial resolution is limited because it requires high X-ray flux for rapid pass/fail solder ball inspection, and the equipment and operation cost of these systems is high [10]. It is also considered unsuitable for online application because of its low throughput.

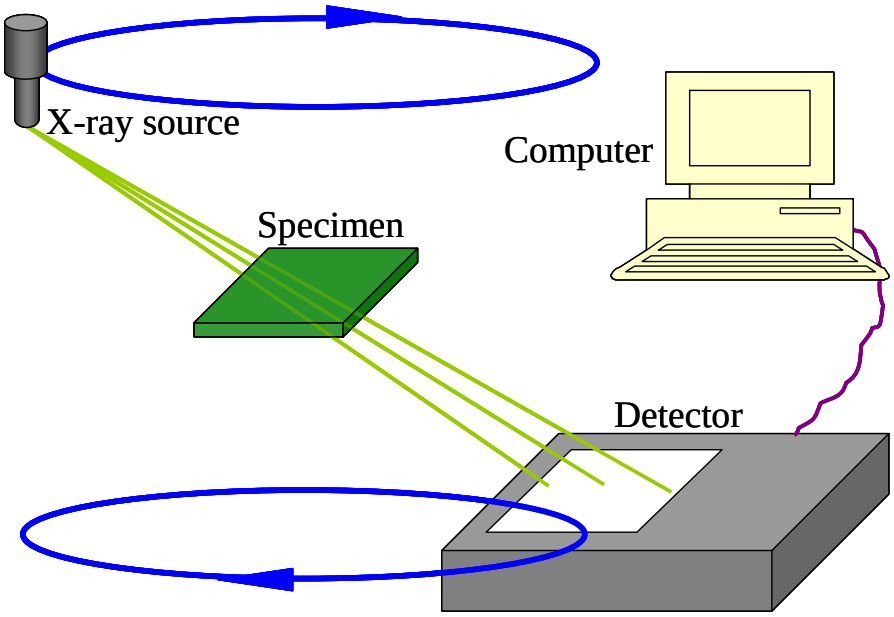


Figure 1-8: X-ray laminography

As shown in Figure 1-9, X-ray tomography generates a 3-D image by reconstructing from a sequence of images which are taken when the device under test (DUT) rotates between the X-ray source and detector. By doing this, the analysis is able to perform virtual cross sectioning of the DUT [11].

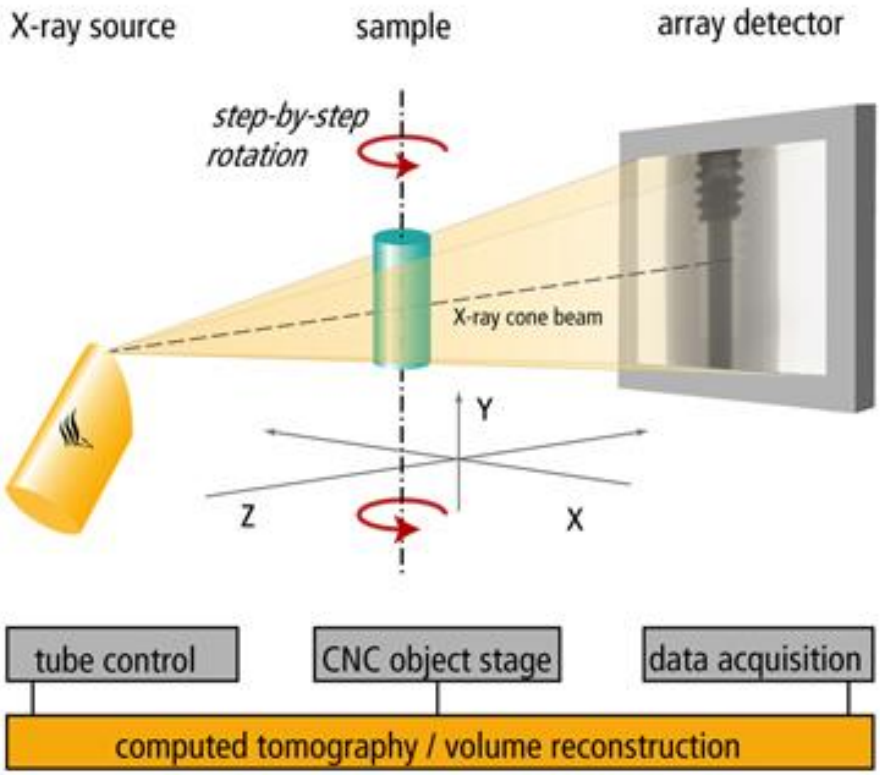


Figure 1-9: X-ray tomography (Source: Phoenix X-ray®)

Figure 1-10 [12] is a 3D image constructed from X-ray tomography, showing a solder ball with a head-in-pillow (HIP) defect on the left and a good solder ball on the right. The X-ray tomography technique is very powerful and can detect a lot of solder joint defects. Theoretically, it should have the ability to inspect all solder joint defects, but sometimes, 3D images are very difficult to interpret. Because the samples need to be rotated during inspection, the space inside the test chamber limits the utility of X-ray tomography. It is not very suitable for inspecting a test board with large dimensions or complicated geometry. Meanwhile, it requires an extremely long time for data acquisition

and image reconstructions, so it is considered unsuitable for online applications. Additionally, the operational cost of this kind of system is prohibitive.

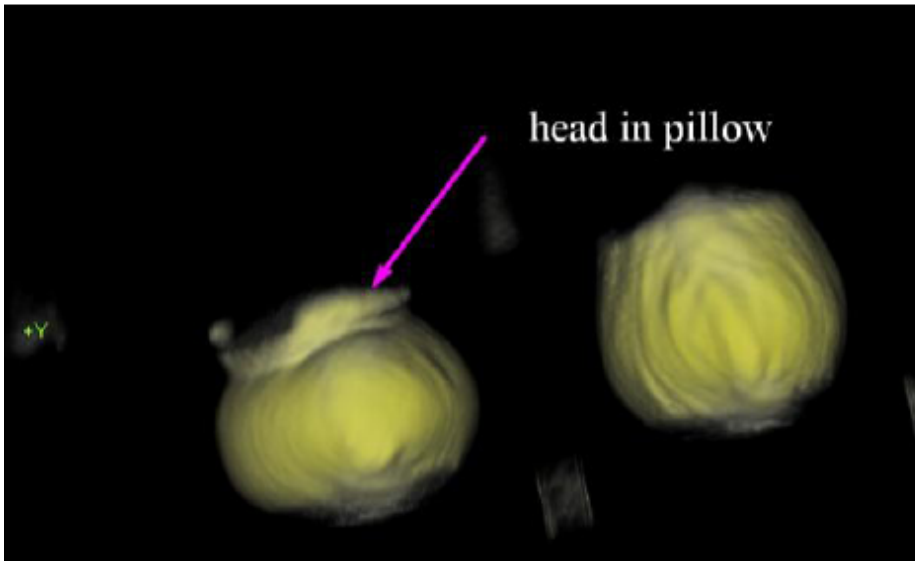


Figure 1-10: 3D X-ray image showing a solder ball with HIP defect

An automated inspection technique for BGA-mounted substrates and solder balls by means of oblique computed tomography (OCT) has been proposed by researchers at Nagoya Electronic Works Corporation, Nagoya University and Gifu University [10]. Oblique computed tomography, as shown in Figure 1-11 is a novel imaging technique, and the proposed technique consists of position adjustment, ball extraction, character extraction and judgment. OCT obtains the projection images of an object from an oblique direction by rotating the X-ray detector first, and then a 3-D OCT image is obtained with 3-D image reconstruction [11]. Linear discriminated analysis and artificial neural network techniques have been used as determination methods for inspecting solder balls

automatically [11]. This technique for online inspection of BGA solder balls has been demonstrated by the developers.

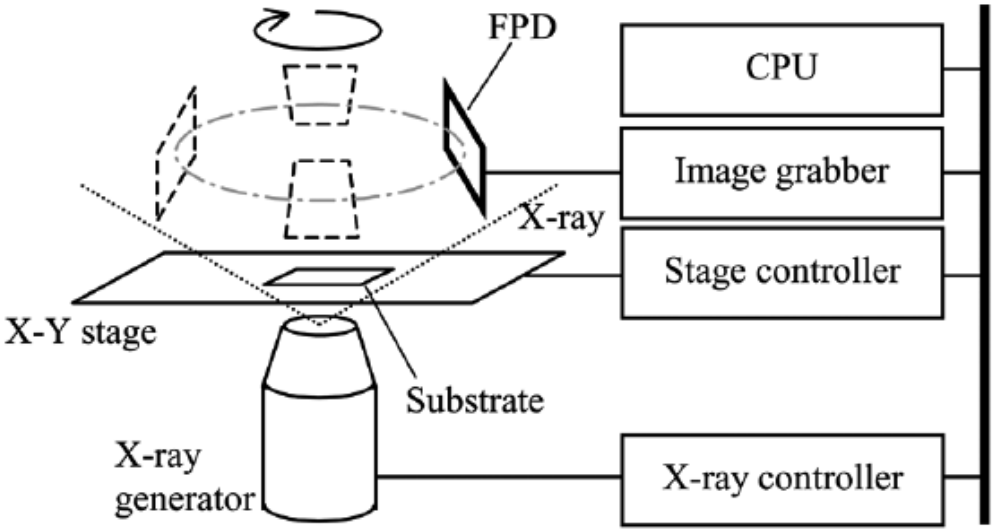


Figure 1-11: Schematic layout of OCT inspection system

1.4 Acoustic Inspection

1.4.1 Scanning Acoustic Microscopy (SAM)

Acoustic inspection is another popular non-destructive technique for inspecting solder balls. In acoustic imaging, a high frequency ultrasonic wave generated from a piezoelectric transducer is focused on the package and an acoustic reflection or transmission from the package's internal regions is captured by the transducers. It works on the principle that the propagation and reflection of acoustic waves will change at the interface between two different materials with different acoustic impedances. This is why acoustic imaging techniques are used extensively in electronic package inspection of interfacial defects such

as voids and delaminations. Because the acoustic impedance of air is almost zero, the ultrasonic wave cannot propagate through a vacuum at any frequency or through air at frequencies above 10 MHz.

Scanning acoustic microscopy (SAM) is a commercial non-destructive solder ball inspection tool which uses an ultrasound point source to scan across the sample surface and capture reflections or transmissions of ultrasonic waves. It usually operates in the frequencies between 10 MHz and 2 GHz.

There are different modes of scanning acoustic microscopy. If the same transducer is used to capture the acoustic reflection, this acoustic imaging mode is referred to as the pulse echo mode. C-mode scanning acoustic microscopy (CSAM) is the most popular pulse echo mode, and it forms images by capturing acoustic reflections from a specific depth region in the packages. Figure 1-12 shows a typical schematic of a CSAM system, in which water acts as a couplant and propagates the acoustic energy from the transducer to the specimen to be tested. When there is a flaw, it reflects a different echo whose amplitude is proportional to the difference in acoustic impedances between the flaws and surrounding medium. The typical received reflection waveform in the time domain is shown in Figure 1-12.

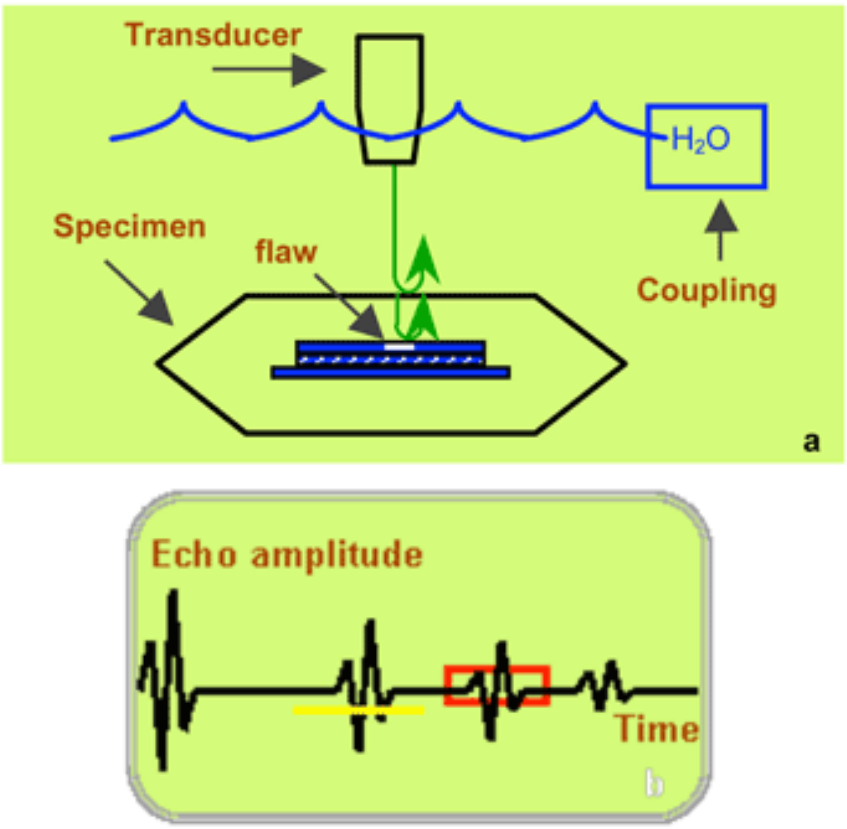


Figure 1-12: Schematic of CSAM operation principle (Source: Intel Corporation)

CSAM has several limitations. First, CSAM can only detect interfacial defects such as voids, cracks and delaminations on a die-ball interface. The frequency downshifting [13] causes a significant reduction in the resolution, especially when a high frequency transducer is used. The edge effect [14] of CASM decreases measurement resolution, and CSAM always requires a coupling medium (usually deionized water).

If an additional transducer is placed below the package to act as a receiver of acoustic transmission through the samples, it is called the transmission mode. Through scanning acoustic microscopy (TSAM) image is the absorption of ultrasound as the ultrasound

passes through the package, which is similar to 2D Transmission X-ray. Figure 1-13 shows a comparison between CSAM and TSAM. TSAM is relatively easy to set up; however it provides less spatial resolution than CSAM and it does not provide any depth information about the defect.

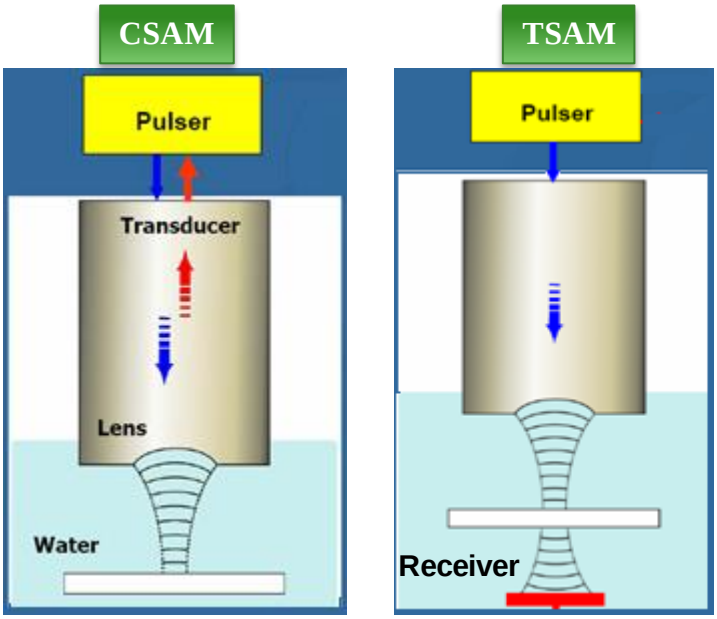


Figure 1-13: Schematics of CSAM and TSAM

Figure 1-14 shows that the focused beam of an ultrasonic transducer forms a shape of an hour glass, thus forming a focus zone. The hourglass shaped beam narrows to the spot size at the waist, as shown in Figure 1-15. There are 2 key parameters to characterize an ultrasonic transducer: resolution and depth of field. Resolution determines the smallest flaw that it can capture, while the depth of field defines the effective depth for ultrasound wave penetration. Equation 1.1 shows the detailed calculations. Based on the equation, the resolution of an ultrasonic transducer improves with increases in the frequency of the

transducer at the expense of penetration depth. For example, a transducer with a center frequency at 230MHZ and F# at 2 has a resolution of 11 microns and depth of field as 0.185mm. If the frequency increases to 300MHz, the resolution becomes 8 microns with depth of field as 0.142mm.

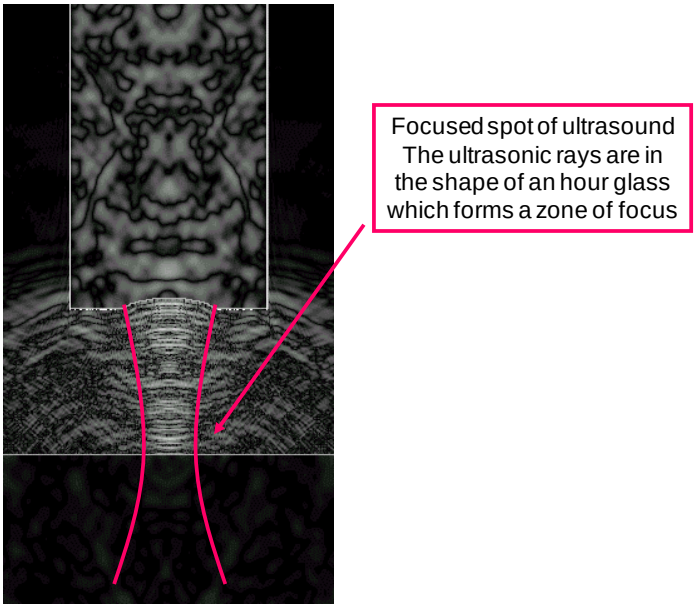


Figure 1-14: Focused beam of an ultrasonic transducer

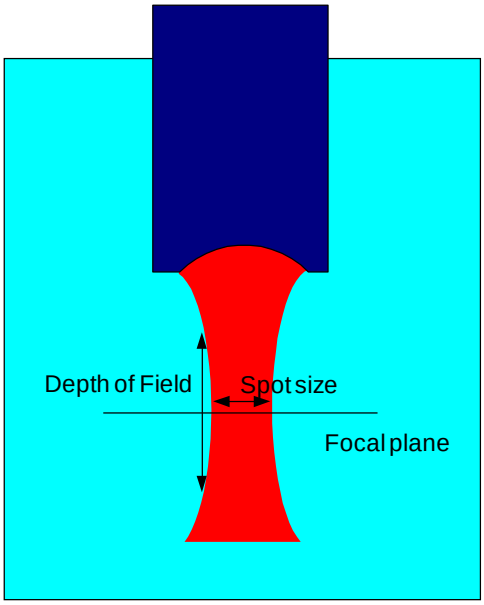


Figure 1-15: Schematic of focused beam of an ultrasonic transducer

$$Resolution\ (\Delta X) = 0.707 * 1.22F^{\#}\lambda \qquad (1.1)$$
$$Depth\ of\ field\ (\Delta Z) = 7.1(F^{\#})^2\lambda$$
$$where\ F^{\#} = \frac{Focal\ length}{Diameter}$$
$$\lambda = \frac{Velocity\ (mm/\mu s)}{Frequency\ (MHz)}\ in\ mm$$

Therefore, SAM has some limitations for detecting solder joint integrity in chip packages with large thickness, such as ball grid array (BGA) packages [15]. High frequency ultrasound is greatly attenuated, and this causes poor resolution due to the decrease of signal to noise ratio as ultrasound propagates deeper into the thick specimen, so defects that are located deep beneath the specimen may not be detected. Diagonal/vertical defects will not be detected, neither. The only reported SAM applications for BGA package inspection has been to detect popcorn failure [16] and die-die attach interfacial delamination [17], and these types of defects are both located in the upper layer of the BGA package where large penetration depth is not required.

1.4.2 Acoustic Emission

Besides SAM, a new technique based on acoustics, called acoustic emission (AE), is developed and applied to inspection of solder ball defects. Acoustic emission refers to the spontaneous release of transient elastic waves due to a sudden redistribution of stress in a material when a structure is subjected to internal damage that can be caused by an external

stimulus such as a change in pressure, load, or temperature. In such circumstances, the localized damage will trigger a release of energy in the form of acoustic/stress waves that propagates in a radial direction from the source and are recorded by sensors [18]. This technique has been applied to accurately detect the onset of pad cratering during a four-point bend test [18-20]. The test results demonstrate that acoustic emission tests can detect pad cratering much earlier than can electrical tests. However, acoustic emission shows limited applications for inspecting solder ball defects that are not caused by mechanical shock.

Figure 1-16 shows a schematic illustration of the four-point bending test set-up [18]. Strain gages were attached at the corners of the package to measure the strain during the bend test. Meanwhile, the daisy chain resistance was monitored in situ. Two acoustic emission sensors were also clamped on the ends of the PCB to detect the pad cratering crack that cannot be captured by daisy chain resistance measurement. The sensors were connected to the AE monitoring system via a preamplifier.

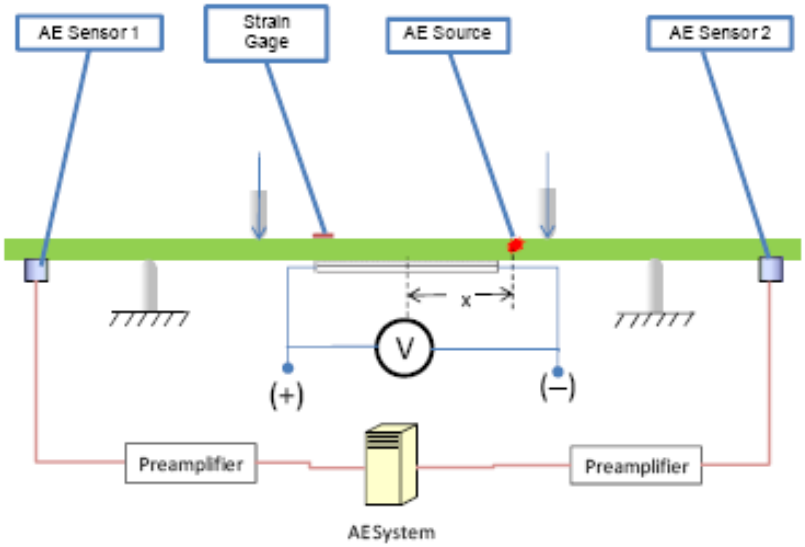


Figure 1-16: Schematic of bending test set-up

1.5 Laser Ultrasound-Interferometric Inspection System

The overall objective of this research is to develop a noncontact, nondestructive, automated, accurate and low-cost system for evaluating the quality of solder joints/balls in packaged electronic devices, including flip chip packages, chip scale packages, ball grid arrays packages and land grid array packages, etc. In addition, the non-destructive inspection system under development aims to provide a solution that can overcome some of the limitations of current non-destructive inspection techniques. This system is expected to be used in-line during the assembly process or off-line during process development and failure analysis.

This research is based on laser ultrasound and interferometric techniques. The system uses a pulsed Nd:YAG laser to induce ultrasound in the chip packages in the thermoelastic regime to avoid any damage to the packages. It then measures the transient

out-of-plane displacement response on the package surfaces using a laser Doppler vibrometer. The solder joints/balls with different qualities cause different responses. Solder joint defects may be detected and/or classified by analyzing the transient out-of-plane displacement responses. Figure 1-17 shows the operating principle of the laser ultrasound inspection (LUI) system from laser-induced ultrasound generation in the packaged electronic devices, to signal acquisition of transient out-of-plane displacement responses on the package surface with a laser Doppler vibrometer. A typical captured time-domain signal is also shown in Figure 1-17.

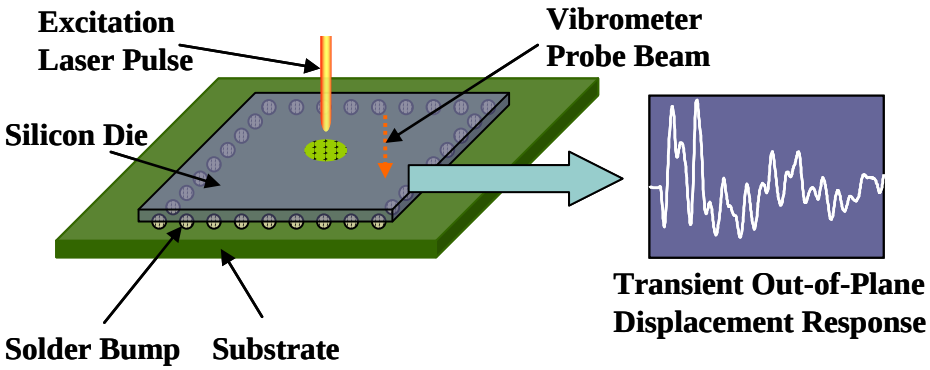


Figure 1-17: Operating principle of laser ultrasound-interferometric inspection system

In previous work, the developed system has been successfully applied to detect solder joint defects including missing, misaligned, open, and cracked solder bumps in flip chips, land grid array (LGA) packages and multilayer ceramic capacitors (MLCCs) [21]. Some reliability studies on solder joints under accelerated thermal cycling have also been reported using this system [22, 23]. Table 1-1 shows the comparisons among all the

different non-destructive inspection methods for solder joint integrity. Various features are included, and the laser-ultrasound method shows its uniqueness and potential. However, there are still some research gaps that need to be addressed before the system will be ready for industrial use.

Table 1-1: Comparisons of different non-destructive solder ball inspection methods

Features			Laser-Ultrasound	Electrical Test	X-Ray		Acoustic Inspection
					2D X-Ray	3D X-Ray	
Contact or Non-contact			Non-contact	Contact via test pad on PCB	Non-contact	Non-contact	Contact(immersed in water)
Throughput			High	High	High	Low	Medium
Cost			$200K	Low	$150K - $250K	$350K - $500K	$200K - $250K
Resolution			Has been used to detect presence of micro-cracks	Low	1~2 microns	1~2 microns	Resolution increases with frequency of ultrasonic transducer at expense of penetration depth. For examle, transducer with 230MHz frequency can have resolution of 11microns.
Capabilities	Silicon die defects		Yes	Yes	Yes	Yes	Yes
	Interlayer delamination		Yes	No	No	Yes	Yes
	Solder bump defects	Missing	Yes	Yes	Yes	Yes	Yes
		Misaligned	Yes	No	Yes	Yes	No
		Cracks	Yes	No	No	Yes	No
		Open	Yes	Yes	No	Yes	Yes
		Voids	Yes	No	Yes	Yes	No
	Package Types	FCP	Yes	Yes	Can apply to various package types, however, it's difficult to interpret images of multilayered or double-sided samples	Test chamber has very limited space (2~3 inches), unsuitable for sample with large dimension or complicated geometry	Incapable of detecting package with large thickenss because of lack of penetration ability
		CSP	Yes	Yes			
		LGA	Yes	Yes			
		BGA	Yes	Yes			
		MLCC	Yes	Yes			

The research objectives for the work in this thesis include: 1) Develop a control interface to integrate all the different modules in the current system to achieve full automation and improve system user-friendliness. 2) Develop a new signal-processing method for analyzing the transient out-of-plane displacement signals without the requirement of a known-good reference chip. 3) Expand the application scope of the inspection system to inspect the second level solder ball interconnects in the BGA packages. Two types of process-induced defects including poor-wetting and solder ball

voids will be investigated. Meanwhile, solder ball fatigue caused by cyclic mechanical bending and thermal cycling is also studied using this system. 4) Perform finite element analysis to study the thermo-mechanical reliability of solder balls in PBGA package under cyclic thermal loads.

1.6 Dissertation Outline

This dissertation consists of seven chapters. A brief outline of the content covered in each of these chapters is given in this section.

Chapter 1 gives an introduction to the motivation for the work presented in this dissertation. Different non-destructive inspection systems are briefly reviewed and compared to show their limitations. Then a laser ultrasound-interferometric inspection system is then proposed to try to overcome some of these limitations.

Chapter 2 goes over different backgrounds that are needed for this thesis work, including electronic packaging, laser optics, laser ultrasound generation and detection, mechatronics, digital signal processing, statistics and finite element analysis.

Chapter 3 introduces the hardware and software of the laser ultrasound-interferometric inspection system. Different hardware modules are described and integrated into a whole inspection system. Moreover, the system alignment and

throughput are covered. Finally, the software interface that is developed to automate the inspection procedure is presented.

Chapter 4 covers a signal processing method called Hybrid Reference Method. The motivation of this signal processing method is to eliminate the need of a known-good reference chip for comparison. Plus, the method also takes manufacturing variations into consideration. The development and application examples of this new signal processing method are demonstrated in this chapter.

In Chapter 5, we will see that the developed laser ultrasound-interferometric system is used to inspect two types of process-induced defects on BGA packages, including poor-wetting and void. This is the first time that the system is applied to inspect the quality of BGA packages. What's more, other solder ball evaluation methods including X-Ray, SAM, electrical testing and cross-sectioning will also be carried out for comparison.

In Chapter 6, the focus is now on service-induced defects on BGA packages. Two common types of the service-induced defects are evaluated using the inspection system, including displacement and temperature related defects. In the displacement related accelerated life testing, a FCBGA package is the test vehicle that goes through mechanical bending. While in the temperature related accelerated life testing, 2 types of PBGA packages are put into a thermal chamber to go through temperature cycles. Other NDT methods including 3D X-Ray, acoustic emission and electrical testing will also be

adopted for comparison. In addition, a thermo-mechanical finite element analysis will be presented to support the experimental work.

Chapter 7 summarizes the work presented in this dissertation, lists the unique contributions and provides the scope for potential future research.

Chapter 2 LITERATUR AND BACKGROUND

Development of the laser ultrasound inspection system entails multidisciplinary expertise including electronic packaging, laser optics, laser ultrasound generation and detection, mechatronics, digital signal processing, statistics and finite element analysis, etc. Only the successful integration of these various technologies can lead to the successful development of an inspection system that meets the overall research goal.

2.1 A Brief Overview of Electronic Packaging

As consumer demands are driving microelectronics products towards low-cost, high-performance and miniaturization, the packaging of electronic circuits, i.e. electronic packaging, has become a crucial area of microelectronic technology. Electronic packaging is defined as a bridge that interconnects integrated circuit (IC) and other components into a system-level board to form electronic products [24]. In the processes of microelectronics manufacturing, electronic packaging provides electrical as well as thermal and mechanical functions to semiconductor chips. As shown in Figure 2-1 [25], electronic packaging is typically divided into the following five levels:

Level 0: semiconductor chip level (integrated circuit (IC)).

Level 1: chip on a carrier. In this level, an IC die is assembled into a package carrier (substrate or lead frame) with interconnections

Level 2: the packaged IC die mounted to a printed wiring board (PWB) or to another type of substrate

Level 3: board-to-board interconnects.

Level 4: connections between two subassemblies. For example, a rack or frame may hold several shelves of subassemblies that must be connected together to make up a complete system, such as a server and a super computer.

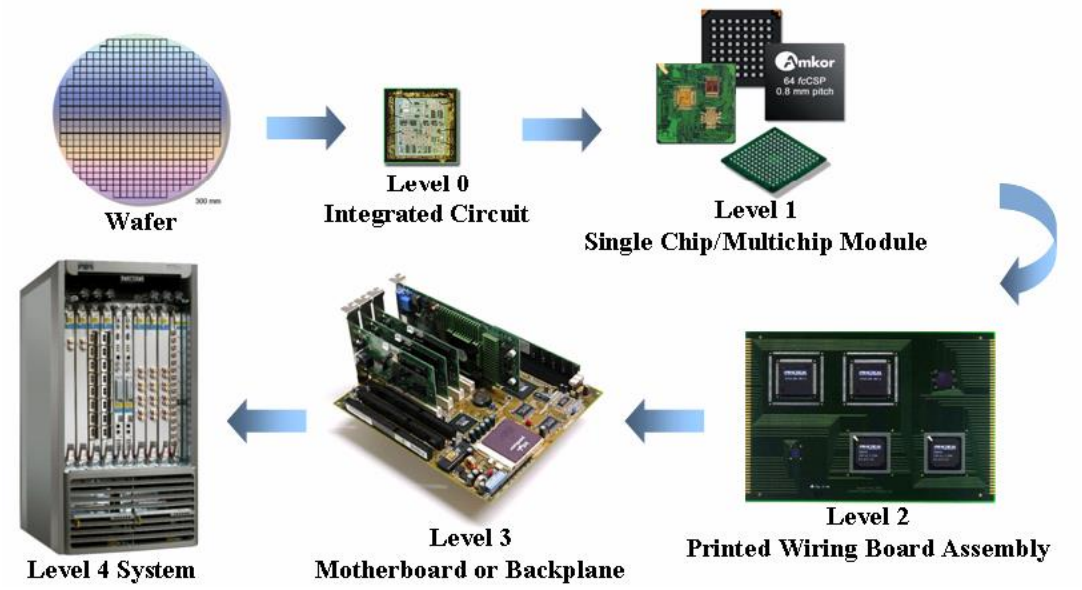


Figure 2-1: Electronic packaging hierarchy

In this thesis work, the electronic packaging of Level 2 is the main focus, i.e. the interconnection between a silicon die and a printed wiring board (PWB).

2.2 Evolution of Electronic Packaging

A schematic of the evolution of electronic packaging of Level 2 is given in Figure 2-2. Dual In-Line Package (DIP) was a typical through-hole packaging technology starting in the 1970s. In a DIP, the input/output (I/O) connections in the form of pins were arranged along two edges of the package. During assembly, the pins of the components were inserted into the holes of the PWB, and then they were sent to a wave soldering machine to finish assembly. Later, surface mount devices (SMDs) were developed and started to replace DIP. First, the assembly of SMDs was much easier than that of DIP, owing to the introduction of the reflow oven. Moreover, SMDs allowed greater I/O density, because the I/O pins were arranged along four edges of the package instead of only 2 edges on DIP. As shown in Figure 2-2, the Quad Flat Packs (QFP) package was a rudimentary type of SMDs. QFP packages have "gull wing" leads extending from each of the four sides that build the connection between the component and PWB. However, both DIP and QFP only take advantage of the sides of the components, leaving a significant amount of area on the back side of the board unutilized. To address this issue, area array package was invented. The Ball Grid Array (BGA) package is a typical type of area array package. It uses solder balls instead of pins to build the interconnection distributed on the whole area underneath the package. In addition to a larger I/O density, the solder balls also significantly reduce the electrical parasitics and

resistance due to their shorter interconnect lengths [26]. The BGA packages further evolved to Chip Scale Package (CSP). In a CSP, a package size to silicon size ratio of 1.2 can be achieved. Even though solder balls started to emerge in BGA and CSP packages as the 2nd level interconnects, the wire-bond technique was still dominant in 1st level packaging. Then with the advancement on flip-chip technology, the BGA and CSP packages have evolved into Flip Chip On Board (FCOB) packages where the solder balls served as the 1st level interconnects, with the silicon die flipped down and placed directly on the board using solder balls. This reduces the number of levels in the packaging hierarchy to one, thereby increasing the signal speed significantly. The I/O density in FCOB packages will achieve its limit when the pitch of solder balls cannot shrink any further. Consumers' demands are driving the current trend in the microelectronics industry to make electronic products more compact. Therefore, 3D packaging, such as stacked die, package-on-package (PoP) and through-silicon via (TSV), was invented in order to utilize space in the vertical direction.

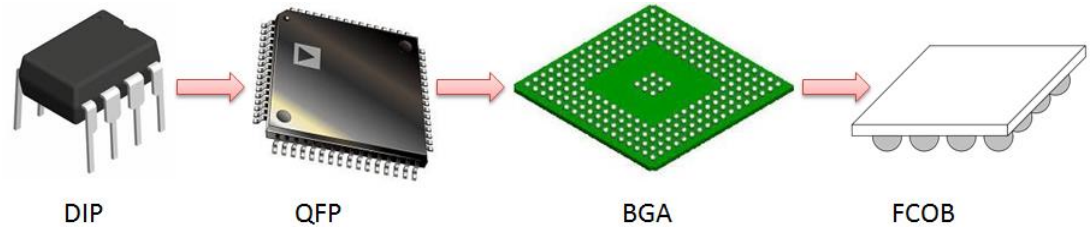


Figure 2-2: Evolution of electronic packaging technologies

Figure 2-3 shows the next generation 3D package architecture, which utilizes the different electrical packaging technologies mentioned previously. Four dynamic random-access memory (DRAM) dies are stacked together using TSVs. These stacked dies and an application-specific integrated circuit (ASIC) are assembled on an interposer using micro balls. The interposer is then assembled on a substrate using flip chip bumps. Finally the package is balled with BGA balls, which will be the interconnections between the package and the PWB.

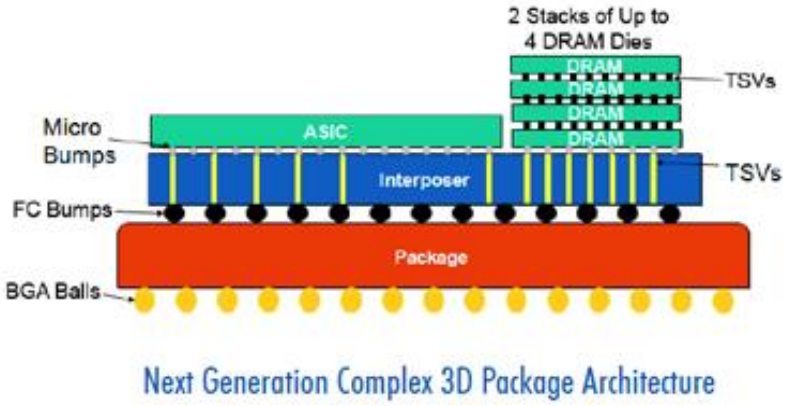


Figure 2-3: Next generation complex 3D package architecture (Courtesy of Amkor)

The adoption of BGA and flip chip technologies has brought great success to the microelectronic industry. However, new challenges come along with the success. The solder balls are now hidden from view between the chip and the substrate, which makes it very difficult to non-destructively inspect and evaluate the quality of the solder balls. Consequently, there is now a great need for quality and reliability assurance of the solder ball interconnections in electronic packages.

2.3 Assembly Process of SMDs

2.3.1 Flip Chip on Board (FCOB) Package

The assembly of the FCOB package, also called direct chip attachment (DCA) is a process of bonding the active side of the silicon die onto the board using solder bumps. The general assembly process is illustrated in Figure 2-4. The first step is a fluxing operation. Flux is a weak acid material which removes oxides from the bonding surfaces and protects the surfaces against further oxidation during the reflow soldering process. It can be applied either by dipping the flip chip into a level flux bath or flux can be dispensed onto the actual substrate bond sites. Once the flux is applied to the wettable surfaces, a pick-and-place machine places the chip onto the substrate. This assembled chip goes through a convection reflow oven. A reflow temperature profile controls the temperatures of different zones in the reflow oven. During the reflow process the flux is activated, and it cleans the wettable surfaces, preventing the surfaces from re-oxidizing [27]. When the reflow temperature rises to the melting point of the solder, the solder bumps become molten and adhere to the substrate pads. Finally, the formation of solder connections is completed during the cooling down.

The substrate and PCB are usually made of organic material, which introduces a large mismatch of the coefficient of thermal expansion (CTE) with silicon. This will cause a severe reliability issue and decrease the life of the assembly dramatically. To

address this reliability issue, underfill is used. Underfill is a polymer adhesive material (usually an epoxy based material) that is able to absorb and redistribute the stress induced by a mismatch of CTE. So after the formation of solder interconnections, underfill is dispensed to fill the gap between the bottom of the chip and the top of the substrate. The underfill is then cured in a thermal chamber at a given temperature for a given duration of time. In addition, underfill can effectively "glue" the package to the PCB to improve drop-test performance. Flip chip packages with underfill usually have a service life at least 10 times longer than those packages without underfill.

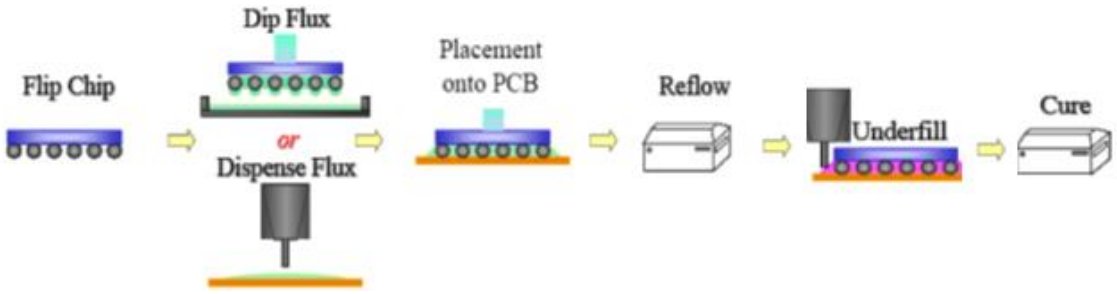


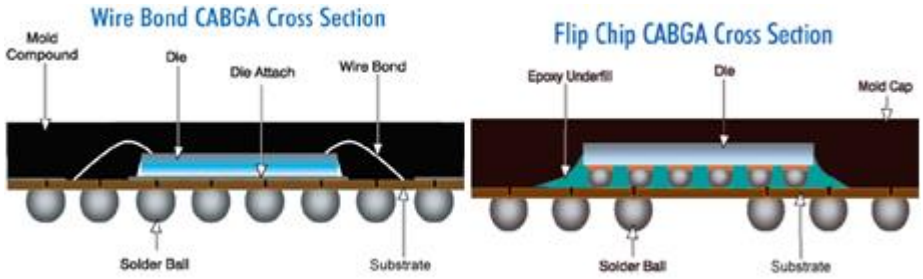
Figure 2-4: Assembly process of FCOB package

2.3.2 Ball Grid Array Package

Based on the materials of the substrate, BGA packages can be classified into two categories: ceramic BGA (CBGA) and plastic BGA (PBGA). The CBGA package is the earliest type of BGA package, with its substrate made of ceramics, like alumina. Plastic substrates made of organic laminate eventually replaced ceramic substrates because of their lower cost, lower density and better electrical performance. What's more important, the coefficient of thermal expansion (CTE) mismatch between organic laminate and

PWB is very small, which leads to much better reliability for PBGA. Now PBGA is much more popular than CBGA.

Based on the technologies used in the 1st level interconnections, BGA packages can also be classified into two categories: wire bond BGA and flip chip BGA (FCBGA). Their cross-section images are shown in Figure 2-5. In the figure, CABGA refers to ChipArray BGA, which is one type of BGA package with a small height. In the wire bond BGA package, the active side of the silicon die is face up and wires serve as the interconnections between the die and the substrate. In a FCBGA package, the active side of the silicon die is flipped down and the solder bumps build the connection between the die and the substrate.



(a) (b)

Figure 2-5: Cross sections of BGA (a) wire bond BGA, and (b) flip chip BGA (Courtesy of Amkor)

The general assembly process of BGA packages is very similar to that of FCOB packages as shown in Figure 2-4, except for two steps. First, the fluxing operation is replaced by the use of solder paste printing, during which a stencil is used to apply the solder paste to the copper pads on the bare PWB. The solder paste contains the solder

material and the flux. The flux has the same function as in FCOB assembly, i.e. oxidation removal and prevention. Additionally, solder paste is very tacky; therefore, it serves as glue and temporarily holds the BGA package in place prior to the reflow process. Secondly, BGA packages usually don't need underfill to improve their reliability. Because the BGA substrate and PCB are usually made of similar material, there is a good match of the coefficient of thermal expansion (CTE). Therefore, the solder balls on 2nd level packaging are only subjected to low stress during service.

2.4 Quality and Reliability of Solder Joint

Quality and reliability are key considerations that cannot be overlooked in the development of new packages. Quality is defined as conformance to the set standard of a product when it arrives to the customer, and reliability is the probability that a product can perform its intended function for a given time under specified operating conditions[5].

The solder joint is one of the most vulnerable parts in the electronic products, and it can be subject to a number of quality and reliability defects. Based on when the defects are introduced, the defects can be classified into two categories: process-induced defects and service-induced defects. As the name implies, process-induced defects refer to defects introduced during assembly. Common process-induced solder ball defects include

cracked, head-in-pillow (HIP), open, poor-wetting, starved, misaligned, missing, and voids.

In a recent investigation lead by Oresjo S. [28], a large number of solder joints from different component types were inspected. Different component types were examined, including BGAs, quad flat packs (QPFs), connectors, chip resistors, and chip capacitors with different sizes and pitches. The study revealed that the average defect level in industry was 1079 ppm (parts per million). The most common defects are opens (48 percent), shorts (23 percent), insufficient solder (15 percent), and missing components (4 percent), as shown in Figure 2-6.

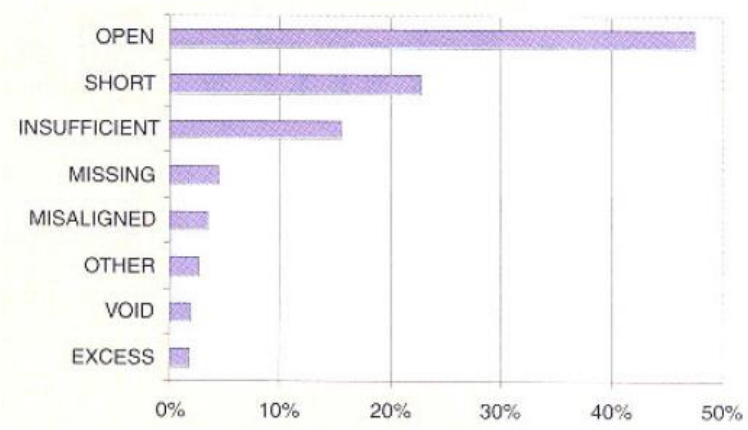


Figure 2-6: Defect type spectrum

Service-induced defects refer to defects introduced during service. The reliability issues of solder balls are mainly caused by the operating conditions of the electronic products. These defects can act either as sources for instantaneous catastrophic failures or as latent defects that can affect long term reliability. We can classify the fatigue

mechanisms of solder balls into three types, including temperature related, displacement related and acceleration related. For example, electronic products used in automotive underhood applications [29] are usually subjected to temperature and displacement related loadings. R. Tummala reported that fatigue of solder joints in electronic assemblies is believed to play a role in 90% of all structural and electrical failures [5]. However, it takes a long time from the start of fatigue until failure. Obtaining such life data (or times-to-failure data) may be very difficult or impossible. What's more, enterprises and researchers cannot afford the necessary testing time due to very limited time between product design and release. For example, the release of the next generation of smart phones and tablets usually comes within two years. Given these difficulties and the need to observe times-to-failure data to better understand the failure modes and life characteristics, products are placed into more serve use conditions to force them to fail more quickly; this is known as accelerated life testing. As mentioned earlier, temperature related, displacement related and acceleration related fatigue are three major types of fatigue mechanism. And the accelerated life testing is designed to induce such failure mechanisms.

2.4.1 Temperature related Accelerated Life Testing

Accelerated thermal cycling (ATC) is the most common temperature related accelerated life testing. In ATC, electronic packages are put into a thermal cycling

chamber, where a temperature profile is cycling. The temperature range is much more severe than service temperatures under regular conditions. The most common temperature profile is from -40 to +125 degree Celsius. Because there is a CTE mismatch between package constitutions, package constitutions will deform because of the thermal strain. Figure 2-7 shows the deformation of a simple electronic packaging structure under cooling and heating. Meanwhile, cyclic thermal stress is applied to the solder joints, which eventually introduces crack initiation, then crack propagation and finally through crack. The through crack leads to an open circuit. Therefore, a resistance test is usually used to monitor crack development. It can be implemented either in-situ or off-line with certain internals.

However, when compared with the actual thermal distributions in electronic devices, thermal cycling testing is not a realistic representative. In thermal cycling, whole packages are nearly at the uniform temperature all the time and only negligible thermal gradients exist within the mounted package [30]. To address this issue, power cycling is proposed, where the temperature distributions simulats as closely as possible actual operational conditions by increasing the temperature of the die when the power is “on ” and allowing a natural temperature decrease when the power is “off " [30].

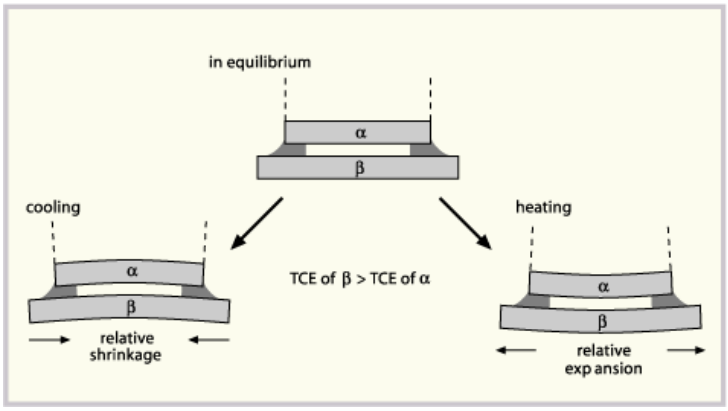


Figure 2-7: Deformation of a simple electronic packaging structure under cooling and heating (Source: http://www.ami.ac.uk/courses/topics/0162_sctm/)

2.4.2 Displacement related Accelerated Life Testing

Mechanical bending is a typical displacement related accelerated life test. Three- and four-point mechanical bending are common test setups. Figure 2-8 [31] shows an example of a three-point bending setup, and a four-point bending setup is seen in Figure 2-9 [32]. Controlled displacement is applied to the contacting head. Generally speaking, the four-point bending test is better than the three-point bending test because of the constant moment applied to the board. During cyclic bending, solder balls are subject to cyclic strain and stress until the yielding point of the solder ball is reached. Then the solder ball crack initiates and propagates till the formation of a through crack. Beside solder ball cracking, pad cratering is another typical failure mode during mechanical bending. Pad cratering refers to the initiation and propagation of fine cracks beneath the copper pads in the organic substrate materials or PCB laminates [18]. Resistance

monitoring and strain monitoring are usually configured on the test boards to record the reliability data for future analysis.

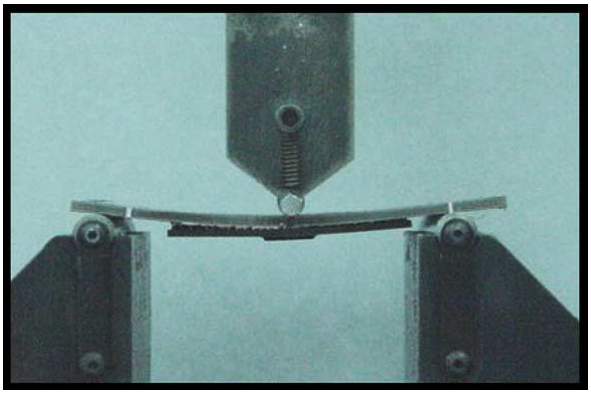


Figure 2-8: Three-point bending setup

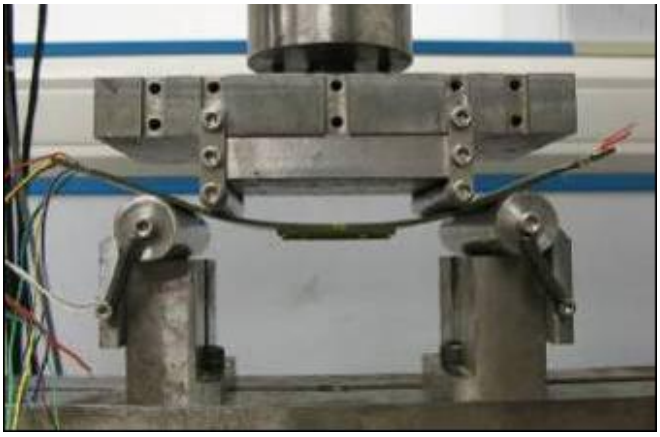


Figure 2-9: Four-point bending setup

2.4.3 Acceleration related Accelerated Life Testing

The drop test is the most typical kind of acceleration related accelerated life testing. Figure 2-10 [33] shows a schematic of a drop test and how acceleration changes over time. In the test, the test vehicle is mounted on the base plate with its corners fixed on the

standoffs while the base plate is welded to the drop table. The drop table is released at a certain height to hit on the strike surface [33]. An accelerometer is attached to the base plate to monitor the acceleration. Compared to the previous two types of accelerated life testing, solder ball failure in a drop test is very different. It's a purely brittle fracture, while ductile fractures dominate in the previous two types of accelerated life testing. There is almost no phase for crack propagation because of the transient shock in the drop test. As portable electronics are booming, acceleration related accelerated life testing plays a key role in product characterization.

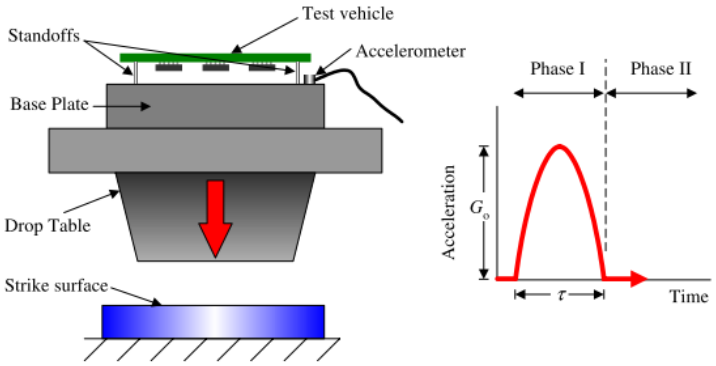


Figure 2-10: Schematic of a typical drop test and acceleration signal

In addition, humidity related accelerated life testing [34] is common, especially for electronic packages with polymer encapsulation, for example, PBGA package with molding compound on top. The polymer material is susceptible to water absorption. Moisture diffusing through the polymer can transport ions to the die surface and other interfaces and possibly cause electrical current leakage, corrosion and delamination.

The current trend in the electronic industry is to make products that are compact, miniature, high density, environment-friendly and low-cost. Scaling demands are driving the ball size and ball pitch to the limits of current technologies. As the ball size decreases, assembly defects are more likely to appear, since an assembly process with a tight tolerance is required. Meanwhile, the smaller solder ball becomes less compliant, making it more susceptible to thermal and mechanical failures. Higher processing temperatures required for lead-free materials increase thermal stresses, which will cause solder balls to fail during manufacturing or in service.

In summary, these trends further intensify the focus on the quality and reliability of the solder joints. At the same time, these trends also place an ever-increasing challenge on technologies that are capable of identifying solder ball defects non-destructively. Higher I/O density and smaller ball size will require a solder joint inspection system with higher resolution. If the solder joint defects can be detected as early as possible, the quality and reliability of such a package can be improved through rework, and this will save the microelectronic industry millions of dollars per year.

2.5 Finite Element Method

Even though the accelerated life testing expedites the failure of the electronic products, however, it is still very expensive and time-consuming to do accelerated life testing. Finite element method (FEM) analysis is proposed to overcome the limitations

of the accelerated life testing. FEM has several advantages. First of all, it is very flexible because the geometry, material properties and loading conditions can be easily changed, which provides tremendous values to the product designers. Then, FEM can save a lot of money and resources which should have been invested onto the actual accelerated life testing. A finite element analysis (FEA) usually starts with material properties setup, geometric modeling, meshing, loading, solving and finally post-possessing. Figure 2-11 [35] shows an example of one-quarter modeling of a PBGA chip.

FEM has been widely used to study the reliability of the electronic products [35-37], especially the solder joint reliability and it has demonstrated its capability. However, standalone FEA is inconclusive without any actual accelerated life testing results. In FEA, the experimental parameters get simplified. For example, the material properties are assumed to be linear, isotropic and temperature independent. In a word, FEA can never replace the actual accelerated life testing; however, it provides a flexible and convenient way to investigate reliability.

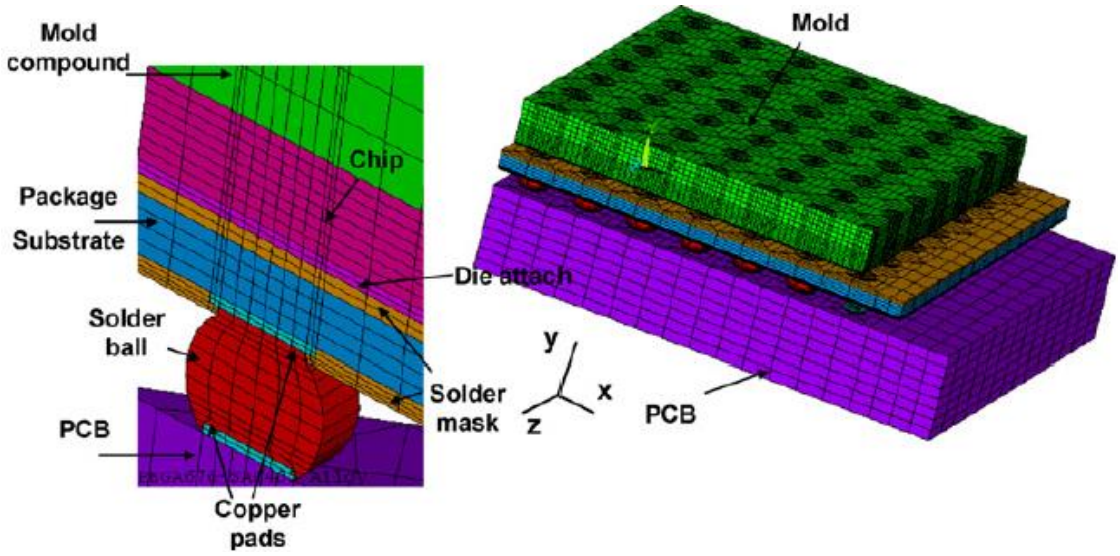


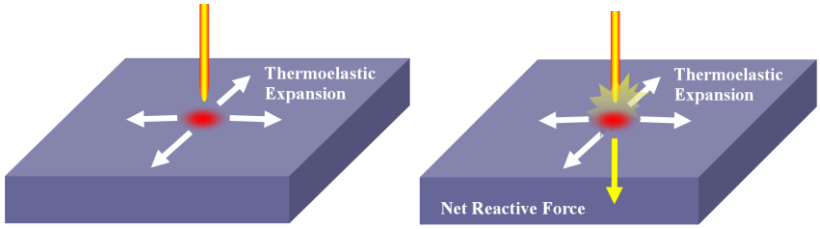
Figure 2-11: A one-quarter modeling of a PBGA chip

2.5 Laser Ultrasound Generation and Detection

Using pulsed lasers to generate ultrasound is beneficial due to its noncontact nature. Unlike traditional contact piezoelectric transducers (PZTs), pulsed lasers do not require couplants on the surfaces of samples [38]. This makes laser ultrasound convenient and suitable for automated inspection. Depending on the laser power density, there are two main regimes of laser-generated ultrasound: thermoelastic regime and ablation regime. When the incident power density on the area illuminated by the laser is relatively low and the local temperature is below the melting point of the material, ultrasound is generated through the thermoelastic mechanism [39].

As shown in Figure 2-12(a), the incident laser beam rapidly heats up a thin layer of material on the top surface. The heated region expands through the thermoelastic effect and axially symmetric tensile stresses are generated. The heated portion is then followed

by a slower contraction as the laser pulse is momentarily shut off. The rapid expansion and contraction create ultrasound which propagates through the sample. If the local temperature rises very rapidly and higher than the melting point of the surface materials, local vaporization and ejection of small particles occurs, as shown in Figure 2-12(b). This phenomenon is called ablation, and it can be used for cutting and cleaning in industrial processes [11]. In order to avoid any surface damage to the packaged electronic devices in the non-destructive laser ultrasound inspection system, the laser power is controlled within the thermoelastic regime.



(a) (b)

Figure 2-12: Ultrasound generation in (a) thermoelastic regime, and (b) ablation regime

The optical detection techniques for ultrasound can be classified into interferometric and non-interferometric techniques. Since the amplitude of ultrasound generated in the thermoelastic regime lies in the micro or even nano-scale, the interferometric technique is preferred due to its high measurement resolution. Figure 2-13 illustrates how a heterodyne Michelson optic fiber interferometer is used for ultrasound detection. The heterodyne interferometer is a two-beam interferometer with a reference arm and an object arm

reflected from the object. The two beams to be mixed are of slightly different optical frequencies. Typically, this is obtained by passing a laser beam through an acousto-optical modulator (Bragg cell). The frequency shifted beam (of frequency $\Omega + \omega_B$) will be refracted at a different angle and will serve as the reference arm. The unaltered beam (of frequency Ω) will be the object beam. Both beams pass through a beam-splitter and are collected by the optical detector. The heterodyne interferometer has a broad detection bandwidth and a good immunity to ambient vibrations. The optic fiber interferometer also adds flexibility in configuring the system [40].

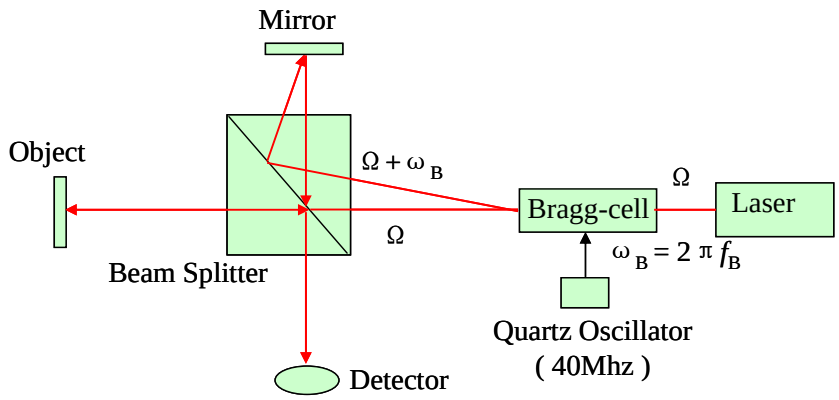


Figure 2-13: Schematic of heterodyne interferometer

2.6 Signal Processing for LUI Signals

To evaluate the solder ball quality, LUI signals need to be processed and analyzed. A number of signal-processing methods, both in the time and frequency domains, have been implemented. Liu [41] used Periodogram averaging to analyze the signal power density

distribution in the frequency domain. A frequency shift between the reference signal from a good sample and the signal measured from a defective sample was observed as well. However, the frequency changes caused by solder ball defects are very subtle, and are usually below the frequency resolution on the spectrum. Liu [41] also proposed the error ratio (ER) method to compare signals directly in the time domain. This method integrates the squared error between the measured and referenced signals and then normalizes this integrated value by the total energy of the reference signal, as represented by Equation 2.1, where *f(t)* is the measured signal and *r(t)* is the reference signal. As the defect grows severe, the ER value gets larger. Since a number of factors besides the solder joint integrity itself affect the ER values, there are some limitations with this method. The scale of the ER depends on the device being tested and should only be used for relative comparisons between similar product types. This limitation makes it difficult to set up a universal threshold ER to separate defective samples from reference samples. Meanwhile, ER values can also be affected by laser power fluctuation [42]. Alternatively, Zhang [42] proposed the Modified Correlation Coefficient (MCC) method to analyze the time domain signals in a statistical way, as shown in Equation 2.2. The MCC is a normalized measure of the strength of the linear relationship between signals, and each measured result is a number between 0 and 1. When the correlation result equals to 1, the two signals are independent, and when it is close or equal to 0, the two signals have strong linear dependence. In other words, similar samples will have a relatively low MCC, while

dissimilar samples will have a relatively high MCC. Large MCC values indicate that the chip under test is not similar to the known-good reference, which brings the quality of the solder balls in the chip under inspection into question.

$$Error\ Ratio = \frac{\int [f(t) - r(t)]^2 dt}{\int [r(t)]^2 dt} \tag{2.1}$$

$$MCC = 1 - \left(\frac{\sum_n (R_n - \bar{R})(A_n - \bar{A})}{\sqrt{(\sum_n (R_n - \bar{R})^2)(\sum_n (A_n - \bar{A})^2}} \right)^2$$

$$where \begin{cases} R_n: reference\ signal,\ \bar{R}:\ mean\ of\ R_n \\ A_n: measured\ signal,\ \bar{A}:\ mean\ of\ A_n \\ n\ is\ the\ sample\ length\ of\ the\ signal \end{cases} \tag{2.2}$$

The transient out-of-plane displacement signal induced by the laser pulse is intrinsically non-stationary and broadband, with frequencies ranging from kilohertz to megahertz. FFT-based power spectrum analysis, Error Ratio and MCC methods all use raw transient responses from the entire frequency range to extract and quantify the difference between different signals. However, defect features are more prominent in specific frequency ranges rather than being evenly spread across the whole frequency range. The data analysis in the whole frequency range might obscure the frequency components that are most sensitive to the defects. To overcome this problem, Yang [43, 44] developed wavelet analysis and local temporal coherence (LTC) analysis methods. The advantage of wavelet analysis is that it can decompose a signal into a series of wavelet components, each of which is a time-domain signal that covers a specific frequency band, and allows

identification of local features from the scale of wavelets. LTC is a measure of time-dependent shape differences between two signals, and it emphasizes the short-time coherence between signals [45], which is very suitable for the LUI signals that are intrinsically non-stationary.

However, all of these signal processing methods require a known-good reference chip for comparison, which typically involves expensive testing using alternate non-destructive methods. In addition, using a single known-good chip totally ignores the manufacturing variations, which may introduce statistical insignificance. This drawback largely limits the application of this inspection system.

A signal processing method developed by Zhang based on structural symmetry is used to overcome this limitation. The precondition of this method is that the solder ball layout and inspection pattern of the chip under test are symmetric. The LUI signals from symmetric inspection locations on a good chip should be very similar to one another. However, structural symmetry in the defective chip is jeopardized because of the presence of defect(s) and the signals from symmetric inspection locations may demonstrate differences. Even though this symmetric method eliminates the need of a known-good reference chip, it requires the symmetric solder ball layout and inspection pattern, which is not present in all the test cases.

Researchers have investigated other methods to process LUI signals. Blouin et. al [46] proposed a Synthetic Aperture Focusing Technique (SAFT) to improve flaw

detectability and spatial resolution during detection of small defects within a material. In SAFT, the pulse-echo measurements made at a series of locations are combined to form a map of the ultrasonic reflectivity of the insonified region of interest. The flaw re-radiates and alters the acoustic field, which can be identified based on the reconstructed map. Experiments were performed on an aluminum test specimen with a contoured back surface and two flat-bottom holes drilled in it. And it is demonstrated that SAFT data processing improves flaw detectability and spatial resolution. Wu et al. [47] used a wavenumber-frequency domain filtering technique to process the laser-generated signals for defect detection in welding. 2D Fourier fast transform (FFT) was implemented to compute the filtering results in the wave-number and frequency domains. Then the characteristic of the LUI signals can be extracted based on the filtering results, such as wave speed and wave type. In the experimental setups mentioned previously, the distance between the ultrasound generation location and the location of the detection sensors is much larger than the ultrasound wavelength. Therefore, the processing methods mainly focus on the physical features of the laser-generated ultrasound waves, including time of flight, wave speed, wave frequency, wave number etc. However, in the proposed LUI system for solder ball inspection, the laser incident point is very close to the laser interferometer because of the small size of the chip package. As the chip package size continues to shrink, it will be more and more difficult to implement these processing methods and extract information related to the wave characters. Therefore, signal

processing methods that are suitable for this specific application are really needed to address the limitations.

CHAPTER 3 LASER ULTRASOUND AND INTERFEROMETRIC INSPECTION SYSTEM

Figure 3-1 shows the schematic of the laser ultrasonic-interferometric inspection (LUI) system that has been developed for this work. The system consists of (a) a pulsed neodymium-doped yttrium aluminum garnet (Nd:YAG) laser to generate the laser pulses, (b) a fiber optic beam delivery system to transmit laser pulses onto the package surface, (c) a laser Doppler vibrometer that captures the transient out-of-plane displacement responses with an ultrasonic arrival on the package surface, (d) an autofocus system to adjust the standoff height between the laser Doppler vibrometer head and the surface of the chip under test to achieve the optimal signal strength [48] (e) an automated X-Y positioning table to position the packages to be tested, (f) a manual stage sitting on the automated positioning stage to adjust the position of the laser excitation spot on the package surface, (f) a vision system to determine the location of the packages by capturing the fiducials on the PWBs, and (g) a PC to coordinate the operations of these components and to acquire and process the transient displacement responses. Figure 3-2 shows a ball grid array (BGA) package being inspected with the laser ultrasound-interferometric system.

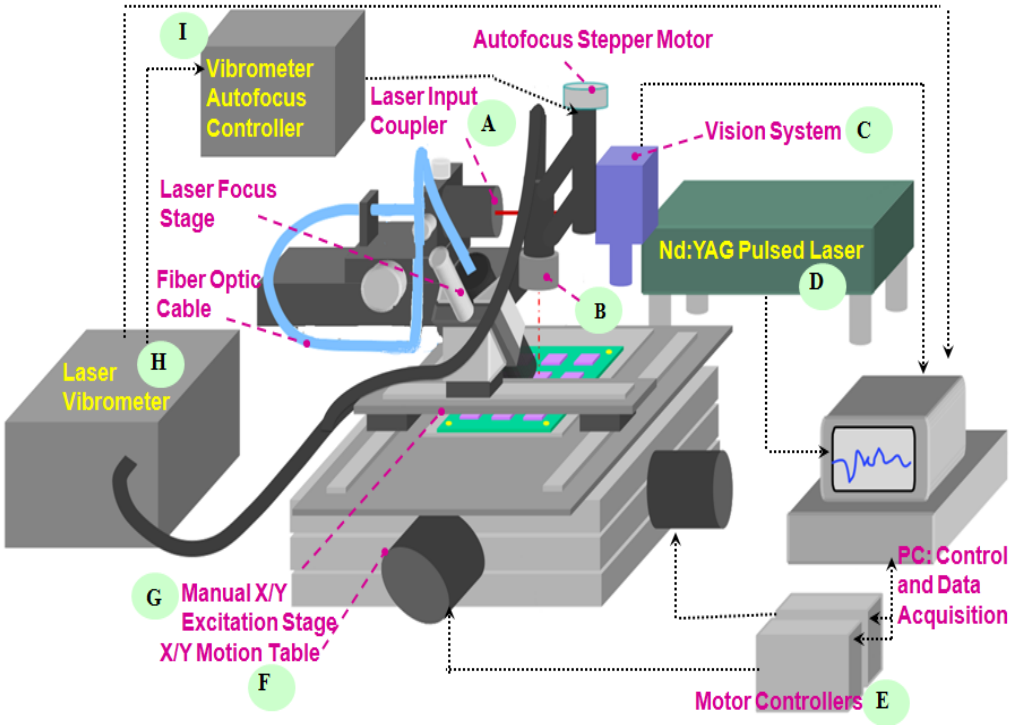


Figure 3-1: Schematic of laser ultrasonic-interferometric inspection (LUI) system

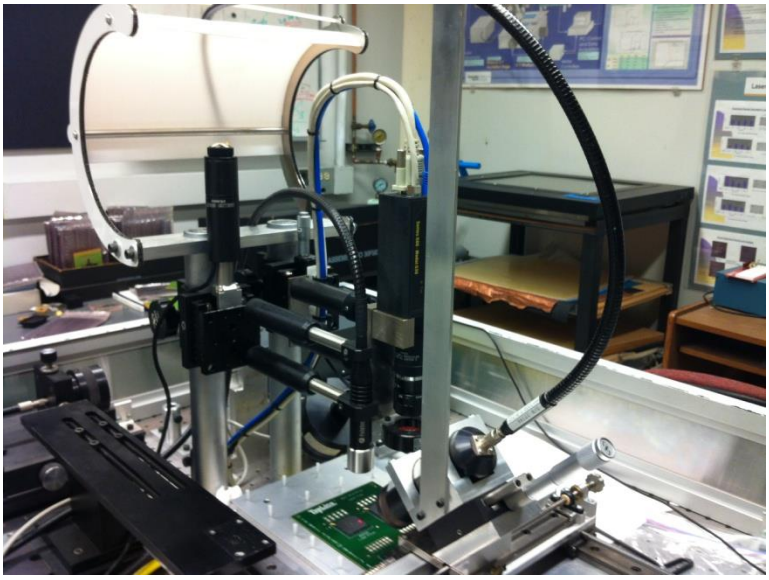


Figure 3-2: BGA package being inspected with laser ultrasound-interferometric system

In this chapter, the inspection system hardware and control software will be described.

In addition, the alignment procedure is covered. Finally, the system resolution and throughput will be discussed.

3.1 System Hardware

3.1.1 Pulsed Nd:YAG Laser

A Polaris II Q-switched Nd:YAG laser system from New Wave Research, shown in Figure 3-3, was used as the pulsed laser source. The pulsed Nd:YAG laser generates laser pulses with a duration of 4~5 ns at the wavelength of 1064 nm. The repetition rate of the laser can be adjusted from 1 to 20 Hz. The pulse energy is adjustable through a motorized optical attenuator, and it can be measured by a laser power meter, as shown in Figure 3-4. The proper laser energy level needs to be determined for different types of test vehicles. An excessive energy level will damage the chip surface, while an insufficient energy level cannot generate the ultrasonic response with enough strength. The diameter of the laser beam is 3 mm. After 30-minute of warm up, the energy stability pulse by pulse is over 98% for 10,000 shots.

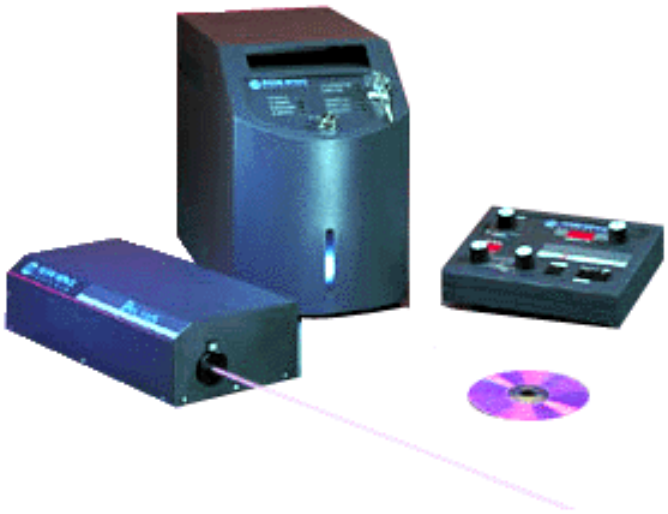


Figure 3-3: Pulsed Nd:YAG laser system (Source: New Wave Research®)

Figure 3-4: Laser Power Meter (Source: www.directindustry.com)

3.1.2 Fiber Optic Beam Delivery System

The delivery of nanosecond scale laser pulses in the mJ energy range through optical fibers was a challenging task. Fused silica fiber was chosen due to its high damage threshold. The goal of the fiber delivery system is to deliver the required pulsed laser through one fiber with minimal energy loss and maximal flexibility. This delivery system

is from US Laser Corporation, with its schematic seen in Figure 3-5 [49]. It consists of an input coupling assembly, a rugged fiber optic cable with a 600 μm core diameter and an output focusing objective.

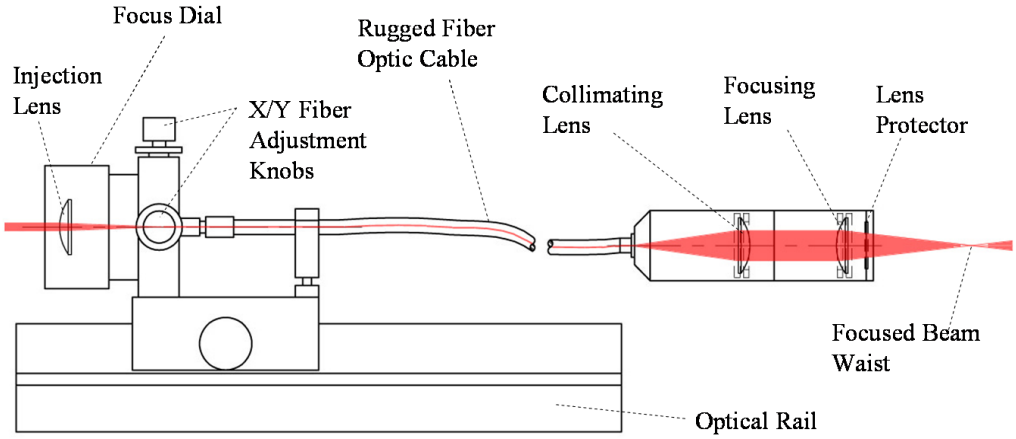


Figure 3-5: Fiber optic laser beam delivery system

3.1.3 Laser Doppler Vibrometer

In the system, a laser Doppler vibrometer is used to capture the transient out-of-plane displacements in nanometer scale induced by laser-generated ultrasound. As shown in Figure 3-7 and Figure 3-9, this laser Doppler vibrometer consists of a heterodyne fiber optic interferometer model OFV-511 and an ultrasonic vibrometer controller OFV-2570, both from Polytec®. The operating principle of the heterodyne interferometer is shown in Figure 2-13. The vibrometer is used to directly measure the transient out-of-plane displacement responses on the package surface. Its sensor head is positioned perpendicular

to the sample surface. A red continuous laser beam with a wavelength of 650nm is delivered by the senor head to the sample surface. The laser has a spot size of 3 μm to facilitate a high spatial resolution. The vibrometer controller incorporates a velocity decoder with bandwidth up to 10 MHz bandwidth and a displacement decoder with the bandwidth up to 24 MHz. In this work, only the displacement decoder is used. The maximum displacement it can measure is 75 nm. The vibrometer has a high displacement measurement resolution of 0.3 nm. At each inspection point, multiple measurements were taken under a series of laser pulses and were then averaged to suppress noise. Additionally, the vibrometer controller has an LED display for the control settings and signal level display. The signal level data gave feedback to the autofocus system to improve the signal-to-noise ratio (SNR).

Figure 3-6: Polytec OFV-511 heterodyne interferometer (Source: Polytec®)

Figure 3-7: Polytec OFV-2570 vibrometer controller (Source: Polytec®)

3.1.4 Vision System for System Alignment

Fiducial marks are circular, square or cross-shaped solid pads on printed wiring boards; they are a common feature of printed wiring boards. During assembly, the fiducial marks serve as reference features for pick-and-place machines that use vision systems to accurately place components on their corresponding bond pads. Figure 3-8 shows an example of a circular fiducial mark and a cross-shaped fiducial mark on a PWB. In this research work, the fiducial marks are used in a similar way to align the specimen under test so that the inspection points and laser excitation points are precisely located. The smart

sensor DVT Series 600 (shown in Figure 3-9) was selected for this research. It uses a 3.6 x 4.8 mm CCD with 480 x 640 pixel resolution. This sensor produces 8-bit grayscale images and incorporates a number of useful software tools for easy image processing. An Ethernet port is used as the communication port between the camera and the control PC.

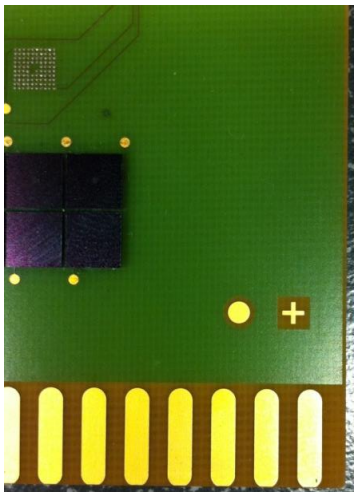


Figure 3-8: A circular fiducial mark and a cross-shaped fiducial mark on a PWB

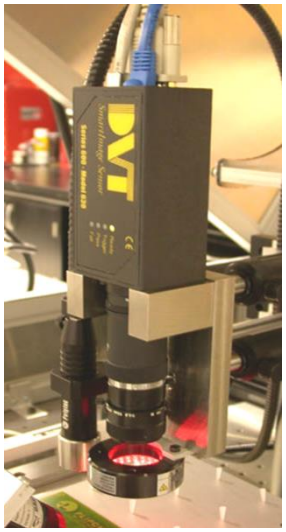
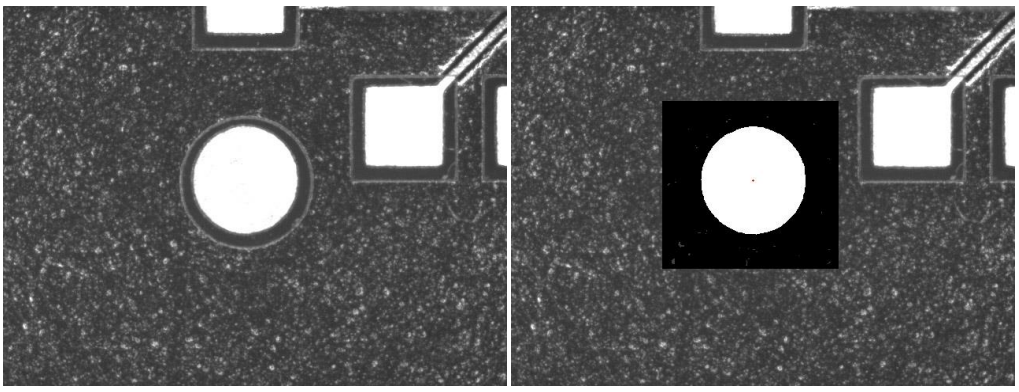


Figure 3-9: DVT series 600 smart sensor for fiducial mark locating

The software, called FrameWork, was provided with the sensor to manage and operate the DVT smart sensor. In FrameWork, the “blob” software tool was selected for fiducial mark locating. The tool can group light or dark pixels together and then calculate the centroid position of the resulting blob of pixels; this is ideal for fiducial measurement because fiducial marks are often gold plated pads against the high contrast background of the substrate material, forming a bright spot in an image. The vision system comes with an alignment and calibration procedure to find the actual scale factor between units of pixels and real distance units, as well as to eliminate image distortion [49].

The fiducial marks are measured with sub-micron resolution and ±1.0 μm repeatability in the view area of the vision system. Figure 3-10 shows the measurement of an actual fiducial mark on a test substrate [49].



(a) (b)

Figure 3-10: Blob measurement of fiducial marks: (a) raw image (b) fiducial blob

3.1.5 X-Y Positioning Table

An X-Y positioning table from Nutec Inc., as shown in Figure 3-11, features excellent

accuracy, orthogonality and bidirectional repeatability. The manufacturer's specifications claim an accuracy of 7.5 μm per 100 mm of travel, an orthogonality error of less than 7.5 arc-seconds and a bidirectional repeatability of ±1.0 μm. The precise, preloaded, crossed-roller bearings in the stage eliminated the problems with play. The precision-grade lead screw drive also provides positioning accuracy and repeatability. The motion stage has a travel of 200 mm x 200 mm as well as a large mounting surface. The positioning table positions the test boards under the vibrometer light beam for measurement. The positioning repeatability of the stage has been separately verified to be approximately ±6 μm and ±4 μm in the X and Y axis [49].

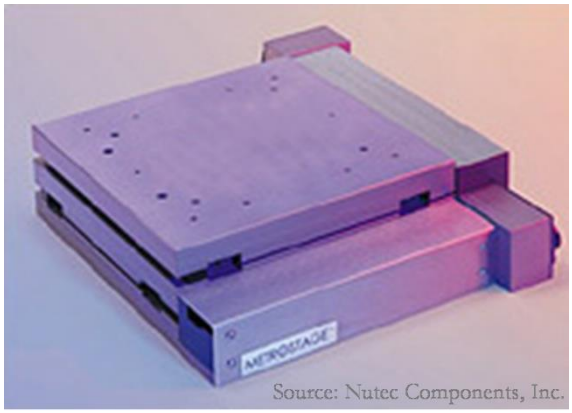


Figure 3-11: X-Y positioning table (Source: Nutec®)

3.1.6 Vacuum Fixture

A vacuum fixture, as shown in Figure 3-12, is used to constrain test boards on the X-Y positioning table in experiments. This fixture consists of a vacuum plate to hold test boards

as large as 152.4 mm x 203.2 mm. The vacuum plate has channels on its back surface to connect two vacuum ports in the fixture base plate to 48 individual ports in the vacuum plate. Two separate vacuum port arrangements were built into this fixture for holding various sizes of test boards. A precision alignment fence was again used for repeatable component placement and orientation. The vacuum plate was anodized to improve its long-term durability and scratch resistance. During inspection, the vacuum system is turned on to prevent any movement of the test boards.

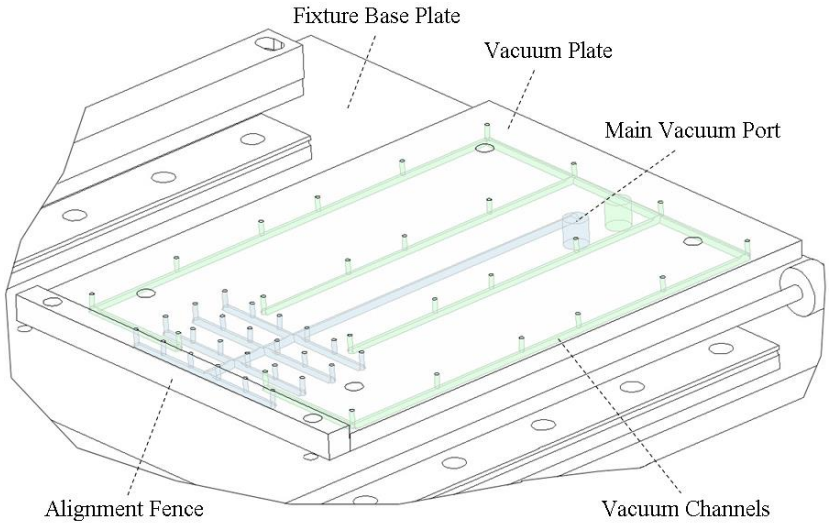


Figure 3-12: Vacuum fixture

3.1.7 Manual Laser Positioning Stage

Repeatable laser excitation positioning is realized by a manual X/Y stage shown in Figure 3-13. It uses preloaded linear motion components and linear encoders for precision positioning. The stage was designed with a locking mechanism that allowed fine

positioning through an adjustor screw when locked and rapid manual repositioning when unlocked. During inspection, the locking screws were tightened to achieve repeatable laser excitation positioning. The linear encoders have 1.0 μm resolution, and an LED display was available to display the real-time locations of the laser in X and Y directions. Overall, the stage precision was estimated at better than ±10 μm in each axis.

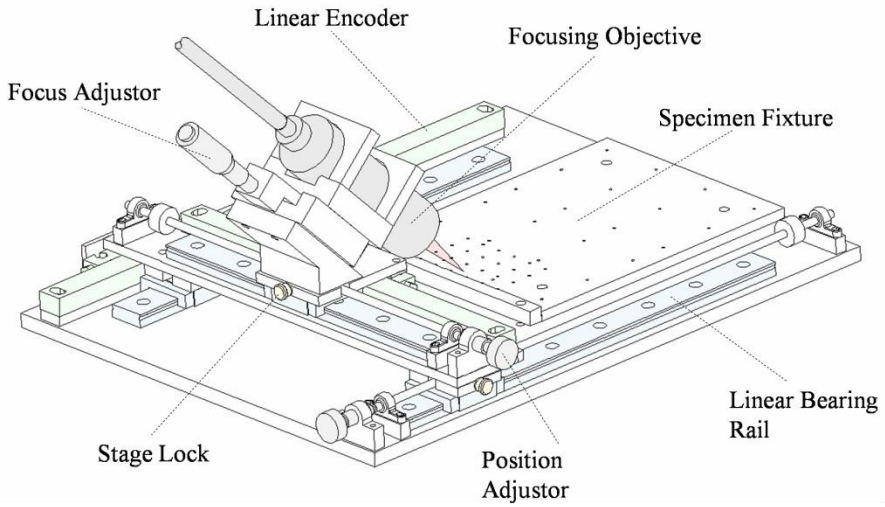


Figure 3-13: Manual X-Y laser excitation positioning stage

As shown in Figure 3-13, the manual focus stage for the output objective of the fiber optic beam delivery system was mounted on the X-Y stage with a 45° angle in order to allow the laser vibrometer to perpendicularly measure the out-of-plane displacement. This setup also causes the laser spot excited on a specimen to be elliptical instead of circular, as shown in Figure 3-14. This focus stage has a 25.0 mm of total travel, allowing the laser spot size to be adjusted over a wide range to control the laser energy density excited on the package surface. The range of possible excitation areas varies from 1.48 mm^2 to

approximately 3.81 mm^2, providing much more flexibility in adjusting the excitation spot size and then controlling the laser pulse energy density.

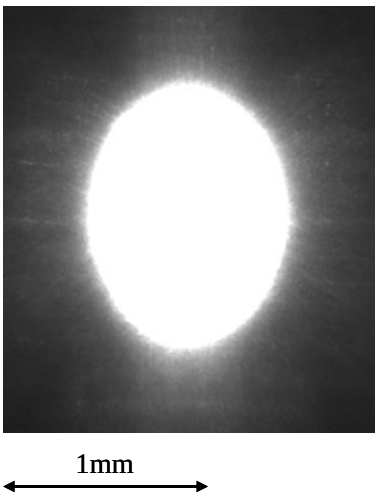


Figure 3-14: Elliptical shape of laser spot

3.1.8 Autofocus and Local-Search System

When the chip surface is smooth, a large amount of the incident laser beam can be reflected back into the laser vibrometer, which can produce a signal with good SNR. However, when the chip surface is rough, it leads to a scattered beam with speckle [50]. In this circumstance, the amount of the reflected light received by the photodetector inside the interferometer is greatly reduced. As a result, the signals received by the laser interferometer have a poor signal-to-noise ratio (SNR), which jeopardizes the accuracy of the whole measurement. To solve this issue, the vibrometer head is mounted onto a motorized linear stage. This stage controls the standoff distance between the focusing head and the chip surface with a fixed focal length, which allows the spot size of the laser to be

adjusted while searching for a desirable signal strength. The vibrometer signal intensity is fed back to the autofocusing controller. During inspection, if the initial vibrometer signal intensity is below the expectation, the motorized linear stage will adjust the standoff height between the head and the chip surface until an optimal signal intensity is achieved. Input shaping is implemented to control the motion of the linear stage for vibration reduction. Figure 3-15 shows the schematics of the autofocus system [48].

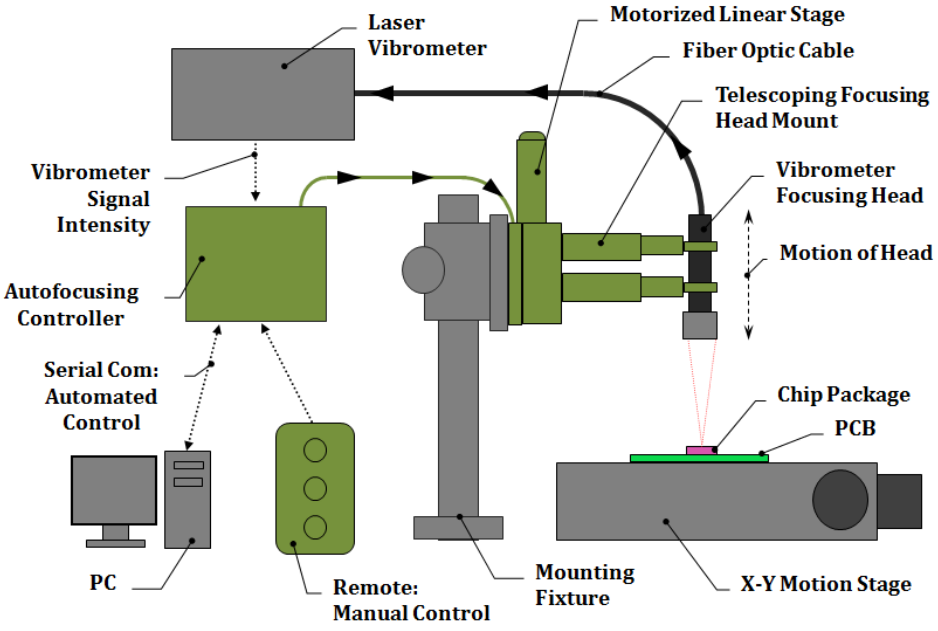


Figure 3-15: Schematic of the autofocus system

If the autofocus system still fails to focus properly, a local searching system will be implemented. In this case, the target surface is moved slightly from its initial position, and the measurement is taken again. The local search procedure can be repeated at different points around the actual measurement point chosen within the geometric grid until the

desired signal strength is achieved. Figure 3-16 shows a typical local search pattern. In this pattern, the center marker represents the initial inspection location, while the rest of the markers are the alternative inspection points with a pitch of 1 micron. Once the vibrometer signal intensity is above the desired level at one of the alternative inspection points, the local searching is terminated.

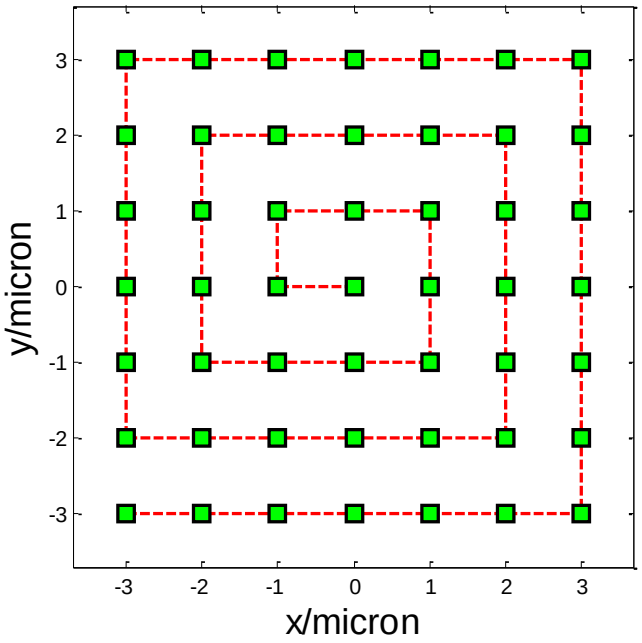


Figure 3-16: A typical local search pattern

3.1.9 DAC Board

To capture the ultrasound responses on a nanometer scale, a high-resolution and high-sampling rate data acquisition board is needed. A GaGe CompuScope 8327 PCI A/D card (as shown in Figure 3-17) was selected for this purpose. It comes with dual-channels, 14 bits resolution, various sample rates ranging from 10kHz to 125MHz. Its input ranges,

coupling and impedances can also be easily adjusted. What's more, it provides a software development kit (SDK) for Matlab, which is ideal to develop a control interface to integrate all the subsystems mentioned above.

Figure 3-17: GaGe CompuScope 8349 PCI A/D card (Source: GaGe)

3.2 System Alignment and Coordinate Transformation

Different subsystems have to be integrated to function as a whole system to enable and facilitate the inspection process. Before inspection, alignment should be first performed to build appropriate ‘recipes’ for measurement of the test boards. During the alignment, the test board is first placed and constrained on the X-Y stage with the vacuum on. Then the fiducial marks on the test board are captured and located by the vision sensor. Next the translation and rotation of the CAD frame coordinate system in the design file (Gerber file) relative to the vision sensor (CCD camera) coordinate system are calculated by using a

coordinate transformation program. Once the translation distance and rotation angle are obtained, all the coordinates in the design file can be transformed to the measurement coordinates to locate the inspection and excitation points. These inspection and excitation points are written to a text file which will be used for future inspection.

Figure 3-18 shows the components of the system with their respective coordinate frames [49]. There are four coordinate systems to describe the inspection system including the base frame of the vision sensor, the frame of the vacuum fixture, the frame of the PCB design and the local frame of a chip on the PCB.

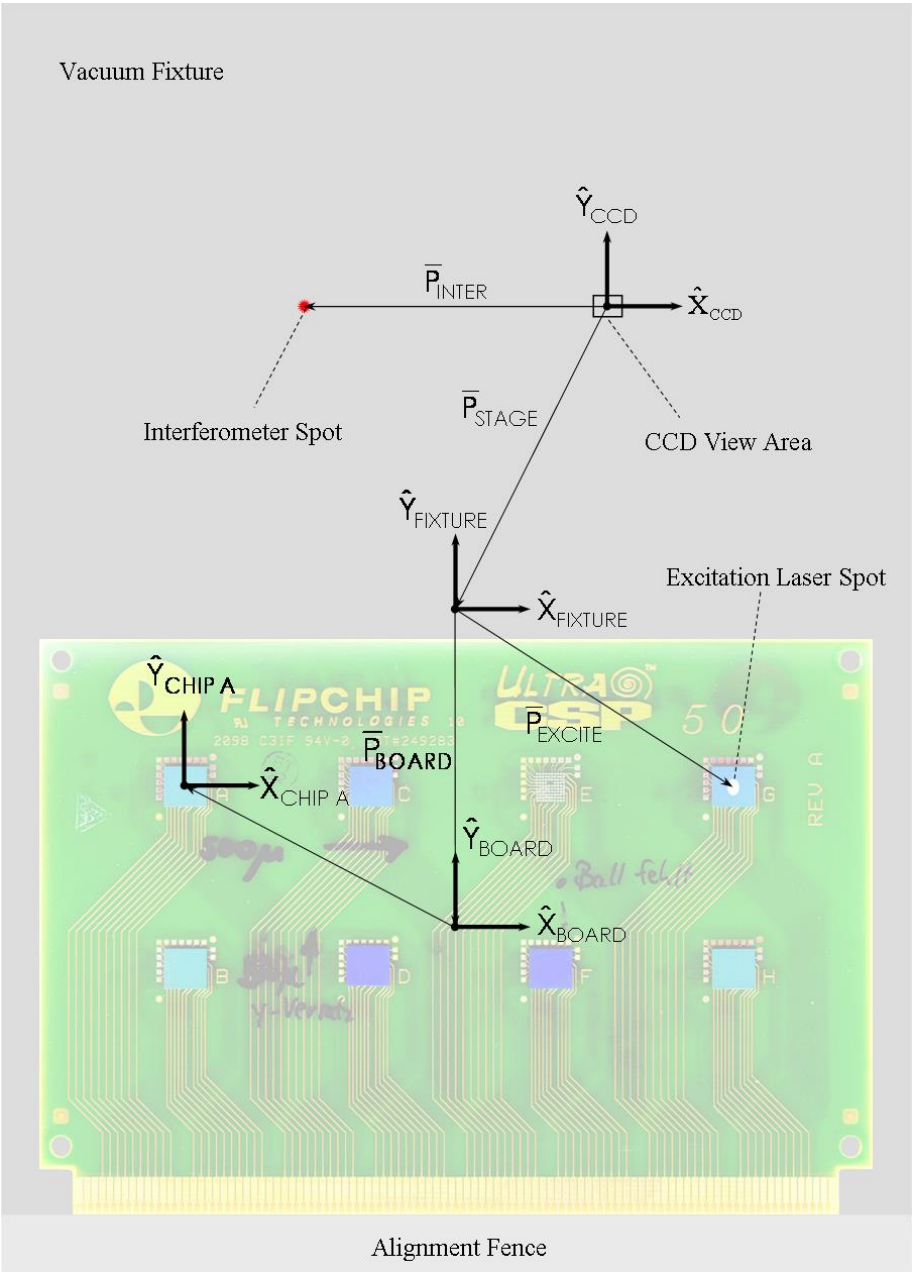


Figure 3-18: Coordinate frames for inspection: chain of coordinate frames from the base frame (CCD) to the local specimen frame

Two coordinate frames, as shown in Figure 3-18, the PCB design coordinate system (the CAD frame) and the vision sensor coordinate system (the measurement frame) are used to calculate the rigid body transformations by assuming that there is no non-linear

transformation between different parts. Two fiducial marks on the test board are measured to calculate both translation and rotation of the CAD frame relative to the vision coordinate system. Once the rigid body transformations, i.e. the translation and rotation between the two frames, are available, all the inspection and excitation locations can be transformed from the CAD frame to the measurement frame. The rotation transformation provides a skew correction allowing the sample to be arbitrarily positioned on the fixture as opposed to having to be aligned against an alignment fence.

The coordinates of a fiducial mark in the CAD frame can be denoted as (x' , y'), the coordinates of the same point in the measurement frame as (x,y), the translation between the two frames as X and Y, and the rotation between the frames as θ. The translation matrix $T(X,Y)$ in a 2-D homogeneous form can be written as [40],

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = T(X,Y) \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & X \\ 0 & 1 & Y \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-1}$$

The rotation matrix $R(z,\theta)$ can be written as,

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = R(z,\theta) \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta & 0 \\ sin\theta & cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-2}$$

The composition of XY translation and z-axis rotation is,

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = T(X,Y)R(z,\theta) \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta & X \\ sin\theta & cos\theta & Y \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{3-3}$$

Given two measured fiducial points (x_1', y'_1), (x_2', y'_2) and their coordinates *(x_1,y_1)*, *(x_2, y_2)*, in the CAD frame, the simultaneous equations are solved to calculate *sinθ, cosθ, X* and *Y as*,

$$sin\theta = \frac{(x_1'-x_2')(y_1-y_2)-(y_1'-y_2')(x_1-x_2)}{(x_1'-x_2')^2+(y_1'-y_2')^2} \quad (3\text{-}4)$$

$$cos\theta = \frac{(x_1'-x_2')(x_1-x_2)+(y_1'-y_2')(y_1-y_2)}{(x_1'-x_2')^2+(y_1'-y_2')^2} \quad (3\text{-}5)$$

$$X = x_1 - x_1'cos\theta + y_1'sin\theta \quad (3\text{-}6)$$

$$Y = y_1 - x_1'sin\theta - y_1'cos\theta \quad (3\text{-}7)$$

3.3 System Integration and Control Interface

After alignment is done, all the experimental parameters can be set up. A graphical user interface (GUI), shown in Figure 3-19, was developed using Matlab for the experimental parameter setup and experiment control. In the GUI, there are two menus, Experiment and Manual Control.

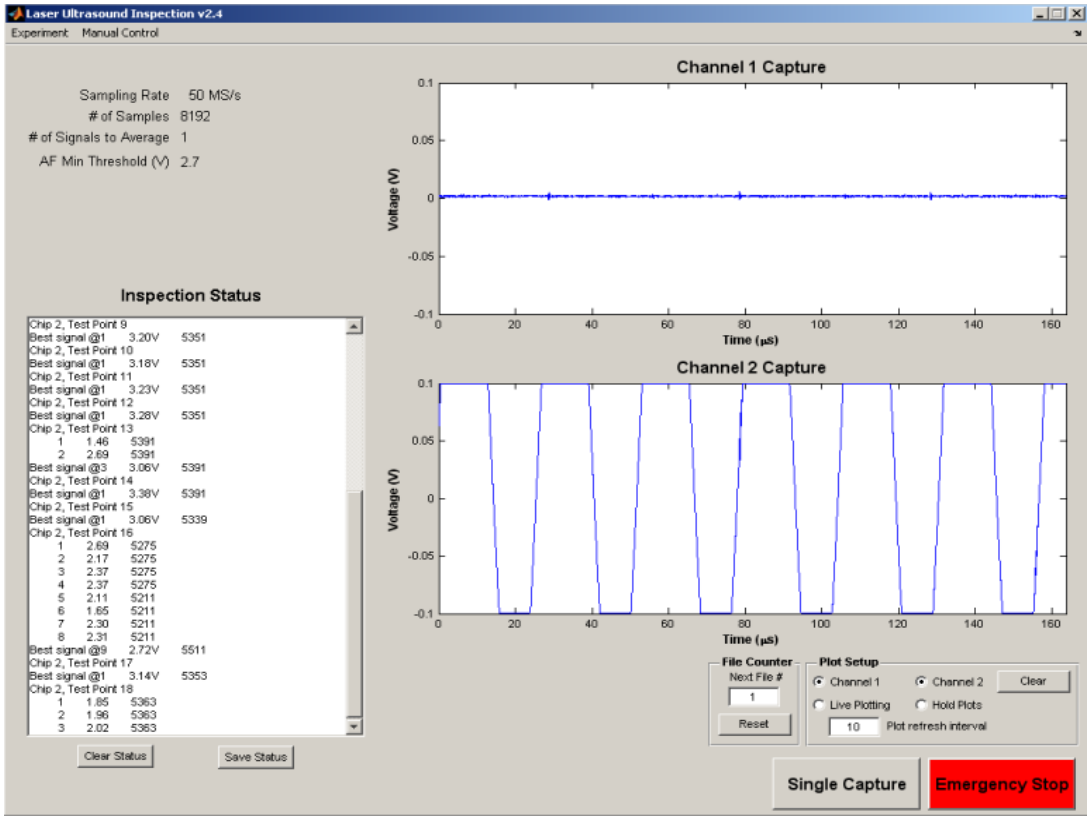


Figure 3-19: Screenshot of GUI to control inspection system

The menu of Manual Control is shown in Figure 3-20. With Manual Control, a user can perform simple controls on the laser, X-Y stage and autofocus system. It is designed mainly for routine system calibration and parameter optimization. During a typical automated inspection process, this menu is not needed.

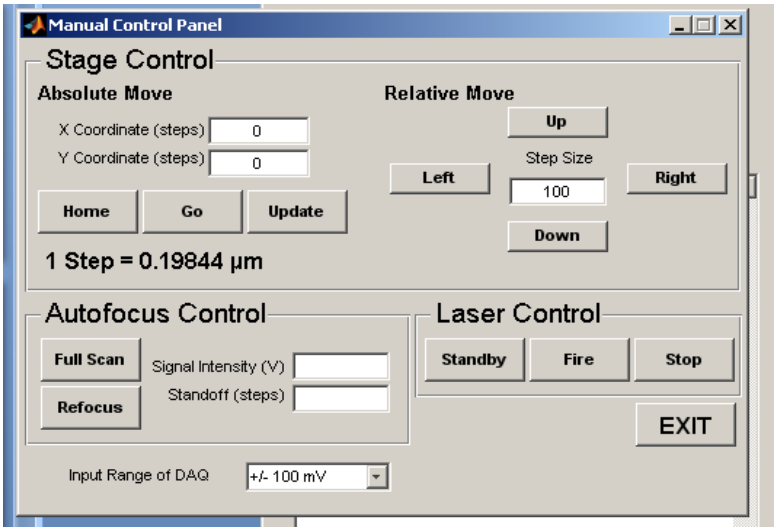


Figure 3-20: Screenshot of Manual Control GUI

The screenshot of the Experiment menu is displayed in Figure 3-21. There are 4 sub-menus: Properties, Load Test Points, Run and Exit.

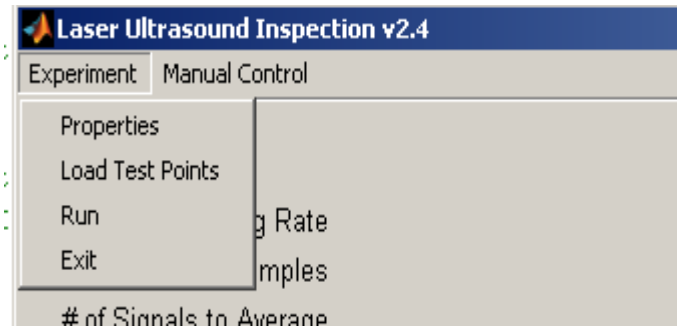


Figure 3-21: Screenshot of the Experiment menu

In the sub-menu of Properties shown in Figure 3-22, all experimental parameters can be configured here, including File Options, Data Acquisition Options, Autofocus Options, and Laser Options. In File Options, the name and saving directory of the result files can be configured. Data Acquisition Options allows the operator to set the sampling rate, number of signals to be averaged, signal length, input range, coupling, trigger and so on. In the

Autofocus Options, the operator needs to set up the minimum threshold which is the minimal signal intensity level that autofocus system has to achieve before searching stops. Meanwhile, the local search pattern needs to be configured in case the minimum threshold cannot be achieved. The laser power, repetition rate can be configured in Laser Options.

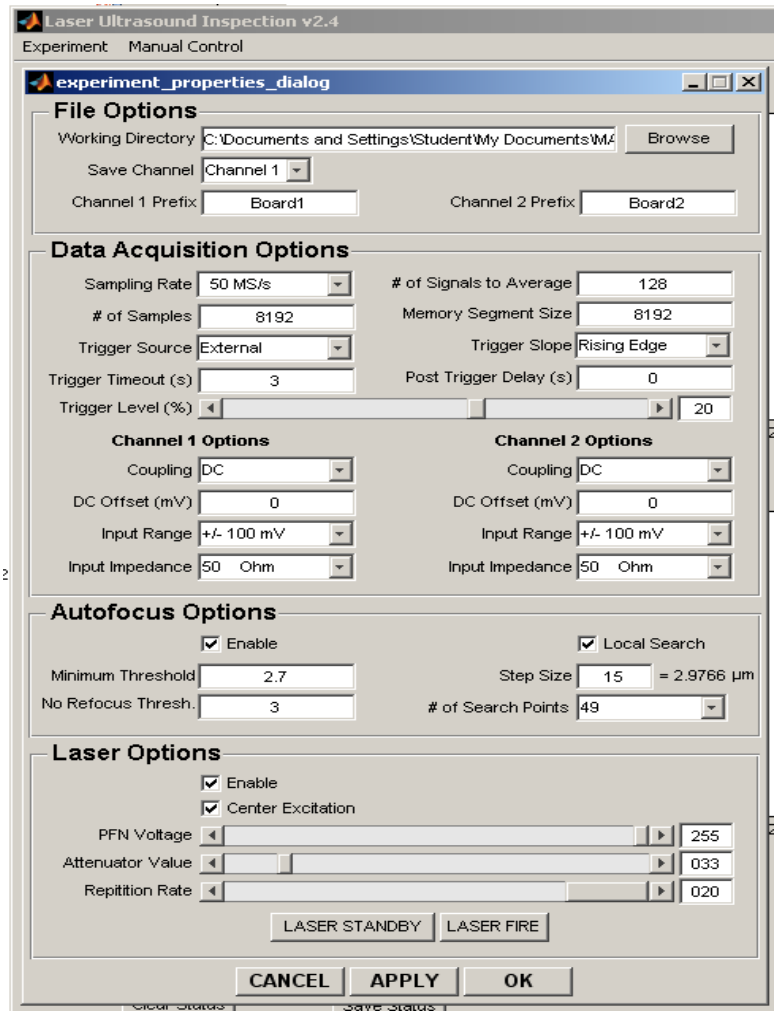


Figure 3-22: Sub-menu of Properties

After the configuration of these experimental parameters, the operator needs to click the Load Test Points sub-menu. This will automatically load the text file that is generated

during board alignment. As shown in Figure 3-23, the inspection and laser excitation points are extracted from the text file.

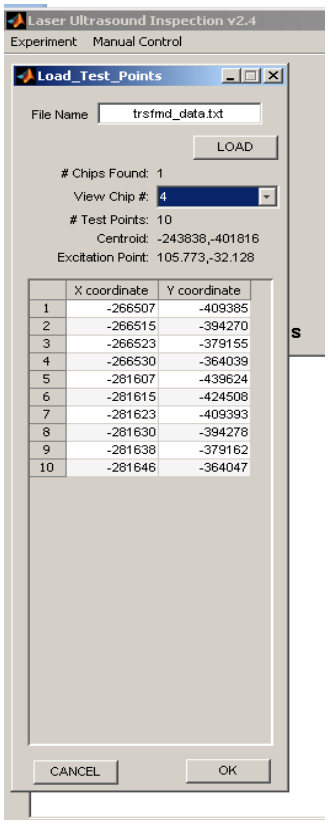


Figure 3-23: Screenshot of Load Test Points

After loading test points, the operator clicks the Run sub-menu, and the inspection process starts by following the created 'recipe'. The X-Y positioning table and pulsed laser are then driven automatically or manually to the desired positions, separately following the 'recipe', and they complete the whole inspection process. During inspection, the operator can monitor the real-time inspection status based on the waveform plotting window and the Inspection Status window. The waveform plotting window as shown in the right of the front panel of the GUI (Figure 3-19) plots the signal of the current inspection point. The

Inspection Status, as shown in Figure 3-24, will display the current inspection point on the current inspection point. Meanwhile, the results from the autofocus system are also displayed and updated in real-time.

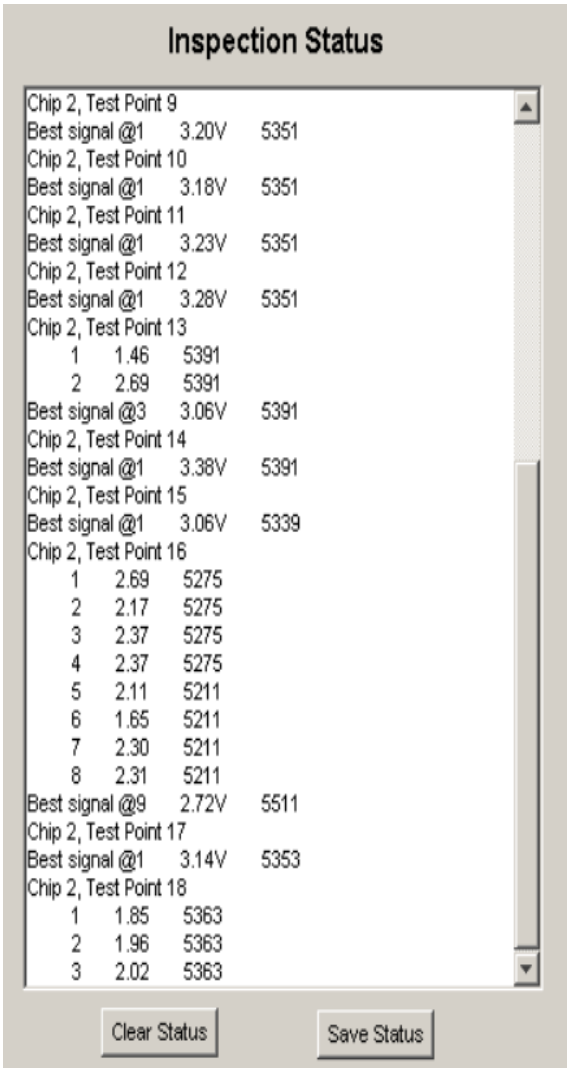


Figure 3-24: Screenshot of Inspection Status

In addition, the inspection can be stopped at any time during inspection by clicking the Emergency Stop button on the GUI.

Before the GUI was developed, the operator needed to switch between various control

interfaces to access each sub-system, such as stage motion, data acquisition and laser. With the newly developed GUI, the different sub-systems are integrated into a single interface. The system performance is greatly improved by increased user-friendliness, higher throughputs and better repeatability.

3.4 System Throughput

Since one of the research objectives is to deploy this inspection system on an assembly line for on-line inspection, system throughput is an important concern. The total test time equals the board alignment time plus the inspection time.

As shown in the following equation, the total test time for one chip equals the board alignment time plus the inspection time. The board alignment time usually takes about 2 minutes.

*Total test time = board alignment time + number of inspection points * (time for stage movement + time for autofocusing and local searching + data acquisition time)*

The time per inspection point includes the time for stage movement, autofocusing and data acquisition. The time for stage movement is very short, less than 0.5 seconds. The time for autofocusing depends significantly on the surface roughness of the test sample. The

surface of a flip chip package is usually the bare silicon, which produces a smooth surface and benefits the reflection of laser light back to the interferometer. During the inspection of a chip with a smooth surface such as a flip chip, there is almost no need for the autofocusing system and time for autofocusing and local searching is negligible. However, if a chip has a rough surface, such as a PBGA package with a mold compound surface, some efforts are required for the autofocusing system and local search system to obtain the desired signal intensity level. An average of 15 seconds is usually needed under this circumstance.

After each laser pulse is fired, the transient out-of-plane displacement responses are picked up by the laser interferometer. The transient responses die out completely before the next laser pulse. Therefore, the time for data acquisition is obtained by dividing the number of signals to be averaged with the laser repetition rate (in Hz).

The number of signals to be averaged depends on the signal intensity level. If the signal intensity level is very good, a small number of signals is enough to improve SNR after being averaged. However, a large number of signals must be averaged for SNR enhancement during the inspection of PBGA packages. A higher laser repetition rate also improves the inspection speed. The laser repetition rate is set at the upper limit of the current Nd:YAG laser, i.e. 20Hz.

Therefore, faster stage, smoother surface finish, smaller number of signals to be averaged and higher laser repetition rate will improve the system throughput. Among all

the factors, increasing laser repetition rate is the most efficient method. A 100Hz laser can run 5 times faster than the current 20Hz laser.

3.5 System Resolution

The system resolution has not been fully characterized since it varies from test vehicle to test vehicle. For example, the inspection resolution depends on the types of test vehicles. Resolution from inspecting from flip chip packages should be better that that obtained from BGA packages due to higher SNR. What's more, the system resolution depends on the types of solder joint defects. For example, the system resolution cannot be the same for inspecting the solder joint cracks and solder joint bridging. So far, this system has been used to successfully detect the presence of a micro-crack of 100 microns on a flip chip package.

Chapter 4 DEVELOPMENT OF HYBRID REFERENCE METHOD

4.1 Motivation

The principle underlying this system's evaluation of package quality is the quantification of the differences in transient out-of-plane displacement responses between the devices to be tested and that of a known good device. In order to quantify the response differences, a number of signal-processing methods, both in the time domain and the frequency domain, have been implemented. Liu [41] used Periodogram averaging to analyze the signal power density distribution in the frequency domain. A frequency shift between the reference signal from a good sample and the signal measured from a defective sample was observed as well. However, the frequency changes caused by solder ball defects are very subtle, and are usually below the frequency resolution on the spectrum. Liu [41] also proposed the error ratio (ER) method to compare signals directly in the time domain. This method integrates the squared error between the measured and referenced signals and then normalizes this integrated value by the total energy of the reference signal, as represented by Equation 2.1, where *f(t)* is the measured signal and *r(t)* is the reference signal. As the defect becomes severe, the ER value gets larger. Then Zhang [42] proposed the Modified Correlation Coefficient (MCC) method to analyze the time domain signals in

a statistical way. The MCC is a normalized measure of the strength of the linear relationship between signals, and each measure results in a number between 0 and 1, which represent exact-correlation and no-correlation, respectively. Compared to the ER method, the MCC method is a better choice. First of all, this is because the MCC is immune to laser power fluctuation, while the signal magnitude fluctuation brought by laser power fluctuation can lead to distorted ER values. In addition, the scale of the ER depends on the device being tested and should only be used for relative comparisons between similar product types. This limitation makes it difficult to set up a universal threshold of ER to separate defective samples from good samples.

FFT-based power spectrum analysis, Error Ratio and MCC methods all use raw transient responses from the entire frequency range to extract and quantify the differences between different signals. However, defect features are more prominent in specific frequency ranges rather than being evenly spread across the whole frequency range. The data analysis in the whole frequency range might obscure the frequency components that are most sensitive to the defects.

To extract more useful information from raw signals and to improve inspection sensitivity, Yang [43, 44] developed the wavelet analysis and the local temporal coherence (LTC) analysis methods. The wavelet analysis and the local temporal coherence (LTC) analysis methods did improve the inspection sensitivity. Yang [43, 44] was able to get larger MCC values after the signals were processed by both methods. However, all of

these signal processing methods require a known-good reference chip for comparison, which typically involves expensive testing using alternate non-destructive methods. In addition, using a single known-good chip totally ignores the manufacturing variations, which may introduce statistical insignificance. This drawback largely limits the application of this inspection system. Therefore, it would be very helpful to develop a signal processing method that does not require a pre-established known-good reference chip. In this chapter, a Hybrid Reference Method is proposed to overcome this limitation.

4.2 Hybrid Reference Method

The proposed Hybrid Reference Method (HRM) aims to provide a means to analyze the inspection data without requiring a pre-established known-good reference chip. This approach assumes that the signal correlation among defect-free devices is better than the signal correlation among defective devices. Therefore, the differences in vibration response caused by manufacturing variations must be smaller than the differences in vibration response caused by defects or quality degradation. Another necessary assumption is that good devices have to be present in the sample set. In addition to the aforementioned assumptions, it is important to note that the efficiency of this method is influenced by the sample set size. A larger sample size will produce a more representative hybrid reference.

The first step of this approach is to correlate each of the inspected chips to each other

using the Modified Correlation Coefficient (MCC) method as shown in Equation 2.2. Each correlation result is a number between 0 and 1, which represent exact-correlation and no-correlation respectively. The results of all such correlations are assembled into a 3-D matrix that contains all the cross-correlations between chips in a set of inspected chips. The *(i,j,n)*th element in this matrix contains the MCC value for Chip *i* and Chip *j* at inspection point n. Each slice of the 3D matrix is a 2D matrix that contains the cross-correlation results at each inspection point. In addition, this 2D matrix is symmetric and contains zeros along the diagonal.

Then the mean for each column of the 2D matrix is obtained to form a vector *S*. *S* is a vector whose size equals the total number of samples, and each element is associated with one chip in the sample set. The value of the element reveals the level of the signal similarity between one chip and the rest of the sample pool at a specific inspection point. Figure 4-1 illustrates the overall process visually.

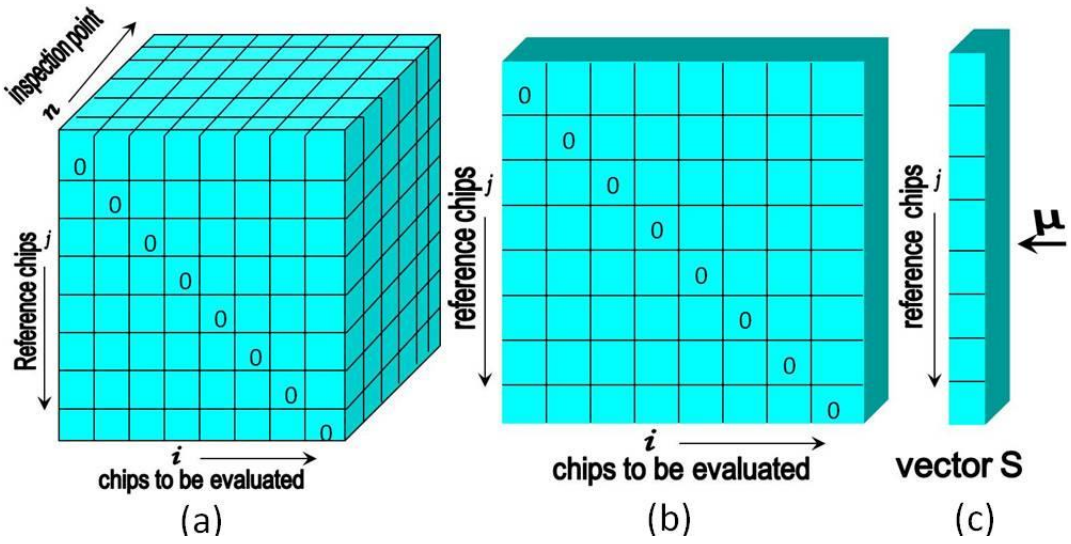


Figure 4-1: (a) 3D cross-correlation matrix, (b) 2D cross-correlation matrix for a specific inspection point, and (c) vector S for a specific inspection point

To select the chips that have the most similar signals at a specific inspection point, a selection threshold is constructed based on Equation 3.1 and then applied to the vector *S*. The chips with element values below the threshold are the chips that are selected as the most similar chips at this specific inspection point. The value of the selection coefficient, *C*, must be determined uniquely for each package type to compensate for manufacturing variations, and also to guarantee that enough chips are selected at each inspection point.

$$\text{selection } threshold = \mu + C\sigma \tag{3.1}$$

$$where \begin{cases} \mu \text{ is the mean of vector } S \\ \sigma \text{ is the standard deviation of vector } S \\ C \text{ is the selection coefficient to determine selection threshold} \end{cases}$$

Finally, the time domain signals from these selected samples are averaged at this specific inspection point to form hybrid reference signals at this specific inspection point.

The arithmetic average is used because of the characteristics of the arithmetic mean. At each inspection point, the signal received by the sensor, y_i can be modeled as $y_i = y + \epsilon_i$, where i is the index of chips, and ϵ_i, is the measurement error that follows a normal distribution with zero mean and standard deviation of σ. Constructing a virtual reference is the same as finding the best estimator of 'y', the true signal. In statistics, it's been proven that the arithmetic mean is a minimum-variance unbiased estimator, i.e. its mean square error (MSE) is least, since MSE equals the summation of the square of bias and variance. A series of hybrid reference signals at all the inspection points will be produced and they together constitute a Virtual Reference Chip. This Virtual Reference Chip serves as a pre-established known-good reference chip. What's more, it is a much better choice because the use of an actual known-good reference chip ignores manufacturing variations, which may lead to biased MCC results.

4.3 Application of Hybrid Reference Method

Two types of FCOB package, FC48 and FC317 were used as test vehicles to develop this method. The test vehicle specifications are tabulated in Table 4-1. As shown in the table, the solder material in all the test vehicles is lead-free because the microelectronic industry is migrating toward the environmentally friendly lead-free solder. No prior information about the quality of the test vehicles was provided, which is usually the case in

on-line inspection.

Table 4-1: Test vehicle specifications for development of HRM

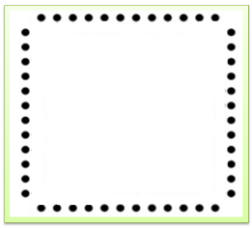
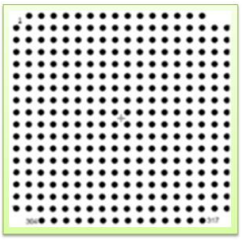
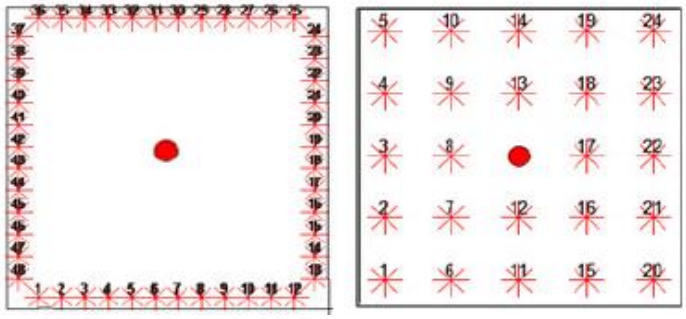
Device name	FC48	FC317
Device type	FCOB	FCOB
I/O count	48	317
Package size	6.35mm x 6.35mm	5.08mm x 5.08mm
Bump layout		
Bump diameter	190μm	135μm
Bump height	140μm	119μm
Bump pitch	457μm	254μm
Solder material	Lead-free	Lead-free
Substrate	FR4	FR4
Underfill	No	No

Figure 4-2 shows the inspection patterns for both types of test vehicles. In the figure, the laser excitation point is denoted as a solid red circle that is positioned at the center of the chip surface. As shown in Figure 4-2, FC48 has 48 inspection points which are located just above its solder bumps, and FC317 has 24 inspection points which covers the surface. The inspection points of FC48 are located on the right top of the solder bumps to directly

reflect the solder bump quality. As for FC317, an ideal inspection pattern will cover each individual inspection point. However, when time cost is also taken into account for the design of the inspection patterns, a 24-inspection-point pattern covering the entire chip area was chosen rather than the 317 inspection point pattern for FC317. There were a total of 51 FC48 chips and 55 FC317 chips used in this investigation.



(a) (b)

Figure 4-2: Test patterns for (a) FC48 and (b) FC317

After the LUI signals at all the inspection points from all the chips were recorded and cross-correlated using MCC, the 3-D matrix and the vector *S* were obtained for each type of test vehicle. Then the most similar chips were selected using Equation 3.1. In the case of the FC48 test vehicle, -0.5 was empirically chosen as the optimum value for selection coefficient C in Eq. 3.1 after several trials while -0.3 was chosen for FC317 test vehicle. At each specific inspection point, the chips with element values below the threshold are selected as the most similar chips. Therefore, different inspection points can have different combinations of selected chips to form the virtual reference signal.

Figure 4-3~Figure 4-6 demonstrate the processes of the Hybrid Reference Method on

the FC48 test vehicles at inspection point #1. Figure 4-6 shows all the time domain signals obtained at inspection point #1 for all the FC48 chips. As shown in the figure, it is extremely difficult to visually determine which chips have the most similar signals. Figure 4-4 shows the selection results for vector S of at inspection point #1 where the yellow horizontal line represents the selection threshold. There are 21 chips with values below the selection threshold, and they are selected as the most similar chips at inspection point #1. The time domain signals of the selected chips are plotted in Figure 4-5. As shown in the figure, the signals are fairly similar to each other. In addition, the variations of these selected signals represent the manufacturing variations. By averaging these selected signals, the virtual reference signal at inspection point #1 is generated, as shown in Figure 4-6. This process is repeated for other inspection points until the hybrid reference signals are produced for all the inspection points.

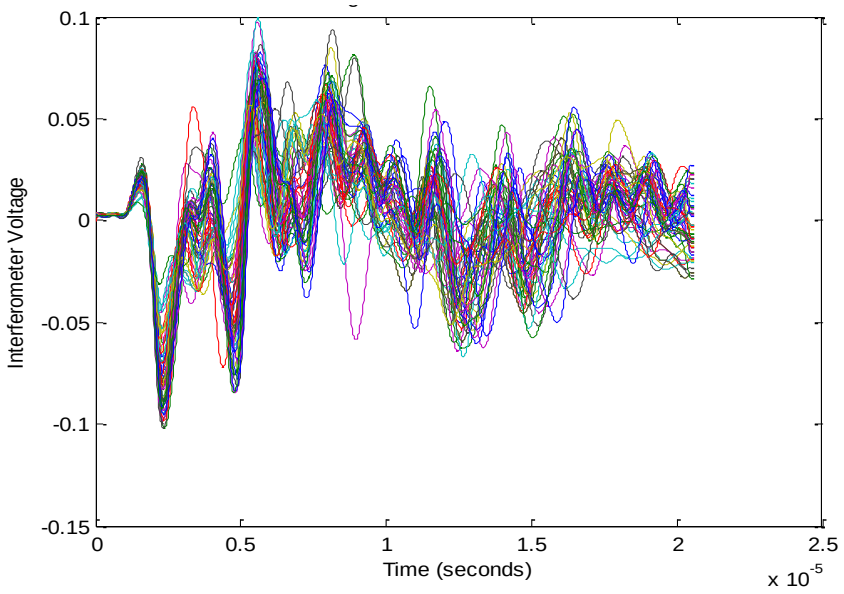


Figure 4-3: Time domain signals of all FC48 chips at inspection point #1

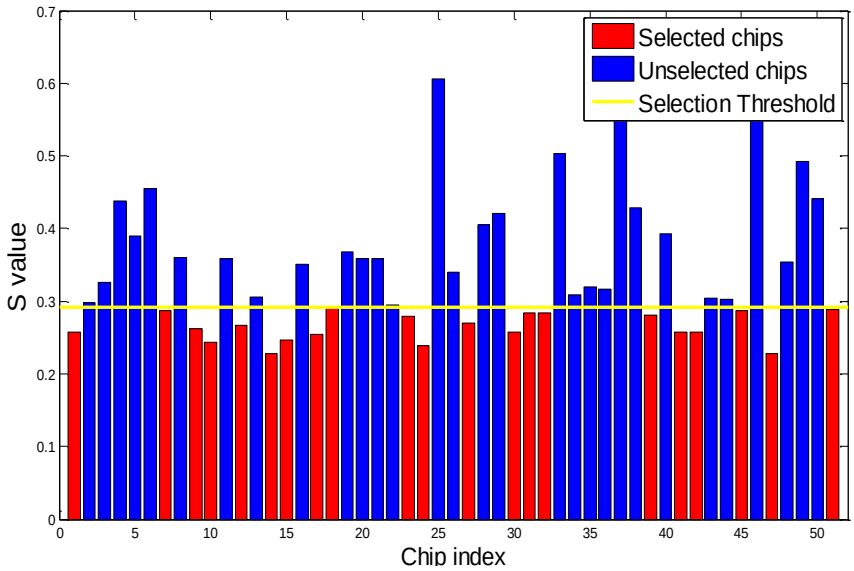


Figure 4-4: Selection result of FC48 chips at inspection point #1

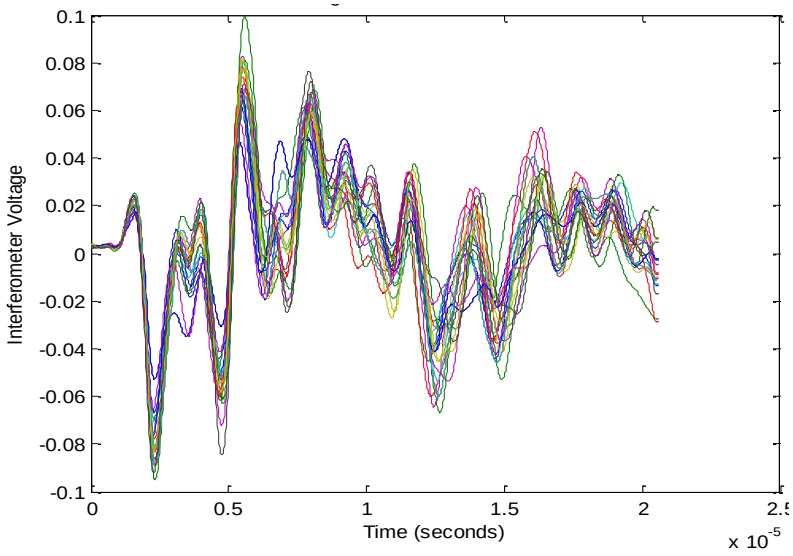


Figure 4-5: Signals of selected FC48 chips at inspection point #1

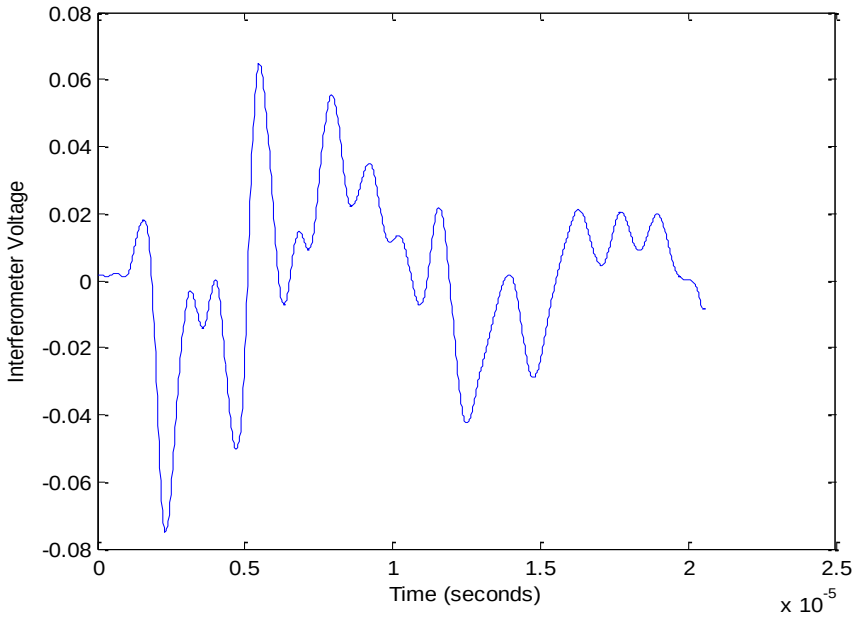


Figure 4-6: Hybrid signal at inspection point #1

4.4 Chapter Summary

In summary, with the implementation of the Hybrid Reference Method, the costs associated with extensive and expensive testing to finding a known-good chip can be significantly reduced. Furthermore, the use of the virtual hybrid reference instead of a single known-good chip reduces the influence of manufacturing variations by averaging signals from the most similar chips. The Hybrid Reference Method makes this inspection system more robust and productive. With the implementation of the Hybrid Reference Method, this inspection system can be used in assembly lines for high volume inspection of electronic components. The virtual hybrid signals can be configured to be updated on the fly as more and more similar chips under inspection are selected and added into the pool.

Last but not least, even though this method is developed using flip chip packages, it can be applied to any type of package, which truly opens the windows for this inspection system.

Chapter 5 INSPECTION OF PROCESS-INDUCED SOLDER BALL QUALITY IN BGA PACKAGES

Previous application examples for this inspection system include flip chips, chip scale packages (CSPs), land grid array (LGA) and multilayer ceramic capacitors (MLCCs). BGA packages have not yet been investigated by using the LUI system even though BGA packages have a large market share in the microelectronic industry. There are several challenges in the inspection of BGA packages. First, the surface of a BGA package is usually encapsulated with a molding compound to protect the chip, as shown in Figure 2-5. Molding compounds are one type of polymer with a rough surface. The rough surface will scatter the laser light from the interferometer. Therefore, the amount of laser light returning to the interferometer is reduced because of scattering. This introduces a lot of random noise into the signals that are output from the interferometer. In addition, the laser-induced ultrasound signals are much attenuated because of the presence of the molding compound. This usually leads to a small SNR. As for flip chips and chip scale packages (CSPs) test vehicle, their surface is made of silicon with a very smooth surface. A strong signal can be easily obtained. What's more, BGA packages usually have a relatively large dimensions and weights, which make it difficult to excite them by a laser pulse. Therefore, high laser power is required to generate a relatively large response from BGA packages.

Figure 5-1 shows the comparison of a typical signal obtained by the LUI system from a flip chip package and a PBGA package. Both signals have the same number of averages. And the distances between the inspection point and the laser excitation point are the same. As shown in the figure, the signal from the PBGA package has smaller amplitude than that of the flip chip package. Moreover, the signal from the flip chip package is more smooth, which implies less noise. In other words, the signals from BGA often come with poor SNR.

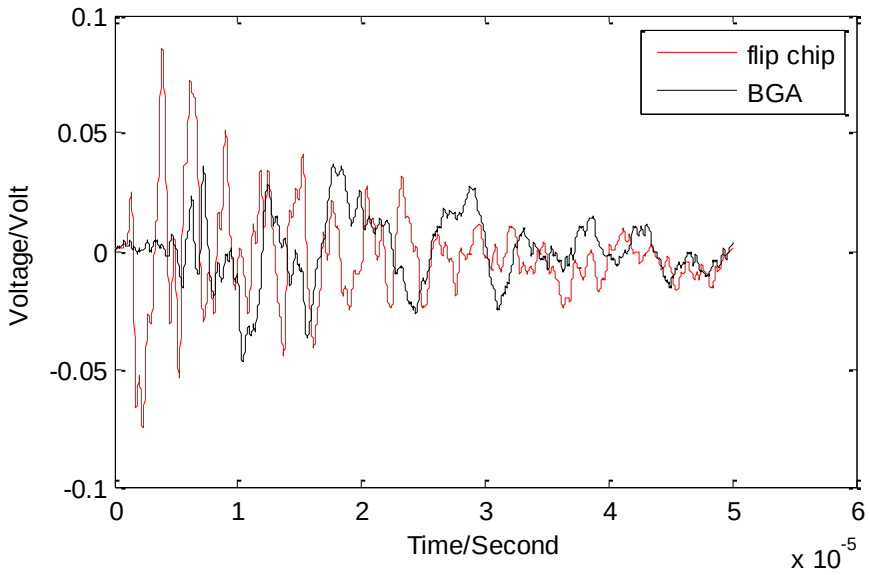


Figure 5-1: Comparison of a typical signal from a flip chip package and a PBGA package

To improve the SNR of signals from BGA packages, the auto focus system is designed to maximize the amount of laser light returning to the interferometer by adjusting the distance between the sample surface and the interferometer lens.

As mentioned earlier, the solder joint interconnect is one of the most vulnerable parts

in an electronic product, and it can be subject to a number of quality and reliability issues. Based on when the defects are introduced, the defects can be classified into two categories: process-induced defects and service-induced defects. As the name implies, process-induced defects refer to defects introduced during assembly. Common process-induced solder ball defects include cracked, head-in-pillow (HIP), open, poor-wetting, starved, misaligned, missing, and voids. In this chapter, two types of process-induced defects are investigated on BGA packages, including poor-wetting and void. The LUI system will be used to study both types of process-induced issues. Other solder ball evaluation methods including X-Ray, SAM, electrical testing and cross-sectioning will also be carried out for comparison.

5.1 Introduction to Poor Wetting

Generally speaking, poor wetting refers to non-wetting and dewetting. Non-wetting is the condition wherein the solder coating has contacted the surface but did not adhere completely to it, causing the surface or a part thereof to be exposed. Dewetting is the condition wherein the solder recedes after the surface is coated, creating irregular mounds of solder, but leaving behind no exposed areas [51]. Even though some poor wetted solder balls can still pass the continuity test, they will decrease the interfacial strength of the interconnection thus reducing the service life of the end-products. Meilunas et al. [52]

reported early separation between solder alloy and the component attachment pad in the accelerated thermal cycling because of poor wetting. The worst situation of poor wetting leads to completely open circuitry [53]. If the poor wetting can be detected as early as possible in the manufacturing line, the quality and reliability of such a package can be improved through rework.

Common causes of poor wetting include: (1) poor wettability of metallization, (2) poor solder alloy quality, (3) poor solder paste quality, (4) poor flux activity, and (5) improper reflow profile/atmosphere. Poor wettability of metallization can be due to impurity or tarnishes or to the nature of the metallization of pads or solder joints. Bradley and Banerji [54] have investigated the effect of PCB finish on the wettability of BGA packages. Chunho and Baldwin [53] have developed a yield model that provides the relationships of the interconnect wettability to the statistical variations of the design parameters such as solder ball size, pad size and substrate warpage. Li et al. [55] have found that excessive underfill material acts as a barrier preventing the solder balls from wetting during the second level assembly. Lai et al. [56] have studied how the solder materials affect the growth of the intermetallic compound (IMC) layer. Time, temperature and reflow atmosphere also have great influence on wetting performance. Insufficient heat input, due to either too short a time or too low a temperature, will result in an incomplete fluxing reaction as well as incomplete metallurgical wetting and accordingly will result in poor wetting [51]. Lead-free materials usually have a higher

melting temperature range than the SnPb solder [57]; thus more heat input is required to avoid the poor wetting issue. On the other hand, an excessive heat input prior to solder melting will not only oxidize the metallization of pads and leads excessively, but will also burn off more fluxes [1]. Guo et al. [58] and Li et al. [59] have carried out research on the effects of reflow on wettability in lead-free solders.

5.2 Introduction to Solder Ball Void

Voids are defined as cavities formed in solder joints, and are common in all surface mount applications. These can be divided into the following categories: macro voids, planar micro voids, shrinkage voids, pin-hole voids, and Kirkendall voids [60]. Macro voids, which are the focus of this study, refer to large preexisting voids that are created during the manufacturing process [61]. A macro void is usually negligible at the solder ball and BGA component stage, and it is introduced mainly by the entrapped gas bubbles during the reflow process.

Various factors can contribute to void formation. Some of these factors are related to the material issues like surface finish on the substrate [62], solder ball alloy [63], solder paste type and flux volatilization, while others are dependent on process parameters in the assembly process, circuit board contamination or human factors, like reflow profile and reflow atmosphere [64]. For example, moisture in the component or printed circuit board

(PCB) will contribute to outgassing which increases void formation. Lead-free solder has a higher melting temperature range than SnPb solder [57], and this elevated melting temperature of lead-free alloys releases more volatile compounds from the substrate and the components, which means that more gasses are likely to be trapped in lead-free solder balls. Meanwhile, lead-free solders have higher surface tensions than SnPb equivalents, which may also result in increased solvent retention [65, 66]. As lead-free solder has become dominant, void in lead-free solder is now getting more attention.

How void affects the reliability of the solder joint is a controversial issue. On the one hand, a void is considered to be a stress concentrator. Its presence is expected to affect the mechanical properties of solder joints, and reduce the strength, ductility, creep and fatigue life [51]. It also interrupts heat dissipation hence producing spot overheating [67]. Furthermore, it has been observed that the resistance of the solder joint will increase with the occurrence of large (or numerous) voids as the cross sectional area of the solder joint is considerably reduced [68]. Additionally, the formation of voids causes localized nonhomogeneity of current density, which aggravates electromigration (EM) effects and may lead to an electromigration-related failure [69, 70].

On the other hand, voids may act as crack arrestors, stopping the propagation of a crack and requiring additional energy to reinitiate a continuous crack through the remainder of the joint [64]. Several researchers have investigated the reliability of solder joint with voids [71-78]. It has been difficult to study the effect of voids on the reliability

of solder joint, as this has been an uncontrolled factor in the assembly process, and it is difficult to isolate the effect of voids on the reliability of solder joints. Numerous studies have been conducted in the past to study the effect of voids, but most of the results have been contradictory, with some showing a positive effect, while others showed a negative effect on the reliability of the solder joint [68]. Despite this uncertainty, the consensus is that the size and the location of voids are the most important factors in determining the effect of voids on the performance and reliability of solder joints. As for the size, voiding is acceptable at low contents, while excessive voiding affects mechanical properties, decreasing the strength, ductility and fatigue life of the interconnections. In terms of location, voids located at the interface of the solder ball and the substrate are more likely to be a reliability hazard than voids in the bulk/interior of the solder ball [68, 78].

The Institute for Printed Circuits (IPC) has developed standards for screening voided solders based on size and location. Based on 2-D X-ray images, the IPC-7095 standard specifies three categories for void size for BGA solder joints. These categories are based on the percentage of the solder ball cross sectional area occupied by the voided area. In the case of multiple voids in the same solder joint, the standard suggests adding all the voids together and using this as the total void percent area [79]. Table 5-1 shows the voids classification according to this standard [74]. This standard does not specify a category for voids larger than 36% and assumes that this is beyond acceptable limits of

most products. Class III products offer the highest reliability with the smallest allowable void area, and are usually used in aerospace and defense.

Table 5-1: Void classification from IPC-7905

Location of Void	Class I	Class II	Class III
Void in bulk of solder	20.25% - 36% of Area	9% - 20.25% of Area	0 - 9% of Area
Void at interface of solder	12.25% - 25% of Area	4% - 12.25% of Area	0 - 4% of Area

2-D X-ray is the most widely used non-destructive technique for void evaluation. Void in the solder ball cause material density differences, which are reflected by a light color on the X-ray image. Figure 5-2 is a 2D X-Ray image showing solder ball voids as the white spots, and the sizes of white spots represent the void sizes. Now some modern X-ray inspection tools have built-in image-processing software that can automatically measure the size of voids in the solder balls. However, it is difficult to determine whether the voids are at the interface between the substrate and the solder ball or at the interface between the ball and the PCB, or internal to the ball. Moreover, 2-D X-ray techniques have problems inspecting solder balls in the presence of interference. The interference may be caused by multiple-layer components, overshadowed balls, the presence of via or traces on the substrate. As more complex packages, such as 3-D packages [80], emerge in

the market, this problem will limit the application scope of the 2-D X-ray tool. Now some researchers have initiated a robust void detection algorithm [81] to solve this problem.

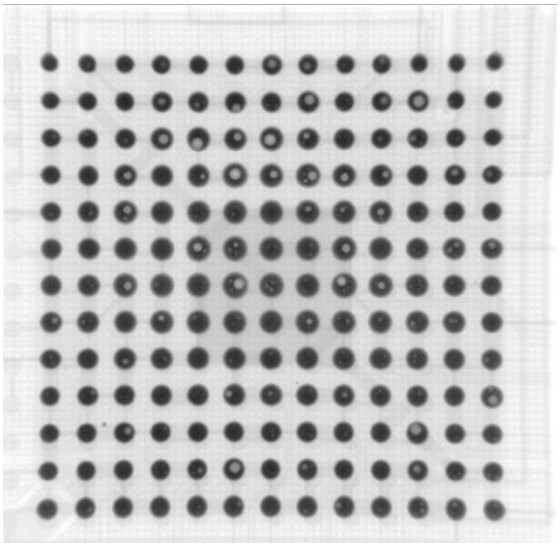


Figure 5-2: X-Ray image showing solder balls with voids

5.3 Test Vehicle Fabrication

As shown in Figure 5-3, two types of daisy chained PBGA packages, BGA225 (with 5 daisy chains) and BGA169 (with 7 daisy chains), assembled on the same PCB were used in this investigation. They went through the regular BGA reflow process, i.e. solder paste printing, chip placement and reflow. Type IV solder paste is used during solder paste printing. A standard lead-free BGA reflow profile was used for building the defect-free chip, as shown in Figure 5-4. The length of time during which the solder is heated to above the solder melting temperature (217°C for SAC305 lead-free solder) is referred to "time above liquidus" (TAL). The maximum reflow temperature (peak temperature) is achieved during the TAL [82]. A total of 11 defect-free PCBAs (Printed

Circuit Board Assembly) were fabricated, which includes 22 BGA225 chips and 22 BGA169 chips.

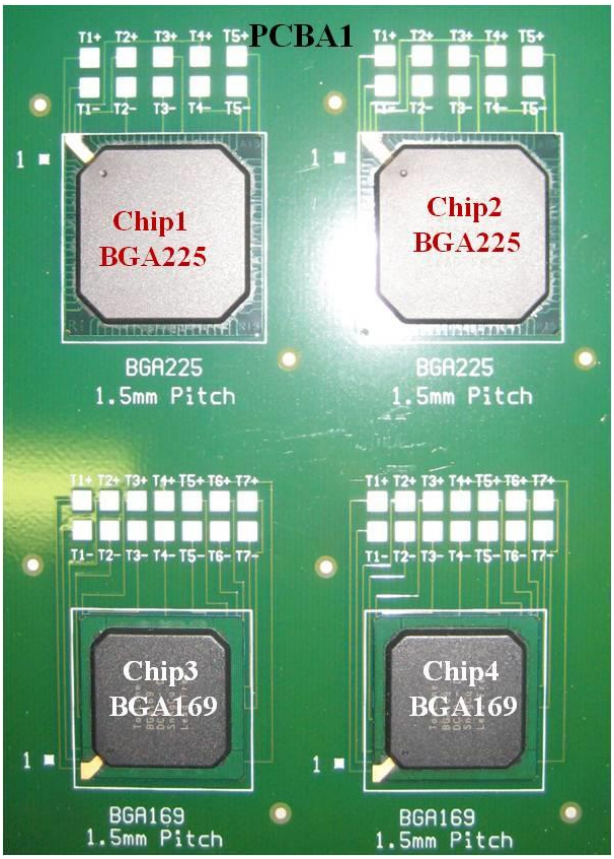


Figure 5-3: Test Vehicle

A modified reflow profile was used to intentionally create solder balls with poor wetting issues, as shown in Figure 5-4. Comparing the standard and modified reflow profiles, there is no difference during the soak/preheat zone. However, the peak temperature in the standard reflow profile is 240°C while the peak temperature of the modified profile is 225°C as shown in solid line in Figure 5-4. Furthermore, the TAL lasts over 70 seconds in the standard profile, while it is only 30 seconds in the modified

profile. Therefore, the solder may not totally melt and collapse. The integrity of the interfacial bonding can be jeopardized under the modified reflow profile. Lall et al. [83] found that improper reflow due to low peak temperature and less TAL resulted in solder joints with poor wetting in package-on-package (PoP). One PCBA, including 2 BGA225 and 2 BGA169 chips was built under modified reflow profile.

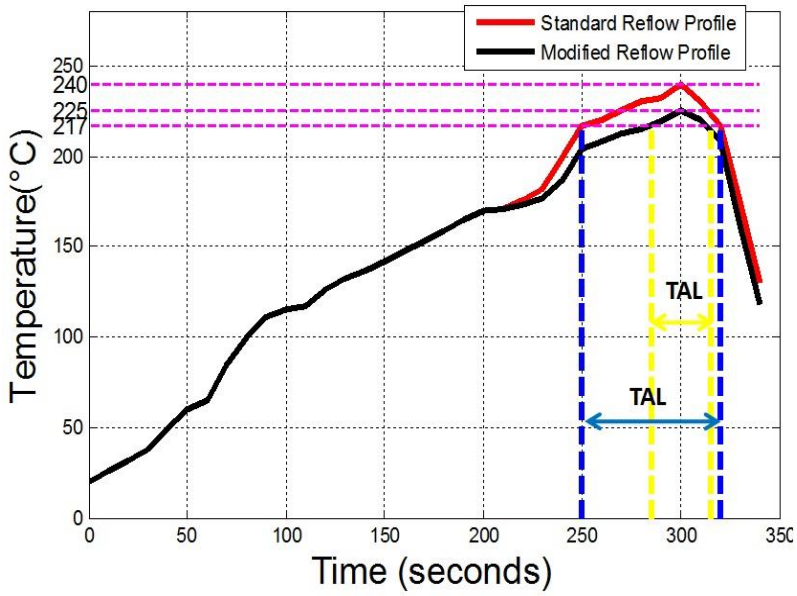


Figure 5-4: Standard and modified lead-free BGA reflow profiles

The standard BGA reflow process does not need any additional flux dip, as the solder paste itself contains the flux. However, to intentionally create voids in the solder joints, additional flux was added by dipping the BGA to a flux reservoir before chip placement, because flux volatilization in solder paste was reported as the single largest source of gases that form voids in solder joint [64]. Specifically, a no clean tacky flux was utilized. Two BGA225 and Two BGA169 chips from one PCBA were dipped into

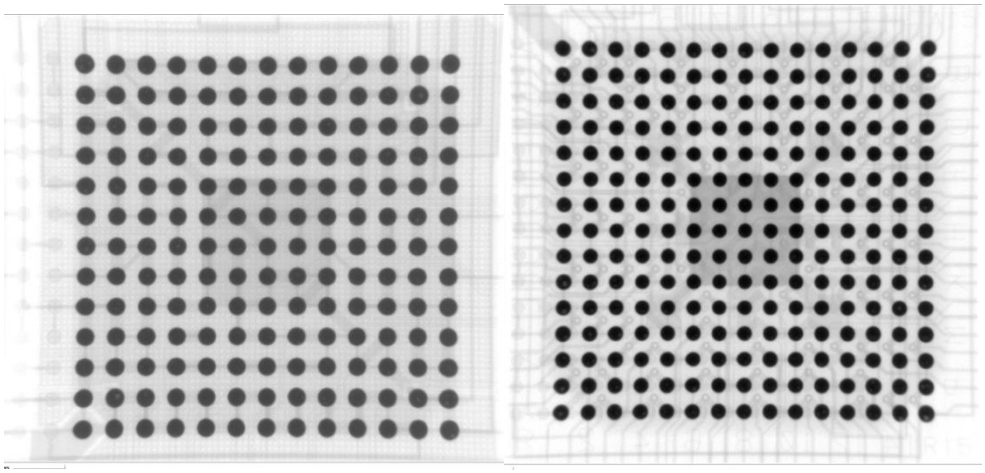
flux. By controlling the volume of flux dip, two different levels of voids were proposed: relatively low and relatively high. The names of all the BGA packages used in this study are listed in Table 5-2. These names will be used in the following analysis.

Table 5-2: Summary for BGA test vehicles

Chip Type	**Chip Conditions**			
	Defect-free and void-free	Poor wetting	Void	
			Low level	High level
BGA225	PCB1Chip1~PCB11Chip2	PCB12Chip1~PCB12Chip2	PCB13Chip1	PCB13Chip2
BGA169	PCB1Chip3~PCB11Chip4	PCB12Chip3~PCB12Chip4	PCB13Chip3	PCB13Chip4

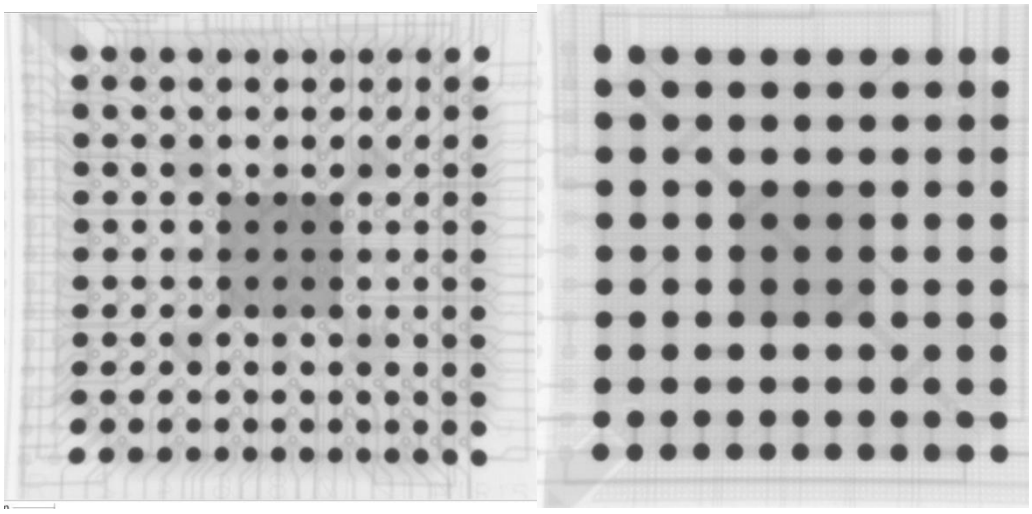
To check the proposed quality conditions of the test vehicles built, all the test vehicles were first inspected using the continuity test after reflow. In the continuity test, all the daisy chains in all the chips on PCB1~PCB11 passed the continuity test. At the same time, none of the daisy chains in the chips on PCB13 failed, which was an indication that the solder ball voids, if present, were not too severe to induce a resistance change. As for PCB12, 1 out of 5 daisy chains in Chip1BGA225 failed the electrical test while 2 out of 5 daisy chains in PCB12Chip2BGA225 failed. No daisy chains failed in PCB12Chip1BGA169 while 2 out of 7 daisy chains failed in PCB12Chip2BGA169. Therefore, it could be confirmed that the poor-wetting was successfully created such that some daisy chains failed the continuity test. However, some daisy chains still passed the test even with the presence of the poor-wetting.

Then all the test vehicles went through the 2D X-ray test. Nothing abnormal like bridging and void could be found in the chips on PCB1~PCB11. Moreover, all the solder balls had smooth shapes and uniform sizes. Figure 5-5 shows a typical example of void-free BGA169 and BGA225 chip. The built-in image processing software in the X-ray tool also measured 0% void fractions for almost all the solder balls from chips on PCB1~PCB11. As for PCB12, X-ray images of PCB12Chip2BGA225 and PCB12Chip1BGA169 are shown in Figure 5-6. As mentioned in the results of the continuity test, both chips failed the continuity test. However, it is really difficult to find any obvious defects in the solder balls from these 2-D X-ray images. This also indicates that that 2-D X-ray technique has problems detecting interfacial defects, because interfacial defects are too small compared to the standoff height of the solder balls.



(a) (b)

Figure 5-5: 2-D X-RAY images for void-free chips: (a) BGA169, (b) BGA225

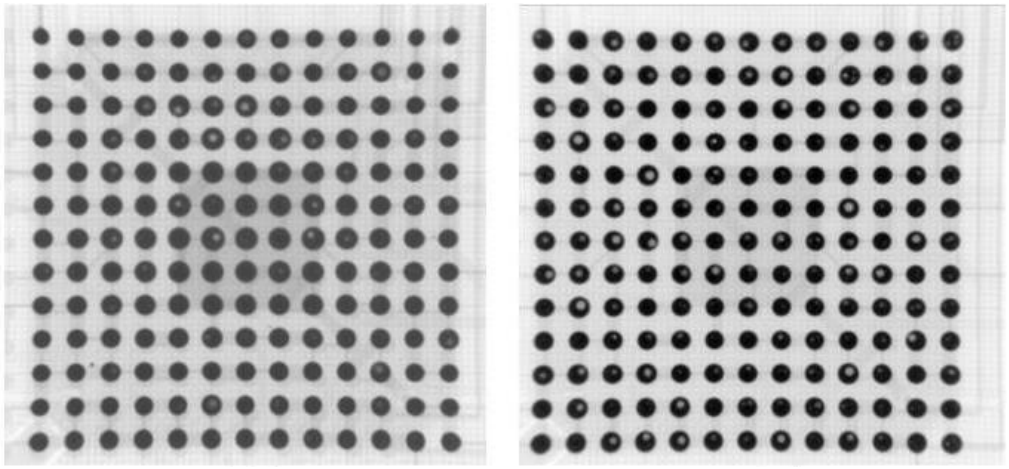


(a) (b)

Figure 5-6: 2-D X-RAY images: (a) PCB12Chip2BGA225, (b) PCB12Chip1BGA169

The 2-D X-ray images of PCBA13Chip1BGA169 (small void fraction) and PCBA13Chip2BGA169 (relatively large void fraction) are shown in Figure 5-7. As shown in the figure, the white spots located inside some solder balls are voids created by flux. There are solder balls with a single void and some with multiple voids at different locations. Moreover, PCBA13Chip2BGA169 have more solder balls with voids than PCBA13Chip1BGA169 according to the images. To quantify the solder ball voids, the built-in image processing software in the X-ray tool was used to measure the void size. Table 5-3 lists the results of void measurements for voided samples using the image processing software in the X-ray tool. As shown in Table 5-1, the void classification depends on the void size and void locations in the vertical direction, i.e. solder ball interfaces or bulk solder. However, the 2D X-ray tool is unable to give void locations in the vertical direction. Here, voids are assumed to be located at the solder ball interface,

which represents the worst case; therefore the percentage ranges from the third row of Table 5-1 are used for the void classification.



(a) (b)

Figure 5-7: 2-D X-RAY images for (a) PCBA13Chip1BGA169 (small void fraction), (b) PCBA1bChip2BGA169 (relatively large void fraction)

Table 5-3: Measurement results for BGA solder ball void

Chip	PCBA12Chip 1BGA225	PCBA12Chip 2BGA225	PCBA12Chi p1BGA169	PCBA12Chip 2BGA169
Total # of Balls	225	225	169	169
% of Balls W/Voids	51	87	54	92
% of Class I	1	2	2	6
% of Class II	5	23	14	55
% of Class III	45	62	38	31
% of Average Void Fraction	1.5	3.6	2	6.2
% of Standard Deviation of Void Fraction	2	3.1	3.1	4
% of Maximum Void Fraction	14	24	15	23

The following is a summary from the void measurement results:

1). On PCBA13, Chip2BGA225 and Chip2BGA169 have more solder balls with voids than Chip1BGA225 and Chip1BGA169, respectively. Plus, the average void fractions in Chip2BGA225 and Chip2BGA169 are larger than those of Chip1BGA225 and Chip1BGA169. Both suggest that two different levels of void fractions were successfully created by controlling the volumes of flux dip.

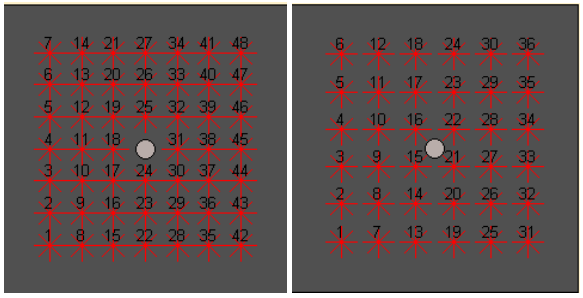
2). There are many variations and random factors during void formation. Even when a condition in a chip is conducive for solder balls to be induced with voids, some solder balls will be void free and others will have large voids (over 10%). Therefore, there are different void classifications of solder balls on a single chip. Compared to the mean of the void fraction, the standard deviation of the void fraction is fairly large, which shows the large variation of void sizes.

3). As shown in the table, most voids are the Class III type, and the average void fractions are very small. It is very difficult to build chips with large void fractions for all the solder balls, and this has also been reported by former investigators. Echeverria et al. [79] reported an average void fraction that is less than 3% in their assembly, and Wickham et al. [65] had an average void fraction smaller than 4% in their samples. Chips with relatively large void fractions were initially built for better comparison. However, as mentioned in the test vehicle preparation section, the concern was that some other defects besides voids, for example, insufficient bonding and poor solder shape profile, could be

induced by adding a large volume of flux dip,. These untended defects will distort the expected experimental results, and the effect of void will not be isolated. These new defects will also cause changes in the vibration responses of the chips, which will make it difficult to identify the root causes of the LUI signal change.

5.4 Construction of Hybrid Reference Signal and a Pass/fail Threshold

Figure 5-8 illustrates the inspection pattern for both test packages. The test locations are marked with asterisks. There are a total of 48 inspection points and 36 inspection points for BGA225 and BGA169, respectively. These inspection points are evenly distributed on the molding compound to match the area array of solder balls in both test packages. The laser source (denoted as a solid circle in the figure) is positioned at the center of chip surface in both inspection patterns.



(a) (b)

Figure 5-8: Inspection patterns for test packages: (a) BGA225 and (b) BGA169

All the defect-free chips, i.e. chips from PCB1~PCB11, were then selected as the most similar chips to produce the hybrid reference using the previously developed Hybrid Reference Method. Their signals at the same inspection point are averaged to form the hybrid reference signal for each inspection point. All these chips are selected is based on the results of the electrical test and the X-ray tests. First of all, they all passed the electrical test. Moreover, the X-ray test revealed uniformity and similarity among these chips. To further justify such selection, the LUI signals from all these 22 defect-free chips were cross-correlated with each other using the MCC method. The mean of all the MCC values in each correlation is extracted as a quality signature, which can be a flag to reflect the overall similarity between two chips. There are a total of 231 (C_{22}^{2}) quality signatures for each type of test vehicle. The histograms of all these quality signatures are plotted in Figure 5-9. The mean and standard deviation (STD) of all these quality signatures are also provided in the figure. As shown in the figure, all quality signatures are non-zero, which implies the presence of manufacture variance among defect-free chips. The mean and standard deviation (STD) of the cross-correlation results are very small, which indicates a good similarity among all the defect-free chips. Therefore, all 22 defect-free chips on PCB1~PCB11 are selected as the most similar chips to produce hybrid reference signals. Please be aware that this chip selection is different from the use case of flip chip packages in Chapter 4. In the case of flip chip packages, no prior information about the

quality was provided, however, the quality of these BGA chips is known based on the sample building process, and is confirmed by electrical tests and X-ray tests.

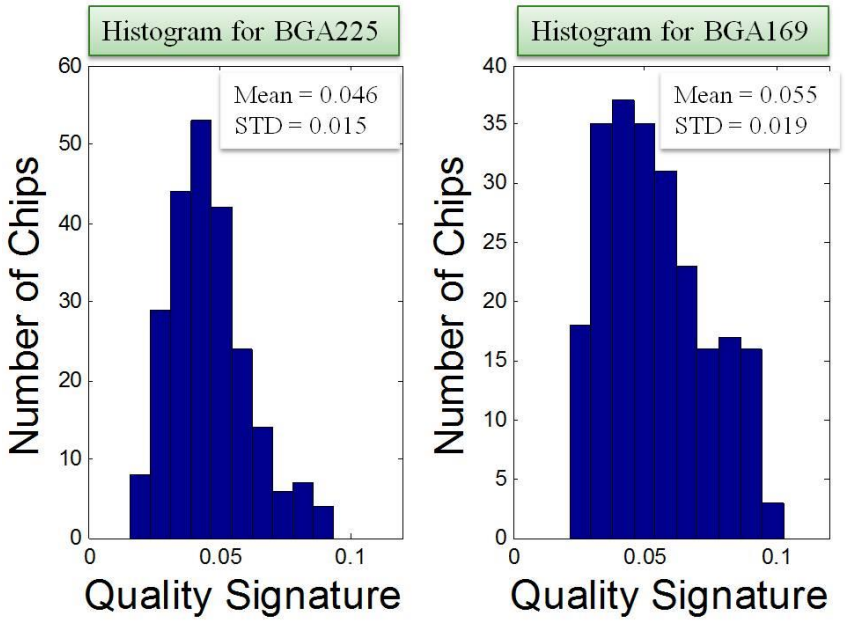


Figure 5-9: Histograms of quality signature for BGA225 and BGA169 cross-correlation

After the establishment of hybrid reference signals, the LUI responses from chips under test are correlated back to the hybrid reference signals using MCC at each individual inspection point. Now a specific pass/fail threshold must be constructed to flag the quality of the chip under test. Previously, no specific threshold was ever constructed. Failure was usually defined with an obvious increase in MCC. For example, Figure 5-10 [84] shows the MCC results for FC48 packages with increasing numbers of thermal cycling. As shown in the figure, at 0, 10 and 20 cycles, the MCC values are fairly stable and small. Starting from 30 cycles, the MCC values begin to pick up until 50 cycles with

a very obvious MCC increase at all the inspection points. Therefore, we would conclude that solder ball fatigue or failure is detected at 50 cycles. However, there are some limitations if a specific threshold is missing. First, it is impossible to tell the earliest detectable fatigue or failure. Second, it is difficult to apply such judgments in the manufacturing line owing to throughput requirement. Last, this judgment ignores testing variation. A statistically meaningful threshold is needed to accept or reject the chip under inspection. What's more, each inspection point should have its own threshold so that we can see clearly which inspection points are above the threshold and which are below. The location of the inspection points usually corresponds with the solder ball location. Therefore, the failure site can be identified based on which inspection points are above the threshold. Furthermore, signal characteristics like signal frequency and amplitude vary from inspection location to location. It is justified to have different thresholds at different inspection location. For example, it is reasonable to set a low threshold at an inspection location that is very sensitive to defects.

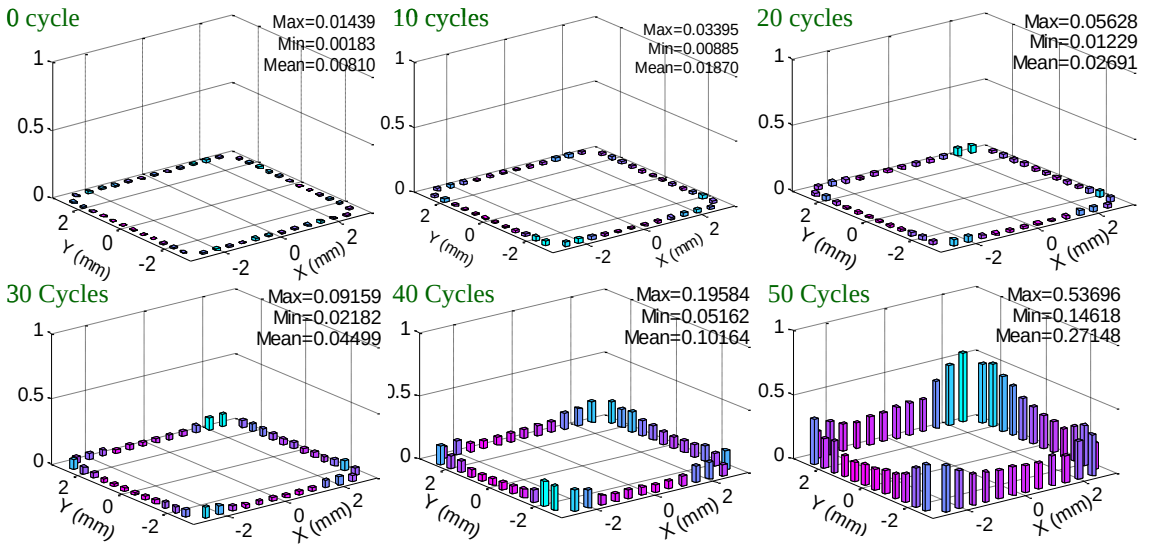


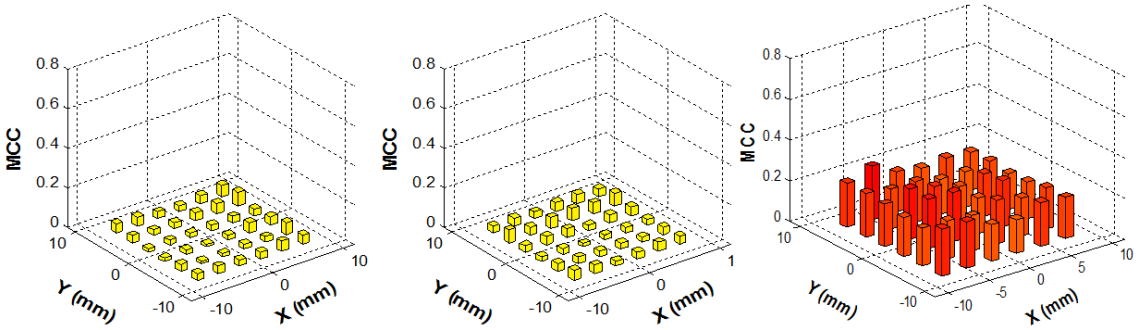
Figure 5-10: MCC values of 48 inspection points with thermal cyclings

At each inspection point, the mean (μ) and standard deviation (σ) of the cross-correlation results should be able to represent the distribution of the MCC values between any two good chips, since only the defect-free chips are used during cross-correlation. Let $Threshold = \mu + k\sigma$, then a proper k is determined based on Chebyshev's inequality. Chebyshev's inequality states that for any number, $k > 1$, at least $(1 - 1/k^2)$ of the population values lie within "plus or minus" k standard deviations, σ, of the mean value, μ. And Chebyshev's inequality can be applied to any type of probability distribution. For example, if $k = 3$, the threshold at each inspection point is determined by summing the mean and three times the standard deviation of the cross-correlation results. Based on Chebyshev's inequality, at least 89% of the MCC values between two good chips are below the threshold. Meanwhile, Type I error is 11% at the most, which suggests that the probability of a good chip being rejected is less than 11%. By

controlling k, we can have either a tight or loose quality control standard. Plus, the confidence and Type I error of the threshold is controllable by *k*.

5.5 LUI Inspection Results of Poor-wetting and Solder Ball Voids

Figure 5-11 shows the MCC results for BGA169, with the bar height representing the MCC value. Figure 5-11(a) and (b) are the MCC results from PCBA1Chip1BGA169 and PCBA1Chip2BGA169 correlating with the hybrid reference. Figure 5-11(c) shows the thresholds that are calculated using the aforementioned approach. $k = 4$ is chosen for BGA169 to generated the thresholds. Therefore, Type I error is 6% at most, which suggests that the probability that a good chip is rejected is less than 6%. As we can see, each inspection point has its own threshold because of its unique signal feature. It can be observed that the MCC values at all inspection points of both chips are below the thresholds. We can conclude that both chips are accepted as good chips based on LUI.



(a) (b) (c)

Figure 5-11: MCC results for (a) PCBA1Chip1BGA169 vs. hybrid reference, (b) PCBA1Chip2BGA169 vs. hybrid reference, (c) threshold

Figure 5-12 shows the MCC results for PCB12Chip1BGA169, PCB12Chip2BGA169, PCB13Chip1BGA169 and PCB13Chip2BGA169 respectively. It's clearly shown that MCC values at some inspection points exceed the thresholds for PCB12Chip1BGA169, PCB12Chip2BGA169 and PCB13Chip2BGA169. However, the MCC values are all clearly below the thresholds for PCB13Chip1BGA169, i.e. the chip with small void fraction.

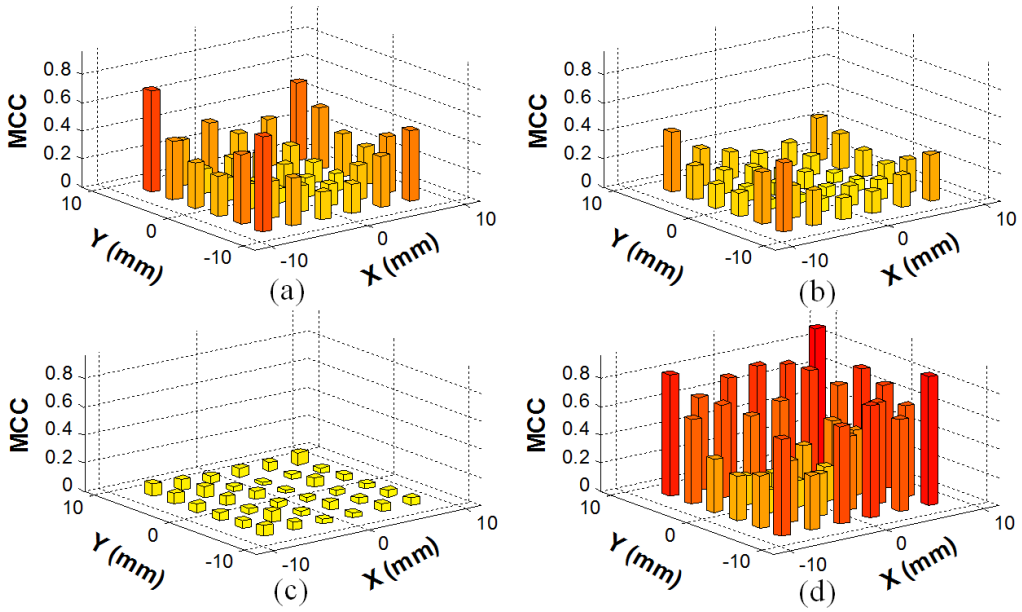


Figure 5-12: MCC results for (a) PCB12Chip1BGA169 vs. hybrid reference, (b) PCB12Chip2BGA169 vs. hybrid reference, (c) PCB13Chip1BGA169 vs. hybrid reference, (d) PCB13Chip2BGA169 vs. hybrid reference

Figure 5-13 plots the MCC values at all 36 inspection points for all the BGA16 chips in the study, as well as the thresholds at all the inspection points. The condition of each inspection point of all the chips can be clearly found out. First, the MCC values at

all the inspection points are below the threshold for all the chips on PCBA1~PCBA11. So it is for PCB13Chip1BGA169 even though PCB13Chip1BGA169 is a chip with small solder ball voids. Then, both poor-wetting chips have lots of inspection points with their MCC values above the threshold. Likewise, the chip with the large void has lots of inspection points with MCC values above the threshold.

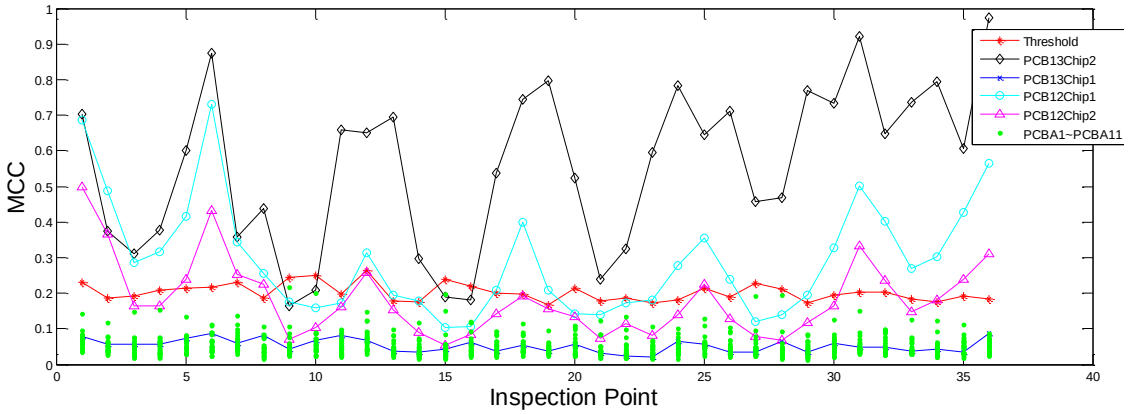


Figure 5-13: MCC values at all 36 inspection points for all the BGA169 chips

The comparison leads to a judgment that chips with small voids are accepted as good chips, while chips with larger voids are assessed as defective chips. Such differences may be attributed to the resolution of the inspection system. Smaller structural changes are expected for the chip with small void fractions. Therefore, the changes on the vibration signal signature are small and are below the resolution of the inspection system. The inspection system treats the small void fractions as manufacturing variations. As the void size increases until the signal changes are above the

manufacturing variation and system inspection variation, the system will flag it, just like the case of large void fractions.

Both poor-wetting chips are rejected as defective chips, as shown in Figure 5-13. One of them has larger MCC values than the other poor-wetting chip, which indicates more severe poor-wetting degradation. Despite the same reflow process for both chips, the level of poor-wetting degradation is different. It is not easy to quantitatively control the degradation level because it is likely that random factors other than the reflow profile may affect the formation of solder ball connection with the printed circuit board.

The inspection results of BGA225 chips are shown in Figure 5-14, and they turned to be very similar with those of BGA169 chips. First, the MCC values at all the inspection points are below the threshold for all the BGA225 chips on PCBA1~PCBA11. So it is for PCB13Chip1BGA225, i.e. the chip with small solder ball voids. Then, both poor-wetting chips have lots of inspection points with MCC values above the threshold. Likewise, the chip with the a large void has lots of inspection points with MCC values above the threshold.

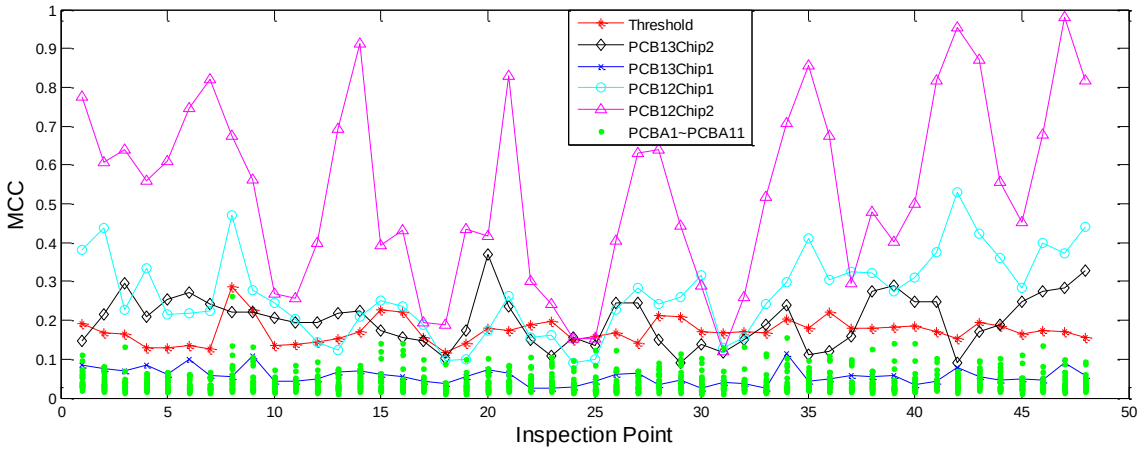


Figure 5-14: MCC values at all 48 inspection points for all the BGA225 chips

5.6 Scanning Acoustic Microscopy (SAM) Test Results

Scanning acoustic microscopy is also used to evaluate solder ball quality. Figure 5-15 shows the C-mode SAM (CSAM) image of a good BGA169 chip at the package-solder interface using a 15MHz transducer. A low frequency transducer was chosen at the expense of good resolution in order to guarantee that ultrasound would be able to penetrate into the BGA package. However, the resolution on the CSAM images is too low to evaluate the quality of the solder balls at the interface. When the transducer is focused on the solder ball/PCB interface (where the poor-wetted solder balls are located), no interpretable CSAM images could be obtained. This is because the ultrasonic waves are largely attenuated and scattered when ultrasonic waves propagate through the spherical solder balls [85]; therefore few ultrasonic waves are reflected back and received by the transducer.

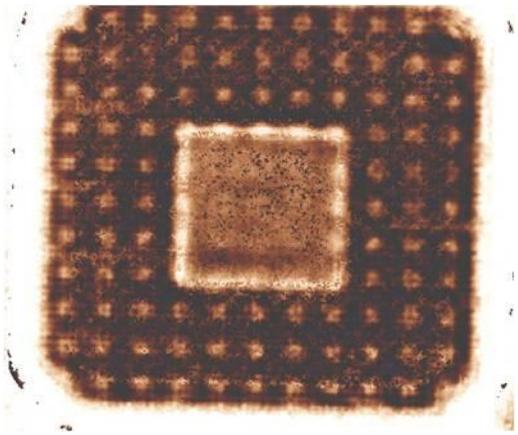


Figure 5-15: CSAM image of a good BGA169 chip at the package-solder interface

Due to the limitations of CSAM in the application of the BGA package, we turn to TSAM. Figure 5-16 shows the TSAM image of the same BGA chip while Figure 5-17 shows the TSAM image of PCBA12Chip1BGA169. The transducer frequency is also 15MHz. It seems that some solder balls are missing in Figure 5-17 compared to Figure 5-16. Actually, there is no solder missing. The non-wetted solder balls lead to open and intermittent connections, so relatively small amounts of ultrasonic waves could propagate through different layers of the package and be picked up by the receiving transducer because of the attenuations due to non-wetted solder balls. Therefore, TSAM is able to distinguish between a good chip and a poorly wetted chip. However, as shown in Figure 5-16, edge effects obscure the solder balls located at the edge of the package, since the ultrasonic waves get scattered when they propagate to the edge. In addition, the solder balls located underneath the silicon die are very blurry. At this location, ultrasonic waves have to propagate through multiple interfaces (molding compound/die, die/die attach and

die attach/substrate) before reaching the receiving transducer. More attenuations and reflections of the ultrasonic waves are expected along the path with multiple interfaces, which make the solder balls smaller and fuzzier.

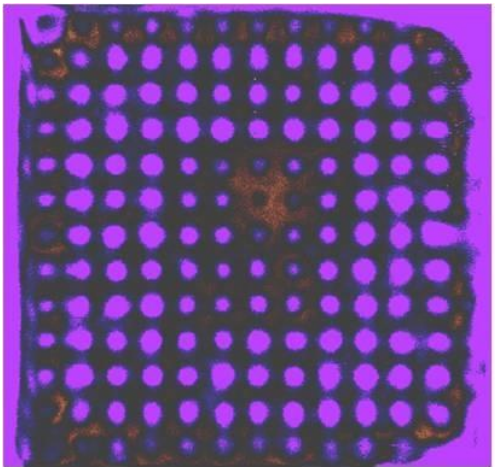


Figure 5-16: TSAM image of a good BGA169 chip

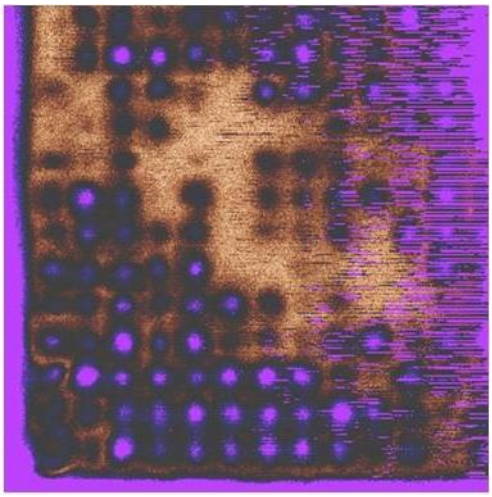


Figure 5-17: TSAM image of PCBA12Chip1BGA169

Figure 5-18 shows the through SAM (TSAM) image of PCBA13Chip2BGA169 (with relatively large void fraction) under a 15MHz transducer. As mentioned earlier, the

ultrasonic waves are unable to propagate through voids in solder balls and this will result in less transmitted ultrasonic signals at the void sites. This should have shown up as a color difference due to the presence of voids in the solder balls similar to the case of 2D X-ray images. However, this kind of void-related color difference is not found in Figure 5-18. The possible reasons could be attributed to the attenuations and scattering of ultrasonic waves during propagation through a thick BGA package. Only a small amount of these ultrasonic waves propagate through the thick BGA package, and then are picked up by the receiving sensor. This definitely decreases the resolution of TSAM.

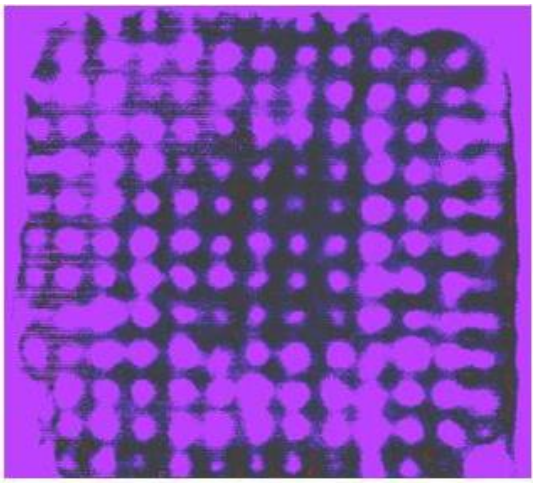


Figure 5-18: TSAM image of PCBA13Chip2BGA169 (chip with relatively large void fraction)

5.7 Cross-Sectioning Results

Finally, cross-sectioning was done to further confirm the presence of the proposed defects, including poor-wetting and voids. Figure 5-19 shows how a typical good solder

ball looks after cross-sectioning. The solder ball has a smooth shape and a tight interfacial connection with the pad. The solder balls fully wets on the copper pad. In addition, no obvious voids can be observed within the solder ball.

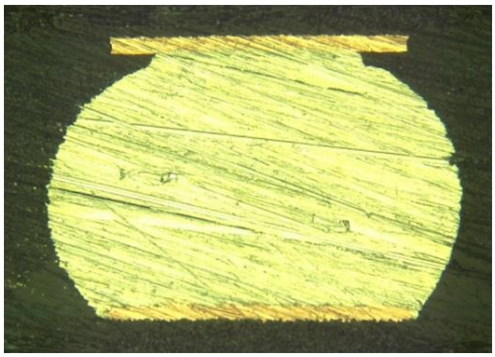


Figure 5-19: Cross-section of a good solder ball

The cross-section images of some typical solder balls from PCB12Chip1BGA169 are displayed in Figure 5-20 and Figure 5-21. These three solder balls didn't fully collapse like the good solder ball in Figure 5-19, which led to the irregular solder ball shapes. In addition, they had poor interfacial connection with the copper pad. The color of the intermetallic compound (IMC) layer in these solder balls was different from that in Figure 5-19 which may be attributed to insufficient intermetallics formed under different reflow profiles. An intermittent connection was observed in Figure 5-21. Because of poor wetting, the interfacial IMC is very brittle. The crack could easily initiate and propagate during regular sample handling and transportation. Finally, it can be clearly seen in Figure 5-20 and Figure 5-21 that the solder balls did not completely cover their copper

pads, as the good solder ball in Figure 5-19 did. All these figures confirm the presence of poor wetting. Since there is not a well-defined metric to quantify the severity of the poor-wetting based on cross-section images, the correlation between the cross-sectioning results and the localized MCC is not explored.

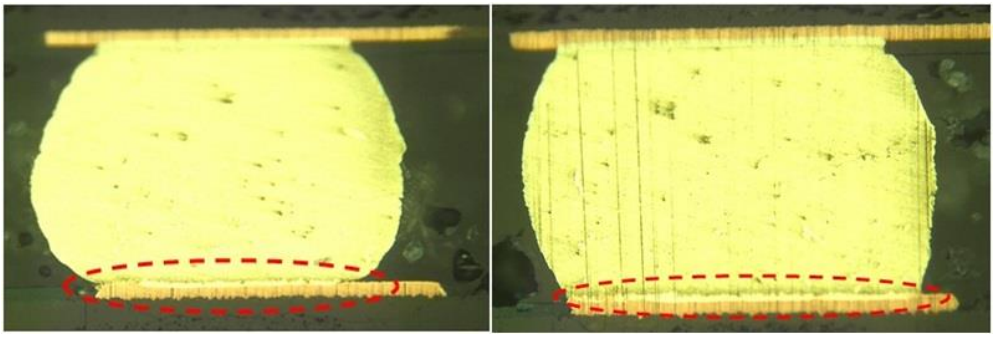


Figure 5-20: Cross-sections of two poor-wetted solder balls

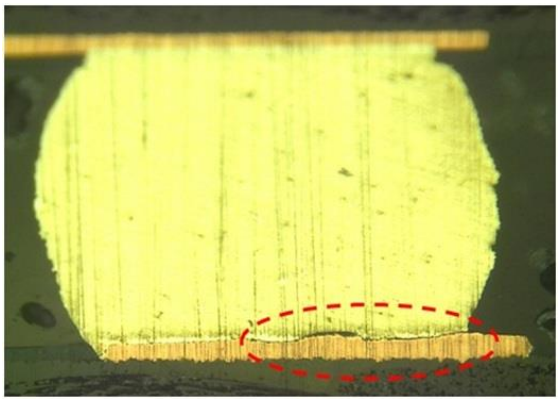


Figure 5-21: Cross-section of poor wetted solder ball showing intermittent connection

The cross-section images of some typical solder balls from PCBA13Chip2BGA169 are shown in Figure 5-22(a) ~ (f). Figure 5-22(a) shows a solder ball with almost no voids. In Figure 5-22(b), a large void is observed near the interface between the solder ball and substrate. In Figure 5-22(c), a large void is located near the interface between the

component and the solder ball. In Figure 5-22(d), a large void is located in the bulk solder. Figure 5-22(e) and (f) show the occurrences of three small voids and two medium size voids respectively near the solder ball interfaces with the component and substrate. Once again, these figures show the variations and randomness of void formations as discussed previously in X-ray inspection results. Voids with different sizes and locations are formed in the solder balls even though all the solder balls go through the same assembly process. Furthermore, it is also observed that voids in solder balls tend to accumulate near the interface between the silicon die and solder balls. This is because the voids, which are essentially gas bubbles, have lower densities than the molten solder. The buoyancy effects cause the bubbles to rise to the top of the solder joints [68]. This justifies the previous assumption during the void classification that voids are located on the interface instead of bulk solder.

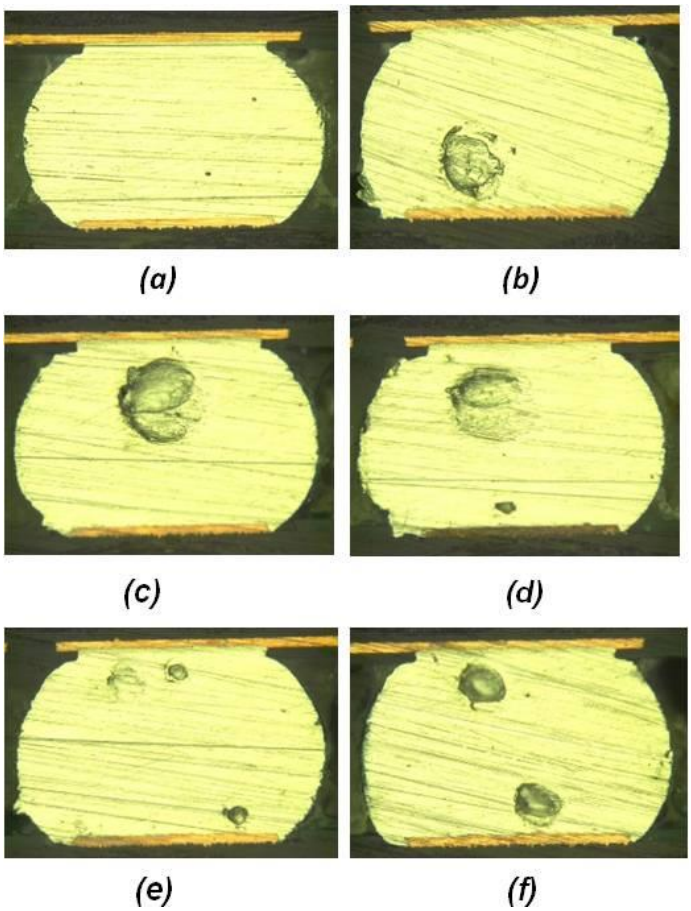


Figure 5-22: Cross-section images of solder balls on PCBA13Chip2BGA169 (a) voids-free, (b) large void at solder ball and substrate interface, (c) voids located near solder ball and component interface, (d) large void in bulk solder, (e) three small voids near component and substrate interface, (f) two medium size voids near component and substrate interface

5.8 Chapter Summary

In this chapter, we demonstrated the application of the LUI system on two types of process-induced defects on BGA packages, including poor-wetting and void. This is the first time that the LUI inspection system was applied to inspect the quality of BGA packages. The LUI inspection system is able to detect poor wetting and voids in the solder

ball with certain resolution. It definitely expands the application scope of this non-destructive inspection technique.

Then we also demonstrated the construction of the pass/fail threshold that separates the good and bad chips from a statistical perspective, while previous analysis usually lacked such a specific or pre-defined threshold.

What's more, other non-destructive techniques were also used to evaluate the same sample set, including X-Ray, SAM and electrical testing. X-ray is very powerful for detecting and measuring solder ball voids. It evaluates each solder joint independently, and gets information such as void size and in-plane location of voids. However, the X-ray technique has problems detecting interfacial defects, because the interfacial defects are too small compared to the standoff height of the solder ball. As for SAM, both CSAM and TSAM have difficulty evaluating the quality of solder balls located along the path with multiple interfaces. Additionally, both CSAM and TSAM images are single-frequency responses, 15MHz here. It's necessary to change the transducers if other frequency responses are needed, which is a disadvantage compared with broadband laser-generated ultrasound.

CHAPTER 6 INSPECTION OF SERVICE-INDUCED SOLDER BALL QUALITY IN BGA PACKAGES

Service-induced defects are defects introduced during service. The reliability issues of solder balls are mainly caused by the operating conditions of the electronic products. These defects can act either as sources for instantaneous catastrophic failures or as latent defects that can affect long term reliability. Compared with process-induced defects, service-induced defects are more common because all microelectronic products are subject to various types of fatigue under normal service. For example, the interconnections in the central processing unit (CPU) of our laptop are subject to shear stress when the laptop is running. All the chips in our cellphones are subject to a transient shock impact when our cellphones fall on the ground. Over time, the fatigue will grow, and accumulate until a failure occurs. One day we may find out that our cellphones cannot connect to WiFi or hear any voice, etc. Overall, we can classify fatigue mechanisms into three types: temperature related, displacement related and acceleration related. In this chapter two of them will be investigated—displacement and temperature related fatigue. In the displacement related accelerated life testing, a FCBGA package is the test vehicle that goes through mechanical bending. In the temperature related accelerated life testing, 2 types of PBGA packages are put into the thermal chamber to go

through temperature cycling. The LUI system will be used to study both types of reliability issues. Other NDT methods including 2D X-Ray, 3D X-Ray, acoustic emission and electrical testing will also be adopted for comparison. In addition, a thermo-mechanical finite element analysis will be presented to support the experimental work.

6.1 Evaluation of Solder Ball Quality under Mechanical Bending

6.1.1 Sample Preparation

The chip of interest is a flip chip BGA (FCBGA) chip reflowed onto an organic PCB as shown in Figure 6-1. There are a total of 1152 solder balls on the second level with their layout available in Figure 6-1. A metal lid, as an encapsulation and heat sink, is glued on the top of the chip to protect the silicon die. A controlled four-point bending test was performed on the samples using the Instron® machine. Figure 6-2 shows a schematic illustration of the four-point bending test set-up [11]. Strain gages were attached at the corner of the package to measure the strain during the bend test. Meanwhile, the daisy chain resistance was monitored in situ. Two acoustic emission sensors were also clamped onto the ends of the PCB to detect the pad cratering crack that cannot be captured by a daisy chain resistance measurement. The sensors were connected to the AE monitoring system via a preamplifier. Three different displacements were used (1.5 mm, 2.5 mm and

4 mm) to produce 3 different quality conditions: defect-free, acoustic detection & no electrical open, and electrical open. Under each displacement setting, two boards were subject to the bending test. Two chips under bending with a 1.5mm displacement are denoted as Chip1 and Chip2. Chip3 and Chip4 are chips under a 2.5mm displacement while Chip5 and Chip6 are bent with a 4mm displacement. A total of 6 boards were used for this investigation.

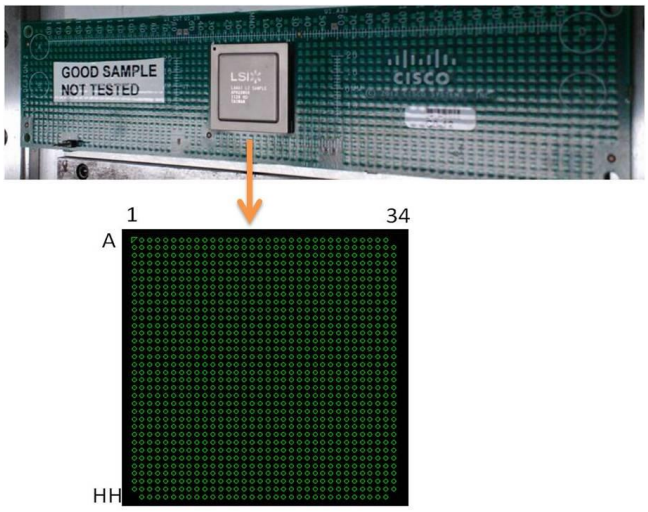


Figure 6-1: Test vehicle and its solder ball layout

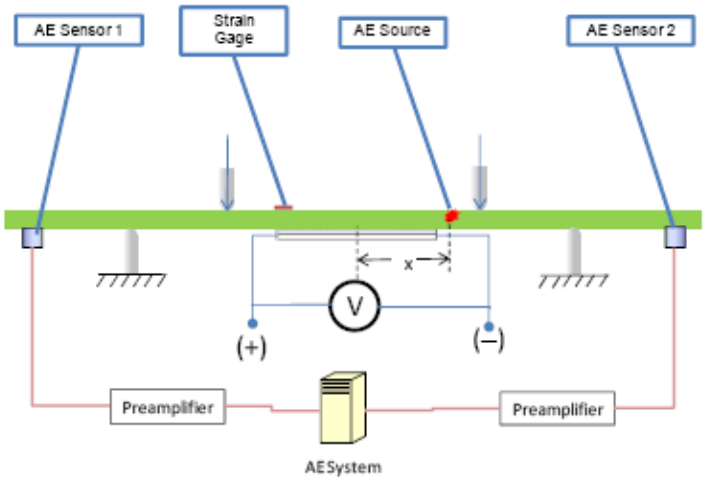


Figure 6-2: Schematic of bending test set-up

The major failure modes under mechanical bending include solder ball cracking and pad cratering. Pad cratering refers to the initiation and propagation of fine cracks beneath BGA pads in the organic substrate materials or PCB laminates [11]. It has caused considerable concern as a type of latent defect that can impact long term reliability. Pad cratering is well known to occur under application of excessive mechanical loads, such as drop and shock tests. And recent work has also shown that pad cratering can also occur under thermal cycling conditions with a wide temperature range [18]. Figure 6-3 shows a schematic illustration of a pad cratering crack.

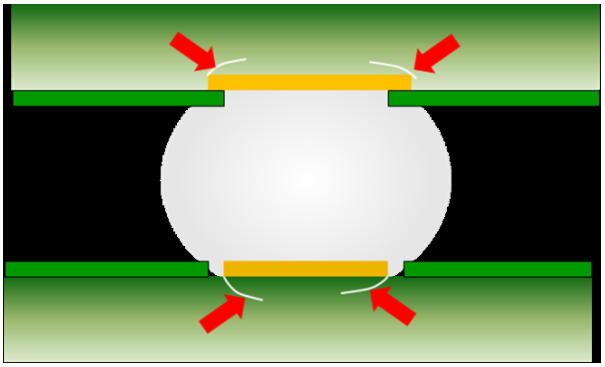


Figure 6-3: Schematic illustration of pad cratering crack

Neither resistance change nor acoustic emission was observed during the 1.5mm displacement bending test. As for the 2.5mm displacement bending test, acoustic emission was detected but without resistance change, which indicated formation of partial pad cratering cracks or partial brittle intermetallic cracks. Both acoustic emission and resistance increase to infinity were observed during the 4mm displacement bending test, which suggested an open daisy chain caused by through pad cratering cracks or through brittle intermetallic cracks. After the bending test, the test samples went through a 3D X-ray test and laser-ultrasound testing.

6.1.2 LUI with Metal Lid

In LUI testing, the test vehicles were tested using the inspection pattern shown in Figure 6-4. During the test, the chip was divided into 4 quadrants (Q1~Q4) for the inspection and the laser was fired at the center of the each quadrant. For example, when

the laser was incident in the center of the first quarter (Q1), signals from inspection points at Q1 were recorded. Then this step was repeated for Q2, Q3 and Q4. The inspection pattern was used is because the chip has a large number of solder balls, which introduced high stiffness for the whole chip-package structure. By dividing the chip into 4 quadrants, signals strength and signal-to-noise ratio could be improved. There are a total of 64 inspection points in each quadrant, thus leading to 256 inspection points for a single chip. The red stripe in Figure 6-4 represents the transition step on the metal lid, which is not a flat surface as shown in Figure 6-1. No inspection points were landed there, since the interferometer cannot receive the laser reflection from an uneven surface.

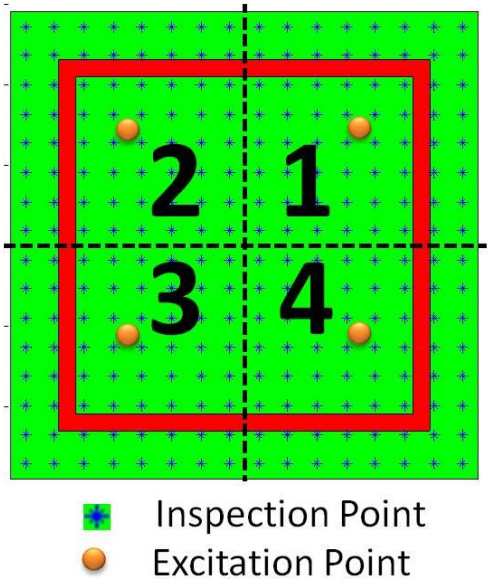


Figure 6-4: Test pattern for test vehicle with metal lid

In LUI testing, signals from one of the good chips, Chip1, are chosen as reference signals for computing MCC. Figure 6-5 shows the MCC bar plots, with the bar heights

indicating MCC values. The larger the height, the less the signals from the tested chip match with the signals from the reference chip, and thus the worse the solder ball quality. As shown in the figure, Chip6, one of two chips with the open electrical path, has the most high-end MCC values, followed by Chip5, the other chip with the open electrical path. Then, Chip4, tested with 2.5mm displacement, has some medium MCC values. The other chip tested with 2.5mm displacement, Chip3, has the lowest MCC values, while the chip with 1.5mm bending, Chip2, has a larger MCC value than Chip3, which doesn't match the acoustic emission inspection results. What's more, it is expected that a larger MCC should be observed at the two vertical edges of the defective chips where the critical solder balls are located under bending. However, this trend is not shown clearly in this figure. We attribute these contradictions to the glue between the metal lid and the silicon die. When the laser-generated ultrasound propagates on the package, any local variation of glue, such as, volume, is likely to introduce certain unknown changes to the signals. These changes to signals tend to change the MCC values even though they have nothing to do with the solder ball quality. To eliminate this potential error source, the metal lid was taken away from the package and the glue was removed. The inspection of chips without the metal lid is discussed in the following section.

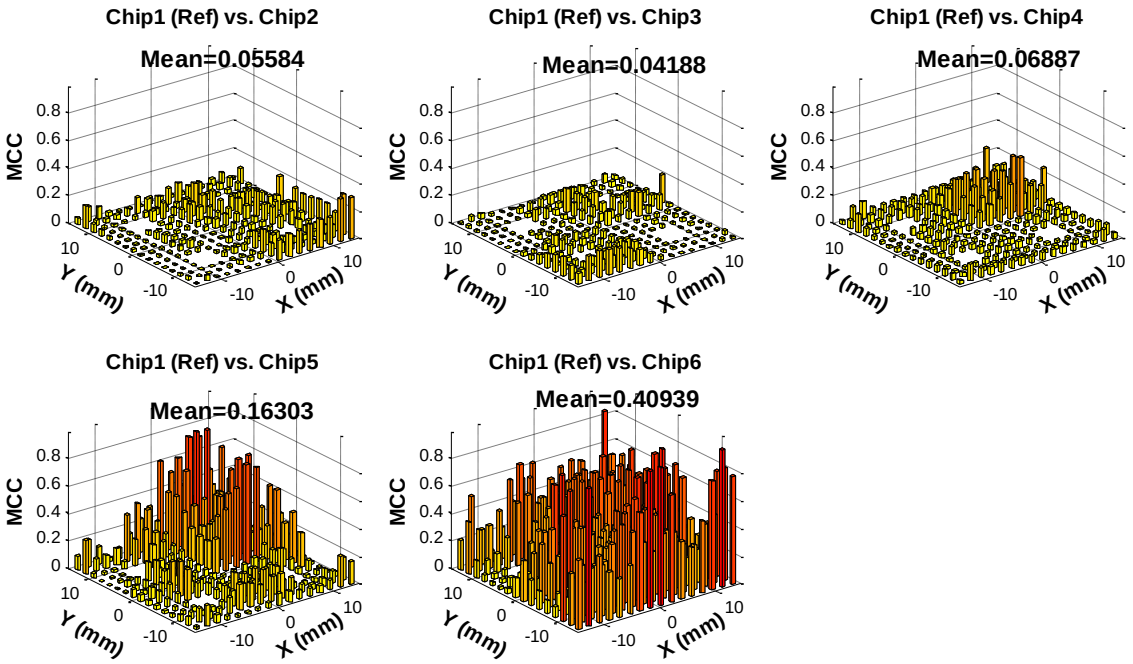


Figure 6-5: MCC bar plots for test chips with metal lid on

6.1.3 LUI without Metal Lid

The metal lid was taken away from the package carefully to avoid any unnecessary damage to solder balls. The residual adhesive on the chip was also removed by using isopropyl alcohol (IPA) to make a clean and flat surface. Figure 6-6 shows what the test vehicle looks like after removal of the metal lid and adhesive. The silicon die, underfill fillet and substrate surfaces were exposed. A similar inspection pattern was used to inspect the chip without the metal lid. As shown in Figure 6-7, the chip was still divided into 4 quadrants. The inspection points on the substrate and silicon die were plotted with different markers since inspection results from the substrate and silicon die will be

compared later. The red stripe in Figure 6-7 represents the presence of underfill fillet. Likewise, no inspection points were placed there because it is not a flat surface.

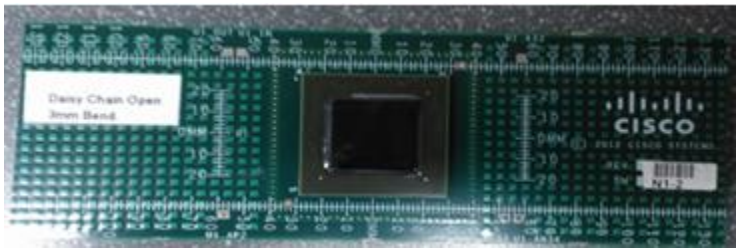


Figure 6-6: Test vehicle after removal of metal lid

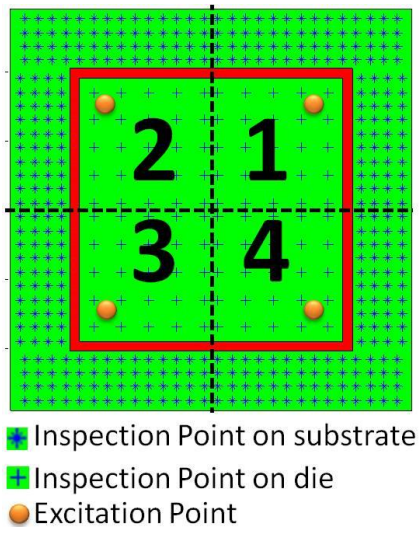


Figure 6-7: Test pattern for Test Vehicle without metal lid

As in the previous test, the signals from Chip1 were also used as reference signals for the tests without the metal lid for computing MCC. Figure 6-8 shows the MCC bar plots for chips without the metal lid. As shown in the figure, both chips with open electrical paths, Chip5 and Chip6, have lots of large MCC values. Moreover, the MCC values at their vertical edges are larger than those at their horizontal edges. This is

expected, because solder balls at the vertical edges are subject to the largest strain during bending. Chip4 has medium MCC values, with some large MCC values located at the top right corner and the left vertical edge. Chip2, one of the good chips, shows small MCC values, which indicates good similarity with the reference chip, Chip1. Therefore, it can be classified as a good chip. Chip3 also has small MCC values, which means that it will also be assessed as a good chip based on LUI results, even though pad cratering was captured using acoustic emission during bending. One possible reason is that the LUI system resolution is below the solder ball defects in Chip3.

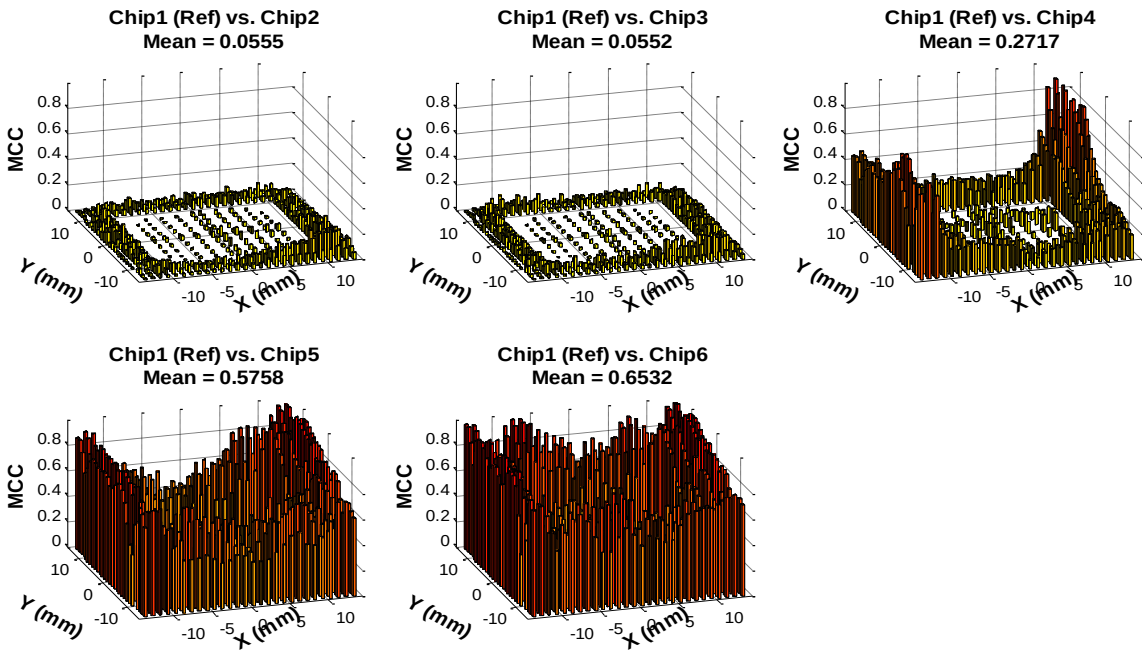


Figure 6-8: MCC bar plot for test chips without metal lid

To explore the LUI test results further, the means of the MCC values at the inspection points from the substrate and the silicon die are plotted and compared in Figure 6-9. First, both Chip2 and Chip3 still show very good similarity with the reference chip at all four quadrants. As for the defective chips, the means of the MCC values at the silicon die are much lower when compared to those at the substrate. The explanation is that the solder balls underneath the substrate degraded much more than the solder balls underneath the silicon die during bending. Compared to the previous test results when the metal lid was on, the test after removing the metal lid and adhesive demonstrated better and more convincing results.

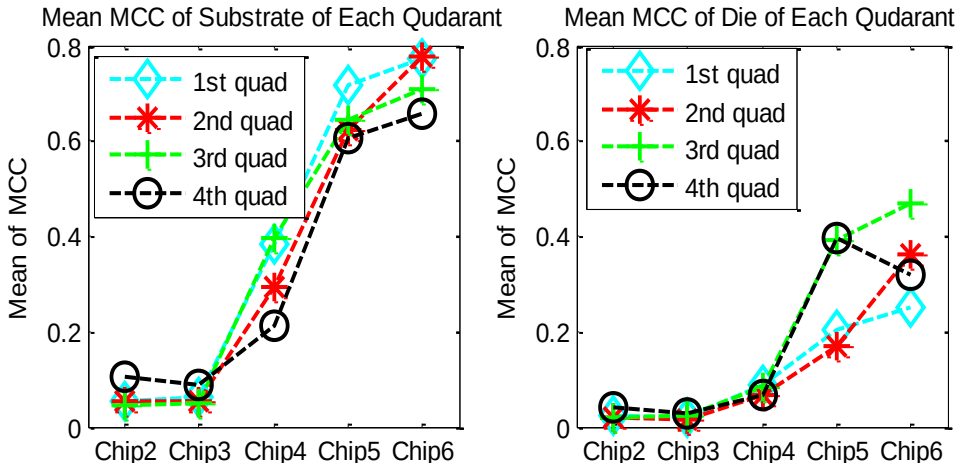


Figure 6-9: Mean of MCC values of inspection points from on substrate and die

Another interpretation of the signals from LUI is the signal energy. Here, signal energy at each IP is calculated using Equation 6.1. Then the average of the signal energy is plotted for each chip. This is shown in Figure 6-10. The two chips with 4mm bending, Chip5 and Chip6 have larger average signal energy, while Chip4, has medium average

energy compared to the two open chips. The two chips with 1.5mm bending, Chip1 and Chip2, as well as Chip3 have small average signal energy. This is because pad cratering and brittle intermetallic cracks will reduce the stiffness of the whole chip package, leading to larger signal amplitude under laser pulse excitation. Therefore, chips with more damage are supposed to have larger average signal energy and this is what we observed in Figure 6-10.

$$E(x) = \sum_t (f(x,t))^2$$
$$where\ E\ is\ energy, f(x,t)\ is\ signal\ amplitude\ at\ time\ t. \tag{6.1}$$

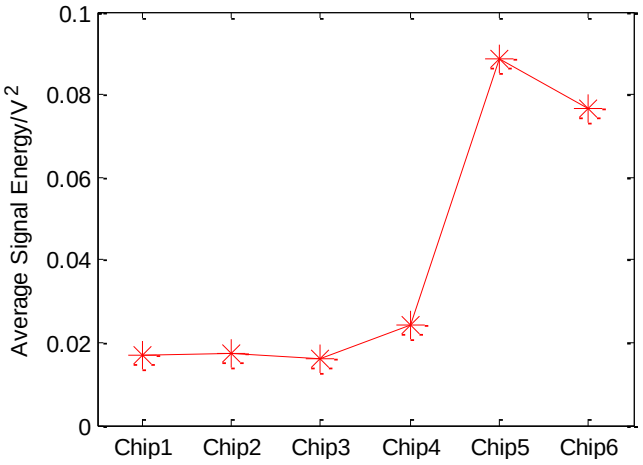


Figure 6-10: Average signal energy for test vehicle

6.1.3 3D X-ray Test Results

After LUI, the test vehicles went through 3D X-Ray testing. Figure 6-11 shows 3D X-ray images for solder ball A1 on Chip6 and its neighboring solder balls. Chip6 has an electrical open path caused by bending. Solder ball A1 is located at the corner, which is highly likely to have defects like pad cratering and intermetallic cracks because of

bending damage. However, it is difficult to observe any defect based on the 3D X-ray images. Similarly, no obvious defects were found for other solder balls located at the corners on Chip6 nor were they found on any other defective chips, as shown in Figure 6-12 and Figure 6-13.

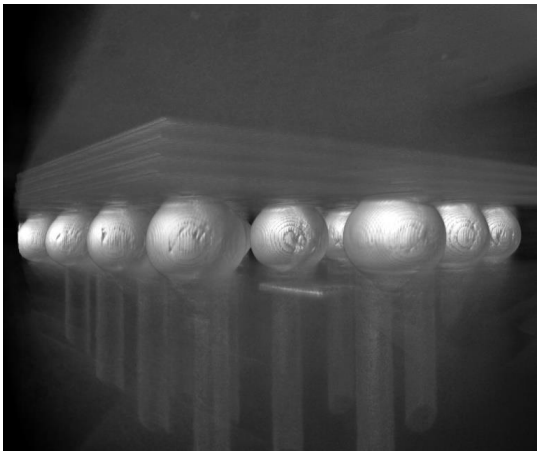


Figure 6-11: 3D X-ray Images for solder ball A1 on Chip6 and its neighboring solder balls

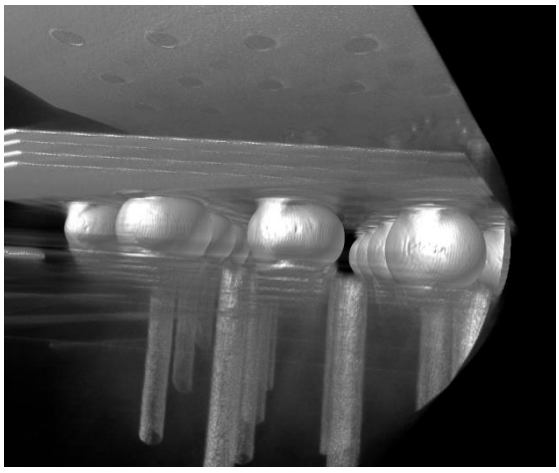


Figure 6-12: 3D X-ray Images for solder ball A1 on Chip5 and its neighboring solder balls

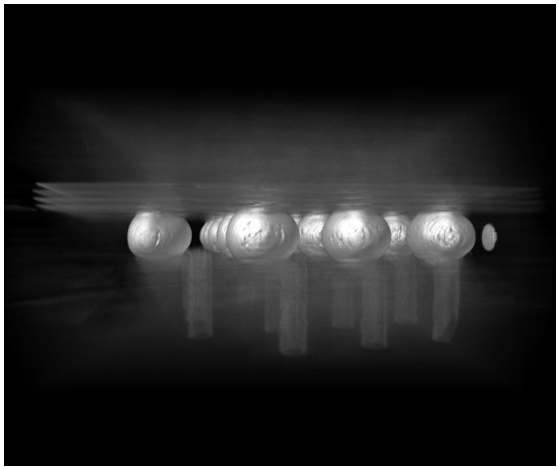


Figure 6-13: 3D X-ray Images for solder ball A34 on Chip4 and its neighboring solder balls

6.1.4 Cross-Sectioning Results

Finally, the chips were cross-sectioned and Scanning Electron Microscopy (SEM) was used to evaluate the solder ball quality. Only the solder balls at the edge of the chip were cross-sectioned since that's where defects were expected to show up under mechanical bending. To quantify the cross-sectioning results, a severity index from 0 to 1 was assigned to each individual solder ball based on its defect severity. A severity index of 0 represents a good solder ball with no defects. The index level increases with the solder ball defect severity until 1, which represents both major pad cratering and intermetallic break simultaneously in a solder ball. Table 6-1 lists the classification of the severity index with the corresponding defect severity and their symbols, and Figure 6-14 shows some typical cross-sectioning images of solder balls with different levels of defect severity. Pad cratering is classified into 3 levels of severity: laminate crack (fine pad

cratering), intermediate pad cratering and major pad cratering. Figure 6-14 (a) shows an example of major pad cratering that already caused an electrical open path. An example of intermediate pad cratering is shown in Figure 6-14 (b) as a partial crack. The example of a laminate crack (fine pad cratering) is also shown in Figure 6-14 (e). In addition, examples of intermetallic crack are also seen in Figure 6-14 (c) and (f).

Table 6-1: Classification of solder ball severity index

Defect Description	Severity Index	Symbol
Good	0	ʘ
Laminate Crack	0.125	—
Intermediate Pad Cratering	0.25	/
Inter-metallic Break	0.50	⁘
Major Pad Cratering	0.50	X
Major Cratering & Inter-metallic Break	1.00	↕

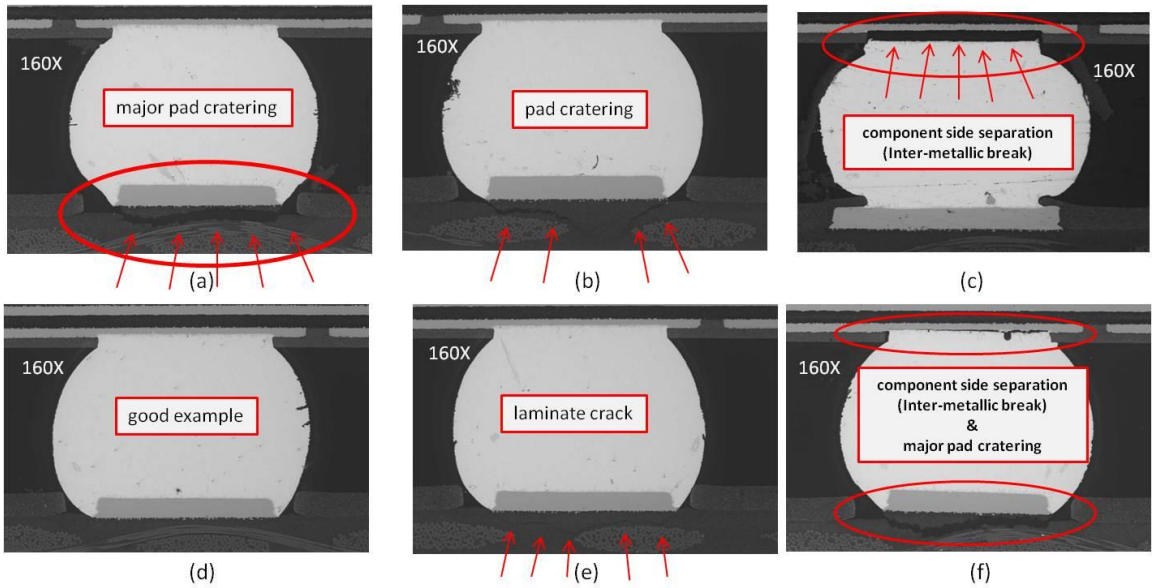


Figure 6-14: Cross-sectioning images of solder balls with different levels of defect severity: (a) major pad cratering, (b) intermediate pad cratering, (c) intermetallic crack (d) good solder ball, (e) laminate crack (fine pad cratering), (f) both major cratering and intermetallic break

After the assignment of the severity index, the averages of the severity index in each quadrant are plotted in Figure 6-15. The averages of the severity index range from 0 to 1, which can be easily correlated to MCC with the same range. No defects are observed for the solder balls of Chip1 and Chip2. Therefore, the average is zero for both chips. Comparing this figure with Figure 6-9, which plots the mean MCC values of each quadrant, there is a very strong correlation and similarity. Chip6 has the largest average severity index at all quadrants, which matches its largest means of MCC in the LUI results. Then the quadrants on Chip5 have the second largest average of severity index, based on cross-sectioning results that correspond to the second largest means of MCC

based on LUI results; this is followed by Chip4. Chip 3 has a very small average severity index, and it also has small MCC values in the LUI test.

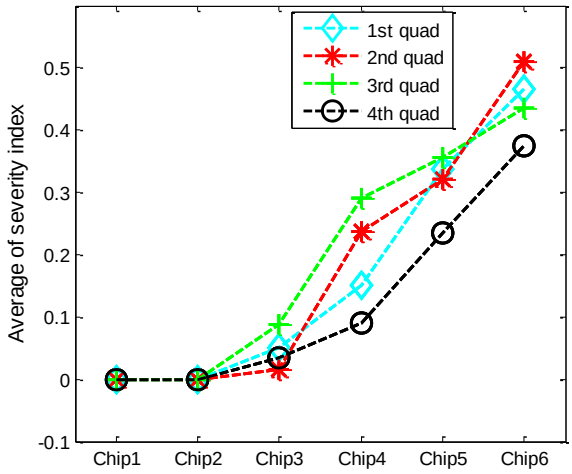


Figure 6-15: Average of severity index for test vehicles

6.1.5 2D MCC Color Map

To better interpret the correlation between the LUI results and the cross sectioning results, the 3D bar plot of the MCC value was converted into a 2D color map, with color specifying the magnitude of MCC, i.e. the local severity of solder ball defects. Inspection results on the silicon die are not included during the conversion because the generation of 2D color maps requires high spatial inspection density for data interpolation. However, as shown in the inspection pattern (Figure 6-7), the inspection density on the silicon die is relatively small. Also, cross-sectioning is only focused on the edge of the chip instead of the silicon die region. The MCC color map and cross-sectioning details will be put together for analysis. Figure 6-16 shows Chip2's MCC color map and its detailed

cross-sectioning results. No defects are observed during cross-sectioning which validates its MCC color map, dominated by deep blue. As shown in Figure 6-17, the MCC color map of Chip3 is very similar to that of Chip2. However, some laminate cracks (fine pad cratering) are present at the vertical edges; these are captured by the acoustic emission during the bending test but missed by the LUI system. As mentioned previously, a possible reason is that the severity of the laminate cracks (fine pad cratering) is below the LUI system resolution. Signal changes due to these are not picked up by the system.

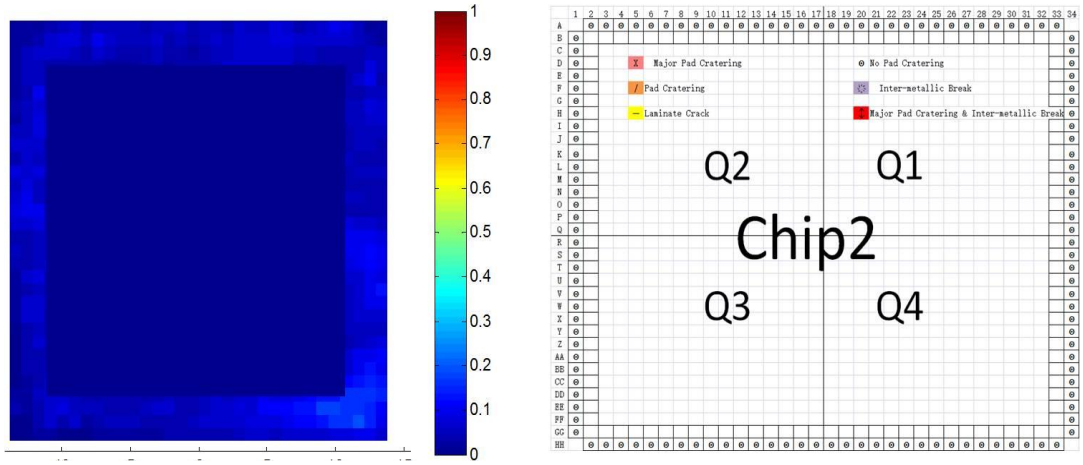


Figure 6-16: MCC color map and the cross-sectioning results for Chip2 (Good Chip)

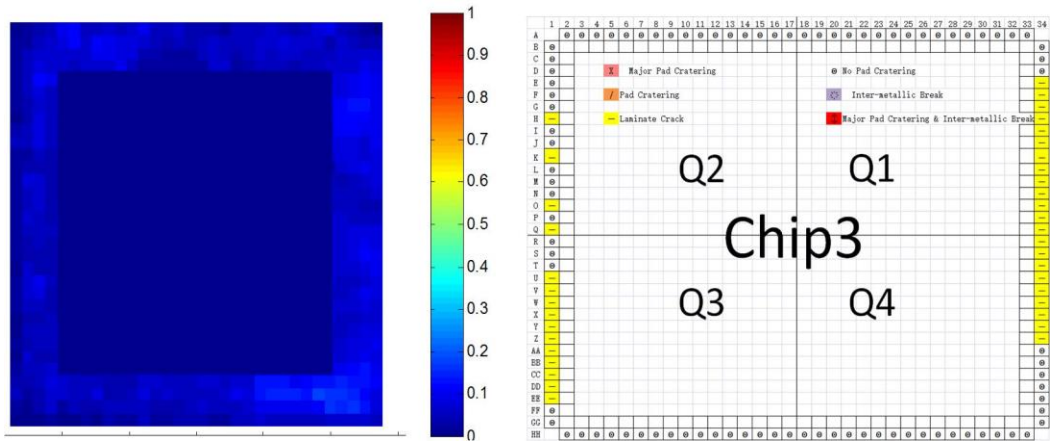


Figure 6-17: MCC color map and the cross-sectioning results for Chip3 (Cracked Chip)

Figure 6-18 shows Chip4's MCC color map and its cross-sectioning results. Even though Chip4 was bent under the same displacement as Chip3, it was damaged more severely. As shown in the cross-sectioning results, some major pad caterings are observed at the lower part of the left edge where light yellow and red regions show up in the MCC color map. A similar scenario is also found at the top part of the right edge. Light blue and green regions at the lower right edge correspond to the solder balls with laminate cracks that are less severe than major pad caterings. At the middle of the two horizontal edges, the solder balls are intact, which also matches the color map, where the corresponding regions are dominated by blue. Overall, there is a strong match between the MCC color map and the cross sectioning results for Chip4.

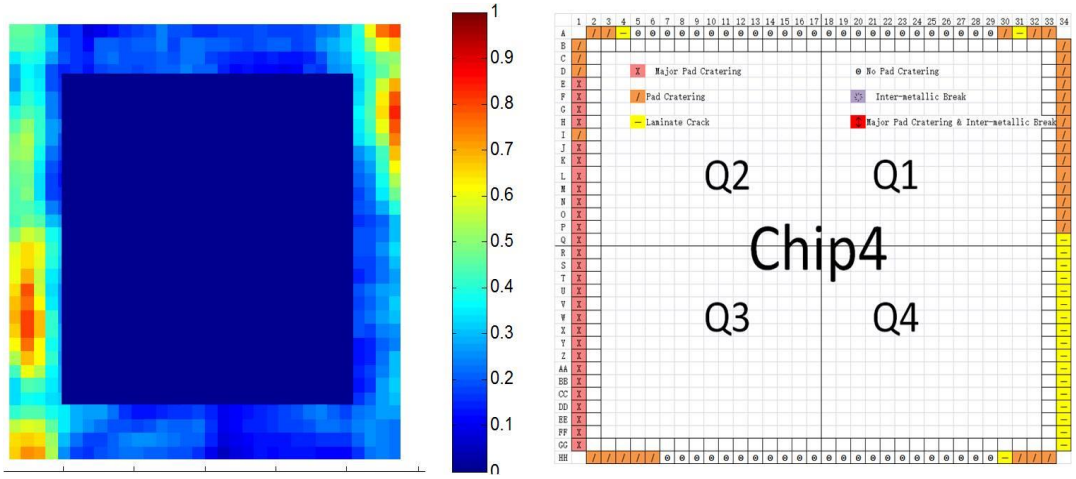


Figure 6-18: MCC color map and the cross-sectioning results for Chip4 (Cracked Chip)

Figure 6-19 and Figure 6-20 show the MCC color maps and the cross-sectioning results for Chip5 and Chip6, respectively. For both chips, the two vertical edges are dominated by deep red in the MCC color maps, which indicate severe solder ball damage. The solder ball damage was discovered during cross-sectioning and included inter-metallic breaks and major pad cratering. On the horizontal edges, from center to corner, the solder ball quality degradation is clearly reflected by the color evolution on the color map, from blue to yellow and finally to red. For both chips, some intact solder balls remain at center of the horizontal edges as shown in the cross-sectioning results. However, as shown in the MCC maps, their MCC values are about 0.4 instead of some small values like 0.1. The reason is that their responses under laser excitation are affected by adjacent defective solder balls. These defects will change the whole chip package structure, thus altering the response under laser excitation for all the inspection points.

With the help of the MCC color map, the LUI testing results show a better correlation with the cross-sectioning results.

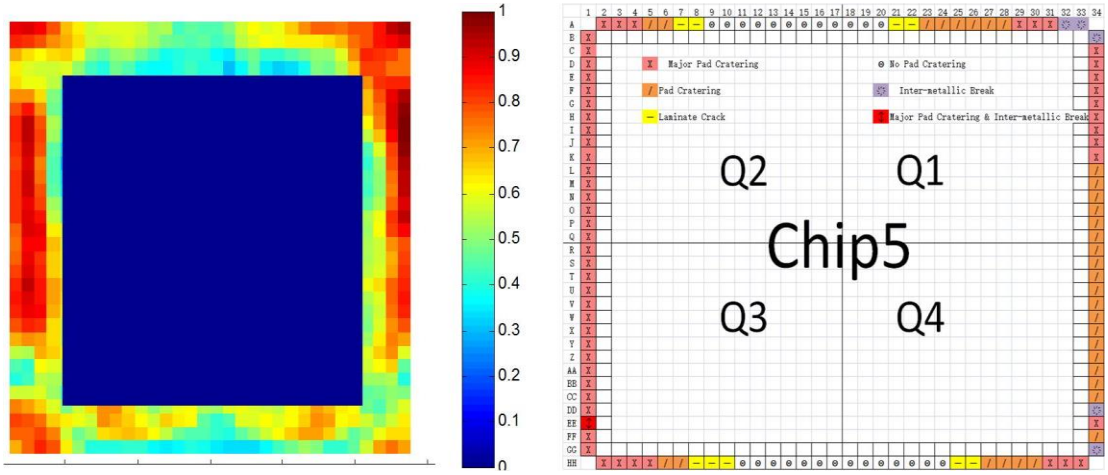


Figure 6-19: MCC color map and the cross-sectioning results for Chip5 (Open Chip)

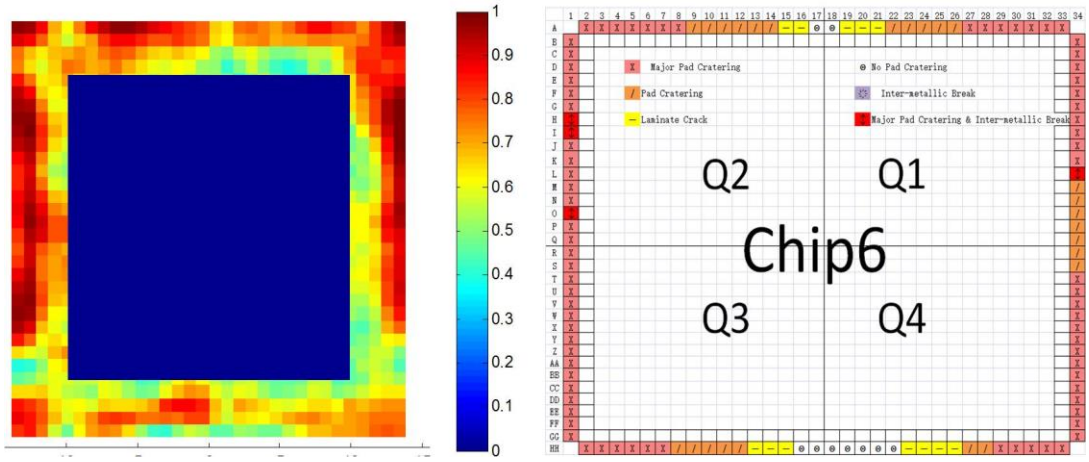


Figure 6-20: MCC color map and the cross-sectioning results for Chip6 (Open Chip)

6.2 Evaluation of Solder Ball Quality under Thermal Cycling

6.2.1 Finite Element Analysis of Thermo-Mechanical Reliability

In this section, a three-dimensional (3-D) finite element model is constructed for BGA169 and BGA225, respectively. Only a quarter model was built by taking advantage of the structural symmetry of both packages. ANSYS® 14 is the software package used in this work.

A finite element model often starts with geometric modeling. The geometric modeling includes building the die, die adhesive, molding compound, substrate, copper pad, solder mask, solder ball and printed circuit board. All the dimensions were measured using a mounted cross-section sample.

Meshing is needed after geometric modeling. There are 2 mesh methods: free mesh and mapped mesh. In free mesh, there are no restrictions in terms of element shapes and node location, while mapped mesh allows the user to define the element shape and node location. A free volume mesh contains only tetrahedron elements, while a mapped volume mesh contains only hexahedron elements. Mapped mesh is preferred for the purpose of simulation accuracy.

The volumes were meshed using linear elastic and viscoelastic elements, SOLID185. SOLID185 is used for 3-D modeling of solid structures. As shown in Figure 6-21, it is defined by eight nodes with three degrees of freedom at each node: translations in the nodal x, y, and z directions. The element has plasticity, hyperelasticity, stress stiffening, creep, large deflection and large strain capabilities.

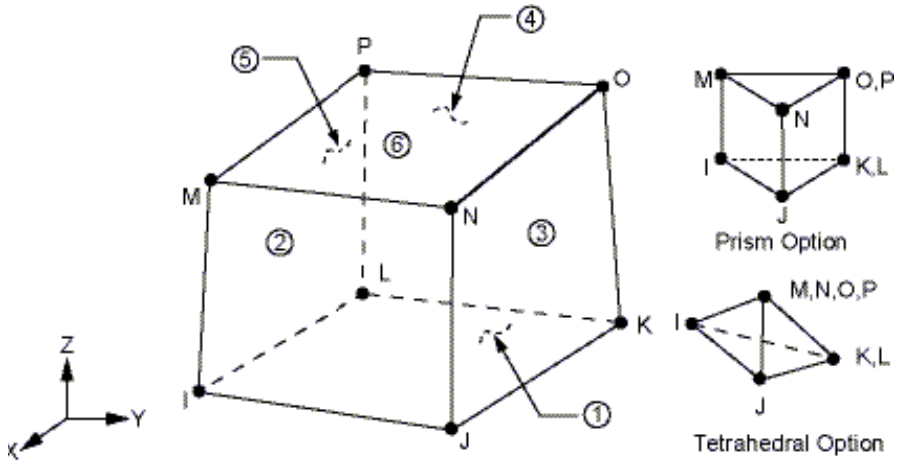


Figure 6-21: 3-D structure solid of SOLID185 element [Source: ANSYS® User Manual]

The meshing of representative solder ball columns including the die, die adhesive, molding compound, substrate, copper pad, solder mask, solder ball and printed circuit board is shown in Figure 6-22 and Figure 6-23 in detail, where different colors represent different materials in the figure.

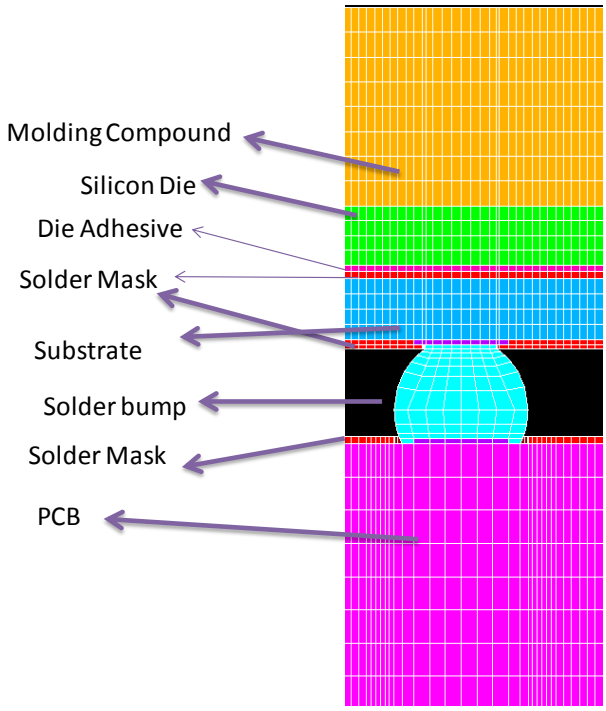


Figure 6-22: Meshing of representative solder ball column

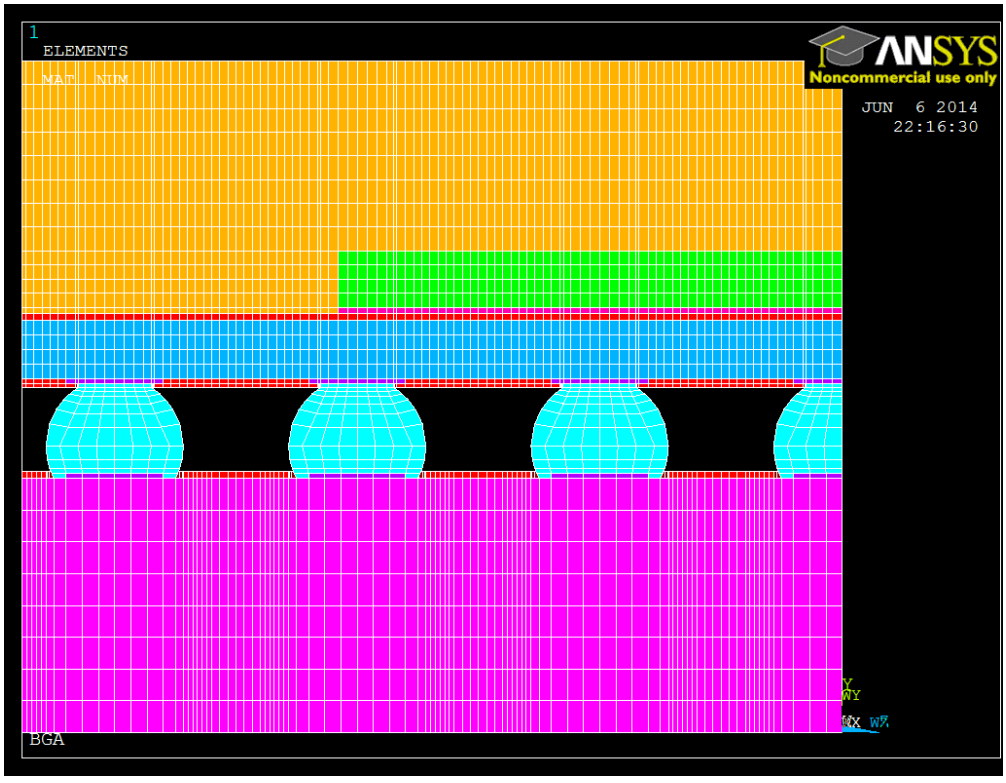


Figure 6-23: Cross-section image of the meshing of the PBGA modeling

To accurately simulate the thermomechanical response of the PBGA assembly, material properties were chosen to be temperature dependent whenever the data was available. Table 6-2 shows the material properties used in this work.

Table 6-2: Material properties used in the finite element modeling

Material	Model	Modulus(GPa)	Possison's Ratio	CTE(ppm/C)
Die	Elastic Iostropic	131	0.3	2.8
Die Adhesive	Temperature Dependent Elastic, Iostropic	1.8@213K 1.8@298K 0.24@213K 0.24@213K	0.3	60@213K 60@253K 129@293K 129@573K
Copper	Elastic Iostropic	120	0.35	17
PCB	Elastic Orthotropic	in-plane:15.93 out-of-plane: 6.94	in-plane:0.39 out-of-plane: 0.11	in-plane:13 out-of-plane: 65
Substrate	Elastic Orthotropic	28.5	0.3	in-plane:15 out-of-plane: 55
Solder	Temperature Dependent Viscopalstic, Iostropic	53.4@213K 49.0@273K 45.5@323K 40.0@398K	0.35	20.6@213K 21.3@273K 22.1@323K 23.4@398K
Mold Compound	Elastic Iostropic	25	0.3	9
Solder Mask	Tempertature Dependent Elastic, Iostropic	2.4	0.29	60@213K 60@353K 130@393K 130@573K

Solder creep behavior is temperature and time dependent. These effects become significant at temperatures of $0.4T_{melting}$, and above. The melting point for SAC305 solder is around 217^{o}C; therefore, creep behavior in SAC305 lead-free solders is important in thermomechanical fatigue calculations. To model these effects, Anand's unified viscoplastic model was employed to represent the inelastic deformation behavior for solder alloys. The viscoplastic model is very suitable for large, isotropic, viscoplastic deformations in combination with small elastic deformations and is a single-scalar internal variable model [86]. Two basic features in the Anand model make it ideal for this application. First, this model needs no explicit yield condition and no loading/unloading criterion, which makes it easier to apply to a wide range of problems. Second, this model employs a single scalar as an internal variable to represent the averaged isotropic resistance to plastic flow, the deformation resistance s. ANSYS provides a simple way to directly implement this material model by providing the nine constants listed in Table 6-3. The stress dependent strain rate is shown in Equation 6.2, where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, m is the strain rate sensitivity, ξ is the multiplier of stress, R is the gas constant and T is the absolute temperature. These properties have been determined experimentally by previous researchers [87].

$$\dot{\varepsilon_p} = Ae^{\frac{-Q}{RT}}[sinh(\xi\frac{\sigma}{s})]^{\frac{1}{m}} \qquad (6.2)$$

Table 6-3: Material constants of Anand's viscoplastic model for SAC305 solder

Parameter	Value	Description
S_0 (N/mm^2)	2.15	Initial value of deformation resistance
Q/k (1/K)	9970	Activation energy/Boltzmann's constant
A (1/sec)	17.994	Pre-exponential factor
ξ	0.35	Multiplier of stress
m	0.153	Strain rate sensitivity of stress
H_0 (N/mm^2)	1525.98	Hardening constant
$\hat{S}$ (N/mm^2)	2.536	Coefficient for deformation resistance saturation value
N	0.028	Deformation resistance value
a	1.69	Strain rate sensitivity of hardening

As for the boundary condition, the free body motion is constrained at the lower left element in the x, y and z directions. What's more, zero displacement is applied to two symmetric surfaces normal to X and Y directions.

Figure 6-24 and Figure 6-25 show the quarter model of BGA169 and BGA225, respectively. They are very similar to each other except for the dimensions and the number of solder balls.

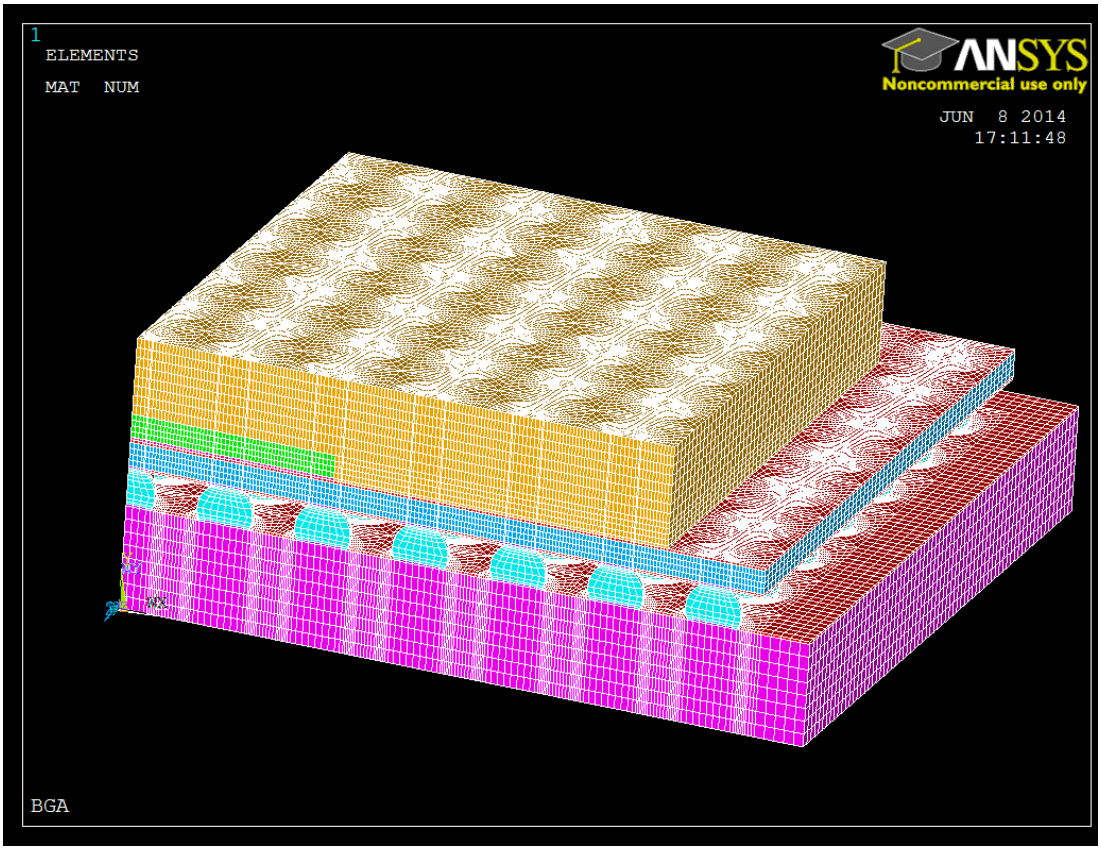


Figure 6-24: Quarter model of BGA169

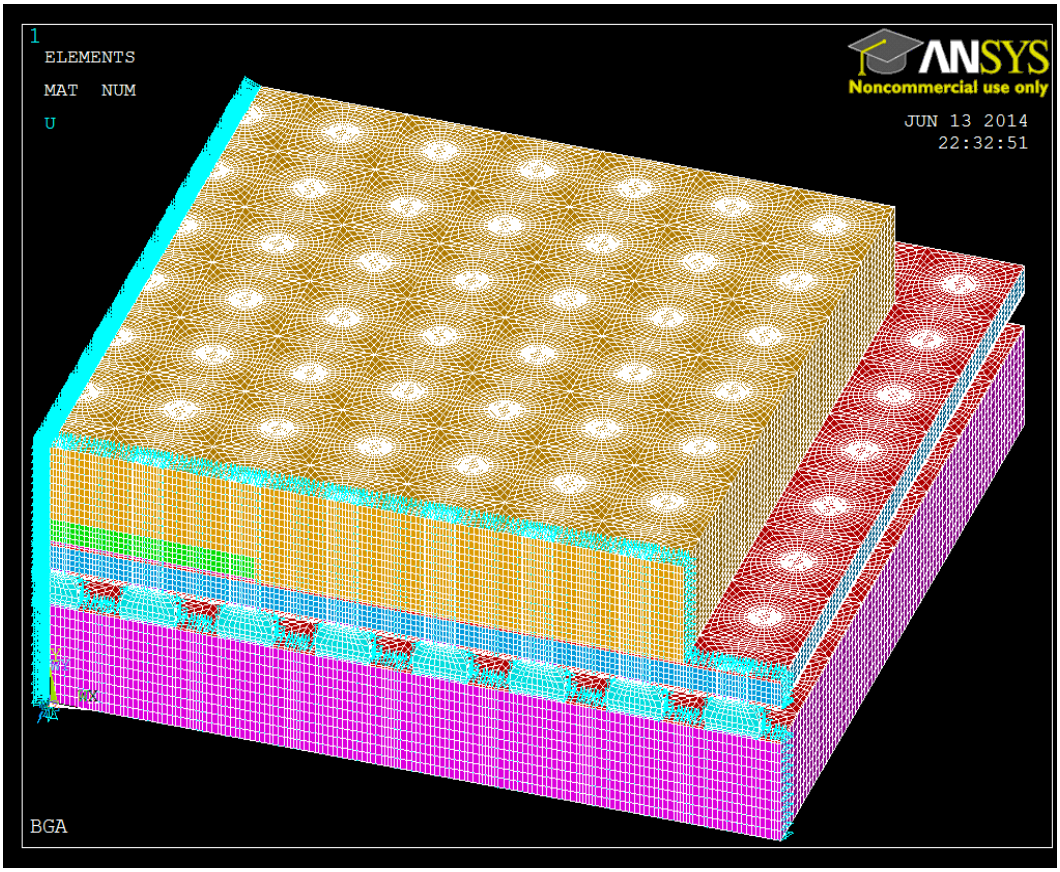


Figure 6-25: Quarter model of BGA225

Both quarter models were subjected to a cyclic thermal loading from -40°C to 125°C, the same as the condition used in the actual ATC test. The stress-free reference temperature was set at 217°C, which is the melting point of solder balls. The temperature profile is shown in Figure 6-26. First, the package is cooled down from its stress-free temperature to room temperature; then ATC temperature loading from -40°C to 125°C is applied. The dwell time at the two extreme temperatures is 15 minutes, while the ramp time is 15 minutes. Therefore, each cycle takes 1 hour.

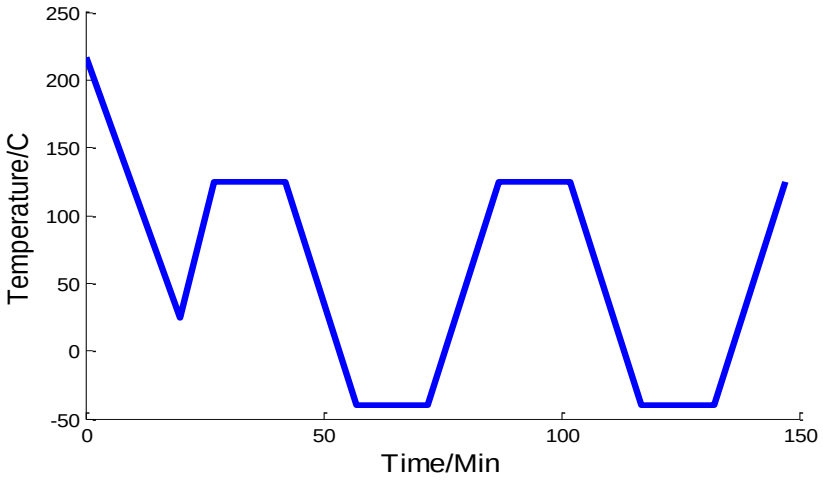


Figure 6-26: Temperature profile used in the finite element simulation

The main motivation of this simulation is to identify the critical solder ball location which is the solder ball that is most likely to fail first. This could be done by extracting damage metrics from the simulation results. The effective plastic strain and inelastic strain energy density are the two most commonly used damage metrics.

The effective plastic strain of the solder balls can be calculated according to Equation 6.3 [88]

$$\varepsilon_{\text{eff}} = \frac{\sqrt{2}}{3}\sqrt{(\varepsilon_1 - \varepsilon_2)^2 + (\varepsilon_1 - \varepsilon_3)^2 + (\varepsilon_3 - \varepsilon_2)^2} \tag{6.3}$$

where ε_i $(i = 1,2,3)$ are the principal strains.

The inelastic strain energy density *W* [89], which is integral of the stress σ_{ij} with respect to the inelastic strain ε_{ij}^{in}, and is defined in tensor format in Equation 6.4.

$$W = \int_0^{\varepsilon_{ij}^{in}} \sigma_{ij} d\varepsilon_{ij}^{in} \tag{6.4}$$

Figure 6-27 shows the effective plastic strain contour of the solder balls from the BGA169 quarter model at the end of the 4th cycle. The maximal effective plastic strain is located at the second solder ball on the diagonal direction from the center that is the neutral point. Figure 6-28 is the zoom-in view of at the maximal effective plastic strain location; it shows that the maximal effective plastic strain is located on the top layer of the solder ball at the component side. Figure 6-29 shows the inelastic strain energy density contour for the same model at the same time. And it leads to the same observation as the case of effective plastic contour. The maximal inelastic strain energy density is located on the top layer of the second solder ball on the diagonal direction from the center. Therefore, it can be concluded that the critical solder ball is the second solder ball on the diagonal direction from the center, and the crack starts to initiate at the top layer of that solder ball at the component side based on finite element simulation results for BGA169. This observation matches the mechanics theory. The critical solder ball is expected to appear at the shadow of the die corner that is the location of the largest CTE mismatch in the PBGA assembly. Figure 6-31, Figure 6-32, Figure 6-33 and Figure 6-34 show the effective plastic strain contour and inelastic strain energy density contour for BGA225 at the 5th cycle, respectively. Likewise, the critical location in BGA225 is located on the top layer of the second solder ball on the diagonal direction from the center. Even though the number of solder balls in BGA225 is different from that of BGA169, they have the same die size, which leads to the same location of the critical solder ball. In BGA225, the

solder ball located at the shadow of the die corner is exactly the second solder ball on the diagonal direction from the center.

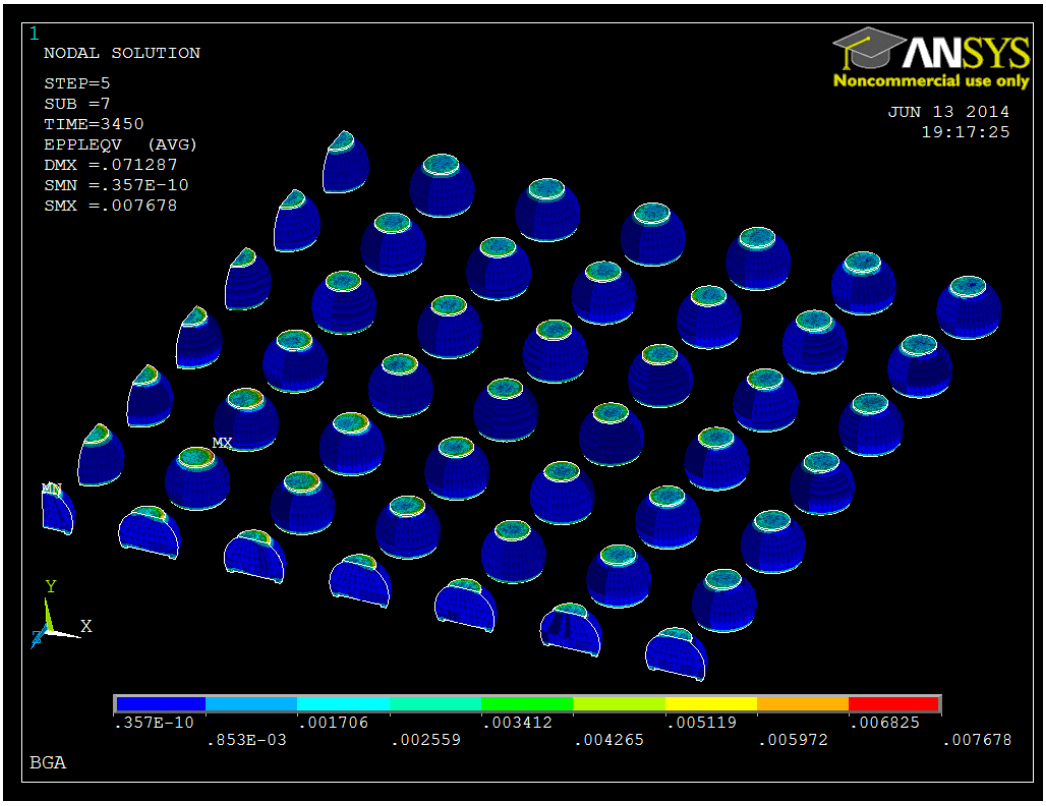


Figure 6-27: Effective plastic strain contour of the solder balls of BGA169

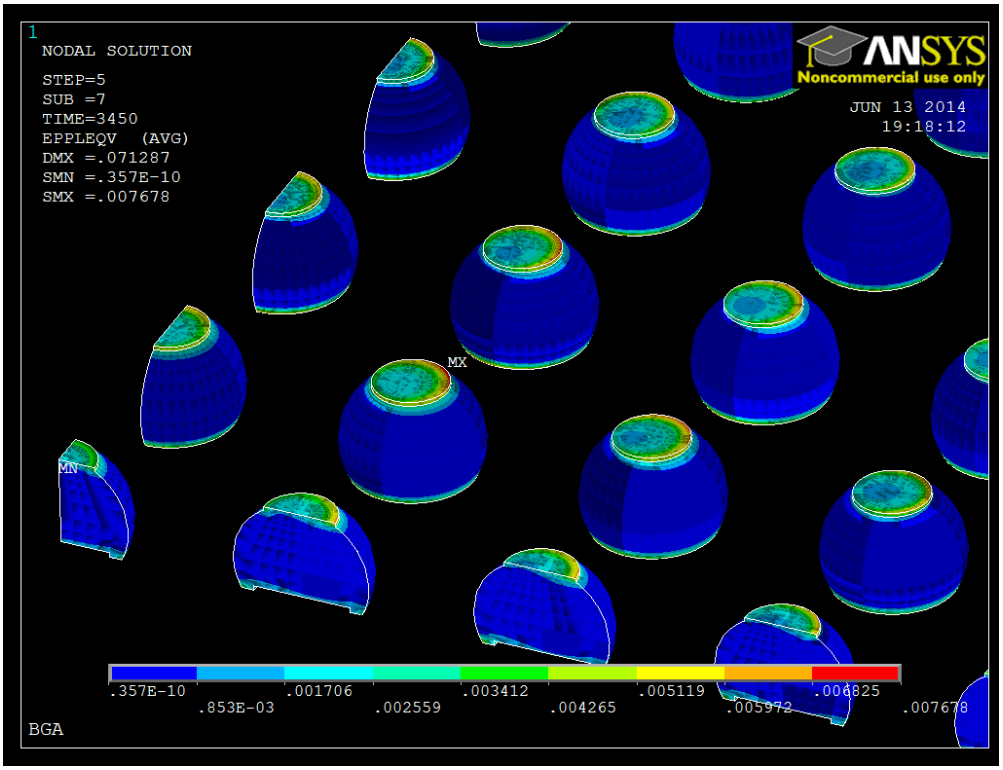


Figure 6-28: Zoom-in of maximal effective plastic strain contour of the solder balls of BGA169

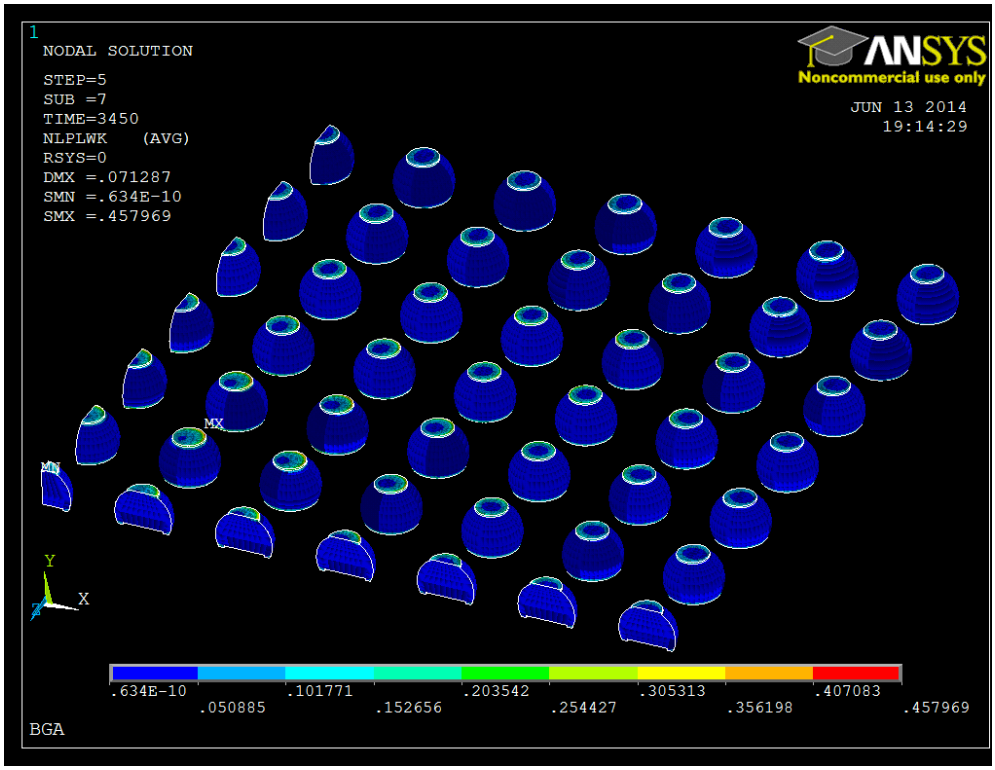


Figure 6-29: Inelastic strain energy density contour of the solder balls of BGA169

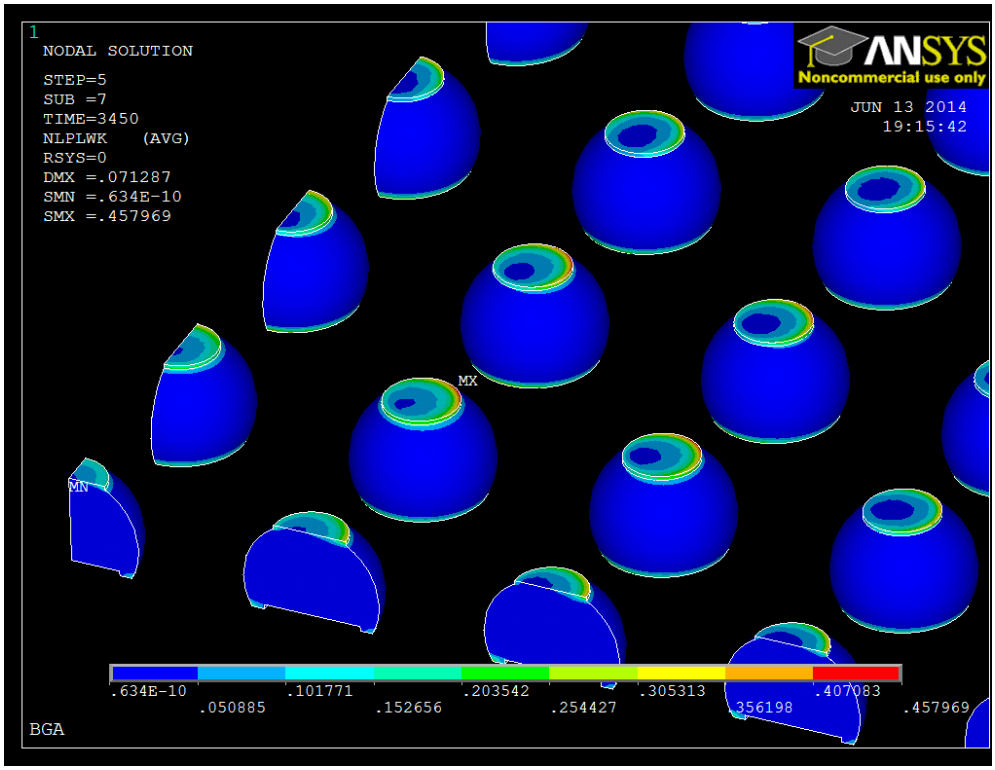


Figure 6-30: Zoom-in of maximal inelastic strain energy density contour of the solder balls of BGA169

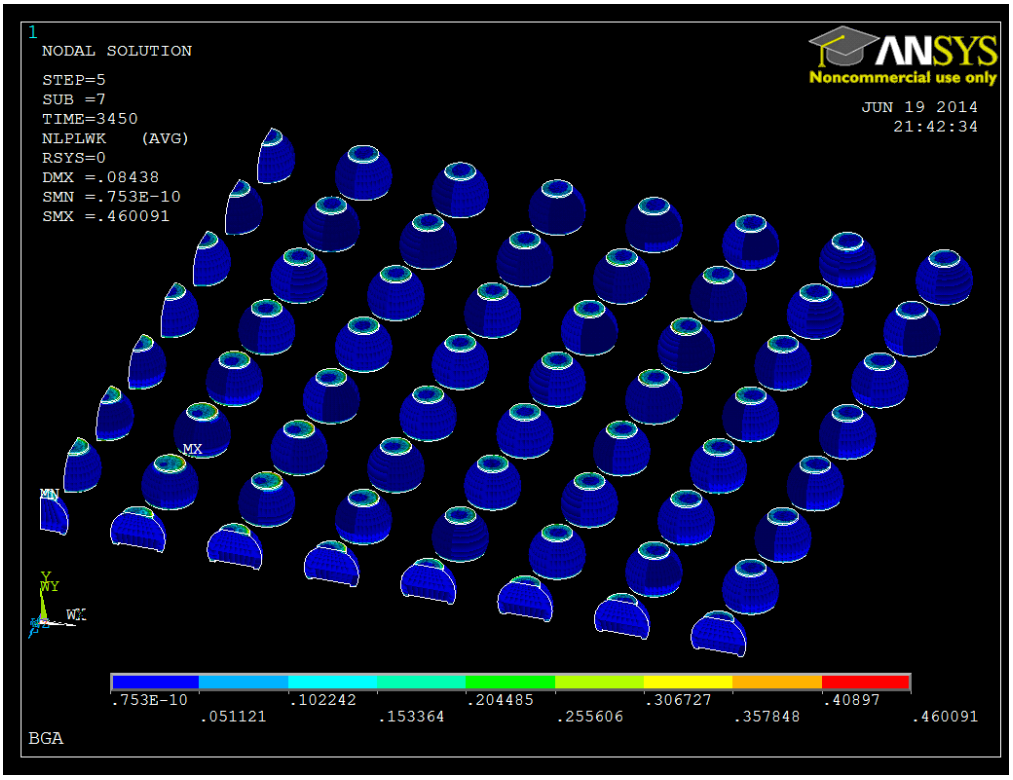


Figure 6-31: Inelastic strain energy density contour of the solder balls of BGA225

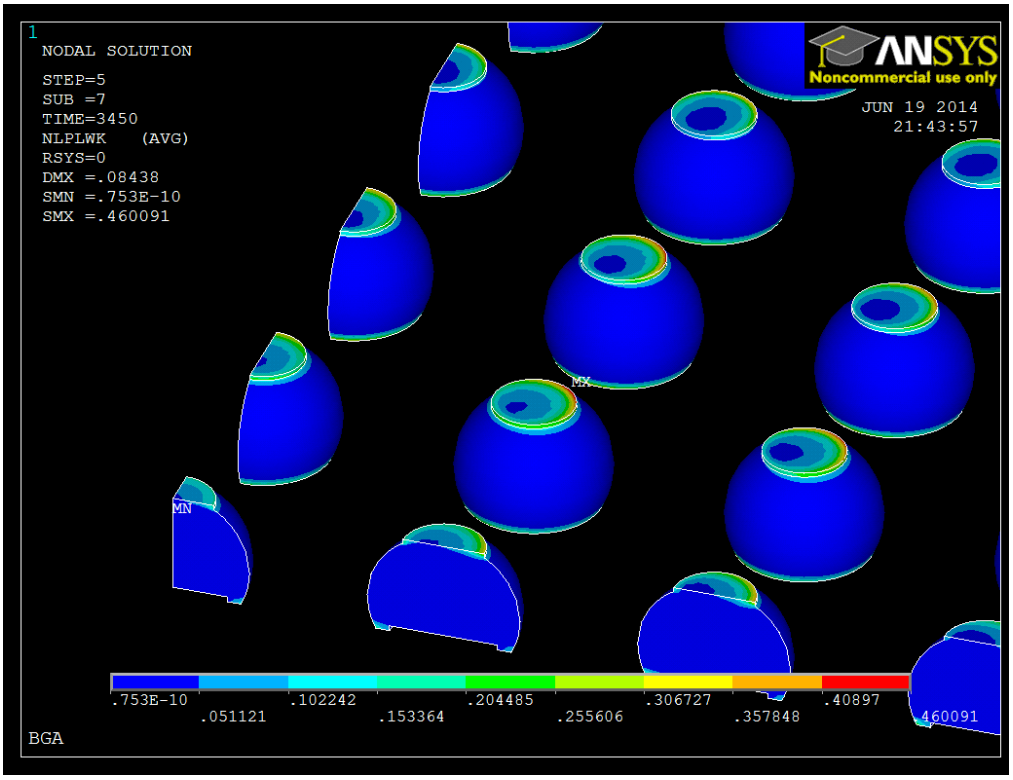


Figure 6-32: Zoom-in of maximal inelastic strain energy density contour of the solder balls of BGA225

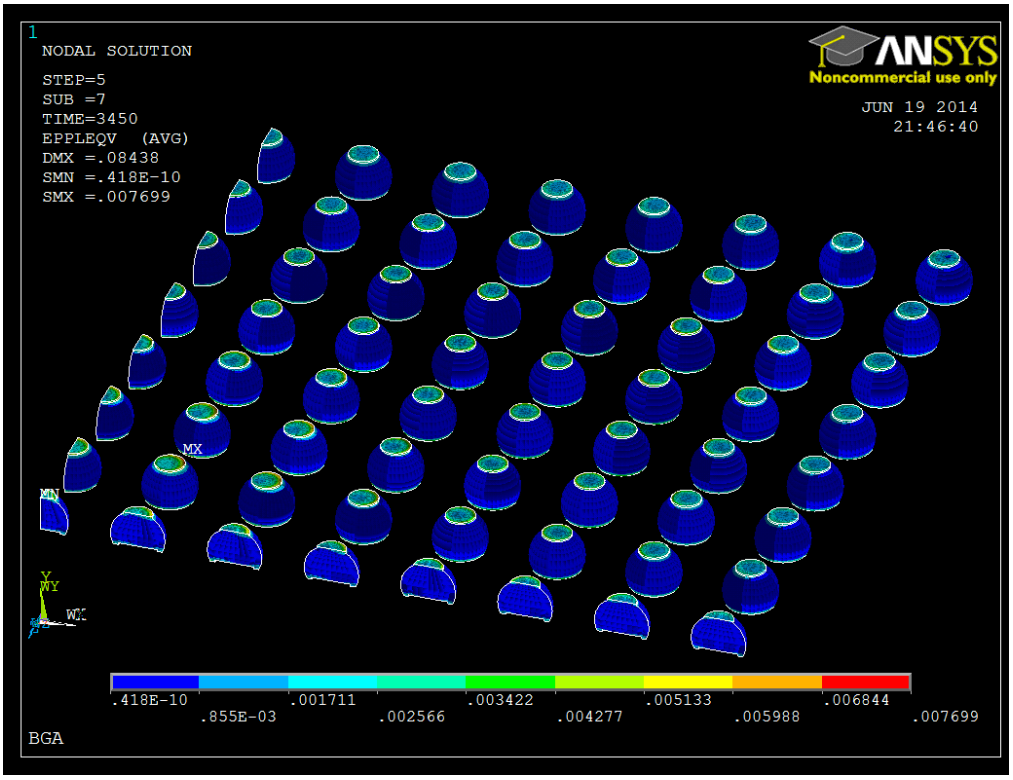


Figure 6-33: Effective plastic strain contour of the solder balls of BGA225

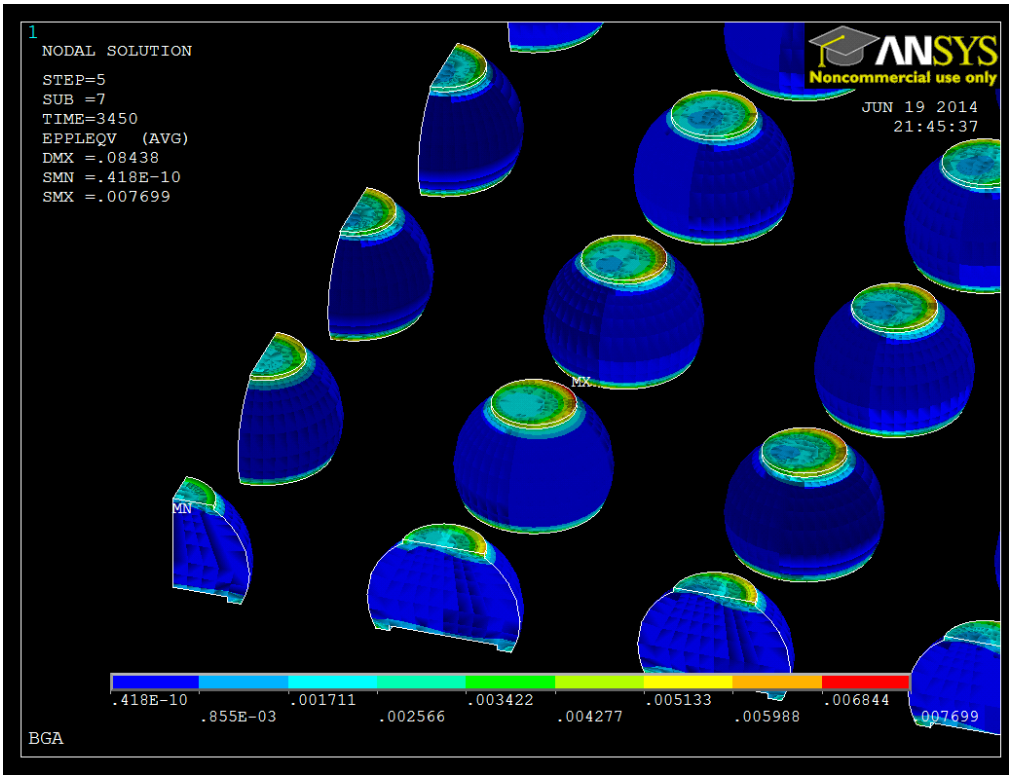


Figure 6-34: Zoom-in of maximal effective plastic strain contour of the solder balls of BGA225

6.2.2 LUI Evaluation of PBGA under Thermal cycling

In this section, the LUI system is used to evaluate the solder ball cracks caused during the thermal cycling. The test vehicles are the same as those in the evaluation of process-induced defects, as shown in Figure 5-4. A total of 4 PCBAs are involved in the evaluation. Therefore, there are 8 BGA169 chips and 8 BGA225 chips in total. Following the naming method shown in Table 5-2, these four PCBAs are referred to PCBA14~ PCBA17. The test vehicles are placed in a thermal cycling chamber that runs the temperature profile shown in Figure 6-26. The temperature profile is from -40°C

(minimum) to 125°C (maximum), with a 15-minute dwell time at each of the two temperature extremes. And the ramp time is 15 minutes. Therefore, each cycle takes 1 hour. This profile follows the JEDEC standard JESD22-A104-C under condition I. Before the thermal cycling test started, all the chips went through resistance measurement and LUI testing. The test results serve as comparison benchmarks, since the resistance and the LUI response are expected to change after the thermal cycling. The inspection patterns are the same as those in the evaluation of process-induced defects, as shown in Figure 5-8.

Ideally, the hybrid reference signals generated for the evaluation of process-induced defects will be also chosen for this reliability study because they are for the same test vehicles. Figure 6-35 shows the MCC results of PCBA14Chip1BGA169 and PCBA15Chip1BGA169 at 0 cycle with the hybrid reference signals from Chapter 5. As shown in the plot, the MCC values are fairly high, with some MCC values above the threshold defined in Chapter 5. The reason may be related to the material aging under room temperature. The study of process-induced defects was performed right after the test vehicles were built, while this reliability study started after two years. The material aging during the two years altered the whole chip structure, thus the LUI response, which leads the obvious difference from the hybrid reference signals. Therefore, the hybrid reference signals and the thresholds could not be used in the reliability test any more.

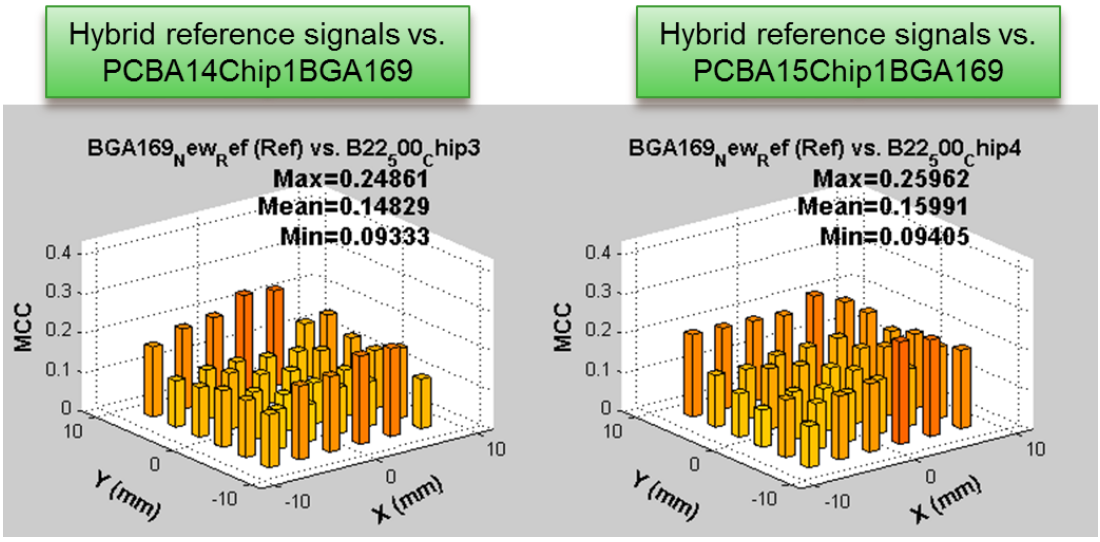


Figure 6-35: MCC results between the hybrid reference signals from Chapter 5 and PCBA14Chip1BGA169 and PCBA15Chip1BGA169 before any thermal cycling.

A compromise was adopted to produce reference signals and thresholds that can be used in this reliability study. Before the test vehicles were put into the thermal chamber, each chip was tested six times using the LUI system. For each chip, the signals from one of the six tests were randomly chosen as the reference signals for this specific chip. Next, the signals from the remaining five tests were correlated with the reference signals, thus generating five sets of MCC values. These five sets of MCC values quantify the test variation for this specific chip. The mean and standard deviation were extracted from these five sets of MCC values. The thresholds were calculated as the summation of the mean and triple standard deviation at each inspection point. In this way, each inspection point has its own unique threshold. Later, the LUI signals from the chips that have undergone the thermal cycling will be correlated to the reference signals. The MCC

values from the correlation will be compared to the thresholds for defect identification. There may be presence of a quality issue if the MCC value is larger than the threshold. Because it is very unlikely that an MCC value that will be larger than the 3-sigma control limit. Please note that there is only the test variation present rather than the manufacturing (chip-to-chip) variation, because each chip correlates with its initial state before thermal cycling. Therefore, the threshold obtained using this method will be much smaller than the threshold obtained in the process-induced defects because the manufacturing (chip-to-chip) variation was excluded. This implementation will also make the threshold very sensitive to the changes in the thermal cycling. An example is illustrated from Figure 6-36 to Figure 6-38. Figure 6-36 shows the LUI signals from six tests at IP #6 of PCBA14Chip1BGA169 before thermal cycling. The five MCC results are plotted in Figure 6-37 with the signal from the first test as reference. The threshold at IP #6 is also plotted in the same figure. Figure 6-38 shows the reference signal and the signal after the same chip is thermal-cycled at IP #6. The correlation result is then compared with the threshold to determine the quality of the solder balls near IP #6. The whole process repeats for all the inspection points.

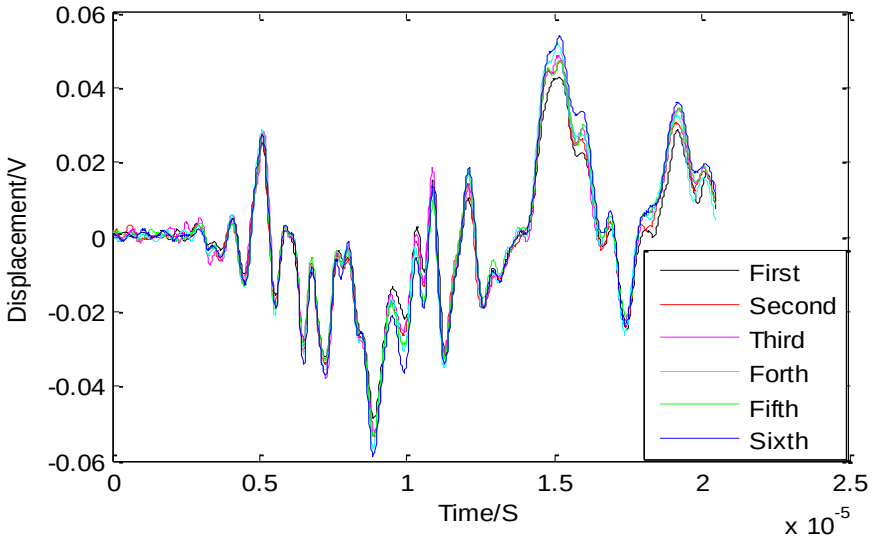


Figure 6-36: The LUI signals from six tests at IP #6 of PCBA14Chip1BGA169 before thermal cycling

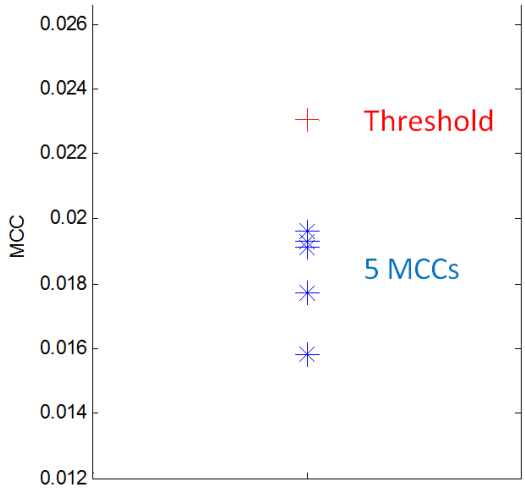


Figure 6-37: Five MCC results and the threshold for at IP #6

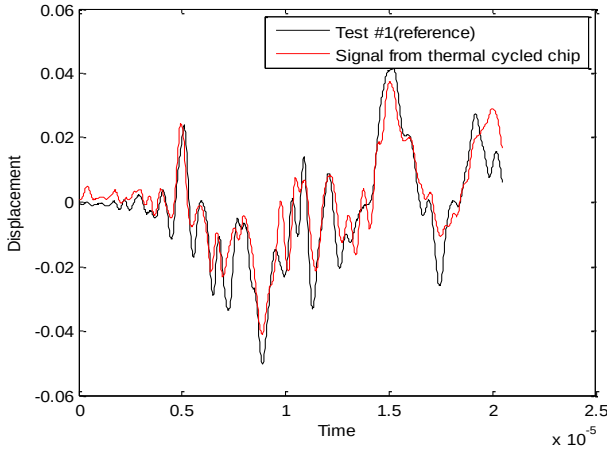


Figure 6-38: Reference signal and the signal after the same chip is thermal-cycled at IP #6

Figure 6-39 shows the five sets of MCC values and the associated thresholds at all 36 inspection points for PCBA15Chip1BGA169. As shown in the figure, the thresholds vary from inspection point to inspection point. The LUI signal from each inspection point has its unique features, such as frequency and amplitude, which leads to different MCC values. For example, the MCC values at IP #1 are relatively high, while the MCC values at IP #4 are fairly low. Figure 6-40 shows the five sets of MCC values and the thresholds at all 36 inspection points for another BGA169 chip, PCBA15Chip2BGA169. Coincidently, there is a peak at IP #1 and a trough at IP #4. The trend of the threshold is also very similar for both chips, and a strong correlation is present between the thresholds of both chips. This phenomenon can be explained by the inspection pattern. As shown in both figures, the threshold line is likely to have peaks at IP#1, #7, #13, #25, #30, #31 and #36. These inspection points are all located near the edge of the chip, far away from the

laser excitation point. The trough is likely to show up at IP#4, #10, #15, #21, #27 and #28. These inspection points are mostly located near the chip center, i.e. the laser excitation point. Due to signal attenuation, small signal amplitudes are likely to be present at inspection points that are far away from the laser excitation point. Given the same amount of noise at all inspections points, a smaller SNR is expected for the inspection points that are far away from the laser excitation point. Therefore, the MCC values tend to be higher. What's more, the ultrasonic waves will reflect and scatter when they propagate to the edge. The reflection and scattering waves will bring more uncertainties to signals, thus leading to larger MCC values. This phenomenon also justifies the necessity to set different thresholds at different inspection points.

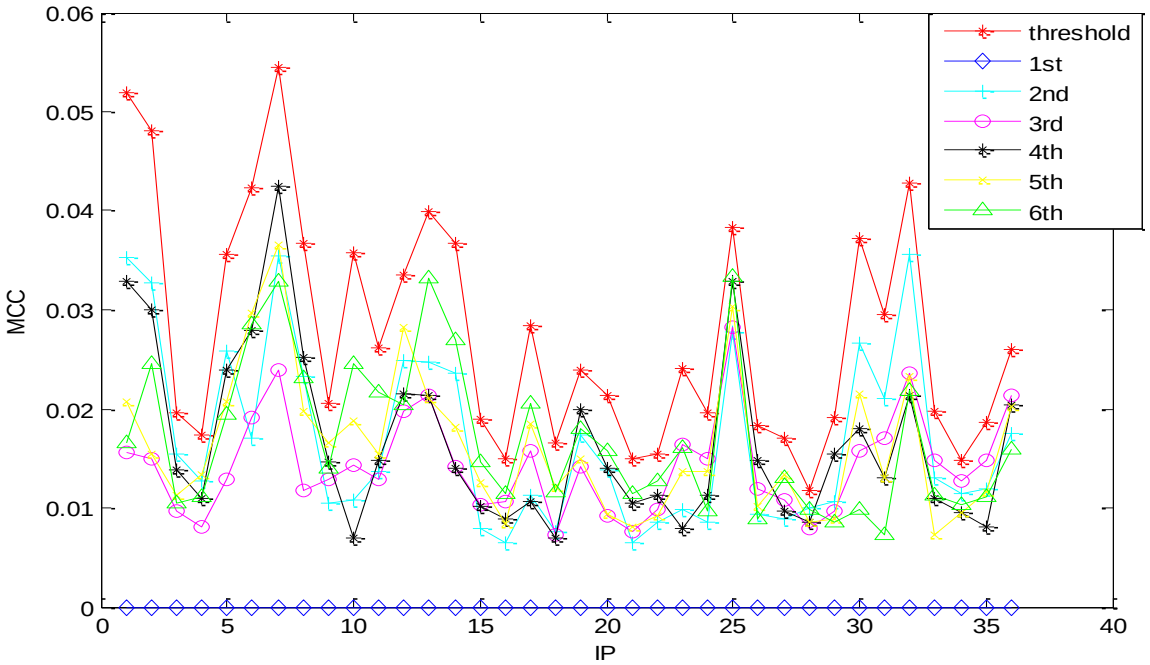


Figure 6-39: Five sets of MCC values and the associated thresholds at all 36 inspection points for PCBA15Chip1BGA169

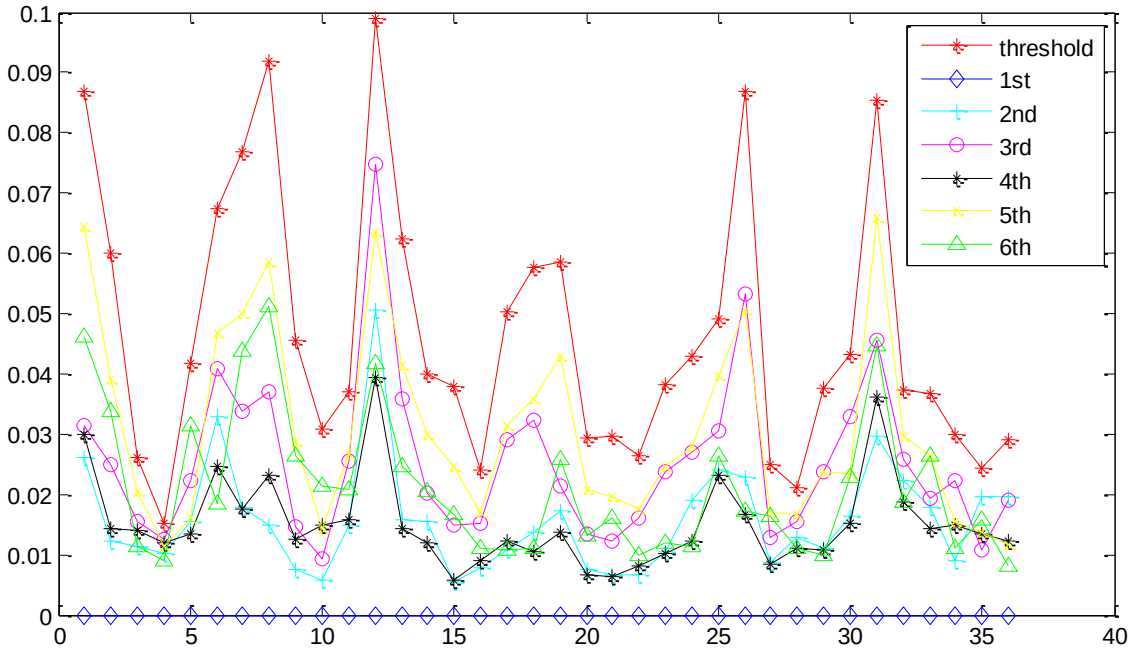


Figure 6-40: Five sets of MCC values and the associated thresholds at all 36 inspection points for PCBA15Chip2BGA169

The first objective of this study to try to identify the minimal solder ball crack length that the LUI system can capture. If the LUI system is capable of detecting the solder ball crack at an early stage, it will fill a huge gap in this research area. Numerous efforts have been spent to detect the solder ball cracks as early as possible, and different indicators have been developed to flag the solder ball cracks, such as RF impedance [90] and electrical resistance [91-93]. Among all these indicators, electrical resistance is the most popular. However, the electrical resistance is not sensitive to the early stages of interconnect degradation, such as a partial crack of a solder joint. Electrical resistance may overestimate chip lifetime and preclude the opportunity to conduct preventive maintenance, allowing the probability of severe damage to the system [90].

It often takes some time for the solder balls to initiate cracks under the thermal cycling. And we estimate that it takes 800 cycles before the solder ball crack initiates for the test vehicle we used. Before 800 cycles, the test vehicles were taken out from the thermal chamber for LUI and resistance tests every 400 cycles. After passing 800 cycles, a smaller interval, 50 cycles, was selected in case we overestimated the minimal detectable solder ball crack length. Figure 6-41 shows the MCC values for PCBA15Chip1BGA169 until 1200 cycles, as well as the thresholds at all the inspection points. Before 1200 cycles, all the MCC values were below the thresholds, which implies that the fluctuation of the MCC values can be attributed by the 3-sigma test variation. However, at 1200 cycle, the MCC values were above the thresholds. This can only be attributed to certain structural change of test vehicles rather than to test variation. Figure 6-42 shows the MCC results in 3D bar format with the mean of the MCC values available. As shown in the figure, there is a sharp jump in the mean of MCC values at 1200 cycle.

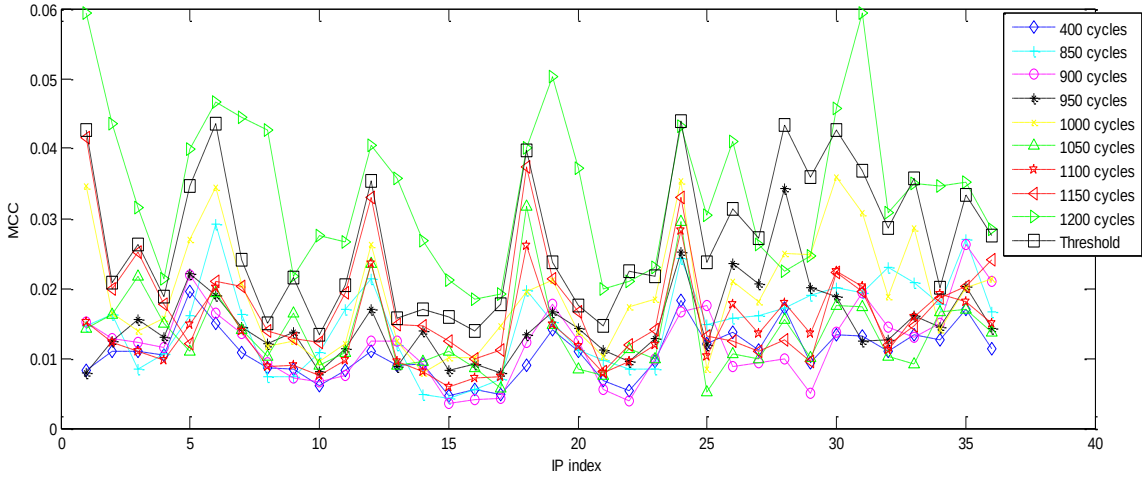


Figure 6-41: MCC values for PCBA15Chip1BGA169 until 1200 cycles, as well as the thresholds at all the inspection points

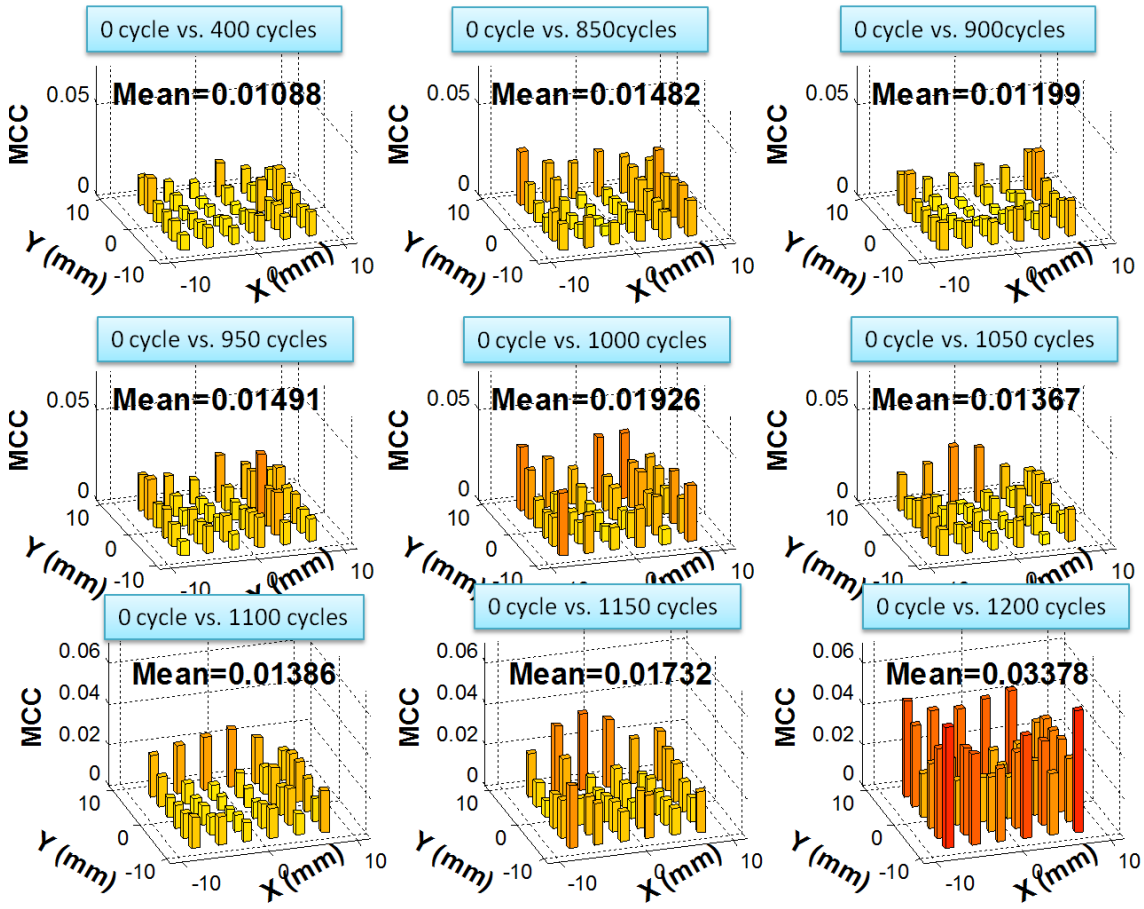


Figure 6-42: MCC results of PCBA15Chip1BGA169 in 3D bar format

The MCC results for PCBA15Chip2BGA169 are plotted in Figure 6-43. As shown in the figure, several MCC values begin to surpass the thresholds at 1050 cycles, and more MCC values become larger than the thresholds at 1100 cycles. For all the BGA169 test vehicles, the first time that there are MCC values above the thresholds ranges from 1050~1200 cycles. Based on the simulation results, the solder ball crack should initiate at the die corner first because of the largest CTE mismatch. Assuming that the solder ball crack initiation is the root cause for the MCC value to raise above the threshold, inspection points located on or near the die corner should be above the threshold first while other inspection points should be still below threshold. Based on the inspection pattern shown in Figure 5-8, MCC values at IPs #15, #16, #21 and #22 should surpass the thresholds first, while the rest of the inspection points should stay below their thresholds. However, both Figure 6-41 and Figure 6-43 show that the MCC values at most IPs are still above thresholds. This seems to imply the presence of certain non-localized effects that introduces changes to the whole structure. Material property change during the thermal cycling is one possible reason.

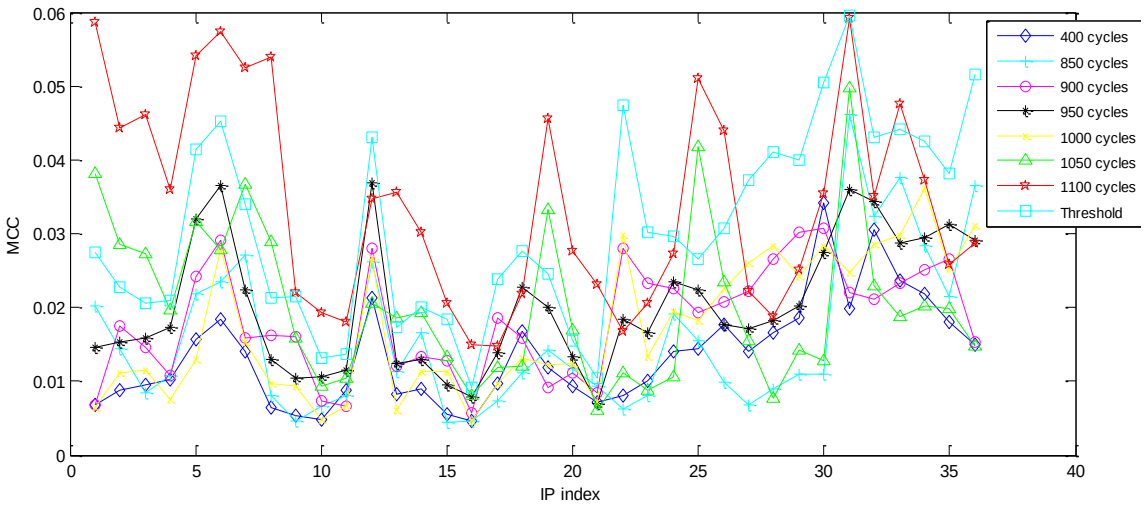


Figure 6-43: MCC results for PCBA15Chip2BGA169

The time domain signals at IP#1, #8 and #15 of PCBA15Chip1BGA169 before the thermal cycling and at 1200 cycles are displayed in Figure 6-44. First, a phase shift is observed at all three inspection points. What's more, the phase shift polarity is consistent regarding shift direction. Signals at 1200 cycles always lag compared to signals at the initial condition. The magnitude of the phase shift tends to increase as the inspection points move away from the laser excitation point. The phase shift at IP #15 is so small that it has to be zoomed in to be seen because IP #15 is very close to the laser excitation point. The larger distance between the laser excitation point and the inspection point, the larger the MCC values, as shown in Figure 6-44. It can be concluded that the phase shift in the time-domain signal results in the increase of the MCC values. Similar lagging phase shifts are also found in other chips after the thermal cycling.

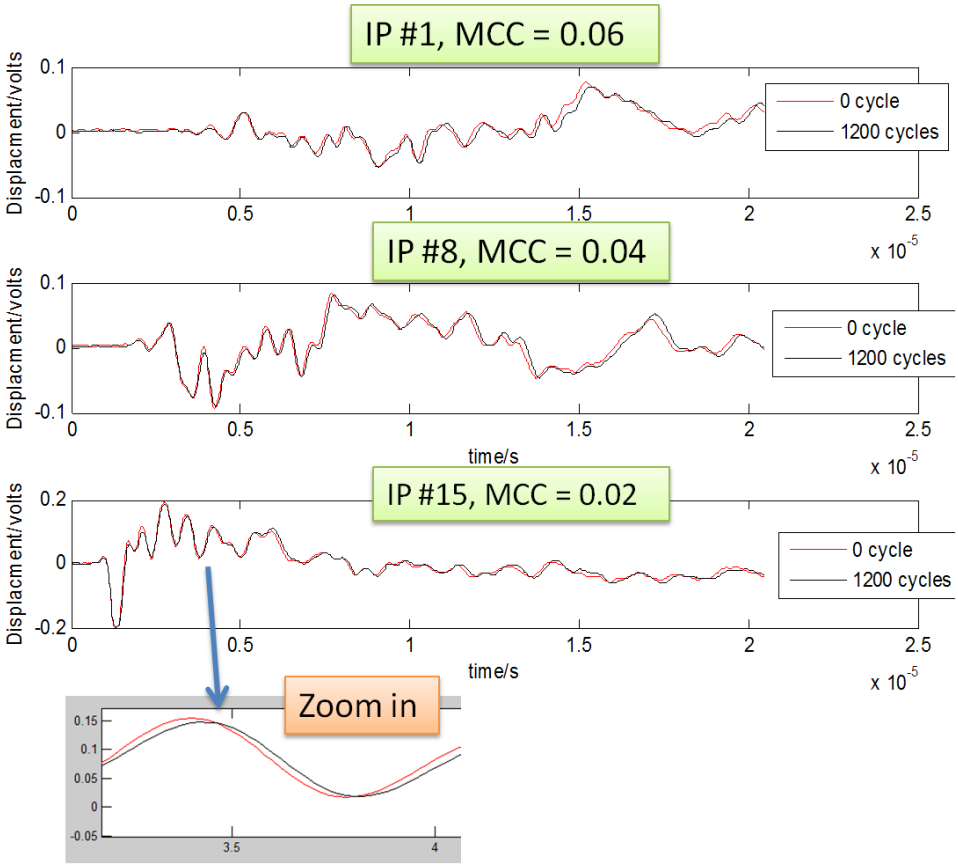


Figure 6-44: Time domain signals of IP#1, #8 and #15 of PCBA15Chip2BGA169 at 0 cycle and at 1200 cycles

The lagging phase shift indicates that the laser-ultrasound waves travel slower and are captured later after thermal cycling. This is because the laser-ultrasound waves initiate on the surface of the PBGA chips and also propagate through the surface of the PBGA chip, which is made of the molding compound. Changes in the molding compound properties may possibly be attributed to the lagging phase shift. In addition, Figure 6-45 shows the result of dynamic mechanical analysis (DMA) on the molding compound. The glass transition temperature is around 125°C, where there is a sharp drop on the storage modulus. Compared to the highest temperature in the thermal cycling,

140°C, the glass transition temperature of the molding compound is relatively low. And it is very likely that certain material properties of the molding compound change during thermal cycling.

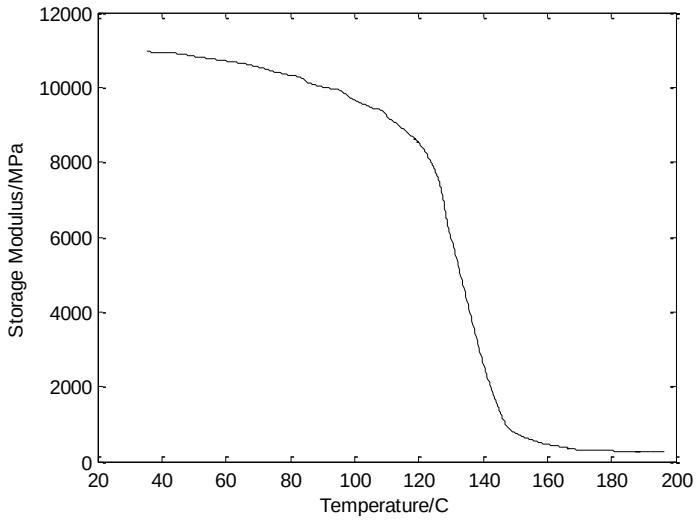


Figure 6-45: Test result of dynamic mechanical analysis (DMA) on the molding compound

Figure 6-46 plots the time domain signals of IP#2 of PCBA17Chip1BGA169 at 0, 800, 1200, 1600 and 2000 cycles. The phase shift increases until 1200 cycles. However, at 1600 cycles and 2000 cycles, the increase of the phase shift discontinues. Figure 6-47 shows 3D MCC plots for these cycles, which shows the increase of MCC values as the thermal cycling continues in spite of the stable phase shift after 1200 cycles. Based on the previous assumption that the phase shift is related to the material property change during the thermal cycling, we can assume that the change of the material property discontinues

after 1600 cycles. In addition, the increase of MCC values after 1200 cycles cannot be attributed to the phase shift anymore. Solder ball cracking becomes the most possible source of the increase of MCC. However, all these assumptions and analysis need to be validated by material characterization.

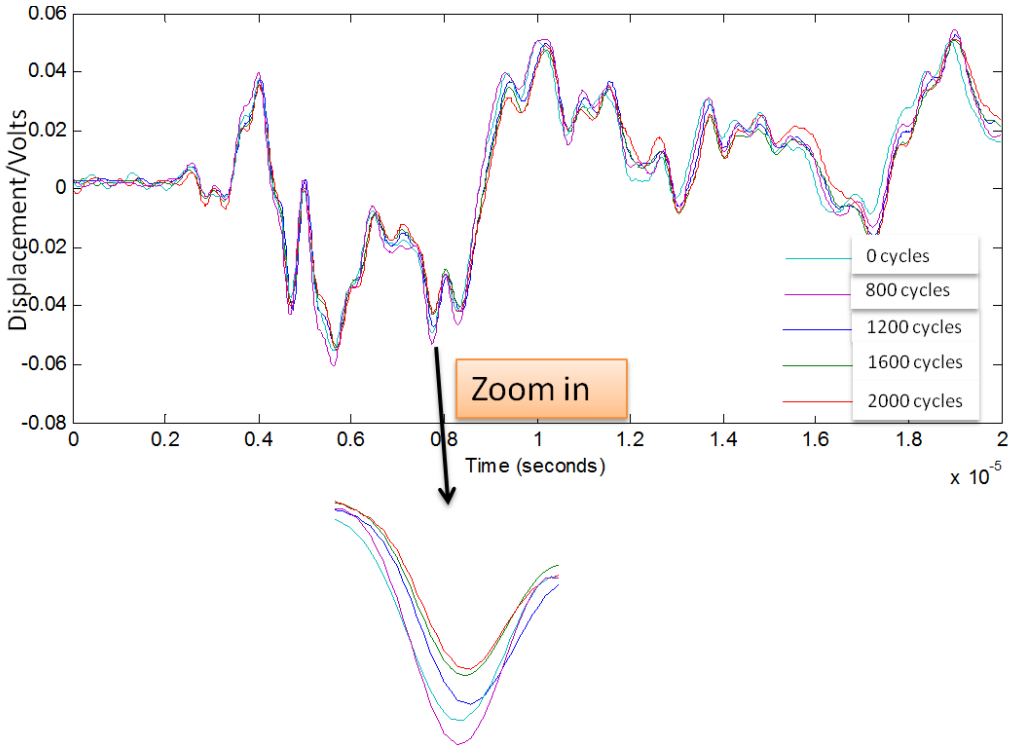


Figure 6-46: Time domain signals of IP#2 of PCBA17Chip1BGA169 at 0, 800, 1200, 1600 and 2000 cycles

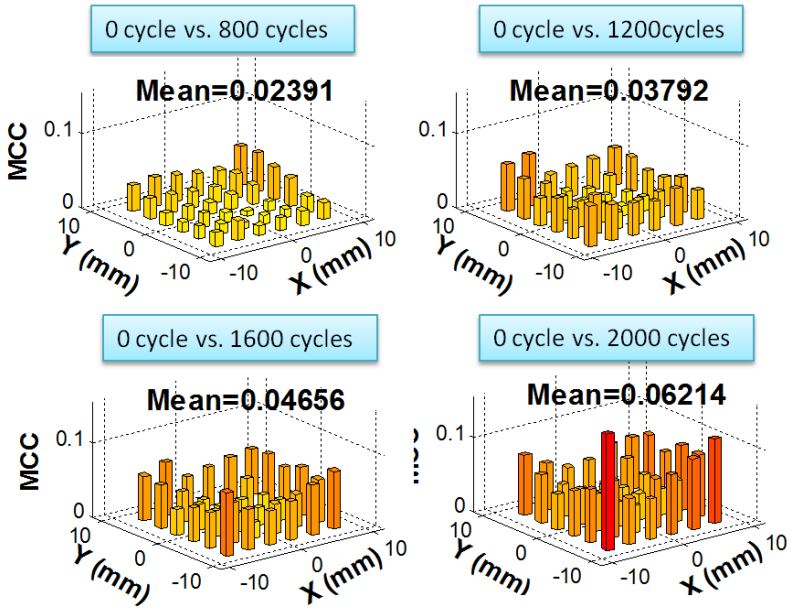


Figure 6-47: 3D MCC plots of PCBA17Chip1BGA169 at 800, 1200, 1600 and 2000 cycles

6.2.3 Material Characterization

When a wave travels through a medium, the wave speed is determined by the material properties of the medium, specifically the elastic properties and the density. The relationship is shown in Equation 6.4, where C_{ij} is the elastic properties and ρ is the density. Since the molding compound is an isotropic material, the C_{ij} is proportional to the Young's modulus. Therefore, material characterization needs to be focused on the molding compound. To be more specific, the Young's modulus and density have to be measured and compared at different cycles.

$$v = \sqrt{\frac{C_{ij}}{\rho}} \tag{6.4}$$

Tensile testing is the most common method to measure the Young's modulus. In a tensile test, the stress and strain are measured then the Young's modulus is directly obtained from stress divided by strain. The material samples need to be in a dog bone shape in a tensile test. However, there is no bulk molding compound available. The molding compound available is only from the surface of the test vehicle. It is very thin and small, which is not suitable for the tensile test at all. Nanoindentation is a popular material characterization method that can be used to measure the Young's modulus of a material with irregular shape. In a nanoindentation test, a hard tip whose mechanical properties are known is pressed into sample whose properties are unknown. While indenting, various parameters such as load and depth of penetration can be measured and plotted to create a load-displacement curve. The Young's modulus of the material under test can be calculated with the material properties of the indentation tip and the slope of the curve.

The molding compound samples were carefully removed from the PBGA chips at different cycles. Figure 6-48 shows how the indentation samples look. Because the removal of the molding compound is destructive to the chip, the chip cannot be put back into the thermal chamber after this. This limits the number of samples available for material characterization. The molding compound at 5 different cycles：0，800，1200，1600 and 2000 cycles was used for the test. For each cycle, there are 2 pieces of molding

compound samples, with 3 nanoindentation points on each sample. Therefore, a total of 6 data points can be obtained at each cycle.

Figure 6-48: Molding compound sample for nanoindentation

As shown in Figure 6-49, the nanoindentation tool from Hysitron was used in the test. During the test, the samples were put into the chamber of the nanoindentation tool and a Berkovich tip was used to indent the molding compound surface. Figure 6-50 shows a screenshot of the loading and unloading curve during testing. The software on the tool would calculate the Young's modulus based on the curve, as shown in Figure 6-50.

Figure 6-49: Nanoindentation tool from Hysitron

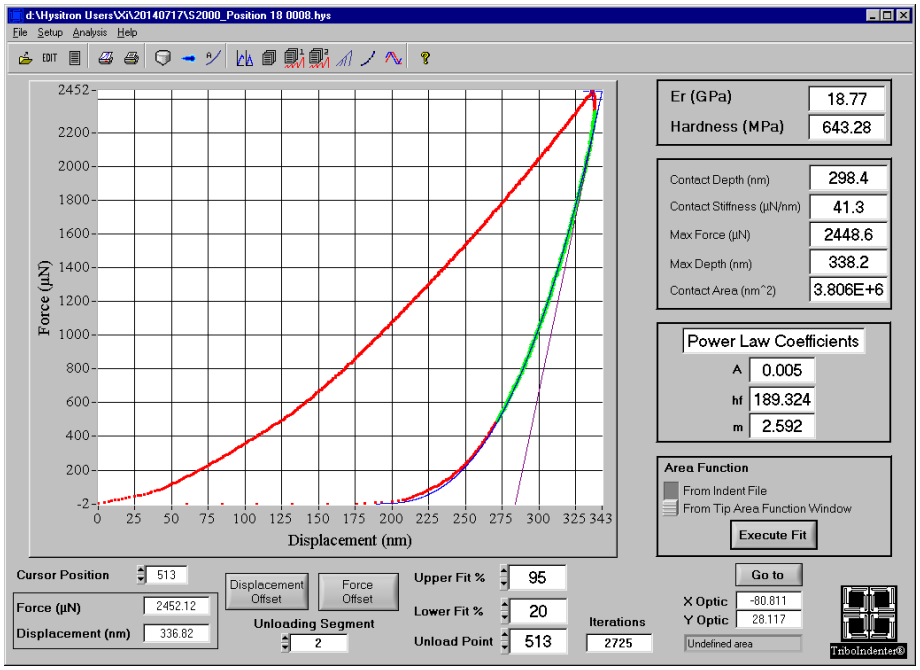


Figure 6-50: Screenshot of the loading and unloading curve during testing

Figure 6-51 shows the box plot of the Young's modulus of the molding compound measured from the nanoidentation test. As shown in the plot, the Young's modulus of the molding compound follows a decreasing trend from 0 cycle to 1200 cycles. But after

1200 cycles, the trend doesn't last any more, and the Young's modulus becomes fairly stable.

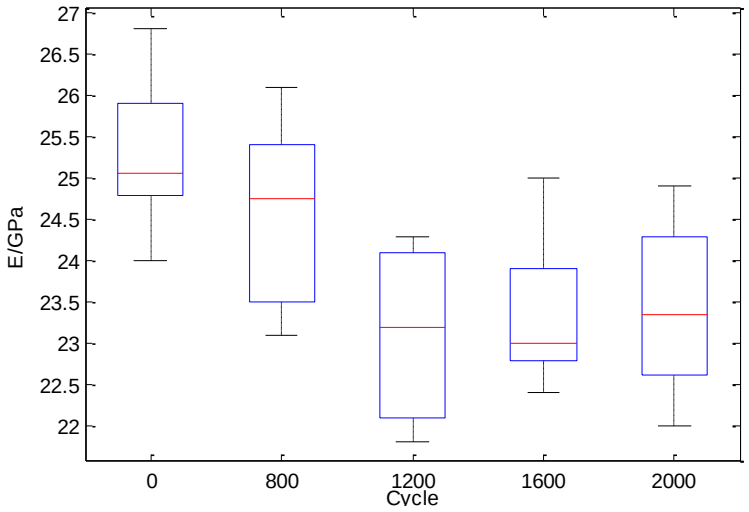


Figure 6-51: Box plot of the Young's modulus of the molding compound

Another factor affecting the wave speed is density. The density measurement is straightforward. The mass was measured by a scale with precision of 0.0001 gram. And the volume was measured by the setup shown in Figure 6-52. A cup with deionized water is put on the scale. Then the mold compound sample is hung by a wire and fully immersed in the deionized water. Because the density of the deionized water equals 1 g/mm^3, the sample volume equals the mass difference before and after the immersion of the sample. With both mass and volume available, the density is calculated by mass divided by volume. The same pieces of molding compound samples used in the nanoindentation test were used in the density measurement. Since there were only two

pieces of samples at each cycle, the density of each piece was measured five times to reduce the random error. The average density for each piece is extracted and plotted in Figure 6-53. No obvious trend can be observed. Therefore, we can conclude that the density of molding compound during thermal cycling remains the same.

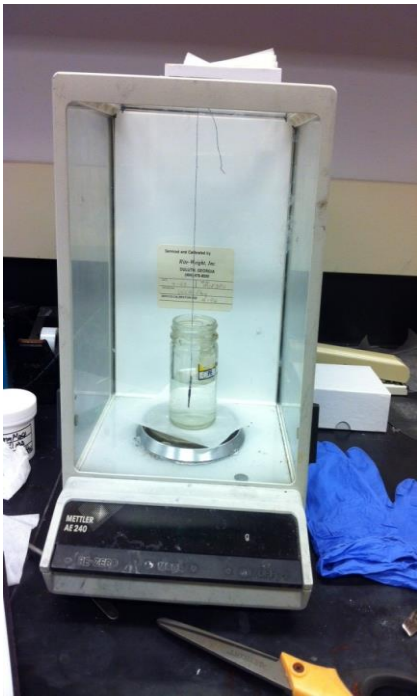


Figure 6-52: Experimental setup for density measurement

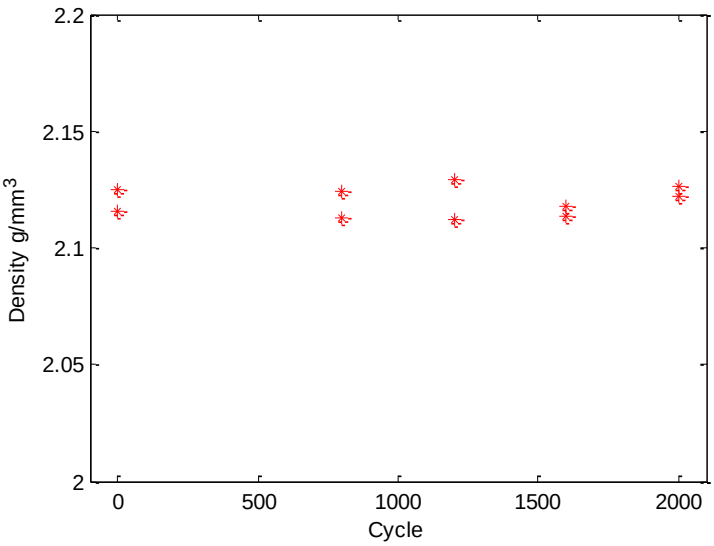


Figure 6-53: Density measurement results

The reduction of the Young's modulus of the molding compound can be explained by the internal thermomechanical degradation during thermal cycling. Molding compound is made of highly filled epoxy, and silica is usually the filler. Silica is an inorganic material with a small CTE. Epoxy is an organic material with a large CTE. The CTE of epoxy (around 55 ppm/°C) is about 100 times of CTE of silica (around 0.55 ppm/°C). A huge CTE mismatch is present. During thermal cycling, the molding compound is subject to cyclic expansion and contraction. Overtime, the bonding between silica and epoxy gets looser and looser. In addition, the internal movements of silica and epoxy get intensified when the temperature of the thermal cycling reaches above the glass transition temperature of the molding compound, i.e. 125°C. The polymer becomes soft after reaching glass transition temperature. Both factors will change the internal grains and grain boundaries of the molding compound, resulting in the reduction of the Young's

modulus. As the thermal cycling continues, the previous change reaches an equilibrium state and the Young's modulus now becomes stable. This validates the results from the LUI testing, which shows that the increase of the phase shift stopped after 1200 cycles. Based on the LUI signals, the time when the material property changes discontinue should be between 1200 cycles and 1600 cycles.

Based on Equation 6.5, the reduction of the Young's modulus till 1600 cycles with stable density results in the decrease of the wave speed. This will introduce the lagging phase shift whose magnitude is time-independent for the LUI signals at a specific cycle. However, as shown in Figure 6-44, this is not the case. The magnitude of the lagging phase shift tends to increase over time. Therefore, the time-dependent lagging phase shift cannot be fully attributed to the decrease of the wave speed. There are some other factors. One possible reason can be the effects of material properties changes on the package structure. The laser-generation ultrasound signal can be decomposed into two parts: wave propagation and structural vibration. The decrease of the wave speed only changes the wave propagation part in the LUI signal. The structural vibration response is similar to an impulse response because the laser pulse can be viewed as an impulse impact. The change of material properties of the molding compound definitely alters the whole package structure, such as stiffness and mass, thus changing the structural vibration response. In addition to the material property change, the solder ball crack will initiate

and then propagate during thermal cycling, which is another factor contributing to the change of the whole package structure.

Overall, it becomes very difficult to investigate how the initiation and propagation of solder ball crack during thermal cycling affect the LUI signals because the change of the material properties adds a new variable to the experiment. Due to the limited number of the test vehicles, only a preliminary and qualitative test was carried out in this thesis work.

6.2.4 Cross-Section Results

Cross-sectioning is also performed on these chips. First, one BGA169 chip and one BGA225 chip from PCBA14 were cross-sectioned after 800 cycles. Very tiny cracks were found at the solder balls near the die corner while other solder balls were still intact. Figure 6-54 and Figure 6-55 show an example of the tiny solder ball crack and the intact solder ball respectively. As shown in Figure 6-54, the tiny solder ball crack is located on the component side. The MCC values stay below the thresholds for all the chips. This means that the initiation of such a tiny crack is below the resolution of the LUI system regardless of the presence of the material properties change.

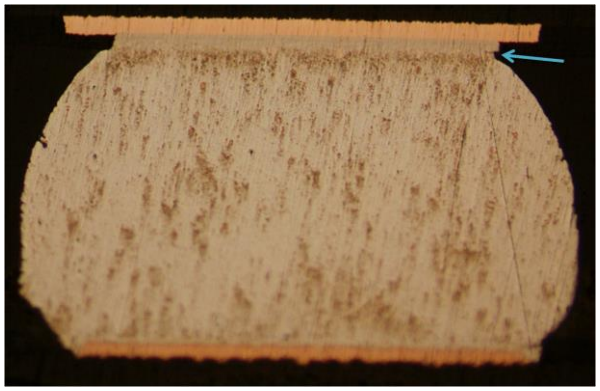


Figure 6-54: Tiny solder ball crack at the die corner at 800 cycles

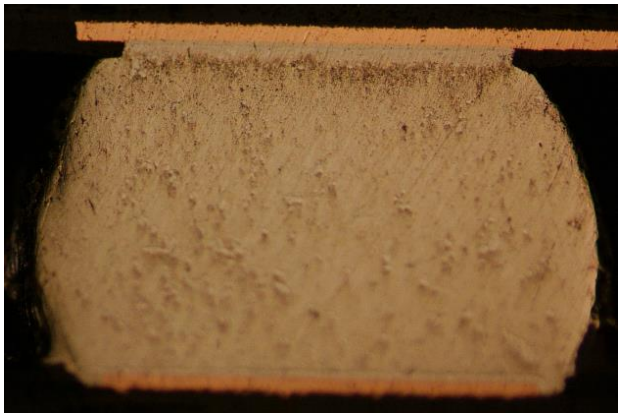


Figure 6-55: Intact solder ball at 800 cycles

At 1200 cycles, one BGA169 chip and one BGA225 chip from PCBA15 after 1200 cycles were cross-sectioned. Some small solder ball cracks were observed near the die corner, as shown in Figure 6-56. The crack length at 1200 cycles is larger than found at 800 cycles.

Figure 6-56: Solder ball cracks at the die corner at 1200 cycles

Figure 6-57 shows the cross-sectioning images of two critical solder balls from chips on PCBA16 at 1600 cycles. As shown in the figure, the cracks propagated further compared to cracks at 800 cycles and 1200 cycles. However, the electrical resistance in all daisy chains still didn't change at 1600 cycles.

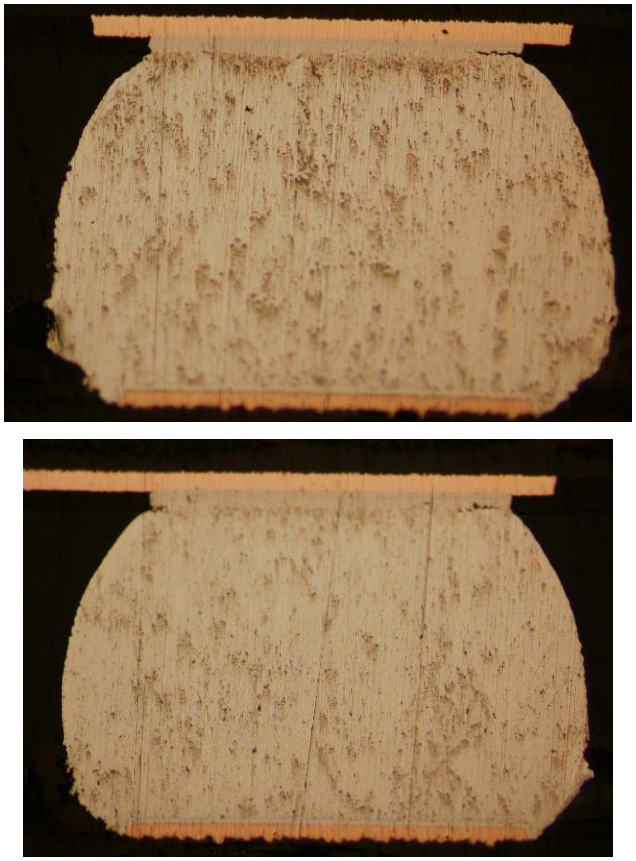


Figure 6-57: Solder ball cracks at the die corner at 1600 cycles

Figure 6-58 shows the cross-sectioning images of two critical solder balls chips on PCBA17 at 2000 cycles. Longer cracks were present, and they almost accounted for one third of the solder diameter. However, the electrical resistance still remained the same as that of 0 cycle.

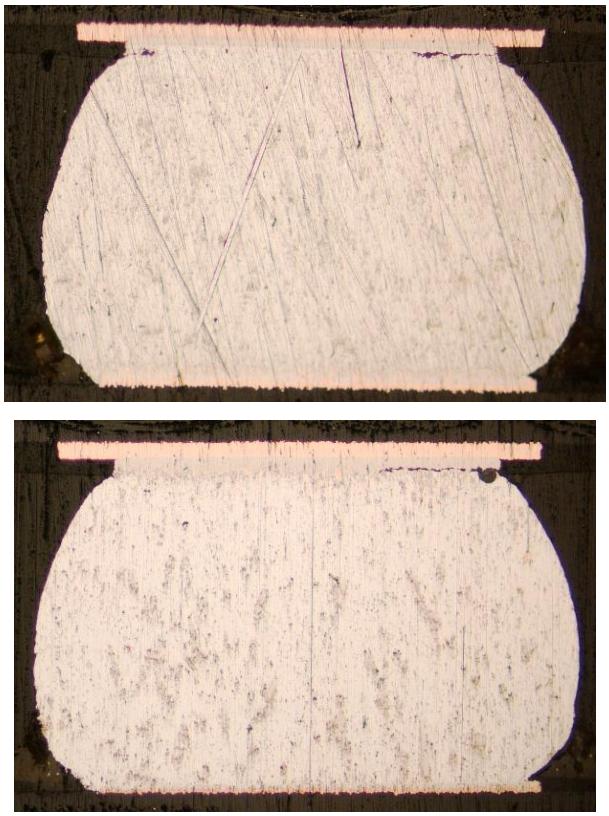


Figure 6-58: Solder ball cracks at the die corner at 1600 cycles

The cross-sectioning results validate the finite element simulation results that the critical solder ball is located at the die corner. However, it is difficult to tell whether the solder ball cracks caused by the thermal cycling contributed to the change of the LUI signals due to the presence of the material property change in the molding compound. The electrical resistance didn't change at all, even though the solder ball cracks had propagated to one third of the solder diameter at 2000 cycles. This demonstrates that the electrical resistance is a lagging indicator for monitoring solder ball crack.

6.3 Chapter Summary

In this chapter, the LUI system was applied to investigate displacement and temperature related solder ball fatigue. In the study of displacement related solder ball fatigue, a FCBGA package went through a mechanical bending test. The failure modes mainly included pad cratering and brittle intermetallic cracks with different levels of severity. 3D X-ray analysis showed limited capability for inspecting such kinds of failure modes. The LUI system not only captures the general trend of chip quality by using the MCC comparison and signal energy, but also reveals local defect severity by using a MCC color map. By assigning a severity index to each individual solder ball, the cross-section results were quantified. A strong correlation was found out between the cross-section results and the LUI results.

As for the temperature related accelerated life testing, 2 types of PBGA packages were put into the thermal chamber to go through the temperature cycle. A thermo-mechanical finite element analysis was presented to support the experimental work. By locating the maximal effective plastic strain and inelastic strain energy density from the finite element simulation results, the critical solder ball was identified to be located at the shadow of the die corner that is the location of the largest CTE mismatch in the PBGA assembly.

In the experimental work, a lagging phase shift was observed in the LUI time-domain signals of the chips after the thermal cycling. The phase shift resulted in the increase of the MCC values, thus surpassing the threshold at 1200 cycles. And the phase

shift tends to be stable till 1600 cycles. It was assumed that the phase shift was related to the material property changes of the molding compound, because the lagging phase shift indicated that the laser-ultrasound waves travelled slower. And when a wave travels through a medium, the wave speed is determined by the material properties of the medium, specifically the elastic properties and the density. The Young's modulus and density of the molding compound was then measured to validate the assumption. The Young's modulus of the molding compound turned out to follow a decreasing trend from 0 to 1200 cycles. But after 1200 cycles, the trend did not last any more, and the Young's modulus became stable. The density of the molding compound is very stable throughout all the cycles. This finding validated the assumption.

The cross-sectioning results validate the finite element simulation results showing the critical solder ball is located at the die corner. However, it is difficult to tell whether the solder ball cracks caused by the thermal cycling contributed to the change of the LUI signals due to the presence of the material property change of the molding compound. The electrical resistance didn't change at all even though the solder ball cracks have propagated to one third of the solder diameter at 2000 cycles. This demonstrates that the electrical resistance is a lagging indicator for monitoring solder ball cracks.

Overall, it becomes very difficult to investigate how the initiation and propagation of solder ball cracks during the thermal cycling affects LUI signals because the change of the material properties adds a new variable to the experiment. Due to the limited number

of test vehicles, only a preliminary and qualitative test was carried out in this thesis work. A thorough investigation of the material property changes on the bulk molding compound during the thermal cycling needs to be completed to support the further study.

Chapter 7 CONCLUSION

The achievement of the research objectives has enabled the laser ultrasound inspection system to inspect a broader range of solder ball defects in a variety of electronic packages. The performance of this system has been improved through system hardware upgrading and software integration. The development of the Hybrid Reference Method adds more flexibility and robustness to the inspection system. The investigation of BGA packages is the first time that the LUI system has been applied to inspect the quality of BGA packages. Both process-induced and service-induced solder ball defects were inspected. The experimental work as well as the simulation work characterized the performance of the laser ultrasound inspection system on BGA applications. In this chapter, a summary of the unique contributions made in this dissertation and the scope for future research is given.

7.1 Summary of Unique Contributions

The unique contributions made in this dissertation are as follows.

(a) A GUI was developed to fully integrate and automate different modules. Before the development of the GUI, the operator needed to switch between various control interfaces to access each sub-system, such as stage motion, data acquisition and laser

firing. The new process permits the integration of different sub-systems into a single interface. As a result, the system performance is greatly improved, it is more user-friendly, and it permits higher throughputs and better repeatability.

(b) The successful development of the Hybrid Reference Method (HRM) significantly improved the flexibility and robustness of the inspection system. Before the Hybrid Reference Method was introduced, a reference chip was required to set up a benchmark for comparison. The costs associated with the extensive and expensive testing to look for a known-good chip are fairly high. It is not convincing that the potential customers need to buy other non-destructive solder ball inspection tools like X-Ray tools to generate reference chips before the LUI system can be used. The HRM solves this problem and reduces such costs, which enables extension of the application scope of the system. Furthermore, the use of the virtual hybrid reference, instead of a single known-good chip, takes the chip-to-chip variations into consideration, which improves the measurement accuracy.

(c) The construction of the pass/fail threshold was proposed to separate the good and bad chips from a statistical perspective, whereas previous analysis usually lacked such a specific or pre-defined threshold. What's more, each inspection point now has its own threshold so we can clearly see which inspection points are above the threshold and

which are below. The location of the inspection points usually corresponds to the solder ball location. Therefore, the failure site can be identified based on which inspection points are above the threshold. The combination of the Hybrid Reference Method and a pass/fail threshold make this inspection system more robust and productive.

(d) The quality inspection on BGA packages is the first time that the LUI system was applied to inspect the quality of BGA packages. Since BGA packages have a large market share in the microelectronic industry, the success of the work opened a totally new application scope for this non-destructive inspection technique.

First, two types of process-induced defects including poor-wetting and solder ball voids were investigated. The successful creation of poor wetting and voids in the solder balls provides a means for the artificial creation of defects. In addition, other solder ball evaluation methods including X-Ray, SAM, electrical testing and cross-sectioning were also carried out for both types of process-induced defects. A comprehensive comparison between different solder ball evaluation methods was presented, which provides guidance on how to choose the best solder ball evaluation method for different process-induced defects.

Then, two service-induced defects were fully studied including displacement and temperature related fatigue. In the displacement related accelerated life testing, a FCBGA package went through mechanical bending. The failure modes mainly included pad

cratering and brittle intermetallic cracks with different levels of severity. The LUI system not only captured the general trend of chip quality by using MCC comparison and signal energy, but also revealed local defect severity by using a MCC color map. The LUI inspection showed superiority over 3D X-ray. What's more, the LUI results had a good correlation with the cross-section results that were quantified by assigning a severity index. This is also the first time that the LUI system was used to inspect solder balls that underwent displacement related accelerated life testing This successful application helps to expand its range of applications.

In the temperature related accelerated life testing, 2 types of PBGA packages were put into the thermal chamber to go through the temperature cycle. A lagging phase shift was observed in the LUI time-domain signals of the chips after the thermal cycling. The phase shift resulted in an increase of the MCC values, surpassing the threshold at 1200 cycles. And the phase shift tended to be stable at 1600 cycles. The lagging phase shift indicated that the laser-ultrasound waves travelled slower. When a wave travels through a medium, the wave speed is determined by the material properties of the medium, specifically the elastic properties and the density of the medium. Material property changes are expected during the thermal cycling.

In the material characterization, the Young's modulus of the molding compound turns out to follow a decreasing trend from 0 cycle to 1200 cycles. But after 1200 cycles, the trend disappears, and the Young's modulus becomes stable. The density of the

molding compound is very stable throughout all the cycles. This finding matches with the observation in the LUI signals.

The cross-sectioning results validate the finite element simulation results, which showed that the critical solder ball is located at the die corner. However, it is difficult to tell whether the solder ball cracks caused by the thermal cycling contributed to the change of the LUI signals due to the presence of the material property change of the molding compound. The electrical resistance doesn't change at all even though the solder ball cracks had propagated to one third of the solder diameter at 2000 cycles. This demonstrates that the electrical resistance is a lagging indicator for monitoring solder ball crack.

Overall, it becomes very difficult to investigate how the initiation and propagation of solder ball crack during thermal cycling affects LUI signals, because the change of the material properties adds a new variable to the experiment. Due to the limited number of test vehicles, only a preliminary and qualitative test was carried out. A thorough investigation of the impact that material properties changes have on the bulk molding compound during the thermal cycling must be completed to as part of the further study.

(e) A finite element model was developed to study the thermo-mechanical reliability of solder balls in PBGA packages under cyclic thermal loads. The viscoplastic constitutive law was integrated into the model to represent the inelastic stress/strain

behavior of lead-free solder. The effective plastic strain and inelastic strain energy density were extracted from the simulation as damage metrics. Both damage metrics showed that the critical region is located on the top layer of the solder ball under the die corner shadow at the component side. This can be well explained by the CTE mismatch in PBGA packages. What's more important, this result matched cross-section observations of solder ball cracks.

7.2 Scope for Future Research

In order to improve the current inspection system and expand the application, there is a tremendous scope for pursuing further research. Some potential directions for future research are presented in this section.

7.2.1 Multiple Pulsed Laser Excitation Points

In the current system setup, there is only one laser excitation point, which set a cap on the system performance in various ways. First, the energy that is available to excite the chip is limited under the current setup. To prevent chip surface damage, the laser energy has a cap. Limiting testing to one laser excitation point makes it worse. Multiple laser excitation points can address this issue. For example, we can have 4 laser excitation points at the center of the four quadrants of each wafer. The total excitation energy would

then quadruple, which would generate stronger LUI response. As the structure of the chip package is becoming more and more complicated, larger excitation energy is required to make sure that the response has enough signal amplitude and strength.

Secondly, multiple laser excitation points are likely to generate new vibration modes, especially high-frequency modes that are more sensitive to defects. The pulse laser excitation can be viewed as an impulse input. For a given structure, an impulse input can usually lead the impulse response only with the first several natural modes. Multiple impulse inputs at different locations of a structure are likely to generate new vibration modes, especially high-frequency modes that are more sensitive to defects.

One possible way to realize this configuration but without requiring big changes in the current setup is to use multiple fibers or to use a laser beam shaper.

7.2.2 Expansion of Application Scope

This dissertation has investigated solder ball quality under mechanical bending and thermal cycling, which are two most common sources of solder ball fatigue. The drop test is another common source of solder ball fatigue. Brittle fracture is the dominant failure mode under drop testing. The world is entering a mobile era with all these portable electronics and drop testing plays an important role in product characterization. If the

system can be used in reliability studies of the drop test, it will open a new application window.

Besides the evaluation of solder ball quality under drop tests, the current prototype system can also be used to detect the void in the underfill. Void in the underfill can cause reliability defects such as solder bridges and solder joint cracks possibly resulting in early failure in thermal reliability. Currently, only C-SAM has the ability to detect voids in the underfill [94]. In addition, the system can be expanded to 3D package inspection and characterization.

7.2.3 Signal Feature Extraction for Failure Mode Classification

Currently, the system is mainly used to differentiate good chips from bad chips, and also to identify the failure site sometimes. However, information related to the failure mode is not available. The information related to the failure mode is very important for defect root cause analysis. For example, solder ball voids may be related to possible moisture or contamination during reflow. The current available signal processing methods mainly focus on defect detection and only a very limited set of signal features is exacted for this purpose. For example, in the Modified Correlation Coefficient (MCC) method, only a linear correlation in the time-domain is extracted. Generally speaking, signal features regarding the frequency-domain are more closely related to the defect than to time-domain. Zhang observed the decrease of certain natural frequency caused by

solder ball crack. However, this is not enough for failure mode classification. The decrease of certain natural frequency can also be related to other failure modes, such as pad cratering. Therefore, more signal features need to be extracted to correlate with the failure modes. Fox example, the magnitude of the frequency shift can be used to separate pad cratering and solder ball crack. In addition, machine learning can be adopted to build a classification system when there is a large amount of data.

7.2.4 Multiphysics Simulation on Laser-Generated Ultrasound

In the current experimental setup, the laser pulse is usually excited at the center of the chip packages while the interferometer inspection positions are normally selected directly on solder balls. However, when the chip under test has hundreds or even thousands of solder balls, it is impossible to inspect all the solder balls. A down-sampling inspection pattern is necessary for the interest of throughput. The choice of the down-sampling inspection pattern is closely related to the inspection sensitivity. Certain inspection patterns are superior to others. Currently, the down-sampling inspection pattern is determined empirically. Multiphysics simulation can be adopted to provide guidance to optimize the inspection pattern. The simulation can be carried out numerically, i.e. using the finite element method. In the multiphysics model, the pulsed laser radiation needs to be modeled as a transient temperature distribution. Then the transient temperature distribution will produce a transient stress/strain field in the

electronic package, which will finally generate transient out-of-plane displacement responses on the chip surface. The simulation can bring huge robustness to the inspection system. By taking advantage of this model, we can predict the transient out-of-plane displacement responses even before running actual tests. We can change many variables in the model, including the laser energy, the location of laser excitation, inspection location and the chip package. The effects of multiple laser excitations can also be evaluated using this model. For example, the simulated LUI responses can be obtained for a defect-free chip in the model. If a solder ball crack is introduced at the corner of the chip, we can change the model accordingly and get the new simulated LUI responses. Different signal processing methods can be used to extract the defect features from these responses. What's more, the simulated LUI response can be picked up at different locations and it is likely that certain inspection locations are more sensitive to the defects. Meanwhile, the laser input can be simulated at different locations besides the center of the chip. Likewise, it is possible that certain laser excitation locations can be more sensitive to defects. In a word, the optimization of the laser excitation locations and interferometer inspection positions can be achieved using the model, which will provide great guidance to the actual tests.

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