AMORPHOUS METAL TUNGSTEN NITRIDE AND ITS APPLICATION FOR MICRO AND NANOELECTROMECHANICAL APPLICATIONS

Dissertation By
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ABSTRACT

Amorphous Metal Tungsten Nitride and its Application for Micro and Nano-ElectroMechanical Application

Abdulilah Mohammad Mayet

The Objective of this doctoral thesis is to develop, engineer and investigate an amorphous metal tungsten nitride (aWN_x) and to study its functionality for applications focused on electromechanical system at the nano-scale. Charge transport based solid state device oriented complementary metal oxide semiconductor (CMOS) electronics have reached a level where they are scaled down to nearly their fundamental limits regarding switching speed, off state power consumption and the on state power consumption due to the fundamental limitation of sub-threshold slope (SS) remains at 60 mV/dec. NEM switch theoretically and practically offers the steepest sub-threshold slope and practically has shown zero static power consumption due to their physical isolation originated from the nature of their mechanical operation. Fundamental challenges remain with NEM switches in context of their performance and reliability: (i) necessity of lower pull-in voltage comparable to CMOS technology; (ii) operation in ambient/air; (iii) increased ON current and decreased ON resistance; (iv) scaling of devices and improved mechanical and electrical contacts; and (v) high endurance. The *"perfect"* NEM switch should overcome all the above-mentioned challenges. Here, we show such a NEM switch fabricated with aWN_x to show (i) sub-0.3-volt operation; (ii) operation in air and vacuum; (iii) ON current as high as 0.5 mA and ON resistance lower than 5 kΩ; (iv) improved

mechanical contact; and the most importantly (v) continuous switching of 8 trillion cycles for more than 10 days with the highest switching speed is 30 nanosecond without hysteresis.

In addition, tungsten nitride could be the modern life vine by fulfilling the demand of biodegradable material for sustainable life regime. Transient electronics is a form of biodegradable electronics as it is physically disappearing totally or partially after performing the required function. The fabricated aWN_x suites this category very well, despite not being a universal bio-element. It has been found that aWN_x dissolves in ground water with a rate of ≈ 20-60 nm h^{-1}. This means that a 100 nm thick aWN_x disappears in ground water in less than a day and three days are enough to dissolve completely a 300 nm thickness device.

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Dedicated to my lovely family

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
ANIC	Advanced Nanofabrication Imaging and Characterization
APT	Atomic Probe Tomography
AR	Aspect Ratio
aWN_x	Amorphous Tungsten Nitride
BOE	Buffered Oxide Etch
BUV	Broadband Ultra Violet
CMOS	Complementary Metal-Oxide Semiconductor
CNT	Carbon Nanotube
DI	De Ionized Water
DIBL	Drain Induced Barrier Lowering
DMD	Digital Micro-Mirror Device
DUV	Deep Ultra Violet
Ebeam	Electron Beam
EBL	Electron Beam Lithography
ER	Edge Roughness
ERS	Energy Reversible Switch
F_e	Electrical Force
FET	Field-Effect Transistor
FinFET	Fin-Field-Effect Transistor
F_m	Mechanical Force
FOX	Field Oxide
GW	Ground Water
HF	Hydro Fluoric Acid
HMDS	Hexamethyldisilazane
HP	High Performance
HRTEM	High Resolution Transmission Electron Microscope
I_{ds}	Drain to Source Current
ITRS	International Technology Roadmap for Semiconductors
LOP	Low Operating Power
LPCVD	Low Pressure Chemical Vapor Deposition
LSTP	Low Standby Power

LTO	Low Temperature Oxide
MEMS	Micro Electro Mechanical Systems
MOSFT	Metal-Oxide-Semiconductor Field Effect Transistor
NEMS	Nano Electro Mechanical Systems
NF	Nano-Fabrication and Thin Film
NPR	Negative Photo Resist
NT	Nano-Tube
NTFET	Nano-Tube Field Effect Transistor
NW	Nano-Wire
NWFET	Nano-Wire Field Effect Transistor
PEB	Post Exposure Bake
PECVD	Plasma Enhanced Chemical Vapor Deposition
polyMUM	polySilicon Multi User MEMS Process
PPR	Positive Photo Resist
PR	Photo Resist
PVD	Physical Vapor Deposition
RIE	Reactive Ion Etching
RIE	Reactive Ion Etching
RTA	Rapid Thermal Anneal
SEM	Scanning Electron Microscope
SiO_2	Silicon di Oxide
SOI	Silicon On Insulator
SS	Sub-threshold swing
TEM	Transmission Electro Microscope
TFET	Tunneling Field Effect Transistor
UV	Ultra Violet
V_d	Drain Voltage
V_g	Gate Voltage
V_{pi}	Pull-in Voltage
V_{po}	Pull Out Voltage
V_s	Source (Cantilever) Voltage
WN_x	Tungsten Nitride
XRD	X-ray Diffraction

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Chapter 1

INTRODUCTION

1. INTRODUCTION

The “least effort” principle is a broad theory hypothesized in 1894 by French philosopher Guillaume Ferrero, who published an article in the "Revue Philosophique de la France et de l’Étranger”. The principle states that people, animals and machines will choose the path of least effort. One of the most daunting tasks since the dawn of history is repeatability of counting and related calculations. These tasks require a high degree of caution and accuracy. Therefore, counting aid apparatuses began appearing in history starting with scribing numbers on bones and stones, followed by the counting board (abacus) and eventually Napier´s bones was invented in the early 17th century [1]. Over the next two centuries, mechanical calculators were further developed. In the late 19th century Herman Hollerith invented the first electromechanical counting machine called “the tabulating machine”. In the early 20th century, IBM, Inc. implemented Howard Aiken’s idea to build a complicated counting machine, commonly called “Mark I”. This machine used punched cards weighing about 5 tons to perform calculations. A wrong calculation incident occurred when a punched hole was blocked by an insect. After this, any software issues were called “bug”. A few decades later, in 1946, Electronic Numerical Integrator And Computer (ENIAC) was launched as the first fully electrical computing machines run by electric boards and vacuum tubes. Simultaneously, solid state

transistors were invented and a decade later the integrated circuit was fabricated. This event started the modern era of computation. In 1975, the Altair 8800 personal computer launched a new industry of microcomputers which inspired Steve Jobs to start Apple and Bill Gates to start Microsoft.

Today's integrated circuits consist of billions of nano-scaled transistors called Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), which are capable of processing vast data in a short time. A MOSFET works by applying a voltage to the gate which induces conduction of charge carriers in the channel between the source and drain. The minimum voltage required is known as the threshold voltage (V_{th}). A shorter gate length means a smaller footprint and faster transistors, which is the ultimate goal of the semiconductor industry. It has been predicted by Gordon Moore (co-founder of Intel) that the number of transistors in a microchip doubles every two years and is known as Moore's Law. The tremendous advances made in the semiconductor industry have been driven by Moore's Law to achieve unprecedented performance/cost perspective [2]. However, as a trade-off, the power consumption and heat generation by these transistors are increasing exponentially, leading to this phenomenon being termed "the energy management crisis for the digital era" [2, 3] (Fig. 1-1).

Shrinking transistor size is performed by making the gate length physically shorter which demands more sophisticated processes and ultra-expensive lithography tools [2] (Fig 1-2). One of the most pressing issues of shrinking the size of a transistor is the increase in leakage current (I_{off}) causing higher heat generation. This phenomenon is known as the short channel effect. Furthermore, charge transport based devices depend

on an un-scalable value called thermal voltage ($V_T=k_BT/q$), where k_B = Boltzmann´s constant, T = temperature and q = electron charge. The thermal voltage directly affects a feature called sub-threshold slope (SS). SS is simply defined as how much voltage is needed for a rapid rise in current flow change from ON to OFF state or vice versa (equal 60 mV/decade for transistors) [4]. This unit indicates that at least 60 mV of voltage is required to achieve an appreciable change in current flow (10 times more) to distinguish between OFF and ON state (or simply 1 and 0). The high SS value raises a serious challenge to achieve higher performance transistors with a lower threshold voltage.

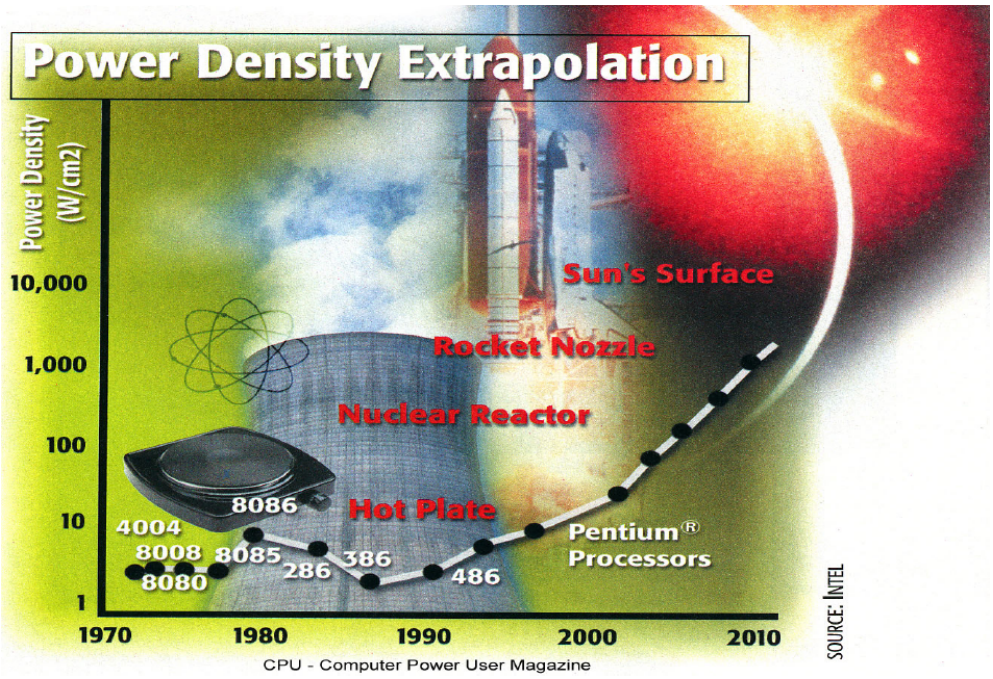

Figure 1-1 | Power Density of CPU [2]

From a physical standpoint, this indicates that alternative transistor architecture and physics is required to reduce the power consumption. Some examples include but are not limited to: double or tri gate multi-gate transistor, tunneling field effect transistor (FET),

carbon nanotube FET, gate all around nanowire FET, silicon nanotube FET and nanoelectromechanical (NEM) switch. Some of these new approaches have improved performance and individual low standby power consumption. Despite the better control of leakage current, the new alternatives of charge transport devices overall consume higher amount of standby power due to increasing number of devices in a specific area. Therefore, mechanical switches started drawing attention for their inherent zero-state leakage current and nearly ideal sub-threshold swing [5].

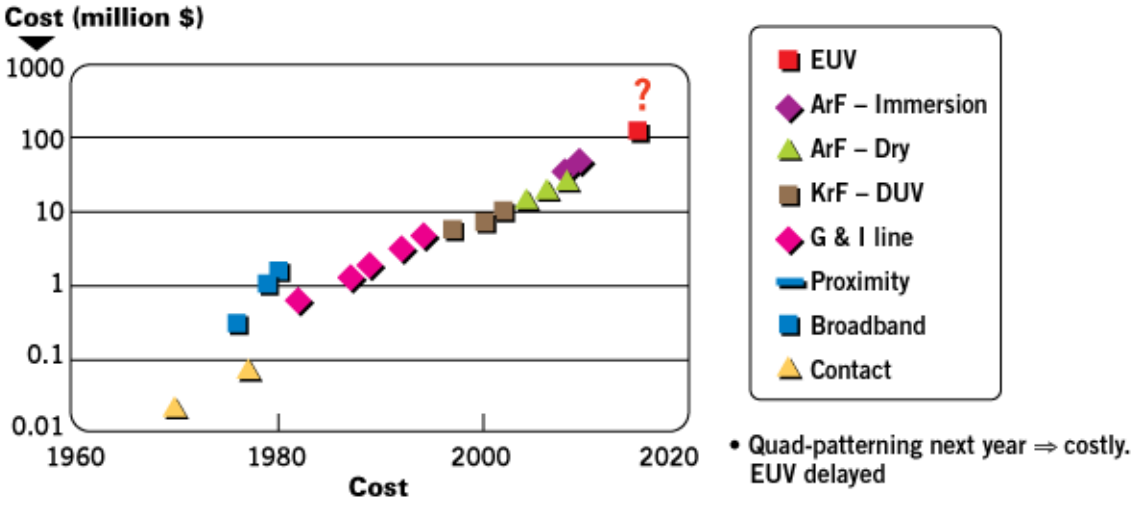

Figure 1-2 | Lithography Equipment cost for fine features (ASML)

2. ELECTRO-MECHANICAL SWITCHES (RELAYS)

Electro-mechanical (EM) switches are virtually ideal switches for their inherent zero leakage current and abrupt switching. In fact, some of the early versions of computers were constructed by using electromechanical switches (relays). The first electro-mechanical programmable calculating machine, called Z3, was built in 1941 using electro-mechanical relays [6, 7]. These relays were operated by electromagnetic

attraction force generated by a solenoid coil to pull the armature in order to open or close the circuit (Fig. 1-3).

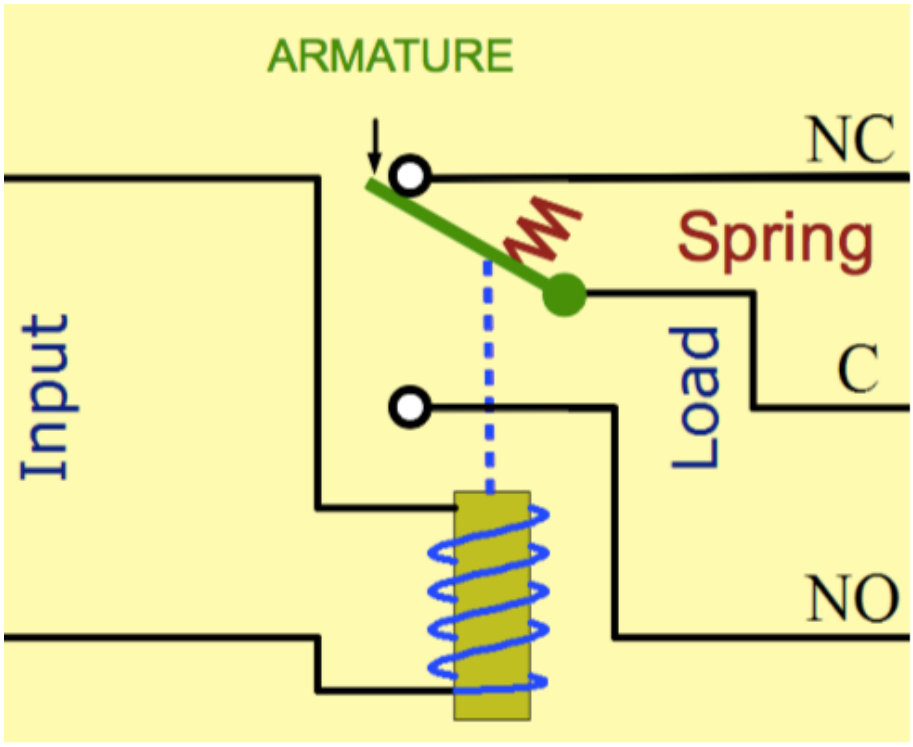

Figure 1-3 | Electro-mechanical switch NC.

The generated electromagnetic force by the solenoid coil consumes high power and takes a long time to operate the armature [8]. For these reasons the EM switches did not last long against vacuum tubes and solid state technology. In order to minimize the operational power consumption and increase the switching speed, electrostatic force (F_e) should be used instead of electromagnetic (F_g) force. However, the electrostatic force is much weaker than the electromagnetic force but much faster in response, analogous to charging and discharging a facing capacitor electrodes. Hence, the overall size and gap of EMS should be shrunk to minimize the required voltage for pulling the armature.

Minimizing the dimensions of the switch to micrometer size delivered a lower pull-in voltage in the range of 30 to 50 volts, which can be achieved using Micro-Electro-Mechanical Switch (MEMS). MEMS actuation by electrostatic force led to significant reduction in operational power and increase in switching speed, since there is no coil charging and discharging. Microscale devices are dependent on surface area parameters rather than volume parameters. They are affected by friction rather than inertia, heat transfer rather than heat content, and electrostatic force rather than magnetic force. MEMS switching time is in microsecond range. The terms armature, solenoid coil and contact are replaced with cantilever, gate plate and drain, respectively.

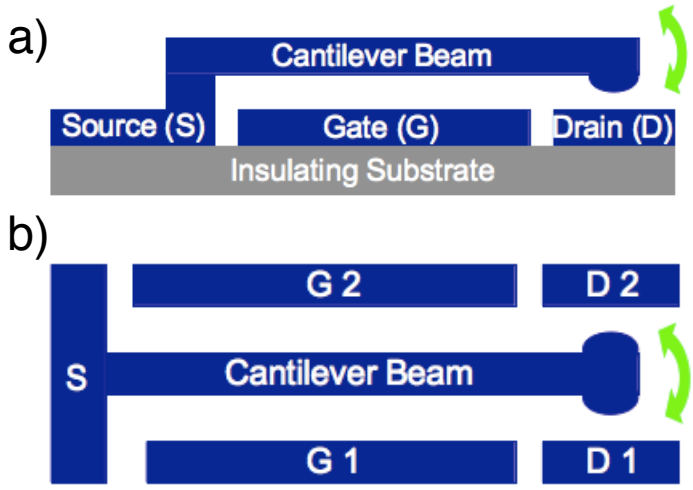

Figure 1-4 | a) vertical M/NEMS (side view); b) Lateral M/NEMS (top view).

MEM switches have been fabricated out of a polysilicon layer coated with gold on a silicon substrate, for a variety of applications. These MEMS have serious limitations such as low Young's modulus value (for Si ≈ 160 GPa), the presence of large grains, very high internal residual stress and high resistivity due to the grain boundaries. These effects

shorten the lifetime of MEM switches significantly. Early MEMS were vertically operated (vertical MEMS) (Fig. 1-4 upper), the cantilever moves out of the plane direction, analogous to the early EM switches but pulled down by electrostatic force.

3. NEMS REVIEW

Nanometer sized MEM switches (called NEM switches) could be designed and fabricated to operate either vertically or laterally (parallel to the plane) [4]. The cantilever width of lateral NEM switches must be sub-micron range, preferably sub-100 nm. The lateral NEM switch could be fabricated by a single mask (Fig. 1-4 lower). Scaling down the size of MEMS into nanometer range can lead to low actuation voltage (sub-1 volt) with high speed (GHz range) [9]. The first demonstrated NEM switch was fabricated in 2004 by using carbon nano tube (CNT) [10] and lightened the way toward further development of NEM switches. Later research lead to a comprehensive design of NEMS as suspended gate for MOSFET transistors and also a two terminal capacity switch [11-13]. These achievements were in 2005 using vertical NEM switches.

While research continued in the field of vertical NEM switches especially with CNTs, the first lateral NEM switch was demonstrated in early 2006 as a NEM resonator [14]. Again, this opened the door widely for lateral NEM switches. Over the next four years, vertical NEM switches were fabricated using a polysilicon material with metal at contact area for higher conductivity and lifetime. Titanium metal and alloys have been investigated to fabricate NEM switches. An all metal NEM switch has been fabricated out of TiN, reaching pull in voltage around 13 volt [15]. The structure NEM switch has been

used to develop a non-volatile memory (NVM) device [16]. A random access memory (RAM) device has also been fabricated using NEM switch [17]. An analytical model of suspended gate FET transistor has been developed with extensive simulation work [18, 19]. A few complex designs have been fabricated as the four terminal relay in 2009 [20].

In early 2010, lateral NEM switches start appearing notably on the surface [21, 22]. Other material also has been used to fabricate the NEM switched such as silicon carbide (SiC) to withstand harsh environment and elevated temperature up to 500°C [22]. For the first time, an all metal NEM switch was fabricated out of nickel in early 2010. This device was fabricated in a unique way using focus ion beam (FIB) to reach around 1 to 20 nm gap [23]. Another high achievement by this same device was 1 volt operation. Consequently, alternative materials to silicon have been extensively studied and experimented to fabricate NEM switches. Late in 2010, a silicon carbide nanowire was used to fabricate a NEM switch with pull-in voltage around 1 volt and sub-microsecond switching time [24].

An interesting research showed that the lateral NEM switches with double side gate, as in Fig. 1-4 (lower), has shorter settling time than the vertical design. This is because of the confined air on both sides of the cantilever. Another advantage of the lateral NEM switch is the extra degree of freedom the other gate provides. The existence of the other gate allows to construct XOR/XNOR gate with only two NEM switches, unlike CMOS which needs at least eight transistors [25]. Later, during 2011, lateral NEM switches were explored and fabricated extensively, however few of them exhibited acceptable switching characteristics with adequate lifetime results [26]. A lateral NEM

switch fabricated of platinum-coated polysilicon showed longer lifetime and steeper I-V curve [27]. An extensive sensitivity study was conducted on lateral NEM switches and showed very interesting results [28]. Another all metal lateral NEM switch was fabricated out of platinum and integrated with a CMOS device using a standard electron beam lithography (EBL) process [29].

After this progress, in 2012, NEM switches started to be considered to fabricate logic gates and memory cells. Non-volatile memory (NVM) could be fabricated using two terminal NEM switches to function as a diode because of their excellent retention and hysteric behavior [30]. NEM switches with metal electrodes are highly susceptible to oxidation. Lower frequency shows less contact resistance than higher frequency. Encapsulating the device properly from oxygen would overcome the oxidation issue but the contact deterioration issue still not solved completely [31]. High-performance CNT NEM switch has been reported with response time about 10 nS [32]. Different shapes and designs were used in order to lower the pull-in voltage including a U-shape design [33].

Elaborate efforts have been made to integrate NEMS technology with CMOS to optimize the advantage of both devices, energy conservation from the first and speed from the second. Micro-architecture and circuit design have been tailored to MEM-relay device properties for implementation of complex arithmetic units in early 2013 [34]. NEM switches employ the progress in nano machining. However, there would be a limit in scaling down the NEM switches. Adhesion, contact resistance, and actuation voltage are the limiting factors for NEM switches [35]. Another interesting idea has been investigated to make the physical contact between the cantilever and the drain in two

steps. The first step uses a hard material (high contact resistance) to lower the electric field strength between the two electrodes and the second step uses a soft material (low contact resistance) to get high current flow [36].

In early 2014, a very compelling NEM switch design was illustrated as curved switch coated with amorphous carbon. The curved electrode overcome the excessive field and the amorphous carbon coating has lower surface energy than metal to overcome the adhesion issue [37]. Another fabricated NEM switch with curved electrodes operates at high temperature 300°C [38]. The first experimental NEMFET has been demonstrated with silicon nanowire suspended over FET transistor. The fabricated device showed an impressive result of pull-in voltage less than 2 volts [39]. Another very exciting research and experiment have been conducted to extract the contact adhesion force without the need for finite element (FEM) simulation. This work hypothesizes that the adhesion force is proportional to the contact size, and would be negligible for very small size and coated with thin oxide [40]. All metal NEM switch fabricated from molybdenum drew attention for sustaining elevated temperature environment at 300°C for more than 1000 cycles [41]. The adhesion force yields hysteresis style operation for the NEM switch. In NEM switch the hysteresis is undesired, unlike in non-volatile memory (NVM) devices. The hysteresis is highly desired in NVM to store the status for the next reset. One experiment shows NEMNVM that function only with one gate and the reset signal is applied to the same gate as a sequence of pulses to release the cantilever from the adhesion status. This experiment was conducted at elevated temperature (300°C) successfully [42]. Combining a piezoelectric material on the doubly clamped NEM switch at both anchors, yields in

lowering the pull-in voltage by 50% [43]. A design for a multi layer lateral NEMS has been suggested to reduce the footprint of the device. The cantilever and gate length has been divided into three layers in the z direction [44]. A three terminal NEM switch has been fabricated out of suspended graphene disk. The pull-in voltage was high around 30 volts, but the idea was unique. Due to high Young's modulus of graphene (1 TPa) there is very low hysteresis in I-V curve [45].

More recently, in 2015, a few more experiments conducted on NEM switches analyzed the adhesion force components, and lead researchers to correlate deflection profile, surface energy and all different types of forces acting on the contact area, such as Casimir force and fringing field [46]. One motivation in the NEMS domain is to employ NEM switches for ultra low power operation since this is an ultimate advantage of NEM switches. An analytical model is developed to assess the switching energy of a NEM switch. Shrinking the gap between drain and cantilever to below 1 nm causes the adhesion force to pull the cantilever toward the drain to form a normally closed (NC) switch. The mechanical restoring force will not encounter the electrostatic force so the pulling energy will be reduced ten times [47].

Amorphous metal (metallic glass) is brittle compared to crystalline metal. Scaling down the size is not only limited by successful operation, it is limited also by the material property. The material's microstructure should be comparable with smallest characteristics dimensions to pass over the crucial role of material-induced size effects. This would affect the metallic glass to be transitioned from brittle-to-ductile [48]. This

transition occurred when the wall thickness is below certain size (called threshold size) [49]. Fig 1-5 shows ideal position NEM switch and activated one.

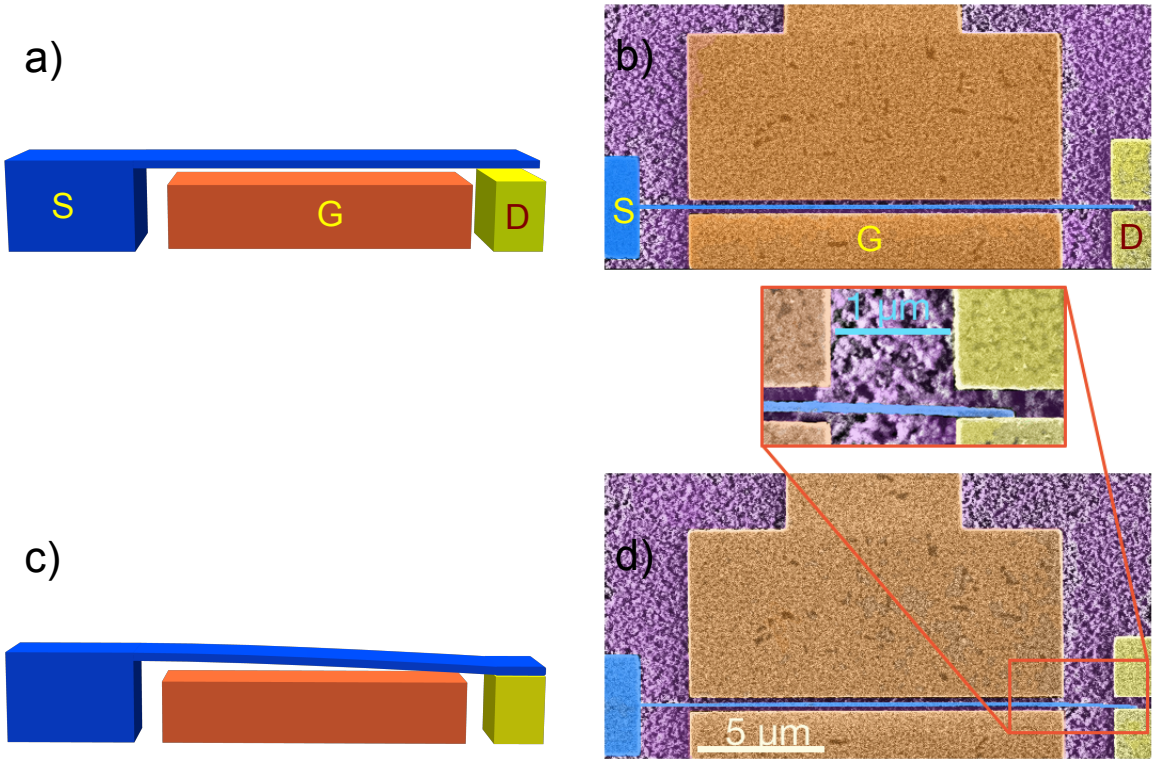

Figure 1-5 | Three terminals NEM switch design and SEM picture; a) and b) idle position; c and d) pulled-in position.

4. Status Quo and Motivation

The MEM and NEM switches and devices have excellent characteristics in abrupt switching with quasi-zero leakage current (no heat generation). On the other hand, the micron and nano crystalline clusters limit NEM switch fabrication. Silicon on insulator (SOI) substrate could be used to fabricate cluster free NEMS devices. Other materials and designs have been investigated to avoid the high cost of SOI substrate and silicon material defects. Carbon nano-tube and different metals (such as titanium) with harder

and higher elasticity and smart designs has been conducted to overcome these defects [10, 16, 20, 50-56]. In addition to the switching functions NEM devices can be used for high sensitivity sensors, motion detection (accelerometers and gyroscopes), valves, pumps and many others [57-63].

From all the above-listed developments in electrostatically actuated NEM switch evaluation, design, and fabrication over the last decade, the following table depicts their summary (Table 1-1):

Periodical	Description	Design	Type	Length Width Thick Gap	V_{pi}	Cycles	Switch Time
MRS 2006 Hunt	CNT	Double Clamped	Vertical		4.5V		2.8nS
APL 2008 Lee	TiN all metal NEMS	Single Clamped	Vertical	300nm 200nm 35nm 15nm	12V	400	
SSE 2008 Park	TiN all metal NEMS	Both	Vertical	300nm 200nm 35nm 20nm	12V	400	
DRC 2008 K Akarvardar & P. Wong	Theoretical work, Simulation no experiment	Single Clamped	Lateral		2.24 V		
IEEE 2008 International Conference on Computer-Aided Desig, Chen	Theoretical work, Simulation no experiment Complex circuit design using NEMS	Single Clamped	Vertical	2.3μm 90nm 90nm 10nm	0.2V		
IEDM 2009Tsu Jae (UC Berkeley)	Poly-Si0.4Ge0.6/ PVD W/ALD TiOx (3A) 20 - 200C	4 Terminal	Vertical		5V	100	

Periodical	Description	Design	Type	Length Width Thick Gap	V_{pi}	Cycles	Switch Time
IEDM 2009 Tsu Jae (UC Berkeley)	Poly-Si0.4Ge0.6/ PVD W/ALD TiOx (3A) Inverter	4 Terminal	Vertical	30µm 4μm 1μm 200nm	2V	100	100 nS
IEDM 2009 J B Yoon (KAIST)	PVD TiN + MOCVD TiN Oil packaging	Single Clamped	Vertical	200 - 700 nm 400-900 nm 30nm 40nm	8 - 12V	50	
IEDM 2010, Philip Wong (Stanford)	MOCVD TiNVertical metallic spacer	Single Clamped	Lateral	- - 1.1μm 350nm	18.6 to 34 V		
Science 329, 1316 (2010) Mehregany (CWRU)	PECVD 3C-SiC (N_2 doped) 500C, 21B cycles	Single Clamped	Lateral	8µm 200nm 400nm 150nm	6V	21B	2 μS
IEEE SENSORS 2010 Conference Massoud Tabib-Azar (U. Utah)	W, 1 GHz, 1V	Single Clamped	Lateral	- - - 20nm	1V		1 μS
JMEMS April 2010 Tsu Jae	Poly-Si0.4Ge0.6/ PVD W/ALD TiOx (3A)	Seesaw	Vertical		8 - 10V	400	
Nano Letters 2010, Roukes (Caltech)	SiC	Double Clamps	Lateral	8µm 25nm 25nm 27nm	1 - 1.5V	few	
MEMS 2011, Philip Wong (Stanford)	Pt/Poly-SiUniform electrostatic control	Both	Lateral	15µm - - -	15 - 26V		
DTIP 2011,Philip Wong (Stanford)	Doped poly-Si	Single Clamped	Lateral	20µm 300nm 1100nm	32V		
Transducers 2011, Philip Wong (Stanford)	Poly-Si/HfO2/Pt Fork architecture	Single Clamped	Lateral	15µm 1μm 1μm 500nm	19.3 V		

Periodical	Description	Design	Type	Length Width Thick Gap	V_{pi}	Cycles	Switch Time
Transducers 2011, Philip Wong (Stanford)	Poly-Si Two switches	Single Clamped	Lateral		12.8 V 21.8 V		
IEDM 2011, Philip Wong (Stanford)	Pt/Ti Integrated with CMOS	Single Clamped	Vertical	3.5µm 80nm 65nm 100nm	4.3V		
Sensors and Actuators A 166 (2011) 269–276 Victor Bright (Colorado, Boulder)	ALD W ALD W 5M cycles	Double Clamped	Vertical	3µm 500nm 32nm 30nm	1.5 - 2V	300	
APL 2012 Chengkuo	Si NW Dual contact	U shaped	Vertical	5μm 90nm 90nm 145nm	1.12 V	12	
IEEE MEMS conference 2013 M. Shavezipur	ALD TiN & Psi soft contact	Single Clamped	Lateral	12μm 800nm 1μm 700nm	27V	10k	0.1 S
IEEE 2013 Hussain	Amorphous WN all amorphous metal	Single and Double Clamped	Lateral		3.5V		
JMEMS March 2013 Howe (Stanford)	PSi + Pt side wall	Single Clamp	lateral	16µm-500nm 1.2μm-600nm	12V	100M	1-0.5 μS
MEMS 2014 Chengkuo Lee	PSi encapsulated vacuum Heavy duty structure and 500C	Single Clamped	Lateral Curved	R-75μm 5μm 40μm 1.5μm	26V	100k	13μS
MEMS 2014 Urs Duerig	PSi amorphous carbon Heavy duty structure	Single Clamped	Lateral Curved	R-75μm 1μm 220nm 60nm	7V	100M	200nS

Periodical	Description	Design	Type	Length Width Thick Gap	V_{pi}	Cycles	Switch Time
Nano Letters 2014 Xiang UC SD	Ge/Si core shell NW First NW NEMFET	Double Clamped NW	Vertical	1.32μm 25nm 25nm 35nm	2V	130	
RSC 2014 Chengkuo Lee	Mo metal all metal NEMS	Double Clamped	Lateral	28μm 300nm - 150nm	7.5V	20k	
IoP Nanotechnology, 2016 Hussain	Amorphous WNx all amorphous metal	Single clamped	Lateral	15μm 190nm 500nm 150nm	0.8V	100	

Table 1-1 | The status quo of electrostatically actuated NEM switch.

From the above table of the status quo, it is clearly observed that NEM switches are developing rapidly in terms of lifetime, pull-in voltage and switching speed. Many materials have been investigated for nano-fabrication where polysilicon is not compatible. The silicon-on-insulator (SOI) substrates have been experimented for nano-machining conjugated with metal [64-68]. The trade-off here is the high cost of SOI substrate, which limits its usage from a financial perspective. Besides, the other issues of silicon still standing to be solved.

Carbon nanotubes (CNT) appeared to be a competitor candidate for their electrical and mechanical properties for a wide spectrum of applications [69-71]. The main issue for CNT is the reproducibility and controllability [72, 73]. In the past, a titanium nitride (TiN) based vertical cantilever NEM switch with a 15 nm thickness with a 35 nm air gap showed interesting characteristics of SS equals to 3 mV/decade and current on/off ratio of

more than 10^5 in ambient air for hundreds of cycle times [15]. SiC has been considered and utilized to fabricate NEM switches. The fabricated devices exhibited very promising results of sub 100 nm dimensions and low pull-in voltage [22]. The major concern with SiC is its high value of hardness for micromachining plus the high thermal budget requirement for material formation.

Finding of a new material that is superior to silicon and also CMOS compatible is a top priority to fabricate a high-performance NEM switch. The new material should exhibit certain characteristics such as high Young's modulus for greater restoring force, high hardness to preserve the contact surface, high density to have shorter damping amplitude and time, oxidant resistance, grainless to reduce the internal stress and compatible to CMOS process. If this material is innovated, then it could be the holy grail to fabricate sub-100 nm structure without mechanical deformation or compromised structural integrity.

An extensive screening process has been conducted to look for a material that is compatible with CMOS micromachining process and overcome deficiencies of silicon in MEMS devices. The material should be highly conductive (preferably metallic) and easily micro-machined. Tungsten has been found to be the best candidate because it is CMOS process compatible, used in CMOS fabrication and commercially available with low cost. However, tungsten has polycrystalline microstructure which can deteriorate the functionality of NEM switches. Fabricating a metal with a single crystalline microstructure is not possible with the status-quo CMOS processes. Consequently, the other alternative is to fabricate an amorphous metal from tungsten by alloying it with

another element to prevent the crystallization process. Adding nitrogen atoms among tungsten atoms in certain condition produce an amorphous metal alloy without deteriorating the tungsten metal characteristics. The name of new alloy is amorphous tungsten nitride (aWN_x).

	14 nm CMOS	30 nm NEM Switch
NAND Gate Size μm^2	0.248	0.9 scalable up to 0.1
Switching Energy >1 MHz	High at low frequency > pJ Low at high frequency < aJ	Constant around aJ
Leakage current	71 nA	≈ Zero
V_{dd} / V_{th}	1 / 0.6 volt	0.6 / 0.6 volt
Cost $/unit	0.1	< 0.05
Speed	5.5 GHz	33 MHz
Performance	20 - 30 Years	15 - 20 years
Integration Density	4 millions gates per mm^2 with 13 wiring levels	Single layer so far
Production Yield	Off record, ≈ 60%	Lower than CMOS
Other usages	Logic gates, Sensors, Analogue amplifier, Power electronics, ADC and DAC	Logic gates, Switches, Relays, Power switches, Sensors, Mass inertia sensors

Table 1-2 | Comparison between NEM switches and CMOS MOSFET.

NEM switches are superior to CMOS technology in some fields and lagging in others. From the prospective of energy consumption and dissipation, foot print,

subthreshold slope and cost NEM switches are forerunner. However, in case of speed, reliability, lifetime, endurance and compatibility solid state are the champions [25, 74-76]. The following table 1-2 shows the comparison between state of art of NEM switches and CMOS MOSFET.

5. RESEARCH OBJECTIVE AND DISSERTATION OUTLINE

This doctoral thesis investigates the development and engineering of an amorphous metal, tungsten nitride (aWN_x), to overcome material related issues associated with fabrication of NEM switches. The fabrication process of the NEM switches using aWN_x is extensively investigated. Fabricated NEM switches have been characterized and experimented and engineered to overcome all the defects mentioned earlier. High endurance and expendability experiments have been conducted.

Chapter 2 shows the process followed to develop and engineer amorphous metal tungsten nitride (aWN_x). The material was subjected to three independent tests to confirm amorphousness. This section also includes mechanical and electrical properties of this new material. Lifetime and reliability tests are disclosed, as well as a study of compatibility under harsh environment.

Chapter 3 describes several designs of NEM switches using different dimensions and layouts. Corresponding theoretical pull-in voltages have been calculated. Simulation has been conducted for selected designs and dimensions using COMSOL™ software. The results have been tabulated and compared.

Chapter 4 demonstrates the different processes followed to fabricate the NEM switches. Four different processes have been pursued. Each step of the processes is discussed and characterized. A spacer technology has been described and discussed for this material. Different processes were compared and the most promising one has been used to carry out the fabrication. Electron beam (E-beam) lithography (EBL) process has been developed for each process and effective parameters have been listed. Exposure energy and proximity effect has been discussed and considered to reach the most effective conditions. Ultra violet light lithography (UVL) has been developed for the mentioned process as well.

Chapter 5 presents the electrical characterization results of the fabricated aWN_x NEM switches. The operation of NEM switches was determined by performing current – voltage (I-V) measurements and plotting the I-V curves. Pull-in voltage, resistance and contact resistance were extracted from the I-V curves as well as the endurance of the device. Characterization was completed under vacuum to prevent device breakdown in ambient air. I-V curves have been plotted for different devices.

Chapter 6 highlights the experimental behavior that proves aWN_x is a promising candidate for NEM switch fabrication as well as a potential material for other MEM/ NEM device applications. The high endurance behavior against corrosion and non-crystalline structure of amorphous WN_x is presented. To further understand its suitability for biodegradable and implantable MEM/NEM devices, the dissolution rate of aWN_x in different types of aqueous solutions under different conditions were studied and discussed.

Chapter 7 discusses the major achievements and future challenges of the work presented in this doctoral thesis. It summarizes the key findings of the conducted experiments. It also provides the advantages and breakthroughs associated with the amorphous WN_x NEM switches and devices.

Chapter 2

AMORPHOUS WN_X METAL, FABRICATION AND CHARACTERIZATION

1. INTRODUCTION

Diminishing dimensions in charge transport based solid-state complementary metal oxide semiconductor (CMOS) devices have contributed to higher speed but at the cost of rising power consumption due to the unintended movement of charges even in the OFF state. Additionally, fundamental limitation of sub-threshold slope (SS) following Boltzmann's Rule (kT/q) for charge transport devices remains at 60 mV/dec (limiting faster switching from OFF to ON state and vice versa) which also results in higher dynamic power consumption. Tunnel field effect transistor (TFET) and nanoelectromechanical (NEM) switch are two attractive options to lower the SS below present fundamental limitation of 60 mV/dec [77]. Compared to TFET devices, NEM switches theoretically and practically offer the steepest SS and nearly have shown zero static power consumption due to their physical isolation originated from their mechanical operation. While choice of switch design can facilitate interesting attribute(s), and many NEM switches have been demonstrated with attractive features [10, 16, 20-22, 24, 29, 51-53, 55, 56, 78-85], fundamental challenges remain with NEM switches in context of their performance and reliability (especially from electrical and mechanical perspectives):

(i) necessity of lower pull-in voltage (Vpi) comparable to that of state-of-the-art CMOS technology; (ii) operation in ambient/air; (iii) increased ON current and decreased ON resistance; (iv) scaling of devices and improved mechanical and electrical contacts; and (v) high endurance. If all the above mentioned challenges can be overcome in a single design of NEM switch, that would be the most "perfect" NEM switch ever. Here, we show such a switch fabricated with amorphous metal tungsten nitride (aWN_x) nano-ribbon.

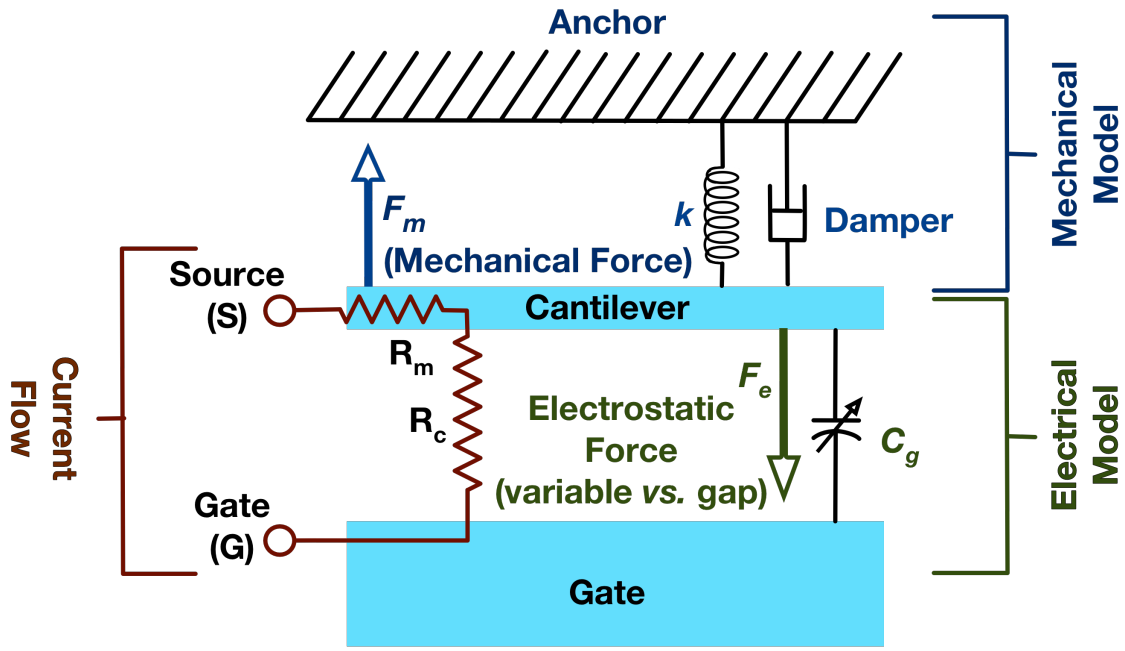

Figure 2-1 | NEM switch; mechanical and electrical equivalent circuitry for two terminal NEM switch.

Generally, NEM switches are mechanical switches, which have an active element (mainly a movable cantilever singly or doubly anchored) actuated (pulled) by electrostatic force (F_e) generated from the opposing fixed and rigid electrode. The mechanical and electrical schematic and equivalent circuitry is demonstrated in Figure

2-1 where R_m is the amorphous metal internal resistance of the cantilever and gate, R_c is the contact resistance between the cantilever and the gate, F_m is the mechanical restoring force, F_e is the electrostatic pulling force and C_g is the capacitance between the gate and the cantilever. The active element and static part are analogous to a capacitor facing plates. The active element has an inherent mechanical restoring force (F_m), which opposes the external influence (F_e). NEM switch operation embraces mechanical and electrical activities concurrently. The mechanical operations include: acceleration, deceleration, hammering style impact, damping and oscillation. The electrical activities include: electric charge, discharge, high current flow, charge accumulation and abrupt discharge. This complex operation of NEM switches cause the material of the active element as well as the electrode to deteriorate rapidly and shorten the lifetime of the switch, consequently impairing the electrical functionality. Most of the NEM switch defects are categorized into four main categories: (i) electrical discharge damage to contact area; (ii) electrode weariness and deterioration; (iii) stiction and (iv) mechanical failures (fracture or fatigue) of the active element, as visualized in Figure 2-2 (a-f) [55, 56].

Figure 2-2(a) shows the side view of vertically actuated 3 terminal NEM switch in idle mode and Figure 2-2(b) shows operational mode when the active element contacts the electrode. The movement of the active element toward electrode causes a high accumulation of electric charges inversely proportional to the gap between them. This accumulation of charges could cause abrupt electric discharge (spark) especially with the existence of high surface roughness as shown in Figure 2-2(c). This electric discharge

could cause material melting (burn-out). Ablation and electrode surface damage could occur as a direct result of electric discharge as in Figure 2-2(d) [24]. At the contact point, the active element is exposed to three balanced forces; electrostatic force (F_e) induced by the pull-in voltage, van der Waals force and Casimir force toward the electrode, and mechanical restoring force (F_m) outward of electrode [78, 82]. Failing to restore the active element to its original position when the F_e vanishes causes stiction as shown in Figure 2-2(e) [79].

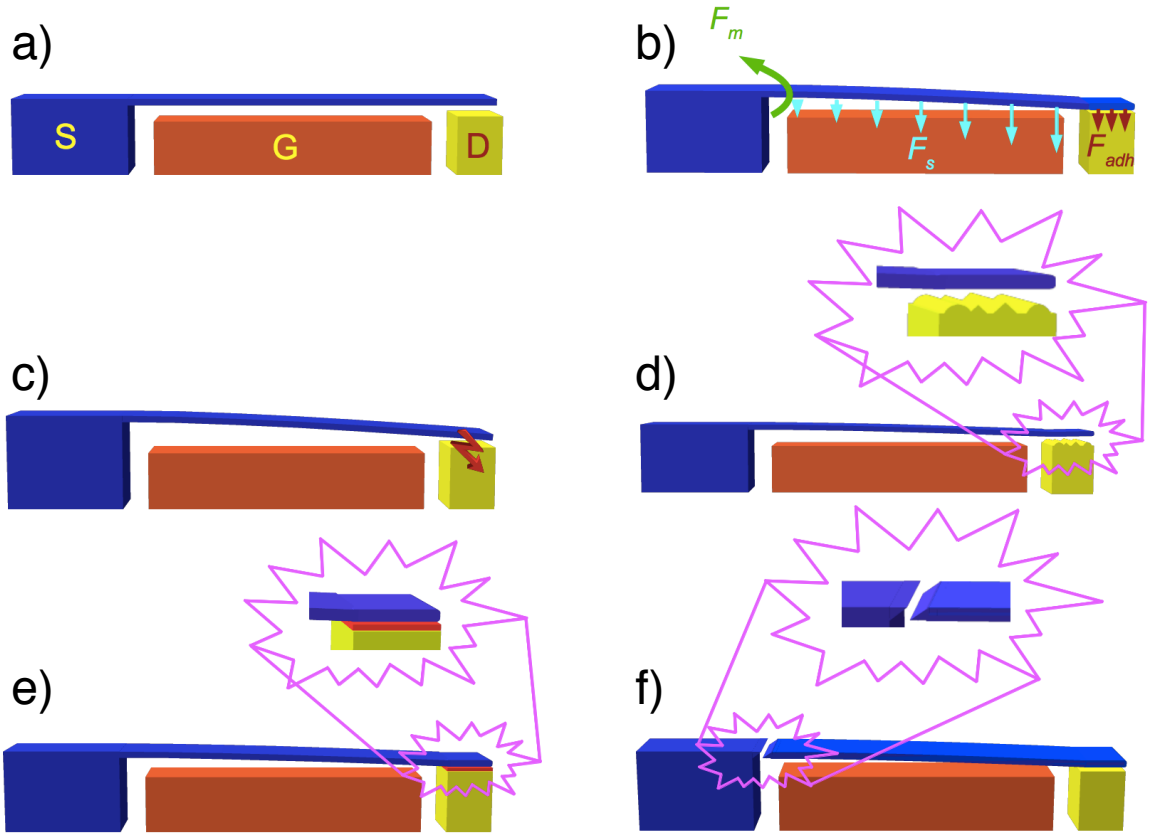

Figure 2-2 | NEM switch; a) idle position; b) pulled in position; c) electric discharge fault; d) ablation fault; e) stiction fault; f) fracture fault.

The material of the active element should have a high spring constant (high Young's modulus) to overcome the stiction issue. On the other hand, high Young's

modulus leads to high pull-in voltage, as they are directly proportional. To overcome this issue, the NEMS switch should be fabricated with smaller dimensions (gap and thickness) [10]. Finally, when the NEM switch operates without any of the above mentioned failures, the active element still faces mechanical failure. This failure is known as material fatigue or fracture and normally occurs near the anchor as shown in Figure 2-2(f) [77]. This failure occurs because of the grain boundary inter-stress and defects.

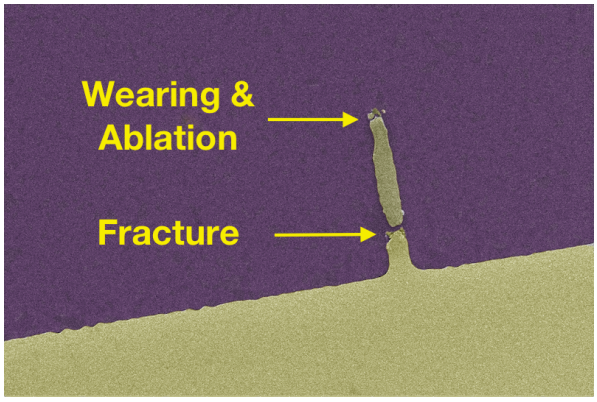

Figure 2-3 | SEM image from broken NEM switch after a few million cycles.

These defects weaken the strength of the material and degrade the electrical and thermal conductivity. This failure is the origin of NEM switch unreliability and short lifetime, resulting in only a few million cycles at the most. Figure 2-3 shows a defective cantilever, fabricated using gold (Au), due to fracture and contact area wearing. To overcome most of these issues, first we need to use a structural material which ideally will be of amorphous nature (for dimensional scalability) with (i) ultra-low surface roughness and (ii) optimal Young's modulus (high enough to counter act the stiction but to avoid the risk of higher pull-in voltage is compensated by dimensional scaling). Amorphous material is scalable to the nano-scale without structural defects. At the same

time, materials with high Young's modulus are stiffer and result in higher switching frequency (improved switching speed). As of today various materials have been used ranging from mono to poly-crystalline materials but yet no single material has come out as forerunner [10, 16, 20-22, 24, 29, 50-53, 55, 56, 79-81, 85]. Therefore, we have used aWN_x nano-ribbon as a unique choice of material for NEM switches and potentially for NEM systems.

2. AMORPHOUS TUNGSTEN NITRIDE

Amorphous WN_x has a grain-less molecular structure unlike tungsten poly-crystalline structure of 50-100 nm grain size [86]. AWN_x is generally corrosion resistant, is highly endurable, has a smooth surface, and has lower contact wear and exacerbation resistance [87]. It is to be noted that the terms amorphous metal and metallic glass are not the same. Conventionally, the terminology metallic glass is used for non-crystalline metal formed by continuous cooling from the liquid phase. On the other hand, the terminology amorphous metal is used for non-crystalline metal fabricated by methods other than from liquid, such as chemical vapor deposition (CVD) or physical vapor deposition (PVD).

In this paper, we have used reactive sputtering using PVD tool with tungsten (W) target to form aWN_x. Although many choices are available in context of choosing an amorphous material, we chose tungsten (W) based nitride alloy due to its: (i) intrinsic material characteristic: as a transition metal, tungsten and its nitride has simple crystalline structure which can be easily altered to transform them into amorphous films; (ii) commercial availability; (iii) economical; and (iv) CMOS compatibility: tungsten, unlike

most other type of metals, can be easily micro-machined with standard reactive ion etching (RIE) process using either sulfur hexafluoride (SF_6) or chlorine (Cl_2) gases [88].

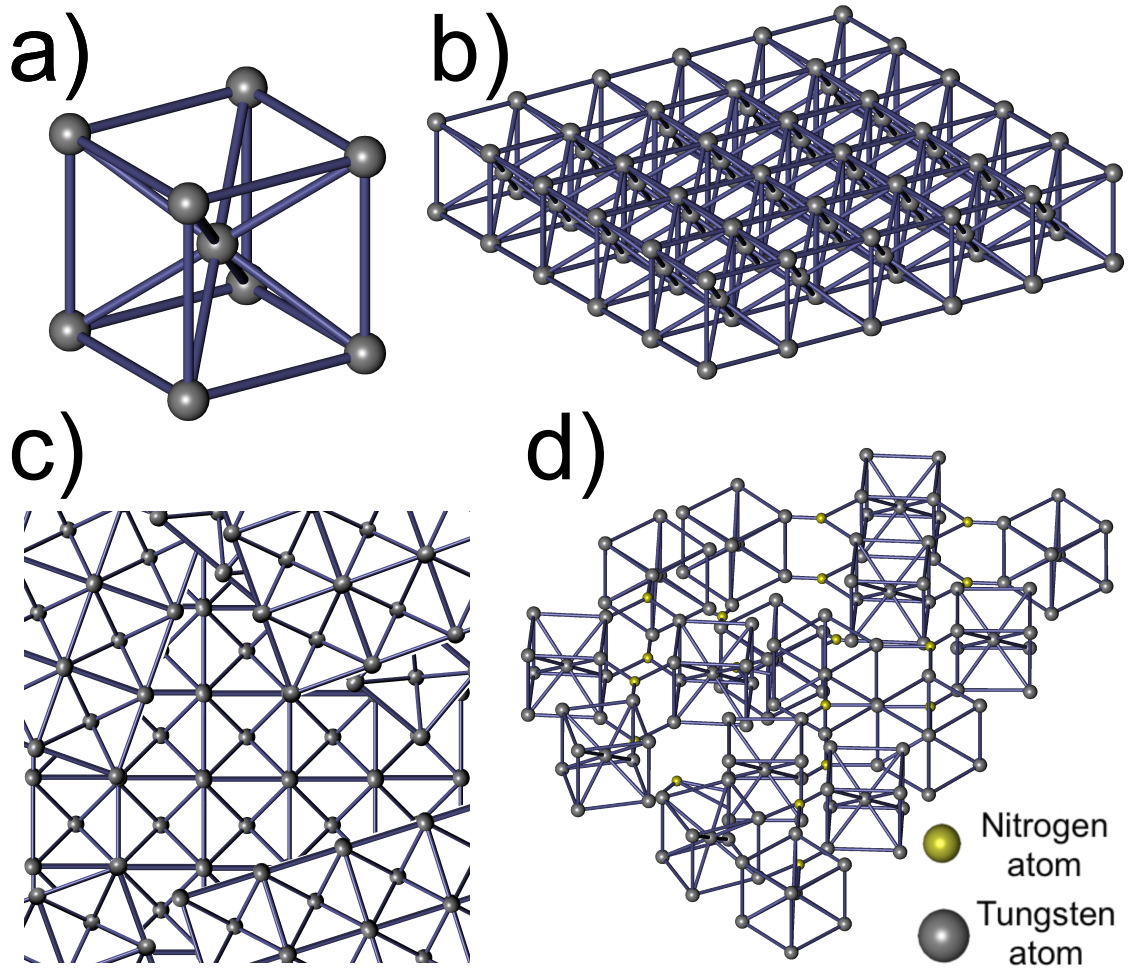

Figure 2-4 | Tungsten molecular structures; a) single crystal, b) single crystal structure, c) poly crystalline structure, d) amorphous WN_x molecular structure.

We developed a reactive ion etching process using chlorine (Cl_2) and oxygen (O_2) plasma, to pattern the amorphous WN_x thin film. These gases were chosen since tungsten is known to form volatile oxy-chloride compounds (WO_xCl_y) [89], while nitrogen can be emitted as nitrogen gas (N_2) [90, 91]. Furthermore, since this etch chemistry is selective

to WN_x over silicon oxide (SiO2), it is amenable to the use of a SiO2 hard mask for high-aspect-ratio etching. This feature makes aWN_x an attractive metal compared to other hard metal which requires focus ion beam (FIB) for micromachining [92].

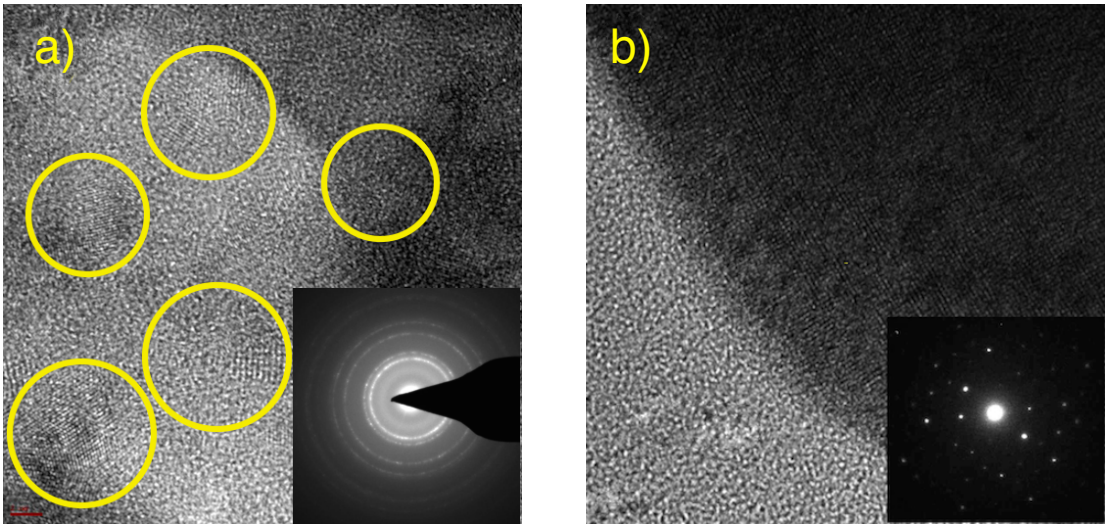

Figure 2-5 | a) TEM image of amorphous WN_x and TEM diffraction at lower right corner; b) TEM image of annealed crystalized WN_x and TEM diffraction at lower right corner.

Figure 2-4 shows the difference in the molecular structure among crystalline, poly-crystalline and amorphous WN_x. Amorphous WN_x material exhibits high melting point, hardness and electrical conductivity. Tungsten nitride alloy is a chemically stable compound due to its directional nature of the metal non-metal hybrid bonding [93-95].

Previously demonstrated aWN_x were not fully amorphous because when the material is exposed to a high temperature it starts crystallization as shown in Figure 2-5(a) [96]. In this figure, the image taken by using High-Resolution Transmission Electron Microscopy (HRTEM) tool shows the existence of a few crystalline islands (yellow circles) in the surrounding amorphous structure. This existence of crystalline clusters is presented in the TEM diffraction image as rings (lower right corner). As the

material is exposed to high temperature above 480°C it starts the crystallization process, as shown in Figure 2-5(b) TEM image and diffraction pattern. Figure 2-6 shows the Grazing Incidence X-ray Diffraction (GI-XRD) spectrum of the non-annealed amorphous WN_x (red) and also annealed crystalline WN_x (green). The wide spike around 40 degrees of the red curve indicates existence of few crystalline clusters embedded in the amorphous majority. The green curve shows typical spectrum of a crystalline material with sharp spikes after anneal. The amorphousness has a range from low (existence of few crystalline clusters) to high (no existence of crystalline structure).

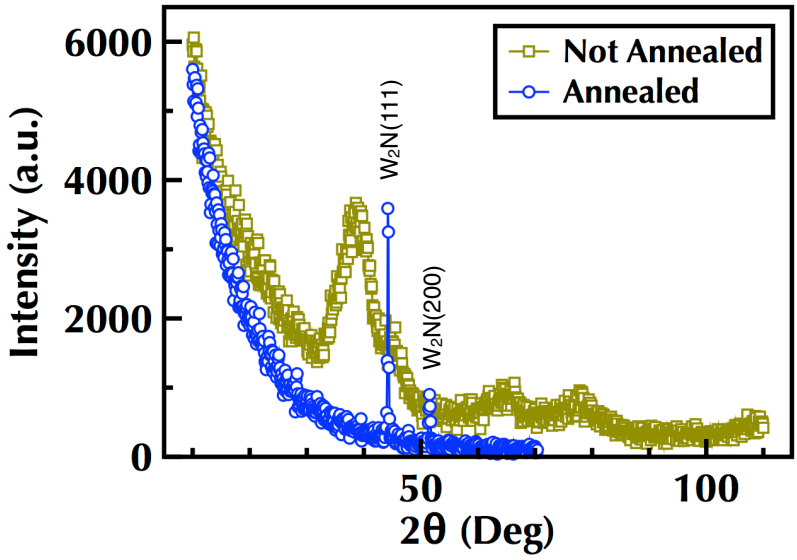

Figure 2-6 | WN_x XRD spectrum for non-annealed amorphous WN_x in red and annealed in green.

Metal in general has high adatom mobility to form crystalline structure by its nature. The natural tendency of metal is to from crystalline structures, because crystalline structures have less Gibbs Free Energy, ΔG, than amorphous structures. Existence of Nitrogen (N_2) gas in the plasma of the deposition chamber breaks the N_2 molecules into

N radicals to react with W atoms. This reaction slows down the adatom mobility to generate the amorphous molecular structure of WN_x. However, even a minimal existence of crystalline WN_x will completely crystalize all the material when exposed to high temperature above 480°C. Our objective was to achieve totally crystalline cluster free amorphous metal before fabricating the NEM switches by altering the sputtering conditions. Five different variables are typically associated to achieve this goal: pressure, power, gases mixture ratio, separation distance between target and substrate, and finally power type: alternating current (AC) or direct current (DC). In our study, we chose to fix the power to AC 300 W and maximized the distance from target to substrate in order to minimize the adatom mobility.

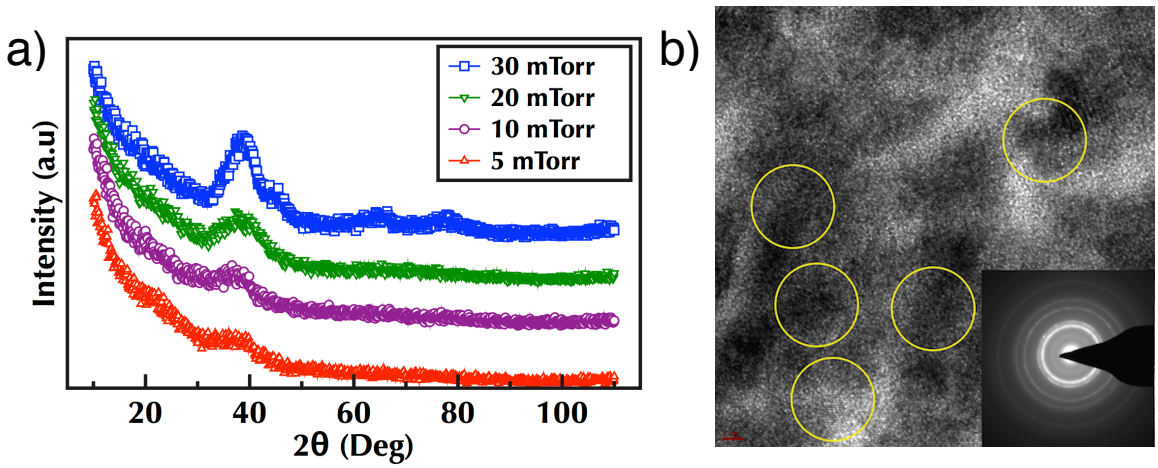

Figure 2-7 | a) XRD spectrums of WNx sputtered under gas mixture ratio Ar:N_2 55:5 at different chamber pressure values; b) TEM image for WN_x sputtered under 30 mTorr pressure and TEM diffraction image as an inset.

The ratio of Argon (Ar) gas to N_2 gas was fixed to 55:5 sccm and varied the sputtering pressure from 30 mTorr to 5 mTorr in four steps. The most amorphous structure was found at the lowest pressure, as shown in the XRD spectrum for all the

samples formed at various pressures (Fig 2-7(a)). Fig 2-7(b) shows the TEM and the diffraction image for the lowest pressure condition.

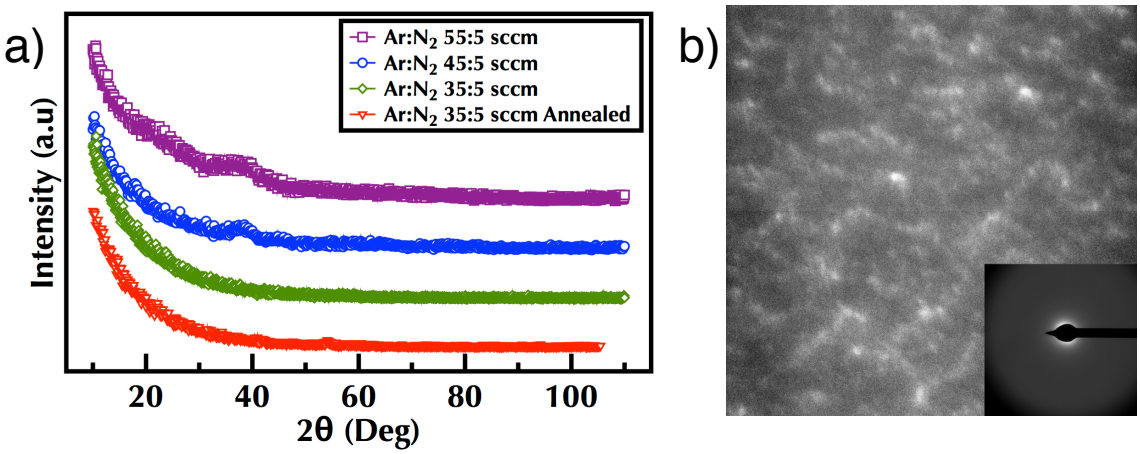

Figure 2-8 | a) XRD different spectrums of WNx sputtered under pressure 5 mTorr with different gases mixture ratio Ar:N2 55:5 to 35:5 sccm plus annealed one; b) TEM image for WNx sputtered under 5 mTorr pressure and gas mixture ratio Ar:N2 35:5 sccm, with TEM diffraction image as an inset.

The next step was to fix the pressure at 5 mTorr and vary the gas mixture ratio to optimize the amorphization process further. Figure 2-8(a) shows the XRD result of varying the mixture ratio by reducing the Ar flow and fixing the N_2 flow until we achieved the most optimal result at ratio of 35:5 sccm (Fig 2-8(b)). At this final condition it was found that the deposited film is quasi-state amorphous with nearly no existence of any crystalline clusters in the test sample.

3. Physical Characteristics of aWN_x

The mechanical strength of the amorphous WN_x film was evaluated using a nano-indentation tool (static load ranging from 300 µN to 4000 µN, with a deflection ranging from 20 nm to 170 nm). The measurement was performed on a 1µm thickness layer of

amorphous WN_x on a silicon substrate to isolate the silicon substrate effect on the measurement. The Young's modulus of the sample was found to be 300 GPa, while the hardness was found to be 3 GPa [97]. These high values of elasticity and hardness together with the grain-less amorphous structure have significant advantage in strengthening NEM switches against stress and deformation. This would eventually reflect a longer operational lifetime and less contact resistance. The existence of nitrogen atoms among the tungsten atoms reduces the tendency of native oxide formation as noted from the four probe sheet resistance measurement. The sheet resistance was 200 μΩ.cm and remained constant being measured just after deposition and again after four weeks exposure in normal ambient air with an average daily humidity of 70% or above. The deposited aWN_x has density, 17.5 g/cm^3. This value lies between the hexagonal crystalline (δ-WN, 18.1 g/cm^3) and cubic crystalline (β-W2N, 16.1 g/cm^3) densities, [98-102]. The deposited film has a slightly tensile stress, 500 MPa, which is advantageous to avoid sagging of the suspended part of the switch, thanks to the strain gradient. All the measured values comply with earlier reported values by others [94, 103].

The surface roughness of the deposited layer of WN_x was characterized using atomic force microscope (AFM) Agilent 5500 SPM using the intermittent contact imaging mode. It was found that the average value of surface roughness is 2.53 nm for a projected area of 64 μm^2. The median value is 2.31 nm with the maximum value of 30 nm and minimum value of nearly 0 nm, Fig 2-9. Both the amorphous nature and the smooth surface of the material yield a reduction of electric discharge phenomenon which prevents micro-welding failure by reducing the amount of energy stored in the active

element of the NEM switch. Some prior works have used a thin oxide layer on the contact surface to limit the current flow and electric discharge by increasing contact resistance, which eventually suppresses the ON current [104]. However, the thin oxide layer wears off during operation cycles causing the switch performance to deteriorate rapidly [16]. In that context, using the developed aWN_x material with its smooth contact surface does not pile up charges at sharp spikes, and further its stronger molecular bonds via closed pack atomic density prevent oxidation [100-102]. Consequently, this helps in achieving a moderate contact resistance to prevent excess charge passage. Additionally, due to the high hardness of aWN_x, the electrode and active element in the NEM switches are highly resistant to ablation and wearing effect.

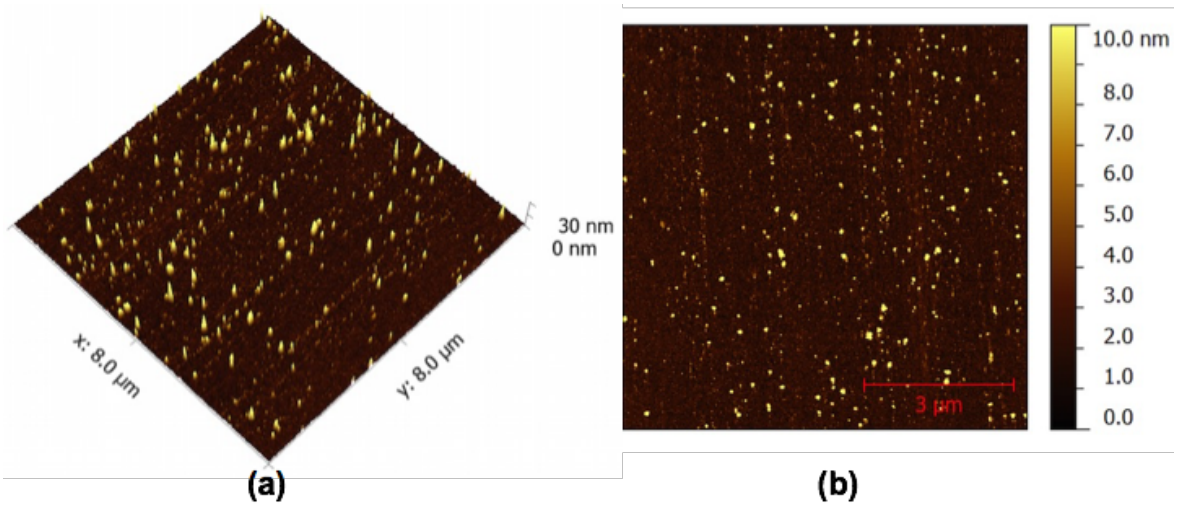

Figure 2-9 | Atomic force microscopic (AFM) images of surface roughness of WN_x a) 3D view for 8 µm × 8 µm area and b) top view for 8 µm × 8 µm area.

The lack of enough mechanical restoring force causes stiction in MEM or NEM devices. Some researchers proposed to use high pull-back voltage at an opposing electrode to overcome the stiction issue [50, 51]. This is not a practical solution as it

needs high voltage operation, slows down the speed and makes the switch unreliable. In contrast, aWN_x with fairly high Young's modulus (300 GPa) reflects high value of spring constant. This gives an adequate mechanical force (F_m) to pull back the active element after removing the electrical pull in force (F_e), thus eliminating the need for pull back high voltage. Other causes of stiction are the van der Waals force as well as the Casimir force [46, 50, 79]. One way to overcome them is to have high enough mechanical force, but not too high that it increases the pull in voltage, as V_{pi} is directly proportional to F_m. Silicon made NEM switches have higher probability for stiction due to their low Young's modulus (about 160 GPa). On the other hand, material with high value of Young's modulus has almost no stiction issue, such as amorphous carbon, carbon nanotube (CNT) and silicon carbide (SiC), where the value is around 700 GPa. Our aWN_x has an intermediate value of Young's modulus which overcomes the stiction issue that exists in silicon based NEM switches and does not require high operating voltage, which is required by carbon based material.

Finally, mechanical failure occurs in NEM switches because of the cluster boundary existence, which can cause fracture, deformation, material fatigue, or all three [101, 105]. The boundaries among the grains are the weakest point in the material (weakest link in the chain) and fractures occur at these boundaries. This defect shortens the lifetime of the device tremendously [24, 95]. Therefore, the material used to fabricate the NEM switches needs to be either mono-crystalline or amorphous to overcome this defect of poly-crystalline material. Since mono-crystalline metal is not possible through

conventional CMOS processes, therefore, amorphous metal such as WN_x can play a critical role.

4. Testing the aWN_x Under Harsh Environment

The aWN_x has been tested in three different simulated harsh environment conditions. These simulations are far more severe than real life harsh environment. The aWN_x film withstood all the experiments, which were as follows:

1. High temperature 750°C under Ar gas flow for 90 min. XRD measurement shows the WN_x film is still amorphous as shown in Fig. 2-10 with an unchanged sheet resistance.

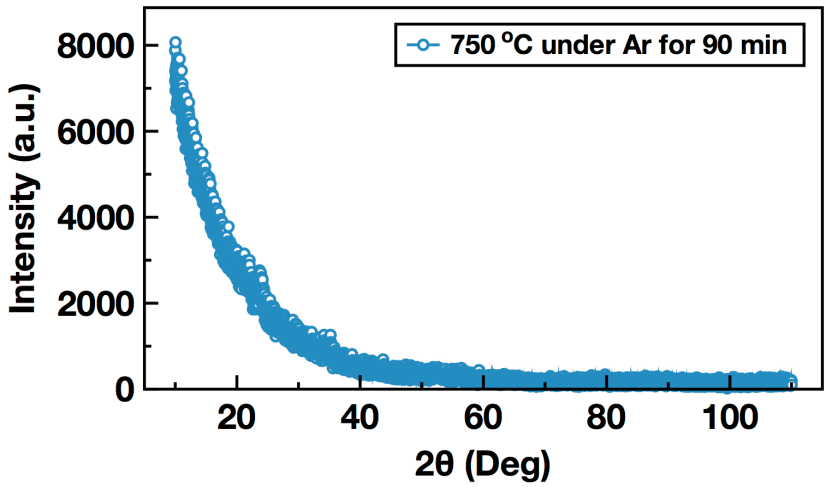

Figure 2-10 | XRD data for the WN_x film after exposing to 750°C with Ar flow.

2. High temperature 750°C under N_2 gas flow for 90 min. XRD measurement shows the WN_x film is still amorphous as shown in Fig. 2-11 with same low sheet resistance as before.

3. High temperature 750°C under O_2 gas flow for 90 min. XRD measurement shows the WN_x film still amorphous as shown in Fig. 2-12. The amorphous metal conductivity degraded slightly, but it is better than silicon. The four point probe test shows low resistivity for the amorphous metal, 3 Ω/□.

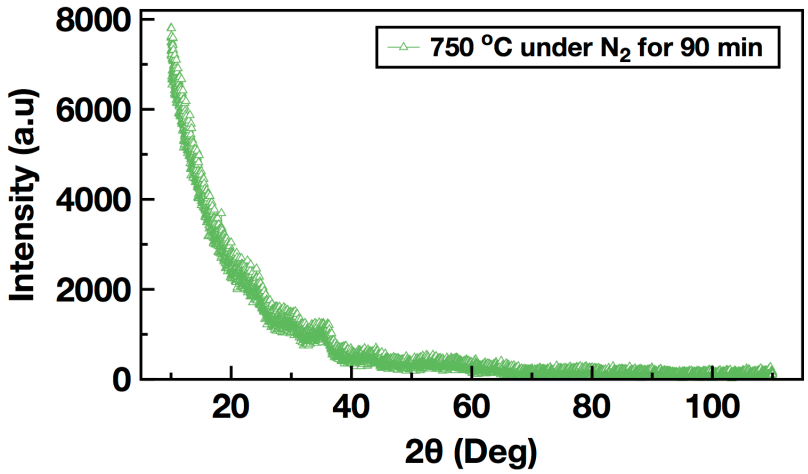

Figure 2-11 | XRD data for the WN_x film after exposing to 500 °C with N_2 flow.

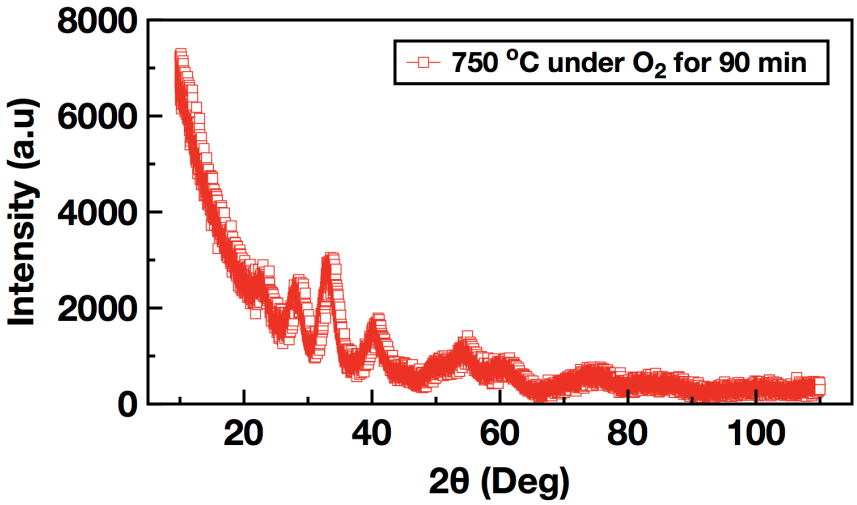

Figure 2-12 | XRD data for the WN_x film after exposing to 500 °C with O_2 flow.

These extreme environment tests confirm that the aWN_x based fabricated devices are harsh environment proof as well as they are remarkably stable at high temperature of

post-processing micromachining. This criterion allows the fabrication of the NEM switches side by side to CMOS elements in hybrid NEMS-CMOS systems during the front end of line (FEOL) process stage. The FEOL process include ion implantation step which demand an annealing step at high temperatures (800-1050°C). Amorphous WNx withstands these elevated temperatures, unlike other materials used for M/NEMS fabrication, which give and advantage of fabricating the NEMS devices at the FEOL process.

5. COMPARISONS BETWEEN WN_X AND OTHER COMMONLY AVAILABLE MATERIALS FOR NEM SWITCHES

Most of the NEM switches are fabricated from polycrystalline silicon material (PSi) with or without an upper coating of a metal layer, mainly gold. Some groups demonstrated side wall coating of hard metal for better contact and electrical characteristics. Other groups fabricated NEM switches in all metal form but polycrystalline metal or different carbon base materials such as SiC or carbon nanotube (CNT). Comparisons between these materials and amorphous WN_x are listed in details in this section. Polycrystalline silicon has been used extensively to fabricate MEM switches, and devices collaborated with a top gold thin film layer. The gold layer helps to overcome the compressive residual stress and improve the conductance of silicon. Polycrystalline structure of silicon is not scalable to nanoscale due to the large grain size of a crystalline cluster in the same range of NEM switch electrodes dimensions which deteriorate the mechanical and electrical property of NEM switches and devices. Different tactics and

method have been used to overcome these issues of polycrystalline to fabricated idea NEM switches. The following table 2-1 demonstrated the cons and pros of different used materials for NEM devices fabrication [22, 91, 106-110]:

Material	Pros	Cons
Poly crystalline Silicon (PSi)	1. Simple fabrication process. 2. Standard process 3. COMS compatible	1. Unscalable to nanoscale. 2. Mechanically brittle 3. Low Young's modulus and hardness. 4. Low conductivity. 5. High roughness surface.
Mono crystalline Silicon (SOI)	1. Simple fabrication process. 2. Standard process. 3. COMS compatible. 4. Scalable to nanoscale.	1. Mechanically brittle 2. Low Young's modulus and hardness. 3. Low conductivity. 4. Too smooth surface cause stiction. 5. High cost of material.
Silicon with side wall metal layer	1. CMOS compatible. 2. Standard process. 3. High conductivity and lower contact resistance. 4. High endurance > million cycles. 5. Moderate Young's modulus and hardness.	1. Complex fabrication process. 2. Layer delimitation issue. 3. Mechanically brittle due to silicon structural layer.
Silicon carbide SiC	1. High temperature endurance. 2. Very high endurance > billion cycles. 3. Very high Young's modulus and hardness. 4. High frequency operation. 5. Moderate resistivity.	1. Not CMOS compatible. 2. Polycrystalline and unscale-able. 3. High pull-in voltage due to high Young's modulus. 4. Hard to micromachine. 5. Not vertical side wall etching.

Material	Pros	Cons
All metal	1. CMOS compatible. 2. Electrically stable device. 3. High Young's modulus hardness and conductivity.	1. Complex fabrication process. 2. Mechanically defect-able due to polycrystalline structure. 3. Unscalable to nanoscale. 4. High roughness surface.
Amorphous Metal (WN_x)	1. CMOS compatible. 2. Electrically stable device. 3. High Young's modulus hardness and conductivity. 4. Easy micromachining. 5. Mechanically stable device. 6. Very high endurance > trillion cycles. 7. High frequency operation. 8. Scalable to nanoscale. 9. High temperature endurance.	1. High density material causes proximity error in EBL. 2. Not vertical side wall etching. 3. High pull-in voltage due to high Young's modulus. 4. Not easy micromachining.

Table 2-1 | Comparisons between aWNx and other materials

6. SUMMARY

Table 2-2 summarizes all the characteristics of the innovated aWN_x. These unique properties of aWN_x make the material perfect for NEM switch fabrication. It overcomes the challenges mentioned in this chapter. Next chapter presents the fabrication process of aWN_x NEM switches.

Property	Value
Young's Modulus, E	300 GPa
Hardness, H	3 GPa
Resistivity, ρ	200 $\mu\Omega$·cm
Density, ρ_m	17.5 g/cm^3

Table 2-2 | aWN_x characteristics.

Chapter 3

NEMS Design And Simulations

1. Introduction

Although MEMS concept was started 50 years ago in 1964 (when the sacrificial layer technique started), the first electrostatic based MEM switch was not fabricated until 1990. The progress in this field was not as aggressive as it was in CMOS and MOSFET, Fig. 3-1.

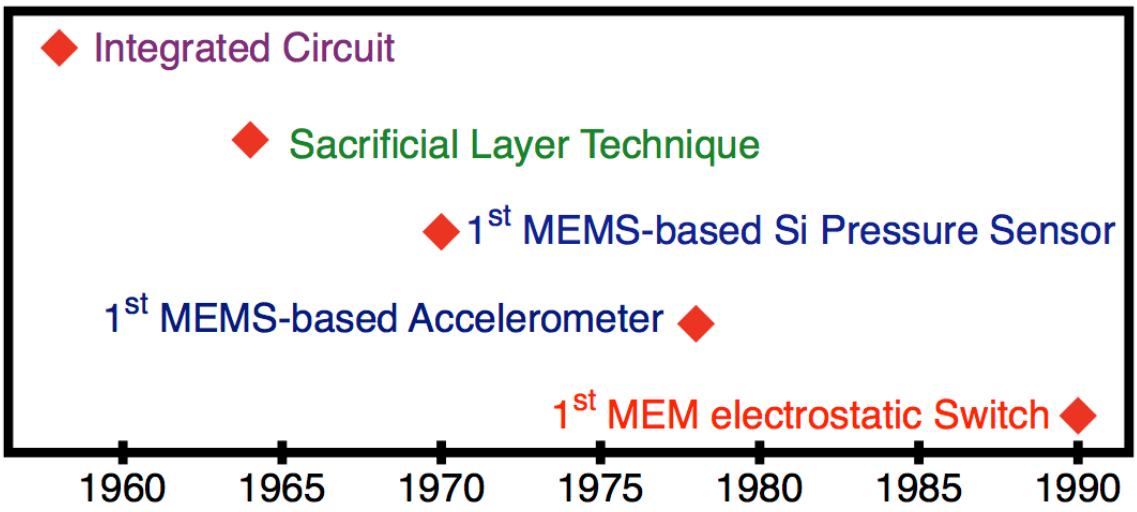

Figure 3-1 | MEMS technology time line.

Amorphous WN_x has unique characteristics which make it a promising material for NEMS fabrication. Following characterization of the aWN_x, the values of Young's modulus, hardness, and density were used to design NEM switches with different dimensions and geometries. The theoretical pull-in voltage (V_{pi}) was both calculated and

simulated. The goal was to obtain the first ever 3 terminals NEM switch that has a sub-1 volt value for V_{pi}.

This chapter is divided into three major sections: (i) the theoretical calculations for vertical and lateral NEM switches using several different geometries; (ii) the computer aided simulation of two designs using COMSOL™ and (iii) summary of the final design according to the calculations and process boundaries.

2. NEMS CONCEPT AND THEORETICAL CALCULATIONS

For device design, the length of the active element (cantilever) of the NEM switch has two effects: shorter length results in faster operation speed, and longer length results in lower pull-in voltage. Both the speed and the pull-in voltage are directly proportional to the Young's modulus and cantilever thickness; and are inversely proportional to the length of the cantilever [72, 111]. Therefore, an optimal design is to reduce all the dimensions of the NEM switch except the cantilever length, leading to reduction of pull-in voltage and increment of the quality factor and resonant frequency. The switching speed increases as the pull-in voltage decreases. Hence, high Young's modulus and nano-scale dimensions are desired for optimal NEM switch fabrication. Therefore, designs have been developed for three different sizes, starting with large dimensions (sub-micron) with pull-in voltage around 10 volts down to nanoscale dimensions to achieve the sub-1 volt pull-in voltage. The calculations are based on the material parameters of aWN_x, which have been characterized earlier in this thesis. The relevant material parameter is the Young's modulus (E) and other parameters come from the design dimensions. NEM

switches are categorized into two main categories, lateral and vertical. The cantilever of the lateral design moves in the direction of the plane parallel to the substrate. On the other hand, the cantilever of the vertical design moves out of the plane perpendicular to the substrate. The following subsections will talk about the different kinds of NEM switches in detail.

3.2.1 Lateral Design NEM Switches

Fabrication of a lateral NEM switch is simpler than a vertical one because it is a single mask process. However, the lateral NEM switch demands a sub-micron lithography process. The cantilever can be singly clamped (from a single side, Fig. 3-2) or doubly clamped (from both sides, Fig. 3-3). Beside the cantilever, either clamped at one side or both sides, there is a static island called gate (G) and static electrode called drain (D).

A potential difference is applied between the cantilever and the gate to generate an attractive electrostatic force *(F_e)* which pulls the cantilever towards the gate and makes contact with the drain, Fig. 3-2(b). As the cantilever moves towards the gate, when it reaches one-third of the initial gap distance between the cantilever and gate, the cantilever will *fall* towards the gate, Fig. 3-2(a-d) [112-114]. This distance is called the pull-in distance and the voltage required to move the cantilever to this point is called the pull-in voltage (V_{pi}).

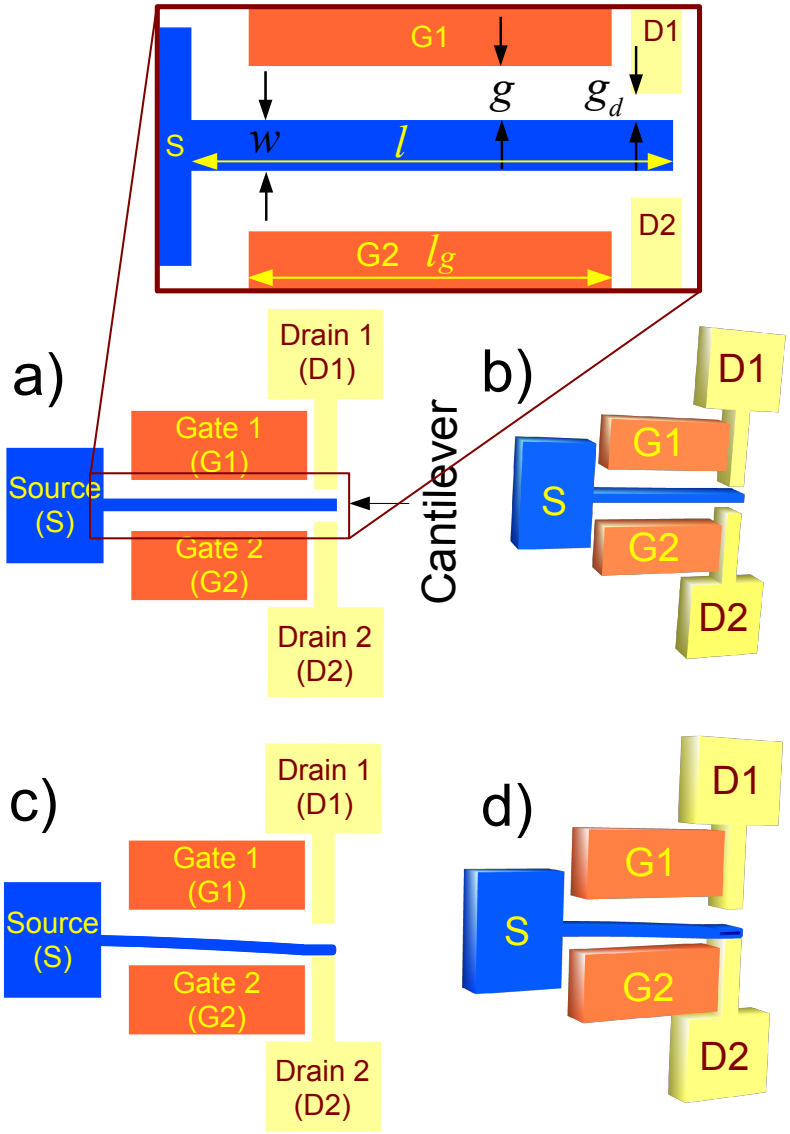

Figure 3-2 | Single clamped NEM switch. a) top view schematics of an idle position (inset: symbols guide), b) 3D view of an idle position, c) top view schematics of an actuated position, d) 3D view of an actuated position.

To ensure that the cantilever makes contact with the drain, the drain should not be separated from the cantilever more than the pull-in distance, otherwise the system might collapse when instead the cantilever makes contact with the gate, Fig 3-4. In the case of a singly clamped cantilever, the drain will be located at the free end of the cantilever (Fig.

3-2(a-c)); and in the case of a doubly clamped cantilever, the drain will be located in the middle of the cantilever (Fig. 3-3).

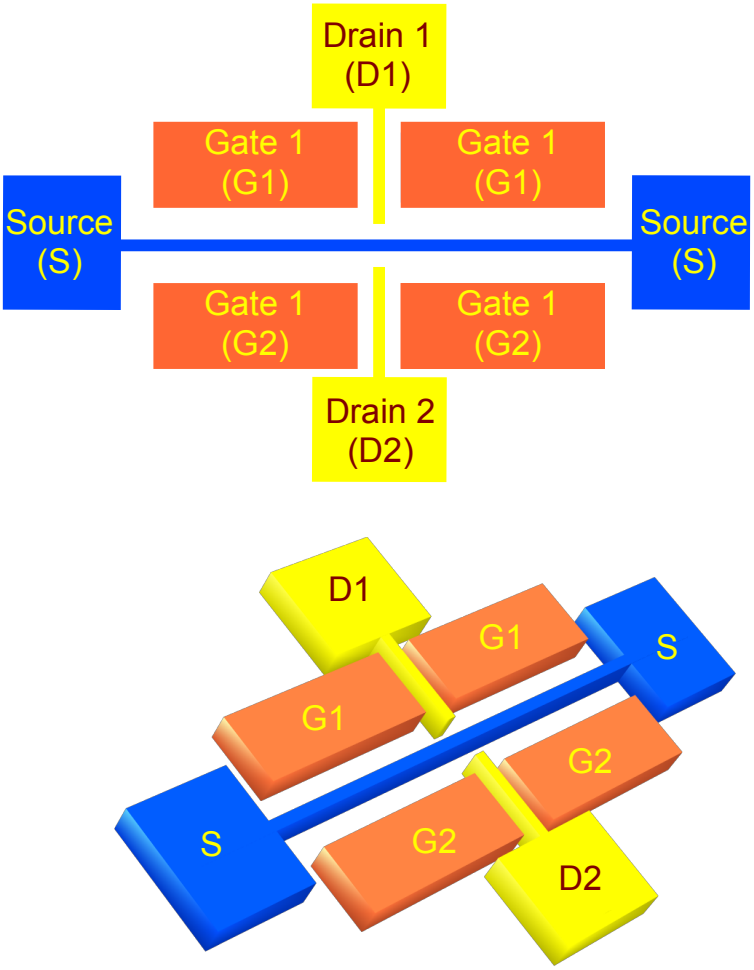

Figure 3-3 | Double clamped NEM switch; upper: top view; lower: 3D layout.

The Fig. 3-2(a) inset shows the NEM switch enlarged layout with the symbols guide. The potential difference between gate and cantilever (source) is called gate voltage (V_g).

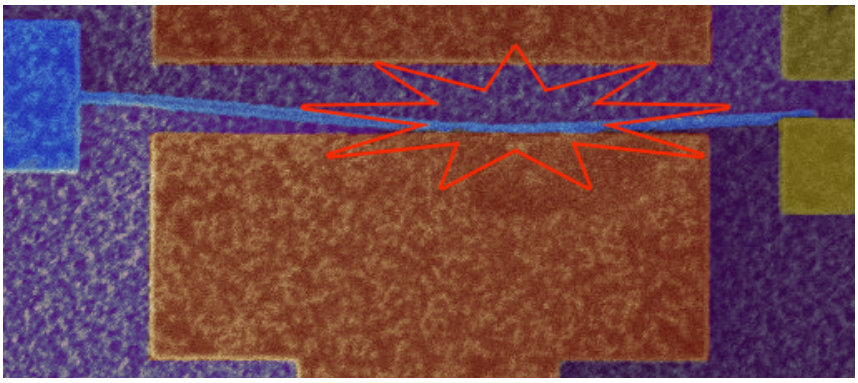

Figure 3-4 | SEM image of a collapsed NEM switch.

The applied V_g induces opposite polarity charge on the facing side of the cantilever. Consequently, this opposing polarity of charges generates electrostatic force (F_e) which pulls the cantilever toward the gate, according to the following formula:

$$F_e = \frac{1}{2}\frac{CV^2}{d_o} \qquad (1)$$

where

d_o: distance between cantilever and gate; sometimes called the gap (g).

V: potential difference between cantilever and gate.

C: capacitance.

As the cantilever starts moving, there will be a mechanical counter-force (F_m) generated by the cantilever material directly proportional to the spring constant of the cantilever material Fig 2-2(b). The force could be calculated by the following expression:

$$F_m = k \cdot d \qquad (2)$$

Spring constant (k) should be calculated using the formula of distributed pressure instead of the point load pressure for lateral NEM switches which is [115]:

$$k = \frac{2Etw^3}{3l^3} \quad (3)$$

where

E: Young's modulus.

d: cantilever tip distance travel.

l: cantilever length.

w: cantilever width.

t: cantilever thickness.

k: spring constant.

The V_{pi} is calculated by the following formula.

$$V_{pi} = \sqrt{\frac{8kd_o^2}{27C_g}} \quad (4)$$

$$d_{pi} = \frac{d_o}{3} \quad (5)$$

where

d_o: the gap between cantilever and gate; sometimes called (g).

l_g: gate length.

C_g: Capacitance between the cantilever and the gate.

ε: the permittivity of the gap dielectric.

The pull-in distance (d_{pi}) is measured from the moving side, which is the cantilever side. This phenomenon adds some challenges in NEMS fabrication because it dictates to ensure the gap between the cantilever and the drain (g_d) does not exceed one-third of the initial distance between the cantilever and the gate gap (g) [22]. From the expression above it is clear that varying the dimensions will directly affect the V_{pi}. It is observed by Prof. Philip Wong's group at Stanford University that the operational value of V_{pi} is 40% lower than the calculated value due to fringing field [116]. This assumption turned out to be true in our work as well (the reduced pull-in voltage called Adjusted V_{pi}). For sub-1 volt NEM switches, the dimensions must be in the nano regime. Lateral NEM switch is simpler to fabricate than a vertical one because it needs only a single layer mask. The requested nanoscale could be reached by a deep ultraviolet (DEV) or electron beam lithography (EBL) tool. In this work, EBL has been used to fabricate the NEM switches because of the short turnaround time from design to fabrication.

There is also a shorten formal to calculate V_{pi} as illustrated by another group as follow [115]:

$$V_{pi} = \sqrt{\frac{1.72}{\alpha_2}} \qquad \text{4a}$$

$$\alpha_2 = \frac{6\varepsilon l^4}{Et^3 g^3} \qquad \text{4b}$$

where α_2 is a constant calculated by the above formula.

This value is an excellent approximation for single clamped cantilever MEM/NEM switch under the condition that there is no curvature in the beam, the gate electrode length equal to the cantilever length and width of the cantilever should not exceed 5X of the gap. The calculated results for the first design, with relatively large dimensions, are shown in Table 3-1. This device was actually easily fabricated and faced no issues in lithography and etching. These results will be explored more in the next chapter on fabrication and characterization.

Dimensions	Value
l	16 μm
l_g	14 μm
g	740 nm
w	200 nm
V_{pi} **(Theoretical)**	19.45 volts
V_{pi} **(Adjusted)**	11.67 volts

Table 3-1 | Pull-in voltage values for lateral NEM switch with large dimensions

Smaller devices have been designed to reach lower pull-in voltage as listed in Table 3-2. After fabricating the large dimensions NEM switch, we fabricated a smaller device in order to get a lower pull-in voltage. However, reducing the gaps between cantilever and gate as well as cantilever and drain was difficult and it took a very long time before we got a functional device. The issues and difficulties will be discussed in detail in the next chapter.

Dimensions	Value
l	11 μm
l_g	9 μm
g	170 nm
w	170 nm
V_{pi} (Theoretical)	3.67 volts
V_{pi} (Adjusted)	2.20 volt

Table 3-2 | Pull-in voltage values for lateral NEM switch with small dimensions

The design dimensions and calculations made for NEM switch with targeted V_{pi} of less than 1 volt are listed below in Table 3-3:

Dimensions	Value
l	14 μm
l_g	12 μm
g	200 nm
w	140 nm
V_{pi} (Theoretical)	2.11 volt
V_{pi} (Adjusted)	1.27 volt

Table 3-3 | Pull-in voltage values for targeted V_{pi} < 1 volt lateral NEM switch with small dimensions

3.2.2 Vertical Design NEM switches

Vertical NEM switches require more steps of fabrication process than lateral NEM switches. A single mask is not enough to fabricate a three terminal vertical NEM switch, the process demands multiple masks, a minimum of three masks are required. One mask is for gate and drain, another mask is for the dimple, and the last mask is for cantilever,

Fig 3-5. The three masks process is very tricky as a planarization step is needed after depositing the sacrificial layer above the gate and drain. Without planarization for the sacrificial layer, the cantilever will follow the profile of the underlying layers as demonstrated in Fig. 3-6. A non-straight cantilever profile limits the operation and the lifetime of the NEM switch. To avoid the topography and different layers contour, a two terminal vertical NEM switch is considered in this thesis. The substrate will act as the gate, and a top structure will act as the cantilever (source), Fig. 3-7. This design is used for endurance test in Chapter 5.

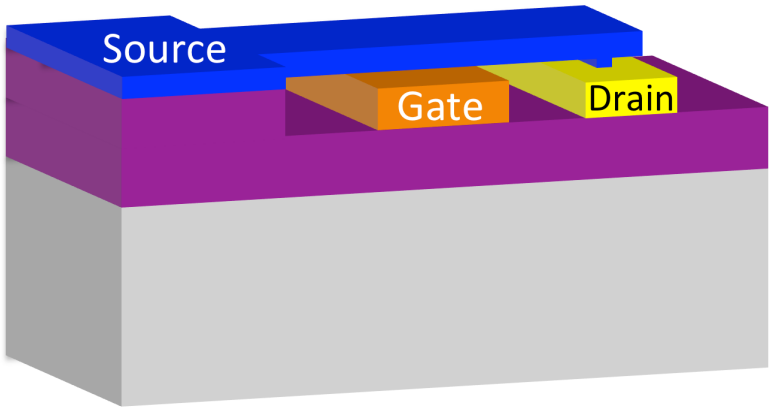

Figure 3-5 | Three masks for vertical NEM switch fabrication: 1) gate and drain, 2) dimple 3) cantilever.

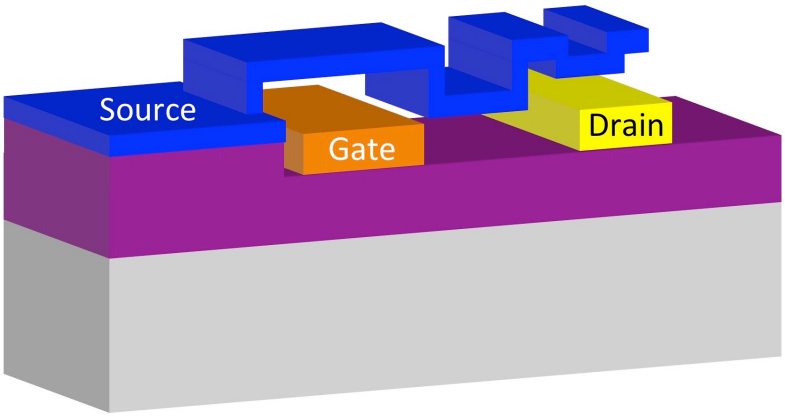

Figure 3-6 | Vertical NEM switch where the cantilever follows the same profile as underlying layer.

The fabrication of vertical switches does not need EBL because the critical dimensions are the thickness of the cantilever and the gap between the cantilever and the gate. The layer deposition tool controls these two variables, not the lithography step. Contact aligner with broad ultraviolet (BUV) lamp could be used for the lithography process to fabricate vertical NEM switches. The dimensions of gate, drain, dimple and cantilever are in the range of microns, but the thickness of the cantilever (t) and the sacrificial layer (g) are in the range of nanometers. Vertical NEM switches have a high possibility of sagging and stiction because of the large structural area compared to the thickness.

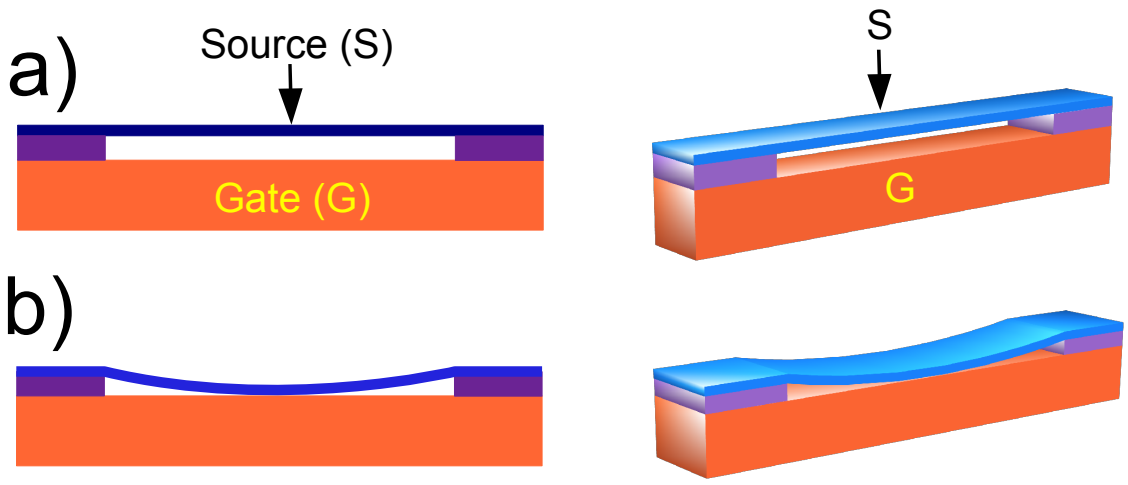

Figure 3-7 | Two terminal vertical MEM switch; a) at idle position; b) at actuation position.

The vertical NEM switch dimensions that this thesis considers in design and fabrication are listed below, Table 3-4.

Dimensions	Vertical NEMS 1	Vertical NEMS 2
l	15 μm	10 μm
g	200 nm	200 nm
t	150 nm	150 nm
V_{pi} (Theoretical)	1.2 Volt	2.6 volt
V_{pi} (Adjusted)	0.7 Volt	1.6 volt

Table 3-4 | Vertical NEM switch dimensions and pull-in voltage values.

3. NEM Switch Simulation by COMSOL™

In the previous sections, three different dimensions of lateral NEM switches and two vertical NEM switches have been investigated starting from a relatively large one to small one. In this section, the medium and the small size NEM switches were simulated using COMSOL™ to validate the chosen dimensions for fabrication. The theoretical calculations consider only the facing plates capacitance, however at the nano-scale, the side and the stray capacitance are significant. The simulation considers all the capacitance not only the facing plates, and should result in a lower Vpi.

Parameter	Value	V_{pi} (Simulated)	V_{pi} (Theoretical)	V_{pi} (Adjusted)
l_g	14 μm	2.4 volts	2.11 volts	1.27 volts
g	200 nm			
w	140 nm			
l_g	9 μm	4.35 volts	3.67 volts	2.20 volts
g	170 nm			
w	170 nm			

Table 3-5 | Lateral NEM switch dimensions and pull-in voltage results.

It is observed from Table 3-5 that the V_{pi} simulated values are higher than the theoretical calculated values. The V_{pi} voltage is a mathematical singular point in the solution, which causes a mathematically unstable operation within the simulation. When the simulation reaches this point, it gives error messages and stops the process. Therefore, it is necessary to make the simulation around the V_{pi}, value which will yield an appropriate approximation to the V_{pi}, [113, 117, 118].

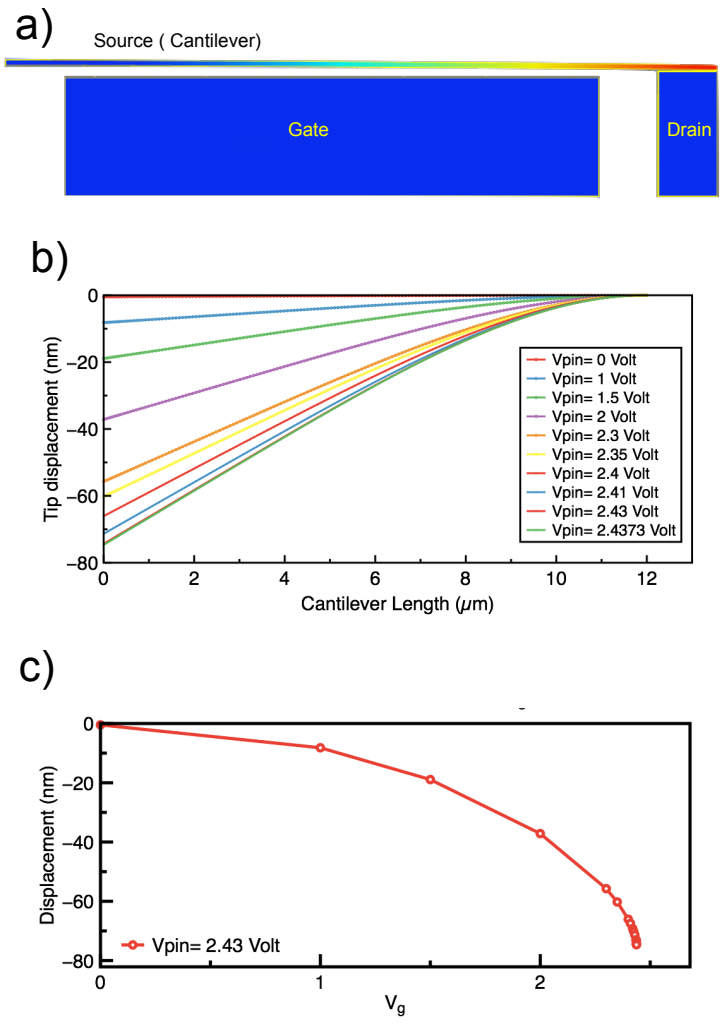

Figure 3-8 | COMSOL™ simulation for the small size NEM switch, a) 3D picture, b) multiple deflection profiles at various V_g, c) the cantilever end deflection distance at various V_g.

Fig. 3-8(a) shows 3D device layout of the simulated NEM switch. The figure shows the position of deflected cantilever at the drain. Fig. 3-8(b) shows the cantilever deflection profile for multiple gate voltages (V_g). The deflection distance of the beam is directly proportional to the applied gate voltage. When the V_g value approaches the V_{pi} the deflection distance increases rapidly until the cantilever falls on the gate or on the drain at V_g equals V_{pi}. Fig. 3-8(c) shows the free end of the cantilever versus the V_g variation. The free tip of the cantilever follows the same scenario of the cantilever profile in Fig. 3-8(b). This value of V_g is just prior the pull-in where the switch becomes unstable, and the simulation software (COMSOL™) gives an error message (reach the boundary pole). Fig. 3-8(b, c) shows that the V_{pi} equals 2.4 volts. Vertical NEM switch has been simulated by COMSOL as well for the cantilever length 12 μm and the outcome is presented in Fig 3-9.

4. SUMMARY

The operation of NEM switches has been discussed, and formulas for calculating theoretical pull-in voltage have been presented. Different sized NEM switches have been suggested for both lateral and vertical design. The corresponding pull-in voltages have been calculated. Starting with lateral NEM switches, the size of the first design was large and resulted in a pull-in voltage of 9 volts. A smaller device gave a pull-in voltage of 1.8 volts. Finally, the smallest one achieved the goal of a sub-1 volt pull-in voltage. For vertical NEMS, two dimensions have been investigated and the smaller one yielded a

sub-1 volt pull-in voltage. The summary of the design dimensions and pull-in voltages are listed in Table 3-6.

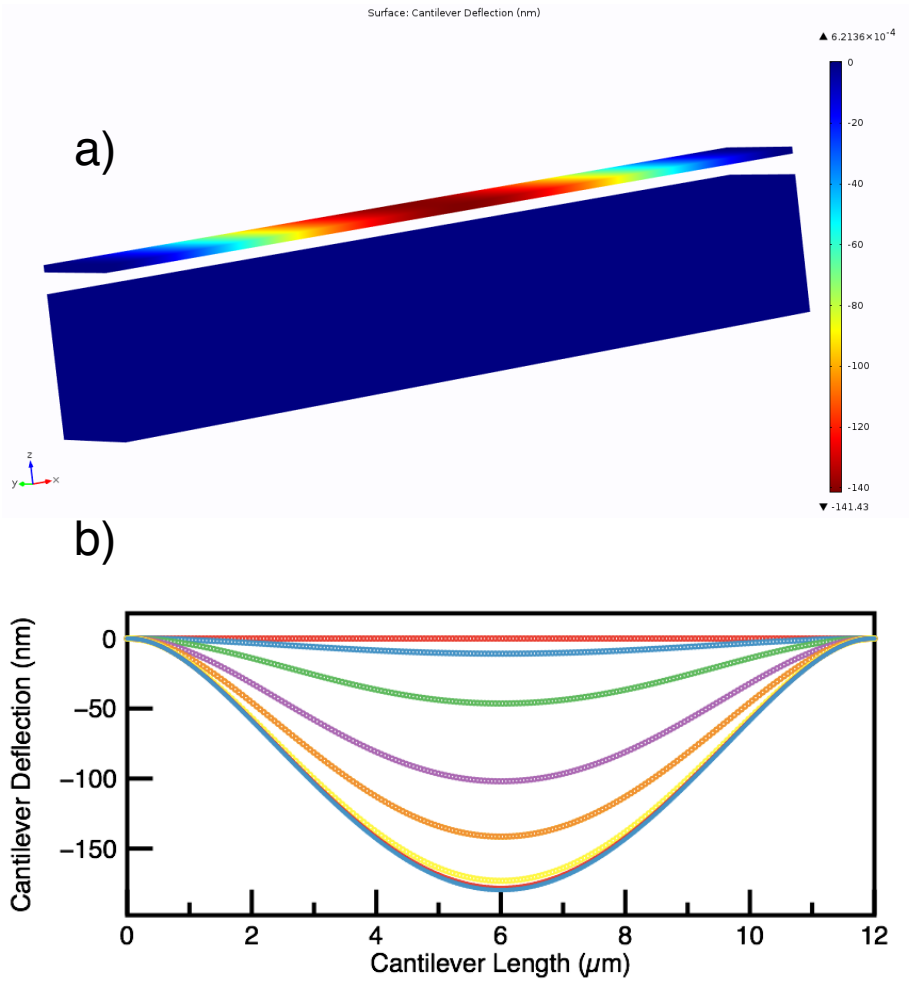

Figure 3-9 | COMSOL™ simulation for a vertical NEM switch a) 3D picture, b) multiple deflection profiles at various V_g.

The following two chapters will show and discuss the fabrication and experiment analysis of NEM switches. Chapter 4 will discuss in details the 3-terminals lateral NEM switches and chapter 5 will discuss the 2-terminals vertical NEM switches. In addition, chapter 5 will show high endurance test and device dissolution experiment.

Dimensions	L-NEMS 1	L-NEMS 2	L-NEMS 3	V-NEMS 1	V-NEMS 2
l	16 μm	11 μm	14 μm	15 μm	10 μm
l_g	14 μm	9 μm	12 μm	15 μm	10 μm
g	740 nm	170 nm	200 nm	200 nm	200 nm
w	200 nm	170 nm	140 nm	150 nm	150 nm
V_{pi} (Theoretical)	19.45 volts	3.67 volts	2.11 volts	1.2 Volt	2.6 volt
V_{pi} (Adjusted)	11.67 volts	2.20 volts	1.27 volts	0.7 Volt	1.6 volt
V_{pi} (Simulated)	N.A.	4.35 volts	2.1 volts	NA	NA

Table 3-6 | Summary of lateral NEM switch dimensions and corresponding pull-in voltage.

Chapter 4

LATERAL NEM SWITCHES FABRICATION AND CHARACTERIZATION

1. INTRODUCTION

Lithography is the most dominating constraint and the bottleneck in semiconductors fabrication. In general, lithography accounts for around 35% of total process steps. Fabrication of the lateral NEM switches requires an advance lithography tool that can expose feature sizes in the nanometer regime. This could be done by either EBL or deep ultraviolet (DUV) lithography tools [77]. The DUV tool needs a special kind of mask called reticles to project the design on silicon substrate. These reticles must be outsourced, and the simulation software is not available in-house to check the designs before fabricating the reticles. In addition, fabrication of a sub-100 nm structure using the DUV lithography tool requires complex techniques such as phase shift masks, immersion, double exposure and double patterning [119]. Sidewall spacers could be a route to creating small gaps with less difficult lithography. The following Fig. 4-1 shows the progress in optical lithography throughout the recent years.

Due to the limitation and complication of the optical lithography, this research is conducted using EBL system. EBL is much superior in making fine feature sizes sub-100 nm, but it has its limitations, such as: very slow, low throughput, and high proximity error

due to forward and backward scattering electrons (Fig. 4-2). The figure below shows the scattering electron trajectory calculated using Monte Carlo simulation [120]. This scattering could cause severe issues in exposing fine feature sizes. As the accelerating voltage increase, the scattering electron area increases (the EBL used in this thesis has 50 kV acceleration voltage). All these limitations introduced high challenges in the NEMS fabrication process. Many experiments have been conducted to optimize the exposure conditions to achieve the smallest feature size.

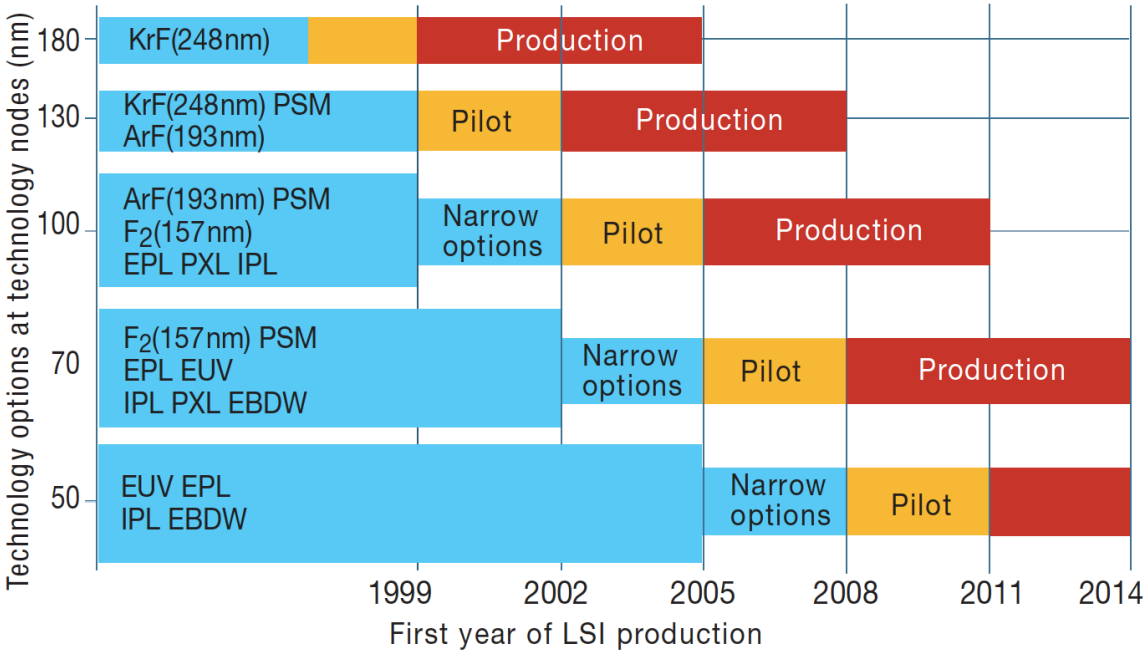

Figure 4-1 | The UV light source for lithography [119]

Lithography by EBL could reach very small feature size around 30 nm (has been successfully exposed by the researcher). The issue is that the cantilever is a thin structure lying beside or between two large structures, which are the gates. Plus the gap between the cantilever and the drain must be ⅓ of the gap between the gate and the cantilever. This is way beyond the EBL capabilities [120]. Another issue is that the EBL is a shared

tool and most of the users are using low sensitivity positive photo resist (PPR) which demands high current exposure. NEM switch fabrication process demands high sensitivity negative photo resist (NPR) which needs low current exposure. The tool needs a long time (more than 4 hours) to stabilize the e-beam when changed from high to low current. Additionally, tungsten has a much higher atomic number than silicon, which causes more backscattered electrons. Amorphous WN_x has a shorter mean free path than a crystalline structure, which also generates more backscattered electrons. Proximity is the killing error for EBL process to fabricate NEM switches.

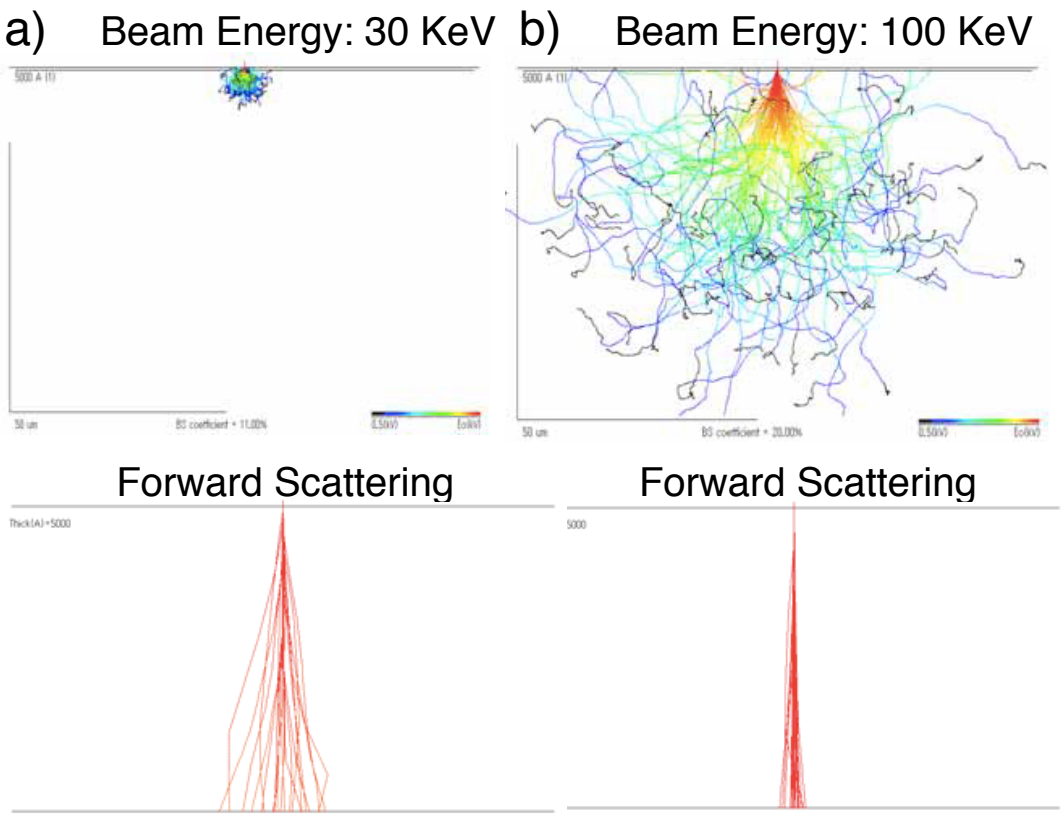

Figure 4-2 | Electron beam scattering and energy distribution profile [120].

2. LATERAL NEM SWITCHES FABRICATION

Four different process recipes have been conducted and will be discussed. These recipes are standard recipes in most semiconductor fabrication industry. The following Fig 4-3 shows SEM pictures of different NEM switches fabricated with following recipes: (i) top-down process without hard mask (HM), (ii) top-down process with HM, (iii) bottom-up process and (iv) hybrid process between top down and bottom up process. These processes are discussed in detail in the following section. The most successful recipes were the top-down process with hard mask and the top-down process without hard mask, Fig 4-3(a,b). The other two recipes were not successful due to large stringers at side edge of the structure and over exposure. The side edge stringers in bottom-up process (looks like ears) deteriorate NEM switch operation as in Fig 4-3(c). The hybrid process overcomes this issue of stringers but has issue of overexposing the fine features and gaps, Fig 4-3(d).

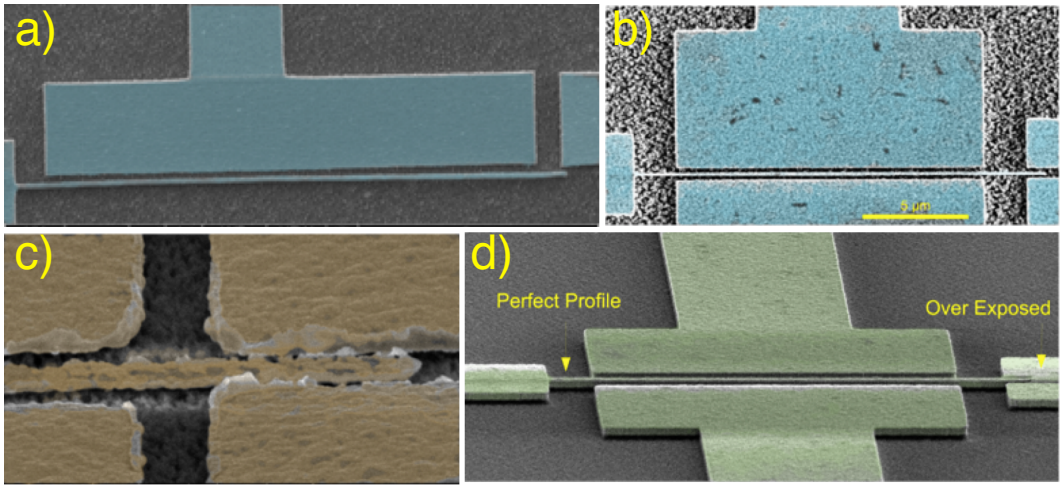

Figure 4-3 | SEM image for NEMS fabricated by different processes; a) top down without HM, b) top down with HM, c) bottom up, d) hybrid.

Therefore, this thesis will explore the top down processes in full details and pass over the other two processes in brief explanation.

4.2.1 Top-Down Process Without Hard Mask

In top-down process, the materials of interest are deposited and will be micromachined to reach the desired structure and layout [24, 121]. The process starts with a high conductive Si substrate followed by deposition of 2 μm thick silicon dioxide (SiO_2) using plasma enhanced chemical vapor deposition (PECVD). The quality of this layer is not as good as thermal silicon oxide, however, it is faster to etch during the release step to avoid long exposure of aWN_x to hydrofluoric acid (HF). Next, the substrate is placed in sputtering tool for depositing the amorphous WN_x on top of the SiO_2 by physical vapor deposition (PVD). The aWN_x layer has been deposited with two different thicknesses; one is 300 nm for faster operation devices and the other is 500 nm for higher current flow devices. Then, the complete substrate is coated by a negative photo resist (NPR). Many types of NPR have been used throughout the experiments. Fig. 4-4 shows the process flow steps. This process is without using a hard mask (HM). To avoid using a HM, a rigid and high etch resistant resist must be used to withstand the aggressive gases used for etching. Therefore, the resist SU8 has been used after diluting to achieve thicknesses of 300 to 500 nm after coating and baking. For nano-size structure, the resist thickness must not exceed 3X the minimum feature size [122, 123]. This process steps are as follow:

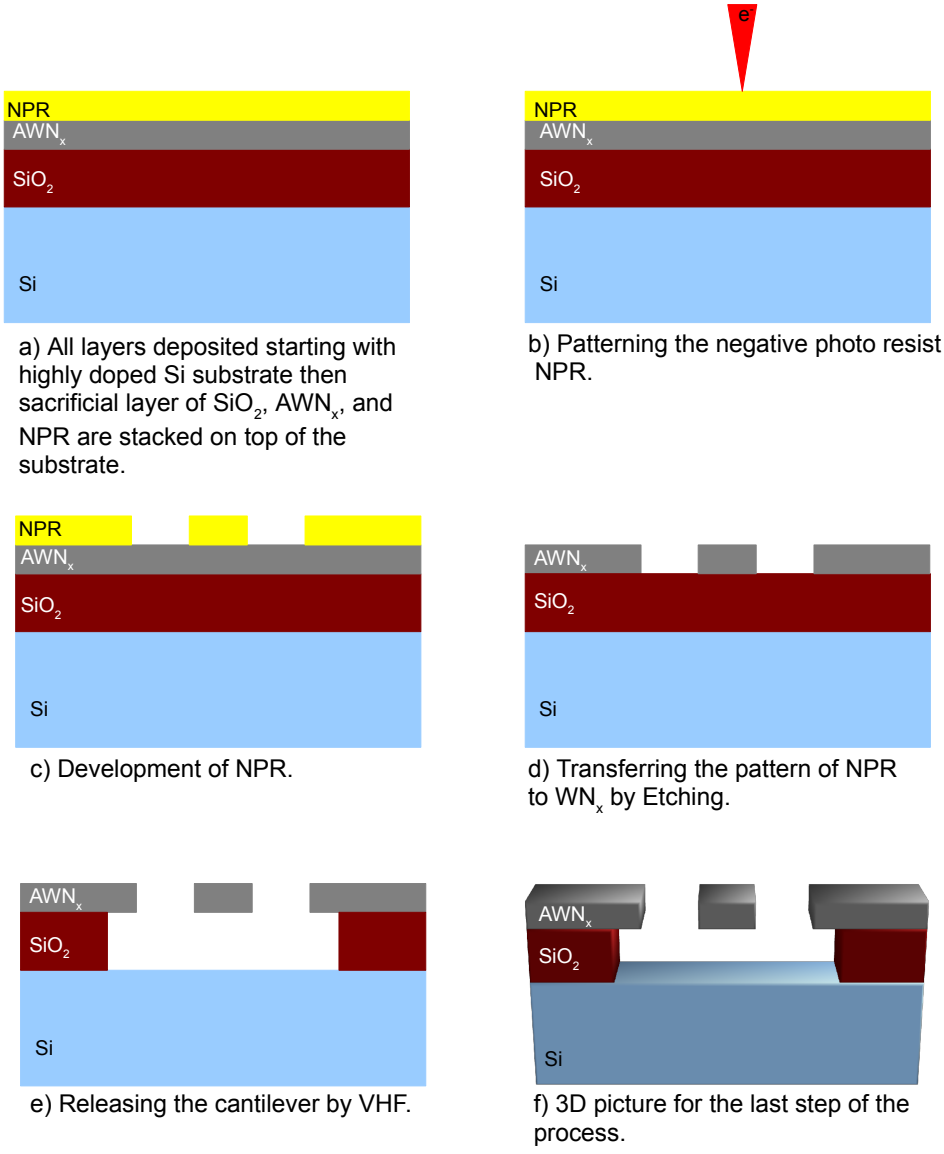

Figure 4-4 | The process steps for top down process without hard mask.

1. Deposition Stack of Layers

Start with <100> orientation silicon substrate cleaned in piranha solution to remove all the residuals polymers and impurities. Then deposit 1 to 3 μm film of SiO_2 by PECVD tool. The PECVD oxide is more desired than furnace oxide (FOX) because it has a faster

deposition and release time than the FOX due to its weaker bonds. Amorphous tungsten nitride (aWN_x) of 100 to 500 nm thickness film is deposited with the same recipe as explained in chapter 2. The deposited layer internal residual stress is slightly tensile stress, less than -500 MPa, so there is no need for annealing [124].

2. SU8 Resist Coating

SU8 resist is available commercially with high viscosities, which are suitable for coating thick layers, from 2 μm up to 100 μm. It is considered as an epoxy rather than NPR. The benefit of SU8 is its high resistance to etching and high sensitivity for Ebeam exposure (more than 50 $\mu C/cm^2$). This sensitivity has been characterized experimentally because the suppliers of SU8 do not declare it as Ebeam compatible resist and do not supply the needed information for EBL process. The SU8 needs to be diluted to have 300 - 500 nm thickness [125, 126]. For better adhesion and higher aspect ratio (AR) for SU8 resist, it is better to perform a post-exposure baking (PEB) at 95° to 100° C for one minute to dehumidify the substrate (as SU8 is very sensitive to water and humidity). Then the substrate could be diced or cleaved manually for EBL exposure. It is better to cleave the substrate after the resist coating to maintain the uniformity of the resist coating [122].

3. EBL Exposure

This step is the most critical part of the entire thesis. Patterning the photoresist (PR) with nanostructure is a very sensitive and not easy task. This step consumed a very long time to achieve sub-100nm structures. This fine structure is the foundation for the sub-1

volt devices. Ebeam tool has four variables that directly affect the minimum size of the pattern exposure on PR. These variables are as follows:

- Electron beam high voltage accelerator (this is fixed by the supplier).
- Exposure flashes density per die.
- Electron beam current.
- Dwell time, exposure time.

The first variable is fixed and not allowed to be changed. The last three variables are accessible by users. The existing Ebeam tool in KANF has no proximity correction software which causes proximity error and over exposure for dense areas and under exposure to sparse areas. To overcome this issue, the design should take care of this issue manually however it consumes a very long time in trial error phase to get the best exposure parameters. The proximity error is generated by the scattered electron at exposure time (Fig. 4-2) [88, 91, 120, 122, 127, 128].

Low current intensity is recommended for nano-size pattern exposure as expressed in equation number 6. Therefore, a high sensitivity PR should be used for structure pattern exposure in short time.

$$d_p = \sqrt{\frac{4 i_p}{\beta \pi^2 \alpha_f^2}} \qquad (6)$$

where:

d_p : electron beam spot diameter

i_p : current intensity

β : beam brightness, which is proportional to acceleration voltage.

α_f : the convergence angle of Ebeam.

For SU8 the best exposure conditions were found as follow:

- Dwell time: 0.30 µS.
- Fine feature dwell time should be doubled and the surrounding to be reduced to 10% to overcome the proximity error.
- Exposure current is 50 pA.
- Exposure flashes density is 60,000 dots / 1,200 µm die size.

Develop the resist with the standard SU8 developer. After development, the substrate must be rinsed by IPA. Never use water, because SU8 is water dissolvable. There is also no need for post-exposure baking (PEB) as it will cause over exposure.

4. Etching the Amorphous WN_x

Tungsten is a transition metal and it is not easily etched, like most metals. Only a few gases are capable of etching tungsten, such as Cl_2, SF_6 and CF_4 [88, 124, 127, 129, 130]. The gas CF_4 causes polymer residuals at the side wall, therefore, it is not recommended to be used for lateral NEM switch fabrication. The gas SF_6 was selected and the etching recipe is as follows:

- SF_6/Ar : 15/5 sccm
- Pressure 20 mTorr.
- Power: ICP 1000 W, platen 50 W.
- Temperature: 10° C.

The etching rate is around 80 nm/min. The gas ratio is very aggressive and etches the PR faster than the metal. Therefore, the metal thickness cannot be greater than the PR thickness. The maximum thickness of the PR should not exceed 3X the minimum feature size; otherwise the structure of the patterned PR will not be stable and fall, as shown in Fig. 4-5. Due to the limitation of the metal thickness that can be etched, the hard mask (HM) concept has been considered and will be discussed in the next section.

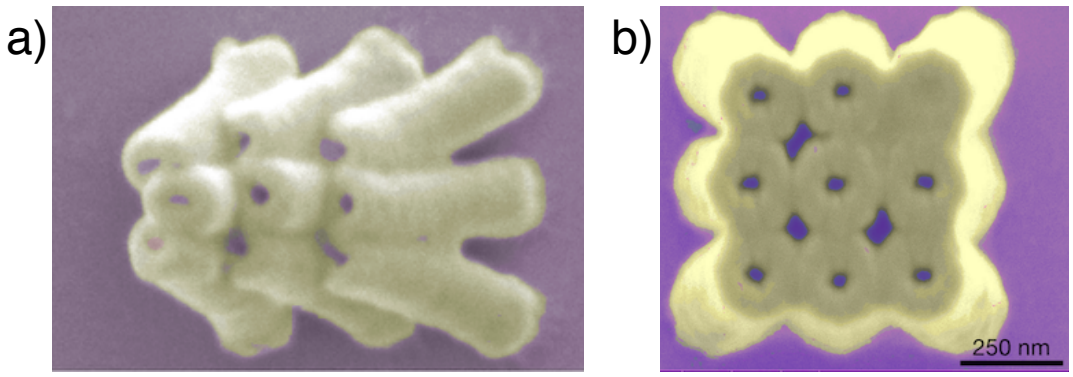

Figure 4-5 | Fallen down SU8 patterned structure due to very high AR a) tilted view, b) top view.

5. NEMS Release

After etching the metal, which is the main part of the NEM switches, the substrate is ready for NEMS release. There are two ways to release the device, either by liquid hydrofluoric acid (HF) or by vapor hydrofluoric acid (VHF) method. The use of liquid HF requires a special drying method to avoid stiction. For this reason, critical point dryer (CPD) is used. The liquid HF releases the device fully and makes the area beneath the released part very smooth, with very low residuals of SiO_2 or roughness. The disadvantage of this method is that it requires a long drying time by CPD, and the probability of stiction is high. The VHF method is easier and safer because there is no

submersion of the substrate into the acid. The process is to expose the substrate to the vapor HF at 40˚ C. This method leaves some residuals and roughness beneath the released part. The stiction probability is low, but the probability of not achieving full release is high. Fig. 4-6 shows the substrate after release by each method.

The process for releasing the NEMS device by liquid HF:

1. Submerge the substrate into the liquid HF for 15s.
2. Submerge the substrate into DI water for 1 to 2 min.
3. Submerge the substrate in 3 baths sequentially:
    i. Methanol/DI water: 20/80
    ii. Methanol/DI water: 50/50
    iii. Methanol/DI water: 80/20
4. Submerge the substrate in methanol in the CPD to dry it out.

The process for releasing the NEMS device by VHF is simple, just place the sample in the chamber for the needed time at 40° C. The lateral etching rate is about 50 nm/min.

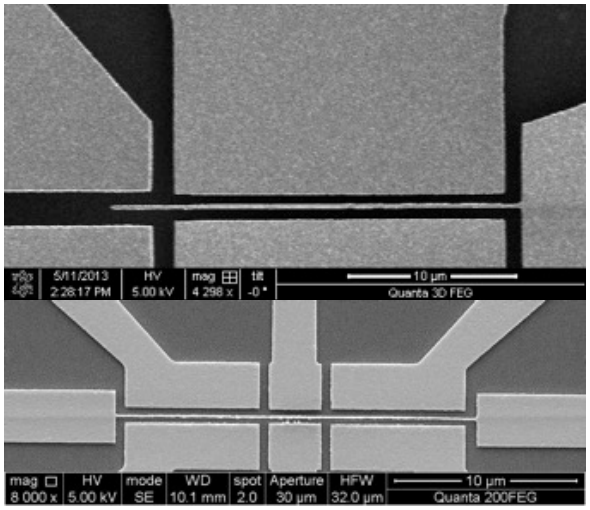

Figure 4-6 | Released NEMS devices. Upper: Released by HF. Lower: Released by VHF.

4.2.2 Top Down Process With Hard Mask

Any photoresist is a polymer compound and its etch rate by any gas is much higher than the etch rate of the solid material beneath it, especially metals, and in our case amorphous WN_x. For etching a 300 nm thick aWN_x layer, we need the PR thickness to be around 500 nm. However, this thickness is too high for sub-100 nm structures causing the structure to fall, as in Fig. 4-5. Therefore, a hard mask (HM) should be used on top of aWN_x layer. The PR will be patterned and used to etch the HM. Then the HM will be used to etch the aWN_x layer. The idea is simple, but it will add one step in layers stack and one step in etching.

The task here is to find a material that is easily etchable and has high etching selectivity with the desired layer, aWN_x. SF_6 is a very aggressive gas that can etch most materials without selectivity. Extensive research was done on different types of gases and their etch rate and selectivity of different materials, it was found that Cl_2 mixed with O_2 can etch the amorphous WN_x with high selectivity of SiO_2 (15:1) [129]. Another advantage of using SiO_2 as HM is that it will be etched away at the release step. The process steps are listed in Fig. 4-7. It is observed that the new process is similar to the former process except with additional steps for etching the HM and a separate step for etching the amorphous WN_x. This process steps are as follow:

1. Deposition Stack of Layers

Starting with the same sequence as the former recipe with additional one layer of PECVD SiO_2 on top of the aWNx layer.

2. *SU8 Resist coating*

The resist coating recipe on the HM will be the same as in the former section on aWN$_x$. Plus there is an additional advantage that the resist adhesion on SiO_2 is better than on amorphous WN$_x$.

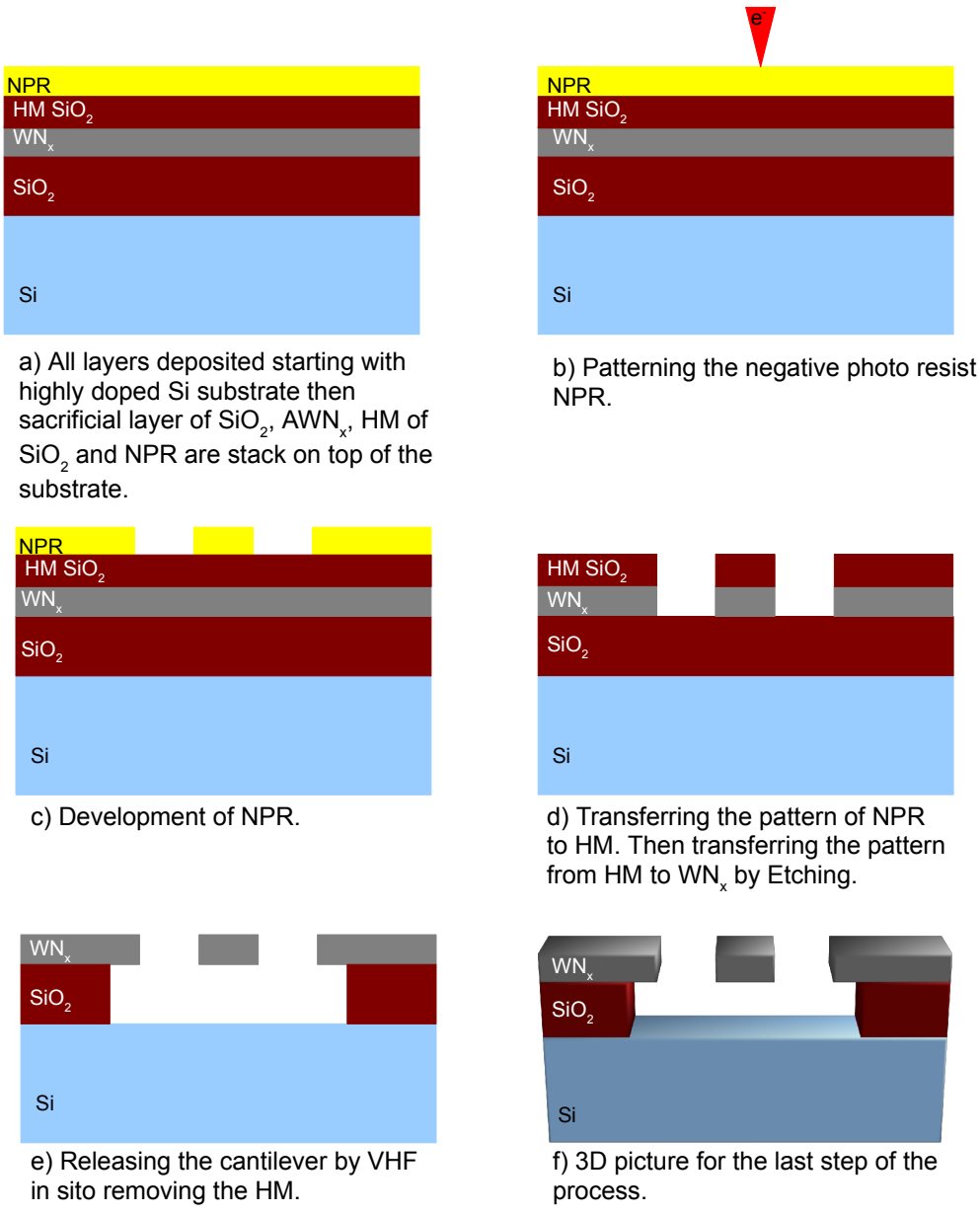

Figure 4-7 | The process steps for top down process with hard mask.

3. EBL Exposure and PR patterning

The EBL exposure parameters to the coated photoresist will be similar to the one in the former section. The adhesion of the PR to the SiO_2 is stronger than the adhesion to silicon or metal layer. Additionally, the exposed patterns have less proximity error due to smaller atoms of silicon and oxygen compared to tungsten, which cause less Ebeam scattering. Therefore, the Ebeam current flow should be increased for exposure. Proximity correction should be re-evaluated because of the new material beneath the PR. After exposure, the resist should be developed as mentioned in the former step.

4. Etching the HM

The HM is SiO_2 and it has a standard recipe for etching. The etching recipe is as follows:

- C_4F_8/O_2: 40/5 sccm
- Pressure 10 mTorr.
- Power: ICP 1500 W, platen 100 W.
- Temperature: 10° C.

It is better to ash the PR after etching the HM to avoid any polymer deposition when the amorphous WN_x layer is etched. The etching rate is 240 nm/min.

5. Etching the aWN_x with HM of SiO_2

The developed recipe is as follow:

- Cl_2/O_2 : 30/5 sccm
- Pressure 5 mTorr.

- Power: ICP 1000 W, platen 200 W.
- Temperature: 80^{o} C.

It is found that the etching rate is very fast at about 300 nm/min. This recipe allows etching WN_x with very high AR. The thickness of 600 nm has been effectively etched with 100nm of HM.

6. Etching the aWN_x with HM of SiO_2

The release process is the same as the one in the former section after ashing the SU8 resist for 5 min. Exposed SU8 is one of the toughest PR to remove and ash is the best method.

4.2.3 Bottom Up (Lift Off) Process

A bottom-up process is opposite from the top-down process. The material of interest (WN_x in our research) is deposited on top of the patterned PR. Then, the PR is removed and the unwanted material on top of the PR will be lifted off with the PR (sometimes called lift-off process) [22, 24]. There is no need for etching in this process (Fig. A-1). For EBL process, a positive photoresist (PPR) is recommended to minimize the exposure time. In this research, the positive resist PMMA is used because of the availability. Due to the stringers at the edge of the NEM switches, this process was not used in fabrication.

4.2.4 Hybrid Process

This process is a combination of both the bottom-up and the top-down processes. In this process, the HM is deposited with the lift-off process (bottom-up) and the aWN_x is etched as in the top-down process. In this process, we have chosen the metal nickel (Ni) as the HM because nickel has a very high etching resistivity for both aggressive gases, SF_6 and Cl_2.The process steps have been illustrated in Fig. A-2.

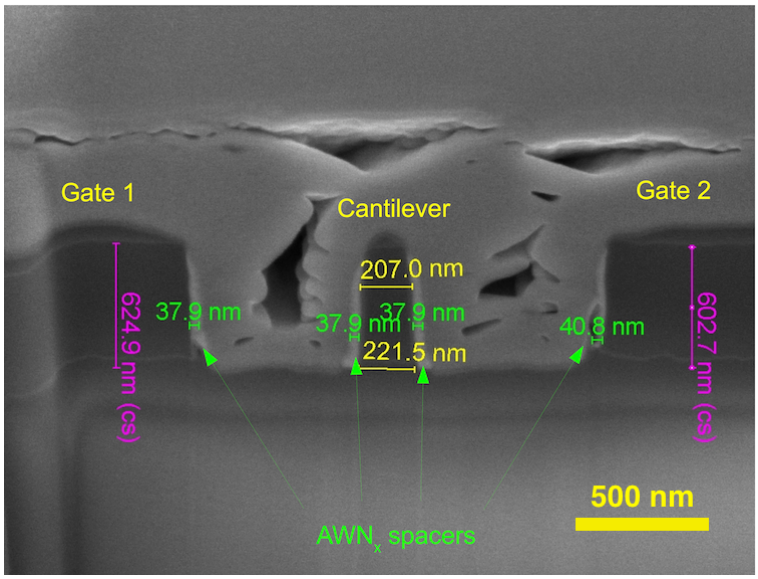

Figure 4-8 | SEM image of Si NEM switch with aWN_x spacer.

4.2.5 Introduction of the Spacer Concept

Another concept worth a try and evaluation is the spacer concept. As stated before, Si has many deficiencies in electrical characteristics. Other groups have used Si to fabricate NEMs devices and then deposit a thin layer of ALD metal at the edges of the NEM switches to overcome these deficiencies. ALD is an expensive choice and a time-consuming process [131]. During the research, NEM switches have been fabricated out of

Si and an aWNx spacer has been sputtered at its edges. The following Fig. 4-8 shows the SEM image of the cantilever cross section. This method provides the opportunity to reach even smaller feature sizes than those achieved by direct exposure. The critical feature size could go down to 10 nm or even lower. These devices where not fabricated due to time limitation.

3. LATERAL NEM SWITCHES CHARACTERIZATION

The pull-in voltage has been theoretically derived by analyzing the electrostatic force that pulls the beam toward the gate electrode: [91, 132, 133]

$$V_{pi} = \sqrt{\frac{8kd_o^2}{27C_g}} \qquad (7)$$

where C_g is the gate capacitance and d_o is the thickness of the air gap between the gate electrode and the beam.

The gate capacitance can be obtained from the parallel plate capacitor equation:

$$C_g = \frac{\varepsilon_0 A}{d_o} = \frac{\varepsilon_0 l_g t}{d_o} \qquad (8)$$

where l_g is the gate electrode length and ε_0 is the permittivity of air. Note that the actuation area is determined by the length of the gate electrode l_g rather than l.

Substituting Equation (8) into Equation (7), the pull-in voltage can be expressed as:

$$V_{pi}^2 = \frac{16}{81} E \frac{g^3 w^3}{l_g l^3 \varepsilon} \qquad (9)$$

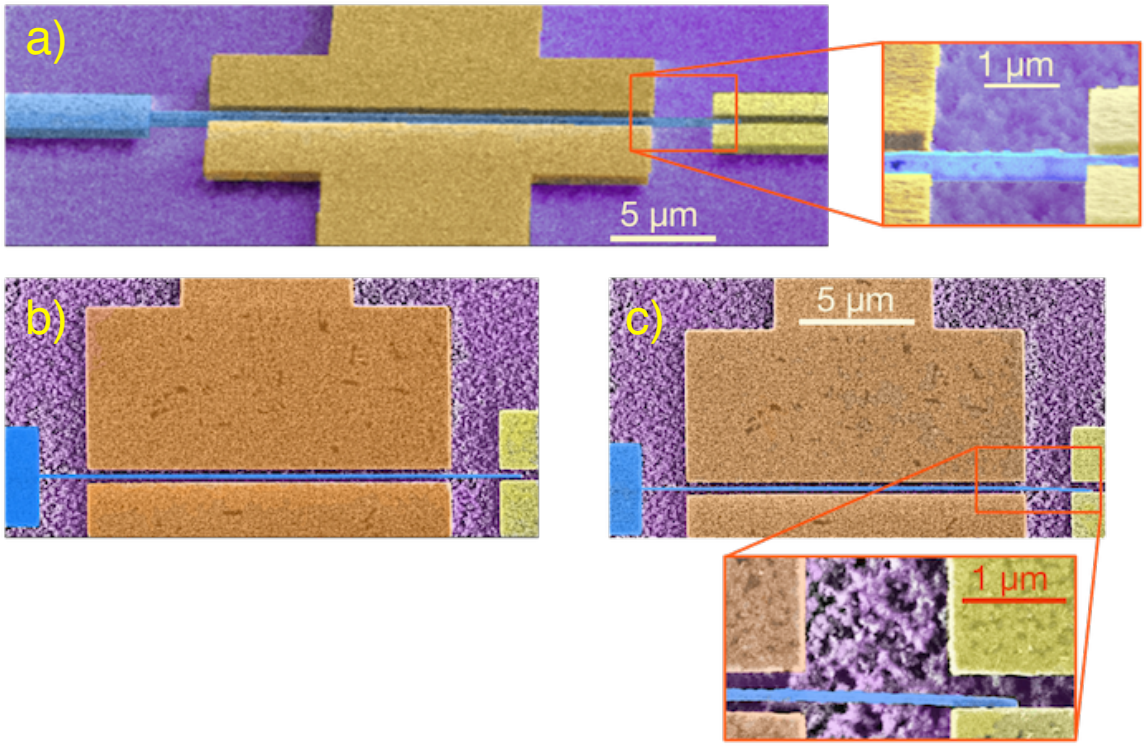

Figure 4-9 | SEM images of fabricated NEM switch a) shows the nano-size structure and high aspect ratio with zoomed-in 74° tilted view, b) top-down view; c) actuated NEM switch.

An interesting observation is that the pull-in voltage is independent of the thickness of the laterally actuated cantilever, since both the electrostatic actuation force and mechanical spring restoring force are directly proportional to thickness. It is important to note that Equation (11) is an approximation since the derivation of the effective spring constant assumes a uniform distribution of load across the cantilever beam, whereas the electrostatic force is applied only across the portion of the beam directly facing the gate

electrode (the effect of 2-dimensional fringing electric fields is neglected as well). The effect of the attractive electrostatic force is overestimated because it is assumed to be applied at the point of maximum deflection (i.e., at the tip). Hence, V_{pi} is underestimated using Equation 11 [28, 134-136]. For the device design in Fig. 4-9 (w = 200 nm, d = 220 nm, l_g = 15 μm, l = 20 μm), and a Young's modulus of 300 GPa for aWNx, the pull-in voltage is calculated to be 1.33 V.

4.3.1 I-V Measurement for NEM Switches

The transfer (I-V) characteristic of the device was obtained using a Keithley 4200 SCS parameter analyzer combined with a probe station placed on top of air table at ambient air condition. The drain electrode was biased at a voltage of 0.1 V, while the source was grounded. The gate voltage was applied to only one gate terminal, and swept from 0 to 10 V and back down to 0 V, with a step size of 50 mV. The measured data are shown in Fig. 4-9. V_{pi} is 1.8 volts for the first switching cycle, which is approximately 20% larger than the calculated theoretical value. This is expected because of the approximations involved in deriving the V_{pi} equation [28, 91, 134-136]. The switching was repeated by reapplying the gate voltage sweep (Fig. 4-10). It should be noted that the off-state current measured was the noise floor of the setup (~1 pA). (This was the detection limit of the setup, and these current values are observed even when the probes are open-circuited.) Also, the on-state current was limited by setting the current compliance level on the source terminal to 11 nA, so as to avoid the possibility of welding the mechanical contact during the DC measurements. The switching behavior is

not abrupt, as is expected for mechanical switching. For low values of applied gate voltage, the current increases exponentially. This may be attributed to increased tunneling leakage current as the contact air gap is reduced with increasing gate voltage [134, 137].

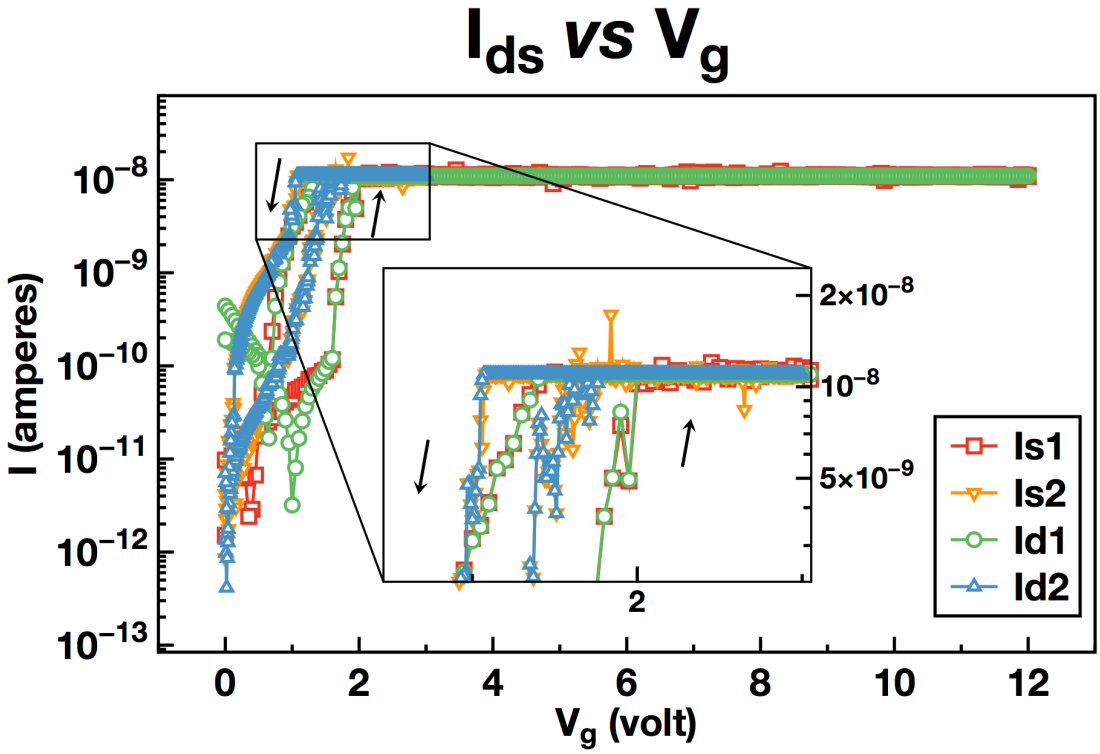

Figure 4-10 | The transfer characteristics of the WN_x device shows a V_{pi} voltage of 1.8 V and I_{on} / I_{off} ratio = 10^4. Device dimensions: w = 200 nm, d = 220 nm, t = 500 nm, l_g = 15 µm, l = 20 µm.

Once physical contact is made, a steeper change in the drain current is seen. It is to be noted that the gate voltage (V_g) has been swept more than 3 V, which is about 3× the V_{pi}. With low hardness material devices, this high gate voltage would break down the cantilever due to excessive electrostatic force and weld the cantilever to the drain due to the strong adhesion, as shown in Fig 3-4. These faults, called breakage and stiction, occur

frequently for NEM switches fabricated with poly silicon material. It is also noted from the same I-V curve that the NEM switch is still functional after the cantilever is pulled out from the drain at 1.3 Volts (called pull out voltage, V_{po}).

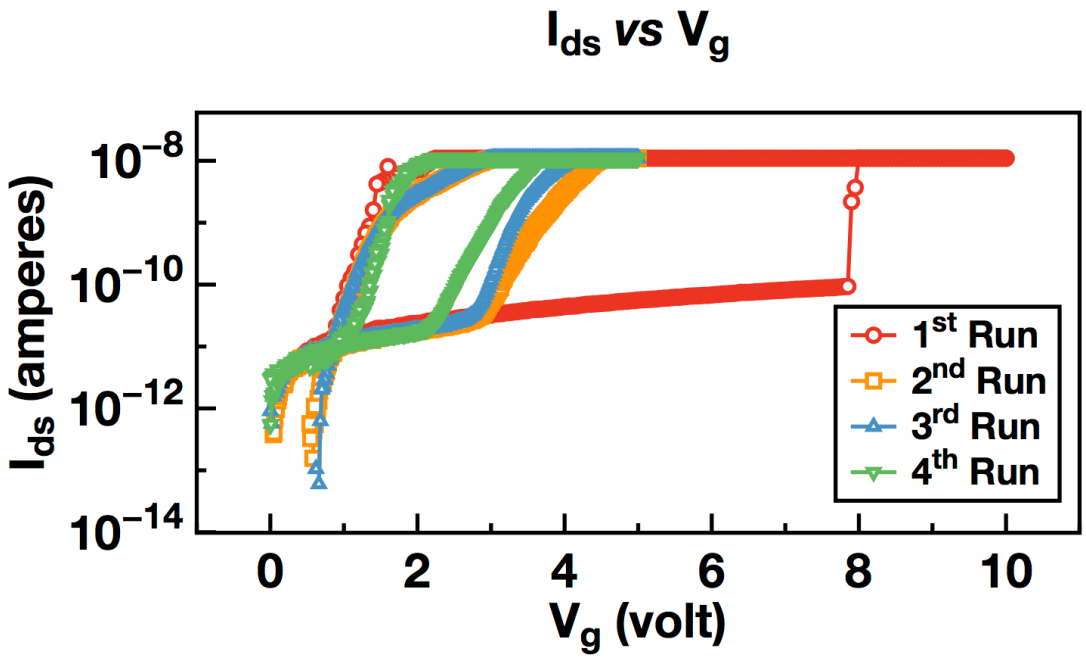

Figure 4-11 | I-V curve for 4 consecutive cantilever pull-in operations.

For the second sweep, the I-V curve starts to dampen (lowering of voltage) due to the high sweep of Vg. Fig. 4-11 shows the V_g sweep range was adjusted to maximum voltage not more than 25% of the V_{pi}. This figure shows I-V current profile in ordered and tidy shape for several sweeps. The pull in voltage of the second cycle is about 30% of the first cycle. However, it became more stable in the consecutive cycles. The deviation of V_{pi} of the second and later operation cycles is less than 20% from each other. These characteristics of NEM switch are due to the unique combination of high elasticity and hardness of the material [91]. Typically, WN_x atoms are arranged randomly inside the NEM switch structure. After the first run the atoms rearrange themselves, causing the V_{pi}

reduction. Also, this reduction can be attributed to charge accumulated and traded in the PECVD oxide layer beneath the probe pads [33]. Amorphous metal has a unique cluster free molecular structure that after the first deformation faces molecular relaxation process [49, 138]. Characterization and dimensions summary are listed in Table 4-1.

Parameter	Value	V_{pi} (Simulated)	V_{pi} (Theoretical)	V_{pi} (Shorten)	V_{pi} (Adjusted)	V_{pi} (Measured)
l	15 μm	4.30 Volts	3.05 Volts	3.55 Volts	1.83 Volts	1.60 Volts
g	200 nm					
w	220 nm					

Table 4-1 | The pull-in voltage as calculated, simulated and measured.

4.3.2 Sub-1 Volt NEM Switches

To achieve lower voltage operation, which is desirable for lower dynamic power consumption, the beam width and actuation air-gap thickness were reduced to 190 nm and 150 nm, respectively. The switch design and measured transfer characteristics are shown in Fig. 4-12. The calculated value of V_{pi} for this device is 0.69 V and as expected, the measured value of V_{pi} (0.8 V) was found to be higher (15%). In this case, the current compliance was not introduced since the on-state current was expected to be lower due to the scaled dimensions of the device. The drain current was close to 3 nA for 0.1 V V_{ds}, which indicates a high contact resistance of 30 MΩ. This can be attributed to very small actual contact area for the scaled NEM device. Although minimal contact area is advantageous for reducing stiction probability, it also increases the contact resistance. The I-V sweep done only one time (because of fragility of the single clamped nano-scale

cantilever in ambient air) and the low value of current below pA is noise because it is beyond the reading resolution (pA), that is why I_d does not equal I_s. All the dimensions, as well as the pull-in voltage comparisons (theoretical, simulated, empirical and measured), are listed in Table 4-2.

Parameter	Value	V_{pi} (Simulated)	V_{pi} (Theoretical)	V_{pi} (Shorten)	V_{pi} (Adjusted)	V_{pi} (Measured)
l	15 μm	2.10 Volts	1.59 Volts	1.85 Volts	0.95 Volts	0.80 Volts
g	150 nm					
w	190 nm					

Table 4-2 | The Sub-1 Volt V_{pi} as calculated, simulated and measured.

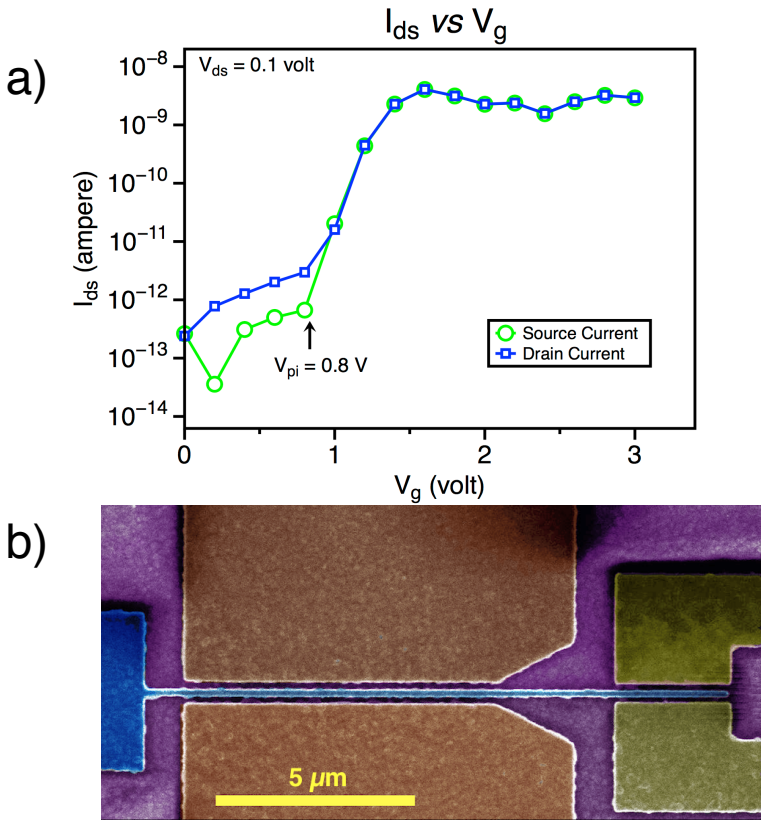

Figure 4-12 | a) The transfer characteristics of the sub-1 V WN_x NEM switch shows a pull-in voltage of 0.8 V. b) Top view SEM image shows the device dimensions as: w = 190 nm, d = 150 nm, t = 500 nm, l_g = 15 µm, l_c = 20 µm.

Another experiment run was done for a different device presented in Fig. 4-13. The I-V curve is presented in Fig. 4-14. The figure shows very low SS value equal to 5 mV/ decade and high on off ratio, $I_{on}/I_{off} > 10^2$. The most interesting parameter of this switch was the pull-in voltage, $V_{pi} < 0.3$ Volt. The experiment run at ambient air only for a single time, because of the same reason as for the former NEM switch. Later the electron beam lithography tool was down for long time that the NEM switch could not be fabricated again and this experiment was one of the last experiment performed in the research. This was the reason that the endurance experiment devices have been fabricated using contact aligner.

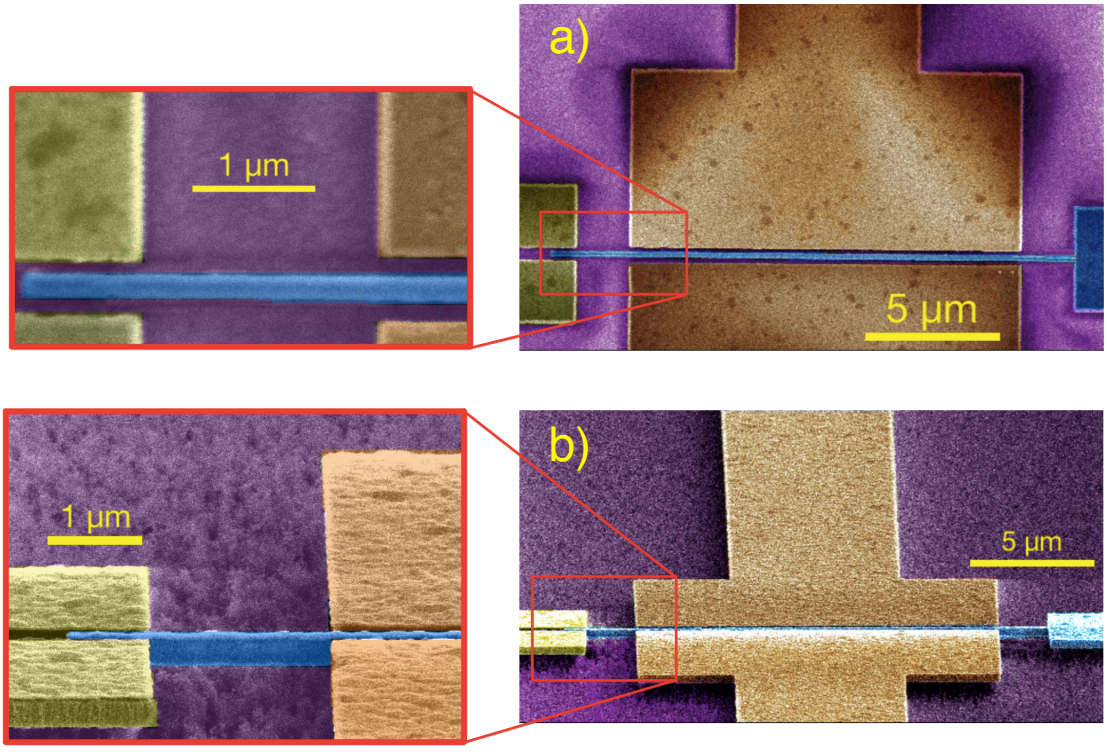

Figure 4-13 | SEM image of a low V_{pi} three terminal lateral NEM switch; a) top view shows the device dimensions as: w = 180 nm, d = 100 nm, t = 300 nm, l_g = 14 µm, l_c = 16 µm, b) tilted view .

Amorphous WNx material has a closed pack molecular structure and atomic density that have very low edge roughness that prevent oxidation [100-102]. These two criteria yield to have low contact resistance. The measured contact resistance was about 4 kΩ. All the dimensions, as well as the pull-in voltage comparisons (theoretical, simulated, empirical and measured) are listed in Table 4-3.

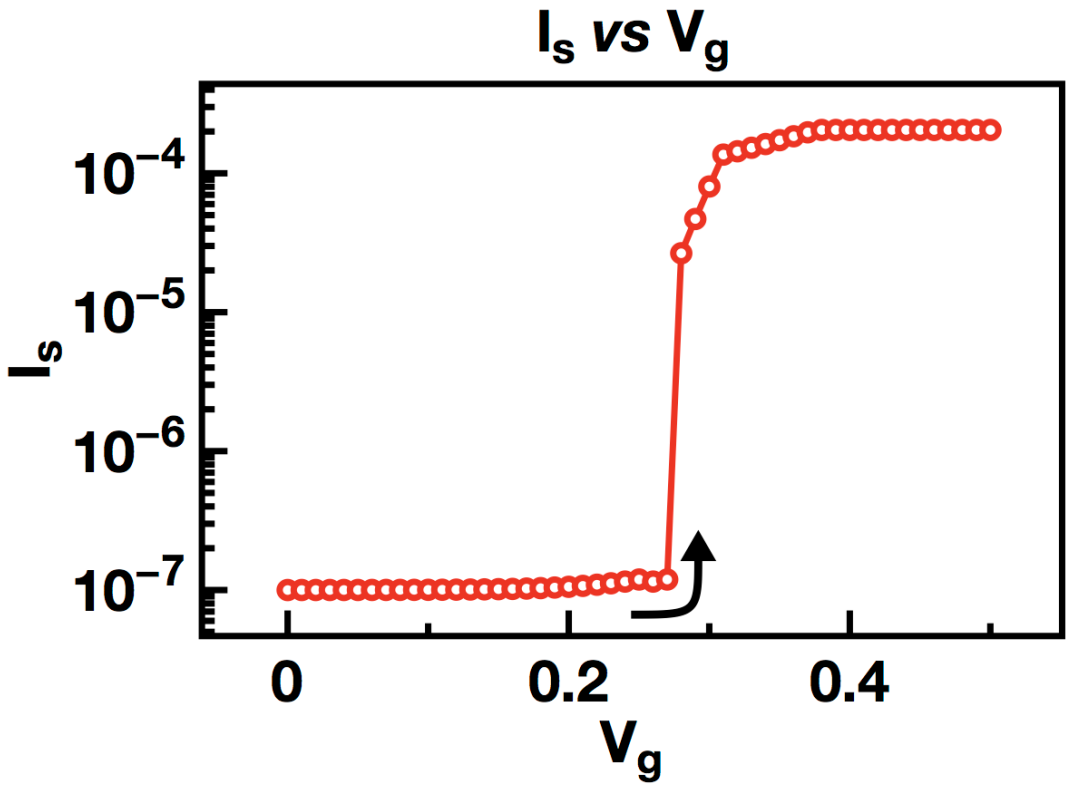

Figure. 4-14 | The transfer characteristics of the lateral NEM switch with V_{pi} sub-1 V and SS = 5 mV/decade.

Parameter	Value	V_{pi} (Theoretical)	V_{pi} (Shorten)	V_{pi} (Adjusted)	V_{pi} (Measured)
l	14 μm	0.91 Volts	1.06 Volts	0.55 Volts	0.28 Volts
g	100 nm				
w	180 nm				

Table 4-3 | The device with lowest V_{pi} as calculated, simulated and measured.

It is observed that the measured V_{pi} is for all the above-listed NEM switches are close to the adjusted calculated value. The adjusted value is 60% of the analytically calculated value. This reduction in the value is due to measurement error, cantilever cross section profile Young's modulus alteration due to sub-100 nm structure size and others as demonstrated by Prof. Howe group [26, 116]. The last two tables are for the same NEM switch, but the gap and width are different due to systematic errors in reading the dimensions of the less than 100 nm dimensions of the NEM switch from SEM picture. Cantilever width and the gap are more critical than the length of the cantilever, where 10% variation in the width could reflect more than 35% error in calculation as table 4-4 shows more accurate calculated V_{pi} compared to the measured one. The anchored side of the cantilever is not 100% rigid where the release step could etch particular volume beneath the cantilever edge and yield a flexible edge rather than a stiff one. Another source of error that the analytical calculations involve the measured Young's modulus with nano-indentation method or reported figures for large-scale dimensions. Professor Howe group showed that the Young's modulus of nanoscale dimensions is much lower than the reported one about 50% [26]. This reduction could resolve the mismatching issue between the analytical result and the experimental one.

Parameter	Value	V_{pi} (Theoretical)	V_{pi} (Shorten)	V_{pi} (Adjusted)	V_{pi} (Measured)
l	14 μm	0.59 Volts	0.69 Volts	0.35 Volts	0.28 Volts
g	90 nm				
w	150 nm				

Table 4-4 | The device with lowest V_{pi} as calculated, simulated and measured.

4. High Contact Resistance in Lateral NEM Switches

Contact resistance Rc in the actuated lateral NEM switches is higher than the one in vertical switches for few reasons as follow:

1. Etching in micromachining process forms the contact area in lateral NEM switches. In this process the etching profile never comes vertical 90° from the horizon [89]. This inclined vertical sidewall profile leads to point style contact less than 1% of the total contact area as can be demonstrated below.

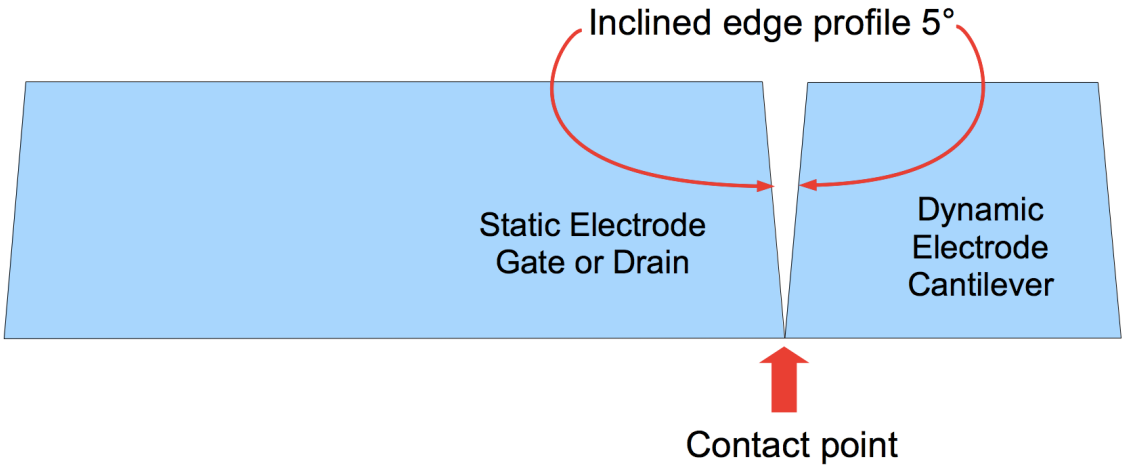

Figure. 4-15 | Small contact area at lateral NEM switches.

2. Another cause is the etched profile of the WNx is not highly smooth, unlike the surface roughness which is less than 2.30 nm as illustrated in the figure below. This lead to a further cutback in the effective contact area to show also no more than 5% of the contact area. The figure shows as well the inclined style of the sidewall of the etched profile.

3.

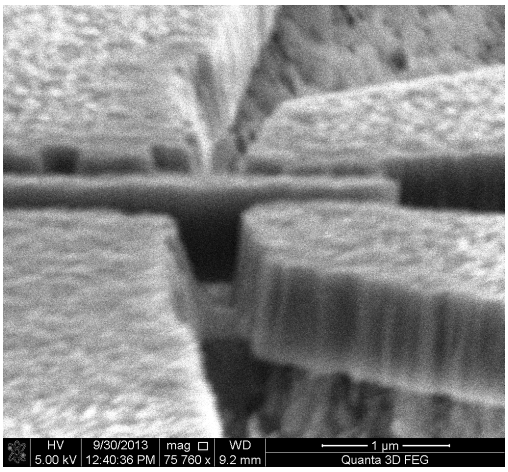

Figure. 4-16 | High edge roughness and incliness.

Ohm's law correlates the current flow with the applied voltage and resistance as well as the resistance to the resistivity (ρ) follow:

$$R = \rho \frac{l}{A} \qquad (10)$$

Considering the resistivity (ρ) and length are constant (c) then the equation will be:

$$R = \frac{C}{A} \qquad (11)$$

and

$$I = \frac{VA}{\rho l} \qquad (12)$$

So the current flow is directly promotional to the contact area. Scaling down the contact area of resistance of 5kΩ to exhibit less than .05% of effective area lead to contact resistance increment of 2000%.

4. On the other hand, for the vertical NEM switched, the effective parameter on the contact resistance is the surface roughness where it is not very high around 2.31 nm as an average value. In addition, the consecutive layers, sacrificial layer as well as the lower side of cantilever follow the same profile of the beneath surface and are not altered by RIE etching process. This lead to a low surface mismatch between the top surface of the fixed electrode and the lower surface of the cantilever (the movable electrode), which is the primary cause of low contact resistance for vertical NEM switches.

5. CONCLUSION

In the previous sections, four different recipes of NEM switch fabrication have been conducted and discussed. These recipes are standard in the semiconductor fabrication industry. The following table 4-5 will summarize the differences between these recipes and the optimal one for NEMS fabrication.

Amorphous tungsten nitride (aWN_x) is a prospective high-quality structural material for fabrication of NEM switches. We report deposition and etch processes for amorphous WN_x thin films using reactive sputtering and reactive ion etching, respectively. Initial experimental results indicate that aWN_x can be used to achieve low-voltage NEM switches. We report a pull-in voltage of 0.8 V for a scaled device with 150

nm air gap and 190 nm width. High contact resistance (on the order of 10 MΩ) is experimentally observed; indicating that further optimization of the contact electrode material is required for future application of WN_x devices. Another NEM switch showed V_{pi} = 0.28 Volt with contact resistance of about 4 kΩ and dimensions of 100 nm air gap and 180 nm width. This further supports the potential of aWN_x based NEM switch devices.

Process	Pros	Cons	Result
Top down No HM SEM Image Fig. 4-8	1. Simple process. 2. Fewer steps needed 3. Vertical profile. 4. Functional device	1. Low thickness etch. 2. No etching stop layer. 3. Ar damages aWN_x	
Top down with HM SEM Image Fig. 4-9	1. High vertical profile. 2. Functional device. 3. Etch stop layer available.	1. Two more steps needed in process. 2. Precautions needed at etching the HM.	
Bottom Up down SEM Image Fig. 4-10	1. Simple process. 2. Fewer steps needed 3. Vertical profile.	1. Low thickness of aWN_x. 2. High edge stringers affect the NEMS operation.	
Hybrid with HM SEM Image Fig. 4-11	1. Simple process. 2. High vertical profile. 3. Functional device.	1. Two more steps needed in process. 2. Precautions needed at lift off the HM. 3. Possibility of cross linking between structures.	

Table 4-5 | Comparisons between different process recipes.

Chapter 5

ENDURANCE AND EXPENDABILITY

1. INTRODUCTION

As the name suggests, the operation of Nano Electro-mechanical Switches is governed by both electrostatic and mechanical forces. Specifically, the active part (mainly a movable cantilever singly or doubly clamped) is continuously affected by each or both of these forces throughout every step of operation. This operation includes: acceleration, deceleration, hammering style impact, damping, oscillation, electric charge, discharge, high current flow, charge accumulation and abrupt discharge. This complex operation causes the material of the active part as well as the electrode to deteriorate rapidly, thus impairing the electrical functionality and shortening the lifetime of the switch. Static experiments of amorphous WN_x show high endurance behavior against corrosion and against formation of crystallites. This chapter will illustrate the dynamic experiment behavior to prove that amorphous WN_x is an adequate candidate for NEM switch fabrication.

Another interesting characteristic of WN_x is its dissolution ability in solutions such as water. This feature gives WN_x superiority over other materials to fabricate expendable devices that vanish within a specific time. Dissolution tests have been conducted for different WN_x based devices (resistive heater, accelerometer, NEM switch) in ground

water (GW), deionized water (DIW) and saline water (SW). This chapter will discuss the dissolution rate in different types of aqua solutions under different conditions.

2. ENDURANCE

5.2.1 Challenges:

In order to design the suitable material for NEM switches, the challenges must first be discussed. This is best done by following the position of the active part during operation.

The movement of the active part toward the electrode causes a high accumulation of electric charges, inversely proportional to the gap between the active part and the electrode. As the active part moves nearer to the electrode, the charge accumulation increases. This accumulation of charges could cause abrupt electric discharge (spark) especially with the existence of high surface roughness, as shown in Fig. 2-2(c). This electric discharge could cause material melting (burn-out). Ablation and electrode surface damage could also occur as direct result of electric discharge, as in Fig. 2-2(d) [24].

At the contact point, the active part is exposed to three balanced forces; electrostatic force (F_e) induced by the pull-in voltage, van der Waals and Casimir forces (called adhesion force (F_{adh})) toward the electrode, and mechanical restoring force (F_m) outward from the electrode [78, 82]. Failing to restore the active part to its original position when the F_e vanishes is called stiction, as shown in Fig. 2-2(e) [54]. Therefore, the material should have a high spring constant (high Young's modulus) to overcome the stiction issue. However, a high spring constant (high Young's modulus) leads to high

pull-in voltage, as they are directly proportional. To overcome this issue, the NEMS switch should be fabricated with smaller dimensions (gap and thickness) [10].

Finally, when the NEM switch operates without facing any of the above mentioned failures, the active part could face a mechanical failure. This failure is known as material fatigue and fracture and normally occurs near the anchor, as shown in Fig. 2-2(f) [77]. This failure occurs because of the grain boundary inter-stress and defects. These defects weaken the strength of the material and degrade the electrical and thermal conductivity. This failure is the main reason for NEM switch unreliability and short lifetime resulting in a few million cycles at most. Figure 2-3 shows a defective cantilever, fabricated using gold (Au), due to fracture and contact area wearing.

5.2.2 Solution

WN_x has a grain-less molecular structure, corrosion resistance, high endurance, smooth surface, low contact wear and exacerbation resistance [87]. These characteristics make WN_x a promising solution to the challenges of NEM switch operation. Welding is a serious issue for traditional **M**EMS devices and present day **N**EMS devices (including NEM switches). To prevent welding, some prior works have used a thin oxide layer on the contact surface to limit the current flow and electric discharge by increasing contact resistance but with a side effect of suppressing the ON current [31]. Additionally, the thin oxide layer wears off during the operation cycles causing the switch performance to deteriorate rapidly [16]. In comparison the aWN_x NEM switches have smooth contact surface with no spikes that focus the electric field causing electric discharge as well as

generating Joule heating [139]. Amorphous WN_x also has strong molecular bonds via closely packed atomic density that prevent further oxidation [100-102]. Consequently, this helps in achieving a moderate contact resistance to prevent excess charge passage and avoids formation of native oxide which ensures constant operation throughout the switch lifetime.

Another critical challenge with NEM switches is ablation and surface deterioration. Usually hard materials do not face this type of failure, but they do experience high resistance to current flow that limits the switching efficiency and causes excessive heat generation, resulting in welding. As mentioned before, a thin oxide layer has the issue of wearing off during the cycles of operation and is therefore not a viable solution. Another proposed solution is dual contact NEM switch, however this is not practical due to complicated fabrication process, larger footprint and need for high voltage and power to operate, which defeats the goal of low to no power switches [36, 140]. In contrast, amorphous WN_x has high hardness, which makes the electrode as well as the active element highly resistant to ablation and wearing effect. Furthermore, it has high electrical and thermal conductivity, which avoids the possibility of welding and does not deteriorate the main function of a switch.

Next, stiction is another major challenge in scaling up of NEM switches for complex circuitry. The lack of enough mechanical restoring force causes of stiction. Some researchers proposed the use of high pull-back voltage at an opposing electrode to overcome the stiction issue [50, 51]. This is not a practical solution as it needs high voltage operation, slows down the speed and makes the switch unreliable. In contrast,

amorphous WNx has fairly high Young's modulus (300 GPa), reflecting a high value of spring constant. This provides an adequate mechanical force (F_m) within the material to pull back the active part after removing the electrical pulling force (F_e), thus eliminating the need for a high pull back voltage from an opposing electrode [91]. Other causes of stiction are the van der Waals force as well as the Casimir force [46, 50]. One way to seize them is to have high enough mechanical restoring force to overcome the accumulated force for stiction. At the same time, the spring constant should not be too high that it increases the V_{pi}, as they are directly proportional. Silicon based NEM switches have higher probability of stiction due to their low value of Young's modulus (about 160 GPa). On the other hand, material with high value of Young's modulus have almost no stiction issue; such as carbon compounds which have a Young's modulus value around 700 GPa. Amorphous WN_x has an intermediate value of Young's modulus, which overcomes the stiction issue that exists in silicon based NEM switches and does not require high V_{pi} as is needed for carbon based material.

Another cause of no surface adhesion is the high roughness surfaces. As the amorphous WN_x has high hardness and the NEM switch has been fabricated using a SiO_2 sacrificial layer (which is removed by release), some residual SiO_2 will exist on the surface of the gate and cantilever. The high surface roughness and the thin layer of SiO_2 prevent the adhesion between the two facing parts [40, 141, 142]. Figure 2-9 shows the AFM picture of the amorphous WN_x surface. In addition, the high Young's modulus leads to a high spring contact for WN_x. The high spring constant generates high restoring

mechanical force, which overcomes the adhesion force. This justification is used later in this section to explain the lack of adhesion in 2 terminal NEM switch operation.

Cluster boundaries which exist in crystalline or non-perfect amorphous materials cause fracture, deformation, material fatigue or all three [101, 105]. This type of defect is called a mechanical failure. The grain boundaries are the weakest points in the material (weakest link in the chain) and fractures occurs at these boundaries. This defect shortens the lifetime of the device tremendously [95]. Therefore, the material to be used to fabricate the NEM switches needs to be either mono-crystalline or highly amorphous to avoid this failure and defect of poly-crystalline material. Fabrication of mono-crystalline metal is not possible in conventional CMOS processes, thus amorphous metal is the more feasible choice. Therefore, our next focus was to use a WNx based nano-ribbon as structural material for a two terminal NEM switch.

3. HIGH ENDURANCE NEM SWITCH

5.3.1 Design and Fabrication:

For device design, the NEM switch cantilever length has two effects: shorter one has faster operation speed and longer one has lower pull-in voltage. Both the speed and the pull-in voltage are directly proportional to the Young's modulus and thickness, and inversely proportional to the length of cantilever [72, 111]. Therefore, an optimal design is to reduce all the dimensions of the NEM switch except the length, which leads to pull-in voltage reduction and increment in the quality factor and resonant frequency. The switching speed increases as the pull-in voltage decreases. Hence, high Young's modulus

and nano-scale dimensions are desired for optimal NEM switch fabrication. Following this design rule, we fabricated a doubly clamped cantilever vertically actuated NEM switch using amorphous tungsten nitride (aWN_x). Figure 5-1(a) shows the cantilever molecules in amorphous structure for demonstrations purpose and Fig. 5-1(b,c) show the idle position and actuated position vertical NEM switch. Scanning electron microscope (SEM) image is shown in Fig. 5-1(d). COMSOL simulation results are presented in Fig. 3-9(a,b).

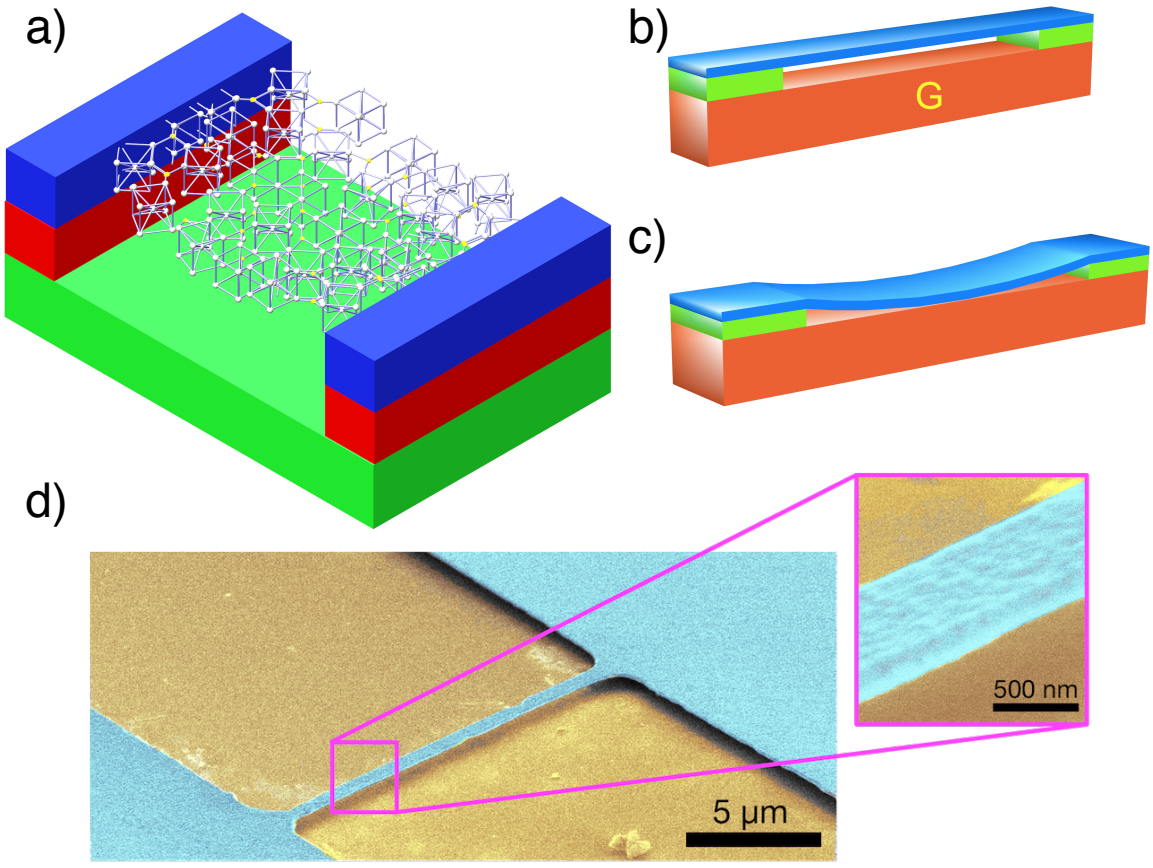

Figure 5-1 I a) Cantilever of vertical NEM switch shown with molecules in amorphous structure for demonstration purposes; b) 3D layout of vertical NEM switch in idle position; c) 3D layout of vertical NEM switch in actuation position; d) SEM image of aWNx double clamped cantilever vertical NEM switch before and after trillion cycles run.

A thin (30 nm) layer of amorphous WNx was deposited on heavily doped (50 mΩ.cm) prime quality n-type 4” silicon (100) wafer to act as lower electrode (the gate). Then, a 300 nm thick layer of silicon dioxide (SiO_2) as sacrificial layer was deposited using plasma enhanced chemical vapor deposition (PECVD). Finally, the active layer of amorphous WNx based nano-ribbon (100 nm) was formed as described before in chapter 2.2. Positive photoresist was used to pattern the active layer by ultra violet (UV) contact aligner. The amorphous WNx nano-ribbon was then etched using reactive ion etching (SF6/Ar : 15/5 sccm plasma at 10° C and 20 mTorr pressure) to form nano-ribbon of 100 nm (thickness) × 2 μm (width) × 12 μm (length) with 300 nm air gap. The sacrificial layer (PECVD SiO_2) was then etched using liquid hydrofluoric acid (HF) to form the free-standing cantilever structure. Then the released devices were dried by CPD. Vapor HF is not suitable for this process as it leaves a high thickness residue of SiO_2. It is noted from the process steps, that the static and dynamic parts of the NEM switch are made of the same material (aWNx) to prevent the diode effect and welding [91].

5.3.2 Non-Hysteresis Operation:

The fabricated devices were then probed using Keithley 4200 SCS semiconductor parameter analyzer to obtain the electrical performance of the devices in ambient pressure environment. As part of the measurement procedure, to ensure the isolation between the contact pad and bottom static electrode, an I-V sweep was conducted on a contact pad without a hanging cantilever. Isolation was confirmed with measured current in the pico-amps range (which is considered as noise) with no direct relation to the voltage.

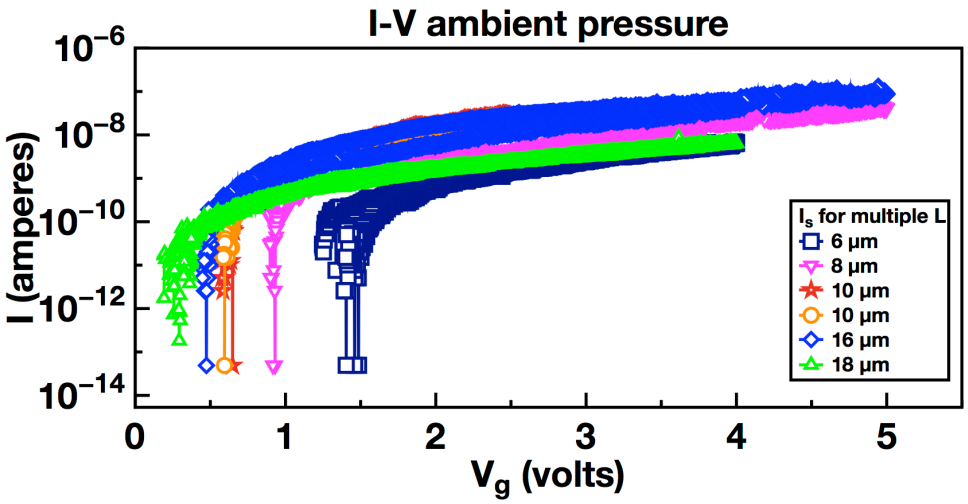

Figure 5-2 I I-V transfer curves of multiple runs of two terminal NEM switches with different cantilever lengths.

The transfer (I-V) characteristic in Fig. 4-11 is shown for a single clamped lateral NEM switches fabricated from WN_x Fig. 4-9. It shows typical nature of hysteresis expected in such switching. However, a series of I-V curves in Fig. 5-2 for different lengths of cantilevers range from 6-18 µm shows hysteresis less behavior. The measured value of V_{pi} complies within 60% of the calculated V_{pi} (adjusted value).[91, 116] Additionally, it is observed that the pullout voltage (V_{po}) equates with the V_{pi} from the same figure. This equivalent value of V_{po} and V_{pi} reflects an adiabatic operation of NEM switch, because of the absence of hysteresis power loss. Hysteresis behavior takes part in NEM switches mechanical operation due to the existence of adhesion force (F_{adh}), which is a sum of van der Waals force and Casimir force, when the electrostatic force (F_e) vanishes. The high Young's modulus of

amorphous WN_x generates a higher mechanical restoring force (F_m) similar to the results of SiC based material and carbon nano-tube (CNT).[24, 143]

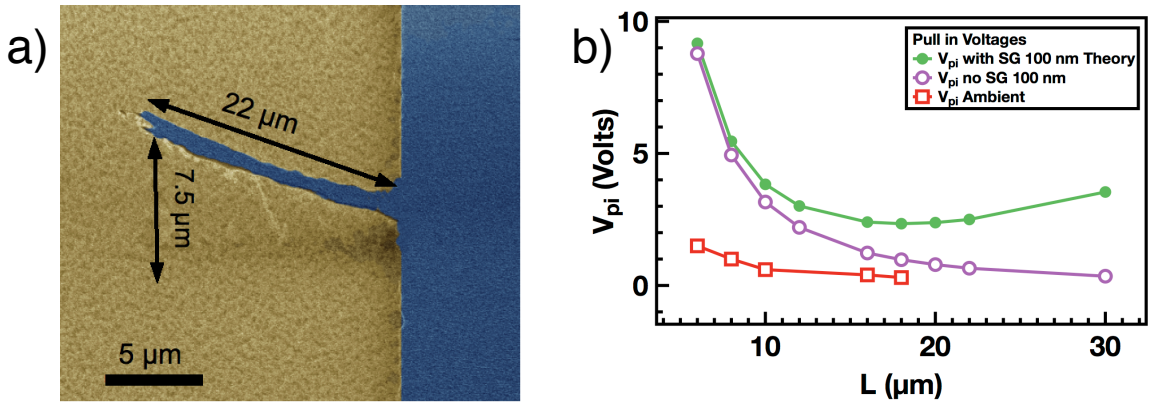

Figure 5-3 I a) Single clamped ribbon style cantilever curved upward due to a tensile residual stress; b) pull-in voltages versus cantilever length, calculated value with and without residual stress gradient and measured value (ambient).

Figure 5-3(a) shows single clamped ribbon style cantilever curvature upward, because of the residual stress gradient of WN_x. The generated bending moment (M), which adds an extra force in favor to the mechanical restoring force (F_m) to overcome the adhesion force. M could be calculated by the following formula [144]:

$$M = \frac{\Delta Z E w t^3}{6l^2} \qquad 13$$

where:

M is the bending moment,

E is the Young's modulus,

w is the width of the cantilever beam,

t is WN_x film thickness,

l is the length of the cantilever,

ΔZ is the cantilever tip deflection distance.

The gap between the cantilever and the gate is directly proportional to the cantilever length. Figure 5-3(b) shows when the length of the cantilever exceeds 18 μm, the pull-in voltage start increasing due to the increment in the gap. This experiment adopted double clamped vertical NEM switches. The F_m of the double clamped NEM switches is 64 times greater than the single clamped NEM switches according to the following formula for point load:

- for the single clamped NEMS:

$$F_m = g\left[\frac{Etw^3}{4l^3}\right] \quad (14)$$

- for double clamp NEMS:

$$F_m = g\left[\frac{16Etw^3}{l^3}\right] \quad (15)$$

This high F_m plus the high moment (M) overcome the F_{adh} causing hysteresis-less switching behavior as shown in Figure 5-2. In contrary, single clamped lateral NEM switches fabricated from WN_x does not show this hysteresis-less behavior because its mechanical restoring force is 64 times less than the double clamped one and the lack of the surface tensile stress (M) affect this phenomena further (Fig. 4-11). At the same time, this is beneficial to produce lower pull-in voltage as we

observed sub-0.3 pull-in voltage (0.28 volt) with a high I_{on}/I_{off} about 10^3 (Fig. 4-14). By reducing air gap between the gate the cantilever body and/or by increasing the cantilever length, a doubly clamped vertically actuated switch can experience further lowering of V_{pi} [35, 40, 47, 140, 141, 145-153].

The measured resistance is about 5 kΩ where the cantilever resistance is 0.2 kΩ for 12 μm length switch and 0.17 kΩ for 10 μm length switch. The resistance was calculated from the measured resistivity (using a 4-points probe measurement tool) and the switch dimensions – the resistance is directly proportional to the resistivity and length and inversely proportional to the cross section area. The total resistance is the sum of cantilever resistance and the contact resistance. The contact resistance turns to be less than 5 kΩ, around 4.8 kΩ. Figure 5-4(f) shows the contract resistance, which is in range of few kΩs (at the contact state) and does not increase even after trillion cycles (discussed next). It is to be noted that the low contact resistance does not change based on the switch architecture.

5.3.3 High Endurance Experiment:

Next we tested the device to study its endurance and lifetime by connecting the device to a function generator and oscilloscope, as shown in Fig. 5-4(a). This figure shows a simplified circuit schematic for NEM switch connected to the function generator for V_{in} and the oscilloscope for $V_{out.}$. The electric model of the circuit is illustrated in Fig. 5-4(b), the function generator is connected to Source (S) while the oscilloscope is connected to Gate (G). The oscilloscope internal resistance, which is about 1 MΩ, acts in series to the contact resistance R_c and metal resistance R_m, which in total is a few kΩ.

Figure 5-4(c) shows the input voltage wave form V_{in} and output voltage wave form V_{out} as measured. The fabricated NEM switch shows a delay of 30 nS (switching time) running at 1 MHz, reflecting the maximum operation frequency of 17 MHz. However, running the NEM switch at lower speed (10 mS) shows no delay due to slow speed (similar results have been achieved by others) [52, 154]. As described earlier, the NEM switches function by hammering the source (cantilever) on the drain electrode, which might damage the contact area and consequently increase the contact resistance and shorten the switch lifetime. On the other hand, hammering could remove the native oxide layer from source (cantilever) and drain surfaces to decrease the contact resistance – a paradoxical phenomenon. Both of these competing phenomena are unwanted in context of NEM switch's continuous operation. It is to be noted that, micro-scale switch might have different material properties than occur at nanoscale dimensions [52]. In our case, the aWN_x NEM switch was operated consecutively for 10 days at the frequency 10 MHz and it completed an unprecedented 8 trillion cycles without any degradation in performance and the switch remains alive. The SEM image and I-V curve taken after 10 days look exactly the same as before starting of the endurance test (Fig. 5-1(d)). Figure 5-4(d) shows the input and output voltage waveform at low frequency 100 Hz, the switch illustrates perfect square wave profiles of both input and output voltage. Figure 5-4(e) shows the same waveform as in (Fig. 5-4(c)) but at higher frequency of 2 MHz.

When we ran the same test with another set of NEM switches fabricated of gold (Au), the switch failed only after million cycles and blew out (Fig. 2-3). The output waveform profile is affected and destroyed unlike the device fabricated by amorphous

WN_x. Gold (Au) is a poly-crystalline material, which has large crystalline boundaries that limits the nano-scaling and builds internal stress which causes operational defects in form of electrode wearing, or active part fractures or fatigue [77].

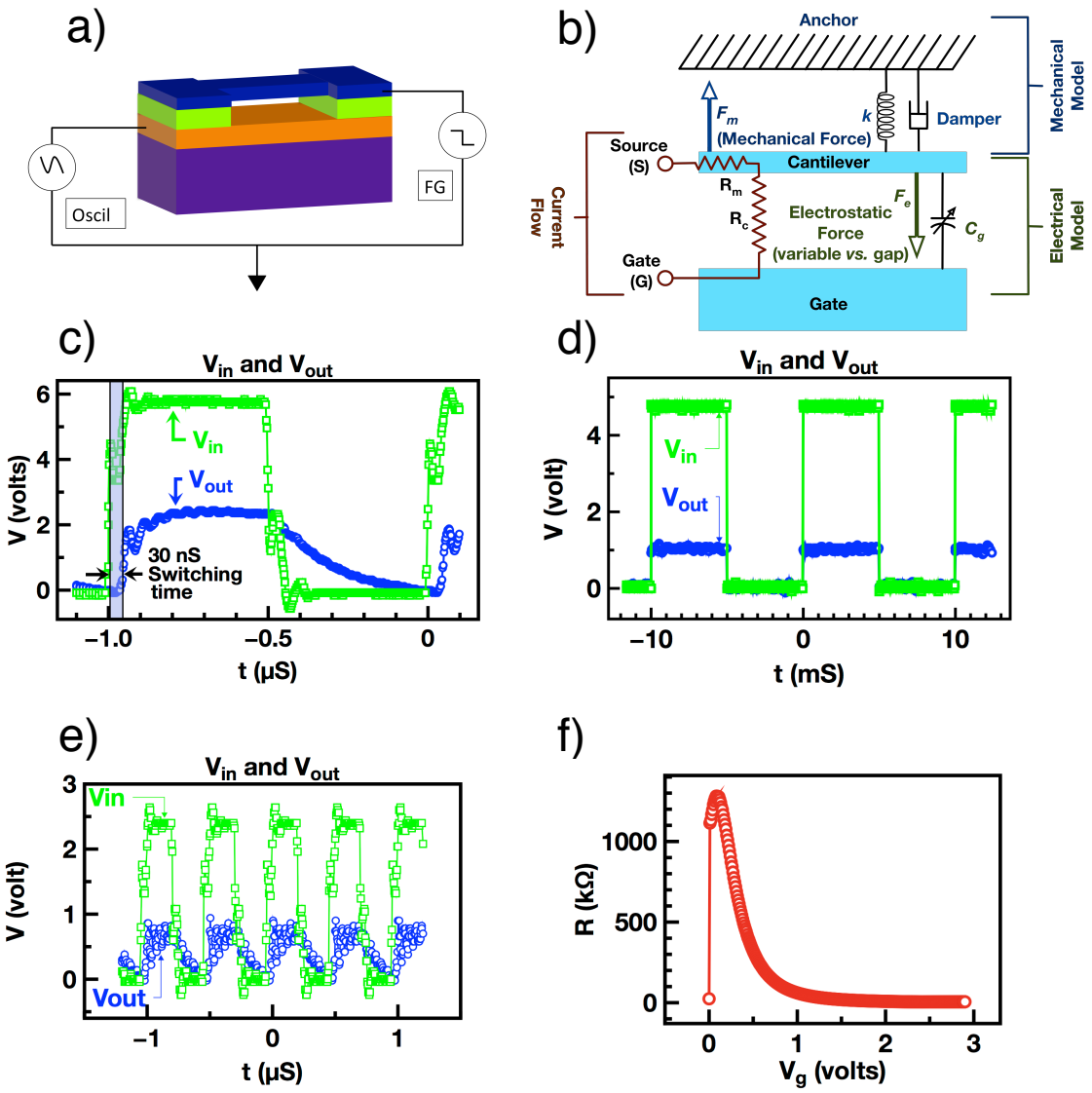

Figure 5-4 | a) Simplified circuit schematic for NEM switch; b) mechanical and electrical equivalent circuitry and schematic in different statuses; c) input and output voltage signal; d) input and output functions at low frequency 100 Hz; e) input and output functions of a high frequency 2.5 MHz; f) Contact resistance change *vs.* applied voltage.

The V_{in} and V_{out} curves depict the bouncing and settling delay of the cantilever at the pull-in state. The settling time reveals the Q of the device and the speed. Tungsten and its alloys are high density and hard material which yield higher quality factor longer damping time and higher pull-in voltage [75]. Figure 5-4(c) shows the switching time around 30 nS and settling time less than 10 nS. The quality factor for W made devices are around 60 to 100. Higher quality factor leads to longer settling time and vice versa. The impact velocity could be calculated analytically using the kinematic equations:

$$v_f = 2\frac{g}{t} \qquad 16$$

which is equal to 13 m/S. The kinetic energy is proportional to the square of velocity. Reducing the drain gap will lead to a reduction in final velocity (impact velocity) and consequently the switching power.

4. AMORPHOUS WN_X RESONATORS

The aWN_x as an alloy of transition metal has a high Young's modulus, which elevate the resonant frequency as well as the nanoscale dimensions of the fabricated devices as demonstrated by the following formula:

$$\omega_o = \sqrt{\frac{EI}{\rho A l^4}}\,\hat{\omega} \qquad 17$$

where $\hat{\omega}$ denotes a non-dimensional natural frequency. The first harmonic is used to simplify the equation which is 3.5 [115]. The resonant frequency could be approximated in simpler formula as follow [155, 156]:

$$f_o = \frac{2}{\pi}\sqrt{\frac{Ew^2}{\rho_c l^4}} \qquad 18$$

On the other hand, the high density of the amorphous metal alloy cause a reduction in the resonant frequency as they are inversely proportional. However, the high density is highly demanded in inertia base sensors such as accelerometers and gyroscope. The fabricated single clamp NEM switches described above in the previous section 4.3 have the resonant frequency in the range of MHz (2 MHz) which give a broad window of operation unlike previously demonstrated Si-based MEM switches.

The mechanical quality factor of the fabricated device could be estimated analytically from the following equation:

$$Q \approx \frac{\omega_o}{2\delta} \qquad 19$$

where δ is the damping coefficient. This relation state that the quality factor is directly related to the Young's modulus, width and thickness of the cantilever, and inversely with the length of the cantilever. Amorphous WN_x material gives an opportunity to fabricate a

high quality factor NEM devices. For the above-fabricated NEM switches in section 4.3, the analytical value of Q is in the range of 10^{13} as stated by the formula above.

5. EXPENDABILITY

Tungsten nitride (WN_x) could fulfill the demand of biodegradable material for sustainable devices. Transient electronics is a form of biodegradable electronics that physically disappear totally or partially after performing a required function. This property allows such devices to function not only in biological environments but also in zero-waste consumer electronics, secure electronics, disposable sensors and many others. This category of electronics must be integrated with a similar category of conductors. Our fabricated amorphous metal, WN_x, suites this category very well, despite not being a universal bio-element [157-173]. It has been found that tungsten dissolves into an oxide form of tungsten (WO_x) with a rate of ≈ 20-60 nm h^{-1} [157, 164]. These characteristics make WN_x an advantageous material to fabricate disposable and transient electronics. 16 hours are enough to completely dissolve a 100 nm thick amorphous WN_x in ground water at room temperature and 3 days are enough to completely dissolve a 300 nm thickness device.

5.5.1 Dissolution Rate of WN_x:

The goal in the conducted experiment is to study the dissolution rate of amorphous WN_x in different solutions at different conditions. Additionally, the dissolution behavior is recorded for different device geometries in range of simple heater to NEM switch. Starting with NEM switches, the experiment is done on different solutions at different

temperature. The NEM switches have been submerged in ground water, DI water and saline water at 0 °C, 25 °C (room temperature, RT) and 60 °C. The samples at RT and 60 °C have been sonicated. The results are demonstrated in Fig. 5-5(a).

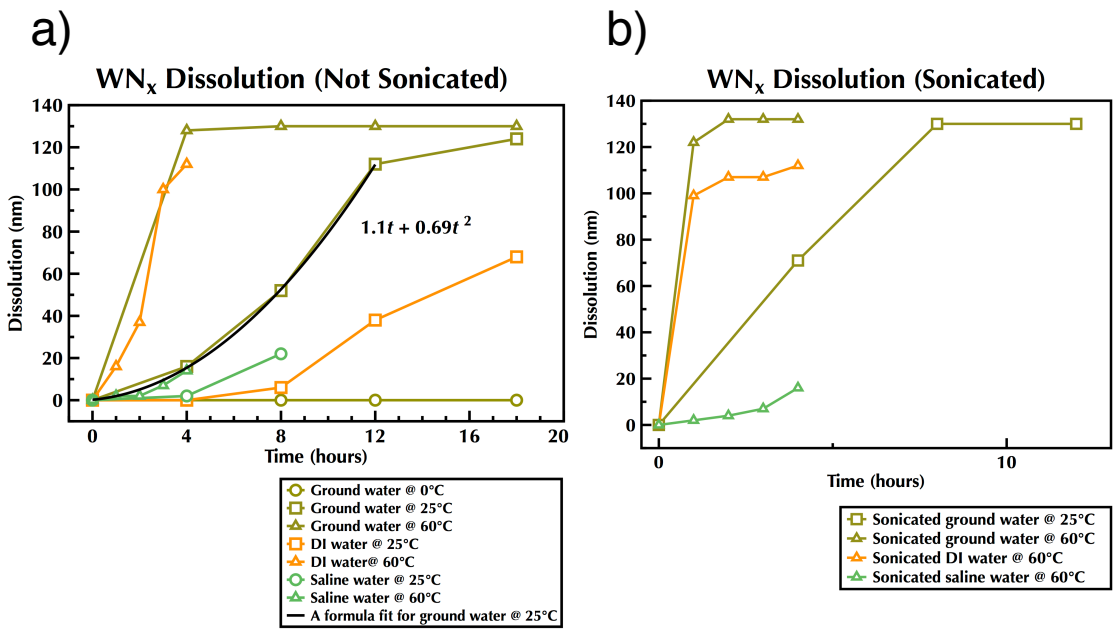

Figure 5-5 | The dissolution rate of WN_x in different solutions at different temperatures and conditions; a) with without sonication; b) with sonication.

It is observed that the dissolution rate at freezing temperature (0 °C) is almost zero, almost not dissolvable. Another observation is that the ground water (GW) is the best solvent for WN_x, better than DI water and saline water. The used ground water is the tap water which is desalinated sea water provided by the municipal. The total dissolved salt (TDS) is about 600 PPM with little alkaline base around 7.2 pH value. These results have been referenced to the Kingdom of Saudi Arabia National Environmental Standard and from the study [174, 175].

The theory behind this phenomenon is that the tungsten inside water starts the erosion process with the existence of dissolved oxygen inside the solution. This reaction at equilibrium state is as the following formula shows:

$$6H_2O + 3O_2 + 12e^- \rightarrow 12OH^- \quad (20)$$

$$2W + 16OH^- \rightarrow 2WO_4^{-2} + 12e^- + 8H_2O \quad (21)$$

yields the following redox equation:

$$2W + 4OH^- + 3O_2 \rightarrow 2WO_4^{-2} + 2H_2O \quad (22)$$

In the case of saline water, the existence of Na+ and Cl^- ions reduces the amount of dissolved oxygen in solution. After the formation of adequate quantity of tungsten oxide, the corrosion rate (dissolution rate) becomes much faster and the fabricated device starts disappearing rapidly compared to other materials, such as Si or SiO_2 [157, 164, 170]. The disappearance of the tungsten oxide takes a long time, however this is done after the disappearance of the fabricated devices. Sonication speeds up the dissolution rate rapidly, as shown in the Fig 5-5(a,b). Heat also speeds up the dissolution rate by increasing the oxidation rate. The dissolution rate of WN_x in ground water environment could be shown with the following formula:

$$\Delta h = 1.1t + 0.69t^2 \quad (23)$$

where Δh is the dissolved thickness in (nm) ($\Delta h = h_1 - h_2$ (starting thickness minus end thickness (in nm))) of aWN_x and t is time in hours.

5.5.2 Optical and SEM Pictures:

The presumption that the dissolution process starts slow and gets faster after a time has many applications that will be discussed later. As stated earlier, the dissolution experiments have been conducted on both, macro, micro and nano scale devices. The macro devices are resistive heater sputtered on PDMS substrates (Sens.), the micro scale devices are accelerometers (Acc.) and the nano scale devices are the NEM switches, Fig. 5-6(a-c).

The sputtered WNx resistive heater on PDMS (Sens.) was submerged in GW at room temperature without sonication for time intervals as illustrated in Figure 5-7. It is observed that in this macro device experiment, the dissolution process took longer time due to the large area to be dissolved and the penetration of WNx in PDMS micro pores. This penetration caused more adhesion force between WNx and PDMS. It required 36 hours to dissolve completely 300 nm thick WNx.

Macros scale devices (in our case accelerometer) have been fabricated by WN_x. Fig 5-6(b). The fabricated devices have been dissolved in GW at same conditions as the thermal heater above. Figure 5-7 shows the dissolved devices in time intervals as above. The AFM pictures in figure 5-7 are for the proof mass of the accelerometers.

Experiments at the nanoscale have been conducted on NEM switches. Figure 5-7 shows the SEM pictures of the dissolution process in GW at room temperate without sonication. It shows that 300 nm thickness NEM switch decays very fast, especially at the suspended part of the cantilever, because it is being dissolved simultaneously from top and bottom. After 16 hours, the complete part of the cantilever is gone, and after 24

hours, the entire device disappeared. The black color residual is the etched SiO2 beneath the WNx device.

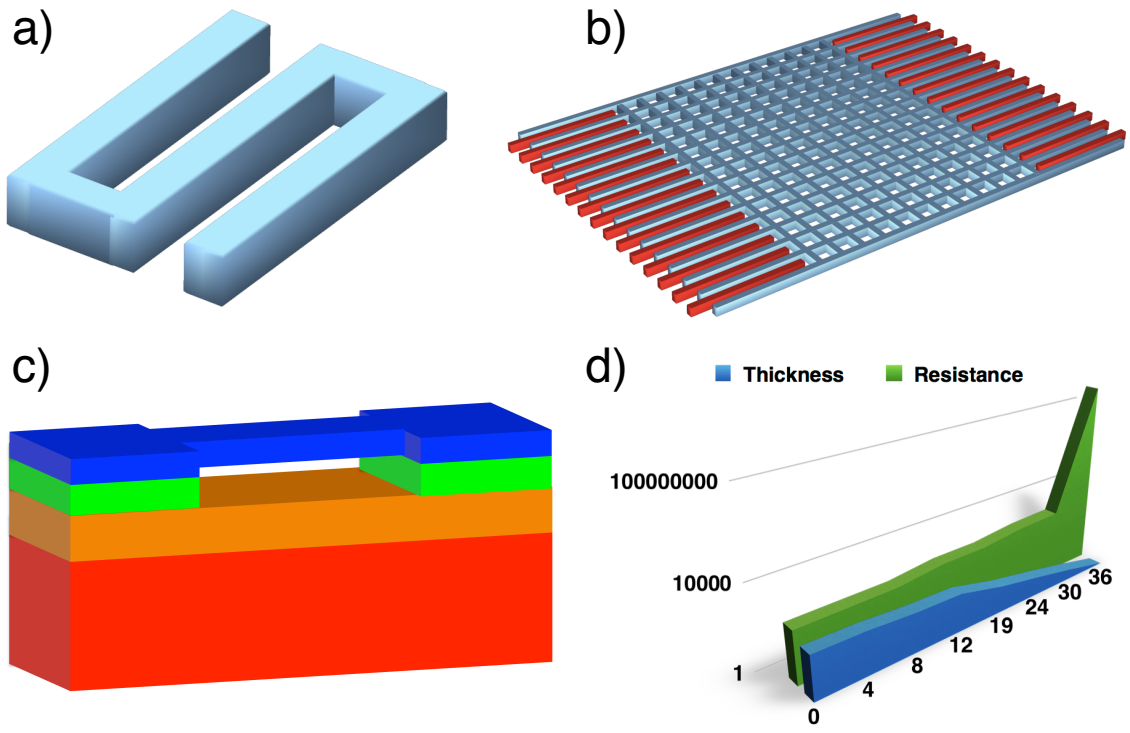

Figure 5-6 | a) a resistive heater in macro scale; b) an accelerometer in micro scale; c) a nano scale device NEM switch; d) WN_x dissolution and resistivity increment versus time.

Figure 5-7 also shows the STEM image of cross section of WN_x device dissolved in GW at room temperate without sonication. The initial device thickness was 475 nm. The STEM specimen was prepared on an FEI Helios NanoLab 400S FIB/SEM dual beam system using Pt/C deposition for sample protection. Then the HAADF (High-angle annular dark-field)-STEM images were obtained using an FEI Titan ST electron microscope operated at 300 kV. The STEM images are the most accurate at showing the exact dissolution rate in addition to proof of complete device disappearance.

Several devices were fabricated from WN_x at macro, micro and nano scales and their dissolution rates were studied. The resistivity of WN_x has been measured during the dissolution process and has been recorded in the Fig 5-6(d). The figure shows the increment in resistance due to reduction in thickness of WN_x. Figure 5-7 shows pictures of different devices during the dissolution process.

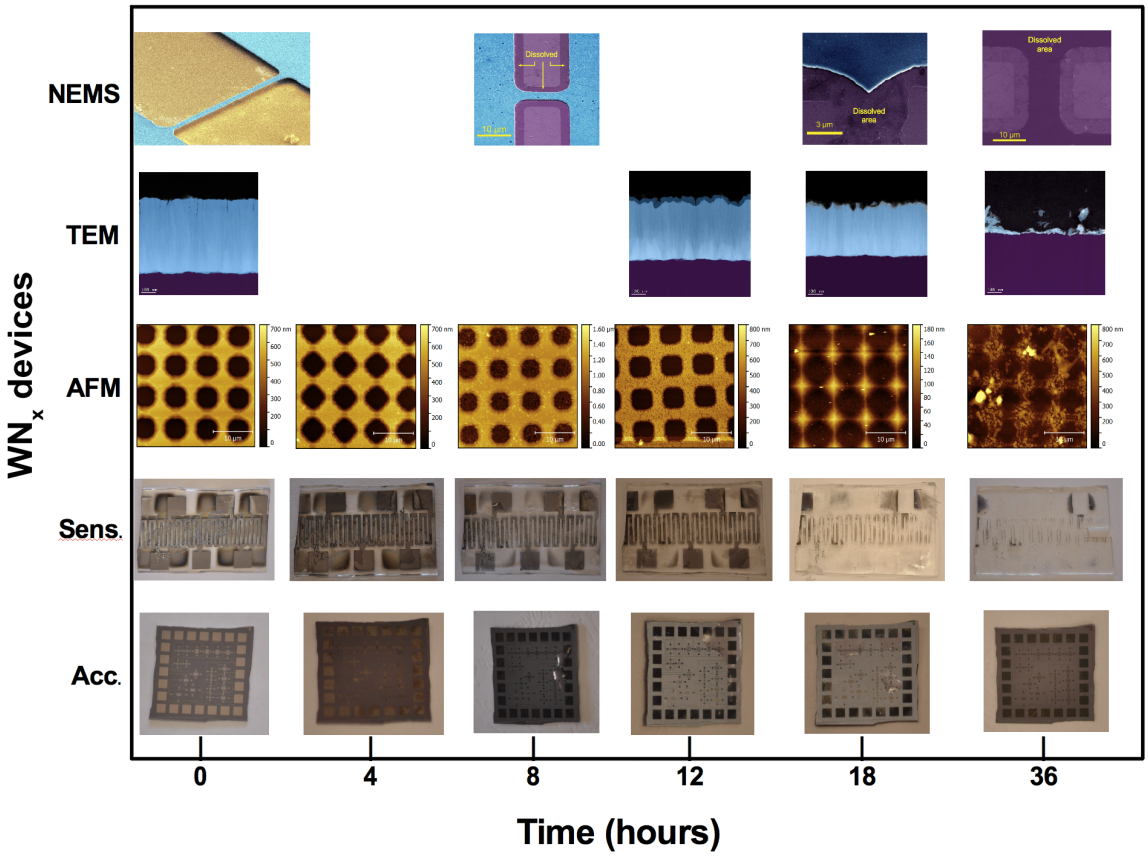

Figure 5-7 | Pictures of different dissolved WN_x fabricated devices in GW at room temperature with no sonication at different times.

6. CONCLUSION

This thesis characterizes an amorphous WN_x based nano-ribbon doubly clamped vertical NEM switch with the following attributes: (i) sub-1-volt switching operation (V_{pi} = 0.3 volt) due to high Young's modulus (300 GPa) and low dimension of the device (100

nm thick and 300 nm air-gap); (ii) high Young's modulus yields higher mechanical restoring force, F_m resulting in overcoming van der Waals and Casimir forces lowering possibility of irreversible (non-volatile) stiction; (iii) long lifetime of NEM switches with high endurance; (iv) high hardness; and finally (v) unprecedented 8 trillion cycles of switching. The aWN_x molecular structure of a closed pack atomic density originated oxidation resistance, and smooth surface resulted in less change in contact area due impact and optimal contact resistance to eliminate mechanical welding and electrical fusing from excessive heating in the contact area due to large current density. As a result, we could achieve a high ON current (0.5 mA) and moderate ON resistance (< 5 kΩ); a record endurance for any NEM switches demonstrated ever with equal pull-in and pull-out voltage eliminating any hysteresis loss and delay. Figure 5-8 shows the status quo and progress in NEM switches field and the status of this work in both ambient, air and vacuum.

Furthermore, we have demonstrated the dissolution of WNx devices in fairly short time, about three days for small sized devices in GW. The dissolution rates of WN_x under different combinations of water type, temperature and sonication were studied. It was determined that WNx dissolves in water by oxidation process that starts out slow and speeds up rapidly. The water type also impacts the dissolution rate with highest dissolution rates achieved in ground water and the lowest rates in saline water. High temperature and sonication also speed up the dissolution rate tremendously with almost no dissolution at 0 °C and increased rates at 25 °C and 60 °C. The same measurements were also performed for different WN_x device types and sizes, macro-sized resistive

heater, micro-sized accelerometer, nano-sized NEM switch, with similar results. Images were captured at different stages of dissolution and show complete disappearance of the WN_x material. This work proves that amorphous WN_x is a viable candidate for biodegradable devices which has a broad range of possible applications.

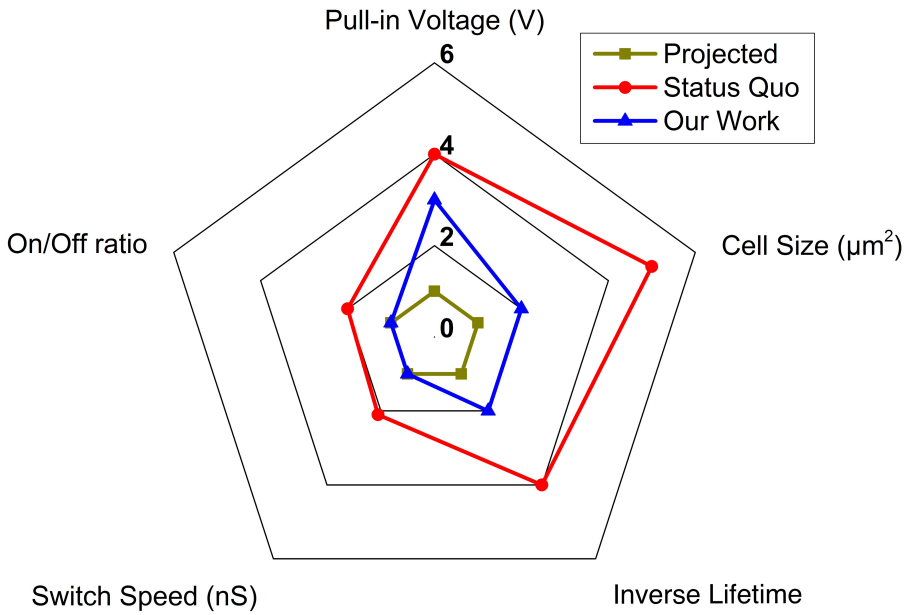

Figure 5-8 | NEM switches status quo and progress.

Based on this study, the nano-structuring of amorphous metal such as WN_x can further yield "*ideal*" NEM switches, high endurance and biodegradable devices.

Chapter 6

ACHIEVEMENTS AND CHALLENGES

1. INTRODUCTION

In this doctoral thesis we have investigated the potential of NEM switches for present day use and promising future applications. As stated at the beginning of this dissertation, MEM switches are devices currently being used in a wide area of applications, however their development has been relatively slow compared to the fast development of semiconductors in the last few decades. The transition from MEMS to scaled down NEMS has continued to be slow. The main reason behind this is the polycrystalline silicon material used for MEMS fabrication poses several limitations when used at the scaled down size of NEMS; as discussed in chapter one. Alternative materials must be found to pursue the development of this area of technology. Many materials have been researched and some presented good results, however none have been suitable for integration within existing CMOS manufacturing processes nor appropriate for future development. This dissertation presents a new material, amorphous tungsten nitride (aWN_x), which is compatible with existing CMOS manufacturing technology and its properties are not only suitable for NEMS fabrication but enables achievement of low power (sub-1 volt) and high endurance operation. Additionally, the unique properties of aWN_x make it a promising candidate for other applications such as biodegradable electronics.

2. REVIEW OF MAJOR ACHIEVEMENTS

The evolution of new technology demands inspiration, passion, hard work and patience. This research started with the foundation of MEMS technology, lead to the innovation of a new material and resulted in the fabrication of a cutting edge 3 terminal NEMS device that operates in sub-1 volt regime with high ON current and unprecedented high endurance. The achievements of this research are outlined below:

1. An innovative material has been developed, amorphous WN_x. The material shows a high degree of amorphousness, that even with annealing under harsh environment it does not convert to a poly crystalline structure. The development process passed through consecutive steps of varying different parameters of sputtering, such as the target-substrate distance, chamber pressure, gas ratio and substrate temperature. The final achieved material is targeted to overcome most of the existing mechanical and electrical failures of NEM switches. Justification behind choosing WN_x as the ultimate material to fabricate NEM switches has been explained in chapter 2. Finally, the material properties of amorphous WN_x have been studied thoroughly, including measurement of the value of the Young's modulus, hardness, electrical conductivity and surface roughness. Internal residual stress has been measured to be slightly tensile. Degree of amorphousness has been measured by XRD, TEM image, and TEM diffraction image.

2. Designs of multiple sized single clamped and double clamped vertical and lateral NEM switches have been created. The operation of these designs has been simulated by COMSOL™ software. The results have been compared with calculated

values. Divergence in values has been justified in chapter 3. Based on these calculations and simulations, two different sizes have been selected for fabrication for lateral and vertical NEM switches. The large size has calculated pull-in voltage around 10 volts and the small size has calculated pull-in voltage less than 1 volt. The final designs have been fabricated using EBL for the lateral NEM switches and UV lithography for the vertical NEM switches. EBL recipes have been extensively developed to achieve the targeted geometry. Vertical NEM switches have no critical dimensions, so UV lithography was sufficient for their fabrication.

3. The development and optimization of different processes to fabricate the NEM switches have been presented in chapter 4. Process tuning started with simple top down recipe using SU8 negative photo resist with EBL, good results were reached for large geometry, above 200 nm feature size. Fine tuning the process for less than 100 nm feature size, required a search for higher resolution photo resist. Negative photo resist is more convenient for EBL process, but a bottom up process was developed using positive photo resist, PMMA. This process gave high accuracy feature size and better resolution; however an issue with this process was stringers at the edges of structure and difficulties to lift off the WN_x from 100 nm structures. A hybrid process was developed between lift off process and etching process depositing Ni by e-beam evaporator. The stringers issue was solved but the sub 100 nm lift off issue remained. Finally, the best results came by using top down process with SiO_2 hard mask. This HM does not affect the NEM switch operation because it is removed during the release step. Successfully, lateral NEM switches with sub 100 nm feature size have

been fabricated. For vertical NEM switches EBL is not required. UV contact aligner has been used with the same top down process. Positive photo resist was used in conjunction with bright field mask which gives the same effect of negative photo resist.

4. The fabricated samples have been characterized in chapter 4. The characterization was done in ambient air environment using probe station, Keithley analyzer, function generator and oscilloscope. Larger than 200 nm NEM switches showed high pull-in voltage of about 15 volts. Consecutive cycling showed lower pull-in voltages. Smaller feature sized devices, below 100 nm, showed lower pull-in voltages starting from sub 2 volts and a few of them showed sub 1volt. Un-precedent result of pull-in voltage equal to 0.8 volt has been achieved by 3-terminal NEM switch. Low sub-threshold slope has also been achieved of 5 mV/decade.

5. The major characteristics of amorphous WN_x NEM switches have been demonstrated in chapter 5. Most of the electrical and mechanical faults within NEM switches have been overcome by using amorphous WN_x as demonstrated in the high endurance test run under high vacuum. D-Prober was used to cycle the NEM switch for more than 8 trillion cycles in 10 days. This high number of cycling has never been presented before. The delay time was 30 nS. Even after the endurance test was over, the NEM switches were still in operational condition. The other, no less important, interesting feature of amorphous WN_x fabricated devices is its dissolvability. Amorphous WN_x is dissolves in ground water at about 20 nm h^{-1}. This is a critical

phenomenon that could help in building sustainable and degradable devices. These features play crucial roles in many fields.

3. FUTURE WORK

This thesis concludes by highlighting the future prospects of using amorphous WN_x to fabricate different devices. The properties of amorphous WN_x make it a highly attractive material for use in the nano-scale regime as well as for high endurance devices. Regarding device fabrication, improvement and optimization in the EBL process can be done to target the sub-10nm regime. Specifically, proximity effect correction software must be used with optimized parameters to overcome the over and under exposure for critical patterns. Exposure energy *vs*. beam focus array should be developed to get the best parameters for each structure layout. Spacer formation process should be utilized to get a self-aligned critical nano size patterns. Simulation software should be used for DUV process to finalize the mask design. From the material perspective, more work should be done on amorphous WN_x to be utilized such as low cost material to fabricate sensors, conductors, NEM and MEM switches, heaters and many other applications devices that withstand harsh environment conditions. Further research should be conducted to find other ways to fabricate amorphous WN_x alloys for utilities and industrial use, as it has shown many interesting characteristics.

6.3.1 Sub-10 nm NEM Switches

In order to get a NEM switch to operate at less than 10 aJ energy, the gap should be less than 10 nm to utilize the adhesion force for closing the switch. This type of switch is

the perfect match to adiabatic style switching. The lithography should be engineered excellently with extreme caution to achieve these critical dimensions. This type of NEM switch could be vertical or lateral style, but the vertical one will be easier to fabricate. EBL or DUV process could be used to achieve these critical dimensions.

6.3.2 Special Type Switches

Dissolution characteristics could be used to fabricate safety switches for sensitive devices. High density of WN_x gives a preference to fabricate high sensitivity inertia based sensors such as accelerometers and gyroscopes. WN_x dissolution characteristics could be used for final tuning the mass of the switch according to special circumstances. In addition, different dissolution rates for different solutions could be utilized to fabricate ion and salt sensors.

6.3.3 Special Sensors

The WN_x material is very attractive to fabricate sensors because of the high resonance frequency and quality factor. In addition, WN_x is harsh environment resistant and expendable. Different bio-sensors could be fabricated using this material. In addition, WN_x is one of the best candidates for high security military devices fabrication for the mentioned characteristics. More research should be done on how to utilize the dissolution rate for building certain functional sensors and switches.

6.3.4 High Power MEM and NEM switches

The WN_x material is highly conductive (metal like) and could be used for high power and high current flow devices. High hardness, elasticity, and moderate surface roughness and contact resistance give the aspect of non-welding and no hysteresis operation. Therefore, there will be minimum energy loss and welding effect of high current flow. Such type of switches should be fabricated and tested.

Appendix A

FABRICATION PROCESS

1. BOTTOM UP PROCESS

A bottom-up process is opposite from the top-down process. The subject material (aWNx in this research) is deposited on top of patterned PR. When the PR is removed the unwanted material on top of the PR will also lift off (sometimes called lift-off process) [22, 24]. There is no need for etching in this process (Fig. A-1). For EBL process, a positive photoresist (PPR) is recommended to minimize the exposure time. In this research, PMMA positive photoresist is used because of its availability. Due to the stringers at the edge of the NEM switches, this process was not used in fabrication.

A.1.1 Deposition of PECVD SiO_2

As in section 2.1 the process starts with highly doped Si substrate cleaned in a piranha solution.The silicon dioxide layer is deposited by PECVD tool. Start with <100> orientation silicon substrate cleaned in piranha solution to remove all the residuals polymers and impurities. Then deposit 1 to 3 μm film of SiO2 by PECVD tool. The PECVD oxide is more desired than furnace oxide (FOX) because it has a faster deposition and release time than the FOX due to its weaker bonds.

A.1.2 PR coating, PMMA

Next, the positive tone photoresist (PMMA) is deposited on top of the SiO2 layer. It is better to use a thick resist, preferably above 800 nm thickness. The coating speed should be high to achieve an uniform coating across the wafer.

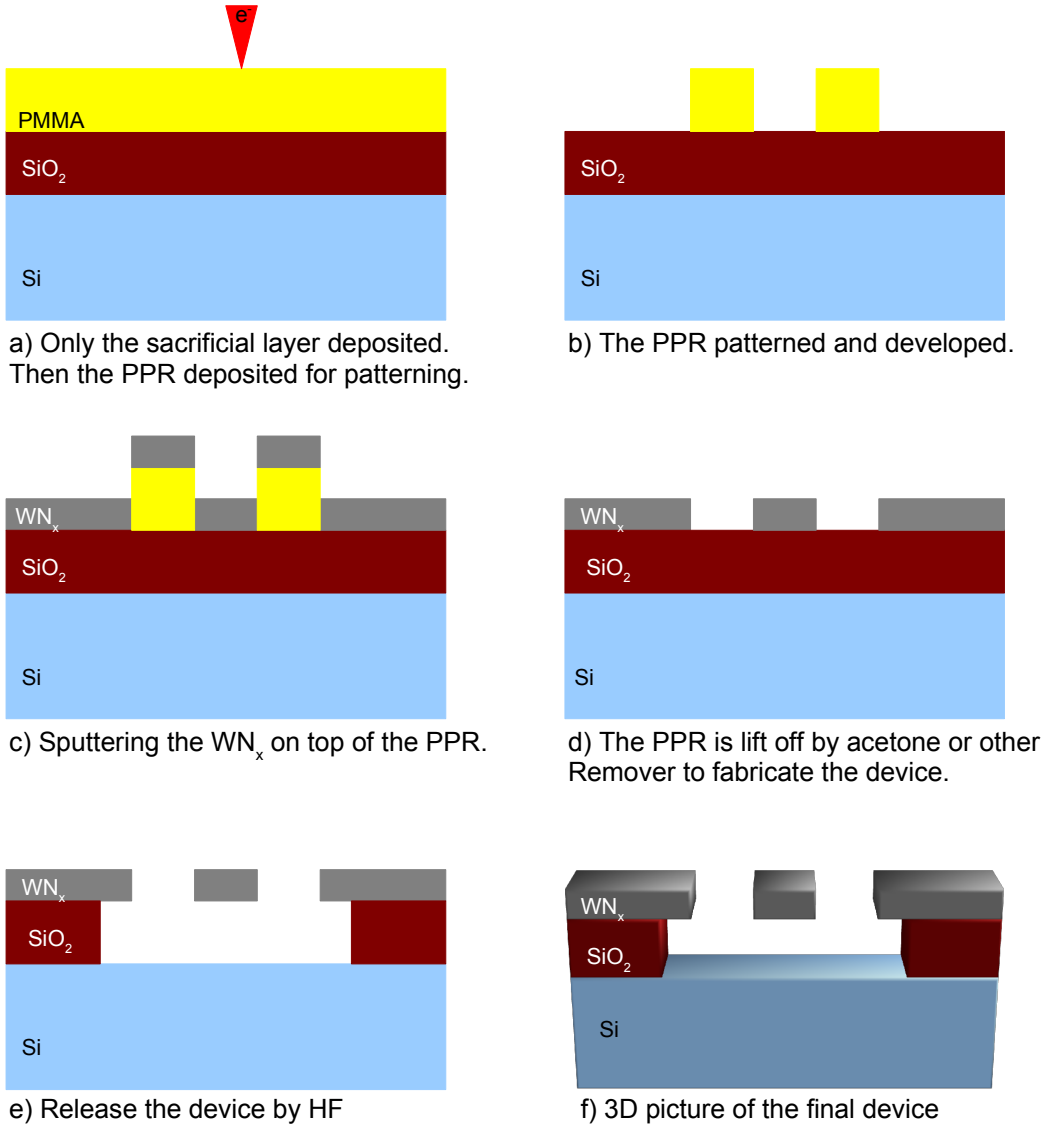

Fig. A-1 | The steps for bottom up process.

A.1.3 EBL Exposure

After coating the resist, the substrate is diced and exposed using EBL tool. As stated before, PMMA sensitivity is very low. The EBL settings are as follows:

- Dwell time: 1.0 μS.
- Fine feature dwell time should be doubled and the surrounding reduced by 10% to overcome the proximity error.
- Exposure current is 500 pA.
- Exposure flashes density is 60,000 dots / 1,200 μm die

Develop the resist with the standard developer of PMMA. It is better to use bilayer resist for lift-off process to minimize the strings at the structures' edges.

A.1.4 Deposition of PVD AWNx and PR lift off

After patterning the PR, amorphous WNx is deposited by the sputtering tool, as explained in chapter 2. It is best to remove the resist very quickly following aWNx deposition as the resist can harden over time which limits its removability. For PMMA, acetone with ultrasonic agitation is sufficient. The process took its name from this step, lift-off process.

A.1.5 HF Release

The NEM switches are released by removing the SiO2 sacrificial layer using HF, following the steps as stated in the former sections.

It is noted that the thick layer of PR caused high proximity error. Therefore, it is recommended to use thin resist, but the thin layer of resist is not enough to pattern out the

above deposited layer. Another issue with this method is that stringers exist at the edge of the side wall. Therefore, this processing method is not very reliable (Fig. 4-11). The next section will discuss a hybrid process to overcome these issues with the lift off process.

2. HYBRID PROCESS

This process is a combination of both the bottom-up and the top-down processes. In this process, the hard mask (HM) is deposited with the bottom-up process (lift-off) and the aWNx is etched as in the top-down process. In this process, we have chosen the metal nickel (Ni) as the HM because nickel has a very high etching resistivity for both aggressive gases, SF6 and Cl2.The process steps have been illustrated in Fig. A-2. The process steps are as follow:

A.2.1 Deposition of the stack layers

As in section 2.1 the process starts with highly doped Si substrate cleaned in a piranha solution. Then a 1 to 3 μm thickness film of SiO2 is deposited by PECVD tool. After that, 100 to 500 nm thick amorphous WNx film is deposited as explained in chapter 2. Now the substrate is ready for the next steps of micromachining (lithography).

A.2.2 PPR coating, PMMA

The substrate is coated with positive tone photoresist (PMMA) with a thickness in the range of 300 - 400 nm. Low thickness photoresist is more viable for sub-100 nm structures. The coating speed should be high with high acceleration to obtain a uniform film.

A.2.3 EBL Exposure

After coating the resist, the substrate is diced and exposed using EBL tool. As stated before, PMMA sensitivity is very low. The exposure parameters will be same as those stated in section 4.3.

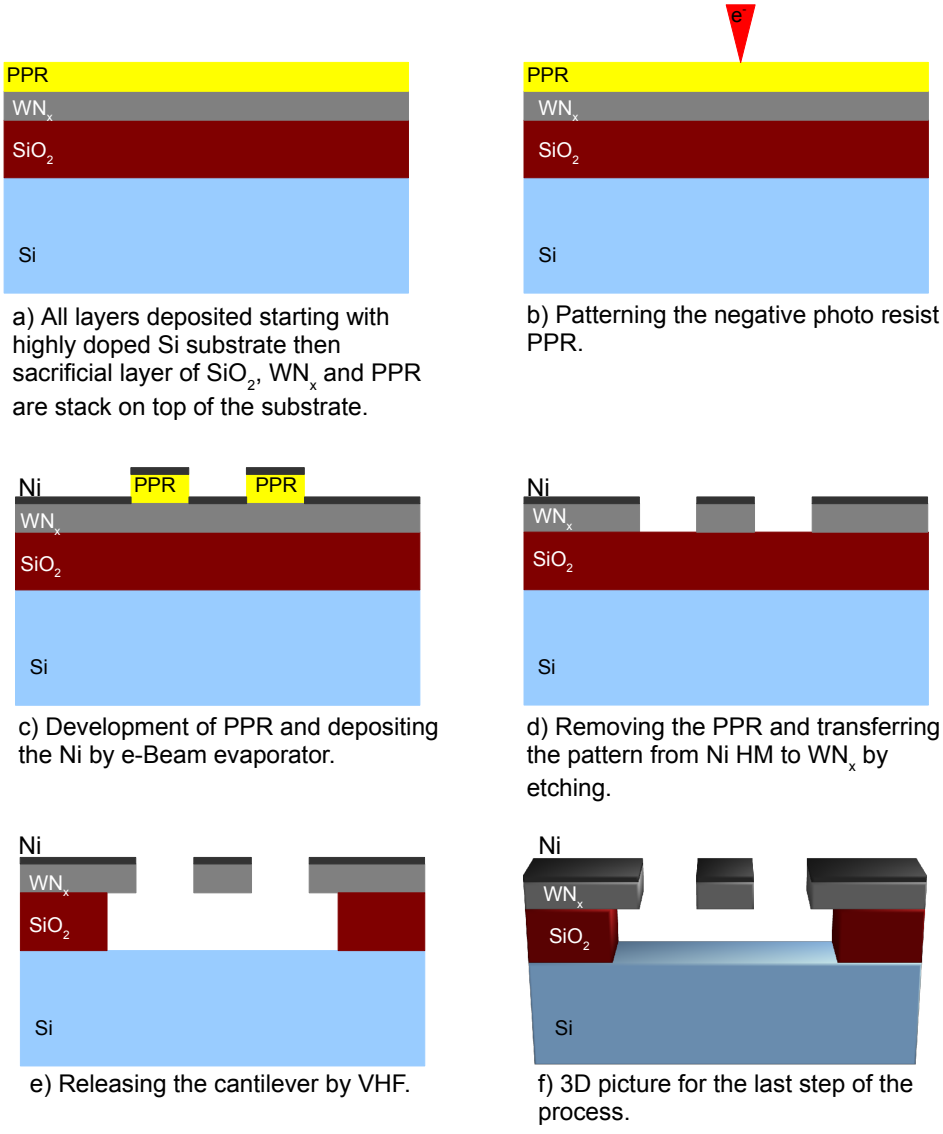

Fig. A-2 | The process steps for hybrid process.

A.2.4 Deposition of Ni

This step is unique to this hybrid process and is not done in the former recipes. The Ni (which is the HM for the WNx) is deposited by Ebeam evaporator. Small pieces of Ni (chips) are placed inside an alumina crucible (very brittle crucible which requires extra precautions) and evaporated by electron beam. The required thickness is about 30 nm using a deposition rate of about 02 nm/min. Then the substrate is submerged in acetone with agitation to remove the PR and lift off the excess nickel on its top.

A.2.5 Etching the aWNx with Ni HM

The aWNx metal layer is etched through the openings in the Ni HM using Cl2 gas. Ni is highly resistive to Cl2 gas. Follow the same recipe as in section 3.4.

A.2.6 HF Release

Released as stated formerly.

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