NANOSCALE ELECTRODE AND DIELECTRIC MATERIALS, PROCESSES AND INTERFACES TO FORM THIN-FILM TANTALUM CAPACITORS FOR HIGH-FREQUENCY APPLICATIONS

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NANOSCALE ELECTRODE AND DIELECTRIC MATERIALS, PROCESSES AND INTERFACES TO FORM THIN-FILM TANTALUM CAPACITORS FOR HIGH-FREQUENCY APPLICATIONS

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[Dedicated to my parents]

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SUMMARY

Smart systems have continuously evolved with the integration of computing, communication, power, and sensing functions that utilize heterogeneous technologies such as digital, RF, analog, MEMS, sensors and optics in ultra-miniaturized form-factors with escalating component densities. This entails the use of multiple power converters for specific voltage and current applications. These power convertors invariably utilize components such as capacitors and inductors to store and release the energy in specific intervals determined by the switch frequency. Today's components with low volumetric density and thick form-factors are a major roadblock to miniaturization of the power modules. Moreover, such components are placed far away from the chips leading to large interconnect parasitics and lower operating frequencies. On the other hand, thinfilm passive technologies are limited to low densities and would require a large area to meet the required capacitance or inductance values. Hence, novel thinfilm technologies with high densities and small form-factors are required to enable miniaturization and performance at high frequencies. However, processing high surface area electrodes as thinfilms with substrate-compatible processes, and achieving low leakage currents and low ESR (equivalent series resistance) for high frequency stability are major challenges to accomplish these goals. Furthermore, novel packaging technologies are required to integrate these high-density passives as thin-films in substrates.

This thesis addresses these challenges with tantalum-based ultrathin high-density capacitors at higher operating frequencies with lower leakage properties and their integration in silicon substrates. The thesis also explores titanium-based high-density capacitors with high-permittivity titania as dielectric to improve the capacitance density

and investigates the leakage properties of the titania dielectric as well as its chemical composition.

The first part of the thesis focusses on the processing of high-density capacitors as thin-films based on tantalum with low leakage properties (< 0.01 μA/μF) and for high-frequency applications in low power modules. The anodization kinetics and the underlying leakage current mechanisms are investigated to provide optimal process guidelines. The capacitors demonstrated high capacitance density of 0.1 $\mu F/mm^2$ at 1-10 MHz in form-factors of 50 μm, which corresponds to 6X higher volumetric density relative to the commercial capacitors.

The second part of the thesis demonstrates the integration of the aforementioned tantalum-based high-density capacitors as thin-films on silicon substrates. The high-density capacitors as thin-films were laminated onto silicon substrates followed by planarization, via-drilling, lithography and metallization.

The last part of the thesis explores the use of titanium as an alternative material for high-density capacitors. The chemical structure and electrical properties of anodized titania were investigated for their application as conformal ultra-thin dielectrics on high-surface-area titanium electrodes.

In summary, the thesis demonstrates fabrication, characterization and integration of ultrathin power capacitors as thin-films for high-frequency applications with low leakage properties.

CHAPTER-1

INTRODUCTION

1.1 Strategic Needs

Miniaturization and performance enhancement of passive components are the primary drivers for electronic component technologies. Today's components face major roadblocks in meeting these two parameters in future electronic systems. These limitations predominantly arise from current microscale materials with inadequate properties and their processing constraints. Nanoscale materials provide unique and unparalleled opportunities to overcome these challenges. They show higher volumetric energy storage density and efficiency because of their inherently superior properties. These include properties such as high surface-area electrodes, high-quality dielectric, self-healing characteristics among electrodes and frequency-stability for capacitor applications. For inductor applications, nanomaterials offer several advantages such as low coercivity, high resistivity, high field anisotropy, and high saturation magnetization [1]. Nanomaterials are also processable as thin-films on a variety of substrates into a variety of architectures at lower temperatures. Nanostructured components, thus, can comprehensively address the future system component needs.

The key performance metrics for today's and next-generations capacitors are volumetric capacitance density, leakage current, equivalent series resistance (ESR) and operational frequency. These parameters are governed by electrodes and dielectric materials and structures. The fundamental equation that governs the capacitance is given as:

$$C = \frac{A\varepsilon\varepsilon_r}{t} \qquad (1)$$

where A = Surface area of the electrode, ε = Permittivity of vacuum, ε_r = Relative permittivity of the dielectric, and t = thickness of the dielectric. Equation (1) suggests that high capacitance densities are achieved using one or all of the three factors: thin dielectrics, high-permittivity dielectrics, and high-surface area electrodes.

Several approaches utilizing the above-mentioned parameters have led to key capacitor technologies. These include MLCC (multilayered ceramic capacitors) [2], trench capacitors [3], electrolytic capacitors [4] or ferroelectric thin-film capacitors [5] (Fig-1.1).

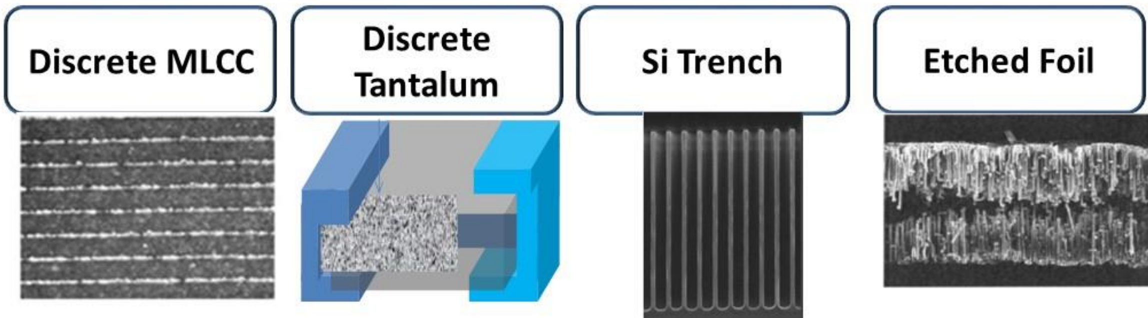


Figure 1.1: Key capacitor technologies utilizing high surface area electrodes or high-permittivity dielectrics

In MLCCs, high-permittivity ferroelectric films [6] such as BT (barium titanate), PZT (lead zirconate titanate) are patterned with electrodes and layered such that they are connected in parallel to increase the effective surface area. They achieve high capacitance density from stacked electrodes contributing high surface area and low ESR leading to high-performance capacitors. Though MLCC still maintains highest market share among capacitors with lowest ESR, highest frequency-stability, and capacitance densities, they are restricted by their processing and packaging limitations. They are manufactured as discrete components and assembled on the system board or embedded in the substrate [6]. Trench

capacitors, on the other hand, are silicon integrated capacitors that achieve high capacitance by forming deep trenches in silicon substrates to increase the electrode area, followed by a conformal dielectric film and counter electrodes [7].These processes require techniques such as ALD (Atomic Layer Deposition) and plasma etching that have low manufacturing throughput and are expensive.

Capacitors that are directly deposited as thin-film layers during substrate or wafer fabrication provide proximity advantages to active devices for high performance, while resulting in simultaneous miniaturization. These thin-film layers are within 30-40 microns from the active devices, while the capacitors themselves may range from 1-50 microns in thickness. This potentially results in much superior system performance. However, these types of capacitors have other limitations. These include defects that form during the capacitor processing, thus affecting not only the yield of the capacitor but also of the entire substrate [8]. As a result, they tend to be expensive and are not scalable to high-volume manufacturing. In addition, achieving very high capacitance density with substrate-compatible materials and processes is yet another challenge.

Today's tantalum capacitors are formed from porous tantalum electrodes that are anodized to form conformal dielectrics. Counter electrodes are deposited on these porous preforms to complete the capacitor structure. They achieve high capacitance densities, low leakage and high reliability [9]. These capacitors are however typically manufactured as thick discrete components that are only surface-mounted on the system board [10]. The large size and high processing temperatures of Ta electrodes limit them to be processed and

integrated as thin-films on active silicon [11]. The thesis addresses these issues by employing nanoscale materials and substrate compatible processes.

The volumetric capacitance densities for different approaches are compared in Fig-1.2, illustrating lowest densities for thin-films and trench capacitors compared to MLCCs, followed by tantalum capacitors. Because of their unique properties, nano-capacitors can achieve superior performance compared to the current approaches as also illustrated in Fig-1.3. Nanostructured electrodes create ultra-high surface area for enhancing the capacitance density while thin defect-free nano-dielectrics can achieve high capacitance with low leakage, and can be effectively created by electrochemical processes. Processing of conducting polymers at nanoscale also enables high yield and reliability because of their conformality and self-healing characteristics. Such ultra-thin nano-capacitors can be processed in 3D package architectures with GT-PRC's 3D IPAC (Integrated Passive and Active Components) concept, as also illustrated in the Fig-1.3.

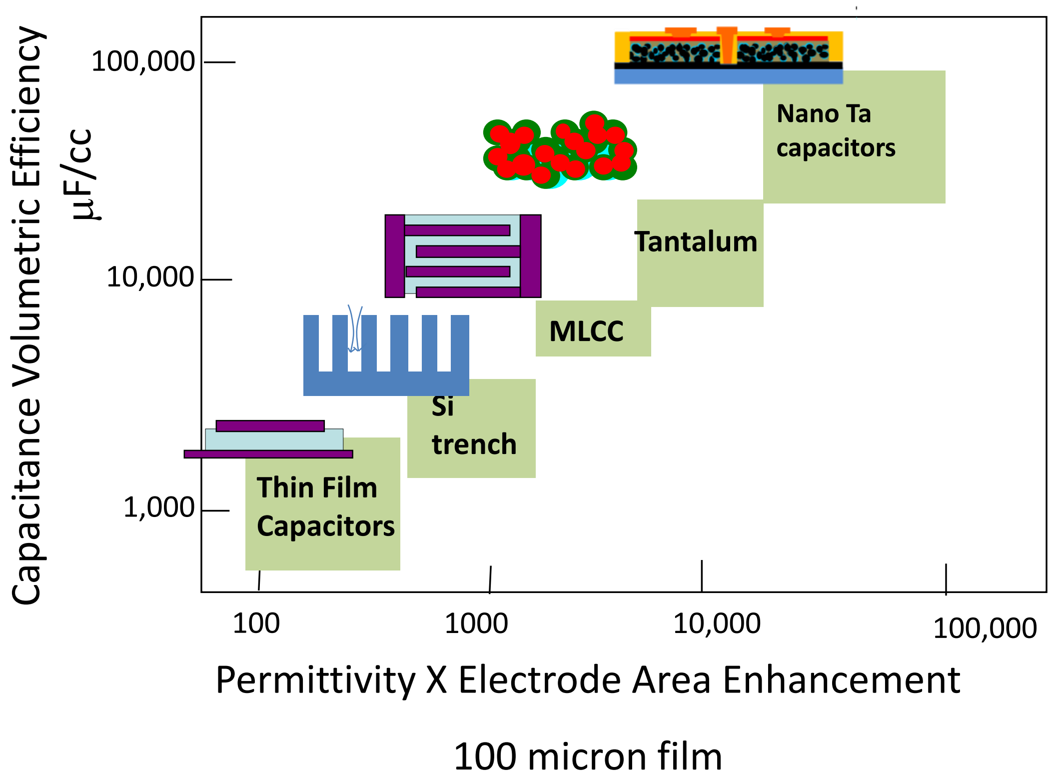


Figure 1.2: The developed capacitor technology benchmarked with state-of-the-art capacitor technologies

Nano-capacitors, however, face one key limitation. They result in a narrow resistive path between the dielectric and the current collector owing to conducting polymer or conducting oxide that has limited electrical conductivity, which increases the ESR. The high ESR results in poor frequency-stability because of the long charge-discharge times, which are directly proportional to the product of R and C [12]. Incorporation of low-conductivity cathodes for self-healing and high yield further degrades the ESR. Achieving substrate-compatible thin capacitors with porous tantalum high surface area electrodes, nanoscale conformal dielectrics with high dielectric strength and low defect densities, and counter-electrodes conformally deposited over the dielectrics to achieve low ESR can overcome this limitation. This forms the key focus of this thesis.

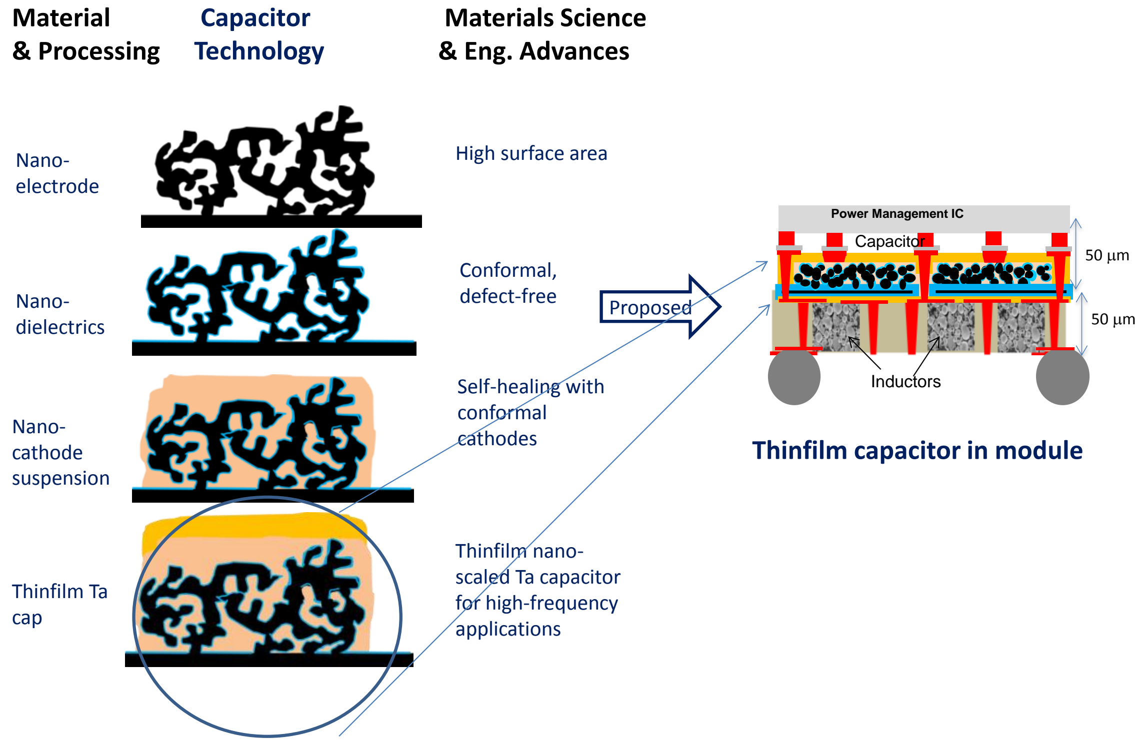


Figure 1.3: Nanoscale materials, processes and integration structures for high-performance and ultraminiaturized Ta capacitors

1.2. Research Objectives

The objectives of this research are to fabricate, characterize and integrate thin-film tantalum capacitors with high volumetric density, low leakage current, and high reliability with high-frequency-stability using nanoscale electrodes and dielectric processes. The specific quantitative objectives of the proposed research are compared with the prior art in Table-1.1.

Table 1.1: Objectives vs state-of-the-art, and challenges for the proposed research.

	Prior Art	Objectives	Challenges
Volumetric capacitance density (μF/mm^3) @ 5 MHz	0.3	2	Nanoscale Ta as high surface area electrodes
Leakage current (μA/μF)	0.1	0.01	Conformal ultra-thin dielectrics with low-defect density
Operating Frequency	≤100 KHz	1-10 MHz	Conformal, low-resistivity cathode in nano-porous structure; Low resistance contacts and interfaces
ESR (mOhms)	50	50	
Thin-film capacitor integration	SMD	Thin-film on silicon	Metal-polymer interfaces with poor adhesion and interfacial resistances

1.3. Technical Challenges

The above-mentioned objectives pose four key technical challenges. These are compiled in the last column of Table 1. The details of the technical challenges are described in the following section.

1.3.1 Nanoscale Ta as high surface area electrodes

Traditionally, in high surface area tantalum capacitors, the electrode surface is generated by partially sintering micron sized Ta particles around a Ta wire. Obtaining the requisite volumetric density in thin form-factor creates a major bottleneck in capacitor miniaturization. With traditional tantalum capacitors, lead-frame packaging of the tantalum capacitors further lowers the capacitance density. For example, a Panasonic 220 µF capacitor with sintered tantalum as the anode and conducting polymer as cathode comes in geometries of 3.5 mm X 2.8 mm and thickness of 1.9 mm yielding a volumetric capacitance density of 12 $\mu F/mm^3$ [13], which reduces to < 0.5 $\mu F/mm^3$ at frequencies above 1 MHz. Furthermore, sintering Ta particles as thin films on most substrates pose a major challenge due to their high temperature of sintering (> 1500°C) that organics, silicon and glass substrates would not be able to sustain. The thesis addresses this challenge by forming highly-porous and thin Ta films on micron-thick Ta foil at lower sintering temperatures and is described in detail in Task 1.

1.3.2 Conformal ultra-thin dielectrics with low defect density

Achieving an ultra-thin, high-permittivity dielectric by electrochemical process remains a major barrier in capacitor technology. Electrochemical dielectric deposition remains most reliable, low-cost process to achieve highly-conformal dielectrics at low temperatures and

cost. Anodization kinetics differs for dielectrics grown on planar tantalum and porous anode with different porosities. In a sintered electrode system, the local field strength, as well as the local ionic current density, could lead to different oxide formation rates and different dielectric thickness for oxides at different depths of the electrodes [14]. This leads to defects such as pin-holes and electron and ion traps in the dielectric resulting in higher leakage current and a drop in reliability at higher bias. The challenge is addressed by growing thin, conformal dielectrics with minimum defect density using the process of anodization and is discussed in Task-2.

1.3.3 Conformal, low-resistivity, cathode in nano-porous structure

High volumetric capacitance density, frequency-stability, and high yield require self-healing cathodes with low ESR. Conducting polymers have lower conductivity compared to metals, leading to higher electrode resistivity and high ESR [15]. Designing the cathode material and process to facilitate complete electrode coverage while retaining conductivity and self-healing properties is a key challenge in the current study.

Traditional cathode materials such as inorganic conducting oxides, organic conducting polymers are designed to impregnate the porous architecture that has larger pore size and distribution. From a processing stand-point, pre-polymerized conducting polymers readily infiltrate into the commercial Ta capacitors with cylindrical geometry. The cathode can readily access the high surface area anode by flowing along a radially inward direction. However, the presence of tantalum foil as carrier substrate supporting the porous Ta anode blocks the cathode infiltration from one side making it harder for the cathode to infiltrate the thin-film porous anode systems. Hence, cathode flow profile for a thin-film system differs from that of cylindrical geometries. This affects the accessed surface area of the

anode and therefore, the effective capacitance density of the capacitor. Non-conformal or thinly-coated cathode on high surface area anode also increases the ESR, causing capacitance droop at a higher frequency [16]. This challenge is addressed by using two part conducting polymer for better infiltration and better conductivity in Task-3.

1.3.4 Metal-polymer interfaces with poor adhesion and interfacial resistances

The capacitor structure comprising of tantalum oxide - fragile conducting polymers- gold interfaces presents mechanical reliability issues because of inferior adhesion strength of metal with an organic polymer. Polymer-based current collectors such as silver paste and carbon black add interfacial resistance, in addition to increasing the device thickness by several microns. The interfacial resistance between the conducting polymer and metal current collector increases the effective ESR leading to capacitor roll-off' by 200 KHz [17]. Formation of non-Ohmic contact (polymer and carbon paste) at the interface also increases the leakage current because of Schottky-based electronic defects [14]. The challenge is addressed by employing direct metallization of evaporated metal on conducting polymer and is discussed in Task-4.

1.4. Research Tasks

Four research tasks are defined to address the above-mentioned technical challenges and are compiled in Table-1.2. These tasks are described in this section. The process and the materials used for the fabrication of the proposed thin-film Ta capacitors are briefly described before defining the tasks.

High surface area anodes are fabricated by printing tantalum paste onto tantalum foils into pre-defined patterns, followed by sintering at 1200°C and 5E-8 bar. This is followed by conformal dielectric growth through the process of anodization. A conducting polymer that acts as a cathode is infiltrated into the nano-porous Ta by solution dipping process, followed by low-temperature baking to remove the solvent from the conducting polymer. The polymer is subtractively-patterned using RIE with evaporated metal (Au/Cu) as the etch mask. Fig-1.4 illustrates the process steps for fabricating the high-density capacitors.

Table 1.2: Challenges and tasks for the proposed research

Challenges	Tasks
1. Nanoscale Ta as high surface area electrodes.	1. Fabricate high surface area, printed nano-porous Ta anode.
2. Conformal ultra-thin dielectrics with low-defect density	2. Grow ultra-thin, conformal, high-permittivity dielectric using electrochemical process
3. Conformal, low-resistivity cathode in nano-porous structure; Low-resistance contacts and interfaces	3. Model, design and develop the cathode deposition process in nano-porous architecture
4. Metal-polymer interfaces with poor adhesion and interfacial resistances	4. Direct metallization of cathode with thin-film metals

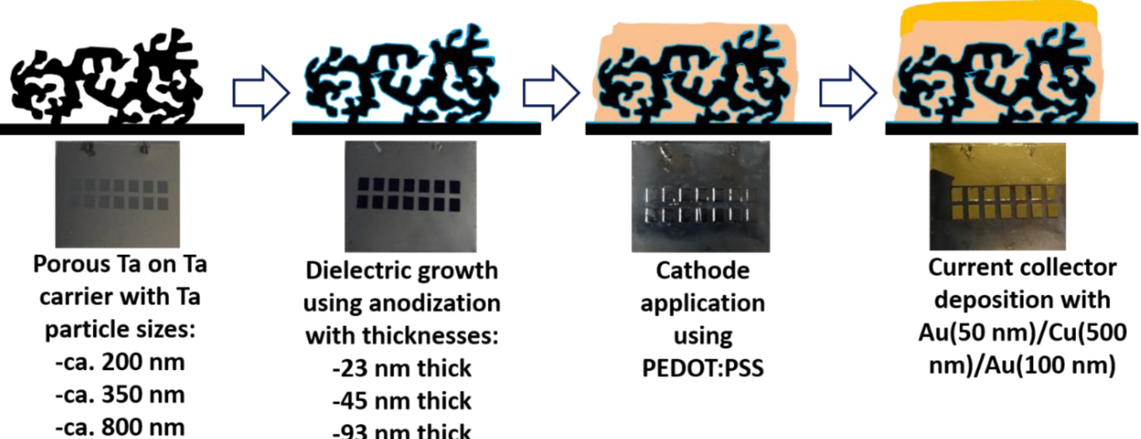


Figure 1.4: Process flow describing the fabrication of printable thin film tantalum capacitor array

1.4.1 Task-1: Fabricate high surface area, printed nano-porous Ta anodes

The objective of this task is to fabricate thin-film Ta anodes using nano-particles to address the challenges of volumetric density and capacitor miniaturization. Anodes were fabricated by stencil printing Ta paste formulated with organic binders and solvents. The organics were de-bindered, followed by sintering of Ta particles at 1200°C and 5E-8 bar to form the high surface area anode. Lowering the particle size increases the surface area of the anode, decreases the sintering temperature, but also reduces the pore fraction due to particle coagulation. Pore sizes were engineered by varying the polymer to tantalum metal ratio to yield anodes with reduced packing density. This opened up pores inside the porous electrode structure allowing cathode to infiltrate inside the deep pores of the anode.

1.4.2 Task-2: Grow ultra-thin, conformal, high-permittivity dielectric using electrochemical process

The objective of this task is to address the challenge of poor and non-conformal dielectric in thin and printed Ta anode by growing thin, conformal dielectrics with minimum defect density. Tantalum being a valve metal has a high oxygen affinity and is readily oxidized to tantalum oxide. The dielectric was grown on high surface tantalum anode by the process of anodization using phosphoric acid chemistry. Anodization was performed in steps to drive the tantalum and oxide ions across the dielectric in a controlled manner that led to a uniform growth rate of dielectric on the high surface area anode with conformal coverage and minimal defect density. Dielectric quality was investigated using leakage conduction analysis.

1.4.3 Task-3: Model, design and develop cathode deposition processes in nano-porous architecture

The objective of this task is to form a thick and conformal coating of conducting polymers in nano-porous anodes to improve ESR and frequency-stability of the capacitor. The conducting polymer with low viscosity infiltrates the pores of the anode and access the anode leading to higher capacitance density and better coverage, which would eventually lower the ESR and increase the operating frequency.

1.4.4 Task-4: Direct metallization of cathode with thin-film metals

The objective of this task is to have a low-resistivity cathode-current-collector interface and subsequently characterize the finished capacitor with lower ESR. This was done by reducing the number of interfaces contributes to lowering the ESR of any capacitor. The direct metallization approach of evaporated metal-conducting polymer was studied and compared with traditional metal-polymer composites (C-black/Ag-paste). The fabricated capacitors were characterized for ESR, frequency-stability using an impedance analyzer. ESR contributions from anode, cathode and interfaces will be de-embedded from various test-structures. This is followed by integration of these capacitors on silicon.

1.5. Dissertation Outline

Chapter-2 presents the literature review of key capacitor technologies with an emphasis on their functionality, architecture and application. The state-of-the-art power modules are also discussed in this section followed by the key capacitor technologies which are discussed next.

Chapter-3 presents the work on development of high-density thin film tantalum capacitors. Anodes with different particle sizes were used to optimize the capacitance density and operational frequency. New materials and processes for cathodes and current collectors were developed to obtain low resistivity interfaces, and low ESR and high-frequency-stability. The chapter also presents the leakage current characterization of tantalum pentoxide and the conduction mechanisms contributing to the same.

Chapter-4 presents the integration of tantalum-based high-density capacitors on silicon substrates. The high-density capacitors as thin-films are laminated onto silicon substrates followed by planarization, via-drilling, lithography and metallization. The characterization of tantalum pentoxide as a dielectric is presented in the next chapter.

Chapter-5 presents the fabrication and characterization of high-density capacitors using high surface area titanium metal electrodes, conformal high-K and thin-film dielectric of titania. The chemical structure and electrical properties of anodized titania are investigated for their application as conformal ultra-thin dielectrics on high-surface area titanium electrodes.

Chapter-6 concludes the dissertation and summarizes the key findings of the different chapters in the dissertation.

Chapter-2

LITERATURE REVIEW

This chapter begins with a description of power module packaging trends starting from power modules having discrete passives SMT mounted on top to power modules with embedded thin-film passives. The chapter then highlights the role of capacitors in a power module, followed by a review of the key capacitor technologies, which are classified into thin-film and discrete with a detailed review on tantalum-based capacitors. The electrical performance of the discrete tantalum capacitor is benchmarked with the other discrete commercial technologies. Furthermore, the chapter also discusses the emerging nano-capacitor technologies to improve the capacitance densities by using high surface-area anode and high-permittivity dielectrics.

2.1 Trends in Power Modules

Ever increasing functionalities in an ultra-miniaturized electronic system entail multiple operational voltage and power levels for different components such as logic and memory devices, display backlighting, disk drives among others. Multiple power convertors such as buck convertors, boost convertors, invertors, etc., are used to address these needs by transforming the central power supply voltage to the desired device voltage or power levels. These power convertors consist of active power management integrated circuit along with input decoupling capacitors, storage inductors and output filter capacitors (Fig-2.1).

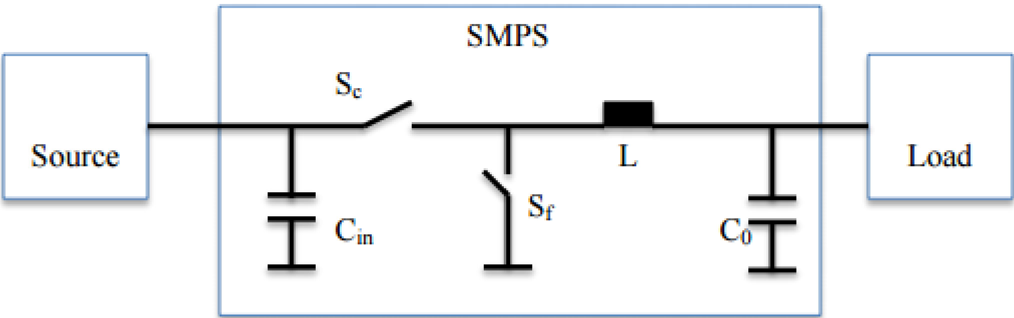


Figure 2.1: A simple schematic showing circuitry of buck convertor

2.1.1 Types of power modules

There are three types of power modules in production as shown in Fig- 2.2:

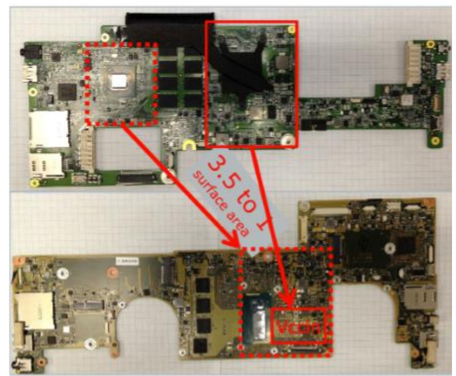
1) Power modules with discrete components that are SMT-assembled onto board (Fig-2.2a)

2) Package-integrated modules with embedded discrete passive components, (Fig-2.2b), and 3). Power modules with embedded thin-film passives (Fig-2.2c),

(a)

Figure 2.2: Three classes of power modules: (a) DC-DC convertors with surface-mount components (Ex. Texas Instruments) [18] (b) Power modules with embedded discrete passives (ex. Murata's µDc-Dc convertors with embedded ferrites) [19] (c) Power modules with embedded thin-film passives (ex. Intel Haswell processors) [20],

(b)



(c)

(Figure 2.2 continued)

Discrete power modules consist of wire-bonded dies on lead-frame packages and surface-mounted passive components separately packaged on a board (Fig-2.2a). The large interconnections due to wire bonds increases the overall size, system parasitics and real estate consumption. Other advanced interconnection technologies beyond wire-bond packages are explored to improve miniaturization and performance.

The second class of power modules involves chips, which are embedded within the package with surface mounted discrete passives. For example, the MicroSIP module by Texas Instruments[21, 22] (Fig-2.3) has an embedded die (~130 µm) in an organic core with surface mounted capacitors and inductors. These components are bulky with

thicknesses of several hundred microns. The packaging associated with these surface mounted passive components forces them to be placed far away from the active components, which add to parasitics from long interconnection lengths limiting their performance at high operating frequency.

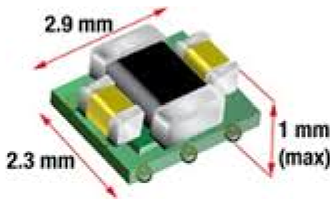


Figure 2.3: Texas Instruments MicroSIP module [22]

Another example is TDK's embedded multi-phase power module [23] (Fig-2.4), which has a power management IC embedded inside the substrate using TDK's Semiconductor Embedded in Substrate (SESUB) technology along with surface mounted discretes that lead to a module size of 11X11X1.6 mm^3. Other approaches use embedded discrete capacitors[24] with surface mounted chips on top of the capacitor. Such method allows for shorter interconnection yielding lower parasitics and higher operating frequencies, however, challenges abound in terms of reliability and cost.

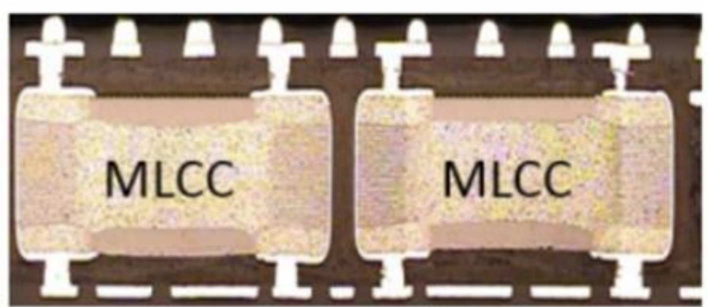


Figure 2.4: Embedded discrete capacitors [19]

The on-chip regulators mitigate the interconnection parasitic issues due to ultrashort distance to the loads compared to off-chip voltage regulators, thus, providing faster response and improved power delivery networks. However, they are limited to low voltage and current rating with degraded convertor efficiency, increased process complexity and die cost. An example of an on-chip regulator (Fig-2.5) is the embedded trench or metal-insulator-metal on a chip [25].

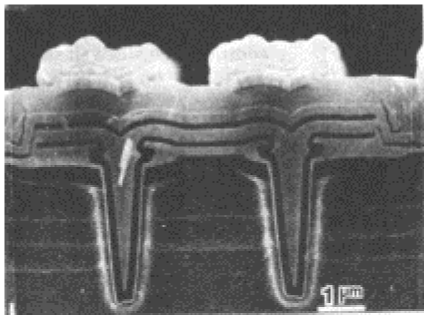


Figure 2.5: On-chip regulator with embedded capacitor [26]

Similarly, the fully-integrated-voltage-regulator by Intel with embedded thin-film inductors along with their Haswell processors (Fig-2.6) eliminates several external power management ICs, with MIM capacitor on die or trench capacitors [27, 28].

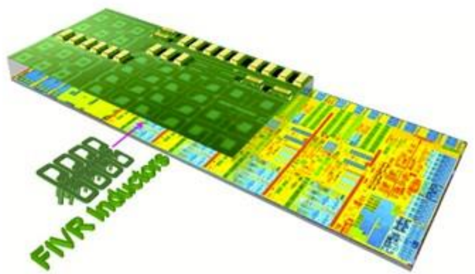


Figure 2.6: Embedded passives on an on-chip power convertor (Intel Haswell processor) [27]

Passive components such as inductors and capacitors are the critical energy storage components that determine the size and performance of voltage regulators. Today's functional modules utilize discrete passive components manufactured separately and are assembled onto the packages and boards and are typically 0.5 mm thick, resulting in module thicknesses of above 1 mm. Over the past 15 years, they have successfully migrated to thinner form-factors for some applications, yet face fundamental materials and manufacturing barriers in reaching thicknesses less than 300 microns. In spite of the advances in homogeneous or heterogeneous component integration as discrete component arrays or Integrated Passive Devices (IPDs), the limitations from component thickness still remain.

Passive components, which are still at milliscale in geometry and form-factors are therefore, a major impediment to miniaturization of power modules. The trend towards miniaturization of power module from discrete to partially integrated modules is shown in Fig-2.7.

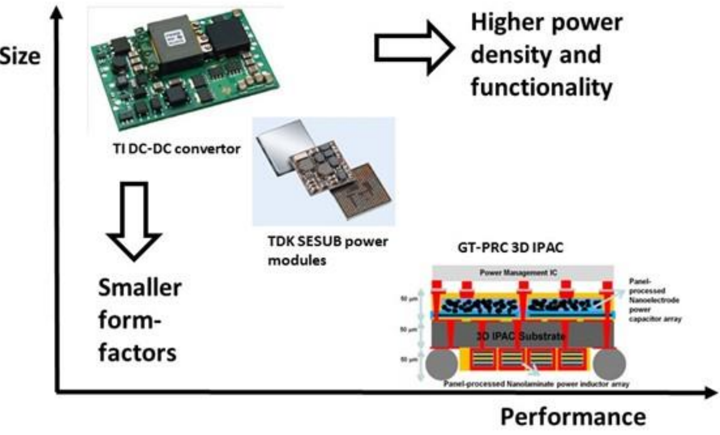


Figure 2.7: Trends towards miniaturized power modules

Georgia Tech Packaging Research Center (GT-PRC) envisioned an ultra-miniaturized miniaturized power convertor module with ultrathin capacitors and inductors with form-factors less than 50 μm. These next generation power convertors will have ultra-miniaturized passive components embedded inside ultra-miniaturized substrates and placed beneath the die enabling shorter interconnections, lesser parasitics with about 10X increase in power densities at higher operational frequencies. Hence, thin-film passive components with best properties and their integration into ultrathin substrates are required to meet the stringent needs for size and performance. The subsequent sections in this chapter will focus only on capacitors.

2.1.2 Role of capacitors in power supply

Capacitors are important for levelling out voltage fluctuations across signal ground planes. The voltage fluctuation can arise from current surge and current drop and the parasitic inductance caused by long interconnections according to the equation.

$$\Delta V = L\frac{dI}{dt}$$

Where ΔV = voltage fluctuation, L = parasitic inductance and dI/dt = rate of surge or drop in the current through the power ground lines. The fluctuation in voltages across the signal ground planes could lead to improper functioning of the chips such as erroneous switching of transistors in a high-frequency switching.

Capacitors maintain constant voltage supply by acting as charge reservoirs that supplies charge when there is a drop in voltage and absorbs charge when there is a voltage

surge. The subsequent sub-sections describe the different capacitor technologies used in electronics industry.

2.2 Capacitor Technologies

Capacitors used in the electronics industry generally fall into two categories (Fig-2.8) - thin-film layers using substrate-compatible processes and traditional discretes (surface mounted to board). They are described in detail in the subsequent sub-sections.

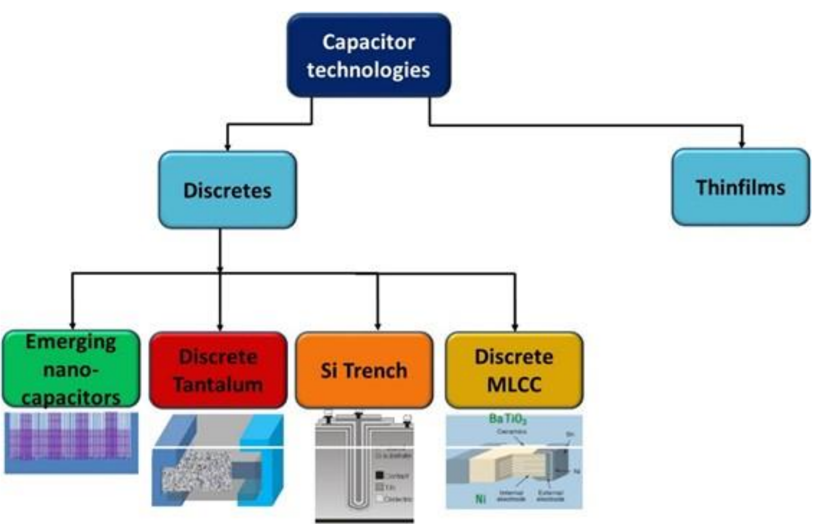


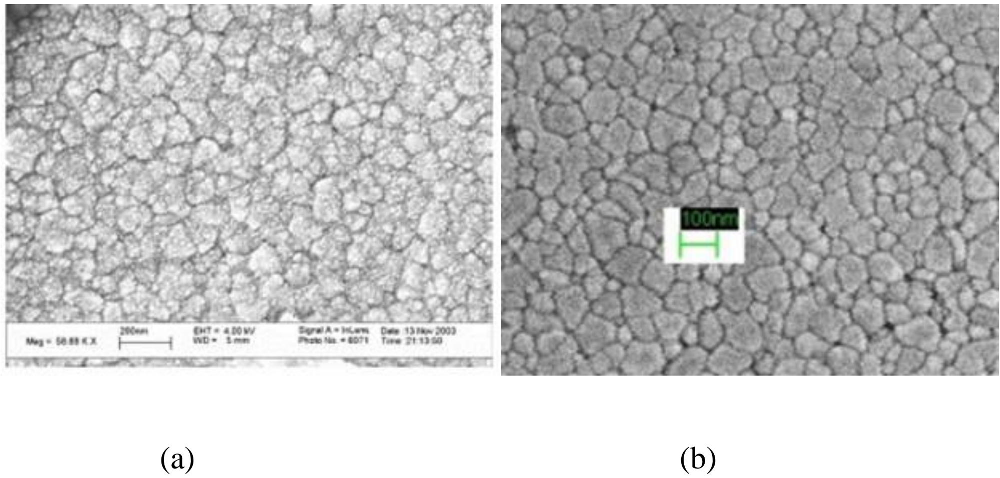
Figure 2.8: Classification of capacitor technologies

2.2.1 Thin-film capacitors

The first class of capacitors comprises high-permittivity dielectrics and nanostructured electrodes that are directly-deposited as thin-film layers, providing proximity to active devices, while resulting in simultaneous miniaturization. They are placed within 30-40

microns from the active devices, while the capacitors themselves may range from 1-50 microns in thickness [14]. These include high-permittivity dielectrics such as barium titanate and barium strontium titanate with silicon, glass or organic substrate-compatible processes both as ceramic thin-films and ceramic-polymer composites [19].

Perovskites thin-film capacitors based on barium titanate (BT), barium strontium titanate (BST) and lead-zirconium titanate (PZT) with permittivity of more than 1000 and dielectric thickness in the range of 100-1000 nm have been reported [29]. Different approaches were used to synthesize these films. Takano demonstrated sputtered BST based capacitor integrated on silicon yielding capacitance densities of ~2 $\mu F/cm^2$, leakage of less than nA/nF at 3V and TCC under 25% [30]. Other approaches used solution derived techniques for thin-film synthesis. High quality BT films (Fig-2.9a) were synthesized on free standing foils, which yielded dielectric constants of 900 [31]. Sol-gel derived thin-film PZT dielectrics (Fig-2.9b) along with conducting metal oxide electrodes (lanthanum nickel oxide) as the bottom electrode [32] were synthesized with capacitance densities of 2.2-4.3 $\mu F/cm^2$ with leakage properties in the range of 6.3-7.8 $\mu A/cm^2$. The type of bottom electrode was observed to have an effect on the capacitance density and leakage with different capacitance densities and leakage current observed for solution derived LNO and sputtered Pt as bottom electrode, which could be attributed to the roughness of electrodes, defects in sol-gel films and inter-diffusion between the electrode and the dielectric.



(a) (b)

Figure 2.9: (a) Hydrothermal BT films[31] (b) Sol-gel based PZT films [32]

In other high-temperature consumer and automotive applications, novel nano-dielectrics with high K, low loss, high temperature stability such as $Ca_2Nb_3O_{10}$ have been developed. These high-K dielectrics are used as two-dimensional (2D) oxide nanosheets derived from layered compounds as shown in Figure , with permittivity of 210 with ultra-thin (2 nm) perovskite dielectrics, yielded high capacitance densities at higher temperatures with very low TCC (Fig-2.10) indicating temperature stability [33].

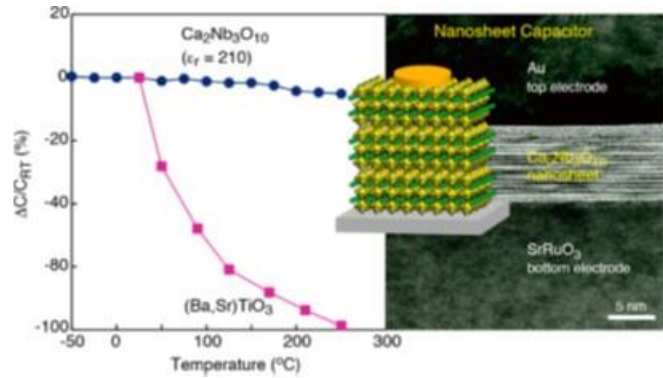


Figure 2.10: Temperature dependence of the capacitance change relative to RT value ($\Delta C/C_{RT}$) for $Ca_2Nb_3O_{10}$ nanosheet and perovskite thin films (left); High-resolution TEM image of an Au/$(Ca_2Nb_3O_{10})_n$/ $SrRuO_3$ nano-capacitor (right) [33]

However, these types of capacitors have other limitations. These include defects that form in the capacitor fabrication process, thus affecting not only the yield of the capacitor but also of the entire substrate. As a result, they tend to be expensive and are not scaled up to high-volume manufacturing. In addition, there is another challenge related to achieving very high capacitance density with substrate-compatible materials and processes.

2.2.2 Discrete Capacitor Technologies

Tantalum capacitors, Multilayered co-fired Ceramic Capacitors (MLCC), and Integrated Passive Devices (IPDs) fall under the second category. They provide high volumetric capacitance density at low cost, tested and ready for board-level assembly using standard Surface Mount Technologies (SMT). However, they are manufactured and assembled as thick components, limiting their use in emerging high-performance and miniaturized applications. MLCC, trench capacitors, porous electrode-based capacitors are well established to achieve high capacitance densities. Fig-2.11 compares high-surface-area architectures for different capacitor technologies.

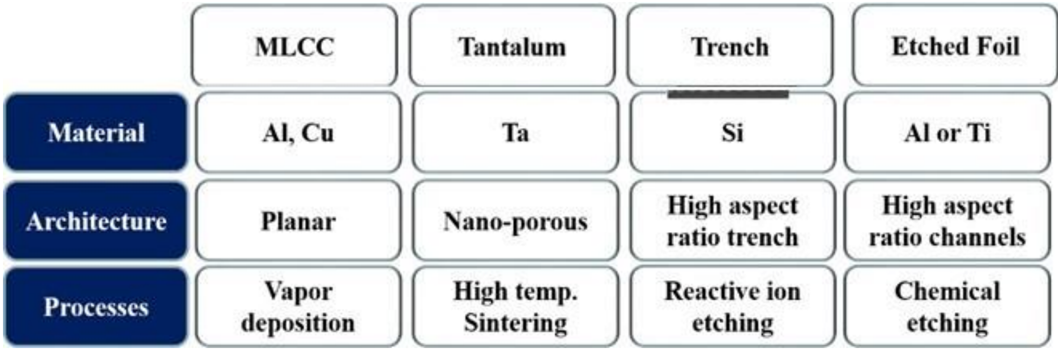
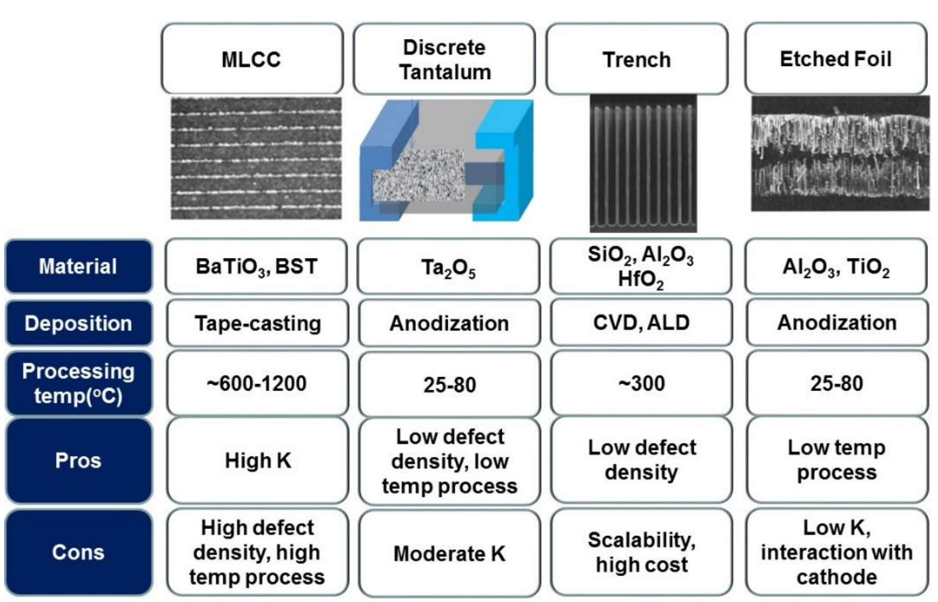


Figure 2.11: High surface-area anodes for capacitor technologies

Depositing conformal high-permittivity dielectrics over larger areas is critical to forming the capacitor and usually requires vapor deposition techniques such as CVD (Chemical Vapor Deposition) and ALD (Atomic Layer Deposition) [14, 34]. They are used in silicon trench capacitors as well as etched foil capacitors. These deposition techniques have their set of drawbacks which includes high cost, high deposition time and low throughput and non-conformality for complex porous architectures. They are also reported to yield higher defect densities due to non-uniformity and non-conformality of the grown film leading to higher leakage current. On the other hand, methods such as thermal oxidation or nitridation limit the dielectrics to lower permittivity values.



	MLCC	Discrete Tantalum	Trench	Etched Foil
Material	$BaTiO_3$, BST	Ta_2O_5	SiO_2, Al_2O_3 HfO_2	Al_2O_3, TiO_2
Deposition	Tape-casting	Anodization	CVD, ALD	Anodization
Processing temp(°C)	~600-1200	25-80	~300	25-80
Pros	High K	Low defect density, low temp process	Low defect density	Low temp process
Cons	High defect density, high temp process	Moderate K	Scalability, high cost	Low K, interaction with cathode

Figure 2.12: Dielectric systems

Some of the dielectric systems used for various capacitor technologies are shown in Fig-2.12. An alternative approach is to use thin-films of high K dielectrics such as barium titanate, barium strontium titanate and their derivatives. However, they lead to low

dielectric constant at high frequencies yielding low capacitance densities and high processing temperatures to form the required microstructure leading to substrate-incompatible processes. Anodization is used for valve metal-based electrodes due to their affinity for oxygen.

Accessibility of the high-surface-area architectures outlined earlier to the cathode is imperative to achieving high capacitance densities. ALD TiN has been widely used in trench capacitors [35, 36], however, the coverage limitations inside the trenches are the major roadblock. The other cathode options include manganese oxide [37, 38]; conducting polymers such as PEDOT:PSS [39], P3HT [40], PANI [41] and polypyrrole [42] are synthesized by a host of methods such as calcination of manganese salts, dispensing monomer solutions for in-situ polymerization, dispensing pre-polymerized suspensions [14], sol-gel [43], hydrothermal and other techniques [44]. The key attributes of the some of the various cathode options are listed (Table-2.1).

Table 2.1: Summary of materials used as cathode in high-density capacitors

	Organic	**Inorganic oxides**	**Inorganic nitrides**	**Metals**
Materials	PEDOT	MnO_2	TiN	Cu
Processes	Dipping, Dispensing	Dipping, Dispensing	ALD	PVD
Conductivity (S/cm)	400-600	10^{-6}-10^{3}	10^{4}-10^{5}	$6x10^{5}$
Processing temperature (°C)	~70-120	~280	~300	180-200
Self-healing	Yes	Yes	No	No
Applications in capacitors	Discrete Ta, Etched foils	Discrete Ta, Etched foils	Si trench	MLCCs

Each of the capacitor technology is described below.

2.2.2.1 Trench Capacitors:

Trench capacitors provide high capacitance density by virtue of their high aspect ratio surface-area trenches. Trench capacitors are typically made of silicon electrodes. Multilayered nano-dielectrics and counter electrodes are then sequentially deposited to form nano-capacitor structures. With this concept, a capacitance density of above 4 μF/mm^3 at 11-V breakdown was demonstrated using multiple-layer "ONO" (aluminum oxide-titanium nitride-aluminum oxide) stacks as shown in Fig-2.13. The limited trench aspect ratios pose a challenge in terms of achieving higher capacitance density. In addition, the use of expensive tools renders them non-scalable for high-volume manufacturing so as to end up with low cost [45].

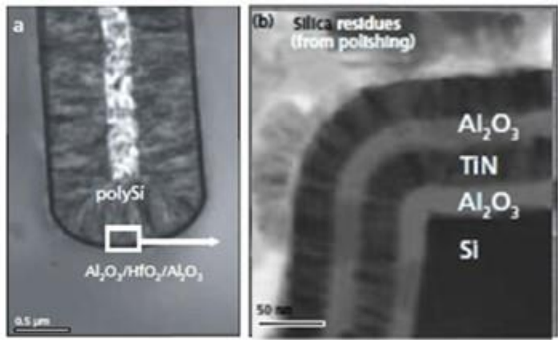


Figure 2.13: Silicon trench capacitors for DRAM applications [46]

2.2.2.2 Multilayered Ceramic Capacitors:

MLCCs provide high capacitances (Fig-2.12) by building stacks of metal and high-permittivity dielectrics. However, these ceramic capacitors require elevated processing temperatures leading to substrate-incompatibility and prohibit component miniaturizations. They can be mounted as die-side decoupling capacitors for low-frequency noise harmonics and are placed close to voltage regulator modules (VRMs) on the PCB while they can be mounted as land-side capacitors on the back of the package with the processor on the top and used at high frequencies (Fig-2.14).

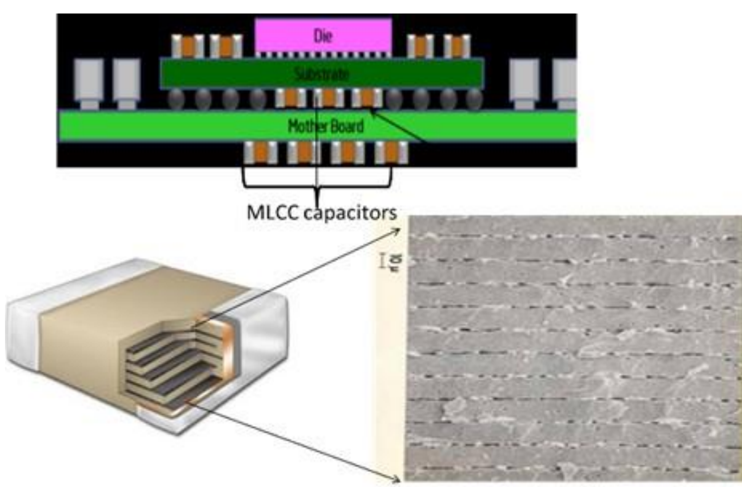


Figure 2.14: MLCC capacitors for high and low frequency applications

MLCC electrodes are migrating towards Ni-based electrodes from precious metals due to their lower cost and CTE mismatch with the dielectric, even though the oxygen migration from the dielectric towards metal cathode under electric field lowers the Schottky barrier and leads to higher leakage current and lower breakdown voltage. Miniaturization of MLCC capacitors entails thinner electrodes and dielectrics, which contribute to reliability

issues such as temperature and voltage stability. Issues related to the higher temperature coefficient of capacitance have been surmounted by using dopants such as Yttrium, Dysprosium and Mg in barium titanate [47, 48] which led to size reduction in MLCC based capacitors with commercial MLCC capacitors by Murata in form-factors of 50 µm, (Fig-2.15) and geometries of 0.25X0.125 mm^2. However, they yield 1pF – 10 pF and have a voltage rating of 6.3V.

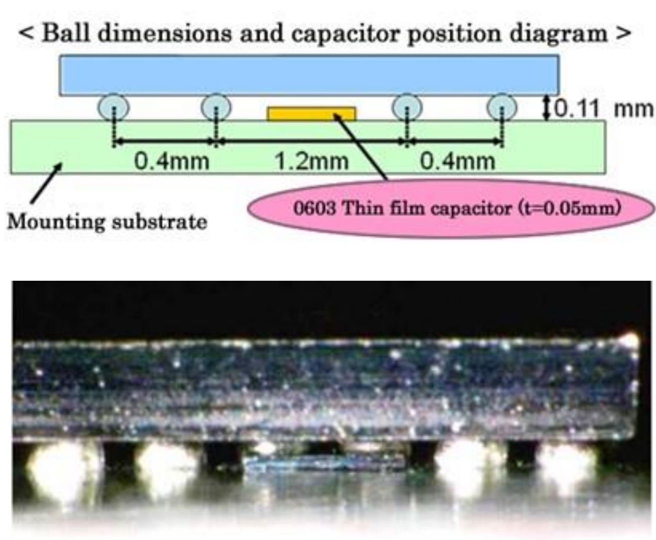


Figure 2.15:MLCC thin-film capacitor

2.2.2.3 Porous electrode-based capacitors:

Nanoparticle electrodes provide much higher surface-area compared to trench capacitors and are currently being developed to improve the capacitance density by a factor of 10 X at lower cost using scalable materials, tools and processes. The porous electrodes with partially-sintered nanoparticles provide ultrahigh surface-area per unit volume resulting in area enhancement of above 1000X for a 50 micron thick film. For example, tantalum high-

density capacitors (Fig-2.16) are pursued by industry for low-frequency power applications with high-surface-area generated through sintering of tantalum particles.

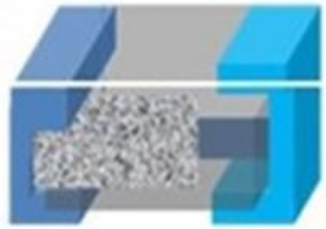


Figure 2.16: Tantalum capacitor [49]

Alternative high-surface-area electrode architectures have been and continue to be pursued to meet higher capacitance density requirements. Such high-surface-area electrode architectures include high-surface-area CNTs [50], sintered copper electrodes on silicon [51], etched aluminum electrodes [32] among others. These approaches face limitations in achieving high capacitance density due to the lower permittivity of the dielectrics such as silicon dioxide (~4) and alumina (~9). Aluminium [32] and titanium [14, 34] are some of the electrode systems that are commonly etched using electrochemical (wet-etching) or reactive plasma (dry-etching) processes, to yield high aspect ratio deep channels or trenches. They are also used for low-frequency applications.

Anodization is widely used in the electrolytic aluminum and tantalum industry to grow the dielectric due to high oxygen affinity for both. The consistency, conformality and thickness uniformity of the dielectric is monitored by the time, current, voltage and the concentration of the electrolyte. The liquid electrolyte is capable of reaching the narrow and deep channels in the metal, which oxidizes the metal on contact to form a dielectric oxide on the anode. The dielectric thickness increases with the anodizing voltage at a rate of

approximately 1-2 nm/V. It is known that out of all the available dielectric materials, oxides, nitrides, and oxynitrides have the highest breakdown voltages. This implies that these dielectric films can be easily thinned down to a few 10s of nanometers without compromising on their reliability. The rated, anodizing and the operating voltages are carefully designed to produce safe and reliable capacitors.

Anodization kinetics do not change when the anodization conditions such as anodization electrolyte and their concentration, anodization time and voltage and temperature stay the same. However, in a high surface-area electrode system such as sintered electrodes, the local field strength as well as the local ionic current density could lead to different dielectric thickness for oxides at different depths of the electrode [52]. Some of these anodized dielectrics such as titania and tantalum pentoxide have shown amorphous to crystalline phase transition yielding a crystalline metal oxide layer underneath (near/at the oxide/metal) at anodization bias as low as 5V (Fig-2.17). These crystalline regions manifest as non-stoichiometric oxides or metal oxides with the respective metal in lower oxidation states. With grain sizes, ca.1 nm, these porous crystalline phase heavily contributes to the leakage conduction in dielectrics such as titania [53-57].

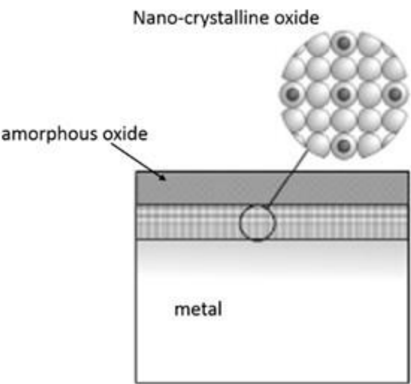


Figure 2.17: Oxide with amorphous and crystalline phases [55]

Electrical properties of Tantalum capacitors:

The electrical properties such as leakage current, ESR and yield are determined by the cathode materials. Manganese oxide (MnO_2) and conductive polymers such as PEDOT: PSS are the most widely used self-healing cathodes (described later) in the tantalum capacitor industry [58]. MnO_2 is formed by dipping the anodized high-surface-area electrodes into an aqueous manganese nitrate ($Mn(NO_3)_2$) solution, followed by thermal annealing. Multiple impregnations and annealing cycles are employed for conformal MnO_2 coating over the high surface-area architectures. Equivalent Series Resistance (ESR) in MnO_2 can be lowered by controlling the oxygen levels during the reaction to prevent the formation of resistive manganese oxide (Mn_2O_3). This leads to the formation of dense, smooth and uniform manganese dioxide layers with higher electrical conductivity. The introduction of oxidizing agents such as nitric acid, hydrogen peroxide, and ozone during the annealing of $Mn(NO_3)_2$ was explored for forming highly-conductive and conformal MnO_2 layer with lower ESR.

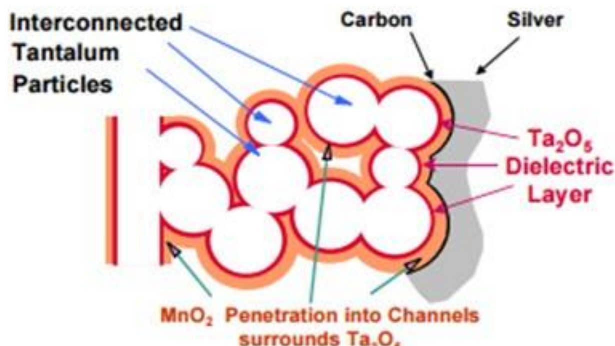
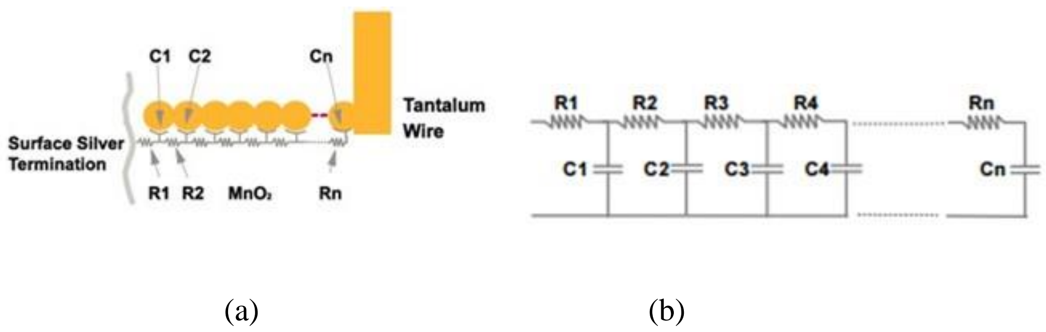


Figure 2.18: Construction of tantalum capacitor with MnO_2 as cathode [58]

With MnO_2 electrodes (Fig-2.18), the leakage current can be decreased but their lower conductivity (~10 S/cm) yields higher ESR (equivalent series resistance), which degrades the frequency stability of the capacitor. This is illustrated in Fig-2.19 with the performance of the tantalum capacitor like an RC ladder circuit.



(a) (b)

Figure 2.19: (a) Schematic of conduction path of MnO_2 in tantalum capacitor, (b) Construction of RC ladder representing tantalum capacitor [58]

The resistance offered by the MnO_2 increases as we move from the capacitor layers closest to the surface termination towards the layer near the tantalum wire due to larger conduction pathways. Capacitance, frequency and ESR are governed by the equation

$$\omega R_i C_i = 1$$

where w = angular operating frequency, R_i = resistance associated with MnO_2 conduction pathway from surface termination to the ith layer and C_i = capacitance contribution from the ith layer. Consequently, these layers are isolated from the external circuit at higher frequencies and they stop contributing to the overall capacitance leading to a frequency roll-off.

To address this challenge, alternative organic polymers such as thiophene-based PEDOT with higher conductivity[59], self-healing characteristics [58], higher conformality [60], better ESR [58] and ease of processibility are being actively used in tantalum capacitor industry. They form oligomers on in-situ polymerization and not big molecules; hence, they can easily penetrate into the high-surface-area architectures of the anodized anode. They show roll-off at much higher frequencies compared to MnO_2 due to their higher conductivity (~100-600 S/cm) and better coverage leading to lower electrode resistance and ESR as compared to MnO_2 based capacitors (Fig-2.20).

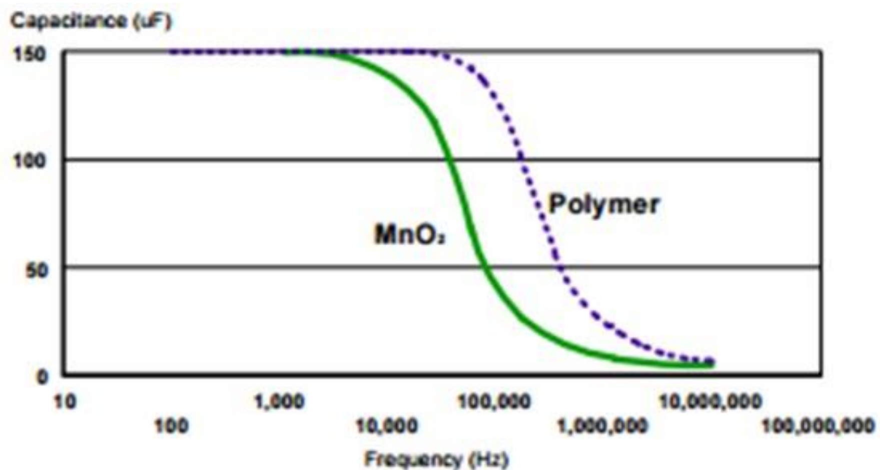
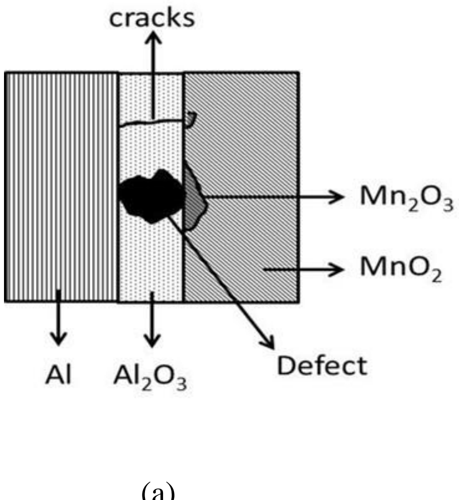


Figure 2.20: Plot showing the capacitance roll-off for MnO_2 vs conducting polymer as cathode in tantalum capacitor [58]

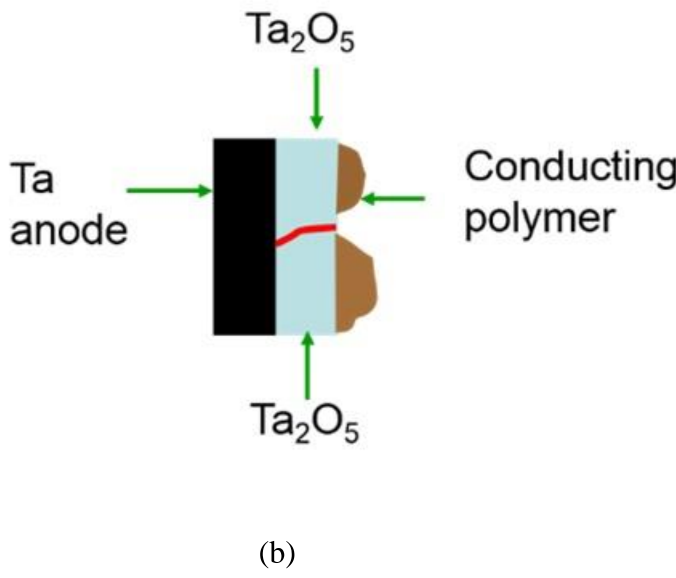
In-situ polymerized PEDOT: PSS generate iron based side-products, which degrade the dielectric yielding high leakage currents [44, 51]. Pre-polymerized PEDOT: PSS surmounts the shortcoming with no side products, however, the polymer infiltration and thick conformal coverage remain a major challenge that affects the cathode coverage [14]. Shortening the polymer chain length brings down the viscosity of the polymer suspension and assist the infiltration process. Pioneered by Hereaeus, the particular technology comes

as two different conducting polymer suspension with varying viscosities where the lower viscosity conducting polymer infiltrates the porous channels forming a conformal coverage while the high viscosity conducting polymer forms a thick coating on the surface of the anode and serves to provide good electrical contact with the current collectors and minimize any handling induced defects in the dielectric. Furthermore, cathodes such as MnO_2 and PEDOT: PSS exhibit self-healing behavior [58]. During self-healing, the presence of defects sites in the dielectric offers a low resistance path in the otherwise insulating dielectric leading to a current surge through the conducting polymer next to it. This causes the conducting polymer at those localized sites to evaporate, thereby, locally isolating the defects. The current surge accounts for the initially high normalized leakage current; as the self-healing takes place, the normalized leakage current comes down as the current encounters resistance while passing through the defect-free regions of the dielectric (Fig-2.21a and b).



(a)

Figure 2.21: Schematic of self-healing mechanism (a) with MnO_2 (b) with PEDOT:PSS



(b)

(Fig. 2.21 continued)

Poly(3-hexylthiophene-2,5-diyl) or P3HT is another potential candidate. The conductivity of P3HT is in the range of ~10^3 S/cm, which could be further enhanced by the addition of endometallo fullerene or Phenyl-C61-butyric acid methyl ester (PCBM). However, the self-healing capability of P3HT as a cathode is still a subject of investigation.

For comparison purpose, the three most widely used capacitor technologies (MLCC, silicon trench and porous electrode (tantalum and etched foils) are evaluated for their performance with respect to their electrical properties in Fig-2.22. Almost of them show similar capacitance densities and leakage current properties. Silicon trench show lesser capacitance density due to limited aspect ratio and smaller device thickness. Operating frequency is another major metric governing the high-density capacitor application. The inherent geometry of these capacitors, use of interface materials with electrodes such as silver paste and carbon black as current collectors coupled with their placement in a package adds to the parasitic inductance limiting their operating frequencies. Most of the

high surface-area capacitors by leading capacitor manufacturers such as AVX, Panasonic, Kemet, etc., operate in the frequency range of 100 HZ-100 KHz. The issue is described in detail in chapter-3.

Figure 2.22: Electrical performance of the commercial capacitor technologies

2.2.2.4 Emerging nano-capacitors:

The combination of AAO templates with ALD technology is another effective way to obtain highly controlled nano-capacitors. Such a capacitive structure is shown in Figure . Banerjee et al. [61, 62] demonstrated $TiN/Al_2O_3/TiN$ MIM nano-capacitors using this method with the densities on $100 \mu F/cm^2$. Further increase in the capacitance densities is achieved by employing high-k dielectric materials such as HfO_2 [63], Ta_2O_5 [64] and pervoksites [65].

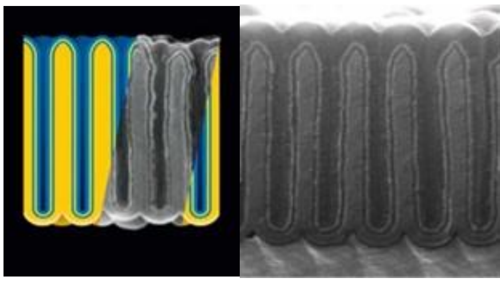


Figure 2.23: SEM image of cross-sectioned AAO-based electrostatic nano-capacitor with stacked TiN electrode and Al_2O_3 dielectric [62]

GT-PRC has recently demonstrated low-temperature sintering of base metals such as copper directly on silicon to form porous copper electrodes. Alumina is conformally deposited over the porous copper electrodes using ALD, followed by dispensing of conducting polymer as cathode [44, 51]. In the second approach, etched valve metal foils were evaluated as high surface-area electrodes, followed by anodization process for dielectric formation. The electrochemically-etched Al foils with high aspect ratio of above 50 were anodized to form conformal, thin aluminum oxide dielectric [32]. In both the approaches, PEDOT: PSS was used as the cathode material, which was conformally coated over the dielectric using solution-dispensing methods. High-surface-area nanoscale tantalum electrodes were also integrated onto silicon substrates as an alternative anode structure[66]. These advances have resulted in capacitance densities of 100 $\mu F/cm^2$ using silicon- or package-compatible processes. The approaches are schematically illustrated in Figure 2.24. The high-surface-area tantalum based approach along with high-surface-area titanium based capacitors will form the focus of this thesis and will be described in the subsequent chapters.

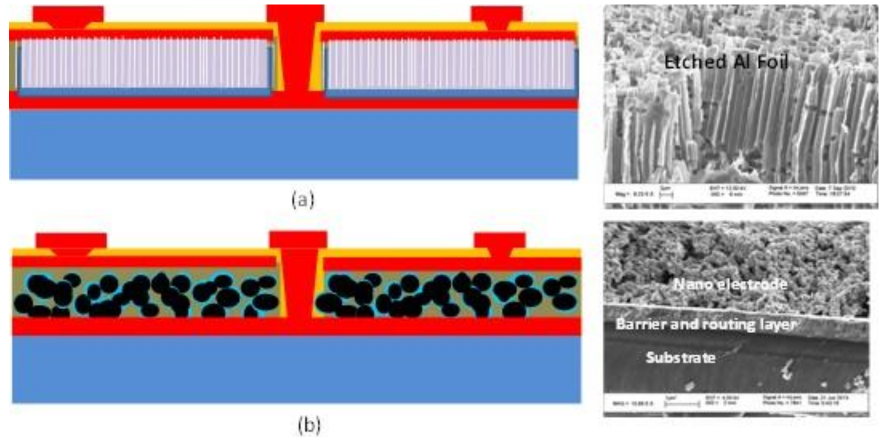


Figure 2.24: Two approaches for integrating high-density nano-capacitors: a.)Etch-foil, b.)Nanoparticle electrode [49].

2.3 Summary

The different types of power modules along with the trend to power module miniaturization are described in the first part of the chapter. The second part of the chapter described the different capacitor technologies.

Chapter-3

TANTALUM-BASED CAPACITOR – FABRICATION AND CHARACTERIZATION

Abstract

This chapter describes ultrathin tantalum-based high volumetric density power capacitors for 1-10 MHz frequency applications with low leakage properties. Dielectrics with low defect density were grown on high surface-area sintered tantalum anodes using self-limiting anodization process. The fundamental mechanisms that govern the film growth and quality are investigated to provide anodization process guidelines. Thiophene-based conducting polymers were used as the cathodes. Complete filling of conducting polymer was achieved by optimization of conducting polymer application process. EDS and structural SEM studies were performed to investigate the morphology and structure of the tantalum pentoxide films. The fabricated capacitor showed 0.1 μF/mm^2 of capacitance density in the 1-10 MHz range, which is 6X enhancement relative to the commercially available power capacitors. The leakage properties of the anodized porous tantalum are investigated with different leakage models used to identify the defect mechanisms in the tantalum pentoxide formed at different voltages.

3.1 Introduction

The trend towards miniaturized electronics with higher performance has stimulated interest in the development of affordable, compact, and highly-efficient capacitors. Tantalum [14, 34, 51, 66] and MLCC [1, 31, 49], trench capacitors [3] technologies are well-established to achieve high capacitance densities as shown in Chapter 2. Most of these aforementioned capacitor technologies come in large form-factors with low volumetric densities and are packaged as surface mount devices (SMDs) [12, 14-16] leading to large conduction pathways with lower operating frequencies. This research work focuses on developing high volumetric density miniaturized tantalum capacitors with stable capacitance at high operating frequency with low leakage currents.

Electrical properties such as volumetric capacitance density, operating frequency, ESR, etc., of a high density tantalum capacitors largely depends on the anode architecture, cathode conductivity and cathode coverage. A Panasonic SMD tantalum capacitor (Fig 3.1a-b) with cylindrical anode geometry, manganese dioxide as cathode and carbon and silver paste as current collector packaged inside a molded case with lead frame interconnections for anodes and cathodes yields ca. 220 µF of capacitance at 120 Hz for 3.5X2.8 mm^2 cross-section corresponding to ~22.4 $\mu F/mm^2$ of capacitance density. Packaging considerations swells the form-factor (capacitor thickness) to 1.9 mm that limits the volumetric capacitance density to 12 $\mu F/mm^3$. Processing them as printable tantalum anode scales down the geometry as well as the form-factor of the anode as the dimensions can be controlled by the stencil opening and the height. The surface area enhancement from

the anode could be controlled by controlling the size of the tantalum particles in the paste and sintering conditions yielding high surface-area anode architecture in a very small volume leading to higher volumetric capacitance density.

Operating frequency is another major metric governing the high-density capacitor applications. The tantalum electrode network, the inherent cylindrical geometry of commercially available Ta capacitors, use of interface materials with electrodes such as silver paste and carbon black [12, 15-16] as current collectors coupled with their placement in a lead-frame package adds to the parasitic inductance, limiting their operating frequencies. Most of the high surface-area capacitors by leading capacitor manufacturers such as AVX, Panasonic, Kemet, etc., operate in the frequency range of 100 HZ-100 KHz [14]. The use of a thin tantalum foil as a carrier and also the extended planar anode, as proposed in this thesis, would lower the conduction pathways between the tantalum particles and the bottom termination (tantalum carrier foil) would reduce the Equivalent Series Resistance (ESR) of the capacitor compared to conventional SMD tantalum capacitor where the conduction pathways between the sintered tantalum particles and the tantalum wire (bottom electrode termination) yields a higher ESR of the anode [16]. The use of silver paste and carbon black in commercial Ta capacitors preserves the insulation resistance of the tantalum pentoxide dielectric by eliminating any diffusion of the current collector metal (generally silver) through the cathode into the dielectric. Furthermore, silver paste and carbon-black based current collector adds to mechanical stability by improving the adhesion between the organic cathode and metallic collector and, therefore, eliminates reliability concerns. However, these current collectors are required in several

microns of thickness to be effective in preventing any silver diffusion to the dielectric that adds to the thickness of the capacitor by several microns. Moreover, the use of epoxy-based current collectors (Ag-paste) contributes to higher Equivalent Series Resistance (ESR) of the cathode due to limited electrical conductivity, thus, pushing back the operating frequency of the capacitor according to the following equation:

$\omega RC = 1$ --- (1)

Here, ω corresponds to the operating frequency, R denotes the ESR and C denote the capacitance. Direct metallization of thin tantalum capacitor using pure gold/copper metal can address this issue by reducing the resistance of the electrode, thus, pushing up the operating frequency of the capacitor. Moreover, direct metallization on the cathode using sputtering or evaporation leads to a much thinner current collector and yields a capacitor with thin form-factor. Thin metal layers along with the smaller geometries and thickness reduce the conduction pathways between tantalum particles and the current collector further reducing the ESR leading to higher operating frequencies (Fig-3.1c).

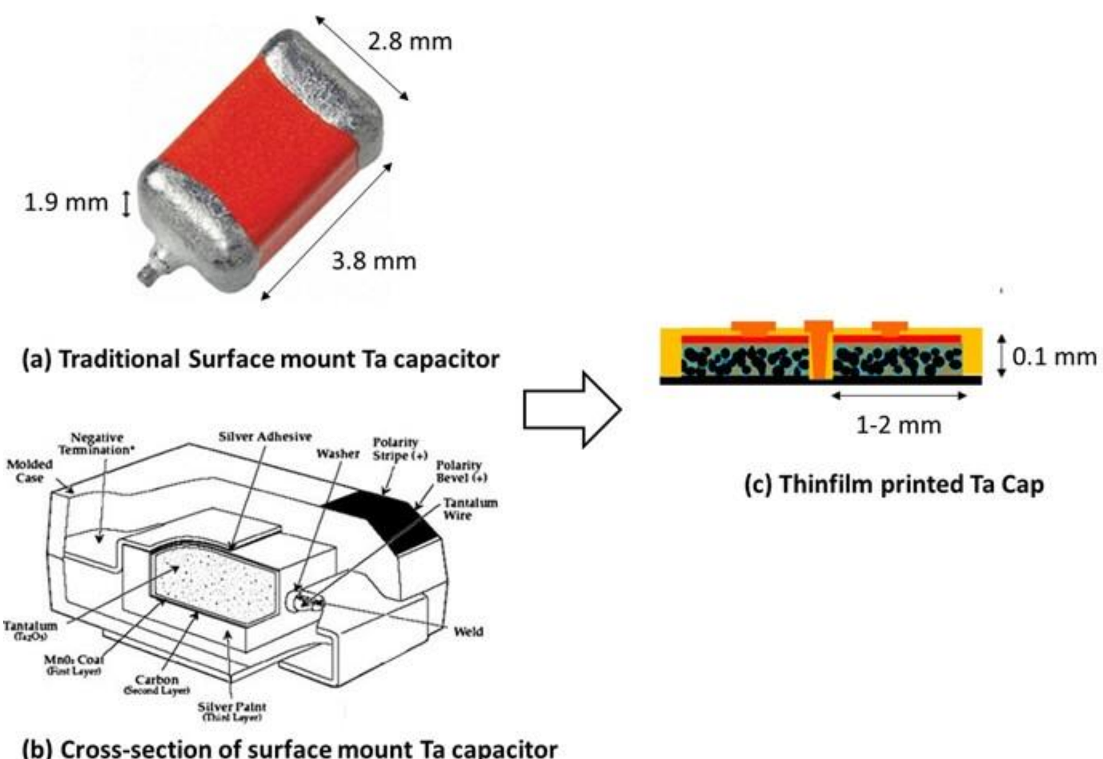


Figure 3.1: Schematic of high-density surface-mount Ta capacitor vs thin-film Ta capacitor developed in this work

In this work, we propose a high-density tantalum capacitor as thin-film to address the issue of low volumetric densities and operating frequencies. Processability of Ta particles in thin film form-factors, high-quality dielectric deposition and accessing larger Ta surface area to yield high capacitance densities remains the key focus of this chapter. Integration technology for thin-film Ta capacitors on several substrate platform such as glass, silicon or organics for high volumetric density was developed and is described in Chapter- 4.

3.2 Experimental

The proposed capacitor consists of Ta foil with an array of printed and sintered tantalum particles. Tantalum pentoxide grown on the porous Ta surface through the process of electrochemical oxidation of tantalum forms the conformal dielectric. PEDOT:PSS was used as the cathode with Au as the current collector. Further details are described in the subsections below and the cross-sectional illustration is shown in Fig-3.2.

Figure 3.2: Cross-sectional illustration of fabricated thin film Ta capacitor

High surface area porous tantalum electrodes were fabricated by printing and sintering the tantalum particles (0.2-0.6 µm) on 50 µm Ta foil. The printable paste consisted of tantalum metal loadings of up to 81% suspended in 1,2- propane diol and polymer. The printed thin-film paste was annealed in stages – at 100°C and 400°C (process flow schematic in Fig-3.3a) as part of a de-bindering process to remove the organic solvent and binders followed by sintering at a temperature of 1200°C. The sintered Ta pads had 2x2.6 mm^2 dimension with 50µm thickness. Tantalum particles of four different grades were used – 200 KCV, 80 KCV, 60 KCV and 30 KCV. Further details about these anodes are described in the results and discussion section.

The dielectric was grown on high surface tantalum anode by the process of anodization at room temperature using 0.1 M phosphoric acid chemistry. Dielectric films were grown on 80 KCV porous anodes using three different anodization voltages – 8V, 20V, and 40V respectively [5-8]. The anodization bias was applied in two steps with ramp of 0.01V/2s up to the destination voltage followed by dwell (Fig-3.3b) at the desired voltage till the anodization current dropped to 20 μA. The phosphoric acid assisted tantalum anodization exhibits a bilayer structure and follows a point defect model, which is further delved upon in the results and discussions section.

Pre-polymerized conducting polymer, PEDOT:PSS suspension, with low viscosity, high conductivity and self-healing characteristics was used as cathode. The anodized porous anodes were dipped in diluted and concentrated aqueous polymer suspension several times to facilitate impregnation of polymer (Fig-3.3c). The samples were dipped in conducting polymer with different dilutions at dipping rate of 1 mm/s using a robotic arm to ensure no air was trapped as a bubble. Each dip was followed by annealing to cure the conducting polymer and eliminate the solvent. It was seen that the number of dips, dwell time inside the conducting polymer suspension and the duration of annealing affected the extent of infiltration.

The cured conducting polymer layer was capped with a current collector to bring down the contact resistance during probing. Au/Cu/Au stack was evaporated as current collector on top of the conducting polymer infiltrated structure. Thin Au layer (~50 nm) was used to

prevent copper diffusion into conducting polymer at the conducting polymer-metal interface.

Hitachi SU8230 SEM microscope was used for the morphological analysis. 4294A precision impedance analyzer and 42941A impedance probe were used for capacitance measurements. Keithley 6485 picoammeter was used for the leakage current analysis.

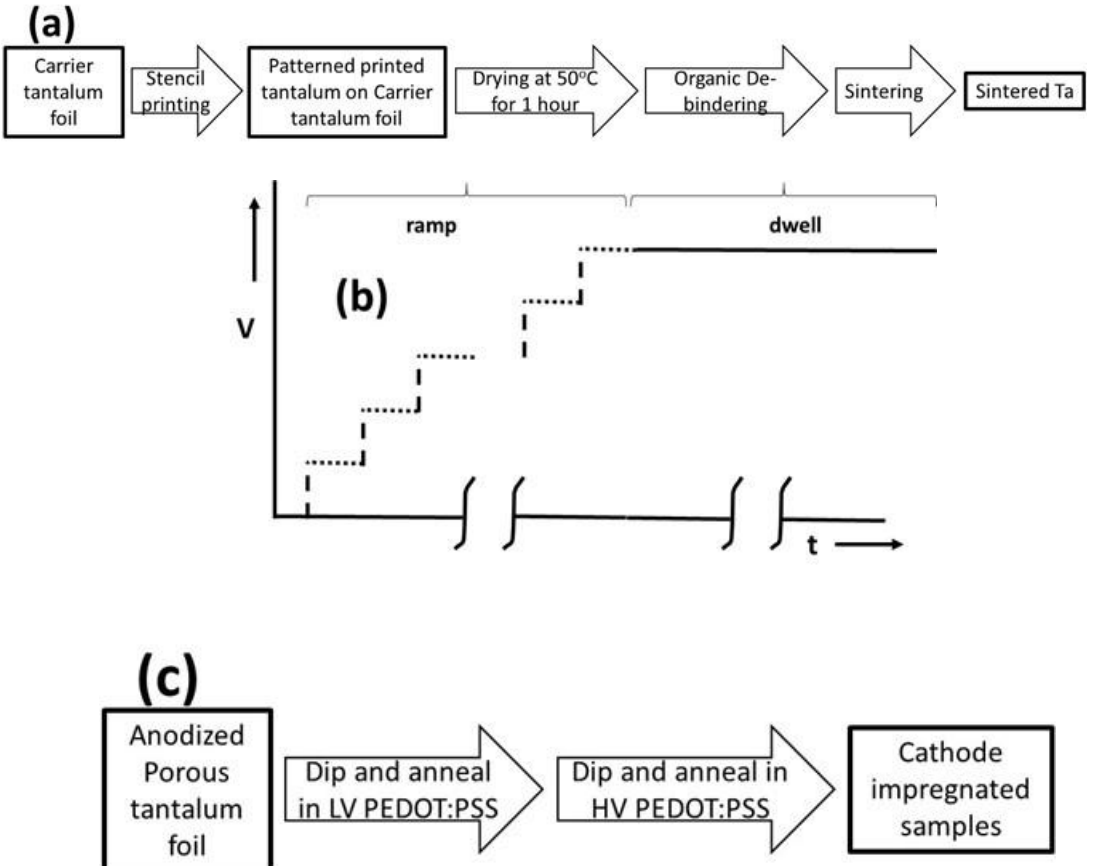


Figure 3.3: a. Flowchart of tantalum particle sintering; b. Bias application schematic for ramp and dwell; c. Flowchart of cathode infiltration

3.3 Results and Discussions

The samples were characterized for their surface area, cathode infiltration, and capacitance density as a function of frequency and leakage mechanisms and are described in the subsequent sub-sections.

3.3.1 Morphological Characterization and surface area estimation of high surface area anode

Fig.3.4 shows the SEM micrographs for the four different particle grades as mentioned before. The particle size and the pore size distribution of the particle grades is also listed in Table- 3.1. The 200 KCV particle grade were imaged to show particle sizes ranging from 110 nm – 160 nm (Fig. 3.4a), while, 80 KCV (Fig. 3.4b) corresponds to particle sizes in the range of 180-250 nm. The 60 KCV (Fig. 3.4c) had bigger particles ranging from 290-400 nm, while, the 30 KCV showed particle sizes in the range of 500-800 nm (Fig.3.4d). The surface area of the different particle grades was estimated from the micrographs using the stereological estimation. Three test lines were drawn on each micrograph and the line length was normalized by the magnification of the image acquisition. The number of intersections of the test lines was counted and the ratio of twice the total number of intersections and the total normalized test length provides the surface area per unit volume of the structure. As expected 200 KCV particle grade provided the highest surface per unit volume as well as the highest surface area enhancement (obtained from the ratio of SA/vol of the porous sample and SA/vol of planar sample with similar dimensions of the porous anode) due to smaller particle size, whereas, the 30 KCV registered the lowest surface area per unit volume and the lowest surface area enhancement due to the larger particle size.

The ‘C’ and ‘V’ in the ‘KCV’ stands for capacitance and voltage. Hence, at 1V, the 200KCV particle grade corresponds to powder with capacitance of 200KμF/g at 1V, while, 80 KCV, 60 KCV, and 30 KCV corresponds to powder grade yielding 80 KμF/g, 60 KμF/g and 30 KμF/g respectively. The high gravimetric capacitance density for the 200 KCV particle grade could be attributed to the larger surface area derived from smaller particle size. Similarly, the 30 KCV particle grade yielded smallest surface area due to bigger particle sizes and lower gravimetric capacitance densities.

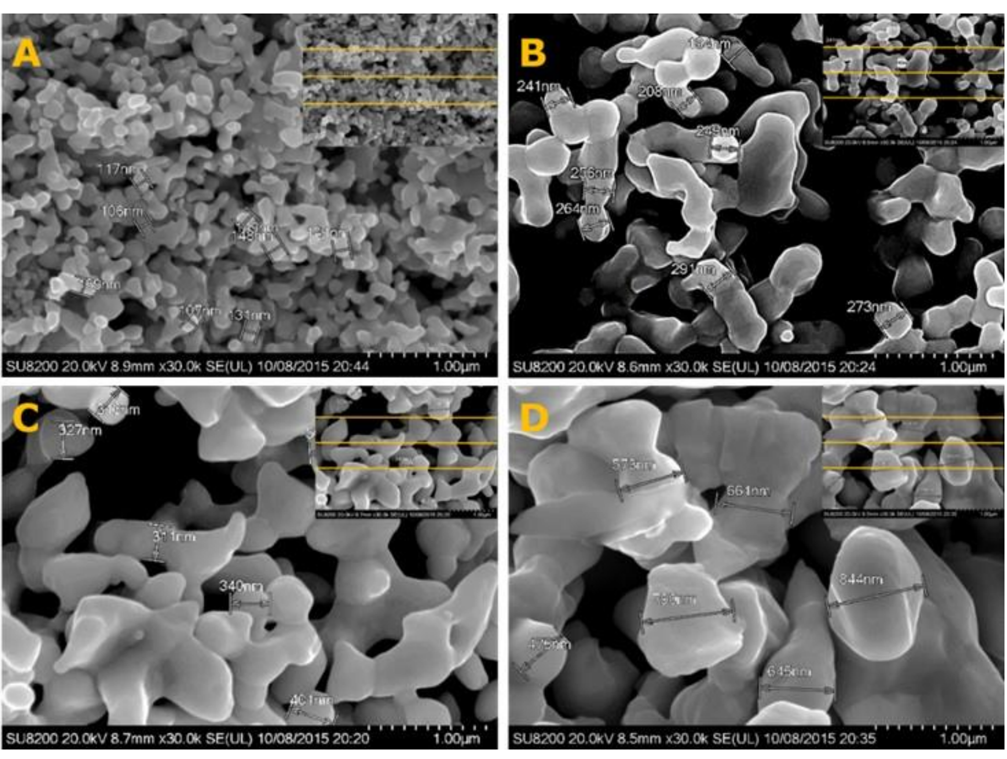


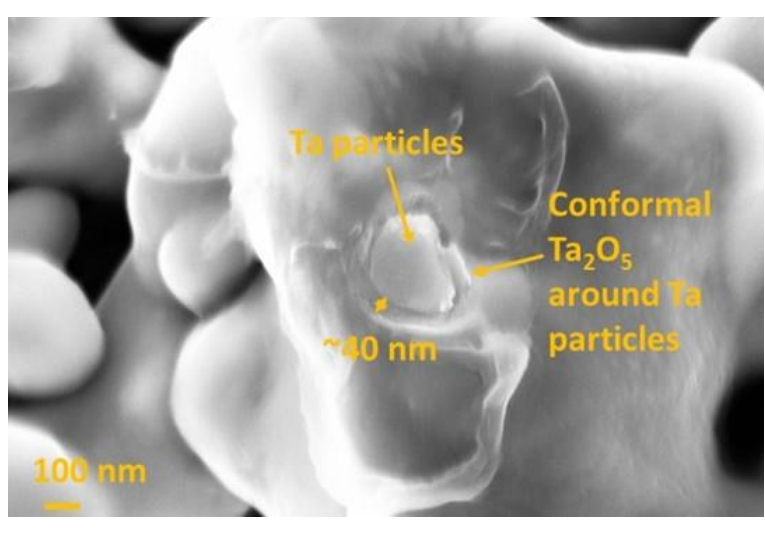
Figure 3.4. SEM micrographs of sintered tantalum anodes with different grades; a) 200 KCV; b) 80 KCV; c) 60 KCV; d) 30 KCV; The inset in each figure shows the micrograph with test lines intersecting the microstructure; used for stereological estimation of surface area.

Table-3.1. Surface area estimation of different particle size using stereological grain counting

Particle size distribution (nm)	Pore size distribution (nm)	Total intersections of test lines with grains	Total normalized length of test lines (cm)	Surface area per unit volume (cm^2/cm^3) of the porous sample	Surface area per unit volume (cm^2/cm^3) of planar sample with similar dimension	Surface area enhancement (X)
110-160	200-500	110	0.00084	261904.8	417.7	627.0
180-250	500-1000	49	0.00084	116666.70	417.7	279.3
290-400	500-2000	31	0.00084	73809.52	417.7	176.7
500-850	500-4000	20	0.00084	47619.05	417.7	114.0

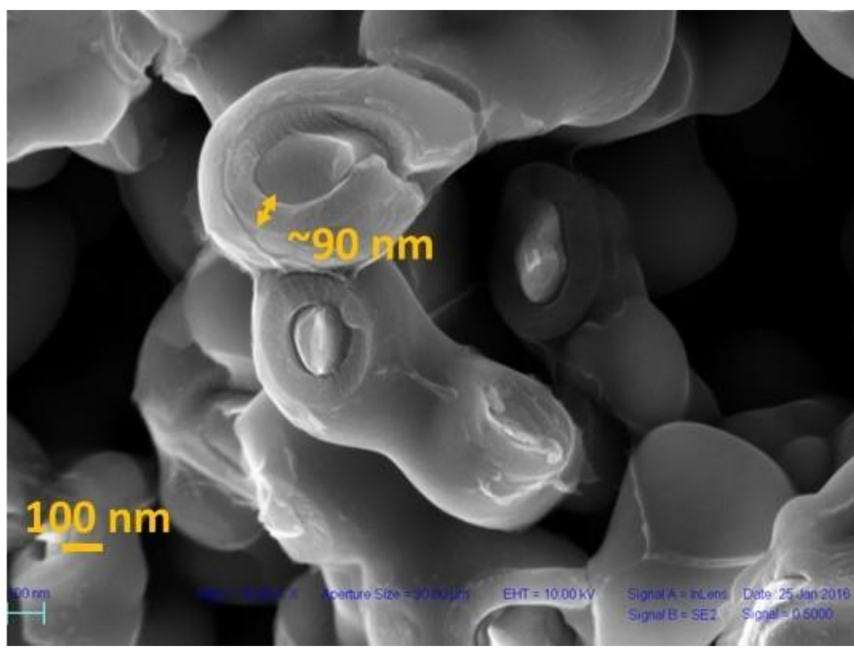
3.3.2 Anodization Characteristics

Three different anodization voltage (8V, 20V, and 40V) were chosen to optimize the leakage current properties. Anode particles with 300 nm particle sizes were used for this purpose. The SEM micrographs of the samples anodized with 20 and 40 V are shown in Fig-3.5. They correspond to a dielectric thickness of ~40nm and ~90 nm respectively, which is consistent with the values reported in the literature [67].



(a)

Figure 3.5: SEM Micrograph for (a) 20 V anodized dielectric (b) 40 V anodized dielectric



(b)

(Figure 3.5 continued)

Anodization proceeds through potentiodynamic mode [14] during ramp process (Fig. 3.6a). The plots for all the three dielectric thicknesses show similar trends. At 1.5 V, the energy supplied by the potential difference surmounts the activation barrier for ionic diffusion through the oxide diffusion layer, which accounts for the rise in anodization current [68]. Thereafter, the self-limiting nature of the anodization [69] leads to stabilized current for the remaining duration of anodization [68]. The eventual drop in anodization current (Fig. 3.6b) can be explained on the basis of point defect model [70], which forms the basis for tantalum anodization using phosphoric acid chemistry where the oxide growth proceeds at two interfaces – metal/oxide and oxide/electrolyte (Fig 3.6c).

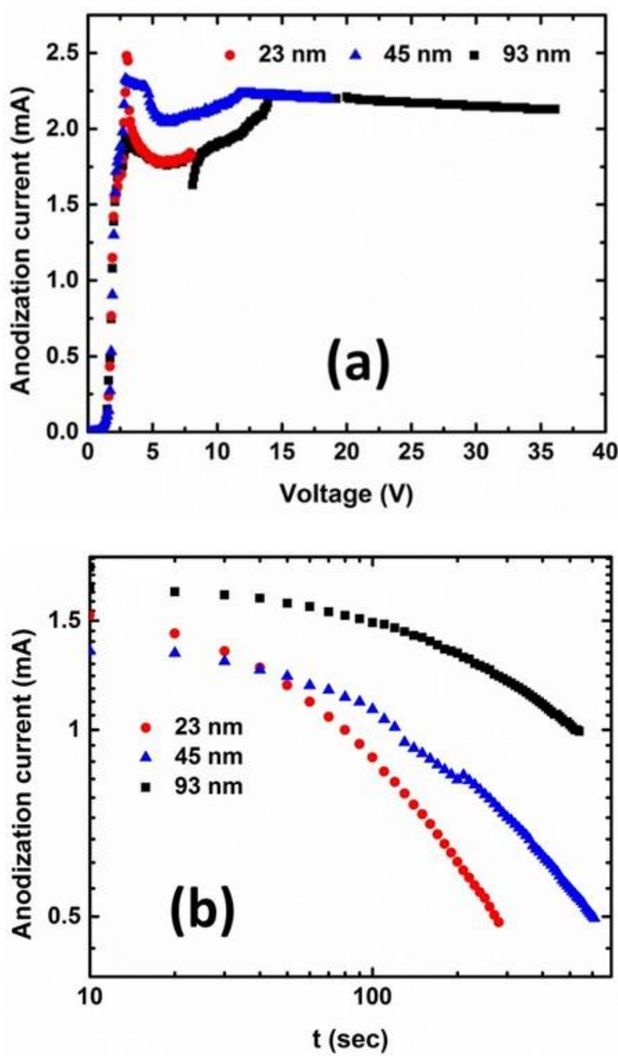
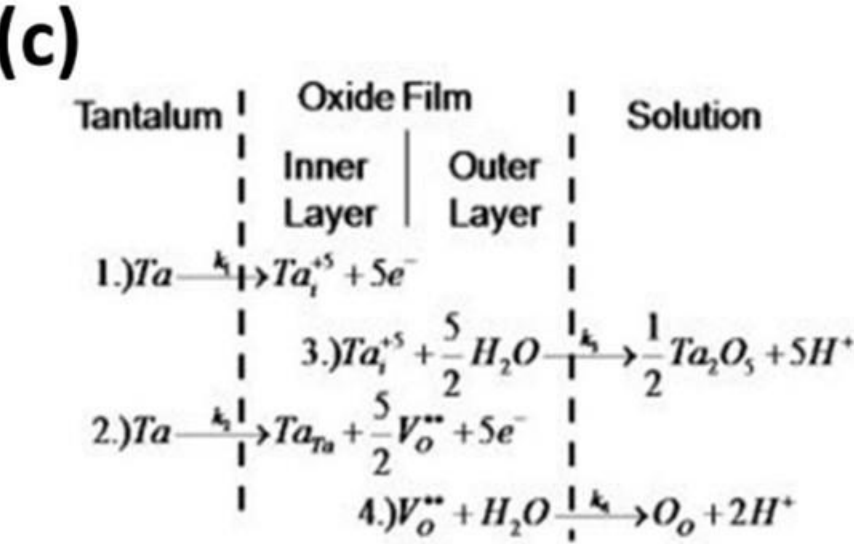


Figure 3.6. (a) Anodization current as a function of voltage during ramp; (b) Anodization current as a function of time during dwell; (c) Point defect model for Ta anodization



(Figure 3.6 continued [71])

The oxide growth is accompanied by point defect generation at the metal/oxide interface and annihilation reactions at the two interfaces. Inner oxide layer forms through the generation of oxygen vacancies at metal/oxide interface followed by their hydrolysis, while, the outer layer forms through the formation of tantalum interstitials at the metal/oxide interface followed by their outward migration and hydrolysis to yield tantalum pentoxide [72]. Outer oxide layer also incorporates some of the phosphate groups from the electrolyte solution in the anodization bath that enhances the quality of the dielectric layer [73].

The potential drop at the two oxide interfaces are governed by the equations (2-3) [70]

$$\Theta_{o/el} = \Theta_o - \Theta_{el} = \alpha V + \beta pH + \Theta^o{}_{o/el} \text{-----------------(2)}$$

$$\Theta_{m/o} = \Theta_m - \Theta_o = (1-\alpha)V + \beta pH + \Theta^o{}_{o/el} - EL \text{-----(3)}$$

Where $\alpha = d\Theta_{o/el}/dV$ is defined as the polarizability at the oxide/electrolyte interface, $\beta = d\Theta_{o/el}/dpH$ is the pH dependence of the potential drop at the oxide/electrolyte interface, E = Electric field and L = oxide thickness. The rate of oxide film formation slows down at large enough oxide thickness (L) due to a drop in the rate of point defects generation caused by a reduced potential $\Theta_{o/el}$ (equation-3) and the oxide exists in a quasi-steady state. The quasi-steady state accounts for the logarithmic drop in the anodization current-anodization voltage plot. Consequently, point defects generation is assumed to be the rate determining step in anodization [71].

3.3.3 Wetting Properties of Cathode on Dielectric

Wettability of the tantalum pentoxide by the conducting polymer (PEDOT: PSS) play an important role in driving the polymer inside the porous architecture and finally the electrical properties of the capacitor. The wetting properties of the aqueous based PEDOT: PSS was studied by investigating the contact angle of the tantalum pentoxide dielectric grown on planar and porous tantalum. The viscosity of the as-received low viscosity PEDOT: PSS was similar to that of water (0.89 mPa.s). The PEDOT: PSS exhibited a wetting angle of 70° on planar tantalum pentoxide and 25° on porous Ta surface (Fig-3.7a). However, better wetting properties of the conducting polymer in the case of a porous system could be ascribed to higher surface energy of porous surfaces between air and oxide surface (γ_{SA}). Higher surface energies yield higher cosine of contact angle (ψ) given by the equation (4), which amounts to a lower contact angle. (γ_{SL}) and (γ_{LA}) correspond to surface

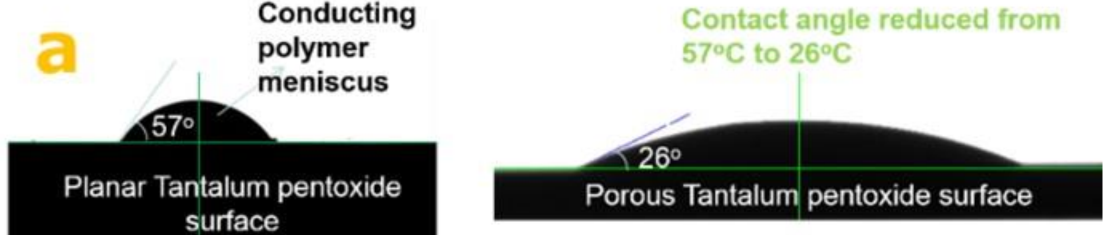
energy between the oxide and conducting polymer and between air and conducting polymer.

$$\cos\psi = \frac{\gamma_{SA} - \gamma_{SL}}{\gamma_{LA}} \quad \text{---------------------------------------} \ (4)$$

3.3.4 Cathode Infiltration inside Porous Structure

Fig. 3.7b shows the SEM micrograph of 60 KCV particle grade impregnated with conducting polymer not showing any infiltration beyond the first 10-12 µm. This was corroborated using Energy Dispersive Spectroscopy. Compositional analysis of the cross-section of the capacitor (not shown here) revealed non-uniform distribution of conducting polymer at different depths; strongest conducting polymer signals, characterized by % weight Sulfur were observed from the capacitor surface (5-10% at depths of 0-8 µm) followed by a marked drop in those signal strength (<0.2 %) beyond 8 µm. It is important to note that S that remains as a part of polymer backbone has a lower wt% in a polymer chain, thereby reducing the overall sulfur signals. Thin film geometry of the anode and the presence of Ta carrier underneath the porous Ta limits cathode infiltration inside the porous anodes from one side accounting for poor cathode infiltration. Impregnation was improved in this work by using 30 KCV grade (Fig. 3.7c) with particle size of ca. 500-850 nm with pore size distribution of 1 µm – 4 µm. Larger pores allowed better infiltration all through the 50 µm thick porous architecture. This is also corroborated by the EDS line-scan across the cross-section of the sample as shown in Fig-3.7d. Sulfur accounted for nearly 10% of the overall signals in the first five microns, which were dominated by the signals of carbon coming from conducting polymer, and is present throughout the cross-section as seen in

the EDX line-scan (Fig-3.7d), which suggest the presence of conducting polymer throughout the cross-section of the porous architecture. Tantalum dominated the EDX signals in the intermediate depths and near the bottom of the porous anode, which suggests the pores may not have been filled that is important for lowering the ESR. Hence, further processing is required to fill the conducting polymer in the nano-pores, instead of conformally coating the Ta_2O_5, as seen in Fig. 3.7c. Multiple dipping and subsequent drying steps facilitated better impregnation of conducting polymer in nano-channels. This was done by increasing the number of dips and the duration of dwell. The SEM micrographs of the improved infiltration are shown in Fig-3.8 along with the EDX line-scans (fig-3.9) across the cross-section of the sample (EDX spectra at the top and bottom of the conducting polymer infiltrated porous structure). Fig-3.8a shows the filling of pores near the bottom of the porous structure by the conducting polymer. Fig-3.8b is a magnified view of the region shown in Fig-3.8a. The line scan for such a scan shows the presence of sulfur and carbon through the sample cross-section (Fig-3.9a and b). This is a marked improvement in the context of pore filling with carbon signals dominating the EDS signals till 20 µm from the surface of the sample, while, the sulfur content is nearly 7-15% (3.9c and d) till the first 15 µm indicating thorough filling of the pores with conducting polymer. Cathode infiltration inside the thin-film anode could be further bolstered using a vacuum suction. Infiltration process would be assisted by drilling through vias through the Ta carrier foil with the aim of introducing larger vacuum gradient in the pores by means of a suction underneath the thin-films that will pull the conducting polymer inside the pores further in. However, this is beyond the scope of this research work.



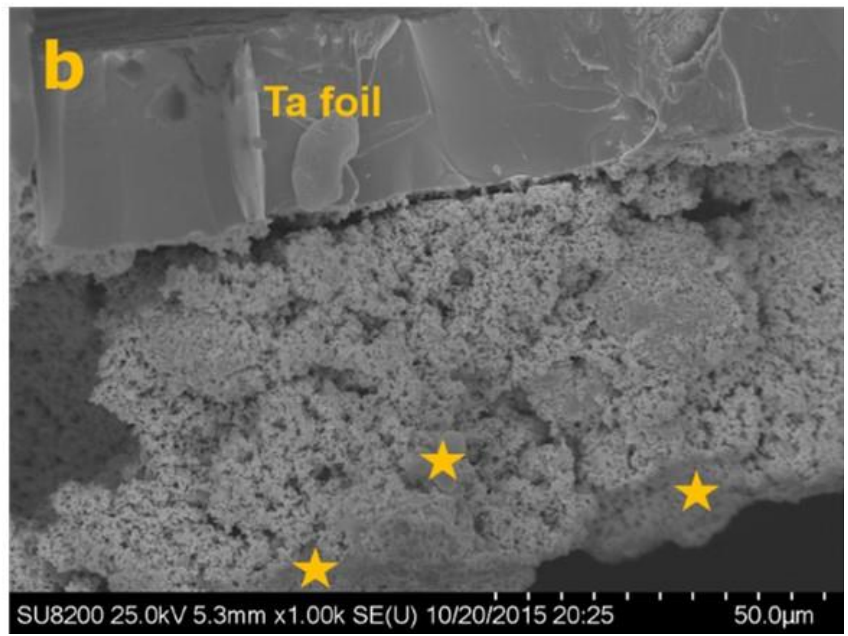
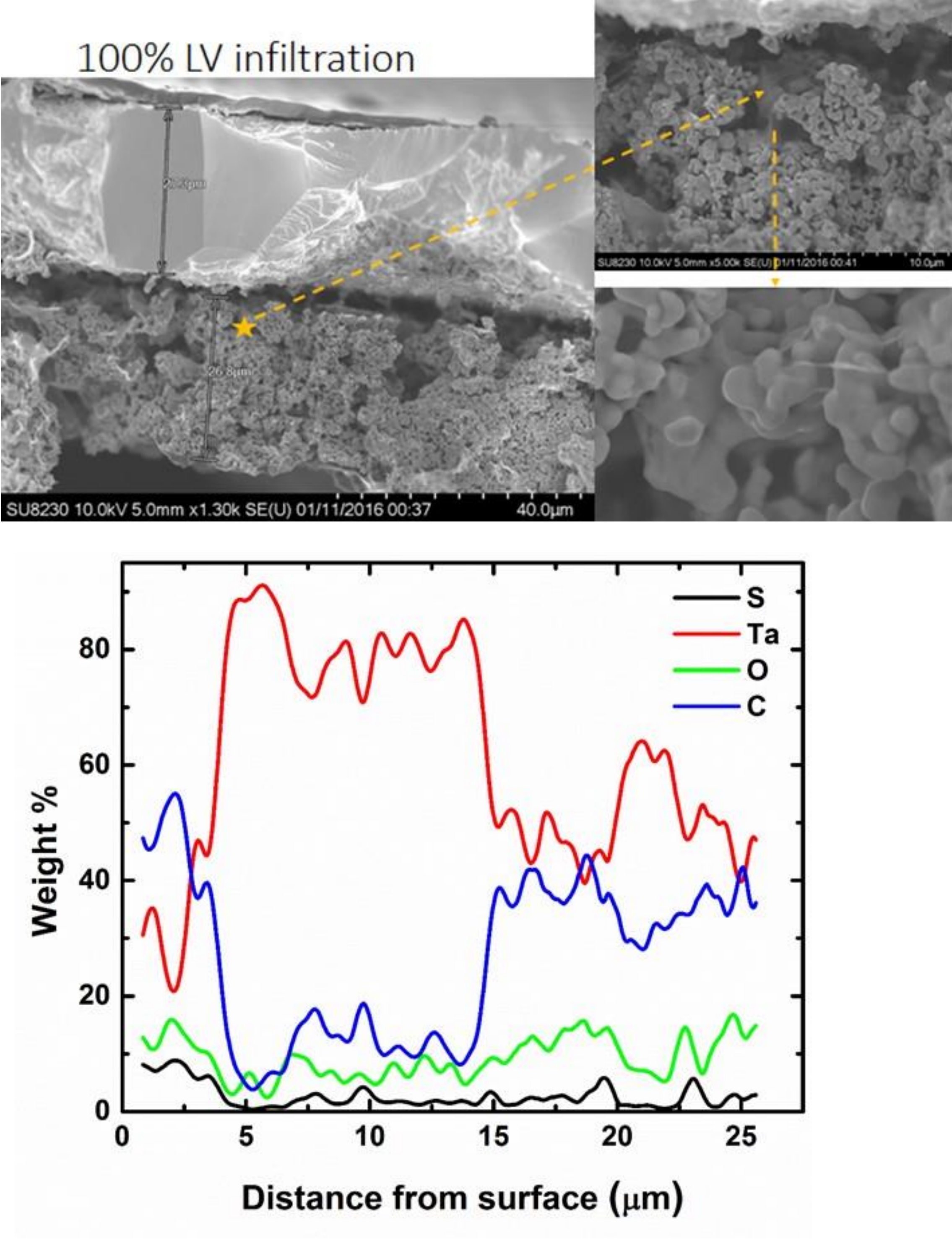
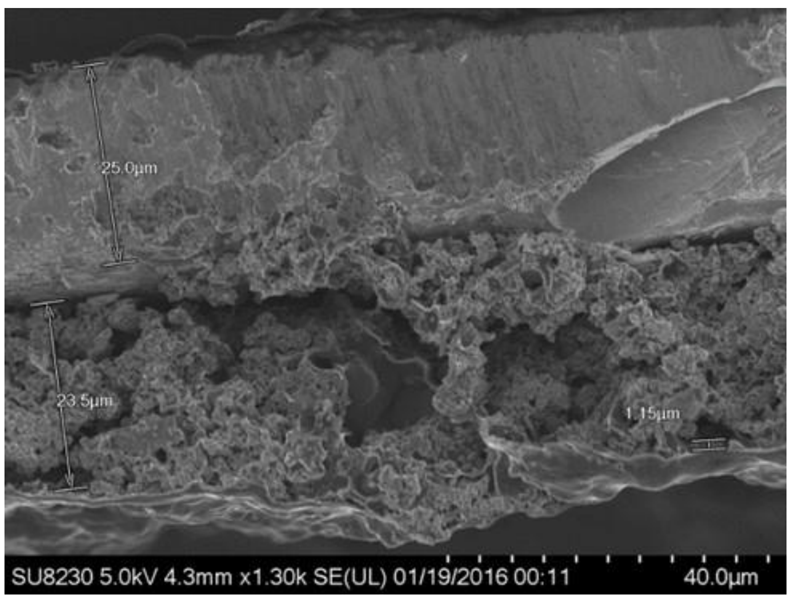


Figure 3.7. (a) Wetting properties of conducting polymer on planar and porous tantalum pentoxide surface; SEM micrograph showing conducting polymer infiltration through (b) 60 KCV particle grade (c) 30 KCV particle grade (d) conducting polymer infiltration at different depths along the anodized anode



(Figure 3.7 continued)



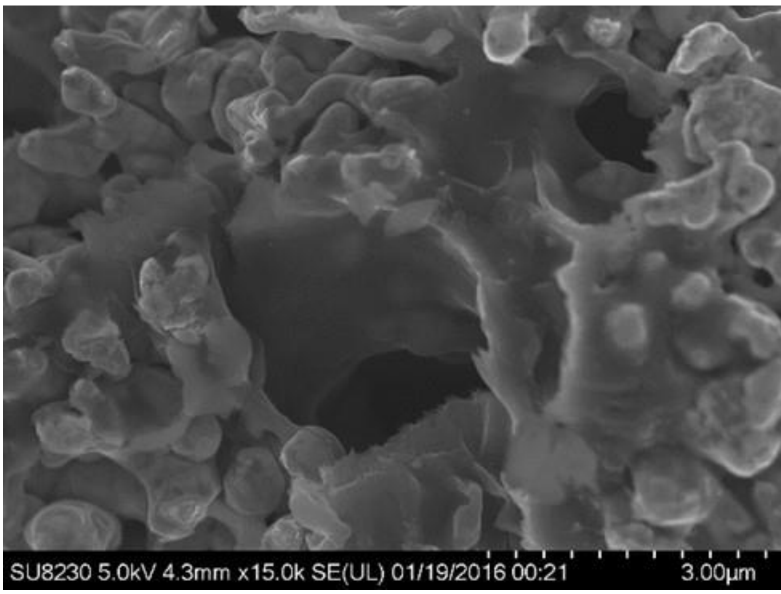


Figure 3.8: SEM micrographs showing (a) filling of pores by conducting polymer through the cross-section of sample (b) magnified view of the cross-section near the bottom of the porous architecture

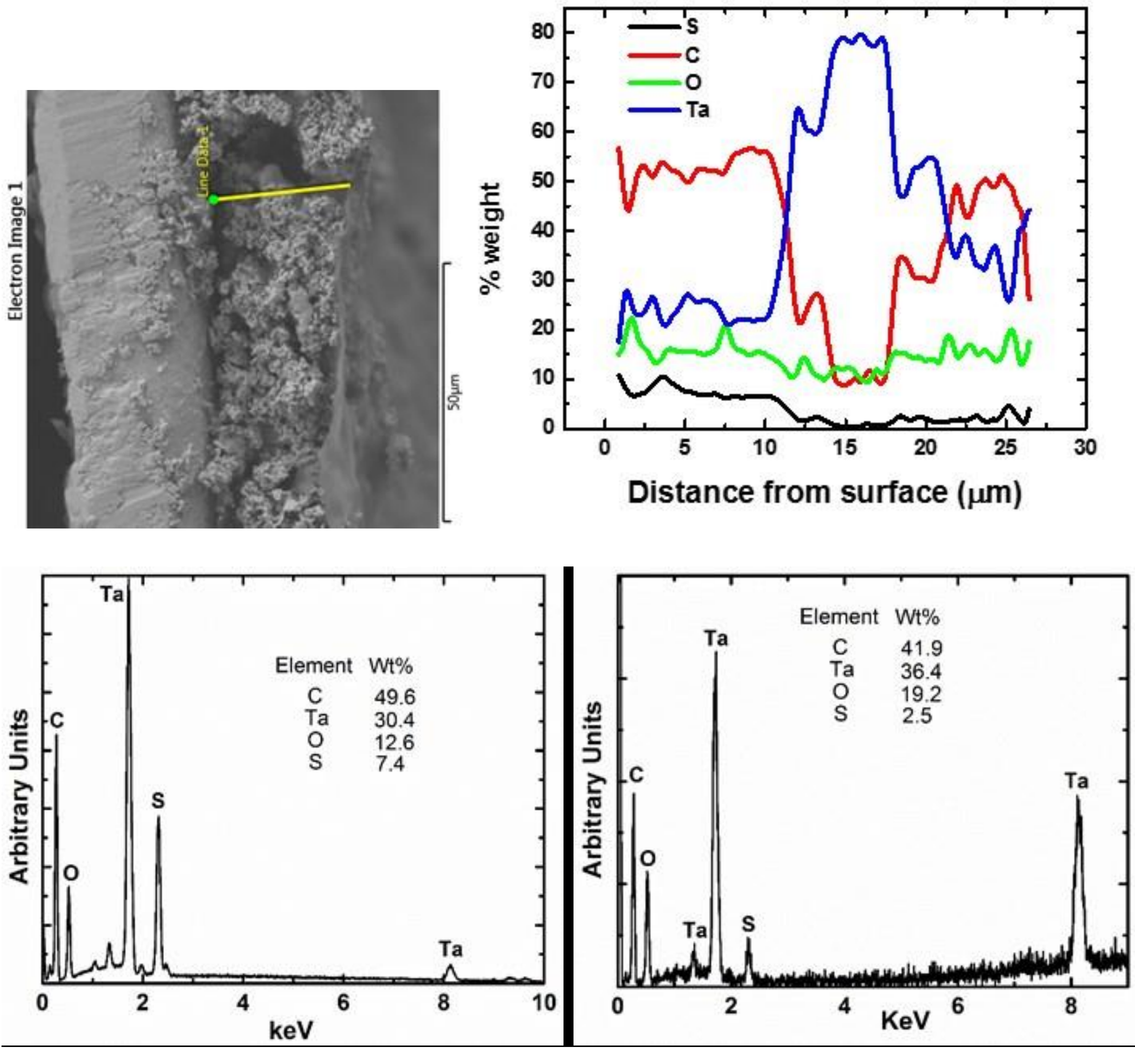


Figure 3.9: (a) Electron image of the sample showing the region with the line-scan, (b) EDS line-scan showing the elemental composition of the elements across the cross-section, (c) EDX spectrum at the top of the porous architecture, (d) EDX spectrum at the bottom of the porous architecture

Table-3.2: capacitance density measurements (μF/cm^2) at low frequencies from wet and dry measurement methods for a capacitor with 43 nm dielectric thickness for 25 μm anode thickness

Particle size (nm)	Cap density from wet measurements (100 HZ)	Cap density from dry measurements (100 Hz)	Cap density from dry measurements (> 1 MHz)	Conducting polymer Infiltration efficiency (%)
Planar Ta	0.42	0.4	0.4	100
100-150	450	100	-	22
250-400	120	30	25	25
700-850	18	14	11	78

3.3.5 Electrical Characterization

The electrical characterization includes measurement of capacitance density as a function of frequency for different particle sizes (keeping dielectric thickness as constant), leakage properties as a function of dielectric thickness (keeping the particle size as constant) and investigation of leakage conduction mechanism in tantalum pentoxide are described in the subsequent sub-sections.

3.3.5.1 Capacitance density at high frequencies for different particle sizes

The capacitors were characterized for capacitance density as a function of frequency (Fig-3.10). The results discussed here unless otherwise stated have a dielectric thickness of 45 nm. The capacitors with 150 nm anode particle size did not demonstrate a stable capacitance as a function of frequency as observed by a gradual drop of 9% in capacitance at lower frequencies (50 Hz – 1 MHz) followed by a steady capacitance drop of 27% in the

higher frequency range (1MHz – 10 MHz). This drop could be attributed to thin or incomplete coverage of conducting polymer over the porous anode structure, which leads to a rise in ESR. This could be seen from the SEM micrograph (fig-3.7b) where the conducting polymer coverage was observed at depths of few hundred nanometers from the top surface. The incomplete coverage yields inaccessible surface area and lowers realized capacitance. This is corroborated from the ratio of capacitance density measurements from wet and dry measurements (both at 100 Hz) given by the conducting polymer infiltration efficiency (Table-3.2). The capacitance in a wet-measurement method was measured by dipping the anodized porous tantalum as the anode in a sulfuric acid electrolyte with platinum metal as the cathode. The details on wet-measurements method are described in Appendix-A. Liquid electrolyte accesses the entire surface area of the nano-porous anode, hence, the capacitance obtained from the liquid measurements was assumed to be maximum achievable capacitance and was benchmarked with the capacitance obtained using conducting polymer as the cathode. Finer particles after sintering are known to yield better packing density in the sintered compacts that reduces the pore size and density in the samples with 150 nm average particle size making the conducting polymer infiltration hard inside the pores. In the case of 150 nm anode particles, the conducting polymer infiltration efficiency is a mere 22%.

In addition to a drop in capacitance, a lower cathode infiltration leads to a larger resistance path. ESR (R), operating frequency (ω) and capacitance (C) are related by the following equation:

$$\omega RC = 1$$

For a capacitor with higher ESR, the capacitance keeps going down, the resonant frequency got pushed higher up and the LC resonance was never observed in the case with 150 nm anode particles. On the other hand, capacitors with 250 nm anode particle size showed a stable capacitance density of 0.25 μF/mm^2 before drooping off at 1.33 MHz (Fig-3.10). The plot for the 250 nm anode particle was obtained after accounting for the parasitic inductance from the measurement tool and the capacitor itself. A porous structure with larger particle size further aided the cathode impregnation through the pores with cathode accessing the surface area in the first 10 microns of the porous structure. However, the still inaccessible surface areas by cathode meant a capacitance droop at higher frequencies (Fig-3.10) and a lower realized capacitance density. This was again corroborated by the cathode infiltration efficiency of 25% marginally above the one corresponding to 100-150 nm particle anodes (table-3.2).

The operating frequency was pushed further by using coarser particles having large pore sizes that ensured even thicker conformal coating preventing a capacitance droop at higher frequencies. This was accomplished using the larger particle size of 700 nm, which showed stable capacitance density up to 10 MHz. This could be due to better-conducting polymer impregnation through the larger pore sizes, which led to thicker coverage corroborated by the SEM micrograph (Fig-3.8c) and cathode infiltration efficiency of 78% (Table-2). The downside of working with larger particle size is the overall lower capacitance density compared to capacitance densities obtained from smaller particle size.

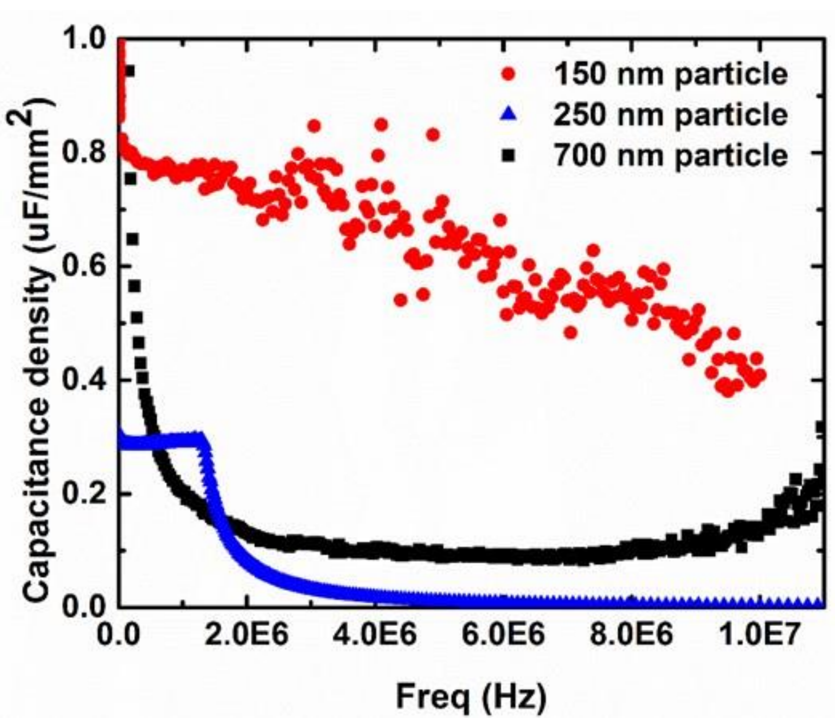


Figure 3.10. Cap density profile as a function of frequency (43 nm dielectric) with varied anode particle sizes

3.3.5.2 Leakage properties as a function of dielectric thickness

The capacitors were optimized for leakage properties by growing dielectrics of different thicknesses as mentioned in the experimental section. Fig-3.11a shows the normalized I-V plot for capacitors (with metal as the top electrode) for dielectric thicknesses of 23 nm, 45 nm and 93 nm for capacitors with a particle size of 300 nm. As expected, the thicker dielectric showed lower leakage current even at a higher voltage as compared to thinner dielectric because of the relatively lower defect density. The thinnest dielectric showed the worst leakage characteristics due to leakage contributions from ion hopping, SCLC and Schottky mechanisms based on leakage models [14]. The capacitance measurement after

leakage current measurement showed no change in capacitance for capacitors with either of the dielectric thicknesses indicating the robustness of the dielectric.

The presence of thicker dielectric reduces the leakage current from close to 2.5 μA/μF to less than 0.05 μA/μF at 3V as the dielectric thickness was raised from 23 nm to 93 nm. The conducting polymer as the cathode was shown to demonstrate self-healing (Fig-3.11b). The capacitor was subjected to a DC voltage, known as burn-in voltage (usually 50-60% of the anodization voltage), and dwelled at that voltage for one minute.

The normalized leakage current dropped by more than 100% for thicker dielectrics (45 and 93 nm) at that voltage, exhibiting the self-healing behavior. During self-healing, the presence of defects sites in the dielectric offers a low resistance path in the otherwise insulating dielectric leading to a current surge through the conducting polymer next to it. This causes the conducting polymer at those localized sites to evaporate, thereby, locally isolating the defects [16]. The current surge accounts for the initially high normalized leakage current; as the self-healing takes place, the normalized leakage current comes down as the current encounters resistance while passing through the defect-free regions of the dielectric. The self-healing behavior is not profound in thinner dielectrics compared to the thicker dielectrics on account of relatively larger defect densities already incorporated in the former during anodization, hence, providing multiple pathways for current propagation.

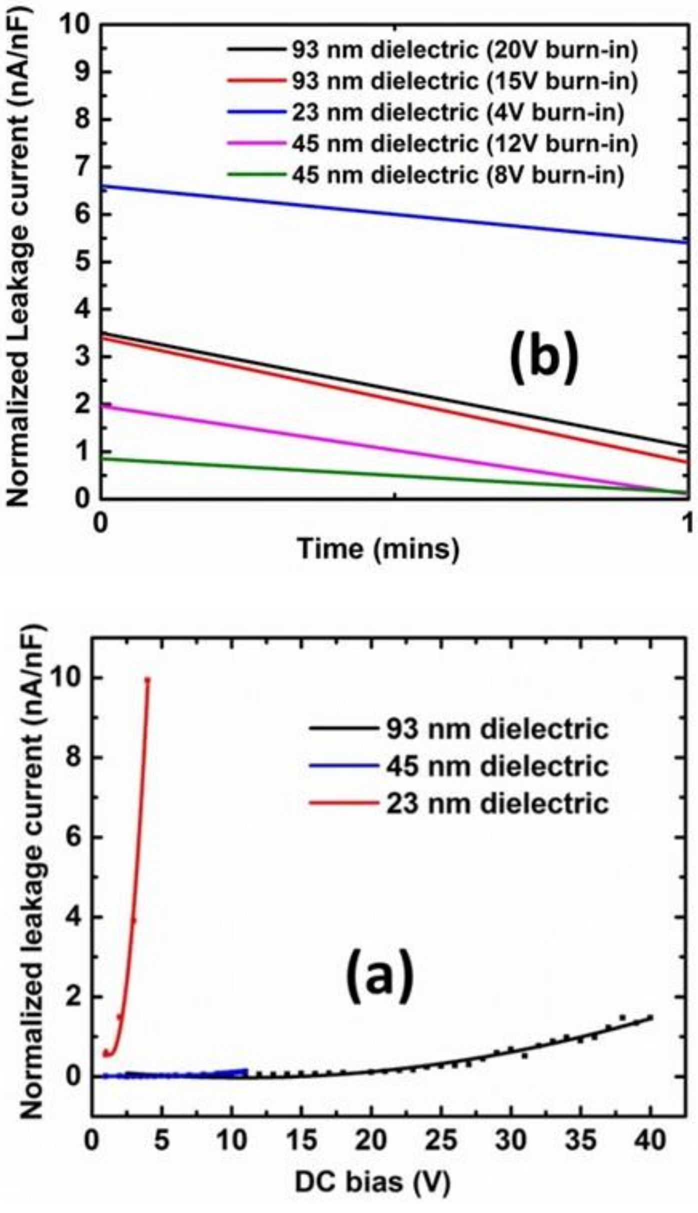


Figure 3.11. (a) Leakage current: I-V plots for different dielectric thicknesses (b) Plots showing self-healing behavior in capacitors with different dielectric thickness (each point in the plot represents average of data from five samples)

3.3.5.3 Investigation of leakage conduction mechanisms

Leakage in a dielectric could be attributed to the material and structural properties of the dielectric. Structural properties of the dielectric could be attributed to mechanical defects such as pin-holes, cracks, etc. The present analysis deals with the material properties of the dielectric that contributes to the leakage in the dielectric. Anodized tantalum was characterized for different leakage conduction mechanisms using four classical leakage mechanisms - Schottky effect, Poole-Frenkel effect, Ion Hopping mechanism and Space Charge Limited Conduction (SCLC) mechanism (Fig-3.12).

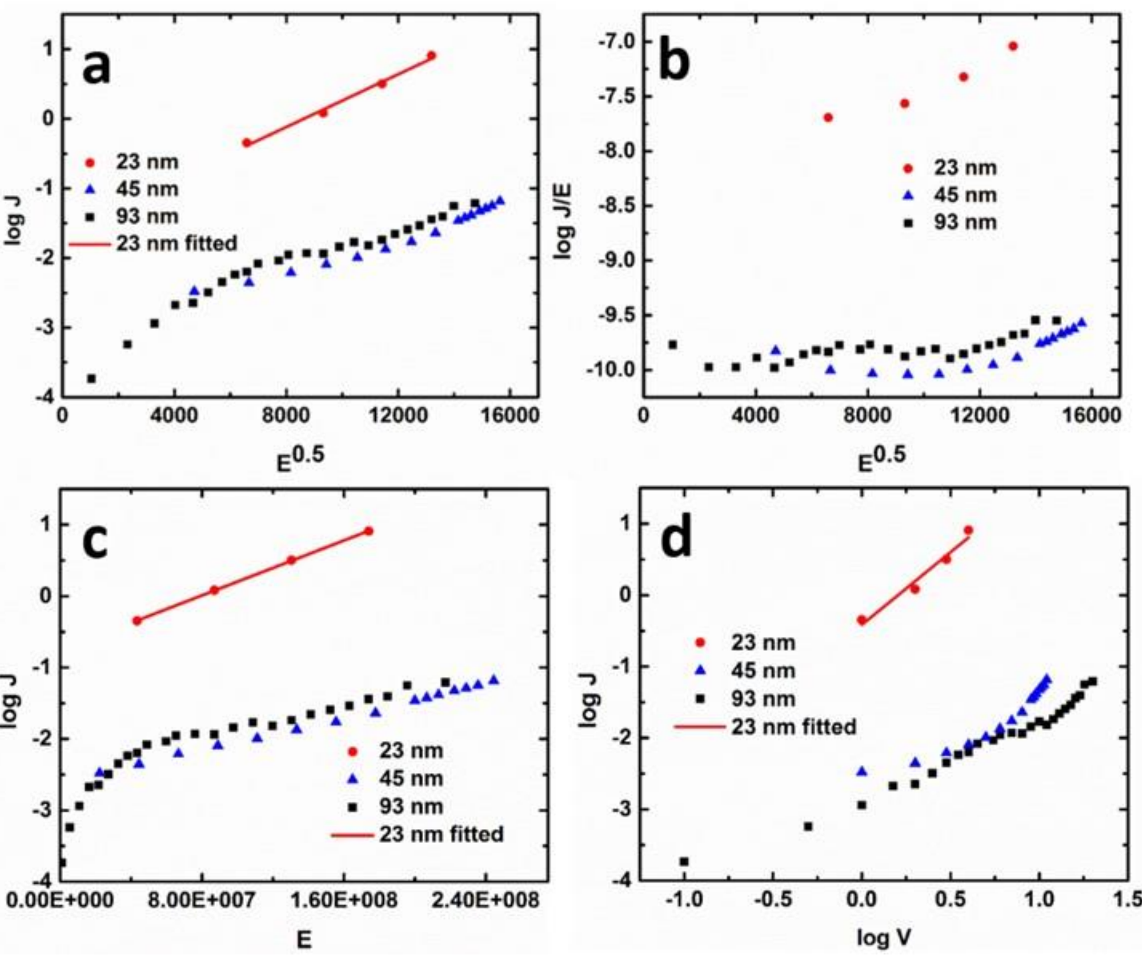


Figure 3.12: Conduction mechanism (a) Schottky (b) PFE (c) Ion hopping (d) SCLC

Schottky conduction mechanism corresponds to the lowering of energy barrier due to thermal excitation of electrons across the metal-dielectric interface [74]. The leakage current flow attributed to Schottky mechanism [75] is given by

$$\ln(J_s) = \frac{1}{2KT}\beta\sqrt{E} + \left[\ln\left(A^{*}T^{2}\right) - \frac{q\phi_s}{KT}\right]$$

where, J_s is the current density, E is the electric field, A^* is the Richardson constant, T: absolute temperature, Φ_s is the barrier height, K is the Boltzmann's constant, β is a material constant given by

$$\beta = \sqrt{\frac{q^3}{\Pi\varepsilon\varepsilon_o}}$$

where, ε: relative permittivity at high frequency (optical dielectric constant), ε_o: permittivity in vacuum and q: elementary charge. The optical dielectric constant is used for the sake of calculation since the dielectric relaxation time is slower than the electron residence time in the dielectric [74]. Defects in the titania dielectric would be dominated by Schottky electronic conduction mechanism if the plot of ln(Js) vs √E is linear with a slope close to 2.4E-04 assuming an optical dielectric constant of 4.1 [76]. In Fig. 3.12a, the experimental data for the thinnest dielectric anodized fits the characteristic Schottky plots quite well. Furthermore, the slopes for the thinnest dielectric (1.9E-04) comes close to the theoretically calculated slope of 2.4E-04. Hence, only the thinnest dielectrics exhibit Schottky conduction mechanisms. This could be attributed to the high electric fields experienced by the electrons in the thinnest dielectric exciting them to surmount the metal-dielectric Schottky barrier (Fig-3.13).

For further understanding the leakage current mechanism Poole-Frenkel mechanism was analyzed, that involves electron hopping from a trapped site in the dielectric (created by an ion vacancy) into its conduction band of the dielectric under

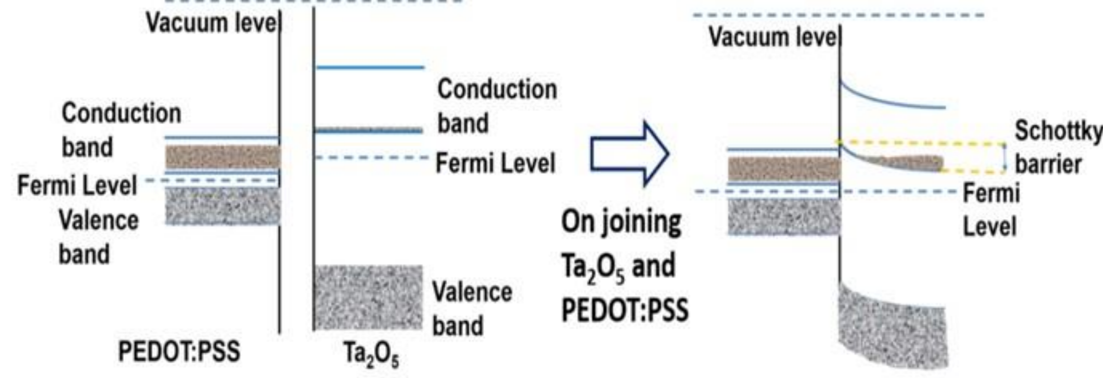


Figure 3.13: Schematic of band diagram depicting the Non-Ohmic contact between the PEDOT:PSS and Ta_2O_5

applied electric field. Leakage current attributed to Frenkel-Poole Mechanism[74, 75] is given by

$$\ln\frac{J_{PF}}{E} = \frac{\beta}{\zeta KT}\sqrt{E} + \left[\ln(C) - \frac{q\phi_s}{\zeta kt}\right]$$

Here, J_{PF} is the current density, C is a proportionality constant and ζ can take a value between 1 and 2 and is a function of the acceptor compensation in the material. Frenkel-Poole effects dominate the defects in dielectric if the plot of ln (J_{PF}/E) vs √E is a straight line and the value of ζ falls between 1 and 2. In Fig. 3.12b, the experimental plots for none of the dielectrics fit the characteristic PFE plots. Hence, Poole-Frenkel conduction as a leakage mechanism could not account as the mechanism for the leakage current in the titania dielectric.

Ionic conduction as a defect mechanism could be attributed to the hopping of vacancies such as oxygen vacancies/interstitials and titanium ion/interstitials vacancies within the dielectric. The current attributed to ion hopping [74] is given by

$$\ln(J) = \frac{qa}{KT}E + \left[\ln(qan\nu) - \frac{E_a}{KT}\right]$$

where a = mean hopping distance of the ions, n = electron concentration in the conduction band, υ = frequency of thermal vibration of electrons at the trapped sites and E_a = activation energy for the electrons to jump from the trap states to the conduction band. Ion hopping defects would be present in the dielectric if the slope of ln(J) vs E is a straight line with a slope close to 1.58E-08, assuming mean hopping distance of 4 Å (based on interatomic distance). In Fig. 3.12c, the slope for thinner dielectric (1.2E-08) comes close to the theoretically calculated slope of 1.58E-08 while the thicker dielectric, anodized to 20V has a slope (0.55E-08) that lies far away from the theoretical value. On the other hand, the experimental data for the thickest dielectric does not show a straight line. Since lower anodization voltage yield thinner dielectrics application of bias leads to higher electric field experienced by the trapped ions such as oxygen and tantalum vacancies or oxygen and tantalum interstitials. Thus, it is easier for the oppositely charged species to migrate to the oppositely charged electrodes leaving behind oppositely charged vacancies. This is also known as Schottky ionization defects (not to be confused as the cause for Schottky electronic conduction mechanism discussed earlier). For example, a Schottky effect in a Ta_2O_5 lattice can be characterized by the creation of tantalum and oxygen vacancies represented by V_{Ta}^{-5} and V_o^{+2} respectively) in equation (5).

$$Ta_2O_{5\,Lattice} \Leftrightarrow 2V_{Ta}^{-5} + 5V_o^{+2}$$ ----------------------------(5)

In addition, a trapped ion in a dielectric would experience electric field when placed under an electric bias and will have enough energy to relocate by leaving its lattice point, thereby forming a vacancy) and occupying an interstitial, also known as Frenkel defects. Frenkel defects in a Ta_2O_5 lattice could be explained in terms of oxygen vacancy and oxygen interstitials or titanium vacancy and titanium interstitial, represented by V_o^{+2} and O_i^{-2} or V_{Ta}^{-5} and Ta_i^{+5} as given in equations (6) and (7) respectively.

$$O_{Lattice} \Leftrightarrow O_i^{-2} + V_o^{+2}$$ ------------------------------------(6)

$$Ta_{Lattice} \Leftrightarrow Ta_i^{+5} + V_{Ta}^{-5}$$ ------------------------------------(7)

SCLC is an electronic conduction mechanism, which is observed when an electrode makes Ohmic contact with the dielectric leading to electron transport from the electrode to the dielectric, which subsequently migrate under an electric field induced space charge [74]. Dielectrics with SCLC mechanism yield a power law relationship between J and voltage (V), with different slopes at different voltage [77, 78]. In Fig. 3.12d, the slope for the thinner dielectric (8V anodized sample) plot is a straight line with a slope of 2 till 3V. For the thicker dielectric (formed at 20V), the log J-log V plot displayed a slope of 3 between 7-11V. The thickest dielectric (formed at 40V) displays different slopes for different DC bias. The slope corresponds to 0.78 in the DC bias below 1V, indicating negligible leakage below 1V, whereas the slope stays close to 1 (~1.14) for the region between 1 and 10V suggesting near-Ohmic contact for the entire bias range (Fig-3.12d). The slope goes up to 2.48 between 11-20V. This could be attributed to the lower work-function of tantalum relative to tantalum pentoxide, which leads to the formation of Ohmic junction through which electrons could flow from metal to semi-conductor (Fig-3.14). The

different slopes at different voltages closely follow with the characteristics of SCLC mechanism mentioned in [77].

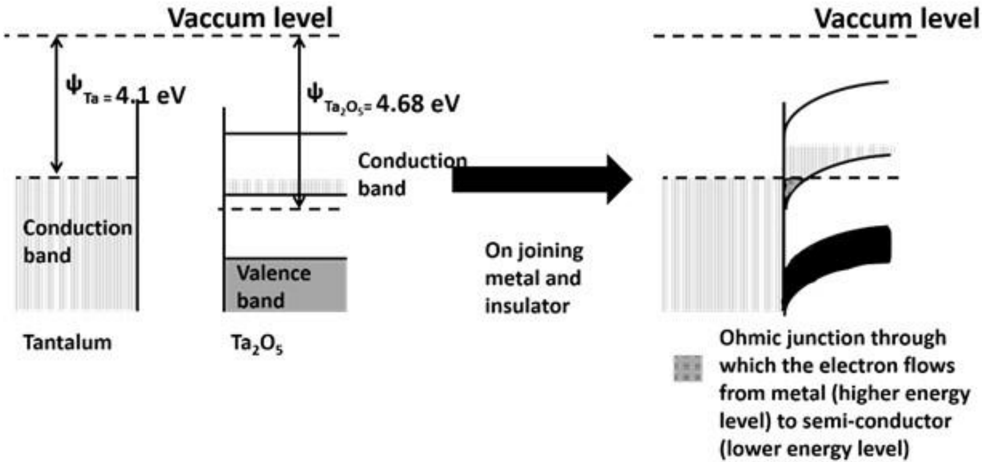


Figure 3.14: Schematic of band diagram depicting the Non-Ohmic contact between the Ta and Ta_2O_5

Thinnest dielectricss have high-leakage currents because of multiple active conduction mechanisms. The above analyses indicate that leakage conduction from electrons is manifested by the electron hopping across the electrode-dielectric interface, whereas vacancies and interstitials of oxygen and tantalum account for the leakage conduction from ions. The two thicker dielectrics have lower defect density due to only one conduction mechanism (SCLC) and hence would yield lower leakage current.

3.4 Conclusions

The work addresses the strategic need for ultra-miniaturized power capacitors using nano-scale anodes, nano-scale dielectrics and nano-scale cathodes in new geometries and small form-factor. The research also investigates the effect of particle size variation in anode particles on the resulting capacitance density and surface area enhancement, and the film growth mechanisms during anodization. The work also studies the extent of cathode

infiltration inside the porous capacitor architecture for different particle size anodes and its effect on the ensuing operating frequency. The capacitors with 700 nm particle anode size demonstrated capacitance densities of 0.13 μF/mm^2 up to 7 MHz, which is 5X more than any reported till date at the mentioned frequency. The study explores the effect of dielectric thickness on the leakage current of the capacitors, resulting less than 0.05 μA/μF at 3 V for thicker dielectrics (with thicknesses more than 45 nm). The study also analyzes the different leakage conduction mechanisms to account for the difference in leakage currents in thinner and thicker dielectrics.

Chapter-4

CAPACITOR INTEGRATION

Abstract

This chapter describes the integration of the pre-fabricated capacitor on silicon substrates. The chapter recapitulates the fabrication of high-density tantalum capacitors, followed by a description of integration steps to embed the high-density capacitors on silicon substrates. Each integration step was characterized using SEM and confocal optical microscopy. The planarization layer was observed to conform along the trenches between the tantalum pads. The drilled vias, separately accessing the anode and cathode, were 300 µm wide with the vias metallized using seed layer deposition and electroplating to complete the integration process.

4.1 Introduction

Next generation electronics demand power supply with minimum noise levels for high performance and efficiency. Passive components such as decoupling capacitors help achieve these noise targets by bypassing high impedance power supply components in the circuit. The state-of-the-art discrete capacitors cannot meet the performance requirements due to their long interconnection lengths that induces large parasitic inductances and limit their operating frequency [79, 80]. However, if the decoupling capacitors are placed closed to the active IC, they can be far more effective with reduced inductances from shorter interconnection lengths [81]. Integration of decoupling capacitors in multichip power modules, close to active chip has therefore been researched extensively. Glass- and silicon-based interposer technologies that utilize vertical through-via interconnections have shown way to improve power distribution network (PDN) performance with thin power-ground planes [82-84]. However, integration of ultra-high density capacitors with such substrate has not yet been demonstrated.

Leading-edge discrete passives such as multilayered ceramic capacitors (MLCCs) from Murata are less than 150 microns thick, and can be embedded in thin organic laminates or assembled on the backside of the package [85]. In order to address the thicknsess constraints and excessive parasitics from SMT components, integrated capacitors are pursued with trench capacitors or thinfilm MIM capacitors. Most substrate-integrated decoupling capacitors rely on thin high-permittivity dielectrics to be able to integrate close to IC. These include ferroelectrics such as barium titanate and lead lanthanum zirconate titanate [31, 86-88]. In addition to the high processing temperatures (>700°C) of the above-mentioned ferroelectrics, they also show poor voltage response that limits their applications

in power electronics. Several groups have also worked on tantalum pentoxide dielectrics (Ta_2O_5) for planar [89, 90]or TSV- or TPV-integrated decoupling capacitors [81, 91]. However, Ta_2O_5 capacitors are limited to low capacitance densities (~5 nF/mm^2) that would require large-area capacitors to meet the required capacitance. Thin particulate electrode-based tantalum capacitors with high surface area per unit volume, if integrated directly on silicon, can meet the capacitance targets for decoupling without taking up extra package space.

The key process challenge with tantalum capacitors is the high processing temperature for electrode formation. This paper demonstrates an innovative approach to address this challenge by pre-fabricating electrodes on a free-standing foil, which are then transferred onto the active wafer to form the capacitors. The integration approach is designed to also embed these thin tantalum capacitors on alternative substrates such as organic, glass and silicon, with copper via interconnections for lower parasitics. A schematic of the integrated capacitor structure with electrodes, dielectrics and copper via interconnections is shown in Fig. 4.1.

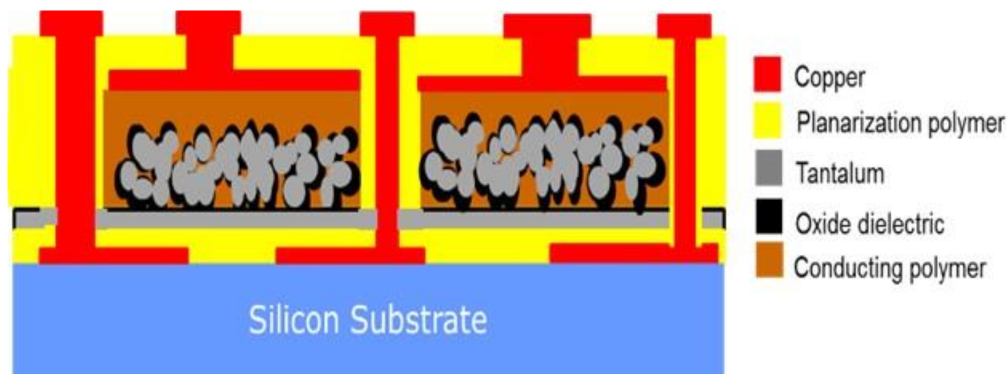


Figure 4.1: High-density capacitor developed in this work

4.2 Fabrication of capacitor

The schematic in Fig-4.2 highlights the steps to fabricate high-density capacitor. Tantalum foil with sintered tantalum pads was laminated onto silicon substrates using a roll laminator. This was accomplished by roll-laminating ABF polymer dielectric (15 µm thick) onto silicon substrates at 110°C with roller-roller gap of 1 mm at speed 1. This was followed by roll-laminating the tantalum anode foil (with sintered tantalum pads) onto the ABF dielectric under the same roll-lamination conditions. The samples were annealed at 190°C for 90 mins to cure the ABF dielectric. Tantalum pentoxide, as a dielectric, was grown using the known anodization process. Anodization conditions were optimized to minimize the leakage properties (discussed in chapter-3). This was followed by cathode deposition using conditions described in chapter-3. Conducting polymer was used as the cathode along with evaporated metal current collector (described in Chapter-3). The cathode material was chosen because of its self-healing characteristics while the metal-current collector interface lowered the ESR. The cathode was patterned with a subtractive plasma-etching with the patterned metal current collector as the etch mask to conclude the capacitor fabrication. This was followed by integration of the capacitor, which is described in the subsequent section.

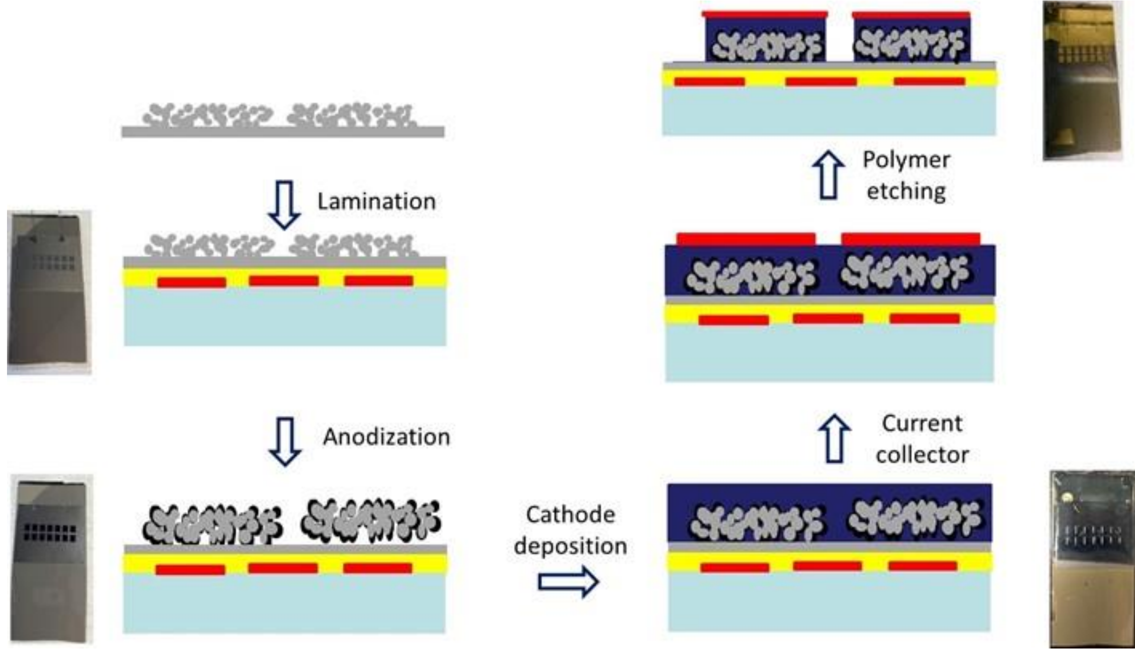


Figure 4.2: Schematic of capacitor fabrication

4.3 Integration of capacitor

The integration of the capacitor involves steps such as planarization, via-drilling, seed layer deposition, lithography, metallization, photo-resist stripping and seed layer removal (Fig-4.3) shown in the schematic.

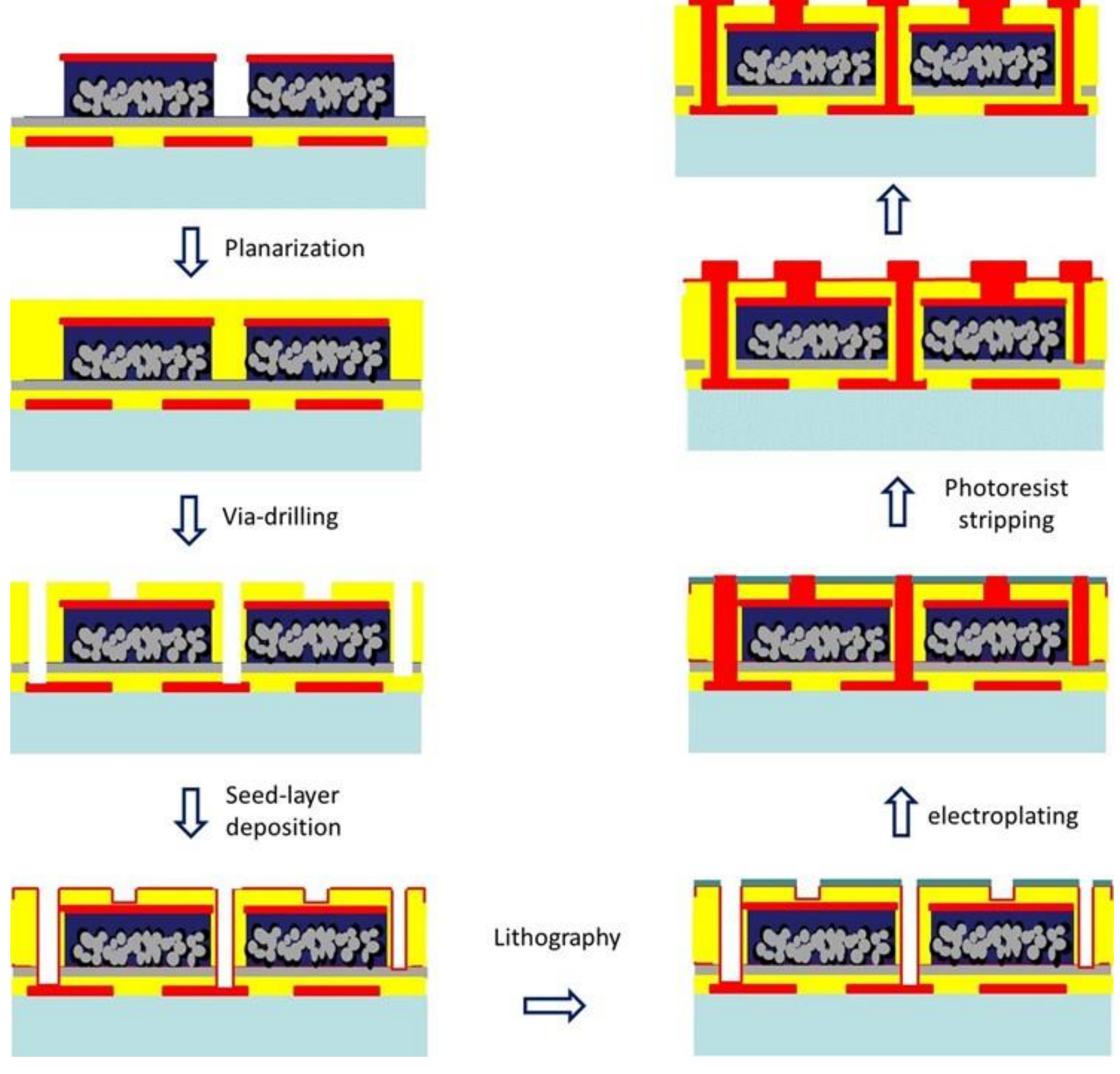


Figure 4.3: Schematic of capacitor integration

4.3.1 Planarization

A planarization layer is required to embed the capacitor in substrates as a part of the package. There are different planarization options available (Table-4.1).

Table 4.1: Planarization options

Providers	Polymer	Pros	Cons
-Dupont -HD Microsystems	Polyimide	-Very high elongation to failure; extremely tough; -standard material for WLP passivation	-High moisture absorption (1.5%) -High temp curing (<300 C)
-BCB	Benzo-cyclobutene	-Standard material for passivation; -Low loss; -13% elongation to failure; 80 MPa strength	-High-temp curing (250 C)
-Zeon Chemicals	ZIF	-Low moisture uptake -Curing temperature – 180 °C/30 min	Unavailable
-Ajinomoto	ABF	-Available in multiple thicknesses -Low loss	-High curing temperature (190 °C for 90 min) -Low elongation to failure (5%); -Strength: 90-100 MPa;

Table-4.1 continued			
-TOK	Photo-dielectric	-Photo-definable -Low dielectric loss -Good elongation to failure (12-15%) compared to epoxies	-High curing temperature (250 °C)
-Dow corning -Sylgard 184	Siloxane PDMS	-Low moisture absorption -Low curing temperature -100% elongation to failure	-Low strength (6 MPa)
-Parylene + ABF	CVD deposited	-Very low moisture uptake -Highly conformal -Low loss	-Limited thickness

There were three front-up options available at Georgia Tech as a planarization layer – Zeon ZS 100, ABF and parylene. Zeon ZS 100 has a low moisture uptake and a loss of less than 0.005 [92, 93], however, it was not readily available. On the other hand, ABF is available in multiple thicknesses and is a standard polymer dielectric pursued as a planarization layer in the industry [94]. CVD parylene, on the other hand, has a very low moisture uptake and

a very low loss and is deposited using CVD making it extremely conformal [95]. However, CVD process also makes it available in limited thickness.

In this work, ABF was used as the planarization material by vacuum-laminating the ABF onto the fabricated capacitor. The thickness of the ABF layer was 45 µm. The vacuum lamination was performed under 0.1 atm pressure followed by a load of 100 atm pressure at 93°F. The vacuum sucked the air from the trenches between the capacitor pads and the applied pressure and heat led to the flow of the polymer and the subsequent conformal filling of the trenches between the capacitor pads with the polymer dielectric. This was followed by curing of the polymer dielectric at 190°C for 90 mins. Fig-4.4 shows the SEM micrograph of the dielectric planarization layer. The micrograph shows the Ta pads on Ta foil laminated onto Si/SiN using ABF. Another ABF layer is laminated onto the tantalum pads and is shown to conform to the trench region between the tantalum pads.

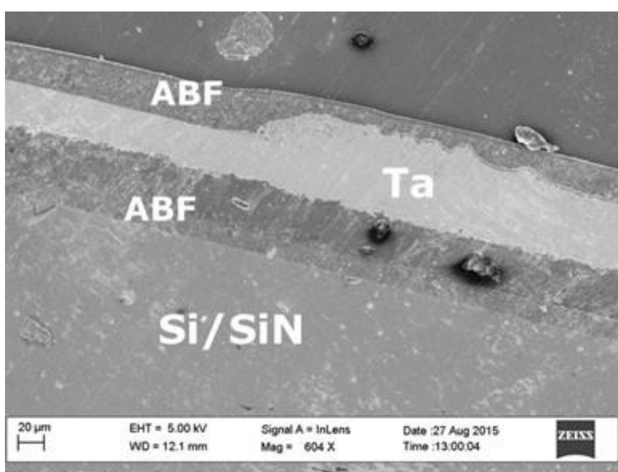


Figure 4.4: SEM micrograph of planarized ABF on finished capacitor

4.3.2 Via-drilling

The next step in the integration process is to drill vias to separately access anodes and cathodes. The vias were drilled through the planarization polymer by CO_2 laser with the metal layer underneath acting as the etch-stop layer with tantalum as the etch-stop layer for the anode and current collector for the cathode respectively. The via-drilling step was outsourced to Micron laser. The vias were characterized using SEM (Fig-4.5a). The depth of the via was measured by observing the cross-section of the via on the cathode and anode. The vias accessing the anode has a depth of 35 μm (Fig-4.5b) while the vias accessing the current collector cathode has a depth of 15 μm (Fig-4.5c). The via was 310 μm at the top and 240 μm wide at the bottom indicating a taper of 45°. The via ablation left behind some amount of silica filler residues as shown in the SEM image (Fig-4.5d), which could be attributed to the presence of polymer and silica fillers. Permanganate de-smear is the most common approach to eliminate this residue. However, a milder process was desired. Hence, the silica fillers were eliminated using Reactive Ion etching (using Plasma-therm RIE) with CHF_3 and O_2 gas as the etchant gas with CHF_3 gas used for etching through the silica particles. Further optimization is being carried out by researchers at Georgia Tech – Packaging Research Center.

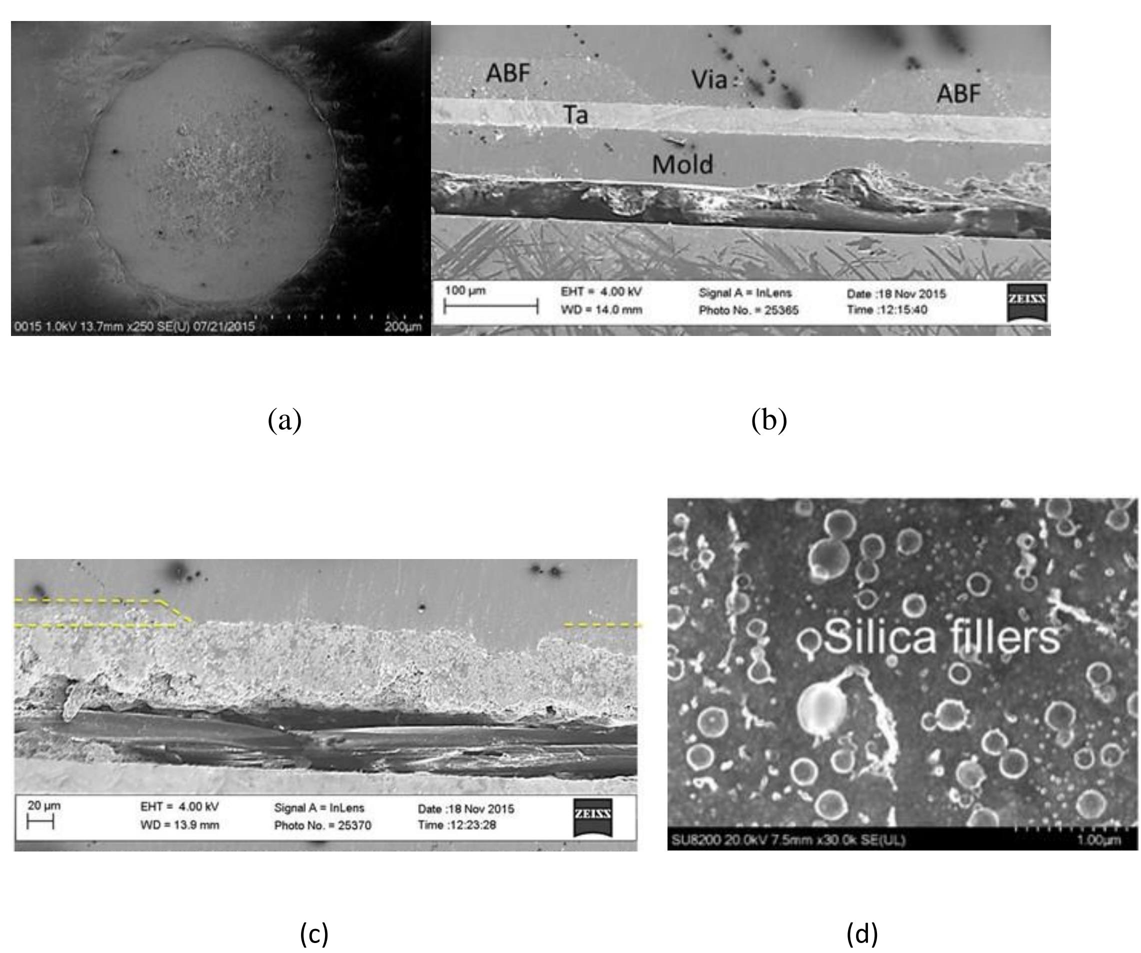


Figure 4.5: (a) SEM micrograph of the drilled-via (top-view) on tantalum (b) Cross-section of the via on tantalum anode (c) Cross-section of the via on current collector cathode (d) SEM micrograph of the silica filler residue inside the via

4.3.3 Seed layer deposition

Copper has been used as the interconnect material in microelectronics packaging due to its low resistivity and high electro-migration resistance. This work reports the first demonstration of copper as an interconnection material for integration of high-density capacitor in silicon substrates. Copper deposition was carried out in two steps – seed layer deposition using electroless copper deposition followed by electrolytic copper deposition

in the vias. The seed layer deposition was carried out using electroless plating technique. Electroless copper served as the template for copper deposition using electroplating (described in the next section) with copper ions getting electrochemically reduced to copper on the electroless copper surface with the latter acting as an electrode. The key step in electroless plating is the adhesion of copper to the insulating ABF polymer dielectric. Higher adhesion could be typically achieved by modifying the surface of the polymer dielectric so as to lower the interfacial energy between the metal and the dielectric. This could be accomplished by physical or chemical treatments[96]. Physical treatment induces mechanical anchoring of the metal or the catalyst in the small cavities created on the roughened surface of the polymer dielectric. Chemical treatments involve forming chemical groups on the surface, which can form chemical or ionic bonds between the polymer dielectric and the catalyst/metal. This work involved physical treatment to induce adhesion of the polymer dielectric to the catalyst or the metal using a swell-and-etch treatment. The swell treatment rearranges the polar groups in the polymer dielectric into packets for etching (Fig-4.6). The polymer surface was then de-smeared using permanganate solution, which preferentially attacked the ether linkages within the packets to form pores or micro-cavities. This was followed by dipping the polymer dielectric in a neutralizer bath to remove the etchant before the catalyst deposition step.

Figure 4.6: Mechanism of swelling in epoxy based polymer dielectric – polar groups re-arranged into packets[96]

Next step involved palladium incorporation as a catalyst for reduction of copper ions on polymer surface during electroless plating. The electroless bath usually has reducing agents such as HCHO, Dimethyl amine borane (DMAB), etc., which helps reduce copper salts in the bath to copper[97]. The reduction is catalyzed at the Pd catalyst sites anchored on polymer dielectric surface where the copper salt is reduced to Copper. Electroless plating was subsequently performed for 20 mins followed by a dip in acid bath and passivation to prevent oxidation. Fig-4.7 shows the electroless plated vias on gold pads and tantalum corresponding to the cathode (Fig-4.7a) and the anode (Fig-4.7b) respectively. The surface roughness on anode via bottom is found to be less than 1 µm on tantalum anode pads. The roughness on cathode via was much higher corresponding to 10-15 µm arising from printed tantalum anode topography. Electroless copper deposition was followed by the lamination of 15 µm thick dry photoresist film that serves as a mask for selective electroplating of the vias on cathode and anode.

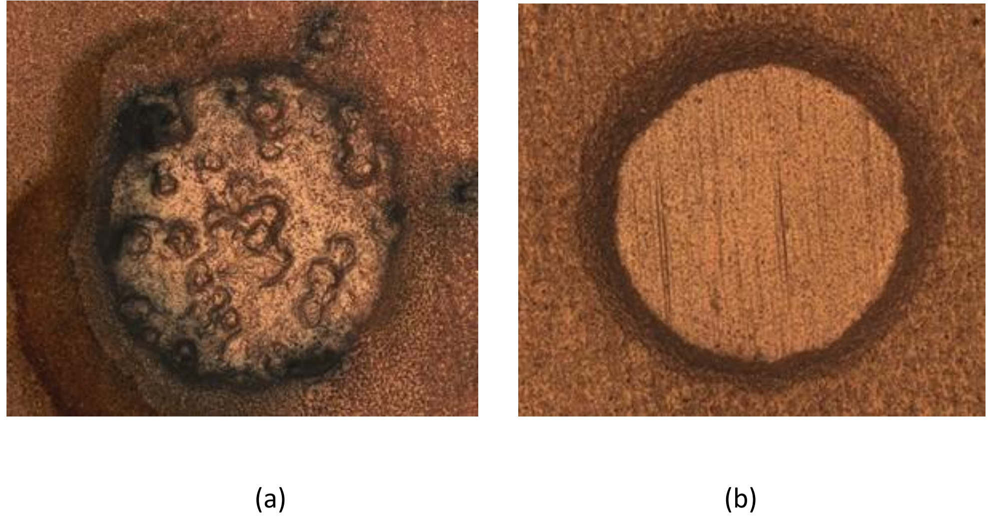


Figure 4.7: Optical micrograph of electroless plated vias (a) cathode (b) anode

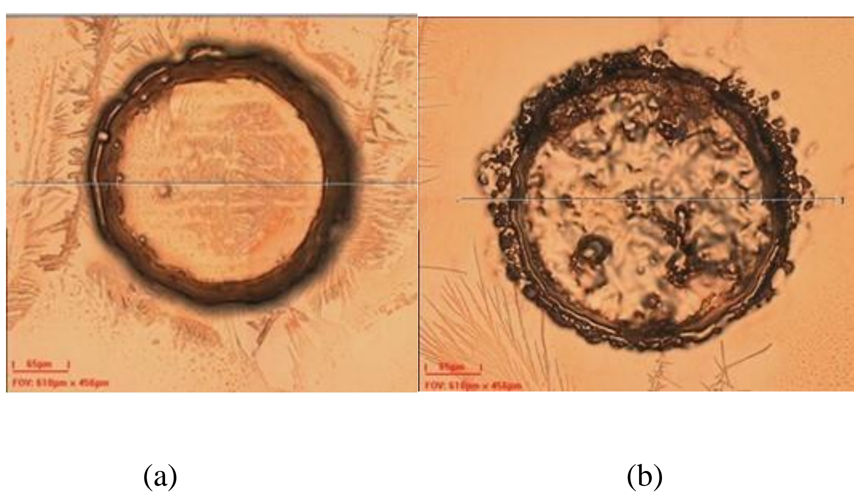
4.3.4 Metallization

The final step in the integration of high-density capacitor is metallization of the vias through electroplating of copper. Electroplated copper provides void-free fill with low resistivity, and large grain size of copper, which is responsible for its high electro-migration resistance and higher reliability [98]. Electroplating bath consisted of cupric ions, sulfuric acid, and trace organic additives. Electrical contact was made to the seed layer and current was passed to reduce the copper ions at the surface of the sample. The additives consisted of suppressors such as polyethylene glycol that reduce the plating rate at the top of the vias by blocking of growth sites on the copper surface. Other additives such as di-mercapto-propane sulfonic acid accelerated plating in the bottom of the vias [98]. The conditions of the electroplating are mentioned in Table-4.2.

Table 4.2: Electroplating conditions

Parameters	**Values**
Bath temperature	30°C
Current density	1 A/dm^2
Plating Chemistry	Atotech
Plating duration	25 mins
Agitation	Air

Fig-4.8 shows the optical micrographs of the electroplated vias on tantalum (Fig-4.8a) and gold pads (Fig-4.8b) with partially filled vias. The electroplating step is being further optimized at the GT-PRC along with the supply chain partners to achieve complete filling. The photoresist was stripped post the electroplating step followed by seed layer etching to finish the integration process.



(a) (b)

Figure 4.8: Optical micrograph of electroplated vias (a) tantalum anode (b) current collector cathode

4.4 Summary

The chapter demonstrates integration process for the high-density capacitors. The chapter discussed the conformal filling of the planarization layers in the trenches as well as the via drilling process to separately access the anode and cathode. Further optimization steps are being carried out at GT-PRC to completely fill these vias using the electroplating process.

CHAPTER-5

HIGH-DENSITY TITANIUM CAPACITORS – AN ALTERNATIVE APPROACH

5.1 Introduction

Approaches to achieve high capacitance density can be broadly classified as those with high-surface-area but low permittivity, or with high-permittivity thin-films with limited enhancement in surface-area as described in Chapter-2. This chapter explores an alternative approach to address both the above limitations, by advancing all the three parameters: high-surface-area electrodes, thinner, and high-permittivity dielectrics to increase the capacitance density. This research demonstrates high-density capacitors using high-surface-area titanium metal electrodes, conformal high K and thin-film dielectric of titania. An illustration of this capacitor approach is shown in Fig. 5.1. High-permittivity and thin-film titania dielectric were grown on high-surface-area titanium anodes using anodization while conducting polymer was used as the cathode.

Titanium capacitors are gaining momentum as an alternative approach to tantalum due to their high permittivity compared to other oxides, and also abundant availability in mineral ores [99]. Titanium power technologies have claimed to have developed capacitor smaller and lighter than traditional capacitor with 300% more energy storage capacity. The choice of titanium metal as an alternative to tantalum comes because of its ability to form high permittivity oxide with simple electrolytic processes such as anodization. Titanium

ore abundance in the US is also a driving force to evaluate this valve metal's properties for capacitor applications. Among the key prerequisites of high energy density capacitors, the most critical one is to obtain anode metal that can be processed so as to obtain large surface/volume ratio. Titanium metal can be easily etched using wet chemical etchants or sintered [14] to form a porous anode to create desired high-surface-area geometry, to enable a low series resistance in a packaged capacitor while conformal, defect free high permittivity titania could be grown using low-cost anodization [34].

Commercially-available porous titanium foils with high-surface-area were used as the anode. The permittivity of anodized titania ranges from 40-120 [100], much higher compared to other oxide dielectrics such as alumina or tantalum pentoxide. The self-limiting nature of anodization process also leads to a uniform dielectric coating on the high surface electrodes [101]. The high capacitance density also results from thinner titania films obtained by controlling the anodization voltage. The chemical structure and electrical properties of anodized titania are investigated for their application as conformal ultra-thin dielectrics on high-surface-area titanium electrodes. The chemical structure is studied by XPS depth-profiling for the first time along with the role of anodization conditions on dielectric thickness, leakage current, and capacitance densities.

Pre-polymerized conducting polymer suspensions, PEDOT: PSS was used as the cathode. It is important to note that the cathode may not access the entire porous anode structure depending on the pore and particle size. This has been highlighted in the

schematic. Different leakage current models were used to identify the defect mechanisms in the titania film formed at different voltages. EDS and structural SEM studies were performed to investigate the morphology and structure of the titania films.

The key focus of the chapter is to: a.) investigate the role of anodization conditions on capacitance density and leakage currents, b.) elucidate the dielectric film composition along its thickness using surface analysis technique such as XPS, c.) demonstrate higher capacitance density with porous electrodes and conformal dielectrics.

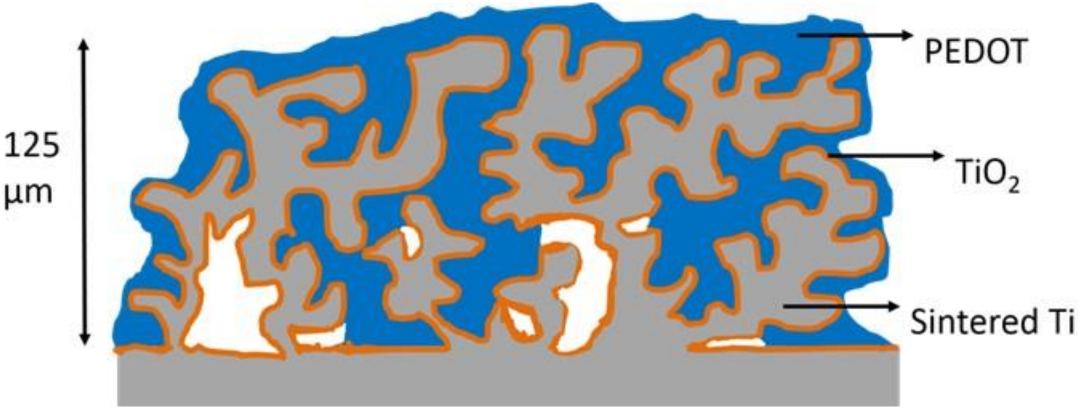


Figure 5.1: Cross-sectional representation of the etched Ti capacitor

5.2 Materials and Methods

The materials and processes for the high-density capacitor fabrication are described in the subsequent sub-sections.

5.2.1 High-surface-area Anode:

The high purity, commercially-available porous titanium foils (Accumet Materials, NY, USA) with a thickness of 125 μm were used as the anode. The porous foils were fabricated using powder metallurgy, involving particle sintering at higher temperatures, to provide high-surface-area of 8 m^2/g (estimated using BET technique).

5.2.2 High permittivity thin-film Dielectric:

High-permittivity titania (TiO_2) dielectric was conformally grown over the high-surface-area anode using electrochemical anodization. An anodically grown oxide, titania, was grown in a potentiostatic mode in a dilute phosphoric acid electrolyte with a concentration of 0.1 mM. The anodized films were thereafter rinsed in deionized water and dried at 100°C for 30 min to ensure complete removal of the electrolyte. The anodization process was performed under a bias voltage of 10 V with respect to the cathode (Pt) at room temperature for 30 min. The anodization conditions are listed in Table 5.1.

Table 5.1: Titanium anodization conditions

Anodization Voltage (V)	Anodization time (min)	Temp. (^{O}C)	phosphoric acid concentration (mM)	Current density (mA/cm^2)
10	30	25	0.1	20
40	30	25	0.1	20

The anodization reaction for titanium can be represented as:

$$Ti + 2H_2O \rightarrow TiO_2 + 2H_2 \text{----------------------------} (1)$$

The thickness of the dielectric was controlled by the anodizing voltage. A lower anodization voltage corresponds to a lower driving force for the diffusion of the oxide anions to form the dielectric oxide layer, which culminates in the formation of a thinner dielectric. Porous electrode capacitors were also compared with the planar titanium electrode capacitors, fabricated under similar conditions for their electrical properties.

5.2.3 Cathode

For the initial capacitance measurements, aqueous sulfuric acid (10 wt.%) was used as the counter electrode or the cathode. For practical solid-state capacitors device, conducting polymer, PEDOT: PSS (Heraeus, Leverkusen, Germany) was chosen as the

cathode. The electrode was dispensed as a suspension of pre-polymerized nanoparticles in 5 wt.% Dimethyl Sulfoxide (DMSO). The choice of this liquid-based cathode was based on its ability to wet the deep porous structures of the anodized titanium. The chosen conducting polymer has a conductivity of ca. 400-600 S cm^{-1}.

Zeiss Ultra60 FE-SEM was used for the morphological analysis. HP 4285A precision LCR meter was used for C-V measurements. Keithley 6485 picoammeter was used for the leakage current analysis.

5.3 Results and Discussion

The samples were characterized for the pore morphology, oxide composition, and leakage properties followed by their electrical characterization. Each of them is described in the subsequent sub-sections.

5.3.1 Morphological Characterization of high-surface-area anode

The commercially-acquired porous titanium anode was studied for the pore size and morphology before and after dielectric formation. The SEM micrograph in Fig. 5.2 shows high-surface-area anode with pore sizes ranging from 0.5- 20 µm. It is also evident from the micrograph that the porous anode was fabricated by sintering the micron-sized titanium particles that led to random pore size distribution. The absence of through-channels results in inaccessible surface-area inside the bottom electrode architecture implying the

possibility of reduced cathode penetration inside the porous structure. This could lead to a substantial reduction in the capacitance density of the fabricated structure.

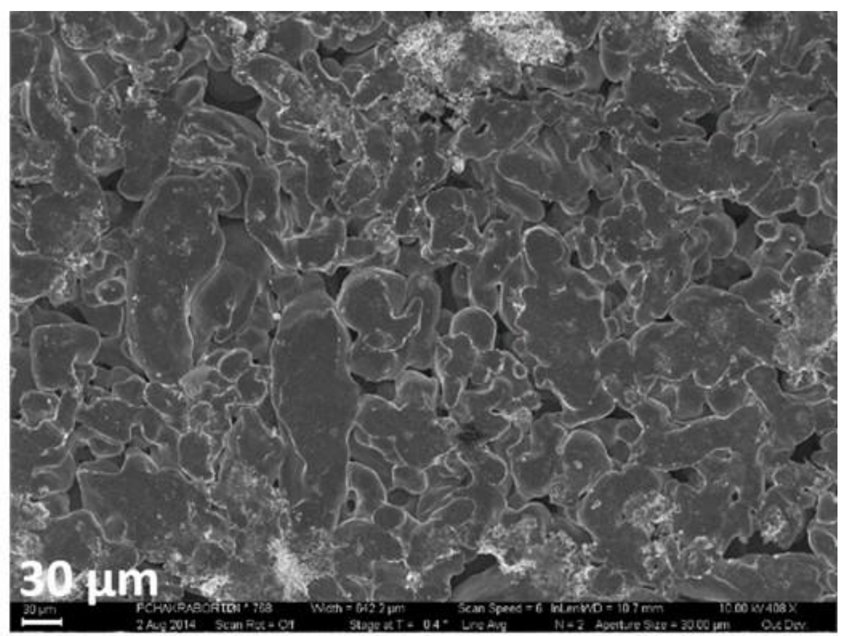


Figure 5.2: SEM micrograph of porous titanium electrode

The dielectric formation was carried out using anodization of planar and high-surface-area titanium anode under acidic conditions, as described earlier. Fig.5.3 shows the SEM micrograph (using in-lens detector) of a cross section of planar titanium anodized at 40V. The thickness of the planar anodized film at a formation voltage of 40 V was measured as 137.2 nm, corresponding to a rate of dielectric formation of 3.43 nm/V. Consequently, the permittivity of the anodized layer was estimated to be 37.59 [100, 102, 103]. The high-surface-area Ti anode was anodized using the same conditions as the ones for the planar Ti. Anodization kinetics do not change when the anodization conditions such as anodization electrolyte and their concentration, anodization time and voltage and temperature stay the same. However, in a sintered electrode system, the local field strength,

as well as the local ionic current density, could lead to different dielectric thickness for oxides at different depths of the electrode [68]. However, for the purpose of this study, the dielectric thickness was assumed to be the same for both the porous and the planar structures. Anodized titanium is known to yield porous oxide, which tends to render poor dielectric properties. Thicker titanium oxide were thus formed to reduce the dielectric porosity and defect density [69, 104].

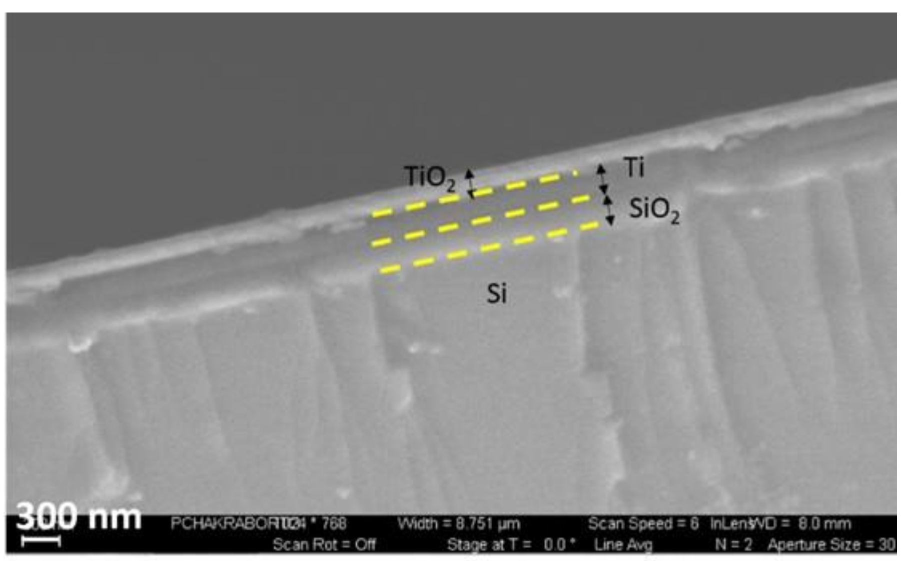


Figure 5.3: SEM micrograph of a cross section of planar anodized Ti

5.3.2 Chemical state characterization of the titania dielectric

The oxide distribution in the anodized dielectric was studied using surface sensitive XPS technique. The XPS scans were performed at different depths of the dielectric thickness. The scans were corrected for carbon peak electrostatic charging. The depth profile was carried out using Ar^+ (3 keV) ion bombardment. The sputtering rate of the titanium oxide was estimated to be 0.07 nm/min. The thickness of the anodized dielectric

was also estimated using the XPS depth profile and was found to be ~ 37 nm. It is important to note that the samples characterized using XPS were anodized with 8 V and estimated to have 34.3 nm thickness.

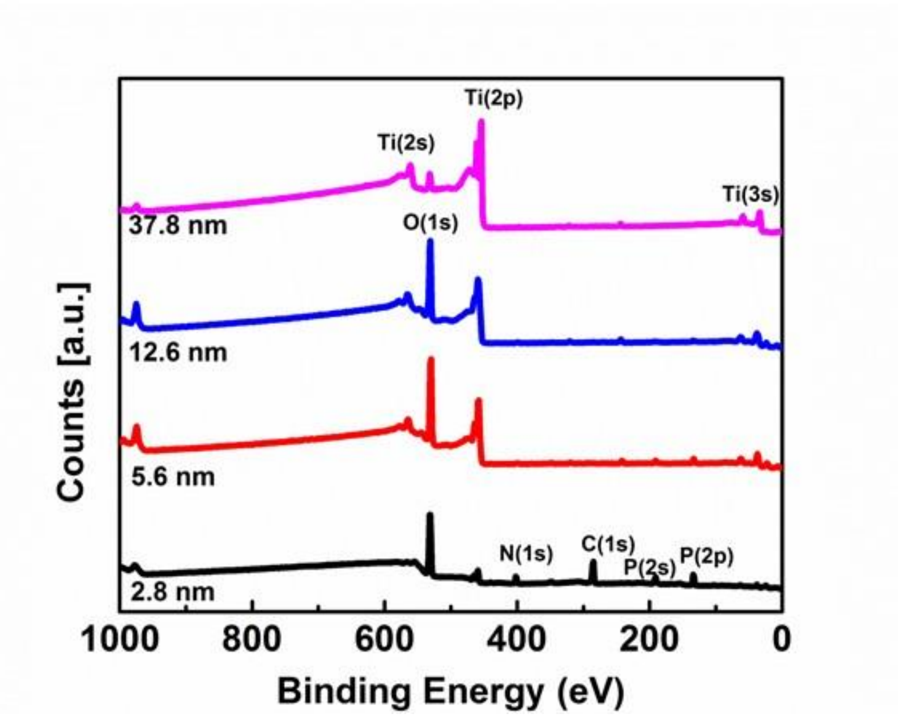


Figure 5.4: Survey scans of Ti at different etch depths

The survey scans of the TiO_2 film at three different depths are shown in Fig. 5.4. The evolution of Ti and decrease of oxygen peaks is clearly seen along the depth of the dielectric thickness. The presence of P in the initial layers of the dielectric is also evident from the scans. Incorporation of P in anodized films is known to occur with phosphoric acid as electrolyte [73]. It is also expected to yield lower ionic conductivity[105]. The phosphorus percentage reduces from 10% at the surface (etch depth of 2.8 nm) to an almost negligible amount at an etch depth of 12.6 nm. This differs from the phosphorus incorporation in Ta_2O_5 where the phosphorus concentration is same till halfway through

the film thickness. Beyond the halfway thickness no further phosphorous is observed in the case of tantalum [73]. The peak at 978 eV belongs to the Auger peak of oxygen.

Fig. 5.5 shows the core-level scans of Ti at different etch depths. Ti 4p core level scans appear as a doublet at 459 eV($4p_{1/2}$) and 465 eV ($4p_{3/2}$) that tend to shift to 454 and 460 eV respectively with increasing sputtering depth. The peak shifts to lower binding energies with the increasing etching depth, clearly show the evolution of Ti from higher oxidation states to purely metallic. The presence of a broad peak, instead of resolved Ti doublet at 16.8 nm (sputtered depth level), indicates the existence of different Ti sub-oxides, which later emerge as a clear doublet around 40 nm of sputtered depth.

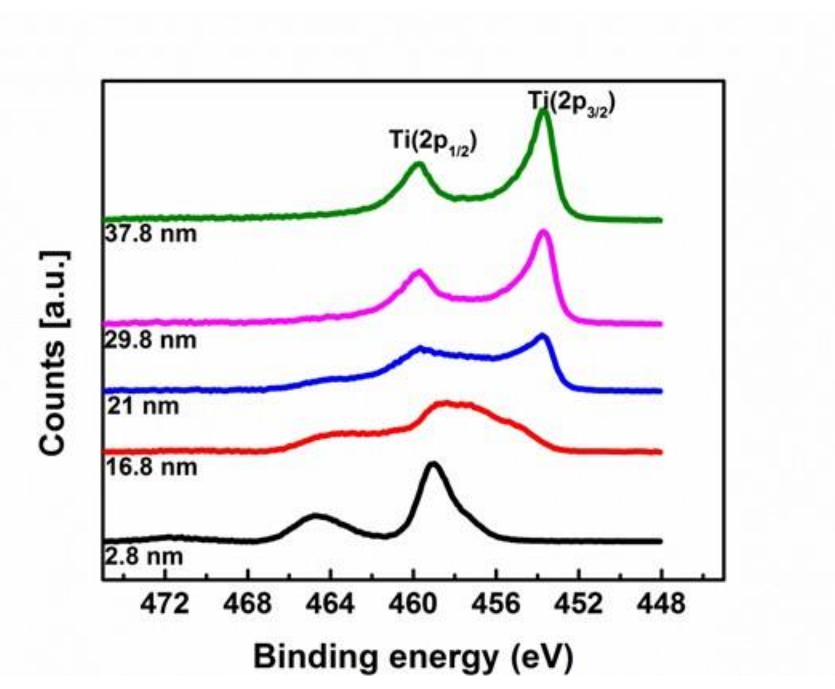


Figure 5.5: Ti Core level scans of TiO2 films at different etch depths

The Ti sub-oxides were elucidated by de-convoluting the acquired scans at each level with Gaussian components using standard FWHM and position from known valence states. The de-convoluted peaks at each level are shown in Fig. 5.6.

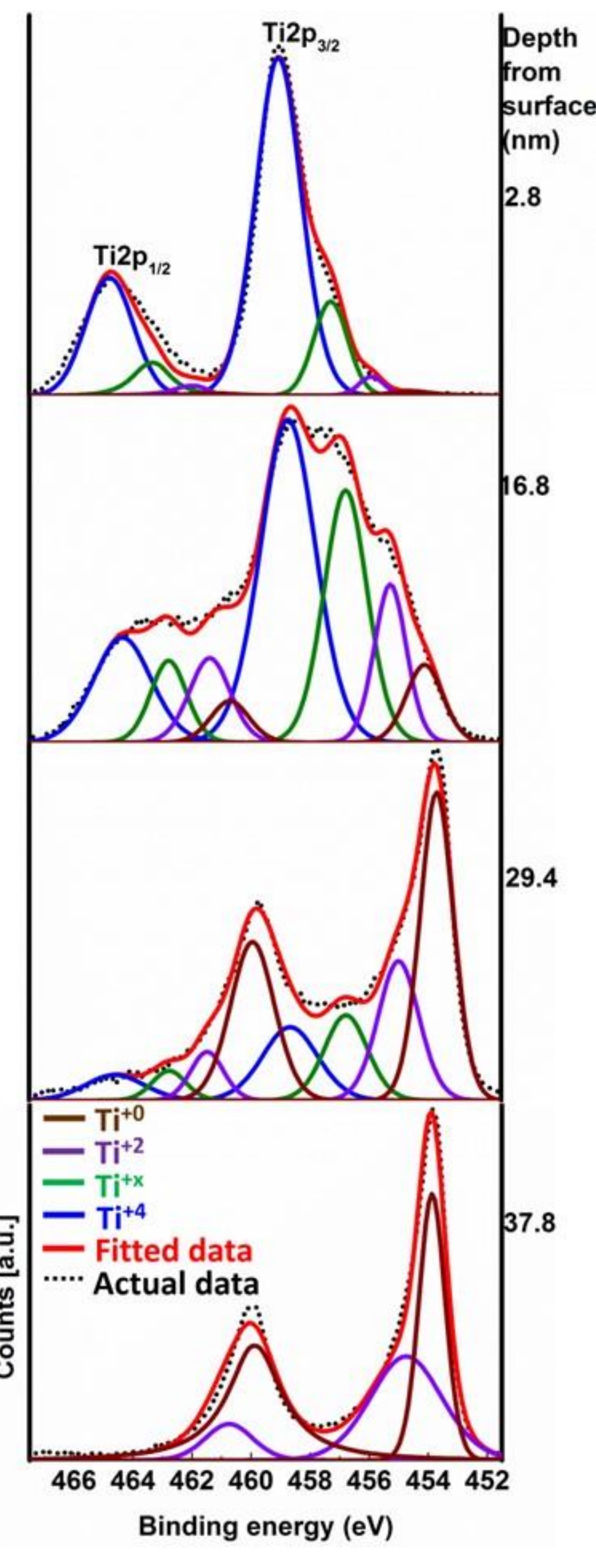


Figure 5.6: De-convoluted peaks of Ti showing Ti and its oxides at various etched depths

The surface of the TiO_2 was dominated by Ti (+4) state, which is also significantly present in the middle of the dielectric thickness (16 nm). The peak at binding energy 458.8 eV corresponds to Ti^{4+}. The de-convolution also demonstrates the presence of non-stoichiometric oxides of Ti (depicted as Ti^{x+}) at different depths of the oxide. A trace amount of Ti in oxidation state +2 can be seen near the surface, which rises as we again go down along the depth of TiO_2 film. The distribution of the oxides in the dielectric is summarized using a depth profile plot in Fig. 5.7 where the percentages of Ti in different oxidation states are plotted at different etch depths. It is interesting to note that the all the oxidation states are present in almost equal quantities around 20 nm depth, beyond which the oxide content drops to less than 0.1%. Thus, the Ti^{+4} oxide is primarily present at the surface of the anodized titanium film and a mix of oxides are observed at intermittent and lower depths. The emergence of non-stoichiometric oxides along with lower valence oxides such as Ti^{+2} indicate that the thermodynamics/kinetics or both of the dielectric formation changes along the anodized thickness.

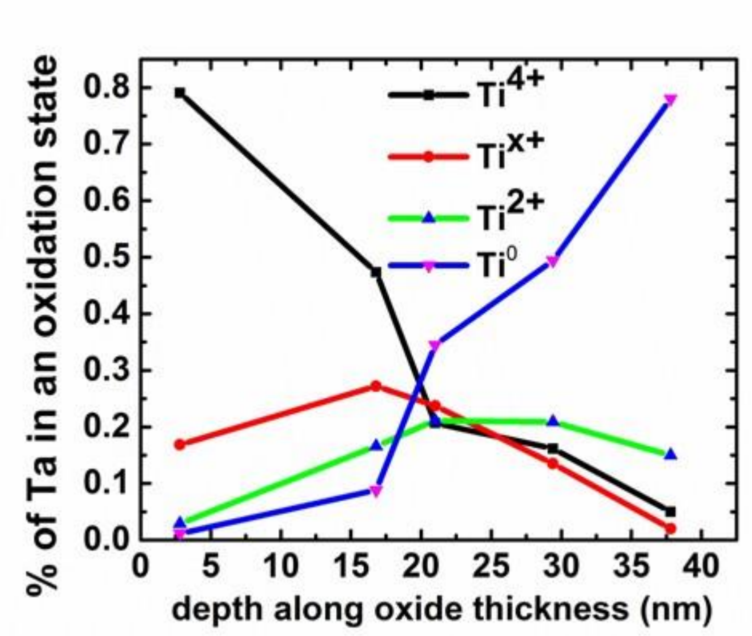


Figure 5.7: Depth profile of Ti in different oxidation states along dielectric thickness

Thermodynamically, Gibbs energy favors the reduction of titania when in contact with a metal (in this case Ti) as given by the equation (2).

$$Ti + TiO_2 \rightarrow TiO_x + TiO_{2-x} \text{------------------(2)}$$

This could explain the presence of sub-oxides near the metal/oxide interface.

Anodization kinetics of titanium predicts the formation of anodic film through the outward diffusion of the titanium cations and inward diffusion of oxide anions. Titania is known to exist in amorphous phase in the outer part of the anodic oxide film (at the oxide/electrolyte interface), which is further stabilized by the incorporation of electrolyte derived species such as phosphorous corroborated by our XPS study. This is accompanied

by the amorphous to crystalline phase transition yielding a crystalline titania layer underneath (at the oxide/metal) instances of which have been reported in the literature at anodization bias as low as 5V [53-56]. Oxide ions could migrate faster along the open channels of amorphous oxide structure while they diffuse along slower paths via vacancies [57]. Lower oxide mobility yields oxygen deficiency in those regions that manifest as non-stoichiometric oxides or titanium oxides with titanium in lower oxidation states. Conversely, higher oxide mobility would lead to Ti oxide with Ti in its highest oxidation states. The XPS data evinces the Ti^{4+} at the top of anodic oxide film while the non-stoichiometric oxides and Ti^{2+} are present underneath. With grain sizes, ca.1 nm, the porous crystalline phase heavily contributes to the leakage conduction in titania dielectric [53]. The above discussion, as well as the XPS study further, suggests that the amorphous titania comprises of stoichiometric oxides whereas crystalline titania yields non-stoichiometric oxides.

Valence band spectra of TiO_2 at different etch depths is shown in Fig. 5.8. The presence of poorly formed Fermi level at the surface is typical for a dielectric and is clearly seen at etch depth of 2.8 nm in Fig. 5.8. This shows that the surface is dominant with insulating titanium oxide layer. As the etch depth increases the Fermi level gets more pronounced due to higher carrier density at the Fermi level. This is possible only when the valence band is above the Fermi level, which indicates the presence of Ti metal at etch depths of 37 nm. Hence, XPS core level and valence band results corroborate each other with a dielectric thickness of 37 nm. Valence band states in between the titanium oxide and Ti metal represent a contribution of different Ti sub-oxides dominant at different etch levels. Valence band spectra could be used to glean information on the band-gap of the

oxide. The binding energy axis intercept of the tangent drawn at the inflection point of the valence band spectra is a function of the band gap. The binding energy intercept diminishes away near the Ti/TiO_2 interface (the intercept with the binding energy axis is negative). A negative intercept is observed for the valence spectra at etch depth of 37.8 nm, which could be ascribed to the presence of valence band near or above the Fermi Level. This indicates the presence of metallic Ti near the Ti/TiO_2 interface, which is consistent with the observations mentioned from the analyses above.

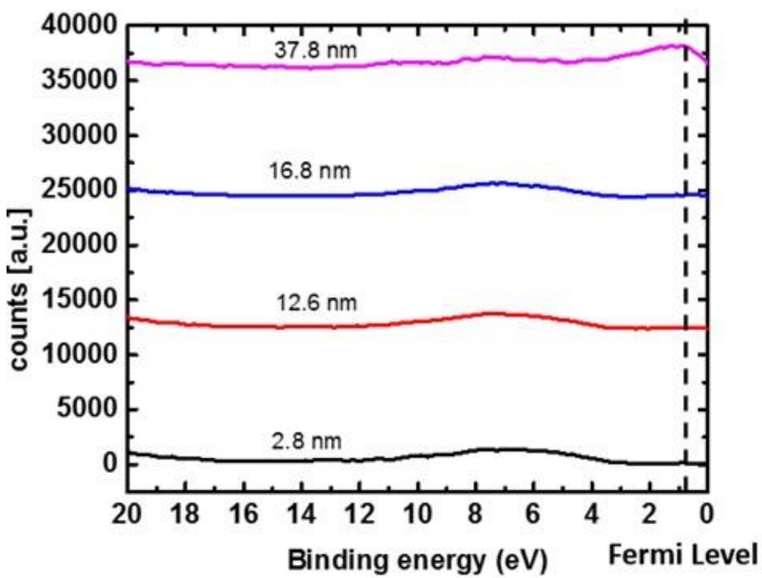


Figure 5.8: Valence band of Ti oxides at near surface and near the Ti–TiO_2 interface

Cathode infiltration inside the high-surface-area anodized electrode:

The infiltration of the conducting polymer inside the porous regions of the anodized Ti anode was validated by performing an EDS at the very bottom of the porous Ti. The presence of carbon and sulphur, which form the PEDOT backbone chain, at a depth of 125 microns from the top surface of the Ti electrode confirmed the penetration of

conducting polymer. Strong oxygen signals obtained from the same region could be attributed to both the titania film and the conducting polymer counter electrode.

5.3.3 Electrical Characterization:

The electrical characterization for the planar and high-density capacitors are described in the subsequent sub-sections.

5.3.3.1 Planar thin-film capacitors:

The capacitance density for planar films registered a decrease from 0.97 μF cm^{-2} to 0.43 μF cm^{-2} as the formation voltage was increased from 10V to 40V. This dip in capacitance density stems from thicker dielectric formed at higher anodization voltages, which reduces the capacitance. However, the dielectric quality improves with thicker dielectrics. Fig. 5.9 shows the normalized I-V plot for capacitors (with metal as a top electrode) with formation voltages of 10 and 40 V. As can be seen from the figure, the thicker dielectric showed lower leakage current at a higher voltage as compared to thinner dielectric because of the relatively lower defect density.

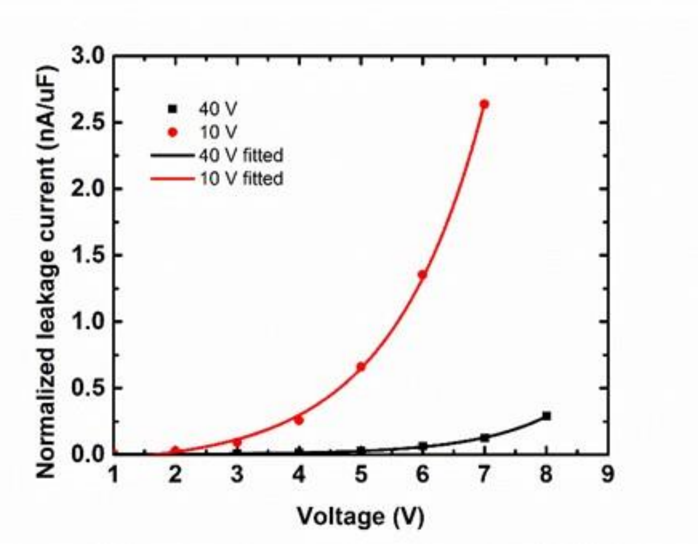


Figure 5.9: I–V curve for planar titanium capacitor

The presence of thicker dielectric reduces the leakage current from 146 nA nF^{-1} to 11 nA nF^{-1} as the formation voltage was raised from 10 to 40 V. Thinner dielectrics as compared to thicker ones are more prone to pin-holes and other defects, leading to much higher leakage current.

The defect mechanisms in the formed dielectric at 10 and 40V were analyzed using five known classical leakage mechanisms – Schottky effect, Poole- Frenkel effect, Ion Hopping mechanism, Space Charge Limited Conduction (SCLC) and Fordheim-Nordler-Tunneling (FNT) mechanism.

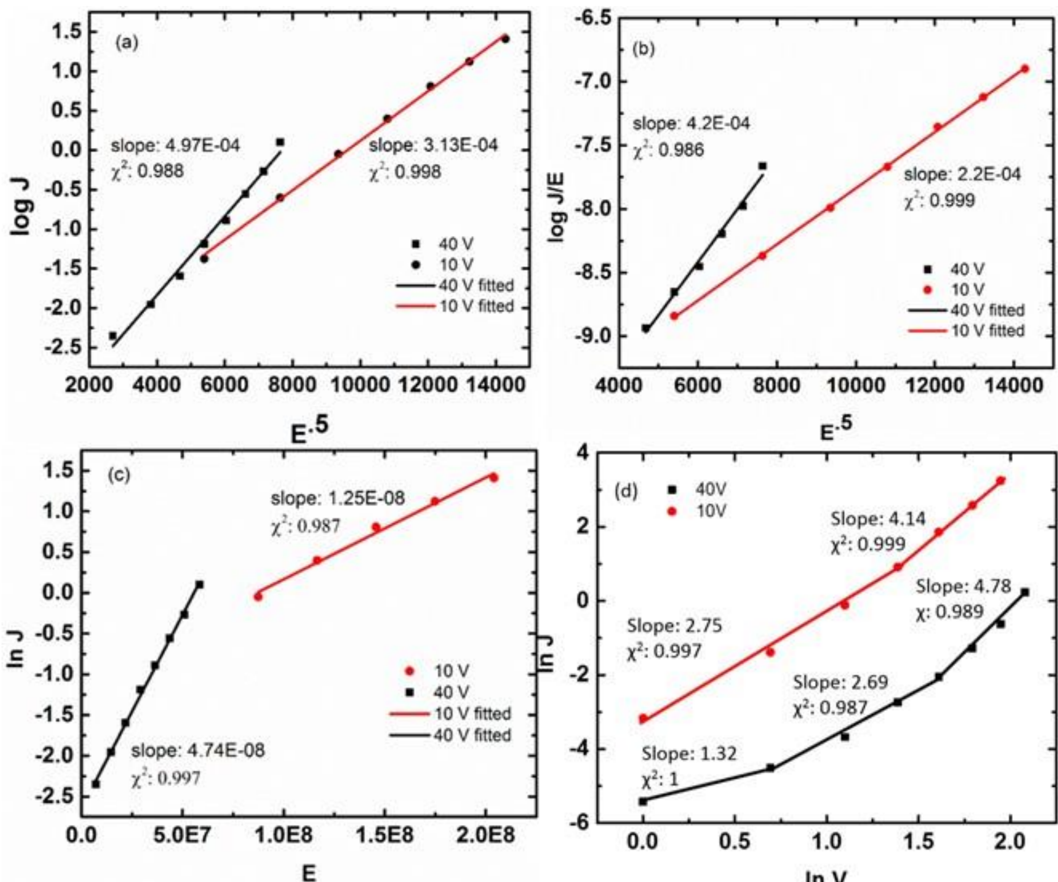


Figure 5.10: Defect mechanism (a) Schottky effect (b) Poole-Frenkel effect (c) Ion hopping (d) SCLC mechanism of planar titanium dielectrics

Schottky conduction mechanism corresponds to the lowering of energy barrier due to thermal excitation of electrons across the metal-dielectric interface [51]. The leakage current flow attributed to Schottky mechanism [75] is given by

$$\ln(J_s) = \frac{1}{2KT}\beta\sqrt{E} + \left[\ln\left(A^*T^2\right) - \frac{q\phi_s}{KT}\right]$$

where, J_s is the current density, E is the electric field, A^* is the Richardson constant, T: absolute temperature, Φ_s is the barrier height, K is the Boltzmann's constant, β is a material constant given by

$$\beta = \sqrt{\frac{q^3}{\Pi \varepsilon \varepsilon_o}}$$

where, ε: relative permittivity at high frequency (optical dielectric constant), ε_o: permittivity in vacuum and q: elementary charge. The optical dielectric constant is used for the sake of calculation since the dielectric relaxation time is slower than the electron residence time in the dielectric [74]. Defects in the titania dielectric would be dominated by Schottky electronic conduction mechanism if the plot of ln(Js) vs √E is linear with a slope close to 5.5E-04 assuming an optical dielectric constant of 7.29 [76]. In Fig. 5.10a, the experimental data for both 10V and 40V anodized dielectric fits the characteristic Schottky plots quite well. However, the slopes for both thinner (3.3E-04) and thicker (4.97E-04) dielectrics register a mismatch compared to the theoretically calculated slope of 5.5E-04. Hence, it can be inferred that none of the dielectrics exhibit Schottky conduction mechanisms. This can be supported by the band diagram near the Ti-TiO_2 interface (Fig-5.11) where the electrons in the Ti metal on contact between the metal and the oxide layer would lower their energy by transporting from conduction band of the metal to the conduction band of the oxide and vice versa, thus, yielding an Ohmic contact and no Schottky barrier [106, 107].

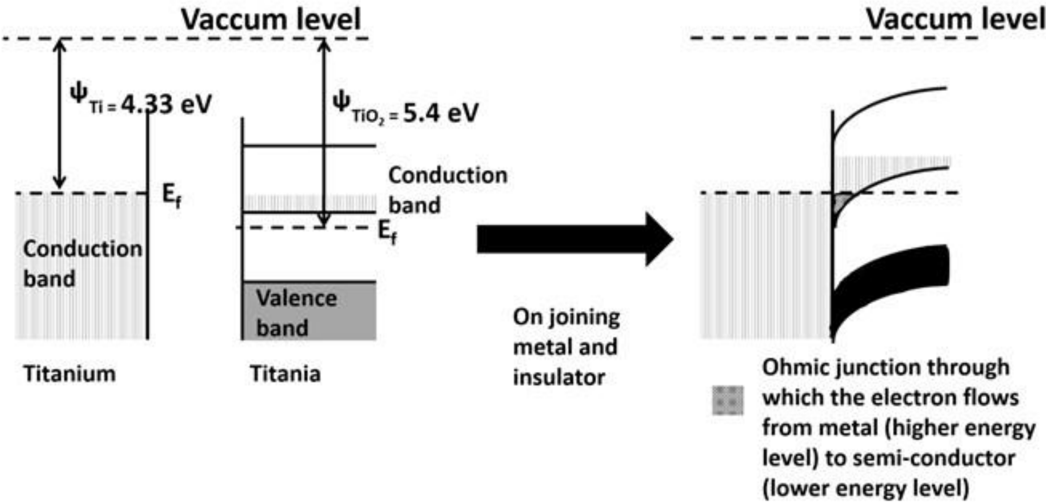


Figure 5.11: Schematic of band diagram depicting the Ohmic contact between the Ti and TiO_2

For further understanding the leakage current origin, Poole-Frenkel mechanism was analyzed, that involves electron hopping from a trapped site in the dielectric (created by an ion vacancy) into its conduction band of the dielectric under applied electric field [74]. Leakage current attributed to Frenkel-Poole Mechanism [75] is given by

$$\ln \frac{J_{PF}}{E} = \frac{\beta}{\zeta KT}\sqrt{E} + \left[\ln(C) - \frac{q\phi_s}{\zeta kt}\right]$$

Here, J_{PF} is the current density, C is a proportionality constant and ζ can take a value between 1 and 2 and is a function of the acceptor compensation in the material. Frenkel-Poole effects dominate the defects in dielectric if the plot of ln (J_{PF}/E) vs √E is a straight line and the value of ζ falls between 1 and 2. In Fig. 5.10b, the value of ζ for the thinner dielectric is 5.4 while the ζ value for the thicker dielectric is 2.6, both of which falls outside the theoretical range of calculated values of ζ. Hence, Poole Frenkel conduction as a

leakage mechanism could not account as the dominant mechanism for the leakage current in the titania dielectric.

Ionic conduction as a defect mechanism could be attributed to the hopping of vacancies such as oxygen vacancies/interstitials and titanium ion/interstitials vacancies within the dielectric [108]. The current attributed to ion hopping [74] is given by

$$\ln(J) = \frac{qa}{KT}E + \left[\ln(qan\nu) - \frac{E_a}{KT}\right]$$

where a = mean hopping distance of the ions, n = electron concentration in the conduction band, υ = frequency of thermal vibration of electrons at the trapped sites and E_a = activation energy for the electrons to jump from the trap states to the conduction band. Ion hopping defects would be present in the dielectric if the slope of ln(J) vs E is a straight line with a slope close to 1.58E-08 assuming mean hopping distance of 4 Å (based on interatomic distance). In Fig. 5.10c, the slope for thinner dielectric (1.25E-08) comes close to the theoretically calculated slope of 1.58E-08 while the thicker dielectric (4.74E-08) lies far away from the theoretical value. Since, lower anodization voltage yield thinner dielectrics, application of bias leads to higher electric field experienced by the trapped ions such as oxygen and titanium vacancies or oxygen and titanium interstitials. Thus, it is easier for the oppositely charged species to migrate to the oppositely charged electrodes leaving behind oppositely charged vacancies. These are also known as Schottky ionization defects [109] (not to be confused as the cause for Schottky electronic conduction mechanism discussed earlier). For example, a Schottky effect in a TiO_2 lattice can be characterized by

the creation of titanium and oxygen vacancies represented by V_{Ti}^{-4} and V_o^{+2} respectively) in equation (3).

$$TiO_{2\,Lattice} \Leftrightarrow V_{Ti}^{-4} + 2V_o^{+2} \text{---------------------------(3)}$$

In addition, a trapped ion in a dielectric would experience electric field when placed under an electric bias and will have enough energy to relocate by leaving its lattice point, thereby forming a vacancy) and occupying an interstitial also known as Frenkel defects [109]. Frenkel defects in a TiO_2 lattice could be explained in terms of oxygen vacancy and oxygen interstitials or titanium vacancy and titanium interstitial represented by V_o^{+2} and O_i^{-2} or V_{Ti}^{-4} and Ti_i^{+4} as given in equations (4) and (5) respectively.

$$O_{Lattice} \Leftrightarrow O_i^{-2} + V_o^{+2} \text{-----------------------------------(4)}$$

$$Ti_{Lattice} \Leftrightarrow Ti_i^{+4} + V_{Ti}^{-4} \text{-----------------------------------(5)}$$

Presence of ionic conduction in the thinner dielectric was also corroborated by the variation of leakage current with time (not shown here), which could be attributed to the migration of vacancies [31] For thinner dielectrics, leakage current reduces by about 40%, which indicates the presence of ionic conduction; for thicker dielectrics, the leakage current showed a stable behavior with time.

Nerstian behavior is primarily observed in nano-crystalline TiO_2, which leads to proton conduction. The nano-crystalline TiO_2 in anatase form can adsorb water from the air which enhances the proton conductivity in a wet atmosphere [110]. The system described in our study has a formed dielectric with an amorphous phase on the top and the

crystalline phase underneath. Hence, the possibility of proton conductivity was not considered. However during the process of titania formation, it is possible for the crystalline oxide (below the amorphous phase) in the dielectric to have trapped oxo and hydroxo groups, which would witness proton conduction [111].

SCLC is an electronic conduction mechanism, which is observed when an electrode makes Ohmic contact with the dielectric, leading to electron transport from the electrode to the dielectric, which subsequently migrate under an electric field induced space charge[74]. Dielectrics with SCLC mechanism yield a power law relationship between J and voltage (V), with different slopes at different voltage [74, 78]. In Fig. 5.10d, the slope for thinner dielectric (10V anodized sample) plot is a straight line with a slope of 2.75 till 3V, thereafter the slope changes to 4.14 for the current densities between 4 and 7V. For the thicker dielectric (formed at 40V), the log J-log V plot displayed a slope of 1.32 till 2V suggesting near-Ohmic contact between electrode and dielectric. (On the contrary, the thinner dielectrics display Ohmic behavior at voltages lower than 1V.) The slope for the thicker dielectric swelled to c.a. 2.69 for the region between 2 and 5V while the slope was found to be 4.78 between 5V and 8V. The different slopes at different voltages closely follow with the characteristics of SCLC mechanism mentioned in [77].

FNT conduction mechanism corresponds to the tunneling of electrons through the potential barrier into the conduction band of the dielectric even though the energy of the incident electron is less than the potential barrier. FNT conduction dominates when a plot of ln(J) vs 1/E is a straight line. FNT is usually observed at very high applied electric field

or with dielectrics thinner than 10 nm. Since the dielectric thickness in this study is much greater than 10 nm, FNT mechanism would not hold true [74].

In summary, the thinner dielectrics showed a combination of ionic and trap-enhanced SCLC, while thicker dielectrics showed Schottky conduction. However, it is highly likely that multiple conduction mechanisms co-exist.

5.3.3.2 High-surface-area capacitors

A capacitance density of 39 μFcm^{-2} was measured using liquid cathodes. The liquid electrolyte penetrates the porous electrodes and accesses the total surface-area, resulting in a maximum capacitance density. The inability of the polymers to reach all the crevices in the porous network renders lower capacitance density. The fabricated capacitor devices with PEDOT-PSS yielded a capacitance density of 7.15 μFcm^{-2}, which corresponds to a surface-area enhancement of 7.5X for the high-surface-area titanium anode as compared to planar titanium devices (shown in Table – 5.2). The area enhancement is estimated based on an oxide thickness of 34.3 nm for planar samples for the 10V anodization.

Table 5.2: Area enhancement using porous Ti v planar Ti

	Planar thin-film	Porous thick-film
Cap Density (μF/cm^2)	0.97	39 (Liquid) 7.15 (PEDOT-PSS)
Area enhancement (X)	1	40 (Liquid) ~7.5 (PEDOT-PSS)

The capacitance density can be further improved by modifying the bottom electrode structure to give higher surface-area with open pores and higher porosity. The capacitance density would also increase with better infiltration of conducting polymers into the porous structure. The leakage current of the high-surface-area capacitor, as shown in Fig. 5.12 was found to be higher than those measured with aluminum based capacitors [51, 112]. The results corroborate with the high leakage in titania reported earlier by Burns [113] and Tanvir et. al. [100]. Presence of defects such as thinner dielectric spots, lower interfacial barrier because of lower work function of Ti electrodes leading to Schottky conduction, lattice defects such as Schottky and Frenkel defects (described earlier) causing ionic conduction, trap-enhanced SCLC, and pin-holes in anodized oxide films could be attributed to the high leakage current in the titania film. The conformal nature of dielectric formed by anodization could also lead to higher built-in stresses in the dielectric in a high-surface-area titanium capacitor. The stresses could lead to subsequent cracks in the dielectric during capacitor operation at higher voltages. This could account for the high leakage current in

the high-surface-area capacitor as compared to the planar titanium capacitors. Further improvement in the anodization conditions and cathode processing to invoke self-healing can lower the leakage currents.

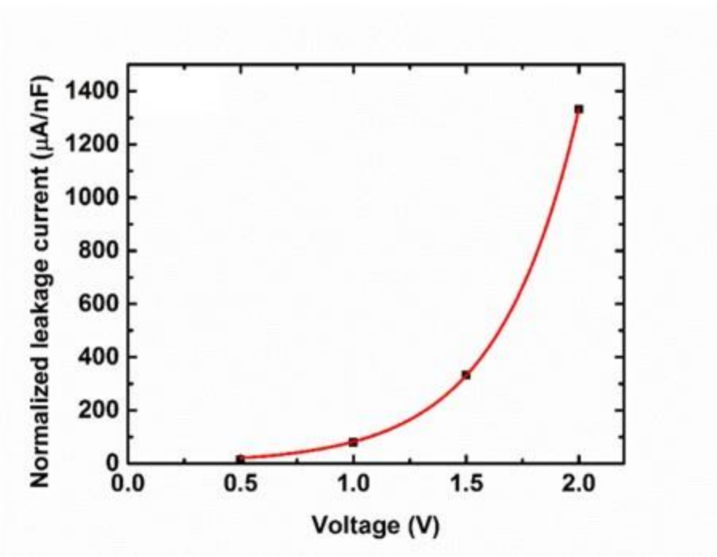


Figure 5.12: I–V characterization for porous titanium capacitor

5.4 Conclusions

This chapter describes new materials and structures to enhance the capacitance density by advancing all the three parameters that affect the capacitance: surface-area, permittivity and thinness of dielectric. An initial proof-of-concept was demonstrated with porous titanium electrodes. The porous titanium capacitors were benchmarked with planar titanium capacitors.

The fabricated capacitor showed 7.15 μF cm^{-2} at 100 kHz. which corresponded to 7.5X enhancement in surface-area compared to planar thin-film capacitors. This is the first

demonstration of high-density capacitors using high-surface-area titanium anodes along with high permittivity and thin-film titania as the dielectric. A leakage current of 10 nA nF^{-1} was achieved with higher anodization voltages for planar titanium capacitors while retaining a planar capacitance density of 0.44 μF cm^{-2}. Various leakage conduction mechanisms were analyzed using different models to account for difference in leakage currents in thinner and thicker dielectrics. The thinner dielectrics showed a combination of ionic and trap-enhanced SCLC, while thicker dielectrics showed Schottky. XPS depth profile and valence band spectra confirmed the presence of Ti oxide as Ti(+4) near the surface while mixed oxides were observed at intermittent depths, which contributes to the poor dielectric properties. Capacitance density of 7.15 μF cm^{-2} and 7.5X area enhancement over planar foils was achieved with solid cathodes. More process optimization is required with solid cathodes to yield higher capacitance and lower leakage currents.

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Chapter-6

SUMMARY AND OUTLOOK

6.1 Research Summary

Emerging smart systems, with their multitude of functionalities, require a large number of power modules to convert the battery voltage to the desired voltage and current for a particular application. The performance and size of these power modules are limited by the thick surface mounted passives such as capacitors and inductors, impeding the path to system miniaturization. The critical parameters governing the performance of power-supply capacitors are their capacitance density, operating frequency, and leakage properties. These properties are governed by the electrode area per unit volume, quality of the grown dielectric film and the net resistance from the electrodes. Fabrication of ultra-miniaturized capacitors is also limited by the geometry and processing of high surface area electrodes with low-cost substrate-compatible processes.

This study uses an innovative approach to achieve high capacitance density and low leakage currents with ultra-thin capacitors. The first part of the study investigates the processing of high-density tantalum capacitors in ultrathin form-factors at high frequencies with low leakage properties. The anodes were stencil printed on an ultrathin carrier foil with the stencil thickness defining the anode thickness. Different anode particle sizes were used to optimize the cathode impregnation inside the porous architectures and ensure lower ESR and higher operating frequencies. Different dielectric thickness was studied to optimize the leakage properties of the capacitor. The capacitors with low profiles of 50 µm

or lesser demonstrated capacitance densities ~0.2 μF/mm^2 at 1-10 MHz, which is 6X more than the capacitance densities of the commercial capacitors in the afore-mentioned frequency range at 20X thinner form-factors. Furthermore, the capacitors showed leakage of less than 0.01 μA/μF at 3V, which is equivalent to the leakage properties demonstrated by the commercial capacitors. The power capacitors developed in the study are expected to significantly reduce the number and the occupied area of such power capacitors. Furthermore, the thin form-factor of the developed power capacitors will help reduce the overall thickness profile of the power module enabling miniaturization.

The second part of the study demonstrates the integration of the above-mentioned in the silicon substrates. The integration steps involved lamination of the capacitors using build-up polymer dielectrics followed planarization with the same build-up dielectric,and via-drilling to separately access the anode and cathode. This was followed by electroless copper deposition to form seed-layer followed by semi-additive copper plating, photo-resist stripping and finally seed-layer stripping. The study enables seamless integration of the above-mentioned power capacitors as embedded thin-film high-density power capacitors, thus, eliminating the real-estate associated with the surface mounted discretes.

The final part of the study investigates the feasibility of porous titanium-based high-density capacitors with high-surface-area and high-permittivity from the titania dielectric contributing to the high capacitance density. The study also investigates the dielectric properties of the anodized titanium. The study showed the presence of crystalline phase in

the lower layers of the grown anodized titanium, which was responsible for the high leakage current in the high-density titanium based capacitor system.

6.2 Future Work

The following guidelines are suggested for future research in this area:

Improve the operating frequency of the ultrathin power capacitor:

- The optimized cathode infiltration showed the presence of sulfur signals up to 15 μm deep inside the porous anode (Chapter-3). The anode thickness could be further reduced to below 15 μm to ensure complete filling of the pores, reduce the ESR and raise the operating frequency from the demonstrated 1-10 MHz to more than 100 MHz. The approach would involve some trade-off with the capacitance density which could be offset by using smaller particle sizes, which would generate higher surface-area and higher volumetric densities. Furthermore, the lower form-factors of less than 5 μm would eliminate the issue of insufficient impregnation at deeper depths from the anode surface.
- The operating frequency could be improved by further optimizing the cathode impregnation process. This includes the number of dips, dwell of the anodized samples inside the conductor polymer solution and the duration of annealing. Approaches involving a higher number of dips and the larger dwell inside the conducting polymer could be explored.
- The conducting polymer should be replaced with metal to further lower the ESR and increase the operating frequency.

Integration of the power capacitors onto silicon substrates:

Different steps in the integration process could be further optimized.

- **Hermetic encapsulation:** The process needs to be modified to incorporate a hermetic layer that protects the cathodes.

- **Copper electroplating**: The current plating process leads to large electro-plating times and incomplete filling of the vias. The process can optimized by building the right sample holder frame to ensure optimum current density and smaller plating times.

APPENDIX-A

An electrolyte in contact with a metal generates an additional capacitance from the separation of electronic and ionic charges at the metal-electrolyte interface, usually referred to as an electrochemical double layer. In order to understand the dielectric contribution to the capacitance in the presence of an electrochemical double layer, a schematic illustration of the interfaces involved in the capacitor system is shown in Fig. A1. The contribution of charge accumulation at the electrolyte-dielectric interface is nullified when a much lower permittivity dielectric is attached to the electrochemical double layer in series. The phenomenon is represented through a mathematical expression shown as Equation 2.

D1 = Dielectric from the oxide layer

C1 = capacitance from the oxide layer

D2 = Dielectric from the double layer

C2 = capacitance from the double layer

Here, C's are calculated using the standard equation,

$$C = \frac{A\varepsilon\varepsilon_r}{t} \quad (1)$$

where,

A = Surface area of the electrode

ε = Permittivity in vacuum

ε_r = Relative permittivity of the dielectric

t = thickness of the dielectric

Here, $\varepsilon_{r(D1)} << \varepsilon_{r(D2)} => C_1 << C_2$

C_1 and C_2 are in series, so

$$C_{eff} = \frac{(C_1 \times C_2)}{(C_1 + C_2)} \cong C_1 \quad (2)$$

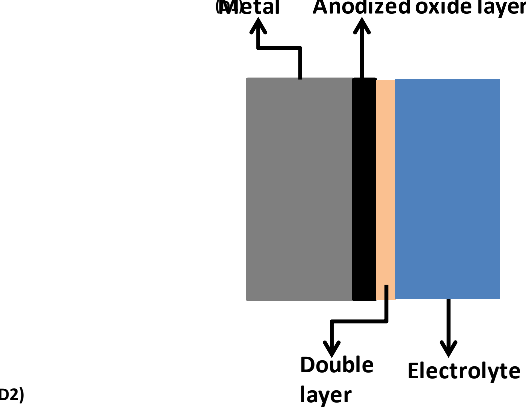

Fig. A1: *Illustration representing the two dielectrics in the wet-system (metal oxide and electrochemical double layer)*

As derived above, it can be seen that when two capacitors are attached in series with different values, the effective capacitance is closer to the smallest capacitor. In this case where the capacitance from the dielectric is much less than that of the electrochemical double layer, the measured capacitance is predominantly from the dielectric.

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