Solid-state Memory on Flexible Silicon for Future Electronic Applications

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ABSTRACT

Solid-state Memory on Flexible Silicon for Future Electronic Applications

Mohamed Tarek Ghoneim

Advancements in electronics research triggered a vision of a more connected world, touching new unprecedented fields to improve the quality of our lives. This vision has been fueled by electronic giants showcasing flexible displays for the first time in consumer electronics symposiums. Since then, the scientific and research communities partook on exploring possibilities for making flexible electronics. Decades of research have revealed many routes to flexible electronics, lots of opportunities and challenges. In this work, we focus on our contributions towards realizing a complimentary approach to flexible inorganic high performance electronic memories on silicon. This approach provides a straight forward method for capitalizing on the existing well-established semiconductor infrastructure, standard processes and procedures, and collective knowledge. Ultimately, we focus on understanding the reliability and functionality anomalies in flexible electronics and flexible solid state memory built using the flexible silicon platform. The results of the presented studies show that: (i) flexible devices fabricated using etch-protect-release approach (with trenches included in the active area) exhibit ~19% lower safe operating voltage compared to their bulk counterparts, (ii) they can withstand prolonged bending duration (static stress) but are prone to failure under dynamic stress as in repeated bending and re-flattening, (iii) flexible 3D FinFETs exhibit ~10% variation in key properties when exposed to out-of-plane bending stress and out-of-plane stress does not resemble the well-studied in-plane stress used in strain engineering,

(iv) resistive memories can be achieved on flexible silicon and their basic resistive property is preserved but other memory functionalities (retention, endurance, speed, memory window) requires further investigations, (v) flexible silicon based PZT ferroelectric capacitors exhibit record polarization, capacitance, and endurance (1 billion write-erase cycles) values for flexible FeRAMs, uncompromised retention ability under varying dynamic stress, and a minimum bending radius of 5 mm, and (vi) the combined effect of 225 °C, 260 MPa tensile stress, 55% humidity under ambient conditions (21% oxygen), led to 48% reduction in switching coercive fields, 45% reduction in remnant polarization, an expected increase of 22% in relative permittivity and normalized capacitance, and reduced memory window (20% difference between switching and non-switching currents at 225 °C).

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LIST OF ABBREVIATIONS

IoT	Internet of Things
IoE	Internet of Everything
SS	Subthreshold Swing
NVM	Nonvolatile Memory
RAM	Random Access Memory
ReRAM	Resistive Memory
FeRAM	Ferroelectric Memory
PCRAM	Phase Change Memory
MRAM	Magnetic Memory
AFM	Atomic Force Microscopy
NEM	Nanoelectromechnical
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
FET	Field Effect Transistor
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
TANOS	Tantalum Nitride-Alumina-Nitride-Oxide-Silicon
1T	One Transistor
1T1R	One Transistor-One Resistor
1T1C	One Transistor-One Capacitor
2T2C	Two Transistors-Two Capacitors
SOI	Silicon on Insulator
SSD	Solid State Drive
ULSI	Ultra Large Scale Integration
CNTs	Carbon Nanotubes
ZnO	Zinc Oxide
GI-XRD	Grazing Incidence X-Ray Diffraction
OLED	Organic Light Emitting Diode
CES	Consumer Electronics Show
M2M	Machine to Machine
PP-SSS	Privacy Protection Solid State Storage
PVDF-TrFE	Poly[vinylidenefluoride-co-trifluoroethylene]
FOX	Field Oxide
ITRS	International Technology Roadmap for Semiconductors
CMOS	Complementary Metal-Oxide-Semiconductor
MOSCAP	Metal-Oxide-Semiconductor Capacitor
Vramp	Ramping Voltage
TDDB	Time Dependent Dielectric Breakdown
DIBL	Drain Induced Barrier Lowering
ILD	Interlayer Dielectric
Dit	Interfacial Defects Density
BOX	Buffered Oxide
CVS	Constant Voltage Stress
PZT	Lead Zirconium Titanate
FG	Floating Gate

CT	Charge Trap
QDs	Quantum Dots

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Chapter 1 Introduction and Review on Physically Flexible Nonvolatile Memory

Solid-state memory is an essential component of the digital age. With advancements in healthcare technology and the Internet of Things (IoT), the demand for ultra-dense, ultra-low-power memory is increasing. In this chapter, we present a comprehensive perspective on the most notable approaches to the fabrication of physically flexible memory devices. With the future goal of replacing traditional mechanical hard disks with solid-state storage devices, a fully flexible electronic system will need two basic devices: transistors and nonvolatile memory. Transistors are used for logic operations and gating memory arrays, while nonvolatile memory (NVM) devices are required for storing information in the main memory and cache storage. Since the highest density of transistors and storage structures is manifested in memories, the focus of this chapter is flexible NVM. Flexible NVM components are discussed in terms of their functionality, performance metrics, and reliability aspects, all of which are critical components for NVM technology to be part of mainstream consumer electronics, IoT, and advanced healthcare devices.

This Chapter briefly outlines the operating principles, common nonvolatile memory architectures of different NVM cells and technologies, and a literature review of the flexible NVM research area and highlights the most common approaches for making flexible NVM. The material presented is published as:

- Ghoneim, M.T.; Hussain, M.M. Review on Physically Flexible Nonvolatile Memory for Internet of Everything Electronics. *Electronics* **2015**, 4, 424-479.

Chapter 2 and 3 demonstrate the reliability studies of flexible high-κ/metal gate devices, including flexible MOSCAPs and flexible FinFETs on silicon. These chapters represent our contribution in showing the first key element in NVM cells which is the select/access transistor. We first study the electrical and mechanical reliability aspects of a flexible version of a simple metal-oxide-semiconductor structure then move forward to undertake the performance analysis of high performance flexible non-planar 3D FinFET CMOS. These two chapters are published as:

- Ghoneim, M.T.; Rojas, J.P.; Young, C.D.; Bersuker, G.; Hussain, M.M. Electrical Analysis of High Dielectric Constant Insulator and Metal Gate Metal Oxide Semiconductor Capacitors on Flexible Bulk Mono-Crystalline Silicon. *IEEE Trans. Rel.* 2015, 64, 579-585.
- Ghoneim, M.T.; Kutbee, A.; Nasseri, F.G.; Bersuker, G.; Hussain, M.M. Mechanical anomaly impact on metal-oxide-semiconductor capacitors on flexible silicon fabric. *Appl. Phys. Lett.* 2014, 104, 234104.
- Ghoneim, M.T.; Alfaraj, N.; Torres-Sevilla, G.A.; Fahad, H.M.; Hussain, M.M. Out-of-Plane Strain Effects on Physically Flexible FinFET CMOS. *IEEE Trans. Electron Devices*, 2016, 1-8.
- Torres-Sevilla, G.A.;* Ghoneim, M.T.;* Fahad, H.;* Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible nanoscale high-performance FinFETs. *ACS Nano* 2014, 8, 9850-9856. [* Equal Contributions]

Chapters 4 and 5 represent the second main component of NVM which is the storage elements. Chapter 4 demonstrates a flexible resistive memory device (memristor—storage element in ReRAM) on flexible silicon and chapter 5 demonstrates

flexible ferroelectric capacitors (storage element in FeRAM) on silicon. The presented work in these two chapters has been published as:

- Ghoneim, M.T.; Zidan, M.A.; Salama, K.N.; Hussain, M.M. Towards neuromorphic electronics: Memristors on foldable silicon fabric. *Microelectron. J.* 2014, 45, 1392-1395.
- Ghoneim, M.T.; Zidan, M.A.; Alnassar, M.Y.; Hanna, A.N.; Kosel, J.; Salama, K.N.; Hussain, M.M. Thin PZT-Based Ferroelectric Capacitors on Flexible Silicon for Nonvolatile Memory Applications. *Adv. Electron. Mater.* 2015, 1, 1500045.
- Ghoneim, M.T.; Hussain, M.M., 2015. Study of harsh environment operation of flexible ferroelectric memory integrated with PZT and silicon fabric. *Appl. Phys. Lett.* 2015, 107, 052904.

Finally, chapter 6 provides useful insights based on the learnt lessons from our research pursuits and outlines future directions towards achieving fully flexible NVM modules and systems for IoT and wearable electronic applications.

1.1. NVM Operating Principles

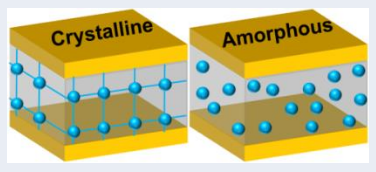
Similar to how we define the human brain's ability to memorize as the ability to remember useful information over long- and short-term durations, electronic memories have the ability to retain stored information over various durations. An electronic memory that is able to retain information over short periods of time (milliseconds) is identified as a volatile memory. In this case, when the power goes off, information stored in the volatile memory is lost. On the contrary, an electronic memory that is able to store information over long periods of time (~10 years is the industry standard) is called a

nonvolatile memory (NVM). NVMs can retain information even when no power is supplied. There are five major classes of NVMs [1]: resistive random access memory (ReRAM) also referred to as memristor [2-5], ferroelectric RAM (FeRAM), [6] magnetic RAM (MRAM) [7, 8], phase change RAM (PCRAM) [9, 10], and flash memory (floating gate (FG) and charge trapping (CT)) [11, 12, 13]. Other technologies, such as nano-electromechanical (NEM) NVMs [14, 15] and molecular based NVMs [16] exist but they are not mainstream. Table 1.1.1 summarizes the principles of operation of the leading NVM technologies and indicates which technologies have already been demonstrated in a flexible form. Note that the terms 'floating gate' and 'charge-trapping flash' are used interchangeably in recent literature. In Table 1.1.1, the distinguishing property is whether the charge-trapping layer is a conductor or an insulator, although both conducting and insulating layers (with or without embedded NPs and QDs) trap charges; nanoparticles (NP) embedded in an insulator for charge trapping are also considered FG-Flash.

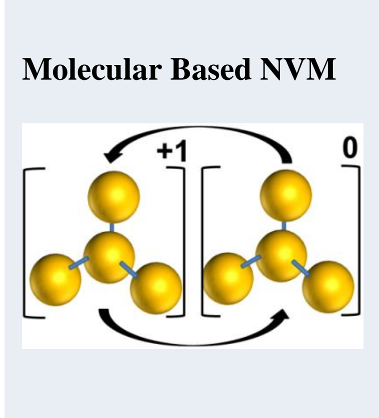
Table 1.1.1: Operation Principles of Common NVM

NVM Type	Operation Principle	Flexed
ReRAM (Memristor) Conductive Path	A resistive oxide is sandwiched between two metallic layers. The resistance of the oxide changes with applied "set" and "reset" voltage pulses. A high-resistance state corresponds to "0" and a low-resistance state corresponds to "1."	**Yes**

FeRAM	A ferroelectric material has two possible polarization states inherent from its crystalline structure. Applying write/erase voltage pulse switches for positive to negative polarization states, corresponding to “0” or “1.”	**Yes**
MRAM	Spintronic devices such as magnetic tunneling junctions are composed of a fixed (“pinned”) magnetic moment layer, a tunneling barrier (oxide), and a free layer. Current flowing in nearby lines is expected to magnetize the free layer. If the free layer magnetic moment is parallel to that of the pinned layer, the device is “ON” and the resistance across the structure is low. If the free layer is magnetized such that its magnetic moment is anti-parallel to the pinned layer, the device is “OFF” and the structure will be in high-resistance state.	**No**
PCRAM	Current or laser pulses are applied to change the phase of a material from crystalline (low	**Yes**

		resistance) to amorphous (high resistance) and vice versa at a localized space, which changes the material's electrical and optical properties. Short pulses above the melting temperature are needed to make the change from the crystalline to the amorphous phase, while longer pulses below the melting temperature are required to restore the crystalline order of the material.	
Flash	**FG**	FG flash has the same structure as a field effect transistor (FET) except that its gate dielectric is split into three layers. The first is tunneling oxide, the second is an embedded conductor layer (i.e., doped polysilicon or embedded quantum dots (QDs) or metallic nanoparticles (NPs)) floating gate, and the third is a blocking oxide. When a programming voltage is applied, carriers tunnel from the channel to the floating gate. This results in a shift of the threshold	**Yes**

		voltage of the transistor corresponding to “1.” A reverse bias is applied during the erase operation to move the charges back into the channel.	
	CT	The charge trap flash replaces the floating gate with a conductor layer that has an insulting layer (i.e., silicon nitride). The most common structures are the SONOS (Polysilicon-oxide-nitride-oxide-silicon) and the TANOS (titanium-alumina-nitride-oxide-silicon).	**Yes**
NEM-NVM	A nano-electromechanical switch is fabricated such that (i) upon applying a programming electrical signal, its pull-in voltage shifts when operated at a designed switching voltage or (ii) it has a free moving cantilever that has bistable physical states affecting its electrical properties.		**No**

Molecular Based NVM 	A bistable molecule can be switched from a low-conductance state (“0”) to a high-conductance state “1” by applying brief bias voltage pulses to switch the state through oxidation and translation of the molecular structure between the two stable states.	**No**

1.2. NVM Architectures

NVM architectures are an important element in memory design that can be classified into three main categories: the 1T, where the memory cell is composed of a single transistor (‘T’ stands for transistor); the 1T1C or 1T1R, where the memory cell is composed of an access/select transistor and a nonvolatile storage structure (‘C’ stands for capacitor and ‘R’ stands for resistor); and the 2T2C (two transistors and two capacitors per memory bit) [1, 17, 18]. Other variations of these main architectures [17, 19] and different arrangements, such as the 1T2C, have also been reported [20-22]. Furthermore, there are differences in the way memory cells are connected to each other. For instance, NOR-type flash and NAND-type flash memories both have a 1T architecture but different cell connections [23]. Also, there is the crossbars configuration in which each memory cell is connected to four neighboring cells [6]. Figure 1.2.1 shows the schematic arrangements of the three main architectures, NOR and NAND flash arrangements, and the crossbars configuration.

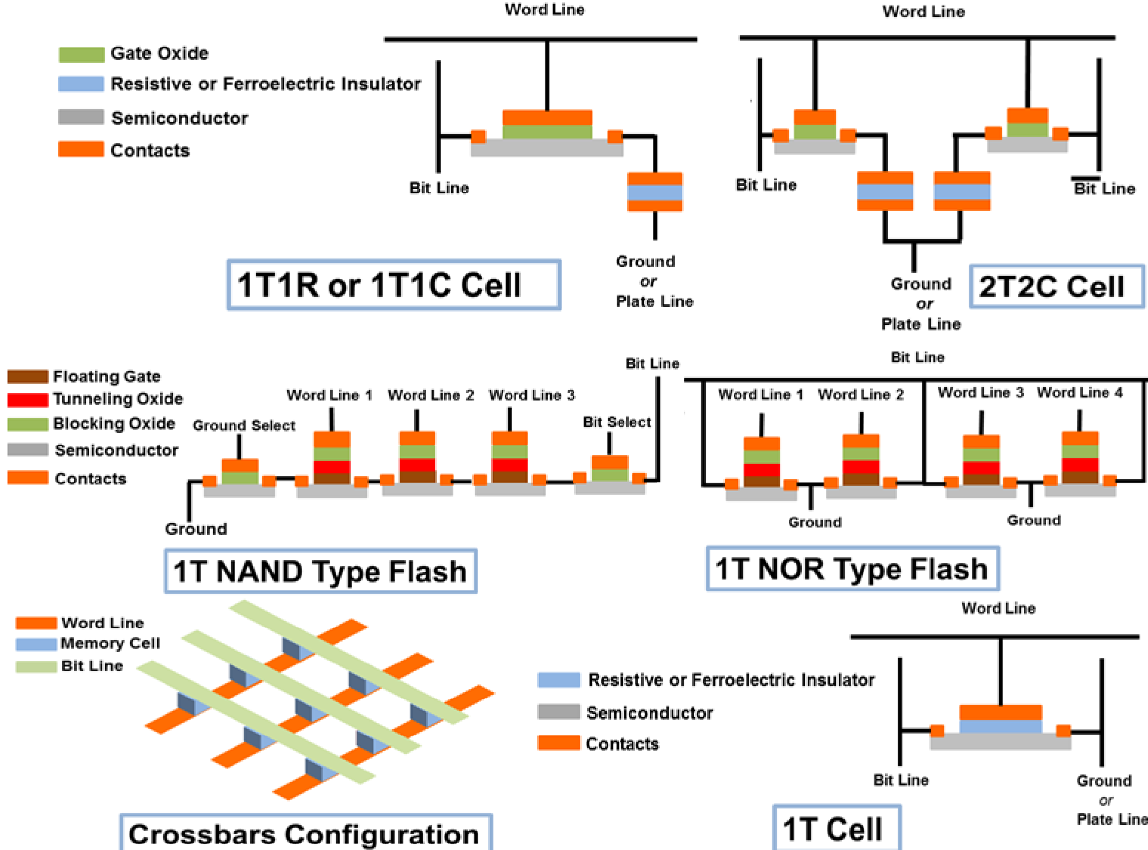


Figure 1.2.1: Architectures of NVM

1.3. Literature Review

Recent advancements in flexible electronics research will enable novel applications ranging from stylish flexible gadgets for real-time monitoring of health-related vital signs to novel biological applications such as electronic skin [23-33]. Critical advances have been made in recent years that rely on organic materials as active elements because of their inherent flexibility. Mainstream approaches to capitalize on naturally flexible substrates like polymers can be categorized into (i) all-organic systems, where both devices (specifically active materials) and substrates are made up of organic materials [34-40] or inkjet- and screen-printed in thin layers onto paper and organic

substrates [41-44] and (ii) hybrid systems, where inorganic electronic devices are transferred onto an organic substrate using transfer printing and other transfer techniques [45-53], laser lift-off transfer [54], and low-temperature direct deposition of inorganic devices on plastic organic substrates [55-58]. Other approaches use silicon-on-insulator (SOI) substrates, and controlled spalling technology to peel-off thin semiconductor layers [59-61]. In addition, a complementary transfer-free approach has recently been introduced, where thinning down the inorganic substrate through traditional, standard fabrication processes improves the flexibility of the substrate [62-67].

These approaches are all geared towards achieving fully flexible electronic systems. The three main components in any electronic system are (1) processing units, (2) the main memory, and (3) storage. Processing units perform logic operations through transistor logic, while the main memory performs temporary short-term storage (cache) with a quick access feature, also known as primary storage or random access memory (RAM), through access transistors and capacitors that store charges. Storage refers to the long-term retention of information, traditionally implemented using hard disks. However, at present, a shift towards other NVM types in a solid-state drive (SSD) format for supporting faster performance and higher integration densities within strict area constraints is taking place. Hence, the main electronic devices required to build an electronic system are transistors, capacitors, and NVM devices. Emerging NVM such as resistive random access memory (ReRAM), flash memory, phase change RAM (PCRAM), and ferroelectric random access memories (FeRAMs) have the benefits of fast switching, low-operation voltage, and ultra-large-scale-integration (ULSI) densities. These attractive qualities not only make them a favorable option for replacing magnetic

hard disks but also for replacing quick access, volatile, and dynamic RAM. This means that future electronic systems will require combinations of only two essential devices: transistors and NVM devices.

An objective assessment of the discussed mainstream and complementary approaches to flexible electronics must focus on their ability to provide high-performance, reliable NVM devices with ULSI density transistors. In this section, we present the mainstream NVM architectures and technologies with a special focus on most up-to-date techniques for producing flexible NVM devices.

Every memory cell consists of a gating device for access/select that is usually implemented using a transistor. Hence, memory arrays are where the largest number of transistors exist in an electronic system, a consequence of their ULSI density and low cost/bit ($/bit). Furthermore, with the continuous reduction in $/bit of NVMs and the higher switching speeds between memory states ('0' to '1' or vice versa) of emerging NVM technologies, replacing volatile random access memory and magnetic hard disks with faster SSDs made up of transistors and NVM structures becomes feasible. Here, the progress made over the past few years in three prominent types of flexible NVM technologies is discussed: (i) resistive, (ii) ferroelectric, (iii) phase change, and (iv) charge-trapping NVMs. In addition, the reliability aspects of the devices reported are discussed and an assessment for emerging technologies that provides useful insights towards their potential for commercialization is also provided. Figure 1.3.1 briefly positions the focus of this review in context of flexible electronics research.

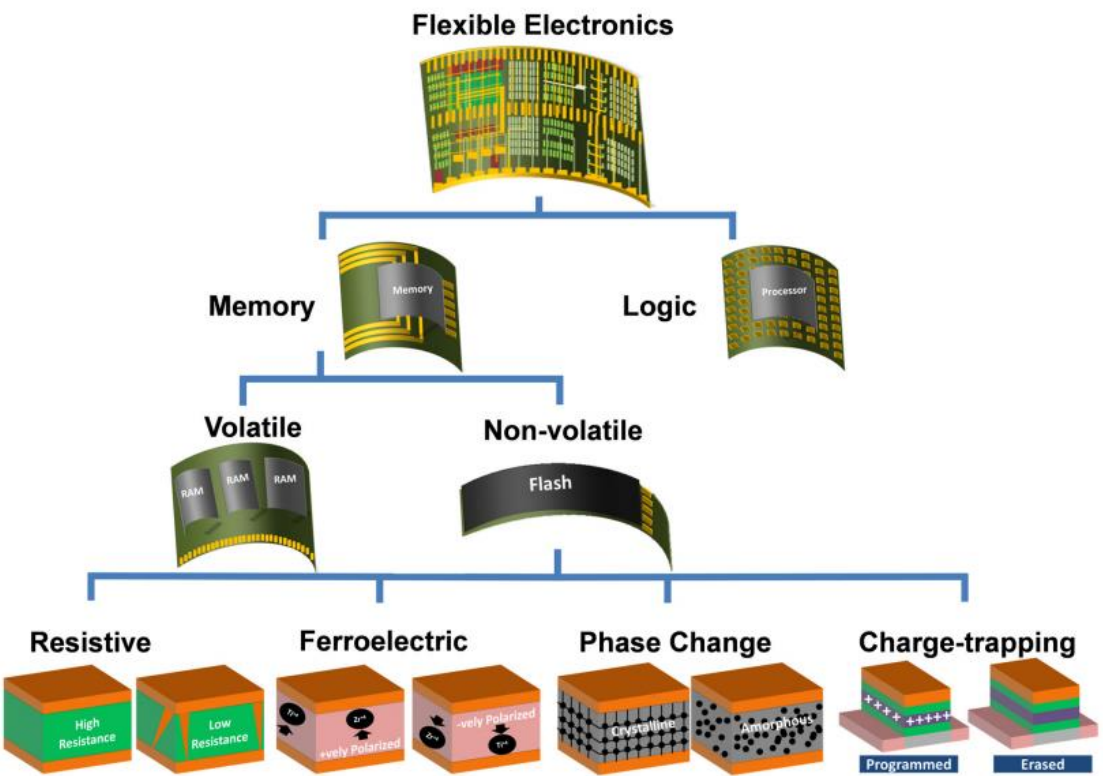


Figure 1.3.1: Chart highlighting the focus of the review.

As of today variety of materials have been used to build NVM devices. For example, NMVs based on; (i) embedded 0-dimensional gold nanoparticles (NPs) [68-72], black phosphorous quantum dots (QDs) [73], and silicon QDs [74], (ii) 1-dimensional zinc oxide (ZnO) nanowires [75], silicon (Si) nanowires [76], and carbon nanotubes (CNTs) [77-79], and (iii) 2-dimensional graphene [80-82], graphene oxide [83-89], molybdenum disulfide (MoS_2) [90, 91], zinc oxide (ZnO) [75], and hydrated tungsten tri-oxide ($WO_3.H_2O$) nano-sheet [51] have already been reported.

Although, these and other similar reports have focused on discrete memory devices or cells, academic researchers and semiconductor industries have reported macroelectronics (large area electronics) focusing on mainly artificial skin [92-94] and display technology where memory has not been an integrated built-in module. Sony

reported a rollable organic light emitting diode (OLED) based display in 2010 [95]. Samsung in the consumer electronics show (CES) 2011 and, later, LG and Nokia demonstrated a flexible display prototype [96]. However, the futuristic vision of the IoT where everything is connected, communicating, and making real-time decisions with artificial intelligence, with the associated emerging markets of big data analysis and machine-to-machine (M2M) technologies, would require more than flexible displays. The steep increase in the number of sensors from few millions in 2007 to billions of devices in 2013 is expected to persist, reaching the trillion sensor devices mark by 2023 due to the impact of IoT [97]. These sensors will be integrated in smart cards and RFIDs, vehicular technologies, buildings, infrastructures, healthcare, smart energy, factories, and supply chain management [97-99], as well as on humans for improving regular day to day experience [100]. To achieve such functionalities and fulfill the futuristic vision, IoT devices will require: (i) increased intra-node processing for real-time decision making, (ii) robustness to environmental variations (reliability), (iii) ultra-low power operation, (iv) ultra-high density integrated NVM and (v) smart antennas for wireless communications [101-105]. In addition, IoT devices should be physically flexible to enable wider adaptation in wearable forms and conforming to curvilinear structures in various forms.

To this end, integrated device manufacturers (IDMs) have already demonstrated devices designed to meet the IoT requirements. In 2014, Aitken et al. identified the 65 nm CMOS technology as the most suitable IoT chip process based on wafer cost and die area analysis [106]. In 2015, Yamamoto et al. demonstrated a novel gate stack in 65 nm CMOS technology for ultra-low leakage devices [102], Ueki et al. from Renesas

Electronics Corporation developed a low power 2 Mb ReRAM macro in 90 nm CMOS technology [107], Whatmough et al. implemented a 0.6 volts transceiver in 65 nm CMOS technology [108], and Yamauchi et al. developed an embedded flash memory in vehicle control systems for IoT applications [99]. Furthermore, Hitachi researchers have studied how to profit from IoT for 10 years and used big data analysis to introduce the wearable happiness meter to unravel the link between physical motion and happiness [100]. Tanakamaru et al. introduced privacy protection solid state storage (PP-SSS) for what they called, "the right to be forgotten," where data is physically and automatically broken hardware-wise to co-op with anticipated security and privacy issues in the IoT era [109]. These are all great milestones in providing useful insights of what the future holds with the IoT revolution.

Based on the existing progress and current status, it is evident that while IoT devices are required to attain physical flexibility, they still have to rely on CMOS technology while pushing for ultra-low power consumption, ultra-low leakage currents, improved reliability, and ultra large scale co-integration of NVMs, CPUs, and antennas. Flexible antennas have been studied for decades and will not be discussed in this section [110-115]. As aforementioned, NVM modules require information storage elements and select access transistors; therefore, a NVM perspective of the flexible electronics arena provides a comprehensive overview of the basic elements needed for implementing all electronic systems, including systems suitable for IoT applications.

1.3.1. All Organic Systems

Most organic electronics use a variety of polymeric semiconductors as channel materials, polymeric ferroelectrics for nonvolatile storage, and thick, durable insulating polymers to support the flexible substrate. Figure 1.3.1.1a shows a representative structure for an all-organic deposited NVM that uses a quinoidal oligothiophene derivative ($QQT(CN)_4$) as the organic channel material and a polyvinilidene-co-trifluoroethylene (PVDF-TrFE) as the ferroelectric material; Figure 1.3.1.1b shows an inkjet-printed organic inverter on a plastic substrate. Compared to inorganic silicon electronics, the all-organic approach is more challenging with respect to the performance of organic materials, especially as transistor channel materials. The highest reported mobility for most organic channel materials is more than 20 times lower than silicon [116-119], with the exception of 43 cm^2/V.s peak hole saturation mobility reported by Yongbo Yuan *et al.* in 2014 [120]: this translates into lower performance. Furthermore, organic electronics have yet to match the reliability of inorganic electronics nor can they compare in thermal stability [121]. To capitalize on the low-cost benefits of an all-organic system, there is a need to integrate polymeric dielectrics because they typically have low dielectric constants compared to the semiconductor industry's high-κ dielectrics and, in most cases, are even lower than that of SiO_2 [122]. Although it is a challenge to achieve the high capacitance values required for high-performance electronic devices using all-organic materials, there are also benefits from their use such as extremely high flexibility and conformal abilities. Currently, flexible organic electronic research has already gained solid grounds in commercial applications like active-matrix organic light-

emitting diode (AMOLED) displays [123]. Therefore, organic electronics show true potential for further expansion and enhanced maturity in macroelectronics.

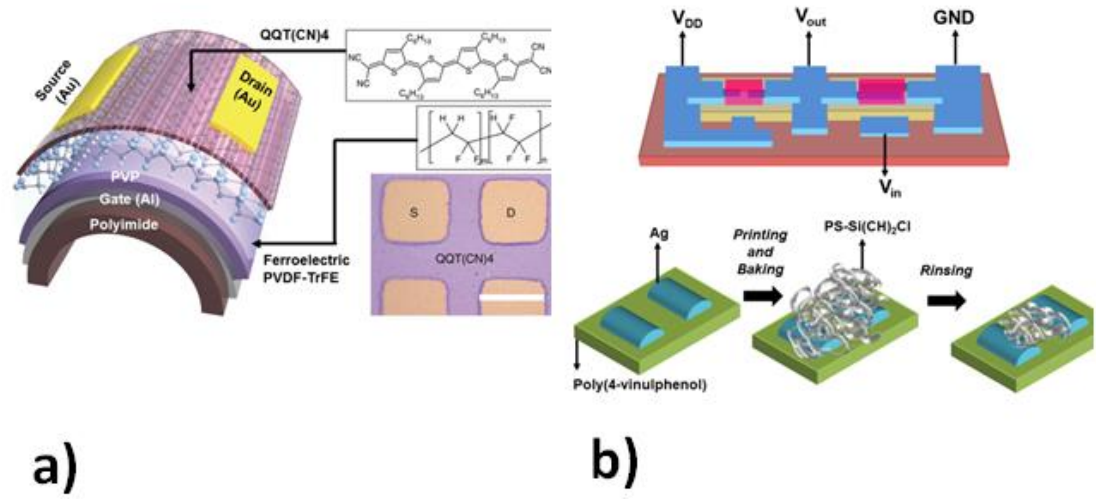


Figure 1.3.1.1: a) Schematic representation of the devices and molecular structure of the organic semiconductor QQT(CN)4 and the ferroelectric PVDF-TrFE. Reprinted by permission from Macmillan Publishers Ltd: Nature Communications [35], copyright (2014), b) schematic of an all-inkjet-printed inverter using two p -type OTFTs (top) and diagrams of the PS brush treatment procedure on the PVP gate dielectric and Ag S/D electrodes (bottom). Reprinted with permission from [43]. Copyright © 2013 WILEY-VCH Verlag GmbH & Co.

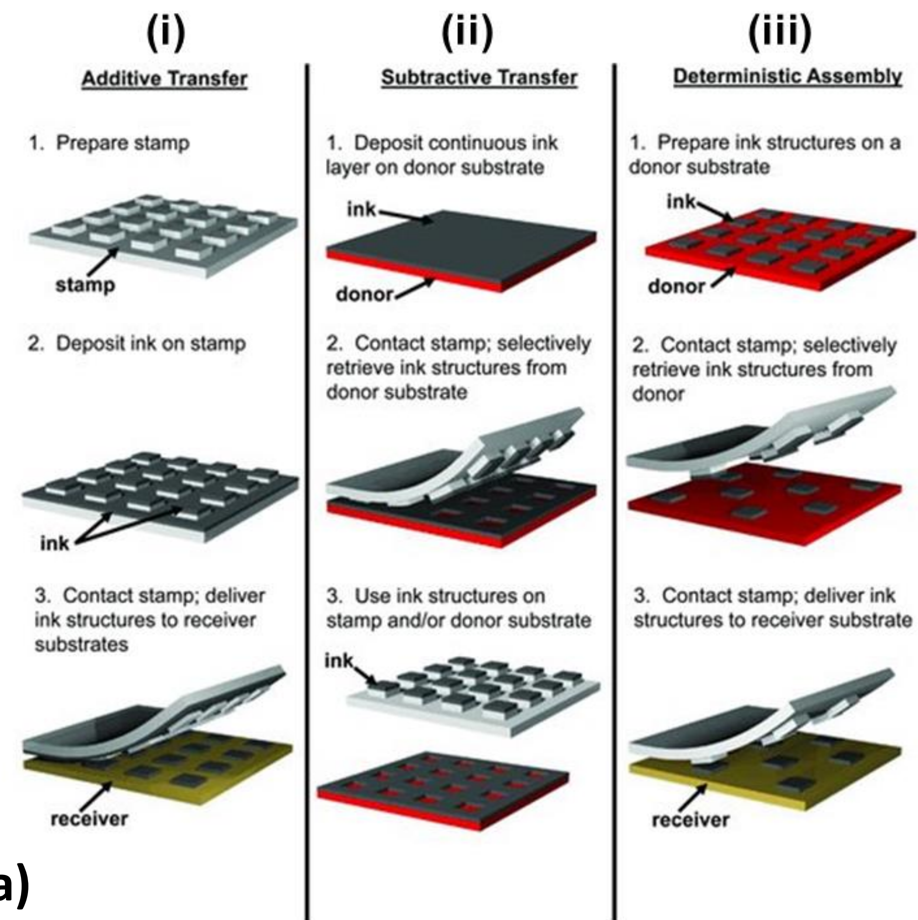
1.3.2. Hybrid Systems

Hybrid systems use both organic and inorganic materials, making them conducive to a wider spectrum of techniques with greater versatility. Figure 1.3.2.1 is an illustrative summary of available flexible hybrid techniques. In transfer printing, a molded polymer is used as a stamp that can be functionalized with desired materials and then printed onto a different substrate. Figure 1.3.2.1aa shows the three modes of transfer printing by John Rogers's group at the University of Illinois at Urbana-Champaign [45]. Figure 1.3.2.1bb shows a representative generic transfer technique, where devices are fabricated on a specific rigid substrate and then transferred to one that is flexible (a banknote in this

case). A specific type of transfer is the laser lift-off by Keon Jae Lee's group at the Korea Advanced Institute of Science and Technology (KAIST), where a laser shot is used to etch a sacrificial layer to release the device for transfer (Figure 1.3.2.1c) [54]. Figure 1.3.2.1d shows a resistive memory structure made up of room-temperature-sputtered and e-beam-evaporated materials on a flexible substrate [55]. The mainstream hybrid transfer approach achieves high performance by transferring high-performance inorganic devices onto an organic substrate for flexibility; however, it adds extra nonconventional transfer steps and suffers low yields. Although this is mitigated by the direct-deposition-on-plastic-substrates approach, using plastic adds temperature restrictions to the fabrication process. As a result, it is a challenge to produce high-quality films such as atomic-layer-deposited high-κ dielectrics that usually require temperatures above 300°C. And finally, because the different solvents used for patterning and photolithography should not affect the flexible organic substrate, there are limitations to suitable plastic material choices.

The spalling technique uses stressor layers to initiate fracture-modes in SOI and semiconductor substrates. In 2012, Banarjee *et al.* reported on the exfoliation of thin-film transistors from prefabricated bulk wafers using the spalling technique [124]. In the same year, Shahrejerdi *et al.* reported having performed, at room temperature, controlled spalling of full SOI wafer circuitry and successfully transferred the surface layer to a flexible plastic substrate [59, 125]. The authors deposited a nickel (Ni) stressor layer that abruptly discontinued near one edge of the wafer where a crack in the mono-crystalline silicon (Si) was initiated by an applied force [126, 127]. However, before the force is applied, polyimide tape is added to support the flexible peeled fabric-bearing ultra-thin

body devices (Figure 1.3.2.2). This approach has also been reported for single crystals of germanium (Ge) and gallium arsenide (GaAs) [60, 128]. Another spalling approach was used by Bellanger and Serra where Si (100) foils were peeled off from the bulk substrate [61]. The challenges faced by the spalling technique are two fold: first, extra deposition and complex tuning of a stressor material with a specific thickness followed by etching are required and second, once the crack has been initiated, the peeling-off process requires high dexterity that is not suitable for mass production.



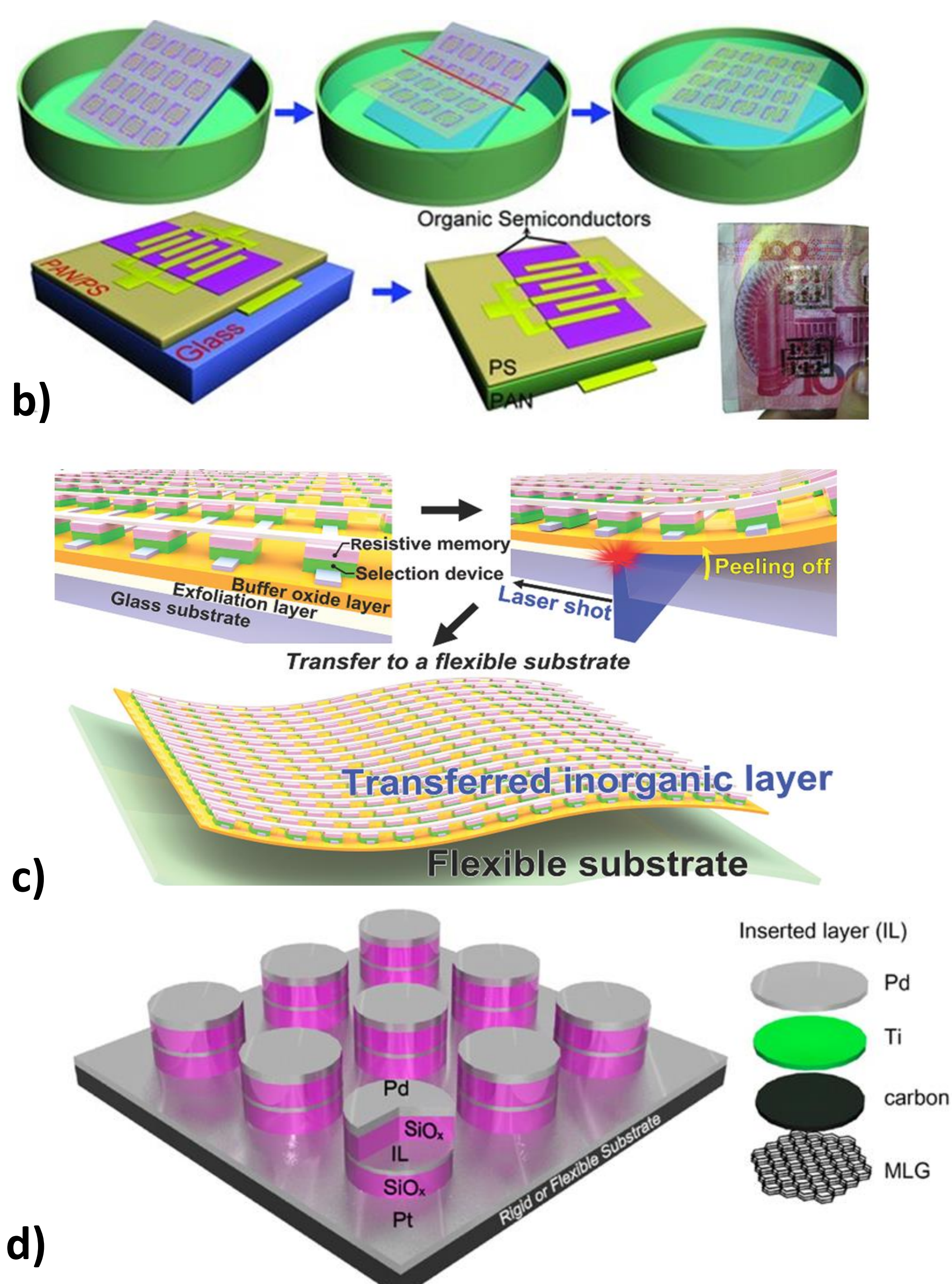


Figure 1.3.2.1: a) Schematic illustrations of three basic modes for transfer printing. Reprinted with permission from [45]. Copyright © 2012 WILEY-VCH Verlag GmbH & Co., b) schematic diagram of the fabrication procedures for the freestanding OFETs using modified water-floatation method. Reprinted with permission from [52]. Copyright © 2013 WILEY-VCH Verlag GmbH & Co., c) schematic illustrations of the process for fabricating flexible crossbar-structured memory on a plastic substrate via the laser lift-off transfer method. Reprinted with permission from [54]. Copyright © 2014 WILEY-VCH Verlag GmbH & Co., d) schematic illustration of the cells in the conducting-interlayer SiOx memory device sputtered at room temperature. Reprinted with permission from [55]. Copyright © 2014 WILEY-VCH Verlag GmbH & Co.

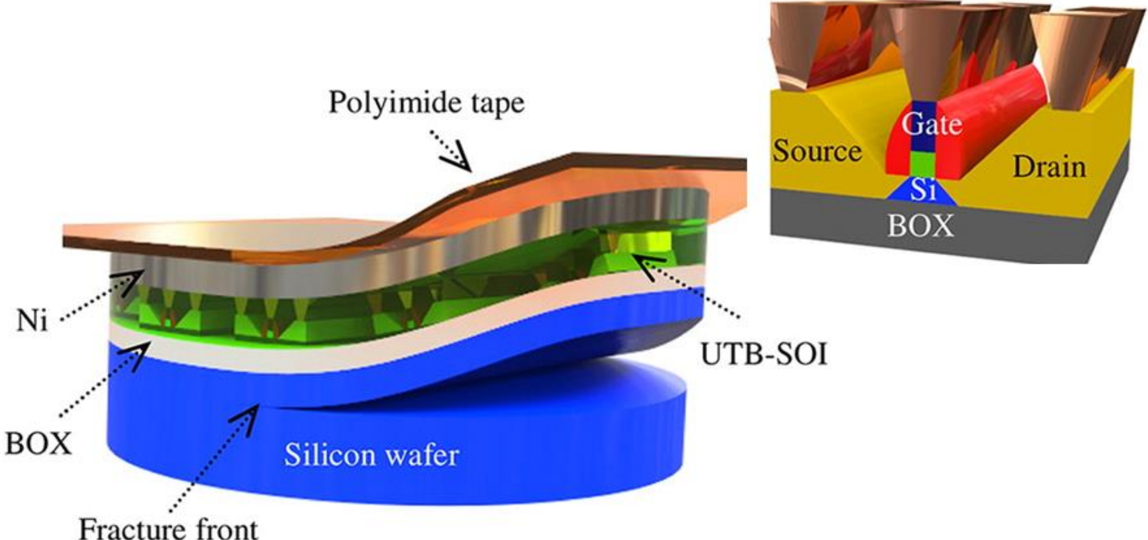


Figure 1.3.2.2: Schematic illustration of the controlled spalling process used for removing the prefabricated devices and circuits from the rigid silicon handle wafer. The inset schematically shows the device architecture for the ultra-thin body transistors with raised source/drain regions. Reprinted with permission from [59]. Copyright (2012) American Chemical Society.

1.3.3. Flexible Silicon Systems

The complementary transfer-free approach uses a fundamental inverse proportionality between the material's thickness (t) and its flexibility. Equation 1 shows the relation between the deflection 'δ' occurring in a material, with flexural modulus "$E_{Flexural}$", thickness 't,' length 'L' and width 'w,' due to an applied force 'F.' $E_{Flexural}$ is a material property. Therefore, for specific 'L' and 'w,' a material with lower thickness 't' would experience larger deflections 'δ' due to the same applied force 'F' (i.e. it becomes more flexible). Hence, we transform traditional, rigid electronic devices on economical Si (100) wafers into new, flexible devices by sufficiently reducing the thickness of the host's substrate.

$$\delta = \frac{FL^3}{4E_{Flexural}\boldsymbol{wt^3}} \qquad (1)$$

This approach provides a pragmatic solution to the aforementioned critical challenges by copying the associated perks of high performance, reliability, ULSI density, and the low cost of inorganic silicon-based electronics to the flexible arena via a transformed version of traditional devices. Moreover, the silicon industry has capitalized on monolithic integration over the past few decades and because of its core competitive advantages, it has grown into a huge market. Hence, preserving monolithic integration by using Si as a flexible substrate further improves this flexing approach. Figure 1.3.3.1 lists the different silicon-flexing techniques [62, 66, 67]. The scanning electron microscope image in Figure 1.3.3.1b illustrates the added advantage of extra device active area, which may be available in the form of conformal deposition of device layers through release trenches (holes) [129]. The etch-protect-release approach incurs some lost area, which is compensated by the potential reliability associated with the relatively novel air-gap shallow trench isolation (STI) technology [130]. On the other hand, remaining portions of the wafer can be recycled after chemical mechanical polishing and the holes network has a self-cooling effect, acting as air cooling channels for heat dissipation [131].

Although, conceptually the soft back-etching process (Figure 1.3.3.1c) is similar to the traditional back-grinding technique, there are considerable differences. For example, the soft back etch is a simple and delicate process compared to the complex and abrasive nature associated with the induced scratches, crystal defects, and the formation of stresses that take place during back grinding [132]. Furthermore, using the soft back etch requires no chemical mechanical polishing and leaves no residual stress on the substrate unlike the machining stress caused during back grinding [133-135]. Finally,

back grinding to thinner substrates causes subsurface damage [135] and shallow surface cracks [134].

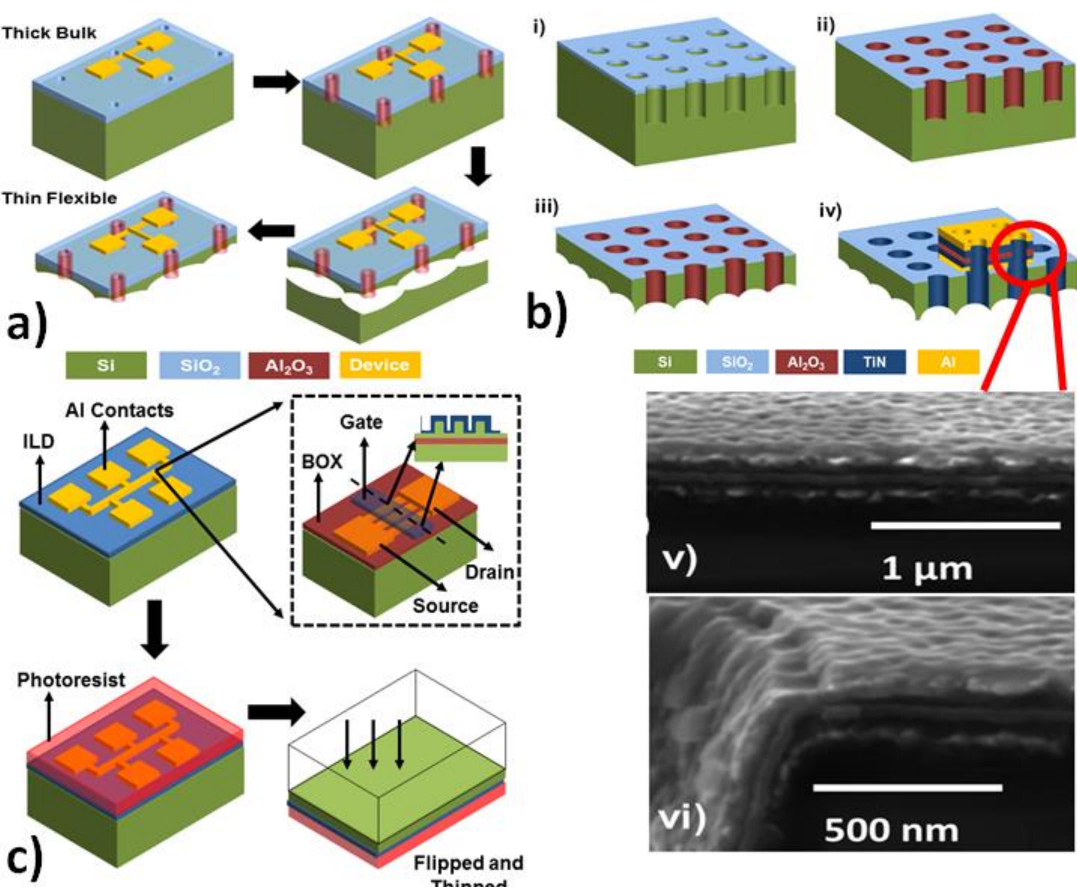


Figure 1.3.3.1: a) Device first approach illustration where the devices are fabricated in a traditional fashion, then, protected using photoresist (PR). The PR is then patterned and the pattern is transferred to the field oxide (FOX) layer then to the Si substrate. Using the spacer technique, a highly conformal atomic layer deposition (ALD) spacer is deposited for sidewalls. Finally, the dies are put in a reactive chamber containing XeF2 gas for isotropic Si when the etching regions merge, the top flexible portion of Si (100) containing the devices can be safely released, b) device last approach illustration where flexible silicon fabric is first released then devices are built. Adapted with permission from [129]. Copyright © 2014 WILEY-VCH Verlag GmbH & Co., c) illustration of the soft-etch back approach where the traditional dies containing devices are covered with PR for protection, then, the die is flipped upside down and etched using DRIE to the desired thickness. Adapted with permission from [67]. Copyright (2014) American Chemical Society.

Fracture strength is a property that applies to all techniques because it determines the overall mechanical stability of an ultra-thin flexible electronic system [136]. To assess the fracture strength of a substrate, the most common method is the three-point bending test [137]. For Si thicknesses greater than 100 μm, the linear elastic bending beam theory provides an accurate estimation of fracture strength [138,139]; however, thinner substrates produce a nonlinear deflection-load relationship that is used to estimate fracture strength (Figure 1.3.3.2). This is caused by the large deflection of the thin silicon substrate resulting from horizontal forces at the supporting bearings; to account for this nonlinearity, in 2015 Liu *et al.* introduced the large deflection theory of beam [137]. This relationship provides important insights for theoretical limitations of flexible silicon thinner than 100 μm. Furthermore, based on the application's required bending radius, the thickness of the flexible silicon substrate must be adjusted such that the applied stress (stress=Young's modulus x strain (ε), where nominal strain is defined as $\varepsilon_{nominal}$=(thickness (t))/((2 x bending radius (r))) is lower than the fracture stress (fracture stress of thin Si substrates is higher than that of thicker substrates). For instance, [137] shows that for a 50-μm thick silicon substrate, the fracture stress is ~ 1.1 GPa. At the lowest estimate for Si (100), the Young's modulus is 128 GPa [140]; hence, the minimum bending radius that would cause fracture stress for a 50-μm thick flexible silicon substrate is ~ 3 mm and decreases with decreasing thicknesses. Therefore, a vanilla flexible silicon substrate that is 50-μm thick or less with a bending radius of > 3 mm will safely operate below the fracture stress level. We would like to point out that these results are for a bare silicon (100) substrate with no additive layers or patterns for devices. Therefore, based on the properties of the material, thickness of the substrate, and the bending radius necessary

for a specific application, the most suitable approach and material system can be determined. Noteworthy, the nominal strain is only a nominal value; whereas, the actual stress value depends on the modulus of elasticity of specific constituent material stacks.

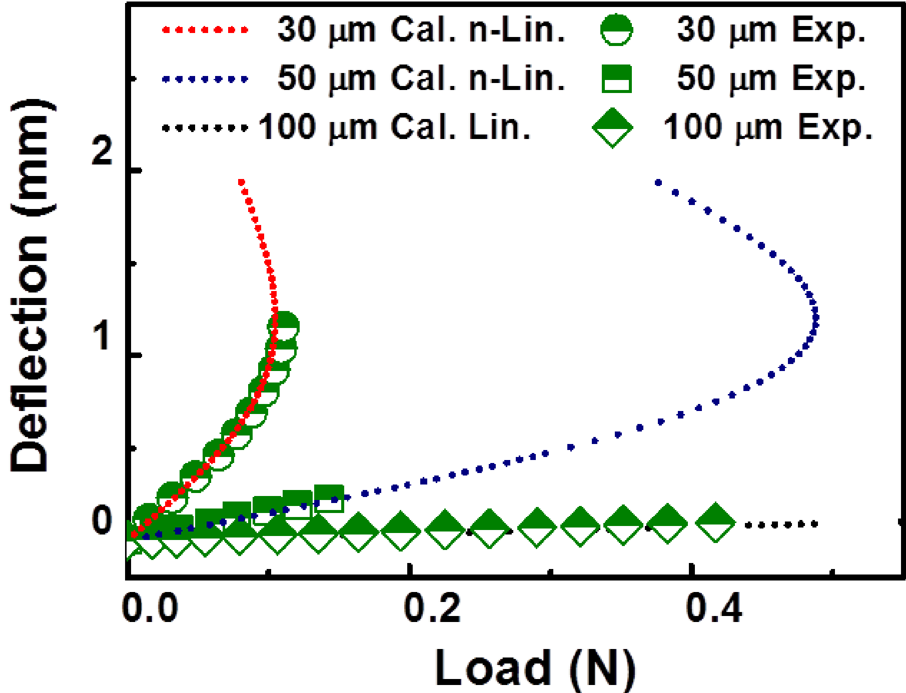


Figure 1.3.3.2: Deflection versus applied load plot for various thicknesses of flexible substrates, dotted lines showing non-linear analytical solution for 30 and 40 μm thick substrates and linear analytical solution for 100 μm thick substrates. Adapted courtesy of Prof. YongAn Huang, Huazhong University of Science and Technology, China.

As identified by the International Technology Roadmap for Semiconductors (ITRS) 2013 Emerging Research Devices report, the main challenge will be to identify replacement technologies for static RAM and flash as they approach their physical limits [141]. Replacements must provide electrically accessible, high-speed, high-density, low-power NVMs that meet the reliability requirements for the desired devices including surviving high temperatures. It will be important to identify and address other reliability

issues early in the development process. The temperature requirement for flexible, inorganic silicon-based NVM devices is a given because the materials used will have already survived the high thermal budgets required for the deposition of high-quality thin films used in complementary metal oxide semiconductor (CMOS) technology and subsequent front-end-of-line processing anneals. Due to the advancements in lithography, properties of a flexible inorganic NVM also rely on high integration density.

Challenges common to both organic and inorganic material systems toward their application in future electronics, including IoT devices include (i) attaining high speeds, (ii) being suitable for low-power devices, and (iii) identifying and assessing the reliability issues that arise when devices are flexed beyond the standard studied stresses in planar substrates. In addition, organic electronics must also achieve temperature stability and satisfactory integration density. The forthcoming sections of the dissertation focus on our contributions in advancing the status quo of the flexible silicon system approach as a feasible solution for future flexible IoT and wearable memories and electronic systems.

1.4. References

[1] Han, S.-T.; Zhou, Y.; Roy, V.A.L. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* 2013, 25, 5425-5449.

[2] Govoreanu, B.; Kar, G.; Chen, Y.; Paraschiv, V.; Kubicek, S.; Fantini, A.; Radu, I.; Goux, L.; Clima, S.; Degraeve, R. 10× 10nm^2 Hf/HfOx crossbar resistive RAM with excellent performance, reliability and low-energy operation. In IEEE International Electron Device Meeting, Washington, DC, USA, 5-7 December 2011, pp. 31.6.1-31.6.4.

[3] Jo, S.H.; Chang, T.; Ebong, I.; Bhadviya, B.B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano Lett.* 2010, 10, 1297-1301.

[4] Strukov, D.B.; Snider, G.S.; Stewart, D.R.; Williams, R.S. The missing memristor found. *Nature* 2008, 453, 80-83.

[5] Chua, L.O. Memristor-the missing circuit element. *IEEE Trans. Circuit Theory* 1971, 18, 507-519.

[6] Shannigrahi, S.R.; Jang, H.M. Fatigue-free lead zirconate titanate-based capacitors for nonvolatile memories. *Appl. Phys. Lett.* 2001, 79, 1051-1053.

[7] Parkin, S.; Xin, J.; Kaiser, C.; Panchula, A.; Roche, K.; Samant, M. Magnetically engineered spintronic sensors and memory. *Proc. IEEE* 2003, 91, 661-680.

[8] Gupta, M.K.; Hasan, M. Robust High Speed Ternary Magnetic Content Addressable Memory. *IEEE Trans. Electron Devices* 2015, 62, 1163-1169.

[9] Lencer, D.; Salinga, M.; Wuttig, M. Design Rules for Phase-Change Materials in Data Storage Applications. *Adv. Mater.* 2011, 23, 2030-2058.

[10] Yoon, J.M.; Shin, D.O.; Yin, Y.; Seo, H.K.; Kim, D.; Kim, Y.I.; Jin, J.H.; Kim, Y.T.; Bae, B.-S.; Kim, S.O. Fabrication of high-density $In_3Sb_1Te_2$ phase change nanoarray on glass-fabric reinforced flexible substrate. *Nanotechnology* 2012, 23, 255301.

[11] Jeon, Y.; Lee, M.; Moon, T.; Kim, S. Flexible Nano-Floating-Gate Memory With Channels of Enhancement-Mode Si Nanowires. *IEEE Trans. Electron Devices* 2012, 59, 2939-2942.

[12] Yoon, K.; Il Han, P.; Seongjae, C.; Jang-Gn, Y.; Jung Hoon, L.; Doo-Hyun, K.; Gil Sung, L.; Se-Hwan, P.; Dong Hua, L.; Won Bo, S.; Wandong, K.; Hyungcheol, S.; Jong-Duk, L.; Park, B.-G. A Vertical 4-Bit SONOS Flash Memory and a Unique 3-D Vertical Array Structure. *IEEE Trans. Nanotechnol.* 2010, 9, 70-77.

[13] Lee, J.S.; Kim, Y.M.; Kwon, J.H.; Shin, H.; Sohn, B.H.; Lee, J. Tunable memory characteristics of nanostructured, nonvolatile charge trap memory devices based on a binary mixture of metal nanoparticles as a charge trapping layer. *Adv. Mater.* 2009, 21, 178-183.

[14] Pott, V.; Vaddi, R.; Geng Li, C.; Lin, J.T.M.; Kim, T.T. Design Optimization of Pulsed-Mode Electromechanical Nonvolatile Memory. *IEEE Electron Device Lett.* 2012, 33, 1207-1209.

[15] Young Choi, W.; Hei, K.; Lee, D.; Lai, J.; Tsu-Jae King, L. Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration. In IEEE International Electron Devices Meeting, Washington, DC, USA, 10-12 December 2007, pp. 603-606.

[16] Green, J.E.; Choi, J.W.; Boukai, A.; Bunimovich, Y.; Johnston-Halperin, E.; DeIonno, E.; Luo, Y.; Sheriff, B.A.; Xu, K.; Shin, Y.S. A 160-kilobit molecular electronic memory patterned at 1011 bits per square centimetre. *Nature* 2007, 445, 414-417.

[17] Joachim, H.O.; Jacob, M.; Rehm, N. 2T2C signal margin test mode using a defined charge exchange between BL and/BL. U.S. Patents US6876590 B2, 5 April 2005.

[18] Wang, X.P.; Fang, Z.; Li, X.; Chen, B.; Gao, B.; Kang, J.F.; Chen, Z.X.; Kamath, A.; Shen, N.S.; Singh, N.; Lo, G.Q.; Kwong, D.L. Highly compact 1T-1R architecture ($4F^2$ footprint) involving fully CMOS compatible vertical GAA nano-pillar transistors and oxide-based RRAM cells exhibiting excellent NVM properties and ultra-low power operation. In IEEE International Electron Devices Meeting, Washington, DC, USA, 10-12 December 2007, San Francisco, CA, USA, 10-13 December 2012, pp. 20.6.1-20.6.4.

[19] Joachim, H.O.; Jacob, M.; Rehm, N. 2T2C signal margin test mode using a defined charge exchange between BL and/BL. U.S. Patents US20040095821 A1, 20 May 2004.

[20] Ogasawara, S.; Ishiwara, H. Fabrication and characterization of 1T2C-type ferroelectric memory cell with local interconnections. *Jpn. J. Appl. Phys.* 2002, 41, 6895.

[21] Hyun-Soo, K.; Shuu'ichirou, Y.; Toru, I.; Takaaki, F.; Hiroshi, O.; Hiroshi, I. Fabrication and Characterization of 1 k-bit 1T2C-Type Ferroelectric Memory Cell Array. *Jpn. J. Appl. Phys.* 2005, 44, 2715.

[22] Hyun-Soo, K.; Shuu'ichirou, Y.; Hiroshi, I. Improved Data Disturbance Effects in 1T2C-Type Ferroelectric Memory Array. *Jpn. J. Appl. Phys.* 2004, 43, 2558.

[23] Zhou, H.; Seo, J.-H.; Paskiewicz, D.M.; Zhu, Y.; Celler, G.K.; Voyles, P.M.; Zhou, W.; Lagally, M.G.; Ma, Z. Fast flexible electronics with strained silicon nanomembranes. *Sci. Rep.* 2013, 3, 1291.

[24] Des Etangs-Levallois, A.L.; Lesecq, M.; Danneville, F.; Tagro, Y.; Lepilliet, S.; Hoel, V.; Troadec, D.; Gloria, D.; Raynaud, C.; Dubois, E. Radio-frequency and low noise characteristics of SOI technology on plastic for flexible electronics. *Solid-State Electron.* 2013, 90, 73-78.

[25] Nasr, B.; Wang, D.; Kruk, R.; Rösner, H.; Hahn, H.; Dasgupta, S. Flexible Electronics: High-Speed, Low-Voltage, and Environmentally Stable Operation of Electrochemically Gated Zinc Oxide Nanowire Field-Effect Transistors. *Adv. Funct. Mater.* 2013, 23, 1729-1729.

[26] Han, S.T.; Zhou, Y.; Wang, C.; He, L.; Zhang, W.; Roy, V. Flexible Electronics: Layer-by-Layer-Assembled Reduced Graphene Oxide/Gold Nanoparticle Hybrid Double-Floating-Gate Structure for Low-Voltage Flexible Flash Memory. *Adv. Mater.* 2013, 25, 793-793.

[27] Farsinezhad, S.; Mohammadpour, A.; Dalrymple, A.N.; Geisinger, J.; Kar, P.; Brett, M.J.; Shankar, K. Transparent anodic TiO_2 nanotube arrays on plastic substrates for disposable biosensors and flexible electronics. *J. Nanosci. Nanotechnol.* 2013, 13, 2885-2891.

[28] Majewski, L.; Grell, M.; Ogier, S.; Veres, J. A novel gate insulator for flexible electronics. *Org. Electron.* 2003, 4, 27-32.

[29] McAlpine, M.C.; Friedman, R.S.; Lieber, C.M. High-performance nanowire electronics and photonics and nanoscale patterning on flexible plastic substrates. *Proc. IEEE* 2005, 93, 1357-1363.

[30] Sun, Y.; Rogers, J.A. Inorganic semiconductors for flexible electronics. *Adv. Mater.* 2007, 19, 1897-1916.

[31] Rogers, J.A.; Someya, T.; Huang, Y. Materials and Mechanics for Stretchable Electronics. *Science* 2010, 327, 1603-1607.

[32] Sokolov, A.N.; Tee, B.C.K.; Bettinger, C.J.; Tok, J.B.H.; Bao, Z. Chemical and Engineering Approaches To Enable Organic Field-Effect Transistors for Electronic Skin Applications. *Acc. Chem. Res.* 2012, 45, 361-371.

[33] Wang, C.; Hwang, D.; Yu, Z.; Takei, K.; Park, J.; Chen, T.; Ma, B.; Javey, A. User-interactive electronic skin for instantaneous pressure visualization. *Nat. Mater.* 2013, 12, 899-904.

[34] Mei, Y.; Loth, M.A.; Payne, M.; Zhang, W.; Smith, J.; Day, C.S.; Parkin, S.R.; Heeney, M.; McCulloch, I.; Anthopoulos, T.D. High Mobility Field-Effect Transistors with Versatile Processing from a Small-Molecule Organic Semiconductor. *Adv. Mater.* 2013, 25, 4352-4357.

[35] Kim, R.H.; Kim, H.J.; Bae, I.; Hwang, S.K.; Velusamy, D.B.; Cho, S.M.; Takaishi, K.; Muto, T.; Hashizume, D.; Uchiyama, M. Non-volatile organic memory with sub-millimetre bending radius. *Nat. Commun.* 2014, 5, 3583.

[36] Liu, X.; Guo, Y.; Ma, Y.; Chen, H.; Mao, Z.; Wang, H.; Yu, G.; Liu, Y. Organic Electronics: Flexible, Low-Voltage and High-Performance Polymer Thin-Film Transistors and Their Application in Photo/Thermal Detectors . *Adv. Mater.* 2014, 26, 3569-3569.

[37] Lai, Y.-C.; Huang, Y.-C.; Lin, T.-Y.; Wang, Y.-X.; Chang, C.-Y.; Li, Y.; Lin, T.-Y.; Ye, B.-W.; Hsieh, Y.-P.; Su, W.-F. Stretchable organic memory: toward learnable and digitized stretchable electronic applications. *NPG Asia Mater.* 2014, 6, e87.

[38] Tiwari, J.N.; Meena, J.S.; Wu, C.S.; Tiwari, R.N.; Chu, M.C.; Chang, F.C.; Ko, F.H. Thin-Film Composite Materials as a Dielectric Layer for Flexible Metal–Insulator–Metal Capacitors. *ChemSusChem* 2010, 3, 1051-1056.

[39] Kraft, U.; Sejfić, M.; Kang, M.J.; Takimiya, K.; Zaki, T.; Letzkus, F.; Burghartz, J.N.; Weber, E.; Klauk, H. Flexible Low-Voltage Organic Complementary Circuits: Finding the Optimum Combination of Semiconductors and Monolayer Gate Dielectrics. *Adv. Mater.* 2015, 27, 207-214.

[40] Yokota, T.; Kuribara, K.; Tokuhara, T.; Zschieschang, U.; Klauk, H.; Takimiya, K.; Sadamitsu, Y.; Hamada, M.; Sekitani, T.; Someya, T. Flexible Low-Voltage Organic Transistors with High Thermal Stability at 250° C. *Adv. Mater.* 2013, 25, 3639-3644.

[41] Lien, D.-H.; Kao, Z.-K.; Huang, T.-H.; Liao, Y.-C.; Lee, S.-C.; He, J.-H. All-printed paper memory. *ACS Nano* 2014, 8, 7613-7619.

[42] Kim, S.; Cook, B.; Le, T.; Cooper, J.; Lee, H.; Lakafosis, V.; Vyas, R.; Moro, R.; Bozzi, M.; Georgiadis, A. Inkjet-printed antennas, sensors and circuits on paper substrate. *IET Microw. Antennas Propag.,* 2013, 7, 858-868.

[43] Chung, S.; Jang, M.; Ji, S.B.; Im, H.; Seong, N.; Ha, J.; Kwon, S.K.; Kim, Y.H.; Yang, H.; Hong, Y. Flexible High-Performance All-Inkjet-Printed Inverters: Organo-Compatible and Stable Interface Engineering. *Adv. Mater.* 2013, 25, 4773-4777.

[44] Baeg, K.J.; Caironi, M.; Noh, Y.Y. Toward printed integrated circuits based on unipolar or ambipolar polymer semiconductors. *Adv. Mater.* 2013, 25, 4210-4244.

[45] Carlson, A.; Bowen, A.M.; Huang, Y.; Nuzzo, R.G.; Rogers, J.A. Transfer printing techniques for materials assembly and micro/nanodevice fabrication. *Adv. Mater.* 2012, 24, 5284-5318.

[46] Stauth, S.A.; Parviz, B.A. Self-assembled single-crystal silicon circuits on plastic. *Proc. Natl. Acad. Sci.* 2006, 103, 13922-13927.

[47] Kim, T.-i.; Jung, Y.H.; Chung, H.-J.; Yu, K.J.; Ahmed, N.; Corcoran, C.J.; Park, J.S.; Jin, S.H.; Rogers, J.A. Deterministic assembly of releasable single crystal silicon-metal oxide field-effect devices formed from bulk wafers. *Appl. Phys. Lett.* 2013, 102, 182104.

[48] Lee, C.H.; Kim, D.R.; Zheng, X. Fabricating nanowire devices on diverse substrates by simple transfer-printing methods. *Proc. Natl. Acad. Sci.* 2010, 107, 9950-9955.

[49] Kim, S.; Jeong, H.Y.; Kim, S.K.; Choi, S.-Y.; Lee, K.J. Flexible memristive memory array on plastic substrates. *Nano Lett.* 2011, 11, 5438-5442.

[50] Sevilla, G.A.T.; Rojas, J.P.; Fahad, H.M.; Hussain, A.M.; Ghanem, R.; Smith, C.E.; Hussain, M.M. Flexible and Transparent Silicon-on-Polymer Based Sub-20 nm Non-planar 3D FinFET for Brain-Architecture Inspired Computation. *Adv. Mater.* 2014, 26, 2794-2799.

[51] Liang, L.; Li, K.; Xiao, C.; Fan, S.; Liu, J.; Zhang, W.; Xu, W.; Tong, W.; Liao, J.; Zhou, Y. Vacancy Associates-rich Ultrathin Nanosheets for High Performance and Flexible Nonvolatile Memory Device. *J. Am. Chem. Soc.* 2015, 137, 3102-3108.

[52] Zhang, L.; Wang, H.; Zhao, Y.; Guo, Y.; Hu, W.; Yu, G.; Liu, Y. Substrate-free ultra-flexible organic field-effect transistors and five-stage ring oscillators. *Adv. Mater.* 2013, 25, 5455-5460.

[53] Kang, B.; Lee, W.H.; Cho, K. Recent advances in organic transistor printing processes. *ACS Appl. Mater. Interfaces* 2013, 5, 2302-2315.

[54] Kim, S.; Son, J.H.; Lee, S.H.; You, B.K.; Park, K.I.; Lee, H.K.; Byun, M.; Lee, K.J. Flexible Crossbar-Structured Resistive Memory Arrays on Plastic Substrates via Inorganic-Based Laser Lift-Off. *Adv. Mater.* 2014, 26, 7480-7487.

[55] Wang, G.; Raji, A.-R.O.; Lee, J.-H.; Tour, J.M. Conducting-Interlayer SiO_x Memory Devices on Rigid and Flexible Substrates. *ACS Nano* 2014, 8, 1410-1418.

[56] Lin, C.; Su, C.; Chang, C.; Wu, H. Resistive Switching Behavior of $Al/Al_2O_3/ZrO_2/Al$ Structural Device for Flexible Nonvolatile Memory Application. *IEEE Trans. Magn.* 2014, 50, 1-4.

[57] Hota, M.; Bera, M.; Maiti, C. Flexible metal–insulator–metal capacitors on polyethylene terephthalate plastic substrates. *Semicond. Sci. Technol.* 2012, 27, 105001.

[58] Hagendorfer, H.; Lienau, K.; Nishiwaki, S.; Fella, C.M.; Kranz, L.; Uhl, A.R.; Jaeger, D.; Luo, L.; Gretener, C.; Buecheler, S. Highly transparent and conductive ZnO: Al thin films from a low temperature aqueous solution approach. *Adv. Mater.* 2014, 26, 632-636.

[59] Shahrjerdi, D.; Bedell, S.W. Extremely flexible nanoscale ultrathin body silicon integrated circuits on plastic. *Nano Lett.* 2012, 13, 315-320.

[60] Stephen, W.B.; Keith, F.; Paul, L.; Davood, S.; John, A.O.; Devendra, S. Layer transfer by controlled spalling. *J. Phys. D: Appl. Phys.* 2013, 46, 152002.

[61] Bellanger, P.; Serra, J. Room Temperature Spalling of Thin Silicon Foils Using a Kerfless Technique. *Energy Procedia* 2014, 55, 873-878.

[62] Rojas, J.P.; Ghoneim, M.T.; Young, C.D.; Hussain, M.M. Flexible High-/Metal Gate Metal/Insulator/Metal Capacitors on Silicon (100) Fabric. *IEEE Trans. Electron Devices* 2013, 60, 3305-3309.

[63] Rojas, J.P.; Sevilla, G.T.; Hussain, M.M. Structural and electrical characteristics of high-k/metal gate metal oxide semiconductor capacitors fabricated on flexible, semi-transparent silicon (100) fabric. *Appl. Phys. Lett.* 2013, 102, 064102.

[64] Nassar, J.M.; Hussain, A.M.; Rojas, J.P.; Hussain, M.M. Low-cost high-quality crystalline germanium based flexible devices. *Phys. Status Solidi RRL* 2014, 8, 794-800.

[65] Sevilla, G.A.T.; Inayat, S.B.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible and Semi-Transparent Thermoelectric Energy Harvesters from Low Cost Bulk Silicon (100). *Small* 2013, 9, 3916-3921.

[66] Rojas, J.P.; Torres Sevilla, G.A.; Ghoneim, M.T.; Inayat, S.B.; Ahmed, S.M.; Hussain, A.M.; Hussain, M.M. Transformational Silicon Electronics. *ACS Nano* 2014, 8, 1468-1474.

[67] Torres Sevilla, G.A.; Ghoneim, M.T.; Fahad, H.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible Nanoscale High-Performance FinFETs. *ACS Nano* 2014, 8, 9850-9856.

[68] Zhou, Y.; Han, S.-T.; Sonar, P.; Roy, V.A.L. Nonvolatile multilevel data storage memory device from controlled ambipolar charge trapping mechanism. *Sci. Rep.* 2013, 3, 2319.

[69] Kim, S.-J.; Lee, J.-S. Flexible organic transistor memory devices. *Nano Lett.* 2010, 10, 2884-2890.

[70] Ye, Z.; Su-Ting, H.; Zong-Xiang, X.; Roy, V.A.L. Low voltage flexible nonvolatile memory with gold nanoparticles embedded in poly(methyl methacrylate). *Nanotechnology* 2012, 23, 344014.

[71] Li, J.; Yan, F. Solution-Processable Low-Voltage and Flexible Floating-Gate Memories Based on an n-Type Polymer Semiconductor and High-k Polymer Gate Dielectrics. *ACS Appl. Mater. Interfaces* 2014, 6, 12815-12820.

[72] Kim, S.-J.; Song, J.-M.; Lee, J.-S. Transparent organic thin-film transistors and nonvolatile memory devices fabricated on flexible plastic substrates. *J. Mater. Chem.* 2011, 21, 14516-14522.

[73] Zhang, X.; Xie, H.; Liu, Z.; Tan, C.; Luo, Z.; Li, H.; Lin, J.; Sun, L.; Chen, W.; Xu, Z. Black phosphorus quantum dots. *Angew. Chem., Int. Ed.* 2015, 54, 3653-3657.

[74] Dung, M.X.; Choi, J.-K.; Jeong, H.-D. Newly Synthesized Silicon Quantum Dot–Polystyrene Nanocomposite Having Thermally Robust Positive Charge Trapping. *ACS Appl. Mater. Interfaces* 2013, 5, 2400-2409.

[75] Sohn, J.I.; Choi, S.S.; Morris, S.M.; Bendall, J.S.; Coles, H.J.; Hong, W.-K.; Jo, G.; Lee, T.; Welland, M.E. Novel Nonvolatile Memory with Multibit Storage Based on a ZnO Nanowire Transistor. *Nano Lett.* 2010, 10, 4316-4320.

[76] Jeon, Y.; Lee, M.; Moon, T.; Kim, S. Flexible Nano-Floating-Gate Memory With Channels of Enhancement-Mode Si Nanowires. *IEEE Trans. Electron Devices* 2012, 59, 2939-2942.

[77] Hwang, S.K.; Lee, J.M.; Kim, S.; Park, J.S.; Park, H.I.; Ahn, C.W.; Lee, K.J.; Lee, T.; Kim, S.O. Flexible Multilevel Resistive Memory with Controlled Charge Trap B- and N-Doped Carbon Nanotubes. *Nano Lett.* 2012, 12, 2217-2221.

[78] Yu, W.J.; Chae, S.H.; Lee, S.Y.; Duong, D.L.; Lee, Y.H. Ultra-Transparent, Flexible Single-walled Carbon Nanotube Non-volatile Memory Device with an Oxygen-decorated Graphene Electrode. *Adv. Mater.* 2011, 23, 1889-1893.

[79] Tsai, C.-L.; Xiong, F.; Pop, E.; Shim, M. Resistive Random Access Memory Enabled by Carbon Nanotube Crossbar Electrodes. *ACS Nano* 2013, 7, 5360-5366.

[80] Hong, A.J.; Song, E.B.; Yu, H.S.; Allen, M.J.; Kim, J.; Fowler, J.D.; Wassei, J.K.; Park, Y.; Wang, Y.; Zou, J.; Kaner, R.B.; Weiller, B.H.; Wang, K.L. Graphene Flash Memory. *ACS Nano* 2011, 5, 7812-7817.

[81] Lee, W.; Kahya, O.; Toh, C.T.; Özyilmaz, B.; Ahn, J.-H. Flexible graphene–PZT ferroelectric nonvolatile memory. *Nanotechnology* 2013, 24, 475202.

[82] Kim, S.M.; Song, E.B.; Lee, S.; Zhu, J.; Seo, D.H.; Mecklenburg, M.; Seo, S.; Wang, K.L. Transparent and flexible graphene charge-trap memory. *ACS Nano* 2012, 6, 7879-7884.

[83] Wang, S.; Pu, J.; Chan, D.S.H.; Cho, B.J.; Loh, K.P. Wide memory window in graphene oxide charge storage nodes. *Appl. Phys. Lett.* 2010, 96, 143109.

[84] Hong, S.K.; Kim, J.-E.; Kim, S.O.; Jin Cho, B. Non-volatile memory using graphene oxide for flexible electronics. *Nanotechnology (IEEE-NANO), 2010 10th IEEE Conference on* Year, 604-606.

[85] Jeong, H.Y.; Kim, J.Y.; Kim, J.W.; Hwang, J.O.; Kim, J.-E.; Lee, J.Y.; Yoon, T.H.; Cho, B.J.; Kim, S.O.; Ruoff, R.S. Graphene oxide thin films for flexible nonvolatile memory applications. *Nano Lett.* 2010, 10, 4381-4386.

[86] Kafy, A.; Sadasivuni, K.K.; Kim, H.C.; Akther, A.; Kim, J. Designing flexible energy and memory storage materials using cellulose modified graphene oxide nanocomposites. *Phys. Chem. Chem. Phys.* 2015.

[87] Li, R.; Sun, R.; Sun, Y.; Gao, P.; Zhang, Y.; Zeng, Z.; Li, Q. Towards formation of fibrous woven memory devices from all-carbon electronic fibers. *Phys. Chem. Chem. Phys.* 2015, 17, 7104-7108.

[88] An, B.W.; Kim, K.; Kim, M.; Kim, S.-Y.; Hur, S.-H.; Park, J.-U. Direct Printing of Reduced Graphene Oxide on Planar or Highly Curved Surfaces with High Resolutions Using Electrohydrodynamics. *Small* 2015, 11, 2263-2268.

[89] Seo, S.; Yoon, Y.; Lee, J.; Park, Y.; Lee, H. Nitrogen-Doped Partially Reduced Graphene Oxide Rewritable Nonvolatile Memory. *ACS Nano* 2013, 7, 3607-3615.

[90] Bertolazzi, S.; Krasnozhon, D.; Kis, A. Nonvolatile Memory Cells Based on MoS2/Graphene Heterostructures. *ACS Nano* 2013, 7, 3246-3252.

[91] Zhang, E.; Wang, W.; Zhang, C.; Jin, Y.; Zhu, G.; Sun, Q.; Zhang, D.W.; Zhou, P.; Xiu, F. Tunable Charge-Trap Memory Based on Few-Layer MoS2. *ACS Nano* 2015, 9, 612-619.

[92] Forrest, S.R. The path to ubiquitous and low-cost organic electronic appliances on plastic. *Nature* 2004, 428, 911-918.

[93] Reuss, R.H.; Chalamala, B.R.; Moussessian, A.; Kane, M.G.; Kumar, A.; Zhang, D.C.; Rogers, J.A.; Hatalis, M.; Temple, D.; Moddel, G.; Eliasson, B.J.; Estes, M.J.; Kunze, J.; Handy, E.S.; Harmon, E.S.; Salzman, D.B.; Woodall, J.M.; Alam, M.A.;

Murthy, J.Y.; Jacobsen, S.C.; Olivier, M.; Markus, D.; Campbell, P.M.; Snow, E. Macroelectronics: Perspectives on Technology and Applications. *Proc. IEEE* 2005, 93, 1239-1256.

[94] Lumelsky, V.J.; Shur, M.S.; Wagner, S. Sensitive skin. *IEEE Sens. J.* 2001, 1, 41-51.

[95] Ricker, T. Sony's rollable OLED display can wrap around a pencil, our hearts (video). AOL Tech. 2010, available at: http://www.engadget.com/2010/05/26/sonys-rollable-oled-display-can-wrap-around-a-pencil-our-heart/.

[96] Skillings, J. Samsung shows off Youm flexible display. CBS Interactive Inc. 2013, available at: http://www.cnet.com/news/sprint-puts-cramming-behind-it-with-50-million-settlement/.

[97] De Boeck, J. IoT: the Impact of things. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. T82-T83.

[98] Takenaka, T.; Inoue, H.; Hosomi, T.; Nakamura, Y. FPGA-accelerated Complex Event Processing. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C126-C127.

[99] Yamauchi, T.; Kondo, H.; Nii, K. Automotive Low Power Technology for IoT Society. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. T80-T81.

[100] Yano, K.; Akitomi, T.; Ara, K.; Watanabe, J.; Tsuji, S.; Sato, N.; Hayakawa, M.; Moriwaki, N. Profiting From IoT: The Key Is Very-Large-Scale Happiness Integration. . In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C24-C27.

[101] Turnquist, M.; Hiienkari, M.; Mäkipää, J.; Jevtic, R.; Pohjalainen, E.; Kallio, T.; Koskinen, L. Fully Integrated DC-DC Converter and a 0.4V 32-bit CPU with Timing-Error Prevention Supplied from a Prototype 1.55V Li-ion Battery. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C320-C321.

[102] Yamamoto, Y.; Makiyama, H.; Yamashita, T.; Oda, H.; Kamohara, S. Novel Single p+Poly-Si/Hf/SiON Gate Stack Technology on Silicon-on-Thin-Buried-Oxide (SOTB) for Ultra-Low Leakage Applications. In Symposium on Very Large Scale

Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. T170-171.

[103] Lee, A.; Chang, M.-F.; Lin, C.-C.; Chen, C.-F.; Ho, M.-S.; Kuo, C.-C.; Tseng, P.-L.; Sheu, S.-S.; Ku, T.-K. RRAM-based 7T1R Nonvolatile SRAM with 2x Reduction in Store Energy and 94x Reduction in Restore Energy for Frequent-Off Instant-On Applications. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C76-C77.

[104] Kobayashi, M.; Hiramoto, T. Device Design Guideline for Steep Slope Ferroelectric FET Using Negative Capacitance in Sub-0.2V Operation: Operation Speed, Material Requirement and Energy Efficiency. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. T212-T213.

[105] Steegen, A. Technology innovation in an IoT Era. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C170-C171.

[106] Aitken, R.; Chandra, V.; Myers, J.; Sandhu, B.; Shifren, L.; Yeric, G. Device and technology implications of the Internet of Things. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Honolulu, HI, USA, 9-12 June 2014, pp.1-4.

[107] Ueki, M.; Takeuchi, K.; Yamamoto, T.; Tanabe, A.; Ikarashi, N.; Saitoh, M.; Nagumo, T.; Sunamura, H.; Narihiro, M.; Uejima, K.; Masuzaki, K.; Furutake, N.; Saito, S.; Yabe, Y.; Mitsuiki, A.; Takeda, K.; Hase, T.; Hayashi, Y. Low-Power Embedded ReRAM Technology for IoT Applications. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. T108-T109.

[108] Whatmough, P.-N.; Smart, G.; Das, D.; Andreopoulos, Y.; Bull, D. M. A 0.6V All-Digital Body-Coupled Wakeup Transceiver for IoT Applications. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C98-C99.

[109] Tanakamaru, S.; Yamazawa, H.; Takeuchi, Ken. Privacy-Protection Solid-State Storage (PP-SSS) System: Automatic Lifetime Management of Internet-Data's Right to be Forgotten. In Symposium on Very Large Scale Integration, Digest of Technical Papers, Kyoto, Japan, 15-18 June 2015, pp. C130-C131.

[110] Antonio, C.; Barrera, C. Flexible microstrip antennas. *Proc. SPIE* 2013, 8730, 873009.

[111] Ahmed, S.; Tahir, F.A.; Shamim, A.; Cheema, H.M. A Compact Kapton-based Inkjet Printed Multiband Antenna for Flexible Wireless Devices. *IEEE Antenn. Wirel. PR.* 2015.

[112] Inui, T.; Koga, H.; Nogi, M.; Komoda, N.; Suganuma, K. A Miniaturized Flexible Antenna Printed on a High Dielectric Constant Nanopaper Composite. *Adv. Mater.* 2015, 27, 1112-1116.

[113] Nicolas, T.; Philippe, C.; Ronan, S.; Vincent, S.; Hiroyuki, F. Polydimethylsiloxane membranes for millimeter-wave planar ultra flexible antennas. *J. Micromech. Microeng.* 2006, 16, 2389.

[114] Khaleel, H.R.; Al-Rizzo, H.M.; Rucker, D.G. Compact Polyimide-Based Antennas for Flexible Displays. *J. Display Technol.* 2012, 8, 91-97.

[115] Garg, D.P.; Anderson, G.L. Research in active composite materials and structures: an overview. *Proc. SPIE* 2000, 3992, 2-12.

[116] Li, J.; Zhao, Y.; Tan, H.S.; Guo, Y.; Di, C.-A.; Yu, G.; Liu, Y.; Lin, M.; Lim, S.H.; Zhou, Y. A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* 2012, 2, 754.

[117] Kang, I.; Yun, H.-J.; Chung, D.S.; Kwon, S.-K.; Kim, Y.-H. Record high hole mobility in polymer semiconductors via side-chain engineering. *J. Am. Chem. Soc.* 2013, 135, 14896-14899.

[118] Caraveo-Frescas, J.; Khan, M.; Alshareef, H. Polymer ferroelectric field-effect memory device with SnO channel layer exhibits record hole mobility. *Sci. Rep.* 2014, 4, 5243.

[119] Min, S.-Y.; Kim, T.-S.; Kim, B.J.; Cho, H.; Noh, Y.-Y.; Yang, H.; Cho, J.H.; Lee, T.-W. Large-scale organic nanowire lithography and electronics. *Nat. Commun.* 2013, 4, 1773.

[120] Yuan, Y.; Giri, G.; Ayzner, A.L.; Zoombelt, A.P.; Mannsfeld, S.C.; Chen, J.; Nordlund, D.; Toney, M.F.; Huang, J.; Bao, Z. Ultra-high mobility transparent

organic thin film transistors grown by an off-centre spin-coating method. *Nat. Commun.* 2014, 5, 3005.

[121] Yang, Y.; Yang, H.; Yang, M.; Shen, G.; Yu, R. Amperometric glucose biosensor based on a surface treated nanoporous ZrO_2/chitosan composite film as immobilization matrix. *Analytica Chimica Acta* 2004, 525, 213-220.

[122] Kim, S.H.; Hong, K.; Xie, W.; Lee, K.H.; Zhang, S.; Lodge, T.P.; Frisbie, C.D. Electrolyte-Gated Transistors for Organic and Printed Electronics. *Adv. Mater.* 2013, 25, 1822-1846.

[123] Oh, C.H.; Shin, H.J.; Nam, W.J.; Ahn, B.C.; Cha, S.Y.; Yeo, S.D. 21.1: Invited Paper: Technological Progress and Commercialization of OLED TV. *Dig. Tech. Pap. - Soc. Inf. Disp. Int. Symp.* 2013, 44, 239-242.

[124] Zhai, Y.; Mathew, L.; Rao, R.; Xu, D.; Banerjee, S.K. High-performance flexible thin-film transistors exfoliated from bulk wafer. *Nano Lett.* 2012, 12, 5609-5615.

[125] Shahrjerdi, D.; Bedell, S.; Khakifirooz, A.; Fogel, K.; Lauro, P.; Cheng, K.; Ott, J.; Gaynes, M.; Sadana, D. Advanced flexible CMOS integrated circuits on plastic enabled by controlled spalling technology. In IEEE International Electron Devices Meeting, San Francisco, CA, USA, 10-13 December 2012, pp. 5.1. 1-5.1. 4.

[126] Murray, C.E.; Saenger, K.; Kalenci, O.; Polvino, S.; Noyan, I.; Lai, B.; Cai, Z. Submicron mapping of silicon-on-insulator strain distributions induced by stressed liner structures. *J. Appl. Phys.* 2008, 104, 013530-013538.

[127] Hu, S. Film-edge-induced stress in substrates. *J. Appl. Phys.* 1979, 50, 4661-4666.

[128] Bedell, S.W.; Shahrjerdi, D.; Hekmatshoar, B.; Fogel, K.; Lauro, P.A.; Ott, J.A.; Sosa, N.; Sadana, D. Kerf-less removal of Si, Ge, and III–V layers by controlled spalling to enable low-cost PV technologies. *IEEE J. Photovolt.* 2012, 2, 141-147.

[129] Ghoneim, M.T.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Additive advantage in characteristics of MIMCAPs on flexible silicon (100) fabric with release-first process. *Phys. Status Solidi RRL* 2014, 8, 163-166.

[130] Seo, J.; Han, K.; Youn, T.; Heo, H.-E.; Jang, S.; Kim, J.; Yoo, H.; Hwang, J.; Yang, C.; Lee, H. Highly reliable M1X MLC NAND flash memory cell with novel

active air-gap and p+ poly process integration technologies. In IEEE International Electron Devices Meeting, Technical Digest, Washington, DC, USA, 9-11 December 2013, pp. 3.6.1-3.6.4.

[131] Ghoneim, M.T.; Fahad, H.M., Hussain, A. M., Rojas, J.P.; Torres Sevilla, G.A.; Alfaraj, N.; Lizardo, E.B.; Hussain, M.M. Enhanced cooling in mono-crystalline ultra-thin silicon by embedded micro-air channels. *AIP Adv.* 2015, 5, 127115.

[132] Takahashi, K.; Terao, H.; Tomita, Y.; Yamaji, Y.; Hoshino, M.; Sato, T.; Morifuji, T.; Sunohara, M.; Bonkohara, M. Current status of research and development for three-dimensional chip stack technology. *Jpn. J. Appl. Phys.* 2001, 40, 3032.

[133] Gao, S.; Dong, Z.; Kang, R.; Zhang, B.; Guo, D. Warping of silicon wafers subjected to back-grinding process. *Precis. Eng.* 2015, 40, 87-93.

[134] Jeon, E.-B.; Park, J.-D.; Song, J.H.; Lee, H.J.; Kim, H.-S. Bi-axial fracture strength characteristic of an ultra-thin flash memory chip. *J. Micromech. Microeng.* 2012, 22, 105014.

[135] Sekhar, V.N.; Shen, L.; Kumar, A.; Chai, T.C.; Zhang, X.; Premchandran, C.; Kripesh, V.; Yoon, S.W.; Lau, J.H. Study on the Effect of Wafer Back Grinding Process on Nanomechanical Behavior of Multilayered Low-K Stack. *IEEE Trans. Compon. Packag. Manuf. Technol.* 2012, 2, 3-12.

[136] Lu, S.-T.; Chen, W.-H. Reliability and flexibility of ultra-thin chip-on-flex (UTCOF) interconnects with anisotropic conductive adhesive (ACA) joints. *IEEE Trans. Adv. Packag.* 2010, 33, 702-712.

[137] Liu, Z.; Huang, Y.; Xiao, L.; Tang, P.; Yin, Z. Nonlinear characteristics in fracture strength test of ultrathin silicon die. *Semicond. Sci. Technol.* 2015, 30, 045005.

[138] Paul, I.; Majeed, B.; Razeeb, K.; Barton, J. Statistical fracture modelling of silicon with varying thickness. *Acta Mater.* 2006, 54, 3991-4000.

[139] Wu, J.; Huang, C.; Liao, C. Fracture strength characterization and failure analysis of silicon dies. *Microelectron. Reliab.* 2003, 43, 269-277.

[140] Boyd, E.J.; Uttamchandani, D. Measurement of the Anisotropy of Young's Modulus in Single-Crystal Silicon. *J. Microelectromech. Syst.* 2012, 21, 243-249.

[141] Committee, I.R. International Technology Roadmap for Semiconductors: 2013 Edition Executive Summary. *Semiconductor Industry Association, San Francisco, CA, available at: http://www. itrs.net/Links/2013ITRS/2013Chapters/2013ExecutiveSummary. pdf* 2013.

Chapter 2 Reliability of Flexible High-k/Metal Gate Devices

In this chapter, we study the electrical and mechanical reliability of high- κ Al_2O_3 gate stacks by conducting accelerated tests on the metal-oxide-semiconductor capacitor structure and monitoring its response.

First, we report on the electrical study of the high-κ/metal gate metal oxide semiconductor capacitors (MOSCAPs) on a flexible ultra-thin (25 μm) silicon fabric which is peeled off using a CMOS compatible process from a standard bulk mono-crystalline (100) silicon substrate. A lifetime projection is extracted using statistical analysis of the ramping voltage (Vramp) breakdown and time dependent dielectric breakdown (TDDB) data. Then, we study the effect of mechanical stress on the devices' electrical behavior.

2.1. Device Fabrication

Our process is standard complementary metal oxide semiconductor (CMOS) compatible and generic to any pre-fabricated as well as post-fabricated devices [1-9]. Three uniquely distinguishable features of this process are (i) usage of the most conventional and commercially widely available low-cost bulk mono-crystalline silicon substrate, (ii) ultra-large-scale-integration density and high thermal budget compatibility, and (iii) cost effectiveness including recyclability of the same wafer for multiple production cycles. Although the process and its effectiveness to transform varieties of silicon electronics (metal-oxide-semiconductor capacitors and transistors, thermoelectric generators, micro-lithium ion battery, laterally actuated micro-electro-mechanical systems based thermal actuator, etc.) into a flexible, semi-transparent one have been chronicled in various publications in the past, just a brief introduction is presented here.

We start with any substrate or chip where the devices are already fabricated retaining the intended performance-energy-cost effectiveness, ultra-large scale-integration density, and high thermal budget processes as required. The p-type, 4-inch silicon substrate used in this work is lightly doped with boron. The gate stacks in the MOSCAPs are deposited with an atomic layer deposited (ALD) 10 nm aluminum oxide (Al_2O_3) high-κ dielectric, and a 20 nm tantalum nitride (TaN) metal gate. Aluminum (Al) is used as a contact metal (Figure 2.1.1 parts a through f). Then, we lithographically pattern the resist to expose the areas where the release holes are to be formed. With reactive ion etching (RIE), we make trenches through the interlayer dielectric (ILD) layers to expose the silicon substrate. Next, we perform a selective (to oxide or other insulating layers used in ILD) deep reactive ion etching (DRIE) to make trenches in the silicon (Figure 2.1.1g). Subsequently, we form a vertical sidewall to especially cover the silicon sidewalls (of the trenches). Next, we use a xenon di-fluoride (XeF_2) based isotropic etching process to form caves inside the silicon. When the wall between adjacent caves is etched, the top portion of the silicon substrate with the pre-fabricated devices detaches, releasing a flexible silicon fabric (Figure 2.1.1h). In the present experiment, the fabric is 25 μm thick and has an area of 6 cm^2 (Figure 2.1.2).

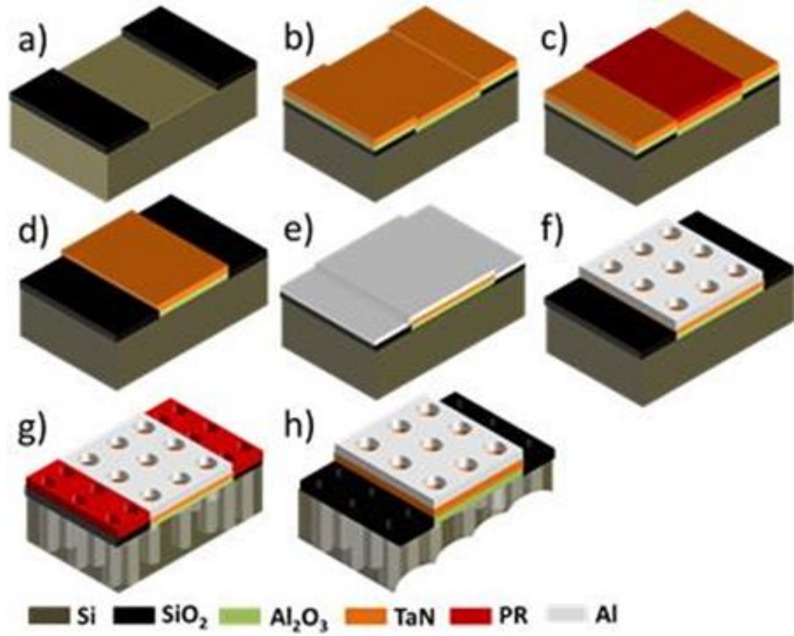


Figure 2.1.1: Main fabrication steps of MOSCAPs on flexible silicon.

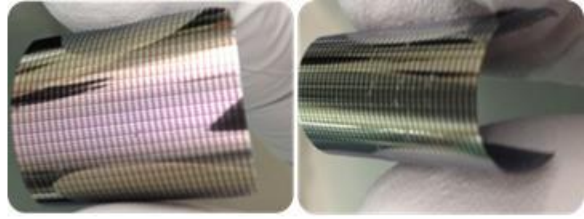


Figure 2.1.2: Digital photo of the actual fabricated MOSCAPs on flexible ultra-thin Si fabric.

2.2. Electrical Characterization

Fabricated MOSCAPs were characterized using capacitance voltage (C-V) measurements at low and high frequencies. We also extracted the parasitic capacitances. The C-V curves were collected using an E4980A Precision LCR Meter (Agilent Technologies), with a 30 mV small AC signal superimposed on a direct current (DC) voltage bias. Figure 2.2.1 shows the normalized capacitance of the flexible and inflexible devices, with flexible devices having a smaller effective area as there are 25 holes of the radius of 5 μm (i.e. 80% of total area) through the gate stack of each flexible device. The

figure shows common C-V behavior in terms of accumulation (<–2V), depletion (–2V→ +2V), and inversion (> +2V) regions, as well as a reduction in inversion capacitance due to the minority carriers' inability to follow the AC signal at higher frequencies.

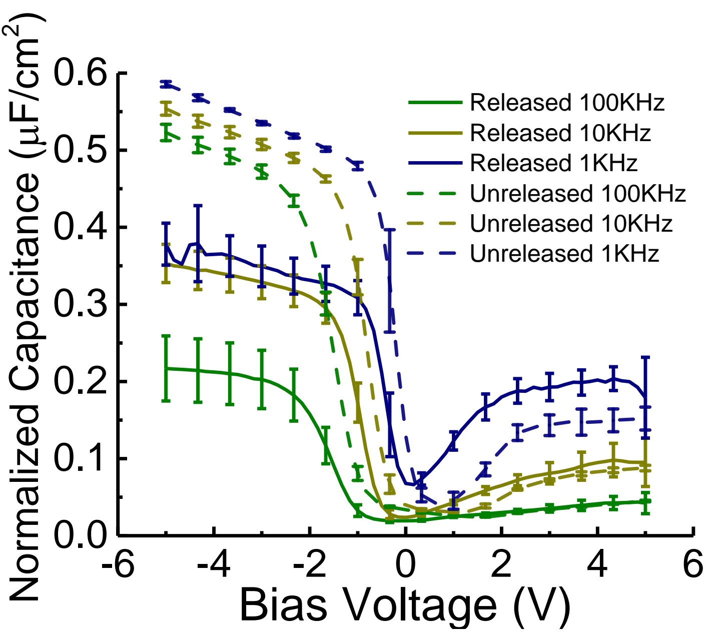


Figure 2.2.1: Normalized C-V curves for flexible and inflexible MOSCAPs at different frequencies.

Although the frequency response in both types of devices is similar, the features in accumulation differ due to a difference in the properties of the inflexible silicon bulk and the ultra-thin fabric of the released flexible silicon. We can infer that, due to a poor contact between the bottom chuck and thin silicon fabric, the released device is more sensitive to the C-V frequency. There is an overall degradation in the normalized capacitance ranging from 30% at 1 KHz to 50% at 100 KHz, and a failure to operate at 1 MHz. It is also observable that, whereas the accumulation (below ~ –2V) charge of flexible devices has a lower value, and is more dispersed relative to bulk devices, the behavior is reversed in the inversion region (above ~ +2V) where the capacitance values

of flexible devices are slightly higher than their bulk counterparts. This result implies that the generated traps and defects due to the release trenches have a net negative polarity. This negative polarity imposes a frequency limitation on our flexible devices associated with the drop in capacitance value as frequency increases. This result can be explained by the difference in the nature of our flexible silicon fabric compared to that of bulk silicon. The substrate is lightly doped, i.e. its resistivity is 11-20 Ω.cm, and a limited number of free carriers are available. In the inversion region, because of the limited amount of free charges in the lightly doped substrate and its relatively high resistivity, the ability of charges to follow-up the fast changing voltage decreases. This inability of charges to respond is evident in the C-V curves from the drop in inversion capacitance maximum as the frequency of the voltage signal increases. In flexible silicon, the available carriers are not only limited by the light doping level but also the limited supply of free carriers at the poor contact between the bottom chuck and the silicon fabric. This limitation amplifies the drop in capacitance phenomenon, that the accumulation mode maximum capacitance is also degraded as voltage signal frequency increases. The relative drop between flexible and inflexible capacitance is 30% at 1 KHz, and 50% at 100 KHz. This poor contact can be attributed to the non-planar bottom of the silicon fabric resulting from the isotropic etching release step (Figure 2.2.2). Still, this limitation can be overcome by using a silicon-on-insulator (SOI) type substrate where the non-planar bottom formation will be inhibited by the presence of a ceiling buried oxide (BOX) layer, or an all front contact scheme can eliminate the problem but at the cost of more real estate. The frequency dispersion can also result from high interface defect density (D_{it}). Equation (1) shows how D_{it} is calculated.

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{C_{lf}}{C_{ox} - C_{lf}} - \frac{C_{hf}}{C_{ox} - C_{hf}}\right) \quad (1)$$

Using the oxide capacitance in the accumulation region (C_{ox}) and the capacitances in the inversion region at the lowest and highest available frequencies (C_{lf} and C_{hf}, respectively), we find that D_{it} for flexible devices is 3.8 x 10^{11} $cm^{-2}eV^{-1}$. For bulk inflexible devices, D_{it} is 1.6 x 10^{11} $cm^{-2}eV^{-1}$. Therefore, the interface defects density for flexible devices is ~137% higher than that of the inflexible ones. This result can be attributed to the structural features associated with the presence of a network of release holes.

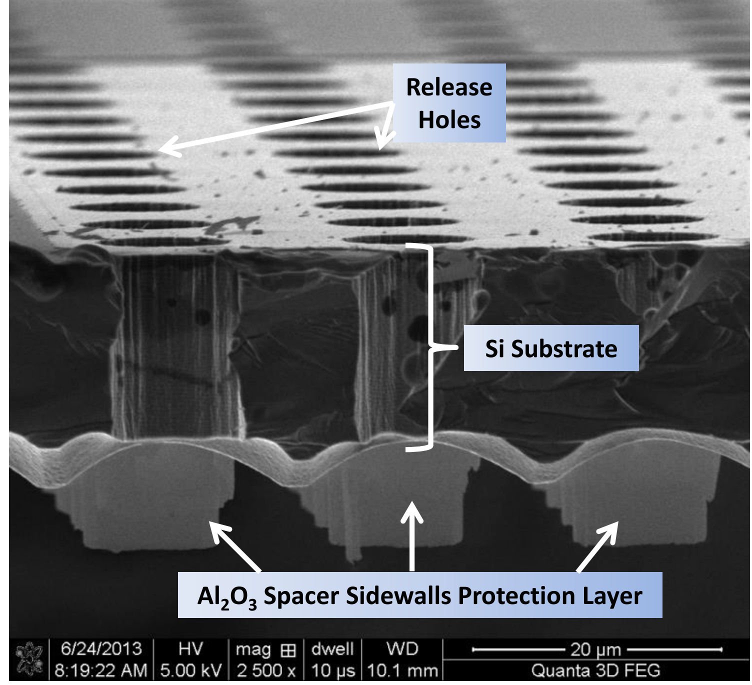


Figure 2.2.2: The scanning electron microscope image of the thin silicon fabric showing the scallops at the bottom of the structures, which might be caused by the release processing step.

To solve this dilemma, capacitance was corrected for series resistance (R_{series}). The plot in Figure 2.2.1 is for capacitance measurement using the parallel equivalent

circuit model (C_p) with a dissipation factor (D). The conductance (G_p) is calculated using (2), and R_{series} is calculated using (3) [10].

$$G_p = D\omega C_p \qquad (2)$$

$$R_{series} = \frac{\left[\frac{G_p}{\omega C_p}\right]^2}{\left[1+\left[\frac{G_p}{\omega C_p}\right]^2\right]G_p} \qquad (3)$$

R_{series} was calculated using (3) at different frequencies ($\omega = 2\pi f$). The results of R_{series} at -5 V (deep accumulation) are shown in Table 2.2.1. The higher values of R_{series} for flexible devices are attributed to the non-planar bottom shown in Figure 2.2.2. Figure 2.2.3 shows the modified version of the C-V plot after accounting for series resistance. Although there is observable improvement in the frequency dispersion, it can be deduced that the remaining dispersion is due to intrinsic properties of the high-κ Al_2O_3 rather than extrinsic factors.

Table 2.2.1: Series resistance values for released and bulk devices at different small signal excitation frequencies

Frequency	1 kHz	10 kHz	100 kHz	1 MHz
R_{series} (released)	321 kΩ	57 kΩ	37 kΩ	26 kΩ
R_{series} (bulk)	91 kΩ	16 kΩ	2 kΩ	1 kΩ

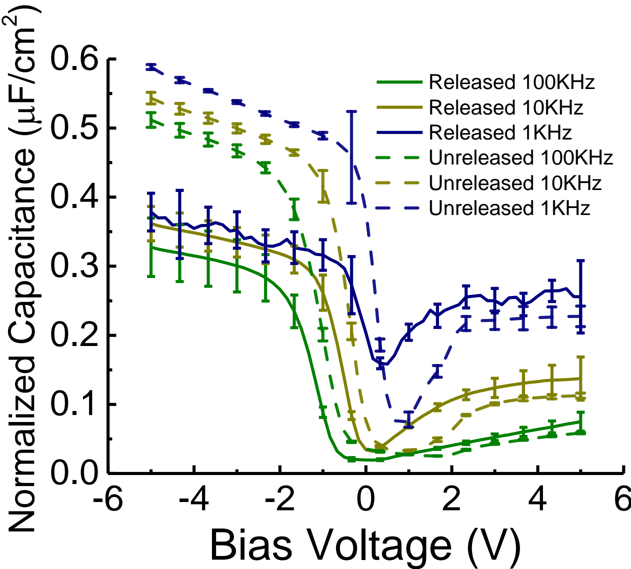


Figure 2.2.3: Normalized C-V curves for flexible and inflexible devices corrected for series resistance.

Dummy MOSCAPs with 300 nm thermal SiO_2 dielectric are used to extract parasitic capacitance (capacitance due to the external cables and connections that does not pertain to the actual device). If we examine dummy MOSCAPs fabricated on the same wafer with released and unreleased devices (Figure 2.2.4, corrected for series resistance), we observe that there is almost no frequency dispersion in the unreleased dummy MOSCAPs. The Si-SiO_2 interface has very low defect density for thermal oxide, and as a result, there is no frequency dispersion. On the other hand, we notice that the released dummy devices exhibit frequency dispersion. Excluding the series resistance effect and the SiO_2 interfacial defects (based on the non-dispersed unreleased dummy devices), we can attribute this dispersion to the etching holes covered with Al_2O_3 sidewalls in the active area of the devices leading to the introduction of significant defects in the oxide. Therefore the high-κ Al_2O_3 has a high defect density, leading to mild dispersion in unreleased actual MOSCAPs as shown in Figure 2.2.3, and calculated in

previous D_{it} calculations, while the presence of release holes and Al_2O_3 spacers introduces significant defects in dummy MOSCAPs (Figure 2.2.4). Finally, both the defective high-κ Al_2O_3 and the release holes introduced defects lead to severer dispersion, as shown in released MOSCAPs (Figure 2.2.3) and D_{it} calculations. However, today's technology might be more forgiving on this shortcoming thanks to today's 10s or 100s of nanometers technology nodes, as then the release trenches do not need to go through the active areas. Hence, these results can be more of a guideline for our release process than a frequency imposed limitation because, without holes in active areas, D_{it} is only mandated by the material system and fabrication processes which can be optimized without interfering with our release process.

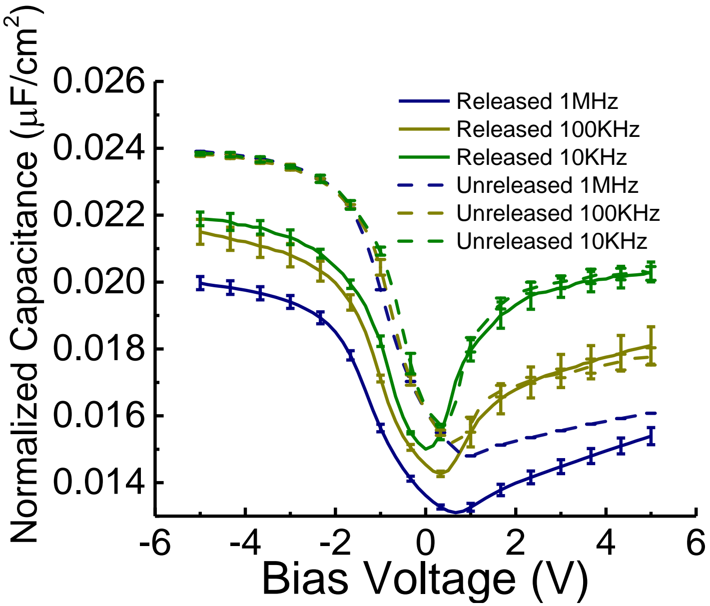


Figure 2.2.4: Normalized C-V curves for flexible and inflexible dummy MOSCAPs at different frequencies.

2.3. Electrical Reliability Analysis

Reliability analysis was done by executing the V_{ramp} test on 20 devices with 200 mV increments. V_{bd} was then determined as the median value which coincided with the

value of most occurrences. After determining V_{bd}, TDDB measurements were done at three different stress voltages (±200 mV incremented to 85% of V_{bd}). However, using 85% of V_{bd} for flexible devices resulted in immediate breakdown in 10s of seconds; hence, the values have been reduced to 72% for flexible devices. Each constant stress voltage was applied to 10 devices to construct a single line on a Weibull distribution $(ln(-ln(1-F))$ versus time plot, where F is the fraction of the device number, arranged in ascending order with respect to time-to-breakdown (t_{bd}), divided by the total number of measured devices at the same stress voltage. From the Weibull plot, the value of t_{bd} corresponding to F = 0.63 $(ln(-ln(1-F)) = 0)$ is extracted for lifetime projections.

In the V_{ramp} breakdown measurements, devices were subjected to incremental increases in gate voltage until the dielectric breakdown (determined as greater than an order of magnitude leakage current increase) occurs (Figure 2.3.1). The inset shows a histogram for extracting the average value of most occurrences. This value is carried forward to be used as a stress voltage in the constant voltage stress (CVS) measurements in the TDDB study. The actual voltage drop across the gate dielectric is actually lower than the applied voltage because some voltage is dropped across the bottom chuck and lightly doped p-type substrate. To quantify this drop for the purpose of obtaining accurate reliability projections, we calculate the built-in voltage drop (V_{bi}).

$$V_{bi} = \varphi_m - \varphi_{p-si} \qquad (4)$$

φ_m is the work function of the metal-stainless steel in volts (~4.7 V [11]), and φ_{p-si} is the work function of the p-type silicon in volts (2.194 V), calculated using (5), and (6).

$$E_{FV,p-si} = -K_B T \; x \; ln\,(\frac{p}{N_v}) \qquad (5)$$

$$q\varphi_{p-si} = q\chi_{si} + E_{g,si} - E_{FV,p-si} \qquad (6)$$

The difference between the Fermi level energy and the valence band energy of p-type silicon ($E_{FV,p-si}$ ~0.296 eV) is calculated using the background thermal energy ($K_B T\sim$ 0.026 eV at 300 k), the Boron doping concentration ($p\sim$ 2.2 x 10^{14} cm^{-3} [12]), and the valence band effective density of states (N_v~3.1 x $10^{19}cm^{-3}$ [13]). The work function of the p-doped silicon then reduces to simple addition between the electron affinity of Si ($q\chi_{si}$ ~1.39 eV), the forbidden band gap of Si ($E_{g,si}$~1.1 eV), and $E_{FV,p-si}$ calculated in (5). Using (6) to calculate φ_{p-si} , and plugging the result into (4), gives V_{bi} of ~ 2.5 V. In Figure 2.3.1, we observe that, until 0-7 volts, there is no physical damage in the material as evident by all the appended sweeps for 0-3, 0-5, 0-6 volts following the same slope patterns. Then, at the 0-8 volts sweep, we see the wear out phase leading to breakdown characterized by a very steep slope, until reaching a set current compliance limit. The subsequent 0-9 volt sweep confirms that the material was indeed permanently damaged (hard breakdown) because the initial current value at 0.1V is very high while the current exhibits Ohmic-like behavior.

Under a continuous stress, a random creation of defects contributing to the electron transport through the dielectric occurs, culminating in the run-away defect generation process [14]. At this stage, a permanent conductive path between the top electrode and bottom semiconductor through the dielectric is formed. The average applied voltage at which breakdown occurs is 9.43 V for released devices compared to 9 V for unreleased (corresponding to an effective E-filed of 6.93 MV/cm, and 6.50 MV/cm

on the dielectric in released, and unreleased devices, respectively after deducting V_{bi} at the backside contact).

TDDB and lifetime projections are then carried out. Figure 2.3.2a shows TDDB data for flexible devices at different CVS values. Clearly, as the stress voltage increases, the initial leakage current increases, and t_{bd} decreases significantly. The observed decrease in the leakage current during the initial stress time period is due to the continuous trapping of injected electrons in the high-κ film [15].

Similar measurements have been performed on 10 released devices, and the Weibull distribution plot [Figure 2.3.2b] was constructed to extract the 63% t_{bd} value to be used in lifetime projections [Figure 2.3.2c]. From the linear fit (based on the electric field driven primary degradation mode) in Figure 2.3.2b, the safe operating voltage (V_{Safe}) for released devices would be <5V, which is acceptable for most integrated circuits as technology scaling is heading in the direction of reducing supply voltages to 1 V and lower. Similarly, Figure 2.3.3 parts (a) through (c) represent an example of (a) the TDDB plot for the unreleased devices stressed at 7.8 V, 7.65 V, and 7.45 V; (b) the corresponding Weibull distribution plot for the t_{bd} extraction; and (c) lifetime projections.

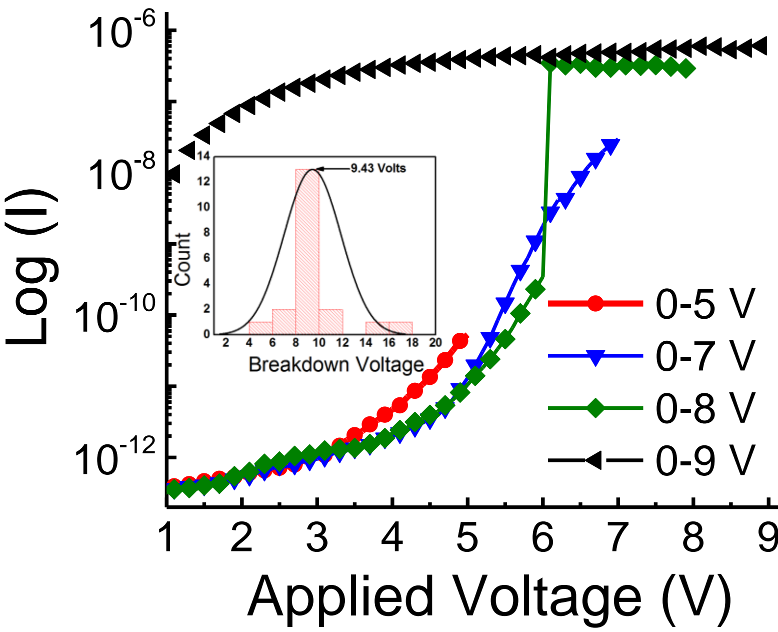


Figure 2.3.1: The current-voltage dependencies for the subsequent applied $_{Vramp}$ measurements with a 1V increment. Inset: the histogram of V_{bd} values obtained on tested devices.

These plots show that the unreleased devices pass the ten years benchmark at <6 V (exceeding the released devices by 1V). However, the lightly doped wafer had a resistivity in the range of 11-20 Ω.cm. Because the devices are back gated, there is a voltage drop across the Si bulk. This lost voltage is 20 times higher for the unreleased devices compared to the released ones because the bulk silicon is 500 µm thick compared to 25 µm of the released fabric. Hence, although the stress voltage is higher for unreleased devices, a higher portion of the applied voltage drops in the silicon bulk, resulting in a much lower stress voltage applied to the gate stack (detailed calculations provided in next paragraphs).

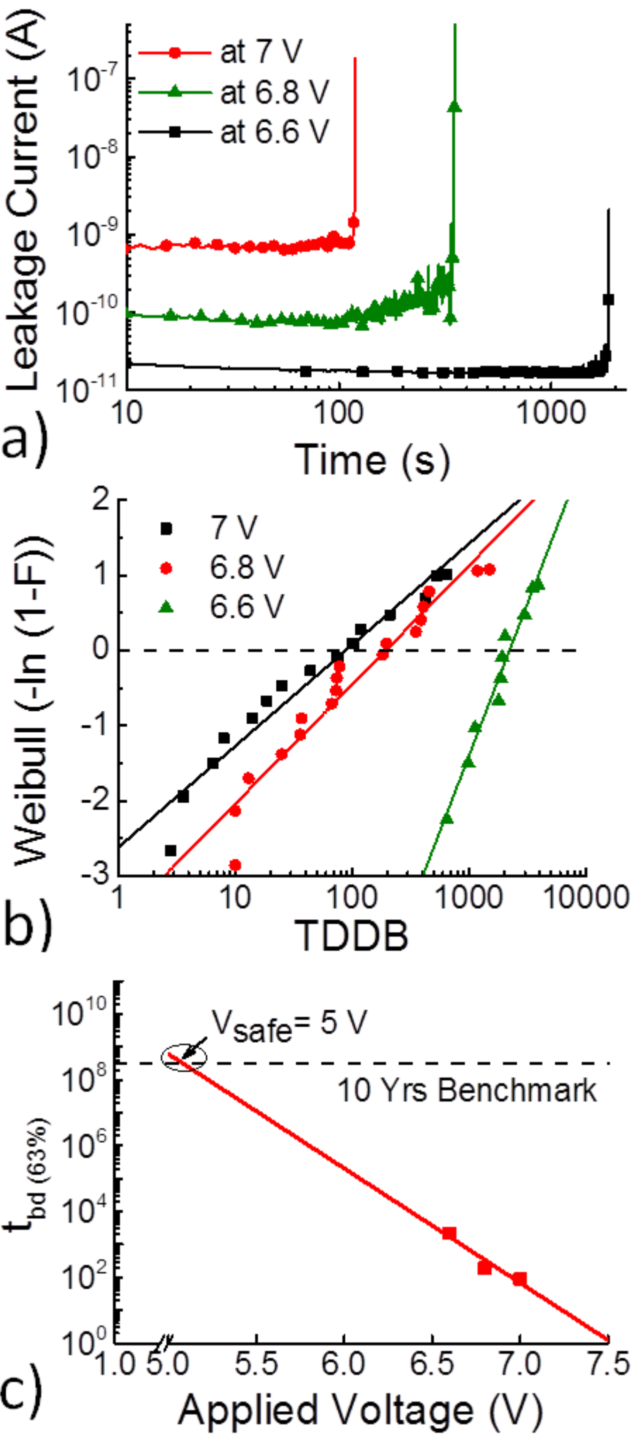


Figure 2.3.2: a) Sample constant stress voltages (CVS) measurements performed on flexible devices, b) corresponding Weibull distributions, and c) lifetime projection plot.

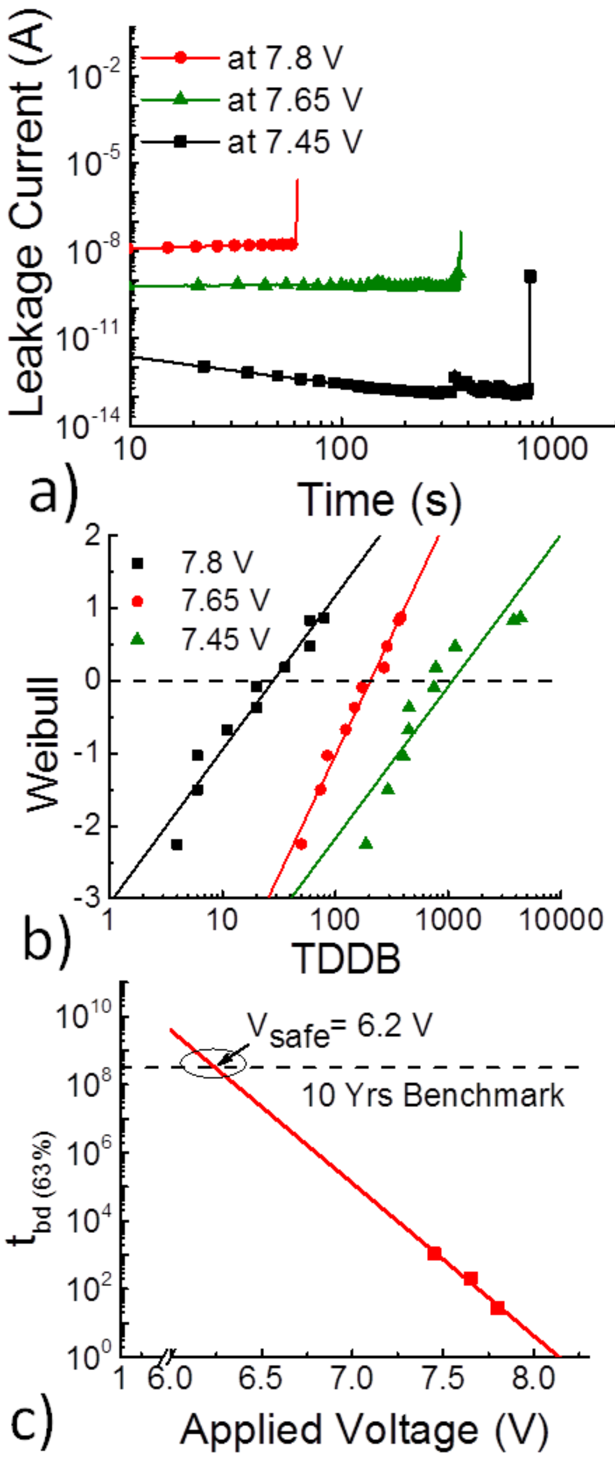


Figure 2.3.3: a) Constant stress voltages (CVS) measurements on unreleased inflexible devices, b) corresponding Weibull distributions, and C) lifetime projections plot.

Overall, the actual voltage stressing the dielectric in the released device case is higher than that for unreleased counterparts due to the larger voltage drop across the lightly doped Si bulk. Moreover, the employed extrapolation model for lifetime projection uses a conservative linear on a semi-log scale fitting, comparing to the power-law model (lifetime α V^{-n}) fitting which would lead to a significantly higher lifetime for the same operational voltage [16]. Note that, in both cases, the range of the used stressing voltage values might be too narrow comparing to the intercept at the ten years benchmark voltage value [16-19]. The selection of stress voltages is done based on practical considerations; they are chosen to result in a breakdown around a few thousand seconds, then further readings at +/- 200 mV increments are taken.

Although the above reliability analysis allows us to make certain conclusions regarding the difference between the flexible and inflexible MOSCAPs, a closer look at the dielectric reliability irrespective of the probing setup would enable discerning the variation in the dielectric physical properties due to the flexing process. To achieve that result, we define the effective voltage (V_{eff}) as the voltage across the dielectric, which can be calculated using a simple voltage divider (7), while the MOSCAP can be modelled as in Figure 2.3.4.

$$V_{eff} = (V_{app} - V_{bi})x \frac{R_{Dielectric}}{R_{Dielectric} + R_{Silicon\ Body}} \quad (7)$$

where V_{app} is the actual applied back gate voltage, V_{bi} is the built-in voltage drop at the metal chuck and the p-type Si interface due to the difference between the work function of the metal and the electron affinity of the p-type Si, $R_{Dielectric}$ is the resistance of the dielectric, and $R_{Silicon\ Body}$ is the resistance of the Si bulk.

$$R_{Dielectric} = \rho_{Dielectric} \; x \; \frac{t_{Dielectric}}{A_{Device}} \quad (8)$$

$$R_{Silicon\ Body} = \rho_{Silicon\ Body} \; x \; \frac{t_{Silicon\ Body}}{A_{Device}} \quad (9)$$

where ρ and t are the resistivity in Ω.cm, and thickness of the corresponding materials, respectively. $\rho_{Dielectric}$~ 10^{14} Ω.cm for Al_2O_3, $\rho_{Silicon\ Body}$~15.5 Ω.cm for lightly doped p-type Si, A_{Device} is device area (which does not contribute in effective voltage calculation), $t_{Dielectric}$ = 10 nm, and $t_{Silicon\ Body}$ = 500 μm and 25 μm for the inflexible and flexible MOSCAPs, respectively. Plugging these values into (7) through (9), we find that the effective voltage across the flexible and inflexible devices is 99.99% of the applied voltage. This happens because of the negligible resistance of the Si body compared to that of the much higher dielectric resistance. Therefore, the series resistance effect due to changes in the Si thickness can be safely neglected.

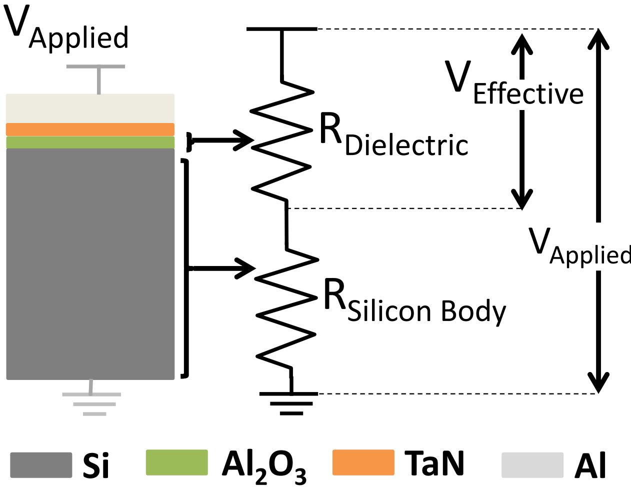


Figure 2.3.4: Modelling of back gated MOSCAPs in terms of series resistances.

2.4. Mechanical Reliability Analysis

Next, we studied the impact of mechanical stress on the high-κ/metal-oxide-semiconductor capacitors built on flexible silicon (100) fabric. The mechanical tests include studying the effect of bending radius up to 5 mm minimum bending radius with respect to breakdown voltage and leakage current of the devices. We also report the effect of continuous mechanical stress on the breakdown voltage over extended periods of times. Specifically, we study the effect of external mechanical strain at different bending radii and time of strain at specific bending angles on the breakdown voltage of the flexible MOSCAP devices. This is especially important since in many biomedical applications, for example, to monitor vital signs of body organs, the flexible devices are actually bent most of the time.

Figure 2.4.1 shows the variation in the average breakdown voltage with different bending radius corresponding to varying a nominal strain ($\varepsilon_{nominal} = t/2R$, t is the substrate thickness and R is the bending radius), the inset depicts the bending measurements test structures. The five x ten millimeter-squared silicon piece hosting MOSCAPs (100x100 μm^2 – 250 x 250 μm^2 areas) was fitted on top of the curved structures, with devices facing upwards, and fixed from edges using Kapton tape. The plot shows that the average breakdown voltage increases with the increased applied strain, reaching a 200% increase at $\varepsilon_{nominal}$ of 0.25%. This was observed in the past too as self-healing property of Al_2O_3 [20] where Al_2O_3 thin films exhibit lower leakage currents on subsequent sweeps and explained by an electrical anneal phenomenon. In our case, more stressed bonds (due to higher strain at lower bending radius) initially pass higher currents leading to a similar electrical annealing step which heals the device and makes it less prone to breakdown.

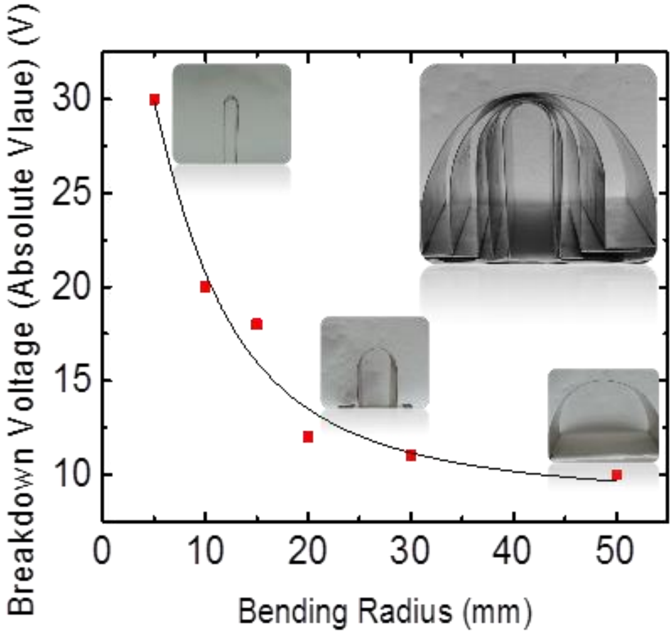


Figure 2.4.1: Average breakdown voltage of MOSCAPs versus bending radius.

Another important indication of the reliability of flexible devices is the leakage current, which have been monitored during the extended periods of time. Figure 2.4.2 shows the leakage current in flexible MOSCAPs at different stress voltages, as a percentage of the average breakdown voltage, over a time period of 6 days (5 x 10^5 s) while being bent at 5 mm bending radius ($\varepsilon_{nominal}$ = 0.25%). The trend shown in this plot indicates that the devices can safely operate at 75-85% of their breakdown voltage for little more than a day. The observed leakage current decrease over stress time is attributed to the significant charge trapping which is especially more prominent in Al_2O_3 high-κ dielectric. On the other hand operation at 95% of breakdown voltage shows an order of magnitude increase in leakage current which is indicative of a permanently damaged dielectric in TDDB test.

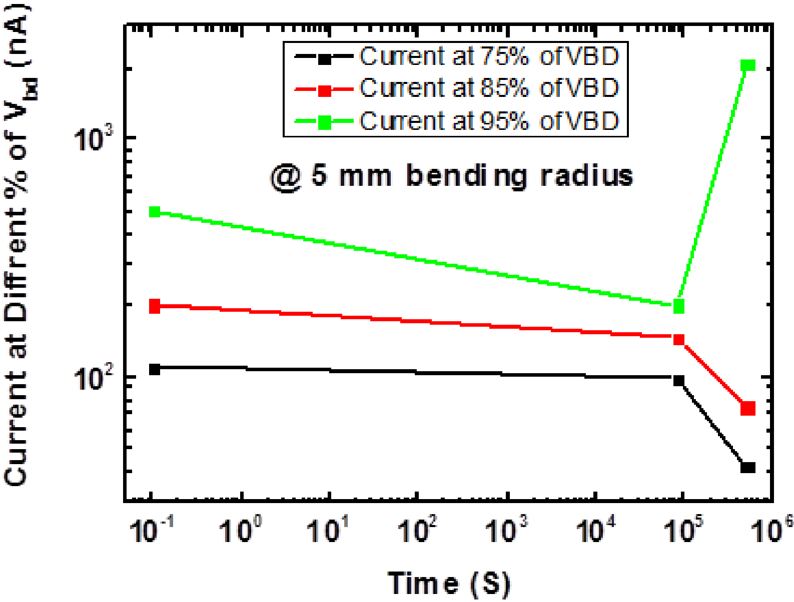


Figure 2.4.2: Leakage current versus time corresponding to different values of constant stress voltages.

Further mechanical assessment is performed to determine the durability of these devices when tampered mechanically. This is done by monitoring the breakdown voltage value of the devices after a number of bending cycles at the minimum bending radius of 5 mm corresponding to a 0.25% nominal strain. The bending steps were done manually to simulate a real environment where the devices are exposed to physical unbalanced perturbation due to an expanding heart, for instance.

Figure 2.4.3 shows the resulting breakdown voltage versus the number of bending manual cycles showing around 12% decrease in breakdown voltage after 50 cycles and complete failure after 100 cycles, This imposes a limitation on these flexible MOSCAPs as they cannot withstand multiple flexing and de-flexing cycles making them unsuitable for applications where frequent bending at 5 mm bending radius is required.

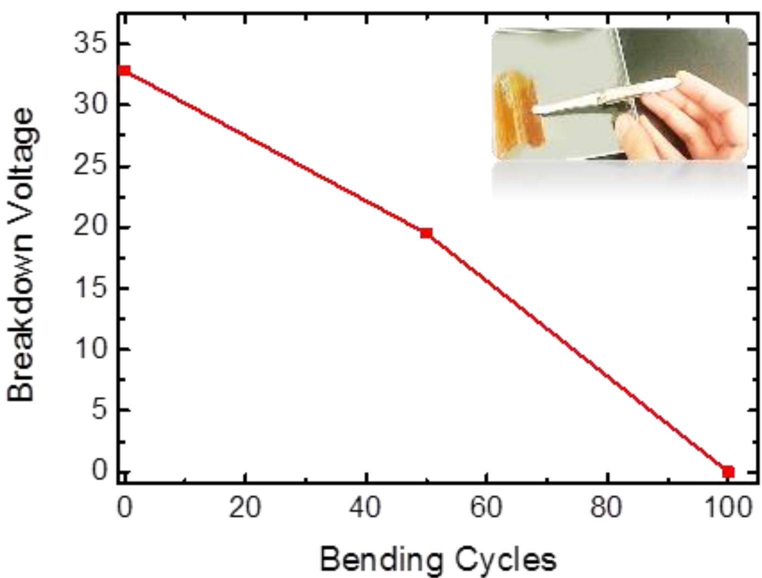


Figure 2.4.3: Breakdown voltage as a function of bending cycles. Inset: the samples are extended using the Kapton tape from both edges to enable manual bending of the sample at the center of the bending structure.

2.5. Conclusion

In summary, the released devices show acceptable operational voltages below 5 V compared to 6.2 V for bulk unreleased devices (degradation of ~ 19%). However, such magnitude of the operational voltage makes the degradation non-significant as today integrated circuits pursue operation voltages of around 1V to minimize power consumption. Moreover, calculations performed to assess the series resistance, due to substrate thickness differences between flexible (25 μm) and bulk (500 μm) stacks for back gated MOSCAPs, show negligible difference. Finally, the frequency response degradation of the flexible MOSCAPs is attributed to both a poor contact between the scalloped silicon fabric and the bottom electrode, and higher defects at the interface between holes and device active area hindering the ability of carriers to respond at higher frequencies. In addition, the devices can withstand higher voltages when bent at smaller bending radii (up to 5mm) for a small time, survive extended time periods under continuous mechanical stress, although can be exposed only to a limited number of

bending cycles. Hence, they are more suitable for applications where flexible devices are bent for long duration (static mechanical stress) than ones where continuous stressing/relaxing cycles repeatedly occur (dynamic stress), like when wrapped around a joint.

2.6. References

[1] Rojas, J. P.; Sevilla, G. T.; Hussain, M. M. Structural and electrical characteristics of high-k/metal gate metal oxide semiconductor capacitors fabricated on flexible, semi-transparent silicon (100) fabric. *Appl. Phys. Lett.* 2013, 102, 064102,.

[2] Rojas, J. P.; Hussain, M. M. Flexible semi-transparent silicon (100) fabric with high-k/metal gate devices. *Phys. Status Solidi RRL* 2013, 7, 187–191.

[3] Rojas, J. P.; Ghoneim, M. T.; Young, C. D.; Hussain, M. M. Flexible High-κ/Metal Gate Metal/Insulator/Metal Capacitors on Silicon (100) Fabric. *IEEE Trans. Electron Dev.* 2013, 60, 3305 -3309.

[4] J. P. Rojas, G. A. Torres Sevilla, and M. M. Hussain, "Can We Build a Truly High Performance Computer Which is Flexible and Transparent?" *Sci. Rep.*, vol. 3, pp. 2013.

[5] Ghoneim, M. T.; Rojas, J. P.; Hussain, A. M.; Hussain, M. M. Additive advantage in characteristics of MIMCAPs on flexible silicon (100) fabric with release-first process. *Phys. Status Solidi RRL* 2013, 163-166.

[6] Sevilla, G. T.; Inayat, S. B.; Rojas, J. P.; Hussain, A. M.; Hussain, M. M. Flexible and Semi-Transparent Thermoelectric Energy Harvesters from Low Cost Bulk Silicon (100). *Small* 2013, 9, 3916–3921.

[7] Ahmed, S. M.; Hussain, A. M.; Rojas, J. P.; Hussain, M. M. Solid state MEMS devices on flexible and semi-transparent silicon (100) platform. In 27th Int. Conf. on Microelectromech. Syst,, San Francisco, California, USA, 2014.

[8] Ghoneim, M. T.; Kutbee, A.; Nasseri, F. G.; Bersuker, G.; M. M. Hussain. Mechanical Anomaly Impact On Metal-oxide-semiconductor Capacitors On Flexible Silicon Fabric. *Appl. Phys. Lett.* 2014, 104, 234104.

[9] Ghoneim, M. T.; Zidan, M. A.; Salama, K. N.; Hussain, M. M. Towards Neuromorphic Electronics: Memristors on Foldable Silicon Fabric. *Microelectron. J.*, 2014, 45, 1392-1395.

[10] Nicollian, E. H.; Brews, J. R. *MOS Physics and Technology*, Wiley, New York (1982).

[11] Szadkowski, A. J.; Kalnitsky, A.; Ma, K. B.; Zukotynski, S. Implications of the change in work function of chromium by the presence of hydrogen on the properties of electrical contact between chromium and hydrogenated amorphous silicon. *J. Appl. Phys.* 1982, 53, 557-558.

[12] ASTM International Report: Designation: F 723 – 99.

[13] Green, M. A. Intrinsic concentration, effective densities of states, and effective mass in silicon. *J. Appl. Phys.* 1990, 67, 2944.

[14] Vandelli, L.; Padovani, A.; Larcher, L.; Bersuker, G. Microscopic modeling of electrical stress-induced breakdown in poly-crystalline hafnium oxide dielectrics. *IEEE Trans. Electron Dev.* 2013, 60, 1754 -1762.

[15] Bersuker, G.; Chowdhury, N.; Young, C.; Heh, D.; Misra, D.; Choi, R. Progressive breakdown characteristics of high-κ/metal gate stack. In Int. Rel. Phy., Phoenix, AZ, USA, 2007.

[16] Yoshida, C.; Sugii, T. Reliability study of magnetic tunnel junction with naturally oxidized MgO barrier. In Int. Rel. Phy., Anaheim, CA, USA, 2012.

[17] Shou-Chung, L.; Oates, A. S. Reliability of porous low-κ dielectrics under dynamic voltage stressing. In Int. Rel. Phy. Anaheim, CA, USA, 2012.

[18] Chen, F.; Parkinson, P.; McStay, I.; Settlemyer, K.; Reviere, R.; Tews, H.; Seitz, M.; Min-soo, K.; Ruprecht, M.; Jinghong, L.; Jammy, R.; Strong, A. Time-dependent dielectric breakdown evaluation of deep trench capacitor with sidewall hemispherical, polysilicon grains for gigabit DRAM technology. In Int. Integ. Rel. Wrks., 2002.

[19] Banerjee, P.; Ditali, A. Uniqueness in activation energy and charge-to-breakdown of highly asymmetrical DRAM Al_2O_3 cell capacitors. *Electron Device Lett.* 2004, 25, 574-576.

[20] Lu, C.-C.; Lin, Y.-C.; Yeh, C.-H.; Huang, J.-C.; Chiu, P.-W. High mobility flexible graphene field-effect transistors with self-healing gate dielectrics. *ACS Nano* 2012, 6, 4469-4474.

Chapter 3 Performance Analysis of High Performance Flexible Non-planar 3D FinFET CMOS

In this chapter, we present a comprehensive electrical performance assessment of hafnium silicate (HfSiOx) high-κ dielectric and titanium nitride (TiN) metal gate integrated FinFET-based complementary─metal─oxide semiconductor (CMOS) on flexible silicon-on-insulator (SOI). The devices were fabricated using state-of-the-art CMOS technology and then transformed into flexible form by using a CMOS-compatible mask-less deep reactive-ion etching (DRIE) technique. Mechanical out-of-plane stresses (compressive and tensile) were applied along and across the transistor channel lengths through bending ranging from 0.5 to 5 cm radii for n-type and p-type FinFETs. Electrical measurements were carried out before (for reference) and after flexing, and all flexing (bending) measurements were taken in the actual flexed (bent) state to avoid relaxation and stress recovery. The results show that global stress from substrate bending affects the devices in different ways compared to the well-studied uniaxial/biaxial localized strain. It is dependent on the type of channel charge carriers, the orientation of the bending axis, and the physical gate length of the device. We therefore outline useful insights on the suitability of flexible FinFETs for future free-form electronic applications.

The Internet of Everything (IoE) envisions connection of living beings (e.g. humans, plants, animals, and birds) and objects to the cloud where vital signs, activity rates, and other aspects of daily life can be monitored and analyzed to inform decisions and improve lifestyles. In that sense, IoE devices require close proximity to human body, fast decision making capability, and low heat dissipation. They must have low power consumption (dynamic and static), high performance, and flexibility. Subthreshold swing

(SS) is a critical parameter to this end because it affects the switching speed of a transistor and its dynamic power consumption. Planar CMOS-based technology exhibits a theoretical limit of 60 mV/decade on the achievable SS ($SS = V_T \left(1 + \frac{C_D}{C_{OX}}\right) \ln(10)$, where V_T is thermal voltage (25 mV @300 K), C_D and C_{OX} are the depletion and oxide capacitances, respectively, when $C_{OX} \rightarrow \infty$). On the other hand, tunnel FinFETs have been demonstrated with < 60 mV/decade SS [1].

The nonplanar 3D architecture of a FinFET device also enables low-power operation and further scaling, to cope with Moore's law [2, 3]. The FinFET devices are already commercially available at higher technology nodes (22 and 14 nm). The international technology roadmap for semiconductors (ITRS) predicts that the physical gate length requirement is 7 nm by 2025 [4]. Although such state-of-the-art CMOS electronics exhibit unparalleled advantages, they are rigid which raises a significant mismatch with non-uniform body contour and asymmetric skin surfaces of living being. Therefore, they need to be of free form – physically flexible and stretchable.

3.1. Device Fabrication and Characterization

To build state-of-the-art FinFETs, we used SOI substrates with a 90 nm SOI layer and a gate first approach. The fins were patterned using deep ultraviolet lithography to achieve sub-70 nm features, followed by an anisotropic reactive ion vertical etch of silicon to achieve a 90 nm fin height. The gate stack were then formed by successive atomic layer depositions (ALD) of 4 nm hafnium silicate ($HfSiO_x$) gate dielectric layers and 10 nm of TiN gate metal material. After the nitride (Si_3N_4) spacer formation, we carried out ion implantation of the source and drain regions followed by a salicidation

process using nickel silicide (NiSi) and aluminum silicide (AlSi) metallization to guarantee high-quality (Ohmic contacts between the metal contacts and transistor terminals.. Then we carried out activation anneal of the dopants at 1000 ℃ for 10 seconds. We studied devices with physical gate lengths that varied from 90 nm to 10 µm. A summary of the main fabrication steps is depicted with a cross-section showing fin internal structure in Figure 3.1.1(a-c).

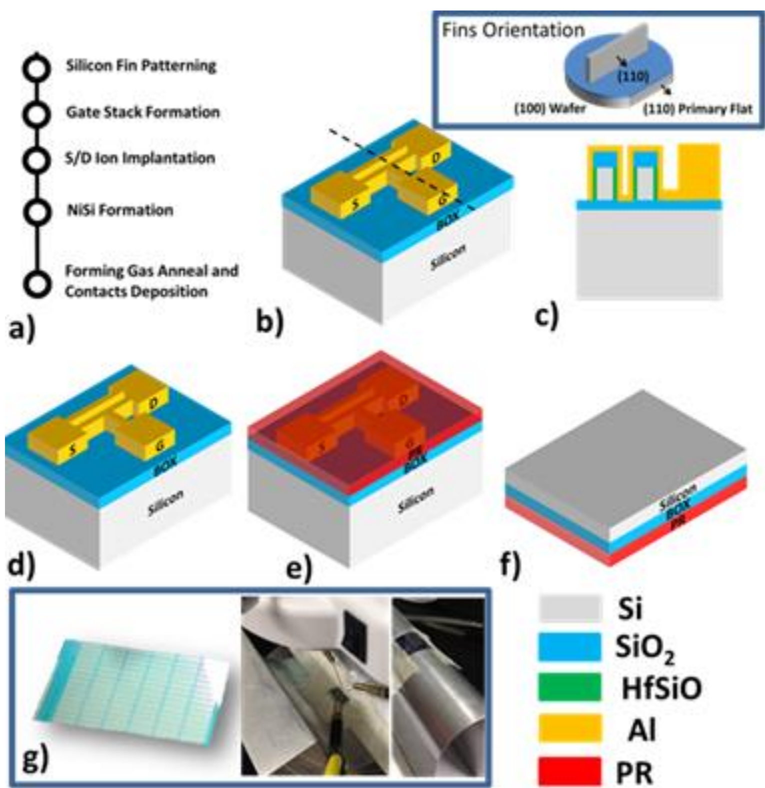


Figure 3.1.1: Fabrication flow (a-f) and characterization setup (g) of flexible FinFET.

The fabricated devices were then protected from the top side using ECI 327 positive-tone photoresist. Then we flipped the protected devices upside down on a carrier wafer to etch the back side. Figure 3.1.1(d-f) show the main flexing steps, illustrating how a DRIE etch using SiF_6 and C_4F_8 at −20 ºC is used to transform the

sample bulk from rigid form into a 50-µm-thick flexible fabric that houses the fabricated devices. We used a Keithley 4200-SCS Semiconductor Characterization System on a manual SemiProbe probe station, as well as custom-designed curved aluminum surfaces for device characterization (Figure 3.1.1(g)), the sample was placed with devices side facing upwards (away from the custom-designed aluminum structures contact) for probing. Bending was done along the fins (i.e., where the bending axis is parallel to the line connecting source and drain) and across the fins (i.e., where the bending axis is perpendicular to the fin length).

3.2. Silicon's Bending Ability and Limitations

Fracture strength determines the overall mechanical stability of a flexible system. The three-point bending test is widely used to assess the fracture strength of a substrate. For silicon thicknesses below 100 µm, the linear elastic bending beam theory cannot provide an accurate estimation of fracture strength because thin substrates produce a nonlinear deflection-load relationship, due to the large deflection of the thin silicon substrate resulting from horizontal forces at the supporting bearings, that is used to estimate fracture strength[5]. In 2015, Liu *et al.* introduced the large deflection theory of beam to account for this nonlinearity [6]. This provides important insights for theoretical limitations of flexible silicon thinner than 100 µm. Furthermore, based on the application's required bending radius, the thickness of the flexible material substrate (this analysis holds for isotropic materials for simplicity or if the effect is dominantly expressed for a specific plane. However, silicon is anisotropic and the stress is related to the strain by the elasticity matrix which is a 4th ranked tensor and is used in finite element

simulations in the following section) must be adjusted such that the applied stress is determined as

$$\sigma = Y\varepsilon \qquad (1)$$

where σ is the stress in Pascals, Y is Young's modulus, and ε is the nominal strain, which can be calculated as

$$\varepsilon_{nominal} = \frac{t}{2R} \qquad (2)$$

where t is the substrate thickness and R is the bending radius.

The applied stress must be lower than the fracture stress. Reference [6] showed that for a 50-µm-thick silicon fabric, the fracture stress is about 1.1 GPa. Substituting a (100) silicon Young's modulus of 128 GPa [7] in Equation (1), the and resulting strain value from Equation (2), we obtain a minimum bending radius for the 50-µm-thick flexible silicon fabric of approximately 3 mm, which decreases with a decreasing thickness. Therefore, a plain flexible silicon substrate that is 50-µm-thick or less with a bending radius of more than 3 mm will safely operate below the fracture stress level. We emphasize that these results are for a bare silicon substrate with no additive layers or patterns for devices. Therefore, based on the material's properties, substrate's thickness, and the bending radius necessary for a specific application, we can determine the most suitable approach and material system for fabricating a thin substrate. Noteworthy, silicon is an anisotropic material and its stress/strain relation is described by an eleasticity matrix not a simple value for Young's Modulus (as used in the example of a specific plane (100) of interest). Nonetheless, These results identify important boundary

limitations and guarantee that a bending of 0.5 cm is reasonably far from fracture stress regime. In most cases where flexible electronics are required to wrap around curvilinear objects, such as covering a fingertip or an arm, a bending radius of 3 mm would suffice. Moreover, continuing to reduce the substrate's thickness is another option that would enable us to decrease the bending radii and achieve a similar nominal strain corresponding to stress values below the fracture limit. Nonetheless, polymeric electronics exhibit better flexibility and might be a more feasible option for extreme applications that require folding of the substrate. Sekitani *et al.* demonstrated ultra-flexibility using polymeric substrates and pentacene semiconductor-based organic-thin-film transistors (OTFT) that can bent at 100 μm radius for open applications [8].

3.3. Effect of Bending Axis Orientation, Stress Type, Carrier Type on FinFET Performance

Empirical analysis of the effects of bending direction and bending axis orientation on the dimensions of the fins, representing the channels that carriers travel through, should provide useful insights into the feasibility of the integration of state-of-the-art CMOS devices into the aforementioned emerging applications. By using silicon's Young's modulus (128 GPa for (100) silicon), we can relate the (100) silicon Poisson's ratio of 0.17 [9] to the change in dimension through the following basic equation

$$v \approx \frac{\Delta L'}{\Delta L} \qquad (3)$$

where $\Delta L'$ is transverse strain and ΔL is the axial strain, as shown in Figure 3.3.1(a). Figure 3.3.1(b) shows the finite element method (FEM) simulation results for surface tensile and compressive stresses, anticipating that compressive stress has a greater impact

on device behavior (nearly doubling applied stress at the surface containing the devices), while illustrating the two bending conditions (across and along the channel). Figure 3.3.2 shows the effect of compressive and tensile stresses on the saturation transfer I—V characteristics of a sub-micron physical gate length (L_g) n-type (Figure 3.3.2(a-b)) and p-type (Figure 3.3.2(c-d)) FinFET for out-of-plane bending at radii of ±5 cm, corresponding to a 0.05% nominal strain in both cases. The measurements confirm that compressive stress always has a more pronounced effect for both devices—for different channel carriers types and for both bending axes (i.e., along and across the channel). We note the change of bending dimensions analysis by the output I—V characteristics curves, which showcase the pattern on a linear scale (Figure 3.3.2(e-f)). Based on changes in the fin/channel dimensions depicted in Figure 3.3.1(a), the pattern is expected. However, this pattern was not meticulously followed in the case of along-the-channel bending, indicating that the variation is better explained as an anomaly in behavior within a specific variation range than a consistent trend.

Localized strain enhancement in CMOS transistors has been extensively studied for decades [10], and with the assumption that different carriers will respond to stress differently. Wesler *et al.* used energy band diagrams to explain the different responses to stress with respect to carrier types [11]. For instance, in the suggested $SiO_2/Si/Si_{0.7}Ge_{0.3}$ strained structure, a barrier hole well in the valence band corresponds to a surface electron well in the conduction band. The strained silicon surface energy band structure is similar to the bent FinFETs case, where the stress gradient along the silicon thickness due to bending induces a strain effect, rather than the SiGe layer, influencing the effective masses (m^*) of charge carriers due to the deformations in the constrained/stretched energy

(E) bands ($m^{*} \alpha \, (\frac{d^2E}{dK^2})^{-1}$, where K is proportional to crystal momentum). However, due to band bending in different directions, tensile and compressive strains should form different barrier and surface well structures, depending on carrier type. This affects the transport properties especially at the edges of the channel (or fins) where lateral stress values are relatively higher and extra surface and barrier wells for carriers are likely to form. Oppositely charged free carriers behave differently depending on the bending axis (Figure 3.3.2). Further FEM analysis, as represented by Figure 3.3.3(a), shows a three-dimensional stress distribution in a fin bent across the channel and along the channel. Comparing the two stress profiles, it is clear that bending across the channel leads to different stress distribution than bending along the channel. As can be deduced from the results shown in Figure 3.3.2, electrons are more sensitive to stress when the channel is bent along its length, while holes are more sensitive when the bending axis is perpendicular to the channel length. Because CMOS-based technology utilizes both n- and p-type field-effect transistors (FETs) on the same wafer, the assessed degradation should be the worst-case scenario for both of the two channel types. Furthermore, localized stress due to SiGe source and drain has historically been used to strain the channel and enhance mobility. On the other hand, a dissimilar effect takes place in this study. This is because empirical stress imposed by out-of-plane bending causes a different stress distribution profile and different magnitudes compared to localized stress when both are exposed to same strain values. The inset in Figure 3.3.3(b) shows the calculation of the displacement required for specific strain and the resulting stress profiles for out-of-plane and in-plane stressed at the same strain values. Figure 3.3.3(c) shows the simulation setup and the values of the stiffness matric for accounting for silicon

anisotropy. The simulated fin was rotated 45 degrees in the XY plane to align the fin plane with the (110) plane while the wafer plane is (001). Using equations (1-2), the stress regime for 0.5 to 5 cm bending radii is 80 to 800 MPa, corresponding to an intermediate stress range relatively lower than that used in strained silicon to engineer mobility enhancements [12]. Still there were cases of mobility enhancements for long-channel devices flexed along the channel, but due to the complexity of the testing setup and sources of variation while contacting the devices, the conclusion would be an anomaly within ±5% for short-channel devices. Other key switching properties are summarized in Table 3.3.1.

Table 3.3.1: Key switching properties of FinFETs under out-of-plane stress

Extracted Parameter	**Method**	**% change**
Subthreshold Swing (SS)	$SS = \min(\frac{\Delta V_{GS}}{\log(I_{DS1}/I_{DS2})})$	~10%
Threshold Voltage (V_{TH})	$V_{th} = I_{ds}/g_m - V_{GS}\|@ \max g_m$	~10%
Drain Induced Barrier Lowering (DIBL)	$DIBL = \frac{V_{TH,sat} - V_{TH,lin}}{V_{DD} - V_{DS,low}}$	±50%
Maximum Transconductance (g_m)	$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$	-40%

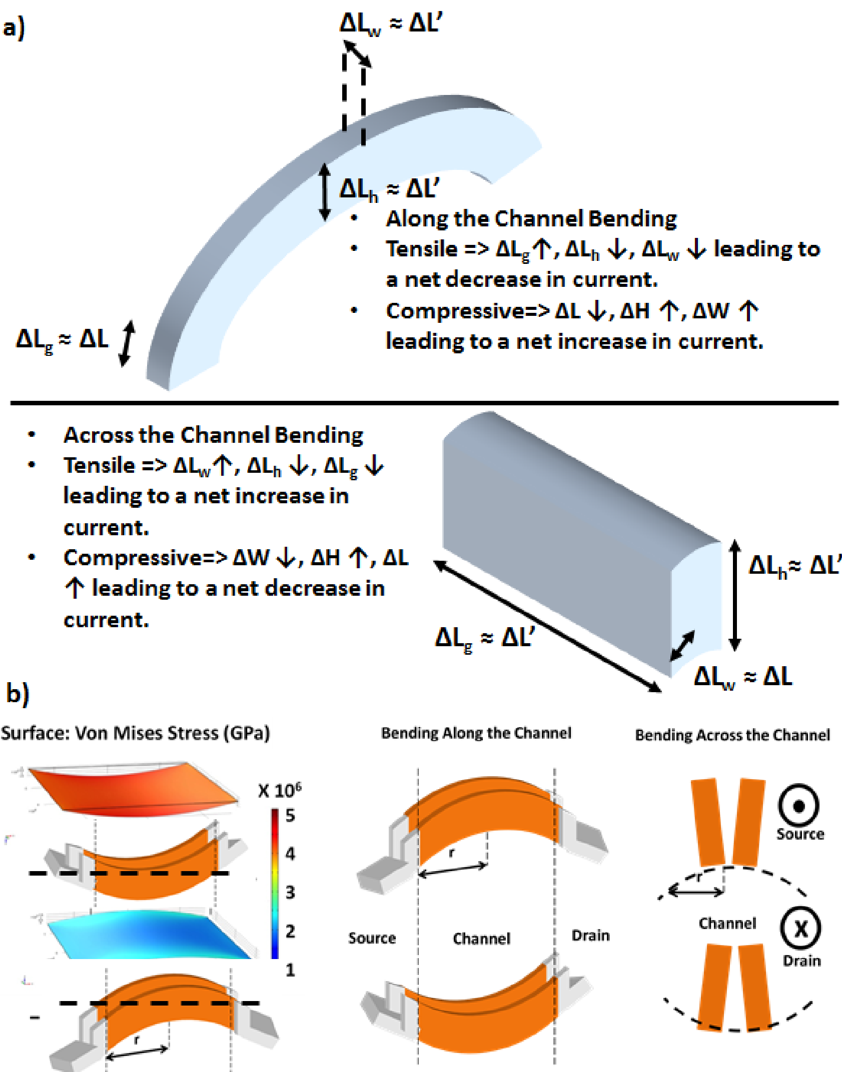


Figure 3.3.1: Illustrations on changes in fin dimensions (a), and FEM simulations for Von Mises stress distribution (b).

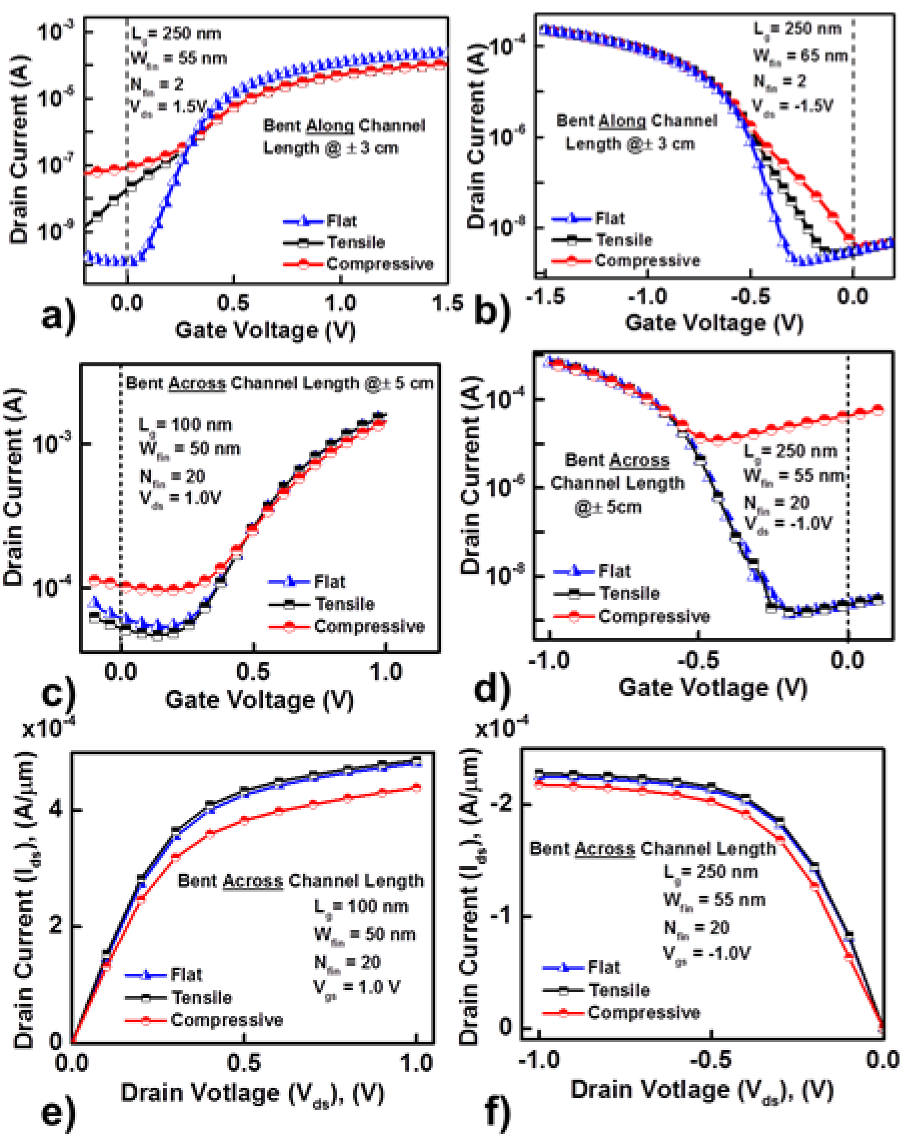


Figure 3.3.2: Transfer (a-d) and output (e-f) plots of FinFETs of various dimensions under varied stress conditions and bending axes

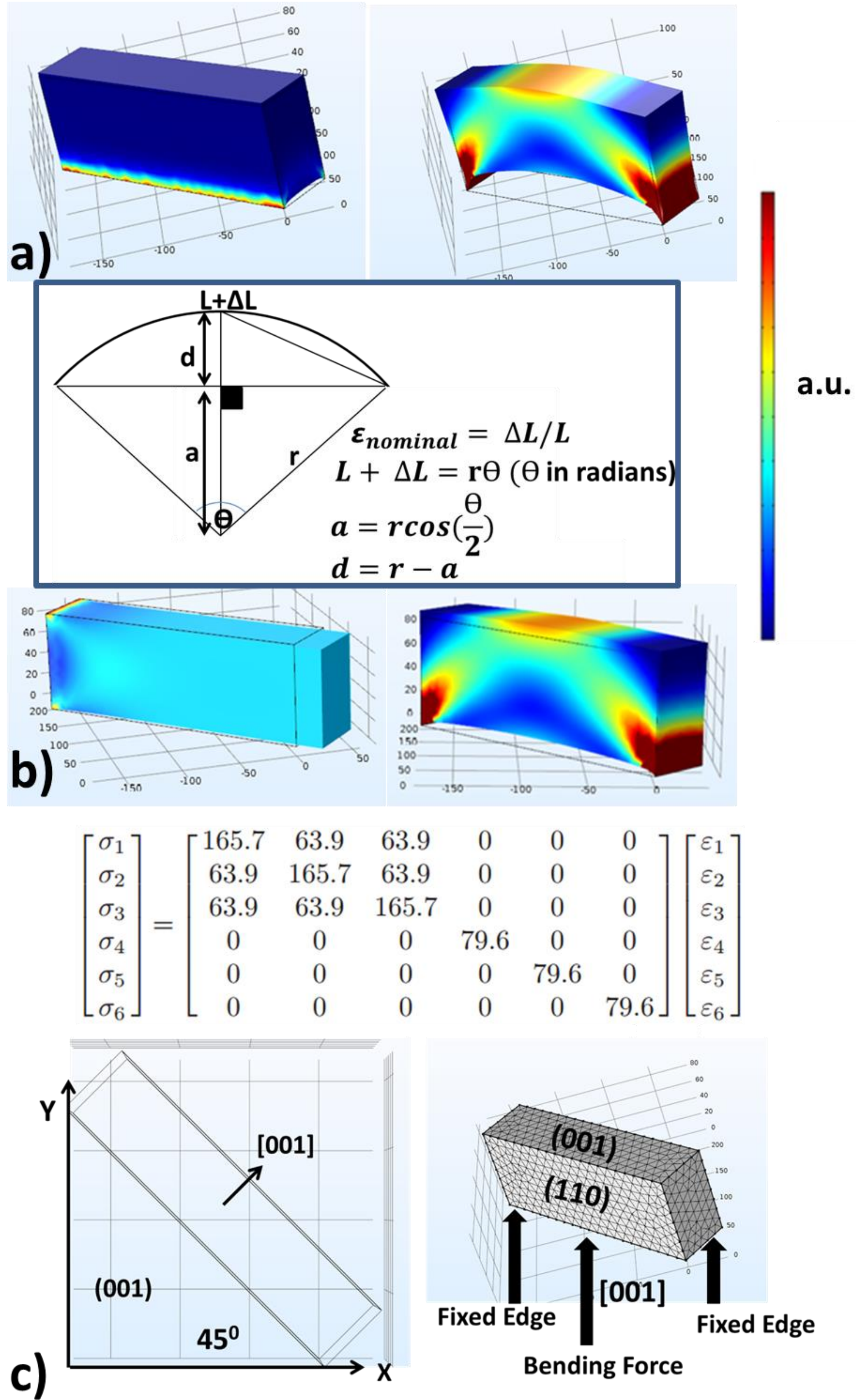

a)
L+ΔL
d
a
r
θ
$\varepsilon_{nominal} = \Delta L/L$
$L + \Delta L = r\theta$ (θ in radians)
$a = r\cos(\frac{\theta}{2})$
$d = r - a$
a.u.
b)
$$\begin{bmatrix}\sigma_1\\\sigma_2\\\sigma_3\\\sigma_4\\\sigma_5\\\sigma_6\end{bmatrix} = \begin{bmatrix}165.7 & 63.9 & 63.9 & 0 & 0 & 0\\ 63.9 & 165.7 & 63.9 & 0 & 0 & 0\\ 63.9 & 63.9 & 165.7 & 0 & 0 & 0\\ 0 & 0 & 0 & 79.6 & 0 & 0\\ 0 & 0 & 0 & 0 & 79.6 & 0\\ 0 & 0 & 0 & 0 & 0 & 79.6\end{bmatrix}\begin{bmatrix}\varepsilon_1\\\varepsilon_2\\\varepsilon_3\\\varepsilon_4\\\varepsilon_5\\\varepsilon_6\end{bmatrix}$$
c)
Y
X
[001]
(001)
45°
(001)
(110)
[001]
Fixed Edge
Fixed Edge
Bending Force

Figure 3.3.3: FEM stress profile for along and across the channel bending (a), in-plane/out-of- plane stress (b), and crystallographic orientation and bending simulation setup and the stiffness matrix used in simulations (c).

The large variation in the drain-induced barrier lowering (DIBL) implies that the devices suffered from significant threshold voltage (V_{TH}) shifts when functioning in the saturation regime. An increment under compressive stress implies that the device suffers higher leakage currents due to a relatively larger reduction in V_{TH}. A decrease in DIBL under tensile stress would lead to a device with relatively larger V_{TH} than designed, and, consequently, lower overdrive voltage (V_{DD}–V_{TH}, where V_{DD} is the supply voltage) and on-state currents (I_{ON}). The decrease in the peak transconductance (g_m) would degrade the performance of a transistor device while operating as an amplifier, because the gain of an amplifier is proportional to the transconductance of the device. Ideally, ICs are designed to tolerate 10% deviation in circuit parameters. Therefore, for anomalies greater than 10%, serious considerations are essential when integrating such high-performance devices in flexible ICs that are intended to function properly under various bending conditions. This can be mitigated by redundant compensation elements to adjust the parameters. Current design for yield in deep-submicron technologies already uses similar techniques to comply with 3σ and 6σ standards (σ measures variability), accommodating process variations for extremely scaled emerging nodes. For instance, adding a backup transistor connected in parallel when needed to enhance the circuit current as the original transistor experiences increased V_{TH} and lower current. The observed trend for increased gate leakage with bending can be utilized to sense the leakage current and determine the corresponding parameter deviation, allowing us to make dynamic decisions to engage added components and correct the deviation effect.

To extract the effective mobility (μ_{eff}), we use the following equation

$$\mu_{eff} = \frac{g_d L_g}{W Q_n} \qquad (4)$$

where g_d is the drain conductance, Q_n is the mobile charge density in the channel, and W is the channel width. Figure 3.3.4 depicts the extracted effective mobility values versus L_G for tensile and compressive bent n- and p-type FinFETs. Conclusively, FinFETs with longer L_G exhibited higher deviations from the unbent benchmark, for both majority carrier and applied stress types. For instance, n-type a representative FinFET showed a deviation of 13% for an L_G of 10 μm, compared to a 2.3% deviation for L_G of 110 nm. Similarly, a representative p-type FinFET had a 90% deviation for L_G of 10 μm and 2.7% deviation for L_G of 250 nm. Although the long-channel p-type FinFET exhibited a 90% deviation in its effective mobility, their functionality is still attested as a switch, as evidenced in Figure 3.3.4(c). Under both applied stress types, the on-to-off current ratio (I_{ON}/I_{OFF}) was about 10^3 with low gate leakage.

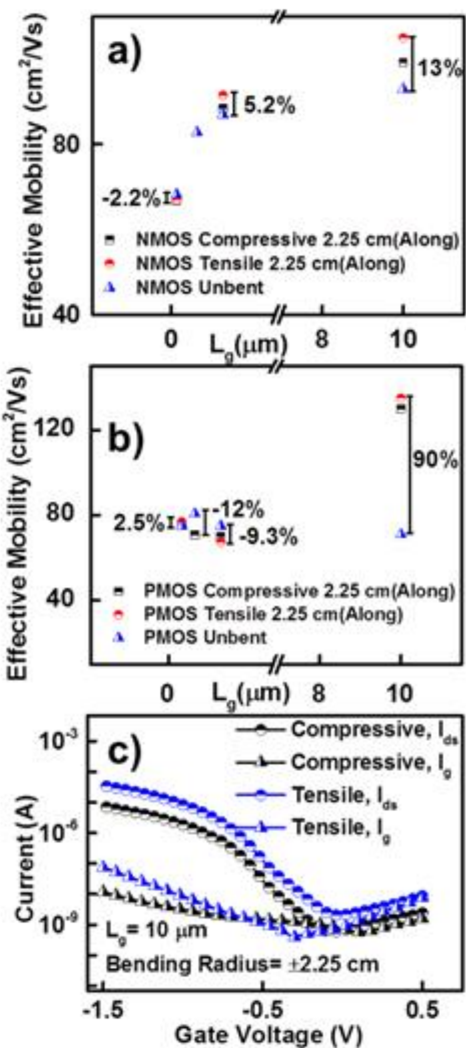


Figure 3.3.4: Mobility *vs.* gate length (a-b) and functional device with 90% mobility change (c).

In ultra-large scale integration (ULSI), the flowing drain current in the on-state (I_{ON}) and the off-state (I_{OFF}) are critical properties of every device. Depending on the magnitudes of I_{ON}, V_{DD}, and gate capacitance ($C_G \approx$ oxide capacitance (C_{OX})), the intrinsic delay (t_d) of the device is determined ($t_d = CV_{DD}/I_{ON}$). Figure 3.3.5(a) shows the variation on the gate delay with the I_{ON}/I_{OFF} ratio for a representative p-type FinFET device The higher the $I_{ON,}$ the faster the circuit, because the total capacitance of the

circuit, including parasitic, is proportional to the time constant (τ), which affects the speed at which the circuit can operate.

The ultimate goal of strain engineering is to increase I_{ON} through mobility enhancements. A FET current is given by

$$I_{ds} = \frac{WC_{OX}\,\mu_{eff}}{L_G}\left[V_{DS}(V_{GS} - V_{TH}) - \frac{V_{DS}^2}{2}\right] \qquad (5)$$

I_{ON} corresponds to the saturation current (I_{SAT}) when $V_{DS} \geq V_{GS}-V_{TH}$ and is approximately (discarding short channel modulation effect) given as

$$I_{ON} = \frac{WC_{OX}\,\mu_{eff}}{2L_G}(V_{GS} - V_{TH})^2 \qquad (6)$$

For a representative short-channel p-type FinFET (where L_G is less than 250 nm), the change in I_{ON} is less than 1% under both tensile (1.5 cm bending radius) and compressive stress (−3 cm bending radius), as shown in Figure 3.3.6(a). This is justified by the insignificant deviations in μ_{eff} and V_{TH} while other parameters are physical. Even for a long-channel p-type FinFET device (L_G = 10 µm)—where the change in calculated μ_{eff} is was about 90%—the changes in I_{SAT} were –2.4% for tensile stress and –1.5% for compressive stress (both at 2.25 cm bending radius), at $V_{DS} = V_{GS} = -1.5$ V. The extreme variation in μ_{eff} did not translate into current variation—although the change in V_{TH} while operating in the saturation regime (extracted using the Ghibaudo method for short-channel devices, *i.e.* the intercept with V_{GS} axis from $I_{DS}/\sqrt{g_{m,sat}}$ *vs.* V_{GS} plot [13]) is less than 8% in worst-case compressive stress, and less than 1% for tensile stress (at 2.25 cm bending radii). Hence the calculated mobilities do not reflect actual degradation, which is attributed to the susceptibility of the measurement used for mobility calculations to noise,

namely the strong dependence of mobility on g_d which is measured at very low drain voltages (between 25 and 50 mV).

The integrity of the gate oxide in scaled CMOS-based devices is another critical issue. Scaling compromises the reliability and physical limits of the best available oxide in terms of interface quality and defect density. Therefore, high-κ dielectrics have been used to replace SiO_2. The FinFETs in this work utilize a few nanometers of $HfSiO_x$ high-κ dielectric layers. A consistent trend of increasing gate leakage between the gate terminal and the source of a FinFET has been observed, especially under tensile stress for a representative short-channel 250 nm p-type FinFET (Figure 3.3.5(b-c)). This is in line with previous observations by Choi et al. on the reduction in the work function of TiN due to tensile out-of-plane bending which reduces the Gate/Oxide barrier height causing higher leakage currents [14]. This does not affect the functionality of the device due to the orders of magnitudes difference between I_{DS} versus V_{DS}, as depicted in Figure 3.3.5(d). Nonetheless, we found that FinFET devices with various dimensions had still been functioning after long bending durations (about one year), as depicted in Figure 3.3.6.

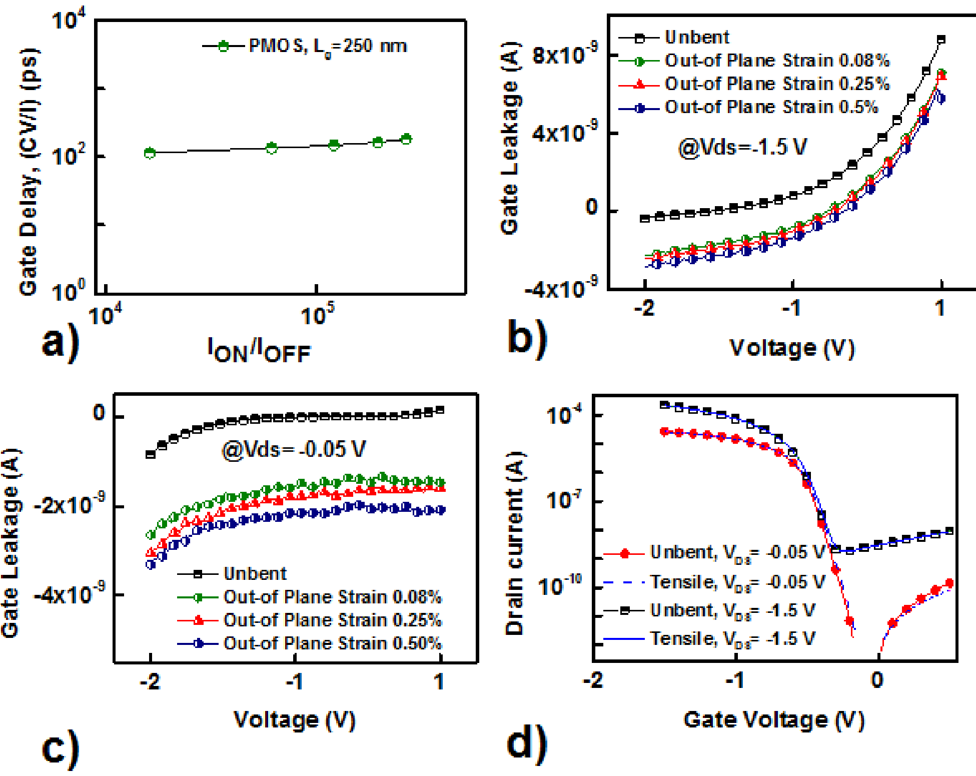


Figure 3.3.5: Gate delay (a) and leakage trends (b-c) for a 250 nm p-type FinFET with the transfer plot shown in (d).

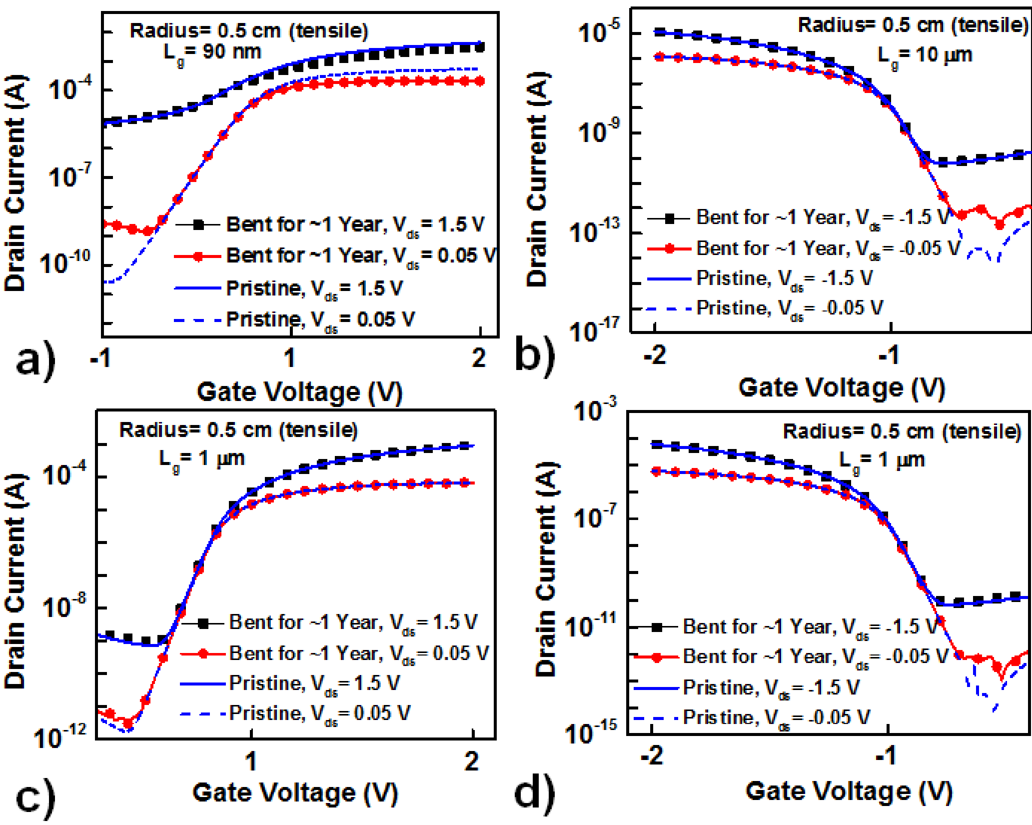


Figure 3.3.6: Transfer plots for short and long channel FinFETs bent for 12 months at 0.5 cm bending radius (a-d).

The presence of leakage currents is a major issue in deep-submicron technologies [15]. I_{OFF} is highly dependent on V_{TH}, dielectric integrity, and operation temperature. Device operation dependency on temperature was not studied in this work. I_{OFF} is inversely proportional to an exponential function in V_{TH} ($I_{OFF} \alpha\, e^{(V_{GS}-V_{TH})}$). Therefore, leakage current is strongly affected by shifts in V_{TH} and might require circuit correction (although the variation in our case is within 10%). The degradation in dielectric integrity is evident from the increasing gate leakage with increasing bending radius. Tensile stress increased a maximum of three times at 0.5 cm bending radius along the channel. This means that in a battery-operated IoE system, where the device is in standby mode most of the time and leakage power dominates, the useful time before a re-charge is required will

be reduced at least three times. The effect is not direct due to the existing positive feedback loop between flowing current and temperature. The higher currents increase the temperature. The relation between the temperature and the semiconductor band gap is given by the Varshni's equation

$$E_g(T) = E_g(0) - \frac{T^2}{T-\beta} \qquad (7)$$

where E_g is the band gap in eV, T is the temperature, and β is a material property. This in turn reduces the V_{TH}, and consequently, increases the current further. This feedback loop is a common cause of thermal runaway failures in ICs. Therefore, a 3× increment in I_{OFF} can translate to severer effects and requires closer studies at the circuit level to prevent the potential for eventual failures during the useful lifetime of an electronic system.

At the device level, still no observable degradation in switching behavior under various bending conditions is present. The gate leakage is 1000× less than the drain currents (*i.e.* I_{ON} will not be significantly affected by this mild increase in leakage, and functionality is preserved).

3.4. Residual Stress vs. Effective Stress

In microcrystalline silicon transistors, Dong *et al.* showed the effect of bending of flexible TFTs [9]. All measurements were taken in the flat position after the sample had been exposed to various bending stress types and various durations. We anticipate this work to be an important milestone in assessing out-of-plane stress effects on transistor characteristics. However, the work focused on residual stress rather than real-time actual stress measurements. Residual mechanical stress is the stress that remains in the material after mechanical deforming. If the material is originally flat and bending occurs within

the elastic region, then, re-flattening the material leaves no residual mechanical stress. This explains the minor deviations in the transfer and output I—V curves concerning the effect on source-to-drain currents and gate leakage. Similarly, stress recovery and self-healing properties are widely used concepts in reliability physics, drawing the cutline between an electrically stressed and post-stressed device. We have previously shown a self-healing property in metal–oxide–semiconductor capacitors (MOSCAPs) subjected to mechanical stresses through electrical annealing by passing current [16]. The same study shows that for silicon based CMOS dynamic stress (successive bending and flattening) has severe effect on the reliability of the structure. Hence, they are more suitable for bent static structures than dynamic ones. Accelerated ramping voltage (V_{ramp}) analysis, time dependent dielectric breakdown (TDDB), and bias temperature instability (BTI) tests used in assessing devices' useful projected lifetime employ various stress methods in which relaxation time has a strong effect on the measurements. For instance, one of the challenges in the reliability assessment of high-κ dielectrics, including $HfSiO_x$, is the accuracy of the BTI test composed of stress-measure-stress cycles to track the shift in V_{TH} due to the relaxation/recovery of degradation when stress is removed in the measurement step [17]. Figure 3.4.1 shows the transfer I—V characteristics curves of long- and short-channel n- and p-type FinFET devices before and after applying stress. Evidently, the variation does not reflect the significant deviations experienced under effective stress as previously depicted in Figure 3.3.2, because of the absence of residual mechanical stress. The results of the flexible microcrystalline silicon TFT show that devices can be folded for storage then unfolded when needed, recovering their characteristics after being re-flattened [9]. In their work, Dong *et al.* used 150-nm-thick

silicon nitride (Si_3N_4) as a gate insulator. Although Si_3N_4 was shown to exhibit high trap densities, which is expected to worsen with bending due to increased dielectric stress, it was shown that relaxation/recovery time decreased as the Si_3N_4 thickness increases [18], thus manifesting the durability of the Si_3N_4 TFTs when re-flattened. This work shows that this conclusion can be extended to scaled high-performance high-κ dielectric FinFETs that use thin (4-nm–thick) HfSiO gate insulators.

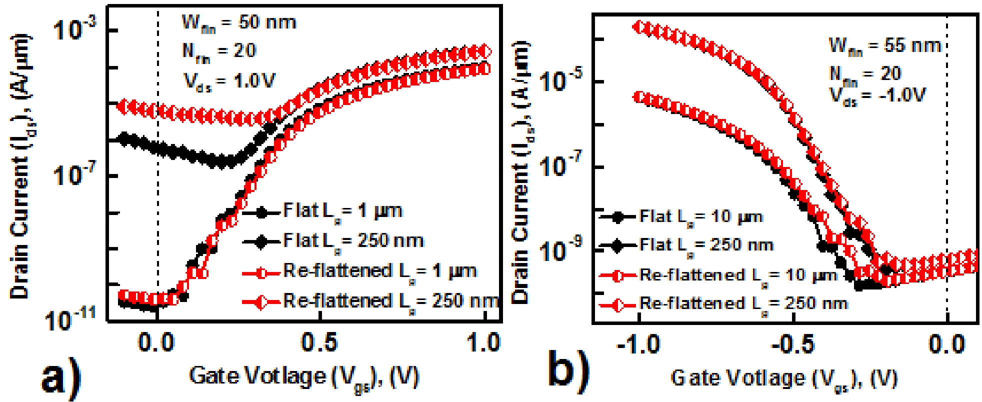


Figure 3.4.1: Transfer plots for re-flattened n-type (a) and p-type (b) FinFETs.

3.5. Conclusion

We have presented a comprehensive analysis on varying flexed (bent) states of flexible high-performance FinFET CMOS. This also helps avoiding stress recovery when re-flattened. Nonetheless, due to the sensitivity of the measurements, an extra source of variation (*i.e.* contact resistance) is added. As previously mentioned, the outlined percentage variations are ultimately useful for the actual systems applications, whether it is through flexible ICs for IoT, IoE, or wearable electronics. The results show that most variations are restricted to ±10%, which is similar to the process variations range in deep-submicron technologies where possible mitigation solutions are already practiced. Moreover, it provides insight into the degree of variation in device characteristics when

they are bent, which complements previous work and shows that variations can be mitigated to render the devices suitable for performing while bent as well as when flattened. This work presents the possibility of adding the flexing ability to industry-grade FinFETs without sacrificing functionality and highlights the various effects that out-of-plane bending has on these devices.

This concludes the first part of the dissertation concerned with the demonstration of field-effect transistors (gating structures for memory arrays) on flexible Silicon. The second part focuses on storage devices.

3.6. References

[1] Zhang, J.; De Marchi, M.; Gaillardon, P.E.; De Micheli, G., 2014. A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current. In Proceedings of the International Electron Devices Meeting (IEDM'14) (No. EPFL-CONF-201905).

[2] Moore, G.E. Cramming more components onto integrated circuits. *IEEE Solid-State Circ. Newslet.* 2006, 3, 33-35.

[3] Yu, E.; Chang, L.; Ahmed, S.; Wang, H.; Bell, S.; Yang, C. Y.; Tabery, C.; Ho, C.; Xiang, Q.; King, T. J.; Bokor, J. FinFET scaling to 10 nm gate length. In Proc. IEEE Int. Electron Devices Meeting, 2002, pp. 251-254.

[4] Semiconductor Industry Association. International Technology Roadmap for Semiconductors. 2013.

[5] Wu, J.; Huang, C.; Liao, C. Fracture strength characterization and failure analysis of silicon dies. *Microelectron. Rel.* 2003, 43, 269-277.

[6] Liu, Z.; Huang, Y.; Xiao, L.; Tang, P.; Yin, Z. Nonlinear characteristics in fracture strength test of ultrathin silicon die. *Semicond. Sci. Techol.* 2015, 30, 045005.

[7] Boyd, E. J.; Uttamchandani, D. Measurement of the anisotropy of young's modulus in single-crystal silicon. *J. Microelectromech. Syst.* 2012, 21, 243-249.

[8] Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. Flexible organic transistors and circuits with extreme bending stability. *Nat. Mater.* 2010, 9, 1015-1022.

[9] Dong, H.; Kervran, Y.; Coulon, N.; De Sagazan, O.; Jacques, E.; Mohammed-Brahim, T. Highly Flexible Microcrystalline Silicon n-Type TFT on PEN Bent to a Curvature Radius of 0.75 mm. *IEEE Trans. Electron Devices* 2015, 62, 3278-3284.

[10] Thompson, S. E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C. H. A 90-nm logic technology featuring strained-silicon. *IEEE Trans. Electron Devices* 2004*,* 51, 1790-1797.

[11] Welser, J.; Hoyt, J.; Gibbons, J. NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures. in Proc. IEEE Int. Electron Devices Meeting, 1992, pp. 1000-1002.

[12] Rim, K.; Chu, J.; Chen, H.; Jenkins, K. A.; Kanarsky, T.; Lee, K.; Mocuta, A.; Zhu, H.; Roy, R.; Newbury, J.; Ott, J. Characteristics and device design of sub-100 nm strained Si N-and PMOSFETs. In Symp. VLSI Technol., Dig. Tech. Pap., 2002, pp. 98-99.

[13] Dobrescu, L.; Petrov, M.; Ravariu, C. Threshold voltage extraction methods for MOS transistors, In Proc. Semicond. Conf., 2000, pp. 371-374.

[14] Choi, Y. S.; Numata, T.; Nishida, T.; Harris, R.; Thompson, S. E. Impact of mechanical stress on gate tunneling currents of germanium and silicon p-type metal-oxide-semiconductor field-effect transistors and metal gate work function. *J. Appl. Phys.* 2008, 103, 064510.

[15] Goto, K.; Fushida, A.; Watanabe, J.; Sukegawa, T.; Kawamura, K.; Yamazaki, T.; Sugii, T. Leakage mechanism and optimized conditioms of Co salicide process for deep-submicron CMOS devices. In Proc. IEEE Int. Electron Devices Meeting, 1995, pp. 449-452.

[16] Ghoneim, M.; Kutbee, A.; Nasseri, F. G.; Bersuker, G.; Hussain, M. Mechanical anomaly impact on metal-oxide-semiconductor capacitors on flexible silicon fabric. *Appl. Phys. Lett.* 2014, 104, 234104.

[17] Lee, B. H.; Choi, R.; Sim, J. H.; Krishnan, S. A.; Peterson, J. J.; Brown, G. A.; Bersuker, G. Validity of constant voltage stress based reliability assessment of high-κ devices. *IEEE Trans. Device Mater. Rel.* 2005, 5, 20-25.

[18] Zaghloul, U.; Papaioannou, G.; Coccetti, F.; Pons, P.; Plana, R. Dielectric charging in silicon nitride films for MEMS capacitive switches: Effect of film thickness and deposition conditions. *Microelectron. Rel.* 2009, 49, 1309-1314.

Chapter 4 Flexible Memristor

Moving to storage elements, we demonstrated for the first time memristive devices fabricated on bulk monocrystalline silicon (100) which is next transformed into a flexible thin sheet of silicon fabric with all the pre-fabricated devices. This process preserves the ultra-high integration density advantage unachievable on other flexible substrates.

Memristors have attracted lots of interest in the scientific community since their inception followed by long sought experimental demonstration [1, 2]. They offer an alternative intriguing option to complementary metal oxide semiconductor (CMOS) based flash non-volatile memory (NVM) which is approaching scaling limits. For instance, based ITRS report of 2012 flash memory ½ pitch should reach 10 nm by 2020 [3]. Cross bars resistive RAMs with 10 nm x 10 nm cell size have already been reported in IEDM, 2011 [4]. Additionally it can also be a complementary option for volatile memory like dynamic random access memory (DRAM). The simple structure of memristive devices and facile fabrication enables its scaling down to regimes beyond state-of-the-art CMOS technology. In addition, there are proposed techniques to replace the extra gating transistor for memristive cells [5]. This makes memristors an excellent candidate to act as synapses in neuromorphic circuits. It has been experimentally demonstrated that CMOS neurons and memristor synapses in crossbars configuration can support synaptic functions [6]. While memristive devices can serve as analogous components of brain neurons. The brain cortex itself is folded enabling ultra-compact integration. Therefore, exploring memristive devices on foldable platform is an important and timely step towards future electronic applications.

To this end, several approaches have been followed mostly focused on building memristive devices from organic materials on organic flexible substrates [7], or building inorganic memristive devices on flexible organic substrates at low temperatures [8, 9]. Although these approaches are key steps forward, some key fundamental challenges exist with these approaches especially due to the incorporation of organic material systems. For instance, organic materials are less thermally stable for practical operation than inorganic materials, and their processing does not allow the high integration density achievable in current silicon based semiconductor technology [10-13]. Although having the inorganic memristor on an organic substrate is an important step forward, it still faces the thermal budget limitation which affects the performance of the devices. A third approach is building inorganic electronics on inorganic substrates that are flexible. In previous works, we reported the successful integration of various devices on flexible thin Si (100) fabric [14-17]. This approach enables making the conventional optimized devices and material systems to be transformed into flexible structures without sacrificing integration density or imposing thermal limitations. Indeed, capitalizing on the ultra-high density inherent in the Si industry is essential for matching the compactness and computation efficiency of the brain.

4.1. Device Fabrication

The memristor material system (Al, TaN and Al_2O_3), deposition and patterning processes (sputtering and ALD) are standard CMOS processes. The maximum temperature required for our releasing step is 300°C which is relatively low and can be done before or after device fabrication based on the followed flexing approach ("device first" or "device last"). Hence, we preserve the desired characteristics of bulk devices,

such as high integration density and film quality while adding the flexibility feature to the memristors. Our transformation processes can be achieved through two approaches. The first is the “device first” approach (details can be found in [12]). The second is the “device last” approach implemented for this study. The process utilizes a 300 nm thermally grown SiO_2 on Si (100) 4’’ wafers for devices isolation, Figure 4.1.1a. The oxide layer is then patterned using photolithographic techniques (ECI 3027 positive photoresist, 200 mJ/cm^2 exposure dose and Metal Free AZ 726 developer) to have 10 µm diameter holes with 20 µm pitch, followed by a deep reactive ion etching (DRIE) using the Bosch process of successive SF_6 etching and C_4F_8 deposition cycles for smooth sidewalls up to 25 µm depth, Figure 4.1.1b. Then a spacer formation process is carried out using conformal atomic layer deposition (ALD) of 50 nm Al_2O_3 at 300°C using O_2 plasma and a consecutive directional reactive ion etch (RIE) in CHF_3 that removes the spacer from vertical surfaces leaving the sidewalls protection intact (not shown). Finally, the sample is placed in a XeF_2 reaction chamber where isotropic etching of Si takes place at the bottom of the deep hole network to peel off a thin Si (100) fabric that is flexible up to a bending radius of 10 mm (0.125% nominal strain, $\varepsilon_{nominal}= t/2R$, where t is the substrate thickness and R is the bending radius). In our process we released a 3 x 4 cm^2 area of the 4’’ wafer for flexible memristive devices while the rest hosted the bulk devices for a comparative analysis. The devices were built using 200 nm sputtered Al common bottom electrode (Figure 4.1.2a) then an ALD stack of 20 nm TaN/ 10 nm Al_2O_3/ 20 nm TaN without breaking the vacuum, followed by another 200 nm sputtered Al for top contact, Figure 4.1.2b. The TaN layer is there to prevent the Al ions from diffusing into the dielectric and preserve the quality of the top surface of ALD Al_2O_3

from physical damage during top Al electrode sputtering process. The devices were 100 x 100 μm^2 (a motor neuron is 100 µm in diameter).

Figure 4.1.3 shows a digital image of the fabricated foldable devices after cutting the anchored edges and releasing the fabric from the bulk wafer. The thin fabric and network of release holes both contribute to the flexibility of the fabric, which in this case reached 1 cm bending radius. The relation between the flexibility (a measure of the tendency of a material to bend) and the thickness of the fabric is inversely proportional. Therefore, as the thickness of the fabric decreases, the bendability increases significantly. A previous study on holes effect on bendability can be found in [11] where an increase of 64% in bendability due to release holes has been demonstrated.

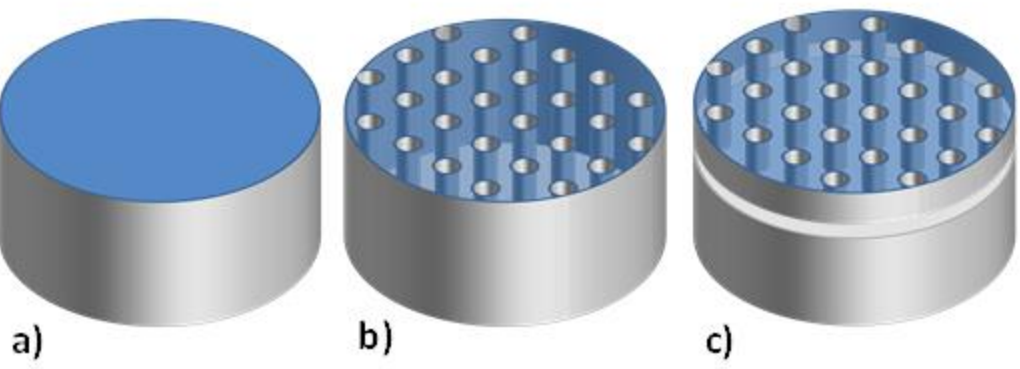


Figure 4.1.1: Peeling off a thin flexible Si fabric from bulk Si (100); a) thermal oxidation to grow 300 nm SiO_2 on Si, b) patterning and etching deep trenches in SiO_2 and Si bulk (~25 um deep) followed by a spacer formation step to protect trenches sidewalls (not shown), c) peeling thin Si (100) sheet using XeF_2 isotropic etch at the bottom of the trenches.

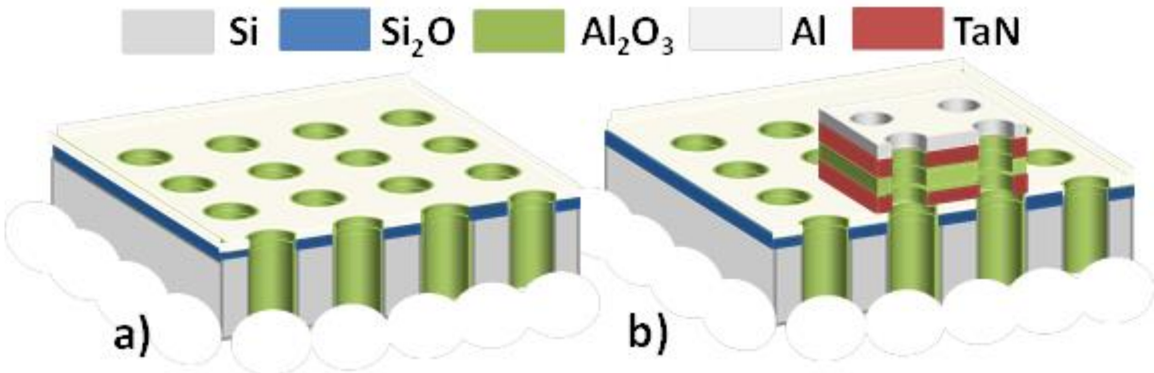


Figure 4.1.2: Memristor fabrication; first, the peeled Si fabric (Figure 4.1.1) is sputtered with 200 nm of Al acting as common bottom contact electrode (a), Then, the sample with Al bottom electrode on top is inserted into an ALD reaction chamber where 20 nm TaN/ 10 nm Al_2O_3/ 20 nm TaN are deposited without breaking the vacuum, afterwards, using photolithographic techniques and ECI 3027 photoresist, the active areas of the devices are protected and the stack is etched using RIE followed by subsequent removal of PR in Acetone (b).

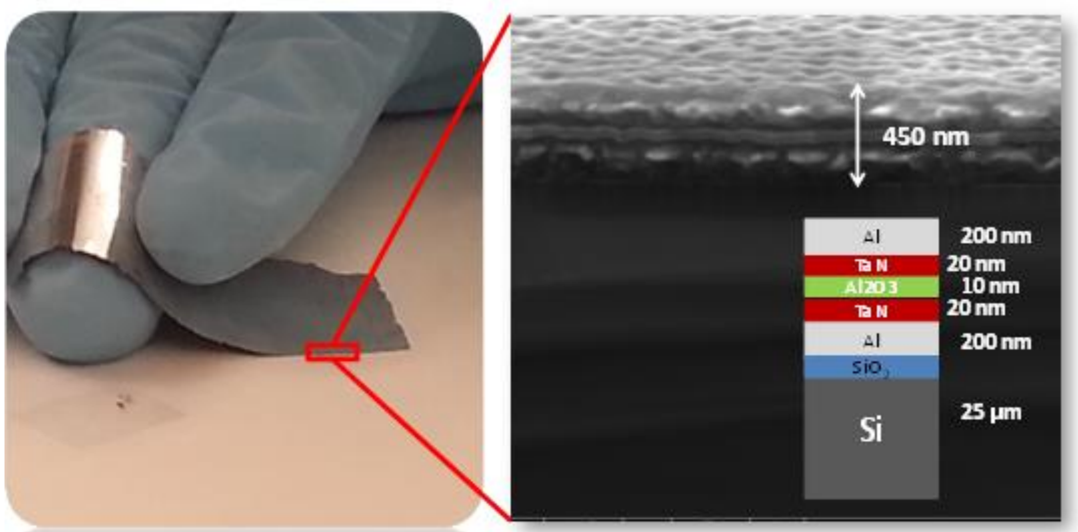


Figure 4.1.3: Digital image of actual fabricated memristors on flexible Si fabric (25 µm thick) (left). It is to be noted there is no support platform to hold or to handle the released silicon fabric. Scanning electron microscope image of device and platform stack (right).

4.2. Device Characterization

Basic IV characterization of 10 flexible/foldable and 10 bulk/inflexible devices was performed on a Keithley 4200 SCS. All fabricated memristors had a common bottom Al electrode while the patterned top electrode identified the device under test.

Figure 4.2.1 shows the hysteresis properties of the average values for ten bulk and ten foldable devices. The high switching voltages are attributed to the high quality of ALD Al_2O_3 and the conduction mechanism dependence on a soft breakdown phenomenon and in turn they effect a lower R_{OFF}/R_{ON} ratio (R=V/I, hence, breakdown currents occurring at higher voltages result in higher R_{ON} while R_{OFF} is relatively unchanged leading to a lower R_{OFF}/R_{ON}). Another factor contributing to the low R_{OFF}/R_{ON} ratio is the nature of breakdown in high-κ dielectrics. The breakdown occurs in phases. First, a soft-breakdown (reversible) occurs, then, by increasing the applied electrical stress a hard-breakdown follows (permanent physical damage). Since memristive effect rises due to a soft-breakdown phenomenon, it is very critical to do the voltage sweeps in a suitable range that would suffice to cause a soft-breakdown but would not provide enough stress for a hard-breakdown. This borderline is practically difficult to achieve. The closer the sweeping range to this borderline, the higher the R_{OFF}/R_{ON} ratio because R_{ON} gets much smaller with severer soft-breakdown; whereas, R_{OFF} is almost unchanged as long as no physical hard-breakdown occurs. Therefore, the R_{OFF}/R_{ON} ratio becomes more of an optimization problem that deviates from the main reporting of this study (i.e. reporting a facile process for making foldable memristive devices on silicon fabric with preserved memristive properties). The results indicate that there is no significant deviation in device properties due to the flexing step. Furthermore, these results are for devices the size of a motor neuron, which is much bigger than a synapse. Scaling these devices to nanoscale lateral dimensions would enable low power operation. In addition, scaling down would provide a safer mode operation for our process as the release holes (separated by 10 μm) do not have to pass through the devices' structures anymore. This is because the reported

devices have a network of holes passing through the devices' active layers as we make the 10 μm holes separated by 10 μm while devices are 100 x 100 μm^2, while making devices that are few nanometers x few nanometers would enable stacking multiple devices in between the holes with no holes passing through. This means that the devices can show more similarity in terms of physical structure to regular bulk devices.

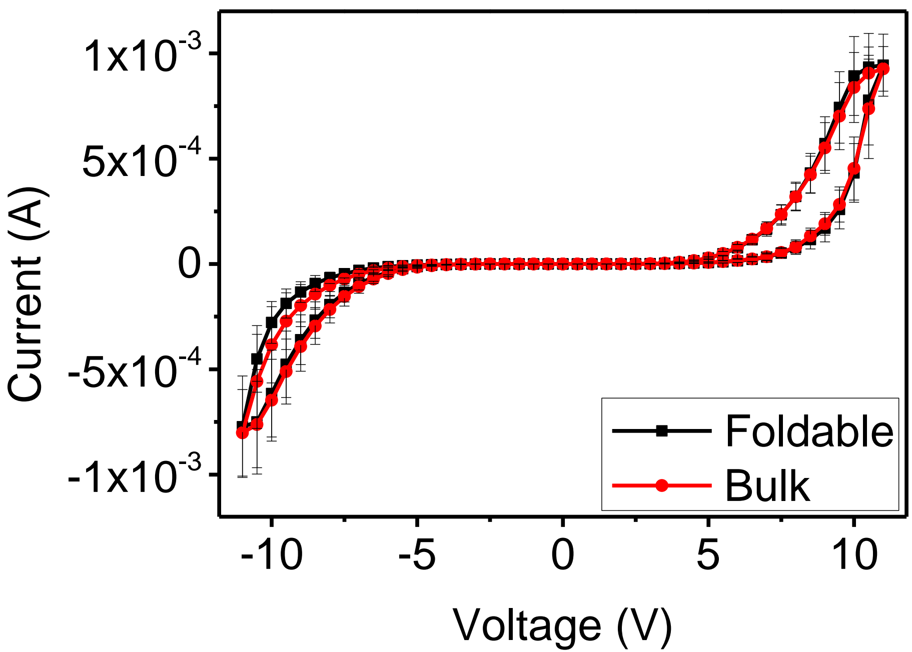


Figure 4.2.1: Basic IV hysteresis properties of foldable vs. bulk memristors

Furthermore, the devices were bent at different bending radii to assess the variability in performance while bent. Figure 4.2.2 shows the IV hysteresis curves for four different bending radii corresponding to a varying nominal strain of 0.042–0.125%. The superimposed curves show consistent functionality with varying width of the hysteresis loop, especially on the positive side. To quantify this difference, the value of high resistance state (HRS) and low resistance state (LRS) were measured and plotted against bending radius (Figure 4.2.3). The measurements are based on the simple average

of four overlapping cycles (Figure 4.2.4 shows overlapping last few cycles for a representative device) of the same device to ensure consistency. The conclusion to be drawn from Figure 4.2.2 and Figure 4.2.3 is that bending induces variations in R_{OFF}/high resistance state (HRS) and R_{ON}/low resistance state (LRS) values. The trend depicted in Figure 4.2.3 is not based on statistical analysis rather single devices with multiple sweeps. The observed trend is that LRS (R_{ON}) increases at lower bending radius and HRS (R_{OFF}) decreases, resulting in an overall degradation in the HRS/LRS ratio. This would impose limitations on the achievable bending of the flexible devices and would be an important issue for further investigations. Although several models have been extensively used [18–20], there is a need to develop new models to account for flexible devices as presented in this paper.

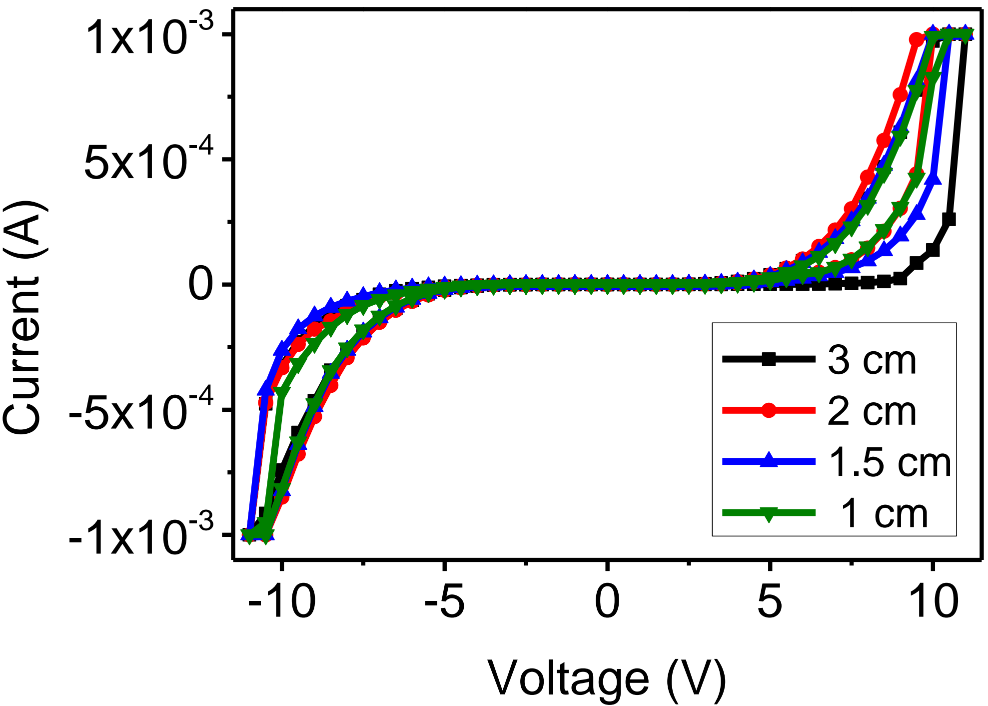


Figure 4.2.2: IV hysteresis loops for memristive devices at different bending radii.

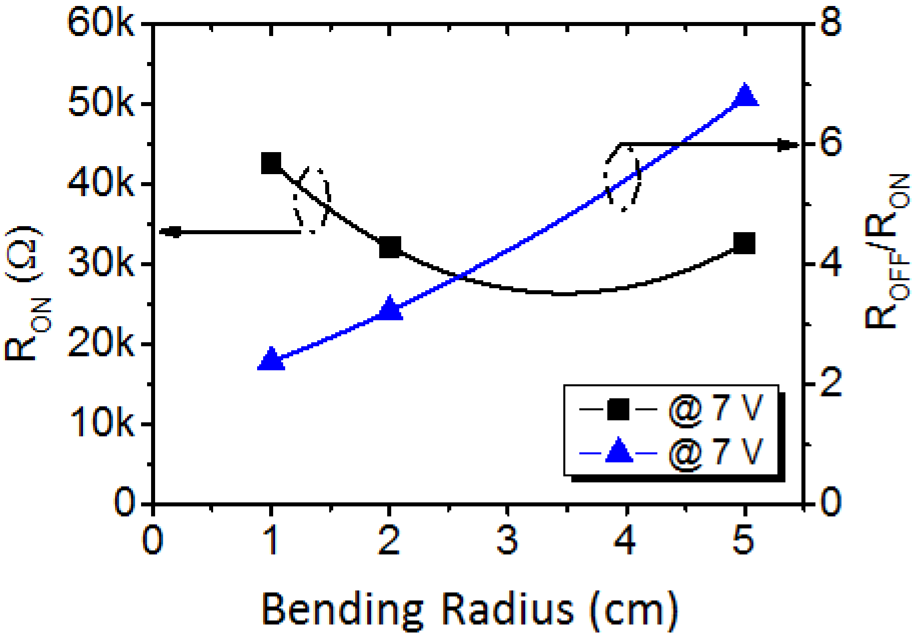


Figure 4.2.3: Variation of R_{ON} (left) and R_{OFF}/R_{ON} ratio (right) as a function of bending radius.

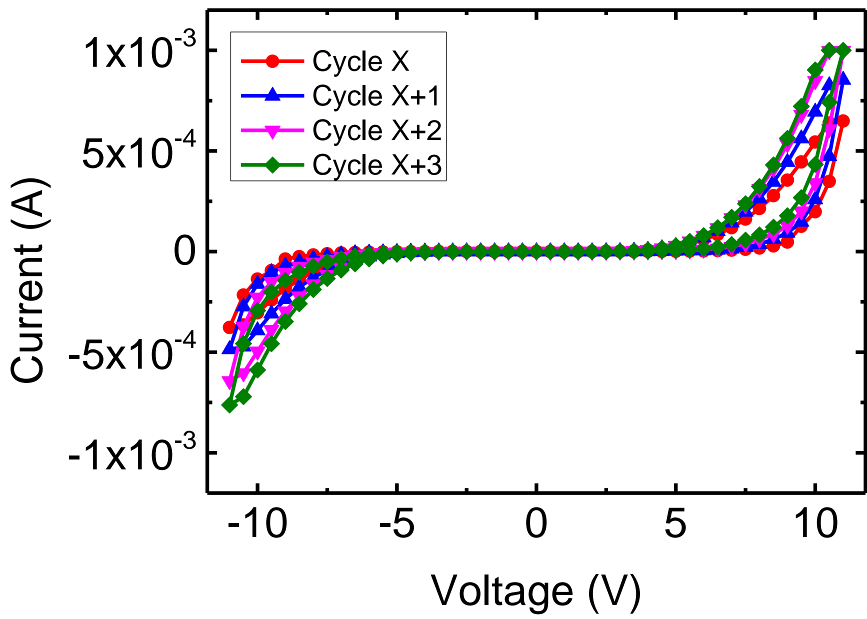


Figure 4.2.4: Overlapping cycles for a representative device.

4.3. Conclusion

The results show that the basic memristive IV properties of these devices match that of their bulk counterparts with no significant deviation. Further investigations are recommended on the effect of bending on the HRS/LRS ratio and possible mitigations. We believe our process offers a pragmatic step towards densely integrated memristive systems, structurally capable of mimicking our biological neuromorphic systems.

4.4. References

[1] Chua, L. O. Memristor-The missing circuit element. *IEEE Trans. Circuit Theory* 1971, 18, 507- 519.

[2] Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S. The missing memristor found. *Nature*. 2008, 453, 80-83.

[3] ITRS, DRAM and Flash Production Product Generations, 2011.

[4] Govoreanu, B.; Kar, G. S.; Chen, Y.Y.; Paraschiv, V.; Kubicek, S.; Fantini, A.; Radu, I. P.; Goux, L.; Clima, S.; Degraeve, R.; Jossart, N. 10×10 nm^2 Hf/HfO_x crossbar resistive RAM with excellent performance, reliability and low-energy operation. Electron Devices Meeting (IEDM), 2011 IEEE International , vol., no., pp.31.6.1,31.6.4, 5-7 Dec. 2011.

[5] Zidan, M.A.; Eltawil, A.M.; Kurdahi, F.; Fahmy, H.A; Salama, K.N. Memristor multiport readout: A closed-form solution for sneak paths. *IEEE Trans. Nanotechnol.* 2014, 13, 274-282.

[6] Jo, S.H.; Chang, T.; Ebong, I.; Bhadviya, B.B.; Mazumder, P.; Lu, W. Nanoscale memristor device as synapse in neuromorphic systems. *Nano lett.* 2010, 10, 1297-1301.

[7] Gorshkov, K.; Berzina, T.; Erokhin, V.; Fontana, M. P. Organic memristor based on the composite materials: Conducting and ionic polymers, gold nanoparticles and graphenes. *Proc. Comp. Sci.* 2011, 7, 248-249.

[8] Chou, K.I.; Cheng, C.H.; Zheng, Z.W.; Liu, M.; Chin, A. RRAM on flexible substrate with excellent resistance distribution. *IEEE Electron Device Lett.* 2013, 34, 505-507.

[9] Mondal, S.; Chueh, C.H.; Pan, T.M. High-Performance Flexible ReRAM Device for Low-Power Nonvolatile Memory Applications. *IEEE Electron Device Lett.* 2013, 34, 1145-1147.

[10] Cao, Q.; Kim, H.S.; Pimparkar, N.; Kulkarni, J.P.; Wang, C.; Shim, M.; Roy, K.; Alam, M.A.; Rogers, J.A. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* 2008, 454, 495-500.

[11] Li, L.; Ling, Q.D.; Lim, S.L.; Tan, Y.P.; Zhu, C.; Chan, D.S.H.; Kang, E.T.; Neoh, K.G. A flexible polymer memory device. *Org. electron.* 2007, 8, 401-406.

[12] Lee, K.H.; Lee, G.; Lee, K.; Oh, M.S.; Im, S. Flexible low voltage nonvolatile memory transistors with pentacene channel and ferroelectric polymer. Appl. Phys. Lett. 2009, 94, 093304.

[13] Gergel-Hackett, N.; Hamadani, B.; Dunlap, B.; Suehle, J.; Richter, C.; Hacker, C.; Gundlach, D. A flexible solution-processed memristor. *IEEE Electron Device Lett.* 2009, 30, 706-708.

[14] Rojas, J.P.; Sevilla, G.T.; Hussain, M.M. Structural and electrical characteristics of high-k/metal gate metal oxide semiconductor capacitors fabricated on flexible, semi-transparent silicon (100) fabric. *Appl. Phys. Lett.* 2013, 102, 064102.

[15] Rojas, J.P.; Hussain, M.M. Flexible semi-transparent silicon (100) fabric with high-k/metal gate devices. *Physica status solidi (RRL)-Rapid Research Lett.* 2013, 7, 187-191.

[16] Ghoneim, M.T.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Additive advantage in characteristics of MIMCAPs on flexible silicon (100) fabric with release-first process. *Physica status solidi (RRL)-Rapid Research Lett.* 2014, 8(2), pp.163-166.

[17] Rojas, J.P.; Ghoneim, M.T.; Young, C.D.; Hussain, M.M. Flexible High-κ/Metal Gate Metal/Insulator/Metal Capacitors on Silicon (100) Fabric. *IEEE Trans. Devices* 2013, 60, 3305-3309.

[18] Biolek, D.; Biolkova, V.; Biolek, Z. SPICE model of memristor with nonlinear dopant drift. *Radio Eng.* 2009.

[19] Kvatinsky, S.; Friedman, E.G.; Kolodny, A.; Weiser, U.C. TEAM: threshold adaptive memristor model. *IEEE Trans. Circuits Syst.* 2013, 60, 211-221.

[20] Radwan, A.G.; Zidan, M.A.; Salama, K.N. On the mathematical modeling of memristors. In 2010 IEEE International Conference on Microelectronics, 2010, pp. 284-287.

Chapter 5 Flexible FeRAM

Nanoscale transistors and ferroelectric capacitors are essential for ultra-large-scale-integration (ULSI) memories. The relatively simple metal-ferroelectric-metal structure of ferroelectric capacitors makes it relatively easy to fabricate and scale down (similar to metal-insulator-metal capacitors-MIMCAPs, and metal-resistive material-metal memristors). Analogous to MIMCAPs ability to store information as charge in a capacitor for volatile DRAM, and Memristors ability to store its bi-stable resistance information for non-volatile memory (NVM), ferroelectric capacitors bi-stable polarization states provide useful information for NVM applications. Due to the massive market of memory technology, volume manufacturing using CMOS process already offers significantly practical low-cost memory solution. Therefore, through a transfer-less process, we show a flexible version of a silicon based NVM ferroelectric capacitors using a 280 nm thick lead zirconium titanate (PZT).

Memory arrays have the largest number of transistors in an electronic system due to their high integration density. Typically, a unit memory cell (bit) consists of a storage device and a select transistor. A lead zirconium titanate (PZT) based ferroelectric memory storage device can switch in the pico seconds regime [1,2]. However, the actual memory speed is usually much slower than what can be realized due to the impedance of the drive and sense circuitry (i.e. transistors and word/bit lines capacitances)[3]. Hence, using polymer based transistors that have at least 20-40 times lower mobility (~10-12 $cm^2/V.s$) [4-6] compared to silicon (~200-400 $cm^2/V.s$) [7] is a key area of improvement, not to mention the effect on processor speeds. The main advantage of FeRAM compared to other non-volatile memory technologies is its low cost per bit, a dominant factor in the

memory market. In addition, FeRAM combines the advantages of NVM with a much faster access time and lower operation voltage [8,9]. In addition, two main problems with the state-of-the-art redox memories (memristors) are endurance and variability; current FeRAMs are better in both aspects [10]. FeRAM can be embedded monolithically in CMOS logic level fabrication with minimal extra processing steps, designed masks, and the associated costs (commercially available in Texas Instruments' microprocessors and Fujitsu's RF tags [11-13]). There are different types of memory architectures utilizing ferroelectric capcitors such as 1T-1C (unit cell consists of 1 access transistor and 1 storage ferroelectric capcitor), 2T-2C (unit cell stores data as two opposite values in two connected 1T-1C structures), and 1T (unit cell is a single transistor with ferroelectric material as gate insulator to access and store information as a shift in the transistor's threshold voltage) [14]. PZT is the preferred ferroelectric material in FeRAM because of its excellent properties. Although high-performance and reliable PZT FeRAM are readily available on silicon, a flexible version has never been achieved [6, 15, 16] and the crystallization bake required for PZT films (~700°C) which is much higher than widely used naturally flexible substartes like polymer, paper and fabric. Furthermore, owing to the monolithic integration ability of FeRAM with CMOS circuitry, PZT capacitors can be integrated on top of CMOS Integrated Circuits (ICs) without degrading its functionality. It has been reported that silicon based NMOS ICs can withstand up to 875 °C for 4 minutes without affecting its functionality [17]; therefore, the crystallization bake of PZT at 700 °C for 1 minute should not be an integration concern. Therefore, demonstration of a PZT based FeRAM on flexible silicon opens up a new area of innovation and technology transfer potential.

In this chapter, the ferroelectric devices were fabricated using state-of-the-art CMOS processes (sputtering, photolithography, and reactive ion etching (RIE)). The PZT film was spun using *sol-gel* technique plus associated pyrolysis and crystallization bakes. We characterized the PZT film's morphology using atmoic force microscopy (AFM). The crystallinity and dominant crystal orientation of the PZT film were extracted from a grazing incidence x-ray diffraction measurement (GI-XRD). The devices are then protected and an extra fabrication process of soft-backside etch [18] is performed to transform the 500 µm thick rigid and bulk silicon (100) substrate into a flexible 40 µm silicon with the pre-fabricated devices. Finally, the flexed devices are evaluated for key performance parameters at different bending radii corresponding to nominal strain values ranging from 0.04% (at 5 cm bending radius) to 0.4% (at 5 mm bending radius). The pre and post release state devices were characterized for electrical performance, like memory hysteresis, capacitance-voltage, current-voltage measurements, data retention, endurance, and imprint (the most critical for FeRAM failure) for different temperatures. Retention tests measure the ability of the FeRAM cell to retain the stored information over extended periods of time (>10 years). Endurance assessment provides information on the number of switching cycles (change of stored logic state between '0' and '1', write-erase cycles) that the memory cell can perform during its useful lifetime, and is strongly dependent on the operation frequency. The imprint phenomenon is critical in ferroelectric memory as it is the tendency of the memory cell to get stuck on a pre-stored state; in other words, one of the logic states becomes more preferred over the other. These critical aspects of NVM are thoroughly studied and compared with status-quo.

5.1. Device Fabrication

Bulk PZT FeRAM Capacitors' Fabrication:

Figure 5.1.1 highlights the main steps in fabrication for making bulk FeRAM ferroelectric capacitors. Figure 5.1.1a shows a bulk monocrystalline silicon (100) wafer with 300 nm of thermally grown SiO_2. A bilayer of titanium (10 nm)/ platinum (100 nm) is then sputtered without breaking the vacuum (Figure 5.1.1). Titanium is for adhesion and platinum acts as the ferroelectric capacitor's bottom electrode. Four layers of thin PZT ($Pb_{1.1}Zr_{0.48}Ti_{0.52}O_3$) film are then spin coated using *sol-gel* technique at 1500 rpm for 35 seconds. After each spin, a pyrolysis bake step at 350°C for 8 minutes each is performed. For final PZT crystallization, rapid thermal annealing (RTA) step at 700 C for 1 minute under Ar atmosphere is applied after the second and fourth layers (Figure 5.1.1c). Alternatively, RTA in oxygen atmosphere is recommended for improved results due to the correlation between PZT oxygen content and leakage current density [19]. The 4 spin coated PZT ceramic layers resulted in a 280 nm thick film. The top platinum electrode was then sputtered (Figure 5.1.1d) and patterned together with PZT film using positive tone photoresists (PR) ECI 3027 and a timed etch in a reactive ion etching (RIE) chamber maintaining a low power Ar plasma at low temperature (10°C) (Figure 5.1.1e,f). The ferroelectric capacitors in our study are squares with side lengths of 100 µm, 150 µm, 200 µm, and 250 µm, scalable down to 0.1 μm^2 (demonstrated in 2006 [20]).

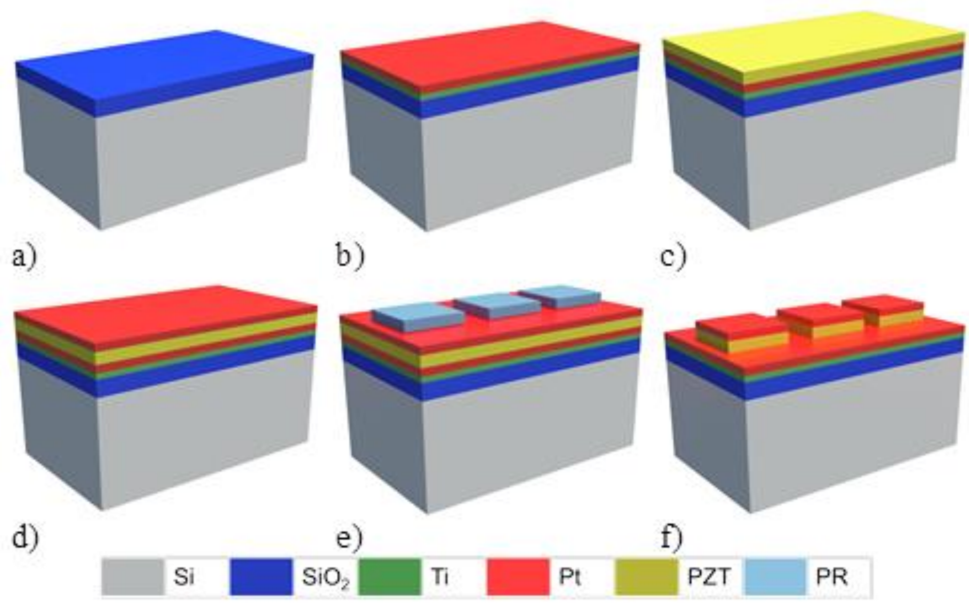


Figure 5.1.1 Fabrication process flow of bulk FeRAM

Transforming the Bulk Devices into Flexible FeRAM Capacitors:

The flexing approach followed in this work consists of a single extra processing step utilizing a deep reactive ion etching (DRIE). Figure 5.1.2 highlights the flexing process main steps. First the devices are protected using ECI 3027 PR (Figure 5.1.2a). Then, the sample is flipped upside down and etched in the DRIE chamber for few hours until the desired thickness is reached (Figure 5.1.2b). We have previously reported an alternative flexing approach (trench-protect-release-reuse) for making various flexible devices (metal/insulator/metal capacitors for DRAM [21-23], memristors for ReRAM [24], metal/oxide/semiconductor capacitors and field effect transistors [25-28], FinFET [29], and thermoelectric generators [30]) on a flexed silicon substrate.

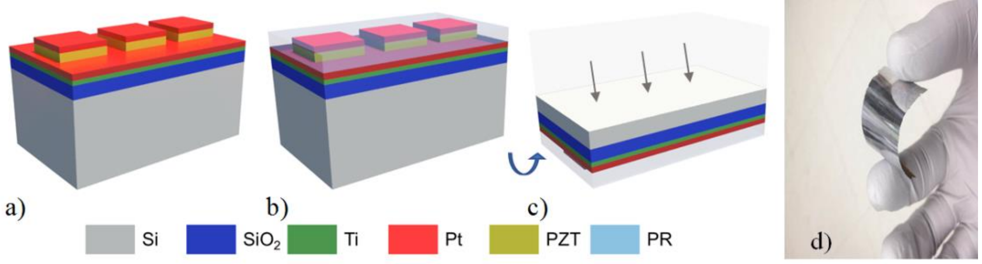


Figure 5.1.2: Fabrication process flow for flexing the silicon substrate. (a-c): silicon substrate with pre-fabricated FeRAM devices undergoes soft etch back process (upside down) to thin down the substrate to achieve an ultra-thin version of flexible silicon with pre-fabricated devices (d).

5.2. Device Characterization

Memory Properties of Bulk PZT FeRAM Capacitors:

The PZT film crystallinity is assessed through a GI-XRD measurement at incidence angle (ω) of 4° confirming polycrystalline nature with (110) as the prominent crystal orientation (Figure 5.2.1a). Figure 5.2.1b shows the morphology of the final PZT ceramic layers acquired from an intermittent mode AFM measurement of a $10 \times 10\ \mu m^2$ area. The film had an average surface roughness (R_a) of 0.62 nm and root mean square roughness (R_{rms}) of 0.81 nm, with scattered pinholes of ~5-6 nm deep (Figure 5.2.1c shows the height profile at the dashed line in Figure 5.2.1b). The small surface roughness indicates a high quality smooth surface and consequently a good interface with the top platinum electrode. This formation of pinholes issue can be mitigated by surface pre-treatment of the bottom electrode or alternative sputter deposition at elevated temperatures [31,32]. Figure 5.2.1d shows a scanning electron microscope image of the transformed 40 µm flexible bearing the FeRAM memory devices.

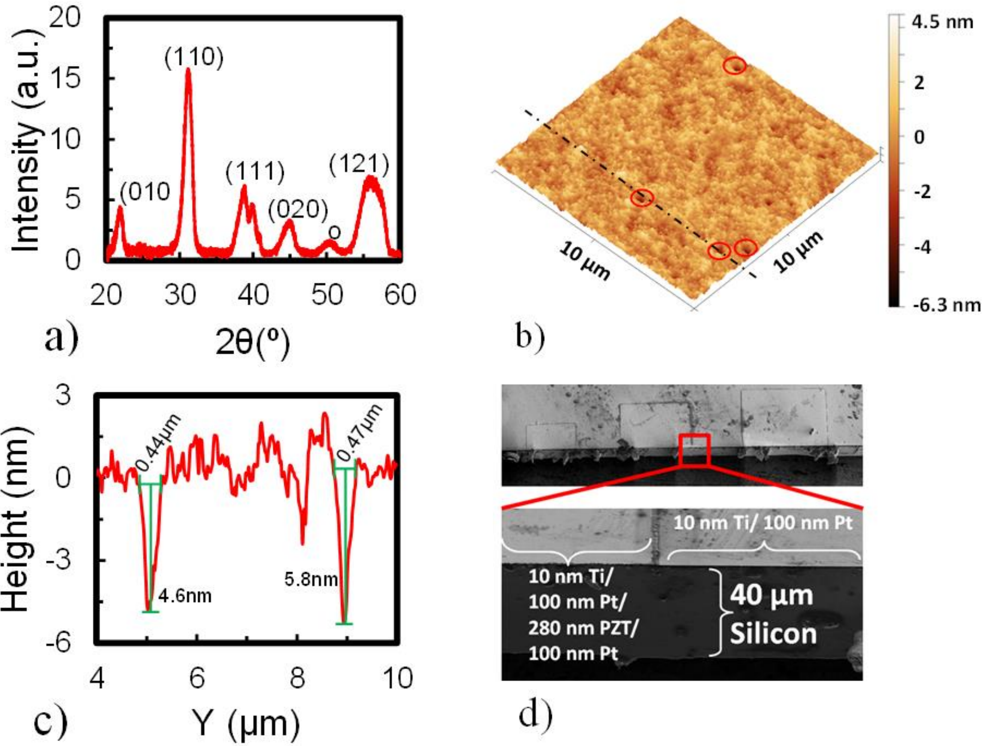


Figure 5.2.1: a) Grazing incidence X-ray diffraction (GI-XRD) of as deposited PZT thin film, b) atomic force microscopy (AFM) measurement, c) height profile of the dotted line in part (b), and d) scanning electron microscope (SEM) cross-section image depicting the thickness of the final fabric.

The electrical characterization measurements were performed on an aixACCT TF Analyzer 2000E which utilizes the feedback virtual ground method (Figure 5.2.2c, inset). This method ensures that although the cables capacitances are in place; they are electrically ineffective. Figure 5.2.2a shows the basic polarization vs. electric field behavior of the ferroelectric memory, exhibiting a positive remnant polarization (Pr_+) of 13.5 µC/cm^2, a negative remnant polarization (Pr_-) of -11.5 µC/cm^2, and coercive electric fields (Ec) of 50 kV/cm and -60 kV/cm for Ec_+ and Ec_-, respectively. The higher remnant polarization values are desirable for facile detection of switching while reading memory cells and, thus, adding immunity to bit reading errors. The relatively low coercive electric fields are key enablers for low operation voltage FeRAM. The Pr_+ state corresponds to a

digital memory bit “0” and Pr_- corresponds to a “1.” In the actual FeRAM memory array, it is the difference between switching and non-switching currents that determines the state of the stored bit [33]. The post-fatigue plot shows the behavior of a representative device after suffering from consecutive switching cycles and dropping its remnant Pr values to ~20% of the pre-fatigue state. Fatigue is a phenomenon experienced by ferroelectric thin films when subjected to alternating switching pulses due to trapping of defects at the interfaces between ferroelectric/electrodes and grain boundaries of the polycrystalline film, resulting in loss of polarization [34]. Figure 5.2.2b shows the current-voltage behavior vs. time behavior for a positive up negative down (PUND) measurement when a ± 15 volts pulse of 100 µs duration is applied. Lower voltages down to 3 volts were also achieved. Lower operation voltages result in lower remnant polarization. In contrast, maximum operation voltage ensures that the collected fatigue, endurance, and retention data are at the highest possible degradation conditions. Hence, our results and analysis are based on the 15 volts maximum operation voltage for assessing the memory devices reliability aspects. In a FeRAM memory array, the resulting currents due to switching/non-switching is then passed to a sense resistor and converted into a voltage level that is then passed to a comparator circuitry to determine if the read state is a “0” or a “1” bit. The difference between the two voltage levels is referred to as the memory window. Thus, there is a proportionality relation between the difference in switching and non-switching currents and the memory window. To study the effect of the pulse width of the applied voltage signal on the memory window, the percentile lost in memory window due to the reduced pulse width (faster switching) is depicted in Figure 5.2.2c. Acceptable operation speed would be up to 0.5-1 µs at which

~15-20% of memory window is lost. The 0.5 μs represents the fastest switching time for polymer based FeRAMs. It is important to distinguish the ability of PZT to switch as a material in the pico seconds regime and the read/write speed of an actual memory array due to bit/word line capacitances and drive and sense circuitry delays (70 ns is the fastest reported) [35]. Figure 5.2.2d shows the capacitance-electric field measurement of the PZT ferroelectric capacitors, indicating maximum capacitance around E_c fields and lower values as electric field increases due to space-charge depletion near the PZT/electrode interface [36]. Figure 5.2.3 provides a simple polarization and capacitance behavior variation analysis in terms of cycle-to-cycle variability for ten consecutive cycles (Figure 5.2.3a,c) on the same device, and device-to-device variability for ten random devices (Figure 5.2.3b,d). The plots are for average values and the error bars represent the standard deviation, insets show the actual plots for the first and tenth cycles.

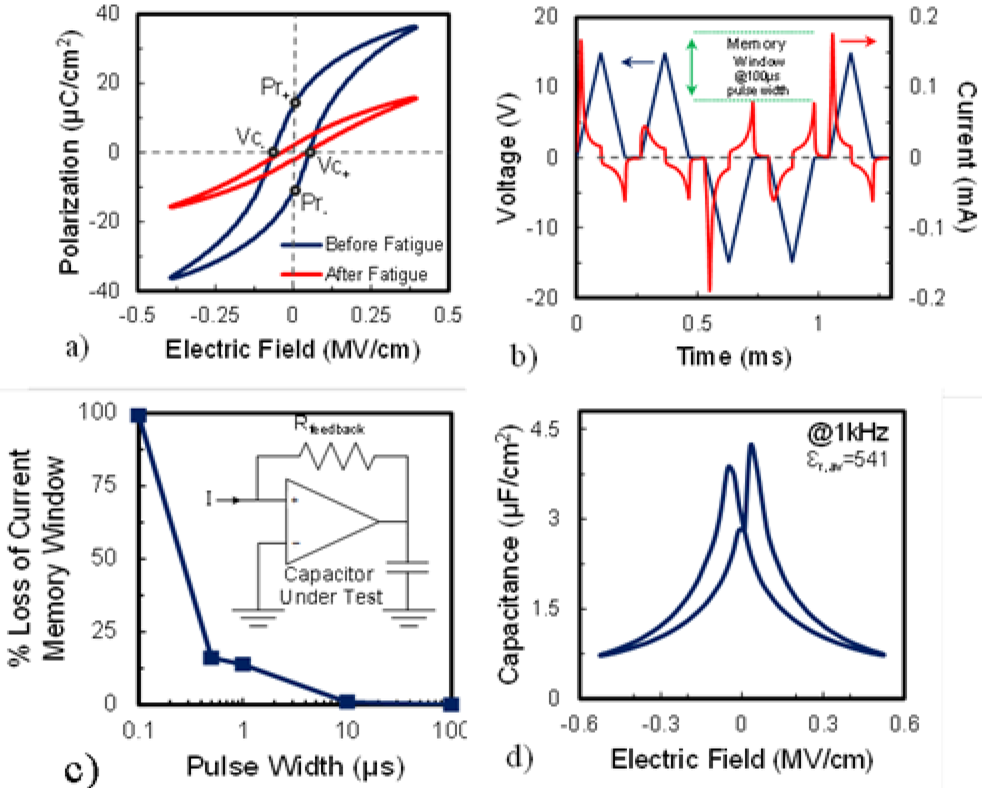


Figure 5.2.2: Representative plots for various ferroelectric memory properties; a) Basic polarization-electric field plot, b) current-voltage plot *vs.* time for memory window extraction, c) percentage loss of current memory window versus pulse width, *inset* showing the schematic of the virtual ground feedback method used for eliminating connection parasitics from actual device measurements, d) capacitance-electric field plot of ferroelectric memory

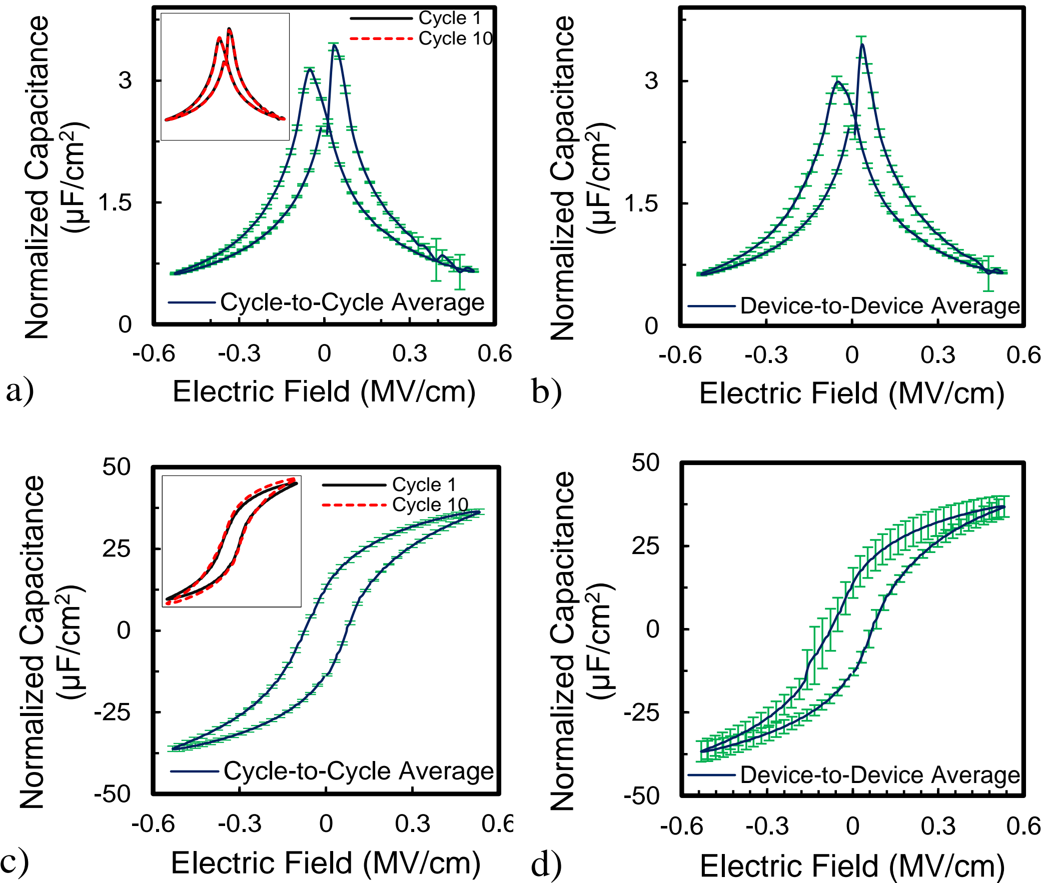


Figure 5.2.3: a) Cycle-to-cycle capacitance variation of ferroelectric memory, inset showing 1st and 10th cycles, b) device-to-device capacitance variation for 10 devices, c) cycle-to-cycle polarization variation, inset showing first and tenth cycles, d) device-to-device polarization variation for 10 devices.

Reliability issues of FeRAM are, then, attested using imprint, endurance, and retention tests. Imprint is one of the most critical issues for FeRAM and its rate increases with temperature. Imprint is the tendency of the ferroelectric capacitance to maintain one state over the other when it stays in that state for long durations. Figure 5.2.4a shows the shift in the coercive voltage due to ferroelectric imprint at 125°C for different bias voltages. The elevated temperature is to amplify the imprint effect to be able to assess over short durations. Figure 5.2.4b shows the reversibility of the imprint phenomenon through applying a constant bias voltage for a brief amount of time to restore the perfect

symmetry of the device. Figure 5.2.4c shows the fatigue test results of the ferroelectric capacitors at different disturbance electric fields (E_c ~70 kV/cm, intermediate electric field (E_{im}) ~210 kV/cm, and saturation electric field (E_{sat}) ~ 700 kV/cm) at a fatigue frequency of 20 kHz and hysteresis measurement at ± 10 V at 1 kHz. The devices lost ~50% of P_r after 10^6 switching cycles. These results depend heavily on the fatigue frequency that similar devices subjected to E_{im} can survive up to 10^9 cycles (compared to 10^3-10^7 for flash memories) [10] before losing 50% of their polarization at 1 MHz (Figure 5.2.4d). Figure 5.2.4e shows the stable value of non-volatile charges (dP_{sw}) (i.e. the difference between switching, P_{sw}, and non-switching, P_{nsw}, polarizations). Retention tests show that the cells can retain information for long durations at room temperature (25°C), fluctuations start to show up at 150°C, and at 200°C ~30% of P_r is lost (Figure 5.2.4f) (at room temperature the theoretical rentention would be infinite for our PZT FeRAM since 100% of the data is retained even after 10^5 s, practically it should retain data for 10 years (best projected) — best demonstrated for FeRAM is 3 days (2.5 x10^5s)) [37].

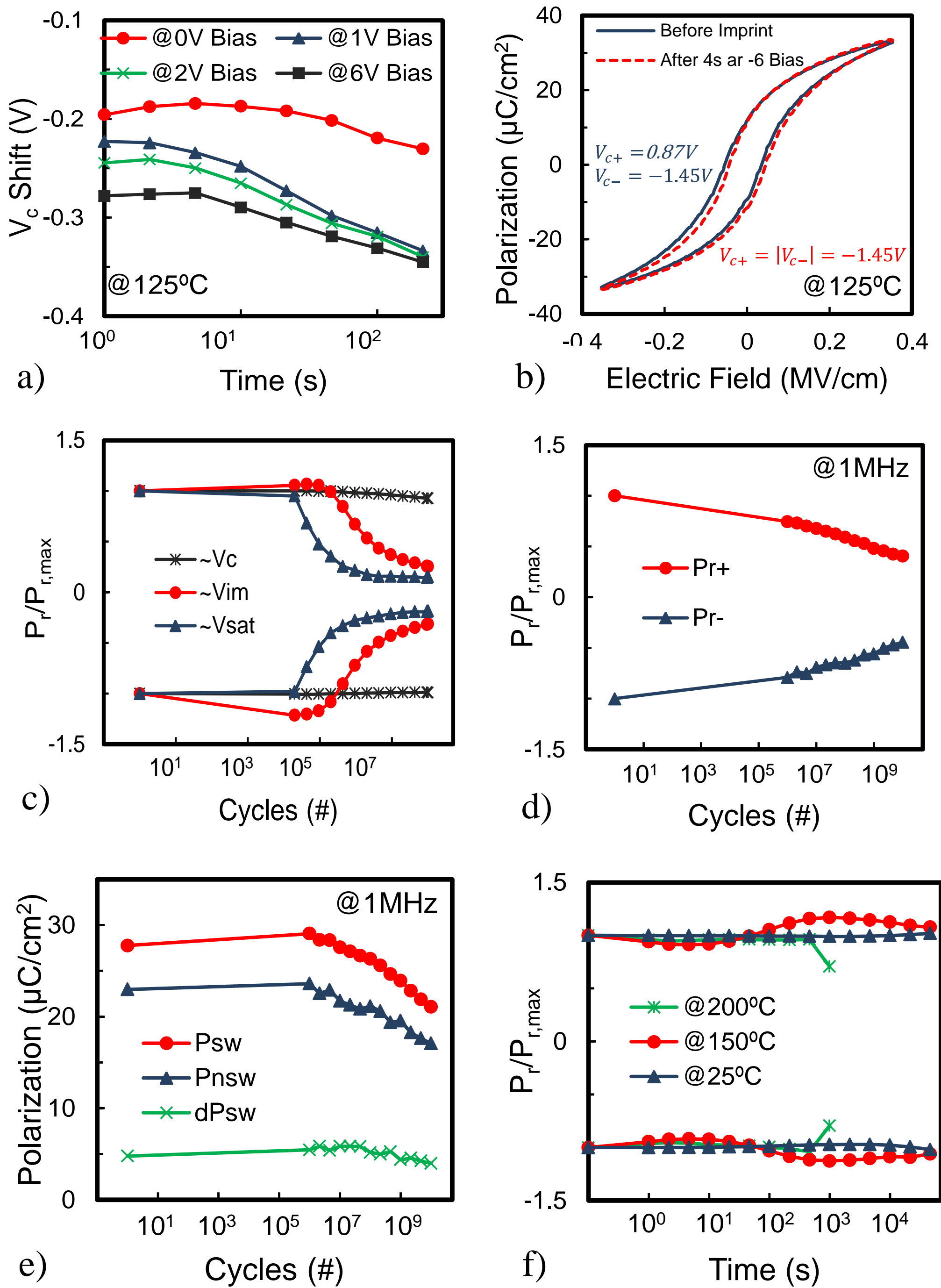


Figure 5.2.4: a) Fatigue test for ferroelectric capacitors at different disturbance signal's amplitudes, b) fatigue test results at 1 MHz, c) non-volatile charges stability assessment as a function of switching cycles, d) retention measuremet at various temperatures, e) imprint test of ferroelectric capacitors at different bias voltages at 125°C, and f) restored symmetric behavior after applying a constant bias voltage to counteract the imprint effect.

Memory Properties of Transformed Flexible PZT FeRAM Capacitors:

ULSI chips for data management require integrated circuits with areas in the cm^2 regime. Furthermore, roadmap wise, there are two main reasons why a flexible version of FeRAM is needed for future generations of flexible electronics. First, the future of flexible electronics as a vision extends to a fully flexible processing unit that can perform key computations. Hence, it is not the size of the FeRAM that is in question but rather the size of the micro-processor that has the embedded FeRAM. The size of state-of-the-art commercial processors is around $2.25\ cm^2$ (22 nm technology). Monolithic integration ability is also a critical concern. In order to have high performance compact flexible electronic systems, we need all the main components including memory and logic blocks to be built on the same substrate which has to be flexible. Otherwise, the small memory module that is inflexible has to be connected to other blocks through bonding which imposes alignment challenges and adds unnecessarily bulky components to the system. To this end, flexible state-of-the-art FinFETs on silicon, using the same processes used in this work, have been reported [18], and this is the first time flexible non-volatile PZT ferroelectric capacitors on silicon are reported and fully characterized. Both are key enabler elements for fully flexible monolithically integrated electronic systems. The second main reason is application dependent, for instance a few mm^2 area would not be necessary to flex when the application is a curved big TV screen but when the application is wrapping around a fingertip, then flexing becomes necessary. Status quo of FeRAM is that even low storage sized FeRAMs have cm scale dimensions (for instance, Fujitsu's 4MB FeRAM nonvoltaile memory MB85R4M2T is ~1.5 cm^2 and Texas Instruments

embedded 128KB FeRAM Microcontrollers (MSP430FRxx FRAM) all have dimensions in excess of 1 cm). The flexible memory devices bearing silicon is 40 μm thick and the minimum bending radius achieved is 5 mm. Figure 5.2.5 summarizes the properties of the flexible memory devices. All plot lines are based on average values of seven new devices with error bars representing standard deviation. Evidently remnant polarization and capacitance mildly decrease as bending radius decreases (Figure 5.2.5a,b). This is due to the increased mechanical stress (nominal strain, $\varepsilon_{nominal} = t/2R$, where t is substrate thickness and R is the bending radius, i.e. at minimum bending radius of 0.5 cm, the devices experience 0.4% nominal strain). H. Zhu *et al.* showed that PZT remnant polarization decreases linearly with increased applied mechanical stress due to lattice distortions [38]. To mitigate the experienced nominal strain, a thinner substrate can be made. Thinner silicon is a possible optimization that would also reduce the minimum bending radius achievable due to the inverse proportionality between flexibility and substrate thickness. Figure 5.2.5c shows the fatigue variation for an array of devices at 5 cm bending radius, confirming negligible variability. Hence, the fatigue improvement translated to ~15% increase in retained data after 10^{10} cycles in Figure 5.2.5d can be safely attributed to the increased bending rather than the device variability. The relationship between fatigue behavior and mechanical stress due to bending has not been explored for this work but these results suggest that the topic should be interesting for future investigation.

Finally, the flexible ferroelectric memory devices were tested after 100s of bending cycles at minimum bending radius (5 mm). Figure 5.2.5e,f show the polarization and capacitance plots after the 10th and the 1000th bending cycles, showing insignificant

performance deviations. The devices' retention ability was also preserved after 1300 bending cycles at minimum bending radius (Figure 5.2.5g).

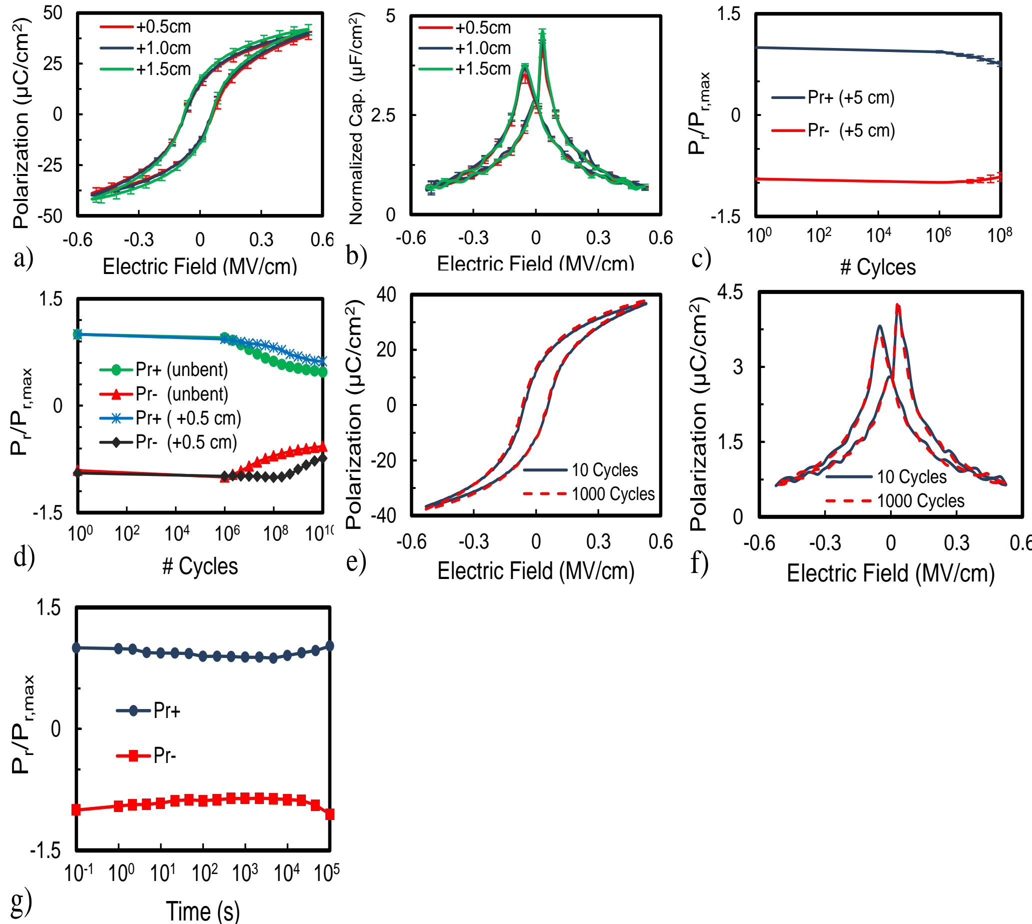


Figure 5.2.5: a) Polarization, b) capacitance, and c) fatigue behavior variation at different bending radii (lines represent averages of 7 devices with error bars representing standard deviation), d) fatigue enhancement at minimum bending radius, e) basic hysteresis plot for polarization versus applied voltage after 1000 bending cycles at minimum radius (5 mm), f) capacitance-voltage plot after 1000 bending cycles at minimum radius, and g) representative retention polarization plot of a device after 1300 bending cycles at minimum bending radius.

Overall, the flexible ferroelectric capacitors utilizing PZT on silicon exhibited (i) excellent flexibility, matching that of FeRAM built on naturally flexible polymeric substrates using organic molecules and inkjet methods [15,39]; (ii) record capacitance and polarization values compared to other polymer based flexible FeRAMs; (iii) record

endurance for flexible FeRAM at 1MHz operation frequency; (iv) uncompromized retention capability even after 1300 bending cycles at 5 mm radius; (v) manufacturability due to usage of CMOS technology based silicon platform and commercial availability of PZT [40]. Furthermore, the thin PZT film reduces the coercive voltages required for switching the devices and the cost effectiveness of the process, and supports lateral dimensions' scaling for ULSI density ferroelectric memory. Table 5.2.1 summarizes the progress to date towards flexible FeRAMs over the past few years and the presented work. The shaded cells are for best reported values where this work stands out well except cell size which is limited due to our own lithographic capability. This is subject to further optimization as bulk inflexible PZT cells of 0.1 μm^2 has been previously reported [20]. Furthermore, the better values for flexible PZT memory cells on platinum foil are first achieved on silicon. The last step in the reported fabrication flow was peeling-off the Pt/PZT stack from silicon substrate. Hence, the same process could be applied until the last step while replacing peeling off with soft-back etch of the silicon substrate leading to similar performance. The higher capacitance is desirable to stand out from memory array bit line capacitance. The lower the switching time, the higher the memory acceptable operation frequency. Due to the difference between silicon's melting point (~1400°C) and that of most polymeric substrates (~200°C), this work's flexible ferroelectric memory on silicon can withstand much higher temperatures. Fatigue values are reported for the number of cycles at which the memory cell retains more than 50% of the its initial remnant polarization. The higher the disturbance frequency the lower the fatigue experienced by the material. Since PZT memory cells can function at 1 MHz (higher than acceptable operation frequencies for P(VDF-TrFE)), it survives 100 times more cycles

when unbent and 1000 times when bent at minimum bending radius (5 mm). PZT retention properties are well known ~infinity, as evident from the 0% data loss after ~10^5 s (Figure 5.2.5g). Owing to the robustness of silicon and associated processing techniques out of 50 tested devices, only two were initially short circuited. Indeed, PZT is expected to have higher switching currents given the fact that it has higher normalized polarization per unit area (i.e. more polarization charges) and fast switching ability (up to 10 ns). Since current is equal to the rate of change of charges with time; therefore, the more charges and fast switching time both contribute to much higher currents compared to organic FeRAMs. Nonetheless, PZT FeRAM is still desirable for low power applications because of the overall low switching energy requirement for write-erase cycles (down to 200 fJ/bit) [52]. Our fabricated FeRAM capacitors require ~20 nJ per write-erase operation. The lower switching currents renders FeRAM, in general, and PZT, specifically, suitable for low power non-volatile memory applications. Most interestingly, the minimum bending radius achieved on our 40 µm silicon was the lowest among all reported values for polymeric substrates since 2010. Furthermore, the devices survived after 1000 bending cycles at 5 mm bending radius with no observable performance deviation compared to 500 bending cycles highest reported for polymeric devices at 11 mm radius. It is to be noted that although thicker PZT ceramic layers are desirable for lower leakage currents, larger domain size, and high remnant polarization; they are not economically feasible. For instance, *sol-gel* PZT solutions cost ~$100/ml. Standard flow is composed of 24 spin coatings to achieve a 2 µm thick PZT layer. For an industrial 8" wafer, the cost per wafer using standard flow amounts to ~ $6 (0.06 ml for 2 µm thick PZT layer) just for the amount of PZT that remains on the wafer. Alternatively, we have

shown 4 ceramic layers of *sol-gel* PZT resulting in a 280 nm thin film PZT that exhibits excellent flexible ferroelectric memory performance compared to polymeric ferroelectric based memories for 14% of that cost. Furthermore, the PZT film has area of improvement in terms of removal of pinholes, annealing in an oxygen rich environment, or deposition of a passivation layer to prevent degradation. All stack patterning was done using timed etch in Ar plasma with no specific etching gases. To this end, our thin film PZT FeRAM memory opens up an opportunity to low cost batch fabrication of flexible, and yet, high performance non-volatile memory applications. Finally, the core value of utilizing silicon‘s flexing ability is the compatibility of the process for monolithic integration with CMOS electronics which is only possible for our flexible silicon based ferroelectric memory. Indeed, our focus is not reporting state-of-the-art FeRAM neither in terms of scaled dimensions nor best performance but rather, this work shows that state-of-the-art FeRAMs built on silicon can be made flexible using our processes without compromising functionality or reliability. For example, in 2013, Texas Instruments showed 180 nm FeRAM nodes using 70 nm thick metalorganic chemical vapor deposited (MOCVD) PZT with1.5 V operation voltage and $>10^{15}$ write/read cycles.[54] Worth mentioning, there are significant cost advantages using our sol-gel technique versus the expensive MOCVD technique; however, utilizing the results of this work and Texas Instruments‘ reported FeRAM, a flexible version of the 70 nm thick PZT based, 180 nm FeRAM, with 1.5 V operation voltage on silicon is feasible.

Table 5.2.1: Summary of research progress in flexible ferroelectric memory devices over the past few years.

Reference	This Work (2014)	M. Li *et al.* (2013)[41]	U. S. Bhansali *et al.* (2013)[42]	Y. Song *et al.* (2012)[43]	W. Y. Kim *et al.* (2012)[44]	Z. Zou *et al.* (2012)[45]
Ferroelectric Material	PZT	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE) and $BaTiO_3$ nanofiber	P(VDF-TrFE)	PZT
Flexible Substrate	Silicon	Organic	Organic	Organic	Aluminum Foil	Platinum Foil
Transfer Required	No	No	No	No	Yes	Yes
P_r ($\mu C/cm^2$)	18	7	6.7	5	11	25.5
P_{max} ($\mu C/cm^2$)	38	--	--	9.3	18	60.8
E_C (MV/m)	6	120	55	37	83	5.49
E_{Sat} (MV/m)	40	250	120	--	120	20
Capacitance($\mu C/cm^2$)	4	--	0.045	--	--	--
Speed (μs)	0.5	--	--	--	--	--
Temperature(°C)	>300	--	--	--	--	--
Fatigue (Retains >50% of P_r)	10^9 (unbent) $>10^{10}$ (bent)	--	10^5	--	--	10^7
Retention	>10 years	--	--	--	--	--
Cell Size (mm^2)	0.01-0.0625	0.059-1.38	--	--	0.025	0.00785
Yield	>95%	--	--	--	--	--
Minimum Bending Radius (mm)	5	--	--	--	6	--
Bending Cycles	1000 @ 5 mm radius	--	--	--	500 at 11 mm radius	--
Suitable for Monolithic Integration with CMOS	Yes	No	No	No	No	No

Reference	M. A. Khan *et al.* (2012)[46]	M. A. Khan *et al.* (2011)[47]	S.-M. Yoon *et al.* (2011)[48]	D. Mao *et al.* (2010)[49]	D. Mao *et al.* (2010)[50]	D. Mao *et al.* (2010)[51]
Ferroelectric Material	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)	P(VDF-TrFE)
Flexible Substrate	Organic	Organic	Organic	Organic	Organic	Organic
Transfer Required	No	No	No	No	No	No
P_r ($\mu C/cm^2$)	7.4	7.5	9.1	7	7	7.4
P_{max} ($\mu C/cm^2$)	9	--	--	8.5	8	8.5
E_C (MV/m)	--	60	52.2	--	--	50
E_{Sat} (MV/m)	--	--	120	75	140	95
Capacitance($\mu C/cm^2$)	0.065	--	--	0.15	--	0.062
Speed (µs)	10,000	--	--	10	--	--
Temperature(°C)	--	--	--	100	--	--
Fatigue (Retains >50% of P_r)	10^6	10^6	--	--	10^6	--
Retention	--	--	--	--	--	--
Cell Size (mm^2)	--	--	0.000625-0.04	--	--	0.03-0.25
Yield	--	--	--	--	--	--
Minimum Bending Radius (mm)	--	--	6.5	--	--	--
Bending Cycles	--	--	--	--	--	--
Suitable for Monolithic Integration with CMOS	No	No	No	No	No	No

5.3. Harsh Environment Analysis

Recently the potential application of lead zirconium titanate (PZT) in high-temperature harsh environments has gained interest. Owing to the material's high Curie temperature (T_C~390°C) [53], Lead Pb^{+2} based piezoelectric sensors and actuators are desirable in petrochemical deep oil well drilling, automotive fuel injectors, and aerospace monitoring of deep space probes applications [53-57]. Actual PZT sensors suitable for high-temperature high-pressure environments have already been reported [56]. Although PZT exhibits ferroelectric as well as piezoelectric properties [58-62], utilizing its ferroelectric properties in high temperature applications has not been equally explored. Various PZT thin film optimizations and scaling down of device dimensions have already been studied as PZT is the most widely used material in today's commercial FeRAM [11,12,20]. Previous studies have been done on the reliability of PZT based ferroelectric memories under high temperatures up to 350 K (177 °C) [63]. Today, harsh environments require electronics that can collectively function above 200°C, withstand high pressures, and fight corrosive environments (O_2, and H_2O vapor rich) [54]. It has been reported that PZT (52/48--$PbZr_{0.52}Ti_{0.48}O_3$) loses up to 45% of its polarization on applying 1.5 GPa mechanical compression whereas PZT (95/5-- $PbZr_{0.95}Ti_{0.05}O_3$) can get totally depolarized (dysfunctional) [64]. This necessitates the study of the combined effect of high-temperature and high-pressure combined, if the devices are to be functioning in such harsh environments. Moreover, there is an increased demand for automation and deployment of robotic systems in harsh environments such as off-shore oil and gas rigs [65] which can heavily benefit from the introduction of a flexible high density memory module. A fully flexible electronic system that can affix and conform to any non-planar

surface needs an integrated flexible memory for several critical functions, such as programming and data storage [66, 67]. Continuous data transmission to cloud from various nodal system deployed in a cyber-physical system will require excessive amount of power and centralized processing and storage of data will cause more power consumption and will expose the data to potential vulnerability through cyber security challenges. Therefore, in-situ data processing storage and transmission of only filtered critical data are better options for efficient information and energy management. Thus, built-in data processing unit and memory components are going to be integral parts for such electronic systems. All tests were carried out at 1.25 cm bending radius state (bending upward) under ambient conditions (a gas mixture of 78% nitrogen, 21% oxygen, and ~1% argon).

The ultra-thin flexible ferroelectric memory array was bent on a 2.5 cm diameter metallic cylinder stub brought in contact with a thermal chuck (Figure 5.3.1(a) inset). All measurements were taken using aixACCT TF Analyzer 2000E utilizing the feedback virtual ground method in which connection cables' capacitances are electrically inactive. The temperature was varied in steps of 50 °C from room temperature at 25 °C up to 225 °C under ambient conditions. This wide temperature range covers the targeted harsh/extreme environment applications: (i) oil and gas industry's deep well drilling temperature requirements are similar to inside a combustion engine in hot weather ~200 °C [55, 68, 69]; (ii) a space craft on a mission to Mercury's temperature requirements are 175 °C and NASA's extreme temperature electronics program has testing facilities for up to 250 °C [70]; and (iii) moreover, silicon is limited in electronic performance to below 250 °C (thermal insulating packaging techniques can let devices survive higher external

temperatures) [71]. To overcome that, using silicon carbide or gallium nitride as base platform for future applications can open up new paradigm of memory devices. The bent devices experienced a constant high-pressure of 260 MPa (operation pressure in deep wells~20,000 psi [55] which is equivalent to 138 MPa), resulting from the tensile stress due to bending the ferroelectric memory devices at 1.25 cm bending radius throughout the measurements. Although the substrates mechanical flexibility allowed a bending radius down to even 0.5 cm [72], the anomaly in retention behavior at this radius at room temperature did not allow for a lower curvature measurement. The tests were carried out under ambient conditions with typical humidity (55%) level in Saudi Arabia (it is to be noted that harsh environments have humidity levels ranging from 10- 100%) [69]. Figure 5.3.1 shows the cycle-to-cycle variation of polarization *vs.* voltage bias (a) and capacitance *vs.* voltage bias (b) for 10 consecutive cycles, at 1 KHz frequency. The error bars represent standard deviation (~2.5% for polarization values between P_r and saturation polarization (P_{max}) and ~1.7% for capacitance values). Hence, same device is characterized at different temperatures except for retention and fatigue tests at 25 °C and 225 °C due to the destructive nature of the measurement.

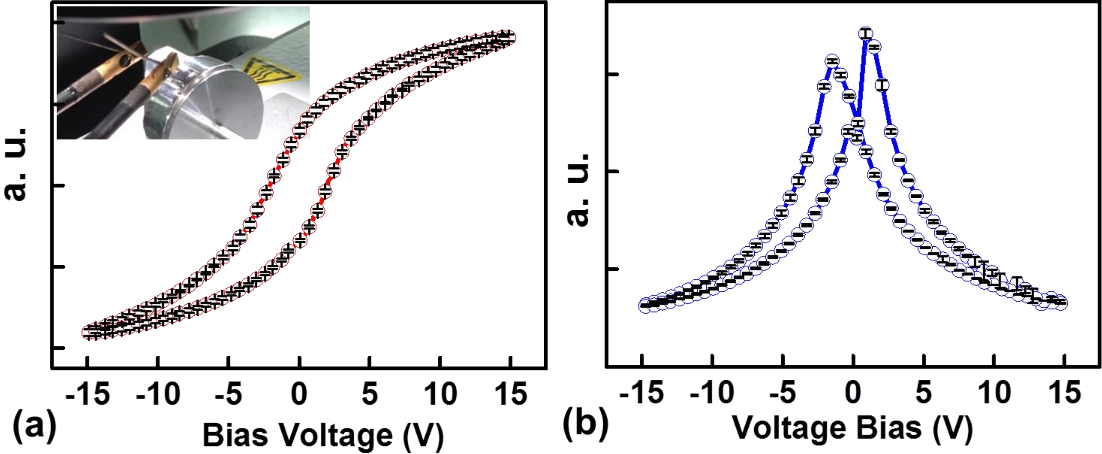


Figure 5.3.1: Cycle-to-cycle variation in polarization of the memory devices (a), inset showing the physical set-up utilizing a 2.5 cm diameter metallic stub, and capacitance (b) behavior of flexible ferroelectric PZT memory capacitors.

The flexible PZT ferroelectric capacitors function as the storage element in FeRAM, where the two possible polarization states of the devices correspond to a binary value ("0" or "1"). Therefore, it is critical to have two distinguishable polarization states with sufficient charges. Figure 5.3.2 shows the polarization *vs.* applied voltage (Figure 5.3.2(a)), the change in P_{r+}/P_{r-} and V_{c+}/V_{c-} (Figure 5.3.2(b)), and the change in P_{max+}/P_{max-} (Figure 5.3.2(c)) at different temperatures. One of the most critical reliability aspects of FeRAM is imprint, which is the device preference to stick to specific memory state and is worsened by high temperatures. The imprint property is usually manifested as a shift in the coercive voltages shifting the hysteresis plot laterally and increasing one of the polarization state at the expense of the other [73]. However, the plots show that although V_{c+} decreased with temperature; V_{c-} did not increase with an equivalent amount. In addition, there is a similar decrease in P_{r+} and P_{r-} values which in case of imprint should have compensated each other. Finally, the reduction in P_{max} values confirms that the observed trend is due to the combined thermal and mechanical stress the devices are

exhibiting, not imprint phenomenon. As temperature increases, the ability of interfacial traps at the PZT/electrodes interface are more able to respond to high frequency alternating small signals; hence, they do not contribute anymore to the hysteric behavior of the devices [63]. This explains the observed anomaly in the behavior of coercive electric fields: initially, the devices had interfacial traps concentrated at the interface between the top Pt electrode and the PZT thin film due to the exposure of PZT to ambient during the transfer from the RTP to the sputtering step. This also happens after sputtering the bottom Pt electrode and before spinning PZT but Pt, as an inert metal, is much more durable and resistant to contaminants than PZT. For instance, it has been reported that the properties of PZT films are intensely sensitive to vapor H_2O in air [74]. This means that the interface at the PZT/top electrode has significant traps and defects introduced during the process compared to the bottom electrode/PZT interface. The decrease in V_{c+} with temperature indicates that these traps have a net negative polarity, possibly due to adsorbed water or hydrogenous species [75]. For the same reason (more charges/traps are able to respond to the varying AC small signal), capacitance increases as temperature increases (Figure 5.3.3(a and b)) [63]. The increase in relative permittivity (ε_r) at low electric fields (coercive field) with temperature for PZT below the Curie temperature has already been reported up to 85 °C [76]. Here, we extend this regime up to 225 °C, noting that ε_r starts to saturate as we get closer to T_C. Table 5.3.1 summarizes the anomalies in basic performance metrics of the flexible ferroelectric devices at maximum temperature, and constant tensile high pressure. The results show that the memory devices can still function properly when the maximum percentile change is a decrease in V_{c+} which means that when the devices operate at high temperatures, the required electric field to switch

the polarization decreases (lower power operation). Since circuit designers tolerate behavior variation within 10% of electronic components, these memories should be used for a specific operation temperature as in the wide range (25–225 °C), the change is less than 10%. Nevertheless, if the devices are designed for the high coercive switching fields at lower temperature, they would still function in the dynamic range up to higher temperatures as required switching fields is lower, and the requirement is satisfied. The caveat would be making sure that the read voltage does not switch the device causing erroneous readout, which is an optimization issue. The other most affected parameter is the 45% decrease in remnant polarization (from 14 to 7.5 μC/cm^2). Although this is a significant degradation; it should not affect the functionality. Actually, most of the reported functional polymer based flexible FeRAMs over the past five years fall within the 7-8 μC/cm^2 P_r range at room temperature [41,46,48,49,77-81]. Figure 5.3.3(c) depicts the reduction in memory window as a function of increased temperature. Figure 5.3.4 represents memory window extraction plots. The memory window is defined as the ratio of switching current (I_{sw}) and non-switching current (I_{nsw}). For the reported devices, peak switching and non-switching currents were 2 mA and 1 mA, respectively. For memory array operations, the resulting currents due to switching/non-switching is passed to a sense resistor, converted into a voltage level, and passed to a comparator circuitry to determine if the read state is a "0" or a "1" bit. Although the shrinkage in memory window is severe, still 20% higher switching currents at 225 °C can be distinguished with a sensitive sense circuitry. Based on the above results, memory window proves the limiting case for higher temperature operations because once the switching and non-

switching current are non-distinguishable to the sense circuitry, the memory device functionality fails.

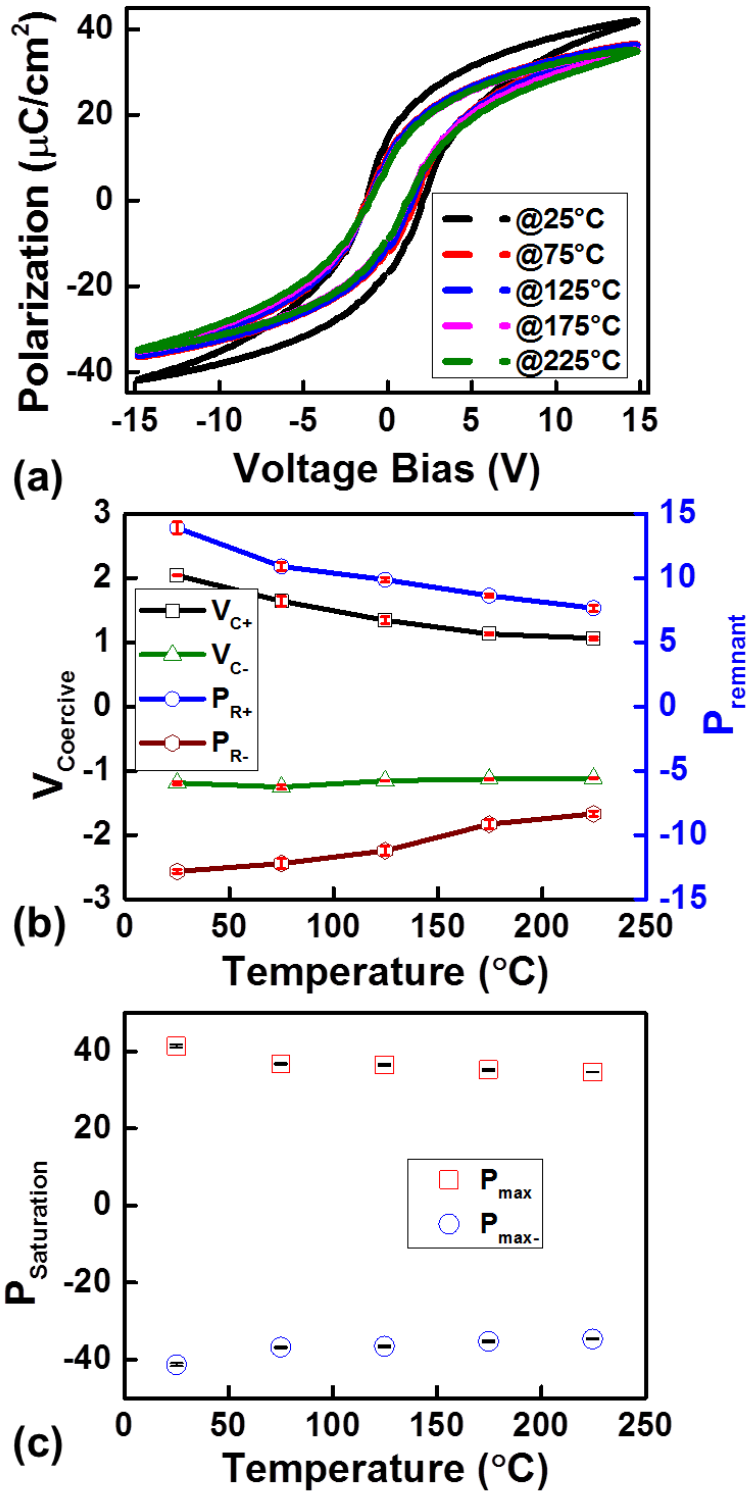


Figure 5.3.2: Polarization hysteresis plots vs. voltage bias (a), change in coercive voltage and remnant polarization (b), and decrease in saturation polarization (c) at wide range of temperatures.

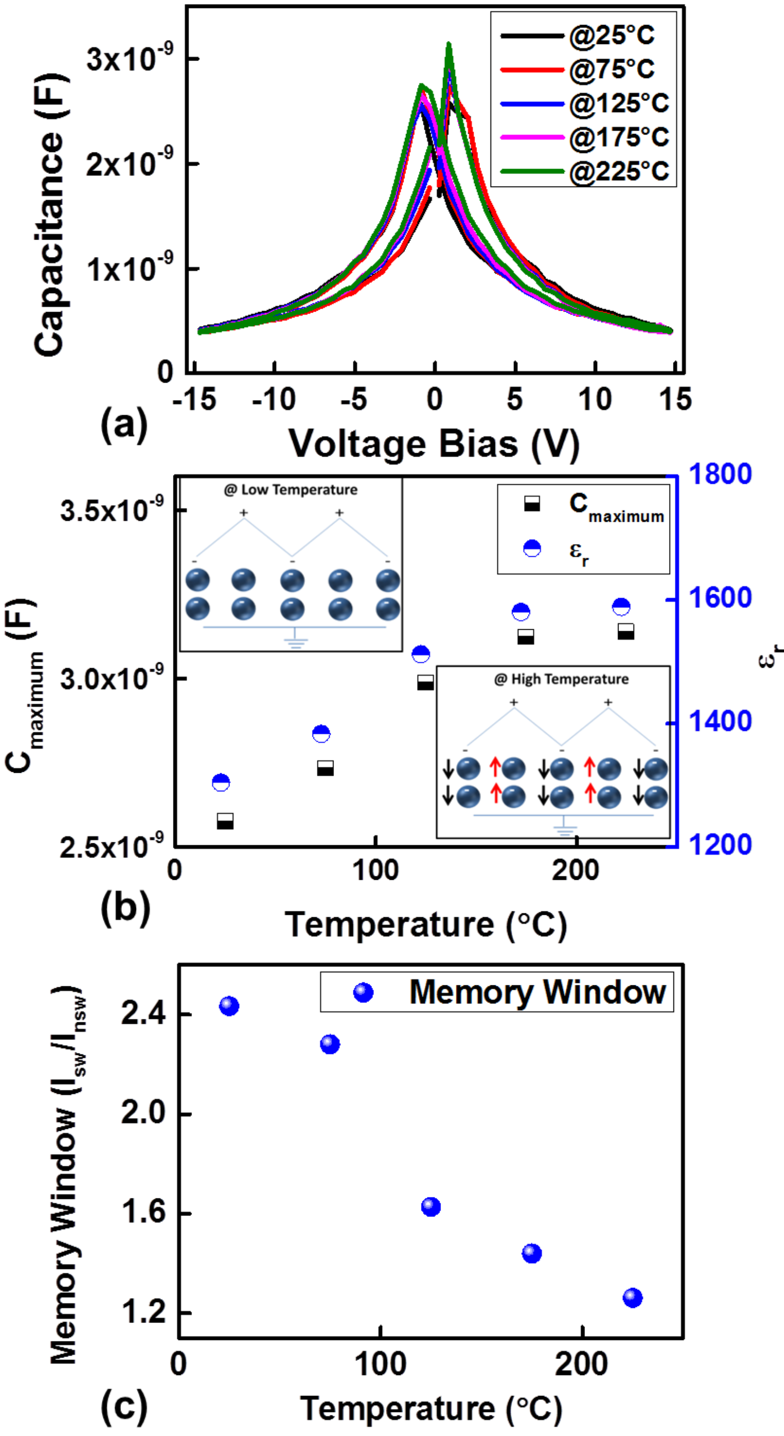


Figure 5.3.3: Capacitance–voltage plot (a), maximum capacitance and relative permittivity (b), and memory window plotted as a function of temperature (c).

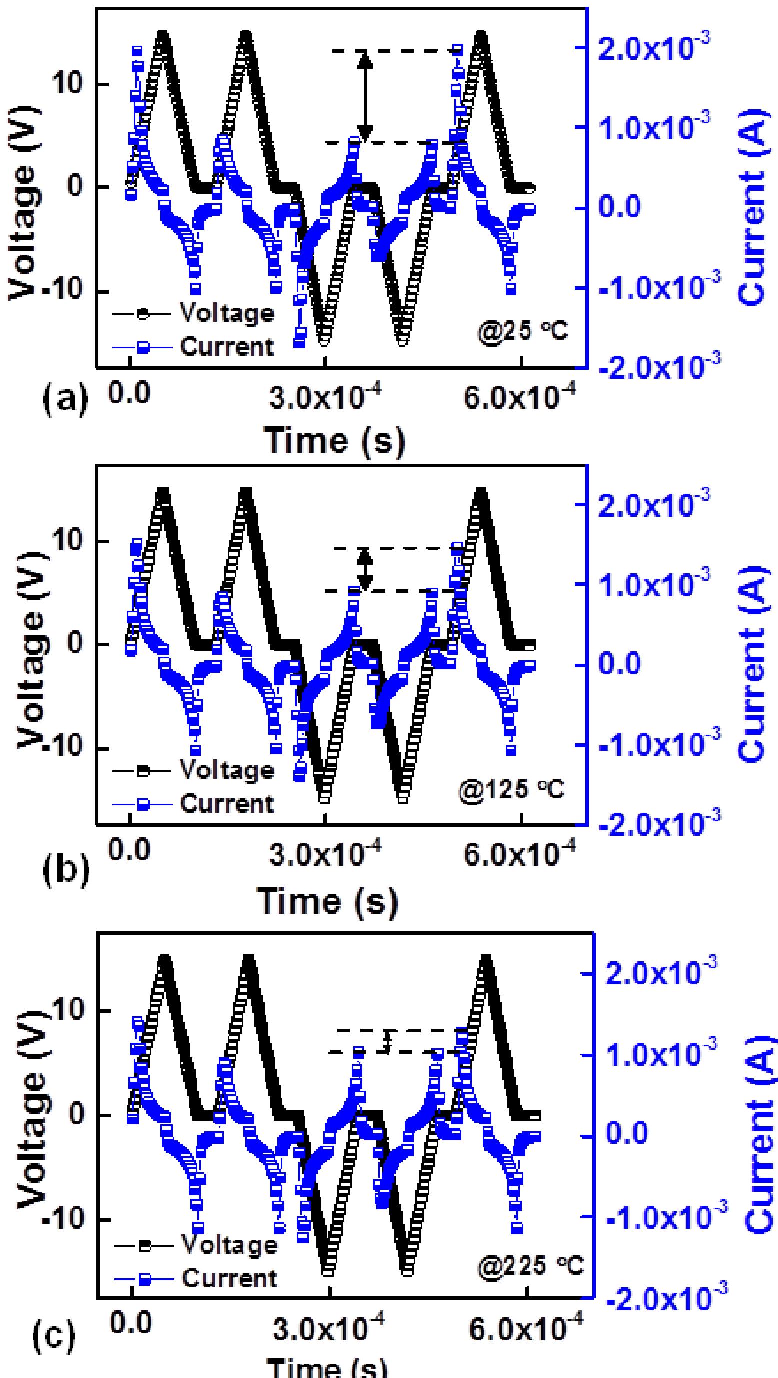


Figure 5.3.4: Memory window calculations from voltage–current *vs.* time plots at different temperatures (a-c).

Table 5.3.1: Percentage change in ferroelectric properties of PZT memory under harsh conditions

Performance Metric	*% Change at 225 °C and 260 MPa*
Remnant Polarization (P_{r+})	- 45
Remnant Polarization (P_{r-})	- 35
Coercive Voltage (V_{c+})	- 48
Coercive Voltage (V_{c-})	- 8
Saturation Polarization ($P_{max\ \pm}$)	- 15
Maximum Capacitance	22
Relative Permittivity	22

Figure 5.3.5(a) shows the data retention ability for the memory devices uncompromised at highest temperature. The retention ability indicates how long (without consuming power) the storage memory cell can retain the stored data (bit) accurately. Reported values for FeRAM and industry standard for non-volatile memories is 10 years. Retention measurement was executed by applying ±15 volts write/ read pulse, pulse duration is 50 μs and read frequnecy is 1 KHz. Another important memory property is fatigue. Fatigue measurements indicate how many switching cycles (read/write cycles) can a memory cell undertake before it fatigues. An acceptable indication of the functional number of cycles is when $P_{r+/-}$ values lose 50% of thier initial values. Figure 5.3.5(b) shows the fatigue behavior at 1 MHz disturbance signals (common operation frequency for commercially available FeRAM) of the bent memory devices at 25 °C and 225 °C indicating its ability to switch up to 10^9 cycles at elevated temperatures.

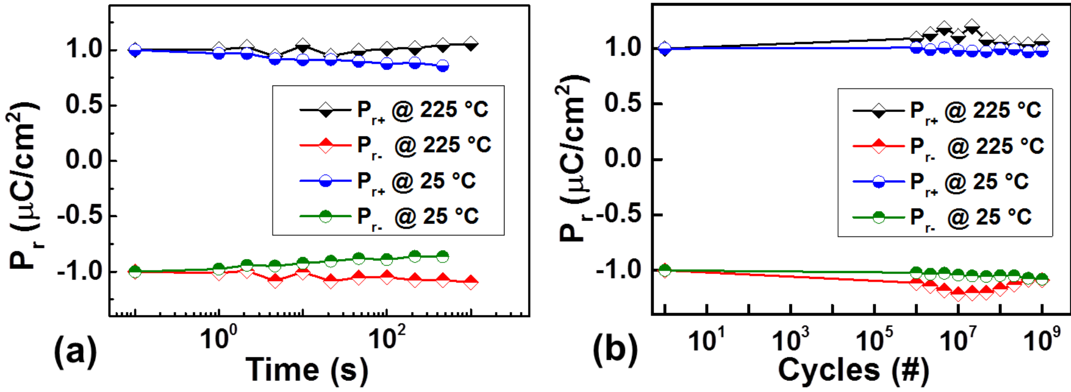


Figure 5.3.5: Retention (a) and fatigue (b) tests of flexible bent ferroelectric PZT memory at room temperature and 225 °C.

In addition to the flexible PZT memory's ability to retain more than 50% of its basic properties and an uncompromised fatigue and retention behavior under high-temperature and high-pressure conditions; PZT ferroelectric non-volatile memories are intrinsically radiation hard. It has been previously reported that PZT thin film non-volatile memory can with-stand up to 10^{15} neutron/cm^2 dose while retaining 90% of their initial switching charge [82]. Furthermore, PZT non-volatile memories are not the factor limiting hardness level in CMOS electronics but rather silicon [83]. Therefore, PZT based non-volatile memories have an intrinsic edge for applications inside nuclear reactors, inter and extra space missions, and nuclear warfare applications.

5.4. Conclusion

Ultra-thin version of the inorganic thin films can provide exciting flexibility while retaining the advantageous attributes inherent in the state-of-the-art electronics. From that perspective, we have shown a pragmatic CMOS based approach to transform thin PZT based FeRAM on silicon into a flexible FeRAM. Although many optimization opportunities exist the demonstrated device show exciting performance specially in

flexible state namely: (i) record polarization, capacitance, and endurance (1 billion write-erase cycles) values for flexible FeRAMs, (ii) uncompromised retention ability under varying dynamic stress, and (iii) a minimum bending radius of 5 mm. The combined effect of 225 °C, 260 MPa tensile stress due to bending at 1.25 cm radius, and 55% humidity under ambient conditions (21% oxygen), led to a maximum 48% reduction in switching coercive fields, 45% reduction in remnant polarization, and an expected increase of 22% in relative permittivity and normalized capacitance. Although the devices showed uncompromised data retention and fatigue properties under harsh conditions, the reduced memory window (20% difference between switching and non-switching currents at 225 °C) requires sensitive sense circuitry for proper functionality and is the limiting factor preventing operation at higher temperatures.

5.5. References

[1] Li, J.; Nagaraj, B.; Liang, H.; Cao, W.; Lee, C.H.; Ramesh, R. Ultrafast polarization switching in thin-film ferroelectrics. *Appl. Phys. Let.* 2004, 84, 1174-1176.

[2] Larsen, P.; Kampschoer, G.; van der Mark, M.; Klee, M. Ultrafast polarization switching of lead zirconate titanate thin films. In Applications of Ferroelectrics, 1992. ISAF'92., Proceedings of the Eighth IEEE International Symposium on 1992, 217-224.

[3] Patel, R.; Ipek, E.; Friedman, E.G. 2T–1R STT-MRAM memory cells for enhanced on/off current ratio. *Microelectron. J.* 2014, 45, 133-143.

[4] Li, J.; Zhao, Y.; Tan, H.S.; Guo, Y.; Di, C.-A.; Yu, G.; Liu, Y.; Lin, M.; Lim, S.H.; Zhou, Y. A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* 2012, 2, 754.

[5] Kang, I.; Yun, H.-J.; Chung, D.S.; Kwon, S.-K.; Kim, Y.-H. Record high hole mobility in polymer semiconductors via side-chain engineering. *Journal of the American Chemical Society* 2013, 135, 14896-14899.

[6] Caraveo-Frescas, J.; Khan, M.; Alshareef, H.N. Polymer ferroelectric field-effect memory device with SnO channel layer exhibits record hole mobility. *Sci. Rep.* 2014, 4.

[7] Mizuno, T.; Takagi, S.; Sugiyama, N.; Satake, H.; Kurobe, A.; Toriumi, A. Electron and hole mobility enhancement in strained-Si MOSFET's on SiGe-on-insulator

substrates fabricated by SIMOX technology. *IEEE Electron Device Letters* 2000, 21, 230-232.

[8] Shannigrahi, S.; Jang, H.M. Fatigue-free lead zirconate titanate-based capacitors for nonvolatile memories. *Appl. Phys. Lett.* 2001, 79, 1051-1053.

[9] Nagel, N.; Bruchhaus, R.; Hornik, K.; Egger, U.; Zhuang, H.; Joachim, H.-O.; Rohr, T.; Beitel, G.; Ozaki, T.; Kunishima, I. New highly scalable 3 dimensional chain FeRAM cell with vertical capacitor. In Digest of Technical Papers on VLSI Technology, 2004, 146-147.

[10] Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-based resistive switching memories–nanoionic mechanisms, prospects, and challenges. *Adv. Mater.* 2009, 21, 2632-2663.

[11] Derbenwick, G. F.; Kamp, D.A.; Philpy, S. C.; Isaacson, A. F. Celis Semiconductor Corporation 2000.

[12] Eshita, T.; Wang, W.; Nakamura, K.; Mihara, S.; Saito, H.; Hikosaka, Y.; Inoue, K.; Kawashima, S.; Yamaguchi, H.; Nomura, K. Int. Symp. Appl. Ferroelectr. Int. Symp. Piezoresponse Force Microsc. Nanoscale Phenom. Polar Mater. USA 2014.

[13] Evans, J. Embedding FeRAM, www.eetimes.com, accessed: Dec, 2014.

[14] Lee, S.Y.; Kim, H.H.; Jung, D.J.; Song, Y.J.; Jang, N.W.; Choi, M.K.; Jeori, B.K.; Lee, Y.T.; Lee, K.M.; Joo, S.H.; Park, S.O.; Kim, K. In Symp. VLSI Technol., Dig. Tech. Pap., USA 2001.

[15] Han, S.T.; Zhou, Y.; Roy, V. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* 2013, 25, 5425-5449.

[16] Khan, M.A.; Bhansali, U.S.; Almadhoun, M.N.; Odeh, I.N.; Cha, D.; Alshareef, H.N. High-Performance Ferroelectric Memory Based on Phase-Separated Films of Polymer Blends. *Adv. Funct. Mater.* 2014, 24, 1372-1381.

[17] Tseng, Y.-C.; Xuan, P.; Javey, A.; Malloy, R.; Wang, Q.; Bokor, J.; Dai, H. Monolithic integration of carbon nanotube devices with silicon MOS technology. *Nano Lett.* 2004, 4, 123-127.

[18] Torres Sevilla, G.A.; Ghoneim, M.T.; Fahad, H.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible nanoscale high-performance FinFETs. *ACS Nano* 2014, 8, 9850-9856.

[19] Ayguavives, F.; Agius, B.; EaKim, B.; Vickridge, I. Oxygen transport during annealing of Pb (Zr, Ti) O 3 thin films in O 2 gas and its effect on their conductivity. *J. Mater. Res.* 2001, 16, 3005-3008.

[20] Hidaka, O.; Ozaki, T.; Kanaya, H.; Kumura, Y.; Shimojo, Y.; Shuto, S.; Yamada, Y.; Yahashi, K.; Yamakawa, K.; Yamazaki, S. High Density and High Reliability Chain FeRAM with Damage-robust MOCVD-PZT Capacitor with SrRuO3/IrO2 Top Electrode for 64Mb and Beyond. 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers. 126-127.

[21] Rojas, J.P.; Ghoneim, M.T.; Young, C.D.; Hussain, M.M. Flexible High-/Metal Gate Metal/Insulator/Metal Capacitors on Silicon (100) Fabric. *IEEE Trans. Electron Devices* 2013, 60, 3305-3309.

[22] Ghoneim, M.T.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Additive advantage in characteristics of MIMCAPs on flexible silicon (100) fabric with release-first process. *Physica Status Solidi (RRL)-Rapid Res. Lett.* 2014, 8, 163-166.

[23] Rojas, J.P.; Hussain, M.M. Flexible semi-transparent silicon (100) fabric with high-k/metal gate devices. *physica status solidi (RRL)-Rapid Res. Lett.* 2013, 7, 187-191.

[24] Ghoneim, M.T.; Zidan, M.A.; Salama, K.N.; Hussain, M.M. Towards neuromorphic electronics: Memristors on foldable silicon fabric. *Microelectron. J.* 2014, 45, 1392-1395.

[25] Ghoneim, M.; Kutbee, A.; Nasseri, F.G.; Bersuker, G.; Hussain, M.M. Mechanical anomaly impact on metal-oxide-semiconductor capacitors on flexible silicon fabric. *Appl. Phys. Lett.* 2014, 104, 234104.

[26] Rojas, J.P.; Sevilla, G.T.; Hussain, M.M. Structural and electrical characteristics of high-k/metal gate metal oxide semiconductor capacitors fabricated on flexible, semi-transparent silicon (100) fabric. *Appl. Phys. Lett.* 2013, 102, 064102.

[27] Ghoneim, M.T.; Rojas, J.P.; Young, C.D.; Bersuker, G.; Hussain, M.M. Electrical Analysis of High Dielectric Constant Insulator and Metal Gate Metal Oxide Semiconductor Capacitors on Flexible Bulk Mono-Crystalline Silicon. *IEEE Trans. Rel.* 2015, 64, 579-585.

[28] Rojas, J.P.; Sevilla, G.A.T.; Hussain, M.M. Can we build a truly high performance computer which is flexible and transparent? *Sci. Rep.* 2013, 3.

[29] Sevilla, G.A.T.; Rojas, J.P.; Fahad, H.M.; Hussain, A.M.; Ghanem, R.; Smith, C.E.; Hussain, M.M. Field-Effect Transistors: Flexible and Transparent Silicon-on-Polymer Based Sub-20 nm Non-planar 3D FinFET for Brain-Architecture Inspired Computation (Adv. Mater. 18/2014). *Adv. Mater.* 2014, 26, 2765-2765.

[30] Sevilla, G.A.T.; Inayat, S.B.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible and Semi-Transparent Thermoelectric Energy Harvesters from Low Cost Bulk Silicon (100). *Small* 2013, 9, 3916-3921.

[31] Endo, A.; Kawashima, N.; Takeuchi, S.; Ishikawa, M.; Kurosawa, M. Modification of deposition process of piezoelectric polycrystalline film by hydrothermal method-Improvement of the deposition process by pre-treatment using hydrogen peroxide. *MRS Proc.* 2005, 872, J1-3.

[32] Tsuchiya, K.; Kitagawa, T.; Nakamachi, E. Development of RF magnetron sputtering method to fabricate PZT thin film actuator. *Precision Eng.* 2003, 27, 258-264.

[33] Shannigrahi, S.; Jang, H.M. Fatigue-free lead zirconate titanate-based capacitors for nonvolatile memories. *Appl. Phys. Lett.* 2001, 79, 1051-1053.

[34] Yoo, I.-K.; Desu, S. Mechanism of fatigue in ferroelectric thin films. *Physica Status Solidi (a)* 1992, 133, 565-573.

[35] Takashima, D. Overview of ferams: Trends and perspectives. *Non-Volatile Memory Technology Symposium (NVMTS), 2011 11th Annual*, 1-6.

[36] Pandey, S.; James, A.; Raman, R.; Chatterjee, S.; Goyal, A.; Prakash, C.; Goel, T. Structural, ferroelectric and optical properties of PZT thin films. *Physica B: Cond. Matt.* 2005, 369, 135-142.

[37] ITRS report 2013, emerging research memory devices-projected and demonstrated parameters.

[38] Zhu, H.; Chu, D.; Fleck, N.; Rowley, S.; Saxena, S. Polarization change in ferroelectric thin film capacitors under external stress. *J. Appl. Phys.* 2009, 105, 061609.

[39] Ng, T.N.; Russo, B.; Krusor, B.; Kist, R.; Arias, A.C. Organic inkjet-patterned memory array based on ferroelectric field-effect transistors. *Org. Electron.* 2011, 12, 2012-2018.

[40] Kerckhof, S.; Standaert, F.-X.; Peeters, E. Smart Card Research and Advanced Applications, Springer International Publishing 2014.

[41] Li, M.; Katsouras, I.; Asadi, K.; Blom, P.W.; de Leeuw, D.M. Low voltage extrinsic switching of ferroelectric δ-PVDF ultra-thin films. *Appl. Phys. Lett.* 2013, 103, 072903.

[42] Bhansali, U.S.; Khan, M.A.; Alshareef, H.N. Organic ferroelectric memory devices with inkjet-printed polymer electrodes on flexible substrates. *Microelectron. Eng.* 2013, 105, 68-73.

[43] Song, Y.; Shen, Y.; Liu, H.; Lin, Y.; Li, M.; Nan, C.-W. Enhanced dielectric and ferroelectric properties induced by dopamine-modified BaTiO 3 nanofibers in flexible poly (vinylidene fluoride-trifluoroethylene) nanocomposites. *J. Mater. Chem.* 2012, 22, 8063-8068.

[44] Kim, W.Y.; Lee, H.C. Stable ferroelectric poly (vinylidene fluoride-trifluoroethylene) film for flexible nonvolatile memory application. *IEEE Electron Device Lett.* 2012, 33, 260-262.

[45] Zuo, Z.; Chen, B.; Zhan, Q.-f.; Liu, Y.; Yang, H.; Li, Z.; Xu, G.; Li, R.-W. Preparation and ferroelectric properties of freestanding Pb (Zr, Ti) O3 thin membranes. *J. Phys. D: Appl. Phys.* 2012, 45, 185302.

[46] Khan, M.; Bhansali, U.S.; Zhang, X.; Saleh, M.M.; Odeh, I.; Alshareef, H.N. Doped polymer electrodes for high performance ferroelectric capacitors on plastic substrates. *Appl. Phys. Lett.* 2012, 101, 143303.

[47] Khan, M.A.; Bhansali, U.S.; Alshareef, H.N. Fabrication and characterization of all-polymer, transparent ferroelectric capacitors on flexible substrates. *Org. Electron.* 2011, 12, 2225-2229.

[48] Yoon, S.-M.; Jung, S.-W.; Yang, S.; Park, S.-H.K.; Yu, B.-G.; Ishiwara, H. Bending characteristics of ferroelectric poly (vinylidene fluoride trifluoroethylene) capacitors fabricated on flexible polyethylene naphthalate substrate. *Curr. Appl. Phys.* 2011, 11, S219-S224.

[49] Mao, D.; Mejia, I.; Stiegler, H.; Gnade, B.; Quevedo-Lopez, M. Polarization behavior of poly (vinylidene fluoride-trifluoroethylene) copolymer ferroelectric thin film capacitors for nonvolatile memory application in flexible electronics. *J. Appl. Phys.* 2010, 108, 094102.

[50] Mao, D.; Mejia, I.; Stiegler, H.; Gnade, B.; Quevedo-Lopez, M. Fatigue characteristics of poly (vinylidene fluoride-trifluoroethylene) copolymer ferroelectric thin film capacitors for flexible electronics memory applications. *Org. Electron.* 2011, 12, 1298-1303.

[51] Mao, D.; Quevedo-Lopez, M.; Stiegler, H.; Gnade, B.E.; Alshareef, H.N. Optimization of poly (vinylidene fluoride-trifluoroethylene) films as non-volatile memory for flexible electronics. *Org. Electron.* 2010, 11, 925-932.

[52] Shiga, H.; Takashima, D.; Shiratake, S.-i.; Hoya, K.; Miyakawa, T.; Ogiwara, R.; Fukuda, R.; Takizawa, R.; Hatsuda, K.; Matsuoka, F.; Nagadomi, Y.; Hashimoto, D.; Nishimura, H.; Hioka, T.; Dohmae, S. A 1.6GB/s DDR2 128Mb Chain FeRAM with Scalable Octal Bitline and Sensing Schemes. In Technical Report of IEICE. ICD 2009, 109, 1-6.

[53] Ansell, T.Y.; Cann, D.P.; Sapper, E.; Rödel, J. Thermal Depolarization in the High-Temperature Ternary Piezoelectric System Pb_xTiO_3–Bi_yScO_3–zBi (Ni1/2Ti1/2) O_3. *J. Am. Ceram. Soc.* 2015, 98, 455-463.

[54] Amalu, E.; Ekere, N.; Bhatti, R. In Int. Conf. Adap. Sc. Tech., Accra, Ghana, Jan. 2009, pp. 146-153.

[55] Ohadi, M.; Qi, J. Thermal management of harsh-environment electronics. In Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium, 2004. 231-240.

[56] Asadnia, M.; Kottapalli, A.; Miao, J.; Randles, A.; Sabbagh, A.; Kropelnicki, P.; Tsai, J. High temperature characterization of PZT (0.52/0.48) thin-film pressure sensors. *J. Micromech. Microeng.* 2013, 24, 015017.

[57] Chen, J.; Cheng, J.; Dong, S. Review on high temperature piezoelectric ceramics and actuators based on BiScO 3–PbTiO 3 solid solutions. *J. Adv. Dielect.* 2014, 4, 1430002.

[58] Fu, Y.; Fu, G.; Li, M.; Jia, D.; Jia, Y.; Liu, B. Investigation of Pt/Pb (Zr0. 2Ti0. 8) O3/Ti-Al-O/Si heterostructure as metal/ferroelectric/insulator/semiconductor. *Appl. Phys. Lett.* 2014, 104, 041903.

[59] Verma, R.M.; Rao, A.; Singh, B. Electrical characterization of the metal ferroelectric oxide semiconductor and metal ferroelectric nitride semiconductor gate stacks for ferroelectric field effect transistors. *Appl. Phys. Lett.* 2014, 104, 092907.

[60] Lim, Y.T.; Son, J.Y.; Shin, Y.-H. Domain switching of fatigued ferroelectric thin films. *Appl. Phys. Lett.* 2014, 104, 192902.

[61] Khan, A.I.; Yu, P.; Trassin, M.; Lee, M.J.; You, L.; Salahuddin, S. The effects of strain relaxation on the dielectric properties of epitaxial ferroelectric Pb ($Zr_{0.2}Ti_{0.8}$) TiO_3 thin films. *Appl. Phys. Lett.* 2014, 105, 022903.

[62] Lou, X.; Zhang, H.; Luo, Z.; Zhang, F.; Liu, Y.; Liu, Q.; Fang, A.; Dkhil, B.; Zhang, M.; Ren, X. Effect of polarization fatigue on the Rayleigh coefficients of ferroelectric lead zirconate titanate thin films: Experimental evidence and implications. *Appl. Phys. Lett.* 2014, 105, 102907.

[63] Pintilie, L.; Dragoi, C.; Radu, R.; Costinoaia, A.; Stancu, V.; Pintilie, I. Temperature induced change in the hysteretic behavior of the capacitance-voltage characteristics of Pt–ZnO–Pb ($Zr_{0.2}Ti_{0.8}$) O_3–Pt heterostructures. *Appl. Phys. Lett.* 2010, 96, 012903.

[64] Shkuratov, S.I.; Baird, J.; Antipov, V.G.; Talantsev, E.F.; Jo, H.R.; Valadez, J.C.; Lynch, C.S. Depolarization mechanisms of $PbZr_{0.52}Ti_{0.48}O_3$ and $PbZr_{0.95}Ti_{0.05}O_3$ poled ferroelectrics under high strain rate loading. *Appl. Phys. Lett.* 2014, 104, 212901.

[65] Stavinoha, S.; Chen, H.; Walker, M.; Zhang, B.; Fuhlbrigge, T. Challenges of robotics and automation in offshore oil&gas industry. IEEE 4th Ann.l Int. Conf. Cyber Tech. Autom Contr. Intel. Sys. (CYBER), 2014, 557-562.

[66] Lien, D.-H.; Kao, Z.-K.; Huang, T.-H.; Liao, Y.-C.; Lee, S.-C.; He, J.-H. All-printed paper memory. *ACS nano* 2014, 8, 7613-7619.

[67] Lien, D.-H.; Kuo, Z.-K.; Huang, T.-H.; Liao, Y.-C.; Lee, S.-C.; He, H. Paper memory by all printing technology. In 2014 Symp. VLSI Tech. (VLSI-Technology): Dig.Tech. Papers, 1-2.

[68] Baldwin, C. Optical fiber sensing in the oil and gas industry: overcoming challenges. In OFS2014 23rd International Conference on Optical Fiber Sensors 2014, 9157C9154-9157C9154-9154.

[69] Udrea, F.; Ali, S.Z.; Brezeanu, M.; Dumitru, V.; Buiu, O.; Poenaru, I.; Chowdhury, M.; De Luca, A.; Gardner, J. SOI sensing technologies for harsh environment. CAS 2012 (International Semiconductor Conference), 3-10.

[70] Patterson, R.L.; Hammoud, A.; Elbuluk, M. Electronic components for use in extreme temperature aerospace applications. 2008.

[71] Mehregany, M.; Zorman, C.A.; Rajan, N.; Wu, C.H. Silicon carbide MEMS for harsh environments. *IEEE Proc.* 1998, 86, 1594-1609.

[72] Torres Sevilla, G.A.; Ghoneim, M.T.; Fahad, H.; Rojas, J.P.; Hussain, A.M.; Hussain, M.M. Flexible nanoscale high-performance FinFETs. *ACS Nano* 2014, 8, 9850-9856.

[73] Inoue, N.; Hayashi, Y. Effect of imprint on operation and reliability of ferroelectric random access memory (FeRAM). *IEEE Trans. Electron Devices* 2001, 48, 2266-2272.

[74] Baniecki, J.; Cross, J.; Tsukada, M.; Watanabe, J. H2O vapor-induced leakage degradation of Pb (Zr, Ti) O_3 thin-film capacitors with Pt and IrO_2 electrodes. *Appl. Phys. Let.* 2002, 81, 3837-3839.

[75] Zhang, J.; Webster, J. Wiley encyclopedia of electrical and electronics engineering. John Wiley & Sons, Inc 1999.

[76] Wolf, R.; Trolier-McKinstry, S. Temperature dependence of the piezoelectric response in lead zirconate titanate films. *J. Appl. Phys.* 2004, 95, 1397-1406.

[77] Han, S.T.; Zhou, Y.; Roy, V. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* 2013, 25, 5425-5449.

[78] Bhansali, U.S.; Khan, M.A.; Alshareef, H.N. Organic ferroelectric memory devices with inkjet-printed polymer electrodes on flexible substrates. *Microelectron. Eng.* 2013, 105, 68-73.

[79] Song, Y.; Shen, Y.; Liu, H.; Lin, Y.; Li, M.; Nan, C.-W. Enhanced dielectric and ferroelectric properties induced by dopamine-modified $BaTiO_3$ nanofibers in flexible poly (vinylidene fluoride-trifluoroethylene) nanocomposites. *J. Mater. Chem.* 2012, 22, 8063-8068.

[80] Hwang, S.K.; Min, S.Y.; Bae, I.; Cho, S.M.; Kim, K.L.; Lee, T.W.; Park, C. Non-Volatile Ferroelectric Memory with Position-Addressable Polymer Semiconducting Nanowire. *Small* 2014, 10, 1976-1984.

[81] Reeder, J.; Kaltenbrunner, M.; Ware, T.; Arreaga-Salas, D.; Avendano-Bolivar, A.; Yokota, T.; Inoue, Y.; Sekino, M.; Voit, W.; Sekitani, T. Mechanically adaptive organic transistors for implantable electronics. *Adv. Mater.* 2014, 26, 4967-4973.

[82] Moore, R.; Benedetto, J.; McGarrity, J.; McLean, F. Neutron irradiation effects on PZT thin films for nonvolatile-memory applications. *IEEE Trans. Nucl. Sci.* 1991, 38, 1078-1082.

[83] Coic, Y.; Musseau, O.; Leray, J. A study of radiation vulnerability of ferroelectric material and devices. *IEEE Trans. Nucl. Sci.* 1994, 41, 495-502.

Chapter 6 Conclusion

6.1. Status Quo

The presented work demonstrated the potential of transforming traditional high performance nonvolatile memory devices into flexible form. The necessary elements for building memory arrays have been separately demonstrated and their reliability has been assessed. The major findings can be summarized in:

- Flexible devices fabricated using etch-protect-release approach (with trenches included in the active area) exhibit ~19% lower safe operating voltage compared to their bulk counterparts. This is attributed to the added interfacial defects due to the altering of the active area. This can be mitigated by designing the release holes network such that it overlaps unused space and/or scaling the devices' active areas.
- Flexible silicon devices can withstand prolonged bending duration (static stress) but are prone to failure under dynamic stress as in repeated bending and re-flattening. This suggests they are more suitable for applications where the curvature does not change as in wrapping around an arm wrist or a finger than around a body or mechanical joint.
- Flexible 3D FinFETs exhibit ~10% variation in key properties when exposed to out-of-plane bending stress. Circuit techniques already exist to comply with similar variability due to different component tolerances and process variations. Hence, circuit designers can include the extra variation into consideration to embrace the effect of bending.

- Out-of-plane stress does not resemble the well-studied in-plane stress used in strain engineering, in terms of both absolute values and stress distribution. This consequently leads to different effects that depend on carrier type, crystal orientation, and type of the stress.
- Resistive memories can be achieved on flexible silicon and their basic resistive property is preserved. Nonetheless, deeper analysis and assessment of key memory properties is required for a conclusive result.
- Flexible silicon based PZT ferroelectric capacitors exhibit record polarization, capacitance, and endurance (1 billion write-erase cycles) values for flexible FeRAMs, uncompromised retention ability under varying dynamic stress, and a minimum bending radius of 5 mm. This makes flexible PZT capacitors on silicon a feasible candidate for high performance flexible nonvolatile memories.
- Flexible PZT ferroelectric capacitors can withstand harsh environments required for oil industry and space application (due to the excellent radiation hardness of PZT). Exhibiting the combined effect of 225 °C, 260 MPa tensile stress, 55% humidity under ambient conditions (21% oxygen), leads to 48% reduction in switching coercive fields, 45% reduction in remnant polarization, an increase of 22% in relative permittivity and normalized capacitance, and reduced memory window (20% difference between switching and non-switching currents at 225 °C). This sets the limits for operation temperature in harsh environments as a shrinking memory window requires a more sensitive circuit for correct readout and increases the chances of erroneous readings which can be fatal in sensitive applications.

6.2. Future Directions

Demonstrating the essential elements functionality is the first step towards a fully flexible NVM module. The next step is using the collective knowledge from these experiments and results and putting the elements together in an actual memory array. This can be a straightforward step or other key issues can come into play such as the parasitic capacitances of bit/word/plate lines and the variation of resistance and how it might affect the overall functionality of the array. Our group is currently investigating these issues by transforming a commercial grade FeRAM into flexible form and monitoring its read/write ability.

We believe that FeRAM would be a suitable candidate for flexible NVM because of its superior endurance compared to flash memories, good retention, fast read/write, and low operation voltage as the technology is already mature. On the other hand, memristors are still in the infancy phase and there are critical issues related to variability, forming, and reliability that are being investigated.

3D FinFETs and high-κ gate stacks have pushed the limits of scaling and adopting them in flexible electronics should add the flexibility feature without interrupting the scaling trends. Overall, adopting the CMOS technology and silicon as a flexible substrates provides an alternative direction of preserving the state-of-the-art electronic devices properties while adding the flexibility feature, given the limitations on bending radius which implies that polymer based electronics and silicon based flexible electronics can complement each other as each can serve a niche. Flexible silicon electronics are more suitable when performance is valued over flexibility and polymer based electronics

are more suitable when flexibility is valued over performance. This can also open an opportunity for hybrid integration of various modules to achieve optimal systems which can make use of the Lego concept for connecting and assembling various electronic modules at the package and the die level [1].

Another common issue with all flexible electronics, especially memory modules because of the high integration densities, is heat dissipation and thermal management. The portable nature of new electronics requires them to be light weight, flexible, and reasonably sized. Therefore, using the traditional bulky heat sinks to increase the surface area is no longer an option. This limits the available surface area for heat dissipation and thus allowable the power of the circuits. Moreover, there is no longer a dedicated fan for forced convection to push the hot air and increase the cooling efficiency; now, it is still air. Finally, the most stringent requirement is for wearable electronics where although the electronics can function at higher temperatures reliably, the human skin cannot with stand the temperature comfortably. This limits the maximum temperature to around 37 °C. All these suggest that thermal management will require lots of innovative technologies and solutions to overcome the imposed limitations so that we can still enjoy the functionalities we enjoy in today’s bulky electronics but in wearable and flexible forms.

To this end, we have briefly studied the effect on thermal cooling for the flexible silicon substrate versus traditional bulk [2]. The next step would be manipulating the release holes and testing their dimensions and aspect ratios to render them effective in exposing more area for free convection. Also innovative techniques such as micro fabricated heat sinks that have high surface to volume ratio for light weight and small size while exposing more area for heat dissipation are worth investigating [3]. Evidently,

the future of flexible electronics is still green and as scientists and researchers keep pushing the limits new applications and directions will unfold for further pursuits for the overall benefit of improving the quality of our lives.

Useful Applications Based on the Reported Results

Although flexible electronics is still in the developmental stages; few commercial products already hit the market. For instance, in 2013 LG and Samsung introduced organic light emitting diode (OLED) based flexible television displays. Nonetheless, the real vision for flexible electronics is still futuristic where real full systems such as computing devices (ex: mobiles, electronic tablets, and computers), can be made flexible and lightweight to the extent that one can roll them/wear them conveniently.

Other startups, such as the UK based FlexEnable, are already utilizing the organic transistors technology and advertising flexible smart phones, X-ray detectors, and flexible fingerprint sensors. The applications range from roll-able mobile phones to door handles that can detect who is opening the door for security purposes.

Storage devices and transistors are at the heart of all electronic systems to store and process data and generate useful information. Therefore, researching how these specific devices behave with flexing and bending pushes forward flexible electronic systems technologies collectively. Current approaches include building flexible thin film transistors (TFTs) using organic/oxides/amorphous silicon channel materials that are fabricated at low temperatures on an organic flexible substrate. The motilities reported for these devices are at least an order of magnitude lower than that of traditional monocrystalline silicon. This means any electronic device capitalizing on these TFTs will

be ten times slower than the traditional devices we enjoy today. Still, adding the excellent flexibility feature of these materials is a great advantage and an important step forward.

In this thesis, we have demonstrated the potential of our pragmatic approach for building flexible versions of state-of-the-art storage devices and high-performance transistors (high- κ FinFETs that are commercially used in today's Intel's higher technology nodes microprocessors). The conclusions drawn demonstrate the potential of the approach and provide effective guidelines for system designers to utilize today's high performance electronics in flexible form as a new library cell among other flexible electronics technology alternatives. One example to demonstrate the need for flexible high-performance devices is in automotive applications where autonomous cars are not a far-fetched goal anymore. For autonomous driving to happen, enormous amounts of data need to be stored and processed in a reliable fast manner related to road conditions, traffic analysis, navigation routes, and avoiding fatal accidents that can happen in a split of a second. To realize this scenario we need today's bulky rigid but high performance reliable electronics. This would impose extra requirements in terms of space and location of the electronic system modules which is already tight for the inside of a traditional automobile with limited interior space and all the curved stylish structures designed for comfort and safety. On the other hand, the conformal flexible organic electronics solve the area challenge as they can fit on the inside curved structures but their reliability and performance pose a more serious challenge. Fortunately, an alternative route exists midway based on the demonstrated studies in this work. That is transforming today's electronic to gain the flexibility feature given special care is given to account for the reported anomalies and trends with bending. This way, we can reap the benefits of high-

performance and reliable operation while adding acceptable flexibility. Indeed, the alternative routes will also have their niche applications where acceptable reliability and performance are required along with excellent flexibility, such as in flexible displays.

Furthermore, there is the emerging IoT vision where trillions of sensors and devices will be connected and communicating with the cloud for information storage and computing, exchanging and analyzing “big data.” This big data would require gigantic storage capacities. Hence, being able to conform to curved surface on our bodies, plants or nonliving structures would be essential to sense/monitor and store information for later transmission and exchange with the cloud. Data transmission is an energy intensive process due to the power requirements for amplification; hence, the less frequent the better, especially for IoT devices which would be battery operated. This adds a bigger storage capacity requirement so store information over longer time durations until the next transmission interval. Integration density and monolithic integration are two perks of today’s silicon based non-volatile memories (for example: flash drives are commercially available in tens of GBs in the area of a finger nail), which is not the case with organic materials based chips and devices. This is an example of another niche application where capitalizing on flexed version of today’s high integration density and suited for monolithic integration inorganic memories on silicon, as demonstrated and studied herein, would be advantageous.

6.3. References

[1] Ghoneim, M. T.; Hussain, M. M. Lego Silicon Dies for Pre-packaging Integration. Patent Pending (In Process).

[2] Ghoneim, M.T.; Fahad, H.M.; Hussain, A.M.; Rojas, J.P.; Sevilla, G.A.T.; Alfaraj, N.; Lizardo, E.B.; Hussain, M.M. Enhanced cooling in mono-crystalline ultra-thin silicon by embedded micro-air channels. *AIP Adv.* 2015, 5, 127115.

[3] Ghoneim, M. T.; Hussain, M. M. Microfabrication Techniques for Thermal Management of IoT Devices. Patent Pending (In Process).

[4] FlexEnable. “Enabling transformational products using flexible electronics.” Accessed: 15/11/2016 <http://www.flexenable.com/applications/>