Electrical characterization of process and irradiation-induced defects in GaAs

by

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Declaration of Authorship

I, Shandirai Malven Tunhuma, declare that this dissertation, which i hereby submit for the degree Magister Scientiae is my original work and has not been submitted by me for any degree at this or another institution.

Signed: _____

Date: _____

"Only the best is good enough."

Munyaradzi

Abstract

Electrical characterization of process and irradiation induced defects in GaAs

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Supervisor: Prof. Mmantsae Diale

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Gallium arsenide (GaAs) technology leads the implementation of high frequency devices with superior performance. A vast number of optoelectronic applications are based on the material owing to its direct and wide bandgap. Over the years the number of these applications continues to grow but they remain highly cost-ineffective partly due to the growth techniques and the presence of defects in GaAs. These areas have been researched on intensively over the past four decades with much controversy, particularly on the subject of the EL2 defect. This defect plays an important role in the design and operation of GaAs based devices. It is therefore important to understand its electronic properties and influence on device operation.

Schottky barrier diodes (SBDs) were fabricated on *n*-type GaAs. The quality of the contacts was evaluated using current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements before and after exposing them to different processing techniques and radiation types. Deep-level transient spectroscopy (DLTS) and Laplace deep-level transient spectroscopy (L-DLTS) were used to characterize the electrically active defects in the material. Defects with almost similar emission rates which were not observed in the past were identified using L-DLTS due to its high resolution.

I-V and *C-V* measurements on as-deposited Au/*n*-GaAs SBDs in the $80 - 480$ K range showed that the EL2 defect has a profound effect on the diode characteristics. The influence of the defect caused the temperature dependent behavior of the *C-V* barrier height to be split into two temperature intervals, each with a unique temperature coefficient. Exposure of the devices to temperatures above

300 K resulted in the deterioration of their *I-V* characteristics. Permanent physical modification of the SBDs was observed at 400 K and above.

Inductively coupled plasma (ICP) etching, Electron beam deposition (EBD) and electron beam exposure (EBE) were observed to impact significantly on diode *I-V* and *C-V* characteristics. ICP etching resulted in devices with a lower reverse leakage current and high barrier height whereas EBD fabricated devices exhibited the poorest characteristics. DLTS results revealed that processing introduced electrically active defects in the bandgap. EBE induced defects had different electronic properties to all the processing and radiation induced defects observed in previous studies.

I-V and *C-V* characteristics of SBDs exposed to alpha and beta-particle irradiation were identical to as-deposited samples. This demonstrated the radiation hardness of GaAs. DLTS spectra of alpha-particle irradiated SBDs displayed the defect peaks sitting on a skewed baseline which hampered accurate L-DLTS measurements. In addition to the prominent irradiation induced defects, high energy electron-irradiation was observed to induce defects with electronic properties similar to those of the EL2.

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Abbreviations

SBD	Schottky barrier diode
DLTS	Deep-level transient spectroscopy
L-DLTS	Laplace-transform deep-level transient spectroscopy
EBD	Electron beam deposition
DLTS	Deep-level transient spectroscopy
L-DLTS	Laplace-transform deep-level transient spectroscopy
EBE	Electron beam exposure
ICP	Inductively coupled plasma
MBE	Molecular beam epitaxy
MOCVD	Metal organic chemical vapour phase
LED	Light emitting diode
YAG	Yttrium-aluminum garnett
MIGS	Metal-induced gap states
UDF	Unified defect model
DIGS	Disorder-induced gap states
EWF	Effective work function
RE	Resistive evaporation
MS	Metal semiconductor
RF	Radio frequency
HDPE	High density plasma etching
MOVPE	Metalorganic vapor phase epitaxy

Physical Constants

Boltzmann constant	k	$=$	$1.380\,658 \times 10^{-23}$ JK^{-1}
Elementary charge	e	$=$	$1.602\,177 \times 10^{-19}$ C
Electron rest mass	m_e^*	$=$	$9.109\,390 \times 10^{-31}$ kg
Electron-volt	eV	$=$	$1.602\,177 \times 10^{-19}$ J
Vacuum permittivity	ϵ_0	$=$	$8.854\,188\,58 \times 10^{-14}$ F cm^{-1}
Planck's constant	h	$=$	$6.626\,076 \times 10^{-34}$ Js

Symbols

α	Temperature coefficient
I-V	Current-voltage
I-V-T	Current-voltage-temperature
C-V	Capacitance-voltage
C-V-T	Capacitance-voltage-temperature
a.c.	Alternating current
d.c.	Direct current
ϕ_{Bn}	Schottky barrier height
ϵ_s	Permittivity of a semiconductor
ϕ_{IV}	*I-V* barrier height
ϕ_{CV}	*C-V* barrier height
$\rho(x)$	Charge density of a semiconductor
$\phi(x)$	Electrostatic potential
$e\phi_m$	Metal work function
$e\chi$	Electronic affinity of a semiconductor

For my parents

Chapter 1

Introduction

Gallium arsenide forms the basis for the high frequency and high speed electronics industry (Baca and Ashby, 2005). The discovery of the transistor by Bardeen and Brattain in 1948 saw the material being considered for development of electronic devices. It was not until 1970 that it entered the commercial market. Today its market share is relatively small compared to elemental semiconductors such as silicon and germanium but its importance lies in the applications it enables. The crucial properties of GaAs are high electron mobility, light emission and availability of diverse bandgap engineering approaches. Currently, most of the satellite power in space is provided by solar cells made on the semiconductor owing to its superior radiation hardness (Fraas and Partain, 2010).

As the demand for faster and miniature devices continues to grow, GaAs finds itself as a suitable candidate for newer co-integrated technologies which have multiple applications. The contrast of GaAs to other semiconductors is, the difficulty in growing and purifying it. Defects are almost always present (Seebauer and Kratzer, 2008). These defects can be advantageous or detrimental to the operation of devices. An understanding of the impact of defects on device properties is essential for successful design and fabrication. Space charge spectroscopy studies give insight on their most relevant properties. These characterization techniques continue to improve with time in speed and resolution. Defect studies of GaAs using modern methods are particularly important because most of them where conducted in the past using analogue and rudimentary methods.

1.1 Motivation

A summary of the native, radiation and process induced defects that occur in GaAs is given by Simoen et al. (2015). This is a compilation of the results that have been produced in past studies. The subject of defects in GaAs has been studied extensively in the past. However deep-level transient spectroscopy (DLTS) was being performed as introduced by Lang in 1974 on analogue platforms. Over the years DLTS has been improved to give resolutions that are higher by up to an order of magnitude. Laplace transform DLTS (L-DLTS) has revolutionized the space charge spectroscopy of defects in semiconductors (Emiroglu et al., 2008). It is clear that the current literature on defects in GaAs needs an overhaul.

The identity of the native EL2 defect in GaAs is arguably the most exasperating problem in the history of semiconductor physics (Kaminska and Weber, 1993). This defect is always present in material grown at a sufficiently high rate. Several studies have been carried out resulting in different models being developed for its chemical and/or microscopic structure without conclusive viewpoints. Every device design has to account for the detrimental effects of the defect. This situation has negative implications on the cost-effective production of GaAs devices. A complete understanding of this defect's structure and mechanisms of its metastability will undoubtedly lead to significant advancement of the microelectronics industry.

Metalization is an important step in the fabrication of semiconductor devices. The mechanisms of defect formation during contact fabrication have also been studied with different viewpoints arising. Nel and Auret studied these defects in 1988 using conventional DLTS in *n*-GaAs. Since then, there has been significant progress on the subject giving interesting results with the most recent being discrete breathers or vibrational nodes in germanium (Archilla et al., 2015). It is necessary to establish if this phenomenon can be observed in GaAs.

1.2 Aim

The aim of this study was to use Laplace transform deep-level transient spectroscopy to study the fine structure of defects introduced in *n*- GaAs during device fabrication processes and by particle irradiation from radionuclide sources. The main focus was on how the electronic properties of the EL2 defect were affected.

1.3 Objectives

- To produce high quality Schottky barrier diodes (SBD) with high barrier heights, low series resistance and low reverse leakage current.
- To determine the effect of the EL2 defect on the current-voltage*(I-V)* and capacitance-voltage *(C-V)* characteristics of GaAs devices.
- Characterization of defects introduced by radionuclides and processing in GaAs.
- Determination of the effects of several processes on the electronic properties of the EL2 defect so as to gain insight on its microscopic structure.
- To study the fundamentals of energy transfer during defect formation by introducing defects using sub-threshold energies.

1.4 Layout of the dissertation

- **Chapter 2** covers the theoretical aspects of metal semiconductor(MS) contacts. The theory summarizes deviation of real devices from ideal models.
- **Chapter 3** discusses the theoretical aspects of defects in semiconductors. Special consideration is given to the electronic properties of defects and the DLTS and L-DLTS methods.
- **Chapter 4** explains the experimental techniques that were applied during fabrication and characterization of devices. The instrumentation used is also described in detail.
- **Chapter 5** is a presentation and discussion of results obtained.
- **Chapter 6** concludes the study and describes the future work arising.

1.5 Gallium arsenide

Figure 1.1 shows the zincblende cubic structure of GaAs after Martienssen and Warlimont (2006). It consists of polar layers of gallium(Ga) and arsenic(As) which

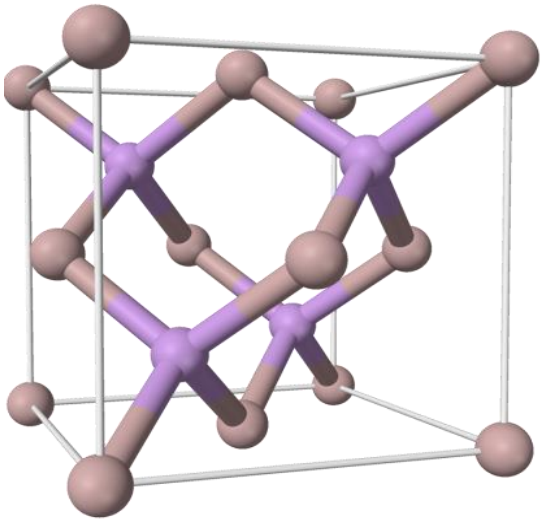


Figure 1.1: Model of a cubic unit cell of GaAs showing the zincblende crystal structure. The brown spheres represent gallium and the purple spheres represent arsenic.

are covalently bonded. Each Ga atom bonds with 4 As atoms forming a 4 co-ordinate tetrahedron with a lattice constant of 5.67 Å (Seebauer and Kratzer, 2008). The structure has two inter-penetrating face centered cubic sub-lattices separated by 2.44 Å along the body diagonal (Blakemore, 1982). Group four elements are intentionally introduced at Ga sites where they act as dopants and the material becomes *n*-type.

Bulk crystal growth is done using either Czokralski or Bridgman methods. The desirable properties of a substrate are minimal dislocations, a relatively high resistivity and uniformity (Shur, 2013). Resistivity is particularly important because it lowers substrate capacitance allowing high frequency operation of GaAs based devices (Naber, 1995). For this reason, impurities or defects have been intentionally introduced to obtain near-ideal resistivity. The EL2 defect has been deliberately employed for these purposes (Supiski et al., 1993). The structure of the defect has been a subject of debate for many years but it is widely believed to be associated with the As antisite (Boudinov et al., 2003). This is despite that the first recorded junction capacitance measurement in the history of mankind was done on the same defect (Williams, 1966).

Besides improving resistivity the defect can also be intentionally introduced during growth by adjusting stoichiometry to compensate for carbon impurities (Grovenor,

1989). However, it also has detrimental effects on devices as it traps electrons that are accelerated into semi-insulating regions creating fixed charge regions (Baca and Ashby, 2005). Thus, it is taken into consideration in all GaAs device designs.

Epitaxy is the growth of crystalline semiconductor films on crystalline substrates for a device of interest (Ramesh, 2013). High purity thin layers can be grown using molecular beam epitaxy (MBE) or metal organic chemical vapor phase deposition (MOCVD). MBE is an atomic-specific, ultra-high vacuum (UHV) technique which involves interactions of thermally sublimated material with a heated substrate surface (Henini, 2012). The atoms or molecules condense at the surface and may react with each other. The end product is a new crystalline layer at a precisely controlled composition, thickness and morphology. MOCVD involves pyrolysis of gas phase metalorganics and hydrides over heated semiconductor substrates in a reactor. The gases are introduced at high pressure. The end products are deposited and bond with the substrate surface forming crystalline layers (Ramesh, 2013).

1.5.1 Properties and applications

The table below shows some of the physical properties of GaAs.

Table 1.1: Physical properties of GaAs (Naber, 1995).

Bandgap (eV)	1.43
Electron mobility (cm^2/Vs)	5000
Hole mobility (cm^2/Vs)	250
Thermal conductivity ($W/cm^2/°C$)	0.5

GaAs has a direct bandgap which permits light emission at a high efficiency as well as fast electron conduction (Fox, 2001). The high electron mobility makes it ideally suited for the fabrication of high frequency and low power devices (Chang and Kai, 1994). A wider bandgap allows the material to be used for high temperature applications.

Several electronic and photonic devices have been implemented on GaAs to date with light emitting diodes (LEDs) being the largest application. The electronic devices include heterojunction bipolar transistors(HBTs), field effect transistors(FETs) and diodes whereas the photonic devices include light emitting diodes(LEDs), laser diodes (LDs) and photo-detectors. A substantial number of applications

have benefited from GaAs structures. These include radiation hard electronics, space solar cells, computer networking and microwave diode technologies. The following is a list of some significant contributions:

- GaAs based LEDs have notably revolutionized lighting by improving reliability, cost and efficiencies (Schubert, 2006).
- In fibre-optic communications, GaAs edge emitting laser repeaters have significantly improved the cost and capacity to decode the signal over long distances (Baker, 2012).
- In cellular phone technology GaAs is very competitive in meeting cell phone power amplifier technical requirements and at infrastructure level (Tateoka et al., 1995).
- Incorporation of GaAs in yttrium aluminum garnett (YAG) lasers has seen them becoming smaller, reliable and increase in power output making them more convenient for cosmetic surgery (Ahluwalia, 2008).
- GaAs edge emitting lasers have been used to produce cost effective compact disc (CD) and digital versatile discs (DVD) players which record at ultra high speeds (Uchida et al., 2006).
- Gunn diode oscillators made from GaAs can operate at ultra high frequencies of up to 200 GHz. They are used in aviation for collision prevention radar and for adaptive cruise control in automobiles (Forster et al., 2007).

Chapter 2

Metal semiconductor contacts

2.1 Introduction

Metal semiconductor (MS) contacts are classified based on their rectifying properties. Rectifying contacts are referred to as Schottky contacts and non-rectifying contacts are referred to as ohmic contacts. These junctions are very important tools in the field of semiconductor physics as they allow for the electrical characterization of most semiconductor properties. This chapter explains the theory of formation and properties of Schottky barrier diodes (SBDs) made on *n*-type semiconductor material both under ideal and non-ideal conditions. Electrical characterization done on GaAs was through MS contacts. In addition ohmic contacts are also discussed in brief as they are also an important constituent of the SBD.

2.2 Schottky Barrier diodes

2.2.1 Ideal band structure

An ideal energy-band diagram for a particular metal and *n*-type semiconductor before making contact is shown in Figure 2.1a. In isolation, the metal and the semiconductor have generally different Fermi level positions (E_F) relative to the vacuum level (Grundmann, 2006). The metal is characterized by its work function $e\phi_m$ and the semiconductor is characterized by its electron affinity $e\chi$ (Sze and Kwong, 2006). The case depicted is when the metal work function $(e\phi)$ is greater than the semiconductor work function $e(\phi_n + \chi)$, where e is the electronic charge.

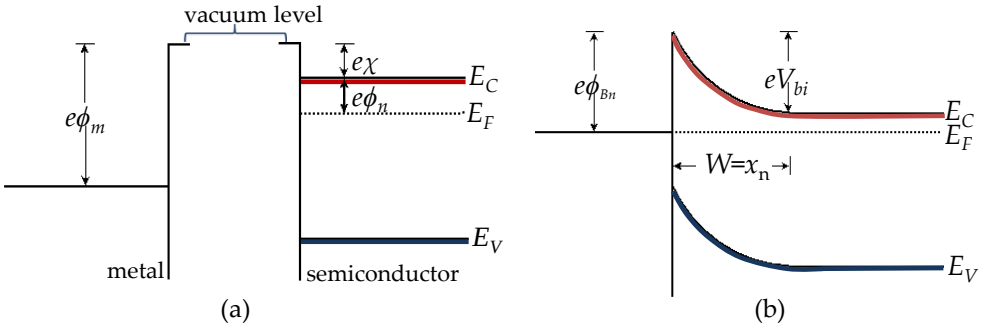


Figure 2.1: a) Energy band diagram for a metal and semiconductor before contact b) Ideal energy-band diagram of an MS junction between a metal and an n-type semiconductor (Neamen, 2010).

E_V and E_C are the top of the valence band and the bottom of the conduction band respectively.

If the metal and the semiconductor are brought into intimate thermodynamic contact as shown in Figure 2.1b, electrons will flow from the semiconductor into the metal's lower energy states, in-order to attain thermal equilibrium as a single system. In the process Fermi levels align resulting in energy bands bending (Neamen, 2010). Across the MS interface bending sets a barrier to current flow. Positively charged donor atoms corresponding to the zone depleted of electrons remain in the semiconductor, with a charge that is equal and opposite in magnitude to that accumulating at the metal surface. These positively charged atoms form a space charge region .

The potential barrier seen by electrons in the metal trying to move into the semiconductor is known as the barrier height (ϕ_{Bn}) (Singh and Singh, 2009). It can be defined as the difference between the metal work function and the electron affinity of the semiconductor (Chang and Kai, 1994).

$$\phi_{Bn} = \phi_m - \chi \tag{2.1}$$

On the semiconductor side V_{bi} is a built in potential barrier. It is the barrier seen by electrons in the conduction band trying to move into the metal (Li, 2012). It represents the depletion region without an applied external bias and is given by

$$V_{bi} = \phi_{Bn} - \phi_n \tag{2.2}$$

2.2.2 Forward and reverse bias

Current flow at room temperature is mainly due to the flow of majority carrier electrons possessing sufficient energy to overcome the barrier. Electron flow in the semiconductor to metal direction corresponds to a positive current flow from the metal into the semiconductor. Without any external bias at thermodynamic equilibrium, current flow in both directions is balanced (Chang and Kai, 1994).

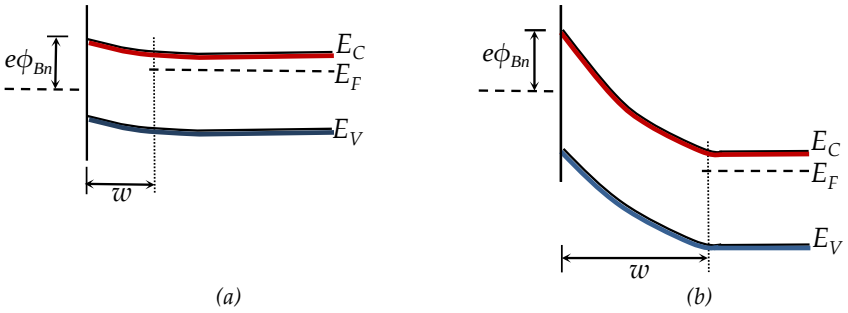


Figure 2.2: Ideal energy band diagram of a MS junction (a) under forward bias (b) under reverse bias.

If a positive voltage is applied to the semiconductor with respect to the metal, the semiconductor's Fermi level is raised in energy relative to that of the metal. The depletion width (w) is collapsed. Electrons have to overcome a lower potential barrier on the semiconductor side. In this situation a greater number of electrons can easily flow into the metal, which leads to a larger current due to majority charge carriers. In the other direction electron flow from the metal to the semiconductor remains constant. This condition is known as forward bias (Streetman and Banerjee, 2014).

If a negative voltage is applied to the semiconductor with respect to the metal, the Fermi level is lowered in energy relative to that of the metal. The depletion width (w) is increased. Electrons have to overcome a larger potential barrier on the semiconductor side. In this situation a small reverse current of electrons flowing from the metal to the semiconductor is observed. This condition is known as the reverse bias. Asymmetry between the forward and reverse current flow mechanisms creates non-linear voltage characteristics (Colinge and Colinge, 2005).

2.2.3 Ideal junction properties

In the formation of the Schottky barrier, the semiconductor's conduction and valence bands at the surface are brought into a definite energy relationship with the Fermi energy in the metal (Mönch, 2013). This relationship serves as a boundary condition to the solution of Poisson's equation in the semiconductor. In the one dimensional case, the electric field in the space charge region is determined from Poisson's equation

$$\frac{dE}{dx} = \frac{\rho(x)}{\epsilon_s} \tag{2.3}$$

where $\rho(x)$ is the charge density in the semiconductor and ϵ_s is the permittivity of the semiconductor. Using the depletion width approximation i.e. assuming that it is possible to divide the semiconductor into two regions namely:

I The depletion region, directly below the metal, which is devoid of free carriers

II The bulk of the semiconductor, which is electrically neutral, uniform in doping density (N_D) and in which no electric field exists.

$$\rho(x) = \begin{cases} eN_D, & \text{if } x \leq x_n. \\ 0, & \text{if } x \geq x_n. \end{cases} \tag{2.4}$$

where $w = x_n$ (Figure 2.1b.) is the width of the depletion region. Integrating equation 2.3 twice and applying the boundary conditions we obtain the electric field as

$$E = -\frac{eN_D}{\epsilon_s}(x_n - x) \tag{2.5}$$

Which is a linear function of the distance x. The depletion width may be calculated for a uniformly doped semiconductor as

$$w = x_n = -\frac{eN_D}{\epsilon_s}(x_n - x) \tag{2.6}$$

at a reverse bias V_R (Neamen, 2010).

2.3 Non ideal effects on the barrier height

A MS contact formed between gallium arsenide and any other material will always have a band gap of around 0.8 V (Grundmann, 2006). Myburg et al. (1998) using 43 different metals on *n*-GaAs showed that there is no linear relationship between the Schottky barrier height and the metal work function. This experimental evidence shows that barrier height is less sensitive to metal work function than postulated in Section 2.2.1 (Rhoderick and Williams, 1988). The Schottky barrier height is altered from its theoretical value by other factors including electric field, and the presence of surface or defect states (Brennan, 1999). An equivalent circuit of a real SBD is shown below

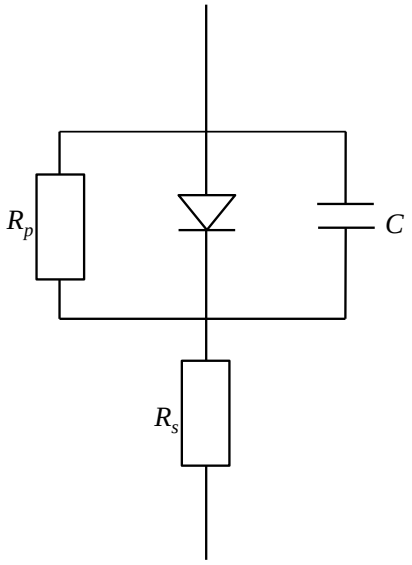


Figure 2.3: Sketch depicting an equivalent circuit of a real Schottky diode showing the series resistance (R_s) and parallel resistance (Rp).

A model of a real Schottky diode takes account of the following

a) An insulating interfacial layer of atomic dimensions exists between the metal and the semiconductor. The layer can withstand a potential difference but will be transparent to the flow of electrons between the metal and semiconductor.

b) The interface states per unit area per energy at the interface are a property of the semiconductor surface and are independent of the metal.

c) A distribution of surface states exists at the MS interface, with the assumption that all states below the surface potential are of donor type, and all states above it are of acceptor type (Sze and Kwong, 2006).

2.3.1 Nature of the metal semiconductor interface

The quality of a Schottky contact is notably determined by the quality of the interface between the deposited metal and the semiconductor surface (Hudait and Krupanidhi, 2001; Diale and Auret, 2009). In GaAs-based devices, performance has been experimentally shown to be affected to a greater extent by surface and interface defect density (Ozavc et al., 2013). According to Tung (2014) it can also be explained in the chemical bonding picture, where diode characteristics depend on the atomic structure of the MS interface. Atomic structure of the interface is controlled by nature of the bonds broken or formed during device fabrication. The cleaning procedure used prior to Schottky metalization is therefore very important in determining the nature of the MS interface and the quality of the devices. This cleaning must remove organic and ion metal surface contaminants. Experimentally, such a clean surface is achieved by employing an organic solvent cleaning protocol followed by etching to remove oxide layers. A detailed description of the cleaning procedure for GaAs is given in Section 4.2.1

2.3.2 Image force lowering

It is the image charge induced lowering of the barrier energy for charge carrier emission in the presence of an electric field (Sze and Kwong, 2006). As carriers approach the MS interface from the semiconductor, at a distance x, mirror charges of an opposite polarity are induced in the metal. As a consequence an electric field is created with field lines perpendicular to the surface. The electrostatic force of attraction between the two image charges, a distance x apart, towards the metal is given by

$$F = -eE = \frac{-e^2}{4\pi\epsilon_s(2x^2)} \tag{2.7}$$

The force (F) in Equation (2.7) is known as the image force. The corresponding potential which is work done by the field on the electron to transfer it from infinity is

$$F = -\phi(x) = \int_x^\infty E\,dx = \int_x^\infty \frac{e}{4\pi\epsilon_s(4x'^2)}\,dx' = \frac{-e}{16\pi\epsilon_s(x)} \tag{2.8}$$

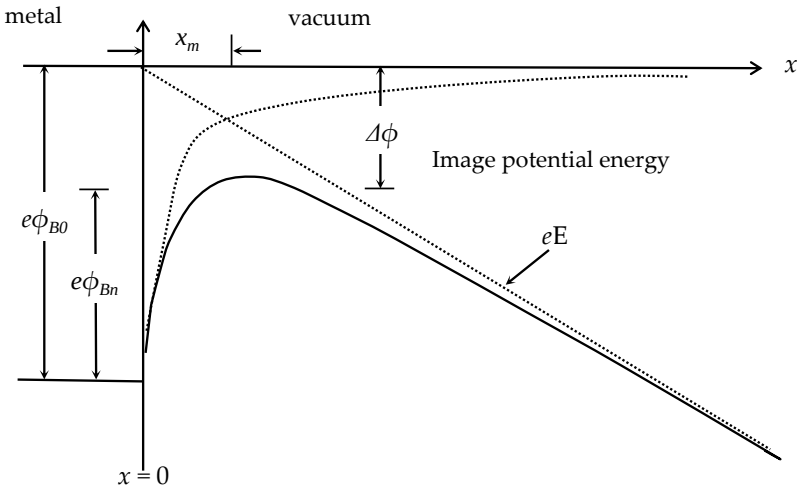


Figure 2.4: Metal-dielectric interface showing distortion of the potential barrier due to image forces with a constant electric field.

where x' is the integration variable. If this potential is combined with variation of potential due to the constant electric field the potential energy is found as

$$-\phi(x) = \frac{-e}{16\pi\epsilon_s x} E_x \tag{2.9}$$

The variation of potential energy of the electron, assuming constant electric field is plotted in Figure 2.4. The peak potential barrier is now lowered. This lowering of the potential barrier is the image force lowering also known as the Schottky effect. Potential energy reaches a maximum at

$$x_{max} = \sqrt{\frac{e}{16\pi\epsilon_s E}} \tag{2.10}$$

(Baliga, 2010). The Schottky barrier height change due to image force lowering is given by

$$\phi_{Bn} = \phi_{B0} - \Delta\phi \tag{2.11}$$

2.3.3 Surface states

The symmetry at the surface of a semiconductor material is different from that of the bulk. Edge termination of the periodic structure, introduces incomplete covalent bonds at the surface leading to a change of electronic band structure from the

bulk material to the vacuum (Rhoderick and Williams, 1988). Consequently surface electronic states known as Tamm Schockley states are created. These surface states result in electron energy levels within the bandgap (Bardeen, 1947). They can be wave functions that have surface peaks at, or resonant states that have enhanced amplitudes at the surface, but are coupled to bulk states (Tung, 2001).

2.3.4 Fermi level pinning

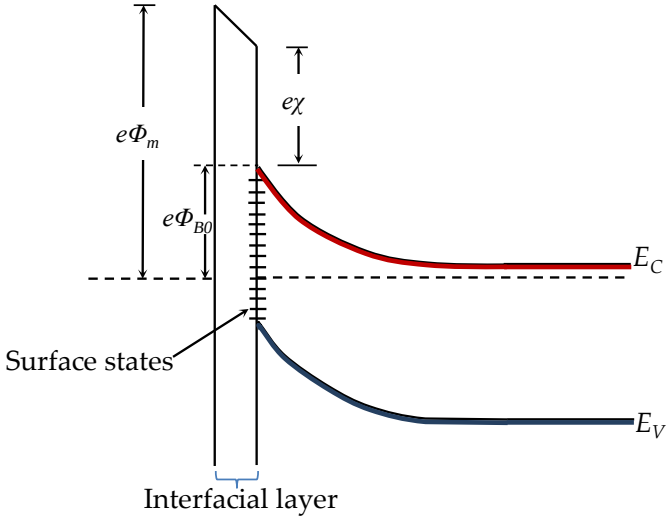


Figure 2.5: Energy band diagram of a metal-semiconductor junction showing surface states and an interfacial layer.

Mid-gap states at the surface or near the interface affect the Fermi level position relative to the valence band maximum and conduction band minimum. When a metal is brought into intimate contact with the semiconductor during barrier formation, thermal equilibrium has to be established resulting in band bending (Section 2.2.1). In the presence of surface states, electrons from the valence band of the semiconductor will be trapped by these vacant states. This occurs until the Fermi level coincides with the level to which the surface states are filled. Such a situation is known as Fermi level pinning.

A number of models have been developed to explain the origins of Fermi level pinning and its effects on the Schottky barrier height. The proposed origin of the pinning states varies with the model employed.

- The metal induced gap states (MIGS) model proposes that mid-gap states originating from the penetrating of the metal wave functions into the semiconductor are responsible for pinning (Tersoff, 1984).
- The unified defect model (UDF) ascribes pinning to defect states related to stoichiometric variation especially the arsenic antisites in GaAs (Bardeen, 1947).
- In the disorder-induced gap state (DIGS) model, the pinning states are a result of the loss of two dimensional periodicity due to disorder of the bonding interface (Hasegawa et al., 1987).
- In the effective work function (EWF) model pinning occurs at metallic clusters formed by metallurgic reactions at the interface (Freeouf and Woodall, 1981).

2.4 Current transport mechanisms

Majority carriers are responsible for carrier transport across the junction. Current transport can occur through different mechanisms as shown in Figure 2.6. Thermionic emission is the emission of electrons from the semiconductor over the Schottky barrier into the metal. On heavily doped semiconductors at low temperatures, tunneling of carriers at energies lower than the full barrier height can lead to current that exceeds thermally activated transport over the barrier. The effect of tunneling is to reduce the Schottky barrier for thermionic emitted carriers by an amount which depends on the form of the energy barrier and the temperature. When tunneling combines with partial thermal activation the mechanism is known as thermionic field emission (TFE), it occurs when the temperature is very low. Field emission is when the tunneling current is very low, and electron energy is close to the Fermi level.

Generation and recombination of carriers also occurs within the space charge region normally via localized states at low temperatures. There is also current transport due to holes injected from the metal that diffuse into the semiconductor (equivalent to recombination in the neutral region). Furthermore there is a probability of having edge leakage current due to a high field in the proximity of the metal-contact or interface current due to defects at the MS interface. For low mobility semiconductors, the theory of diffusion of electrons in the depletion region becomes significant.

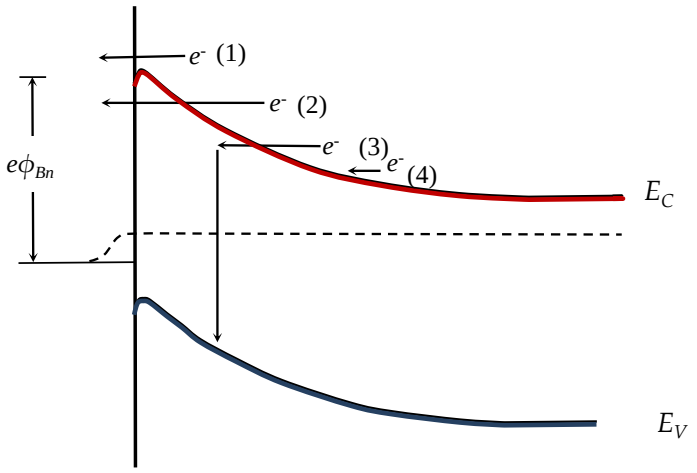


Figure 2.6: Current transport mechanisms across a forward biases Schottky barrier diode (1) Thermionic emission (2) Tunnelling (3) Recombination (4) Diffusion of electrons.

The carrier density of the material used for the work reported in this dissertation was relatively low. Gallium arsenide is a high mobility semiconductor. We can therefore sufficiently describe the current transport as due to the thermionic emission mechanism (Sze and Kwong, 2006).

2.4.1 Thermionic emission theory

Assumptions of the thermionic emission theory

i) The barrier height is larger than kT

ii) Thermal equilibrium is established at the plane that determines emission

iii) Thermal equilibrium is not disturbed by net current flow (Sze and Kwong, 2006).

Two current fluxes can be superimposed, one from the metal to the semiconductor and the other from the semiconductor to metal each with a different quasi-Fermi level. Current flow from the semiconductor to the metal is solely dependent on the barrier height.

In the nomenclature used from here onwards, the subscripts of the current density (J) indicate the direction of electron flow. J_{sm} is the electron current density due to

the flow of electrons from the semiconductor into the metal over the barrier. The conventional current direction is opposite to electron flow. The current density J_{sm} is a function of the concentration of electrons which have x directed velocities sufficient to overcome the barrier.

$$J_{sm} = e \int_{E_c'}^{\infty} v_x \, dn \tag{2.12}$$

where E_C' is the minimum energy required to overcome the barrier, v_x is the carrier velocity in the direction of electron transport, and e is the magnitude of the electronic charge. The incremental electron density is given by

$$dn = g_c(E) f_f(E) d(E) \tag{2.13}$$

Where $g_c(E)$ is the density of states in the conduction band and $f_f(E)$ is the Fermi-Dirac probability function. Assuming that the Maxwell-Boltzmann approximation applies, it may written that

$$dn = \frac{4\pi(2m_e^*)^{3/2}}{h^3} \sqrt{E - E_c} \exp\left[\frac{-(E - E_F)}{kT}\right] dE \tag{2.14}$$

If all the electron energy is postulated to be kinetic and the minimum x-directed velocity required to overcome the barrier is considered. Integration gives

$$J_{sm} = \left(\frac{4\pi e m_e^* n k^2}{h^3}\right) T^2 \exp\left[\frac{-e(\phi_n + V_{bi}}{kT}\right] \exp\left(\frac{eV_a}{kT}\right) \tag{2.15}$$

$$J_{ms} = \left(\frac{4\pi e m_e^* e k^2}{h^3}\right) T^2 \exp\left[\frac{-e\phi_{Bn}}{kT}\right] \tag{2.16}$$

where V_a is the applied bias. The net current density is a sum of the current density in both directions and can be written as

$$J = J_{sm} - J_{ms} \tag{2.17}$$

which is defined to be positive in the direction from the metal to the semiconductor. We find that

$$J = \left[A^* T^2 \exp\left(\frac{-e\phi_{Bn}}{kT}\right)\right] \left[\exp\left(\frac{eV_a}{kT}\right) - 1\right] \tag{2.18}$$

where

$$A^* = \left(\frac{4\pi e m_e^* k^2}{h^3}\right) \tag{2.19}$$

The parameter A* is called the effective Richardson constant for thermionic emission (Sharma et al., 2011). Equation 2.18 can be written in usual diode form as

$$J = J_{ST}[A^*T^2\left(\frac{eV_a}{kT}\right) - 1] \tag{2.20}$$

where J_{ST} is the reverse saturation current density and is given by

$$J_{ST} = [A^*T^2\left(\frac{-e\phi_{Bn}}{kT}\right) - 1] \tag{2.21}$$

From Equation 2.11 the change in Schottky barrier height due to image force lowering can be in-cooperated (Neamen, 2010). Equation 2.21 can therefore be written as

$$J_{ST} = A^*T^2\left(\frac{-e\phi_{B0}}{kT}\right)\exp\left(\frac{e\Delta\phi}{kT}\right) \tag{2.22}$$

2.4.2 Current-voltage relationship

The current-transport in a MS junction is due mainly to majority carriers. As already described in Section 2.4, the current transport can be adequately described by thermionic emission theory because it is the principal current transport mechanism. For pure thermionic emission, the relationship between the current I and the applied bias voltage V in the forward direction assuming that $V > 3kT/e$ is given by:

$$I = AA^*T^2\exp(-\frac{e\phi_0}{kT})\left[\exp\left(\frac{e(V - IR_s)}{nkT}\right) - 1\right] \tag{2.23}$$

where e is the electronic charge, k the Boltzmann constant, T the absolute temperature, R_s the series resistance, $\phi_0 = \phi_{IV}$ the zero-bias barrier height, A the diode area and A*$(= 8.16Acm^{-2}K^{-2})$ is the Richardson's constant (Karatas and Altndal, 2005a). The prefactor of the second exponential in Equation 2.23 gives the reverse saturation leakage current, I_S. The ideality factor n is given by

$$n = \frac{e}{kT}\left(\frac{dV}{d(\ln I)}\right) \tag{2.24}$$

where $0 \leq n \leq 1$ is a measure of the adherence to pure thermionic emission and it reflects barrier deformation under bias (Mayimele et al., 2015). The zero bias barrier height, (ϕ_0) is obtained from (I_S):

$$\phi_0 = \frac{kT}{e} \ln \frac{AA^*T^2}{I_s} \tag{2.25}$$

Reverse leakage current refers to the maximum current that flows through the junction at zero bias (Crofton and Sriram, 1996). Its value is obtained as the intercept of the current axis when $V = 0$.

2.4.3 Capacitance voltage relationship

The SBD is a majority carrier device implying that there is no diffusion capacitance associated with it under forward bias. When switching the bias condition of a Schottky diode there is no minority carrier stored charge to remove. This eliminates minority carrier storage time enabling the SBDs to be used in fast switching applications. According to the Schottky-Mott theory, depletion layer capacitance can be expressed as

$$C^{-2} = \frac{2(V_{bi} - V_A)}{e\epsilon_S A^2 N_D} \tag{2.26}$$

where, A is the diode area, V_{bi} the diffusion potential at zero bias obtained from the extrapolation of linear C^2-V plots to the V axis; and V_A is the applied voltage (Diale and Auret, 2009). The capacitance of a Schottky diode is characterized by the width of the depletion layer (Sharma et al., 2011). Diffusion potential (V_{bi}) is given by the intercept on the voltage axis and is used to determine the barrier height (Mtangi et al., 2009)

$$\phi_{cv} = V_{bi} + V_0 \tag{2.27}$$

V_0 is the potential difference between the conduction band minima and the Fermi level in the neutral part of the semiconductor (Karatas and Altndal, 2005b):

$$V_0 = kT \ln \left(\frac{N_C}{N_D} \right) \tag{2.28}$$

In Equation 2.28, N_C is density of states in the conduction band and N_D the doping density obtained from the gradient of C^2-V plots.

2.4.4 Temperature dependence of *n*-GaAs diode characteristics

According to the Fermi level pinning model discussed earlier in Section 2.3.4, metal induced gap states or defect states at the interface can pin the Fermi level (Bardeen, 1947; Tersoff and Harrison, 1987). In the case that the Fermi level is pinned by MIGS, the temperature dependence of the barrier height is governed by the band gap. On the other hand should the Fermi level be pinned by defect states the temperature dependence of the barrier height would be governed by the ionization entropy. The dependence of Schottky barrier height on temperature can be used to account for the physical mechanism responsible for Fermi level pinning at the MS interface.

Several studies have revealed a strong dependence of *n*-GaAs diode characteristics on temperature (Hudait and Krupanidhi, 2001; Ozavc et al., 2013; Korucu et al., 2013; Mamor et al., 2014). Kim et al. (2007) studied the temperature dependence of Au*n*-GaAs *I-V* characteristics using a semi analytical model in the $83 - 323$ K temperature range. They reported that the variations in the diode characteristics with temperature were consistent with those of the energy band gap. Halil et al. (2014) explained the temperature dependence of the *I-V* and *C-V* characteristics at high temperatures $280 - 415$ K using a Gaussian distribution of the Schottky barrier height.

The dependency on temperature of diode *I-V* characteristics has also been accounted for as due to local non-uniformities of the Schottky barrier. At high temperatures, there are possible inhomogeneities in the interface layer thickness and non-uniformities of the interfacial charges (Tung, 1992). Other researchers have attributed the variation with temperature to changes in carrier transport mechanisms which are recombination-generation in the space charge region and tunneling in the barrier (Tung, 2001; Sharma et al., 2011; Janardhanam et al., 2012).

Figure 2.7 shows the expected *I-V* characteristics depending on the current transport mechanisms. In some cases flattening of *I-V* curves can also be attributed to series resistance.

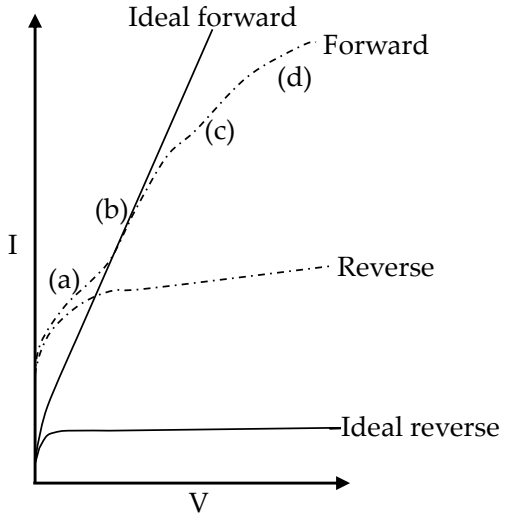


Figure 2.7: Typical *I-V* characteristics of a Schottky barrier diode showing regions of (a) generation-recombination (b) thermionic emission (c) hole injection (d) reverse leakage current.

Experimental results show a behavior of both the *(I-V)* and *C-V* barrier heights that is contrary to the theoretically expected negative temperature coefficient for *n*-GaAs (Ozavc et al., 2013; Mamor et al., 2014). Analysis of *I-V* characteristics reveals an abnormal decrease in the barrier height with decreasing temperature leading to non-linearity in the activation energy versus kT plot.

C^2-*V* plots are straight lines in the most cases and ϕ_{CV} decreases with increasing temperature. This variation has been explained using the potential fluctuations model as due to barrier height in-homogeneities (Werner and Guttler, 1991). The behavior of the *C-V* barrier height can be described using an equation of the form

$$\phi_{(T1-T2)} = \phi(T = 0) + \alpha T \tag{2.29}$$

where α is the temperature coefficient in the temperature range $T1 - T2$ (Mtangi et al., 2009).

Generally ϕ_{CV} is observed to be higher than ϕ_{IV} in all cases at the same temperature. Werner and Guttler (1991) ascertained that spatial variations in the barriers cause current to flow preferentially through band minima causing *I-V* barrier height to be lower. The disparity has also been attributed to the existence of excess capacitance (Halil et al., 2014).

2.5 Ohmic contacts

An ohmic contact is a low resistance junction providing conduction in both directions between the metal and the semiconductor (Crofton et al., 1997). It follows Ohm's law implying that a low barrier to current conduction exists at the MS interface and its purpose is to let current into and out of any semiconductor device. In general, the key to making an ohmic contact is to design low enough barriers to allow current across the interface by thermionic emission or narrow enough barriers to allow current across the interface by field emission (Rhoderick and Williams, 1988).

The principal current transport mechanism for ohmic contacts to GaAs is tunneling. If a semiconductor has a net doping density of 1.0×10^{20} cm^{-3} then in practice, a Schottky contact behaves as an ohmic contact (Schroder, 2006). Thus the two most important aspects for ohmic contact design in GaAs are a thickness closer to the depletion width or a high enough carrier density of the n^+ substrate to encourage tunneling. This has been achieved in some cases by heteroepitaxy of highly doped intermediate layers by MBE (Murakami, 2002).

Desirable properties for ohmic contacts are low contact resistance, thermal stability and high edge acuity (Wang, 2008). The contact should be such that no potential exists between the metal and the semiconductor (Ghosh, 2008). In-order to reduce resistivity and the unintentional barrier of ohmic contacts, it is essential to anneal them at sufficiently high temperatures in a forming gas (Kim et al., 2007). The Au-NiGe is the most prefered ohmic contact to GaAs because it is highly reproducible (Shih et al., 1987)

Specific contact resistance can be expressed as

$$R_C = \left(\frac{\partial J}{\partial V} \right)^{-1}_{V=0} \tag{2.30}$$

and is defined as resistance of the contact at zero bias (Mayer and Lau, 1990).

Chapter 3

Defects in semiconductors

3.1 Introduction

Semiconductors are technologically important because their electrical conductivity can be modified by the addition of low concentrations of impurity atoms. Substitutional impurities introduce donor and acceptor states in the bandgap close to the bottom of the conduction band and to the top of the valence band. Structural defects also introduce levels in the bandgap that are in most cases farther from the band edges. This chapter examines the different types of defects found in semiconductors and their classifications. A simplified mathematical description of the theoretical basis for deep-level transient spectroscopy (DLTS) is also given. DLTS is the main measurement technique which was used to electrically characterize defects in this study.

3.2 Classification of defects

Lattice defects are classified according to dimensions:

- Zero-dimensional defects affect isolated lattice sites in the crystal structure and are called point defects (Hull and Bacon, 2011). Only single atoms are considered. A detailed description of them is given in section 3.3
- One dimensional defects are called dislocations. They are lines along which the crystal pattern is discontinued. These can be either edge or screw dislocations (Kane et al., 1970).

- Two dimensional defects are surfaces along which distinct crystallites are joined together. They are called planar defects and can also include stacking faults and twins (Rockett, 2007).
- Three dimensional defects are any volumes in the semiconductor that differ in composition, structure or orientation to the rest of the crystal (Yacobi, 2003). These include precipitates which are small volumes of different crystal structure and voids or inclusions of second phase particles.

3.3 Point defects

According to Bourgoin and Lannoo (1983), a point defect is a modification in the crystal matrix with an extension in the order of the lattice constant which results in a deviation from lattice periodicity. The defects can be formed under the following circumstances.

- when an atom is missing from a position that ought to be filled in the crystal, a vacancy is created (Yu, 2007)
- when an atom occupies an interstitial site where no atom would ordinarily appear, an interstitial is created (Watkins, 2000).

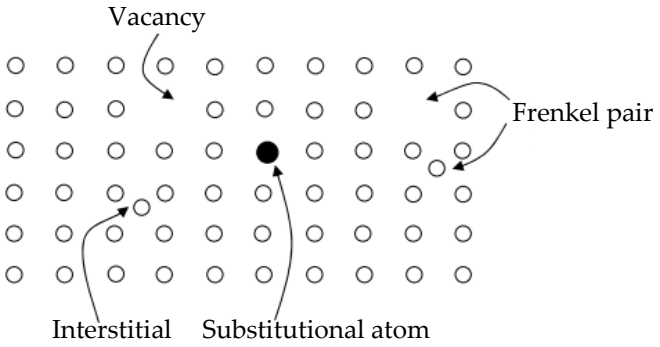


Figure 3.1: An illustration of a vacancy, interstitial, substitutional atom and Frenkel pair.

Vacancies and interstitials are collectively known as intrinsic defects. Interstitial sites in most crystalline solids are small and high energy defects owing to their

unfavorable bonding configuration. Vacancies are present in significant concentrations in all crystalline materials and they govern solid state diffusion (Krause-Rehberg and Leipner, 1999).

Ordered compounds can have more complex intrinsic defects.

- A Schottky defect involves paired vacancies on the cation and anion sub-lattices which form a neutral defect (Tilley, 2005).
- A Frenkel defect is created when an ion abandons a lattice sight and occupies an interstitial position (Nishi and Doering, 2000)
- An antisite defect is formed in compounds whose atoms are less strongly ionized such that species exchange sites so that an A atom appears at the B sub-lattice or vice versa. This type of defect is fairly common in GaAs (Fleetwood and Schrimpf, 2008).

Extrinsic defects arise in impure crystals due to foreign atoms containing different charge states to the ions they replace. They can reside in substitutional sites or assume interstitial configurations. In some cases they combine to form defect complexes. In GaAs the vacancies and interstitials are symbolized as V_{Ga} , V_{As}, Ga_i and As_i. Antisite defects are symbolized by Ga_{As} and AS_{Ga}. In the past the EL2 has been associated with complex defect configurations such as $As_{Ga}V_{Ga}V_{As}$ but of late it has been almost exclusively associated with AsGa (Overhof and Spaeth, 2005).

3.3.1 Electronic properties of point defects

Point defects change the local lattice potential and may introduce secondary electronic states in the bandgap. In the nomenclature used in this chapter, a defect state within the band gap will be referred to as a trap. According to Mooney (1999) the trap can either be

- An electron trap if its energy level is closer to the conduction band than to the valence band and $c_n > c_p$ where c_n is the rate of electron capture and c_p is the rate of hole capture. If an electron trap increases in positive charge when ionized it is referred to as a donor.

- A hole trap if its energy level is closer to the valence band that to the conduction band $c_n \geq c_p$. If a hole trap becomes more negatively charged when it emits a hole it is referred to as an acceptor.
- A midgap level or recombination center when both c_n and c_p are large

The electron capture rate is given by

$$c_n = \sigma_n \langle v_{th} \rangle n \tag{3.1}$$

and the hole capture rate is given by

$$c_p = \sigma_p \langle v_{th} \rangle p \tag{3.2}$$

where p and n are the hole and electron trap concentrations, σ_p and σ_n are the capture cross sections and $\langle v_{th} \rangle$ is the thermal velocity of the electrons (Auret and Deenapanray, 2004). Charge contributes to a defect's capture cross section as it determines whether it is going to be attractive, repulsive or neutral to carriers. Position of the trap in the bandgap determines the probability of re-excitation into E_V or E_C. The thermal velocity

$$\langle v_{th} \rangle = \sqrt{\frac{3kT}{m_e^*}} \tag{3.3}$$

where m_e^* is the effective mass of the electron. A symmetrical equation holds for holes. Thermal emission rate is directly proportional to a Boltzmann factor $\exp(-\Delta E(kT))$ where $\Delta E = E_C - E_T$ is the energy of the trap from the band edge with E_C and E_T being the energies of the conduction band and trap respectively (Okumura, 2001). Using the principle of detailed balance which states that in neutral material at thermal equilibrium emission and capture rates must be equal, the emission rates of electrons to the conduction band is given by

$$e_n(T) = \frac{g_0}{g_1} \sigma_{ap} \langle V_{th} \rangle N_c \exp\left(-\frac{E_C - E_T}{kT}\right) \tag{3.4}$$

g_0/g_1 is the degeneracy between filled and empty levels and N_C is the effective density of states in the conduction band given by

$$N_C = 2M_C \left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}} \tag{3.5}$$

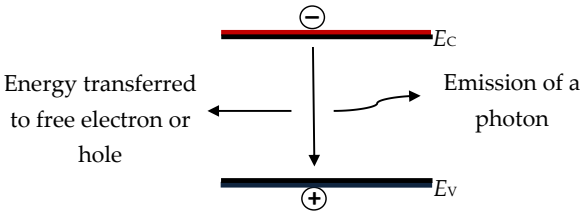
(Blood and Orton, 1978) M_c is the number of equivalent band minima (=3) for GaAs

3.3.2 Shallow and deep level defects

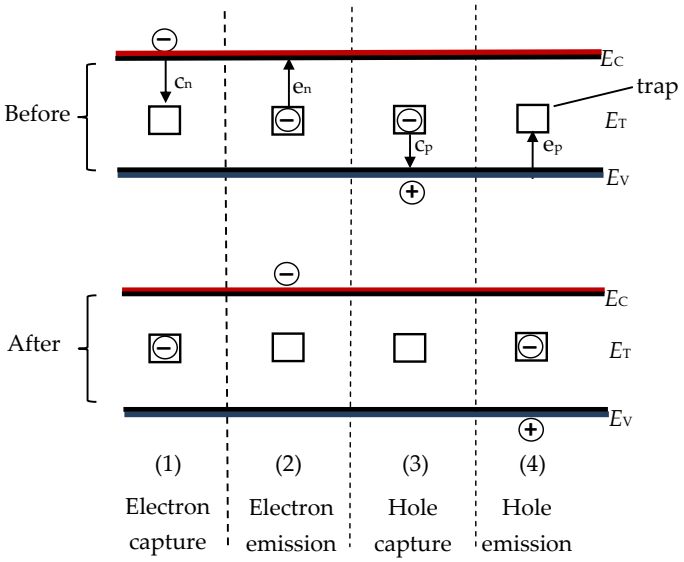
Defects can be classified as shallow level defects or deep level defects. Shallow level defects are donors or acceptors that bind one charge carrier. The properties of shallow levels agree with those predicted by the Bohr model of the hydrogen atom (Poole and Charles, 2004). Deep levels are defects with properties deviating from those predicted by the Bohr model of the hydrogen atom.

3.3.3 Capture and emission

The occupancy of deep levels is changed through carrier transitions between bands. An electron captured from the conduction band can stay until it is emitted due to thermal or optical excitation or until a hole is captured. After that it can either emit the hole or capture an electron Schroder (2006) as shown in Figure 3.2.



(a)



(b)

Figure 3.2: a) band to band recombination, b) Possible interactions between a defect level and the energy bands, E_T is the effective energy of the trap.

The possible transitions are

i) Carrier regeneration

ii) Electron trapping

iii) Hole trapping

iv) Recombination

In Figure 3.2b) a recombination event occurs in the order (1) then (3). A regeneration happens if (4) occurs after (2). If (1) is followed by (2) or (3) is followed by (4) then the event is classified as trapping.

3.4 Deep level transient spectroscopy

DLTS measures the capacitance of a MS junction due to emission of carriers by defects in the space charge region. The emission rate is obtained by processing a capacitance signal. It is based on the Equation 3.4 and is attributed to Lang (1974) who presented a way of displaying emission data spectroscopically as a function of temperature (Peaker et al., 2012). As a result the properties of deep states can be probed by perturbing their occupancy and their carrier density then observing the relaxation. A voltage pulse can be used to fill and empty charge traps so as to scrutinize them. The defects will be detected at a temperature determined by their capture cross section and position in the energy gap.

The depletion with (w) of a SBD extends with applied bias (V) as approximated by

$$w = \sqrt{\frac{2\epsilon(V_{bi} + V)}{eN}} \tag{3.6}$$

The corresponding junction capacitance is a function of the junction area (V). This implies that the magnitude of the bias during a pulse time t_p determines the magnitude of w (Benton, 1990). Hence we can monitor the concentration of holes or electrons trapped by deep levels using capacitance.

$$C = \frac{\epsilon A}{w} \tag{3.7}$$

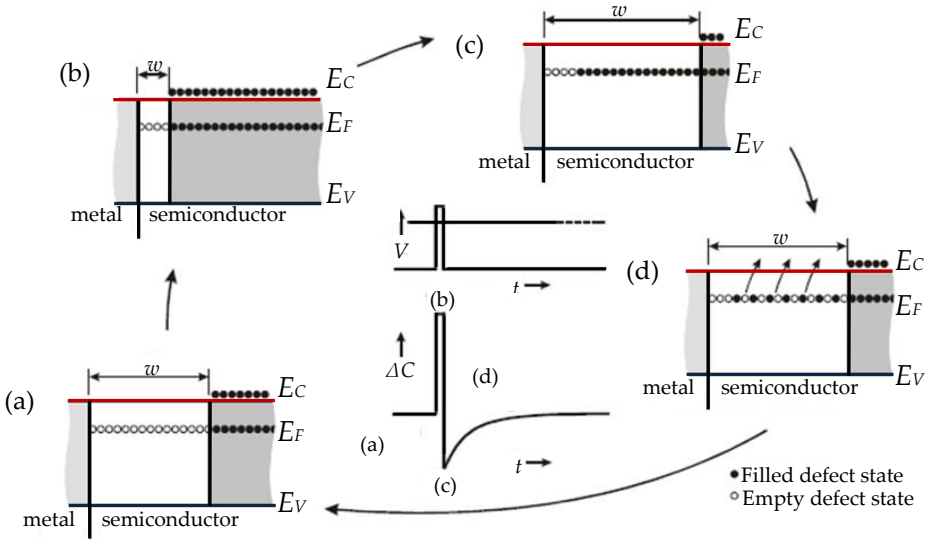


Figure 3.3: Variation in trap occupancy for a DLTS scan cycle a) reverse bias b) filling pulse c) directly after pulse removal, c) time t after pulse removal.

In Figure 3.3(a) Under a steady state with reverse bias V_R traps in the depletion region below the Fermi level are assumed empty. When the filling pulse is applied (Figure 3.3(b)) the depletion width is reduced allowing free carriers to enter the depletion region corresponding to the applied bias. V_R and V_P determine the section of the space charge region where the trapping deep levels are situated (Simoen et al., 2015). Upon entry the electrons are captured by empty traps at an exponential rate given by

$$N(t) = N_T[1 - \exp(-c_n t)] \tag{3.8}$$

where N_T is trap density (Auret and Deenapanray, 2004).

At the end of the pulse V_R returns to its steady state value. In Figure 3.3(c) electrons quickly acted upon by the junction electric field are emitted.Finally in Figure 3.3(d) trap occupancy exponentially relaxes and there is thermal emission of the trapped charges.

The parameter space of DLTS is made up of the following

1 Filling pulse.

2 External reverse bias V_R.

3 Duration of the pulse width t_p.

4 Rate window frequency.

5 Sample temperature.

In a DLTS scan the sequence is repeated periodically. The capacitance transient's time constant is a function of the trap's emission rate. Probability of finding a deep level unoccupied at the beginning of the capacitance transient is determined by the pulse width.

3.4.1 The rate window scan

A trap exhibits a typical temperature at which a peak in DLTS signal is observed. At lower temperatures, the emission rate will be slow and at higher temperatures the emission rate will be very fast. As a result the nature of the time constant is expected to vary with increasing or decreasing temperature (Simoen et al., 2015).

In a rate window scan the capacitance is monitored over an observation time window, (t_1-t_2). The difference in capacitance C(t_1)-C(t_2) gives a peak shaped curve as shown in Figure 3.4.

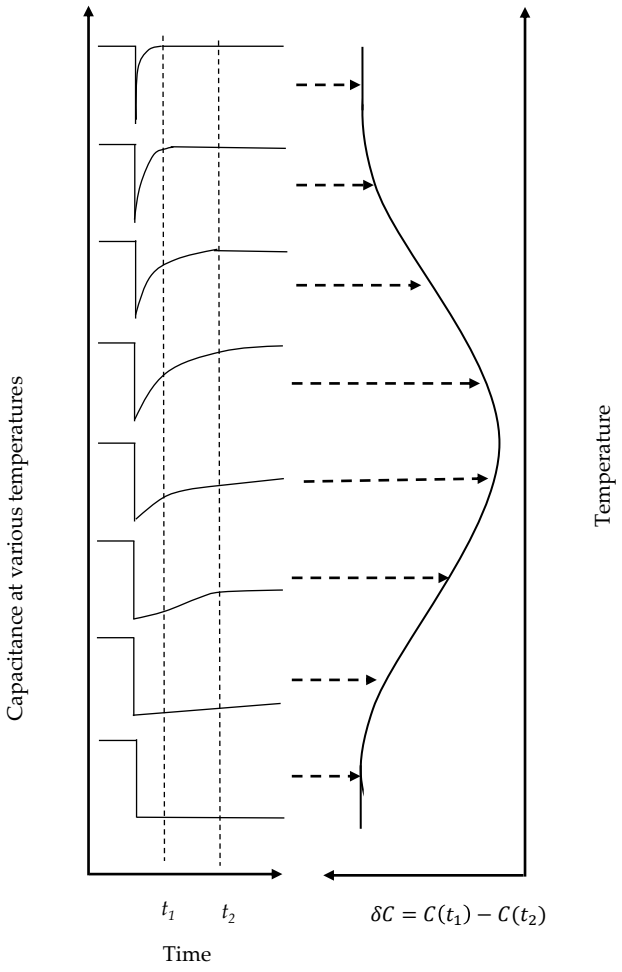


Figure 3.4: Left: change in the capacitance transient with increasing temperature Right: DLTS obtained from plotting δC.

The peak maximum corresponds to an emission rate given by Lang (1974)

$$\tau_n = \frac{t_2 - t_1}{ln(\frac{t_1}{t_2})} \tag{3.9}$$

If the scan is repeated for several rate windows $(t_1 - t_2)$ pairs. Arrhenius analysis can be done according to Equation 3.4 from the slope of the linear fit(least squares) of a $\ln(e_n/T^2)$ versus (1/T) curve to get the activation energy from the slope and

the capture cross section from the y-intercept. If we assume that the peak height is directly proportional to the defect concentration, then concentration can be obtained from

$$N_T = \frac{2\Delta C}{C} N_D \tag{3.10}$$

where ΔC is the capacitance change immediately after removing the filling pulse (Carter and Norton, 2013).

3.4.2 Limitations of DLTS

The limitations of DLTS emanate from its deficiencies in resolution when it comes to separating closely spaced transients or different impurities with similar emission properties (Dobaczewski et al., 1994). This is also compounded in some cases by the Pole-Frenkel effect which results in an increased emission with increasing field. As a result the emission from a specific defect will change continuously within defined limits in the range of fields within a depletion region (Goodman et al., 1994). In addition, DLTS is also not effective for high resistivity materials due to problems in obtaining a proper junction in them. It is mainly used for defect identification purposes but cannot decipher the chemical or microscopic structure of defects.

3.5 Laplace transform DLTS

A quantitative improvement in DLTS resolution was introduced by Dobaczewski et al. (1994). This technique is based on the assumption that capacitance transients are characterized by a spectrum of emission rates. It makes use of Tikhonov's regularization to separate the constituent exponentials by imposing a constraint on the second derivative (Eiche et al., 1992). Then using inverse Laplace transforms

$$f(t) = \int_0^\infty F(s) e^{-st}\, ds \tag{3.11}$$

where $F(s)$ is the spectral density function an inverse function of $f(t)$ the recorded transient (Dobaczewski et al., 1994). $F(s)$ is a delta function therefore a plot of $F(s)$ versus emission rate produces a spectral function which can be used as a defect signature. The area under each peak is directly related to the trap concentration and is a function of the emission rate. Up to 32000 transients can be captured

at a fixed temperature and averaged. Fixing the temperature improves the time constant resolution. A good signal to noise ratio provides an order of magnitude better resolution than conventional DLTS (Dobaczewski et al., 2004).

3.6 Radiation damage due to ion implantation

Radiation damage introduces various defects in solids. The defects introduced can be impurities or structural defects (Section 3.2). Important factors of the defect formation include ion mass, dose rate, total dose, target species and temperature (Haskell et al., 1971). As it slows down , an implanted atom causes a cascade of displacements as it collides with target atoms (Dresselhaus and Kalish, 2013). The displaced atom leaves a vacancy and occupies a substitutional or interstitial position whereas the implanted ion may become a substitutional impurity by occupying an interstitial position or a vacancy (Gibbons, 1972). Implantation induced changes correlate to changes in conductivity (Yang and King, 1995).

Defects generally diffuse to regions of lower concentrations. Upon formation an interstitial moves around and if it encounters a vacancy they combine to form a Frenkel pair or in some cases to recover the solid. For low radiation doses simple point defects are created at low concentrations. At high doses the defects cluster to become complexes (Rimini, 2013). In ionic bonded and covalently bonded solids, the energy required to form a vacancy equals the sum of energies needed to break the bonds binding the atom and move it to the crystal surface (Crawford and Slifkin, 2013).

3.7 Defects introduced by Electron beam deposition (EBD)

A brief description of the EBD technique is given in Section 4.2.5. EBD is known to introduce defects in semiconductor materials. Several researchers have speculated on the mechanisms of formation of these defects. It was Ning (1978) who first speculated that X-rays originating when the EB electrons strike the molten metal cause the defects in the material. This viewpoint was countered by Nel and Auret (1988) during electrical characterization of defects introduced during metalization of epitaxial *n*-GaAs. They showed that the damage was being caused by stray

electrons from the electron (E-)gun during deposition and electrons backscattered by the metal target. An exposure to the stray electrons without an actual deposition showed the presence of all electron beam deposition (EBD) defects observed during the actual evaporation.

At that time formation of point defects was widely believed to be a result of elastic collisions within the sub-lattice resulting in elastic scattering. The electrons in their experiment had a maximum energy of around 3.6 keV which fell short of the threshold displacement energies for GaAs. This led them to speculate that another process other than scattering was responsible for formation of the defect species. Another viewpoint was from Christensen et al. (1992) who speculated that low energy ions are produced close to the filament during the evaporation process which collide with the sample and introduce defects.

This is contrary to what was observed by Auret et al. (2012a) who placed a shield in the path between the sample and the E-gun. They also placed the sample at a distance away from the E-gun. Nonetheless they observed the defects on *n*-Si. Their results showed that exposing *n*-Si to EBD conditions without depositing any metal results in a totally different defect species to what is observed from high energy electron irradiation.

Using the same experimental setup as Auret et al., Coelho et al. (2015) came to a conclusion that a different defect formation mechanism was at play since there was not enough energy to form Frenkel pairs. In their EBE experiments they observed different defects in germanium to those observed during EBD or after ion implantation. They speculated that this was due to intrinsic non-localized excitations, which modify defects deeper in the surface rendering them observable. According to them energy was actually transferred without an interaction with the lattice structure but through phonon activity.

Chapter 4

Experimental techniques

4.1 Introduction

In this chapter we briefly describe the apparatus and experimental techniques that were used. Silicon doped *n*-GaAs supplied by Spire Corporation and Epi Materials Limited with free carrier densities of approximately 1.0×10^{15} cm^{-3}, MOVPE grown on n^{+} substrates, was used. Its crystal orientation was (100).

4.2 Device fabrication

4.2.1 Cleaning procedure

Before fabrication of MS devices meticulous cleaning is required. Dedicated glassware and tweezers are used for each cleaning stage in order to avoid contamination and make devices that have almost ideal parameters. The cleaning procedure is done in three parts. Firstly degreasing is done in-order to remove surface contaminants. The degreasing procedure was performed in two steps namely

- Boiling in trichloroethylene for 3 minutes.
- Boiling in Isopropanol for 3 minutes.

Thereafter the samples were rinsed in deionized water and the first etching step followed in-order to remove any surface states and/or dangling bonds.

- A dip in a solution of H_2O: H_2O_2: NH_4OH in the ratio 100:1:3 for 30 seconds.

Wet etch steps are highly affected by temperature. After preparation etch solutions have to be used immediately. The advantage of wet etching is that it doesn't cause surface electronic damage as is the case for dry etching. A brief description of the inductively coupled plasma etching process is given in Section 4.2.6. After rinsing again in deionized water, the second etching step is done which involves

- A 1 minute deep in a solution of H_2O : HCl in the ratio 1:1.

This final etching step is done in order to remove oxides on the top layer. The samples are rinsed again in deionized water and dried with nitrogen gas.

4.2.2 Ohmic contacts

Immediately after chemical etching, samples were quickly transferred into the vacuum chamber of an Edwards 304 resistive coating unit. The vacuum was pumped down to a pressure of approximately 1×10^{-7} mbar. A Au:Ge eutectic was evaporated on the n^+ backsides of the samples to form an ohmic contact with a Au overlayer. Thereafter the contacts were annealed for 2 minutes at 450 °C in Ar to alloy and lower the contact resistance.

4.2.3 Schottky contacts

A cleaning procedure same as the one followed in Section 3.3 was followed. The only difference was that instead of boiling the dipped samples were placed in an ultrasonic bath at room temperature during degreasing. Once etched the samples were loaded into either a resistive deposition chamber or an electron beam deposition (EBD) chamber. High purity metals were deposited through a metal mask, to make circular contacts of 0.6 mm radius. A cross sectional profile of the fabricated SBDs is shown in Figure 4.1.

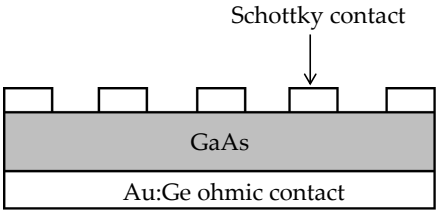


Figure 4.1: Schematic representation of the cross section of a SBD showing fabricated metal contacts.

4.2.4 Resistive evaporation (RE)

Resistive evaporation systems are made up of a vacuum chamber, crucibles, a substrate holder and a thickness monitor. A high voltage is applied across a crucible heating it and evaporating the metal under vacuum. The thickness of contacts being deposited on the material is recorded by a quartz crystal monitor. For good quality contacts small conical crucibles that require a relatively less amount of heating before the evaporation starts are used. High heat can cause annealing of the samples. Resistive evaporation does not introduce any defects in the semiconductor material. However its limitation is that it can only be used on metals of relatively lower melting points e.g. platinum at 1554 °C.

4.2.5 Electron beam deposition (EBD) and exposure (EBE)

An EBD system is made up of a vacuum chamber, metal crucibles, substrate holders, a thickness monitor, a water cooled hearth, electron emitter and magnetic lens. A filament is heated to source electrons which are then accelerated and focused on a metal target by electromagnets. The accelerated electrons thermally evaporate the metal towards the sample. EBD can deposit metals with higher melting points at a more controllable rate. Depositions of ruthenium and tungsten were done at a pressure of approximately 1×10^{-6} mbar. This pressure changed during device fabrication depending on the metal beam current and duration of deposition.

In EBE samples are mounted in a vacuum chamber under EBD conditions without actually depositing the metal. The electron beam is focused on a metal target at a beam current that is insufficient to deposit the metal. The energy of the electron source is 10 keV. (N_2:H_2) foaming gas is introduced in the chamber to maintain

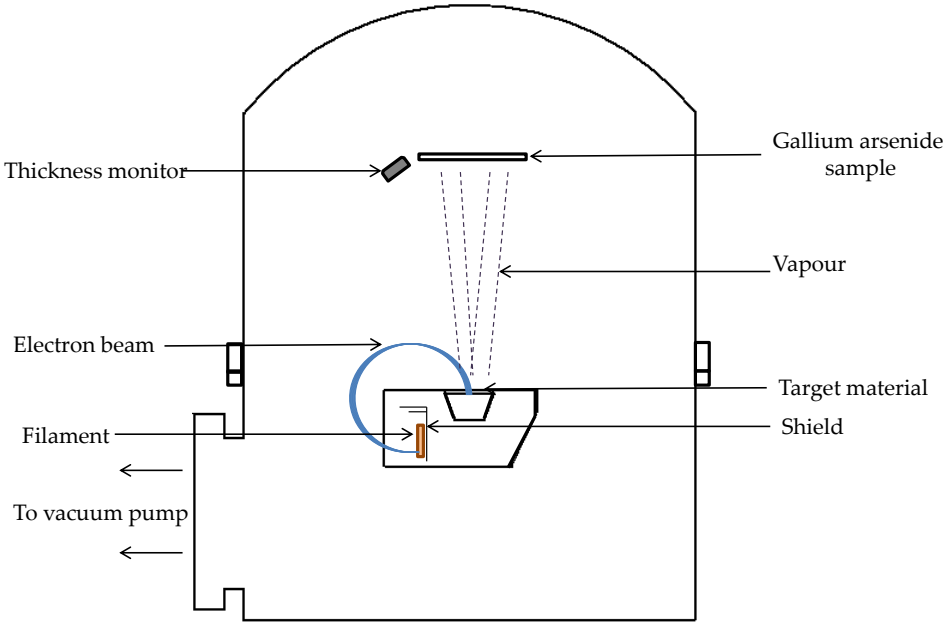


Figure 4.2: Schematic representation of the electron beam deposition system.

pressure constant. In our experiments a tungsten metal target was used at a pressure of 1×10^{-4} mbar and a beam current of 100 mA. Thereafter Schottky contacts are deposited on exposed samples using resistive evaporation.

4.2.6 Inductively coupled plasma (ICP) dry etching

Plasma etching is a processing step meant to rid the semiconductor surface of any contaminants and improve its morphology. ICP dry etching is classified as high density plasma etching (HDPE). It uses two power supplies, one generating the plasma and the other controlling the ion energy by providing RF power (Baca and Ashby, 2005). Inductively coupled RF power dissociates source gases to generate the plasma. A Copra DN200 GT source built by CCR Technology was used. This source is located in the same chamber shown in Figure 4.2. RF power is supplied by a CESAR RF power generator. After loading the samples into the vacuum chamber, a pressure burst of Ar was used to ignite the plasma. Ar partial pressure was maintained within a range corresponding to the required ion energy (20 eV). Samples were placed in a position adjacent to the plasma source for 5 minutes during the etch.

The energetic particles that make up the gas plasma (not exclusively Ar ions) are known to introduce electrically active defects close to the MS junction (Auret et al., 2012b)

4.3 Defect introduction by alpha and beta particle sources

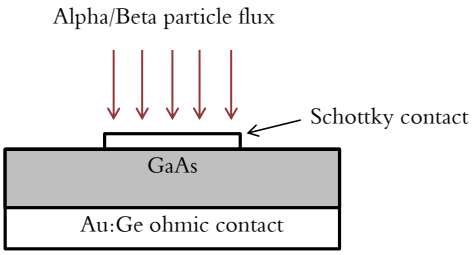


Figure 4.3: A schematic representation of an particle flux incident on a SBD.

A detailed description of the alpha-particle source used in this study was reported by Auret et al. (1993). Owing to the long half-life of the radioactive isotope, the source is not expected to have undergone significant change. The Am-241 radionuclide has a half-life of 433.6 years. Energy ranges of the emitted particles are between 5.4 MeV and 5.5 MeV at a flux of 7.1×10^6 cm^{-2}s^{-1}. Devices exposed to this source are placed in contact with the Am 241 foil for irradiation. Figure 4.3 shows a radiation flux incident on a SBD.

The beta particle source is an Sr-90 radionuclide with a half life of 28.8 years.This electron source emits electrons within the energy range 100-2000 keV at a flux of 6.8×10^9 cm^{-2}s^{-1}. Devices exposed to this source are put in close proximity but not in direct contact.

4.4 Characterization Techniques

4.4.1 *I-V* and *C-V* measurements

I-V and *C-V* meauserements are carried out by a system consisting of a probe station, HP4140 pA meter/DC voltage source and a HP 4192A LF Impedance analyser with a current limit of 1.0×10^{-14} A. Devices are placed on the probe station in

a cubic dark housing to avoid light inteference. The measurements are controlled by a Labview^{TM} program. The programme measures and generates various plots and calculates diode parameters such as the ideality factor (n), barrier height (ϕ_{IV}) and device series resistance from *I-V* results. From *C-V* results the program calculates the carrier concentration (N_D), barrier height (ϕ_{CV}) and built in voltage (V_{bi}) as well as plotting carrier concentration depth profiles. For *C-V* characterization, an a.c. voltage with an oscillating frequency is superimposed on a d.c. bias in a desired range to obtain the capacitance.

4.4.2 Temperature dependent measurements (*I-V-T* and *C-V-T*)

The same setup described in section 4.4.1 is used. However for temperature control samples are mounted in a JANIS closed cycle helium cryostat. Heat is supplied through a conducting stage made of sapphire and indium foil. The temperature is monitored by a Lakeshore 340 temperature controller with a sensitivity of ± 0.1 K. In a study to observe the effect of high temperatures on the electrical characteristics of Au/n-GaAs SBDs temperature cycling was employed. We designed an experiment to track any modifications to the devices as a result of heating during operation. The measurements were done by carrying out a measurement at an elevated temperature (annealing mode) and at room temperature immediately afterwards (post annealing mode).

4.4.3 DLTS measurements

The DLTS setup consists of

- A helium cycling cryostat with a conducting stage made of indium and sapphire where the sample is mounted. The stage has an inbuilt heater and the cryostat provides cooling power of up to 10 K.
- A Lakeshore 340 temperature controller.
- Boonton 7200 capacitance meter with a 100 mV a.c. ripple voltage, at 1MHz with an offset bridge.
- Agilent 3320A 15MHz waveform external generator for providing the required quiescent reverse bias and a filling pulse.

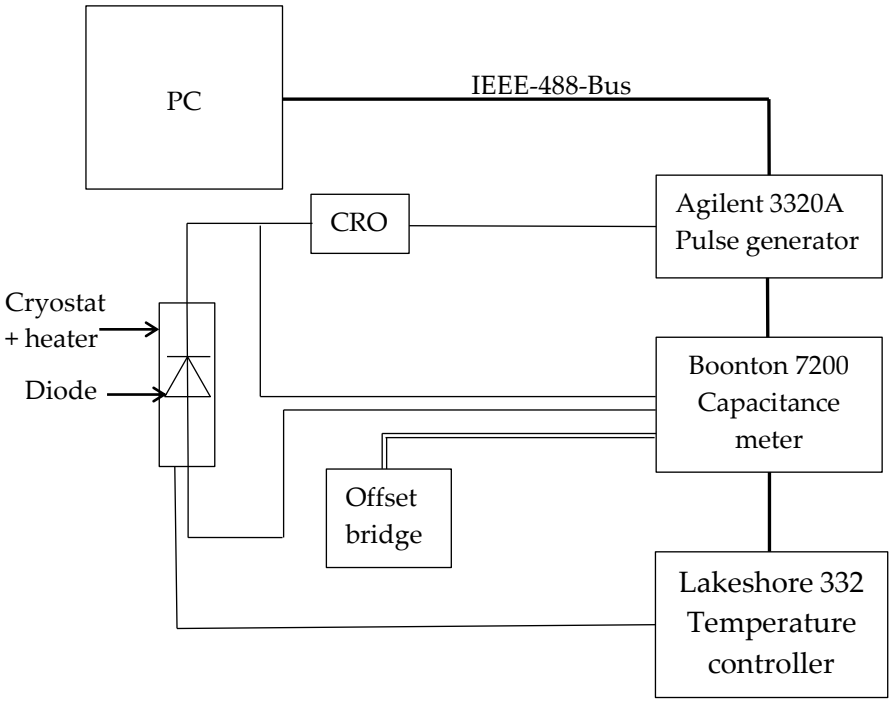


Figure 4.4: Schematic representation of DLTS and L-DLTS instrumentation.

- Computer with A2D card

A block diagram for the measurement system is shown in Figure 4.4. The sample to be measured is mounted on the conduction stage. Two probes connect the ohmic and the Schottky contacts to the capacitance meter. The pulse generator maintains the reverse bias and supplies the filling pulse. The software supplies a capacitance transient which is displayed on the screen of the PC. As temperature is varied a DLTS spectrum is obtained. All the defects observed are then accurately measured using L-DLTS to get the signatures and defect concentrations. The L-DLTS software uses three routines for Tikhonov's regularization namely FITKREG, CONTIN and FLOG. A screenshot of the Front panel for L-DLTS is shown in Figure 4.5

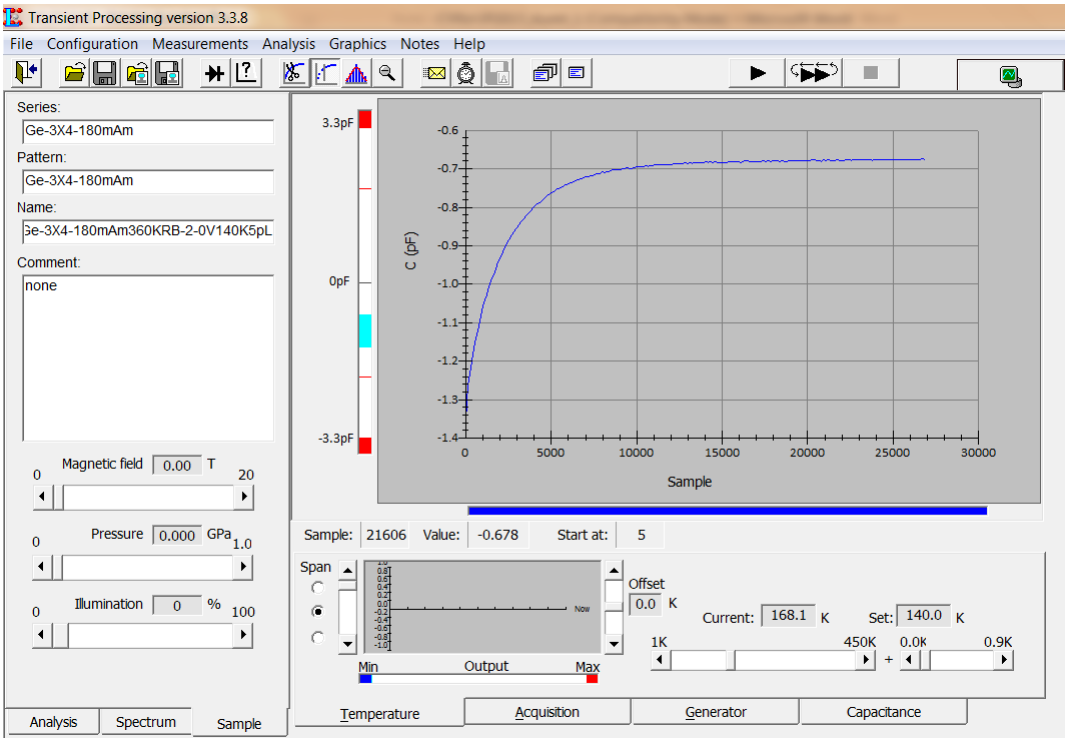


Figure 4.5: Screenshot of the Front panel of Laplace transient processing software.

Chapter 5

Results and discussion

5.1 Introduction

In this chapter a summary of the results will be presented followed by manuscripts that have been submitted to journals for publication. In Section (5.2) results obtained from *I-V* and *C-V* measurements are presented. Temperature dependent measurements *(I-V-T)* and *(C-V-T)* were done in a wide range in-order to observe the effect of the EL2 defect on the electrical characteristics of *n*-GaAs Schottky diodes. Section (5.3) entails a detailed electrical characterization of process induced defects in *n*-GaAs. This is a comparative study of the electrical characteristics of devices that have been subjected to inductively coupled plasma (ICP) etching and electron beam deposition (EBD). Defect formation at sub-threshold energies was investigated by creating the conditions which samples are exposed to during EBD, a technique termed electron beam exposure (EBE). Finally, results obtained from the electrical characterization of radiation induced defects using L-DLTS are presented in the last section (5.4). MOVCD grown GaAs doped with Si to 1.0×10^{15} cm^{-3} was used. DLTS measurements on this material in the 15-390 K temperature range established that the only electrically active defect present in as-deposited material was the EL2 at an activation energy $(E_C - 0.83)$ eV.

5.2 *I-V* and *C-V* measurements on Au/*n*-GaAs SBDs

Before processing or introducing defects, a thorough understanding of the device characteristics of as-deposited SBDs is essential. Figure 5.1 shows the general *I-V*

characteristics of Au Schottky contacts deposited on *n*-GaAs measured at room temperature. Au was chosen because it produces the highest barrier heights compared to other common metals on *n*-type semiconductors (Mayer, 1984).

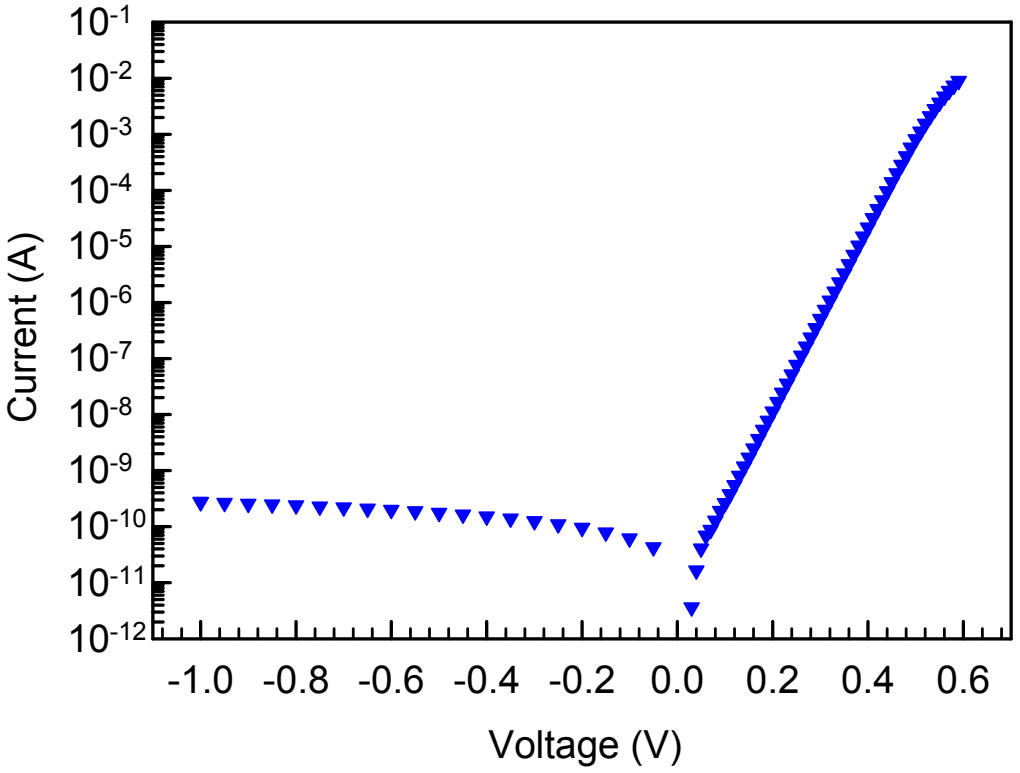


Figure 5.1: *I-V* characteristics of the as-deposited Au/*n*-GaAs SBDs at room temperature.

From the *I-V* graph, it can be deduced that thermionic emission is the dominant current transport mechanism over the barrier. The SBDs show good rectification properties which are attributed to the cleaning procedure used before deposition described in Section 2.3.1 (Baca and Ashby, 2005). Ideality factor and barrier height (ϕ_{IV}) were calculated from a least squares fit of the linear region of the forward bias *I-V* curve using Equations 2.24 and 2.25, respectively.

Table 5.1: Diode parameters obtained from the *I-V* characteristics of as-deposited Au-*n*/GaAs SBDs at room temperature.

Ideality factor,*n*	1.03
Saturation current, I_s (A)	5.99×10^{-12}
Schottky barrier height, ϕ_{IV} (eV)	0.86
Series resistance, R_s (Ω)	3.33

The ideality factor was very close to unity which implies that high quality devices were fabricated. In addition, the curve shows a minimal effect of series resistance. This would be observed as flattening of the *I-V* curve at higher forward current. Series resistance is a function of contact quality and bulk wafer resistivity (Kimoto et al., 1993). The reverse leakage current shows just slight increase with increasing reverse bias.

Figure 5.2 shows the $1/C^2$ versus V curve which was used to analyze the *C-V* characteristics. The equations used were described in section 2.4.3.

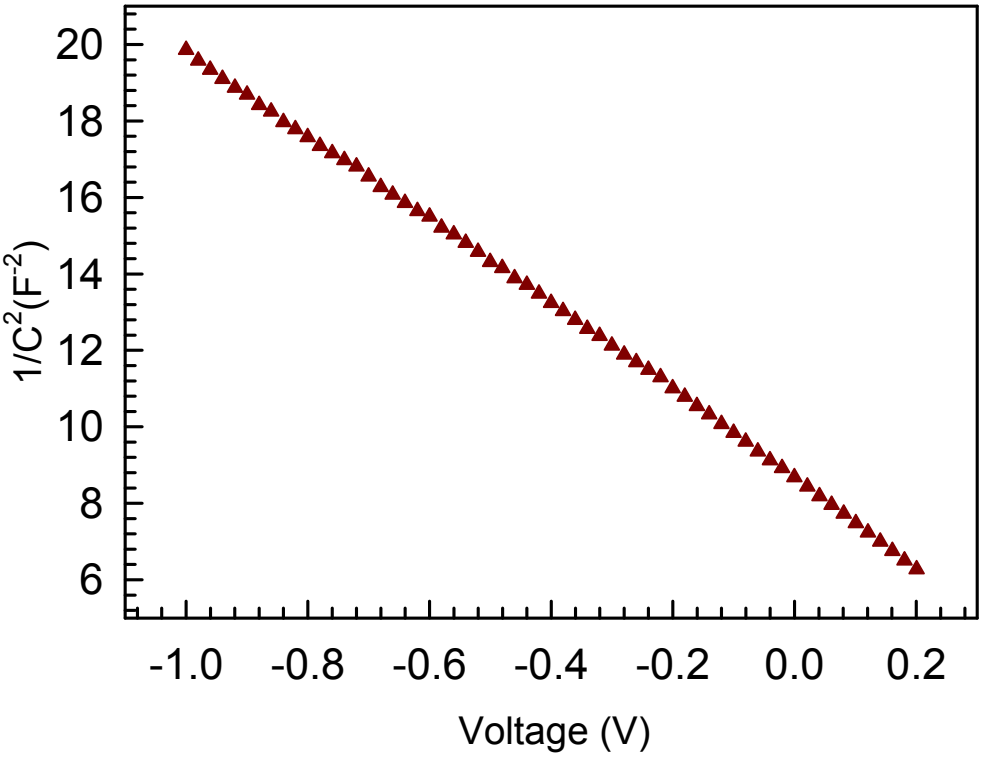


Figure 5.2: *C-V* characteristics of the as deposited Au/*n*-GaAs SBDs obtained at room temperature.

For *C-V* characterization, an a.c. voltage with an oscillating frequency of 1 MHz was superimposed on a d.c. bias in the -1 V to 0.2 V range. The resultant capacitance is dependent on how the charge distribution within the system adjusts itself under applied bias. It is therefore a differential capacitance. The measured free carrier concentration (Table 5.2) confirmed the material specifications by suppliers.

Table 5.2: Diode parameters obtained from the *C-V* characteristics of as-deposited Au-*n*/GaAs SBDs at room temperature.

Free carrier concentration, N_D(cm^{-3})	1.02×10^{15}
C-V barrier height, ϕ_{CV} (eV)	0.86
V_{bi}, (eV)	3.33

5.2.1 *I-V-T* and *C-V-T* measurements

The results from *I-V-T* and *C-V-T* measurements are presented in Paper 1 appended at the end of this chapter. A strong dependence of diode characteristics on temperature was observed. At temperatures greater than 400 K large deviations from pure thermionic emission were observed. The main finding was that the influence of the EL2 defect split the *C-V* barrier height vs T graph into two ranges each with a unique temperature coefficient. Figure 5.3 shows two linear fits of these regions. Variation of the carrier concentration also confirmed the assertion. Increase in temperature caused the EL2 to release trapped carriers thereby contributing to the measured carrier concentration.

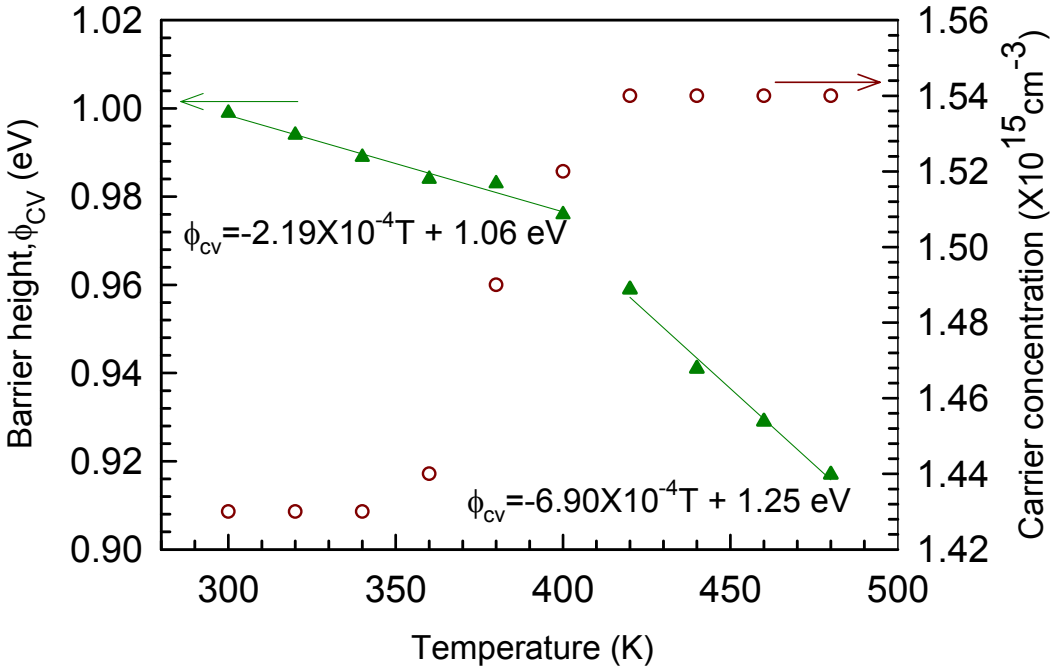


Figure 5.3: Variation of free carrier concentration and *C-V* barrier height with temperature of Au/*n*-GaAs SBDs.

5.3 Process induced defects

5.3.1 *I-V* and *C-V* characteristics

In this section, results obtained from measurements on SBDs that have been exposed to different processing techniques are presented. The desirable diode characteristics are high *I-V* and *C-V* barrier height and an ideality factor close to unity. Figure 5.4 shows the *I-V* characteristics of devices that have been:

i) Dry etched by ICP before resistive evaporation of Au Schottky contacts (ICP).

ii) Exposed to electron beam evaporation conditions before resistive evaporation of Au Schottky contacts (EBE).

iii) Fabricated by resistive evaporation (RE)

iv) Fabricated by electron beam deposition (EBD).

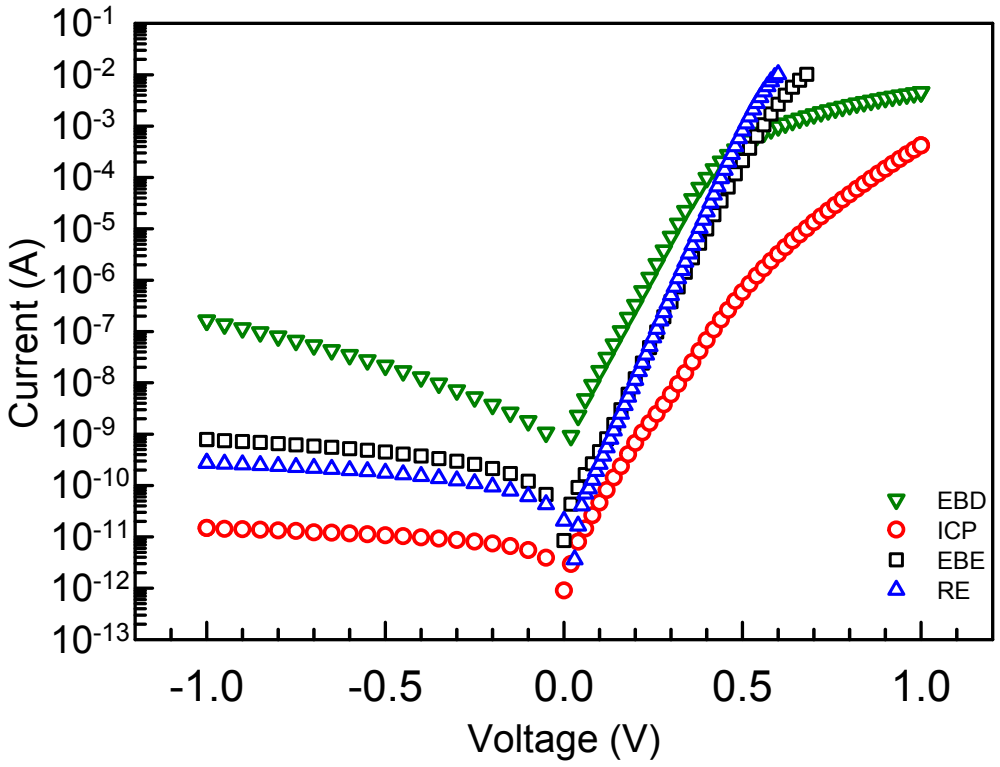


Figure 5.4: *I-V* characteristics of ICP etched Au/*n*-GaAs SBDs, EBE processed Au/*n*-GaAs SBDs, EBD fabricated W/*n*-GaAs SBDs and Au/*n*-GaAs SBDs fabricated by resistive evaporation (RE).

Thermionic emission remains the dominant current transport mechanism in all the devices. The *I-V* plot for the ICP exposed sample shows evidence of generation-recombination current at low voltages and dominance of thermionic emission at greater voltages. Analysis of the *I-V* characteristics was strictly done on linear regions that resemble thermionic emission only.

Table 5.3: Diode parameters of *n*-GaAs Schottky diodes exposed to different processing techniques.

Process	n	ϕ_{IV}(eV)	ϕ_{CV}(eV)	Current at -1 V (A)
ICP	1.46	0.87	1.15	1.48×10^{-11}
EBE	1.17	0.84	1.02	7.80×10^{-7}
EBD	1.29	0.78	0.91	1.63×10^{-7}
Resistive	1.03	0.86	1.02	1.50×10^{-9}

The data in Table 5.3 shows that processing affects the electrical characteristics of the devices. Among other changes, processing can introduce change in surface stoichiometry which can introduce surface states and change the position where the Fermi level is pinned (Léonard and Tersoff, 2000). SBDs made by RE were used as control devices for the experiment. They had good characteristics with an ideality factor of almost unity and have been discussed in Section 5.2.

The plot obtained from ICP etched samples shows two distinct linear regions as was observed by Ozavc et al. (2013), thus a linear fit was used in the $0.1 < \mathrm{V} < 0.2$ region. Such separate linear regions have been attributed to barrier height inhomogeneities (Mayimele et al., 2015). ICP etched SBDs had the highest ideality factors and had very low reverse leakage current in comparison to the other samples. When considering the barrier height and leakage current, it was clear that ICP improves device characteristics. A similar result was observed in germanium(Coelho et al., 2014). The relatively high ideality factor can be attributed to surface damage by the energetic particles that make up the plasma. As a result, surface or defect states are introduced in the bandgap causing deviation from pure thermionic emission.

For EBD fabricated SBDs, reverse leakage current was higher than the rest of the devices. Flattening of the curve above 0.5 V showed that the devices had a high series resistance. In addition, the diodes also showed the lowest barrier heights. These results confirm that EBD produced the poorest devices of all the techniques under investigation. In the past, EBD has been shown to introduce near surface defect states that result in non ideal diode characteristics (Myburg and Auret, 1992).

EBE processed SBDs showed diode characteristics that were closest to those of the SBDs fabricated with resistive deposition. This shows that there was moderate to low effect on the diode characteristics. In total, all the processing techniques investigated had a significant impact on *I-V* and *C-V* characteristics of SBDs.

5.3.2 Discussion of DLTS results

The main objective was to observe the effects of processing techniques on the electronic properties of the EL2 defect. However, it was observed that processing did not have any significant effect on the defect. It is in that regard that our focus was shifted to other defects introduced by the processing and not the EL2. Figure 5.5 shows normalised DLTS scans in the 15-385 K range.

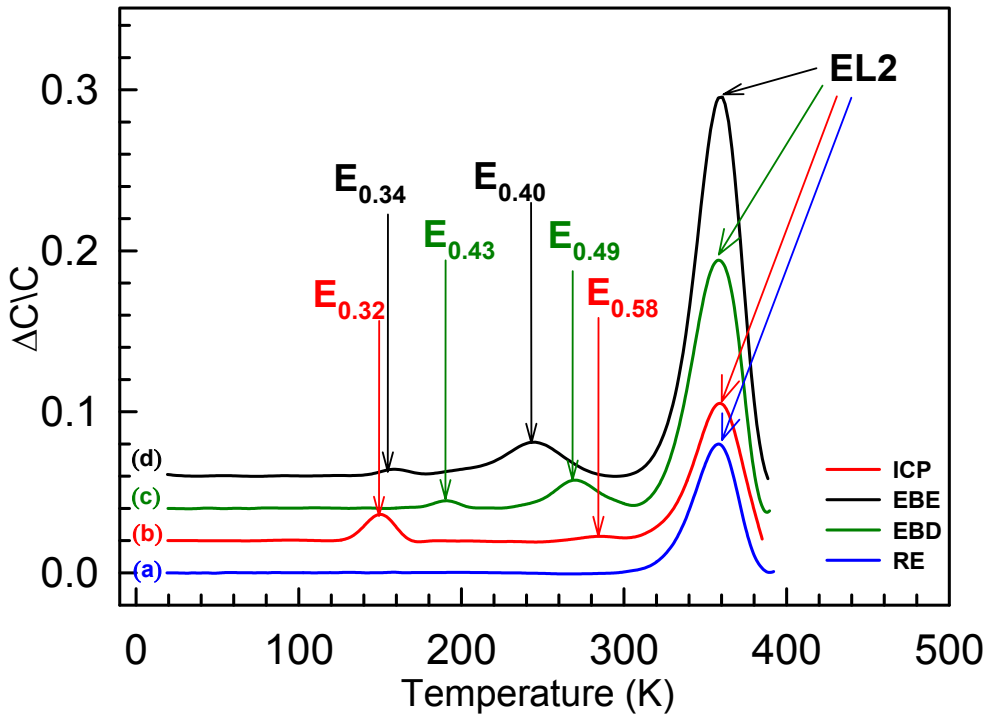


Figure 5.5: DLTS spectra of (a) RE deposited Au/n-GaAs SBDs (b) ICP etched Au/n-GaAs SBDs (c) EBD fabricated W/n-GaAs SBDs (d) EBE exposed Au/n-GaAs SBDs recorded at a quiescent reverse bias of 2.0 V,rate window of 4Hz and a filling pulse width of 1 ms. (The $E_{0.40}$ and $E_{0.49}$ signatures where obtained by averaging L-DLTS emission rates).

5.3.2.1 Inductively coupled plasma (ICP) etching

The resulting spectra show two defect levels induced by the ICP, namely $E_{0.32}$ and $E_{0.58}$. These have been reported in the past by Auret et al. (2012). Their activation energies $E_C - 0.32$ eV and $E_C - 0.58$ eV are obtained from the Arrhenius plots shown in Figure 5.6. The $E_{0.58}$ defect is metastable and can transform reversibly once exposed to annealing at 390 K under zero or reverse bias. This defect appears to be similar to the M4/M3 metastable defect observed in dc H plasma treated GaAs (Nyamhere and Venter, 2012).

ICP induced defects form because of the disruption of the lattice by incident plasma ions leading to the formation of defects such as vacancies and antisites. These ions can also change the surface stoichiometry which results in surface states and a change of the Fermi level pinning position in the process (Baca and Ashby, 2005).

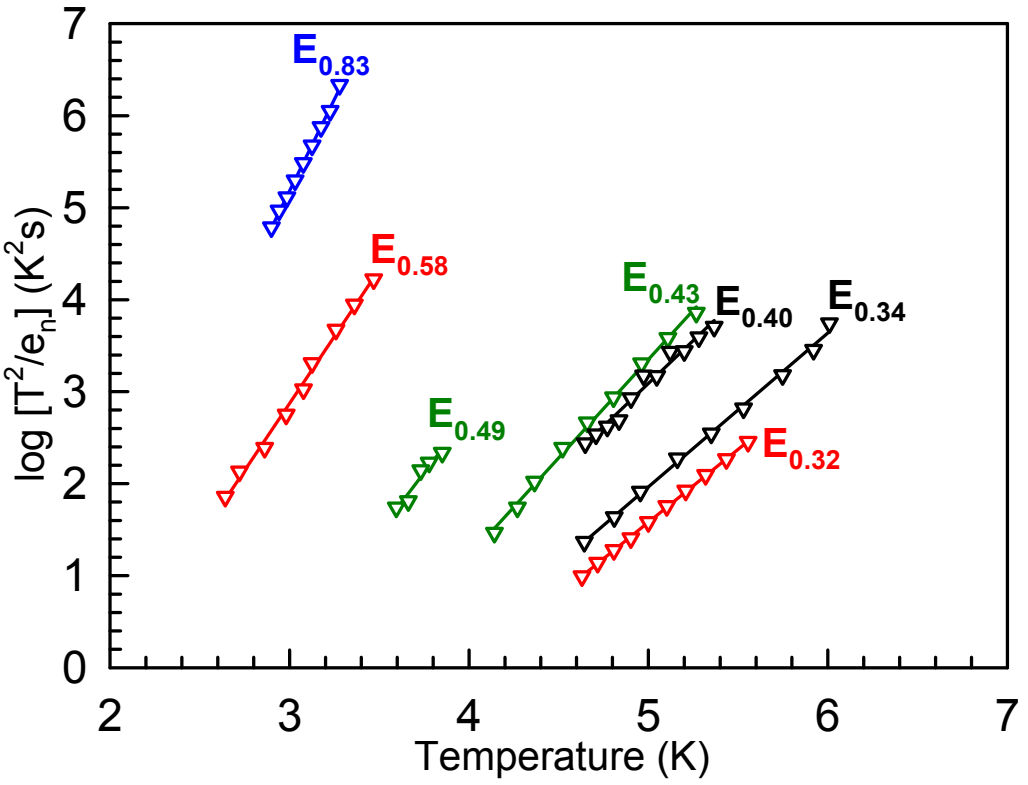


Figure 5.6: Arrhenius plots for defects introduced by EBD, EBE and ICP in *n*-GaAs. (The $E_{0.40}$ and $E_{0.49}$ signatures where obtained by averaging L-DLTS emission rates).

5.3.2.2 Electron-beam deposition (EBD)and exposure (EBE)

In this subsection, we present results obtained from the devices fabricated using EBD and those processed through EBE. The metal that was chosen for EBD was tungsten because it has a high melting point therefore a higher power is required for its deposition. This results in significant damage within the semiconductor.

The EBD and EBE spectra in Figure 5.5 show sets of three peaks each for both spectra (b) and (c). These defect levels were only observable after applying a filling pulse of at least 0.2 V. Owing to this requirement, Auret et al. (2012) suggested that they might originate from a continuum of defect states close to the *n*-GaAs epilayer surface. This is also evidenced by the signatures obtained for the $E_{0.40}$ and $E_{0.43}$ on Figure 5.5. The activation energies obtained from Arrhenius analysis of conventional DLTS results were not in agreement with what is predicted by Equation 3.4 and the temperatures at which the peaks were observed.

L-DLTS spectra from these peaks show a number of peaks which vary inconsistently with varying temperature. This also goes to second the notion of a continuum of energy states. The signature for the whole continuum of defect states was obtained by averaging their emission rates at 5 K steps using L-DLTS. The resulting energy levels were 0.40 eV and 0.49 eV for the EBE and EBD defects respectively as displayed in Figure 5.6.

Table 5.4: Summary of electronic properties of process induced defects in *n*-GaAs.

Defect label	$E_T \pm 0.01$ (eV)	σ_{ap} $\pm 1\%$ (cm^{-2})	Process
$E_{0.32}$	0.32	4.62×10^{-15}	ICP
$E_{0.34}$	0.34	8.26×10^{-16}	EBE
$E_{0.40}$	0.40	2.64×10^{-14}	EBE
$E_{0.43}$	0.43	6.48×10^{-15}	EBD
$E_{0.49}$	0.49	2.39×10^{-13}	EBD
$E_{0.58}$	0.58	2.08×10^{-16}	ICP
$E_{0.83}(EL2)$	0.83	2.80×10^{-15}	Native

From the data in Table 5.4, the EBE defects observed are different to those observed by other processing techniques including EBD. A comparison of their DLTS spectra showed a temperature shift in the positions of the peaks. They were also different to the defects that were reported after ion implantation or particle irradiation (Claeys and Simoen, 2013). Ion solid interactions could not account for the formation of these defects since the energies involved were insufficient. The defects are therefore distinct and their formation mechanism is unique to them. Due to the limitations of DLTS we were only able to identify these defects. At this stage the formation mechanisms of the defects cannot be explained.

5.4 Irradiation induced defects

5.4.1 High energy electron-irradiation induced defects

Electron-irradiation was done using a Sr-90 radionuclide described in Section 4.3. Ruthenium was chosen as Schottky contact material because of the stability of

Ru/GaAs structure (Myburg et al., 1993). At high fluencies, high energy electron-irradiation was observed to introduce the same set of defect levels as those introduced by alpha-particles. This confirms that at such fluences electron irradiation also introduces defects of an extended nature such as vacancy and or interstitial clusters and their combinations with impurities or foreign species (Section 3.6). The *I-V* characteristics were not affected by the irradiation. This is a characteristic of GaAs which has seen it being used in harsh radiation environments like for space solar cells to power satellites (Werthen et al., 1986). In Paper II radiation induced (RI) EL2-like defects are presented. These are defects associated with the EL2 which were not observed in the past due to the low resolution of conventional DLTS. Figure 5.7 shows L-DLTS spectra of these defects.

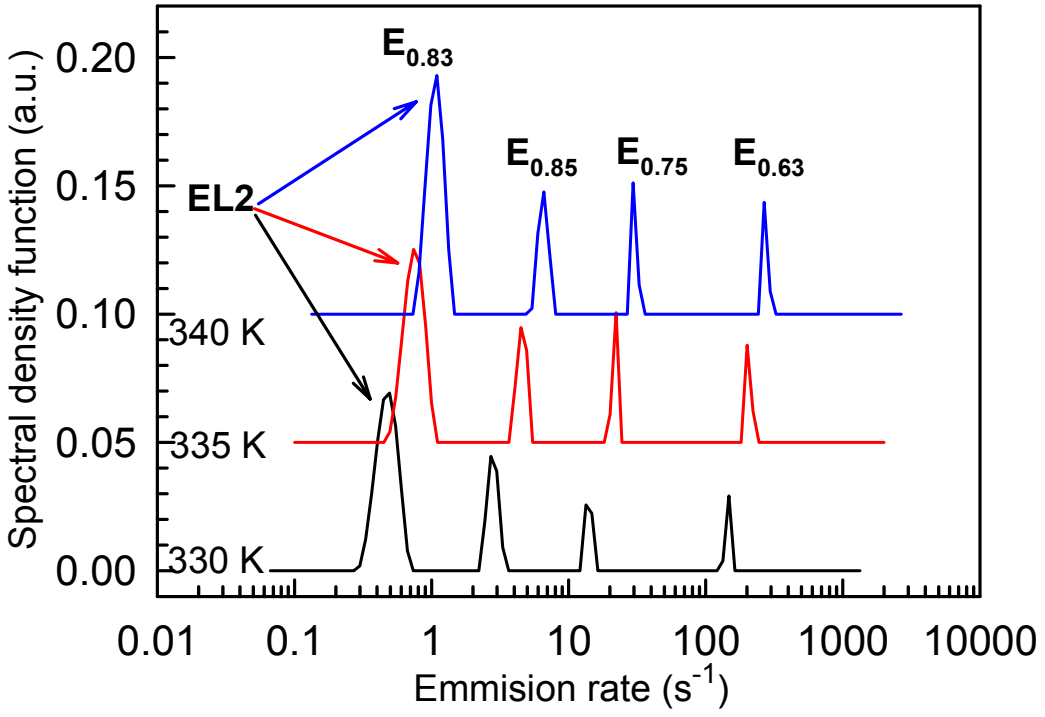


Figure 5.7: Laplace-DLTS spectra of radiation induced EL2-like defects in *n*-GaAs.

5.4.2 Alpha-particle irradiation induced defects

The alpha-particle irradiation was done using an Am-241 radionuclide described in Section 4.3. Alpha particle irradiation did not have any impact on SBD *I-V* characteristics. Of interest is the baseline that is observed on the DLTS spectrum obtained after alpha-particle irradiation. The peaks appear superimposed on a

skewed baseline. This baseline was detected by Laplace DLTS and hence hindered accurate determination of defect signatures. It introduced inaccuracy in the Laplace spectra as its capacitance signal was captured as a relaxation. It was therefore impossible to observe the fine structure of the alpha-particle induced defects using L-DLTS. Paper III has results from conventional DLTS only. Figure 5.8 displays (a) the control spectrum and (b) the spectrum observed after 20 minutes of 5.4 MeV alpha particle irradiation.

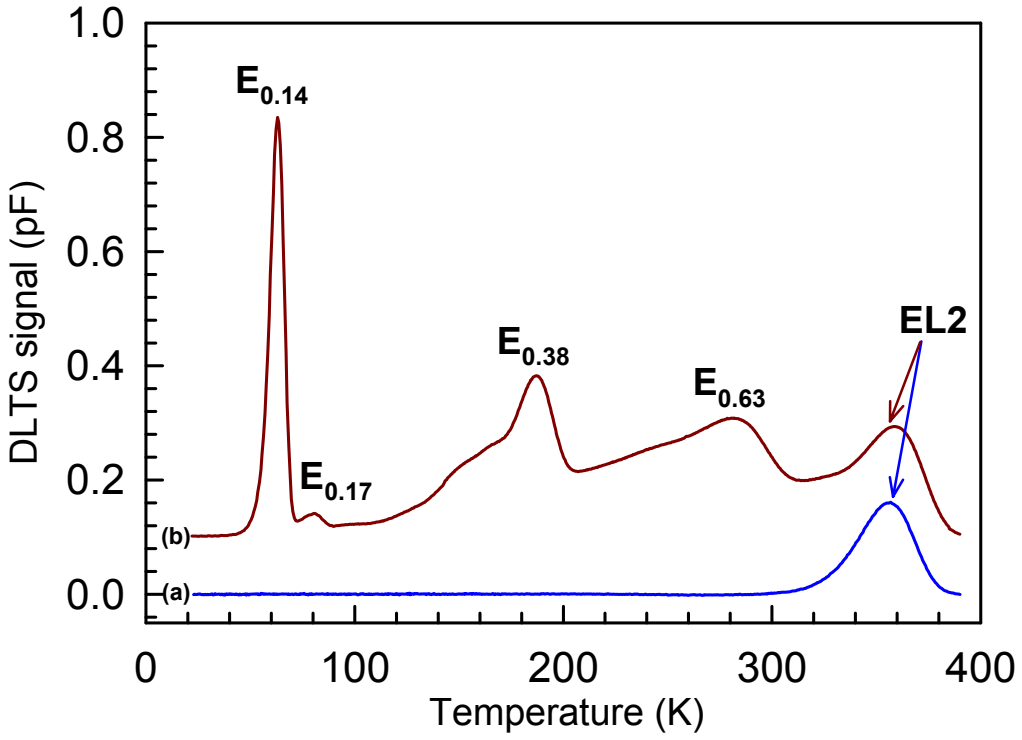


Figure 5.8: DLTS spectra of (a) as-deposited (b) 5.4 MeV alpha-particle irradiated Au/*n*-GaAs SBDs recorded at a quiescent reverse bias of 2 V, rate window of 4Hz, a filling pulse of 0 V and pulse width 1ms.

Paper I

The effect of high temperatures on the electrical characteristics of Au/*n*-GaAs Schottky diodes

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The effect of high temperatures on the electrical characteristics of Au/n-GaAs Schottky diodes

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ABSTRACT

In this study, the current–voltage *(I–V)* and capacitance–voltage *(C–V)* characteristics of Au/n-GaAs Schottky diodes have been measured over a wide temperature range, 80–480 K. The diodes were rectifying throughout the range and showed good thermal stability. Room temperature values for the ideality factor, *I–V* barrier height and *C–V* barrier height were found to be $n=1.10$, $\phi_{IV}=0.85$ eV and $\phi_{CV}=0.96$ eV, respectively. ϕ_{IV} increases and n decreases with an increase in temperature. We investigated the effect of elevated temperatures on the barrier height and ideality factor by measuring the diodes at a high temperature (annealing mode) then immediately afterwards measuring at room temperature (post annealing mode). The measurements indicate *I–V* characteristics that degrade permanently above 300 K. Permanent changes to the *C–V* characteristics were observed only above 400 K. We also noted a discrepancy in the *C–V* barrier height and carrier concentration between 340 and 400 K, which we attribute to the influence of the EL2 defect (positioned 0.83 eV below the conduction band minima) on the free carrier density. Consequently, we were able to fit the ϕ_{CV} versus temperature curve into two regions with temperature coefficients -6.9×10^{-4} eV/K and -2.2×10^{-4} eV/K above and below 400 K.

1. Introduction

Gallium Arsenide is a very important direct bandgap semiconductor. At present it is used for many applications such as solar cells in space, sources and detectors in optical fibres and as microwave sources [1–3]. The high electron mobility and high carrier saturation velocity of the material makes it ideally suited for the fabrication of high frequency and low power devices [4]. Several opto-electronic devices have been implemented on it to date. These include multi junction photovoltaics, MOSFETs and low noise avalanche photodiodes [5,6]. More often these devices require metallization, therefore in order to understand their electrical characteristics we use the simple metal semiconductor (MS) structure also known as the Schottky barrier diode [4].

The quality of a Schottky contact is notably determined by the quality of the interface between the deposited metal and the semiconductor surface [7]. In GaAs-based devices the performance has been experimentally shown to be affected to a greater extent by surface and interface defect density and also the series resistance [8]. According to Tung [9,10] it can also be explained in the chemical bonding picture, where the diode characteristics depend on the atomic structure of the MS interface.

Several researchers have studied the electrical characteristics of Au/n-GaAs Schottky diodes and have reported a strong dependence of diode characteristics on temperature [4,7,8,11–13]. Kim et al. [14] studied the temperature dependence of Au/n-GaAs *I–V* characteristics using a semi analytical model in the 83–323 K temperature range. They reported that the variations in the characteristics with temperature were consistent with those of the energy band gap. Örzeli et al. [12] explained the temperature dependence of the *I–V* and *C–V* characteristics at high temperatures (280–415 K) of Au/n-GaAs Schottky diodes using a Gaussian distribution of the Schottky barrier height. Similar experiments have been undertaken with samples exposed to and measured at the same high temperatures in other materials [15,16]. It is also important to take note of any changes and modifications as they occur when the device is exposed to high temperatures during measurement or operation since diode electrical characteristics are sensitive to heat treatment [17]. The annealing behaviour of GaAs Schottky diodes has already been the subject of a number of investigations [18–21]. Changes brought about to the diode characteristics by thermal annealing have variously been attributed to solid-phase reactions, dispersion of native oxides and failure of diffusion barriers at the interface [21,22].

However, most of these annealing studies were done systematically by exposing the diodes to high temperatures and then

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measuring them at room temperature. There is a need to compare the measurements done during annealing and post annealing. This is because, as the temperature increases, the diodes are annealed and interfacial reactions may ensue. After exposure to these high temperatures the devices may be operated at a different, and usually lower, temperature. Studying the behaviour of the devices during annealing and post annealing may yield insights important for packaging, temperature processing and safe temperature operating ranges for the GaAs devices.

In this study gold contacts were deposited on epitaxial n-GaAs. We investigated the effects of high temperatures by comparing the rectification properties and thermal stability of the MS contacts in two modes: during annealing and post annealing. The post annealing measurements were undertaken at 300 K. These 300 K measurements were designed to track any modification to the Au/GaAs system accompanying the annealing. We also considered and monitored the effects of the EL2 defect on the free carrier concentration and the rectification properties of our samples using Laplace deep-level transient spectroscopy (L-DLTS).

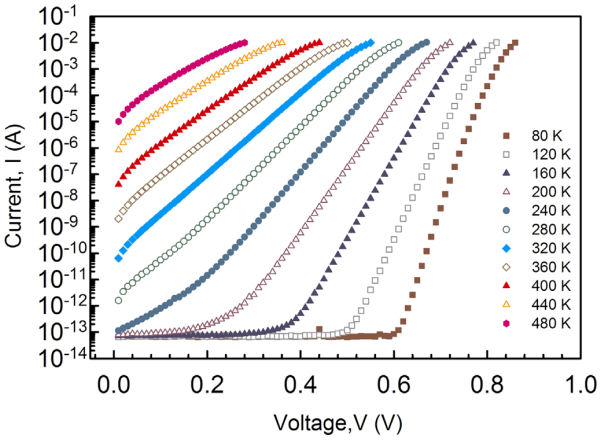

Fig. 1. Semi logarithmic forward current–voltage characteristics as a function of temperature for Au/n-GaAs Schottky diodes during annealing.

2. Experimental details

MOCVD grown n-GaAs with a free carrier density of 1.4×10^{15} cm^{-3} and $<100>$ orientation, supplied by Epi Materials Limited, was used. The wafers were first degreased by boiling in trichloroethylene for 5 min then in isopropanol for 3 min. They were then etched in a fresh solution of H_2O:H_2O_2:NH_4OH (100:1:3) for 60 s and rinsed in 18 MΩ cm deionised water. The second etching step involved removal of the native oxide layer by etching the samples in a fresh H_2O:HCl (1:1), followed by a rinse in deionised water then blow drying in compressed nitrogen gas. Au–Ge (88%:12%) ohmic contacts were evaporated on the back of the wafer in an Edwards 304 resistive coating unit pumped down to 4×10^{-7} mbar. This was followed by thermal annealing at 450 °C for 3 min in flowing argon gas.

The wafers were cleaned again, repeating the degreasing, etching and oxide removal steps. This time, an ultrasonic bath was used instead of boiling. Immediately thereafter the samples were transferred into the vacuum system for Schottky metallization. Circular contacts of 0.6 mm diameter and 500 Angstrom thickness were resistively deposited on the epitaxial layer. Temperature dependent *I–V* and *C–V* characteristics were recorded in the 80–480 K range using a JANIS closed-cycle liquid helium cryostat, an HP4140B pico-ammeter and an HP4192A LF Impedance meter. A Lakeshore 332 temperature controller with a sensitivity of ±0.1 K was used to control the temperature.

The *I–V* and *C–V* investigations were carried out in two modes: (1) during annealing, conducted at some elevated temperature in the 80–480 K range in 20 K steps, and (2) post annealing measurements, conducted at 300 K after the annealing described in (1). Once the correct annealing temperature was established, a further 5 min was allowed for the system to establish equilibrium. All the *C–V* measurements were done at 1 MHz. Finally, Laplace deep-level transient spectroscopy (L-DLTS) measurements were carried out in a JANIS cryostat within the temperature range 80–480 K.

3. Results and discussion

Our post annealing data is limited to measurements done above 300 K as no significant changes were noted for thermal treatment below 300 K. Fig. 1 shows the semi-logarithmic plot of the forward bias *I–V* characteristics of the Au/n-GaAs diodes obtained in the 80–480 K range in the annealing mode. The diodes are rectifying throughout the temperature range indicating good thermal stability. The data in Fig. 1 was fitted satisfactorily in the linear regions of the curves using the pure thermionic emission model. No well-defined linear region is observed in the 400–480 K curves. These results differ with the post annealing mode forward bias characteristics which were all fitted satisfactorily using the thermionic emission theory up to 480 K.

For pure thermionic emission, and for $(V>3kT/q)$ the relationship between the current I and the applied bias voltage V is given by:

$$I = AA^*T^2 exp\left(-\frac{q\phi_0}{kT}\right)\left[exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

where q is the electronic charge, k the Boltzmann constant, T the absolute temperature, R_s the series resistance, ϕ_0 $(=\phi_{IV})$ the zero-bias barrier height, A the diode area and A^* $(=8.16$ A cm^{-2} K$^{-2})$ is the Richardson's constant. The prefactor of the second exponential in Eq. (1) is the reverse saturation leakage current, I_S. The ideality factor n is given by [23]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (2)$$

n is a measure of adherence to the pure thermionic emission theory as it reflects barrier deformation under bias [11]. The zero bias barrier height, (ϕ_0) is obtained from the reverse saturation leakage current (I_S):

$$\phi_0 = \frac{kT}{q}\ln\frac{AA^*T^2}{I_s} \quad (3)$$

A plot of variation of n and ϕ_0 against temperature during annealing is shown in Fig. 2. ϕ_0 varies from 0.78 eV at 80 K to a maximum of 0.86 eV at 400 K where as n decreases from 1.21 at 80 K to 1.02 at 400 K. This behaviour of the barrier height during annealing is contrary to the negative temperature coefficient for n-GaAs and has been observed by other researchers [7,8,23,24]. The variation of diode characteristics confirms the linear correlation between n and ϕ_0 [25].

In both modes n and ϕ_0 show a strong dependence on temperature. The dependency on temperature of diode *I–V* characteristics has been accounted for as due to several factors, chief amongst them the local non-uniformities of the Schottky barrier. At high temperatures, there are possible inhomogeneities in the interface layer thickness and non-uniformities of the interfacial charges [26]. Other authors have attributed these to changes in

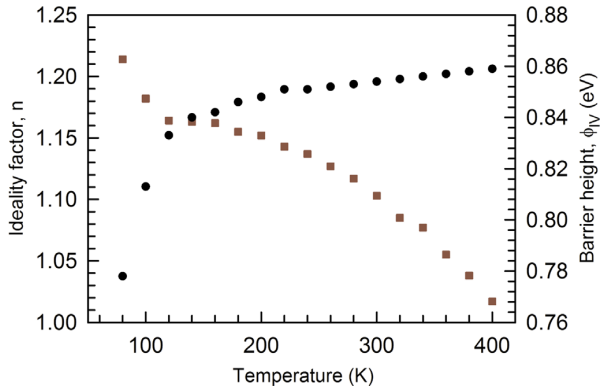

Fig. 2. *I–V* barrier height, ϕ_{IV} and ideality factor, n versus temperature for Au/n-GaAs Schottky diodes during annealing.

carrier transport mechanisms that is recombination-generation in the space charge region and tunnelling in the barrier [10,27,28]. The variation of ϕ_0 with temperature has also been linked to changes in the band gap [14].

Post annealing, n varies from 1.10 after 300 K to 1.14 after 480 K and ϕ_0 decreases from 0.85 eV to 0.79 eV in the same temperature range. Fig. 3 is a comparison between n during annealing and post annealing modes in the 300–400 K range. At room temperature, an almost ideal behaviour is observed. We observe that whilst the ideality factor during annealing has an increasing trend, in the post annealing mode, it has a decreasing trend with increase in temperature. A similar increase in barrier height with temperature in the post annealing mode has been observed in Au/n-Si Schottky diodes and was explained in terms of metallic-like phases produced on the interface because of the annealing process [22]. This change in post annealing characteristics is of a low order of magnitude as shown in Fig. 3 by a nominally flat post annealing curve. However, the change may be due to degradation of diode characteristics since the ideality factor is increasing. Whilst the measurements during annealing show an improvement in the diode's characteristics, post annealing measurements show that the diodes become poorer with increasing annealing temperatures above 400 K.

According to the Schottky-Mott theory, depletion layer capacitance can be expressed as [29]:

$$C^{-2} = \frac{2(V_{bi} - V_A)}{q\varepsilon_S A^2 N_D} \tag{4}$$

where, A is the diode area, V_{bi} the diffusion potential at zero bias obtained from the extrapolation of the linear C^{-2}–V plot to the V axis; and, V_A is the applied voltage. The capacitance of a Schottky diode is characterised by the width of the depletion layer [30]. The intercept on the voltage axis gives the diffusion potential V_{bi} which is used to determine the barrier height [24]:

$$\phi_{CV} = V_{bi} + V_0 \tag{5}$$

where V_0 is the potential difference between the conduction band minima and the Fermi level in the neutral part of the semiconductor [31], and is given by:

$$V_0 = kT \ln\left(\frac{N_C}{N_D}\right) \tag{6}$$

where N_C is density of states in the conduction band and N_D the free carrier concentration obtained from the gradient of the C^{-2}–V plots. From our results, all the C^{-2}–V plots were straight lines. ϕ_{CV} is observed to be higher than the ϕ_{IV} in all cases at all temperatures. Werner and Güttler [32] ascertained that spatial variations in the barriers cause current to flow preferentially through band minima causing I–V barrier height to be lower. The disparity can also be a result of the existence of "excess" capacitance [12].

The values of ϕ_{CV} during annealing show a general decrease across the 80–480 K range. This temperature dependence has been explained using the potential fluctuations model [32] as due to Schottky barrier height inhomogeneities. Fig. 4 shows a comparison of ϕ_{CV} post and during annealing. The post annealing values are overall lower, at all temperatures. The observed ϕ_{CV} trend during annealing shows a change in the temperature slope around 400 K. We fitted the C–V barrier height curve into two linear regions as shown in Fig. 5. The 300–400 K and 400–480 K regions yield equations of the form [24]: $\phi b_{(T1-T2)} = \phi(T = 0) + \alpha T$ were α is the temperature coefficient in the given temperature range $T1$–$T2$. The linear fitting results in two equations:

$$\phi_{b_{300-400\,K}} = -2.19 \times 10^{-4} T + 1.06 \text{ eV} \tag{7}$$

$$\phi_{b_{400-480\,K}} = -6.90 \times 10^{-4} T + 1.25 \text{ eV} \tag{8}$$

We propose that the sharp increase in carrier concentration within the 340–400 K range, as shown in Fig.5, could be explained by the EL2 defect which we observed using L-DLTS measurements. The EL2 deep donor as shown in Fig. 6(inset) is located at an

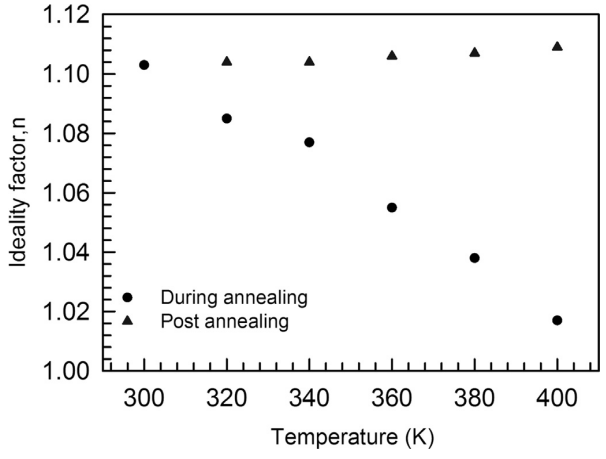

Fig. 3. Plots of ideality factor, n versus temperature during and post annealing.

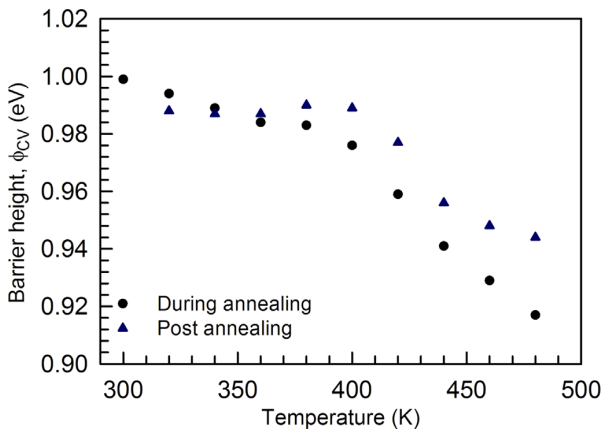

Fig. 4. Plots of C–V barrier height, ϕ_{CV} versus temperature during and post annealing.

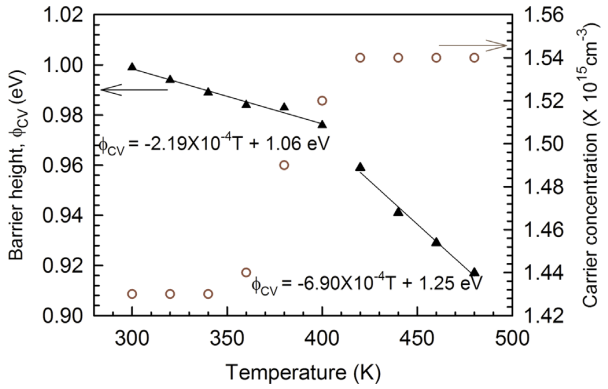

Fig. 5. Free carrier concentration and *C–V* barrier height, ϕ_{CV} versus temperature during annealing.

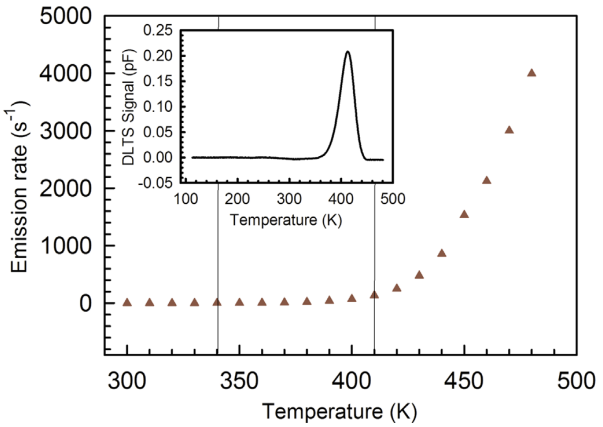

Fig. 6. Emission rate of the EL2 defect as a function of temperature. Inset: DLTS signal for as deposited diodes measured at a reverse bias of −2 V, a filling pulse V_p =0 V and at a rate window of 80 s^{-1}.

energy level of 0.83 eV below the conduction band minima and has an apparent capture cross section of 2.410^{-13} cm^2.

The atomistic origin of this defect has been a subject of controversy for several decades but it is widely believed to involve an arsenic antisite [33]. Fig. 6 shows the emission rate of the EL2 as a function of temperature. The graph is divided into three grid sections. In the 300–340 K temperature range there is not enough energy to release free carriers from the traps, the carrier concentration (Fig. 5) remains nominally constant and it is consistent with the emission rate (Fig. 6) in the same temperature range which is relatively flat. The increasing annealing temperature in the 340–400 K range causes the EL2 to release trapped charges, thus increasing the free carrier density (Fig. 5) [24].There is a correlation with the increase in the emission rate of the EL2 in the same temperature range. This is also supported by the nominally flat post-annealing ϕ_{CV} and that during annealing, the ϕ_{CV} is characterised by a low temperature coefficient below 400 K. Since the ϕ_{CV} is determined from the charge balance details between the metal, the interface and the semiconductor, it will change to maintain this balance [17].

Above 400 K however, there is modification of the *C–V* Schottky barrier. The post annealing ϕ_{CV} is no longer flat, that is, it returns a "new" barrier height for each annealing. The barriers in both modes are now characterised by new temperature coefficients. This, we attribute to interfacial reactions at the interface between the gold and GaAs. Above 400 K, carrier concentration saturates, the reason being that the traps have released all the trapped free carriers owing to the higher emission rate shown in Fig. 6.

However for the post-annealing mode, the carrier concentration saturates at a value lower than that for the annealing mode. The reasons for this are the subject of our current investigations. Besides the EL2, no other electrically active defects were observed by DLTS in the as received samples.

4. Conclusion

We have investigated the *I–V* and *C–V* characteristics of Au/n-GaAs Schottky diodes in the 80–480 K range. The ideality factor and ϕ_{IV} both modify permanently during annealing above 400 K. The post annealing results also show that diodes exposed to higher temperatures modify permanently. *C–V* measurements show a general decrease in ϕ_{CV} both during and post annealing. Our results suggest that exposure of the Au/n-GaAs Schottky barrier diodes to high temperatures above 400 K lead to their physical modification. We also observed an abrupt rise in the free carrier concentration about 340–400 K which we attributed to the emissions of trapped charges by the EL2 defect.

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Paper II

The fine structure of electron irradiation induced EL2-like defects in *n*-GaAs

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The fine structure of electron irradiation induced EL2-like defects in *n*-GaAs

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Defects induced by electron irradiation in n-GaAs have been studied using deep level transient spectroscopy (DLTS) and Laplace DLTS (L-DLTS). The $E_{0.83}$ (EL2) is the only defect observed prior to irradiation. Ru/*n*-GaAs Schottky diodes were irradiated with high energy electrons from a Sr-90 radionuclide up to a fluence of 2.45×10^{13} cm^{-2}. The prominent electron irradiation induced defects $E_{0.04}$, $E_{0.14}$ and $E_{0.38}$ and $E_{0.63}$ were observed together with the metastable $E_{0.17}$. Using L-DLTS, we observed the fine structure of a broad base EL2-like defect peak. This was found to be made up of the $E_{0.75,}$ $E_{0.83}$ and $E_{0.85}$ defects. Our study reveals that high energy electron irradiation increases the concentration of the $E_{0.83}$ defect and introduces a family of defects with electronic properties similar to those of the EL2.

INTRODUCTION

Defect engineering has enabled the development of optimized semiconductor material structures. In some semiconductor materials, point defect engineering has improved device performance and suppressed undesirable properties.[1,2] Particle irradiation induced defects modify the electronic properties of semiconductors.[3] These modifications lead to applications such as carrier lifetime control and device isolation.[4] Understanding the physical properties and occurrence of defects will potentially lead to improved device designs.

In the past, studies have been carried out to gain insight into defects induced by particle irradiation on GaAs devices.[5,6] Such information is vital considering the wide range of optoelectronic applications of these devices under various conditions. An example of such an application is the use of GaAs solar cells in space where they are exposed to highly energetic radiation particles.[7] Moreover in developing future technologies, for both natural and harsh radiation environments, it is crucial to have a clear view of potential radiation problems.

The EL2 defect is very important in GaAs because it affects the optical properties and controls the performance of GaAs based devices.[8,9] In some instances, the defect traps electrons when they are accelerated into semi insulating regions and may create regions of fixed trap charge that can ruin devices.[10] On the other hand it can be deliberately introduced to increase resistivity of bulk so as to lower substrate capacitance and allow high frequency operation of devices. It is arguably the most studied defect in semiconductor physics, with a lot of controversy among researchers for many years, concerning its properties and microscopic structure.[11-14]

All the microscopic models that exist are only coherent in that the properties of the EL2 are As antisite related.[15] An alternate viewpoint proposes oxygen related centers.[16] It has also been postulated that there exists a whole family of midgap levels so called the "EL2 family".

The limitation in most of these studies was the low resolution of conventional DLTS. DLTS is a systematic technique for studying defects in semiconductors which displays emission data spectroscopically as a function of temperature.[17] Conventional DLTS is unable to distinguish the fine structure of closely spaced defects, that is, defects with similar emission rates, which are shown as single, broad based peaks.[18] As a result, most reports on induced defects in n-GaAs have not reported on the fine structure of the defects. L-DLTS provides a solution by offering a higher resolution than the standard DLTS method of up to an order of magnitude.[18,19] Dobaczewski *et.al* [20] were the first to use L-DLTS to study the EL2 in GaAs. They did a comparative study of five liquid encapsulated Czokralski (LEC) grown GaAs crystals from different sources and they observed a defect family of at least two peaks in each sample.

This work adds on to this body of knowledge, by considering MOVPE grown n-GaAs. We have investigated the defects introduced in Ru/*n*-GaAs Schottky barrier diodes by electron irradiation using DLTS. Using L-DLTS, we explored the fine structure and annealing behavior of these defects in detail for the first time. The results show two EL2-like mid-gap energy levels. In the nomenclature used in this article we shall refer to them as radiation induced (RI) EL2-like defects. This is an important result especially considering the interest in defect engineering using the EL2[10] and recent progress in growth of cheaper GaAs which is going to be highly influenced by the presence of defects in the material.[21]

EXPERIMENTAL PROCEDURE

Si doped *n*-GaAs (1 0 0) epitaxial layers (5µm) grown by OMVPE on n^+ GaAs substrates were used in this study. The average free carrier density was 1.0×10^{15} cm^{-3} as specified by the suppliers (Spire Corporation). Firstly, samples were degreased and etched chemically. A Au:Ge (88%:12%) eutectic was resistively deposited on the n^+ sides to form an ohmic contact, with a Au overlayer followed by a 2 min anneal in Ar at 450 ℃. Thereafter 1000 Å thick Ru contacts, 0.6 mm in diameter, were deposited on the epitaxial layer using electron beam evaporation. Contact quality was evaluated using current-voltage (*I-V)* and capacitance-voltage (*C-V)* measurements.

The devices were then irradiated with MeV electrons for 5 hours up to a dose of 2.45×10^{13} cm^{-2} from an Sr-90 radionuclide. A detailed graphical representation of the energy distribution of electrons emitted by the radionuclide is given by Auret *et al*.[22] The carrier concentration of the samples after irradiation was monitored

through *C-V* measurements in order to see whether the accuracy of the DLTS measurements was not being compromised by a high radiation dose through carrier removal. DLTS spectra were recorded at a scan rate of 2 K/min in the 15–390 K temperature range, at a quiescent reverse bias (V_R) of –2 V, filling pulse amplitude (V_p) – 0.2 V and filling pulse width (t_p) 1 ms. The defects observed from the scans were characterized using L-DLTS.[20] Forward bias filling pulse was set at –0.2 V in order to avoid the capacitance signal from surface states. Surface states are sometimes confused with, or prevent, the detection of deep levels in the bulk of the material.[23,24]

The signatures (energy level in the band gap (E_t), and apparent capture cross section (σ_n)) of the induced defects were calculated using log (e_n/T^2) versus (1000/T) Arrhenius plots, from the slope and y-intercept, respectively according to the equation[18]

$$e_n = \sigma_n \langle v_{th} \rangle \frac{g_o}{g_1} N_c \exp\left(-\frac{E_c - E_t}{k_B T}\right) \qquad \mathbf{1}$$

Equation 1 gives the emission rate as a function of temperature T, where $\langle v_{th} \rangle$ is the thermal velocity of electrons, (E_c – E_t) is the activation energy, N_c is the density of conduction band states, g_0 and g_1 are the degeneracy terms referring to the states before and after electron emission and k_B is the Boltzmann constant. Capture cross section is assumed to have a T^2 dependency, hence the log(e_n/T^2) versus 1000/T plots. The true capture cross section of some of the defects was then obtained using the pulse width method which is described briefly in part B of the next section. In-order to investigate the thermal stability of the defects, the samples were annealed in the 0-300 ℃ range with incremental steps of 50 ℃.

RESULTS AND DISCUSSION

A. Electron irradiation induced defects

Irradiation induced defects emanate from collisions of energetic particles which result in elastic scattering. A Frenkel pairs is created when a particle imparts energy to a lattice atom to displace it forming a vacancy-interstitial pair. Mobile vacancies and interstitials are also introduced through the same mechanism. Electron irradiation results in the formation of simple point defects only. This can be ascribed to the relatively low mass of the electron compared to that of the recoiling nucleus rendering the nucleus incapable of imparting energy for further displacements. At room temperature the threshold displacement energy in GaAs has been observed to be approximately 9.0 eV for Ga and approximately 9.4 eV for As.[25]

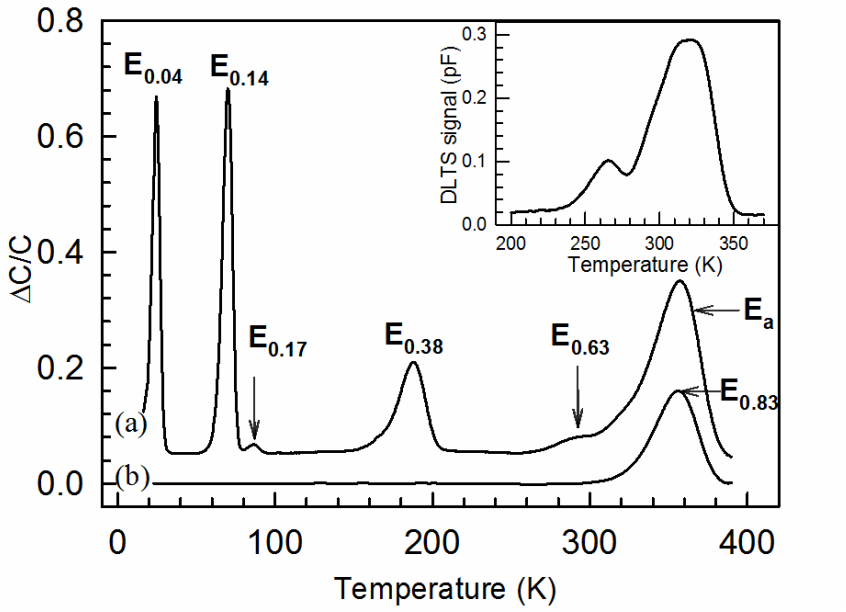

FIG. 1. DLTS spectra of (a) as deposited samples (b) MeV electron irradiated samples recorded at a quiescent reverse bias (V_R) of –2 V at a rate window of 4 Hz, filling pulse (V_p) of –0.2 V and pulse width (t_p) of 1 ms. E_a is a compound peak of three defects. Inset : Broad peaks observed after radiation exposure for 24 hours

Figure 1 depicts the results of the DLTS scans obtained at a rate window of 4 Hz. Curve (a) is the control spectrum obtained from the as-deposited samples before irradiation. It shows only the native ($E_{0.83}$) defect present which is also well known as the EL2 defect. Similarly, the 0.83 eV energy level has been observed in GaAs (as-grown) samples by other researchers and in GaAs based structures grown through molecular beam epitaxy and LEC.[17,26-28] The EL2 defect can exist in two different atomic configurations, a normal configuration and a metastable one. The metastable configuration is attainable by photoquenching at low temperatures in which all the optical, magnetic and electrical properties disappear.[29]

Dobaczewski *et.al* [17] reported the presence of four energy levels associated with the EL2 in LEC as-grown samples measured by L-DLTS. In our as grown samples only the $E_{0.83}$ was observed in a measurable concentration before irradiation. The presence of As antisite related defects in GaAs is highly dependent on the growth conditions namely, growth rate, stoichiometry and temperature.[30,31] Curve (b) reveals emission peaks from defects induced by electron irradiation into the GaAs. The peaks have been labeled $E_{0.04}$, $E_{0.14}$, $E_{0.17}$, $E_{0.38}$, and $E_{0.63}$ based on their energy levels. Additionally, a compound broad based peak has been labeled E_a.

A metastable defect that has been reported on, in the same temperature range, superimposed on the $E_{0.38}$ peak was not observed in our scans.[32] This is because its presence and magnitude is highly dependent on the bias conditions, temperature-cycling and incident particle type. The $E_{0.04}$, $E_{0.14}$ and $E_{0.38}$ defects have the same electronic structure and are point defect in nature. They are termed *primary electron irradiation induced defects* as they are observable with the same signatures after being induced by different radiation types.[33] The defects $E_{0.04}$ and $E_{0.14}$ are unsimilar charge states of the isolated As vacancy. Also, the $E_{0.38}$ has been attributed to close As vacancy-interstitial pairs.[34] The $E_{0.17}$ defect is metastable and can be reversibly transformed by introducing zero and reverse bias anneals.[35] Lastly, the $E_{0.63}$ can only be observed at relatively high radiation fluencies which implies that it might be a complex defect.

B. The fine structure of the radiation induced EL2-like defects

Using L-DLTS we were able to resolve the fine structure of the broad peak labeled E_a in Figure 1. As a result three unique energy levels were identified which are displayed in Figure 2 as $E_{0.75}$, $E_{0.83}$ and $E_{0.85}$, respectively. The $E_{0.63}$ already appears on the DLTS spectrum (b) in Figure 1.

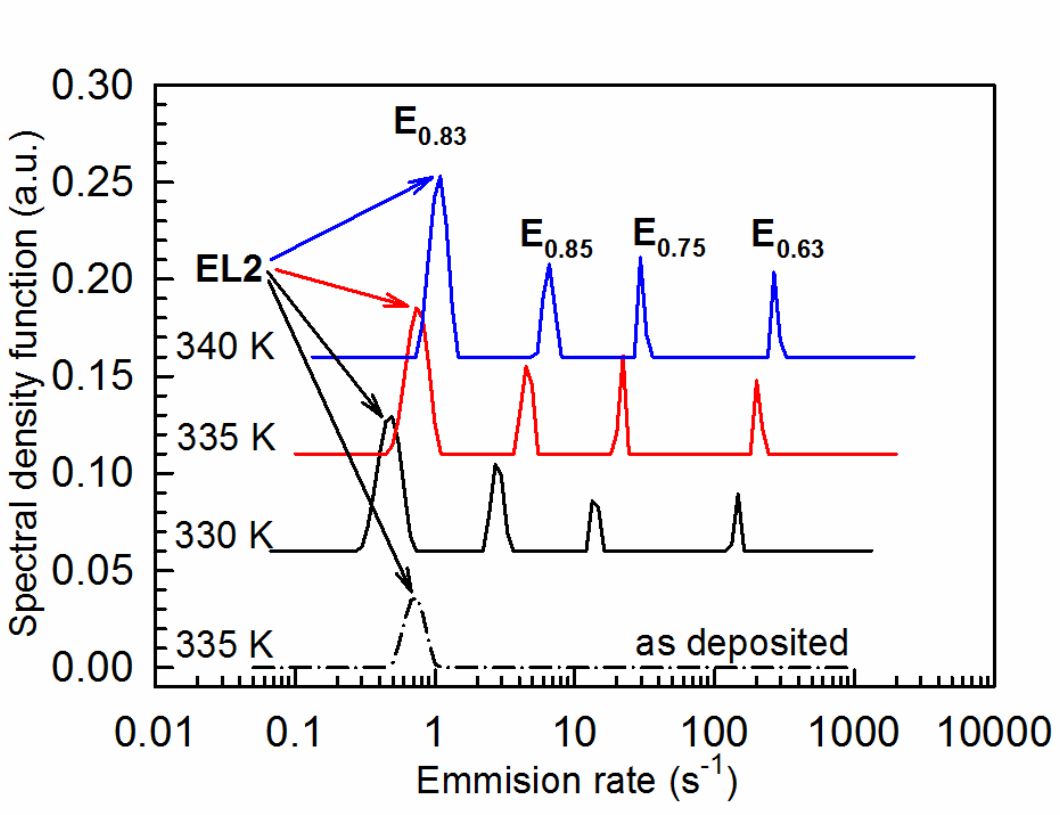

FIG. 2. Laplace DLTS spectra showing the EL2 and radiation induced EL2-like defects in MOVPE grown *n*-GaAs and the reference spectrum.

By varying pulse width and observing the spectral response, we confirmed that we were probing different and unique energy states. The Arrhenius plots of the three energy levels with the $E_{0.63}$ are shown in Figure 3.

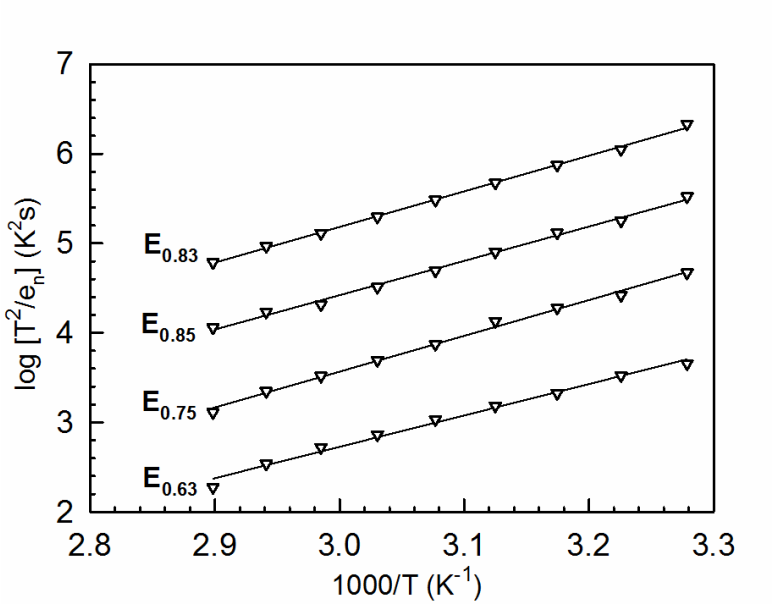

FIG. 3. Arrhenius plots for the EL2 and EL2-like electron irradiation induced defects

Several authors have reported on the existence of least two midgap energy levels in n-GaAs. Dobaczewski *et al* [17]reported four energy levels similar to Figure 2 in LEC (as-grown) samples using Laplace DLTS. Saxena *et al* [36] observed the 0.76 eV and 0.83 eV energy levels using capacitance-voltage-time measurements. Furthermore similar energy levels to those found in our experiments have been reported on by other researchers. The 0.75 eV has been observed in InAs quantum dots embedded in a GaAs matrix using L-DLTS [27] and the 0.85 eV energy level was predicted by Li *et al,* [37] using density functional theory (DFT) calculations on supercells of 64 atoms. Hall Effect measurements on the EL2 have determined the energy range to be in the 0.72 eV to 0.80 eV range.[38] However Bourgoin *et al* [38] gave a detailed account on why Hall measurement results cannot reliably measure the energy level of the EL2. A discrepancy is noted between the 0.83 eV and the 0.85 eV energy levels on the Arrhenius plots in Figure 3. Equation 1 dictates that the 0.85 eV energy level must be observed at a temperature above the 0.83 eV energy level contrary to what is displayed in figure 2. We speculate that this is a result of the measurement of a dominant signal from the 0.83

eV energy level that perturbs the signal from a defect with an almost similar activation energy. Lagowski *et al* [39] observed an oxygen related deep level with an energy almost identical to that of an As antisite using controlled oxygen doping. They concluded that the dominant energy level of the EL2 impedes the identification of the other energy level by DLTS measurements. However Subramanian *et al* [40] had earlier argued that the 0.83 eV energy level cannot be associated with oxygen but proposed that it is related to another impurity. We can therefore not directly conclude that our results are a direct result of an oxygen related trap. Arrhenius plots of all the defects identified in this study are shown in Figure 4.

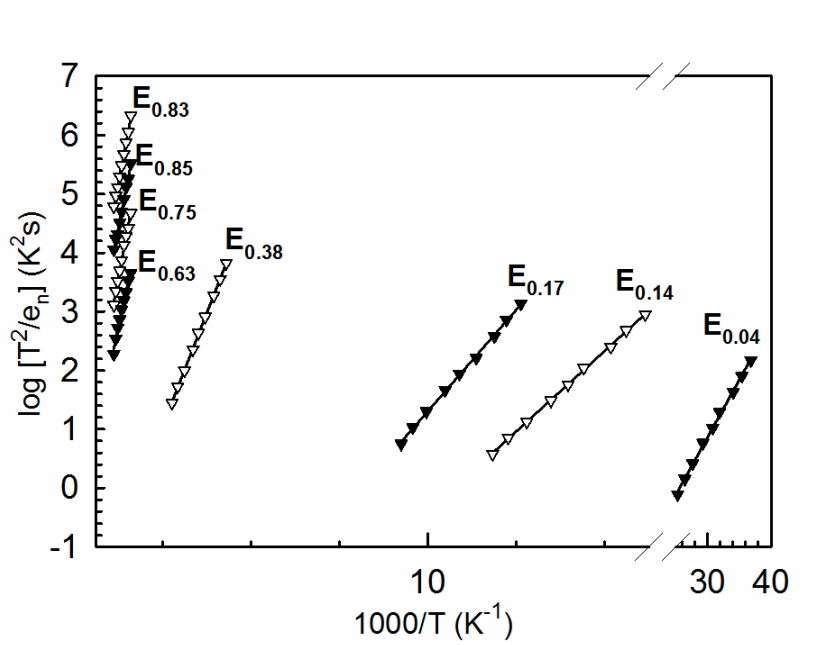

FIG. 4. Arrhenius plots for defects introduced by MeV electrons in MOVPE grown *n*-GaAs

The resulting defect 'signatures' are summarized in Table 1. Apparent capture cross section calculations obtained directly from Equation 1 have been shown in the past to be erroneous since in some instances, they do not account for temperature and electric field dependencies.[41]

TABLE I. Electronic properties of defects in MeV electron irradiated, MOVPE grown *n*-GaAs at V_R = –2.0 V, V_P = –0.2 V and t_p = 1 ms.

Defect label	E_t (meV)	σ_n (cm^{-2})
$E_{0.04}$	38.7	1.6×10^{-17}
$E_{0.14}$	135	3.0×10^{-15}
$E_{0.17}$	171	3.4×10^{-13}
$E_{0.38}$	382	7.4×10^{-16}
$E_{0.63}$	634	1.0×10^{-15}
$E_{0.75}$	749	5.2×10^{-15}
$E_{0.83}$ (EL2)	833	2.8×10^{-15}
$E_{0.85}$	852	3.4×10^{-14}

Accurate capture cross section values can be obtained by using the filling pulse a technique which is highly demanding in terms of instrumentation.[42] In principle trap filling will proceed exponentially with a time constant given by the equation[43]

$$\tau_c = \frac{1}{\sigma_n v_{th} n} \qquad \mathbf{2}$$

were n is the free carrier concentration at the measurement temperature. By monitoring the peak of the DLTS signal as a function of filling pulse as shown in Figure 5 we determined τ_c from the slopes of the semi-logarithmic graphs.

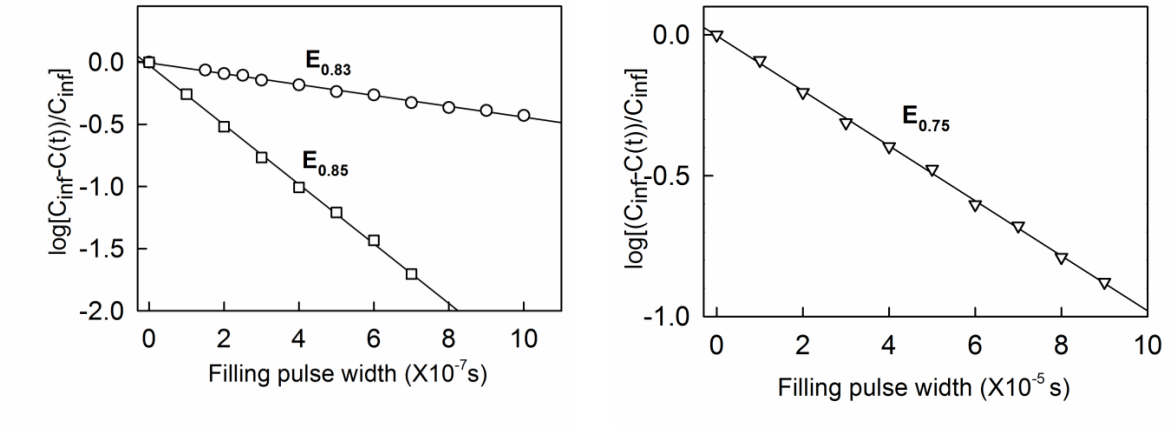

FIG. 5. Determination of accurate capture cross section of the EL2 radiation induced EL2-like defects using the pulse width method at 320K.

The results are displayed in Table 2 showing an almost similar σ_n for the $E_{0.83}$ and $E_{0.85}$ and a lower value by almost two orders of magnitude for the $E_{0.75}$.

TABLE II. Values of the capture time constant (τ) and capture cross section (σ_n) for defects in the EL2-like defects obtained using the pulse width method at 320 K.

Defect label	τ(s)	σ_n(cm^{-2})
$E_{0.75}$	4.2×10^{-7}	5.5×10^{-15}
$E_{0.83}$ (EL2)	2.3×10^{-6}	1.0×10^{-15}
$E_{0.85}$	1.0×10^{-4}	2.3×10^{-17}

Spatial distribution of the electron irradiation induced defects in GaAs was obtained using the fixed bias, variable pulse method.[44] Profiling of the depth distribution of the defects was done at a constant reverse bias of -5 V. Additionally, a comparison was done between the concentration depth of the $E_{0.83}$ before and after irradiation as displayed in Figure 6.

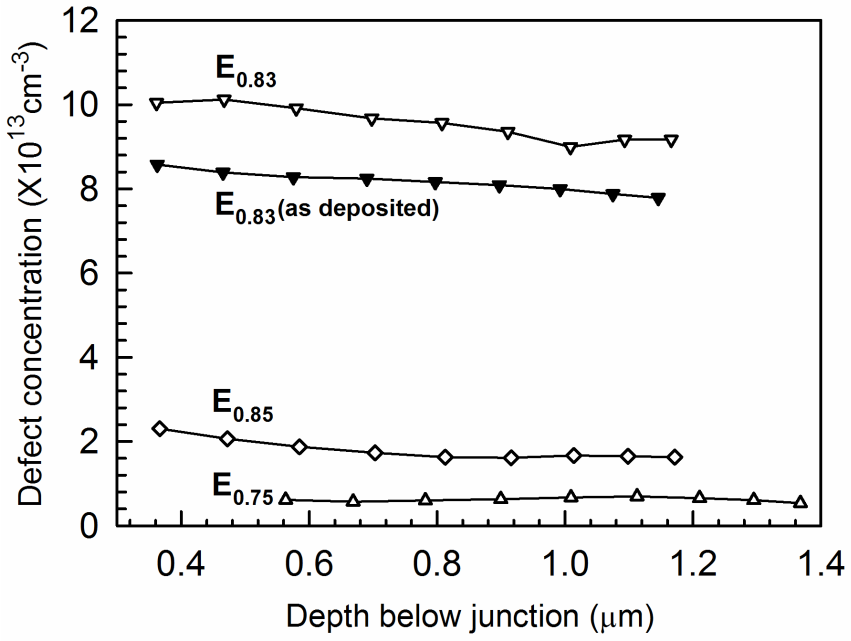

FIG. 6. Depth and concentration of the defects introduced by MeV electrons in Ru/*n*-GaAs Schottky diodes compared to as deposited (unirradiated) samples.

The defect concentration of the $E_{0.38}$ shows a general decrease deeper into the bulk. A comparison of its depth profiles before and after irradiation shows an increase in the defect concentration of close to an order of magnitude as a result of the electron irradiation. Depth profiles of the $E_{0.85}$, $E_{0.75}$ defects are similar and flat. The $E_{0.83}$ is at a higher concentration than the rest of the defects, explaining why it is the one most likely to be detected by DLTS measurements. Concentrations of these defects are consistent with the 10^{16} to 10^{13} cm^{-3} range that was reported for EL2 defects by other researchers in VPE grown n-GaAs.[45]

C. Annealing of the EL2-like radiation-induced defects

In our previous study we investigated the effect of dynamic annealing on the electrical characteristics of Au/n-GaAs Schottky barrier diodes[46]. We attributed an inconsistency in the behavioral trend of the *C-V* barrier height to the EL2 defect. Figure 7 shows the results of our measurements on the thermal stability of the radiation induced EL2-like defects on Ru/n-GaAs Schottky barrier diodes.

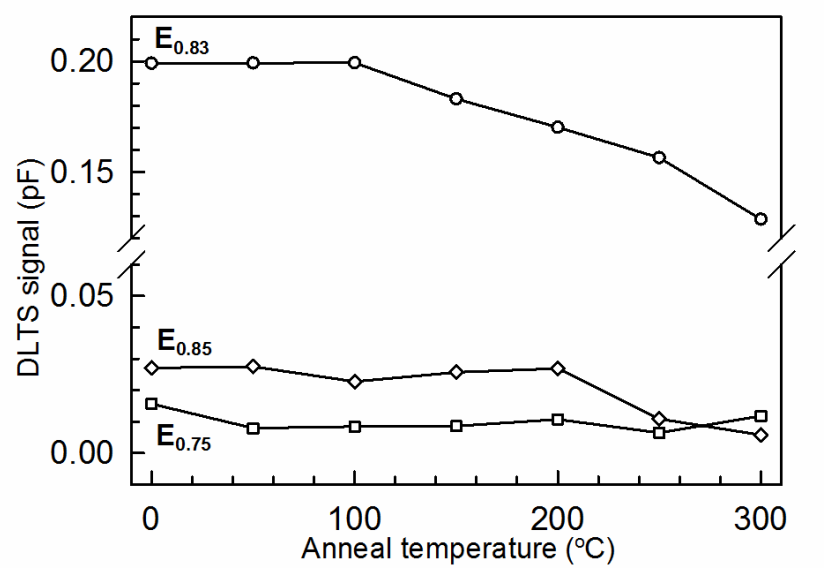

FIG. 7. Isochronal annealing (5 min periods) of the EL2 and radiation induced EL2-like defects in *n*-GaAs

It was only after annealing at 100 °C was there a notable decrease in the concentration of the $E_{0.83}$. Its overall reduction in concentration after annealing at 300 °C was 65%, whereas that for the $E_{0.85}$ was 21% when compared to unannealed samples. An inconsistent trend was observed for the $E_{0.75}$ throughout the annealing steps. The overall difference in behavior during annealing suggests that all radiation induced EL2-like defects might be of different species. Also the annealing behavior of the EL2 in this case suggests carrier removal which is consistent with our findings in reference 45.

CONCLUSIONS

Ru Schottky barrier diodes were fabricated on *n*-type GaAs. DLTS measurements were carried out before and after high energy electron irradiation. The $E_{0.04}$, $E_{0.14}$, $E_{0.17}$, $E_{0.38}$, $E_{0.63}$, $E_{0.75}$, and $E_{0.85}$ defects were detected after irradiation. Irradiation increased the defect concentration of the native $E_{0.83}$ defect found in as deposited samples. Performing L-DLTS on the broad EL2-like peak revealed the $E_{0.75}$, $E_{0.85}$ and $E_{0.83}$ defects. Using the pulse width method the accurate capture cross section of the EL2 and EL2-like defects was measured. The true capture cross sections for the $E_{0.83}$ and $E_{0.85}$ were observed to be almost similar and greater than that of the $E_{0.75}$ by almost two orders of magnitude. Depth profiling was also done using the fixed bias variable pulse method, which showed the higher concentration of the $E_{0.83}$ compared to all the observed defects. Annealing within the 0 – 300 °C range did not introduce any new defects but lead to the general decrease in concentration

of the $E_{0.85}$, $E_{0.83}$ and $E_{0.75}$. We can conclude that in addition to vacancies and interstitials high energy electron irradiation also induces midgap electron traps with electronic properties similar to the EL2 defects in n-GaAs.

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Paper III

Electrical characterization of 5.4 MeV alpha-particle irradiated; low doped, *n*-type gallium arsenide

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Electrical characterisation of 5.4 MeV alpha-particle irradiated; low doped, n-type gallium arsenide

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Abstract. We have investigated the effects of alpha particle irradiation on the electrical characteristics of Au/n-GaAs Schottky diodes The diodes were irradiated with an Am-241 alpha-particle source up to a fluence of 2.6×10^{10} cm^{-2} at room temperature. The induced defects were studied using deep level transient spectroscopy (DLTS) in the 15-300 K range and revealed the defects $E_{0.04}$, $E_{0.14}$, $E_{0.17}$ and $E_{0.38}$. The current-voltage *(I-V)* characteristics remain largely unchanged after irradiation, whilst capacitance-voltage (*C-V)* characteristics showed a decrease in net doping density.

1. Introduction

Defect engineering has enabled the development of optimized semiconductor material structures. Understanding the physical properties and occurrence of defects will potentially lead to optimal device design. Particle irradiation induced defects modify the electronic properties of semiconductors [1, 2]. These modifications lead to applications such as carrier lifetime control and device isolation [3] .

GaAs based devices have been used in space applications, where they are exposed to irradiation from highly energetic particles. The importance of information; on the influence of radiation on the electrical characteristics of these devices can therefore not be overemphasized. In the past studies have been carried out to in order to gain insight on the effects of particle irradiation on GaAs devices [3-7]. In this study we have investigated the defects introduced in Au-n/GaAs Schottky barrier diodes by alpha particle irradiation using DLTS. This study was limited to only low doped GaAs. DLTS is a convenient and powerful technique for studying defects in semiconductor materials [7].

2. Experimental details

(MOVPE) grown,silicon doped *n*-GaAs with an average free carrier density of 1.0×10^{15} cm^{-3} and <100> orientation, supplied by Spire Corporation, was used. The wafers were degreased and etched chemically. Au-Ge (88%:12%) ohmic contacts were resistively deposited on the n^{+}- backsides of the samples. Thereafter 1000 Å thick Au contacts, 0.6 mm in diameter, were resistively deposited on the epitaxial layer. Contact quality was evaluated using *I-V* and *C-V* measurements.

The samples were irradiated with 5.4 MeV He ions (α-particles) from an Am-241 radionuclide for 20 min to a dose of 2.56×10^{10} cm^{-2}. DLTS spectra were recorded at a scan rate of 3 K/min in the 15–300 K temperature range. The quiescent reverse bias was –2 V, filling pulse amplitude -0.5 V and filling pulse width 1 ms.

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The DLTS defect signature (energy level in the band gap, E_t and apparent capture cross section, σ) were determined from the slope and y-intercept, respectively, of log (e_n/T^2) versus (1000/T) Arrhenius plots.

3. Results and discussion

The parameters deduced from the *I-V* and the *C-V* measurements of the Schottky diodes before and after irradiation are shown in Table 1. The *I-V* characteristics do not show any changes in ideality factor and barrier height after particle irradiation. However, the *C-V* characteristics show a decrease in the net doping density. This decrease has been explained as due to the traps introduced by the irradiation, trapping carriers [4].

Table 1. Schottky diode *I-V* and *C-V* parameters obtained from the Schottky diode before and after α-particle irradiation.

	Ideality factor	Barrier height (eV)	Nd ($\times 10^{14}$ cm^{-3})
As deposited	1.02	0.89	7.64
5.4 MeV irradiated	1.02	0.89	6.68

Figure 1 depicts the DLTS scans obtained at a frequency of 200 Hz. Curve (a) is the control spectrum obtained from the as-deposited samples before irradiation. It shows no defects present in measurable quantities in the 15-300 K temperature range. Curve (b) reveals emission peaks from defects induced by α-particle irradiation superimposed on a "skewed baseline'. The peaks are labelled $E_{0.04}$, $E_{0.14}$, $E_{0.17}$ and $E_{0.38}$ in.

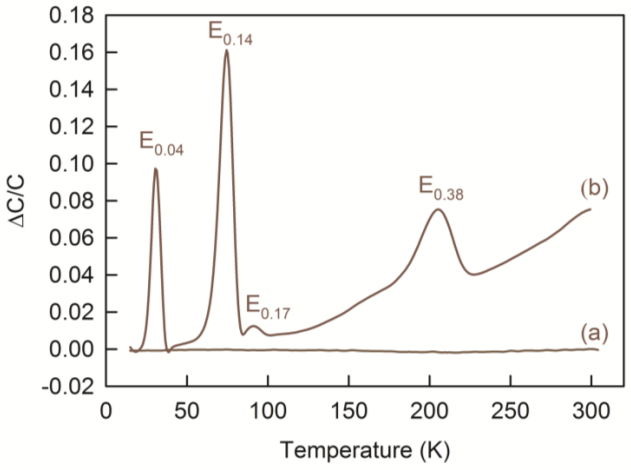

Figure 1. (a) DLTS spectra of un-irradiated (b) 5.4MeV alpha particle irradiated samples recorded at a quiescent reverse bias of 2 V at a rate window of 200 Hz and filling pulse 0 V and pulse width 1 ms.

A metastable defect that has been observed by other researchers was not observed in our scans [8]. This is because its presence and magnitude is highly dependent on the bias conditions, temperature and incident particle type [4]. The "skewed baseline' in curve (b) has been observed only in α-particle irradiated gallium arsenide but not in other semiconductor materials exposed to the same type of

radiation. It can therefore not be explained in terms of ion-solid interactions. A similar baseline was observed by Janse van Rensburg *et al* [9]in europium and xenon implanted GaN thin fims without conclusion on its causality. The forward bias filling pulse in all the measurements done for the purpose of this study was -0.5 V in order to avoid the capacitance signal from surface states. This is also shows that the baseline is not a consequence of surface states [10]. Surface states are sometimes confused with, or prevent, the detection of the presence of deep levels in the bulk of the material [11].

Irradiation induced defects are a result of collision of energetic particles. The Frenkel pair, is created when a particle imparts energy to a lattice atom to displace it forming a vacancy-interstitial pair [12]. However considering the energy transferred to atoms of the crystal by alpha particles not only point defects, but defects consisting of clusters of atoms displaced from their normal lattice sites can be formed[6]. The Arrhenius plots for the defect characteristics are shown in figure 2, from them defect 'signatures' shown in table 2 were deduced.

The defects $E_{0.04}$, $E_{0.14}$ have been confirmed to be caused by primary defects such as the single and double charge states of the vacancy in the As sub-lattice. It has been proposed that the two are different charge states (o/+) and (+/o) of the isolated vacancy V_{As}-A_{Si} in GaAs. The $E_{0.38}$ is speculated to be related to close As vacancy interstitials[11] .

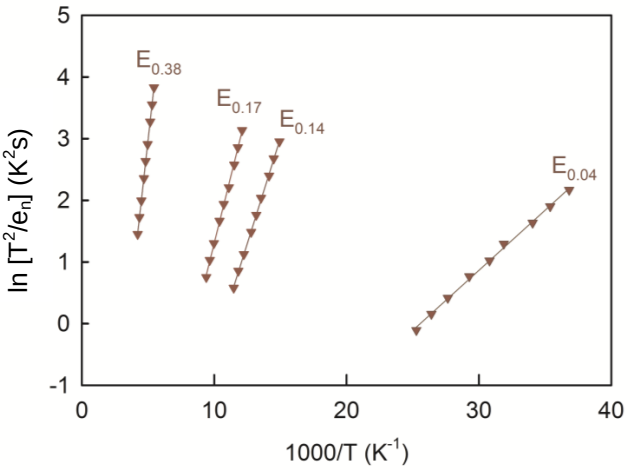

Figure 2. Arrhenius plots of defects observed after alpha particle irradiation

$E_{0.04}$, $E_{0.14}$ and $E_{0.38}$ have the same electronic structure and are point defect in nature as they are observable with the same signatures after being induced by different radiation types [10] .The charge state of the $E_{0.38}$ is highly field dependent[3]. Further, the defects are dependent on the growth technique and carrier density implying that they emanate from the defects and impurities on the as grown GaAs[10] .Table 2 summarises the defect signatures. The defect characteristics shown in the table corresponds to those that have been observed by other researchers [6].

Table 2 . Characteristics of alpha-particle irradiation induced defects detected by DLTS in OMVPE-grown *n*-GaAs.

Defect label	Activation Enthalpy (meV)	Capture cross section (cm^{-2})
$E_{0.04}$	38.7	1.6×10^{-17}
$E_{0.14}$	135	3.0×10^{-15}
$E_{0.17}$	171	3.4×10^{-13}
$E_{0.38}$	382	7.4×10^{-16}

4. Conclusions

We have used DLTS to study the defects in the 15 -300 K range in α-particle irradiated GaAs. Four defect peaks were observed namely the $E_{0.04}$, $E_{0.14}$, $E_{0.17}$ and $E_{0.38}$ defects which are all point defect in nature. They have been associated with solid-ion interactions. The defects have been previously shown to be related to isolated vacancies and vacancy-interstitial pairs in the As sublattice. The $E_{0.38}$ defect has been observed to be field dependent. The *(I-V)* characteristics remained significantly constant confirming the radiation hardness of GaAs. A decrease in carrier density was observed from the (C-V) characteristics after irradiation. We therefore can conclude that alpha particle irradiation affects the electrical characteristics of *n*-GaAs based devices.

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Chapter 6

Conclusions

6.1 Introduction

The research contained in this dissertation is an excerpt of the investigations done on the electrical characteristics of *n*-GaAs with a focus on the electronic properties of the EL2 defect. It is clear that due to the high resolution of L-DLTS, we were able to look at the fine structure of a compound electron irradiation induced defect which would otherwise be referred to as the EL2. In this chapter conclusions specific to each section are summarized.

6.1.1 *I-V-T* and *C-V-T* measurements

The study showed that the EL2 defect had profound effects on the electrical characteristics of GaAs based devices at high temperatures. The influence of the defect caused a split of the *C-V* barrier height vs temperature results into two temperature intervals, each characterized by a unique temperature coefficient. From the results it was deduced that exposure of Au/*n*-GaAs SBDs to temperatures above 300 K results in the deterioration of their dynamic *I-V* characteristics. Permanent changes to the *C-V* characteristics and carrier concentration were observed above 400 K. It was inferred that exposure of Au/*n*-GaAs SBDs to temperatures above 400 K results in their physical modification.

6.1.2 Process induced defects

EBD and ICP etching were observed to significantly deteriorate the diode *I-V* characteristics. DLTS results after EBE confirmed that sub-threshold energies introduce defects in *n*-GaAs. At such incident particle energy levels the defect formation could not be accounted for by ion-solid interactions. The different signatures of defects formed after EBE, EBD and MeV electron irradiation revealed that different mechanisms were responsible for defect formation in each process. Processing was observed to have an insignificant impact on the electronic properties of the EL2 defect.

6.1.3 Irradiation induced defects

The fine structure of defects introduced by high energy beta particles and alpha particles was studied.The defect concentration of the EL2 was observed to be significantly higher than all the radiation induced defects. The DLTS spectra of alpha-particle irradiation induced defects exhibited peaks sitting on a skewed baseline which hindered accurate L-DLTS measurements. It was concluded that in addition to the prominent irradiation induced defects high energy electron irradiation introduces defects with electronic properties similar to those of the EL2 in GaAs

6.2 Future work

Several defect states were reported within this thesis. However the chemical identity and microscopic structure of most of them remain uncertain due to the limitations of DLTS and L-DLTS. It is therefore necessary to adopt other defect identification techniques like photoluminescence and Hall effect measurements in a bid to understand the nature of these defects.

The irradiation experiments were done at room temperature where the vacancies and interstitials are mobile. A study of the first generation defects has to be carried out. This is achievable by irradiation at very low temperatures. It is also essential to re-look at the fine structure of defects introduced by other incident ion types in *n*-GaAs that were reported in the past using conventional DLTS.

To the best of the author's knowledge, annealing studies involving the observed process induced defects have not been carried out. Such a study will aid in understanding the defect species and the mechanisms of defect formation during EBD which have been under scrutiny for many years. Also, in-order to fully understand the interactions in the vacuum chamber during EBD, mass spectrometry of all the particles in the chamber has to be done.

Finally, all the experimental work that has been carried out can be extended to include *p*-type GaAs, *n*-type GaAs of different free carrier densities and GaAs grown using different techniques like molecular beam epitaxy and liquid encapsulated Czokralski (LEC).

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