Field-effect transistors based on solution processed zinc tin oxide

Feldeffekttransistoren basierend auf flüssigprozessiertem Zink-Zinn-Oxid

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)

genehmigte Dissertation von M.Sc. Reinhold Benedikt Sykora aus Augsburg

Tag der Einreichung: 09.10.2017, Tag der Prüfung: 15.01.2018

Darmstadt — D 17

1. Gutachten: Prof. Dr.-Ing. Heinz von Seggern

2. Gutachten: Prof. Dr.-Ing. Horst Hahn

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Fachbereich Material- und Geowissenschaften

Elektronische Materialeigenschaften

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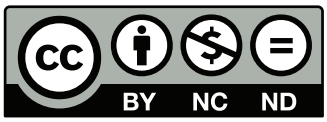

Erklärung zur Dissertation

Hiermit versichere ich, die vorliegende Dissertation ohne Hilfe Dritter nur mit den angegebenen Quellen und Hilfsmitteln angefertigt zu haben. Alle Stellen, die aus Quellen entnommen wurden, sind als solche kenntlich gemacht. Diese Arbeit hat in gleicher oder ähnlicher Form noch keiner Prüfungsbehörde vorgelegen.

Darmstadt, den 09.10.2017

(M.Sc. Reinhold Benedikt Sykora)

Zusammenfassung

Fast alle Transistoren basieren auf anorganischen Halbleitern, wie zum Beispiel Silizium. Trotz dessen vielfälitger Verwendung besitzt es auch einige Nachteile. Erstens muss die kristalline Reinheit sehr hoch sein, um gute Bauteileigenschaften zu erhalten. Um dies erreichen zu können sind teure und aufwändige Herstellungsmethoden nötig. Für spezielle Anwendungen wie zum Beispiel radio-frequency identification (RFID)-Systeme sind dessen hohe Herstellungskosten nicht geeignet. Auf der anderen Seite besitzt Zink-Zinn-Oxid (ZTO), als ein amorpher Metalloxid Halbleiter (AOS), welcher aus der Flüssigphase hergestellt wird, trotz seines amorphen Charakters gute Transistorkennwerte. Im Gegensatz zum umfassend untersuchten Indium-Gallium-Zink-Oxid (IGZO) enthält es nicht das teure Indium.
In dieser Arbeit wurde eine Prekursorenroute entwickelt, die nicht auf dem gängigen, aber giftigen Methylglycol basiert. Als Hauptlösungsmittel diente Ethanol, mit Ethylenglycol als optionalem Zweitlösungsmittel. Mit Hilfe dieser Prekursorlösungen konnten dünne ZTO-Schichten entweder mittels Aufschleudern oder Drucken hergestellt werden. Untersuchungen ergaben, dass die erhaltenen Filme eine geringe Oberflächenrauigkeit haben und hauptsächlich eine amorphe Struktur zeigen, in der Zinkoxid Nanokristallite enthalten sind. Die prozessierten ZTO-Schichten sind transparent und zeigen eine n-Dotierung. Anhand Untersuchungen von Bottom-Gate-Transistoren konnte herausgefunden werden, dass ein Verhältnis von Zink zu Zinn von 7:3 die besten Transistorkennwerte erzielte. Ferner wurde gezeigt, dass ein Ersatz von 40 % Ethanol durch Ethylenglycol die Bauteilkennwerte verbessern konnte und dass Salzsäure, welche als Stabilisator in der Prekursorenlösung dient, Elektronenfallen erzeugen kann. Mit Hilfe eines Multischichtenansatzes von gedruckten ZTO-Schichten war es möglich, die Transistorkennwerte zu verbessern. Die höchste je berichtete Elektronenmobilität von $7.8\,\mathrm{cm^2V^{-1}s^{-1}}$ für gedruckte ZTO-Transistoren wurde bei acht prozessierten Schichten erhalten. Es konnte des weiteren gezeigt werden, dass ein Transistor, der aus mehr als vier ZTO-Schichten aufgebaut ist, eine höhere Widerstandsfähigkeit gegenüber positivem Gate Spannungsstresstest (PBS) und gegenüber Wasser als Elektronendonator und Sauerstoff als Elektronenakzeptor im ZTO-System zeigt. Transistoren, welche mehr als vier ZTO-Schichten besitzen, zeigen gute Kennwerte, obwohl sie bei 350 °C anstatt der Standardeinstellung von 500 °C ausgeheizt wurden. Der Grund für die besseren Transistor-Kennwerte und die höhere Widerstandsfähigkeit gegenüber Gasen in der Atmosphäre mittels Multischichtenansatzes konnte auf eine verbesserte Oberflächenbedeckung und eine höhere Filmqualität zurückgeführt werden. Des weiteren war es möglich einen Aufbau für zeitabhängige Transistormessungen zu realisieren und die ersten Ergebnisse zeigten, dass die schnellsten Einschaltzeiten gemessen werden konnten, wenn der

Transistor im linearen Bereich betrieben wird. Die höchste Schaltfrequenz eines Transistors wurde mit 1.33 MHz gemessen. Es konnte gezeigt werden, dass der Einschaltvorgang anhand von zwei Zeitkonstanten beschrieben werden kann. Es ist anzunehmen, dass die kurze Zeitkonstante den Transport der injezierten Ladungsträger repräsentiert, während die lange Zeitkonstante den Transport der gefangenen Ladungsträger darstellt.

Außerdem konnten funktionale ZTO Top-Gate-Transistoren mit den organischen Dielektrika Polymethylmethacrylat (PMMA), Polystyrol (PS) und ein vernetzbares Copolymer (PAZ) realisiert werden. Es konnte gezeigt werden, dass eine Dicke des Dielektrikums PMMA von mindestens 490 nm nötig ist, um gute Transistor-Kennwerte bei niedrigen Leckströmen zu erhalten. Die besten Top-Gate-Transistoren konnten durch eine veränderte Elektrodenstruktur realisiert werden, die eine Überlappung zwischen Source/Drain und Gate-Elektode reduziert. Der beste gedruckte ZTO Top-Gate Transistor, der diese Elektrodenanordnung in Verbindung mit PMMA benutzt, zeigte eine Elektronenbeweglichkeit von bis zu 4.4 $cm^2V^{-1}s^{-1}$. Dieser Wert ist der höchste je berichtete Wert für einen gedruckten ZTO/PMMA Top-Gate-Transistor. Im Vergleich dazu zeigten die Top-Gate-Transistoren mit PS und PAZ deutlich geringere Transistorkennwerte. Diese Messergebnisse konnten mit einer besseren Benetzung des polareren PMMA auf dem eher hydrophilen ZTO begründet werden.

Die in dieser Arbeit präsentierten Ergebnisse könnten zur Prozessierung von kosteneffizienten, umweltfreundlichen, gedruckten und leistungsfähigen Dünnschichttransistoren beitragen.

Abstract

Most of the transistors are based on inorganic semiconductors such as the ubiquitous silicon (Si). Nevertheless they have some problematic issues. First, their crystalline quality must be very high to guarantee good device properties. Second, in order to achieve the first point costly and demanding processing methods are necessary. For certain application like radio-frequency identification (RFID) tags these processing cost are too high. On the other hand zinc tin oxide (ZTO) as an amorphous oxide semiconductor (AOS) can be processed out of solution and ensures good device characteristics even in the amorphous phase. In contrast to the widely studied indium gallium zinc oxide (IGZO) it does not contain the costly indium. In this thesis a precursor route for ZTO was developed that does not use the common but toxic 2-methoxyethanol as a solvent. It applied ethanol (EtOH) and ethylene glycol (EG) as an optional co-solvent. By applying this precursor solution thin ZTO films could be processed either by spin coating or ink-jet printing. Investigations revealed their smoothness, and predominant amorphous phase with small embedded zinc oxide (ZnO) nanocrystallites. The obtained transparent films exhibited an n-doped character. By building bottom-gate transistors using these ZTO films it could be shown that a Zn:Sn ratio of 7:3 produces the best transistor results, the replacement of 40 % of EtOH by EG could improve the thin film transistor (TFT) performance, and the stabilizer hydrochloric acid (HCl) led to the creation of electronic trap states. A multiple layer approach led to the improvements of all transistor parameters. The highest ever reported mobility of up to 7.8 $cm^2V^{-1}s^{-1}$ for an ink-jet printed bottom-gate ZTO transistor was obtained by processing eight layers. It could also be shown that a transistor composed of more than four layers had better resistance against positive bias stress (PBS) and water (H_2O) or oxygen (O_2) in the atmosphere. While H_2O acts as an electron donor in the ZTO system, O_2 leads to electron accumulation at the oxide surface. Devices composed of multiple layers showed acceptable performance even if annealed at a reduced temperature of 350 °C compared to the standard setting of 500 °C. The reason for the multiple-layer enhancements was identified as an improved surface coverage and film quality. A setup for time dependent transistor measurements was realized and the first results revealed, that the fastest switching of the ZTO transistors took place in the linear regime. The highest switching frequency of a transistor was measured to be 1.33 MHz. The investigated on-switching behavior can be described by two time constants. It is very likely that the small time constant represents the transport of the injected charge carriers while the long time constant is a measure for the transport of trapped charge carriers. Functional hybrid top-gate transistors using ZTO and the organic dielectric materials poly(methyl methacrylate) (PMMA), polystyrene (PS), and a benzyl azide containing copoly-

mer (PAZ) could be processed. It was shown that a minimal thickness of 490 nm of the organic dielectric PMMA was necessary to ensure good device performance and small leakage currents. The best performance could be achieved if new electrode masks were applied in order to reduce the overlap between the source/drain and gate electrode. The best working printed ZTO top-gate transistor using these masks and a PMMA layer showed a mobility of up to $4.4\,cm^2V^{-1}s^{-1}$. To the best of the author's knowledge this is the highest reported mobility of an ink-jet printed ZTO/PMMA top-gate transistor. The top-gate transistors using PS and PAZ as dielectrics exhibited inferior device performance. This result could be explained by a better adhesion of the polar PMMA to the quite hydrophilic ZTO surface. The results presented in this thesis could contribute to realizing easily processable, cost efficient, environmental friendly, printable, and good performing TFTs.

Contents

1 Introduction

We are living in the electronic age. Almost everyone naturally uses smartphones, computers, and other smart devices. But only very few people know how these devices work or that most of them contain millions and millions of transistors. But what are these transistors and how did they evolve? They were first realized 70 years ago at Bell Laboratories. One year later Jon Bardeen and Walter Brattain first reported a point contact transistor using germanium (Ge) as the active material [1]. With this three terminal device it was possible to amplify current signals. Their advisor William Shockley published soon after a work explaining the principle behind this new device [2]. Bardeen and Brattain already reported that their new device also worked using silicon (Si) as the active material. The major benefit of this material is the quality of the interface between its perfectly ordered single crystalline phase with electron mobility values of up to $1500\,\mathrm{cm^2V^{-1}s^{-1}}$ [3] and its amorphous oxide state silicon dioxide (SiO_2). Due to this fact most electronic devices continue to be based on this material combination. A big drawback of this material system is that its electronic properties suffer greatly if impurities are introduced or if the polycrystalline or even the amorphous phase is used for the production of transistors. Therefore great effort has to be taken to process single crystalline Si with very few defects. These processes are very complex and costly. For certain low demanding products like RFID devices or membranes other materials came into consideration for research groups all over the world. These materials include small organic molecules and polymers first reported by Chiang *et al.* in 1977 [4]. The benefits of these organic semiconductors are that most of them especially the polymers can be processed out of solution at low temperatures, making them feasible for flexible substrates [5]. Their two main problems are that they are very sensitive to oxygen (O_2) and water (H_2O) in the atmosphere and that they normally exhibit small charge carrier mobility values in the range of $1\,\mathrm{cm^2V^{-1}s^{-1}}$ or smaller. In 2004 amorphous oxide semiconductor (AOS)s evolved as another kind of material since Nomura *et al.* [6] reported on indium gallium zinc oxide (IGZO) which they processed at room temperature making it possible to realize electronic devices on flexible substrates. Since then many research groups worked on crystalline zinc oxide (ZnO) as a promizing transparent conductive oxide (TCO) material [7, 8, 9]. Due to the introduction of additional elements into the ZnO system amorphous phases can be realized and the scattering of charge carriers at grain boundaries can be avoided [10]. The main benefits of this kind of materials are that most of them can be processed out of solution, they form transparent thin films, they exhibit large mobility values of up to $100\,\mathrm{cm^2V^{-1}s^{-1}}$, and they are normally not sensitive to atmospheric H_2O and O_2 [11]. As Nomura *et al.* several research groups work on AOS materials containing indium.

Unfortunately, this rare earth element is not so abundant [12] with a concentration of 10^{-7} in the crust of the earth [13]. In addition, it has to be taken into account that most research groups use the toxic solvent 2-methoxyethanol which is not suitable for industrial production.

Recently the first industrial products based on printed electronics like the membrane switches produced by the company Metafas displayed in **Figure 1.1** has been realized [14].

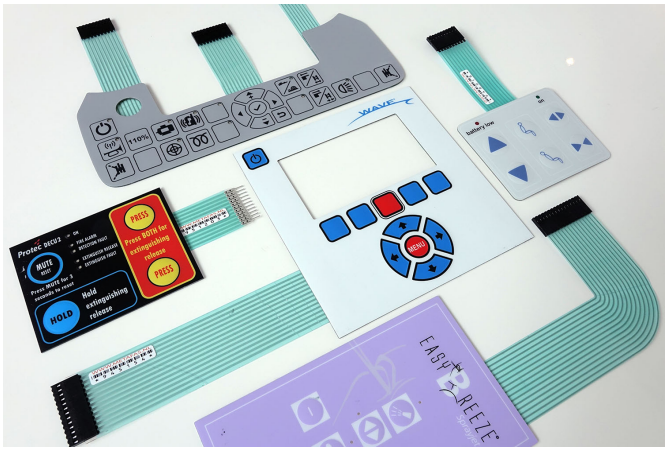

Figure 1.1: Different printed membrane switches distributed by the company Metafas from the Netherlands [14].

An important building block of such membranes are transistors. For this electronic devices different layout configurations exist. The two main layouts can differ in the position of the gate electrode. In comparison to the widely processed bottom-gate configuration the use of the top-gate layout has certain advantages. For instance organic dielectric materials can not be processed in the bottom-gate approach since the decomposition of the precursor normally requires high temperature which would severely affect them [15]. Furthermore the dielectric layer can act as a protective layer of the semiconductor against any interaction with gaseous species [16]. The benefits of organic dielectric materials in particular are their transparency, flexibility, and processing simplicity [17, 18].

The aim of this PhD project was to develop a cost efficient and environmental friendly precursor solution route. A route based on ethanol has been realized to achieve indium free zinc tin oxide (ZTO) films. Using this precursor solution ZTO thin films and field-effect transistors were first produced and characterized on purchased prestructured bottom-gate, bottom-contact thin film transistor (TFT) substrates. Then ZTO top-gate transistors based on different solution processed organic dielectrics could be processed and characterized.

This thesis is separated into six chapters. Following the introduction the thesis continues with a chapter about the basics of inorganic semiconductors and field-effect transistors with a focus on transparent conductive oxides and the investigated material ZTO. The experimental part dealing with the precursor route, processing methods, different transistor layouts, and the thin film as well as the electrical

characterization is introduced in chapter 3. Chapter 4 presents and discusses the main results of the research. First the outcome of the thin film characterization is presented followed by a section of how different factors of the precursor route influence the transistor performance. In the next section the effect of multiple-layers on printed transistors is investigated. Then the results of transistors processed at a reduced annealing temperature are introduced. Chapter 4 closes with the analysis of organic dielectrics and the results of hybrid top-gate transistors using ZTO as the semiconductor and organic polymers as the dielectric. The conclusion and outlook is presented in chapter 5.

2 Theory

In this chapter the basic principles of inorganic semiconductors with a focus on amorphous semiconductors will be presented. The differences to other materials such as metals and dielectric materials are introduced. Then the theory of field-effect transistors is reported followed by a section about transparent conductive oxides. This chapter closes with a presentation of the main features of the semiconductor: zinc tin oxide (ZTO).

2.1 Basics of inorganic semiconductors

In this section the basic concept of inorganic semiconductors such as its simplified band diagram, the Schottky effect, and current transport mechanisms will be introduced by referring to the books written by Kittel and Sze [19, 3].

Simplified band diagram

Band diagrams are a representation of Bloch functions that solve the Schrödinger equation for a one electron problem in a periodic lattice. They can be drawn in a Brillouin zone, which is an area in reciprocal space. A simplified band diagram of an ideal semiconductor at a temperature of 0 K can be seen in **Figure 2.1**.

Two important bands are drawn in this diagram with the ordinate being the energy of an electron E_e and the abscissa being the distance in the real space. On the one hand there is the completely filled valence band with the valence band maximum (VBM) and on the other hand the empty conduction band with the conduction band minimum (CBM). The energy spread between these two locations is called the band gap E_g. In the case of an undoped semiconductor the Fermi energy lies somewhere close to the middle of this band gap dependent on the density-of-states (DOS) of the two bands.

Using the definitions from **Figure 2.1** the simplified band diagram of a metal and a dielectric in comparison to a semiconductor can be drawn according to **Figure 2.2**. On the one hand in a metal the conduction band is not completely filled with electrons. The absence of a band gap is the reason why metals show electrical conductivity even at a very small temperature close to 0 K. Their resistivity is very low with typical values around $10^{-6}\,\Omega$cm [19]. On the other hand dielectrics such as SiO_2 ($E_g = 9.3$ eV [20]) or

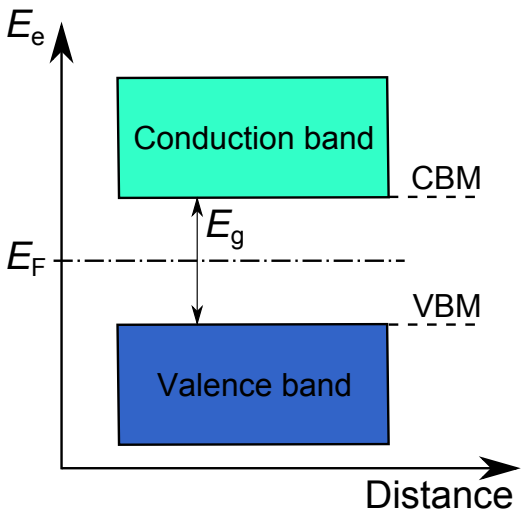

Figure 2.1: Simplified band diagram of an ideal semiconductor. The ordinate represents the energy of an electron E_e and the abscissa the location in the real space. The band lower in energy displayed in blue is the valence band with its maximum point the valence band maximum (VBM). The band higher in energy displayed in green is the conduction band with its lowest point the conduction band minimum (CBM). The energy difference between CBM and VBM is called the band gap E_g. At 0 K the Fermi energy E_F lies exactly in the middle of the band gap in the case of an ideal undoped semiconductor.

PMMA ($E_g = 4.8$ eV [21]) exhibit very large band gaps. The difficulty of optical excitation and charge carrier injection explains the high resistivity of these materials of up to 10^{17} Ωcm.

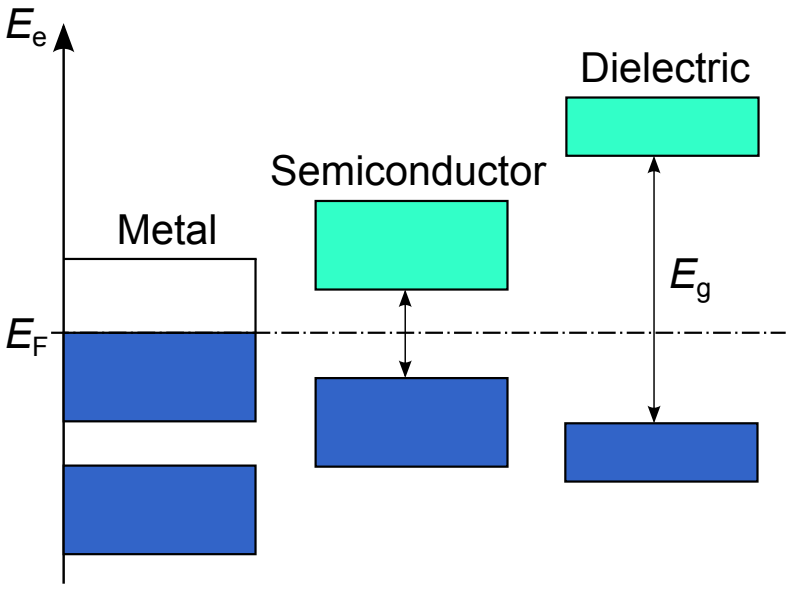

Figure 2.2: Comparison of the simplified band diagram of metals, semiconductors, and dielectrics. Displayed in blue are the valence bands and in green the conduction bands. Note that the band at E_F is not completely filled in the case of a metal. The semiconductors exhibit a small and the dielectric a large band gap.

Important electronic levels

A material can be defined as a semiconductor if its electrical resistivity measured at room temperature lies between 10^0 and $10^{11}\,\Omega$cm. A perfect semiconductor shows zero conductivity at a temperature of 0 K. Typical and widely studied semiconductors are the element-semiconductors Si and Ge and the compound semiconductors, for example gallium arsenide (GaAs). Semiconductors exhibit small band gaps unlike insulators. For instance Ge exhibits a band gap of 0.66 eV and the band gap of GaAs has been measured at 300 K to be 1.43 eV. If energy is introduced into the system, which exceeds the value of the band gap, electrons can be excited from the fully occupied valence band to the empty conduction band. During this process a positively charged hole is created in the valence band. Both, the electrons and holes, can lead to an increase in conductivity after the application of a voltage.
But the band gap is not the only important value to characterize a semiconductor. The difference in potential energy of an electron between the Fermi level E_F and the vacuum level E_VAC is defined as the work function Φ. Typical values for the work function are 5.1 eV for gold (Au) [3] and 4.6 eV for indium tin oxide (ITO) [22]. Other fundamental parameters of a semiconductor are the valence band offset $E_\mathrm{F} - E_\mathrm{VBM}$, which is the difference between the Fermi level and the VBM. The ionization energy E_ion is the energy that is necessary to extract an electron from the valence band to the vacuum level. **Figure 2.3** displays these main parameters in an electronic scheme of an n-type semiconductor. The energy differences are displayed in blue and the energy levels are shown in red.
The free charge carriers within a semiconductor drift through the material under an applied voltage with the drift velocity $v_\mathrm{D} = \mu\,\mathscr{E}$ where $\mathscr{E}$ is the electric field defined as $\mathscr{E} = V/d$. The unit of the mobility μ is $\mathrm{cm}^2\ \mathrm{V}^{-1}\mathrm{s}^{-1}$. Both electrons and holes can contribute to the overall conductivity σ of a semiconductor according to the formula $\sigma = (ne\mu_\mathrm{e}) + (pe\mu_\mathrm{h})$. In this formula n and p describe the concentration of electrons and holes, respectively, e the elementary charge, and μ the mobility of electrons or holes.

Schottky effect and transport mechanisms

In a unipolar n-type field-effect transistor (FET) the electron injection from the metallic electrodes to the semiconducting material is important. There are two major different metal/semiconductor contact possibilities. The Ohmic contact and the Schottky contact. It is characteristic of an Ohmic contact that the space charge region becomes so small that the electrons can pass it via tunneling which leads to a current independent on the sign of the applied voltage. The Schottky contact will be introduced by referring to the book of Bergmann and Schäfer [23]. If an electric field is applied the potential energy for emission of electrons is reduced owing to the image force. **Figure 2.4** illustrates the Schottky effect that appears at a metal/vacuum interface.

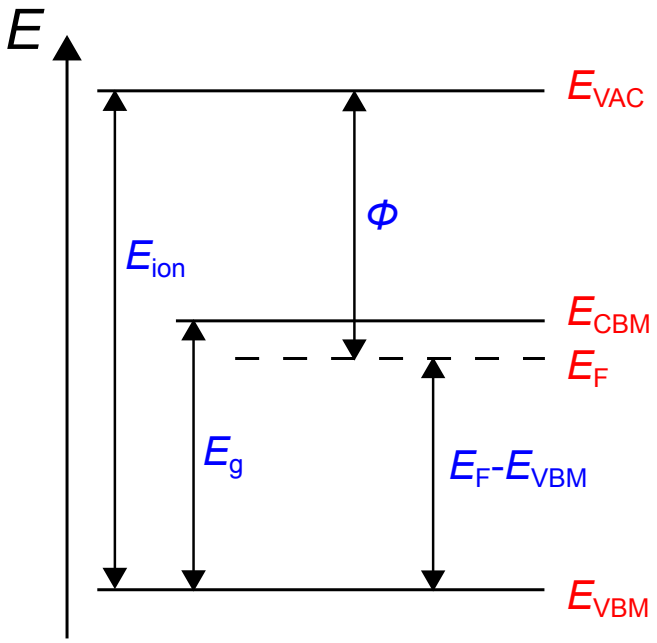

Figure 2.3: Energy scheme of an n-type semiconductor showing the main parameters valence band offset $E_F - E_{VBM}$, band gap E_g, work function Φ, and ionization energy E_{ion} displayed in blue. The main energetic levels E_{CBM}, Fermi energy E_F, E_{VBM}, and vacuum level E_{VAC} are labeled in red.

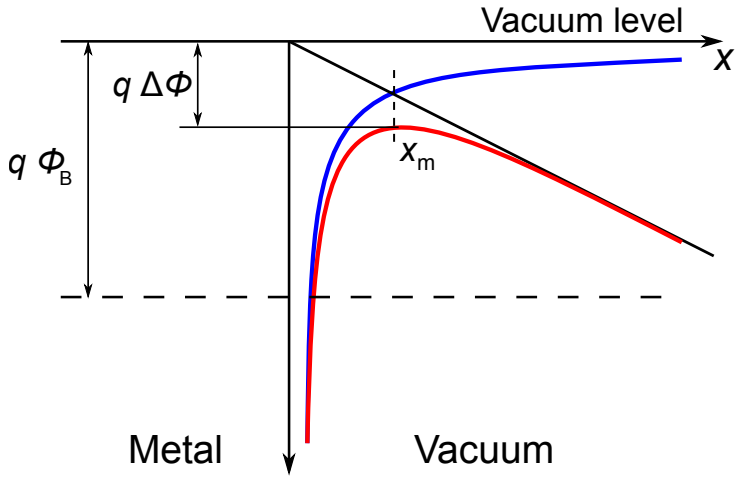

Figure 2.4: Illustration of the Schottky effect at a metal/vacuum interface. The image force at the interface leads to a decrease of the initial work function Φ_B by a value of $\Delta\Phi$.

The initial barrier height for thermionic emission of an electron out of the metal $q\Phi_B$ is reduced by $q\Delta\Phi$ due to the image force and the maximum is shifted to x_m. This image force is a result of the created positive elementary charge within the metal that is induced by the removed electron from the metal into the vacuum by the application of an external voltage. The total energy as a function of the distance x at the interface has consequently two contributions, the Coulomb energy from the image force, and the energy from the external applied field $\mathscr{E}$ (**Equation 2.1**).

$$E(x) = \frac{q^2}{16\pi\varepsilon_0 x} + q\mathscr{E}x \tag{2.1}$$

In **Equation 2.1** q labels the electric charge and ε_0 the vacuum permittivity. The changed work function $\Delta\Phi = \sqrt{\frac{q\mathscr{E}}{4\pi\varepsilon_0}}$ and its position $x_\mathrm{m} = \sqrt{\frac{q}{16\pi\varepsilon_0\mathscr{E}}}$ can be obtained if the derivative of (**Equation 2.1**) is set equal zero $\frac{\mathrm{d}E(x)}{\mathrm{d}x} = 0$.

If the metal is brought into contact with a semiconductor instead of the vacuum the relative permittivity of the semiconductor has to be taken into account. The electric field $\mathscr{E}$ in the space charge region of the semiconductor can now be written as displayed in **Equation 2.2**.

$$\mathscr{E} = \sqrt{\frac{2qN_\mathrm{D}}{\varepsilon_0\varepsilon_\mathrm{r}}\left(V - V_\mathrm{D} - \frac{k_\mathrm{B}T}{q}\right)} \tag{2.2}$$

N_D is the concentration of donors of the n-type semiconductor and V_D is the diffusion voltage. V_D in combination with the applied voltage V represents the factor for the activation energy $\Delta E = q(V_\mathrm{D} + V)$. This activation energy has to be overcome to inject electrons from the semiconductor into the metal since the current has to be proportional to $n_0 \exp\left(-\frac{q(V_\mathrm{D}+V)}{k_\mathrm{B}T}\right)$. n_0 represents the equilibrium concentration of electrons within the bulk of the semiconductor. With the help of **Equation 2.2** the voltage dependent barrier height $q\Phi_\mathrm{B}(V)$ within the space charge region of the semiconductor as a result of the Schottky effect can be determined using **Equation 2.3**

$$q\Phi_\mathrm{B}(V) = q\sqrt[4]{\frac{N_\mathrm{D}}{8\pi^2}\cdot\frac{q^3}{\varepsilon_0^3\varepsilon_\mathrm{r}^3}\left(\left|V - V_\mathrm{D} - \frac{k_\mathrm{B}T}{q}\right|\right)} \tag{2.3}$$

The next image visualizes the three main current transport mechanisms at an interface between a metal and an n-type semiconductor if a bias is applied in reverse direction (**Figure 2.5**). The thermionic emission over the barrier into the semiconductor is displayed in red. This mechanism normally occurs in medium doped semiconductors such as Si with $N_\mathrm{D} \leqq 10^{-17}$ cm^{-3} and is typical for Schottky diodes. The tunneling through the barrier (green) is the standard process in an Ohmic contact with heavily doped semiconductors. The recombination of electrons with holes from the metal in the space charge region is displayed in blue. Other mechanisms like recombination in the neutral region, edge leakage, and interface currents because of traps at the interface will not be presented because their role is negligible in standard inorganic semiconductors.

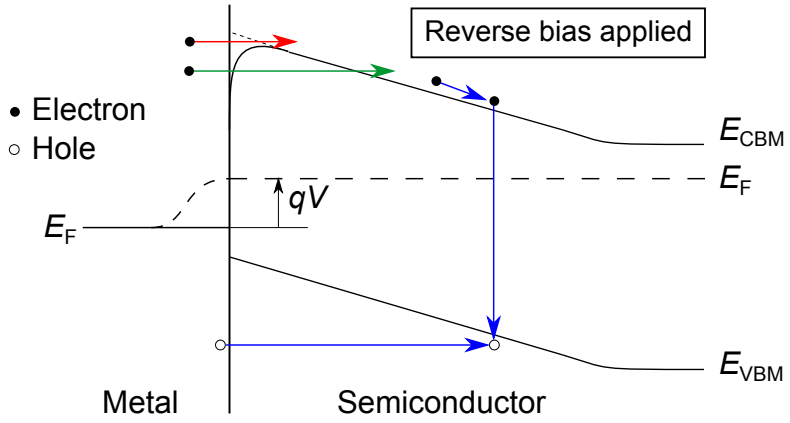

Figure 2.5: Representation of the three main current transport mechanisms that are possible at a metal/semiconductor interface under reverse bias condition. They are the thermionic emission over the barrier displayed in red, the field-emission or tunneling through the barrier shown in green, and the recombination in the space charge region of the semiconductor shown in blue.

2.2 Theory of field-effect transistors

In this section the basics of field-effect transistors will be presented since the properties of the semiconductor ZTO was analyzed using these electronic devices. First, the basic layout and electrical connection of a three terminal device is shown and discussed. Second, the Shockley equations, the most important equations defining a transistor, are discussed. Third, the various operation regimes and the two main *I*-*V*-characteristics transfer and output in a field-effect transistor, are analyzed. The section closes with a representation of how the most important transistor parameters were obtained graphically using the transfer characteristics.

TFT working principle

Transistors are, apart from diodes, detectors or photovoltaic cells, other devices relying on semiconductors. FETs are one part of the family of transistors. Their concept was first reported in the 1930's by Lilienfeld [24, 25, 26]. 30 years later the first TFT was realized by Weimer [27]. A few years later the first TFTs using tin dioxide (SnO_2) as semiconductor were reported by Klasens and Koelmans [28] and Boesen and Jacobs [29] in the case of ZnO. In 2004 Nomura *et al.* revived the research in AOSs by reporting that IGZO exhibits good transistor properties even if processed at room temperature [6]. Here the basic principle of these electronic devices will be presented by referring to the book *Physics of Semiconductor Devices* written by S.M. Sze [3]. If only one type of charge carrier is employed in a device it is called unipolar. Since most of the AOSs such as ZTO are n-type semiconductors the mechanism of electrons as the majority charge carriers will be discussed. Before the basic principles of a FET are

explained the field-effect shall be presented referring to a metal-insulator-semiconductor (MIS) diode as displayed in **Figure 2.6**.

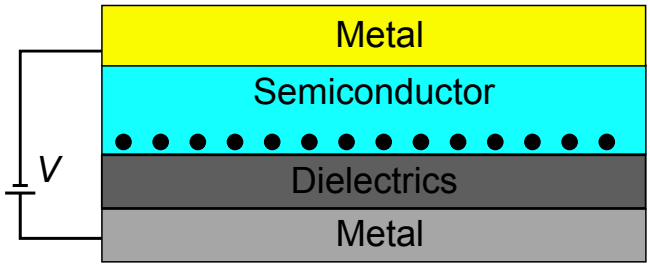

Figure 2.6: Sketch showing the field-effect of a metal-insulator-semiconductor (MIS) diode. This diode could be represented as a plate capacitor where the semiconducting and the dielectric layer is placed between the metal plates. Due to the application of an external voltage between the metal plates, electrons, represented as black dots, are accumulated at the semiconductor/dielectric interface.

If a voltage V is applied to the metallic layers of a MIS diode, electrons, represented as black dots, can be injected from the top metal and can be accumulated at the semiconductor/dielectric interface. The amplitude of this voltage determines the amount of accumulated electrons. If the top-electrode of a MIS diode is separated into two parts, which define the channel, the three terminal arrangement of a FET shown in **Figure 2.7** can be obtained. A FET can be described as an arrangement of resistors R within the semiconducting layer connected with capacitors C in the dielectrics known in electrical engineering as transmission line [30]. A variable contact resistance R_C may appear between source and/or drain electrode and the semiconducting channel which could lead to an S-shape in the output characteristic which will be discussed later with the help of **Figure 2.12**.

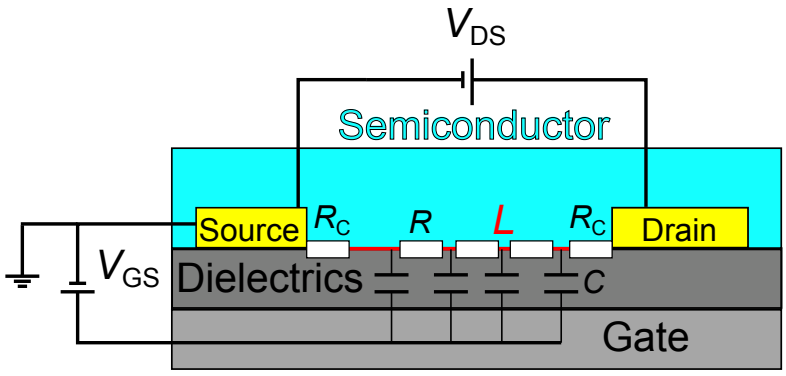

Figure 2.7: Sketch showing the principle layout of a bottom-gate, bottom-contact transistor. It is composed of the three electrodes gate, source, and drain and the semiconductor which forms the conductive channel with length L highlighted in red. A FET can be described as an arrangement of resistors R within the semiconducting channel by capacitors C to the gate [30]. A contact resistance R_C could exist between the source and/or drain electrode and the semiconducting channel.

The source and drain electrodes are separated from the gate electrode by a dielectric layer of a certain thickness. This three terminal arrangement is called bottom-gate, bottom-contact. Another arrangement of the three electrodes would be the bottom-contact, top-gate configuration. Both arrangements will be discussed in **Figure 3.4**. There exist two possible operation modes in a unipolar transistor. First, there is the mostly desired accumulation mode. This mode occurs if 0 V is applied between the source and the gate electrode and only very low current can be measured between the source and drain electrode (I_D). If a positive bias is now applied between the source and gate electrode (V_{GS}) electrons which are injected by the source and the drain electrode accumulate due to the field-effect at the semiconductor/dielectric interface. After the application of a positive bias between the source and drain electrode (V_{DS}) these accumulated electrons can be driven toward the drain electrode and an increase in the drain-current can be detected. The length L of this conductive channel between the source and the drain electrode is highlighted in red, but its width W is not displayed in **Figure 2.7**. Second, there is the depletion mode. In this mode a drain-current can be detected even though the gate-source voltage is 0 V. This could happen if the intrinsic semiconducting material already contains enough free charge carriers to contribute to a current flow. A negative V_{GS} bias has to be applied to turn such a device off. These devices can be called always-on devices. The threshold voltage V_{th} can be used to differentiate between the two modes. It represents the V_{GS} at which a conductive layer within the channel is formed by the accumulation of electrons. If its value is positive the transistor works in enhancement mode and if it is negative the transistor works in depletion mode. In addition this parameter is a measure for the amount of electronic trap states. Therefore it should be close to 0 V to obtain an energy efficient device which can be operated at small driving voltages.

Operation modes

There are three main operation modes in a FET, which are illustrated in **Figure 2.8**. In all three modes the source-gate voltage V_{GS} is larger than the threshold voltage V_{th}. In the first mode the source-drain voltage is smaller than the source-gate voltage (a). In this case the electrons can travel through the conductive channel from the source to the drain electrode. This channel was created by the accumulation of charges at the dielectric/semiconductor interface. The constant field is indicated by black arrows within the dielectric. In this mode the transistor can be seen as a resistor showing Ohmic behavior. This mode is called the linear regime. If the source-drain voltage is equal to the gate-source voltage it leads to a contraction of the channel where its depth y is reduced to zero at the drain electrode. This point at the drain electrode is called the pinch-off point and is highlighted as a red dot in **Figure 2.8** (b). The arrows in the dielectrics illustrate the direction of the electric field and clarify the field free pinch-off point. If

the source-drain voltage is increased even further (c) the drain-current does not increase further but stays constant. The channel length L is hereby reduced. This mode is called the saturation regime.

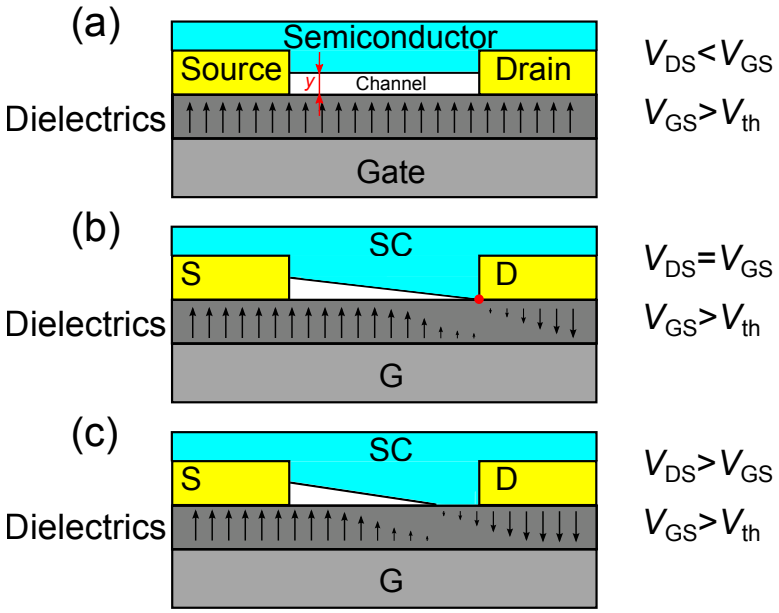

Figure 2.8: Operation modes of a FET operating with a source-gate voltage V_{GS} above the threshold voltage V_{th}. It shows the linear regime if the source-drain voltage V_{DS} is smaller than V_{GS} (a), the pinch-off point in red if $V_{DS} = V_{GS}$ (b), and the saturation regime if $V_{DS} > V_{GS}$ (c). The direction of the electric field within the dielectric layer is indicated by black arrows.

Shockley equations and transistor parameters

The dependencies between the drain-current and the two characterisic voltages V_{DS} and V_{GS} can be extracted using the Shockley equations. For the linear regime **Equation 2.4** can be applied. This equation is a result of the linear model [31] if a small V_{DS} is applied. In this case the transistor can be seen as a resistor, where its resistivity can be changed by the applied V_{GS} bias. The equation can be derived if the velocity and the applied electric field are assumed to be constant. The drain current can be written as a product of the charge density times the velocity $I_D = -WQ_{inv}v$ where the velocity is defined as $v = \mu\mathcal{E}$. Replacing the charge density by the expression $Q_{inv} = C'(V_{GS} - V_y - V_{th})$ the drain current can be written as $I_D = -WC'(V_{GS} - V_y - V_{th})\mu\mathcal{E}$. By substituting the electric field by its definition $\mathcal{E} = V_y/y$ the drain current is $I_D = -WC'(V_{GS} - V_y - V_{th})\mu\frac{dV}{dy}$. This expression can be written as $\int_0^L I_D dy = \mu WC' \int_0^{V_{DS}} (V_{GS} - V_y - V_{th})dV_y$. After the integration **Equation 2.4** can be obtained.

$$I_D = \frac{WC'}{L} \cdot \mu \cdot \left((V_{GS} - V_{th}) - \frac{1}{2}V_{DS}\right) \cdot V_{DS} \qquad \text{for} \qquad |V_{DS}| \leqq |V_{GS} - V_{th}| \tag{2.4}$$

The greek symbol μ represents the electron mobility and C' labels the areal capacitance. C' is calculated by $C' = \varepsilon_0 \varepsilon_r d^{-1}$ where ε_0 is the permittivity of vacuum, ε_r the dielectric dependent relative permittivity, and d is the thickness of the dielectric layer. Since transistors containing electronic trap states at the dielectric/semiconductor interface were characterized in this thesis, the threshold voltage (V_{th}) has to be taken into account.

To obtain the equation for the saturation regime (**Equation 2.5**) the quadratic model has to be applied [31]. Here the same assumptions made for the linear model have to be used but this time the charge density may change between the source and drain electrode. First this equation describes a linear increase of the current but eventually peaks. This happens if the charge density at the drain electrode becomes zero as shown in **Figure 2.8** (b). After this pinch-off point holes are accumulated since the sign of the electric field changes. This effect leads to the creation of a depletion layer at the drain electrode where the in excess applied V_{DS} bias is stored. **Equation 2.5** can be derived by applying **Equation 2.4**, which yields the following expression for the drain current for a small section of the channel with the width y: $I_D = C' \frac{W}{dy}(V_G - V_S - V_C - V_{th})dV_C$. In this equation the expressions V_G, V_S and V_C label the voltages at the gate, source, and within the channel, respectively. This equation can be integrated using the following limits $0 \leqq y \leqq L$ and $0 \leqq V_C \leqq V_{DS}$ yielding $\int_0^L I_D dy = \mu C' W \int_0^{V_{DS}} (V_G - V_S - V_C - V_{th}) dV_C$. The result of the integration is $I_D = \mu C' \frac{W}{L}[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}]$ if $| V_{DS} | < | V_{GS} - V_{th} |$. **Equation 2.5** for the saturation regime is obtained if $| V_{DS} | > | V_{GS} - V_{th} |$ is valid.

$$I_D = \frac{WC'}{2L} \cdot \mu \cdot (V_{GS} - V_{th})^2 \qquad \text{for} \qquad | V_{DS} | > | V_{GS} - V_{th} | \tag{2.5}$$

Since two voltage values can be changed in such a FET as introduced in **Figure 2.7**, two kinds of current voltage I-V-curves can be plotted (**Figure 2.9**). The output characteristic in which I_D is plotted against V_{DS} at constant V_{GS} voltages were obtained if **Equation 2.4** was applied as displayed in **Figure 2.9** a). First a linear increase of I_D as a function of V_{DS} can be seen (Linear regime). The non-linear regime is reached when V_{DS} becomes equal to V_{GS}, which is highlighted by a dashed black line. After that the drain-currents reach a steady state, which is called the saturation regime. The reason for this behavior was explained in **Figure 2.8** (c). **Subfigure 2.9** (b) displays the corresponding transfer characteristic where I_D is plotted against V_{GS} at a constant V_{DS} voltage using **Equation 2.5** and **Equation 2.4** for $V_{GS} > V_{DS}$. I_D increases in a quadratic dependency on V_{GS} until V_{DS} is equal to V_{GS} (dashed black line). Then I_D increases linearly with increasing V_{GS}. The transistor parameters for the plots were: $W = 10{,}000\,\mu m$, $L = 20\,\mu m$, $C' = 38.4\,nF/cm^2$ of a 90 nm thick SiO_2 layer, $\mu = 5\,cm^2\,V^{-1}s^{-1}$, and $V_{th} = 0\,V$.

The most important transistor properties can be obtained by a graphical analysis of the transfer characteristic. The linear or field-effect mobility μ_{lin} can be determined if the drain-current values in the linear

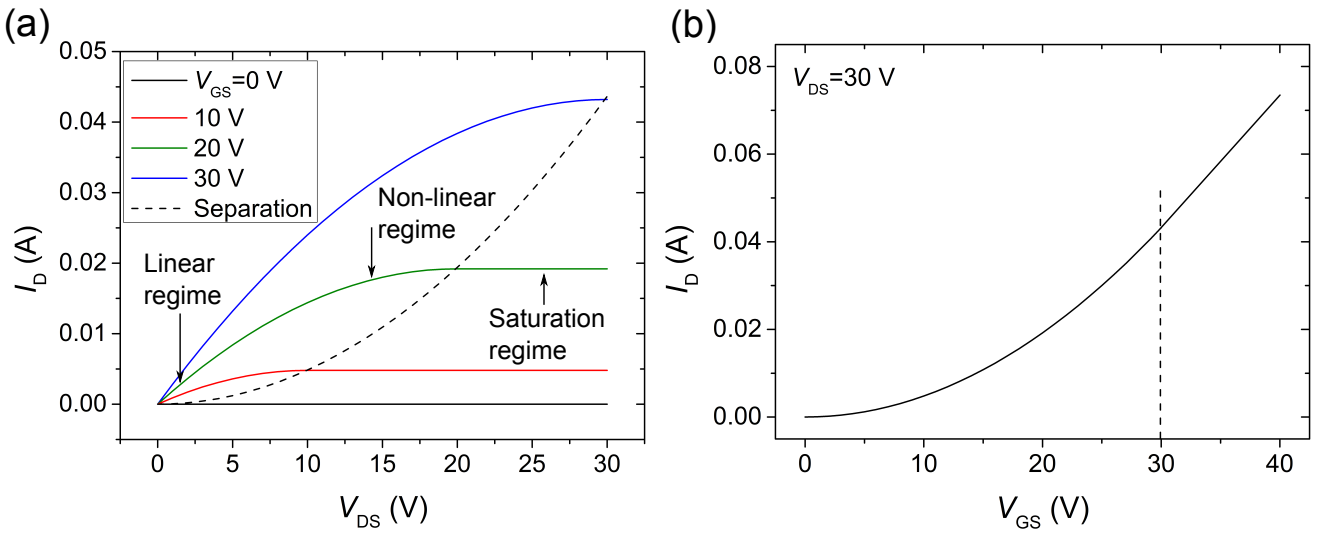

Figure 2.9: *I-V*-characteristics of an ideal n-type FET calculated using **Equation 2.4** and **Equation 2.5**. Subfigure (a) shows the ideal output characteristics, where I_D is plotted against V_{DS} at constant V_{GS}. In subfigure (b) the corresponding ideal transfer characteristics is obtained if I_D is plotted against V_{GS} at a constant V_{DS}. The dashed lines represents the boarder between the non-saturation and saturation regime.

region of the output curves are plotted against the V_{GS} as displayed in **Figure 2.10** (a). μ_{lin} can be calculated using the slope of the linear fit and **Equation 2.6**. This equation can be derived from **Equation 2.4**.

$$\mu_{lin} = \frac{L}{V_{DS} W C'} \left(\frac{\partial I_D}{\partial V_{GS}} \right) \tag{2.6}$$

The saturation mobility can be obtained if the transfer characteristics in the saturation regime is plotted in a square root (sqrt) fashion as shown in **Figure 2.10** (b). Using the slope of the linear fit and **Equation 2.7** μ_{sat} can be calculated. The sqrt-plot helps to graphically determine μ_{sat} due to the quadratic dependency of I_D to V_{GS} according to **Equation 2.5**. The threshold voltage can also be extracted from **Figure 2.10** (b) as the x-axis intercept of a linear fit. Both methods results in the same mobility of 5.0 $cm^2\ V^{-1}s^{-1}$.

$$\mu_{sat} = \frac{2L}{WC'} \left(\frac{\partial I_D^{0.5}}{\partial V_{GS}} \right)^2 \tag{2.7}$$

The on/off-current ratio can be determined if the drain-current is plotted semi-logarithmically as a function of V_{GS} in **Figure 2.11**. In this graph the subthreshold swing (S.S.), which is defined as S.S. $= \left(\frac{d \log I_D}{dV_{GS}} |_{max} \right)^{-1}$, can be calculated as the inverse of the logarithmic slope of I_D highlighted in red.

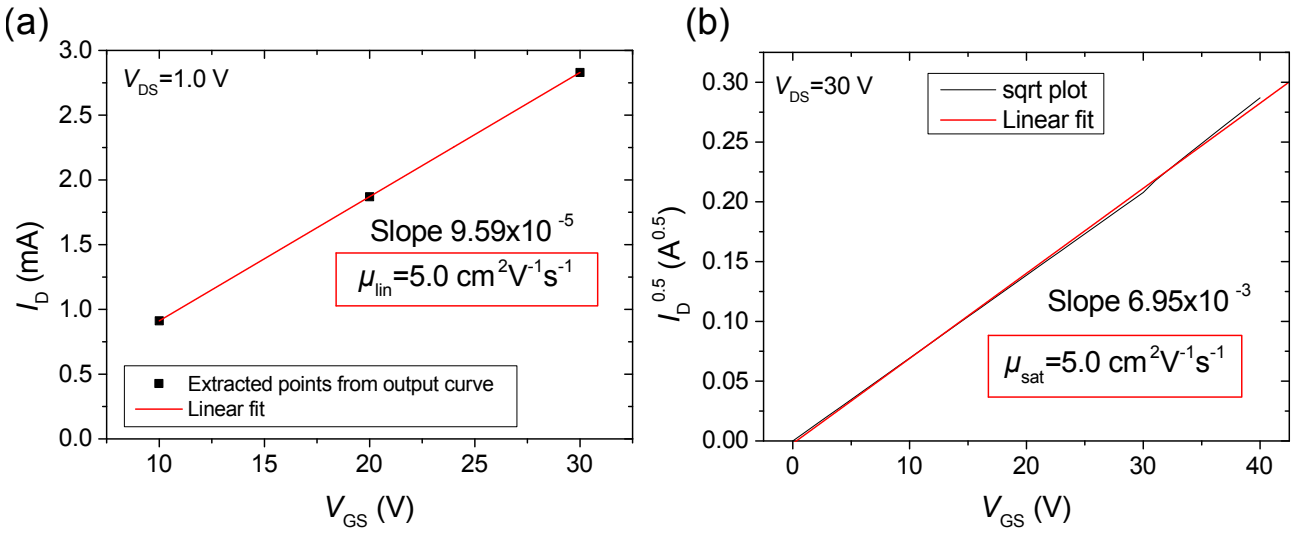

Figure 2.10: Linear plot of a the drain-current as a function of V_{GS} at a constant $V_{GS} = 1.0$ V. The point values are taken from the corresponding output characteristic which is not shown (a). The sqrt-plot of the drain-current as a function of V_{GS} is displayed in subfigure (b). Using the slope of the linear fit of the left plot the linear mobility μ_{lin} can be obtained using **Equation 2.6** and the slope of I_D of the right plot can be used to calculate the saturation mobility μ_{sat} according to **Equation 2.7**.

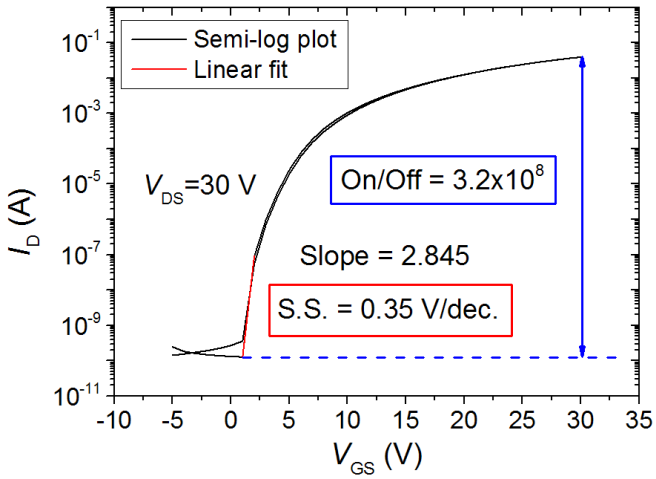

Figure 2.11: The on/off-current ratio as well as the subthreshold swing (S.S.) can be determined if the transfer characteristics is plotted semi-logarithmically.

The output characteristic gives information on possible contact resistances between the semiconductor and the source and drain electrodes as introduced in **Figure 2.7**. These resistances can sometimes be seen by the S-shape of the drain-currents close to $V_{DS} = 0$ V. One example of an output characteristic with an enlarged section showing the contact resistance in the red box is displayed in **Figure 2.12**. This contact resistance occur if the curves do not show straight lines at this point meaning no Ohmic behavior. If the linear mobility is determined according to **Figure 2.10** (a) the appearance of this contact resistance

could lead to the extraction of false data points since the contact resistance appear in the linear regime of the output characteristic.

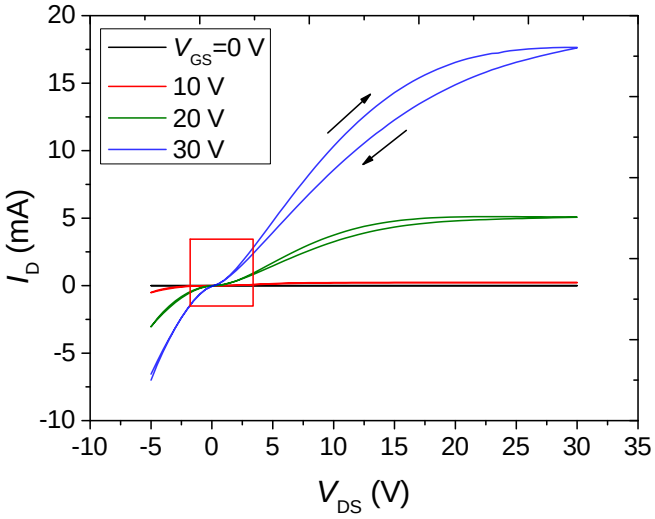

Figure 2.12: Example of an output characteristics that shows pronounced contact resistance. This S-shape of the drain-currents is highlighted by a red box. In addition, the hysteresis, meaning the difference between the forward and backward sweep of V_{DS}, is marked by black arrows.

Hysteresis as a difference between the forward and the backward sweep of the source-drain voltage can also be identified in an output characteristic. **Figure 2.12** displays such a hysteresis in the form of two black arrows. The reason for this hysteresis is the existence of electron trap states at the semiconductor/dielectric interface [32].

2.3 Basics of amorphous oxide semiconductors

At this point the characteristics of amorphous semiconductors will be discussed referring to the books of Mott and Hunklinger [33, 34]. It is important to reveal the differences between these semiconductors and their crystalline counterparts since most AOSs and also zinc tin oxide (ZTO) are amorphous. In amorphous semiconductors similar to crystalline semiconductors there are bands and a band gap. In the amorphous phase there are differences in the binding length and binding angles between the neighboring atoms that define the band gap. These differences lead to the fact that the DOS show no clear edge but an exponentially phased out trend. This means that the states do not occur often and they are far apart. The electrons in these states are localized. **Figure 2.13** represent the DOS plot of an amorphous semiconductor. The delocalized states of the valence and conduction band are displayed in green and the localized states are displayed in blue. Both states are separated by the mobility edge. The mobility edge states of the valence and conduction band are labeled as E_V^m and E_C^m. E_V' and E_C' show the edges of the localized band states. Defect states could exist within the band gap of an amorphous semiconductor as

shown in **Figure 2.13**. These defect states could appear because of unsaturated chemical bonds [33] or adsorbates. Differences in light absorption occur between amorphous and crystalline semiconductors. Transitions can occur between localized states of the valence and the conduction band. This could result in smaller band gap values of amorphous semiconductors in comparison to their crystalline counterparts as for instance in the case of Si. Gap states close to the mobility edge of the conduction band could be responsible for the hysteresis in *I*-*V*-curves of transistors. Wide deep states close to the mobility edge of the valence band are reported to be the reason why AOSs normally show no p-type conductivity [35].

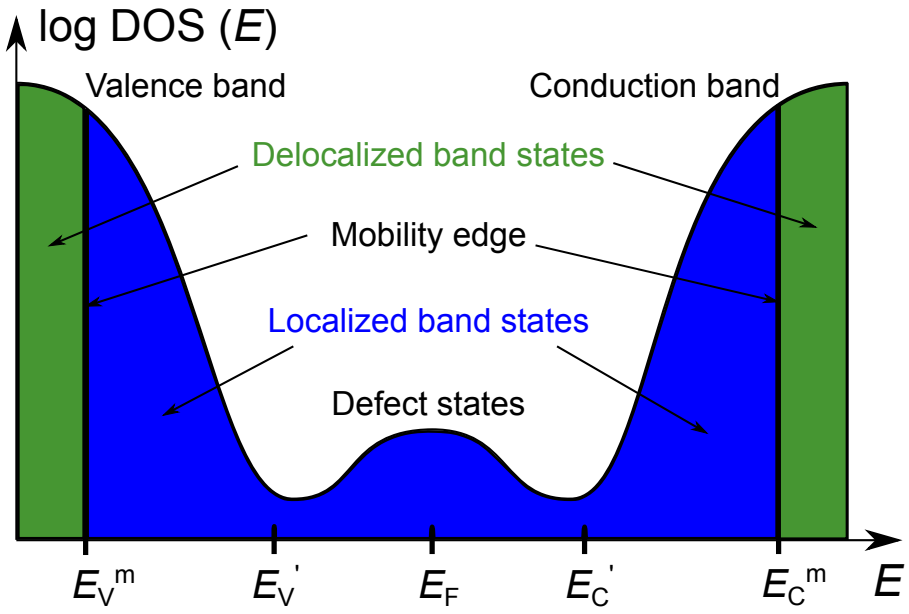

Figure 2.13: DOS with respect to energy in a logarithmic scale for an amorphous semiconductor. The delocalized states and the localized band states of the valence and conduction band are displayed in green and blue, respectively. The mobility edge of the valence and conduction band are labeled as E_V^m and E_C^m. E_V' and E_C' show the edges of the localized band states. Defect states can exist within the band gap. This scheme was inspired by images in the books of Mott [33] and Hunklinger [34]

Amorphous oxide semiconductors can be divided into binary systems such as ZnO, SnO_2, and In_2O_3, ternary systems such as ZTO, indium zinc oxide (IZO), and quaternary systems such as IGZO and hafnium zinc tin oxide (HZTO). ZnO is the most studied AOS material and ITO is the most studied material of all TCOs. O_2 vaccancies lead to highly n-type doping in these systems with mobilities ranging from 1 to 100 $cm^2\ V^{-1}s^{-1}$ [11]. Almost all of the TCOs possess an amorphous structure, thus avoiding electron scattering at grain boundaries during charge transport and trap states that are normally observed in polycrystalline films [10]. In addition, they exhibit large band gap energies ranging from 2.8 to 3.7 eV, which makes them transparent in the visible region of the electromagnetic spectrum [36]. In contrast to the rigid sp^3 orbital system of Si, where Hall mobility values deteriorate from the crystalline to the amorphous phase, transition metal oxides show comparable Hall mobilities in the crystalline and

the amorphous phase. This effect is due to the metal-oxygen-metal bonding between the large metal *s*-orbitals and the small oxygen (O) *p*-orbitals which is not extensively altered at the crystalline to amorphous transition [6]. **Figure 2.14** taken from the publication by Nomura *et al.* [6] illustrates this model in subfigure **b** and compares it with the rigid sp^3 orbital system of a classical semiconductor with a covalent bonding system such as Si in subfigure **a**. Transition metal cations possessing an electronic configuration $(n\text{ -}1)d^{10}n\ s^0$ with n being geater than or equal to 5 show the above described behavior between the crystalline and amorphous phase [37]. The widely studied materials IZO, IGZO, and ZTO fulfill this requirement. ZTO was evaluated in the framework of this thesis.

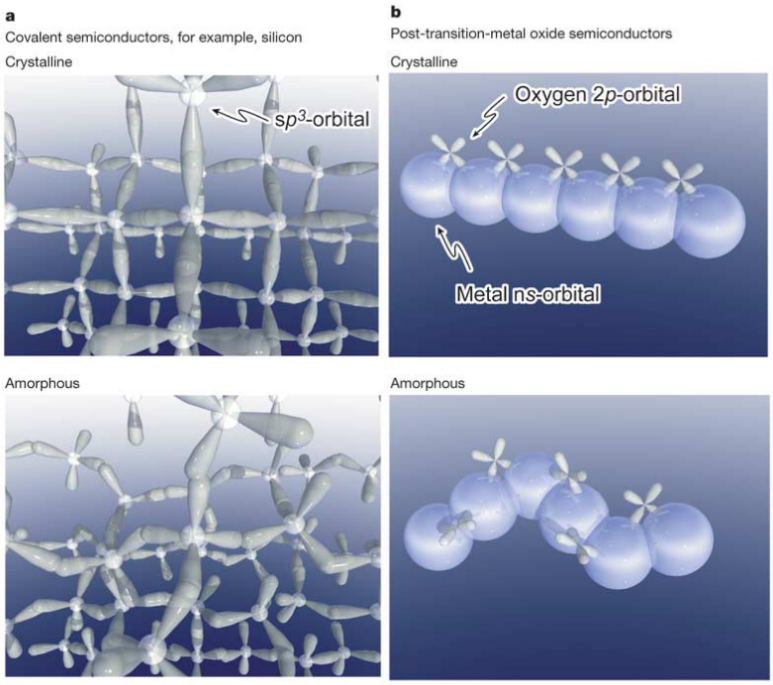

Figure 2.14: Illustration of the orbital arrangement in a classical sp^3-hybridized semiconductor as Si **a**, and in a TCO composed of big *s*-orbitals and small *p*-orbitals **b**. In the former case the overlapping between the orbitals and consequently the electron mobility detoriates by the crystalline to amorphous transistion, but in the latter case the overlapping of the big *s*-orbitals is not altered extensively. This image was taken from the publication of Nomura *et al.* [6].

A detailed picture of the band structure of such a covalent semiconductor as Si in comparison to a more ionic like semiconductor such as a TCO will now be presented. A sketch of these two systems is illustrated in **Figure 2.15** referring to the review article of Kamiya and Hosono [10].

In Si the band gap E_g is defined as the gap between the VBM and CBM. The former is known to be the bonding sp^3-hybridized σ-orbitals and the latter is known to be the anti-bonding sp^3-hybridized σ^*-orbitals (a). E_g is formed because of the energetic splitting of the two states. If a Si vacancy V_{Si} is formed, a dangling bond state with one unpaired electron is created in the middle of the band gap (b). This state can act as a trap state for electrons and holes affecting the functionality of n- and p-type Si

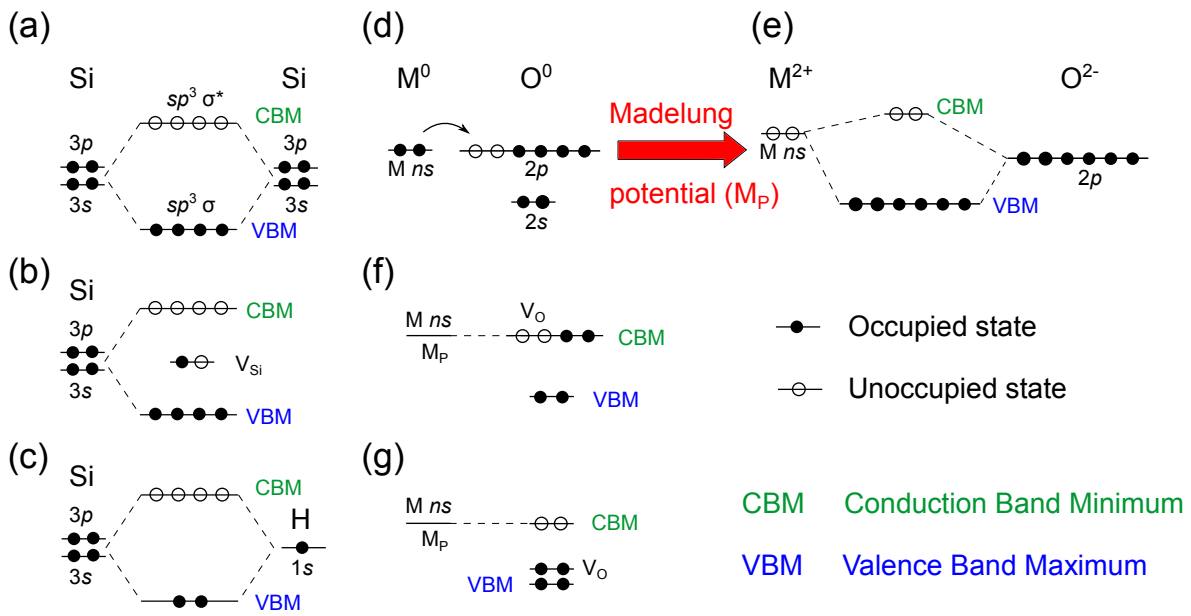

Figure 2.15: Simplified band structure of Si and TCO. The band diagram of Si (a) is altered to (b) if a Si vacancy V_{Si} is created in the middle of the band gap. This unoccupied state can act as electron or hole trap state. This state can be negated by hydrogen treatment (c). The equilibrium band structure of a transition metal oxide (d) is changed by electron transfer from the metal to the O atom, which is indicated by an arrow. The created ionic states are stabilized by the Madelung potential M_P leading to a rise in the cationic level and a decrease in the anionic level (e). If an O vacancy V_O is created in the metal oxide, states will appear in or near the conduction band maximum which can act as donors (f). Normally these states are not stable and relax to occupied states near the VBM, which can not act as electronic trap centers (g). This image was inspired by the publication of Kamiya and Hosono [10].

devices. To avoid such dangling bonds the semiconductor is passivated using hydrogen in order to move this state into the valence band (c). The band diagram of a TCO is displayed in **Figure 2.15** (d). It is changed if two electrons are transferred from the metal to the O atoms. This leads to a reorganization of the band structure because the electronic level of the metallic cation is increased and the electronic level of the O anion is lowered according to the Madelung potential. In this case the VBM is formed by the O 2*p*-orbitals which are now fully filled while the CBM is formed by the unfilled metallic *s*-orbitals (e). If an O vacancy V_O is now created, states in or near the CBM states appear which can act as shallow donors, but not as trap centers for electrons (f). These states are not stable and relax to fully occupied states near the VBM that can no longer act as electron trap centers (g). For TCOs the Madelung potential is very important since it is the cause of their transparency, large band gap, and small amount of electron trap states in the band gap [35].

2.4 Zinc tin oxide as semiconductor

Zinc tin oxide (ZTO) can be seen as a combination of ZnO and SnO_2. It can be written as $(ZnO)_x(SnO_2)_{1-x}$ with x being in the range between 0 and 1. ZTO, especially with $x < 50\,\%$, is also reported to be very stable against chemical etching [38]. The ZTO system is widely studied in the literature since it does not contain the not so abundant but widely used indium [12]. In 2010 Lee *et al.* showed that ZTO exhibits a band transport in the saturation regime [39]. This band transport is due to delocalized states which are more pronounced at higher values of the charge carrier concentration *n*. Temperature dependent mobility measurements reveal that the mobility decreased with increasing temperature in the saturation regime. This trend is typical for a band transport. Their result show a clear mobility edge with good agreement with the model of Mott [40].
Currently ZTO films are processed by sputtering [41, 42, 43, 16] or spin-coating techniques [44, 45, 46, 47] which are both associated with a large material consumption. In contrast, the ink-jet printing process is more favorable because the ink is mainly supplied to the area of interest. No additional post processing like patterning with masks or photolithography are necessary, thereby leading to a reduction in potential production costs by 64 % [15]. This implies that production waste can be reduced and the scale of production can be increased [48].

There are two ZTO phases reported in the literature. The first one is the trigonal, illmenite phase of $ZnSnO_3$ first processed via an ionic exchange reaction by Kovacheva and Petrov in 1998 [49] and the second one is the inverse cubic spinell phase of Zn_2SnO_4 first reported by Barth and Posnjak in 1932 [50]. Kovacheva and Petrov reported that the $ZnSnO_3$ phase is not thermodynamically stable and decomposes into Zn_2SnO_4 and SnO_2 [49]. The bandgap of $ZnSnO_3$ has been reported to be 3.5 eV and the work function to be 5.3 eV [51]. Zn_2SnO_4 has a bandgap of 3.35 eV [41] and a work function of 5.02 eV [52]. The CBM is defined in both phases by unoccupied 4*s* and 5*s* orbitals of zinc (Zn) and tin (Sn), respectively [38].

The first transistors were processed by magnetron sputtering reported by Chiang *et al.* in 2004 [42]. Jeong *et al.* reported on thin film transistors composed of solution processed ZTO [53]. They employed $Zn(CH_3COO)_2 \cdot 2\,H_2O$ and $Sn(CH_3COO)_2$ in a solution of 2-methoxyethanol and ethanolamine as a stabilizer. Their thin films show an amorphous structure with embedded nanocrystals if processed at 500 °C. It was reported that if other elements like indium (In) or tin (Sn) are added to the crystalline ZnO the system transforms into an amorphous structure [54, 55]. Processed bottom-gate, top-contact transistors using SiO_2 gate dielectrics exhibit a maximum mobility of $1.1\,cm^2\,V^{-1}s^{-1}$. Ink-jet printed ZTO transistors were first reported by Kim *et al.* in 2009 [56]. They used a similar precursor route and transistor layout as reported by Jeong *et al.* [53], but this time the solution was applied via ink-jet

printing. Their maximum saturation mobility was reported to be 0.6 cm^2 $V^{-1}s^{-1}$. Unfortunately, almost all groups use the widely applied but toxic 2-methoxyethanol as a solvent, which is not suitable for industrial production. In 2015 Branquinho *et al.* [57] showed that a precursor solution based on EtOH can result in high quality ZTO layers. They could create transistors with a saturation mobility of 0.8 cm^2 $V^{-1}s^{-1}$ using a thin AlO_x dielectric layer.

3 Experiment

This chapter will introduce the ethanol (EtOH) based precursor route. The two solution processing methods, spin coating and ink-jet printing, are presented. In addition, the various thin film characterization techniques that give information about the morphology, structure, and electronic levels of ZTO are displayed. Then the different transistor layouts used throughout this thesis will briefly be presented. The chapter closes with a presentation of the electrical characterization of the transistors.

3.1 Precursor route

In this section it will be presented how the ZTO precursor solution was processed. The precursor route is also based on EtOH as a solvent similar to the one described by Branquinho *et al.* [57]. But in contrast to their approach no urea ($CO(NH_2)_2$) as a fuel but HCl as a stabilizer and oxidation agent was added. First the hygroscopic salts zinc nitrate hydrate ($Zn(NO_3)_2 \cdot xH_2O$) 99.999 % and tin(II)-chloride ($SnCl_2$) 99.99 % both purchased from Sigma-Aldrich were weighted in a nitrogen (N_2) filled glove box (GB). This mixture of salts was then dissolved in 99.8 % pure EtOH (H_5C_2-OH) ordered from Carl Roth GmbH in air. The obtained solution exhibits precipitation, since basic tinchlorid is not stable under hydrophilic conditions (**Equation 3.1**) [58].

$$SnCl_2 + H_2O_{(g)} \rightleftarrows Sn(OH)Cl + HCl \qquad \text{Precipitation} \tag{3.1}$$

With addition of HCl 34 wt % (Merck) the balance of **Equation 3.1** can be shifted to the left. This avoids the formation of basic tin hydroxide chloride Sn(OH)Cl salt as a product of the presented hydrolysis reaction (**Equation 3.2**). The $SnCl_2$ is strongly reductive [59]. Oxygen from the air leads to a slow oxidation of $SnCl_2$ from Sn^{2+} $2\,Cl^-$ to Sn^{4+} $4\,Cl^-$ (**Equation 3.2**) [58]. The formation of Sn(OH)Cl and the resulting precipitation reaction are avoided.

$$SnCl_2 + 2\,HCl + \tfrac{1}{2}\,O_2 \longrightarrow SnCl_4 + H_2O \qquad \text{No precipitation} \tag{3.2}$$

The difference between the two reactions can be seen in the pictures of precursor solutions in **Figure 3.1**. Picture (a) shows precipitation of Sn(OH)Cl if no HCl was added. A clear solution with no signs of precipitation can be seen in picture (b).

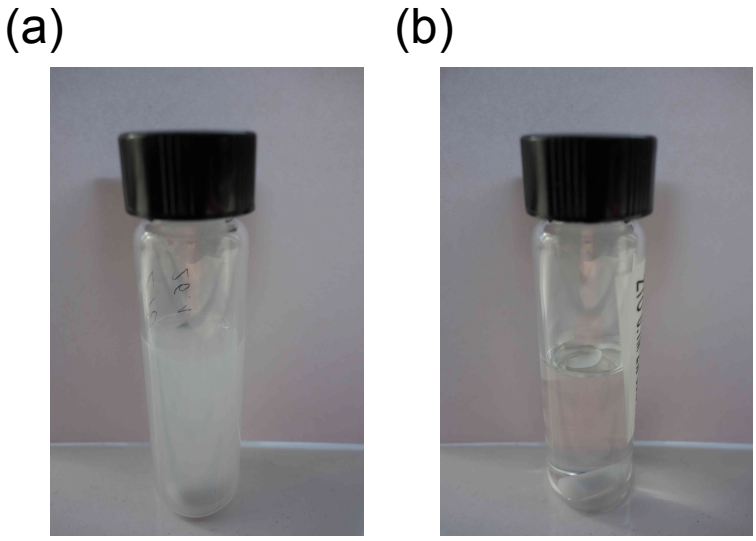

Figure 3.1: Pictures of the ZTO precursor solution without the addition of HCl showing precipitation (a) and with the addition of HCl resulting in a clear solution (b).

This precursor solution was then stirred for at least 14 hours at room temperature in air. Before usage it was filtered through a 0.2 µm polytetrafluoroethylen (PTFE)-filter in order to remove any residuals. The final precursor solution is stable for up to twelve month stored in ambient atmosphere.

3.2 Processing methods

The above described precursor solution was either applied by spin coating or ink-jet printing. Both methods will now briefly be described. In addition, it will be explained how the processed films are transformed to the oxide state and which organic dielectrics were used for the top-gate transistors.

Spin coating and annealing condition

Spin coating or spin casting is a common method for the application of solutions or dispersions. After dispensation onto the substrate, thin films can be processed by rotating the substrate at high angular velocity between 1500 and 5000 revolutions per minute (rpm). As first reported by Lawrence in 1988 [60] the spin coating process can be separated into four steps: preparation, acceleration, decrease of thickness, and drying (**Figure 3.2**).

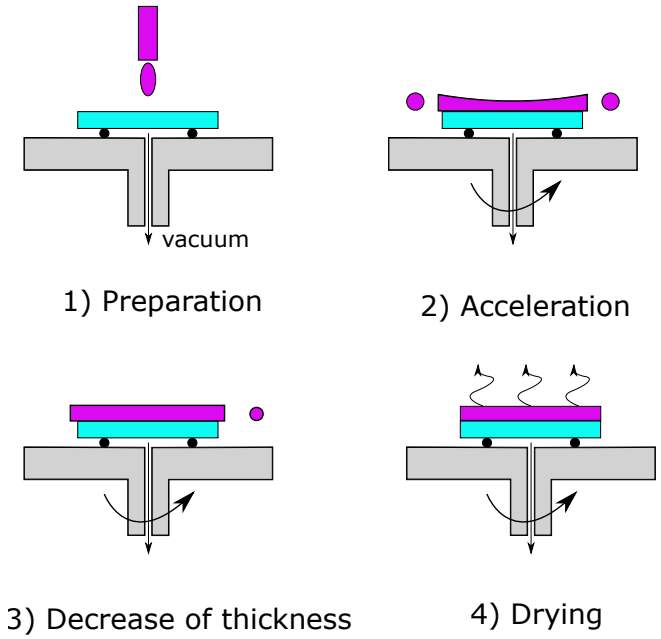

Figure 3.2: Illustration of the four steps of a spin coating process: 1) preparation, 2) acceleration, 3) decrease of layer thickness, and 4) drying.

First, the substrate is fixed onto the spinning table by using a slight vacuum. Then the precursor solution is applied and the spin coater is turned 'on' simultaneously. At the beginning excess solvent is thrown off the substrate until the film is thin enough that it can withstand the rotating speed of the substrate. The acceleration of the substrate until the final spin casting speed was reported to have an influence on the uniformity of the layers. The higher the final spin coating speed the more uniform the layers will be [61]. Once the film can follow the speed of the substrate the viscous and adhesive forces match the centrifugal forces. The viscosity of the solution, determined mainly by its concentration, has the biggest impact on its flow. During the last step the layer thickness is decreased by the drying process, meaning the evaporation of solvent. The final film thickness depends on the concentration of the solvent at the beginning and the spinning speed.

After the application of the precursor solution, either by spin coating or by ink-jet printing, it has to be transformed to its semiconducting oxide state. This process is normally performed by thermal decomposition of the precursor in an oven or on a hotplate. But other methods like UV ozone treatment in combination with thermal annealing [62], chemical decomposition [63, 64], and laser sintering [65] are possible too. However, in this thesis the processed precursor solution was annealed at 500 °C for 10 min on a hotplate in air after each layer deposition step if not stated otherwise.

Ink-jet printing

Apart from the above described spin coating process, ink-jet printing was also used throughout this thesis for the application of ZTO precursor solutions. The description of this technique will refer to

the review articles of Cummins [66], Derby [67], and Wijshoff [68]. First the different types of ink-jet printing systems will be presented. Second, the piezoelectrically driven system will be discussed in more detail. This subsection closes with an explanation of the possible interactions between the drops and the substrate including the coffee stain effect, and a presentation of the most important ink parameters.

Since its invention in the beginning of the early 19th century ink-jet printing was applied in the publishing and graphics industry. But the first commercial ink-jet printing systems were not produced before the 1950's. Ink-jet printing technology can be divided into two main branches: the continuous branch where drops are ejected continuously and the drop-on-demand (DOD) branch. The on demand drops are created by thermal, piezoelectric, electrostatic, or acoustic excitation. Since in this thesis the DOD technique based on piezoelectric excitation was used, it will now be discussed briefly.

Figure 3.3 shows an illustration of how a piezoelectric powered DOD ink-jet printer works. The ejection of the ink is managed by a piezoelectric transducer which is displayed in red. The necessary pressure to eject ink droplets is created by mechanical forces which are created by the inverse piezoelectric effect and the application of an electrical bias signal.

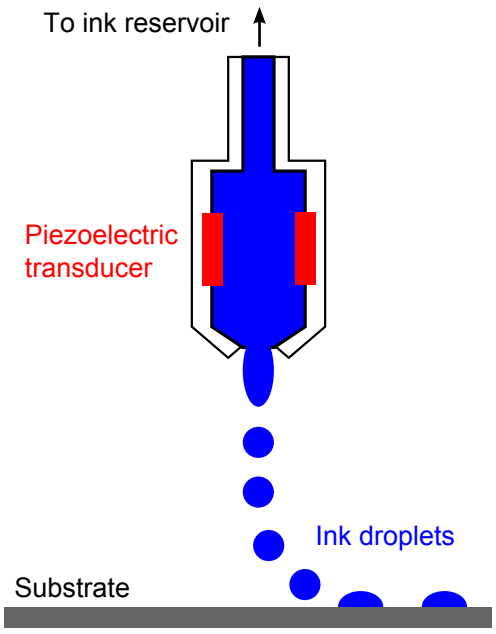

Figure 3.3: Sketch of a piezoelectric driven DOD ink-jet system containing a piezoelectric transducer displayed in red.

A satisfying printing result not only requires an advanced printing system but additionally certain properties of the ink. The main constants which characterize the quality of the ink are composed of these parameters: density ρ, dynamic viscosity η, and surface tension κ. They are used to define the Reynolds *Re*, Weber *We*, and Ohnesorge *Oh* numbers which are expressed in **Equations 3.3** to **3.5**.

$$Re = \frac{v_{\mathrm{F}} \rho d_{\mathrm{n}}}{\eta} \tag{3.3}$$

$$We = \frac{v_{\mathrm{F}}^2 \rho d_{\mathrm{n}}}{\sigma} \tag{3.4}$$

$$Oh = \frac{\sqrt{We}}{Re} = \frac{\eta}{(\sigma \rho d_{\mathrm{n}})^{0.5}} \tag{3.5}$$

The other parameters are the fluid velocity v_{F} and the diameter of the printing noozles d_{n}. Fromm defined another constant Z as $Z = 1/Oh$ here labeled as Fromm number [69]. This number should range between one and 10 according to Reis and Derby in order to achieve a good drop formation [70, 67]. If Z is smaller than one the ink is too viscous to be ejected and if Z is larger than 10 its viscosity is too small leading to the creation of satellite drops and spilling. Another effect, which often appears in the printing process, is the coffee stain effect. It occurs when the contact line of the solvent is pinned which leads to a material transport from the center of the droplet to its edge, where a ring is created after the evaporation of the solvent [71]. Another explanation was given by Hu and Larson in 2006 [72]. They explained that it occurs if the Marangoni flow, which is created by the latent heat of evaporation, is suppressed.
For the application of the precursor ink a commercially available desktop DOD ink-jet printer Dimatix DMP2831 from the Fujifilm Holdings Corporation was used. The cartridges store up to 1.5 mL ink, which is ejected through 16 nozzles. Each printed drop contains 10 pL of ink. The spacing between the individual drops was set to 20 µm. Using the printer software it is possible to operate the printer with a predefined printing pattern. The printed films were thermally annealed in the same manner as the spin coated films.

3.3 Transistor layouts

Displayed in **Figure 3.4** are four different layouts possible in a thin-film transistor [15].
FETs can be distinguished by the location of the gate electrode at either top or bottom and by the position of the source and drain electrodes relative to the semiconductor as either staggered or coplanar. Staggered is used if the source and drain electrodes are on opposite sides of the semiconductor/dielectric interface and coplanar if they are orientated on the same sides defined by Wallmark and Johnson [73]. The staggered bottom-gate layout is mainly used for the application of amorphous Si because it can easily be processed and shows the best electrical performance. This is the standard layout for display

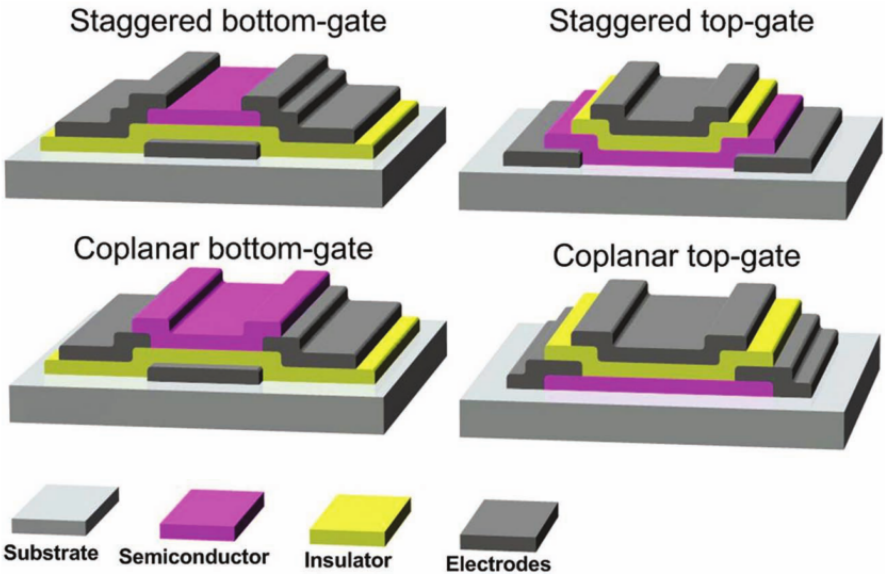

Figure 3.4: Illustration of four main field-effect transistor layouts namely bottom-gate or top-gate orientation in staggered or coplanar positioning of the source and drain electrodes relative to the semiconductor. This illustration was taken from the publication of Fortunato *et al.* [15].

manufacturing because the gate electrode shields the semiconductor from the backlight. Polycrystalline Si is normally processed using a coplanar top-gate structure because its crystallization requires high temperature which could affect the lower layers. This layout also protects the semiconductor from contact with air.

Bottom-gate, bottom-contact layout

Now the layouts applied in this thesis will be presented and discussed. Prestructured and commercially available substrates from the Fraunhofer Institute for Photonic Microsystems IPMS (Dresden, Germany) were used as a standard. They exhibit a bottom-gate, coplanar bottom-contact layout, a size of 15x15 mm, and are labeled from here on as Fraunhofer (FH) substrates. The substrates consist of n-doped Si ($n = 3x10^{17}$ cm^{-3}) exhibiting a thickness of 675 µm and act as the gate of the transistor. They were covered at the IPMS by a 90 nm thick thermally grown SiO_2 used as gate insulator, followed by interdigitated source/drain electrodes composed of 10 nm ITO as an anchor layer and 30 nm Au. From the 16 prestructured transistors only four with a channel length $L = 20$ µm and a width W of 10 mm ($W/L = 500$) were analyzed to avoid short channel effects. The main benefit of these substrates is that only the semiconductor has to be applied in order to build functional devices. **Figure 3.5** (a) shows a cross-sectional representation of a single source-drain structure and **Figure 3.5** (b) displays the top view image of the interdigitated source/drain structure of a 20 µm channel length transistor. In the top right and bottom left of the latter image a part of the contact pads can be identified.

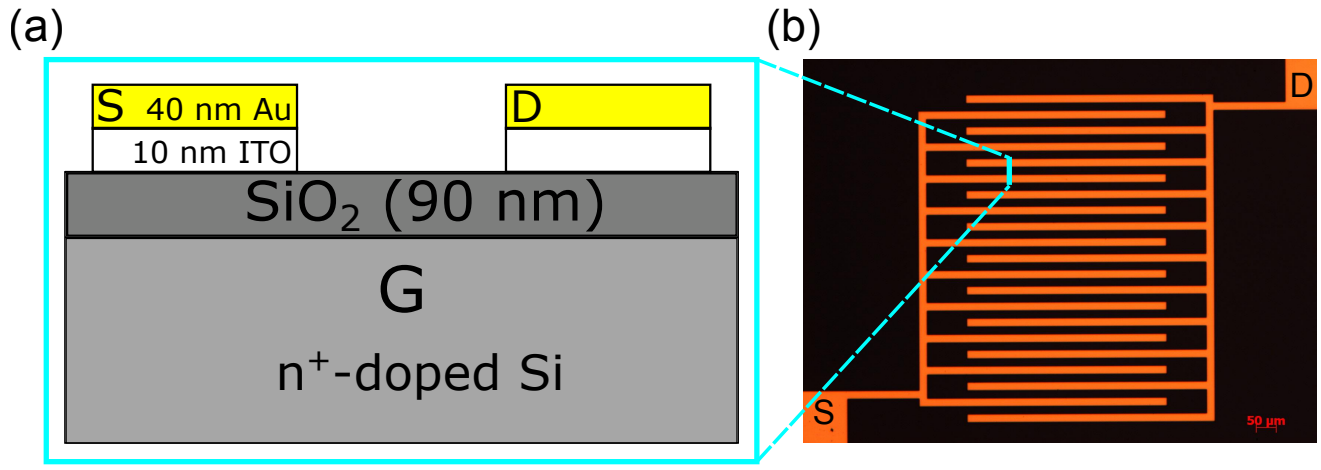

Figure 3.5: Cross-sectional representation of a FH substrate exhibiting a bottom-gate, bottom-contact layout (a). Top view image of a FH substrate showing the interdigitated source/drain structures with a channel length of 20 µm and a channel width of 10 mm (b).

The FH substrates were first cleaned by ultrasonication in technical acetone for 10 minutes, followed by a purging step with de-ionized (DI)-H_2O. These two steps were necessary in order to remove a protective polymer layer applied by the supplier. Then they were cleaned by ultrasonication in pure acetone and propanediol for 15 minutes. Subsequently they were treated in an air plasma (70 W) for 60 s in a home made vacuum chamber in combination with the RF-generator PFG 300 RF by Trumpf Hüttinger GmbH & Co KG if ZTO was applied by ink-jet printing. If ZTO was applied by spin coating the substrates were put for 15 min in an UV-ozone photoreactor PR-100. Both treatments were performed to increase the hydrophilicity of the substrates and to remove organic residuals.

Top-gate layout

In addition staggered top-gate transistors were processed. Glasses with a thickness of 1.1 mm and covered with 100 nm ITO were purchased from VisionTek Systems Ltd. (Chester, UK). These substrates were patterned in order to define ITO contact pads using a photolithographic process which involved the application of the photoresist AZ 1518 via spin coating followed by a UV treatment for 1 min and sequential development and etching in MIF 726 and hydrobromic acid (HBr). Then they were cleaned by ultrasonication in N-methyl-2-pyrrolidone (NMP) and acetone for 60 min each. Each of the glass substrates were cut into four 25x17.5 mm pieces. Remaining glass splinters were sprayed off with DI-H_2O. Then they were cleaned by ultrasonication in 5 vol % Deconex watery solution, followed by a DI-H_2O spraying and N_2 drying step. They were put in acetone and propanediol and cleaned by ultrasonication for 15 minutes each.

Figure 3.6 displays the masks for the evaporation of the source-drain (black) and the gate structure (red). The substrate is cut along the green lines in order to obtain four samples. A single transistor with the

three electrodes and channel is shown as an enlargement of this figure. The glass substrates with the

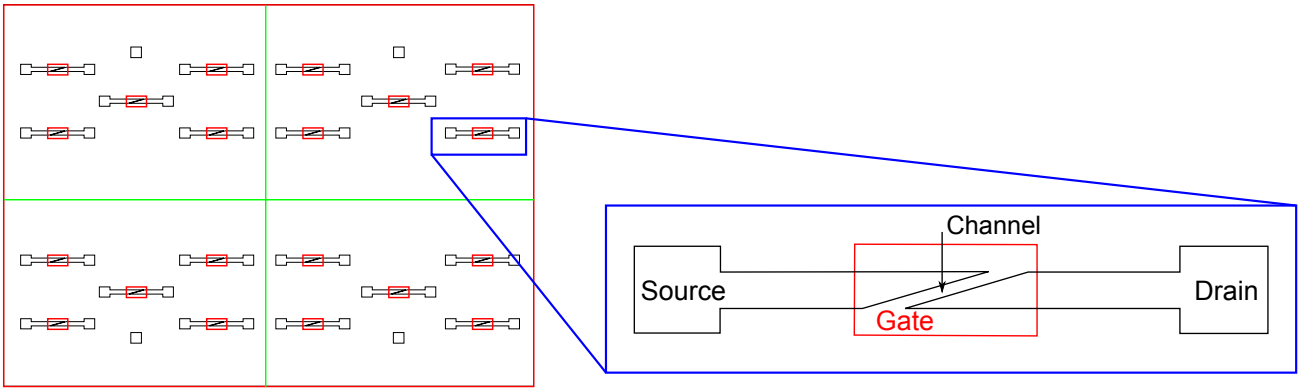

Figure 3.6: Masks for the top-gate source-drain structure and the gate structure displayed in black and red, respectively. The substrate is cut along the green lines into four samples. It also shows an enlargement of the super-imposed masks of one top-gate transistor.

ITO contact pads were transferred to the evaporation chamber were 40 nm thick Au source and drain structures were applied. They define a channel with a length of 54 µm and a width of 1520 µm. Au was applied via a standard physical vapor deposition (PVD) process in an ultra high vacuum (UHV) chamber at a pressure of $<10^{-6}$ mbar. The metal is heated via Joule heating until it starts to evaporate. The oscillating quartz crystal measures the rate of deposition in Å/s and the amount of deposited material in nm if the shutter above the evaporation boat is opened. When the deposition rate has reached the desired value, the shutter below the sample holder containing the sample can be opened and the deposition of the material onto the substrate starts. If the desired thickness is achieved the shutter is closed again. Typical metallic film thickness values are 40 nm and deposition rates are 2.0 Å/s. The noble metal Au was used because it does not oxidize and is stable against the acidic precursor solution. In addition, it sustains the annealing step at 500 °C. After the processing of ZTO either by spin coating or ink-jet printing the organic dielectrics are applied. They are applied by spin coating and drying as presented in the next subsection. The final device was obtained by thermal evaporation of 40 nm of Au top-gate electrode in the evaporation chamber. A representation of this staggered top-gate transistor is displayed as a cross-section representation in **Figure 3.7** (a) and as a top view image of the channel region in **Figure 3.7** (b).

Organic dielectrics

In the top-gate configuration organic dielectrics were applied. Now these polymeric materials will be presented. PMMA was mainly used as the organic dielectric for top-gate transistors throughtout this thesis. PMMA shows good thermal and mechanical resistance and exhibits an electric resistivity ex-

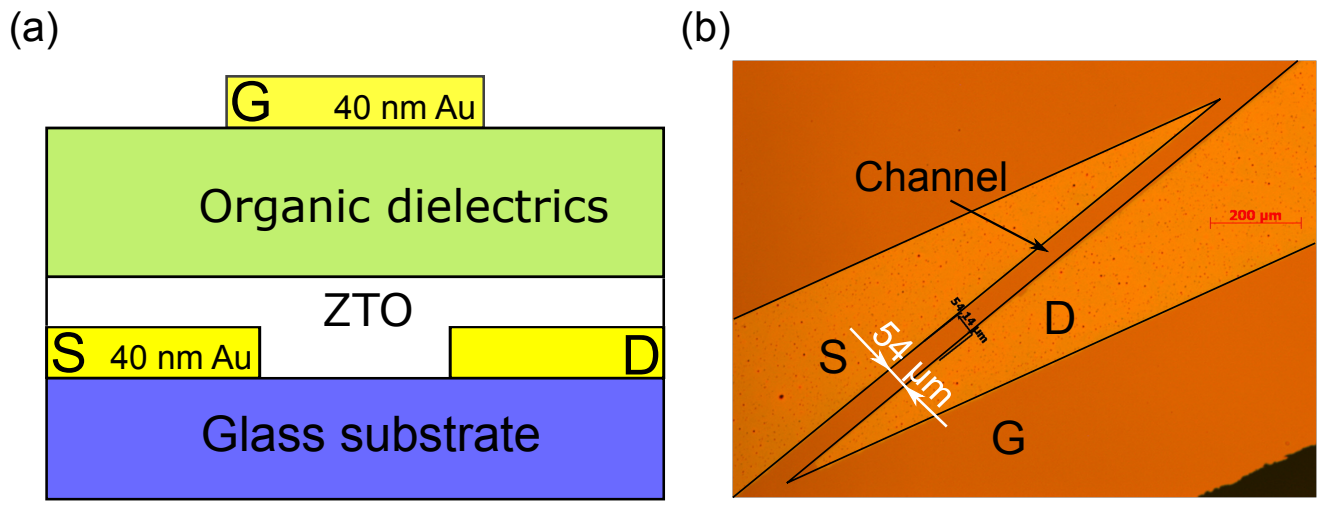

Figure 3.7: Cross-sectional illustration of the staggered top-gate layout used (a). Top view image of the channel region with labeling of the three electrodes (b).

ceeding $2{\cdot}10^{15}$ Ωcm [74]. The structural formula of PMMA also known under its industrial brand name PLEXIGLAS® can be seen in **Figure 3.8**. According to Kawamoto *et al.* [21] it exhibits the following values for the band gap, the work function, and the ionization energy: $E_g = 4.8$ eV, $\Phi = 5.0$-5.2 eV, and $E_{\text{ion}} = 8.1$ eV.

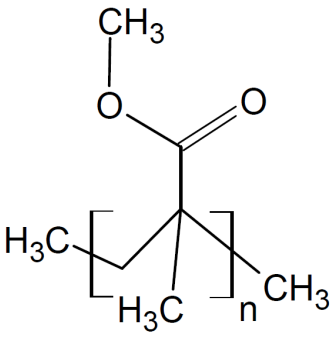

Figure 3.8: Structural formula of poly(methyl methacrylate) (PMMA).

The utilized PMMA 7N granulates were purchased from Evonik Performance Materials GmbH and have a molar mass of 94.000 g/mole. PMMA solutions were produced by dissolving 6 or 10 wt % of PMMA in *n*-butyl acetate ($H_3C{-}CO{-}O{-}C_4H_9$) purchased from Sigma-Aldrich, then stirring the mixture for at least 15 hours at 70 °C in a glove box. After filtering using a 0.2 µm PTFE filter the final solution was obtained and left stirring on a stirring plate. Thin PMMA layers were obtained by spin coating the final solution at various spinning speeds and drying the films at 110 °C for 10 min on a hotplate. This temperature was selected because it is above the glass transition temperature T_G of PMMA of 105 °C and below its melting point of 160 °C.

Another polymeric dielectric used was PS with a T_G of 100 °C, purchased from BASF SE. Solutions in *n*-butyl acetate are prepared in the same manner as the PMMA solutions. The solution is applied

similarly to the PMMA solution by spin coating and drying at 110 °C for 10 min on a hotplate. The structural formula of PS is displayed in **Figure 3.9**. The following electronic levels were reported for PS: $E_g = 4.1$ eV [75], $\Phi = 5.0$-5.4 eV and $E_{ion} = 8.1$ eV [21].

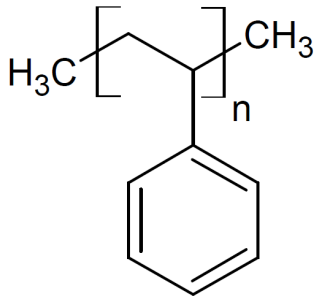

Figure 3.9: Structural formula of polystyrene (PS).

The so called PAZ was applied as a third organic dielectric. It was developed by the Fraunhofer Institute for Applied Polymer Research in Potsdam and its insulating propertiers were evaluated by the Electronic Materials Division group at the Technische Universtiät Darmstadt. How it is synthesized and information on this dielectric can be found in the publication of Simas *et al.* [76]. **Figure 3.10** displays the structural formula of the PAZ copolymer before crosslinking. It is composed of three blocks namely a styrene block (k), a 4-vinylbenzyl nitride block (l), and a methyl methacrylate block (m). Two different version of the PAZ exist. The PAZ 12 contains no styrene block, 12 mol% of the 4-vinylbenzyl nitride block, and 88 mol% of methyl methacrylate block and the PAZ 14 contains 45 mol% of the styrene block, 14 mol% of 4-vinylbenzyl nitride block, and 41 mol% of methyl methacrylate block. The polymers were dissolved in *n*-butyl acetate and processed by spin coating. The cross-linking reaction of both copolymers took place by drying the films at 250 °C for 10 min on a hotplate. In order to achieve denser films a double layer approach was used.

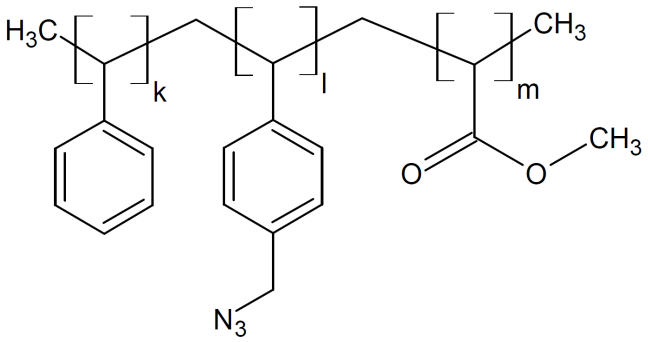

Figure 3.10: Structural formula of the PAZ copolymer containing a styrene block (k), a 4-vinylbenzyl nitride block (l), and a methyl methacrylate block (m).

3.4 Thin film characterization techniques

In this section the thin film characterization techniques will briefly be presented. Before thin films were produced the precursor solution could be analyzed using thermogravimetric analysis (TGA). Information about the topography of the ZTO films has been obtained by atomic force microscopy (AFM) and scanning electron microscopy (SEM). The crystal structure of ZTO was investigated by X-ray diffraction (XRD) and transmission electron microscopy (TEM). The thickness of the solution processed thin films was measured by profilometry. The important parameters band gap, valence band offset, and work function of ZTO have been determined using the methods of ultraviolet-visible (UV-Vis) spectroscopy, X-ray photoelectron spectroscopy (XPS), and ultraviolet photoelectron spectroscopy (UPS), respectively.

Thermogravimetric analysis

The method of TGA will be introduced at this point summarizing information given by the book of Skoog and Leary [77]. TGA is widely used for the determination of melting points of metals or glass transition temperatures of polymers. With the help of this method one can determine physical changes of the sample as melting, sublimation, oxidation or decomposition. During a TGA experiment the mass of a sample is monitored while it is heated at a constant rate under a specific atmosphere. The machine consists of a precise scale and an oven, a flushing system for various gases and a computer in combination with a controlling software. Around 20 mg of a sample is put into an aluminum crucible which is positioned on the scale. A change of the sample weight manipulates a connected shutter that diminishes the light intensity. This change in light intensity can be detected with the help of a photo diode in combination with an amplifier. The detected photo-current reveals a mass gain or mass loss. This change of mass as a function of temperature is then plotted. A TG209F1-Iris scale from Netzsch was used for the TGA measurements of this thesis.

Atomic force microscopy

The working principle of an AFM is illustrated in **Figure 3.11**. With the help of an AFM information about the topography and roughness of a sample can be obtained. The tip, which probes the surface of the sample, is attached to a cantilever. The force between the sample surface and the tip deflects the cantilever. The deflection of the tip is detected by a LASER and a photo diode during the scan of the sample surface in the x- or y-direction which produces an AFM image.

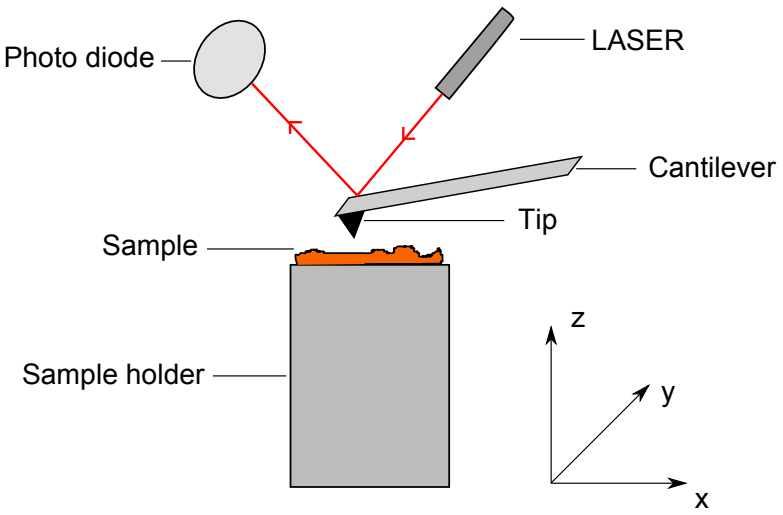

Figure 3.11: Illustration of the working principle of an AFM.

There are four different basic operational modes. The contact and non-contact mode and the static and dynamic mode. The AFM used in this thesis works in non-contact and dynamic mode. Therefore only these two modes will be described briefly by referring to the publication of Meyer [78]. If an AFM is working in non-contact mode the distance between the surface of the sample and the tip is on the order of tens of nm and information about the topography of the sample (z-direction) can be received. Dynamic mode means that the cantilever is vibrating near to its resonance frequency. It should be mentioned that attracting forces destabilize and decrease the resonance frequency whereas repulsive forces stabilize the motion of the cantilever and increase the resonance frequency. During the scan the frequency is kept constant and the variation of the amplitude is detected. Investigations of the topography were carried out using an Asylum research MFP-3D microscope and HQ:NSC19/AlBS tips. The obtained images were analyzed with the help of the open source software Gwyddion. This software was applied to level and remove the noise from the raw data. The most important parameter extracted by this software is the root-mean-square roughness R_q. It is determined from the complete AFM image and calculated using **Equation 3.6** [79].

$$R_q = \sqrt{\frac{1}{N}\sum_{j=1}^{N} r_j^2} \tag{3.6}$$

Scanning electron microscopy

Micrograph information of the ZTO surfaces can be obtained with the help of SEM. How it works will briefly be presented by referring to the book of Skoog and Leary [77]. The microscope can be divided

into three main parts, where all parts have to be kept under UHV. The first part is the electron gun, the second part is the focusing part, and the third part is the sample chamber containing the sample, sample holder, and the detectors. In the electron gun the electrons are generated and accelerated. In the second part the electron beam is condensed and focused by electromagnetic lenses and in the third part the electron beam scans the sample surface and the sample signals are collected by detectors. The electron gun consists of a metallic filament, a Wehnelt cylinder, and an anode. The thin metallic filament, widely made out of tungsten, is heated to a temperature close to the melting temperature in order to create free electrons. These free electrons are then accelerated towards the anode by applying a voltage of up to 50 kV. Only the fastest electrons can pass the negatively charged Wehnelt cylinder. In the second part of the microscope condenser lenses are applied for the de-magnification of the electron beam and objective lenses are used for a final focusing of the beam on the sample. Two other lenses within the objective lens are used to scan the sample surface in the x- and the y-direction. In this way a topological signal as a function of the x- and y-position can be obtained. If the electron beam hits the surface of the sample several interactions may occur. The most important one is the creation of secondary electrons (SE). They are a result of the inelastic scattering of the primary electrons with the surface electrons of the sample at a depth between 0.5 and 5 nm. The sample electrons gain enough energy to leave the sample because of energy transfer. These secondary electrons are then collected using a detector consisting of a scintillator, a photo cathode, and a photo multiplier. The scintillator creates light after electron bombardment, which is sent to a photo multiplier. The signal enhancement is around 10^5. The SE signal is very sensitive to the surface and therefore gives information of the surface topography. An element specific micrograph of the sample can be obtained if backscattered electrons (BSE) are analyzed. These BSE occur after the elastic scattering of the primary electrons with the nuclei of the sample up to a depth of 1.5 µm. They can be detected by a pn-junction detector. For the characterization of the ZTO thin films a FEI Quanta 200F microscope was used.

X-ray diffraction

With the help of XRD one can gain access to crystallographic information of a sample. The diffraction of an X-ray beam on a crystal can be simplified to the diffraction of an X-ray beam at lattice planes of a crystal. A monochromatic X-ray beam hits an ordered lattice with the distance d between the lattice planes under an angle Θ (**Figure 3.12**). Constructive interference can only be detected if the wavelength λ of the X-ray beam multiplied by an integer n is equal to the additional travel length d times sin Θ. n is called the order of diffraction and it is an important factor in Bragg's law of diffraction (**Equation 3.7**) [80].

$$n\lambda = 2d\sin\Theta \tag{3.7}$$

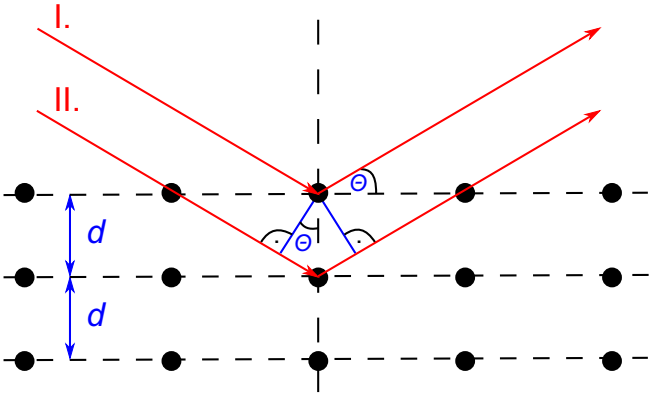

Figure 3.12: Diffraction of an X-ray beam by an ordered crystal with a lattice distance d. Constructive interference does only occur when the additional travel length of beam II $2d\sin\Theta$ is an integer n times the wavelength λ of the X-rays according to Bragg's law of diffraction (**Equation 3.7**).

The thickness of the solution processed ZTO films is very small measuring a couple of tens of nanometers. Normally an XRD experiment gives information about the bulk of the sample. In order to characterize the surface of a sample, grazing incident X-ray diffraction (GIXRD) can be used. In GIXRD the incoming X-ray beam hits the sample at a constant incidence angle Ω which is typically smaller than 5 °. The GIXRD investigations were carried out on a Seifert PTS 3003 X-ray machine utilizing Cu K_α radiation.

Transmission electron microscopy

A TEM was applied to examine the microstructure and phases of thin films of ZTO. Here its working principle will shortly be presented. In a UHV column the high energetic electron beam is focused on the very thin sample with the help of electromagnetic lenses. Since the thickness of the sample is on the nm scale the electron beam passes the sample and can be detected. The TEM operates on the same basic principle as a light microscope but uses electrons not photons leading to a higher resolution. The glass lenses of a light microscope are replace by electromagnetic lenses. In **Figure 3.13** the main parts of a TEM are illustrated.

The electron gun (1) contains the filament, which is heated by high currents in order to produce free electrons. Tungsten is mainly used as the filament material. These free electrons are then accelerated by a high voltage. In order to select the electrons with the highest speed a so called Wehnelt cylinder is used. It is negatively charged to let only the fastest electrons pass. The condenser lenses (2) reduce the size of

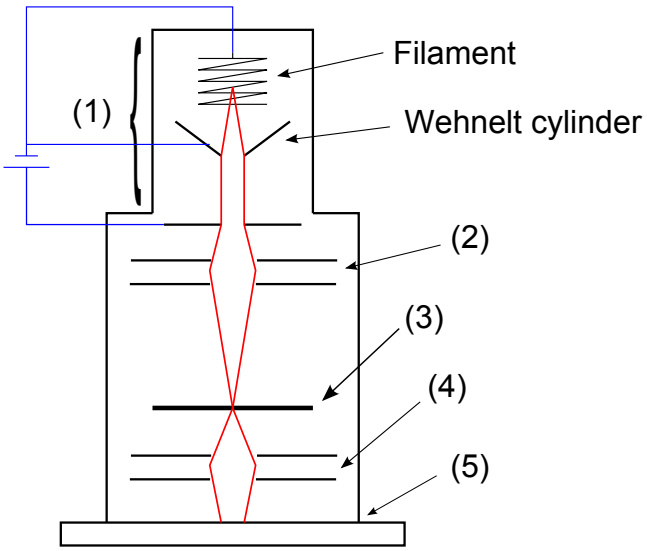

Figure 3.13: Working principle of a TEM. The electron gun (1) contains the filament which is heated by high currents to create free electrons. These are accelerated by high voltages through the negatively charged Wehnelt cylinder towards the anode. The electron beam is focused onto the sample in the sample holder (3) using the condenser lenses (2). The projection lenses (4) magnify the image on the detector (5).

the electron beam and focus it on the sample, which is placed in the sample holder (3). The objective lens focuses the resulting image after the beam has passed through the sample towards the detector (5). The projection lens (4) is there to magnify the image. These elements create an image of the sample which is formed on the detector. For the structural analysis of the ZTO film a FEI Talos F200X microscope at 200 kV located at the ETHZ was used.

UV-Vis measurement

Absorption spectroscopy in the visible and ultraviolet region of the electromagnetic spectrum can be applied to obtain information about the absorption of the analyzed material and to determine its band gap. Its measurement principle will now briefly be presented by referring to the book of Skoog and Leary [77]. For these measurements a lamp with a continuous light intensity over a broad wavelength range is necessary. The electrical excitation of hydrogen or deuterium can be used for the UV range between 160 to 375 nm. For longer wavelengths from 350 to 2500 nm a tungsten lamp is applied. These lamps are powered by a precise DC power supply to guarantee a stable light intensity. The produced light passes a wavelength selector before it strikes the reference or sample. The photo detector collects the transmitted light signal. Three measurements are necessary to obtain the final transmitted signal of the sample. First a transmission measurement if a blend structure blocks the incoming light has to be performed. Then a quartz glass substrate as the reference has to be measured. Finally a quartz glass substrate covered with ZTO has to be measured. The quartz glass substrate was used because the standard

glass substrate absorbs in the visible region. The transmission T of this substrate was measured between a wavelength λ of 200 and 800 nm. Its absorption A was then calculated according to $A = 2 - \log(T)$. Then the transmission of the ZTO film on the substrate was measured and A was calculated accordingly. Finally the absorption of the ZTO film was obtained after the subtraction of the two values. The UV-Vis measurements were performed using a PERKIN ELMER Lambda 900 spectrometer. In 1966 Tauc and colleagues reported a method to extract the band gap out of the results of an absorption measurement [81]. In this Tauc plot the expression $(\alpha h\nu)^2$ is plotted against the photonic energy $E_{ph} = h\nu$. The exponent 2 has to be used if a direct band gap is expected. The absorption coefficient α is thereby defined as $\alpha = -\frac{\ln(T)}{d_l}$ with d_l being the thickness of the analyzed layer.

Profilometry

The profilometer operates according to electromechanics [82]. **Figure 3.14** illustrates the working principle behind this device. A needle moves with a constant force and velocity along the layer. On top of the needle is a tip made out of diamond with a radius of around 10 µm. The force can be varied between 0.01 and 0.15 mN. With the help of the so called linear variable differential transformer (LVDT)-sensor the vertical deflection of the needle can be measured. Consequently, an altitude profile can be obtained. The sensor is composed of one primary coil, two secondary coils, and a core made out of soft iron. The core is connected to the needle. Its position compared to the combination of coils defines the magnetic flux, which acts between the primary and the secondary coil. If an AC bias signal is applied at the primary coil an AC bias signal is induced at the secondary coil. Because these signals can be measured precisely the deflection of the needle can be determined. An average of the layer thickness can be determined if multiple scans along the edge of the deposited material or over a scratch in the organic dielectrics are performed. For this thesis a Bruker Dektak XT was used.

X-ray and UV photoelectron spectroscopy

The two surface analysis methods XPS and UPS are presented briefly referring to the book 'Photoelectron Spectroscopy' written by Hüfner [83]. Both methods work according to the photoelectric effect. Photons with an energy greater than the binding energy of the electrons hit the sample. During the interaction element specific core electrons can be removed from the sample. These electrons can either directly leave the sample which are detected as the normal XPS signal or Auger electrons are created as a two electron process. Latter occur if electrons from an outer shell refill the created hole due to irradiation and the released energy is utilized to eject an electron from an outer shell. These Auger electron sig-

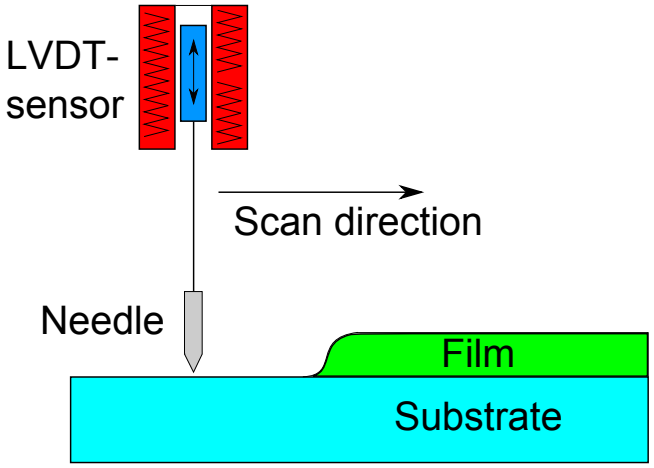

Figure 3.14: Scheme of the working principle of a Dektak 8 device, containing the needle and the LVDT sensor.

nals can overlap with the signal from the photo electrons. **Figure 3.15** shows a scheme of the energetic conditions in an XPS experiment.

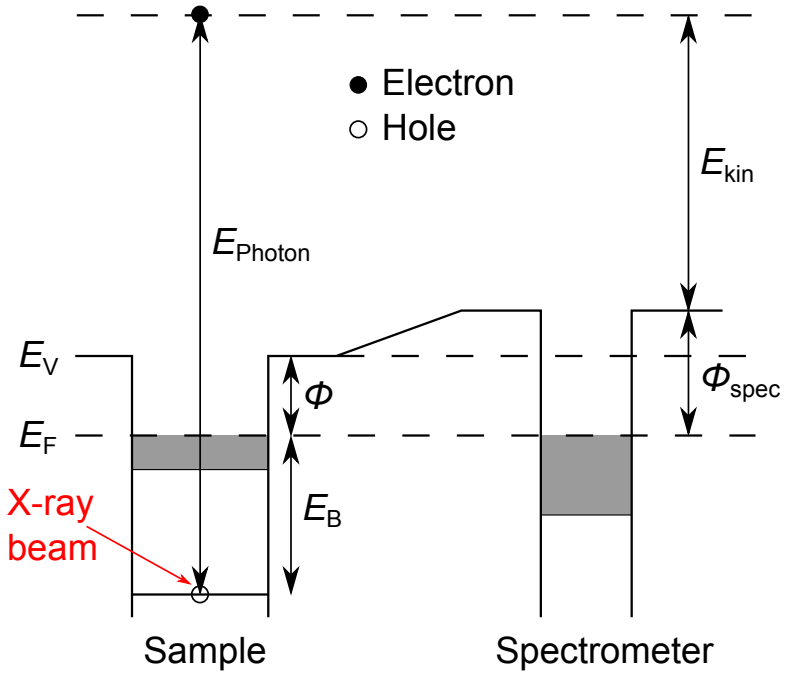

Figure 3.15: Scheme showing the main parameter in an XPS experiment. The X-ray beam with a known photonic energy E_{Photon} leads to the extraction of a core electron with a binding energy E_B. The electron leaves the sample with a kinetic energy E_{kin} which can be measured by the spectrometer using **Equation 3.8**. Φ and Φ_{spec} are the work function of the sample and the spectrometer, respectively.

X-ray photons with an energy of E_{Photon} extract electrons from the core level with a binding energy of E_B. The kinetic energy E_{kin} of these photo electrons can be determined using **Equation 3.8**.

$$E_{\mathrm{kin}} = E_{\mathrm{Photon}} - E_{\mathrm{B}} - \Phi_{\mathrm{spec}} \tag{3.8}$$

$E_{\mathrm{Photon}} = h\nu$ is the photonic energy of the incident photons, E_{B} is the binding energy of the core electrons, and Φ_{spec} is the work function of the spectrometer. The last term can be canceled out electronically. For the XPS measurement a aluminum (Al) K_α source (50 W, 15 kV) with an energy of 1486 eV and a spot size of 200 µm in diameter was applied.

The work function of thin films is normally determined by UPS. The sputtered thin film was illuminated by helium (He) 1 atoms having an energy of $E_{\mathrm{Photon}} = 21.2$ eV. The work function can be obtained from **Equation 3.8** if one takes into account that the slowest electrons have a kinetic energy of zero at the edge of the secondary electrons (SK) in **Equation 3.9** [84]. The determination of the work function in an UPS experiment is illustrated in **Figure 3.16**. The UPS spectrum can be measured if a external bias signal is applied in order to extract the electrons from the sample and to determine the work function of the sample from the known work function of the spectrometer. For the XPS/UPS measurements were conducted with a setup from the company 'Physical Electronics'.

$$\Phi = E_{\mathrm{Photon}} - E_{\mathrm{B(SK)}} \tag{3.9}$$

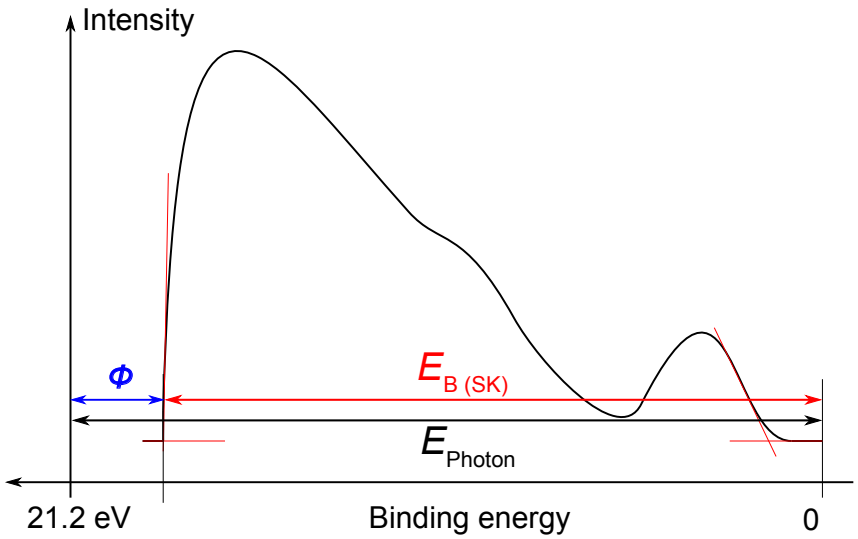

Figure 3.16: Determination of the work function Φ using UPS and **Equation 3.9**.

3.5 Electrical characterization

In this section it will be explained how the transistors were characterized electrically. In the first subsection it will be shown how the *I*-*V*-characteristics were obtained. The electrical stress measurements are presented in the next subsection. In the third subsection it will be illustrated how the switching times of transistors can be measured. The impedance measurements are presented in the last subsection.

Measurement of *I*-*V*-characteristics

As already explained in the theory section of this thesis the field-effect transistor is a three terminal device. These three electrodes have to be contacted with tungsten needles. A voltage difference is applied between the source-gate and the source-drain electrodes keeping the source electrode grounded. All electrodes were connected to a semiconductor parameter analyzer via BNC coaxial cables. For the measurement of the transistors built on FH substrates the analyzer 4155C from Agilent was used. The top-gate transistors were electrically characterized using the analyzer 4155A from Hewlett Packard. The probing of the electrodes took place in a N_2 filled GB in order to cancel the possible effects of H_2O and O_2 on the transistor performance if not stated otherwise. Now the procedure for measuring the current between source and drain (drain-currents I_D) and between source and gate (gate-currents I_G) of the the two layouts will be presented. I_D and I_G were measured simultaneously in both cases. The main interest is in the evolution of the drain-currents, but also the gate-currents can reveal insight on the leakage behavior of the dielectric. Values of drain-current are only trustworthy if they are at least 100 times larger than the corresponding gate-currents. The transfer characteristics for the transistors built on FH substrates were obtained by sweeping the source-gate voltage from -5 V to 30 V keeping the source-drain voltage constant at 30 V. The 30 V value for V_{DS} was applied to measure transfer characteristics in the saturation regime. The corresponding output characteristics were measured by sweeping the source-drain voltage from -5 V to 30 V at constant source-gate voltages of 0, 10, 20, and 30 V. The output characteristics for a V_{GS} of 0 V gives information about the intrinsic conductivity of the analyzed semiconductor. The measured drain current can be written as $I_D = ne/t$ giving $n = I_D t/e$. If this expression for n is introduced in the formula $\sigma = \mu ne$ a direct proportionality between the conductivity and the current is obtained ($\sigma = \mu I_D t$). The voltage sweep for the transfer and the output characteristic were measured in 0.5 V or 1.0 V steps. All characteristics were recorded in both directions, meaning a forward and back sweep of the applied sweeping bias. By using this measurement condition a hysteresis between both scan directions may occur which gives information about electronic trap states in the channel region of the transistor. The transfer characteristic of the top-gate transistors was measured by sweeping V_{GS} from -10 V to 60 V keeping V_{DS} at 40 V or 60 V. The output characteristic was obtained by sweeping V_{DS} from

-5 V to 60 V at constant V_{GS} values of 0, 20, 40, and 60 V. In this case higher voltages had to be applied than for the FH substrates in order to accumulate sufficient charges due to the larger thickness of the organic dielectrics than the SiO_2 layers. The step size for the voltage sweep for both characteristics was 1.0 V. The electrical measurement took place in a N_2 filled GB if not stated otherwise. The obtained *I-V*-characteristics can be used to extract the main transistor parameters by applying the Shockley equations **2.4** and **2.5** or rather the adapted **Equations 2.6** and **2.7**.

Electrical stress measurement

Electrical stress measurements of transistors built on FH substrates were conducted and performed in air. The source and drain electrodes were hereby connected and grounded. Then a positive bias of +30 V was applied at the gate electrode for a certain time using the semiconductor parameter analyzer HP 4155A. This stress measurement is labelled positive bias stress (PBS). After 0, 30, 90, 210, and 510 s of gate bias stress the transfer characteristics were recorded with the help of the HP 4155A. The most important result of such a stress measurement is the maximum shift of the threshold voltage ΔV_{th}. The results from these stress measurements were also reported in the literature [85, 86, 16].

Time dependent measurement

Apart from the charge carrier mobility of a transistor the rise time, or the time needed to turn the transistor from its off-state to its on-state, is an important parameter too. In order to access this parameter, time dependent measurements of printed ZTO transistors on FH substrates were performed in air using the setup displayed in **Figure 3.17** and **Figure 3.18**.

To ensure a better electronic contact, the Si gate electrode was treated for this measurement since it exhibits a native SiO_2 layer [87, 88]. First the native SiO_2 layer was scratched away inside a GB using a pen with a diamond tip. The scratched surface was then covered with a silver paste (AUROMAL from DODUCO GmbH). The source electrode was grounded during the measurements. Between the source and gate electrode a voltage pulse in form of a step function was applied beginning at time $t = 0$ s. For the charging measurement of the capacitor, which is composed of the areal gate electrode and the interdigitated source/drain structure including the ZTO layer, no voltage signal ($V_{DS} = 0$ V) was applied at the source and the source and drain electrode were connected as shown in red in **Figure 3.17**.

In order to determine the switching speed of the transistors a positive bias V_{DS} was applied at the source. Using an oscilloscope with an internal resistance of 1 MΩ the time dependence of the voltage at the drain electrode was measured. In order to allow for a faster signal at the oscilloscope a resistor of 1 kΩ is introduced in parallel to the large internal resistance of the oscilloscope.

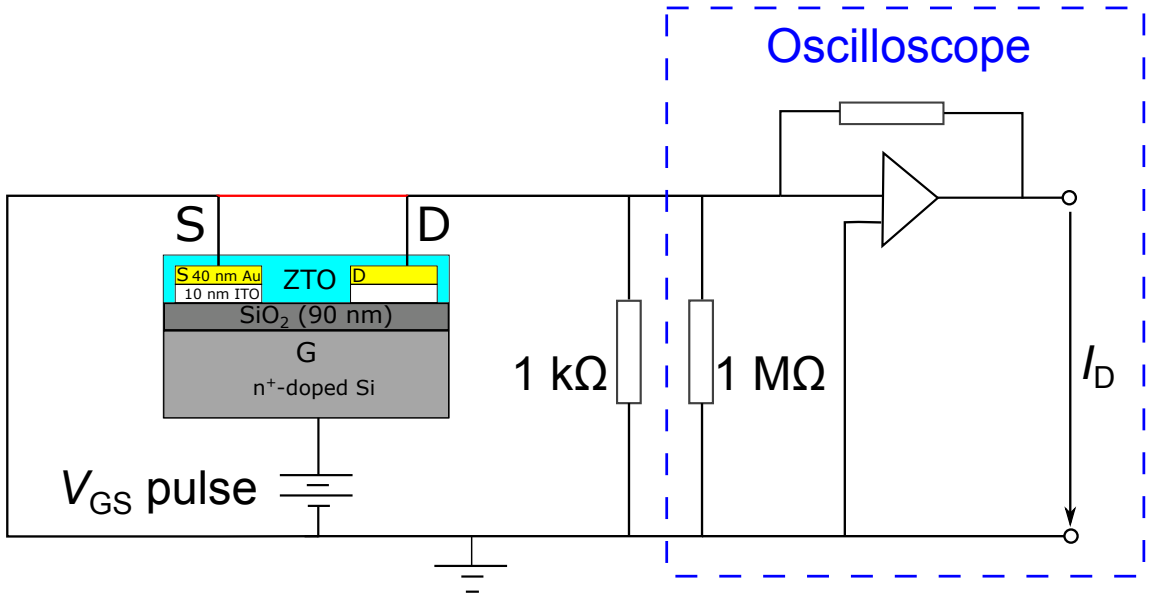

Figure 3.17: Setup of the measurement circuit for the time dependence charging of the capacitor consisting of the n-doped Si gate electrode, the 90 nm thick SiO_2 dielectric, the ZTO film, and the ITO/Au source and drain structures. Using a pulse generator HP 8114A in combination with a function/arbitrary waveform generator HP 33120A a voltage step function was applied at time t = 0 s to the gate electrode. The source and drain electrode were grounded. The time dependent drain signal was measured using a Tektronix TDS 5052 B digital phosphor oscilloscope displayed within the dashed blue box. A faster signal at the oscilloscope was obtained if a resistance of 1 kΩ was introduced parallel to the internal resistance of 1 MΩ of the oscilloscope.

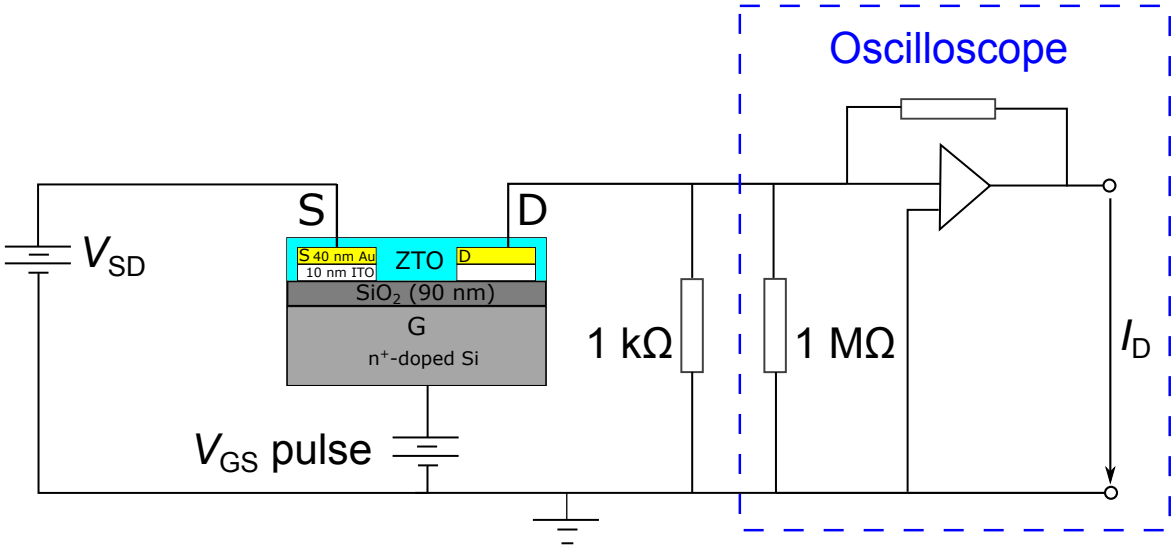

Figure 3.18: Adapted setup for the time dependent measurement of printed ZTO transistors on FH substrates. At the source electrode a constant bias was applied by means of a laboratory power supply PS-2403D from Conrad Electronic SE.

In order to obtain the rise time of the analyzed transistors two measurements have to be performed. First the drain current I_D for $V_{DS} = 0$ V as a function of the V_{GS} voltage pulse has to be measured. This signal

represents the charging of the capacitor consisting of the n-doped Si gate electrode, the 90 nm thick SiO_2 dielectric, the ZTO film, and the ITO/Au source and drain structures. Secoundly the I_D current at a constant V_{DS} has to be recorded. The final curve, which represents the filling of the transistor channel with electrons, can be obtained by subtracting the pure capacitive current from the current under V_{GS}-bias according to the literature [89, 90]. **Figure 3.19** illustrates this approach. The black curve represents the utilized voltage pulse applied at the gate electrode. A value of 30 V is applied for 30 µs. The charging of the capacitor with $V_{DS} = 0$ V is displayed as the green curve (I). The red curve shows the measured signal for $V_{DS} = 30$ V applied between source and drain electrode (II). The time for switching the transistor 'on' or 'off' can be determined from the blue curve. This curve was obtained by subtracting the green from the red curve (II-I). Here only the 'on' switching behavior was investigated.

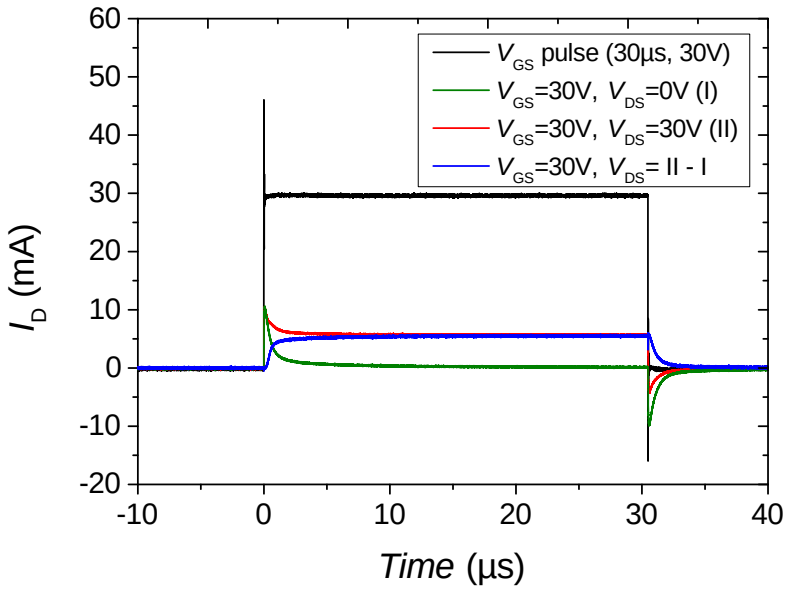

Figure 3.19: Current-time diagram showing the rectangular pulse (30 µs, 30 V) applied at the gate (black curve), the charging response of the capacitor (green), the measured drain signal if an additional $V_{DS} = 30$ V is applied (red curve), and the blue curve. The last mentioned curve is the result of the subtraction of the green from the red curve.

In order to fit the blue curve of **Figure 3.19** a double exponential function was applied. The overall fitting curve can be described by **Equation 3.10** and a representation of the curve can be seen in **Figure 3.20**. In contrast to the publication of Nasr *et al.* [90] where a single exponential function for fitting the measurement data could be used, a double exponential function had to be applied to fit the measurement results reported in this thesis. The measured curves had to be shifted by a time offset t_0 in order to obtain a rise of the signal at $t = 0$ s. This time interval is necessary to fill the channel from source and drain electrode with electrons [91].

$$I_D = \begin{cases} 0 & \text{for} \quad t < t_0 \\ I_1 \left[1 - \exp\left(-\frac{t-t_0}{\tau_1}\right)\right] + I_2 \left[1 - \exp\left(-\frac{t-t_0}{\tau_2}\right)\right] & \text{for} \quad t \geq t_0 \end{cases} \tag{3.10}$$

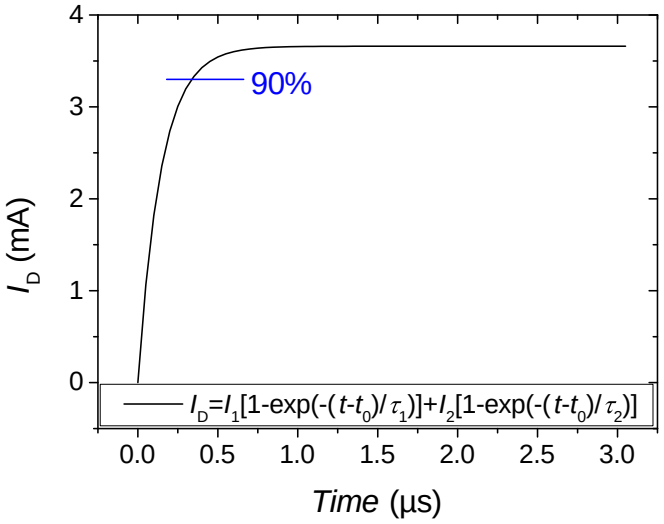

Figure 3.20: Representation of a double exponential fitting curve applying **Equation 3.10**.

The switching time to turn the transistor 'on' is the sum of two time constants τ_1 and τ_2. The short time τ_1 could represent the time that is necessary to move the injected electrons towards the drain electrode. The long time constant τ_2 could display the time that is necessary to move the trapped electrons towards the drain electrode. The switching time can be defined as the time which is required to increase the current to 90 % of its saturated value [3].

Impedance spectroscopy

In order to characterize the quality of the various organic dielectric layers, impedance spectroscopy measurements were performed. **Figure 3.21** represents the layout for the metal-insulator-metal (MIM) diode structure used for impedance spectroscopy measurements.

It consists of a glass substrate, that has been covered with a 100 nm thick ITO layer as a bottom-electrode. This ITO covered glass substrates were purchased from VisionTek Systems Ltd. (Chester, GB). Then the organic dielectric materials were applied by spin coating and drying as described in section 3.3. The MIM diode, that is highlighted in red, is finalized by the thermal evaporation of a 50 nm thick top Au electrode. The area of the active diode is 0.09 cm^2. The organic dielectric had to be scratched away in certain areas in order to contact the ITO bottom-electrode. These diodes were then measured within a N_2 filled GB using an impedance analyzer Solartron SI1260 in combination with a Solartron 1296 dielectric interface. The ITO bottom-electrode with a work function of 4.6 eV [22] was connected to the negative

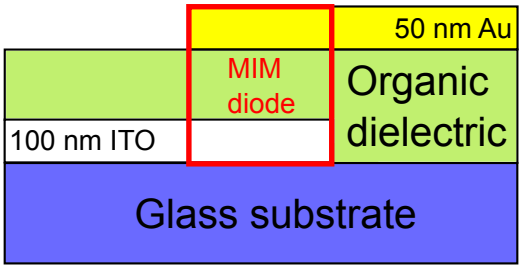

Figure 3.21: Representation of the processed metal-insulator-metal (MIM) diode layout using a glass substrate covered with 100 nm of ITO, spin coated organic dielectric and a 50 nm thick top Au electrode.

output and the Au top-electrode with a slightly higher work function of 5.3 eV [92] was connected to the positive output of the dielectric interface. The real and imaginary part of the impedance (I_r & I_i) as well as the capacitance (C_r & C_i) were measured as a function of the frequency between 1 Hz and 1 MHz in 10 steps per decade. During the AC measurement a DC bias signal of 0 V and a AC signal of 0.5 V was superimposed. The dielectric constant ε_r of the organic dielectric can be determined by using the classical formula for a plate capacitance $C = \varepsilon_r \varepsilon_0 A/d$. C is the capacitance, ε_0 the permittivity of vacuum, A the area of the capacitor, and d its thickness. Using a C value at a high frequency of 10^4 Hz the dielectric constants of the various organic dielectrics could be calculated as proposed by Simas *et al.* [76]. Another important parameter which can be determined from an impedance measurement is the loss factor tan δ. It is a measure of how much electric energy is destroyed by the dielectric and it gives information about the quality of the dielectric films. The loss factor is calculated by dividing the imaginary by the real part of the capacitance according to this expression: $\tan \delta = \frac{C_i}{C_r}$ [93].

4 Results and discussion

In this chapter the results of the research will be presented divided into seven sections and discussed. The first section deals with the investigation of the precursor decomposition and presents results from the thin film characterization. In the following section effects of the precursor route on bottom-gate transistors will be introduced. The third section discusses the results of the investigation of multiple-layer effects on printed bottom-gate transistors. The fourth section gives information about how fast solution processed transistors can be switched to the on-state. In the following section the results of transistors processed at a reduced annealing temperature are presented and discussed. In section 4.6 the effects of the atmosphere on the transistor performance is shown. In the final section of this chapter the results of the organic/inorganic ZTO top-gate transistors are presented. In all images the number of processed ZTO layers and their processing method, either spin coating or ink-jet printing, is indicated.

4.1 Results of thin film characterization

In this section the results of the precursor decomposition and thin film characterization are presented and discussed. The decomposition analysis of the precursor solution was performed by TGA. Information about the morphology of thin films was obtained by AFM and SEM. XRD and TEM results reveal the nanocrystalline structure of ZTO. The electronic properties such as band gap, valence band offset, and work function of ZTO were obtained by UV-Vis absorption and XPS/UPS measurements.

First the temperature necessary for the complete decomposition of the precursor was investigated. The TGA investigation was carried out by Dr. Hoffmann of the department of Prof. Dr. Jörg J. Schneider at the Technische Universität Darmstadt. In order to obtain the sample for the TGA analysis 5 mL of the precursor solution described in section 3.1 was dried in a vacuum oven at 110 °C for 16 h in order to remove the solvent. **Figure 4.1** shows the loss of mass of such a dried powder if heated at a rate of 10 °C/min at a constant O_2 flow rate of 40 mL/min up to 600 °C. The first pronounced mass loss starts already at 50 °C and is a result of the removal of solvent which was stored in pores within the powder. This loss only leads to a 5 % reduction of the initial mass. Then there follows a constant loss of mass until 370 °C followed by a large mass loss from 87 % to 55 %. The large loss of mass is due to the decomposition of the precursor and the transformation to the oxide state. This decomposition starts at 400 °C [94] for the nitrates according to the equation $Zn(NO_3)_2 \longrightarrow ZnO + NO_2 + NO + O_2$ [95]. The mass loss for this reaction is 13.0 % which can not entirely explain the observed mass loss

of 32 %. The additional mass loss can be attributed to the decomposition of the tin chloride [96]. This decomposition is the result of six different steps as reported by Al-Gaashani *et al.* [97]. Since the complete decomposition of the precursor salts is completed at around 500 °C, this temperature was used as the annealing temperature throughout this thesis.

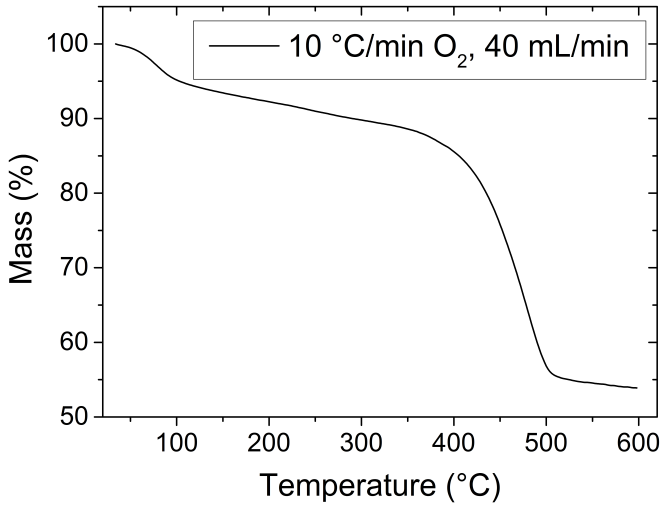

Figure 4.1: TGA result of a dried ZTO solution at a heating rate of 10 °C/min and an O_2 flow rate of 40 mL/min. It shows two main mass loss signals at around 100 °C and between 400 and 500 °C.

Now the results of the topography of spin coated and ink-jet printed ZTO films will be presented. Thin films were processed via spin coating (5000 rpm, 30 s) of a ZTO precursor solution of 0.3 mol/L. As substrates an ozone treated (15 min) Si substrate with a 230 nm thermally grown SiO_2 layer and a glass substrate object holder were utilized. Both films were first dryed at 90 °C for 10 min in order to evaporate the solvent and then annealed at 500 °C for 60 min in an air filled oven. **Figure 4.2** shows AFM images of an area of 5x5 µm, displaying the film topography on Si (a) and on glass (b). The root mean square (rms) roughness and the average grain size were determined to be 2.45 nm and 5.98 nm for ZTO deposited on SiO_2. If ZTO was deposited on glass these values were determined to be 2.06 nm and 6.49 nm, respectively. Both topographic images show a clear particle-like structure of the ZTO independent of the substrate used. This structure is typical of solution processed ZTO and has been widely reported and discussed in the literature [98, 99, 57]. They report spin-coated ZTO films with rms values ranging between 1.91 and 8.55 nm.

Figure 4.3 displays an AFM image on an area of 5x5 µm of a printed thin ZTO film. It was produced by ink-jet printing one layer of 0.3 mol/L solution onto a FH substrate. The substrate was not exposed to air plasma prior to the printing. The printed film was annealed at 500 °C for 60 min in an oven in air. As the spin coated ZTO films, it shows a particle-like structure with a greater number of particles and a greater size which is confirmed by a greater rms value of 4.21 nm and an average grain size of 18.70 nm.

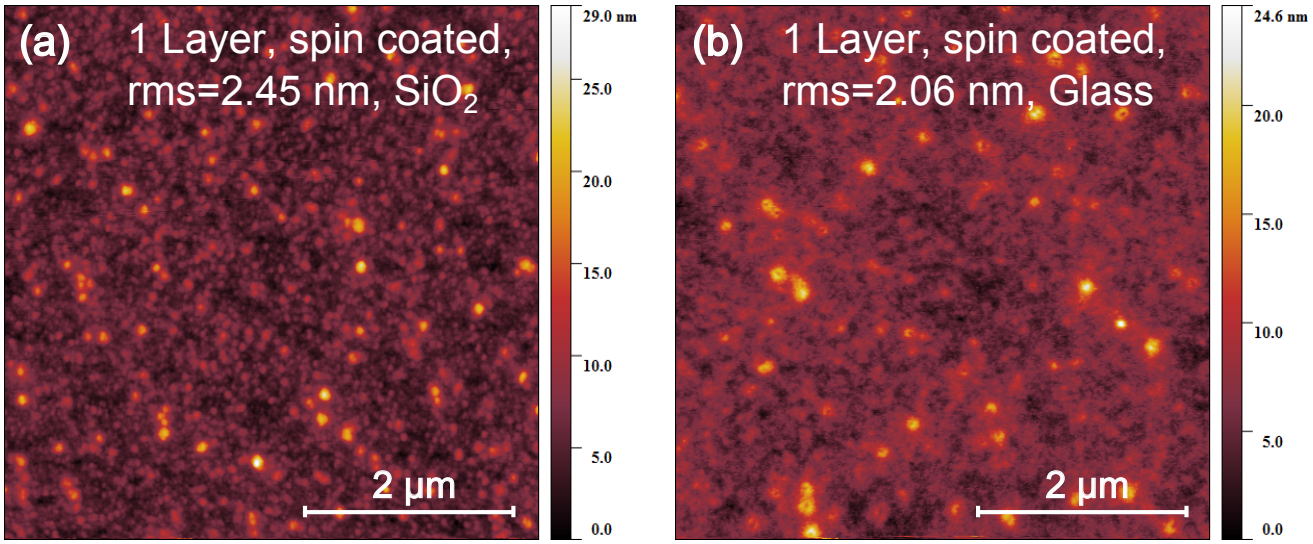

Figure 4.2: AFM images of thin, spin coated ZTO films (5000 rpm, 30 s) processed on a Si/SiO_2 (230 nm) substrate (a) and on a glass substrate (b). The images exhibit rms roughness values of 2.45 nm and 2.06 nm for **Figure 4.2** (a) and **Figure 4.2** (b), respectively. The average grain size was determined to be 5.98 nm on the Si substrate and 6.49 nm on the glass substrate. Both images show a particle-like structure.

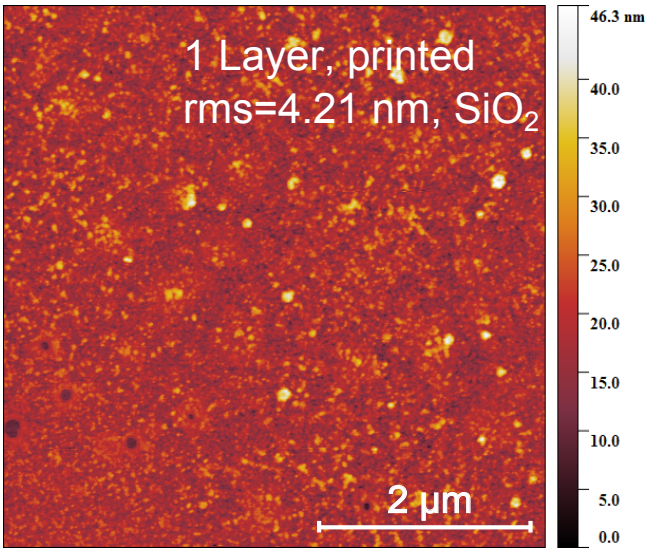

Figure 4.3: AFM image of an ink-jet printed ZTO film on a FH substrate. It shows a rms roughness value of 4.21 nm and an average grain size of 18.70 nm. Similar to the AFM images presented in **Figure 4.2** individual grains are visible.

Additional information of the topography of ZTO films was obtained by SEM. This investigation was carried out by Ulrike Kuntz from the metallurgy group of the Technische Universtität Darmstadt. The spin coated film was processed by spin coating of a 0.1 mol/L ZTO solution at 4000 rpm for 30 s followed by a drying step at 100 °C and a subsequent annealing step at 500 °C on a hotplate in air for 15 min. The ink-jet printed film was processed by printing one layer followed by an annealing step. Both ZTO films were processed on a Si substrate with a 90 nm thick SiO_2 layer. The images of **Figure 4.4** were taken at

the same magnification. **Figure 4.4** (a) shows the spin coated and **Figure 4.4** (b) the ink-jet printed film. Both show a structure that includes cracks. Similar ZTO structures have been reported by several groups [100, 57].

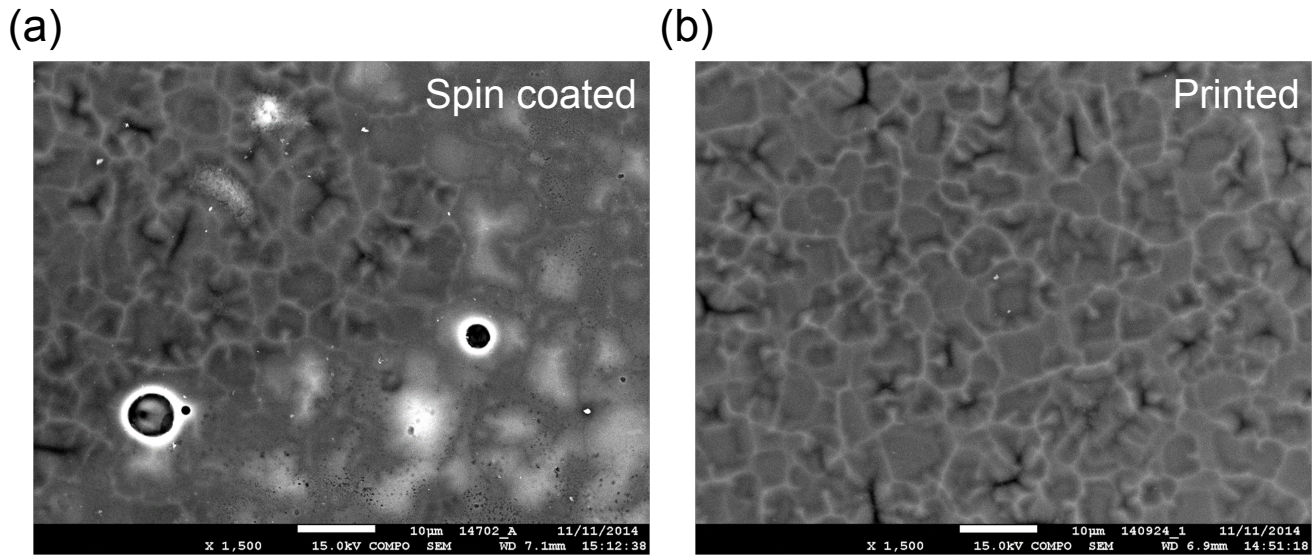

Figure 4.4: SEM images of a spin coated (4000 rpm, 30 s) ZTO (a) and an ink-jet printed ZTO film (b). They were applied on a Si substrate with a 90 nm thick SiO_2 layer. Both of them show a structure including small cracks.

The topography of the ZTO films determined by SEM reveal a particle-like structure in agreement with the previously discussed AFM images. This structure was found for the spin coated as well as the ink-jet printed films. Also the type of substrate, Si or glass, has no influence on the topography. They all show a quite smooth surface especially if spin coated with rms roughness values around 2 nm.

In the following the crystallographic structure of the ZTO films will be discussed. To gain insight into the structure two analyzing methods were used: GIXRD and TEM. The main results have been published by Sykora *et al*. [101]. Cross section TEM and GIXRD studies were performed using the transmission microscope FEI Talos F200X at 200 kV and a Seifert PTS 3003 diffractometer utilizing Cu K_α radiation, respectively. The GIXRD measurement was carried out by Dr. Joachim Brötz of the Department of Structural Research at the Technische Universität Darmstadt and the TEM measurements were carried out by Dr. Alla Sologubenko of the Laboratory for Nanometallurgy and ScopeM of the ETH Zürich. The TEM and the GIXRD measurements were performed on thin printed ZTO films (0.1 mol/L) composed of four and eight layers deposited on Si/SiO_2 (90 nm) substrates and annealed after each layer deposition. Results of both measurements are displayed in **Figure 4.5**.

Figure 4.5 shows the cross section TEM image where the SiO_2 and the ZTO layer is labeled in white. The ZTO layer shows a mixture of an amorphous phase where crystalline particles of different sizes are embedded. From the magnified section of one of the crystalline particles of the TEM image the lattice

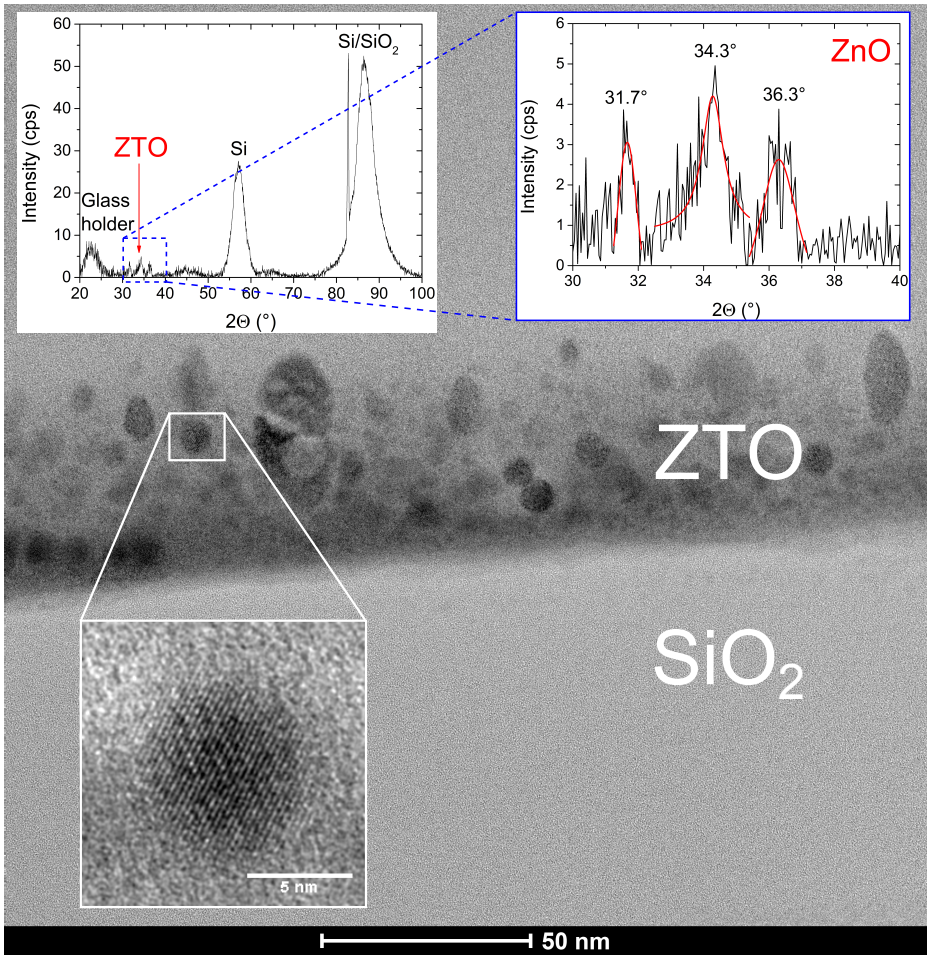

Figure 4.5: Cross-section TEM image of a printed ZTO film composed of eight layers shows an amorphous phase with embedded nanocrystallites (one particle is enlarged). The insets show the GIXRD diffractogram of a four layered printed ZTO film obtained after a grazing-angle measurement at $\Omega = 7\,^{\circ}$ (left) and an enlarged section of it. Diffracted signals of ZnO can be identified.

spacing could be determined to be 0.28 nm. This value is in good agreement with the lattice spacing of the (100) planes of the hexagonal wurtzite structure of ZnO [102, 103]. The size of the particles is decreasing from the surface of the ZTO towards the ZTO/SiO_2 interface. It is remarkable that at the interface between the ZTO and SiO_2 layer, where the current transport occurs, only very few tiny particles or in other words only the amorphous phase of ZTO can be seen. The inset on the left side of **Figure 4.5** shows the GIXRD diffractogram obtained after a very long measuring time of 59 hours. Apart from dominant peaks from the Si substrate and the glass holder, three small peaks at 31.7 °, 34.3 °, and 36.3 ° have been detected in the enlarged section of the diffractogram of the right inset. These peaks can be attributed to the (100), (002), and (101) diffraction peaks from ZnO reported at 31.9 °, 34.4 °, and 36.3 ° [104]. The remaining SnO_2 is likely to be responsible for the amorphous phase around the ZnO nanocrystallites. Sections between 30 and 40 ° of the 2Θ-value of GIXRD measurements of thin films composed of two, four, eight, and twelve printed ZTO layers are displayed in **Figure 4.6**. All

diffractograms show a broad peak between 30 and 38 ° which includes the diffracted signal of the ZnO phase. These broad peaks are typical for an amorphous phase or more precise for phases containing small nanocrystllites and are reported by other groups in the field of solution processed ZTO. Some claim that the broad peak contain the ZTO phases $ZnSnO_3$ or Zn_2SnO_4 [53]. Other groups just identify these peaks as an amorphous ZTO phase without going into detail [41, 42, 105, 106]. Taking the results from **Figures 4.5** and **Figure 4.6** into account one can say that the material system analyzed in this thesis is mainly amorphous with embedded ZnO nanocrystallites. This mixture of phases shall be called ZTO similar to the most publications in the literature.

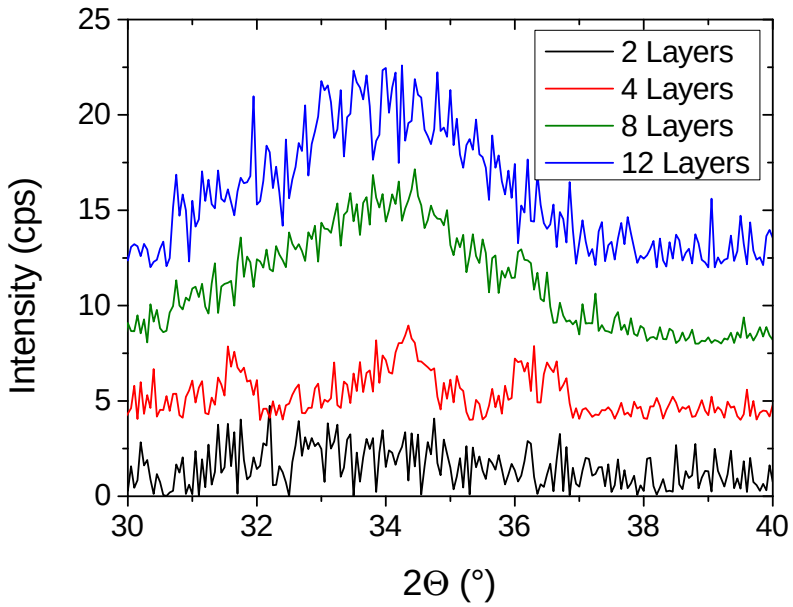

Figure 4.6: GIXRD measurement of thin films composed of increasing numbers of printed ZTO layers. The broad peak is typical for an amorphous structure, but individual smaller peaks can be identified. The red curve is the one from the inset of **Figure 4.5**. The diffractogram was measured at a grazing-angle of $\Omega = 7\,°$. The curves are separated by 4 cps for a clearer representation.

In order to determine if the ZTO films absorb in the visible region of the electromagnetic spectrum first the transmission of a thin film is measured. It was processed via spin coating one layer (4000 rpm, 30 s) of a ZTO solution of 0.3 mol/L on a quartz glass substrate followed by an annealing step. **Figure 4.7** shows the absorption as a function of the wavelength λ. Almost no absorption can be seen in the visible region which is typical for a transparent material. A straight line fitted to the absorption edge results in the determination of a wavelength of $\lambda = 329$ nm at the x-axis intercept. Using this value and the fundamental equation $E = h\nu$ the band gap could be determined to be $E_g = 3.77$ eV. The Tauc's plot of the ZTO film is displayed in the inset of **Figure 4.7**. With the measured thickness of 30 nm the expression $(\alpha h\nu)^2$ could be calculated and plotted as a function of the energy of the absorbed photons. Using a linear fit and the extension to the x-axis a direct band gap of 5.13 eV could be obtained. While

the value determined using the Tauc's plot is high and is in the region of an insulator, the value obtained from the absorption edge lies in the reported range of 3.3 to 3.9 eV for the ZTO band gap [41, 42]. Therefore this value was adapted for further discussion.

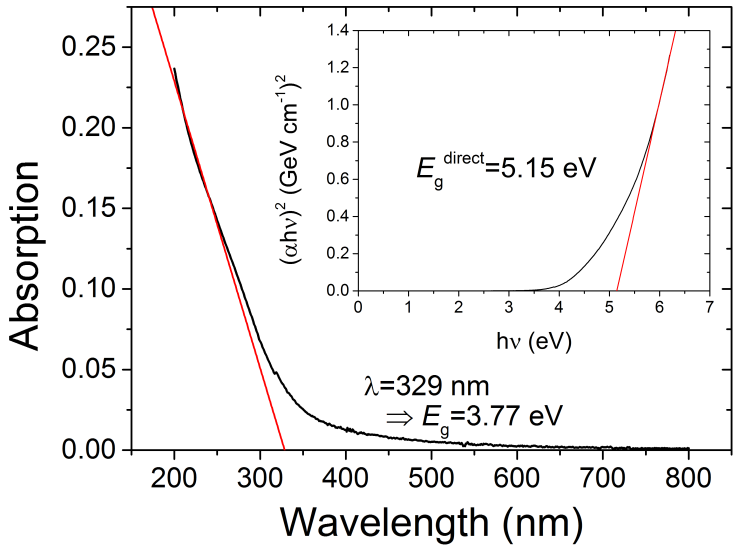

Figure 4.7: Absorption of a ZTO film as a function of the wavelength. There is almost no absorption in the visible region. By fitting a straight line to the adsorption edge a wavelength of the x-axis intercept can be determined to be $\lambda = 329\,\text{nm}$. This corresponds to a value of the band gap of $E_g = 3.77\,\text{eV}$. The inset shows the Tauc's plot of the absorption results for a direct semiconductor. A direct band gap of 5.13 eV could be determined by fitting a straight line to the curve and extending it to the x-axis.

Apart from the band gap of ZTO other energetic levels such as the valence band offset ($E_{\text{VBM}} - E_{\text{F}}$) and the work function Φ need to be known before a band diagram can be drawn. These missing levels can be obtained by XPS and UPS. For the XPS/UPS investigation a 0.1 mol/L ZTO solution was spin coated (4000 rpm, 30 s) on a Si substrate with a native SiO_2 layer and annealed. This procedure was repeated two times. The final layer thickness was determined by profilometry to be 24 nm. A Si substrate with a native oxide layer is necessary to ensure a conducting connection between the spectrometer and the sample. **Figure 4.8** displays the survey spectrum of the XPS measurement after the film was sputtered for 30 s with argon atoms with an energy of 1 kV. No charging effects could be detected meaning the binding energy values are not shifted towards higher energy values. The XPS and UPS measurements were performed by Markus Motzko from the Surface Science Group of the Technische Universität Darmstadt and the survey spectrum was reviewed by Dr. Andrea Gassmann of the Electronic Materials Group of the Technische Universität Darmstadt.

In the survey spectrum the main peaks of Zn, Sn, and O are present. The missing core level 1s C peak at 284.5 eV confirms that the surface contamination has been removed during the sputtering process. Apart

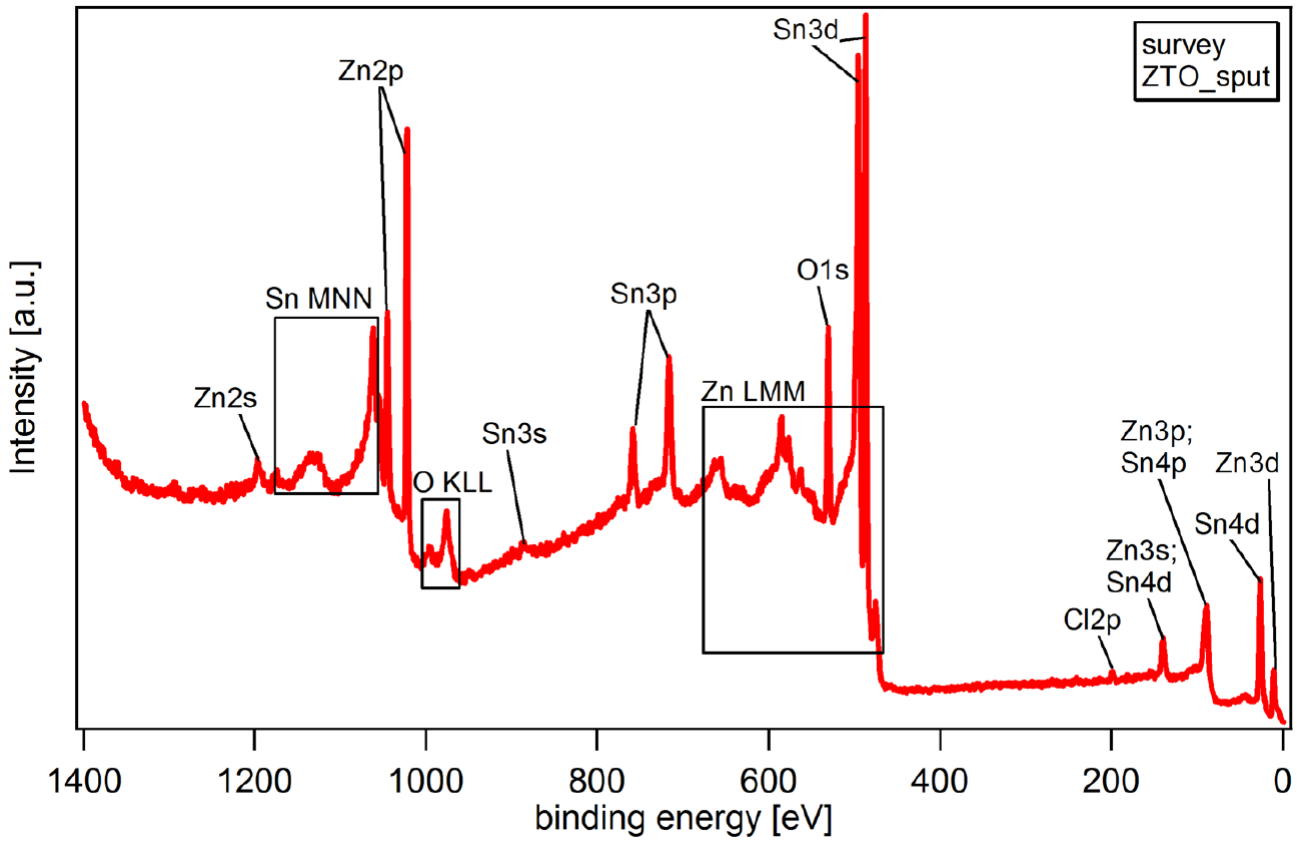

Figure 4.8: XPS survey spectrum of a 24 nm thick ZTO film, which was sputtered for 30 s with Argon atoms with an energy of 1 kV in order to remove any surface contamination. The main peaks of Zn, Sn, and O are indicated. A small peak of Cl is still present. The absence of the C and the N peak indicate a thorough removal of surface contaminations and a complete decomposition of the nitrate during processing.

from that a small Cl peak from the precursor solution can be detected at 200 eV. This peak can either be explained by still present $SnCl_2$ which was not completely decomposed during the annealing steps or by a residual from the addition of HCl. The absence of the N 1s peak normally present at 398 eV is due to the complete decomposition of the NO_3^- ion from the Zn salt. Finally one can say, that the spectrum contains all expected elemental signals and is very similar to an XPS survey spectrum for a solution processed fluorine doped ZTO recently reported by Salmeh *et al.* [107].

For the determination of the valence band offset and the work function, XPS and UPS were applied. The position of the valence band maximum measured by XPS can be seen in **Figure 4.9**. The value of the valence band offset $E_{VBM} - E_F$ was determined by the intersection (blue cross) of the two linear fited lines in red color to 3.37 eV and is in good agreement with literature values for ZTO positions containing a Sn^{4+} state [108]. Sn^{2+} would have a value around 2 eV smaller. The complete oxidation of the Sn ions during the precursor route decompostion was hereby confirmed.

The work function was determined by UPS. In **Figure 4.10** the complete UPS spectrum was shifted by the application of a retarding voltage of $V_R = 6$ eV. This bias is necessary to completely extract the

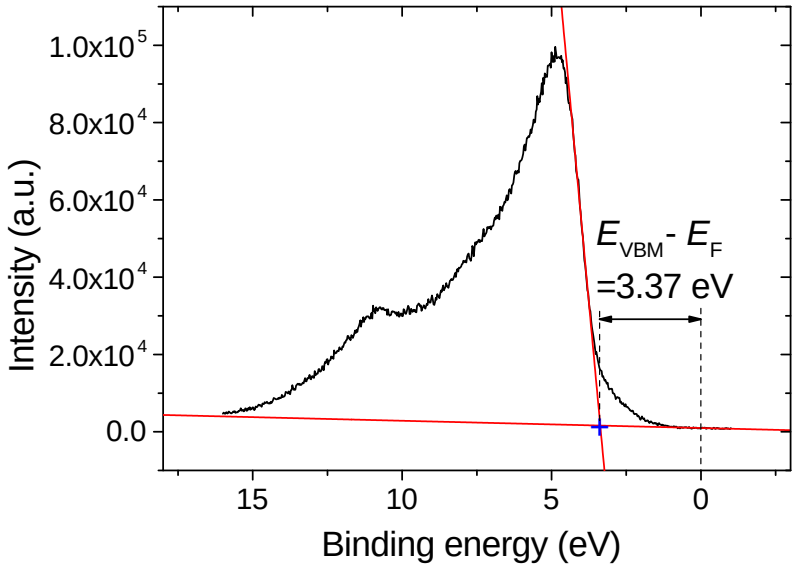

Figure 4.9: A part of the XPS spectrum shows the valence band with the identification of the valence band offset $E_{\mathrm{VBM}} - E_{\mathrm{F}}$. The value of 3.37 eV highlighted as the blue cross was determined by the intersection of the two red fitting lines.

photoelectrons. The binding energy of the secondary electron edge $E_{\mathrm{B(SK)}}$ with a value of 17.43 eV can be used to calculate the work function of ZTO by applying **Equation 3.9**. A value of $\Phi = 3.77$ eV was obtained. This value is 1.25 eV smaller than the reported value for Zn_2SnO_4 [52] and 1.53 eV smaller than the value reported for the $ZnSnO_3$ phase [51]. The work function of ZnO is 4.5 eV [109] and the work function of SnO_2 is 4.75 eV [110]. The work function of the investigated ZTO is closest to the value of ZnO.

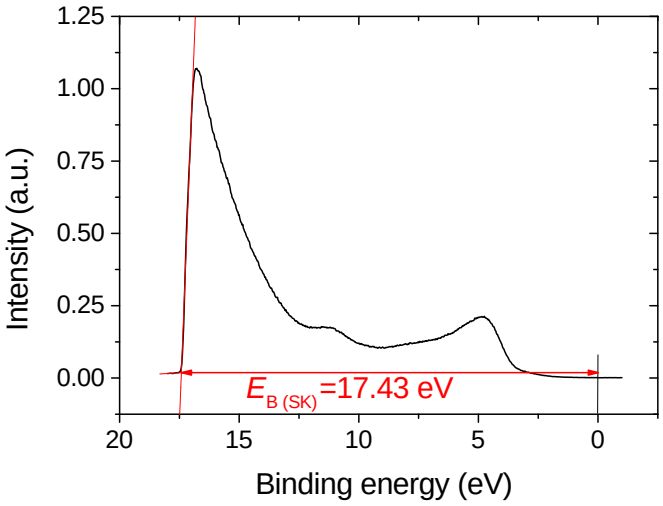

Figure 4.10: UPS spectrum for the determination of the ZTO work function Φ applying the binding energy of the secondary electron edge $E_{\mathrm{B(SK)}}$ of the extracted electrons. The positions of the energetic level was determined by the intersections of the red fitting lines. The complete spectrum was shifted by the application of the retarding voltage $V_{\mathrm{R}} = 6$ V in order to extract the photoelectrons.

The band diagram of the analyzed ZTO system can be drawn according to **Figure 4.11** if all extracted energetic levels are taken into consideration. The Fermi level lies close to the conduction band minimum which makes the analyzed ZTO system to an n-type semiconductor. But it has to be taken into account that the energetic levels, valence band offset and work function, have been determined from a sputtered ZTO sample under UHV conditions. The ZTO system as processed throughout this thesis in air and under ambient conditions may have slightly different energy values.

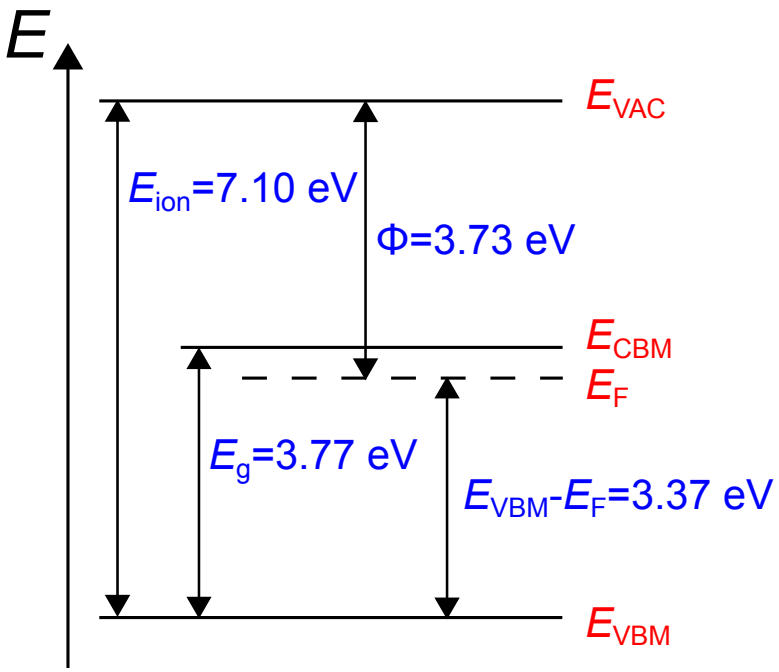

Figure 4.11: Band diagram of the ZTO system. The fix vacuum level E_{VAC}, conduction band minimum E_{CBM}, Fermi level E_F, and valence band maximum E_{VBM} are highlighted in red. The energy level differences like work function Φ, ionization energy E_{ion}, band gap E_g, and valence band offset $E_{VBM} - E_F$ are displayed in blue. The n-doped ZTO system shows an offset between the Fermi level and the conduction band of 0.40 eV.

Taking all results of this section into account one can say that the solution processed ZTO samples as of this thesis exhibit quite smooth surfaces when processed by either spin coating or ink-jet printing. AFM as well as SEM studies confirm the particle-like structure of the thin films. The TEM and XRD investigation reveal that the ZTO forms basically an amorphous phase where small ZnO nanocrystallites are embedded (see **Figure 4.5**). By XPS/UPS the complete oxidation of the Sn-ion could be confirmed. With the help of the UV-Vis absorption measurements, the band diagram of the ZTO system can be completed as shown in **Figure 4.11** and demonstrates that ZTO is an n-type semiconductor.

4.2 Effects of precursor route on bottom-gate transistors

The following sections concentrate on the influence of the precursor route on solution processed ZTO bottom-gate, top-contact transistors. It will be investigated if the ZTO transistors have to be measured in the GB or in air, which Zn to Sn ratio results in the best performance, and which effect the use of a second solvent and the amount of HCl have on the performance of bottom-gate transistors. The transistor layout where the ZTO is applied can be seen in **Figure 3.5**.

In general, the environment, in which the *I-V*-characteristics of metal oxide based transistors are recorded, can affect their results. From AOS transistors it has been reported that they have been measured in air [45, 111, 56], in a N_2 atmosphere [112, 113, 114] or had to be protected by additional coatings [106, 115, 100]. In order to check if the present analyzed ZTO semiconductors show any sensitivity towards H_2O and O_2, a typical result of a single transistor was initially measured in air and afterwards in a N_2 filled GB with O_2 and H_2O concentration lower than 10 parts per million (ppm). This device was produced by spin coating (5000 rpm, 30 s) of a single layer of a 0.3 mol/L ZTO solution on a pre-structured FH substrate with a 90 nm SiO_2 layer. The sample was annealed at 400 °C for 60 min in air. **Figure 4.12** shows the transfer characteristics of this sample measured under both conditions.

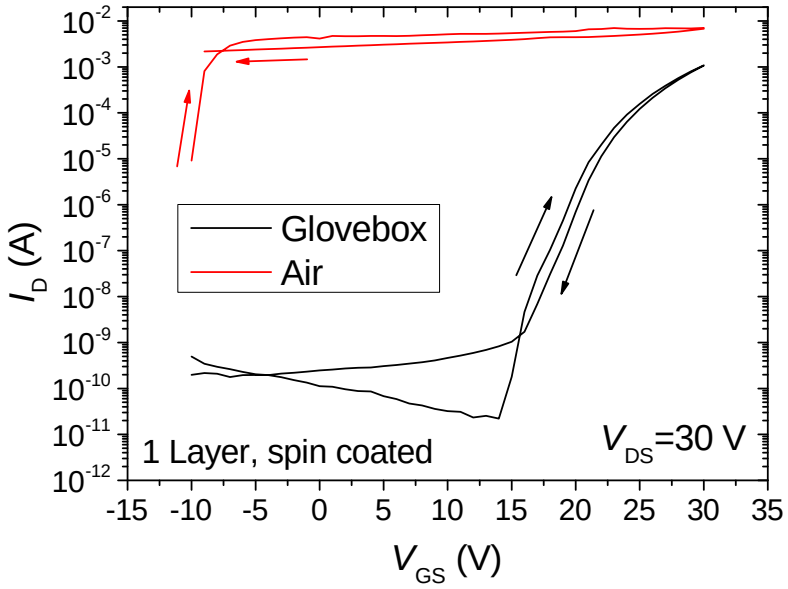

Figure 4.12: Transfer characteristics of a one layered bottom gate, bottom contact spin coated (5000 rpm, 30 s) ZTO device, measured in a N_2 filled GB (black curve) and in air (red curve). The black curve shows a normal FET characteristic, whereas the red curve shows no off-state.

The transfer characteristics measured in the GB shows the standard transistor behavior with a distinctive off-state and on-state, in contrast the characteristics measured in air does not show any off-state. This indicates that the threshold voltage or the complete off-region is shifted to larger negative voltages. It

exhibits higher currents and can better be described as an always-on device. To compare to transistors based on ZnO, they are normally measured in the GB [112, 113] and such based on SnO_2 are normally characterized in air [116, 117, 118]. A possible explanation of the higher current for the transfer characteristics measured in air has been given by Park *et al.* [119]. Their suggestion is that H_2O molecules are adsorbed at the AOS material, in this case IGZO. The adsorbed H_2O molecules on thick AOS layers could create an accumulation layer close to the surface and could therfore act as a donors. Bauskar *et al.* reported in more detail about this process [120]. A sketch of this process is displayed in **Figure 4.13**.

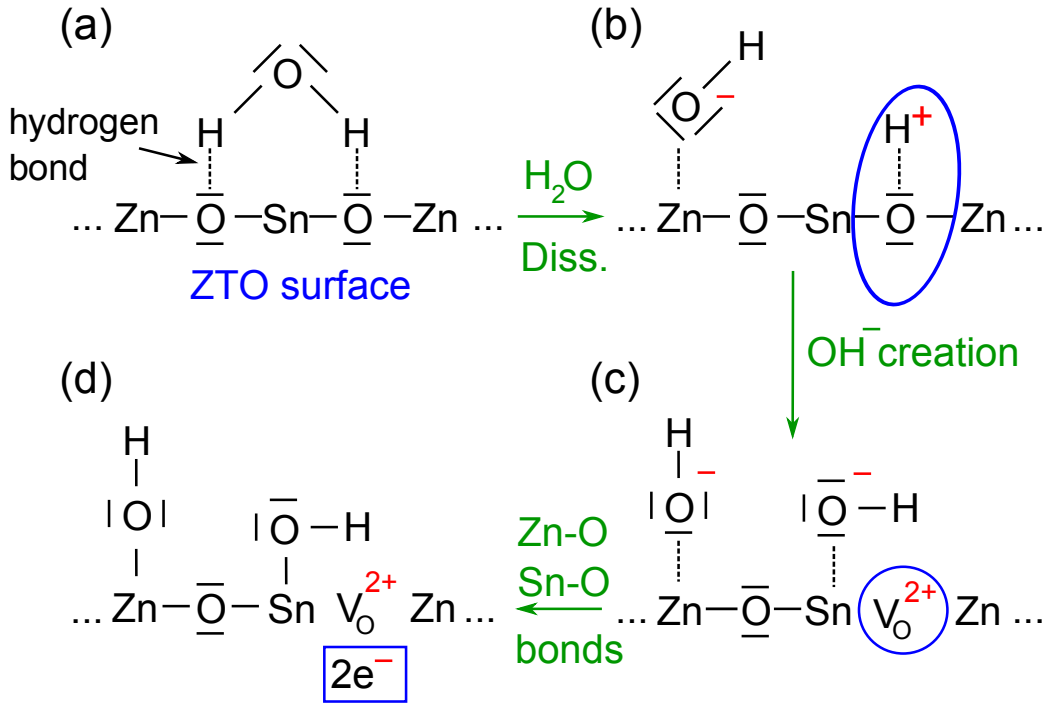

Figure 4.13: Simplified sketch of H_2O adsorption on a ZTO surface. First the water molecule is chemisorbed via hydrogen bonds with O of the ZTO surface (a). Then the water molecule is dissociated to OH^- and H^+ (b). H^+ can react with O of the ZTO surface to form another OH^- (c). During this process an oxygen vacancy $V_O{}^{2+}$ is created. Two free electrons appear during the creation of the Zn−O, Sn−O bonds (d). These electrons can lead to an increase of the charge carrier concentration and consequently to an increase in conductivity. This sketch was inspired by the publications of Bauskar *et al.* [120] and Patil *et al.* [121].

H_2O molecules can chemisorbed on the ZTO surface via hydrogen bonds with terminal O of the ZTO (a). The first aqueous layer can then be dissociated to OH^- and H^+ (b). The hydroxyl ion is adsorbed at the Zn or Sn ions of the ZTO surface and the proton can react with O of the ZTO surface to form another OH^- ion (c). As a result an oxygen vacancy $V_O{}^{2+}$ appears. If bonds are formed between the metal ions of Zn and Sn and oxygen two free electrons are created. These electrons are accumulated at the ZTO surface leading to an increase in conductivity.

Figure 4.14 displays the corresponding output characteristics of such devices once again measured in a GB (a) and in air (b). The forward and the backward direction of the scan are indicated by black arrows. In addition, the corresponding gate-currents are shown as dashed lines.

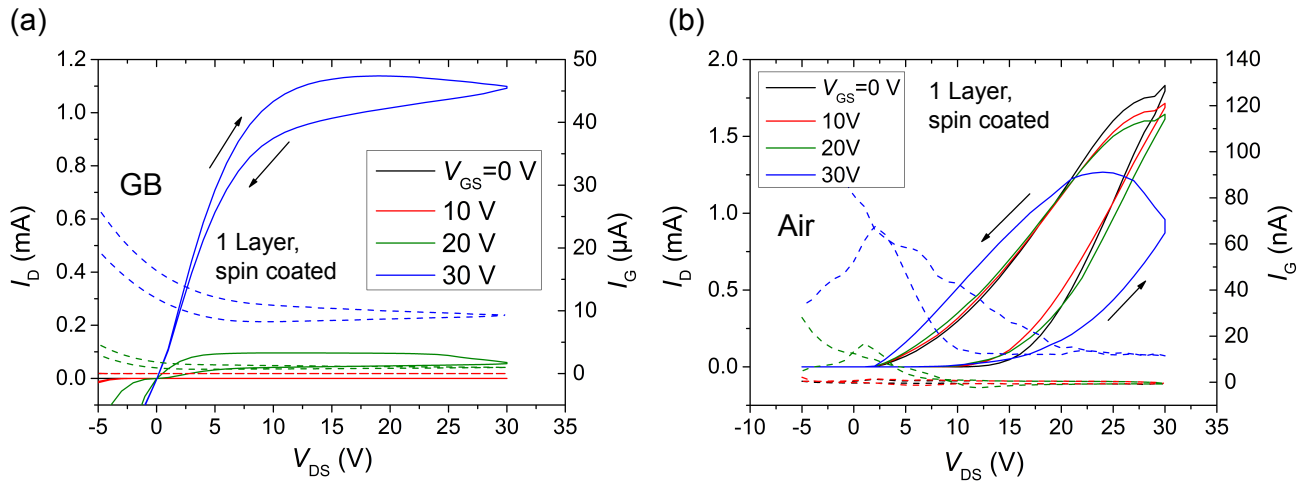

Figure 4.14: Output characteristics of a single layer spin coated ZTO transistor measured in a N_2 filled GB (a) and in air (b). The black arrows indicate the forward and backward scan. The dashed lines represent the corresponding gate-currents.

The output curves of the transistor measured in N_2 show the expected transistor behavior with a linear and a saturation regime. The smaller currents in the backward scan compared to the forward scan can be explained by electron trap states at the interface between the ZTO semiconductor and the SiO_2 dielectric layer. This clockwise hysteresis is due to the fact that in order to achieve the same amount of charge carriers in the channel a higher voltage has to be applied to the gate due to trapped electrons that do not contribute to the current transport [32]. Currents as small as 1 nA have been measured for $V_G = 0$ V. This means that almost no current flows between source and drain without the application of a finite potential between the source and gate electrode. The gate-currents are 100 times smaller than the drain-currents. In contrary, the output curves measured in air show currents of up to $I_D = 1.8$ mA if 0 V is applied between source and gate. These output characteristics show no linear or saturation regime. They exhibit larger currents in the backward than in the forward direction (arrows). The gate-currents are 100,000 times smaller than the corresponding drain-currents. In addition, these curves show a huge counterclockwise hysteresis. It is reported to be a result of the flipping of electrical dipoles at the interface [32]. These dipoles could be adsorbed and diffused H_2O molecules. As a consequence of these results all *I*-*V*-curves of the present transistors are measured in a N_2 filled GB if not stated otherwise.

At this point of the thesis experiments were performed to determine the ratio between Zn and Sn in the precursor solution for the best transistor performance. Three different solutions with weight fractions of Zn to Sn of 7:3, 1:1, and 3:7 at a concentration of 0.30 mol/L were processed according to the method

described in section 3.1. 0.21 g $Zn(NO_3)_2 \cdot xH_2O$ and 0.09 g $SnCl_2$ were dissolved in 5 mL EtOH for the 7:3 solution and the opposite amounts for the 3:7 solutions. For the 1:1 solution 0.15 g of each salt were dissolved. In each solution 50 µL HCl amounting to 1 vol% was added. The ZTO precursor solution was applied via spin coating (5000 rpm, 30 s) onto FH substrates and annealed at 500 °C for 15 min in air. The 1:1 and especially the 3:7 device exhibit a inferior substrate coverage. The sqrt- and the semi-logarithmic plot of the transfer characteristics can be seen in **Figure 4.15**.

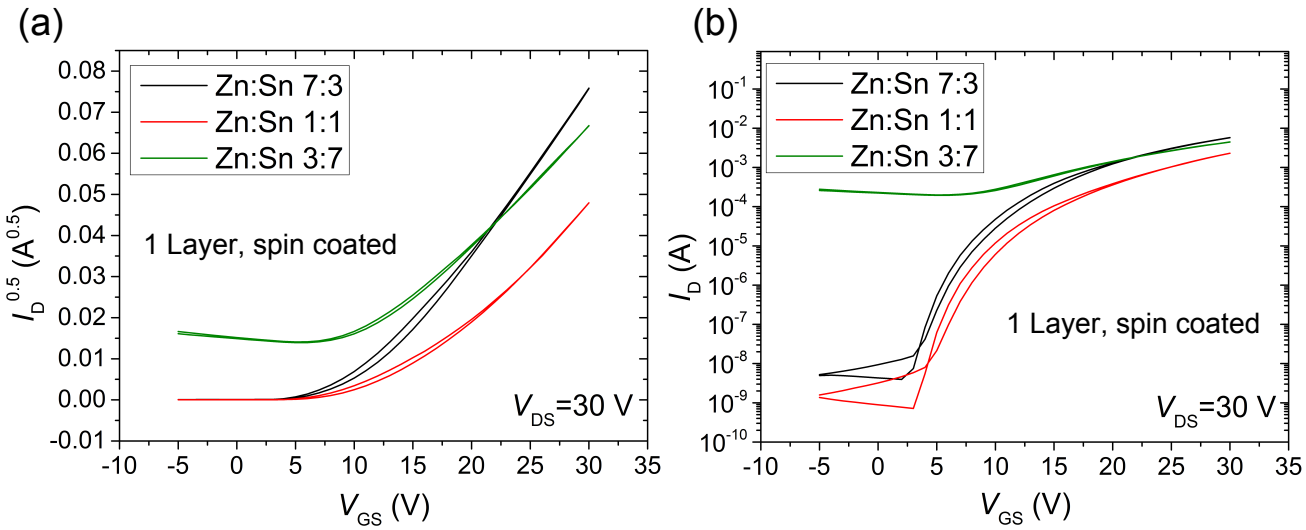

Figure 4.15: Transfer characteristics of single layer ZTO transistors spin coated (5000 rpm, 30 s) on FH substrates based on different weight ratio of Zn to Sn. The black curves show the results of the 7:3, the red curves of the 1:1 and the green curves of the 3:7 ratio. Subfigure (a) shows the sqrt-plot of representative curves of the three devices and subfigure (b) shows the corresponding semi-logarithmic plot. All sweeps were performed at a constant source-drain voltage $V_{DS} = 30$ V.

Without considering the extracted values of the transistors which are summarized in **Table 4.1** one can already realize from **Figure 4.15** that the device with the 7:3 ratio shows the superior performance. It exhibits the highest on-current and the lowest threshold voltage. The transistor of the 1:1 ratio shows smaller off-currents but in addition smaller on-currents compared to the transistor with the 7:3 ratio. The transfer characteristics of the device with a 3:7 ratio show no clear field-effect anymore but rather an always-on device with very large off-currents in the order of several hundred µA. Such a depletion mode transistor is not wanted since a negative voltage has to be applied in order to turn the device into the off-state. **Figure 4.16** shows the output characteristics of the transistor with the 7:3, 1:1, and 3:7 ratio, respectively. All graphs show clear gate modulation and the characteristic of the transistors with the 7:3 and 1:1 ratio also exhibit saturation behavior. The transistor with the 3:7 ratio shows no saturation. The transistor with the 7:3 ratio exhibits drain-currents which are three times larger than the transistor with

the 1:1 ratio at similar applied voltages. All output characteristics show hysteresis for the scan direction which is indicated by the black arrows. They likewise exhibit contact resistances.

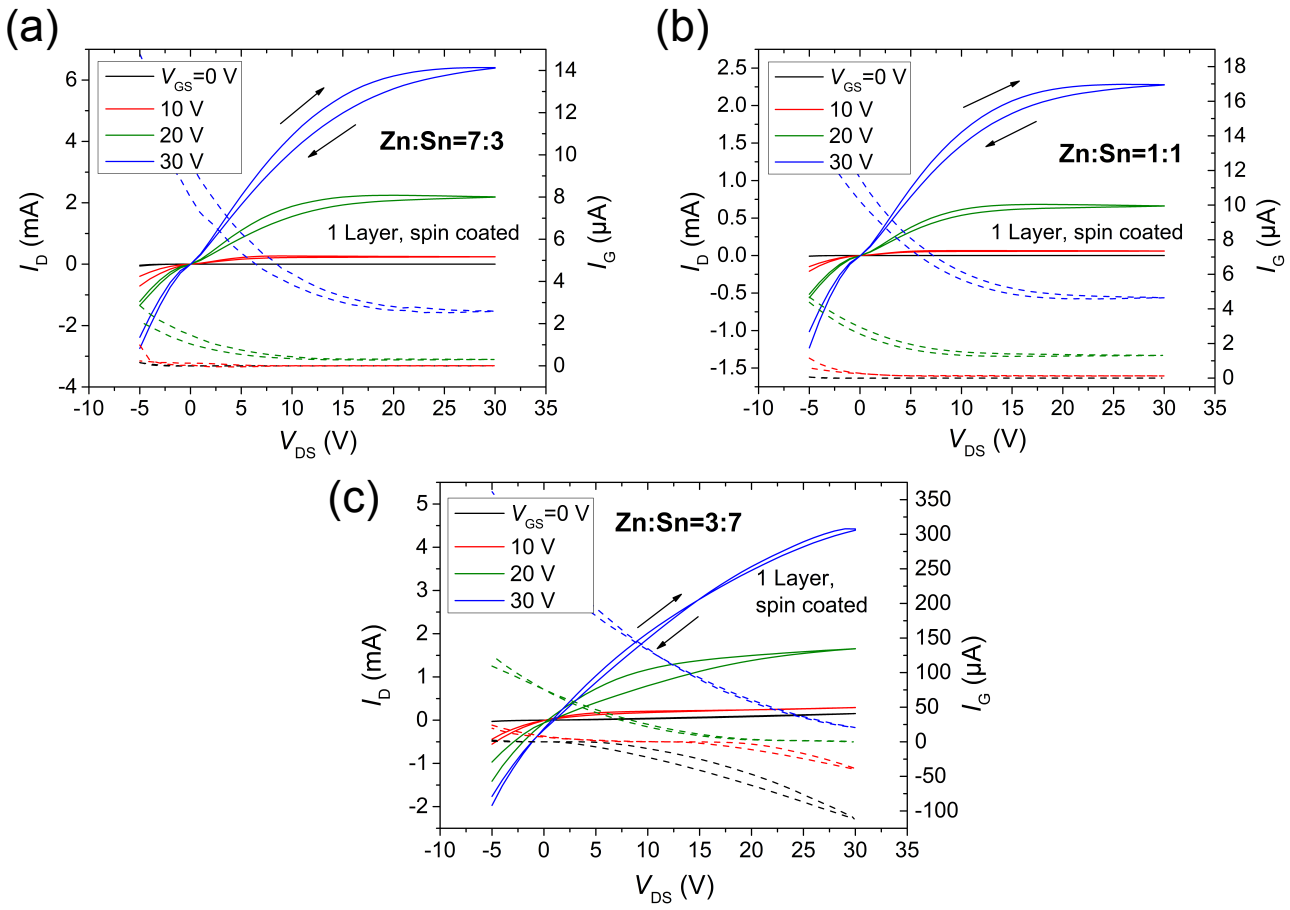

Figure 4.16: Output characteristics of the FH transistors based on different mass weight ratios of Zn to Sn. Subfigure (a) shows the output curves for a transistor with a Zn:Sn ratio of 7:3 and subfigure (b) displays the output curves for a transistor with a ratio of 1:1 and subfigure (c) displays the output characteristics of 3:7.

Table 4.1 summarizes the main transistor parameters of the transistors with variable Zn to Sn ratios. The values in parentheses represent the corresponding standard deviation calculated from four devices. It can be observed that the saturation mobility deteriorates strongly when the precursor solution incorporates more Sn than Zn. The on/off-current ratio decreases too. The transistors with a ratio of 3:7 show very small on/off-current ratio with a value of only 2.2×10^2.

If only pure EtOH is used as a solvent for dissolving the precursor salts a solution with a very low viscosity is obtained. The main ink properties which are density, dynamic viscosity, and surface tension were determined by Dr. Julia Gebauer at the Universität Duisburg-Essen (UDE) to be 780.9 kg/m^3, 28.99 $\pm$3 mN/m, and 1.38 $\pm$3 mPa s, respectively. Applying these parameters and the cartridge dependent values for the velocity (6 m/s) and the noozle diameter (21.5 µm), the inverse Ohnesorge number Z can be calculated by **Equation 3.5** to be 16. Since this value is higher than 10, drop formation with

Table 4.1: Saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing (S.S.), and on/off-current ratio (I_{on}/I_{off}) for transistors with a Zn:Sn weight fraction of 7:3, 1:1, and 3:7. The values in parentheses represent the corresponding standard deviation calculated for four devices.

Zn:Sn ratio	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
7:3	1.61 ($\pm$0.30)	15.2 ($\pm$3.15)	1.18 ($\pm$0.23)	3.2×10^7 ($\pm3.7\times10^7$)
1:1	0.83 ($\pm$0.18)	14.4 ($\pm$0.60)	0.99 ($\pm$0.11)	2.3×10^6 ($\pm6.6\times10^5$)
3:7	0.06 ($\pm$0.03)	4.1 ($\pm$1.56)	2.24 ($\pm$2.23)	2.2×10^2 ($\pm3.5\times10^2$)

such a low viscosity ink is difficult to achieve. In order to increase the viscosity a second solvent was added. For this purpose ethylene glycol (EG) ($HO-C_2H_4-OH$) was applied because its vapor pressure is 5.3 Pa, which is considerably smaller than the high vapor pressure of EtOH with 58 hPa. In addition, it was reported that if two solvents with variable vapor pressures are combined, a Marangoni flow [72] can be achieved that could diminish the coffee stain effect [122, 123].

In order to find the concentration of EG which leads to transistors with a better performance, precursor solutions with 20, 40, 50, 60, and 100 vol% of EG were added to the EtOH based precursor solution. In each solution 1 vol % HCl was added as a stabilizer. **Figure 4.17** shows the transfer curves in a semi-logarithmic plot for the best working devices with various EG contents. The transistors were processed via spin coating (4000 rpm, 30 s) two layers of the precursor solution (0.1 mol/L) on FH substrates and annealing after each layer deposition. All characteristics were measured at a constant source-drain voltage of $V_{DS} = 30$ V.

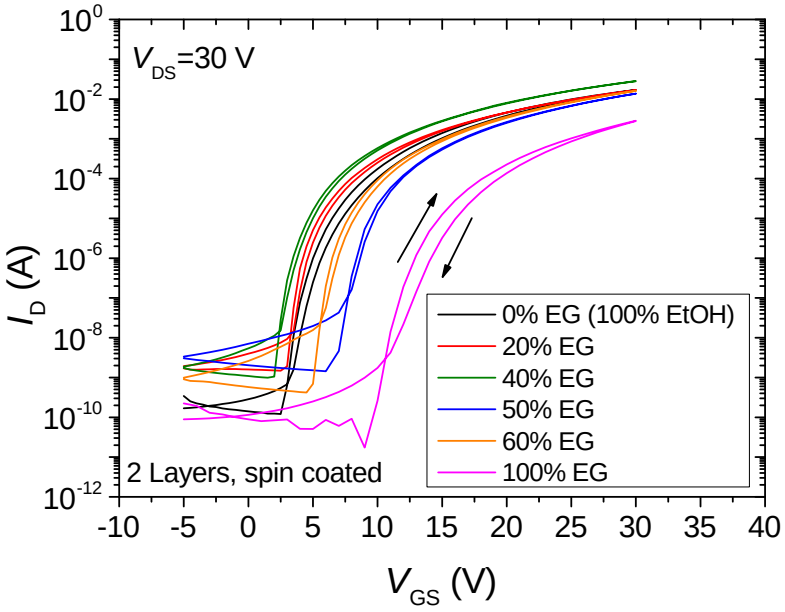

Figure 4.17: Transfer curves of transistors based on increasing vol % of EG in the EtOH precursor solution measured at a source-drain voltage of $V_{DS} = 30$ V.

It can be seen that the devices produced from a mixture of solvents show higher off-currents than the single solvent solutions (black and pink curves). The device with the pure EG solvent solution (pink curve) exhibits the highest threshold voltage and the largest hysteresis indicated by the arrows. The highest on-currents and the smallest threshold voltage as well as the smallest hysteresis are shown by the device with a 40 vol % of EG (green curve). In this figure only the transfer curves from the devices with the highest saturation mobility are plotted. **Figure 4.18** illustrates the mean values and their standard deviation of the saturation mobility (μ_{sat}) in black and the threshold voltage (V_{th}) in red for an increasing amount of EG. The solid lines show the trend of the two transistor parameters.

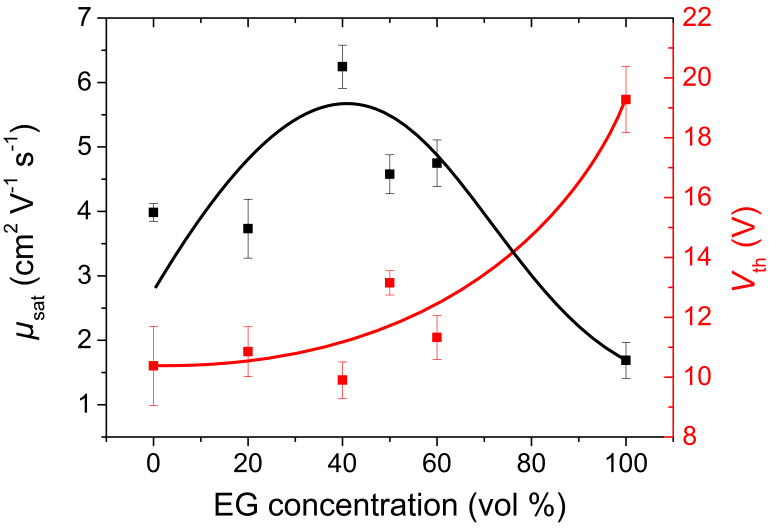

Figure 4.18: Comparison of the saturation mobility (μ_{sat}) and the threshold voltage (V_{th}) of transistors which were produced from precursor solutions with increasing amounts of EG (vol %). These mean values as well as the error bars were calculated from the four 20 µm channel length devices. The solid lines guide the eye with respect to the two transistor parameters.

The saturation mobility (black curve) is 4 $cm^2V^{-1}s^{-1}$ for a pure EtOH based precursor solution. It reaches its peak value of 6.2 $cm^2V^{-1}s^{-1}$ for a concentration of 40 vol %. Further addition of EG leads to a decrease to 5.6 $cm^2V^{-1}s^{-1}$ before the mobility drops sharply to a value of only 1.7 $cm^2V^{-1}s^{-1}$ for a pure EG based precursor solution. The threshold voltage (red curve) does not change strongly and varies between 9.9 V (40 vol %) and 10.9 V (20 vol %) before it increases to 19.3 V for a precursor solution based on EG as a solvent. The standard deviations, indicated by the error bars, of the saturation mobility as well as the threshold voltage values are small and show similar values.

Figure 4.19 displays the extracted mean values of the on/off-current ratio (I_{on}/I_{off}) and the subthreshold swing (S.S.) including the corresponding standard deviations represented as error bars. As before the solid lines highlight the trend of the two transistor parameters. The highest on/off-current ratio (green curve) was calculated for the pure EtOH based precursor solution with a value of 1.3×10^8. It then decreases to a value of 1.0×10^7 (50 vol %). The precursor solutions with EG again shows higher on/off-

current ratio with a value of 8.6×10^7. The subthreshold swing (blue curve) does not change considerably when EG is added into the EtOH based precursor solution. The smallest value was determined to be 0.44 V/decade for the solution with 60 vol % of EG and the highest value is 0.64 V/decade for the pure EG based precursor solution. The standard deviations, indicated by the error bars, of the subthreshold swing and especially the on/off-current ratios are quite large except for the solutions with 40 and 50 vol % of EG.

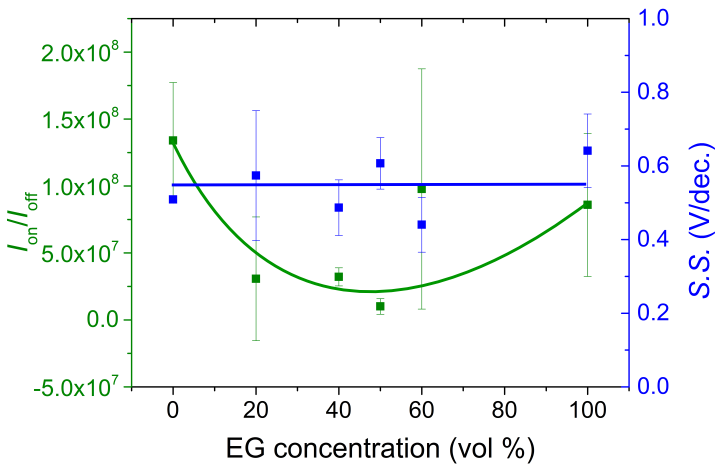

Figure 4.19: Comparison of the on/off-current ratio (I_{on}/I_{off}) and the subthreshold swing (S.S.) of transistors which were produced from precursor solutions with increasing amounts of EG (vol %). These mean values as well as the error bars were calculated from the four 20 µm channel length devices. The solid lines indicate the trend of the two transistor parameters.

Summarizing all presented results on the inclusion of EG into the EtOH based precursor solution, one can say that adding 40 vol % of EG meaning a EtOH/EG ratio of $\frac{1.5}{1.0}$, creates the best performing transistor with the highest saturation mobility of 6.2 $cm^2V^{-1}s^{-1}$, the smallest threshold voltage of 9.9 V, acceptable on/off-current ratio of 3.2×10^7, and a subthreshold swing of 0.49 V/decade. An analysis of the most important ink parameters were measured by our project partner at the Universität Duisburg-Essen (UDE). The density, dynamic viscosity, and surface tension of a solution with 40 vol % of EG were measured to be 977.4 kg/m^3, 38.53 $\pm$0.17 mN/m, and 7.89 $\pm$0.1 mPa s, respectively. The resulting inverse Ohnesorge number was calculated from **Equation 3.5** to be 3.4. This number is within the range of an ink which allows for good drop formation.

As already mentioned in the chemical reaction, described by **Equation 3.1** and **Equation 3.2** the addition of HCl is necessary to oxidize the Sn ion and consequently avoid precipitation. It is now determined how much HCl is necessary to guarantee a complete oxidation and the effect of HCl on the transistor performance is discussed. Bottom-gate, bottom-contact devices were processed by spin coating (4000 rpm, 30 s) and annealing of two successive ZTO layers on FH substrates. The 0.1 mol/L precursor solutions

had a HCl content of 0.25, 0.50, 1.00, 5.00, and 10.0 vol%. **Figure 4.20** displays the transfer curves in a linear (a) and semi-logarithmic plot (b) of the best performing transistor using precursor solutions with various amounts of HCl.

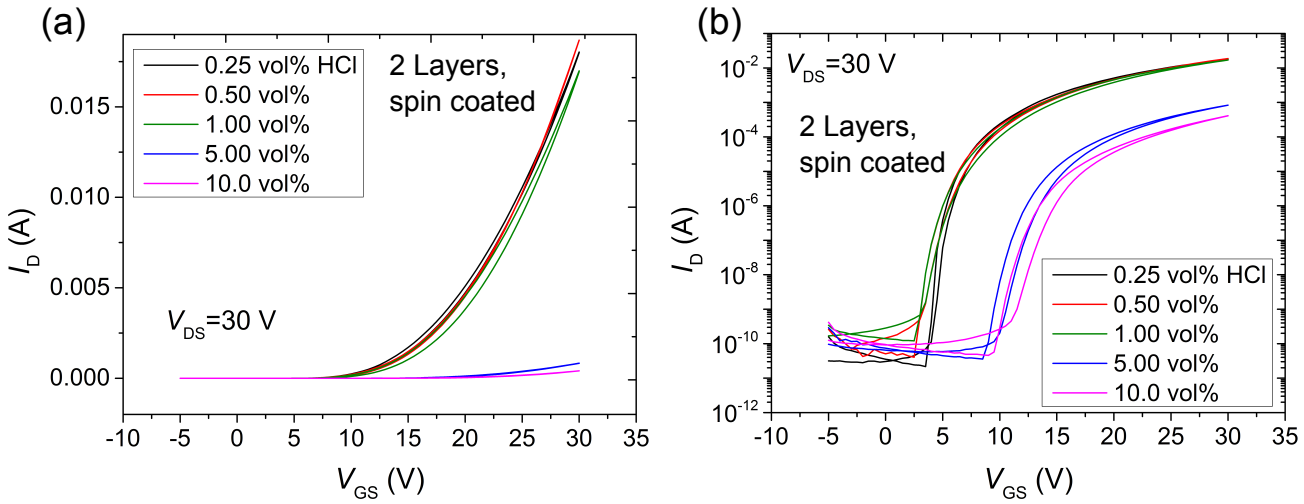

Figure 4.20: Transfer curves in a linear (a) and semi-logarithmic plot (b) of the best working transistors processed with precursor solutions with different vol% of HCl. The curves were measured at a constant source-drain voltage of 30 V. The precursor solution with 0.125 vol% and without the addition of HCl showed precipitation as displayed in **Figure 3.1** (a).

The curves of the linear plot in **Figure 4.20** (a) reveal that the transistor with the highest on-current was processed using the precursor solution with 0.5 vol% of HCl. The transistors processed with solutions of 0.25 or 1.0 vol% of HCl exhibit characteristics with similar current values, however the currents drop sharply if precursor solutions with a higher HCl content of 5 or 10 vol% were used. The semi-logarithmic plot of **Figure 4.20** (b) show a clear separation between the threshold voltage from the transistors with a small amount of HCl and the transistors processed with the 5 or 10 vol% solutions. Apart from that the HCl content in the precursor solutions has no clear effect on the off-currents of the transistors. This means that the overall conductivity of the layer is not changed or the introduction of additional HCl does not lead to a doping effect. The smallest value of the off-currents was measured for the transistor processed with the smallest HCl content. It can be seen that a smaller amount of HCl in the precursor solution leads to a steeper onset behavior or in other words smaller subthreshold swing values. The output characteristics of the devices made from the precursor solution with the smallest HCl content of 0.25 vol% and the highest HCl content of 10.0 vol% are displayed in **Figure 4.21**.

The 0.25 vol% transistor shows a maximum drain-current of 17.5 mA at $V_{DS} = V_{GS} = 30$ V and the 10.0 vol% transistor shows a maximum drain-current value at the same voltage values of only 0.45 mA. The 0.25 vol% device show almost no hysteresis, but hysteresis is clearly visible at the 10.0 vol% device. Remarkably, the values for the maximum gate-currents are around 20 times larger for the 0.25 vol%

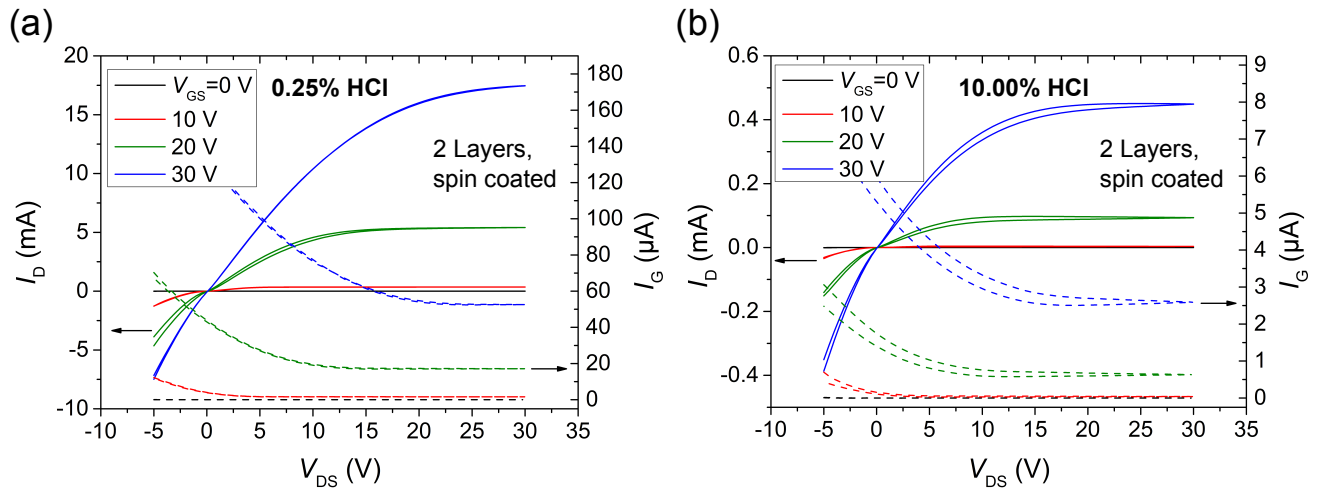

Figure 4.21: Output curves of devices built by processing precursor solutions with 0.25 vol% (a) and 10.0 vol% HCl (b). The solid lines show the drain-current values and the dashed lines the corresponding gate-currents.

transistor than for the 10.0 vol% transistor. But they are still 315 times (0.25 vol% transistor) and 180 times (10.0 vol% transistor) smaller than the drain-current value at the same voltage settings. The main transistor parameters from the transistors based on precursor solutions with different amounts of HCl can be seen in **Table 4.2**. These are the mean values and their standard deviation values in parenthesis calculated from four 20 µm channel length transistors each.

Table 4.2: Saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing (S.S.), and on/off-current ratio (I_{on}/I_{off}) for transistors built from precursor solutions with different amounts of HCl. The values in parenthesis represent the corresponding standard deviation calculated from four devices.

HCl content (%)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
0.25	4.16 (±0.10)	8.5 (±0.46)	0.38 (±0.08)	5.4×10^8 ($\pm2.6\times10^8$)
0.50	4.70 (±0.43)	10.9 (±1.22)	0.35 (±0.05)	4.9×10^8 ($\pm1.1\times10^8$)
1.00	3.98 (±0.14)	10.4 (±1.32)	0.51 (±0.01)	1.3×10^8 ($\pm4.3\times10^7$)
5.00	0.32 (±0.03)	15.1 (±0.93)	0.59 (±0.01)	2.0×10^7 ($\pm3.0\times10^6$)
10.00	0.19 (±0.02)	17.3 (±1.40)	0.58 (±0.12)	5.0×10^6 ($\pm1.5\times10^6$)

The highest saturation mobility of 4.70 $cm^2V^{-1}s^{-1}$ was obtained for the 0.50 vol% transistors but this value shows in addition the highest standard deviation in mobility. The transistors made with precursor solutions containing a small amount of HCl exhibit good mobility values around 4 $cm^2V^{-1}s^{-1}$. The mobility of the transistors made with 5 or 10 vol% transistors deteriorates sharply to only 0.19 $cm^2V^{-1}s^{-1}$. As already realized from **Figure 4.20** the threshold voltage values increase with increasing amount of HCl in the precursor solution from 8.5 V (0.25 vol%) to 17.3 V (10.0 vol%). The values of the subthresh-

old swing deteriorates with increasing HCl content. The smallest value of 0.35 V/decade was measured for the 0.50 vol% device and the largest value of 0.59 V/decade for the 5 vol% device. Since the off-currents did not change very much as displayed in **Figure 4.20** (b), the decrease in the on/off-current ratio from the 0.25 vol% transistors with a value of 5.4×10^8 to the 10.0 vol% transistors with a value of 5.0×10^6 is a result of the decrease in on-current values with increasing amount of HCl. The values presented in **Table 4.2** clearly show that using less HCl lead to improved TFT performance. The results reveal that HCl can introduce additional electronic trap states at the ZTO/SiO_2 interface. But it has to be taken into account that if less than 0.25 vol% or no HCl is added to the precursor solution precipitation will occur. At least 0.5 or better 1.0 vol% of HCl is necessary to guarantee a stable long term precursor solution.

To summarize this section it can be said that the ZTO transistor has to be measured in the GB instead of air due to the adsorption of gaseous species, mainly H_2O, which leads to an always 'on' device, large contact resistances and hysteresis. Furthermore the best working devices were achieved for a weight fraction of Zn to Sn of 7:3. The partial replacement of the solvent EtOH by EG could improve the transistor performance as well as the solution parameters for printing. The best working devices were achieved with a volume fraction of 40 % EG. In addition it could be shown that the reduction of HCl in the precursor route will lead to better devices because the amount of charge trap states can be reduced. However a small amount of HCl is necessary to guarantee a stable solution with no precipitation.

4.3 Multiple-layer approach of printed bottom-gate transistors

The main part of this section has been published in Sykora *et al.* [101]. It will be shown how the application of a multiple-layer approach improves the device performance of printed bottom-gate ZTO transistors. In addition, the results of positive bias stress (PBS) tests on two printed TFTs will be presented and discussed.

In order to investigate the electrical properties of nanocrystalline films, printed field-effect transistors were processed on FH substrates. **Figure 4.22** displays the transfer curves of five transistors with a variable number of sequentially printed and annealed ZTO layers on prestructured FH substrates using a 0.1 mol/L precursor solution. The transfer characteristics clearly demonstrate an improvement in transistor properties with an increasing number of ZTO layers. The better performance is visualized by the increasing amplitude and slope of the drain-currents, the increasing on/off-current ratio, and the decreasing hysteresis indicated by the arrows. These results indicate that an increasing number of printed ZTO layers improves the functional layer. The only drawback is the increasing off-current which demonstrates a higher channel conductivity that is due to the larger thickness and probably a better coverage of the SiO_2 channel area. The best transistor performance was achieved by using eight layers. Printing

of additional ZTO layers leads to a slight decrease in transistor performance which could be related to the additional heating steps following the 8th layer. It is believed that after eight layers the additional application of ZTO does not improve the semiconducting/dielectric ZTO/SiO_2 interface anymore and remaining voids and inhomogeneities may even deteriorate because of the additional heating.

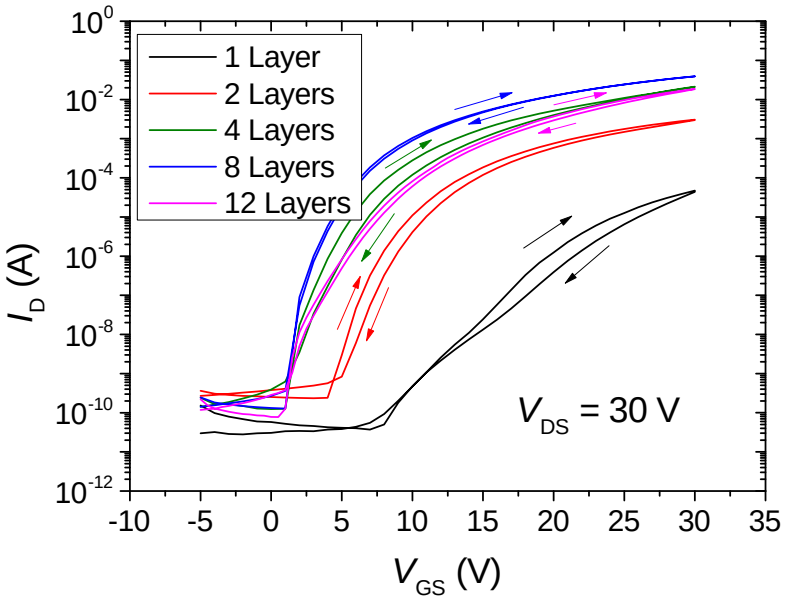

Figure 4.22: Transfer curves of FETs fabricated on FH substrates with an increasing number of printed ZTO layers. The devices were measured at a source-drain voltage $V_{DS} = 30$ V [101].

Figure 4.23 displays the output characteristics of the transistor composed of one (a), two (b), eight (c), and twelve (d) ZTO printed ZTO layers. The solid lines display the drain-currents I_D and the dashed lines the corresponding gate-currents I_G. All curves show a clear gate modulation and saturation behavior apart from the one layered device. The large drain-current of up to 38.7 mA at $V_{DS} = 30$ V and $V_{GS} = 30$ V for the eight layered device can be attributed to the good ZTO film quality and the large W/L ratio. The difference between the forward and the backward sweep of the drain-current is indicated by arrows in the subfigures. This clockwise hysteresis, which is an indication for the existence of electronic trap states, is very large in the one layered device. It decreases drastically from the two to the eight layer device. The twelve layer device shows the reappearance of a pronounced hysteresis which again point to an increase number of trap states. The gate-currents indicated by the dashed lines are at least 20,000 times smaller than the corresponding drain-currents for all devices. The transistor composed of 12 layers exhibits drain-currents that are only 400 times larger than the gate-currents. The higher I_G values are likely to appear because of the greater film thickness and excessive thermal stress.

The extracted transistor parameters including the thickness of the printed layers are displayed in **Table 4.3** for the transistors based on one, two, four, eight, and twelve layers of printed ZTO. All reported values of **Table 4.3** reveal that the transistor with a single layer shows clearly inferior properties to

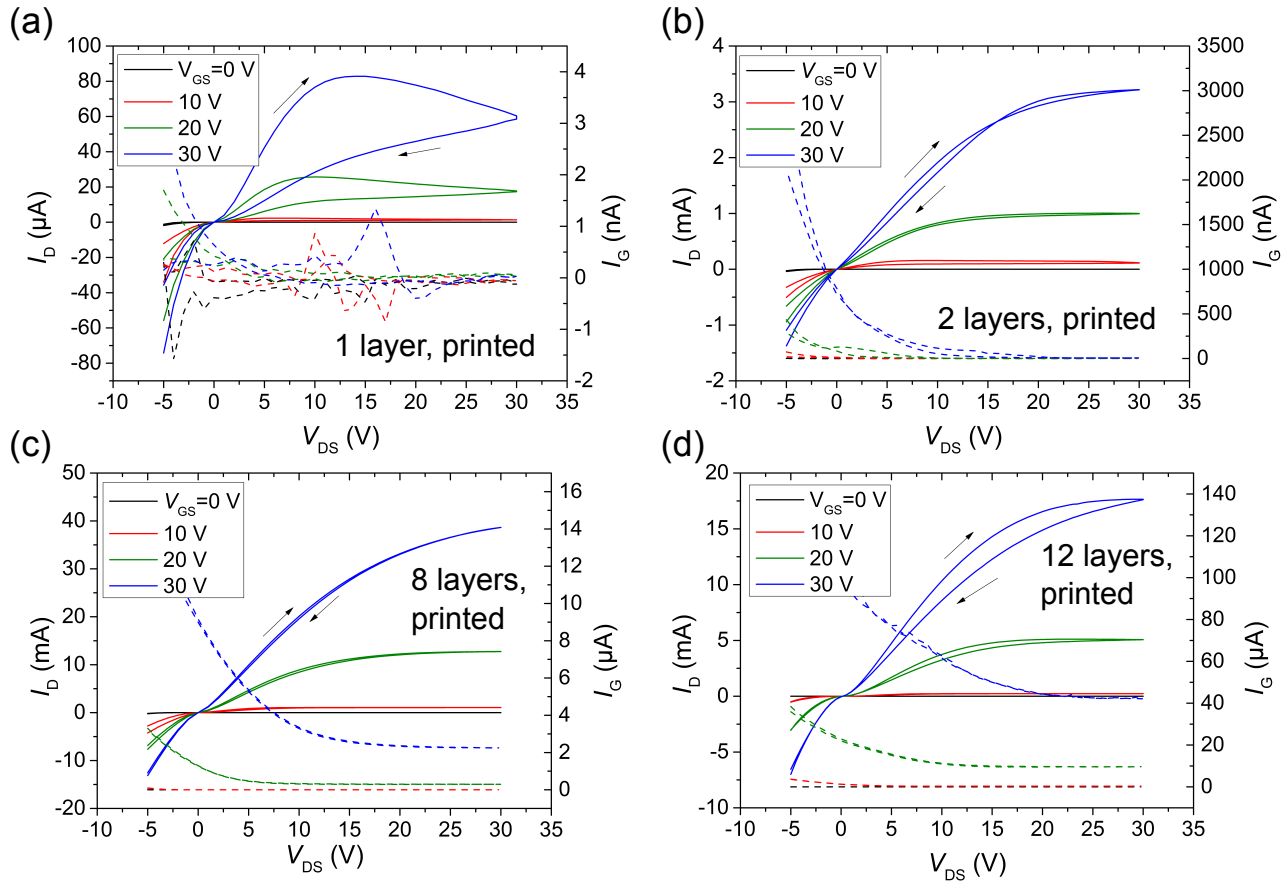

Figure 4.23: Output characteristics of the transistor based on one (a), two (b), eight (c), and twelve (d) printed ZTO layers, measured at source-gate voltages V_{GS} of 0, 10, 20, and 30 V. The solid lines display the drain-currents I_D and the dashed lines the corresponding gate-currents I_G [101].

those with multiple layers. The current values I_D increase by almost three orders of magnitude, and mobilities μ_{sat} increase by a factor of 150. The largest calculated value is 7.8 $cm^2V^{-1}s^{-1}$. In addition, these transistors exhibit high on/off-current ratios I_{on}/I_{off} exceeding 10^8. The decreasing subthreshold swing with increasing number of layers is likewise remarkable. The value of 350 mV/decade for the best transistor is still large compared to common values reported for inorganic metal oxide semiconductor field-effect transistor (MOSFET) of about 70 mV/decade and indicates the presence of trap states at the ZTO/SiO_2 interface. This interpretation can be seen in the observed threshold voltage V_{th} which decreases from 19.6 V to 7.0 V for one to eight layers, respectively. These values indicate a decreasing number of trap states. **Table 4.3** confirms this suggestion and contains the trap density n_{trap} calculated using the equation $n_{trap} = \frac{V_{th}C'}{e}$. Even for the best transistors with eight layers trap states are present. This transistor showed the best performance since the application of another four layers lead to a decrease in mobility and on/off-current ratio and to an increase in the threshold voltage and subthreshold swing.

The peak in the saturation mobility μ_{sat} as a function of the number of applied layers has already been reported by Walker *et al.* [124].

Table 4.3: Layer thickness (t), saturation mobility (μ_{sat}), threshold voltage (V_{th}), trap density (n_{trap}), subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}) for transistors composed of one, two, four, eight, and twelve applied ZTO layers [101].

Number of layers	t (nm)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	n_{trap} (cm^{-2})	S.S. (V/decade)	I_{on}/I_{off}
1	3	0.05	19.6	4.7×10^{12}	1.79	1.3×10^{6}
2	10	0.82	10.0	2.4×10^{12}	0.88	1.3×10^{7}
4	27	6.62	11.9	2.9×10^{12}	0.47	1.7×10^{8}
8	34	7.76	7.0	1.7×10^{12}	0.35	3.2×10^{8}
12	43	6.21	12.3	2.9×10^{12}	0.51	2.4×10^{8}

In order to understand the reason for the different transistor performance the morphology of the printed ZTO films has been investigated by AFM images within the channel region of the corresponding transistors. **Figure 4.24** (a) shows the morphology of a single ZTO layer. One can observe a grain-like structure with a tendency to a small agglomeration on top of a uniformly background. The small grains are most likely ZnO nanoparticles which could be detected in the cross-section TEM image of **Figure 4.5** while the background is due to an amorphous structure. This structure can explain the inferior transistor properties of the single layer device, because electrons face difficulties in finding a conducting path between the source and drain electrode. This results in the rather small electron mobility of around $0.05\,cm^2V^{-1}s^{-1}$. The corresponding rms roughness is 3.68 nm. **Figure 4.24** (b) shows the topography of the printed film with two layers with a rms value of 3.54 nm. The substrate coverage degree is improved but not ideal. The small ring structures are a result of small drops spilling during the printing process. The substrate coverage is further improved if four layers of ZTO were printed as displayed in subfigure (c) resulting in an almost complete coverage and a rms roughness of 3.30 nm. The topography of the eight layer device is shown in subfigure (d). Whereas the rms roughness of 2.77 nm is still in the same order of magnitude as the single, double, or eight layer device, the substrate is, now, completely covered by ZTO. This indicates that the good coverage is most likely responsible for the high saturation mobility of up to $7.8\,cm^2V^{-1}s^{-1}$ and for the above discussed increased conductivity of the transistor channel. The larger rings in **Figures 4.24** (c) and (d) occur because the hydrophilic ink is printed on a more hydrophobic ZTO surface. The twelve layer image of subfigure (e) shows a complete substrate coverage but in addition a larger roughness (rms = 4.91) compared with the film consisting of eight layers (rms = 2.77).

The single layered device and the device composed of eight layers were also examined by the application of positive bias stress (PBS). **Figure 4.25** shows the PBS test of the sample where just a single ZTO

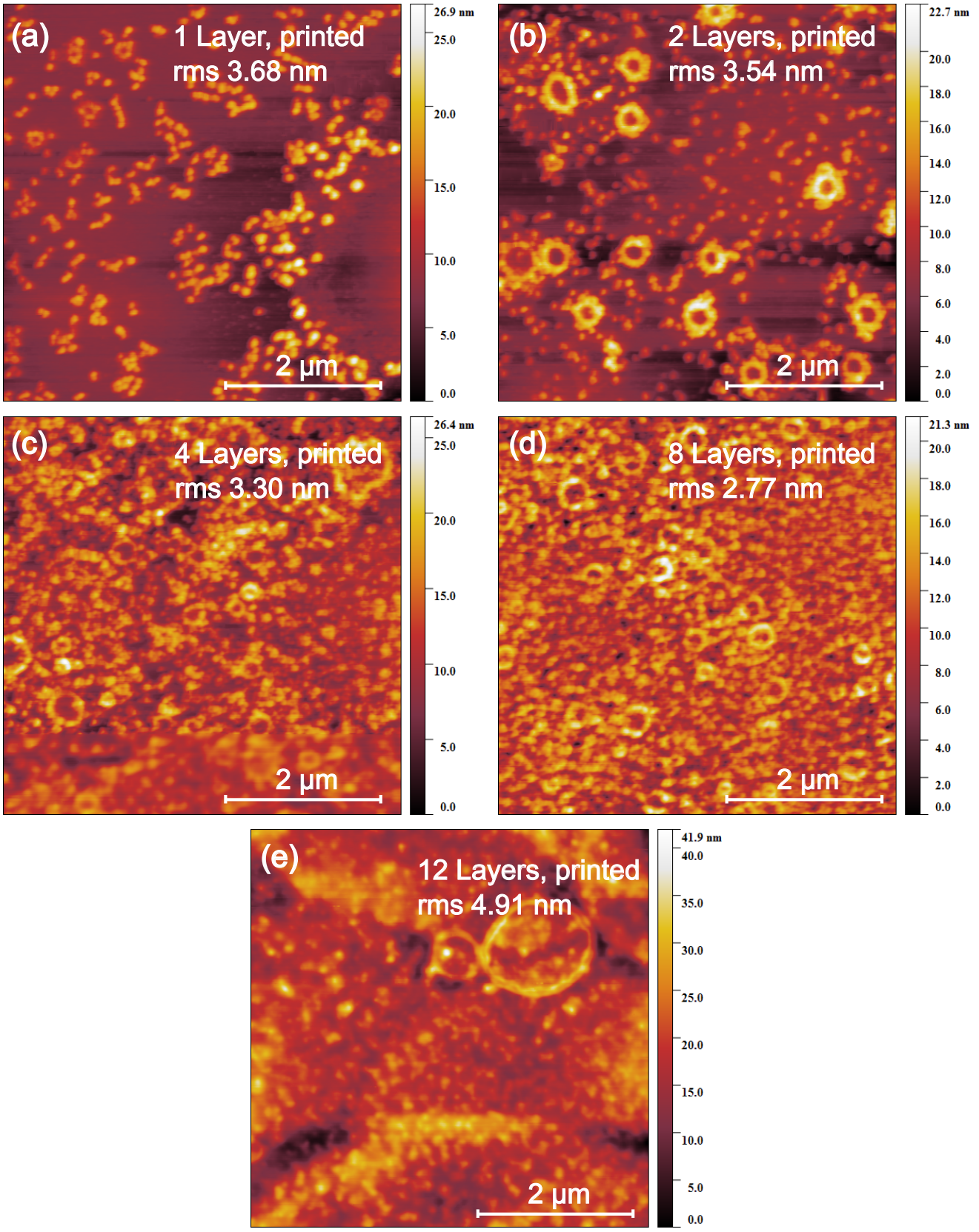

Figure 4.24: AFM images of the printed ZTO for one (a), two (b), four (c), eight (d), and twelve layers (d) recorded within the channel region of the corresponding transistors. The rms roughness values are included in the images [101].

layer was applied via ink-jet printing. A positive bias between source and gate electrode of 30 V was applied for 0, 30, 90, 210, and 510 s. After each stress period the transfer curves were recorded in air.

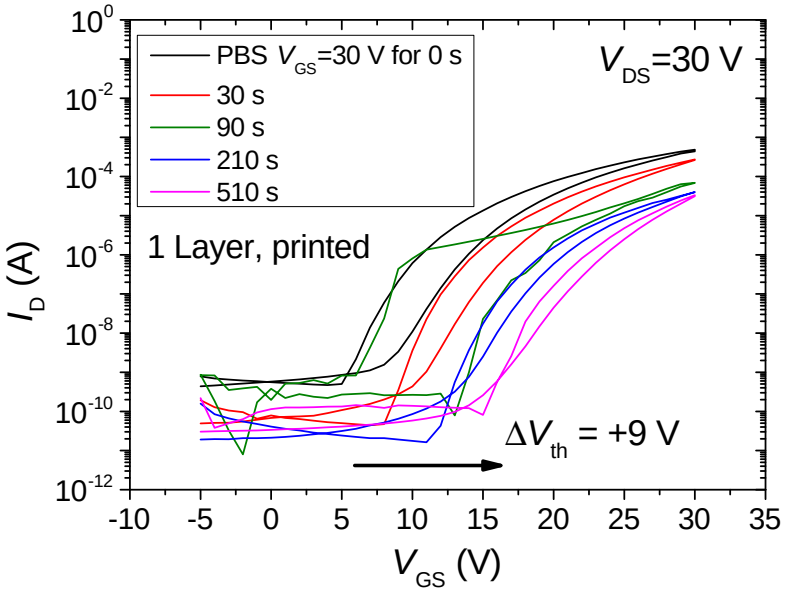

Figure 4.25: Positive bias stress (PBS) test on a printed ZTO transistor composed of one layer. A positive source-gate bias of $V_{GS} = 30$ V was applied for 0, 30, 90, 210, and 510 s and the transfer characteristics at a constant source-drain bias of $V_{DS} = 30$ V was measured.

A clear shift of the threshold voltage to the positive voltage region is visible. The total shift from the non stressed transistor (black curve) to the longest stress time of 510 s (pink curve) is +9 V. This value is quite large but smaller than the positive shift of around 14 V for the same stress conditions reported by Jeong *et al.* for an undoped ZTO film [125]. In addition it has to be mentioned that they measured a fresh and unstressed device for each stress time period in contrast to the results presented here where the stress has been applied successively on the same sample. The present value is comparable to the +8 V shift reported by Chen *et al.* [126]. Their interpretation for spin coated ZTO transistors is an adsorption of O_2 during the application of the bias stress time. Apart from the shift in threshold voltage, smaller off-currents and especially on-currents could be measured with increasing stress time. **Table 4.4** summarizes the effect of increasing stress time on the main transistor properties of this single layered device.

The subthreshold swing values exhibit no great change after PBS, but the saturation mobility deteriorates with increasing stress time. The initial threshold voltage of 14.0 V increase to 23.0 V after PBS of 510 s. The on/off-current ratio does not change significantly. One can say that the one layered device is greatly affected by the PBS.

In order to check if a transistor with a thicker and denser ZTO device is more robust against PBS, the device composed of eight printed ZTO layers was tested. The result is shown in **Figure 4.26**.

Table 4.4: Results of positive bias stress (PBS) on a ZTO transistor composed of a single printed ZTO layer showing saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}).

PBS time (s)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
0	0.199	14.0	1.39	1.0×10^6
30	0.204	18.3	1.07	5.8×10^6
90	0.105	21.6	0.81	8.7×10^5
210	0.034	19.1	1.04	2.4×10^6
510	0.071	23.0	1.28	4.1×10^5

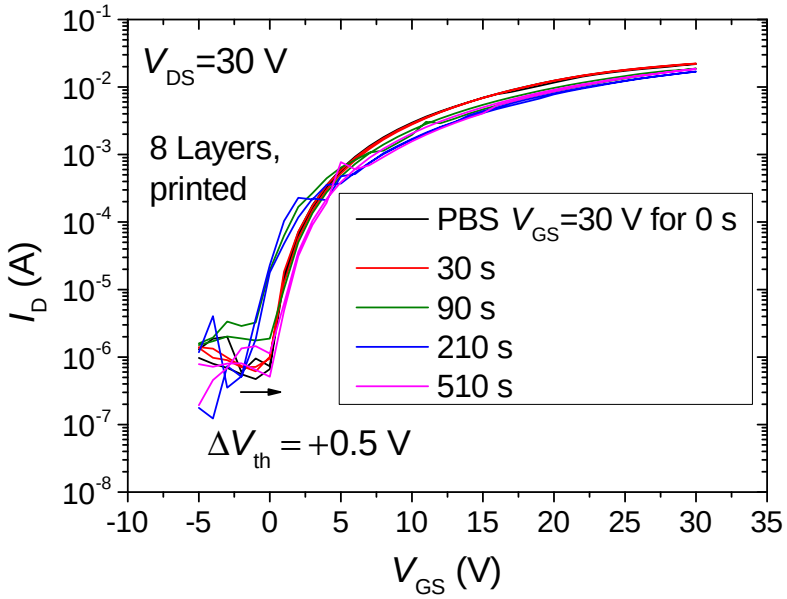

Figure 4.26: PBS test of a printed ZTO transistor composed of eight printed ZTO layers.

The semi-logarithmic plot of the transfer characteristics of this device exhibits no great change under PBS. No big change in the off-currents as well as the on-currents of the device can be seen in **Figure 4.26**. Its main properties as a function of PBS time are displayed in **Table 4.5**.

Table 4.5: Results of PBS of a transistor composed of eight printed ZTO layers showing saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}).

PBS time (s)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
0	3.556	0.8	0.741	3.0×10^4
30	2.493	0.1	0.776	3.1×10^4
90	2.617	0.5	1.402	1.0×10^4
210	2.372	1.3	1.300	3.3×10^4
510	2.565	0.9	1.500	2.7×10^4

The saturation mobility first decreases from $3.556\,cm^2V^{-1}s^{-1}$ of the non stessed device to around $2.5\,cm^2V^{-1}s^{-1}$ after the first stress test for 30 s. After that it does not change significantly. Also the threshold voltage does not change drastically from the non stressed to the dressed device. The subthreshold swing constantly increased from an initial value of 0.741 V/decade to a value of 1.500 V/decade after a PBS of 510 s. The ratio between the on-currents and off-currents are not greatly affected by the PBS.

Compared with the one layered device the device composed of eight layers shows a greater resistance against PBS. A possible explanation for this greater resistance is a semiconductor/dielectric interface of higher quality, where the creation of electronic trap states through adsorbates is less likely. Another reason for the improved stress resistance of the eight layered device compared to the one layered device is the increased thickness of the ZTO layer. Yun *et al.* report that due to a greater thickness of ZTO the electric field and consequently the adsorption of O_2 at the channel is reduced [127].

Taking all results of this section into consideration one can say that increasing the number of ZTO layers leads to a better device performance. The best working device built by eight layers and exhibits a saturation mobility of $7.76\,cm^2V^{-1}s^{-1}$. To the best of the author's knowledge this is the highest reported value for an ink-jet printed ZTO transistor. The reason for this effect could be identified by AFM investigation to be a better degree of substrate coverage. This lead to denser ZTO layers and to a better semiconductor/dielectric interface. After a certain number of layers the transistor performance did not increase any further. A possible explanation for an optimal number of layers could be that the additional heat treatment after the 8th layer lead to a continuous deterioration of the interface quality. In addition it was shown that the transistor based on eight printed ZTO layers has a higher resistance to PBS compared to the transistor based on one printed layer. In the first case the threshold voltage shifted by 9 V in the positive direction after a PBS of 510 s at a constant gate-source bias of 30 V. An explanation can be seen in a better interface quality and a thicker semiconducting layer of the eight layered device.

4.4 Time dependent measurements of printed bottom-gate transistors

Apart from the transistor parameters saturation mobility and threshold voltage it is likewise very important to gain information of how fast a transistor turns from its off to its on-state. The setup of **Figure 3.18** is used to measure the switching speed of two printed ZTO transistors from the preceding section, one with two and one with eight layers. The rectangular voltage signal applied at the gate electrode had the values of 10, 20, and 30 V. The constant source-drain potential V_{DS} was chosen to be 10, 20, and 30 V in order to obtain information of the linear as well as the saturation regime. **Table 4.6** displays the results of these measurements for the eight layered device. The values represent the time necessary to increase the drain signal to 90 % of the saturated value.

Table 4.6: Time in µs as a function of applied V_{GS} and V_{DS} bias values which is necessary to turn a ZTO transistor consisting of eight printed layers into the on-state.

V_{GS} (V)	$V_{DS} = 10$ V	$V_{DS} = 20$ V	$V_{DS} = 30$ V
10	1.932	1.975	1.994
20	1.252	1.394	1.471
30	0.906	0.930	1.085

The switching time increases if the potential difference between the source and drain electrode is slightly increased. An increase in the gate-source potential leads to a strong decrease of the switching time. The shortest time to turn this printed ZTO transistor 'on' was when the gate-source bias had a large value of 30 V and the source-drain potential had a small value of 10 V. These voltage values reveal that the fastest switching time could be obtained in the linear regime of this transistor. Its value of 0.906 µs can be applied to calculate the switching frequency to be 1.10 MHz. The switching time could be further reduced if charging of parasitic capacitors could be avoided [128]. These parasitic capacitors occur due to an overlap of the gate with the source and drain electrodes [129].

Since this transistor has a quite large linear mobility of 1.96 $cm^2V^{-1}s^{-1}$ it will also be investigated how fast a transistor with a smaller linear mobility of 0.87 $cm^2V^{-1}s^{-1}$ turns on. The curves for the determination of the linear mobility can be seen in **Figure 4.27**.

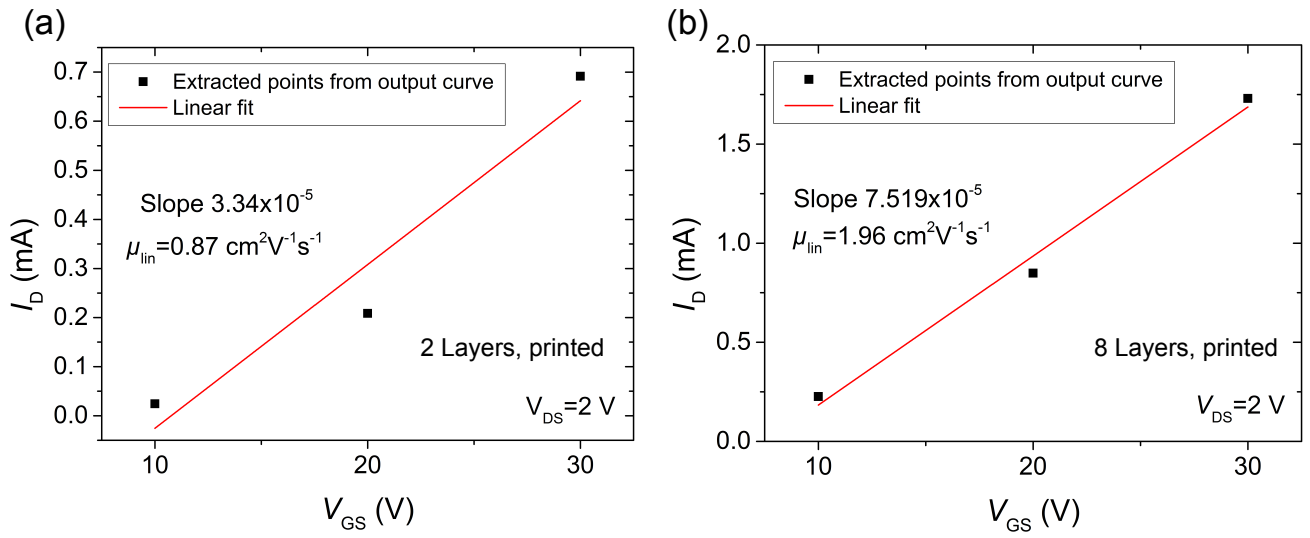

Figure 4.27: Determination of the linear mobility of the two (a) and eight (b) layered device using the method of **Figure 2.10** (a) and **Equation 2.6**.

Table 4.7 summarizes the time dependent measurement results of a printed ZTO device consisting of two layers. In comparison to the eight layered device, the results of the two layered device shows longer switching times if a gate pulse of 10 V is applied. But the results of a 20 or 30 V gate pulse reveal a

shorter switching time compared to the device made of eight layers. The smallest rise time of 0.752 µs results in a switching frequency of 1.33 MHz. This value is 154 ns smaller or 230 kHz greater than the highest switching frequency of the eight layered transistor.

Table 4.7: Time in µs as a function of applied V_{GS} and V_{DS} bias values which is necessary to turn a ZTO transistor consisting of two printed layers into the on-state.

V_{GS} (V)	$V_{DS} = 10$ V	$V_{DS} = 20$ V	$V_{DS} = 30$ V
10	2.862	3.153	3.088
20	1.016	1.063	1.092
30	1.011	0.752	0.755

One parameter, which contributes to the shorter switching time of the two layered device, is the time interval t_0 from 0 s, referring to the time the rectangular gate pulse is turned on, to the beginning of the signal rise. **Figure 4.28** (a) displays the subtracted curve of the transistor with eight layers. It shows the double exponential fit of the subtracted data in red and the 90 % value in blue. The extracted parameters for the fit are: $I_1 = 3.53$ mA, $\tau_1 = 2.38 \times 10^{-7}$ s, $I_2 = 0.13$ mA, and $\tau_2 = 4.86 \times 10^{-6}$ s. The amplitude I_2 of the large time constant of the fit is quite small with only 0.133 mA compared to the small time constant amplitude of $I_1 = 3.53$ mA. The 90 % time value was determined to be 0.906 µs. An enlargement of the onset of this signal is shown in **Figure 4.28** (b). The time interval t_0, that is the time necessary to detect a rise of the voltage signal, of 0.2 µs is displayed in green. The measured current signal of subfigure (a) was shifted by this time interval which results in subfigure (b).

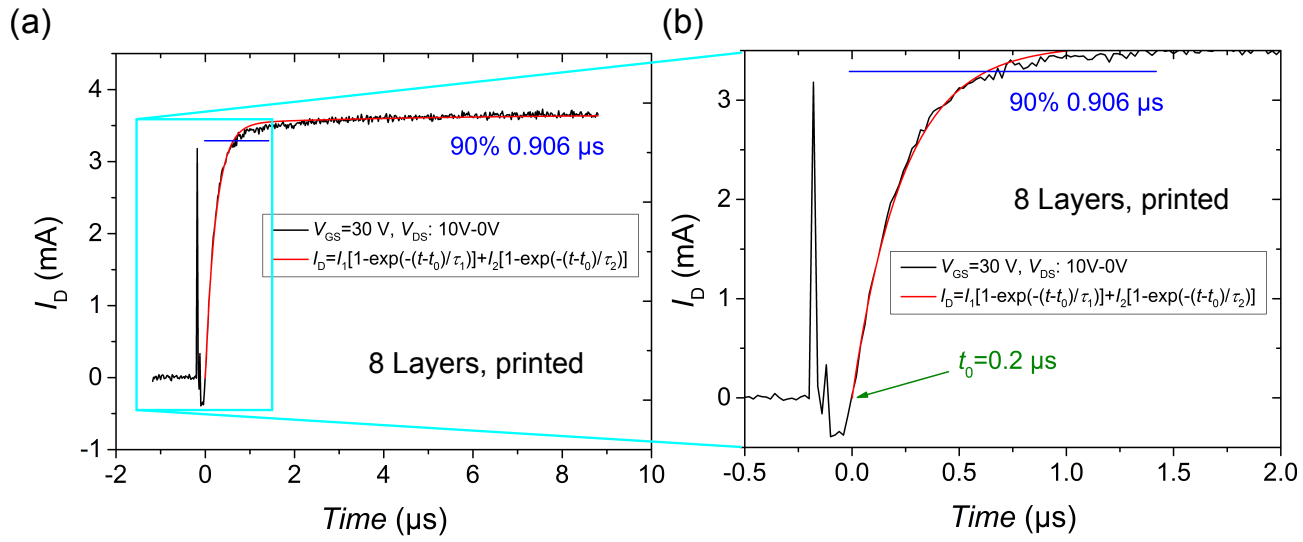

Figure 4.28: Subtracted current signal of the eight layered device including the double exponential fit displayed in red and the 90 % time value (a). Enlargement of the subtracted signal where the current signal from subfigure (a) was shifted by the time interval t_0 of 0.2 µs (b).

Figure 4.29 shows the same as **Figure 4.28** but for the subtracted signal of the transistor composed of two printed ZTO layers. The extracted fit parameters are $I_1 = 1.62\,\text{mA}$, $\tau_1 = 2.15 \times 10^{-7}\,\text{s}$, $I_2 = 0.13\,\text{mA}$, and $\tau_2 = 2.07 \times 10^{-6}\,\text{s}$. The overall amplitude $I_0 = I_1 + I_2 = 1.75\,\text{mA}$ is less than half of the value of the eight layered device. But both time constants are a little bit smaller compared to the fit of the transistor composed of eight layers. The main difference is the shorter 90 % time value of 0.752 µs. The current signal of subfigure **Figure 4.29** (a) was shifted by $t_0 = 0.14\,\mu\text{s}$ in order to obtain subfigure (b). This time interval of the two layered device is 60 ns smaller than the time interval for the eight layered device.

A possible explanation for the additional switching time difference could be the charging of the ZTO capacitor. This capacitor could exist between the source/drain structure, the ZTO film, and the areal gate electrode. Since the degree of SiO_2 surface coverage of the ZTO made out of eight layers is larger than the degree of the two layered device, more time is probably needed to charge this capacitor.

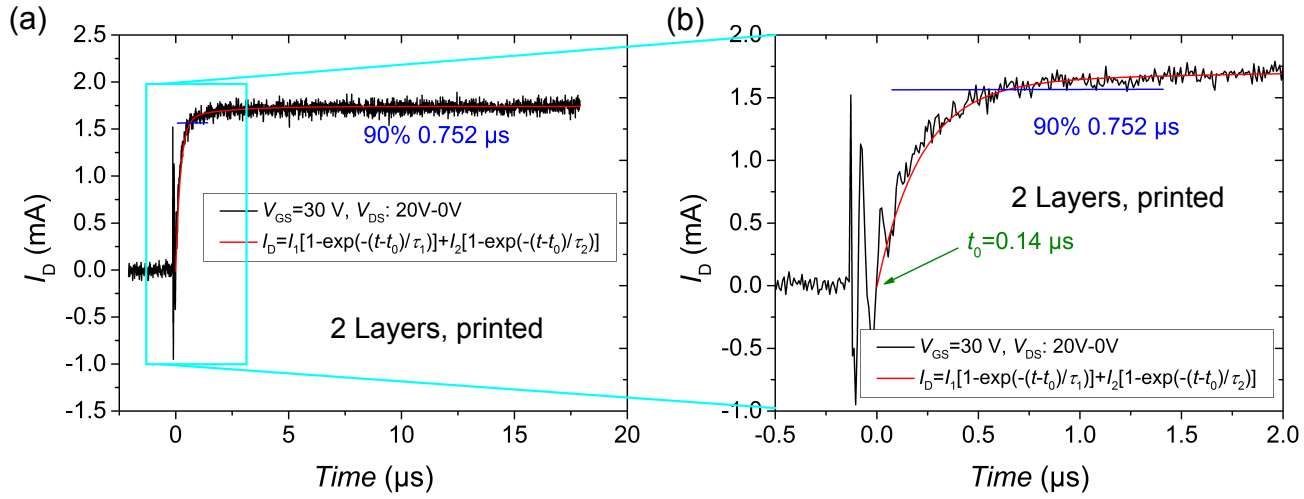

Figure 4.29: Subtracted current signal of the two layered device including the double exponential fit displayed in red and the 90 % time value (a). Enlargement of the subtracted signal shifted by the time interval t_0 of 0.14 µs (b).

To check this assumption the time dependent voltage signal at a gate pulse of 30 V and a source-drain bias of 0 V was measured for the two and eight layered devices (**Figure 4.30**). For these measurements the setup of **Figure 3.17** was used. If a double exponential decay function was applied for the fitting the measured current signal could nicely be fitted (red curves). From these plots the specific time constant τ of the capacitor can be determined. A voltage of 12 V was chosen in order to avoid the noisy maximum value. The time constant or in other words the time span between the time at 12 V and 4.44 V is displayed. The latter value is 1/e $\approx$ 37 % from theory [130]. Applying this value and the overall resistor R of the circuit of 1,000 Ω (**Figure 3.17**) the capacitance C can be calculated according to equation $\tau = RC$, where τ is the characteristic RC-time.

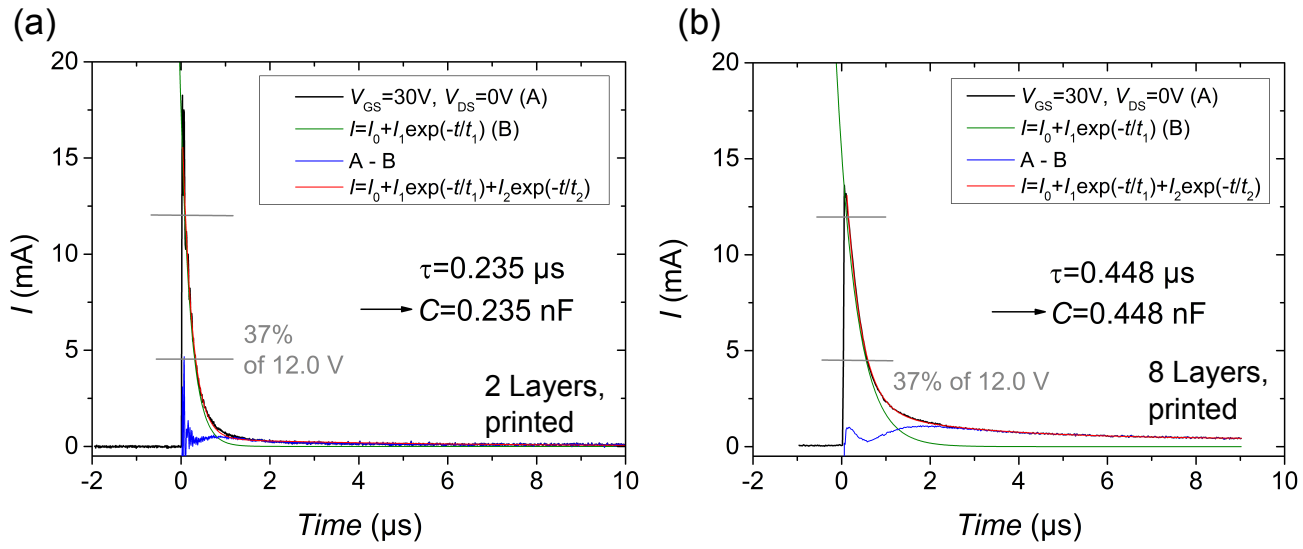

Figure 4.30: Time dependent charging of the capacitor consisting of the electrodes and the ZTO layer at grounded source and drain contacts and a gate pulse of 30 V for the two (a) and the eight layered device (b). The capacitance values can be calculated via the specific time constant τ determined at 37 % of 12 V. The experimental data can be nicely fitted by a double exponential decay function displayed in red. If a single exponential decay function, necessary to charge the electrodes (green curve), is subtracted from the measured signal (black curve) the charging response of the ZTO is obtained (blue curve).

A single exponential decay function (green curves) is not sufficient to fit the measured charging response of the capacitor composed of the electrodes and the ZTO film (black curve). The response of the ZTO film (blue curve) can be obtained if the charging response of the electrodes (green curve) is subtracted from the overall charging response (black curve). It can clearly be seen that the charging of the ZTO film takes longer in the case of the eight layered device of **Figure 4.30** (b) compared to the two layered device of **Figure 4.30** (a). The first small peak in the ZTO charging response (blue curve) is due to the underestimation of the fit of the noisy maximum of the measured signal (black curve). The measured response can nicely be fitted if a double exponential decay function is applied (red curve). The extracted parameters of the double exponential fit in the case of the two layered device are $I_0 = 0$ mA, $I_1 = 0.47$ mA, $t_1 = 4.18\times10^{-6}$ s, $I_2 = 17.46$ mA, and $t_2 = 2.27\times10^{-7}$ s. The parameters for the eight layered device are determined to be $I_0 = 0.38$ mA, $I_1 = 1.66$ mA, $t_1 = 2.66\times10^{-6}$ s, $I_2 = 15.76$ mA, and $t_2 = 3.44\times10^{-7}$ s. The value of I_0 for the eight layered device indicates that it was not possible to completely charge this capacitor after 9 µs. The amplitude of the large time constant I_1 for t_1 is greater for the eight layered device compared to the device composed of two layers. In addition, the amplitude of the small time constant I_2 for t_2 is smaller for the device composed of eight layers compared to the two layered device. In other words the capacitor of the transistor processed using two printed ZTO layers is charged faster than the transistor composed of eight printed ZTO layers. The charging time of the two layered device is 0.235 µs which is close to half the time necessary to charge the capacitor of the eight layered device (0.448 µs).

The corresponding capacitance value of the transistor made out of eight layers is likewise around two times larger compared to the transistor made out of two ZTO layers. The main factor contributing to this difference is that the SiO_2 substrate is not homogeneously covered with ZTO if only two layers are applied according to **Figure 4.24** (b). The difference in charging time could explain the longer switching time of the eight layered transistor compared to the transistor composed of two layers. It could also be said that one can determine the surface coverage degree by measuring the capacitance of the printed ZTO transistor.

In this section time dependent measurements on printed ZTO transistors were performed. The fastest switching time could be measured if the transistor was performing in the linear regime. The two layered device exhibited a shorter switching time compared to the eight layered device. The shortest switching time was measured to be 0.752 µs resulting in a switching frequency of 1.33 MHz. It could be shown that a shorter time interval t_0 for the onset and a faster charging time of the corresponding capacitor could explain this result. The highest switching frequency is 13 times larger than frequency values reported in the literature for AOS transistors using a solid electrolyte gating approach [89, 90]. This approach normally enhances the saturation mobility but not the switching behavior of the AOS. Of course the here reported switching speed is considerably slower than state of the art UHV processed inorganic semiconductors like for instance a $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ heterojunction-based short channel TFT with a switching time of only 0.11 ps resulting in a switching frequency of 9.09 THz [131]. Nevertheless for certain low-demanding RFID-tags the switching speed of the here presented ZTO transistors would be sufficient to fulfill the requirements according to ISO/IEC 18000-2.

4.5 Impact of reduced annealing temperature on bottom-gate transistors

A great obstacle for precursor based AOSs on the way to industrial production is the requirement of high annealing temperatures to transform the precursor solutions to the oxide state. The above described precursor route for ZTO requires 500 °C for the complete decomposition of the precursor as displayed in the TGA of **Figure 4.1**. In this section the results for a reduced annealing temperature are presented. These results were obtained in cooperation with the student Christopher Soon. The transistors were produced by spin coating a ZTO precursor solution of 0.1 mol/L on FH substrates. The substrates covered with thin ZTO films were annealed at a reduced annealing temperature of 350 °C. This temperature was selected because it is the highest possible temperature which the widely used flexible substrate polyimide (PI), better known under the commercial name Kapton®, can sustain. In order to improve the performance of the devices the spin coating and annealing step was repeated several times.

Before the main transistor properties of the two, four, and eight layered devices are displayed, the *I-V*-curves of the best transistors will be presented and discussed. **Figure 4.31** shows the transfer char-

acteristic in the sqrt-plot (a) and the semi-logarithmic plot (b) for a transistor composed of two ZTO layers.

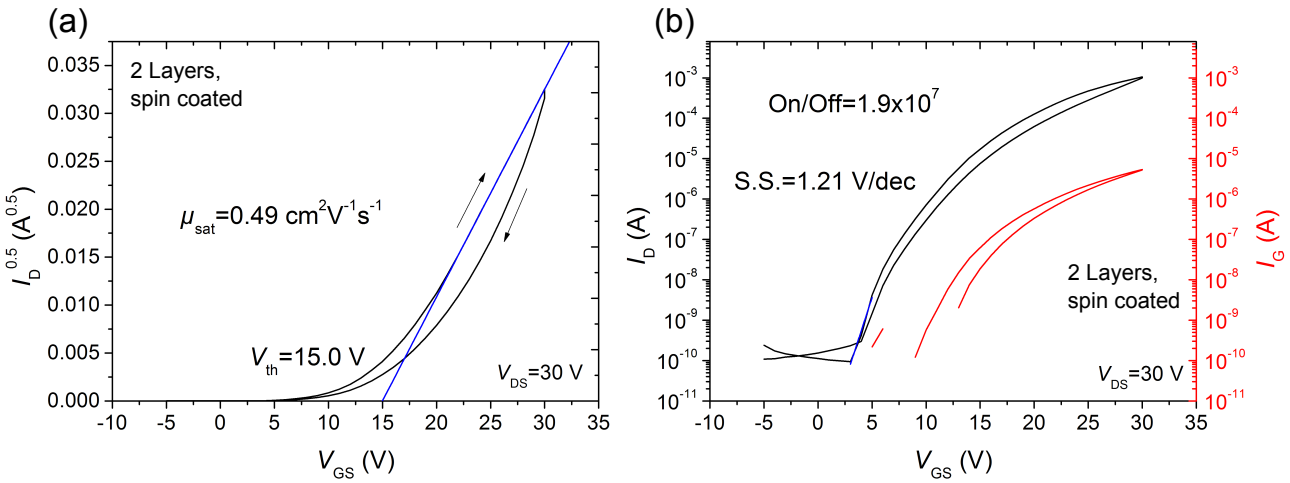

Figure 4.31: Transfer characteristics as sqrt-plot (a) and as semi-logarithmic plot (b) of the two layered ZTO transistor processed by spin coating and annealing at 350 °C on a FH substrate.

Even though only two layers of ZTO were applied to build these transistors and with an annealing temperature of 350 °C a reasonable saturation mobility of 0.49 $\mathrm{cm^2V^{-1}s^{-1}}$ and a threshold voltage of 15.0 V was determined. Remarkable is the large hysteresis between the forward and the backward scan indicated by the black arrows in **Figure 4.31** (a). The reason for this hysteresis is the existence of electron trap states at the ZTO/SiO_2 interface. These are most likely a result of incompletely removed precursor residuals or the adhesion of gaseous species which will be discussed in the next section. From **Figure 4.31** (b) it can be derived that the on/off-current ratio is 1.9×10^7 and the subthreshold swing is 1.213 V/decade. The gate-currents I_G, which are displayed in red, are around 200 times smaller than the corresponding drain-currents I_D. The output characteristics of this device is displayed in **Figure 4.32**.

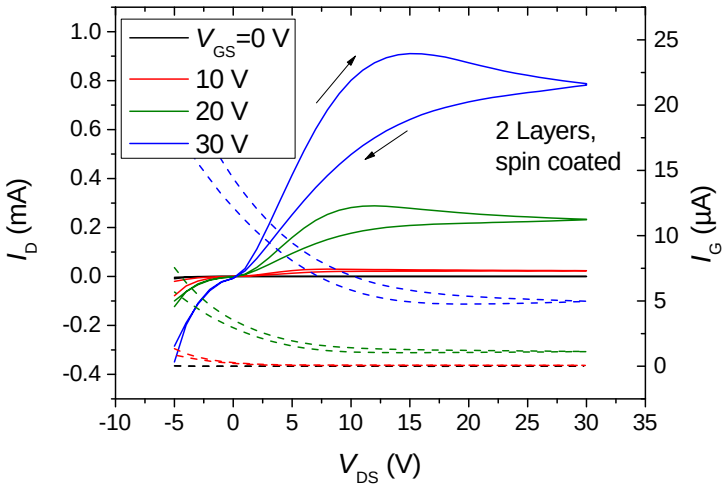

Figure 4.32: Output characteristic of the two layered spin coated ZTO transistor annealed at 350 °C.

The output curves exhibit a pronounced contact resistance and a huge hysteresis, especially if the highest gate-source voltage of 30 V is applied. The scan direction of the hysteresis is again noted by the black arrows in **Figure 4.32**. The dashed curves are the gate-currents which are 150 times smaller than the drain-currents at $V_{DS} = V_{GS} = 30$ V.

In order to improve the transistor performance more layers were applied. **Figure 4.33** shows the transfer and output characteristics if four ZTO layers were processed. All transistor parameters, especially the saturation mobility and the subthreshold swing could be improved compared to the two layered device.

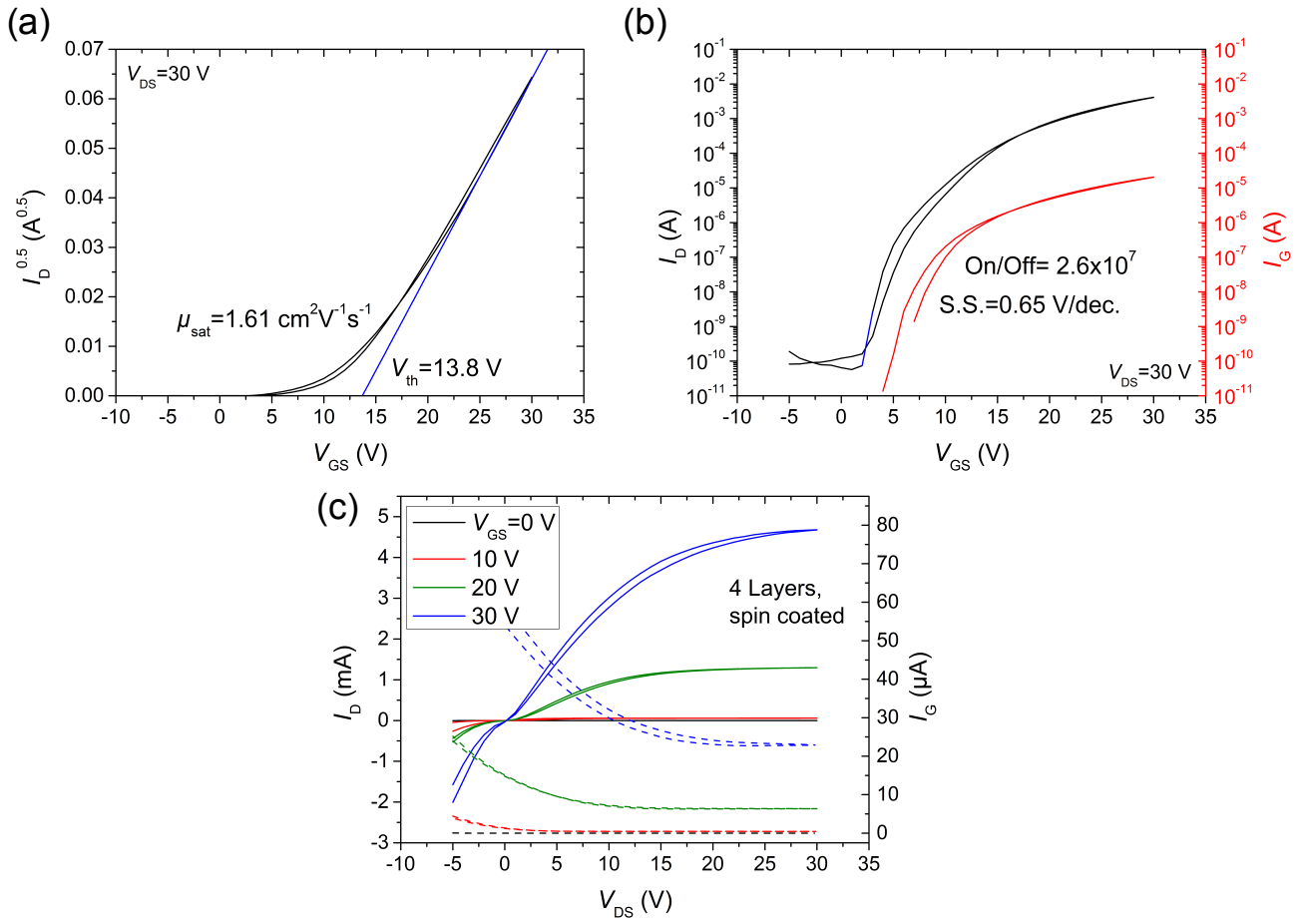

Figure 4.33: Transfer characteristics as sqrt-plot (a) and as semi-logarithmic plot (b) and output characteristic of the four layered ZTO transistor processed by spin coating and annealing at 350 °C on a FH substrate.

The transfer characteristics of the best working device based on eight spin coated layers is displayed in **Figure 4.34**. The saturation mobility has been increased to 3.99 cm^{2}V^{-1}s^{-1} and the threshold voltage of 14.2 V is similar to the two layered device. The hysteresis decreased certainly and is almost not visible anymore. The on/off-current ratio could was further increased to 1.6×10^8 and the subthreshold swing decreased to 0.548 V/decade. The gate-currents increased, but they are still 184 times smaller than the drain-currents.

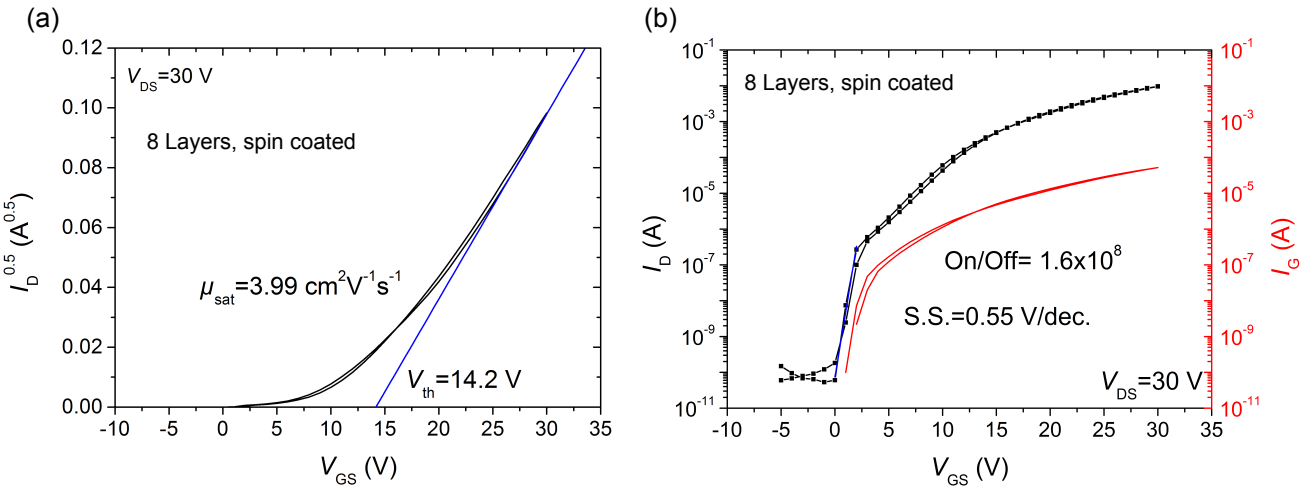

Figure 4.34: Transfer characteristics in the sqrt-plot (a) and in the semi-logarithmic plot (b) of the eight layered spin coated transistor annealed at 350 °C. Since the transfer characteristics shows an abrupt change in current at a $V_{GS} = 2$ V the individual measurement points are shown too.

Figure 4.35 displays the output curves of the eight layered transistor. These curves still show contact resistance. The output curves show almost no hysteresis anymore, which is a result of an improved semiconductor/dielectric interface. The maximum on-current at $V_{DS} = V_{GS} = 30$ V was increased by a factor of 10 compared to the two layered device. These curves now show a clear saturation behavior unlike the output curves of the two layered device in **Figure 4.32**. The gate-currents are 164 times smaller than the drain-currents.

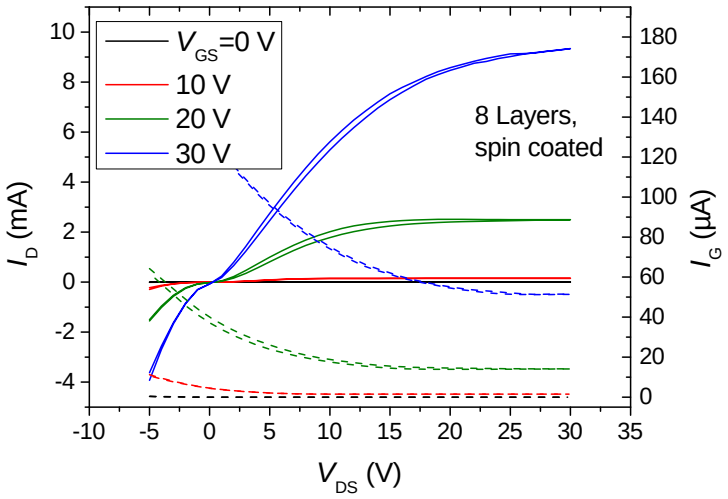

Figure 4.35: Output characteristic of the eight layered spin coated transistor annealed at 350 °C.

The most important parameters of the transistors built by applying two, four, and eight ZTO layers via spin coating and annealing at 350 °C are shown in **Table 4.8**. The displayed values are the mean values of four devices on one FH substrate and the values in parentheses are the corresponding standard deviation values.

Table 4.8: Results of 350 °C annealing experiment showing the saturation mobility (μ_{sat}), threshold voltage (V_{th}), subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}) of the two, four, and eight layered device. The values are mean values of four four working devices with their standard deviation values displayed in parentheses.

Amount of ZTO layers	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	S.S. (V/decade)	I_{on}/I_{off}
2	0.37 (0.12)	17.1 (1.9)	1.33 (0.21)	2.1×10^7 (3.0×10^7)
4	1.33 (0.44)	14.5 (1.8)	0.80 (0.13)	2.6×10^7 (1.0×10^7)
8	3.54 (0.35)	12.7 (1.0)	0.50 (0.09)	8.0×10^7 (5.5×10^7)

The values from **Table 4.8** support the finding of the *I-V*-curves from the two, four, and eight layered device because all transistor properties could be improved if more ZTO layers were applied. The reason for this improvement, a better semiconductor/dielectric interface through improved surface coverage, was already discussed in the preceding section of this chapter. The results of the transistor based on eight applied ZTO layers show especially promising results even if the annealing temperature is reduced to 350 °C. Its saturation mobility is almost two times greater than the value of 1.84 $cm^2V^{-1}s^{-1}$ reported by Yoo *et al.* for a spin coated ZTO transistor annealed at 350 °C [132]. It has however, to be mentioned that their mobility value was achieved for a single layer device but an additional microwave irradiation step was necessary. Without irradiation they only achieved a mobility of 0.15 $cm^2V^{-1}s^{-1}$. Larger saturation mobilities for a spin coated ZTO transistor annealed at 300 °C of up to 5.5 $cm^2V^{-1}s^{-1}$ was reported by Seo *et al.* [133]. Their initial mobility of 5.5×10^{-3} $cm^2V^{-1}s^{-1}$ could be increased drastically by extra post annealing steps in vacuum and wet air.

In this section it was shown that spin coated ZTO transistors produced at a reduced annealing temperature of 350 °C can lead to reasonable device performance. The two layered device exhibits a saturation mobility of only 0.5 $cm^2V^{-1}s^{-1}$ but it was possible to increase it to almost 4 $cm^2V^{-1}s^{-1}$ for the transistor composed of eight layers. The on/off-current ratio shows acceptable values exceeding 10^7. In general, these results suggest that ZTO can in principle also be applied on flexible substrates but further evaluation is necessary.

4.6 Atmospheric effects on bottom-gate transistors

In this section different effects of the atmosphere on the performance of solution processed ZTO transistors shall be presented and discussed. A change in the transistor performance has been recognized if the ZTO devices were transferred into the GB and measured there. The *I-V*-characteristics of the four devices namely A to D of 20 µm channel length with a single ink-jet printed and annealed ZTO layer shown at **Figure 4.22** were measured. 10 minutes went by between the measurement of the first device A

and the last device D. Device A was measured a second time after the measurement of device D. **Figure 4.36** shows the transfer characteristics of these devices in a linear and in a semi-logarithmic plot.

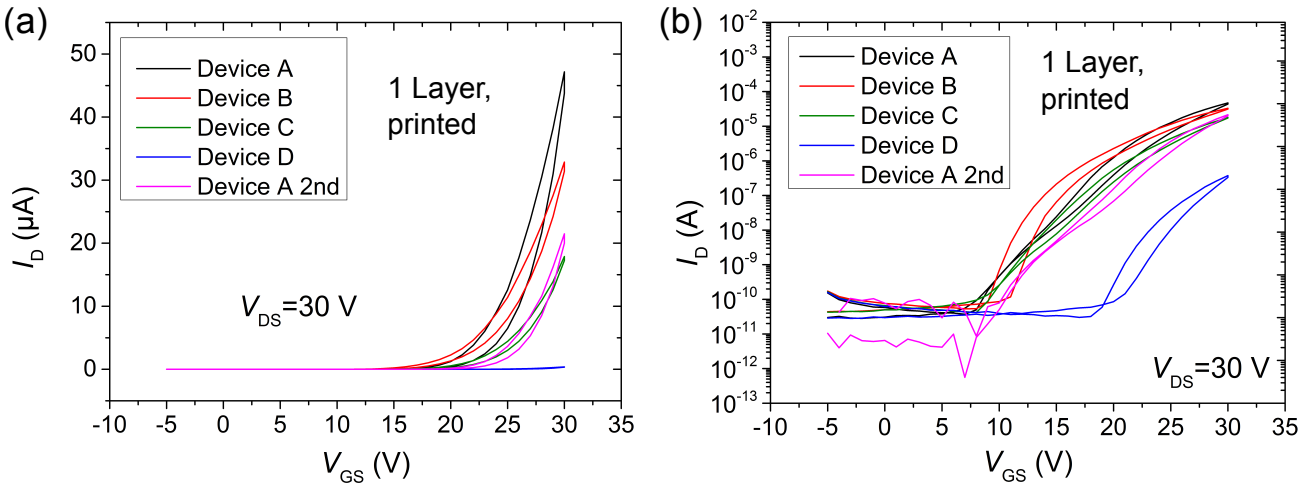

Figure 4.36: Transfer characteristics of four 20 µm channel length transistors of a one layered printed ZTO transistor introduced in **Figure 4.22**. The transistor was introduced into the GB and the devices were measured from A to D. Device A was measured a second time after the measurement of device D. Subfigure (a) shows the linear and subfigure (b) displays the semi-logarithmic plot measured at a constant source-drain voltage of 30 V.

One can already see from the linear plot 4.36 (a) that the drain-currents clearly decrease from measurement to measurement. The more time the transistors spent in N_2 atmosphere in the GB the smaller the on-currents or the higher the threshold voltage. From 4.36 (b) it can be assumed that there is a clear tendency for the shift of the threshold voltage towards higher voltage values, especially for the last measured device D. But it can not be excluded that the device D exhibits in general a worse performance compared to the other devices on this substrate. The off-currents exhibit similar values from transistor A to transistor D. The on-current of the first measured device A also degrade as shown by the second measurement after 15 min the sample spent in the GB. **Table 4.9** summarizes the main transistor parameters extracted from the transfer characteristics of the devices of **Figure 4.36**.

It can be seen that the saturation mobility decreases from the measurement of the first transistor A ($0.046\,cm^2V^{-1}s^{-1}$) to the last transistor D ($0.001\,cm^2V^{-1}s^{-1}$). The already revealed shift in the threshold voltage occurred from 19.6 V of device A to 23.7 V of device D. The decrease in the on/off-current ratio could be connected to the decrease in on-currents from A to D. The subthreshold swing is not affected by the short term storage in an N_2 atmosphere.

In order to check if a thicker film shows a similar behavior a FH substrate was coated with eight ink-jet printed ZTO layers and measured subsequently in the GB. The sample was fabricated according to the device presented in **Figure 4.22**. The measured transfer curves of the devices A to D are plotted on a semi-logarithmic scale in **Figure 4.37**.

Table 4.9: Saturation mobility (μ_{sat}), threshold voltage (V_{th}), maximum drain-current I_D^{max}, subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}) for the four 20 µm channel length transistors A to D of devices with a single ZTO layer. Device A was measured a second time after device D.

20 µm device	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	I_D^{max} (µA)	S.S. (V/decade)	I_{on}/I_{off}
A	0.046	19.6	47.2	2.26	1.3×10^6
B	0.022	17.7	32.9	1.17	6.2×10^5
C	0.020	20.4	17.9	2.43	4.3×10^5
D	0.001	23.7	0.6	1.90	1.2×10^4
A 2nd	0.031	21.5	21.4	2.22	2.7×10^5

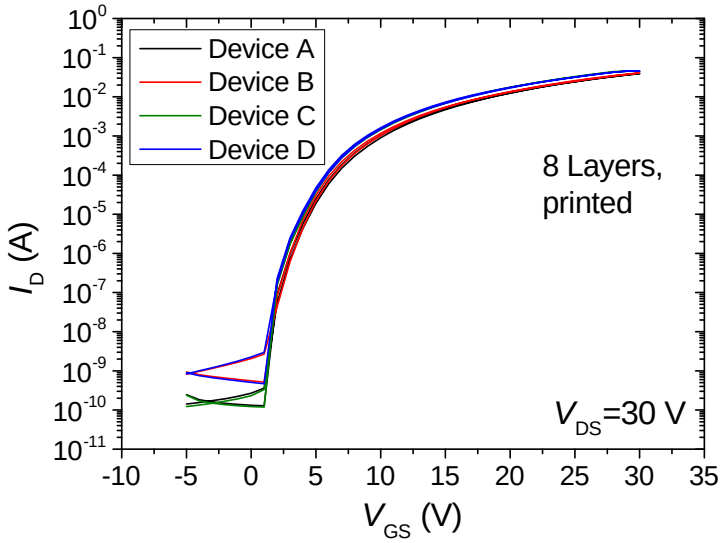

Figure 4.37: Transfer characteristics of four 20 µm channel length transistors of an eight layered printed ZTO transistor introduced in **Figure 4.22**. The transistor was introduced into the GB and the devices were measured from A to D.

Apart from a difference in the off-currents no big change in the threshold voltage and in the on-currents can be detected in contrary to the single layered device of **Figure 4.36**. The most important transistor values of these devices are displayed in **Table 4.10**.

The results from **Table 4.10** could confirm the statement made for **Figure 4.37** because the difference in threshold voltage from the highest value of 7.0 V for device A to the smallest value of 5.8 V for device D is only 1.2 V and shifts slightly to the negative voltage region. This is in contradiction to the trend for the single layered device of **Figure 4.36** and **Table 4.9** where the threshold voltage shifted by positive values. The maximum drain-currents which were extracted from the transfer curves increased from 39.2 mA for device A to a value greater than 45.0 mA for device D. The final current could not be measured because it reached the compliance of the semiconductor parameter analyzer. Similar to the results of the single layered device, the subthreshold swings are not affected by the short term storage within the GB. The

Table 4.10: Saturation mobility (μ_{sat}), threshold voltage (V_{th}), maximum drain-current I_D^{max}, subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}) for the four 20 µm channel length transistors A to D of a device composed of eight printed and annealed ZTO layers.

20 µm device	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	I_D^{max} (mA)	S.S. (V/decade)	I_{on}/I_{off}
A	7.76	7.0	39.2	0.35	3.1×10^8
B	7.86	6.7	40.7	0.45	7.9×10^7
C	9.79	6.3	45.0	0.31	3.8×10^8
D	9.00	5.8	>45.0	0.37	9.6×10^7

values for the on/off-current ratio vary only slightly. Unlike the result of the one layered device the transistor performance of the device based on eight layers did not degrade during short term storage in the GB during the *I-V*-measurement. A possible explanation can be seen by the fact that in this case the SiO_2 substrate is completely covered by ZTO as shown in the AFM micrographs of **Figure 4.24** (d) and N_2 was not able to reach and affect the transistor channel at the ZTO/SiO_2 interface. The SiO_2 substrate of the single layered device was not completely covered, which can be seen in **Figure 4.24** (a) and N_2 can most probably interact with the channel region. Such an explanation was similarly reported in the literature for a solution processed ZnO transistor which can be regarded as comparable to the ZTO transistors presented here [134]. In this regard Ortel *et al.* [134] found a difference in mobility between transistors measured in air and in N_2 atmosphere of 34 % for thin films but only 5 % for thick films exceeding 10 nm.

In cooperation with the student Paula Connor the effect of storage in N_2 atmosphere on bottom-gate bottom-contact transistors was further investigated. Therefore a transistor was processed by spin coating (5000 rpm, 30 s) of two layers of a 0.1 mol/L ZTO solution on the FH substrates. They were initially measured inside the GB and afterwards stored there. The measured transfer curves as a function of storage time within the GB of the two layered device can be seen in **Figure 4.38**.

The figure reveals that the sample storage under N_2 atmosphere had a strong influence on the device performance. It could be seen that the storage lead to an increase in the on-currents as well as the off-currents. The latter is an indication of a general increase in conductivity of the ZTO semiconductor with time in the GB. In addition, the observed hysteresis as a result of electron trap states by O_2 adsorption can be considered to be reduced with storage time. The shift of the threshold voltages towards negative voltages supports this suggestion and can be regarded as a reduction of the electron trap density. **Figure 4.39** shows the evolution of the saturation mobility (black data) and the threshold voltage (red data) as a function of the amount of days spent in N_2 atmosphere. The points represent the mean values and the error bars the corresponding standard deviation values for transistors with a channel length of 20 µm.

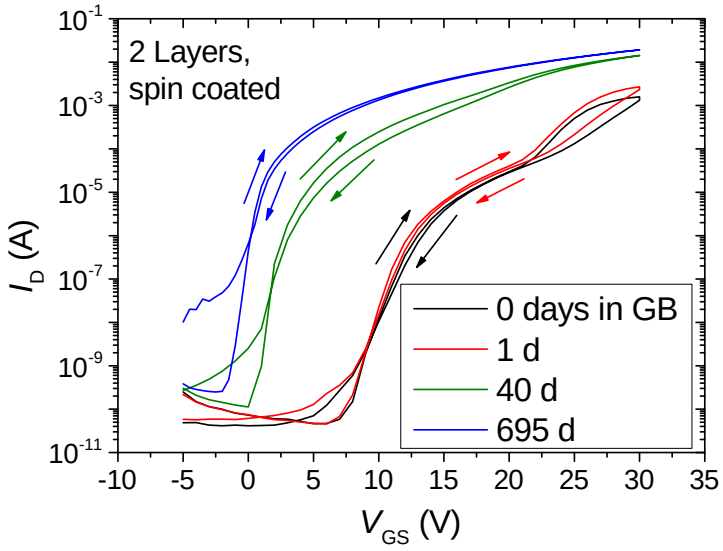

Figure 4.38: Transfer characteristics of a bottom-gate, bottom-contact device composed of two spin coated layers measured after 0, 1, 40, and 695 days in a N_2 filled GB.

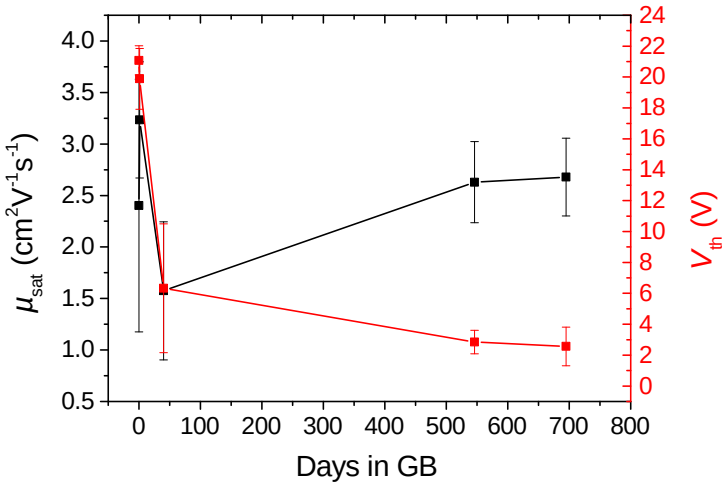

Figure 4.39: Saturation mobility (μ_{sat}) as the black curve and threshold voltage (V_{th}) as the red curve of two layered ZTO bottom-gate, bottom-contact devices as a function of days spent in an N_2 filled GB. The drawn mean values as well as the corresponding standard deviations as error bars were calculated from the four 20 µm channel length devices.

The initial mobility of 3.2 $cm^2V^{-1}s^{-1}$ dropped to a value of 1.6 $cm^2V^{-1}s^{-1}$ after 40 days within the GB. Longer storage times of almost two years under N_2 atmosphere lead to a renewed increase in mobility to values of up to 2.7 $cm^2V^{-1}s^{-1}$. The threshold voltage shows a sharp decrease from the initial value of 21.1 V to 6.3 V after 40 days of storage and keeps decreasing to values as low as 2.6 V after a storage time of 695 days. Both transistor parameters displayed in **Figure 4.39** seem to approach a steady state at long storage time in the GB. The large standard deviation of both parameters for short storage times decrease as well. Keeping the large values of the standard deviations in mind it can be speculated that the saturation mobility does not change considerably over storage time in the GB while the threshold voltage exhibits a drastic decrease. The other two main transistor parameters, on/off-current ratio (green

data) and subthreshold swing (blue data), are displayed in **Figure 4.40** and shows the mean values as well as the standard deviation calculated for four 20 µm channel length transistors.

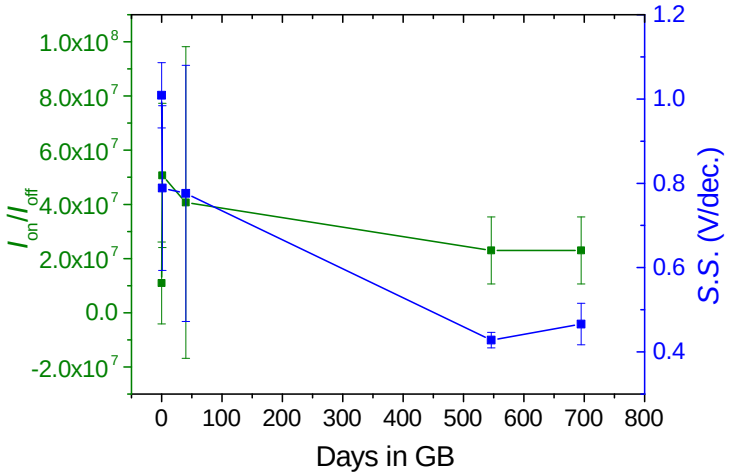

Figure 4.40: On/off-current ratio (I_{on}/I_{off}) as the green curve and subthreshold swing (S.S.) as the blue curve of the two layered ZTO bottom-gate, bottom-contact devices as a function of days spent in an N_2 filled GB. The drawn mean values as well as the corresponding standard deviations as error bars were calculated from the four 20 µm channel length devices.

The initial on/off-current ratio of 1.1×10^7 rises to 5.1×10^7 before it falls to a value of 2.3×10^7 after the long storage time of almost two years in N_2 atmosphere. The sharp increase at first could be explained by an increase in on-current which consequently lead to an increase in mobility (see **Figure 4.39**). A reason for the long term decline of the on/off-current ratio can be seen in the increase in off-currents with storage time. The rise in off-currents as well as on-currents can clearly be seen in **Figure 4.38**. The subthreshold swing decrease from 1.0 V/decade after a storage time of 24 hours to a value of 0.8 V/decade. After leveling off after 40 days of storage it continuous to decrease to a value of about 0.45 V/decade.

The decrease of the threshold voltage as well as the subthreshold swing indicates an improvement of the ZTO/SiO_2 interface. A possible explanation for this effect could be that H_2O and/or O_2, which was adsorbed to the interface after the final annealing step in air, desorbs during storage in N_2 atmosphere. The detachment of these gaseous species is possible because the device is composed of only two thin ZTO layers which do not homogeneously cover the substrate, as demonstrated in **Figure 4.24** (b). In addition it has to be taken into account, that the thickness of the amorphous ZTO layer is only 10 nm so that the gaseous species can penetrate the layer. In order to check how this device behaves if it is brought back into air the following experiment was performed. After a long storage time of 1000 days inside the GB the device was measured within the GB before it was transferred back into air where it was measured after 5 min. **Figure 4.41** shows the transfer characteristic in the sqrt-plot (a) and in the semi-logarithmic plot (b) of this device after the measurement in the GB (black curve) and in air (blue curve).

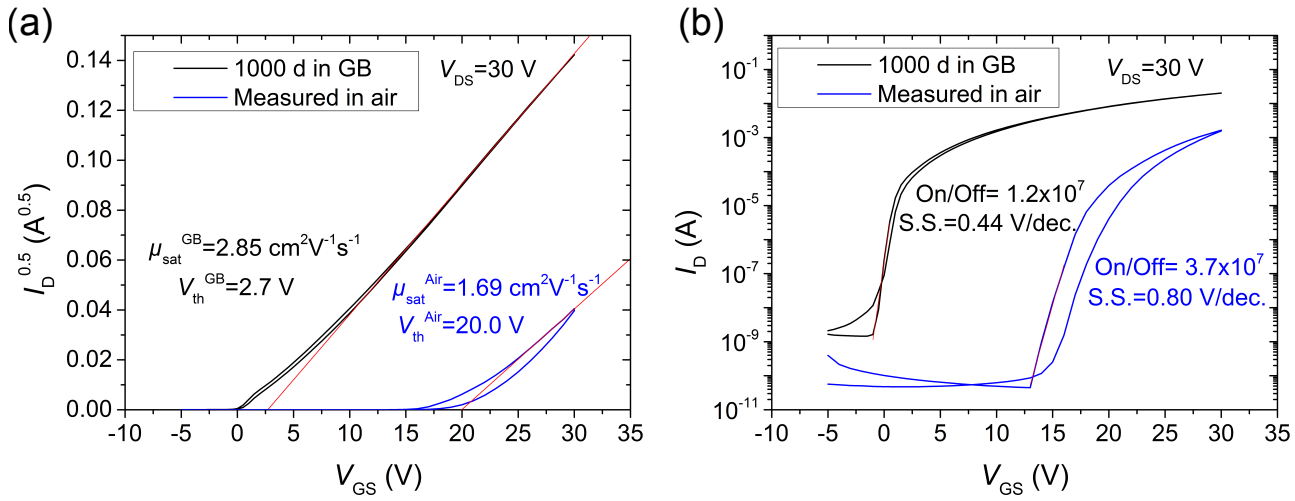

Figure 4.41: Transfer characteristics of a device based on two spin coated layers once measured inside the GB after 1000 days of storage inside the GB (black curves) and once measured in air after 5 min of storage (blue curves). Subfigure (a) displays the transfer characteristics in the sqrt-plot and subfigure (b) shows the transfer characteristic in the semi-logarithmic plot. The most important tranistor parameters are included in the graphs.

As can be seen from the main transistor parameters shown in **Figure 4.41** the performance of the device degrades significantly if it is brought to and measured in air. Not only the threshold voltage shifts by +13 V but also the subthreshold swing almost doubles. Apart from that the hysteresis is more pronounced in air and the on-currents as well as the off-currents decrease clearly. These results indicate an electron trapping mechanism due to oxygen in air.

In this section the effect of the atmosphere by exposing the ZTO transistors to pure N_2 atmosphere was investigated. A short storage of single layer ZTO transistors in a N_2 filled GB lead to a drastic degradation of TFT performance, specifically a pronounced reduction of the on-currents leading to smaller saturation mobility values. This effect can be explained by adsorbed gaseous species, mainly H_2O. If a transistor composed of eight printed layers was stored shortly in the GB no significant change in transistor performance was detected when measured in the GB. Long term storage of a two layered spin coated ZTO transistor showed a drastic reduction in the threshold voltage from the initial value of 21 V to only 2 V after a storage time of up to 695 days. A possible explanation of this effect could be the detachment of H_2O which could act as electronic trap states as discussed in section 4.2.

The decrease in on-currents as well as off-currents in air could be explained by the loss charge carriers. **Figure 4.42** (a) shows a sketch of the ZTO layer in air. O_2 molecules could be adsorbed at the ZTO surface (step (1)). Since O is strongly electronegative it attracts electrons from the ZTO layer (step (2)). As a result O_2^- adsorbates can occur (step (3)). Franke *et al.* [135] described this process in more detail as displayed in **Figure 4.42** (b). The energetic level of the adsorbed O_2 molecules is according to Franke *et al.* [135] close to the Fermi level of the n-type AOS. Therefore the adsorbed O_2 could act as electron

acceptors building O_2^- adsorbates. These electrons originate from intrinsic O vacancies V_O close to E_C and are piled up at the surface of the AOS. This results in the creation of an electron depletion layer of thickness Λ_{air} at the surface. The accumulated electrons at the surface lead to a band bending and to the creation of a barrier height $eV_{surface}$ of up to 1 eV. The oxygen in air could therefore explain the trapping of electrons if the ZTO devices were measured in air. These trapped electrons can be released during the long term storage experiment in the GB leading to an increase of the off as well as on-currents as shown in **Figure 4.38**.

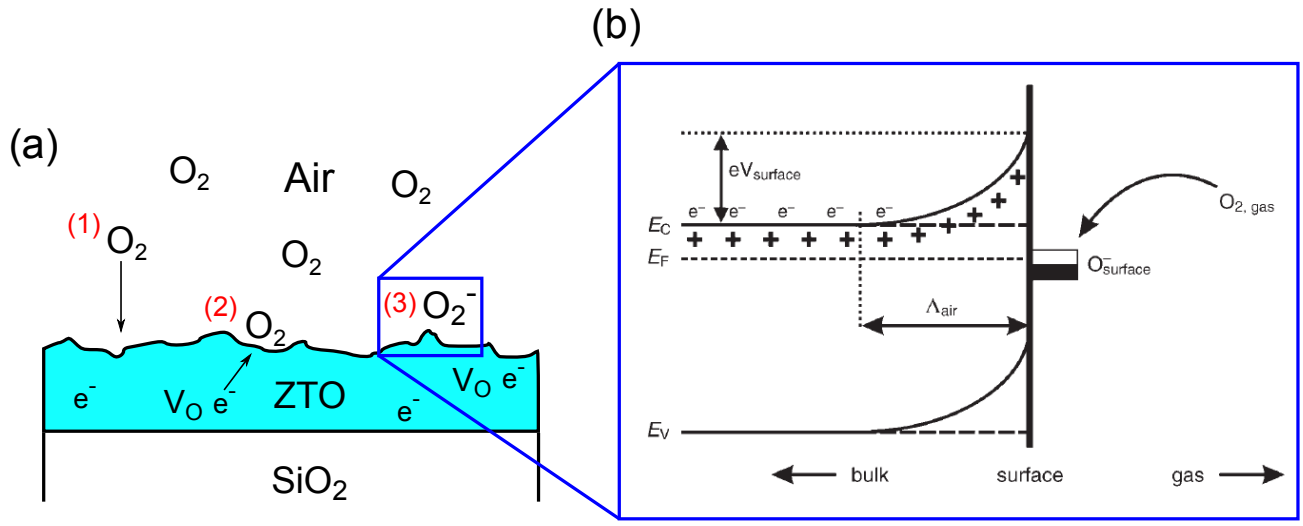

Figure 4.42: Subfigure (a) displays a sketch of the ZTO layer in air. The creation of O_2^- adsorbates can be divided into three steps: First, the adsorption of O_2 molecules at the ZTO surface; second the attraction of electrons to the adsorbed O_2 molecules; Third, the creation of O_2^- adsorbates. Subfigure (b) shows a simplified band diagram according to Franke *et al.* [135] where O_2 is adsorbed on an AOS surface. The accumulated electrons lead to the creation of a depletion region with thickness Λ_{air} and a barrier of height $eV_{surface}$.

The results of this chapter reveal that the analyzed ZTO system may in addition be applied as a gas sensing material. As a matter of fact the combination of ZnO and SnO_2 has already been reported to exhibit good sensitivity in the detection of 1-butanol and dimethyldisulphide [136] or ethanol [137, 138] and its sensitivity towards H_2O and O_2 has been reported too [139, 120].

4.7 Top-gate transistors based on different organic dielectrics

Up to this point only bottom-gate transistors based on SiO_2 as a gate dielectric have been discussed. Before the presentation of top-gate transistors based on different organic dielectrics the quality of these dielectric layers will be presented and discussed. Therefore MIM diodes were processed using the layout shown in **Figure 3.21** of section 3.5. Two different organic dielectric materials were evaluated: on the one hand the widely studied PMMA and on the other hand PAZ 12 as a thin film dielectric. One layer

of 10 wt% PMMA dissolved in *n*-butyl acetate was spin coated at 4000 rpm for 30 s and subsequently dried at 110 °C for 10 min in air in order to evaporate the solvent. In the case of PAZ 12 two layers were applied by successively spin coating each from 3 wt % PAZ 12 dissolved in *n*-butyl acetate at 1500 rpm for 30 s and cross-linked at 250 °C for 10 min on a hotplate in air. The final film thickness was determined by a profilometer. The thickness of the PMMA layer was 470 nm and the thickness of the double PAZ 12 film was 210 nm. As a top electrode 50 nm of gold was evaporated through a shadow mask. The areal capacitance as a function of the measurement frequency can be seen in **Figure 4.43**. The capacitance values were scaled to an equal thickness of 100 nm.

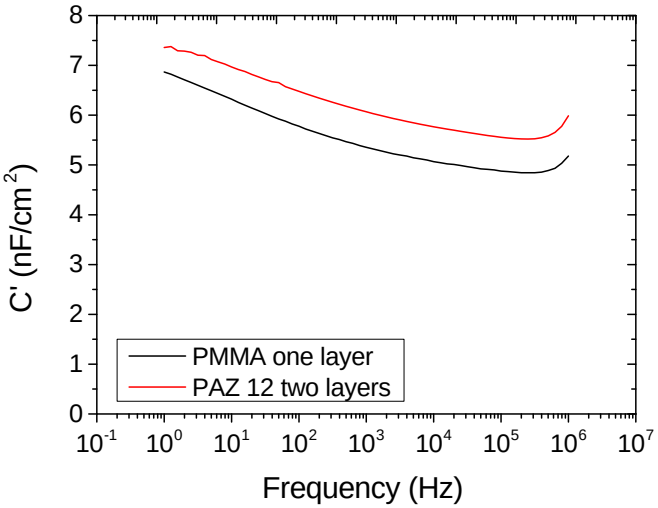

Figure 4.43: Frequency dependent areal capacitance of diodes with PMMA or PAZ 12 as organic dielectric layers. The capacitance values were scaled to a thickness of 100 nm for both dielectrics. The thin film PAZ dielectric was processed as a dual layer but PMMA was processed as a single layer.

The dielectric constant ε_r of PAZ 12 and PMMA could be determined at 10,000 Hz to be 2.87 and 2.68, respectively. The value for PAZ 12 is quite close to the value of 3.0 reported in the literature [76]. The fact that these capacitors were processed in air instead of the GB could probably explain the difference. These values were applied for the calculation of the saturation mobility of the here investigated top-gate transistors. For the top-gate transistors using PS as the dielectric layer an ε_r of 2.5 from literature was applied [140]. PAZ 12 exhibited a slightly larger capacitance compared to PMMA. The loss factor tan δ, which was calculated as stated in section 3.5, as a function of the applied frequency can be seen in **Figure 4.44**. Also the values for the loss factor were scaled to a thickness of 100 nm for both dielectrics. It can be seen from **Figure 4.44** that the PAZ diode shows higher loss factor values in the medium frequency range compared to the PMMA diode. But the PMMA layer exhibits a slightly higher loss factor compared to the PAZ 12 layer in the high frequency range. This result could be explained by the difference in the chemical formula of both materials. PAZ 12 consists of 88 mol% of methyl methacrylate and 12 mol% of benzyl azide which is not present in the pure PMMA film.

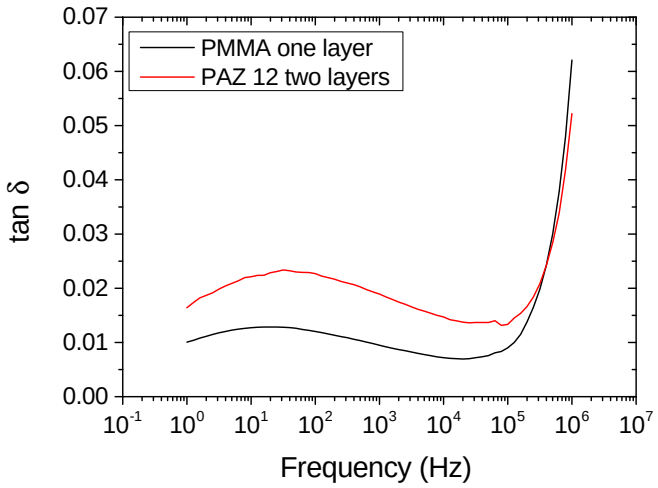

Figure 4.44: Frequency dependent loss factor tan δ of diodes with PMMA or PAZ 12 as organic dielectric layers. The values of the loss factor were scaled to an equal thickness of 100 nm.

Now the results of ZTO top-gate transistors will be presented and discussed. At the beginning PMMA was applied as a dielectric since it is well established in the field of organic FETs. First, the necessary thickness of the PMMA film for a high saturation mobility and small gate leakage-current had to be determined. Therefore two successive ZTO layers were deposited by spin coating (3000 rpm, 30 s) a solution of 0.1 mol/L and subsequent annealing. Two spin coated layers were sufficient to generate decent device performance according to the preceding sections. After the semiconductor was deposited, the samples were transferred into the GB where the PMMA layer was processed via spin coating followed by a drying step at 110 °C. The utilized parameters as well as the resulting thickness are displayed in **Table 4.11**.

Table 4.11: Solution and spinning speed parameters to achieve PMMA films with certain thickness values.

Conc. (wt %)	Speed (rpm)	Thickness (nm)
10	2000	680
10	3000	540
10	4000	490
6	1500	300

As a first step top-gate transistors were processed by using these PMMA layers with different thickness. **Figure 4.45** represents the semi-logarithmic transfer curves of these transistors. It shows the drain-currents (a) and the corresponding gate-currents (b) measured at a constant source-drain voltage of 60 V.

In **Figure 4.45** (a) it can be seen that the on-currents of the top-gate transistors increase with decreasing PMMA thickness. This result is more pronounced if the threshold voltages of the top-gate transistors

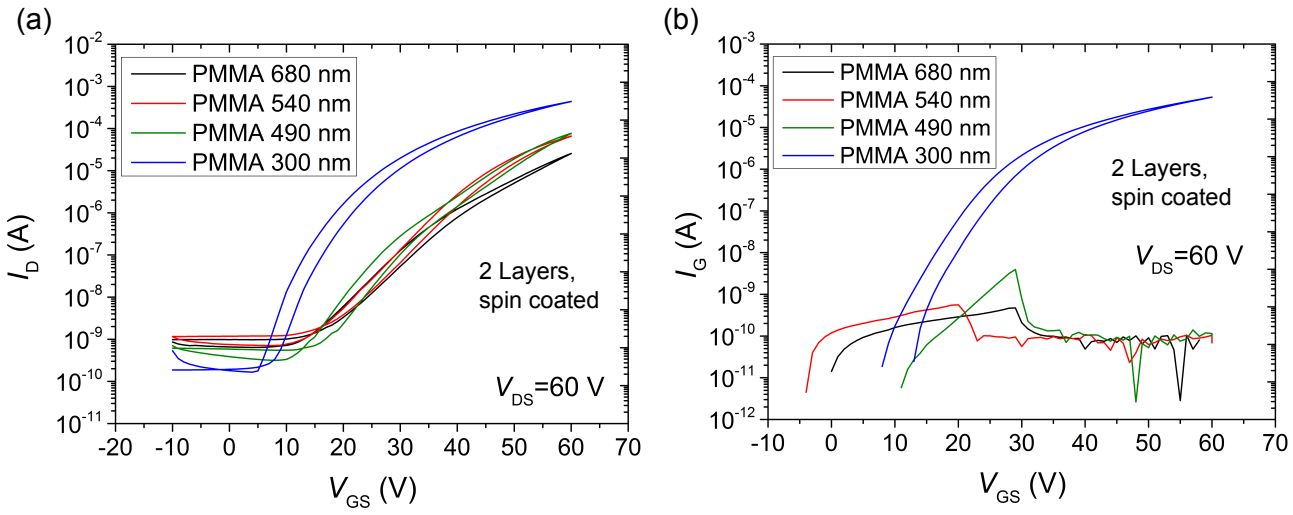

Figure 4.45: Transfer characteristics in the semi-logarithmic plot showing the drain-currents (a) and the gate-currents (b) of top-gate transistors based on a two spin coated ZTO layers in combination with PMMA dielectric layers of decreasing thickness.

were scaled to a common value according to **Figure 4.46**. This was expected since a smaller thickness of the dielectric layer leads to larger electric fields if the applied gate voltage is not changed.

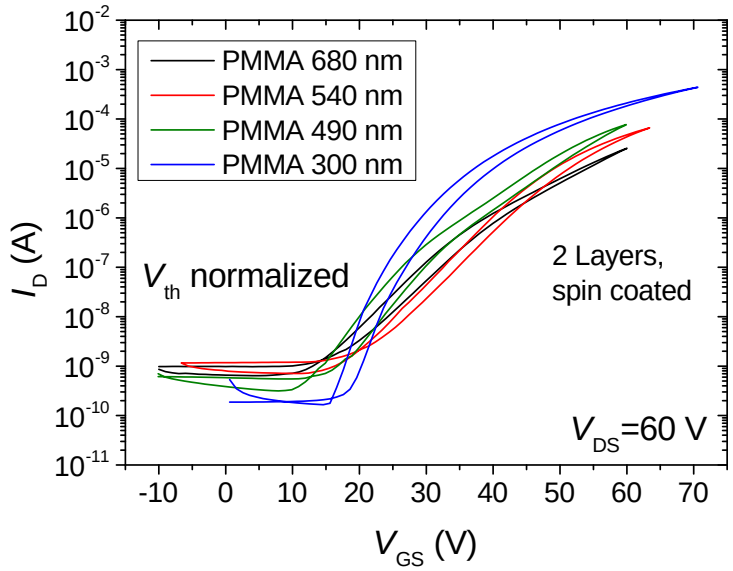

Figure 4.46: Transfer characteristics in the semi-logarithmic plot showing the drain-currents of top-gate transistors based on a two spin coated ZTO layers in combination with PMMA layers of decreasing thickness. The corresponding threshold voltage values were scaled to a common value.

All transistors exhibit similar threshold voltages apart from the transistor with the thinnest PMMA layer. It shows the smallest threshold voltage and subthreshold swing which suggests fewer electron traps at the interface between the ZTO and PMMA layer. But the trap density n_{trap} of this transistor is $1.26\times10^{12}\,\text{cm}^{-2}$ which is greater than the trap density of the transistor with a 680 nm thick PMMA

layer ($8.84\times10^{11}\,\mathrm{cm}^{-2}$). In this case the larger areal capacitance of the thinner PMMA layer has a greater effect on the trap density than the smaller threshold voltage compared to the transistor with the thicker PMMA layer. It can further be noticed that the off-currents decrease with decreasing PMMA layer thickness. The results presented so far suggest that the top-gate transistor with a 300 nm PMMA layer shows the best transistor performance. But **Figure 4.45** (b) reveals that it shows the highest gate leakage-currents exceeding 10 µA at $V_{DS} = V_{GS} = 60$ V. The maximum drain-currents are only 19 times larger than the maximum gate-currents. The other transistors show gate-currents which do not exceed 10 nA.

The high gate leakage could likewise be seen if the output characteristics of the transistors with 488 and 300 nm PMMA are compared (**Figure 4.47**). The output characteristics of the transistor with 488 nm PMMA in **Figure 4.47** (a) exhibits saturation behavior and small gate leakage below 1 nA. All curves traverse through $I_D = 0$ A for various gate voltages and show a small contact resistance in form of the S-shape around $V_{GS} = 0$ V. In addition it exhibits quite large hysteresis especially for $V_{GS} = 60$ V. The output characteristics of the transistor with 300 nm PMMA in **Figure 4.47** (b) show large gate leakage in the µA range. The curves do not traverse through $I_D = 0$ A for different gate voltages which is another proof of large gate leakage of the device.

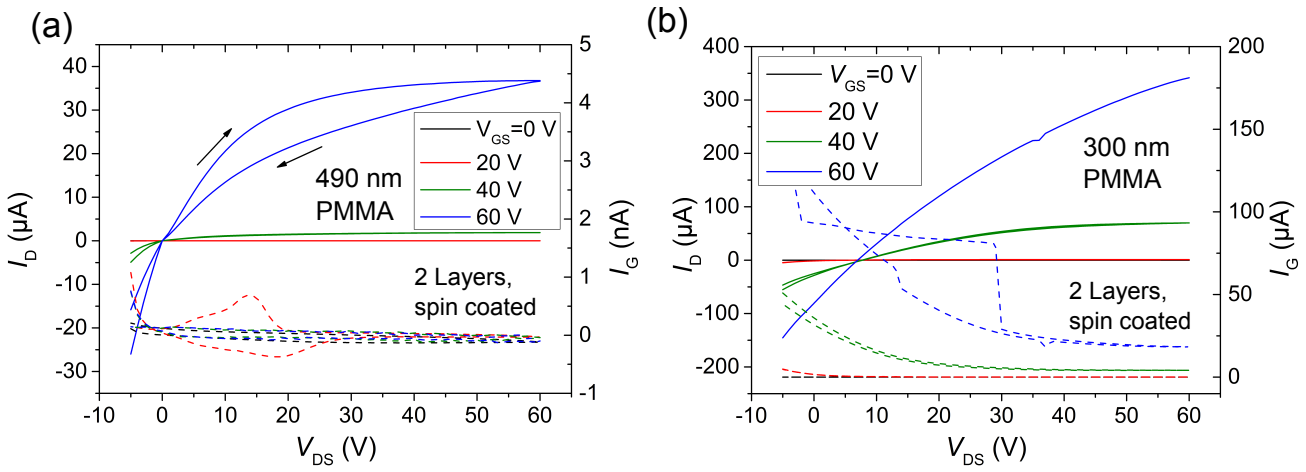

Figure 4.47: Output curves of the top-gate transistors with 490 (a) and 300 nm PMMA (b). The solid lines represent the drain-currents I_D and the dashed lines represent the gate-currents I_G.

In order to check if 300 nm of PMMA would be sufficient for a printed ZTO four layers of ZTO were applied by ink-jet printing of a 0.1 mol/L precursor solution with an EtOH to EG ratio of $\frac{1.5}{1.0}$. Four layers were chosen because the AFM image (**Figure 4.24**) of section 4.3 revealed a complete coverage and good film quality at this amount of layers. Results for this precursor solution were already discussed in section 4.2. Since this precursor solution has a higher viscosity compared to the pure EtOH based precursor solution the cartridge head temperature had to be increased to 35 °C to form stable drops for

printing. The other printing parameters were the same as written in section 4.3. The films were annealed after each printing step. For the deposition of the dielectric material one layer of PMMA was applied in the GB resulting in a thickness of 300 nm. The achieved transfer characteristic in sqrt-plot (a) and semi-logarithmic plot (b) are displayed in **Figure 4.48**.

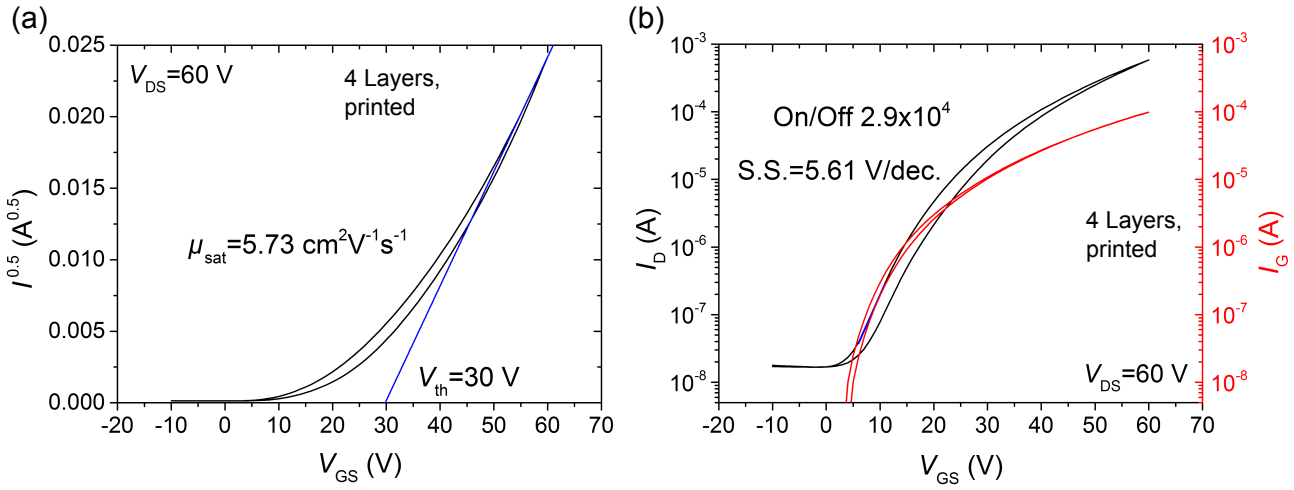

Figure 4.48: Transfer characteristic in sqrt-plot (a) and semi-logarithmic plot (b) of the top-gate transistor based on four printed ZTO layers applied processing a precursor solution with an EtOH to EG ratio of $\frac{1.5}{1.0}$ and a PMMA layer of 300 nm thickness.

Using the slope of the linear plot in **Figure 4.48** (a) a high saturation mobility of 5.73 cm^{2}V^{-1}s^{-1} is obtained at a source-drain voltage of 60 V. The respective threshold voltage is determined to be 30 V. With the help of the semi-logarithmic plot of **Figure 4.48** (b) the on/off-current ratio and the subthreshold swing have been calculated to be 2.9×10^4 and 5.61 V/decade, respectively. The red curve in **Figure 4.48** (b) shows the gate leakage-currents. They reach a value of up to 100 µA, at $V_{DS} = V_{GS} = 60$ V which is only six times smaller than the maximum drain-current. These high gate-currents can be seen in the output characteristics too (see **Figure 4.49**). As already seen in **Figure 4.47** a higher source drain voltage than 0 V has to be applied in order to measure a positive drain-current which is a clear indication for a high gate leakage. Despite the fact that the saturation mobility of this transistor is high, it is not applicable as a device because of the large gate leakage-currents.

Table 4.12 summarizes the main transistor parameters of the top-gate PMMA thickness variation experiment. Looking at the results of the table and the transistor characteristics the best working transistor had a PMMA thickness of 490 nm. It exhibits a quite good mobility of 3.05 cm^{2}V^{-1}s^{-1} while keeping small gate leakage-currents below 1 nA. The device with the largest mobility is not desirable because it exhibits very large gate leakage-currents exceeding 10 µA. In summary it has to be said that all devices display large threshold voltages and subthreshold swings. The on/off-current ratios with values exceeding 10^4 are acceptable. The saturation mobility of 3.05 cm^{2}V^{-1}s^{-1} of the best working device is compara-

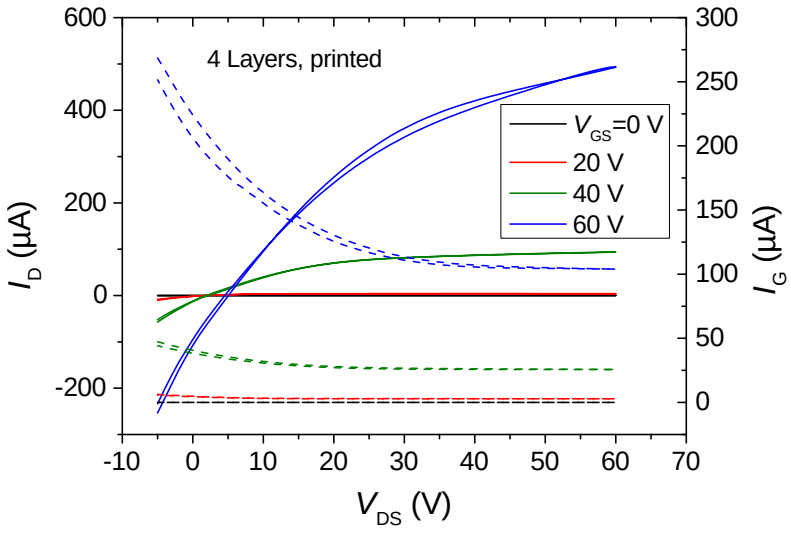

Figure 4.49: Output characteristics of the top-gate transistor based on four printed ZTO layers processed by a precursor solution with an EtOH to EG ratio of $\frac{1.5}{1.0}$ and a PMMA layer of 300 nm. The drain-currents I_D are displayed as solid lines and the corresponding gate-currents I_G as dashed lines.

ble with a value of 3.07 $cm^2V^{-1}s^{-1}$ reported in the literature [141], where spin coated lanthanum (La) doped ZTO in combination with a dielectric PMMA layer were processed. The disadvantage of their La doped transistors is the use of a rare earth metal which is not so abundant in the world. In addition, they report about undoped ZTO transistors that do not exhibit any off-state.

Table 4.12: Results of the PMMA thickness variation experiment of ZTO top-gate transistors showing PMMA layer thickness d_{PMMA}, saturation mobility (μ_{sat}), threshold voltage (V_{th}), maximum drain-current from the output characteristics I_D^{max}, gate-current I_G^{60V} at $V_{DS} = V_{GS}$, subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}). The ZTO layer of the TFT marked with a star was processed using four printed layers with a precursor solution having an EtOH to EG ratio of $\frac{1.5}{1.0}$.

d_{PMMA} (nm)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	I_D^{max} (µA)	I_G^{60V} (nA)	S.S. (V/decade)	I_{on}/I_{off}
680	1.84	40.6	14.8	<0.1	8.48	4.0×10^4
540	2.06	37.2	41.4	<0.1	7.87	9.3×10^4
490	3.05	40.7	36.7	<0.1	6.38	2.4×10^5
300	3.35	25.5	342	18,500	2.63	2.6×10^6
300*	5.73	30.0	342	100,000	5.61	2.9×10^4

All top-gate transistors presented so far exhibit quite large threshold voltages exceeding 25 V. A possible approach to reduce this parameter and, in addition, improve the other transistor parameters could be to reduce the overlap between the source-drain electrodes and the top-gate electrode. This overlap leads to additional parasitic capacitance [142] which could diminish the field-effect. New shadow masks for the source-drain as well as the gate structure were designed. **Figure 4.50** shows the enlargement of the new

masks for the source-drain and the gate structure in black and red, respectively. In addition it shows a microscope image of the channel region defined with these new masks. Although the channel has the same dimension than defined by the old masks displayed in **Figure 3.6** the overlap area between the source-drain and the gate electrode is five times smaller in the case of the new masks compared to the old masks.

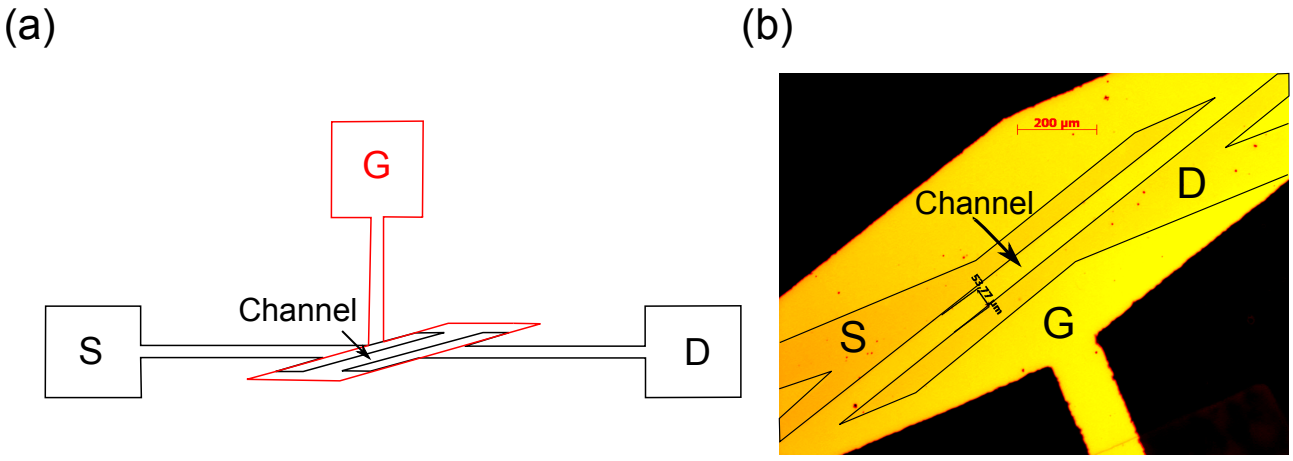

Figure 4.50: Enlargement of the new top-gate masks defining the source-drain electrode (black) and the gate electrode (red) for one transistor (a). A smaller overlap of the source-drain and the gate electrode compared to the old masks displayed in **Figure 3.6** can so be realized. A top view image of the defined channel region using these masks is displayed in subfigure (b).

Using these new masks top-gate transistors were built by successively printing and annealing four ZTO layers. The PMMA dielectric layer with a thickness of 570 nm was applied in air and not in the GB in order to avoid possible environmental effects on the ZTO layer described in section 4.6. **Figure 4.51** displays the transfer characteristics of such a device in sqrt-plot (a) and in semi-logarithmic plot (b).

With the help of the linear fit displayed as the blue line in the sqrt-plot of **Figure 4.51** (a) the saturation mobility of 4.41 $cm^2V^{-1}s^{-1}$ has been obtained. The threshold voltage with a value of 1.7 V is also small especially compared to values presented so far. With the help of the semi-logarithmic plot in **Figure 4.51** (b) the on/off-current ratio and the subthreshold swing could be determined to be 6.1×10^5 and 1.87 V/decade, respectively. The transfer characteristics exhibits a small hysteresis for the different scan directions as indicated by the arrows in **Figure 4.51** (b). In addition, the gate leakage-current shown in red is remarkably small with values less than 1 nA. **Figure 4.52** shows the corresponding output characteristics of this transistor with the drain-currents displayed as solid and the gate-currents as dashed lines.

The output curves exhibit a clear field-effect, but no ideal saturation behavior. The gate leakage-currents are similar to those of presented transfer characteristics (see **Figure 4.51**). They are smaller than 1 nA and all curves traverse through $I_D = 0$ A for various gate voltages. In addition, the output characteristics

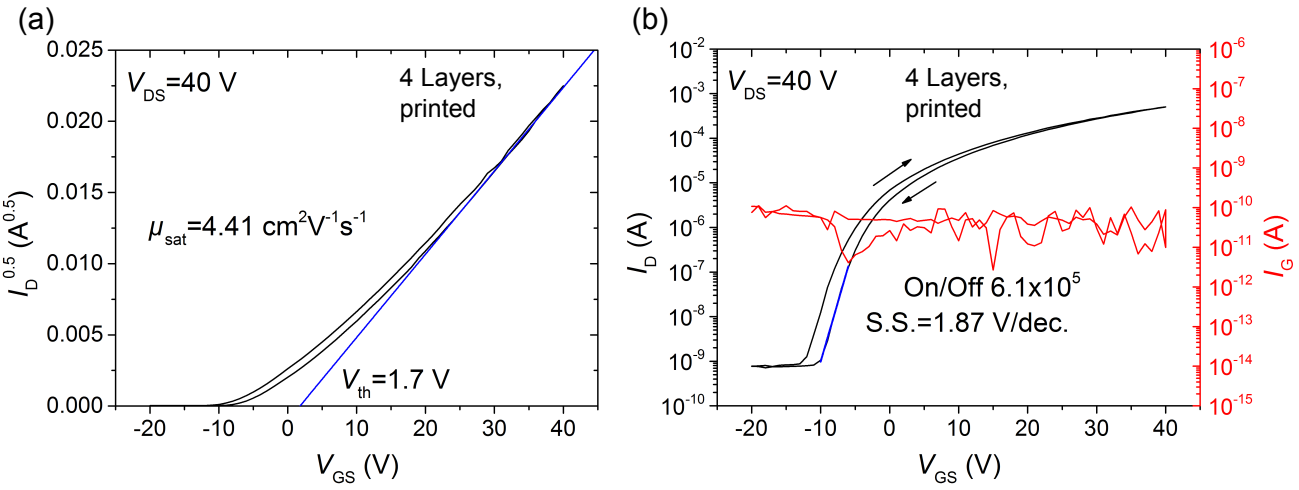

Figure 4.51: Transfer characteristic in sqrt-plot (a) and semi-logarithmic plot (b) of a top-gate transistor based on four printed ZTO layers using new electrode design and a 570 nm thick PMMA layer processed in air.

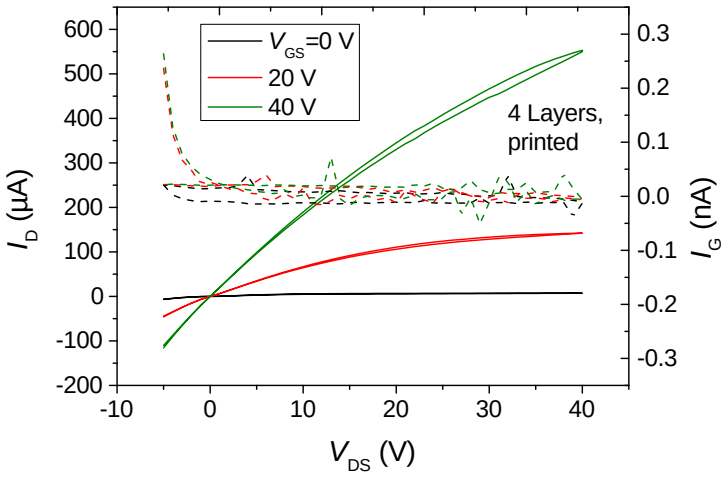

Figure 4.52: Output characteristic of the top-gate transistor based on four printed ZTO layers using new electrode masks and a 570 nm thick PMMA layer processed in air. The drain-currents I_D are displayed as solid lines and the corresponding gate-currents I_G as dashed lines.

show no contact resistance at $V_{DS} = 0$ V. The maximum drain-current at $V_{DS} = V_{GS} = 40$ V reached a value of 555.0 µA.

At this point top-gate transistors applying other organic dielectrics than PMMA will be presented. The transfer characteristic of a transistor based on four consecutively printed ZTO layers and a 630 nm thick polystyrene (PS) layer applying the new electrode design can be seen in **Figure 4.53**.

The saturation mobility is calculated to be 0.15 cm^{2}V^{-1}s^{-1} and the threshold voltage is determined to be 9.7 V at a source-drain voltage of 40 V. The threshold voltage is in an acceptable range but the saturation mobility is small, especially compared to transistors with the PMMA dielectric layer of similar thickness as displayed in **Figure 4.51**. Despite the off-current is smaller than the top-gate transistor using

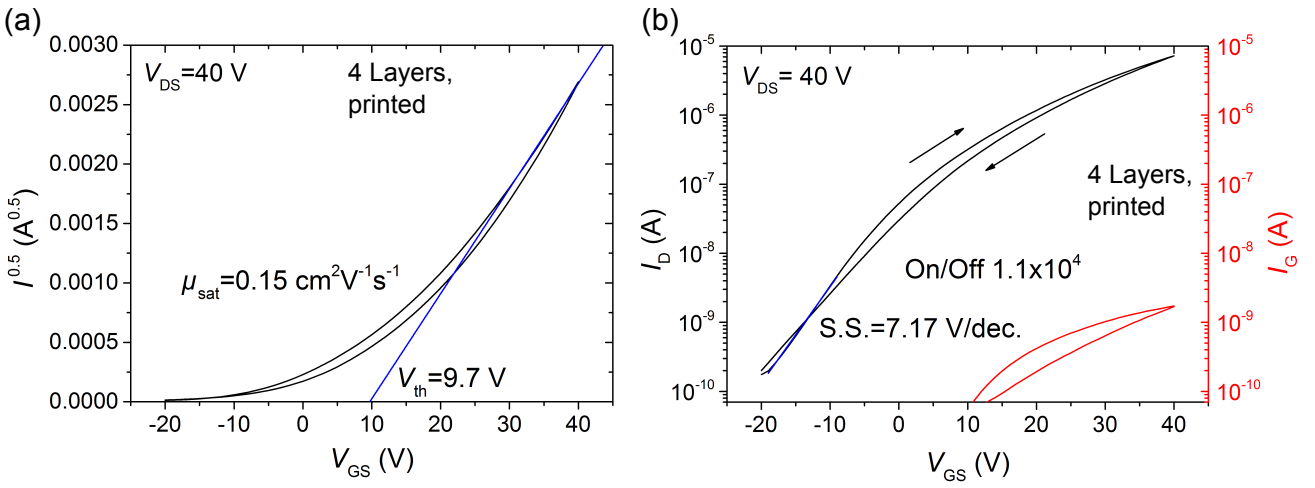

Figure 4.53: Transfer characteristic in the sqrt-plot (a) and semi-logarithmic plot (b) of a top-gate transistor based on four printed ZTO layers using the new electrode design and a 630 nm thick polystyrene (PS) layer processed in air.

PMMA, the on/off-current ratio with a value of 1.1×10^4 is smaller than that of the PMMA transistor. The subthreshold swing of 7.17 V/decade is much larger than the value of the PMMA transistor. In addition, this transistor shows a hysteresis but it is smaller compared to the PMMA transistor. The gate leakage-current shown in red in **Figure 4.53**, is small with a maximum value of 1.7 nA. The output characteristic of this transistor can be seen in **Figure 4.54**.

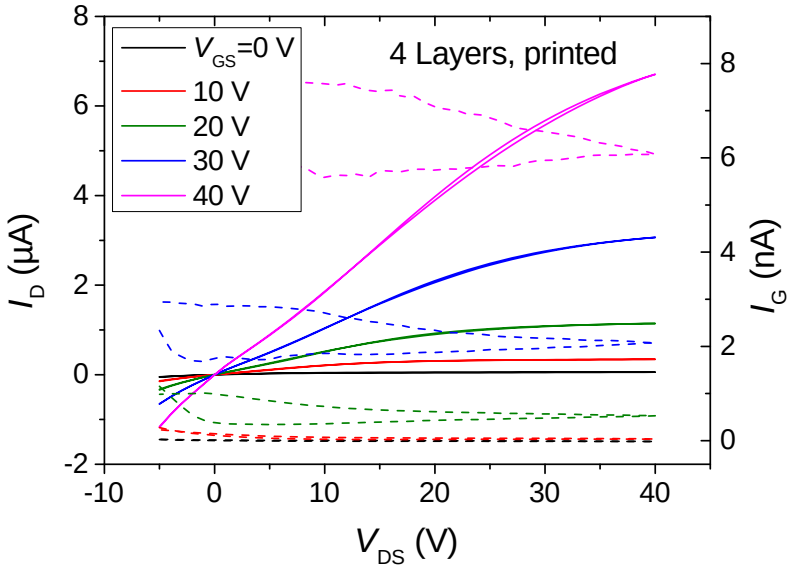

Figure 4.54: Output characteristics of the top-gate transistor based on four printed ZTO layers using the new electrode design and a 630 nm thick PS layer processed in air. The drain-currents I_D are displayed as solid lines and the corresponding gate-currents I_G as dashed lines.

The output characteristics do not show a clear saturation behavior but a pronounced field-effect. They show no delayed current onset as shown in **Figure 4.47** (b) and **Figure 4.49** and the dashed gate leakage-

currents exhibit small values of not more than 8 nA. The maximum gate-current value at $V_{DS} = V_{GS} = 40$ V is almost two orders of magnitude smaller than the maximum drain-currents of the PMMA transistor.

Now the results of top-gate transistors applying benzyl azide containing copolymer (PAZ) 14 as the dielectric layer and four printed ZTO layers are presented and discussed. The PAZ 14 film was processed by spin coating (5000 rpm, 30 s) of two successive layers of a 6 wt % solution of PAZ 14 dissolved in *n*-butyl acetate which were cross-linked on a hotplate in air. Its final thickness was measured to be 270 nm. The transfer curves in sqrt-plot and semi-logarithmic plot are displayed in **Figure 4.55**.

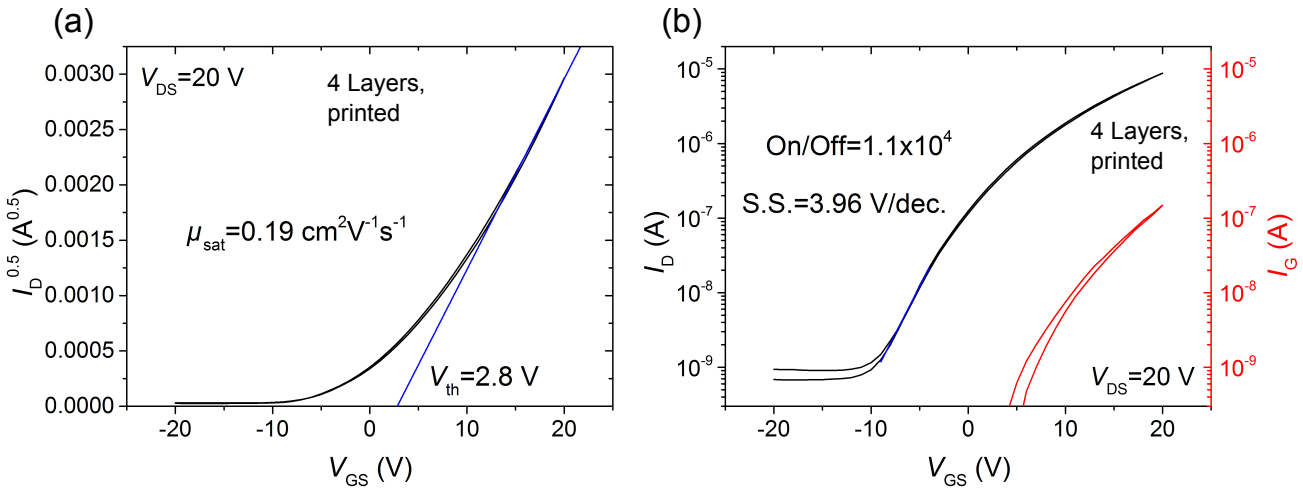

Figure 4.55: Transfer characteristic in sqrt-plot (a) and semi-logarithmic plot (b) of the top-gate transistor based on four printed ZTO layers applying the new electrode design and a 270 nm thick PAZ 14 double layer processed in air.

A value of 0.19 $cm^2V^{-1}s^{-1}$ was obtained for the saturation mobility which is slightly higher than the mobility of the PS transistor but much smaller than that of the PMMA transistor. But it has to be taken into account that the mobility of the PAZ 14 transistor is obtained for a smaller source-drain voltage of 20 V instead of 40 V for the PMMA transistor. The threshold voltage exhibits a small value of only 2.8 V. It is around 7 V smaller than the value of the PS transistor but 1 V larger than the PMMA transistor value. The on/off-current ratio is quite small with a value of 1.1×10^4. The subthreshold swing of 3.96 V/decade is not small, but still 3 V/decade less than the value of the PS transistor and more than 2 V/decade larger than the value of the PMMA device. The gate leakage-current with a maximum value of 0.15 µA at $V_{DS} = V_{GS} = 20$ V is also bigger than the values of the PMMA or PS transistors. An advantage of this device is that it does not exhibit any hysteresis unlike the PMMA and PS transistor. In addition, no sign of hysteresis is visible in the output characteristic shown in **Figure 4.56** as well.

The output curves in **Figure 4.56** exhibit a clear field-effect but no pronounced saturation behavior. In addition, it can be seen that a current of 0.12 µA can be measured even though 0 V is applied between the source and gate electrode. This indicates that the amount of electrons in the ZTO film is large enough

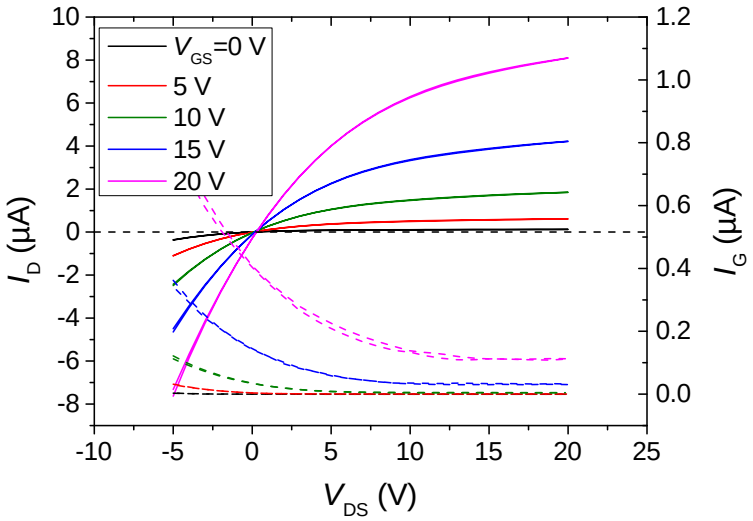

Figure 4.56: Output characteristic of the top-gate transistor based on four printed ZTO layers applying the new electrode design and a 270 nm thick PAZ 14 layer processed in air. The drain-currents I_D are displayed as solid lines and the corresponding gate-currents I_G as dashed lines. A dashed black line is introduced to highlight the $I_D = 0\,\mu A$ value.

for a current transport without the introduction of additional electrons by the field-effect. No contact resistance can be detected but a little current onset difference at $V_{DS} = 0\,V$ is visible.

Table 4.13 summarizes the obtained characteristic parameters of the top-gate transistors based on four printed ZTO layers with three different organic dielectric materials: PMMA, PS, and PAZ 14.

Table 4.13: Results of top-gate transistors built of four layers of printed ZTO and the organic dielectrics PMMA (570 nm), PS (630 nm), or PAZ 14 (270 nm). It shows the saturation mobility (μ_{sat}), threshold voltage (V_{th}), maximum drain-current from the output characteristics I_D^{max}, gate-current I_G at $V_{DS} = V_{GS}$, subthreshold swing (S.S.), and the on/off-current ratio (I_{on}/I_{off}).

Dielectrics	μ_{sat} ($cm^2V^{-1}s^{-1}$)	V_{th} (V)	I_D^{max} (µA)	I_G (nA)	S.S. (V/decade)	I_{on}/I_{off}
PMMA	4.41	1.7	555.0 (@40 V)	0.65	1.87	6.1×10^5
PS	0.15	9.7	6.7 (@40 V)	6.0	7.17	1.1×10^4
PAZ 14	0.19	2.8	8.1 (@20 V)	110	3.96	1.1×10^4

The PMMA transistor shows the best values in all transistor parameters. Remarkably, the saturation mobility with a value of 4.41 $cm^2V^{-1}s^{-1}$ is more than 20 times larger than the mobilities of PS or PAZ 14 transistors. This value is 1.4 $cm^2V^{-1}s^{-1}$ higher than the value reported in the literature by Yue *et al.* [141]. The threshold voltage of 1.7 V is notably small and similar to the value reported in the above mentioned publication. The maximum drain-current at $V_{DS} = V_{GS} = 40\,V$ of 555 µA is almost 15 times larger than the published value of 37 µA. In addition, the maximum gate leakage-current of 0.65 nA is sufficiently smaller than the published value of 0.7 µA.

Despite the fact that the PS as well as the PAZ 14 transistor were processed exactly the same manner as the PMMA transistor, the parameters of the PS and PAZ 14 devices show inferior values. If the results of the PMMA and PS transistor are compared, even the dielectric thickness values are comparable. One possible explanation for the inferior transistor performance could be found in a bad interface between the organic dielectrics and the top-gate electrode. In order to determine how smooth the surface of the PMMA and PS layers are, AFM images were taken (**Figure 4.57**).

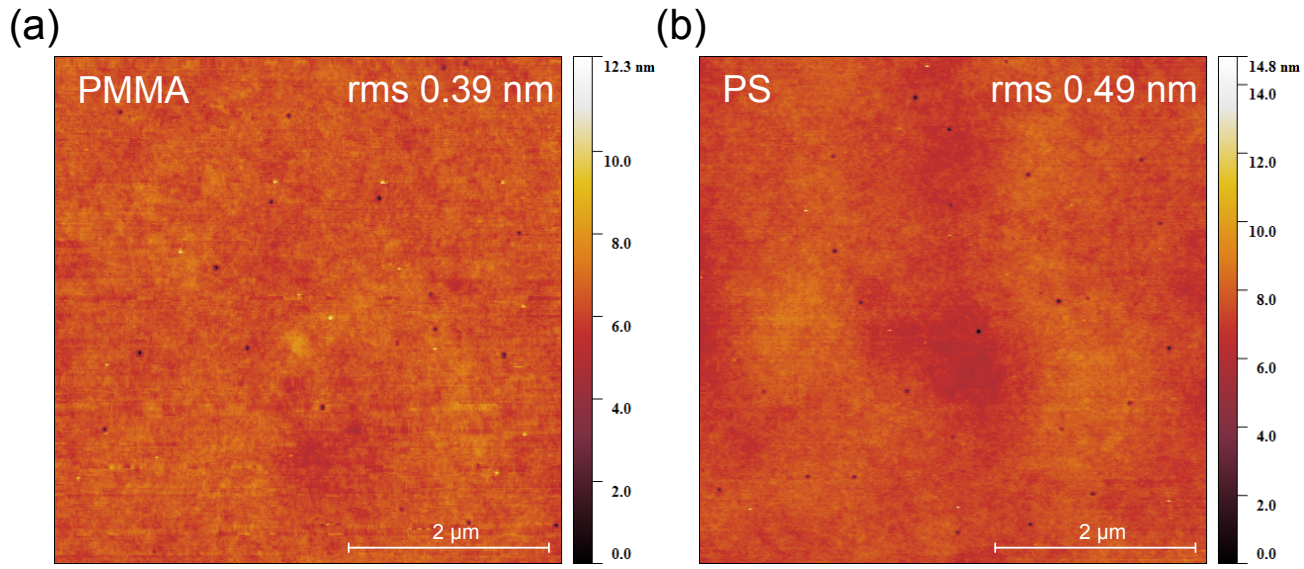

Figure 4.57: AFM images of the surface of PMMA (a) and PS (b).

The AFM images of show a very similar topography of both dielectric materials and the rms roughness of 0.39 nm for PMMA and 0.49 nm for PS are also very close. Therefore the interface between the organic layers and the top Au electrode should be of similar quality. Consequently the ZTO/PS and the ZTO/PAZ 14 interface must be of inferior quality compared to the ZTO/PMMA interface. A possible explanation could be found in the adhesion of the organic dielectric material to the ZTO surface. Contact angle measurements reveal a value of 45 °-51 ° for the printed ZTO film which means that the surface is quite hydrophilic. The result of the contact angle measurement can be seen in **Figure 4.58**. A good adhesion of the more polar material PMMA [143, 144, 145] compared to PS and PAZ 14 on an oxide surface is more likely and was reported in literature [146, 147]. Wu also explains that the polarity is a very important parameter in the wettability of polymers on a substrate [143]. The polarity of PMMA could account for hydrogen bonds to the ZTO [147] surface since it has, similar to the SiO_2 surface, most likely hydroxy groups at the surface as shown in **Figure 4.13**.

Because of the difference in polarity the adhesion of PS or PAZ 14 on the ZTO is not ideal. The resulting interface of inferior quality could affect the charge accumulation and consequently the saturation

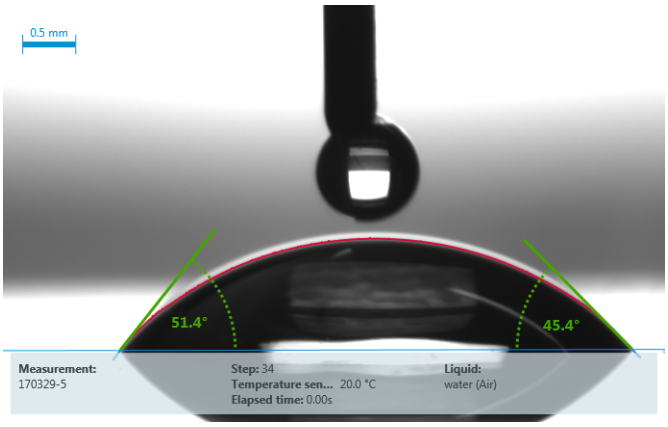

Figure 4.58: Contact angle measurement of a ZTO film consisting of two ink-jet printed layers on a glass substrate revealing a contact angle of 45.4 ° on the right side of the drop and 51.4 ° on the left side of the drop.

mobility. It was also reported in the literature that non-polar organic films could delaminate on the polar hydrophilic ZTO surface [148].

Taking everything presented in this section into consideration one can see that by processing thinner PMMA layers spin coated ZTO top-gate transistors with higher saturation mobilities could be achieved. The big drawback of the transistor with the thinnest PMMA layer is that it exhibits very large gate leakage. The top-gate device with 490 nm thick PMMA shows a similar saturation mobility but comparatively very small gate-currents. If top-gate transistors were processed using the ZTO solution with an EtOH to EG ratio of 1.5 to 1.0, transistors with a high saturation mobility could be processed. But these devices also show high off and gate-currents. Using new masks for the evaporation of the electrodes a smaller overlap between the gate electrode and the channel region as well as transistors with better performance could be realized. The best working device applying PMMA as a dielectric layer exhibit a saturation mobility of 4.41 $cm^2V^{-1}s^{-1}$. This device shows a small threshold voltage of 1.7 V and acceptable values of the on/off-current ratio and the subthreshold swing of 10^5 and 1.87 V/decade, respectively. ZTO top-gate transistors using PS or PAZ 14 as organic dielectrics show inferior device performance. This result could be explained by a better adhesion of the more polar PMMA compared to PS or PAZ 14 on the ZTO surface.

5 Conclusion and outlook

5.1 Conclusion

The scope of this thesis was to develop a precursor route for the processing of an amorphous oxide semiconductor (AOS), to analyze the resulting solution processed thin films, to build and characterize bottom-gate, bottom-contact transistors, and to evaluate the processed AOS in combination with various organic dielectrics in a hybrid organic-inorganic top-gate approach.

Zinc tin oxide (ZTO) was selected as the AOS material of choice since it does not contain the not so abundant indium. Using HCl as a stabilizer and oxidation agent long term stable precursor solutions could be obtained. By applying these precursor solutions, ZTO films were processed out of solution either by spin coating or ink-jet printing. The benefit of this route is its ease of processing, its environmental friendliness, and its cost effectiveness. The investigation of the ZTO films reveal their smooth and particle-like structure. Their structure was found to be mainly amorphous with the inclusion of small ZnO nanocrystallites. It could be shown that the investigated ZTO films are transparent and represent an n-type semiconductor.

The investigation of the factors influencing the precursor route and consequently the transistor performance indicate three main results. First, the devices with the best transistor performance have a weight fraction of Zn to Sn of 7:3. Second, in order to increase the viscosity of the precursor solution and consequently the printing performance, the introduction of a second solvent was investigated. The best performing transistors are realized if 40 vol% of ethanol is replaced by ethylene glycol. Third, it could be shown that by reducing the amount of HCl, which acts as an oxidation agent and stabilizer in the precursor route, transistors with better device performance can be processed. However, it has to be taken into account that a certain amount of HCl is necessary to guarantee long term stability of the solution.

In section 4.3 it was shown that by applying a multiple-layer approach the performance of printed ZTO transistors can be improved. Not only is the saturation mobility of the transistor increased as reported earlier in our group, but the threshold voltage can also be reduced. The best working device, composed of eight layers, shows a mobility of $7.8\,\mathrm{cm^2V^{-1}s^{-1}}$, which is to the best of the author's knowledge the highest reported value for an ink-jet printed ZTO transistor and was published in Applied Physics Letters. The beneficial multiple-layer approach is based on a better surface coverage degree of the SiO_2

layer and an improved film quality. In addition, transistors based on a higher amount of layers show a greater resistance against positive bias stress (PBS) compared to a single layered device.

Time dependent measurements revealed that the shortest switching time can be obtained if the ZTO TFTs operate in the linear regime. It could be shown that a device composed of two printed layers exhibits a shorter switching time compared to an eight layered device. The reason for this was shown to be a combination of a faster signal rise and charging of the corresponding capacitor. Both results could again be connected to the microstructure since the substrate of the two layered device is, in comparison with the eight layered device, not homogeneously covered.

Section 4.5 showed that this multiple-layer approach can also be applied in order to process ZTO transistors at a reduced annealing temperature of 350 °C. This temperature was selected because it is the highest temperature certain flexible substrates can sustain. The transistor composed of eight layers with a maximum mobility of $4.0\,cm^2V^{-1}s^{-1}$ exhibit superior performance compared to the transistors with two or four layers.

How atmospheric conditions affect the ZTO device performance was also analyzed. Transistors that are introduced into the glove box (GB) for measurements lead to severe performance degradation. However, this effect occurs especially if the SiO_2 substrate is not homogeneously covered with ZTO. Printed transistors composed of eight layers do not show this degradation. During a long term storage experiment of up to 700 days in the N_2 filled GB it could be shown that the threshold voltage as well as the subthreshold swing of a two layered device decreased. Both parameters are a measure of the amount of electron trap states at the semiconductor/dielectric interface. Their decrease reveal an improved interface between ZTO and SiO_2 which could be explained by the removal of adsorbed gaseous species like O_2 and H_2O. The increase of the on as well as the off-current during the storage time can be connected to the desorption of O_2.

Taking all results of the characterization of the bottom-gate, bottom-contact transistors into account, one can conclude that the application of the multiple-layer approach not only leads to better performance of the ZTO transistors in terms of electrical characteristics but also to an improvement against PBS and effects of atmospheric H_2O and O_2. **Figure 5.1** displays a model of how the ZTO film is supposed to look like if it is composed of less than four (a) or more than four layers (b). It shows a cross-sectional scheme of a bottom-gate, bottom-contact transistor where ZTO is applied for example by ink-jet printing. The model is based on the AFM images of **Figure 4.24**. In **Figure 5.1** (a) the applied ZTO does not cover the SiO_2 completely. The adsorption of small gaseous molecules (e.g. H_2O and O_2) at the SiO_2 surface could be a consequence. These molecules can either act as donors in the case of H_2O as discussed in **Figure 4.13** or as acceptors (O_2) as presented in **Figure 4.42**. These adsorption processes can be avoided if more than four ZTO layers are applied which results in a denser film, that completely covers

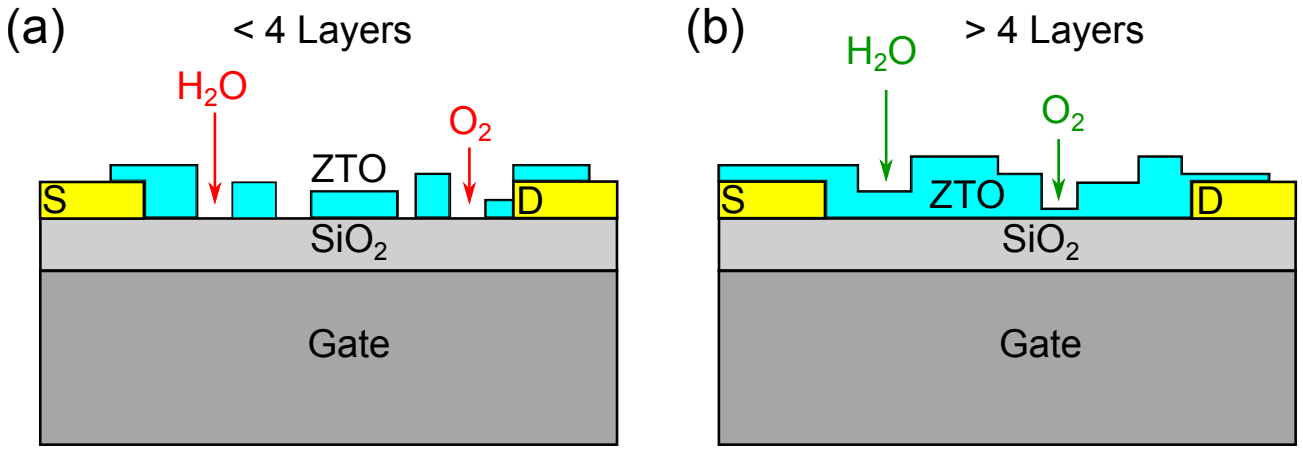

Figure 5.1: Scheme of bottom-gate, bottom-contact transistors with less (a), and more than four printed ZTO layers (b). In the first case the SiO_2 substrate is not completely covered by ZTO allowing gaseous molecules like H_2O and O_2 to be adsorbed at the SiO_2 surface. In the second case, although the ZTO surface is not smooth, it completely covers the SiO_2 layer. In this case H_2O and O_2 can not reach the dielectric/semiconductor interface anymore.

the SiO_2 substrate. This effect can also explain the improved *I*-*V*-characterisics and PBS resistance of ZTO transistors composed of multiple layers.

In section 4.7 it was shown that it is possible to process functional top-gate transistors using ZTO as the active material in combination with different organic dielectric materials. A certain minimum poly(methyl methacrylate) (PMMA) thickness is necessary to achieve good device performance while keeping the gate leakage low. The best working device processed by two spin coated ZTO layers and a 490 nm thick PMMA layer shows a mobility of 3.1 $cm^2V^{-1}s^{-1}$ which is similar to a value reported in the literature for a spin coated ZTO transistor using a PMMA dielectric layer. The drawback of these transistors is that they show large threshold voltages exceeding 25 V. By applying new electrode masks this value could be reduced to 1.7 V for an ink-jet printed top-gate transistor composed of four printed ZTO layers and a PMMA layer of 570 nm. This device exhibits a mobility value of up to 4.4 $cm^2V^{-1}s^{-1}$ which is, to the best of the author's knowledge, the highest reported value for a printed ZTO/PMMA top-gate transistor. Top-gate transistors using PS and PAZ 14 as organic dielectric materials have been realized but they show inferior device performance. This result has been explained by a better adhesion of the more polar PMMA dielectric compared to the polystyrene (PS) or benzyl azide containing copolymer (PAZ) 14 dielectric to the quite hydrophilic ZTO substrate.

5.2 Outlook

Certain aspects of this thesis should further be investigated. The results of section 4.5 suggest that it is possible to achieve good device performance at a reduced annealing temperature. Further experiments

using flexible substrates like polyimide (PI) would be necessary to decide if ZTO could also be applied as a material for flexible electronics.

The effect of different atmospheric conditions on the ZTO device performance should be analyzed in more detail. The investigation of different gaseous species, especially H_2O and O_2 in a chamber with controllable gas inlet system, would be preferable. The results obtained using such a chamber could be used determine the possibility of using ZTO as a gas sensing material.

Time dependent measurements could be performed on the hybrid ZTO top-gate transistors especially if the results are compared with measurements using other dielectric materials like high-*k* dielectrics (e.g. Al_2O_3 and HfO_2) or solid electrolyte gating materials. The latter material is widely processed in an in-plane layout where all three electrodes are located in the same plane. This layout in combination with ZTO, organic dielectrics or solid electrolyte gating materials could also be evaluated in terms of TFT performance and switching behavior.

List of Figures

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List of abbreviations

AFM	atomic force microscopy
Al	aluminum
AOS	amorphous oxide semiconductor
Au	gold
BSE	backscattered electrons
C	carbon
CBM	conduction band minimum
Cl	chlorine
DI	de-ionized
DOD	drop-on-demand
DOS	density-of-states
EG	ethylene glycol
EtOH	ethanol
FET	field-effect transistor
FH	Fraunhofer
GaAs	gallium arsenide
GB	glove box
Ge	germanium
GIXRD	grazing incident X-ray diffraction
H_2O	water
HBr	hydrobromic acid

HCl	hydrochloric acid
He	helium
HZTO	hafnium zinc tin oxide
In	indium
IGZO	indium gallium zinc oxide
ITO	indium tin oxide
IZO	indium zinc oxide
La	lanthanum
LVDT	linear variable differential transformer
MIM	metal-insulator-metal
MIS	metal-insulator-semiconductor
MOSFET	metal oxide semiconductor field-effect transistor
N	nitrogen
N_2	nitrogen
NMP	N-methyl-2-pyrrolidone
O	oxygen
O_2	oxygen
PAZ	benzyl azide containing copolymer
PBS	positive bias stress
PI	polyimide
PVD	physical vapor deposition
PMMA	poly(methyl methacrylate)
ppm	parts per million
PS	polystyrene

PTFE	polytetrafluoroethylen
RFID	radio-frequency identification
rms	root mean square
rpm	revolutions per minute
SEM	scanning electron microscopy
SE	secondary electrons
Si	silicon
SiO_2	silicon dioxide
Sn	tin
SnO_2	tin dioxide
TGA	thermogravimetric analysis
TCO	transparent conductive oxide
TFT	thin film transistor
TEM	transmission electron microscopy
UHV	ultra high vacuum
UDE	Universität Duisburg-Essen
UPS	ultraviolet photoelectron spectroscopy
UV-Vis	ultraviolet-visible
VBM	valence band maximum
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
Zn	zinc
ZnO	zinc oxide
ZTO	zinc tin oxide

Nomenclature

ε_0	Vacuum permittivity
ε_r	Relative permittivity
η	Dynamic viscosity
κ	Surface tension
λ	Wavelength
S.S.	Subthreshold swing
μ	Mobility
μ_{lin}	Linear mobility
μ_{sat}	Saturation mobility
Ω	Grazing-angle
Φ	Work function
ρ	Density
σ	Conductivity
τ	*RC*-time
Θ	Diffraction angle
A	Absorption
C	Capacitance
c	Vacuum velocity of light
C'	Areal capacitance
C_r	Imaginary part capacitance
C_r	Real part capacitance

d	Thickness of dielectrics
d_l	Layer thickness
d_n	Noozle diameter
e	Elementary charge
$E_{\mathrm{B(SK)}}$	Binding energy at secondary electron edge
E_B	Binding energy
E_C’	Edge of localized conduction band states
E_C^m	Mobility edge of conduction band
E_e	Electronic energy
E_F	Fermi energy
E_g	Band gap
E_ion	Ionization energy
E_kin	Kinetic energy
E_ph	Photonic energy
E_VAC	Vacuum level
E_V’	Edge of localized valence band states
E_V^m	Mobility edge of valence band
I_D	Drain-current
I_G	Gate-current
I_i	Imaginary part impedance
I_r	Real part impedance
k_B	Boltzmann constant
L	Channel length
n	Concentration of electrons

n_0	Equilibrium concentration
N_D	Donor concentration
Oh	Ohnesorge number
p	Concentration of holes
Q	Charge
q	Electric charge
Q_{inv}	Areal charge of the inversion layer
Q_{inv}	Charge in the inversion layer
R_q	Roughness
Re	Reynolds number
T	Transmission
t	ZTO film thickness
T_G	Glass transition temperature
t_t	Transit time
V	Voltage
v	Velocity
V_{DS}	Drain-source voltage
V_D	Diffusion voltage
v_D	Drift velocity
v_F	Fluid velocity
V_{GS}	Gate-source voltage
V_R	Retarding voltage
V_{th}	Threshold voltage
W	Channel width

We	Weber number
y	Channel depth
Z	Fromm number
$\mathscr{E}$	Electric field
h	Planck constant
tan δ	Loss factor
V_O	Oxygen vacancy
V_{Si}	Silicon vacancy

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2004 - 2006	R&D employee: PCI Augsburg GmbH
2001 - 2004	Apprenticeship: Chemical laboratory worker: PCI Augsburg GmbH
1997 - 2001	Secondary modern school: Realschule Bobingen
1991 - 1997	Elementary school: Grund- & Teilhauptschule Inningen

Internships

05/2012 - 07/2012	*Discrete element simulations and X-ray tomography observations of microstructures obtained by Electron Beam Melting*, GMP2 at SIMAP (Grenoble)
08/2010 - 09/2010	*Experimental studies of resistive switching in HfO_2 thin films*, EME at ANU (Canberra) with DAAD research grant

Publications & Conference contributions

Publications

B. Sykora, D. Wang, H. von Seggern
Multiple ink-jet printed zinc tin oxide layers with improved TFT performance
Applied Physics Letters 109, 033501, 2016

U. Hörmann, C. Lorch, A. Hinderhofer, A. Gerlach, M. Gruber, J. Kraus, B. Sykora, S. Grob, T. Linderl, A. Wilke, A. Opitz, R. Hansson, A. S. Anselmo, Y. Ozawa, Y. Nakayama, H. Ishii, N. Koch, E. Moons, F. Schreiber, and W. Brütting
V_{OC} from a Morphology Point of View: the Influence of Molecular Orientation on the Open Circuit Voltage of Organic Planar Heterojunction Solar Cells
The Journal Of Physical Chemistry C 118, 26462-26470, 2014

Conference contributions

Inorganic-organic bottom-contact/top-gate transistors based on ink-jet printed Zinc Tin Oxide and different organic dielectrics
Talk in the workshop on OTFTs, Sensors & Circuits 1, ISFOE, Thessaloniki, July 2017

Hybrid top-gate transistors based on solution processed zinc tin oxide and organic dielectrics
Talk HL 27.2, DPG Frühjahrstagung, Regensburg, March 2016

Non-toxic, cost-efficient precursor solution route for printed amorphous zinc-tin-oxide transistors
Talk C4.3 1230, FEMS Euromat, Warsaw, September 2015

Field-effect transistors based on printed amorphous zinc tin oxide
Poster HL 21.25, DPG Frühjahrstagung, Berlin, March 2015

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